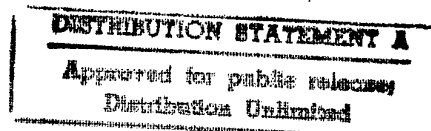


**** WOCSDICE 97 ****

**21st Workshop on Compound Semiconductor
Devices and Integrated Circuits**

May 25-28, 1997
Scheveningen, The Netherlands



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III-V's Review

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WOCSDICE 97

Programme

Sunday, May 25

19.00 Welcome Reception

Monday, May 26, morning

8.30 - 8.40 Opening and Welcome

8.40 - 10.10 Session 1: Reliability and Characterization

- 08.40 1. (Invited Paper) *F. Fantini, Parma University:*
"Reliability and degradation of HEMTs and HBTs"
- 09.10 2. *K. Lipka, P. Schmid, J. Ibbetson, N. Nguyen, U. Mishra and E. Kohn:*
"High Temperature Operation of GaAs Based HFET Structure Containing Layers Grown at Low Temperature".
3. *J. Grajal de la Fuente, V. Krozer, M. Schüßler, M. Brandt, H. Hartnagel:*
"Application of Semiconductor Interface Modelling to Reliability Characterisation".
4. *G. Meneghesso, G. Pelosi, A. Neviani, M. Hurt, X. Peatman, M. Shur, E. Zanoni:*
"Study of breakdown mechanism in 2D MESFETs".
5. *D.V. Morgan, Y.H. Aliyu and H. Thomas:*
"Metal probe technique for characterisation of semiconductor materials used in optoelectronic devices".
6. *S. Mohammadi, D. Pavlidis, B. Bayraktaroglu:*
"A Novel Approach for Determining the Reliability of AlGaAs/GaAs HBTs from Low-Frequency Noise Characteristics"

10.10 - 10.40 Coffee Break

10.40 - 12.35 Session 2: Optoelectronics

- 10.40 1. (Invited Paper) *M.K. Smit, Y.-S. Oei, Delft University, T. Staring, Philips Optoelectronics:*
"Photonic Integrated Circuits for multiwavelength applications"
- 11.10 2. *B.H.P. Dorren, A. Yu. Silov, M.R. Leys, J.E.M. Haverkort, J.H. Wolter, D.H.P. Maat, Y. Zhu, Y.S. Oei, F.H. Groen:*
"Polarization independent InGaAs/InP chopped quantum well interferometric space switch at 1.55 μm ".
3. *C. Llorente, R.M. Lorenzo, A. Sanz, I. De Miguel, E.J. Abril, M. López, M. Aguilar:*
"Design and analysis of a 1 x 8 wavelength division multiplexer based on the self-imaging theory".
4. *R.M. Lorenzo, C. Llorente, I. De Miguel, E.J. Abril and M. López:*
"Design and analysis of a 1 x 32 tapered coupler based on the self-imaging theory".
5. *R. Hakimi, B. Schmidt and M.-C. Amman:*
"Reduced Spectral Linewidth of Tunable Twin Guide Laser Diodes with Buried Facet Structure".
6. *W. Steffens and M.-C. Amman:*
"Effect of internal reflections on wavelength selectivity in widely tunable laser diodes".
7. *O.A. Tkachenko, D.G. Baksheyev and V.A. Tkachenko:*
"Irradiated quantum well in a potential step as photon source and electron pump".
8. *B. Willen, U Westergren:*
"HBT-based PIN diodes for high-speed OEIC-receivers".

12.35 Lunch

Monday, May 26, afternoon

14.00 - 15.30 Session 3: Integrated Circuits and Noise

- 14.00 1. (Invited Paper) *G. Gatti, ESTEC:*
"Space applications of GaAs MMICs"
- 14.30 2. *J. Berntgen, M. Heuken and K. Heime:*
"The influence of the cap layer on the low frequency noise of 2DEG structures".
3. *A. Matulionis, J. Liberis, I. Matulioniene, P. Gottwald, J. Karanyi, B. Szentpali, H.L. Hartnagel, K. Mutamba, A. Sigurdadóttir:*
"Hot-Electron Diffusion Coefficient in Standard Doped InP Channels".
4. *A.P. de Hek, F.L.M. van den Bogaart:*
"Broadband High Efficient X-band MMIC Power Amplifiers for Future Radar Systems".
5. *F.E. van Vliet, J.L. Tauritz, F.L.M. van den Bogaart:*
"On the Design and Application of Narrow tunable MMIC Filters".
6. *P. Marsh, D. Pavlidis:*
"Noise Analysis of InGaAs Mixer Diodes at Millimeter Wave and Far-Infrared Frequencies"

15.30 - 16.10 Coffee Break

16.10 - 18.00 Session 4: Quantum Effects and Tunneling

- 16.10 1. (Invited Paper) *K. Von Klitzing, Max Planck Institute Stuttgart:*
"Semiconductor quantum devices"
- 16.40 2. (Invited Paper) *M. Yamamoto, NTT System Electronics Labs.:*
"Resonant Tunneling Diode and HEMT Integrated Devices and Circuits".
- 17.10 3. *A. Sigurdardóttir, K. Mutamba, A. Vogt and H.L. Hartnagel:*
"Investigation on Tunnelling Effect in Stressed InAs/AlSb/GaSb-Resonant Tunnelling Diodes".
4. *M.I. Lepsa, Th.G. Van de Roer, J.J.M. Kwaspen, W. Van der Vleuten, L.M.F. Kaufmann:*
"Three Terminal Double Barrier Resonant Tunneling Devices Based on the Direct Contacting of the Quantum Well".
5. *Jozsef Karanyi and Bela Szentpali:*
"Quantum mechanical tunneling in GaAs ohmic contacts".
6. *J.J. M. Kwaspen, M.I. Lepsa, Th.G. Van de Roer, W. Van der Vleuten, H.C. Heyker, L.M.F. Kaufmann:*
"Accurate Equivalent-Network Modeling of GaAs/AlAs Based Resonant Tunneling Diodes with Symmetrical Thin Barrier and Spacer Layers"

19.00 Dinner

Tuesday, May 27

8.30 - 10.00 Session 5: Novel Techniques and Devices

- 08.30 1. (Invited Paper) *K. Ensslin, Swiss Federal Institute of Technology:*
"Ballistic electron transport in semiconductor nanostructures"
- 09.00 2. *Nils G. Weimann and Lester F. Eastman:*
"Effect of Threading Dislocations on the Electron Mobility in GaN and its consequences for Vertical Devices".
3. *P. Gluche, A. Aleksov, A. Vescan, W. Ebert and E. Kohn:*
"A Technical Approach Towards Diamond Power Transistors".
4. *G. Höck, A. Gruhle, T. Hackbarth, E. Kohn and U. König:*
"High Current Si_{0.3}Ge_{0.7} p-Channel Hetero MOSFETs".
5. *D.A. Romanov, E.B. Gorokhov, V.A. Tkachenko and O.A. Tkachenko:*
"Insertion of slipping planes in quantum well with 2DEG for creating one-dimensional -barriers".
6. *F. Ejeckam, Yu-Hwa Lo, M. Seaford, L.F. Eastman:*
"Lattice Constant Engineering Using Compliant Universal (C.U.) Substrates".

10.00 - 10.30 Coffee Break

10.30 - 12.30 Session 6: Field Effect Transistors and Diodes

- 10.30 1. (Invited Paper) *T. Enoki, NTT System Electronics Labs.:*
"InP-based HEMT ICs for ultra high speed optical communication systems"
- 11.00 2. *Helmut Brech, Thomas Simlinger, Thomas Grave and Siegfried Selberherr:*
"Influence of Gate length on the DC-Characteristics and f_T of Pseudomorphic Power-HEMTs".
3. *R. Fauquembergue, P. Desplanques, F. Dessenne and D. Cichoka:*
"Monte Carlo Simulation of III-V Nitrides FET's".
4. *F. Fumi, M. Peroni, C. Lanzieri, A. Cetrionia, A. Gasparotto:*
"Optimization of multifunction self-aligned-gate (MSAG) GaAs MESFET".
5. *D. Théron, S. Piotrowicz, X. Wallart, F. Diette, B. Bonte and Y. Crosnier:*
"InP based HEMT structures with a large bandgap barrier layer for power application in V band".
6. *Ferdouse Khaleque:*
"Room temperature InSb MISFETs".
7. *K. Lübke, T. Hilgarth, Ch. Diskus, A. Stelzer, A. Springer and H.W. Thim:*
"Zero-bias Detection with In_{0.38}Ga_{0.62}As Schottky Barrier Diodes".
8. *X. Mélique, E. Lheurette, P. Mounaix, F. Mollot, O. Vanbésien and D. Lippens:*
"InP-based Heterostructure Barrier Varactor".

12.30 Lunch

14.00 - ca. 23.00 Excursion and Banquet

Wednesday, May 28

8.30 - 10.00 Session 7: Heterobipolar Transistors

- 08.30 1. (Invited Paper) *D. Streit, TRW Electronic Systems* :
"HBT Production for commercial Applications:
Present and Future Trends"
- 09.00 2. *Burhan Bayraktaroglu*:
"Highly robust GaAs Cascode HBTs for microwave and millimeter-wave
application".
3. *A. Huber, C. Bergamaschi, T. Morf, H. Jäckel*:
"Low Frequency and Microwave Noise Performance of InP/InGaAs HBTs
as a Function of Bias-Point, Temperature and Emitter-Geometry".
4. *B.C. Lye, H.K. Yow, P.A. Houston, C.C. Button*:
"GaInP/AlGaAs/GaInP Double Heterojunction Bipolar Transistors with
Zero Conduction Band Spike at the Collector"
5. *A.R. St Denis and D.L. Pulfrey*:
"A microscopic view of quasi-ballistic transport in HBTs".
6. *R. Beccard, M. Volk, D. Schmitz, H. Juergensen, M.A. Knowles, D. McCullogh,
N. Pan and D. Hill*:
"Multiwafer Planetary Reactors: A tool for Reliable Mass Production of
HBT Wafers".

10.00 - 10.30 Coffee Break

10.30 - 12.15 Session 8: Technology

- 10.30 1. (Invited Paper) *L.F. Eastman, G. Martin, B. Pereiaslavets, M. Seaford, K. Chu,
Cornell University*:
"Optimization of Pseudomorphic MODFETs with Arbitrary Lattice Constants".
- 11.00 2. *A. Vogt, H.L. Hartnagel, M. Rodewald, H. Fueß, P. Ressel, K. Vogel, J. Würfl*:
"Pd-based Ohmic Contacts to GaSb".
3. *L. Cattani, M. Borgarino, J. Tasselli and A. Marty*:
"Minimum detectable outdiffusion length measurement for Be-doped
AlGaAs/GaAs HBT".
4. *D.W. Davies, D.V. Morgan and H. Thomas*:
"Characterisation of indium based ohmic contacts to GaAs using an ion-
assisted deposition technique".
5. *M. Chahoud, H.-H. Wehmann and A. Schlachetzki*:
"Anisotropic-etching simulation of InP".
6. *F. Dillmann, A. Brennemann, H. Hardtdegen, M. Marso, P. Kordos, H. Lüth,
F.J. Tegude*:
"Novel concept for an integrated photoreceiver based on selective
GaAs-epitaxy".
7. *Fedir V. Motsnyi*:
"Using of polariton and impurity photoluminescence for diagnostics of GaAs
semiinsulating substrates and structures on its base for transistor devices".

12.30 Lunch

End of Workshop

Monday, May 26

8.40 - 10.15 Session 1: Reliability and Characterization

08.40 1. (Invited Paper) *F. Fantini, Parma University:*
"Reliability of heterostructure devices"

09.10 2. *K. Lipka, P. Schmid, J. Ibbetson, N. Nguyen, U. Mishra and E. Kohn:*
"High Temperature Operation of GaAs Based HFET Structure
Containing Layers Grown at Low Temperature".

3. *Jesús Grajal de la Fuente, Viktor Korzer, Martin Schüßler, Michael Brandt and Hans Hartnagel:*
"Application of Semiconductor Interface Modelling to Reliability
Characterisation".

4. *G. Meneghesso, G. Peloso, A. Neviani, M. Hurt, X. Peatman, M. Shur, E. Zanoni:*
"Study of breakdown mechanism in 2D MESFETs".

5. *D.V. Morgan, Y.H. Aliyu and H. Thomas:*
"Metal probe technique for characterisation of semiconductor
materials used in optoelectronic devices".

6. *S. Mohammadi, D. Pavlidis, B. Bayraktaroglu:*
"A Novel Approach for Determining the Reliability of AlGaAs/GaAs
HBTs from Low-Frequency Noise Characteristics"

Reliability and degradation of HEMTs and HBTs

Fausto Fantini, Paolo Cova, Mattia Borgarino, Laura Cattani, and Roberto Menozzi

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The reliability of heterojunction devices, in particular HEMTs and HBTs, is quite a new item, so that research efforts are still mainly concentrated on the end-life problems. Electronic devices manufactured with compound semiconductors are quite different and numerous, so that the failure mechanisms too are various; nevertheless it is possible to identify some points in common with MESFETs [1], the most mature and widespread product in the compound semiconductors technology:

1. the absence of a natural surface passivation;
2. the impossibility to make a mono-metal system;
3. the low resistance to EOS/ESD.

On the other hand, since in HBTs the heterojunction may conduct high currents, they also exhibit degradation mechanisms similar to those of optical devices, in particular related to the growth of crystal defects.

In this paper we report on the reliability of HEMTs and HBTs, mainly looking at the end-life problems and related physical mechanisms. Not enough data have been collected up to now to give reliable figures on the failure rates. Nearly all the components here taken into account are based on GaAs substrates: only few results on InP based devices are available until now.

HEMT

During the last ten years the HEMT has substituted the MESFET in many applications, because of his higher speed, but the understanding of the failure mechanisms induced by stress tests and their relationship with failures occurring in operating conditions is still far from being complete and satisfactory. It is possible to group the observed failure mechanisms in four categories.

EOS, ESD, and burn-out. It is usually very difficult to analyse compound semiconductor devices failed in field for EOS (Electrical Over-Stress) and ESD (Electro-Static Discharge) because, due to their intrinsic weakness (very short and large channels, very short gate-drain and gate-source distances), they appear often completely destructed [2, 3]. The mode of failure is termed "burn-out", whereas the cause may be an EOS or an ESD, for which HEMTs have a very low threshold value (according with the Human Body Model), in the order of a few hundred volts, so that the handling precautions become mandatory for these devices. The high energy involved in the ESD phenomenon frequently induces

major damage in the devices, similar to that caused by surcharge effects, due to pulses that are quite common in the RF applications. However, burn-out can also occur in the absence of any overstress effect. The cause of the failure is usually a short-circuit between the electrodes under bias. The origin of the short is located either on the surface between the gate and drain, or at the interface between the channel and the buffer layer [4]. The mechanism can be either the semiconductor oxidation, with the consequent formation of GaO and then a metallic path, due to the excess As, or Au electromigration from the drain towards the gate, along the surface. In experiments made on AlGaAs/GaAs HEMTs [5] a degradation of the Schottky barrier after ESD stress was found.

Ohmic contacts. The Au-Ge-Ni multilayer is most frequently used. The failure mechanism is the increase of the resistance at high temperatures ($> 200^\circ\text{C}$), probably due to the Ga out-diffusion. The activation energy is very high, so that it is not easy to extrapolate these data to the operating conditions. This problem was experienced also in the ohmic contacts for power devices, but it is possible to overcome this limit by using large Au stripes, which are less sensitive to this phenomenon. It was recently claimed [6] the dependence of the degradation on the stress type: failure mechanisms in the case of high temperature storage, DC bias and DC bias with RF superimposed differ significantly and the contacts degrade more rapidly under RF life testing. Unfortunately no clear physical explanation of this behavior was proposed up to now. It was found a decrease in transconductance related to ohmic contact damage. RF life tests have also shown [7] a decrease of drain current, transconductance and gain and an increase in noise figure, attributed to gate metal (Ti/Pt/Au) interdiffusion and ohmic contact (Au-Ge-Ni) degradation. In [8] HEMTs were submitted to HTS and operating life tests and the degradation was associated with significant amount of Ga and As out-diffusion through the ohmic areas. A TiN barrier placed between the AuGe/Ni/Au contact and the Ti/Pt/Au overlay metal was found to be effective in eliminating this degradation and increasing the mean time to failure.

Schottky contacts. Even the gate contact degradation is less important than for MESFETs, due to the distance from the channel, the barrier height determines device characteristics. Various effects, depending on the barrier material, were found.

In [9] HEMTs with Al/Ti and Al/Ni Schottky contacts were compared by means of bias and thermal stress. For Al/Ti contacts, a decrease in barrier height was observed under storage tests up to 275 °C. The formation of metallic compounds, such as Al_3Ti , is believed to be responsible for this decrease. On the contrary, Al/Ni Schottky contacts showed an increase of the barrier height: either the migration of Ni into the Al film or the reaction of Ni with GaAs are possible explanations in this case [10]. As shown in the Arrhenius plot of Fig. 1, an activation energy $E_a=1.7$ eV was obtained.

At higher temperature (300°C) the reaction between Al and Au leads to the catastrophic failure well known as "purple plague".

Hot carriers. Interface states at the GaAs surface in the area between gate and drain and electron traps related to DX centers in the doped AlGaAs layer were indicated as the cause of parasitic effects, such as the presence of kink in the output characteristics. Moreover, these centers are responsible for the degradation of the transconductance for positive values of the gate voltage and they can affect the device life. The sensitivity of the HEMT drain characteristics to hot electrons and thermal stress cycles, due to the enhancement and depletion of these centers was observed [11]. It has also been observed a correlation between the "kink" effect and the variation of the frequency dispersion of the output conductance, attributed to that deep levels present in the AlGaAs layer.

Unpassivated AlGaAs/GaAs HEMTs showed rapid and irreversible degradation of the electrical characteristics, induced by hot electrons: decrease in drain current and increase in transconductance frequency dispersion [12].

In [13], it was reported that the gate breakdown voltage of an unpassivated AlGaAs/GaAs HEMT can move to higher negative values when a current is allowed to flow through the gate under reverse gate bias voltage. When a reverse bias is applied between the gate and source, this breakdown "walkout" can be accompanied by a permanent increase in device source resistance and decreases in g_m and I_{DSS} . A similar effect was observed in AlGaAs/InGaAs/GaAs PHEMTs and in GaAs MESFETs, but not in SiN passivated devices, so that an explanation could be the oxidation of the exposed AlGaAs/GaAs layers near to the recessed gate edges, where the electric field is the highest. The oxidation may result from the humidity present in the air and the avalanching process under a high reverse gate bias.

Studies on dual channel HEMTs ICs were performed [14], and the importance of the electron channels separation distance on the reliability of these devices was underlined. The failure mechanisms were trap generation at the donor layer-GaAs interface, increased impurity concentration in the GaAs separating the two channels and metal migration (Au), primarily from the ohmic contacts.

PHEMTs

An additional source of degradation for AlGaAs/InGaAs/GaAs PHEMTs could be the generation of traps in the InGaAs strained layer, due to the growth of edge dislocations in the [100] directions [15].

Lifetesting experiments [16] have been carried out in order to assess the stability of the InGaAs buried strained layer and related interfaces during operation, indicating that interfaces of InGaAs strained quantum well HEMTs do not induce particular degradations after 3000 hours into biased aging tests, although deep level centers appear in the n-AlGaAs layer.

Although aluminium molar fraction of PHEMT is lower than for lattice matched AlGaAs/GaAs HEMT, instabilities of the electrical characteristics induced by DX-centers, accelerated by the temperature, were recently found [17].

About the sensitivity of PHEMTs to hot electrons, tests on commercial devices [18] showed different behaviors. In some case it was found a recoverable (the devices recovered their original characteristics after some tenth of hours) increase of the drain current and consistent negative shift of the threshold voltage (Fig. 2), probably due to enhancement-depletion of traps below the gate; storage tests (without bias) at 180°C gave rise to the same results. This type of degradation has been recently demonstrated [19] to be in a strict correlation with the change of the RF direct gain S_{21} (Fig. 3). In other devices [20] a permanent gate-drain breakdown walkout appeared (Fig. 4); the explanation is that, possibly due to negative fixed charge generation in the gate-drain region, where the electric field is very high and impact ionization takes place, a new, more relaxed distribution of the field arises, increasing the voltage needed for the breakdown, so that it is possible to rise the level of the hot electrons stress (higher V_{DS}) and furthermore to increase the breakdown voltage.

HBTs

Heterojunction bipolar transistors have received considerable attention as devices for high speed and high frequency applications owing a number of advantages over other devices. A cutoff frequency f_t of 59 GHz and a maximum oscillation frequency f_{max} of 68 GHz have already been demonstrated in GaInP/GaAs system [21]. In spite of these very attractive performances, a lot of efforts are required in order to improve the device stability and reliability.

A primary reliability issue is the investigation of the base dopants stability, particularly Be and C. The most serious concern in using Be is the doping impurities diffusion from the base into the emitter layer during the transistor operation. The experimental data on the activation energy concerning the current peak degradation of tunnel diodes [22] and the numerical investigations concerning the DHBT degradation [23] suggest a recombination-enhanced diffusion of Be interstitials. The diffusion affects

the threshold voltage V_{BEth} , which is a parameter widely employed to monitor the device degradation during an accelerated lifetesting. An increase in the threshold voltage is usually reported as consequence of the Be diffusion towards the emitter layer [24-31]

A number of other related phenomena are reported such as an increase of the offset voltage [28], of the collector current ideality factor [28] and of the inverted collector current ratio [32]. Concerning the microwave characteristics, a decrease of the cutoff frequency f_t and an increase of the maximum oscillation frequency f_{max} were observed [28].

Several solutions have been proposed to improve the device stability.

An undoped setback layer placed between base and emitter is employed in order to reduce the impact of the diffusion on the electrical characteristics of the device. This is the case, even if a small negative shift of the threshold voltage can be observed, as shown in Fig. 5 [23].

Also a graded emitter layer reduces the sensitivity of the HBTs to the base dopant out-diffusion. Since the diffusion coefficient is inversely proportional to the gallium vacancies concentration [33] the Be stability can be improved by growing epitaxially the wafer with a high V/III beam flux ratio [34].

The dependence of the diffusion on the mechanical stress [25, 35] can be employed to improve the Be stability, as demonstrated in [36] and more recently in [37], because the finite mechanical strain, induced by a superlattice structure at the emitter-base junction, inhibits the diffusion of interstitial atoms.

In a recent work [38] it was suggested that a Be concentration of 10^{19} cm^{-3} should be considered an upper limit to the base dopant level concentration for the fabrication of a reliable device. In light of these considerations other materials were used as an alternative p-type dopant to Be, such as C and Zn [39]. The behavior of C-, Zn-, and Be-doped base HBTs ($C=5 \times 10^{19} \text{ cm}^{-3}$, $Zn=4 \times 10^{18} \text{ cm}^{-3}$, $Be=4 \times 10^{18} \text{ cm}^{-3}$) was compared under identical bias stress conditions. For both Zn- and Be-doped devices a significant shift in V_{BEth} was observed together with a decrease in gain. No significant change was detected for C-doped base devices. Therefore an attractive choice for HBTs using a very high base dopant concentration is carbon, thanks of his very low diffusion coefficient [26, 40]. This is likely a consequence of the fact that C occupies the As rather than the Ga sublattice, as in case of the Be impurities [41]. In spite of his low diffusivity, the C atoms suffer from a stability problem due to his inclination to the formation of C-H complexes [42] in presence of hydrogen contamination. SIMS analysis demonstrated that hydrogen is incorporated during MOCVD growth [43-46] and also that it can be absorbed during a plasma deposition of SiN_x [47] or introduced by a H^+ implant isolation [48]. The effect of a carbon passivation by H atoms is a time-dependent current gain, a behavior which

negatively affects the device reliability. A decrease of the current gain was ascribed to the debonding of H from the C acceptors, probably enhanced by minority carrier injection [42]. This mechanism should give rise to an increase of the effective base doping [43, 45]. During current stress tests of C-doped HBTs an initial current gain increase has also been observed [43, 49, 50], as reported in Fig. 6. This behavior has been explained by the reduction of recombination centers involving hydrogen atoms [49] and it seems to affect also the low frequency noise spectra of the HBT [50].

The use of carbon as base dopant may originate not only hydrogen related instability. Due to the small covalent bonding radius of C [51], a high carbon concentration is responsible for a lattice contraction. The associated lattice mismatch induces a mechanical stress, that can affect the HBT reliability, as already observed in the case of the laser [52]. This agrees with the reliability similarities between HBT and laser proposed in [38]. The codoping with indium of heavily C-doped base layer releases the strain induced by the C impurities and therefore improves the HBT stability [53].

About ohmic contacts in HBTs, the main issue is the increase in the contact resistance during device operation. A number of metal systems has been proposed for both p-type and n-type ohmic contacts either alloyed or non alloyed and investigated under thermal stress.

AuGe/Ni/Ti/Au alloyed contacts to n-type GaAs, degrade under thermal stress. Ga and Au interdiffusion is believed to be responsible for this degradation [31]. In AuGe/Ni/Ti/Pt/Au contacts, the insertion of Pt contributes to block Au diffusion. Thickness lower than 50 nm leads to an improvement of the contact stability [54].

Systems using refractory materials were also investigated for p-type contacts, such as Pt/W/Ag, Pt/Zn/Au and Pt/Ti/Pt/Au. Not only do these contacts provide low resistivity, but they are also reliable under thermal stress [55].

An important issue is that associated with base contact penetration. The base layer of high performance HBTs is usually designed with a thickness lower than $0.1 \mu\text{m}$. Hence it is essential that the metal system used for the base contact is stable under operating condition. The penetration of the base metal through the base layer leads to a serious degradation of the B-C junction or even to his short circuit. Different metal systems (Pt/Ti, Au/Ti, Au/Pt/Ti) have been compared in order to identify a low resistance and reliable contact. The use of refractory metals (such as W) as a diffusion barrier permits to improve the contact stability under thermal stress [56].

InP based devices

InAlAs/InGaAs on InP HEMTs studies [57] showed that, by reducing the channel thickness, the reverse

gate breakdown voltage improves and this effect was attributed to the increased effective bandgap resulting from energy quantization in the channel.

In [58] it has shown a good reliability of these devices when WSi ohmic contacts are employed, because of the good stability of this alloy under high temperatures (170-200 °C), although Ti and F, detected in the InAlAs layer after the life tests, should cause a decrease of carrier concentration in the epitaxial layer.

About hot electron effects on InP based HEMT, it has recently been found [59] a behavior similar to that of PHEMT, with a reduction of the transconductance at high V_{GS} values, probably due to surface degradation correlated, also in this case, with the RF characteristics change.

Surface degradation, in this case after thermal stress, has been found in [60], attributed to lattice disorder induced on the surface of InAlAs, probably by either the introduction of vacancies or indium segregation. This degradation was suppressed by passivating the devices with SiN. Thermal stress tests have also produced g_m and I_{DSS} decrease, and catastrophic failure, due to migration of ohmic metal from the contacts to the gate [61].

In [62] it was found a reliability improvement of InP based HEMTs, by adding 10% Ga to the InAlAs layer, likely due to the high mobility of Ga atoms during MBE growth, resulting in a reduction of the cluster formation in the InAlGaAs layer.

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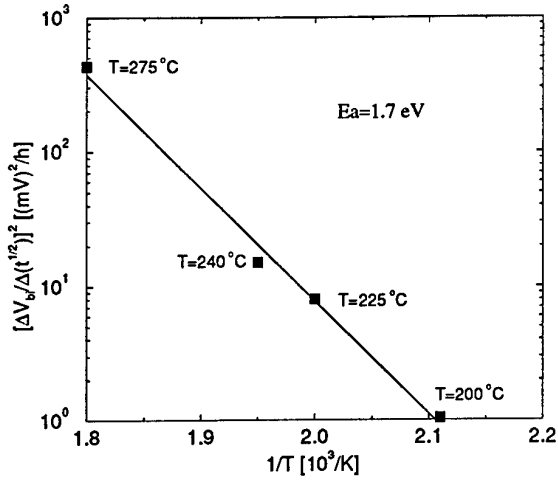


Figure 1: Arrhenius plot for the degradation of V_{bi} of HEMTs stressed at various temperatures.

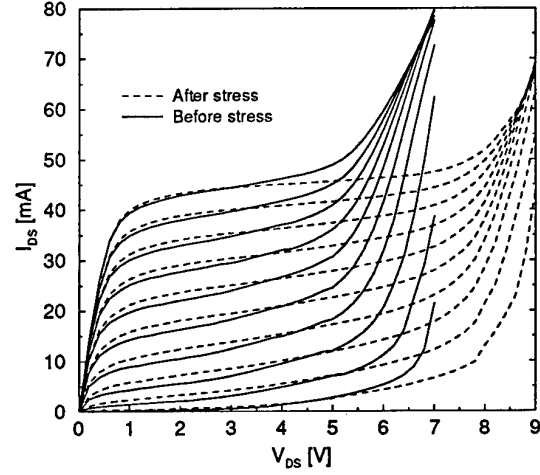


Figure 4: Breakdown walkout of a PHEMT after hot electron stress.

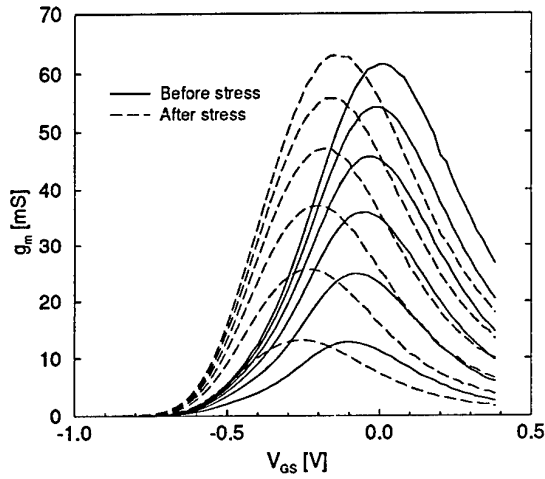


Figure 2: Variation of the transconductance curves of a PHEMT after hot electron stress test, due to trapping-detrapping phenomena under the gate.

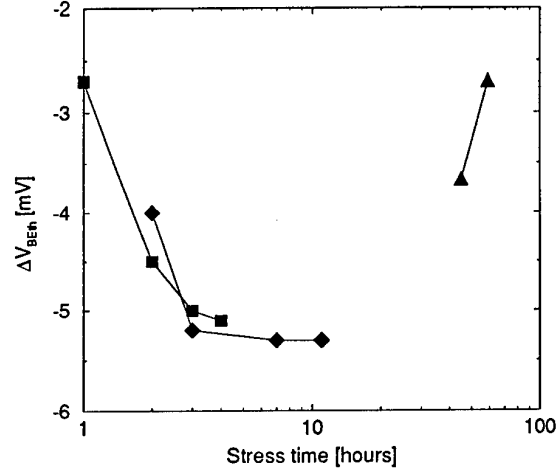


Figure 5: Negative shift of V_{BE} for three Be doped HBTs stressed at room temperature with $J_C = 10^4$ A/cm².

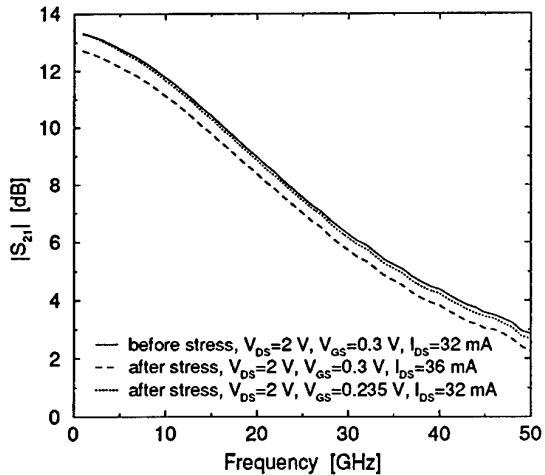


Figure 3: Magnitude of S_{21} , measured at $V_{GS} = 0.3$ V, $V_{DS} = 2$ V, versus frequency, before and after hot electron stress.

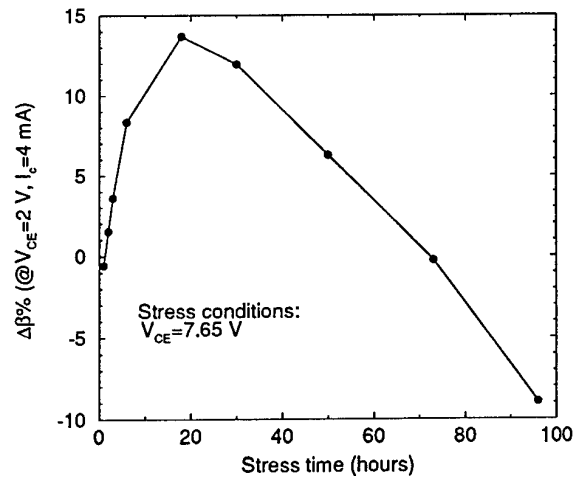


Figure 6: Current gain β versus stress time for a carbon doped HBT.

High Temperature Operation of GaAs Based HFET Structure Containing Layers Grown at Low Temperature

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Abstract

Operation at elevated temperature is one of the important parameters of sensor applications in harsh environment. In many cases the temperature limit is imposed by that of the associated electronic semiconductor device, where the limit is frequently associated with the intrinsic carrier activation by the band gap. However, although operation at 500°C has been demonstrated with GaAs based FET devices, the present limit is still determined by the contact stability, defect activation in the Schottky barrier and the semi-insulating substrate and the degradation of the carrier mobility in the channel [1].

In this approach a heterostructure FET technology will be discussed, where operation up to 500°C has resulted in only minor changes in the maximum drain current, threshold voltage and sub-threshold leakage current (see figs. 1a and 1b).

The device cross section is shown in fig. 2. Two Low-Temperature-Grown (LTG)-materials are implemented: an LTG-AlGaAs surface and Schottky barrier layer on top of the channel and an LTG-GaAs buffer layer. Ohmic and Schottky contacts have been fabricated using standard material systems of Ni/Ge/Au and Ti/Pt/Au. The penetration of the ohmic contact material into the heterostructure upon temperature stress is controlled by the AlAs diffusion barrier below the channel. The Schottky metal / LTG-AlGaAs semiconductor interface is believed to be formed by a Ti:Al:As intermetallic compound similar to that used to stabilize Ti:Al contacts to GaAs [2]. The buffer layer leakage is reduced and stabilized by using LTG-GaAs, which is known to produce an extremely high resistivity [3].

In the experiment the device was held at a temperature above 500°C for approx. 30 min. At 540°C the Schottky diode shunts through and becomes conductive. Thus channel modulation collapses. However upon cooling to approx. 500°C, the original characteristics are restored. Only at 570°C the contacts degraded permanently destroying the device. This may even be pushed out further by employing refractory metallization concepts based on Si and W.

The criteria for the high stability in performance for operation up to very high temperatures, like the 500°C applied here, will be discussed. Optimized GaAs based FET devices may be capable to operate at very high temperatures even above 500°C.

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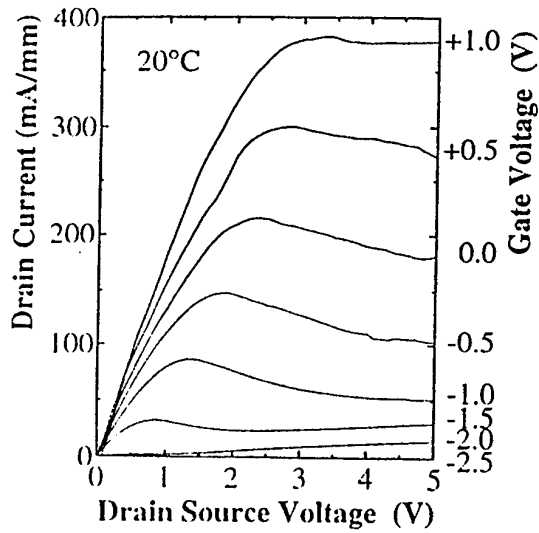


Fig. 1a
 Output characteristics of 1 μ m gate
 length HFET Structure at 20°C

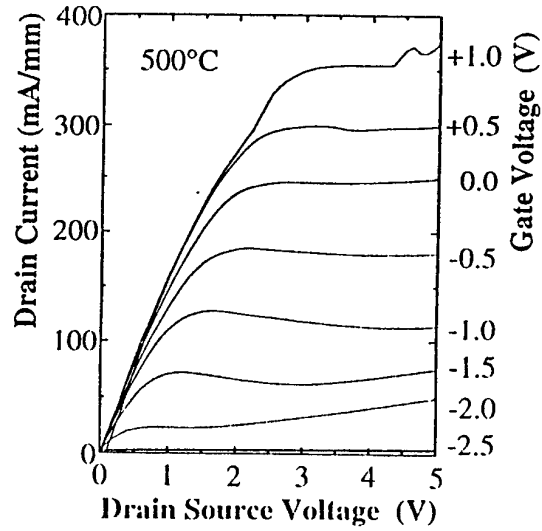


Fig. 1b
 Output characteristics of 1 μ m gate
 length HFET Structure at 500°C

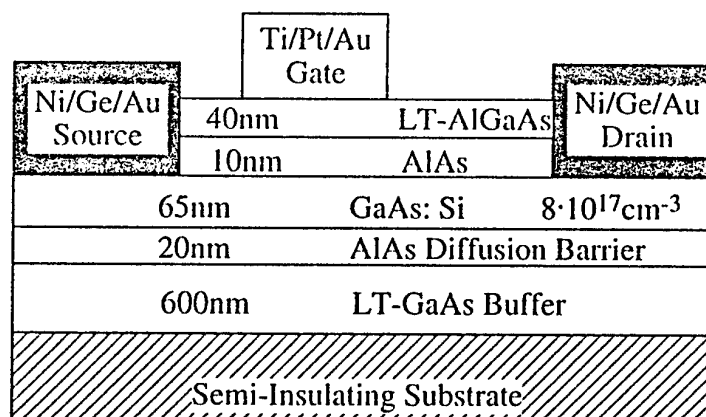


Fig. 2
 Device cross section

Application of Semiconductor Interface Modelling to Reliability Characterisation.

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Characterisation of the reliability of semiconductor devices by the physics of failure approach is of increasing interest in semiconductor research. Considerable effort is being made to reduce the reliability qualification phase in the development of devices and circuits. The two main activities in this area are the accelerated lifetime tests and the prediction of reliability at the design stage. The former is oriented towards the measurement of the final product reliability. The latter is based on the concept of design-for-reliability. The physics-of-failure requires a physical understanding of the mechanisms affecting reliability, and the development of models based on physical considerations to enable accurate prediction of reliability. Numerical modelling is an adequate tool to undertake electrical and reliability characterisation of semiconductor devices. The most important physical mechanisms can be included there in predictions of the reliability. However, little progress has been made in incorporating failure mechanisms into the numerical simulation of reliability [1]. Our aim is to show that the accurate modelling of the interface between different materials can be used to explain theoretically the experimentally observed junction degradation. Our numerical model for the carrier transport in bulk semiconductors is based on the classical drift-diffusion formulation. The interface condition for the Poisson equation takes into account discontinuities in the band structure and localized states at the interface. For the carrier continuity equations the transport across the interface is described by thermionic emission, self-heating effects and an exact solution of the Schrödinger equation [3]. The new model is used to analyse the temperature dependent behaviour and the contribution of surface charge densities at the interface to the operation of heterojunction bipolar transistors. To demonstrate the usefulness of the proposed approach an abrupt $Al_{0.42}GaAs/GaAs/Al_{0.2}GaAs$ DHBT is considered. Figure 1 shows measured and simulated Gummel-plots at 500 K respectively for three different surface charge densities σ at the emitter-base interface. The different performances can be explained by the modification of the band diagrams[4]. The surface charge density changes the distribution of the potential drop on both sides of the heterojunction. Thus, different transport mechanisms can limit the transport through the interface.

- drift-diffusion in the emitter space charge region for positive charges due to the effective barrier reduction, and
- thermionic emission for negative charges due to the effective barrier enhancement.

No parameters have been changed in the simulation at this temperature apart from the material constants. It is demonstrated that this particular HBT device incorporates a negative surface charge at the heterointerface. The polarity and the magnitude of the charge cannot be distinguished from the base current for negative charges, but is easily identifiable from the collector current in the Gummel plot. The presented results contribute also to the understanding of the mechanisms taking place during device ageing. In such situations an initial shift of the collector current towards larger voltages can be observed experimentally and could be explained by the creation of negative surface charges. Square pulses have been applied to a SHBT $Ga_{0.5}In_{0.5}P/GaAs/GaAs$ [5, 2]. The experimental results and the simulations are depicted in figure 2. Interface charges can be used to explain the degradation of the collector current. The creation of interface charges can be explained

as defects between different materials or junctions. The interface charges can be generated by a mismatch in the crystal structure (the traps were already existing and have been emptied by the stress), or could be created by the application of stress. It is important to observe that the creation of traps continues gradually with applied electrical stress until ultimately the junction is destroyed. Interestingly even in the case of severe damage the principal operation of the junction can still be observed when stressed with electrical pulses. This indicates that the degradation has a spot nature rather than a global degradation of the material. The good agreement between simulations and experimental results indicate that the interface charges are a good candidate to explain the degradation at the heterojunction under electrical stress.

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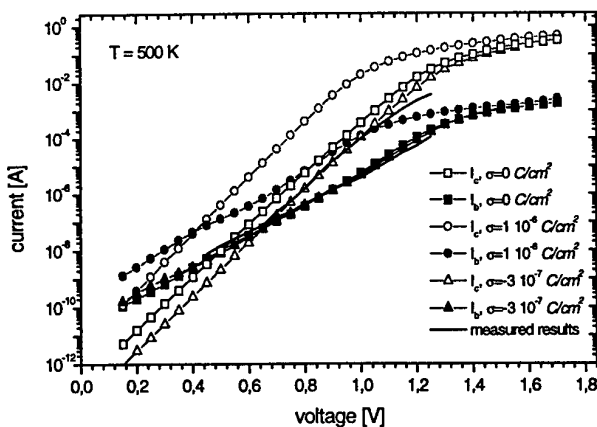


Figure 1. Gummel plots for 500K

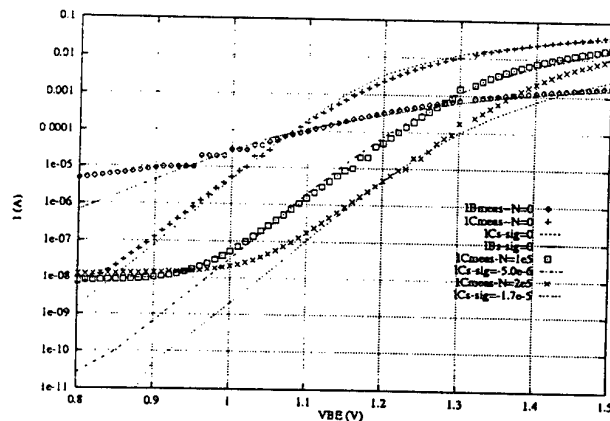


Figure 2. Gummel plots for reliability.

Study of breakdown mechanism in 2D MESFET's

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A novel, laterally gated FET named two dimensional MESFET (2D-MESFET's) has been recently presented by Peatman and coworkers [1]. The 2D-MESFET's side contacting gates establish a lateral metal/two-dimensional electron gas junction [2], a geometry which is fundamentally different from conventional FET devices.

In this work we have characterized and studied the impact-ionization-induced instabilities in the output characteristics of these devices. The instabilities appear as an increase of the output conductance, g_D . Based on the value of g_D , the output characteristics can be separated into three different regions, each corresponding to a different impact ionization regime: Region I, no impact-ionization and very low values of g_D ; Region II, starting of impact-ionization regime (pre-avalanche) and corresponding slight increase of g_D ; Region III, onset of carrier avalanche and consequent large increase in g_D . In support of this picture we observed the same correlation between impact ionization and g_D also changing device biasing and temperature.

Fig.1 reports the schematic cross section of a typical device indicating the new approach in the device layout: two lateral gate substitute the top single gate usually adopted in conventional devices. Fig.2 reports typical I_D , I_G vs. V_{DS} characteristics for different V_{GS} . In the same figure the three regions characterized by different values of g_D are separated by dashed lines. In order to understand the correlation between the observed g_D behaviour and impact ionization let us consider the I_D , I_G vs. V_{DS} curves at a single value of $V_{GS} = -0.3$ V. The $|I_G|/I_D$ ratio as a function of $1/(V_{DS} - V_{DSsat})$ evaluated at $V_{GS} = -0.3$ V is depicted in Fig.3. In the impact ionization regime the ratio $|I_G|/I_D$ is proportional to $\exp[-L_{eff}/(V_{DS} - V_{DSsat})]$ [3] where L_{eff} is the region where impact ionization can be assumed to take place, and it is characterised by an effective electric field with a value [3,4] $E_{eff} = (V_{DS} - V_{DSsat})/L_{eff}$. The $|I_G|/I_D$ ratio is dominated by impact ionization for high V_{DS} , that is, in the range $1/(V_{DS} - V_{DSsat}) < 0.15$ V⁻¹. Dashed line in Fig. 3 represents the best fit of $|I_G|/I_D$ in this region according to the exponential law shown in the inset. This relation allows us to evaluate the contribution of impact-ionization even when it is remarkably smaller than the reverse current. At low V_{DS} , in fact, $[1/(V_{DS} - V_{DSsat}) > 0.15$ V⁻¹], the experimental data depart from the exponential law because in this range I_G is dominated by the gate diode reverse current. By using the data extrapolated by the dashed line of Fig.3, it can be seen in Fig.4 that the onset of impact-ionization occurs at $V_{DS} \approx 4$ V which corresponds to the first kink voltage. This means that the first kink is linked with the starting of impact-ionization (region II). In Fig.4 it can also be seen that the second kink (region III) starts when impact ionization becomes very high (higher than the leakage current), i.e. $\text{Log}[|I_G|/I_D] > -3$ or $|I_G|/I_D > 10^{-3}$, at $V_{GS} = -0.3$ V. We can in this way correlate the increase of the g_D with the different impact-ionization regime: I) no impact-ionization; II) starting of impact-ionization regime (pre-avalanche); III) starting of avalanche. The Region III can be better understood by looking at Fig. 2 where $|I_G|$ current is plotted in linear scale and the strong increase of I_G coincides with the second kink.

Reporting the same extrapolation procedure, above described, for different values of V_{GS} , (see Fig.5), and for different temperatures, see Fig.6, a good correlation between kinks in I_D and the onset of pre-avalanche and avalanche regime is still observed.

As a last remark, it can be observed that the V_{DS} value at which the second kink (Region III) occurs decreases on increasing the drain current (biasing V_{GS} more positive), see Figs. 2 and 5. On the other hand the "sharpness" of the kink increases on lowering I_D (towards pinch-off). This behaviour suggests a positive self limited feedback mechanism similar to what happens in SOI-MOSFET's [5]. In SOI-MOSFET's holes generated by impact ionization raise the body potential thus reducing the threshold voltage and leading to a sudden increase in I_D . This positive feedback mechanism is quenched by the increase of drain saturation voltage V_{DSsat} (due to the increase of body potential), which reduces the electric field. A similar effect can occur in the 2D-MESFET's due to the accumulation of holes generated by impact-ionization.

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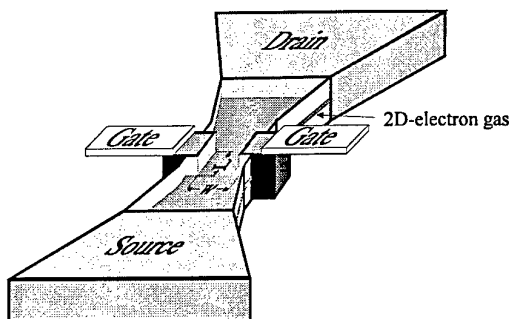


Fig.1 Schematic view of novel 2D-MESFET's

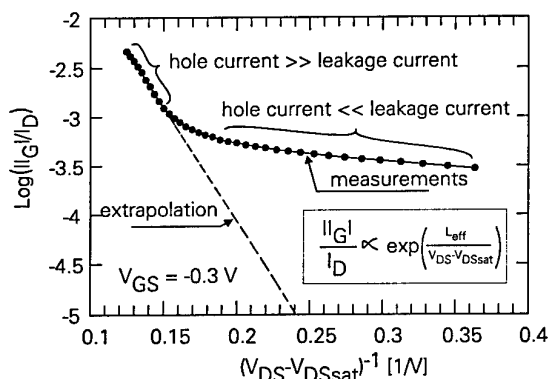


Fig.3 $|I_G|/I_D$ plotted against $1/(V_{DS}-V_{DSsat})$. Exponential dependency of the current ratio at high drain bias indicated impact ionization occurring in the channel

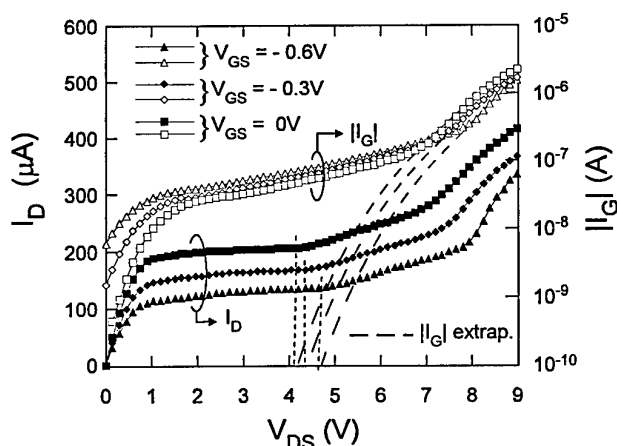


Fig.5 I_D and I_G vs. V_{DS} evaluated at different V_{GS} . The extrapolated data indicate the correspondence between impact ionization and regions I, II, and III (or kinks).

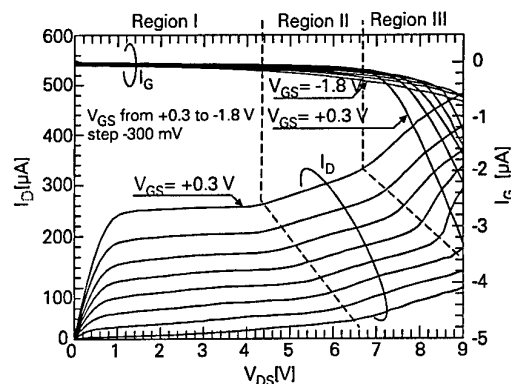


Fig. 2 I_D and I_G vs. V_{DS} for 2D MESFET. Applied V_{GS} ranges from -1.8 V to 0.3 V (step 0.3 V).

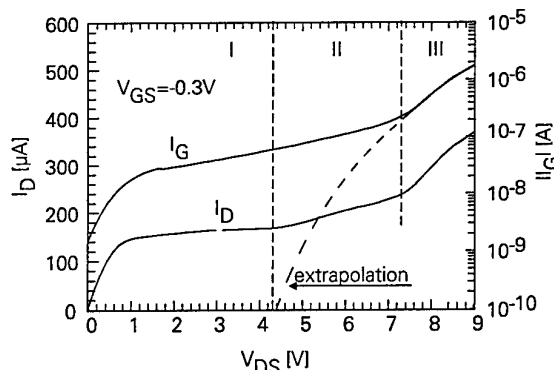


Fig.4 I_D and I_G vs. V_{DS} evaluated at $V_{GS} = -0.3$ V. Data extrapolated in Fig.3 are also depicted and the correspondence between impact ionization and different regions is clearly visible

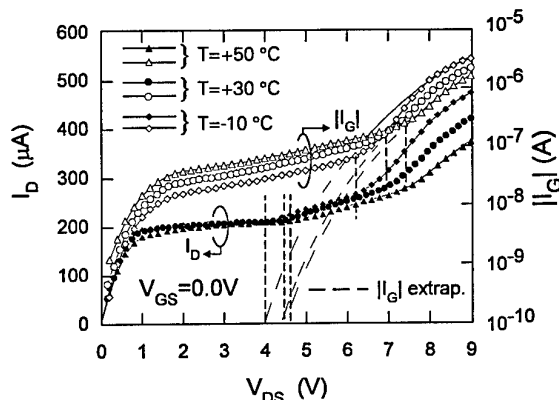


Fig.6 I_D and I_G vs. V_{DS} evaluated at different temperature. Correlation between impact ionization and kinks is still present.

METAL PROBE TECHNIQUE FOR CHARACTERISATION OF SEMICONDUCTOR MATERIALS USED IN OPTOELECTRONIC DEVICES

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High quality optoelectronic devices are required for further development and improvement of visible displays and optical fibre transmission systems. Light emitting diodes, laser diodes and photodetectors have become very important key components and are indispensable in these systems. Photoluminescence (PL) technique is extensively used to characterise semiconductor wafers for optoelectronic applications. The technique is based upon the radiative recombination of excess carriers which have been generated by the absorption of light from an external source. The problem that has been experienced in practice is the lack of correlation between the PL intensity from the semiconductor layers and the electroluminescence observed from full LED or laser diodes fabricated from such layers.

This paper presents a technique for the rapid evaluation of the wafers grown for fabricating LEDs or laser diodes. High-brightness visible light emitting materials based on the $(\text{Al}_x\text{Ga}_{1-x})_{0.5}\text{In}_{0.5}\text{P}$ quaternary alloy lattice matched to GaAs were used for these investigations. This is an important material system because its direct band gap energy extends from 1.8 up to 2.3 eV, as the aluminium composition x , increases from 0 to 0.7 [1-2]. This property makes AlGaInP an excellent material for efficient double heterostructure LEDs and Laser diodes with a wide colour range. The epitaxial layers were grown on n^+ -GaAs substrates by low pressure Metal Organic Vapour Phase Epitaxy (MOVPE). Photoluminescence measurements were made using an Ar^+ ion laser (514 nm) for electron excitation with a power range of 0 to 100 mW. EL measurements were made using a Keithley 238 Current-Source Measurement Unit which biases the devices, using CW or Pulse modes. A Keithley 199A Scanner was connected to a calibrated Silicon detector through a transimpedance amplifier to convert the detector current into a measurable voltage. Figure 1(a) shows the PL intensity plotted against the full device EL data measured at 20 mA for a typical LED. Each data point on the curve represents a different material structure. The scatter of results and variation of both EL and PL outputs illustrates the lack of correlation between the two techniques and hence PL alone cannot be used to qualify layers grown for LEDs or lasers. These results suggest that there is a need for alternative rapid characterisation technique which will give data that correlates well with the actual device electroluminescence performance. Preliminary studies were carried out by melting Indium wire using a standard soldering iron to form a surface contact. The material was firstly cleaved into a 3.0 mm x 3.0 mm size samples. Indium dot contacts with a diameter of about 0.5 mm were then applied on the front and rear surfaces of the material using a fine solder tip (0.5 mm). The most significant parameters in this study are the length of time (about 15 seconds) that the tip of the soldering iron was left in contact with the front

the length of time (about 15 seconds) that the tip of the soldering iron was left in contact with the front surface to form the Ohmic contact and the size of the diced sample. The samples were forward biased and the light emitted was collected using a calibrated silicon detector positioned close to the chip on a probe station. The EL from the indium dot devices are compared with those from the data collected from full processed diodes. The measured light intensities of the Indium dot contacts correlates well the relative EL intensities obtained from full diode structures as can be seen with the least square fit to the data in Figure 1(b). The main disadvantage of the indium dot contact method is that it requires cleaving of the LED wafer into small regular sized pieces and careful application of the indium contacts on the front and rear of the wafer. The process is time consuming and destructive in the sense that wafer dicing is needed and the indium dots are difficult to remove after measurements. It is therefore not a practical wafer qualifying technique. The success of the indium dot technique led to the development of an metal probe technique which offers all the advantages and without the disadvantages identified above.

In the metal probe technique a metal finger is used to contact the (surface) p-side of the sample while the n-side (rear) is placed on a metal base. The probe is biased through the electrical connections at the base and the light is coupled from a hole in the finger and collected. The results for the 1.0 mm diameter hole are compared with the EL data of a full diode in Figure 2(a). The relative intensities of the samples measured using this technique are in a very good agreement with the measured EL values of the full diodes. Furthermore, the optical arrangement is such that the light emitted can be coupled in a spectrometer to perform Spectral Response(S-R) measurements to determine the emission wavelength as a function of the relative light intensity. Inset in Figure 2(b) shows a typical measured S-R plot.

The technique is simple, and can be used to qualify LED or laser wafers. The technique also allows a non destructive testing of variations in EL across a sample (i.e. emission intensity and wavelength). It reduces the long and costly fabrication process time required for producing a fully processed LED, thus allowing device processing to be carried out only on good layers.

ACKNOWLEDGEMENTS

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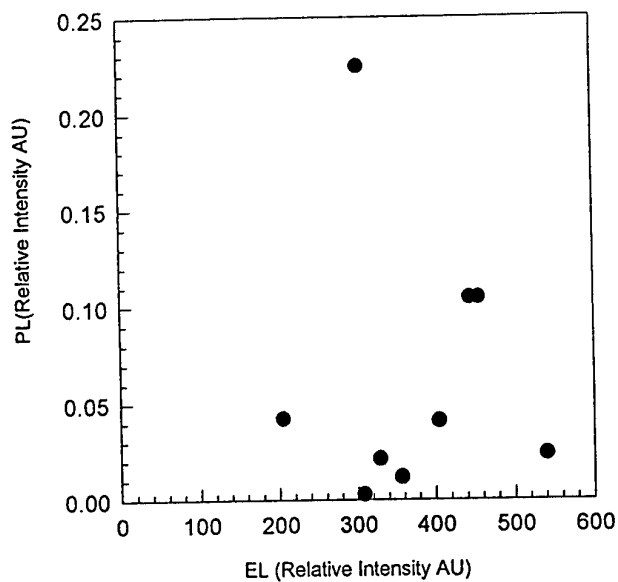


Figure 1(a): Plot of PL intensity against full device EL data measured at 20 mA.

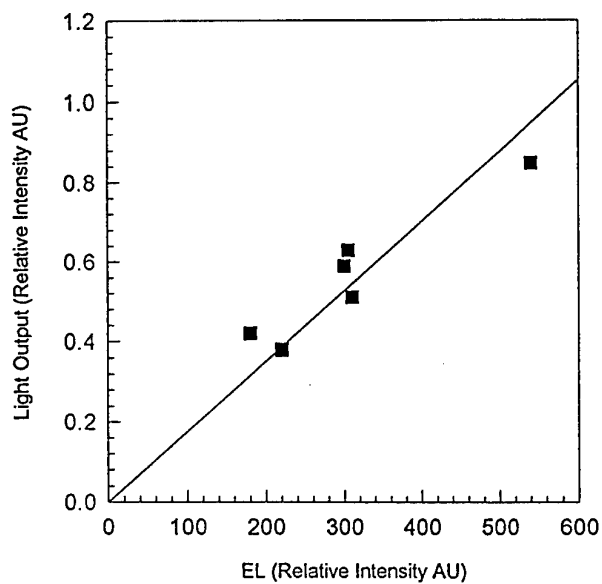


Figure 1(b): Plot of EL output from indium dot devices compared with EL measured from a full processed device

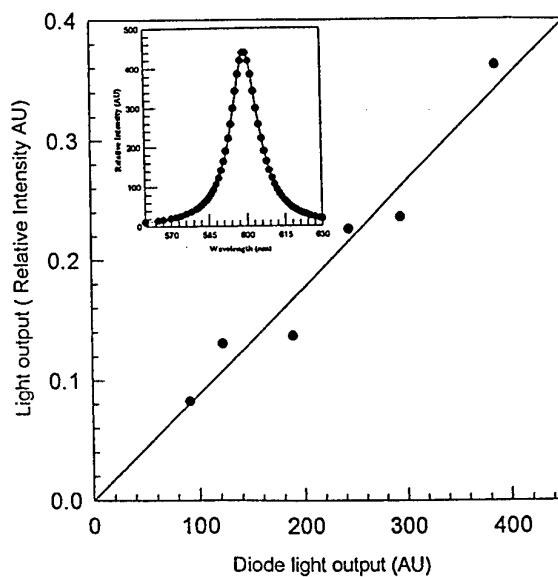


Figure 2(a): Plot of light intensity measured using metal probe against EL measured from a full processed device (Insert) Figure 2b shows a typical S-R plot measured using the metal probe.

A NOVEL APPROACH FOR DETERMINING THE RELIABILITY OF AlGaAs/GaAs HBTs FROM LOW-FREQUENCY NOISE CHARACTERISTICS¹

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Several studies have addressed the reliability characteristics of AlGaAs/GaAs Heterojunction Bipolar Transistors (HBTs) using traditional approaches which include bias and thermal stressing under DC and, in some cases, under microwave conditions. The technique addressed in this work aims at the evaluation of reliability characteristics based on a drastically different approach, which relies on the establishment of a relationship between the low-frequency noise properties and the reliability of devices. Single heterojunction AlGaAs/GaAs HBTs were fabricated using a self-aligned process technology. The devices analyzed were from different lots which manifested clearly different reliability characteristics, namely high and small degradation upon DC stress. The process used for HBT realization differed between the lots but device design and overall DC electrical characteristics were about the same. The low reliability HBTs showed a median failure time of ~200 hours at elevated junction temperature of 150°C while the high reliability devices exceeded 5000 hours at the same junction temperature without any failures.

Bias and temperature dependent low frequency noise characterization revealed that both the base and the collector noise levels were lower in the highly reliable transistors compared to the non-reliable ones. Especially the base noise of reliable HBTs was significantly lower (one to two orders of magnitude at 10 Hz) compared to that of non-reliable HBTs (see Fig. 1).

After about 20% degradation of the current gain under constant DC bias, both the base and the collector noise increased. For low reliability devices, the collector noise increased by about one order of magnitude at 10 Hz, after stress application. The stress did not affect the magnitude of the collector noise at higher frequencies (see Fig. 2).

The base noise showed much more distinct differences in characteristics upon stress application. The unstressed devices showed base noise of lower magnitude, but had also pronounced bias dependent characteristics. In particular, the base noise of unstressed devices did not change significantly with base current while stressed devices showed a dramatic increase in base noise for higher base currents (see Fig. 3).

The identification of generation-recombination noise centers was carried out by temperature dependent noise characterization. Additional studies were carried out on both the low and the high reliability HBTs. These studies reveal activation energies for base and collector trap centers in the range of 120 to 150 meV.

In summary, we report the bias and temperature dependent noise characteristics of both high and low reliability single-heterojunction AlGaAs/GaAs HBTs and propose a novel approach for predicting the reliability of HBTs without performing time consuming DC and temperature stress biasing. The proposed technique employs the base noise as a sensitive tool for determining which HBTs are likely to exhibit fast degradation.

¹ This work was sponsored by Naval Research Laboratory Contract No: N00014-95-C-6026 (DARPA MAFET Thrust 2 Program).

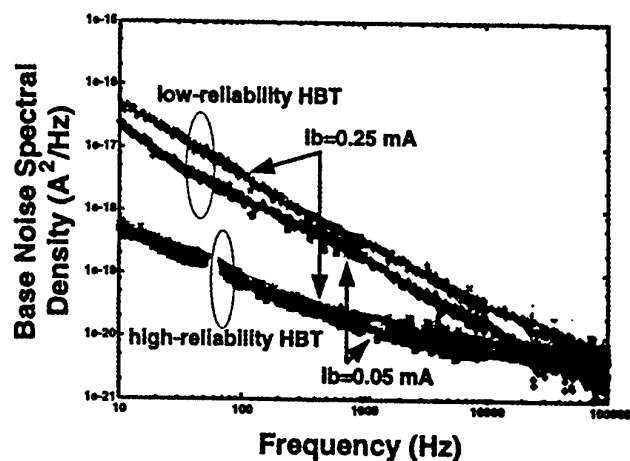


Fig. 1: Base noise of High-Reliability and Low-Reliability HBTs.

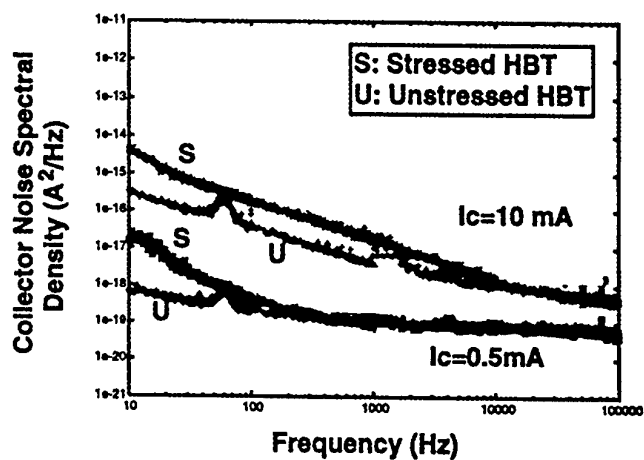


Fig. 2: Collector Noise of Low-Reliability HBTs before and after stress.

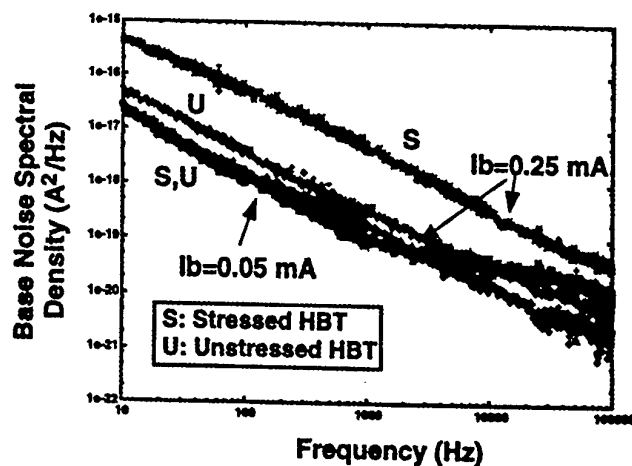


Fig. 3: Base noise of Low-Reliability HBTs before and after stress.

Monday, May 26

10.30 - 12.30 Session 2: Optoelectronics

- 10.30 1. (Invited Paper) *M.K. Smit, Delft University:*
"Photonic Integrated Circuits for multiwavelength applications"
- 11.00 2. *B.H.P. Dorren, A. Yu. Silov, M.R. Leys, J.E.M. Haverkort, J.H. Wolter, D.H.P. Maat, Y. Zhu, Y.S. Oei and F.H. Groen:*
"Polarization independent InGaAs/InP chopped quantum well interferometric space switch at 1.55 μm ".
3. *C. Llorente, R.M. Lorenzo, A. Sanz, I. De Miguel, E.J. Abril, M. López and M. Aguilar:*
"Design and analysis of a 1 x 8 wavelength division multiplexer based on the self-imaging theory".
4. *R.M. Lorenzo, C. Llorente, I. De Miguel, E.J. Abril and M. López:*
"Design and analysis of a 1 x 32 tapered coupler based on the self-imaging theory".
5. *R. Hakimi, B. Schmidt and M.-C. Amman:*
"Reduced Spectral Linewidth of Tunable Twin Guide Laser Diodes with Buried Facet Structure".
6. *W. Steffens and M.-C. Amman:*
"Effect of internal reflections on wavelength selectivity in widely tunable laser diodes".
7. *O.A. Tkachenko, D.G. Baksheyev, M.B. Wojtsekhowski and V.A. Tkachenko:*
"Irradiated quantum well in a potential step as photon source and electron pump".
8. *B. Willen, U Westergren:*
"HBT-based PIN diodes for high-speed OEIC-receivers".

Photonic Integrated Circuits for multiwavelength applications

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***Abstract.** An overview is given of advanced photonic devices for multiwavelength applications and the potential and prospects of photonic integration are discussed.*

1. Introduction

Optical communication is rapidly gaining importance. The explosive growth of services like internet requires both higher network capacity and network flexibility. Both can be provided by exploiting the wavelength domain as an additional dimension [1]. This is done in so-called multi-wavelength (MW or WDM, wavelength division multiplex) networks, where wavelength is used for increasing link capacity as well as for signal routing.

MW-links and networks require optical components with an increased functionality. Photonic integration is a key technology towards greater circuit complexity. Photonic Integrated Circuits (PICs) that have been fabricated so far include multiwavelength receivers [2-6], multiwavelength lasers [7-11], and add/drop multiplexers [12,13]. The development of more complex integrated all-optical cross-connect circuits is progressing. When multiwavelength networks become widely deployed, these devices are expected to gain a competitive edge over discrete solutions.

In this paper a review is given of some work on PHASAR-based PICs for WDM applications, starting with a brief summary of the operating principle of a phased-array demultiplexer. The first WDM systems are point-to-point connections using a number of different wavelength channels to increase the transmission capacity. Such systems will benefit from a PHASAR demultiplexer with integrated detectors which is discussed in Section 3, or a multiwavelength laser (Section 4). Network flexibility can be obtained by employing add/drop multiplexer PICs, as presented in Section 5. The article will be concluded with a discussion of the prospects and strategy for photonic integration.

2. PHASAR principle of operation

Figure 1 shows the schematic layout of a PHASAR-demultiplexer. When the beam propagating through the transmitter waveguide enters the Free Propagation Region (FPR) it is no longer laterally confined and becomes divergent. On arriving at the input aperture of the phased array the beam is coupled into the array and propagates through the individual waveguides to the output aperture. The length of the array waveguides is chosen such that the optical path length difference between adjacent waveguides equals an integer multiple of the central wavelength of the demultiplexer (as measured inside the waveguide). For this

wavelength the fields in the individual waveguides will arrive at the output aperture with equal phase (apart from an integer multiple of 2π), and the field distribution at the input aperture will be reproduced at the output aperture. The divergent beam at the input aperture is thus transformed into a convergent one with equal amplitude and phase distribution, and an image of the input field at the object plane will be formed at the centre of the image plane.

The dispersion of the PHASAR is due to the linearly increasing length of the array waveguides, which will cause the phase change induced by a change in the wavelength to vary linearly along the output aperture. As a consequence, the outgoing beam will be tilted and the focal point will shift along the image plane. By placing receiver waveguides at proper positions along the image plane, spatial separation of the different wavelength channels is obtained.

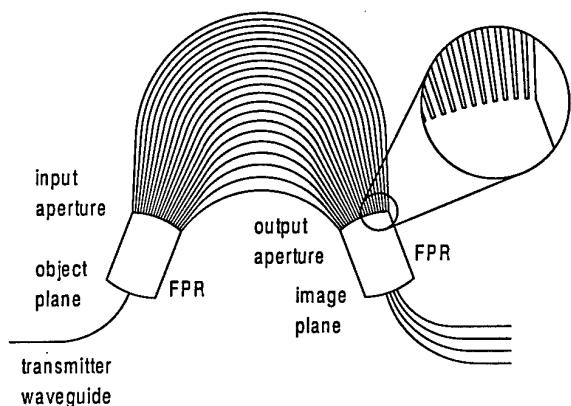


Figure 1a Schematic layout of a PHASAR demultiplexer

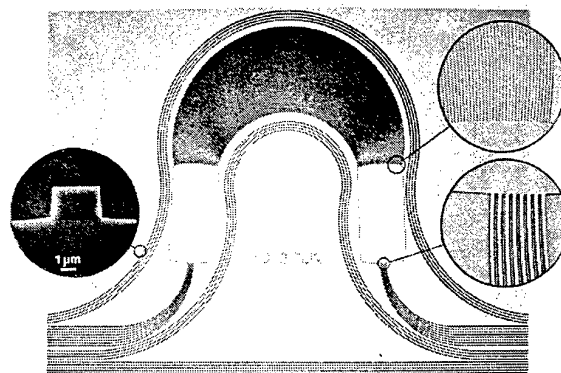


Figure 1b Microscope photograph of an 8x8 PHASAR demultiplexer / wavelength router. The insets show the waveguide cross section (left) and an enlargement of the junctions at the array and at the receiver side of the FPR (right). Chip size is $2.6 \times 3.2 \text{ mm}^2$.

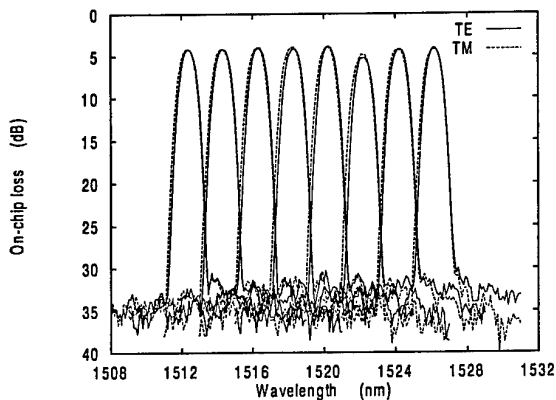


Figure 1c Filter response (superposition of 8 channels) of the PHASAR shown above.

PHASARS have proven to be robust and fabrication-tolerant devices [14]. They are particularly suited for integration with other active and passive components because they are realised in conventional waveguide technology and require little or no additional processing steps.

3. PHASAR-based multiwavelength detector

Fast, polarization-independent WDM receivers are key devices to upgrade high-capacity links. Figure 2a shows a photograph of a compact low-loss polarization-independent 8-channel WDM receiver with 400GHz (3.2nm) channel spacing [6]. The upper part of the photograph shows the PHASAR-demultiplexer, which was realized in conventional 2 μ m wide, double-heterostructure ridge waveguides. The triangular region is included in order to compensate the birefringence of the applied waveguide structure (Figure 2b, left). Without compensation the wavelength responses for TE and the TM-polarisation are shifted by several nanometers, the so-called polarisation dispersion. In the triangle the InP top load has been locally removed (Figure 2b, right), thus increasing the birefringence. By properly shaping the compensation region this increased birefringence compensates the polarisation dispersion of the rest of the array.

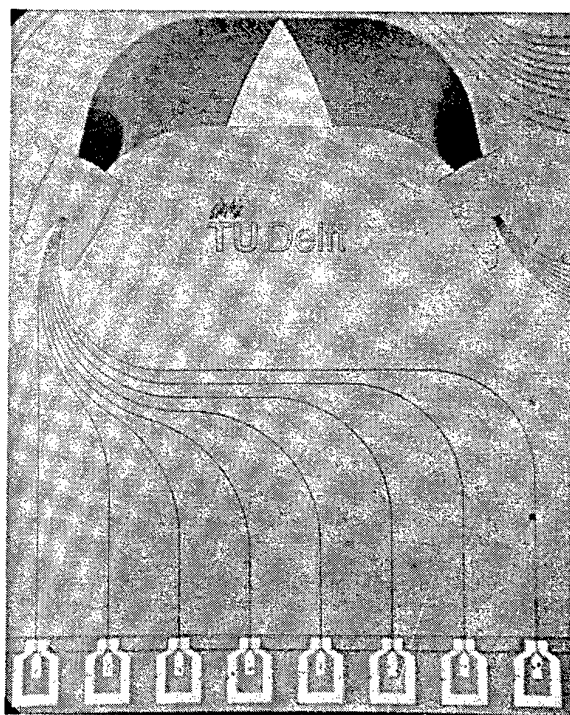


Figure 2a Photograph of a PHASAR demultiplexer with integrated photodetectors. Full size is only 3.1 x 3.9 mm².

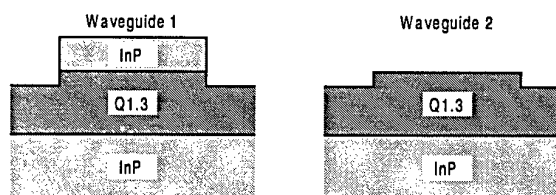


Figure 2b Waveguide structure outside (left) and inside the triangular dispersion region (right)

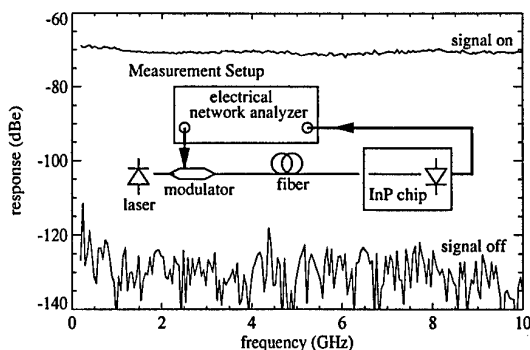


Figure 2c Electrical response of the photodetectors as a function of the modulation frequency.

The lower part of Figure 2a shows the detectors, which were fabricated in a twin-guide structure with an absorbing InGaAs layer and a p-type InP top layer on top of the slightly n-type doped transparent waveguide stack. As a first step, the absorbing top layer is removed by selective chemical etching, leaving small absorbing regions on top of the transparent waveguide stack at the position of the detectors. In this way efficient detectors with low capacitance are realized. HF-response measurements show a 3dB channel bandwidth well in excess of 10GHz (Figure 3c). On-chip loss of the device is 3dB for TE and 5dB for TM-polarization, the channel uniformity is better than 1dB with negligible polarization dispersion, and DC-crosstalk levels are lower than -40 dB (electrical). The residual polarisation dispersion is almost negligible.

4. PHASAR-based multiwavelength laser

Complementary to the demultiplexer with integrated detectors is a multiwavelength laser, i.e. a laser source that can be operated at several wavelengths simultaneously. Two approaches have been employed to reach this goal. The first is to integrate a DFB laser array with a star coupler [7,8], the second is to use a wavelength-selective element within the laser cavity, e.g. an etched grating [9] or a phased-array wavelength multiplexer [10,11,15]

Figure 4a shows a photograph of a recently fabricated PHASAR-based multiwavelength laser [11]. The wavelength-selective element in the cavity is a PHASAR having a 400GHz (3.2nm) channel spacing, and a 38.75 nm free spectral range. Nine input waveguides are connected to 500 μm long amplifier sections (the light regions at the right), while the remaining two are used for testing purposes. If one of the amplifiers is turned on, it will start emitting spontaneous emission which will be filtered by the PHASAR. After reflection at the output facet (left) it will come back in the amplifier. If the roundtrip gain becomes greater than one the device will start lasing at the maximum of the PHASAR passband. Figure 4b shows the output spectrum for simultaneous operation of 4 wavelength channels.

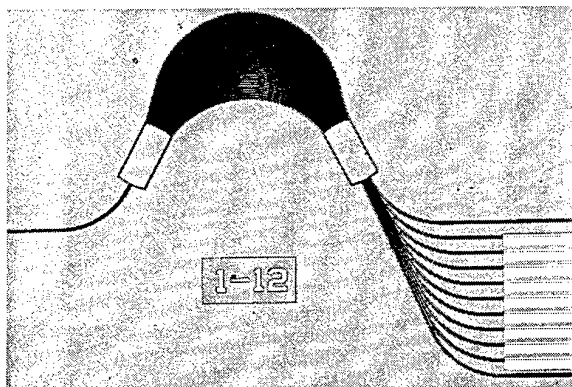


Figure 4a Photograph of the multiwavelength laser. Full size is only 3.5 x 2.5 mm².

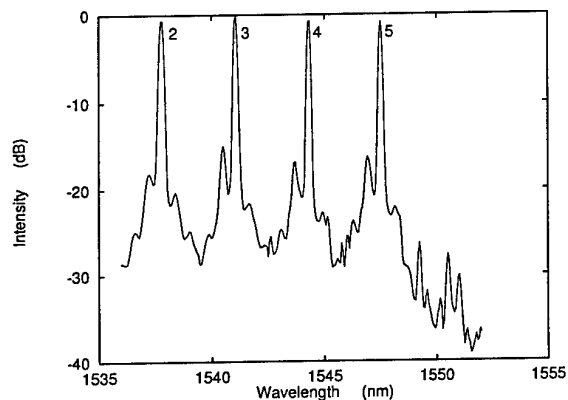


Figure 4b Spectrum for simultaneous four channel operation.

An important advantage of this type of laser is the fact that the channel wavelengths are set by the multiplexer, so that no wavelength mismatch can occur between the laser source and the multiplexer. Another advantage is the very accurate channel spacing. Disadvantage is the relatively large cavity length (6 mm for the device shown in Figure 4a), which is a problem at high modulation rates. Modulation speeds of 620 Mb/s have been successfully demonstrated [15]. Although multiwavelength operation at very high bitrates is difficult the device has an interesting potential as a discretely tunable laser in combination with an (integrated) external electro-absorption modulator: the channel spacing is much better defined than in DFB laser arrays. Linewidths in cw-mode are good: using a delayed self-homodyne technique, a linewidth of 21MHz has been observed.

5. PHASAR-based add/drop multiplexer

One of the key functions in WDM networks is to add and drop selected signals from those present on a single fiber. The first add/drop multiplexers (ADM) have been realized in silica-on-silicon waveguides, integrating three PHASARs and 16 thermo-optical switches [12]. A compact ($3 \times 6 \text{ mm}^2$) reconfigurable InP-based integrated 4-channel ADM has been reported recently [13], employing switches based on electro-optical phase shifting in a Mach-Zehnder interferometer (MZI) configuration, which allow for a very short reconfiguration time.

The layout of this ADM is shown in Figure 5. It consists of a single PHASAR, integrated with four loop-back paths containing the MZI switches. The input signal containing multiple wavelengths is led to the input of the PHASAR (right side) and multiplexed to the four outputs at the left side, which are fed to the four Mach-Zehnder switches on top of the PHASAR. In the off-state these switches couple the signals to their upper output ports which are looped back to the PHASAR and multiplexed in the output port at the left, which is routed to the right side of the chip.

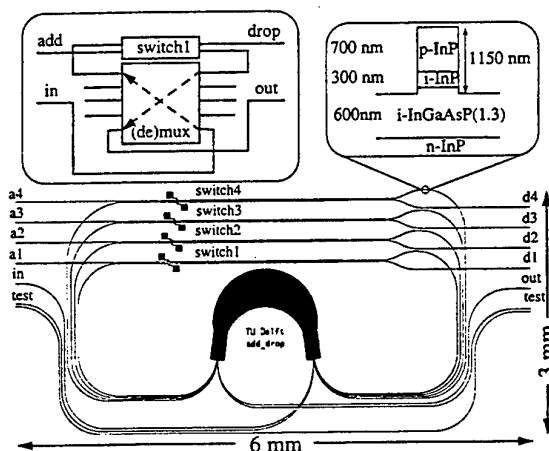


Figure 5 Waveguide layout of the add/drop multiplexer. The upper part of the mask contains the 4 MZI switches, while the lower part shows the PHASAR which is used as both a demultiplexer (the light travels from right to left) and multiplexer (the light travels in the opposite direction, from left to right). In addition a number of test waveguides have been included.

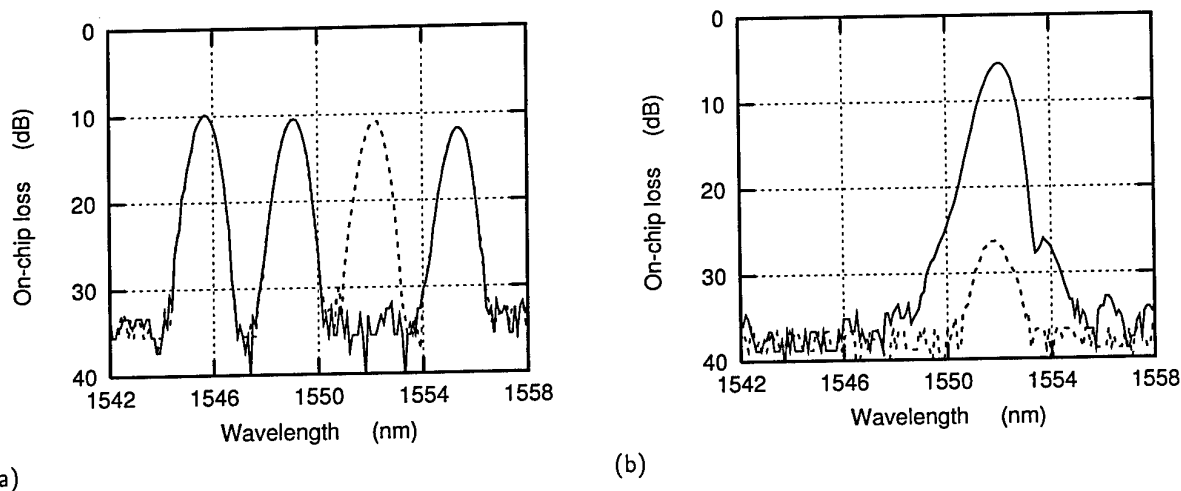


Figure 6 Transmission spectra from (a) the input port to the output port, and (b) the input port to the channel 3 drop port, with switch 3 on (solid) and off (dashed).

Figure 6 shows the performance of the device, with switching of channel 3 as an example. Two cases are shown: the signal on channel 3 is either dropped (switch 3 is on, solid lines), or passed (switch 3 is off, dashed lines). The other channels are passed (i.e. switches off). Figure 6a shows the transmission from the main input to the main output port. The total on-chip loss is only 10dB, which includes propagation loss through the PHASAR (twice), through the switch (once), and through more than 2 cm waveguide length containing 3-9 waveguide crossings. The dropped signal will appear at the drop port (Figure 6b). Residual crosstalk in both the main output port and the drop port is lower than -20 dB. It is limited by the switches.

6. Photonic Integration

The market for photonic integrated circuits, although rapidly growing, is still small. For switches and modulators integration has proven its value. For many applications, however, micro-optic, hybrid or fibre-based devices combine low cost with high performance and integrated solutions are restricted to a few special applications so far.

A strong feature of photonic integration is reduction of packaging costs in circuits containing many interconnected components. Figure 7 shows the scheme of an optical crossconnect with four input and four output fibres, each of them carrying four wavelengths. It consists of four input demultiplexers, followed by an equaliser stage consisting of sixteen SOAs (Semiconductor Optical Amplifiers), four 4x4 switching matrices and four multiplexers for multiplexing the rerouted input signals to the four output fibres. If this component is realised with discrete planar components it requires more than one hundred fibre-chip connections. If it is realised in integrated form this number is reduced to eight!

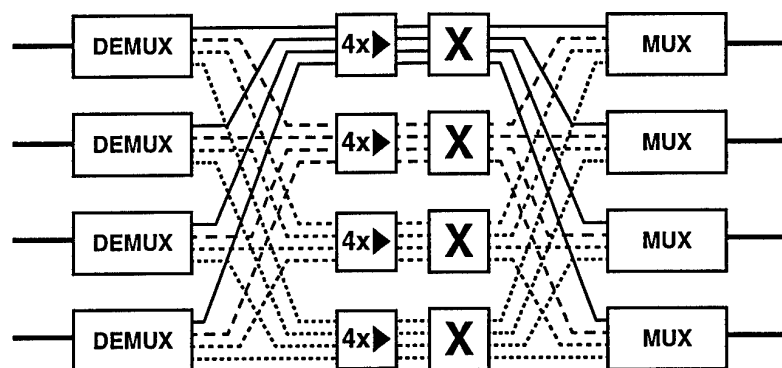


Figure 7 Scheme of a multiwavelength crossconnect consisting of four input demultiplexers, two interconnect networks, an equaliser stage with sixteen SOAs, four 4x4 switch matrices and an output stage with four multiplexers. Total number of components involved exceeds one hundred.

As can be seen from figure 7 circuits as complex as multi-wavelength crossconnects can be composed of only three different components: (de)multiplexers, SOAs and optical switches. A technology capable of integrating these three components will be also be usable for realisation of add-drop multiplexers (same components), multi-wavelength lasers (SOAs and a multiplexer) and, if the SOAs can be used as detectors by reversely biasing them, also for multiwavelength receivers. Such a technology may thus cover the demand for a broad variety of components required in tomorrow's photonic networks.

Two developments are presently speeding up the development of integration technology. For the first time a technology requiring devices with a high level of functionality, multiwavelength technology, is penetrating the network, thus creating a market to justify investments in technology development.. Secondly, progress in epitaxial technology (MOCVD and CBE) makes it possible to grow selectively different structures in different areas. In this way different devices can be optimised individually and the need to sacrifice device performance to a practical integration scheme is strongly reduced. Modern integration technology is, therefore, in a much better position for meeting system demands on device performance and is expected to become a key technology for the photonic telecommunication network.

7. Conclusion

Multi-wavelength links and networks require devices with increased functionality as compared to single-wavelength networks. Photonic integration of (de)multiplexers, switches and SOAs has the potential to meet the demands on functionality, performance and cost imposed by modern photonic networks, and will become a key technology if the rapid growth of multi-wavelength technology continues in the coming years.

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Polarization independent InGaAs/InP chopped quantum well interferometric space switch at 1.55 μm .

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Abstract:

A Mach-Zehnder Interferometric (MZI) space switch using a novel CBE grown InGaAs/InP chopped quantum well (CQW) phase section is presented. Each CQW consists of three 31Å InGaAs strained quantum wells separated by 12Å InP barriers. This structure shows a shift of the absorption edge as high as 80nm at 10V reverse bias. The heavy hole and light hole subbands cross at approximately 0.6% tensile strain. Using these chopped quantum wells, we realized MZI's with low attenuation and a $V^2.l$ product as low as 3.6 $V^2.cm$. Finally, we realized full polarisation independent switching using 0.75% tensile strained CQW's.

A first constraint for the design of a MZI space switch at 1.55 μm is waveguide transparency. When using tuning sections based on the Quantum Confined Stark Effect (QCSE) with InGaAs/InP quantum wells, the QW-thickness is limited to a maximum of 40Å for preserving waveguide transparency. Such a small QW-thickness is far from optimum for an appreciable QCSE. Chopped quantum wells allow to combine waveguide transparency at 1550 nm with a large bandgap shift. We have grown three CQW samples consisting of 20 CQW's, each with three strained 31Å InGaAs QW's separated by 12Å InP barriers (See Fig. 1). The CQW's are embedded into a p-i-n structure. A cross-sectional view of the structures is depicted in figure 1.

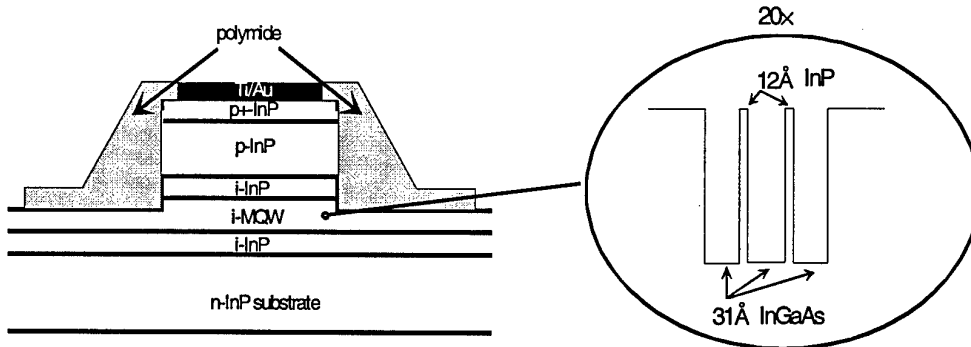


Fig 1: A cross-sectional view of the MZI-tuning section using chopped quantum wells.

We have grown CQW's with a tensile strain of 0.43%, 0.55% and 0.75% within the wells to obtain polarisation independent switching. Fig. 2a shows the effective red shift of the lowest confined energy state under applied bias of the sample with 0.43% tensile strain. Red shifts as high as 80nm at 10V applied bias are observed. Fig. 2b shows the effective absorption edges for TE and TM polarization as obtained by cleaved-side photocurrent measurements at 4K. We observe that the heavy-hole and light-hole subbands cross around 0.6% tensile strain.

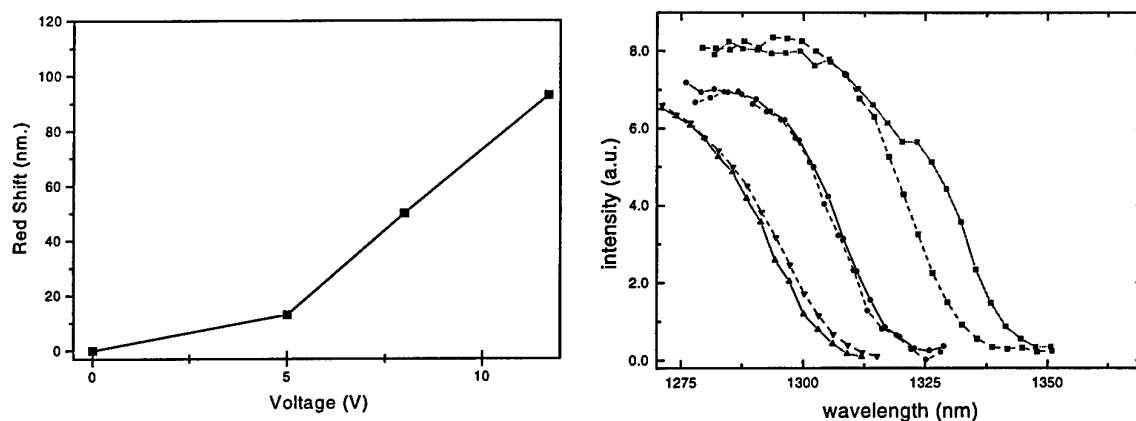


Fig 2: (a) Measured red shifts of the CQW sample under applied bias at 4K (the line is only a guide to the eye). (b) Absorption edges for TE (full curves) and TM (dashed curves) polarization for (■) -0.43%, (●) -0.55% and (▲, ▼) -0.75% strain.

We have realized MZI-switches employing CQW-material. The switch with 0.55% tensile strained CQW's shows a waveguide propagation loss of 3.8dB/cm and 2.5dB/cm for TE and TM respectively at 1.55 μm . The $V^2.l$ product required for switching is as low as 3.6 $\text{V}^2.\text{cm}$.

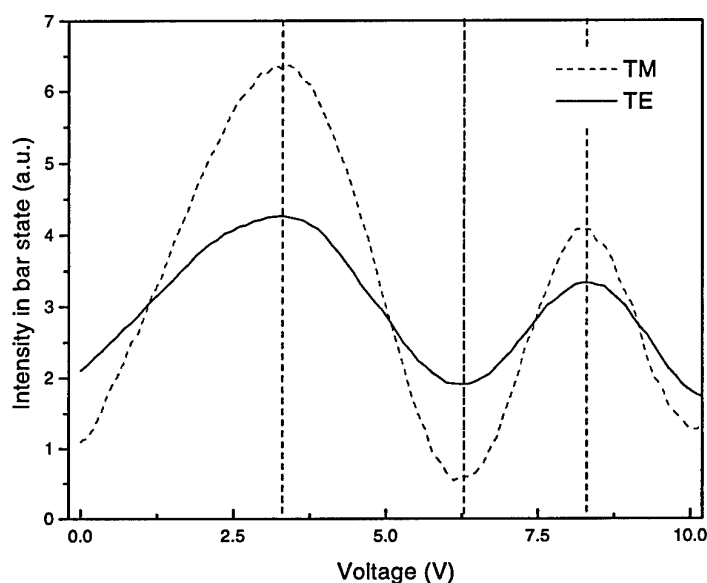


Fig 3:
Switching curve for a
MZI-space switch using
chopped quantum wells.
The MZI has 4mm tuning
sections.

Fig. 3 shows polarization independent switching at 1.55 μm for an MZI-switch with 4mm phase sections with 0.75% tensile strained CQW's. The switching curves for TE and TM propagation show identical switching voltages. The propagation losses and crosstalk are not yet identical for the present generation MZI's and will be further optimized.

DESIGN AND ANALYSIS OF A 1x8 WAVELENGTH DIVISION MULTIPLEXER BASED ON THE SELF-IMAGING THEORY

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The property of multimode waveguides of reproducing an input field in multiple (or single) images at intervals periodically spaced (self-imaging theory) has been applied into the study of optical devices. Concerning to this, the method of analysis in which the propagation of each mode is studied and, eventually, the output field is calculated by means of the recombination of the propagated mode fields, is called multimode interference (MMI) [1]. This theory drives to practical devices like couplers [2], splitters [3] and switches [4] that have been developed so far. The reason why is that MMI technology improves features like cost savings, lower dimensions, better manufacturing tolerances and simple fabrication. Polarisation changes transparency and simple design criteria are additional goals for these devices.

Wavelength division multiplexing (WDM) is the way to increase the optical fibres transmission capacity, and several works have been done [5] in order to get as much channels as possible in the field of broadband telecommunication networks [6]. Several numerical techniques has been used to analyse dielectric waveguiding problems, and the beam propagation method has become one of the preferred solutions [7].

In this paper, we have analysed a 1x8 wavelength division multiplexer, by means of the self-imaging effect, and so it could be called a MMI coupler. Our design is novel as far as we have reduced its dimension without any penalty in other feature, reducing both computing time analysis and future fabrication costs. 8 are the number of channels chosen to work with, running from 1.538 to 1.552 μm , and the cladding, n_c , and core, n_r , refractive index are 1.445 (SiO_2) and 1.473 respectively. So weak guiding glass waveguides with step refractive index profile are about to use.

This device can be easily decomposed in three different stages and two of them are MMI devices. The middle section only works carrying the signal from the input to the output sections (see Figure 1).

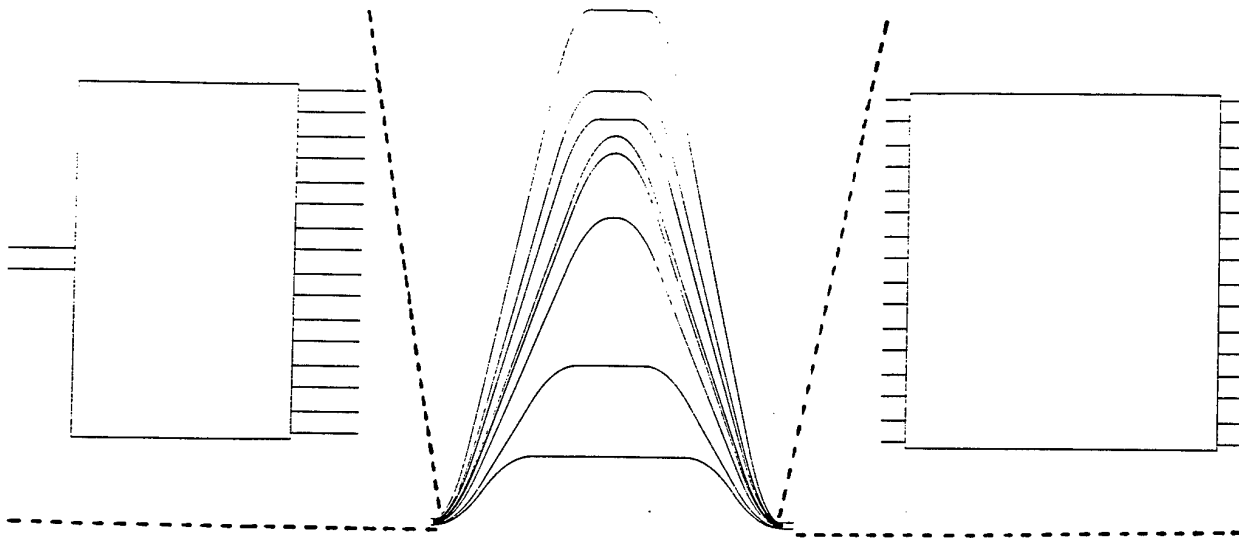


Figure 1. Structure of our design, in which the three different stages can be easily seen since a zoom has been done.

The input section is a 1x8 power splitter, and its dimension can be reduced if only the even modes are excited at the input by the mechanism called symmetric interference. 8 equally spaced images are obtained at the output of the first section. The output MMI element is a 8x8 splitter, in which its 8 input are combined to get constructive interference in order to drive the field distribution to one and only one output. The key parameter in this combiner is the input signals phase [8], and this is the task for the middle section. The phase differences conditions to get constructive interference can be shown in the Table I. The phase of the field which has traveled through each waveguide depends on the waveguide length and so, this length is what we have to play with.

Table 1: Phase conditions to be satisfied at the input of the second MMI device to get constructive interference at the desired output. Only these data are needed because of the theoretical symmetry.

O\I	1	2	3	4	5	6	7	8
8	π	$-7\pi/8$	$\pi/8$	$\pi/2$	$-\pi/2$	$\pi/8$	$-7\pi/8$	0
7		π	$\pi/2$	$\pi/8$	$\pi/8$	$-\pi/2$	0	
6			π	$\pi/8$	$\pi/8$	0		
5				π	0			

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DESIGN AND ANALYSIS OF A 1x32 TAPERED COUPLER BASED ON THE SELF-IMAGING THEORY

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A theoretical and practical development of the Multimode Interference Technology (MMI) has been carried out lately. This theory drives to practical devices like, for instance, couplers [1], splitters [2], [3], wavelength division multiplexers [4] and switches [5] that have been developed so far. The reason is that MMI technology improves features as cost savings, lower dimensions, better manufacturing tolerances and simple fabrication. Polarisation changes transparency and simple design criteria are additional goals for these devices. The MMI technology main drawback is that couplers tend to be large if we are trying to get low loss and high accurateness when signals are driven out to our clients.

The number of clients, users of these optical communication networks, are currently rising. It is within this context in which we locate our paper. We will design a device that splits an optical signal in 32 output channels both reducing dimensions and improving features.

With this paper, we aim to show that it is possible to reduce the rectangular splitters dimensions and improve their characteristics, controlling the excited number of modes with an appropriate taper. In order to simulate the present devices behaviour, order 0 and order 2 finite differences BPM have been used.

A 1-by-32 coupler will be design for the third telecommunication window, i.e., a wavelength, λ , of 1.55 μm . The material we have worked with is SiO_2 ($n_r=1.445$). We carried out the design with weakly guiding glass waveguides with a step refractive index profile equal to 0.005.

Traditionally power splitters have used a rectangular waveguide as MMI section, as shown in Figure 1.(a). When we wish to distribute the signal to a high number of outputs, the size of the former design becomes a problem. Tapered design illustrated in Figure 1.(b) will reduce dimensions without penalty in the features couplers.

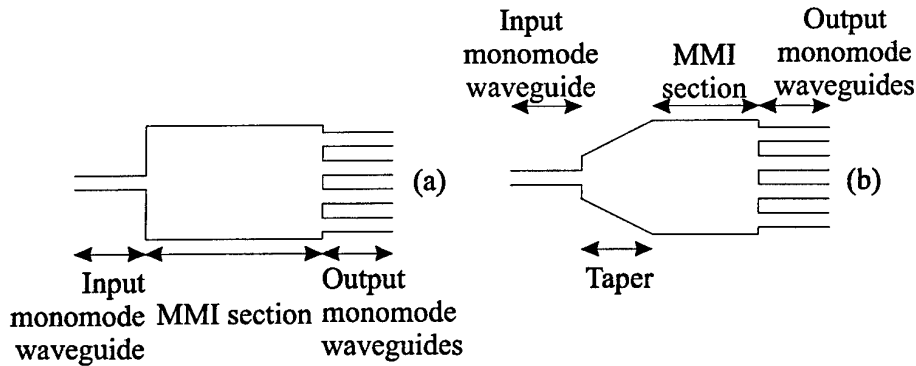


Figure 1. Geometry of two MMI power splitters. (a) Classical coupler using a rectangular MMI section. (b) Coupler using a taper to drive the input signal to the MMI waveguide.

Every dimension have been optimised and several parameters studied. Table 1 show the result of this work. Among others, wavelength influence, fabrication tolerances and bandwidth are to be highlighted.

Table 1. Summary of the parameters of 1-by-32 rectangular and tapered couplers.

	Rectangular coupler	Tapered coupler
Device width	7750 μm	7750 μm
Device length	31106 μm	24106 μm
Excess losses	0.8 dB	0.51 dB
Uniformity	1.13 dB	0.44 dB
Taper length tolerance	-	$\pm 105 \mu\text{m}$
Taper width tolerance	-	$\pm 50 \mu\text{m}$
MMI section length tolerance	$\pm 115 \mu\text{m}$	$\pm 115 \mu\text{m}$
MMI section width tolerance	$\pm 3 \mu\text{m}$	$\pm 3 \mu\text{m}$
Wave reflected energy	-55 dB	<-55 dB
Uniformity polarisation dependence	0.20 dB	≈ 0 dB
Excess losses polarisation dependence	0.09 dB	0.03 dB
Bandwidth	± 15 nm	49 nm

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Reduced Spectral Linewidth of Tunable Twin Guide Laser Diodes with Buried Facet Structure

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Electronically wavelength tunable single mode laser diodes are key components for advanced photonic applications [1,2]. An advanced type of continuously wavelength tunable laser diode requiring only one tuning current is the $1.55\mu\text{m}$ InGaAsP/InP tunable twin guide (TTG) laser [3]. As with other electronically tunable laser diodes, the TTG laser exhibits an excess linewidth broadening during tuning [4]. This broadening is due to carrier density fluctuations caused by noise processes in the tuning region which lead to refractive index fluctuations, that finally result in an excess linewidth broadening. The origin of carrier density fluctuations in the tuning region and their effect on linewidth broadening has already been described in [5 - 7]. In this paper we demonstrate for the first time, that the linewidth broadening in TTG laser diodes can significantly be reduced by burying the facets of the TTG laser (BF-TTG-laser).

Both the spectral density of the voltage noise at the terminals of the tuning diode and the spectral density of the FM noise indicate a significant $1/f$ carrier noise of up to several hundred kHz which is essentially caused by surface recombination at the laser facets. It has been shown that the $1/f$ carrier noise in heterostructure laser diodes can significantly be reduced by facet passivation with sulphur [8]. This noise reduction is clearly attributed to the temporary removal of surface states by the sulphur passivation [5]. A permanent removal may be achieved by entirely burying the tuning region of InGaAsP/InP TTG laser diodes within InP. Fig.1 schematically shows the longitudinal section of this BF-TTG laser structure. The thickness of the InP window at the facets is

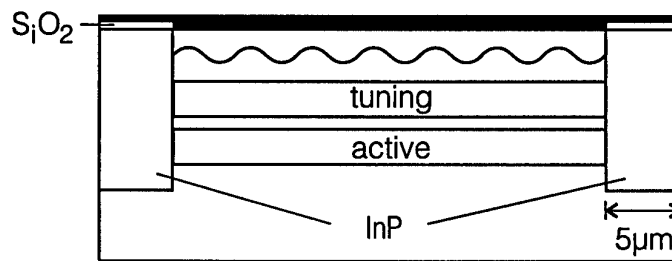


Figure 1: Longitudinal section buried facets tunable twin guide (BF-TTG) laser.

5 μm . As active and tuning layers are completely embedded in high-bandgap InP, surface states are essentially excluded. Due to the lacking surface recombination the carrier density fluctuations in the active and the tuning region significantly decrease.

Fig. 2 displays the spectral density of noise power at the terminals of the tuning diode of TTG lasers with and without InP-windows in the frequency range from 1 kHz to 10 MHz. As can clearly be seen, the BF-TTG laser shows a distinctly lower noise level. At a tuning current of 5 mA (500 A/cm²) we obtain a reduction in noise power of about 15 dB at 1 kHz. In accordance with the noise reduction in the tuning region the spectral linewidth broadening was also drastically reduced. Therefore the BF-TTG laser with InP-windows exhibits a linewidth reduction by about 10 MHz as compared with the previous TTG laser at a tuning current of 5 mA.

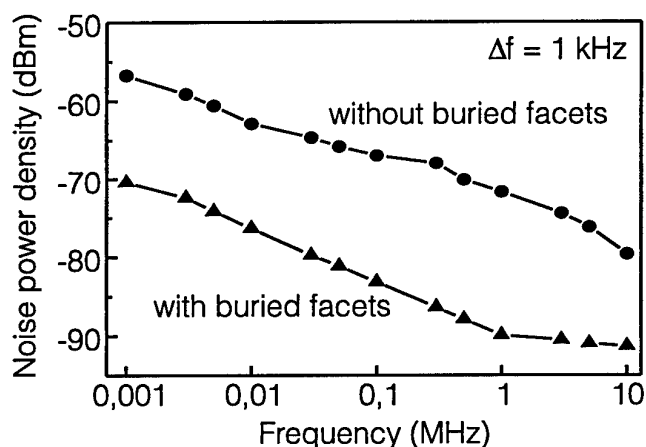


Figure 2: Spectral density of noise power at the tuning diode terminals of TTG laser with and without buried facets.

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Effect of internal reflections on wavelength selectivity in widely tunable laser diodes

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Abstract: A key issue in widely tunable lasers is the number of accessible wavelength channels. Typically only 25% of the available cavity modes can be accessed [1]. This paper investigates the suppression of individual modes by internal reflections caused by the index perturbation of a codirectional coupling grating and the improvement by applying a tapered grating structure.

Introduction: Tunable semiconductor lasers are key devices for advanced photonic systems in optical communications, measurement and sensing. Among the various laser structures presented so far, the devices with codirectional mode coupling [1, 2, 3] offer the advantage of requiring only one single control current for tuning. Wide wavelength tuning of up to 74.4 nm with side-mode-suppression-ratio (SMSR) of > 25dB has been reported. However, typically at most ~25% of the available modes can be accessed [1]. An essential origin of the unsatisfactory wavelength access represent the multi-mirror-effects caused by internal reflections at the grating.

Device Structure: Fig. 1 illustrates the twin-guide structure of a vertical coupler filter (VCF). The twin waveguide structure supports two transverse modes which exhibit a clear spatial separation essentially confined either in WG1 (mode *R*) or in WG2 (mode *S*). Coupling between the two codirectionally propagating modes is accomplished by the grating with grating period Λ (typically 10-20 μm). A maximum coupling efficiency is achieved at wavelength $\lambda_o = \Lambda \Delta n_{eff}$, where Δn_{eff} is the difference of the effective refractive indices of the two modes *R* and *S*. The structure enables the selective refractive index change by local index variations within one of the waveguides. Thus, tuning can be achieved by adjusting the refractive index of one of the waveguide modes [2]. To study the longitudinal mode selectivity, we assume a laser with variable total length L_T and a constant coupler length of $L_C = 600 \mu\text{m}$ yielding a complete coupling between modes *R* and *S* at the filter wavelength. For comparison we consider an ideal cavity design with $L_C/L_T = 1$ and a realistic one with $L_C/L_T = 0.5$ [4]. Longitudinal mode spacing is 0.57 nm and 0.28 nm, respectively.

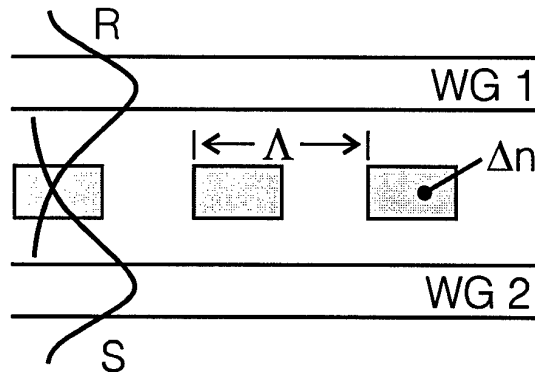


Fig. 1: Schematic longitudinal section of a vertical coupler filter (VCF) for codirectional coupling between modes *R* and *S*.

Calculations: The codirectional coupling of modes *R* and *S* and the backward reflections at the periodic perturbations are taken into account by a 4×4 transfer matrix for each period. The power transfer through the coupler and the reflected power in mode *R* and *S* can be modelled by multiplying the transfer matrixes of all periods. Owing to the fabrication tolerances of at least 0.1 μm the reflections at the numerous perturbations exhibit random phase and are therefore not phase-matched at any wavelength [5]. Simulations have been carried out assuming an effective refractive index of 3.3 for mode *R* and an effective refractive index difference between modes *R* and *S* of 0.1. The end mirror reflection

coefficient is taken to be 0.3. The resulting effective filter transfer functions for two different tuning currents are displayed in Fig. 2a. Evidently the filter transfer function is disturbed by backward reflections at the periodic perturbations. The longitudinal mode with the maximum power transmission through the VCF exhibits the lowest threshold gain. It also can be seen from Fig. 2a that the filter transfer function consists of an ideal filter curve and, due to the random phase distribution, a superimposed corrugation. During tuning, the ideal filter curve is shifted whereas the corrugations are fixed for each wavelength deviation. These corrugations may suppress or enhance individual modes. At wavelengths with local minima (see arrows) no longitudinal modes can be accessed. So, the existence of internal reflection affects the number of accessible modes but also the side mode suppression ratio.

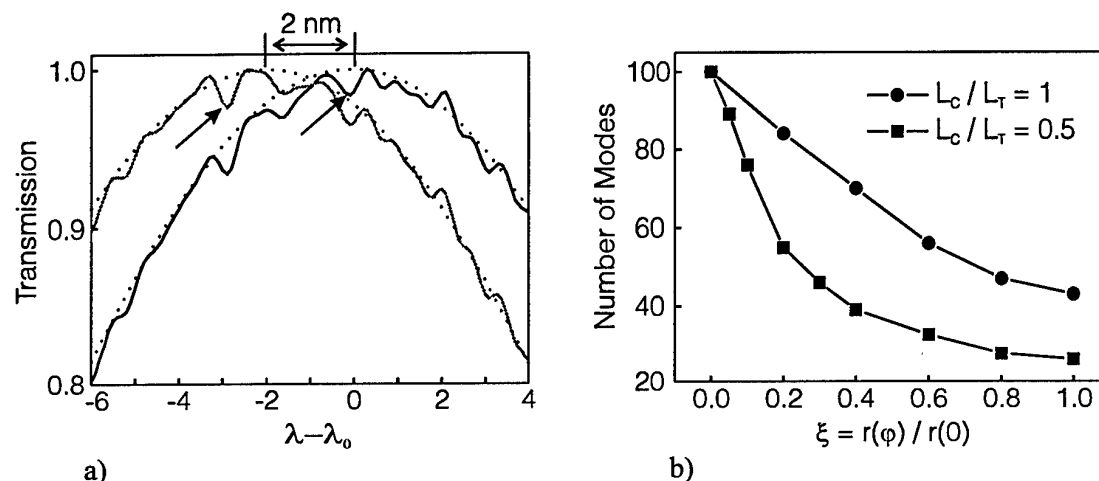


Fig. 2: a) VCF Filter curves for two different tuning currents. The dotted lines indicate the idealized case with no internal reflections. b) Number of accessible modes against power reflection ratio ξ of tapered grating.

Improvement of Wavelength Access: A significant reduction in backward reflection without affecting the codirectional mode coupling can be obtained by lateral tapering of the index perturbations [5]. The reduction in reflection is measured by the power reflection ratio $\xi = r(\varphi)/r(0)$ which relates the reflection of the tapered transition $r(\varphi)$ with that of the non-tapered structure $r(0)$, where φ is the slant angle. A reduction by more than two orders of magnitude is possible for typical device structures without affecting the codirectional coupling. The number of accessible modes of the studied device is plotted against ξ in Fig. 2b. It can be seen that a reduction in parasitic reflections strongly increases the number of accessible modes.

Conclusion: The wavelength selectivity of widely tunable lasers utilizing a VCF has been studied. Depending on the statistical phase distribution of the internal backward reflections, constructive or destructive interference occur and thus may randomly corrugate the filter curve. The corrugation may randomly suppress individual modes and restricts the number of accessible modes.

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Irradiated quantum well in a potential step as photon source and electron pump

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Inelastic resonant electron transmission through semiconductor triple-barrier asymmetric structures [1] and Stark superlattices [2] has recently been predicted to be almost full due to photon-induced transitions between two or more quasilevels. In this report we will show that analogous strong response to irradiation can be produced by the structure in which electron tunneling in elastic channel is absent and which possesses only one quasilevel. Analytic solution for the time-periodic Schrödinger equation with potential in the form of a sharp step with δ -well placed at the higher potential side gives the Breit-Wigner-type formula for transmission coefficient with emission of quantum $\hbar\omega$:

$$T_{-1} = T_{\max} \frac{\Gamma_e \Gamma_i}{(E - \hbar\omega - E_0 - \delta E_0)^2 + \frac{1}{4}(\Gamma_e + \Gamma_i)^2},$$

where E is the energy of the electrons incident from the higher potential side, E_0 and Γ_e the quasilevel and its width in the absence of hf field, δE_0 and Γ_i the shift and broadening of the quasilevel due to inelastic decay, Γ_i being proportional to the square of hf field amplitude. Thus, one can control the probability of inelastic transitions by varying frequency $\hbar\omega$ and irradiation intensity. When $\Gamma_i = \Gamma_e$ the inelastic transmission coefficient, at the resonance $E = \hbar\omega + E_0 + \delta E_0$, reaches its maximum $T_{-1} = T_{\max}$. Analytic treatment and numerical modeling of real structures show that $T_{\max}$ can be close to unity at relatively small amplitudes of hf fields.

Such configuration can be made of an n -Ga_{0.65}Al_{0.35}As/GaAs/Ga_{0.65}Al_{0.35}As/ n -GaAs structure with the voltage applied to its doped contacts to prevent from band bending [Fig. 1(a)]. Alternating voltage is provided by monochromatic infrared irradiation polarized along the growth direction of the structure. Numerical calculations show that 70%-transmission with emission of photons occurs in such structure, at optimized barrier thickness, frequency and amplitude of the high-frequency field, when cold electrons of energy E fall onto the quantum well from the higher potential side of the structure. With the account of elastic channel the transmission becomes almost full (95%) whereas it is small (4%) in the absence of irradiation [Figs. 1(b), 1(c)].

Stacking such well-in-step configurations in a single heterostructure permits of making a tunable cascade-amplifier of irradiation, and in this case inevitable technological non-uniformities of the cascades and deviating positions of quasilevels will not impede its workability. Indeed, since the electron motion above the step is classically allowed the energy of incident electron and, respectively, the frequency of the hf field are more widely variable than in resonant photon-assisted tunneling through two quasilevels E_0 and E_1 of an asymmetric triple-barrier structure [1]. In the former case the only resonant condition $E = E_0 + \hbar\omega$ must hold instead of two conditions in the latter case: $E = E_0$, $E_1 = E_0 - \hbar\omega$. It differs advantageously from single-well [3] and multiple-well [4] cascades in which photon must couple the pairs of quasidecrete states.

Due to detailed balance, an analogous p - i - n structure with an In _{x} Ga_{1- x} As quantum well can act, at a corresponding direct voltage, as an electron pump for electrons incident on the potential step from n -GaAs side and having the energy of the quasilevel.

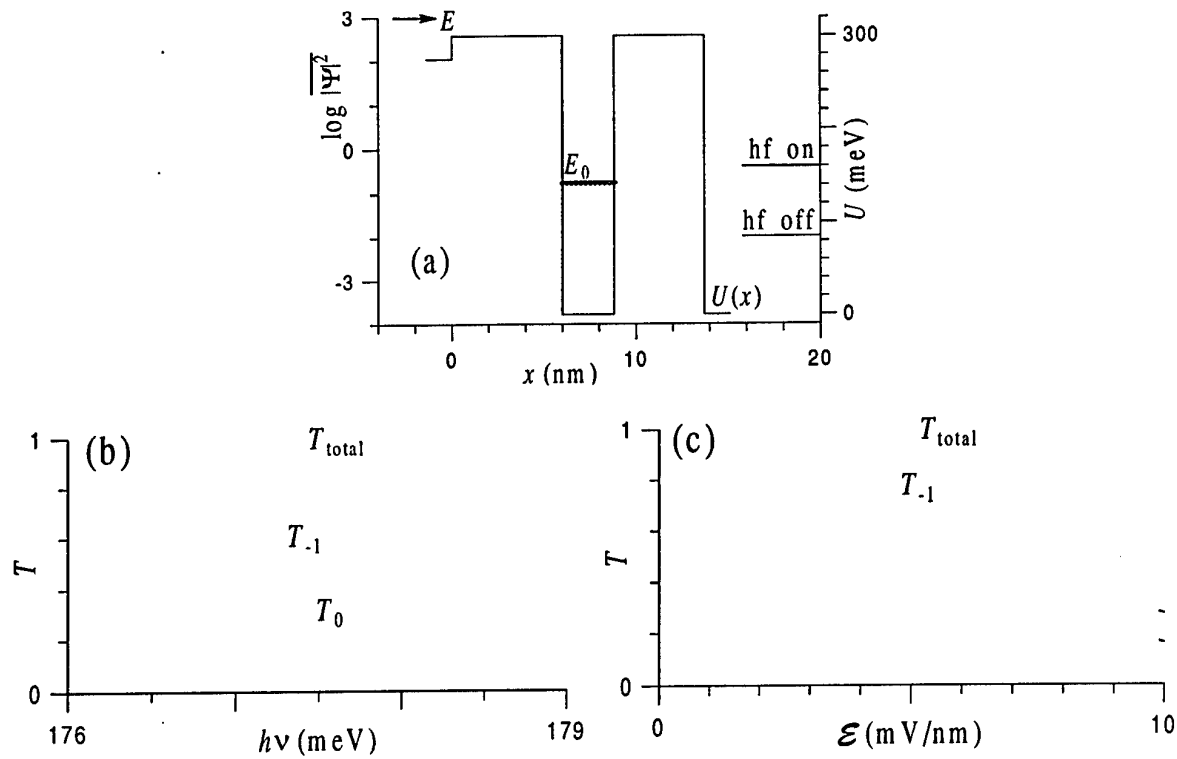


Figure 1. (a) Time-averaged probability density $|\Psi|^2$ and potential of the structure $U(x)$. Electrons of energy $E = 320$ meV are incident from the left. Switching on hf field ($\hbar\omega = 177.5$ meV, amplitude $\mathcal{E} = 5$ mV/nm) results in strong increase of transmission. (b) Frequency dependence of elastic, T_0 , inelastic, T_{-1} , and total transmission at fixed amplitude $\mathcal{E} = 5$ mV/nm. (c) Transmission at resonant frequency $\hbar\omega = 177.5$ meV versus amplitude of hf field.

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HBT-based PIN-diodes for high-speed OEIC-receivers

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Introduction

The growth and spread of the information society continue to increase, and new telecommunication services are emerging. The resulting requirements for an increased capacity of the transmission systems can be met by increased time, wavelength, or space multiplexing. These techniques are not exclusive, but it is of decisive importance that the limitation of each one is determined. When time multiplexing is used for fibre optical transmission, the limitations are optical dispersion and the maximum bandwidth of the optoelectronic interfaces, that is, the transmitter and the receiver. The bandwidth of an optoelectronic transmitter is mainly governed by the high-frequency properties of the light-emitter itself, and a hybrid solution with a separate driver is therefore competitive with the monolithic counterpart. In contrast to this, a receiver benefits substantially from monolithic integration regarding sensitivity and bandwidth, and is today the most frequent developed OEIC.

Fig.1. Bandwidth and quantum efficiency dependence of the collector width for an HBT-based PIN-diode.

It has become a common technique to employ the base-collector-subcollector region of an InP-HBT as a PIN-type photodetector used in OEIC-receivers. This means that the collector thickness must be designed regarding the photodetector response. Both the amount of detected photons and the time required to get the generated charge carriers out of the active area increases with the absorption depth, so the optimum choice is a tradeoff between quantum efficiency and bandwidth, as shown in Fig. 1. High-speed detectors require a thin *i*-layer, so the absorption in the underlying subcollector is significant. The shown transit time delay is therefore valid only if the effects of slow carriers diffusing from the subcollector region can be neglected. This is achieved by including a properly graded heterojunction in the collector-subcollector interface to create an effective hole barrier in the valence band.

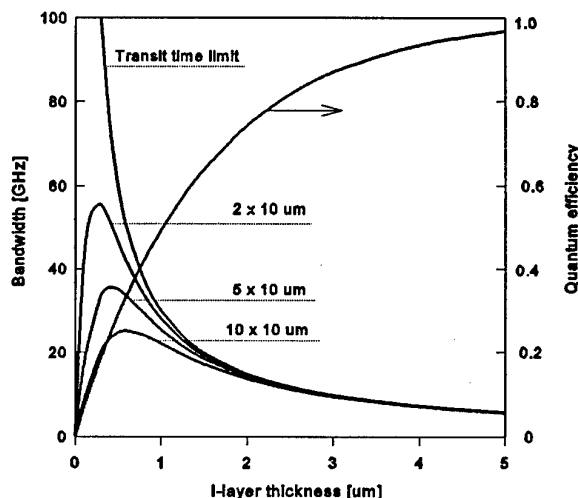
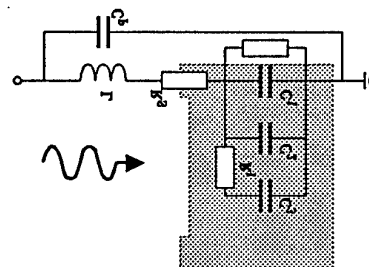


Fig.2. Equivalent model for an HBT-based PIN-diode.



An HBT-based photodetector differs significantly from a conventional *pin*-diode, the main difference being the thickness of the base layer in an HBT that is made extremely thin to enhance the high-speed properties. When used as the *p*-layer in a *pin*-diode, the thin layer results in a high series resistance, making the conventional model that consists of a series resistor and a leakage resistor in parallel with a capacitor inadequate. The frequency dependence of

evaluated PIN-diodes cannot be explained by a single pole equivalent. This can be understood since a part of the *i*-layer situated sufficiently close to the *p*-contact does not suffer from the high serial resistance in the *p*-layer because the holes will drift directly towards the contact, while the central part is strongly affected from this resistance since the holes must traverse a significant part of the *p*-layer. This effect is especially pronounced for wide active areas. The distributed base resistance is approximated as the single intrinsic resistance R_i in Fig.2.

Further, the active part shaded by the contact metal must be separated out to allow for an adequate input signal area. Thus the device area needs to be partitioned into three separate regions, one passive region below the contact metal, one low resistive active region close to the contact, and one high resistive active region in the centre of the device. The resulting extended equivalent small-signal model shown in Fig.2 is found appropriate in our simulations, and it also strongly shows the importance of using a circular base contact to decrease the effect of the high base resistance.

The implication of the thick collector layer on the HBT performance is a decrease in the base-collector capacitance, C_{BC} . It also makes C_{BC} bias dependent, as shown in Fig.3, since the wide collector not is depleted at zero bias. The maximum frequency of oscillation, f_{max} , increases over the entire bias range, while the transit frequency, f_T , is almost constant, so the f_{max} -to- f_T ratio is almost three at a high bias. The base-collector time delay $\tau_{BC} = f_T / (8 f_{max}^2) = R_B C_{BC}$ is also plotted in the figure and displays the rapid decrease in the capacitance, assuming a constant base resistance.

OEIC-receivers with transimpedance amplifiers have been designed using InP-HBTs, shown in Fig.4, and fabricated in our in-house HBT fabrication process. Evaluation of realised receivers showed a good agreement with simulations for receivers designed with a low bandwidth, Tab.1. There where a small discrepancy for those with the largest bandwidth, which could be attributed to the design that was based on the conventional PIN-diode model. A good agreement was obtained also for high bitrates, after resimulation with the improved model. The required bandwidth for a receiver depend on system requirements, but 28 GHz is thought to be sufficient for 40-Gb/s communication.

Fig.3. Cutoff frequency and base-collector time delay dependence of the collector-emitter bias for an HBT with a thick collector layer.

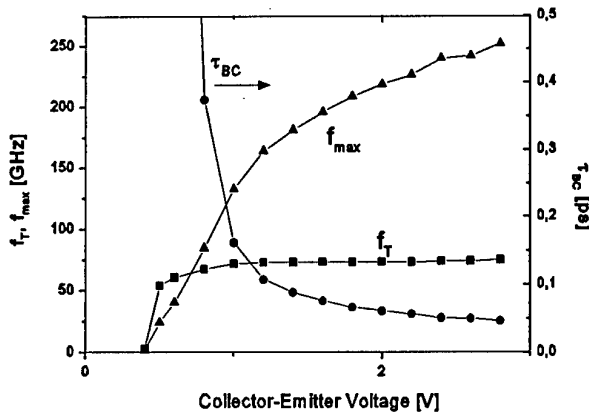
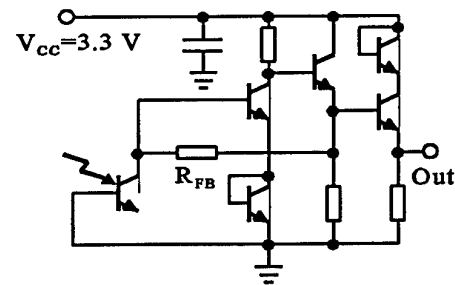


Fig.4. OEIC-receiver with transimpedance amplifier and PIN-diode



<i>Table 1. Simulated and measured parameter values for OEIC- receivers. Bi trate [Gb/s]</i>	Ztrans [k]	BW [GHz]	Pmin [dBm]	Ztrans [k]	BW [GHz]	Pmin [dBm]
	Simulated			Measured		
10	1.33	8	-21	1.39	7.7	-21
20	0.82	15	-17	0.86	14.2	-17
40	0.30	28	-12	0.32	24.5	-12

Conclusions

An extended PIN-diode model has been developed. It is found from both evaluation of single devices and realised OEIC-receivers that this model is required to explain the high-frequency behaviour of the photodetector. OEIC-recievers has been designed and evaluated, with a bandwidth ranging up to 24 GHz. There is a good agreement between measured results and simulations, regarding bandwidth, transimpedance, and sensitivity. These results prove the possibilities to use HBT-based PIN-diodes to fabricate complete OEIC-receivers for 40-Gb/s fibre optical communication systems.

Monday, May 26

14.00 - 15.30 Session 3: Integrated Circuits and Noise

- 14.00 1. (Invited Paper) *G. Gatti, ESTEC:*
"Space applications of GaAs MMICs"
- 14.30 2. *J. Berntgen, M. Heuken and K. Heime:*
"The influence of the cap layer on the low frequency noise of 2DEG structures".
3. *A. Matulionis, J. Liberis, I. Matulioniene, P. Gottwald, J. Karanyi, B. Szentpali, H.L. Hartnagel, K. Mutamba, A. Sigurdadottir:*
"Hot-Electron Diffusion Coefficient in Standard Doped InP Channels".
4. *A.P. de Hek, F.L.M. van den Bogaart:*
"Broadband High Efficient X-band MMIC Power Amplifiers for Future Radar Systems".
5. *F.E. van Vliet, J.L. Tauritz, F.L.M. van den Bogaart:*
"On the Design and Application of Narrow tunable MMIC Filters".
6. *P. Marsh, D. Pavlidis:*
"Noise Analysis of InGaAs Mixer Diodes at Millimeter Wave and Far-Infrared Frequencies"

SPACE APPLICATION OF GaAs MMICs

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ABSTRACT

This paper will review space application of GaAs MMIC technologies starting from an historical background, pointing out advantages and disadvantages, and concluding with qualification and process issues.

MMIC in space: an historical background

As for any relatively new technology, the introduction of MMICs in on-board space equipments has followed after 4 to 5 years of their use in terrestrial and, especially, in military applications. Until the mid 80's, at least in Europe, the use of MMICs in on-board space equipments was very limited. The limited number of programmes, and the relatively relaxed requirements for mass and volume of units did not constitute a strong pull for MMIC technologies.

This was combined with the lack of sufficient reliability track records of MMIC technologies and by a limited knowledge of the technology among space equipment manufacturers and payload prime contractors. Additionally the lack of design expertise and specific CAD tools was a further barrier for a wide use of MMICs. One further reason was the perceived high initial development cost, not always justified by the limited number of units of the same type to be constructed.

With the time, the more complex satellites and, as a consequence, the higher number of equipments to be installed on-board, have begun to demand largely reduced mass and volume, which have been realisable only using miniaturised technologies such as MMICs. Later, the continuously increasing number of commercial telecommunication satellite programmes has also required a reduction in the equipment manufacturing time and cost, which has further incremented the use of MMICs.

Today, MMICs are present in practically every on-board space microwave module and developers are pushing ahead with this technology to maximise its advantages. For example multi-function MMICs are designed to combine more than one basic function on a single chip. This is made possible by the mastering of MMIC design techniques, reached in space equipment manufacturers and by the availability of better and more advanced design tools.

Advantages and disadvantages

As indicated in the previous paragraph the main advantage of using MMICs in space is the reduced mass and size, which are at a premium in any space programme.

As an example figure 1 (courtesy of Alcatel Espace, Toulouse, France), shows the evolution of a satellite, Ku-band, channel amplifier starting from a unit built in 1988 to the present generation, and to the next future implementation.

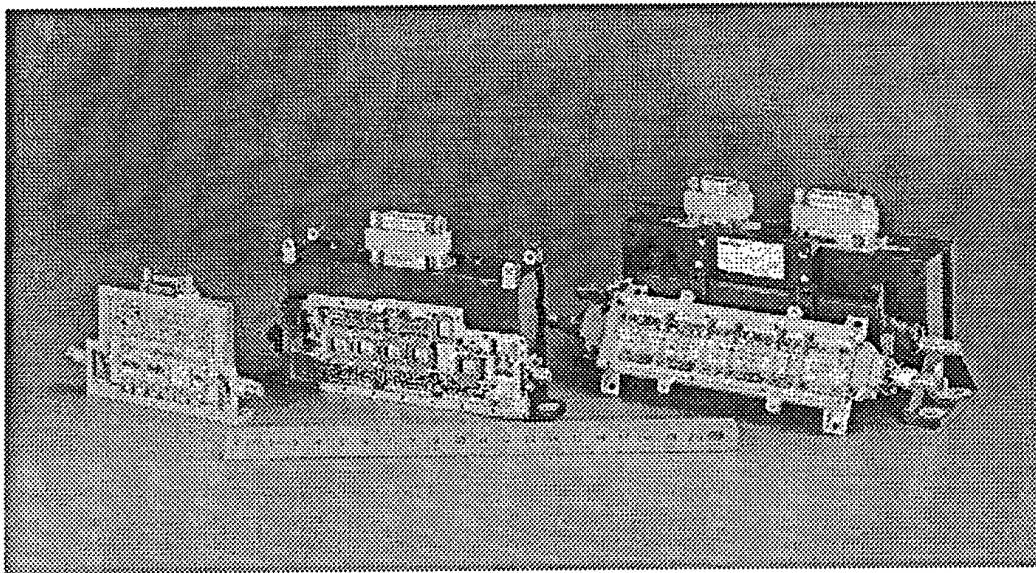


Figure 1 - Various generations of Channel Amplifiers (courtesy Alcatel Espace)

The units shown in figure 1 have the following characteristics:

	Next future	Today	1988
Technology	RF and DC: MCM	RF: micro-packaged MMICs DC: PCBs	RF: discretes, bare chips DC: PCBs
Mass	95 g	220 g	550 g
Volume	165 cm ³	286 cm ³	614 cm ³

The above table clearly indicates that even though miniaturization of equipments has in the MMIC technologies a main pillar, this would not be maximized without a combination of other advanced technologies. In particular, microwave equipments are not only constituted by the microwave modules: all the biasing circuits, the telemetry and telecommand functions (always present in on-board space equipments), shall also be implemented using miniaturize technologies such as DC hybrids, ASICs, thin and thick film technologies, surface mounted components, etc. Additionally, newer technologies such as multi-layer substrates, allow to implement advanced Multi-Chip-Modules (MCMs) further reducing the overall mass and dimensions [1].

Another advantage of MMICs is the improved reliability resulting from the elimination of several assembly and integration steps and, in particular, by the elimination of bonding wires.

In addition the reduced number of assembly and integration steps and procedures, combined with the much reduced tuning time (using MMICs at a mature design status), yields a significant reduction in the equipment manufacturing time and, therefore, cost.

In applications such as active antennas (like in the case of the ESA program ENVISAT-1 where a C-band, active antenna using 320 T/R modules is used for SAR imaging) MMICs give the additional advantage of providing more repeatable and tracking performance, compared to implementation using discrete devices.

As the frequency increases, and reach mm-wave frequencies the use of MMICs gives the advantage of a large reduction of discontinuities and parasitics, which makes MMICs the ideal candidate for realising low power circuits at frequencies up to 100-120 GHz, with characteristics superior to any

other alternative implementation. In the future ESA program PLANCK, more than 200 MMICs operating over channels ranging from 30 to 100 GHz will be used to implement advanced radiometer concepts.

GaAs MMICs have also the advantage of being much less sensitive to radiation effects than Si based devices, at least at the level of radiation expected in common satellite applications. This simplifies the electrical and, especially, mechanical design of equipments, by avoiding the need for thick radiation shields.

Besides all the advantages mentioned above, the use of MMICs in space has also disadvantages. One of them is the development cost which is acceptable only if the number of units to be produced is high, considering that for an ad-hoc MMIC development at least two design cycles, including foundry runs, are necessary (for an average cost, for a single chip design, approximately between 130 KEcu to 280 KEcu depending on the process used and on the complexity of the chip). Some of the space equipment manufacturers have, in some cases, overcome this cost issue by designing "universal", simple MMIC building blocks (e.g. gain blocks) that they could re-use in various types of equipments.

The most important disadvantages of MMICs are, however, due to thermal dissipation and electrical losses. In fact, GaAs is not a good heat conducting material (46 W/m°C compared to 118 W/m°C for Silicon). Additionally MMICs devices cannot be industrially produced with a thickness below, typically, 100 μm to maintain a reasonable production yield. This limits the use of MMICs in space applications for high power amplifiers as the devices would run at an excessively high temperature, with a resulting reduction of life-time and performance (output power, gain, power added efficiency). The use of discrete MESFETs (or HBTs, or P-HEMTs) gives much better performance as these devices can be thinned down to 30-50 μm and directly soldered on the equipment base-plate, with a significantly increased thermal conductance.

Concerning electrical losses, a $\lambda/4$, 50 Ω line at 12 GHz typically has a 0.1 dB higher loss on GaAs than on ceramic substrates, such as Alumina. Even though this difference could seem small, it produces degradation of performance, often unacceptable in space applications, in power amplifiers and in low noise amplifiers. Just as a rule of thumb, a 0.1 dB loss at the output of a power amplifier gives a reduction of about 1 % in power added efficiency. Therefore, generally speaking, MMICs are not used in space equipments in the input stages of low noise amplifiers and in the driver and output stages of power amplifiers.

Another disadvantage of MMICs is that it is today not possible, at least at industrial processes level, to mix different technologies on the same chip. For example it is not possible to have a chip where very low noise performance is mixed, for example, with high power capability. This disadvantage becomes a limiting factor when multi-function MMICs devices are desirable, e.g. input limiters based on PIN diodes, directly integrated with LNAs based on P-HEMT devices.

Design approach

The design approach for MMICs to be used in on-board space applications is in many aspects not very different from the design for other applications. Notably, however, there are some basic differences, mainly related to a design strategy aimed at maximizing reliability and reduce manufacturing risks. In particular any schedule impact shall be avoided considering that the time from order to delivery is constantly reducing. For units for commercial satellites this can be as short as 6 months.

In terms of reliability, typical commercial satellites of today are required to operate reliably for 15 years. This means that no compromise, beside introducing proper redundancy schemes at equipment level, can be made in order to guarantee this long-life cycle for the single MMICs.

Degradation of MMIC performance can be, generally speaking, related to:

- operating temperature of the active devices (channel temperature)
- current density in transmissions lines and DC lines

- level of signal power compression and ratio between average and peak power
- assembly, integration, testing procedures and processes
- packaging procedure and processes.

A good review of the reliability issues for MMICs in space applications is reported in reference [2].

Over the operating temperature range, the device biasing point and class of operation shall be selected to maintain the channel temperature typically below 110° C, at the higher operating temperature range of the equipment base-plate, and with the worse signal level condition (e.g. no-signal in class A operation). This is typically a critical design challenge for power amplifiers, where the design shall aim at maximizing power added efficiency while maintaining good linearity and avoid excessive gate currents and excessive compression levels (see following remarks).

Concerning current densities (normally to be maintained below $2 \cdot 10^5$ A/cm²) this is an issue that normally affects the gate metallization, as they have the smallest dimensions in the active devices, and, to a lesser extent, DC biasing lines and choke inductors which normally carry the highest DC currents. For the gate metallization the designer shall pay particular attention to limit the average total gate current by reducing the degree of compression, especially in presence of signal with high peak to average voltage ratio, and to properly set the impedance of the DC biasing network in order to limit this current.

Regarding the compression level, high values of RF overdrive (typically above 2 dB of compression, single carrier operation, but very much depending on the device technology) can cause the generation of hot-electrons near the drain end of the channel. If these electrons possess sufficient energy they can tunnel in the SiN passivation and be trapped there, degrading the device performance. The phenomena is aggravated when the RF signal has an high peak to average power ratio (as multi-carrier signals, typical of satellite telecommunication applications). Also in this case the designer shall make sure that in all operating conditions, including over the temperature range, the degree of compression at each stage is maintained within safe limits [3].

In relation with assembly, integration and testing procedures and processes, the designer, when feasible, shall design circuits to make them more robust against ESD (electrostatic discharge) events by, for example, using high pass matching networks (with inductors going from the signal line to ground) against low pass networks.

For packaging, the designer shall make sure that the selected package is treated in a manner to avoid release of hydrogen which can significantly degrades the MMIC performance. In addition and when possible, the designer shall select processes that are more resistant to this contaminant (e.g. with Al based gates). Particular care shall also be given to the optimization of the packaging and sealing processes to minimise moisture content in the hermetically sealed package.

In terms of specifications, design of MMIC for on-board space applications is often different in terms of bandwidth of operation (typically smaller than, for example, for military systems but wider than for terrestrial communications), type of RF signals, environmental constraints, etc. Operating temperature ranges are, for example, different and generally wider than in other applications (e.g. in airborne equipments can be maintained, in many cases, over a more limited temperature range by cooling and/or heating) and to avoid extremely sophisticate compensating schemes the designer shall well predict performance over temperature and, when possible, use on-chip compensation techniques.

Additionally adequate performance margins shall be built-in during the design to reduce the risk of delays and additional costs during the equipment production cycle. These performance margins should include also stringent review of the MMIC stability behavior, to exclude possible oscillations or spurious generation which could jeopardise the manufacturing schedule of a unit, or even the payload/instrument performance if not detected well in advance. In particular special attention shall be concentrated on excluding possible common-mode oscillations that could arise in circuits containing balanced structures (e.g. power amplifiers), which are not detectable by using the standard input-output stability analysis and verification methods [4].

Moreover the selection of the foundry and of the foundry process shall be done to guarantee proper availability during the multi-year development time of programs, especially for non-commercial programmes. In terms of space qualification it is a good starting point for a designer to start designing MMICs with processes that are used for large volume production (e.g. for consumer, terrestrial markets). These processes are so well controlled that they will inherently provide highly reliable products also for space, when applying the specific design and application strategy mentioned above.

At the European Space Agency the most important recommendations for the design of MMICs for on-board space applications are included, together with documentation and test requirements, in a specific document [5] which is applicable to all ESA R&D contracts including MMIC designs.

Qualification

There is not a standard approach toward MMIC qualification at world-wide level. However we can at least distinguish between two general approaches: one is the so called "Capability Approval" approach and the second is the "Project qualification" approach. In the first case a process at a foundry is defined within a "capability domain" and specific evaluation tests are carried out at process level to demonstrate its quality characteristics, and the capability is maintained over the years with regular maintenance testing. If a MMIC is designed and manufactured according to the "capability domain", then only a limited number of testing is required to procure this specific MMIC. This approach is convenient if a large number of different devices have to be procured from the same supplier, using the same process. This has been the case for the ESA project ENVISAT-1 for which most of the MMICs for the SAR T/R modules have been produced by GEC-MMT using their process F20, under ESA Capability Approval.

In all the other cases, the approach is more oriented to specific MMIC devices, for a specific project. After the process has been submitted to evaluation tests, qualification tests (wafer acceptance test, lot acceptance tests) are specifically run on the specific MMIC to be procured. This approach gives more flexibility to procure devices using different supplier and different processes.

Processes

The largest number of GaAs MMICs used in space applications have been based on conventional, ion-implanted, 0.5 μ MESFET processes. More recently, and especially in view of the exploding new market for on-board Ka-band equipments for multi-media satellite applications, the number of MMICs using GaAs 0.25 or 0.15 μ m P-HEMT processes have been constantly growing. In addition, the interest is growing, for some applications, to utilise normally-on/normally-off technologies to reduce power consumption, in low signal applications, and/or implement mixed analogue/digital MMICs.

For applications above 30 GHz, the use of InP based, P-HEMT MMICs technologies has been already considered especially in applications, such as wide-band radiometers, where the noise figure minimization is fundamental for the instrument performance (and even cryogenically cooling of devices is envisaged to reduce further the noise-figure). However the maturity of these processes is still limited, mainly because there is not a clear, strong market pull for these, still quite expensive, processes.

Concerning HBT processes, their application to space units could be advantageous, for example, for high efficiency, pulsed power amplifiers at frequencies below Ku-band. However, limitations in process maturity and general concerns on the process reliability have, until now, practically excluded these devices from on-board space applications, at least in Europe.

The situation is different for power HFET devices (non to be confused with HEMT devices). HFETs are practically an improvement of MESFET devices, where higher break-down voltage, higher power added efficiency, higher gain in class AB and B operation, higher reliability have been accomplished using a low doped AlGaAs layer on the top of a standard GaAs channel. Also for these devices, however, the applicability range is limited to frequencies below Ku-band. The major source for this

technology, available for discrete devices and MMICs, is Texas Instruments (USA), but some other suppliers are working on similar concepts which are potentially very interesting for applications in on-board solid state transmitters. Equipments which utilise HFETs are already flying in several satellites.

For a summary of GaAs MMIC processes available in Europe the reader can find a good reference at: <http://www.estec.esa.nl/xrmwww/mmic/mmicpr.htm>.

Ground applications

The design and applications of MMICs for satellite ground terminals does not differ at all from other commercial applications of MMICs. In particular the DBS receiver market is one of the biggest consumer application of GaAs MMICs (the other being the mobile phone market). Also in this area, however, the introduction of MMICs is justified only when the overall cost is minimised, and where the performance is acceptable. Even in the DBS receiver market until recently the standard chip set for the Ku-band out-door unit would be constituted by discrete P-HEMT chips and one MMIC down-converter.

The coming market for Ka-band multi-media services will definitely constitute a new opportunity for GaAs manufacturers for high volume productions of various MMICs. In particular the implementation of low cost, 30 GHz power amplifiers with 1 to 2 W output power capability will pose a great challenge both at design and process level.

Conclusions

Following a slow start, MMICs are now constantly present in on-board space equipments. Their application is not, however, generalised to all sorts of functions due to performance and reliability restrictions, and, in any case, shall be accompanied by other miniaturised technologies to maximise the overall advantages. MMIC design for space applications shall be oriented toward reliability, production cost reduction, and schedule risk minimisation. In the future, the use of MMICs in on-board space equipments will further expand to higher frequencies, multi-function circuits, manufacturing using different devices (HBTs, P-HEMTs) and other semiconductor compounds (e.g. InP). Ground terminals already constitute a large volume, consumer application of MMIC technologies and will further expand to meet the requirements of the new, multi-media Ka-band satellite applications.

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The influence of the cap layer on the low frequency noise of 2DEG structures

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The low frequency (LF) noise characterization and optimization of semiconductor devices gain more and more in significance, due to increasing requirements for high-tech applications. Modern HFETs based on InP exhibit very low microwave noise due to the spatial separation of the electron supplying layer and the channel. However, these devices suffer from their LF-noise, which limits their applicability as oscillators, mixers and as wideband amplifiers.

In general the normalized spectral LF-noise of a homogeneous semiconductor sample is given by the following equation, where S_V describes voltage fluctuations, S_I current fluctuations and S_R the resistance fluctuations.

$$\frac{S_V}{V^2} = \frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{\alpha_H}{N f} \quad (1)$$

(with: f = frequency, N = total number of free charges, α_H = Hooge parameter)

The Hooge parameter α_H used in (1) depends on the scattering mechanisms and on the quality of the crystal [1]. For this reason a LF-noise minimization requires an optimization of the crystalline quality. In order to achieve good ohmic contacts at semiconductor devices a thin highly doped cap layer is necessary. Usually this cap layer, which has also the function of a kind of passivation, remains on the device after processing. In TLM structures the cap layer leads to a parallel conduction between the channel with its 2DEG and the depleted cap layer. The total normalized spectral LF-noise of this TLM structure composed of the sum of two noisy currents i_{cap} (cap layer) and i_{chan} (channel) is then calculated as:

$$\frac{S_V}{V^2} = \frac{S_I}{I^2} = \left(\frac{R_{chan}}{R_{cap} + R_{chan}} \right)^2 \cdot \frac{\alpha_{H cap}}{N_{cap} f} + \left(\frac{R_{cap}}{R_{cap} + R_{chan}} \right)^2 \cdot \frac{\alpha_{H chan}}{N_{chan} f} \quad (2)$$

In order to minimize the effect of the noise in the cap layer on the total noise, a very high resistance R_{cap} and a good crystalline quality (low α_{chan} , α_{cap}) is needed. The requirement concerning the relation of the two resistances ($R_{cap} \gg R_{chan}$) has to be increased considerably, because the Hooge parameter in the cap layer can be several orders of magnitudes higher than in the channel. This is caused by surface degradation and small defects due to the high doping level of the upper layer deteriorating its noise behavior. Measurements of different Al-free TLM structures on different samples made of InP/In_xGa_{1-x}As/InP (with x between 0.53 and 0.67) having a 10 nm InGaAs cap layer ($N_D = 8 \cdot 10^{18} \text{ cm}^{-3}$) always showed quite high effective Hooge parameters of about $1 \cdot 10^{-3}$. If the total noise appearing between the contacts is only related to the channel, this effective Hooge parameter will be extracted. In fig. 1 the calculated effective Hooge parameter is shown vs. the free charge concentration (variation due to depletion) of the following structures: channel: $n_s = 1.7 \cdot 10^{12} \text{ cm}^{-2}$, thickness: 12 nm, $\mu_{chan} = 7800 \text{ cm}^2/\text{Vs}$, $\alpha_{H chan} = 8 \cdot 10^{-5}$, cap layer: $N_D = 8 \cdot 10^{18} \text{ cm}^{-3}$, thickness: 10 nm, $\mu_{cap} = 1000 \text{ cm}^2/\text{Vs}$, $\alpha_{H cap} = 8 \cdot 10^{-2}$. Here $\alpha_{H chan}$ was chosen according to literature as for instance [2], and our experimental data from transistor measurements. In contrast to that, the Hooge parameter of the cap layer was chosen significantly higher according to [1], [3]. Thus $\alpha_{H cap} = 8 \cdot 10^{-2}$ seems to be a quite realistic value for this example. Fig. 1 shows that even if the cap layer is depleted to a tenth and its resistance does not affect the total resistance of the parallel conduction, the effective Hooge parameter calculated to $6 \cdot 10^{-4}$ is still more than ten times higher than $\alpha_{H chan}$. Poor ohmic contacts could be excluded as origin of the strong noise, because investigations of HFETs (manufactured with a gate

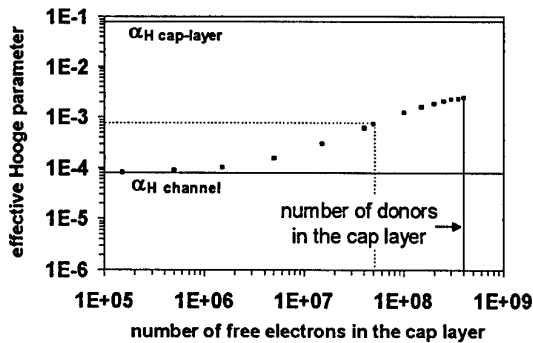


Fig. 1: Calculated effective Hooge parameter of the given parallel conduction ($l = 100 \mu\text{m}$, $w = 50 \mu\text{m}$) vs. the depletion of the cap layer.

recess) existing on the same samples showed parasitic Hooke parameters being nearly two orders of magnitudes lower than the measured ones of TLM structures. This difference will be discussed in the following section.

HFETs biased in the ohmic region can be subdivided into two areas, the parasitic area (index 'par') and the gated area (index 'g'). The normalized spectral noise of this serial combination is thus written as:

$$\frac{S_V}{V^2} = \frac{S_I}{I^2} = \frac{S_R}{R^2} = \left(\frac{R_{\text{par}}}{R_{\text{par}} + R_g} \right)^2 \cdot \frac{\alpha_{H \text{ par}}}{N_{\text{par}} f} + \left(\frac{R_g}{R_{\text{par}} + R_g} \right)^2 \cdot \frac{\alpha_{H g}(\mu_g)}{N_g f}, \quad (3)$$

While the first term describes the noise contribution of the parasitic area, the second term results from the gated area and strongly depends on the gate source voltage V_{GS} . If a depletion type n-HFET is biased with positive gate source voltages in the ohmic region (enhancement mode) the gated area usually has no LF-noise contribution if the gate length L_G is smaller than the parasitic length $L_{DS}-L_G$. The total noise then results from the parasitic area, which is comparable to a TLM structure with cap layer.

The only difference between TLM and HFET is that the current flow in the cap layer of the HFET is suppressed due to the gate recess. In fig. 2 the 1/f-noise behavior of an unstrained HFET is shown in dependence on the effective gate source voltage. From these measurements the Hooke parameter $\alpha_{H \text{ par}}$ describing the parasitic area could be calculated as $\alpha_{H \text{ par}} = 9 \cdot 10^{-5}$. Strained HFETs ($x = 0.67$) showed a lower Hooke parameter of $\alpha_{H \text{ par}} = 5 \cdot 10^{-5}$, which is related to the higher conduction band discontinuity. Due to the lower potential step of the unstrained structure, the electron density distribution function penetrates deeper into the graded channel interfaces. Therefore a poor quality of the channel interface affects the noise less, if the potential step is higher.

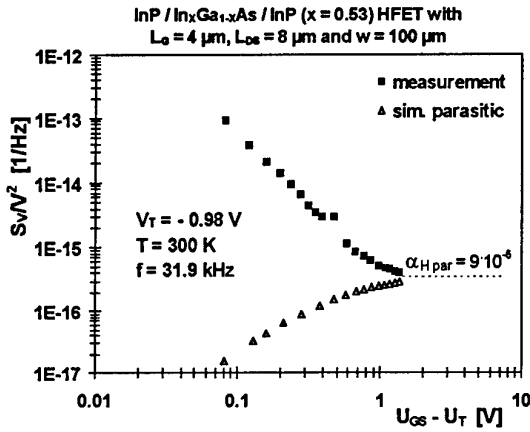


Fig. 2: Measured normalized spectral noise of the given HFET vs. the effective gate source voltage. Additionally the simulated parasitic contribution is shown.

Similar investigations have been performed at strained and unstrained $\text{InAlAs}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{InAlAs}$ heterostructures based on InP with 10 nm thick cap layers ($N_D = 5 \cdot 10^{18} \text{ cm}^{-3}$). This kind of 2DEG devices promise lower LF-noise due to the higher conduction band discontinuity. But on the other hand their noise behavior is very sensible to oxidation processes at the Al-containing layers. Different TLM structures showed quite low effective Hooke parameters of about $2\text{--}4 \cdot 10^{-5}$ independent on strain which results from a excellent quality of crystal of both layers, the channel and the cap layer. These results promise a very low LF-noise of the HFETs because the noise contribution of the cap layer is then totally suppressed. Noise measurements performed at these HFETs manufactured with a channel recess did not come up to the high expectations. On the contrary the HFETs showed a much stronger LF-noise ($\alpha_{H \text{ par}}$ of about $5 \cdot 10^{-4}$), which is related to oxidation processes at the upper InAlAs layer.

The LF-noise investigations of TLM-structures and HFETs made of different materials based on InP showed that the cap layer can have a noise contribution even if its ohmic resistance does not contribute to the total resistance of the parallel conductance. This increase of noise is deduced to defects and surface degradations. For this reason it is necessary to suppress any current in this upper layer. The experiments demonstrate that a gate recess followed by an isolating passivation will be the best way of fabricating noiseless HFETs in order to prevent oxidation processes acting as noise sources.

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Hot-Electron Diffusion Coefficient in Standard Doped InP Channels

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Diffusion coefficient of electrons is one of the most important transport parameters. According to Einstein relation its value at low electric fields is determined by electron mobility. However, this relation does not hold for hot electrons, and independent measurements of diffusion coefficient must be performed at high electric fields. Time-of-flight measurements (often used to measure diffusion coefficient in semi-insulating samples) cannot be applied to conductive channels being of interest for field-effect transistors. Another technique [1] is based on hot-electron noise measurements at microwave frequencies. It has been applied to measure hot-electron and hot-hole diffusion coefficients in elemental and compound semiconductors including lightly n-type InP [2-4], but, to our knowledge, no data on standard doped n-type InP is available.

Figure 1 presents experimental results on longitudinal noise temperature T_n of hot electrons measured for MOVPE-grown n-type InP channels in comparison to those for lightly n-type GaAs and InP. The investigated standard doped n-type InP ($n = 10^{17} \text{ cm}^{-3}$, open circles) and lightly n-type InP (closed circles) demonstrate similar hot-electron noise properties.

The dependence of noise temperature on electric field, $T_n(E)$, together with that of the differential conductivity, $\sigma(E)$, are used to obtain the field dependence of longitudinal diffusion coefficient (Fig. 2):

$$D(E)/D_0 = T_n(E)/T_0 * \sigma(E)/\sigma_0. \quad (1)$$

Two ranges of electric fields are evident in Fig. 2. At fields up to $\sim 8 \text{ kV/cm}$ the differential conductivity decreases, and the decrease prevails over the increase in noise temperature. As a result, the diffusion coefficient decreases (open circles). In this range of fields, velocity fluctuations, conductivity, and electron diffusion are controlled by the kinetic processes inside the central valley. At high electric fields, $E > 8 \text{ kV/cm}$, the intervalley transfer of hot electrons becomes the dominant source of electron velocity fluctuations. Note that the intervalley fluctuations manifest themselves at a lower field as compared to that of the related effects on macroscopic averages (e.g., the threshold field for Gunn effect is around 12 kV/cm).

To our knowledge, this is the first publication of the experimental data on hot-electron diffusion coefficient obtained for a standard-doped InP channel (for the results on lightly n-type InP see [2-4]).

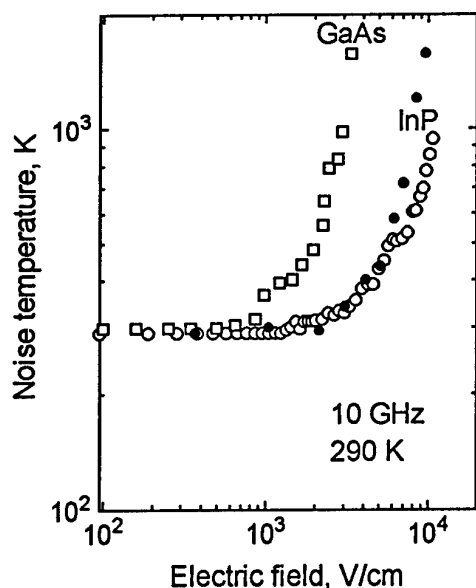


Fig.1. Room temperature data of field-dependent hot-electron noise temperature for n-type GaAs and InP samples containing different density of electrons.

Lightly doped GaAs: $n = 9 \cdot 10^{14} \text{ cm}^{-3}$ [3].

Lightly doped InP: $n = 3.2 \cdot 10^{15} \text{ cm}^{-3}$ (closed circles, [3]);

Standard doped InP: $n = 1 \cdot 10^{17} \text{ cm}^{-3}$, (open circles, present paper).

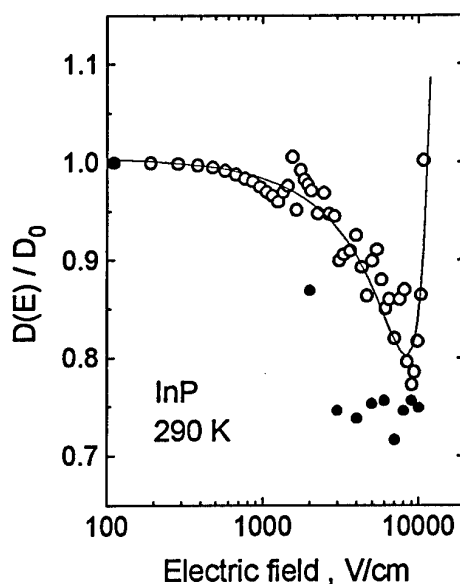


Fig.2. Field dependence of hot-electron diffusion coefficient for n-type InP.

Experimental data:

$n = 2.7 \cdot 10^{15} \text{ cm}^{-3}$, $D_0 = 116 \text{ cm}^2/\text{s}$ (closed circles [2],

$n = 1 \cdot 10^{17} \text{ cm}^{-3}$, $D_0 = 80 \text{ cm}^2/\text{s}$ (open circles, present paper).

Solid line is a fitted polynomial approximation.

In conclusion, hot-electron diffusion coefficient is measured for standard doped n-type InP. The transition from the intravalley fluctuation-controlled diffusion to the intervalley-transfer-dominated diffusion is evidenced at around 8 kV/cm electric field.

Acknowledgments

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Broadband High Efficient X-band MMIC Power Amplifiers for Future Radar Systems

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Abstract

The results of a power amplifier chip set for future radar systems are discussed. Excellent broadband frequency behaviour is shown. A driver amplifier with 50% band width and an output power of more than 1.3 Watt is discussed. A high power amplifier with 30% bandwidth, 5 Watt output power and a Power Added Efficiency of more than 30% is demonstrated. The driver amplifier results demonstrate the capabilities of the pseudomorphic HEMT technology for the development of broadband single chip power amplifiers for future radar systems.

Introduction

Active phased array antenna's form the basis of future advanced radar systems. These phased array antenna's may contain several thousand Transmit Receive (TR) modules. To make such systems economically realisable integration of the TR modules is necessary. This can be realised by reducing the number of MMICs used in a TR module. A picture of a typical future TR module is shown in figure 1.

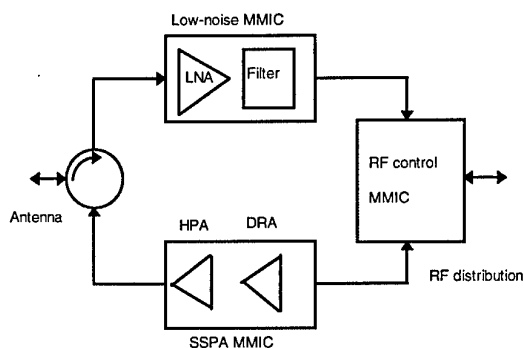


Figure 1: Typical architecture of future TR modules

Developments performed by TNO regarding the Low Noise Amplifier with filter and the RF control MMIC are discussed in [1].

The by TNO developed high efficient broadband power amplifier chip set is discussed in the next sections. The chip set consists of one Driver Amplifier and one High Power Amplifier. These amplifiers have been developed in the scope of the WEAG/TA1/CTP8.1 programme.

This programme was carried out by a consortium consisting of Siemens, Dassault Electrotechnique, Fraunhofer-IAF and TNO-FEL.

Driver Amplifier

The driver amplifier is developed in the pseudomorphic HEMT (PHEMT) process of IAF. This process consists of 0.3 μm HEMTs, E-beam gate technology, MIM capacitors and airbridges. The viaholes and backside processing of the presented amplifier are performed by Siemens.

The goal of the amplifier depicted in figure 2 was to demonstrate that it is possible to develop broadband power amplifiers at X-band with high gain (≈ 30 dB) at a small chip size.

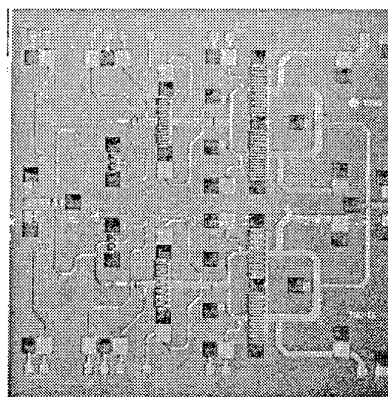


Figure 2: Driver Amplifier, chip size 14.4 mm²

The advantage of the used PHEMT technology over MESFET technology is the increased gain at X-band of the output amplifier stage 12 dB compared to 7 dB. This increased gain makes the realisation of small size power amplifiers possible.

The measurement results of the driver amplifier are depicted in figure 3. The measurement results show that an amplifier has been developed with an output power of more than 1.3 W and 28 dB gain. These results have been obtained between 8 - 13.2 GHz. This shows the potential of the used PHEMT technology for the development of small sized broadband High Power Amplifiers.

At this moment TNO is developing a broadband single chip power amplifier consisting of both driver and High Power Amplifier. With an enhanced version of the PHEMT technology of IAF that has an output power of 1 W/mm FET size.

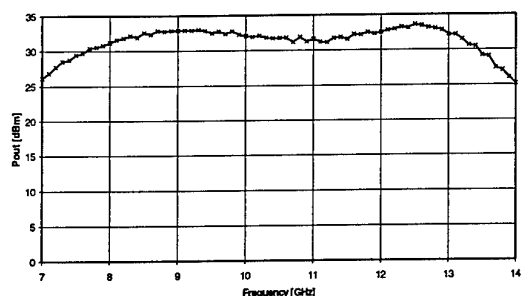


Figure 3: CW measurement result Driver Amplifier ($P_s=3$ dBm)

High Power Amplifier

A 5-Watt High Power Amplifier is developed in the Siemens DIOM20HP process (Refs [1] and [2]). This process consists of 0.5 μ m MESFETs, a self aligned gate technology, localised ion implementation, MIM capacitors, via holes and airbridges. This technology offers high performance, high reliability and good reproducibility at low costs.

A photograph of the realised High Power Amplifier is shown in figure 4. The measured large-signal measurement results are depicted in figure 5.

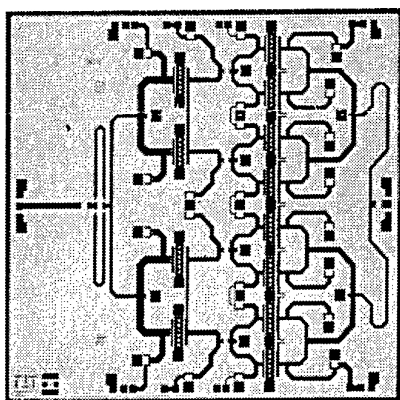


Figure 4: 5-Watt High Power Amplifier, chip size 22 mm²

The measurement results show that an excellent performance has been obtained. The pulsed output power is more than 5-Watt over a 30% bandwidth. The Power Added Efficiency is more than 30% over a 30% bandwidth. At 8.8 GHz a peak output power of 7-Watt and a Power Added Efficiency of 40% has been measured.

MESFETs with a reduced drain-source spacing, but well within the maximum tolerable temperature limits, are used to reduce amplifier size. The output matching of the transistors is based on measured load-pull data. The load-pull data is obtained with an in-house developed unique high-power on-wafer active load-pull system that is capable of providing load impedances with reflection

coefficients up to 1.

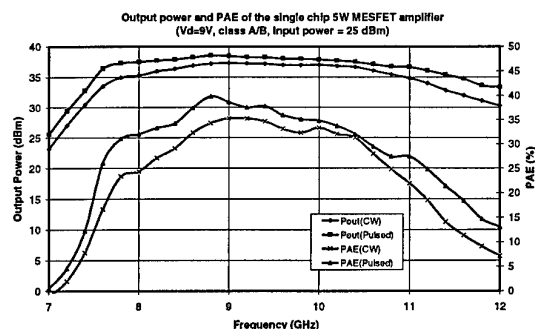


Figure 5: Measurement results 5-Watt High Power Amplifier

Multiple-order input, interstage and output matching networks are used in order to obtain the required bandwidth. Careful attention is paid to make the amplifiers stable. Stability analysis is carried out for all odd and even modes using open-loop transfer function techniques. Amplifier design is carried out with HP-EEsof software using the EEFT3 transistor models. Parameter extraction for this model is optimised to obtain a good agreement over the required bandwidth between model predictions and measured transistor performance under high power conditions and under optimum load conditions. Parameter extraction is carried out on transistors with exactly the same size as those used in the high power amplifier. A typical example is shown in figure 6.

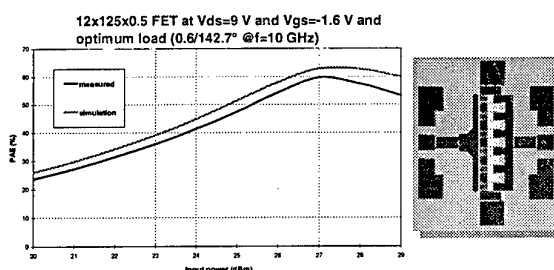


Figure 6: Agreement between modelled and measured PAE of the transistor shown on the right side.

Conclusions

The driver amplifier developed in the PHEMT process of IAF has a frequency bandwidth of more than 50%, an output power of more than 1.3 Watt and a gain of more than 28 dB. The in the Siemens DIOM20HP process developed High Power Amplifier shows excellent output power of more than 5-Watt over a frequency band of 30% at X-band. The power Added efficiency is more than 30% over this frequency band.

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On the Design and Application of Narrow Tuneable MMIC Filters

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Introduction

System designers world-wide require miniature microwave filters. The potential market for these filters is enormous. For narrow tuneable microwave filters, no off-the-shelf solutions are available. Specific areas where these filters are needed are high-performance front-ends such as used in e.g. satellite communication systems, radar systems and measurement equipment.

Over the last five years, we have investigated monolithic GaAs filter integration. One of the results of these research efforts has been a design strategy to integrate narrow band pass filters. This strategy will be discussed as well as recent results.

Design strategy

The main reason for the introduction of active elements in monolithic filters is the lack of high-quality passive components in standard GaAs technology. This limit results in filters that have at best a moderate bandwidth. Results of our research efforts were obtained using active inductors. The active inductors are separately optimised to provide an optimal large-signal performance. They are used to form a tapped active resonator, where the tap is used to obtain a low impedance. The resonator is then used to form a band stop filter. Band stop filters have been individually characterised, measured results will be shown. The band stop filter is in turn used in a differential structure, together with a matched broadband amplifier to result in the desirable band pass response. Measured results for these filters will be shown. The bandwidth was measured to be as low as approximately 70 MHz, the noise figure 6 dB and the tuning range from 9 to 11 GHz.

The filters were realised in Philips' d02ah process, using 0.2 μm PHEMTs that offer an f_T of 62 GHz.

Non-ideal effects

The resulting filters have a limited dynamic range. For the band pass filters described, however, the large-signal behaviour is highly frequency dependent. In the pass band, the sensitivity for large signals is high. Large signals result in an increasing insertion loss. For the signals outside the pass band, where the large signals to be suppressed are expected, this sensitivity is significantly lower. Since large signals must be suppressed when outside the pass band, the situation may be well tolerable.

Conclusion

Although the use of narrow MMIC filters in high-performance front-end requires a careful trade-off, we believe that the introduction of MMIC filters adds significant advantages to the performance of the front-end. The filters are the only available option, whenever small, fast-tuneable filters are needed.

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Area		Application	Advantages
Civil	Communication	portable telephones	small, light, potentially inexpensive
		communication satellites	small, light, remotely tuneable
	Instrumentation	generators	less expensive
		receivers	less expensive
military	Radar	broadband phased-arrays	small, low-cost, high tuning speed
	Electronic Warfare	frequency hopping	high tuning speed

Figure 1: Table summarizing the main applications of narrow MMIC tuneable filters.

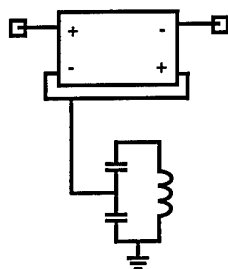


Figure 2: Schematic of the band stop filter.

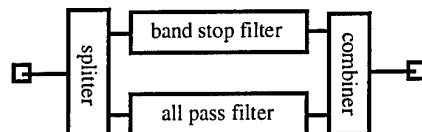


Figure 3: Topology of the band pass filter.

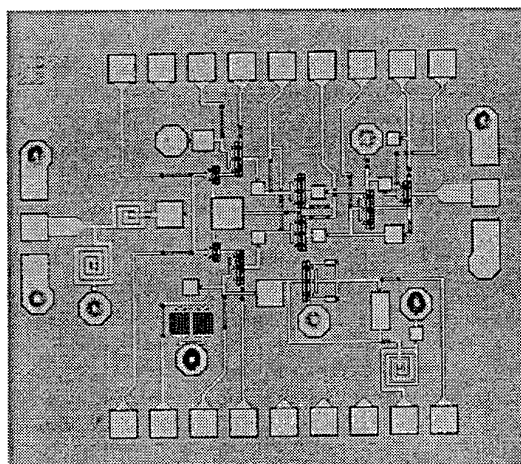


Figure 4: Layout of the tuneable band pass filter.

NOISE ANALYSIS OF InGaAs MIXER DIODES AT MILLIMETER-WAVE AND FAR-INFRARED FREQUENCIES¹

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InGaAs Schottky mixer diodes permit operation with reduced local oscillator power (P_{LO}) compared with GaAs diodes and combine high sensitivity with integration capability with other InP-based components. Diode design should lead to both conversion loss (L_c) and noise temperature (T_{mix}) minimization. There are, however, several trade-offs that need to be made in such optimization. For example high highly doped or thin n-InGaAs layers permit conversion loss reduction but may introduce tunneling currents and thus noise. The use of InGaAs instead of GaAs allows larger Γ -L valley separation and thus reduced mixer losses due to electron scattering and intervalley transfer. Moreover, the diode behavior needs to be analyzed under realistic non-equilibrium dynamic conditions as occurring in practice. It is the purpose of this paper to present L_c and T_{mix} extraction as obtained by Monte-Carlo simulation for various designs and compare such data with experimental results

The InGaAs diodes considered in this work were similar to the ones previously reported by the authors and consisted of a low doped ($\sim 2 \times 10^{17} \text{cm}^{-3}$) n- region with thickness in the range of 500Å to 2000Å and having a 1.4µm anode diameter. The DC bias diode noise ($S_{DC10GHz}$) was measured at 10GHz and the simulated noise was obtained from the short-circuit noise and current characteristics obtained from Monte-Carlo analysis. Good agreement in noise characteristics is obtained between measured and simulated characteristics at low bias current I_{DC} . However, as I_{DC} increases, the measured noise increases more rapidly while their dynamic resistance remains relatively low ($\sim 17\text{ohm}$). Furthermore the measured noise showed an inverse relation with frequency which was more pronounced at higher I_{DC} ; the noise temperature (T_{DC}) declined by about an order of magnitude as the frequency increased from 1.4GHz to 10GHz. These results indicate that InGaAs mixer diodes biased beyond their Schottky barrier height exhibit noise that is dominated by a mechanism which is not due to effects taken into account in our Monte-Carlo model such as hot electron effects, impact ionization and intervalley transfer.

InGaAs and GaAs diodes of the above doping and 500Å n- layer thickness were simulated as mixers as a functions of frequency and P_{LO} and their T_{mix} and L_c showed the expected increases with frequency. The results demonstrate the superior performance of InGaAs vs. GaAs diodes in terms of noise. The increase of noise with frequency is related to the increased importance of scattering as the frequency increases while the improved performance of InGaAs mixer diodes is related to the InGaAs material's lower scattering rates and effective mass. At 1.2THz, similar InGaAs and GaAs diodes present minimum, double-sideband (DSB) T_{mix} 's of 385K and 430K respectively, with respective associated single-sideband (SSB) L_c 's of 5.7dB and 6.4dB. A much

¹ This work was sponsored by ARO-URI Contract No. DAALO3-92-G-0109

higher advantage is expected at 4.8THz where the respective minimum InGaAs and GaAs DSB T_{mix} 's are 1213K and 2106K with associated respective SSB L_c 's of 10dB and 11dB.

Overall, we present the noise and conversion loss characteristics of high performance InGaAs diodes for millimeter-wave and far-infrared frequency operation, analyze their noise properties by means of Monte-Carlo simulation which allows consideration of non-equilibrium effects and compare their performance to the more traditional mixer technology based on GaAs.

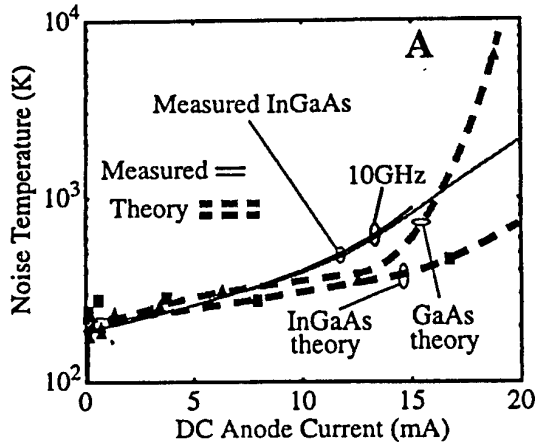


Fig. 1A: Noise temperature, T_{DC} , vs. DC bias current. Here the n-layer thickness and doping are 2000Å and $2 \times 10^{17} \text{cm}^{-3}$ respectively.

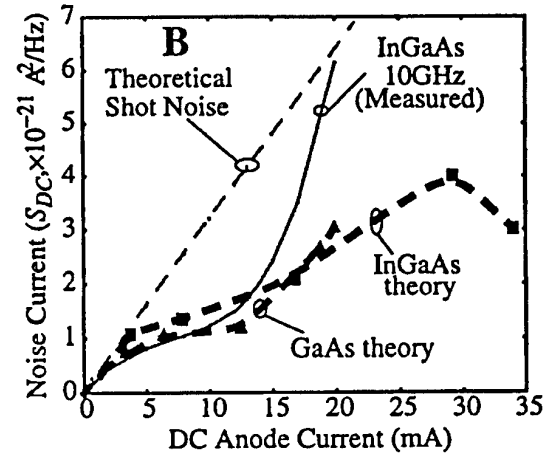


Fig. 1B: Noise current squared, vs. DC bias current. Here the n-layer thickness and doping are 2000Å and $2 \times 10^{17} \text{cm}^{-3}$ respectively.

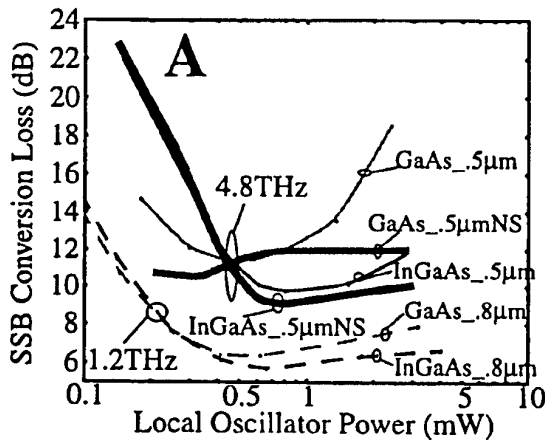


Fig. 2A: Simulated single-sideband mixer conversion loss as a function of local oscillator power and frequency for InGaAs and GaAs diodes having anode diameters of 0.5μm and 0.8μm. Here the n-layer thickness and doping are 500Å and $2 \times 10^{17} \text{cm}^{-3}$ respectively. The NS suffix means these diodes were simulated with all electron scattering mechanisms disabled.

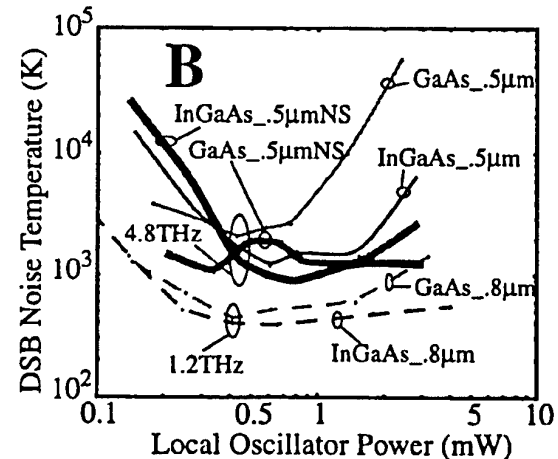


Fig. 2B: Simulated double-sideband mixer noise temperature as a function of local oscillator power and frequency for InGaAs and GaAs diodes having anode diameters of 0.5μm and 0.8μm. Here the n-layer thickness and doping are 500Å and $2 \times 10^{17} \text{cm}^{-3}$ respectively. The NS suffix means these diodes were simulated with all electron scattering mechanisms disabled.

Monday, May 26

16.00 - 18.00 Session 4: Quantum Effects and Tunneling

- 16.00 1. (Invited Paper) *K. Von Klitzing, Max Planck Institute Stuttgart:*
"Semiconductor quantum devices"
- 16.30 2. (Invited Paper) *M. Yamamoto, NTT System Electronics Labs.:*
"Resonant Tunneling Diode and HEMT Integrated Devices and Circuits".
- 17.00 3. *A. Sigurdardottir, K. Mutamba, A. Vogt and H.L. Hartnagel:*
"Investigation on Tunnelling Effect in Stressed InAs/AlSb/GaSb-Resonant Tunnelling Diodes".
4. *M.I. Lepsa, Th.G. Van de Roer, J.J.M. Kwaspen, W. Van der Vleuten, L.M.F. Kaufmann:*
"Three Terminal Double Barrier Resonant Tunneling Devices Based on the Direct Contacting of the Quantum Well".
5. *Jozsef Karanyi and Bela Szentpali:*
"Quantum mechanical tunneling in GaAs ohmic contacts".
6. *J.J. M. Kwaspen, M.I. Lepsa, Th.G. Van de Roer, W. Van der Vleuten, H.C. Heyker, L.M.F. Kaufmann:*
"Accurate Equivalent-Network Modeling of GaAs/AlAs Based Resonant Tunneling Diodes with Symmetrical Thin Barrier and Spacer Layers"

Semiconductor Quantum Devices

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Epitaxial growth is an established method for the production of a large number of semiconductor devices where the thickness of the active layer has to be controlled with high accuracy. Quantum wells, resonant tunnel diodes, superlattices or the cascade laser are typical examples. Whereas the control of layer thicknesses in the growth direction for the realization of two-dimensional electron systems is relatively simple, optical and electron beam lithography are normally necessary to produce a lateral confinement of the electronic system in the range $0.05 - 0.5 \mu\text{m}$ (one- and zero-dimensional electron systems). However the Stranski-Krastanov growth and the MBE-growth on patterned substrates opened new ways for the realization of one- and zero-dimensional electron system. Recent optical and transport measurements on self-assembling InP and GaAs quantum dots are presented with the focus on single electron devices.

Resonant Tunneling Diode and HEMT Integrated Devices and Circuits

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This paper reports our recent activities aiming at constructing quantum functional devices and circuits based on the monolithic integration of InP-based resonant tunneling diodes (RTDs) and high electron mobility transistors (HEMTs).

We demonstrate an approach of employing series-connected resonant tunneling (RT) devices with a peak current modulation scheme driven by an oscillating bias voltage. This approach makes possible the implementation of a variety of quantum functional circuits with reduced complexity. The principle of operation is to control the switching sequence of these RT devices at the rising edge of the oscillating bias voltage by changing the effective peak currents, using control gates. We employed a newly developed InP-based RTD and HEMT parallel-connected integrated device. In this device, the effective peak currents can be modulated through the gate voltage applied to the HEMT.

We also report that an InP-based resonant tunneling high electron mobility transistor (RTHEMT) features a pronounced negative differential resistance (NDR) and a negative transconductance, and is suitable for high-performance RF device applications.

With the use of an RTD as a quantum effect device in combination with a HEMT, these InP-based RTD/HEMT integrated devices and circuits can fully utilize the functionality arising from NDR at room temperature.

I. Introduction

The negative differential resistance (NDR) of resonant tunneling (RT) devices offers the possibility of greatly reducing circuit complexity [1-5]. A resonant tunneling diode (RTD) provides clear NDR at room temperature. It also provides high peak current density, resulting in ultrahigh-speed switching times that reach 1.5 ps for InP-based RTDs [6].

To create viable quantum functional devices and circuits, the development of circuit configuration that can fully utilize NDR characteristics is indispensable. The development of a three-terminal RT device suitable for integration is also a key issue.

A monostable-to-bistable transition logic element (MOBILE) consists of two series-connected RT devices with a peak current modulation scheme and is driven by an oscillating bias voltage [4]. A MOBILE provides multi-input and multi-output capabilities without sacrificing the intrinsic high-speed characteristics of RTDs. It also features weighted sum threshold logic with both positive and negative weights [7].

These advantages make MOBILEs suitable for applications in parallel processing architectures for computation such as artificial neural networks or cellular automata [4]. Indeed, simple one-dimensional cellular automata for a random sequence generator have been demonstrated [8].

We recently demonstrated that a variety of functional circuits of reduced complexity can be constructed by extending the circuit concept of the MOBILE to include three or more RT devices connected in series. The principle of operation behind a generalized circuit is to control the switching sequence of these RT devices at the rising edge of the oscillating bias voltage by changing the effective peak currents, using control gates. The basic RT device we employed was a newly developed

InP-based RTD and high electron mobility transistor (HEMT) parallel-connected integrated device in which the effective peak currents could be modulated through the gate voltage applied to the HEMT.

Based on this circuit concept, we designed a literal gate (one of the fundamental multiple-valued logic gates), an analog-to-quaternary quantizer, and a programmable logic gate performing AND, OR, NAND, NOR and XOR according to the appropriately applied control voltages. We fabricated these, using the InP-based RTD/HEMT monolithic integration technology. We then experimentally confirmed the proper operation of these functional circuits at room temperature.

The InP-based resonant tunneling high electron mobility transistor (RTHEMT) incorporated a pseudomorphic InGaAs/AlAs/InAs RTD into the source of a non-alloyed ohmic contact InAlAs/InGaAs HEMT. We demonstrated that this device features a pronounced NDR and a negative transconductance also at room temperature.

II. InP-Based Resonant Tunneling Diode and HEMT Integrated Device in Parallel Connection

Development of a basic NDR device with a peak current modulation capability suitable for integration is essential in furthering the applicability of quantum functional circuits based on MOBILEs. We recently developed an InP-based RTD and HEMT parallel-connected integrated device [9]. Its epitaxial layer structure is shown in Fig. 1. The effective peak current can be modulated through the gate voltage applied to the HEMT, as shown in Fig. 2. This approach enables the separate optimization of an RTD showing NDR characteristics and a HEMT responsible for peak current modulation. This separate optimization is advantageous for reproducibility and uniformity, which are indispensable for integration.

On the same wafer, we obtained a high peak current density of $9 \times 10^4 \text{ A/cm}^2$ with a good peak-to-valley ratio of 5.5 for InGaAs/AlAs/InAs RTDs and a maximum transconductance of 850 mS/mm for 0.7 μm -gate-length InAlAs/InGaAs HEMTs at room temperature.

Another advantage of this technology is that it enhances circuit design flexibility by using RTD/HEMT integrated devices with a combination of HEMTs in peripheral circuits on the same wafer.

III. Quantum Functional Circuits Based on Series-Connected Resonant Tunneling Devices with Peak Current Modulation Capability

To further the applicability of MOBILEs, it is also essential to develop a variety of quantum functional devices and circuits. For this purpose, we recently proposed a monostable-multistable transition logic gate (MML). This is based on a generalization of the device concept of the MOBILE, by increasing the number of series-connected RT devices up to three or more [10]. The principle of operation is to control the switching sequence of these RT devices during the critical period of increasing the oscillating bias voltage by changing the effective peak currents, using control gates, before this critical period.

Figure 3(a) shows a circuit configuration of a literal gate composed by the MML device concept [10]. A literal gate is one of the basic logic gates in multiple-valued logic (MVL). The present literal gate is composed of the three NDR devices A, B and X connected in series and driven by an oscillating bias V_{CK} . The effective peak currents of NDR devices B and X are modulated through the gate voltages applied to HEMT1 and HEMT2 connected in parallel with the RTDs B and X, respectively. The maximum value of V_{CK} is selected so that one of the three NDR devices is switched from the peak to valley state. The device switched at the rising edge of V_{CK} is the one having the smallest effective peak current. By designing the transconductance of HEMT1 and HEMT2 differently through the gate widths, we can control the relative magnitude of peak currents, as shown in Fig. 3(b).

Based on this principle, we can obtain the literal operation. Its V_{out} versus V_{in} characteristics are shown in Fig. 3(c). By using the InP-based RTD/HEMT integration technology, we successfully demonstrated the literal operation at room temperature, as shown in Fig. 3(d).

The device concept of the present literal gate can be extended to implement a two-input logic gate. Furthermore, by introducing two control voltages, a programmable logic gate can be constructed [11]. Its circuit configuration is shown in Fig. 4(a). By varying the control voltages V_{con1} and V_{con2} , one of the five logic functions of AND, OR, NAND, NOR and XOR can be selected. By varying the maximum value of the oscillating bias voltage, the logic function of XNOR can also be obtained. The programmable logic functions were confirmed experimentally, and the EXOR operation is shown in Fig. 4(b). This flexible logic gate is promising for the implementation of programmable logic circuits.

The literal gate and programmable logic gate described above include one NDR device between the output terminal and ground, resulting in an output level of "1" or "0". By increasing the NDR device number up to two or more between the output terminal and ground, MVL circuits having multiple-valued output can be constructed.

Figure 5(a) shows the circuit configuration of an analog-to-quaternary quantizer consisting of six NDR devices connected in series, where three NDR devices X, Y, and Z are involved between the output terminal and ground [12]. The maximum value of the oscillating bias voltage V_{CK} is chosen so that the three NDR devices out of the six are switched. By varying the relative magnitude of the effective peak currents of NDR devices through the input signal applied to the HEMT as shown in Fig. 5(b), the switching sequence can be controlled. This results in the V_{out} vs. V_{in} characteristics shown in Fig. 5(c). Here, four different levels of output voltage were obtained as a function of V_{in} . These resulted from the differing number of switched NDR devices involved between the output terminal and ground at the rising edge of V_{CK} . Proper operation was also confirmed experimentally, as shown in Fig. 5(d).

The present analog-to-quaternary quantizer will be useful for implementation of multiple-valued logic circuits and analog-to-digital converters.

These quantum functional circuits are advantageous in reducing circuit complexity in terms of total number of devices and logic gates in the critical path. This in turn would result in low power consumption and high-speed operation.

IV. InP-Based Resonant Tunneling HEMT

In implementing high-performance analog RF devices, it is essential to utilize active devices with strong nonlinear characteristics. To achieve functional devices with such characteristics, we recently developed an InP-based resonant tunneling high electron mobility transistor (RTHEMT) [13].

An InP-based RTHEMT incorporates a pseudomorphic InGaAs/AlAs/InAs RTD into the source of a non-alloyed ohmic contact InAlAs/InGaAs HEMT. Figure 6(a) shows an SEM photograph of a fabricated RTHEMT. The epitaxial layer structure is the same for the RTD and HEMT parallel-connected integrated device, and only the wiring is altered to obtain the series connection of an RTD and a HEMT.

Figure 6(b) shows the source-drain I-V characteristics of an RTHEMT at room temperature. A pronounced NDR is clearly obtained. A most significant feature is that the drain current I_{DS} saturates near the valley current after the resonance peak. The key mechanism of this near-flat valley current is ascribed to the drastic change of the potential of the floating source (V_s) of the HEMT arising from the switching of the RTD from peak to valley that occurs when the I_{DS} exceeds the RTD peak current. The result is the decreased effective gate voltage (V_{GS}) and hence lowered saturation current of the HEMT. The effect is enhanced by the high transconductance and significantly reduced parasitic resistance of the present non-alloyed ohmic contact InAlAs/InGaAs HEMT.

Figure 6(c) shows the transfer characteristics at $V_{DS} = 2$ V; a pronounced negative transconductance (NT) is clearly shown. As a result of the near-flat valley current, the NT is obtained in a wide range of V_{DS} . This is attractive for circuit applications with a large operating margin.

The strong nonlinearity of the RTHEMTs presented here is highly preferable for use in high-performance analog devices, including frequency multipliers [14], mixers, oscillators, etc.

V. Summary

In summary, we have shown that a novel class of logic circuits, such as literal gates, programmable logic gates, and analog-to-quaternary quantizers, featuring enhanced design flexibility along with reduced circuit complexity, could be constructed based on series-connected resonant tunneling devices with a peak current modulation scheme driven by an oscillating bias voltage.

We have developed an InP-based RTD and HEMT parallel-connected integrated device for use as a basic resonant tunneling device capable of peak current modulation. We have successfully employed this device to demonstrate the proposed quantum functional circuits at room temperature.

We have also demonstrated that the RTHEMT, having an InGaAs/AlAs/InAs RTD incorporated into the source of an InAlAs/InGaAs HEMT, features a pronounced negative differential resistance with a near flat valley current and a negative transconductance.

Clarification of useful targets for applications is a key issue for further advancement. In this context, high-performance RF analog circuits constructed with RTHEMTs are highly attractive. The literal gate and analog-to-quaternary quantizer offer the potential to construct viable multiple-valued logic circuits. Furthermore, the analog-to-quaternary quantizer will be useful for the implementation of high-speed analog-to-digital converters. The programmable logic gate is promising for the implementation of programmable logic circuits.

The RTD/HEMT integrated devices and circuits offer enhanced functionality and room temperature operation. We expect them to be useful in future electronic systems.

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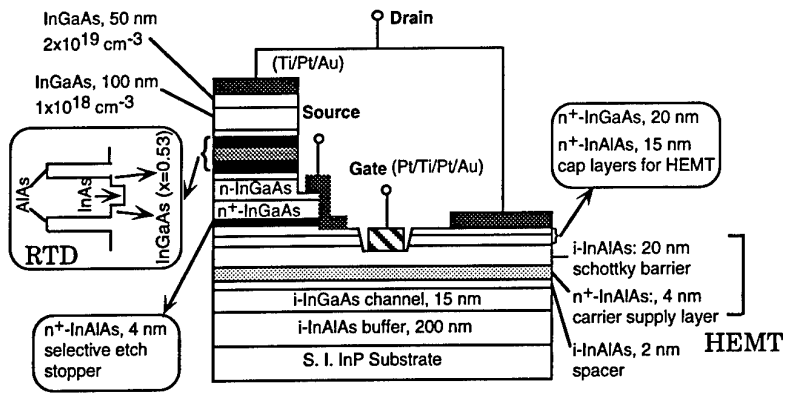


Fig. 1. Schematic cross section of the InP-based integrated device, in which an RTD and HEMT are connected in parallel.

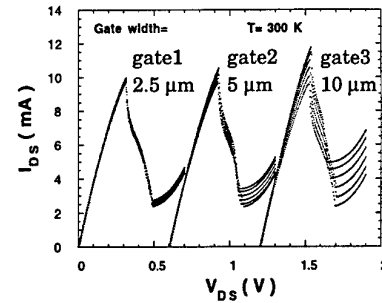


Fig. 2. I-V characteristics of an integrated device, in which one RTD is in parallel with three HEMT's with a nominal 1: 2: 4 (2.5 : 5 : 10 μm) gate width ratio. The modulation amplitude is proportional to the total current. The curves for gates 2 and 3 are shifted from the origin for clarity.

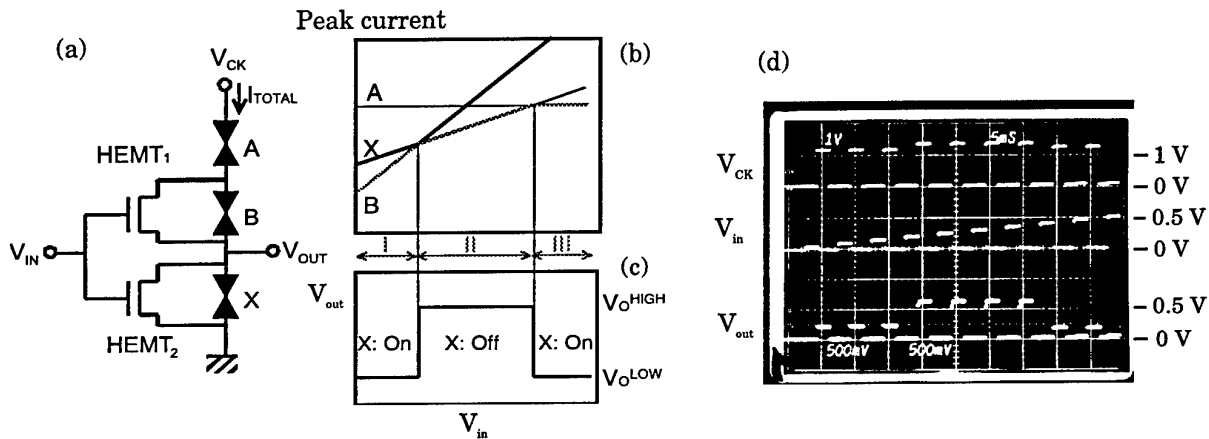


Fig. 3. Literal gate. (a) Circuit configuration. (b) Effective peak currents of A, B, and X as a function of V_{in} . (c) V_{out} vs. V_{in} characteristics showing literal operation. (d) Literal operation obtained for a fabricated circuit at room temperature.

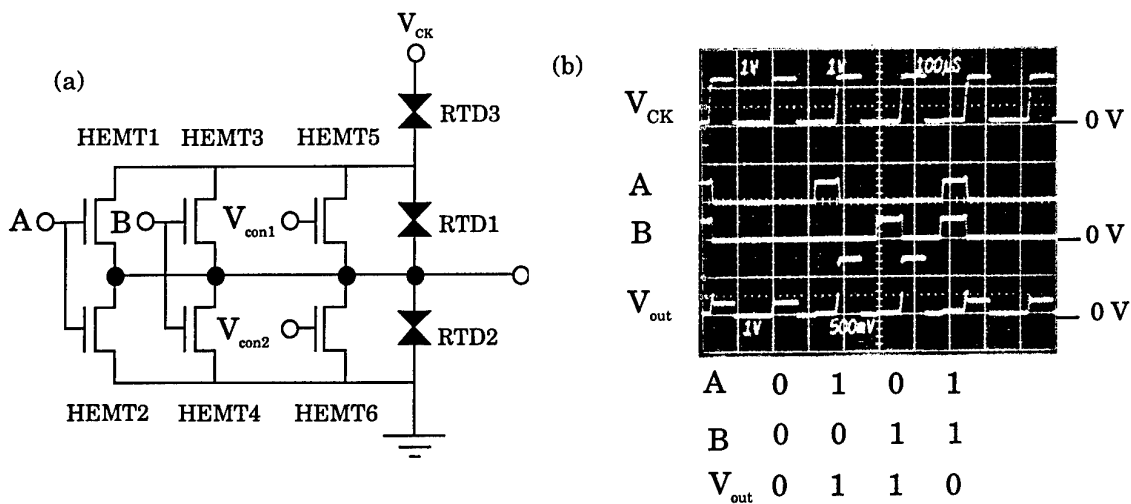


Fig. 4. Programmable logic gate. (a) Circuit configuration. (b) Experimental demonstration of the XOR operation.

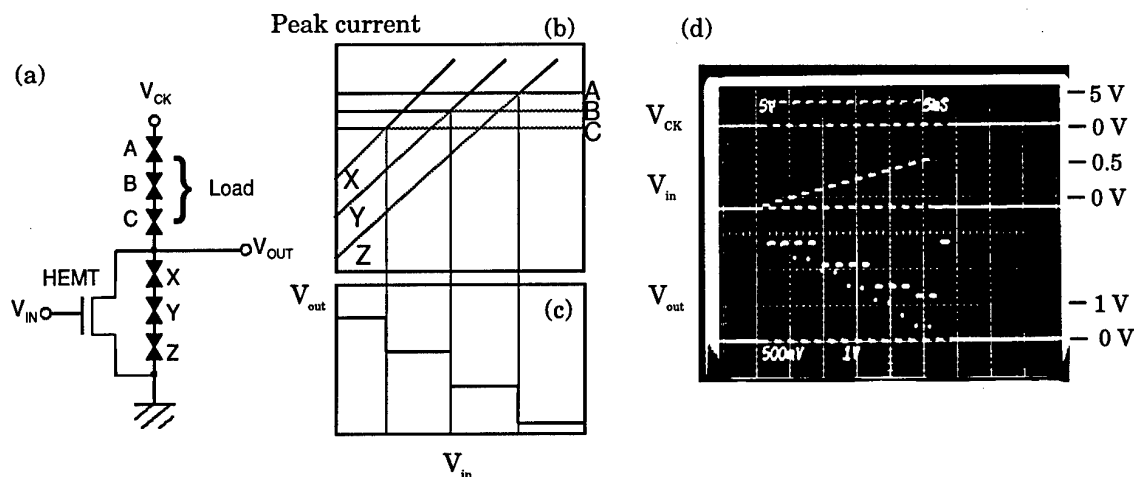


Fig. 5. Analog-to-quaternary quantizer implemented with six NDR devices connected in series. (a) Circuit configuration. (b) Effective peak currents of six NDR devices as a function of V_{in} . (c) V_{out} vs. V_{in} characteristics. (d) Circuit operation of a fabricated analog-to-quaternary quantizer.

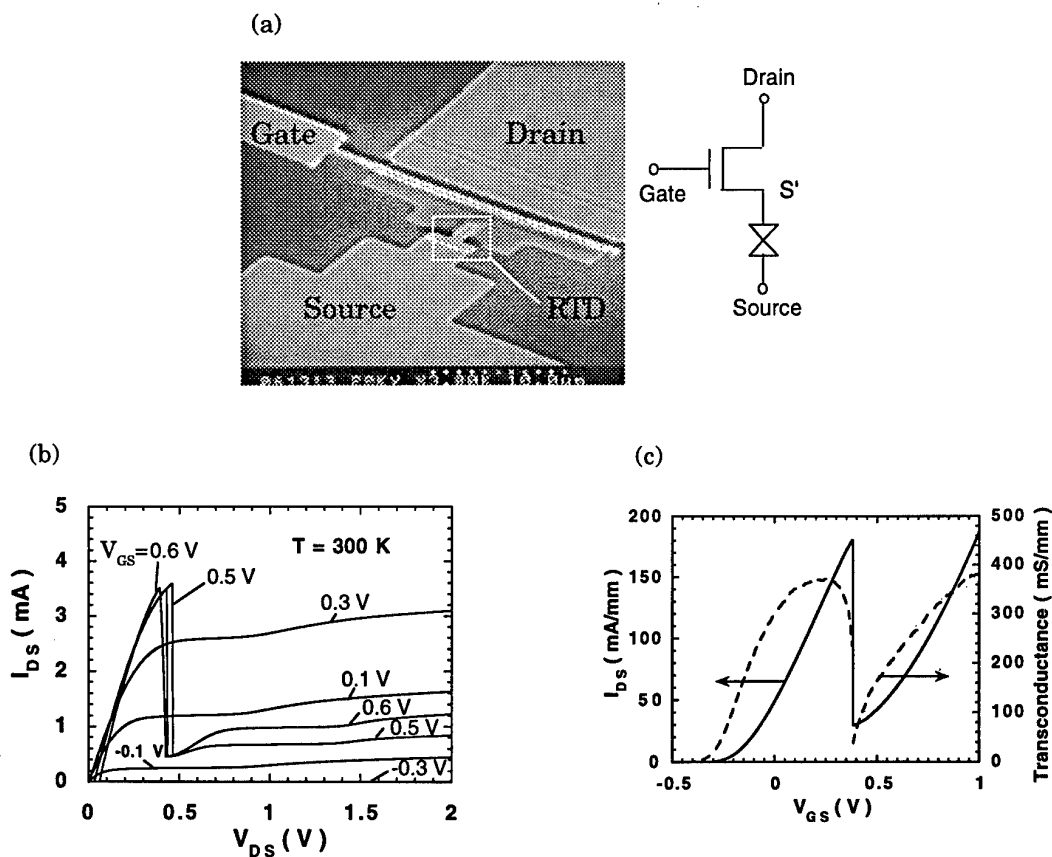


Fig. 6. Resonant tunneling HEMT. (a) SEM photograph of a fabricated RTHEMT. The RTD has an area of $2 \times 3 \mu\text{m}^2$. The gate length is $0.7 \mu\text{m}$ and width is $20 \mu\text{m}$. The inset shows the equivalent circuit. (b) The source-drain I-V characteristics at room temperature. (c) The transfer characteristics at $V_{ds} = 2 \text{ V}$.

Investigation on Tunnelling Effect in Stressed InAs/AlSb/GaSb-Resonant Tunnelling Diodes

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In the last years resonant tunnelling diodes (RTDs) have been of increasing interest for different applications. Several studies including both fabrication and characterization of RTDs have been carried out in order to increase for example the peak to valley current ratio and the peak current. For high frequency applications the device capacitance is of an extremely high importance. Some capacitance models for AlAs/GaAs- and GaAs/GaAlAs RTDs have already been introduced in [1], [2] and [3]. An interesting application of a double barrier RTD (DBRTD) as a pressure sensor has been presented in [4] and [5].

For an improved understanding of the tunnelling effect and the capacitance in DBRTDs we measured the current voltage characteristics and the capacitance voltage characteristics of InAs/AlSb/GaSb-resonant interband tunnelling diodes (RITD) as a function of uniaxial pressure. The RITDs show a special pressure dependence of the current voltage characteristics, which is due to the particular tunnelling path involved in the conduction mechanism.

The RTDs considered here have been grown by MBE on a (001)-oriented GaAs substrate. They consist of two undoped AlSb barriers of width 25 Å and an undoped 65 Å GaSb quantum well. There are 10 nm thick undoped InAs spacer layers on both sides of the double barrier structure. The double barrier structure is sandwiched between two $1 \times 10^{17} \text{cm}^{-3}$ n-doped InAs injection layers of 50 nm width. The electrodes consist of heavily doped ($1 \times 10^{18} \text{cm}^{-3}$) InAs layers. Non-alloyed Cr/Au ohmic contacts have been used.

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THREE TERMINAL DOUBLE BARRIER RESONANT TUNNELING DEVICES BASED ON THE DIRECT CONTACTING OF THE QUANTUM WELL

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Abstract

Three terminal (3T) Double Barrier Resonant Tunneling (DBRT) devices with the base contact to the quantum well have been fabricated from GaAs/AlAs material system. The plane of the very thin quantum well is reached using high selective etching processes and a nonalloyed Ti/Pt/Au metallization scheme is used to obtain a Schottky base contact. DC and AC electrical measurements demonstrate that the base contact lies on the quantum well of the device DBRT structure and the base voltage modulates the collector current. It is shown that the electrical characteristics of these devices enlarge the possibilities of investigation of the DBRT structures and suggest important applications in high-speed electronics.

Introduction

From the beginning the long range application of the resonant tunneling structures was their implementation in three terminal devices. A particularly powerful concept for achieving this has been to incorporate a double barrier resonant tunneling structure into one or another of the junction or transport regions of a bipolar [1], hot electron [2], or field effect transistor [3]. In this implementation the primary operational parameters are those of the "traditional" device, with the tunneling features added to alter these characteristics. However, in order to take advantage of the potential high speed and small size of the resonant tunneling structures it is obvious that the structure itself had to be processed for a 3T device. This approach consists in to make direct contact to the quantum well of a DBRT structure and thereby form a 3T device in which the quantum well base is two-dimensional (2D), with transport proceeding from three dimensional (3D) emitter to 2D base and then to 3D collector. The primary challenge of this approach consists in the difficulty of exposing and making contact to a such thin layer ($\sim 5\text{nm}$) as the quantum well base. This technological obstacle determined that similar tries for the obtaining of 3T-DBRT devices to conduct only to partial results [4, 5], the total settlement of the problem being under way. In this paper we propose a solution to fabricate such a 3T-DBRT device, based on GaAs/AlAs material system. Our 3T-DBRT device originates from a "classical" DBRT structure so a transistor action is not obtained because there is no separation between the controlling and current-carrying electrons. Even then, it demonstrates interesting electrical properties which permit for example the investigation of the switching characteristics of the DBRT structure and suggest some applications.

Device Description and Fabrication

A schematic cross section of the 3T-DBRT device is shown in Fig. 1. The GaAs/AlAs heterostructure was grown by molecular beam epitaxy on a semi-insulating GaAs substrate. The double barrier region, comprising 2.5 nm barriers and a 5 nm quantum well, was embedded by 2.5 nm GaAs spacer layers, all unintentionally doped. Surrounding these layers were grown low doped and contact (n^{++}) GaAs layers. The device processing consisted mainly in mesa etching steps for the collector, base and emitter definition, followed by the corresponding contact deposition using the lift off technique. In all these processes optical lithography was used. The plane of the quantum well was reached by high selective dry etching using pure Freon[®] 12 (CCl_2F_2) in conventional planar RIE system while the other two mesa processes were carried out by wet chemical etching. The metallization scheme consisted of Ge/Ni/Au for the emitter and collector ohmic contacts and Ti/Pt/Au for the quantum well base contact. Finally, specific contact pads suitable for microwave measurements using Cascade probes were deposited and air bridge interconnections were grown between these and the device contacts by gold electroplating.

Results

Both three terminal and two terminal DC I-V characteristics of the 3T-DBRT devices were measured (see Figs. 2 and 3). The I-V characteristics between Base-Emitter (B-E) and Base-Collector (B-C) terminals demonstrate that the base contact lies on the quantum well of the device DBRT structure. During processing a thin oxide layer is interposed between the base (Schottky) contact and quantum well material. The DBRT structure which arises between the oxide layer and the second AlAs barrier of the basic

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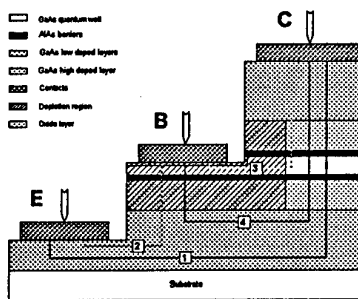


Fig. 1 Schematic cross section of the 3T-DBRT device. The paths 1, 2, 3 and 4 indicate the possibilities of the current flow.

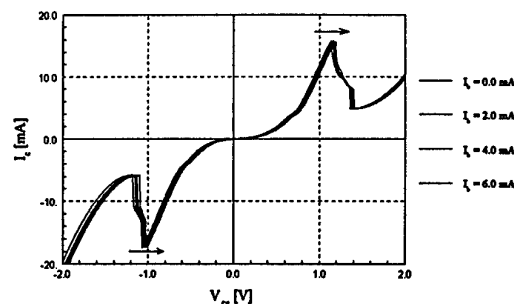


Fig. 2 Common emitter I-V characteristics of the 3T-DBRT device for different base constant currents.

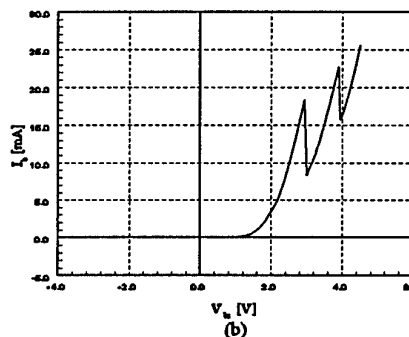
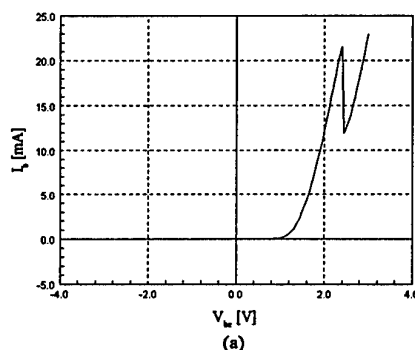


Fig. 3 Two terminal B-E (a) and B-C (b) I-V characteristics of the 3T-DBRT device.

structure accounts for the B-E characteristic. Further on, the B-C characteristic is the result of two DBRT structures connected in series because the large depletion region underneath and laterally the base surface determines the current to follow the path 4, showed in the cross-sectional picture of the 3T DBRT device. Further on, the common-emitter characteristics of the device presented in Fig. 3 show clearly that the collector current is modulated by the quantum well base potential. They can be explained, qualitatively, making use of the physical picture (energy band diagram) of the DBRT structure. The device transfer characteristic (collector current function of base current) shows abrupt switching properties. Using microwave measurements, the conclusions established in DC conditions have been confirmed. We have used the third device terminal to measure the switching time of our DBRT structure in a much more simple way than previously reported efforts [6, 7]. The experimental value for this parameter is in accordance with the theoretical estimation using the DC properties of the device.

The electrical characteristics of our 3T-DBRT devices suggest the possible use of these in fast switching applications and high-frequency tuned oscillators.

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Quantum mechanical tunneling in GaAs ohmic contacts

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The ohmic contacts on GaAs are generally supposed to be Schottky barriers with very thin space charge layers due to the high dopant concentration. The current flowing through them obeys quantum mechanical tunneling [1] [2] [3]. It is obvious to assume that the doping atoms occupy randomly the lattice sites and therefore the shape of the potential in the space charge layer exhibits variations even in the case of uniform doping. The expected effect should be greater when the space charge width is in the range of the average distance of the doping atoms, i.e. in the case of higher doping concentrations. Therefore refinements of the picture take into account the potential variations in the space charge layer caused by the random distribution of the dopants [4] [5] [6]. In the present work we investigate this fluctuations by Monte-Carlo simulation. The results of the different theories and our computations are reviewed and compared with the last published measurements [7].

The plane of the junction was assumed to be equipotential and this boundary condition was introduced into the computations by the electrical image method. The electrostatic potential was computed in a prismatic volume in which the positively charged donors were randomly distributed in the points of a cubic lattice having a constant of GaAs (0.56 nm). The top surface of the prism is $0.5 \times 0.5 \mu\text{m}^2$ which is a macroscopic area. The space charge region is bounded by the equipotential surface belonging to $V=0$. The depletion approximation was used i.e. the charges of donors out of this boundary were not taken into account. For removing the edge effect the central prismatic region in which the computations were made was embedded in two successive regions: the first neighbouring one which has a width of the double of the average of depletion layer and the second one which extends to the infinity. The charges were distributed also randomly in the first region while in the second one a continuous space charge equal to the average of the doping was considered. The values of the electrostatic potential were computed in equidistant grid points in cross-sectional planes parallel to the junction.

In the case of moderate doping concentrations the average potential follows well the parabola known from the continuous space charge model, however the widths and forms of the elementary potential functions differ significantly. For higher doping (over 10^{19}cm^{-3}) even the average potential does not fit to the continuous model. The currents were computed along each elementary square according to the WKB approximation. Through the thinner depletion regions quasi-exponentially more tunnelling currents flow.

The following table shows the doping concentrations according to the different models (rows) fitted to the measured contact resistance values (columns):

experiment [7]		NiGeAu/n-GaAs($2 \cdot 10^{18} \text{ cm}^{-3}$)		PdGeTiPt/n-GaAs($2 \cdot 10^{18} \text{ cm}^{-3}$)	
metalisation and heat treatment		350°C /15s	390°C /90s	350°C /15s	390°C /90s
contact resistance (300K)		28.7 mWcm ²	0.66 mWcm ²	0.35 mWcm ²	8.2 mWcm ²
1	continuous model [4]	$1.6 \cdot 10^{18}$	$2.5 \cdot 10^{18}$	$3.0 \cdot 10^{18}$	$1.8 \cdot 10^{18}$
2	continuous model [3]	$1.5 \cdot 10^{18}$	$3.0 \cdot 10^{18}$	$3.2 \cdot 10^{18}$	$1.8 \cdot 10^{18}$
3	quasi-cont. model [2]	$2.3 \cdot 10^{18}$	$3.3 \cdot 10^{18}$	$3.8 \cdot 10^{18}$	$2.4 \cdot 10^{18}$
4	Monte-Carlo model [4]	$1.4 \cdot 10^{18}$	$2.0 \cdot 10^{18}$	$2.3 \cdot 10^{18}$	$1.6 \cdot 10^{18}$
5	Monte-Carlo model [5]	$2.0 \cdot 10^{18}$	$3.0 \cdot 10^{18}$	$3.5 \cdot 10^{18}$	$2.2 \cdot 10^{18}$

First column represents the case where the metal is not alloyed. The 1, 2 and 4 models result a lower doping concentration than the original one. These models seem to overestimate the tunneling current. The 3 and 5 models seem to be closer to reality. The second and third columns represent the experimental situation where the doping concentrations have been increased under the metalization by alloying or sintering. In these cases all models result in higher concentrations. It is difficult to judge them because there are no independent data of doping but it should be noted that the model 4 gives the original concentration only. The fourth column shows the compensation effect due to the amphoteric behaviour of Ge [7]. Here the models 1, 2 and 4 show again lower concentrations than the original one.

ACKNOWLEDGEMENT: This work have been supported by the Hungarian National Scientific Research Found (OTKA) under grants TO 15612, TO 22487 and by the EC under Copernicus 941180 contract.

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ACCURATE EQUIVALENT-NETWORK MODELING OF GaAs/AlAs BASED RESONANT TUNNELING DIODES WITH SYMMETRICAL THIN BARRIER AND SPACER LAYERS

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Abstract

Both the classical Esaki and the Quantum-Inductance equivalent-network models [1,2,3] are used in this work to describe the bias-voltage and microwave frequency dependency of the small-signal intrinsic impedance of our MBE grown GaAs/AlAs based Double Barrier Resonant Tunneling Diodes (DBRTDs). They have 5 nm quantum wells and symmetrical thin barrier and spacer layers, each nominally 2.5 nm thick (Fig.1). The devices under investigation are planar types (Fig. 2) with coplanar microwave probe access from the network analyser to the metallized SIG (signal) and GND (ground) pads on the Si-substrate. The DC I-V curve and the microwave reflection coefficient S11 of the extrinsic DBRTD, and S11 of the OPEN and SHORT reference structures are measured at the reference planes (pads) indicated. The SHORT and OPEN structures are used to determine the bias-voltage independent extrinsic elements of the equivalent circuits, Cex, Rex and Lex (Fig. 4a,b), describing the microwave behaviour of the Au interconnections. Only Rex is frequency dependent due to skin losses.

A prerequisite for accurate determination of the actual intrinsic elements Rd (dynamic resistance), Cd (dynamic device capacitance), Lqw (quantum inductance) and Rs (series resistance) is a stable, non-oscillating DBRTD in the negative differential resistance (NDR) region. A stable DBRTD has at least no plateaus in the NDR region of its I-V curve, so the conductance Gd (=1/Rd) has only one negative peak there (Fig. 6a,b). By a proper choice of the device area (36 μm^2 , /Rd+Rs+Rex/ > 50 Ohms at the largest S11, at 50 MHz) and a specially designed bias circuit, the stability condition was met in our experiments.

An S11 data array was collected in the 0 to +2V range of the I-V curve (mesa top = +), where S11 of the extrinsic DBRTD was measured at 75 bias points and from 0.05-40.05 GHz (401 points) after network analyser calibration with on-wafer standards. Fig. 3 shows some of these S11's in a compressed Smith chart, amongst them S11 of the steepest NDR bias-voltage point (largest negative Gd, /S11/ ~ 3.9). The prober-chuck temperature was 20.5°C.

Carefull optimisation of the equivalent-circuit S11 to match the measured S11 data at each bias point, leads to the conclusion that the 3-element Esaki model only fits the measured S11 data array in the NDR region sufficient accurate if (in contrast to the usual opinion in a number of papers) the dynamic conductance Gd and capacitance Cd are taken frequency as well as bias-voltage dependent (see Gd and Cd versus frequency at the steepest NDR point shown in Fig. 5).

The same measured small-signal S11 datasets can be described perfectly by the behaviour of the 4-elements Quantum-Inductance circuit model over the whole bias voltage (0-2 V) and frequency range (0.05-40.05 GHz) with only bias-voltage dependent elements (Fig. 6b-e). The measurement of S11 on the stable DBRTD throughout the whole NDR region results in the correct determination of the parameter τ , defined as $\tau = L_{qw}/R_d = L_{qw}/G_d$ indicating the carrier lifetime of the quasibound states in the quantum well. The display of this parameter continuously over the whole undistorted NDR is a novelty. Fig. 6f shows τ versus the bias voltage. The (small) voltage region immediately after the peak voltage and preceeding the valley voltage give less reliable values of τ due to inaccuracies in the (large negative) values of Lqw and Rd. τ is not defined where Gd=0. The peak value of τ (~22 ps) corresponds with the negative Gd peak (same bias-voltage) and when τ is compared with the calculated quasi-bound state lifetime given in [4] an AlAs barrier thickness of 8 monolayers (2.264 nm) is found as closest result.

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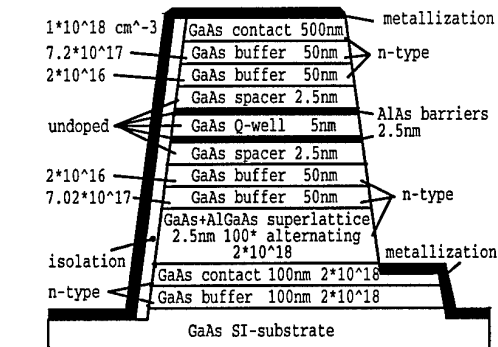


Fig. 1 MBE grown DBRTD layer structure

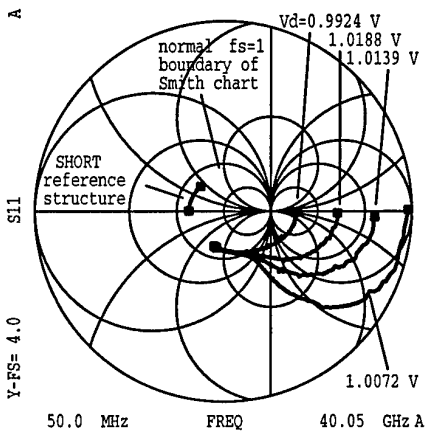


Fig. 3 S11 of SHORT ($Z_{int}=0$) and S11 of extrinsic DBRTD at several bias voltages V_d

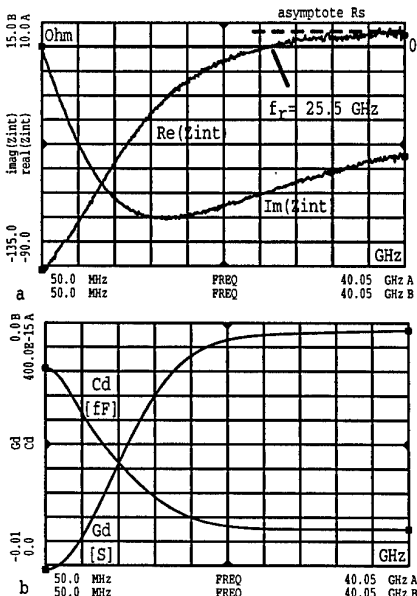


Fig. 5 In steepest point of the NDR region (1.0072 V): a) $\text{Re}(Z_{int})$ and $\text{Im}(Z_{int})$ b) G_d -f, C_d -f

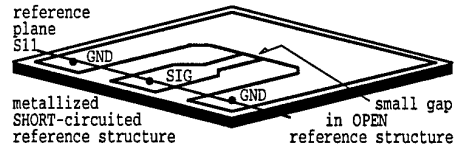
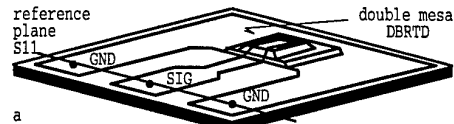


Fig. 2a Planar DBRTD with coplanar line
2b SHORT and OPEN reference structure

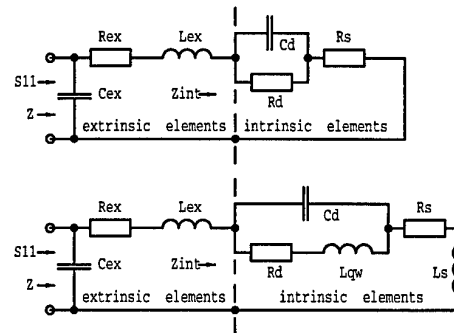


Fig. 4a Extrinsic elements and Esaki model
4b Extrinsic elements and Quantum-Inductance model $L_s \leq 1 \text{ pH}$

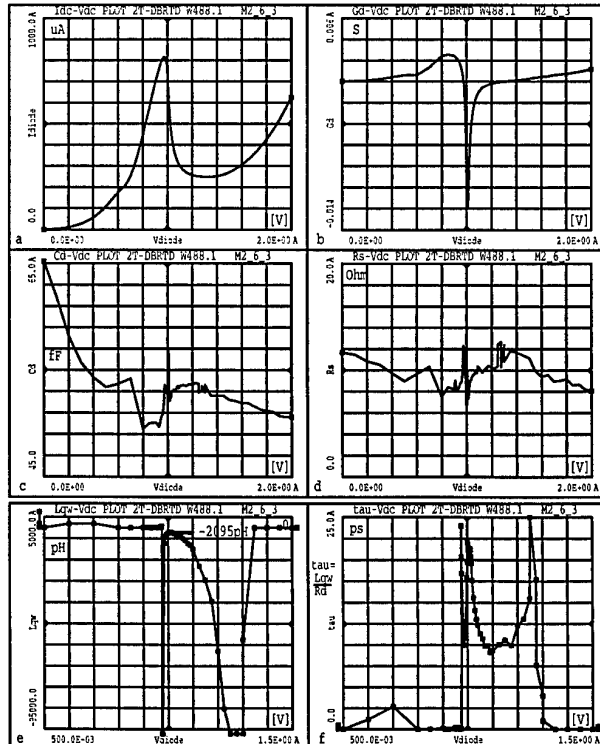


Fig. 6 a) measured DC I-V, b-e) dynamic G_d - V_d , C_d - V_d , R_s - V_d , L_{qw} - V_d and f) τ - V_d , $\tau=L_{qw}/R_d$

Tuesday, May 27

8.30 - 10.00 Session 5: Novel Techniques and Devices

08.30 1. (Invited Paper) *K. Ensslin, Swiss Federal Institute of Technology:*
"Ballistic electron transport in semiconductor nanostructures"

09.00 2. *Nils G. Weimann and Lester F. Eastman:*
"Effect of Threading Dislocations on the Electron Mobility in GaN
and its consequences for Vertical Devices".

3. *P. Gluche, A. Aleksov, A. Vescan, W. Ebert and E. Kohn:*
"A Technical Approach Towards Diamond Power Transistors".

4. *G. Höck, A. Gruhle, T. Hackbarth, E. Kohn and U. König:*
"High Current Si_{0.3}Ge_{0.7} p-Channel Hetero MOSFETs".

5. *D.A. Romanov, E.B. Gorokhov, V.A. Tkachenko, O.A. Tkachenko:*
"Insertion of slipping planes in quantum well with 2DEG for
creating one-dimensional barriers".

6. *F. Ejeckam, Yu-Hwa Lo, M. Seaford, L.F. Eastman:*
"Lattice Constant Engineering Using Compliant Universal (C.U.)
Substrates".

Experimental Observation of an Artificial Band Structure in Lateral Superlattices

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Abstract

Short period lateral superlattices are fabricated on AlGaAs/GaAs-Heterostructures by electron beam lithography. The samples are experimentally investigated by low temperature magneto transport experiments. For small values of the lateral potential modulation, the amplitude of the Shubnikov-de Haas oscillation is modulated, reflecting the oscillating band width of the Landau bands. For increasing values of the potential modulation the Landau band width increases, and the internal structure of the Landau bands is resolved. In particular, a splitting of the maxima of SdH oscillation is observed and attributed to the dominant energy bands and gaps within the Hofstadter butterfly energy spectrum. These experiments constitute the experimental observation of band structure effects, arising from an artificially imposed superlattice potential.

Introduction

The energy spectrum of Bloch electrons in a magnetic field has been calculated almost 20 years ago by Hofstadter [1]. This spectrum combines in a unique way the continuous spectrum of a periodic potential with a discrete spectrum arising from the magnetic quantization. Several attempts have been made to observe experimentally the theoretically predicted features. In a conventional 3-dimensional crystal lattice, huge magnetic fields are required in order to have one flux quantum penetrating a unit cell. In artificial superlattices, as they can be fabricated nowadays on semiconductor heterostructures, it is possible to have a small number of flux quanta per unit cell for experimentally available magnetic fields. The limitation in this case is the size of the lattice constants, usually much larger than the Fermi wave length of the electrons. Therefore, artificial lateral superlattices are usually dominated by classical phenomena. Nevertheless, a whole wealth of classical effects has been discovered recently in magneto transport experiments [2-5]. The dominant quantity in the classical regime is the cyclotron diameter at the Fermi energy. Pronounced magnetoresistance oscillations were observed, reflecting the commensurability of the cyclotron diameter with the lattice constant. In this paper we show, that for small period lateral superlattices a completely new regime can be tackled. In particular, we show that the miniband structure within a Landau band can be resolved in an experiment. The dominant energy bands and gaps within the Hofstadter energy spectrum lead to additional oscillations, as they can be observed in a transport experiment.

Modulation of Shubnikov-de Haas Oscillations

Electron beam lithography is the tool of choice nowadays for the fabrication of highly controlled lateral nanostructures on semiconductors. Figure 1 presents a square array of voids patterned into an electron beam sensitive resist layer on top of a semiconductor heterostructure. The period in this case is 105 nm,

which is about 2-3 times larger than the Fermi wave length of the electrons. A gate metal is evaporated on top of this patterned resist layer, leading to a laterally patterned gate electrode. Via the application of a voltage with respect to the two-dimensional electron gas (2DEG), a lateral potential modulation can be induced into the system. The smaller the lattice period, the more crucial becomes the distance of the 2DEG with respect to the sample surface. In our case, the 2DEG is located only 37 nm from the sample surface, thus allowing us to transfer this extremely small period lateral superlattice. The combination of high resolution lithography with this expertly grown 2DEG close to the sample surface, forms the basis for the observation of lateral band structure effects [6].

In Fig. 2a we present a typical experimental resistance trace as a function of magnetic field at a bath temperature of 30 mK. The fast oscillations are the usual Shubnikov-de Haas (SdH) oscillations, which are periodic as a function of $1/B$. It is obvious, that the amplitude of the SdH oscillations is additionally modulated.

This effect has first been observed in a pioneering work of Weiss et al. [2] and has thereafter been explained by Beenakker [3], Winkler et al. [4] and Gerhardts et al. [5]. The Landau levels, that form in a homogeneous 2DEG in the presence of a quantizing magnetic field widen into Landau bands, once a lateral potential modulation is imposed on the system [7]. A Landau level has no spatial dispersion which leads to the Landau degeneracy of Landau levels. In the case of a lateral superlattice, the Landau bands develop a spatial dispersion leading to the band width of a Landau band. As a function of magnetic field, this dispersion can strongly vary and in particular, it can vanish and therefore lead to zero band width at particular magnetic fields, where the classical cyclotron diameter is commensurate with the lattice period. These so-called flat band positions [7], where the Landau band dispersion vanishes are marked in Fig. 2a by the vertical dash lines. It is obvious, that at these magnetic field positions, the upper envelope of the SdH oscillations, as well as the lower envelope display minima. In-between, where the Landau bands do have a spatial dispersion, a group velocity can be defined that leads to an additional conductivity mechanism and therefore to the maxima in the resistance trace in-between the flat band conditions, as can be seen in Fig. 2a.

Figure 2b presents data on the same sample but for a negative gate voltage, that strongly increases the amplitude of the potential modulation. To first approximation the Landau band width is proportional to the amplitude of the potential modulation. As the potential modulation is increased, the internal structure of the Landau bands can be resolved at some energy level. The Landau band width is then no longer related to a spatial dispersion, but rather to a series of minibands within a Landau band. This means, that the above-mentioned band conductivity mechanism no longer exists. On the other hand, a different mechanism sets in, namely the scattering conductivity that reflects the density of states at the Fermi energy. This density of states of a Landau band is especially large, when the dispersion vanishes and therefore, the Landau band width becomes small.

In Fig. 2b we observe that the maximum of the modulation of the SdH oscillations now occurs at flat band again marked by the vertical dash lines. This is in contrast to the observation of Fig. 2a. We conclude, that the conductivity mechanism that gives rise to the modulation of the SdH oscillation has changed as the potential modulation is increased from Fig. 2a to Fig. 2b. For large values of the potential modulation, the internal structure of a Landau band becomes important even though no direct signature of these minibands is yet observed in Fig. 2b [see also Refs. 7 and 8]

For even more negative gate voltages (Fig. 3), a very extreme situation can be realized. The dash lines again show the position of flat band condition, where the amplitude of the SdH oscillations is maximum. In-between, at a magnetic field of roughly $B \sim 0.65$ T, the SdH oscillations are entirely quenched. This is related to the fact that neighboring Landau bands start to overlap for these large values of the potential modulation, and no Landau gap remains, giving rise to this quenching of the SdH oscillation. Having this picture in mind, we can extract a value for the potential modulation, which is of the order of 5% of the Fermi energy. Even though, this is still a relatively small value in energy (about 1 meV), it is larger than

the intrinsic collision broadening of single levels, which we estimate to be less than 0.5 meV for our particular sample. This estimation of the Landau band width and with it the potential modulation, is in agreement with estimations based on screening calculations. The experimental data presented so far, indicates that the subbands within Landau bands are resolved at some level even though they do not seem to show up directly in the transport experiments.

Internal structure of a Landau band

In order to resolve internal minibands and gaps within a Landau band one has to analyze very carefully SdH oscillations at large values of the potential modulation. Figure 4 presents a typical example where the resistance is plotted in a very small window of magnetic field. The dashed vertical line again marks flat band condition while the dash dotted line shows the magnetic field position where the band width of the Landau bands is maximum. Overall $1/B$ -periodic SdH oscillations are observed. At the maximum marked by the vertical arrow a splitting into 2 sub-maxima is observed. At this magnetic field 2.15 flux quanta penetrate a unit cell of the lattice. This is close to the theoretical prediction of Hofstadter [1] stating that for p/q flux quanta per unit cell a Landau band should split into p -subbands each of which is q -fold degenerate. The position where Φ / Φ_0 ($\Phi_0 = h/e$) exactly equals 2 is close to the dash dotted line where the Landau band width vanishes. Here it is very difficult to see internal splittings which is the reason why this splitting is then observed at a slightly higher magnetic field. At 2.15 flux quanta per unit cell the Hofstadter spectrum still roughly shows 2 dominant bands in the spectrum.

Figure 5 presents another resistance trace for a different gate voltage and in a different magnetic field regime, where a SdH maximum splits into 4 sub-maxima. Again, the window in resistance and magnetic field is very small where this particular splitting can be observed. Without showing the data we would like to mention that we observed similar splittings on this and on other samples for Φ / Φ_0 equal to 2, $2/3$, $3/4$, $3/2$ and $5/6$. The 2 examples as presented in Fig. 4 and Fig. 5 of this paper are meant to illustrate typical splittings as they can be observed in our samples. The experimental situation is much more involved than the calculated Hofstadter energy spectrum based on a single electron picture only considering the lowest Landau band. The coupling of Landau bands has been theoretically considered, and it was found that even though the energetic size of minibands and gaps can be modified the number of subbands is pretty much conserved. [9]

Electron-electron interactions can have various effects. Screening for example [10,11], can strongly change the effective potential modulation and with that the width of Landau bands. In order to observe the splittings within a Landau band the Fermi energy has to be positioned in this band at least in the case of a transport experiment. This is exactly the regime, where the density of states is high and therefore screening is strong. In other words, the observation of a Hofstadter subband splitting will be especially difficult in the quantum Hall regime, where the density of states within a Landau band is very high. This is one of the reasons we believe, why we can detect splittings of SdH maxima, just where SdH oscillations start to appear. Once the amplitude becomes 50% or more of the total resistance the modulation of the density of states at the Fermi energy and with that the effective band width of the Landau bands can be strongly modulated thus complicating the observation of subband splittings. Nevertheless, we conclude that the basic predictions of theory can be found in our experimental data.

Conclusions

Semiconductor technology has reached a mature state, where lateral nanostructures can be fabricated with feature sizes that are comparable to the Fermi wave length of the electrons. In this paper we have presented data that show splittings of SdH maxima, reflecting the creation of an artificial band structure. The challenge that lies ahead is the fabrication of even smaller lattice constants, which should enable us to observe higher order subband splittings at finite magnetic field or even a band structure at zero

magnetic field. Even though there is qualitative understanding of our experimental observations, a detailed theoretical calculation taking into account the experimental reality such as Landau band coupling and electron electron interaction is not available so far.

Acknowledgments

We thank Martin Holland from the University of Glasgow for his expert sample growth. The possibility to induce small lattice constants relies fundamentally on a 2DEG located close to the sample surface. It is a pleasure to thank Jörg Kotthaus for discussions and contributions to this project. We thank the Deutsche Forschungsgemeinschaft and the Schweizerischer Nationalfonds for financial support.

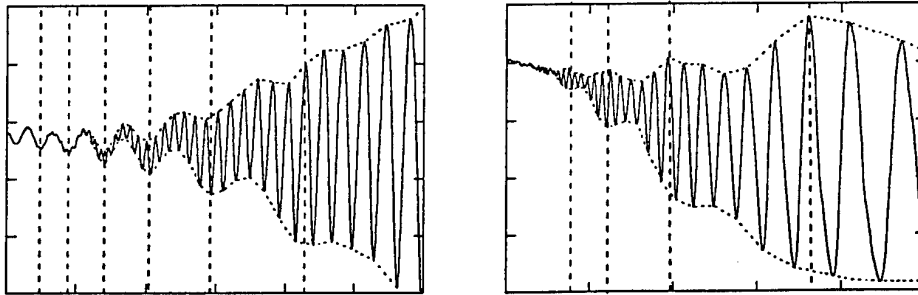
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Figure Captions

Fig. 1: AFM image of the patterned electron sensitive resist layer. The lattice period is 105nm.

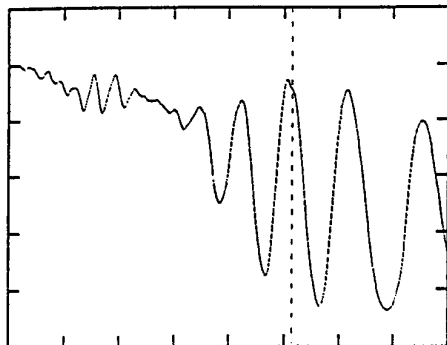
Fig. 2:



(a) Magnetoresistance trace of a two-dimensional lateral superlattice with period $a = 139$ nm in a low magnetic field regime for weak potential modulation. The vertical dashed lines indicate the magnetic field positions where the Landau bands are flat. The dashed lines connecting minima and maxima of the SdH oscillations are guides to the eye.

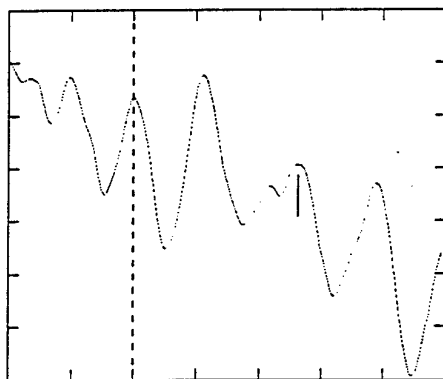
(b) Regime at larger potential modulation where the envelope of the SdH maxima and minima displays maxima and minima, respectively, at flat band.

Fig. 3:



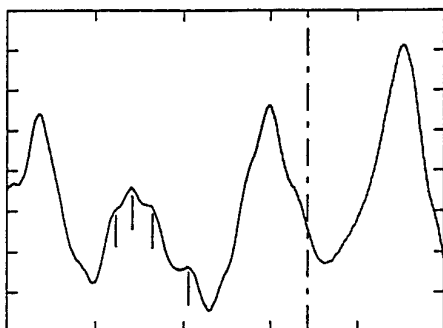
Magnetoresistance at very negative gate voltage and stronger potential modulation for $a = 139$ nm. At $B \approx 0.65$ T the Shubnikov-de Haas oscillations are entirely damped which allows us to estimate the Landau band width

Fig. 4



Magnetoresistance in a magnetic field regime for $a = 139$ nm where a maximum of the Shubnikov-de Haas oscillation splits into a doublet. The dashed line indicates flat bands, the dash-dotted line wide bands. The vertical arrows show numbers of flux quanta per unit cell as indicated. The thin vertical lines are guides to the eye and point to the observed sub-maxima.

Fig. 5



Same sample as in Fig. 4 for an even more negative gate voltage where a Shubnikov-de Haas maximum splits into four sub-maxima.

Effect of Threading Dislocations on the Electron Mobility in GaN and its consequences for Vertical Devices

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Student Paper

We propose a model that explains the observed low transverse electron mobilities in GaN by scattering of electrons at charged dislocation lines, and a microwave transistor device structure using vertical carrier transport to minimize scattering at dislocation lines. Epitaxial growth of GaN on sapphire and 4H-SiC results in a lattice mismatch of 16% and 3.5%, respectively. TEM investigations of hexagonal GaN films grown by MOCVD on sapphire have shown dislocations densities in the range of 10^{10} cm^{-2} .

Following the minimum energy approach developed by Read¹, the fraction of filled traps along edge dislocation lines in GaN approaches unity for doping densities of 10^{18} cm^{-3} . This transverse mobility component is calculated using Pödör's approach for scattering at a charged line² and combined with the mobility due to ionized-impurity scattering (Conwell-Weisskopf³) formula shows a maximum transverse mobility at a carrier density of 10^{18} cm^{-3} for a dislocation density of 10^{10} cm^{-2} . Experimental data⁴ follows the trend of our model. Vertical devices with current flow parallel to the dislocation lines are only affected by trapping of the free carriers, but not by scattering at charged dislocation lines.

The active region of the proposed vertical transistor (SIT, Static Induction Transistor) consists of a $3 \mu\text{m}$ thick layer of unintentionally n^- -doped epitaxial GaN on an n^+ -SiC substrate. The drain is contacted on the wafer backside, source and gate fingers are interdigitated on the epi surface. Current flow from drain to source is controlled by recessed Schottky gate contacts. The design goal is highly efficient operation at high frequencies. Device optimization is carried out using the 2D-device simulator ATLAS (Silvaco Inc.), theoretical unity gain occurs at 100 GHz for $.8 \mu\text{m}$ source finger width, $.5 \mu\text{m}$ gate length and $.4 \mu\text{m}$ source-gate spacing.

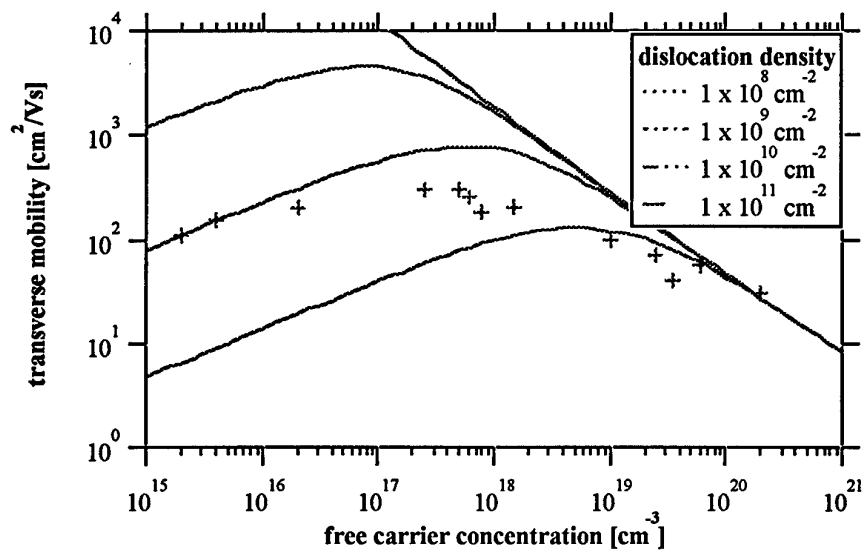
* email: weimann@ee.cornell.edu, phone: (607) 255-9609, fax: (607) 255-4742

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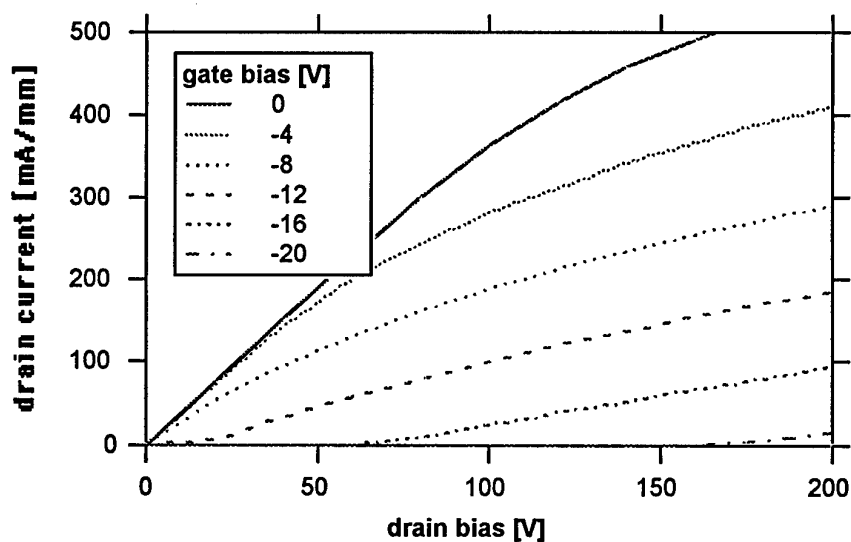
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³ E. M. Conwell, V. F. Weisskopf, Phys. Rev. 77, 388 (1950)

⁴ Prof. Moustakas, Boston U; private communication



Transverse mobility component in hexagonal GaN at $T = 300$ K due only to scattering at charged dislocation lines and ionized impurities vs. free carrier density.
Experimental data (+), samples grown by ECR-MBE⁴



simulated output curves of GaN SIT device with
 $0.8 \mu\text{m}$ source finger width, $5 \cdot 10^{16} \text{ cm}^{-3}$ background n -doping and
drain contact resistivity of $2 \cdot 10^{-3} \Omega\text{cm}^2$ (substrate backside)

A Technological Approach Towards Diamond Power Transistors

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Abstract

There are three wide gap materials considered for advanced power device concepts. These are SiC, GaN and diamond. Although SiC and GaN devices are well advanced, diamond has proven a very difficult material. No donor doping has yet been found and the only acceptor available (boron) shows an activation energy of 360mV and thus freeze out at R.T.. Based on ideal materials data a power handling capability above 20W/mm may be predicted for diamond FET devices; and even discarding n-channel devices due to the lack of a suitable donor, 10W/mm may be feasible for p-channel FETs [1]. However, extrapolation of state-of-the-art data only yield a maximum power density of 0.2W/mm, well below the 2.5 to 3.0W/mm obtained at microwave frequencies with SiC and GaN heterostructures. The main reason limiting the available power density is indeed the freeze out of the boron deep acceptor doping. Here a alternative approach is discussed, where the hole conduction of a hydrogen terminated surface is used as channel in a MESFET configuration [2]. This layer is activated at R.T. and contains approx. 10^{13}cm^{-2} sheet charge [3], which is in the order of that of device structures on SiC and GaN.

P-channel FET devices have been fabricated on synthetic Ib diamond substrates of 3x3mm surface area. These substrates are nitrogen doped and insulating. The active layer represents the surface of a 100 nm thick, nominally undoped buffer layer. It was grown by microwave plasma CVD in H_2 atmosphere containing 1.5% CH_4 , and was H-terminated after growth. The electrical properties of metal contacts on this surface are work function dependent and ohmic as well as Schottky barrier characteristics can be obtained [4]. In this case Au is used for the source and drain contacts and Al for the gate. In this configuration the FET is pinched off at zero gate bias and therefore enhancement mode.

In an FET device with 8.5 μm gate length and 500 μm gate width a maximum drain current of 22mA/mm is obtained in conjunction with a maximum source to drain bias of -196V, representing a gate to drain breakdown voltage of -203V. The breakdown was destructive and melted the metallization patterns, however, without effecting the diamond surface. Thus, it was concluded that the intrinsic breakdown condition was not yet reached. First microwave measurements on this device resulted in an $f_T=0.2\text{GHz}$ and an $f_{\text{max}}=0.5\text{GHz}$ at -15V drain bias. These first data were obtained at a low drain current of only 4.7mA/mm due to the fact, that a high source series resistance still dominates the transconductance at medium and high current levels. This can also be seen from the maximum forward gate bias, which can be as high as -6V, although the diode barrier height is only in the order of 0.9V [2].

At the gate length of 8.5 μm , the optimum load line will support an RF output power of 0.54W/mm. Scaling the device gate length down to 1 μm and assuming an undegraded drain breakdown voltage this is expected to result in an RF power density of approx. 6W/mm, which is approx. twice of that of SiC and GaN power FET structures.

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High Current Si_{0.3}Ge_{0.7} p-Channel Hetero MOSFETs

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1. Introduction

The introduction of SiGe bandgap engineering to Si technology made it possible to realize p-type hetero FETs. The enhanced hole mobility in compressive strained SiGe-channels (up to 700 cm²/Vs for Si_{0.3}Ge_{0.7} [1]) makes p-type HFETs favourable for CMOS applications [2]. In this talk we present a p-type hetero MOSFET with a Si_{0.3}Ge_{0.7}-channel on a Si_{0.7}Ge_{0.3} buffer.

2. Device Structure and Fabrication

Fig. 1 shows the structure of the p-channel HFET. The heterostructure was grown by molecular beam epitaxy (MBE) on an n⁻-Si Substrate. The layer sequence starts with a relaxed SiGe-buffer. The Germanium content was graded from 5% to 30%. The buffer layer is followed by the compressive strained Si_{0.3}Ge_{0.7}-Channel and the tensile strained Si-cap. A Boron doping spike was placed beneath the channel, in order to increase the sheet carrier density.

The gate oxide was fabricated by wet thermal oxidation of the Si-cap at 750°C. The thickness of the oxide was derived from C-V-measurements to 7 nm. To reduce the density of interface traps, the oxide was annealed at 450°C in H₂-ambient for 5 min.

The ohmic contacts were fabricated by a BF₂⁻-implant at 50 keV. To activate the implanted dopants, the sample was annealed at 650°C for 30 s.

Fig. 2 shows the band diagram of the heterostructure, calculated with a 1d drift diffusion simulator [3].

3. Results

Fig. 3 shows I_D - V_{DS}-Characteristics of the fabricated transistors with 1.3 μm gate length. They exhibit a maximum drain current density of 200 mA/mm at the transconductance maximum and up to 500 mA/mm at a gate bias of -6 V. This high currents are due to the increased sheet carrier density by the additional doping spike on the backside of the channel. Fig. 4 shows the transfer characteristics of the fabricated devices. The maximum transconductance is 90 mS/mm at a gate bias of -1.5 V and a drain to source voltage of -3 V.

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Insertion of slipping planes in quantum well with 2DEG for creating one-dimensional δ -barriers

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Insertion of crystallographically perfect one-dimensional obstructions on the way of two-dimensional electrons of the buried quantum well by means of slipping planes is suggested. Positions of the (111) family slipping planes are determined by Franck-Read sources which are set in action by compressing the GaAs/AlGaAs heterostructure in a lateral direction at heating above 400°C [1,2]. The shift of the crystal lattice along the slipping planes by several monolayers result in formation of terraces on each heteroboundary, including the surface (Fig. 1). In the quantum well the adjacent terraces are separated by asymmetric oblique-shift narrowings which can reflect the electrons. Electron transparency of the systems of such obstacles has been calculated by S -matrix method [3] taking into account the excitation of additional transverse modes at the locations of narrowings. It was found that the obstacles can, with good precision, be considered as one-dimensional δ -barriers with magnitude proportional to the square of the shift height h , *i.e.* the transmission coefficient $T \approx k_y^2/(k_y^2 + G^2/4)$, where effective magnitude of the δ -barrier $G \propto h^2$.

Multiple electron reflections from such barriers should lead to 2DEG mobility anisotropy in the plane of the quantum well (x, y). Applying transverse magnetic field allows of further increased anisotropy provided that $kT/\hbar\omega_c \ll 1$, because the motion becomes finite along y -direction within magnetic length while remaining free along x -axis. The electron wave function is chosen in the form $\Psi(x, y) = \psi(y) \exp(ik_x x)$. Then $\psi(y)$ is obtained from the one-dimensional Schrödinger equation

$$-\frac{\hbar^2}{2m} \frac{\partial^2 \psi}{\partial y^2} + \left[U(y) + \frac{m\omega_c^2}{2} (y + k_x l_B^2)^2 \right] \psi = E\psi,$$

where $\omega_c = eB/mc$ is the cyclotron frequency, $l_B = \sqrt{\hbar c/|eB|}$ the magnetic length, and $U(y) = \sum_i G_i \delta(y - y_i)$. The energy levels E_n vs. longitudinal momentum, *i.e.* vs. position of the magnetic parabola minimum $y_B = -k_x l_B^2$, were calculated, and oscillations in $E_n(p_x)$, or $E_n(y_B)$, were found. According to perturbation theory these oscillations (magnetic valleys) are the direct exposure of total probability density at the locations of δ -barriers y_i : $E_n(p_x) - E_{n,2DEG} = \sum_i G_i |\Psi_n(y_i)|^2$. Thus, when the slipping plane spacing is much greater than magnetic length the response in $E_n(p_x)$ does not mix with those from other δ -barriers and has remarkably simple form of squared Hermitian polynomial with index n (Fig. 2). So obtained deviations in dispersion law $E_n(p_x)$ from Landau levels of uniform 2DEG are proportional to the magnitude of δ -barriers and sufficiently large to be measurable.

The deviations should exhibit in asymmetric broadening of cyclotron resonance line towards lower photon energy. Moreover, increased density of states at the extrema of $E_n(p_x)$ should lead to the magnetoresistance oscillations vs. magnetic field additional to SdH-oscillations [4]. By comparing magnetooptical and magnetotransport measurements with AFM images of the surface, *i.e.* with the values of shift-narrowings in the quantum well, one could verify our suggestion about the possibility of making and using one-dimensional δ -barriers in uniform 2DEG.

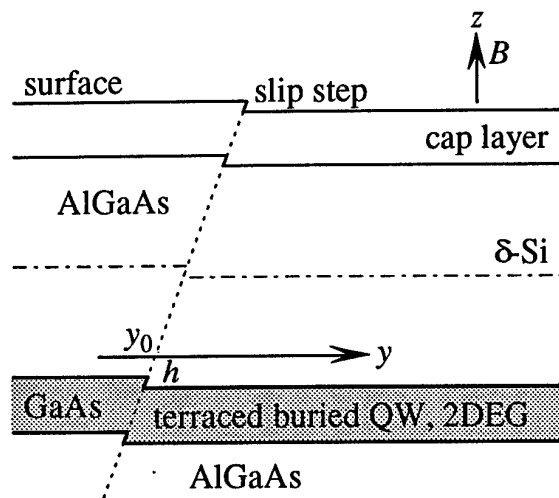


Figure 1. Schematic view: shift of the material of a heterostructure along (111) slip plane.

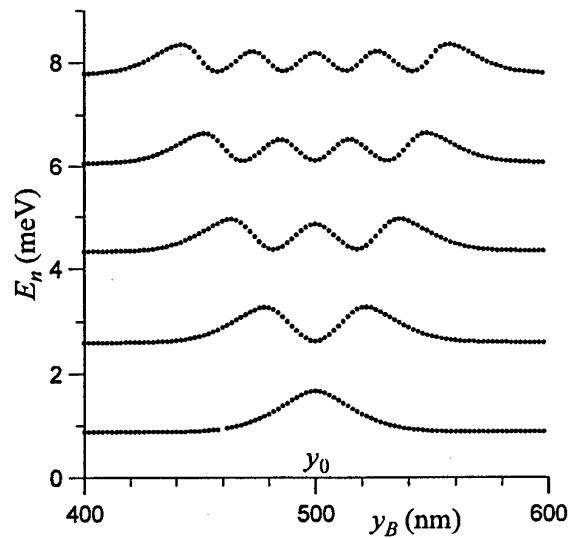


Figure 2. Dispersion law response to the single slip plane located at y_0 . Magnetic field $B = 1$ T, the thickness of GaAs quantum well 10.2 nm, slip step height $h = 2.83$ nm.

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Lattice Constant Engineering Using Compliant Universal (C.U.) Substrates

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Ultra thin (30-100Å) GaAs epitaxial layers, on etch-step layers, are twist-bonded to another GaAs substrate, at 550°C, 100 ATM pressure for 30 minutes. The substrate and the etch-step layer are both removed by selective etches after the bonding. A regular array of screw dislocations is formed at the twist-bond interface, allowing movement. Growth of .30 µm InSb (15% larger lattice constant) on the thin, GaAs Compliant Universal (C.U.) substrate yielded excellent morphology, and TEM revealed no threading dislocations. In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As MODFET's and 1.3 µm and 1.5 µm lasers normally grown at the InP or other lattice constant can now be grown on this GaAs C.U. substrate.

Research is underway to initiate Si C.U. substrates. The C.U. substrate will allow an order of magnitude more opportunities for materials combinations for future devices.

Tuesday, May 27

10.30 - 12.30 Session 6: Field Effect Transistors and Diodes

- 10.30 1. (Invited Paper) *T. Enoki, NTT System Electronics Labs.:*
"HEMT ICs for ultra high speed optical communication systems"
2. *Helmut Brech, Thomas Simlinger, Thomas Grave and Siegfried Selberherr:*
"Influence of Gate length on the DC-Characteristics and f_T of Pseudomorphic Power-HEMTs".
3. *R. Fauquembergue, P. Desplanques, F. Dessenne and D. Cichoka:*
"Monte Carlo Simulation of III-V Nitrides FET's".
4. *F. Fumi, M. Peroni, C. Lanzieri, A. Cetronia, A. Gasparotto:*
"Optimization of multifunction self-aligned-gate (MSAG) GaAs MESFET".
5. *D. Théron, S. Piotrowicz, X. Wallart, F. Diette, B. Bonte and Y. Crosnier:*
"InP based HEMT structures with a large bandgap barrier layer for power application in V band".
6. *Ferdouse Khaleque:*
"Room temperature InSb MISFETs".
7. *K. Lübke, T. Hilgarth, Ch. Diskus, A. Stelzer, A. Springer, H.W. Thim:*
"Zero-bias Detection with $\text{In}_{0.38}\text{Ga}_{0.62}\text{As}$ Schottky Barrier Diodes".
8. *X. Mélique, E. Lheurette, P. Mounaix, F. Mollot, O. Vanbésien, D. Lippens:*
"InP-based Heterostructure Barrier Varactor".

InP-based HEMT ICs for Ultrahigh-Speed Optical Communication Systems

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INTRODUCTION

Recently developments in optical communications technology already enable the commercial use of 10-Gbit/s systems [1]. Experimental development of the next generation of cost-effective TDM and WDM optical fiber networks has started [2, 3]. It is very important and urgent for device researchers to clarify and demonstrate how fast electronic circuits can operate.

InP-based HEMTs have achieved record current gain cutoff frequency (f_T), transconductance (g_m) [4], and maximum oscillation frequency (f_{max}) [5] and are considered to be the fastest devices in practical use. An f_T and f_{max} of over 300 GHz and a g_m over 1000 mS/mm will be available in integrated circuits. We have previously demonstrated a baseband amplifiers with a gain-bandwidth product of 297 GHz [6] and high yield, low noise amplifiers with a noise figure of 2.8 dB at 50 GHz using 0.1- μ m-gate InAlAs/InGaAs HEMTs [7]. In addition to demonstrating the feasibility of the device for MMICs, we have successfully expanded the applicable field of the device to high-speed digital ICs by introducing an InP recess-etch stopper [8].

In this paper device design for ultrahigh-speed digital ICs and fabrication technologies are discussed, and the key ICs and modules for 40-Gbit/s optical transmission systems are summarized.

DEVICE DESIGN

The empirical relationship between the maximum bit

rate of T-FF and the f_T of the used FETs tells us that f_T of over 160 GHz will be needed to make 40 Gbit/s ICs. To clarify the details of the device parameters, a gate delay time (τ_{pd}) of an inverter was calculated for various f_T and g_m using an analytical expression for the τ_{pd} of the SCFL (Source Coupled FET Logic) [9], as shown in Fig. 1. Realistic parameters, which were extracted from our fabricated FETs and are shown in Table I, are assumed in the calculation. The gate capacitance is derived using f_T , g_m , and other parasitic. It can be reasonably considered that the increase in g_m corresponds to the vertical scaling (thinning a barrier thickness, d) and that the increase in f_T corresponds to the lateral scaling (shortening a gate length, L_g).

Figure 1 clearly shows that it is important to balance g_m with f_T for high speed operation in the most effective

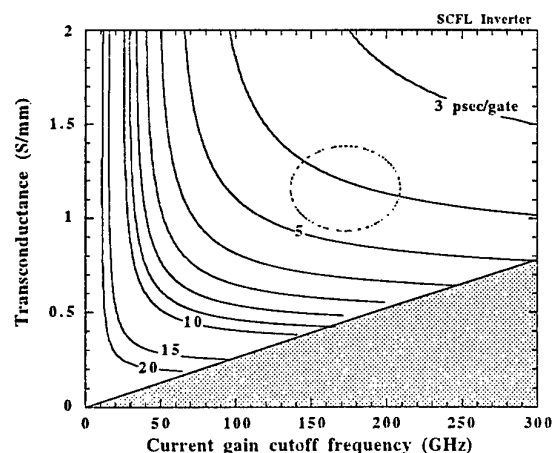


Figure 1. Gate delay of an SCFL inverter for various transconductances and current gain cutoff frequencies.

way. Shortening the gate length without making the channel shallower or making the channel shallower without shortening the gate length respectively require extremely high f_T or g_m .

In addition to the intrinsic gate delay, the transmission delay in the interconnection line can not be neglected in circuits. The transmission delay was measured to be 8 psec/mm [10]. From the inverter cell size, transmission delay of about 1 ps should be taken into account. Thus, for over-40-Gbit/s ICs, the intrinsic τ_{pd} should be about 4 ps/gate. A g_m of 1 to 1.4 S/mm and an f_T of 150 to 200 GHz are the balanced performance for the applications.

Figure 2 shows the calculated transconductance for various gate lengths and barrier thicknesses using the two-region model which assumes a mobility of 10000 $\text{cm}^2/\text{V}\cdot\text{s}$ and a saturation velocity of 2.7×10^7 cm/s. Figure 3

Table I. Parameters for the calculation in Fig. 1.

Inverter gain	2	C_{ds}	14 fF/mm
Gate width	20 μm	R_g	0.7 Ω
g_m/g_d	20	R_s	0.16 $\Omega\cdot\text{mm}$
C_{gd}	252 fF/mm	R_d	0.24 $\Omega\cdot\text{mm}$
C_p	2.5 fF	R_{LS}	7.5 Ω

C_p : Electrode parasitic capacitance, R_{LS} : Turn-on resistance of level-shift diode

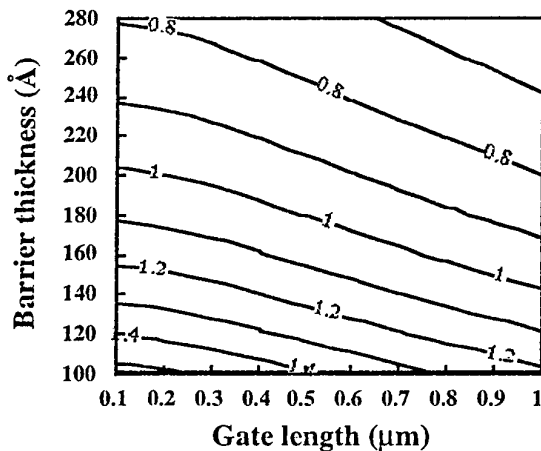


Figure 2. Calculated transconductance for various gate lengths and barrier thicknesses. A mobility of 10000 $\text{cm}^2/\text{V}\cdot\text{s}$, a saturation velocity of 2.7×10^7 cm/s, and a source resistance of 0.16 $\Omega\cdot\text{mm}$ were assumed.

summarizes the dependence of f_T on L_g . The balanced performance is achievable by using InAlAs/InGaAs HEMTs with a gate length of 0.15 to 0.1 μm and a barrier thickness of 200 to 120 Å. An optimum channel-aspect ratio (L_g/d) is about 8 for the applications. No other FETs can guarantee the performance at the moment.

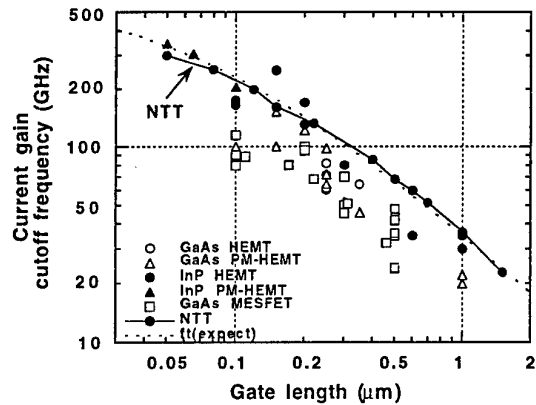


Figure 3. Dependence of current gain cutoff frequency on gate length.

DEVICE STRUCTURES AND FABRICATION TECHNOLOGY

Figure 4 shows a schematic crosssection of the completed device. The epitaxial layers were grown by MOCVD. An InP recess-etch stopper with a thickness of 50 Å was inserted in the InAlAs barrier and resulted in the drastic improvement in controllability of the threshold voltage (V_{th}) and the barrier thickness. The stopper also enlarges the process margin for the gate recess [8]. This stopper technology is the key for applying the HEMTs in digital ICs. Based on the discussion above, the barrier thickness including the InP recess-etch stopper was designed to be 140 Å. The V_{th} standard deviation of below 50 mV is obtainable with high reproducibility using a conventional wet-etching technique. The measured electron mobility of the wafers described in this paper is 6500 to 7500 $\text{cm}^2/\text{V}\cdot\text{s}$.

In addition to FETs, a level-shift diode is also needed in digital ICs. Especially in series gate configuration which is generally used in functional ICs, the level-shift diode is indispensable. To reduce the interconnection length and

CR-delay time composed of turn-on resistance of the level-shift diode and the gate capacitance of the next stage, a small diode with a low turn-on resistance is necessary. For this purpose, InGaAs-pn layers [11] or InAlAs-Schottky layers were grown on the HEMT layers with an n^+ -InP etch stopper as shown Fig. 4.

The fabrication process for ICs is as follows. The anode electrode of the diode consists of WSiN/Ti/Pt/Au was made in the alignment-mark level, and InAlAs layers were etched using the electrode as a mask. The n^+ -InP layer in Fig. 4 serves as an etching stopper. After mesa isolation, an ohmic electrode consisting of Ti/Pt/Au was lifted off. For high reproducibility and uniformity of the gate, we used an EB direct writer with a thin EB resist to delineate the footprint of the gate and replicated it on the SiO_2/SiN films by using RIE. The aspect ratio of the opening was reduced by making the side-etch in the top SiN layer during the RIE in order to completely fill the groove with the gate metal [12]. After removing the resist, the gate recess etching was carried out. Then, as a Schottky gate metal which is stable with InP, WSiN was deposited using a reactive sputter [13]. The gate electrode consisting of Ti/Pt/Au was lifted off and WSiN was etched using the gate electrode as a mask. An SEM cross-sectional view is shown in Fig. 5.

The InP recess-etch stopper enable us to independently control the lateral etching during the gate recess from the

vertical etching depth because the etching selectivity between InP and InAlAs exceeds 400. Optimization to ensure the breakdown voltage has been carried out as shown in Fig. 6. In the figure, the gate-recess etching time is normalized by the vertical etching time for the layers on the InP recess-etch stopper. Although g_m decreases by increasing the over-etching time, BV_{ds} drastically increases and C_{gd} decreases. Over-etching by a factor of 3.5 makes 150-nm-lateral etching of the gate recess which results in

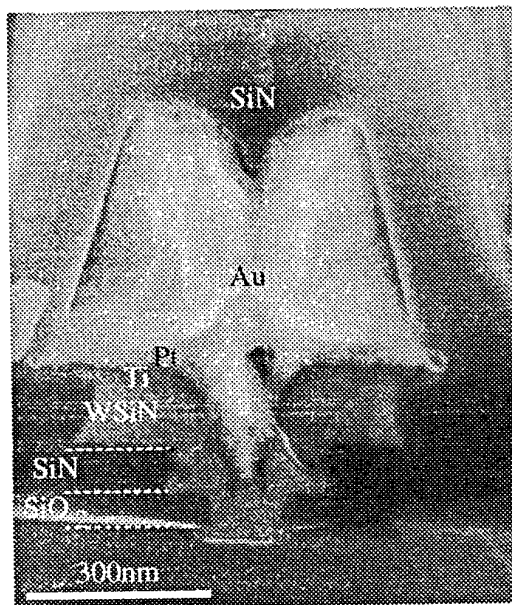


Figure 5. SEM cross-sectional view of 0.1- μm -T gate.

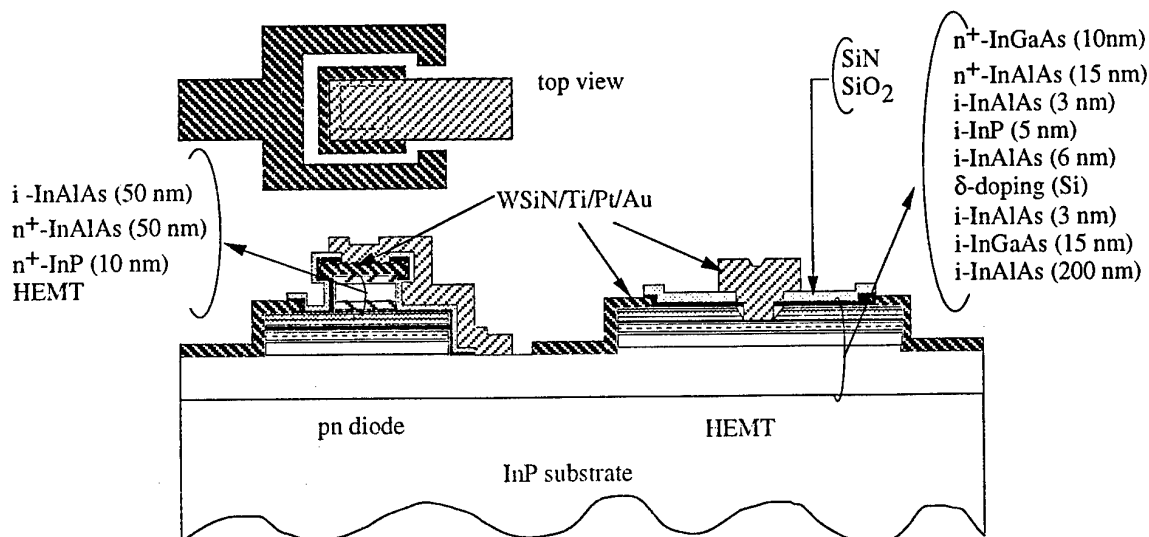


Figure 4. Structure of InAlAs/InGaAs HEMT and InAlAs-Schottky diode.

BV_{ds} of as high as 6 V and a reduction of C_{gd} by a factor of 2. This optimization is important for the practical use.

First-level and cross-over interconnection lines were made by a lift-off and an electro-plating methods, respectively. MIM capacitors were made with a SiN film

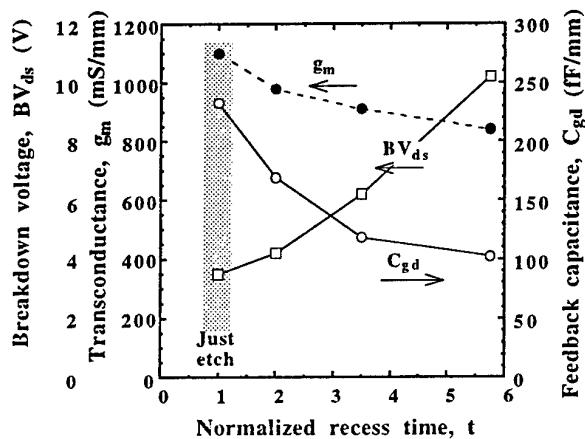


Figure 6. Dependence of device characteristics on the gate recess-etching time.

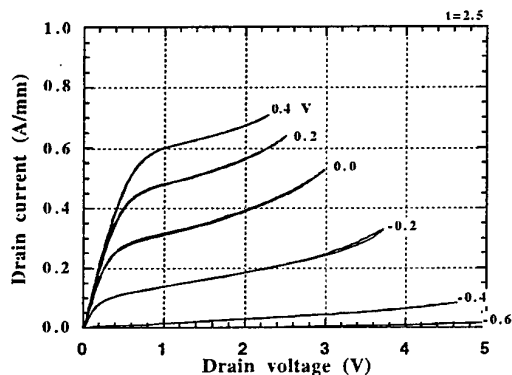


Figure 7. Typical I-V characteristics of 0.1-μm-gate InAlAs/InGaAs HEMT.

Table II. Performance of 0.1-μm-gate InAlAs/InGaAs HEMTs on a 2-inch wafer. (N=32)

	Average	Standard deviation
V_{th} (mV)	-419	32
g_m (S/mm)	0.95	0.032
f_T (GHz)	174	7.2
f_{max} (GHz)	523*	43*

* Accuracy of the values was poor due to large scattering of Mason's unilateral gain.

and resistors were made with the HEMT layers.

DEVICE PERFORMANCE AND DIGITAL CIRCUIT APPLICATION

Figure 7 shows typical I-V characteristics of the 0.1-μm-gate HEMTs described above. The normalized etching time in the gate-recess etching is about 3.5. Table II summarizes characteristics of the 0.1-μm-gate HEMTs on a 2-inch wafer. The f_T and f_{max} in Table II were estimated by extrapolating the current gain and the Mason's unilateral gain in the frequency range of 10 to 30 GHz to the unity gain with 6 dB/oct. Although reliable values for f_{max} were not able to be obtained because of the small feedback capacitance, the equivalent circuit analysis confirmed that the f_{max} of the device derived from the maximum available gain was also close to 500 GHz as shown in Fig. 8.

Static frequency dividers consisting of SCFL have been fabricated as test circuits for the feasibility study. A 40.4-GHz operation was demonstrated using the devices with f_T of 195 GHz and g_m of 1.2 S/mm [11]. It was also clarified that the transmission delay dominates about 25 % of the total delay in the circuits. Maximum toggle frequency using the device described above was also 35.3 ± 2.0 GHz with a yield of 75% on a 2-inch wafer. To boost the operation frequency, the interconnection length of the critical path in the circuit should be minimized using 2nd-

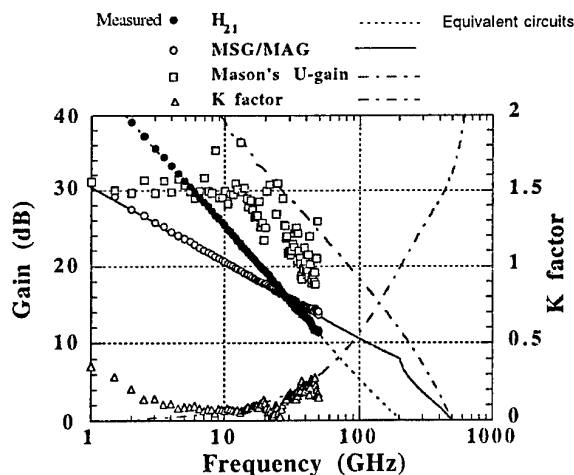


Figure 8. Frequency dependence of current gain, power gains, and stability factor.

level interconnection technology in addition to shorten the gate length.

IC SETS AND MODULES FOR 40-Gbit/s TRANSMISSION EXPERIMENTS

Table III summarizes IC sets using our InAlAs/InGaAs HEMTs for 40 Gbit/s optical transmission experiments. To boost the operation bit rate of ICs and modules as high as possible, the following novel circuit technologies was used.

- (1) Distributed-circuit design techniques [7,14,15].
- (2) High-speed Latching Operation Flip-Flop circuit [16]
- (3) Super-Dynamic Flip-Flop circuit [17].
- (4) Wideband data and clock buffer using peaking and feedback techniques [18]
- (5) Chip-size cavity package with 6-RF ports [19]

The highest operation bit rate of 64 and over 40 Gbit/s for multiplexers (MUX) and demultiplexers (DEMUX) were measured on wafer. Error-free operations up to the maximum bit rates were confirmed. The packaged IC modules for the MUX and DEMUX also operated at beyond 40 Gbit/s. A microphotograph of the 2:1 MUX and the module are shown in Fig. 9 and 10.

Electrically multiplexed and demultiplexed 40 Gbit/s,

Table III Summary of ICs and modules for optical transmission experiments using InAlAs/InGaAs HEMTs.

Circuit	Bandwidth/ Bit rate	Gain (dB)	Output	Power (W)
2:1 MUX ^[18]	1-64 Gbit/s (1-52 Gbit/s)*	---	0.92V _{pp}	2.2
Preamp. ^[14]	DC-32 GHz	9	1.0V _{pp}	0.44
Baseband amp. ^[7]	DC-47 GHz	16	1.2V _{pp}	1.1
Signal distributor ^[15]	DC-100 GHz	-2.5	0.5V _{pp}	1.1
Decision ^[18]	15->40 Gbit/s (15-46 Gbit/s)*	---	0.94V _{pp}	1.7
1:2 DEMUX ^[18]	2-40 Gbit/s (2-40 Gbit/s)*	---	0.94V _{pp}	3.8
Frequency Divider ^[11]	DC-40.4 GHz	---	0.4V _{pp}	0.55
Frequency Divider ^[18]	2-46 GHz	---	0.4V _{pp}	1.1
Limiting amp. ^[14]	34-40 GHz	17	10dBm	0.070

*:Performance of packaged IC modules

300-km transmission has been successfully demonstrated using the IC modules described above [18, 20]. The block diagram of the experiment is shown in Fig. 11. Details on photonic devices and fiber technologies will be presented in ref. 18 and 20. Four-channel 10-Gbit/s PRBS (2^7-1) signals from a PPG were multiplexed to 20 Gbit/s using two GaAs MESFET MUXs to get input signals in Fig. 11. The MUX and DEMUX modules using InP-based HEMTs are used for the front ends of the transmitter and the receiver. Forty-Gbit/s eye patterns at nodes denoted by A-to-D are shown in Fig. 12. Clear eye opening of the MUX and successful regeneration of signals by the MUX after 300-km transmission were achieved. The 20-Gbit/s output signal was demultiplexed by a Si-bipolar decision circuits and the bit error rate (BER) performance of the four 10-Gbit/s channels in the 40-Gbit/s data stream was measured. The average receiver sensitivities at the BER of 10^{-9} before and after transmission were respectively -24.8 ± 0.2 dBm and -24.3 ± 0.6 dBm.

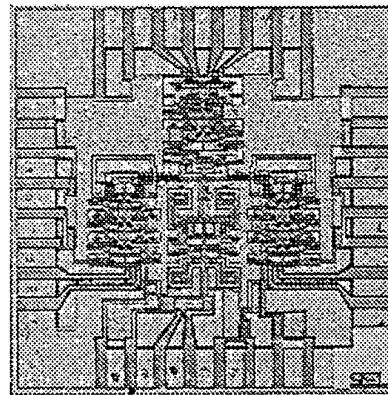


Fig. 9. Microphotograph of 2:1 multiplexer which operates up to 64 Gbit/s.

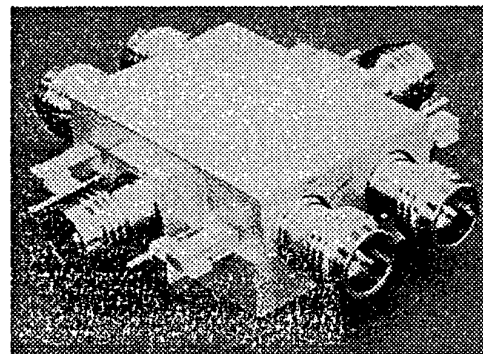


Fig. 10. Chip-size cavity module with 6 RF-ports.

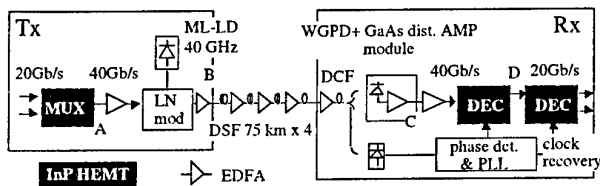


Figure 11. Experimental setup for a 40-Gbit/s, 300 km optical repeater.

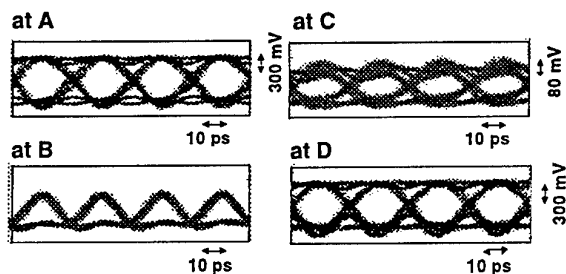


Figure 12. Eye patterns at A-to-D nodes in Fig. 11.

CONCLUSIONS

A 0.1- μm -gate InAlAs/InGaAs HEMT with an f_T of over 160 GHz and a g_m of over 1 S/mm is now available for application in circuits. An InP recess-etch stopper improved the uniformity of threshold voltage and enabled us to apply the HEMTs in digital ICs. Novel circuit technologies make the most of the high-speed performance of the devices and boost the operating speed of ICs. As a benchmark for future large-capacity networks, electrically multiplexed and demultiplexed 40 Gbit/s, 300-km transmission was successfully demonstrated using the device technologies described in this paper.

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Influence of Gatelength on the DC-Characteristics and f_T of Pseudomorphic Power-HEMTs

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Abstract -Measurements and simulations of two pseudomorphic HEMTs designed for power applications are presented. The HEMTs are fabricated on the same wafer and do only differ in their gate lengths of 220 nm and 500 nm. Mixed hydrodynamic/drift-diffusion simulations are performed with a single consistent set of parameters. The important parameters g_m , g_{out} and f_T compare very well with the measured data. Therefore we are able to make accurate predictions of important circuit design parameters for a wide range of gate lengths relevant for modern GaAs MMICs.

I. INTRODUCTION

Low cost, high performance power MMICs are required for many commercial system applications. Most of them are very cost driven with superior high frequency power capabilities in combination with high yield. Especially the reduction of gate length is a sensitive parameter of production cost which has to be balanced with the needed device performance. Rising the current gain cut-off frequency f_T also trades off with high output conductance. Accurate device simulation can be a substantial aid for the optimum device design for given requirements. But prerequisite is that the simulation is able to describe the device characteristics with a consistent set of parameters, i.e., not fitting the simulation to different devices individually. In this paper we present measurements and simulations with such a parameter set of two pseudomorphic HEMTs with gate length of 220 nm and 500 nm fabricated on the same wafer which compare very well.

II. SIMULATIONS AND MEASUREMENTS

In Fig. 1 the schematic cross section of the investigated HEMTs is shown. To simulate the influence of the gate length on the transport characteristics of the HEMT a hydrodynamic model is used in the channel and the upper barrier layer between gate and channel. Moreover source and drain contacts have to be on top of the cap layer only, i. e., not contacting the channel directly [1].

First the simulation of the HEMT with 220 nm was matched to the measurements by fitting parameters such as the effective distance from gate to channel d_{gch} , the active doping, the interface charge density between passivation and semiconductor, the low field mobility μ_0 and the saturation velocity v_{sat} . All parameters are found well within realistic ranges. In Fig. 2 simulations and measurements of the transfer characteristics of the two HEMTs are shown. Even though the parameters are fitted for the device with $l_g=220$ nm only, also the HEMT with $l_g=500$ nm is simulated very precisely. Also the measured and simulated transconductance g_m shown in Fig 3 compare very well. Both measurements and simulations show that V_T and $g_{m\max}$ is shifted about 100 mV and $g_{m\max}$ is raised about 50 mS/mm by reducing l_g from 220 nm to 500 nm. The maximum in g_m is reached at the same drain current.

$C_{GS}+C_{GD}$ can be determined from simulations using the quasi static approximation

$$C_{GS} + C_{GD} = \left. \frac{\partial Q_G(V_{GS})}{\partial V_{GS}} \right|_{V_{DS}=const} \quad (1)$$

Below pinch off both transistors show the same capacitance. In the active region they differ due to the difference in their gate contact area. Using the approximation

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$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \quad (2)$$

f_T can be calculated. Fig. 4 shows the calculated $f_{T \max}$ versus I_g and g_{out} at the bias point of $f_{T \max}$ along with the measured data. It is shown that the simulated data are slightly higher than the measured ones. This is mainly due to a coplanar structure in which the HEMTs are embedded for RF measurements. The simulated f_T as well as g_{out} coincide very well with the measured data.

III. CONCLUSION

Measurements and simulations of two HEMTs which differ only in their gate length are presented. The simulated data obtained with one consistent set of parameters compare very well with the measurements. Also the calculated f_T shows the gate length dependence of the f_T very precisely. Therefore we are able to predict major device parameters important for circuit design with very high accuracy.

IV. REFERENCE

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V. FIGURES

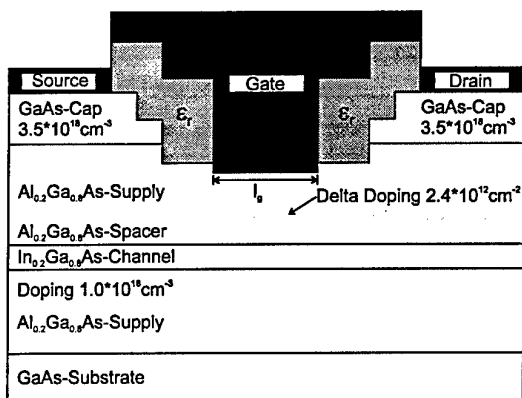


Fig.1 Schematic cross section of the simulated HEMTs

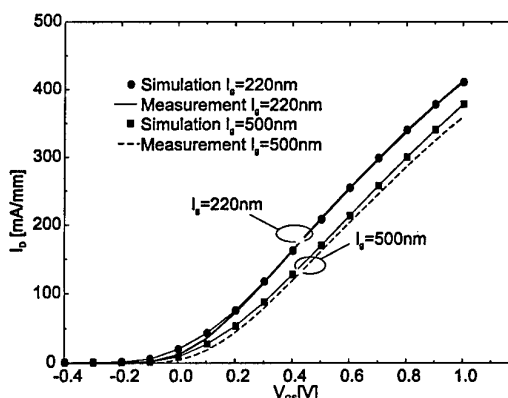


Fig.2 Measured and simulated transfer characteristics of the two HEMTs

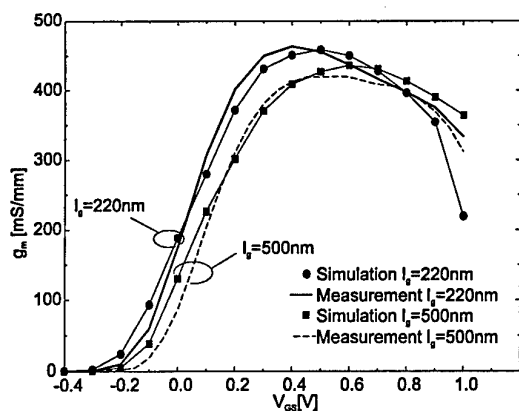


Fig.3 Measured and simulated transconductance of the two HEMTs

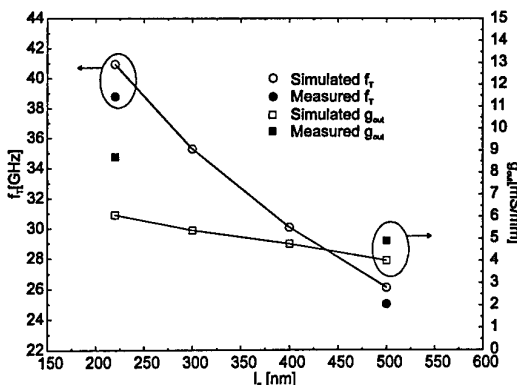


Fig.4 Measured and simulated f_T and g_{out}

MONTE CARLO SIMULATION OF III-V NITRIDES FET's

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III-V Nitrides have recently attracted considerable attention for their application in short wavelength optoelectronic devices. They are also very appealing because their thermal stability, their high breakdown voltages due to a wide band gap and their high electron velocities make these materials suitable for high power and high temperature electronic devices. When grown on Sapphire or SiC substrates, III-V nitrides crystallize in the Wurtzite (hexagonal) phase, whereas on Si or GaAs substrate, the Zinc-Blende (cubic) phase is obtained and exhibits better electronic transport properties than the Wurtzite one [1]. Recently, microwave Heterojunction Field Effect Transistors (HFET's) on III-V Nitrides in the Wurtzite form have been demonstrated, exhibiting interesting performance in terms of current densities, transconductances, current cut-off frequencies...[2]

In this paper, we report on the theoretical comparison of Wurtzite and Zinc-Blende III-V Nitride. We first determine the bulk transport properties of GaN and GaAlN and found, as already reported [1], that Cubic-GaN presents better electronic transport properties than Hexagonal GaN. Then, using a 2D Monte Carlo device simulation, we investigate the capabilities of GaN MESFET and $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$ HFET with very short gate length ($0.12\mu\text{m}$). A comparison of typical results is presented on figure 1 for GaN MESFET's, showing that the cubic-form exhibits higher transconductance and cut-off frequency values than the wurtzite one. Moreover, the cubic $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$ HFET structure exhibits transconductance as high as 480 mS/mm , cut-off frequency of 180GHz and current densities in excess of 900mA/mm , demonstrating that III-V Nitrides are very good candidates for high power, high frequency applications.

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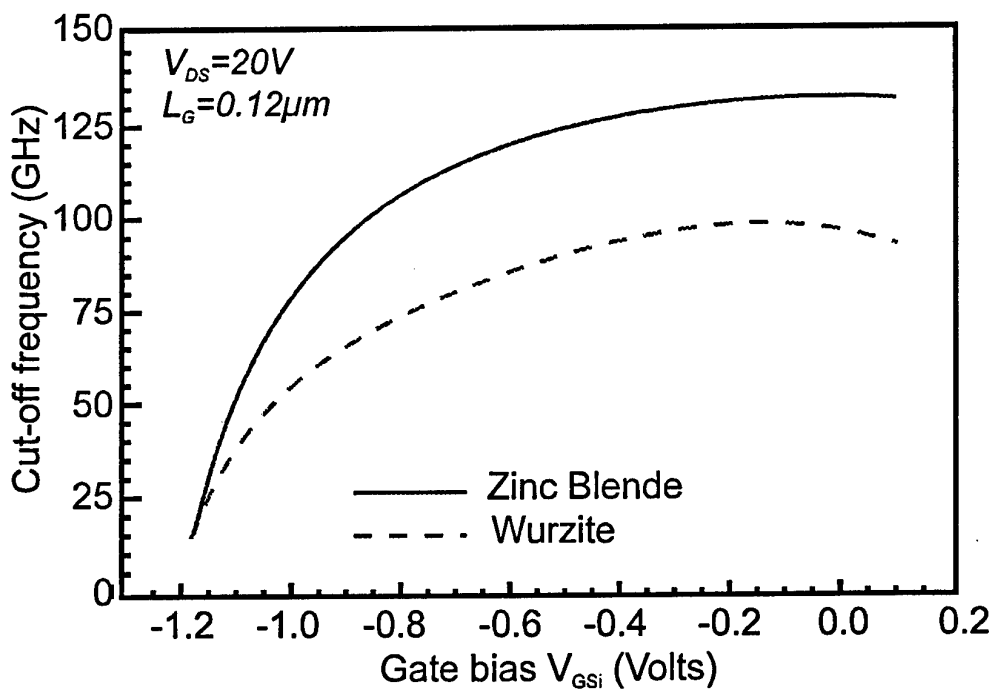
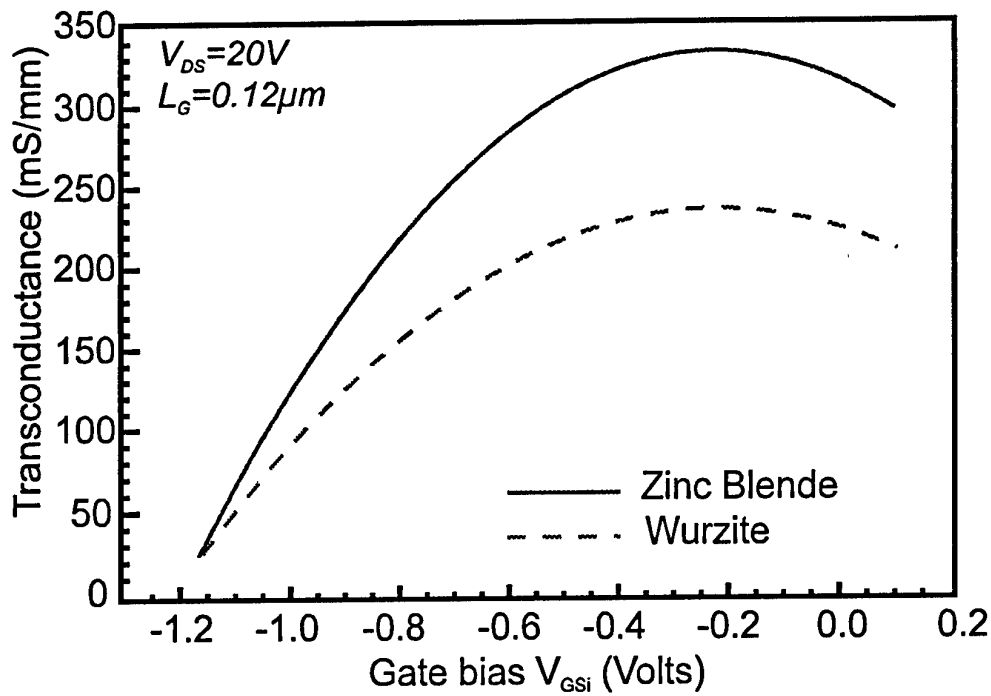


Figure 1 : Comparison of Transconductance and cut-off frequency of Zinc Blende and Wurzite GaN MESFET's

Optimization of multifunction self-aligned-gate (MSAG) GaAs MESFET

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Selective implantation of $^{28}\text{Si}^+$ and $^{12}\text{C}^+$ was used to realise the active channels of multifunction (low-noise and power) self-aligned MESFET devices¹, with a planar process characterised by a drastically reduced complexity, thus making it feasible the simultaneous realisation on the same chip of devices with different functions. Carbon was chosen for maximum long-term stability of the devices, because of the very low diffusivity of that element in GaAs. It will be shown that, in spite of the well known low activation efficiency of implanted carbon as a shallow acceptor, a carbon buried layer is very effective for carrier confinement in the conductive channel, allowing the realisation of high performance SAGFET devices.

Channel implantation was activated by rapid thermal annealing (RTA) before gate formation. A thin WNX and a thick Au film were then sputter-deposited on the entire wafer, and the masking gate geometry was defined on the Au cap by ion milling. After the $^{28}\text{Si}^+$ self-aligned (n^+) implantation and RTA, the WNX layer was removed by anisotropic CF_4/O_2 reactive ion etching. Source and drain contacts were formed by Au/Ge/Ni alloying. To increase gate-drain breakdown voltage a low resistance, T-shaped gate structure was formed by CF_4/O_2 etching of the WNX layer². A standard technology was then used to complete the multifunction devices and MMIC's. Both power and low-noise experimental devices showed DC performance comparable to that of standard recessed-gate MESFET's if no buried layer was added to SAGFET's, e.g. $\text{IDSS}=280\text{mA/mm}$, $\text{VPO}=4.5\text{ V}$ for power, and $\text{IDSS}=180\text{ mA/mm}$, $\text{VPO}=2.0\text{ V}$ for low-noise devices. Measurements performed at 12 GHz reflected the DC similitude between SAGFET's without buried layer and recessed-gate MESFET's, in particular in terms of maximum power (500 mW/mm) and minimum noise ($\text{NFMIN}=2\text{ dB}$), but a lower power added efficiency (PAE) and $\sim 1\text{ dB}$ lower associated gain was observed in SAGFET's because of poor carrier confinement in the channel ("short-channel" effect).

The optimum choice of doses and energies of channel implantation for each function was optimised with the aid of an extensive computer simulation of the electrical characteristics of the devices as a function of the technological parameters (channel and " n^+ " implantations, gate geometry, etc.).

A two dimensional drift-diffusion commercial software³ has been used for the device simulation, while doping impurities implantation profiles have been obtained from SIMS measurements. Other physical input characteristics for the simulator, like doping activation, mobility etc., has been obtained through a preliminary extensive electrical characterisation (Hall, I-V, C-V) of the technological processes. In particular it has been considered that Carbon impurities electrically behave as acceptors having either a shallow or a deep ionisation potential level with respect the valence band level⁴.

A satisfactory threshold voltage prediction has been obtained from simulations, while the systematic underestimation of drain saturation current ($\sim 20\%$) suggests that an enhanced carriers drift velocity overshoot appears, not considered by drift-diffusion models, because of the self-aligned technology.

Introduction of implanted carbon allowed the realisation of SAGFET's with a considerably higher DC transconductance (roughly doubled: $IDSS = 400 \text{ mA/mm}$, $VPO = 4.0 \text{ V}$ for power, and $IDSS = 270 \text{ mA/mm}$, $VPO = 1.5 \text{ V}$ for low-noise devices). Better confinement of carriers in the channel, also confirmed by the negligible dependence of VPO on gate length during T-gate formation, yields a globally better RF performance: noise measurements gave $NF_{MIN} = 1.5 \text{ dB}$ with $G_{ASS} = 7.5 \text{ dB}$, while power devices showed a 35% PAE at 500 mW/mm , making our SAGFET technology a convincing multifunction, low cost substitute of the traditional recessed-gate technology.

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InP based HEMT structures with a large bandgap barrier layer for power application in V band.

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GaAs pseudomorphic HEMT's present very high capabilities for power applications in the V and W bands [1]. However at very high frequencies they suffer from a limited gain and a low power added efficiency especially at large gate widths [2]. In contrast, InP based HEMT's present higher frequency capabilities but have a poor breakdown. In order to improve the breakdown, a high bandgap material can be incorporated in the barrier layer of the device structure such as $\text{Al}_{0.6}\text{In}_{0.4}\text{As}$. [3] or AlInP [4]. In this paper we have investigated novel structures with a $\text{AlAs}/\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ superlattice or a $\text{Al}_{0.65}\text{In}_{0.35}\text{As}$ layer as a barrier and a single or double heterojunction (devices A and B). The structures are described in the figure 1. The device process consists of ohmic contacts, MESA etching, followed by the gate deposition and lift-off. A tri-layer PMMA/PMMA-MAA/PMMA resist system is used for the T shape gate fabrication. The source drain distance is $2\text{ }\mu\text{m}$ and the gate length is about $0.25\text{ }\mu\text{m}$. The dc characterisation of the device A has given a maximum current density of 650 mA/mm and a breakdown voltage of the gate diode of about 11 V (figure 2) which is clearly attributed to the large bandgap barrier layer. The power capability is therefore about 800 mW/mm . The device B presents a maximum current density of 1450 mA/mm due to the pseudomorphic $\text{Ga}_{0.35}\text{In}_{0.65}\text{As}$ channel and a breakdown voltage of about 3.5 V (figure 3). The $\text{I}\times\text{V}/8$ product is then 450 mW/mm . Further breakdown characterization reveals the large breakdown capability of sample A can hardly benefit because of an uncontrollable destruction of the devices when a moderately high drain voltage (3V or more) is applied at open channel. This phenomenon cannot be prevented by usual gate or drain current limitations.

These devices have been extensively measured under small and large signal conditions. Power results obtained at 60 GHz are shown in figure 4 and 5. The device B is biased at $V_{\text{ds}} = 2\text{ V}$ and $V_{\text{gs}} = -1.5\text{ V}$. It provides an output power density of 365 mW/mm with 28% power added efficiency and 9.2 dB linear gain. Biased at $V_{\text{ds}} = 2\text{ V}$ and $V_{\text{gs}} = -0.9\text{ V}$, the device A shows an output power density of 126 mW/mm with 14.6% power added efficiency and 7.3 dB linear gain. As observed, the device B delivers a higher power than the device A because of its higher drain current. Due to its moderate breakdown and large drain current, this device is well designed for low voltage high frequency applications. However the sample A has shown a higher power density capability from dc measurements. In order to take advantage of this, the intrinsic instabilities leading to device destruction at high drain bias must be removed. We will suggest several solutions and discuss their possible effect on the device characteristics.

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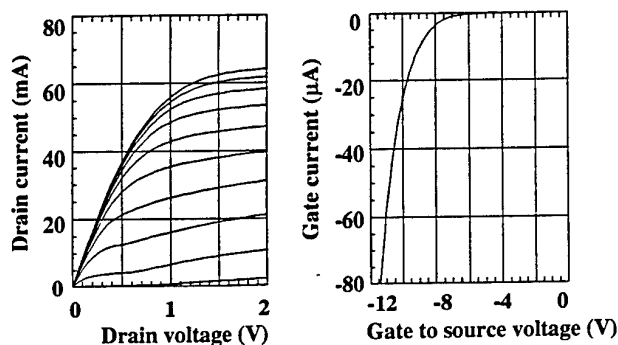
GalnAs $5 \times 10^{18} \text{ cm}^{-3}$	7 nm
AlInAs	5 nm
4 X { AlAs	2 nm
AlInAs	3 nm
$\delta = 5 \times 10^{12} \text{ cm}^{-2}$	
AlInAs	3 nm
AlAs	2 nm
GalnAs	15 nm
LT AlInAs buffer	300 nm
AlInAs	100 nm

S.I. InP substrate
Sample A

GalnAs $5 \times 10^{18} \text{ cm}^{-3}$	7 nm
$\text{Al}_{0.65}\text{In}_{0.35}\text{As}$	15 nm
$\delta = 4 \times 10^{12} \text{ cm}^{-2}$	
$\text{Al}_{0.65}\text{In}_{0.35}\text{As}$	5 nm
$\text{Ga}_{0.35}\text{In}_{0.65}\text{As}$	15 nm
$\delta = 2 \times 10^{12} \text{ cm}^{-2}$	
AlInAs	5 nm
LT AlInAs buffer	300 nm
AlInAs	100 nm

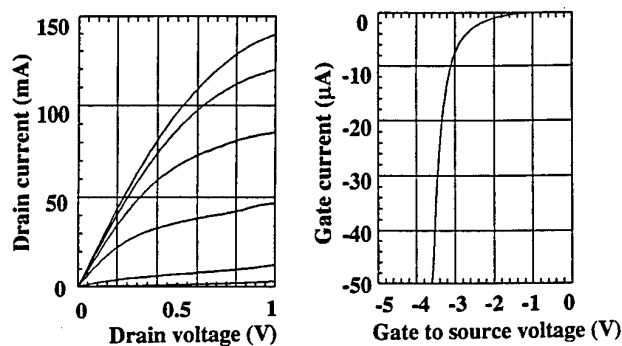
S.I. InP substrate
Sample B

Figure 1 : The device structures under investigation.



$V_{gs} = -1.6 \text{ to } 0.4 \text{ V}$, step : 0.2 V.

Figure 2 : dc device I-V and breakdown characteristics of sample A.
The device width is $2 \times 50 \mu\text{m}$.



$V_{gs} = -2.5 \text{ to } 0.6 \text{ V}$, step : 0.5 V

Figure 3 : dc device I-V and breakdown characteristics of sample B.
The device width is $2 \times 50 \mu\text{m}$.

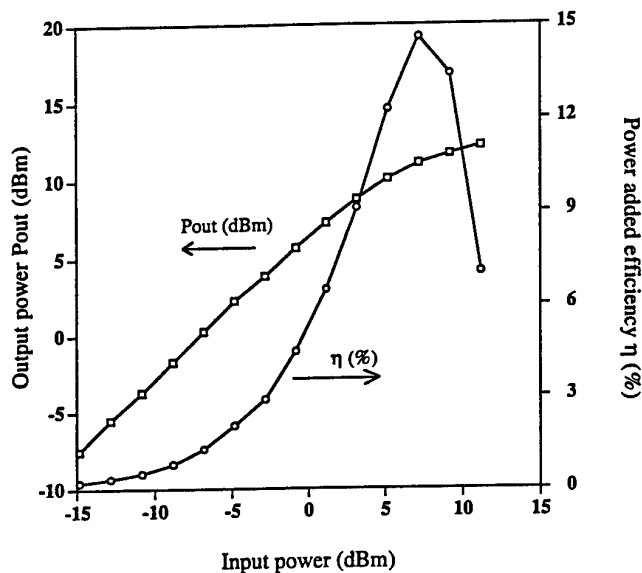


Figure 4 : Output power and efficiency at 60 GHz for sample A.
 $V_{ds} = 2 \text{ V}$, $V_{gs} = -0.9 \text{ V}$.

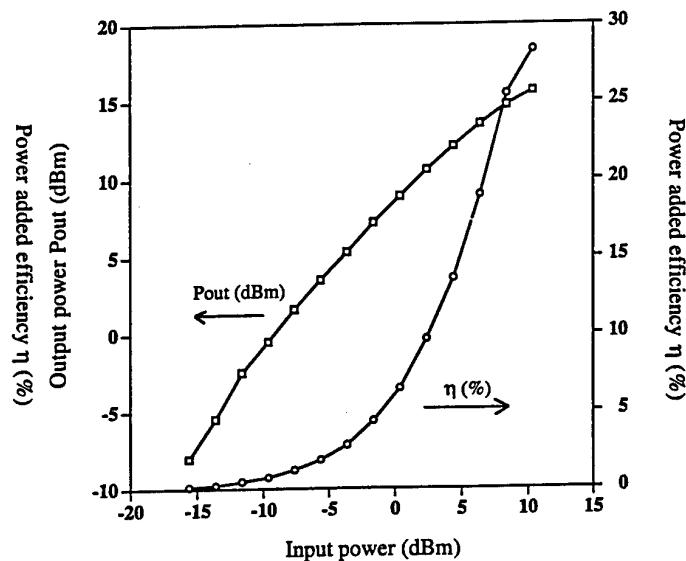


Figure 5 : Output power and efficiency at 60 GHz for sample B.
 $V_{ds} = 2 \text{ V}$, $V_{gs} = -1.5 \text{ V}$.

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May 25-28, 1997

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Title
Room temperature InSb MISFETs

ABSTRACT

Indium Antimonide (InSb) has a very high mobility compared to Si or GaAs but its high intrinsic carrier concentration at room temperature due to its small band gap has meant that the devices had to be cooled to low temperatures. Room temperature operation of devices including MISFETs, LEDs and detectors with high performance have been demonstrated in InSb. This has been achieved by using the principle of exclusion/extraction in MBE grown heterostructures of InSb. A novel self-aligned technique has been used for fabricating the MISFET. A low temperature photolytic oxide with a very low interface state density ($D_{it} \sim 3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$) has been used as the gate oxide. This has given an AC g_m of 100 mSmm^{-1} and an f_t of about 14GHz for a $1 \mu\text{m}$ gate length. Work is underway to increase the f_t to about 60GHz for a $1 \mu\text{m}$ gate as predicted by modelling.

Zero-bias Detection with $\text{In}_{0.38}\text{Ga}_{0.62}\text{As}$ Schottky Barrier Diodes

K. Lübke, T. Hilgarth, Ch. Diskus, A. Stelzer, A. Springer, H. W. Thim

Introduction

The demand for an increase in data transfer rate and sensor sensitivity raises the interest in devices for millimeter wave applications. The advantage of millimeter-wave-sensors is their robustness against environmental factors like dust, water vapour and noise.

In millimeter-wave-systems suited for automotive applications Schottky-barrier diodes are used for detecting and mixing signals because of their high switching speed which results from the unipolar conduction mechanism. III-V semiconductors are the preferred materials because of their higher electron mobility. In this work the design and fabrication procedures of a zero bias $\text{In}_{0.38}\text{Ga}_{1-0.38}\text{As}$ -Schottky detector diode for 35 GHz are described.

Design

The voltage sensitivity of a detector diode is defined as the output voltage generated by the diode into the load circuit divided by the RF-power absorbed in the diode [1].

The voltage sensitivity, β_v , of a circuit with load resistance R_L is given by

$$\beta_v = \frac{0.0005}{(I_s + I_0)(1 + R_j/R_L) \left[1 + (\omega C_j)^2 R_s R_j \right]} \left[\frac{\text{mV}}{\mu\text{W}} \right].$$

I_s reverse saturation current

I_0 bias current

C_j junction capacitance of the diode

R_s series resistance

R_j dynamic resistance ($=q/nkT(I_s+I_0)$).

It is well known that large LO power is needed to minimize conversion loss of a GaAs Schottky mixer diode. This is a consequence of the high barrier height of about 0.7 eV of GaAs Schottky diodes. For a typical set of parameters ($f=35\text{GHz}$, $n=1.4$, $R_s=10\ \Omega$, $C_j=70\ \text{fF}$, $R_L=1\ \text{M}\Omega$) the maximum of the sensitivity β_v can be calculated from the above equation. If the detector should be used without bias current, which simplifies circuitry, then $I_0=0$ and the saturation current I_s has to be in the range of $10^{-6}\ \text{A}$. This corresponds to a barrier height of approximately 0.22–0.25 eV. To achieve mixing with high sensitivity at zero bias the energy barrier of the diode must be made low [2]. This has been accomplished by embedding an InGaAs layer underneath the Schottky contact.

Diode Fabrication

The diodes have been fabricated using epitaxial layers of $\text{In}_{0.38}\text{Ga}_{0.62}\text{As}$ grown by metal organic vapor deposition (MOCVD) on semi-insulating GaAs substrates. In order to grow good quality $\text{In}_{0.38}\text{Ga}_{0.62}\text{As}$ layers on GaAs a graded buffer layer is needed to compensate the difference in lattice constants between InGaAs and GaAs. The Indium-content is increased from 0 to 38% in steps of 5% in this layer. The first active layer grown is an n^+ -InGaAs layer doped $6 \cdot 10^{18}\ \text{cm}^{-3}$ with a thickness of 0.8 μm for low R_s . On top of this layer a 0.19 μm thick n -InGaAs layer with $2 \cdot 10^{16}\ \text{cm}^{-3}$ doping concentration has been grown. To form the ohmic contact the n -doped layer on the top is removed by etching and the

conventional Ni/Au/Ge/Au layer system is thermally evaporated onto the n^+ -layer and alloyed. After that a double layer of Cr/Au is evaporated on both the Schottky-contact-area and the ohmic contact.

A cross-sectional view of the Schottky-barrier diode is shown in Fig. 1. Fig. 2 shows a SEM photograph of the diode.

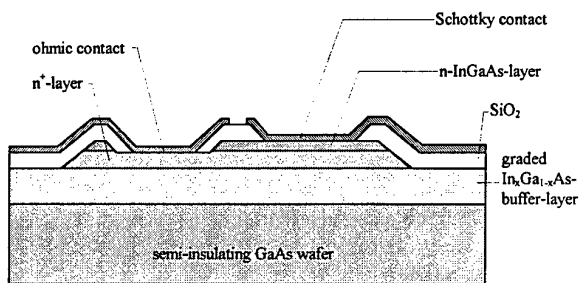


Fig. 1: Cross-sectional view of the sandwich Schottky barrier diode

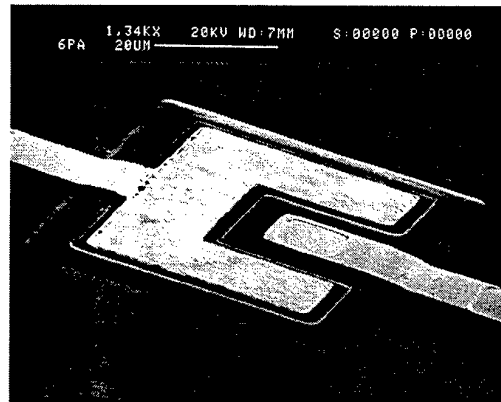


Fig. 2: SEM picture of the diode

Diode Characteristics

The semi-logarithmic plot of the forward current-voltage relationship was used to calculate ideality factor, series resistance and barrier height of the devices. Typical values for reverse saturation current I_s , series resistance R_s and ideality factor n of diodes with contact area $3 \mu\text{m} \times 3 \mu\text{m}$ are shown in Tab. 1.

ideality factor	saturation current	series resistance	barrier height	capacitance
1.45	$8.2 \cdot 10^{-6} \text{ A}$	9.7Ω	0.22 eV	10.7 fF

Tab. 1: Typical values of $\text{In}_{0.38}\text{Ga}_{0.62}\text{As}$ Schottky barrier diodes with anode area of $3 \mu\text{m} \times 3 \mu\text{m}$

Using this value the diode's cut-off frequency $f_{co} = 1/2\pi R_s C$ was calculated to be approximately 1500 GHz.

Conclusion

The fabricated diodes have been operated as mixers in a 35 GHz radar system in order to test their high frequency performance. The diodes were connected to a 50Ω stripline. A sensitivity of $1 \text{ mV}/\mu\text{W}$ was obtained in this configuration.

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INP-BASED HETEROSTRUCTURE BARRIER VARACTOR

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The decrease of the output power in harmonic multiplication chains is one of the key issue in the development of millimeter and submillimeter wave systems. In this paper we investigate how this major drawback can be overcome by means of heterostructure barrier varactors (HBV's) in the framework of an ESA contract*. This kind of device consists of a blocking wide gap semiconductor sandwiched between two narrow gap spacer layers. The main motivations for developing such a structure are the natural symmetry in the capacitance voltage characteristics, the numerous degrees of freedom in the design and more importantly the possibility to stack several structures on the same epitaxy. On the other hand, from the material point of view, InP-based material system appears preferable with respect to GaAs for operating at very high frequency. Its advantages in terms of high mobility, high conduction band offset and high doping levels are now widely recognized.

In order to improve the voltage capability and hence the output power, several tracks were followed. In a first stage, we tried to improve the breakdown voltage of a single device. Indeed, it can be shown that a conventional HBV cannot operate at high voltage owing to parasitic tunneling current. On this basis, we grew by GSMBE Single Heterostructure Barrier Varactor (SHBV) with a step-like barrier scheme alleviating the problem of leakage current by Fowler Nordheim tunneling emission (Fig. 1). By this means, we obtained an improvement by a factor of 3 of the breakdown voltage ($V_b=6V$) limited now by impact ionization. Then, an effort was devoted to the optimization of the capacitance versus voltage characteristic and of the series resistance which are major figures of merit in the multiplication performance. To this aim, varactor diodes were fabricated in a two step mesa technology according to two test patterns. The first one uses concentric pad circles and the diodes are rf tested by positioning directly the probes on the diode ohmic contacts. Such an arrangement permits one to assess the intrinsic elements of the devices over a very broad frequency band. The other maskset involves air-bridged devices interconnected to coplanar waveguide footprints (Fig. 2). In that case, the extrinsic elements of the interconnections to the external circuit can be accurately measured. At last, we decided to apply the fabrication techniques to some epilayers which consist of two stacked SBV's grown on the same epitaxy. The associated advantages of such Dual Heterostructure Barrier Varactors (DHBV's) are a breakdown voltage twice higher and a lower capacitance by a factor of two.

Figure 3 shows and compares the I-V characteristics measured at room temperature for a SHBV and a DHBV respectively. The I-V characteristics appears remarkably symmetric attesting the high quality of epilayers. Moreover, the characteristics scale with complexity in agreement with the above arguments. An illustration of typical capacitance-voltage variations measured at 500MHz and at the pump frequency of 85 GHz is reported in Figure 4 for a DHBV. The capacitance versus voltage varies steeply with a ratio of 5:1 and a normalized capacitance of about $1fF/\mu m^2$ at 0V. Measurements of the contact resistance R_c were made by a TLM procedure and values as low as $2 \times 10^{-7} \Omega.cm^2$ were found. Turning now to the second mask set, Figure 4 shows the variation of the reflection coefficient plotted in a Smith Chart along with the data calculated from using a lumped element circuit. It consists of extrinsic elements ($L_p=75pH$, $C_p=17fF$) and of intrinsic elements (C_d and G_d) measured previously. Concerning the overall series resistance R_s which includes many contributions notably the resistance due to ohmic contacts and to epilayers along with the lateral access resistance, it was found that the latter was the dominant in the present technological runs with values typically of 5 or 10 Ω according to the technology employed.

* In collaboration with Matra Marconi Space Toulouse, Chalmers University and Observatoire de Paris

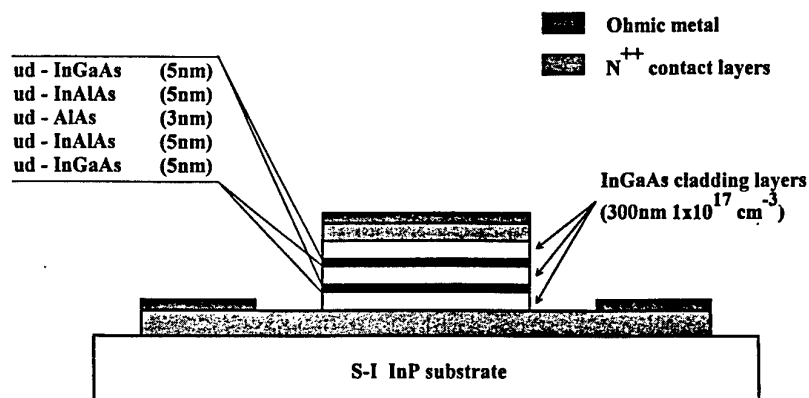


Fig.1: Schematic of DHBV's in a two step mesa technology

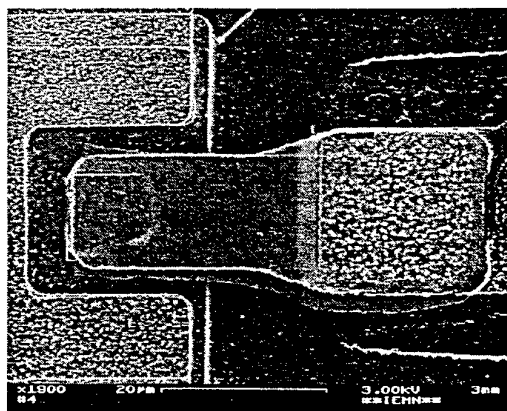


Fig. 2: SEM view of an air-bridged device

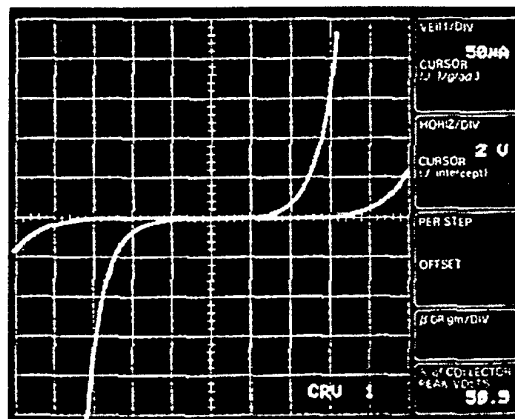


Fig. 3: I-V characteristics for SHBV's and DHBV's

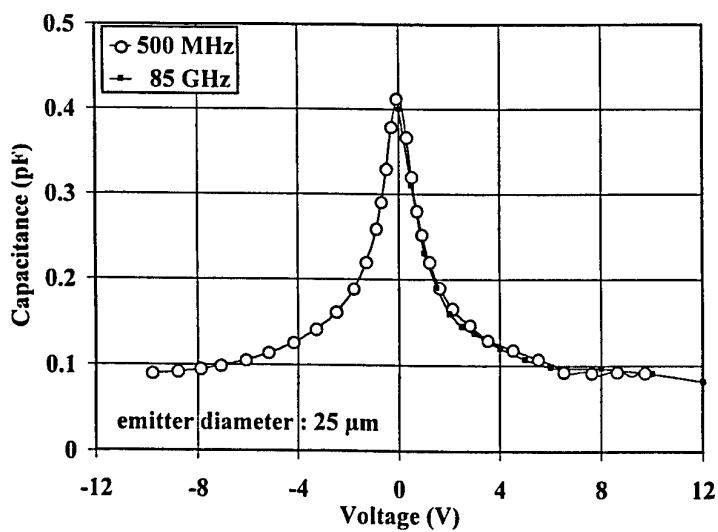


Fig. 4: Capacitance-voltage characteristics at 500 MHz and 85 GHz respectively

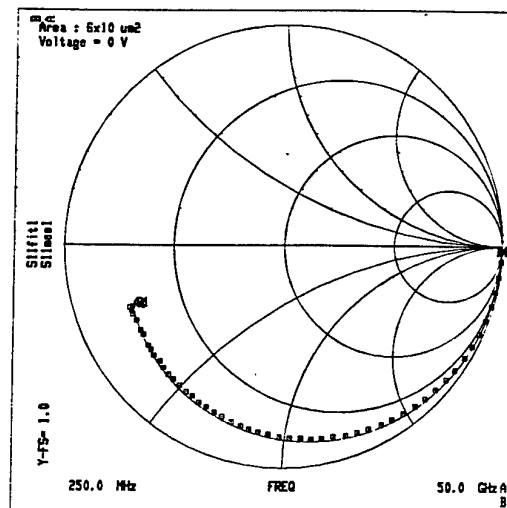


Fig. 5 Reflection coefficient for a DHBV (Area 6x 10 μ m²)

Wednesday, May 28

8.30 - 10.00, Session 7: Heterobipolar Transistors

08.30 1. (Invited Paper) *D. Streit, TRW Electronic Systems :*

"HBT Production for commercial Applications:
Present and Future Trends"

09.00 2. *Burhan Bayraktaroglu:*

"Highly robust GaAs Cascode HBTs for microwave and
millimeter-wave application".

3. *A. Huber, C. Bergamaschi, T. Morf, H. Jäckel:*

"Low Frequency and Microwave Noise Performance of
InP/InGaAs HBTs as a Function of Bias-Point, Temperature
and Emitter-Geometry".

4. *B.C. Lye, H.K. Yow, P.A. Houston, C.C. Button:*

"GaInP/AlGaAs/GaInP Double Heterojunction Bipolar
Transistors with Zero Conduction Band Spike at the Collector"

5. *A.R. St Denis and D.L. Pulfrey:*

"A microscopic view of quasi-ballistic transport in HBTs".

6. *R. Beccard, M. Volk, D. Schmitz, H. Jürgensen, M.A. Knowles,
D. McCulloch, N. Pan and D. Hill:*

"Multiwafer Planetary Reactors: A tool for Reliable Mass
Production of HBT Wafers".

**HBT Production for Commercial Applications:
Present and Future Trends**

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A wide variety of commercial wireless products such as cellular phones and digital radios are now being sold that use TRW's GaAs heterojunction bipolar transistor monolithic microwave integrated circuits. These HBT MMIC-based products are attractive for consumer electronics because they have performance and price advantages compared to traditional silicon or GaAs MESFET products. TRW's commercial HBT MMIC chip production has been growing at a compound annual rate of over 100% for several years, and this growth rate is projected to continue through the foreseeable future. We are currently shipping over two million HBT integrated circuits per month to original equipment manufacturers around the world. Next generation insertions for our GaAs HBTs will include MMICs for high speed digital and optoelectronic products in addition to the traditional microwave applications. We describe the production methodology, reliability, and applications of our GaAs HBTs for present and future products. In addition, we will present insertion opportunities and recent results of our development work for InP-based HEMT and InP-based HBT MMICs and monolithic HEMT-HBT integrated circuits.

HIGHLY ROBUST GaAs CASCODE HBTs FOR MICROWAVE AND MILLIMETER-WAVE APPLICATIONS¹

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The high power density of GaAs HBT allows the fabrication of compact microwave power amplifiers for monolithic integration. In such applications, special care is needed in the design of transistor cells to ensure that thermal stability is maintained by eliminating local temperature variations. The main source of thermal instability in high power HBT cells is the electrothermal feedback at the emitter-base junction. The Thermally-Stable Cascode HBT (TSC-HBT) design described here overcomes this problem by separating the electrical regulating part of the device from the heat generating part. The electrothermal feedback is therefore eliminated resulting in very robust devices that also have high microwave power gain characteristics.

As illustrated in Figure 1, each sub-cell of the TSC-HBT is electrically isolated from one another. The common-emitter (CE) part of each sub-cell resides in the "cold zone" of the device since the voltage drop across this part is small. The common-base (CB) part, on the other hand, sustains most of the collector voltage and has a higher junction temperature. However, the local temperature of this part of the device can not influence the local current, which is regulated by the CE section in the cold zone.

Figure 2 shows a SEM picture of a TSC-HBT cell with 12 emitter fingers arranged in 6 sub-cells. The maximum power handling capability of TSC-HBT designs were compared to conventional Cascode HBTs by fabricating them on the same wafer. As shown in Figure 3, the TSC-HBT can dissipate 300% more power than an identical size conventional

Cascode cell with the same thermal impedance. Since the ruggedness of an HBT is related to its power handling capacity, TSC-HBT showed excellent thermal stability under heavy microwave bias conditions. An 8-finger cell was tested at 10 GHz with load impedances varying from values for optimum power output to conditions for VSWR of 4:1. The transistor dc voltage and current was increased by 300% of the nominal bias conditions while the load impedance was in mismatch. No device failure was observed due to thermal instability.

The small-signal microwave characteristics of a 8-finger TSC-HBT are shown in Figure 4. The current gain cut-off frequency, f_T , of 50 GHz and the maximum frequency oscillation, f_{max} , value of larger than 100 GHz were obtained for devices with 1 μ m thick collector layers. At 8 GHz, 0.5 W output power was obtained with 19.5 dB gain and 70% PAE. The same cell produced again 0.5 W output power at 14 GHz with 17 dB gain and 54.5% PAE. A larger cell produced 1.0 W output power at 8 GHz with 19.5 dB gain and 61.5% PAE. The devices were found to have useful large-signal power gain (>8 dB) at frequencies up to 35 GHz.

Finally, the reproducibility of TSC-HBT was determined by measuring the small-signal microwave power gain at 11 GHz using on-wafer probes across the entire wafer. As shown in Figure 5, the power gain variation was about 0.3 dB out of approximately 30 dB at this frequency. This variation is about the same as the repeatability of the measurement system itself.

¹ This work was sponsored by Naval Research Laboratory Contract No: N00014-95-C-6026 (DARPA MAFET Thrust 2 Program).

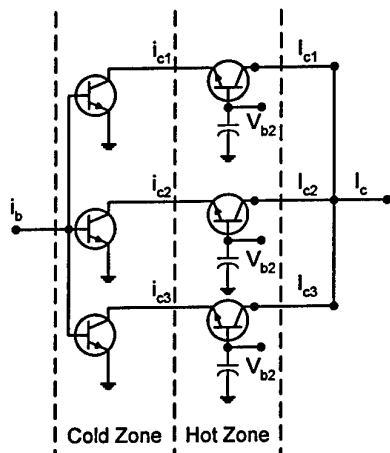
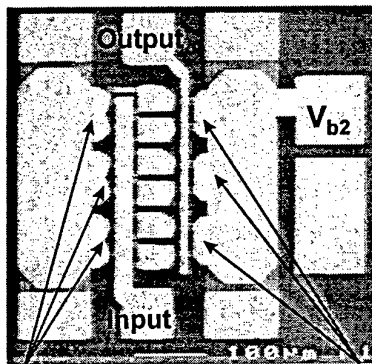


Figure 1: Schematic drawing of a 3 sub-cell TSC-HBT showing the separation of current regulating and power generating regions into independent temperature zones.



CE sub-cells **CB sub-cells**

Figure 2: Photograph of a 12-finger Cascode HBT with 6 sub-cells in common-emitter and common-base stages. The base voltage of the CB device is adjusted with V_{b2} .

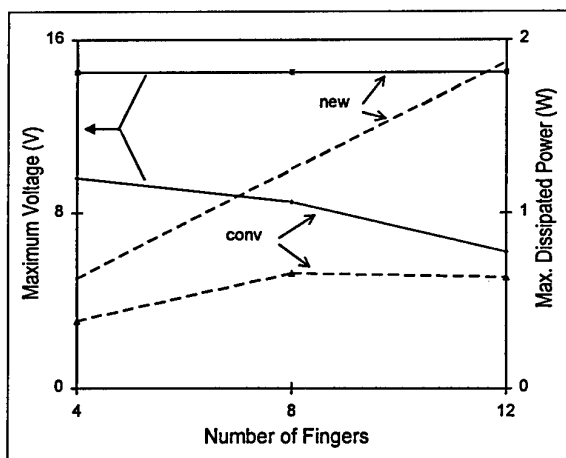


Figure 3: The maximum voltage and power dissipation as a function of cell size. Both types of devices were fabricated on the same wafer, and tested with 41 kA/cm^2 current density.

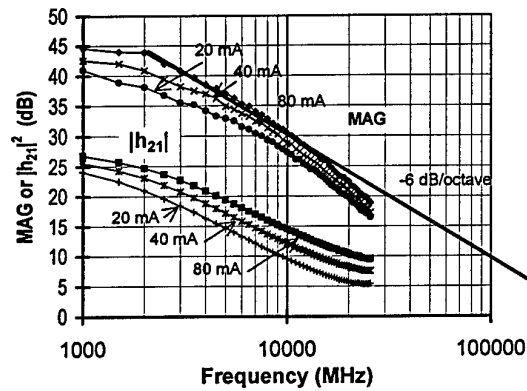
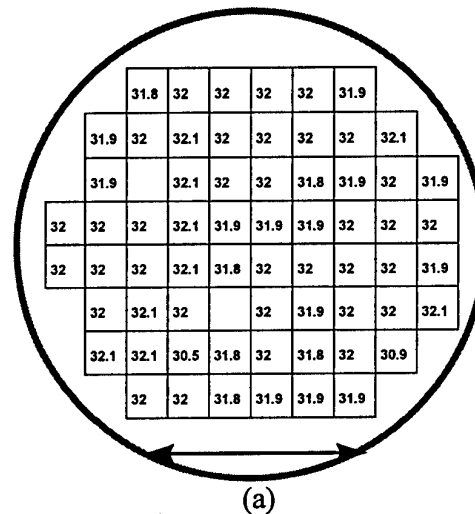
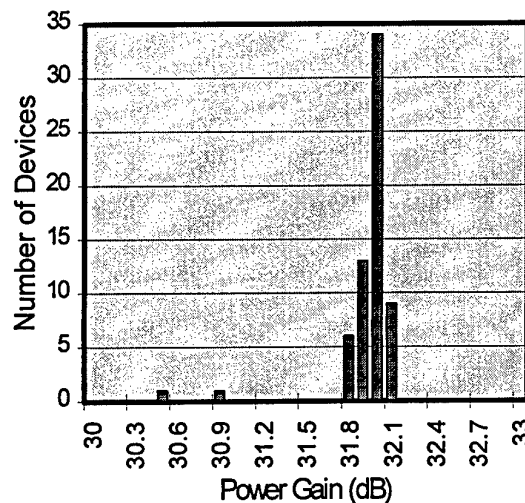


Figure 4: Small-signal microwave characteristics of 8-finger TSC-HBT cell as a function of collector current.



(a)



(b)

Figure 5: Maximum Available Gain (MAG) at 11 GHz (a) variation across a 3-inch wafer, (b) variation statistics.

Low Frequency and Microwave Noise Performance of InP/InGaAs HBTs as a Function of Bias-Point, Temperature and Emitter-Geometry

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Abstract

A complete low frequency and microwave noise characterization as a function of emitter-geometry, bias-point and frequency of InP/InGaAs HBTs has been carried out. The small-signal parameters of an equivalent noise model were extracted.

1 Introduction

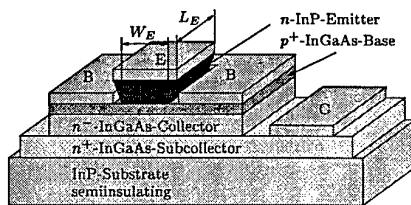
InP-based HBTs are advantageous for optoelectronic applications because of the excellent optical and transport properties of both InP and InGaAs. In these broadband applications, an optimal noise performance is important in the whole frequency band, from a few hertz to tens of gigahertz. The aim of this presentation is to show whether there is a tradeoff between the optimization of low frequency noise and microwave noise performance.

2 Measurement / Model

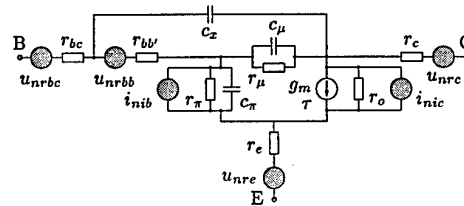
Using a MOCVD-grown epitaxial layer structure and a self aligned emitter technology, high speed InP/InGaAs HBTs with f_T and f_{max} of 80 GHz and 120 GHz respectively, were successfully fabricated [1].

Low frequency noise from 2 Hz to 200 kHz and microwave noise on wafer measurements from 2 to 26 GHz were carried out at different bias points and temperatures. In order to optimize the emitter geometry, we have varied the emitter widths W_E from 1 μm to 2.5 μm in steps of 0.5 μm with emitter lengths L_E of 5, 8, 16 μm (W_E , L_E see Figure 1(a)).

We developed a small signal noise model (Fig. 1(b)) which consists of two correlated shot noise sources, the thermal noise source of the parasitic resistance and a frequency dependent noise source at the input of the transistor. Noise measurements were used to determine the magnitude and the correlation of these noise sources.



(a) Cross-sectional view of the HBT

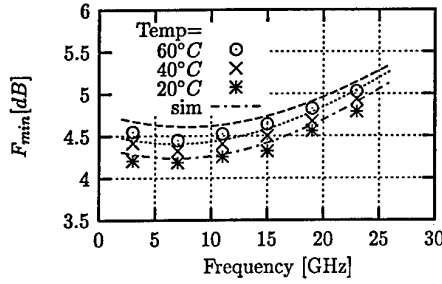


(b) Equivalent circuit model

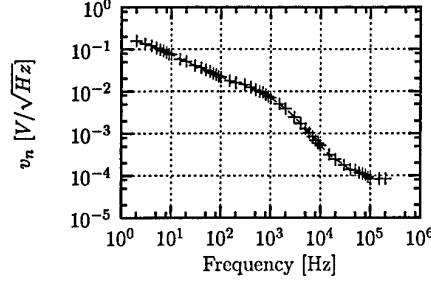
Figure 1: Cross-sectional view and circuit model of the HBT

3 Results

Figure 2(a) shows the simulated and measured results of the microwave noise figure. A very good agreement between measurements and simulation has been achieved even at different temperatures. In the low frequency region we observed significant burst noise with an corner frequency of 1 kHz (Fig. 2(b)). As depicted in Figure 3, we observed an optimal emitter geometry and bias point for achieving a minimum microwave noise measure [2].

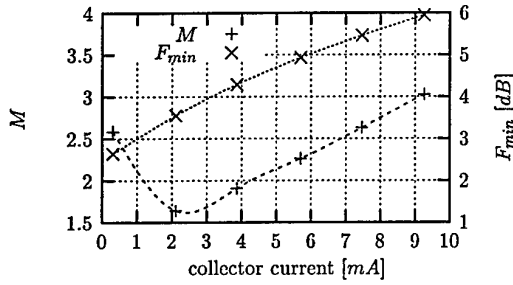


(a) Minimum noise figure of a $1.5 \times 8 \mu m^2$ HBT for the temperatures of 20, 40 and $60^\circ C$ at $I_C = 2 mA$

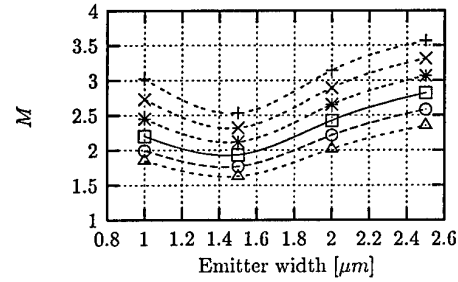


(b) LF Noise of a $2.5 \times 8 \mu m^2$ HBT for the temperatures of $20^\circ C$ at $I_C = 2 mA$

Figure 2: HF and LF noise characteristics of the HBT



(a) Measured noise measure and noise figure vs the collector current of an $1.5 \times 8 \mu m^2$ at $f = 10 GHz$



(b) Measured noise measure M vs the emitter width W_E for an emitter length $l_E = 8 \mu m$, $f = 10 GHz$, $I_C = 2 mA$ (Δ) ... 7 mA (+)

Figure 3: Optimal bias-point and emitter-width for a minimal noise measure M

References

- [1] R. Bauknecht, H. Schneibel, J. Schmid, and H. Melchior, "12 Gbit/s Laser Diode and Optical Modulator Drivers with InP/InGaAs Double HBTs," *Electronics Letters*, vol. 32, pp. 2156–2157, Nov. 1996.
- [2] A. Huber, C. Bergamaschi, R. Bauknecht, H. Jäckel, and H. Melchior, "Minimization of the Noise Measure of InP/InGaAs HBTs." Accepted for the 9th Intl. Conference on Indium Phosphide and Related Materials 97.

GaInP/AlGaAs/GaInP Double Heterojunction Bipolar Transistors with Zero Conduction Band Spike at the Collector

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GaInP/GaAs/GaInP double heterojunction bipolar transistors (DHBTs) make use of the large breakdown voltage offered by the wide gap collector for high power applications. However, the conduction band spike at the abrupt GaAs/GaInP base-collector junction gives rise to an undesirable voltage dependence of gain at low collector-emitter bias. Solutions to this problem include the incorporation of an undoped GaAs spacer layer, adjacent to the GaInP collector, and/or an n^+ doping region in the vicinity of the spike to encourage tunnelling. Drawbacks to these methods are the reduced Kirk effect current and tunnelling breakdown if the n^+ layer is not positioned accurately. We present a novel approach to eliminate the conduction band spike using AlGaAs as the base material, which has been shown to have a zero conduction band offset with GaInP for an Al concentration in the group III sublattice of $\geq 11\%$.

A compositionally graded base layer structure was designed to have a sizeable bandgap difference between the emitter and base (estimated to be 0.214eV at the GaInP/Al_{0.21}Ga_{0.79}As emitter junction), a reasonable compositional built-in quasi field of 15.6kV/cm and a zero conduction band discontinuity at the Al_{0.11}Ga_{0.89}As/GaInP collector junction. Fig. 1 shows the output characteristic of the DHBT with the graded AlGaAs base and is compared to an AlGaInP/GaAs/GaInP device with identical collector doping and thickness ($2 \times 10^{16} \text{cm}^{-3}$ and $1 \mu\text{m}$, respectively). The effectiveness of using the AlGaAs base to remove the current blocking conduction band spike is clearly evident from the relatively sharp increase in the collector current at low V_{CE} for the AlGaAs base device. The breakdown voltages, V_{CEO} and V_{BCO} , are 44.5V and 54.5V respectively, and are comparable with the GaAs base device. Magneto-transport measurements were carried out in the base and showed a reduced electron mobility compared to GaAs (fig.2). Despite the lower base doping and the built-in field, which results in a reduction of the base transit time, the common emitter current gain was less in the AlGaAs base device (fig.3) due to the much reduced minority electron lifetime in the p^+ AlGaAs base compared to the GaAs base (fig.4). In addition, the ideality factor for the base current reflects the reduced quality of the emitter-base interface with Al in the base. Despite these limitations, the structures described here will be useful in high power HBT applications.

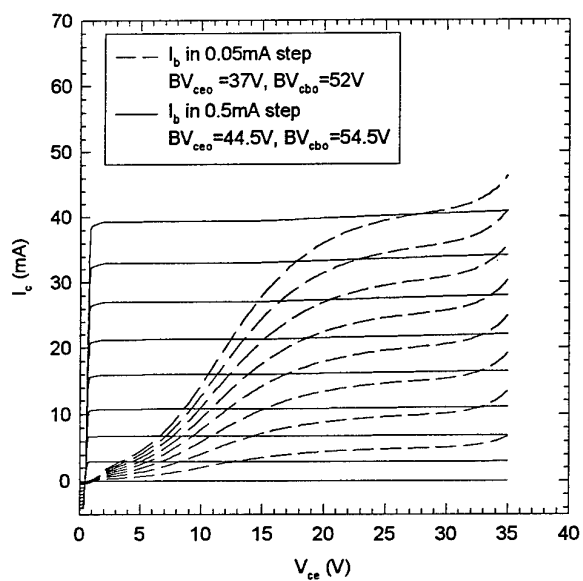


Figure 1.

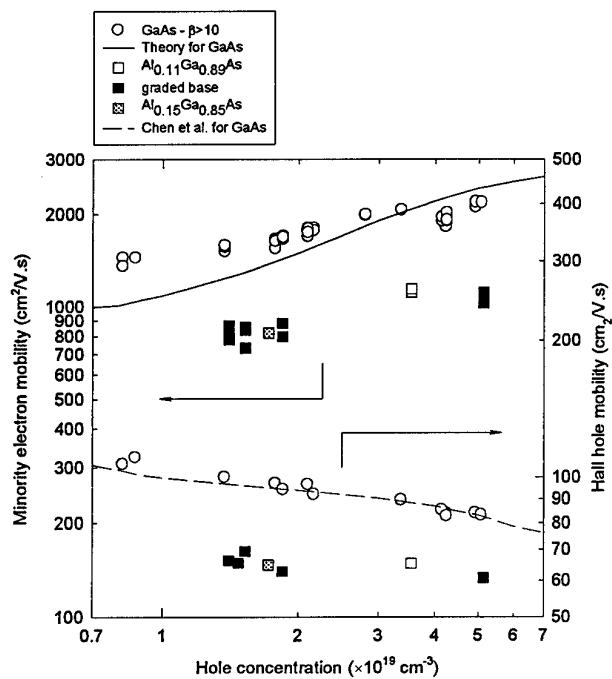


Figure 2.

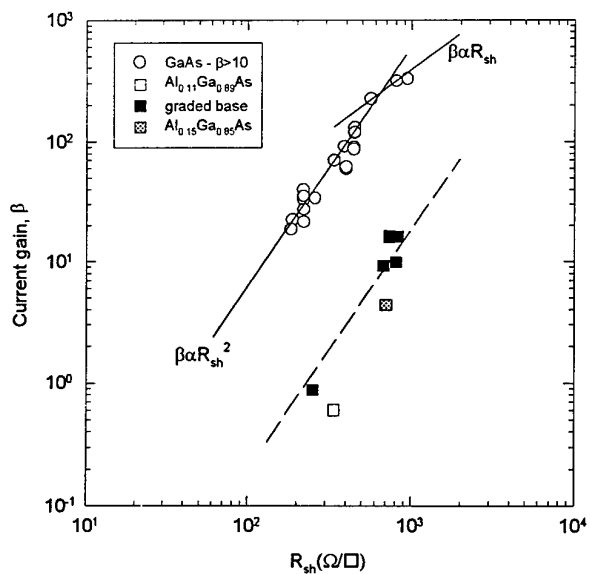


Figure 3.

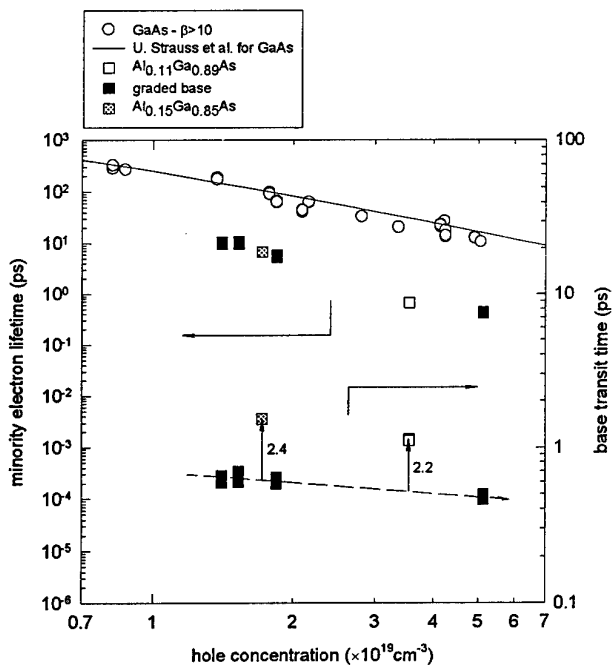


Figure 4.

A microscopic view of quasi-ballistic transport in HBTs

A.R. St Denis and D.L. Pulfrey

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Vancouver, British Columbia V6T 1Z4, Canada

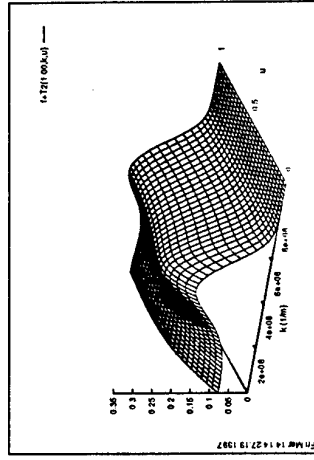
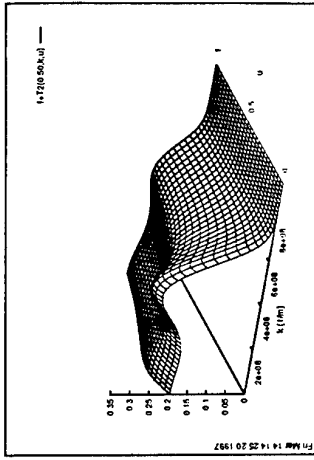
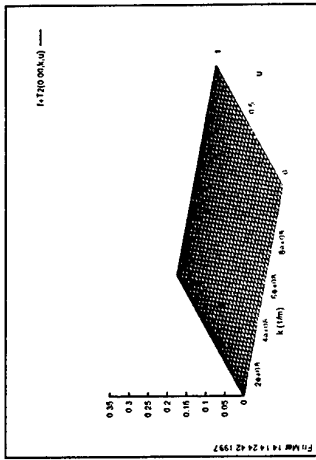
In the steady-state, field-free case the Boltzmann Transport Equation reduces to an ordinary differential equation that can be solved exactly using an integrating factor. We have used such an approach to investigate transport in the short base region of an AlGaAs/GaAs HBT. The injection of electrons into the base by thermionic emission and tunneling at the emitter-base junction has been taken into account via an appropriate boundary condition. So far, scattering mechanisms due to ionized impurities and polar-optical phonons have been considered. The results are interesting because of the novel perspective of transport that is given by being able to view the evolution of the components of the distribution function at various positions in the base.

Results at three positions in the base are shown in Fig. 1 for the case of screened ionized impurity scattering in a highly doped base (10^{19} cm^{-3}) of width equal to one mean-free-path length ($920 \text{ \AA}$). Column 1 is the total forward-going distribution, and is the sum of the components shown in the other three columns. Column 2 is the distribution of ballistic electrons, *i.e.*, those that entered from the emitter and have not yet scattered. Column 3 is the distribution of electrons that had been moving towards the emitter and were reflected from the electrostatic potential barrier at the base-emitter junction. Column 4 is the distribution of electrons that have been scattered into the forward direction. Note that the vertical scale for the components in Columns 3 and 4 is 1/10 that for the distributions in Columns 1 and 2.

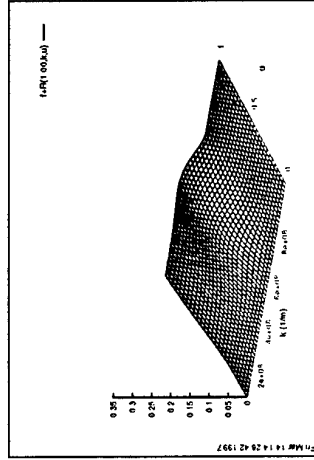
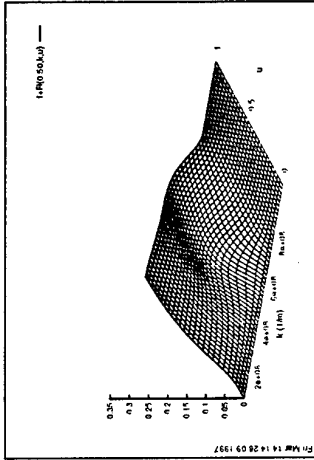
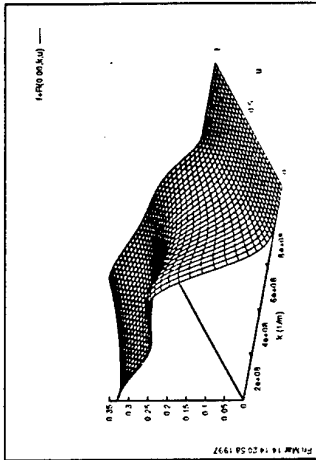
The implications of these results as regards the collector current and the base transit time for HBTs with very short bases will be discussed. Results for polar-optical phonon scattering will also be presented.

In the figure on the accompanying page, the top, centre and bottom rows show the forward-going distribution and its components at the emitter-edge of the base, the centre of the base, and the collector-edge of the base, respectively.

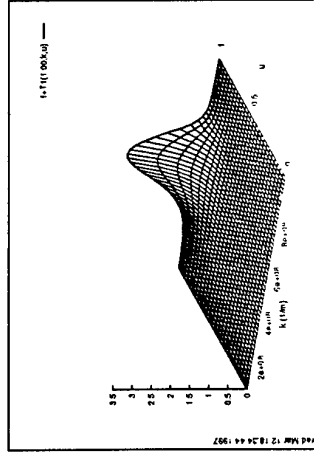
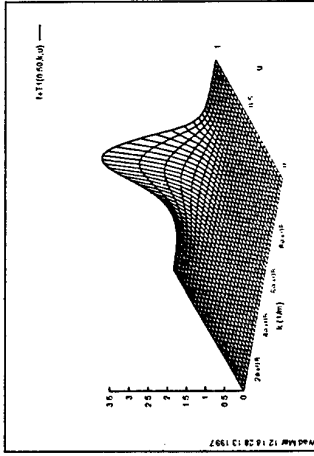
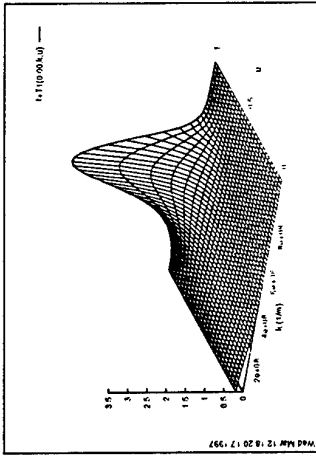
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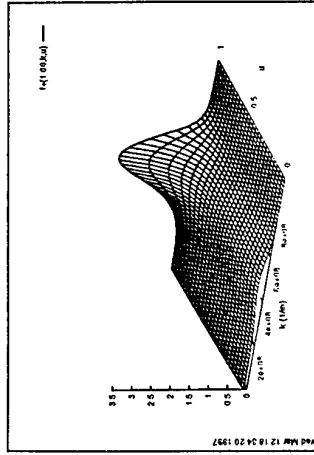
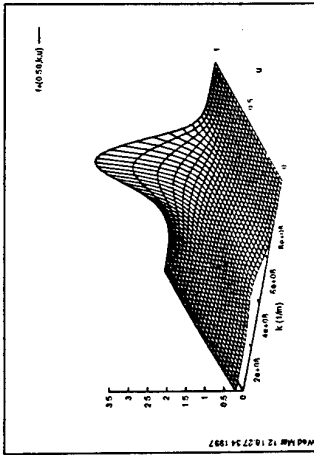
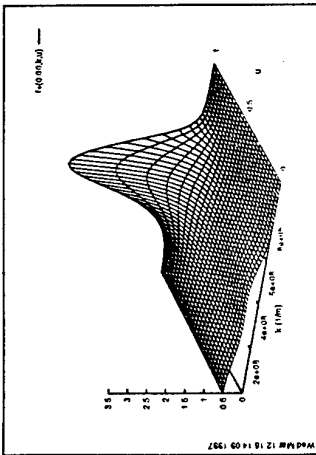
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BALLISTIC



TOTAL



Multiwafer Planetary Reactors: A Tool for Reliable Mass Production of HBT Wafers

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Kopin Corporation, 695 Myles Standish Boulevard, Taunton, MA

Reliable production of HBTs requires a highly reproducible supply of epitaxial wafers. This means for the MOVPE growth that a maximum of reproducibility and uniformity is needed. With the AIXTRON Planetary Reactors[®] we present a class of MOVPE reactors that meets these requirements in an optimum way. The reactors have loading capacities from 7x2" wafers up to 95 2" wafers (or equivalent numbers for 3", 4" or 6" wafers). In this study, we present data obtained on a 5x4" reactor (AIX 2400).

For the production of HBT structures, GaAs, AlGaAs and GaInP were grown as base materials. All these materials can be grown with thickness uniformities in the 2% range on 4" wafers. This was verified by growing Bragg reflectors showing very uniform colours over the entire 4" area. Doping was performed with silicon as an n-type dopant using silane and with carbon using TMAs. Doping uniformities are better than $\pm 3\%$ for n-type material (Si). Carbon doping yields high acceptor concentrations above 10^{19} cm^{-2} . The uniformity of carbon doped layers is better than $\pm 5\%$. On the other hand, undoped material can be grown with low background carrier concentrations (10^{14} cm^{-3} for GaAs).

The compositional uniformity of GaInP is also excellent. Room temperature PL maps show standard deviations of the emission wavelength around 2 nm across a 4" wafer. Run-to run reproducibilities of all layer properties were in the 1%-regime.

The results show that the AIXTRON Planetary Reactors[®] are inherently uniform in all layer characteristics. No tuning of parameters is necessary to obtain stable and uniform conditions. This is due to the unique design of the reactors where a controlled depletion of the gas phase is used. This is caused by the geometry of the reactor where the gas is flowing radially from the center to the exhaust while the substrates perform a double rotation. Furthermore, this leads to extremely uniform wafer surface temperatures leading to very homogeneous doping.

Wednesday, May 28

10.30 - 12.30 Session 8: Technology

- 10.30 1. (Invited Paper) *L.F. Eastman, G. Martin, B. Pereiaslavets, M. Seaford, K. Chu, Cornell University:*
"Optimization of Pseudomorphic MODFETs with Arbitrary Lattice Constants".
- 11.00 2. *A. Vogt, H.L. Hartnagel, M. Rodewald, H. Füss, P. Ressel, K. Vogel, J. Würfl:*
"Pd-based Ohmic Contacts to GaSb".
3. *L. Cattani, M. Borgarino, J. Tasselli and A. Marty:*
"Minimum detectable outdiffusion length measurement for Be-doped AlGaAs/GaAs HBT".
4. *D.W. Davies, D.V. Morgan and H. Thomas:*
"Characterisation of indium based ohmic contacts to GaAs using an ion-assisted deposition technique".
5. *M. Chahoud, H.-H. Wehmann and A. Schlachetzki:*
"Anisotropic-etching simulation of InP".
6. *F. Dillmann, A. Brennemann, H. Hardtdegen, M. Marso, P. Kordos, H. Lüth and F.J. Tegude:*
"Novel concept for an integrated photoreceiver based on selective GaAs-epitaxy".
7. *Fedir V. Motsnyi:*
"Using of polariton and impurity photoluminescence for diagnostics of GaAs semiinsulating substrates and structures on its base for transistor devices".

Optimization of Pseudomorphic MODFET's with Arbitrary Lattice Constants

Lester F. Eastman, Glenn Martin, Boris Pereiaslavets,
Matthew Seaford and Kenneth Chu

School of Electrical Engineering and National Nanofabrication Facility
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The optimization of MODFET's based on GaAs, InP, and GaN are included. In addition to low-dislocation, strained (pseudomorphic) structures, use of the novel Compliant Universal (C.U.) substrate [1] will be presented. In all cases, the use of an appropriately thin quantum well will be emphasized, to limit the 2DEG to the ground state, thus avoiding the extra scattering effects of excited-state electrons. Optimum spacer layer thicknesses, in the range of 30-50Å, will be presented for room temperature operation. Strain compensation of barriers and channels, for larger 2DEG densities and for reliability, will be covered. The GaAs-based structures are InGaP/InGaAs/InGaP/GaAs, and the InP-based structures are InAlAs/InGaAs/InAlAs/InP. The AlGaIn/GaN structures are presently grown on Sapphire or SiC, although C.U. substrates or bulk GaN or AlN will be studied in the future. The 2DEG density values are $3 \times 10^{12}/\text{cm}^2$ in GaAs-based structures, $8 \times 10^{12}/\text{cm}^2$ in InP-based structures, and $\geq 1 \times 10^{13}/\text{cm}^2$ in GaN-based structures. MODFET's with $< .25 \mu\text{m}$ gate lengths have yielded f_{max} values of 250 GHz, 330 GHz, and 103 GHz respectively for the GaAs, InP, and GaN devices. Using the GaAs C.U. substrate, with a lattice constant of $\sim 5.95\text{\AA}$, it is predicted that an InAlAs/InAs/InAlAs MODFET will have an $f_{\text{max}} > 1\text{THz}$. The electron mobility and effective transit velocity, both dependent on the lattice constant, will be enhanced, while the barrier for the 2DEG confinement will be adequate.

[1] Applied Physics Letters, 70 (13) 1685-1687 (March 31, 1997).

Pd-based Ohmic Contacts to GaSb

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Abstract

In the last years the contact technology to GaSb has attracted some interest. The antimonides offer a tremendous variety of possible applications both in microwave electronics and optoelectronics.

Previously, ohmic contacts to GaSb were mainly gold-based and they often included a volatile dopant, e. g. zinc for p-type GaSb and tellurium and sulphur for n-type GaSb. Au shows a strong diffusion into GaSb [1] whereas these dopants are also known for their tendency to be unstable.

We have shown that Pd-based ohmic contacts and Ge as a donor could be an alternative [2], but the obtained specific contact resistivities were not sufficient for microwave applications. Thus, we followed two strategies to improve the performance of the ohmic contacts. On the one hand, we added a small amount of Au to our PdGe-contacts to promote the creation of an Au-Ga phase, so that Ge could take over the lattice sites of Ga. On the other hand, we went back to the volatile but efficient dopants Te and Se but now they were implanted, so that the disadvantage of the contamination of the evaporation system could be avoided. In addition, we wanted the dopant to be in the first metal layer deposited on the semiconductor.

The contacts on n-type GaSb were made on substrates while the contacts on p-type GaSb were deposited on molecular beam epitaxy grown layers on semiinsulating GaAs substrates. Measuring transmission line structures lead to the determination of the specific contact resistivity. Apart from the evaporation of metallizations, the dopants tellurium and selenium were implanted with varying the implantation energy and the dose.

The measured specific contact resistivities for non-alloyed PdAu contacts on p-type GaSb were between $9 \times 10^{-6} \Omega\text{cm}^2$ and $3 \times 10^{-6} \Omega\text{cm}^2$. Alloying the contacts in a rapid thermal annealing oven (RTA) for 1 min at different temperatures from 200 °C to 400 °C did

not improve the contact. Test ohmic contacts with Au and TiAu as metallizations gave similar results.

The PdGeAu contacts on n-type GaSb gave a specific contact resistivity of $1 \times 10^{-5} \Omega\text{cm}^2$ after alloying at 350 °C for 1 min in a RTA. This compares favourably with other reported results. PtAu overlayers were used. The ratio of the thicknesses of the Pd, Ge and Au is critical. For PdGeAu the sequence 8.7 nm/56 nm/23.3 nm was found to be optimal.

The implanted ohmic contacts gave only ohmic behaviour for low implantation energies. This can be explained by the swelling effect of GaSb after irradiation with ions [3]. The implantation energies were too high and the radiation damage under the metallization too severe. But an implantation energy of 10 keV and a dose of $1 \times 10^{15} \text{ cm}^{-2}$ of tellurium lead to a specific contact resistivity of $6 \times 10^{-5} \Omega\text{cm}^2$ after alloying at 300 °C for 30 s in a RTA. The metallization consisted of PdAuPtAu with the sequence 10 nm/11 nm/50 nm/100 nm. Selenium did not give ohmic behaviour.

In conclusion we have shown that non-alloyed PdAu ohmic contacts which give as low specific contact resistivities as gold-based contacts. PdGeAu metallizations on n-type GaSb lead to lower specific contact resistivities than PdGe contacts without Au and they are as low as gold-based contacts on n-type GaSb. Te-implanted ohmic contacts on n-type GaSb are only ohmic for low implantation energies.

References

- [1] A. Piotrowska et al., Acta Phys. Pol. A 87, 419 (1995).
- [2] A. Vogt et al., J. Vac. Sci. Technol. B 14 (6), 3514 (1996).
- [3] R. Callec et al., Appl. Phys. Lett. 59 (15), 1872 (1991).

MINIMUM DETECTABLE OUTDIFFUSION LENGTH MEASUREMENT FOR Be-DOPED AlGaAs/GaAs HBT.

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Recent reports [1, 2] show that beryllium is a widely used base dopant for HBTs. By designing a beryllium doped HBT, it should be taken into account that the most serious concern for the device stability is the diffusion of the doping impurities from the base into the emitter layer.

Some parameters allow to characterize the effects of the base dopant outdiffusion, such as threshold voltage [3] and inverted collector ratio R [4, 5]. By means of this ratio, the quantity named *minimum detectable outdiffusion length* $L_{min-diff}$ can be defined [5]. This length gives indications on the device susceptibility to the base dopant outdiffusion and therefore it may be used to design the epitaxial structure of a HBT. Although this length was theoretically introduced in [5] it was never experimentally measured. This work suggests a technique, which allows an experimental evaluation of $L_{min-diff}$.

We have current stressed triple mesa, Be-doped AlGaAs Single Heterojunction Bipolar Transistor (SHBT); Fig. 1 shows the epitaxial structure of the devices. During the stress the devices were operating in the forward active region, with a stress emitter current density of about $10^4 A/cm^2$. The stress temperature was about $-20^\circ C$, in order to inhibit the thermally activated mechanisms. We have recorded, up to 28 hours, the variations of the threshold voltage V_{BEth} , of the offset voltage V_{CE0} and of the inverted collector current ratio R ; in particular, Fig. 2 depicts the behaviour of R . All these data confirm that the degradation mechanism is a base dopant outdiffusion towards the emitter.

We simulated the beryllium outdiffusion by means of numerical techniques, as reported in a previous work [6]. After each stress step, the collector current was fitted and then the obtained outdiffusion length L_{diff} was correlated with the corresponding R value on a L_{diff} - R plane (see Fig. 3). The experimental points obtained from different devices show a similar behaviour, in agreement with the hypothesis that the same degradation mechanism affects all the devices. By approximating this curve with two straight lines (Fig. 3), we can identify a critical value of L_{diff} . Below this value we can't detect any noticeable variation of the ratio R : this critical value is the definition of $L_{min-diff}$ given in [5]. The value of about 10nm is in fairly good agreement with the theoretical value of about 13nm, which can be evaluated from the work of Chang [5], for the HBT structure reported in Fig. 1.

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- [5] Y.Chang et al. *Solid-St. Electron.*, **37**, 1413 (1994)
- [6] M.Borgarino et al. *Solid-St. Electron.*, **39**, 1305 (1996)

PROFILE	Aluminium Mole Fraction	Thickness [nm]	Dopant	Concentration [cm ⁻³]
N+ GaAs Cap Layer	0.00	300	Si	4.0x10 ¹⁸
N+ AlGaAs	0.28-0.00	50	Si	1.2x10 ¹⁸
N AlGaAs	0.28	200	Si	5.0x10 ¹⁷
N AlGaAs	0.00-0.28	50	Si	5.0x10 ¹⁷
P+ GaAs	0.00	90	Be	5.0x10 ¹⁹
N- GaAs	0.00	1000	Si	1.7x10 ¹⁶
N+ GaAs	0.00	1000	Si	4.0x10 ¹⁸
Semi-insulating GaAs Substrate				

Figure 1: Epitaxial structure of the stressed SHBT.

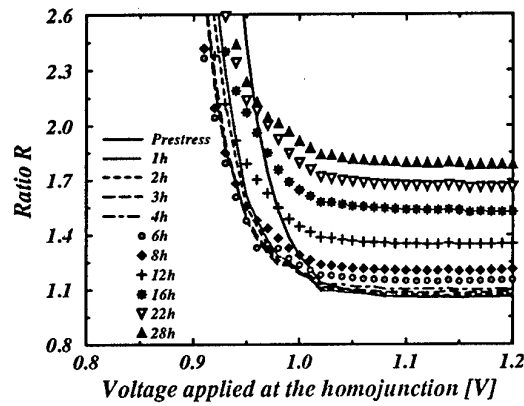


Figure 2: Impact of the stress on ratio R. Stress conditions: $J_C = 1 \cdot 10^4 A/cm^2$ and $V_{CE} = 1.50V$, $T = -20^\circ C$.

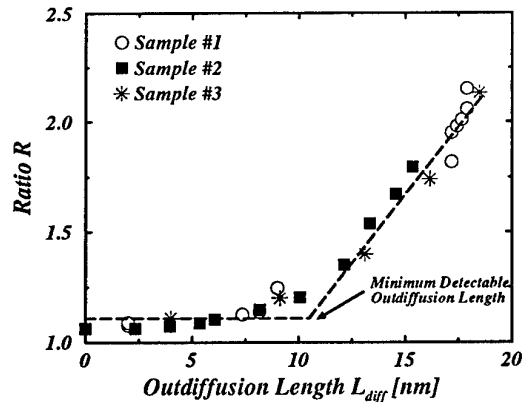


Figure 3: Correlation between the outdiffusion length L_{diff} and the ratio R: determination of the minimum detectable outdiffusion length $L_{diff-min}$.

Characterisation of indium based ohmic contacts to GaAs using an ion-assisted deposition technique

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The technique of ion assisted deposition (IAD) involves the simultaneous evaporation and ionisation of a source material during deposition. The ionised fractions are accelerated to 1keV and implanted into the semiconductor surface, resulting in premixing the metallisation in the near surface region during deposition. Previous work [1] has shown specific contact resistances (ρ_c) an order of magnitude lower for ion assisted AuGe contacts compared to conventionally evaporated contacts to n-GaAs after annealing. The technique has been extended to In/GaAs with the view to producing a graded interfacial layer of InGaAs and hence good ohmic behaviour. Depositing indium tin oxide (ITO) over the indium interfacial layer would lead the way to an improved transparent ITO contact technology. The high conductivity of ITO has been shown to provide an excellent spreading layer for LED devices [2].

Two material structures have been used in this study. (i) For the I-V measurements the structure shown in figure 1a was used. Indium dot contacts were defined using a metal shadow mask of area $3.8 \times 10^{-3} \text{cm}^2$ onto lightly doped ($N_d = 2 \times 10^{16} \text{cm}^{-3}$) n-type GaAs, grown epitaxially by molecular beam epitaxy (MBE) onto a highly doped n^+ substrate. The back contact was a conventional Au/Ni/AuGe ohmic contact. Characteristics were obtained for conventionally evaporated indium and ion mixed samples of 1keV ion energy of varying doses (low= $1.3 \times 10^{15} \text{ions/cm}^2$, med.= $2.8 \times 10^{15} \text{ions/cm}^2$, high= $4.7 \times 10^{15} \text{ions/cm}^2$). (ii) TLM measurements were carried out using the structure shown in figure 1b. This consists of a $2 \mu\text{m}$ n^+ GaAs layer (Si doped to $2 \times 10^{18} \text{cm}^{-3}$), grown epitaxially on a semi-insulating GaAs substrate.

The as-deposited characteristics are shown in figure 2. From the forward bias I-V curve a barrier height of 0.67eV and an ideality factor of 1.17 was calculated for the conventionally evaporated sample. A barrier height could not be obtained from the ion

mixed characteristics since they are dominated by a highly resistive region probably caused by ion damage at the metal-semiconductor interface. Annealing of the contacts removed the ion damage and intermixing of the In/GaAs resulted in a graded junction [3] and hence ohmic behaviour for temperatures in excess of 320°C. Using this information the TLM contacts were annealed for one minute at various temperatures between 320°C and 475°C. The results are summarised in figure3, the ion mixed samples have a lower minimum specific contact resistance ($3 \times 10^{-6} \Omega \text{cm}^2$ after annealing for 1 minute at 375°C compared to $6.2 \times 10^{-6} \Omega \text{cm}^2$ after annealing for 1 minute at 400°C for the conventional samples).

Acknowledgements

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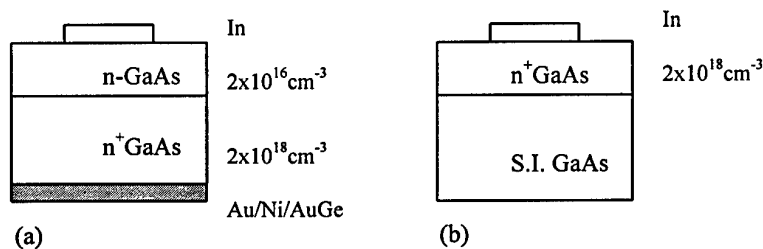


Figure 1: Sample structures used for (a) I-V measurements and (b) specific contact resistance measurements

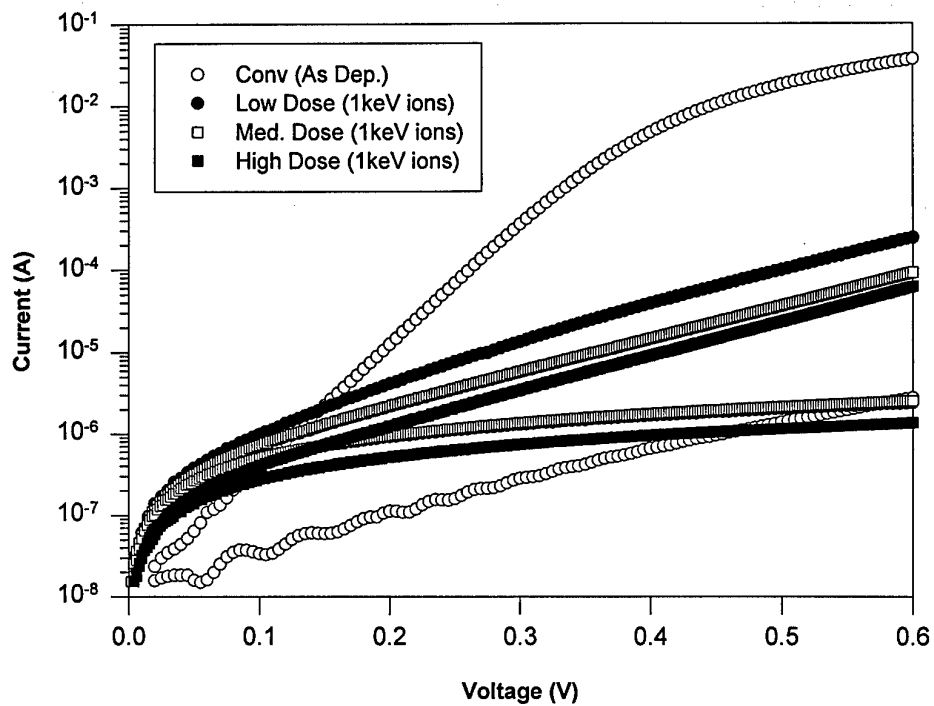


Figure 2: The as-deposited I-V characteristics for ion mixed and conventionally evaporated indium onto n-GaAs

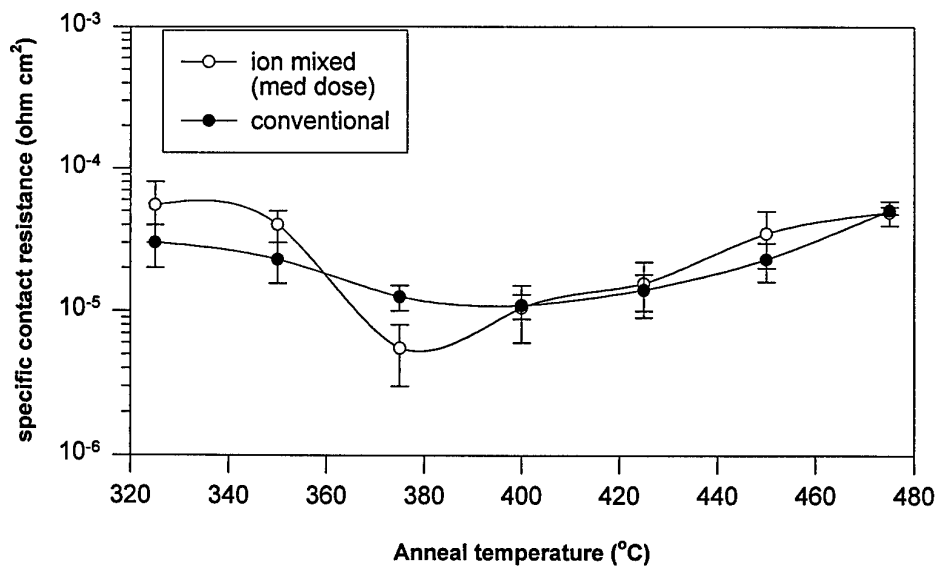


Figure 3: Specific contact resistance plot for conventionally evaporated indium and med. dose 1keV ion mixed indium after annealing for 1 min.

Anisotropic-etching simulation of InP

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Anisotropic etching is a widely used process in semiconductor-based micromechanics and microelectronics. Because of its dependence on many factors like etching time, structure of the mask, and orientation-dependent etching rates the prediction of the etching result is sometimes very difficult. Therefore, an etching-simulation program is very useful in order to minimize the technological expenditure. In principle the etching behaviour at concave patterns differs largely from that of convex structures. In the first case the slowest etching planes are decisive for the resulting pattern whereas in the second case the fastest etching planes determine the shape of the resulting structure. This is in contrast to the growth behaviour where with convex structures the slowest-growing planes and at concave corners the fastest-growing planes determine the final shape. This equivalence was exploited in our simulation program.

In this model the semiconductor is represented by cells of a cubic-primitive lattice thus allowing the simulation of diamond or zinkblende structures. The basic assumptions of our simulation algorithm are as follows:

- a) The simulation is carried out stepwise (etching steps).
- b) Each cell of the semiconductor's surface is considered under the aspect whether it belongs to a certain crystallographic plane or not, i. e. whether its neighbours in this plane are present or not.
- c) Depending on the experimentally found differences in the etching rates certain crystallographic planes are immune against the etching attack for a given fraction of an etching sequence and others are not. A cell that is in contact with the etching solution and that belongs to an immune plane remains in the solid.
- d) If a cell does not belong to any of the immune planes, it may belong to a convex structure. In that case the vicinity of this cell is inverted, i. e. all cells present are removed and all empty sites of the lattice are filled with cells. Thus we obtain a concave corner. According to the equivalence of growth and etching at this inverted structure growth steps are performed as prescribed by the respective etching rates. Subsequently the structure is inverted back to the originally convex shape.
- e) Cells, which do not belong to at least one of the considered planes neither in the normal nor in the inverted structure, are removed in every second step.

- f) Identical etching steps should be evenly distributed within a complete etching sequence.

We applied our model to InP etched by HBr. In order to determine the relevant etching rates we etched through a waggon-wheel mask. From the resulting etching figure we were able to identify the crystallographic directions in which the etching rate shows maxima and minima. In a second experiment we used a mask with stripes along these directions. At the cleavage planes we identified the crystallographic planes and the respective etching rates.

Finally we compare our simulations with experiments and found a very good agreement for purely concave structures, like the waggon-wheel of Fig. 1 which is almost identical to the etched figure and the example of Fig. 2 where a circular mask is used. A sufficient agreement for convex and mixed concave-convex structures was found, although we only take into account low indexed crystallographic planes.

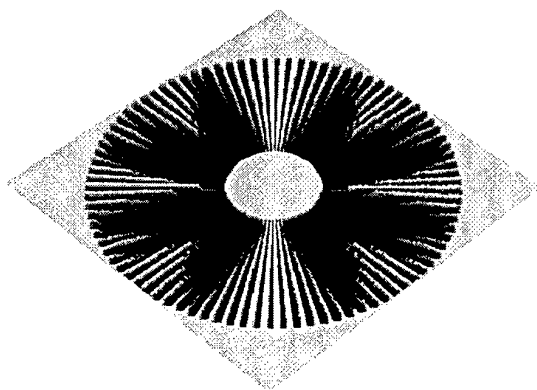


Fig. 1: Simulated waggon-wheel structure of InP in HBr.

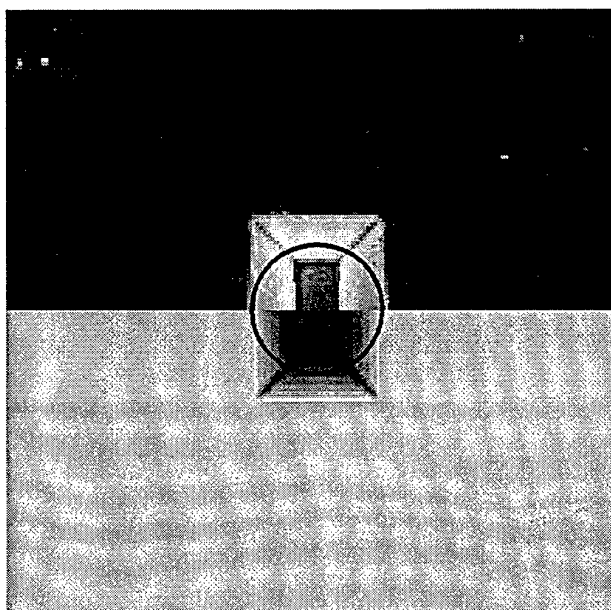


Fig. 2: Etch pit in InP through a circular mask (solid line); upper half experiment, lower half simulation.

Novel concept for an integrated photoreceiver based on selective GaAs-epitaxy

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Abstract

A novel concept for an optoelectronic front-end-receiver has been developed. For the first time, a pin-photodiode is integrated with a vertical JFET, a so called Permeable Junction Base Transistor (PJBT). Both devices are fabricated using the same layer structure. We present results of the single devices, prepared on the same sample, and first measurements of the integrated photoreceivers at 0.85 μm wavelength.

Fig. 1 shows the concept of our integration. The same layer structure is used for both devices, it consists of a sequence of n-i-p⁺-i-n-doped GaAs, grown by MOVPE with N₂ as carrier gas [1]. The upper intrinsic layer is used as an absorption layer of the diode. The quasi metallic p⁺-layer ($p = 1 \times 10^{20} \text{ cm}^{-3}$) serves as a homoepitaxial gate of the PJBT, so controllably short gate lengths can be defined by epitaxy [2]. The advantage compared to conventional PBT concepts is, that a very clean interface between the gate and the conducting channel is achieved. Using optical lithography and anisotropic Reactive Ion Etching (RIE) with a SiO₂-layer as an etching mask, channels with vertical sidewalls are etched in the GaAs to fabricate the transistor. The minimum channel width is about 0.7 μm . After thermal annealing and several cleaning steps (to remove RIE-damages and contaminations) a second, selective epitaxy is used for the n-doped (about $1 \times 10^{16} \text{ cm}^{-3}$) channels. Further fabrication steps are several metallizations and mesa etchings. The photodiode is contacted to the transistor using air bridge technology. At last, a Si₃N₄ antireflecting-coating is deposited.

First results show transconductances of the PJBT of more than 100mS/mm and a f_{max} of more than 2 GHz. Calculations show, that frequencies above 10 GHz are realistic by reducing parasitic capacitances and by using e-beam lithography to achieve shorter channel widths, making this concept useful for 10Gbit/s receiver systems. The photodiodes with an antireflecting coating have responsivities of 0.17 A/W and quantum efficiencies of 24 % at a wavelength of 0.85 μm . Fig. 2 shows a comparison of

the photocurrent of the single diode and the integrated receiver. The first realized receivers have responsivities of 8.0 A/W.

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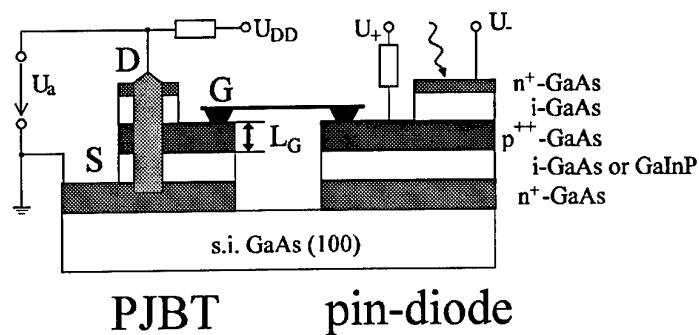


Fig. 1: Concept of the integration of a PJBT and a pin-diode

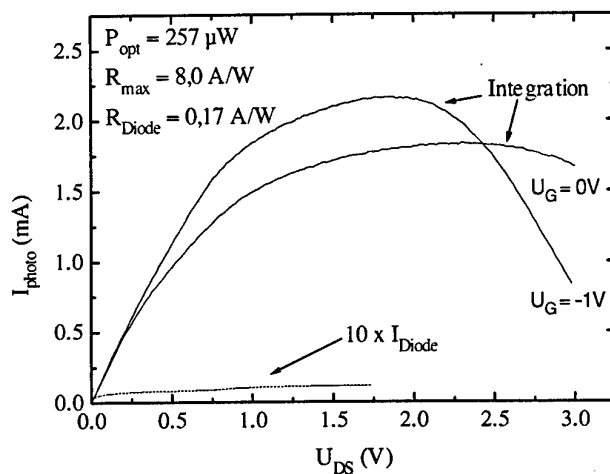


Fig. 2: Comparison of the photocurrent of the diode and the integrated receiver at $\lambda = 0.85\mu\text{m}$

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Using of polariton and impurity photoluminescence for diagnostics of GaAs semiinsulating substrates and structures on its base for transistor devices

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Photoluminescence (PL) method is one of the most simple, accessible, sensitive, express and non-destructive method of quality control of semiconductor materials. In this review report the expedience of using the PL method in GaAs semiconductor device technology has been demonstrated with example of author's works [1-2]. The following questions are considered:

1. Peculiarities of PL method.
2. Background impurities and other defects.
3. PL criteria of choice of the most perfect semiconductor substrates.
4. Influence of technological regimes Si^+ -ion implantation, thermic and pulse photon annealing on semiinsulating material quality.
5. Determination of PL characteristics in presence of which FET on base MBE $i\text{-n}^+\text{-n-n}^+$ GaAs structures cannot be made.
6. Influence of the growth conditions on the quality of $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ substrates with 2D electron gas.
7. Fluctuation of single quantum wells width along layers at traditional and non-traditional growth of $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ by MOC method.
8. Influence of barrier layers on the quantum well quality.

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