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6. AUTHOR(S) William C.B. Peatman, President				
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13. ABSTRACT (Maximum 200 words) There is an accelerating need for electronic devices and integrated circuits which operate at extremely high temperatures. Increasingly, electronics are finding applications in measurement and control systems in automotive and jet engine environments, for example, where temperatures can easily exceed 150°C. Wide band gap materials have shown promise for high temperature applications, however, cost and reliability issues presently limit their widespread use. GaAs MESFETs have shown some promise at temperatures as high as 400°C, however, high gate leakage currents and degraded breakdown characteristics lead to poor reliability and large variations in device characteristics. Recently, a greater than tenfold reduction in the threshold voltage temperature coefficient was demonstrated in the heterodimensional MESFET compared with GaAs MESFET. Heterodimensional devices have also demonstrated excellent operation to high breakdown voltage. The goal of this project is to explore the feasibility of developing heterodimensional technology for high power and/or high temperature applications.				
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Final Progress Report
(ARO Contract DAAG55-97-C-0046)

1. List of Manuscripts:

Abstract to the National Radio Science Meeting, International Union of Radio Science (URSI), p. 193, Jan. 5-8, 1998.

2. Scientific Personnel supported by this project:

William C.B. Peatman, Ph.D
Michael S. Shur, Ph.D (subcontract to RPI).

3. Report of Inventions:

None.

4. Scientific Progress and Accomplishments:

- Visit of Peatman to RPI on Aug. 21-23, 1997 to review/set-up high temperature testing capability (no data taken).
- Visit of Peatman to RPI on Oct. 13-16, 1997 to perform first high temperature measurements on 2DI-MESFETs (see data attached).
- Visit of Peatman to Cornell Nanofabrication Facility on Nov. 3-5 to fabricate new 2-D MESFETs in collaboration with RPI personnel. Fabrication is ongoing (see photos). This effort has resulted in new recipes for electron beam lithographic definition and ohmic contact lift-off and interconnect lift-off. Equipment interruptions and facility closures at Cornell Nanofabrication Facility were encountered, however, these should be resolved shortly
- High temperature 2-D MESFET model was developed and implemented into the AIM-Spice code and is now available for modeling the high temperature properties of the 2-D MESFET (See data attached).
- Final report summarizing progress to date and plans for future research (this report).

5. Technology Transfer:

None.

6. Plans for 1998:

Design, fabricate and test high temperature 2-D MESFET devices (e.g. mixers, op-amps).
Refine and further validate the temperature model of the 2-D MESFET.
Perform fundamental studies of 2-D MESFETs including breakdown and noise properties.

Heterodimensional Technology for High Power, High Temperature Electronics

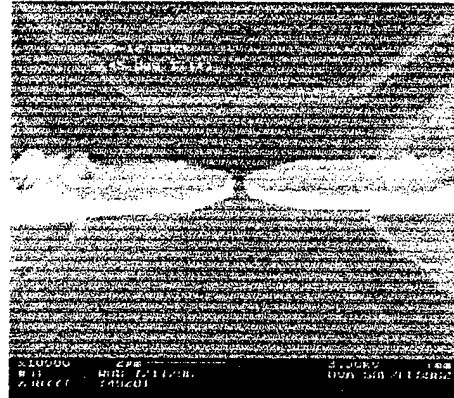
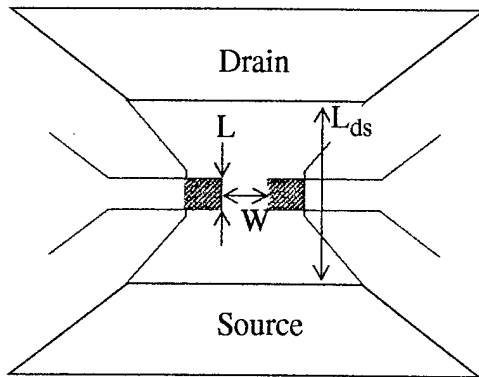
The Schottky junction between the 3-d metal and the 2-d electron gas is a fundamentally new contact of an important new class of semiconductor devices called heterodimensional electronics. Due to the two dimensional spreading of the junction electric field, breakdown voltages as high as 50 V have been demonstrated [1]. The same property leads to higher electrostatic damage immunity. Because the conducting channel is sandwiched between two wider band gap layers, the Schottky barrier is larger than in bulk (homo) Schottky junctions. Note that the channel is degenerately doped (as in conventional HFETs), however, the charge control is achieved by changing the *width* of the conducting channel, rather than the conductivity, as in the HFET [2]. This means the conducting channel remains degenerately doped until pinch-off. This situation is quite different from the case of either the conventional MESFET or HFET in which the gate modulates the channel *charge density*. The heterodimensional 2-D MESFET has unique charge control properties (due to the gate/2-DEG geometry) which have been shown to offer advantages for low power electronics [3].

An important advantage of GaAs technology is its ability to operate in a wide temperature range. The large band gap of GaAs allows GaAs based ICs to operate at temperatures considerably higher than those for silicon based technology (see for example [4], [5]). However, characteristics of conventional MESFETs, particularly the threshold voltage and the low-field mobility, depend strongly on the operating temperature [6], [7]. These temperature effects have to be taken into account when designing GaAs MESFET integrated circuits and therefore impose additional burdens on the designer. Recently, we demonstrated that the heterodimensional 2-D MESFET exhibits much weaker temperature dependence of current-voltage characteristics compared to conventional MESFET technologies [8]. Drain current measurements performed at different temperatures illustrate that our devices have smaller threshold voltage variations and mobility degradation compared to conventional MESFET structures. A least square fit to the extracted threshold voltage values gives a temperature sensitivity of 0.086 mV/K. In a conventional MESFET the threshold voltage V_T changes with the temperature T according to $V_T = V_{T0} - K(T - T_0)$ where $K \sim 1.4$ mV/K [7]. The Fermi level shift contributes only about 25% of the total shift in V_T . The much smaller temperature dependence of the 2-D MESFET threshold voltage will simplify circuit design and may also lead to a greater integration scale for low power digital ICs.

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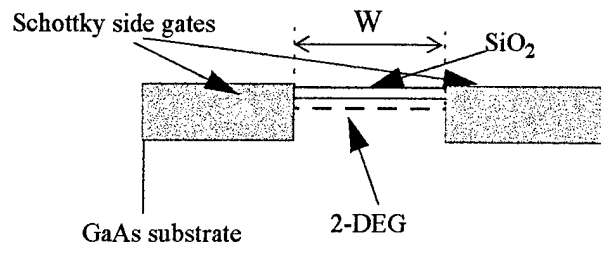
top view:



cross section through gates:

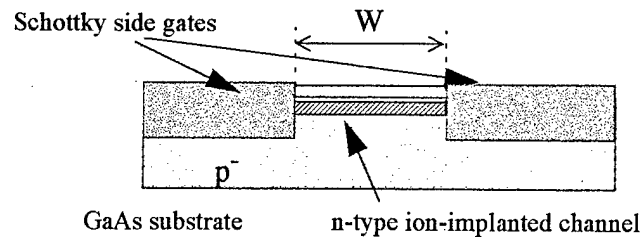
2-D MESFET

- AlGaAs/InGaAs/GaAs heterostructure
- 2-DEG channel
- electroplated Pt/Au gates



2-DI MESFET

- bulk n-GaAs material
- implanted Si channel
- electroplated Pt/Au gates



2-D JFET

- bulk n-GaAs material
- implanted Si channel
- implanted p+ gates

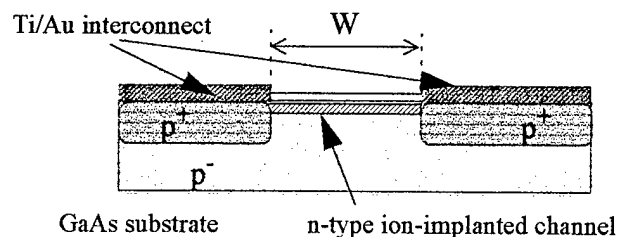


Fig. 1. (a) Illustration of the top view of a 2-D MESFET and SEM image of corresponding view, and (b) cross section of 2-D MESFET, 2-DI MESFET, and 2-D JFET showing evolution toward more manufacturable process.

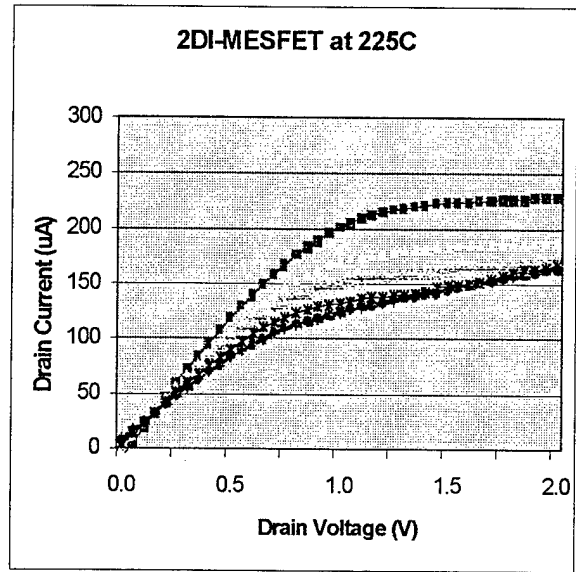
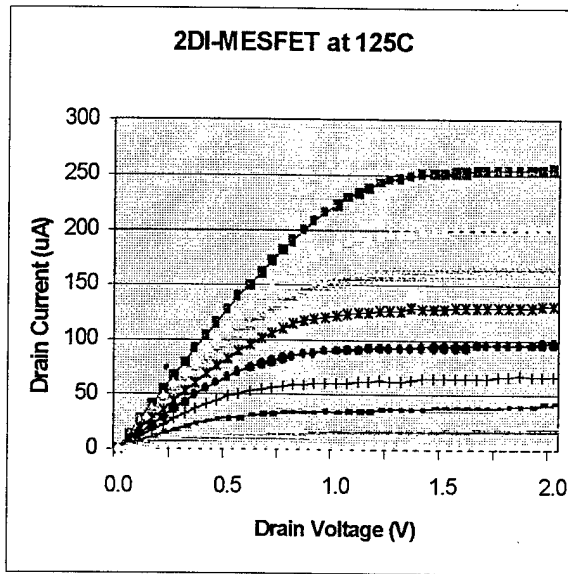
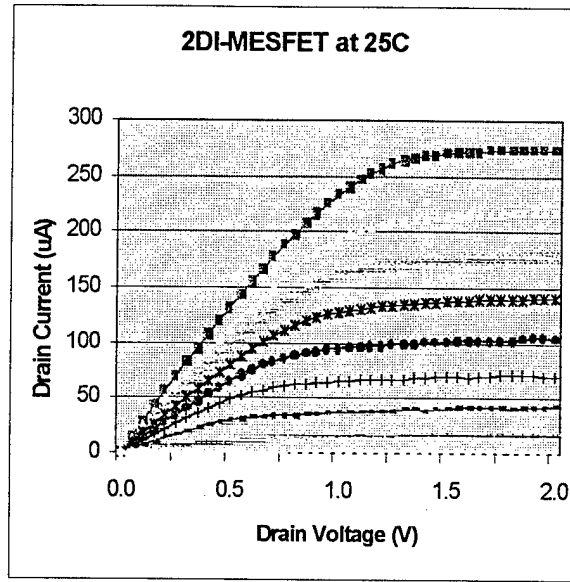
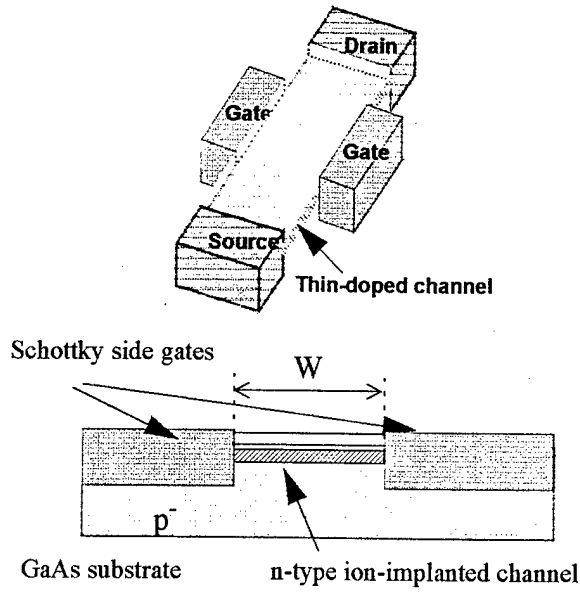


Fig. 2. Schematics (top left) and I_D - V_{DS} characteristics of 2-DI-MESFET (ion-implanted channel 2-D MESFET). Preliminary high temperature characteristics indicate that the Schottky/ion-implanted channel junction leakage current limits the output characteristics at above about 150°C. Note, the gate leakage current reached the compliance value of 5 μA , thereby limiting further drain current modulation at 225°C. Good high temperature operation will require a high temperature-stable Schottky metallization.

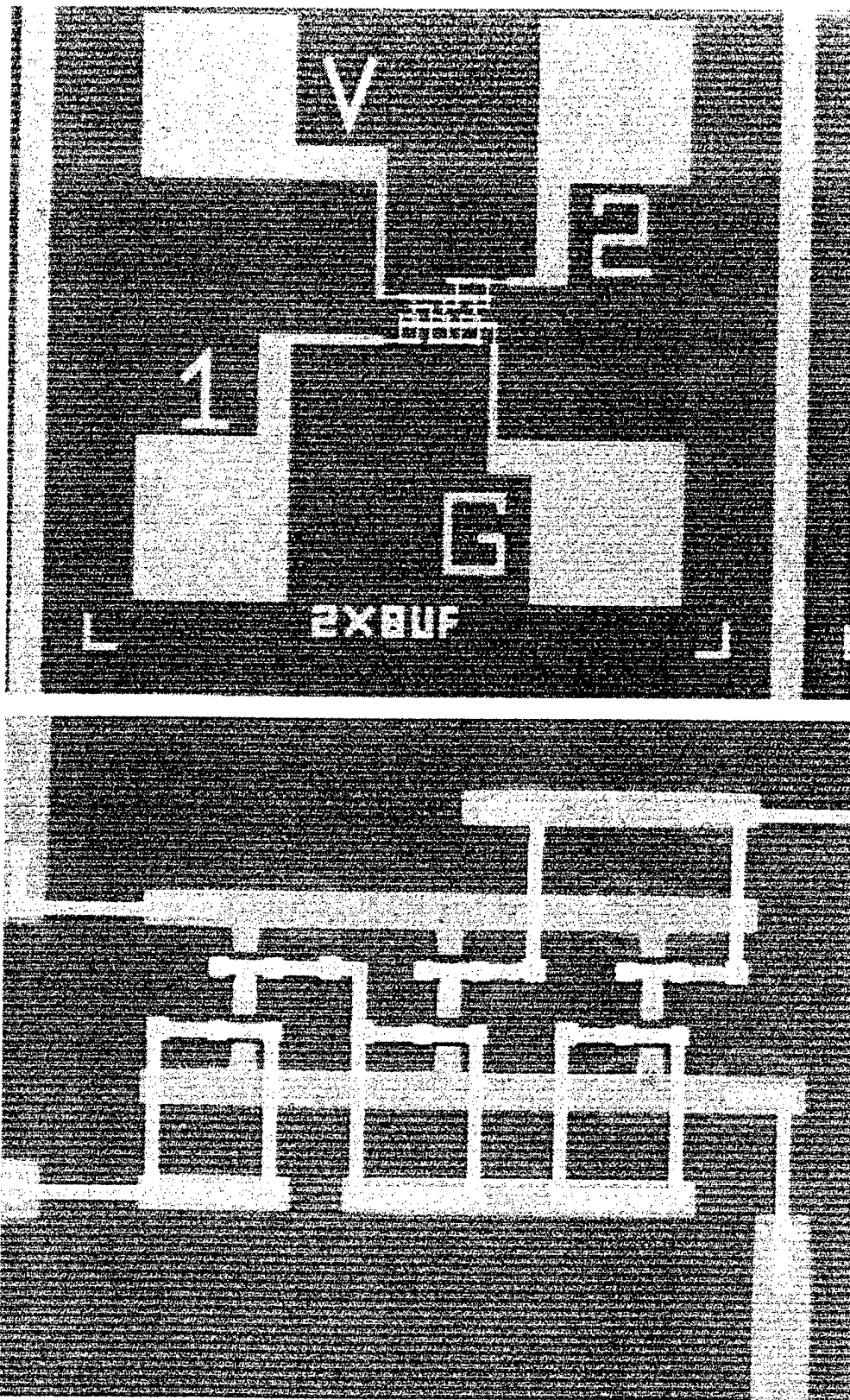


Figure 3. Layout of 2-D MESFET DCFL buffer circuit showing contact scheme (top) and individual gates (below). The minimum interconnect widths are nominally 1.5 micron.

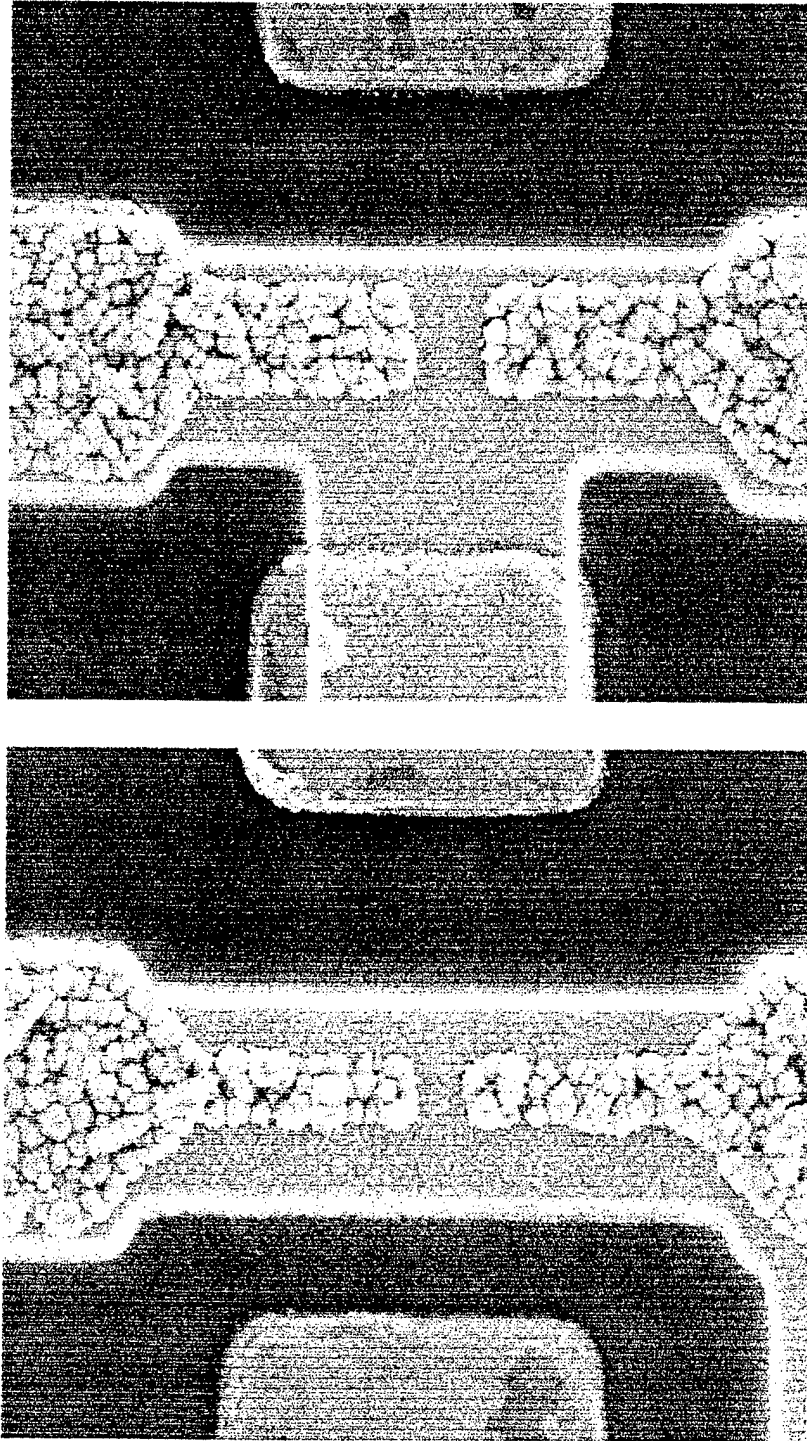


Figure 4. Close-up views of D-mode (top) and E-mode (bottom) gates having channel dimensions ($L \times W$ where W is the gate-gate spacing) of 0.6×0.45 and 0.3×0.3 micrometer respectively. The interconnect metal overlays each device, joining both inputs electrically (the interconnect above the channel is separated from the channel by about 120 nm of SiO_2).

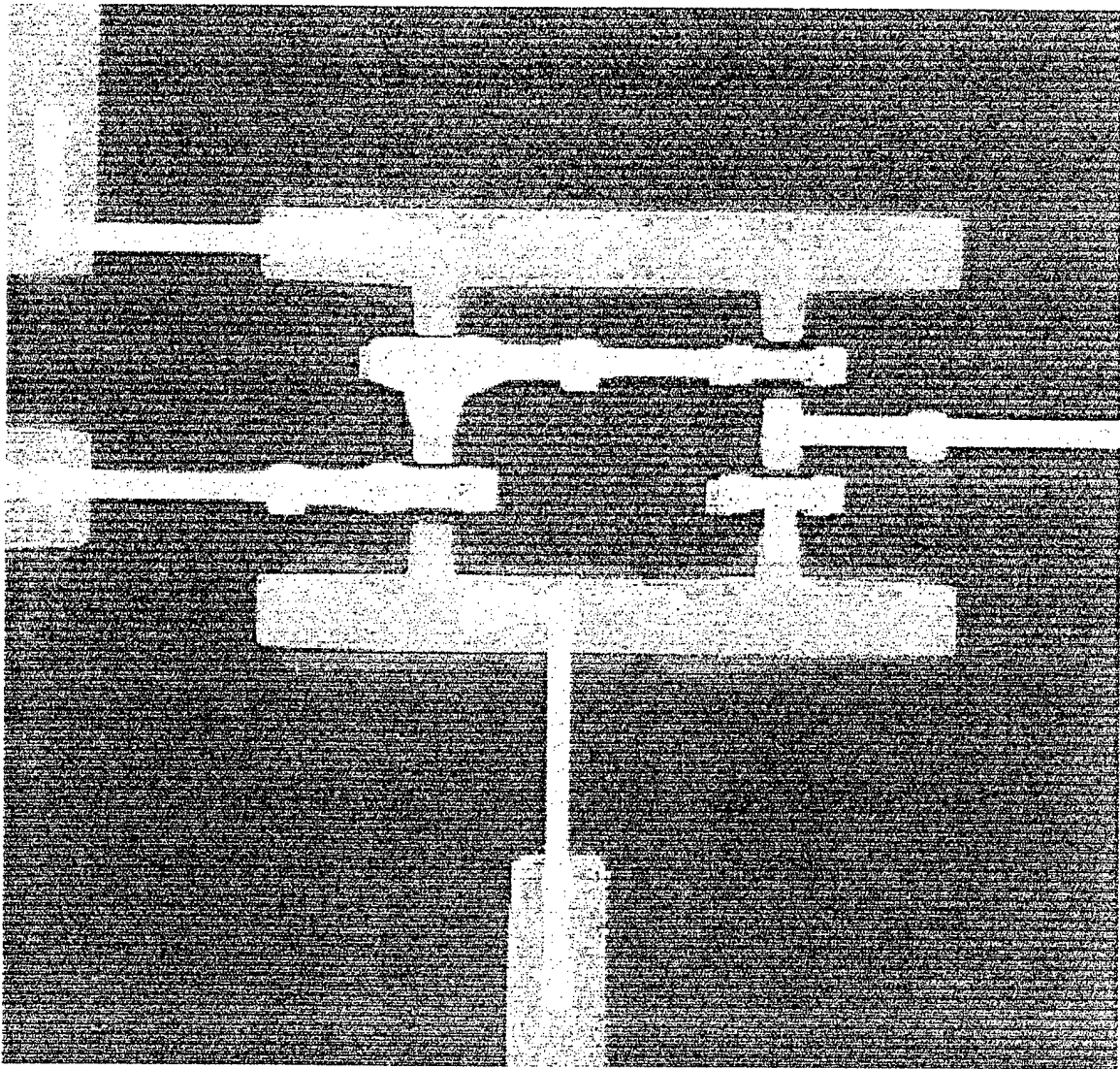


Figure 5. Scanning electron microscope image of a DCFL 2-D MESFET buffer circuit.

Model of the Temperature-Dependence of the 2-D-MESFET

Benjamín Iñíguez, Jianqiang Lü , Michael Shur and William Peatman

1) Abstract

We report the temperature dependence of the parameters of the new physically-based model for the 2-D MESFETs. The model is valid for many different configurations, including a "single" gate in which the sidewall contacts are biased together, a dual gate configuration in which the gates are biased independently, and a multiple gate configuration for 3 or more side gates. The model, which has been implemented in the circuit simulator AIM- Spice, is suitable for circuit simulation and accurate in all regimes of operation.

2) MODEL

The drain current of the unified 2-D MESFET is given by the expression:

$$I_{ds} = \frac{g_{ch} V_{ds} (1 + \lambda V_{ds})}{\left[1 + (V_{ds} g_{ch} / I_{sate})^m\right]^{1/m}}, \quad (1)$$

where V_{ds} is the drain-source voltage, I_{sate} is a unified expression of the saturation current, λ is the output conductance parameter, m is a knee-shape fitting parameter and g_{ch} is the extrinsic conductance given by:

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(R_s + R_d)}. \quad (2)$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(R_s + R_d)} \quad (2)$$

Here, $g_{chi} = qn_i\mu_n/L$, μ_n is the electron mobility and n_i is the electron sheet charge density per unit length given by:

$$n_i = \frac{n'_i}{[1 + (n'_i/n_{max})^\gamma]^{1/\gamma}} \quad (3)$$

where n_{max} is the maximum electron sheet density per unit length, γ is a fitting parameter and n'_i is given by an approximate solution of the unified charge control model [8]:

$$n'_i = \frac{2c_{eff}\eta V_{th}}{q} \log \left[1 + \frac{1}{2} \exp \left(\frac{V_{GS} - V_T}{\eta V_{th}} \right) \right] \quad (4)$$

Here, η is the subthreshold ideality factor, V_{th} is the thermal voltage and c_{eff} is considered as a capacitance fitting parameter.

The saturation current is written as [5, 6]:

$$I_{sat} = \frac{g_{chi} V_{gte} \varsigma}{(1 + t_c V_{gt}) \left(1 + g_{chi} R_s + \sqrt{1 + 2g_{chi} R_s + (V_{gte}/V_L)^2} \right)}, \quad (5)$$

where ς is the transconductance expansion factor, t_c is the transconductance compression factor, $V_L = F_s L$ with F_s being the saturation field.

The effective gate voltage swing, V_{gte} , is related to the gate-source voltage, V_{gs} , and the threshold voltage V_T as follows:

$$V_{gte} = V_{th} \left[1 + \frac{V_{GS} - V_T}{2\eta V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{GS} - V_T}{2\eta V_{th}} - 1 \right)^2} \right], \quad (6)$$

where the parameter δ determines the width of the transition between below and above threshold. Please note that (6) represents the equation used in [6] where we replaced V_{th} with ηV_{th} .

As explained in [7] the modulation of the effective channel length because of the lateral depletion regions strongly affects the characteristics of short-channel devices. The expression of the intrinsic channel conductance should be replaced by:

$$g_{chi} = \frac{qn_i\mu}{L + \alpha d_{dep}}, \quad (7)$$

where α is a fitting parameter and $d_{dep} = \frac{1}{2} \left(W_m - \frac{n_i}{n_s} \right)$.

The temperature dependence of the current model is introduced by the parameters V_{th} , V_T , μ , η and λ :

$$V_{th} = kT / q, \quad (8)$$

where k is the Boltzmann constant and T is the temperature.

$$V_T(T) = V_T(T_{nom}) - T_{vto} (T - T_{nom}), \quad (9)$$

where $V_T(T_{nom})$ is the threshold voltage at room temperature T_{nom} and T_{vto} is a fitting parameter.

$$\mu(T) = \frac{1}{1/\mu_{imp} + 1/\mu_{po}}, \quad (10)$$

where

$$\mu_{imp} = \mu_0 (T/T_\mu)^{xtmo}, \quad (11)$$

$$\mu_{po} = \mu_1 (T_\mu/T)^{xtm1} + \mu_2 (T_\mu/T)^{xtm2}, \quad (12)$$

μ_0 being a temperature-independent parameter that is identified with the introduced value of μ in an AIM-Spice file, and T_μ , μ_1 , μ_2 , $xtmo$, $xtm1$ and $xtm2$ fitting parameters. By default $\mu_1 = \mu_2 = 0$ and $xtmo = xtm1 = xtm2 = 0$, so we have to give values to these parameters in order to account for the temperature dependence of the model.

$$\eta(T) = \eta_0 \left(1 + \frac{T}{T_{\eta_0}} + \frac{T_{\eta_1}}{T} \right), \quad (13)$$

where η_0 is a temperature-independent parameter that is identified with the introduced value of η in an AIM-Spice file, and T_{η_0} and T_{η_1} are fitting parameters.

$$\lambda(T) = \lambda_0 \left(1 - \frac{T}{T_\lambda} \right), \quad (14)$$

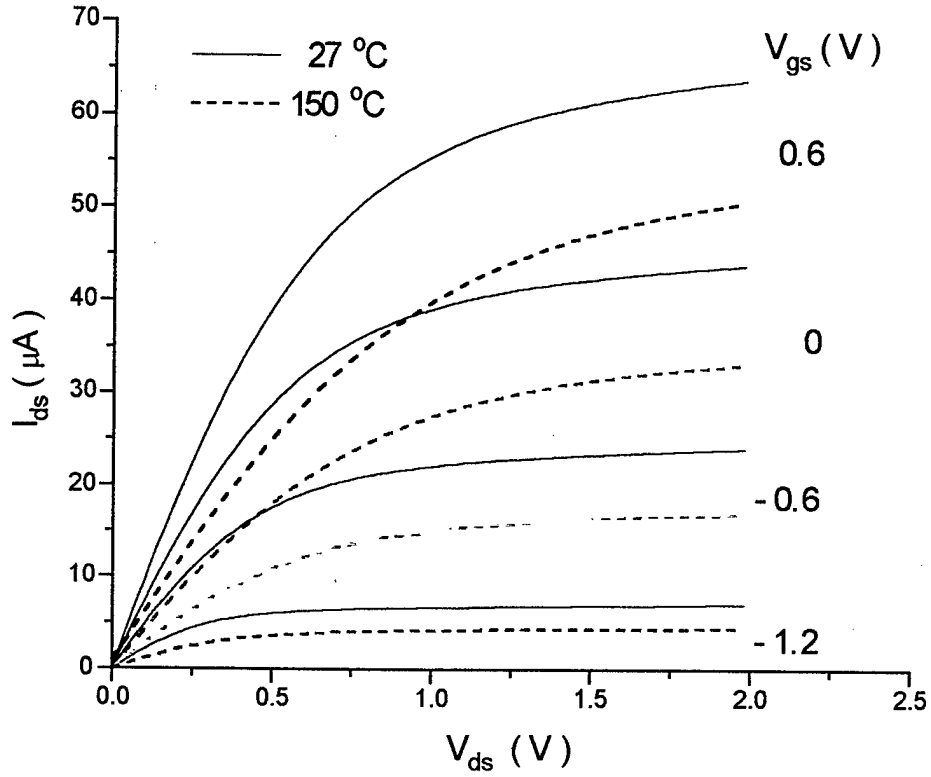
where η_0 is a temperature-independent parameter that is identified with the introduced value of λ in an AIM-Spice file T_λ is a fitting parameter.

If the sheet density, n_s , is not introduced explicitly in the AIM-Spice circuit, a temperature dependence of it is given by the Schottky barrier, $\Phi_B(T)$:

$$\Phi_B(T) = \Phi_B(T_{nom}) - \Phi_{B1}(T - T_{nom}), \quad (15)$$

$$n_s = 2\epsilon_s \frac{\Phi_B}{Wq^2}. \quad (16)$$

In the following figure, we show plots of drain current versus drain voltage at two different temperatures: 27 °C and 150 °C.



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