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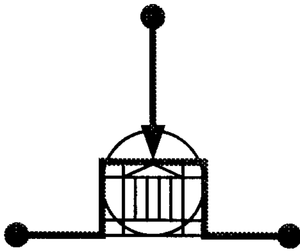

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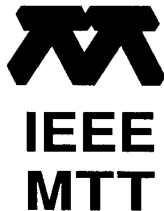

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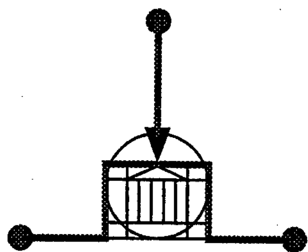

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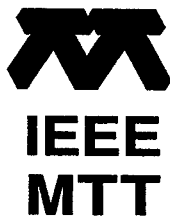

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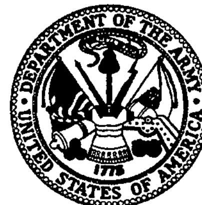

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Professor Aldert van der Ziel

(December 12, 1910 - January 20, 1991)

The van der Ziel Award, sponsored by Northrop Grumman, was established in honor of Professor Aldert van der Ziel for his long, distinguished and illustrious career as an educator and a research scientist. Past recipients of the Aldert van der Ziel Award include Arthur Milnes and Lester Eastman. The Aldert van der Ziel Award for 1997 will be presented to Professor Herbert Kroemer.

HERBERT KROEMER

Dr. Herbert Kroemer is the *Donald W. Whittier Professor of Electrical Engineering* at the University of California at Santa Barbara (UCSB), where he has been since 1976. He was born (1928) and educated in Germany. He received a Ph.D. in Physics (Solid State Theory) in 1952 from the University of Göttingen, Germany, with a dissertation on the theory of what would now be called *hot-electron effects* in the then-new transistor. Since then, he has worked on the physics and technology of semiconductors in a number of research laboratories in Germany and the U.S.:

1952-54 Fernmeldetechnisches Zentralamt (FTZ), Darmstadt, Germany
1954-57 RCA Laboratories, Princeton, NJ
1957-59 Philips Zentrallabor, Hamburg, Germany
1959-66 Varian Associates, Central Research Laboratory, Palo Alto, CA
1966-86 Fairchild R&D Laboratory, Palo Alto, CA
1968-76 EE Dept, University of Colorado, Boulder, CO

He is the originator of several important device physics concepts, starting with the drift-transistor concept (1953), soon followed by the first *heterostructure* concept, the heterostructure bipolar transistor concept (1957). His 1963 proposal of the double heterostructure laser, seven years ahead of technological realization, was an outgrowth of the transistor work. In 1964 he was the first to publish an explanation for the Gunn effect. In the late 70s, he was one of the first to apply the emerging new molecular beam epitaxy technology (MBE) successfully to new and unconventional materials combinations, such as GaP-on-Si and GaAs-on-Si structures, and to new or previously unattainable heterostructures, expanding quickly into quantum well and superlattice structures, and making several contributions to the development of MBE itself.

He is a Fellow of the IEEE and the APS. He was Chairman of the 1972 *International Symposium on GaAs and Related Compounds*, and of the 1974 *Device Research Conference.* Other professional honors include the following:

1973 *J.J. Ebers Award* of the IEEE
1982 *Senior Research Award* of the ASEE;
GaAs Symposium Award and *Heinrich Welker Medal* of the International Symposium on GaAs and Related Compounds
1984 *Honorary Doctorate of Engineering*, Technical University of Aachen, Germany
1986 Appointed *Donald W. Whittier Professor*;
Jack Morton Award of the IEEE
1997 *Foreign Associate*, National Academy of Engineering

His research interests continue to be in semiconductor heterostructures, ranging from their basic physics to their device utilization, with an emphasis on new kinds of quantum-effect structures, and on heterostructures between semiconductors and superconductors.

1997 INTERNATIONAL SEMICONDUCTOR DEVICE RESEARCH SYMPOSIUM

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ALDERT VAN DER ZIEL AWARD

YEAR	RECIPIENT	AFFILIATION
1997	Herbert Kroemer	University of California - Santa Barbara
1995	Lester F. Eastman	Cornell University
1993	Arthur G. Milnes	Carnegie Mellon University

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1995	Erno Klaassen	Stanford University
1993	Edgar Martinez	Wright Laboratory
	Kaushik Bhaumik	Cornell University
1991	R. Mickevičius	Wayne State University

Introduction

This volume contains the Proceedings of the Fourth International Semiconductor Device Research Symposium (ISDRS-97, Charlottesville,Virginia, December 10-13, 1997).

The goal of this international meeting is to provide a congenial forum for the exchange of information and new ideas for researchers from university, industry and government laboratories in the field of semiconductor devices and device physics. Our other goal is to make this conference truly international. To achieve this, the symposium has sub-committees in Asia, Europe, Japan and the former Soviet Union. This conference is organized in cooperation with the IEEE MTT Society, the United States National Committee of URSI and the Russian Physical Society.

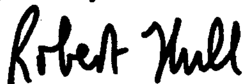
The program committee received submissions from 21 countries, representing four continents. Of the submitted papers, 80 have been selected for oral presentations and about 85 for poster presentations. These papers cover a broad range of topics, including novel and ultra-small devices, photonics and optoelectronics, heterostructure and cryogenic devices, wide band gap semiconductors, thin film transistors, MEMS, MOSFET technology and devices, carrier transport phenomena, materials and device characterization, simulation and modeling. It is hoped that such a broad range of topics will foster a cross-fertilization of the different fields related to semiconductor materials and devices.

In addition to the regular sessions, we are very pleased to offer two Special Symposia this year. These are "Organic and Polymeric Devices" and "Nanoscale and Quantum Confined Structures." The plenary session has three excellent talks by Professors Hasegawa of Hokkaido University and Fabian Pease of Stanford University, and Bernie Meyerson of IBM's TJ Watson Research Center.

The first ISDRS symposium in 1991 was dedicated to the memory of Professor Aldert van der Ziel who made seminal contribution to the theory of semiconductor devices, especially to the theory of noise, and who educated literally hundreds of graduate students. Past awardees include Arthur Milnes and Lester Eastman. We are pleased to announce that the 1997 award goes to Professor Herbert Kroemer of the University of California at Santa Barbara. Every year a Best Student Paper Award is chosen by the Organizing Committee at the close of the symposium from evaluations received from the participants. The 1995 Best Student Paper Award was Erno Klaassen of Stanford University, "Thermally Based Systems in CMOS Technology."

ISDRS-97 was made possible by the generous support of the Army Research Office and the Virginia Institute for Microelectronics. We are also grateful to many individuals, including the Special Symposia chairs and the session chairs, and the international Symposium Co-Chairs, and others whose contributions have made the Symposium a success. Special thanks to L. Tawney for her dedication and superlative contributions to the program, registration and administrative functions. Finally we thank the authors for their technical abstracts.

We hope that you find the symposium stimulating and that you will look forward to ISDRS-99.



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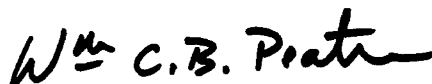

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Present Status and Future Directions of Quantum Electronic Device Research

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According to the "Roadmap" for Si LSI industry, the semiconductor fabrication technology will continue to progress in miniaturization from the present submicron range into the decananometer range early in the next century. In fact, production-level realization of the minimum feature size of 70 nm is targeted at the year of 2010, making the dimensions of scaled-down transistors comparable with the Fermi wavelength of electrons in semiconductors. However, how well such scaled-down devices based on semi-classical operation principle perform in the "quantum regime" still seems to be an open question.

Advance of the fabrication technology into the nanometer range, on the other hand, has opened up exciting possibilities of constructing novel electronic devices directly based on the quantum mechanics. In these devices, quantum mechanical wave-particle motions of individual electrons are controlled by artificial quantum structures such as quantum wells, quantum wires, quantum dots and single and multiple tunneling barriers so as to realize devices with new functions and higher performances. The purpose of the present paper is to discuss the present status and future directions of research on the quantum devices.

Since electrons manifest either wave-nature or particle-nature predominantly depending on their environments, one can conceptually envisage two kinds of electronics in the quantum regime, i.e., "quantum wave electronics" and "single electronics". In the former, electrons are put into various phase-coherent structures and their wave properties are utilized to realize various new devices including quantum wire transistors, interference devices, Y-switches, couplers, resonant tunneling devices and superlattice devices. In the single electronics, on the other hand, electrons are put into "dot" structures and their particle-nature is emphasized, leading to single electron transistors, single electron memories, dot-based cellular automata etc. Previously, single electron devices were mostly based on the Coulomb blockade mechanism resulting from the classical charging energy. However, as the dot sizes are reduced for operation at higher temperatures, quantum effects will predominate particularly in semiconductors. Present status and critical issues of these quantum devices and their fabrication technologies are presented and discussed. Particularly, an emphasis is placed on the research of "quantum dot"-based non-classical single electron devices which are currently intensively studied by a Priority Area Research Project on "Single Electron Devices and Their High Density Integration" (April 1996 - March 2000) under the support from Ministry of Education, Science, Sports and Culture, Japan. In this project, intensive collaborative efforts toward future are being made to find ways through the vast open fields of the quantum regime where no "roadmaps" exist.

SiGe Technology

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Silicon Germanium (SiGe) based technology went "commercial" in September of 1996, with the manufacturing qualification of a SiGe-based heterojunction bipolar transistor technology at IBM's East Fishkill facilities. Although fabricated within a conventional CMOS production environment and toolset, the advantages of the SiGe heterostructure were maintained. One of the most interesting aspects of this exercise was the systematic parceling out of the performance benefits of the SiGe heterojunction among several key device parameters, a requirement to achieve the best overall system level results. This resulted in a 65/55Ghz process supporting 3.3/5.8 volt operation, with HBT yields supporting integration at or above 20,000 devices. SiGe BiCMOS technology supports accompanying FET integration levels exceeding 500,000 gates, enabling fundamentally new circuit architectures. This talk will review the fundamentals of SiGe technology, its transition from experiment to production, several early commercial applications, and will close with an overview of the technology roadmap for future SiGe based devices.

Semiconductor Electronics Off-the-Roadmap

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Two of the major issues on the current National Technology Roadmap for Semiconductors (NTRS) are (1) the introduction of wafers of diameter 12 inches and above, and (2) the patterning of devices at 180nm and below. There is a case to be made that by successfully addressing the patterning issue for feature sizes down to 25 nm, i.e. beyond the end of the roadmap, we will eliminate the second issue.

There are already demonstrations that field effect transistors with effective gate lengths of 25nm work. One of the key requirements is that the channel region be very thin; down to 10nm. Such a transistor needs a volume of single-crystal silicon of about 100 x 200 x 20 unit cells. This is smaller than the grain size in many polycrystalline silicon films and suggests that at this size it might be worth revisiting the issue of how to form single crystal silicon islands on amorphous substrates and eliminate the wafers altogether. Thin film transistors in annealed polysilicon on amorphous substrates have recently shown impressive mobility (e.g. 300cm2/(v-s) reported by Sigmon et al. 1997) and there exist ways of enhancing the formation of single crystal islands by treating the substrate by prior patterning (e.g. Smith et al. 1979), and by subsequent scanned radiation (e.g. Gibbons et al. 1978). Other potential techniques for enhancing single crystal island formation on substrates include special treatment during deposition.

Obviously if we can solve the problem of how to grow 100nm single crystal islands of silicon on amorphous substrates we can also form true three-dimensional arrays of active devices and this may well significantly alleviate the third major NTRS issue: interconnects.

GaAs SCHOTTKY DIODE TECHNOLOGY FOR SUBMILLIMETER WAVELENGTHS

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Abstract

GaAs Schottky barrier diodes continue to be heavily used in millimeter and submillimeter wavelength heterodyne receivers. This is because the diode technology is well known, reliable, and yields acceptable sensitivities at room temperature. The UVa Surface Channel technology has led to the development of planar diode mixers to near 1 THz and highly efficient planar multipliers to 320 GHz. Beyond these frequencies, whisker contacted diodes remain a viable technology.

This presentation will begin with a review of the status of GaAs Schottky diode technology at the University of Virginia. At this point, we believe that most of the important device issues have been identified and largely resolved. Thus, our major focus is being shifted to circuit level considerations. Recent systems results will be summarized, including work on planar diode mixers and multipliers. These planar systems are beginning to yield higher levels of fixed-tuned bandwidth and, in some cases, better performance than was achieved with whiskered diodes. Finally, we will look to the future which should include Submillimeter-wave Monolithic Integrated Circuits (SMICs) and the fabrication of inexpensive waveguide structures for submillimeter wavelengths. The success of SMICs will rely not only on advanced fabrication processes, but also advanced circuit and device simulation tools which must accurately include device level effects such as velocity saturation.

In conclusion, GaAs Schottky device technology is reaching maturity for submillimeter-wave applications. Our primary goal in the next few years will be to increase system bandwidth and reliability, while also reducing component costs, by achieving higher levels of integration.

Hot Electron Bolometer Mixers, State of the Art in Europe

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In this paper will be given a short overview of superconducting hot electron (HEB) mixers and some results obtained in Europe. Excellent results have been obtained and both phonon cooled and diffusion cooled versions have been realized.

For radio astronomy and remote sensing applications at frequencies of the order THz there is a strong need for receivers with much higher sensitivity than is available at present. Today, most receivers for frequencies near and above 1 THz have to rely on Schottky-diode mixers, with rather poor sensitivity [1,2]. Low noise SIS mixers based on superconductors have excellent performance and have replaced Schottky-diode mixers for frequencies up to about 650 GHz, corresponding to the energy gap of niobium [1,2,4,5]. Since niobium tri-layer technology is by far the most successful SIS-mixer technology and since the RF loss will be significant above the energy gap of niobium [3, 6], it may be very difficult to realize SIS mixers with a noise temperature limited to a few times the quantum limit ($T_{q\text{-limit}} \approx hf/k$) above about 700 GHz.

Superconductor Hot-Electron Bolometer (HEB) mixers utilizing thin superconducting films in the resistive state have recently emerged as a serious alternative to the traditional mixers used in THz receivers [7-9]. In one version, phonon cooled devices are used. In another version one is utilizing diffusion-cooling of hot electrons [10,11]. Which version which will come out as the better one is unclear at the moment when this lecture note is produced (Sept. 1997). These recently proposed devices have a very simple structure, and can be realized with a technology which is relatively uncomplicated compared to the SIS and Schottky diode fabrication. Based on the frequency insensitive nature of the electromagnetic interaction and the non linearity of these devices, the devices should be possible to use to several THz, where the device can be integrated with planar antennas.

The principal disadvantage of a bolometric mixer is the response time τ_o of the bolometer, limiting the maximum IF to $1/2\pi\tau_o$. In Fig. 1 the basic elements of the bolometer are shown. The absorbing part of the bolometer (the electrons in the hot-electron bolometer) has a certain heat capacity C, and there is a thermal conductance from the absorber to the thermal bath. The response time is then $\tau_o=C/G$, i. e. the larger the heat capacity and the smaller the thermal conductance the longer is the response time.

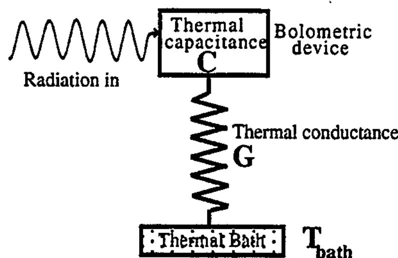

Figure 1. Basic elements of a bolometer.

A superconducting Hot Electron Bolometer consists of one or several superconducting thin film strips in parallel, deposited on a substrate, of for example, silicon, single crystalline

quartz or sapphire. The strips are cooled to the superconducting state and then heated by DC and microwave power to temperatures near the superconducting to normal transition-temperature, where the superconductor will gradually become normal (Fig. 2).

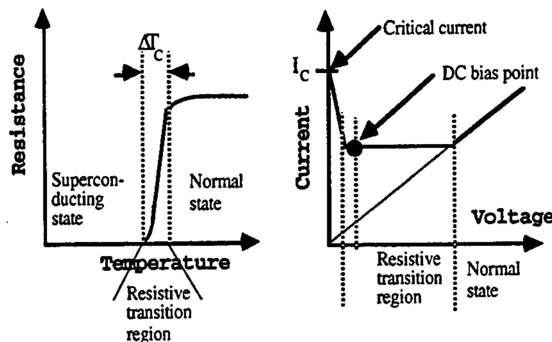

Fig. 2. The three states of the bolometer: the superconducting, resistive and the normal state.

The resistance of the device in the resistive transition region, may be explained with the help of several possible physical phenomena, such as formation of normal domains, phase slip centers, and moving magnetic vortices [12, 13, 14].

If the signal and LO frequency are high enough so that $f_{LO}, f_s > 2\Delta/h$, (2Δ is the energy gap) the full length of the superconducting strip will be seen as a normal conductor strip by the RF. In this case the absorption of RF power by the normal electrons in the HEB is essentially frequency independent. Therefore, these mixers will operate up to RF frequencies well into the THz range, i.e. to much higher frequencies than the gap frequency of the superconductor. On the other hand, if the signal and LO frequency are low enough so that $f_{LO}, f_s < 2\Delta/h$, the modulation of the resistance at the IF frequency will be noticed by the RF and LO, and power is transferred to the image frequency $(2f_{LO}-f_s)$ [15]. Since $f_{IF} < 1/2\pi\tau_o$ it follws that the IF impedance is essentially equal to the DC small signal impedance, i.e. dV/dI in the bias point.

There are two types of bolometric devices, the "phonon cooled" and the "diffusion cooled" ones. Since the maximum IF-frequency is determined by the electron temperature relaxation time τ_o, i. e. $f_{IF} < 1/(2\pi\tau_o)$, a major issue is to find ways of making the time constant τ_o, short enough.

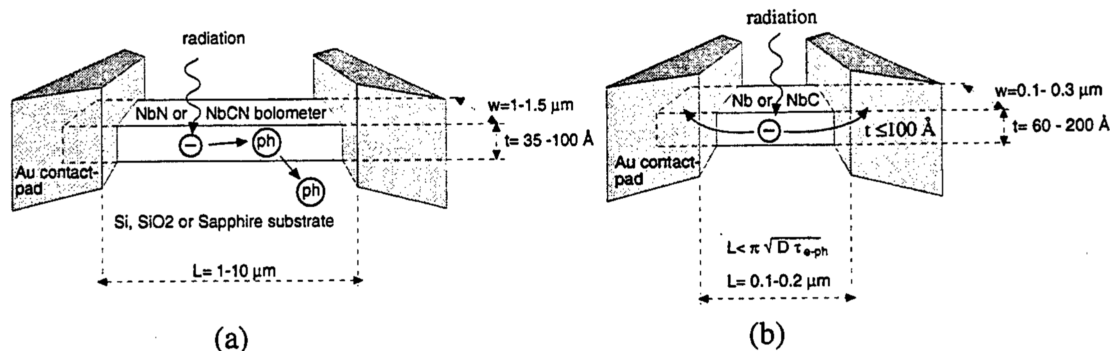

Figure 3. The two types of bolometric devices, phonon cooled (a) and diffusion cooled (b).

Typical dimensions of the **phonon cooled** devices are shown in Fig 3a. To obtain a short relaxation time for the heated electrons (τ) and to avoid lattice heating effects in the superconductor, the bolometer should be ≤ 50Å thick and ≤1 μm wide. For Nb the resulting bandwidth corresponding to $(2\pi\tau)^{-1}$ is of the order 100 MHz [7,9], and for NbN several GHz [8]. With higher T_c, a higher operating temperature can be used, yielding shorter τ. NbN mixers have so far demonstrated >3 GHz bandwidth [16, 17].

The diffusion **cooled device** was first suggested by Prober [10,11]. For the cooling of hot electrons in this device is used the rapid diffusion of hot electrons out of a submicron length strip of superconductor into normal metal contacts (Fig. 3b). For the diffusion mechanism to dominate over the electron-phonon cooling, it is necessary to make the micro bridge extremely short. The appropriate length L can be estimated from [10]

$$L \approx 2\sqrt{D \cdot \tau_{ee}}$$

where D is the diffusion constant and τ_{ee} is the electron-electron energy relaxation time. Basically when an electron in the middle of the bridge absorbs energy from an RF photon, it will stay excited for the time τ_{ee} while it can diffuse the distance L/2 to the normal metal contact which will serve as a heat sink. The pads must be normal metal since Adreev reflection [18] at the interface between the thin hot superconductor (with very small energy gap 2Δ) and the cold superconductor (with full size energy gap 2Δ) will otherwise trap the electron in the bridge. For a 10 nm thick Nb film, L≈0.2 μm. In other materials, such as NbN, it is much shorter, and hence is not likely to perform well in a diffusion cooled mode.

Results obtained in Europe known to the author at the time of writing this abstract are as follows:

Phonon cooled at Chalmers and MSPU: 480 K at 620 and 900 K at 980 GHz [19]
Phonon cooled at IRAM: 9OO K at 800 GHz [20]
Diffusion cooled at KOSMA: 1500 K at 666 GHz [21]
Diffusion cooled at RUG & SRON: 2200 K at 735 GHz [22]

The Moscow State Pedagogical University (MSPU) has made most important contributions to the field partly in collaboration with other groups in Europe and US.

A crucial number is the maximum IF bandwidth. For a phonon cooled HEB-mixer a 3.2 GHz IF bandwidth (conversion gain) has been measured and for diffusion cooled between 2 and 6 GHz [23, 24]. The LO power needed is less than 100 nW.

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Planar Technology of Schottky Diodes and other Components for Quasioptic Integration

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In view of the may applications of Terahertz electronics, such as atmospheric evaluation from satellites, plasma density and temperature distributions in systems like Tokamak's, inter-satellite communication etc., a quasioptical approach by monolithic integration is of great interest now. Matrices of antennas, Schottky diodes and bias supplies are interconnected by towers and airbridge structures to avoid frequency limitations by stray capacitances. Diode-series resistances are reduced by micromechanical metal membranes deposited into substrate cavities from the back side with subsequent partial removal of the carefully designed n layer using epitaxial GaAlAs etch stop layers. The antennas are dipole or slot structures.

The matrices are structured for harmonic extraction using different antennas for each of the relevant frequencies. The corresponding illumination and emission waves are polarized orthogonally to each other, in order to achieve their separation by polarization filters, although classical quasi-optical filters can also be employed. Other examples are quasi-optical sources using an array of mutually coupled sources, and quasi-optical mixers.

The fabrication technologies are presented in detail, in particular also regarding high fabrication yield and operational reliability. Here the details are given of Schottky interface preparation for low-noise operation, of the metalisation sequences and of the use of suitable insulators such as polyimides.

Heterostructure Field-Effect Transistors for mm-Wave Applications - a Short Review

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Over the last dozen years heterostructure field-effect transistors (HFETs) have reached a high degree of maturity. These devices have been developed to the point where they now provide circuit designers with a transistor that can operate beyond 100 GHz. The maturity of the technology has taken the devices from academic laboratories to the fabrication lines of major foundries. This development has been enabled by advances in fine-line lithography, layout optimization and material structure development. Of particular significance, the micro-fabrication in the vertical and lateral directions can be performed with acceptable yields.

This paper will provide a brief review of the present state-of- the-art of these devices. Performance data will be shown and the specific design enhancements leading up to the latest improvement will be discussed. Using a simple equivalent circuit model, it will be shown where future improvements can be made. One of the more critical parameters for high performance is the electron transport properties of the semiconductor material. At present, the most common approach of achieving better transport properties is by an increase in the In-concentration in InGaAs. This can be done using thin strained layers (the pseudomorphic approach), or by using lattice-mismatched structures (the metamorphic approach). Both approaches can be used on GaAs and InP substrates. However, the monotonically decreasing bandgap with In-concentration results in break-down- and output resistance-problems when the concentration is too high. Different approaches for optimizing such structures and possible alternative material choices will discussed.

Millimeter and Submillimeter Wave Semiconductor Device Development at RIKEN and Tohoku University

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Abstract

Schottky barrier diodes (SBD's) remain an important device for detecting and mixing at terahertz frequencies, particularly in space applications and plasma diagnostics. Resonant tunneling diodes (RTD's) are also of interest, due to their potential for submillimeter wave signal generation. We will briefly outline the ongoing efforts in fabrication and testing of both SBD's and RTD's being carried out jointly at RIKEN and Tohoku University.

Submillimeter wave and terahertz applications require sub-micron anode SBD's. While UV contact photolithography is suitable for producing circular anode patterns down to 0.7 µm in diameter, smaller diameter diodes are needed to extend operation beyond 1.4 THz. A simple E-beam exposure technique involving the control of an SEM system was developed to pattern 0.3 µm or smaller anodes, suitable for use at frequencies up to 2.5 THz. Additionally, precisely controlled ECR plasma etching and high temperature annealing techniques have been employed to minimize surface defects for these anodes, and thus reduce 1/f noise. Such diodes have been optimized for plasma diagnostics using an IF in the 100 KHz to 1 MHz range, but are also being developed for radiometer applications at 2.5 THz using a higher IF.

In order for an RTD to oscillate in the millimeter and submillimeter wave region, a diode mesa structure of several microns or less is required. Fabrication of such RTD's has been investigated using both wet and dry etching processes, with significantly better results obtained using dry etching. RTD power combining at frequencies up to 100 GHz has been demonstrated using such diodes in a quasi-optical resonator.

Part of this work was carried out at the Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University, supported by the Heiwa Nakajima foundation and a Grant-in Aid of Scientific Research from the Ministry of Education, Science and Culture of Japan.

Dopant Fluctuations and Quantum Effects in Sub-0.1um CMOS

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I. INTRODUCTION

The scaling of CMOS gate lengths below 0.1um will expose physical phenomena which are not important for current (and past) technologies. Among these are the discrete nature of dopant ions, tunneling, and size quantization. In this work we attempt to quantify the magnitude of these effects and identify methods to reduce or eliminate device degradation due to them.

To date, transistor dimensions are much larger than the screening length of an individual dopant ion (≈ 100Å). Moreover, the number of dopant ions in a single device is rather large (> 1000). Given these conditions it is perfectly reasonable to assume that the net effect of the dopant ions may be described by a continuous charge distribution. Indeed, this assumption has proven to be quite accurate in device simulation for current and past technology nodes. As we scale the gate length below 0.1um, however, we must begin questioning the validity this assumption. Another common assumption is that the current flowing through the gate insulator is neglible and can be ignored. Sub-0.1um technologies will require[1] effective gate oxide thicknesses below 30 Å. Since direct tunneling current increases exponentially with reduced oxide thickness, a limit will be reached where the thickness can no longer be scaled. Finally, degradation of transistor performance due to carrier confinement quantization should be investigated for very small geometry structures. We shall investigate these issues using device simulation tools and suggest methods to reduce or avoid their effects.

II. DOPANT ION FLUCTUATIONS

As previously mentioned the discrete nature of dopant ion charge will become evident in scaled technologies.[2,3] We have performed a simulation study on the magnitude of the effect of channel dopant ion position fluctuations in scaled MOS devices. A three-dimensional drift-diffusion simulator (TMA Davinci) is employed to simulate carrier transport. Since we are using a drift-diffusion model we cannot (with any certainty) make any conclusions about scattering-limited transport regimes. We therefore limit our analysis to the MOSFET subthreshold region.

The charge due to a dopant ion is modelled by assigning a meshpoint with a dopant concentration equal to the inverse of the volume associated with that meshpoint. In our simlations a uniform grid spacing of 2nm is used in the channel region. The test device used in the analysis is an NMOS with $t_{OX} = 3nm$, $x_j = 10nm$ and $N_{CHAN} = 1 \times 10^{18} cm^{-3}$. In Fig. 1 the sub-threshold potential barrier for electrons injected from the source is illustrated for a $W = L = 40nm$ device.

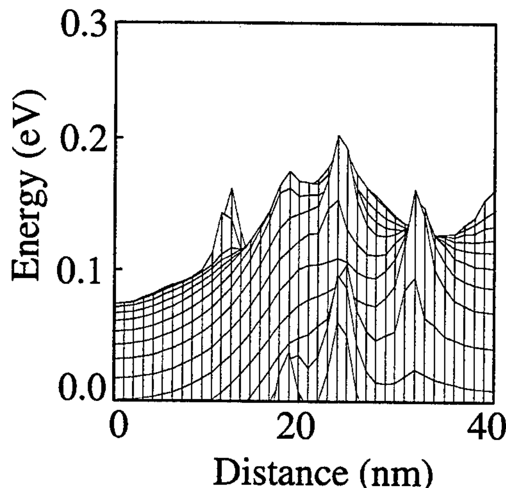

FIG. 1. Electron potential barrier for source electrons in a $W = L = 40nm$ NMOS for $V_{GS} = 0.3V$ and $V_{DS} = 1.0V$ (subthreshold region).

The location and magnitude of the "peaks" and "valleys" in the source barrier will depend on the arrangement of the channel dopant ions. In Fig. 2, I_{DS}-V_{GS} characteristics for different random ion arrangements are shown. The dots in this figure correspond to the continuous dopant charge simulation. Note the discrete dopant ion simulations predict a significant variation in V_T as well as a negative shift in the average V_T compared with the continuous simulation. The negative shift is due to the fact that thermal transport over a barrier decreases exponentially with energy. Since the source barrier due to discrete ions fluctuates (Fig. 1), a disproportionate amount of the current flows through a potential "valley" thus reducing V_T.

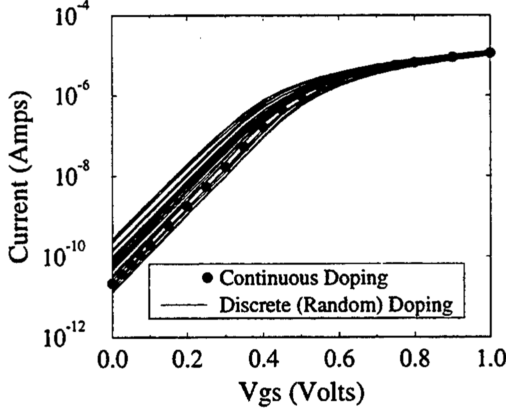

FIG. 2. I_{DS} vs. V_{GS} for continuous (dots) and discrete random (lines) channel doping distributions. The discrete random profiles exhibit significant variations in threshold voltage depending on the arrangement of channel dopant ions.

It is the variation in V_T due to ion arrangement that is of concern for scaled technologies. The standard deviation in sub-threshold V_T (voltage at $I_{DS} = 1nA$) for 100 random dopant distributions is $38mV$ for the $W = L = 40nm$ device. In order to understand the dependence of this variation on device geometry, simulations were carried out for three different gate lengths and two different gate widths. The results are summarized in Table I. As expected, the variation in threshold decreases significantly as the gate length increases. However, these simulations indicate that threshold variance does not decrease for wider devices. The reason for this is that the subthreshold current flow is highly localized. Nearly all of the current flows through the path with the lowest barrier height.

W	L	σ_{V_T}
40nm	40nm	38mV
40nm	80nm	27mV
40nm	120nm	20mV
80nm	40nm	39mV

TABLE I. Threshold voltage ($I_{DS} = 1nA$) standard deviation due to random dopant ion arrangment for various gate lengths and widths. Sample size for all cases is 100. Variation in threshold voltage decreases as gate length increases. However, there is no dependece on gate width. This is due to the fact that the sub-threshold current flow is highly localized.

From this simulation study it is evident that random dopant ion arrangement is a formidable issue for sub-0.1um CMOS. What can be done to reduce or eliminate these effects? The most obvious solution is to remove the dopant ions from the vicinity of the current flow path. To test this, channel dopant ions were completely removed from the surface ($0 - 5nm$) of the $L = W = 40nm$ structure. Indeed, this results in a reduction in threshold standard deviation of 32% (from $38mV$ to $26mV$). However, it will be hard to push such techniques much further. The reason for this is dopant ion charge will always be required to screen the drain potential from the source. An ultimate solution is provided by a structure composed of a narrow semiconductor channel sandwiched between gates on top and bottom (see insert of Fig. 3). In this structure, the drain potential can be screened by charge on the opposing gates provided that the silicon film is sufficiently thin (i.e. $\approx L_G/4$).[4,5] Therefore, no dopant ions are required in the channel. In Fig. 3, simulated I_{DS}-V_{GS} curves for a double gate device are shown for varying channel doping. For channel doping levels below $1 \times 10^{17} cm^{-3}$ the I_{DS}-V_{GS} characteristic is independent of doping level and thus impervious to dopant fluctuations.

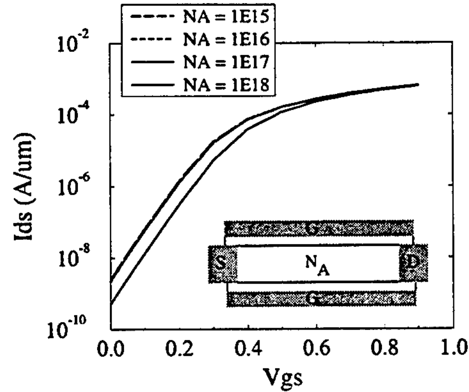

FIG. 3. I_{DS}-V_{GS} curves for a double gate device with $t_{OX} = 30Å$, $L_G = 40nm$ and $t_{Si} = 8nm$ for different channel doping concentrations. The IV characteristics remain unchanged for doping concentrations below $1 \times 10^{17} cm^{-3}$. The drain potential is completely screened by the opposing gates so no dopant ions are required in the channel.

III. GATE INSULATOR TUNNELING

As the gate length of the MOS transistor is scaled, the gate oxide thickness must also be scaled.[1] The ultimate scaling limit for gate oxide thickness will most likely be determined by direct tunneling current. To estimate this limit we employ a non-equilibrium Green's function simulator (NEMO) de-

veloped at Texas Instruments Inc.[6] In Fig. 4, measured and simulated IV characteristics are illustrated for a $Si/SiO_2/Al$ MOS capacitors with different oxide thicknesses. The simulations employ a two-band model with Hartree self-consistent potentials and include injection from both bound and continuum states.[7] The oxide effective mass ($m^*_{SiO_2} = 0.42m_0$) has been extracted by Brar et. al.[8] Oxide thicknesses are extracted from CV measurements using a multi-band Hartree self-consistent simulator.[7]

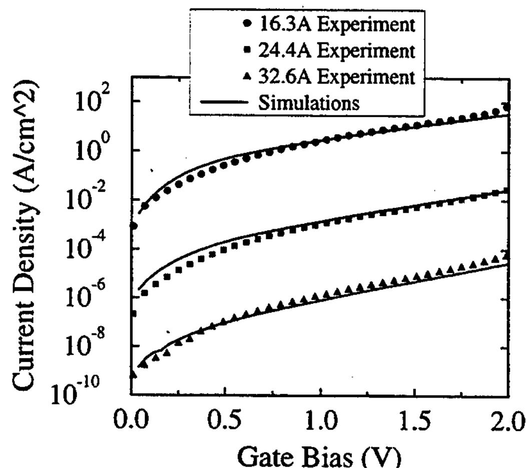

FIG. 4. Current density vs. gate bias for $Si/SiO_2/Al$ MOS capacitors with different oxide thicknesses. Symbols represent data, lines are simulation. The substrate is n-type with a concentration of $1 \times 10^{18} cm^{-3}$.

In Fig. 5, simulated current density vs. oxide thickness at 1.0V is shown. For the purpose of approximating a scaling limit for oxide thickness we shall assume a limit of $1nA$ per micron of gate width as an allowable upper bound for leakage current. For a gate length of $0.1um$, this corresponds to a tunneling current density of $1A/cm^2$ (assuming homogeneous flow through the gate insulator). According to the curve in Fig. 5, this corresponds to an oxide thickness of approximately 17Å. One can obtain thinner effective oxide thicknesses by employing a gate dielectric with a higher permitivity than SiO_2. Dielectrics such as TiO_2 ($\epsilon \approx 30$)[9] and Ta_2O_5 ($\epsilon \approx 25$)[10] have been suggested for gate insulators. However, it is not yet clear if these dielectrics can form high quality interfaces required to obtain high channel mobilities. The use of nitrided oxides has also been studied.[11,12] These films provide high channel mobilities as well as a marginal reduction in the effective gate oxide thickness.

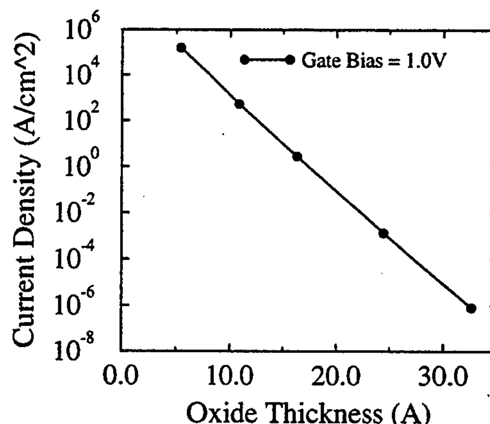

FIG. 5. Simulated direct tunneling current density vs. gate oxide thickness for a $Si/SiO_2/Al$ capacitor with $V_{GB}=1.0V$.

IV. SIZE QUANTIZATION

Another effect that reduces the performance of MOS devices is energy quantization due to the inversion layer confining potential. This results in a reduction in the density of states in the channel and moves the channel charge centroid away from the gate.[13] As illustrated in Fig. 6 this reduces the inversion capacitance (and thus the drive current) of the MOS device. For an oxide thickness of 20Å, quantization results in a $\approx$12% reduction in inversion capacitance. Unfortunately there is not much one can do to reduce or eliminate this effect.

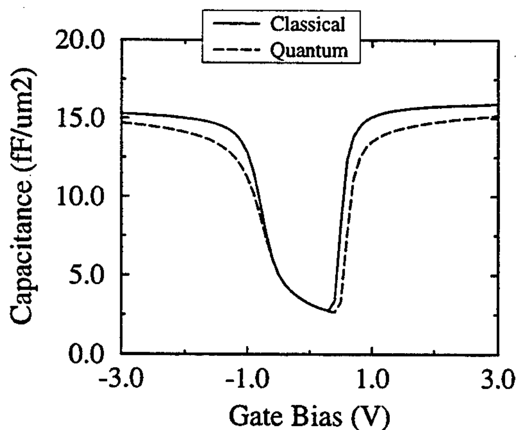

FIG. 6. Comparison between quantum and classical simulation of an MOS capacitance-voltage characteristic. Oxide thickness is 20Å, channel doping is $N_A=10^{17}$, and the gate material is TiN. The inversion capacitance predicted quantum mechanically is 12% less than the classical prediction.

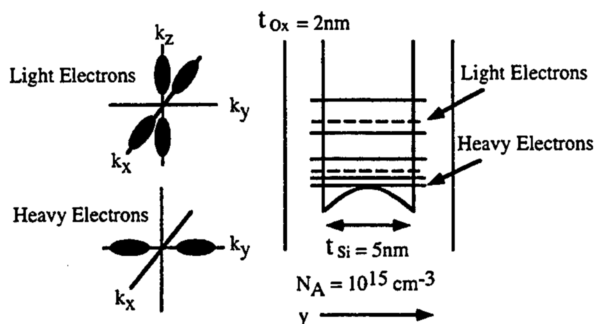

FIG. 7. Conduction band edge and bound state energies for a double gate capacitor. For small silicon film thicknesses, size quantization is enhanced. The density of states and therefore the drive current is subsequently reduced.

We shall now investigate the size quantization effect on the double gate structure. It was shown in section II that this structure provides a solution to the dopant fluctuation problem for thin silicon films. We would like to know at what film thicknesses does size quantization begin to seriously degrade device performance. As shown in Fig. 7, for very thin silicon films the confining potential is determined by the oxide barriers which results in enhanced quantization. One would therefore expect that for thin enough films, degradation due to quantization would also become enhanced.

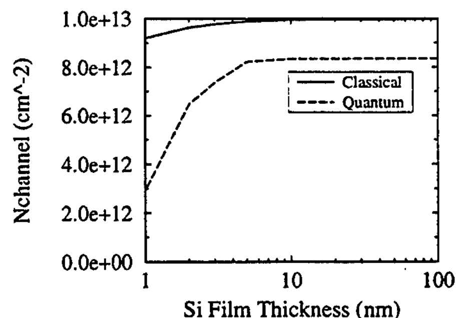

FIG. 8. Double gate capacitor (channel) inversion charge vs. silicon film thickness. Size quantization effects become more pronounced for film thicknesses below ≈ 5nm. Channel doping is $N_A = 10^{15}$, $t_{ox} = 20$Å, gate material is TiN, and $Vgs = 1.0V$.

To determine the onset of this enhancement we calculate the inversion charge in a double gate capacitor both classically and quantum mechanically as a function of silicon film thickness. An efficient multi-band Hartree self-consistent Poisson solver is used for the calculations.[7] In Fig. 8 it is apparent that for Si film thicknesses below ≈ 5nm quantization begins to seriously reduce the amount of charge in the channel. As mentioned previously, a ratio between the gate length and the silicon film thickness of approximately four must be maintained in order to avoid punchthrough. This suggests that a double gate structure impervious to dopant fluctuation effects should be scalable to a gate length of about 20nm before quantum effects seriously degrade device performance.

V. CONCLUSIONS

We have investigated the effects of dopant fluctuations, tunneling and size quantization on sub-0.1um CMOS. It was shown that dopant fluctuation effects can be supressed with a thin intrinsic layer in bulk devices and eliminated using a double gate device. Direct tunneling current places the scaling limit of SiO_2 gate insulator thickness at approximately 17Å for $L_G = 0.1um$ devices. Alternate gate dielectrics with higher permitivity offer possible methods to push this limit further. Size quantization effects were shown to not severely degrade the performance of the double gate structure until the silicon film thickness is reduced to below 5nm. This suggests that size quantization limits the scaling of this structure to gate lengths of about 20nm.

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Laterally Modulated, Heterodimensional Junction Field Effect Transistor for Ultra Low Power Applications

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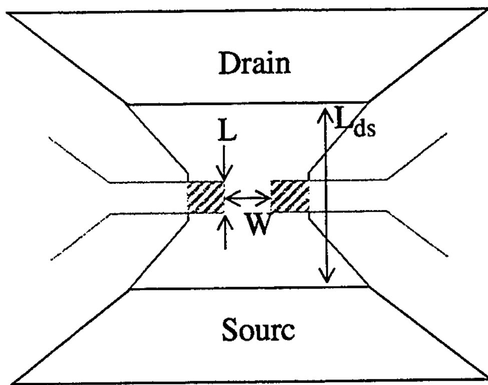
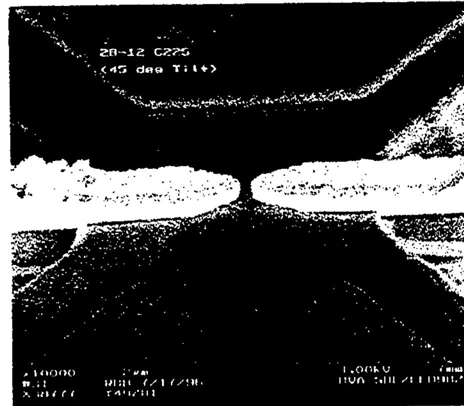
Abstract: The 2-D JFET, fabricated on bulk n-GaAs, utilizes p+ implants on both sides of a very thin, shallow n-type Si-implanted channel ($n_s \sim 2 \times 10^{12}$ cm^{-2}) to laterally modulate the current between the source and drain. Prototype 2-D JFETs having nominal gate length and channel width of 1 µm had V_T=0.1 V, peak current of 10 µA, and saturation voltage of 0.35 V. Due to the sidegate geometry, 2-D JFET device dimensions (both gate lengths *and* channel widths) may be scaled to deep submicron dimensions without degradation of the electrical characteristics. The excellent low power operation together with a manufacturable process make the 2-D JFET very promising for future ultra low power IC applications.

Introduction: Recently, we proposed and fabricated a new transistor called the 2-D metal-semiconductor field effect transistor (2-D MESFET) in which sidewall Schottky contacts on either side of an AlGaAs/InGaAs/GaAs heterostructure laterally deplete the narrow 2-D electron gas (2-DEG) channel [1]. One of the principal advantages of this device is that the narrow channel effect (NCE), which leads to parasitic currents at the gate edges in a top-gated structure, is eliminated by the unique sidewall gate geometry. Thus, 2-D MESFET device dimensions (gate lengths *and* channel widths) may be scaled to deep submicron dimensions without degradation of the electrical characteristics [2]. A second advantage of the device is that the heterodimensional Schottky metal/ 2-DEG contact has unique electronic properties which provide a larger depletion width, smaller capacitance, and higher breakdown voltage than conventional metal/semiconductor contacts [3]. Together, the deep submicron dimensions and small gate-to-channel capacitance of the 2-D MESFET are promising for future high speed, low power IC applications. In fact, AIM-Spice simulations of 11-stage 2-D MESFET ring oscillators predict an order-of-magnitude improvement in the power-delay product compared to existing technologies [2]. In order to demonstrate a lower cost, more manufacturable 2-D MESFET fabrication process, we have also investigated 2-D MESFETs fabricated on ion implanted material (the 2-DI MESFET), in which the MBE-grown AlGaAs/InGaAs/GaAs heterostructure is replaced by bulk n-GaAs material having a thin Si-doped channel [4]. The ion implanted devices still have excellent electrical characteristics at sub-half-micron channel widths, including low output conductance, low saturation voltage, and large ON/ OFF ratio. However, the 2-D MESFET process still faces a major manufacturability roadblock—the sidewall Schottky contacts are formed by the electrochemical plating of Pt/Au metal into etched submicron gate trenches. Electroplating techniques are not generally used in the production of commercial GaAs LSI circuits.

The 2-D JFET: In this work, we investigate a new all-ion-implanted, quasi-heterodimensional field effect transistor, the 2-D JFET. The 2-D JFET, fabricated on bulk n-GaAs, utilizes p+ Be implants on either side of a very thin Si-doped channel (7×10^{12} cm^{-2} at 40 keV) to laterally modulate the conducting channel between the source and drain contacts. The geometry of the 2-D JFET is identical to that of the 2-D MESFET, except ion implants replace both the degenerate 2-DEG channel and the electroplated Schottky gates. Fig. 1 shows a schematic of the 2-D MESFET and illustrates the evolution of the device from the Schottky-gated 2-D MESFET to the all-ion

top view:

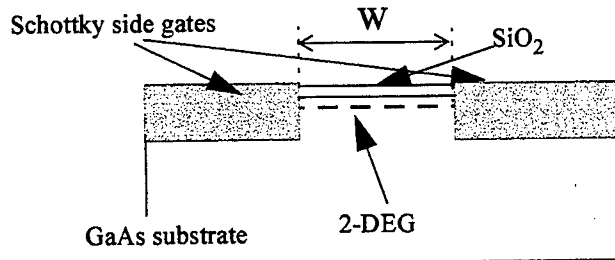




cross section through gates:

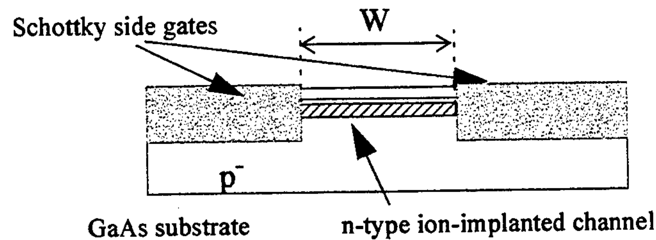
2-D MESFET

- AlGaAs/InGaAs/GaAs heterostructure
- 2-DEG channel
- electroplated Pt/Au gates



2-DI MESFET

- bulk n-GaAs material
- implanted Si channel
- electroplated Pt/Au gates



2-D JFET

- bulk n-GaAs material
- implanted Si channel
- implanted p+ gates

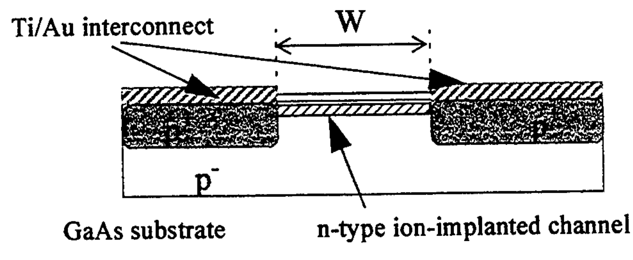


Fig. 1. (a) Illustration of the top view of a 2-D MESFET and SEM image of corresponding view, and (b) cross section of 2-D MESFET, 2-DI MESFET, and 2-D JFET showing evolution toward more manufacturable process.

implanted 2-D JFET. Prototype 2-D JFETs had nominal gate lengths, L_g, of 1, 2, 4, and 5 μm; nominal gate-to-gate widths, W, of 1, 2, and 3 μm; and drain-to-source spacing, L_{ds}, of 15-20 μm. Future device dimensions will be scaled to submicron values, limited only by lithography and lateral diffusion but not by deleterious short or narrow channel effects.

Results: Fig. 2 shows measured and modeled current voltage characteristics for a dual-gated 2-D JFET having W=2 μm and L_g=4 μm. The effective channel width, as predicted by ATHENA simulations shown later in this paper, is closer to 1.4 μm due to lateral diffusion of the p+ implants. The threshold voltage of the device is -0.25 V, the peak current at V_{gs}=0.6 V is about 40 μA, and the saturation voltage at V_{gs}=0.4 V is approximately 0.5 V. The modeled characteristics were obtained using the 2-D MESFET AIM-Spice model, a physics-based semi-empirical FET model which models the drain current behavior in both the above-threshold and below-threshold regimes of operation using a single, continuous analytical expression [5].

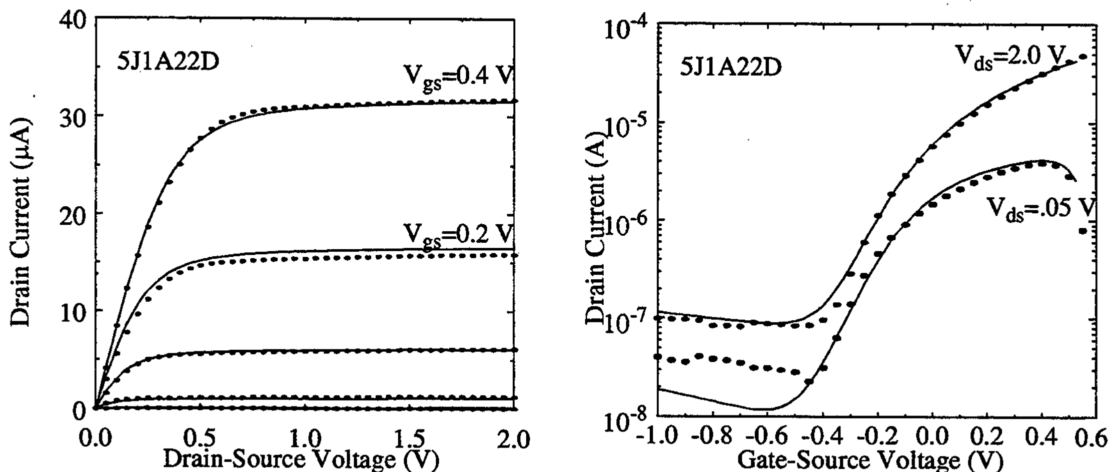


Fig. 2. Measured (dots) and modeled (lines) drain current characteristics for a dual-gated 2-D JFET having nominal L_g=4 μm and W=2.0 μm. Following implant and RTA, the actual channel width is closer to 1.5 μm. The leakage current should improve by at least an order-of-magnitude following optimization of the isolation etch and the gate metal.

Fig. 3 shows the drain current versus drain-source voltage characteristics of a coaxial 2-D JFET having nominal L_g=W=1 μm. Following the RTA, the effective W is ~ 0.4 μm. The threshold voltage of this device is 0.1 V, the peak current at V_{gs}=0.5 V is 10 μA, and the saturation voltage at V_{gs}=0.5 V is 0.35 V. As evident in the figure, the output conductance is negligible (less than 0.5 mS/mm) despite the narrow channel width.

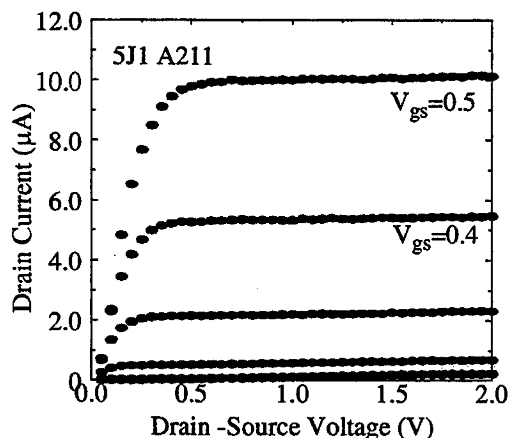


Fig. 3. Measured I_d vs. V_{ds} characteristics of a coaxial 2-D JFET with effective W=0.5 μm.

Simulations: The implant profiles and effective channel widths were simulated using the numerical process simulator ATHENA [6]. Doping profiles from this simulation are shown in Fig. 4 for a 2-D

JFET with a nominal channel width of 1.0 μm. This plot illustrates both the quasi-heterodimensional nature of the p+/n contact as well as the lateral diffusion which reduces the effective channel width from 1.0 μm to less than 0.5 μm. ATLAS II simulations of the 2-D JFET and 2-D MESFET demonstrate that the energy band diagrams of the two devices are qualitatively very similar, as shown in Fig. 5 [6].

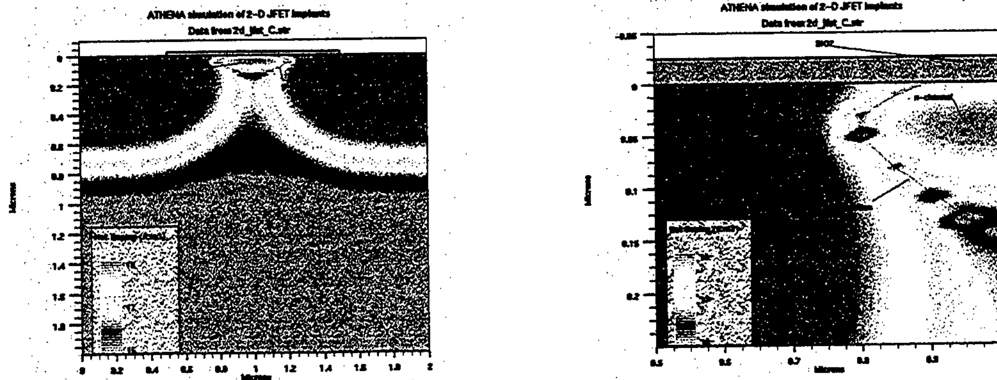


Fig. 4. ATHENA simulations of the implanted regions in the 2-D JFET. The plot on the left shows the doping contours in a cross section of the 2-D JFET. The plot on the right is a close-up of the channel region. These plots illustrate the quasi-heterodimensional nature of the p+/n contact as well as the lateral diffusion length of the p+ regions.

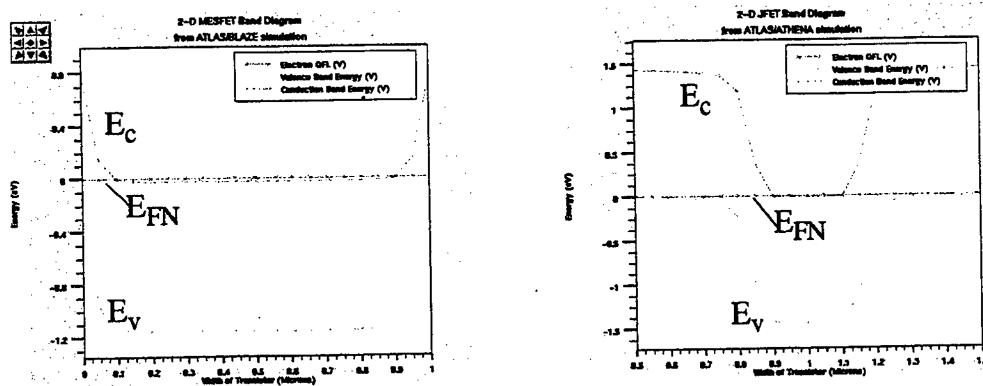


Fig. 5. Comparison of energy band diagrams through the channel of the 2-D MESFET (left) and the 2-D JFET (right).

Summary: We have demonstrated for the first time fully-ion-implanted, quasi-heterodimensional 2-D JFETs with effective channel widths as low as 0.5 μm. This approach offers the excellent low power characteristics of 2-D MESFET technology using a fully manufacturable process and is hence very promising for future ultra low power IC applications.

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Compact Logic/Memory Elements Using a Gated 2D-2D Quantum Tunneling Transistor*

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We have fabricated a novel quantum device, the double electron layer tunneling transistor (DELTT), from an MBE-grown double quantum well heterostructure. The DELTT is entirely planar in configuration, enabling ease in fabrication. Its operating principle is based on 2D-2D resonant tunneling, which can be easily controlled by surface Schottky gates. We illustrate the multifunctionality of a single DELTT at 77 K by demonstrating (1) a bistable memory and (2) logic elements such as exclusive-OR and NAND gates. These circuits use considerably fewer transistors than their conventional counterparts.

1. Introduction

Quantum devices based on resonant tunneling have long been of great interest because they are the fastest electronic devices known, due to the short characteristic time of the coherent tunneling process. The double-barrier-resonant tunneling diode (RTD) has been demonstrated to operate at frequencies up to 712GHz. [1] In addition to high speed applications, various novel digital circuit applications have been demonstrated, which rely on the negative differential resistance (NDR) characteristics inherent in resonant tunneling. [2] However, all these circuits are constructed using either two-terminal RTD devices, or hybrids formed by combining RTD structures with conventional transistors. This approach suffers from either the lack of isolation between input and output terminals, an increase in circuit complexity, or a reduction in speed from the presence of conventional devices. While the addition of a third gate-controlled terminal to an RTD would be ideal, such geometries have typically required lateral depletion and/or lateral quantum confinement [3], which is highly problematic owing to the stringent lithographic tolerances required.

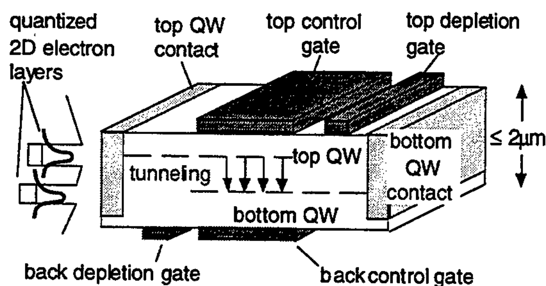

Fig. 1. Schematic of the DELTT. Energy band diagram is shown at left.

In this work, we report a new quantum FET based on 2D-2D resonant tunneling, the double electron layer tunneling transistor (DELTT). Using the DELTT's multi-functionality, we demonstrate several circuits at 77 K. These include bistable memories, highly compact digital logic elements, and gate-controlled oscillators.

2. Device Operating Principle And Fabrication

A schematic of the DELTT is shown in Fig. 1. Its principle of operation is the gate control of 2D-2D resonant tunneling between the two 2D electron layers in a double quantum well (DQW) hetero-structure. Due to the requirement of conservation of energy and momentum, resonant tunneling can occur only when the two energy-dispersion paraboloids rest on top of one another, yielding states in both QWs with identical energy and momentum. [4] As a result, the tunneling current can be controlled by either (1) varying the densities of either 2D layer with surface Schottky gates, or (2) changing the Fermi level difference between the QWs by applying a source-drain bias. The advantages of the DELTT over tunneling transistors based on laterally gated RTDs are (1) sharper tunneling resonances due to greater restrictions in momentum space (i.e. 2D-2D tunneling instead of 3D-2D); (2) an entirely planar configuration allowing a vastly easier fabrication.

Devices were processed from an MBE-grown heterostructure with two modulation doped 120 Å GaAs QWs separated by a 125 Å $Al_{0.3}Ga_{0.7}As$ barrier. The top and bottom QWs had electron densities of 8.0 and 2.0 x 10^{11} cm^{-2}, respectively. The source (top QW) and drain (bottom QW) contacts are formed by diffusing Au/Ge/Ni

to both QWs, and then using Ti/Au gates to deplete the QW one does *not* wish to contact. (See Fig. 1.) Vertically aligned 200 x 500 μm^2 front and back gates act third and fourth terminals, modulating the density of the top and bottom QWs respectively. Our innovative flip-chip epoxy-bond-and-stop-etch (EBASE) processing technique allows placement of the backgates less than 2 microns from the bottom QW.

3. Current-Voltage Characteristics.

To characterize the DELTT device, we measure the small signal source-drain conductance G_{SD} vs. control gate voltage. In the device of this work, the top QW has about 4 times higher electron density than the bottom QW, with no gate bias applied. In Fig. 2(a) we show G_{SD} vs. the top control gate voltage V_{TC}, at a fixed back control gate voltage V_{BC}=0. When $V_{TC} \approx$ -0.7 V, the top QW is sufficiently depleted that it has the same electron density as the bottom QW, causing the energy-momentum paraboloids to coincide and tunneling to occur. This results in a large resonant tunneling peak at $V_{TC} \approx$ -0.7 V. At more positive V_{TC}, the densities are imbalanced, and the resonant

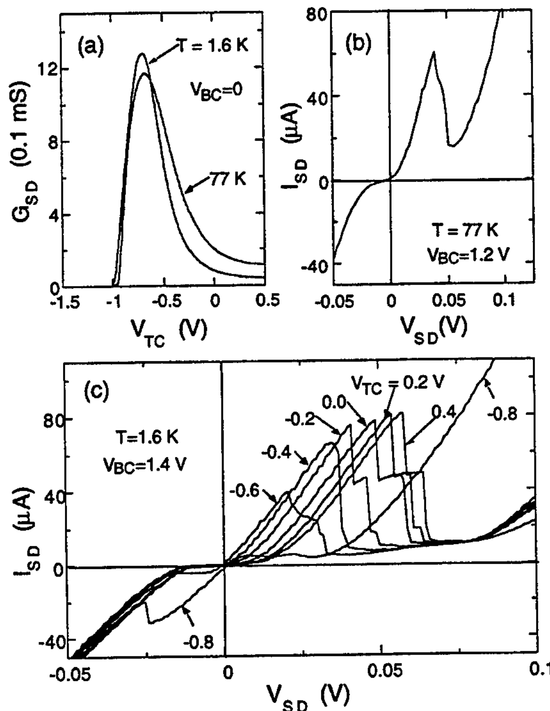

Fig. 2. (a) source-drain conductance vs. V_{TC} at 1.6 and 77 K. (b) 77 K source-drain I-V curve for V_{BC}=1.2 V. (c) 1.6 K source-drain I-V curves for V_{BC}=1.4 V and several different V_{TC}.

tunneling is quenched, causing G_{SD} to drop by a factor of ~50 at 1.6K. We note that the peak position is also controlled by V_{BC}: for more positive V_{BC}, the peak occurs at more positive values of V_{TC}. The data thus clearly demonstrate the gate control of the tunneling current.

The DELTT's operating temperature is limited by the energy difference ΔE between the two QW subbands in the ungated regions adjacent to the control gate. When kT is comparable to ΔE, significant leakage current appears. By increasing ΔE, the operating temperature can be increased significantly. Because this device has a large built-in density imbalance, it continues to exhibit negative transconductance at relatively high temperatures. The resonance in G_{SD} still exhibits a peak-to-background ratio of 10:1 at 77K, as shown in Fig. 2(a). We have observed ratios of 2:1 at 170 K. The I-V curve also exhibits a strong resonance, with a peak-to-valley ratio of ~4:1 occuring at 77K, as shown in Fig. 2(b). Room temperature operation should be possible with narrower QWs and a larger ΔE.

Fig. 2(c) shows the source-drain current vs. source-drain voltage (I-V) at several different V_{TC}, with V_{BC}=1.4V. The data was taken at 1.6 K. V_{TC} strongly influences the peak position and peak current. The peak-to-valley ratio is ~10:1. We note that, in contrast to RTDs, a resonance peak occurs only for one source-drain bias polarity. Application of $V_{TC} \leq$ -0.8V changes the sign of the density imbalance, causing the peak to shift to an opposite source-drain bias polarity. Biasing V_{BC} similarly shifts the resonance in the I-V curve.

This unique property of control of the tunneling current by biasing one or more Schottky gates enables a single DELTT to operate as a multiple-input, multifunctional device. As we demonstrate below, a single DELTT can act as a bistable memory cell, a highly compact digital logic element, or a gate-controlled oscillator. Interconnection of multiple DELTTs is expected to further increase functionality.

4. Bistable Memory Cell

Since the I-V curve of a single DELTT exhibits NDR, a hysteresis in the source-drain current vs. V_{TC} is observed when a DELTT is integrated with a properly chosen load resistor. Fig. 3(a) shows the circuit, which has V_{DD}=15 mV and a load resistance of 4 kΩ. Fig. 3(b) shows a sketch of the I-V

curves of the DELTT at three different V_{TC}, along with the load line of the resistor. At intermediate V_{TC} the resistor load line intersects the I-V curve at two stable points (and one unstable point). By sweeping the gate above or below two threshold values, the circuit can be made to have only a single stable point, into which it will latch, as shown in Fig. 3(c). The circuit will then remain in that stable point once V_{TC} is returned to an intermediate value. Thus at intermediate V_{TC} the circuit state depends on its past history, meaning it behaves as a bistable memory element. In Fig. 3(d) we show an oscilloscope trace of the circuit current when a triangular wave V_{TC} is applied. The circuit switches to the low or high current state whenever one of the gate thresholds is reached. Elsewhere we demonstrate a bistable memory using two DELTTs in series, biased so that both stable points of the circuit are in an I-V valley of a DELTT. [5] This minimizes the static power dissipation of the circuit, causing it to act much like a unipolar CMOS memory cell, but with only two transistors instead of the usual four.

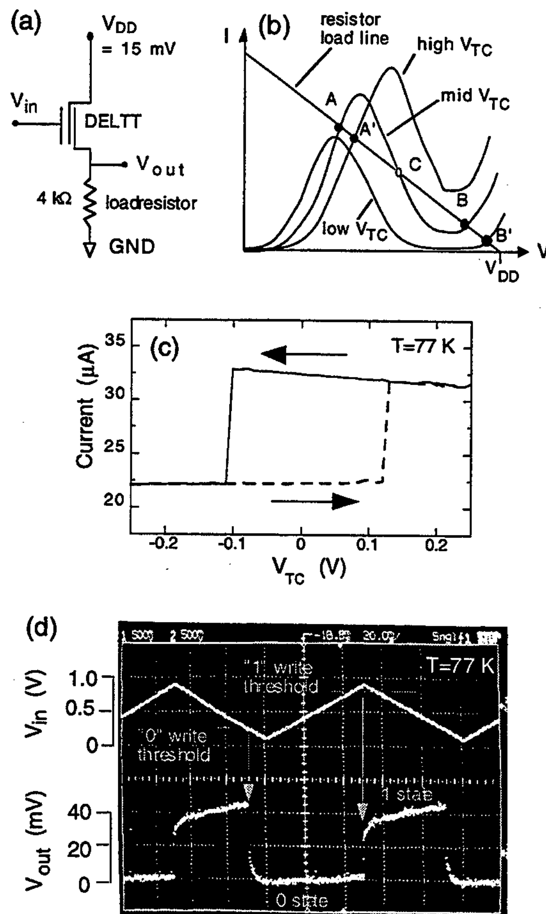

Fig. 3. (a) Bistable memory circuit. (b) DELTT I-V curves for different input gate voltages V_{TC}, and load line of resistor. Stable and unstable points are indicated. (c) 77 K hysterisis of circuit current vs. V_{TC}. (d) 77 K demonstration of memory effect. The memory state switches when the input exceeds one of the writing thresholds.

5. Compact Digital Logic Elements

Due to the gate-tunability of the tunneling resonance, various digital logic functions can easily be implemented using a single DELTT. Figure 4(a) shows a circuit which can act as either a NAND or XOR gate, with the particular function determined by the (fixed) value of the back control gate bias V_{BC}. Two inputs, V_A and V_B, are connected by a resistive summing network to the top control gate, and a constant source-drain voltage V_{DD} is applied. The source-drain current constitutes the output, which is monitored. In order to obtain the XOR function, high current must flow when one of the inputs is high, but not when both are high or both are low. This is accomplished by choosing V_{DD} such that the I-V curves behave as sketched in Fig. 4(b). Only when a single input is high does V_{TC} reach an intermediate value, causing the resonant current peak to occur at V_{DD}. In Fig. 4(c) we show an oscilloscope trace of this circuit taken at 77 K, with biasing parameters of V_{DD}=20 mV and V_{BC}=1.2 V. Square wave inputs of 0.7 V amplitude were fed to inputs A and B. (Here we use the sign convention that -0.7 V is high and 0 V is low.) The output clearly shows the XOR function.

Other logic functions can be obtained by simply changing the circuit biasing parameters. For the case V_{BC}=1.2 V, inspection of Fig. 4(b) shows that simply increasing V_{DD} to 40 mV causes the circuit function to change from XOR to AND. The function can also be changed by letting V_{DD} remain at 20 mV, and instead changing V_{BC}. When V_{BC}=0.3 V, the valleys in the I-V curves lift up (not shown) for all but the most negative V_{TC} values. This results in the circuit function changing from XOR to NAND, as shown in Fig. 4(d). This clearly demonstrates that, due to the DELTT's multifunctionality, a single device can be operated as various digital logic elements.

While the devices studied in this work have insufficient gain to produce significant fan-out, they constitute a proof-of-principle of multifunctional logic. By increasing the electron density in QWs and bringing the

gates closer, it is expected that the gain can be increased sufficiently for good fan-out.

6. Gate-Tunable Oscillator

Because the DELTT exhibits NDR in its I-V characteristics, it can be made to oscillate by choosing a load line which intersects only the NDR region of the I-V curve, producing a single *unstable* operating point. Unlike RTDs, the DELTT has the additional advantage that the oscillator behavior can be switched on and off via well-isolated control gates. Fig. 5 shows the generation of oscillating output when V_{DD}=26 mV. The top two traces are pulsed inputs to the top and bottom control gates, respectively. The bottom trace is the output current from the device. Depending on the gate inputs, the oscillation is turned on or off. Since the control gate area of this device is quite large (200x500μm²), the low oscillation frequency is determined by the large gate capacitance and resulting high RC time constant. With intrinsic tunneling times of order 1 ps, devices with gate areas of a few μm² should oscillate at microwave frequencies.

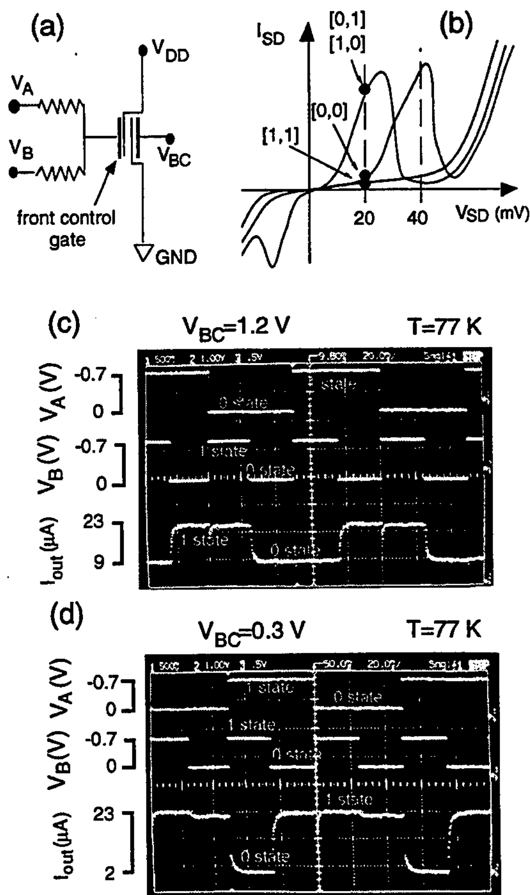

Fig. 4. (a) Digital logic circuit with dual inputs. V_{BC} selects the logical function. (b) Sketch of circuit current vs. V_{SD}, for the different input combinations, at V_{BC}=1.2 V. For V_{SD} = 20 mV, the function is XOR, while for V_{SD}=40 mV the function is AND. (c) 77 K demonstration of XOR function for V_{BC}=1.2 V and V_{SD}=20 mV. (d) When V_{BC}=0.3 V, with V_{SD} unchanged at 20 mV, the function changes from XOR to NAND.

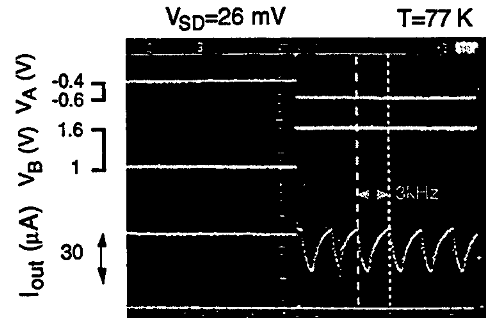

Fig. 5. Demonstration of gate-control of an oscillator. As the gate voltages are varied, the circuit switches from a single stable point to a single unstable point, turning on the oscillations.

7. Summary

We fabricated a novel multifunctional quantum tunneling transistor whose structure is entirely planar. Its operating principle is based on the gate-control of 2D-2D resonant tunneling. Using a single device at 77 K, we demonstrate a bistable memory, digital logic elements such as XOR and NAND gates, and a gate-controlled oscillator.

8. References

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Photoluminescence studied of $In_{1-x}Ga_xAs/GaAs$ quantum dots in high magnetic fields up to 45 Tesla

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Abstract-We report photoluminescence measurement on $In_{1-x}Ga_xAs/GaAs$ quantum well and dots grown on (111)B GaAs substrate in high magnetic fields up to 45 Tesla. A well-defined PL line with half width at half maximum of approximately 5.5 meV is observed. From an analysis of the zero field transition energy, we point out the importance of an internal piezoelectric field to this observation. By analyzing the diamagnetic shift of the PL peak energy in both Faraday and Voigt configurations, the optical characteristic of a quasi-zero dimensional exciton is discussed.

I. INTRODUCTION

Following the progress of the growth technique, the structure of a semiconductor has moved from the two dimensional quantum well to a zero dimensional quantum dots. This structure has attracted great attention not only for its potential application in laser devices but also from fundamental physical point of view where carriers are spatially confined by three dimensional potential [1,2]. It has been investigated both by experimental study and theoretical modeling. The optical measurements includes, temperature dependence the photoluminescence spectrum of InAs/GaAs quantum dots [3], Zeeman splitting of the InGaAs/GaAs quantum dots [4] and exciton diamagnetic shift of self-formed InAs/GaAs quantum dots [5] etc.. The theoretical modeling simulates the optical transition of the quantum dots containing one, two, and a few electrons in a parabolic or a spherical shape potential [6,7,8]

In most of experimental studies, the dots are grown on a (100) oriented substrate and the measurements are conducted at low magnetic field (B<15 Tesla). The luminescence spectrum from these samples is generally wide (~20 meV) due to the inhomogeneity of the dots size and shape. At low magnetic fields, the excitonic energy shift is small. Thus it introduce an uncertainty in interpretating the data.

In this paper, we report photoluminescence (PL) measurements on $In_{0.25}Ga_{0.75}As/GaAs$ quantum well and dot growth on high index plane of GaAs (111)B in high magnetic fields up to 45 Tesla. A well defined spectrum originated from the quantum dots with a half width at half maximum (HWHM) of approximately 5.5 meV is observed at zero magnetic field. This is attributed to the effect of piezoelectric field. In magnetic field, there is a large quantitative difference of the energy shift of the QD between the Faraday and Voigt configuration. From an analysis of the data, we conclude that the PL reflects a transition from un-screened electron-hole pair.

II. EXPERIMENTAL

Luminescence was excited using a solid state laser at an energy of 1.8eV utilizing its full power of 15 mW. The emission signal is collected by using a fiber bundle. This signal was analyzed using a 0.25m spectrometer and a nitrogen cooled CCD detector. The measurements were conducted at 4.2K using a long period pulsed magnetic field with a duration of approximately 15ms.

The sample was grown by molecular beam epitaxy (MBE) with three solid sources of In, Ga, and As. The growth rates of the sources were all measured using the reflection high-energy electron diffraction oscillation spectroscopy. Using this technique the fluxes of indium and gallium were adjusted so that the nominal In fraction in each layer would be close to 0.25. The sample was grown on undoped (111)B GaAs substrate at a temperature of 590 C. The sequence of layers deposition is as following: (a) a 3500 Å GaAs buffer, (b) $In_{0.25}Ga_{0.75}As$ quantum well (QW), (c) 3500 Å GaAs spacer layer, (d) $In_{0.25}Ga_{0.75}As$ quantum dots follows by a capping layer of GaAs. The nominal thickness of the QW and dots is 15 Å. The dots are formed by coherently strain in the layer with a diameter of approximately 500 Å measured by atomic force microscope.

III. RESULTS AND DISCUSSIONS

The zero field spectra is plotted in figure 1. It shows two lines at energy of 1448.4 meV and 1479.5 meV. These transitions are far above the unstrained bulk $In_{0.25}Ga_{0.75}As$ band gap of 1152.8meV ($E(In_xGa_{1-x}As)=1.519-1.538x+0.475x^2$ [9]). Therefore, the observed transitions originate from the dots and

quantum well. To differential the two signals, the sample are wet etched to the thick GaAs layer(the layer between QW and QD). The PL signal from this etched sample gives a transition at 1479 meV and 1519 meV corresponding to the QW and bulk GaAs transitions. Therefore we assign the high and low energy lines observed in the un-etched sample as transition from the quantum well and dots. Since PL is probing the lowest in transition energy, therefore the features is arised from the radiative recombination between the ground state of the conduction (E1) and valence band (H1) labbled as 1s HH.

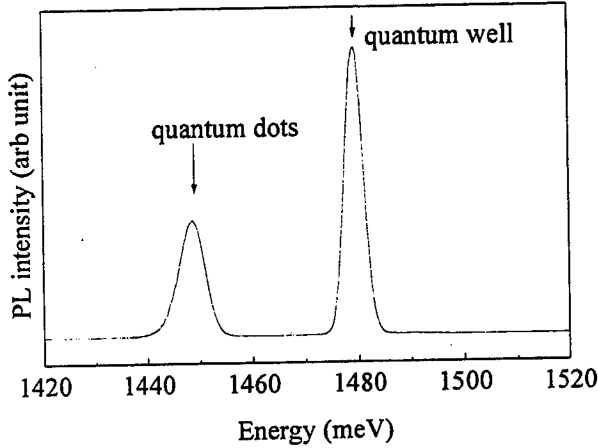

Figure 1: PL spectrum at zero field showing the assignment of the transition from quantum dots and quantum well.

In comparison with the data that has been reported, The two PL lines are extremely sharp with a half width at half maximum (HWHM) of 4 and 5.5 meV for QW and QD respectively. Considering the narrow well width of approximately 15 Å, this is somehow unexpected due to the fluctuation of layer width. We will discuss this later. First, the optical transition is analyzed. Using the flat band excitonic model of [10], the transition energy of the QW is calculated as a function of well width and indium concentrations. The mass parameters for the conduction band is $m_e(In_xGa_{1-x}As)=0.0665-0.0435x$ [11]. For the valence band, Luttinger parameters for GaAs and InAs is used, and are linearly interpolated for the alloy. Since the In concentration is high, giving a larger lattice mismatch about 1.8%, therefore the strain effect needs to be included. In the (111)B orientation, the energy shift of band edge of conduction and valence band due to the strain is [12].

$$\Delta E_c = a_c \varepsilon_{xx} \qquad (1)$$
$$\Delta E_v = a_v \varepsilon_{xx} + 2\sqrt{3}\, d\, \varepsilon_{xy}$$

where ΔE_c, ΔE_v are the energy shift of CB and VB respectively. a_c, a_v and d are the deformation potential and its values are taken from reference [11,12]. ε_{ii}, ε_{ij} are the diagonal and off-diagonal components of the strain tensors.

The results of the calculation are plotted in Figure 2. Using the nominal growth parameters of indium concentration of 25% and well width of 15 Å gives a transition energy of 1421 meV. This is far below the observed value of 1479.5 meV. To increase the transition energy, the indium concentration is reduced to 15%. This gives an energy of 1445 meV. This value, still, is too low in energy to fit the data. Therefore, other factors have to be encounted for. As the sample was grown on (111)B substrate, the non off-diagonal elements of the strain tensor ε_{ij} give rise to an internal piezoelectric field pointing from A(cation) to B(anion). The strength of the field can be estimated from [11]

$$F = 2\, e_{14}\, \varepsilon_{xy} / \varepsilon\, \varepsilon_0 \qquad (2)$$

where e_{14} is the piezoelectric constant, ε_0 the free space permittivity and ε is the dielectric constant. For a 1.8% lattice mismatch (indium concentration of 25%), equation (2) predicts a built-in field of 3.6 times 10^7 V/m. This gives a linear potential drop of 54 meV across the band edge in the well resulting in a triangular shape of the potential profile for both CB and VB. The carriers are therefore become more strongly confined in the well region. This lead to a larger confinement energy [13,14]. Hence the observed transition energy is higher then that predicted. A similar argument also apply for the QD structure. The energy level of a electron(hole), located away from the bottom of the triangular conduction (valence) band, is thus less sensitive to the side fluctuation of the structure. This lead to a rather sharp PL line width in the system studied in this report.

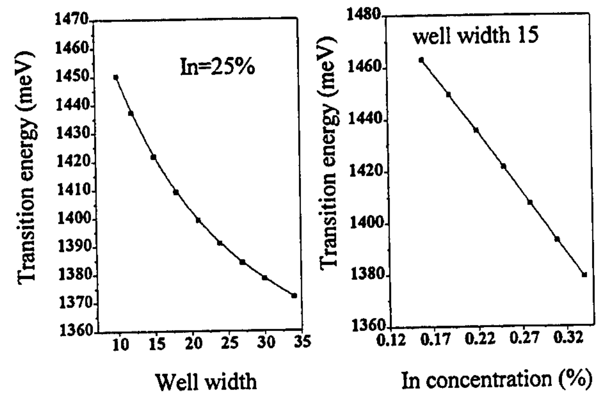

Figure 2: Calculated transition as a function of well width (left plot) and indium concentration (right).

Comparing the PL transition of QW and QD, the

transition from the dots fall below about 30meV. Since the carriers in a QD are confined in the layer plane (x-y plane), therefore the drop in energy is attributed to the variation of the height of quantum dots during growth.

Next, we move to discuss the field-dependent spectra. The field-dependent spectra for both field geometries is plotted in figure 3 and the transition energies are summarized Figure 4. In a magnetic field, the energy shift of the excitonic energy level is determined by Coulomb interaction and the cyclotron energy. The optical characteristics of the excitonic transitions in a quantum well system can be categorized into two regions: (a) low magnetic fields: In this regime, the Coulomb interaction dominates over the magnetic interaction. Therefore the effect of the magnetic field can be treat as a perturbation. To a good approximation, the diamagnetic shift is

$$\Delta E_{dia} = e^2 \langle r^2 \rangle B^2 / 8 \mu c^2 \quad (3)$$

The excitonic transitions move parabolically with fields. (b) High fields regime, as fields increase, the cyclotron energy increases. the Coulomb binding energy becomes less important. Thus the energy shift is dominated by the free carriers cyclotron energy ($heB_\perp/2\pi m$ where $B_\perp$ is the perpendicular magnetic field component). The optical transition is therefore moves linearly with fields.

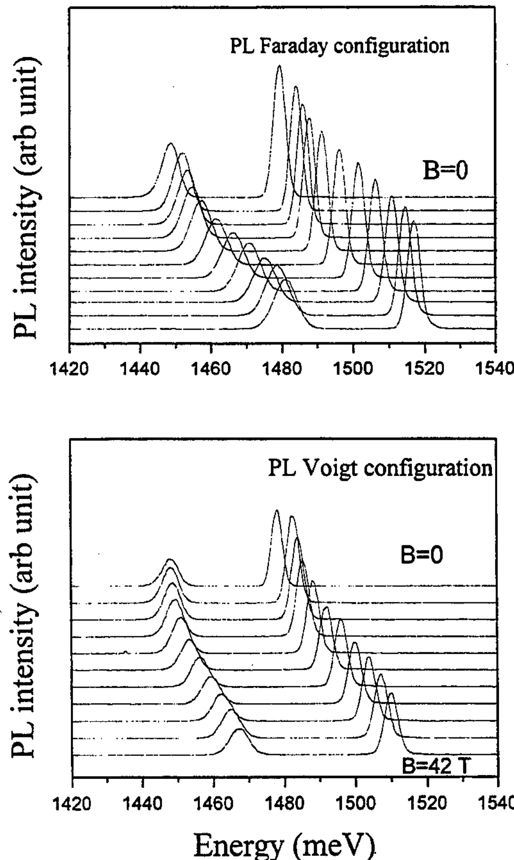

Figure 3: Field-dependent PL spectra in Faraday (upper plot) and Voigt (lower plot) configurations.

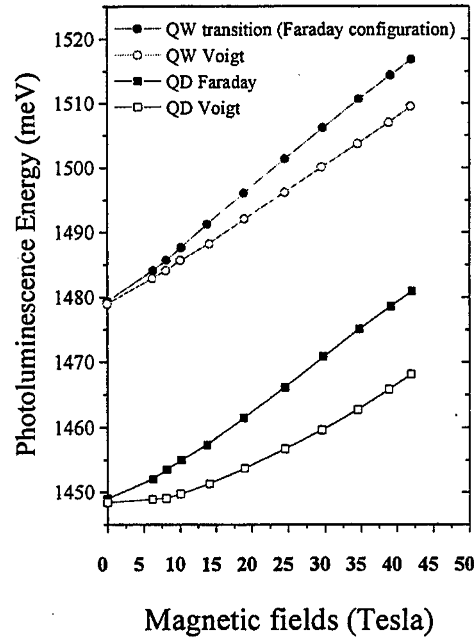

Figure 4: The PL energy of quantum well and dots in both Faraday and Voigt configurations. The solid line is a guide for eye.

We first discuss PL in Faraday configuration (B parallel to the growth direction). At low magnetic fields, the PL from QW and QD move quadratically in fields as expected. Above 15 Tesla, both PL lines move linearly with fields at a rate of 0.92 meV/T and 0.83 meV/T for the QW and QD respectively. By 42.3 Tesla, it shift upward by 37 meV and 29 meV. The smaller diamagnetic shift of the QD reflects a larger excitonic Rydberg energy. As we have discussed before, the thickness of the dots in the growth direction is larger then the width of the QW. Therefore, the extra binding energy is contributed from the lateral confinement (x-y direction). Thus it provides a strong evidence that the exciton are spatially confined by a three dimensional potential. Since the diameter of the dots is wide (~500 Å) in comparison with the Landau cyclotron radius, we conclude that the carrier wavefunctions are concentrated within the spatial extent of dots. Hence the observed transition is originated from a zero dimensional states.

In Voigt configurations, as the magnetic fields are applied perpendicular to the growth direction, it shrink carrier wavefunctions in the growth direction introducing an additional confinement effect. Both PL lines fall below the corresponding Faraday trace reflecting an enhancement of excitonic binding energy. For the QW transition, it follows each other closely at low fields and gradually depart linearly at high fields. The rate of the transition is 0.74 meV/T. For the QD, a

very different behaviour is observed. The PL peak energy remains nearly unchanged up to 10 Tesla and move non-linearly with increasing fields. In comparison with the corresponding Faraday trace, it shift about half the amount.

The highly parabolic energy shift of the QD, especially in the Voigt PL, indicates a suppression of free-carriers characteristic and the PL comes from an excitonic radiative recombination. Considering the low excitation power used in this measurement (15 mW) and the dots density of the sample, to a good estimation, each dot contains one exciton. Therefore, the screening effect and particle correlations is negligible leading to an observation of the single particle energy level of the dots [16.17].

In summary, photoluminescence has been employed to study the optical characteristic of InGaAs/GaAs quantum dots. A narrowest PL line that has been reported is observed. This is attributed to the built-in piezoelectric field in which it localized carriers. We presented the experimental observation of the energy level of single electron-hole state in a quantum dots. This is useful in understanding the optical and magnetic properties of the quantum dots structure. Since the diamagnetic shift is larger at high fields, thus the data is particular sensitive to deduce the exciton reduced mass in a quantum dot.

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FEM Self-Consistent Simulations of Vertical Quantum Dot Structures.

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Abstract

We present a model for calculation of the electronic properties of a vertical quantum dots structures in a regime where the energy level separation is comparable to or larger than the Coulomb charging energy at low temperature. We use a full 3D self-consistent Poisson-Schrödinger simulation to compute the quantized energy spectrum of the entire nanostructure. The structure is discretized using finite element method which appears to be more flexible than the finite difference method, allowing the use of unstructured mesh.

1 Introduction

Quantum dots are often called artificial atoms because they share features such as shell structure in their energy spectrum and discretenes of the charge. Such features were observed in recent experiments by Tarucha and coworkers [3][4] [5], using a gated submicron double-barrier resonant tunneling structure (Fig 1).

We have tried to develop a realistic model to confirm these observations. Moreover, we have explored new numerical schemes in order to circumvent drawbacks inherent to those traditionally used.

The major drawback of finite differences is that the method can only deal with structured grids, where a point is uniquely determined by a triplet (i, j, k) (assuming 3D simulations). Therefore, we have switched from the difference method to the finite element method. That is, instead of taking a finite number of points, and replacing derivatives by differences, we choose a finite number of piecewise polynomials, such that the pieces can be chosen to fit the geometry of the problem, and approximate the exact solution by a combination of these trial functions.

In order to keep the mesh uniformity all over the structure, the best compromise is achieved by an unstructured grid. This type of mesh cannot be dealt by finite differences, but by finite elements.

Regarding the eigenvalue solver, we have noticed that with the IEOM method traditionnally used in our group, most of the computational time has been spent in the Gram-Schmidt orthogonalization procedure. To avoid this overhead, we use a method that still belongs to the subspace iteration method family, but, instead of iterating on the eigenvectors, we iterate on the subspace[1].

2 Model

2.1 Poisson equation

In the finite element formulation, instead of solving Poisson's equation directly, one approximates the weak form :

$$\int_\Omega \nabla \cdot (\varepsilon \nabla \phi) \, W \, d\Omega = - \int_\Omega \rho(\phi) \, W \, d\Omega \qquad (1)$$

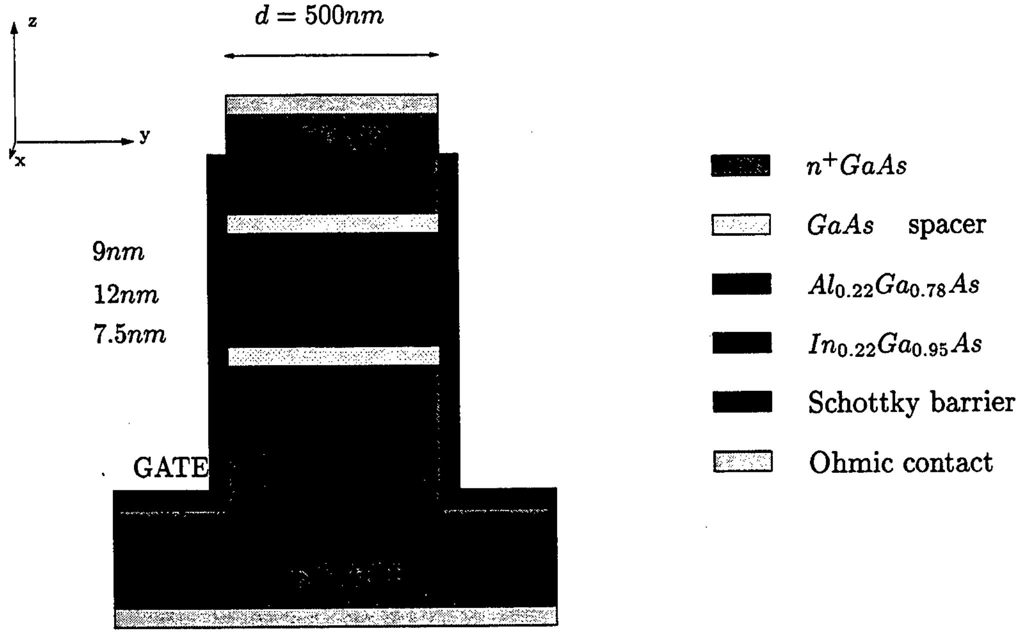

Figure 1: vertical quantum dot structure schematics

where one multiplies the differential equation by a test function W and integrate over the volume Ω of our device. We have approximated ϕ in each elementary hexahedron by $\tilde{\phi} = \sum_{i=1}^{8} N_i(x,y,z)\ \phi_i$, where $N_i(x,y,z)$ is a trilinear polynomial and ϕ_i the value of the potential at node i. Choosing 8 different test functions $W_i = N_i$ (Galerkin method), we obtain a system of 8 equations with 8 unknowns ϕ_i. Replacing ϕ by $\tilde{\phi}$ in (1), integrating by parts , and summing over all the hexahedra of the volume, yields in the matrix formulation :

$$[K]_P\ \{\phi\} = \{R\} \tag{2}$$

where $[K]_P$ is the $n \times n$ stiffness matrix, easily showen to be symmetric positive definite (n being the total number of nodes), with
$K_{ij} = \varepsilon \int_\Omega \left(\frac{\partial N_i}{\partial x}\frac{\partial N_j}{\partial x} + \frac{\partial N_i}{\partial y}\frac{\partial N_j}{\partial y} + \frac{\partial N_i}{\partial z}\frac{\partial N_j}{\partial z} \right) d\Omega$. $\{\phi\}$ is the potential and $\{R\}$ is the right hand side vector with $R_i = \int_\Omega \rho N_i d\Omega$, with $\rho = q[p(r) - n(r) + N_D^+(r) - N_A^-(r)]$. $p(r)$, $n(r)$, $N_D^+(r)$ and $N_A^-(r)$ are the hole, electron, ionized donor and ionized acceptor concentrations, respectively.

We can take advantage of the sparsity of $[K]_P$ to solve (2) iteratively by the preconditioned gradient method.

2.2 Schrödinger equation

The same procedure, applied to the one particle Schrödinger equation, leads to the generalized eigenvalue problem :

$$[K]_S\ \{\psi\}_i = \epsilon_i\ [M]\ \{\psi\}_i, \quad i = 1 \cdots n \tag{3}$$

Again, $[K]_S$ is the Schrödinger stiffness matrix and is the discretized form of the integral of the Hamiltonian:

$$\hat{H} = -\frac{\hbar^2}{2}\nabla\left[\frac{1}{m^*(\mathbf{r})}\nabla\right] + E_c(\mathbf{r}) + E_{xc}(n) \tag{4}$$

where $m^*(\mathbf{r})$ is the position dependent effective mass of the electron in the different materials, $E_c(\mathbf{r}) = \phi(\mathbf{r}) + \Delta E_{os}$, is the conduction band edge, where $\phi(\mathbf{r})$ is the electrostatic potential, ΔE_{os} is the conduction band offset, and $E_{xc}[n]$ is the exchange and correlation potential computed by LDA. $\{\psi\}_i$ are the eigen-

vectors, ϵ_i are the eigenvalues and $[M]$ is called the mass matrix.

(3) is an n-dimensional problem but if we are only interested in the first q eigenvalues, with $q \ll n$ (usually around 20), we find the q-dimensional subspace spanned by the q eigenvectors corresponding to the lowest q eigenvalues by the following procedure:

(a) Choose a set q of linearly independent vectors as an initial guess for the basis of the subspace

(b) Find the projections of $[K]_S$ and $[M]$ onto the subspace.

(c) Using any transformation method, find the q eigenvalues of this projected system.

(d) Build a new basis using linear combinations of the eigenvectors of the subspace and go back to (b).

It can be proved that the sequence (b), (c), (d) converges to the desired subspace. It will be noted that Gram-Schmidt orthogonalization is not required since we don't iterate on the eigenvectors but on the subspace.

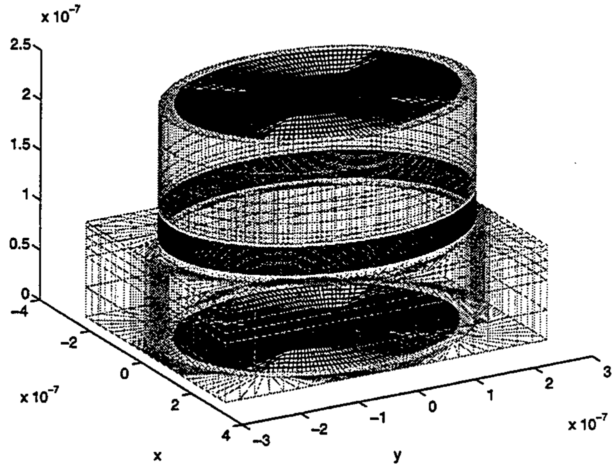

Figure 2: disccretized mesh of the device

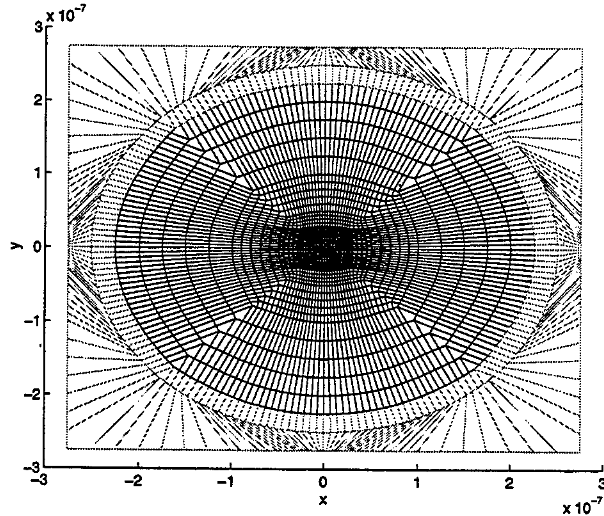

Figure 3: mesh of the device, top view.

3 Results

The device shown schematically in Fig 1 consists of a 12nm undoped $In_{0.05}Ga_{0.95}As$ well, 9.0 and 7.5n undoped $Al_{0.22}Ga_{0.78}As$ barriers and $n-GaAs$ source and drain. A circular schottky gate around the dot region gate allows one to tune the number of electrons inside the dot. The associated mesh is presented on Fig 2 and 3.

The conduction band profile of the structure is presented on Fig 3 and is in good agreement with former calculations [4].

At last, Fig 5 shows the Coulomb staircase, that is, the number of electrons inside the dot with respect to the gate voltage. The various step sizes can be explained by simple electrostatic arguments. The ground and first step correspond to the s state, the last four steps are associated to the two degenerated p states. This explains that the second step is the

widest: it corresponds not only to the energy required to put the third electron in the dot but also to the energy required to bring the p states at the Fermi level. First and second electrons share the same wave function, thus, the Coulomb repulsion is important. According to energy minimization principle, the fourth electron occupies a state orthogonal to the one associated with the third electron. Wave functions overlaping is weak as well as Coulomb repulsion; third step width is then shorter than first. Similar consideration holds for the fourth stair.

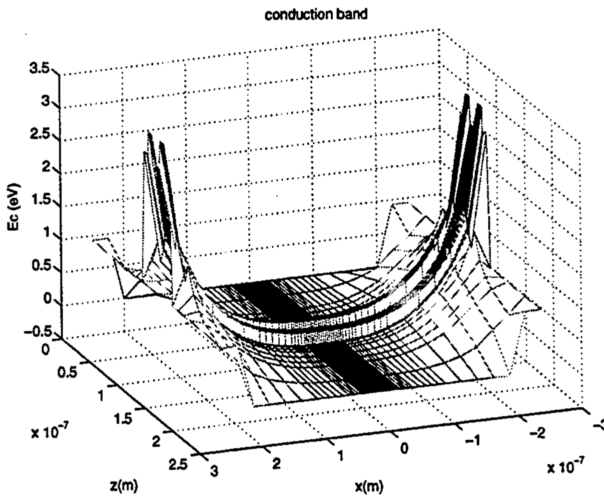

Figure 4: conduction band profile

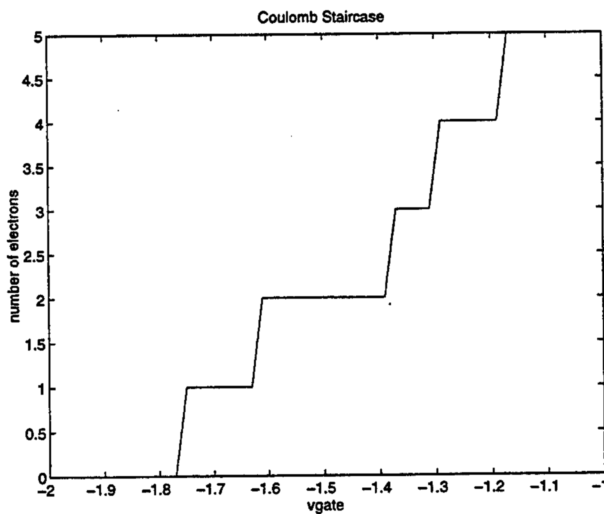

Figure 5: Coulomb staircase

4 Conclusions

We have performed self-consistent Poisson/Schrodinger simulations on a vertical quantum dot structure using the finite element method as dicretization scheme. The evolution of the number of electron in the dot with respect to the applied gate voltage shows good agreement with recent experiments.

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InP BASED HETEROSTRUCTURE DEVICES AT MILLIMETER AND SUBMILLIMETER WAVE-LENTGHS

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This paper deals with recent advances in the design and fabrication of InP-based devices currently used in non-linear electronics at millimeter and submillimeter wavelengths. Devices making use of barrier-quantum well schemes will be more specially addressed with main emphasis on band gap engineering aimed at increasing the device performances in terms of non linear effects, frequency and power capabilities. First of all, from the point of view of device physics, special attention will be paid to the tunneling and quantum-size effects, which play a key role in the current-and capacitance-voltage characteristics of devices and which will be studied on the basis of quantum transmission probability and two-dimensional carrier density calculations. Then from the technological side, some of the challenging issues will be studied and illustrated by the fabrication of high performance planar integrated Resonant Tunneling Diodes (RTD's) and Heterostructure Barrier Varactors (HBV's). At last, we will consider the prospects for terahertz operation and will discuss in what extent the quantum effects involving ultra-fast tunneling and localization effects could be used for alleviating some of the frequency limitations of conventional devices, notably of Schottky's, in mixing, harmonic multiplication and power generation.

ADVANCES IN SUBMILLIMETER SEMICONDUCTOR-BASED DEVICE DESIGNS AND PROCESSES

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Abstract

Planar submillimeter circuits are slowly replacing whisker-contacted devices at frequencies above 100 GHz, but in many cases the size constraints brought on by the short wavelengths associated with high frequency operation have not been adequately addressed. Also, reproducibility becomes more important as we make the transition from tunable, whisker-based circuits to more monolithic designs. We are continuing to develop new circuits and integration techniques to reduce parasitic losses and make monolithic circuits with more reproducible characteristics. New photolithography techniques have been incorporated in our process in the last several months, and the use of better dry-etching equipment is enabling us to better control etching.

We will discuss second-generation designs of our quasi-optic and microstrip MMIC multipliers. Improvements have been made to our processing technology to make dimensions, and thus impedances, more accurate for both the active devices and the passive circuitry. Many of our alignment tolerances between layers need to be much less than a micron, and even passive structures incorporate extensive two micron-sized lines and spaces that must be accurately fabricated. The new designs and preliminary results will be discussed. In addition, a diode array produced about 10 mW with over 20% efficiency at 270 GHz.

We are also fabricating new 2.5 THz mixer diode circuits on membranes with 0.1 micron air-bridged anodes. We plan to have new results for the conference.

Characterization of the Microwave PIN Diode for High Speed Data Modulation

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I. Abstract

An accurate model to characterize a PIN diode as a variable resistor driven by high speed digital data and RF pump signals is presented. The model extracts the electron density function resulting from these signal drives. This is used to obtain a closed form expression for the PIN diode resistance. A high speed reflection pulse amplitude modulator which is an essential block for implementing more complex digital modulators, is also examined using this model.

II. Introduction

DI rect PAM modulation [1] using PIN diode to control the level of RF signal according to the baseband modulating signal offers a number of advantages over the conventional method. In this method, a high speed attenuator, which can be realized using pin diode, is designed to change the level of the RF signal associated with the amplitude of incoming data. The PIN diode has been traditionally used for microwave switches and attenuators. This device is also a common device for the variable attenuators. The recent progress in MMIC technology for silicon devices in microwave millimeter waves [2] as well as growing demand for high speed communications has been made PIN diode very attractive. The on-off mode of PIN diode has already been considered for vector modulators. However, the speed of the attenuator is limited by the hysteresis effect when on-off switching mode is employed[4]. In this mode of operation, when diode condition changes from forward bias to reverse bias, a minimum time is required to clear out the stored charge accumulated during the forward bias state. This time is a function of carrier life time as well as the ratio of the forward bias current to the reverse bias current [5]. This speed limitation can be overcome by operating the PIN diode in the forward bias mode only. Hence, an accurate model is required to characterize the forward biased PIN diode driven by high speed data at the microwave and millimeter frequencies.

The PIN diode has been studied extensively in the literature [4-8]. However, an accurate model that describes the PIN diode in response to high speed data is not available. In this paper the PIN diode operation in response to high speed multilevel data is studied. The residue theorem and complex inversion formula are used to obtain the electron density function. A device model is derived from this density function. The method results in a closed form formula to study the PAM modulator using PIN diode.

III. Analysis

The fundamental equations for PN junction analysis are as follows [6][7]:

$$\frac{\partial n}{\partial t} = D_n \frac{\partial^2 n}{\partial x^2} - \frac{n}{\tau_n} \quad (1)$$

$$\frac{\partial p}{\partial t} = D_p \frac{\partial^2 p}{\partial x^2} - \frac{p}{\tau_p} \quad (2)$$

Assuming a symmetrical structure, electron and hole mobility carriers may be considered to be the same. It is also possible to approximate $\tau_p = \tau_n = \tau$ and define an ambipolar diffusion constant as $D = 2D_nD_p/(D_p + D_n)$. Using this and taking the Laplace transform to Eq.1 , results in:

$$\frac{\partial^2 N(x,s)}{\partial x^2} = (\frac{1+s\tau}{\tau D})N(x,s) \quad (3)$$

where, $N(x,s)$ is the Laplace transform of $n(x,t)$. Eq.3 has the following solution:

$$N(x,s) = k_1 e^{-\sqrt{\frac{1+s\tau}{\tau D}}x} + k_2 e^{\sqrt{\frac{1+s\tau}{\tau D}}x} \quad (4)$$

Using this solution, and considering the PIN diode, shown in Fig.1, is symmetrical, we can assume $N(x,s) = P(x,s)$. For a symmetrical PIN diode it can be shown[3]:

$$N(x,s) = \frac{N(\frac{W}{2},s)}{cosh(\sqrt{\frac{1+s\tau}{\tau D}}\frac{W}{2})} cosh(\sqrt{\frac{1+s\tau}{\tau D}}x) \quad (5)$$

When the PIN diode is forward biased with high speed data, three current component have to be considered. The first component is a DC bias which makes diode to operate under forward bias condition. The second component arises from the incoming data signal that is used to control the level of attenuator. The last current component is the RF current component at the frequency ω_o. Under higher power operation, the RF signal harmonics have to be considered as well. Thus, the total current in the PIN diode may be expressed [3]:

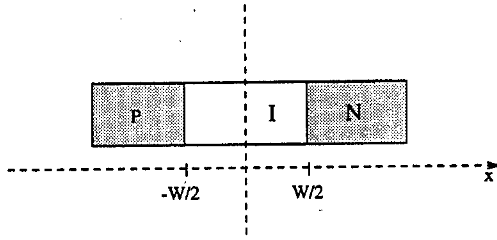

Fig. 1. The PIN diode structure

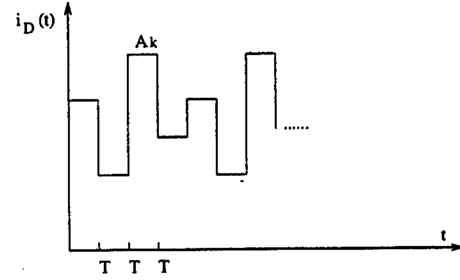

Fig. 2. A two level data sequence

$$N(x,s) = \frac{\cosh(\sqrt{\frac{1+s\tau}{\tau D}}x)}{2AqD\sqrt{\frac{1+s\tau}{\tau D}}\sinh(\sqrt{\frac{1+s\tau}{\tau D}}\frac{W}{2})}(\frac{I_o}{s}+I_D(s)+I_R(s)). \quad (6)$$

The $N(x,s)$ may be separated into three components as

$$N(x,s) = N_1(x,s) + N_2(x,s) + N_3(x,s) \quad (7)$$

The time domain components of densities are:

$$n_1(x,t) = L^{-1}(N_1(x,s)) \quad (8)$$

$$n_2(x,t) = L^{-1}(N_2(x,s)) \quad (9)$$

$$n_3(x,t) = L^{-1}(N_3(x,s)) \quad (10)$$

The residue theorem and complex inversion formula can be used to obtain these components.

A. DC Response

The DC current is used to ensure that the diode operates in forward bias condition only. The Laplace transform of electron density resulting from the DC current $N_1(x,s)$is given by:

$$N_1(x,s) = \frac{\cosh(\sqrt{\frac{1+s\tau}{\tau D}}x)}{2AqD\sqrt{\frac{1+s\tau}{\tau D}}\sinh(\sqrt{\frac{1+s\tau}{\tau D}}\frac{W}{2})}\frac{I_o}{s} \quad (11)$$

To obtain the residues, an integration contour with radius Z_m may be considered as follows :

$$Z_m = (m+\frac{1}{2})(\frac{1}{\tau}+D(\frac{2m\pi}{W})^2) \qquad m = integre \quad (12)$$

This choice for Z_m insures that the contour does not pass through any of the poles [9]. Now, we can obtain the residues $F_1(x,s)e^{st}$ for different poles.
For $s=0$, the residue R_o is given by [3]:

$$R_o = \sqrt{\tau D}\frac{\cosh(\frac{x}{\sqrt{\tau D}})}{\sinh(\frac{W}{2\sqrt{\tau D}})} \quad (13)$$

The residue for $s = s_k, k = 1,..,$ poles are given by:

$$R_k = \frac{4D\cos(\frac{2k\pi}{W}x)e^{-[\frac{1}{\tau}+D(\frac{2k\pi}{W})^2]t}}{W\cos(k\pi)(-\frac{1}{\tau}-D(\frac{2k\pi}{W})^2)} \qquad k = 1,2,...,m \quad (14)$$

The only pole left in equation is the second order pole at $s = -\frac{1}{\tau}$ and it is a second order pole. A simple result for R' is obtained as [3]:

$$R' = -\frac{2D\tau}{W}e^{\frac{-t}{\tau}} \quad (15)$$

Using residue theorem, the electron density function corresponding to the DC current can be shown as[3]:

$$n_1(x,t) = \frac{I_o}{2AqD}(\frac{\sqrt{\tau D}\cosh(\frac{x}{\sqrt{\tau D}})}{\sinh(\frac{W}{2\sqrt{\tau D}})} - \frac{2D\tau}{W}e^{-\frac{t}{\tau}} +$$

$$\sum_{k=1}^{\infty}\frac{4D\cos(\frac{2k\pi}{W}x)e^{-[\frac{1}{\tau}+D(\frac{2k\pi}{W})^2]t}}{W\cos(k\pi)[-\frac{1}{\tau}-D(\frac{2k\pi}{W})^2]})(16)$$

As may be seen from Eq.16, as t tends to infinity, the second and third components approach zero and the electron density after transition time can be obtained from the first term. This is consistent with the well known steady state relation [4]. The second and third terms also show that diode operation in the on-off mode is limited to slow speed operation only.

B. Data Response

A PAM sequence with period T is considered as the data signal. This current generates the component $n_2(x,t)$.Such a signal is shown in Fig.2 and it can be expressed as:

$$i_D(t) = \sum_{k=0}^{\infty} A_k(u(t-kT) - u(t-(k+1)T)), \quad (17)$$

where A_k is the amplitude of signal. The Laplace transform of this signal is given by:

$$I_D(s) = \sum_{k=0}^{\infty}\frac{2A_k}{s}e^{-kTs}\sinh(\frac{sT}{2}), \quad (18)$$

Hence, this component of density function is given by [3]:

$$N_2(x,s) = \frac{1}{2AqD}(\frac{cosh(\sqrt{\frac{1+\tau s}{\tau D}}x)}{\sqrt{\frac{1+\tau s}{\tau D}}sinh(\sqrt{\frac{1+\tau s}{\tau D}}\frac{W}{2})}$$

$\sum_{k=0}^{\infty} \frac{2A_k}{s} e^{-skT} sinh(\frac{sT}{2}))(19)$

Using final value theorem,
$lim_{t\to\infty} n_2(x,t) = lim_{s\to 0} sN_2(x,s)$, the electron density function because of data level variations is estimated as:

$$lim_{t\to\infty} n_2(x,t) = 0 \tag{20}$$

It may be easily seen that there is not electron density due to this signal when $t \to \infty$. This shows that the forward bias operation doesn't impose limitation on the speed PIN diode operations. These interesting results can be used to design the high speed multilevel digital modulators[1].

C. RF Response

The electron density for the third component of the current, i.e. RF current, can also be computed in a similar way. We consider an RF signal with only a sinusoidal component which may be expressed as:

$$i_{RF}(t) = Bcos(\omega t) \tag{21}$$

The Laplace transform of this signal is:

$$I_r(s) = \frac{Bs}{s^2+\omega^2}, \tag{22}$$

where, B is the amplitude of sinusoidal and ω is its frequency. This component of current results in the third component of the electron density. This component can be written as follows [3]:

$$n_3(x,t) = \frac{B}{2AqD}(\frac{cosh(\sqrt{\frac{1+j\omega\tau}{\tau D}}x)e^{j\omega t}}{2\sqrt{\frac{1+j\omega\tau}{\tau D}}sinh(\sqrt{\frac{1+j\omega\tau}{\tau D}}\frac{W}{2})} + \frac{cosh(\sqrt{\frac{1-j\omega\tau}{\tau D}}x)e^{-j\omega t}}{2\sqrt{\frac{1-j\omega\tau}{\tau D}}sinh(\sqrt{\frac{1-j\omega\tau}{\tau D}}\frac{W}{2})} -$$

$$\frac{2D}{W\tau}\frac{e^{\frac{-t}{\tau}}}{(\frac{1}{\tau})^2+\omega^2} +$$

$$\sum_{k=1}^{\infty}\frac{4D(\frac{-1}{\tau}-D(\frac{2k\pi}{W})^2)cos(\frac{2k\pi}{W}x)}{Wcos(k\pi)[(\frac{-1}{\tau}-D(\frac{2k\pi}{W})^2)^2+\omega^2]}e^{-[\frac{1}{\tau}+D(\frac{2k\pi}{W})^2]t})$$

As may be seen, this density component includes a harmonic term and two transient terms. Factor ω at denominator shows that in the higher frequency operation these two transient terms disappear rapidly.

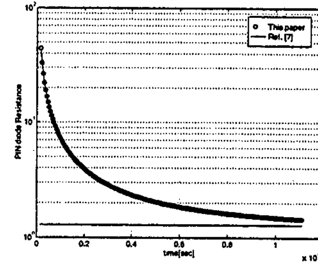

Fig. 3. The pin diode forward bias resistance with I=1 mA

D. Pin Diode Voltage

The total electron density, $n(x,t)$, is consists of three components and is given by:

$$n(x,t) = n_1(x,t) + n_2(x,t) + n_3(x,t) \tag{23}$$

Using Ohm's law, the the pin diode voltage may be written as:

$$v(t) = \frac{i(t)}{A\mu q}\int_0^{\frac{W}{2}} \frac{dx}{n(x,t)} \tag{24}$$

IV. Numerical Simulation

A. Forward Biased resistance

The model was applied to study the response of a cylindrical pin diode with radius $r = .78mm, \mu = .061m^2/V, D = 15.6\times10^{-4}cm^2/s, \tau = 5\times10^{-6}sec, W = 28\mu m$. As a first step, the PIN diode is considered to operate in its linear region without any bias variation (only a constant DC bias), and it is assumed that no RF signal is applied to the diode. The DC current values is assumed 1mA. The results obtained from our model were compared with the previously reported results [4]. As may be seen in Fig.3, the final value of the pin diode resistance approaches the well known results; however, the resistance value in transition time is much higher than its final value. It is an important factor that limits the PIN diode speed as a data modulator for on-off operation. For instance, for diode understudy(as seen from Fig.3), the maximum speed of data modulation in on-off mode is less than 100 kbps.

B. PIN diode as high speed PAM modulator

B.1 Basic Structure

The model developed above was used to study a basic multilevel PAM modulator. This circuit is shown in Fig.4. An RF signal with peak value of 1 volt and frequency of 2.5 GHz is applied to circuit. The data rate was selected to be 40 Msym/sec and data level symbols corresponding to the derive current ,.1, .3, .5, and 1 mA were applied to the diode. The diode always operates in forward biased condition. To avoid the transition time behavior , the circuit is studied after .04 msec. The PIN diode resistance because

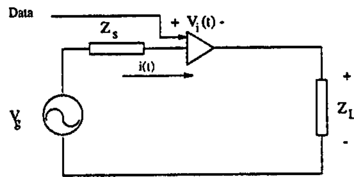

Fig. 4. Basic structure to study the PIN diode modulator

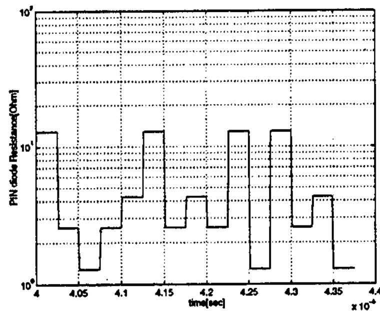

Fig. 5. Pin diode forward biased resistance

of data drive is shown in Fig.5. The PIN diode voltage is obtained using Eq.24 and is shown in Fig. 6. As may be seen, the net dc level of current controls the resistance of the PIN diode in forward bias mode, and level variation doesn't impose any limitation on modulator performance.

B.2 High Speed Reflection PAM Modulator

The model also developed above was next used to study a reflection multilevel PAM modulator. This is an essential block in a high speed multilevel modulator[1]. The circuit block consists of two PIN diode derived by high speed data and a Lange coupler as shown shown in Fig.7. A multilevel baseband PAM signal is used as the drive current for the PIN diode while an RF signal pumps the power in the modulator. Again, in this experiment, the data rate was selected 40 Msym/sec and pump frequency was selected to be 2.5 GHz with peak amplitude 1 volt. A four level data symbols corresponding to the drive current, .1, .3, .5, and 1 mA is applied to diode. The PIN diode voltage is shown in Figure 8. The output voltage of reflection modulator is shown in Fig.9. As may be seen, a high performance modulator has been implemented using this configuration.

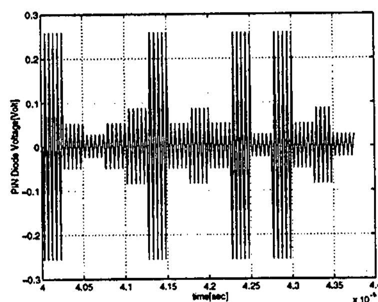

Fig. 6. Pin diode voltage in the basic structure

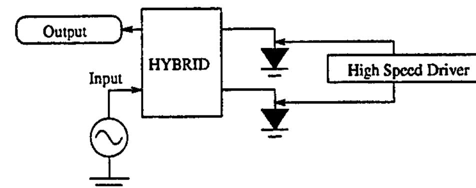

Fig. 7. A reflection multilevel PIN diode PAM modulator

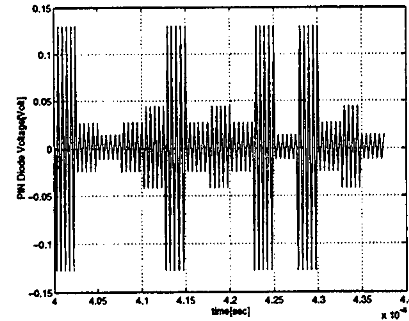

Fig. 8. Pin diode voltage in the reflection modulator

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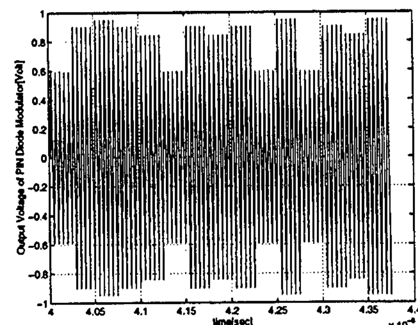

Fig. 9. Reflection modulator Output

OPTICAL COUPLING AND CONVERSION GAIN FOR NbN HEB MIXER AT THz FREQUENCIES

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I. INTRODUCTION

NbN Hot Electron Bolometric (HEB) mixers represent a promising approach for achieving receiver noise temperatures of a few times the quantum noise limit at frequencies above 1 THz. These HEB mixers have so far demonstrated a DSB noise temperature as low as 500 K at 630 GHz [Kroug et al., 1997; and others], and 980 K at 900 GHz [Kroug et al., 1997]. Noise temperatures of about 1000 K or less can be expected for frequencies above 1 THz in the future. NbN HEB mixers have been shown to have sufficient bandwidths for the anticipated applications such as future receiver frontends for THz astronomical observation from space. A receiver noise bandwidth of 5 GHz and a conversion gain bandwidth of 3 GHz were measured by [Ekström et al., 1997]. The LO power required is typically 100 nW, which makes NbN HEB mixers suitable for use with future solid state tunable THz sources. However, the LO power is not at such a low level, as to cause the device to saturate by thermal radiation. This paper describes the development of a 2.5 THz HEB mixer, employing NbN, and our first results from measurements with this mixer.

II. DEVICE DESIGN AND FABRICATION

NbN Films

The NbN films were fabricated on silicon substrates at Moscow State Pedagogical University (MSPU) by magnetron reactive sputtering in an argon/nitrogen gas mixture. For this work we have primarily used films of thickness 3.5-4 nm in order to maximize the conversion gain bandwidth. The production of such thin films is presently still an evolving technology, but recent films on both sapphire and silicon substrates have shown much improved properties [Cherednichenko et al., 1997]. The optimum thickness, based on the sapphire work, appears to be close to 3.5-4 nm [Cherednichenko et al., 1997]. The films used for the devices we have tested so far have T_c = 7.5 - 9 K and the transition width is about 1 K.

Optical Design

Optical design considerations are crucial for efficiently coupling LO and signal power into the device. It is clear that quasi-optical coupling to the device is the only alternative for frequencies as high as 2.5 THz. We chose to use an extended hemispherical silicon lens coupled to a log-periodic spiral antenna (see Figure 1), as successfully demonstrated and analyzed at 250 GHz and 500 GHz by [Filipovic et al, 1993]. The log-periodic spiral antenna is convenient at this stage since it can be used over a very wide frequency range; later versions will employ twin-slot or twin-dipole antennas tuned to specific frequencies. We scaled the di-

mensions of the lens and the antenna used in the 250 GHz setup by a factor of ten, resulting in a lens diameter of 1.3 mm. We chose an extension length, beyond the hemispherical lens, of 0.33 times the lens radius. We can predict the amount of beam-scan which would result from misalignment of the center of the antenna with respect to the center of the lens: a 20 micrometer misalignment results in a 5 degree beam scan. This makes it imperative to use an accurate alignment procedure, which will be described below. We are not employing a matching layer at this stage.

Device Fabrication

Devices have been fabricated at MSPU as well as at UMASS/Amherst. The processes are somewhat different at the two locations, but in what follows we will emphasize the UMASS process. The gold log-periodic antenna is fabricated using liftoff. After the pattern has been defined in the photoresist, a 40 nm thick layer of Nb is applied by sputtering. Next, 20 nm of Ti and 100 nm of Au are deposited by E-beam evaporation, and the liftoff is performed. The NbN strips are then defined and etched using Reactive Ion Etching (RIE). The substrate is thinned by lapping to a thickness equal to the lens extension length. The position of a square alignment window for the lens is then defined in a photoresist layer on the opposite side of the substrate from the antenna and device, using an infrared mask aligner. The alignment window is etched by RIE to a depth of 100nm. The lens is attached to the silicon substrate using purified bees wax. The final dimensions of the device strips are about 0.6 μm long by 1.0 μm wide. The number of strips is from one to three. The mask also has a different pattern for which the smallest teeth, which determine the highest frequency of the antenna, are twice as large, i.e. the highest frequency is 1.25 THz. This antenna can have up to five strips. Figure 2 shows an SEM picture of a device with four strips, recently fabricated at UMASS/Amherst.

III. EXPERIMENTAL SETUP

Optical Setup

The optical coupling loss as well as the receiver noise temperature are measured with a CO_2 laser pumped FIR methanol laser as the LO source. A 1 mil mylar beam splitter acts as a diplexer between the LO and a chopped hot/cold noise source. The cooled IF amplifier has a bandwidth from 1250 to 1750 GHz, with noise temperature less than or equal to 10K. In order to measure the conversion gain directly, we employed two lasers at UMASS/Lowell. The active medium was difluoromethane, and the frequency 1.56 THz. The lasers were slightly detuned and produced an IF of 600 kHz. The IF bandwidth of NbN HEB devices cannot be easily measured at THz frequencies. This measurement requires one fixed source for the RF input, and a tunable source for the LO, or vice versa. The tunable source may be a sideband generator, which produces a tunable sideband from a fixed laser frequency. Future such measurements are being planned with a source of this type at UMASS/Lowell.

IV. RESULTS AND DISCUSSION

Laser Measurements

The best device available for the preliminary measurements was one fabricated at MSPU, which was integrated with a regular spiral antenna. Figure 3 shows three IV-curves for this device. The physical temperature was 4.73 K and T_c was 7.5 K. In the particular case shown, the LO power produced an IV-curve which is almost identical to one recorded at an elevated temperature of 6.8 K (a resistive heater was then used to heat the device). The significance of this observation is that the device is heated to an electron temperature close to T_c by the laser power, as required for optimum mixer operation. The near coincidence of the two

curves is expected since the LO radiation is at a frequency much higher than the superconducting gap frequency; LO heating effects should then produce results close to those due to thermal heating.

The IF power in a 50 MHz bandwidth was measured for three conditions: (i) device superconducting at V=0; (ii) with optimum DC bias but no LO power; (iii) with optimum DC bias and the LO power on. The change in IF power from (i) to (iii) amounted to 8 dB. From these data we can estimate the device output noise temperature (T_{out}) to be in the range 40-80 K. The uncertainty is due to our incomplete knowledge of the amplifier noise temperature. This value of T_{out} is in the expected range.

We were also able to measure the amount of 2.5 THz laser power absorbed by the device, by utilizing the IV-curves. The power absorbed at what would be a typical optimum operating point was in the range 100 nW to 800 nW. The measured laser power after the paraboloid mirror was 2.5 mW. The ratio of these numbers gives an estimate of the total optical coupling loss of 35 dB. FTS measurements indicate that much of this loss may be due to the frequency response of the spiral antenna; similar measurements on the log-periodic spiral antenna show that its response is expected to reach 2.5 THz. We are continuing our experiments to obtain a measurement of the mixer noise temperature. We also expect to improve the optical coupling. We have tested the 1.25 THz version of our log-periodic antenna/device at 620 GHz at Chalmers University of Technology, using a different lens (12.5 mm diameter). The DSB receiver noise temperature was 1000 K, with similar performance at least up to 750 GHz. Fourier Transform Spectrometer measurements of the direct detection response near T_c for the same device indicate broadband coupling from 300 GHz to 1.2 THz, as expected. Our antenna design and device fabrication technology have thus been validated up to 1.2 THz so far.

The intrinsic (device only) conversion gain at 1.56 THz was measured in the two-laser setup to be 3 dB, with a probable error of +/- 2 dB. The absorbed power from the RF laser was obtained by the technique we employed for the absorbed LO power, at a high enough RF power level to make this possible. Calibrated attenuators were then used to lower the RF power until the mixer was shown to be operating in its linear region. The IF power was observed on a spectrum analyzer, and the IF voltage was measured directly on an oscilloscope. The optical coupling loss was estimated to be about 33 dB in this case. Note that HEB mixer theory allows actual conversion gain to be realized. The conversion gain at higher IF frequencies may be somewhat lower; so far, the best intrinsic conversion gain of any HEB THz mixer at about 1 GHz IF, inferred from noise measurements, is about - 6 dB (Kroug et al., 1997).

V. CONCLUSIONS

We have shown that lasers can be quasi-optically coupled at THz frequencies to NbN HEB mixer devices integrated with log-periodic or spiral antennas and small silicon lenses. The very small LO power to be expected from such devices when optimally matched (as low as 100 nW) has been verified. We have also demonstrated conversion gain of an HEB mixer device at 1.56 THz, for a 600 kHz IF frequency, and measured a DSB receiver noise temperature of 1000K at 620 Ghz.

VI. ACKNOWLEDGMENTS

This work was supported by the Russian Program on Condensed Matter (Superconductivity Division) under Grant No.93169, as well as grants from the National Science Foundation (ECS-96128), The National Research Council, and NASA (NRA 93-OSSA-06). Millimetrics, Inc. provided access to their IR mask-aligner. We gratefully acknowledge their assistance with this crucial step in our fabrication process.

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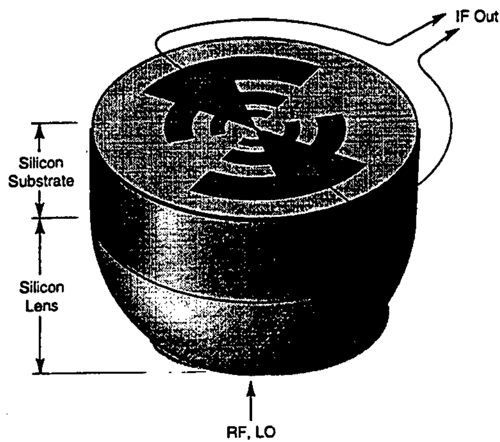

Figure 1: Log-Periodic antenna fabricated on an extended hemispherical silicon lens.

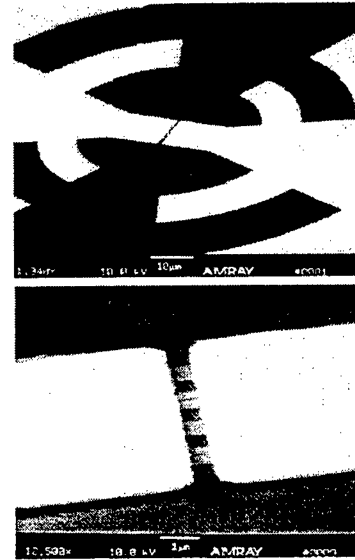

Figure 2: SEM photographs of the NbN device.

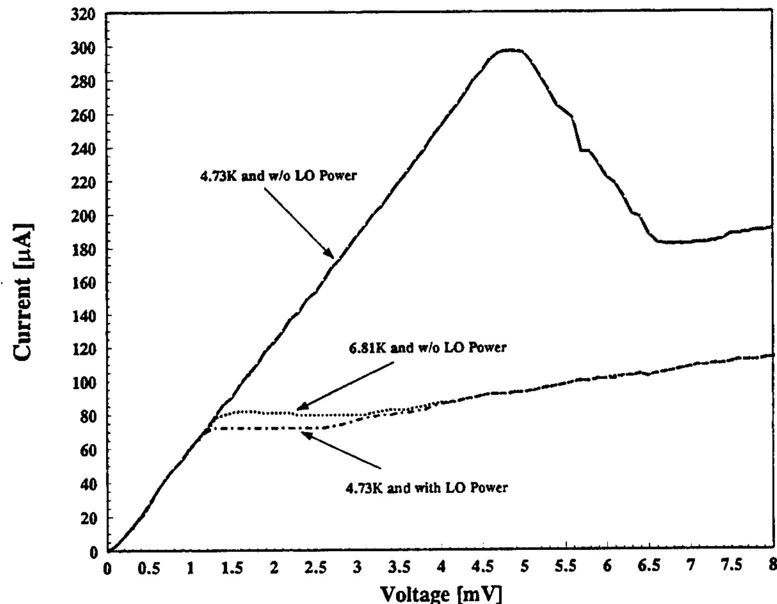

Figure 3: I-V Characteristics of a quasi-optically coupled NbN device.

Solid State Spin-Flip Terahertz Maser

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Radiation sources based on stimulated emission, lasers and masers have revolutionized many technologies. Their spectral range extends from far infrared nearly to the soft X-ray region. At the same time, development of micro-electronics has pushed the frontier of the electronic devices beyond 100GHz range. Conspicuously, the wide frequency gap between electronics and optics, specifically in $100GHz$ - $10THz$ range, remains largely uncovered by the coherent sources of radiation. Recent development of Quantum-Cascade Laser [1] based to the intersubband transitions in two-dimensional semiconductor structures is a promising step, but so far, it had not been operated at wavelengths longer than $10\mu m$.

It is highly desirable to develop an injection-pumped source of coherent THz radiation, where the radiation would originate from the transitions between the states of mobile current carriers. But this task is impeded by two obstacles -

- the mobile carriers are easily scattered in the momentum space resulting in a broadened gain curve and low gain, and
- the presence of mobile carriers leads inevitably to the free-carrier absorption making the lasing threshold unsustainably high.

Recent developments of the layered two-dimensional structures, however, had created an opportunity to circumvent the aforementioned obstacles First of all, in two-dimensional structures the continuous spectrum free-carrier absorption exists only for the electro-magnetic waves polarized in the plane of growth or TE. Absorption of the TM polarized radiation is quantized and thus if the frequency of the radiation is far from the intersubband resonances, the absorption is very low. Second, scattering of the mobile carriers occurs in the momentum space, and it does not influence the spin co-ordinate directly. The spin-spin relaxation time in the paramagnetic resonance T_2 is orders of magnitude longer than the momentum relaxation time τ [2]. Furthermore, the recent development of digital magnetic semiconductor heterostructures with very high effective values of Lande splitting factor g (order of 10^2 or more at temperatures less than 30K) [3] makes it possible to move the paramagnetic resonance frequency into the THz range at a magnetic field less than $1T$, achievable using compact magnetic sources. Finally, recent experiments on spin-tunneling

[4], and spin-transistors [5] have open a possibility of selective injection of carriers with one spin into the semiconductor [6] - thus creating the population inversion. In this paper we propose a new type of the solid-state radiation source - Spin-Tunneling-Pumped-Maser and evaluate the gain, threshold, and output power for this device.

The proposed structure is shown in Fig.1 and consists of the multiple alternating layers of undoped wide-bandgap semiconductor -barriers (B) and lightly-n-doped or intrinsic semiconductor S with large effective g-factor. This multilayered structure is placed between two thick layers of oppositely-magnetized ferromagnetic layers - emitter (E) and collector (C), made from high-coercivity material. There are also small barriers separating the ferromagnetic electrodes from the active semiconductor layer. The thickness of the semiconductor layers, t must be small enough to prevent free-carrier absorption of the TM waves - less than 30$\AA$ according to our estimate. The ferromagnetic layers provide injection of the spin-polarized carriers and they also serve as the metallic single mode waveguide walls. Thus the width of the semiconductor layer W_s shall be equal to $W_s = \lambda/2n_\lambda$, where n_λ is index of refraction at THz wavelength λ.

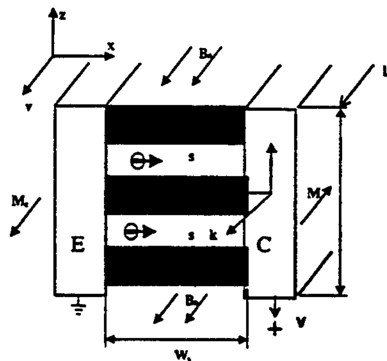

Figure 1: Cross sectional view of the proposed THz Maser.

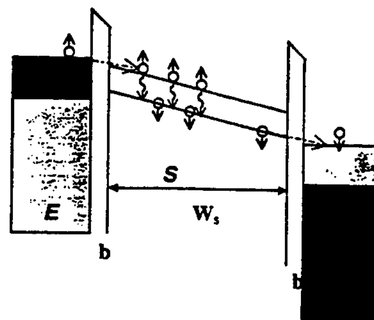

Figure 2: Conduction-Band Diagram of the Proposed Maser.

The conduction band diagram is shown in Fig.2. A lateral DC magnetic field $\mathbf{B_0}$ is applied along y axis, causing a Zeeman splitting

$$\hbar\omega = |g_y|\frac{e\hbar}{2m}B_0 = hc/\lambda \tag{1}$$

in the conduction band, where g_y is an effective Lande factor in the plane of quantum wells. Thus the spins aligned along the negative direction of y, or $s_y = -1/2$ have a lower energy If the ferromagnetic layer E has been magnetized in the negative direction y, then, assuming a simplified Stoner [5] model, the conduction subband with the $s_y = -1/2$ is fully occupied and lies below the Fermi level, while the $s_y = 1/2$ subband is only partially occupied and thus can be injected into the semiconductor, thus contributing to conductivity. The ferromagnetic material in the collector, on the other hand, is magnetized in the opposite direction and thus can only accept electrons with $s_y = -1/2$. Then, according to [5] the tunneling current on both interfaces is spin-polarized, characterized by the polarization efficiency $\eta = (J_+ - J_-)/(J_+ + J_-)$, which has been measured to be of the order of 50%. Since more electrons with $s_y = +1/2$ are injected by the emitter and more electrons with $s_y = -1/2$ are collected by the collector, there is a possibility of maintaining a steady-state population inversion in the active region. We performed theoretical analysis of the proposed device using all th experimentally-verified material parameters and obtain the following results:

- The condition for the existence of gain in the in the half-wavelength layer W_s is

$$v_n g_y \tau_s \ln(1+\eta) B_0 \frac{\pi}{n_\lambda}\frac{2mc}{e} \approx 0.1T \cdot cm, \tag{2}$$

  where v_n is drift velocity of electrons, and τ_s is spin-lattice relaxation time, and $n_\lambda \sim 3$. If the applied DC magnetic field $B_0 = 1T$, spin-polarization efficiency $\eta = 0.5$, and saturation velocity is $v_n = 10^6 cm/s$, this requirement can be satisfied if $g_y \sim 400$ and $\tau_s \sim 10^{-9}s$. With the above parameters, the wavelength is estimated to be $\lambda \approx 50\mu m$, and the active region width is $W_s \approx 8\mu m$.

- maser gain for the TM- polarized microwave is

$$G = \frac{J}{eW_s}\left[\eta - \ln(1+\eta)\right]\tau_s \frac{(g_x)^2}{16}\frac{\hbar\omega}{mc^2}\frac{e^2}{m}\eta_0 n_\lambda T_2 \tag{3}$$

  where $\eta_0 = 377\Omega$, and T_2 is a spin-spin relaxation time which in high quality semiconductor materials is of the order of $10^{-11}s$ Thus for $J = 10kA/cm^2$ and $g_x \approx 400$ one can expect gain of the order of $1cm^{-1}$ for the $50\mu m$ range, assuming that all radiation is confined inside the active layers. So, for practical purposes one shall multiply the gain by the "filling factor" of the order of $F \sim 2n_\lambda Nt/\lambda$ where N is a total number

of active layers. Assuming that whole epitaxial structure is about $5\mu m$, and active layers are twice as thin as barriers, we obtain $F \sim 0.2$, and the gain of the order of $0.2cm^{-1}$

- Threshold current
$$I_{th} = \frac{e}{\tau_s}\frac{(2\alpha L + T)}{\eta - \ln(1+\eta)}\frac{\lambda^2}{8n^2\sigma_M}, \tag{4}$$
where T is transmission of the output mirror For the $5mm$ long cavity and a 10% transmission mirror we obtain $I_{th} = 1A$.

- Output power
$$W_{out} = \frac{(I - I_{th})}{e}\hbar\omega\frac{T}{T + 2\alpha L}(\eta - \ln(1+\eta)) \tag{5}$$
For a 4A input current, output power is about 1mW. It is difficult to estimate the potential efficiency of the proposed device at the present since one does not really know the voltage drop on the contacts and in the semiconductor, but assuming it to be on the order of 1V, the slope efficiency is about 0.02%

The main challenge lies of course in finding materials combining a high effective g and long spin-spin and spin-lattice relaxation times at elevated temperatures, since so-far all the enhancements of g had been observed only at temperatures lower than 30K. Hopefully, new "digital magnetic superlattices" offer a plausible solution to these problems. It is important to note that the gain is directly proportional to both τ_s and T_2, and square of g. Therefore, small improvements in each of these factors can result in orders of magnitude increase in gain.

In conclusion, we proposed a novel injection-pumped source for the coherent THz radiation based on the effect of spin-polarized injection and showed how the problem of the free-carrier absorption can be alleviated. We evaluated conditions for population inversion, the gain, and the output power of the prospective device, showing that with the advances in growth of two-dimensional diluted magnetic materials such device may be feasible.

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Direct Measurements of Electron Energy Relaxation Times at an AlGaAs/GaAs Heterointerface in the Optical Phonon Scattering Range

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I. Introduction

Low-temperature energy relaxation processes for two-dimensional electron gas media in AlGaAs/GaAs heterostructures have long been the object of active research [1]. Still, substantial discrepancies persist between the existing theory and the experimental data on inelastic relaxation [1,2]. A discrepancy, rapidly growing with increasing electron temperature T_e (beginning from T_e~10 K), is observed in the dependence of the energy loss rate (ELR), Q_e, on electron temperature, under strong heating conditions ($[T_e-T]/T \gg 1$) [2].

Experiments conducted at somewhat higher temperatures in GaAs/AlGaAs quantum wells with various electron concentrations, show that at higher sheet concentrations of electrons ($n_s \approx 10^{11}$-10^{12} cm^{-2}), the characteristic time τ_{LO}, which describes the energy loss rate, exceeds the time for spontaneous optical phonon emission (~ 0.1 ps) predicted by theory [1], by more than an order of magnitude. This effect is well explained by the hot phonon model [1].

Accurate energy loss data are missing in the temperature range from about 20K to about 40 K. For this reason, and because of the discrepancy between theory and experiments in the temperature region around 10 K discussed above, the *direct determination* of the inelastic scattering time in low-dimensional structures in the entire temperature range from 4.2 K to 50 K is of interest. Such experiments are also necessary for different applications.

II. Experimental Setup and Device Configuration

In order to determine the energy relaxation times in heterostructures of AlGaAs/GaAs at lower temperatures, we used the technique of millimeter wave spectroscopy with high temporal resolution [3]. The most important advantages of this technique are the quasi-equilibrium conditions under which the measurements are performed, and the lack of other perturbing factors (such as magnetic fields, high energy excitations etc.).

We employed radiation from two 2-mm range backward wave oscillators (with generation frequencies of about 140 GHz), separated in frequency by a value Δf, to investigate the dependence upon Δf of the heterodyne signal produced by the two oscillators, as a dc current was passed through the sample. Our measurements of τ_e were performed under quasi-equilibrium conditions, i.e. at such low fields that the carrier heating is negligible. The absorption of electromagnetic power by the free carriers leads to heating of the electron gas. The sample responded to the increased electron temperature T_e by changing its resistance. We measured the voltage response ΔU at a frequency Δf due to this change in resistance. The measured millimeter wave response time, derived from the frequency domain data, was taken to be equal to the energy relaxation time of the free carriers in the absence of the bolometric effect, using the following expression:

$$\Delta U(\Delta f) = \frac{\Delta U_{\Delta f=0}}{\sqrt{1+\left(2\pi\Delta f\tau_e\right)^2}} \tag{1}$$

The sensitivity of our equipment allows us to make use of a minimum dc power level of P_{dc}~$5*10^{-17}$ W/el, which translates to an increase in T_e of less than 0.1 K at 4.2 K. The millimeter-wave absorbed power level was estimated to be $P_{ac}<10^{-17}$ W/el. The relaxation time decreases with increasing temperature. For this reason, the maximum temperature at which measurements can still be performed with satisfactory accuracy is limited mainly by the maximum achievable frequency, Δf_{max}. In our case, Δf_{max}=1500 MHz, which corresponds to a value for τ_e~100 ps, determined with an error not exceeding 20%. The maximum temperature we could reach was then 50 K.

In the case of strong dc heating, the voltage response ΔU was related to the electron temperature T_e known from dc power losses in the 2DEG-channel. The electron temperature T_e was determined from the Shubnikov-de Haas oscillation amplitude damping technique up to T_e=12 K, but at higher temperatures it was obtained by comparing the measured Q_e values with well-known reference data for $Q_e(T_e)$ valid for concentrations close to ours [4]. It is important that at temperatures up to 12 K our data is in very good agreement with that of [4] and other references.

The experimental structures were manufactured by molecular beam epitaxy and had a carrier mobility of $7.5*10^5$ cm^2 /V*s and a carrier sheet concentration $n_S=4.2*10^{11}$ cm^2 at T = 4.2 K. The mesa structures, with an area of 400*100 μm^2, had AuGeNi ohmic contacts.

III. Results and Discussion

The experimentally obtained dependence $\tau_e(T)$ is shown in Fig.1. The whole temperature range can be divided into three regions: 1) a region with a slow decrease of τ_e with increasing temperature (4.2 K<T<15 K); 2) a region in which τ_e=const (16 K<T<21 K); 3) a region with a fast decrease of the energy relaxation time, starting at T~25 K. Fig. 1 also contains the data on $\tau_e(T_e)$ for the case of strong heating by a DC electric field (in which case the temperature scale corresponds to T_e). At $T(T_e)$ < 15 K the values of τ_e under quasi-equilibrium conditions are close to those observed under strong heating. The same is observed in the high temperature region. A small difference between the $\tau_e(T)$ and $\tau_e(T_e)$ values in the intermediate temperature region may be accounted for by the insufficient accuracy of the technique we used to determine the T_e value under strong heating conditions. Thus, the results obtained show that τ_e is a function of the electron temperature only.

In the low-temperature range, 4.2-15 K, acoustic phonon scattering processes which are due to the piezoacoustic potential (PA), and to the deformation potential (DA), coexist [2]. In this region, the decrease of τ_e gradually slows down as the temperature grows, with the lessening of the PA process contribution. The value of the constant relaxation time, τ_{DA}=0.61 ns, in this region is lower than that obtained in [4] (~0.9 ns) but very close to τ_e=0.5 ns, found from the first direct measurements [5]. According to [4], the constant relaxation time observed in the range 16 K<T<21 K corresponds to a predominance of DA processes (energy losses of the form Q_e~$(T_e^{\gamma}-T^{\gamma})$ where γ=2). A transition to linear dependence Q_e~
(T_e-T, predicted by theory [2], and which should entail a linear *increase* of τ_e with temperature, agrees neither with our results, nor with the commonly known experimental data on $Q_e(T_e)$. We have thus obtained further evidence for this discrepancy between theory and measurements. Ridley [1] discusses other processes which may explain the discrepancy, but we are not aware of any work in which these possibilities have been explored in detail.

Finally, we attribute the rapid decrease of the relaxation time at T>25 K to the influence of optical phonons. Assuming that the contribution of the acoustic deformational scattering is constant up to 50 K, we single out the temperature-dependent contribution of τ_{eO}: $\tau_{eO}^{-1} = \tau_{e}^{-1} - \tau_{DA}^{-1}$. If τ_{eO} is determined by the scattering due to optical phonons, then its temperature dependence must be described by the following expression:

$$\tau_{eO} = \frac{\pi^2 k_B T \tau_{LO}}{3\varepsilon_F}\left(\frac{k_B T}{\hbar\omega_{LO}}\right)^2 \exp\left(\frac{\hbar\omega_{LO}}{k_B T}\right), \qquad (2)$$

where k_B is the Boltzmann constant, and ε_F is the Fermi energy. This equation follows from the expressions [1]:

$$\tau_e = \frac{d\varepsilon}{dP}, P = \frac{\hbar\omega_{LO}}{\tau_{LO}}[\exp(-\frac{\hbar\omega_{LO}}{k_B T_e}) - \exp(-\frac{\hbar\omega_{LO}}{k_B T})], \qquad (3)$$

Further, we have made use of [4]:

$$dQ_e(T_e) = \frac{d\varepsilon}{\tau_e(T_e)}, d\varepsilon = \frac{\pi^2 k_B^2 T_e dT_e}{3\varepsilon_F}; \qquad (4)$$

The data we obtained do indeed agree well with expression (2) for the commonly accepted value $\hbar\omega_{LO}$=36.5 meV (see inset in Fig.1). Hence τ_{eO} can be identified with the contribution of the optical phonons. The characteristic lifetime τ_{LO} of the optical phonons obtained from the values of τ_{eO} is approximately equal to 4.5 ps. This is 30 times as great as the time for spontaneous emission of optical phonons [1]. We obtained this result both for quasi-equilibrium conditions and for strong heating. This fact demonstrates that in the case of interaction with the optical phonons, too, τ_{LO} is determined by the electron temperature T_e only, and that the decreased probability of electron-phonon interaction is connected with the re-absorption of the optical phonons. Their population appears to be the same under equilibrium and non-equilibrium conditions.

Using the measured values of τ_e, one can calculate the dependence of the energy loss rate on the electron temperature,by using (4). The dependence obtained by numerical integration of our data for τ_e (T) shows good agreement with the experimental data taken from [4] and other measurements for samples with concentrations not very different from that of our samples.

IV. Conclusion

The technique we used to directly determine τ_e in two-dimensional electron gas in heterostructures of GaAs/AlGaAs permitted us to observe the transition from the region in which the PA- and DA- processes coexist, to the region in which DA scattering predominates, and with a further increase of temperature, also the transition from acoustic phonon scattering to scattering due to optical phonons. The value of the effective lifetime of the optical phonons τ_{LO}=4.5 ps (at $n_S \sim 4*10^{11}$ cm^{-2}) was obtained. It was shown that in the whole temperature range (4.2-50 K) the relaxation time is determined by the electron temperature.

V. Acknowledgements

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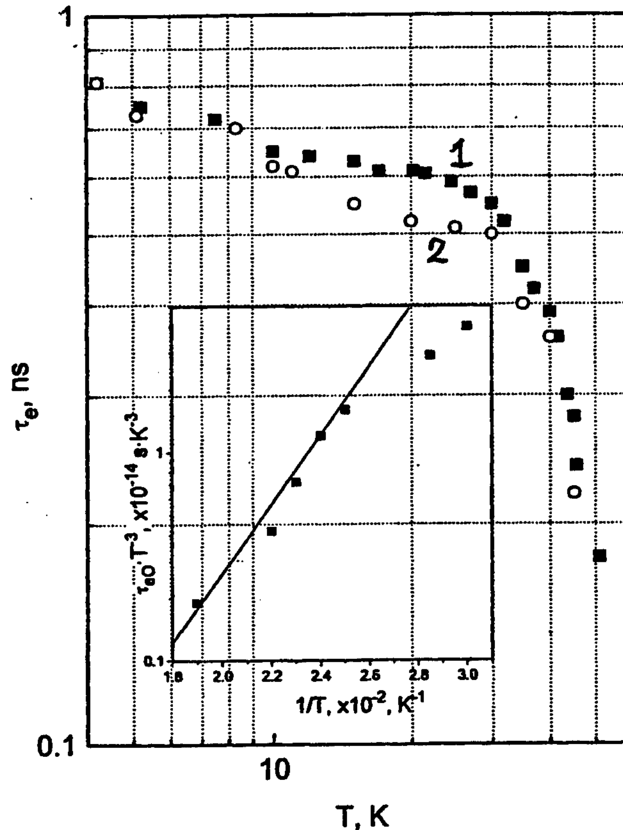

Fig.1. Temperature dependence of the energy relaxation time $\tau_e(T)$ (1 - quasi-equilibrium data; 2- under strong dc heating conditions). The inset shows the dependence of $\tau_{eO}T^{-3}$ upon T^{-1} (the straight line corresponds to $h\omega_{LO}$=36.5 meV).

The Effect of Hydrogen on the Schottky Barrier Height and Electrial Properties of $TiSi_2$/Si(100) by Furnace Annealing

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With increasing circuit speed and functional complexity of design, greater demand is placed on the performance of the interconnects. The requirement of conformity for contact and via filling has increased the usage of CVD deposited metal films for advanced ULSI multilevel interconnects.[1] Si(100)/$TiSi_2$/TiN/W is one of the most common metallization schemes used for sub 0.35μm manufacturing. However, it is observed that the resistance of boron doped p^+-Si contact increases abruptly[2] after CVD W deposition. The W film is deposited from the reduction of WF_6 by H_2/SiH_4 and atomic hydrogen can be the reaction by-products. It is well known that hydrogen can passivate the activity of various shallow impurities as well as deep centers. This causes significant changes in the electrical and optical properties of semiconductor[3] materials. There are reports that suggest thermal annealing at elevated temperature (e.g. > 200 °C in inert gas ambient) can restore the electrical property of dopants.[4] Since this Si/$TiSi_2$/TiN/W metallization is essential for wafer fabrication, it is of fundamental and practical importance to understand the effect of hydrogen on the Schottky barrier height and electrical properties of the Si(100)/$TiSi_2$ interfaces.

In this experiment, samples with 154 Å thick C49 phase $TiSi_2$ formed on Si(100) surfaces with boron implant (~ 2×10^{15} cm^{-2}, 50 KeV) and forming gas annealing (12 % H_2 + 88 % N_2, eight consecutive 30 min annealing cycles at 450 °C). The Schottky barrier heights were measured using a metal-semiconductor-metal structure (MSM), which basically consists of two Schottky diodes connected back to back. The Schottky barrier height (SBH) formed at the metal-semiconductor interface was measured by internal photoemission spectroscopy at 77 K. The reverse bias I-V measurement is also performed at 77 K as shown in Fig. 2. The photoemission yield, Y, which is known to follow Fowler's law, is proportional to $(h\nu - \Phi_B)^2$, where $h\nu$ is the energy of the incident radiation and Φ_B is the barrier height measured from the metal Fermi level. [5] Fig. 1 shows the Fowler plots of photoresponse w.r.t. number of annealing cycles. It was difficult to determine the SBH of the untreated diodes and those that have been subject to up to three consecutive annealing cycles (i.e. because of large reverse leakage current). The photoresponse increased dramatically upon the fourth annealing, but began to decrease again after the fifth annealing cycle. Extrapolation from the linear portion of these two Fowler's plots gave a SBH of 0.64 eV. This suggests that the current transport mechanism changed from tunneling to thermionic

emission when the boron was deactivated. Fig. 2 shows that the reverse current dropped when the photoresponse was high. The signal to noise ratio for the photocurrent measurement also becomes poor after the fifth annealing cycle and the barrier height cannot be measured again. This can be explained by hydrogen accumulating at the $TiSi_2$ grain boundaries,[6] resulting in less excited electrons surmounting the barrier. These results suggest that hydrogen has been catalyzed by either Si or $TiSi_2$ to form atomic hydrogen which diffuses rapidly into the Si(100)/$TiSi_2$ interface through the barrier metal and passivates the boron. It is also well known that the neutralized boron can be reactivated in p^+-Si by annealing at greater that 160 °C, corresponding to a reactivation energy of 1.5 eV. Competition between deactivation and activation of the dopant could be the reason for the behavior in the I-V measurements observed after the fourth annealing cycle.

From the experimental results, it is clear that both electrical and optical properties of the diodes were significantly affected by hydrogen annealing.

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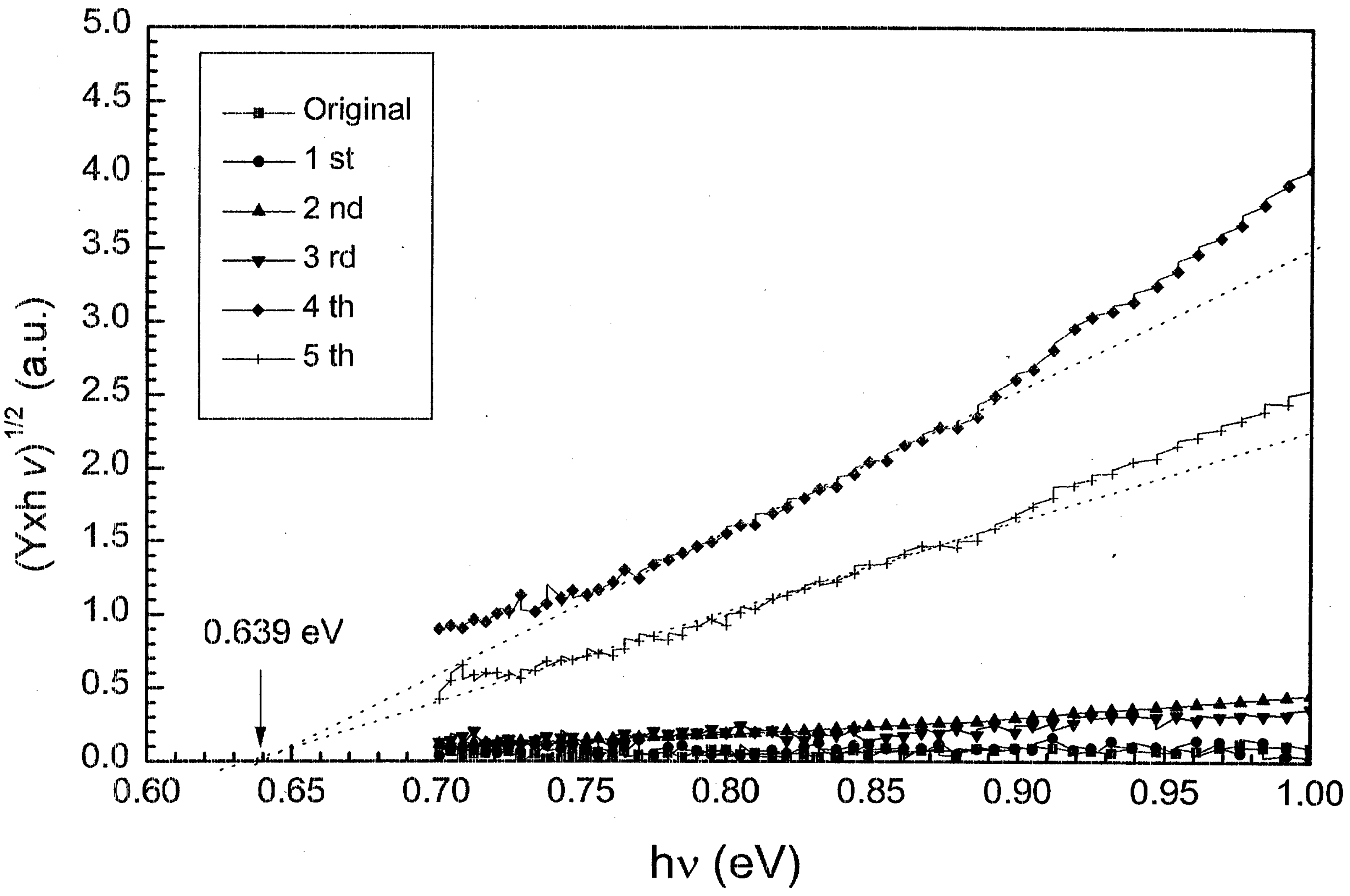
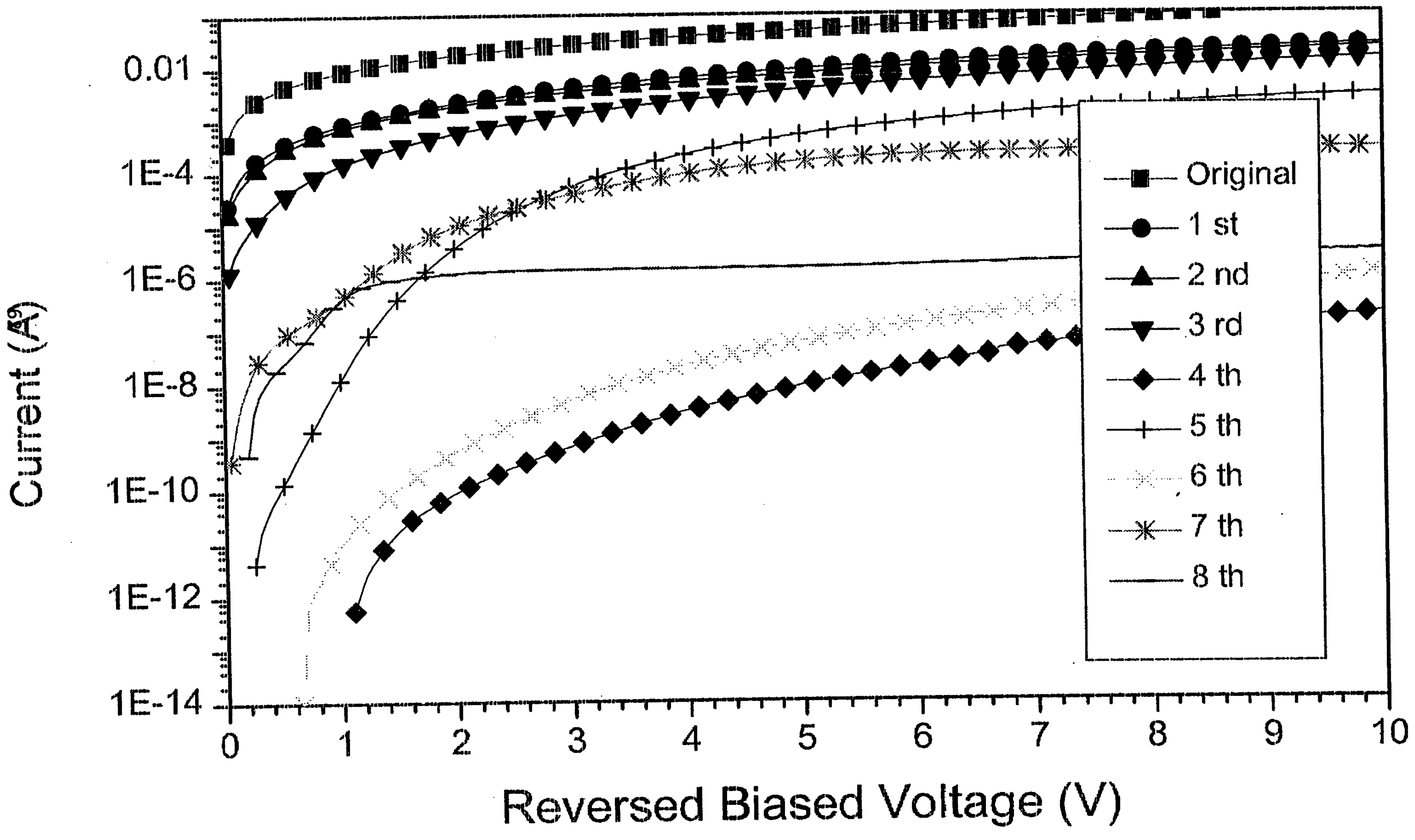


Fig. 1 Internal Photoemission Measurement
Original
1 st
2 nd
3 rd
4 th
5 th
0.639 eV
$(Y\times h\nu)^{1/2}$ (a.u.)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
0.60
0.65
0.70
0.75
0.80
0.85
0.90
0.95
1.00
$h\nu$ (eV)

Fig 2. Reverse Bias Current Measurement



A Study of Double Pseudomorphic System with Oppositely Strained Layers $Al_{0.6}In_{0.4}As/In_{0.8}Ga_{0.2}As$ on InP

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Abstract

As a new hetero-junction structure for InP PHEMT, a double pseudomorphic system with oppositely strained layers $Al_{0.6}In_{0.4}As/In_{0.8}Ga_{0.2}As$ on InP substrate has been described in this paper. Our experiment results have shown that the mobility μ_e of this system is up to 11839 $cm^2/v.s$ and the 2DEG density is $3.73\times10^{12}/cm^2$ at room temperature. The mobility of this system has been increased by 31.9%, compared with the conventional pseudomorphic system of $Al_{0.48}In_{0.52}As/In_{0.8}Ga_{0.2}As$ that was specially grown under the same condition in our experiment for comparison. It implies that the stress of the extra In composition channel layer $In_{0.8}Ga_{0.2}As$ has been compensated by that of extra Al composition barrier layer $Al_{0.6}In_{0.4}As$ to some extent, so the mobility can be improved obviously.

Introduction

In the past few years, significant efforts have been made to improve the performance of $Al_{0.48}In_{0.52}As/In_xGa_{(1-x)}As$ InP PHEMTs [1]–[5], because of its attractive intrinsic properties, such as high mobility , high peak velocity, high conduction-band discontinuity and so on. Among these efforts, the most effective approaches were to shrink gate length and to use In-rich channel heterojunction material systems. Up to now, many excellent results have been reported. For example, 50nm self aligned gate pseudomorphic $In_{0.8}Ga_{0.2}As$ channel HEMTS with f_t of 340 GHz have been reported by Loi D.Nguyen et al. A number of different systems of $Al_{0.48}In_{0.52}As/In_xGa_{(1-x)}As$ have also been proposed. In these systems, the indium composition x in the channel layers is generally more than 0.53, even x=1. In addition, Albert Chin et al. have reported the results through the use of a novel channel design utilizing oppositely strained layers with x=0.25 and 0.8[5].

In this paper, we proposed a new system with extra In composition pseudomorphic channel layer and extra Al composition pseudomorphic barrier layer, which we called "double pseudomorphic system". Our comparison experiments have shown that this structure can increase the electron mobility by 31.9% or so, compared with the conventional system, and keep high 2DEG density at the same time.

Experiment and result

Fig.1(a) shows the structure of the double pseudomorphic system for PHEMT. The heterostructures used in this study were grown by Gas Source Molecular Beam Epitaxy (GSMBE) on Fe-doped semi-insulating (100) InP substrate. Both of the channel layer $In_{0.8}Ga_{0.2}As$ and the barrier layer $Al_{0.6}In_{0.4}As$ are lattice mismatched to InP, but they are oppositely strained layers. It is the point different from the conventional system which only has a mismatched channel layer, shown in Fig.1(b).

For comparison, both kinds of heterojunction structures were grown under the same condition. In the first experiment, results are shown in the left column of table 1. The mobility of the double pseudomorphic system at room temperature μ_{e300} is up to 11839 $cm^2/v.s$,31.9% higher than that of conventional one, and the 2DEG density n_{300} is $3.73\times10^{12}/cm^2$. For conforming these results, the second experiment has been done afterward, results shown in the right column of table 1.

(a)
n+ $In_xGa_{(1-x)}As$ 100Å x=0.53
$In_xGa_{(1-x)}As$ 30Å x=0.53
strained $Al_{0.6}In_{0.4}As$ 300Å
Si-doped 5×10^{12}
$Al_{0.48}In_{0.52}As$ 60Å
strained $In_xGa_{(1-x)}As$ 60Å x=0.8
$Al_{0.48}In_{0.52}As$ 3000Å
Fe-InP Substrate

(b)
n+ $In_xGa_{(1-x)}As$ 100Å x=0.53
$In_xGa_{(1-x)}As$ 30Å x=0.53
$Al_{0.48}In_{0.52}As$ 300Å
Si-doped 5×10^{12}
$Al_{0.48}In_{0.52}As$ 60Å
strained $In_xGa_{(1-x)}As$ 60Å x=0.8
$Al_{0.48}In_{0.52}As$ 3000Å
Fe-InP Substrate

Fig 1. (a) structure of double pseudomorphic system
(b) structure of conventional pseudomorphic system

Table 1. Property comparison of double pseudomorphic system with conventional one

	First experiment		Second experiment	
system	double	conventional	double	conventional
thickness of barrier (Å)	300	300	200	200
Al composition	0.6	0.48	0.6	0.48
thickness of channel (Å)	60	60	60	60
In composition	0.8	0.8	0.8	0.8
μ_{e300} $cm^2/v.s$	11839	8973	11791	9605
μ_{e77} $cm^2/v.s$	60985	48170	58312	33372
n_{300} cm^{-2}	3.73×10^{12}	5.1×10^{12}	3.14×10^{12}	2.96×10^{12}
n_{77} cm^{-2}	3.19×10^{12}	3.72×10^{12}	2.8×10^{12}	2.55×10^{12}

From the results of the experiments, we can see:

No matter the temperature is at 300K or 77K,the mobility of double pseudomorphic system is always higher than that of conventional one.

In both experiments, the mobility and the 2DEG density of the double pseudomorphic system vary only a little, much less than those of conventional system. The percentages of the mobility and 2DEG density deviation in those two experiments are shown in table 2.

Table 2. The percentage of mobility and 2DEG density deviation of two experiments

system	double	conventional
$\Delta \mu_{e300}/\mu_{e300}$	0.4%	7.0%
$\Delta \mu_{e77}/\mu_{e77}$	4.4%	31%
$\Delta n_{300}/n_{300}$	16%	42%
$\Delta n_{77}/n_{77}$	12%	31%

Table2 shows that the double pseudomorphic system has a better repeatability than conventional one.

Discussion

<1>Why does the double pseudomorphic system have higher mobility and much better repeatability than conventional one? Our explanation is as follows:

$In_{0.8}Ga_{0.2}As$ channel layer can be regarded as the composition of 0.4255× $In_{0.53}Ga_{0.47}As$, which is lattice-matched with InP, and 0.5745×InAs; and $Al_{0.6}In_{0.4}As$ barrier layer can be regarded as the composition of 0.769× $Al_{0.48}In_{0.52}As$, which is lattice-matched with InP, and 0.231×AlAs. As is known, the lattice parameter of InAs is 6.0583Å, which is more than that of InP, 5.8687Å. The lattice parameter of AlAs is 5.66Å, which is less than that of InP. InAs and AlAs are lattice mismatched with InP, but they cause opposite stresses to InP. The oppositely strained channel and barrier layers mentioned above can compensate the stresses each other to some extent. Therefore, the mobility and the repeatability can be improved.

<2>The double pseudomorphic system has two advantages: One is that the stress can be reduced by the adjacent oppositely strained layers, resulting in the improvement of mobility, 2DEG density and repeatability. The other is that Al-rich barrier layer can reduce the reverse leakage current of the Shottky diode of PHEMT's gate, because of its wider bandgap.

<3>With the concept of the stress compensation utilizing oppositely strained channel and barrier, it is possible to improve the properties of AlGaAs/InGaAs heterojunction material on GaAs as well.

Summary

We proposed a double pseudomorphic system with oppositely strained layers

$Al_{0.6}In_{0.4}As/In_{0.8}Ga_{0.2}As$ on InP for PHEMT. Our comparison experiment results have shown that this new structure has higher mobility with high 2DEG density and better repeatability, compared with conventional one. This is because the stress of the double pseudomorphic system has been reduced by the compensation of two oppositely strained layers. Optimizing the In and Al compositions and the channel and barrier thickness, it is still possible to get further improvement for the heterojunction materials. With the concept, it is possible to improve properties of other heterojunction materials, such as AlGaAs/InGaAs on GaAs.

Acknowledgment

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Measurement-Based Interconnect Capacitance Characterization for Circuit Simulations

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ABSTRACT

A characterization methodology to model interconnect capacitance for accurate circuit simulation is presented. The method utilizes a simple measurement scheme to measure inter-layer capacitances. The measured data is then used to tune a layout tool for accurate interconnect parasitic extraction. Results show good fit between simulated and measured ring oscillator speeds for a production 0.5μm, 3-level metal process.

I. INTRODUCTION

The impact of interconnect on circuit performance is continuously increasing. Accurate and efficient characterization of on-chip interconnections is required to give circuit designers an honest assessment of speed and noise issues.

Past characterization methods have relied on interconnect simulations [1, 2]. This work explicitly demonstrates a measurement-based method to characterize interconnect capacitance for circuit simulation. The advantage of this technique is two-fold: one, it provides a direct means of measuring interconnect capacitances, and two, it assesses the actual extent of interconnect capacitances variations without relying on ad hoc methods.

The organization of this paper is as follows. First, the test structure and measurement methodology is briefly reviewed. Second, we will describe a method for calibrating a layout tool's parasitic extractor for accurate interconnect capacitance extraction. Lastly, results are given to demonstrate the accuracy of the method.

II. MEASUREMENT METHODOLOGY

Measurement of inter-layer interconnect capacitances were made using a technique called *Charge-Based Capacitance Measurement (CBCM)* [3].

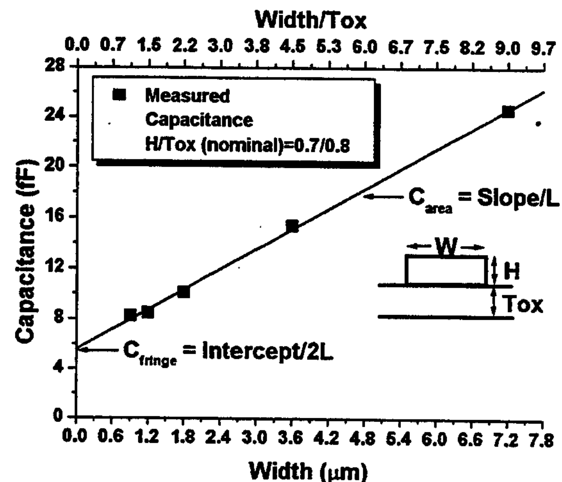

Figure 1. Measured interconnect capacitance data collected from CBCM test structures to characterize M2 to M1 inter-layer capacitance.

This methodology allows capacitances as small as ~10aF to be measured. Consequently, the area allotted for each test structure can be very small thus allowing many different structures to be included for characterization. The measurement technique is also efficient: only a DC ammeter is needed.

Figure 1 shows data collected from 5 CBCM test structures from one die location for a 0.5μm, 3-level metal technology. M2 to M1 inter-layer capacitance parameters, C_{area} and C_{fringe}, can be directly calculated. This process was repeated for a total of 25 dies and for all inter-layer capacitance combinations. The results are summarized in Tables 1 and 2.

The magnitude of this measured interconnect capacitance variation is substantial compared to device saturation current (Idsat) variation (Figure 2) for the same technology. These capacitance fluctuations are not currently taken into account in modern

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mean (sigma)	Poly	M1	M2	M3
Sub	91.7 (1.99)	32.8 (0.71)	16.5 (0.37)	10.3 (0.18)
Poly		63.3 (1.20)	22.2 (0.69)	11.7 (0.32)
M1			53.0 (3.66)	16.9 (0.49)
M2				45.1 (1.74)

Table 1. Means and sigmas for all combinations of measured area capacitances. Column labels denote identity of top layer. Row labels denote bottom layer. All units are in aF/μm^2.

mean (sigma)	Poly	M1	M2	M3
Sub	45.5 (4.02)	46.9 (1.15)	35.8 (2.31)	25.6 (1.73)
Poly		57.2 (1.53)	38.3 (1.45)	27.3 (1.10)
M1			56.4 (2.41)	30.9 (1.33)
M2				40.3 (6.43)

Table 2. Similar data as in Table 1 for measured fringe capacitances. All units are in aF/μm.

circuit simulators.

III. Calibrating the Layout Tool

The simplicity and accuracy of CBCM allows it to be used for interconnect capacitance characterization in much the same manner as current device test structures are used for device (i.e. SPICE) characterization. Just as device parameters are carefully extracted for SPICE simulators, so too must interconnect parameters be carefully calibrated for layout tools, which ultimately use such information for accurate interconnect parasitic extractions for circuit simulations.

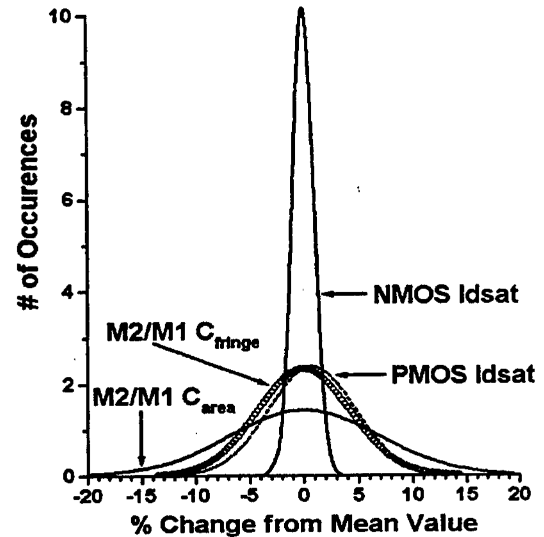

Figure 2. Magnitude of M2 to M1 inter-layer capacitances variation is comparable to device Idsat variations.

This calibration is a necessary step to ensure that measured results are properly used by layout tools for performing parasitic extraction. The extraction algorithms usually provide approximations to more complicated effects.

An example is shown in Figure 3. Most layout parasitic extractors tend to treat the capacitance of three closely-spaced metal lines as three times the capacitance of an isolated line. Unfortunately, this is not the case. Nearby metal lines tend to shield each other's electric field lines from the metal surface to the ground plane. The overall capacitance is therefore reduced from the previous approximation. This reduction is a strong function of spacing between nearby lines as Figure 4 shows. The weak dependence on ILD thickness is also shown. Errors as large as 35% can result if such calibration is not performed.

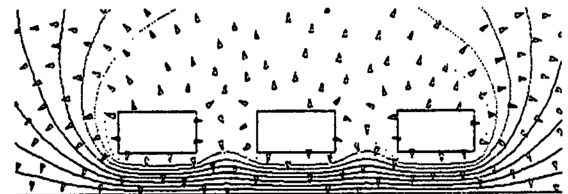

Figure 3. Nearby metal lines tend to shield the electric fields lines (denoted by arrows) from terminating on the ground plane. The overall effect is reduced capacitance.

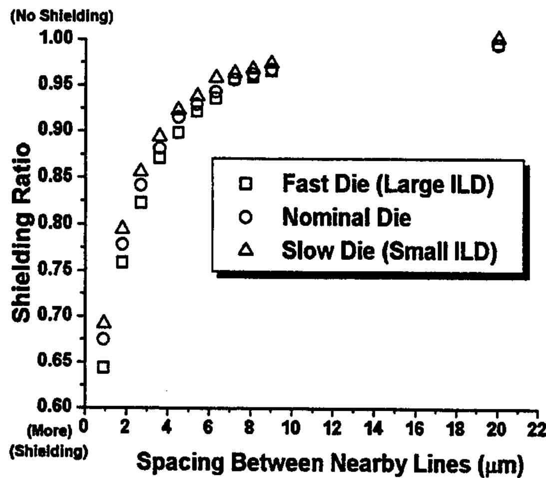

Figure 4. Dependence of shielding ratio for the 3 closely spaced lines of Figure 3. Shielding ratio is defined as the ratio of actual capacitance over 3 times the capacitance of one isolated line. All data points are from 3-D EM field simulations.

For the layout tool to reflect this shielding effect, a corrective factor will be needed to scale down its fringing capacitance value. Only the fringing component needs to be corrected due to the fact that field lines from the area component are not shielded by the presence of nearby lines (Figure 3).

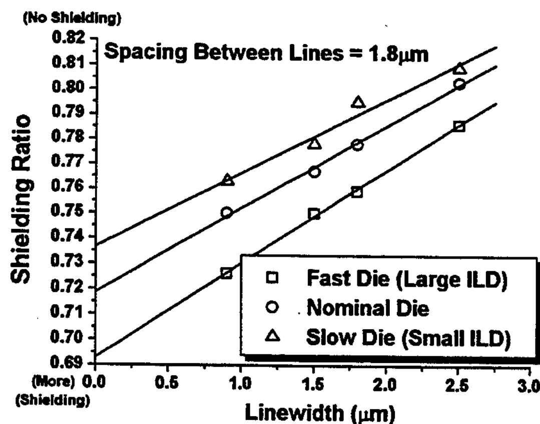

Figure 5. The intercept determines the corrective factor for the fringing component of inter-layer capacitance.

To determine this corrective factor, a 3-D EM field simulator, RAPHAEL[4], was used to simulate the shielding ratio as a function of linewidths. The 3 line system of Figure 3 is simulated and the results are shown in Figure 5. Since the shielding ratio only corrects for fringing capacitances, only the Y-axis intercept values should be used. These values correspond to theoretical zero area capacitances while fringing capacitances are still retained.

The corrective factors thus obtained from Figure 5 show that dies with a large ILD (inter-level dielectric) thickness display a smaller shield ratio (i.e. more shielding) than dies with small ILDs. A larger ILD thickness means that the field lines, on the average, have a longer distance to travel from the metal surface to the bottom ground plane. They are therefore more likely to be intercepted by other field lines, and shielded from the ground plane. This means that ILD process variations can cause a substantial change in interconnect capacitance behavior and should be modeled for improved simulation accuracy.

IV. RESULTS

The entire measurement and calibration schemes were used to characterize Interconnect Dominated Ring OScillator (IDROS) circuits for a 0.5μm, 3-level metal technology.

CBCM test structures were designed to measure inter-layer M2 to M1 capacitances for a "fast", "slow", and nominal die. C_{area} and C_{fringe} components were then determined. These designations were made from IDROS speed measurements. Each stage was loaded with a M2 to M1 "snake" pattern as shown in Figure 6. This pattern includes many parallel lines close to one another and provides a unique opportunity to showcase the need to calibrate the layout tool with a corrective fringe component factor.

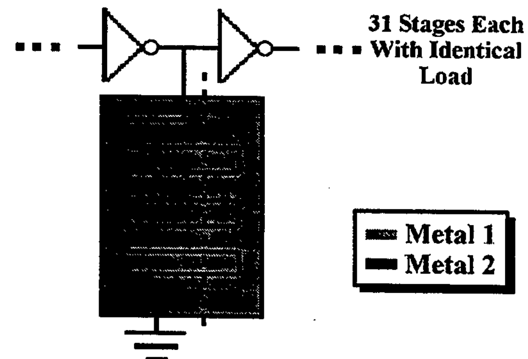

Figure 6. This specific pattern allows many parallel M2 lines to be close to one another (along dashed line). Line width is 1.8μm with 1.8μm spacing between lines.

The final results are summarized in Table 3 and show the improved fit using a fringing capacitance corrective factor. The underestimation of IDROS speed for slow and nominal dies (~ 6%) with this

methodology is most likely due to measurement error and intra-die variation in ILD thickness. Specifically, variation in I-V parameters only account for 32% of the measured range of ring oscillator speeds. The rest is due to interconnect capacitance variations.

	Measured	No Calibration	Calibration
Fast	61.3	51.5	61.4
Nominal	57	46	53.2
Slow	53.5	43.1	50.1

Table 3. Speeds of IDROS circuits in MHz for three dies. The calibration improves fit by up to 18% in some cases.

V. CONCLUSIONS

A methodology to characterize interconnect capacitance for accurate circuit simulation is presented. Measured results show that interconnect capacitance variations are comparable to device Idsat variations. Specially designed interconnect test structures are measured and the data is used to calibrate parasitic extractors within layout tools. This calibration scheme is shown to yield good results in fitting a interconnect dominated ring oscillators for a production 0.5μm, 3-level metal process.

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ANALYSIS OF REFRACTIVE INDEX AND ABSORPTION COEFFICIENT OF SILICON MEMBRANES

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INTRODUCTION

Ultrathin single crystal silicon membranes respond to the needs of the rapidly developing micromachining industry, the research needs within the traditional microelectronics industry and photonic, X-ray, and optics applications. These applications require dimensional stability in flatness and surface planarity. Material preparation is based on growing of Czochralski single crystal silicon with the range of dopants which covers the normal spectrum of Boron, Phosphorus, Arsenic and Antimony, as well as undoped silicon. Ultrathin silicon membranes are made to thicknesses as low as 2-4 microns. They are double side polished, and are extremely flexible due to the dominance of the elastic nature of single crystal silicon. The thickness tolerance range for all membranes, up to 20 microns, remains at +/- 1 micron. Ultrathin and Ultramachining silicon wafers are well suited for microcircuit devices, however, their functional uses extend far beyond this limited field as being a substrate and include mechanical and chemical sensors, silicon on insulator (SOI) devices (ultra- Machining wafers are available with or without SiO_2), infrared and interference filters, visible light detectors and micromachined detector arrays, controlled breakdown voltage diodes and voltage multipliers, where precise thickness control of the silicon is critical to the voltage requirements of the device, X-ray reflectors and focusing mirrors. Additional benefits are derived from having both sides polished, therefore circuits can be patterned on both side of a wafer. Thicknesses of 20-22 microns are arrived at by a chemical/ mechanical polishing process, while thicknesses below this level are polished by chemical methods. Chemical polishing procedures achieve double side polished thinnesses in the 2-4 μ range. Wafers have small damage due to the slow removal rate of Si (about 50 μ per hour). To address concerns related to micro-roughness, an additional production step often follows standard polishing. This "hase-free" step produces the surface smoothness of membranes in the 3-7 angstrom range. Typically wafers have 8-20 A of micro-roughness.

For many applications, the superior precision in controlling wafer planarity, surface texture, thickness uniformity is sufficient and enough. However, in other microelectronic and photonic applications there are new requirements outside of the more traditional silicon fields. The knowledge of absorption coefficient and refractive index spectra are extremely important for all optoelectronic devices. Optical properties of ultrathin silicon membranes have to be studied to provide necessary information.

There were a number of recent reports on the absorption coefficient of silicon [1, 2]. However, excellent wafer planarity and thickness uniformity make it difficult to use conventional transmission measurements for optical characterization of thin Si wafers because of interference effects. Reflection from the back surface induce significant errors in refractive index and absorption coefficient values obtained by using conventional technique, even in the range of relatively small optical transmission, where interference is not visible. In this paper we present results of optical characterization of ultrathin silicon wafers by utilizing both conventional transmission and reflection measurements technique at small values of transmittance, and recently developed optical interference spectroscopy characterization technique [3, 4]. This new technique is based on a self-consistent data-analysis algorithm for simultaneously measured optical transmission and specular reflection, using exact interference equations. Precise spectra of absorption coefficient and refractive index spectra of N- and P- type samples doped with different concentrations of Phosphorus and Boron have been measured in a wide energy range including the subgap range. We compare results in the visible and near infrared regions from two techniques and have determined the range of transmission where conventional technique is applicable. By using interference spectroscopy, we have also received absorption in the Urbax region and absorption related to impurities and intrinsic defects. The analysis of the data indicate that chemical polishing possibly effects subgap absorption.

EXPERIMENTAL TECHNIQUE.

In this study, we used conventional transmission and reflection measurements technique at small values of transmittance, and interference spectroscopy technique which was recently demonstrated in application to the hydrogenated amorphous and poly- silicon thin films [4]. The absolute transmission T and reflection R measurements were performed with Cary 5E Spectrophotometer using a two-beam scheme with specular reflection attachments which ensure a near normal (~8 °) angle of incidence on the sample.

Table 1 gives the parameters of the samples used in this study. All samples had orientation <100>+-0.5°, and were double side polished.

Table 1. Parameters for measured samples.

Notation	Dopant	Resistivity, Ω-cm	Concentration n or p, cm^{-3}	Thickness, μm
N1	Phosph.	0.1-0.3, n	$1.5x10^{16}$ - $7x10^{16}$	9.8
N2	Phosph.	1.5-2.5, n	$1.5x10^{15}$ - $2.5x10^{15}$	101
N3	Phosph.	10-30, n	$4.5x10^{14}$ - $1.5x10^{14}$	199
P1	Boron	<0.015, p	> $5x10^{18}$	9.0
P2	Boron	0.2-0.4, p	$6x10^{16}$ - $9x10^{16}$	24
P3	Boron	168-464, p	$2.5x10^{13}$ - $0.8x10^{13}$	14.5

Because of the high wafer thickness uniformity, typical spectra reveal very good resolved fringes in optical transmission in the range of small absorption (Figure 1). In reflection, fringes are not resolved to the same degree (Figure 2) because reflection measurements require several times larger area of a sample (70-140 mm^2 instead of < 20 mm^2 to measure T). It is obvious, that conventional transmission technique can not be applied in the spectral range where fringes become visible (for this sample at wave lengths greater than 700 nm). Instead, the interference technique has been utilized in this case. The technique has been described previously for a thin film deposited on a substrate [3]. The equations presented in [3] can be easily simplified for our case, since we measure the wafer without substrate. Although we can not use absolute values of reflection for the quantitative analyses, because fringes are not completely resolved, we can use the interference pattern in transmission and reflection for accurately determining the refractive index spectra from the relationship

$$n\,d = m\,\lambda / 4, \qquad (1)$$

where n is the refractive index at the wavelength of extrema λ, and d is the wafer thickness. In this procedure we need to know the order of the fringes m, which can be determined from the

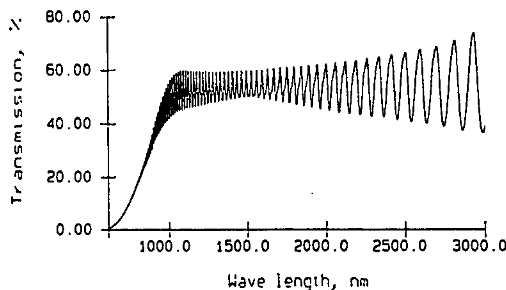

Figure 1. Optical transmission as a function of a wave length.

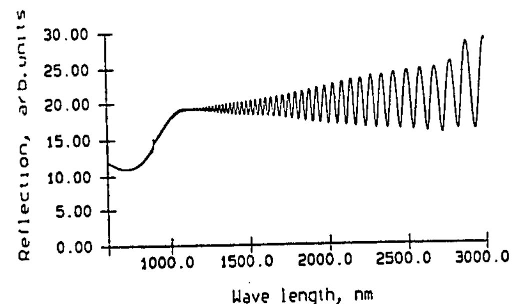

Figure 2. Specular reflection as a function of a wave length.

wavelengths of two adjacent transmission or reflection extrema in the spectral range where there is no dispersion of n. As it will be demonstrated later, this approximation can be applied between 1.5 and 2.5 μm. Independent measurements of the refractive index from the absolute value of reflection in the range of strong absorption have been used in determining thicknesses of samples, as explained below. We can also use the literature data for n (see, for example [5, 6]) in the same spectral range, where n is practically independent on doping level in non-degenerated material.

In the range of strong absorption, the fringes are not resolved and the average transmission is observed. For this range, the simple expressions usually used in conventional transmission measurements for the transmission and the reflection of an optically thick sample are

$$T= (1-R)^2 \ e^{-\alpha d}, \quad (2)$$

and

$$R= [(n-1)/(n+1)]^2. \quad (3)$$

The equation (3) permits us to determine the refractive index from the reflection measurements. After the values of the sample thickness and refractive index spectra are found, the absorption coefficient spectra are calculated from the results of transmission experiments. Better results can be obtained at wavelengths of transmission maxima, where most of radiation pass through the sample due to minimum losses for reflection. If fringes are not completely resolved, calculated absorption coefficient in the transmission minima will give artificially negative value, but at the same time, using transmission maxima gives good results.

In the intermediate region between multiple reflection at two sample surfaces and bulk conditions, the interference still influence the results, even if there are no visible fringes. The spectrum of reflection shown in figure 2 has a minimum at λ= 0.7 μm. The position of this minimum depending on the sample thickness, shifting in the direction of higher λ for thicker samples. At wavelengths to the left from this point, the front surface alone contributes to the total reflection since the optical transmission is close to zero. The drop of R with rising λ is the indicator of the refractive index reducing. This is the spectral range where equation (3) gives correct value of refractive index. To the right from the minimum, the rising of R indicates that the reflection from the back surface contributes more and more until this contribution becomes equal to the reflection from the front surface. Using simple equations (2) and (3) in this case yield higher then real values of refractive index (see data for the sample N3 in Figure 3 at $\lambda >$ 0.7 μm) and lower then real values of absorption coefficient (Sample P3 in Figure 4 at $\lambda >$ 0.8 μm). Thus, conventional transmission measurements do not give correct values of absorption coefficient near the edge.

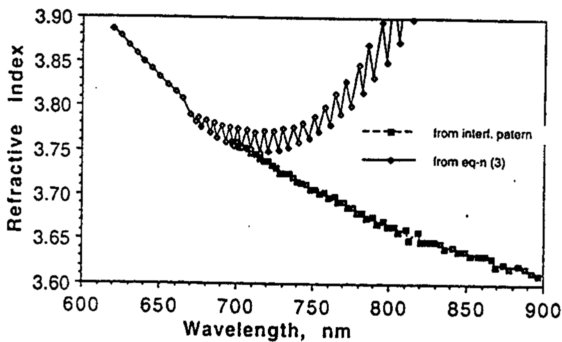

Figure 3. Refractive index spectra calculated from absolute value of R (eq-n 3) and from interference fringes.

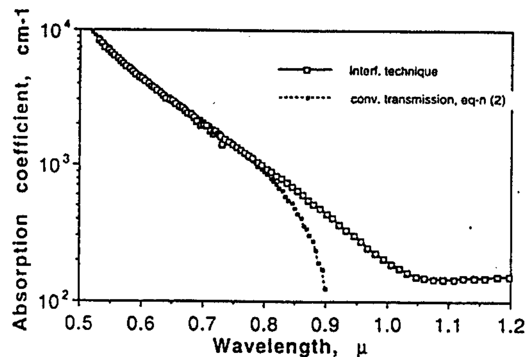

Figure 4. Absorption coefficient spectra from conventional transmission (eq-n 2) and by using interference technique.

EXPERIMENTAL RESULTS.

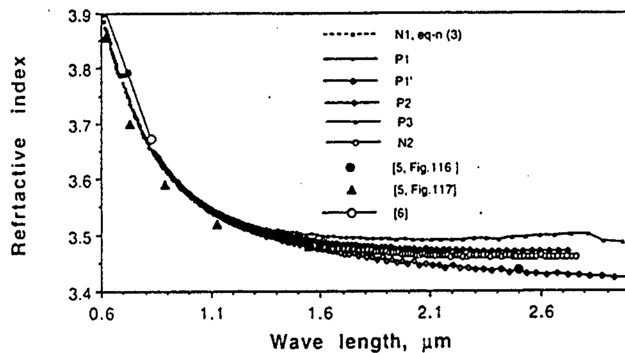

Figure 5. Refractive index spectra of samples with different doping level.

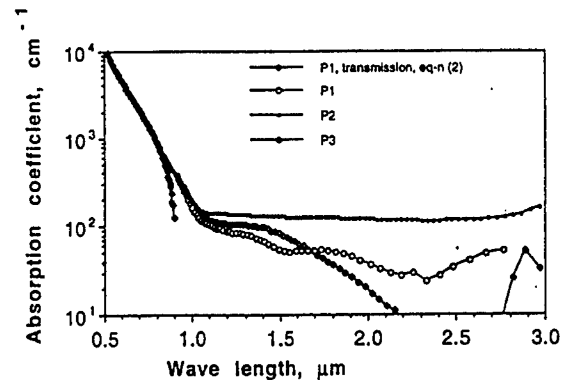

Figure 6. Absorption coefficient spectra of samples with different doping level.

Figure 5 demonstrate refractive index spectra. Literature data are also included. In the subgap spectral range the dispersion is week but the refractive index depends on doping level. Figure 6 demonstrate dependence of absorption coefficient on wavelength for p-Type Si membranes in the extended range. Data for the sample P3 calculated from equation (2) demonstrate fictitious drop of absorption at $\lambda > 0.8$ μm indicating necessity of using interference equation (1). Formulae (2) and (3), both start giving wrong results in this range even although transmission is still very low (at the level of 10-15 %) and fringes are not resolved. The wavelength at which this occurs depends on the sample thickness. For more thick samples this critical λ shifts in the direction of small absorption coefficient and large wavelength. At large wave lengths ($\lambda > 1.1$ μm), which correspond to the subgap energy range (photon energy $\hbar\omega$ < Eg), the absorption is related to impurities and defects. There is no direct evidence of the surface absorption since we could not find direct correlation of this absorption with the sample thicknesses. However, the high level of background absorption, independent of wave length, might indicate the presence of surface defects in some samples (sample P2 in Fig. 6).

CONCLUSIONS

Interference technique gives good agreement with results obtained by conventional transmission and reflection measurements in the range of high absorption, and permits to receive precise optical characteristics in the subgap range, where conventional methods do not work well.

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KINETICALLY UNSTABLE GROWTH OF SEMICONDUCTOR ALLOYS

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Spontaneously formed macroscopic composition–modulated structures have been observed in numerous alloys of III–V and II–VI semiconductors grown by MBE, MOCVD, VPE, and LPE (for a review, see, e. g. [1]). Conventional attempts to explain the phenomenon have used the concept of spinodal decomposition of an alloy [2,3]. The thermodynamic theory of [2,3] developed for metal alloys deals with *closed systems* where the alloy can lower its free energy by the formation of a composition–modulated structure. The kinetics of the spinodal decomposition [3] describes the evolution of an alloy from the initial homogeneous state which is quenched to a temperature, where it is thermodynamically unstable, to a finite equilibrium state, which is the alloy with spatial modulation of composition.

Although the theory of [2,3] can be extended to bulk samples and epitaxial films of semiconductor alloys [4], one should emphasize the basic difference between formation mechanisms and observation conditions of composition–modulated structures in metal alloys, on the one hand, and those in semiconductor alloys, on the other hand. *i)* The formation of composition–modulated structures in metal alloys occurs in closed systems under long time annealing (aging). For typical temperatures of aging, $T \approx 600 - 1000^0$ C, characteristic values of bulk diffusion coefficients are of the order of $D \approx 10^{-11} - 10^{-8}$ cm^{2}s^{-1}. These diffusion coefficients are sufficiently large to promote the formation of composition–modulated structures on an accessible time scale. *ii)* Composition–modulated structures in semiconductor alloys are observed in *as–grown* samples which implies that these structures are being formed *in open systems* in the process of the crystal growth. Bulk diffusion coefficients in semiconductors at typical growth temperature ($T \approx 600^0$ C) are of the order $D \approx 10^{-19} - 10^{-16}$ cm^{2}s^{-1} [5]. These diffusion coefficients are too small to develop a composition–modulated structure during the growth time, and another kinetic mechanism than the bulk migration of atoms is needed for the structure formation.

In the present paper we study the instability which may occur in an *open system* in the process of the growth of an binary alloy $A_{1-c}B_c$, and our treatment is applicable also to the growth of a ternary semiconductor alloy $A_{1-c}B_cC$. The focus is given on the instability of the alloy growth with respect to fluctuations of composition δc. The theory linear in δc is developed, and the criterion is found that the amplitude of composition fluctuation increases with the epitaxial film thickness. This means that the growth of a homogeneous alloy is unstable, and the growth may result in an alloy with a spatial modulation of composition.

We consider the growth of an alloy from the gas phase. We study the epitaxial film on a substrate where the monolayers from the 1st to the Mth are completed, and the $(M+1)$st monolayer is the growing one. Growth on atomically smooth surfaces proceeds via the surface migration of adatoms on and via their incorporation into the growing monolayer. In the process of the growth of each Lth monolayer $(1 \le L \le M)$, there appears the fluctuation of alloy composition $\delta c(\mathbf{r}; L)$, where $\mathbf{r} = (x, y)$ is the two–dimensional position vector. Since we neglect the migration of atoms in the bulk, the fluctuation of composition are "frozen" after the given monolayer is covered by subsequent monolayers.

First, "frozen" fluctuations of composition in the top completed Mth monolayer, $\delta c(\mathbf{r}; M)$, affect the migration of adatoms in the next, growing, $(M+1)$st monolayer via a short–range potential $U_{sr}^{(A,B)}(\mathbf{r}; M+1)$ acting on adatoms A and B. Second, "frozen" fluctuations in all completed monolayers $1 \le L \le M$ create, in accordance with the Vegard's rule, the long–range strain field. Therefore a long–range potential $U_{lr}^{(A,B)}(\mathbf{r}; M+1)$ appears

which is proportional to the strain tensor at the surface ε_{ij}. The total potential acting on adatoms is the sum of short–range and long–range terms,

$$U^{(A,B)}(\mathbf{r};M+1) = V_{sr}^{(A,B)}\delta c(\mathbf{r};M) + V_{lr\,ij}^{(A,B)}\varepsilon_{ij}(\mathbf{r};z)\Big|_{z=Ma}, \tag{1}$$

where the coefficients $V_{lr\,ij}^{(A,B)}$ may be called deformation potentials of the adatom A or B, and a is the lattice parameter. The strain tensor may be given in terms of the static Green's tensor $G_{ij}\left(\mathbf{r}-\mathbf{r}',z,z'\right)$ of the elasticity theory for the semi–infinite medium, found in Ref. [6]. For Fourier transforms, this relation reads

$$\widetilde{\varepsilon_{ij}}\left(\mathbf{k},z\right)\Big|_{z=Ma} = \left(\frac{\partial a}{\partial c}\right)\sum_{L=1}^{M}\frac{1}{2}\left[\nabla_i\nabla'_p\widetilde{G_{jp}}\left(\mathbf{k};z,z'\right) + \nabla_j\nabla'_p\widetilde{G_{ij}}\left(\mathbf{k},z,z'\right)\right]\Big|_{\substack{z=Ma\\ z'=La}}\widetilde{\delta c}\left(\mathbf{k};L\right). \tag{2}$$

The chemical potential of the rare gas of adatoms on the surface is the sum of the potential $U^{A,B}$ and of the entropy term related to the areal concentration of adatoms $N^{(A,B)}$, $\mu^{(A,B)}(\mathbf{r}) = U^{(A,B)}(\mathbf{r}) - T\ln(a^2N^{(A,B)}(\mathbf{r}))$. The gradient of the chemical potential in the inhomogeneous system causes the surface flux of adatoms [7], $\mathbf{j}^{(A,B)}(\mathbf{r}) = -T^{-1}D^{(A,B)}\nabla\mu^{(A,B)}(\mathbf{r})$, where $D^{(A,B)}$ is the diffusion coefficient. By substituting here the expression for the chemical potential, one gets the surface flux of adatoms as a sum of the contributions of diffusion and drift: $\mathbf{j}^{(A,B)}(\mathbf{r}) = -D^{(A,B)}\nabla N^{(A,B)}(\mathbf{r}) - T^{-1}N^{(A,B)}(\mathbf{r})D^{(A,B)}\nabla U^{(A,B)}(\mathbf{r})$.

If there is a oversaturation in the gas phase, there appears the flux of atoms from the gas to the surface which is characterized by the deposition rate $G_0^{(A,B)}$. The concentration of adatoms and surface fluxes of adatoms may be written as sums of equilibrium quantities $N_{eq}^{(A,B)}(\mathbf{r}), \mathbf{j}_{eq}^{(A,B)}(\mathbf{r})$ and excess non–equilibrium quantities $\Delta N^{(A,B)}(t;\mathbf{r})$, $\Delta\mathbf{j}^{(A,B)}(t;\mathbf{r})$ caused by the oversaturation. The excess surface flux of adatoms may be written in terms of the excess areal concentration of adatoms as a sum of diffusion and drift contributions,

$$\Delta\mathbf{j}^{(A,B)}(t;\mathbf{r}) = -D^{(A,B)}\nabla\Delta N^{(A,B)}(t;\mathbf{r}) - T^{-1}D^{(A,B)}\Delta N^{(A,B)}(t;\mathbf{r})\nabla U^{(A,B)}(\mathbf{r}). \tag{3}$$

The excess non–equilibrium areal concentration of adatoms $\Delta N^{(A,B)}(t;\mathbf{r})$ and the excess surface flux of adatoms $\Delta\mathbf{j}^{(A,B)}(t;\mathbf{r})$ obey the continuity equation:

$$\frac{\partial\Delta N^{(A,B)}(t;\mathbf{r})}{\partial t} + \mathrm{div}\Delta\mathbf{j}^{(A,B)}(t;\mathbf{r}) = G_0^{(A,B)} - \frac{\Delta N^{(A,B)}(t;\mathbf{r})}{\tau_{desorption}^{(A,B)}}. \tag{4}$$

Here $\tau_{desorption}^{(A,B)}$ is the average desorption time. We emphasize here that the deposition and desorption terms on the right hand side of Eq.(4) are particular features of an open system.

The set of coupled equations (3,4) allows to find the concentration of adatoms $\Delta N^{(A,B)}(t;\mathbf{r})$ and surface fluxes of adatoms $\Delta\mathbf{j}^{(A,B)}(t;\mathbf{r})$. Boundary conditions needed for these equations depend on the growth mechanism.

We focus on the step–flow growth on a surface vicinal to the (001) surface of a cubic crystal. A perfect vicinal surface displayed in Fig. 1 consists of (001) terraces of equal width L separated by monomolecular–height steps. Each step consists of [110] straight sections of equal length l_K separated by kinks. It was shown in Ref. [8] that the crystal growth on such a surface proceeds via kink flow and step flow, it can be stable against step bunching and step meandering, and the perfect geometry of the vicinal surface persists during the growth.

We consider fluctuations of composition where the characteristic scale of inhomogeneity r_0 is large compared to the spacing between kinks, and treat kinks as continuously distributed along steps (the so called approximation of continuous line sinks). These sinks are asymmetric with respect to lower and upper terraces since the barrier for adatoms approaching the sink from the upper terrace is higher than that for adatoms on the lower terrace. Corresponding boundary conditions at the nth line sink positioned at $x = x_n = nd$ read:

$$\left(D\Delta N(t;\mathbf{r}) + w_+ \Delta j_x(t;\mathbf{r})\right)\Big|_{x=x_n+\eta} = 0 \qquad \left(D\Delta N(t;\mathbf{r}) - w_- \Delta j_x(t;\mathbf{r})\right)\Big|_{x=x_n-\eta} = 0\,, \quad (5)$$

where w_+, w_- are parameters of the asymmetric sink defined in Ref. [9], and $\eta \to +0$.

The set of coupled equations (3,4) subject to the boundary conditions (5) has been solved in the perturbation series with respect to the parameter U/T up to the first–order terms, and both $\Delta N(t;\mathbf{r})$ and $\Delta \mathbf{j}(t;\mathbf{r})$ have been calculated [10]. After the fluxes of both adatoms A and adatoms B attaching the line sink at the given point are known, it is possible to find the fluctuation of alloy composition $\delta c(\mathbf{r})$ which is being frozen at this point of the growing monolayer. The fluctuation $\delta c(\mathbf{r}; M+1)$ formed after the completion of the $(M+1)$st monolayer is found in the form of the linear response to the potential $U^{(A,B)}(\mathbf{r}; M+1)$ which was acting on adatoms during the growth of the $(M+1)$st monolayer. This relation reads for Fourier transforms of δc and U:

$$\widetilde{\delta c}(\mathbf{k}; M+1) = \frac{\bar{c}(1-\bar{c})}{T}\left[R^A(\mathbf{k})\widetilde{U^A}(\mathbf{k}; M+1) + R^B(\mathbf{k})\widetilde{U^B}(\mathbf{k}; M+1)\right]\,, \qquad (6)$$

where response functions $R^A(\mathbf{k})$, $R^B(\mathbf{k})$ are determined by the kinetics of adatom migration on the stepped vicinal surface.

The set of linear equations (1,2,6) describes the dependence of alloy composition fluctuation $\widetilde{\delta c}(\mathbf{k}; M)$ on the monolayer's number M. It was shown in Ref.[10] that one may seek the solution in the exponential form $\widetilde{\delta c}(\mathbf{k}; L) \sim \exp(\gamma k a L)$. Then the inequality $\mathrm{Re}\gamma(\mathbf{k}) > 0$ yields the criterion that the fluctuation amplitude increases with the monolayer's number.

The mechanism responsible for this amplification is the drift of adatoms of the growing monolayer in the effective potential U created by the "frozen" fluctuations of alloy composition in the completed monolayers. The diffusion component of the surface flux of adatoms tends to smooth out fluctuations of composition. For high temperatures, diffusion dominates drift, and no amplification of fluctuation occurs. At a certain critical temperature T_c and at a certain wave vector $\mathbf{k_c}$ there appears amplification of the fluctuation amplitude. This temperature is the temperature of *kinetic phase transition* between the growth of the homogeneous alloy and the growth of the alloy with spatial modulation of alloy composition. At temperatures below T_c, drift dominates diffusion, and there exists a region in the $\mathbf{k}$–space where fluctuations of composition increase from monolayer to monolayer.

The temperature T_c and the wave vector of the most unstable mode $\mathbf{k_c}$ are determined by the interplay of several tendencies. First, the Green's tensor from Eq.(2) is determined by the symmetry of bulk elastic moduli. Second, the symmetry of the deformation potential $V_{lr\,ij}^{(A,B)}$ from Eq.(1) is determined by the symmetry of the surface. Third, the $\mathbf{k}$–dependence of the response functions $R^{(A,B)}(\mathbf{k})$ is governed by the particular kinetics of adatom migration on the stepped vicinal surface. As a result of this interplay, any direction of the wave vector of the most unstable mode of composition fluctuations ("the soft mode") is possible.

Calculations of the kinetic phase transition temperature show that T_c increases with the increase of adatom deformation potential. It means that, in contrast to the effect of long–range elastic forces on the thermodynamic instability of alloys, where they hinder the phase separation, they *favor kinetic instability.* The reason is that adatoms are attracted by domains of the surface with the excess concentration of like atoms, i. e., atoms with larger radius are attracted by domains which are under tensile strain, and smaller atoms are attracted by domains under compressive strain.

Fig. 2 displays the result of model calculations of $\mathrm{Re}\gamma(\mathbf{k})$ which have been performed for $d = 100a$, $l_k = 10a$, $w_+ = 0.01$, $w_- = 0.2$, isotropic deformation potential, and anisotropic diffusion coefficient of adatoms ($D_{yy}^{(A)} = 5D_{xx}^{(A)}$, $D_{yy}^{(B)} = 5D_{xx}^{(B)}$), and $T = 0.7T_c$. There is a region of unstable modes with $\mathrm{Re}\gamma > 0$ with small k_y satisfying the criterion $|k_y| l_K \ll 1$ which justifies the approximation of continuous line sinks.

To conclude, the kinetic mechanism is proposed of the amplification of alloy composition modulation with the thickness of the epitaxial film. Long–range elastic interaction favors the kinetic instability and results in the increase of the kinetic phase transition temperature.

For different values of material parameters, one may expect the appearance of composition-modulated structure with any orientation.

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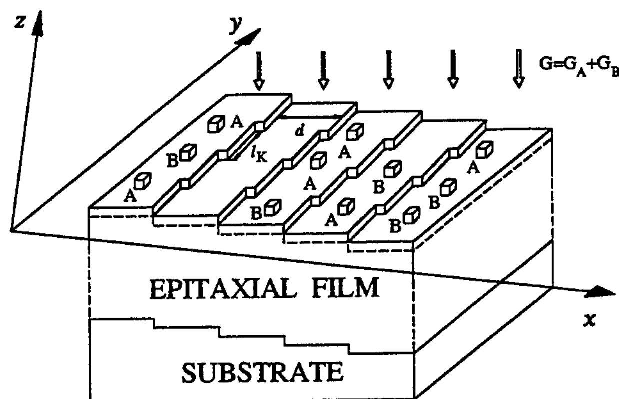

Fig. 1. Growth of an alloy on a vicinal surface. Monolayers are defined in such a way that they repeat the stepped shape of the substrate. The dashed line depicts the top completed monolayer.

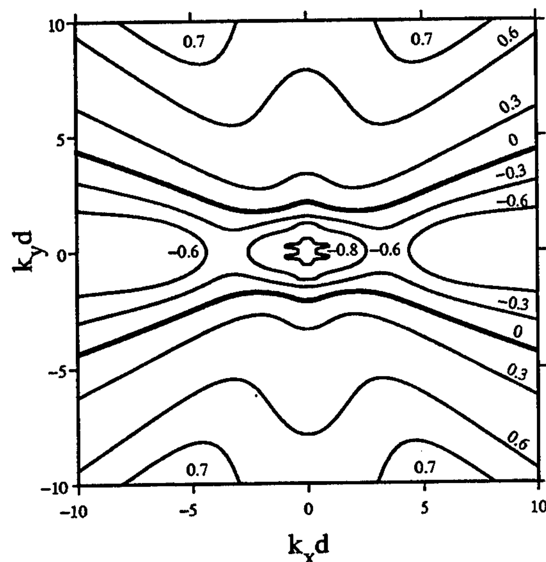

Fig. 2. Amplification coefficient Re$\gamma(\mathbf{k})$ as a function of the 2D wave vector. Regions in the $\mathbf{k}$-space where Re$\gamma > 0$ correspond to unstable fluctuations.

A New Fabrication Technique for Nb Diffusion-Cooled Hot-Electron Bolometers

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Much has appeared in the recent literature about the use of superconductive transition-edge bolometers[1]. Such devices, possessed of very short thermal response times, can be employed as mixers capable of operating to rf frequencies of many terahertz[2]. At such frequencies, these bolometer mixers find wide application to molecular line spectroscopy suitable for space and planetary science.

The bolometer addressed in reference [1] consists of a niobium strip 140 nm wide by 270 nm long by 10 nm thick on a quartz substrate. It is fabricated from a bilayer film consisting of 10 nm of Au atop 10 nm of Nb, where the bolometer element is defined by a chromium etch mask patterned using electron beam lithography and lift-off. Subsequent steps (1) remove the bilayer film from everywhere but underneath the chromium etch mask which protects the microbridge and, using a wet-etch process, the chromium mask itself, (2) thermally deposit 100 nm of bulk gold to form the normal metal contacts, (3) lift-off this gold from atop the microbridge – which step defines the bolometer length – and, (4) remove the 10 nm layer of gold which remains atop the Nb microbridge. In this paper, we suggest a new method of fabricating the bolometer microbridge which should allow for excellent control of the device dimensions.

This method employs a Ga^+ Focussed Ion Beam (FIB) mill to physically carve the bolometer geometry. We start with a quartz substrate upon which are deposited layers of Nb and Au with Cr on top to serve as an etch mask (Fig. 1). This wafer is then patterned and etched down to the quartz over its entire surface except for the area of the bolometer contacts – the eventual site of the bolometer itself (Fig. 2).

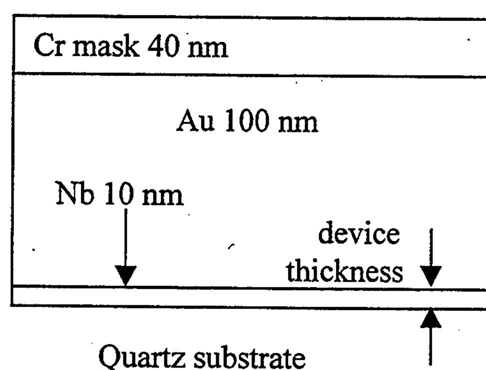

Figure 1. Side view: wafer cross-section.

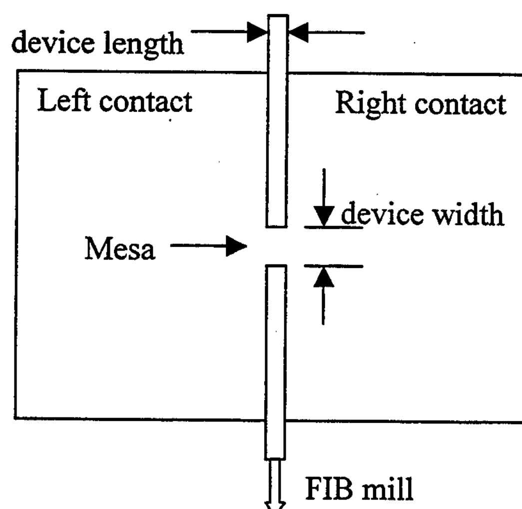

Figure 2. Top view. The FIB mill divides the contact pads, leaving a thin connection which will become the bolometer.

Next the FIB is used to mill away the metal films along the line indicated in Fig. 2, except for a mesa which is allowed to remain in the center of the contacts. Since the mill is completed completely through the metals and into the quartz, this mesa (see Fig. 3) is the only conductive path between the contacts, and it defines the length and width of the bolometer.

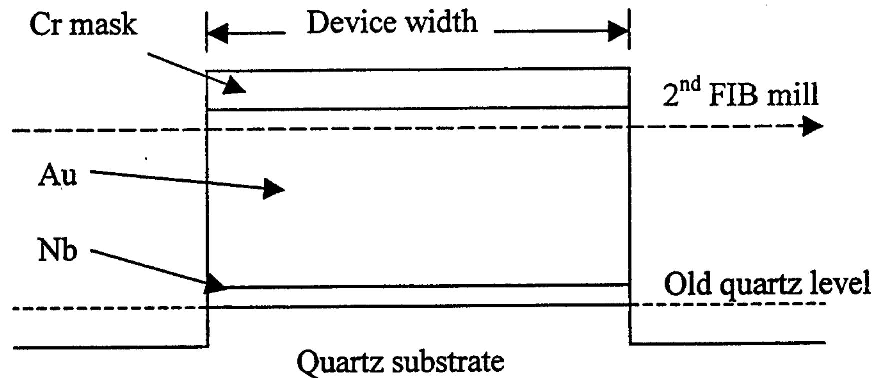

Fig. 3. Mesa cross-section, from top to bottom in Fig. 2. Note that the first FIB mill enters the substrate, removing all electrical connection between the contact pads except at the mesa position. A second FIB mill will remove the chrome mask on the mesa from atop the gold layer, allowing it to be removed.

A subsequent, lower-power FIB mill is used to remove the thin chrome mask from atop the mesa, exposing a layer of gold which is selectively removed by a low-voltage Ar sputter-etch process. Fabrication is completed when the masking chrome is removed with a wet etch. What results is two bulk contacts joined by a thin Nb microbridge whose dimensions are easily controlled by the FIB microscope.

We expect this to be a robust and flexible method of bolometer fabrication for several reasons. Firstly, the site-specific nature of the FIB work means that bolometer processing need not affect other devices on the same wafer. Secondly, the use of bulk gold atop the niobium layer out of which the device is eventually formed greatly simplifies device processing. Most importantly, however, we feel this to be a robust process because it involves only two steps with no photolithographic processing of the microbridge or lift-off steps. We plan additionally to investigate the possibility of turning the bolometer fabrication into a one-step process by using endpoint detection on the FIB mill to facilitate in-situ removal of the gold layer from atop the Nb microbridge.

In conclusion, it should be pointed out that the FIB mill is nominally capable of focussing a beam of Ga^+ ions to a dot 5 nm in diameter. Therefore it is not unreasonable to consider device dimensions of 50 nm by 30 nm by 10 nm thick in the near future, representing a 25-fold reduction in device volume.

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Machine Aligned Fabrication of Submicron Nb/Al-AlO$_X$/Nb Junctions using a Focused Ion Beam

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1. Introduction

In this abstract, a process is described that we are developing which uses a Ga^+ focused ion beam (FIB) for the fabrication of Nb/Al-AlO$_x$/ Nb superconductive-insulating-superconductive (SIS) tunnel junctions. The objective is to use a machine alignment scheme for the definition and insulation of junctions with diameters less small as 0.5μm for high critical current density (J_C) applications. The fabrication of such ultra-small area SIS junctions has typically only been achieved using electron beam lithography and a multi-resist layer scheme [1]. Typical techniques for the fabrication of SIS junctions use a self-aligned resist lift-off process. The resist pattern is used to define both the junction counter electrode and the subsequent insulation field that insulates the base electrode from the wiring layer. The wiring layer contacts the junction counter electrode through a via in the insulation field that is created during resist lift-off.

Figure 1 shows a Nb based self aligned trilevel resist junction insulation process, which is used in this laboratory for fabricating micron-scale SIS junctions. As can be seen from the figure, the trilevel resist is used both as the etch mask for the junction counter electrode (Fig. 1a) and as the deposition mask to the SiO insulation layer (Fig.1b) so that a via in the SiO is created after lift-off (Fig.1c) to the top of the junction Nb counter electrode. A subsequent Nb wiring layer can then interconnect different junctions and electrical elements on the wafer [2]. Generally, such self aligned insulation processes are effective for junctions sizes on the order of a micron or larger [3]. As junction sizes are decreased; however, the lift-off process becomes more difficult to perform and from our experience, it becomes inherently more difficult to successfully insulate the junction for the wiring step. With conventional lithography,

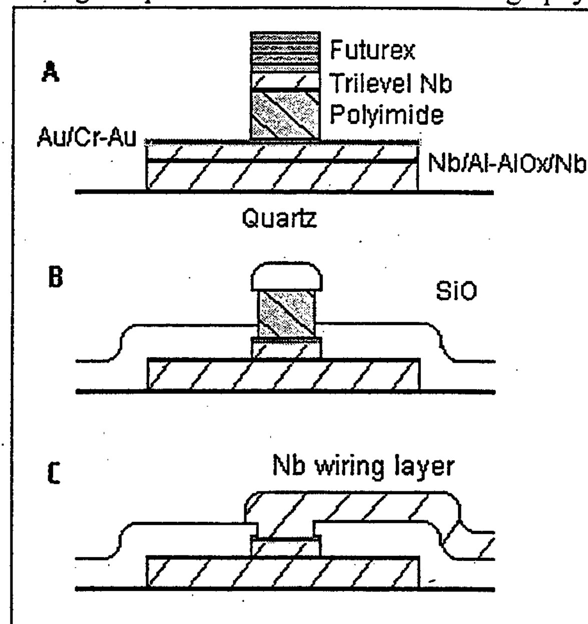

Figure 1 (A) Self-aligned trilevel (Futurex/Nb/ Polyimide) sitting atop an unetched SIS junction. (B) SiO shown covering an etched SIS junction. (C)The SiO is then lifted-off from atop the junction, allowing the Nb wiring layer to contact the junction.

it also becomes more difficult to accurately define junctions smaller than 1μm with a resist feature that is also compatible with the lift-off of the thick junction insulation layer. Conceptually, an alternative to such a self aligned process is a machine aligned method

where the Nb junction etch and the SiO insulation and via definition steps are decoupled and the necessary alignment of the two features are typically done with some lithography tool. Such a process, which decouples the two steps, is very attractive for several reasons: (1) it allows the use of different lithography processes for the two steps, (2) the junction should be very well insulated since it is initially totally "buried" by the insulation layer and (3) it avoids the use of any lift-off processes.

The main drawback with such a process is while for large area junctions the alignment, definition and etching of the required insulation via to the Nb junction counter electrode is feasible, for small junction areas the alignment tolerances are critical. For a 0.5μm diameter junction with a 0.2μm diameter via hole, the via must be aligned to better than 0.15μm in order for the via hole to be registered only on top of the junction. Such tolerances are beyond most commonly used lithography tools.

2. Machine Aligned FIB Technique

We are investigating a machine aligned junction insulation process where the critical alignment and via definition is accomplished with a Ga^+ FIB etching system. The FIB used in this research is an FIB 200 Series Workstation manufactured by FEI Company [4]. Incorporating the FIB into the fabrication process allows for the alignment of sub-micron features, which is not feasible with optical lithography alone.

In this process, the Nb junction counter electrode is defined and insulated in a separate step. This permits the use of, in our case, a thin DUV resist with good resolution of half-micron feature sizes that would otherwise not be suitable for a full self-aligned junction insulation process. After stripping the resist, the junctions are "buried" with a blanket evaporation of 100-300nm of SiO over the entire wafer (Fig. 2a). A thin layer of Cr (20nm) is then deposited on top of the SiO to improve the imaging capabilities of the Ga+ beam in the FIB system. The excellent registration and anisotropic etching capabilities of the FIB system are then used to directly etch a hole in the Cr film directly above the junctions. Alignment is feasible due to the outline of the junction perimeter that is transferred through the SiO layer for registration. The FIB beam is controlled such that the etch is through the thin Cr mask layer but not totally through the much thicker SiO insulation layer (Fig. 2b). The Cr then serves as a mask for an anisotropic CHF_3 reactive ion etch (RIE) of the SiO via. In our process a thin $Cr_{0.1}$-$Au_{0.9}$ layer was previously defined on top of the junction counter electrode to serve as an etch stop for the CHF_3 RIE as well as to promote adhesion between the counter electrode and the Nb wiring layer [5]. The Cr mask layer can now be removed with a simple wet etch before the deposition and definition of the Nb wiring layer, which contacts the Nb junction counter electrodes through the SiO vias (Fig. 2c). To date, via features as small as 200nm have been easily formed using the FIB. The ion column of the FIB uses an ultra-rigid mechanical assembly to ensure beam position and high resolution images, allowing for spot diameters down to 30nm [4]. We therefor anticipate the capability to define via holes smaller than 100nm.

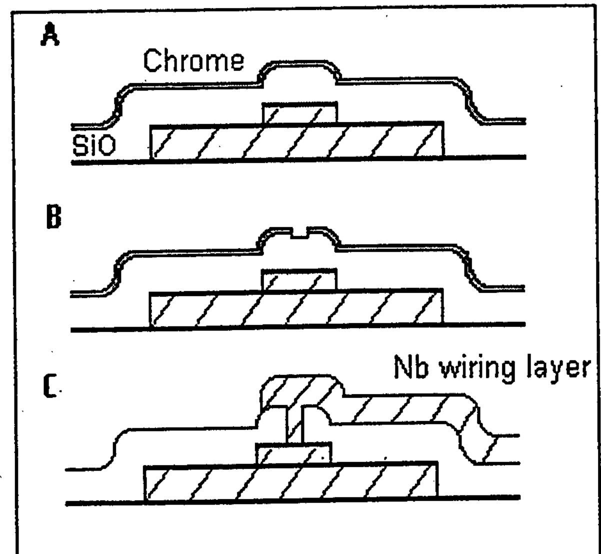

Figure 2 (A) SiO is allowed to deposit directly on top of the SIS junction along with a thin Cr layer. (B) The Cr is then patterned using the FIB. (C) A subsequent RIE of the SiO allows the Nb wiring layer to be contacted to the junction.

To facilitate the control of the FIB Cr etch, an end point detection (EPD) program is used during the etch. The EPD indirectly detects the type of material being milled by measuring the amount of current ejected from the wafer surface during the etch. For example, if the EPD program measures a drop in observed current during an etch, a transition from a conductive material to a less conductive material may be inferred. This tool is therefore very useful in controlling the duration of the FIB etch so that it does not proceed into the Nb counter electrode.

One drawback to this proposed machine aligned FIB junction insulation process is that while with common lithography techniques an entire wafer can be patterned with a single exposure, with the FIB process the SiO vias will be individually defined. It is not clear how robust the process is at this time and whether the etching of the via patterns in the Cr layer can be written and controlled by a computer program much like E-beam lithography.

It is also interesting to note that this technique of defining small insulation vias has an analogous application in the fabrication of Schottky barrier diodes. For the case of whisker contact diodes, the critical step in defining diode areas involves opening a small diameter via in an insulation field to a GaAs surface [6]. Schottky barrier contacts are then formed in a platting process defined by the insulation vias. The FIB SIS junction insulation process should be readily transferable to the fabrication of 100nm diameter whisker-contacted Schottky diodes. Since this application does not require any alignment, it is likely that an array of such via patterns can be "written" using the FIB in a reasonable time frame under computer control.

3. Summary

A new method for defining submicron SIS junctions has been described. Using the small Ga^+ beam size, anisotropic etching and precise alignment capabilities of the FIB system, a machined aligned insulation technique has been described. This new process will allow for the fabrication of sub half-micron junctions with high critical current densities. The use of the FIB system decouples the junction electrode and junction insulation steps in order to avoid lift-off processes, which are problematic for submicron junctions.

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Real Space Transfer of Holes in p-Channel HFETs

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Summary

We present experimental evidence of Real Space Transfer (RST) of holes in a p-type HFET with 0.8 x 10 μm^2 gates at 77 K and room temperature. The hole RST manifests itself via the gate current increase with an increase in HFET drain voltage. The hole RST is less pronounced than electron RST in n-channel HFETs and is suppressed at higher temperatures (373 K).

Introduction. The application of large gate and drain voltages to n-channel enhancement mode Heterostructure Field Effect Transistors (HFETS) causes some of the channel electrons to be accelerated to such high speeds that they can escape across the barrier towards the gate (see Shur et al. [1], Maezawa and Mizutani [2], Laskar et al. [3], and Martinez et al. (4]). This effect is named Real Space Transfer of electrons (RST)[5]. RST may lead to a large increase in gate current with drain bias. This feature allows one to operate an HFET as a Hot Electron Transistor (HET) in a regime where the input is the drain voltage and the output is the gate current. The HFET, operating in the HET mode is similar to a Charge Injection Transistor (CHINT) [6]. In this regime, the device transconductance is defined as $d(I_g)/d(V_d)$ where V_d is the drain-to-source voltage and I_g is the gate current. The transconductance in the HET mode can be an order of magnitude larger than in a conventional mode of operation [4]. The HET mode is also expected to have a higher frequency of operation, limited primarily by the energy relaxation time [6]. In this paper we present, for the first time, experimental evidence that RST of holes can occur in p-channel HFETS.

Experimental results and discussion. The investigated HFET structure is shown in Figure 1. This structure uses a pseudomorphic channel ($In_{0.2}Ga_{0.8}As$) to enhance the electron and hole transport in n- and p-channel devices and a high band-gap $Al_{0.75}Ga_{0.25}As$ layer for charge control. The gate length and gate width are 0.8 and 10 μm, respectively. The device fabrication has been described elsewhere [7].

Figure 2 shows the measured dependencies of the gate current on the drain voltage at 77 K, 293 K, and 373 K with a -3 V gate voltage. As can be seen from the figure, at 373 K, the gate current monotonically decreases with the increase in the drain bias. Qualitatively, this behavior can be explained using a simplistic two diode model, one diode being connected between gate and source and the other between gate and drain. Both diodes carry current due to the applied voltages between these electrodes. As the drain bias increases, the voltage drop across the gate-to-drain diode becomes smaller and when the drain voltage exceeds the gate voltage the gate-to-drain diode becomes reverse-biased and the diode current becomes negligible. Hence, the gate current is expected to decrease with an increase in the drain bias. The two diode model predicts that at large drain bias, the gate current should approach one half of its value at zero drain bias since the gate-to-drain diode is blocking and the gate-to-source diode does not depend on drain voltage. Figure 2 shows that, in fact, with an increase in the drain-to-source voltage, the gate current decreases to a much smaller fraction of its original value.

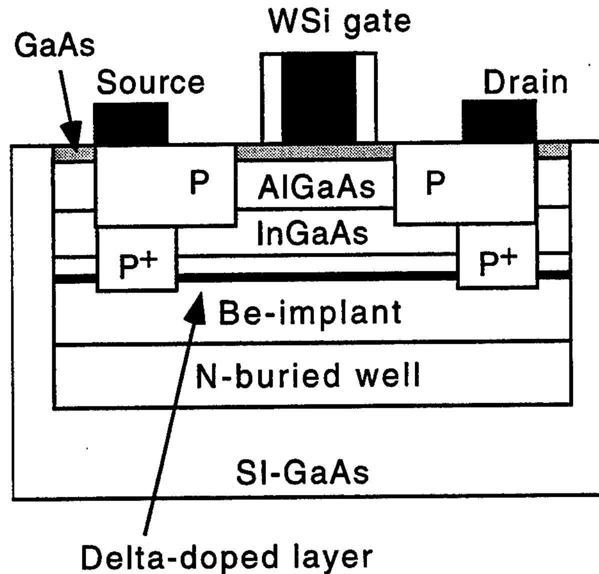

Figure 1. Schematic of p-channel $Al_{0.75}$ $Ga_{0.25}As/In_{0.2}Ga_{0.8}As$ HFET. The structure is grown on semiinsulating GaAs and all layers are grown without doping except for the Delta-Doped layer (which is chosen to adjust the threshold voltage of the n-HFETs.) The n-buried well implantation is used for device isolation and the Be Vt Shift implantation controls the threshold voltage of the p-HFET (n-channel devices are also fabricated on the same wafer.)

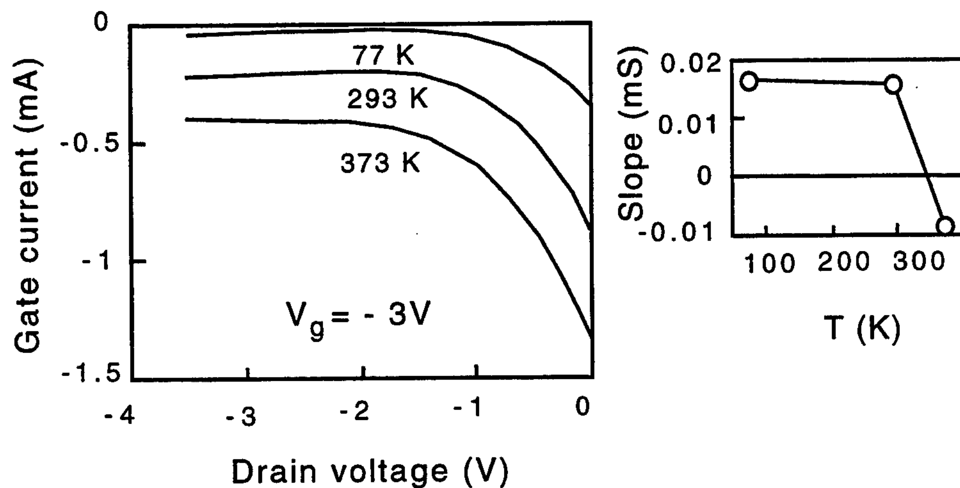

Figure 2. Gate current versus drain-to-source voltage for three different device temperatures. Also shown the value of the gate current slope in the high drain bias region. The gate voltage is -3 Volts.

This effect may be due to the distribution of the gate current over the channel or due to a large source resistance. However the source resistance mechanism which may be responsible for the gate current decrease is not dominant in our devices since the gate current is nearly saturated at high drain voltages at which the drain current continues to increase (see Figure 3).

At a large drain bias, a considerable fraction of the channel can become reverse-biased. The observed saturation of the gate current at large drain biases is primarily related to the formation of a high field region near the drain caused by the velocity saturation. The width of this region is a slow (logarithmic) function of the drain bias (see, for example, [8], and the potential distribution outside of this high region (where most of the gate current flows) is nearly unaffected by the drain bias.

The most interesting feature of the gate current dependence on V_d is an increase in I_g with the drain bias, i.e. the gate current curve has a positive slope when measured at high drain bias and low temperature (77 and 293 K). The insert in Figure 2 presents the slope $\Delta I_g/\Delta V_d$ at V_d = -3 V and emphasizes positive values at the lower temperatures. This behavior is similar to that observed in n-channel HFETs (see [l]-[41) where it was explained by the electron RST, and the increase in the gate current observed in our p-channel devices is a clear indication of the hole RST. A smaller increase in the gate current compared to that in the n-channel HFETs is caused by a higher effective mass of holes. In other words, it is more difficult to obtain hot holes than hot electrons. The disappearance of the hole RST at high temperatures is also caused by the low probability to generate hot holes. With rising temperatures scattering of the holes increases, resulting in an even lower probability to observe hot holes.

In p-channel HFETS, the light holes are heated in the high field region near the drain and experience the RST. The heavy-to-light hole transitions replenish the light holes. The key requirement for the observation of the RST in HFETs is that the carrier heating should occur in the section of the channel where the channel potential is smaller than or close to the gate voltage. This is why the RST effects are only noticeable at fairly high gate voltages in both n-channel and p-channel HFETS.

The device characteristics shown in Figure 2 were measured both at DC and using a pulse mode to ensure that Joule heating plays no role. The results of these measurements were completely identical.

Figure 3 shows the measured dependencies of the drain current on the drain voltage at 77 K for the same device. In n-channel transistors, the RST often leads to a negative differential resistance in the saturation region at high gate voltages [1].

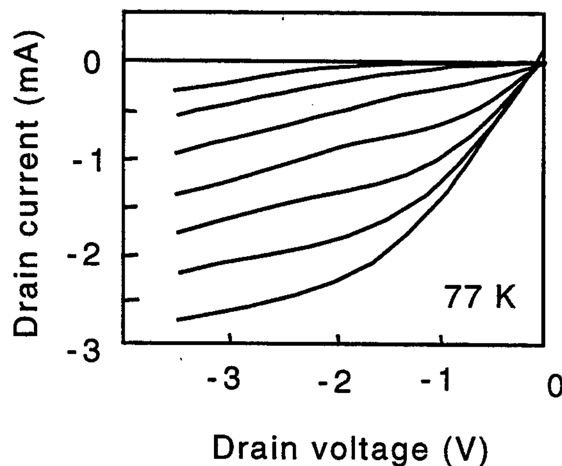

Figure 3. Drain-to-source characteristics of a p-channel HFET operated in normal mode at 77 K. The bottom curve is for V_g = - 3 V, step 0.5 V.

In the p-channel device, this negative resistance is not observed since the hole RST is much less pronounced. There is, however, a reduction in the drain conductance with increase in the gate voltage in the saturation region, consistent with the RST mechanism.

The RST effects in p-channel HFETs should strongly depend on the valence band discontinuity which determines the height of the barrier separating the channel from the gate and on the gate length which affects the potential distribution in the channel. Generally speaking, shorter channel HFETs and HFETs with a larger valence band discontinuity should have stronger RST effects. Hence, we expect that the design of p-channel HFETs may be optimized to achieve sufficiently strong RST effects to make viable complementary HFETs operating in Hot Electron Transistor and Hot Hole Transistor regimes.

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Effect of Surface Recombination on HBT Performance

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Abstract

The effects of the surface recombination at the extrinsic base region on the Early voltage and base transit time are investigated for AlGaAs/GaAs HBTs. It is observed that a reduction in Early voltage and an increase in base transit time exist due to surface recombination at the extrinsic base region.

Summary

Early effect, due to base width modulation with V_{bc} in BJTs, is a major source of nonlinearity in this class of devices. The discussion of the effects of the surface recombination on the Early voltage [1] will proceed as follow. The excess carrier concentration in HBTs is a strong function the proper partitioning of current between the thermionic emission and the tunneling as well as the quasi-fermi level splitting at the emitter-base space charge region. The excess electron carrier concentrations at the emitter-base junction can be expressed as [2]

$$\hat{n}(0) = \frac{n_{a0} \cdot [exp(V_{be} / kT - 1) - \frac{1/S_e}{W_B/D_n + 1/S_c}]}{1 + \frac{1/S_e}{W_B/D_n + 1/S_c}}$$

where n_{a0} is the base doping concentration, S_e (S_c) is the emitter (collector) junction velocity, W_B is the quasi neutral base with, D_n is the diffusivity of the minority carrier at the base. Surface recombination current is expressed as $J_S = q \cdot \hat{n}(0) \cdot S_S$ In the absence of any space charge and neutral base recombination, the collector current for the DHBTs in the presence of surface recombination is given as,.

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$$J_c = -\frac{q \cdot n_{a0}}{(\frac{W_B}{D_n} + \frac{1}{S_e} + \frac{1}{S_c})} \cdot [1 - (\frac{W_B}{Dn} \cdot S_s)] \cdot (e^{qVbe/kT} - e^{qVbc/kT})$$

where n_{a0} is the equilibrium minority carrier concentration at the edge of the emitter-base depletion region on the emitter side. Early voltage, $V_A \sim J_C/(dJ_c/dV_{bc})$ [3], in the presence of surface recombination can be expressed as:

$$V_A^{-1} = -[(\frac{1}{S_e} + \frac{1}{S_c} + \frac{W_B}{D_n})^{-1} \cdot (\frac{d}{dV_{bc}}(\frac{1}{S_c}) + \frac{1}{D_n}\frac{dW_B}{dV_{bc}}) + (\frac{D_n}{S_s} + W_B)^{-1} \cdot \frac{dW_B}{dV_{bc}}]$$

The minority carriers transport across the neutral base region, i.e. the base transit time τ_b, is one of main factors which effects the high-frequency performance of HBTs. The base transit time is strongly related to the injected excess carrier concentrations across the emitter-base junction and the collector current density. The injected electron concentration profile $n(x)$ is given as

$$n(x) = \frac{J_n}{q}\{\frac{n_{ie}^2}{N_A(x)}[\int_x^{W_B} \frac{1}{D_n}\frac{N_A(x)}{n_{ie}^2(x)}dx + \frac{1}{S_e}\frac{N_A(0)}{n_{ie}^2(0)} + \frac{1}{S_c}\frac{N_A(W_B)}{n_{ie}^2(W_B)}]\}$$

The transit time τ_b in the neutral base region is defined as $\tau_b = q \cdot \int_0^{W_B} n(x)dx \big/ J_n$ [4] and can be expresses as:

$$\tau_b = \{\int_0^{W_B} \frac{n_{ie}^2(x)}{N_A(x)} \int_x^{W_B} \frac{1}{D_n(y)} \frac{N_A(y)}{n_{ie}^2(y)} dydx + (\frac{1}{S_e}\frac{N_A(0)}{n_{ie}^2(0)} + \frac{1}{S_c}\frac{N_A(W_B)}{n_{ie}^2(W_B)})$$

$$\int_0^{W_B} \frac{n_{ie}^2}{N_A(x)} dx\} / (1 - \frac{W_B}{D_n} \cdot S_s)$$

Surface recombination velocity as a function of excess carrier is almost a constant, $S_s = S_0$ up to a certain excitation level and the recombination rate, $R \sim \hat{n}(0)$. However, for relatively high excitation level, $S_s \sim \hat{n}(0)^{-1/2}$ and $R \sim \hat{n}(0)^{1/2}$. Fig. 1 shows the calculated V_A for the classical BJTs ($S_c = \infty$), SHBTs ($S_c = v_{th}$) [5], DHBTs without taking into account the surface recombination and DHBTs with the surface recombination. This simulation is performed with V_{be}, 1.4V and T=300°. At a high reverse bias, V_{bc}, Early voltage in DHBT's with surface recombination, V^{SR}_A is significally small comapred to the early voltage of DHBT's without surface recombination. This can be explained by noting that the recombination at e-b junction reduces the amount of carrier transport to the collector, thereby, reducing the collector current density accompanied by a reduction in the effective velocity at b-c junction, S_c, which approaches to thermal velocity, V_{th}. On the other hand at low reverse bias, surface recombination does not affect V_A significally in either DHBTs.

From Fig. 2, the V_A remains unchanged with any change of V_{be} for DHBTs in the absence of surface recombination. V_A is reduced as V_{be} is decreased for DHBTs in the presence of surface recombination. With increasing V_{be}, more excess carriers will be injected from emitter to base. As the excess carrier concentration exceeds the critical

excess carrier concentration, surface recombination velocity is reduced dramatically. Therefore, Early voltage is not strongly effected by surface recombination at the base under high applied voltage. At lower bias, V_{be}=0.8V, surface recombination dominates base current density resulting in a degraded early voltage.

Fig. 3 shows effect of surface recombination on base transit time as a function of emitter-base voltage., Surface recombination modifies the collector current density making the affect of surface recombination on transit time is stronger at low V_{be} than that at a higher V_{be} for V_{bc}=2V. For emitter-base bias less than 1.4V, surface recombination is the major source of the base recombiantion. Therefore, collector current density is reduced by surface recombination while base transit time increases. Fig. 4 shows the behavior of τ_b with varying effective base width at V_{be}=0.8V both in the presence and absence of surface recombination.

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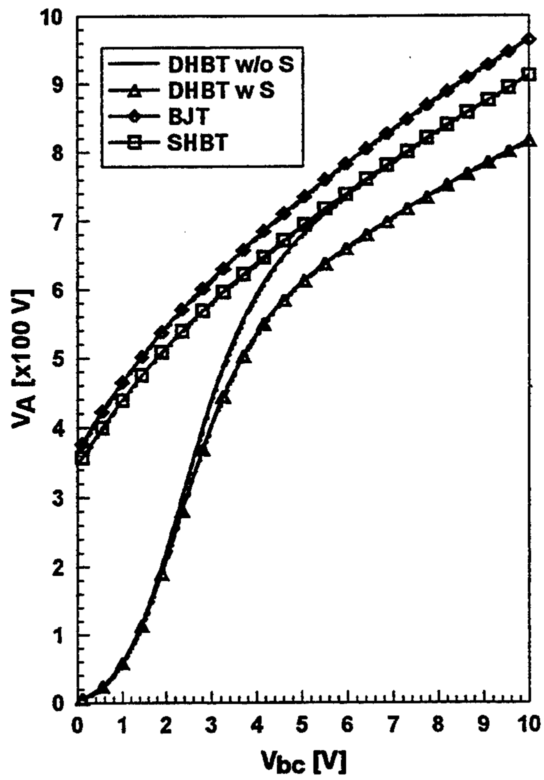

Figure 1. V_A for the BJT, SHBTs, DHBTs

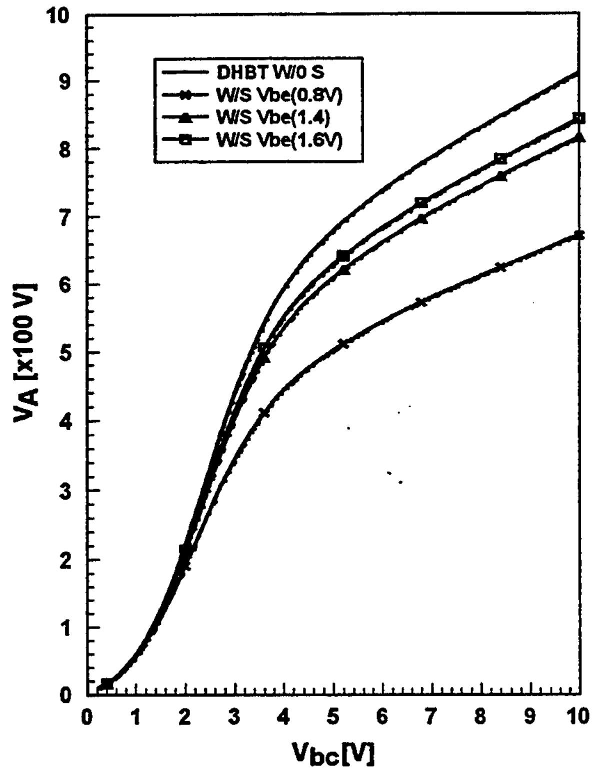

Figure 2. V_A for various V_{be} with/without surface recombination for DHBTs

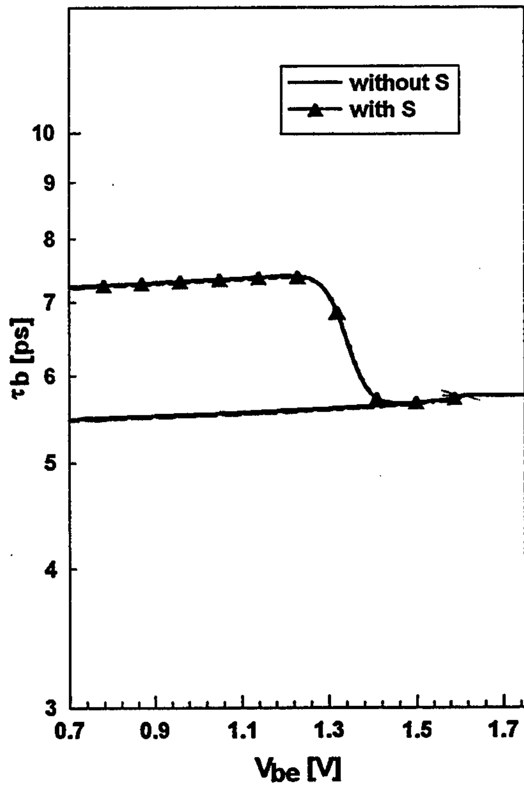

Figure 3 Transit time vs. V_{be} at V_{bc}=2V

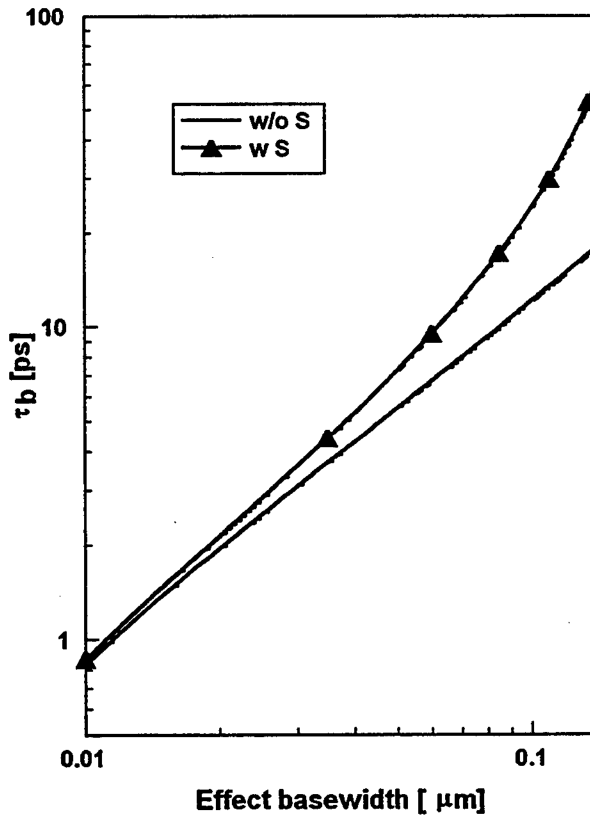

Figure 4. Transit time vs. base width at V_{be}=0.8V

A Model for AlGaAsSb/InGaAs/AlGaAsSb HEMTs

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ABSTRACT

A model is presented to predict the overall performance of AlGaAsSb/InGaAs/AlGaAsSb High Electron Mobility Transistors (HEMTs). The computations provide the current-voltage, small signal and noise performance of this class of HEMTs and may be used to provide design guidelines for achieving ultra low noise HEMTs in this emerging material system. Impact ionization is introduced through Shockley's lucky electrom model. A conduction band discontinuity of 0.6345eV at the $In_{0.53}Ga_{0.47}As/Al_{0.6}Ga_{0.4}AsSb$ heterointerface provides excellent two dimensional electron gas confinement. Predicted noise performance of HEMTs fabricated using the ternary/quaternary system is less than 1dB at 60GHz for an unoptimized structure.

EXTENDED ABSTRACT

Model

Modeling of noise is based upon a self-consistent solution of Schroedinger and Poisson's equations. The quantum well (QW) is formed in InGaAs and Schroedinger equation is solved by approximating the well by straight lines. The solution of Schroedinger equation requires values of the band offset between the lattice matched AlGaAsSb buffer and InGaAs QW and the effective masses in the barriers and in the QW [1]. The determination of the band offset follows the method developed by the present authors. For a type-I heterointerface the Al mole fraction needs to be greater than 0.5 otherwise a staggered type-II heterointerface will result. The Sb mole fraction is decided by the requirement of lattice match [2].

The QW formed in InGaAs is approximated by straight lines and Schroedinger's equation is solved using Airy functions. The calculated average distance of the electron cloud, from the first heterointerface, and the position of the Fermi level are expressed by the followinf functional forms and are used in the evaluation of the dc, small signal parameters and noise [3, 4, 5]:

$$x_{av} = a + b \cdot ln(n_s) \qquad (\mathring{A}) \qquad (1)$$

$$E_F = E_F(0) + \gamma \cdot ln(n_s) \qquad (eV) \qquad (2)$$

where the constants a, b, $E_F(0)$ and γ are determined from the results of quantum calculation. In the absence of any impact ionization, the drain-source current I_{ds} can be written as [4] :

$$I_{ds} = \frac{G_0|V_T|^2}{\mathcal{E}_0 L_1} \cdot (\frac{s}{2}\sqrt{s^2-p^2} - \frac{p^2}{2} ln(\frac{s+\sqrt{s^2-p^2}}{p}) + \frac{\gamma}{|V_T|}[\sqrt{s^2-p^2} - p \cdot cos^{-1}(\frac{p}{s})]) \quad (3)$$

where $G_0 = (\epsilon Z v_s/d_{eff})$, $d_{eff} = d + \Delta d$ with d and Δd being the thickness of $InAlAs$ layer and effective channel thickness, respectively. Z is the width of the gate, L_1 is the length of unsaturated region of the channel. The above equation incorporates the effect of the quantum well through eqns. 1 and 2 via reduced potentials. Also implicit in eqn 3 is the use of a velocity-electric field characteristic of the form $v_d = \mu_0 \mathcal{E}/\sqrt{(v_s/\mu_0)^2 + \mathcal{E}^2}$ where v_d is the drift velocity, μ_0 is the low field mobility, v_s is the saturation velocity and $\mathcal{E}$ is the electric field. The evaluation of d.c. small signal parameters follows the treatment presented in Ref.[5].

The self-consistent noise model [6] is extended to calculate noise properties in AlGaAsSb/InGaAs HEMTs. By accounting for the noise sources and matching the optimized external source impedance to the transistor, the minimum noise figure F_{min} and minimum noise temperature T_{min} are calculated as [6] :

$$F_{min} = 1 + 2 \cdot g_n(R_c + \sqrt{R_c^2 + \frac{r_n}{g_n}}) \quad (4)$$

$$T_{min} = 2 \cdot T \cdot g_n \cdot (R_c + R_{s,opt}) \quad (K) \quad (5)$$

where

$$g_n = g_m \cdot (\frac{f}{f_T})^2 \cdot (R + P - 2C\sqrt{PR}) \quad (6)$$

$$R_c = R_s + R_g + R_i \quad (7)$$

where r_n is the noise resistance, R_c is the correlation resistance, R_s and R_g are the source and drain resistances and $R_i = \frac{L_g}{v_s C_{gs}}$, is the gate charging resistance. L_g represents the length of the gate and v_s is carrier saturation velocity in the conducting channel. P, R and C represent the noise coefficients and $R_{s,opt}$ is the optimal external source resistance. g_m and C_{gs} are the device transconductance and gate capacitance, respectively. T is the operating temperature in ^0K.

Results and Discussion

An $In_{0.53}Ga_{0.47}As/Al_{0.6}Ga_{0.4}AsSb$ double barrier HEMT with a QW width of 100Å is considered. The calculated band offset is 0.984eV. A low field mobility of 53,000 $cm^2/V-s$ and a saturation velocity of $3.2 \times 10^7 cm/s$ is used in the simulation [7]. The donor doping density of $2 \times 10^{18} cm^{-3}$ with a doped epilayer thickness of 350Å is used.

In Fig. 1, the Fermi level and X_{av} are plotted as a function of the 2DEG concentration. The plots are obtained by solving Schroedinger and Poisson's equations self-consistently. The functional forms obtained for E_F and X_{av} (eqns. 1 and 2) results in the calculation of the current-voltage characteristica as shown in Fig. 2 where the gate bias is varied from -1.0 V to 0V

at an interval of 0.5V. An impact ionization constant of $5 \times 10^5/cm$ is used in the computation. The I-V curves for hiher gate bias clearly shows the effcet of impact ionization.

Fig. 3, shows the calculated transconductance as a function of the gate bias. A maximum transconductance of 800 mS/mA, for a gate length of $1\mu m$, is obtained for the unoptimized structure. Fig. 4, shows the minimum noise figure as a function of frequency. The gate and drain biases are 1.5V and 2.0V, respectively. As observed, the minimum noise figure is less thatn 1dB at 60GHz. An optimization based upon (a) QW width (b) gate length and (c) doped epilayer thickness will enable the realization of lower F_{min} upto 100GHz. Moreover, the role of gate drain separation on noise due to impact ionization is under investigation.

Acknowledgement

The authors acknowledge support from the Air Force Office of Scientific Research (AFOSR) and the AFOSR Summer Faculty Research Program.

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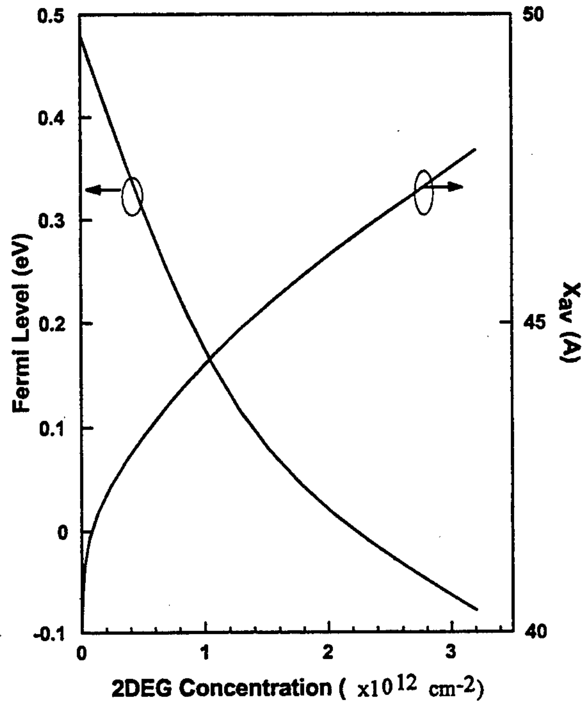

Fig.1 Fermi level and X_{av} as a function of 2DEG concentration at t=300K.

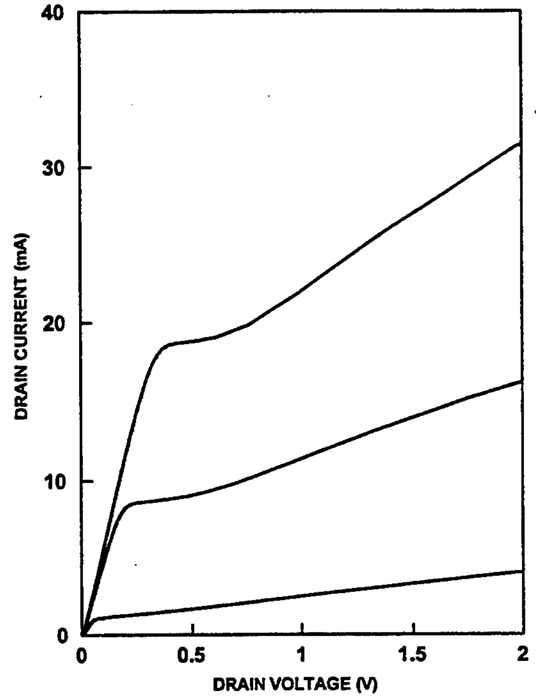

Fig.2 Theoretical I-V curves.

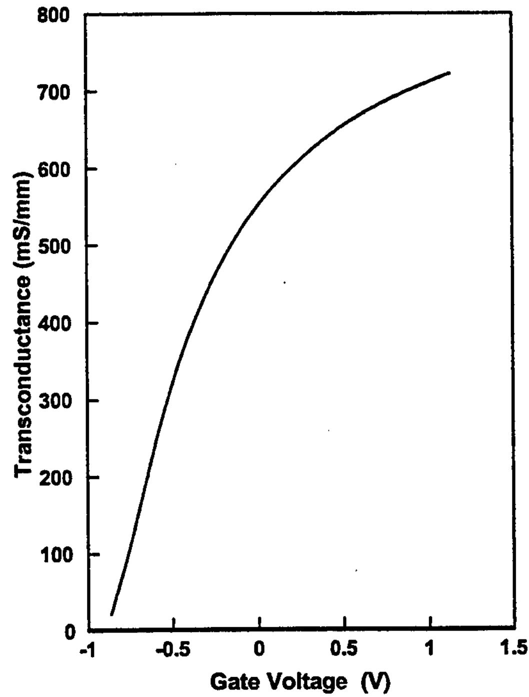

Fig. 3 Transconductance as a function of gate bias. V_D=2.0V.

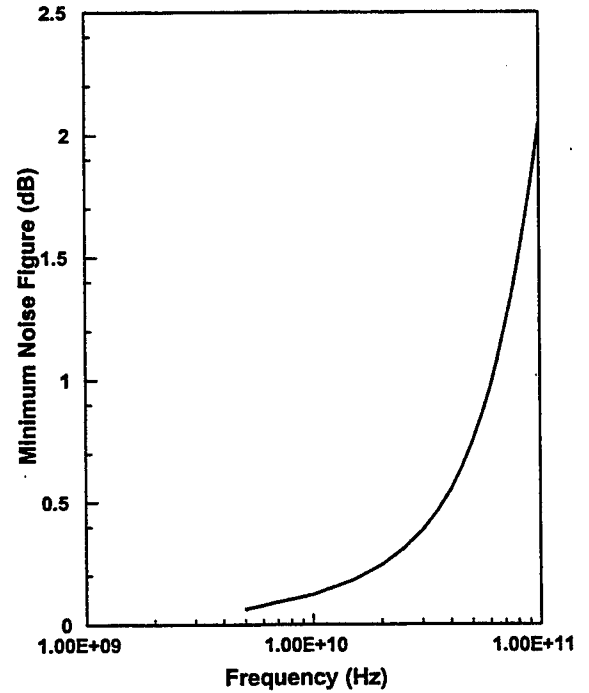

Fig. 4 Minimum noise figure as a function of frequency. V_D=2.0V.

Characterization of Ultra-Thinned MOSFETs

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The first characterization of a MOSFET in which the substrate has been thinned to less than 5μm is reported. A technique has been developed to eliminate kink effect by utilizing a thin chrome-gold contact on the backside of the substrate. In addition, a technique has been developed for transferring the thinned MOSFET substrates to a package that allows bonding in a conventional manner.

A primary application for an ultra-thinning technology is the improvement in the single event upset (SEU) immunity of commercial SRAMS and digital signal processors for space applications. An attractive approach for improving SEU immunity is to utilize ultra-thinning to reduce the charge generation volume for SEU events. Other potential applications for ultra-thinning include 3-dimensional stacked VLSI circuits [1], microwave transmission lines and passive components with low substrate loss, reduced crosstalk in photodetector arrays, improved thermal conductance, and improved mixed-signal isolation.

Initial characterization of ultra-thinned MOSFETs, which were mounted with an insulating epoxy, showed large kink effects. A technique was developed to eliminate the kink effect by utilizing a thin (5nm) chrome/gold contact on the back surface of the thinned substate that was then adhered to a second conductive substrate as shown in Fig. 1. The I-V characteristics of a MOSFET that has been thinned to $\approx$4μm with the substrate floating and the substrate grounded are shown in Fig. 2. The floating substrate case shows a large kink effect, while the kink effect is completely eliminated by grounding the backside contact. The subthreshold characteristics for a thinned MOSFET with a V_{DS} bias of 0.1V and 5V are shown in Figures 3 and 4, respectively. The large V_{DS} bias case shows subthreshold characteristics that are similar to that observed for floating body SOI devices. The subthreshold characteristics also show low junction leakage for the thinned devices. Figure 5 shows the I-V characteristics of the source and drain junctions to the backside chrome-gold contact. Evidently, there is a sufficient number of surface-state sites at the plasma damaged silicon-metal contract to provide a low barrier height.

The technique for precision thinning the MOSFETs involves attaching the substrate to be thinned to a support substrate with small total thickness variation (TTV) with a temporary adhesive. After thinning, chrome/gold is deposited on the backs of the thinned substrate and a second chrome/gold coated substrate is adhered on the back of the thinned substrate using conductive epoxy. The front side adhesive is next dissolved. The attached substrate provides sufficient support for the thinned substrate to allow the thinned substrate to be transferred to a package and bonded in a conventional manner.

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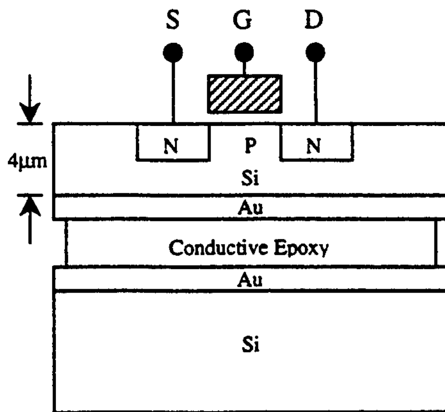

Figure 1. Schematic drawing of a thinned MOSFET attached to a to a second conductive substrate.

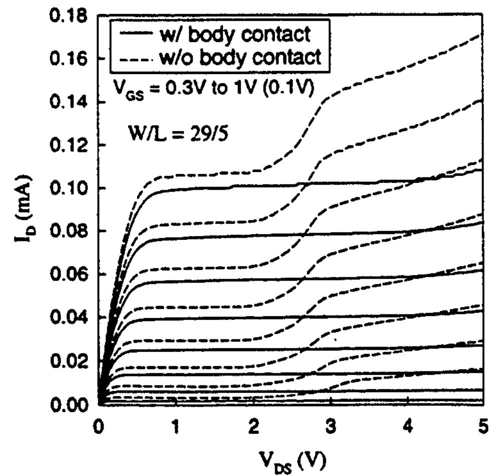

Figure 2. I-V characteristics of a MOSFET that has been thinned to 4μm with the substrate floating and the substrate grounded.

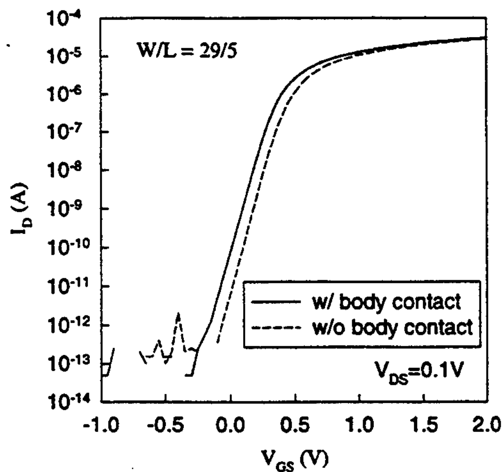

Figure 3. Subthreshold characteristics for a thinned MOSFET with a V_{DS} bias of 0.1V.

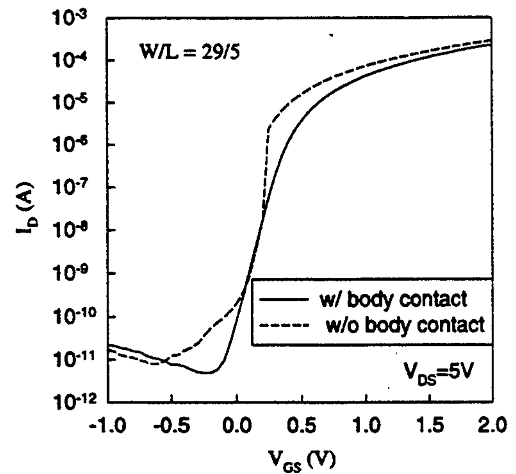

Figure 4. Subthreshold characteristics for a thinned MOSFET with a V_{DS} bias of 5V.

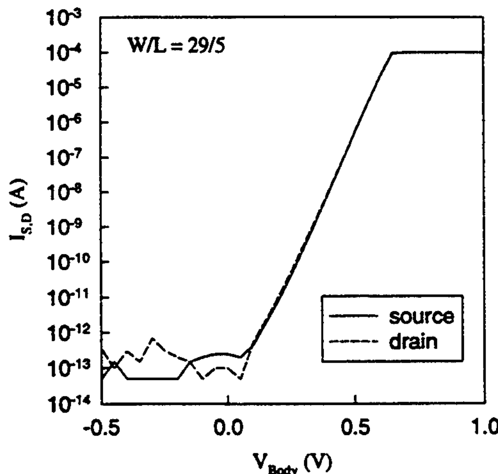

Figure 5. I-V characteristics of the source and drain junctions to the backside contact.

Lateral Channel Engineering in VLSI CMOS FET's

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1. Introduction

As the critical dimensions of CMOS transistor are scaled down into deep-submicronmeter regime and beyond, physical phenomena related to the short-channel effects (e.g., threshold voltage roll-off / up, drain-induced-barrier-lowering (DIBL), punch-through, and subthreshold swing boosting) become increasingly important. For low-voltage / low-power devices, the problems related to the short-channel effects become more complicated. The fundamental nature of the short-channel effects is the impact of drain coupling on the channel / body potential. The gate control over the channel carrier flow could be compromised as a result of the drain coupling.

Two device design approaches can effectively suppress the short-channel effects. One is lateral channel engineering (LCE), such as pocket (Fig.1a) or halo (Fig.1b) implant, to enhance the resistance of surface or subsurface potential barrier to the drain impact. Another is vertical well engineering (VWE), such as retrograded-doped well or delta-doped well (Fig.1c). Table I shows the comparison of performance merit between these two approaches. In this paper, a comprehensive study of the short-channel effects in VLSI CMOS transistors is reported. The major work includes the development of a unified physics-based model for short-channel effects and the study of the impact of lateral channel doping engineering on the MOSFET performance as well as the technology scaling of CMOS IC's.

2. Modeling Short-Channel Effects

2.1 Threshold Voltage Roll-Off / Up

The control of gate electrode and drain over the channel or body potential barrier is manifested in the threshold voltage model derived from the solution of Poisson's equation under the so-called pseudo-2D approximation [1]. Fig.2 shows a typical channel surface doping profile with LCE (e.g., pocket implant) as simulated by SUPREM-IV. The Poisson's equation in the active channel and body region is solved and the ΔV_{th} is found to follow a superposition rule (Fig.3):

$$\Delta V_{th} = -C_1 \cdot e^{-L_{eff}/l} + (k-1) C_2 \cdot e^{-L_{eff}/2l}$$

$$C_1 = 3(\psi_o - \phi_s) + V_{DS}$$

$$C_2 = 2\sqrt{(\psi_o - \phi_s)(\psi_o - \phi_s + V_{DS})}$$

where $l \cong 0.97 X_j^{1/3} T_{ox}^{1/3} X_{dep}^{1/3}$. The effect of vertical well doping engineering is reflected in the back-gate thickness X_{dep}. The scaling down of X_{dep} is highly desirable in order to suppress the short-channel effects [2]. The gate oxide effective thickness, $T_{ox(eff)}$, is determined by the C-V measured data to account for the possible gate-depletion effect and channel quantization effect. The lateral nonuniformity of channel doping due to either pocket / halo implant or the defect-enhanced-diffusion (e.g., TED or OED) is represented by the k-parameter which can be either calculated or extracted from the experiment data. In the case channel and source / drain doping concentrations are not known (e.g., in the case of TED or OED), C1, C2, and k can be extracted from the measured $\log(|\Delta V_{th}|) \sim L_{eff}$ data (Fig.4). The unified physics-based model well predicts the V_{th} roll-off / up characteristics of CMOS devices fabricated by a wide range of CMOS technologies (Fig.5,6,7).

2.2 DIBL and Punchthrough

Fig.8 shows the model-predicted and measured DIBL effect as impacted by the lateral channel doping profile engineering. In the pseudo-2D model the subsurface DIBL leakage is represented by the punchthrough voltage, V_{PT}, which is defined as $V_{PT} = V_{ds}|_{\Delta V_{th}(DIBL)=V_{dd}}$. The proper design of a VLSI CMOS device is to make $V_{PT} > V_{dd}$ in order to suppress the subsurface punchthrough leakage.

3. Impact on CMOS Scaling and Device Performance

3.1 Minimum Acceptable Channel Length

Fig.10 shows the impact of lateral channel doping engineering on the minimum acceptable channel length L_{min} (under two different types of definition) of n-channel MOSFET's of three CMOS technology generations. It is found that through doping profile engineering L_{min} can be pushed down to about 40% that of a device with uniformly-doped channel, which is roughly two technology generations' improvement. Fig.11 further illustrates the impact of LCE on the worst-case L_{min}.

3.2 MOSFET Current

The MOSFET driving current degradation has been reported in CMOS transistors with either LCE [3] or VWE [4]. In this study, the current drive is defined as $I_{dsat}@V_{gs}\text{-}V_{th}=1V$ for fair comparison. It is found that the current is degraded as a result of LATI (large-angle-tilt-implanted) pocket (Fig.12). Different from devices with VWE, in devices with LCE the I_{dsat} degradation shows a more stronger L_{eff}-dependency at short channel region (Fig.13). This phenomenon can be modeled by the so-called bulk-charge-effect in which the depletion charge near the drain region results in a raised local threshold voltage therefore a degraded current:

$$I_{dsat} = \frac{WC_{ox}\mu(V_{gs}-V_{th})^2}{V_{gs}-V_{th}+\alpha_{eff}\cdot E_{sat}L_{eff}}$$

where α_{eff} is the bulk-charge-effect coefficient. In MOS devices with uniformly-doped (UC) channel or VWE, α_{eff} remains independent of L_{eff}. However, in devices with LCE, α_{eff} is a function of L_{eff} and is boosted at very short channel due to an enhanced $N_{body(eff)}$ (hence the bulk-charge-effect). Therefore the MOSFET current degradation becomes more significant in very short L_{eff}. It should be noted that in practical CMOS technology development, the current drive is more reasonably compared at $L_{norm}\text{-}L_{min}$, in which case the current degradation might be less severe since LCE improves the short-channel immunity by reducing the L_{min}.

3.3 $I_{off}\sim I_{dsat}$ Characteristics

In devices with LCE, the $I_{doff}\sim I_{dsat}$ characteristics is improved as a result of suppressed short-channel effects (Fig.14). However, whether there is overall performance merit by applying LCE for a given CMOS technology generation largely depends on the off-state leakage current tolerance determined by a specific application.

3.4 Hot-Carrier Injection

The hot-carrier injection, reflected by the ratio of I_{sub}/I_d, increases as the LATI-pocket implant energy increases (Fig.15). In the studied devices, pocket implant changes the channel surface doping profile in the LDD region (Fig.2), resulting in a larger peak electric field near the drain junction. Design optimization is therefore demanded to achieve good device performance as well as hot-carrier reliability.

3.5 Drain-Source Breakdown Voltage

Fig.16 shows the dependency of the drain-source breakdown voltage BV_{ds} on the LATI-pocket implant energy. In the studied device, the maximum BV_{ds} is achieved at an optimum pocket implant energy of 40KeV due to the doping profile modification near the drain junction region.

4. Summary

We present a comprehensive study on the impact of lateral channel engineering on VLSI CMOS transistor performance and technology scaling. The short-channel effects are suppressed and L_{min} can be pushed down by two generations ahead through lateral channel doping profile engineering such as pocket implant. Degradation of MOSFET current drive, modeled by the L_{eff}-dependent bulk-charge-effect, becomes more significant at very short L_{eff}. The overall transistor design optimization demands to take into consideration of device current drive, off-state leakage current, punchthrough, hot-carrier reliability, drain-source breakdown voltage, etc.

Acknowledgment

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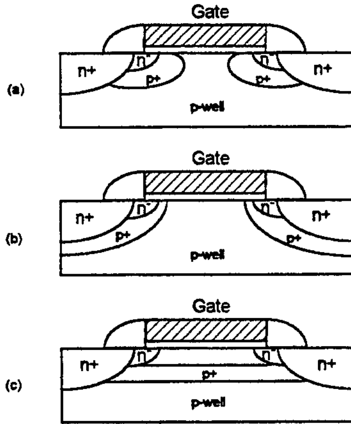

Fig.1 N-channel MOSFET with (a) pocket implant (b) halo implant and (c) well doping engineering.

Approach	LCE	VWE
Example	pocket halo	SSR δ-doping
C_{jsh}, C_{jdh}	+/-	+
C_{gh}	+	-
I_{dsat}	-	-
SCE tailoring	+	-
swing boost	+	-

+: favorable -: unfavorable/degraded

Table-I Comparison of merit between lateral channel engineering and vertical well engineering.

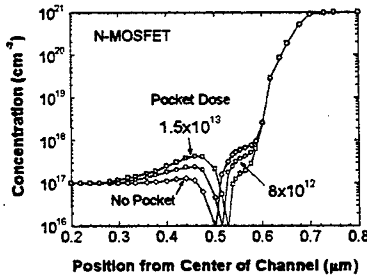

Fig.2 Simulated channel surface doping in MOSFET with lateral channel engineering (pocket implant).

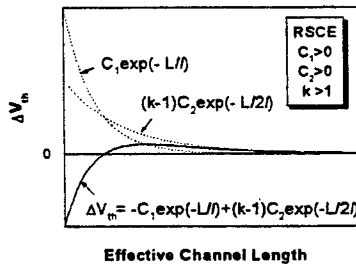

Fig.3 Superposition of ΔV_{th}: k>1 is the prerequisite for the reverse-short-channel-effect (RSCE) to occur.

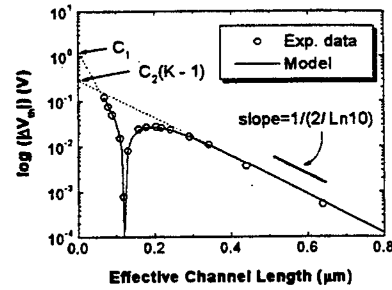

Fig.4 Extraction of the parameters C1, C2, and k from the measured $\log(|\Delta V_{th}|) \sim L_{eff}$ plot.

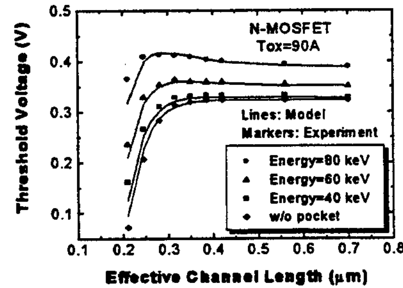

Fig.5 V_{th} roll-off / up characteristics for MOS devices with different pocket implant condition.

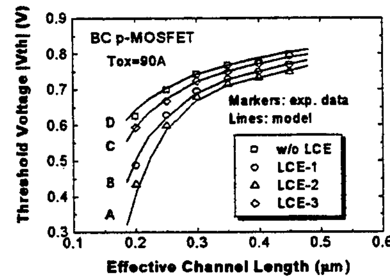

Fig.6 V_{th} roll-off characteristics for a buried-channel p+ gate p-MOSFET with pocket implant.

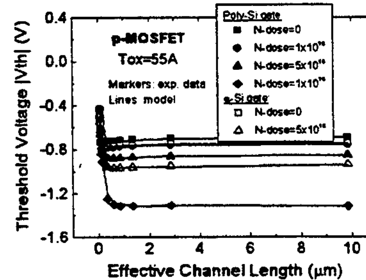

Fig.7 V_{th} roll-off / up in p-MOSFET with gate nitrogen implant. The RSCE is a result of DED effect.

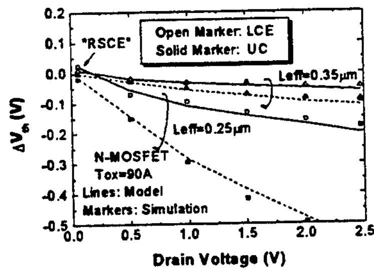

Fig.9 Impact of pocket implant on the drain-induced-barrier-lowering (DIBL) effect.

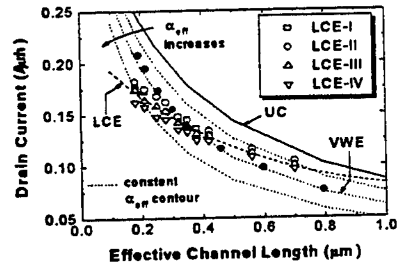

Fig.13 For MOSFET's with LCE and VWE, I_{dsat} is degraded due to bulk-charge effect.

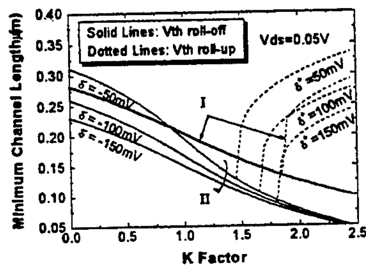

Fig.10 LCE improves the short-channel performance by pushing down L_{min} two generations ahead.

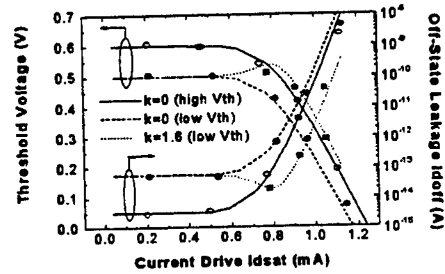

Fig.14 I_{doff}~I_{dsat} characteristics as improved by pocket implant. Lines: model. Points: 2D simulation.

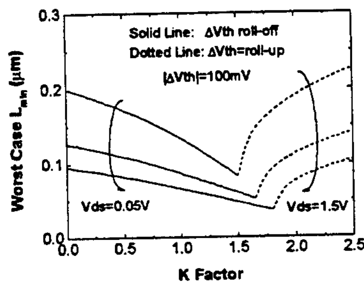

Fig.11 The worst-case L_{min} as improved by LCE in different CMOS technologies.

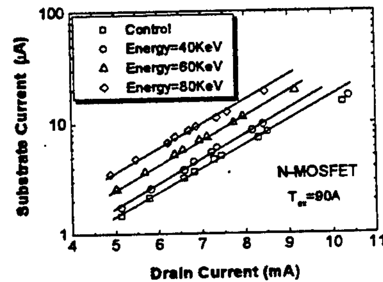

Fig.15 Increase of hot-carrier induced substrate current due to LATI-pocket implant.

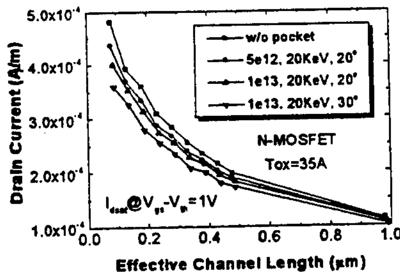

Fig.12 Degradation of device current drive (defined by $I_{dsat}@V_{gs}$-V_{th}=1V) as a result of pocket implant.

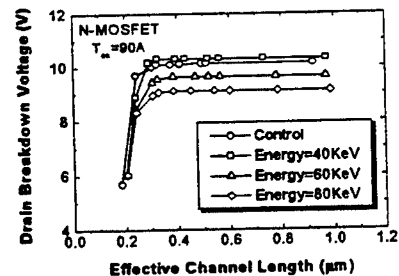

Fig.16 Drain-source breakdown voltage as influenced by LATI- pocket implant.

Breaking the 1V Barrier: Dynamic Threshold Logic for a Wide Range of Supply Voltages Down to 0.3V

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ABSTRACT

We have investigated circuit options to surpass the 1V power supply limitation predicted by traditional scaling guidelines. By modulating the body bias, we can dynamically adjust the threshold voltage to have different on- and off-state values. Several DTMOS logic styles were analyzed for ultra low power. The channel doping profile was optimized for DTMOS operation. Results indicate that DTMOS circuits can work with a power supply down to 0.1V and that high speed can be achieved with a supply down to 0.3V.

INTRODUCTION

The SIA roadmap identifies two paths for voltage scaling—one for low power and one for high performance [1]. As seen in Table 1, both branches show a fairly aggressive scaling of the supply voltage—especially considering how many generations the supply remained at 5V or 3.3V. Nonetheless, even for the low power branch, the supply voltage seems to bottom out at 0.9V. To understand the reason behind this predicted lower bound, it is essential to investigate the tradeoffs and limitations associated with lowering the supply voltage.

Because current drive is dependent on V_{dd}-V_t, simply reducing the supply voltage results in an excessive increase in delay. One model of the scaling dependencies for inverter delay derived in [2] is

$$\tau \propto \frac{CL^{0.5}T_{ox}^{0.5}}{V_{dd}^{0.3}(0.9-V_t/V_{dd})^{1.3}}\left(\frac{1}{W_n}+\frac{2.2}{W_p}\right)$$

This equation shows that if we keep V_t/V_{dd} constant, $\tau \propto T_{ox}^{0.5}/V_{dd}^{0.3}$, i.e. the delay increases only slowly with decreasing V_{dd}. Thus, keeping V_t/V_{dd} nearly constant is crucial for scaling the supply voltages without suffering performance degradation. Acceptable values of V_t/V_{dd} are typically between 1/4 and 1/5 [3-6]. Unfortunately, because of noise and leakage concerns, there is a lower bound on V_t, which places a lower bound on V_{dd}. This reasoning is summarized in Fig. 1.

The above discussion was based on a critical assumption—that we have the same threshold voltage in both the on- and off-state. If we could have a low threshold for the on-state and a high threshold for the off-state, we could raise the acceptable V_{toff}/V_{dd} ratio allowing us to reduce the supply lower than 1V. By manipulating the body potential, we can do exactly that. By coupling the gate to the body, we obtain low leakage (V_g=V_b=0 → V_t high) and high drive (V_g=V_b=V_{dd} → V_t low) for extremely low supply voltages. This configuration is known as DTMOS (Dynamic Threshold MOS) [7]. I-V curves illustrating the improvement are shown in Fig. 2. Because DTMOS takes advantage of the body effect via a forward bias of the body-source junction, a maximum of 0.5V should be applied to the body. Various circuit techniques for avoiding this limitation will be discussed and results will indicate that using supply voltages in the range of 0.3-1.5V is feasible in today's technology.

INVERTER COMPARISON

The inverter comparisons were made using SPICE models extracted from real transistors fabricated with a 0.18μm process with a 0.3V threshold. Each simulated transistor was split into 10 transistors with 1/10 of the desired width to provide accuracy for the RC delay associated with charging the body. Three design options (Fig. 3) are compared with the traditional CMOS inverter. The first variation is the DTMOS inverter introduced in [7]. The second inverter is similar to the first but with a *limiter* transistor to limit each body-source

junction to 0.5V forward bias. The limiter transistors are minimum sized devices. The reference voltages are kept at $0.5 + V_t$ for NMOS and Vdd- $(0.5 + |V_t|)$ for PMOS for the most efficient operation. These reference voltages can either be provided separately or the threshold voltages of the limiter devices can be adjusted such that V_{dd} and GND can be used. The third inverter also uses minimum sized auxiliary devices to *augment* the current drive by manipulating the body bias [8]. This time, however, the body-source junction isn't directly clamped. Rather, any excess current caused by forward biasing is used to charge/discharge the output.

Plots for delay and power*delay for various supply voltages are shown in Figures 4 and 5, respectively. For supply voltages below 0.5V, the clear choice is the straight DTMOS inverter. For supply voltages between 0.5V and 1.5V, both the Limiter and Augmented cases show significant improvement over the traditional CMOS inverter. Since each of the DTMOS variations adds capacitance, the advantages of these variations are more apparent with heavier output loading. Fig. 6 illustrates this point.

DTMOS MOBILITY

Simply lowering the threshold is not the only advantage of tying the gate to the body. Raising the body potential reduces the band bending in the body and leads to lower electric fields. A simulation of the electric field is shown in Fig. 7. The reduced electric field provides DTMOS devices with greater mobility than for standard devices for a given gate voltage. Experimental data verifying this is shown in Fig. 8.

BODY EFFECT

Since the SPICE models used in the inverter comparison were derived from a typical process, they weren't optimized to exploit the DTMOS effect. Figure 4 shows that the delay in the DTMOS inverter starts to increase substantially for supply voltages below 0.4V. A large body effect leads to a large threshold voltage swing and thus allows lower supply voltages since Vt_{on}/Vdd is still small. To exploit the DTMOS effect, we used a mixed-mode device simulator to analyze optimal doping profiles and the extent to which we could enhance the body effect for even lower supply voltages. The doping profile is shown in Fig. 9. T_{CD} is the counter doping junction depth and is varied to achieve the desired off-state leakage current. We targeted 30nA/μm and 10nA/μm for the NMOS and PMOS off-state leakage currents, respectively. With substrate doping of $1e19cm^3$ and extreme counter doping, we were able to achieve a body effect of 0.4 $(\Delta V_t/V_{dd})$—a larger effect could be achieved with thicker oxide or shallower counter doping at the expense of drive current [9]. With this ideal device, we obtained the single-stage delay of an oscillator with various supply voltages as shown in Fig. 10. Our single-stage delays of 109ps @ 0.4V and 85ps @ 0.5V compare well to the values 200ps @ 0.4V and 103.3ps @ 0.5V reported in [10]. This figure shows that a DTMOS device could be used with a supply voltage as low as 0.3V without suffering from severe speed degradation. Furthermore, Vdd can actually be less than Vt_{off} and the circuit will still work--inverter DC characteristics are shown in Fig. 11. The DTMOS (bodies tied to gate) ideal device has gain significantly larger than unity down to 0.1V whereas the CMOS (bodies tied to rails) ideal device only works down to 0.2V. At 0.3V, the CMOS peak gain is greater because the CMOS device is still operating in the subthreshold regime which allows for larger gain.

CONCLUSION

DTMOS circuits are superior to standard circuits at low voltages and operation at very low voltages is possible. The inverter SPICE simulations were based on real devices that were not optimized for the body effect and yet those simulations demonstrate that DTMOS circuits are advantageous and allow for speedy circuits with a supply voltage down to 0.4V. Furthermore, we analyzed DTMOS circuits that allow for use with supply voltages above 0.6V. Thus, DTMOS circuits may be useful at today's power supply voltage in addition to future ultra-low-voltage circuits.

ACKNOWLEDGEMENTS

The authors wish to thank Kazunari Ishimaru for his consultation. This work is funded by ONR contract N00014-96-1-0369 and NSF contract ECS-9634217.

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Year of First DRAM Shipment / Minimum Feature Size (μm)	1995 / 0.35	1998 / 0.25	2001 / 0.18	2004 / 0.13	2007 / 0.10	2010 / 0.07
Power Supply Voltage (V)						
Desktop	3.3	2.5	1.8	1.5	1.2	0.9
Battery	2.5	1.8-2.5	0.9-1.8	0.9	0.9	0.9
Maximum Power						
High-performance with heatsink (W)	80	100	120	140	160	180
Logic without heatsink (W/cm2)	5	7	10	10	10	10
Battery (W)	2.5	2.5	3.0	3.5	4.0	4.5

Table 1. Voltage supply scaling for both high-performance and low-power application branches. Predictions based on standard CMOS circuits suggest that we cannot scale below 0.9V. DTMOS allows us to scale much further. (after [1])

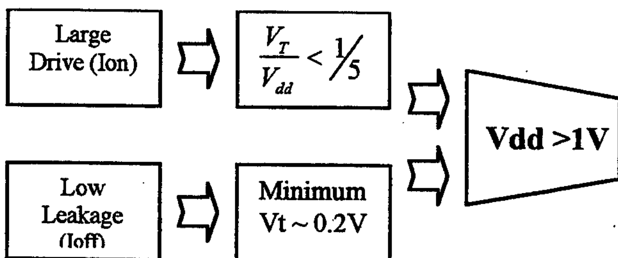

Figure 1. Diagram showing the difficulty in scaling below 1V.

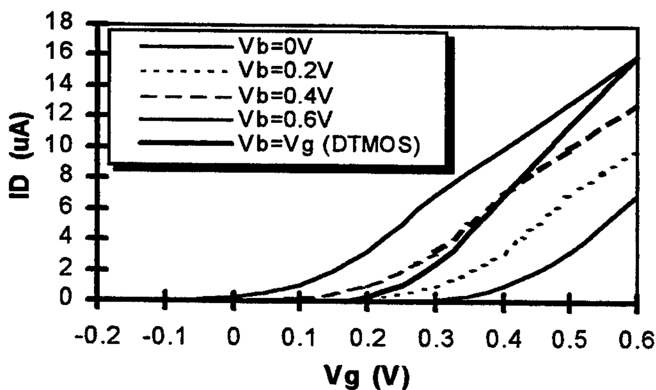

Figure 2. Standard I_d-V_g curves for a MOSFET. The heavy line shows the current-drive advantage of a Dynamic Threshold MOSFET (DTMOS).

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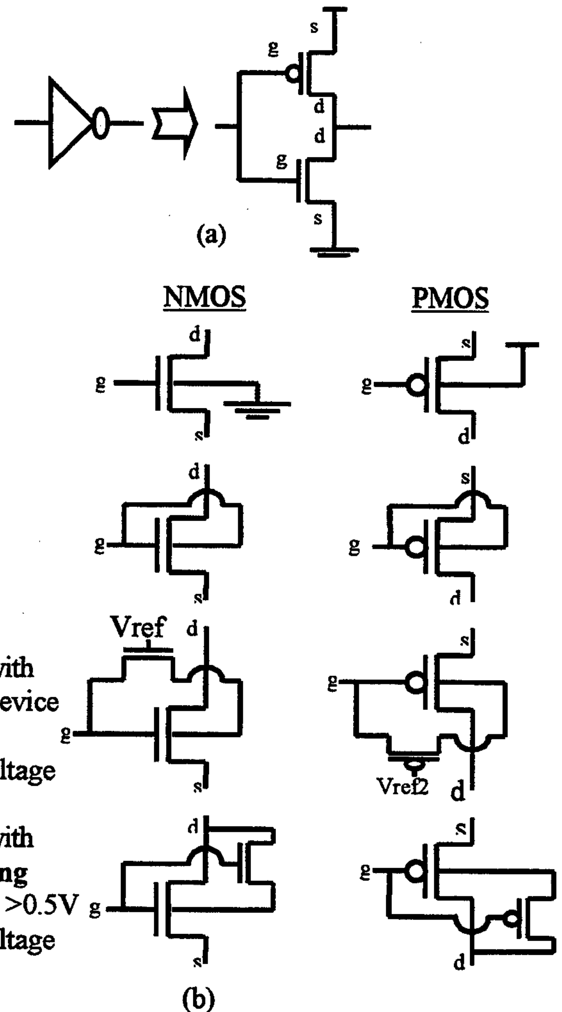

Figure 3. (a) Standard CMOS inverter design. (b) Four designs showing different body connections. For a given logic style, the NMOS and PMOS arrangements can directly replace the equivalent devices shown in the inverter in (a) to provide improved delay at low voltages.

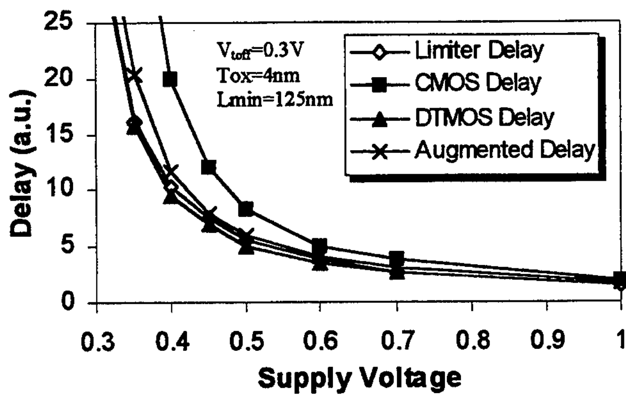

Figure 4. Delay comparison for the four inverters depicted in Fig 3. The DTMOS designs all have noticeable advantage when $V_{dd} < 1V$ ($V_t/V_{dd} > 1/5$).

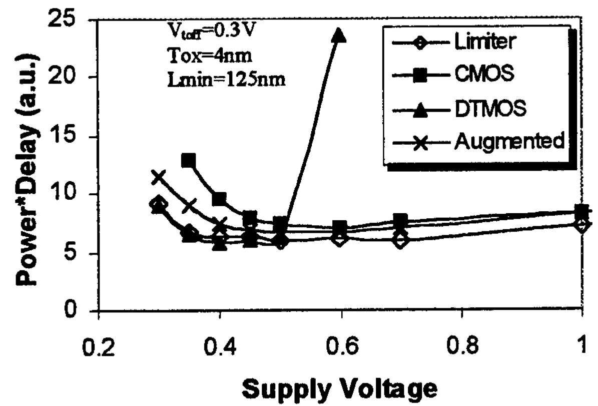

Figure 5. Power*delay comparison for the four inverters depicted in Fig. 3. Straight DTMOS is superior for <0.5V, but the two DTMOS alternatives with auxiliary devices extend the improvement up to 1.5V.

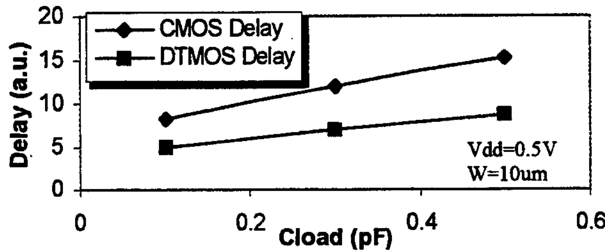

Figure 6. The DTMOS variations are even more advantageous with larger loading. Note, however, that all other delay simulations were run with 0.1pF output loading.

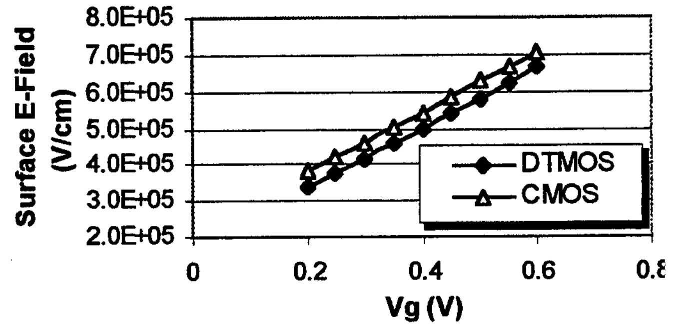

Figure 7. Surface electric field in the channel. The body bias in DTMOS reduces the field and provides a larger mobility.

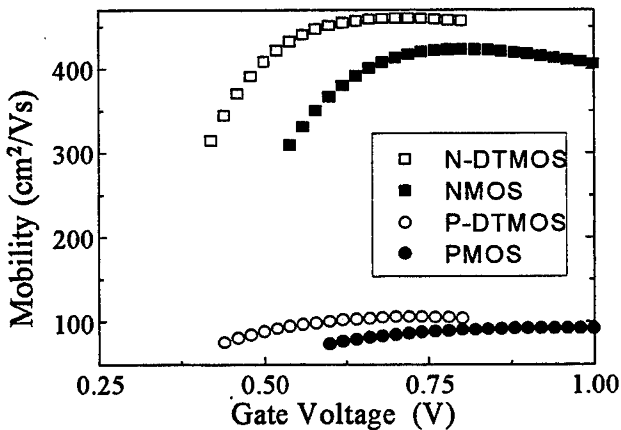

Figure 8. Experimental data showing that mobility in DTMOS is higher because of the reduced electric field. Tox=6.4nm; Vt_n=0.48V; Vt_p=-0.46V

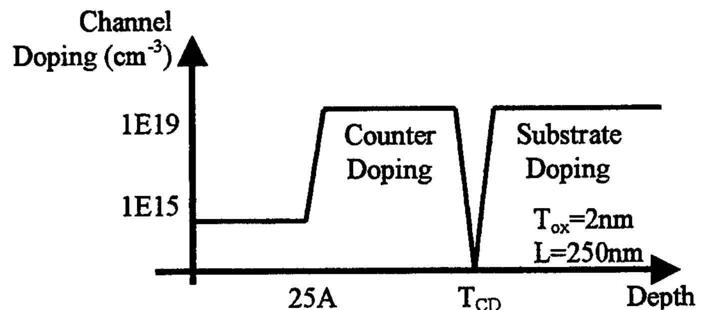

Figure 9. 'Ideal' device channel doping profile. Doping is low at the surface to keep the mobility high. Substrate doping is high for improved body effect. Counter doping is high to reduce V_t.

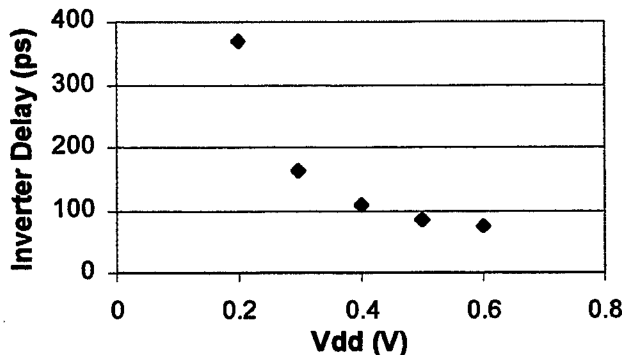

Figure 10. Single stage delay of an oscillator for the ideal DTMOS device. Excessive delay is avoided down to 0.3V.

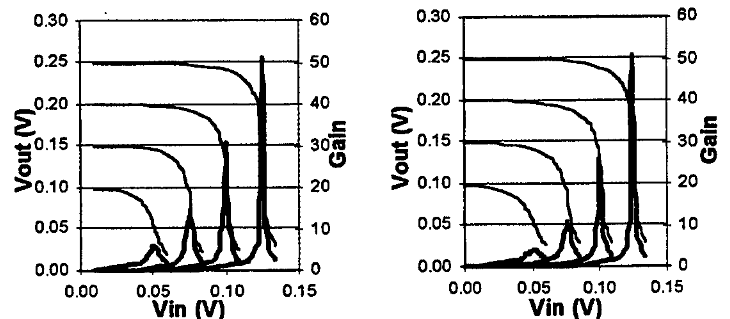

Figure 11. DTMOS inverter gain is shown on the left and the CM[illegible] inverter gain is shown on the right for four different supply voltag[illegible] The ideal DTMOS device provides greater inverter gain at l[illegible] voltages. The CMOS inverter has trouble inverting at 0.1V.

A Dynamic Characteristics of Buried Channel Poly-Si TFTs

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1. Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) at low temperature have attracted much attention in various large area electronic applications such as flat panel displays, page width optical scanners and page width printer heads. In conventional poly-Si TFT, the drain has to be offsetted from the channel region in order to achieve low leakage current. However, this causes severe current pinching problem, resulting in high on-resistance. Recently, a field plated high voltage TFT was proposed to solve the problem. It offers higher current driving capability without increase the leakage current[1]. However, this approach results in a complicated device structure and biasing scheme. In addition, the driving current level and switching speed are more important performance in case of poly-Si TFT LCD panel application. It is well known that the buried channel MOSFETs has higher mobility that that of surface channel devices[2]. The purpose of our work is employing the buried channel for increase the ON-current and obtaining the higher operating frequency.

2. Device Structure and Fabrication

In this paper, we propose a fabrication method for CMOS TFTs with buried channel(BC TFT). The proposed device has been fabricated by implantation doping of poly-Si active buried channel layer and we have designed four terminal electrodes TFTs rather three terminal conventional TFTs. Compared with the conventional poly-Si TFTs, the device has two unique things. The one is the buried channel of active layer for conductivity modulation and the other is the fourth terminal entitled back bias for preventing kink effect and malfunctioned driver for TFT LCD with driving circuit integration.

The schematic diagram of proposed buried channel TFT is shown in Fig. 1. The process sequences to form the buried channel is as follows in case of n-type poly-Si active buried channel layer doped by implantation. We employed 5000 Å wet oxidized silicon wafer for emulating quartz substrate. The 500 Å thick a-Si film was deposited by LPCVD system. BF_2^+ ions ($1\times10^{12}cm^{-2}$, 30KeV) are implanted in order to form p-type back channel conductivity modulation layer. The 500 Å thick a-Si film was deposited and the 1000 Å thick implantation sacrificial TEOS layer deposited and As^+ ions ($1\times10^{14}cm^{-2}$, 70KeV) are implanted into the buried channel forming region. The excimer laser recrystallization was performed. At this time, BF_2^+ ions diffused from lower implanted a-Si layer and As^+ ions was activated by laser energy so that doping profile for buried channel was obtained.

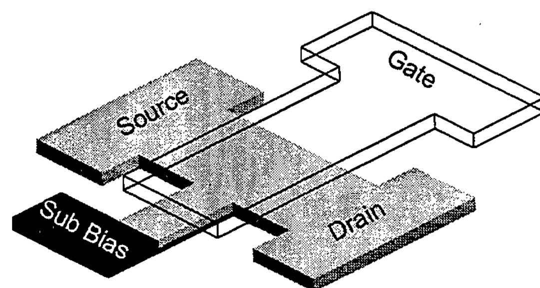

Fig. 1 The schematic diagram of proposed Buried channel TFT.

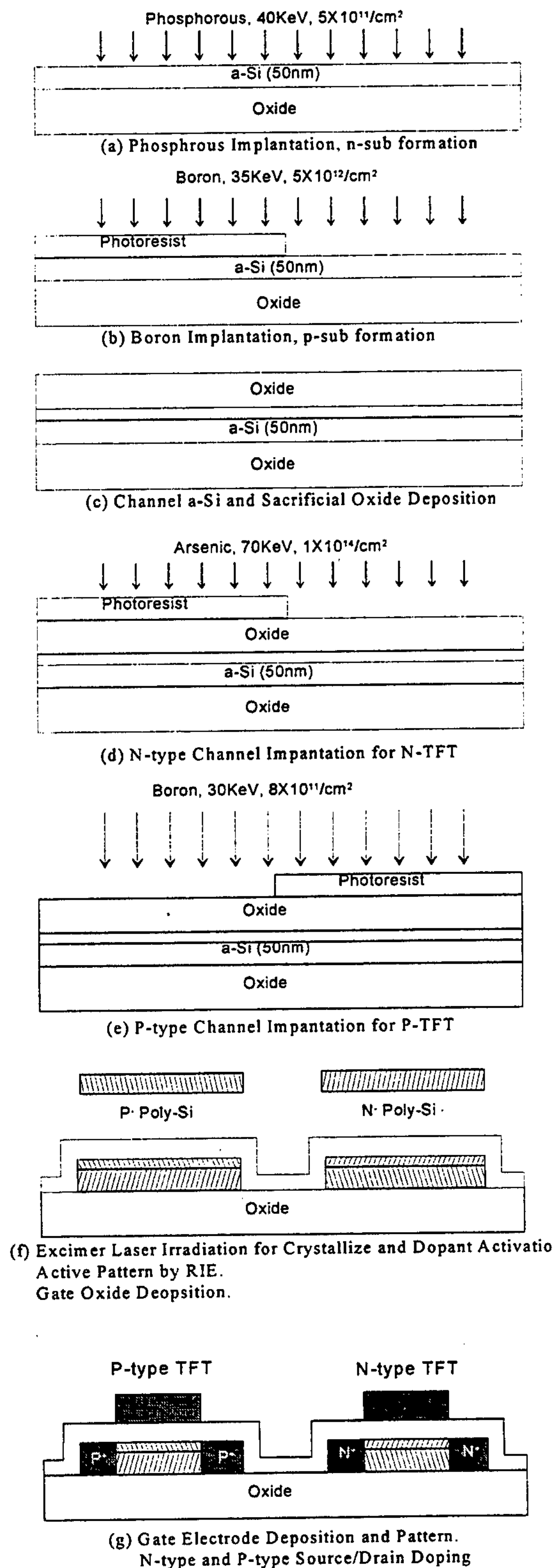

Fig. 2 Fabrication step of proposed BC TFT.

3. Experimental Results

Fig. 3 shows a SIMS profile of active layer doping concentration fabricated by proposed method. Fig. 2 shows the I_D-V_G characteristics of the new and conventional poly-Si TFTs, of which the channel length and width are 2μm and 10μm. The proposed device exhibits superior performance to conventional poly-Si TFTs in on-current(field effect mobility) and leakage current.

We fabricated the 23-stage CMOS inverter chain (ring oscillator) in order to make a comparison of dynamic characteristic between conventional poly-Si TFT circuit and proposed buried channel poly-Si TFT circuit. The size of nMOS and pMOS TFTs of CMOS ring oscillator have been optimized to W/L=10μm/6μm and 20μm/6 μm respectively. The output frequency of the ring oscillator was measured by Tektronix 2430A digital oscilloscope, and plotted as a function of operation voltage(V_{DD}) as shown in Fig. 5. The operating speed of ring oscillators with buried channel is much higher than that of ELA active film. This result is caused by effects of device ON-current, and mobility.

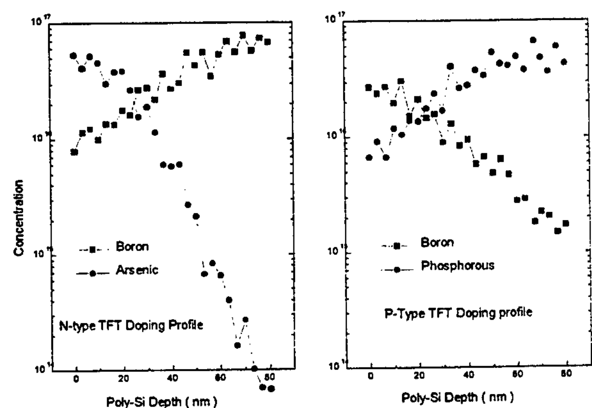

Fig. 3 SIMS profile of fabricated BC TFT active channel

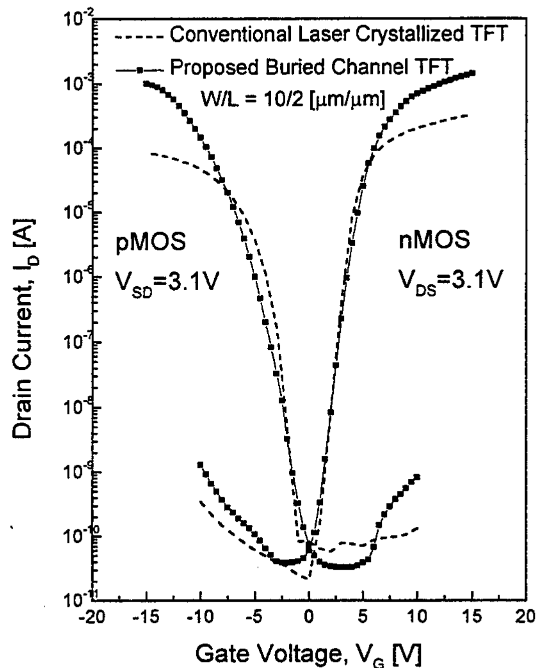

Fig. 4 Transfer characteristics of conventional and novel buried channel TFT.

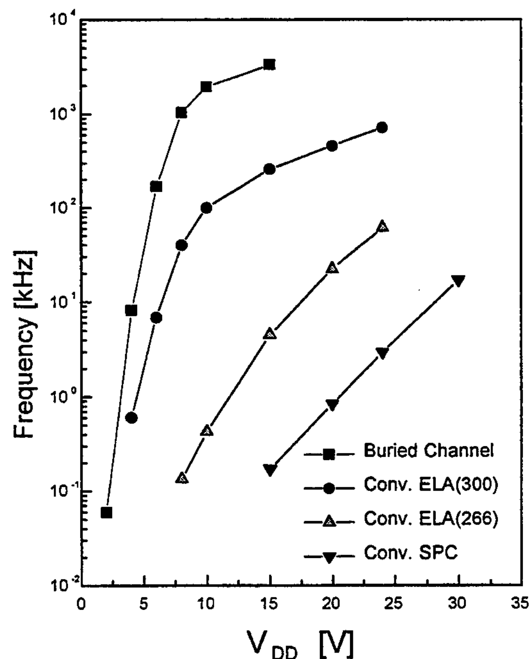

Fig. 5 The operation frequency of 23-stage CMOS ring oscillators as a function of V_{DD}.

4. Conclusion

We have successfully investigated the characteristics of buried channel poly-Si TFT devices and circuits fabricated. It should be noted that the ion shower process may be applicable to fabricate the BC poly-Si TFT, although the impurity doping for forming buried channel was performed by ion implantation. In order to investigate the dynamic characteristics of the poly-Si TFTs processed with various methods, we have fabricated and measured the operation frequency of 23-stage CMOS ring oscillators. The ring oscillators with BC poly-Si TFT operate at much higher speed (at lower V_{DD}) than that of conventional poly-Si TFT, due to effects of device ON-current and mobility.

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Characterization of AlGaAs/InGaAs/GaAs Based Double Heterojunction PHEMT for Linear Power Assessment

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ABSTRACT:- **We report on design and characterization of Pseudomorphic High Electron Mobility Transistors for linear power applications. Compared to conventional single heterojunction, double heterojunction PHEMT shows a flat transconductance of >200 mS/mm over a wide gate bias swing. A high breakdown voltage of 15V was measured. A flat cut-off frequency (f_T) of >15 GHz over a wide gate and drain bias region was achieved. A maximum oscillation frequency (f_{max}) of >75 GHz was obtained.**

I. INTRODUCTION

The growth of personal wireless communication systems has prompted the research interest recently to realize High Electron Mobility Transistors (HEMTs) at microwave frequencies [1-6]. For such applications, non-linearities in the power amplifier design introduce spectral regrowth resulting in adjacent channel interference and reduced spectral efficiency. As a result of this, the magnitude of third and fifth-order inter-modulations which are originated from 2nd and 3rd-order harmonics of fundamental output power increases [1]. The magnitude of these harmonics dependent upon the dc characteristics namely the transconductance (g_{mo}) uniformity with gate bias. A proper layer design structure which provides a uniform transconductance with gate bias is therefore critical to achieve low inter-modulations. Previously, much attention has been focused to increase peak transconductance (g_{mo}), maximum cut-off frequency (f_T), maximum frequency of oscillation (f_{max}) and output power of PHEMTs.

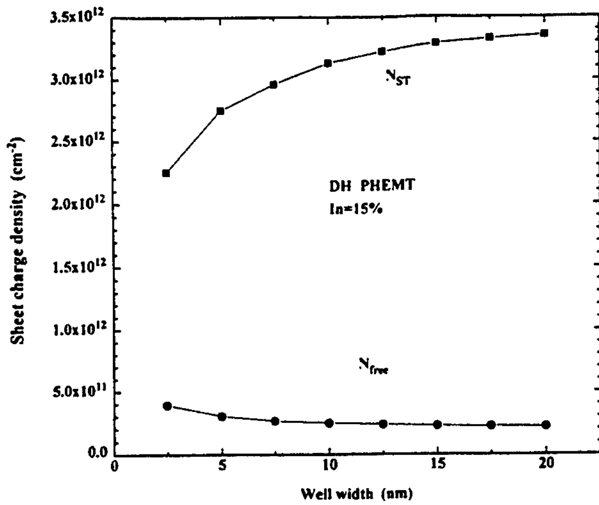
Here, we present design and performance of double heterojunction (DH) Pseudomorphic High Electron mobility Transistor (PHEMT) to achieve flat transconductance and flat cut-off frequency over a wide gate bias swing for linear power applications for wireless communication systems. To achieve this objective, the physical layer parameters (i.e. thicknesses, aluminum and indium contents, doping concentration and delta doping positions etc.) were optimized using numerical calculations and HELENA software [7].

II. DESIGN AND CHARACTERIZATION

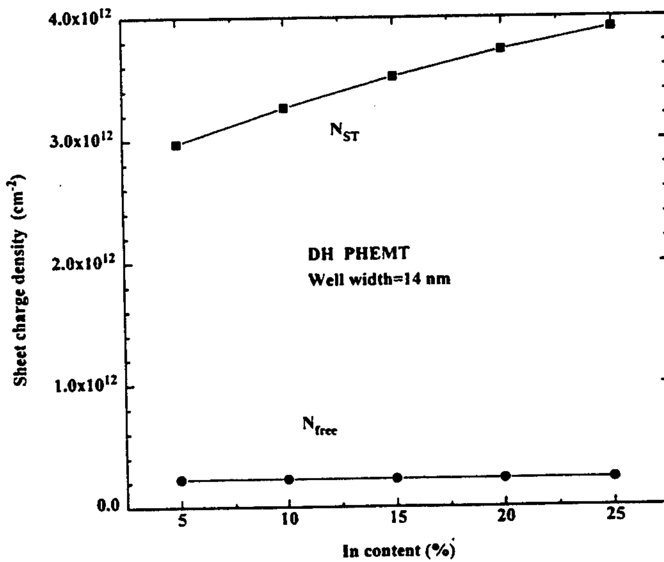
The layer structure was designed using numerical simulations based on a self-consistent calculations of Poisson's and Schrodinger's equations. Figure 1 shows the dependence of maximum sheet charge density (in InGaAs channel layer) on channel width and indium contents. Increasing the channel width increases the maximum channel charge density (N_{ST}) with reducing free electrons in the top AlGaAs layers. The channel electron density almost saturates for well width greater than *12.5 nm*. A large indium contents with thick channels are desirable to increase the channel charge density and low field channel mobility. However, a lattice mismatch strain between InGaAs and GaAs/AlGaAs layers precludes the use of high indium contents in the InGaAs layer. Thus the choice of indium contents and channel width in our study is limited to 20% and *14 nm* respectively.

The proposed device layer structure starting from the GaAs substrate is: 500 *nm* GaAs buffer layer, 100.85 *nm* AlGaAs buffer layer, bottom delta doping electron supply layer (1.7 x 10^{12} cm^{-2}), 3.35 *nm* AlGaAs bottom spacer layer, 14 *nm* InGaAs channel layer (20% indium content), 3.35 *nm* top AlGaAs spacer layer, top delta doping electron supply layer (3.4 x 10^{12} cm^{-2}), 30.85 *nm* undoped AlGaAs layer, and finally 45 *nm* n-doped GaAs cap layer (5x 10^{18} cm^{-3}) to achieve low ohmic contact. Undoped AlGaAs layer beneath the gate surface was used to achieve high breakdown voltage of the device. The above layer structure was grown in our solid source molecular beam epitaxy (MBE) system. For comparison, conventional PHEMT based on a single heterojunction (SH) was also grown and processed under same conditions.

The Hall measurements were performed after removing of top GaAs cap layer at 300 and 77K. A low field channel mobility of 4220 and 6230 $cm^2/V.S$ was measured at 300 and 77K respectively. A channel charge density of 3.22 x 10^{12} and 2.74 x 10^{12} cm^{-2} was obtained at 300 and 77K respectively, in good agreement with our numerical calculations (i.e. 3.6 x 10^{12} cm^{-2} at



(a)



(b)

Fig. 1. The dependence of maximum channel charge density as a function of (a) well width (b) indium contents

300K). Device fabrication of grown layer structure was realized by conventional optical lithography techniques. The active mesa regions were defined by using H_2SO_4:H_2O_2:H_2O etching solution. Ohmic contacts of Ni/Ge/Au/Ni/Au system were deposited by e-beam evaporation and patterned by conventional lift-off processing. A low contact resistance of 0.14 Ω-mm was obtained using four probe TLM measurements. After gate lithography and gate recessing (using Citric acid:H_2O_2:H_2O etching solution) to remove top GaAs cap layer, Ti/Au metals were evaporated to form Schottky gate contact.

DC characteristics of device were tested using HP 4145B semiconductor parameter analyzer. Figure 2 shows *I-V* characteristics of 1.25 x 45 μm^2 DH-PHEMT device. The device shows complete pinch-off with a threshold voltage of -1.72V in agreement with numerical calculations (-1.7V) and HELENA simulations (-1.74). The output channel conductance (g_{ds}) in saturation region of 4 mS/mm was obtained. A high breakdown voltage, defined at a gate leakage current of 1mA/mm was 15V (Fig. 3) which is comparable with double recessed PHEMT technology [6]. A drain source current of 450 mA/mm and a transconductance of 206 mS/mm (Fig. 4) was measured for 1.25 x 45 μm^2 device comparable with other devices of same gate length. Compared with single heterojunction (SH), DH-PHEMT device shows a quasi flat transconductance over a wide gate bias swing of >1.5V which gives a good indication for high linearity of device. However, the peak transconductance of SH-PHEMT was higher than that of DH-PHEMT because of higher mobility (i.e. 5500 $cm^2/V.S$) of this device.

The RF measurements were performed using on wafer microwave probing station (HP8510) from 1 to 40 GHz at different gate and drain biases. A cut-off frequency (f_T) of 15 GHz (Fig. 5) was measured which is comparable with other devices of same gate length [2-6]. The measured f_T values shows good qualitative and quantitative agreement with HELENA simulation. More interestingly is that f_T remains flat over a wide gate and drain bias region as required for linear power of device. A maximum frequency (f_{max}) of 60-80 GHz (Fig. 5b) was obtained which is higher than other devices using similar [4] and different approaches such as doped channel HFET [2], MISFET [3] and InP channel FET [5] of comparable gate length. A higher f_{max} value is primarily due to higher g_{mo}/g_{ds} (i.e. 50) and C_{gs}/C_{gd} (i.e. 15) ratio as a result of higher carrier concentration and good carrier confinement capability. An f_{max}/ f_T ratio of 4-5 over a wide gate and drain bias region was obtained which is

higher than other devices [2-5]. At a low drain-source bias of 2.5-3.0V, f_{max} values were 30-35 GHz suitable for low voltage battery operation MMICs [4].

In summary, we have presented design and performance of double heterojunction PHEMT for linear power applications. DC and RF results indicate that DH-PHEMT is a better candidate for high linearity, power and efficiency and low power consumption MMICs.

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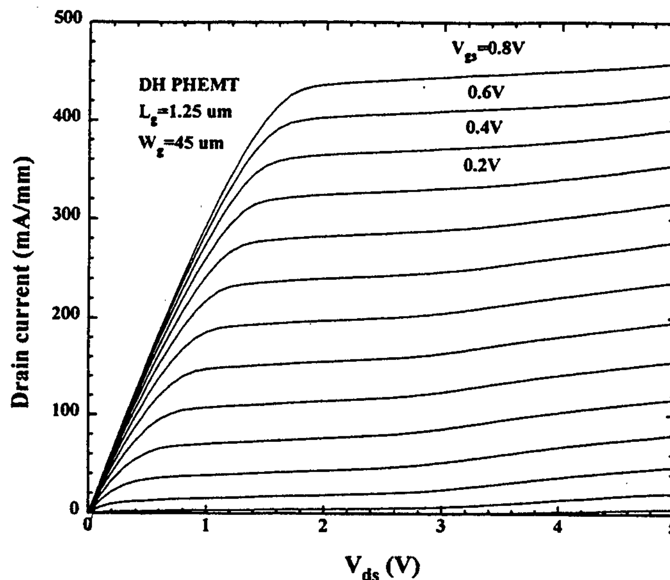


Fig. 2. I-V characteristics of 1.25 x 45 μm^2 double heterojunction PHEMT device.

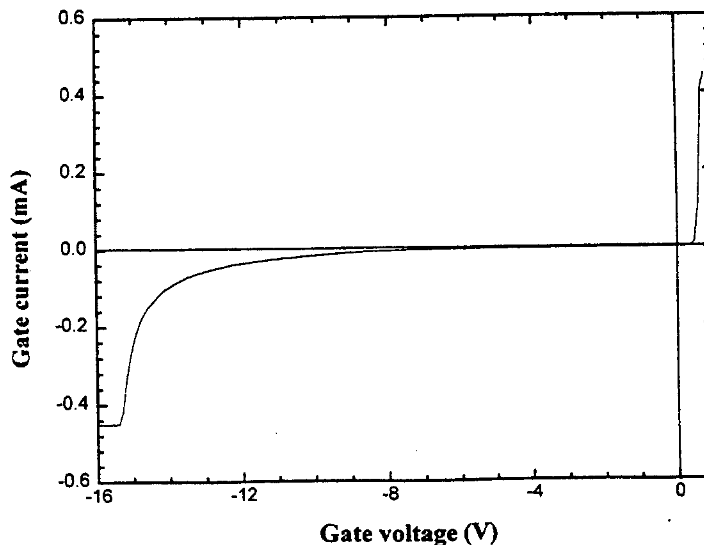


Fig. 3. Breakdown voltage of 1.25 x 45 μm^2 double heterojunction PHEMT device.

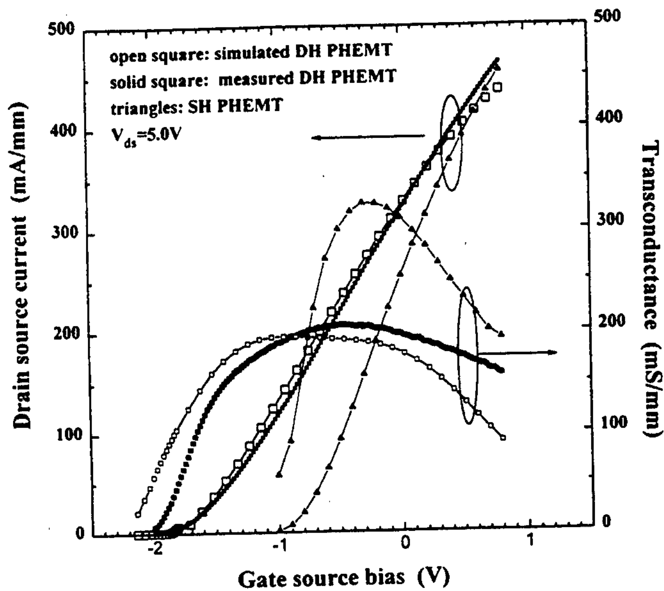
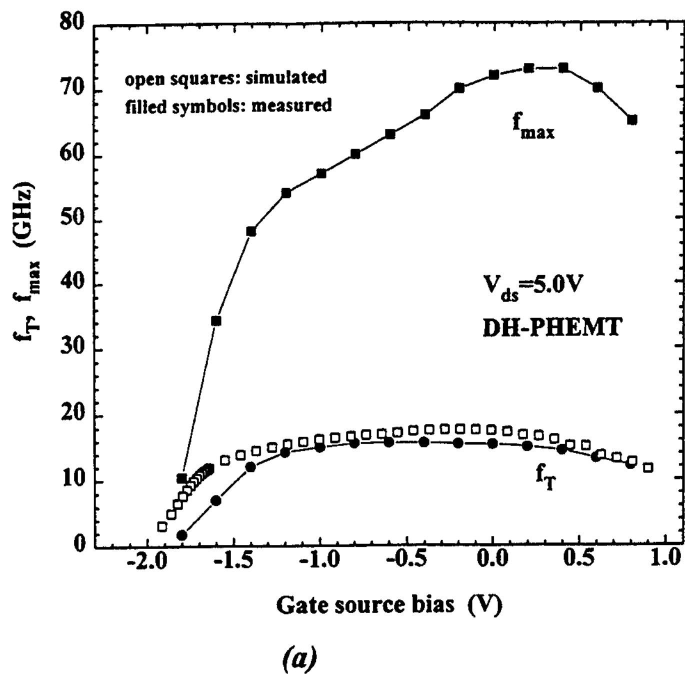


Fig. 4. Transfer characteristics of 1.25 x 45 μm^2 single and double heterojunction PHEMT.



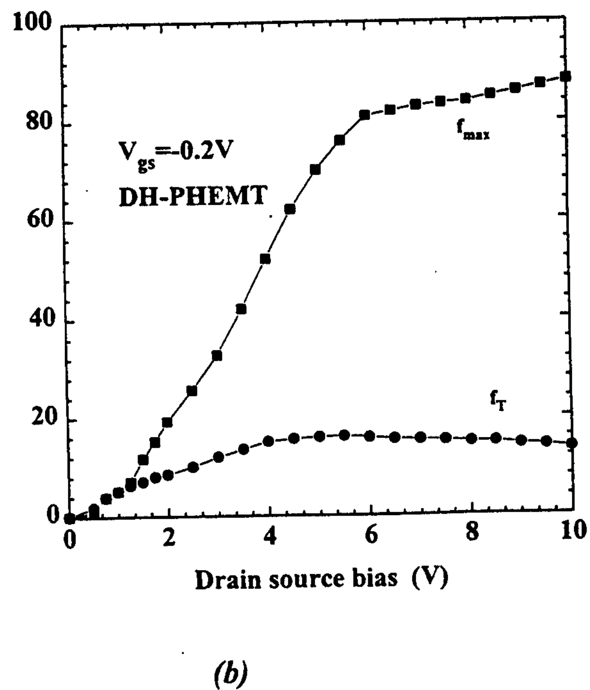


Fig. 5. cut-off frequency (f_T) and maximum frequency (f_{max}) as a function of (a) gate source bias (b) drain source bias of 1.25 x 90 μm^2 double heterojunction PHEMT device.

Single-Electron Spectroscopy of Individual Slow Interface Traps in Submicron MOSFETs

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It is discussed the effect of infrared radiation on random two-level switching in the drain current in a small area MOSFET, which is commonly referred to as a random telegraph signal (RTS). It is shown that the mean duration of one of two current states of the RTS has to depend highly on the intensity, the spectrum, the direction, the polarization of the radiation, that permits to create a novel single-electron spectroscopy of individual slow interface traps giving a lot of unique physical and device information.

The RTSs are caused by random capture and emission of an electron by a single interface trap with the very long mean capture and emission times, τ_c and τ_e.[1] Believing these times to be equal to their equilibrium values, τ_c^e and τ_e^e, one finds the energy level of the trap ε_t with the use of the relationship:

$$\frac{\tau_c^e}{\tau_e^e} = \frac{f}{1-f} = \frac{1}{g}\exp\left(-\frac{\varepsilon_t - \varepsilon_F}{T}\right) \tag{1}$$

(f is the electron occupancy of the level, g is its degeneracy, T is the temperature in energy units, ε_F is the Fermi level). A large body of research has revealed many nontrivial features of these traps, among which are: the sharp temperature dependence of the capture cross section, σ, $\sigma = \sigma_0 \exp(-\Delta E_B/T)$; relatively high activation energy $\Delta E_B \gg \varepsilon_t$; a big scatter of ΔE_B from trap to trap; a drastic change of ε_t with the change of the gate voltage, V_g; and others.[2]

These data fit well the theory of the fluctuation traps.[3,4]. According to this theory such traps are set up by the charges built-in the oxide at the $Si:SiO_2$ interface and distributed at random along it. This causes a random potential pattern with a high amplitude in the near-surface layer of silicon. The wells and mountains of the pattern localize electrons and holes, respectively, nearby this surface. Therein lies the reason of the U-shaped density of the fast interface states.[5] Among these localized states exist some created by the small-scale cluster of attracting charges falling inside the large-scale repulsive fluctuation (Fig.1(a)). The cluster represents the Z-charged nucleus that localizes in its vicinity in *Si* an electron with a high binding energy ε_b. The large-scale fluctuation surrounds the nucleus with a high and broad barrier, with the height ε_B and the radius l, that slows the capture of electrons by this trap and rises its level: $\varepsilon_t = \varepsilon_B - \varepsilon_b$ (Fig.1(b)). Owing to this ε_t appears to be close to ε_F. As the trap captures mainly the electrons activated over the barrier, $\Delta E_B = \varepsilon_B$; as the captured electrons tunnel through the upper part of the barrier into a resonance level of the trap, $\Delta E_B < \varepsilon_B$. The most probable values ε_t and ΔE_B calculated by the optimum fluctuation method, as well as the calculated V_G-dependencies of τ_c and τ_e, of the RTS amplitude, and the like are in a good agreement with those observed at different temperatures.[3,4] Also a slow trap can be created if a like attractive nucleus falls within the potential barrier confining the width of the inversion channel.[3,4]

Consider the effect of a radiation on the RTS produced by such a trap. Under the photon flux I the mean emission time of an electron from the trap must be equal to:

$$\frac{1}{\tau_e} = \frac{1}{\tau_e^e} + \sigma_{ph}^{eff} I, \tag{2}$$

where σ_{ph}^{eff} is the effective photoionization cross section of the trap. Calculating it at the photon energy $\hbar\omega$, such that $0 < \hbar\omega - \varepsilon_b \ll \varepsilon_b$, with the hydrogen-like-center model and neglecting by quantization of electrons in the inversion layer and the reflection of incident radiation from interfaces one obtains that:

$$\sigma_{ph}^{eff} = \sigma_{ph}^0 = 2\pi^2 \frac{e^2}{\hbar c} \frac{\hbar^2}{\sqrt{\varepsilon_s m^* \varepsilon_b}} \left[0.73 \sin^2\theta_a + 1.41 \cos^2\theta_a\right], \tag{3}$$

where m^* and ε_s are the electron mass and the permittivity of *Si*, θ_a is the angle between the vector-potential of the incident radiation and the normal to the interface. This model serves as an approximation

only, but is adequate in many respects. Equation (3) differs from the famous expression for the ionization of a hydrogen-like atom by numerical and angle factors, for an electron moves here in a half-space. At $\varepsilon_b = 0.5eV$ that is usual at near-room temperatures and $m^* = 5\times10^{-28}g$ it gives $\sigma^0_{ph} \approx 10^{-16}cm^2$, and from Eq. (2) it follows: if the emission time of an unirradiated trap is far longer than 1 s, it falls to 1 s under irradiation by the flux $I = 10^{16}cm^{-2}s^{-1}$. Thus, the effect is pronounced.. At low temperatures the values ε_b are noticeably less and σ^0_{ph} is to be higher, that allows to observe this effect still easier.

A moderate radiation affects only the time τ_e, for the thermal emission of an electron from a slow trap is very low. Its effect on the drain current and the capture time is negligible. This latter permits to find which current state of the RTS, the high or the low, corresponds to the filled trap and which to the empty. No other experiments exist, solving this problem being quite ambiguous at low temperatures.[1]

It may be that the reflection of the incident electromagnetic wave by the gate reduces severely its electric field around the trap, causing the effective cross section σ^{eff}_{ph} to be much less than σ^0_{ph}. Consider with the opaque metal gate how to avoid this under the following real conditions:

$$\sqrt{\varepsilon_s}/\Omega_p\tau_p \ll \beta \equiv \sqrt{\varepsilon_s}\omega/\Omega_p \ll 1, \qquad d^2\Omega_p^2\varepsilon_{ox}/c^2\varepsilon_s \ll 1. \tag{4}$$

Here τ_p and Ω_p are the carrier momentum relaxation time and the plasma frequency in the metal, ε_{ox} and d are the permittivity and the thickness of the oxide. If the radiation is polarized along the interface plane, σ^{eff}_{ph} is less than σ^0_{ph}, as the factor $4\beta^2$ estimated as 0.1÷0.01 depending on the gate metal, for the plasma frequency in metals is very high. If the electric field of the wave lies in the plane of its falling:

$$\sigma^{eff}_{ph} = 2\pi^2\frac{e^2}{\hbar c}\frac{\hbar^2}{\sqrt{\varepsilon_s}m^*\varepsilon_b}4\cos^2\theta\frac{1.41\sin^2\theta + 0.73\beta^2}{\cos^2\theta+\beta^2}. \tag{5}$$

θ is the angle the incident wave makes with the normal to the interface. σ^{eff}_{ph} is highly θ-dependent. At $\theta = 0$ and $\theta = \pi/2$ it is much less than σ^0_{ph}, as the same factor $4\beta^2$, but it turns out even to be several times higher than σ^0_{ph} as the angle differs slightly from $\pi/2$: $\beta < \pi/2 - \theta \ll 1$. Both considered limiting cases (see Eqs. (3), (5)) permit to expect that in intermediate cases with the radiation diffraction caused by the real gate structure, one can obtain a high value σ^{eff}_{ph}, if irradiates the MOSFET by a proper way.

The above estimations show a high photosensitivity of RTSs. Thus one can find the spectral curve $\sigma^{eff}_{ph}(\omega)$ from the measured ω-dependence of τ_e and Eq. (2). For hydrogen-like atoms this curve rises by step from nil at the photon energy being equal to the binding energy of an electron by the ion. For real semiconductor traps it rises not by step, but more or less smoothly depending on the deviation of the real electron-trap interaction from the attractive Coulomb potential. The distributed nucleus and the fact that, the height of the barrier is higher along the interface than in the normal direction,[3] are the added factors of a smooth rise of $\sigma^{eff}_{ph}(\omega)$ for these slow traps. The curve $\sigma^{eff}_{ph}(\omega)$ may also exhibit a certain structure in the range $\hbar\omega \approx \varepsilon_b$, being besides θ_a-dependent. Absorbing a photon the captured electron may pass into the free states with a few athimutal quantum numbers L: the transitions in the states with $L = 2$ cause the factor before $\sin^2\theta_a$ in Eq. (3) and in the states with $L = 1, 3$ cause the factor before $\cos^2\theta_a$. The threshold energy for these transitions may be estimated as: $\varepsilon_b + \hbar^2L(L+1)/2m^*r_m^2$, where r_m is the distance of the barrier maximum from the nucleus. So the transitions in the free states with $L = 1, 2, 3$ have to decay at different photon energies, that has to be marked in the curve.

The photoionization of slow traps is also possible at $\hbar\omega < \varepsilon_b$ owing to the tunneling of the excited carrier through the barrier surrounding such a trap. At such photon energies the cross section decreases with decreasing ω primarily because of the tunneling exponent that gives:

$$\ln\sigma^{eff}_{ph}(\omega) = C - \frac{\varepsilon_b - \hbar\omega}{\varepsilon_d}, \tag{6}$$

where C is a certain constant. For the optimum slow interface trap[3] the energy ε_d can be estimated as:

$$\varepsilon_d = \left(\eta Z e^2 \hbar^{2^*} / 2\pi^2 m^* \kappa r_m^3\right)^{1/2}, \quad (7)$$

where η lies from 0.5 to 1, $\kappa = (\varepsilon_s + \varepsilon_{ox})/2$. This gives $\varepsilon_d = 0.006\ eV$ for the values being typical at near-room temperatures: $Z = 4$, $r_m = 5\ nm$, $\kappa = 8$. In the range $\hbar\omega < \varepsilon_b$ the curve $\sigma_{ph}^{eff}(\omega)$ may also have the spikes at certain frequencies that is caused by the optical transitions of the captured electron from the ground state to the resonance ones and its following tunneling through the barrier.

Of considerable interest are the variations of $\sigma_{ph}^{eff}(\omega)$ with the temperature and, especially, with the gate voltage. For understanding these latter consider how the change of V_G varies the structure of a slow trap. Such a trap has 3 different typical lengths: $l \gg r_m \gg a_Z$; here $a_Z \equiv a_1/Z$ is the typical radius of the nucleus, $a_1 = 4\kappa\hbar^2/m^*e^2$ is the scale of the wave function of an electron localized by a sole charge $+e$ built into the $Si{:}SiO_2$ interface.[3] The main effect is caused by the electron screening of the large-scale barrier. The longer its radius l, the easier it is screened and the sharper the decrease of its height ε_B as V_G increases (see Fig. 1(b)). This causes only the corresponding sharp lowering of ε_t and decrease of the capture time and has no effect on the emission time and the photoionization spectrum. These latter depend on the change of ε_b, which is relatively slight, as is determined by the shorter length r_m. The energy ε_b increases as V_G increases.[3] This causes the corresponding increase of τ_e^e and shift of the photoionization threshold being correlated to one another. The spacing r_m lengthens as V_G increases that affects the above-discussed near-threshold structure of the curve $\sigma_{ph}^{eff}(\omega)$. One can calculate this variation using the derived V_G-dependence of the potential energy in the near-nucleus region.[3]

In most papers the slow traps are thought to be placed not in silicon but in the oxide. Consider why the oxide-trap model can not explain the observed V_G-dependencies of τ_c^e and τ_e^e. and why the optical measurement is to clarify the genesis of the traps and to indicate, where they are placed, in SiO_2 or in Si.

By the oxide-trap model the RTSs are caused by multiphonon capture of carriers from the inversion layer into a trap placed in SiO_2 (Fig. 2). The observed decrease of the ratio τ_c^e/τ_e^e, that is, lowering of ε_t (see Eq. (1)), with increasing V_G is explained in this model by the fact that the trap is offset by the distance h from the interface: $h = d \times \partial\varepsilon_t/\partial V_g$.[1,2] In such a case it must be: the longer h, the sharper the increase of τ_e^e as V_G increases, whereas τ_c^e is independent of the shift of ε_t and decreases rather slightly. The experiments have shown just the reverse: the traps with the sharpest decrease of τ_c^e/τ_e^e have a sharp decrease of τ_c^e and a slight increase of τ_e^e,[2] as it must be in the fluctuation-trap model. The oxide-trap model can not also explain the following. At multiphonon capture of an electron from silicon to an oxide trap its capture cross section incorporates not only the probability of thermal activation, $\exp(-\Delta E_B/T)$, but also the probability of electron tunneling through the oxide, $\exp(-h/\lambda)$. Hence the factor σ_0 in the observed relation, $\sigma = \sigma_0 \exp(-\Delta E_B/T)$ must have the form: $\sigma_0 \sim \exp(-h/\lambda)$. The barrier of this tunneling U is very high (>$3\ eV$) for all the studied traps having the level ε_t nearby the Fermi one, and the tunneling length is very short: $\lambda = \hbar/\sqrt{8m_{ox}U} \sim 0.1\ nm$, where $m_{ox} = 1.2\ m_0$ is the electron effective mass in SiO_2. From the V_G-dependencies of ε_t it has been found for most of the studied traps that $h > 1\ nm$; whence it follows that the probabilities of electron tunneling into these traps have to be less than 10^{-4} that causes very small values of σ_0. But the measurements at near-room temperatures have given the high values: $\sigma_0 \sim 10^{-14} \div 10^{-15}\ cm^2$,[2] being typical for attractive centers in Si. In addition, for a number of the traps the V_G-dependence of ε_t is so abrupt that it has been found: $h \sim 10\ nm$. The electron transfer from Si in so distant oxide traps is impossible at all.

The experimental finding of the photosensitivity of the RTS emission time will serve as the reliable evidence of the fact that the electron captured by the interface slow trap is localized in silicon, not in the oxide. The photoionization cross section for the oxide traps under infrared radiation has to be many orders less than it follows from Eqs. (3), (5), for the electron under $\sim 3\ eV$ barrier has a very small scale of its wave function, λ, and has to tunnel to silicon under this barrier through the distance $h \gg \lambda$.

Notice that the like spectroscopy of single defects was applied to $GaAs/Al_xGa_{1-x}As$ tunnel structures, where it revealed that the RTSs were exerted by the ordinary bulk traps placed in wide-gap regions.[6] The above-discussed specific slow interface traps are very different from the bulk silicon and oxide traps, and the spectroscopy is to show their unusual structure and properties. The $Si{:}SiO_2$ heterojunction differs by the fact that its height exceeds noticeably the gap of *Si*. This is why, taken alone, the observation of the radiation effect on one of the times of an RTS in MOSFET answers the principal question, where the slow traps are situated, in *Si* or in SiO_2. In addition, the energy levels of the traps in the $GaAs/Al_xGa_{1-x}As$ structures lie much below than the Fermi level, that permits to study only the light-induced RTSs. This renders impossible the independent temperature measurements of the energy level of the trap with the use of Eq. (1), the measurements of the V_g-dependence of this level, a comparison of these results and the results of the optical measurements. The full complex of these measurements has to provide the unprecedented extensive data on the properties of the discussed interface traps, the $Si{:}SiO_2$ interface.

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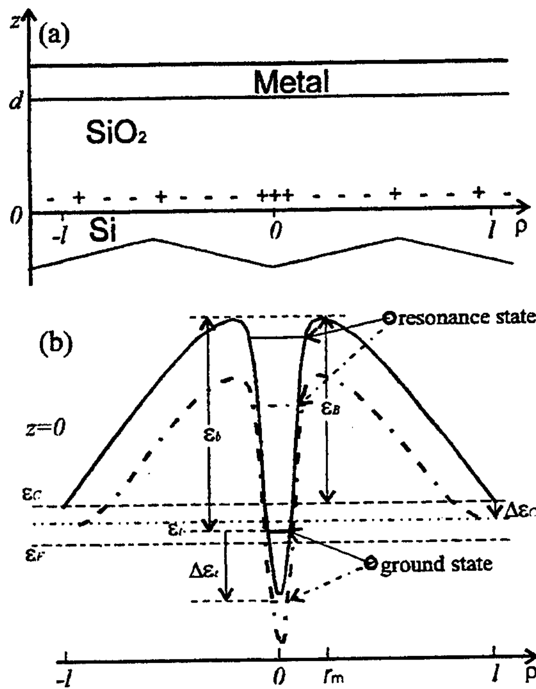

Fig.1 - (a) Random distribution of the charges built-in the oxide: a small-size attractive cluster within a large-scale repulsive fluctuation. (b) The corresponding energy diagram at the $Si{:}SiO_2$ interface: the local bending of the bottom of the silicon conductivity band (the solid curve); the position of this bottom averaged over the MOSFET (the dashed line); the local band bending as the gate voltage increases by the value ΔV_G (the dash-dotted curve). $\Delta\varepsilon_t$ and $\Delta\varepsilon_B = \varepsilon_{B'} - \varepsilon_B$ are the lowerings of the ground state energy and the height of the barrier of this slow interface trap under this voltage change.

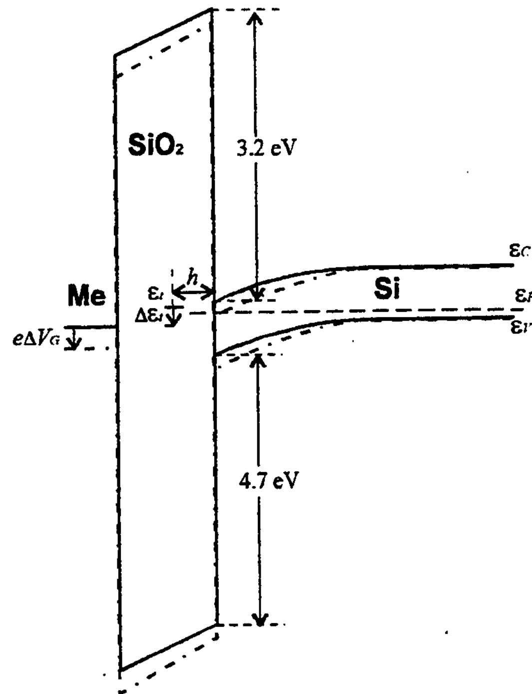

Fig.2 - Energy diagram of a MOS-structure with a slow trap in accordance with the oxide-trap model. (solid curves). The same diagram as the gate voltage increases by the value ΔV_G (dash-dotted curves).

Characterization of Surface Roughness During Molecular Beam Epitaxy on GaAs Substrates by Measurements of Scattered Laser Radiation Intensity

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1.0 Introduction

Usually the direct monitoring of surface roughness of substrates and epitaxial films is performed by means of microscopy - the optical, electron, or tunneling one. As a rule, these methods are used after the epitaxial growth of films is finished. There are just a few works where *in-situ* direct methods of the surface roughness monitoring are used, for example, the tunneling microscopy [1]. Nevertheless, even in that case the growth process must be interrupted for the period of analysis. In addition to the direct monitoring of surface roughness by microscopy the different indirect methods are used. Particularly, an indirect information on surface roughness can be obtained in situ from a RHEED diffraction image. Moreover, the use of RHEED and X-ray spectral analysis together allows the information on the composition of complicated compounds to be obtained in situ. The authors have shown this, for example, in [2] for PbSnTe and CdTe films prepared by molecular beam epitaxy (MBE). But sometimes the electron beam can change the growth conditions near the point where it hits the substrate surface. In other words, the electron beam leave its "track" on the epitaxial film.

Except RHEED, few works are devoted to optical methods of control of the morphology of film surfaces in situ during MBE. Most of them concern the ellipsometry. For example, authors of [3] described the sensitivity of this method with respect to the roughness of GaAs substrate, and in [4] this method was used during MBE of HgCdTe films to control the composition and roughness.

In addition to ellipsometry, authors of [5] have found another optical method sensitive to surface roughness - measurements of intensity of laser radiation scattered by surface (LRSS) Particularly, LRSS allows one to monitor changes in surface microstructure during epitaxy of $In_xGa_{1-x}As$ on GaAs substrates *in situ* with an accuracy about 1-2 monolayers and to watch after formation of mismatch dislocations. LRSS is simpler than ellipsometry and requires only one optical window in the MBE set.

The aim of this work was to study LRSS possibilities for monitoring the annealing of surface of GaAs substrates and MBE growth of ZnSe and Ge films.

2.0 Experimental procedure and discussion

The standard two-chamber high vacuum MBE set was used. It was equipped with the RHEED, an Auger spectrometer, a thickness/rate controller (TRC), and a mass spectrometer. To control the surface roughness *in situ* the authors used LRSS. Using LRSS the data on the changes of roughness of GaAs substrates during the cleaning by heating and on ZnSe and Ge films roughness at the initial stage of the growth were obtained. In Fig.2 the data obtained by LRSS, by mass-spectrometry during the cleaning of two different GaAs

(100) substrates, and by RHEED at the end of the cleaning are given.

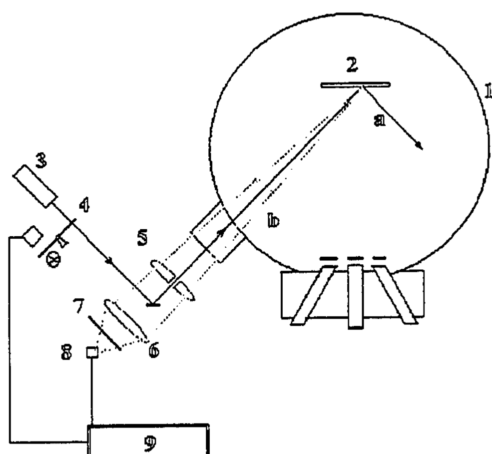

Fig.1. The schematic diagram of LRSS method. 1 - MBE technological chamber, 2 - substrate, 3 - He-Ne laser, 4 - 900 Hz mechanic chopper, 5, 6 - optic lens, 6 - optic filter, 8 - photodiode, 9 - amplifier.

The scheme of the method is shown in Fig.1. The beam of He-Ne laser 4 modulated at frequency 900 Hz hits substrate 2 at the angle close to 45°. Scattered laser radiation is gathered by optical system 5, 6 and then the signal from the photodiode 8 is fed to narrow-band amplifier 9. One can see that at T=100-200° C the scattered radiation intensity falls. This results from the smoothing of surface caused by water desorption. In the temperature range from 350 to 550° C the intensity of the signal increases. At the same time the mass-spectrometer detects As (whose mass equals 75) in the technological chamber (the insert in Fig.2). At T=580° C the signal rises very quickly and (4x2) superstructure appears on the RHEED screen. This corresponds to GaAs surface stabilized by Ga. The roughening of the microstructure of GaAs surface after oxide removal was reported before and confirmed in particular by scanning tunneling microscopy. Indirectly it is confirmed by [3] where changes of ellipsometry angles during the heating of GaAs substrate in vacuum and in the presence of As vapors were investigated (Fig.3). One can see, that in a vacuum at the same temperature as in our experiments (580° C) a drastic decrease of the ellipsometry angle Δ occurs. Authors supposed this fall to be caused by the change of the surface into (4x2) superstructure stabilized by Ga. It was confirmed also by the fact that this transition was not observed during the heating in the presence of As vapors. One can see, that the data obtained from simpler LRSS experiments fairly correlates with the ellipsometry data [3]. And a very high sensitivity of these two optical methods to atomic roughness of surface seems to be very interesting.

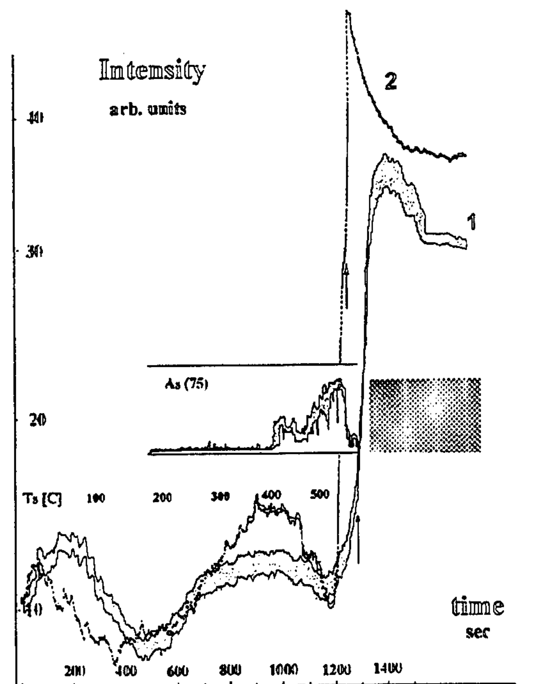

Fig.2. LRSS signal versus time and temperature of GaAs substrate cleaning. Mass-spectrometry data are given in the insert, the time and the temperature scales coincide. The finishing points of heating for both samples 1 and 2 are marked by arrows. On the right hand of arrows the cooling of samples was done.

Ge and ZnSe were deposited by means of thermal evaporation from a diffusion cells. In Fig.4 the LRSS data obtained *in situ*

during the epitaxy of ZnSe and Ge layers are given for two samples. The data were obtained under the same technological conditions: (4x2) superstructure of (100) GaAs substrate at initial stage, substrate temperature during the growth is 280° C; and the same intensities of both molecular beams. Both upper and lower curves correspond to [110] orientations of elliptically-shaped substrates with respect to the laser beam and differ from one another by 90° that was controlled by RHEED.

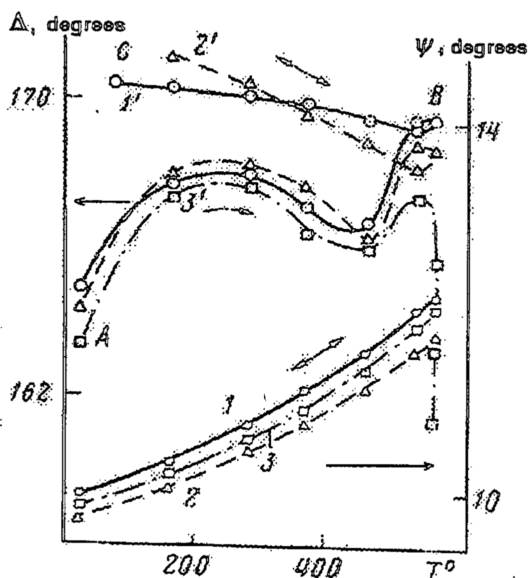

Fig.3. Ellipsometry angles versus temperature of GaAs substrate cleaning [3]. 1, 1' and 2, 2' correspond to the heating temperature below 580° C, 3, 3' - to the heating above 580° C.

One can see, that during the epitaxy of ZnSe the intensity of dispersed laser irradiation is almost constant. It may be caused by two reasons. The first one is the transparency of ZnSe at the wavelength of He-Ne laser. Nevertheless, even in this case the intensity of dispersed radiation may change as the roughness changes because of refraction. The second one is the low adhesion coefficient of ZnSe and low growth rate of ZnSe film at the beginning of the growth on Ga-enriched surface of GaAs reported in [6]. Note that the thickness of epitaxial films in Fig.4 was taken from the data read from the thickness/rate controller in situ and not from direct measurements after the growth has finished. At the beginning of the growth of Ge layer (curve a) LRSS signal slightly decreases, then slightly grows, and then falls again, and decreases several times as the thickness of Ge layer attains a value about 80 nm. For another [110] orientation of the substrate the LRSS signal increases almost monotonously up to a value about 40 nm and slightly descreases to a value of 80 nm (curve b).

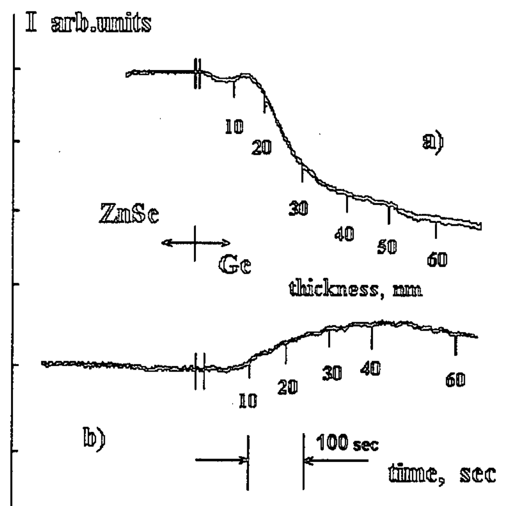

Fig.4. LRSS signal versus time and thickness of Ge epitaxial layer. The moments of ZnSe cell closing and Ge cell opening are marked on the curves. Both curves correspond to [110] substrate orientations which differ from each other by 90 °.

At present the authors can't provide an exact explanation of the above results for the lack of experimental data, but can suppose that the qualitative difference between curve (a) and curve (b) is due to the step-flow growth of Ge layer on GaAs substrate. This type of epitaxial growth is well known and may result from deviation of the crystal plane from a singular orientation.

A small decrease in LRSS signal at the beginning of Ge layer growth may occur as the surface becomes smoother or as

the optical characteristics of the upper layer of the film change at that moment. The authors suppose, that curve (a) corresponds to the direction of laser beam along the steps while curve (b) corresponds to that across the steps. So, for the case of laser beam being directed along the steps (curve a), the subsequent decrease of the signal may result from smoothing of Ge film as its thickness increases. If the laser beam is directed across the steps (curve b), then its dispersion may be caused by the islands on the initial stage and by the steps later.

3.0 Summary

As one can see from the data obtained by LRSS, RHEED and mass-spectrometry, LRSS method is very sensitive to changes in surface roughness of GaAs substrates. Particularly, the intensity of laser radiation dispersed by surface may increase several times in the temperature range 550-580°C where GaAs surface rebuilds into (4x2) superstructure. Also, this method allows the morphology of growing Ge film to be controlled in situ. Experimental data allow us to suppose that this technique is sensitive to the 3D growth and step-flow growth of Ge surface. So, whenever any calibration needs to be done, LRSS method can be used as the main or additional non-destructive method to control the surface conditions of GaAs substrates and epitaxial films during MBE in situ. In addition, it is worth to stress that the experimental data which need to be checked and were not presented in this paper, nevertheless allow us to suppose that this method can be applied to control the growth of several materials in layer-by-layer manner to count the atomic layers just the same as it can be done by RHEED.

Acknowledgements

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New Evidence for Minority Carrier Complete Drag Phenomenon in Silicon and Its Impact on Device Characteristics Modeling

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1. Introduction

A correct treatment of physical phenomena governing charge carrier transport in semiconductor samples allows a better understanding of semiconductor device operation and enables to determine physical limitations on their parameters. Among scattering mechanisms that are responsible for the observed values of charge carrier mobility in semiconductors the contribution of electron-hole scattering (EHS) proves to be rather ambiguous. Since the first mention of EHS as a factor that could substantially change the charge carrier transport coefficients [1], a large number of papers devoted to study of this phenomenon in various semiconductor materials (Ge, Si, GaAs) [2-13] as well as to determination of its effect on the characteristics of semiconductor devices [14-17] have appeared in the literature. It was assumed at first that EHS makes the greatest contribution to charge carrier transport under high injection conditions, when the concentration of the injected carriers exceeds $10^{16}cm^{-3}$. However later it became clear that the influence of EHS can show up much more clearly under low injection conditions. The experimental detection of the effect of minority carrier complete drag in GaAs [18] confirmed the results of the theoretical treatment [3,5] and stimulated interest in the possibility that this effect may appear in Si, which is the most widely used material of semiconductor electronics. In this connection it is worth noting that a comparative estimate of the characteristic parameters of EHS carried out in [19] on the basis of experimental results obtained in [18], showed that effectiveness of EHS in Si is ~40÷50 times greater than in GaAs. However up to now no direct evidence has been presented in the literature in support of minority carrier complete drag existence in Si. To our mind the main difficulty of studying EHS in Si lies in the fact that Si is an indirect-gap semiconductor, as distinct from GaAs. This makes it difficult to use the optical technique, which has made possible a direct detection of minority carrier complete drag in GaAs. Thus the goal of this paper is to produce new experimental evidence for minority carrier complete drag in Si and to define the impact of this phenomenon on the characteristics of semiconductor devices. Our studies will be carried out on the basis of new method put forward recently by the authors [20], which is adapted specially for indirect-gap semiconductors. Therefore the paper is organized as follows. In Section 2 the basic concept and validity of this method are discussed. In Section 3 key results supporting minority carrier complete drag existence in Si are presented. Finally in Section 4 the influence of the drag phenomenon on the injection efficiency of p^+-n junction is discussed.

2. New Method for Determining the EHS Parameters in Structures with p-n junctions

Since optical methods are inapplicable in indirect-gap semiconductors, the only chance to investigate the EHS parameters in Si consists in utilizing electrical methods, e.g. in measuring the characteristics of multilayer structure dependent on EHS. In deciding on a particular characteristic of the structure, results obtained earlier were taken into account. Thus it is well known that EHS has a strong effect on the static current-voltage characteristic (CVC) of Silicon structures. Therefore the CVC of diode p^+-n-n^+ and n^+-p-p^+ structures under low injection conditions were chosen as a basic characteristic for the method under discussion. To find the CVC of the diode structure, it is necessary to solve the continuity equation in the base layer [21]. Using transport equations which correspond to the low injection conditions in n-base layer [12,13] and taking into account the fact that the doping impurities are distributed homogeneously in n-base, it is easy to show that continuity equation in the diffusive approximation can be reduced to [20]

$$\frac{d^2p}{dx^2} - \frac{p}{\mathcal{L}_p^{\,2}} = 0, \qquad (1)$$

where $\mathcal{L}_p = \left(D_p \frac{\mu_{pn}}{\mu_{pn} + \mu_p} \tau_p \right)^{1/2}$, D_p and μ_p are the usual hole diffusion coefficient and mobility respectively, τ_p is the hole lifetime and μ_{pn} is the mobility

determined by electron-hole collisions. Then standard computations based on equation (1) result in an CVC described by

$$V = \frac{k_B T}{q}\ln\left(j/j_0\right) + j\rho_n W_n, \qquad (2)$$

where k_B is Boltzmann constant, T is the temperature, j is the current density, q is the elementary charge, W_n is the thickness of the n-base, ρ_n is the n-base layer resistivity, p_0 is the equilibrium hole concentration in the base layer and in the structures with $\left(W_n/L_p\right) \geq 5$ the quantity j_0 is defined by

$$j_0 = q\left[D_p \mu_{pn}/\tau_p\left(\mu_{pn} + \mu_p\right)\right]^{1/2} p_0. \qquad (3)$$

In the case if n-base layer doping N does not exceed $10^{17}cm^{-3}$ the equilibrium hole concentration can be written as $p_0 = n_{i0}^2/N$, where n_{i0} is the intrinsic carrier concentration in a weakly doped sample. However for highly doped layers with $N > 10^{17}cm^{-3}$ the band-gap narrowing phenomenon must be taken into account in Si [22]. On the basis of data presented in [22] and taking into account corrections introduced by electron-hole collisions [23] the following formula can be obtained for μ_{np}

$$\mu_{pn} = \frac{\mu_p}{\left[\left(j_0\right)_{exp}/\left(j_0\right)_{cal}\right]^2 - 1}, \qquad (4)$$

where

$$\left(j_0\right)_{cal} = \left(\frac{qn_{i0}^2 \exp\left(\Delta E_g/k_B T\right)}{N}\right)\left(\frac{D_p}{\tau_p}\right)^{1/2},$$

$\left(j_0\right)_{exp}$ is the experimentally measured value of j_0. Similar formula can be obtained for mobility μ_{np} in p-base layer of n^+-p-p^+ structure by replacement of indices $n \rightarrow p$, $p \rightarrow n$.

Equation (4) is the basis of the proposed method for determining μ_{pn} using diode structures. The quantities j, V, ρ_n, W_n and T are to be measured and the quantities D_p and ΔE_g are to be taken from independent experiments. As a result mobility μ_{pn} can be determined directly under low injection conditions.

3. Determining the Mobilities μ_{pn} and μ_{np} in Silicon under Low Injection Conditions

We had p^+-n-n^+ and n^+-p-p^+ structures fabricated. The detailed description of the samples has been presented in [20] and [24]. The CVC was measured for each of these structures using the standard techniques. A current density region was chosen for the measurement, in which a low injection level of non-equilibrium charge carriers was produced in the base layer of the structure. All measurements have been performed at temperature T=21°C. The measured data were processed in accordance with equation (4). The final results are presented in Fig.1 and Fig.2 (see points) with allowance made for scatter of the values of electrophysical parameters. Besides the experimental results following additional data are presented in Fig.1 and Fig.2. Curves 1 correspond to majority-electron mobility in Fig.1 and majority-hole mobility in Fig.2. Curves 2 correspond to the high injection level data by Dannhäuser [6] and Krausse [7] extrapolated to the low injection conditions through the use of known formula suggested in [8] (see also [13]).

It is worth mentioning that because of complexity of determining the lifetime in highly doped samples the scatter of this parameter presented in the literature, proves to be rather high. For example in n-type layer with $N=2.3\times10^{17}cm^{-3}$ the measured value of hole lifetime was $\tau_p=2.5\mu s$, whereas according to review paper [25] it lies in the interval $2\mu s \leq \tau_p \leq 16\mu s$. Of course the inclusion of data presented in [25] leads to rather large scatter of μ_{pn} , however to provide unbiased results we tried to take into account the scatter indicated in [25] as well. Thus keeping in mind the fact that the measured values of τ_p in n-type layer lie within the interval indicated in [25] we presented the final results in Fig.1 adding together the scatter indicated in [25] and the scatter inherent in our measurement. In p-type layers the measured

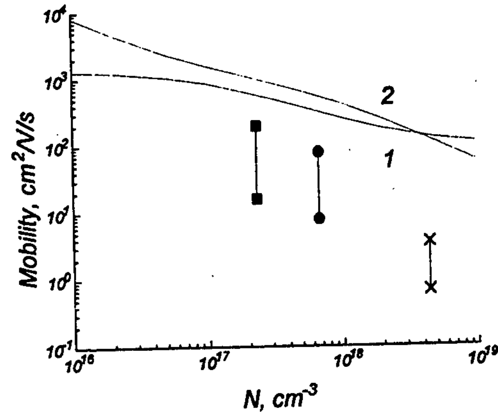

FIGURE 1. Results of measurement of the mobility μ_{pn} in n-type silicon.

values of τ_n differ noticeably from the values indicated in [25], e.g. for $N=5\times10^{17}cm^{-3}$ the measured value of electron lifetime was $\tau_n=0.3\mu s$ whereas according to [25] it lies in the interval $2.5\mu s \leq \tau_n \leq 8\mu s$. Since now the measured values of τ_n are outside of the interval indicated in [25], the

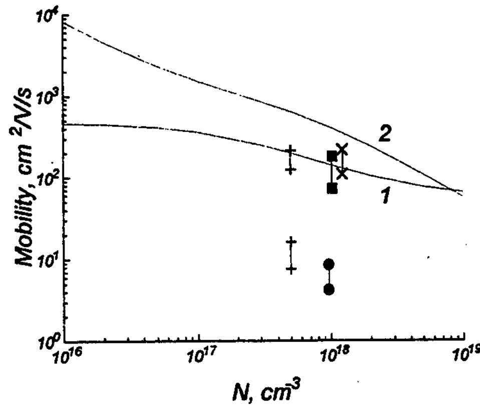

FIGURE 2. Results of measurement of the mobility μ_{np} in p-type silicon.

final results are presented in Fig .2 through the use of two points for each sample. The upper points correspond to the measured values of τ_n whereas the lower points correspond to the lifetime values presented in [25].

It can be seen from Fig.1 and Fig.2 that the measured values of μ_{pn} and μ_{np} turn out to be substantially smaller than the extrapolated values (see curve 2). An additional point to emphasize is that in n-type layers with $N>2\times10^{17}cm^{-3}$ we get that $\mu_{pn}<\mu_n$ (see Fig.1) and in *p*-type layers with $N>10^{18}cm^{-3}$ we get $\mu_{np}<\mu_p$ (see Fig.2). This result is of special interest, since according to [12,13] the condition $\mu_{pn}<\mu_n$ in n-type and $\mu_{np}<\mu_p$ in *p*-type is evidence that minority carrier complete drag by majority carriers is possible both in n-type and *p*-type Si even at room temperature $T=21^0$C.

4. Impact of Minority Carrier Complete Drag Phenomenon on Device Characteristics

In Section 2 the influence of EHS on CVC of diode structure has been already demonstrated over the range of small current density. However it will be shown now that at high current density the minority carrier complete drag phenomenon in highly doped p^+-layer brings into existence nonmonotone dependence of p^+-n junction injection efficiency on temperature, which may be of great importance for power device operation at low temperature. On the basis of transport equations suggested in [12,13] one can easily get within standard approach [1,26] for a saturation current of p^+-emitter j_{sn} following formula

$$j_{sn}=\frac{qn_i^2}{N}\sqrt{\frac{D_n\mu_{np}}{\tau_n\left(\mu_n+\mu_{np}\right)}}. \qquad (5)$$

Taking into account the commonly accepted dependencies on temperature of the parameters appearing in the equation (5) one can easily get

$$\frac{j_{sn}}{n_i^2}=\frac{q}{N}\sqrt{\frac{D_n(T_0)}{\tau_n(T_0)}}\left[Bx^{-(\alpha+1-\beta)}+x^{\beta+\gamma-1}\right]^{-1/2} \qquad (6)$$

where $B=\mu_n(T_0)/\mu_{np}(T_0)$, $x=(T/T_0)$, α, β and γ are of order $\alpha\approx1.5$, $\beta\approx1.5\div2.0$, $\gamma\approx0.1\div0.3$ in highly doped layers and their physical meaning is defined by following expressions

$$\mu_{np}(T)=\mu_{np}(T_0)(T/T_0)^{\alpha},$$
$$\tau_n(T)=\tau_n(T_0)(T/T_0)^{\beta},$$
$$\mu_n(T)=\mu_n(T_0)(T/T_0)^{\gamma}.$$

It follows from (6) that if contribution of EHS is negligibly small, i.e. $B\to0$, the quantity j_{sn}/n_i^2 increases with decreasing temperature. However if EHS is strong and minority carrier complete drag phenomenon comes into existence, i.e. $B>1$, the quantity j_{sn}/n_i^2 becomes a nonmonotone function of the temperature; more specifically it peaks at $T_m=\left[B\frac{\alpha+1-\beta}{\beta+\gamma-1}\right]^{1/(\alpha+\gamma)}$ and then decreases with decreasing temperature. This results in nonmonotone behavior of injection efficiency correspondingly. First it decreases with decreasing temperature, but passes through a minimum at $T=T_m$ and then builds up. The nonmonotone behavior of injection efficiency may be of great importance for low temperature operation of semiconductor devices.

5. Summary

The presented results are the first evidence indicating that minority carrier complete drag phenomenon is possible in Si. They were obtained through the use of the newly suggested method which now is the only method that makes it possible to measure mobilities μ_{pn} and μ_{np} in indirect-gap semiconductors under low injection conditions. Notice that large scatter of the measured μ_{pn} and μ_{np} values is conditioned by the scatter of minority carrier lifetime values. Improvement in technique for determining τ will make it possible to enhance the accuracy of the measured μ_{pn} and μ_{np} values. Yet it is worth noting that development of alternative methods based on different ideas is of great importance to our mind, since they will provide independent check on the presented results.

It follows from our consideration that EHS, and particularly minority carrier complete drag phenomenon, influence the injection efficiency of p^+-n

junction and thus almost all characteristics of bipolar devices. We are sure that this phenomenon is of prime importance for many characteristics of different devices. However up to now this issue has not received sufficient attention in the device modeling.

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Sensor Possibilities of Porous Silicon

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Porous silicon (PS) is a quantum-dimensional material,which main elements are quantum silicon wires and dots. Developed surface and essential dependence of fundamental properties (energy spectrum and density of states) from built-in and applied fields allow to hope on its unusual adsorbate properties. The dependence of PS photoluminescence and conductivity from the composition of gas ambience was observed in a number of publications [1,2]. In this paper the results of different gas ambience influence on optical and electrical properties of porous silicon (PS) and structures on its base are reported.

We investigated PS layers on monocrystalline Si and diode structures formed by aluminium and porous paladium layers on the partially oxidized porous silicon $Si^0(O)$. Wafers used in the experiments were p-type Si 0.03 and 4.5 Ωcm resistivity(ρ), single crystals with <111> and <100> mirror surfaces, respectively.

For the purposes of investigation of structures on the basis of low-dimensional elements an adequate optical media model was determined by comparison thickness d and porosity q layer values, obtained in situ formation PS from time dependence of reflected radiation with those, determined from gravimetrical method. It was stated that Maxwell-Garnet"s procedure in case of depolarization factor β, applicated to cylinder pore media (β_z=1/2, β_x=β_y=0, axe "z" is perpendicular to layer plane) was adequate. The developed method allowed us to determine thickness and porosity of PS layers in the range of thicknesses from 0.08μm up to 20 μm and porosity from 0.1 to 0.85. Thicknesses of Pd layers (d_1) from 10 to 60 nm were also determined from time dependence of reflected laser radiation in the course of its deposition by vacuum evaporation.

The optical experiments were perfomed on laser ellipsometre LEF-3M, equiped with air-tight reaction chamber. The changes of ellipsometric data(ψ ,Δ) in PS reflected radiation(630 ηm) under the influence of gas solvents and

ethylalcohol are discovered. It is stated , that magnitude and kinetics of ψ and Δ changings under the influence of molecules with nonzero dipole moment (acetone, alcohol) and zero dipole moment (benzene, four-chlorous carbon) are essentially distinguished. Follows to note, that influence of gas molecules with the nonzero moment incorvertible unlike the influence of saturated gas with the zero dipole moment. It is found ,that PS samples under the influence of ethylalcohol change a colour (brightly blue on crimson) and save it for a long time after the completion of influence. The ellipsometric data were calculated on the basis of the expressions for the case of anisotropic layer on the isotropic substrate [3]. The complex dielectric function was determined using the adequate effective medium model (described above), varying the number of media and their optical constant values. The initial d and q values, obtained in situ and by ellipsometry, differ not more then 0.02μm and 0.01 for d and q respectively. The comparison of the calculated data with those found by experiment showed that observed ellipsometric data gas exposure dependences are not explained by capillary effect or thin adsorbate layer input without accounting for the component property changes. The essential dependence of optical properties from dipole moment of adsorbed molecules points to possible mechanisms of energy spectrum modification of quantum wires under the influence of appearing electrical fields or components composition changing. The latest mechanism is developed in IR absorbtion bands and refractive index changes after exposure to ethylalcohol vapours, for example.

The current-voltage characteristics of diode structures were investigated by using Pd-Al and Al-Al contacts. Structures with Pd and Al contacts which had different conductivity of initial material, porosity and oxide thicknesses demonstrated different types of I/V characteristics, representing current transport mechanisms similar to Poole-Frenkel; tunnelling;mechanism, governed by the density of charges trapped on the interface states and in the oxide layer on the silicon pillars; barrier and among them like those, which were observed at "Coulomb blockade" [4,5], Transient current characteristics demonstrated the value of constant current time forming about 10^2 s which gives the evidence to charge trapping and releasing in oxide and $Si\text{-}SiO_2$ interfaces [6].

Structures with Pd-Al contacts demonstrated the current change in H_2S environment higher more then some orders of magnitude in comparison with Al-Al contacts. At every subsequent value of applied voltage the time of current rising to $0.8I_{sat}$, where I_{sat} - saturation current value, is 10-15 s, then it

takes 10^2 s to achieve I_{sat} . Quick processes after decomposition of H_2S on Pd electrode are probably determined by forming of polarized hydrogen atom layer on Pd-SiO_2 interface, adsorbtion and desorbtion and atomic hydrogen transition from external to internal Pd surface. Slow processes may be connected with gas diffusion into SiO_2 layer and also with charge trapping in SiO_2 and interfaces [7].

The exposure to H_2S environment not only changes the current magnitude at the fixed voltage, but can change the shape of I/V dependence. It is stated that H_2S effect can cause the reversible change of I/V characteristics parameters.

We had found some particular features of I/V characteristics of Pd-Si^o(O)-Si-Al structures: the negative slope of I(V) in the area of zero bias for both negative (Pd_+) and positive (Pd_-) polarities of applied voltage; the dependence of current on H_2S concentration is not identical in different ranges of applied voltage.

We propose the existence of the built-in space charge in the sample which sign and magnitude is controlled by the applied field and environment. The space charge sign in the initial state corresponds to positive polarity of Pd electrode. The confirmation of this proposal is the existence of the current when the sample was simply in a short circuit with an ammeter and the open-circuit voltage V_{xx} (10-100 mV), which is dependent on electrode material (Pd, Ni, Al) and PS oxidation time. The gas concentration increasing is accompained by V_{xx} decreasing and even changing polarity for several samples.

The gas phase sensitivity of sensor output signal I may be determinated by a potential barrier height φ dependence on gas concentration. For different current transport mechanisms I(φ) has the following form [8]: $I=I_O \exp(-q\varphi/kT)$. The dependence of $\ln I_g/I_{in}$ (I_g and I_{in} - the current in and without gas environment) on H_2S concentration permit us to estimate the change in the potential barrier height Δφ as a function of H_2S concentration. The obtained H_2S concentration dependences of the potential barrier height Δφ and the open-curcuit voltage ΔV_{xx} changes are accompained, what is illustrated by Fig.1. The comparison of concentration dependences of Δφ for mono-Si [9] and obtained for PS structures reveals the more stronger dependence on H_2S concentrations for silicon structures with low dimensional elements, than for analogous structures, based on the same , but mono-Si. The most sensitive to H_2S are structures with d=6÷12 μm, q=0.7÷0.8, d_1=50÷60 nm, formed on p-Si (ρ=0.03 Ωcm).For example, influence of gas phase with H_2S traces (three molecules of H_2S to 10^9 molecules of nitrogen) can change a current through the structure by several times.

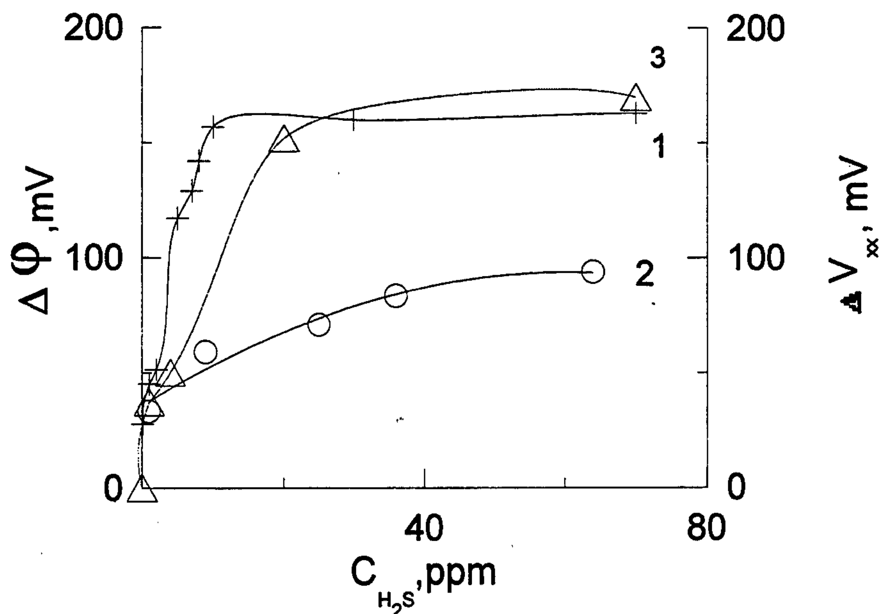

Fig.1. Concentration dependence of $\Delta\ \varphi$ and $\Delta\ V_{xx}$ for PS structures (1,3) and $\Delta\ \varphi$ for mono-Si (2).

The obtained results indicate, that porous silicon- material with quantum dimensional elements- demonstrates a lot of unusual properties , among them especially high sensor sensitivity , which opens the new possibilities of creating sensors on its basis.

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PHYSICAL MODEL OF GR NOISE OBSERVED UNDER INVERSION CONDITIONS NEAR THE pSi/SiO_2 INTERFACES IN SIMOX SUBMICRON MOSFETs AND ITS APPLICATION FOR DEFECT CHARACTERIZATION

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One of the typical noise features of submicron SOI MOSFETs with a *p*-type silicon film is that some non-trivial generation-recombination (GR) noise component manifests itself under inversion conditions near the pSi/SiO_2 interfaces. For the first time, this noise has been found in SIMOX AM *p*MOSFETs [1]. The phenomenon consists in the appearance of a GR noise component with an intensity which increases rapidly with increasing gate voltage in a weak inversion so that this noise becomes very high under strong inversion conditions. The peculiar property of this noise is that it can be described by the following Lorentzian $S_I(f) = a\tau^3/[1+(2\pi f\tau)^2]$ where S_I is the spectral density of the drain current noise, τ is the noise relaxation time that increases with increasing gate voltage, f is the frequency, and, finally, a is the empirical amplitude coefficient. Note that the behaviour of this noise seems to be non-trivial. Really, on the one hand, the fact that this noise is closely related to the specific conditions (inversion) at the pSi/SiO_2 interface suggests that the noise is of an interface nature but, on the other hand, such a noise has to be reduced significantly in AM/DM devices under strong inversion conditions due to screening by the inversion layer [2]. This may result in a decrease but not in an increase of the noise with an increase of the inverting gate voltage in such devices. Moreover, the dependence $S_I(0) \sim \tau^3$ has not been reported previously as a result of experimental

or theoretical investigations (the dependence $S_I(0) \sim \tau^b$ were $b = 1 \div 2$ is usually observed for GR noise components).

Recently we have succeeded in detecting the same noise component in submicron SIMOX EM *n*MOSFETs and DM *p*MOSFETs and to obtain additional important information about the properties of the noise considered. For example, in the case of EM *n*MOSFETs the dependence $S_I(0)/I^2 \sim \tau^3$ is observed (where I is the drain current) and the value of τ appears to be independent of the gate voltage if the value of I is kept constant.

In this paper, the physical model of the noise considered is developed and the results of its application to the experimental data on the noise generated near the inverted back interface are presented. A new method for noise spectroscopy of defects in SOI MOSFETs is developed on the basis of the model proposed.

Accordingly to the model, the noise is due to some defects located in the *p*-Si film at a rather small distance from the interface so that the defects are separated from the interface by the inversion layer. Capture and emission of electrons by such defects in the depletion layer of a MOSFET is accompanied by GR fluctuations of the local space charge. This gives rise to fluctuations of the depletion layer width W and of the inversion layer potential Ψ_s. As a result, the thickness of the *p*-channel in AM/DM *p*MOSFETs and the free electron number in the inversion channel of EM *n*MOSFETs fluctuate which manifests itself as a drain current noise.

By using the Poisson equation and the dependences of I on W in AM/DM *p*MOSFETs and on Ψ_s in EM *n*MOSFETs, the following relations for the drain current spectral density of the increasing low-frequency noise in a linear mode of operation have been obtained for the above two types of devices, respectively:

$$S_I(f) = D_s C_n C_p \left\{ \tau^3 A \Big/ \left[1 + (2\pi f \tau)^2 \right] \right\}, \tag{1}$$

$$S_I(f)/I^2 = D_s C_n C_p \left\{ \tau^3 B \Big/ \left[1 + (2\pi f \tau)^2 \right] \right\}, \tag{2}$$

$$\tau = 1/(C_p p), \tag{3}$$

where D_s is the density of defects, C_n and C_p are their capture coefficients for electrons and holes, respectively, A and B are coefficients determined by the parameters of the devices and their operation conditions and p is the free hole concentration near the defects considered (that decreases with increasing gate voltage). As is seen, the formulae (1) - (3) explain all properties of the GR noise studied including the "exotic" dependences $S_I(0) \sim \tau^3$ and $S_I(0)/I^2 \sim \tau^3$.

By applying (1) and (2) to the experimental data on the noise observed under inversion conditions at the back interface of different SIMOX MOSFETs processed in a 0.5μm technology, the following new information about the defects has been found.

1. The increasing τ values observed in different samples lie in different ranges that change from $\tau = (5 \div 10)$ μs to $\tau = (1 \div 5)$ s.

2. The increase of τ with the back gate voltage U_{Gb} described by the dependence $\tau \sim \exp(\beta_b \cdot U_{Gb})$ is characterized by the fact that the higher the range of τ (where its increase with increasing U_{Gb} is observed), the higher the value of β_b (Fig.1, curve 1). Note that in the framework of the above model this effect is explained as follows. Some difference exists in the

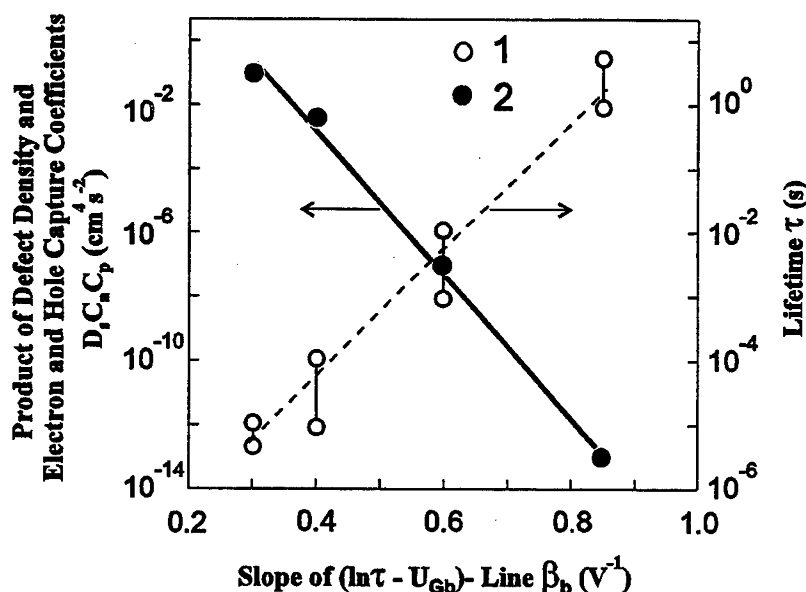

Fig. 1. The intervals of τ where τ increases with increasing back gate voltage (1) and the values of $D_sC_nC_p$ (2) determined in four different devices with different values of β_b

distance of the defects from the back interface in different samples so that higher values of τ (and of β_b) correspond to defects that are located more close to the interface.

3. The correlation is found between the values of $D_sC_nC_p$ and β_b, namely, $D_sC_nC_p$ decreases with increasing β_b (Fig.1, curve 2). Therefore, the smaller the distance of the defects from the interface, the lower the value of $D_sC_nC_p$. One of the possible reason for this is the decrease of D_s. However, some peculiar features of C_n and C_p may be also responsible for this decrease. The values of C_n and C_p can be determined from the experimental values of τ in weak inversion (see (3)) and in strong inversion (for which the above model gives: $\tau = 1/(C_n n)$ where n is the free electron concentration near the defects). Modelling the electron and hole distribution in the devices and combining with the experimental data allows to determine C_n, C_p, D_s and the position of the defects, i.e. to determine the parameters of film-related defects near back and front interfaces in SOI MOSFETs by this new method of noise spectroscopy.

Finally, the model proposed can be also used to explain the rapid increase of the $1/f$ noise typical for non-submicron DM *p*MOSFETs. This can be done by supposing that different GR components connected with the defects situated in different parts of a device area and characterized by different τ contribute to the noise so that its spectrum is the sum of different Lorentzians and this is the reason for the $1/f$ shape of the noise spectra.

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Observation Of Bulk Defects In SiC Crystals

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1.0 Introduction

The unique properties of silicon carbide make it a very promising material for a wide range of electronic applications. Even though recent advances in crystal growth technology have made it possible to produce 6H-SiC single crystals suitable for device fabrication, the presence of high-density defects in SiC substrates limits the large scale commercialization of SiC technology [1].

SiC boules grown by the commonly used physical vapor transport (PVT) method [2] exhibits a variety of crystallographic and structural defects; primarily, growth spirals and hollow structures of micrometric dimensions, called micropipes. Bulk grown 6H or 4H SiC consists of different polytypes (e.g., 3C or 15R) embedded in the main crystal. Considerable effort is underway in the SiC material growth technology to minimize the density of micropipes as well as structural and crystallographic defects. The full advantages associated with the wide band gap of SiC cannot be exploited until we understand the type of defects present and develop methods to minimize their density. New non-destructive methods are essential to map the type, location, and density of defects.

In this paper we report a novel "electrostatic mirror" (EM) method for observing structural defects in wide bandgap semiconductors, specifically, SiC. The micrographs of SiC samples examined using the EM method are more informative than the micrographs obtained by classical secondary electron (SE) imaging techniques. In fact the EM method makes it possible to observe bulk regions of the test samples with a scanning electron microscope resolution.

2.0 Experimental

In order to demonstrate the potential of this proprietary technique, several different SiC samples have been examined. The unique features of the EM method are clearly brought out in the various micrographs of high resistivity (500 Ohm-cm) 6H SiC single crystals presented below. These semi-insulating crystals, with fairly large defect density were grown using sublimation PVT technology, in a (0001) basal plane orientation. The thickness of the samples was about 500μm. Note that by classical transmission electron microscopy (TEM) it would not be possible to observe bulk features of such a thick sample. The EM and SE images were taken with a JEOL JSM-35CF scanning electron microscope. The accelerating voltage was 30 kV and working distance 39 mm. Directly before examination, the samples were subjected to chemical cleaning to remove any surface contamination. Prior surface

preparation consisted of mechanical polishing, ultrasonic cleaning in an acetone bath, etching in 5% HF and rinsing in boiling DI water.

3.0 Results and discussion

Typical micrographs of a PVT grown semi-insulating SiC sample obtained by the EM technique are shown in Figs.1 (a, b). Even though this crystal typically lacked any type of order in defect distribution, the most characteristic feature this sample is the rectangular, hexagonal and square zones often observed around micropipes (marked by arrow).

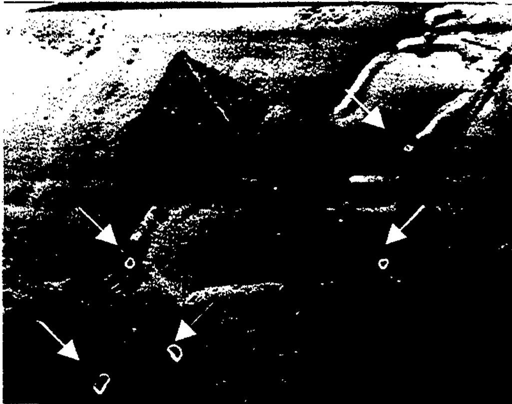

Figure 1(a). EM image of 500 Ωcm SiC wafer at x200 magnification

One possible reason for micropipe formation is super screw dislocation with Burgers vector oriented in the same direction with C-axis [3]. Formation of micropipes can be explained on the basis of instabilities in the crystal growth process such as temperature, pressure variation. In accordance with dislocation theory of polytype formation, the crystallization of new polytype structures is associated with the presence of screw dislocation in a crystal [4]. By Oswald steps rule [4], under unstable growth conditions, a highly unstable phase (for example, metastable 3C SiC) is formed during the beginning of crystallization. The rectangular and hexagonal features which are observed in Figs.1 (a, b), could be interpreted as the initial stages of new polytype crystallization.

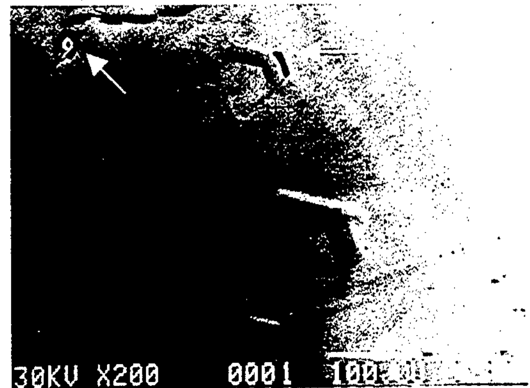

Figure 1(b). EM image of the same sample as in 1 (a). Large micropipes are seen at the edges of the hexagonal structures.

For comparison, images from an identical zone of a SiC sample obtained by the SE and EM imaging techniques are shown in Figs. 2(a, b) respectively. Fig. 2(a) shows three distinct micropipes observed by the SE technique. The micropipes appear as black spots with white surrounding rings, because the SE-emission from the edge of the pipe is higher than the SE-emission from the surface of the sample. On the other hand, the EM image, shown in Fig.2 (b) not only reveals the same micropipes seen in Fig. 2(a) but also possible structural defects in the bulk of the SiC sample, not observed in the conventional SE image.

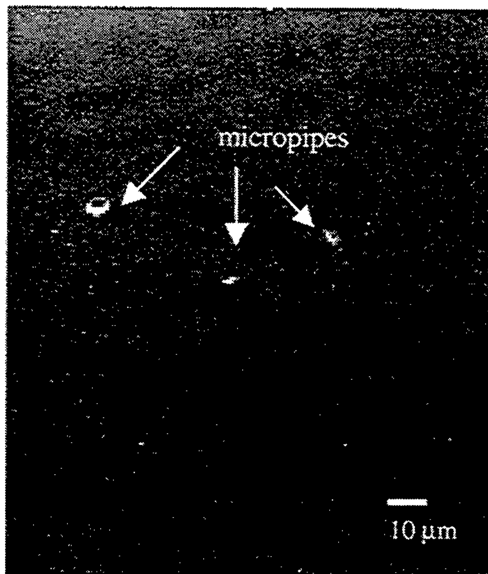

Figure 2 (a). SEM micrograph of SiC sample (SE-mode)

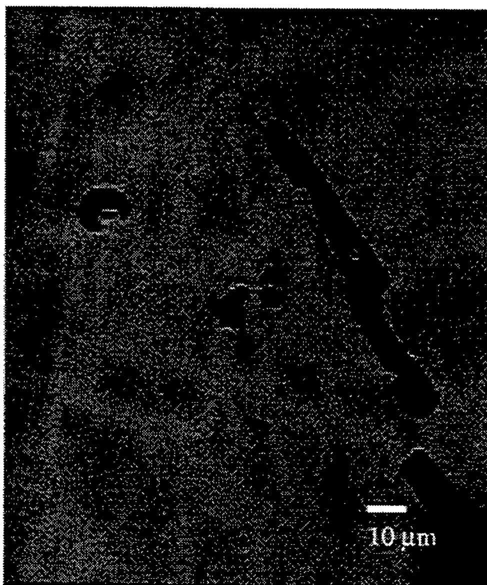

Figure 2(b). EM image of the region in Fig.(a).

Even though presently we are unable to conclude the exact type or nature of these defects, it seems definite that these defects are below the surface. This is confirmed by the fact that optical microscopy observation of the same zone did not indicate the features seen in Fig.2 (b).

4.0 Summary

Bulk defects in 6H SiC crystals have been observed using a new mode of operation of standard Scanning Electron Microscope. Using the EM technique we are able to observe structural defects in the bulk of SiC crystals not possible by normal SE imaging technique. We believe that the EM-method will be a powerful tool for studying and understanding the nature of defects present in wide bandgap semiconductors such as SiC.

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Construction of n-ZnSe-p-PbS heterostructure energy band diagram.

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Now all fields of microelectronics need new semiconductor materials and structures, and the question of fitness of some untrivial structures for device and research-device construction is important and the main attraction at its solving is spared to the problem of band discontinuities on heterointerface determination and surface electron states influence over heterostructure physical characteristics [1,2]. The heterostructures based on n-ZnSe monocrystals and p-PbS thin films grown by low-temperature MBE had been investigated from this point of view.

Recently [3] we have reported some results of electric nvestigations carried out for heterostructure n-ZnSe-p-PbS. Now we propose the band diagram constructed according Harrison-Frensley-Kroemer theory [4-5] fitting for abrupt heterojunctions. The applicability of this model is acknowledged by the results of I-V and C-V measurements (Fig.1). As the plot shows we have exponential forward current-voltage dependence $j \sim exp(eV_d/nkT)$ with sufficient values of ideality factor $n = 3.1 \div 8.0$ (Fig.1,a); the reverse I-V characteristics were linear in the temperature range 77-290 K (Fig.1, b) and C-B studies have been shown the linearity of $C^{-2}=f(V_d)$ dependence (Fig.1,c). Because the classical Anderson theory for abrupt heterostructures [6] appeared inappropriate for describing these current-voltage dependencies we have used the model [7-8]. Thus we obtained the following expressions for both forward and reverse I-V characteristics with account of the surface electron states:

$$I_f=0.25aev_{th}N_D X \exp[-(\Delta E_c+\Delta E_{ss})/2kT] \exp(eV_d/nkT), \qquad (1)$$

where a is the examined hetrerostructure electrical area, v_{th} and N_D are carrier thermal velocity and concentration in n-ZnSe substrate, X is the tunneling transparency coefficient accounting classical effects of carrier effective mass non-symmetry and their wave nature, ΔE_c is the conduction band discontinuity and ΔE_{ss} are the energy spectra of surface electron states appeared at the heterointerface (these values were calculated according [9] from the C-V measurements, ΔE_{ss}=0.22 eV),

$$I_r = I_s X V_a (\delta_1 + \delta_2 - eV_a)^2, \quad (2)$$

where I_s is a saturation current, δ_1, δ_2 are Fermi levels of the heterocomponents. The cureent mechanism realized in our eterostructure was described previously (see [1] and references elsewhere). Some parameters characterized the abrupt heterojunction n-ZnSe-p-PbS are listed in Table 1.

Table 1.

Electron surface states full charge Q_{ss}, Cl · cm^{-2}	Electron surface states density N_{ss}, eV^{-1} cm^{-2}	Space charge region width W, μm	Space charge region capacity C_{ss}, F, cm^{-2}
$2.1 \cdot 10^{-5}$	$1.3 \cdot 10^{13}$	0.11	$1.1 \cdot 10^{-8}$

From the C-V measurements we have obtained the diffusion potential V_d value of 1.7 ÷ 2.0 eV, which hadn't been explained by the classical theories as a difference of heterocomponents work functions (see Table 2): $eV_d^{theor} = \varphi_{ZnSe} - \varphi_{PbS}$ = 1.04 eV. But we have the V_d value very close to the experimental one if we'll take into account the electron surface states energy and potential barrier appeared as the conduction bands discontinuity: $eV_d = eV_d^{theor} + E_{ss} + \Delta E_c$ = 1.90 eV (Fig.2).

The band diagram constructed according our experimental results and mentioned theoretical models is plotted on Fig.2. Here $\Delta E_c = E_{g1} - E_{g2} - \Delta E_v$, ΔE_v is given by the following expression:

$$\Delta E_v = (\varepsilon_p)^{B1} - (\varepsilon_p)^{B2} + \sum_{i=1}^{2} (-1)^i [\{[(\varepsilon_p)^{Ai} - (\varepsilon_p)^{Bi}]^2 \times 0.25 +$$

$$+ (4.24\hbar^2 / a_i^2\}^{1/2} - \{(\varepsilon_p)^{Ai} - (\varepsilon_p)^{Bi}\} / 2 \pm (\varepsilon_0 a_{a1})^{-1} \Sigma q_i^* \pm E_{ss} \pm$$

$$\pm (kT/e) \ln[v_{th} (\tau / D)^{1/2} \delta \Delta a / a^3] \,. \quad (3)$$

where $(\varepsilon_p)^{Ai}$, $(\varepsilon_p)^{Bi}$ are atomic orbital energies of heterocomponents of II and VI groups, q^* are their effective charges [8], D, τ, σ are diffusion coefficient, carrier lifetime and recombination cross-section in the wide-gap substrate (see Tables 2,3). $\Delta a = |a_1 - a_2|$, $a = 0.5(a_1 + a_2)$, a_i $(i = 1,2)$ are lattice constants of PbS and ZnSe.

Table 2.
Parameters used for n-ZnSe-p-PbS heterostructure energy band diagram construction.

	Material	
Parameter	ZnSe	PbS
Lattis comstant a, Å	5.6887	5.9427
Band gap E_g, eV	2.72	0.41
Thermodynamic work function φ, eV	4.84	3.80
m_e/m_0	0.17	0.105
m_h/m_0	0.60	0.105
D, $cm^2 s^{-1}$	15.0	
τ, s	$\sim 10^{-5}$	
σ, cm^2	$\sim 10^{18}$	
N_D, cm^{-3}	$(3.0\div28)\times10^{16}$	

Table 3.
Atomic orbital energes and effektive charge of II-VI elements

Element	$-\varepsilon_{ps}$ eV	q^*, e_0 units
Zn	3.38	0.79
Se	9.53	1.30
S	10.27	1.40

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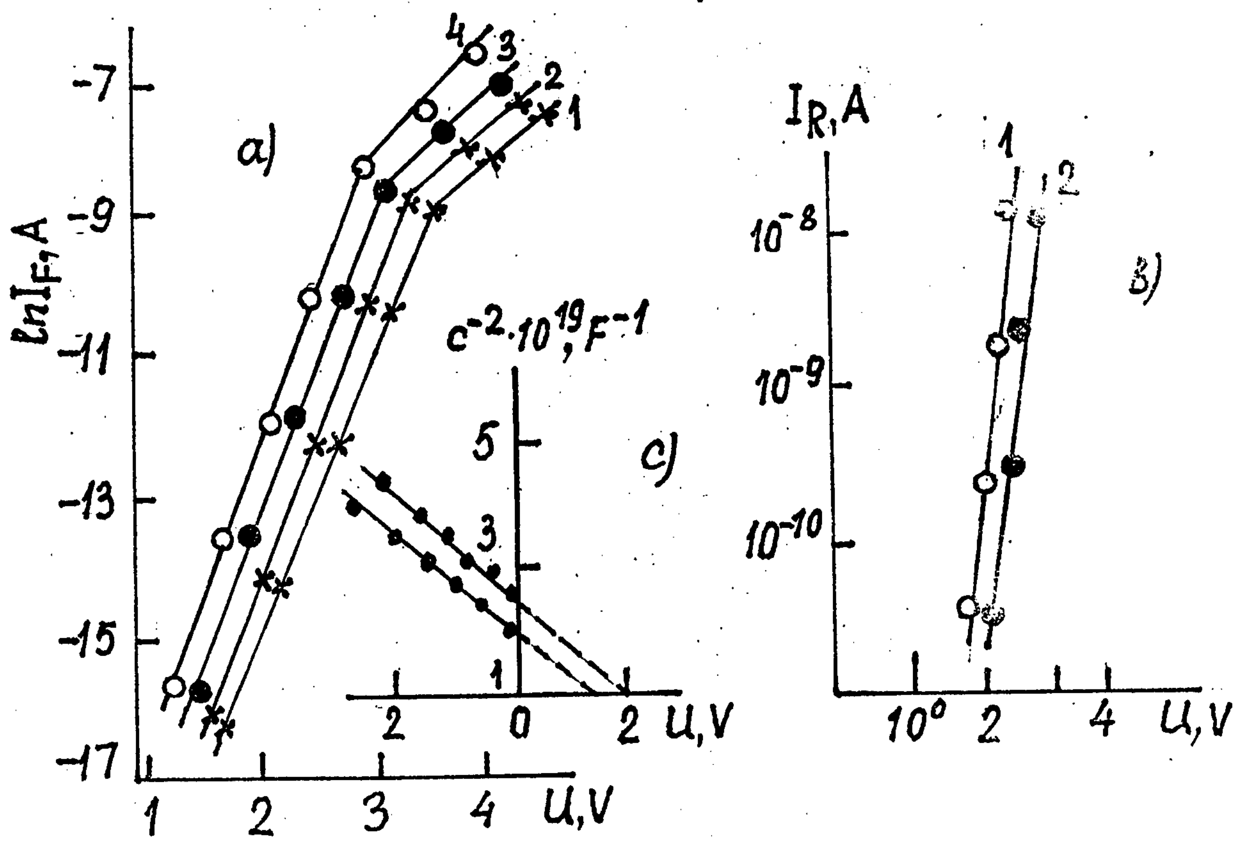

Fig.1. I-V characteristics of n-ZnSe-p-PbS heterostructure.
a)Forward current-voltage dependence; T, K: 1 - 77, 2 - 125, 3 - 205, 4 - 290;
b) reverse I-V characteristics: T, K: 1 - 77, 2 - 290;
c) C-U dependence, f = 1.0 MHz, T, K: 1 - 77, 2 - 290.

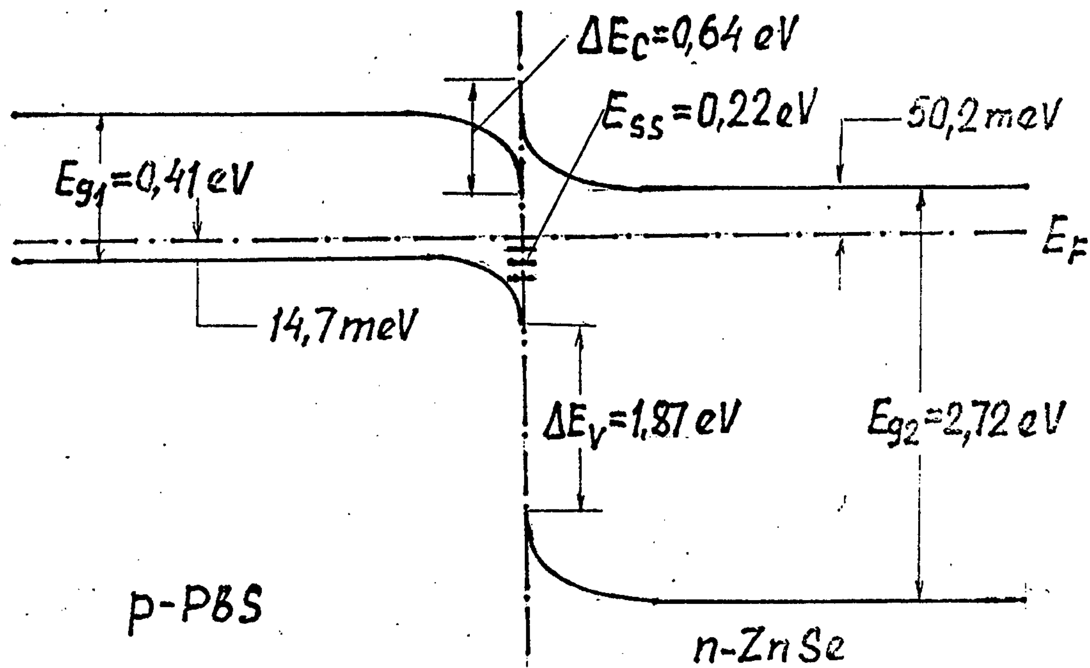

Fig.2. Equilibrium energy band diagram of the examined heterostructure, T = 290 K.

Surface Morphology and Crystallographic Tilt of InAs Epilayers Grown on GaAs Substrates by MBE

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1.0 Intruduction

As the epitaxy technology developed, strained material system has attracted much interesting because of its wide applications but not presently well understood due to the complex relaxation. The growth of InAs on lattice mismatched substrates such as GaAs and Si has received particular attention due to its potential applications[1-4]. Recently, InAs thin films were considered to produce Hall elements and the researchers made great progress[5,6]. The electrical characteristics of InAs thin films show a great difference from the bulk crystal which makes InAs films one kind of promising materials for magnetic sensors because of its larger band gap than InSb and higher electron mobility than GaAs.

In this paper, we have investigated both crystal quality and electrical characteristic of InAs epilayers grown on GaAs substrates by molecular beam epitaxy (MBE).

2.0 Experiments

All the samples were grown on Riber 32P MBE system. Substrates were exactly (001) oriented semi-insulating GaAs. Samples with different thickness were grown at 480 or 450°C. Si was selected as n-type dopant. Growth started under a (2×4) reconstruction GaAs surface examined by RHEED. The streaky pattern turned to spotty at beginning of the growth which was due to the transition from 2D growth mode to 3D growth. The samples were measured by scanning electron microscopy (SEM), Hall measurement and double crystal X-ray diffraction (DCXD).

3.0 Results and discussion

3.1 Surface morphology

Measured by SEM, all the samples grown at 450°C have a rough surface with a relative high density of regular pits while the surface of samples grown at 480° C are smooth. The shape of the pits is hexagonal with a long axis along $[1\bar{1}0]$ direction.

The formation of these pits was considered

a result of strain relaxation and insufficient migration of adatoms on the surface. When InAs grown on GaAs substrate, the lattice mismatch favors the island formation to lower the system energy at first. Then, misfit dislocations create at the islands edge also to relax the strains. In zinc-blende structure, the majority of misfit dislocations, 60° -type dislocations, have a component of screw dislocation which may cause spiral growth when group III adatoms attach to the submonolayer step associated with dislocations[7]. On the other hand, MBE growth is a kinetically limited process and usually achieved through surface migration of newly arrived atoms to the energetically more favorable sites[8]. The morphology of the film surface is thus sensitive to the substrate temperature. Lower temperature offers group III adatoms less energy to motivate and result in a shorter diffusion length of adatoms on the surface. If the adatoms could not combine to a suitable position, the surface can hardly recover to smooth after the islands form.

3.2 Mobility

The electron mobility were measured by van der Pauw method from 72 to 424K. The results are shown in Fig 1. The variation of electron mobility can be explained by parallel conduction theory which considered three spatial regions, surface space-charge layer, bulk region and interface region, contributed to the electrical conduction mechanism in the InAs layers[4].As the thickness increases, the contribution from the bulk region plays a more important role and the electron mobility increases. It is also found that the inferior surface affected the Hall mobility greatly. Another trend of mobility is a dependence on doping level. Sufficient doping level would improve the mobility and its temperature dependence[5]. As measured by TEM, most misfit and threading dislocations tangled within 0.2μm from the InAs/GaAs interface[9]. Therefore, doping Si was started at 0.2μm from the interface in order to minimize

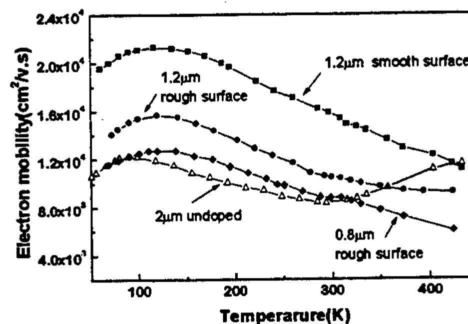


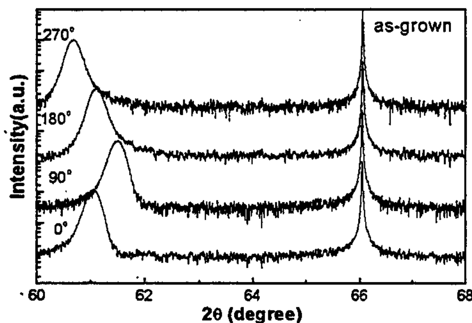
Figure 1. Temperature dependence of electron mobility

the possible effects of misfit and threading dislocations around the interface.

3.3 Crystallographic tilt

The tilt of InAs epilayers with respect to GaAs substrates has been measured by DXCD under ω-2θ mode. The (004) diffraction curves were recorded at four

azimuthal angles in increments from 0°~270° in order to obtain an accurate measure of the tilt. The results of a as-grown sample were shown in Fig.2. A significant tilt, 0.418°, between epitaxy and substrate was observed along one of the two <110> directions.



Figrue 2. DCXD patterns obtained from (004) planes of a as-grown sample

The phenomenon of tilt between epilayer and substrate with misfit has been studied in lattice mismatched systems usually when a miscut substrate is used. The tilt is considered to originate from a combination of two principal effects, geometrical effect of surface steps on offcut substrate and asymmetrical plastic deformation[10]. As the substrates without miscut angle were used in our experiments, the formation of tilt was mainly due to the asymmetrical distribution of misfit dislocations. There exist such a high lattice mismatch between InAs and GaAs that almost all the misfit strains are relieved by misfit dislocations after the InAs layer reaches a certain thickness. The parallel component of 60°-type misfit dislocation is responsible for strain relaxation and the perpendicular component of Burgers vector gives rise to a pure crystallographic tilt[11]. The

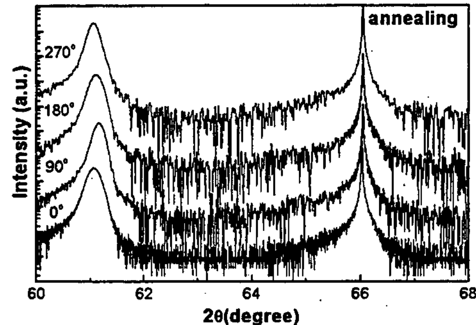


Figure 3. DCXD patterns of the same sample after annealing

anisotropy of the tilt is likely due to the asymmetric distribution of 60°-type dislocations along (110) and $(1\bar{1}0)$ directions which are nonequivalent in zinc-blende lattice.

After rapid thermal annealing at 600°C for 2 minutes under As overpressure, the tilt decreased to 0.047°. as shown in Fig.3. The FWHM of InAs peak rocking curve also decreased from 623 arcsec to 432 arcsec while the peak intensity increased. The variation suggested that *ex su* annealing is effective in reducing the density of structural defects. Durng annealing, misfit and threading dislocations glided and interacted with each other. Some dislocations with opposite Burgers vectors annihilated and the asymmetrical distribution of dislocations was changed. Therefore, the magnitude of the tilt and the FWHM of InAs peak both decreased. The efficiency of annealing has been

demonstrated in other lattice mismatched systems, such as GaAs on Si, by TEM[12].

4.0 Conclusion

The surface morphology of InAs epilayers grown on GaAs by MBE was greatly influenced by growth temperature. The difference of morphology results from different migration of cations which is temperature dependent. The inferior surface decreases the Hall mobility significantly. Samples had a tilt between the substrate and epilayer which was decreased after *ex situ* annealing. The tilt was originated from the asymmetrical distribution of the 60°-type misfit dislocations which was changed during annealing. The improvement of crystal quality after annealing was also demonstrated by the decrease of FWHM of InAs peak.

5.0 References

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Schottky Barrier Height Engineering for Millimeter—Wave Diodes

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I. Introduction

Schottky barrier is the key element in a variety of devices, specifically, detector and mixer diodes for the millimeter—and submillimeter—wave range [1]. In some problems it is required that the barrier height be reduced to achieve, for example, a lower LO power in mixing or a lower noise level in detecting processes [2,3]. As a rule, the Schottky barrier height for III—V semiconductor material is practically independent of the selected metal [4]; therefore, to reduce the effective height of the barrier one needs to use heterostructures with the narrow—band intermediate layers [2], or to subject the surface area of a semiconductor to specific doping processing [3,4].

The present paper reports a study of a possibility to control the effective height of a barrier by precise δ—doping of a GaAs surface layers and successive deposition of an Al layer from trimethylaminealane directly in the MOCVD reactor (*in situ*). The proposed method allows to make reproducible Schottky contacts Al/n—GaAs with a 0.75—0.1 eV effective barrier height and ohmic contacts with a low resistance $<10^{-5}$ Ohm·cm^2 in case of a heavily doped surface. An option for engineering millimeter—wave planar diodes with Schottky barrier on the basis of the obtained structures is proposed.

II. Experimental work

The GaAs epitaxial layers and Al films were produced in a horizontal MOCVD reactor. For growth were used heavily n—doped GaAs substrates oriented 2° off (100). The growth temperature for GaAs films was varied in the 600—650C range. The growth chamber pressure was normally maintained at 50—100 mbar. The group V source was arsine (10% in hydrogen) and the group III sourse was trimethylgallium. The n—type dopant was silane (100 ppm in H_2). The growth interruption step was used for each δ—doping layer.

Al films normally of 0.15—0.35 μm thickness were deposited in the same reactor without breaking growth condition from trimethylaminealane at T=160—200C and a 50—100 mbar pressure .The Al deposition rate was about 1 μm/h. According to the X—ray fluorescence and Auger analyses data, the Al films were free from impurity within sensitivity of the methods used. The electron microscopy revealed an island structure of the Al layers with blocks of 1—4 μm in size. The X—ray diffraction analysis has exposed Al films as a mixed structure with the [100] and [111] orientations of Al blocks. Specific resistance of 0.3 μm thick Al layers was 6—8 μOhm cm, which is 2—3 times worse than in pure bulk Al.

III. Results and discussion

In order to test the current–transport mechanisms, a set of structures was prepared (see the Table). For the current– voltage characterisations simple mesa–structures with a diameter in a 25–500 μm range were fabricated with a photolithography and wet ething. When Al films were deposited on a uniformly n–doped (~10^{17} cm^{-3}) GaAs layer, the usual J/V Schottky diode characteristics were reproducibly obtained. Diodes have the barrier height φ_B=0,75 eV and the ideality factor n≈1.02–1.06. When the surface δ–layers had been built in at 2 nm off the Al–GaAs interface, the tunneling–transparent spike was formed for electrons. In this case the band diagram of the structure looks as shown in Fig.1 The potential drop from the interface towards the δ–layer is determined by the surface concentration of donors N_D^{2D}. A decrease in the effective height of the Schottky barrier can be estimated as

$$\Delta\varphi \approx q\cdot N_D^{2D}\cdot z / \varepsilon\varepsilon_0, \quad (1)$$

where q is the electron charge, ε_0 and ε are the dielectric constants. It is obvious that to provide high tunneling rate through the spike of the potential barrier, the distance z must not exceed the value of several characteristic lengths of decay of the wave function λ. in the barrier [5]:

$$\lambda \approx \hbar/(4qm*\Delta\varphi)^{1/2} \quad (2)$$

where $\hbar$ is the Planck constant, m^* the effective electron mass in the conduction band. Accordingly, z must be not more than several nanometers. The J/V characteristics can be calculated in the usual manner [5]. First approximation for the tunneling probability gives a simple J/V relation

$$j = AT^2\cdot(\exp(eV/kT)-1)\cdot\exp(-e\Delta(V)/kT) \quad (3)$$

where

$$A = 4\pi\cdot e\cdot m*k^2\cdot f/(2\pi\hbar)^3 \quad (4)$$

is the modified Richardson constant with the coefficient f<<1. Weak dependence of f and the effective barrier height Δ on a voltage determines the value of the ideality factor.

Experimental observations confirm, in general, these simple theoretical evaluations. Since it is difficult to increase N_D^{2D}> 6x10^{12} cm^{-2} due to a self–compensation phenomenon [6], the effective height of the barrier can be largely reduced by building in a sequence of δ–layers spaced at a nanometer from each other. The parameters of the investigated structures and the obtained results are presented in the Table.

Table. Parameters of the Al/n–GaAs diodes with surface δ–layers.

Sample number	Number of δ–layers	Separation between δ–layers, nm	N_D^{2D} of one δ–layer, cm^{-2}	Effective height of barrier, eV	Ideality factor
1	–	–	–	0.75	1.02÷1.06
2	1	2	2x10^{12}	0.68÷0.7	1.04÷1.06
3	3	2	2x10^{12}	0.53÷0.57	1.1÷1.2
4	3	2	5x10^{12}	0.25÷0.3	1.2÷1.3
5	3	2	7x10^{12}	ohmic contact ρ_c~10^{-5} Ohm cm^{-2}	–

Experimental I/V characteristics are shown in fig.2. In the limit $N_D^{2D}=7x10\ cm^{-2}$ we have obtained the ohmic I–V curves with a rather low contact resistance.

The planar diodes formed on these structures are essentially an upgraded design of a beam lead planar diode 3A147 that has shown a good performance at Thz frequencies [7]. Besides the differences in topology, provisions were made in the new device design to reduce the spreading resistances at high frequencies. In particular, the computation methods [8,9] as applied to this case have shown that the 2–3 μm gap between the Shottky barrier edge and the planar ohmic contact has to be avoided. So, self–aligned technology in the ohmic contact formation and the increased anode contact perimeter to 5 μm reduce series resistance. Higher capacitance in this case is compensated by formation of mesa–structure. The cross–section of the diode across the anode finger is shown shematically in Fig.3. A part of the metal– coated area of the cathode is formed as a barrier contact from the same material as the anode. According to our data, this provides a reduction of the diode total impedance at frequences above 1 THz. The characterisation of an advanced version of the diodes with a micrometer size of the anode will be presented.

VI. Conclusion

A possibility of the fabrication of Al/n–GaAs barrier contact based on MOCVD non–interrupted process is demonstrated. The effective Shottky barrier height can be varied in the range 0.75–0.1 eV by appropriate δ–doping of a surface layer. Transport processes are discussed, comparision with the experimental data is presented. The developed planar millimeter–wave diodes based on structures with the reduced barrier height are estimated.

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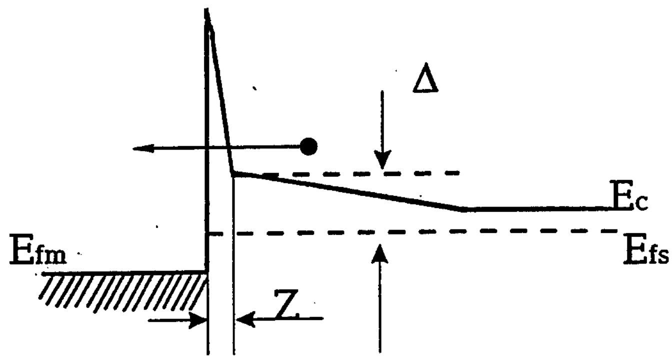

Fig. 1

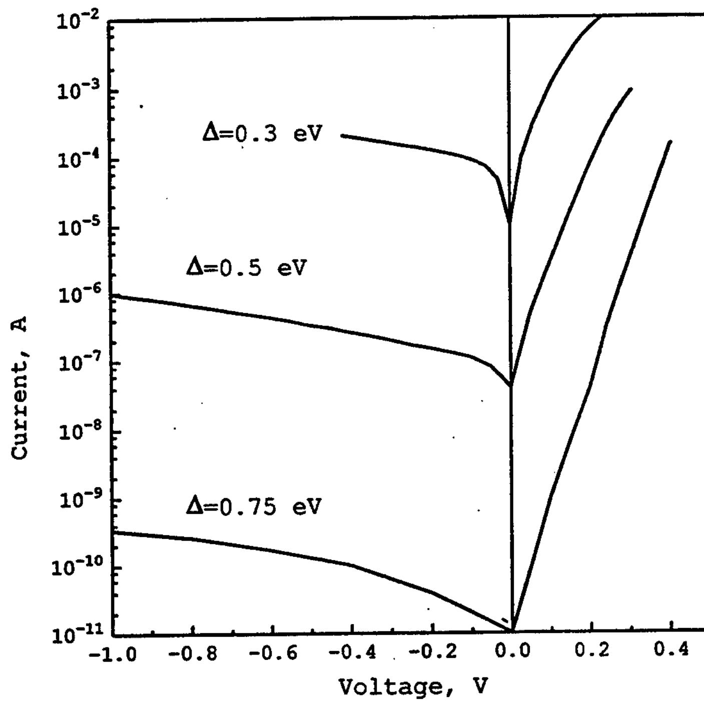

Fig. 2

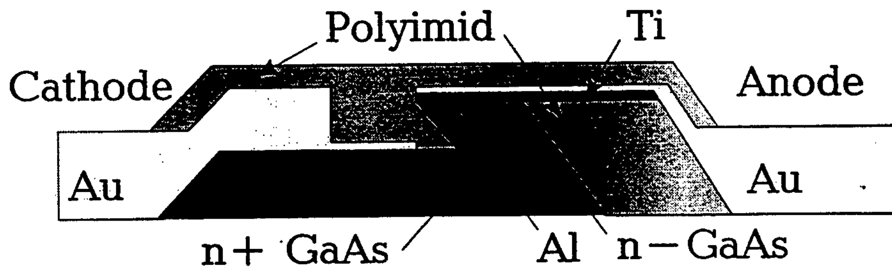

Fig. 3

Multi-Channel 2-D MESFET for Microwave Applications

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I. INTRODUCTION

Integrated circuits designed to operate in the microwave and millimeter-wave regions are in increasing demand for wireless and fiber-optic communications applications. GaAs and InP-based Field Effect Transistors (FETs) and Heterojunction Bipolar Transistors (HBTs) technologies have a clear performance advantage over other technologies (e.g. silicon) and significant progress is evident in improving the reliability and cost of these technologies. As compound semiconductor ICs become more mainstream, power consumption becomes a limitation. Thus, novel approaches will be necessary to combine the high speed performance of III-V technologies with ultra low power consumption of novel structures. One such structure, called the Striped-Channel HEMT [1, 2], attempts to leverage superior electron confinement of charge carriers in quasi-one-dimensional channels using a conventional high speed 2-d electron gas heterostructure system. As an extension of this idea, we propose to utilize so-called heterodimensional (e.g. 3-d metal/2-d electron gas) junctions in a striped-channel configuration. As in the single-channel 2-D MESFET [3, 4], the multi-channel 2-D MESFET gate metal directly contacts the 2-d electron gas and modulates the drain current. The multi-channel device should have an improved impedance match to microwave circuits while maintaining superior electron confinement exhibited by single-channel devices.

The 2-D MESFET gate metal directly contacts the edge of the 2-dimensional electron gas (2-DEG), as shown in Fig. 1. The resulting 3-d (metal)/2-d (2-DEG) junction, called a heterodimensional junction, has unique features including 2-dimensional spreading of the electric field in the depletion region, a low junction capacitance, high breakdown voltage and nearly linear depletion depth versus voltage characteristics [5]. The high degeneracy of the 2-d electron gas is responsible for much weaker temperature dependence of the threshold voltage [6] and lower 1/f noise [7]. A similar structure has demonstrated excellent quantized conductance properties at cryogenic temperatures [8]. For microwave applications, however, much higher current levels are required compared to those attained in single-channel 2-D MESFETs. To this end, we have fabricated multi-channel 2-D MESFET devices having many sub-micron wide channels connected in parallel. This paper discusses the fabrication and electrical characteristics of these devices.

II. DEVICE DESIGN AND FABRICATION

The multi-channel 2-D MESFET was implemented in a common source configuration suitable for coplanar wave analysis at microwave frequencies, as illustrated in Fig. 1(a). The prototype devices used 24 channels on either side of the gate feed (48 channels total), where both the gate and channel regions were square with 0.5 μm by 0.5 μm dimensions. Thus, the total channel width was approximately 24 μm. The individual gate "islands" were strapped together

with an overlay metal so that all gates were biased in common, as shown in Fig. 1(b). Note that in the 2-D MESFET, the gates modulate the width of the 2-DEG channel, analogous to that which occurs in the conventional MESFET (wherein the gate modulates the channel from above). Thus, the charge control in the 2-D MESFET is different from that in either the conventional MESFET or the Heterostructure Field Effect Transistor (HFET).

Devices were fabricated on a typical double δ-doped pseudomorphic $Al_{.24}Ga_{.76}As/In_{.18}Ga_{.82}As$ heterostructure having a 300 K electron mobility μ_n and sheet density n_s of about 6000 cm^2/V-s and 2.9 x 10^{12} cm^{-2}, respectively. Gate processing was performed using electron beam lithography, chemically assisted ion beam etching (to etch through the 2-DEG layer) and Pt/Au electroplating to form the heterodimensional Schottky/2-DEG contacts. The remaining process levels including Ni/Ge/Au ohmic contacts and Cr/Au interconnect metallizations defined using contact UV lithography. Further fabrication details can be found in [3, 4].

III. DC AND RF CHARACTERISTICS

The drain current versus drain-source voltage characteristics I_d - V_{ds} are plotted in Fig. 2. The gate voltage was varied over the range -4.0 < V_g < 0.0 V (1.0 V step). The drain current saturates at about 9.5 mA at V_{ds} = 1.0 V. This corresponds to a unit width current density of about 400 mA/mm and 100 ohm total series resistance (this compares with 210 mA/mm and 3800 ohms for the single channel device in [3]). The threshold voltage was about -4.2 V and the forward saturation voltage was about 0.7 V. The output conductance, g_{ds} at V_{ds} = 2V was only 0.05 mS (2.1 mS/mm). The transconductance, g_m is shown in Fig. 3 together with that for a conventional 1 micron long PHEMT fabricated on the same material. The multi-channel device transconductance was broad and peaked at 3 mS (125 mS/mm) at V_g = 0 V . This yields a peak dc voltage gain g_m / g_{ds} of 60 which is higher than that reported in [1], due primarily to the low output conductance. The present devices exhibited an ON/OFF current ratio of about 10^4 and a drain-gate breakdown voltage of 7 V, illustrating the robustness of the heterodimensional junction. The leakage current I_{leak} was nearly 1 uA, compared to I_{leak} as low as 10^{-11}A in single channel 2-D MESFET devices (the reason for the higher leakage in these prototype multi-channel device is not yet clear). The nearly flat transconductance characteristic (i.e. small transconductance compression) observed in Fig. 3. may be due to a smaller dependence of the gate-channel capacitance on gate voltage and to the elimination of the parasitic MESFET effect. The high series resistance in these prototype devices can be reduced ten-fold by reducing the source-drain separation (factor of 2), increasing the gate width (factor of 4) and by increasing the 2-d electron gas conductivity (by 25 %). Self-aligned ion-implanted source-drain regions would also lead to lower series resistance.

The S-parameters were measured using an HP 8510C network analyzer up to 50 GHz. A conventional microwave small signal circuit model was used for parameter extraction and de-embedding. The extracted parameters were relatively constant over the frequency range of interest and in good agreement with those values obtained at dc. The gain-frequency characteristics are shown in Figs. 4 and 5. The f_T was 14 GHz and f_{max} was 45 GHz. We believe that in the present structure the parasitic capacitances between the gates and the source and drain limit the cutoff frequency. By reducing the gate periphery facing the source and drain, the frequency response could be significantly improved. The parasitic gate resistance can be reduced by using a conventional T-gate, thereby improving the performance further.

IV. SUMMARY

We have fabricated prototype 2-D MESFETs suitable for microwave characterization. The 2-D MESFET utilizes a lateral Schottky/2-DEG gate junction, which we call heterodimensional junction. Devices having 48 0.5 x 0.5 μm channels (24 μm total width) were fabricated on a pseudomorphic AlGaAs/InGaAs heterostructure. Peak dc current of 9.5 mA (400 mA/mm) and transconductance of 3 mS (125 mS/mm) were obtained. The dc voltage gain was as high as 60 due primarily to a low output conductance. Cutoff frequencies, f_T and f_{max} of 14 GHz and 45 GHz, respectively, were obtained in unoptimized devices. These first results suggest that the 2-D MESFET may have microwave applications.

ACKNOWLEDGEMENTS

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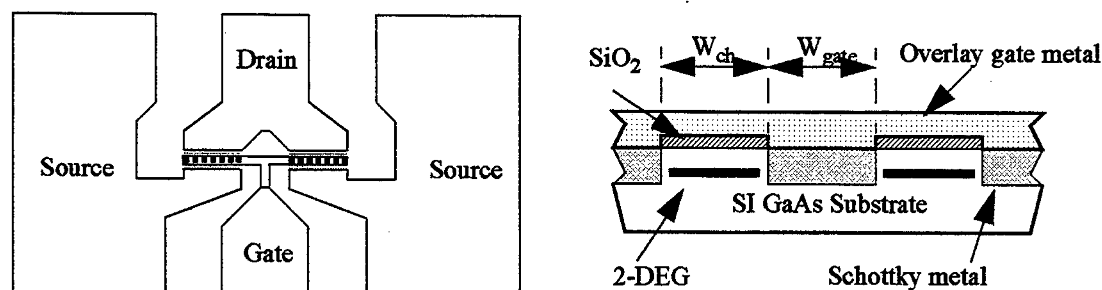


Fig. 1. Perspective views of multi-channel, microwave 2-D MESFET. Top-view (left) shows the co-planar layout with 24 channels on either side of the gate feed. Gate-channel cross-sectional view (right) illustrates the lateral modulation of Schottky/2-DEG junction.

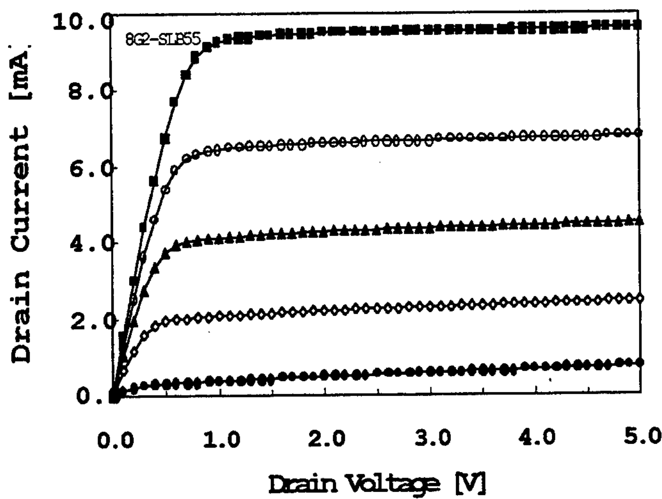


Fig. 2. I_D vs V_{DS} charcteristics of 48 channel 2-D MESFET (0.5 um wide channels) at room temp.

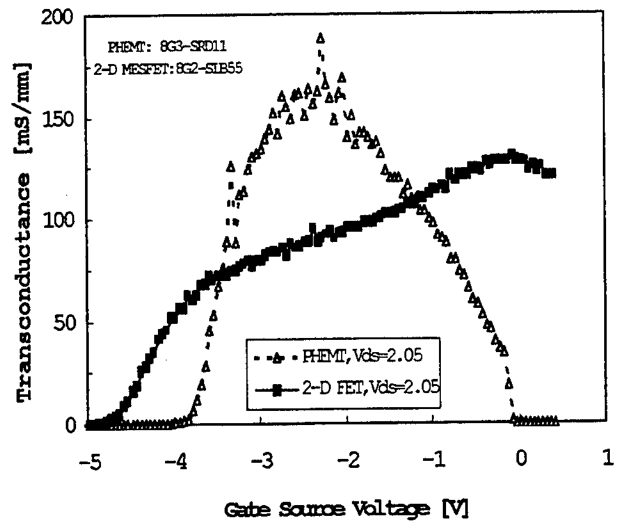


Fig. 3. Transconductance of 2-D MESFET and conventional HFET fabricated on the same wafer..

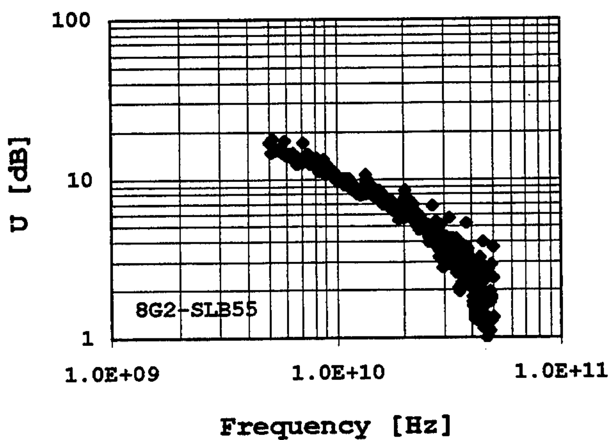


Fig. 4 High frequency characteristics of prototype 2-D MESFET having f_T of 14 GHz.

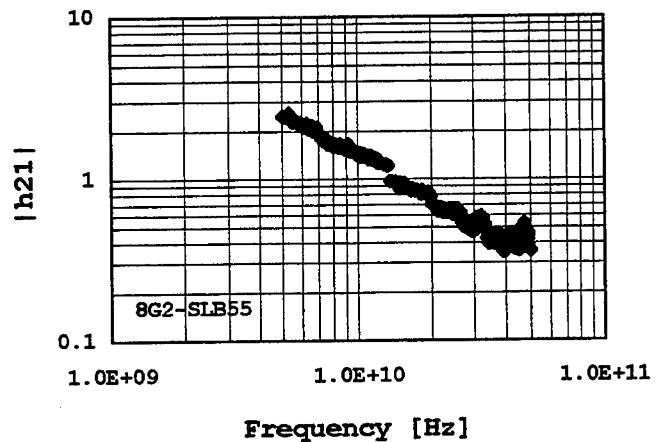
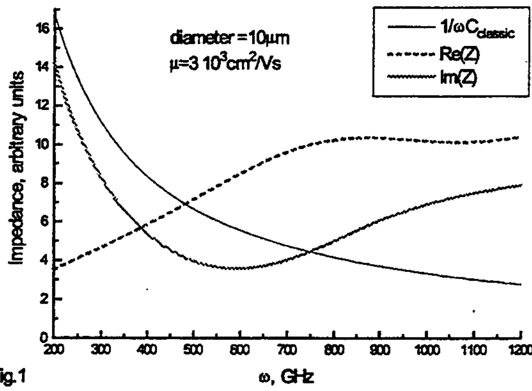
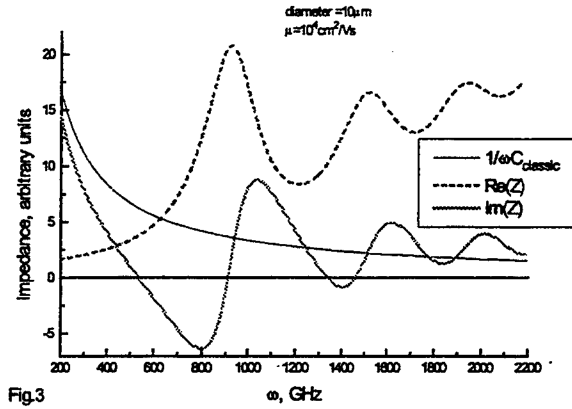
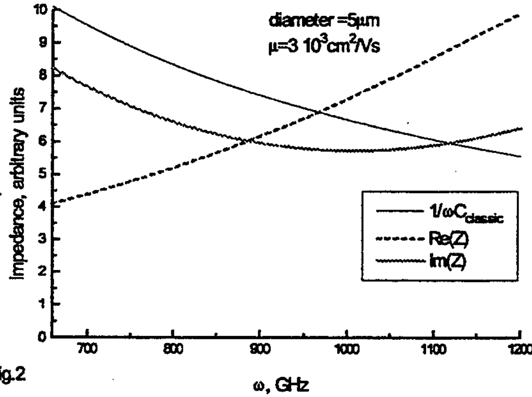


Fig. 5. High frequency characteristics of prototype 2-D MESFET having f_{max} of 45 GHz.







Figs. 1-3. The dependencies of the junction impedance per unity of y-length at frequency. The thin solid lines are the structure impedances calculated for comparison in the framework of the model that does not take into account JPPs excitation. Figs.1-3 present the plots of the impedance of the semiconductor – barrier – semiconductor structures with the following parameters: the lattice dielectric constants of the semiconductor and barrier are supposed to be the same and equal to 13.5; the electron effective mass is $m^* = 0.07m$, the electron concentration in the semiconductor is $10^{18} cm^{-3}$, the thickness of the barrier is $50nm$, the diameters of the structures and the electron mobilities are shown in the figures. The frequency range in the Figs.1-3 corresponds to that where our approach is applicable and the excitation of JPPs essentially changes the impedance.

– semiconductor ($2W \times \infty \times L$) – metal ($z \geq L$). ∞ in y direction does not lead to strong limitation of the obtained results, since they will remain qualitatively the same in the case of cylindrical geometry, and the resonance frequencies, for example, will differ quantitatively from the calculated ones on a factor of the order of unity. All values discussed below (impedance, current) are for the unity of length in y direction. We consider a case of strong skin effect, i.e. the skin layer thickness l_s equaled to $l_s \approx c^*/\omega_p$, if $\omega >> \nu$, or $(c^*/\omega_p)\sqrt{\nu/\omega}$ if $\omega << \nu$, is small in comparison with the semiconductor region dimensions W, L. In this case, the total impedance per unity of length in y direction of the structure could be splited into two parts: $Z = Z_s + Z_j$, where Z_s corresponds to the skin layer impedance of the lateral surface and Z_j corresponds to "junction impedance". Z_s is defined by the well-known expression:

$$Z_s = \frac{4\pi i \kappa_s L}{\omega \varepsilon_s}, \tag{3}$$

where $\kappa_s^2 = -\varepsilon_s \omega^2/c^2$. Z_j is determined by the JPP mode excitation. We define Z_j as the ratio of the voltage drop on the barrier near lateral surface ($x = \pm W$) and the current incoming in JPP. Our calculation shows that the junction impedance per unity of length in y-direction equals to:

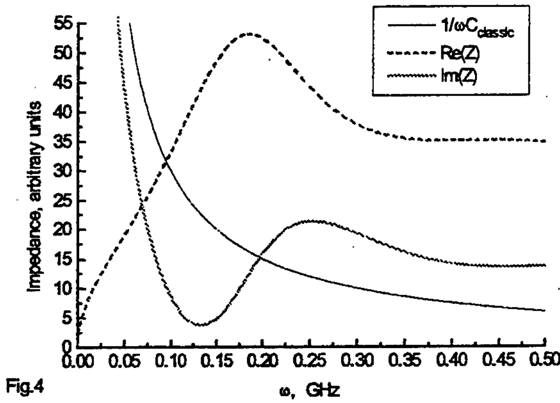
$$Z_j = \frac{i}{C(\omega + i\nu_T)} \frac{qW}{\tan(qW)}, \tag{4}$$

here q is the complex value of JPP wavevector, which is defined by Eq. (1) with a real value of ω. In the low-frequency limit (when $|qW| << 1$) Eq. (4) goes over into ordinary expression for the junction impedance: $Z_j = i/C(\omega + i\nu_T)$. It can be represented as the parallel connection of the capacitance C and the tunnel resistance $R_T = 1/G$.

In high-frequency limit, i.e. $|qW| > 1$, Z_j has a multiresonance character, even when tunnel transparency of the barrier is equal to zero (see Figs.1-4). It can be seen from Figs.1,3,4 that Z_j has peculiarities of the following two types. The first ones correspond to $|Z_j|$ resonance and the second ones correspond to $|Z_j|$ minimum ($|Z_j^{-1}|$-resonance).

As the analysis of Eq. (4) shows, $|Z_j|$ has maxima when $qW = \pi N$ (where $N = 1, 2...$). The structure width is JPP wavelength multiple in this case and the charge distribution has maxima at $x = \pm W$ on the semiconductor surface. Consequently, the voltage drop has maxima at $x = \pm W$ on the barrier lateral surface also. In view of the fact that the structure width is JPP wavelength multiple, JPP oscillation practically does not need incoming current from the external circuit (if JPP attenuation is small). So the structure impedance has maximum in this case.

In the second case, when the structure width is a JPP wavelength half-integer number multiple, the induced



The junction impedance per unity of y-length of the metal – barrier – metal structure with the following parameters: the barrier thickness is $100nm$, the lattice dielectric constants of the metal and barrier are equal to 3, the electron concentration in the metal is $6 \cdot 10^{22}cm^{-3}$, the electron mobility is $\mu = 50cm^2/Vs$, the diameter of the structure is $10cm$. The structure suits to low-frequency experimental study of JPP excitation.

charge near the semiconductor corners at $x = \pm W$, $y = \pm d/2$ has approximately zero value and, as a consequence, voltage drop on the barrier lateral surface is small. So it is necessary to have a significant value of the charge (JPP amplitude) to maintain the voltage, applied by the external circuit, on the junction. Taking into consideration that the structure width is a JPP-wavelength half-integer-number multiple, the charge can be supplied only from the external circuit, i.e. external circuit current is significant and $|Z_j|$ is small.

The resonance-like behavior could be seen for the ordinary $GaAs$-type structure (see Fig.1) with the following parameters: $n = 10^{18}cm^{-3}$, mobility $\mu = 3 * 10^3cm^2/Vs$, $m^* = 0.07m$, $d = 50nm$, $\varepsilon_l = 13.5$, $2W = 10\mu m$. It should be noted that Z_j has unusual asymptotic behavior in the high frequency limit ($\omega >> \nu$): $Z_j = 8\pi(\omega + i\nu)/\omega_p^2$. It is worth reminding that we have in this limit:

$$Z_s = -i8\pi \frac{\omega + i\nu/2}{\omega_p^2} \frac{L}{2\varepsilon_l l_s} \approx -i \frac{L}{2\varepsilon_l l_s} Z_j. \qquad (5)$$

That is $Z_s \ll Z_j$, when $L \sim l_s$ (Z_j, substantiated by JPP, determines the total impedance of the structure!).

The resonances are much better in a high mobility structure $\mu = 10^4cm^2/Vs$ (see Fig.3). In this case the resonances are at the frequencies higher than ν, that is why they are rather sharp. The condition $\omega_{res} > \nu$ imposes strong limitations on the semiconductor parameters. The presence of the positive differential tunnel conductivity worsens the impedance resonance properties, i.e. the resonance is broadened. The presence of the negative differential conductance (NDC) leads to the resonance improvement, the resonances become more narrow. When NDC is sufficiently high, the resonances become self-exciting (i.e. the external circuit current, or the voltage at the structure, or both build up spontaneously).

We propose a metal – barrier – metal structure that could be used for the experimental study of the JPPs in the low-frequency range. The corresponding plots are shown in Fig.4. Here, JPPs determine the impedance of the structure at the frequencies higher than 50MHz.

IV. Conclusions

The analytical expression for JPP spectrum was derived, it is allowing for tunnel conduction and electromagnetic retardation in the hydrodynamic approximation. The impedance of the metal – semiconductor – tunnel barrier – semiconductor – metal structure with finite dimensions was considered in the strong skin effect limit. We have shown that THz impedance of semiconductor diodes with the diameter of several μm changes strongly both qualitatively and quantitatively. We showed that AC impedance of a high electron mobility structure has a multi-resonance behavior. This is due to excitation of JPP modes. The effect potentially has some practical applications. It might be used for microwave filter (when JPP excitations are stabile). Probably this effect might be used for microwave oscillator, based on the resonant tunneling structure itself (without external elements, such as resonance circuit).

V. Acknowledgments

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THz Impedance of Tunnel Diodes: Skin Effect Influence

Michael Feiginov, Vladimir Volkov

Abstract— **We have considered the dynamic response of the semiconductor – tunnel barrier – semiconductor and metal – tunnel barrier – metal structures in the skin effect regime. The tunnel barrier may contain one or more layers. We have shown that a peculiar slow low-frequency plasma waves (plasma junction polaritons – JPP) are excited in the case. As a result, small-signal impedance of the junction and its frequency dispersion qualitatively change. An analytical expression for the impedance is obtained. In the typical GaAs resonant tunneling diode with the diameter equal to 5μm (10μm) the effect at room temperature is to be essential when the frequency is higher than 700 GHz (200GHz).**

I. Introduction

There are several factors limiting the high-frequency operation of the tunnel devices, in particular resonant tunneling diodes (RTDs). As a rule, RC time is thought to be the major limiting factor. But there are peculiar low-frequency plasma excitations that are in the tunnel device itself, which effect on AC impedance was not studied up to date. We have shown that the excitations appear in the skin effect regime and substantially affect the impedance.

We have considered the AC response of a tunnel diode with the finite diameter in the skin effect regime. The tunnel barrier could be one-layer or more layer one. The restriction of applicability of our model is that the total thickness of the barrier is to be small and the total thickness of the semiconductor regions are to be large in comparison with that of the skin-layer in the semiconductor at the frequency of interest. That is our approach is applicable to RTD.

We have shown that a specific plasma waves – junction plasma polaritons (JPPs) – exist close to the barrier. JPPs are characterized by a low speed of propagation along the barrier in comparison with that of the light in the material of the barrier. In other words, it is a low-frequency excitation, that is, for a given wavelength it oscillates with a frequency low in comparison with that of the light with the same wavelength.

We have shown that for a typical parameters of the semiconductor structures under consideration, the high-frequency response is determined by the excitation of JPPs by the inhomogeneous current of the skin-layer at the frequencies higher than 200GHz. The corresponding analytical expression for the impedance was derived. The dependence of the impedance is both qualitatively and quantitatively differs from that predicted by the models which do not take into account JPP excitation.

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II. The spectrum of junction plasma polaritons

We consider a semiconductor – tunnel barrier – semiconductor structure. The semiconductor layers are assumed to be of the same material and infinitely thick. The structure is infinitely large in the junction plane. To simplify this rather complex problem we describe the behavior of electrons in the semiconductor layers in the hydrodynamic approximation. The corresponding equation for the spectrum of antisymmetric (with respect to charge densities, induced in the semiconductor regions) low-frequency mode of plasma excitations (JPPs) has the following form:

$$(\omega+i\nu)(\omega+i\nu_T)\kappa=\omega_p^2\frac{d^*}{2}\times$$

$$\times\left(\kappa^2-\frac{\omega_p^2}{c^{*2}}\frac{\omega}{(\omega+i\nu)}-\frac{\omega(\omega+i\nu_T)}{c^{*2}}\right), Re(\kappa)>0, \quad (1)$$

here: $\omega_p^2=4\pi ne^2/m^*\varepsilon_l$ is the bulk plasma oscillation frequency in the semiconductor, m^*, $\nu=1/\tau$ are the effective mass and reciprocal relaxation time of electrons in the semiconductor regions, respectively; $s^2=V_F^2/3$, V_F is the Fermi velocity of electrons, $d^*=d+2r_{TF}$ is the effective barrier width, r_{TF} is the Thomas-Fermi screening radius, $\nu_T=4\pi Gd^*/\varepsilon_l$ is the reciprocal relaxation R_TC time due to tunnel conduction, $\kappa^2=q^2-\varepsilon_s\omega^2/c^2$, $\varepsilon_s=\varepsilon_l\left[1-\omega_p^2/\omega(\omega+i\nu)\right]$ is the semiconductor dielectric function, ε_l is the lattice dielectric constant, $c^*=c/\sqrt{\varepsilon_l}$. Eq. (1) was obtained in low-frequency ($\max\{|\nu_T|,\ \omega,\ \nu\}<<\omega_p$) and long-wavelength ($q<<\max\{1/d,\ 1/r_{TF}\}$) limits.

In the limit $q>>\omega_p/c^*$ we have $\kappa\approx q$, and Eq. (1) coincides with the previously derived one in the quasi-static approximation (see [1], [3]). One may neglect by the electromagnetic retardation, and JPP goes over into an excitation known as junction plasmon [1]- [3]. But in our case the electromagnetic retardation is very essential, especially in the low frequency region. The finiteness of c in the limit leads to well defined excitations ($Re(\omega)>Im(\omega)$) even when $\omega\ll\nu$:

$$q\approx\omega^{3/4}(i\nu)^{1/4}\sqrt{\frac{2}{c^*d^*\omega_p}}. \quad (2)$$

III. The impedance of the tunnel structure

We consider a structure consisting of metal ($z\leq -L$) – semiconductor with finite dimensions ($2W$ along x axis, ∞ along y axis, L along z axis) – tunnel barrier ($|z|<d/2$)

Microwave HFET Power-Combining Arrays Using Coplanar-Fed Bowtie Antennas

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Abstract — **A quasi-optical power-combining array consisting of bowtie antennas fed by coplanar waveguide is presented. The bowtie structure provides space to accommodate planar tuning structures as well as active devices. An HFET oscillator circuit that includes a pair of open-circuited coplanar stubs is embedded in one arm of each bowtie antenna. The stubs are designed to place the HFET output impedance in the unstable region of the Smith Chart. Experimental results for a 4 × 4 array are discussed and an equivalent circuit model used for the array design is presented.**

I. Introduction

IN RECENT YEARS, scientists and engineers have renewed their efforts to develop reliable and efficient solid-state sources operating at millimeter wavelengths. A significant part of this effort has focussed on quasi-optical techniques as an alternative to more traditional power-combining methods based on microstrip and waveguide structures [1]–[3]. Quasi-optical circuits can have significant advantages compared to their guided-wave counterparts (for example, elimination of waveguide sidewall losses and multi-moding problems). Because they are fully compatible with monolithic fabrication technology, planar quasi-optical arrays offer reduced manufacturing costs and the potential of directly integrating control elements and active devices in a single circuit. These features are of particular interest due to the increasing demand for functional and inexpensive millimeter-wave components by radar and communication system engineers.

Many different quasi-optical power-combining arrays have been investigated in the past, but few topologies have exhibited the design flexibility needed for realizing multi-functional circuits. Several investigators have demonstrated microstrip-based oscillator arrays that include beam scanning capabilities [4],[5]. Others have presented patch antenna or grid oscillator circuits with electronic frequency tuning [6]–[8].

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This paper describes a new quasi-optical array architecture based on bowtie antennas fed by coplanar waveguide (CPW). The bowtie structure allows wide latitude in the grid design, permitting CPW tuning structures and matching networks to be included without disrupting the overall array geometry.

II. Array Design

A diagram of the bowtie grid is shown in figure 1. The arms of the bowtie antennas provide space to accommodate planar transmission lines and semiconductor devices. As a result, impedance tuning circuits and control elements such as varactor diodes can be integrated directly into each cell of the array. The devices embedded in the grid are coupled to free space through CPW lines that feed the antennas. Unlike the more traditional quasi-optical arrays based on dipoles [3], the CPW feed lines can be adjusted to provide impedance matching without significantly disturbing the overall grid structure. In addition, the geometry of the array is fully compatible with standard coplanar HEMT layouts, making this array configuration an ideal candidate for monolithic integration.

A 4×4 version of the bowtie grid (illustrated in figure 1) was built as a proof-of-concept demonstration. The array was fabricated on a copper-clad Rogers *Duroid* 6010 substrate with dielectric constant 10.5 and thickness of 1.27 mm. Each bowtie antenna is 8 mm square and is fed by a 100 μm wide coplanar line with impedance of 75 Ω and electrical length of 30° at 5 GHz. GaAs HFET's (FHX35X, manufactured by *Fujitsu*, Inc.) are attached to the array with silver epoxy and wire bonded to the grid metallization. To facilitate wire bonding, the entire array is gold plated. A pair of open-circuited CPW stubs are placed 600 μm from the gate of each HFET. The characteristic impedance and length of the stubs (50 Ω and 3 mm, respectively) are chosen to give a reflection coefficient looking into the drain that is greater than unity.

Bias to the drains and sources is provided through

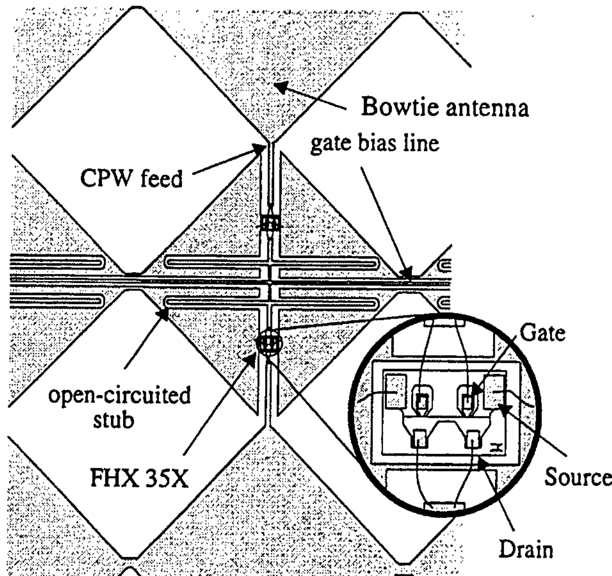

Fig. 1. Diagram of the bowtie oscillator grid. Coplanar feed lines couple the oscillator circuits to the antennas.

the arms of the bowtie antennas. Gate bias is fed through bias lines running horizontally across the array between adjacent bowtie antennas (see figure 1). At RF frequencies, these bias lines are treated as 50 Ω, open-circuited CPW stubs. The open circuits are a result of the array symmetry and arise from image currents on either side of the vertical symmetry planes between adjacent columns of bowtie antennas.

III. Frequency Tuning

The output of the power-combining array was measured using a ridged horn antenna in the far field. A planar mirror placed behind the array provided the external feedback needed for mutual injection-locking and served as a tunable backshort. With a drain bias of 3 V, the backshort position and gate bias were adjusted until oscillation was observed. Figure 2 shows the frequency tuning of the array as a function of mirror position. Also shown is a theoretical tuning curve obtained using the grid's equivalent circuit model and transistor small-signal scattering parameters. The HFET s-parameters were obtained by placing a single device in a 50 Ω test fixture and using an HP-8720 vector network analyzer.

The equivalent circuit model for an infinite array of bowtie oscillators is shown in Figure 3. This circuit, which is based on symmetry and the induced EMF method [9], models travelling waves with transmission lines. The bowtie antennas are represented as transmission lines with characteristic impedances of 80 Ω and electrical lengths of 30° at 5 GHz. Lumped inductors are included in the array circuit model

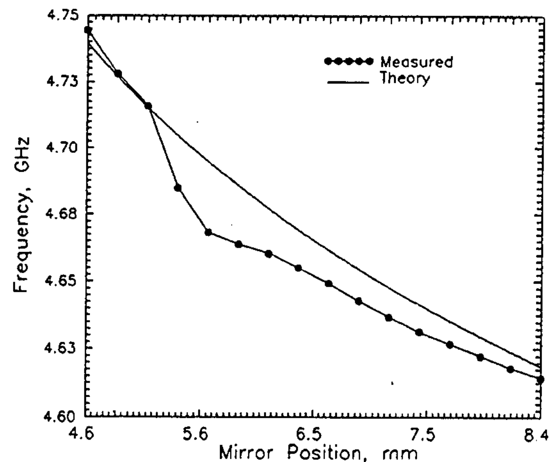

Fig. 2. Frequency tuning curve for the bowtie array vs. mirror position.

to represent wire bonds from the HFET chip to the CPW lines. Because bond inductance is difficult to model accurately, these inductors are adjusted to bring the theoretical tuning curves into agreement with measurement. The fitted value of 2.9 nH for the drain and gate inductance is reasonable for the approximate length (1 mm—2 mm) of bonding wire used.

IV. Radiation and Power Output

Radiation patterns of the array measured in the principal planes are shown in figure 4. The theoretical patterns are for a 4 × 4 array of infinitesimal dipoles on a 1.27 mm thick *Duroid* substrate backed by a planar conductor. The high sidelobe level in the H-plane is believed to be a reflection from the array mount and not due to the array itself. Figure 5 shows the effect of the backshort position on the H-plane antenna pattern. As the backshort is moved towards the array, both the directivity and power radiated decrease. It is estimated from these patterns that the antenna gain of the array is 16 dB. Using this estimated gain and the Friis transmission formula results in a net radiated power of 40 mW and an overall dc-to-RF conversion efficiency of 17%.

Figure 6 demonstrates the effect of altering the dc bias of different rows of the array. Because adjacent rows of devices share a gate bias lead, the dc operating point of pairs of rows can be tuned independently by adjusting gate voltage. It has been shown by Kurokawa [10] and later by York [11], that groups of coupled, non-linear oscillators will mutually injec-

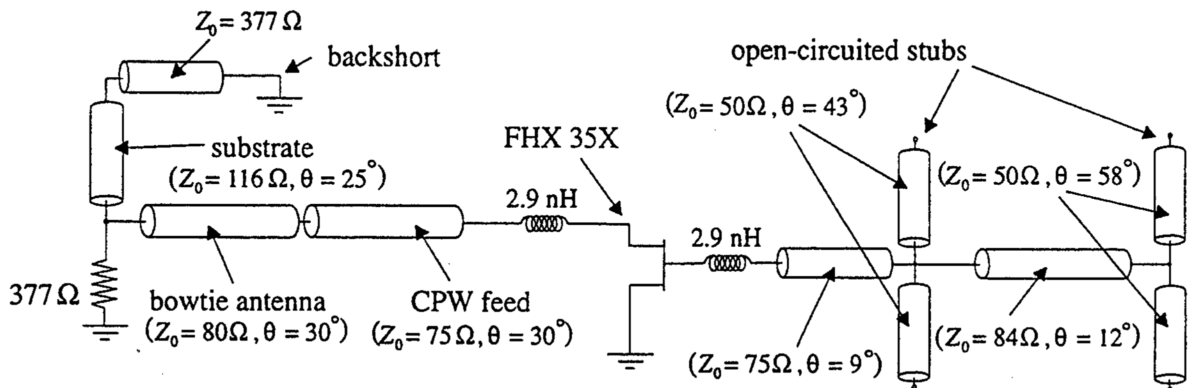

Fig. 3 Equivalent circuit model for an infinite array of bowtie oscillators. Free space is represented as a 377 Ω load and bond wires as lumped inductors. The electrical parameters for each transmission line at 5 GHz is given in parenthesis.

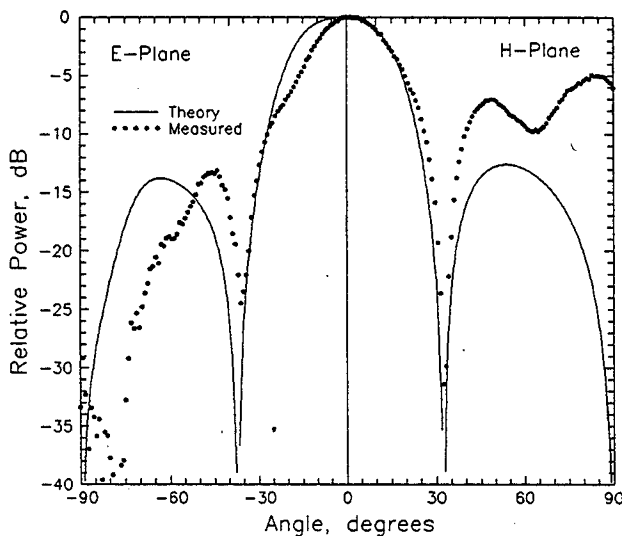

Fig. 4 E-plane (left side) and H-plane (right side) radiation patterns for the bowtie array.

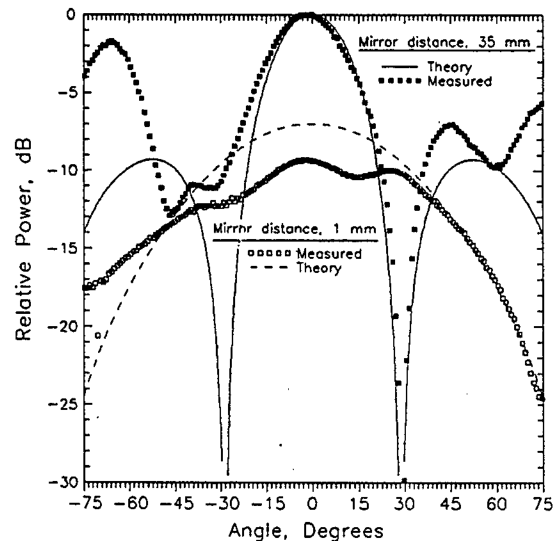

Fig. 5 H-plane radiation pattern of the bowtie array as a function of backshort position.

tion lock to a fixed frequency within a given locking bandwidth. The relative phase of the injection-locked oscillators depends on their initial free-running frequencies as well as complex coupling coefficients that describe the interaction between the oscillators. Adjusting the dc bias of the different rows in the array has the effect of tuning the oscillators' free-running frequencies. Consequently, adjacent rows of devices experience a phase shift that results in the beam steering shown in figure 6. Using this method, the main beam of the bowtie array can be steered by approximately $\pm 6°$ off boresight.

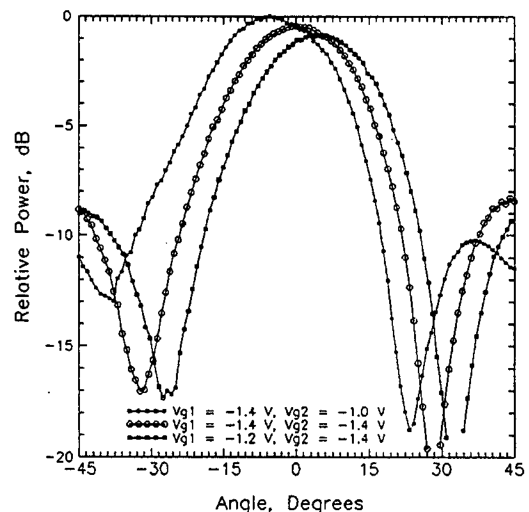

Fig. 6 Beam steering of the bowtie oscillator array in the E-plane. Each antenna pattern corresponds to a different set of gate dc bias voltages.

V. Summary and Conclusions

In this paper, we have presented a new quasi-optical oscillator configuration consisting of an array of bowtie

antennas fed by coplanar transmission lines. As a simple proof-of-concept demonstration, the circuit was not optimized for maximum power output. In addition, the transistors used in the array operate at a relatively low bias (typically, $V_D = 3\,\text{V}$ and $I_{DS} = 8\,\text{mA}$). The flexibility of the array geometry, however, should permit future circuits to be designed for maximum dc-to-RF conversion efficiency without fundamentally disturbing the grid architecture. The arms of the bowtie antennas also may provide space for additional circuits and devices, such as varactor tuning diodes. Because the array structure is based on coplanar waveguide, it is fully compatible with the majority of HEMT device layouts. This feature should prove advantageous for any future monolithically integrated array.

Acknowledgements

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HOT ELECTRON BOLOMETER DETECTORS AND MIXERS BASED ON A SUPERCONDUCTING-TWO-DIMENSIONAL ELECTRON GAS-SUPERCONDUCTOR STRUCTURE

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I. *Introduction*

A recent trend in basic solid state physics research has been toward a study of transport in the two-dimensional electron gas (2DEG) medium situated between superconducting regions [1,2,3]. Due to the very weak scattering of electrons in the 2DEG medium, very interesting mesoscopic effects occur, at sizes of the device which are much larger than other structures in which mesoscopic phenomena have been studied. This also allows one to investigate applications to electronic devices without resorting to sub-micron dimensions. One new potential application area for such devices may be to hot-electron bolometers (HEBs), which are beginning to be employed for very fast direct or heterodyne detection of THz radiation. The interest in a hybrid superconductor-2DEG-superconductor HEB stems from the hope of being able to heat the 2DEG medium with very little power, due to the fact that the 2DEG has a lower heat capacity than a superconductor such as NbN. If the 2DEG can be contacted via superconducting contacts, then we expect that a rapid change in resistance may occur at or near the critical temperature for the superconductor, T_c. The combination of low heat capacity and a steep change in resistance with temperature, should result in a potentially very sensitive detector. For the contacts to be effective, one requires high transparency through the superconductor-semiconductor (S-Sm) interface. The interface must have a low Schottky barrier, and give rise to multiple Andreev reflections. The second feature is emphasized if the region near the S-Sm interface displays a high degree of disorder [1]. We have developed a new S-Sm-S structure with NbN as the S component, which appears very promising based on the above criteria.

II. S-Sm-S Structure: Fabrication and Characteristics

We have manufactured S-2DEG-S structures by using AlGaAs/GaAs single heterostructures between two niobium nitride (NbN) superconducting contacts.

The structures have a topology depicted in Fig.1. A mesa with a profile height of 200 nm was etched in a standard single heterostructure wafer (manufactured by the MOVPE technique with an AlGaAs layer doped to $\sim 10^{18}$ cm^{-3}, and undoped spacer thickness 12 nm). For surface protection, a layer of undoped GaAs was employed. The two-dimensional electron gas was buried at a depth of ~110 nm from the wafer surface. NbN films were created as long (100 μm) strips with a width of d=10 μm, in order to make contact with the 2DEG at the edges of the mesa. The distance between the superconductor contacts (L) is about 2 μm at the 2DEG level. At the same time the distance separating the superconductor contacts is about 1 μm on top of the mesa. The 2DEG-layer had a concentration $N_s=1.4*10^{11}$ cm^{-2}. The Hall mobility $\mu_H=1.5*10^5$ cm^2/Vs, which results in a 2DEG mean free path of about 1.6 μm.

The NbN films were 10 nm thick, and were deposited by dc magnetron sputtering in pure nitrogen ($1.7*10^{-2}$ Pa pressure) and argon (3.5 Pa pressure). The temperature of the wafer during the NbN deposition process was ~200 C. Before metal deposition we used a chemical wafer cleaning procedure. The superconducting structure was fabricated by ion-beam etching. The superconducting transition in the NbN strips was observed at T_c=11K with a transition width of ~0.8 K. The temperature dependence of the resistance R(T) measured with a current of 1 μA is shown in Fig.2. The sharp drop in resistance beginning at 12 K is due to the superconducting transition of the long portion of the NbN strips. The resistance is constant in the interval 8.7K<T<11K and then falls for T<8.7K. It should be noted that at the lowest measuring temperatures (~4.2K) the resistance reaches a constant value, close to the calculated 2DEG-channel resistance (about 35 Ohm).

Control structures with the same topology were also fabricated on pure GaAs wafers with highly doped surface layers of $GaAs^{++}$ ($n_s \sim 2*10^{18}$ cm^{-3}) with a thickness of 250 nm, and mobility close to 10^4 cm^2/Vs at liquid helium temperature ($l \sim 100$ nm <<L). The results for these structures are similar to those obtained for the 2DEG-structures, but the minimum resistance is much greater for the bulk GaAs structures.

The structures were tested by SEM. The SEM images were used to inspect and verify the geometrical parameters of the devices. When inspecting the gap on top of the mesa between the NbN strips, we discovered that some devices exhibited very narrow (<< 1 micron) parasitic superconducting paths due to fabrication problems. These devices could not be used since the super-current was due to the shorting NbN strips. We also checked the structures with a micro-X-ray imaging technique. By these two methods, we were able to select good structures without the parasitic NbN shorting strips. All data reported here are for these devices only.

III. DC Measurements of the S-Sm-S Structures

In our structures with a 2DEG-channel, the value of the electron mean-free-path predicts that the device is in the diffusive and noncoherent regime. The coherence length ξ_N is much smaller than l, which is about 1.6 μm. Typical current-voltage characteristics of our sample with a 2DEG channel at different temperatures are shown in Fig.3. The voltage dependence of the differential resistance R_d=dV/dI for the same temperatures is displayed in Fig.4. These curves have some clear irregular features, inherent in S-Sm-S structures with high barrier transparency: a minimum of R_d at V=0, and an excess current even in the normal conductivity region ($V > 2\Delta/e$). We also observe symmetrical peaks at $V>2\Delta/e$ (points A), which move to zero voltage as the temperature is increased. At the same time, the voltage position of the first bend in the R_d (V) dependence (point B), is practically independent of the temperature. As R_d was measured for different currents, the R_d values were the same for T>9K. For T<8.7K, the temperature dependence of R_d measured at a small voltage (V = 50 μV) approaches $R \sim \exp -(\Delta/kT)$, where Δ = 1.58 meV. We have taken into account that the constant 2DEG channel resistance is about 35 Ohms. The value of Δ is in very good agreement with the value of T_{c1}=8.7K if we use the BCS relation $2\Delta=4.1kT_c$.

The irregular features in the R_d versus voltage curves which we have observed, both in the control bulk GaAs and the 2DEG-channel structures, point to a high transparency of the superconductor-semiconductor interface. They could be caused by multiple Andreev reflections, which arise from the high level of disorder in the NbN thin films. The excess current would be explained as being due to the process of transition from Andreev coherent reflection to the usual quasi-particle transport. In the first case an electron with energy $\varepsilon < \Delta$ (the energy is counted from the Fermi level) creates a hole which moves in the reverse direction. Current continuity is conserved by a Cooper pair which carries the current in the superconductor. In the second case quasi-particles with $\varepsilon > \Delta$ are transmitted through the interface in the usual manner. The transition from the first to the second case would be observed at a voltage close to Δ/e at the superconductor-semiconductor interface region. This transition corresponds to the sharp bend in the R_d(V) curve at the lowest temperatures (point B corresponds to $V= 2\Delta/e = 4.1kT_c/e \sim 3.5$ mV). The value of $2\Delta/e$, rather than Δ/e, is required in order to account for the two S-Sm interfaces. It may be noted that we have observed a fine structure in the R_d(V) curves at small voltages as well (V< 3.5 mV). The voltage position of these features changes rapidly as the temperature increases. The origin of this structure is not clear at the moment.

The voltage position of point A (Fig 4) of the R_d(V) curves is determined by self-heating effects. The temperature dependence of the position of this point is very close to $V \sim (T_c - T)^{1/2}$ if we assume $T_c = T_{c1}$=8.7K . It should be noted that this is the same critical temperature which we obtained from the onset of the low-temperature exponential slope in the R_d(T) dependence. Thus, this temperature plays the role of the critical superconducting temperature for the 2DEG-channel in our structures. It seems likely that it may be explained in the framework of S-I-N-I-S structures with thin insulator (I) layers, in which the order parameter is reduced due the insulator layers.

IV. Discussion of the Measured Data for S-Sm-S Structures

To understand the more pronounced changes in differential resistance observed in hybrid structures with higher-mobility 2DEG, we must once again invoke the ballistic transport properties. Ballistic and diffusion currents can coexist, since l is greater than or close to L for the structures we have used. The relation between these components of the current is determined by the width (d) of the 2DEG region. For the configuration which we have used, the "coupling" between the superconductor regions due to ballistic and diffusive electrons, respectively, may be predicted from the injection angle of the electrons at the interface.

It should be noted that the excess current is very large. Heating of the electron gas would be related to the existence of a fraction of electrons which are transported by diffusion (this fact is supported by the strong temperature and current dependencies of R_d). At the same time, the electron-electron scattering time in 2DEG with $\mu \sim 10^5 - 10^6$ cm^2/Vs at helium temperatures is close to the electron-impurity elastic scattering time. For this reason, diffusing electrons have an opportunity to change their energy and to experience heating in the 2DEG channel. In this situation, the electron temperature T_e is determined by the power loss in the device. The cooling of the electron gas under elastic diffusion transport conditions occurs in the superconductor contacts (similar to the "diffusion-cooling" case for thin film superconductor HEBs). A different case occurs if there is a large fraction of inelastically diffusing electrons; this situation corresponds to electron-phonon cooling being the dominant cooling effect. In the samples we have used, the fraction of inelastically diffusing electrons is very small because $L \ll l_{eph}$ ($l_{eph} = \sqrt{D^* \tau_{eph}}$ where $\tau_{eph} \approx 0.8$ns [4]). Our present devices are characterized by diffusive transport and electron heating in the 2DEG, however, as discussed above. Most of the cooling is expected to occur in the NbN contacts. This is a more complicated situation, which has not yet been analyzed theoretically. By comparison with simpler experiments involving only 2DEG [5], we can use the energy loss rate in the sample, calculated from the applied voltage and the current (about $10^{-13} - 10^{-12}$ W/el), to crudely estimate a very high electron temperature in the 2DEG ($\approx$ 100 K). The increase of the electron temperature in the semiconductor region would in turn result in a decrease of the excess current, I_{c1}. It would also cause a decrease of the interface voltage drop which corresponds to quasi-particle transport across the interface, since electrons with energy $\varepsilon > \Delta$ create a quasi-particle current. The fraction of electrons which undergoes multiple Andreev reflections then sharply declines, and the interface resistance increases, as we have observed. The heating effect should depend on the values of d and w. In general, the heating effect we predict could be used for detection and mixing in these devices, at a reasonably high operating temperature ($\sim$ 4 K).

V. *Conclusion.*

We have manufactured a new type of hybrid S-2DEG-S structures on the basis of AlGaAs/GaAs single hetero-junctions, with NbN as the superconductor. Current-voltage characteristics of this structure were studied under non-coherent ballistic transport conditions. Features of the current-voltage characteristics such as an excess current, and a deep minimum of the differential resistance at V~0 were observed. These features point to the involvement of multiple Andreev reflections in the transport process for current passing through the S-2DEG interface. A high interface transparency, and a large value of excess current, show promise for application of high-disorder NbN thin films as the superconductor contact to GaAs two-dimensional electron gas. An important advantage of the S-Sm-S device is the fact that it operates at much higher temperatures than similar devices which have been investigated previously.

VI. *Acknowledgements.*

This work was made possible thanks to support from the Russian Foundation of Fundamental Research (projects Nos.95-02-06409 and 96-02-18624), the Nanostructure Physics Program, # N1-068/4, and from NATO grant HTECH.LG 960606. We would also like to thank Professor Kei-May Lau for providing us with several 2DEG substrates.

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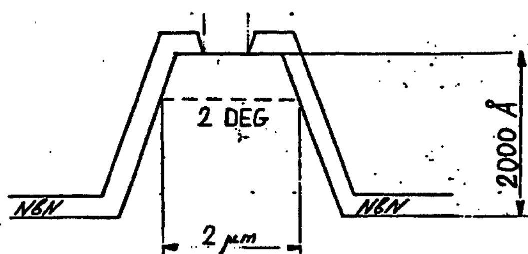
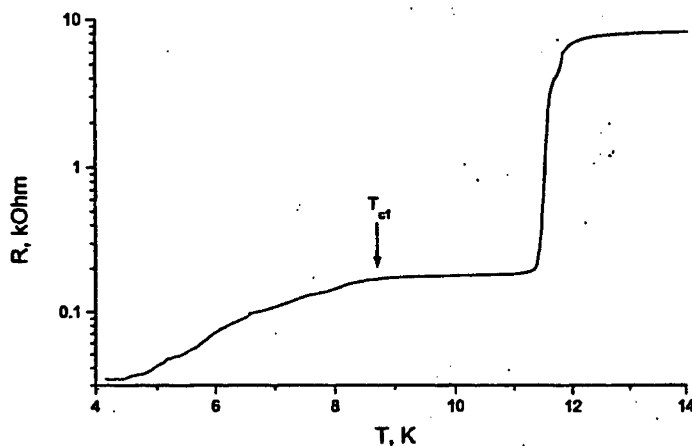
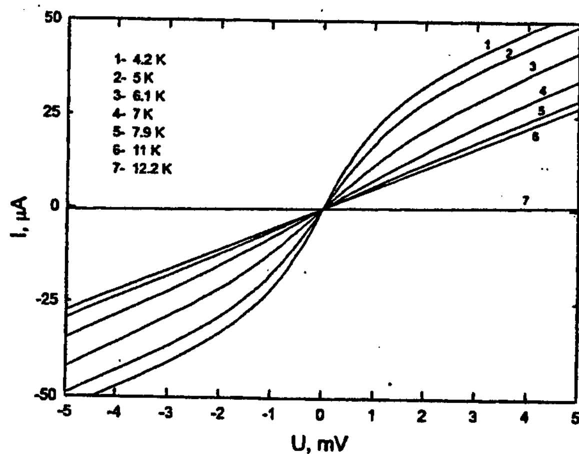


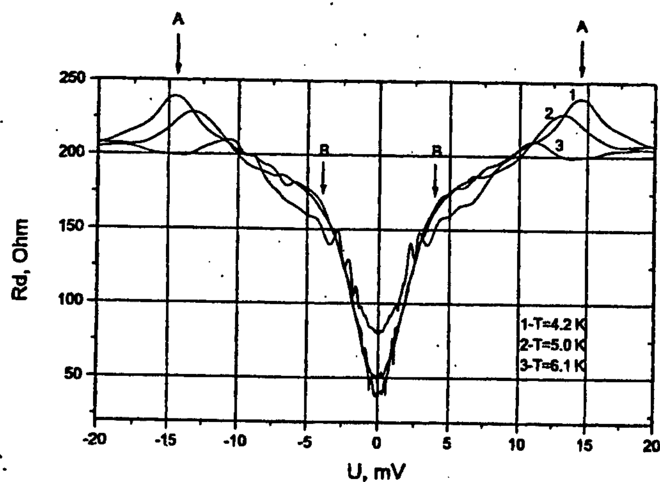
1. Schematic view of the S-2DEG-S structure.



2.Temperature dependence of the resistance for the NbN-2DEG-NbN structure.



3.Voltage-current characteristics of the structure at different temperatures.



4. Voltage dependence of R_d for several different temperatures.

Characterization of DyP/GaAs Schottky Diodes for High Temperature and High Frequency Applications

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Characterization of DyP/GaAs Schottky diodes for high temperature and high frequency applications will be reported in this paper. DC characterization including current-voltage (I-V) and capacitance-voltage (C-V) measurements was performed at different temperatures from 25 to 250 ^{o}C. High frequency characterization was also performed by measuring the scattering parameters (S parameters) of these Schottky diodes as functions of frequency. An equivalent circuit model was drawn from these high frequency measurement data through the use of Touchstone/Libra. A cut-off frequency of close to 2.5 THz was then determined from the equivalent circuit parameters for the Schottky diodes with an area of 10 μm^2.

The development of thermally stable metal contacts is one of the most challenging tasks for the development of III-V semiconductor devices for high temperature and high power applications. When thin metal films are exposed to high temperatures during fabrication or operation, interface reactions between the metal and semiconductor can take place that results in changes in the electrical properties of the contacts. Reliability considerations also require that the contacts and the metal semiconductor barriers are able to withstand harsh environment for relatively long periods of time without degradation. The high melting temperature of rare earth-group V (RE-V) compounds such as dyprosium phosphide (DyP) and dyprosium arsenide (DyAs) makes them attractive for the application as high temperature contacts to III-V compound semiconductors. In this paper, we will report the results from the study of DyP/GaAs Schottky diodes for high temperature and high frequency applications. One should note that the lattice mismatch between DyP and GaAs is less than 0.01% at room temperature.

DyP has been grown on GaAs by solid source MBE using custom designed group V thermal cracker and group III high temperature diffusion cells. DyP was found to be stable in untreated air with no signs of oxidation even after months of exposure. The DyP epilayers are n-type with measured electron concentrations on the order of 3 to 4 x 10^{20} cm^{3} with room temperature mobilities of 250 to 300 cm^{2}/Vs. No definite absorption edge was found in either photothermal deflection spectroscopy (PDS) or Fourier transform infrared spectroscopy (FTIR). This indicates the absence of a bandgap and that DyP is likely a semi-metal. The resistivity values of DyP as determined by four-point probe and Hall measurement were found to be consistent with each other and were in the range of 6.5 x 10^{-5} to 1.5 x 10^{-4} Ω.cm.

DyP/GaAs Schottky diodes were fabricated with an area of 40,000 μm^2. From the I-V data obtained (shown in Fig. 1), rectifying behavior was observed from 25 to close to 200 °C. From these I-V data, a barrier height of approximately 0.81 eV was found at the room temperature. The barrier height, as expected, decreases as temperature increases (shown in Fig. 2). The saturation current increases dramatically as the temperature increases as shown in Fig. 3. These Schottky diodes can be applied for high temperature RF detectors and mixers.

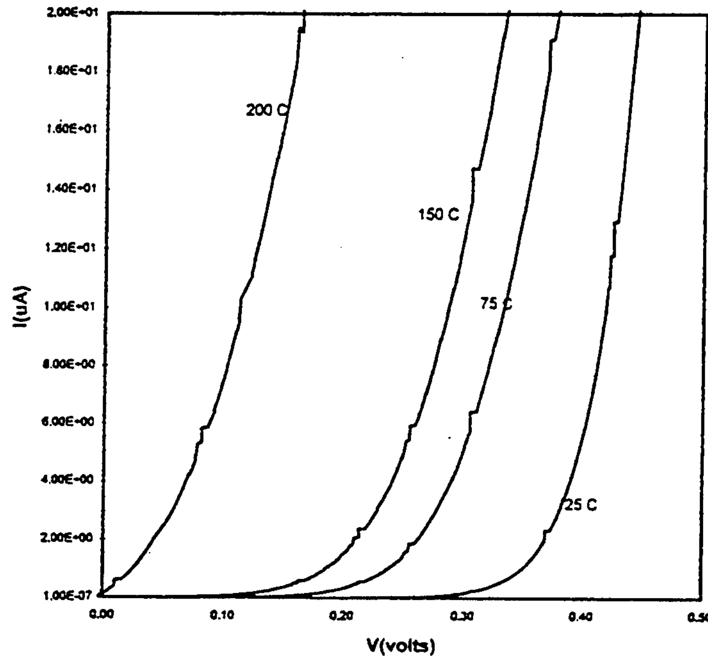

Fig. 1 The I-V curves of DyP/GaAs Schottky diodes at temperatures from 25 to 200 °C.

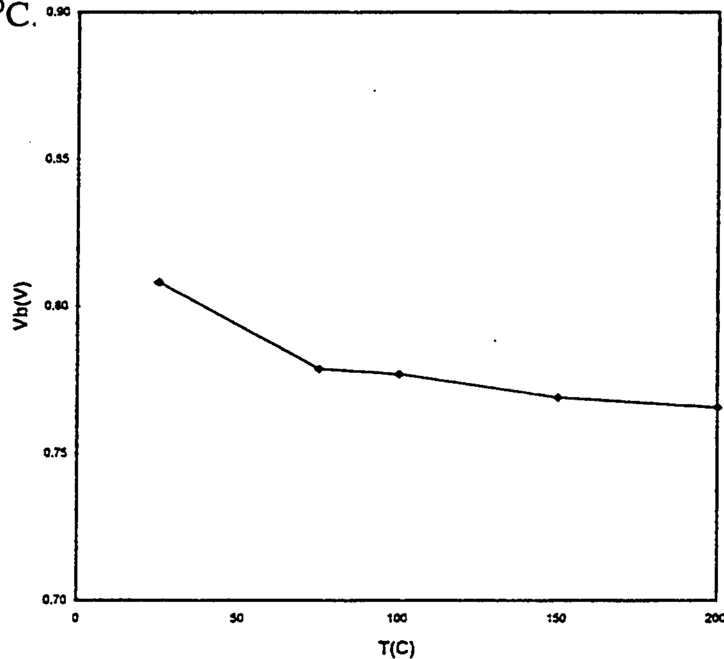

Fig. 2 The barrier height of DyP/GaAs Schottky diodes as a function of temperature.

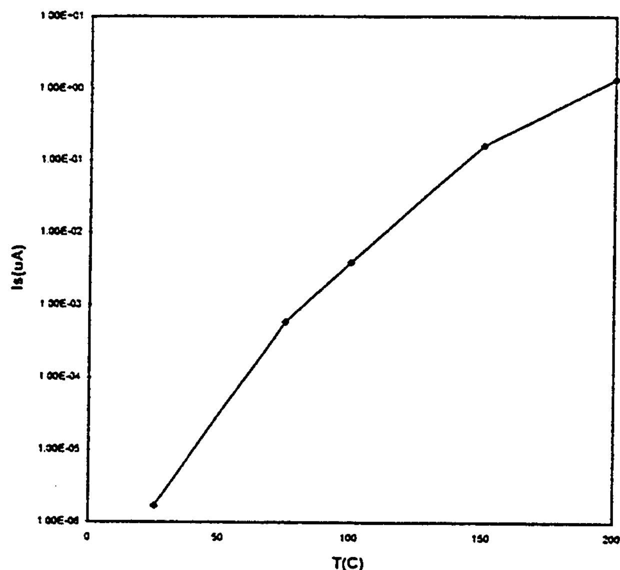

Fig. 3 The saturation current of DyP/GaAs Schottky diodes as a function of temperature.

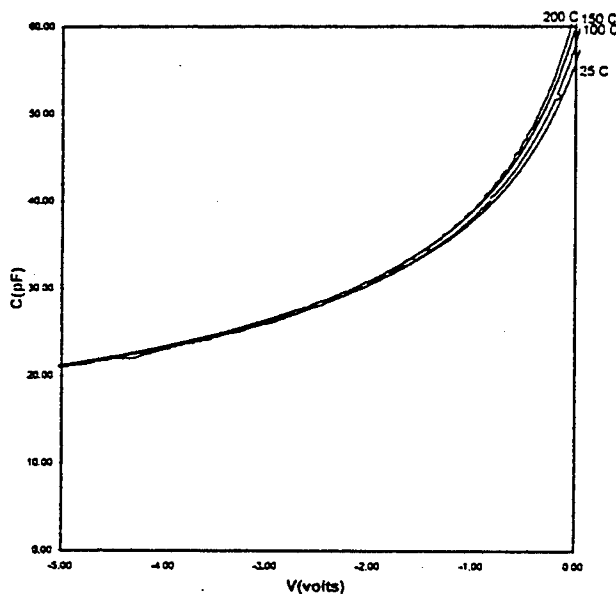

Fig. 4 The C-V curves of DyP/GaAs Schottky diodes at temperatures from 25 to 250 ^{o}C.

From the data obtained, the C-V curves shown in Fig. 4 show little change with temperature from 25 to 250 ^{o}C. They display a C_{max}/C_{min} ratio of close to 3. $1/C^2$-V curve was plotted from the room temperature C-V data are shown in Fig. 5. An uniform doping of 2.3 x 10^{17} cm^{-3} was obtained from this plot which agree very well with the results given by other measurements. The well-behaved C-V curves at elevated temperatures demonstrate the potential of these Schottky diodes as high power frequency multipliers.

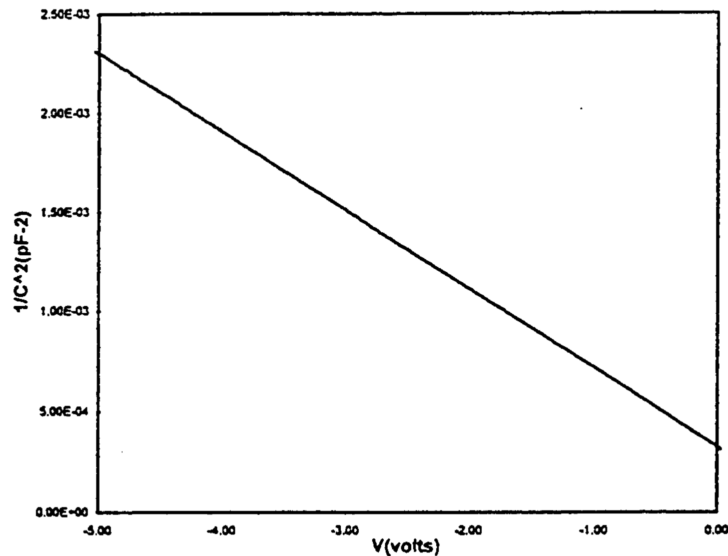

Fig. 5 $1/C^2$ as a function of voltage plotted for DyP/GaAs Schottky diodes.

High frequency characterization of DyP/GaAs Schottky diodes were conducted using a HP vector network analyzer with a frequency capability of 45 MHz to 40 GHz. The equivalent circuit was constructed and the component parameters were obtained from Touchstone/Libra using the S-parameters from these measurements. The component parameters are consistent with the results from our DC measurements. Based on these parameters, the cut-off frequency of the Schottky diodes with an area of 10 μm^2 was determined to be close to 2.5 THz. The cut-off frequency of these diodes can be improved through the manipulation of the doping of GaAs, device layout, etc.

In this study, we report a newly developed group of high temperature and high frequency diodes employing rare earth-group V compounds as Schottky contacts to III-V compound semiconductors. Through the results presented, the high temperature and high frequency capability of DyP/GaAs Schottky diodes have been demonstrated. Rare earth-group V based devices can also be used in high power electronics as the operating temperature of the device is likely to be high. Future work include further development of rare earth-group V compounds, other DyP/GaAs junction device structures, and high temperature and high power circuits employing DyP/GaAs Schottky diodes.

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Physical Aspects of GaAs Schottky Diode Operation at Terahertz Frequency

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I. Introduction.

Schottky barrier diodes are important design components in the millimeter and submillimeter regime because they are majority carrier devices, and therefore possess a rapid response time. In fact, Schottky diodes are the primary nonlinear devices used in both detectors and receivers at very high frequencies [1]. Currently, Schottky diode multipliers operate up to about 800 GHz [2], and a Schottky diode receiver has been realized at 5.0 THz [3]. The full understanding and optimization of such mixers and multipliers will require accurate physics-based simulations tools. At THz frequencies, effects such as electron inertia and velocity saturation must be incorporated into the nonlinear analysis. In this paper, we will focus on the large signal operation of GaAs Schottky diodes within the terahertz regime. It is clear that the enhancement of high frequency performance requires a corresponding reduction in parasitic ohmic losses and capacitance. However, this must often be accomplished while maintaining the necessary nonlinear characteristics (e.g., in receiver design).

To reduce bulk parasitic effects, degenerately doped Schottky diodes are required at THz frequencies. These large increases in the doping will directly influence thermionic emission, field (tunneling) emission, and depletion layer capacitance. Since these factors are known to strongly dictate time-domain device operation, we have previously developed new electron transport models that accurately represent the effects of degenerate doping upon the electron gas in the semiconductor [4]. In this paper, we incorporate these new transport models into a momentum-balance model to study the large-signal operation of a degenerately doped GaAs Schottky diode at THz frequencies. The results of these physics-based studies will be compared to results obtained from a more traditional equivalent circuit-based technique. This more conventional circuit-based approach uses a nonlinear diode I-V characteristic (obtained from measured data) and incorporates time-dependent effects using phenomenological inductive, capacitive, and resistive models. This work will illustrate the general inadequacies of the traditional heuristic approach where simplified time-independent resistance and inductor models are used. Furthermore, these physics-based investigations will provide guidance for future studies of GaAs Schottky diode operation at very high frequencies

II. The Diode Models : Physics-based and Heuristic.

We previously considered the problem of degenerately doped GaAs Schottky diode operation and have developed the general models required to describe electron transport under these conditions [4]. Here, accurate scattering models were established to predict mobility values within degenerate (i.e. $n_e > 6.0 \times 10^{17} cm^{-3}$) GaAs material. In addition, new models for both thermionic and field (tunneling) emission were derived. To more accurately account for

degenerate effects, we include the full Fermi-Dirac distribution function into the Bethe formulation for the emission current. After integrating over velocity-components perpendicular to the barrier, the resulting equation for thermionic emission becomes

$$J_{TE} = A^{*}T^{2}\int_{e_b}^{\infty} dx \ln\left(\frac{1+\exp(e_F - x)}{1+\exp(e_F - x - \gamma)}\right), \tag{1}$$

with $e_b = E_b/k_B T = e^2 N_D w^2/(2\kappa_o k_B T)$, $\gamma = (eV_{bi} - E_b)/k_B T$, where A^* is the Richardson constant, w is the width of the depletion layer , $E_b = \phi_b - E_C(z=w)$ is the barrier height for electrons in the semiconductor for arbitrary applied biases, κ_o is the static dielectric constant and V_{bi} is the built-in voltage. Similarly, the field emission current is determined by the integrated product of the electron distribution with the probability of tunneling through the parabolic barrier. We modify the Padovani and Stratton [5] formulation to include the effects of electrons deep within the distribution function, which leads to the tunneling current expression

$$\begin{aligned} J_{FE} \;=\; & 2e_b A^{*} T^{2} \int_{0}^{\pi/2} d\theta \cos\theta \sin\theta \exp\left(-\alpha\left[\cos\theta - \sin^2\theta \ln\left(\frac{1+\cos\theta}{\sin\theta}\right)\right]\right) \\ & \times \ln\left(\frac{1+\exp\left(e_F - e_b \sin^2\theta\right)}{1+\exp\left(e_F - e_b \sin^2 - \gamma\right)}\right) \end{aligned}, \tag{2}$$

where $\alpha = E_b/E_{oo}$ and $E_{oo} = \left(e^2 N_D/(4\kappa_o m_n)\right)^2$. Previous Monte-Carlo simulations [6] of the electron distribution function at the Schottky diode interface have demonstrated nearly hemi-spherical results. This leads to an electron recombination velocity that is twice as large as the one obtained from the conventional thermionic theory [7]. Hence, we must multiply the derived Richardson constant by two to account for this known form of the electron distribution. Our physics-based model for the total current density through the diode, J, is now given by the simultaneous solutions of the set

$$J = J_{TH}(w) + J_{FE}(w) - eN_d \frac{dw}{dt}, \tag{3}$$

$$(L-w)\frac{dJ}{dt} = \frac{eN_D}{m_n}(V_D(t) - V_{bi} + \frac{E_b}{e}) - \frac{J}{\tau}[\frac{\pi a \sigma_{epi}}{4\sigma_{sub}} + L - w]. \tag{4}$$

Here, Eq. (3) defines the total current density inside the depletion region. Equation (4), derived from momentum balance, gives the total current in the neutral semiconductor region where L is the thickness of the epi-layer and a is the wisker-contact radius and $V_D(t)$ is the diode bias [4]. In Eq. (4) we have also introduced the effects of current spreading in the highly doped substrate through an effective spreading resistance $R_{sub} = (4a\sigma_{sub})^{-1}$, which is valid for a substrate thickness large compared to the contact radius [8]. The equivalent circuit model approach models the intrinsic Schottky diode as a nonlinear current source in parallel with a nonlinear capacitor element [9]. The effects of inertia and current spreading in the substrate are included using a series inductor and resistance, respectively. This heuristic model leads us to the system

$$J = J_s \exp(\frac{E_b - eV_{bi}}{\eta k_B T}) + \frac{(eN_d)^{1/2}}{(2\kappa_o E_b)^{1/2}} \frac{d(V_{bi} - E_b)}{dt}, \quad (5)$$

$$L_{ind} \pi a^2 \frac{dJ}{dt} + J[\frac{\pi a}{4\sigma_{sub}} + \frac{L}{\sigma_{epi}}] + V_{bi} - E_b / e = V_D(t). \quad (6)$$

where $L_{ind} = L\tau/(\pi a^2 \sigma_{epi})$ is the inertial inductance and η is the ideality factor.

III. Results and Conclusions.

A numerical study was performed to compare the physics-based model to the equivalent circuit description of Schottky diode operation. For this study, a whisker point-contacted platinum-GaAs Schottky diode with ϕ_b= 1.02 eV is considered. The contact diameter is $0.25\ \mu m$, the epilayer is 300 $\mathring{A}$ thick and doped $10^{18}\ cm^{-3}$, and the substrate is $3\ \mu m$ thick and doped $8 \times 10^{18}\ cm^{-3}$. First, Fig. 1 compares the physics-based calculations of J, for a range of dc applied biases, to the actual measured data. Here, very good agreement is observed. The experimental data was then used to obtain $J_S = 4.11\ mA/m^2$, $\eta = 1.58$, $\mu_{epi} = 3000\ cm^2 / V \cdot s$ and $\mu_{sub} = 1250\ cm^2 / V \cdot s$ for use in Eqs. (3) to (6). A Runge-Kutta based numerical algorithm was used to solve both the physics-based and heuristic models for a time-dependent biasing of $V_D(t) = 0.7 + 0.26\sin(2\pi f \cdot t)$ where f = 0.5, 1.0 and 2.0 THz. Note, this choice restricts $w \leq L$. The results of these simulations are given in Figs. 2 through 4. At the sub-THz frequency (i.e., 0.5 THz), the heuristic model predicts maximum (dominated by emission) and minimum (dominated by displacement) current densities in very good agreement with the physical model.

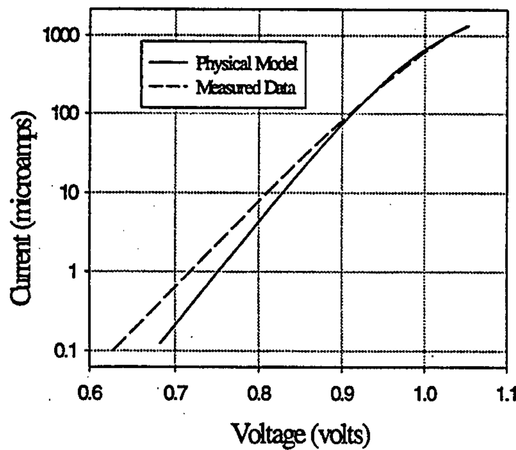

Figure 1. Diode current (dc) versus voltage.

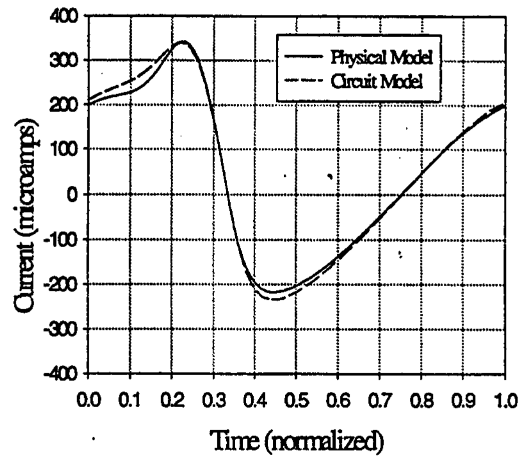

Figure 2. Diode current at 0.5 THz.

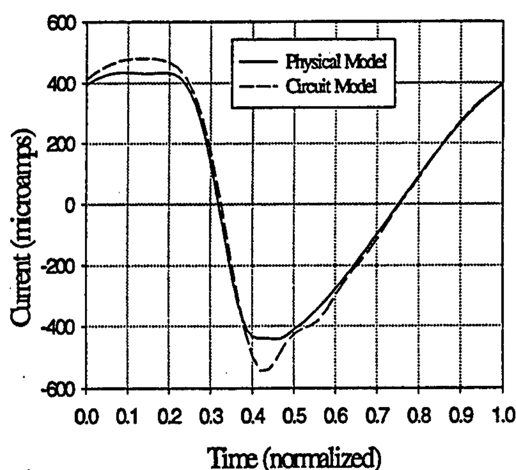

Figure 3. Diode current at 1.0 THz.

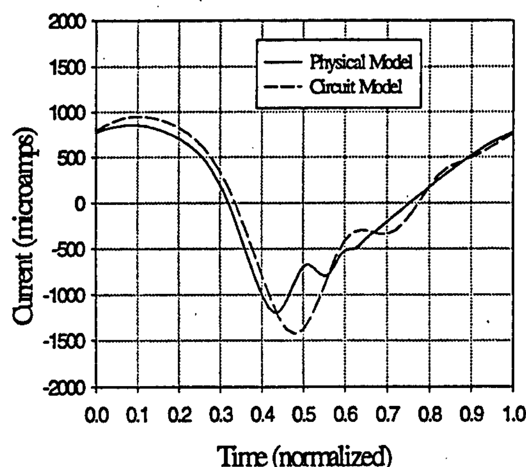

Figure 4. Diode current at 2.0 THz.

However, as the frequency increases, the circuit model tends to overestimate the displacement current and relative phase in comparison with the physical model. This displacement-current phenomena is probably due to the fact that the heuristic model does not include any time dependence into the inductor or spreading resistor models. Conversely, the physical model directly accounts for this effect through the amount of variation in w. In addition, a growing influence of inertial effects on the emission (i.e. particle) current, as a function of increasing frequency, is also exhibited in the 1 and 2 THz results. Finally, the quasi-sinusoidal results indicate that appreciable differences in the fundamental-frequency current (i.e. amplitude and phase) are predicted by the two different diode models at THz frequencies. Since such discrepancies in estimating the time-dependent current (and therefore impedance) can lead to improper circuit matching, resolving these issues theoretically is very important to high frequency component design. Hence, this work has demonstrated the value of the physics-based modeling approach both at sub-THz frequencies, where performance can be accurately estimated without dc measurement-based fitting parameters, and at THz frequencies were the heuristic model begins to fail.

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4H-Silicon Carbide Schottky Barrier Diodes for Microwave Applications

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***Abstract*— The feasibility of SiC Schottky barrier diodes for high power and high temperature microwave applications like detectors and mixers is investigated. The dependence of the zero-bias cut-off frequency for 4H-SiC Schottky Barrier Diodes is determined as a function of structural parameters theoretically and experimentally. Theoretically, a cut-off frequency of 96 GHz is obtained for a diode with an anode radius of 5 μm.**

I. Introduction

Silicon Carbide MESFETs[1] has lately shown good microwave performance. To our knowledge no calculations on the microwave performance for 4H-SiC Schottky diodes has been presented. Recently[2,3] junction diodes has been used to investigate intermodulation behaviour of SiC, operating at a LO of 500 MHz and an IF of 100 MHz. SiC diodes is particularly interesting for high-temperature, high-power and harsh environments. Because of the materials ability to withstand radiation, high electric fields, combined with a high thermal conductivity, and bandgap, the material is interesting to investigate in applications for high frequencies.

II. The Schottky Barrier Diode (SBD)

The proposed Schottky Barrier diode is described in Fig 1. On top of the 4H-n++-type substrate, a highly doped buffer layer is grown, followed by a n-type epilayer. Mesas are etched by IBE method with Ar. Schottky barriers are formed by evaporation of Ti-Au through a lift-off mask. A backside contact is formed by Ni-evaporation and annealing at 950 C for 5 min. in Ar/He 10:1.

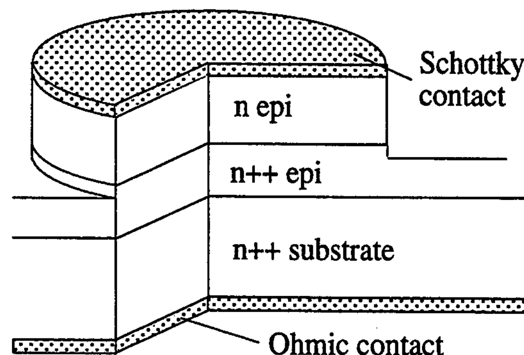

Fig 1. Split view of the Schottky barrier structure

The zero-bias cut-off frequency f_{cut} defined as $1/(2\pi R_S C_0)$ is used as general figure of merit for high frequency Schottky barrier diodes[4]. f_{cut} should be of the order 5-10 times the

operational frequency as a rule of thumb. In order to obtain a high f_{cut}, the series resistance and the junction capacitance should be minimized. In addition, the diode must be able to withstand a certain reverse voltage before breakdown.
The theoretical expression for the series resistance is includes quasi-neutral resistance, resistance from first epi, and spreading resistance in the bulk:

$$R_S(V) = \left(\frac{d_{epi2} - W(V)}{\sigma_{epi2}} + \frac{d_{epi1}}{\sigma_{epi1}} \right) \frac{1}{\pi r^2} + \frac{1}{2\pi\sigma_{bulk} r}$$

Anisotropic doping dependent mobility using the Hall data by Schaffer et. al.[7], and incomplete ionization of donors[6] was used to calculate the conductivity of the epilayers and substrate. Nitrogen donor level was taken to be 100 meV. The effective density of states mass was calaculated from an article[8] by NT.Son et. al. The contribution from the contact resistance was neglected because of a large backside contact (0.64 cm^2) which made its contribution minute.
The cut-off frequency is mainly dependent on the epilayer thickness and doping, the Schottky contact area. This dependence is calculated from textbook formulas[5] and the result is plotted in fig.2, where f_{cut} versus epilayer doping and contact area is plotted. The epilayer thickness is constant in this case and equal to 0.37μm.

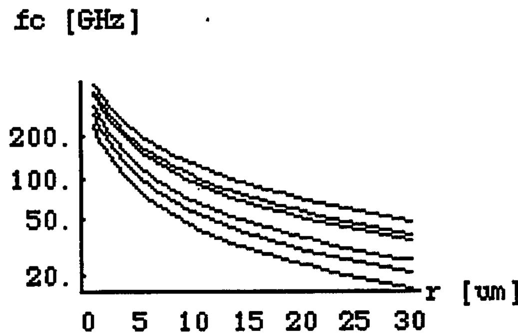

Fig 2. Cut-off frequency as a function of anode radius. The Doping of the epilayer is from the top down $N_D=5\cdot10^{16}$, $8\cdot10^{16}$, $1\cdot10^{17}$, $2\cdot10^{17}$, $3\cdot10^{17}$, $5\cdot10^{17}$ cm-3 . Epilayer thickness=0.37 μm, Vbi=0.97 V.

The ionization integral was also calculated using data from an article by M.Ruff et.al.[6]. In fig 3 below, the calculated breakdown voltage due to avalanche multiplication, versus doping concentration, is plotted. For $N_D=3.1\cdot10^{17}$ cm^{-3} , the diode should withstand a voltage of 150V for this type of abrupt junction. The epilayer of 0.37 μm is fully depleted at 38.6 V.

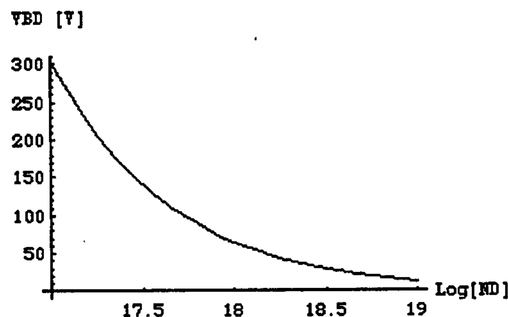

Fig 3. Simulated breakdown for 6H-SiC by avalanche multiplication for an abrupt junction. Doping is in [cm^{-3}].

To make a proper choice of epilayer thickness and doping, all above discussed parameters must be considered.

III. EXPERIMENTAL RESULTS

Diodes were fabricated on 4H-SiC with an n-epilayer thickness of 0.38μm and N_D=3.1·10^{17}, and n^{++} epilayer thickness of 0.5μm and N_D=9.0·10^{18} cm^{-3}. The epilayers were grown on the Si-face of a 4H-SiC substrate with N_D=1.1 10^{19}cm^{-3}, and a thickness of 340 μm. In order to verify the scaling of f_{cut} versus anode radius, a series of diodes with a radius from 5 to 100 μm were fabricated. C-V measurement and I-V measurement were performed. The C-V data is plotted in fig 4 for two diode sizes. This data confirms the nominal doping concentration of the *n*-epilayer. Measurements of C_0 for different anode sizes (7.5-50 μm) gave $C_0=12.9(r/50)^2$ pF, where r is in μm.
The I-V data for a 25 μm diode is shown in fig 5.

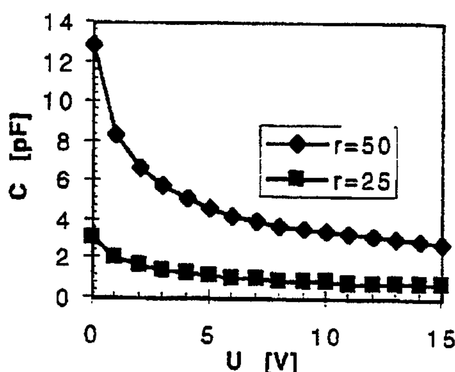

Fig 4. CV-data for two anode sizes, r=25 and 50 μm. $C_{0,25\,\mu m}$=3.13 pF, $C_{0,50\,\mu m}$=12.9 pF

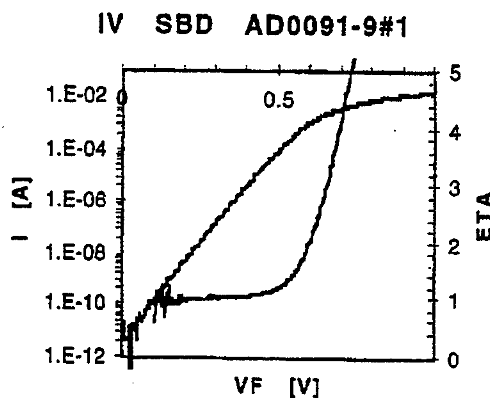

Fig 5. I-V data for a 25 μm 4H-SiC SBD in the forward direction.

I-V measurements gives $I_0=7.9\cdot10^{-12}$ A, η=1.10 and a series resistance for a r=25 μm diode of R_S=19 Ohm, which is higher than the simulated value of R_S=2.24 Ohm. Making a measurement of the differential resistance using a four probe measurement yielded a better estimate of R_S. These measurements were performed for SBDs of different radii (10-50 μm) and gave a R_S dependence on radius in μm as: $R_S=99.3(1/r)^2+54.4(1/r)$ Ω. Theoretically the R_S formula should have been: $R_S=106(1/r)^2+51.8(1/r)$ Ω.
The measured value for a SBD of r=25 μm was 2.47 Ohms. The leakage current in the reverse direction was found to be less than 150 μA at -40V. Reverse leakage currents was found to be consistent with tunneling calculations made using a WKB evaluation of the tunneling probability through a reverse biased Schottky barrier and numerically integrating over all energies[9].

The barrier height (from J_0) was ϕ_{Bn}=0.90 eV with an image force lowering of $\Delta\phi_{Bn}$=0.09 eV.

IV. CONCLUSIONS

The cut off frequency for a diode with r=25 μm was measured to be 20 GHz which is lower than expected (24 GHz). This f_{cut} value is to our knowledge the highest reported for any SiC-Schottky diode and can be further increased by decreasing the anode-area. A f_{cut} consistent with the measured R_S dependence on radius gives f_{cut} =84 GHz for r=5 μm. In the near future we will investigate mixer and detector applications, burn out behavior, high temperature performance, and further optimization of the cut-off frequency.

Acknowledgment

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Modeling of the Heterostructure Barrier Varactor diode

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Introduction

Power sources at frequencies in the millimeter- and submillimeter wavelength range (0.03-3 THz) are needed as local oscillators for mixers. Submillimeter waves are used in research applications like radio astronomy, while millimeter waves are now also used in commercial applications.

To provide power in the submillimeter wavelength range, a multiplier using a reverse biased Schottky diode is commonly used. When the Schottky diode is pumped with a sinusoidal signal, its non-linear capacitance generates harmonics and an external circuit extracts the desired harmonic. An alternative method to produce power is to use direct generators such as Gunn oscillators, but decreasing efficiencies and shrinking dimensions make the out-put power decrease rapidly with increasing frequency. Therefore, varactor frequency multipliers are normally employed in this wavelength range.

A promising symmetric varactor is the Heterostructure Barrier Varactor (HBV) diode [1]. An undoped high band gap semiconductor (barrier) is sandwiched between two moderately n-doped low band gap semiconductors. The barrier prevents electron transport through the structure. Since the HBV has a symmetric C-V characteristic and an anti-symmetric I-V characteristic, it will only produce odd harmonics in a frequency multiplier. For a frequency tripler, only the circuit impedances at the input frequency and the output frequency are of major importance. In contrast, for a tripler circuit using a Schottky diode, also the impedance at the second harmonic (idler) must be matched to convert a reasonable amount of the pump power to the third harmonic. Moreover, it is possible stack several single barrier HBV diodes epitaxially for a high power capability and a low capacitance per unit area.

Simulations of HBV multipliers have predicted high efficiencies, but experimental HBV multipliers have so far shown efficiencies considerably below the efficiencies of the best Schottky varactor multipliers. To make more accurate multiplier simulation possible we are here presenting novel capacitance and conduction current models which easily can be used in large signal simulations.

Capacitance-voltage model

If an abrupt space charge is assumed, the voltage over an HBV with homogeneously doped depletion layers can be calculated from Poison's equation to

$$V(Q) = N\left(\frac{bQ}{\varepsilon_b A} + \mathrm{sign}(Q)\left(\frac{Q^2}{2eN_d\varepsilon_d A^2}\right)\right) \tag{1}$$

where N is the number of barriers, b is the barrier width including undoped spacer layers, Q is the charge stored in the varactor, e is the elementary charge, A is the device area, N_d is the doping concentration in the depletion layer, ε_d is the dielectric constant in the depletion layer, ε_b is the dielectric constant in the barrier. The capacitance can be

calculated as dQ/dV. Equation (1) is not valid for a small bias where screening effects around the barrier decreases the capacitance. The capacitance for zero volt bias, C_0, can be calculated using the theory for a surface space charge region in thermal equilibrium [2] to

$$C_0 = \frac{A\varepsilon_b}{b + 2\frac{\varepsilon_b}{\varepsilon_d}L_d} \quad \text{where} \quad L_d = \sqrt{\frac{kT\varepsilon_d}{N_d e^2}} \tag{2}$$

is the Debye length for electrons. To model the screening effects for small bias an empirical term is added to equation (1), which gives the following novel voltage-charge model for an HBV diode:

$$V(Q) = N\left(\frac{bQ}{\varepsilon_b A} + \operatorname{sign}(Q)\left(\frac{Q^2}{2eN_d\varepsilon_d A^2} + \frac{4kT}{e}\left(1 - e^{-|Q|/(2L_d AeN_d)}\right)\right)\right) \tag{3}$$

Equation (3) gives the C_0 from equation (2) and that dC/dV=0 for zero bias.

We have measured 2 barriers HBV diodes from the material UVA-NRL-1174. The epitaxal structure's active layers are shown in table I. It can be seen in figure 1 that the C(V) characteristic generated from equation 3 agrees very well with the measured C(V) characteristic.

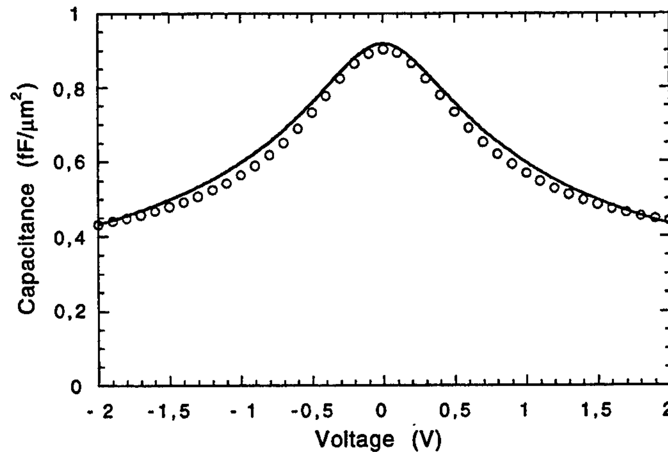

Figure 1: Capacitance-voltage characteristic generated from equation 4 compared with experimental capacitance-voltage characteristic measured at 18 MHz.

Table I

UVA-NRL-1174 HBV Material Structure (only the active layers are shown)

Layer Thickness	Layer doping	Material
2500 Å	$8 \cdot 10^{16}$	GaAs
35 Å	i	GaAs
200 Å	i	$Al_{0.7}Ga_{0.3}As$
35 Å	i	GaAs
5000 Å	$8 \cdot 10^{16}$	GaAs
35	i	GaAs
200 Å	i	$Al_{0.7}Ga_{0.3}As$
35 Å	i	GaAs
2500 Å	$8 \cdot 10^{16}$	GaAs

Conduction current model

A varactor is a much more efficient frequency converter than a varistor. Consequently, the conduction current in an HBV should be as low as possible. Since a considerable amount of power is dissipated in the diode, its temperature will increase and it is therefore not sufficient to characterize its conduction current at room temperature. The conduction current can be calculated by self-consistently solving the Poisson/Schrödinger equations [3]. However, such calculations are time consuming and for multiplier simulations, it is convenient with a simple analytical expression. The conduction current through an HBV diode is well described with the simple empirical model

$$J = aT^2 \mathrm{Sinh}\left(\frac{E_b}{E_0}\right) e^{-\Phi_b/kT} \tag{4}$$

where E_b is the electric field in the barrier and a, E_0 and Φ_b are constants. The electric field in the barrier can be estimated from Poison's equation to

$$E_b = \frac{N_d e \varepsilon_d b}{\varepsilon_b^2}\left(\sqrt{1+\frac{2V\varepsilon_b^2}{N_d e \varepsilon_d b^2 N}}-1\right) \tag{5}$$

where V is the voltage applied over the diode.

We have measured UVA-NRL-1174 HBV diodes at different temperatures. The measured and modeled conduction currents are shown in figure 2. The curves are extracted from equation (4) with $a=170\ A/(m^2K^2)$, $E_0=4.2\ 10^6$ V/m and $\Phi_b=0.17$ eV.

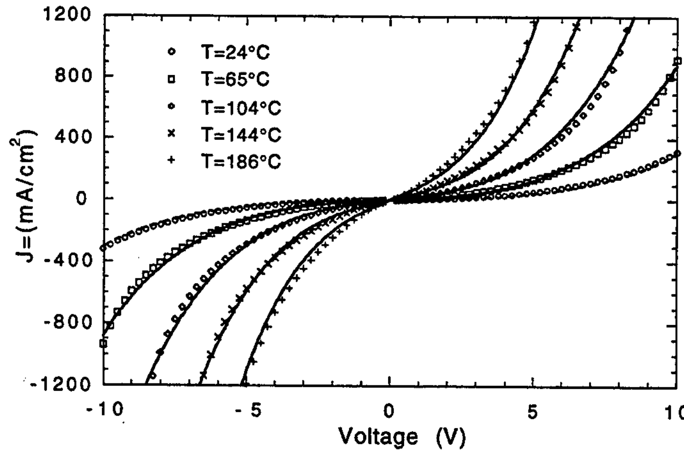

Figure 2: Measured and modeled conduction current density through a 4 barriers HBV diode (UVA-NRL-1174 with two diodes in series).

If the thermal conductance is assumed to be temperature independent, and the dissipated power is approximated to be proportional to the input power, P_{in}, the increase of the temperature is proportional to the input power. Figure 3 shows simulated efficiencies for a 3x78 GHz multiplier. For the upper curve, a constant temperature of 25°C is assumed, and for the lower curves the temperature is assumed to increase linearly with the input power.

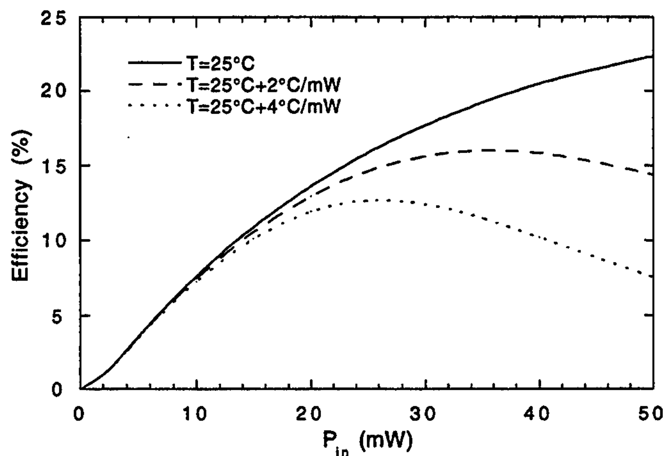

Figure 3: Simulated efficiencies of a 3x78 GHz multiplier using a 32 μm² 4 barriers UVA-NRL-1174 HBV diode. In the upper curve, a constant temperature of 25°C is assumed, and in the dotted curves the temperature is assumed to increase 2°C/mw input power and 4°C/mw input power respectively. Optimum embedding impedances are assumed and the series resistance is assumed to be 30 Ω. Losses in the embedding circuit are not included.

It can be seen in figure 3 that the heating of the diode decreases the efficiency at high input powers, which is in agreement with experimental HBV multipliers [1, 4]. Since also the series resistance is temperature dependent, the degradation of the efficiency due to heating can be expected to be even larger than as shown in figure 3.

The conduction current can be decreased if the barrier height is increased, e.g., by inserting a thin AlAs layer in the middle of the barrier. Furthermore, thermal properties must be considered when designing the diode mount.

The thermal resistance of a planar diode is generally higher than for a whisker contacted diode where the heat efficient can be conducted from the diode through the substrate to a heatsink. Consequently, a planar diode will reach a higher temperature. This is one explanation to why it is generally more difficult to achieve a high multiplier efficiency using a planar diode.

Acknowledgment

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Analysis of Carrier Transport in a Heterostructure Barrier Varactor Diode Tripler

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Abstract - We report the time evolution and the spatial variation of the conduction band, the electric field, and the carrier density for a GaAs/$Al_{0.7}$GaAs Heterostructure Barrier Varactor diode operating in a 3x90 GHz frequency tripler. The third harmonic output power and optimal embedding impedances are given for two different diodes at pump powers of 50 mW and 100 mW.

I. Introduction

The Heterostructure Barrier Varactor (HBV), first proposed in 1989 [1], is a promising device for high efficiency frequency multiplication in the millimeter to submillimeter wavelength range. An undoped high band gap semiconductor (barrier) is sandwiched between two moderately n-doped low band gap semiconductors. The barrier prevents electron transport through the structure. Because of the symmetric C-V and the anti-symmetric I-V characteristic, only odd harmonics of an applied sinusoidal signal is produced, thus simplifying the design of a frequency tripler/quintupler.

Non-linear quasi-static device models have for a long time been used to predict the performance of varactor multipliers. However, in the submillimeter wavelength range, where inertial effects and the limit speed of electrons becomes important, such models starts to be inadequate. Development of large-signal circuit simulators integrated with time-dependent numerical device models is therefore needed.

With the aim to increase the conversion efficiency of HBV diode multipliers, a Drift/Diffusion device model integrated with a Harmonic Balance circuit simulator (DDHB) [2] is used, a powerful tool to analyze the carrier transport while the device is operating as a frequency multiplier.

II. Device Simulation Technique

Carrier transport through the active regions of the HBV is modeled by solving the electron continuity equation (1), the drift/diffusion equation (2), and the Poisson equation (3) self consistently. The resulting equations describing DC and time dependent transport are formulated as

$$\frac{\partial n(x,t)}{\partial t}=\frac{1}{q}\frac{\partial J_n(x,t)}{\partial x}, \qquad (1)$$

$$J_n(x,t)=-q\mu_n(x,t)n(x,t)\frac{\partial \phi_n(x,t)}{\partial x}, \qquad (2)$$

and

$$\frac{\partial}{\partial x}\left[\varepsilon(x)\frac{\partial \psi(x,t)}{\partial x}\right]=q\left[n(x,t)-N_D(x)\right], \qquad (3)$$

where

$$n(x,t)=n_{i,ref}e^{\frac{q}{kT}(\psi(x,t)+V_n(x)-\phi_n(x,t))}, \qquad (4)$$

and where J_n is the electron current density, n is the electron density, ϕ_n is the electron quasi-Fermi potential, ψ is the electrostatic potential, k is the Boltzmann's constant, q is the electron charge, T is the absolute temperature, $n_{i,ref}$ is the intrinsic electron density in the reference material (GaAs), and V_n, μ_n, N_D, and ε are the spatially-dependent alloy potential, electron mobility, donor impurity concentration, and dielectric permittivity, respectively.

The integrated DDHB simulator calculates the time-domain current for a given HBV layer structure, incident pump power level, and embedding impedances seen by the diode. Seven harmonics plus the DC term has been utilized in this work. The employed DDHB simulator with proper boundary conditions is well described in [2].

TABLE I
HBV LAYER STRUCTURE

Layer	Material	Doping [cm^{-3}] Diode I/II	Thickness [Å] Diode I/II
9	InAs	5×10^{18}	100
8	$In_{1\rightarrow 0}GaAs$	5×10^{18}	400
7	GaAs	5×10^{18}	3000
6	GaAs	$8\times10^{16}/1\times10^{17}$	2500/2250
5×4	GaAs	Undoped	35
4×4	$Al_{0.7}GaAs$	Undoped	200
3×4	GaAs	Undoped	35
2×4	GaAs	$8\times10^{16}/1\times10^{17}$	2500/2250
1	GaAs	5×10^{18}	40000
0	GaAs	SI	-

III. RESULTS AND DISCUSSION

Two four barrier HBVs (the epitaxial structures are shown in Table I) have been analyzed with the DDHB simulator. The pump frequency was 90 GHz and the device area 66 μm^2. All simulations were performed by assuming a homogenous temperature of T=300 K across the active device region. A field-independent (low field) electron mobility of 4375 cm^2/Vs in the GaAs region and a calculated extrinsic parasitic series resistance of 4.9 ohm were used. Intrinsic losses, e.g. ohmic losses in layers (No. 2,6), are fully taken into account by the DDHB simulator.

Near optimum fundamental, Z_1, and third-harmonic, Z_3, circuit embedding impedances have first been estimated from an in-house harmonic balance program. This code uses a quasi-static analytical device model [3]. These impedances were then further optimized for maximum conversion efficiency with the DDHB simulator. The output power at the third harmonic and the optimal embedding impedances are shown in Table II. The remaining circuit embedding impedances have been set to short-circuit impedances (1e-4 + j0 Ω) for simulation purposes.

The trajectories during a pump cycle in the current-voltage plane with optimum tripler embedding impedances are shown in Fig. 1.

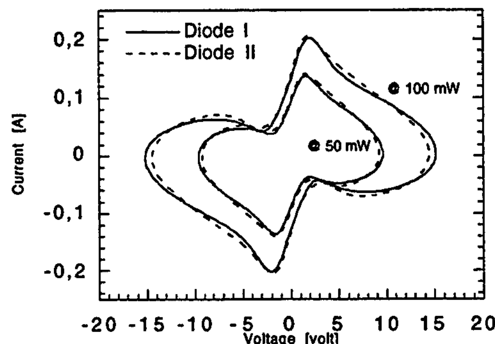

Fig. 1. Current versus voltage during one pump cycle.

The conduction band, the electric field, and the carrier density for diode II pumped at 100 mW are shown in Fig. 2 and Fig. 3d. The electric field changes linearly with distance across the depletion region as expected for a homogeneously doped layer. It is important to notice that the low carrier concentration (~10^{13} cm^{-3}) in the high field region results in an unreasonable high carrier velocity (~10^9 cm/s) by using the field-

TABLE II
OPTIMAL EMBEDDING IMPEDANCES

	DIODE I			DIODE II		
P_{AVA} [mW]	Z_1 [ohm]	Z_3 [ohm]	P_3 [mW]	Z_1 [ohm]	Z_3 [ohm]	P_3 [mW]
50	15+j100	21+j40	11	13+j90	18+j37	10
100	18+j119	27+j47	28	15+j106	23+j44	27

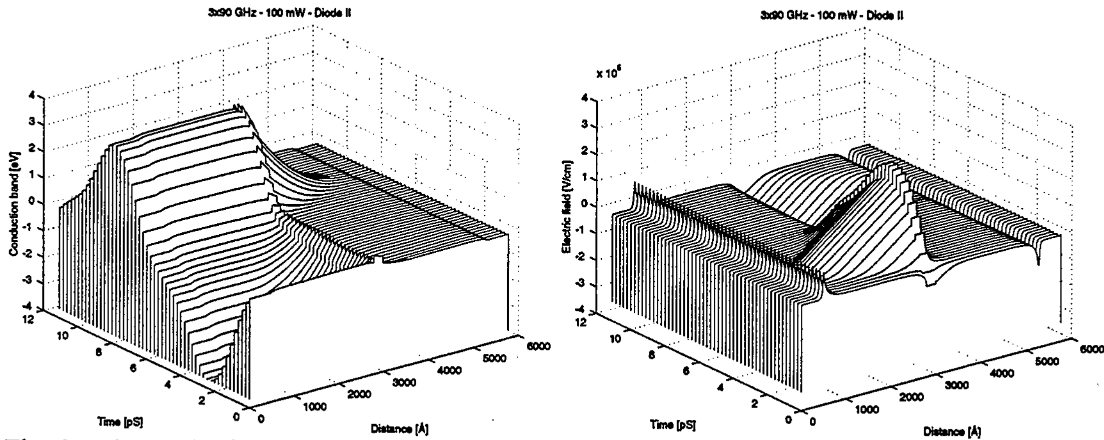

Fig. 2. The conduction band (left) and the electric field (right) versus time and distance for diode II at an incident pump power of 100 mW.

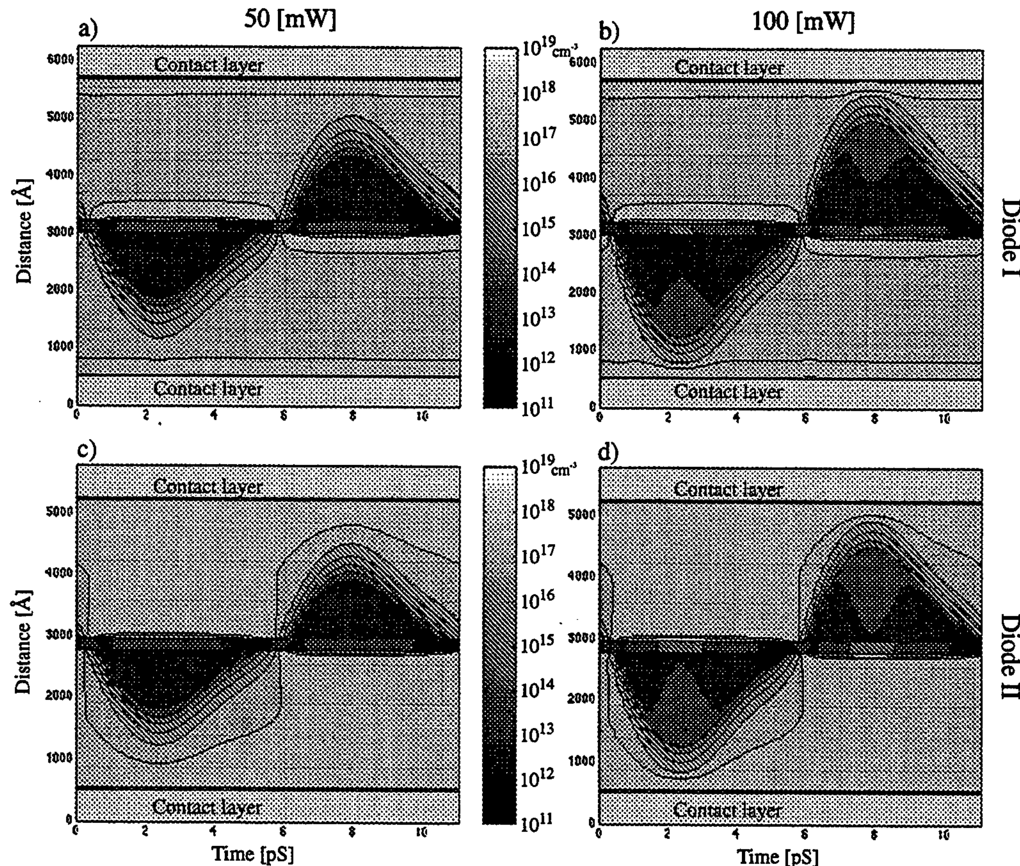

Fig. 3. Contour plot (log scale) of carrier concentration versus time and distance for two different power levels and the two diodes described in Table I-II. Contour lines are at a carrier density of 10^{11}, 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16}, 5×10^{16}, 10^{17}, 5×10^{17}, and 10^{18} cm^{-3} respectively.

independent mobility model. However, the effect on the electric field distribution in the high field region would be very small if current saturation [4] is taken into account ($J = q\, n\, v_{max}$), e.g. through a field-dependent mobility. The depletion edge, however, would be distorted. Moreover, it is clear that the depletion edge is very close to the contact region (punch through) when operating at an incident power of 100 mW.

For comparison, the carrier densities for the two diodes pumped at 50 mW and 100 mW are shown in Fig. 3. Since the elastance, $S=dV/dQ$, is directly proportional to the extension of the depletion region, diode I exhibit a higher elastance swing, S_{max}/S_{min}, during the pump cycle and is therefore more

efficient in a multiplier. This is due to a lower doping and a thicker depletion layer. However, since lower doping and thicker depletion layers also means increased losses, diode II converts almost as much of the pump power to the third harmonic as diode I, see Table II. Notice also the increase in the carrier concentration in the depleted region when both diodes are pumped at 100 mW, see Fig. 3b,d. This is due to thermionic emission and tunneling of carriers across the barrier. However, the carrier injection into the depletion region is too low to noticeably change the spatial variation of the electric field, see Fig. 2 (right).

Diode I corresponds to the HBV diode UVA-NRL-1174, which has been fabricated into a planar geometry and tested experimentally in a 3x80 GHz frequency tripler [5]. The conversion efficiency obtained was 2.5% with an available power of 50 mW. The large discrepancy between simulated efficiency of 22 %, see Table II, and experimental can partly be explained by an increase in temperature. This would affect the conduction current through thermionic emission but also the series resistance (see Dillner et al. this conference).

IV. Conclusions

In spite of the fact that the barrier height is rather low, see Fig. 2 (left), even a large increase in temperature, e.g. T=400K, would have a small effect on the electric field distribution. The carrier concentration would only change a factor of ten in the depletion region and, thus, still be below 10^{15} cm^{-3}. This means that a conventional quasi-static analytical device model is still valid. However, an increase in temperature will deteriorate the multiplier performance. Furthermore, it is important to further study the high frequency performance by taking into account saturation effects. Hence, to optimize HBVs for terahertz frequencies, the physical large-signal simulator will be essential.

Acknowledgment

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INFLUENCE OF A PROFILE OF THE DISTRIBUTION OF IMPURITIES IN A INJECTING LAYER AND TRANSIT REGION ON THE MICROWAVE CHARACTERISTICS OF BÀRITT DIODES

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In spite of the fact that the active properties of the injection-transit-time diodes (ITTDs) in basic are determined by transit effects, they largely depend on a condition of an injecting contact, distributions of impurity atoms, dislocations, centers of capture in the transit region and etc [1]. A deviation of these parameters from required values for the ITTD normal functioning inevitably result in that such parameters as the efficiency of injection, drift velocity in the transit region, density of an average current, time of flight also vary. These changes to a greater or lesser extent influence on static and dynamic characteristics of the device. For example, the influence of traps on the HF characteristic of ITTDs is considered by us in papers [2,3]. Here a case of an influence on the static and dynamic characteristics of ITTD of non-uniform (linear) distribution of the doping of the impurity on the transit region length (part I) and another non-uniform (exponential) distribution of the doping of the impurity in the injecting contact (part II) is analyzed.

Part I. We shall consider a p^+- n- p^+ silicon structure (Fig.1a), where it is supposed that in the n-type transit region a gradient of the doping impurity concentration is available and simultaneously at a forbidden gap of the n- semiconductor traps for injected holes are present. A non-uniform doping of the impurity creates an internal static electric field which has the converse direction to an applied from the outside displacement field of the diode and, hence, can affect on the velocity of injected holes and, thus, on the microwave characteristic of ITTD.

We shall assume that the concentration of the impurities in the n- layer changes under the law (Fig. 1b):

$$N_q(x) = N_{q_1} + a_1 \frac{x}{L}, \qquad a_1 = N_{q2} - N_{q1}, \tag{1}$$

In the equilibrium condition (U=0) the intensity of an internal field will be equal

$$E_{in} \approx \frac{kT_o}{q} \cdot \frac{1}{N_q(x)} \cdot \frac{dN_q(x)}{dx} \approx \frac{a_1 \varphi_T}{(LN_{q1} + a_1 x)}, \tag{2}$$

Here $\varphi_T = \frac{kT_o}{q}$, $0 \le x \le L$, k is the Boltzman constant, T_o is the absolute temperature, q is the charge of electron.

We shall assume, that all impurity are completely ionized and the concentration of holes near the potential barrier submits to the Boltzman statistics. For the Poisson equation we have:

$$-\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon}\left[N_q(x) + P + P_o\right], \quad 0 \le x \le x_m, \tag{3}$$

where x_m is the depletion region length, $P \approx N_A exp\left(-\frac{q\psi}{kT_o}\right)$, ψ is the electrostatic potential, N_A is the concentration of acceptors in the p^+ layer, P_{+o} is the concentration of holes captured on the traps in an interval $0 \le x \le x_m$. From the kinetic equation describing a change in the time of the concentration holes P_{+o} captured on the traps in an equilibrium condition, we obtain [3]

$$P_{+o} \approx \frac{P_o N_t}{P_o + P_t}, \tag{4}$$

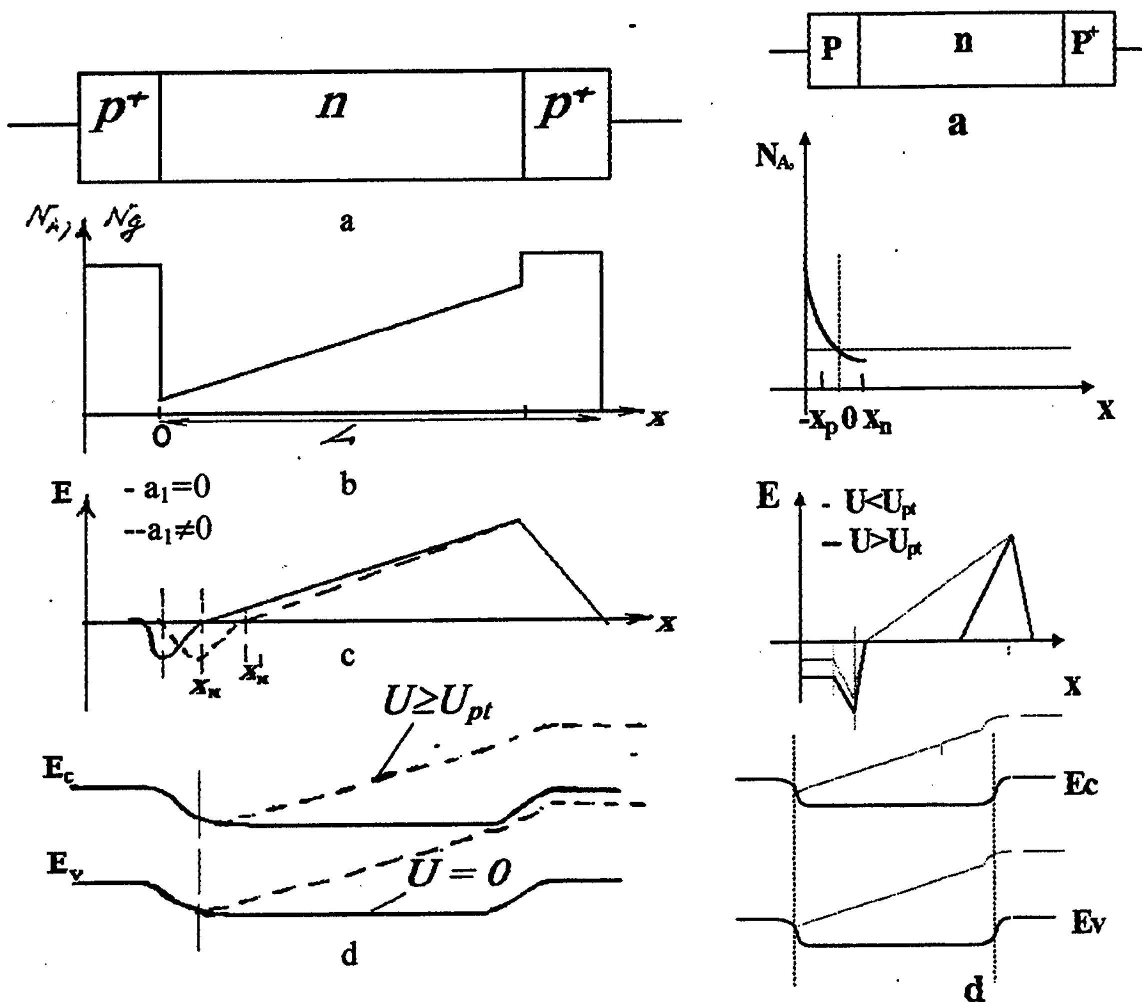

Fig.1. Structure (a), distribution of impurity (b), electrical field (c) and band diagram (d) of ITTD.

Here P_0 is the equilibrium concentration of holes in $0\leq x\leq x_m$ layer, P_t is the Schockly-Read statistical factor for holes, $P_t = N_v\, exp\left(-\dfrac{E_F - E_t}{kT_o}\right)$, E_F is the energy a Fermi, E_t is the energy difference between traps and valence band, N_t is the concentration of the traps. Then at $P_o << P_t$ we have:

$$-\frac{d^2\Psi}{dx^2} = \frac{qN_A}{\varepsilon}\left[R + \frac{a_1 x}{N_A L} + \beta e^{-q\Psi/kT_o}\right], \tag{5}$$

where $\beta = 1 + \dfrac{N_t}{P_t}$, $R = \dfrac{N_{q1}}{N_A}$.

Solving the equation (5), under boundary conditions: $x = x_m$, $\psi = -\varphi_k$, φ_k is the difference of contact potentials, and ignoring the potential drop in the P^+ - layer, we receive expressions for the electrostatic potential and field, analysis of which shows that, with growth of $\beta\,(N_t)$ and a_1, the point x_m (the plane of the maximum barrier) penetrates inside of the n- region. In result, the length of the region $0 \div x_m$ is increased. Here the electrical field has opposite sign ("braking" influence) to the applied field and holes in this region will move very slowly. At the application of the alternating signal, holes will be injected through the potential barrier and to test "braking" influence of internal static electric field before the external applied field does not quickly grow.

Using a technique of calculations of the microwave characteristics of ITTDs with the traps, advanced in [2], for the alternating component of the voltage U_1 on the diode we receive:

$$\frac{d^2U_1}{dt^2}+\xi\frac{dU_1}{dt}-bx\frac{dU_1}{dt}=-\frac{I_1 v_o}{\varepsilon}\beta, \tag{6}$$

which is a non-uniform nonlinear equation, where $\xi = j\omega\beta - \omega_1 = j\omega_o - \omega_1$, $b = \dfrac{q\mu_p a_1}{\varepsilon L}$, $\omega_1 = \dfrac{q\mu_p N_{q1}}{\varepsilon}$,

ω is the angular frequency of a signal, μ_p is the mobility of holes, ε is the dielectric constant of the semiconductor, x is the current coordinate in the flight interval *0-L*.

Solving the equation (6) we receive the expression for the small-signal impedance Z of the device

$$SZ = -\frac{U_1}{I_1} = R - jX$$

where S is the cross - section of the device, $R = R_p + R_{rp}$, $X = X_p + X_{rp}$, R_p, X_p, R_{rp}, X_{rp} are active and reactive components of the impedance at the uniform and non-uniform (with a gradient) distribution of the impurity in the n- layer, accordingly. Expressions for *Rp* and *Xp* coincide with the appropriate equations, received by us earlier in Ref. [1]and their analysis did not carry out here.

Is of interest the analysis of the R_{GR} component which is caused in result of the non-uniformity doping of n-region. The analysis of the expressions for R_{GR} shows, that R can also accept negative values at the flight angels θ satisfying the inequality

$$\frac{2{,}35}{\beta}<\theta<\frac{5{,}6}{\beta}. \tag{7}$$

"Uniform" component R_p, as it is shown in Ref.[2] accepts negative values at the flight angels θ:

$$\frac{3{,}6}{\beta}<\theta<\frac{6{,}6}{\beta}. \tag{8}$$

It is follows from Eqs. (7) and (8) that at certain θ the ranges of the DNR occurrence for both components are overlaped. It means that at corresponding θ and a_1, with other things being equal it is possible to increase considerably the DNR value in ITTD on absolute value. DNR on absolute value is increased also with the increas of the concentration of the traps, but thus a frequency region of an origin DNR is narrowing and displaced to lower frequencies [2]. Hence, combining two ways of the change of the HF parameters of ITTDs with the help of the traps and the profile of the impurities in the transit region it is possible considerably to increase the DNR on absolute size.

Part II. At the analysis of the HF characteristics of ITTDs in the above-stated cases it was supposed that the injecting contact presents it self a similar high doped layer, width of which is much less than the transit length. At the analysis the fall of the static and HF field in the contact region was neglected, it is considered that the alternating HF field in the injecting contact modulates only the velocity of charge carriers. It is supposed that at a small level of injection, the change of the width of the p-n junction under influence the amplitude of the alternating signal can be neglected. It is clear that all these assumptions are more or less idealized. In this section we analyzed the influence of the non-uniform (exponential) distribution of the doping impurity in the injecting contact region on the microwave characteristic of ITTD. We shall consider the *p- n - p +* structure, in the *p* - layer of which with length λ a gradient of the impurity doping, varied under the law, is available (Fig.1b).

$$N_A(x) = N_{A_1}\exp\left(-\frac{ax}{\lambda}\right). \tag{9}$$

Here a is the parameter determining a gradient of impurities, λ is the characteristic length.

The non-uniformity of the impurity distribution in the p - layer creates a internal static electric field, which having a direction converse to the field applied from the outside, and no doubt, will affect the values of the velocity and efficiency of the injection. The plane of the maximum of the potential barrier will tend to be displaced partly in the *p* - layer. Here it is necessary to take into account the modulation of the width of the p-n junction under influence

of the alternating field and the potential drop in the p - layer. The reduction of the voltage on the injecting contact during the negative half-cycle of the alternating signal will be accompanied by an increase of the "static" width of the p-n junction, corresponding $U=U_{pt}$, where U_{pt} is the punch-through voltage of the p-n junction. The flight angle also will change in comparison with the "static" angle. The actual flight angle will also depend on the amplitude of the alternating voltage U_1. The internal static field in a vicinity of the plane of the injection will render "braking" action on the injected holes. This influence is reduced to a decrease of the acting amplitude of the alternating field that will be accompanied by a decrease of the alternating current. The change of the width of the p-n junction under influence of the alternating voltage will be the reason also of a partial HF modulation of the injected holes concentration. Presence of the internal static field results in that the increase of the electrical field in the vicinity of the plane of the injection will be, "to be slowed down", and the slow movement of holes in the beginning of the transit space results in larger delay of the phase between the alternating current and field and, thus, DNR on the absolute value promotes to increase. The calculations and analysis of the microwave characteristics at the assumption that in the plane of the injection, under influence of a the alternating field, the virtual cathode changes and will take place not only modulation of the holes velocity, but also a partial modulation of their concentration, shows that the condition of the DNR occurrence depends remarkable on the value of the relation x/λ. Numerical calculations show that with growth of the

$$\frac{x}{\lambda}=\frac{1}{a}ln\left[\frac{N_{A_1}}{N_A(x)}\right],$$

DNR absolute value is increased (Fig.2) in comparison with similar value for the $p^+ - n - p^+$ ITTD structure, where the p-layer is uniformly high doped. Note that at a=0 all results are reduced to the appropriate expressions received for the uniform distribution in the p^+ layer and receiving experimental confirmation [4,5].

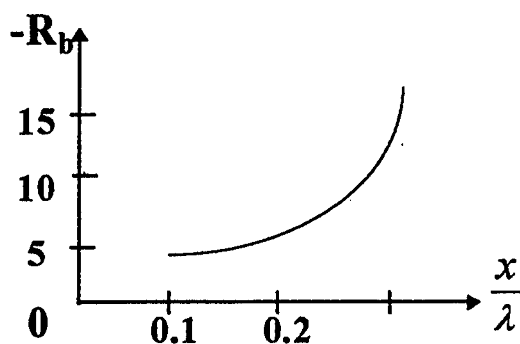

Fig.2 Dependence of DNR on x/λ for p-n-p$^+$ structute

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Design of a 0.6μm GaAs MESFET ASIC for 2.24 GHz Transceiver Applications

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Abstract
The paper describes the design of a complex GaAs integrated circuit using 0.6μm MESFET technology available from TriQuint Semiconductor.The circuit consists of a high speed 8-bit comparator,8-bit prescaler, IF mixer and a digital phase frequency detector for phase locked loop control. The Integrated Circuit is part of a high performance 2.24 GHz transceiver.

Keywords:GaAs,MESFET,High Frequency, Transceiver

1.0 Introduction

The GaAs ASIC is designed to work with a high performance transceiver system.The 2.24 GHz transceiver system is made up of a number of commercial ICs on a Printed Circuit Board(PCB).A full description of the transceiver system is beyond the scope of this paper. The chip receives a 2.24 GHz signal from the TQ9206 voltage controlled oscillator(VCO).This signal is phase locked to a low frequency reference(8.75MHz) signal.The VCO signal is divided by 256 by a synchronous 8-bit prescaler.The prescaled signal is frequency and phase locked to the reference signal using a charge pump PLL.A high speed 8-bit comparator compares the eight bits of the prescaler to the eight external digital inputs and generates a control pulse on match.This allows for digital phase control of the signal generated at 8.75 MHz.The IF mixer uses the 280 MHz and 70 MHz outputs of the counter to generate the 210 MHz IF reference signal.

GaAs technology is chosen for the implementation of this high frequency ASIC.A brief introduction of GaAs technology is given in the next section.Section 3 discusses the CAD tools used in the design process.Section 4 gives the details about the implementation,simulation results and layout of the basic blocks.The last section gives the conclusions and future work.

2.0 GaAs Technology

GaAs integrated circuit technologies are being rapidly developed for high frequency (> 2GHz) wireless communication systems.

Table 1 lists some of the important material parameters of GaAs and Si[1].

TABLE 1.Electronic properties of GaAs and Si at 300K

Property	Si	GaAs
Density (g/cm^3)	2.33	5.32
Relative dielectric constant	11.9	**13.1**
Energy Gap (eV)	1.12	**1.42**
Intrinsic Carrier Concentration (/cm^3)	1.45E+10	1.79E+8
Intrinsic Resistivity (ohm-cm)	2.3E+5	1E+8
Effective mass (m^*/m_e)		
electrons	0.98	0.067
holes	0.49	0.47
Mobility (cm^2/V-s)		
electrons	1500	**8500**
holes	450	400

The relatively large band gap makes it suitable for high temperatures.Its Intrinsic carrier concentration is low and hence the material is semi insulating.Since its resistivity is large, no special measures need to be taken to provide isolation between devices on the chip.It's high electron mobility gives rise to high cut-off frequency.

2.1 TQTRx Process

This mixed-signal GaAs IC has been fabricated using TriQuint Semiconductor's TQTRx process[2].TQTRx is a high performance GaAs E/D MESFET based process for RF transceiver applications. It has high performance

enhancement and depletion mode MESFETS for small signal and depletion mode power MESFET for power amplifier stages.The process cross section for E/D MESFET is shown in Fig 1.Single gate and dual gate configuration are supported.TQTRx features very high value capacitor for increased density and reduced die size.It also features precision NiCr resistors.N+ overlap diodes are supported.Thick plated gold is used for interconnections.The novel idea in this work is the use of this RF technology to design extensive digital and analog components.

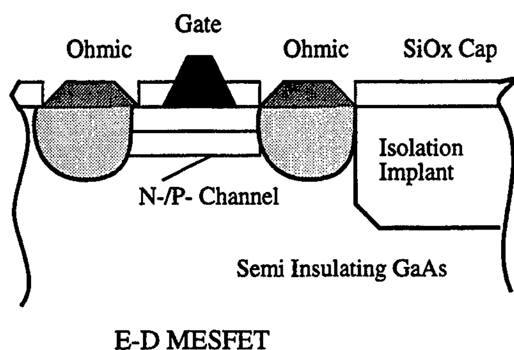

Fig 1: Process cross section

3.0 ASIC Design

3.1 Circuit Logic style

The core cells are designed using Source Coupled FET Logic (SCFL)[3], a fully differential logic family based on TriQuint's TQTRx process.SCFL logic uses differential amplifiers in a manner similar to silicon ECL to create digital logic functions.The basic transistor topology for SCFL AND/NAND is shown in Fig 2.A1, B2, C3 are the inputs and Y1, Y2, Y3 are the outputs. Source followers are included on the outputs to minimize loading of the SCFL circuit and to improve drive capability.Level shifting is required between stages to avoid driving the differential amplifier transistors into the ohmic regions.

The reduced sensitivity to threshold voltage variation, higher speed, high functional equivalence are strong advantages of SCFL when compared with many of the other circuit styles.All the basic digital gates and D Flip flop and I/O cells are designed using this logic style.The I/O cells are used to convert the logic levels between the GaAs and CMOS chips and vice-versa.These standard core cells are used to build up the entire chip.

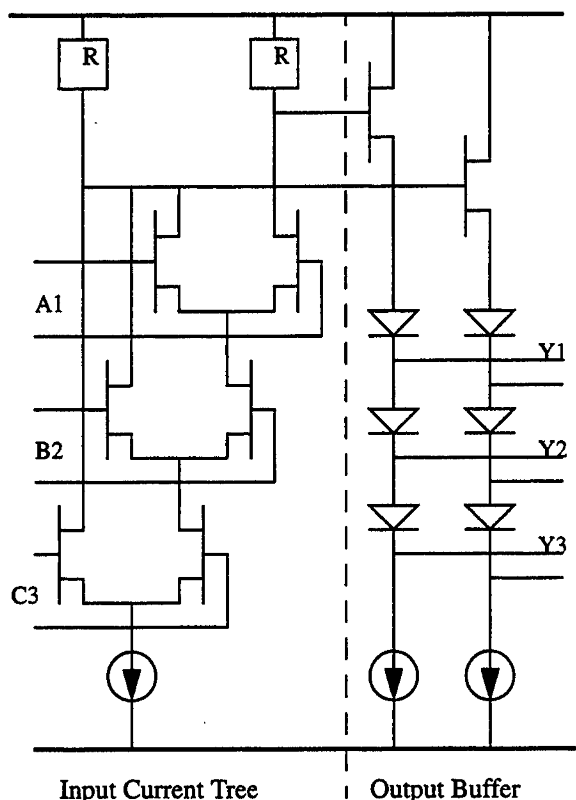

Fig 2: SCFL Circuit Topology

3.2 Input RF circuit

The Input RF circuit takes the 2.24 GHz VCO small signal and conditions the signal to be able to trigger the GaAs logic gates.This signal is used to clock the flip flops in the counter.This input RF circuit also acts as the clock driver.It is designed to minimize the clock skew associated with the distribution of clock to all the flip-flops in the counter.

3.3 8-bit Prescaler.

The prescaler is a 8-bit synchronous counter.It is divided into three blocks of two bits, three bits and three bits each.This breaks the carry chain and reduces the critical path delay.This technique is used to design counters

whose speed is independent of the counter length[4]. Since the first two bits have to run at very high frequency, a high speed 2-bit twisted tail counter, shown in Fig 3 is used. The subsequent two parts are 3-bit carry ripple synchronous carry ripple counters.This prescales the 2.24GHz input signal from the VCO.

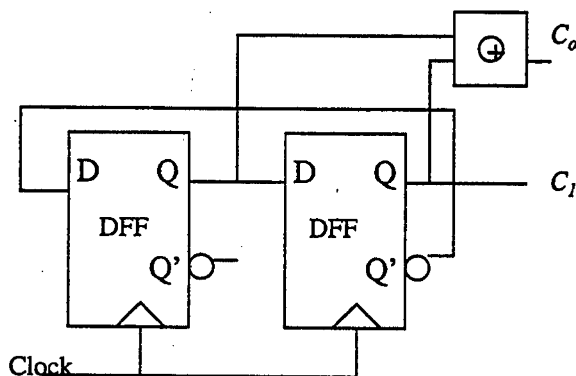

Fig 3 : High speed Twisted Tail Counter

3.4 8-bit Comparator

The 8-bit comparator is built with EXNOR and NAND gates.It compares the eight bits of the prescaler with the eight external digital inputs and generates pulse on match.These pulses are very narrow and cannot be used as such to trigger the external CMOS digital circuits.Hence they are stretched using a simple NOR gate based circuit.

3.5 IF Mixer

The IF reference output signal is generated using an EXOR based digital mixer. It takes the 280 MHz and 70 MHz signals from the output of counter to generate the 210 MHz IF reference.Some filtering is done off chip to eliminate the side bands.

3.6 Phase locked loop

The phase locking of the prescaled VCO signal is done using a charge pump based PLL[5].It uses a D-Flip flop based Phase frequency detector.The charge-pump consists of two MOSFETS.A low pass filter is also used in the loop.The charge pump and the filter are external to the chip.

4.0 Computer aided Design and Numerical Simulations

4.1 Simulation

GaAs MESFET is modeled using TOM2[6] model (TriQuint Own Model).This model applies over a large range of pinch-off voltages, allows size scaling of devices and is suited for modeling R_{ds} changes with frequency.Microsim Design Lab ™ is an integrated schematic capture and SPICE simulation engine with a graphical post-processor[7].It contains a built-in second generation TOM model for GaAs MESFETS.This has been used for the simulation of the circuits.
The digital gates and Flip-flops are simulated at the transistor level using SPICE.Three different models are used in the DC, AC and worst case analyses.The designs in the upper levels of hierarchy are also extensively simulated in SPICE.The simulation results verified the design.The simulation results of the high frequency first two bits is shown in Fig 4.

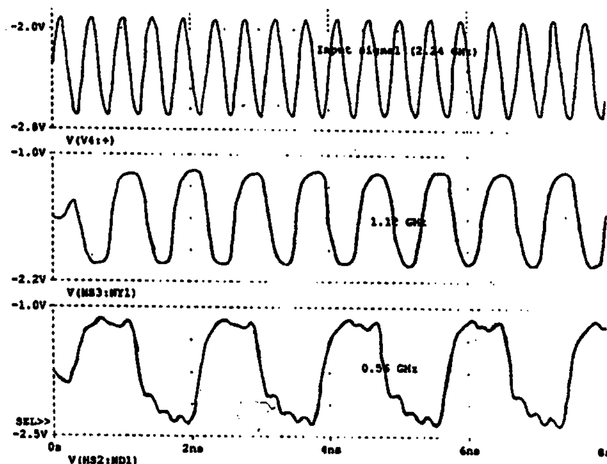

Fig 4 : Simulation results of the first two bits of Counter

4.2 Layout tools

The chip layout is done using ICED-32™[8].The design rule check is performed by IC Editors "The DRC", using the rule set from TriQuint.IC Editor's Netlist Extractor (NLE) is used for netlist extraction from layout and is verified with the schematic netlist using IC Editor's "LVS" tool.
The layout is done in a hierarchical manner.The core standard cells are first laid out and the more complex blocks are built from these standard cells.The thermal effects on the devices is taken into consideration while laying out the cells.The I/O pads are arranged properly and the high frequency RF lines are shielded using grounds on either side.On chip decoupling capacitance is added between power supply and ground.The layout of the complete chip is shown in Fig 5.

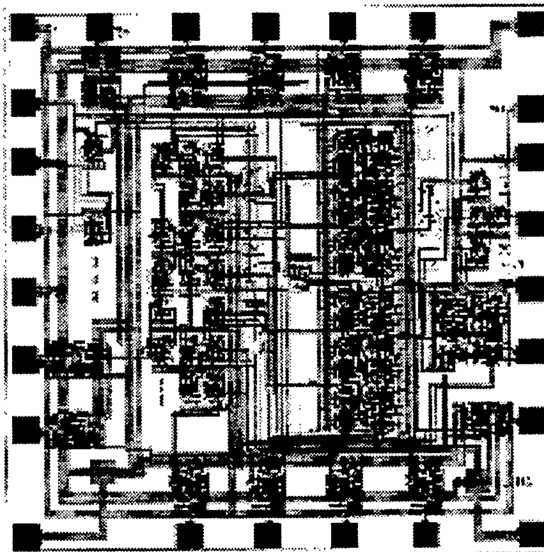

Fig 5 : Layout of the complete chip

5. Conclusions

This paper described all stages in the design of a GaAs MESFET ASIC for 2.24 GHz transceiver applicaions.All the blocks are simulated in SPICE using the state-of-the art second generation TOM model.The layout of the chip is completed. Design rule check is performed on the entire layout.LVS at the chip level is done.The chip will be sent for fabrication in the last week of Oct.The fabricated chip is expected back in the month of January.A printed circuit board is being designed to test this high frequency ASIC.

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Hot-Carrier Effects on High Frequency Performance of 0.8 μm LDD NMOSFETS

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This paper presents the first results on the effects on the hot-carrier (HC) stresses to the high frequency s-parameters and noise parameters of LDD NMOSFETs. Our experiments show that with increasing HC stressing times at the maximum substrate current bias, the minimum noise figure (NF_{min}), the equivalent noise resistance (R_n), the noise reflection coefficient ($|\Gamma_{opt}|$), the maximum frequency of oscillation (f_{max}) and the stability factor (K) all increase,while the unity gain frequency (f_T) decreases. These results have significant consequences for circuit designers using MOSFETs in high frequency analog circuits.

The rapid expansion of the wireless communication market in recent years has put a strong demand in low power and inexpensive microwave devices. The latest evolution in CMOS technology has made MOSFET a viable choice for RF applications, especially for frequency below 2 GHz. However, hot-carrier effects (HCE) have always been a major reliability issue for submicron MOSFETs. As the operating frequency moves higher, the effects of HC damages on MOSFET high frequency performance. In this work, we tested NMOSFET only because NMOSFET has better high frequency performance than PMOSFET. The device was fabricated in a BiCMOS technology. It has dimensions of 60μm/0.8μm, gate oxide thickness of 175 Å, sidewall spacer width of 0.2 μm, and an LDD phophorus implant dose of $2x10^{13}/cm^2$. The transistor was connected to ground-signal-ground style microwave probing pads in common-source configuration, with Port 1 being the gate and Port 2 the drain. For the hot-carrier experiment, the device was subjected to a maximum I_B stress (V_{DS} = 6 V, V_{GS} = 3 V). The small-signal s-parameters (f = 0.5 - 18 GHz, V_{DS} = 3 V), the noise parameters (f = 2 - 6 GHz, V_{DS} = 3 V), and the linear and the saturation I_{DS} *vs.* V_{GS} characteristics were measured at four different stress time: t_{stress} = 0, 10^2, 10^3 and 10^5 s. A dummy pad was prepared by separating a fresh device from its pad with a laser-cutting setup. The s-parameters of the device was calculated from the difference between the y-parameters of the raw data and that of the dummy pad.

Figs. 1 - 4 illustrate the magnitude of the four s-parameters of the device. Both |S11| and |S22| do not

change much (< 1%) with HC stress at $f < 4$ GHz. However, |S12| has a decrease of 14% and |S21| drops by 12.5% at 4 GHz. K for $V_{GS} = 1.5$ V was plotted in Fig. 5. The $t_{stress} = 10^5$ s curve crosses the K = 1 line at a frequency lower than other t_{stress} curves, which means the device reaches unconditional stability at lower frequency at higher stress time. Small-signal parameters at $V_{GS} = 1.5$ V were then extracted from 0.5 GHz to 10 GHz to obtain insights to the changes in s-parameters. Fig. 6 is the schematic of the small-signal model used, and Table 1 lists the parameters most affected by the hot-carrier stress. The decrease in g_m and g_{mb} and the increase in R_D could explain the decrease in |S21|. The gate-to-drain capacitance C_{GD} decreases by about 13%, which may explain the drop in |S12|. With the extracted parameters, f_T and f_{max}, were calculated and plotted in Fig. 7 and Fig. 8 respectively. f_T decreases by about 5% with $t_{stress} = 10^5$ s, but f_{max} increases over the stressing time. This increase is due to the decrease in both C_{GD} and f_T.

Figs. 9 - 11 are plots of NF_{min}, normalized noise resistance r_n, and $|\Gamma_{opt}|$ at $V_{DS} = 3$ V and $V_{GS} = 1.5$ V. NF_{min} and r_n show a similar trend in changes with respect to increasing stress time. The measured NF_{min} at 4 GHz increases by 23.5% and the measured r_n at 4 GHz increases by 41.7% after the 10^5 s hot-carrier stress; both are very significant increases. On the other hand, $|\Gamma_{opt}|$ increases slightly with increasing t_{stress} and this trend is most clear at higher frequencies.

In this paper, we have clearly demonstrated the effects of hot-carrier stressing on LDD NMOSFETs by giving representative results from a 0.8 µm device. We showed that HC stress can significantly degrade their high frequency characteristics- both AC and noise. Therefore, these effects should be carefully considered when using MOSFETs in high frequency analog circuits.

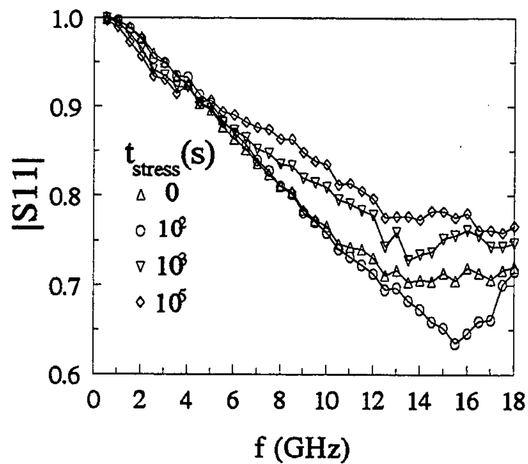

Fig. 1. |S11| at diffrent t_{stress}, V_{GS}= 1.5V, V_{DS}= 3 V.

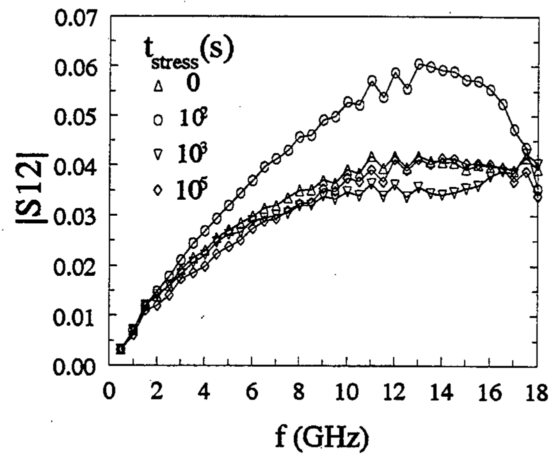

Fig. 2. |S12| at diffrent t_{stress}, V_{GS} = 1.5 V, V_{DS} = 3 V.

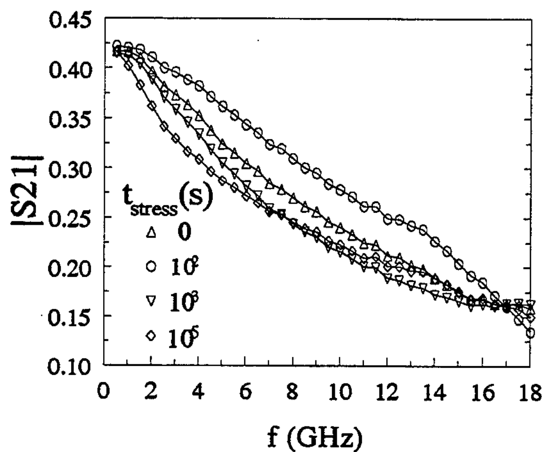

Fig. 3. |S21| at diffrent t_{stress}, V_{GS}= 1.5 V, V_{DS} = 3 V.

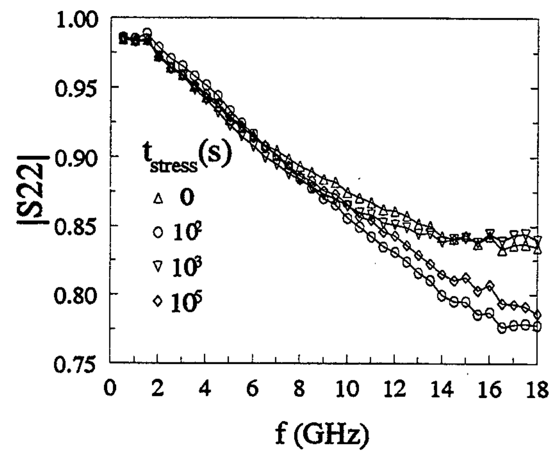

Fig. 4. |S22| at diffrent t_{stress}, V_{GS} = 1.5 V, V_{DS} = 3 V.

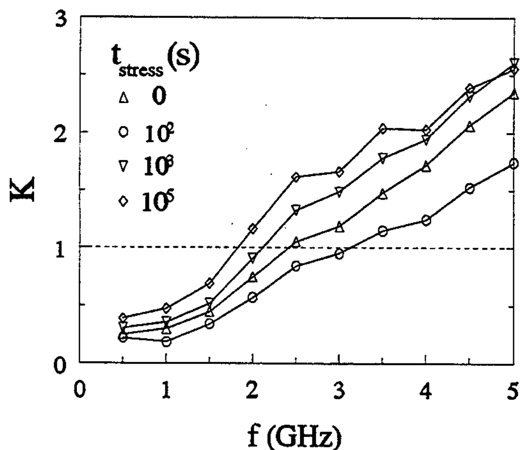

Fig. 5. Stability factor K at diffrent t_{stress}, V_{GS} = 1.5 V, V_{DS} = 3 V.

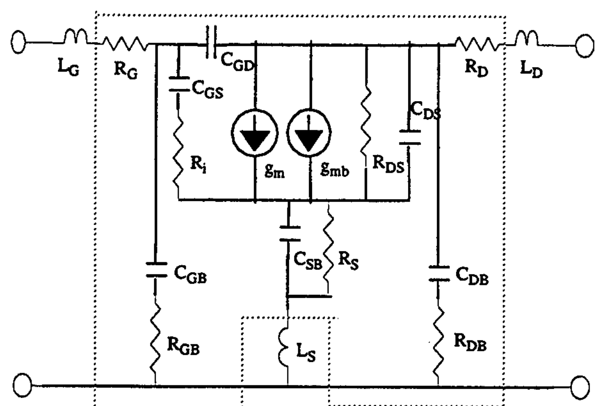

Fig. 6. High frequency MOSFET small-signal model. Intrinsic components are contained in dashed box.

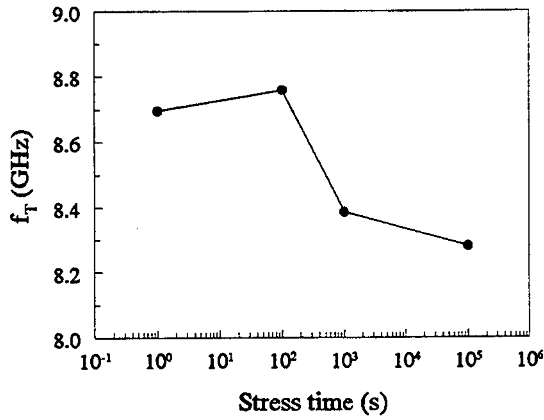

Fig. 7. f_T as a function of t_{stress} at V_{GS} = 1.5 V, V_{DS} = 3 V.

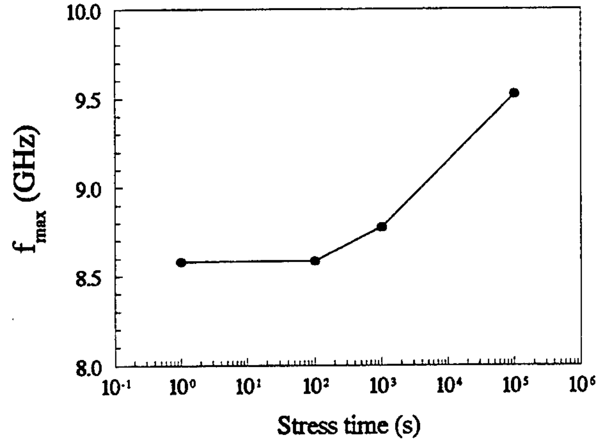

Fig. 8. f_{max} as a function of t_{stress} at V_{GS} = 1.5 V, V_{DS} = 3 V.

Table 1: Changes in small-signal parameters

	$t_{stress} = 0$ s	$t_{stress} = 10^5$ s
g_m (mA/V)	4.28863	3.76895
C_{GD} (fF)	10.0866	8.83141
C_{GS} (fF)	67.0091	62.2156
R_D (Ω)	20.38	30.57
g_{mb} (mA/V)	0.70448	0.61902

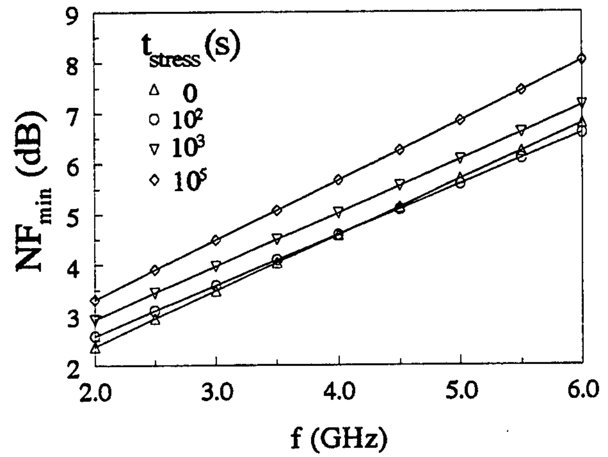

Fig. 9. NF_{min} at diffrent t_{stress}, V_{GS} = 1.5 V, V_{DS} = 3 V.

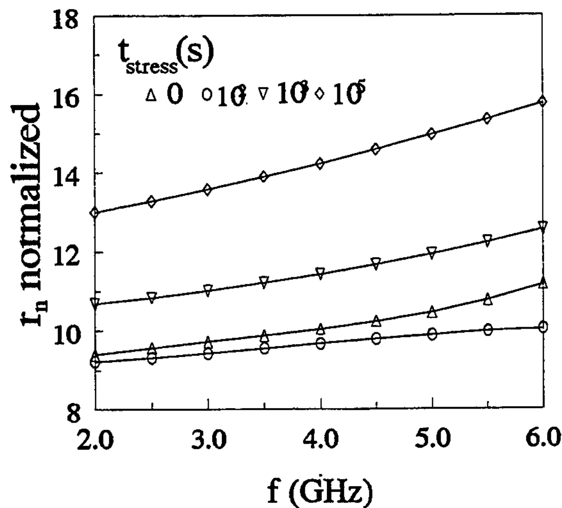

Fig. 10. Noise resistance r_n at diffrent t_{stress}, normalized at 50 Ω, V_{GS} = 1.5 V, V_{DS} = 3 V.

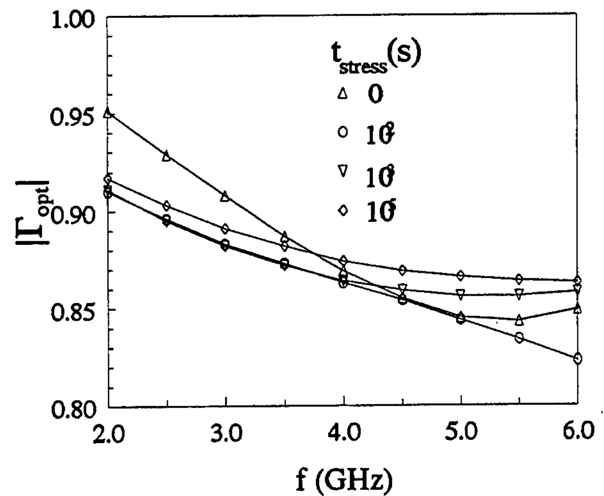

Fig. 11. $|\Gamma_{opt}|$ at diffrent t_{stress}, V_{GS} = 1.5 V, V_{DS} = 3 V.

QUASI ZERO-DIMENSIONAL CONFINEMENT IN DOUBLE-WELL SIDEWALL GATED RESONANT TUNNELING TRANSISTORS

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Vertical gated heterostructures are interesting in their applications in multi valued logic systems and study of quantization effects with possible extensions to single electron transistors. While a lot of work has been done on zero-dimensional (0D) confinement in single well resonant tunneling diodes (RTDs) very little work has been done on double well RTDs and in demonstration of confinement effects at temperatures closer to room temperature. RTDs have been shown to oscillate at frequencies of a few hundred Gigahertz and hence are suitable for high speed circuits [1]. Other applications of such three terminal resonant tunneling transistors (RTTs) include oscillators and high frequency switching circuits. We developed a sidewall gating technique that allows one to fabricate RTTs wherein we have demonstrated that one can pinchoff the RT current peak at room temperatures in single well RTDs thus alleviating the problems associated with a previously used lateral gating scheme [2,3,4]. In addition we have extended this self-aligned sidewall gating technique to quasi- one- dimensional (1D) double well RTDs and have demonstrated that as the device approaches pinch-off one is able to observe resonant tunneling through 1D confined states in vertical sidewall gated resonant tunneling transistors (RTTs) at temperatures as high as 77K [5].

In this paper we shall demonstrate that one can observe; i) room temperature pinchoff and ii) resonant tunneling at 77K through zero- dimensional (0D) states in double well RTTs. The device presented herein is one of the many devices fabricated in a single run with varying minimum widths (0.5 to 0.9 μm). The wider devices (width ≈ 0.9 μm) permit observation of transformation of the tunneling characteristics from a 2D-RTD to a 0D-RTD with increasing lateral confinement caused by the increasing negative gate bias.

The heterostructure grown on a semi-insulating substrate in a GEN II MBE system is shown in Fig 1a. The asymmetric double wells are 180$\AA$ and a 100$\AA$ wide with a 60$\AA$ $AlGaAs$ barrier in between. The two i-GaAs wells are separated from the top and bottom contact n-GaAs regions using a 35$\AA$ $AlGaAs$ barrier and a 100$\AA$ undoped GaAs spacer layer. The access channels to the spacer layer from the n+ GaAs regions are graded to prevent breakdown of the gate Schottky barrier. The top-contact structure is a non-alloyed contact structure and uses the low-temperature

grown GaAs (LTG:GaAs) capping technique. Fabrication details of such devices have already been published [2,4].

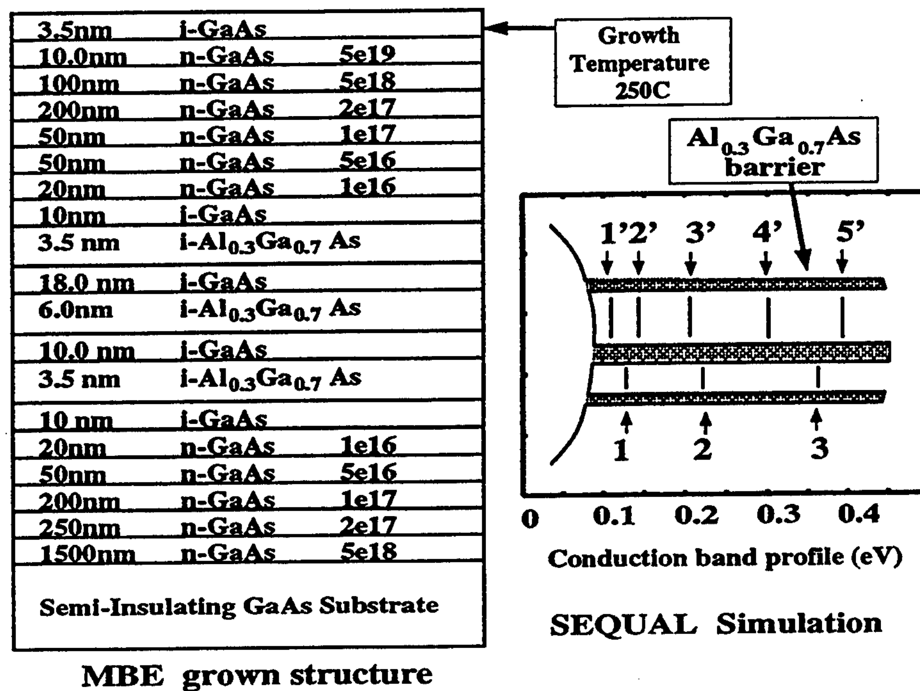

Fig. 1 The double well RTD structure grown in a Varian Gen II MBE. Shown also are the energy levels in the two wells (1, 2, 3 and 1', 2', 3', 4', and 5') at $V_{DS} = 0$ calculated using the SEQUAL simulator.

In the case of the 0.5μm wide devices the lower resonance peaks (i.e. near zero drain bias) are nominally pinched off. Also, the conduction at room temperature for these low biases is dominated by off-resonance tunneling and conduction through the depletion region under the gate. Fig. 2 shows the measured DC characteristics at various gate biases at room temperature and 77K for a 0.7 x 0.7 μm device. Fig 2a shows room temperature pinch-off of these quasi- 0D RTTs. Thermal broadening of the states in the well and conduction above the barrier does not permit observation of fine structure corresponding to 0D confinement in the wells at room temperature. At 77K these features are clearly observable. Fig 2b shows clear pinchoff of the resonant peaks at gate biases $V_{GS} \leq -3$ Volts. As the device approaches pinch-off the main resonant peak splits off into a series of sub-peaks. These I-V curves show clear indication of the multiple sub-peaks arising out of resonant tunneling through 0D states in the well. Fine structure in each of these multiple sub-peaks is also observed.

The main energy levels (1, 2, 3, and 1', 2', 3', 4' 5') of the two wells due to the $Al_{0.3}Ga_{0.7}As$ confinement in the vertical direction (z-axis) calculated using a self-consistent Poisson and Schrodinger equation solver (SEQUAL simulator) are shown in Fig. 1. As is well known, a RT peak in conductance occurs when a resonant energy level in each well lines up with the conduction band edge in the emitter. As the device approaches pinchoff the lateral confinement due to the gates causes the

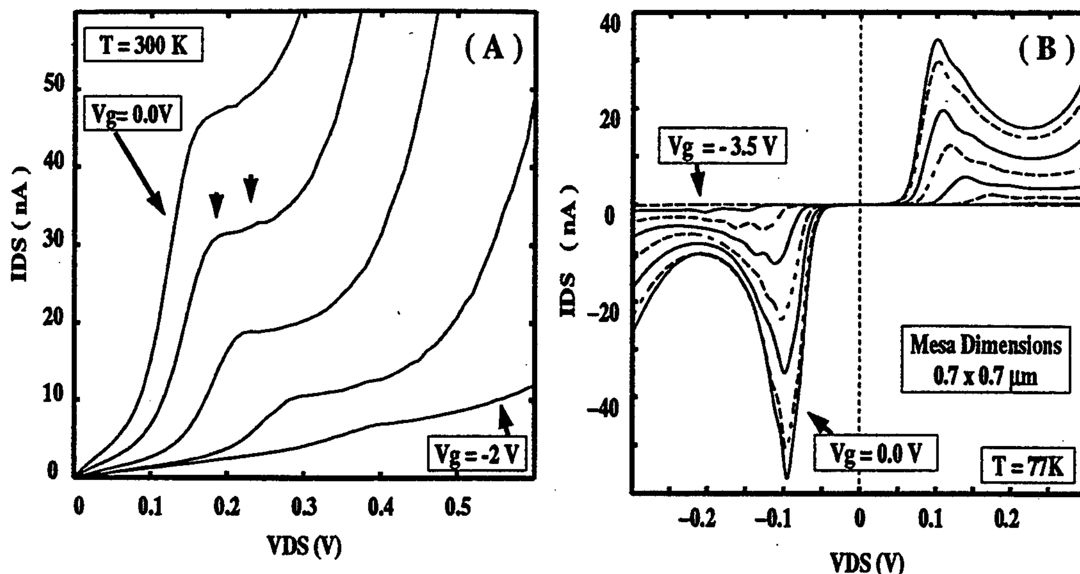

Fig. 2 Measured DC characteristics at (a) room temperature and (b) 77K for a 0.7 x 0.7 μm device at various gate biases. The small arrows in (a) indicate the position of peaks in dI_{DS}/dV_{DS}.

formation of sub-bands in the main resonant level with the separation between sub-bands being determined by the strength of the confining potential. In the present devices, a large portion of the potential drop occurs across the relatively thick (60Å) inter-well barrier thus causing a de-coupling of the states in the two wells. If the gating in both quantum wells is identical, sub-bands of the main resonant levels that are formed near pinch-off due to the lateral confinement would be identical in both the wells. One would then observe resonant tunneling through these sub-bands with maximum tunneling conductance (current) occurring when all sub-bands of one main resonant peak in one well align with the corresponding sub-bands of the main resonant peak in the other well [6]. This results in the observation of a series of sub-peaks in a 0D device instead of a single RT current peak as in the case of a large area RTDs.

These RT current sub-peaks are shown in Fig 3 for both positive and negative drain biases. The separation between the sub-peaks can be correlated to the expected separation between sub-band levels due to the lateral confinement in the wells. The variation of the separation between consecutive sub-peaks with gate bias indicates that this sub-peak formation is due to lateral confinement and not due to inelastic processes like phonon assisted tunneling. While resonant tunneling at 4.2K or lower through such laterally confined, fixed width, 0D triple barrier RTDs have been reported, we believe that this is the first demonstration at 77K of such confinement effects in gated double well RTTs [6]. Fine structure in the sub-peaks corresponding to possible confinement in the emitter has been observed in such 1D and 0D devices and shall be presented. Possible applications including low-power, high frequency circuits shall also be discussed.

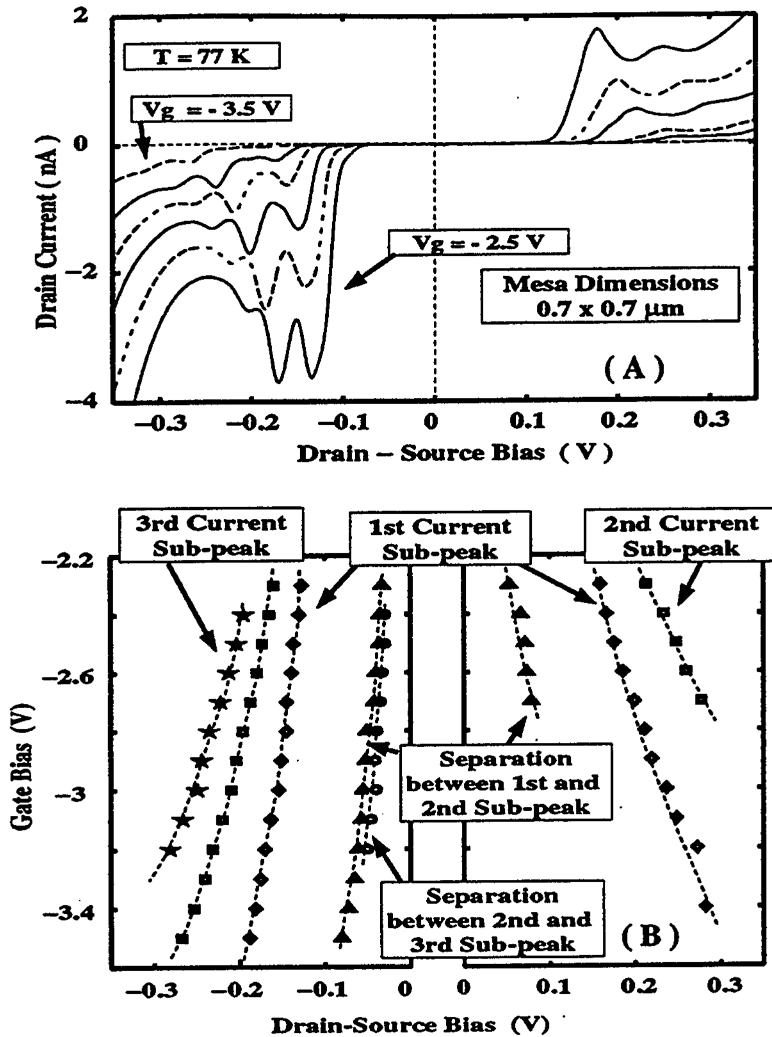

Fig. 3 (a) Measured DC characteristics for $V_{GS} \leq$ -2.5 V. (b) shows the position of the first, second and third sub-peaks in the current caused by the lateral confinement in the wells. Show also are the difference in applied extrinsic bias (V_{DS}) at which these sub-peaks occur. Lines are drawn for visual reference only.

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Semi-analytical Theory of Nanoscale Field-Effect Transistors

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We have used a simple analytically solvable model to analyze the characteristics of dual-gate metal-oxide-semiconductor field-effect transistors with 10-nm-scale channel length L. The model assumes ballistic dynamics of 2D electrons in an undoped channel between highly doped source and drain. When applied to silicon n-MOSFETs, calculations show that the voltage gain (necessary for logic applications) drops sharply at $L \sim 10$ nm, while the conductance modulation remains sufficient for DRAM cell applications until $L \sim 4$ nm.

Rapid progress in scaling down the metal-oxide-semiconductor field-effect transistors (MOSFETs) has characterized the past three decades of development of digital integrated circuits. The recent industrial forecast[1] predicts that this progress will continue for at least 15 more years, resulting in MOSFETs with channel length L as short as 70 nm. Most importantly, such devices would allow the implementation of dynamic random-access memories (DRAMs) with density up to ~ 5 Gb/cm^2.

On the other hand, single-electron devices, in particular the recently suggested SET/FET hybrids[2], may allow room-temperature operation of dynamic memories with a density of 100 Gb/cm^2 and beyond, using a silicon-based technology with minimum feature size below $\sim$ 5 nm. Thus, it is very important to understand whether purely MOSFET-based devices can operate on a comparable scale. Recent experiments[6] with $\sim$ 10-nm-long MOSFETs have shown that their conductance can be gate-modulated by at least three orders of magnitude. We are not aware, however, of any published analysis of 10−nm−scale MOSFETs, with the exception of a couple of Monte-Carlo-calculated $I-V$ curves for some particular devices with $L = 15$ nm[3] and $L = 30$ nm[4]. The main goal of this work was to use a simple model of nanoscale MOSFETs, which captures the essential physics of such devices, for semi-analytical calculation of their basic characteristics. All the examples presented below are for silicon-based n-MOSFETs, although our approach is certainly more general.

The starting point of our model is that for nanoscale devices channel doping becomes *unacceptable.* In fact, the volume of the channel region of a 10 nm-scale transistor is of the order of $2 \cdot 10^{-19}$ cm^3, so that even doping at a level as high as 10^{20} cm^3, beyond the degeneracy threshold for silicon, would result in less than 20 dopants in the whole channel, and hence in large statistical device-to-device variations of transistor parameters. On the other hand, channel doping is *unnecessary,* because the channel length is comparable to the screening length in highly doped source and drain, so that the carriers may be delivered from the contacts[7]. The high doping of the contacts is necessary to ensure low statistical fluctuations and high reproducibility of devices. This is why in our model the channel is a layer of an intrinsic semiconductor connecting n^+ source and drain (Fig. 1a). Because of the absence of impurities electron scattering is so small at our scale of channel length ($L \sim 10$ nm) that it may be ignored[3,4], and the electron transport in the channel considered as completely ballistic. On the other hand, electrons in the source and drain are assumed to be in thermal equilibrium.

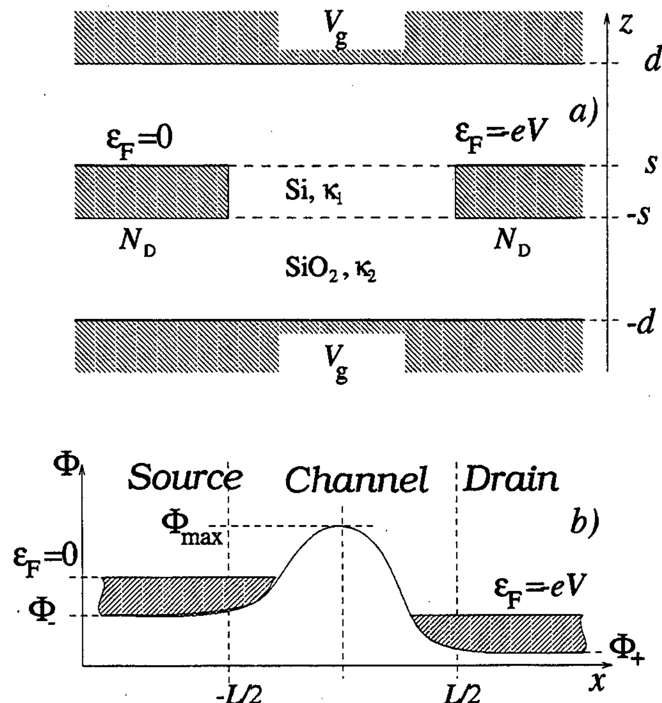

FIG. 1. (a) Sketch of the MOSFET model considered in this work and (b) scheme of the conduction band edge diagram for the electron potential energy $\Phi = -e\phi$.

Thickness $2s$ of the channel is assumed to be so small that in fact it presents a quantum well with 2D electron gas. For Si (100) surface it is well known that the 6-fold valley degeneracy of the bulk Si is lifted and only 2 valleys participate in the lateral transport[5], unless the carrier density is so large that the electrons start to populate higher subbands (which is not the case for the device

considered below).

The channel is sandwiched between plates of a "dual gate"[8,9], the optimal structure to suppress the "short channel effects" (for a review see, e.g., Ref. 10). The field distribution along z may be found from the well-known parabolic approximation[11]. This approximation leads to a 1D Poisson equation for the distribution of electric potential ϕ along the length of channel, source, and drain (at $z=0$):

$$\frac{d^2\phi}{dx^2} - \frac{\phi - V_g}{\lambda^2} = -\frac{4\pi\rho(x)}{\kappa_1}. \qquad (1)$$

Here $\rho = -en$ is the electric charge density averaged over the channel thickness $2s$; within source and drain ρ includes also the dopant charge $+eN_D$. V_g is the gate-source voltage, and λ is the effective screening length

$$\lambda^2 = \frac{s^2}{2} + \frac{\kappa_1}{\kappa_2}s(d-s). \qquad (2)$$

The parabolic approximation is valid if λ is much less than other relevant scales of the problem, notably, the channel length and the screening length of the electron gas without the ground plane, which is close to the effective Bohr radius $a_B = \alpha\kappa\hbar^2/me^2$, where $\alpha \approx 1.5$ accounts for valley degeneracy. For the examples presented below we took the dielectric constants to be $\kappa_1 = 12$ (Si) and $\kappa_2 = 4$ (SiO_2). Boundary conditions for ϕ at $x = \pm\infty$ are determined by the requirement that the Fermi distribution function deep inside source and drain has Fermi levels at 0 and V, respectively, where V is the drain-source voltage.

The second equation relating ρ and ϕ follows from the condition of conservation of the ballistic current components $j_\epsilon^\pm$ for each energy ϵ:

$$j_\epsilon^\pm(x) = -e \cdot n_\epsilon^\pm(x) \cdot v_\epsilon^\pm(x) = const = j_{\epsilon 0}^\pm, \qquad (3)$$

where $v^\pm(x) = \pm\sqrt{2[\epsilon - \Phi(x)]/m}$ is the x - component of the electron velocity, $\Phi(x) = -e\phi(x)$ is the electron potential energy, and $j_{\epsilon 0}^\pm$ are currents into the ballistic channel from the surfaces of source (sign +) and drain (sign −). The latter currents can be found from the usual thermal equilibrium distribution, then the velocity $v_\epsilon(x)$ and density $n_\epsilon(x)$ are found with self-consistent values of Φ. The total electron density n and current j (per unit channel width) can the obtained as integrals of $(n_\epsilon^+(x) + n_\epsilon^-(x))$ and $(j_{\epsilon 0}^+ - j_{\epsilon 0}^-)$, respectively, over energies $\epsilon > \Phi(x)$ (or $\epsilon > \Phi_{max}$ if the potential maximum lies between the point x and the contact, Fig. 1b). For the parameters considered below, tunneling under the potential barrier[12] can be ignored.

The resulting simple set of equations allows the channel length L and current j to be expressed explicitly as analytical (though bulky) integrals for an arbitrary relation between temperature T and Fermi energy ϵ_F in the source and drain, provided that Φ_{max} is considered known (together with the real parameters of the system, including

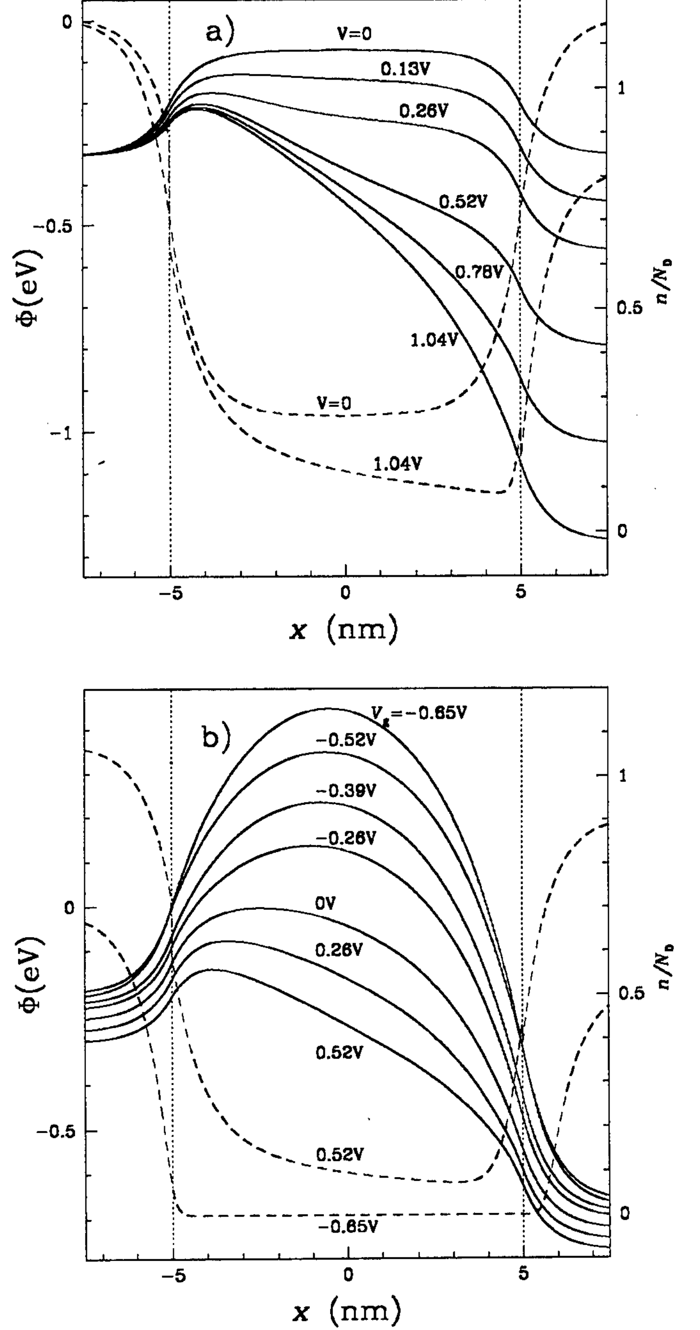

FIG. 2. Distribution of electron potential energy Φ (solid lines) and density n (dashed lines) along a 2D silicon n-MOSFET with a 10-nm-long intrinsic channel and n^+ source and drain ($N_D = 3 \cdot 10^{20} cm^{-3}$), (a) for various drain voltages V in the open state ($V_g = 0.78$V) and (b) for a moderate negative bias $V = -0.52V$ and several values of gate voltage V_g. Geometric parameters (see Fig. 1a) are: $2s = 1.5$ nm and $2d = 6.5$ nm. Temperature $T = 300$ K.

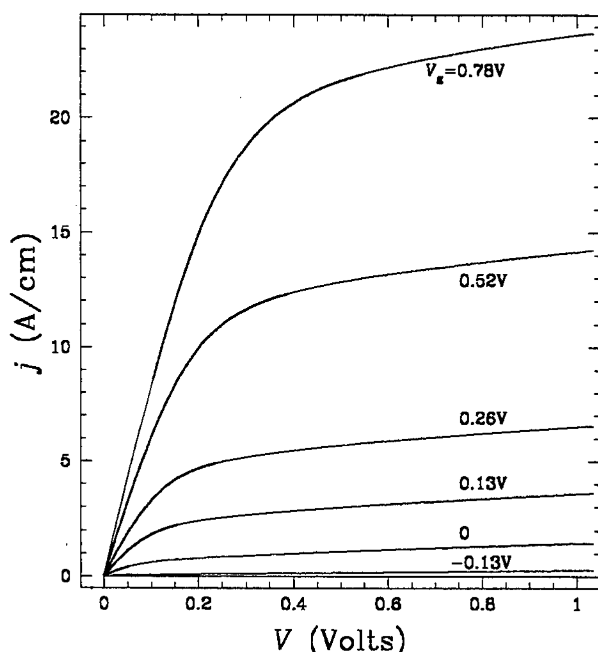

FIG. 3. $I-V$ curves for a n-MOSFET with $L = 10$ nm for several values of gate voltage V_g. Device parameters are the same as in Fig. 2.

the gate and source-drain voltages). The resulting function $L = L(\Phi_{max})$ can be numerically interpolated to the desired values of channel length.

Figures 2-4 show the results of such semi-analytical calculations for a Si/SiO_2 n-MOSFET with a contact doping level[14] of N_D=$3 \cdot 10^{20}$ cm^{-3}, channel thickness $2s = 1.5$ nm, and gate oxide thickness $d - s = 2.5$ nm. For these parameters, the parabolic approximation is indeed applicable: Eq. 1 yields $\lambda \approx 3.6$ nm, so that the ratio λ/L is about 1/3 for $L = 10$ nm. The comparison of λ and the screening lenght a_B is not as good, $\lambda/a_B \approx 1.5$. Though the latter factor can be hardly considered as large, we still believe that the parabolic approximation should work reasonably well provided that the channel length is much larger than a_B. This is due to the fact that the screening at a_B is polynomial[5] (for a point charge, $\phi \sim r^{-3}$ at $r \gg a_B$), while that due to the gates is exponential. Hence in a relatively long device ($L \gg a_B$) the wave vectors of the order of a_B^{-1} can give only a small correction to our results, crudely equivalent to a channel lenght uncertainty of the order of a_B.

Figure 2 shows the distribution of electric potential (solid lines) and electron density (dashed lines) along a 10-nm-channel MOSFET. Clearly, our model is capable of describing the penetration of the electric field into source and drain, as well as the pinch-off effect in relatively long devices (such as that shown in Fig. 2). The $I - V$ curves of such devices show clear saturation (Fig. 3) and hence relatively high voltage gain $G_V = dV/dV_g \mid_{I=const}$. Their transconductance is also very high, for example $S \approx 1.5$ S/mm at $V = V_g = 0.5$ V for $L = 10$ nm.

However, as the length L becomes comparable to the effective screening length λ, electron concentration in the channel becomes controlled more my the drain voltage and less by the gate. The saturation disappears, and the voltage gain above the threshold drops sharply, especially in the range of V_g where the current is substantial (Fig. 4). Beyond $\approx$ 10 nm logic applications of nano-MOSFETs become problematic. However, for DRAM applications (see, e.g., Ref. 13) the voltage gain is of minor importance, since the compact memory cells can be controlled by drivers fabricated using more conservative technology. What is really important for DRAMs is to have the channel current modulated by at least 8 to 9 orders of magnitude (this determines the necessary ratio of retention time to read/write time).

The modulation is limited from the side of small currents by two major effects not accounted for in our model: the thermal activation of holes and tunneling through the gate oxide. The hole activation (and hence the sharp loss of gate control) takes place when the maximum potential in the channel approaches the middle of the band gap; the corresponding region in Fig. 4 is coarsely hatched. To estimate the tunneling current effects, we have calculated the current taking into account the image charge effects and using potential barrier height of 3.2 eV and effective electron mass of SiO_2 $0.4m_0$ (see, e.g., Ref. 15), and assuming that the gates overlap source and drain by 2 nm (the final conclusions are fairly insensitive to this value). Fine hatching in Fig. 4 shows the region where the tunneling current becomes larger than the channel current. The boundary of this region rises very rapidly with a decrease in oxide thickness; for $d - s = 2$ nm it corresponds to $j \sim 10^{-6}$ A/cm. On the other hand, if the oxide is thicker than 2.5 nm, the transconductance and voltage gain fall, while the modulation range remains virtually the same because of the hole activation effects. Hence this value of oxide thickness may be considered as optimal, Further increase of the drain voltage V also does not improve the device performance since at V=0.5 V the transistor is already in saturation. Thus the channel current modulation can hardly be better than that shown in Fig. 4. One can see that the maximum modulation depth falls below $3 \cdot 10^8$ at $L \approx 4$ nm; crudely, this value may be considered as the minimum length of silicon-based MOSFETs for application in traditional DRAM cells. Of course, this does not preclude the possibility that smaller transistors could be used in some novel memories based on different physical principles.

In our analysis, several other potentially important effects have been neglected, including impact ionization, finite rate of the energy relaxation, and source and drain resistance and self-heating. Simple estimates show, however, that all these effects can be ignored for our parameters. Quantum effects have also been neglected, even though the Fermi wavelength ($\lambda_F \approx 5$ nm for $N_D = 3 \cdot 10^{20}$ cm^{-3}) is comparable with the size of the device: these effects are dramatically reduced because the

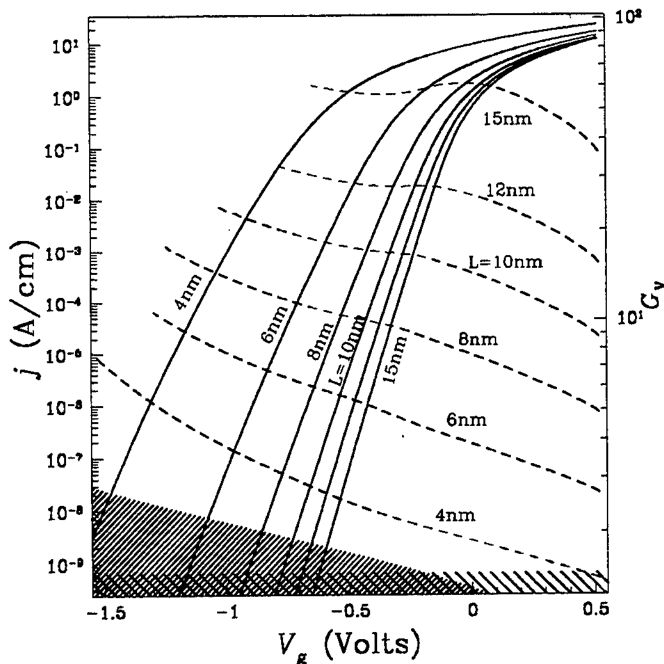

FIG. 4. Linear current density j (solid lines) and voltage gain $G_V = dV/dV_g |_{I=const}$ (dashed lines) as functions of gate voltage V_g for various channel lengths L and source-drain voltage near the saturation offset ($V = 0.52$ V). The fine hatching shows the area of parameters where the gate leakage current exceeds the drain current. The coarse hatching shows the region where the intrinsic carriers in the channel cannot be ignored.

Thomas-Fermi screening length is very small, $\lambda_{TF} < 1$ nm. Obviously, we cannot be certain that some new physical effects do not appear in the devices of this size scale.

To summarize, we have analyzed the ultimate limits of MOSFET scaling, and have found that for silicon-based devices, room-temperature operation with reasonable parameters is still feasible for channel length L down to ~ 10 nm for logic circuits and ~ 4 nm for DRAM cells. Since we have considered a virtually optimal MOSFET structure, it is hard to imagine that these limits could be surpassed without suggesting some radically new physical ideas.

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Self-organization InAs quantum dots formation by As/P exchange reaction on (001) InP substrate

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Three-dimensional (3D) confinement of carriers has received much attention for quantum device applications as well as for fundamental study in quantum physics[1]. In order to fabricate structures showing the predicted quantum effects, various techniques such as wet or dry etching, ion-beam implantation or milling, or regrowth on processed samples have been investigated[2-5]. However, these methods induce large nonradiative recombination of carriers by damage or impurities at the surfaces or the interface.

To eliminate such nonradiative recombination, *in situ* fabrication techniques is required. As an *in situ* fabrication technique, S-K growth on lattice-mismatch substrates by MBE or MOCVD has been recently recognized as a promising technique, and large efforts have been made to fabricate quantum dots structures using this technique[6-10].

Anion exchange reaction at surface of III-V compound semiconductors, because of their importance in growth high quality quantum well, have been studied by many authors[11-14]. However, the previous reports have not considered the effect of strain and the InAs island formation during As/P exchange reaction. In this letter, we propose and demonstrate a method to fabricate an InAs quantum dots on InP substrate by which strain InAs islands are formed *in situ* by using anion exchange reaction. Preliminary characterizations have been performed using AFM and PL spectrum.

The samples used here were fabricated through LP-MOVPE technique with horizontal quartz reactor, which cross section is 1×7 cm^2 rectangle. The system has a fast switching run/vent lines with pressure balance. The processing of fabricating the samples is controlled by computer. 100% arsine (AsH_3) and phosphine (PH_3) were used as source materials of V group. Trimethylinium(TMIn) as source materials of III group and its line equipped with heater. The carry gas was Pd-purified H_2 . (001) oriented InP as substrate. After standard clean treating, the substrate was loaded in the reactor. First the substrate was treated at 650℃ in PH_3 for 5 min, and then InP buffer layer was grown at 600℃ for 15 min, follow, shut off the PH_3 and TMIn and tune on AsH_3 in to reactor, anion exchange reaction occurs on surface of InP to form InAs material due to there be only AsH_3 in vapor. In order to investigate actions of anion exchange reaction for forming InAs dots, two kinds sample was performed, one have a InP cap layer which growth condition is similar with buffer layer and reduces the temperature in PH_3 after grown cap layer. Another has not InP cap layer and reduces the temperature in AsH_3 after anion exchange reaction. In all procedure the flow rate of TMIn (17℃), PH_3 and AsH_3 were 4.4 μ mol/min, 2000 μ mol/min and 440 μ mol/min, respectively, total H_2 flow rate is 6 l/min, the pressure of reactor keeps at 76 Torr. The AFM and PL were employed to study InAs characterizations.

Fig. 1 shows an AFM image in air and room temperature of a sample with 10s of As-P exchange reaction on InP surface without the InP cap layer. The sample was

cooled down after As-P exchange reaction in AsH_3. In fig. 1 we observed clearly many large islands of which the size is about 2000nm, but it appears irregular in shape. G. Hollinger[15], according to SEM, have been pointed that In droplets were formed in As stabilized InP surface after a few minutes at 575℃ under 10^{-5} Torr of arsenic under MBE condition. However, according to the feature of island structures measured by using AFM, we believe that the 3D structure formed in As/P exchange were not the In droplets but InAs islands which were caused by effect of compressive strained of InAs like the case of S-K growth mode. In addition, the small islands with rounded pyramids shape have been also observed in Fig. 1. It suggests that the InAs islands were formed in difference stage at anion exchange reaction as well as process of reduced temperature. It is reasonable to believe that the size of islands is not true state under the condition of 600℃ because of the exchange reaction of As-P going on during the temperature was cooled down from 600℃ to room temperature. At the other hand, islanding of InAs material enhanced As/P exchange reaction, which makes more In atom react with As to form InAs. So the InAs islands formed in this experiment as seen in the Fig. 1 are very large.

The photoluminescence measurements have been performed at room and 10K temperature using a 632.8nm line of He-Ne laser. Average excitation density was about 300 mw/cm^2. A Ge detector (cooled at 77K) mounted on a 0.85m double gratingmonochromator was adapted for detection in lockin mode.

Fig. 2 (a)、(b) shows the 10K PL spectrum for the samples with 7s and 10s, respectively. The spectrum shows three peaks at 925 nm, 1020 and 1440 for the sample with 7s. They can be attributed to the InP bulk, the InAs strain quantum well (SQW) and the InAs quantum dots, respectively. Fig. 2 (b) also shows 1440 and 1060nm peaks. The peak of the InAs islands at 1440nm is also confirmed by measurements on a reference sample without InP cap layer. This sample does not show a PL peak at 1440nm and around 1020nm. At the other hand, the PL spectrum for the sample with 2s (not shown here), there was very weak peaks around 1440nm, which indicate that the intensity of InAs islands is very low due to the short time of anion exchange reaction. However, the peak at 934 nm (1.327eV), which can be attribute to InAs/InP strain quantum well with 1 ML InAs layer, is strong and narrow. The full width at half maximum of the InAs QDs peak shown in Fig. 2 (a) and (b) are 85meV and 98meV, respectively. It suggests the size uniformity was reduced with longer reaction time all though the size distribution is similar (because the position of QDs peak is similar). In addition, the intensity of PL was enhanced with the increase of reaction time shown in Fig. 2. That shows that the density of islands in sample with 10s maybe higher than that of the sample with 7s. In the other hand, when increasing the reaction time, the peak position emission from the SQW (e. g. 2D InAs layer) shift to lower energy, it suggests that the thickness of 2D InAs layer increases with reaction time. For reaction time of 2s, 10s and 30s, energy positions of InAs/InP SQW are 1.340, 1.169 and 1.111eV, so the thickness of InAs 2D layer are about 1ML, 3ML and 4ML, respectively, according to report[16].

Fig. 3 shows a room temperature PL spectrum obtained from the sample of 10s, which gives strong PL emission from QDs but the peak emission from SQW was not found. In addition, the peak shown in Fig. 5 centers at 1520nm, the FMWH is 92 meV.

In conclusion, we have present the results of InAs self-organized quantum dots in InP by using anion exchange reaction at 600 ℃. The islands formation is confirmed

from the AFM measurement as well as PL measurement. However, the size of islands can not be characterized correctly by AFM since an anion exchange reaction still going on during the reduction of temperature. Strong radiate recombination is observed in sample with 10s reaction time, room temperature PL emission centers at 1520nm, and the FMWH is 92meV. The thickness of 2D InAs layer increases with reaction time, 1ML and 4ML InAs can be obtained at 2s and 30s, respectively.

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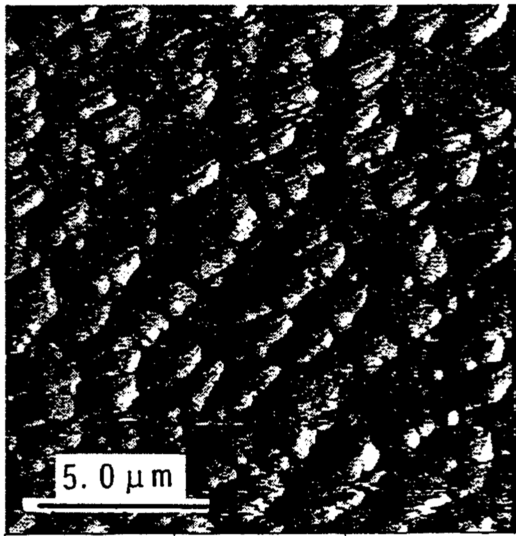

Fig. 1. The AFM image of the sample of which temperature was reduced from 600 ℃ to room in AsH_3, after 10s As/P exchange reaction.

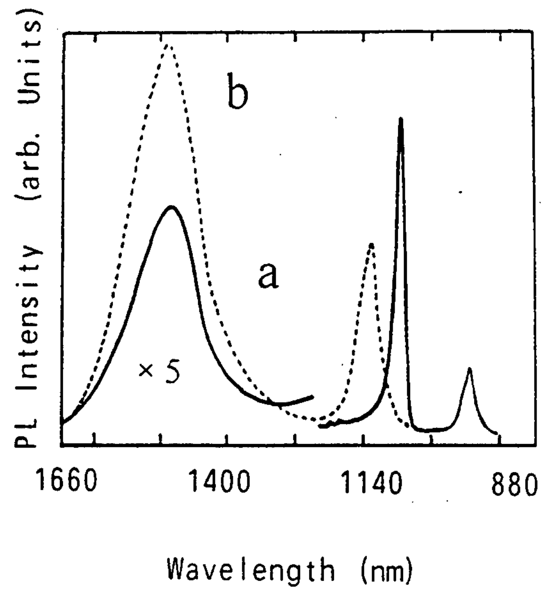

Fig. 2. The 10K PL spectrum for InAs islands embedded in InP, of which formation by using As/P exchange reaction of (a), 7s, and (b), 10s.

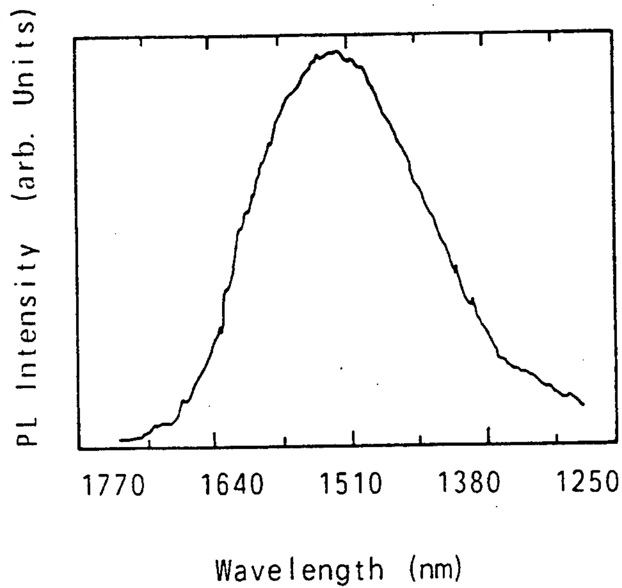

Fig. 3. Room- temperature PL spectrum for InAs islands embedded in InP, which As/P exchange is 10s at 600 ℃.

On The Engineering of The Magnetic Properties of Strained Semiconductor Quantum Dots

Jacob B. Khurgin and Amjad T. Obeidat

RAPID advances in epitaxial growth techniques as applied to semiconductor materials have permitted the development of composite structures with novel electronic and optical proerties. The most recent advances have been made in zero-dimensional systems where various arrangements and geometries of quantum dots (QD's) have been achieved. A quantum dot essetially represents a large-scale model of an atom. Arrays of coupled dots can represent molecules. This brand of bandgap engineering[1] allows the ultimate flexibility in terms of tailoring the physical properties of materials.

When it comes to the magentic properties of materials, the research has bee focused on low dimensional structures made from ferromagnetic or diluted paramagnetic materials. This research has yielded a number of important results such as the giant magneto-resistance of layered materials[2], single-domain ferromagnetic arrays[3], and molecular magnets[4] to name a few. The magnetic properties of such systems are controlled by the interactions between magnetic ions that are introduced either stoichiometrically or by dilution[5]. Quantum confinement in such systems has a mostly qualntitative character; layers of ferromagnetic material remain ferromagnetic and layers of paramagnetic material remain paramagnetic. An analogy can be made with the optical properties of quantum confined structures. Quantum confinement only modefies the absorption spectrum of bulk semiconductors shifting the absorption peak and making them sharper, but preserving the overall oscillator strength.

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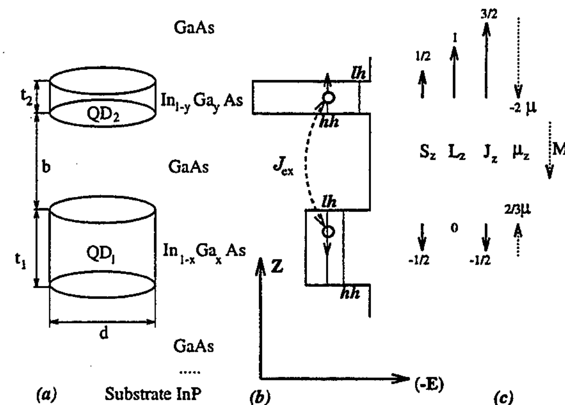

Fig. 1. (a) Cylindrical quantum dots under strain. (b) Energy bands in the z-direction. (c) The magnetic moments in the system.

However, if there are free carriers in one of the bands of a semiconductor, there is a signnificant difference. The weak absorption spectrum of free carriers is replaced with the rich spectrum of intersubband absorption in the presence of quantum confinement. Therefore, following the same analogy, we shall direct our attention to QD's with free carriers (that can have unpaired spins) in order to achieve dramatic change in magnetic properties.

One can then imagine an array of QD's, each having a single carrier that has gotten there by either doping, or more realistically, by applying a potential to the gate. Unfortunately, since each

carrier with an unpaired spin occupies the lowest state in each dot, the exchange interaction, J_{ex}, between the carriers will always be negative $J_{ex} < 0$, yielding a ground state with an anti-ferromagnetic alignment of spins, as predicted by the simple Hubbard model[6].

Anti-ferromagnetic alignment of the spins does not, however, preclude the possibility of having a net microscopic magnetic moment as long as the magnetic moments on neighboring sites do not cancel each other exactly. This is indeed the case for ferrimagnetic materials. But where can this dissimilarity of magnetic moments come from in the case of QD's?

When one looks at the properties of electrons near the bottom of conduction band, they all occupy S-type atomic orbitals with no orbital momentum, and the magnetic moment is equal to $\mu_z = -g_s\mu_B\hbar^{-1}S_z$, where $\mu_B = e\hbar/2m$ is Bohr magneton and $g_s \approx 2$ is a gyromagnetic ratio. The situation is quite different near the top of valence band. Due to strong spin-orbit interaction and the fact that the tetragonal crystal field does not split the triple-degenerate P-type orbitals comprising the valence band, the projection of orbital momentum L_z of holes in the valence band remains unquenched. Therefore, the magnetic moment μ_z of a valence band state is a function of not only its spin S_z but also of its orbital momentum L_z, or

$$\mu_z = -g_J\mu_B\hbar^{-1}J_z \qquad (1)$$

where g_J is the Lande splitting factor that for states near the top of valence band - ${}^2P_{\frac{3}{2}}$ is equal to 4/3.

In order to create a QD ferrimagnetic system we therefore need to combine QD's populated by holes with different values of L_z and J_z. In group III-V and group IV semiconductors, the top of the valence band is four-fold degenerate with holes described by the usual Bloch functions. The projection of the magnetic moment on the z-axis for heavy holes is equal to $\mu_{z,hh} = \pm 2\mu_B$ and for light holes, it is equal to $\mu_{z,lh} = \pm\frac{2}{3}\mu_B$. If a QD with a single light hole is placed next to a QD with a single heavy hole (Fig.1), then, in a way similar to the Hydrogen molecule, the Heisenberg Exchange Hamiltonian in the Ising model can be introduced as

$$\mathcal{H}_{ex} = -\mathcal{J}_{ex}\hbar^{-2}J_{z,hh}J_{z,lh}. \qquad (2)$$

Evaluation of the scalar product $J_{hh} \cdot J_{lh}$ for the cases of parallel ($J_{z,t} = J_{z,hh} + J_{z,lh} = \pm 2\hbar$) and anti-parallel ($J_{z,t} = \pm\hbar$) arrangement shows that the exchange integral $\mathcal{J}_{ex}$ is negative favoring the antiparallel alignment of moments, $J_{<}z,hh >= \pm\frac{3\hbar}{2}$ and $J_{<}z,hh >= \mp\frac{\hbar}{2}$. The magnetic moment of this state, however, is not 0 but is equal to $\mu_z = \pm\mu_{z,hh} \mp \mu_{z,lh} = \pm\frac{4}{3}\mu_B$. Expanding to an array with two sub-lattices of QD's - one with light holes and one with heavy holes we can create a ferrimagnet with a critical temperature on the order of $T_c \sim \mathcal{J}_{ex}/k_BT$.

This Heisenberg approximation is a very crude one and we shall refine it later, but for now the most crucial question is how to obtain an array of alternating light and heavy holes. The answer is to use strain which is capable of splitting the degeneracy of light and heavy holes even in the absence of confinement. The presence of In in GaAs produces a shear strain component which splits the heavy-hole and light-hole energy bands near the Γ point. Now, if one considers situation in Fig. 1, there are two disc-shaped QD's grown on InP substrate. The composition of first QD is $In_{1-x}Ga_xAs$; $x > 0.47$. Therefore, QD1 is under biaxial tension and the light hole, $J_z = \pm\frac{1}{2}$ is above the heavy hole $J_z = \pm\frac{3}{2}$ by as much as few hundred meV. Meanwhile in the second QD, grown from $In_{1-y}Ga_yAs$; $y \leq 0.47$ the heavy hole is above the light hole. By properly choosing the dimensions of QD's it is not difficult to achieve a near resonance between $E_{lh,1}$ and $E_{hh,2}$. Note that while the magnetic properties of the structure do not rely upon resonant tunneling, and thus the structure is relatively tolerant to disorder, it is absolutely crucial to ensure that no QD is occupied by more than one hole.

This puts an upper boundary on disorder

$$\delta E \ll U_i \approx \frac{e^2}{2\epsilon\sqrt{t_i^2 + d_i^2}} \qquad (3)$$

where $i = 1, 2$, and U_i is Coulomb repulsion energy of two holes in the same QD where t is the QD's "thickness" and d is its diameter as shown in Fig. 1. For a QD with $t \approx 20\mathring{A}$ and $d \approx 100\mathring{A}$ U is of the order of 20 meV and (3) can be satisfied.

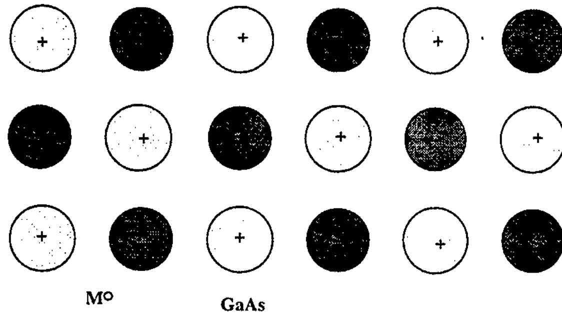

Fig. 2. A 2-dimensional array of starined quantum dots.

Now we can formally introduce the Heisenberg exchange integral in (2) as

$$\mathcal{J}_{ex} = -\frac{2}{3}\frac{4T_1^2}{\bar{U}}, \qquad (4)$$

where $\bar{U}^{-1} = (U_1^{-1} + U_2^{-1})/2$, and T_1 is the probability of hole tunneling between QD1 and QD2 with a change of angular momentum; $\Delta J_z = \pm\hbar$. By using the mean field theory [8] and introducing effective exchange fields for both sub-lattices 1 and 2, the critical temperature can now be found using

$$T_c = \frac{1}{2}\cdot\frac{3}{2}|\mathcal{J}_{ex}|/k_B = \frac{2T_1^2}{\bar{U}k_B}. \qquad (5)$$

Typical values for $\bar{U}$ and T_1 are 20 meV and 7 meV respectively which result in an exchange integral value of approximately 6.5 meV. We have estimated the value of T_c for two superlattice consisting of $In_{1-x}Ga_xAs$ $20\mathring{A} \times 100\mathring{A}$ and of $In_{1-y}Ga_yAs$ $30\mathring{A} \times 100\mathring{A}$ separated by $20\mathring{A}$ barriers. T_c was found to be approximately 50 k. Let us now look at the implications: if QD's are arranged in a two-dimensional superlattice (Fig. 2) we can indeed expect a phase transition at temperature close to T_c which would be a true Curie temperature. But the growth of QD's of different compositions in the same plane appear to be out of reach of today's technology. Besides, exchange interactions between second-nearest neighbors can force both sub-lattices to become anti-ferromagnetic.

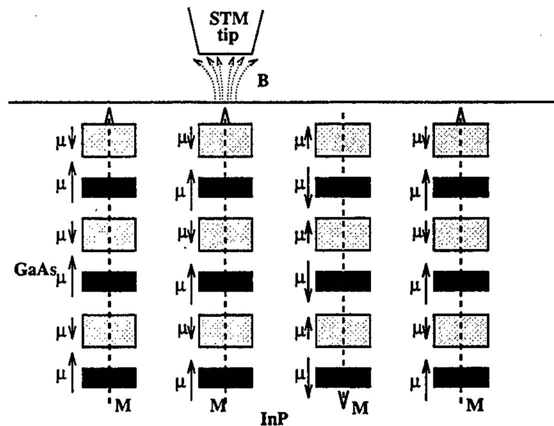

Fig. 3. Pillar arrays of strained quantum dots. The magnetic moments can be written and read with an STM tip.

Let us consider a one-dimensional pillar-like structure (Fig. 3). It is well known [9] that no long-range (i.e. $N_{QD} \rightarrow \infty$) order can exist and thus there is no spontaneous magnetization. But for a limited number of QD's we can expect the system to maintain its spontaneous polarization for as long as $T \ll T_c/lnN_{QD}$. So, for a small number of QD's lined-up in a polymer-like chain, one can expect the magnetic order to be maintained in the absence of external field, albeit at temperatures of the order of 10 k.

The main reason for such a low critical temperature is simply the fact that in QD's, Coulomb interactions responsible for magnetic alignment are scaled down in comparison to conventional materials due to large dot-to-dot distances and

larger dielectric constant. The order of this reduction is comparable to scaling down of the Rydberg energy in such materials. Therefore, in a wider-bandgap material, such as GaN, one can expect an increase in T_c by as much as an order of magnitude.

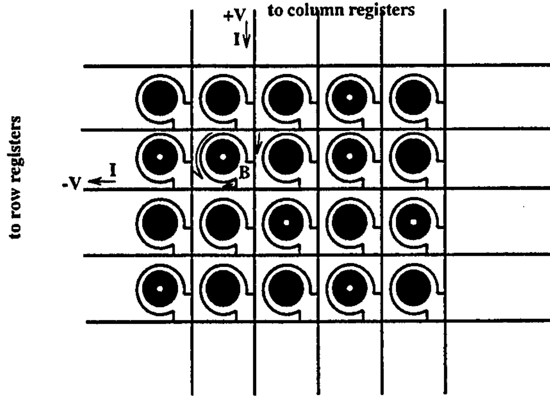

Fig. 4. Geometry for magnetic memory. The data is written by the passing currents through the metal interconnects.

Turning to potential applications, "ferrimagnetic pillars" can act as a storage element (Fig. 4), as a "transmission line" for magnetization, and, possibly, as a base for spin transistors. One can also think about magnetic dipole interactions between the adjacent pillars or spin-preserving transport between them as the operating principle for cellular automata or more conventional switches. A major important feature of artificial ferrimagnets is that their magnetization can also be controlled electrically: by changing the position of Fermi level using an external gate one can change the population of the QD's and thus quench the magnetization.

In conclusion, we examined the magnetic properties of the arrays of compressive and tensile-strained QD's using mean field model with exchange interactions determined from Hubbard model. We have determined the temperature range in which there exist a possibility of observing spontaneous magnetization in one- and two-dimensional QD-arrays, and considered some practical applications.

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Deep Sub-0.1μm Fully Depleted SOI MOSFET's with Ultra-Thin Silicon Film and Thick Buried Oxide for Low-Power Applications

Student paper

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Abstract

We propose device structures of ultra thin FD SOI MOSFETs for very low power applications. In order to design such devices, a novel scaling methodology for FD SOI MOSFETs has been developed and a scaling scenario to the deep sub-0.1 μm regime is shown. The short channel effect is suppressed by ultra thin SOI film and the steep subthreshold slope is achieved by thick buried oxide. It is also shown by means of 2D-device simulation that FD SOI MOSFETs will be miniaturized further than bulk MOSFETs without degrading the steep subthreshold slope and increasing *Vth* fluctuations, even if the gate oxide thickness is not scaled.

1. Introduction

Fully depleted (FD) SOI MOSFETs are attractive for very low power applications due to low parasitic capacitances and a steep subthreshold slope. These merits come from the existence of a buried oxide. The scaling of FD SOI MOSFETs is also promising because the channel depletion width can be limited by the SOI thickness. Several scaled SOI MOSFETs have been proposed or fabricated, and their performances have been confirmed [1-4]. However, they are not suitable for low power applications because the subthreshold slope has been greatly degraded and parasitic capacitances have increased due to thin buried oxide. In this paper, we propose device structures of ultra thin FD SOI MOSFETs for very low power applications. Special attention has been paid to the degradation of the subthreshold slope.

2. Ultra Thin FD SOI MOSFETs

Fig. 1 shows the proposed device structure of a 0.05 μm channel length FD SOI MOSFET. Short channel effect is suppressed by the ultra thin SOI. The non-doped channel reduces *Vth* fluctuations. To realize the steep subthreshold slope and low parasitic capacitances, buried oxide thickness remains thick. Key processes of FD SOI MOSFETs are the reduction of S/D resistance and the gate material for *Vth* adjustment. The S/D resistance is reduced by the selective Si epitaxial growth and the subsequent silicide [4,5], and mid-gap material [6-8] is utilized for the gate electrodes as shown in Fig. 1. The proposed device structure is based on the scaling scenario we have developed for low power FD SOI MOSFETs. The detailed scaling methodology and the comparison with conventional bulk MOSFETs are described in the following sections.

3. Scaling Methodology for FD SOI MOSFETs

Fig. 2 shows a schematic view of FD SOI MOSFETs. We considered four device parameters; gate oxide thickness (t_{fox}), SOI thickness (t_{SOI}), buried oxide thickness (t_{box}), and channel doping concentration (N_A). As shown in Fig.3, subthreshold swing (S) is roughly determined by the ratio of t_{fox} to t_{box}. To realize S lower than 65 mV/dec, t_{box} should be more than ten times as thick as t_{fox}. To understand the degradation of S by the short channel effect (SCE), we have derived the potential at the back interface by solving a 2D Poisson's equation analytically. Here, we have introduced the natural length (λ) [9-11] and modified for the ultra thin FD SOI MOSFETs.

$$\lambda \equiv \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{2\varepsilon_{Si}}\frac{t_{SOI}}{t_{fox}}\right)\cdot t_{SOI}\cdot t_{fox}} \qquad (1)$$

Fig. 4 (a) shows the simulation [12] results of S degradation by SCE for four generations below 0.1 μm

listed in Table 1. When L_{eff} is normalized by λ, the degradation of S shows a universal curve as shown in Fig. 4 (b). It is found that S is always 80mV/dec when $L_{eff} = 6\lambda$. This means that t_{fox} and t_{SOI} only have an influence on SCE of FD SOI MOSFETs and that SCE can be suppressed even if t_{box} is thick.

Fig. 5 (a) summarizes the scaling scenario of FD SOI MOSFETs to the deep sub-0.1 μm regime developed by the above mentioned analytical results. A criterion of SCE is set to S = 80mV/dec (i.e. $L_{eff} = 6\lambda$). Each curve corresponds to S = 80 mV/dec. In the lower left region of each curve, SCE can be suppressed in each generation. Scaling of t_{fox} and V_{dd} is assumed as shown in Figs. 5 (b) and (c). At L_{eff} shorter than 0.15 μm, t_{fox} is assumed to remain 30 Å by the direct tunneling limit. This result shows that the FD SOI MOSFETs can be scaled by thinning t_{SOI} even if the t_{fox} is constant. The constant t_{fox} scaling doesn't enhance the speed greatly, but it can reduce power consumption drastically compared with the conventional scaling.

4. Comparison with Bulk MOSFET's

A. Short Channel Effect

When gate oxide thickness (t_{fox}) does not scale as shown in Fig. 5 (b), SCE of bulk MOSFETs can be suppressed only by the reduction of the channel depletion width and S/D junction depth (X_j). Fig.6 shows S vs. N_A for long channel bulk MOSFETs. Although SCE can be suppressed, increasing N_A (i.e. decreasing the channel depletion width) degrades S of long channel bulk MOSFETs when t_{fox} is constant. Fig. 7 compares the degradation of S in bulk MOSFETs (constant N_A) with FD SOI MOSFETs. The device parameters are shown in Tables 1 and 2. In the 0.1 μm generation, bulk MOSFETs show better SCE than FD SOI MOSFETs [1,7]. In the 0.03 μm generation, however, bulk MOSFETs show worse SCE than FD SOI MOSFETs. This is because the channel depletion width is not scaled in bulk MOSFETs with constant N_A. In FD SOI MOSFETs, the channel depletion width is scaled with t_{SOI} and the degradation of S is suppressed even if N_A is non-doped.

B. Vth Fluctuations

In FD SOI MOSFETs, *Vth* is controlled by N_A within a range of fully depletion. However, to adjust *Vth* to a proper value in case of the N^+ poly Si gate, higher N_A is required with the scaling and causes the problem of *Vth* fluctuations. Fig.8 shows calculated *Vth* fluctuations of FD SOI MOSFETs as a function of L_{eff}. The statistical variation of channel dopant number [13] and the process variation of t_{SOI} are considered. *Vth* is set to the value in the inset. *Vth* fluctuations increase with scaling down the device sizes. On the other hand, FD SOI MOSFETs with non-doped N_A would reduce *Vth* fluctuations drastically, because *Vth* is determined only by the work function difference. Therefore, FD SOI MOSFETs should be miniaturized with non-doped N_A rather than high N_A, and *Vth* should be adjusted by midgap material for gate electrode.

5. Conclusions

We have proposed device structures of ultra thin FD SOI MOSFETs for very low power applications. In order to design such devices, a novel scaling methodology for FD SOI MOSFETs is developed and a scaling scenario to the deep sub-0.1 μm regime is shown. Scaling of the gate oxide thickness and the SOI thickness is essential. The ultra thin SOI film suppresses the short channel effect and the thick buried oxide achieves the steep subthreshold slope. Using the proposed methodology, we have shown that, unlike bulk MOSFETs, FD SOI MOSFETs will be miniaturized further by thinning the SOI thickness without degrading the steep subthreshold slope and increasing *Vth* fluctuations, even if the gate oxide thickness is not scaled.

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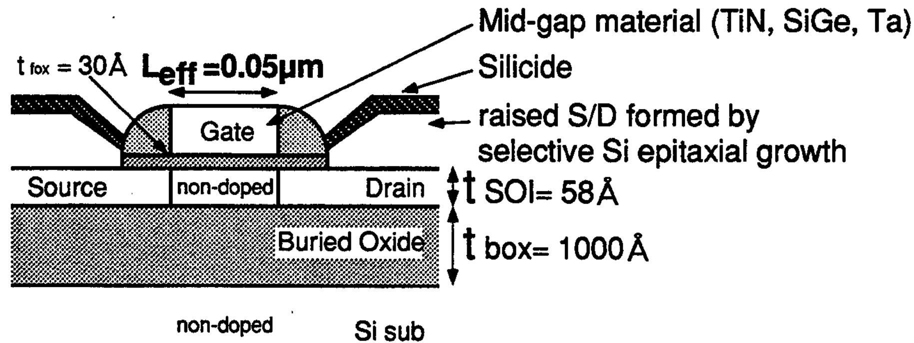


Fig.1 The proposed device structure of a 0.05μm FD SOI MOSFET. Short channel effect is suppressed by the ultra thin SOI. The steep subthreshold slope and low parasitic capacitances are realized by the thick buried oxide. The non-doped SOI reduces Vth fluctuations.

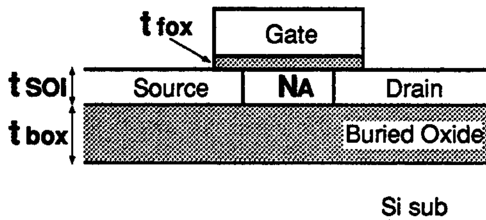


Fig.2 Schematic of FD SOI MOSFETs.

Table.1 Device parameters of FD SOI MOSFETs below 0.1μm. They are based on Fig.5 (a).

	type A	type B	type C	type D
t_{fox}	30Å	←	←	←
t_{SOI}	162Å	98Å	58Å	24Å
t_{box}	1000Å	←	←	←
N_A	1×10^{15} cm^{-3}	←	←	←
N_{sub}	1×10^{15} cm^{-3}	←	←	←
V_{ds}	1V	0.84V	0.71V	0.55V
	0.1μm Generation	0.07μm Generation	0.05μm Generation	0.03μm Generation

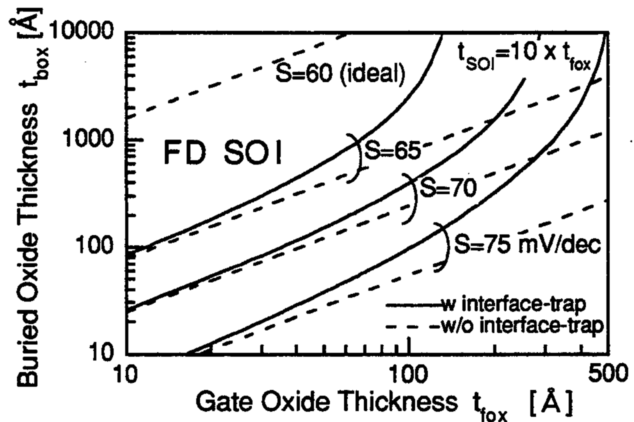
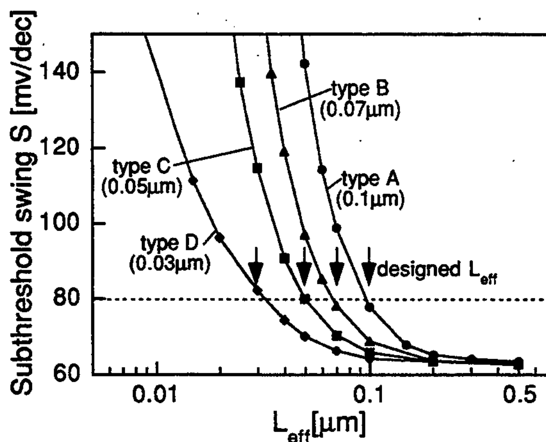
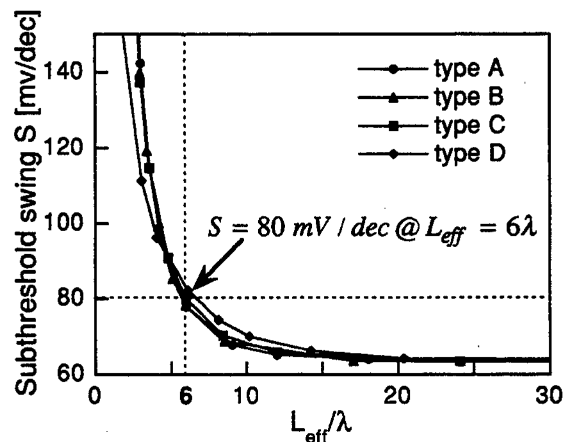


Fig.3 The dependence of S on t_{fox} and t_{box}. To realize S lower than 65 mV/dec, t_{box} should be more than ten times as thick as t_{fox}.

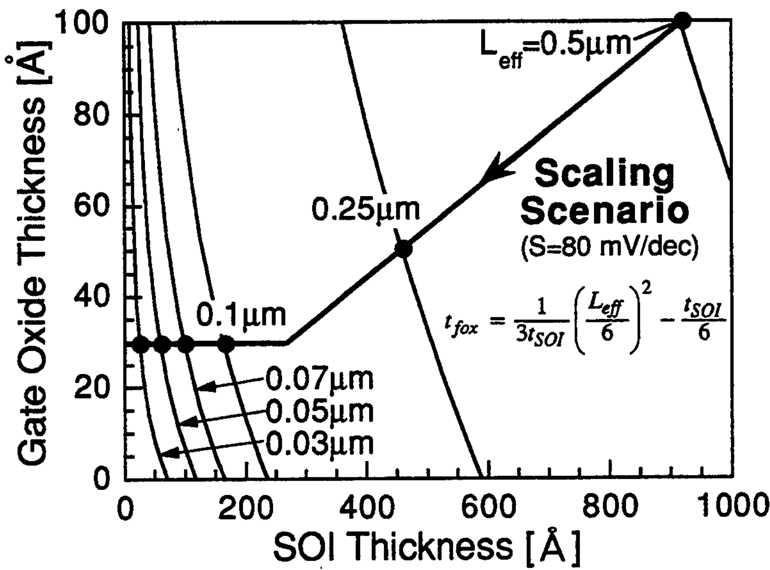


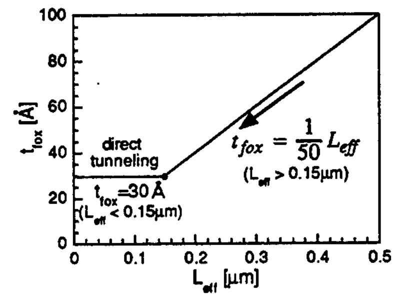
(a) S vs. L_{eff} of FD SOI MOSFETs shown in Table 1.



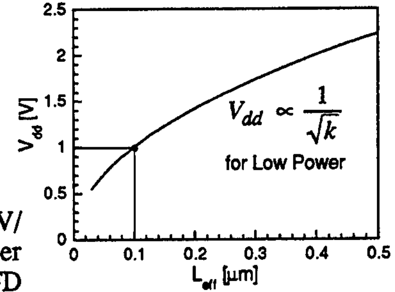
(b) S vs. normalized L_{eff} by λ. S is always 80mV/dec when $L_{eff} = 6\lambda$.

Fig.4 Degradation of S by the short channel effect.





(b) Scaling scenario of t_{fox}.



(c) Scaling scenario of V_{dd}.

(a) Scaling scenario of t_{fox} and t_{SOI}. A criterion of SCE is set to $S = 80$mV/dec (i.e. $L_{eff} = 6\lambda$). Each curve corresponds to $S = 80$ mV/dec. In the lower left region of each curve, SCE can be suppressed in each generation. FD SOI MOSFETs can be scaled by thinning t_{SOI} even if the t_{fox} is constant.

Fig.5 Scaling scenario of FD SOI MOSFETs to the deep sub-0.1μm regime.

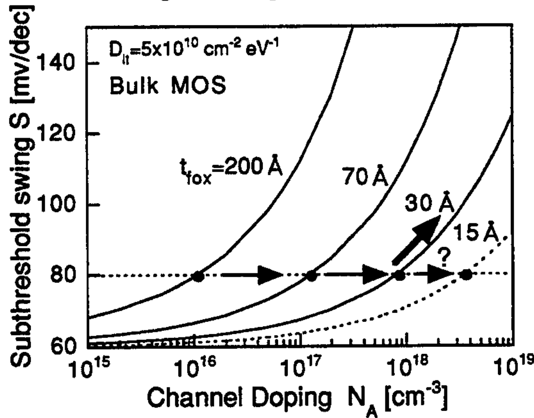


Fig.6 S vs. N_A for long channel bulk MOSFETs. Increasing N_A (i.e. decreasing the channel depletion width) degrades S of long channel bulk MOSFETs when t_{fox} is constant.

Table.2 Device parameters of bulk MOSFETs below 0.1μm. X_j equals to t_{SOI} in Table.1.

	type A'	type D'
t_{fox}	30Å	←
X_j	162Å	24Å
N_A	1×10^{18} cm^{-3}	←
V_{ds}	1V	0.55V
	0.1μm Generation	0.03μm Generation

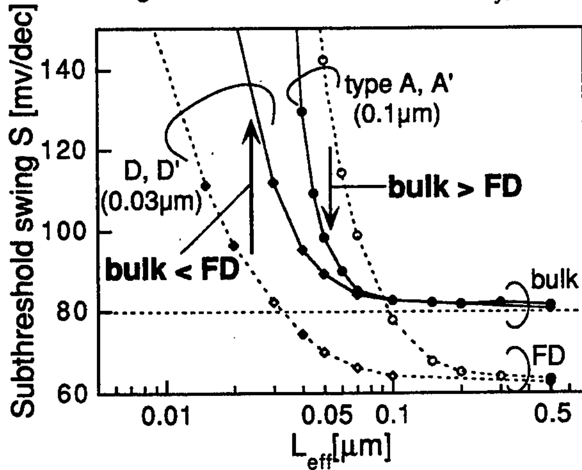
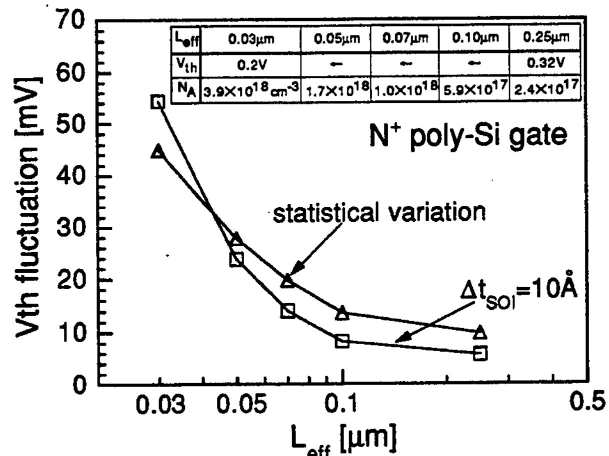


Fig.7 S vs. L_{eff} of FD SOI and bulk MOSFETs shown in Table.1 and 2. In the 0.03 μm generation, bulk MOSFETs show worse SCE than FD SOI MOSFETs.



L_{eff}	0.03μm	0.05μm	0.07μm	0.10μm	0.25μm
V_{th}	0.2V	←	←	←	0.32V
N_A	3.9×10^{18}cm^{-3}	1.7×10^{18}	1.0×10^{18}	5.9×10^{17}	2.4×10^{17}

Fig.8 Vth fluctuations of FD SOI MOSFETs with N$^+$ poly gate. The fluctiations are greatly reduced in the FD SOI MOSFETs with non-doped SOI and the mid-gap gate material.

Simulation of 0.5V Bulk DT-MOSFET's With Sub-0.1μm Gate Length: Device Structures, Characteristics and Circuit Performance

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1.0 Introduction

Scaling MOS device dimensions in the sub-half micron regime requires more frequent reductions in the power supply voltage *Vdd* in order to reduce the dynamic power consumption. The threshold voltage *Vth* itself also has to be reduced simultaneously with *Vdd* to avoid performance loses, which, in turn, results in a significant increase in the standby power dissipation [1-2].

Gate-to-body connected dynamic threshold (DT) MOSFET's is found promising for low-voltage applications in SOI [3]. Recent research interest starts to focus on bulk DT-MOS [4-5]. This paper presents simulation results of 0.5V bulk DT-MOSFET's down to sub-0.1μm gate length. A device structure, consisting of shallow source/drain extensions and pocket dopings, is found to have excellent short channel effects down to 0.07μm gate length under DT-MOS operation. A DSOI (Drain/Source-On-Insulator (SiO_2)) is proposed to reduce source/drain junction capacitances in bulk MOSFET's. Circuit simulation demonstrates that the gate delay time of 0.5V DSOI DT-MOS inverter is comparable to those of 0.5V SOI DT-MOS and 1V conventional bulk CMOS inverters when *Lg* is scaled from 0.18μm to 0.07μm

2.0 Device Structure and Simulation Description

Scaled source/drain junction depths and gate oxides help improve short-channel effects (SCE) such as DIBL. Fig. 1 gives schematic cross sections for the nMOSFET's considered in this work, where *Vb* is the body electrode. Unless otherwise mentioned, device parameters were gate oxide thickness *Tox* = 3nm, S/D extension depth X_{je} = 10nm, and deep S/D depth X_j = 0.1μm. The energy transport model (ETM) was used in 2-D MEDICI simulation [6].

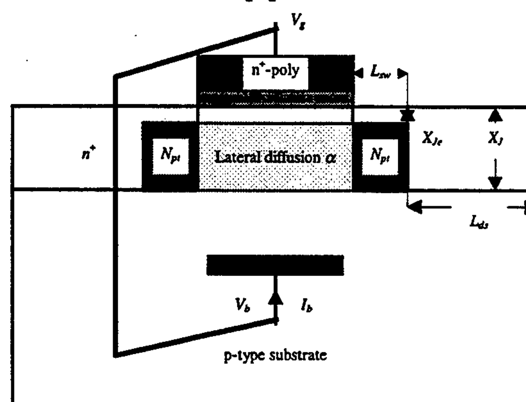


Fig. 1. Schematic cross section of a DT-MOSFET structure having shallow source/drain extensions and idealized p-type pockets with a uniform doping concentration *Npt*, where the lateral diffusion coefficient α accounts for source-to-drain non-uniform doping.

3.0 Results And Discussion

3.1 Power Supply Voltage And *Vth* Lowering Effects

To avoid turning on the source-body *pn* junction, the maximum *Vdd* is set at 0.5V as shown in Fig. 2, which is believed to be attractive for generations down to *Lg* = 0.05μm [7].

DT-MOS operation results in threshold voltage reduction leading to an increased drain conductance in the on-state mode while the off-state drain current equals that of the conventional MOSFET. This is illustrated in Fig. 3, where *Vth* rapidly decreases with rising body voltage as the doping concentration is increased.

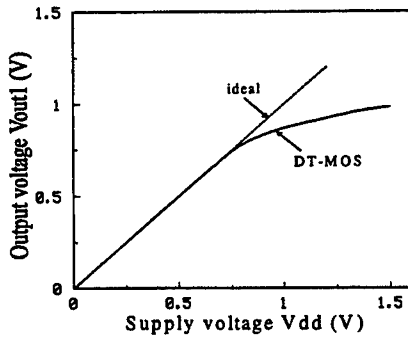


Fig. 2. Output characteristics of DT-CMOS inverter chain, where dashed lines represent the ideal output relationship. *Lg* = 0.07μm, *Vth* = 0.1V taken at *Vds* = 0.5V.

3.2 *Vth* Rolloff And Reverse Short Channel Effect

Fig. 4 shows *Vth* dependence on the gate length *Lg* for devices under DT-MOS and body-grounded (conventional) operations. The conventional device has the same channel dopings as those of its DT-MOS counterpart. It can be seen that *Vth* of DT-MOS device is expectedly lower than that of the conventional one. Forward body biasing reduces the thickness of the space-charge region and bring the back gate (neutral region) closer to the channel. This reduces the normal and reverse short channel effects.

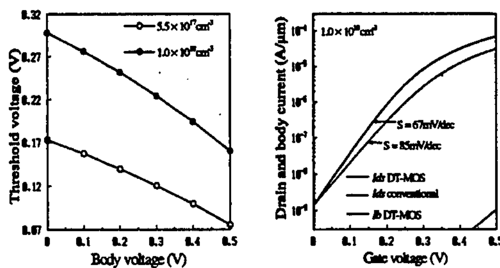


Fig. 3. *Vth* lowering effects and *I-V* characteristics. *Lg* = 0.07μm. (a) *Vth* lowering, *Vds* = 0.025V to avoid the DIBL effect. (b) *I-V* curves at *Vds* = 0.5V. Gate-to-body current *Ib* is negligible.

3.3 Influence of the Gate Oxide Thickness

To increase the speed performance, an effective way is to reduce the gate oxide thickness to improve transistor's current driving capabilities. Fig. 5 shows the variation of *Idsat* and subthreshold swing with *Tox* for a 0.5V 0.07μm DT-MOSFET, where *Vth* is fixed at 0.1V (at *Vds* = *Vbs* = 0.5V) without relaxing *Ioff*. From the figure, as *Tox* is scaled down beyond 3nm, the enhancement of *Idsat* disappears due to the degraded electron mobility.

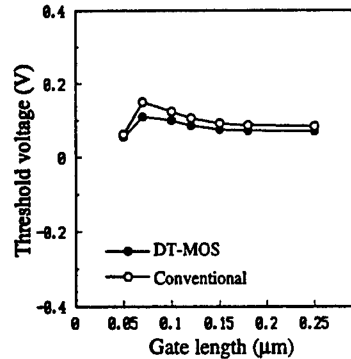


Fig. 4. *Vth* dependence on *Lg* for DT and conventional nMOSFET's. *Vds* = 0.5V.

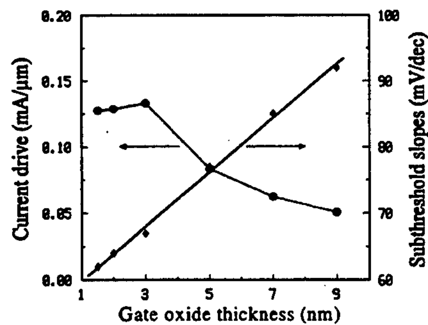


Fig. 5 Variation of on-state currents and *S* factors with the gate oxide thickness in *Lg* = 0.07μm DT-MOSFET. *Vds* = 0.5V.

3.4 Bulk DT-MOS Transistor Performance

A simple first-order expression for the gate delay *tpd* is given by

$$t_{pd} \propto \frac{CV_{dd}}{Idsat}$$

where *C* is the total load capacitance. For a fixed *C*, if *Idsat* decreases at a smaller rate than that of *Vdd* scaling, no penalty is paid for lowering the supply voltage. Using *Idsat*/*Vdd* as a figure of merit, Fig. 6 shows comparisons of the performance as a function of *Vth*/*Vdd* between 0.5V DT transistors and conventional ones under *Vdd* = 0.5V and 1V, where all devices have the same drain extension and pocket doping with *Lg* = 0.1μm

and 0.07μm (all *Vth* obtained at *Vds* = *Vbs* = 0.5V).

From Fig. 6 the following is noteworthy. Firstly, as compared with 0.5V conventional transistors, DT operation shows a significant performance improvement by a factor of 1.6 at *Lg* = 0.1μm and about 2 at *Lg* = 0.07μm. Secondly, at *Lg* = 0.1μm, 0.5V DT and 1V conventional FET's deliver almost the same performance in the range of lower *Vth*/*Vdd*; at *Lg* = 0.07μm, 0.5V DT transistor shows a modestly higher performance than 1V conventional device. In comparison with conventional transistors, 0.5V DT-MOSFET performance scales better with *Lg*.

In DT-MOS, since the gate and body electrodes have the same voltage, the surface potential (substrate band bending) *Vs* is almost invariant to *Vgs* and well reduced in the strong inversion condition from that in the conventional transistor, as shown in Fig. 7. Therefore, electrons are able to traverse the channel suffering less scatterings and the mobility is increased.

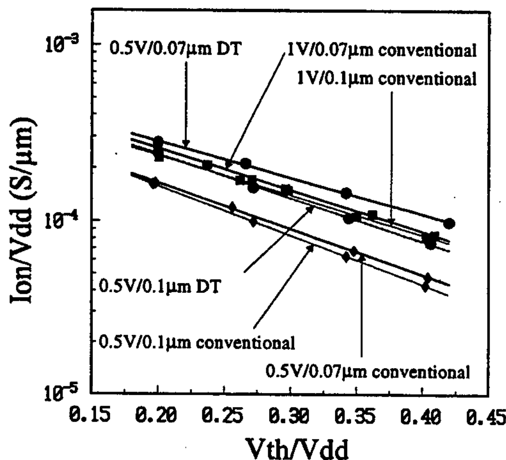


Fig. 6. Transistor performance as a function of the ratio of *Vth*/*Vdd* for bulk DT-MOSFET's under different operation conditions. Dashed curves are for *Lg* = 0.1μm, while solid ones for *Lg* = 0.07μm.

3.5 Circuit Performance And DSOI MOSFET's

Fig. 8 shows the dependence of the gate delay time per stage (*tpd*) of 0.07μm CMOS inverter chains on the gate oxide thickness *Tox*, where *Vth* = 20%*Vdd*. When *Tox* is reduced beyond 3nm, *tpd* of 0.5V DT-MOS increases rapidly, since *Idsat* does not increase as show in Fig. 5. Furthermore, *tpd* of 0.5V DT-MOS is larger than that of 1V conventional CMOS.

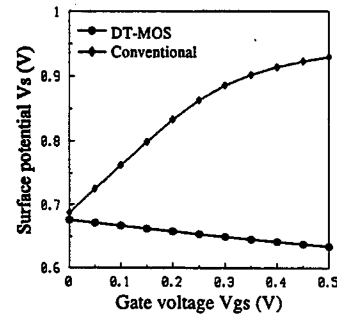


Fig. 7. Dependence of substrate band bending *Vs* on *Vgs* in DT and conventional MOSFET's. *Lg* = 0.07μm, at *Vth* = 0.1V and *Vds* = 0.

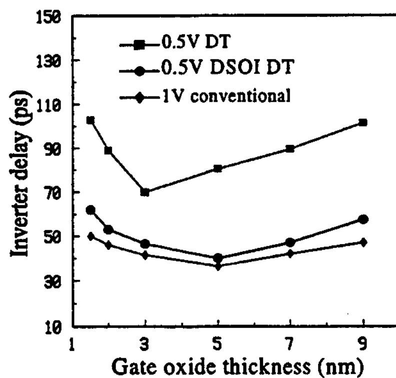
Placing buried oxides under the bottom part of S/D junctions is effective in reducing the junction capacitances and increasing the speed performance in bulk CMOS. We call this DSOI (drain/source-on-insulator). A schematic cross section of DSOI and its *tpd* are shown in Fig.8. It almost matches 1V conventional CMOS in the gate delay.

Fig. 9 demonstrates *tpd* as a function of *Lg* for bulk and SOI CMOS under different operation conditions. SOI silicon layer thickness T_{SOI} is 0.1μm. Such an SOI device has many advantages as described in [8]. Note that the speed performance of 0.5V DSOI DT-CMOS exceeds that of 0.5V SOI and is comparable to that of 0.5V SOI DT-CMOS; a power-delay product reduction by a factor of 3.4 is achieved as compared to 1V conventional bulk CMOS when the parasitic capacitance is taken into consideration.

3.6 Standby Power Reduction

Fig. 10 shows the standby power variation with supply voltages for 0.07μm DT-DSOI and conventional CMOS. *Vth* = 20%*Vdd* is chosen for the latter, while the former maintains equal gate delay times at each *Vdd* by tuning *Vth*. The figure indicate that at *Vdd* = 0.5V a reduction of standby power

dissipation by a factor of 11 can be achieved through DT operation without speed loses.



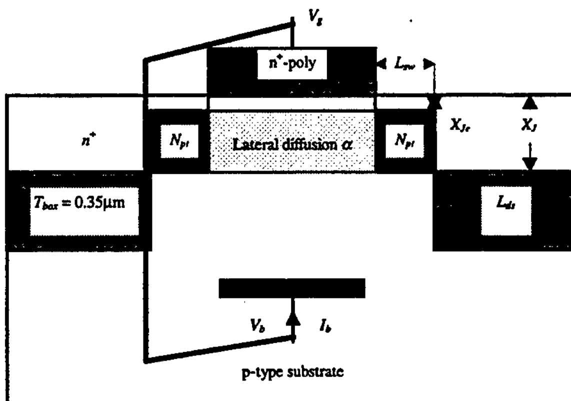


Fig. 8. Comparison of *T*ox dependence of *tpd* for 0.07μm bulk CMOS inverters. *Vth* = 20%*Vdd*. A DSOI (drain/source on insulator (SiO_2)) structure is also shown to reduce S/D junction capacitance in bulk CMOS.

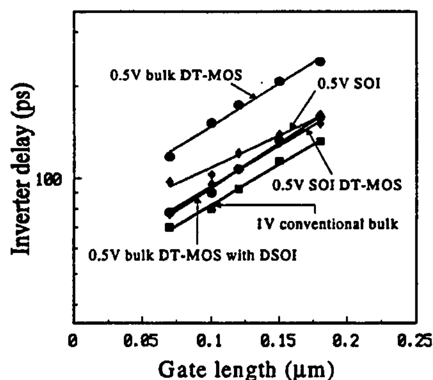


Fig. 9. *tpd* as a function of the gate length for bulk and SOI CMOS. *Vth* = 20%*Vdd*. T_{SOI} = 0.1μm.

4.0 Conclusion

In conclusion, a structure, consisting of shallow source/drain extensions and pocket doping configuration, is shown to have better short channel effects and higher performance figure of merits (*Idsat/Vdd*) under DT operation. Both bulk and SOI DT-MOS are attractive technologies if fast circuit operation at 0.5V or lower voltages is needed. Conventional CMOS can match and exceed DT-MOS performance by operating at a higher voltage with attendant power dissipation. At such higher *Vdd*'s, DT-MOS may be useful as buffer drivers or pass transistors and serve special circuit needs as bipolar transistors do in BiCMOS circuits.

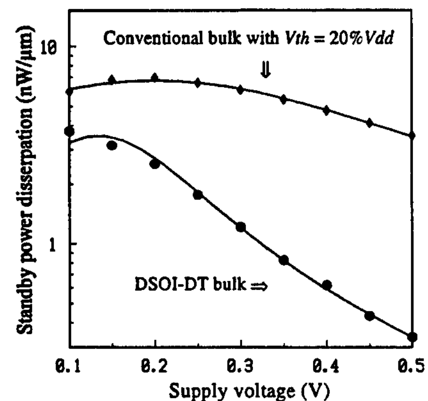


Fig. 10. Standby power dissipation versus *Vdd* for DSOI DT and conventional bulk CMOS with equal gate delay at each *Vdd*, *Lg* = 0.07μm.

Acknowledement: This work was supported in part by *NSF* under ECS-9634217 and *ONR* under FDN00014-96-1-0369.

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STRAIN DEPENDENT CHARACTERISTICS OF SILICON MOSFET's AND THEIR APPLICATIONS

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The piezoresistive properties of bulk silicon have been well studied[1]. However, the effect of strain on FETs fabricated on silicon has been relatively little investigated. The earliest systematic studies of the strain dependence of FET characteristics appear to be that of Dorey and Maddern[2] who measured the characteristics of p-channel enhancement mode MOSFETs fabricated on the silicon <111> surface. They observed a 2% change in the drain current for a stress of 1×10^9 dynes/cm^2.

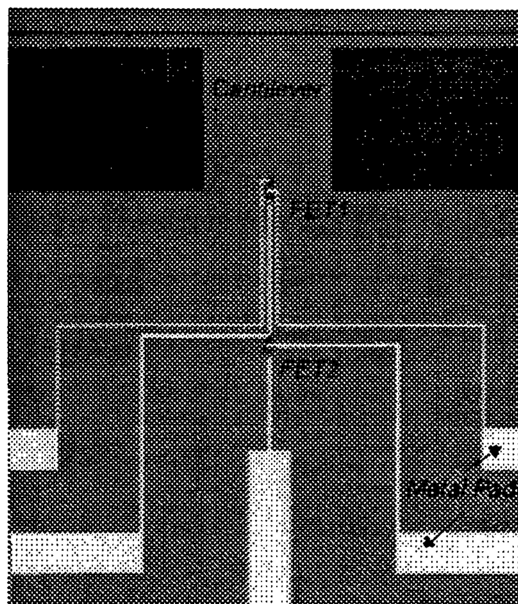

Figure 1: Photomicrograph of the two MOSFETs laid out on the silicon cantilever.

In this paper we report recent measurements on the strain dependence of silicon MOSFETs strategically placed on cantilevers micromachined from 200 μm wafers with a <100> orientation. The micromachining of the cantilevers from silicon was carried out at the AEPL of the University of Virginia.

In figure 1 we show the layout of the MOSFETs on the cantilever. Two transistors were designed into each cantilever in order to permit a differential measurement of the strain characteristics. The characteristics were mapped with a Hewlett-Packard curve tracer. The results obtained on a typical device not subjected to any external strain are shown in figure 2.

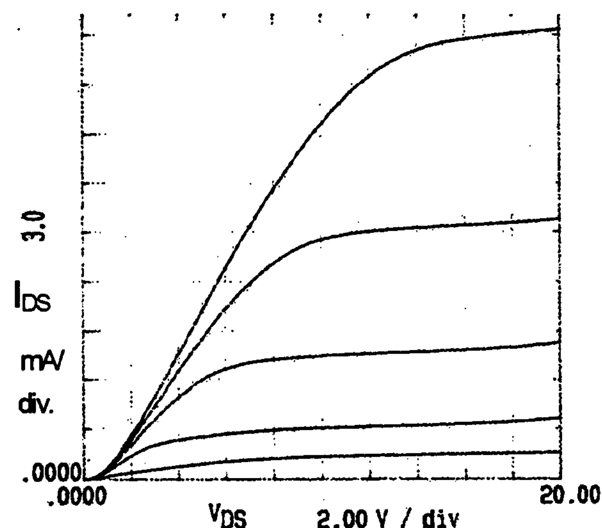

Figure 2: Shows the typical characteristics of the fabricated MOSFETs at room temperature.

The characteristics of the MOSFETs were also measured under both static and dynamic applied strains. In figure 3 we show the output voltage from a unity gain differential amplifier when the cantilever is

strained at 1 Hz with an amplitude of 10^6 Pa. The response to strain is smaller at lower gate voltages where the transistor is in the linear region. A significant improvement is obtained when the MOSFET is operated in the saturation region.

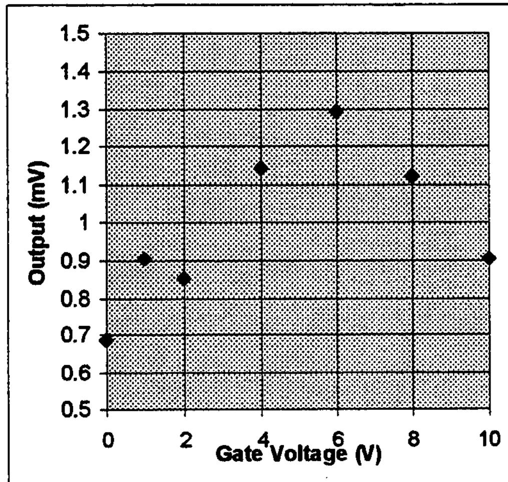

Figure 3: Shows the output voltage induced under a stress of 10^6 Pa applied at a 1 Hz rate. Note the maximum as function of gate voltage.

In all our measurements we obtained easily measureable changes and our results are superior to those published in earlier papers on silicon MOSFETs. Fabrication of such strain sensitive MOSFETs on GaAs would also be of interest. The piezoelectric property of GaAs not present in silicon might provide a superior performance[4]. However silicon has distinct advantages owing to it's mechanical properties.

These MOSFET integrated cantilevers will find a natural use in areas where strain sensors and pressure gauges are employed. Such cantilevers also have unique applications in the fundamental studies of materials properties such as magnetometry and atomic force microscopy.

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CHARGE WAVE DYNAMICS IN A THIN FILM GUNN DIODE

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Dynamics of space charge waves in the thin film diode with the negative differential mobility is investigated. Experimental results tend to confirm that a quasiregular multiple domain mode can exist in a homogenous sample. Some applications of the GaAs driving diode in electrooptical processing devices are considered. Proposed characteristics of an optical 10 GHz band diffraction cell with acting charge wave are calculated.

Since the Gunn effect was discovered in 1963, a large number of papers have been published where the various aspects of this interesting phenomenon have been investigated [1]. From the physical point of view a few types of the dynamic instabilities have been studied exhaustively. These well known objects are the moving dipolar, cumulative domains and the electron waves of small amplitude.

The semiconductor diode with the negative differential mobility [NDM] is a unique natural example of a macroscopic system far from equilibrium and many interesting non-linear wave phenomena, besides domains, may be observed in this active media. The recent developments of the non-linear wave theory give some fresh possible approaches to the problem. For example, in [2] the equations of space charge dynamics are presented in the Korteveg - de Vries equation form. The equation has an analytical solution known as soliton [3]. Therefore, it is reasonable to expect that some soliton-like features ought to be observed in the specimens with the NDM.

Certain signs of the wave nature of the moving Gunn domain manifested themselves in the diodes of high quality. The current oscillations have the marked harmonics of the main transit-time frequency; the current pikes are doubled and may be accompanied by satellites. In experiments [4,5] the switching and competition between the main and one of the high-order mode of generation were observed. It was noticed also that the smaller was the diode thickness the stronger was the deviation from the regular process.

To find out the causes of the features mentioned we have investigated the diode behaviour in more detailes, varying their thickness and also the electric loading of the diode surface. Some results are presented in this paper.

The group of diodes were taken with an ordinary regular domain-type generation. The typical form of the current oscillation [diode # 6K2] is shown in Fig. 1; the upper line is the zero current level. The diode thickness was diminished successively by the chemical-mechanical polishing and the current deviations were monitored. The planar type diodes used in the experiments were made of the epi-layer GaAs wafer with the electron concentration $n = 2 \cdot 10^{15}$ cm^{-3} and the mobility 6.300 $cm^2/V \cdot c$. The ohmic Au-Ge contacts were

evaporated on the facets of the samples. The diodes were of 600 mkm length and width in average, the initial thickness of the active layer was near 40 mkm.

The character of generation changes qualitatively when the diode thickness is reduced to about 15 mkm. In the diode current the second harmonic of the main transit-time frequency arises markebly. Also the threshold voltage and the transit time increase probably because of the bias field becoming more uniform.

When the diode thickness reaches the value of about 8 mkm the character of generation changes radically. With the bias voltage near the threshold the modified single domain mode occures. If the bias voltage is increased the diode current oscillates at any n-th {n=2-3-4 F} harmonic of the main frequency F. During the bias pulse the modes of oscillation alternate chaotically, i. e. the competition of modes occures. The order of the dominant mode depends on the applied voltage nonmonotonically. The current forms of the same diode # 6K2 with thickness near 7 mkm after polishing are shown in Figs. 2-4; the bias voltage V is given in these figures. We suppose the observed picture of oscillation is produced due to excitation of multiple space charge domains moving simultaneously within the sample.

The origin of the multiple domain modes may be explained by taking into account the model described in [6]. Briefly, the domain may be presented as a sum of the time-spatial harmonics $E_n(t,x) \sim E_n \exp j(\omega_n t - k_n x)$, $k_n = \omega_n/v_0 - j \cdot \alpha(\omega_n)$, $\omega_n = 2\pi n v_0/L$, n - the order of the harmonic, L - the sample length, v_0 - the velocity of carriers. In a thick diode all harmonics are synchronized by the main harmonic n=1 because it is a dominant in 'one-dimensional' diode and the single-domain mode occures. In contrast in thin film diodes the factor of amplification $\alpha(\omega_n)$ may have a maximum for any n>1 (space-charge waves of small mode order n fade more intensively at the surface boundaries [7]). In this case the dominant n-th mode can form the n-domain stationary wave. In terms of large signal analysis the magnitude of the first rising domain is limited because of field scattering at the boundaries; as result the electric field outside of the domain not falls enough to prevent the nucleation of subsequent domains.

Investigation of the charge wave phenomena is of interest because of possible application of the NDM diodes as an active steering element in processing optoelectronic devices. Propagating along the sample, the space charge wave induces electrooptically an optical phase grating so that the condition for light diffraction is provided. Efficiency of the diffraction interaction is expected to be high in the integral structure consisting of the NDM diode and optical waveguide. Analogous technique was used in [4].

The application of the electrooptical interaction of light with carrier waves gives certain advantages as compared with acoustooptical or magnetooptical processing devices, especially in microwave frequency band. Our calculation has shown that expected characteristic of an optical 10 GHz band diffraction

cell with NDM diode as a guide of spatial phase grid are quite reasonable for the practical use.

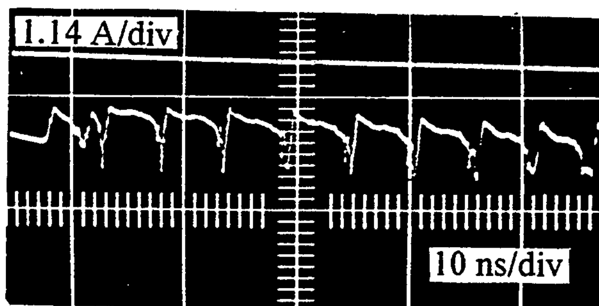

Fig.1 V=190 V

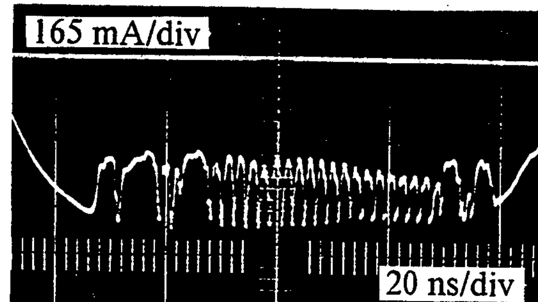

Fig.2 V=200 V

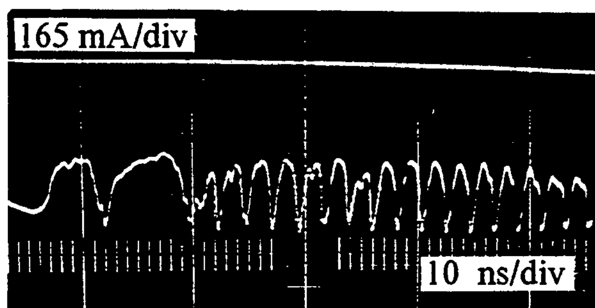

Fig.3 V=200 V

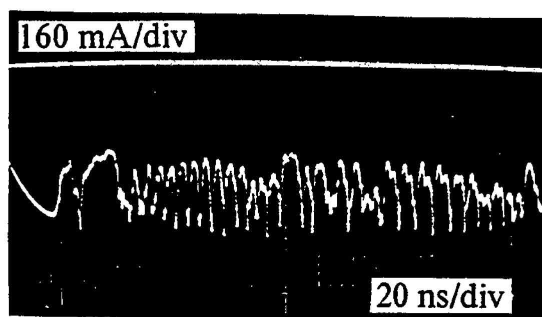

Fig. 4 V=260 V

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Resonant Tunneling Field Emitter

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In a recent work [1] we proposed a new field emitter with potential applications in vacuum microelectronics and sensor technology. The current-voltage characteristic of a resonant tunneling structure quantum mechanically coupled to a vacuum gap is significantly different from that of the conventional Fowler-Nordheim field emitter. First, the voltage drop within the insulating (or semi-insulating) barrier regions reduces the potential barrier for electrons incident on the vacuum gap [2]. Furthermore, the tunneling current is enhanced by the resonant nature of transmission in a multibarrier structures. The resonant tunneling also results in an approximately monoenergetic distribution of electrons within the vacuum gap. Consequently, the interference effects within the classically accessible region of the vacuum gap (investigated in [3] for a Fowler-Nordheim field emitter) are well resolved and produce an oscillatory dependence of the current density on the gap width s and the applied voltage across it, V_g. The proposed structure shown in Figs. 1a and 1b increases the current density even for low field emission.

The main purpose of this work is further reduction of the field levels in both the resonant tunneling filter and within the vacuum gap. This is critical for both experiemental implementation and the reliability of the device.

A structure similar to that shown in Fig. 1a (one barrier energy filter) was recently investigated with an emphasis on the narrow electron energy distribution [4] and the increased current density computed in the WKB approximation [2]. Apart from different material selection and more elaborate computational technique this work differs from [2, 4] in that we include the electron wave reflection at the anode in order to investigate the oscillatory dependence of the tunneling current on the vacuum gap separation and the applied voltage. Furthermore, the introduction of the double barrier energy filter shows the possibility of significant increase in the tunneling current density simultaneously with the relatively low ($\leq 0.1V/\mathring{A}$) vacuum field levels.

We investigate these effects using a model of the tunneling current based on a one-electron effective mass approximation. The current density is given by [5]

$$J = \frac{em^* k_B T}{2\pi^2 \hbar^3} \int_0^\infty \bar{D}(E) dE, \tag{1}$$

where

$$\bar{D}(E) = D(E) \times \ln\left\{\frac{1+\exp[(E_f - E)/k_B T]}{1+\exp[(E_f - E - eV_s - eV_g)/k_B T]}\right\}, \tag{2}$$

m^* is the effective mass within the contact regions, k_B denotes Boltzmann's constant, T is the absolute temperature, voltages V_s and V_g are defined in Fig. 1, E_f is electron imref in the left contact, and the transmission coefficient D is computed using Airy's function version of the transfer matrix method [6].

We consider two types of the resonant tunneling injectors corresponding to a single (Fig. 1a) and double barrier (Fig. 1b) heterostructures. In the case of the emitter shown in Fig. 1a the vacuum gap forms the second barrier required to achieve the resonant transmission.

Most of the numerical results are presented for $CaF_2/CoSi_2$ based structure which is known to produce high-quality tunneling devices [7]. The material parameters (cf. Fig. 1) E_f=13 eV, $m^* = m_0$ for $CoSi_2$ and $m^* = 0.5m_0$ for CaF_2, χ=2 eV, and ϕ=5 eV are taken from [7, 8]. The Fermi energy level E_F=12 eV, barrier height χ=2 eV, and the work function ϕ=4.25 eV are those of [9] for Al/Al_2O_3 structure.

The energy dependence of $\bar{D}$ (transmission coefficient modified by the electron energy distribution factor) for a device with a double barrier heterostructure (cf. Fig. 1b) using $CoSi_2/CaF_2$ is

shown in Fig. 2 for V_s = 4V, V_g = 8V and s = 100Å. The tunneling current density is dominated by a sharp resonance at E = 12.8427 eV just below the imref, E_f = 13 eV (all energies are counted from the bottom of the conduction band of the left contact). The almost monoenergetic nature of electron flux incident on the vacuum gap results in the oscillations of the tunneling current considered as function of the gap separation [1] or the applied voltage (Figs. 3 and 4). For a conventional Fowler-Nordheim injection (cf. curve (c) in Figs. 3 and 4) these oscillations are partially suppressed as a result of the relatively wide electron energy distribution [3, 10].

A high sensitivity of the tunneling current to the vacuum thickness may find applications in the tunneling displacement transducers. The objective is to eliminate interatomic forces between the electrodes and to expand the dynamic range of sensor by increasing the tunneling gap distance by more than an order of magnitude [11].

The current - voltage characteristics of the resonant tunneling field emitters (Figs. 3 and 4) show a significant increase in the current density as compared to a Fowler-Nordheim injection. An appreciable current is computed for the vacuum gap field of about 0.1 V/Å as compared to 0.5 - 0.8 V/Å in Si - based field emitters [12]. This increase in the current density is due in part to the bias voltage V_s which reduces the vacuum barrier height for the incident electron beams by eV_s (Figs. 1a and 1b). The tunneling current is further increased as a result of resonant transmission.

Current density dominated by a sharp Lorentzian peak of the transmission coefficient can be approximated at zero temperature by [13, 14]

$$J \simeq \frac{em^* v_w}{2\pi\hbar^2(s_w + \eta)} \frac{D_L D_R}{(D_L + D_R)}(E_f - E_r) \quad (3)$$

where E_r is the resonance energy, D_L and D_R are the transmission coefficients of the structure located in the left and right side of base region (region 3 in Fig. 1a or region 5 in Fig. 1b), v_w is the electron velocity within the quantum well (base region), s_w is the width of base and η is a quantum correction to the classical oscillation period.

This result is valid assuming transmission coefficients $D_L \ll 1$ and $D_R \ll 1$. For a single barrier emitter (Fig. 1a) the first barrier is to the left of the well and D_R is the transmission coefficient of the vacuum gap. For a double barrier device (Fig. 1b) the first potential barrier is again defined to be to the left of the well (region 5), and itself represents a resonant tunneling structure made of regions 2, 3 and 4.

In both devices D_L is independent of V_g, while $\ln D_R \propto -s/V_g$. Consequently, for sufficiently high V_g, $D_R \gg D_L$ and $J \propto D_L$ is approximately independent of V_g. Note that the saturation of current density requires only that $D_R \gg D_L$, **not** $D_R \sim 1$ so that in the current saturation region the transmission coefficient of the device shown in Figs. 1a and 1b does not loose its resonant character.

The relation $J \propto D_L$ also explains the difference in the saturation current levels for a single and double barrier injectors. In a double barrier device D_L can be made much higher by resonant tunneling.

The effective symmetry concept [15, 16] can be used to further optimize the double barrier structure. The maximum transmission coefficient of the left resonant tunneling energy filter is given by [13, 14]

$$D_L^{max} = \frac{4D_1 D_2}{(D_1 + D_2)^2} \quad (4)$$

where D_1 and D_2 are transmission coefficients of the two barriers of which the energy filter formed (regions 2 and 4 in Fig. 1b). Since the second barrier (formed by part of layer 4 in Fig. 1b) is "downstream" barrier, $D_1 \ll D_2$ and $D_L^{max} \ll 1$. We can somewhat increase D_L^{max} by reducing the thickness of first barrier s_2 as compared to second barrier s_4.

With this in mind consider a structure (using $CoSi_2/CaF_2$) with s_2=16 Å and s_4=24 Å and s_3=20 Å (instead of $s_2=s_4$=20 Å and s_3=50 Å) while the width of base s_5=50 Å is unchanged. The I-V characteristic and the energy dependence of $\bar{D}(E)$ for this structure are shown in Figs. 5 and 6 respectively. The current density increases by a factor of 20 compared to the previous case (Fig. 5). The saturation of current occurs at higher vacuum voltage (corresponding to $D_R \gg D_L$) which is a direct result of a higher D_L.

One disadvantage of the structures considered so far is a high field within the CaF_2 regions (10^7 V/cm). This problem can be alliviated using thicker insulator layers. In a structure with s_2 = 20 Å and s_4 = 60 Å a significant current density (190 A/cm^2) is computed for V_s = 5 V , V_g = 2 V

and s = 100 Å (Fig. 7). This corresponds to the insulator field, $F_{CaF_2} = 6.2\times 10^6$ V/cm. In addition, the vacuum field level is reduced to below 0.02 V/Å as compared to 0.1 V/Å in Fig. 4 and 0.5-0.8 V/Å in Spindt type emitters.

In summary, it appears that it is possible to obtain a significant tunneling current density using resonant tunneling field emitter. Increase in the current density can be achieved simultaneously with lower applied electric field within electron energy filter ($\leq 7\times 10^7$ V/cm) and vacuum gap ($\leq$ 0.02 V/Å).

ACKNOWLEDGMENT

The authors would like to thank Dr. B. Gelmont for several illuminating discussions of this work.

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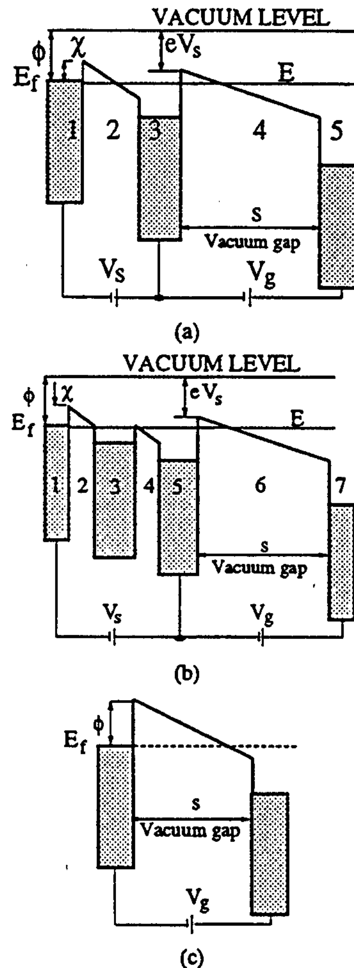

Figure 1: Resonant tunnelling emitter with one (a) or two-barrier (b) heterostructure coupled to a vacuum gap; (a) 1, 3, 5 - $CoSi_2$ (Al); 2 - CaF_2 (Al_2O_3); 4 - vacuum gap; (b) 1, 3, 5 - $CoSi_2$ (Al); 2, 4 - CaF_2 (Al_2O_3); 6 - vacuum gap; Fowler-Nordheim field emitter (c).

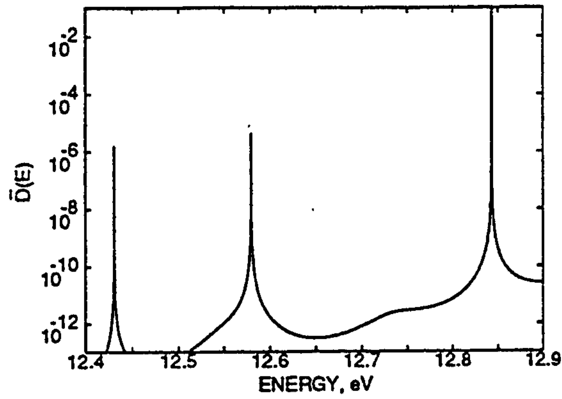

Figure 2: Energy dependence of $\bar{D}(E)$ for the tunneling structure shown in Fig. 1b using $CoSi_2/CaF_2$ with s_2=s_4=20 Å, s_3=s_5=50 Å, s=100 Å, V_s=4V, and V_g=8 V.

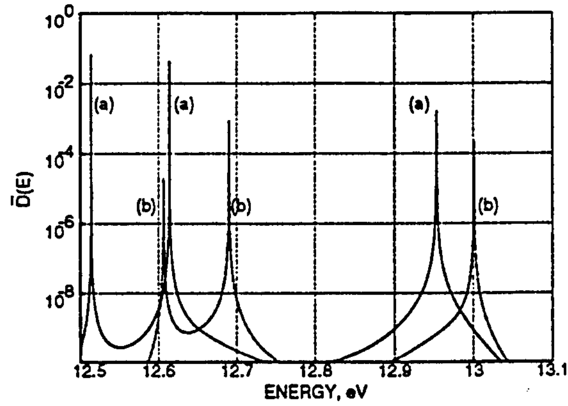

Figure 5: Energy dependence of $\bar{D}(E)$ for the $CoSi_2/CaF_2$ based structure shown in Fig. 1b with s_2=16 Å, s_3=20 Å, s_4=24 Å, and s_5=50 Å (a) and with s_2=s_4=20 Å, and s_3=s_5=50 Å (b). In both cases s=70 Å, V_s=3.8 V, and V_g=10 V.

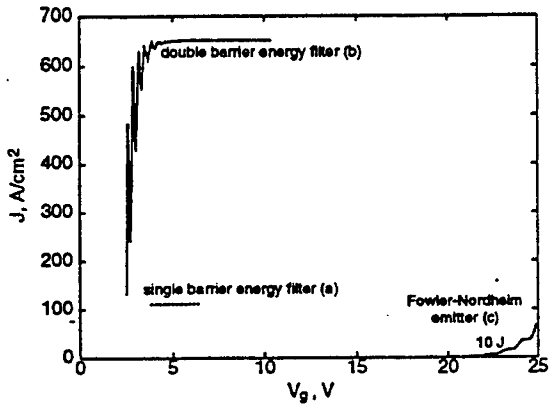

Figure 3: Current-voltage characteristic of Al/Al_2O_3 based field emitters shown in Fig. 1a with s_2=40 Å and s_4=30 Å (a), Fig. 1b with s_2=s_4=20 Å and s_3=s_5=30 Å (b) and Fig. 1c (c). In all cases s=100 Å and V_s=3.7 V for curves (a) and (b).

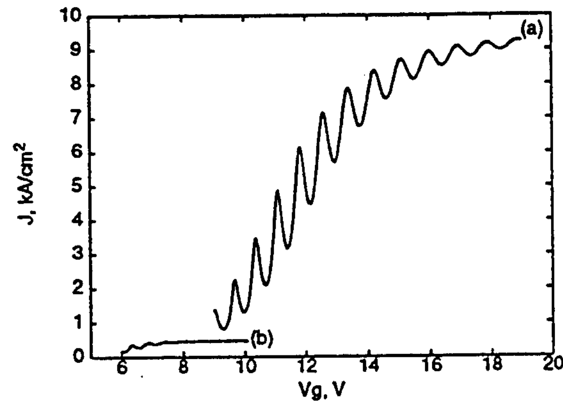

Figure 6: Current density as a function of V_g for the tunneling structure shown in Fig. 1b. Curves (a) and (b) represent the same cases in Fig. 5.

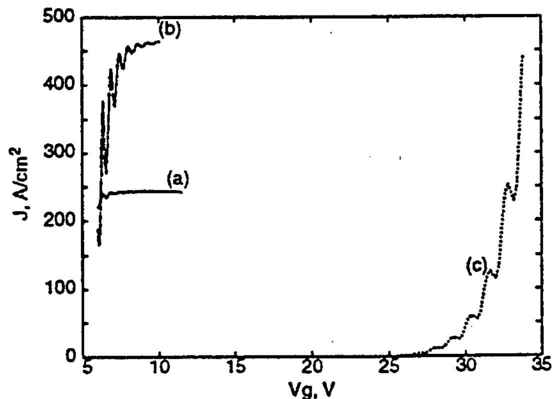

Figure 4: Current-voltage characteristic of $CoSi_2/CaF_2$ based field emitters shown in Fig. 1a with s_2=40 Å and s_4=50 Å (a), Fig. 1b with s_2=s_3=s_4=20 Å and s_5=50 Å (b), and Fig. 1c (c). In all cases s=70 Å, and V_s=3.8 V for curves (a) and (b).

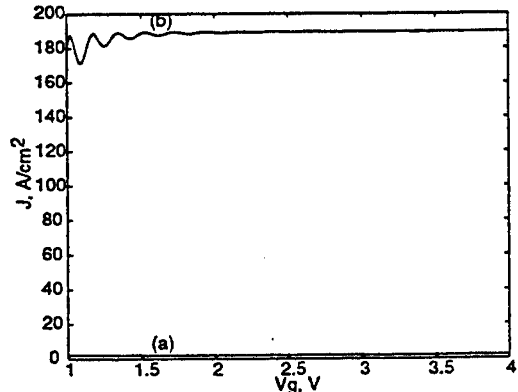

Figure 7: Current density as a function of V_g for the $CoSi_2/CaF_2$ based structure shown in Fig. 1a with s_2=80 Å, s_3=50 Å (a) and Fig. 1b with s_2=s_3=20 Å, s_4=60 Å, and s_5=50 Å (b). In both cases V_s=5 V and s=100 Å.

Yamanov I.L. Muravskiy B.S. Grigorian L.R.

Transistor structure with distributed emitter p^+-n-junction as a new type of a gear with charge accumulation.

As a rule, the transistor structures that are widely used in a modern electronics engineering have collector area noticeably exceeding emitter area, and the absolute valve of transmission factor of a current in the circuit with common base is less then one.

The present message deals with the electrophysical performances of transistor structures that at first, square of collector junction is several orders less than emitter square and secondly, on collector junction which further we call "active contact", there is a current increasement even in that case if the structure is connected under the circuit with common base. The role of an active contact (AC) can be played by metal-tunnel-oxide semiconductor (MTOS-contact) or local n^+-p-junction which with n-area of a structure makes the transistor with the torn off base (Bispin-structure). Both types of structures in fact represent structures with distributed emitter p^+-n-junction and local AC with current increasement.

Figure 1 shows the schematic aspect of structure. The physical processes in structures with distributed p + -n-junction and production processes of structures were considered in works [1-4]. On a base of considered structures series of a new gears were developed permitting effective transformation of potency light and a microwave - radiation, constant voltage resistance capacity into a sequence of impulses, which will be precisely transformed to a machine code or can be immediately used in digital devices of information processing.

As it was shown by our detailed researches of full differential conductivity of both types of structures their physical properties essentially differ from usual transistor structures and important process defining specificity of performances of structures is considered in the present message the process of accumulation of a charge of holes in n-area base of a structure.

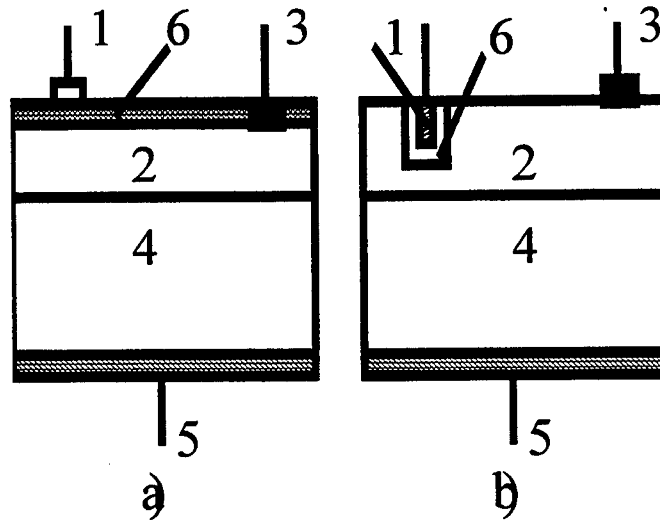

Fig.1.

The schematic aspect is exemplar with distributed p^+-n-junction.

2- n-region, 4-p^+-region, 3,5-ohmic contacts,

a) 1-contact metal tunnel oxide, 6-tunnel oxide,

b) 1-n^+-region, 6-p-region.

The process of accumulation of holes is stipulated by the following reasons. When applying to active contact of an inverse voltage extraction of holes from base begins, and as the thickness of base is 10-15 microns the extracting seizes all area base. A negative gradient of concentration occurres along it in the direction to active contact, and as a result the equilibrium stream of holes from base p^+- area is breaked, and the counter stream of holes from p^+- area appears unstable. It leads to hole accumulation in base, while p^+- area gaines a negative charge equal on magnitude.

The accumulation of holes in base is also due to a voltage drop on a distributed base resistance that for researched structures makes some kOhm. Because of high conductivity the p^+- area potential does not depend on a coordinate and thus voltage along distributed p^+-n- junction will vary, and that is why in a local area under active contact there is a p^+-n- of junction direct displacement.

Hole accumulation effect is connected with capacity increasement of active contact. It is due to the rebuilding prosess of space charge in the contact area where the ionized donors area substituted by stored holes. It reduces space charge area AK and increasement of it's barrier capacity. Volumetric charge as magnitude remains constant, the voltage drop on active contact accurres and at the same time voltage increasement on a distributed resistance of base can be detected. It leads to increasement of direct displacement on a local area of p^+-n- junction and more intensive injection of holes into base.

All considered processes are interconnected and reduce that in an outcome of accumulation of holes in base and stipulated by this contraction of area of a space charge of active contact happens it by tunnel test reducing in an amplification of a current, switching of a structure to high conductivity or emerging of explosive oscillations of a current through active contact and voltages on p^+- area [2]. Thus the transistor structure with distributed emitter p^+-n- by junction represents a new type of a gear with accumulation of a charge.

Prospects of new gears because of transistor's structures with distributed emitter p^+-n- junction is defined by availability of several channels of control, high sensitivity on an input, large magnitude of an output signal, wide range and simple reorganization of a pulse repetition rate of a current through active contact and sawtooth voltage originating on p^+- of area.

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SUPER-NARROW GAP SEMICONDUCTOR DEVICES

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We propose a new approach to the creation of devices with super-narrow gap ($\Delta = 10^{-6} - 10^{-1}$ eV) semiconductor materials. Our idea to build up such gap is based on the usage of exchange interaction energy in an impurity band of nonmagnetic semiconductors doped with transition elements. Atoms of transition elements are to be used as electrical active impurities at the concentration close to critical concentration of Mott's transition to obtaine strong exchange interaction. In our opinion A^3B^5 semiconductors doped with manganese are best suited for this purpose.

Studies / 1,2 / of resistivity, magnetoresistivity and Hall constant as a function of manganese concentration, temperature and magnetic field in indium antimonide doped with manganese (InSb:Mn) demonstrate that:

1.The impurity band of semiconductor (InSb:Mn) splits into two subbands separated by the hard energy gap Δ.

2.The energy Δ has maximal value $\Delta = 10^{-3}$ eV at the critical concentration of insulator-metal transition in InSb:Mn ($N_{mn} = N_c \sim 2 * 10^{17}$ cm^{-3}) and sharply decreases at the concentration exceeding or less than N_c.

3.The upper subband corresponds to the electron band and the lower band corresponds to the holle.

4.The exchange interaction between holes (p-p), exchange interaction between holes and d-electrons of manganese atoms (p-d), as well as the superexchange interaction between manganese atoms via holes (d-p-p-d-p-p ...) are responsible for the energy gap initiation.

There is no question that super-narrow gap semiconductors are very attractive for a number of applications. A great deal of efforts were undertaken

in our studies to create thermoresistors and cryogenic nuclea detectors based on InSb:Mn and operated at the millikelvine range of temperatures /3,4 /. It was shown that sensitivity of such devices exceeded sensitivity of thermoresistors and cryobolometers made of Neutron-Transmutation-Doped Germanium.

Another apllications of super-narrow gap semiconductors comes directly from the millielectronvolt range of its energy , which may be used for creation of far infrared and millimeter wave devices.

The A^3B^5 semiconductors doped with Mn provide also possibility of Δ-energy upper limit extention. The evaluation of Δ for InP:Mn gives Δ~ 0.1eV (while Mn is the deep level center with the binding energy of acceptors E_a = 0.2 eV).

It is of great interest to create two-dimensional strong correlated electron system based on A^3B^5:Mn. In our opinion magnetic subbands of such structure could be extremely sensitive to the external magnetic field. It opens possibilities to create magnetic-tunable two-dimensional devices. Previously the external magnetic field was succesfully used in our studies to tune resistivity (sensitivity) of thermoresistances and cryogenic bolometers made of bulk InSb single crystals /4/.

We should keep in mind that homogenious distribution of impurity (manganese) centers in the crystalline lattice are of great importance for Δ - obtaining. So MOCVD, LPE and MBE -technologies are best suited for Δ-energy creation.

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Speed of operation of light-emitting thyristor-like structures for incomplete gate turn off regime.

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Numerious experimental results for the light-emitting (LE), including lasing (L), thyristors have been reported recently [1-3]. Thyristor-like P^+npN^+ structures (TLSs), which can have S-shaped IV-characteristics, posses another unique property. The gate current (see Fig.1) in the range of incomplete gate turn off regime controls reversibly the width of current conducting region (ON-region), if the condition $\alpha_I + \alpha_{II} > 1$ is satisfied (here α_I and α_{II} are transport factors of injected current carriers for inner bases I and II, respectively). This property allows us to modulate a current density and concentrations of minority carriers in this region, i.e. to control intensity of light emission and regimes of laser operation.

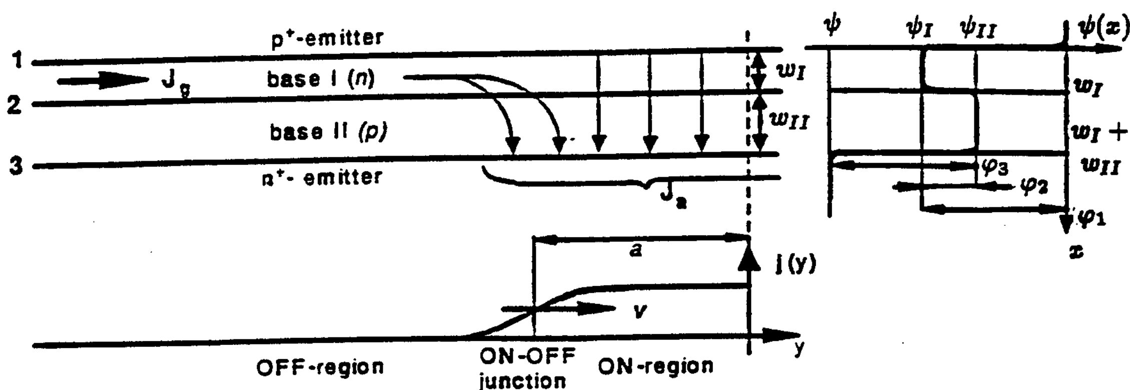

Fig.1. Considered thyristor-like stucture (TLS) with the distributions of the current density $j(y)$ and the potential $\psi(x)$ in it.

The structures of LE TLS and especially L TLS differ greatly from the structure of conventional silicon-controlled rectifiers. For LE and L TLSs the lengths of the *ON*-region, the blocking (*OFF*−) region and the transition region (*ON*/*OFF*-junction) are much greater than the width of gated (controlling) base I (w_I) as well as the width of controlled base II (w_{II}). Therefore, assuming the low injection level at least in gated base I, we can consider quasi-one-dimensional (in x-direction) distribution of minority carrier concentration in both bases. Then a dependence of concentrations on y is caused only by an y-dependence of the voltage drops across three pn-junctions:

$$\varphi_1(y) = \psi_I(y); \quad \varphi_2(y) = \psi_I(y) - \psi_{II}(y); \quad \varphi_3(y) = \psi - \psi_{II}(y),$$

where $\psi_{I,II}(y)$, are the electrical potentials of bases I and II, respectively, and ψ is the voltage across the TLS.

The system of two nonlinear differential equations of the second order is derived to obtain the stationary current distribution in TLS:

$$\frac{\partial}{\partial y}\sigma_I\frac{\partial\psi_I}{\partial y} = R_I, \quad \frac{\partial}{\partial y}\sigma_{II}\frac{\partial\psi_{II}}{\partial y} = R_{II}, \tag{1}$$

where σ_I and σ_{II} are in-plane conductivities of bases I and II, respectively, and

$$R_{I,II} = \sum_{i=1}^{3} A^{(i)}_{I,II}(e^{\varphi_i} - 1).$$

The coefficients $A^{(i)}_{I,II}$ are determined by geometry and material parameters of the bases. The paper [4] shows an example of numerical solution of Eqs.(1) for low injection levels in both bases (when σ_I and σ_{II} do not depend on $\psi_{I,II}$ and ψ).

If the conductivity of base II is comparatively small ($\sigma_I \gg \sigma_{II}$), we can use the particular solution for the second equation of Eqs.(1) to express ψ_{II} through ψ_I and ψ and to modify the system to a single equation for ψ_I. (See [5] for detailed example of these approach.)

One of the most important characteristics of the gate control of LE and L TLSs is the speed of transient processes. Here we solve the nonstationary problem assuming small controlling gate current. In the framework of this assumption we can exploit the stationary wave approach and modify nonstationary problem to the stationary one by introducing a new variable y' instead of y:

$$y' = y - vt,$$

where t is the time and v is the velocity of wave front (ON/OFF- junction). This approach is valid only for the processes that change the current density in the ON-region and the velocity itself slightly. That means that the width of the ON/OFF-junction should be much less than the width of the ON-region. For the case of stationary wave Eqs.(1) are to be transformed to

$$\frac{\partial}{\partial y'}\sigma_I\frac{\partial}{\partial y'} = R^{(0)}_I + v\frac{\partial}{\partial y'}R^{(1)}_I, \quad \frac{\partial}{\partial y'}\sigma_{II}\frac{\partial}{\partial y'} = R^{(0)}_{II} + v\frac{\partial}{\partial y'}R^{(1)}_{II}, \tag{2}$$

where $R^{(0)}_{I,II}$ are the same expressions as $R_{I,II}$ from Eqs. (1); $R^{(1)}_{I,II}$ are the similar expressions with new coefficients $B^{(i)}_{I,II}$ instead of $A^{(i)}_{I,II}$. These forms of Eqs.(2) are results of linearity of transport equations in both bases and of the small voltage drops across the bases in comparison with the voltage drops across the pn-junctions. The specific forms of the coefficients $A^{(i)}_{I,II}$ and $B^{(i)}_{I,II}$ depend on the type of transport in the bases and are defined by their parameters. More detailed expressions of Eqs.(2) for the case of homogeneous doping and of low injection level in both bases can be found in [7].

The assumption of the small velocity v is used to derive Eqs.(2). Using the same procedure as in the stationary case, we can again modify the problem to a single differential equation. To express the velocity v through the other parameters of the

problem apply the conventional procedure of theory for nonlinear stationary waves in homogeneous medium [6] and obtain:

$$v = [J_g^2 - J_{g0}^2(j)]/[2\tau j]. \quad (3)$$

Here J_g is the gate current (in A/cm), j is the current density (in A/cm^2) in the ON-region, J_{g0} is the gate current which provides a neutrally stable position of the ON/OFF-junction for a given current density j. For low injection levels in both bases $J_{g0}^2 = k \cdot j$. In case of homogeneously doped bases, discussed above, the expression for k can be found in [5]. Besides, Eq.(3) contains the important parameter τ which determines the speed of operation of TLS. If base I is doped much heavier than base II ($n_I D_I \beta_I / n_{II} D_{II} \beta_{II} \ll 1$, where n_I, n_{II} are equilibrium concentrations of minority carriers, $D_{I,II}$ are coefficients of diffusion of the minority carriers, $\beta_{I,II}$ are inverse diffusion lengths of the minority carriers: $\beta_{I,II}^2 = (D_{I,II}\tau_{I,II})^{-1}$, and τ_I, τ_{II} are carrier life times in bases I and II, respectively) we can present τ in the form:

$$\tau = \tau_I f_I(z_I, z_{II}) + \tau_{II} f_{II}(z_I, z_{II}).$$

The functions f_I, f_{II} depend on dimensionless widths $z_{I,II} = \beta_{I,II} w_{I,II}$ of the bases. Graphs of the functions f_I and f_{II} are presented in Fig.2a,b. It is worth noticing the features of the obtained results. A shortening of base I leads the function f_I to 0 but relatively slightly changes the function f_{II}. Therefore the speed of operation of the TLS is determined mainly by parameters of base II. On the contrary, a shortening of base II leads to the increase of both f_I and f_{II}. They diverge as z_{II}^{-2} at $z_{II} \to 0$. Thus, to avoid large inertion we do not have to shorten base II excessively. The time τ can be small for a small effective length z_I of base I and the moderately long base II ($z_{II} \geq 0.4$).

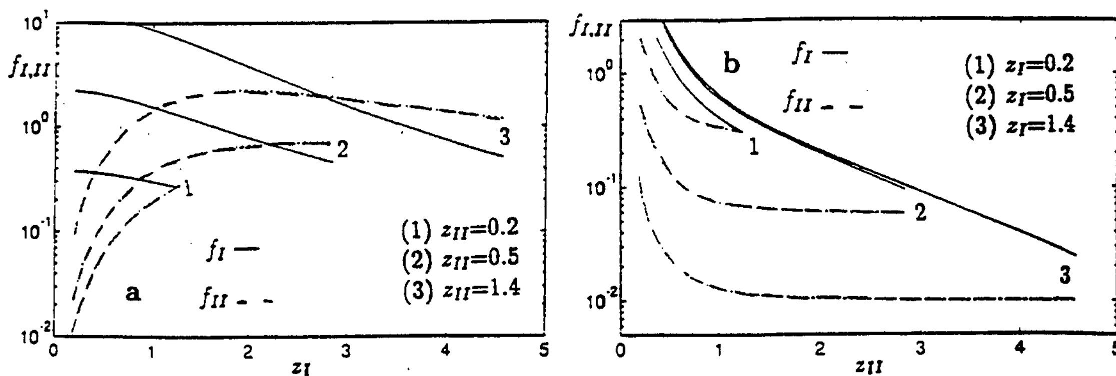

Fig.2. The dependences of two functions f_I and f_{II} from the expresion for characteristic time, $\tau = \tau_I f_I + \tau_{II} f_{II}$, on (a) z_I for given values of z_{II}, and (b) z_{II} for given values of z_I.

We apply Eq.(3) to consider nonstationary (transient and modulation) processes in finite TLS for the gate current $J_g(t)$, which is given function of time, using the equations:

$$v = -da/dt, \quad j = J_a(t)/2a$$

where a is the half-width of the ON-region and J_a is the given anode current. Here we assume that $a(t) \gg \delta a(t)$, where $\delta a(t)$ is the characteristic size of the ON/OFF-junction.

A solution of the obtained differential equation of the first order depends on the only characteristic time $\tau_{eff} = \tau \cdot J_a/J_g$. In contrast to the time τ, which depends only on structure parameters, the time τ_r depends on J_a and J_g (i.e. it depends on a regime of operation, even for assumed low injection levels). Since we can consider only the stationary wave regime with the given $J_g < J_a$, we can obtain only $\tau_r > \tau$.

From the obtained results one can conclude that the smallest τ can be a slightly less than the life time of the minority carriers in base II (τ_{II}). Therefore, small τ_{II} can provide high speed of operation and effective light transmission in LE TLS.

Our results are not valid for the case of the high injection levels for both bases. The approach is also unacceptable for the fastest transient processes caused by large gate current $J_g(t)$, which can not be treated as quasistationary processes.

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THYRISTOR'S SWITCHES WITH TUNNEL DIODE EMITTERS

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1 Introduction

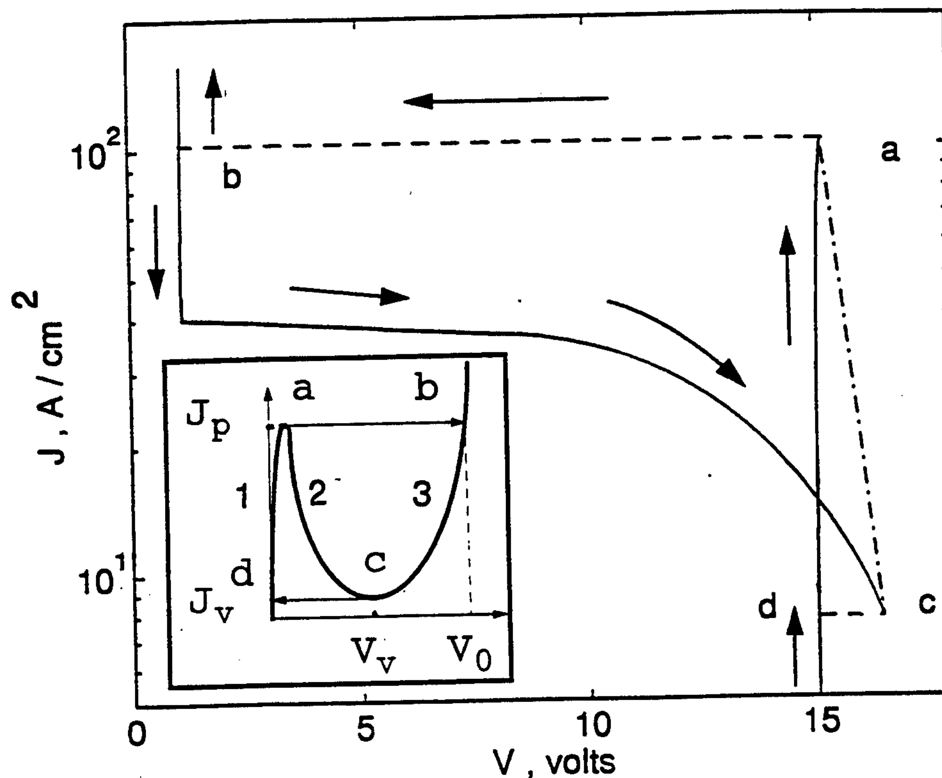
Tunnel diodes are semiconductor devices, well known as negative resistance circuit elements with N-type current-voltage characteristics in the forward direction (see the insert in the Fig. 1). They also serve as suitable connection elements in multijunction semiconductor device structures (for example, in solar cells [1]). We propose a novel application of the tunnel p^+n^+ junction for a thyristor design. In this application the tunnel junction with an N-like forward I-V characteristic is used as one of the thyristor emitters (i.e. as one of the outer thyristor junctions).The switching current is fully determined by a junction peak tunnel current and weakly depends on temperature. The device voltage exhibits discontinuities as the device turns on. Results of numerical simulation of the tunnel emitter's effects on the thyristor's I-V characteristics are presented.

2 Device switching behavior

It is known [2], that the thyristor S-type I-V characteristic is the result of a combination of two different factors. First, a mechanism, which provides a current growth at some critical breakover voltage V_b, must be available. Usually current increases due to avalanche multiplication in the middle (collector) junction of the device or/and punch-through of the lightly doped thyristor base. Second, an increase of injection efficiency of one or both thyristor emitters from almost zero values to the values, close to unity, is another necessary condition for thyristor switching. Currently there are two known mechanisms by which the efficiency increases with injection: (1) Sah-Noyce-Shockley (SNS) recombination[3] through deep centers in the transition region of the emitter junction and (2) emitter shorts[2], which serve as shunts of the emitter junctions at small biases.

Here we consider a third mechanism of injection efficiency increase with the device current. This mechanism takes place if a heavily doped p^+n^+ junction with a tunneling N-type current voltage characteristic is built up at the transition region between the outer region of the device and one of the thyristor base (that means that we consider $(p^+n^+)npn^+$ structures instead of traditional p^+npn^+ devices). Because at low forward biases the current of such an emitter is solely due to Zener's band-to-band tunneling, the injection efficiency γ_1 of this junction is equal to zero. An increase in current J due to avalanche or punch-through of the second base (not adjacent to the tunnel emitter) does not change γ_1, because for currents $0 < J < J_p$ (in the region 1 of the I-V curve, shown in the insert of the Fig. 1) the tunneling current dominates over the recombination and injection components of the total junction current. When the current achieves the peak value J_p, a transition a-b occurs and the voltage V across

the junction suddenly increases to $V_0 = V(J_p)$. We will distinguish two situations. First, at the point, where $J = J_p$ and $V = V_0$ the efficiency γ_1 is controlled by the SNS recombination. This means that the current J_p is less than J_c - the critical current at which injection starts to dominate over recombination within the emitter transition region. In this case the specific features of the N-type I-V characteristic of the tunnel junction are not important. We are mostly interested in the other situation, when at the point $J = J_p$, $V = V_0$ the injection component of the current exceeds the recombination current (i.e. $J_p > J_c$). In this case the result of the transition a-b is an instant increase of the emitter efficiency from 0 to almost 1. If at this point efficiencies γ_1 and γ_2 of the two outer junctions and emitter-to-collector current transfer ratios α_1 and α_2 satisfy the condition $\gamma_1\alpha_1 + \gamma_2\alpha_2 > 1$ the thyristor turns on at $J = J_p$ and the voltage across the device suddenly drops down. As the current decreases below the holding current the device turns off according to the usual switching mechanism. At $J = J_v$ the voltage across the junction exhibits the discontinuity c-d. The less the difference between J_c and J_v the more abrupt is the the device turnoff.

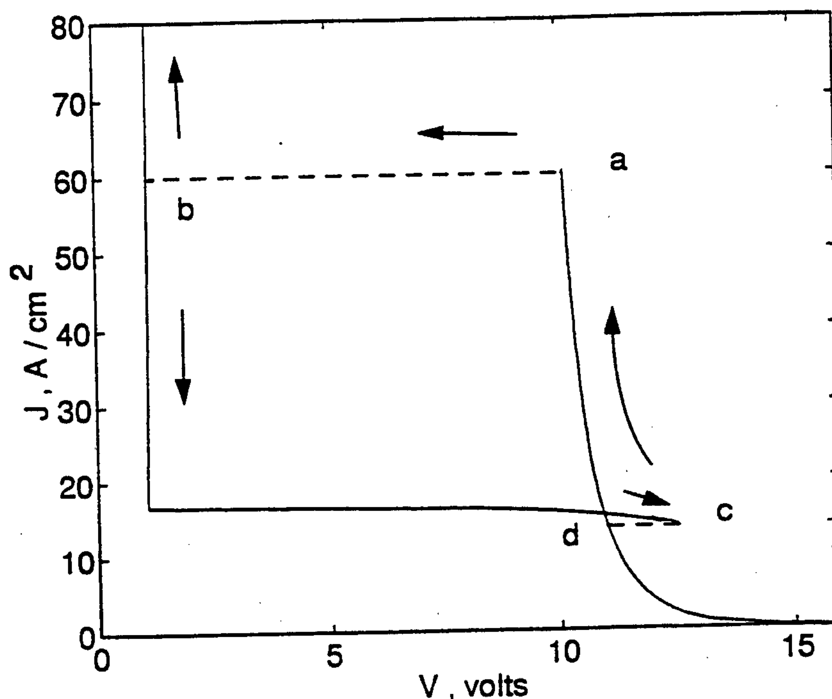


Fiqure 1. Current-voltage characteristic of a symmetric thyristor with two tunnel junctions. An insert shows a schematic view of the tunnel diode I-V characteristics.

3 Simulation results

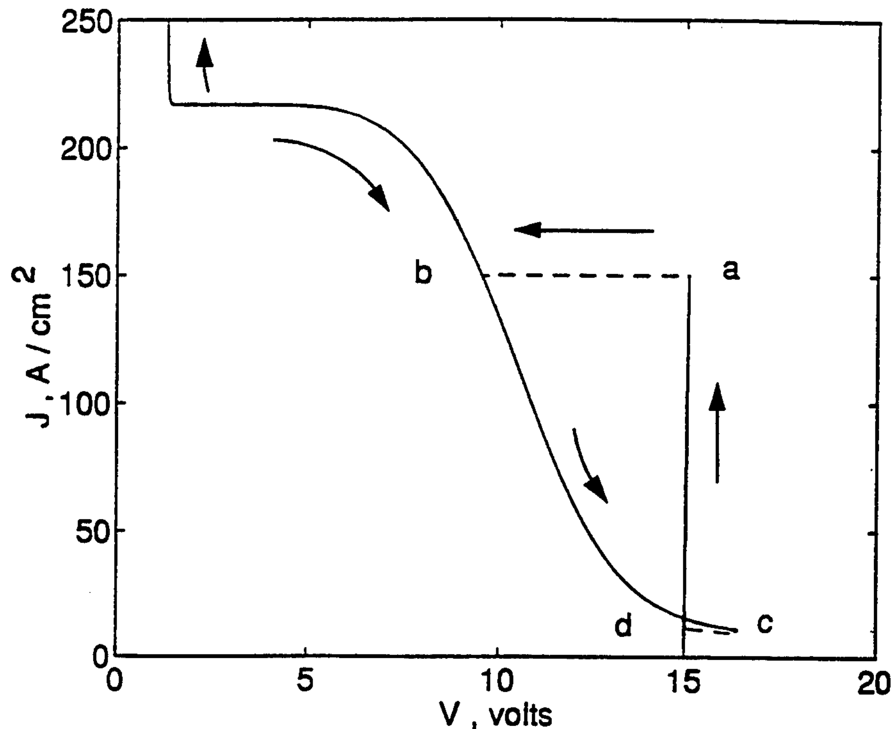
Fig. 1 demonstrates the results of numerical simulation for a symmetrical thyristor with $\alpha_1 = \alpha_2 = 0.93$. Currents J_p, J_v and J_c are $100A/cm^2$, $7.5A/cm^2$ and $38A/cm^2$. Material parameters correspond to $GaAs$. It is seen from the Fig. 1 that there are two abrupt changes of the device voltage at $J = J_p$ and $J = J_v$. There is also a branch c-a of the current-voltage dependence which corresponds to the region 2 in the insert in the Fig. 1.

If a thyristor has only one tunnel junction, adjacent to the base 1, then the device behavior depends also on parameters α_2 and γ_2 of the second base. Fig. 2 shows simulated results for an asymmetric p^+npn^+ structure where only the left junction is tunneling. Parameters J_p and J_v are $60A/cm^2$ and $13A/cm^2$. Currents $J_{c(1)}$ and $J_{c(2)}$ for the left and right junctions are $J_{c(1)} \approx 16A/cm^2$ and $J_{c(2)} \approx 0.05A/cm^2$, i.e. current J_p exceeds both $J_{c(1)}$ and $J_{c(2)}$. Transistor gains are $\alpha_1 = 0.95$ and $\alpha_2 = 0.98$. The first increase in the device current (not seen in the Fig. 2) takes place at $V = V_b \sim 15V$ due to avalanche multiplication in the collector junction. At $J_{c(2)} < J < J_p$ the behavior of the I-V curve is determined by the approximate relationship $\gamma_2\alpha_2M_2 \approx 1$, where M_2 is a multiplication factor for carriers, injected by the second emitter. At $\gamma_2 = 1$ (this corresponds to the voltage $V \approx 12V$ in the Fig. 2) the second breakover takes place where multiplication is still in effect and $M_2 = 1/\alpha_2$. The less α_2, the closer the second breakover voltage is to $V_b = 15V$. We can say that α_2 controls the shape of the I-V characteristic in this case. Note that the current-voltage characteristic, shown in Fig. 2 becomes similar to the curve shown in Fig. 1 at small enough α_2 ($\alpha_2 \approx 0.6 - 0.7$).



Fiqure 2. Current voltage characteristic of a thyristor with one tunnel junction. Transistor's gains are $\alpha_1 = 0.95$ and $\alpha_2 = 0.98$.

If the current J_c for the junction 2 is greater than J_p we obtain a current-voltage characteristic, shown in Fig. 3. The simulation was performed for $\alpha_1 = 0.13, \alpha_2 = 0.98, J_p = 150A/cm^2, J_v = 10A/cm^2, J_{c(1)} = 15A/cm^2, J_{c(2)} = 215A/cm^2$. It is is seen that beside the first breakover due to avalanche at V=15 V there is a region at $8V < V < 12V$, where current J noticeably increases with the decrease in V. At $J > J_p$ we have $\gamma_1 = 1$ and $\gamma_2\alpha_2M_2 + \alpha_1M_1 \approx 1$. It can be easily shown that second breakover voltage decreases as α_1 approaches 1. The type of the I-V curve shown in the Fig. 3 is obviously not desirable for switching purposes and the optimal relationship is $J_p > J_{c(1)}, J_{c(2)}$.



Fiqure 3. I-V characteristic of an asymmetric thyristor with one tunnel junction. Parameters are $\alpha_1 = 0.13$, $\alpha_2 = 0.98$.

4 Summary

In conclusion, we would like to note that the use of tunnel diodes as thyristor emitters may give some advantages over the traditional thyristor design. This is the case, for instance, when SNS mechanism is not effective because of difficulties in controlling the concentration of deep recombination centers during the growth of the thyristor's pn junctions or at high temoeratures. Tunnel emitters may also be used when the technique of emitter shorts is not applicable, like in thyristors with small junction cross areas (for example, light-emitting thyristors for smart pixels). Being added to a thyristor structure, the role of the heavily doped p^+n^+ junction may be twofold. First, they will control the junction behavior at small currents as was described above. Second, their function will be to prevent the thyristor n^+n-base punch-through in the OFF state at such voltages, when the collector depletion region almost reaches the emitter junction. Another useful feature of the tunnel emitters, important for thyristor realizations, is related to a weak dependence of the peak tunnel current J_p on temperature. That specific feature of the tunnel I-V characteristics (in conjunction with potentially high values of J_p up to 1000 A/cm^2 [4]) may essentially expand a range of thyristor operating temperatures.

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AN OPTICAL SENSOR FOR GAS MONITORING

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Student Paper

INTRODUCTION

This paper describes the prototype of selective gas sensors for environmental monitoring of the ambient atmosphere for applications in industry, in other dispersed civil infrastructure systems, and for controlling indoor air quality.

As a result of industrial activity, the concentration of carbon dioxide has increased 20% since preindustrial times, while the concentration of methane is up 50% [1]. As environmental protection strategies progress from simple cause and effect models of pollution prevention to the more sophisticated systems models of industrial ecology [2], one of the most pressing needs is to improve the information-base regarding material and energy flows in systems. Control algorithms to optimize utilization of materials and minimize waste are limited by the availability of accurate, timely, localized information on the concentrations of the products in question. The availability of this information depends in turn on the development of reliable, cost-effective sensors capable of in-situ monitoring of a wide range on substances.

All industrial ecosystem models depend on continuous inputs of energy. Emissions from the use of fossil energy resources -particularly carbon dioxide - have to be controlled if industrial production is to be maintained in an environmentally acceptable way [2]. The elimination or substantial reduction of the environmental pollutants from manufacturing processes and products can only become possible with simultaneous development of the instruments which measure and provide quantitative information regarding their presence. IR spectrometry is currently a particularly important tool for the laboratory study of industrial pollution. There is, however, a need to develop simple, easy to use, inexpensive and reliable devices capable of monitoring industrial gas pollutions in field conditions and for controlling indoor air quality. Currently available sensors suffer one or more of the following disadvantages: loss of calibration over time, high maintenance requirements, high power consumption, expensive, bulky, heavy, fragile, slow, inaccurate.

Demand controlled ventilation to maintain indoor air quality is one example of how continuous and accurate monitoring of CO_2 can produce significant energy saving, thereby reducing atmospheric emissions. Rather than using fixed outside ventilation airflow rate based on peak design occupancy, a CO_2 sensor can be used to provide the amount of outside air ventilation required for the actual number of people present in the zone being controlled [3, 4], thus preventing costly and unnecessary over-ventilation. In one study a constant outdoor air rate allowed peak CO_2 concentration above 800 ppm. A CO_2 sensor-based control kept the concentration below 700 ppm while using 40% less energy than the fixed ventilation rate [5]. In conjunction with variable air volume ventilation systems and variable speed drive fan motors, CO_2 sensors promise enormous energy savings and pollution prevention. Realization of the large potential benefits of this approach depends on integrated control systems, built around low-cost, rugged, reliable sensors.

In this paper we describe a prototype for a carbon dioxide sensor, which when integrated with HVAC controls, promises the dual benefit of reducing air emissions and saving energy, while protecting the indoor air quality. The small size, light weight, low power consumption, fast response time and potentially low cost offer significant advantages over anything now available. By substituting other available emitter and detector elements, the same basic system is capable of measuring a number of other important gases, including carbon monoxide, water vapor, methane, various hydrocarbons, ammonia, and other ozone destructive precursor emissions, and can be used for a variety of applications.

The proposed sensors are solid state and optical. The principle of the method is the absorption of infrared (IR) radiation by the gas molecules at their characteristic absorption wavelengths in the

spectral range between 2.0-5.0 μm. Sensors based on compositionally tuned emitter/detector elements will use as active elements a selective light emitting diode and a pair of matched selective photodetectors. Alloy composition will determine the wavelength of maximum sensitivity. A dual wavelength ratio detection scheme is used.

SENSOR DESIGN

Conventional gas monitors based on infrared absorption typically include a broadband thermal light source with the light beam modulated by a rotating chopper disc to generate light pulses. The system usually incorporates several optical bandpass filters, to provide nearly monochromatic light which passes through the targeted gas and reaches an IR detector. The chopper permits the use of AC signal measurements, thus raising the sensitivity of signal detection and reducing the effects of drift from the amplifier. Two optical bands are usually separated by filtering. These are a band of wavelengths strongly absorbed by the targeted gas, and a band that is not absorbed, which is usually serves as a reference channel. In the range of small gas concentrations, the optical transmittance T of the system, and the intensity of light illuminating the detector are related to the absorbing molecules' concentration C by a logarithmic law

$$-\log T = AC,$$

where A is a constant which is proportional to the product of the absorption coefficient for the gas, and the optical pathlength through the gas. The ratio of the two signals is usually measured which permits reduction of many perturbations due, for example, to fluctuation of source intensity and amplifier drift. These conventional gas monitors have several big disadvantages. The broadband light sources (usually tungsten lamps or glowbars) require high power consumption. Only a very small percentage of this power is used. Most of the energy dissipates in the form of heat causing reduction in the accuracy of measurements. To improve the accuracy, system components, including detector, have to be maintained at a constant temperature. The mechanical chopper makes the system large and consumes energy as well as a moving part that can fail.

Recently mid-infrared light emitting diodes (LEDs) have been developed that offer advantages in the design of gas monitoring sensors. In [6] gas monitors employing infrared LEDs developed by Laser Monitoring System Ltd in the UK have been considered. These LEDs are based on III-V materials, and by suitable tailoring of the LED constituents during manufacture, the emission band can be tuned to a gas absorbing wavelength. It was demonstrated that infrared light emitting diodes can replace the thermal source, bandpass filters and rotating chopper wheel of conventional infrared gas monitors. Long term tests for periods exceeding 15000 h have revealed no gradual change in LED output power, whereas most of thermal sources used in transportable monitors have a relatively short lifetime with considerable aging. Moreover the intensity and peak emission wavelength vary significantly with temperature. PbS or PbSe detectors are the usual detectors in the gas monitors. The detectors have also strong temperature dependence about 1% $^{\circ}C^{-1}$.

In our research, a sensor prototype for monitoring carbon dioxide has been created which employs an LED and a pair of matched photodetectors (PD) developed by ICO Ltd in Russia. Both, the LED and PD are based on polycrystalline thin film technology of lead chalchogenides and operate at room temperature. The internal efficiency for radiative recombination in polycrystalline PbSe depends on doping, and a value as high as 60% has been achieved [7, 8]. The range of sensitivity of the photodetector is 4.21-4.38 mm for the photoconductor sensitive to the absorption of carbon dioxide (see Figure 1), while the range for the reference photoconductor is 3.82-3.97 mm, a range outside of the range of CO_2 absorption. The time constant of the photodetectors is less than 5 ms.
The sensing unit consists of a PbSe LED, PbSe dual photodetectors and an aluminum coated spherical mirror (Figure 2). The dual detectors share the same materials and therefore exhibit approximately the same thermal, optical, and aging characteristics. The benefit of matched detectors is a reduction in error compared to systems using detectors with different operating characteristics. Due to built in, narrow band filters, the sample detector is sensitive in the range of absorption of carbon dioxide and the reference detector is sensitive outside that range. A spherical mirror is used to collect and focus the light of the LED onto the dual detectors.

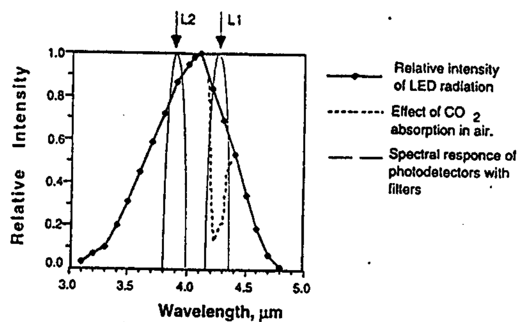


Figure 1. Relative intensity of the light from the uncooled PbSe emitting diode, the effect of absorption of CO_2 in air for the optical path 2 m, and the spectral sensitivity of two narrow band detectors.

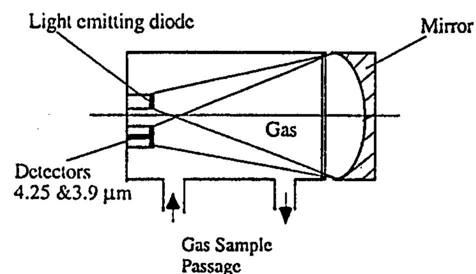


Figure 2. Basic optical setup with mid-IR emitter and two narrow band detectors.

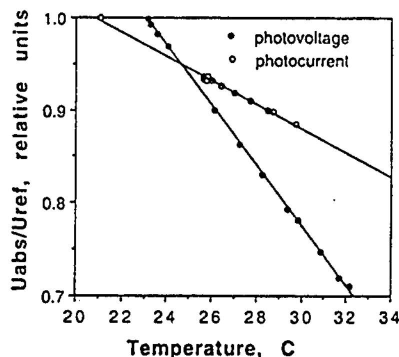
The circuit of the sensor system has been built [9]. The block-diagram includes the LED driver which consists of two voltage-to-current converters generating 1A current pulses at 10% duty cycle and at a frequency 1 kHz, the signal generation oscillator circuit which includes also a decade counter and serves to generate the voltage pulses, the three stage amplifier circuitry for the detector signal amplification, and the signal detection sample/hold circuit with a bandpass filter which integrates the output of the amplifier, holds the signal so that a DC voltage can be produced, and finally resets the circuit. Several criteria are important for design goals of the circuit construction: a) detection noise has to be the limiting factor which determines the sensor sensitivity, b) high circuit stability is required, c) all temperature effects have to be minimized, and d) low power consumption is required.

TEST RESULTS

Test and calibration experiments were performed on the sensor system to determine the ability of the system to accurately monitor the concentration of CO_2. The tests included drift experiments, and the sensitivity of both channel signals and their ratio to temperature conditions. Since the resistance of the PbSe detector has a strong temperature dependence, we have investigated the possibility of utilizing the resistivity of the detector for precise measurements of the detector temperature. The reproducibility of the "zero" signal (both channels of the sensor are exposed to pure nitrogen) has been also investigated.

Calibration experiments for the signal of both channels were performed in 100% nitrogen and at known concentrations of premixed CO_2 with N_2. The results have been used to develop the best algorithm for the sensor output signal. The ratio of signals (A_{rel}) in the absorbing and reference channels was chosen as the output signal, since changes in temperature, source instability, and amplifier drift affect A_{rel} less than each signal alone. Figure 3 shows the temperature dependence of A_{rel} for two different amplifier circuit configurations designed to measure photo voltage signal or photocurrent. The temperature coefficient is much smaller in the second case, however the sensitivity for the CO_2 content is also reduced in this case. Both curves include temperature effects of the circuit itself, which has to be studied separately. Fig. 4 demonstrates the combined effect of the drift and the temperature fluctuation in the ambient air due to the building ventilation system on the resistivity and the ratio of signals. The drift also results from the combination of temperature effects in the circuit and the slow change of detector temperature. The data demonstrate very good correlation between R and A_{ref}.

Figures 5 and 6 demonstrate results of calibration measurements. First, the gas chamber was purged with pure nitrogen and after that premixed CO_2 gases of known concentration were alternated with pure nitrogen starting with the lowest concentration of CO_2. Each gas flowed to achieve a new steady state concentration. The CO_2 content in parts per million is indicated. Calibration of the sensor in the range 0-1000 ppm is shown in Figure 6. This Figure illustrates the expected logarithmic relationship of the output signal to CO_2 concentration over the region 0 to 500 ppm. No temperature correction has been made at this stage which gives large error margins for signals. Data, like those



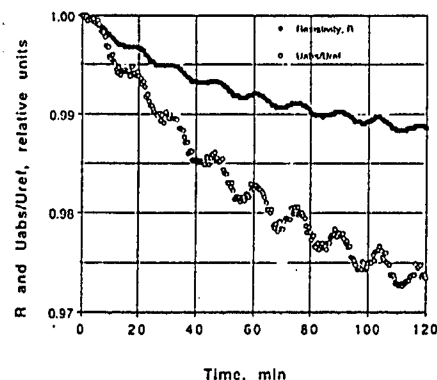


Figure3 . The ratio of signals in the absorbing and reference channels as a function of temperature for two different circuit designs.

Figure 4. The resistivity and the ratio of signals vs. time for ambient air.

shown in Figure 3 provide, however, the necessary information for temperature correction of sensor response.

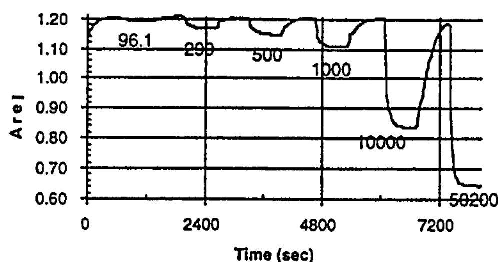


Figure 5. Calibration experiment

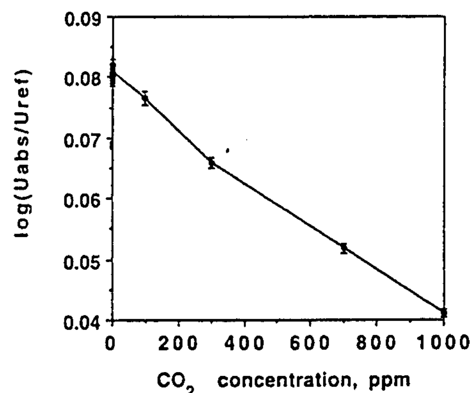


Figure 6. Results of calibration in the range 0-1000 ppm.

CONCLUSIONS

The optical sensor prototype was designed, built and tested to detect carbon dioxide. The optical sensor was tested using nitrogen (0 ppm carbon dioxide) and 6 known concentrations of carbon dioxide. Some preliminary data of the temperature dependence of the sensor system were taken. These results provide the necessary information for temperature correction of the sensor response.

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The Indicator of Dangerous Concentration of Gases and Vapors Based on PbSe-Photoresistors

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The protection of environment becomes one of major problems in the modern world. Gaseous polluting substances, which render negative influence to natural physical and chemical processes and on health of the people, are thrown out in air space in growing quantities. For example, in the last century the concentration of carbonic gas in air has increased more than 2 times, the concentration of methane has increased more than 3.50 times, and the basic increase has occurred in the second half of the current century. Very fast increase of ammonia, nitrogen oxides, and sulfur concentration in air, and pollution air by vapors of a volatile organic compounds is observed also. According to [1], air of large cities contains up to 200 volatile organic compounds. Hens, people need effective methods and devices for controlling undesirable impurity in air of inhabited places and places of industrial activity and for controlling safety of realization of technological processes. At the present, the various companies of the advanced countries produce large assortment of gauges of air pollution by gases and vapors. These devices use various principles of action (electrochemical, thermochemical, catalytic oxidation, photo calorimetric, ionization, optical and other processes) [2]. The leading places in the world market of such devices is occupied by companies: Riken Kaki (Japan), Dragerwerk (Germany), Compur Elektronice (Germany), Bruel and Kjer (Denmark), Àntechnica (Germany) and other.

At the same time, problem of upgrading of existing tools and the creation of new devices with the best parameters is still urgent. It concerns a problem of creation of reliable, sensitive and selective indicators of dangerous concentration of various gases and vapors, capable to work continuously for a long time (during several years) in an automatic mode of operation. Such gauges are necessary, first of all, for maintenance of safe operation of the majority of underground rooms (tunnels, underground collectors, mines, underground warehouses, cellars of industrial and inhabited

rooms, vegetable stores and other objects), in which the occurrence of dangerous concentration of CO, CO_2, CH_4, NH_3, vapors of petrol and other gases and vapors is possible (as a result of work of various devices, during ability to live of the people, as a result of processes of rotting or burning, and for the account of filtration from the ground). The similar indicators can be used for the notification of dangerous concentration of gases and vapors in air of industrial and inhabited rooms, and also as gauges in systems of the automatic control for technological processes, for example, for maintenance of an optimum mode of fuel burning in fire-chambers.

The analysis of produced gauges of dangerous concentration has shown, that the existing devices do not satisfy to some requirements stated above. Thus, for example, various types of sensors, using electrochemical and thermochemical reaction of impurity gases, processes of oxidation of gases on catalysts and other processes, have not necessary selectivity, service life, stability to poisoning impurity. Optical absorption gauges, based on selective absorption of radiation by molecules of pollutant gases, have a prospect of most likely to satisfy the showed requirements. The majority of devices of this type manufactured by an industry use pyroelectric detectors as photodetectors. Advantage of these detectors is an opportunity of work in a wide range of wavelengths. However they have smaller values of detectivity than modern semiconductor photodetectors, which limit threshold values of sensitivity of absorption optical gauges. Moreover, pyroelectric detectors are very sensitive to external mechanical influence.

In the present work, the optical absorption gauge of pollution of air is described which is based on application of a PbSe photoresistor as a detector of radiation. That allows to improve essentially the sensitivity and the stability of the device. In comparison with other types of noncooled detectors, the PbSe-photoresistors have maximum detectivity in the spectral range of 3-5 µm, in which absorption bands of many gases and vapors are available. High parameters of layers of PbSe at rather superficial cooling (253-195 K) allow to apply them with success in a combination with freezer with small (up to 6 W) power input, that allows to increase the detectivity and to expand the area of spectral sensitivity of detectors.

The photoresistors used in this work is a thin film of PbSe on a glass substrate deposited by a method of precipitation from a solution. The sensitive area of the necessary size is formed with by photolithography. The

stability of the photodetector work is provided at the expense of drawing of a thin film of a polymer material on a surface of PbSe, with the subsequent setting of a sensitive element in the tight case. Spectral dependence of photosensitivity of the PbSe-photoresistor at room temperature is shown on Figure 1. Absorption spectra of a number of gases are also shown . The usage of replaceable optical filters makes it possible a detection and a determination of concentration of various impurity in air by utilizing the same device with a PbSe-photoresistor as a photodetector. Detectivity of the photoresistor is $8x10^{8}$cm $Hz^{1/2}$-W^{-1} at maximum of its spectral sensitivity at room temperature.

The basic circuit of the device is shown on the Figure 2. In this circuit, a two-beam principle is used, when the light from a source, ***S***, is shared on alarm, C_S, and reference channels, C_R with different spectral structures of light. The filter in the alarm channel F_S passes the light in a spectral band which correspond to absorption of controllable gases. The filter F_R passes the light in spectral area in which transparency of air does not vary by presence of any probable impurity. Peculiarity of the chosen circuit is the use of the same photodetector, ***D***, for registration simultaneously of an alarm and a reference light flows. For the subsequent division and processing of signals, the light in both channels is modulated by two election-optical modulators, M_S and M_R, having different frequencies. The block of registration and processing, ***B***, allows to set a threshold concentration of

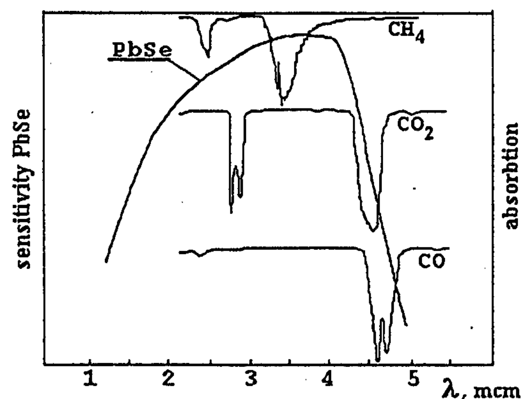

Figure 1. Spectral sensitivity of a PbSe photoresistor, and spectra of absorption bands of CH_4, CO_2 and CO.

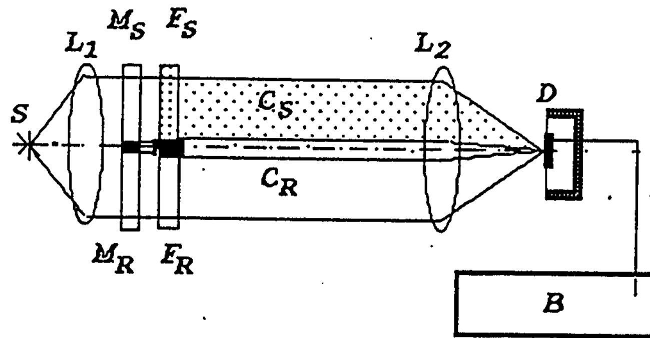

Figure 2. The basic circuit of the gauge, where: S - a source of light, L_1 and L_2 - lens, M_S and M_R - election-optical modulators, F_S and F_R - light filters, C_S and C_R - alarm and reference channels, accordingly, D - a photoreceiver and B - a block of processing and registration.

controllable gas in such a manner that, at excess of this value in air, the block submits a signal of an alarm.

Tests of a prototype of the indicator on the basis of the PbSe-photoresistor have shown:

- For "route" version with optical length 50 mm, the threshold of operation is not worse than 142 ppm for CO (or 8 permissible dose for a working zone).

- For the "local" indicator with length of an optical way 100 mm, the threshold of operation is not worse than 0,15 % of CO concentration in air.

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A Concept of Composite Diode and Thyristor Structures for Power Applications

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A semiconductor diode which can be used in power electrical circuits should combine in itself a high breakdown voltage V_b and a small voltage drop in forward direction at sufficiently large current density J_A. A conventional device which puts into effect both these requirements is a p^+nn^+- or p^+pn^+-diode consisting of two heavily doped p^+ and n^+ emitters which sustain high injection coefficients of their majority carriers at the current density J_A, and a slightly doped p- or n-base as shown in Fig. 1a. On the one hand, this base should be wide enough to provide the high breakdown voltage

$$V_b = E_b \, W \tag{1}$$

where W is the base width, and E_b is the breakdown electric field for a given material.

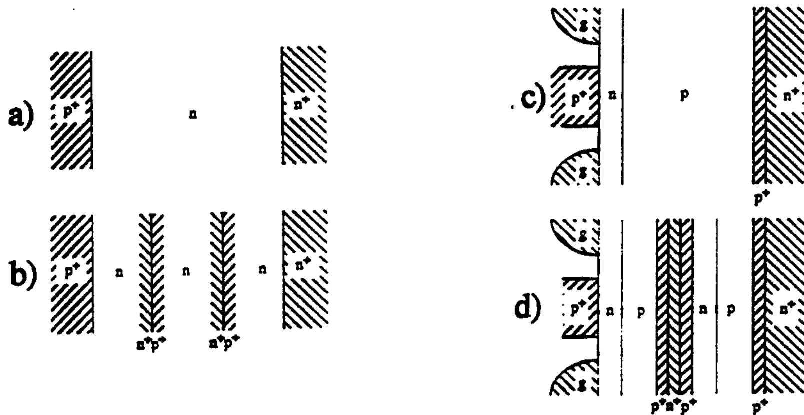

Fig. 1 Sketches of composite diode and thyristor structures

a) A conventional p^+nn^+ diode; b) A three-diode composite structure

c) A conventional gated power thyristor; d) A gated thyristor structure consisting of two thyristors connected in series

We assume the latter to be a fairly well determined value which is true if a region of strong electric field is sufficiently long. Equation (1) is valid for the base pinch-through regime with an approximately homogeneous distribution of the electric field, which is the most favorable at the given W.

On the other hand, being short enough, the base should provide a small forward voltage drop V across the diode. The IV characteristic of a short-base p^+in^+-diode is known to be as follows [1]:

$$J = J^{(1)}(V) = \frac{en_iW}{\tau_{eff}} exp\left(\frac{eV}{2kT}\right), \tag{2}$$

where n_i is the intrinsic carrier concentration in the base material, τ_{eff} is the effective lifetime of non-equilibrium carriers in the base at high injection level. According to the

Eq.(2), the current density J is directly proportional to W and inversely proportional to τ_{eff}, however this is true while Eq.(2) is valid itself. We assume the following inequality to be a criterion of this validity:

$$W < \sqrt{D_a \tau_{eff}} = L_{eff}, \tag{3}$$

where D_a is the ambipolar diffusion coefficient in the base. Equation (3), in particular, results in the fact that the maximum value of the forward current through the diode does not exceed

$$J(V) < J_{max}(V) = en_i \sqrt{\frac{D_a}{\tau_{eff}}} exp\left(\frac{eV}{2kT}\right), \tag{4}$$

while the breakdown voltage

$$V_b \leq E_b L_{eff} \tag{5}$$

for the best forward current. An increase in the base width W beyond the limits defined by Eq.(3) obviously leads to a growth of V_b. However, in this case we obtain a strong increase in the forward voltage drop because of a transition from the recombination limitation of the diode current and the recombination mechanism of thermal losses to the ohmic limitation of the current and, consequently, to local Jouhl's heating of the base. This results in an activation of temperature effects and electron-hole scattering which leads to the further increase in the forward voltage drop. Actually, these are the effects which restrict the value of permissible forward current.

Note, that the value of τ_{eff} in Eqs.(2-5) is not a constant and decreases as J grows because nonlinear radiative and Auger recombination mechanisms become substantial. Therefore, the optimum value of the base width depends on the desired value of J.

The conditions defined by Eq.(3) and Eq.(5) produce certain difficulties for the design of power diodes and, in general, other devices. For instance, such materials as $GaAs$, GaP, and, especially, SiC possess much more values of E_b than Si. For SiC, this advantage can reach $10 - 20$ times [2]. However, the value of L_{eff} in $GaAs$ and GaP does not exceed a few microns and a few tenth of micron in SiC [3], while it is $100 - 500$ μm in Si. Therefore, they have no chances (for the Si temperature range!) to replace silicon in the fabrication of high-voltage devices with a small forward voltage drop.

Below, we suggest a way to overcome the restrictions described by Eqs.(3) and (5). The diode base with the length of W is supposed to be divided by m layers with the length of $W_m = W/m$, the doping of each layer being the same. The number m has to be chosen so that the condition

$$W_m < L_{eff} \tag{6}$$

is met for a chosen value of the optimum current density and, consequently, τ_{eff}. Meanwhile, the total length W should sustain a chosen value of V_b which is limited by the condition $mE_bL_{eff} \geq V_b = E_bW > E_bL_{eff}$.

The layers of the base are separated with thin n^+p^+-junctions so that the entire structure becomes as depicted in Fig.1b. The adjacent p^+nn^+ or p^+pn^+ diodes must

be grown layer by layer forming a united series structure. The contemporary epitaxial technology with application of modulation doping makes it possible.

In the simplest case, thin tunnel junctions with as high as possible tunnel conductivity must be obtained on the boundaries between the bases. This means that both the donor concentration in the n^+-layer and the acceptor concentration in the p^+-layer should be utmostly high, and the junction itself - utmostly abrupt. Such junctions are known to be successfully grown for $GaAs$, InP, GaP [4]. However, we have no such information on SiC, GaN, InN, *etc.*

It is possible to increase the conductivity of the n^+p^+-junction in wide band gap materials by means of growing a narrow band gap insertion in the central part of the junction. The band gap of this insertion must have smooth boundaries to ensure the band structure for an optimum working current to be as depicted in Fig.2.

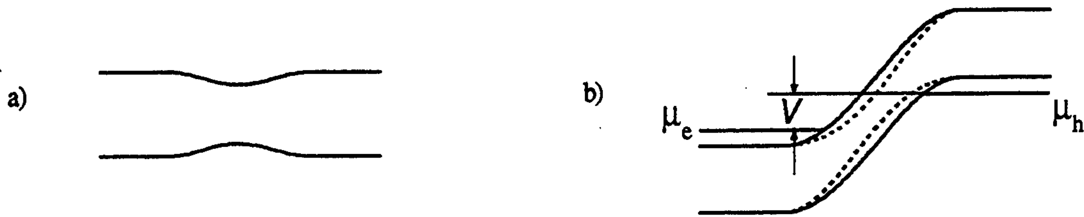

Fig. 2. a) - desired band structure of the n^+p^+-junction (Electric field is assumed to be zero);
b) - band structure for a conventional reverse biased tunnel n^+p^+-junction (solid line) and for a junction with the narrow band gap insertion (dashed line).

The narrower the band gap of the insertion is, the higher its tunnel conductivity is. Such pseudomorphic structure could be easily obtained in $InAs$ (insertion)/$InGaAs$ (cladding layers)/$GaAs$ (basic diodes). However, the fabrication of such structures for GaN and, especially, for SiC needs further investigations and efforts.

In the current range where the value of τ_{eff} provides for Eq.6 to be fulfilled the IV-characteristics of the structure is given by the formula:

$$J = J^{(m)}(V) = \frac{en_iW_n}{\tau_{eff}} exp\left(\frac{eV}{2mkT}\right) , \qquad (7)$$

which is Eq.(2) rewritten for a separate layer with taking into account that the voltage drop across each layer is equal to V/n. Obviously, the current $J^{(n)}(V)$ is substantially smaller than $J^{(1)}(V)$, i.e. if both Eq.(2) and Eq.(7) are valid, the suggested procedure makes no sense.

However, the situation changes dramatically for the following case. Let us assume that the required value of V_b is large enough so that Eq.(3) is met for neither value of J and the condition $W \gg L_{eff}$ is fulfilled instead of Eq.(3). Then, we can find the minimum value of m, which Eq.(6) is met for, and specify the minimum value of current $J^{(m)}_{min}$, starting from which the current defined by Eq.(8) is larger than that in the conventional diode. Usually, this minimum current is not large and corresponds to the threshold of high injection levels for the diode with the base width of W. So for real current densities of above $10^3 A/cm^2$ the decrease in voltage drop can be up to $4 \div 5$ times for $W \simeq (10 \div 15 L_{eff})$.

To verify our approach we have performed numerical simulations of the SiC com-

posite structure using the advanced device simulator "SILVACO"[5] which solves the drif-diffusion set of equations together with the Poisson's equation. The results of the simulation for a SiC structure with $V_b \simeq 6kV$ are shown in Fig.3. The material parameters necessary for the simulations were taken from [6].

As it is seen, the three-diode composite structure exhibits the best performance and allows us to substantially decrease the forward voltage drop across the structure.

The IV-characteristics for reverse biased structure are depicted in Fig.4. As we predicted, the breakdown voltage of the composite structure remained the same.

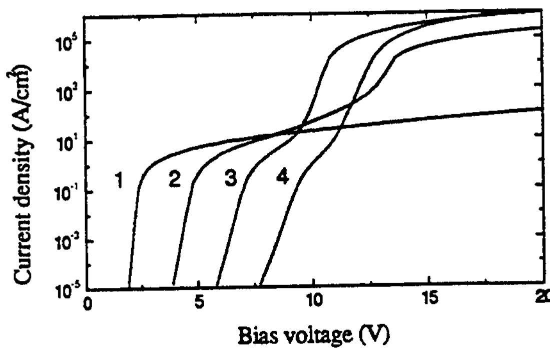

Fig.3 Forward current-voltage characteristics of SiC diodes for a conventional diode with the base width of 40 μm (1) and for two-, three-, and four-diode composite structures with the base widths of 20 μm (2), 13.3 μm (3), and 10 μm (4), respectively.

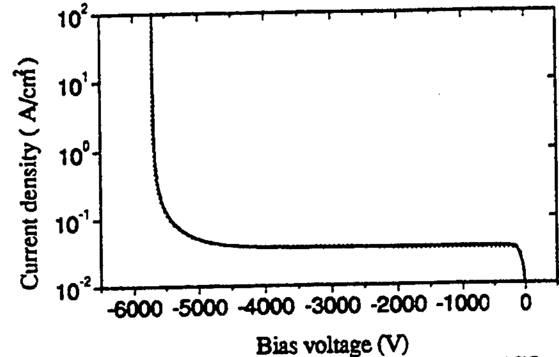

Fig.4 Reverse current-voltage characteristics for a conventional SiC diode with the base width of 40 μm (solid line) and for a two-diode composite structure with the base widths of 20 μm (dotted line)

Our approach can be applied for a power thyristor depicted in Fig.1c. However, it is necessary to stress that in this case it possesses not only quantitative but also qualitative advantages. A wide, slightly doped controlled base of a power thyristor cannot exceed some critical value defined by the condition for the open state of a thyristor:

$$\frac{1}{cosh\frac{W_1}{L_{eff}}} + \frac{1}{cosh\frac{W_2}{L_{eff}}} > 1 \qquad (8)$$

where W_1 and W_2 are the widths of the thyristor bases [7]. Therefore, there is a top limit value of the breakover voltage which could be applied to a conventional thyristor in its forward blocking state. While the composite structure depicted on Fig.1d allows us to reach much larger values of the breakover voltage because the controlled base of each thyristor in the structure is thinner.

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High Bandwidth-Efficiency GaAs Schottky Photodiodes for 840 nm Operation Wavelength

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I. INTRODUCTION

The bandwidth capabilities of optical-fiber telecommunication systems are still not fulfilled with present performance of optoelectronic devices, and high speed photodetectors have been an active research area for the past two decades [1]. It has been shown that a Schottky photodiode, with 3-dB operating bandwidth exceeding 200 GHz, is one of the best candidates for high-speed photodetection [2]-[5]. However, like p-i-n photodiode, Schottky photodiode also suffers from bandwidth-efficiency trade-off. A recent family of photodetectors, resonant cavity enhanced (RCE), has the potential to overcome this trade-off as compared to conventional photodetectors [6]-[12]. The RCE detector operation is principally the same as the conventional one, with the main difference being an increased internal optical field by virtue of a Fabry-Perot resonant cavity. The higher field enables high efficiencies with thinner absorbing layers, resulting in high quantum efficiency with low photo-carrier transit times. The Schottky photodiode has its advantages in its simplicity, compatibility with monolithic integration processes and use of thin Schottky metal as the top mirror of the resonant cavity. However, high-speed RCE photodetector research has mainly concentrated on p-i-n type photodiodes, where near 100% quantum efficiencies along with a 3-dB bandwidth of 17 GHz have been reported [13]. There are only a few reports on RCE Schottky photodiodes [14]-[15]. We briefly report our work on design, fabrication, and testing of high- speed RCE Schottky photodiodes for operation at 840 nm.

II. DESIGN AND FABRICATION

We have fabricated two different structures, S1 and S2, which are optimized for top illumination. The details of the epitaxial structures are given in the Tables 1 and 2. The bottom Bragg mirrors are consist of quarter-wave stacks ($Al_{0.20}Ga_{0.80}As/AlAs$) designed for high reflectivity at 840 nm center wavelength.

Material	Doping (cm^{-3})	Thickness (nm)
$Al_{0.15}Ga_{0.85}As$	10^{17}	80
$Al_{0.15}Ga_{0.85}As$ to GaAs	10^{17}	30
GaAs	10^{17}	120
GaAs to $Al_{0.20}Ga_{0.80}As$	10^{17}	30
$Al_{0.20}Ga_{0.80}As$	10^{17}	160
$Al_{0.20}Ga_{0.80}As$	n^+	400
$Al_{0.20}Ga_{0.80}As$	undoped	230
Bragg Mirror (18.5 pairs)		
S.I. GaAs		

Table 1: Structure of sample S1

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Material	Doping (cm^{-3})	Thickness (nm)
GaAs	10^{17}	350
GaAs to $Al_{0.20}Ga_{0.80}As$	10^{18}	50
$Al_{0.20}Ga_{0.80}As$	$n^+=10^{18}$	500
$Al_{0.20}Ga_{0.80}As$	undoped	260
Bragg Mirror (14.5 pairs)		
S.I. GaAs		

Table 2: Structure of sample S2

Both structures were grown by solid-source MBE on semi-insulating (SI) buffered GaAs substrates. Both samples have low carrier trapping due to graded interfaces of the absorbing layer. The thicker cap layer of sample S2 has the advantage of wavelength tuning by etching the top layer. Prior to the fabrication process, sample S2 was wavelength tuned, according to its reflection spectrum (see Figure 1). About 40 nm recess etch of the top layer resulted in approximately 30 nm shift in resonance wavelength.

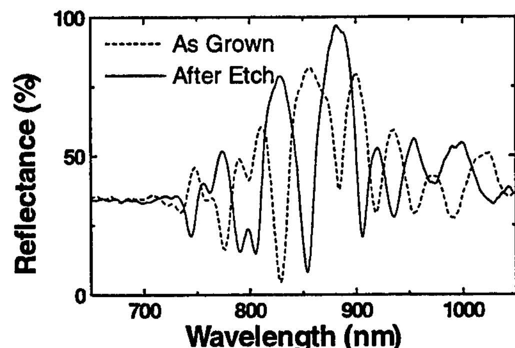

Figure 1: Reflectance tuning by wet etching, for sample S2.

The samples were fabricated using a microwave-compatible monolithic micro-fabrication process. Figure 2 shows the schematics of the fabricated devices. Fabrication started with formation of ohmic contacts to n^+ layers, followed by a recess etch through the top layers (approximately 0.6 μm), a self aligned Ge-Au-Ni-Au lift-off, and a rapid thermal anneal.

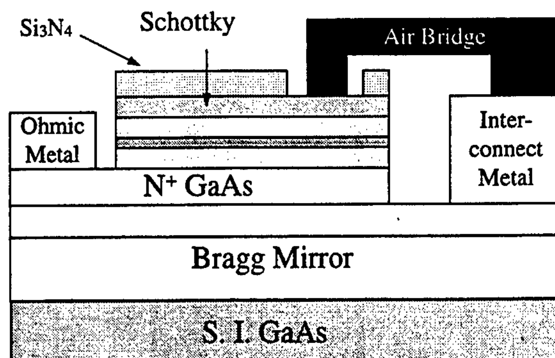

Figure 2: Schematic cross-section of a fabricated Schottky RCE photodiode.

Mesa isolation was achieved by etching away all the epilayers except active areas. Then Ti-Au interconnect metallization, which formed coplanar waveguide (CPW) transmission lines, was defined by lift-off. A thin (10 nm) Au Schottky contact was deposited, followed by a 210 nm thick silicon nitride layer. This silicon nitride besides protecting the surfaces also served as a dielectric for bias capacitors. Finally a thick (~1.0 μm) Ti-Au layer was deposited to form an air bridge connection between the center conductor of CPW and the Schottky metal [15].

III. MEASUREMENTS

Photoresponse measurements were carried out in the 700-900 nm wavelength range, by using a tungsten-halogen projection lamp as the light source and a single pass monochromator. Output of the monochromator was coupled to a multimode fiber. The monochromatic light was delivered to the devices by a light-wave fiber probe, and the electrical characterization was carried out on a probe station. The incident power spectrum was measured by a calibrated optical powermeter.

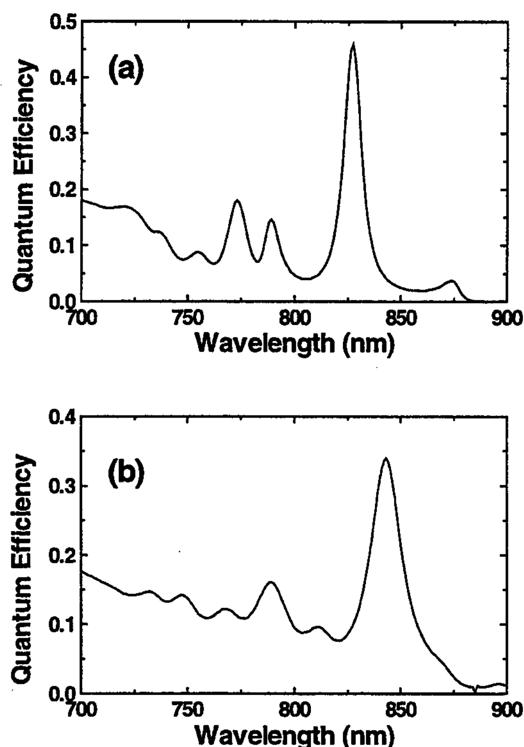

Figure 3: Photoresponse of samples (a) S1 and (b) S2.

For the spectral measurement large area photodiodes were chosen (60x60 to 400x400 μm^2) to ensure all of the optical power is incident on the active area. Silicon nitride layers on top of each sample were separately etched in small steps, by using HF:DI Water (1:1600) solution, in order to obtain maximum quantum efficiency. The peak wavelength shift was very small (less than 1 nm) whereas peak efficiency varied by about 10%. The maximum quantum efficiencies for samples S1 and S2, were obtained at silicon nitride thicknesses of 150 and 130 nm, respectively. Photoresponses of the devices, after silicon nitride layers were etched down to optimum thicknesses, are given in Figure 3. Sample S1 has a higher quantum efficiency (46% at 827 nm), as compared to that (34% at 843 nm) of the sample S2.

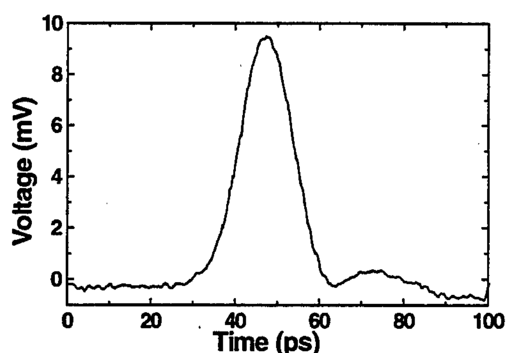

Figure 4: Pulse response of sample S2.

When compared to single pass structures, approximate enhancement factors are 15 and 6 for S1 and S2, respectively. The higher off-resonance photoresponse (hence lower enhancement) of device S2 is a result of thicker absorption layer as compared to S1. The full-width at half maximum (FWHM) is 10 nm for S1, and 9.5 nm for S2. These data were taken without any bias. A -1.5 V bias increased the efficiencies about 3% for both devices. However, at around –2 V the quantum efficiencies started to increase drastically. We believe that this increase is caused by an internal gain mechanism, mainly the beginning of an avalanche breakdown.

High-speed measurements were made with 1 ps FWHM optical pulses obtained from a Ti-Sapphire laser operating at 840 nm. Figure 4 shows the temporal response of a small area photodiode (from sample S2) measured by a 50 GHz sampling scope. The measured photodiode output has a 14 ps FWHM, and a fall time of 9.5 ps. The Fourier transform of the data has a 3-dB bandwidth of 35 GHz. However, since the rise time is very close to the fall time, we conclude that the measurement was limited by the experimental setup.

IV. CONCLUSIONS

Two different RCE Schottky photodiode structures for ~840 nm operation have been demonstrated. Structure S1 had 10 nm FWHM with an enhancement of a factor of 15, whereas structure S2 had 9.5 nm FWHM with an enhancement factor of 6. The temporal response of S2 (which was limited by the experimental set up) was 14 ps, which corresponds to a 3-dB bandwidth of 35 GHz. To our knowledge, our results correspond to the fastest RCE photodetectors in 800-850 nm wavelength region published in scientific literature.

ACKNOWLEDGMENTS

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Real space transfer in δ-doped MQW system: a universal mechanism of far and mid IR lasing

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I. Introduction

Existing intraband semiconductor lasers - i.e. p-Ge hot hole FIR lasers [1] and quantum cascade lasers [2] have their own drawbacks. Hot hole lasers work in the broad region of FIR (30 - 120 cm^{-1}); but they are helium cooled pulsed devices (though works to get cw p-Ge lasers are under way [3]). Quantum cascade lasers are IR sources which stop operate at wavelengh longer than around 10 mkm. So, there is a great need to find out a mechanizm which can provide lasing in wide IR region and to develope a simple semiconductor lasers which could fill frequency band from far to mid IR regions.

In the process of investigation of high electric field lateral transport and real space transfer in selectively doped p-type InGaAs-GaAs we came accross [4,5] seems a universal population inversion mechanizm (which could be realised not only in the structures and the conditions studied) which could serve this goal. It is based on lower heating by lateral electric field of the higher laying low mobility level (states) and could be used in quite broad type of the MQW systems

And in the present report we present general consideration of a possibility of population inversion and stimulated IR emission under RST (including the case of a mixture of RST and intervalley transfer in structures similar to the ones for which the population inversion there recently observed [6]) and give results of the detailed investigations of current-voltage and spontaneous FIR and MIR emissions - voltage characteristics of hot holes in p-type selectively δ-doped InGaAs-GaAs MQW systems under RST. Also data on the hot hole photoluminecence and results on observation of absorption of the FIR radiation in the MQW structures under RST by using intracavity spectroscopy basing on p-Ge laser (which seems gives a prove for FIR radiation amplification in the "shallow" sample studied) are given.

II. Population inversion under Real Space Transfer

Population iversion is higher population (higher occupation number)of the upper states appropriate for specific transitions. Let us discuss first a simplified model: there are two coupled QW: one lays higher in the energy and has high effective mass while another situated lower in energy and has lower effective mass. The barrier between the well is not so thick so that there is overlapping of the corresponding wavefunctions and interwell exchange by scattering processes (and also optical transitions between states in the wells) are posible. Suppose also that the upper well is selectively doped so that mobility in the upper well is substantially lower than that in the lower well (due to both higher mass and the doping) and that there is only one (important for consideration of RST) level in each wells.

Conisder now heating in the wells by lateral electric field E. Carriers being at $E = 0$ in the lower well at high fields reach energy higher than the well separation Δ and RST from the lower well to the upper well should take place. There can be two different situations depending on strengh of the well coupling: the case of weak interwell coupling and the case of strong coupling. In the former the intrawell heating and relaxation is more important than the exchange between the wells so that carrier distributions (electronic temperatures) in the wells can be determined indepenenly of each other; while in the latter case the exchange determines also distribution function (in the lower) well. We will suppose for simplicity that the exchange is elastic with constant exchange potential so that exchange rate is constant due to constant density of states in the wells with only one levels involved.

In the case of low exchange rate one can use approximativly the Maxwellian distribution in the wells with different temperatures T_u and T_l correspodingly with different total concentrations N_u and N_l in the wells. The temperatures in the wells are determined by the intrawell heating and scattering processes (consideration of which we avoid here) while the concentrations should be found from balance of the exchange rates and one can get the following expression for the ratio p of the occupation numbers at the bottoms of the wells:

$$p = \frac{n_u}{n_l} = \left(\frac{T_l}{T_u}\right) \exp -\Delta/T_l$$

We see that at $T_l \simeq \Delta$ and $T_l \gg T_u$ there is population inversion ($p > 1$) between the higher laying and the lower wells. In other words, *just easier heating in the lower well providing higher electronic temperature here (which should be easy achieved due to higher mass in the upper well and its selectively dopping) provide the population inversion.* This is a quite general situation.

In the case of well-barrier RST in a similar way one get the folowing estimate of ratio of the occupation numbers at the bottoms of the barrier and the well:

$$q = \frac{n_b}{n_w} \simeq \left(\frac{T_w}{T_b}\right)^{3/2} \exp -\Delta/T_w$$

Here T_b is electronic temperature in the barrier above the well. We see that once again for $T_w \simeq \Delta, T_w \gg T_b$ there is population inversion ($q > 1$) between the barrier and the well. In the case of exchange dominated situation similar considerations may be made which we will not discuss here.

RST had been apperared in 70s [7] as a spartial analog of the Hot Electron Intervalley Transfer (IVT) - phenomena responsible for the Gunn effect. And though a possibility of population inversion under IVT (Γ valley population inversion) is long known [8] eventially none has discussed the implementation of this inversion in lasing. Also none mentioned that eventially there is substantially higher population inversion (as simulations demonstrate - see e.g. [9]) between higher (L and X) valleys and the lower Γ valley (Γ valley population inversion is eventially an "imprinting" of this inversion). Though in the bulk X, L - Γ optical transitions are forbidden they could become allowed in MQW structures where X, L - Γ mixture occur (e.g. the one with QWs similar to whose where recently population inversion under optical exitatiom has been observed [6]). In any case this situation (mixture of RST and IVT in δ-doped MQW structures) looks quite perspective for IR lasing and should be elaborated and studied in details.

III. The MQW system studied and observation technique used

Transport, IR emission and absorption and photoluminecence observations under RST were performed in this work on selectively (δ) doped p-type strained $In_xGa_{1-x}As$-GaAs MQW systems with different composition x and width d of the wells corresponding to different number and position of the bound states in the wells and their separation from the continuum states and δ-doping of the barriers and also on multipy δ-doped GaAs samples (with the same as in the MQW system δ layers) which serve as reference for transport, emission and absorption mesurements. The $In_xG_{1-x}As$ MQW samples with $0.03 \leq x \leq 0.2$, InGaAs layer thickness $d = 50 - 100A^0$ and GaAs layers of $600A^0$ and number of QW n = 20 were grown by MOCVD technique on GaAs(001) substrates. Two δ-layers of C were introduced at $50A^0$ from both sides of each InGaAs QW in GaAs barrier layers. For the reference samples without QW's only 20 δ layers of C there introduced in GaAs matrix. Typical values of 2D hole concentration N_s and mobility μ were: $N_s \approx (1-3) \times 10^{11} cm_{-2}$ $\mu_{77K} \approx \mu_{4.2K} \approx 3000$ cm2/VЧs. The lateral pulsed electric field 3-10 μs in duration was applied to the structure via strip electric contacts deposited on the sample surface at the distance 3-4 mm. Spontaneous emission of hot holes was studied in the sensitivity bands of FIR photodetector Ge:Ga with teflon filter (λ ≈ 50-120 μm) and of MIR photodetector Si:B .(λ ≈ 20-28 μm) which were placed nearby the sample in the liquid helium. For absorption mesurement the structures were put inside resonator of a p-Ge FIR hot hole laser and the laser power dependence versus electric field applied to the MQW structure were measured for the case the p-Ge laser is set at nearby threshold conditions (to provive stronge influence of the the MQW structure on the laser power). Photolumenecece was exited by Ar gas laser and its spectra were studied during electric field pulse applied to the MQWs.

Fig.1 represents the calculated energy of 2D holes E(k) verus in-plane hole wavenumber k in QWs in In0.18Ga0.82As layers and schemes of the barrier-well valence band at k=0 (with δ layers included) perpendicular to the layers for the samples 1845, 1850 discussed in this report. For 1845 sample (x=0.1, $d = 77A^0$ the barrier-well valence band offset is 39 meV (higher than an optical phonon energy $\hbar\omega_0 = 37$ meV) and there are two hole subbands in QW; they all descend from the heavy hole subband. We call this sample *"deep"*. The strain-induced splitting results in the essential decreasing of in-plane hole mass: at the bottom of the lowest subband hole mass $m_{hh1} \approx 0.1m0$ (cf. [10]) while in unstressed

bulk material $m_{hh} \approx 0.5m0$. Such high barrier mass as campared with that of the well substantially easies process of RST in this system. Separation of the hole subbands hh1 and hh2 in QWs in this sample at k = 0 is 20 meV and intrawell FIR emission with quantum energy $\hbar\omega = 10 - 25meV$ may be observed at $hh_2 \rightarrow hh_1$ transitions while MIR emission ($\hbar\omega = 44 - 62$ meV) may arise only from transitions between barrier and QW states. The bottom of the lowerest (hh_1) hole subband is 30 meV below the barrier i.e. *deeper* than energy of carbon impurities in the barrer (25 meV). As a result at equilibrium (at zero electric field E) all holes should be in the wells (as shown in the Fig1a) and appeared in barriers only at high enogh E due to carrier heating in the wells.

For 1850 sample (x=0.1, $d = 48A^0$) the band offset is 25 meV - below an optical phonon energy and there is only one hole level in the well with its bottom at 20 meV from the barrier - i.e. *shallower* than the carbon impurities in the barriers (*"shallow" sample*). As a result at equilibrium (E = 0) holes should be bound to impurities in the barrier and appear in the wells only at high enough electric field after the impurity breakdown. These consideraton are supported by the observation data presented below.

IV. Observation results and discusion

Current-voltage and emission-voltage characteristics of the "deep" 1845 and "shallow" 1850 samples at 4.2K are presented in Fig.2. For "deep" 1845 sample current begins at lowest fields appllied and there is pronounced increase in the hole mobility (in the slope of the curve) in the moderate electric fields, which seems to result from the dominant role of the ionized impurity scattering in the low field hole mobility. The nonlinear (saturated) part of I-V curve corresponds to the remarkable features (nonmonntonious behaviur) in emission-voltage characteristics both in FIR and MIR ranges. Both the current saturation (which in other samples provides also current instability) and the nonmonotonous dependences of the emission intensities on the electric fields may be naturally explained by RST. Under RST in this sample heated holes under RST are trapped in the wells of the barriers produced by δ doping. Since the hole mobility in barriers is much less than in QWs RST should result in the saturation of I-V characteristic or even in the N-type negative differential conductivity. At the same time the trapping reducing the number of holes in QWs should slow down the emission intensity increase (which in this sample seems is due to the intrawell hole heating) with the field and even result in the drop of the emission intensity just as shown in Fig.2a. In this sample intrawell FIR emission ($\hbar\omega$ = 10-25 meV) may be observed at hh2rhh1 transitions while MIR emission ($\hbar\omega$ = 44-62 meV) may arise only from transitions between barrier and QW states. The maximum of the emission intensity is reached just at the "break" of I-V curve. The following increase of the field results in the drastic fall of the emission intensity due to substantial fall in number of holes in the wells confirming the existence of RST.

Fig.2b represents the current-voltage and emission-voltage characteristics for the "shallow" sample 1850. It is characterized by the same value x = 0.1 but the QWs are narrower. As a result the second hole subband hh2 at k = 0 is situated just at the edge of QW (cf. Fig 1) and the first hole subband hh1 is lifted over the bottom of well. On the other hand the binding energy of carbon acceptor in GaAs is known to be just the same 26 meV. Therefore at liquid helium temperature the holes may be frozen out at the impurities. The freezing is responsible for the

flat part of the plots in Fig.2b up to the threshold electric field $E \simeq 0.5$ kV/cm. The steep rise of the emission at E ¿ 0.5 kV/cm seems to result from RST from δ-layers in the barriers into QWs while the subsequent drop in the emissions are seems due to hole returning back to the barriers. To verify this conclusion the test δ-doped GaAs samples without QWs were grown and investigated. In test samples the threshold electric field was substantially higher - $E \simeq 1.3$ kV/cm than in the sample 1850 and FIR emission intensity was more than ten times weaker (at the same levels of current density). The latter also proves that the emission observed in 1845 and 1850 samples are associated with the transitions to the hole states in QWs rather than between the hole states in the barriers.

Fig 3,4 present data on photoluminecence for similar "deep" (Fig 3) and "shallow" (Fig 4) samples. We see that in the "deep" sample drop in the luminecence intensity is started just at the begining of current saturation demonstrating beging of RST. On the other hand in the "shallow" sample (Fig 4) there is drastic decrease in the phtoluminecence intensity just at the carbon impuriry breakdown and appearence of current also demonstrating appearance of RST. At the same time in this sample first (below the breakdown) there is an increase in the peak energy of the photoluminecence (which is due to photoelectron heating by electric field). After the breakdown there is a decrease in the peak energy of the luminecence which we attribute to cooling down the hole in the wells due to interaction of the heated holes with optical phonons.

It seems likely that the data and discussions given provide clear ehough picture of the procecces of the hole heating, RST and emissions in the systems (though all the details of the proceeces involved surely are a subject for further considerations and calculations). In particular for the 1850 and similar "shallow" samples studied situation is very close to the one needed to provide population inversion and FIR amplification discussed in Section 2.

To study this possibility we use a version of itracavity laser spectroscopy by putting the structures inside a resonator of a p-Ge FIR hot hole laser [1]. The "shallow" or "deep" samples and reference test structure without QWs with δ-layers only were put flat at the top of the p-Ge laser rod with teflon spacer. The electric and magnetic fields in the laser were arranged in the range inside the emission region nearby its boundary to provide substantial influence of the structures on the laser emission power. The laser was in the broad emission mode with central wavelengh $\lambda_l \simeq 100\mu$m ($\hbar\omega \simeq$10 meV) and the wavelengh spread $\Delta\lambda/\lambda \simeq 0.1$.

Fig 5 gives the laser power dependence on the voltage applied to the two "shallow" MWS structures. We see that there is an increase in the laser power (i.e. *bleaching*) in the fields higher than the impuriry breakdown threshold whereas for the "deep" samples and the δ-layers there is a decrease in the power. In some "shallow" samples the bleaching is drastic and results in saturation of a detector used to monitor the p-Ge laser power (like in the sample 1945 in Fig 5); or there can be nonmonotonous behaviour of the bleaching versus electric field (like in sample 1947 in Fig 5) which we attribute to cooling of the holes in the well due to interaction of the heated hole with optical phonons as discussed above in the case of photoluminecence above. Though one can not fully exclude that the bleaching is due to decrease in the some absorption in the MQW structure the facts that it starts after the carbon impurity breakdown threshold and that there is no bleaching in the "deep" structures and in the test δ-doped structure

after the breakdown threshold and because the inversion fits overall pecture of RST give strong evidence that amplificaton of the laser radiation in the "shallow" structures occurs. Polirization of the laser radiation in this experiment is along the structure layers. For this polirization optical transitions are forbiden at k = 0 in the QWs; however they become allowed at $k \neq 0$ where transitions due to the laser radiaton occur.

V. Conclusion

We put forward and present conditions for new population inversion mechanism based on RST in δ-doped MQW systems which seems could be fiasible not only in the MQW structure studied but in quite differend MQW structures and situations. We investigate transport, RST and FIR and MIR emission in several p-type InGaAs-GaAs MQWs structures and test GaAs p-type multiple δ-doped structures and demonstrate that FIR and MIR emissions are a good indicator (diagnostic) of RST. Basing on a version of laser intracavity spectroscopy we observe increase of FIR radiation (bleaching) in the "shallow" MQW structure under RST, which seems to be due to the inversion and amplification mechanism proposed. And our group is now in a possition to disign appropriate lasing system (which we believe should consists of just some cavity etched in the substrate below the appropriate "shallow" MQW structures) and we will report on the attempt to achieve lasing in such a system at the Conference.

VI. Acknowledgment

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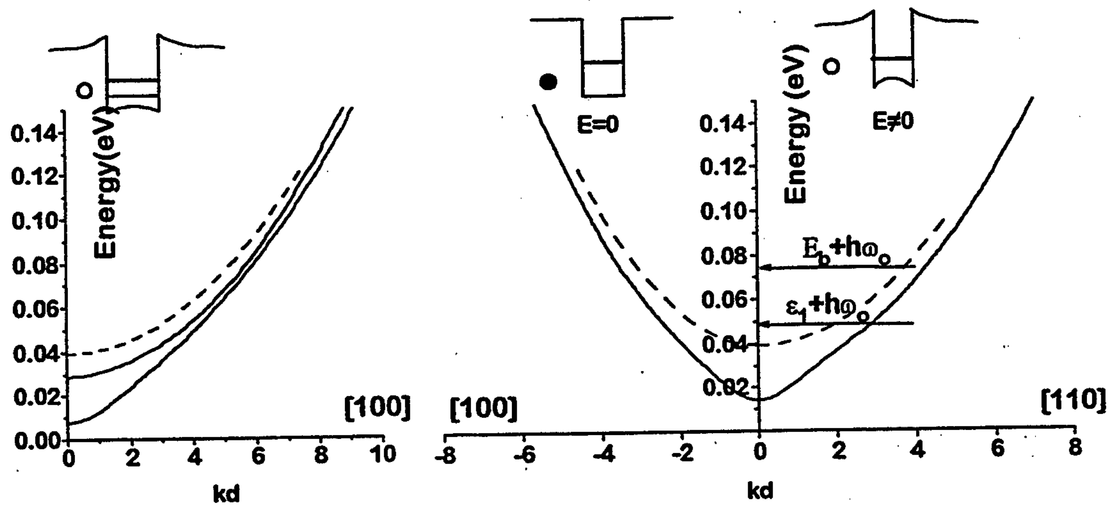


Figure 1: Calculated energies of holes in InGaAs-GaAs QWs with barrier energy shown (dotted lines) and schemes of valence band profiles at zero and nonzero electric fields; left: sample 1845 (x=0.1, d= 77 Å); right: sample 1850 (x=0.1, d = 48 Å).

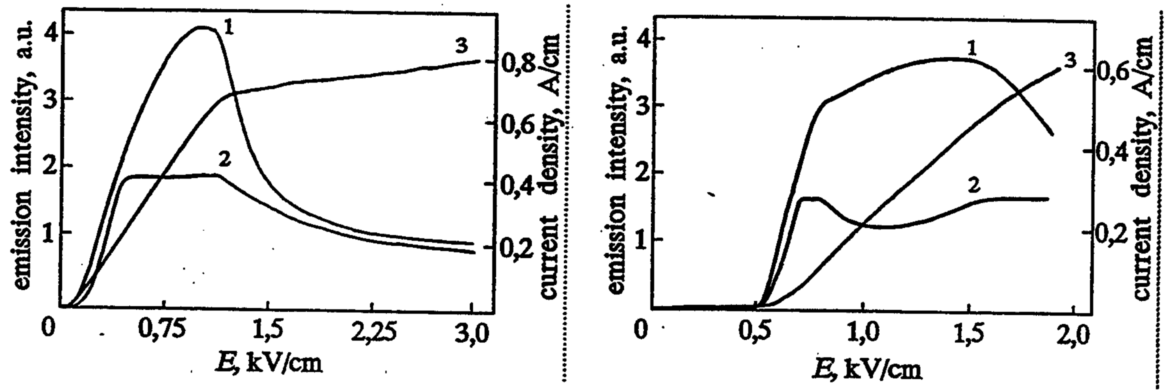


Figure 2: Emission (1,2) and current-voltage characteristics of: left - 1845 sample; right 1850 sample

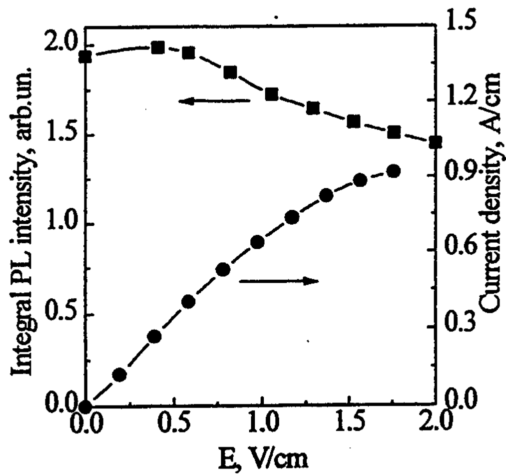


Fig.3 Integral PL intensity (■) and current density (●) versus lateral electric field for 8 nm $In_{0.2}Ga_{0.8}As/GaAs$ quantum wells heterostructurest, T=4.2K.

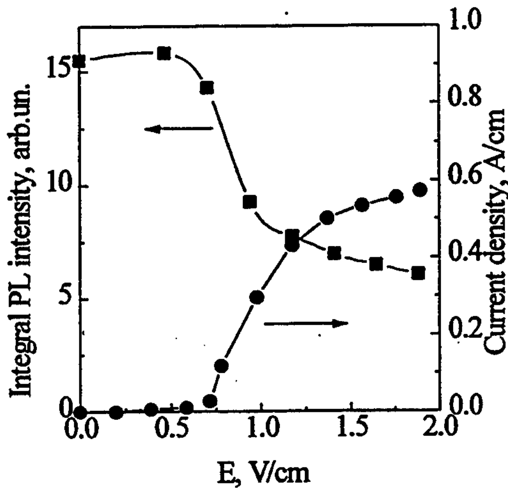


Fig.4a. Integral PL intensity (■) and current density (●) versus lateral electric field for 5 nm $In_{0.1}Ga_{0.9}As/GaAs$ quantum wells heterostructures, T=4.2K.

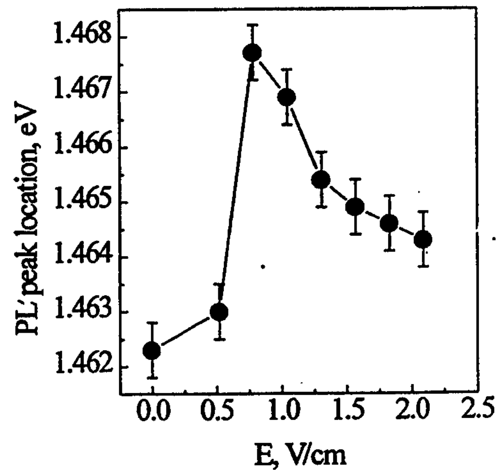
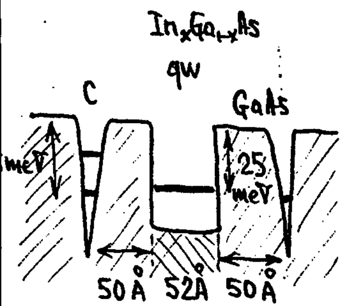
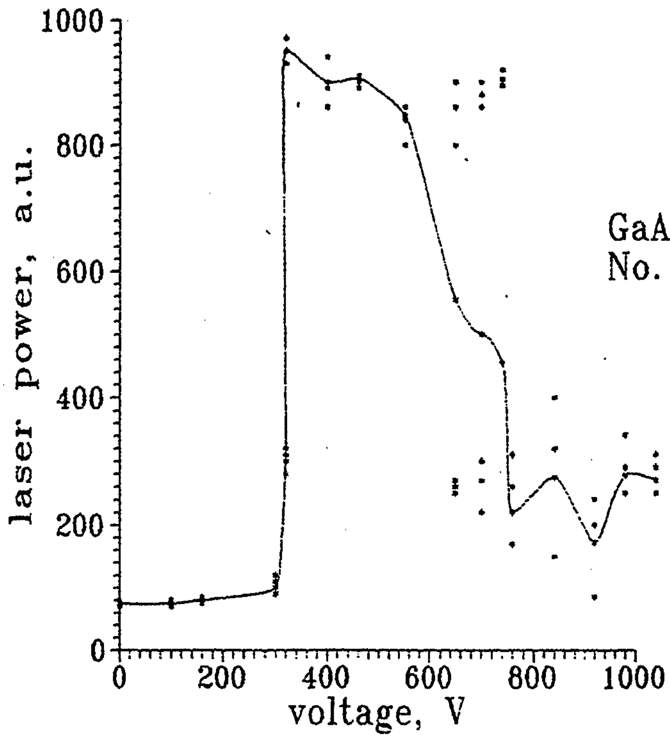
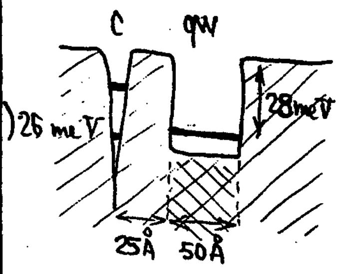


Fig.4b. PL peak location versus lateral electric field for 5 nm $In_{0.1}Ga_{0.9}As/GaAs$ quantum wells heterostructures, T=4.2K.







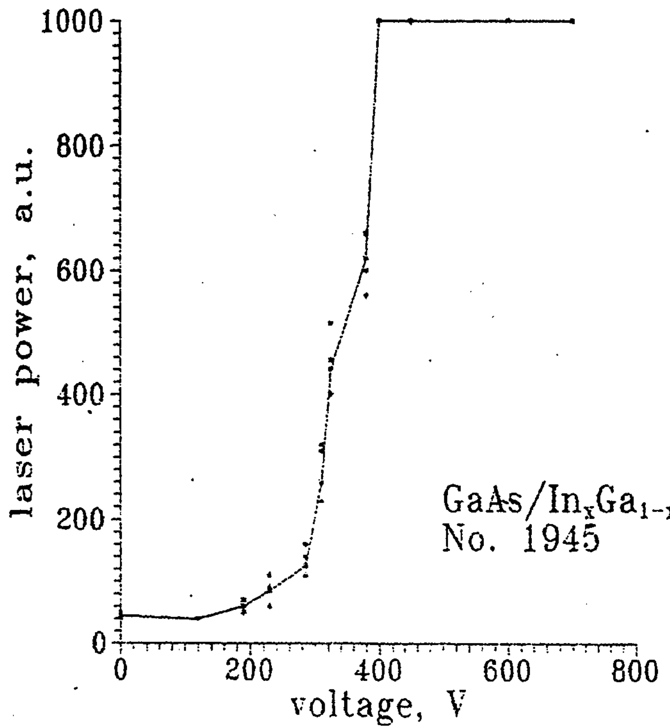


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Fig 5. Laser power dependence on the voltage applied to the two "shallow" structures.

Semiconductor Optical Modulator, Based on Strong Linear Quantum Confined Stark Effect, for Ultra-High-Speed Applications

Michael Feiginov, Vladimir Volkov

Abstract— **We propose design and analyze the properties of the semiconductor optical modulators based on asymmetric two-layer QWs with a heterojunction of the second type between the layers of the QW. This QW is characterized by the strong linear quantum confined Stark effect, substantiated by the essential spatial separation of the photogenerated electrons and holes. We have developed a simple analytical model of the optical modulators. For illustration we have calculated the extinction ratio of 1.55μm electroabsorption waveguide MQW modulator of this type. On the grounds of the experimental data on the exciton absorption, we predict that the driving voltage of 1 Volt is sufficient for extinction ratio of the modulator at room temperature to be of more than 17 dB, with the internal capacity of the modulator p-i-n junction is of only 50fF. The structures of the type are highly promising to be used in both electroabsorption and phase modulators for ultra-high-speed applications.**

Keywords— **Optoelectronics, optical modulators, quantum well, linear quantum confined Stark effect.**

I. Introduction

The electroabsorption (EA) and phase semiconductor optical modulators based on quantum well (QW) structures are very promising for application in the ultra-high-speed fibre-optic transmission systems. The electric circuitry supplying the driving voltage to the modulator imposes more and more tough requirements on the modulator when we move to 40Gb/s and higher, namely, the low driving voltage and low capacity of the modulator, with the extinction ratio, if we consider EA modulator, being sufficiently high. To meet all these requirements we need to design the active region of the modulator so that its optical properties are very sensitive to the electric field. Then we can diminish the driving voltage and/or increase the thickness of the undoped layer of p-i-n structure, that leads to the diminishment of the internal modulator capacity.

The majority of the contemporary semiconductor modulators use the multiple QW (MQW) structures based on the symmetric wells as an active region [1]-[6]. But the symmetric QWs are characterized by the quadratic QCSE (quantum confined Stark effect) only. Here we propose touse MQW active region based on asymmetric QWs. The asymmetric QWs are characterized by the linear QCSE. In the region of small driving electric fields the linear QCSE wins over quadratic one. So, the structures based on the asymmetric QWs are preferable from the point of view of sensitivity to the small electric fields. There are several papers ([7] -[9]) where the semiconductor optical modulators based on asymmetric QWs were considered, but the modulators are based on the QWs consisting of three layers with a barrier in the center of the well, that is of two coupled QWs. Here we discuss the advantages of the asymmetric QWs consisting of two layers with a heterojunction of the second type between them. The use of type II band line-up gives possibility to separate essentially the photogenerated electrons and holes. (In the heterostructures on the base of InGaAsP the type II band line-up could be grown if the strained layers are used.) The excitons generated in the way have an essential dipole moment. It leads to a strong shift of the exciton peak by the external electric field. Notice that depending on the orientation of the field with respect to the exciton dipole moment the exciton absorption line can have "red" or "blue" shift. We developed a simple analytical model for calculation of the parameters of the modulators exhibiting linear QCSE. Further we present the calculation results of the parameters of the EA modulator based on the asymmetric QWs.

We consider QWs schematically shown in Fig.1. The electron on the lowest level in the conduction band (in e-QW) and the hole on the highest level in the valence band (in h-QW) are spatially separated in the structure (S is the distance between "the centers of the masses" of the electron and hole). The structure of the kind was considered in [10] for use in the self-electro-optic effect devices. Here, for illustration, we use some results reported in that paper.

From the point of view of the sensitivity to the electric field, the complex QW consisting of two simple coupled QWs is the only known to us competitor of the asymmetric QW we are considering here, but it has several disadvantages, namely, the shift of the absorption edge with the applied electric field is approximately twice less than that in the case of the asymmetric QW (with the same S) in the region of small fields, if the asymmetry of two coupled QWs is weak [8], [9]. Secondly, in the system of two simple coupled QWs the e-h overlap integral of the electron and hole wave functions decreases too rapidly with the applied electric field. Thirdly, the number of heterointerfaces is higher in the case of coupled QWs, that broadens the exciton peak. The structure for $\lambda = 1.3\mu m$ based on the slightly asymmetric coupled QWs was experimentally studied in [9]. The EA absorption modulator based on asymmetric coupled QWs was theoretically considered in [8], but more poor parameters of the modulator where predicted there, than we do here.

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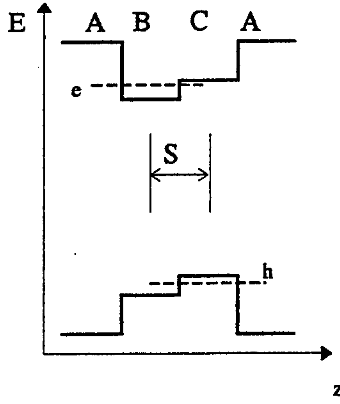

Fig. 1. The schematic band diagram of the asymmetric QW. Layer A is barrier, layer B is the QW for the electrons and layer C is the QW for holes. The heterojunction of the second type is between the layers B and C. S is the mean distance between the electron and hole.

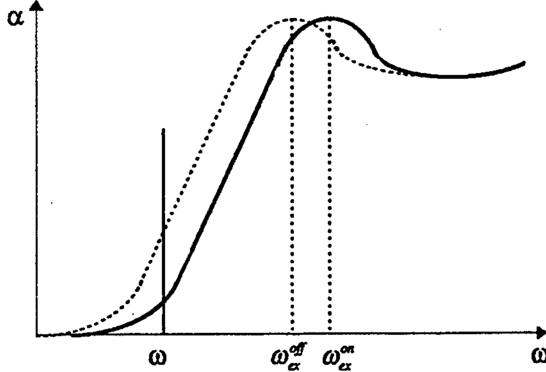

Fig. 2. The schematic view of the absorption spectrum in the active layer of the modulator. ω is the frequency of the incident radiation, $\hbar\omega_{ex}^{on}$ is the energy of the exciton transition peak in the minimum absorption state of the modulator, $\hbar\omega_{ex}^{off}$ is the energy of the exciton transition peak in the maximum absorption state of the modulator; $\hbar\left|\omega_{ex}^{on} - \omega_{ex}^{off}\right| \approx |eFS|$.

To get a modulator with good parameters one has to optimize the QW shape and, in particular, the value of S. From one side, it is desirable to choose a large value of S, since the exciton shift with the electric field is proportional to S. But from another side, it is necessary to ensure that the exciton binding energy and the e-h overlap integral are sufficiently high. The values determine the exciton absorption, that diminishes when we increase S. That is why, S is limited from above by the exciton radius, which for the typical parameters is of the order of 100 Å. Below we show that the band structure profile of the asymmetric QW proposed in [10] gives very good parameters of the EA modulator, though it is not optimized from the point of view of the above requirements.

II. Assessment of the extinction ratio

Let us assess the extinction ratio of the ridge waveguide EA modulator on the example of the QW structure described in [10]. One period of the strained MQW structure consists of 100 Å InP (layer A), 60 Å $InAs_{0.4}P_{0.6}$ (layer B) and 40 Å $In_{0.53}Ga_{0.47}As$ (layer C)[11]. The exciton peak wavelength is close to 1.55 μm. In the case of linear QCSE the extinction ratio (α) in dB could be written down in the form:

$$\alpha = 4.3\Gamma l \frac{\partial a_{asym}}{\partial F}\Delta F, \tag{1}$$

where the numeric coefficient of $4.3 = 10log(2.71...)$ appeared in order to express α in dB, Γ is the optical confinement factor of the active region, l is the length of the modulator, $a_{asym} = a_{asym}[\omega - \omega_{ex}(F)]$ is the material absorption at the given frequency of the incident radiation ω and the energy of the exciton peak $\hbar\omega_{ex}$ (see Fig.2), which is a function of the electric field (F) in the active region; ΔF is the variation of the electric field by the driving voltage. For the derivative in (1) we may use the following Eq.:

$$\frac{\partial a_{asym}(\omega - \omega_{ex}(F))}{\partial F} = -\frac{\partial a_{asym}}{\partial \omega_{ex}}\frac{\partial \omega_{ex}(F)}{\partial F} =$$

$$= \frac{\partial a_{asym}}{\partial(\hbar\omega)}\frac{\partial\left[\hbar\omega_{ex}(F)\right]}{\partial F}. \tag{2}$$

Let us consider the long-wavelength wing of the exciton peak. For the MQW (20 wells) structure with symmetric QWs (10.3nm InGaAsP wells, $S = 0$, and 8nm InP barriers), its parameters were measured in [4]. As it follows from that work, at room temperature

$$\frac{\partial a_{sym}}{\partial(\hbar\omega)} = 400cm^{-1}meV^{-1}. \tag{3}$$

The figure is not the record one. So the more narrow exciton peak was experimentally measured in the modulator structures in [5], where the MQW structure consisting of 21 periods of 93Å/135Å $InAs_{0.4}P_{0.6}/Ga_{0.13}In_{0.87}P$ was considered. The measured half width at half maximum (HWHM) of 6meV is reported in that paper, with the absorption at the exciton peak is 10500cm^{-1} and $\partial\alpha_{sym}/\partial(\hbar\omega) \approx 1100cm^{-1}/meV$. The value of $\partial\alpha_{asym}/\partial(\hbar\omega) \approx 350cm^{-1}/meV$ at zero bias was experimentally measured in [9], where a slightly asymmetric coupled QWs of 4nm each and separated by 1.5nm barrier where considered. It is to be noted here that the number of heterointerfaces in the QW is less in our case than that in [9], that is in the case the HWHM is to be more than that in our case. So, the figure used in (3) seems to be quite reasonable.

Further, we assume that the exciton binding energy is approximately the same in the case of the symmetric wells

[4] and in the case of the asymmetric ones [10]. It is justified since $S_{asym} = 5nm$ is less than the exciton dimension ($\sim 10nm$). The exciton binding energy for differently shaped quantum wells was studied in [12], and it was shown there that if the QW width is below $12nm$, the exciton binding energy approximately neither depends on QW width or applied electric field, $F \leq 150\ kV/cm$. The exciton peak width is to be approximately the same in these two cases (certainly, the quality of the heterostructure is to be the same for these two structures). So, when we change the symmetrical QWs for asymmetrical ones, only the squared e-h overlap integral (M) changes. Consequently, the exciton absorption peak value changes proportionally to M:

$$\frac{\partial a_{asym}}{\partial(\hbar\omega)} \approx \frac{\partial a_{sym}}{\partial(\hbar\omega)} \frac{M_{asym}}{M_{sym}} > \frac{\partial a_{sym}}{\partial(\hbar\omega)} M_{asym}. \quad (4)$$

$$M_{asym} \cong 0.15 + 1.3 \cdot 10^{-3} \frac{cm}{kV} \cdot F. \quad (5)$$

The last Eq. follows from [10] (see Fig.3, curve (a)). All assessment here and below we make for the model (a) (see Fig.3, 4 in [10]) for the band offset parameters. If we use the model (b) [10], then the final result would be only slightly different from that one obtained here.

If the bias voltage changes from 0 to 1 Volt, and the thickness of the undoped region is $0.5\mu m$, then F changes from $20kV/cm$ to $40kV/cm$, if the intrinsic field of p-i-n junction is taken into account. The corresponding value of M_{asym} changes from $M_{asym}^{\min} = 0.176$ to $M_{asym}^{\max} = 0.202$ (for $\vec{F}$ direction corresponding to the "blue" shift), that is its change is negligibly small. So:

$$M_{asym} \approx 0.176. \quad (6)$$

We suppose that the shape of the exciton peak does not change when we change its position by the driving voltage. It is justified in our case, since S is less than the exciton dimension, and M_{asym} only weakly changes by the small electric field.

Now let us assess the shift of the exciton line due to electric field. As it follows from Fig.4 in [10],

$$\frac{\partial \hbar\omega_{ex}}{\partial F} = 0.4 \frac{meV\ cm}{kV}, \quad (7)$$

$$\hbar\omega_{ex}^{on} - \hbar\omega_{ex}^{off} = \frac{\partial \hbar\omega_{ex}}{\partial F} \Delta F, \quad (8)$$

where $\Delta F = 20kV/cm$ for $\Delta V = 1$ Volt change of the driving voltage. The driving voltage of $V = 0$ Volt corresponds to "off" state of the modulator, i.e. the modulator absorption is minimal, and the driving voltage of $V = 1$ Volt corresponds to "on" state of the modulator, i.e. the modulator absorption is maximal. So, for $\Delta V = 1$ Volt

$$\hbar\omega_{ex}^{on} - \hbar\omega_{ex}^{off} \approx 8meV. \quad (9)$$

It is to be noted here that approximately the same value of the shift of the exciton transition energy follows from the simple calculation. When the electric field is applied, the exciton transition energy changes on the value of the product of the exciton dipole moment eS and the variation of the field (ΔF). Then, if we approximate S by the distance between the centers of the e- and h-QWs, we get the following assessment:

$$\hbar\omega_{ex}^{on} - \hbar\omega_{ex}^{off} = eS\Delta F = \quad (10)$$

$$= 5nm \cdot 20keV/cm = 10meV.$$

Eg. (10) is in excellent agrement with the calculation results (9) based on [10].

So, substituting (2) and (4) in (1) we get:

$$\alpha > 4.3\Gamma l \frac{\partial a_{sym}}{\partial(\hbar\omega)} M_{asym} \frac{\partial \hbar\omega_{ex}(F)}{\partial F} \Delta F =$$

$$= 4.3\Gamma l \frac{\partial a_{sym}}{\partial(\hbar\omega)} M_{asym} (\hbar\omega_{ex}^{on} - \hbar\omega_{ex}^{off}), \quad (11)$$

If one use the simplifying Eq.(10), Eq.(11) takes the very simple form:

$$\alpha \approx 4.3\Gamma l \frac{\partial a_{sym}}{\partial(\hbar\omega)} M_{asym} eS\Delta F =$$

$$= 4.3\Gamma l \frac{\partial a_{sym}}{\partial(\hbar\omega)} M_{asym} eS \frac{\Delta V}{d_i}. \quad (12)$$

Now we choose the remaining parameters of the modulator: the modulator length $l = 130\mu m$, the waveguide ridge width $W = 2\mu m$, the thickness of the i-layer $d_i = 0.5\mu m$, the optical confinement factor $\Gamma = 0.6$, that is a reasonable approximation for $0.4\mu m$ active region (20 QWs, $20nm$ each period). Substituting these figures Eq.(3), taken from [4]; Eqs.(6) and (7) based on [10] and $\Delta F = 20kV/cm$, that corresponds to the driving voltage of $\Delta V = 1$ Volt in (11) or (12) ($S = 4nm$), we get the very high value of the extinction ratio of $\alpha > 17dB/1V$, being that the capacity of the p-i-n junction is $C = 50fF$ only.

III. Conclusions

We have analyzed the properties of the ridge waveguide EA modulator based on the strong linear QCSE in an asymmetric MQW structure, where each well consists of two layers with the heterointerface of type II between them. A simple Eq.(12) is derived for the extinction ratio of the EA modulator.

As an example, we considered the ridge waveguide EA $1.55\mu m$ modulator with the following parameters: multiple QW structure with 20 periods, each period consists of e-QW ($6nm$), h-QW ($4nm$) and barrier ($10nm$), e-h separation $S = 4nm$, the band structure of the asymmetric QW is taken from [10], the thickness of the active region is $0.4\mu m$, optical confinement factor $\Gamma = 0.6$, thickness of the undoped region of the p-i-n junction is $0.5\mu m$, the parameters of the exciton peak are taken from the experiment [4], the modulator length is $130\mu m$, the waveguide ridge width is $W = 2\mu m$. We predict that the modulator has the high

extinction ratio of more than 17dB per 1 Volt of the driving voltage and low capacity of the p-i-n junction of 50fF only. The result shows that the modulators based on the asymmetric QWs are very promising for ultra-high-speed communication systems.

Although we made the assessment for EA modulator, the use of the asymmetric QWs is to improve strongly the parameters of the phase modulators due to the fact that the asymmetric QWs are characterized by the linear QCSE, i.e. high sensitivity of the energy of the exciton line to driving voltage.

IV. Acknowledgments

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Photodetectors of Far Infrared Radiation based on New δ-doped Wide-Bandgap Single-Crystal Semiconductor Superlattices

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At the beginning of 80s there were proposed photodetectors based on classical doped superlattices of n-i-p-i type which can have large lifetime of photocarriers and high photosensitivity owing to the effect of spatial separation of nonequilibrium photogenerated electrons and holes [1]. However, such superlattices based on wide-bandgap semiconductors possess very low photosensitivity in the infrared (IR) region of spectrum [2]. In the 70s Dohler proposed δ-doped structures [3] which are grown in such a way that in a single-crystal wide-bandgap semiconductor there are created δ-doped regions with concentration of doping impurity of order 10^{20} cm^{-3} and thickness of order of lattice period [4]. In particular, δ-doped quantum-well superlattices based on GaAs [5], InSb and InAsSb [6] were created in which the absorption of IR radiation is determined by the transitions between minibands formed in a sawtooth potential of such superlattices. The greatest progress in the development of IR photodetectors was achieved when using quantum-well superlattices, first of all, on the basis of GaAs/AlGaAs heterostructures [7]. However, all quantum-well superlattices possess two essential shortcomings: normally incident IR radiation is weakly absorbed in them and photocarriers lifetime and photosensitivity are low [7].

In this presentation we consider δ-doped superlattice of new type on the basis of single-crystal wide-bandgap semiconductors of A_3B_5 type with direct optical transitions that possesses superhigh responsivity in the region of far IR radiation up to $100\mu m$. The proposed superlattice consists of alternating δ-doped layers of donor and acceptor type and its period L consists of two pairs of such δ-doped layers the distances between which are l_a, l_d and l_{ad}, respectively (Fig. 1a). Between δ-doped acceptor layers there is a nondegenerated semiconductor of p-type and in the other regions of lattice there is a nondegenerated semiconductor of n-type. For simplicity we put $\sigma_a = \sigma_d = \sigma$ where σ_d and σ_a are the numbers of atoms per the square unit in δ-doped donor and acceptor layers, respectively. In this case all electrons from donor atoms of δ-doped layers come to acceptor

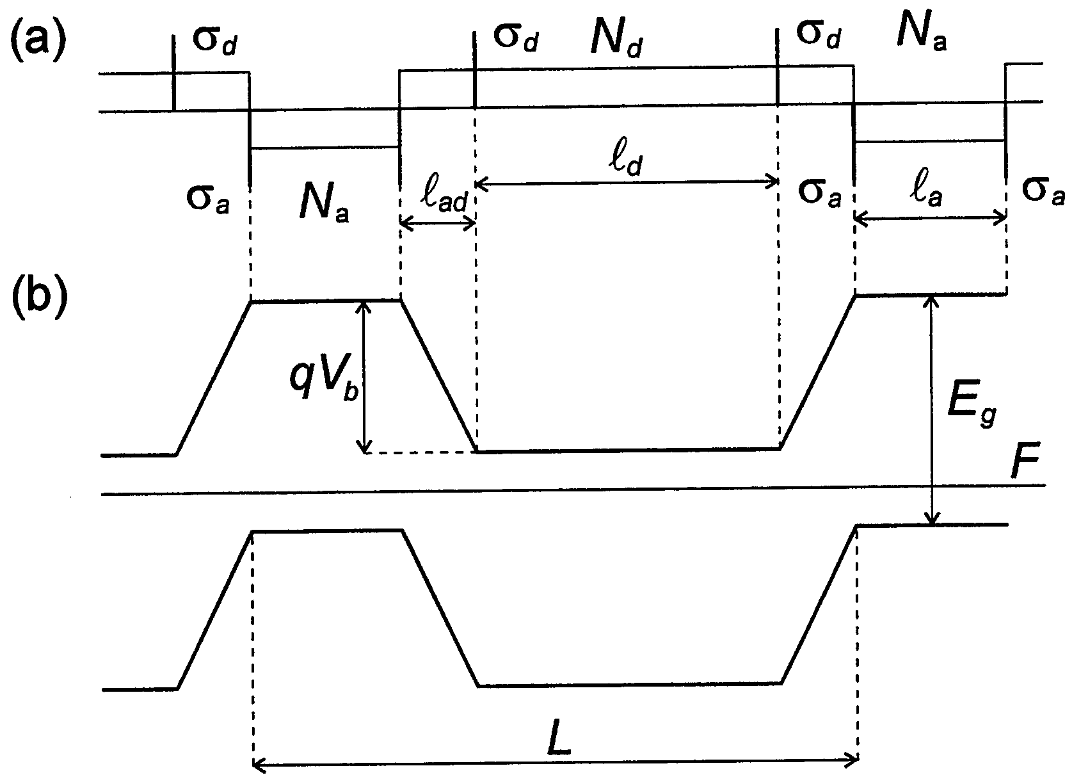

Fig. 1. Structure (a) and band diagram (b) of δ– doped superlattice.

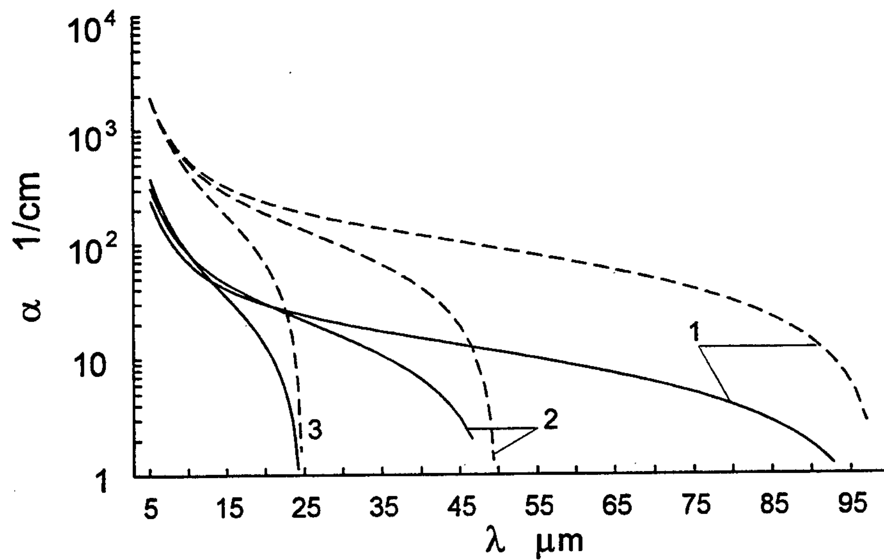

Fig. 2. Absorption coefficient of δ–doped InSb superlattice:
dashed line - absorption coefficient of high field layer, solid line - effective absorption coefficient of superlattice ($\sigma_a = \sigma_d = 5{*}10^{12}$ cm^{-2}, curves 1 - ℓ_{ad} = 40 å, curves 2 - ℓ_{ad} = 38 å, curves 3 - ℓ_{ad} = 33 å).

atoms of neighboring δ-doped layers and δ-doped layers become charged planes with the density of built-in charge $+q\sigma$ and $-q\sigma$, respectively, where q is the charge of electron. As a result, constant electric field $E = 4\pi q\sigma/\epsilon$ arises between every pair of such donor and acceptor δ-doped layers and energy-band diagram of the superlattice has the form shown in Fig. 1b. In this superlattice the absorption of radiation with the quantum energy $\hbar\omega < E_g$ will be determined by Franz-Keldysh effect in the regions of strong field of thickness l_{ad} where electric intensity can reach huge values of order 10^6 V/cm at $\sigma = 10^{13}$ cm^{-3} and $\epsilon \approx 16$. By this, it is essential that there are no tunneling currents between p- and n-regions since these regions are nondegenerated semiconductors.

In the majority of direct-gap semiconductors A_3B_5 interband matrix elements of impulse operator P_{cv} for the optical transitions from the band of light and heavy holes are equal to each other and effective masses of light and heavy holes are strongly different. For this reason in weak electric fields the absorption of photon with $\hbar\omega < E_g$ is determined by tunneling of electrons and light holes and the corresponding absorption coefficient is exponentially small relative to the coefficient of interband absorption α_E [8].

At the same time, it is well known that in the absence of electric field interband absorption is chiefly determined by transitions of electrons from the band of heavy holes because of the high density of states of this band. We showed that for the same reason in superstrong electric field (of interest for us) the absorption of longwave photons with $\hbar\omega < E_g$ is determined by heavy holes rather than light ones. This result follows from the basic formula for the electroabsorption coefficient α_E obtained in [8] for semiconductors with parabolic low of dispersion. We showed that in the proposed superlattice one can easily enough create electric fields such that condition $E \gg (E_g - \hbar\omega)^{3/2}(2\mu)^{1/2}(q\hbar)^{-1}$ is fulfilled both for light and heavy holes even at $\hbar\omega \approx E_g/2$ and found a general expression for electroabsorption coefficient which in asymptotic limit for such superstrong fields is:

$$\alpha_E = \left[3^{1/12}\Gamma^2(2/3)R\sqrt{\hbar\omega_E}(\hbar\omega - E_g + qV_b)\right] / [4\pi qV_b] \qquad (1)$$

where $\Gamma(x)$ is Gamma-function; $R = (2\mu/\hbar^2)^{3/2}(2q^2P_{cv}^2)/(m^2cn\omega)$; $\omega_E = (qE)^{2/3}/(2\mu\hbar)^{1/3}$; n is the refraction coefficient of semiconductor; $\mu^{-1} = m_c^{-1} + m_v^{-1}$, m_c and m_v are effective masses of electron and hole. In deriving (1) we took into account that in the superlattice considered the absorption of radiation with $\hbar\omega < E_g$ takes place in a thin layer of semiconductor of the thickness $l_{eff} = (\hbar\omega - E_g + qV_b)/(qE) < l_{ad}$ and the thicknesses l_a and l_d are large enough so that the energy spectrum of electrons and holes in corresponding potential wells (Fig. 1b) can be considered quasicontinuous. From (1) one can see that, in contrast to weak electric fields [8], in superstrong fields electroabsorption coefficient weakly depends on the energy of quantum up to the values $\hbar\omega = E_g - qV_b$ and is close to the coefficient of interband absorption. Emphasize that, in principle, the values $\hbar\omega = E_g - qV_b$ can be made as small as is wish.

These conclusions are confirmed by our numerical calculations carried out for GaAs, InSb and InAs according to the general formula obtained by us. They show that in the superlattice considered the absorption coefficient can be large enough for GaAs up to $\lambda = 14\mu m$ and InAs and InSb up to $\lambda = 50 - 100\mu m$

(Fig. 2).

We also calculated main characteristics of the photodetectors based on the proposed superlattice and formulated the requirements for the optimum parameters of these δ-doped superlattices on the basis of GaAs, InSb and InAs and found that such superlattices (like classical doped superlattices [1]) possesses very high lifetime of photocarriers and superhigh responsivity. Evaluations show that owing to the spatial separation of photocarriers their lifetime even in InSb can reach the values of order $100\mu s$ at the temperature 100K. For these reasons the proposed superlattices are very promising as an elements of IR focal plane arrays.

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Optical loss investigation in InAs - based long wavelength lasers.

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1. Introduction

In the field of the long wavelength lasers on the base of InAs great progress was achieved in the last few years [1], but working temperature and quantum efficiency of these lasers stayed much lower than for lasers working on the shorter wavelength, less than 1.5 μm [2]. It was shown that Auger recombination determined their maximal working temperature, but this did not explain the low quantum efficiency of these lasers at low temperatures ($\sim$ 77K). One peculiar feature of this laser material is that band gap (E_g) and the spin-orbital splitting (Δ) have nearly the same value. Due to this band structure the intervalence band absorption (IVA) has to be much stronger at the laser wavelength than for lasers on InGaAsP/InP, where it is important loss mechanism [3]. We calculated IVA in InAs and determined its influence on characteristics of long wavelength lasers.

2. Theoretical model

We studied absorption due to transitions between the split-off band and the heavy and light hole bands, and compare the IVA with gain. Four band Kane model was safely used for calculation of the band structure, because the wavevectors of all particles involved were small. We applied the projection operator technique [4] and the following expressions for absorption coefficient were obtained:
For transitions between split-off band and heavy hole band (process 1, it takes place when $\hbar\omega > \Delta$):

$$\alpha_h^{so} = A\,\frac{M_{so,h}^{5/2}(\hbar\omega-\Delta)^{3/2}}{1+\exp\left[\frac{M_{so,h}}{m_h}\frac{\hbar\omega-\Delta}{T}-\frac{\zeta_h}{T}\right]}; \qquad (1)$$

For transitions between split-off band and light hole band (process 2, it takes place when $\hbar\omega < \Delta$):

$$\alpha_l^{so} = A\frac{17E_g^2 + 20E_g\Delta + 6\Delta^2}{3E_g^2}\frac{M_{so,l}^{5/2}(\Delta - \hbar\omega)^{3/2}}{1 + \exp\left[\frac{M_{so,l}}{m_l}\frac{\Delta - \hbar\omega}{T} - \frac{\zeta_h}{T}\right]}, \qquad (2)$$

Where $A = \frac{2\sqrt{2}e^2\hbar\omega}{c\sqrt{\varepsilon_\infty}\hbar^2\Delta^2 m_{so}^2}$, $M_{so,i} = \pm\frac{m_{so}m_i}{(m_i - m_{so})}$, $m_i = m_h$ or m_l. m_h, m_l, m_{so} are hole masses for heavy holes and split-off bands, ζ_h is holes Fermi level, ω is the light frequency and other symbols are standart . These expressions coincide with the relevant formulae from the paper [5] in the case of the nondegenerate holes. It can be shown from (1) that maximum value of the IVA is nearly independent on temperature and is function of hole concentration only. It can be seen from (1) and (2) that absorption due to process 1 when it exists, is more than ten times stronger than absorption connected with process 2 due to higher density of states. To estimate influence of the IVA on the properties of the long wavelength lasers we compare absorption due to process 1 with gain (g) (The expression for gain is taken from [6]). If we disregard Fermi-factors that are near the same in both cases we obtain for the ratio g/α:

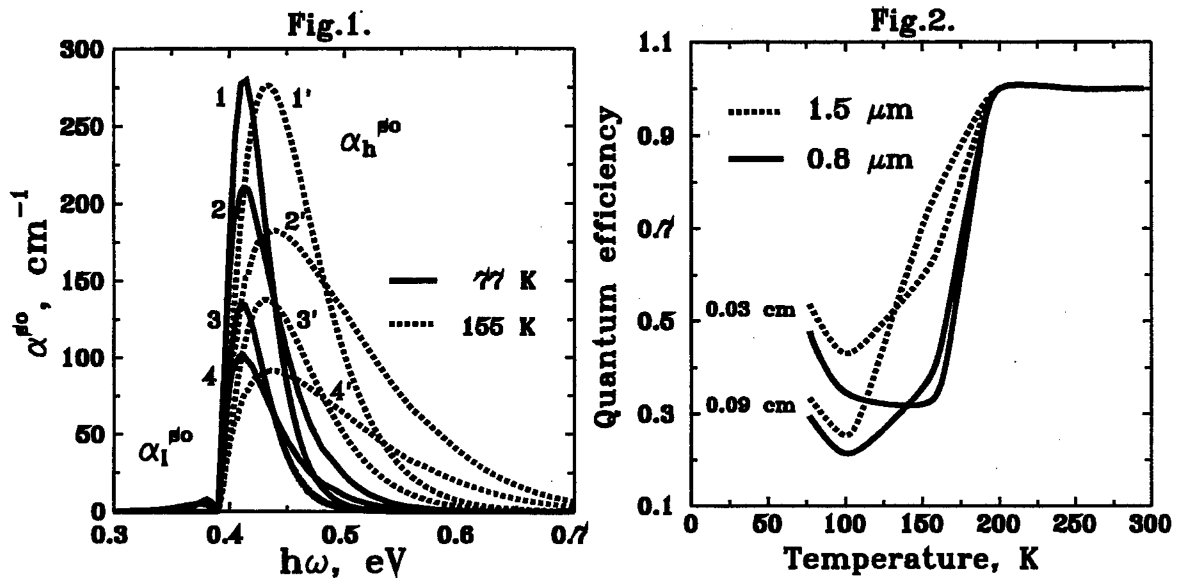
$$\frac{g}{\alpha_h^{so}} = \frac{2}{5}\frac{E_g}{\hbar\omega - \Delta}\frac{\sqrt{m_c}m_{so}^2}{M_{so,h}^{5/2}}. \qquad (3)$$

If we take $\hbar\omega = E_g$, we obtain for InAs at 77 K g/α=1.1. This great value of the IVA follows from the higher reduced density of states for transitions between heavy hole and split-off bands than for transitions between valence and conduction bands. This factor compensates small ratio $(\hbar\omega - \Delta)/E_g$, that appears because processes of the IVA are forbidden in the Γ-point of the Brillouine zone. So IVA heavily influences not only quantum efficiency but also the threshold carrier density for long wavelengh lasers. Frequency dependence of the IVA in InAs due to process 1 and 2 is presented on the Fig.1. Curves 1,1′,3,3′ correspond to expression (1) received in the first approximation at the parameter $\gamma = (\hbar\omega - \Delta)/\Delta << 1$. Curves 2,2′,4,4′ were calculated in the strict Kane model. The carrier concentrations were $6 \cdot 10^{17}$cm^{-3} - curves 1,1′,2,2′ and $3 \cdot 10^{17}$cm^{-3} - curves 3,3′,4,4′. It is evident that IVA can be important only if $\hbar\omega > \Delta$ when the absorption process from the heavy hole band takes place.

3. Results and discussion

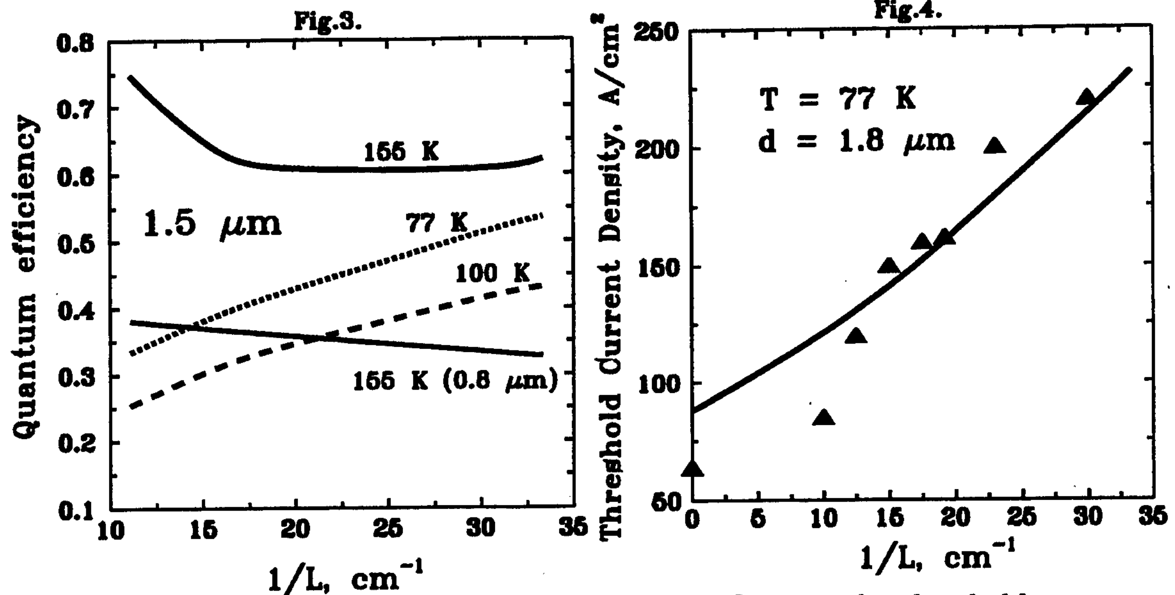
We investigate the influence of the IVA on the threshold current and quantum efficiency for heterolasers with active layer from InAs. We assume standart structure

with InAs active layer with thickness $d = 0.8 - 1.5\mu$m and InAsSbP cladding [1]. Calculation are fulfilled for laser length $L = 0.03 - 0.09$cm. We disregard all other optical losses besides output losses and losses due to IVA and calculate the threshold carrier concentration from the usual equality between gain and total losses on the frequency where effective gain $(g - \alpha)$ has maximum. Quantum efficiency is determined as ratio of output losses to total losses. In InAs the value of spin-orbital splitting is nearly independent on temperature (we accept it value 0.39 eV). Band gap of InAs depends on temperature approximately lineary from 0.41 eV at 77 K till 0.35 eV at 300 K [7]. So in the temperature range 150-200 K Δ and E_g are nearly coincide. That gives a number of peculiarities on the threshold current and quantum efficiency characteristics. External quantum efficiency as function of the temperature is presented on Fig.2 for thickness of active layer 0.8 μm and 1.5 μm and for laser length 0.03 cm and 0.09 cm. The minimum at temperature 100 - 160 K could be seen for all design parameters. It should be underlined that IVA absorption increases not only due to increase of the carrier concentration but also due to displacing of gain maximum through the IVA spectrum with temperature growth.



We also calculated the dependences of external differential quantum efficiency η_i on output losses. They were shown in Fig.3 for three temperatures (77K, 100K, 155K) and for several thicknesses: $d = 1.5\mu m$ and $0.8\mu m$. It should be seen for T=77K and 100K the usual increase η_i with $(1/L)$. At T=155K η_i droped with $1/L$ grouth because IVA increased quicker than output losses at this temperature. We also calculated temperature dependences of threshold current density. Only radiative recombination [8] and Auger recombination [9] were taken into account. It occurs that for all temperatures the nonradiative current is bigger then radiative. The threshold current density dependences on output losses for laser with d=1.8 μm (InAs), T= 77 K are shown on Fig.4. Triangles are experimental data from [10],

contineous line is result of calculation.



In summary we point out that the IVA heavy influences the threshold current and quantum efficiency of lasers based on InAs and can give anomalies on the temperature dependences of its characteristics. To improve the characteristics of these lasers solid solutions with $E_g < \Delta$ must be used to exclude IVA processes at all temperatures.

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Modulation of infrared radiation and photoconductivity in quantum wells in transverse and longitudinal strong electric field

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Light modulation connected with variation of absorption coefficient in transverse (perpendicular to the layers) and longitudinal (parallel to the layers) electric field was studied in simple rectangular and asymmetric tunnel-coupled quantum wells (QW) GaAs/AlGaAs. Two different mechanisms of modulation for these cases are proposed. Photoconductivity of quantum wells in transverse field was also investigated.

1. Transverse electric field. To study electrooptical and photoelectric properties of QW the MQW structure was grown on semiinsulating substrate. The 50 period structure consisted of GaAs QW of width L_W = 5.1 nm and 25.4 nm $Al_{0.33}Ga_{0.67}As$ barriers. The carrier concentration in wells was $3x10^{11}$ cm^{-2}. The substrate and MQW structure were separated with doped (N_D = 10^{18} cm^{-3}) layer of 0.5 μm thick served for creation of ohmic contact. Similar contact was created on free surface of the structure. Sample had an area of 6×4 mm^2. Optical radiation was introduced into the sample through the edge cut at an angle of 45°.

The absorption spectrum for this sample #1 is shown in the figure 1. We used p-polarization of light (electric field of light wave is directed at angle 45° to the optical axis of structure).

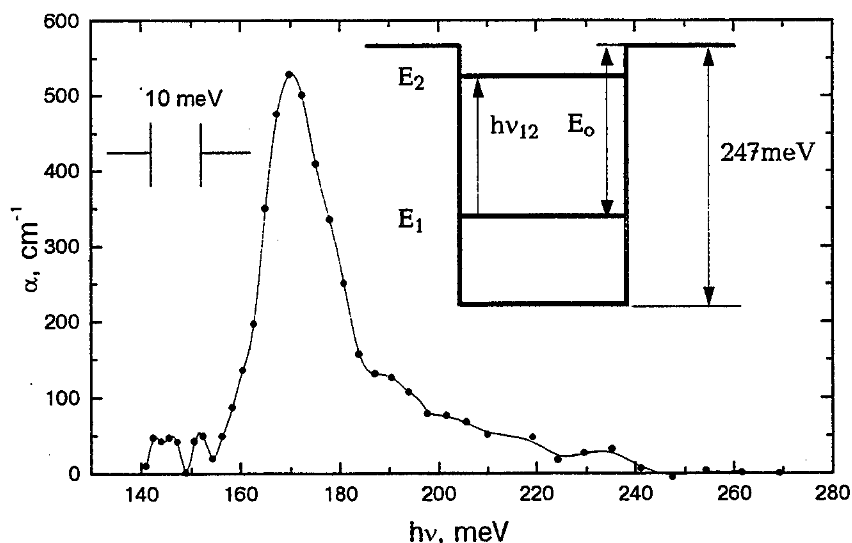

Figure 1. The equilibrium spectrum of optical absorption for sample #1 at T = 77 K.

According to the calculations there are 2 quantum levels in the QW with energies $E_1 = 73$ meV and $E_2 = 243$ meV. The upper level is located at only 4 meV below top of the well. So, equilibrium absorption spectrum has a shape of peak at quantum energy $h\nu_{12} = E_2 - E_1 = 170$ meV. The peak is asymmetric: absorption at shortwave wing is more in

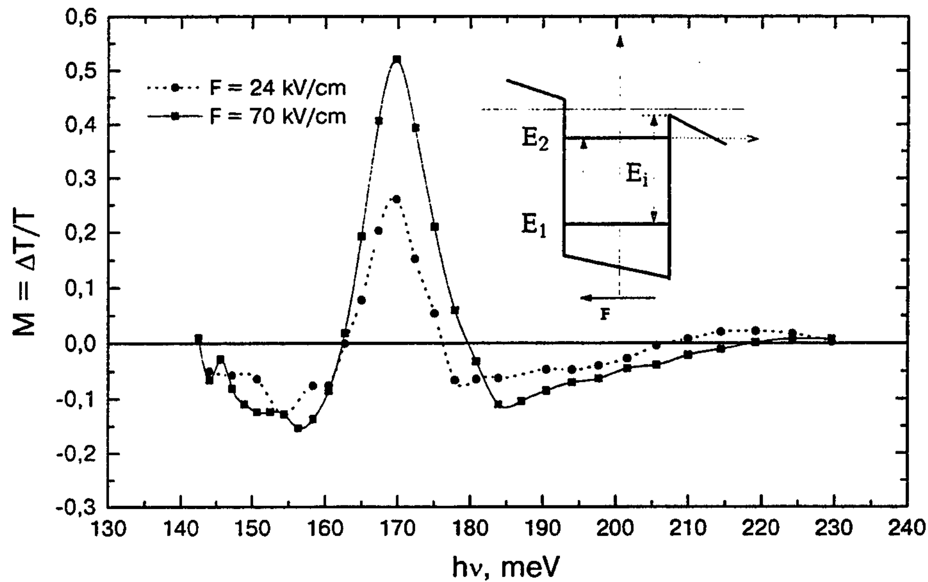

Figure 2. Optical transmission modulation for sample #1 in transverse electric field.

tensive than at longwave one due to contribution of bound-to-continuum transitions (photoionization effect) [1].

Electrooptical studies are carried out in pulse electric field. Amplitude of pulses did not exceed 20 V that corresponds to the electric field F = 70 kV/cm. Duration of pulses was 2 μs. The spectra of light modulation at different electric fields are presented in the figure 2.

There is optical lightening of sample at $h\nu \approx h\nu_{12}$. The region of lightening is surrounded by darkening regions. This is explained by broadening of intersubband ($E_1 \rightarrow E_2$) absorption line due to tunneling electrons from level E_2 into above-barrier space allowed in transverse electric field (see inset in fig.2). One more peak of optical lightening was found at short wavelength. It was more weak and was connected with red shift of photoionization spectrum with electric field. The cut-off of photoionization linearly decreases with electric field: $E_i = E_o - eFL_W/2$. The Stark shift of level E_1 is neglected since it did not exceed 3 meV in electrical field used.

Variation of spectral width of absorption line versus electric field is presented in figure 3. The bend point at this curve corresponds to electric field F^* such that photoionization threshold matches with the energy of intersubband transitions.

Photoconductivity spectrum was studied at the constant bias (F = 12 kV/cm). It was similar to the absorption spectrum.

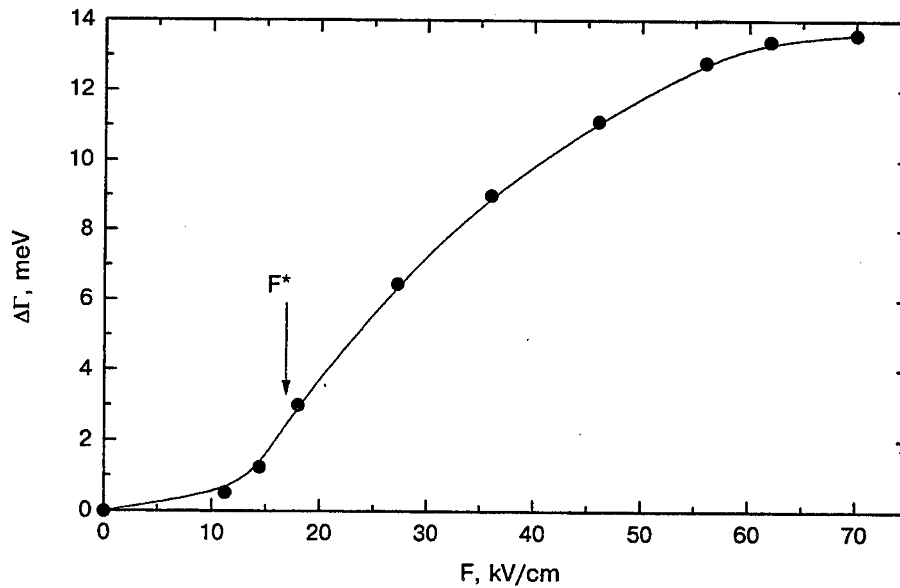

Figure 3. Intersubband absorption line broadening in transverse electric field (sample #1).

2. Longitudinal electric field. Structure of second type represents the selectively doped system consisted from two quantum wells of different width separated by tunnel-transparent barrier (see Fig. 4). The central 10 nm region of wide barrier was doped with Si providing sheet carrier concentration $N_s = 5 \cdot 10^{11}$ cm^{-3}. The number of structure periods was 150.

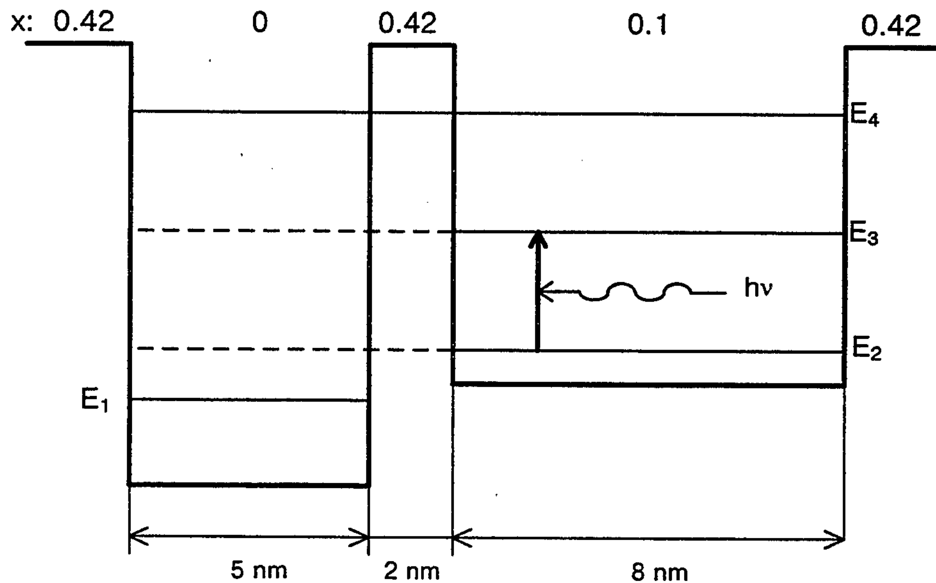

Figure 4. The energy diagram of tunnel-coupled quantum well structure GaAs/$Al_xGa_{1-x}As$ (without considering space charge effects).

This structure (Sample #2) was grown by method of molecular beam epitaxy (MBE) on semiinsulating GaAs substrate. According to the calculations the energy positions of quantum levels measured from bottom of deep well are: $E_1 = 84$ meV, $E_2 = 130$ meV, $E_3 = 237$ meV, $E_4 = 322$ meV.

The equilibrium IR absorption spectra for such structures were measured for light of *s*- and *p*-polarization in multipass waveguide geometry (see inset in Fig. 5). Difference between these spectra is shown in Fig.5. One can see the spectra transformation with temperature due to electron redistribution between energy subbands in wide and narrow QW.

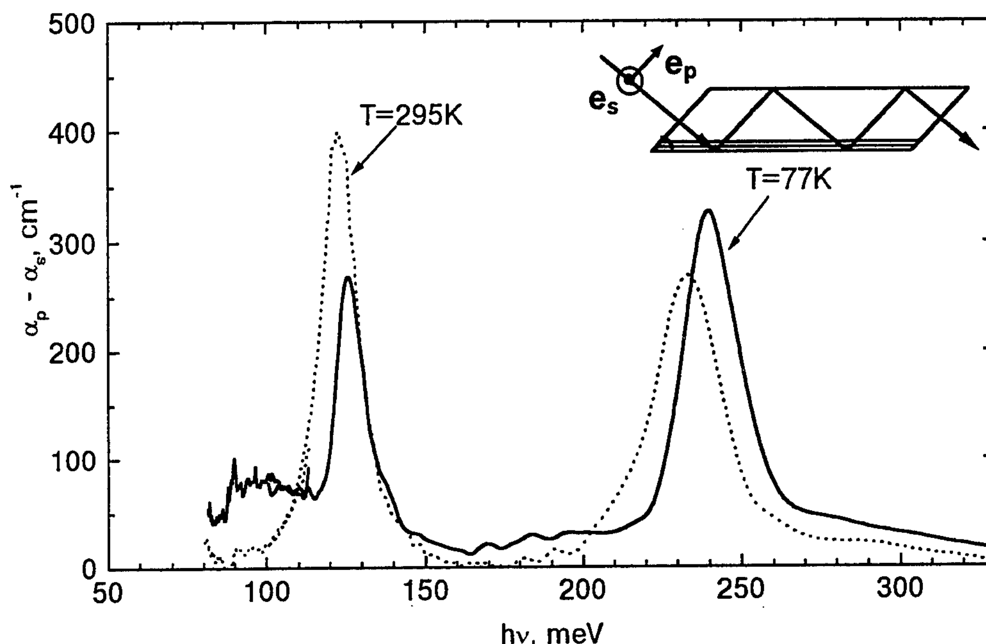

Figure 5. The equilibrium light absorption spectra for structure with tunnel-coupled wells (Sample #2). The unit polarization vectors for light of p- and s-polarization are shown in the inset.

The strong heating longitudinal electric field results in transitions of electrons in real space from narrow well into wide one (the electrons occupied level E_2). Therefore optical absorption appears in the region $\hbar\omega \approx E_3 - E_2$.

We investigated experimentally dependence of absorption modulation on heating electric field at $\lambda = 10.6$ and 9.6 μm and analyzed it. Comparing the variation of absorption coefficient due to electron heating in electric field and the temperature dependence of equilibrium absorption at the same wavelength we determined the electron temperature as a function of electric field.

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Superluminescence and Reversible Picosecond Bleaching of a GaAs Thin Epitaxial Layer

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Part one of this work presents an experimental study of characteristics of the edge radiation that arises (for picosecond lengths of time) during photogeneration of electron-hole plasma (EHP) in a GaAs layer. Photogeneration took place under interband absorption of a giant light pulse having duration of 14 ps. Experiments were carried out at room temperature. Wave-guide properties of GaAs layer and the radiation absorption in non-excited region of GaAs prevented the radiation from going outwards. We have proved superluminescent nature of the radiation by studying that portion of it which goes out of sample because the wave-guide is not perfect. That the radiation had a superluminescent nature was earlier claimed according to indirect signs. It was necessary to establish its real nature since we had earlier observed a number of optoelectronic effects [1] occurring due to a strong interrelationship between that radiation and EHP. Those effects have been linked to Raman scattering, phonon oscillations, intraband absorption of excitation light, EHP heating by the radiation itself (i.e. heating that is a result of intraband absorption of the radiation and the difference between the state energies in which the electron generation and recombination take place). Accordingly, in this way occur variations in the EHP density and temperature as well as in the energy and spectrum of the radiation. Such effects make it possible to perform a picosecond light modulation of transparency and photoconductivity and may also affect the functioning of those elements of semiconductor optoelectronics in which the stimulated radiation is used.

In part two of this work have been discovered new properties of the bleaching (enhancement of transparency T) of a GaAs layer that is being created under the above mentioned photogeneration of EHP. Bleaching that has been measured by the "excite-probe" technique is described by a ratio $lg(T^1/T^0)$; this ratio also indicates a change in the sum of the charge carrier population of the energy levels both in valence and conduction bands, which are bound by means of a direct optical transition, marks 1 and 0 indicating the excitation presence and absence, respectively. Earlier, it has been found by the authors [2] that above the certain threshold level, Θ, the bleaching is a nearly reversible function of time with respect to the excitation light intensity change. It means that the bleaching rises at the pulse front but drops down to a Θ level lagging behind only by ~ 10 ps in relation to the light intensity decrease as the pulse falls. The bleaching drops so fast due to the charge carrier recombination which thus generates the radiation in question. Below the Θ level the bleaching diminishes, the time being peculiar to that of the spontaneous recombination in GaAs i.e. ~ 1 ns. The threshold level Θ of bleaching under a fixed diameter F of the excitation beam does not depend in a wide range either on the photon energy or on the integral energy of the pulse. In the present work it has been experimentally found and explained (in terms of established nature of the edge radiation) that the diameter F of a photoexcited region of GaAs layer exerts an influence both on the threshold preceding the reversible changes in the bleaching and on the time (a picosecond one) of bleaching relaxation. The latter effect alongside with the found variation of the radiation spectrum with the diameter F change have

proved the influence of EHP heating on recombination superluminescence, the heating being created by the superluminescence itself (a mechanism for such feed back has been considered theoretically in [3]). Found was also a correlation between the bleaching variations with the increase in the energy of the excitation pulse and a kindling of radiation peculiar to it. Effects discovered may exert an influence on the functioning of elements relating to the above mentioned areas of semiconductor optoelectronics.

1. Dependence of the radiation energy density D_s on the excitation pulse energy density D_{ex} and diameter F

Note, D_s and D_{ex} are the energy densities average over the photoexcited area and integral over the time, D_s being also integral over the spectrum. Mention should be made that in our experiments it was not possible to reveal any signs of superluminescence by measuring density D_s when changing the size of the area in which the radiation intensifies, the size being of the order of F. Density D_s did not depend on F in a wide range of D_{ex} (see Fig.1). It does not contradict the hypothesis of superluminescence nature of radiation, if take into account that in ~ 10 ps after the excitation ends the studied recombination radiation nearly completely removes the population inversion characteristic of the radiation manifestation, [4,5]. In this case, the change in a total radiation intensification due to the change of F cannot help affecting the quantity D_s.

2. Superluminescence spectrum width

Superluminescence spectrum width, $\Delta\hbar\omega$, contracted by ~ 3 times, gaining saturation, as D_s and the diameter F of a photoexcited area increased (See Fig.2) The $\Delta\hbar\omega(D_{ex}F)$ dependence had an approximately universal character. The above said agrees well with conclusions of theory of superluminescence (an enhanced spontaneous radiation in an active medium without cavity) [6] providing that D_{ex} increase results in the rise of the enhancement coefficient α (having a maximal value over the spectrum). Notion should be made that theory [6] takes into account a spatial inhomogeneity of the enhancement coefficient, which is characteristic of our experiment too.

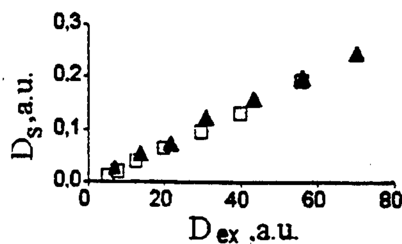


Fig.1 Dependence of the GaAs radiation energy density D_s on the density D_{ex} of the energy of excitation pulse at the energy of the excitation photons $\hbar\omega_{ex}$ = 1.485 eV: ▲-F = 0.2 mm; □- F = 0.7 mm.

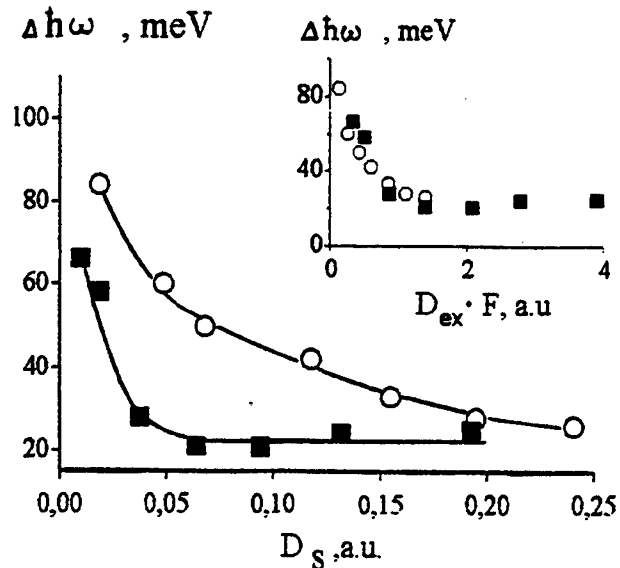


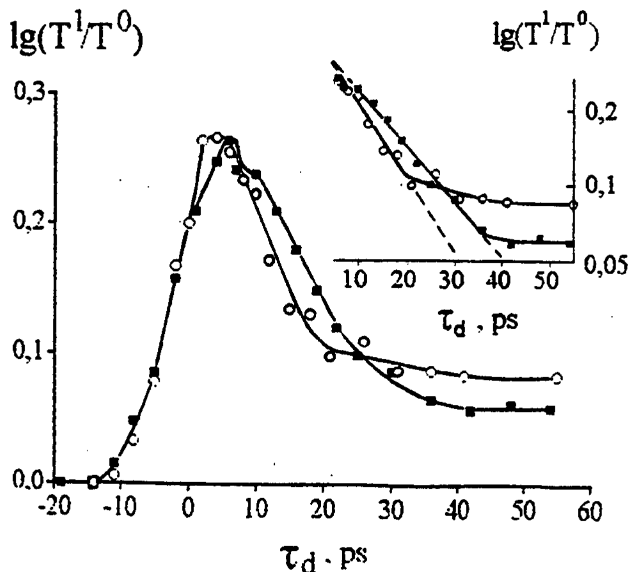
Fig.2. Dependence of the radiation spectrum width $\Delta\hbar\omega$ on D_s (the insertion: the dependence $\Delta\hbar\omega(D_{ex}F)$) at $\hbar\omega_{ex}$ = 1.485 eV: o - F = 0.2 mm, ■ - F = 0.7 mm. Continuous lines here and elsewhere are used for clearness.

3. A picosecond relaxation of GaAs bleaching

Bleaching relaxation down to Θ level occurs when EHP is being cooled and superluminescence is decreasing the EHP density in such a way that the difference between Fermi quasi-levels for electrons μ_e and holes μ_h only slightly exceeds the gap band width [5]. It has been found that a characteristic time of a bleaching relaxation, τ_r, rose as F increased (See Fig.3). It is linked with the fact that the growth of F leads to the increase in the rate of heating EHP due to an intraband absorption of superluminescence radiation (the absorption coefficient $\beta \sim 10$ cm^{-1} [7]). Re-distribution of charge carriers by energies during EHP heating reduces the population inversion. It turns out in the end that F increases (in the range $F \lesssim \beta^{-1}$), both the temperature relaxation and the superluminescent recombination of EHP slow down [3] and in this way inevitably slows down the relaxation of the energy level population by photoexcited charge carriers. This accounts for the observed enhancement of τ_r with F. Apparently, owing to EHP heating by superluminescence the time τ_r proved larger than the time of an energy relaxation of EHP due to generation of optical phonons [8], which in the absence of superluminescence would have determined the bleaching relaxation.

4. Superluminescence spectrum

The above described mechanism of τ_r - F relationship presumes that for a larger F superluminescence must occur at a higher EHP temperature and lower population inversion i.e. at a smaller width of the enhancement spectrum. Localization of the longwave edge of the enhancement spectrum should be approximately the same for the both of F. Then the discrepancy between the enhancement spectra at different F should result in a concentration of the superluminescent spectrum in a more long-wave region at a larger F which was really observed experimentally even when $\Delta\hbar\omega(D_{ex}F)$ dependence had finally gained saturation (See Fig 4).



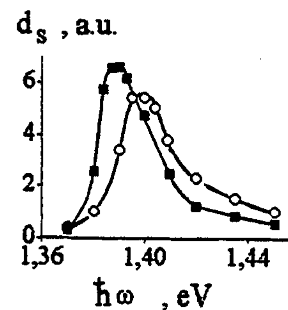


Fig.4. Spectra of the average (over the photoexcited sample area) density d_s of the energy of radiation from GaAs at $\hbar\omega_{ex}$ = 1.485 eV, D_{ex} = 56 a.u.: o - F = 0.2 mm; ■ -F = 0.7 mm.

Fig.3. The variation of bleaching of GaAs with a delay time τ_d between the exciting (ex) and probing (p) pulses at $\hbar\omega_{ex}$ = 1.485 eV, $\hbar\omega_p$ = 1.568 eV, D_{ex} = 56 a.u.: o -F = 0.2 mm, ■ - F = 0.7 mm. Bleaching drop given in the insertion on a semilogarithmic scale occurs with a time constant τ_r = 19 ps at F = 0.7 mm and τ_r = 15 ps at F = 0.2 mm.

5. Bleaching intensification under D_{ex} growth

As is seen in Fig 5, with D_{ex} increase the growth of bleaching slows down, which is similar to $\Delta\hbar\omega$ reduction that indicates kindling of superluminescence. This experimental fact is in good agreement with the idea [2] that in the course of its increasing the concentration of generated EHP first depends mainly on the charge carriers photogeneration rate (i. e. on interband absorption of the excitation light). But when superluminescence kindles, the EHP density will be governed by EHP temperature, which leads to a weaker bleaching dependence of D_{ex}.

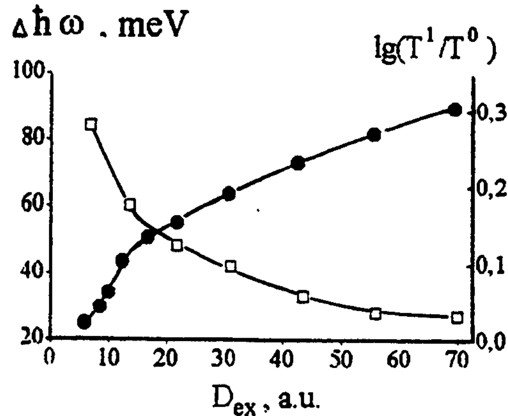


Fig.5. Dependence of bleaching of GaAs (•, $\hbar\omega_p$ = 1.568eV, τ_d = 6 ps) and a radiation spectrum width $\Delta\hbar\omega$ - □ on the density D_{ex} at $\hbar\omega_{ex}$ = 1.485 eV, F = 0.2 mm.

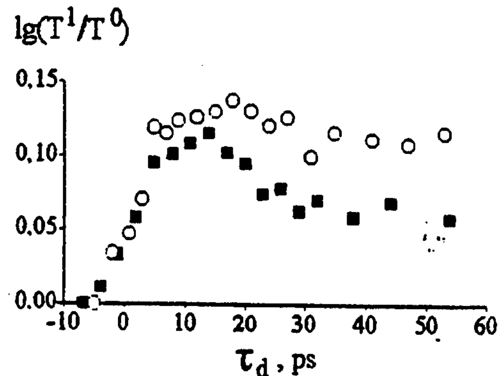


Fig.6. The variation of bleaching of GaAs with τ_d at $\hbar\omega_{ex}$ = 1.485 eV, $\hbar\omega_p$= 1.568 eV, D_{ex} =12.5 a.u.: o- F= 0.2 mm; ■ - F = 0.7 mm.

6. Threshold of reversible bleaching

Fig.6 shows that at a fixed D_{ex} for a larger F takes place a significant reversibility of bleaching, while for a smaller F the bleaching reversibility is not pronounced so far. Accordingly, the reversibility of bleaching arises at large D_{ex} and Θ if F decreases. Calculations have shown [4,6] that at the stage of kindling the intensity of superluminescence grows with αF exponentially. Therefore, the identical for different F superluminescence, which is sufficient for providing picosecond bleaching reversibility, should arise under different enhancement coefficients α_{th}. A larger α_{th} (at a smaller diameter F) requires then a larger EHP density, which , in turn, determines larger values of Θ and D_{ex}.

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New infrared integrated focal plane arrays

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Nowadays infrared (IR) focal plane arrays (FPA) possessing limitingly high threshold characteristics are developed only in hybrid variant when photodetectors made of InSb [1] or CdHgTe [2] are connected to a silicon microscheme (used for signal processing) through contact indium bumps. Planar FPA based on PtSi Schottky photodiodes [3] and microbolometers [4] and also hybrid FPA based on GaAs/AlGaAs quantum-well structures [5] have much lower threshold characteristics.

In this report we describe operation principles and main parameters of FPA of new type proposed and fabricated by us on the basis of InSb. This FPA, in contrast to charge-coupled and charge-injection devices, does not use transfer of photocarriers along the semiconductor–insulator interface and, in contrast to other existing IR FPA, does not use hybrid scheme based on indium bumps. Proposed FPA has very simple architecture and extremely high parameters.

In the proposed FPA photodetectors and elements of photosignal processing are fabricated on a single InSb substrate, by this, every photosensitive cell of this array is *a new semiconductor device which combines all main functions: detection of IR radiation, photosignal storage and readout.* This new device is a planar p^+-n junction which is covered with a thin insulator film; this film, in turn, is covered with two electrodes 1 and 2 (Fig. 1a).The capacitors produced by these electrodes and the low-resistive p^+-region of the

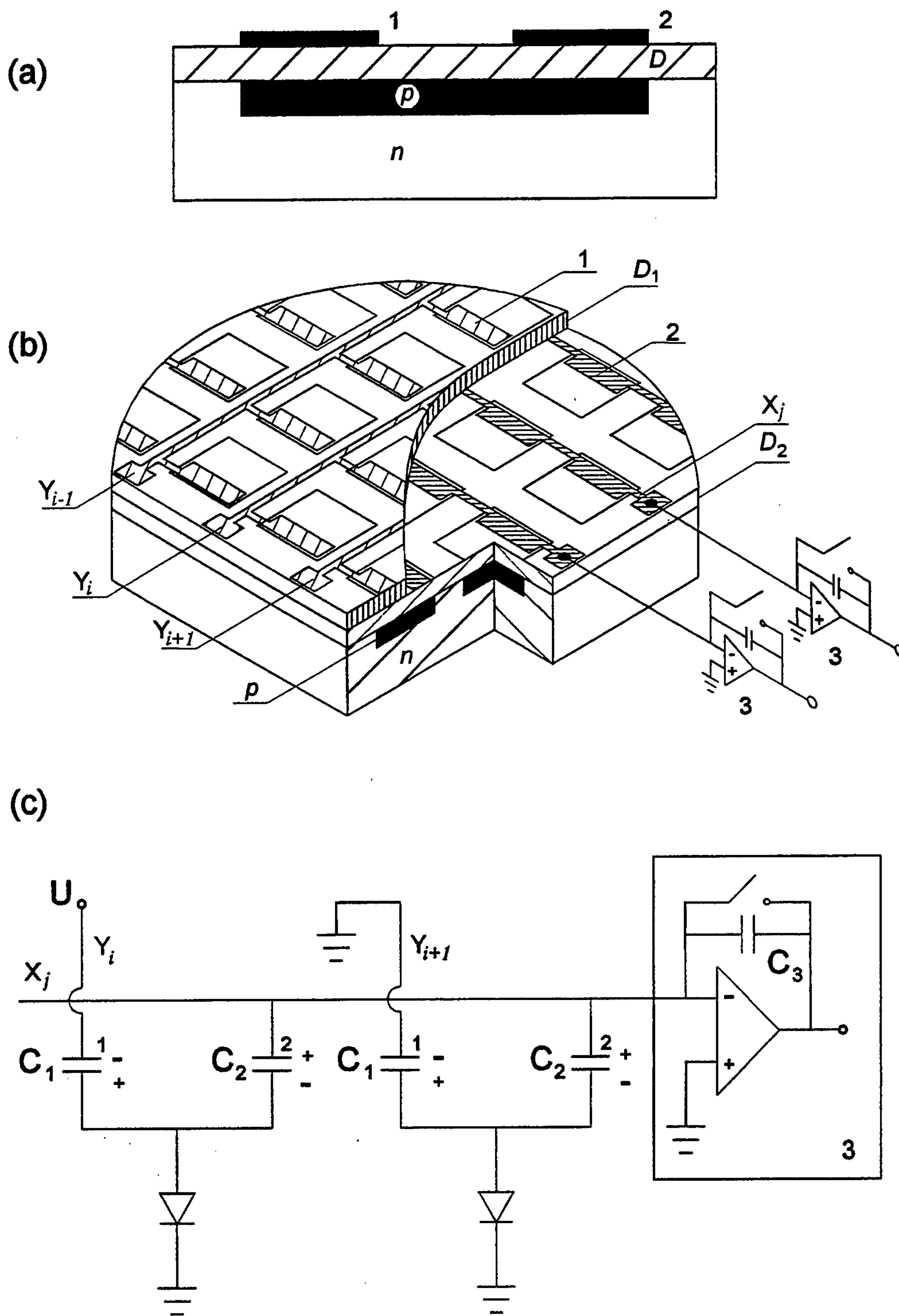

Fig 1

Structure of new photosensitive device (a), new focal plane array on it's base (b) and equivalent cirquit of FPA (c).

1 - electrode, connected to column bus Y_i, 2 - electrode, connected to row bus X_j, 3 - charge amplifier; *D*, D_1, D_2-dielectric layers.

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p^+-n junction are used as elements for storage and readout of photosignal and p-n junction is used as both photodetector and element of commutation.

This new device allowed us to develop FPA of very simple architecture. All electrodes 1 of each column of the array are interconnected with conductive links (buses) Y_i, whereas all electrodes 2 of each row of the array are interconnected with buses X_j (Fig. 1b). Every bus X_j is connected to an inverting input of corresponding operational amplifier which operates in a charge-amplification mode and maintains close-to-zero voltage at each bus X_j. The semiconducting n-layer (substrate of the array) is grounded. Equivalent circuit of such FPA is shown in Fig. 1c. Photosignal storage takes place continuously and simultaneously in all photosensitive cells, whereas readout occurs simultaneously from the whole column selected and takes much less time than storage.

At the initial moment of the storage regime a voltage $U < 0$ is applied to all buses Y_i (electrodes 1, Fig. 1). This voltage is nearly instantaneously distributed between capacitor C_1 and the capacitor of the parallel-connected p-n junction and the capacitor C_2. Owing to the signal and background radiation as well as heat the photo- and dark currents appear in reversely biased p-n junction, which cause discharge of junction capacitance and change the voltages across capacitors C_1 and C_2. The decrease in the voltage across the capacitor C_2 is used in this FPA as a measure of the number of photons incident upon a cell.

To read out the signals stored by the capacitors C_2 the bus of column Y_i selected is kept grounded and the feedback loops of all charge amplifiers break (Fig.1b). Upon grounding of electrode 1 of a sampled cell voltage U_1 of capacitor C_1 is applied to the p-n junction. As a result, the junction which was reversely biased during the storage becomes forward-biased due to the voltage U_1 of the order of several volts. This results in rapid discharge of capacitor C_1 through the forward-biased p-n junction and the establishment of near-zero voltage across the capacitor. Concurrently with the capacitor C_1 capacitor C_2 starts to discharge through the forward-biased p-n junction and charge amplifier or, more precisely, through capacitor C_3 in the feedback loop of the operational amplifier (Fig. 1c).

At high IR intensities or large times of storage the response of the system becomes nonlinear, namely, close to logarithmic. In other words, bright pixels of IR images will have substantially lower contrast in this case. Such feature is advantage of this array for many applications.

We developed mathematical model which describes storage and readout of photosignal as well as threshold characteristics of the proposed FPA and found optimal parameters at which FPA has limitingly high characteristics. We fabricated and experimentally studied the 64×64 format FPA and found that its storage time is more than 300 μs and for this reason BLIP regime can be realized up to 512×512 format.

FPA of such type can be fabricated in hybrid variant for which the storage time can reach the value of order of characteristic time of human eye. In this case BLIP regime can be realized even for FPA of 1024×1024 format.

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4

Dark Current in AlGaAsSb/InGaAs/AlGaAsSb QWIPs

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Introduction

Interest in material systems other than AlGaAs/GaAs for quantum well based devices have increased over the last several years to improve device performance as well as to expand the application of quantum well devices. One such promising new material system is AlGaAsSb. This material system can be lattice matched to InGaAs and InAs, producing either a Type I, Type II staggered or Type II broken band alignment as well as a larger conduction band offset than an AlGaAs/GaAs system [1]. This implies that the AlGaAsSb systems may be a good candidates for QWIPs since reducing the dark can be achieved by an increase the conduction band offset [2]. Furthermore, the operating temperature of the Sb based QWIP can be increased over the AlGaAs/GaAs QWIP as a result of the smaller dark currents. Therefore, the goal of this paper is to address the dark current in an n^+-i-n^+ AlGaAsSb Type I system lattice matched to InGaAs and InAs.

Considering that a QWIP is fabricated in an n^+-i-n^+ structure and assuming that the current exiting the quantum well is equal to the current captured by the quantum well under steady state [3], the dark current results from the contacts or n^+ regions. In this paper, the dark currents of an n^+-i-n^+ QWIP is calculated as a function of applied electric field. The calculation includes the resulting change in the electron's group velocity [4-8], the redistribution of the density of states [4-8] and the transmission coefficient due to the applied field. The electron's group velocity, the redistribution of the density of states as well as the transmission coefficient are calculated by solving Schroedinger equation by the method of the logarithmic derivative of the wavefunction through the retarded Green's function as a function of applied electric field [4-8]. The band offset of the Sb based systems is calculated by the method of Anwar et. al [1].

Theory

The dark currents arising from the n^+ regions consists of a positive z-directed and a negative z-directed current where z is perpendicular to the quantum wells. The total current is the summation of the two components where each component is calculated by integrating over all k-space as [7,8]:

$$J_{tot} = J^+ + J^- = \frac{2q}{(2\pi)^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} dk_x dk_y \left[\frac{1}{2\pi}\int f(E) v_g^{\pm}(E_z) D^{\pm}(E_z) dk_z\right] \quad (1)$$

where q is the elemental charge and k is the wavevector in the x, y and z direction, $v_g(Ez)$ is the local velocity, $D(E_z)$ is the transmission coefficient and $f(E)$ is the Fermi function at the edge of the n^+. Since the local velocity and the transmission coefficient are a function of the z-directed energy, the k_z integral is converted to an integral over energy (as well as the k_x and k_y integrals) ,E_z ,as [7,8]:

$$J_{Tot} = \frac{qm^*}{2\pi\hbar^2}\left[\begin{array}{l}\int_0^\infty dE_t \int_{0,\,kz>0}^\infty f(E)v_g^+(E_z)D^+(E_z)g_{1D}(E_z)dE_z + \\ \int_0^\infty dE_t \int_{0,\,kz<0}^\infty f(E)v_g^-(E_z)D^-(E_z)g_{1D}(E_z)dE_z\end{array}\right] \qquad (2)$$

where $g_{1D}(E_z)$ is the 1-D density of states at the edge of the n^+ regions and E_t is the energy in the transverse direction (x and y). Where the 1-D density of states is calculated as a function of position and energy in both the positive and negative directions as [4-8]:

$$g_{1d}(z,E_z) = \text{Im}\left[\frac{j8/\pi\hbar}{G^+(z,E_z) - G^-(z,E_z)}\right], \qquad (3)$$

the local group velocity in the positive and negative directions, $v_g^\pm(z,E_z) = \text{Re}\left[G^\pm(z,E_z)\right]/2$, are defined in terms of the real part of the logarithmic derivative ($G^\pm(z,E_z)$) of the wavefunction [4-8] and the transmission coefficient [4-8] is obtained from the logarithmic derivative of the wavefunction by subtracting the square of the reflection coefficient at the edge of the n^+ region as:

$$D^\pm(z_i,E_z) = 1 - \left|\frac{G^\pm(z_i,E_z) \mp G_{oi}}{G_{oi} \mp G^\pm(z_i,E_z)}\right|^2 \quad . \qquad (4)$$

Results

The quantum well infrared photodetectors investigated consist of 4 quantum well of 60 Å and 250 Å barriers in an n^+-i-n^+ structure. To verify the dark current calculations described above, a comparison between experimentally measured dark currents as reported by Lui [3] and the present theoretical calculation for an $Al_{.26}Ga_{.74}As/GaAs$ system consisting of 4 quantum well of 60 Å and 250 Å barriers in an n^+-i-n^+ structure is shown in Fig. 1 for a temperature of 82.5K. As demonstrated, the exists excellent agreement between the reported experimental results and the theoretical calculations.

In Fig. 2, the dark currents for an $In_{0.53}Ga_{0.47}As/AlGaAsSb$ QWIP are plotted as a applied electric field with temperature as a parameter. The composition of Al was varied to yield band offsets of 0.78eV and 0.848 eV for 53% In composition requiring that the

lattice matched system be type-I. As one would expect, the dark currents for the InGaAs/AlGaAsSb based QWIP is smaller by several orders of magnitude than for the AlGaAs/GaAs based QWIP. This results from the larger conduction band offset of the InGaAs/AlGaAsSb versus the AlGaAs/GaAs system. Furthermore, the smaller dark currents occurs at room temperature for the InGaAs/AlGaAsSb based QWIP unlike the AlGaAs/GaAs based system which operates at 82.5K. The dark currents for the InGaAs/AlGaAsSb based QWIP can be reduced by at least an order of magnitude by decreasing the temperature to 270 K as shown in Fig. 2.

In Fig. 3, the dark currents for an $In_{0.8}Ga_{0.2}As$/AlGaAsSb based QWIP are shown as a function of electric field. The dark currents decrease further over the 53% In composition QWIP as a result of the larger band offsets 0.99 eV for 80% In. As in the 53 % In case, with decreasing temperature a reduction in the dark currents can be achieved at times greater than an order of magnitude.

It should be noted that the dark currents for the 53% In and the 80% In were calculated using a Fermi level in the n^+ region of 0.13 eV and 0.26 eV above the conduction band. Whereas for the AlGaAs/GaAs QWIP, the Fermi level was 0.078 eV above the conduction band. This along with the low dark currents at room temperature demonstrates the advantage of the InGaAs/AlGaAsSb based QWIP over the AlGaAs/GaAs QWIP. It should also be pointed out that the AlGaAsSb/InAs system results in a band offset greater than the 80% In case further reducing the dark currents.

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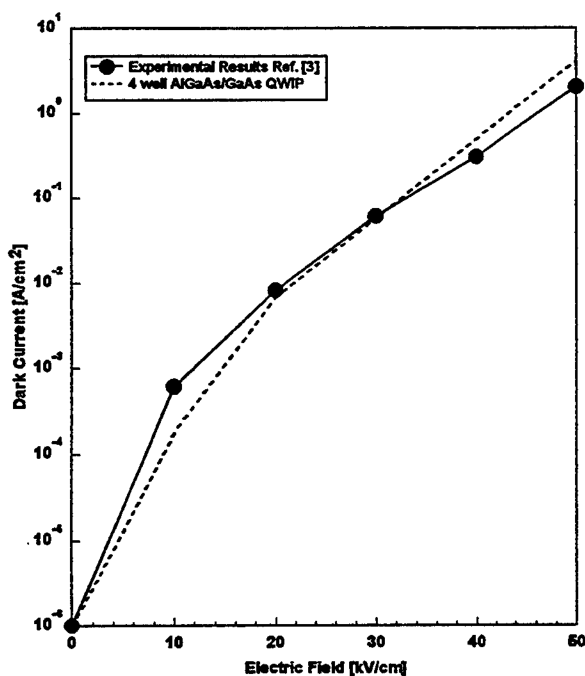

Figure 1

Comparison between the experimentally measured dark currents of Ref. [3] and the calculated dark currents of an AlGaAs/GaAs QWIP

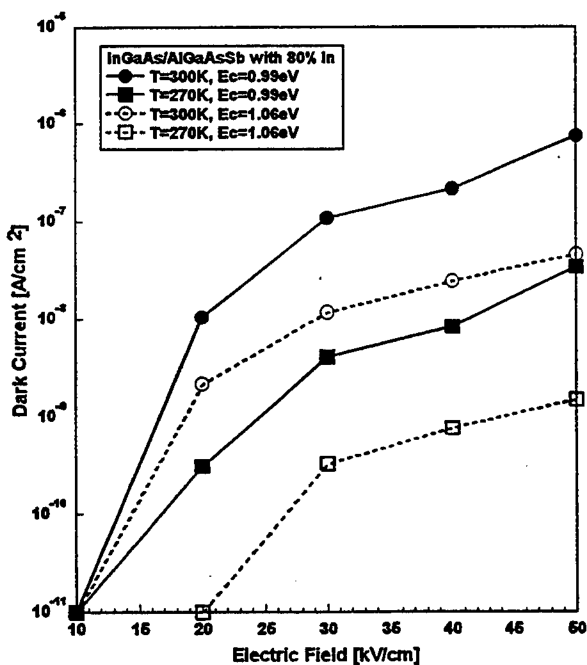

Figure 3
Dark currents of an InGaAs/AlGaAsSb QWIP with 80% In composition.

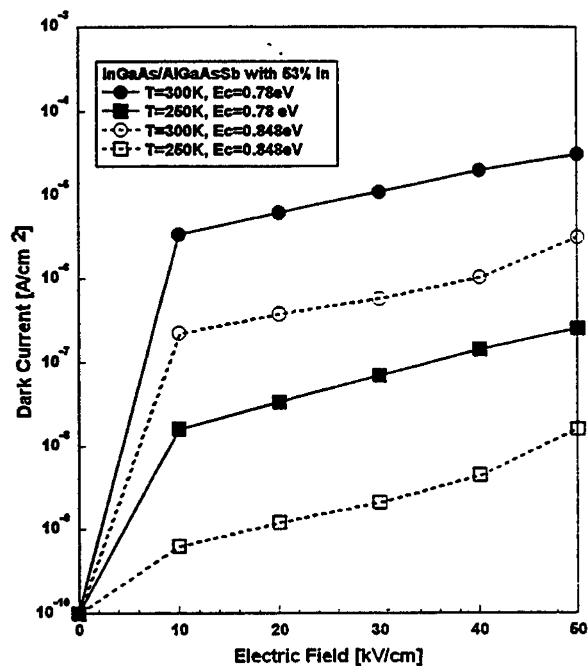

Figure 1

Dark Currents of an InGaAs/AlGaAsSb QWIP with 53 % In composition.

Terahertz Electrically Pumped Quantum Well Lasers Based on Intersubband Transitions

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Abstract: By properly engineering intersubband scatterings and subband levels, terahertz (THz) unipolar lasers can be made from multiple quantum well (MQW) structures under appropriate bias. A three-level system was designed using coupled-triple-well structures in GaAs/AlGaAs. By studying electron transport in such doped MQW structures theoretically and experimentally, relevant structural parameters, such as well widths and barrier widths, are optimized for achieving population inversion between the two upper subbands. Tunable THz spontaneous emission was observed in such structures, and the emission spectra were resolved using an external Fourier transform infrared spectrometer (FTIR). The resolved emission linewidth was less than 5 meV (1.25 THz). Evidence of population inversion was found from measuring the heights of the emission peaks corresponding to different intersubband radiative transitions. For THz emission below the longitudinal optical (LO) phonon energy, the hot electron effect and the internal lattice heating will seriously affect the device perfomance. A numerical calculation, combined with experimental characterizations, was employed to address this issue. Modifications to MQW structures were made to allow devices to possibly withstand high temperature operations ($\sim$ 200 K). In order to effectively confine the mode and greatly reduce the cavity loss, a metallic waveguide was successfully fabricated using selective-etching technique, promising the operations of THz intersubband lasers.

Coupled Monte Carlo-Electrodynamic Simulations of Nanoscale Optical Mixers

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Introduction

Optical heterodyning is a relatively old concept, first proposed for the generation of coherent microwave radiation [1]. Since the output signal is available at any desired difference frequency, photomixing can serve as a versatile process of frequency generation well into the terahertz range. This is particularly important given the lack of solid state coherent sources that can operate at fundamental frequencies in or above the GHz range. For example, while resonant tunnelling diodes [2] and other quantum well structures [3] have been proposed to operate at such high frequencies, their useful range is easily curtailed by the presence of parasitic resistances that offset the internal negative device resistance. Other alternatives such as three-wave mixing in non-linear crystals suffer from the stringent requirements of maintaining phase matching.

Interest in the optical heterodyning concept remained low for many years due to the lack of robust high-quality tunable optical sources and reproducible device structures. The reliability of optical heterodyning typically used to be poor and the output power limited to the micro-Watt range. However, with the advent of new stable, tunable lasers and the development of GaAs based technology, this picture has begun to change. Experiments have reported optical heterodyning in the Ghz and THz regimes [4-6]. Conceptually, high mobility GaAs serves as the photomixing medium, in which photocurrents at the difference frequency are produced by electron-hole pair generation from two incident lasers with a small offset frequency. The time varying photocurrents then serve as the localized sources of electromagnetic radiation. Interdigitated GaAs metal-semiconductor-metal (MSM) structures are becoming increasingly attractive as the photomixing elements due to their advantages in compatibility with planar field effect transistor technology, low voltage operation, negligible leakage currents, and capacitances that are smaller than in other vertical structures.

Almost all of the recent research on optical heterodyning has used GaAs technology with feature lengths in the micron range. However, reducing feature size down to the nanoscale dimensions can be expected to yield superior performance as a result of shorter transit times, lower capacitances, possible ballistic carrier transport, and higher electric fields. Such performance advantages of nanoscale GaAs technology, including superior bandwidth, have already been demonstrated for interdigitated MSM photodetectors [7,8]. However, the potential of nanoscale MSMs for optical heterodyning, their power output capabilities, and conversion efficiency at frequencies in the THz range have not yet been evaluated or studied. It therefore, becomes important to obtain theoretical performance predictions to gauge their utility, before initiating costly fabrication of test nanoscale GaAs MSM structures. This contribution is an effort in that direction, and presents a simulation study of nanoscale GaAs MSMs for optical mixing in the THz range.

Simulation Model

An accurate simulation model for the optical mixer response needs to treat both the semiconductor transport and the electromagnetic radiative aspects on an equal footing. In addition, the mathematical approach needs to adequately incorporate all details of the internal physics on the ultrafast time scales. The ultrafast time scales are a natural outcome of the nanoscale dimensions, the high internal fields, and the desired terahertz frequency range. Particular examples of ultrafast phenomena expected in nanoscale, laser-excited devices include: ballistic transport, picosecond carrier relaxation, and continuous intervalley transfers.

Hence, simplified drift-diffusion schemes with energy independent rate equations which have been used previously, will not suffice for an accurate representation of semiconductor transport for the present case. Another important aspect, in the context of high frequency device simulations, pertains to the relative time scales between electron relaxation processes, and the period of propagating electromagnetic waves. As these characteristic time scales approach one another, it becomes very important to incorporate the dynamic interplay between the time-dependent local electric fields and their influence on carrier transport through a continuous adjustment of carrier velocities. The standard approach of evaluating internal electric fields through Poisson's equation also becomes inappropriate for such high frequency modeling. For instance, quasi-static methods would ignore the propagation aspect, disregard the presence of a vector potential, and discount Lorentz force contributions to carrier motion arising from internal magnetic fields. A more complete treatment of the optical mixer problem, therefore, requires a solution of the full electrodynamic equations coupled with a microscopic model of semiconductor transport.

A full-wave, time-domain, finite-difference (WFTDFD) approach coupled with the Ensemble Monte Carlo scheme was developed, and used here for simulations of the optical mixer. The overall computational scheme shown in Fig. 1, is similar to a procedure used previously for simulating sub-picosecond pump-probe experiments [9]. The numerical procedure is initiated by calculating the initial, steady state electric fields within the MSM prior to external laser excitation. Electron-hole pairs are then introduced into the simulation region, in accordance to the terahertz modulations of the total input laser energy. The kinetic bipolar Monte Carlo semiconductor model, which includes all relevant carrier-phonon and carrier-carrier scattering processes, yields the spatial current densities at each time step. Details of the Monte Carlo model, its implementation, the GaAs parameters and scattering mechanisms used, have been given elsewhere [9]. A three dimensional uniform mesh was used, with spacing less than the Debye length. Periodic boundary conditions were applied along the z-direction, with the top surface being in the x-z plane at y=0, and the surface electrodes separated along the x-axis. The Monte Carlo currents served as sources of radiation, and their values were fed into the WFTDFD model for updating the electromagnetic fields. The WFTDFD scheme which solves Maxwell's equations in the time domain, has been extensively applied to a variety of electromagnetic problems [10]. For numerical stability and computational ease, Maxwell's equations were decoupled, and the electric and magnetic fields evaluated alternately in a leap-frog manner with a time step of 5×10^{-18} second. In order to simulate the infinite space surrounding the GaAs MSM structure, absorbing boundary conditions were implemented [11]. This translated into the inclusion of a 100 grid point thick perfectly matched layer (PML) completely surrounding the vacuum region and the central MSM simulation box. Allowing for a vacuum region beyond the GaAs MSM structure but within the confines of the PML, accounted for internal reflections at the GaAs-vacuum surfaces due to dielectric constant mismatch.

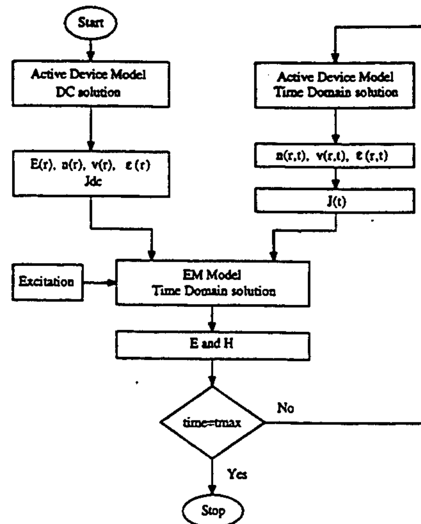

Fig. 1 Flowchart for the coupled Monte Carlo -WFTDFD simulation scheme.

Results and Discussion

Simulations of the all-optical MSM mixer have been carried out based on the coupled technique described above. The goal was to obtain quantitative predictions of the radiated electromagnetic power at the difference frequency and the conversion efficiency in the terahertz range as a function of the applied bias, modulating laser wavelength, photon flux, and device dimensions. Roughly, one expects the greatest efficiency for near-bandedge excitation based on considerations of low input energy and low carrier effective mass. However, the penetration of electric fields into nanoscale MSM structures is known to dramatically decrease with feature size. This suggests that for nanoscale structures *lower* excitation wavelengths which enhances near-surface photogeneration, might have an offsetting advantageous instead. As an initial test, computations of the radiated energy from a photoexcited MSM structure biased to 0.1 Volt, consisting of 100 nm electrodes and a 100 nm airgap spacing were carried out. This scenario yields an average field of only 10 kV/cm, and is well below the threshold limit The MSM was assumed to be illuminated by a 1.55 eV, 50 fs laser pulse with the photon flux creating an effective carrier density of 10^{16} cm^{-3}. Such a pulse represents one cycle in the optical mixing between two lasers incident on the MSM with near perfect frequency matching. Numerical results of the electric and magnetic field distributions prior to, and upon completion of the laser pulse, are shown in Fig 2. A build up of the magnetic field and the launching of an electromagnetic wave can be seen. The output power was also computed by computing the Poynting vector along the GaAs surfaces. For the 1.55 eV pulse, a net conversion efficiency of 0.13 percent was obtained at a biasing voltage of 0.1 Volt. This value is slightly higher than an experimental observation of about 0.01 per cent that has been reported for terahertz frequencies [6]. However, it is expected that by increasing the applied fields and optimizing the device dimensions and aspect ratio, higher efficiencies could be attained. Our preliminary results, therefore indicate the usefulness of nanoscale MSM structures for such high frequency power generation through optical heterodyning. A detailed analysis, and an evaluation of the optical response as a function of various input parameters will be presented at the conference.

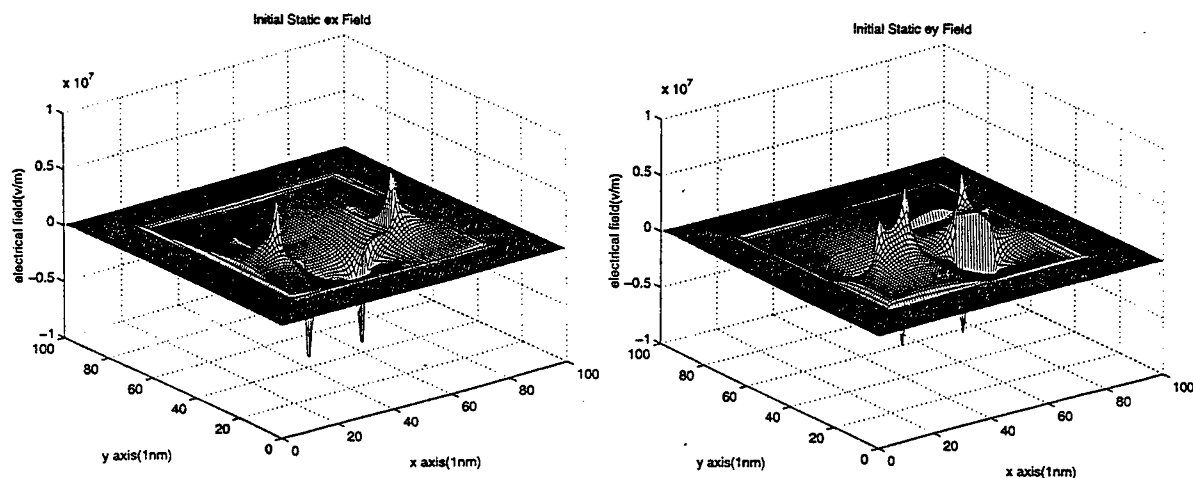

Fig. 2a Electric fields Ex and Ey in simulation region before laser excitation.

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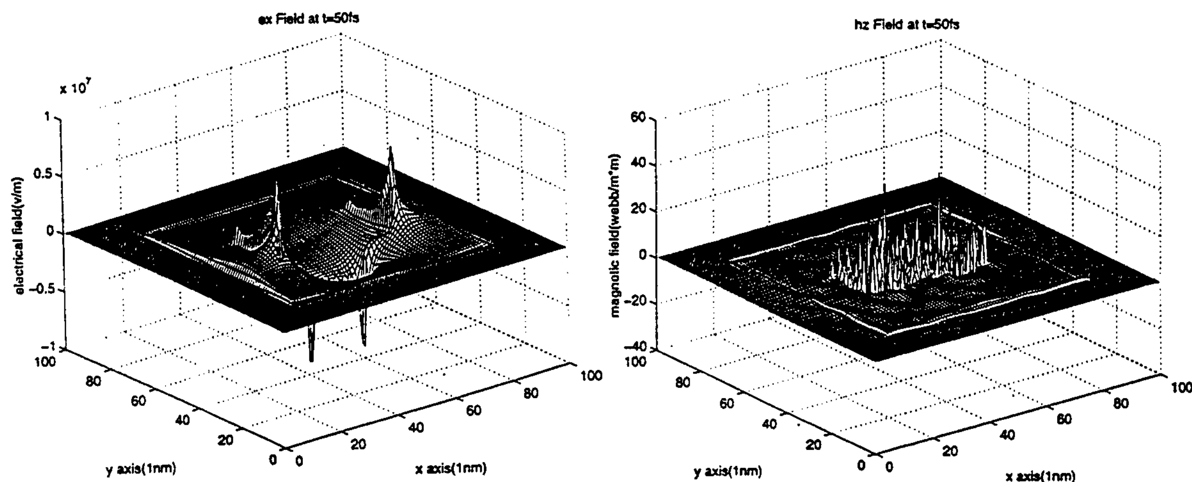

Fig. 2b Electric and magnetic field distributions at end of laser excitation pulse.

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The Performance of the Longitudinal-Field GaAs/AlGaAs Semi-Insulating Multiple Quantum Wells Photorefractive Devices

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Abstract The research results about the transient response of the longitudinal-field multiple quantum wells photorefractive devices are reported; moreover, we also study the performances of the devices in the non-degenerate four-wave mixing geometry.

1. Introduction

Since A.M. Glass et al[1] firstly demonstrated the photorefractive effects in the semi-insulating multiple quantum wells (SIMQWs) materials, the photorefractive effects and its applications of SIMQWs materials have strongly attracted people's interests. SIMQWs materials have many advantages such as fast response, high sensitivity, high spatial resolution, low switch energy and wave mixing operation in the Ramam-Nath regime. People have been successful in fabricating optical correlator[2], spatial light modulators[3] and real-time optical information processing[4] and so on.

In the longitudinal-field Stark geometry[5-9], an ac electric field is applied perpendicular to the plane of the wells, which produces the quantum confined Stark red shift and electric-field-induced broadening of exciton through the large quantum confined Stark effect (QCSE). The changes of exciton absorption coefficient are called the electroabsorption[10], which always accompanies with the changes of the refraction index, they are relevant through the Kramers-Kronig relation[5], the changes of refraction index are named the electrorefraction index. In the longitudinal-field geometry, photocarriers in the light fringes drift parallel to the direction of the applied electric field, they are trapped at the interface between the insulating cladding layer and semi-insulating electro-optical layer, these trapped charges generate the space charge field, the space charge field screens the applied electric field at the same time. Therefore, the space charge field is modulated spatially parallel to the wave vector in the plane of SIMQWs. The optical properties are also modulated through the quadratic electro-optic effects in the electro-optic layer. The devices in longitudinal-field Stark geometry must operate through transients because they have special structure. If a dc electric field is applied to the devices, the field will drop predominantly across the insulating cladding layer instead of the semi-insulating electro-optic layer. Clearly in order to introduce a field into the electro-optic layer, the field must be transient. Nolte et al[5,11] present the equivalent circuit model of the longitudinal-field potorefractive quantum well structure, and study the response of diffraction signals with the time-dependent sinusoidal voltage applied to the devices, they discuss the diffraction signals with the square pulse voltage applied to the devices by the methods of the Fourier transformation.

This paper investigates the temporal response of the electroabsorption of the longitudinal-field SIMQWs photorefractive devices to which an ac square pulse voltage is applied, and discusses the experimental results in details according to the equivalent circuit model. The performance of the devices operated in non-degenerate four-

wave mixing geometry is also investigated.

2. Results and Discussion

The GaAs/AlGaAs SIMQWs sample was prepared by the MBE at low temperature, structure is shown in figure 1. The electrodes were fabricated in both sides of photorefractive devices in order to add a perpendicular field across quantum wells. The absorption spectrum of the longitudinal-field device is measured, shown in figure 2. Its light-hole and heavy-hole exciton absorption peaks locate around 832.9 nm and 836.0 nm respectively. The dependence of the electro-absorption on wavelength of the device is shown in figure 3, while the amplitude of the applied square pulse voltage is 30 V, and its frequency is 20.6 Hz, the largest electroabsorption of the device is 2227 cm^{-1}. According to the electro-absorption experimental data, the calculated electro-refraction index versus wavelength has been given in figure 3 through the following Kramers-Kronig relation:

$$\Delta n(\lambda) = \frac{1}{2\pi^2} P \int_0^{\infty} \frac{\Delta\alpha(\lambda')d\lambda'}{\lambda^2 - \lambda'^2} \qquad (1)$$

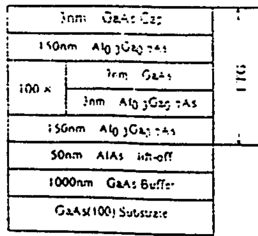

Figure 1. The structure for a longitudinal-field photorefractive SIMQWs.

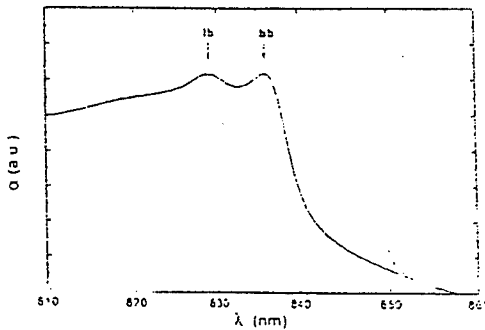

Figure 2. The absorption spectrum of the longitudinal-field device

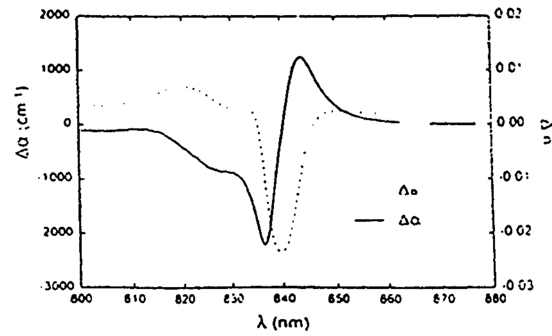

Figure 3. The curve of measured electroabsorption versus wavelength and the calculated values for Electrorefraction index versus wavelength

Besides, we have investigated the temporal response of the electroabsorption as well. In our experiment the device is applied to the single-sided square pulse voltage, a near-infrared laser incidents perpendicularly upon the surface of the device at resonant condition. The changes of the transmitted signal are detected using a silicon photodiode with 650 nm long pass filters, and recorded as a function of time on a digital storage oscilloscope. It is well-known that the changes of the electroabsorption $\Delta\alpha$ are related with the changes of the transmitted signal under the applied field ΔT through the formula :

$$\Delta\alpha = \frac{-1}{L}\ln\left(1 + \frac{\Delta T}{T}\right) \qquad (2)$$

We have measured the time-evolution of the transmitted signal under the applied field, which is equivalent that we have obtained the temporal response curve of the electroabsorption, shown in figure 4. The direction of the electro-optic layer voltage is opposite during the processes corresponding to the rise edge and fall edge of the square pulse voltage. Figure 4 shows that the electroabsorption decreases gradually during the rise and fall processes of the square pulse, but it doesn't become zero; moreover, the peak amplitude at the fall edge is a little lower than that at the rise edge. The phenomenon can be explained well according to the equivalent circuit model. If the resistance of the insulating cladding tends to

infinite in the equivalent circuit model, the electric field across the electro-optic layer E_{EO} is given by:

$$E_{EO}(t) = \frac{V}{L} \cdot \frac{C_b R_{EO}}{2} \cdot \frac{1}{\tau_{die}^{EO} + C_b R_{EO}/2} \cdot \left(u(t) \cdot e^{-\frac{t}{\tau_{die}^{EO} + C_b R_{EO}/2}} - u(t - t_0) \cdot e^{-\frac{t - t_0}{\tau_{die}^{EO} + C_b R_{EO}/2}} \right) \qquad \text{—(3)}$$

where, V is the amplitude of the applied square pulse voltage, L is the thickness of the device layer, u(t) is unit step function, and t_0 is the width of the square pulse voltage. When $t = 0$, corresponding to the rise edge of the square pulse voltage, the value of term in parentheses of formula (3) is 1, therefore, the formula (3) is a time-independent constant, squaring E_{EO}, the red shift of the exciton absorption peak $\Delta\lambda$ can be obtained, which is also a time-independent constant. Therefore, the electroabsorption is a very little constant instead of zero. When $t = t_0$ in the formula (3), corresponding to the fall edge of the square pulse voltage, the value of terms in parentheses of the formula (3) is negative and less than 1. Therefore, the amplitude of the electric field across the electro-optic layer at the rise edge is a little more than that at the fall edge, the electroabsorption peak does so.

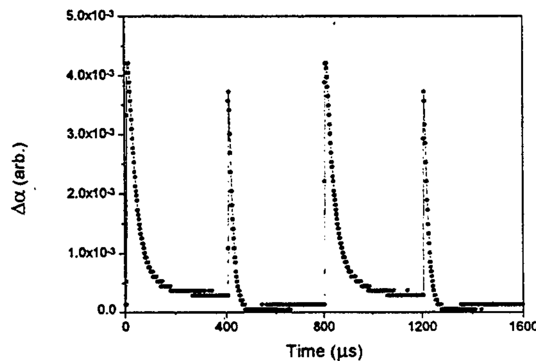

Figure 4. The temporal response of the electroabsorbtion.

The performance of longitudinal-field devices in the non-degenerate four-wave mixing geometry has also been studied.The standard single-sided square pulse voltage is applied to the device, the amplitude of the standard square pulse voltage is 30 V, at frequency of 100 Hz. As the electro-optic layer is photoconductive layer, the resistance of the light fringes is different from that of the dark fringes when write beams write the holographic grating in the device. Therefore, the time-dependent electric field of light fringes is also different from that of dark fringes in the electro-optic layer, the electric field across the electro-optic layer is modulated as well. Due to the quadratic electro-optic effects, both index and absorption gratings are time-dependent, therefore the diffraction signals vary with time. Figure 5 shows the temporal response of the measured first-order diffraction signal. The peak amplitude at the rise edge is different from that at the fall edge of the square pulse voltage, the phenomenon is very similar to the transient phenomenon of the electro-absorption.

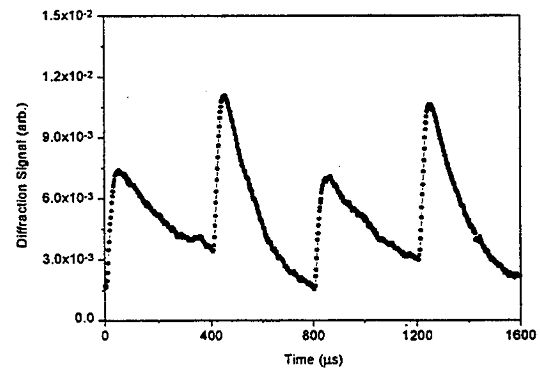

Figure 5. The temporal response of the first-order diffraction signal.

Figure 6 shows the dependence of output diffraction efficiency on wavelength of read beam, the output diffraction efficiency about 0.87% is obtained at the wavelength of

835.6 nm. Figure 7 is the dependence of output diffraction efficiency on the grating fringe. The diffraction efficiency decreases gradually with the grating fringe small. According to the following formula:

$$\eta \propto \left(\frac{1}{1+(\Lambda_c / \Lambda)^2} \right)^2 \qquad (4)$$

the theoretically simulated curve of the diffraction efficiency versus grating fringe is obtained, shown in figure 7, which is consistent with experimental curve very well.

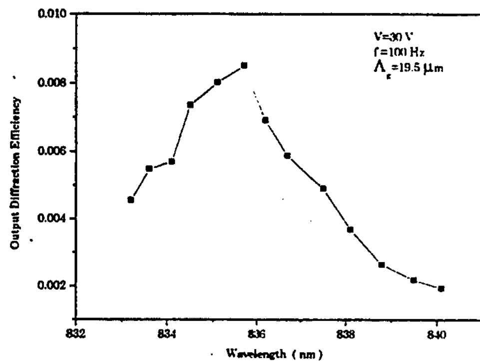

Figure 6. The dependence of the output diffraction efficiency on wavelength of read beam.

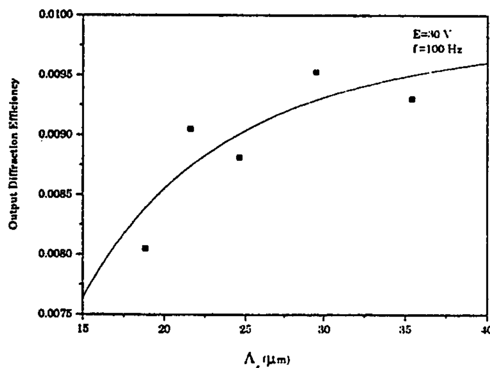

Figure 7. The dependence of output diffraction efficiency on the grating fringe spacing.

3. Conclusion

In conclusion, the transient response of the electroabsorption of the longitudinal-field SIMQWs photorefractive devices is investigated, the results can be explained very well according to the equivalent circuit model. The performance of the devices in the non-degenerate four-wave mixing geometry has been studied in details.

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Ion-Implantation Doping of Silicon Carbide

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Because of their commercial availability in bulk single crystal form, the 6H- and 4H-polytypes of SiC are gaining importance for high-power, high-temperature, and high-frequency device applications. Selective area doping is a crucial processing step in integrated circuit manufacturing. In Si technology, selective area doping is accomplished by thermal diffusion or ion-implantation. Because of the low diffusion coefficients of most impurities in SiC, ion implantation is indispensable in SiC device manufacturing. In this paper we present our results on donor, acceptor, and compensation implants in 6H-SiC.

All of the implants in this work were performed into p- or n-type epitaxial layers (with carrier concentration $\leq 2\times10^{16}$ cm^{-3}) grown on Si-faced, 4° off-axis, (1000), p or n-type ($>10^{18}$ cm^{-3}) 6H-SiC substrates. Multiple energy implants were performed at RT or at an elevated temperature (700-800 °C). The annealings were performed after encasing the samples in an amorphous SiC susceptor or SiC coated graphite susceptor to minimize Si dissociation from the implanted samples during annealing. To evaluate the thermal stability of the implant, secondary ion mass spectrometry (SIMS) measurements were performed on the annealed samples. Rutherford backscattering (RBS) channeling measurements were conducted to assess the crystal perfection qualitatively. To obtain the electrical activation of the implanted impurities, van der Pauw Hall measurements were performed on the annealed samples. Ohmic contacts to the n- and p-type layers were formed by evaporated Ni and Ti/Al alloyed at 1000 °C and 950 °C for 30s, respectively.

Nitrogen and phosphorous are both useful donors in SiC[1-6]. At 4 MeV, the N^+ and P^+ ions have a range of 2.5 μm and 2.0 μm, respectively. Because of its low atom mass the N implants were performed at both room temperature and elevated temperature (ET) yielding good activation results after annealing. Phosphorous being a heavier atom (atomic mass = 31) does not yield favorable electrical activation if the implants were performed at RT. For 15 keV-280 keV multiple energy N^+ implants, performed at RT, with a 1.36×10^{15} cm^{-2} total dose, the measured sheet carrier concentration (n_s) at RT after 1600 °C/15 min annealing is 4.1×10^{14} cm^{-2} with a carrier mobility of 46 cm^2/Vs. The N donor has an ionization energy (E_D) of ~80 meV in 6H-SiC. It is for this reason that the n_s measured does not represent the substitutional N donor concentration. By increasing the measurement temperature to 473 K we obtained an n_s of 1.1×10^{15} cm^{-3}. The n_s seems to increase further at even higher temperatures. For both RT and ET N-implants the RBS yield after annealing

coincided with that of the virgin level indicating a proper lattice recovery[6]. The SIMS measurements did not show any redistribution of N after annealing.

The 20 keV-550 keV multiple energy RT P^+-implanted SiC material with a total dose of 1.36×10^{15} cm^{-2} gave a n_s of only 6×10^{13} cm^{-2} after 1600 °C/15 min annealing. The E_D value of the P-donor is ~85 meV[4], which is close to that of N. The poor activation for RT P-implantation is due to excessive lattice damage. The RBS measurements on annealed material indicated a substantial residual damage in the material. By increasing the implantation temperature to 700 °C we measured an n_s of 7.5×10^{14} cm^{-2} and a μ of 34 cm^2/V.s at RT for 2.7×10^{15} cm^{-2} P dose. These values are comparable to that of the N-implantation. The RBS aligned yield on the annealed material nearly coincided with that of the virgin sample indicating good lattice quality. This means that for P-implantation an elevated implantation temperature needs to be used. The SIMS measurements did not show any significant redistribution of P after annealing.

Aluminum and boron are the popular acceptor dopants in SiC[7-10]. At an energy of 1 MeV the Al and B ions have a range of 0.9 μm and 1.3 μm, respectively. Aluminum is preferred over boron because it is a shallower acceptor. For multiple energy 20 keV-500 keV, 800 °C, Al-implantation with a total dose of 6.67×10^{15} cm^{-2}, we measured a RT hole concentration of ~10^{14} cm^{-2} after a 1600 °C/15 min anneal. The carrier mobility measured was 5 cm^2/V.s. The low value of the measured sheet hole concentration is due to a high acceptor ionization energy (240 meV) of Al in 6H-SiC. The Al implant is reasonably stable during annealing except for a small degree of out-diffusion at the implant tail[9]. The RBS measurements indicated some lattice recovery after annealing, but the scattering yield is higher than that of the virgin level. This means that some residual implant damage remained in the material due to the high atom mass of Al. The Al implants need to be performed at an elevated temperature in order to obtain a satisfactory dopant activation and lattice quality. For RT Al implantation both Al acceptor activation and lattice quality are very poor[7].

Boron is a lighter atom compared to Al and therefore seems more attractive for ion implantation acceptor doping. It is difficult to obtain a high hole concentration at RT using this dopant due to its higher activation energy (350 meV), compared to that of Al. We could not measure any p-type conduction at RT using B ion-implantation. The B also redistributes during high temperature annealing[5].

Compensation implants are required to achieve inter-device isolation in planar high-speed integrated circuits made of n- or p-type epitaxial layers[11-13]. They are also used for junction termination at the wafer surface which helps to increase the junction breakdown voltage[14,15]. We have used multiple energy isoelectronic C or Si ion bombardment to compensate n-type SiC and deep V ion implantations to compensate p-type SiC.

By performing multiple energy 30 keV-1.3 MeV C^+ or 30 keV-1.5 MeV Si^+ bombardments, in n-type 1 Ω-cm resistivity SiC, resistivities as high as 10^{12} Ω-cm were measured over a 1.2 μm depth. The as-implant resistivity increased with the implant dose at first and then decreased at higher doses due to hopping conduction of the carriers from one trap to another. At high doses, an excessive number of traps are created in the material, exceeding the number required to trap all the

carriers. To optimize the resistivity the excessive trap concentration needs to be decreased by high-temperature treatments. If the wafer needs to be subjected to high-temperature heat-treatments (such as ohmic contact alloying, which is usually done at 900-1000 °C in SiC) after compensation ion bombardment, the ion dose must be selected to give optimum resistivity after the heat-treatment. This means that before heat-treatment the ion bombardment should create more traps than the number of carriers in the material. If the bombardment is designed to give optimum resistivity in the as-implant material then the trap concentration will decrease during the heat-treatment giving a reduced electrical resistivity.

We have used multiple energy (15-200 keV) V-implantations to compensate a $2x10^{16}$ cm^{-3} carrier concentration p-type epitaxial layer. For 10^{18} cm^{-3} V implant concentration we measured a resistivity of 10^{13} Ω-cm after 1600 °C annealing. Unlike isoelectronic Si or C ion bombardments in n-type SiC the V-implant needs to be annealed in order to introduce compensating deep donor levels in p-type SiC. The V-implant and the compensation it creates is stable only upto 1500-1600 °C. For heat-treatments above 1600 °C the V implant out diffuses at the surface causing depletion of V and hence a reduction in compensation at the surface region. One of the limitations of V-implantation compensation is its low solid solubility limit (~$2x10^{17}$ cm^{-3}) in SiC. This means that we can compensate p-type material with <$2x10^{17}$ cm^{-3} acceptor concentration using V implantation. We do not have such a limitation in compensating n-type material using isoelectronic ion bombardment. To compensate high donor concentrations we need to introduce more traps by increasing the ion dose.

Acknowledgment

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Integrated CMOS photodiode and Trans-impedance Amplifier

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Abstract--- To study photodiodes compatible with MOSIS AMI 1.2U analog CMOS process, a chip containing 17 photodiodes with different junctions and different sizes is designed and fabricated. An integrated transimpedance amplifier for the photodiode is also designed and fabricated.

1. Introduction

The objective is to design a micro-instrument which can be used to measure the intensity of luminescence with wavelength 508nm, modulated at a frequency 250Hz. The micro-instrument consists of photodiode and trans-impedance amplifier, switched-capacitor filter, dual-slope A/D converter and serial data driver. The photodiode needed has to be high sensitivity, high linearity and low noise. An integrated tranimpedance amplifier is also needed to convert the current signal generated in the photodiode into the low-noise voltage signal with amplification in order to be processed in the down-stream stages.

There are several different pn junctions compatible with the CMOS analog process, which potentially can be used as photodiodes. We designed a prototype chip containing 17 photodiodes with different junctions and different sizes in order to study the spectral characteristics. We also designed an integrated trans-impedance amplifier in the same process.

2. Photodiodes

Basically, there are 5 different pn junctions compatible in CMOS analog process which we can use to design the prototype photodiodes. They are as follows and shown in fig.1.

a) P diffusion / N well

b) N well / P substrate

c) N diffusion / P substrate

d) P base / N well

e) N diffusion / P base (combined with P base / N well in parallel)

In photodiode design, there always exists a trade-off between the response speed and sensitivity. Although a thicker depletion region results in a better sensitivity, but also slower response speed. In our case, the optical signal is modulated at 250Hz, so the response speed is not a concern, but the sensitivity is. Among the above 5 basic pn junctions,

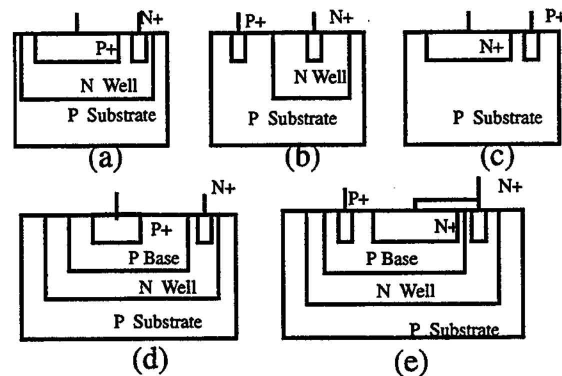

Fig.1 pn junction compatible in CMOS analog process

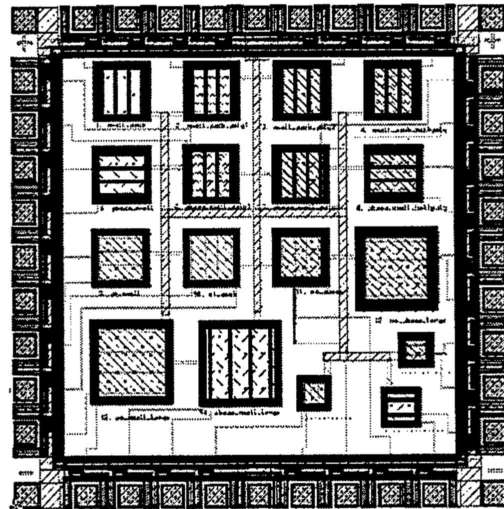

Fig 2 photodiode chip layout

we expect that N well / P substrate junction has the biggest quantum efficiency, but it will suffer from substrate noise. Additionally, the substrate is always tied to VSS, so it cannot work in the photovoltaic mode in which we expect our photodiode will be used. The next best quantum efficiency is expected from P base / N well which can work in

the photovoltaic mode as well. We can get an even better quantum efficiency if we combine the P base / N well junction with N diffusion / P base junction in parallel as shown in fig.1e.

Si photodiodes have an optical response with the sensitivity peak at about 800nm wavelength. The Poly-Si/SiO_2 can be used to alter the optical response characteristic, probably because of thin film interference.[4] We will try to move the response peak toward shorter wavelength by this means. Among the 5 configurations shown in fig.1, only the N well / P substrate junction and P base / N well junction can be covered with Poly-Si. For the above, we designed four photodiodes including uncovered, covered with Poly1, covered with poly2 and covered with both of poly1 and poly2.

Fig.2 shows the designed prototype photodetector chip with 17 photodiodes. It includes all five basic pn junction photodiodes shown in fig.1 with different sizes from 100um x 100um to 300um x 300um and with options of covering.

In the photodiode design, in order to isolate each photodiode from cross-talk in the substrate, a guard ring connected to VSS is used around each photodetector. For the structure of each photodiode, we use a ring similar to a guard ring for the outer pin and parallel stripes for the inner pin, and we use as many contacts as possible on them in order to get good carrier collection efficiency.

3. Photodiode Amplifier

The photodiode trans-impedance amplifier is to convert the photodiode current signal into a voltage signal with amplification. The photodiode amplifier is shown in fig.3. The I-V relation can be expressed as $V_o=RI_S$. The gain of the amplifier is determined by R, which is called trans-impedance in this case. For an ideal OP-AMP with infinite gain, the voltage between the negative and positive inputs, also across the photodiode, is zero. Thus the photodiode works in photovoltaic mode. This circuit has the following features:

a) This circuit has high bandwidth. The photodiode shunt parasitic capacitor, which is about 1~10pF in our case, does not affect the bandwidth because it does not shunt any current when the voltage across it is always zero.

b) This Circuit has high linearity. The non-linearity of the photocurrent does not come into play because the voltage is always zero if the OP-AMP is ideal.

c) Low dark current and low noise. The dark current of the photodiode is small because the voltage across it is zero. The shot noise proportional to the current is also small.

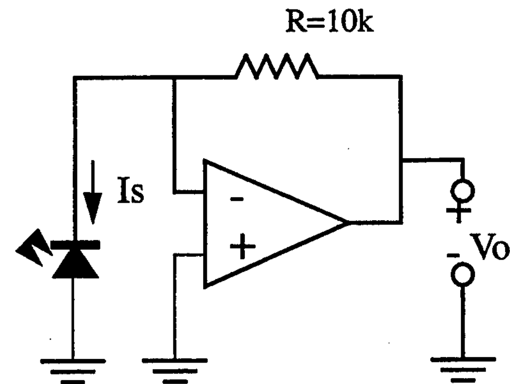

Fig.3 Transimpedence Amplifier

Although photovoltaic mode has advantages, it has a slow response time because the photo-generated carrier does not move at the saturation speed when zero-biased. However, the speed is not a concern in our case.

The 10k resistor is implemented with poly-silicon. The OP-AMP we use is originally from the Oak Ridge National Laboratory with some alteration in the transistor sizing according to 1.2um AMI parameter. The schematic is shown in fig.4 and the layout is shown in fig.5. It consists of a differential input, a level shift stage and an output stage with amplification. The simulation result shows that it has 110dB open loop gain, 40MHz unit gain frequency.

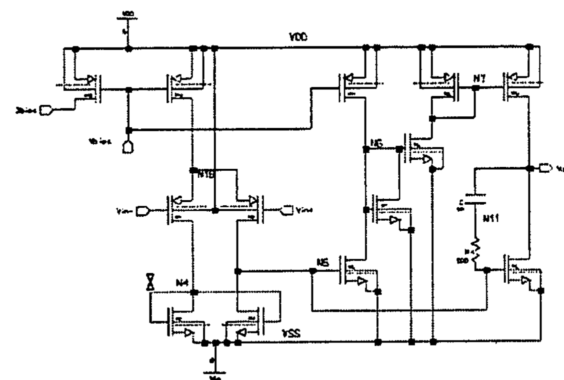

Fig.4 OP-AMP Schematic

4. Summary

This paper presents a prototype photodiode chip and an integrated photodiode trans-impedance amplifier. Both of them are submitted to 1.2u AMI process. Our presentation will focus on design and testing results for these integrated photodiodes.

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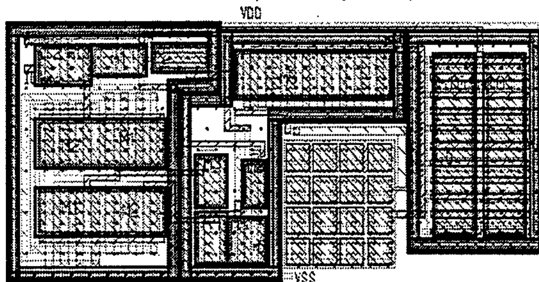

Fig.5 OP-AMP Layout

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Far Infrared Spectroscopy of Strained MQW Ge/GeSi Heterostructures

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1.0 Introduction

Recently there has been considerable interest in studies of strained heterostructures on the basis of Ge, Si and GeSi alloys. The built-in deformation arising from mismatch of lattice periods of Ge and Si opens up new possibilities for band engineering. The p-type heterostructures seems to be more promising because the deformation lifts the valence band degeneracy thus providing holes of low mass in quantum wells (QWs). In the "Ge-like" Ge/GeSi heterostructures QWs for holes are realized in pure Ge layers where high value of two-dimensional (2D) hole mobility can be obtained. This fact and the possibility of band engineering make the strained Ge/GeSi heterostructures a promising material for achieving the population inversions and the generation of far infrared (FIR) emission in strong electric and magnetic fields similar to those in bulk p-Ge [1]. At last the deformation and the confinement significantly modify spectra of shallow impurities in QWs in Ge/GeSi heterostructures thus opening new possibilities for design of photoelectric detectors for long wavelength end of FIR range.

The paper is devoted to the investigation of the strained multi-quantum-well (MQW) $Ge/Ge_{1-x}Si_x$ heterostructures by FIR spectroscopy technique that is known to be a powerful mean to study energy spectra of charge carriers and to reveal hot carrier effects. $Ge/Ge_{1-x}Si_x$ heterostructures ($0.07 \le x \le 0.15$, $d_{QW} = 130 \div 800$ Å, $d_{GeSi} \approx 200$ Å, $n_{QW} = 6 \div 243$) were grown by CVD method on the Ge (111) substrate. Number of periods n_{QW} was large enough to exceed the critical value of HS thickness and to provide the relaxation of the strains between the heterostructure and the substrate. In this case Ge layers undergo biaxial compression in the plane of the heterostructure. If number of periods was insufficient to provide the deformation of the Ge layers the buffer layer $Ge_{1-y}Si_y$ has been grown between Ge substrate and the heterostructure. The deformation of Ge layers may be represented as a result of the hydrostatic compression and the uniaxial tension P_{equiv} along the heterostructure axis. The latter lowers the crystal symmetry and results in decoupling of the light and heavy hole subbands.

2.0. Far IR Magnetospectroscopy of Free Holes in Ge/GeSi Heterostructures

2.1 Cyclotron Resonance in Low Magnetic Fields

Cyclotron resonance (CR) was investigated in both undoped and selectively doped with boron $Ge/Ge_{1-x}Si_x$ in millimeter and submillimeter wavelength range. Earlier [2] in undoped samples CR line of 2D holes of low mass was observed (Figure 1, bold line). The halfwidth of the CR line corresponds to the high 2D hole mobility $\mu \ge 10^5 cm^2/V \cdot s$. Calculated hole energy spectrum in QW is shown in Figure 2. The pronounced nonparabolicity of energy-momentum law is clearly seen. The calculated mass value at the bottom of lowest subband m_c=0.06m_0 is in a good agreement with the observed cyclotron

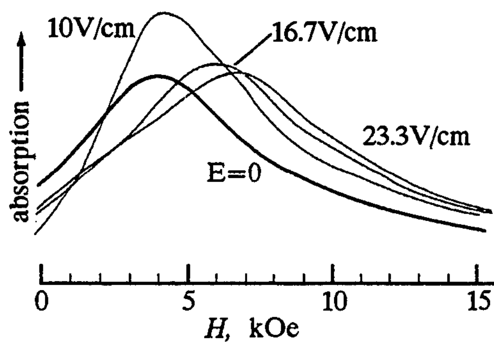

FIGURE 1.CR spectra of photoexcited holes in the undoped $Ge/Ge_{0.12}Si_{0.88}$ heterostructure #306 (d_{QW}=200 Å, d_{GeSi}=260 Å, P_{equiv}=3.6 kbar) in d.c. electric fields; λ=2.11 mm, T=4.2K.

mass. In doped samples a remarkable increase of the 2D hole effective mass with concentration (up to $m_c=0.09m_0$ at $p_s=2\cdot10^{11}$ cm^{-2} and $m_c=0.20m_0$ at $p_s=7\cdot10^{11}$ cm^{-2}) was revealed resulted from the above nonparabolicity of the energy-momentum law. The observed mass values coincide with the effective mass values calculated at the corresponding Fermi energies. The hole scattering rate also increases in the doped samples up to $\upsilon \approx 1\div1.5$ THz in comparison with that in the undoped ones ($\upsilon\approx0.3$ THz).

2.2. CR and Intersubband Absorption in Quantizing Magnetic Fields

FIR absorption spectra of three selectively doped $Ge/Ge_{1-x}Si_x$ heterostructures were investigated in quantizing magnetic fields up to 14 T. The line positions versus the magnetic field are summarized in Figure 3. The positions of the lines 1, 2 and 4 are in a good agreement with

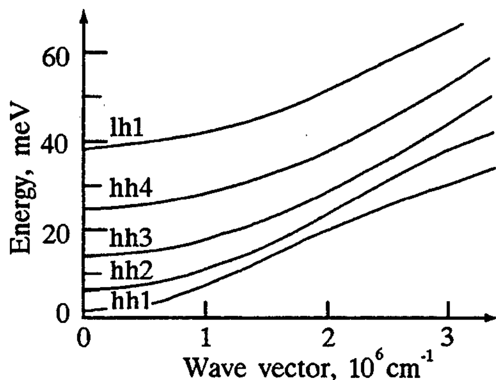

FIGURE 2. Calculated 2D hole energy spectrum in the heterostructure #306

calculated at B = 0 energy gaps between the 1st and the 2nd, 3rd and 4th heavy holes subbands correspondingly. We did not succeed to resolve intersubband transitions at B = 0 because of strong dispersion of energy gaps. In quantizing magnetic fields hole states in QW become zero-dimensional thus resulting in the resonant intersubband transitions. The transitions occur between lowest Landau levels belonging to the different subbands. These levels are not coupled with the other Landau levels and exhibit linearly shift with field with one and the same slope. Thus line positions are independent on the field. The observed shift of line 4 with field can be explained by superposition of hh1→hh4 transition and hh1→lh1 transition to the 1st light hole subband that is closely-spaced to hh4. The lines 3 and 3' shift linearly with field with nearly constant slope. The slope of line 3 corresponds to m_c =(0.08÷0.09)m_0, i.e. the "classical" cyclotron mass value at Fermi energy in these samples. The fact is striking since the hole subbands are highly nonparabolic (Figure 2); it indicates the existence of weakly interacting Landau levels that was confirmed by calculations [3]. We associate the lines 3 and 3' with the CR transitions, i.e. transitions within hh1 subband from the two lowest populated Landau levels. In fields $B \geq 11$ T only one level is populated and line 3' disap-

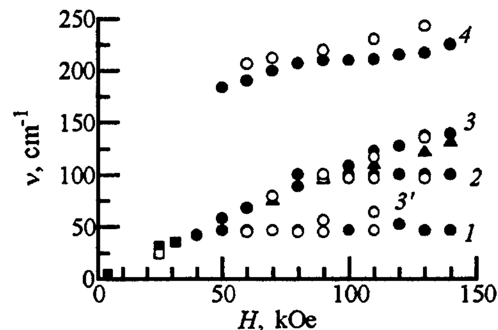

FIGURE 3. Spectral positions of the absorption lines versus magnetic fields of the samples #123 (•,■; x=0.07, $d_{Ge}\approx$ 190 Å, P_{equiv} = 3.6 kbar, n_{QW}=15, $p_s=2.4\cdot10^{11}$ cm^{-2}); #125 (o, □ ;x=0.08, d_{Ge}=180 Å, P_{equiv}=3.6 kbar, n_{QW}=36, $p_s=2.7\cdot10^{11}$ cm^{-2}); #374 (Δ; x=0.09, d_{Ge}=180 Å, P_{equiv}=1.5 kbar, n_{QW}=6, p_s =$2.9\cdot10^{11}$ cm^{-2})

pears (Figure 3).

2.3 Hot Hole Effects

The hole heating in MQW $Ge/Ge_{1-x}Si_x$ heterostructures was investigated by CR technique in undoped samples in d.c. and pulsed electric fields. The electric voltage was applied to the sample via alloyed ohmic contacts deposited on the surface of the heterostructures. CR spectra of photoexcited holes in d.c. fields are presented in Figure 1. Application of d.c. fields about few V/cm results in the remarkable shift of CR line to higher magnetic fields ($m_c \approx 0.12 m_0$ at $E \approx 20$ V/cm). The shift of the CR line is evidently stipulated with the carrier heating and with the strong nonparabolicity of the energy-momentum law. In higher electric fields the CR was studied using the pulsed technique (Figure 4). In the latter case the holes were excited at the impact ionization of residual shallow acceptors in the heterostructure thus modulating the microwave absorption in the sample. In strong electric fields the effective mass increases up to an enormous value ($m_c \approx 0.3 m_0$ at $E \approx 300$ V/cm) that corresponds to the hole heating up to $T_e \geq 200$ K. The latter proves the realization of the streaming motion of the carriers and indicates the possibility of the population inversions of 2D holes in **E** ⊥**H** fields just similar to those in bulk p-Ge [1].

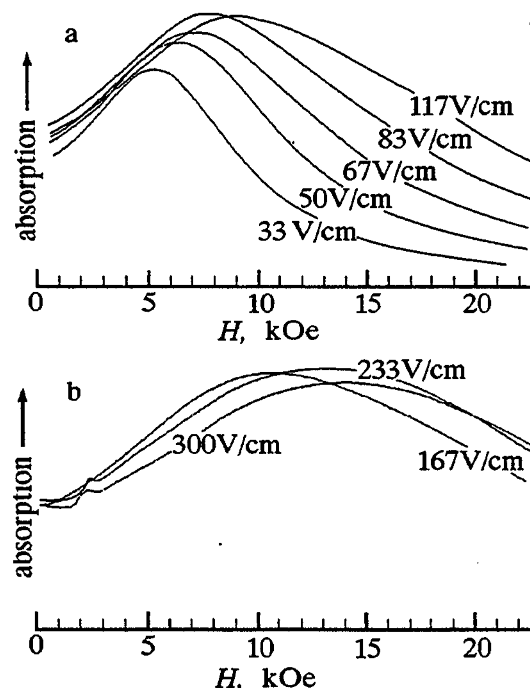

FIGURE 4. Hole CR spectra in undoped sample #306 in pulsed electric fields.

3.0 Shallow Acceptors in Strained MQW Ge/GeSi Heterostructures

FIR photoconductivity (PC) (λ = 100-600 μm) in both the undoped samples with residual shallow acceptors ($N_a \approx 3 \cdot 10^{14}$ cm^{-3}) and in the structures with boron doped quantum wells was investigated (Figure 5). The spectral features associated with confined acceptors were revealed. The PC spectra of the heterostructures lay in the long-wavelength end of the FIR range unlike the spectrum of shallow acceptors in bulk p-Ge with the maximum response at $\nu \approx 100$ cm^{-1} (see, for example, [4]). As it was already mentioned the in-plane hole mass ($m_\perp$=0.053m_0) [5] becomes smaller than the heavy hole mass in unstrained bulk Ge (m_{hh} = 0.35m_0) due to the built-in deformation resulting in the decrease of the acceptor binding energy. The study of the magnetic field effects allows to classify the observed transitions. Since light and heavy hole subbands are decoupled shallow acceptors in strained $Ge/Ge_{1-x}Si_x$ heterostructures may be treated using anisotropic hydrogen-like model just as shallow donors in Ge or Si. As it is seen from Figure 5 magnetic field splits the intensive band at $\nu \approx 25$-40 cm^{-1} into two lines. The most intensive one (as well as the weaker line at $\nu \approx 56$ cm^{-1} at $B = 0$) shifts linearly with the field with the slope corresponding to the cyclotron mass of 2D holes while the position of the second line is almost independent on the field. According to [6] the spectral band $\nu \approx 25$-40 cm^{-1} may be associated with $1S \rightarrow 2P_\pm$ transition which splits into $1S \rightarrow 2P_+$ line tuned by the field and "field-independent" $1S \rightarrow 2P_-$ line. The line at $\nu \approx 56$ cm^{-1} seems to be associated with $1S \rightarrow 3P_\pm$ and to higher P levels transitions.

The peak sensitivity of the structure #306 as photoelectric detector of the long-wavelength end

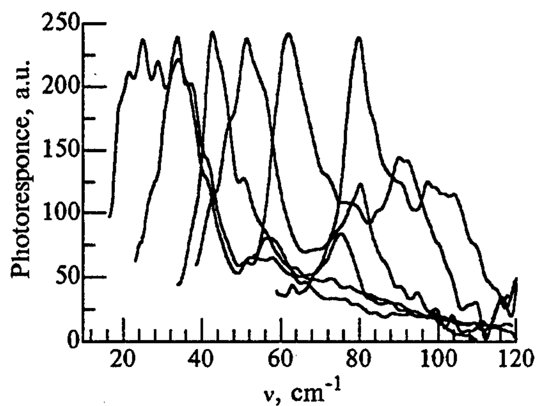

FIGURE 5. FIR photoconductivity spectra of the sample #306 in magnetic fields H||[111] at *T*=4.2K. *H*, kOe: 1 - 0, 2 - 20, 3 - 40, 4- 50.

of the FIR region measured using black body source proved to be high enough $S = 10^4$ V/W thus opening the possibility of its spectroscopy applications.

4.0 Summary

Strained MQW $Ge/Ge_{1-x}Si_x$ heterostructures were investigated by far IR spectroscopy. CR study revealed the strong nonparabolicity of energy-momentum law of 2D holes in the QWs and streaming motion of hot holes in strong electric fields **E**⊥**H**. In strong magnetic fields intersubband transitions were observed for the first time. Spectra of far IR photoconductivity of shallow acceptors in QWs in strained MQW $Ge/Ge_{1-x}Si_x$ heterostructures were studied and possibility of the structure applications as photoelectric detectors for long wavelength end of far IR range were demonstrated.

5.0 Acknowledgments

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Spatially resolved photoresponse of relaxed GeSi films studied at varying temperatures and with linearly polarized light

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Abstract. We use a near-field scanning optical microscope (NSOM) to perform local optical beam induced current and photovoltage measurements on strain-relaxed GeSi films on Si substrates. Topographic and near-field images are acquired simultaneously, enabling us to correlate topographic features and electrical activities of near surface defects. NSOM experiments using linearly polarized light reveal strain field variations associated with threading dislocations as well as with the cross-hatch patterns. Recently we have developed a new instrument to perform experiments in vacuum at temperatures from 300K to 14K. Preliminary data from this instrument shows a decrease in defect electrical activity with decreasing temperature.

1. Introduction

With advances in optoelectronics the need to better characterize submicron devices individually and to study single crystallographic defects is ever greater. While optical microscopes are the most valuable instruments in scientific laboratories, the diffraction-limited resolution of far field optics has prevented us from probing optical and optoelectronic properties of materials and devices at the nanometer scale. The invention of the near-field scanning optical microscope (NSOM) [1, 2] has made it practical to embark on such studies.

Because the sizes of individual crystallographic defects are much smaller than the diffraction limit of visible light, defect characterization has been limited until now to electron microscopy [3]. Using the NSOM aperture as a local light source, we performed near-field optical beam induced current (NOBIC)) measurements to study threading dislocation defects on strain relaxed GeSi films with resolution comparable to what was obtained via electron beam induced current (EBIC) [4]. While scanning force microscopy (SFM) has sub-angstrom sensitivity in detecting topographic changes and EBIC directly probes local electrical properties, NSOM uniquely provides the capability to simultaneously study surface morphology and photoresponse of the same defect non-destructively. In this abstract, we show that carrier generation in GeSi films has a dependence on the direction of the linearly polarized NSOM light, providing us with a tool to study variations in surface strain fields. We also show that NOBIC can be measured at low temperatures to examine the temperature dependence of electrically active defects in the films.

2. Materials and Methods

2.1. Samples

Relaxed GeSi films are used to fabricate Si (Ge) heterojunctions with high 2D electron (hole) gas mobility [5] and to integrate GaAs and InGaP light emitting diodes on Si [6]. The strained-relaxed GeSi samples were grown on (001) Si substrates by molecular beam epitaxy at temperatures ~ 800 to 900 °C. Their growth details and physical properties were

reported in Refs. 6 and 7. The films are completely strain relaxed, exhibiting bulk Ge_xSi_{1-x} optical properties [7]. The threading dislocations inherent in these films are carrier recombination centers so they are detrimental to any optoelectronic devices fabricated on these samples. Therefore, their density is kept as low as possible. Typically, these graded films have threading dislocation densities $\leq 5 \times 10^6$ cm^{-2}, as determined with EBIC [10].

2.2. Near-field Scanning Optical Microscopy (NSOM)

Since diffraction is a far-field phenomenon, optical resolution can be greatly improved by working in the near field. The ultrahigh resolution in near-field imaging arises because the evanescent modes have large wavevector components parallel to the sample surface. Since these waves are non-propagating, the sample must be placed near the subwavelength aperture. The spatial extent of these evanescent waves is approximately the aperture size, $2R$; thus, the resolution of an NSOM is $2R \ll \lambda$, higher than the diffraction limit.

The NSOM tips are tapered single mode optical fibers made by pulling while heating the fibers with a CO_2 laser. The subwavelength apertures are defined by coating the sides of the tapered fiber with Al. The typical tips used in the experiment had ~ 150 nm apertures and far-field optical throughput of ~ 5×10^{-5}. In the near-field experiment, it is critical to regulate the tip-sample separation. Our NSOM setup includes a non-optical feedback mechanism [8].

3. Near-field Optical Induced Current (NOBIC) Experiment

In this experiment, we photo-excite the GeSi samples with light from the NSOM tips and measure the spatial variations of the photoresponse as the sample is scanned beneath the tip at a regulated vertical distance. The laser source was a modulated diode laser of 670 nm wavelength. The samples have built-in *p-n* junctions parallel to the film surface. Excess current due to the photo-excited carriers is detected using a current preamplifier and lock-in amplifier. This experiment can also be done for photovoltage. As the tip moved across the sample, topographic and NOBIC images were accumulated simultaneously.

The small NSOM aperture limits the excitation volume, resulting in high spatial resolution. As the tip is brought into the near-field zone of the surface, the optical beam induced current signal increases by a factor of 2 to 3 due to the contribution of evanescent modes. Near electrically active defects, both traps and recombination centers, photoresponse should be lower than in defect-free regions. In these samples, the most prevalent electrically active defects are threading dislocations, which are expected to show up as dark spots in NOBIC images, similarly to those in EBIC images. By correlating the changes in the NOBIC images with features in the topographic images, we can learn about the electrical activities of near surface defects.

4. Probing Surface Strain Fields with NOBIC

In the previous studies, enhanced NOBIC signals were reported near the recombination regions of threading dislocations [9,10]. Furthermore, the cross-hatch patterns show a weak contrast in both EBIC and NOBIC images, the origin of which was previously not well understood. We performed polarized NOBIC experiments on these samples. In this experiment, NOBIC images at the same sample position were taken using linearly polarized NSOM light at orthogonal orientations. Fig. 1 shows the results of polarized NOBIC images near a threading dislocation: (a) topographic, (b) and (c) NOBIC images taken with linearly polarized light oriented at -45° and +45° respectively, and (d) NOBIC image taken with equal ±45° linear polarization components. It is clear from Fig. 1(b-d) that the dark spot that corresponds to shorter carrier lifetime in the dislocation does not change with polarization direction. However, the bright spots are observed along the polarization directions only. Since the orientation of the polarization axis is the only change between

Fig. 1(b) and (c), the differences in the two NOBIC images cannot be the result of a topographic effect, or of carrier diffusion and/or recombination. The differences must arise from differential carrier generation most likely due to anisotropic absorption. A similar polarization dependence for the cross-hatch contrast has also been observed. One possible cause for such anisotropic absorption is the variations in surface strain fields associated with the underlying misfit dislocation network and the threading dislocations. Strain affects local electronic structure. The reduction in bandgap (deformation potential) depends on the direction of strains. Hence the absorption of light is no longer isotropic in the sample plane.

5. Variable Temperature NSOM

Recent work on these samples has focused upon examining the temperature dependence of the electrically active defects. We have developed an NSOM which works in high vacuum (5×10^{-6} Torr) and is attached by thermally conductive braid to a continuous flow cryostat (custom Oxford Inst. Microstat). This assembly allows us to do near-field examinations of samples at any temperature from 300 to 14K. We have used this microscope to examine the dependence upon temperature of the electrical activity of threading dislocations similar to that shown in Fig. 1 and also on the overall near-field photoresponse. Our initial work here shows that the percent change of signal due to a defect decreases by 2/3 over the full temperature range while the overall response is similar at all temperatures.

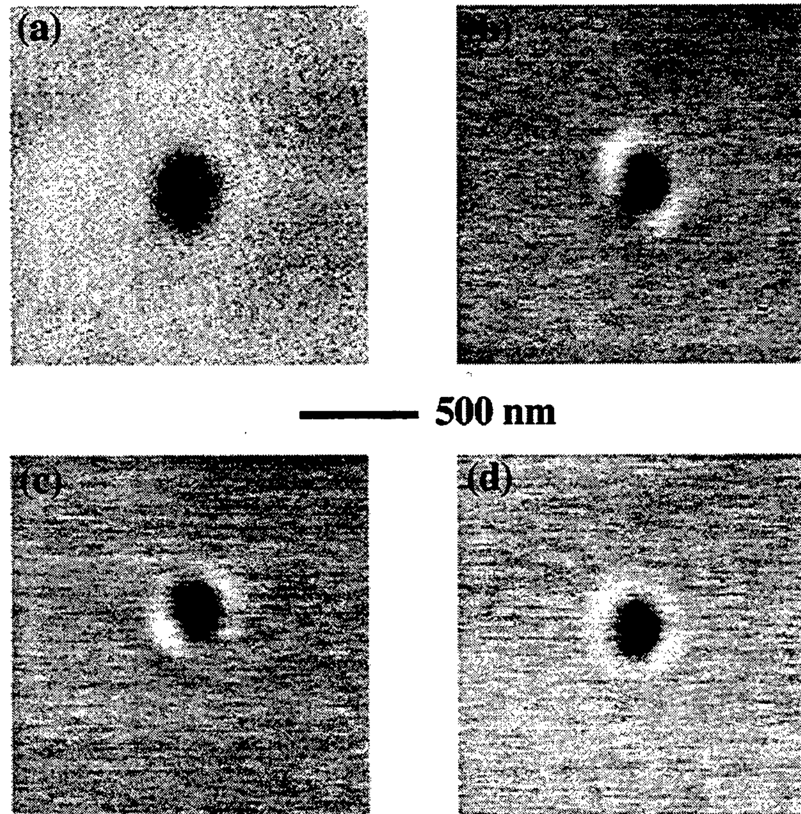

Fig. 1 1.5 x 1.5 μm^2 (a) topographic and (b,c,d) NOBIC images of an isolated threading dislocation. All NOBIC images were taken using polarized NSOM light, but with linear polarization direction at (b) -45°, (c) +45° with respect to horizontal, and (d) mixed polarization with equal ±45° components.

6. Summary

We have used two new NSOM techniques to further probe the electrical activities of near surface defects on relaxed GeSi films. The images are formed by performing optical beam induced current measurements as the tip moves with respect to the sample. The advantages of NSOM over other more commonly used techniques come from the simultaneous measurements of topographic changes and optical properties. The high resolution demonstrated in this paper arises from the small size of the NSOM aperture. NOBIC experiments with linearly polarized NSOM light show that NOBIC could be used as a new technique to map out surface strain field variations. Recent work at low temperatures shows that a NSOM can also be used to probe variation in the spatial extent and magnitude of surface defects as a function of temperature.

7. Acknowledgments

We thank E. A. Fitzgerald, Y. H. Xie, and P. J. Silverman for the GeSi samples. This work is supported by funding from NSF. J. W. P. H. acknowledges a Sloan Research Fellowship.

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Inverter Circuits with Si/SiGe n-type MODFETs

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1 Introduction

Modern consumer electronics require the development of novel Si-based high-speed transistors and integrated circuits with low noise, improved current gain and reduced power consumption operating at frequencies in the GHz range. Besides the traditional scaling of Si CMOS circuits, novel Si/SiGe heterostructure field-effect transistors (HFETs) have emerged as promising candidates for high-speed digital circuits design [1,2]. Recently, very high cut-off frequencies f_t and f_{max} obtained from small-signal S-parameter measurements of discrete transistors have been reported [3-5]. In this contribution, large-signal measurements of Si/SiGe MODFET inverter circuits with delay times from 70 ps down to 25 ps are reported for the first time.

Table 1: Layer sequence of the depletion mode Si/SiGe HFET

Layer Sequence	Depletion FET C1614
cap	5 nm Si undoped
cap spacer	10 nm $SiGe_{40}$ undoped
frontside doping	4 nm $SiGe_{40}$ Sb $1.5 \cdot 10^{19}$ cm^{-3}
spacer	3 nm $SiGe_{40}$ undoped
channel	9 nm Si undoped
back spacer	3 nm $SiGe_{40}$ undoped
backside doping	4 nm $SiGe_{40}$ Sb $8 \cdot 10^{18}$ cm^{-3}
graded buffer	500 nm $SiGe_{40}$ undoped 2μm $SiGe_{0\rightarrow 40}$ 300 nm Si
substrate	p^- Si, >1000 Ωcm

2 Technology

The heterostructure was grown by molecular beam epitaxy (MBE). The layer sequence consists of a relaxed SiGe graded buffer on a p^--Si substrate (1000 Ωcm) followed by an additional Sb-doped SiGe backside doping layer, an undoped spacer, a strained Si quantum well serving as the 2DEG channel, a SiGe spacer, an Sb-doped layer, an undoped SiGe cap spacer and a thin Si cap layer (see tab. 1).
Hall measurements have shown high electron mobilities (μ=1190 cm^2/Vs) and elevated sheet carrier densities ($n_s = 4.4 \cdot 10^{12}$ cm^{-2}) at room temperature. Mesa-isolated heterodevices with Ohmic contacts defined by phosphorous implantation, Rapid Thermal Annealing at 625 °C in N_2, Ti/Pt/Au/Pt/Ti (metal I) evaporation and subsequent lift-off (contact resistances $5 \cdot 10^{-7}$ Ωcm^2) have been fabricated. PtAu T-shaped Schottky gates with footprints down to 150 nm, were patterned by e-beam lithography using a three layer resist system (see fig. 1). The gate was asymmetrically positioned at a source-gate distance d_{SG} of 500 and 200 nm, respectively, to achieve low series resistances R_S down to 0.2 Ωmm. The gate-drain distances d_{GD} were 1.0 and 1.3 μm, respectively. For interconnects a 300 nm thick passivation oxide was sputter-deposited. Contact holes have been etched in a $CHF_3/CF_4/He$ plasma process at 560W. An additional thick Ti/Pt/Au top metallization (metal II) for interconnects and pads was structured by lift-off. Control devices and test structures for the extraction of parasitic elements have also been implemented in the chip layout.

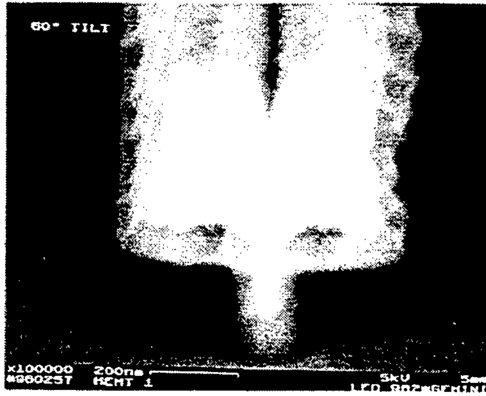

Figure 1: 150 nm T-Gate fabricated in a three layer resist e-beam process

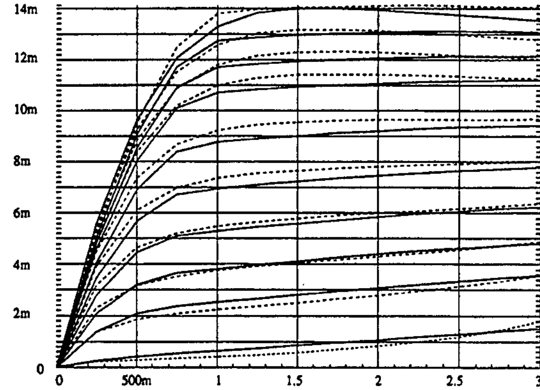

Figure 2: Measured (dashed line) and simulated (solid line) drain current vs. drain-source voltage at different gate source voltages [-1.1 V, -0.72 V, -0.53 V, -0.34 V, -0.15 V, 0.04 V, 0.23 V, 0.325 V, 0.42 V, 0.515 V].

3 Device Performance

N-type Si/SiGe depletion MODFETs with varying gate lengths L from 150 nm to 1 μm and gate widths W from 5 μm to 1000 μm were fabricated. The measured drain current vs. drain-source voltage for a Si/SiGe-MODFET (L= 150 nm, W= 50μm) with high saturation currents above 250 mA/mm is shown in fig. 2. The maximum extrinsic transconductance is 200 mS/mm (d_{SG} = 0.5μm) and 280 mS/mm (d_{SG} = 0.2μm) (see fig. 3). Measurements show extrinsic transit frequencies f_t of 16 GHz (d_{SG} = 0.5μm) and 40 GHz (d_{SG} = 0.2μm) (see fig. 4) and extrinsic maximum oscillation frequencies f_{max} of 45 GHz (d_{SG} = 0.5μm) and 80 GHz (d_{SG} = 0.2μm), all for 150 nm gate length. For a L=500 nm device, a f_t of 11 GHz was found. Table 2 shows the extracted capacitances from S-parameter measurements between 100 MHz and 40 GHz.

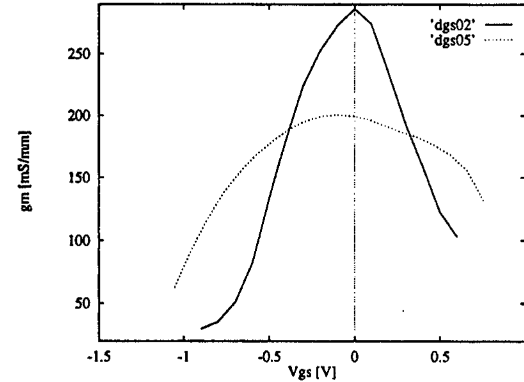

Figure 3: Extrinsic transconductance g_m versus gate-source voltage V_{gs} for d_{sg} = 200 nm (solid line) and d_{sg} = 500 nm (dotted line).

Table 2: Extracted gate-source, gate-drain and drain-source capacitance (C_{gs}, C_{gd} and C_{ds}), threshold voltage V_{th0} and pad capacitances (PadC_{gs}, PadC_{gd} and PadC_{ds}).

C_{gs}	105 fF
C_{gd}	12fF
C_{ds}	13 fF
Pad C_{gs}	5fF
Pad C_{gd}	10fF
Pad C_{ds}	12fF
V_{th0}	-1.3 V

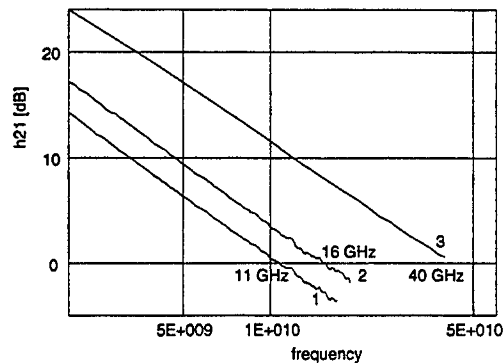

Figure 4: $|h_{21}|$ versus frequency for different gate lengths L and source-gate distances d_{sg}, curve 1: L=500 nm, d_{sg}=500 nm, f_t=11 GHz, curve 2: L=150 nm, d_{sg}=500 nm, f_t=16 GHz, curve 3: L=150 nm, d_{sg}=200 nm, f_t=40 GHz

4 Inverter Circuit

The inverter circuit design is shown in fig. 6 and 5. The circuit consists of a n-type depletion Si/SiGe MODFET (150 nm and 300 nm gate length, respectively, $d_{sg} = 0.5\mu$m and 100 μm gate width) as driver and an ungated n-type MODFET (resistor) as load.

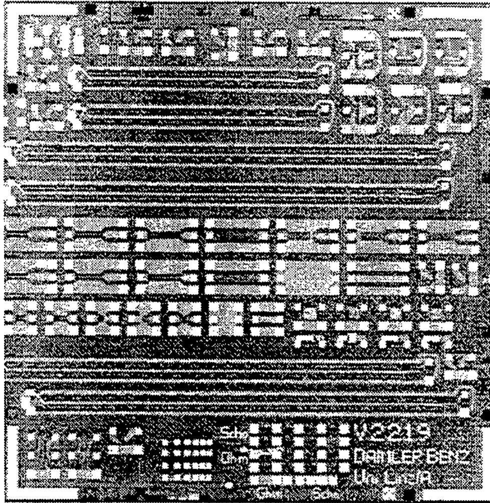

Figure 5: Fabricated test cell with 300 nm and 150 nm gate length inverter circuits in the right upper corner.

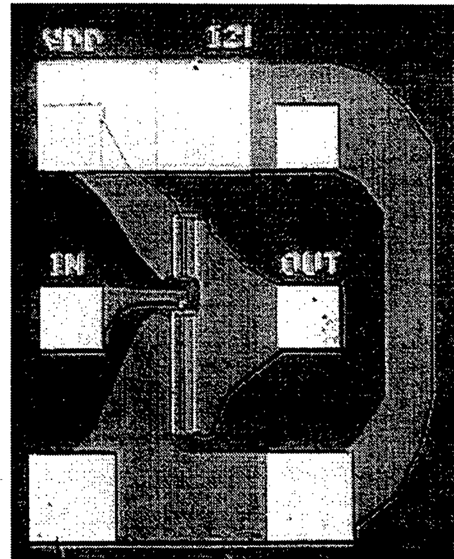

Figure 6: Discrete inverter circuit with a resistor as load and a n-type depletion MODFET as driver.

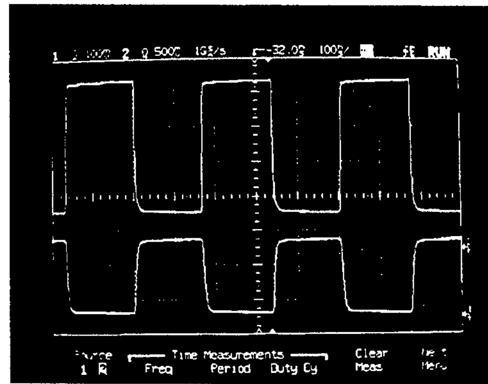

Figure 7: Input and output signal of the inverter circuit

Large signal measurements with an input signal of 600 ps rise time at a supply voltage of V_{dd}= 2 V, show a gate delay of 70 ps for the 300 nm gate length inverter circuit. The maximum output voltage swing is 430 mV. Measurements with an input signal of 150 ps rise time show a gate delay of 25 ps for the 150 nm gate length inverter circuit at a supply voltage V_{dd} = 2 V (see fig. 7 and fig. 8). The gate delay was determined from the delay between the 50% input and output signal value, taking into account the different RC-delays of the measurement equipment, which were calibrated using a special thru-structure of the inverter circuit on the chip.

For digital logic design the inverter circuit of fig. 6 needs a second stage to shift the output to the input levels. The choice of the circuit topology to use with our Si/SiGe MODFETs depends like for well established GaAs HEMTs on the special circuit specifications. Circuit topologies like BFL, UBFL, SCFL, SDFL, DCFL, $\cdots$ (see [6,7]) are suitable for Schottky-gated Si/SiGe MODFETs. In the following section we use a BFL topology with source follower to simulate the delay of an inverter chain. Like in Si CMOS there is no direct correlation between the small signal parameter cut-off frequency f_t of the intrinsic device and the large signal parameter gate delay, because of the other circuit and parasitic elements. Simulations show, that varying of f_t by factor 2 or more the delay varies only by 5%.

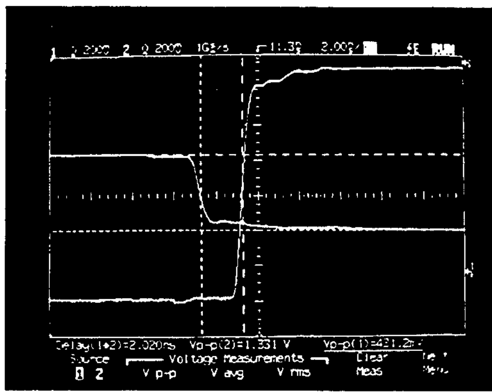

Figure 8: Gate delay and maximum output voltage swing of the inverter.

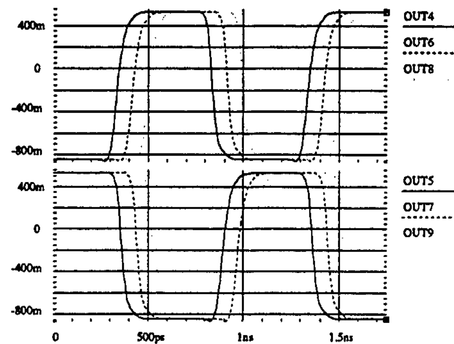

Figure 10: Simulation of an inverter chain, showing the output signal of different stages

5 Circuit Simulation

For simulation of Si/SiGe MODFET circuits we extracted the SPICE parameters for a large signal model based on the Statz MESFET model [8] from small and large signal measurements of discrete MODFETs with different gate lengths and widths. Fig. 2 shows the fitting of the measured and simulated dc-output characteristic of a 150 nm gate length and 50 μm gate width n-type depletion MODFET. To estimate the gate delay of a Si/SiGe MODFET inverter for digital logic design, we use the BFL inverter shown in fig. 9. Fig. 10 shows the output signals of different inverter stages. Fig. 10 also shows the level shifting of the source follower. The gate delay for a 150 nm gate length and 100 μm gate width inverter is 35 ps.

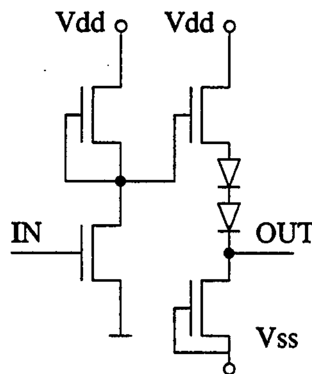

Figure 9: Inverter circuit with source follower.

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In-situ Measurement of Misfit Dislocation Propagation Velocities during the UHV-CVD Growth of SiGe / Si (001)

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An understanding of the kinetics of misfit dislocation propagation is fundamental to successfully modeling strain relaxation of SiGe / Si (001) heterostructures. Previous information about such kinetic parameters has been obtained from *ex-situ* measurements of heterostructures annealed after completion of the crystal growth process. Herein we report direct measurements of the propagation velocities of misfit dislocations obtained during the growth process itself, utilizing the unique capabilities of a specially constructed ultrahigh vacuum transmission electron microscope (UHV-TEM) equipped with *in-situ* chemical vapor deposition growth facilities. In contrast to previous measurements in the InGaAs / GaAs (001) system, which have shown that misfit dislocation threading segments stop propagating during pauses in the growth process with the sample held at temperature [Whaley and Cohen, Appl. Phys. Lett. 57, 144 (1990); Whitehouse, et al., J. Cryst. Growth 150, 85 (1994)] we observe no significant difference in misfit dislocation motion during growth and during post-growth annealing in ultrahigh vacuum for the SiGe / Si (001) system. However, following the formation of a thin native oxide, we find a threefold increase in the magnitude of dislocation velocities. The mechanism causing this increase in dislocation velocity in the presence of a native oxide will be discussed in terms of both dislocation / surface domain interactions and dislocation kink nucleation. The ramifications for the understanding and prediction of strain relaxation during crystal growth and device processing will be addressed.

Scalable Surface Potential Based Compact MOSFET Model

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There is presently a considerable interest in compact MOSFET models accurate for both long-channel and deep submicron devices. This is usually achieved by "binning" or with a large number of adjustable model parameters some of which may become correlated, thus complicating the parameter extraction process [1]. In this work we outline an alternative approach which provides a model accurate over the 0.25-25μ range of channel lengths with a single set of no more than 25 easily extracted parameters. The new model includes most of the essential device physics such as short-channel effects, DIBL, reverse short-channel effect, series resistance, universal mobility dependence on the effective vertical field, velocity saturation, channel-length modulation (CLM), polysilicon depletion layer, etc [2,3].

In the past, several surface potential based models of short-channel MOSFETs were developed either within a gradual channel approximation (zero lateral gradient) context [4-6] or assuming a position-independent lateral gradient factor [7,8]

$$f = 1 - (\varepsilon_{Si}/qN_{sub})\partial^2\Phi/\partial y^2, \tag{1}$$

where N_{sub} is the substrate doping concentration, Φ denotes the surface potential, and y axis is directed from source to drain.

To extend the range of the surface potential based model we combine the latter approach with the CLM description used in [5,9]. This results in the following equation for the drain current

$$I_d = \frac{\mu_s W_{eff} C_{ox}(V_1 + \alpha V_t - 0.5\alpha V_{dsx})V_{dsx}}{L_{eff} - l_d + \delta_0 \mu_s V_{dsx}/v_{sat}}. \tag{2}$$

Here α describes the linearization of the bulk charge as a function of the imref splitting in the channel [2,5], V_t is thermal voltage, $V_{dsx} = \Phi_d - \Phi_s$ is the difference in surface potential at the source and drain ends of the channel,

v_{sat} is the saturation velocity. The normalized mobile charge at the source end of the channel, $V_1 = Q_i/C_{ox}$, is a function of the surface potential:

$$V_1 = \gamma u/[(f\Phi_s - V_t + u)^{1/2} + (f\Phi_s - V_t)^{1/2}] - \Delta V_1^{(poly)}, \qquad (3)$$

where γ is a body factor, $u = V_t \exp[(\Phi_s - 2\Phi_f - V_{sb})/V_t]$, Φ_f is the "Fermi potential" in the bulk, and the last term in (3) describes the voltage drop in the polysilicon depletion layer.

The "effective mobility" μ_s is modified to incorporate the series resistance effect and is expressed as a function of the effective vertical field as defined in [10]. The parameter δ_0 accounts for the difference in velocity-field relations for electrons and holes and l_d describes the CLM [2]. All short-channel effects as well as DIBL are included in a suitably chosen $f(\Phi_s)$ expression to produce a $C^{(\infty)}$ class $I_d(V_{gs}, V_{ds}, V_{bs})$ dependence required for circuit simulators. A smoothing function is used to relate V_{dsx} to the drain bias and drain saturation voltage, the latter computed as in [9]. The moderate inversion region is rigorously described via the first integral of the Poisson equation which includes the lateral gradient factor. The reverse short-channel effect is incorporated in the expression for the flat-band voltage [2] while the concepts of threshold voltage and charge sharing are not invoked. The smooth transition of major model variables from subthreshold to linear region of operation is illustrated in Fig.1.

The new model was applied to devices fabricated using dual poly, self-aligned retrograde twin well, recessed LOCOS CMOS process with $t_{ox} = 6\ nm$. As shown in Fig. 2, a good agreement between the model and the test data was achieved in all regions of operation for both n-channel and p-channel MOSFETs. To summarize, a new surface potential model has fewer parameters than the state-of-the-art regional models and is accurate for (at least) $L_{drawn} = 0.25 - 25\ \mu$ without binning.

The authors are grateful to B. Gelmont and D.P. Foty for several illuminating discussions of this work.

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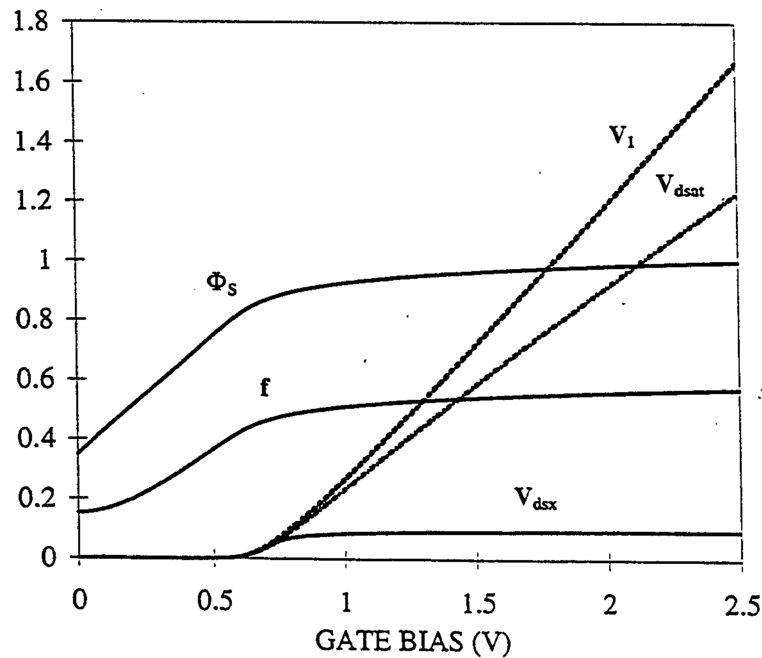
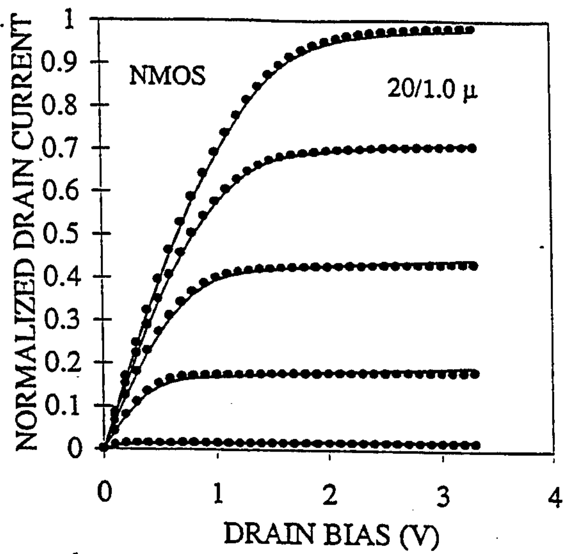
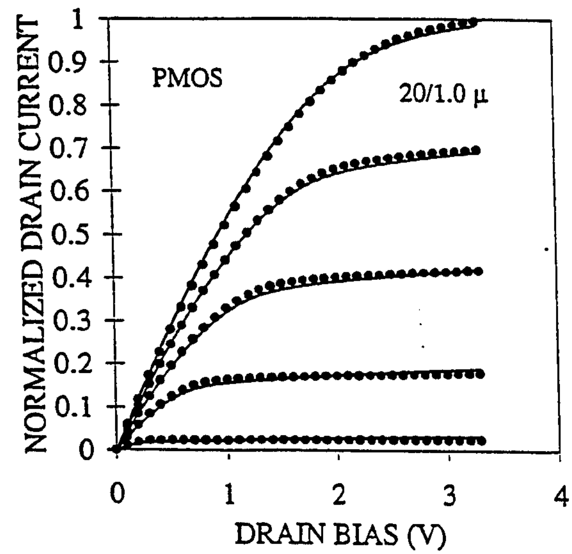
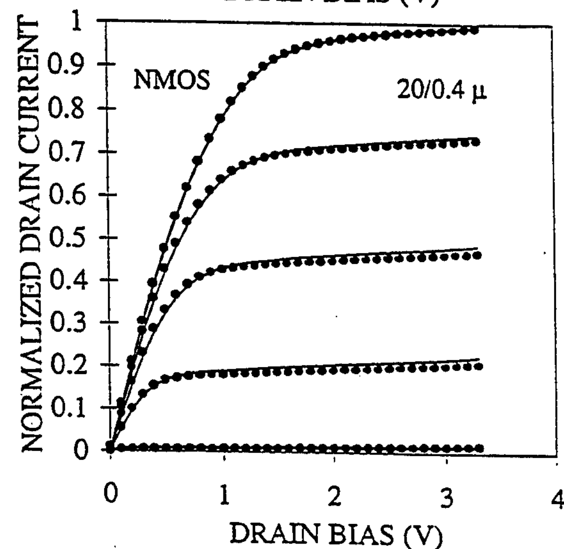
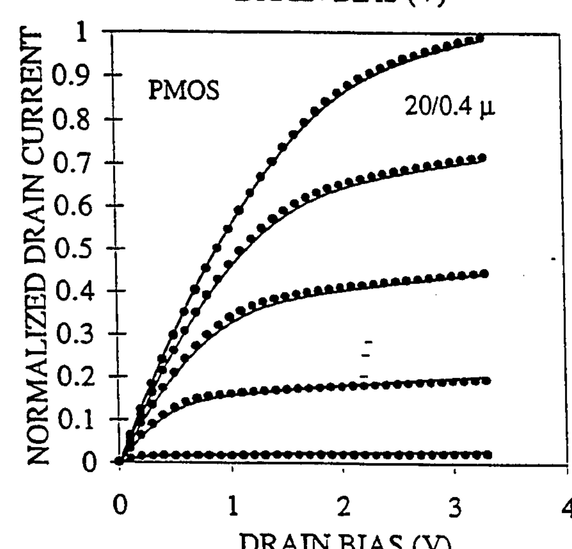


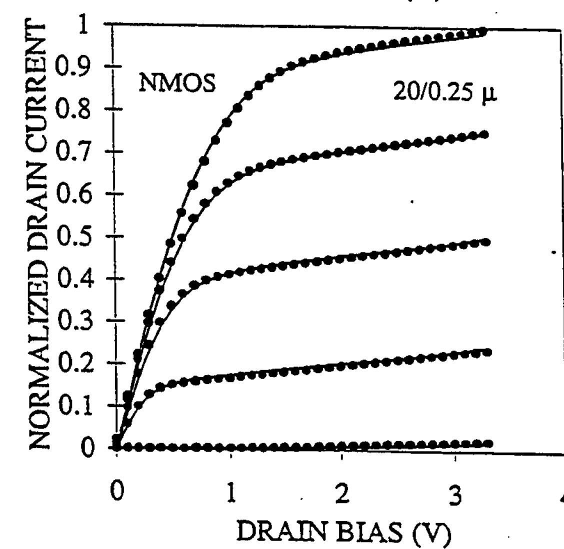
Fig. 1. Typical gate bias dependence of the surface potential Φ_s, lateral gradient factor f, normalized mobile charge V_1, saturation voltage V_{dsat}, and effective drain bias V_{dsx} for $L = 0.25\mu$, $V_{ds} = 0.1V$ and $V_{sb} = 0$.











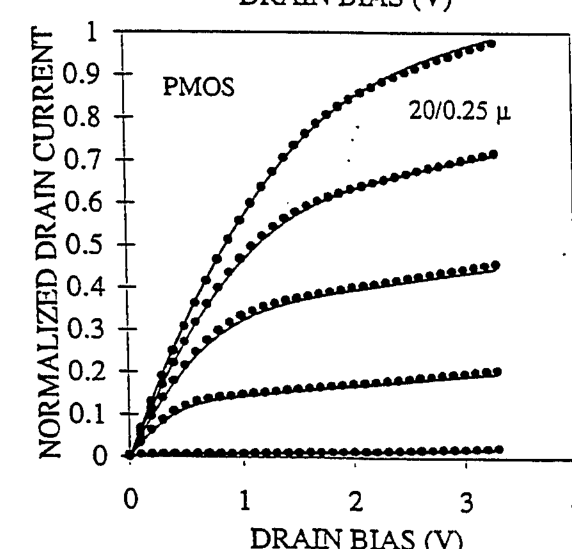


Fig. 2. Normalized measured (solid lines) and simulated (circles) $I_d(V_{ds}, V_{gs})$ characteristics of NMOS and PMOS transistors with different channel lengths at 25°C. Gate voltage starts at 0.66V with increments of 0.66V.

MOSFET Intrinsic-Capacitance Related Inaccuracy in CMOS Circuit Speed Simulation

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1.0 Introduction

Accurate characterization and modeling of MOSFET intrinsic capacitances for CMOS circuit simulation and design has long been an issue of great importance [1-6]. As CMOS technology vigorously advances into deep-submicron regimes, some of the accuracy issues are renewing both research and practical interest in both academic and industrial communities [7]. This extended abstract systematically covers those issues, related to MOSFET intrinsic capacitance characterization and modeling, and their impact on CMOS circuit speed simulation in terms of: (1) quasi-static (QS) and high-frequency (HF) based C-V characterization techniques; (2) QS modeling of intrinsic capacitances considering more advanced device physics such as finite charge thickness due to quantization, polysilicon depletion and non-pinned surface potential effects; (3) non-quasi-static (NQS) effect; and (4) channel charge partitioning schemes. Careful examination and fundamental treatment of the above problems have been made at a physical level. Extensive 2-D simulation using MEDICI and measurement data are deployed for the study. Implications for achieving more accurate characterization and modeling of MOSFET intrinsic capacitances and accurate CMOS circuit simulation are presented. It is believed that the present results could serve as guidelines for future CMOS IC design.

2.0 Experiment, Modeling & Simulation: Results and Discussion

2.1 C-V Characterization Methodologies

It is a standard practice in industry to use large *W* and *L* MOSFETs for capacitance measurement and then use the result to model MOSFETs of very small channel length. Two widely used methods to experimentally characterize MOSFET capacitance are high frequency (HF) and quasi-static (QS) measurement. However, these two types of measurements do not agree with each other, as shown in Figure 1, where the leakage current related error in QS measurement [8] has been carefully removed. To confirm that the discrepancy between the two is physical rather than due to a measurement error, 2-D simulation has been performed and the result is shown in Figure 2. The slope of *Cgc* is frequency dependent.

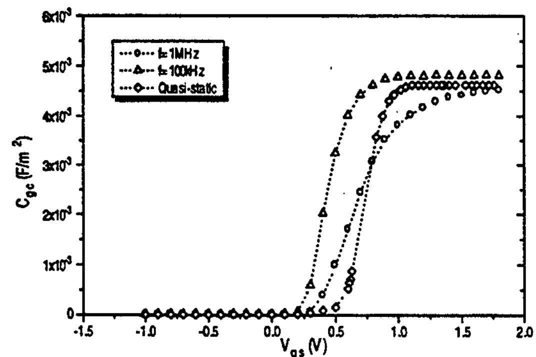

Figure 1. The difference in curve slopes for HF and QS C-V measurements is caused by the RC delay effect. *Tox*=5.7nm, *W/L*=100µm/100µm.

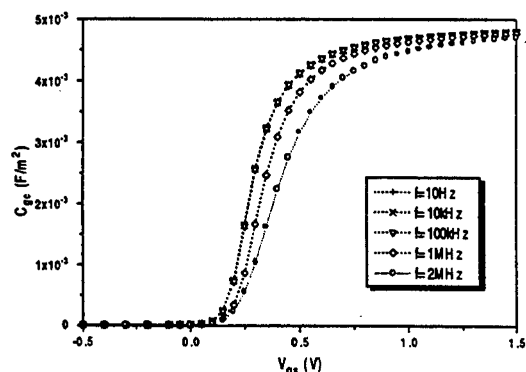

Figure 2. 2-D simulation shows the difference between QS and HF measurement is physical. *Tox*=7nm, *W/L*=50µm/50µm.

The discrepancy between the HF and QS data can be explained by the RC effect of the distributed MOSFET channel resistor and gate capacitance. Larger L results in a more prominent RC delay because of larger channel resistance and capacitance as demonstrated in Figure 3.

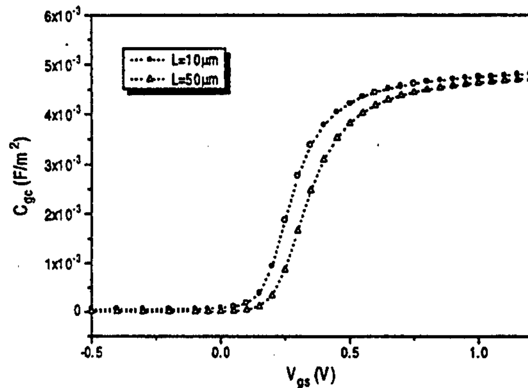

Figure 3. Normalized *Cgc* versus *Vgs*. The difference is caused by RC delay. *Tox*=7nm, *W*=50μm, *f*=1MHz.

Since RC delay is proportional to L^2, curves with the same fL^2 will be expected to behave identically. This is confirmed by Figure 4. For instance, a 0.5μm MOSFET operating at 400MHz is expected to have the same CV curve as a 50μm device at 40kHz as long as the short channel effect is negligible.

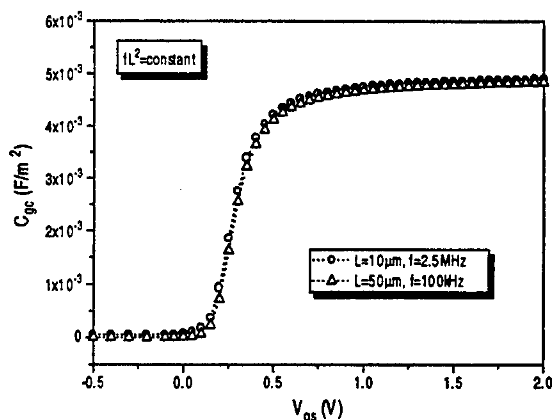

Figure 4. Universal *Cgc* versus *Vgs* for fL^2=constant confirmed by 2-D simulation. *W*=50μm, *Tox*=7nm.

The fact of measurement frequency and channel length dependencies of MOSFET intrinsic capacitances has an immediate practical impact. In practice, because of its simplicity only capacitance of MOSFETs with large channel lengths is measured. QS or lower-frequency (10kHz) data should be used in order to have an accurate model for minimum-channel devices. Unfortunately, 1MHz frequency measurement is the prevalent practice and accounts for much of the claims of *model inaccuracy*. This HF measurement practice should be changed.

2.2 New QS Intrinsic Capacitance Modeling

With the above interpretations in mind, we use QS measurement as the benchmark for intrinsic capacitance model testing. A new QS intrinsic capacitance model was developed considering more advanced device physics such as finite charge thickness due to quantization, polysilicon depletion and non-pinned surface potential effects [9]. Figure 5 gives the plots of *Cgg* versus *Vgs* by comparing this new model and BSIM3v3.1 capmod=2 [10] with QS CV data. It can be observed that the new model can fit data better through the whole operating regions. As is shown in Figure 6, an appreciable difference in the oscillating frequency can be observed for a 0.25μm 101-stage CMOS ring oscillator between these two models, even when the overlap and fringing capacitances were considered in simulation. It is therefore anticipated that in the situation when QS operation maintains, the new model can offer accurate simulation in circuit design.

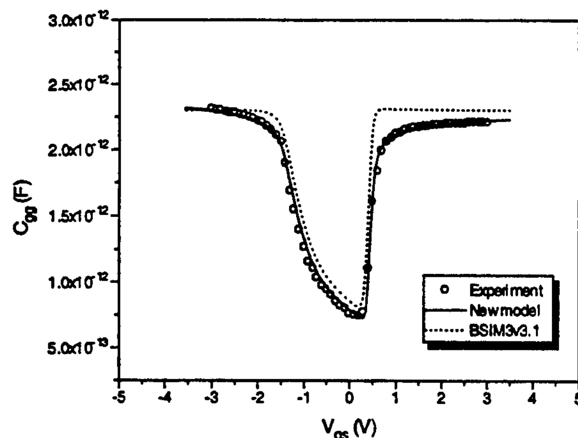

Figure 5. Comparison of *Cgg* versus *Vgs* between the new model, BSIM3v3.1 capmod=2 and QS C-V data. *W/L*=50μm/10μm, *Tox*=7.5nm.

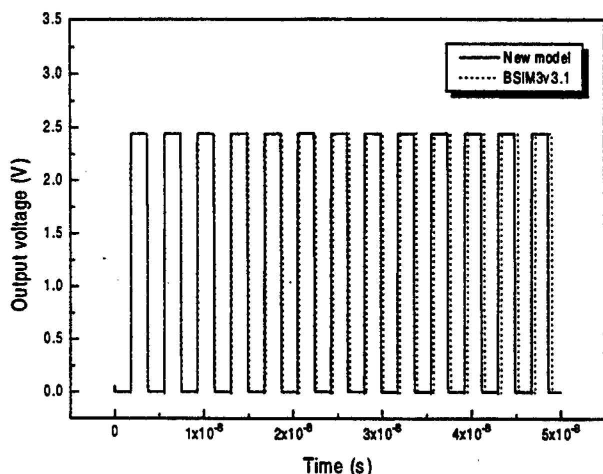

Figure 6. Output voltage waveform of a 0.25μm 101-stage CMOS ring oscillator (*Tox*=7.0nm) simulated with the new model and BSIM3v3.1 capmod=2.

2.3 Non-Quasi Static Model

Only models accounting for the distributed nature of MOSFET channel can predict the effect of RC delay on capacitance of devices over a wide range of channel lengths. Figure 7 is presented to demonstrate that the Non-Quasi Static (NQS) model implemented in BSIM3v3.1 [11] is capable of modeling the frequency dependence of capacitances. Figure 8 illustrates that the two curves with the same value of fL^2 indeed coincide, when simulated using the NQS model. Finally, Figure 9 shows the difference between *Cgc* curves predicted by QS and NQS models, and the percent error between them.

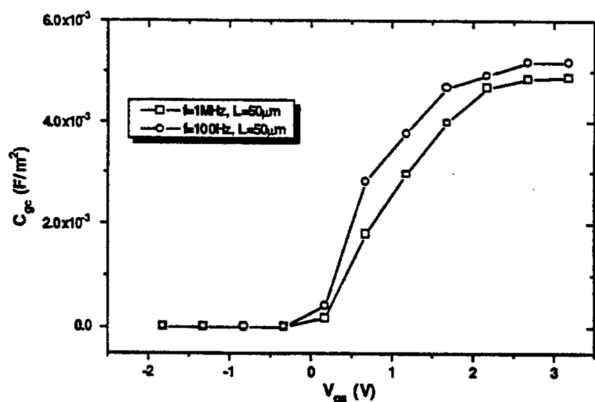

Figure 7. *Cgc* simulated by BSIM3v3.1 NQS model shows similar results as shown in Figures 1 and 2 with RC delay effect. *W*=50μm, *Tox*=7nm.

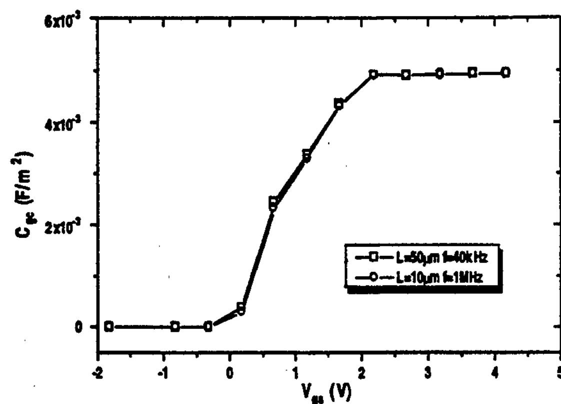

Figure 8. BSIM3v3.1 NQS simulation of *Cgc* versus *Vgs* for fL^2=constant achieves similar universal curves as shown in Figure 4 by 2-D simulation. *W*=50μm, *Tox*=7nm.

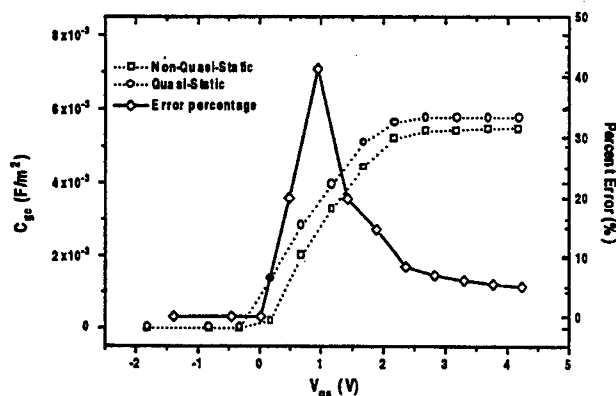

Figure 9. For high frequency transient simulation, using quasi-static instead of NQS model can result in errors as large as 30%. *L*=50μm, *Tox*=7nm.

2.4 Charge Partitioning and NQS Effects for Gate Delays

Even if the *CV* data is perfect, charge partitioning introduces gate speed inaccuracies. Two quasi static charge partitioning schemes are commonly used. The most physical of them (only at low frequencies) [3], 40/60, has been shown to produce an erroneous result during fast transients [11]. 0/100 scheme solves this problem but is entirely artificial. We now use the non-quasi static model as the benchmark to evaluate the error of these two charge partitioning schemes.

Figure 10 shows the ring oscillator speeds for several technology generations, simulated using BSIM3v3. Quasi-static approaches consistently predict slower circuit performance than the non-quasi static model. Figure 11 gives the percent error in simulation results caused by using the two quasi-static models (40/60 and 0/100). The error ranges from 5% for 0.35µm to 15% for 1µm, but becomes less significant with technology scaling.

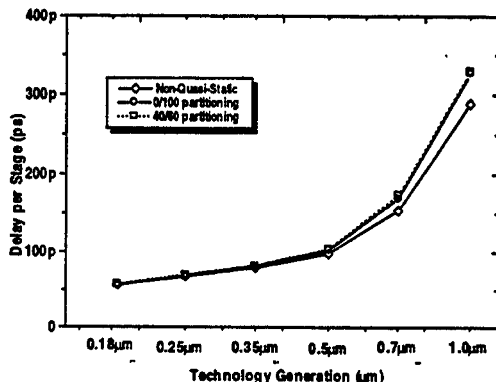

Figure 10. NQS versus charge partitioning: ring oscillator speed simulation shows that the delay may be overestimated if NQS model is not used.

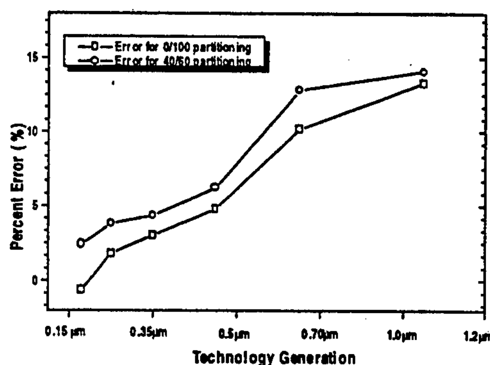

Figure 11. The error of speed simulation can be as large as 14% if NQS model is not used. However the error is small in more advanced technologies.

3.0 Summary

In summary, for accurate intrinsic capacitance model testing, quasi-static CV measurement instead of high-frequency technique should be employed because of frequency and channel length dependence of the distributed RC delay. A new intrinsic capacitance model considering more advanced device physics such as quantization, polysilicon gate depletion and non-pinned surface potential effects was found to fit QS CV data more accurately than BSIM3v3.1 and result in a appreciably different speed prediction for a 0.25µm ring oscillator though the intrinsic capacitance was believed to be a small fraction of the total capacitances. The distributed RC delay can be accurately characterized by the BSIM3v3.1 NQS model. It is also found that the channel partitioning schemes (both 0/100 and 40/60) predict slower circuit speed than the NQS model where the RC delay becomes significant; however, as CMOS technology is scaled down to 0.25µm and beyond, such discrepancy diminishes.

Acknowledgment: The authors are very grateful to Drs. Keith Green and Tom Vrontosos at Texas Instruments and Mr. Junichi Ohtani of Sony Corp. for helpful discussions.

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Distributed Numerical Simulation of Electronic Devices using a Java Interface

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Over the past decade, the Applied Electrophysics Laboratory at the University of Virginia has been developing a system to accurately model and simulate high frequency devices by combining a modified drift and diffusion analysis with a harmonic balance nonlinear circuit analysis[1,2,3]. These devices include GaAs/AlGaAs Heterostructure Barrier Varactors, GaAs Schottky Barrier Varactors, and GaAs or InP Transferred Electron Devices; a SPICE model for SiGe devices is currently in production. Using the Mentat distributed computational system[4] to distribute each device simulation "point", it is possible to obtain key results over a n-dimensional parameter space. Parallelization of this process allows the researcher to obtain in one day a range of data that would take weeks to obtain on a single workstation.

Device simulations operate as text based Fortran programs which are executed on various Unix platforms and due to the complex nature of our distributed computing system, the time to fully understand such a system is too long for most practicing researchers. This investment in time coupled with the cost of the necessary computer hardware makes the large-scale distribution of this code infeasible and impractical. Therefore, the creation of a network based application distribution model is the most practical method of application distribution. The creation of an easy to use, web-enabled device simulation environment is the next step in this system's design, and, in the last three years, a number of technologies have converged to produce an atmosphere conducive to this realization.

Java and the Web enabled us to create a web-based device simulation tool which will work on any major platform. Therefore, a user is able to submit a device simulation, from any machine, and obtain results without spending considerable time and effort learning how to instantiate concurrent jobs on a network of 30+ Unix workstations. As shown in Figure 1, our central controller is a shell script, which then instantiates a C++ program that then, through the Mentat system[4,5], distributes each stand-alone Fortran "point" to each computational unit, and this Java interface interacts directly with the existing device simulation system.

While Java decentralizes the CPU intensive process of maintaining a Graphical User Interface, it also allows us to centralize and control the complex process of device simulation. The machines on which these simulations run, do not deal with user interaction and can devote more resources to the numerical simulation – a more efficient use of computing resources. The user interface software is "deployed" with each use, which, in turn, enables the application developers to quickly upgrade or completely overhaul the distributed process of computation. This makes it easy to add new device codes and computing resources as needed.

Upon entering the simulation area of this site, a user is presented with a login and password dialog which is then encrypted and analyzed by a web server. Upon successful authentication, a user is presented with three choices when entering the simulation area of this web site, they can choose between the TEO, HBV, or the SBV simulation environments. Prior to the submission of a complex parallel job, the user can also run a less accurate analysis called Quick Design. Quickdesign will return rough results in a matter of seconds, and this provides insight to the optimal embedding impedance values and device parameters. After the iterative process of using quick design to roughly predict the results of a full simulation, the user can then submit the simulation to our system. The local system then manages the distribution of the device simulation points, collects the relevant data, and emails a compressed file back to the user.

Web based device simulation applications have the advantage of using a centrally maintained center for computation, and as device explorations move towards smaller slices of time and matter, it will be necessary to simulate this phenomena on increasingly expensive and powerful computers. A system like this allows a world-wide workgroup of design and research engineers to concurrently share the same computational resources without getting lost in the minute details of computing.

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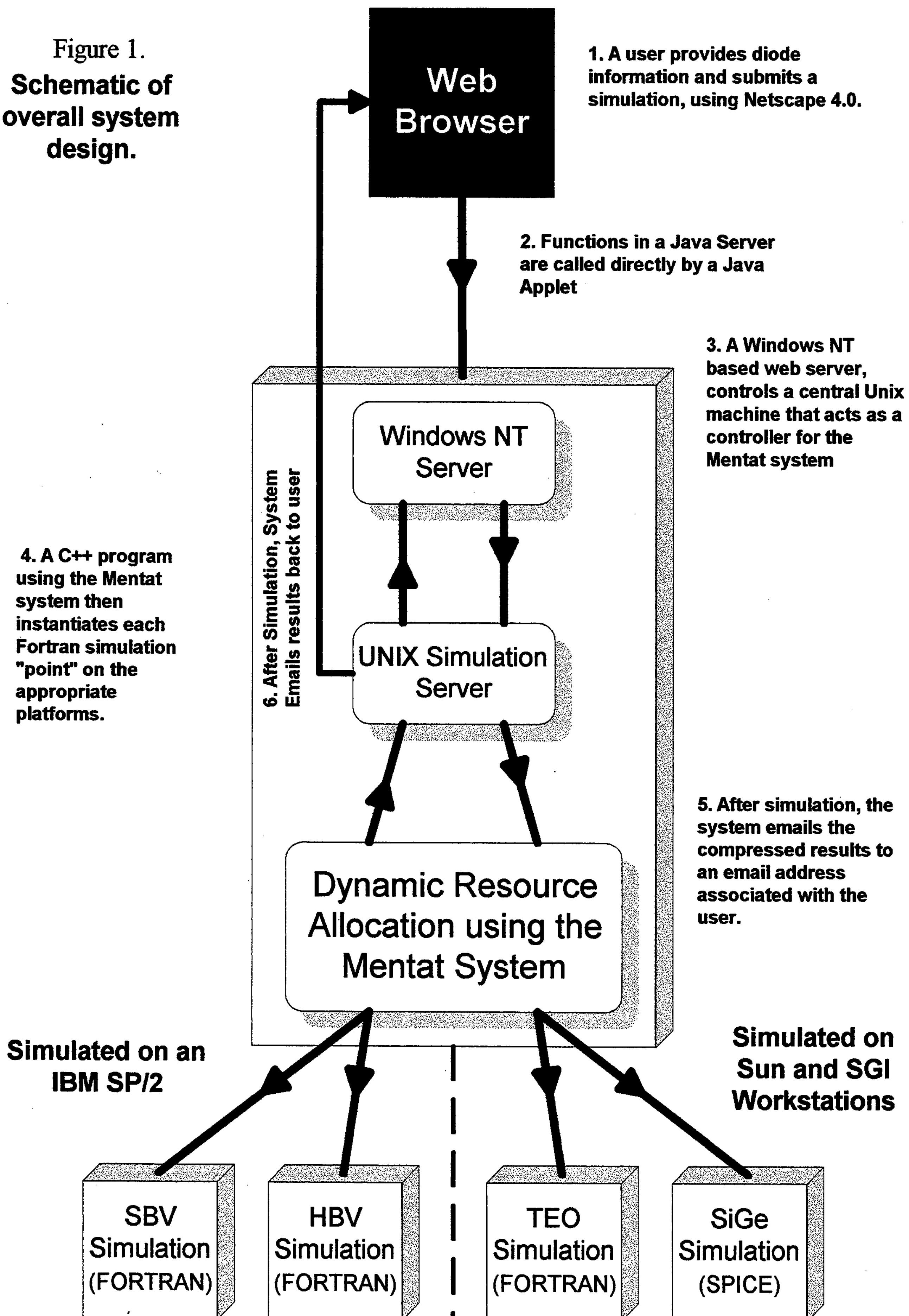

Figure 1. **Schematic of overall system design.**

Modeling and Analysis of Edge Parasitic Transistor Effects in the Mesa-isolated Fully-depleted SOI NMOS Devices

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I、INTRODUCTION

Thin-film fully-depleted SOI CMOS devices keep receiving considerable attention owing to their advantages in low power applications and reduced second-order effects[1]. SOI CMOS technology depends on high quality isolation. Mesa isolation is attractive due to its simplicity in processing and high package density[2], but the island edge effects which result in subthreshold leakage from the lower threshold voltage on SOI island edge are inevitable. Several investigation about the island edge effect of SOI MOSFET have been reported[3-5] recently, but little attention has been paid to modeling the edge parasitic transistor effects[6,7]. Analysis of the influence of various device technological parameter on the edge parasitic transistor effects has not been carefully discussed.

In this paper, we developed an analytical sidewall surface potential model using an quasi-two dimensional approach, then , basing on this potential model, an analysis is made of both the isolation and transistor technological parameters responsible for the appearance of the island edge parasitic effect.

II、THE MODEL

A schematic cross section of the mesa-isolated fully depleted SOI NMOS device with the sidewall structure is shown in Fig.1. Before the onset of strong inversion, Poisson's equation in the thin film is

$$\frac{\partial^2\Phi(x,y)}{\partial x^2}+\frac{\partial^2\Phi(x,y)}{\partial y^2}=\frac{qN_A}{\varepsilon_{si}} \tag{1}$$

where N_A is the extrinsic doping concentration in the film, ε_{si} is the dielectric constant of silicon, t_{si} is the film thickness.

Following[8], we assumed a parabolic function along the vertical(x) dimension for the solution of (1)

$$\Phi(x,y)=C_0(y)+C_1(y)x+C_2(y)x^2 \tag{2}$$

where the coefficient Ci's(i=0-2) are determined by the boundry conditionn of equation(1). Substituting (2) into (1) give an expression of the form in the lateral direction at a vertical location $x=\eta t_{si}$ in the thin film($0\le\eta\le1$)

$$2C_2+\frac{\partial^2\Phi(\eta t_{si},y)}{\partial y^2}=\frac{qN_A}{\varepsilon_{si}} \tag{3}$$

with $$C_2=-(a_1+a_2)\cdot\Phi_f(y)+a_1\cdot V_{gfr}+a_2\cdot V_{gbr} \tag{4}$$

$$a_1=\frac{C_{of}/C_{sb}}{t_{si}^2(1+2C_{si}/C_{ob})} \tag{5}$$

$$a_2=\frac{1}{t_{si}^2(1+2C_{si}/C_{ob})} \tag{6}$$

where $\frac{1}{C_{sb}} = \frac{1}{C_{ob}} + \frac{1}{C_{si}}$, C_{of}, C_{si}, C_{ob} are the front gate oxide capacitance, silicon film capacitance, back gate oxide capacitance respectively. $V_{gfr}=V_{gf}$(front gate bias)-V_{fbf}(front flat-band voltage), $V_{gbr}=V_{gb}$(back gate bias)-V_{fbb}(back flat-band voltage).From equation (2), $\Phi_f(y)$ can be expressed as a function of $\Phi(\eta t_{si},y)$

$$\Phi_f(y)=\frac{\Phi(\eta t_{si},y)-\left(\eta t_{si}^2\cdot a_1 - C_{of}/C_{si}\right)\eta\cdot V_{gfr} - a_2\cdot(\eta t_{si})^2 V_{gbr}}{\gamma} \qquad (7)$$

$$\gamma = 1+\eta\, C_{of}/C_{si} - (\eta t_{si})^2 (a_1 + a_2) \qquad (8)$$

Substituting (7) into equation(4), equation(3) can be rewritten as

$$\frac{\partial^2\Phi(\eta t_{si},y)}{\partial y^2} - \alpha\Phi(\eta t_{si},y) = \beta \qquad (9)$$

$$\alpha = 2\cdot(a_1 + a_2)\cdot\frac{1}{\gamma} \qquad (10)$$

$$\beta = \frac{qN_A}{\varepsilon_{si}} - 2\cdot\left[\frac{(a_1+a_2)}{\gamma}\cdot\left(a_1\cdot\eta^2 t_{si}^2 - \frac{\eta C_{of}}{C_{si}}\right) + a_1\right]\cdot V_{gfr} - 2a_2\left[\frac{(a_1+a_2)\cdot\eta^2\cdot t_{si}^2}{\gamma} + 1\right]\cdot V_{gbr} \qquad (11)$$

For the differential equation of equation(9), its boundary condition are:

$$\Phi(\eta t_{si},0) = \Phi_{edgf}(\eta t_{si})$$

$$\left.\frac{d\Phi(\eta t_{si},y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{\Phi_{edgf}(\eta t_{si}) - V_{ger}}{t_{ed}}$$

$$\left.\frac{d\Phi(\eta t_{si},y)}{dy}\right|_{y=\frac{W}{2}} = 0 \qquad (12)$$

with $V_{ger} = V_{gf} - V_{fbe}$

where V_{fbe} is the sidewall edge flat-band voltage, t_{ed} is the thickness of sidewall oxide, $\Phi_{edgf}(\eta t_{si})$ is the potential along the island sidewall surface. Solving equation(9) under boundary condition(12), we can obtain

$$\Phi_{edgf}(\eta t_{si}) = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V_{ger}}{t_{ed}\alpha^{1/2}} - \sigma\right)\Big/\left(1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{ed}\alpha^{1/2}}\right) \qquad (13)$$

with $\sigma = \beta/\alpha$ (14)

To verify the proposed analytical sidewall surface potential model, the PISCES program was used to simulate the potential distribution within the silicon film. Fig.2 show the calculated and simulated value of $\Phi_{edgf}(\eta t_{si})$ against x for V_{gb} value of -1V,0V,1V. It is clearly seen that good agreement between our analytic model and 2D numerical analysis are obtained.

III、RESULTS AND DISCUSSIONS

As shown in Fig.2, since the electron concentration depends exponentially on the electrostatic potential, the subthreshold characteristics of sidewall parasitic transistor is mainly determined by the upper corner channel, but when the back gate bias increases, the bottom corner channel also contribute to the subthreshold current of sidewall parasitic transistor. Fig.3 present the influence of the channel doping concentration (N_A) on the upper corner potential. When increasing the N_A, the upper corner potential decrease more slowly than the front surface potential. So the higher the channel doping, the more serious the parasitic effect. The fixed positive charges on the sidewall of island has opposite effects on NMOS and PMOS, i.e., reducing the edge effect on the PMOS and enhancing it on the NMOS(as shown in Fig.4). The calculated subtreshold current as a function of front gate

bias for different fixed positive charge densities on the sidewall are also shown in the inset. The parasitic sidewall transistor is normally oriented along(110) surface. Higher fixed positive charge on (110) surface can degrade the electrical behavior of the NMOS transistor. So it is important to reduce the quantity of fixed charge. From fig2. to fig.4, the model results show a good prediction of influence of various device parameter on the potential distribution of sidewall surface as verified by the PISCES data.

The above-derived potential distribution now is used to model the subthreshold current of sidewall parasitic transistor. Substituting equation(13) into the subthreshold current equation[10], the subthreshold current of sidewall parasitic transistor can be calculated. Fig.5 to 7 show the calculated subthreshold current of the parasitic sidewall transistor and the main transistor for the various device parameters. From these figures, we find out that the sidewall transistor is less sensitive to the channel doping ,gate oxide thickness and silicon film thickness. The results are consequence of the enhanced gate control on the sidewall transistor by the gate fringing field. When the current of sidewall transistor is smaller than the main transistor, the "hump" effect will disappear. As shown in these figures, by decreasing the gate oxide thickness, channel doping concentration and silicon film thickness, the sidewall parasitic effect decrease. These results are the same as the SILO-isolated bulk device[9], except for silicon film thickness. But lower channel doping, thinner gate oxide and thinner silicon film will lead to a decrease of the transistor threshold voltage. It is nevertheless possible to adjust the threshold voltage by appropriate choice of mid-gap gate material. Fig.8 exhibits the dependence of edge parasitic transistor effect on the back gate bias. By increasing back gate bias, the "hump" effect can decreased and disappears. This result is verified by the experimental data[12]. Because the sidewall transistor does not scale with device width, the edge parasitic transistor effect will be more serious problem in deep-submicrometer SOI MOSFET's.

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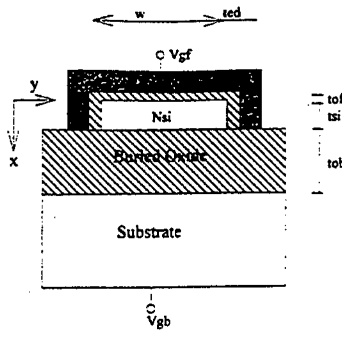

Fig.1. Cross section of the mesa-isolated fully depleted SOI NMOS device.

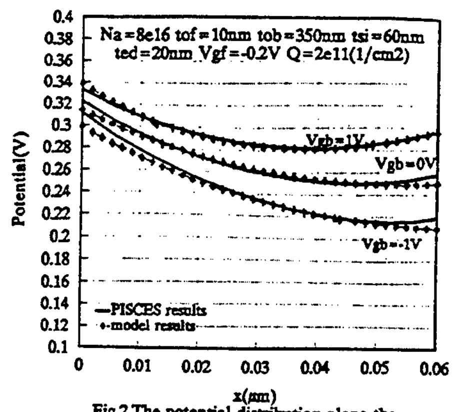

Fig.2.The potential distribution along the sidewall surface versus distance(x) for different back gate biases.

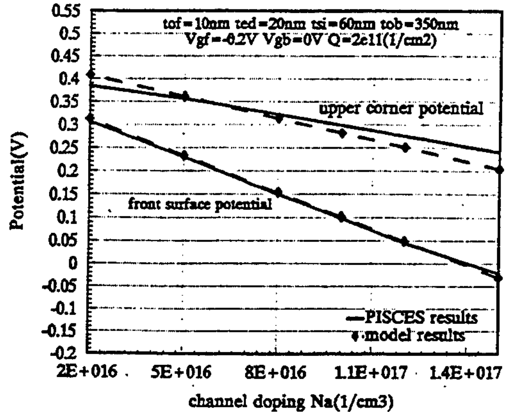

Fig.3.Upper corner potential and the front surface potential versus the channel doping

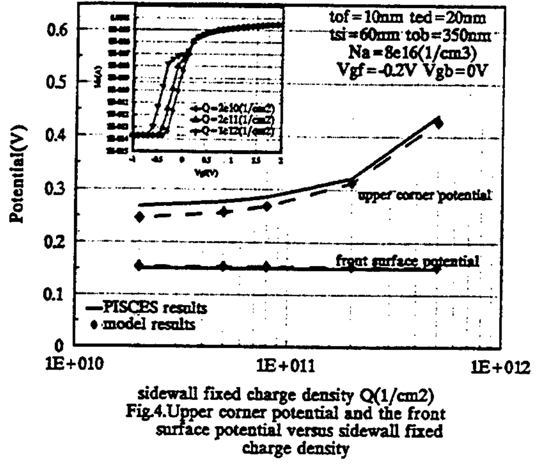

Fig.4.Upper corner potential and the front surface potential versus sidewall fixed charge density

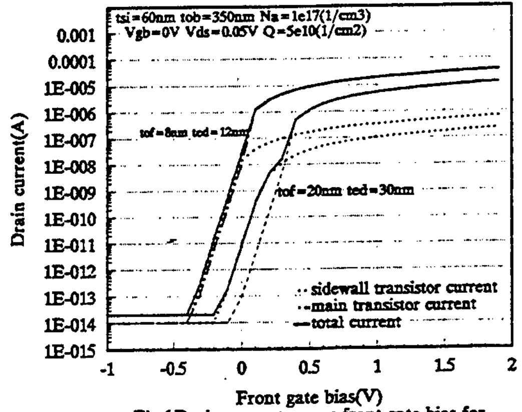

Fig.6.Drain current versus front gate bias for different front oxide thicknesses.

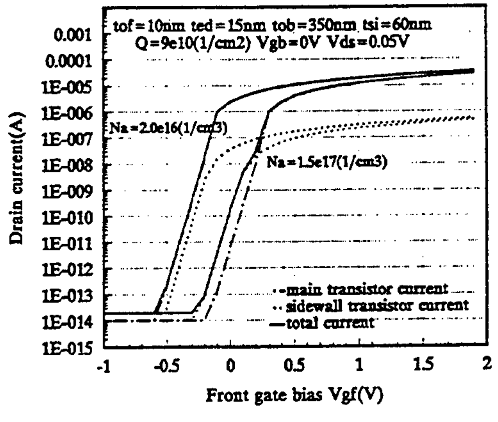

Fig.5.Drain current versus front gate bias for diffrent channel doping

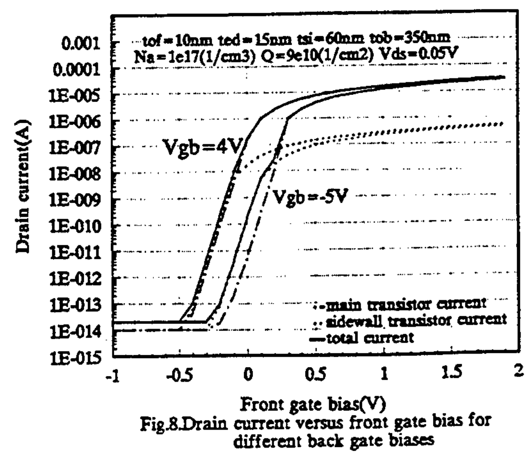

Fig.8.Drain current versus front gate bias for different back gate biases

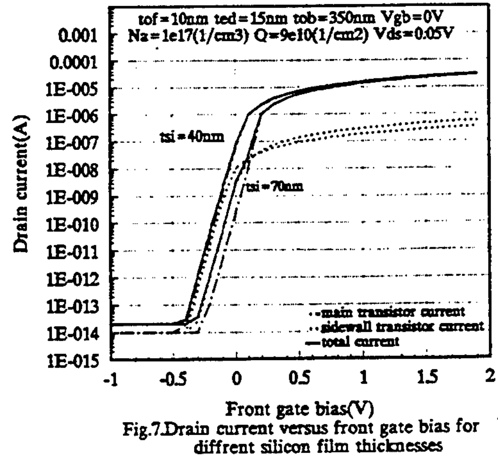

Fig.7.Drain current versus front gate bias for diffrent silicon film thicknesses

High and Low Levels of Simulation of Single-Electron Circuits

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Techniques of high and low levels of single-electron circuit simulation are presented. As regards low-level simulation, visualization of state probabilities and a new algorithm for accurate dc analysis that uses the master equation and Monte Carlo method in combination receive treatment. As for high-level simulation, a SPICE-based simulator for circuits consisting of Single-Electron Transistors (SETs) is proposed. The SPICE-based simulator outperforms the low-level simulator in speed. It also facilitates the study of the integration of SETs and MOSFETs.

1 Introduction

Conventional low-level single-electron simulators treat a circuit as a network of tunnel junctions, capacitors, etc. They are useful for analyzing a single device or small scale circuits precisely. For analyses of large scale circuits, a higher-level simulator that uses simplified device models and offers high-speed simulation is required [1]. In this article we introduce our single-electron circuit simulators: a low-level simulator "ESS" and a SPICE-based high-level simulator "SET-SPICE."

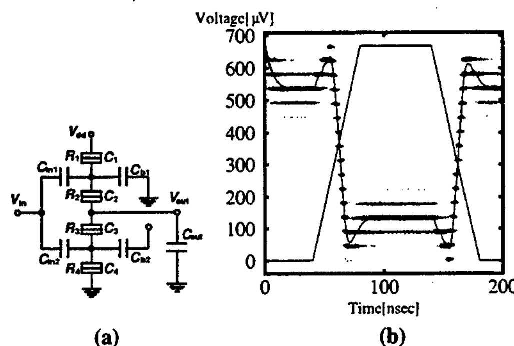

Fig. 1. (a) An inverter circuit proposed by Tucker [5]. (b) A transient response of the inverter to a single input pulse. The curved thin solid line denotes the average output voltage. Thickness of each smoky line represents the probability of the corresponding state. C_{out} is chosen so that fifteen excess charges make full logic swing.

2 Low-level simulator

2.1 Overview

ESS is capable of simulating circuits of arbitrary topology consisting of tunnel junctions, capacitors and voltage sources, using the semiclassical model of single-electron tunneling. It can also take cotunneling [2] into consideration. Simulation methods are the master equation and the Monte Carlo method. The master equation is a set of differential equations that describe the dynamics of a single-electron circuit in terms of probabilities of electric charge states. It can be reduced to a set of simultaneous linear equations, i.e. the steady-state master equation. The Monte Carlo method [3, 4] is widely used for transient simulation and crude dc simulation. It simulates stochastic nature of tunneling events using random numbers.

2.2 Visualization of state probabilities

The solution of the master equation is a set of probabilities associated with charge states. Usually the probabilities are only used to calculate ensemble average of physical quantities. It is helpful if one can *see* the state probabilities.

We have developed a graphical tool that visualizes the probabilities of charge states. Transient waveforms of an inverter circuit (Fig. 1(a)) [5] is shown in Fig. 1(b). The output voltages for various charge states in response to a single input pulse are plotted. The output is drawn so that voltages for probable states look thick and those for improbable states look thin, according to the state probabilities. As can be seen from the figure, possible output voltage is discrete and do not coincide with the average value (solid line).

A similar graph can be plotted out of the data obtained by multiple runs of Monte Carlo simulation. It agrees well with the original graph drawn from the solution of the master equation, thereby mutually validating the other simulation method.

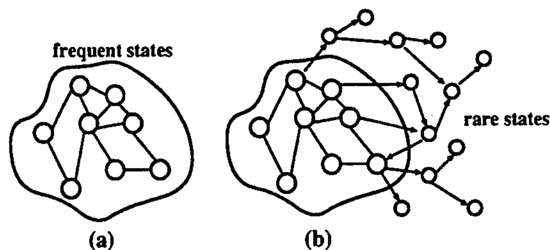

Fig. 2. A new algorithm for dc analysis. (a) Run a Monte Carlo simulation to traverse frequently occupied state space. (b) Directly search for rare states, starting from frequent states.

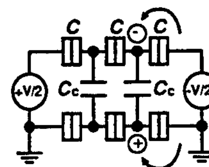

Fig. 3. Capacitively-coupled tunnel junction arrays.

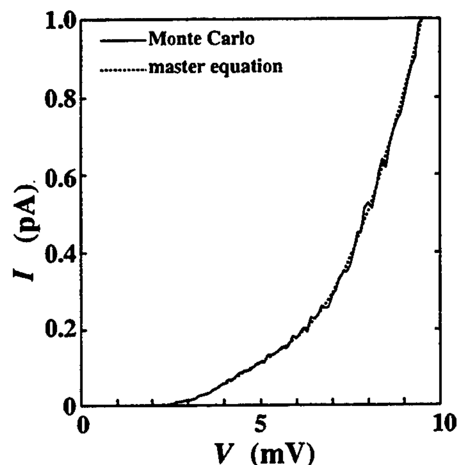

Fig. 4. *I-V* characteristic of the upper array. Our new algorithm gives more accurate result (dotted line) than the Monte Carlo method (solid line).

2.3 A new algorithm for dc analysis

There are two ways of performing dc analysis. One is to run the Monte Carlo simulation and compute time average. The other is to solve the steady-state master equation. The Monte Carlo method cannot incorporate the effects of rare events precisely, and the convergence of averaging calculation is very slow. *I-V* curves obtained by the Monte Carlo method, therefore, are in general inaccurate and not smooth. The steady-state master equation is merely a set of simultaneous linear equations. It cannot, however, be solved without *a priori* information about the circuit, i.e. states that have to be considered need to be predetermined.

ESS uses these two methods in combination to perform dc analysis. It chooses necessary charge states using the Monte Carlo method followed by a direct search procedure [6], and then solves the master equation. First, a Monte Carlo simulation is run to traverse frequently occupied state space (Fig. 2(a)). The states visited during the run are recorded for later use. Then possible transition paths are directly tracked down recursively to search for rare states, starting from each recorded state (Fig. 2(b)) with crudely estimating the rare state probabilities.

Although state probabilities are roughly estimated during the Monte Carlo simulation and the direct search, these procedures are used only to choose states. State probabilities are calculated from the master equation, which gives accurate result. Thus, it is useful for quantitative study of contribution of rare events.

We demonstrate the advantage of our new algorithm with the simulations of the circuit shown in Fig. 3 [7–9]. Figure 4 shows the *I-V* curves for the upper array. The smooth curve (dotted line) cannot be obtained with the Monte Carlo method alone (solid line).

3 High-level simulator

Since low-level simulators treat a circuit as a network of tunnel junctions, simulation of single-electron circuits requires so much memory and computation time that simulation of large scale circuits is impossible. A higher-level circuit simulator is required to investigate single-electron circuits for real applications. Another problem is that conventional simulators cannot simulate MOSFETs. Since output current of a SET is limited by the large tunnel resistance, it has to be amplified with MOSFETs. We propose a high-speed simulation technique for circuits consisting of SETs and MOSFETs.

Our high-level simulator SET-SPICE is based on the SPICE circuit simulator. In SET-SPICE Single-Electron Transistors (SETs) shown in Fig. 5 are treated as circuit elements [10]. Each SET's *I-V* characteristics are used for the calculation. SET-SPICE can correctly simulate a circuit if it satisfies the following two conditions: (i)

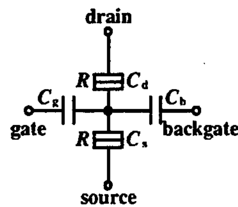

Fig. 5. Schematic of a Single-Electron Transistor (SET) with a backgate.

SET is the only device that contains tunnel junctions, and (ii) all SETs are connected to circuit nodes that have large capacitances. The condition (ii) ensures that each SET can be regarded as being voltage-biased.

I-V characteristics of SETs are calculated using the steady-state master equation. We consider only n most probable states for each SET. Drain current is calculated as

$$I = e \sum_{N} \left[P_{N+1} \Gamma_N^{+} - P_N \Gamma_N^{-} \right], \qquad (1)$$

where P_N is the probability that the central node of the SET accommodates N excess electrons. Γ_N^{+} and Γ_N^{-} are the forward and backward tunneling rates across the drain junction. The state of each SET can be calculated independently of those of the other SETs in a circuit because of the condition (ii). As a result, the number of states considered is dramatically reduced compared to that in the low-level simulator.

The condition (ii) is critical to the validity of the SET-SPICE simulation. Figure 6(b) shows the dependence of the error in the output of an inverter circuit (Fig. 6(a)) [11] on the load capacitor $C_{\rm L}$. The error decreases as $C_{\rm L}$ becomes larger because the charging effect arising on the output node is suppressed.

Although SET-SPICE performs simulation on the basis of dc characteristics of SETs, its transient analysis is also valid under the condition (ii). Transient responses of the inverter (Fig. 6(a)) to a step input voltage is simulated as shown in Fig. 7. The discrepancy in the delay time between the results by SET-SPICE and ESS is smaller with a larger $C_{\rm L}$ (Fig. 7(a)). The relatively large discrepancy seen in Fig. 7(b) is because the condition (ii) is not fully satisfied with the small $C_{\rm L}$.

Computation times for the simulations of an inverter chain are shown in Fig. 8 as a function of the number of inverter stages. Solving

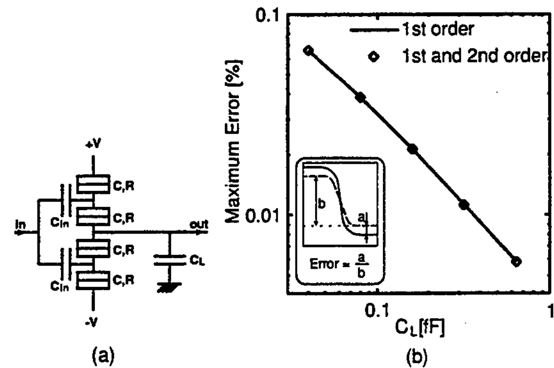

Fig. 6. (a) A complementary inverter circuit [11]. (b) The maximum error in the output voltage versus load capacitance $C_{\rm L}$. Solid line: cotunneling is ignored; squares: cotunneling is considered.

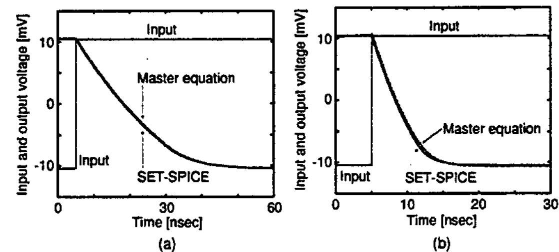

Fig. 7. Transient responses of an inverter to a step input voltage obtained by SET-SPICE (solid line) and ESS solving the master equation (dashed line). (a) $C_{\rm L}$ = 0.64 fF. The maximum error in the delay time is 3 %. (b) $C_{\rm L}$ = 0.16 fF. The error in the delay is 7 %.

the time-dependent master equation by ESS is at least 10^3 times slower than other two methods. Although the computation time for the Monte Carlo simulation is much less than that for the master equation, it grows more rapidly than SET-SPICE. We state that SET-SPICE simulation is the only method applicable to large scale circuits at present.

Since MOSFET device models are built into SPICE, SET-SPICE can simulate circuits consisting of both SETs and MOSFETs. It facilitates the investigation of the interface between the conventional circuits and single-electron circuits. Figure 9(a) shows a test circuit for a co-simulation of SETs and MOSFETs. The simulation results are shown in Fig. 9(b). The output of the NAND gate is buffered by two-stage CMOS inverters, which drive the large output capacitance. The gate capacitance of the first inverter has to be small for the operation speed.

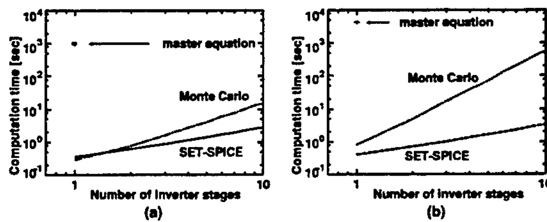

Fig. 8. Computation times for the simulations of an inverter chain using the master equation, Monte Carlo method (one trial) or SET-SPICE. The simulations are performed on a Sun Ultra1/170 clone. (a) Cotunneling is ignored. (b) Two-electron cotunneling is considered.

4 Conclusion

We have proposed techniques of simulation of single-electron circuits. Our low-level simulator ESS has the unique ability to visualize the solution of the master equation. ESS also uses a new algorithm for dc analysis that use the Monte Carlo method to choose the states to be considered prior to solving the steady-state master equation. We suppose this is the best way to perform dc analysis. The high-level simulator SET-SPICE offers high-speed simulation of large-scale circuits consisting of SETs. It is useful for analysis and design of single-electron circuits for real-world applications.

Acknowledgments

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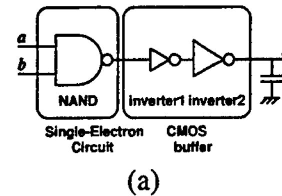
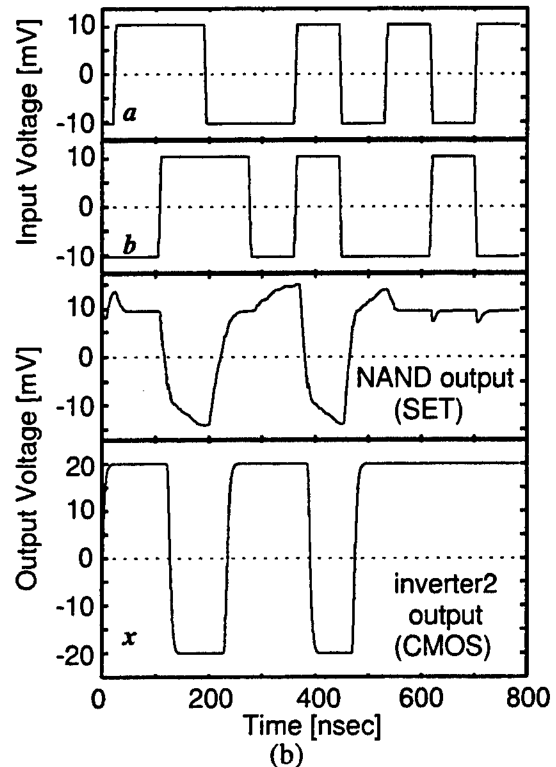


(a)



(b)

Fig. 9. (a) A test circuit for a SET-MOSFET co-simulation. (b) The input and the output waveforms. C_L = 0.16 fF. Gate oxide thickness t_{ox} = 5 nm. Threshold voltages are ∓10 mV for pMOS and nMOS, respectively. Mobilities are $\mu_p = 200$ cm^2/Vs and $\mu_n = 400$ cm^2/Vs. Inverter 1: gate length $L = 50$ nm, gate width $W_p = 0.4$ μm for pMOS and $W_n = 0.2$ μm for nMOS. Inverter 2: $L = 50$ nm, $W_p = 40$ μm and $W_n = 20$ μm.

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SIMULATION OF STRUCTUREL DEFECTS AND THERMAL TENSIONS BY GAUGE FIELD THEORY

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Changes in temperature processes in different plastic flow regions influence upon structure formation of a growing crystal. Because of different conditions the growing structure is not homogeneous and that is why it's deformity has rotational and translation components which are described by gauge field theory. As it is known, there are different gauge field theory versions suggested by different authors [1-4]. In this work we deal with the thermal tension relaxations caused by the polysynthetical twins structure in the silicon ribbons growth by EFG - method. All of the definitions used in the article are identical to those used in [4]. If the new ones occur, they are explained in the text.

Structural defects gauge theory in elastic continuum

Structural defects are treated as results of nonhomogenous Lee-Group influence of gauge transformations $G = GL(3,R) \rhd T(3)$. This group is semilinear product of real nine-parametrical linear transformation group of local basis in solid matter $GL(3,R)$ [5] on one side and translational group of spatial variables that characterize point location $T(3)$ on the other. Matrix form of gauge group Lee is obtained if we inclose three-dimensional space into space with more dimensions [1].

Elastic continuum with defects maps on 4-dimension layered space $L_{4,5}$. 4-dimension Euclide space R_4 form a base in $L_{4,5}$ with local coordinate system $\bar{e}_\alpha, \alpha = 0,1,2,3$, that transfer under coordinate transformations $x^{\alpha'} = x^{\alpha'}(x^\beta)$ according to the law:

$$\bar{e}_{\alpha'} = \frac{\partial x^\alpha}{\partial x^{\alpha'}} \bar{e}_\alpha, \tag{1}$$

Space layer $L_{4,5}$ is a real 5-dimensional space of affine coherency L_5 with local basis $\bar{\psi}_{(\alpha)}, (\alpha) = 0,1,2,3,4$ defined in each point of R_4 with coherent object field $\Gamma_{\beta(\nu)}^{(\mu)}$ and metric tensor components defined by bilinear (scalar in R_4) function $g_{(\alpha)(\beta)} = F(\bar{\psi}_{(\alpha)}, \bar{\psi}_{(\beta)}, x^\gamma)$. Local basis under the point movement from x^β into $x^\beta + dx^\beta$ transfers as follows:

$$d\bar{\psi}_{(\nu)} = \Gamma_{\beta(\nu)}^{(\mu)} \bar{\psi}_{(\mu)} dx^\beta. \tag{2}$$

The gauge group Lee G maps into matrix space (5x5) that operate on local basis:

$$\bar{\psi}_{(\nu')} = M^{-1(\nu)}{}_{(\nu')} \bar{\psi}_{(\nu)}, \tag{3}$$

$$M^{(0)}{}_{(0)} = M^{(4)}{}_{(4)} = 1,\ M^{(i)}{}_{(4)} = b^{(i)},\ M^{(0)}{}_{(i)} = M^{(i)}{}_{(0)} = M^{(0)}{}_{(4)} = M^{(4)}{}_{(0)} = 0. \tag{4}$$

Under the group Lee elements in 4-dimensional subspace of space L_5 tensor components $\varphi^{(\alpha)}$ transform as follows:

$$\varphi^{(0')} = \varphi^{(0)} = x^0,\ \varphi^{(i')} = M^{(i')}{}_{(i)} \varphi^{(i)} + b^{(i')},\ \varphi^{(4')} = \varphi^{(4)} = 1. \tag{5}$$

In this work it is assumed that Latin indexes have values 1,2,3 , Greek without parenthesis - 0,1,2,3 and Greek with parenthesis - 0,1,2,3,4. Time-like components have indexes equal zero while other values go for space components. Transformation law for $\Gamma_{\beta(\nu)}^{(\mu)}$ components can be obtained from eqn. (2) and

invariant matrix has the following zero components: $\Gamma_{\beta(\alpha)}^{(4)} = \Gamma_{\beta(\alpha)}^{(0)} = \Gamma_{\beta(0)}^{(\alpha)} = 0$.

Let $\Gamma_{\beta(4)}^{(i)} = \Theta_{\beta}^{(i)}$.

Spatial components of metric tensor could always be transformed using gauge transformation (3), (4) as

$$g_{(i)(j)} = g_{ij} \quad , \tag{6}$$

where g_{ij} - metric components of tensor R_4. We consider only spatial structure defects so that's why

$$g_{(0)(0)} = g_{00} = -1, \; g_{(0)(i)} = g_{0i} = 0 \, . \tag{7}$$

Eqn. (6) , (7) are true in local basis $\overline{\psi}_{(\alpha)}$ of space L_5 . We will call it a picked basis because it depends upon the choice of coordinate system in R_4 - space.

Field variables $\varphi^{(i)}, \Gamma_{\beta(j)}^{(i)}, \Theta_{\beta}^{(i)}$ describe the elastic continuum with defects. We use distortion tensor components can be used to describe the field $\varphi^{(i)}$ changes under local basis

$$B_{(\beta)}^{(i)} = \nabla_{\beta}\varphi^{(i)} = \frac{\partial}{\partial x^{\beta}}\varphi^{(i)} + \Gamma_{\beta(j)}^{(i)}\varphi^{(j)} + \Theta_{\beta}^{(i)}, \; B_{\beta}^{(0)} = \delta_{\beta}^{0}, \; B_{\beta}^{(4)} = 0, \tag{8}$$

where ∇_{β} denotes the covariant derivative in L_5. Deformity tensor is:

$$u_{\alpha\beta} = \frac{1}{2}(g_{(\mu)(\nu)}B_{\alpha}^{(\mu)}B_{\beta}^{(\nu)} - g_{\alpha\beta}). \tag{9}$$

Let's pick Lagrangian density of elastic continuum with defects as:

$$L = (\mathrm{L}_0 + s_1 L_1 + s_2 L_2)\sqrt{|g|}, \tag{10}$$

$$L_0 = C^{\beta\gamma\mu\nu}(u_{\beta\gamma} - \alpha_{\beta\gamma}T)(u_{\mu\nu} - \alpha_{\mu\nu}T)/2 \quad , \tag{11}$$

$$L_1 = g^{\mu\nu}g^{\beta\gamma}(3\boldsymbol{R}_{\mu\beta,}{}^{(i)}{}_{(j)}\boldsymbol{R}_{\nu\gamma,}{}^{(j)}{}_{(i)} - \boldsymbol{R}_{\mu\beta,}{}^{(i)}{}_{(i)}\boldsymbol{R}_{\nu\gamma,}{}^{(j)}{}_{(j)}) \, , \tag{12}$$

$$L_2 = -g^{\mu\nu}g^{\gamma\delta}g_{(i)(j)}(\nabla_{\gamma}B_{\mu}^{(i)} - \nabla_{\mu}B_{\gamma}^{(i)})(\nabla_{\delta}B_{\nu}^{(j)} - \nabla_{\nu}B_{\delta}^{(j)})/2 \, , \tag{13}$$

where $C^{ijkh} = -c^{ijkh}$, c^{ijkh} - crystal elastic rigidity coefficients ; $C^{0h0k} = \rho g^{hk}$, ρ - material density; $C^{0\alpha ij} = C^{000\delta} = C^{00\alpha\beta} = 0$; $C^{\beta\gamma\mu\nu} = C^{\gamma\beta\mu\nu} = C^{\beta\gamma\nu\mu} = C^{\mu\nu\beta\gamma}$; α_{ij}- crystal heat expansion tensor , $\alpha_{\sigma j} = 0$; ∇_{γ}- operator that denotes the covariant derivative with coherence coefficients $\Gamma_{\gamma\,j}^{\,i} = g^{ik}(\partial_{\gamma}g_{kj} + \partial_{j}g_{\gamma k} - \partial_{k}g_{\gamma j})/2$ for indexes without parentheses and $\Gamma_{\gamma(j)}^{(i)} = \Gamma_{\gamma\,j}^{\,i}$ (in the picked local basis) for indexes in parentheses;

$$\boldsymbol{R}_{\mu\gamma,}{}^{(\alpha)}{}_{(\beta)} = \frac{\partial}{\partial x^{\gamma}}\Gamma_{\mu(\beta)}^{(\alpha)} - \frac{\partial}{\partial x^{\mu}}\Gamma_{\gamma(\beta)}^{(\alpha)} + \Gamma_{\gamma(\xi)}^{(\alpha)}\Gamma_{\mu(\beta)}^{(\xi)} - \Gamma_{\mu(\xi)}^{(\alpha)}\Gamma_{\gamma(\beta)}^{(\xi)} \tag{14}$$

- curvature tensor in affine coherent space L_5.

Lagrangian density (10-13) includes values that have the following physical interpretation:

$\sigma^{ij} = -C^{ijkh}(U_{kh} - \alpha_{kh}T)$ - stress tensor components;

$\sigma^{0h} = 2C^{0h0k}U_{0k}$ - impulse density of a material medium;

$P^{\mu\nu(\alpha)} = sign(g)\varepsilon^{\mu\nu\beta\gamma}\boldsymbol{R}_{\alpha\beta,}{}^{(\alpha)}{}_{(\xi)}\varphi^{(\xi)}/2$ - dislocation density tensor;

$D^{\mu\nu(\alpha)}{}_{(\delta)} = sign(g)\varepsilon^{\mu\nu\beta\gamma}\boldsymbol{R}_{\mu\beta,}{}^{(\alpha)}{}_{(\delta)}/2$ - disclination density tensor;

$\varepsilon^{\mu\nu\beta\gamma}$ - Levi-Civita completely antisymmetric tensor.

Using Lagrangian density (10-13) we can get field equations:

$$\nabla_\eta X^\eta{}_{(h)} = 0,\ \nabla_\eta Z^{\lambda\eta}{}_{(h)} - X^\lambda{}_{(h)} = 0,\ D_\eta U^{\lambda\eta(f)}{}_{(h)} = 0\ , \tag{15}$$

where D_η - covariant derivative operator with coherent coefficients as follows:

$$\Gamma_{\mu(\beta)}^{(\alpha)},\ \Gamma_{\mu\beta}^{\alpha};\ X^\eta{}_{(h)} = \sigma^{\mu\eta} g_{(\alpha)(h)} B_\mu{}^{(\alpha)};\ Z^{\lambda\eta}{}_{(h)} = s_2 2 g^{\lambda\mu} g^{\eta\gamma} g_{(h)(j)} (\nabla_\gamma B_\mu{}^{(j)} - \nabla_\mu B_\gamma{}^{(j)});$$

$$U^{\lambda\eta(f)}{}_{(h)} = s_1 4 g^{\lambda\mu} g^{\eta\gamma} (3 R_{\mu\lambda.}{}^{(f)}{}_{(h)} - \delta^{(f)}{}_{(h)} R_{\mu\gamma.}{}^{(i)}{}_{(j)}).$$

In case of small deformities $B_\mu{}^{(\xi)} \approx \delta_\mu{}^{(\xi)}$ with $\varphi^{(\xi)} = x^\xi + U^{(\xi)}$ from eqn. (15) we can derive equilibrium equation $\nabla_\mu \sigma^{\nu\mu} = 0$ and in case $\Gamma_\beta{}^{(i)}{}_{(j)} = 0$ we get field equations described in [2].

Structure building during the silicon ribbon growth by EFG-method.

Parallel microtwins made out of polycrystal silicon grown by EFG-metod have some advantages when used in sun elements production. Average tangent thermal tensions in polysynthetical region don't reach critical values that cause dislocation formation. Let's analyze the opportunity of getting ribbons with low dislocation densities using the above discussed gauge theory.

Using eqn. (9) , (15) in case of stationary growth regime and insignificant deformations , we get the following equation:

$$\begin{aligned} &S_{bkpt}\Delta\sigma^{pt} + S^i{}_{ipt}(\nabla_b\nabla_k - \frac{1}{2}g_{bk}\Delta)\sigma^{pt} - S^i{}_{kpt}\nabla_i\nabla_b\sigma^{pt} - S^i{}_{bpt}\nabla_i\nabla_k\sigma^{pt} + \\ &+\frac{1}{2}g_{bk}S^{rj}{}_{pt}\nabla_r\nabla_j\sigma^{pt} + \nabla_b\nabla_k\alpha T - \frac{1}{2}s_2(\sigma_{bk} - \frac{1}{2}g_{bk}\sigma^i{}_i - \frac{1}{2}g^{i(l)} * \\ &*(\nabla_b Z_{ki(l)} + \nabla_k Z_{bi(l)})) = 0, \end{aligned} \tag{16}$$

where S_{bkpt} - crystal compliance coefficients; Δ - Laplacian, $\alpha_{ij} = g_{ij}\alpha$, $g^{i(l)} = g^{il}$. Equation (16) transforms into useal thermal tension equation under condition $s_2 \to \infty$.

We assume that ribbon crystallographic surface orientation is (110), direction of growth - $[1\bar{1}2]$ and is opposite to the temperature gradient. Twin borders Σ_3 have orientation $[\bar{1}11]$ and are W_l apart. Local coordinate system orientation in R4 - space is $\vec{e}_1 = \frac{1}{\sqrt{2}}[110],\ \vec{e}_2 = \frac{1}{\sqrt{3}}[\bar{1}10],\ \vec{e}_3 = \frac{1}{\sqrt{6}}[1\bar{1}2]$. Such twins are rotation twins and that is why:

$$\vec{\Psi}_{(r)} = K^i{}_{(r)}\vec{e}_i,\ K^1{}_{(2)} = -K^2{}_{(1)} = \sin\varphi,\ K^1{}_{(1)} = -K^2{}_{(2)} = \cos\varphi,\ K^3{}_{(1)} = K^3{}_{(2)} = K^1{}_{(3)} =$$

$$= K^2{}_{(3)} = 0,\ K^3{}_{(3)} = 1.$$

For Σ_3 border with $y = y_c$ location $\varphi(y) = -\pi\Theta(-(y - y_c))$. From eqn.(2) we can find non-zero components $\Gamma_{2(2)}^{(1)} = -\Gamma_{2(1)}^{(2)} = \Sigma_c \pi\delta(y - y_c)$. Transferring to new variables $\theta_\beta{}^{(s)} = f_\beta{}^{(s)} - \Gamma_{\beta(r)}^{(s)}\varphi^{(r)}$ we will get dislocation density tensor as:

$$P^{0j(h)} = e^{jki}[\frac{\partial}{\partial x^i} f_k{}^{(h)} + \Gamma_{i(l)}^{(h)}\delta_k{}^{(l)} + \Gamma_{i(l)}^{(h)}(f_k{}^{(l)} + \frac{\partial}{\partial x^k}U^{(l)})], \tag{17}$$

where e^{jki} equals 1 if index permutation is even and -1 if it is odd. Second item in brackets (eqn.(17)) characterize twin borders, third and forth - defect generation on those borders. The following boundary conditions are true for ideal borders Σ_3:

$$f_1{}^{(2)} = f_{(3)}{}^{(2)} = f_1{}^{(1)} = f_3{}^{(1)} = 0,\ \frac{\partial}{\partial x^1}U^{(2)} = \frac{\partial}{\partial x^3}U^{(2)} = \frac{\partial}{\partial x^1}U^{(1)} = \frac{\partial}{\partial x^3}U^{(1)} = 0.$$

Using gauge conditions [1] $\nabla_i f^{i(h)} = 0, f^{k(h)} = f^{h(k)} = f^{kh}$, we'll get:

$$\Delta f^{kh} = \frac{\sigma^{kh}}{2s_2},\ Z_{ki}^{\ (h)} = 2s_2(\frac{\partial}{\partial x^i} f_k^{\ (h)} - \frac{\partial}{\partial x^k} f_i^{(h)}). \tag{18}$$

Coefficients $\Gamma_{\mu(\beta)}^{\ (\alpha)}$ satisfy field equations. can be obtained Substituting (18) into (16) we get equation for f^{kh} . From (18) we derive σ^{kh} . The approximate solution for thin plane ribbon with low density is:

$$f^{23} = A(y-y_l)(7-40Y^2+48Y^4)T'''(z), \tag{19}$$

$$f^{33} = -A(7-120Y^2+240Y^4)T''(z), \tag{20}$$

$$f^{22} = -A[(\frac{7}{2}-10Y^2+8Y^4)(y-y_l)^2 T''''(z)+8T''(z)]. \tag{21}$$

where $A = \frac{\alpha \bar{E} W_l^4}{s_2 1{,}152 \cdot 10^4}$; $Y = (y-y_l)/W_l,\ y \in [y_l - \frac{W_l}{2}, y_l + \frac{W_l}{2}]$; y_l – twin-block center coordinate. Expressions obtained for σ^{33}, σ^{23}, σ^{22} are identical to ----those found in [5]. $\bar{E}$ = 2,52· ·10^7 N·sm^-2 - value is greater than Young's modulus $E = S_{11}^{\ -1} = 1{,}3 \cdot 10^7$ N·sm^{-2} .

Let's find tangent tensions in the main system of sliding planes and decompose dislocation density tensor (17) into system elements. Maximum tangent tension value τ arise in the twin borders neighborhood:

$$\tau = \left|\tau_{[0\bar{1}1](111)}\right|_{max} = \frac{\alpha E W_l^2 T''}{12\sqrt{6}}. \tag{22}$$

CONCLUSION

The twinning borders formation, occuring in the plastic flow region during crystal growth, was explained by the means of gauge field theory using geometrical reasoning.

Dislocations develop under the thermal tensions influence in case $\tau > \tau_{critical}$. Near crystallization front under the temperature $T_0 \approx 1688$ K the critical tension value for dislocation formation in Si is $\tau_{critical} = (5 - 10) \cdot 10^{-3}$ N·sm^{-2}. In the observed technological process $T'' \approx 10^3$ Deg·sm^{-2} . Taking $\alpha = 4{,}15 \cdot 10^{-6}$ Deg^{-1} and substituting eqn. (22) into condition $\tau < \tau_{critical}$, we'll get $W_l < 0{,}12$ sm. Twin border distance in Si ribbon is no greater than 0,1 sm. Hence twinning effect is responsible for thermal tension fall.

Obtained approximate solution is true if $\frac{EW^2_{l\,max}}{48 s_2} << 1$. Thus we get thermoelastic theory transfer conditions : $s_2 >> 5{,}25 \cdot 10^3$ N . In this case for the main system sliding planes elements dislocations boundary densities have small values that is $N_{max} << 10^3$ sm^{-2} .

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Two-Dimensional Electron-Hole Plasma on the Si Surface.

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A new line of the recombination luminescence of the non-equilibrium electron-holes pairs connected with the surface charge layer in semiconductor structures have been widely studied experimentally [1-3]. It is shown that the new line of the luminescence is the result of recombination of non-equilibrium two-dimensional electrons and holes.

This paper deals with density-functional calculations of electron structure of two dimensional electron-hole plasma (2D EHP) on the Si surface. We use a simple two-band model taking into account electrons and heavy holes. The ground-state energy is written as a functional of the electron and hole densities. The total energy of the electron-hole system is taken to be:

$$E_t = T[n_e,n_h] + E_c[n_e,n_h] + E_{xc}[n_e,n_h] \quad (1)$$

Here T is the kinetic energy of the electrons and holes, E_c is Coulomb energy, E_{xc} is the exchange-correlation energy.

In this paper we use excitonic units: Ry=e^2/2ka, a=k$h^2/\mu e^2$, where k is the static dielectric constant of Si and μ is the optical mass

The variational problem [Eq. (1)] is equivalent to finding the self-consistent solution of Kohn-Sham equations for the electrons and holes (the z axis is taken to be perpendicular to the surface)

$$\left(-\frac{\mu}{m_i}\frac{d^2}{dz^2} + V_{eff,i}(z)\right)\psi_{n,i}(z) = E_{n,i}\psi_{n,i}(z)$$

where $i=e,h$

The self-consistent potentials $V_{eff,i}$ are given by

$$V_{eff,e} = V_c + V_{xc,e}$$

$$V_{eff,h} = -V_c + V_{xc,h}$$

The Coulomb potential V_c is obtained from Poisson equation:

$$\frac{d^2V_c}{dz^2} = 8\pi\left(n_e(z) - n_h(z)\right)$$

with boundary condition:

$$\frac{dV_c}{dz}\Big|_0 = 8\pi N_s, \quad \frac{dV_c}{dz}\Big|_\infty = 0,$$

where $N_s = N_e - N_h$

N_e, N_h - 2D electron and hole density

We consider the lowest electron and hole states to be occupied, that is

$$n_e(z) = N_e\psi^2_{0,e}(z), \quad n_h(z) = N_h\psi^2_{0,h}(z)$$

The exchange-correlation potential is written as

$$V_{xc,i}(z) = \frac{\delta E_{xc}[n_e,n_h]}{\delta n_i(z)}$$

We use the local-density approximation for exchange-correlation energy (per unit area):

$$E_{xc}[n_e,n_h] = \int dz e_{xc}(n_e,n_h)$$

Here $e_{xc}(n_e,n_h)$ is the exchange-correlation energy per unit volume.

We use a simple approximation for $e_{xc}(n_e,n_h)$:

$$e_{xc}(n_e,n_h) = \left[\varepsilon^G_{xc}(n_e)n_e + \varepsilon^G_{xc}(n_h)n_h\right]f(y) + \frac{1}{2}\left[1-f(y)\right]\left[\varepsilon^L_{xc}(n_e)n_e + \varepsilon^G_{xc}(n_h)n_h\right]$$

where $\varepsilon^L_{xc}(n_i)$ and $\varepsilon^G_{xc}(n_i)$ are the energy per particle in the limits of $n = n_e = n_h$ and $n_{e(h)} \to 0$, respectively,

$$y = \frac{n_e - n_h}{n_e + n_h}.$$

For $f(x)$ we took the same expression as it was taken in [4].

The exchange-correlation energy for the neutral system is approximated by [5]

$$\varepsilon_{xc}^{L} = \frac{1}{2}\frac{a+br_s}{c+dr_s+r_s^2}$$

We take ε_{xc}^{G} of the form

$$\varepsilon_{xc}^{G} = -(24/\pi g_v)^{1/3}[\frac{3}{4}n_i^{1/3} + \frac{3}{28}g_v^{2/3}n_i^{1/6}]$$

where g_v is the valley occupancy.

In this paper we use an iteration technique to solve Kohn-Sham equations self-consistently.

The energy levels, effective potentials and density profile of the photoinduced carriers are calculated. Figure 1 shows the wave functions and effective potential for Si surface (100), where the first layer consisted of holes, while the second one of electrons.

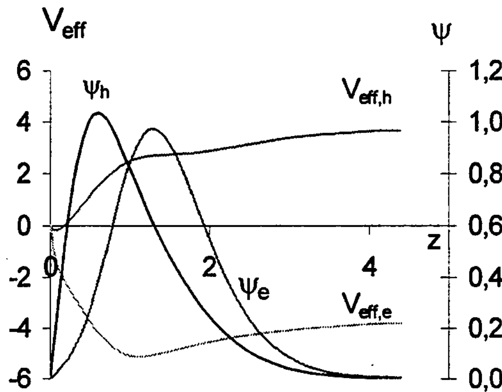

Fig.1 Effective potentials and wave functions along the direction perpendicular to the surface for $N_s=10^{12}$ cm^{-2}

In order to show the capability of creation of the second (electronic) layer, one must calculate the binding energy:

$$\Delta = \frac{E_t(N_e, N_h) - E(0,N_s)}{N_e}$$

Figure 2 demonstrates the dependence of binding energy upon electron density N_e for different N_s.

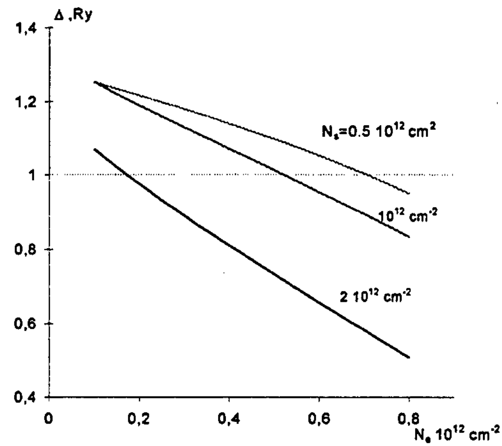

Figure 2. The dependence of the binding energy on electron density of the second layer.

We see that there are densities N_e where 2DEHP is the ground state.The decrease in the binding energy with increasing density N_e (or N_s) is due to the increase of the kinetic energy along a surface of a semiconductor. The stable state of 2DEHP can be observed in the wider area of density for surface with the large value g_v.

In conclusion, the local density-functional method has been used to study structure of 2DEHP. Results show that 2DEHP can exist on the Si surface. It is a clean way to obtain and study a plasma in two-dimensions.

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Analysis of Floating Body Effect in Non-fully Depleted SOI MOSFET's based on Capacitive Coupling

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Abstract

Transient floating body effect in SOI MOSFET's has been shown to be problematic by many researchers [1-3]. Most of the transient effects reported are a direct result of capacitive coupling (CC), but it is not known whether the simple capacitance models used in SPICE models are accurate enough to predict the floating body voltage. In this paper, a comprehensive analysis on capacitive coupling effect in non-fully depleted (NFD) SOI MOSFET is presented. SPICE Level 2 model is compared with 2-D device simulations and the accuracy is discussed for long and short channel devices.

Theoretical Analysis

Fig. 1 shows an example of transient response induced by a gate voltage step in a floating body device. Since the amount of majority carriers is conserved in a short time period, V_B is modulated by CC at the beginning. But on a larger time scale, V_B is controlled by body currents. The time to steady state is ranging from micro-second to second unless the impact ionization current is at a high level [2]. Therefore, CC is normally the dominant effect within a short transient. Fig. 2 shows the equivalent capacitance network for coupling analysis. By assuming the total body charge Q_{Btot} is a constant, the front gate, source and drain coupling factors

$$P_{FGC} = -\frac{C_{Bf,Gf}}{C_{Btot,B}},\ P_{BGC} = -\frac{C_{Bb,Gb}}{C_{Btot,B}},$$

$$P_{SC} = -\frac{C_{Bf,S} + C_{Bs,S}}{C_{Btot,B}},\ P_{DC} = -\frac{C_{Bf,D} + C_{Bd,D}}{C_{Btot,B}} \quad (1)$$

For a long channel and infinitely thick buried oxide device, the junction capacitance and buried oxide capacitance are negligible. Then the coupling factors are simplified to

$$P_{FGC} = -\frac{C_{bg}}{C_{bb}},\ P_{SC} = -\frac{C_{bs}}{C_{bb}},\ P_{DC} = -\frac{C_{bd}}{C_{bb}} \quad (2)$$

where ($C_{Bf,Gf}$, $C_{Bf,S}$, $C_{Bf,D}$, $C_{Bf,B}$) are renamed as (C_{bg}, C_{bs}, C_{bd}, C_{bb}) for simplicity. Since these capacitances are well developed within bulk device physics, the CC effect can be predicted by using bulk model. SPICE Level 2 model was selected for this study.

Simulation Result

Before the analysis, the SPICEL2 model parameters were firstly extracted from the current characteristic of a long channel device simulated by MEDICI. Fig. 3 and 4

plots P_{FGC} as a function of V_G and P_{SC} / P_{DC} as a function of V_D. In subthreshold region, P_{FGC} is always equal to 1 because the drain and source do not couple to the body. In the strong inversion region with zero drain voltage, gate coupling is shielded by inversion layer and hence P_{FGC} is zero. The bulk charge is equally shared by source and drain and therefore P_{DC} and P_{SC} must be equal to 0.5. As V_{DS} increases, drain coupling gets weaker while source coupling becomes stronger. P_{DC} drops to zero upon reaching saturation region and P_{SC} increases to 0.75. In saturation, the gate is still coupled to body through the modulation of drain saturation voltages and P_{FGC} is about 0.25. Source coupling is very strong throughout the strong inversion region.

Circuit simulation using the SPICEL2 model is performed. The floating body configuration is formed by attaching the buried oxide capacitance to the body. The MOSFET models have no internal parasitic. Impact ionization model is disabled. The circuit simulation is compared with MEDICI simulation for gate and drain ramping transient as shown in Fig. 5 and 6. The data agrees very well in both cases.

As channel length scales down, source and drain junction capacitances become significant. By attaching a proper body-source and body-drain diode to the SPICE Level 2 MOSFET model, the coupling factors as a function of channel length can be calculated. The calculated values agree with MEDICI simulation as shown in Fig. 7 to 9. In short channel devices, junction capacitances dominates over the front channel bulk capacitances. Then gate coupling becomes weaker while source and drain coupling become stronger. Fig. 10 (b) shows the SPICE simulated body voltage fluctuation of two NMOSFET's within a typical inverter cycle as shown in Fig. 10 (a). Fig. 10 (c) shows the charge distribution inside a L=0.6μm device during the inverter cycle. Since the total charge Q_{Btot} is conserved, V_B always returns to its initial value after one cycle. Severe instability in circuit operation can be induced by drain coupling in deep submicron devices unless sufficiently low supply voltage is used.

Conclusion

The transient body voltage fluctuation can be accurately modeled with the available transistor and diode capacitance models as shown in this paper. Therefore, accurate simulation of complex SOI circuits using SPICE is a realistic goal. However, the chosen capacitance models must be verified with device simulators as shown in this paper.

Acknowledgements

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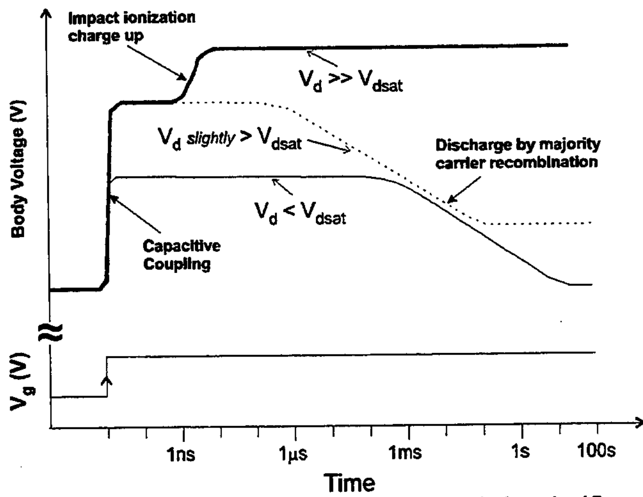
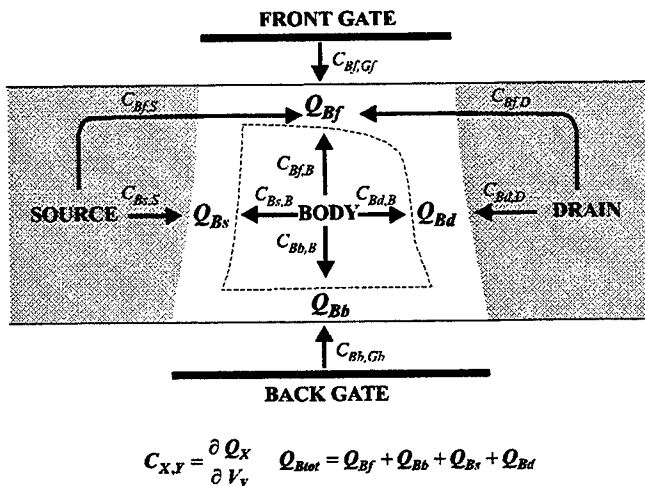


Fig 1 A transient example to illustrate the relative significance of various floating body effects along the time axis. The body voltage is plotted versus time when a gate voltage step is applied under various standby drain bias.



$$C_{X,Y} = \frac{\partial Q_X}{\partial V_Y} \qquad Q_{Btot} = Q_{Bf} + Q_{Bb} + Q_{Bs} + Q_{Bd}$$

Fig. 2 Equivalent capacitance network in a NFD SOI MOSFET for 2-D coupling analysis. The relationship between the body charges and capacitances are clearly illustrated.

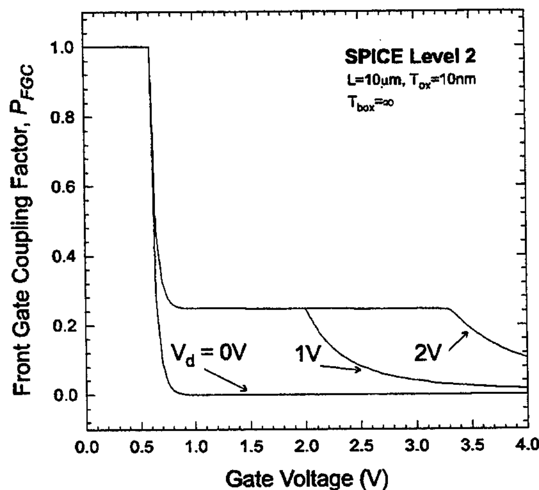


Fig. 3 P_{FGC} versus gate voltage at various drain bias for long channel devices with infinite thick buried oxide. The result is calculated by SPICE Level 2 model.

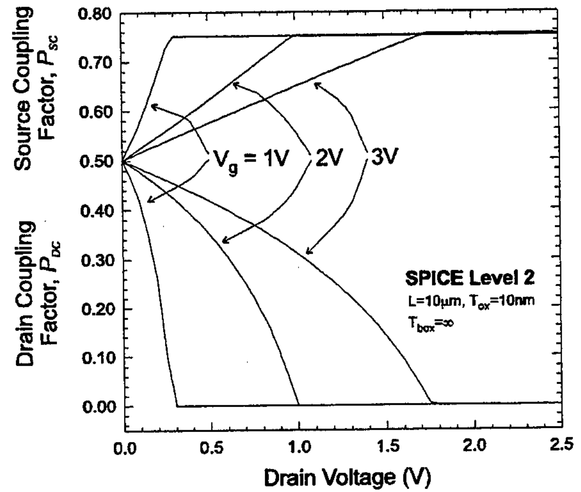


Fig. 4 P_{DC} and P_{SC} versus drain voltage at various gate bias for long channel devices with infinite thick buried oxide.

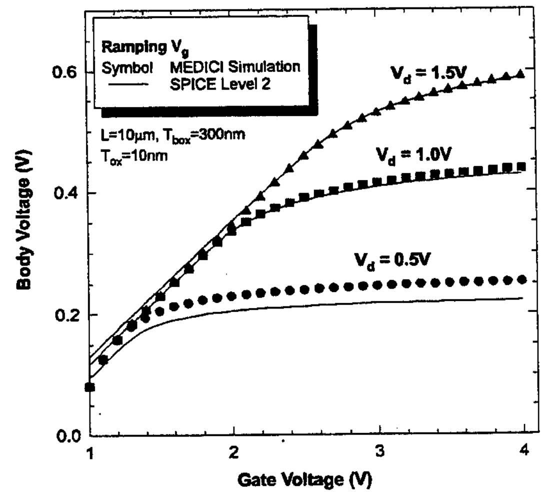


Fig. 5 Body voltage fluctuation upon a front gate voltage ramp for a L=10μm NFD SOI MOSFET at different drain bias.

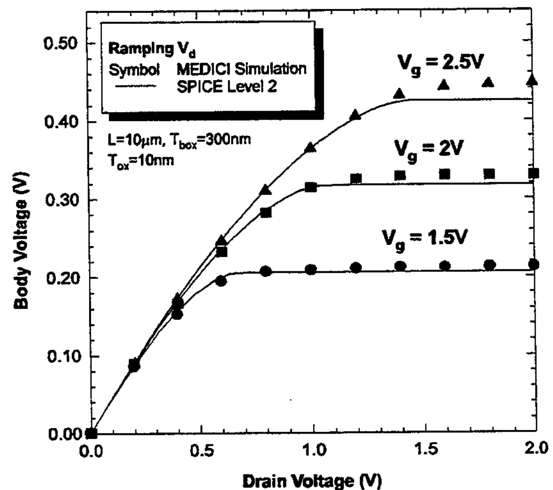


Fig. 6 Body voltage fluctuation upon a source voltage ramp for a L=10μm NFD SOI MOSFET at different gate and drain bias.

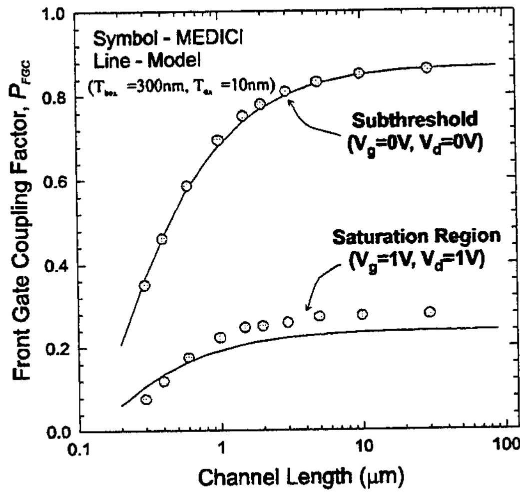


Fig. 7 Front gate coupling factor (P_{FGC}) versus channel length in subthreshold and saturation regions.

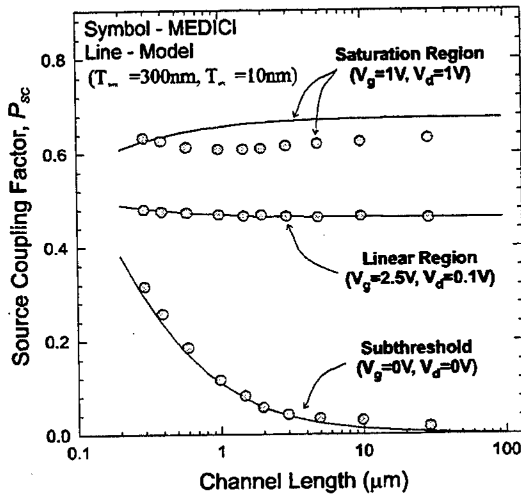


Fig. 8 Source coupling factor (P_{SC}) versus channel length at subthreshold, linear and saturation regions.

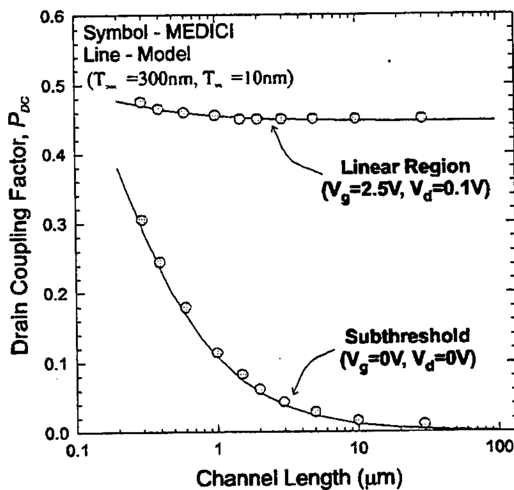


Fig. 9 Drain coupling factor (P_{DC}) versus channel length at subthreshold and linear regions.

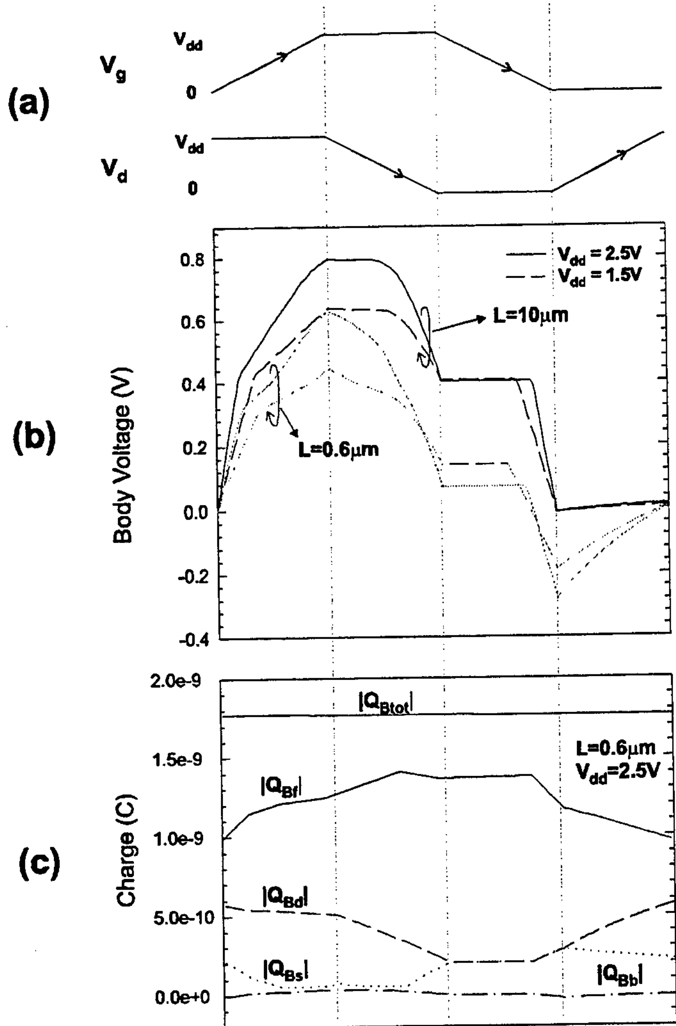


Fig. 10 SPICE simulated body voltage fluctuation of a NMOSFET within a typical inverter cycle. (a) The gate and drain voltages. (b) V_B fluctuation for two NMOSFETs with L=10μm and 0.6μm at V_{DD}=1.5, 2.5V. (c) Body charges distribution in a L=0.6μm device at V_{DD}=2.5V.

A Unified Approach for the Modelling of SAGCM InGaAs/InP Avalanche Photodiodes

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Separate absorption, grading, charge, and multiplication (SAGCM) (shown in Fig.1 with details of device parameters in Table 1) is one of the widely used structures for InP/InGaAs avalanche photodiodes (APDs) in long-distance high data-rate fiber-optical telecommunication systems.

There are several reports of the modelling of SAGCM APDs. But, in all these works, modelling is done separately for each characteristics of APDs like multiplication gain (M) against bias (V), breakdown voltage (V_{br}) or gain as a function of temperature, bandwidth (BW) as a function of gain etc. The problem in such segmented approach is that it requires separate calibration for each of the device characteristics. For example, the calibration for the model of M-V relation with respect to the measured unity gain voltage at each temperature shows mismatch with the model calibrated to the measured bandwidth -gain characteristics (because this involves a separate calibration to calculate the carrier trapping effect corresponding to each gain.).This is undesirable for developing an efficient device simulator. Here, we present a unified approach for the modelling of SAGCM APDs where V_{br}, M-V, their temperature dependence, bandwidth -gain characteristics are all studied using the same model.The model is also generalized and can be applied to a variety of other APD structures.

The present model is based on a stochastic approach. In this model, the first step is to calculate the time impulse response. The multiplication gain (M) at any bias (V) is calculated from the impulse response by taking the ratio of the area under the response curve and the area under the curve obtained with ionization coefficient for electron (α) and hole (β) put to zero. The breakdown voltage corresponds to the minimum value of the voltage at which the impulse response diverges. The frequency response of the APD is calculated from the Fast Fourier Transform of the impulse response. We multiply the above fre-

quency response with the frequency response due to RC time constant $1/(1+\omega^2R^2C^2)^{1/2}$, and then calculate the 3dB electrical bandwidth.

The impulse response is calculated starting from the distribution of initial photogenerated carriers and using a time recurrence relation for the distribution of electrons and holes. The recurrence relation is derived using a simplified time domain stochastic analysis of avalanche multiplication process. The current density is evaluated from eqn.1, where $n^e(i,j)$ and $n^h(i,j)$ are electron and hole densities in the ith mesh and at jth interval, v^e and v^h are respective velocities and w is the thickness of the active region. The algorithm is based on a discrete time setting to be ideally suited for computer modelling. We have incorporated carrier trapping effect at the InGaAs/InP hetero-interface in our stochastic algorithm which is a major factor determining the BW at low values of gain. Fig.2 shows impulse response curves calculated at different gains. One can clearly see from Fig.2, the delayed response due to secondary electrons generated from the primary holes initially trapped at the hetero-interface at M=2.2 and M=2.45.

Fig.3 shows the measured and calculated M-V curve at room temperature. The above model is then used to calculate the 3dB BW as a function of gain. The results are shown in Fig.4. To test the validity of the above model at different temperatures, we calculate V_{br} and M at a bias of $0.9V_{br}$ using the conventional expression for gain (eqn.2) and the present model over a temperature range of -35^0C to 85^0C (Fig.5) for a separate device having $x_d=0.5\mu m$ and $x_{absorp}=3.2\ \mu m$. For this calculation, we have used the well-known Okuto-Crowell expressions (eqns.3 and 4) for α and β. The values of ionization parameters λ_0, E_{r0}, E_i used in the calculation are listed in Table 2. The good agreement between the calculated values using the present model and measured data for V_{br}, M-V, bandwidth-gain indicates that the present approach can be applied to model the above characteristics of SAGCM APDs over different temperatures. The model can be further extended to model excess noise factor and the temperature dependence of gain-bandwidth product also.

In conclusion, a unified approach to model different characteristics of SAGCM APDs is developed which can be used for different APD structures and at different temperatures and can be used to develop an efficient APD simulator.

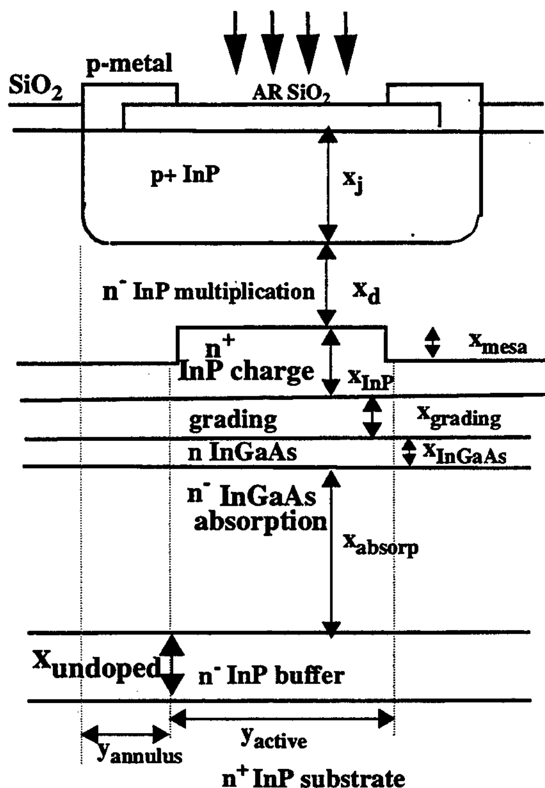

Fig.1 Schematic layer structure of InGaAs/InP SAGCM APD

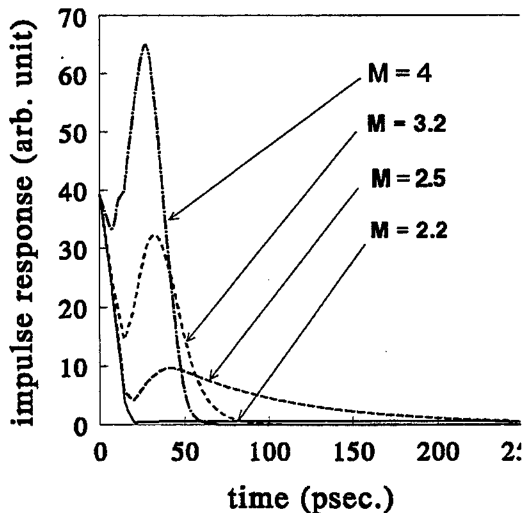

Fig.2 Calculated Impulse response of SAGCM APDs at different gains.

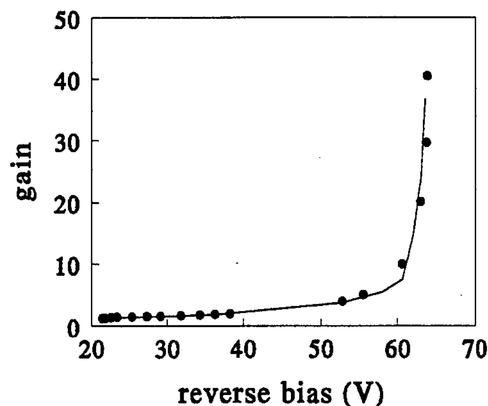

Fig.3 Measured (circle) and calculated (solid line) M-V data for SAGCM APD at 1.3 μm at room temperature.

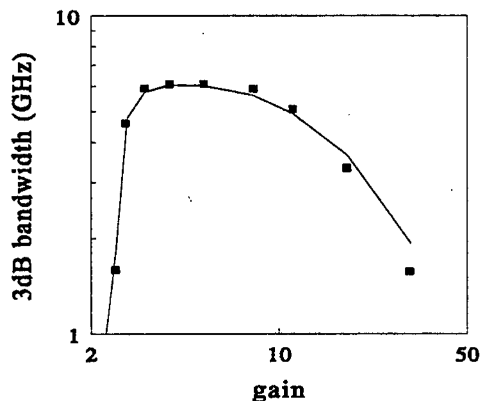

Fig.4 Measured (circle) and calculated (solid line) bandwidth-gain characteristics for SAGCM APD at room temperature.

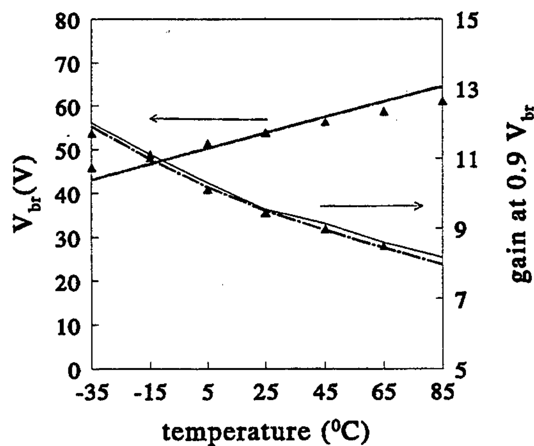

Fig.5 Measured (triangle) and calculated (dash line using eqn. 2, solid line using stochastic model) Vbr and gain at 0.9 Vbr as a function of temperature.

$$J(j\Delta t) = \frac{1}{w}\sum_i q\{n^e(i,j)v^e(i) + n^h(i,j)v^h(i)\} \quad (1)$$

$$M = \exp\frac{\left\{\int_0^w (\beta - \alpha)dx\right\}}{1 - \int_0^w \alpha \exp\left\{\int_0^x (\beta - \alpha)dx'\right\}dx} \quad (2)$$

$$\alpha, \beta = \frac{qF}{E_i}\exp\left\{0.217\left(\frac{E_i}{E_r}\right)^{1.14} - \sqrt{\left[0.217\left(\frac{E_i}{E_r}\right)^{1.14}\right]^2 + \left[\frac{E_i}{qF\lambda}\right]^2}\right\}. \quad (3)$$

$$\lambda = \lambda_0 \tanh\left(\frac{E_{r0}}{2kT}\right) \quad (4)$$
$$E_r = E_{r0}\tanh\left(\frac{E_{r0}}{2kT}\right).$$

Fig.6 Equations used in the text

Table 1: Nominal device parameters

y_{active}	30 μm	$y_{annulus}$	5 μm
x_{mesa}	0.11 μm	x_j	2.5 μm
x_{InP}	0.17 μm	$x_{undoped}$	0
$x_{grading}$, N_G	0.09μm, ~10^{16} cm^{-3}	x_{absorp}	1.0 μm
x_{InGaAs}, N_{InGaAs}	0.02 μm $2x10^{17}$ cm^{-3}	n^--InP, n^--InGaAs	$10^{15}cm^{-3}$

Table 2: The values of ionization parameters used in eqns. 3 and 4.

	E_i (eV)	E_{r0} (meV)	λ_0 (A^0)
α	1.84	46	41.7
β	1.65	36	41.3

Main Parameters of Turn-on Process in 4H-SiC Thyristors

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1 Introduction

SiC thyristors can find use in superhigh voltage and superhigh current systems as well as in high temperature and radiation hard electronics. Recently, 4H-SiC thyristors with high enough forward blocking voltage $V_b \sim 400$ V and rather low residual voltage drop at high forward current density have been produced [1]. The main parameters of turn-on process: time constant of current rise τ_r, critical charge density n_{cr}, and residual voltage drop during turn-on process $V_R(t)$ have been investigated in these 4H-SiC thyristors. The critical current density j_o below which the turn-on state occupies only part of the thyristor's area has been estimated theoretically and experimentally. While theoretical calculations predict its value to be $2{\cdot}10^2$ A/cm^2, experimental results show a range of $3{\cdot}10^2$ to $7.6{\cdot}10^2$ A/cm^2.

2. Experimental details.

The device structures of npnp 4H-SiC thyristors investigated here were identical in design to the structures described in detail in Ref.[1]. The voltage blocking p-layer was 4.5 μm thick and had an acceptor doping concentration $N_a - N_d = 2.8 \cdot 10^{16}$ cm^{-3}. The n-base had a thickness of 0.55 μm and a doping concentration of $4.5 \cdot 10^{17}$ cm^{-3}. The active area of the devices was $S = 3.6 \cdot 10^{-4}$ cm^2. The turn-on process was investigated in a low inductance circuit with a series load resistance $R_l = 50$ Ohm.

3. Results and analysis

3.1. Turn-on process. The time dependences of the voltage across the load resistance, $V_R(t)$, during turn-on process are shown in Fig.1 for different temperatures and for a forward blocking bias $V_O = 30$ V. The steady state current density j_o, attained after the turn-on process terminates, is equal to $V_{Rs}/(R_l \cdot S) = 1400$ A/cm2, where V_{Rs} is the steady state voltage drop across the load resistance R_l at the end of turn-on. At $j = 1.4{\cdot}10^3$ A/cm^2 the V_{Rs} depends only slightly on tempe-rature, being equal to ~25.5 V over the whole temperature range 160 <T< 500 K. Accordingly, the residual voltage drop across the thyristor structure $U_{TSO} = V_O - V_{Rs} = 4.5$ V for all temperatures.
It can be seen from Fig.1 that the turn-on process is strongly temperature dependent, especially at T < 300 K. The total turn-on time is about 180 nsec at 160 K and only about 10 nsec at 495 K.

The $V_R(t)$ dependences shown in the figure have a qualitatively usual form: a relatively fast exponential rise of current ($I = I_o \cdot \exp(t/\tau_r)$), followed by a slower part where the second derivative of current changes sign. The inset in Fig.1 shows the temperature dependence of τ_r . It is seen that τ_r decreases monotonically with temperature increasing from τ_r = 63 nsec at T = 160 K to τ_r = 1.9 nsec at T = 495 nsec. As far as we know τ_r = 1.9 nsec is the minimum τ_r value observed for SiC thyristors.

3.2. Critical charge density . The concept of the critical charge density was put forward in Ref. [2] and developed in Refs. [3, 4]. The critical charge density of a thyristor determines the maximum voltage ramp (dV/dt) of the thyristor [4], the minimum value of the gate control current density [5], the spread velocity of the "on" state [6], the holding current, and the parameters of current filamentation in gate-controlled thyristors [7].

To determine the critical charge density the "dV/dt technique" was used. A forward dc voltage V_o was applied to the thyristor. Then, an additional pulse of amplitude ΔV (rise time < 1 nsec) was applied. The minimum value of ΔV sufficient to turn on the thyristor was registered. The magnitude of the charge appearing in both bases of the thyristor Q_{cr} is equal to

$$Q_{cr} = \int_{V_o}^{V_o+\Delta V_c} C_{jc}(V)dV \qquad (1)$$

where C_{jc} is the capacitance of the central (collector) pn junction . The critical charge density n_{cr} was calculated according to the well known equation:

$$n_{cr} = Q_{cr} / e \cdot S \cdot W_n \qquad (2)$$

The $C_{jc}(V)$ dependence was measured at a frequency of 1 kHz in the range of forward voltage $0 < V_0 < V_b$ with an accuracy of 10^{-2} pF.

At T > 550 K and forward voltage V_o > 5V, the dV/dt switching in 4H-SiC thyristors is qualitatively analogous to the dV/dt effect in Si and GaAs thyristors. [8]. The critical charge value for the SiC thyristor is rather small : Q_{cr} = 5.2 pC at V_o = 5 V and Q_{cr} = 0.32 pC for V_o = 100 V. However, due to small n-base thickness (Wn = 0.55 μm) and very small thyristor area ($S=3.6\ 10^{-4}\ cm^2$) the critical charge density is sufficiently high: $n_{cr} = 1.5\ 10^{15}\ cm^{-3}$ at V_o = 5V and $n_{cr} = 10^{14}\ cm^{-3}$ at V_o = 100 V.

At T < 450 K the dV/dt effect has been found to be anomalous within the whole range of the V_o values for a SiC thyristor. The possible reasons of this anomalous behaviour have been discussed.

3.3. Transient current-voltage characteristics. Fig. 3 shows non-eqiulibrium current-voltage characteristics of the 4H-SiC thyristor under test at sevral time intervals after turn-on of the device. It can be seen from this figure that the residual voltage decreases very rapidly to the steady state value. The residual drop voltages in the device settle to steady state value in 50-100 nsecs after turn on even when at high current density about $5 \cdot 10^4$ A/cm². The duration for this

process is comparable to the current rise time at 300 K. Curve 3 of Fig. 3 corresponds practically to the steady-state current-voltage characteristic.

3.4. Critical current density j_o

It is known there exists a critical current density j_o at which the turned-on state does not spread and occupies only part of the structure. Under this condition, the critical density of minority carrier charge in the thin base of the thyristor
$n_o \approx 2 n_{cr}$ [6]. For GaAs and Si thyristors, the relationship between j_o and n_{cr} has been investigated in [9].

The value of j_o has been estimated using the simplest model [6, 10]. It is assumed that in the turned-on state the minority carrier concentration n_o is constant along the thyristor bases. For thin n-base of the thyristor, one can assume that the common-base current gain α is equal to 0.8. Using the usual expression for the common base circuit configuration gain, it is easy to obtain the hole lifetime in the base of the thyristor: $\tau_p \approx 3.8 \cdot 10^{-9}$ s ($D_p = 2$ cm^2/s). To estimate the electron lifetime in the wide thyristor base τ_n, one can assume the usual relation between wide base width W_p and electron diffusion length L_n : $W_p/L_n = 3$. Using the electron diffusion coefficient $D_n = 15$ cm^2/s, a τ_n of $1.5 \cdot 10^{-9}$s was derived. Taking a value of n_{cr} to be 2 10^{15} cm^{-3} (see Fig. 2), we obtain a j_o value of $2 \cdot 10^2$ A/cm^2.

If the anode current value I_a is low enough (< 15 mA), the on-state occupies only part of the area of the structure. This can be judged from the recombination radiation [9, 11] which lies for SiC in visible part of wavelengths. The radiation can be observed easily through an optical microscope. Knowing the anode current value and the area of the on-state S, one can find the j_o value. The experimental values of j_o fall in the range of $3 \cdot 10^2$ A/cm^2 and $7.5 \cdot 10^2$ A/cm^2. Taking into account the qualitative character of the theoretical model an agreement between theoretical and experimental estimations are quite satisfactory.

Acknowledgements

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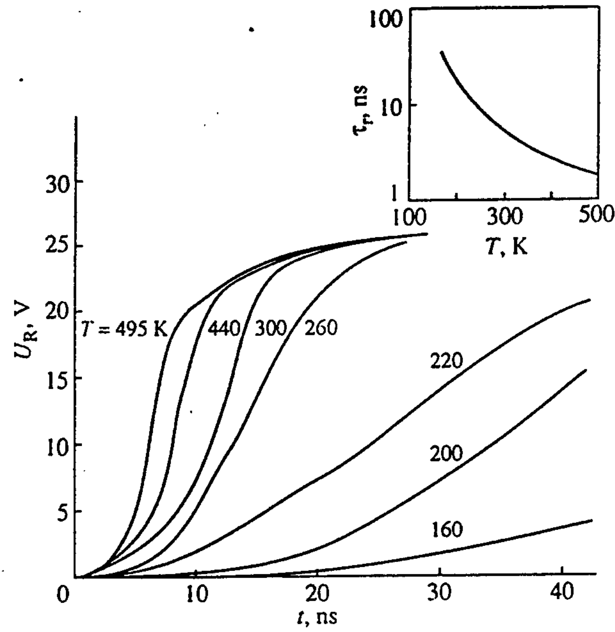

Fig.1. The time dependences of the voltage across the load resistor Rl =50 Ohm during the turn-on process at different temperatures. UO = 30 V. Inset shows the temperature dependence of the time constant of current rise tr .

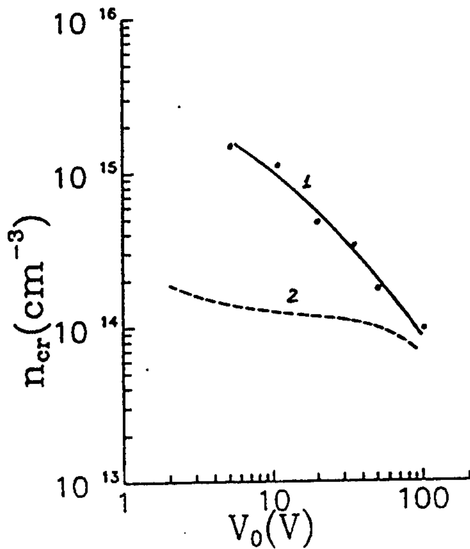

Fig. 2. The dependencies of the critical charge density ncr versus forward voltage Vo. 1 - 4H-SiC thyristor, 560 K 2. GaAs thyristor, 300K.

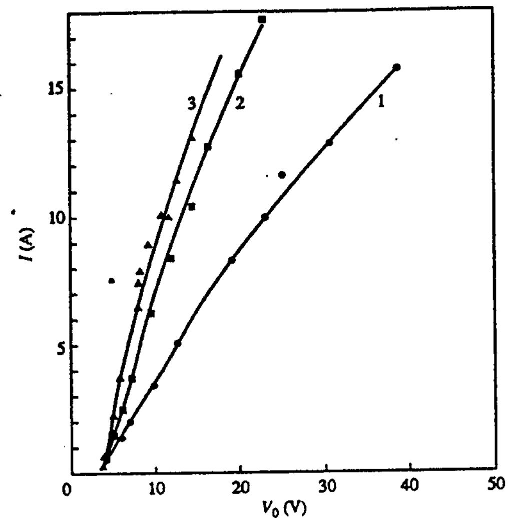

Fig.3. Transient current-voltage characteristics of 4H-SiC thyristors at different intervals after turn-on of the thyristor.
Time: 1-20ns, 2-50ns, 3->100ns. 300K.

On dramatic influence of localization on strong field transport phenomena in silicon carbide polytypes

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The Wannier-Stark localization (WSL) is a complicated process developing in a broad range of electric fields and leading to the energy spectrum transformation and replacement of the band spectrum by a system of energy levels, so-called Wannier-Stark ladder. This problem is important from the both fundamental and applied points of view.

The results presented in this paper are different, but they are reflection of the same phenomenon namely WSL. In particular we will discuss the impact ionization specificity, the different I–V charactiristics of silicon carbide polytypes in the WSL regime and the saturated drift velocities in polytypes with different superstructure parameters for the electric field direction along the crystal axis or the superlattice (SL) axis, $F \parallel C$.

Earlier in our articles [1, 2] the results were presented which allowed to suppose that impact ionization at $F \parallel C$ was characterised by the practical absence of the electron component. But spicifical experimental difficulties did not allow to prove this supposition by direct observation of the electron impact ionization process because the conditions of pure electron exitation could not be provided at that time. The study of current-field characteristics of SiC for fields higher than 10^5 V/cm is a complicated problem because of the high electronic injection and high current density. Besides the electronic component of current should be separated from the hole component since the latter does not exhibit the behaviour inherent for WSL [1]. All these problems have been solved after the development of special tree terminal experimental structure allowing to control the current injected independently of the electric field and to make an electric field in the sample uniform [3].

Besides this experimental structure is available for investigation of impact ionization specificity because it allows to realize the impact ionization exitation by pure electron current. In this case a pulse and a direct voltage was applied to the emitter and collector of the structure. The direct voltage has provided an electron injection from the emitter and a high field in collector and pulse voltage has provided a transport of electrons through a base in coollector. An increase of pulse current was occured during the increase of direct voltage. These changes of the pulse current can be caused by both the change of the injection level and impact ionization in collector region. The monotoneous character of these changes presented in Fig. 1 says that it is evidently induced by the first reason because the impact ionization is characterized by a much sharper current increase. Besides the peculiarities with NDC which arise on I–F characteristics at more strong fields are the results of electro-phonon resonances in the Wannier-Stark ladder regime [4]. It is the main evidence that the electron component of impact ionization is not observed up to the fields almost 5000 kV/cm.

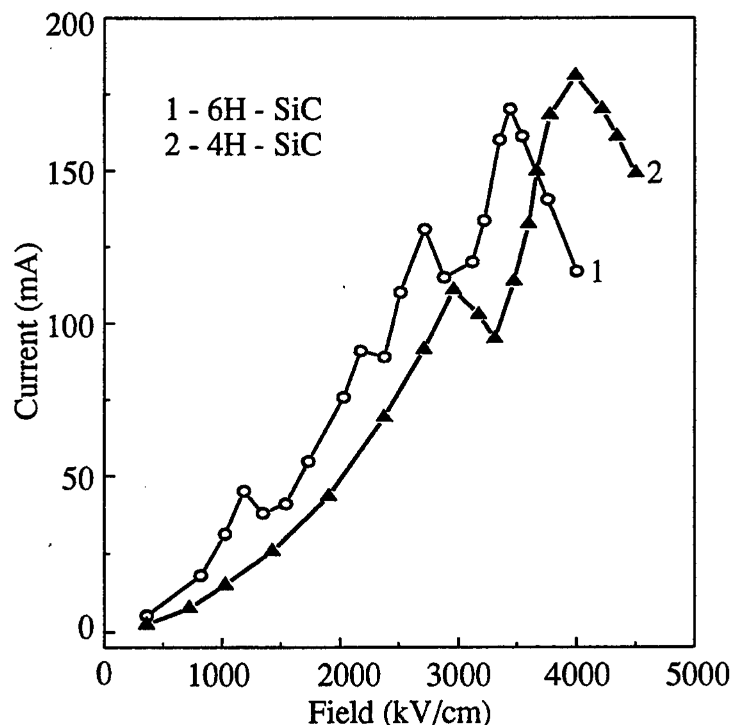

Fig 1.

These data are the evidence of assumption, which is noted above about the absence of the electron component of impact ionization to some values of the electic fields. This phenomenon can be explained by suppression of an electron heating in electron minizone theoreticaly described in [5].

In the flight region of experimental structure, where the electric field was uniform, I–V characteristics of different polytypes were investigated in strong electric field. The most extraordinary feature of these characteristics is the NDC region (Fig. 2) associated with a some threshold field Ft specific for every polytype. For 4H, 6H and 8H the F_t values are 2.9×10^5 V/cm, 1.5×10^5 V/cm and 1.1×10^5 V/cm respectively.

For the treatment of these results in terms of WSL the parameters included in the Esaky-Tsu criterion $F_t > h/ed\tau$ should be obtained. The superlattice constants d for the three polytypes are 5A for 4H, 7.5A for 6H and 10A for 8H. Taking into account the similarity of electrophysical properties of the three polytypes and considering the scattering time t for them as approximately the same one can conclude that there is a qualitative agreement between the threshold fields obtained for the three polytypes and one determined by the criterion. In other words the Esaky-Tsu criterion of NDC associated with the Bloch oscillations correlates well with F_t obtained experimentally for superlattices with periods substantially different.

The reasons mentioned above allows us to interpret the NDC obtained in the framework of WSL. However for the more accurate treatment of data the scattering time t at a strong electric field should be determined experimentally for the three polytypes. Fortunately the experimental method used for the study allows to obtain the t value by the analysis of the same current-field characteristic.

The idea is the following. The electronic transport in the experimental structure used for the measurements is determined by the transit-time mechanism, and the appropriate

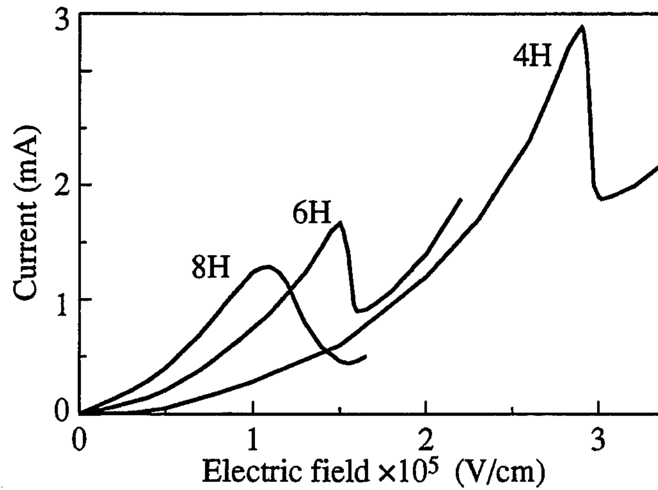

Fig 2.

theory is suitable for such a case. It is known that the current-field characteristic inherent for the transit-time conduction mechanism includes the linear region associated with the space charge limited current. This region is observed when the concentration of the carriers injected is as large as an ionized impurity concentration in the base. It is easy to show that the drift velocity is determined by the characteristic tilt tangent:

$$j = 2\epsilon_s v_s V/w^2 \tag{1}$$

Here j, ϵ_s, v_s, V, w are the current density, the dielectric constant of semiconductor, the saturated drift velocity, the voltage applied to the base and the base width respectively.

The feature of the experimental structure used for the study is an ionized impurity concentration so low that the space charge limitation of the current becomes at low current density when the electric field is insufficient for the carriers velocity saturation. Since the velocity in such a case depends on the field as $v = mV$ (here m is the electron mobility) the resulting law determining the current-field characteristic runs as follows:

$$j = 2\epsilon_s \mu V^2/w^3 \tag{2}$$

Thus the current-field characteristic of the experimental structure includes the following regions: the region with $j \sim V^2$ connected with the space charge limitation of the current injected (3) and the region with $j \sim V$ associated with electronic velocity saturation (2). Then on reaching the threshold electric field value the NDC associated with the Bloch oscillations arises. These regions are identified clearly in the experimental current-field (current-voltage) characteristics of the three polytypes involved into the study.

The electrophysical parameters as important as a high field mobility and saturated velocity are of great self-sufficient interest but in this study they are used for the calculation of the scattering time which can be expressed as $t = mm/e$. Values of high-field mobility m obtained by the processing of the characteristic region with $j \sim V^2$ were found to be 3.1 cm^2/Vs, 4.5 cm^2/Vs and 6.4 cm^2/Vs for polytypes 8H, 6H and 4H respectively. The masses along the superlattice axis at such a strong field can be obtained with the formula:

$$v_s = (8E_p/3\pi m)^{1/2} \tag{3}$$

where the saturation velocity v_s can be extracted from the region with $j \sim V$ and the longitudinal optical phonon energy E_p is taken to be as high as 100 meV.

The experimental results processed this way lead to the following scattering time values: 1.75×10^{-13} s for 8H, 2.05×10^{-13} for 6H and 1.1×10^{-13} for 4H. The fault of t calculation related to variation of the base width is supposed to be about 20% or smaller. Considering these results one can conclude that the both experimentally measured parameters F_t and τ meet the Esaky-Tsu criterion.

To summarise it should be noted that the negative differential conductance was observed in a three superlattices possessing similar electrophysical properties but different periods. The threshold fields of NDC correlate well with the criterion of conductivity in the Bloch oscillations regime. The difference between these threshold field values is in good agreement with the difference of the superlattice constants. Besides the original experimental method has allowed to carry out the measurements of such important parameters as a drift saturation velocity and high field electronic mobility.

The series of papers [3,4,6] is a first study of WSL carried out with a new class of superstructure objects — natural superlattices of a hexagonal silicon carbide polytypes. The data obtained can be considered as both a serious experimental contribution to the problem of WSL and as a result very promising for superhigh frequency devices design.

From the analysis of linear region of I–V characteristics, which have been described by Eq. (1) the values of saturated electron drift velocities for 4H-, 6H-, 8H- and 21R-SiC were obtained which are approximately equal to 3.3×10^6, 2×10^6, 10^6 and 4.4×10^3 cm/sec correspondingly. The low values of velocities,which are significantly less than well known value $v_s = 2 \times 10^7$ cm/sec for $F \perp C$ [7] pay attention itself. But these values qualitatively correspond to the analogical results for artificial SL's in which localization is intrinsic property of these objects. In case of SiC polytypes, the velocity decrease is connected with decrease of the first-minizone width for the noted set of polytypes.

Thus, the presented results are the convincing evidence of minizone structure of electron spectrum in SiC polytypes which is necessary condition of FIL existence. The partial financial support of Russian Foundation of Fundamental Research and Russian Science Program "Physics of Solid State Nanostructures" is gratefully acknowledged.

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OPTOELECTRONIC DEVICES BASED ON GALLIUM NITRIDE

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A number of optoelectronic devices have been produced on the basis GaN-heterostructures: optron, device with switching and stable states remembering by radiation colour, photodetector with switching and memory, transformer of infrared signal into visible one with remembering this signal. The main element of these structures is the M-i-n-GaN-Light-Emitting Diode with GaN active region doped with zinc and oxygen simultaneously.

Emitting GaN-structures oriented in plane (1120) were grown by vapour-phase epitaxy in chloride-hydride system on sapphire substractes with orientation (1012). Growth temperature - 950-1050° C, growth rate - 6-20 (μm/h. Active regions of the structures were doped with iso-electronic impurities Zn and O in order to create the efficient radiation centers. Zn and O ions radii are almost identical to Ga and N ones correspondently. Due to that fact crystal lattice structural disturbance is the least in case of intense doping. So the zinc solubility in GaN was increased to 8-10% in presence of oxygen. Zn and O distributions over a cleaved surface are fairly similar. High-resistant i-regions of the structures were grown of two or more alternating GaN(Zn) and GaN(Zn,O) layers. The layers of GaN)Zn) had higher resistance for spatial separation of active GaN(Zn,O) layers from the regions with strong electrical field.

The luminescence band with maximum 2,55 eV at 300K and linear polarization up to 60% was revealed in GaN(Zn,O) [1,2]. It was associated with presence of pair Zn-O defects. With increasing concentration of Zn and O in i-region nonpolarized bands 2,4 eV, 2,2 eV and 1,8 eV was appeared consequently in addition to the polarized band 2,55 eV. The variety of spectral characteristics allowed to produce the following LED's: blue with polarized emission, with white emission, with controlled emission colour blue to red. Efficiency of the LED's was 0,1-0,3% [3-6].

Covering supphire substrate free surface by photo-sensitive layer converts the device to optron. For example in case of CdS which photo-sensitivity spectrum perfectly agrees with the emission spectrum of blue LED the optron transfer coefficient in current is 25%.

Heterostructure M-ZnTe-i-n-GaN-M can operate as a two-colour LED with switching and memory. At certain working voltage almost all voltage drops on a more resistant layer of ZnTe where electroluminescence with maximum at 2 eV is emitted. Additional pulse of voltage causes reversable electrical break-down in ZnTe that leads to the redistribution of voltage in structure to switching on the LED. The LED emission excites photo-conductivity in ZnTe layer and decreases its resistance additionally. Appeared positive optical feed-back leads to further increasing the LED radiation intensity and switching the device into low-resistant state which is remembered when the working voltage is being applied to the device. Another semiconductor material instead of ZnTe can be used too.

The described device can operate in the regime of photo-detector with switching and memory. Radiation of the device by light pulse from the ZnTe

(or other material) in photo-sensitivity range causes switching of the LED. The device switches to low-resistant state and remembers light signal of external source. The light-sensitive material determines the spectral range response time of the device.

Photo-detector becomes transformer of IR-signal into visible one if the phto-layer sensitivity lies in the IR-range of spectrum (for example PbS, PbSe, Ge, Si etc). Visible signal is remembered and can be recorded from the side of sapphire substrate. The device resolution depends on the resistance of the LED i-layer.

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High Pinch-off Voltage AlGaN-GaN Heterostructure Field Effect Transistor.

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Summary

We report on the fabrication and characterization of a surface-passivated $Al_{0.15}Ga_{0.85}N$-GaN Heterostructure Field Effect Transistor (HFET) with the 1.1 micron gate length, the source-to-drain spacing of 5 micron, the gate-to-drain spacing of 2 micron, and the threshold voltage of approximately -5.5 V. The device has both a high drain-to-source current of 712 mA/mm and a high breakdown voltage (close to 160 V). It exhibits a record cutoff frequency time gate length product of 18.9 micron x GHz, and the maximum frequency of oscillation of 35.3 GHz. These results confirm that doped channel GaN-based HFET have potential for applications in power microwave amplifiers.

Introduction. We recently reported on surface-passivated high current Doped Channel AlGaN-GaN Heterostructure Field Effect Transistors (DC-HFETs) with 1 micron gate length [1] and deep submicron gates [2,3], which demonstrated excellent potential for operation at microwave frequencies. However, these transistors had relatively small breakdown voltages. Since a major expected application of AlGaN/GaN HEMTs is for high power amplifiers, it is extremely important to demonstrate that the record microwave performance can be combined with high breakdown voltages. In this paper, we report on passivated Doped Channel AlGaN-GaN HFETs with high pinch-off voltage and high drain current, which also exhibit a high breakdown voltage close to 160 V, indicating a good potential for GaN-based microwave power amplifiers.

Device fabrication. The material growth by low pressure Metal Organic Vapor Pressure Epitaxy on sapphire substrates and the device epilayer structure are similar to that described previously. [1,2] Our recent measurements of the Quantum Hall and Shubnikov-de-Haas effect on similar AlGaN-GaN modulation doped structures with Si-doped channels clearly showed the existence of the two-dimensional (2D) electron gas in these structures with parallel conduction path provided by three-dimensional electrons. [4] The Hall mobility measurements and theoretical calculations reported in [1,5] showed that the 2D-electron gas mobility in doped channel structures at room temperature is nearly the same as in undoped structures. This is confirmed by our more detailed measurements shown in Fig. 1. As seen, the doped channel AlGaN/GaN heterostructures have the sheet carrier density-mobility product on the order of 10^{16} V/s, which is close to or higher than this product for AlGaAs/GaAs heterostructures. This, combined with a high saturation velocity and a high electric field of the velocity saturation in GaN, (where the peak

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velocity is reached in the electric fields on the order of 150 kV/cm [6]) clearly points out to potential advantages of doped channel AlGaN-GaN HFETs.

The devices exhibited a small gate leakage current of 4.5 microamps at the gate-to-source voltage of - 7 V. From the slope of the current voltage characteristics at gate bias of 2 V, we estimate the source and drain series resistances to be approximately 3.3 ohm-mm or less, which corresponds to the maximum intrinsic transconductance of 180 mS/mm. The negative output conductance in the saturation region at drain-to-source currents higher than 300 mA/mm or so points out to self-heating effects (see, for example, [7]).

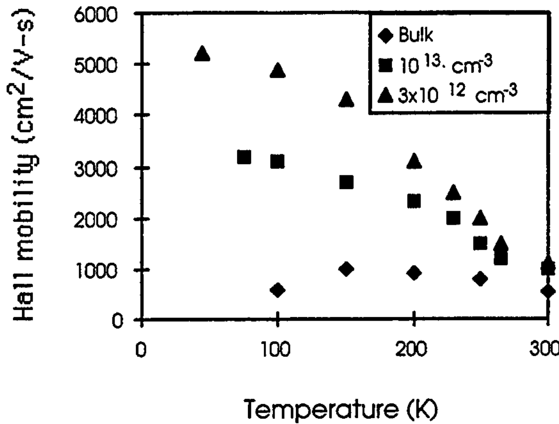

Fig. 1. Hall 2D electron gas mobility in bulk GaN and nominally undoped ($n_s = 3x10^{12}$ cm^{-3}) and doped (($n_s = 10^{13}$ cm^{-3}) AlGaN/GaN heterostructures versus temperature.

The device geometry is as follows: the 1.1 micron gate length, 50 micron gate width, the source-to-drain spacing of 5 micron, the gate-to-drain spacing of 2 micron, the gate-to-channel separation (i.e. the AlGaN barrier layer thickness) measured by cross-sectional TEM is approximately 300 Å. The device fabrication procedure is described in [1] with an additional step of the device surface passivation by a SiO_2 layer in order to improve the breakdown voltage.

Fig. 2 shows the measured current-voltage and transfer characteristic of a typical 1.1 micron gate device.

The threshold voltage estimated by the linear extrapolation of the transconductance near the pinch-off to zero is approximately -5.5 V. The maximum drain current and transconductance are 712 mA/mm and 134 mS/mm, respectively.

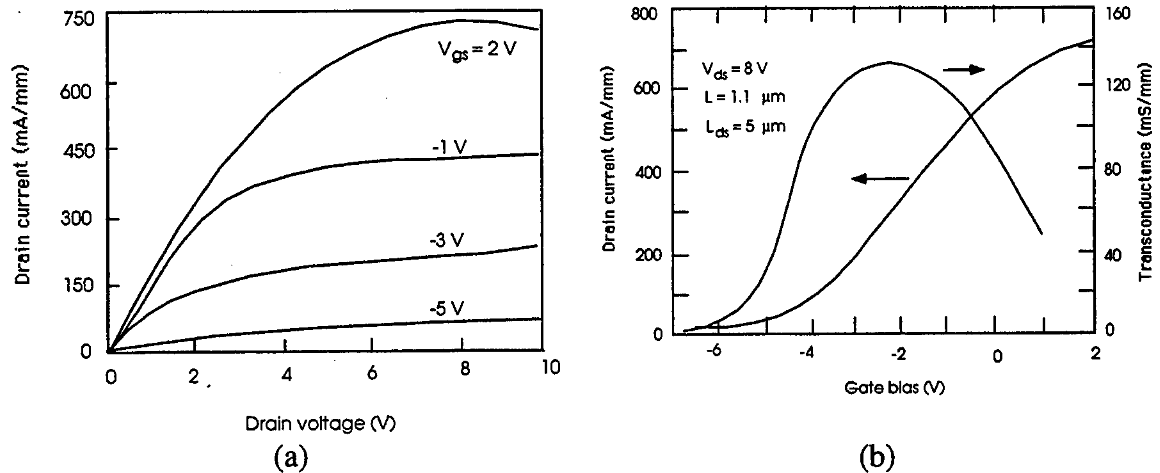

Fig. 2. Measured current-voltage (a) and transfer characteristics (b) of 1.1 micron gate AlGaN-GaN DC-HFET.

Fig. 3 shows the current gain and maximum available gain versus frequency. The cutoff frequency of 17.3 GHz and the maximum frequency of oscillation of 35.3 GHz have been achieved. This corresponds to a record cutoff frequency time gate length product, f_TxL, of 18.9 GHz x micron, slightly better than we reported previously. [1] The improvement in the f_TxL product is larger than the accuracy of the measurements. However, it is more significant that this is obtained for the device with a high breakdown voltage.
For comparison, the best values of the f_TxL product achieved for InGaAs based HFETs are on the order of 27 GHz x micron. [8], see pp. 60-61. We should note that for InGaAs based HFETs, these record values of the f_TxL product do not quite scale with the gate length. For example, the best value of the f_TxL product achieved for a 0.2 micron InGaAs based HFET is 24.4 GHz x micron [8], even though based on the expectation raised by the prospects of the overshoot or ballistic transport one would expect the opposite trend.

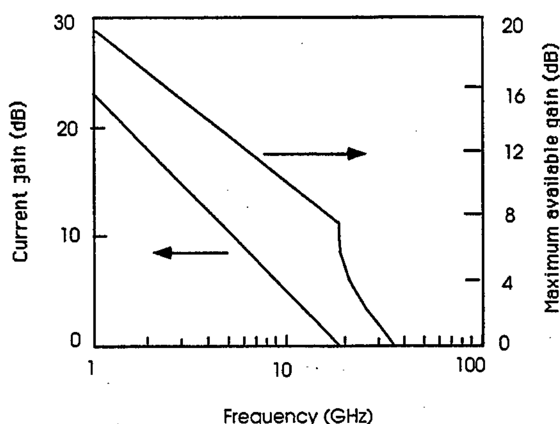

Fig. 3. Current gain and maximum available gain versus frequency.

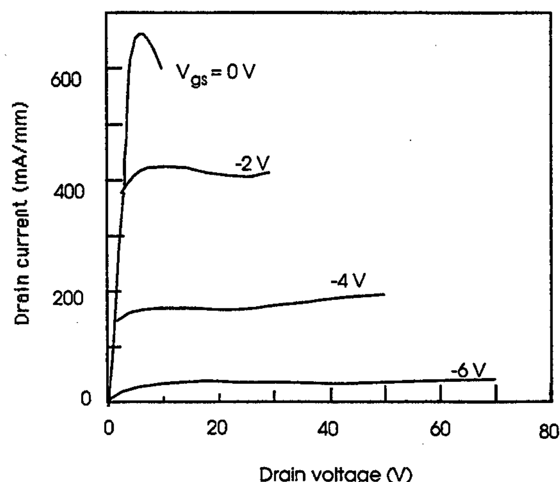

Fig. 4. Current-voltage characteristics of 1.1 micron gate AlGaN-GaN DC-HFET extended to high voltages.

Other groups recently reported excellent results on AlGaN-GaN HFETs. Wu et al. [9] demonstrated the gate-drain breakdown up to 340 V. Gaska et al. reported on the breakdown field of 1.3 MV/cm in AlGaN-GaN HFETs with offset gates. [10]

Mohammad et al. [11] demonstrated reactive molecular beam epitaxy GaN-based HFETs with the maximum current of 695 mA/mm and 222 mS/mm transconductance under light (somewhat smaller in the dark) for 1.5 micron gate device, which had a breakdown voltage of 90 V. Their group also demonstrated the specific contact resistances for the AlGaN-GaN devices as low as 8.9×10^{-8} Ohm-cm^2. [12] More recently, Gaska et al. reported on the AlGaN-GaN HFET grown on a SiC substrate with the device transconductance of 180 mS/mm. [13], [14]

Our devices exhibit higher cutoff frequencies and maximum frequencies of oscillation then reported in literature for this gate size, in spite of higher values of the series resistance. As before, based on the analysis reported in [1], we explain these results by higher gate voltage swing, which allows us to approach the electron velocity saturation.

Fig. 4 shows the current-voltage characteristics for our device extended to high voltages. As seen, the gate-to-drain breakdown voltage higher than 80 V has been obtained. The highest measured breakdown voltages exceeded 151 V under the conditions similar to the breakdown walkout effect observed in GaAs-based HEMTs. [15] When the drain bias reached 135 V at the pinch-off (at the gate bias of -8 V) the drain current rose sharply from 610 μA to 810 μA. At this point of time, the drain bias was turned off. When the drain bias was applied again, the measured breakdown drain voltage reached 151 V (i.e. the drain-to-gate breakdown voltage was 159 V). These numbers varied from a device to device, which shows that the observed breakdown effects are still limited by surface phenomena and may be sensitive to the drain contact geometry. Based on the usual estimate for the maximum power produced by a class A amplifier ($P = I_{max}V_{break}/8$), we may expect microwave power levels over 5 W/mm from comparable GaN-based HFETs.

Acknowledgment. The work at the Rensselaer Polytechnic Institute and APA Optics, Inc. has been supported by the Office of Naval Research (monitored by Dr. Colin Wood).

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Numerical Simulation of 3C-SiC Ballistic Diode Based on the Lei-Ting hydrodynamic balance equations

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Silicon Carbide(SiC) devices has attracted great interest in recent years because SiC devices have 10 times the voltage capability, 100 times the radiation resistance, and 3 times the thermal conductivity of devices based on Silicon or Gallium arsenide. They can also operate at temperature above 600 $^{\circ}C$[1]. The study of 3C-SiC devices, however, has long been hindered by difficulty in sample preparation due to problem such as the large mismatch in lattice parameter with any substrate, and the thermal expansion coefficient between 3C-SiC and e.g. Si. Recently, significant progress in crystal growth and epitaxial of 3C-SiC has led to increased attention to this excellent wide band gap semiconductors.

The short $n^+ - n - n^+$ ballistic diode can be considered as one of the basis structures for modern microelectronics. In particular, the fundamental features of these diodes, including ballistic effect, spatial distributions of various physical quantities, small-signal-impedence behavior,*etc.* have been the subject of many thorough studies. We present a numerical simulation of 3C-SiC Ballistic diode by using a hydrodynamic model[2] based on the Lei-Ting balance equations which has been successfully applied to many types of semiconductor microstructures and devices[3].

The time-independent Lei-Ting hydrodynamic balance equations along with the Poisson equation can be written as follows[2]

$$\nabla \cdot (n\mathbf{v}) = U, \tag{1}$$

$$(\mathbf{v}\cdot\nabla)\mathbf{v} = -\frac{2}{3}\frac{\nabla u}{mn} + \frac{e\mathbf{E}}{m} + \frac{\mathbf{f}}{mn}, \tag{2}$$

$$\mathbf{v}\cdot\nabla u = -\frac{5}{3}u\nabla\cdot\mathbf{v} - W - \mathbf{v}\cdot\mathbf{f} - \nabla\cdot\mathbf{Q}, \tag{3}$$

$$\nabla^2\phi = -\frac{e}{\epsilon}(N_D - n), \tag{4}$$

where n is the electron density, $\mathbf{v}$ is the average velocity of the electrons, U is the net recombination rate per unit volume. u is the average kinetic energy of the electrons. $\mathbf{f}$ and W denote the frictional force due to impurity and phonon scattering and the energy loss rate of the electron system to the phonon system, respectively, which have been given in Ref.[2]. $\nabla \cdot \mathbf{Q}$ is the heat flow. e and m are the electron charge and electron effective mass, respectively. ϕ is the electrical potential. $\mathbf{E} = -\nabla\phi$ is the electric field, ϵ is the static background dielectric constant, and N_D is the net doping concentration.

In our calculation, we employ decoupled method to solve the hydrodynamic balance equations. The discretization of the current continuity equation and the energy continuity equation in the space domain is carried out by means of the generalized Scharfetter-Gummel method[4]. The device considered here is 0.6 μm long. The middle region(~0.3 μm) is doped to the level 5.0×10^{15}cm^{-3}, while the anode and cathode(each ~0.1 μm long), are doped to 5.0×10^{17}cm^{-3}. There is a smooth grading of the doping level at the junctions between the electrodes and the middle region. Here we use a 60-node grid which is uniformly distributed along the device length. The lattice temperature is 300 K. The scattering mechanisms considered here are ionized impurity scattering, acoustic phonon via deformation potential coupling scattering, polar optical phonon scattering and intervalley phonon scattering. The voltage is applied up to 5 V.

The simulation results are presented in Figs. 1-4, where we display the electrical potential, electron velocity, electron temperature and electron density along with the length of device for various bias fields. Fig. 1 shows the electrical potential along the device with different bias fields. The bias is applied at the right contact, while the left contact is grounded, hence the direction of the electron flow is from the left to right. At low bias fields, the electrical potential has a slight decrease along the junctions where the electrons are injected from the heavy-doping region to the light-doping region, then it increases linearly and reaches the saturation value at the right contact. When the bias field is higher than 2V, which is larger than the built-in field resulted from the distribution of electron density, the slight decrease disappears and the electrical potential increases directly and linearly from the value at left contact.

The electron velocity distribution is presented in Fig. 2 under different bias fields. The electron velocity is almost unchanged in both contacts, however, it increases significantly when electrons begin to enter the light-doping region and reaches its maximum value before it decrease to the value at right contact. With increasing bias fields, the electron velocity in both contact regions has a slight increase but has a significant increase in the light-doping region. The position where the electron velocity reaches its peak shifts toward the right contact with increasing bias fields. Furthermore, there is a noticeable overshoot of the velocity when the bias field is greater than 2 V.

The distribution of normalized electron temperature, T_e/T, is plotted in Fig. 3 for different bias fields. Because of the boundary condition imposed, the electron temperature at the electrodes is almost the same as the lattice temperature, while the electron temperature in the middle region is substantially different from the lattice temperature. When the electrons are injected from the heavy-doping region to the light-doping region, the electron temperature under a small bias field(less than 1 V) is slight lower than the lattice temperature. This phenomenon is also found in Si ballistic diode. Similar to the distribution of electron velocity along the device, the electron temperature reaches a peak before the electrons are collected by the right contact. With increasing bias fields, the electron temperature in the

middle region rises quickly. For example, the electron temperature under 5 V bias is as high as about 15 times the lattice temperature, while it is 1.3 times under a 0.5 V bias.

The electron density is plotted in Fig. 4 along the device. The distribution of electron density under different bias is not as obviously different as the electron temperature and electron velocity. The electron density in the light-doping region increases slightly with increasing the bias field.

Acknowledgements

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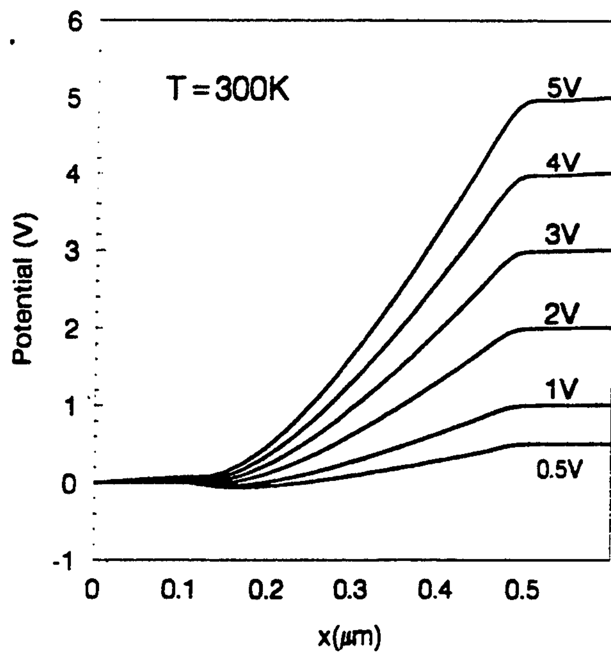

Fig.1 The electrical potential along device under different bias field

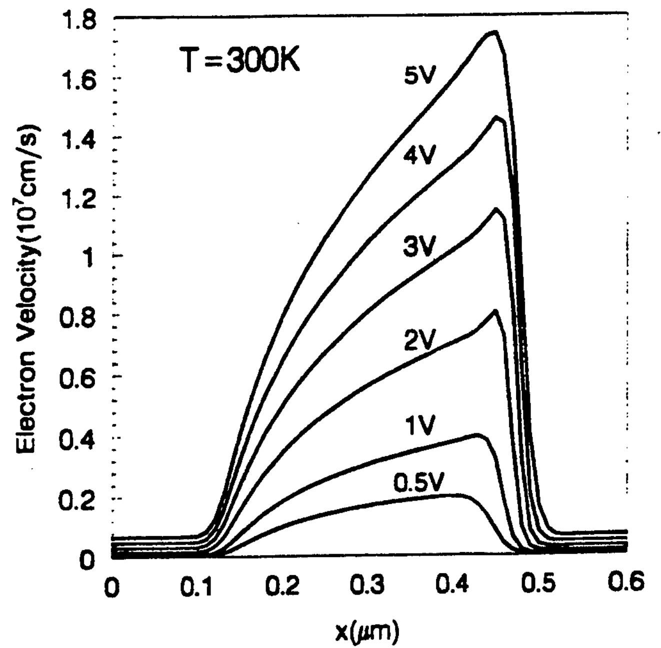

Fig.2 The electron velocity along device under different bias field

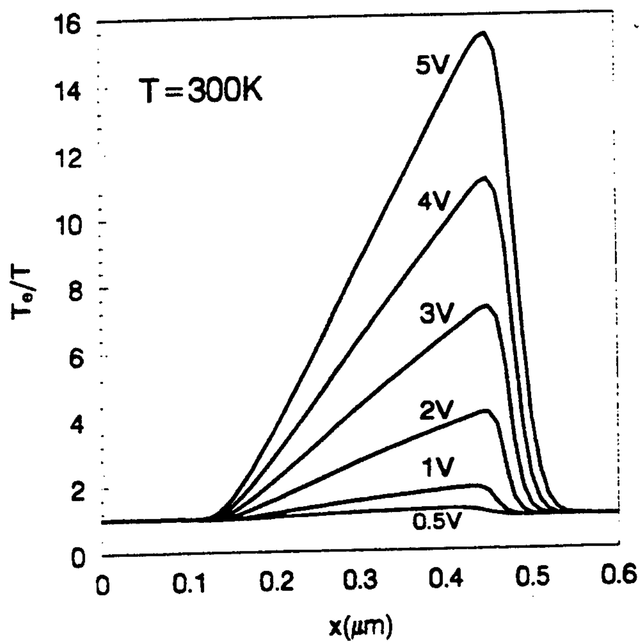

Fig.3 The electron temperature along device under different bias field

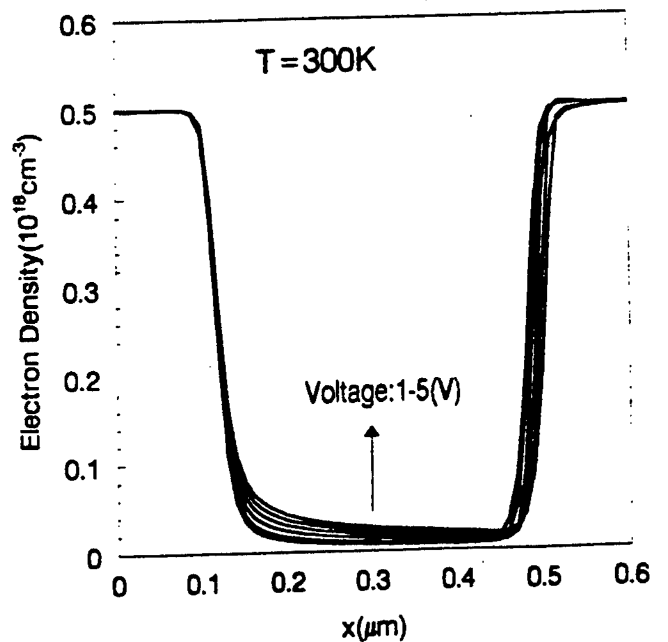

Fig.4 The electron density along device under different bias field

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Electron transport properties of zinc-blende $Ga_{1-x}Al_xN$

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ABSTRACT

GaN/AlGaN high electron mobility transistors (HEMTs) have recently attracted much attention with the large available bandgap of the channel material and excellent thermal properties for possible applications in the high power and high temperature microwave devices. In this paper , the results of electron peak velocity , saturated drift velocity and low-field mobility for $AlN/Al_xGa_{1-x}N/GaN$ are reported from an ensemble Monte Carlo simulation. Acoustic phonons, optical phonons, intervalley, ionized impurity and piezoelectric scattering are included in the simulation. Doping densities ranging from 10^{17} cm^{-3} to 10^{19} cm^{-3} are considered in the temperature range of 50K to 500K. Theoretical calculation of low field mobiltiy shows excellent agreement with experimental data.

EXTENDED SUMMARY

An ensemble Monte Carlo simulation [1, 2] is performed to investigate the electron transport properties of zinc-blende $Ga_{1-x}Al_xN$ for different doping concentration and varying temperature. Acoustic phonons, optical phonons, intervalley, alloy, ionized impurity and piezoelectric scattering are included in the simulation and the values are given in Table.1.

In Fig. 1, the simulated electron drift velocity is plotted as a function of applied electric field in GaN with temperature as a parameter. A peak velocity of 2.6×10^7 cm/s is obtained at a field strength of 145 KV/cm for undoped GaN at room temperature . The position of the peak velocity moves from 140 KV/cm at 100K to 170 KV/cm at 500K. It is interesting to note that the low field mobility increases as the temperature is lowered, whereas, the saturation velocity does not show such a pronounced temperature dependence. This can be explained by noting that the low field mobility, which is dominated by acoustic phonons and polar optical phonon absorption, shows

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improvement due to the suppression of these scattering processes. The high field transport, on the other hand, is dominated by polar optical phonon emission and intervalley scattering that have a weak lattice temperature dependence.

In Figs. 2 and 3, the peak velocity and saturation velocity are plotted as a function of Al-mole fraction, respectively, with doping density as a paramter. The plots show weak doping concentration dependence of the two quantities.With increasing doping density at room temperature the peak velocity, in GaN, decreases from 2.55×10^7 cm/s at 1×10^{17} cm^{-3} to 2.46×10^7 cm/s at 1×10^{19} cm^{-3} . From the figures it is also observed that for doping density of 1×10^{17} cm^{-3}, the peak velocity decreases from 2.55×10^7 cm/s for GaN to 1.88×10^7 cm/s for AlN , and the saturated velocity increases from 1.35×10^7 cm/s for GaN to 1.6×10^7 cm/s for AlN . The peak velocity decreases rapidly with increasing Al mole fraction mainly due to the increase of band-gap, Γ-L separation and effective mass in both valleys.

In Fig.4, the low field mobility is plotted as function of temperature with doping density as a parameter for GaN. On the same plot experimental data reported by Look et. al. is plotted showing excellent agreement. The low field mobility μ(N,300K) changes from 590 cm^2/V-s at 1×10^{17} cm^{-3} to 440 cm^2/V-s at 1×10^{19} cm^{-3} for GaN. The temperature dependence of the low field mobility for a doping level of 1×10^{17} cm^{-3} can be given as $\mu(T) = 1156 - 2.75T + 0.002T^2$ cm^2/V-s. With increasing doping the peak in the low field mobilty decreases and shifts towards higher temperature. This behavior is attributed to the nature of ionized impurity sacttering. Above 200K, polar optical phonons dominate transport in GaN and explains the behavior of the low field mobility at high temperature where they become independent of doping.

The fit to the experimental data required modification in the parameter values in the ensemble Monte Carlo simulation. Following the process reported by Look et. al. the acoustic deformation potential was made 35% higher than the value quoted in the literature. Moreover, the dielectric constants ε_∞ and ε_0 which are involved in polar optical phonon scattering were decreased by 23%, and piezoelectric constant was increased by 12%. The above modifications affect the scattering mechanisms at the low and high electric field limits. Unlike the observation made by Look et. al. [5] where a scaling of the theoretical low field mobility curve by a factor of 1.4 also enabled a fit to the experimental characteristics, such a scaling was not possible with the ensemble Monte Carlo simulation. The lack of such a constant scaling factor is reasonable as the scattering rates are not linear with temperature.

Acknowledgement

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Table-1

Parameter	Symbol(units)	GaN	Fitted Value	AlN
Dielectric const.	ε_∞ (F m^{-1})	5.47	4.2	4.77
Dielectric const.	ε_0 (F m^{-1})	10.4	8.1	8.5
Mass density	ρ ($\times 10^3$ kg m^{-1})	6.1 [3]		3.23
Phonon energy	$\hbar\omega_{LO}$ (meV)	91.2		
99.2				
Piezoelectric const.	h_{pz} (cm^{-2})	0.5 [4]	0.56	0.5 [4]
Acoustic-Deformation potential	E_1 (eV)	9.2	12.5	9.5
Effective mass	m^* (kg)	$0.22m_0$		$0.48m_0$
Lattice constant	a (Å)	5.125		4.980

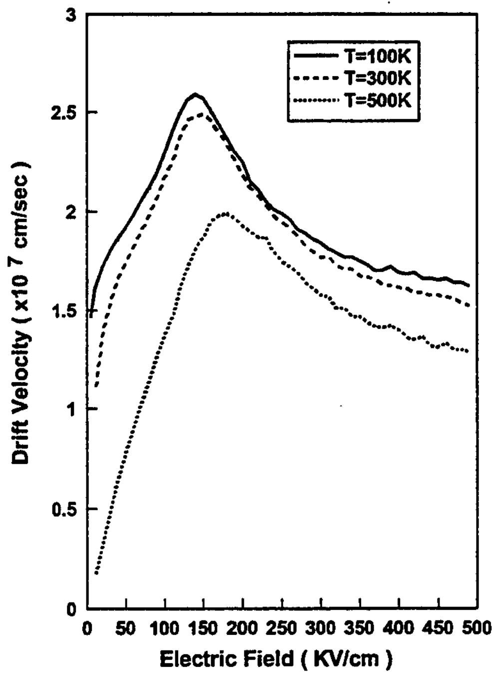

Fig. 1 GaN (undoped) drift velocity vs. electrical field at various temperatures.

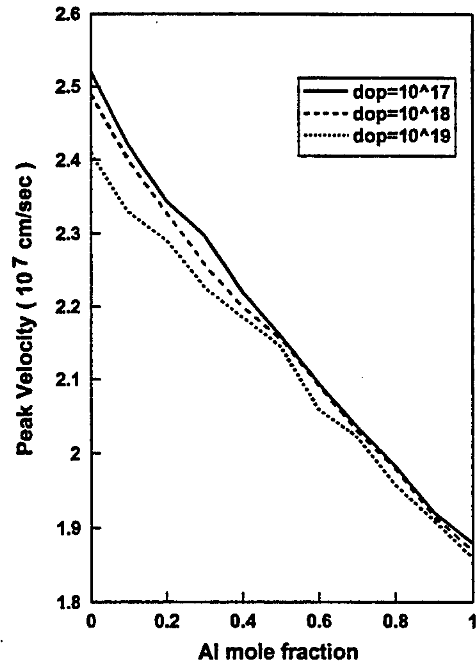

Fig. 2 Variation of the peak velocity in $Al_xGa_{1-x}N$ with the doping concentrations for various values of the Al mole fraction.

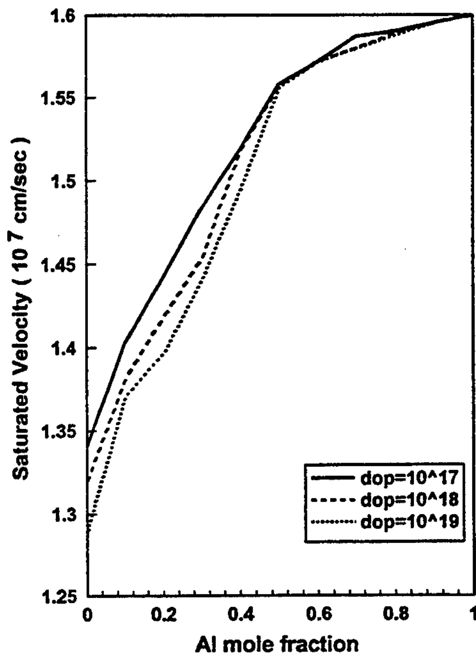

Fig. 3 The saturatrated velocity in $Al_xGa_{1-x}N$ as a function of Al mole fraction for carrier concentrations of 10^{17}, 10^{18} and $10^{19}cm^{-3}$.

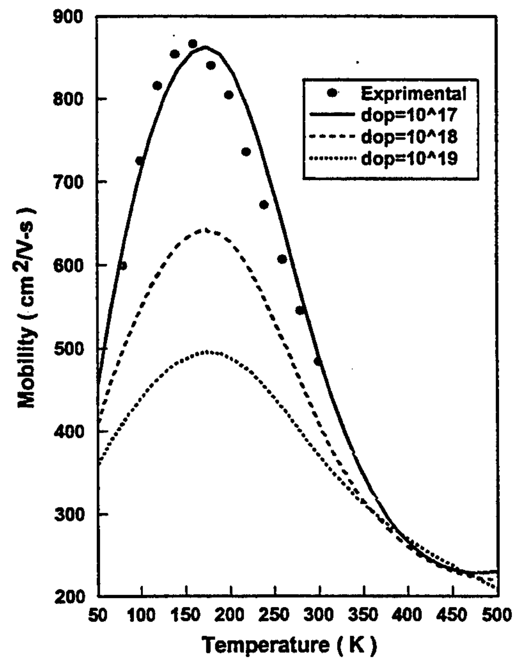

Fig. 4 Experimental (points) and theoretical (lines) mobility for GaN for various temperatures.

"TWO REGION" MODEL OF HIGH FIELD ELECTRON TRANSPORT IN GaN

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SUMMARY

We propose a "two-region" model describing electron transport in polar semiconductors at temperatures smaller than the polar optical phonon energy. Our approach is based on the analysis of two energy ranges - "passive", where the electron energy, ε, is smaller than the optical polar energy, $\hbar\omega_0$, and "active", where ε is greater than $\hbar\omega_0$. We show that an analytical solution can be obtained for high electric fields, when the electrons are more likely to experience a transition from the passive to the active region due to gaining energy from the electric field rather then due to the absorption of optical phonons. We apply this theory to GaN. Our estimates show that for GaN the two region model is applicable for electric fields higher than 20 kV/cm. We compare the results with the theory based on the balance equations and with our Monte Carlo simulations.

1. INTRODUCTION.

A large direct band gap, large breakdown field, and high electron drift velocity make GaN suitable for high-power and high-speed electronic and optoelectronic applications. As follows from the Monte-Carlo simulation [1-5], the intervalley transitions in GaN become essential only in very high electric fields (on the order of 100 kV/cm). In low electric fields, polar optical phonon scattering, ionized impurity scattering, and piezoelectric scattering in the Γ-valley are dominant [6, 7]. The polar optical phonon scattering is also the most important mechanism of the electron energy loss.

We recently developed a two-step model [6],[8], which describes the polar optical scattering in low electric fields for temperatures smaller than the polar optical phonon energy. In the two-step model, the polar optical phonon scattering event is treated as one combined elastic process that includes two successive steps - the absorption and almost immediate emission of a polar optical phonon. This analytical model allowed us to calculate the low field mobility for GaN for a wide range of temperatures and impurity concentrations. It highlighted major differences between the electron transport in GaN and GaAs and facilitated the development of the Doped Channel AlGaN/GaN HFETs, which demonstrated superior performance (see, for example, [9].)

We also developed an analytical theory of the electron transport in higher electric fields based on the balance transport equations and applied this theory to GaN [7]. This theory, which accounts for electron-electron collisions and optical polar phonon screening, is only valid for very high electron concentrations (higher than 4×10^{19} cm^{-3} for GaN at 300 K). However, the qualitative conclusion was the same as we had reached from our mobility calculations: in GaN, the impurity scattering is relatively less important than polar optical scattering, compared to the relative importance of these scattering mechanisms in GaAs.

In this paper, we propose a new approach to the transport theory for semiconductors with a large polar optical phonon energy. Just as the two-step model, this approach is based on

the analysis of two energy ranges - "passive", where the electron energy, ε, is smaller than the optical polar energy, $\hbar\omega_o$, and "active", where ε is greater than $\hbar\omega_o$. We show that an analytical solution can be obtained for high electric fields, when the electrons are more likely to experience the transition from the passive to the active region due to gaining energy from the electric field rather then due to the absorption of optical phonons. We call this new model the "two region" model. Our estimates show that this model is applicable for electric fields higher than approximately 20 kV/cm for GaN, which is much smaller than the peak field of the velocity-field characteristic. In GaAs, this model is not applicable at room temperature but may be valid at 77 K. We compare the results with a theory based on the balance equations and with the results of our Monte Carlo simulations.

2. TWO REGION MODEL.

The electron current density, j, is given by

$$j = j_+ + j_- = env_d = -\frac{e^2F}{6\pi^3 m_n}\int_0^\infty \frac{d^3k\varepsilon}{\nu}\frac{df_o}{d\varepsilon} \quad (1)$$

where f_o is the spherically symmetrical distribution function, m_n is the effective mass, e is the electron charge, ν is the inverse momentum relaxation time, and v_d is the drift velocity,

$$n = n_+ + n_- = -\frac{(2m_n/\hbar)^{3/2}}{3\pi^2}\int_0^\infty d\varepsilon\varepsilon^{3/2}\frac{df_o}{d\varepsilon} \quad (2)$$

is the electron density. Here n_+, n_- and j_+, j_- are the electron concentrations and current densities for the active and passive regions, respectively.

<u>A. Active region.</u> In active region the polar optical phonon emission scattering determines both the inverse energy and momentum relaxation times [10]

$$\nu_{opt} = \frac{e^2\alpha\omega_o\sqrt{2m_n}}{4\pi\varepsilon_o\kappa_o\sqrt{\varepsilon}}\ln\left(\frac{\sqrt{\varepsilon-\hbar\omega_o}+\sqrt{\varepsilon}}{\sqrt{\hbar\omega_o}}\right) \quad (3)$$

where ω_o is the optical phonon frequency, $\alpha = \kappa_o/\kappa_\infty - 1$, κ_o, κ_∞ are the static and high frequency dielectric constants, respectively, and ε_o is the permittivity of free space.
The kinetic equation for a spherically symmetrical distribution function, f_+, in the active region is given by

$$\frac{1}{\varepsilon^{1/2}}\frac{d}{d\varepsilon}\left(\varepsilon^{3/2}\frac{2e^2F^2}{3\nu_{opt}m_n}\frac{df_+}{d\varepsilon}\right) = \nu_{opt}f_+(\varepsilon) \quad (4)$$

f_+ decays very rapidly with energy, ε, and only the region in the vicinity of $\hbar\omega_o$ is essential. Expanding eq. (4) near $\varepsilon = \hbar\omega_o$ we obtain

$$\frac{d}{dz}\left(z^{-1/2}\frac{df_+}{dz}\right) - a_o z^{1/2} f_+ = 0 \quad (5)$$

where $a_o = \frac{3\alpha^2 k_o^4 a_{Bn}^4 F_{Bn}^2}{4F^2}$, a_{Bn} is the electron Bohr radius, $E_{Bn} = eF_{Bn}a_{Bn}/2 = m_{Bn}v_{Bn}^2/2$ is the electron Bohr energy, and $k_o^2 = 2m_n\omega_o/\hbar$ is the radius of the passive region in the wave vector space, $z = (\varepsilon - \hbar\omega_o)/\hbar\omega_o$.
The solution of this equation decaying at large energies is given by

$$f_+ = \frac{3\pi^2 n_+}{k_o^3}\exp(-\frac{2z^{3/2}\sqrt{a_o}}{3}) \quad (6)$$

Hence,

$$j_+ = \frac{ev_{Bn}n_+Fa_o^{1/6}}{12^{1/3}\alpha k_o a_{Bn}F_{Bn}}\Gamma(\frac{2}{3}) \quad (7)$$

where Γ is the Euler integral of the second order.

B. The passive region. When the electric field is high, the electron are transferred from the passive into the active region, since they are accelerated by the electric field. Once the electrons get into the active region, they lose energy via the optical polar phonon emission. Hence, the kinetic energy for the passive region is given by

$$\frac{d}{d\varepsilon}(\varepsilon^{3/2}\frac{2e^2F^2}{3vm_n}\frac{df_-}{d\varepsilon}) + \frac{\alpha e^2\sqrt{2m_n\omega_o\varepsilon}}{4\pi\hbar^{3/2}}f_+(\varepsilon+\omega_o) = 0. \quad (8)$$

Solving eq. (8) and using eqs. (1) and (2), we obtain

$$j_- = \frac{3n_+ev_{Bn}\alpha F_{Bn}(k_o a_{Bn})^3}{4Fa_o^{1/2}} \quad (9)$$

$$n_- = \frac{3\pi n_+\alpha F_{Bn}^2 N_d a_{Bn}^3 q_o^2}{8k_o^2F^2}\{1+\int_0^\infty dz\exp(-z)(1+\frac{(12z)^{2/3}k_o^2}{a_o^{1/3}q_o^2})[\ln(1+\frac{(12z)^{2/3}k_o^2}{a_o^{1/3}q_o^2})-1]-$$

$$\frac{16k_o^3}{a_o^{1/2}q_o^3}\int_0^\infty dz\exp(-z)\tan^{-1}(\frac{(12z)^{1/3}k_o}{a_o^{1/6}q_o})+\frac{8\pi k_o^3}{a_o^{1/2}q_o^3}\}+\frac{3n_+\alpha F_{Bn}^2\hbar\omega_o}{4F^2E_{Bn}\sqrt{a_o}}\{\frac{v_{pzd}\sqrt{k_BT}}{\sqrt{E_{Bn}}}+\frac{\alpha\hbar\omega_o}{E_{Bn}}N_o\} \quad (10)$$

Here q_o is the inverse Debye length, $v_{pzd} = v_{pz}\sqrt{\varepsilon / k_BT}$, where v_{pz} is the inverse piezoelectric momentum relaxation time defined in [11]. (Since v_{pz} is inversely proportional to $\sqrt{\varepsilon}$, v_{pzd} is independent of energy.)

C. Criterion of validity. As mentioned above, this approach is valid when the electric field is high enough, so that electrons are transferred from the passive into the active region as a result of gaining energy from the electric field rather then via the absorption of the polar optical phonons. The power supplied to an electron in the passive region may be estimated as $e\mu F^2$. Hence, the average time required for the transfer into the active region due to the electric field is given by $t_F = \hbar\omega_o/(e\mu F^2)$. This time has to be shorter than the polar optical absorption time, which may be estimated as $\tau \approx \mu_{opt}m_n/e$. Here μ is the low field mobility and μ_{opt} is the mobility limited by the polar optical scattering. The requirement $t_F < \tau$ yields

$$F > F_{crlow} = \left[\hbar\omega_o/\left(\mu\mu_{opt}m_n\right)\right]^{1/2} \quad (13)$$

For GaN, $\hbar\omega_o$= 91.2 meV, $\mu \approx 0.1$ m^2/V-s, $\mu_{opt} \approx 0.2$ m^2/V-s, $m_n = 0.23\ m_e$, and we obtain $F_{cr} \approx 20$ kV/cm, still quite a bit smaller than the electric field on the order of 100 kV/cm, where the intervalley scattering becomes very important.

On the other hand, the electric field has to be small enough so that the loss of energy due to the emission of optical phonons in the active region remains higher than the energy gain for the electrons in the active region. The corresponding critical field, F_{crhigh}, can be determined from the Monte Carlo simulations. F_{crhigh} may be also estimated from the condition $eF_{crhigh}v_d \approx \hbar\omega_o v_{opt}$, . This criterion yields roughly $F_{crith} < 200$ kV/cm.

3. VELOCITY-FIELD CHARACTERISTICS.

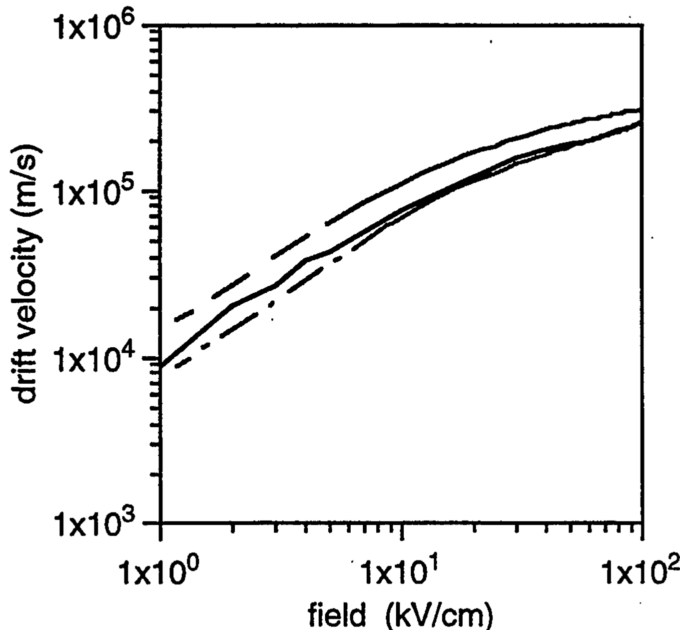

Fig. 1. Electron drift velocity in GaN versus electric field for electron concentration of 10^{17} cm^{-3} at 300 K. Solid line - Monte-Carlo simulation [5]; dashed line - two region model, dash-dotted line - balance equations model.

Fig. 1 shows the calculated dependencies of the electron drift velocity in GaN on the electric field for the electron concentration of 10^{17} cm^{-3} at 300 K. For comparison, we also calculated the velocity-field characteristic using the balance equation approach described in [7]. For a more accurate comparison, we took into account the piezoelectric scattering in addition to other scattering mechanisms considered in [7].As discussed above, the balance transport equations are valid when electron-electron scattering is faster than the rate of phonon scattering, i.e. at carrier concentrations much higher than 4×10^{19} cm^{-3}. As can be seen from Fig. 1, the balance equation approach provides a low bound for the velocity-field characteristics.

The two region model provides an upper bound, since the only scattering mechanism that we account for in the active region is the polar optical phonon emission. The two region model provides a valuable insight into the physics of the electron transport in GaN. In the future work, we will use this model in order to interpret the results of detailed Monte simulations of the electron transport in GaN.

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SOLAR BLIND OPTICAL PHOTODETECTORS BASED ON MONOCRYSTALLINE ZINC SULPHIDE

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1. Introduction

Several space, medical, biological, astronomy and radiometry measurement applications require optical semiconductor detectors with high ultra-violet (UV) sensitivity, insensitive to direct solar radiation, for wavelengths higher than 350 nm and long term stability. The disadvantages of silicon UV-enhanced photodiodes include the facts that silicon is an indirect bandgap material so, the quantum efficiency is low, besides the maximum peak sensitivity is around 700-900 nm. Thus, external filtering is needed to block out the visible and infrared radiation, adding so both, costs and volume to the detector assembly [1]. For the silicon carbide (SiC) based detectors the band gap is larger than the one of Si, making this material more attractive for UV applications. However, monocrystalline [2] or thin-film photodiodes [3] developed based on this material are not real solar blind photodetectors since they are still sensitive to the solar irradiation. Apart from SiC semiconductors, another wide band semiconductor candidate to this applications is the GaAlN. This semiconductor presents a direct band gap with the possibility to tailor the cut-off wavelength by varying the GaAlN alloy composition [4]. At present, UV detectors based on these semiconductors are yet in their infancy and a significant progress in device fabrications can be expect over the next few years.

The large direct bandgap (3.6 eV) of the zinc sulphide (ZnS) may eventually prove to be more promising than SiC for solar blind UV detectors. However, ZnS is an ionic compound and doping effect control is hard to be achieved, requiring new methods for the fabrication of the devices such as, formation of the Schottky barrier by deposition of semitransparent metallic films on ZnS surface. However, the sensitivity of these detectors will be limited by the strong absorption in the semitransparent metallic electrodes. To overcome this difficulty transparent and conductive metal oxide films (TCO) can be applied to produce surface-barrier photodiodes [5].

In the present paper we report an improved version of the surface-barrier ZnS optical detectors that presents an enhanced UV sensitivity by using a transparent electrode based on a TCO film heavily doped with fluorine (FTO), deposited by the spray pyrolysis technique. As the FTO films exhibits a direct bandgap, for comparison proposes, the performances of this type of electrode will be compared with the ones of Sn-doped indium oxide films (ITO) that have a significant absorption at wavelength less than 300 nm. Therefore, we can expect a more higher UV quantum efficiency for the FTO/ZnS detectors than one obtained elsewhere in ITO/ZnS photodetectors [6].

2. Experimental details

N-type ZnS monocrystalline wafers with 10 Ωcm resistivity, were used to fabricate the optical sensors with active areas ranging from 5 to 100 mm^2. The FTO films have been

deposited at 450 °C on the top surface of the monocrystals by the spray technique [5], at atmospheric pressure, under air conditions.

The solution was prepared based on $SnCl_4 \cdot 5H_2O$ precursor, to deposit the FTO films. The precursor have been dissolved to concentration of 0.6 M in alcohol. HF or NH_4F was added to the solution to act as doping of the solution. The deposition rate achieved was near 100 nm/min. The films fabricated on glass and sapphire substrates, in similar conditions as the ones used to deposit over the ZnS films, were used for structural, electrical and optical characterisations.

The back side ohmic contact of the FTO/ZnS sensors was performed similarly to the one performed for ITO/ZnS photodiodes, as described elsewhere [6]. The size of the sensors developed was 3×3 and 10×10 mm^2, respectively.

3. Results

3.1 *Characteristics of the metal oxide films*

The growth mechanism of the films deposited by spray pyrolysis depends on many technical parameters such as the size of droplets, the type of chemical precursors, the substrate temperature, the solution spray rate and the distance between the atomiser and the substrate.

All FTO films deposited exhibit a single phase and are polycrystalline. The x-ray data of the heavy doped FTO (40 at.% F in solution) films as-deposited on glass substrates and with thicknesses near 0.4 μm show a strong preferred grain orientation in the (200) direction.

The electrical data recorded show that mobility and carrier concentration increase with F concentration. This behaviour is explained by the way how the F atoms substitute the anion oxygen in the crystalline lattice, do not giving place to the formation of scattering centres, as it happens with the doped ITO films. The optimised FTO films present sheet resistances of about 10 Ω/sq.

The specular transmission (measured with respect to air) in the wavelength range from 0.3 μm to 2.5 μm of the as-deposited optimised heavy doped FTO and ITO films are shown in Figure 1.

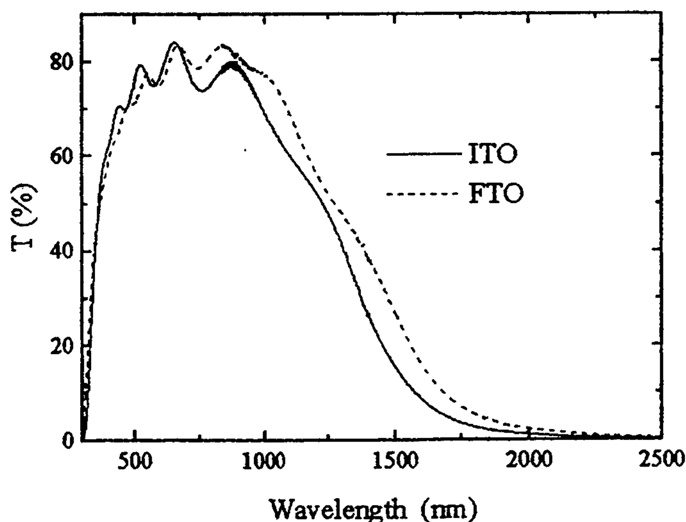

Fig.1 - The specular transmission in the wavelength range from 0.3 μm to 2.5 μm of the as-deposited FTO and ITO films with sheet resistances of 5 and 10 Ω/sq, respectively, for thicknesseses of about 0.4 μm.

The transmission spectra of FTO and ITO films in UV spectral range are shown in Figure 2. The data show that the FTO films are more preferable than the ITO films, for high quantum efficiency UV photodetector applications. In order to decrease the optical losses in the UV region, the film thicknesses used was less than 100 nm.

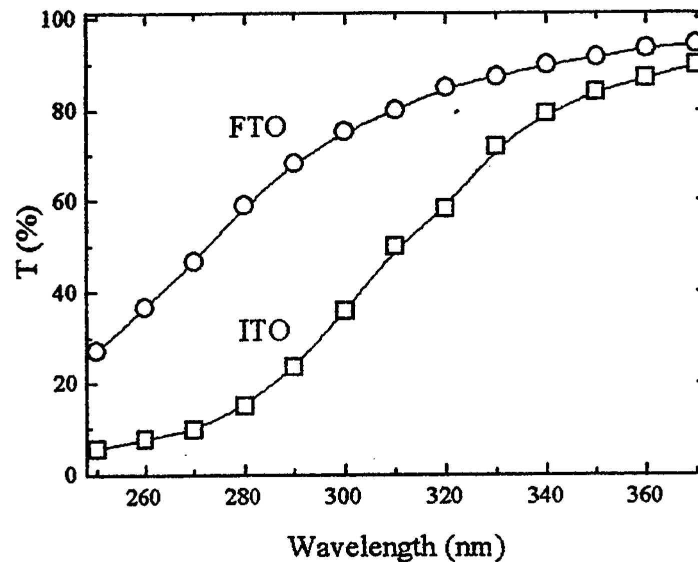

Fig. 2 - Transmission spectra in UV region of heavy doped tin and indium oxide films deposited on sapphire substrate.

3.2 *Characteristics of the photodetectors.*

Figure 3 shows the spectral response of the FTO-ZnO detectors developed in this work and of the ITO/ZnS photodiodes referred elsewhere [6]. In contrast to ITO-ZnS, the maximum spectral sensitivity peak of the FTO/ZnS photodetectors is shifted from 330 to 290 nm, due to the widen of the optical energy bandgap of the FTO layer, when compared to the ITO layer. The combination of a low dark current and a high sensitivity originates a low value for the NEP, ranging from 10^{-14} to 10^{-12} W/Hz$^{1/2}$, function of the area of the detectors.

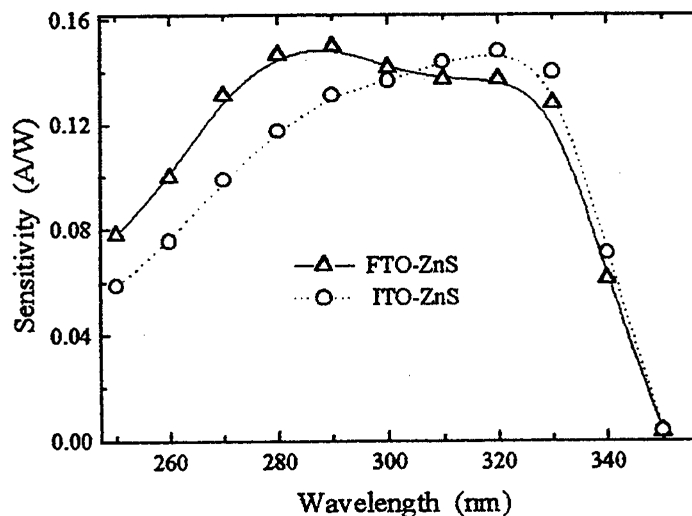

Fig. 3. -The spectral response of the FTO/ZnS and the ITO/ZnS optical detectors.

The dependence of the photocurrent on the light intensities is a linear for the power intensities ranging from 10^{-8} W to 10^{-3} W.
Taking now into account the values of the refractive coefficient and of the transmittance of the FTO electrode (Fig. 2), we estimate an internal quantum efficiency for FTO-ZnS detectors of about 100%, in the UV range. Hence, the recombination losses of the photogenerated carriers in these devices are negligible.
Taking now into account that the value of the coefficient of utilisation (k_u) of the solar radiation is the figure of merit of the solar blind photodetectors [6] and that it is given by:

$$k_u = \frac{\Phi_{eff}}{\Phi} = \frac{\int_0^\infty E_\lambda S_\lambda d\lambda}{\int_0^\infty E_\lambda d\lambda},$$

where E_λ is the spectral distribution of solar irradiation and S_λ is the detector's spectral sensitivity, it is possible to determine the degree of device insensitivity to the solar irradiation.
Using for E_λ the value corresponding to the solar spectrum under AM1 conditions [8] and the measured S_λ, shown in data Fig. 3, the calculated value of k_u was estimated as being 0.1%. This value shows that the developed devices are very perspective for UV measurements under solar background conditions.

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STUDY OF I-V CHARACTERISTICS OF 6H-SiC BGJFETS FOR HIGH TEMPERATURE APPLICATIONS

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This paper reports the I-V characteristics of 6H-SiC buried-gate JFETs (BGJFETs) from room temperature up to 300°C. The n-channel 6H-SiC buried gate depletion mode (normally on) BGJFETs studied in this work were fabricated by Ivanov et al. [1], [2], [3]. The design of these FETs employed a buried p-n junction as the gate and mesa-epitaxial structures with 6H-SiC(0001) substrates and p- and n-epilayers. The abrupt buried asymmetric p^+n junction keeps the space charge region in the n-epilayer. Thus this p^+n junction isolates the conduction channel from the substrate. The p-epilayer is connected to the gate electrode, and thus controls the channel opening depending on the gate bias. The gate contact metal, Ni-Al, was ohmic to the buried gate layer. Typical channel lengths were between 8 to 10 µm and the channel widths were 0.76 mm. Figure 1 illustrate the structure of the buried-Gate BGJFET. The data collected to date represents the test results on more than 350 individual devices from 20 different wafers.

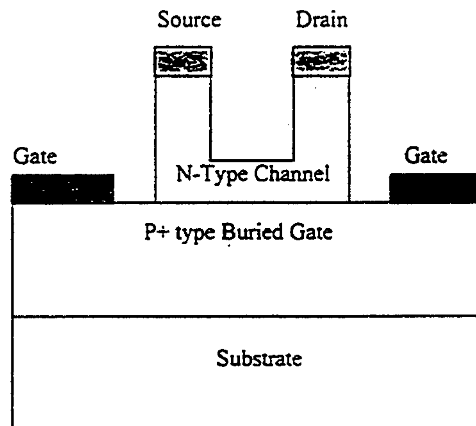

Fig. 1. Schematic diagram of 6H-SiC BGJFET

Figure 2 shows the effects of temperature on threshold voltage. It can be seen that the threshold voltage becomes more negative at higher temperature.

A typical temperature dependence of the saturation drain current for the SiC BGJFETs is shown in Fig. 3. It can be seen that for smaller negative gate voltages, when the drain current is very large, I_{DSAT} decreases with temperature. Although the threshold voltages of the devices become more negative at elevated temperatures, the reduction of carrier mobility in the channel region is the more dominant effect on I_{DSAT} [4]. For smaller values of drain current, I_{DSAT} changes very little with temperature. This behavior can be attributed to increased leakage current with temperature at high reverse bias of gate terminal and negative shift in threshold voltage [4].

The effects of temperature on transconductance of the 6H-SiC BGJFETs is illustrated in Fig. 4. As can be seen from the figure, the transconductance decreases with increasing

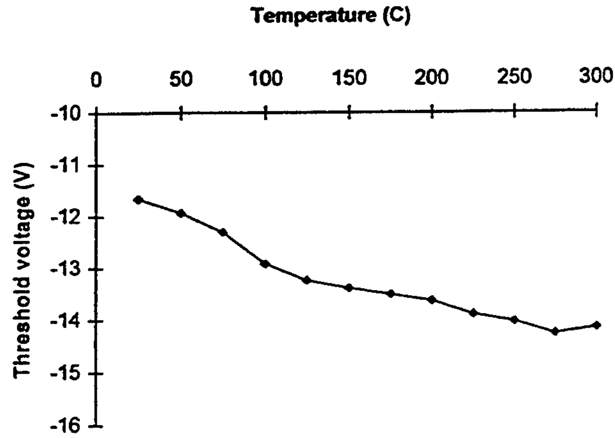

Fig. 2. Effect of temperature on the threshold voltage of the SiC BGJFET.

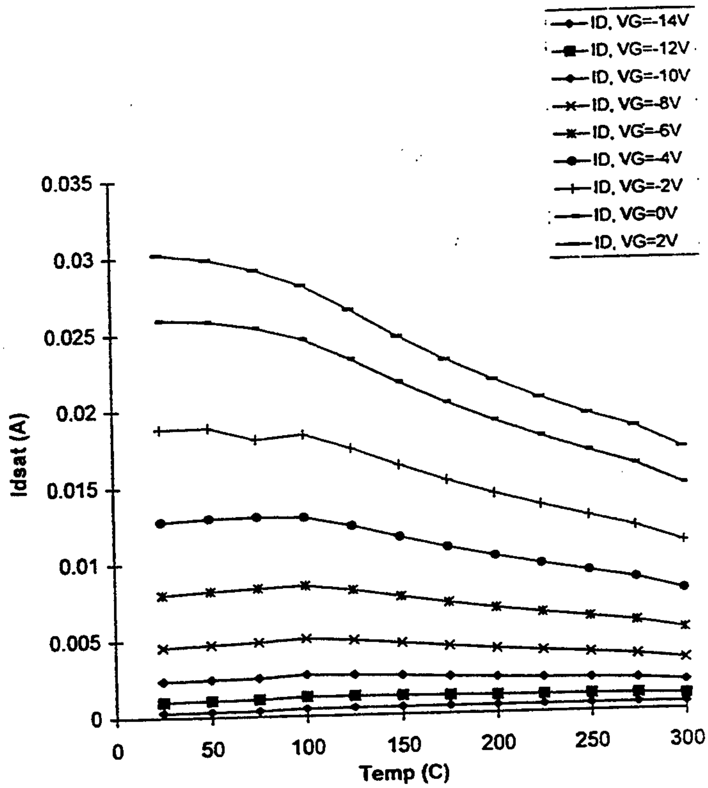

Fig. 3. The effect of temperature on saturation drain current, I_{dsat}, of a typical SiC BGJFET studied.

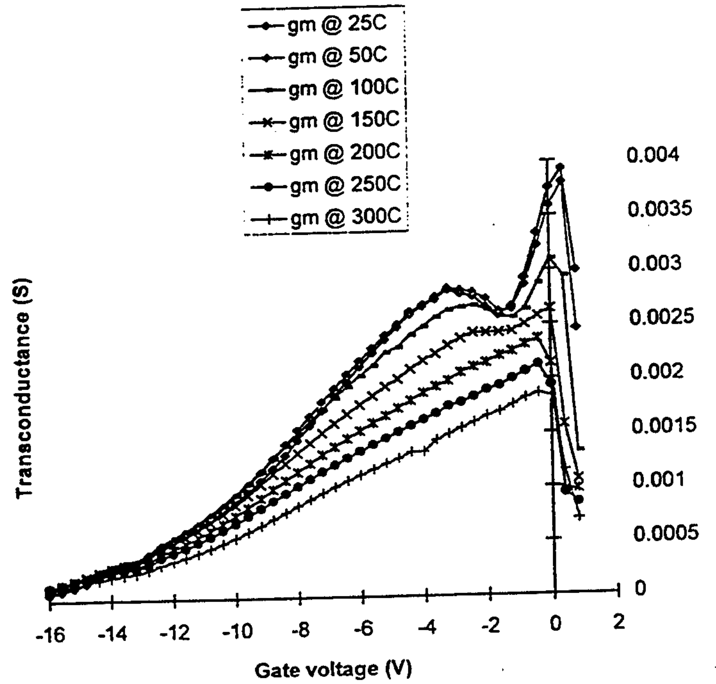

Fig. 4. The effect of temperature on device transconductance.

temperatures. For this device, the DC transconductance was 5.26 mS/mm (normalized as per unit gate width) at $V_{ds} = 25V$ and $V_{gs} = 0$ to 0.5 volt at room temperature. The DC transconductance decreased to 2.89 mS/mm at 300°C for the same bias conditions. The decrease of the transconductance can be attributed to the reduction of electron mobility in the channel [4].

Figure 5 illustrates the effects of temperature on channel conductance. It can be seen that the output conductance decreases with temperature in the linear region. In the saturation region, however, the channel is pinched-off, and the channel conductance is very small.

The channel conductance in the saturation region ($g_{d,sat}$) is a measure of the flatness of the Id-Vds curves in saturation. Figure 6(a) and (b) shows $g_{d,sat}$ as a function of temperature for the SiC BGJFETs. As can be seen from these figures, $g_{d,sat}$ varies very insignificantly with temperature. This property of constant channel conductance is very desirable for high temperature device applications.

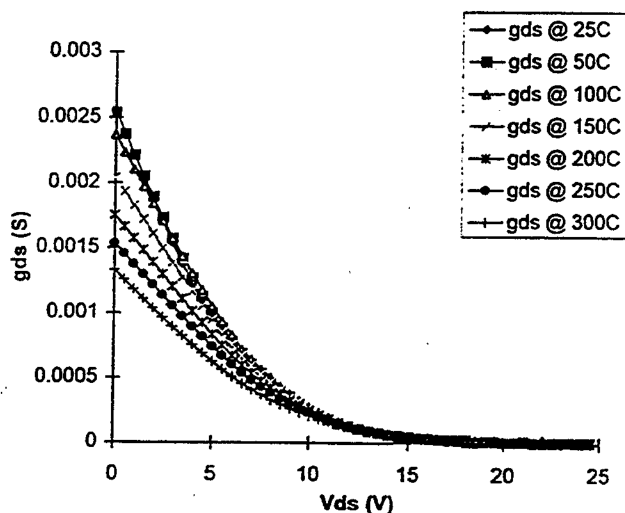

Fig. 5. The effect of temperature on channel conductance of the SiC BGJFET.

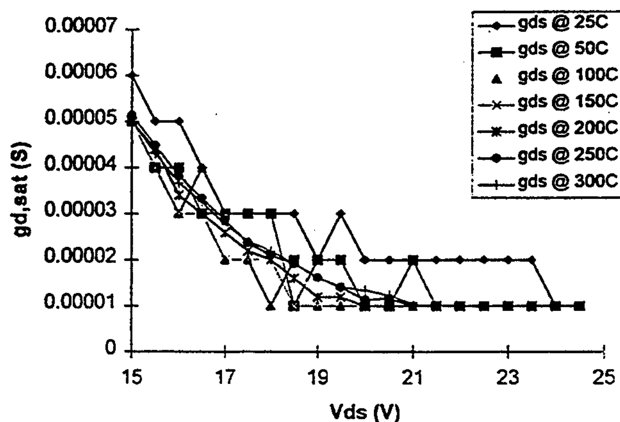

Fig. 6a. The effect of temperature on gd,sat of the BGJFET, with the V_{ds} sweep shown.

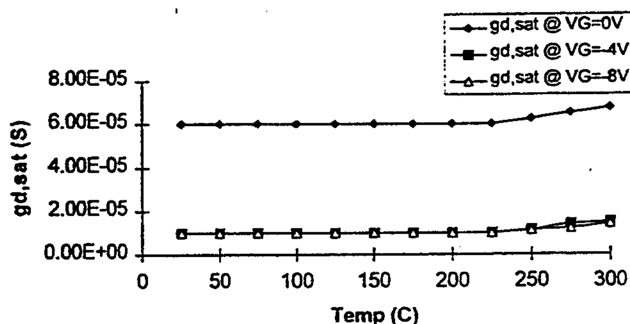

Fig. 6b. The effect of temperature on saturation channel conductance.

Based on the characterization result, it is concluded that these devices are extremely stable and highly promising for high-temperature applications. Well-behaved transistor operations were observed in the tested temperature range. The measurement results indicate that the buried-gate structure helps greatly to isolate the channel from the substrate even at elevated temperatures.

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OHMIC CONTACTS TO n-GaN

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Owing to their wide bandgap, III-V nitrides are attractive for high temperature, high-power applications. Forming low-contact resistance, thermally stable, and uniform Ohmic contacts to wide bandgap materials such as GaN, with a bandgap of approximately 3.4 eV, is, therefore, receiving increased attention. In this work, Cu_3Ge was studied as an Ohmic contact to n-GaN. The specific contact resistance of Cu_3Ge, the contact morphology, and the thermal stability of Cu_3Ge on n-GaN will be presented in this paper.

Contact layers of Cu-Ge alloy with 25% Ge were prepared by sequentially depositing a Ge layer on top of the Cu layer on n-GaN epitaxial layer with moderate doping. This deposition was performed at room temperature and followed by an annealing procedure. The Cu and Ge layer were deposited using electron-beam evaporation under a pressure of 2×10^{-6} Torr at a rate of 4Å/sec. The contact formation was carried out by annealing the samples at 400°C for 30 minutes at a pressure of $\sim 5 \times 10^{-6}$ Torr. The specific contact resistance was determined by the transmission line measurement (TLM) method. Two sets of TLM patterns having dimensions of 210 µm × 210 µm and 260 µm × 210 µm, with spacing ranging from 20 µm to 160 µm were prepared to measure the contact resistivity.

Figure 1 represents the relationship of the contact resistance versus pad spacing obtained from TLM.

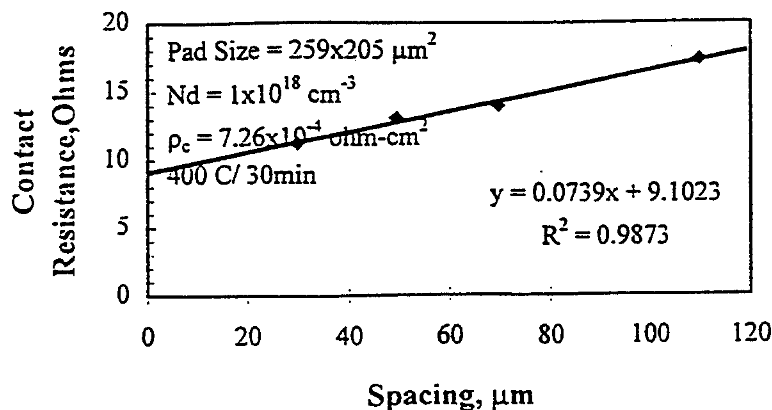

Fig. 1. Contact resistance versus pad spacing for Cu_3Ge Ohmic on n-GaN using TLM.

The contact resistivity of Cu_3Ge on n-GaN determined by TLM ranged from $7.2 \times 10^{-4} \sim 1.4 \times 10^{-3}$ Ω cm^2 after 400°C/30 minute annealing. For lightly doped GaN, this specific contact resistivity is very low. The Ohmic behavior of Cu_3Ge on n-GaN can be

interpreted by tunneling through the heavily doped GaN layer which is formed by the substitution of Ga sites by Ge.

It was found that Cu_3Ge has a good wetting on n-GaN and a reasonable smooth surface which are important issues for forming a good contact. Aging tests of Schottky diode on GaAs, where Cu_3Ge was used as Ohmic contact covered by 4000Å of Au and with 400Å TiW as diffusion barier, concluded that the contact has superior thermal stability even after it was exposed at 300°C for 500 hours in the atmosphere.

Thermal stability of both Pd/Al and Ti/Al Ohmic contacts to n-GaN were also studied in this work. Pd/Al and Ti/Al were deposited using electron beam deposition followed by furnace annealing in an N_2 ambient. Different diffusion barriers were deposited using sputter deposition to test the thermal stability of these Ohmic metallization schemes.

After annealing at different temperatures, the current-voltage characteristics of Pd/Al contacts were obtained; the results are shown in Fig. 2. The thickness of Pd and Al are 125Å and 1000Å, respectively. Rectifying behavior was observed for as-deposited Pd/Al from the current-voltage characteristics. This is expected as the work function of Pd (5.12 eV) is larger than the electron affinity of GaN (4.07 eV).

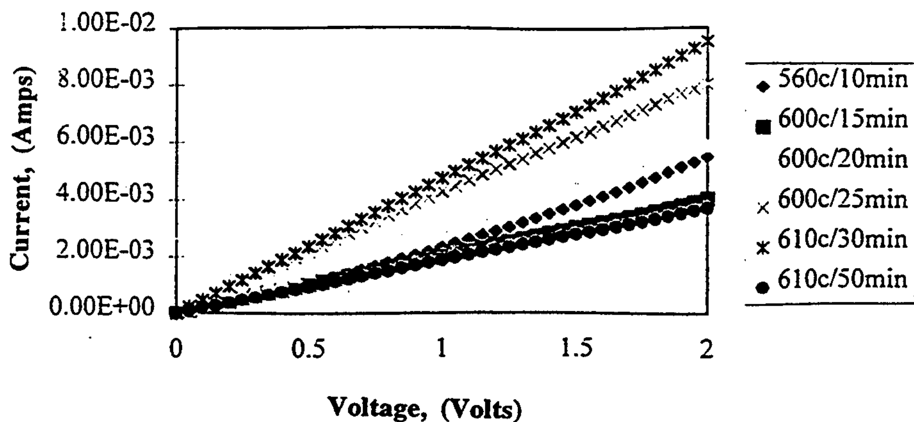

Fig. 2. I-V characteristics of Pd/Al on n-GaN at various temperatures and time.

For Pd/Al contacts, the best furnace annealing condition was found to be 610°C for 30 minutes in the N_2 ambient. Figure 3 shows the specific contact resistances of this metal scheme on n-GaN. These contacts were found to remain Ohmic at temperature up to 670°C, but with severe surface oxidation. Pd/Al contacts were Schottky if the annealing time was less than 15 minutes at 600°C. This implies that the Ohmic behavior could be due to the formation of Al/n-GaN interface which has a low Schottky barrier height. Further annealing increased the contact resistance by the formation of Al_xN_{1-x}/n - GaN [1].

Figure 4 shows the specific contact resistance of Ti/Al on n-GaN as a function of annealing time at 600°C. For Ti/Al contacts on n-GaN, annealing times less than three minutes in the furnace resulted in Schottky I-V characteristics. The best annealing time was found to be five minutes.

It was also found that the I-V characteristics of Pd/Al changed from Ohmic to Schottky after aging at 350°C for only two hours, whereas the Ti/Al specific contact

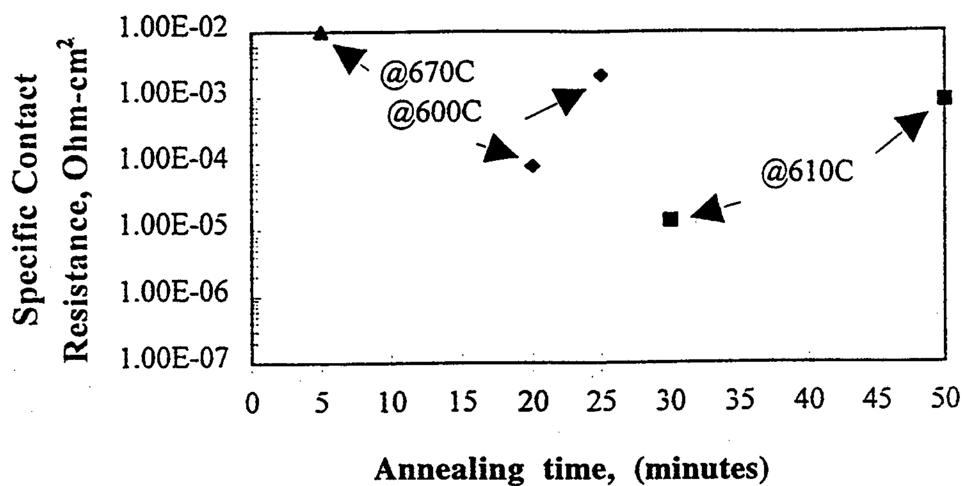

Fig. 3. Specific contact resistance as a function of annealing time at various temperatures for Pd/Al on n-GaN.

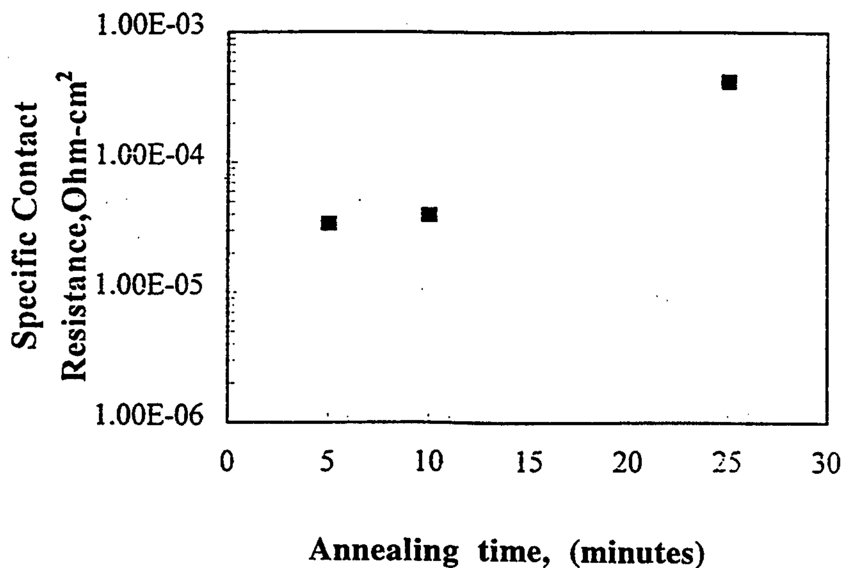

Fig. 4. Specific contact resistance as a function of annealing time at 600°C for Ti/Al on N-GaN.

resistance remained the same even after an aging of 130 hours at 350°C and of 40 hours at 400°C.

In conclusion, the lowest specific contact resistivity obtained from Cu_3Ge on n-type α-GaN is 7.2×10^{-4} Ω.cm^2 after 400°C/30 min annealing. This result is most likely due to the creation of Ge-doped n^+ GaN layer which is suitable for forming a tunneling junction. The thermal stability of Pd/Al and Ti/Al contacts on n-GaN has been studied. The thermodynamic equilibria between metals and GaN will be used to interpret the results and possible transport mechanism will be discussed.

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Circuits with Organic Transistors

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Organic field-effect transistors (FETs) have been investigated by many groups over the past decade [1]. The motivations for this activity range from the use of the FET as a means to study charge transport phenomena to the development of technologies that could be used in future large-area and/or low-cost electronics. The demonstrated compatibility of organic/polymeric FETs with plastic substrates and the successful use of fabrication techniques such as printing in the fabrication of FETs are significant steps toward the realization of low-cost circuits [2,3].

The applications being envisaged for organic FETs include smart cards and electronic price labels [4] and displays. Simple circuits such as inverters and ring oscillators with organic FETs have been reported. These include circuits made entirely of p-channel transistors [4] as well various kinds of complementary and quasi-complementary circuits [5,6]. The advantages of complementary circuits are very well known: low static power dissipation, better noise margins, and comparatively simple circuit design. In the following, we review the various approaches to complementary circuits that we have proposed.

One of the early difficulties of realizing an organic FET based CMOS technology was that the few known materials which formed n-channel FETs were very unstable in air. This was particularly true of C_{60}, which despite possessing mobilities ~ 0.1 $cm^2/V\text{-}s$ [7], was not useful in circuits. To

circumvent this difficulty, we initially proposed the combination of relatively reliable p-channel organic FETs with established amorphous silicon n-channel FET technology. Inverters made with this hybrid technology possessed excellent transfer characteristics [5]. Many p-channel FET forming organic materials have been reported in recent years, with many possessing field-effect mobilities in excess of 0.03 $cm^2/v\text{-}s$. The hybrid organic-inorganic CMOS circuitry would involve a-Si fabrication technology. This would neither be very low-cost nor would it be compatible with plastic substrates. As a result, significant efforts were directed to find improved organic materials which form more stable n-channel FETs.

Laquindanum *et al.*, found that many compounds based on the naphthalene group did form comparatively stable n-channel FETs with mobilities > 10^{-3} $cm^2/V\text{-}s$ [8]. In particular, the material TCNNQD was found to be quite air-stable. Subsequent advances in this general area will be reported.

Inverters were fabricated with p-channel materials such as pentacene and copper phthalocyanine and naphthalenetetracarboxylic dianhydride (NTCDA) as the n-channel material. Very good inverter transfer characteristics were obtained, for both n-channel loads and p-channel loads. This demonstration showed that more complicated complementary circuits could be built with all organic FET technology.

To simplify the fabrication of complementary circuits, we have shown that it is not necessary to pattern the active materials. We have developed a unique organic transistor structure with two active materials which enables us to realize both p-channel and n-channel operation in a single device [9]. The availability of such devices will simplify the fabrication of complementary circuits. The active material consists of two layers: the first (adjacent to the gate dielectric) layer is made up of a material such as α-hexathienylene (α-6T), which exhibits good p-channel operation. This layer is typically 10-20

nm thick. The second active material is chosen for good n-channel operation, and is typically about 20-40 nm thick. The choice of the two active materials must be made taking into account both transport properties and energy levels of the highest occupied and lowest unoccupied molecular orbitals. The energy levels of the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) of the two materials must be such that when the gate is biased negatively with respect to the source, the p-channel material is filled with holes and when the gate is biased positively, the n-channel material is filled with electrons.

In summary, many approaches to fabricating logic circuits based on organic transistors have been outlined. Future improvements in fabrication technology and device reliability will lead to the demonstration of more complicated integrated circuits.

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Organic Thin Film Transistors

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Interest in organic thin film electronic devices, especially electroluminescent devices and field-effect transistors, has increased rapidly in the past several years. The performance of both has improved significantly in this period, and it now seems fairly likely that such devices will find application in commercial products. Organic thin film transistors (OTFTs) in particular have potential for use in active-matrix flat panel displays (both liquid-crystal and organic-emissive) and in low-cost electronic applications (e.g. smart cards, or smart inventory tags).

Organic semiconductors have been of scientific interest for more than forty years, but devices with potentially useful properties have only recently emerged. Since materials that allow bipolar conduction are not common, work on transistor structures has focused on field-effect devices, typically in thin-film form. However, early organic thin film transistor field-effect mobilities were disappointingly low, typically in the 10^{-5} to 10^{-6} cm^2/V-s range, and far too low for most applications [1-3].

More recently, OTFT research has focused on small-molecule organic semiconductors. This change of focus, initially concentrating on α-sexithienyl as the active material, gave dramatically improved field-effect mobility with best results in the 10^{-2} to 10^{-1} cm^2/V-s range [4,5]. Small-molecule organic semiconductors, including α-sexithienyl, often exhibit a strong tendency to form molecular crystals even when deposited on amorphous substrates held at room or somewhat elevated temperature; this molecular ordering may be responsible for the improved mobility [6].

Figure 1 shows the I_D-V_{DS} characteristics of an α-sexithienyl TFT. This transistor uses a silicon wafer as a convenient substrate and gate electrode and thermally grown silicon dioxide as the gate dielectric. The α-sexithienyl active layer was deposited by thermal evaporation with the substrate held at 85 °C. Gold source and drain contacts were deposited by evaporation through a shadow mask; the resulting TFT has a channel length and width of 20 and 220 μm, respectively.

The α-sexithienyl device shown has a mobility near 0.02 cm^2/V-s and an on/off current ratio of about 10^5. The best devices reported using α-sexithienyl or closely related materials have mobility approaching 0.1 cm^2/V-s and on/off current ratio larger than 10^6 [7,8]. Although these results are each about one order of magnitude less

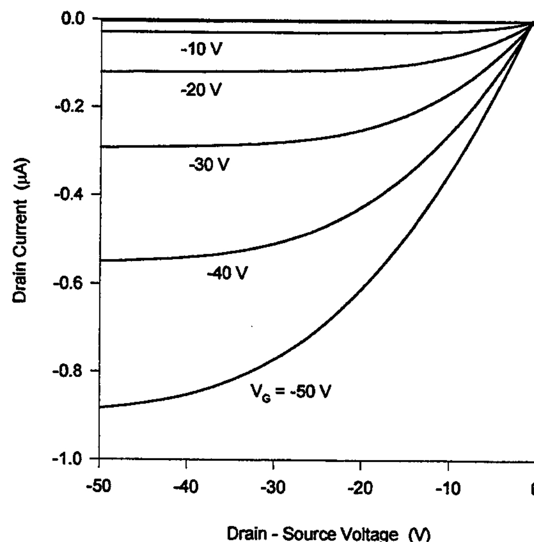

Fig. 1. I_D-V_{DS} characteristics of α-sexithienyl TFT with 20 μm channel length and 220 μm channel width.

than typically obtained for hydrogenated amorphous silicon TFTs, they are approaching the range that may allow use in displays or other applications.

A variety of other materials including metallopthalocyanines [9], oligophenyls [10], and naphthalene derivatives [11] show promise as small-molecule organic semiconductors in TFTs. We have investigated the small-molecule aromatic hydrocarbon pentacene and find that devices fabricated using this material as the active layer can have improved performance compared to α-sexithienyl-based devices. For TFTs fabricated with pentacene layers deposited directly onto silicon dioxide gate dielectric we have obtained mobility near 0.7 $cm^2/V\text{-}s$ and on/off current ratio near 10^8. However, these devices typically have a large positive threshold voltage and large subthreshold slope; large subthreshold slope is also typically observed for α-sexithienyl and other organic TFT active materials.

The large subthreshold slope typically observed for organic TFTs may, in the case of small-molecule materials, be related to the tendency to form molecular crystals. Molecular crystal growth may result in an interface with the underlying gate dielectric that is weakly bonded and poorly controlled, but this interface is critical to operation of the field-effect TFT.

To improve the gate-dielectric/active-layer interface we have investigated the use of self-organizing monolayers [12]. Figure 2 shows the I_D-V_{DS} characteristics and Figure 3 shows the $\sqrt{I_D}$-V_{GS} characteristics for a TFT fabricated by depositing pentacene onto a silicon dioxide gate dielectric treated with octadecyltrichlorosilane (OTS) and held at 60 °C. This device has a mobility near 1.3 $cm^2/V\text{-}s$ and a low threshold voltage.

The α-sexithienyl and pentacene OTFTs described above used shadow masking to define source and drain contacts, but photolithographic or other relatively high-resolution techniques are likely to be necessary for most OTFT

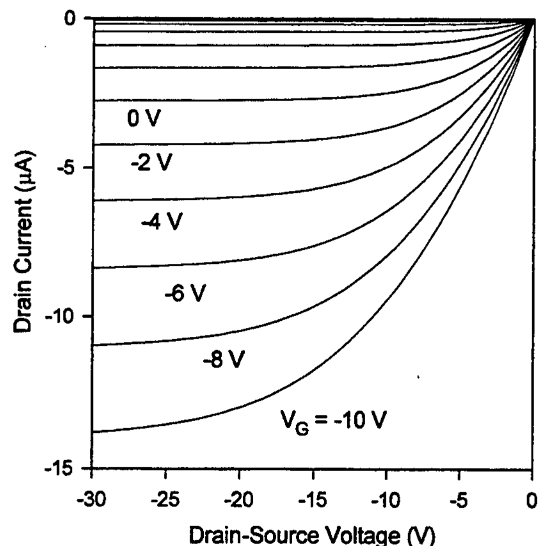

Fig. 2. I_D-V_{DS} characteristics for a TFT fabricated by depositing pentacene onto a silicon dioxide gate dielectric treated with octadecyltrichlorosilane (OTS)

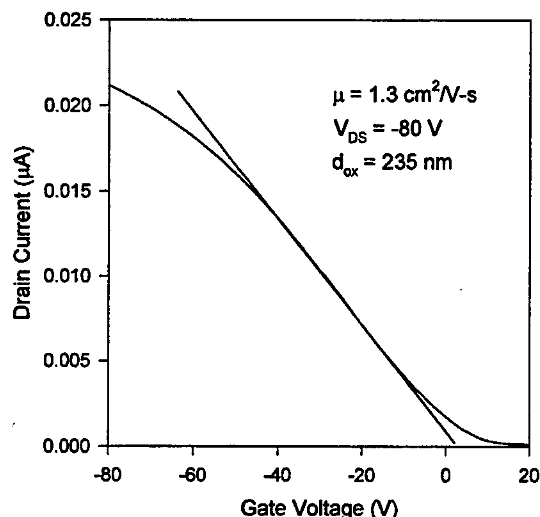

Fig. 3. $\sqrt{I_D}$-V_{GS} characteristics for a TFT fabricated by depositing pentacene onto a silicon dioxide gate dielectric treated with octadecyltrichlorosilane (OTS).

applications. However, α-sexithienyl, pentacene, and many other materials of interest for organic electronics are strongly affected by exposure to solvents and other processing chemicals, often even when the organic material is not attacked in a bulk sense. One approach to minimize the exposure of OTFT active materials to processing chemicals is to use gate electrodes and source and drain contacts deposited and patterned prior to

active layer deposition. However, this leads to devices with source and drain contacts on the same side of the active layer as the gate-accumulated carrier channel and thus only a very small contact area between the channel and the contact since the channel is not accumulated above the source and drain contacts. Shadow-masked top contacts require carriers to travel through an unaccumulated region of active material, but, for devices with gate/source and gate/drain overlap, provide a much larger area for current transport between the accumulated channel and the contacts. For both α-sexithienyl and pentacene OTFTs we have found that top contact (large area) source/drain contacts typically provide better performance.

For bottom contact pentacene OTFTs we have also found that device performance typically improves with increasing substrate temperature during pentacene deposition. However, atomic force microscopy (AFM) reveals that pentacene films deposited even at fairly low temperatures are quite three-dimensional with micron-sized dendritic grains (even when deposited on amorphous substrates) and that film roughness tends to increase with increasing substrate temperature, particularly for OTS-treated substrates. Films deposited onto OTS-treated SiO_2 substrates held near 90 °C often have regions where material has not grown. Device-to-device variability is greater for OTFTs fabricated using such films, likely due to the observed film voids.

To minimize this film connectivity problem we have used a dual-layer pentacene approach [13]. After depositing and photolithographically patterning source and drain contacts, a first layer of pentacene is deposited at relatively high temperature to form good bottom contacts. Next, a layer of pentacene is deposited at low temperature to fill in regions with no initial film growth. Figure 4 shows the $\log(I_D)$-V_{GS} and $\sqrt{I_D}$-V_{GS} characteristics for a stacked-pentacene device using a 30 nm initial layer deposited with a substrate temperature of 90 °C and a 20 nm second layer deposited at room temperature. This device had a field-effect mobility near

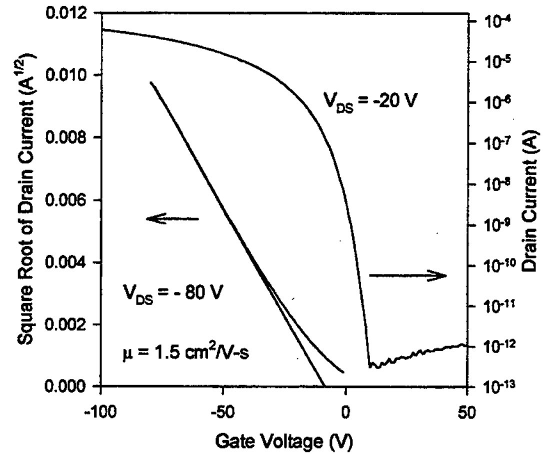

Fig. 4. $\log(I_D)$-V_{GS} and $\sqrt{I_D}$-V_{GS} characteristics for a stacked-pentacene device using a 30 nm initial pentacene layer deposited with a substrate temperature of 90 °C and a 20 nm second layer deposited at room temperature.

1.5 cm^2/V-s, a low threshold voltage, an on/off current ratio greater that 10^8, and a subthreshold slope less than 1.6 volts/decade.

The device shown in Figure 4 used heavily doped single crystal silicon as a convenient substrate and gate electrode with thermally grown SiO_2 as the gate dielectric. For displays and other applications device fabrication on glass, polymer, or other substrates is of interest. Figure 5 shows a stacked-pentacene TFT fabricated on a glass substrate and using a patterned nickel gate electrode, patterned palladium source and drain contacts and a patterned ion-beam-deposited silicon oxide gate dielectric [15]. This device had a field-effect mobility near 0.2 cm^2/V-s; it is

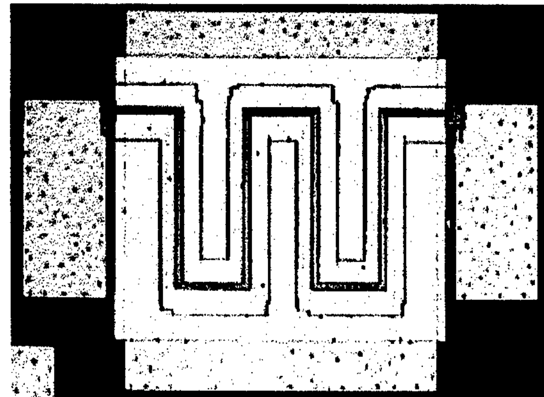

Fig. 5. Microphotograph of stacked-pentacene OTFT with patterned electrodes and gate dielectric.

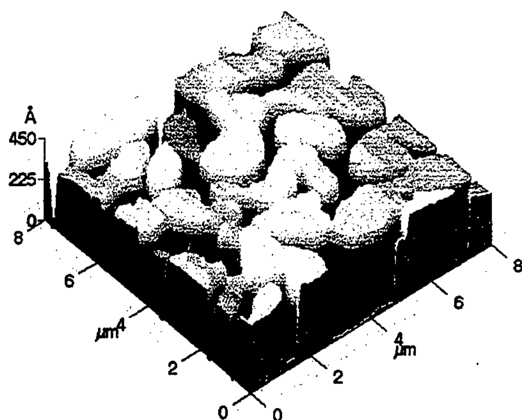

Fig. 6. Atomic force image of quaterphenyl deposited onto SiO_2 held at 60 °C.

likely that performance similar to that obtained on silicon substrates will be possible.

The film connectivity problem observed for pentacene films may also affect other materials of interest for OTFTs. For example, OTFTs fabricated using sexiphenyl active layers have been reported [10], but other reports have not found transistor action [14]. For quaterphenyl we have obtained both results (OTFTs with mobility near 0.01 cm^2/V-s, and devices with little or no transistor action) for different, but nominally identical, deposition runs. Figure 6 is an AFM image of a quaterphenyl layer deposited onto SiO_2 held at 60 °C. It is clear that film connectivity may severely impact device performance for this film, even if carriers can be accumulated in individual grains.

It is likely that OTFT performance will continue to improve. Device processing will require significant changes from the techniques used with inorganic semiconductors, particularly for low-cost applications, but workable approaches are developing.

Acknowledgements

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Organic and Polymeric Thin-Film Transistors and Their Underlying Structural Requirements

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The last few years have witnessed high and growing interest in organic and polymeric materials as active components for electronic devices. This is driven by the potential advantages of such devices, which include much more facile fabrication (e.g. sublimation, solution- or melt-processing) and better thermomechanical compatibility with plastic substrates. The ultimate vision would be all-plastic devices for, e.g., thin, flexible flat-panel displays that could be printed onto a plastic roll through a continuous, ambient-temperature printing process.

Organic thin-film-transistors (TFTs) were first demonstrated in a hexamer of thiophene (α-hexatiophene or α6T) beginning with the pioneering work by Garnier and co-workers.[1, 2] In our studies we have examined a broad variety of organic and polymeric materials in an attempt not only to identify those with the best electronic properties, but also to understand fundamentally and in a predictive manner their dependence upon chemical and molecular structure, crystallization, morphology, and substrate orientation.

In terms of chemical structure, materials that are good candidates for TFTs have conjugated or fused aromatic structures. Among the former, thiophene oligomers and polymers have been foremost in terms of mobility and source-drain-current on/off ratios. Typical values for α6T or di-hexyl α6T are 0.02-0.05 cm^2/Vs and 10^6, respectively;[3, 4] for di-hexyl α4T (i.e. the tetramer of thiophene) we very recently achieved mobilities up to 0.23 cm^2/Vs.[5] α6T is a high-melting and poorly soluble material which is therefore commonly deposited by vacuum evaporation, while the di-hexyl-substituted α6T and α4T, and regular hexyl-substituted polymeric thiophenes, are soluble in organic solvents and can therefore be deposited by solution casting and spin coating. Fused organic compounds are actually the ones that have yielded the highest mobilities to date. For pentacene[6, 7] and anthradithiophene,[8] mobilities of 0.2-1.0 cm^2/Vs (or even higher) have been reported; these are similar to those of amorphous silicon. On the other hand, there are other fused-ring organics (such as

naphthalene tetracarboxylic dianhydride (NTCDA) or its perylene analog (PTCDA)) that give orders of magnitude lower mobilities.

What is the reason for this wide variability in electrical characteristics? This brings us to the next levels of structure, i.e. those of the intermolecular packing (i.e. unit-cell structure) and molecular orientation on the device. For efficient electronic transport the molecules must be packed in the unit cell in such a way as to maximize overlap of their π–π molecular orbitals. In polythiophenes the molecular chains are coplanar and parallel to each other, ensuring good overlap of their molecular orbitals.[9] Another efficient way to accomplish this for chain molecules is to be arranged in a herringbone pattern with the molecular chains parallel; this is the case for α6T and other thiophene-based organic materials. [10, 11]

However, this is not sufficient by itself: the relative orientation of these molecules on the substrate is also of paramount importance. For maximal efficiency in electronic transport, the direction of π–π molecular overlap must coincide with the direction from the source to the drain electrode. In thin-film transistors this is parallel to the substrate, which means that the molecules should optimally be perpendicular (or close to that) to the substrate. This is in fact the case for most of the organic and polymeric TFT materials (e.g., α6T and its analogues, anthradithiophene, etc.), as we were able to show using X-ray and electron-diffraction analyses.[8,10] In some of these, such as the phthalocyanines,[12] the planar molecules are deposited slightly off-normal to the substrate and arranged in layers with alternating inclination. We were able to demonstrate clearly the role of molecular orientation on the substrate through study of PTCDA[13] and NTCDA,[14] which have extremely similar chemical structures but organize themselves differently upon evaporation on the device substrate. PTCDA, which deposits its molecules close to parallel to the substrate has mobilities at least two orders of magnitude lower than NTCDA, whose molecules arrange themselves edge-on a chevron-like pattern.

The final level of organization that controls the electronic properties of organic and polymeric TFTs is the morphological one, i.e. the growth habit of the molecules leading to macroscopic crystals and polycrystalline aggregates. In most of these materials, we found through electron-microscopic investigation that the morphology consists of very small, irregular grains (generally in the 100 nm range).[9, 11-14] The small size and irregularity of these grains does not preclude reasonable mobilities as long as the crystals are in good contact. Of course, larger,

more perfect, flat crystals are far more preferable. One can obtain crystals in the μm range by slow crystallization from the melt, as was done for α6T. However, these undergo transverse fracture during cooling to room temperature, so that the effective coherence length is reduced.[11] Another way to attain very large crystals is by vacuum deposition onto heated substrates. In most cases, however, nucleation at such high temperatures is very sparse so that the resulting large and regular single crystals end up being separated far from each other and therefore allow no macroscopic current between source and drain.[12] It should be noted that the crystal growth habit is to a large extent an inherent characteristic of each material. We have in fact studied a number of compounds that fulfill the necessary structural and orientational requirements and that even grow crystals of high regularity and perfection, but whose habit is that of small, three-dimensional crystals (e.g., cubic or pyramidal) instead of the desired flat, two-dimensional (lamellar) ones. These are therefore not useful as semiconducting thin-film materials.

The best morphological characteristics so far have been achieved for pentacene[6,7] and dihexyl-substituted α4T.[5] These materials yield flat, large single crystals (sometimes tens of μm) at fairly mild substrate temperatures (≤85°C), in good contact with each other, and with the preferred perpendicular molecular orientation. As a result, these two compounds are in fact the two with the highest mobilities to date (0.2 cm^2/Vs for dihexyl α4T and 1 cm^2/Vs for pentacene). These results demonstrate the demanding hierarchical levels of molecular and supramolecular organization that must coexist in order to provide organic and polymeric thin-film transistors with competitive electronic properties to those of silicon.

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Processing and Integration Issues in Organic Light Emitting Diode Displays

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Abstract

The impact of system issues such as power dissipation and full color capability on process and device integration is examined. Power dissipation is especially important because of the self-heating of the display. Specific areas which have been examined are the integration of TFT's and OLED's together to form an active matrix, rugged substrates, and methods to integrate different patterned organic layers onto a common substrate

Introduction

Since the seminal work of Tang and Van Slyke [1] there has been an increasingly strong interest in developing flat panel displays based on organic LED's (OLED's), either based on polymers or small organic molecules [2,3,4]. While most research has focused on improving the performance or stability of isolated devices, consideration of the final display product as a system introduces new issues to be considered. Using the system drivers of power dissipation and full color, we show that the ability to integrate both optimum organic layers for individual red, green, and blue devices and thin film transistors (TFTs) for an active matrix architecture is highly desirable for a system. We then examine several issues in these areas from a process technology point of view.

System Motivation

The system power efficiency is especially important for displays based on OLED's because the stability of the organic materials and interfaces and the device reliablity are critical issues which depend on temperature [5-8]. Therefore the self-heating of devices must be understood. We have measured and modelled the self-heating of flat panel displays as a function of their power dissipation density, orientation, and size [9]. The experimental results for a power density of 220 W/m^2 are shown in Fig. 1 for plates of both horizontal and vertical orientation. Note that for a fixed power density, the self-heating rises sharply as the display size increases. Modeling shows this effect to be due to a rapid drop in convection efficiency at larger dimensions [9]. Because OLED device efficiencies are typically on the order of several lumens/Watt (assume 3 lm/W), operating at a typical brightness of 100 cd/m^2 implies a power density of only 105 W/m^2. However, to achieve high contrast in a system, a circular polarizer or other plate (with < 50% transmission) may be used, doubling the required power to 210 W/m^2. Any further substantial power inefficiencies would be highly undesirable because of the resulting self-

heating of the devices would be on the scale of many tens of degrees, leading to premature device degradation.

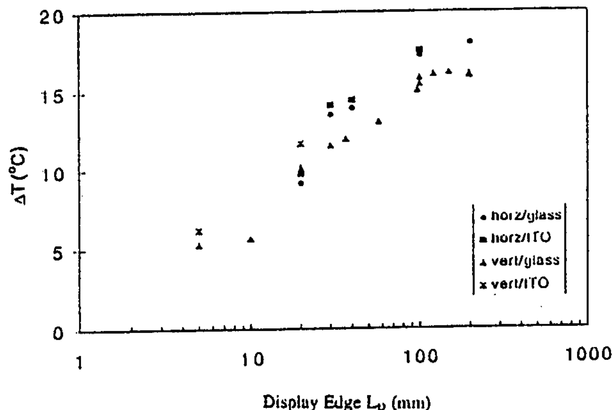

Fig. 1. Measured temperature rise of glass flat panels (on both front and back sides) as a function of edge dimension for both horizontal and vertical orientation for a power density of 220 W/m^2 [9]

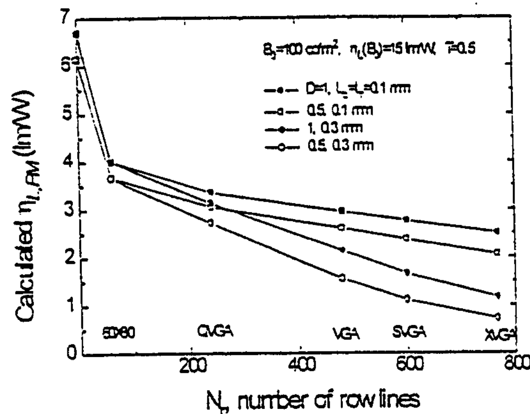

Fig. 2. System power efficiency for a passive matrix display as a function of the number of lines, assuming ITO data lines of 10 Ω/sq, Al row lines of 0.05 Ω/sq, pixel size 0.1 x 0.1 or 0.3 x 0.3 mm^2, device efficiency of 15 lm/W, system brightness of 100 cd/m^2.

In OLED display systems demonstrated to date, the passive matrix addressing approach has been chosen for addressing pixel elements [10,11]. This implies driving them at low duty cycles for very high brightness. Due to the higher OLED voltages and power dissipation in the data and select lines, a much higher drop (easily as large as 4 X) in the system efficiency can occur (Fig. 2). Because such an efficiency drop, and the resulting device temperature increase may be unacceptable, the integration of TFT's with the OLED's for an active matrix (AM) architecture is highly desirable. This solution yields a display with far higher power efficiency, but requires the integration of TFT's and OLED's. Furthermore, many approaches to achieve full color involve inherent energy efficiencies, such as white OLED's followed by color filters. Because of the excessive heating this implies, the ability to integrate different organic layers for optimum R, G, and B devices for color is also highly desirable. Finally, unbreakable substrates (as opposed to glass) would be highly desirable.

TFT Integration on Stainless Steel Foil Substrates

An active matrix architecture allows devices to be operated close to DC, as opposed to the low duty cycles of a passive matrix. The TFT choices for large area applications include amorphous silicon (a-Si) with a μ of ~1 cm^2/Vs and polysilicon (p-Si) with μ ~ 30 cm^2/Vs. To demonstrate that a-Si TFT's are capable of providing appropriate current levels for OLED's, we integrated a-Si TFT's and OLED's onto a common substrate. In place of glass, we chose thin stainless steel foils (thicknesses from 25 to 200 μm) because of their rugged and flexible nature, and because they more easily withstand the process temperatures of a-Si TFT fabrication than plastic substrates. Fig. 3

shows the device structure, in which a standard a-Si TFT is first fabricated on the steel foil. The organic used was the polymer PVK doped with electron transport agents and a dye, a combination which has demonstrated brightnesses in excess of 10,000 cd/m^2 [12]. Because the foils are opaque, a top emitting OLED structure was used with a semi-transparent top contact [13,14]. The transistor W/L ratio was 18 and the OLED diameter was 0.25 mm.

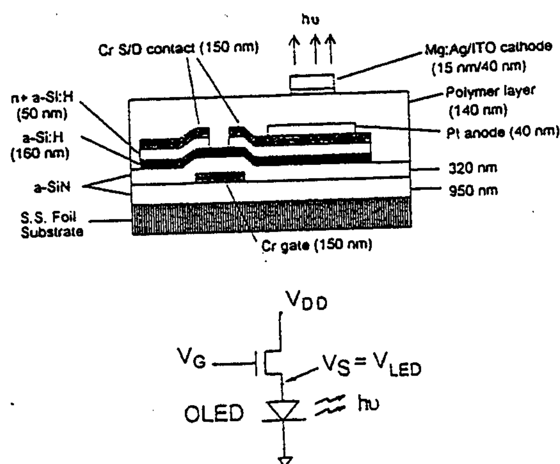

Fig. 3. Cross section of integrated TFT/OLED structure on flexible stainless steel foils.

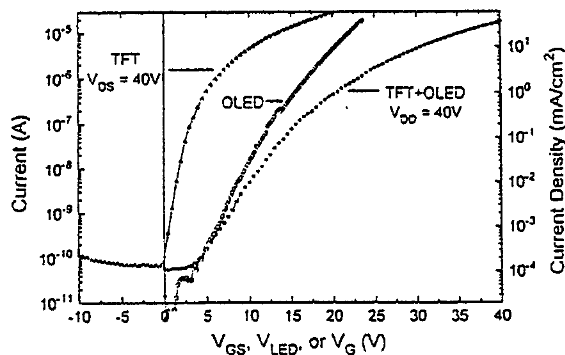

Fig. 4. Current vs voltage of isolated LED (LED voltage), isolated TFT (V_{GS}) and TFT-OLED combination (V_G).

Fig. 4 shows the I-V curve of the isolated LED, isolated TFT, and of the TFT driving the LED in series. The TFT, which was operated in saturation mode, can clearly provide currents densities to the OLED of mA/cm^2, which is typical of that used in OLED applications. Furthermore, because of the rugged nature of the substrates, dropping the foils from a height of 10 m onto concrete had no effect. The 25-μm foils could also be wrapped around a pencil with no change in TFT characteristics.

Full Color Integration

The most power-efficient route towards full color would be direct integration of optimized R,G, and B devices onto a single substrate. This is difficult in OLED technology, however, because the sensitivity of the organics to solvents and water makes their patterning by conventional etching and photolithographic processes problematic. Furthermore, with polymer-based devices, the spin coating of a second polymer layer can cause the dissolution of a previously formed layer. Therefore we have developed the process shown in Fig. 5 which allows us to integrate and pattern multiple organics by spin-coating onto a single substrate [15]. The organic layer is deposited onto a substrate with a patterned insulator, and then patterned by dry-etching using the metal cathode as a self-aligned mask. The sidewall of the device is then coated with metal to seal the edges so that it is stable to further spin-coating and processing. Fig. 6 shows I-V and L-V curves both of a virgin PVK/Alq/nile red device and of the same device after green and blue devices were subsequently integrated onto the same substrate. Note there is no

degradation of the device from the subsequent processing, and operation of the optimized integrated RGB devices has been demonstrated [15].

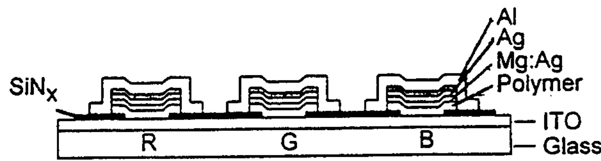

Fig. 5. Structure for integration of multiple organics on a single wafer by spin-coating, using a patterned nitride and metal sidewall sealing.

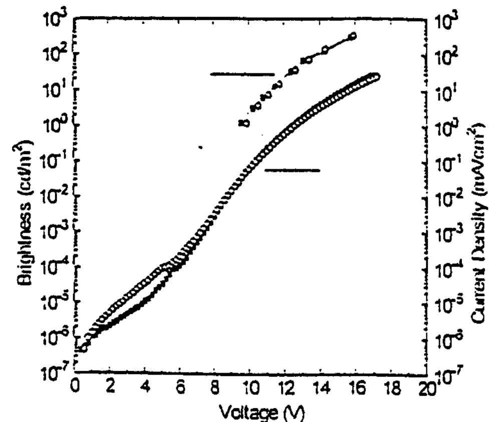

Fig. 6. L-V and I-V curves of both a virgin isolated PVK/PBD/nile red device (squares) and the same device after the fabrication of green and blue devices on the same substrate (circles).

Summary

Key motivations from a system point of view in OLED displays are high system power efficiency (for low self-heating), full color, and ruggedness. These require the integration of TFT's for an active matrix architecture, novel substrates, and novel approaches for the patterning of organic-based devices. This work has been supported by NSF (in part through its Research Experience for Undergraduates Program), the NJ Comm. on Science and Tech., and DARPA (USAF-TPSU-PU-1464-967).

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High Efficiency Photonic Devices Made with Semiconducting Polymers and Their Applications for Emissive Displays and Image Sensors

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Conjugated polymers are a novel class of semiconducting materials which combine the optical and electronic properties of semiconductors with the processing advantages and mechanical properties of polymers. Most of the photonic phenomena known in conventional inorganic semiconductors have been observed in these semiconducting polymers. The dream of using such materials in high performance "plastic" photonic devices is rapidly becoming reality: High efficiency photonic devices fabricated from conjugated polymers have been demonstrated, including light emitting diodes, light emitting electrochemical cells, photovoltaic cells, photodetectors, and optocouplers; i.e., all the categories which characterize the field of photonic devices. The performance parameters of these organic devices have been improved to levels comparable to or even better than their inorganic counterparts.

The molecular structures of several conjugated polymers are shown in Figure 1. Because of the sp^2p_z bonding of these planar conjugated macromolecules, each carbon is covalently bonded to three nearest neighbors (two carbons and a hydrogen); and there is formally one unpaired electron per carbon. Thus, the electronic structure depends on the number of atoms per repeat unit. In the case of poly(paraphenylene vinylene), PPV, the repeat unit contains eight carbons; PPV is a semiconductor in which the fundamental p_z-band is split into eight sub-bands. The energy gap of the semiconductor, the π-π^* gap, is the energy between the highest occupied molecular orbital and the lowest unoccupied molecular orbital.

The quantum efficiency of radiative recombination is high in certain conjugated polymers such as in PPV derivatives. These materials have been used in fabrication of polymer LEDs.[1,2] The emission color can be varied with relative ease by modification of the molecular structure. Emission over the entire visible spectrum has been demonstrated with impressive efficiency, brightness, and uniformity.

The device architecture is the "sandwich" configuration; i.e., a layer of semiconducting polymer laminated between two electrodes, as sketched in Fig. 2. Typical I-V and L-V data from a MEH-PPV LED are shown in of Fig. 2. The device turns on below 2V and reaches 100 cd/m^2 at ~ 2.5 V (the brightness of a TV screen),

4000 cd/m^2 for V~ 4V (the brightness of a fluorescent lamp) and over 10,000 cd/m^2 for V> 5 V. The external quantum efficiency is 2~2.7 % ph/el, and the luminous efficiency is 3~4 lm/W.[3] The device operation lifetime has been improved to >10^6 hour·cd/m^2; i.e., in excess of 10^4 hours at 100 cd/m^2. These numbers are approaching (or comparable) to the lifetimes of ZnS-based and Alq-based electroluminescent devices. The polymer LEDs can be used in fabrication of flat-panel emissive displays, several ptototypes of x-y addressable polymer LED matrices are shown in Fig. 3.

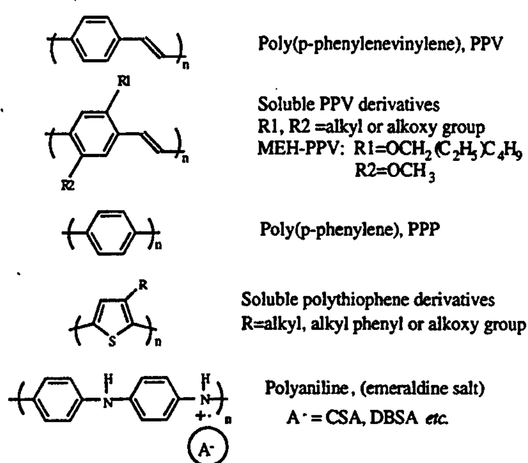


Fig. 1 Molecular structures of conjugated polymers.

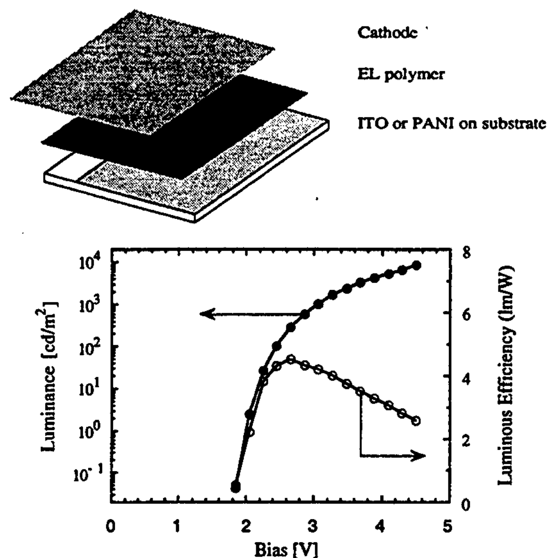
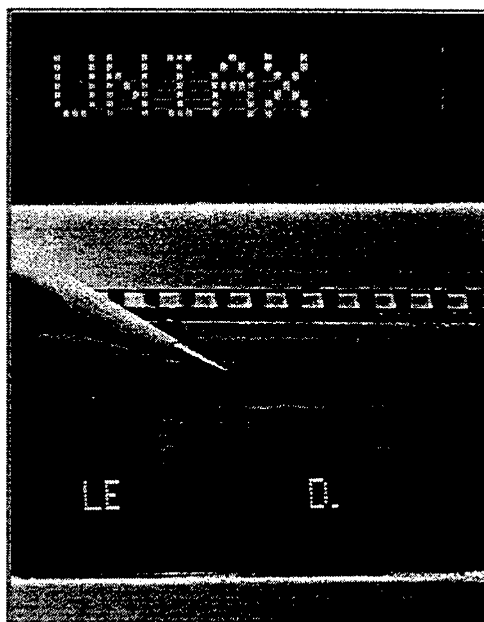


Fig.2 Polymer LED in sandwich configuration (upper panel) and typical data of luminance and luminous efficiency of MEH-PPV LEDs.



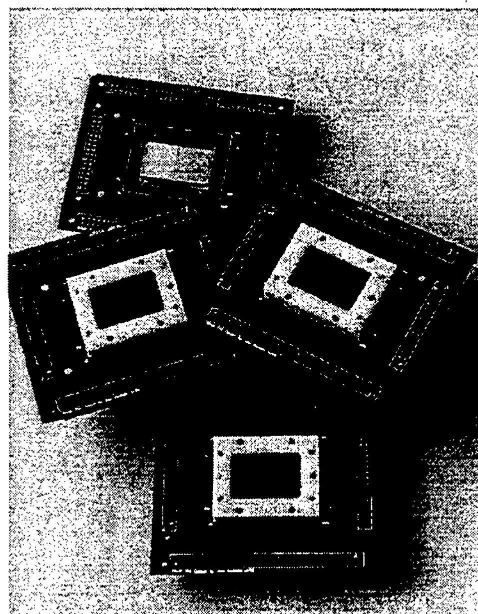


Fig. 3 Prototypes of x-y addressable polymer LED matrices.

By laminating a blend of a luminescent polymer and a solid state electrolyte (such as PEO:Li^+) between two air stable contact electrodes, a dynamic p-i-n junction can be created under external bias.[4] The semiconducting polymer is electrochemically doped p-type on one side and n-type on the opposite side. Light is emitted from the compensated insulating region in the center. Ohmic contacts form at the electrode/polymer interface due to the doping process. As a result, facile electron and hole injection are achieved with stable metals (such as Au) as electrodes. The operation voltages are low, in the range of 2-5 V. Due to the balance of hole and electron injections at the contacts, the external EL efficiencies of polymer LECs are typically high, 2-4% ph/el for EL polymers with red, green, or blue color.

The metal/polymer/metal thin film devices are not only good light emitting devices. They are also good photodetectors. At -10 V bias, the photosensitivity of Ca/MEH-PPV/ITO devices is 45-90 mA/W (10~20% el/ph at 430 nm).[5] In photodiodes fabricated with poly(3-octylthiophene), the photosensitivity is even higher; 0.2-0.4 A/W over entire visible spectral range,[6] comparable to that made with inorganic semiconductors. These polymer photodiodes can be used in fabricating large size, flexible photodiode matrices for image applications. An image obtained by scanning a polymer photodiode array is shown in Fig. 4.

Fig. 4 A color image scanned by a polymer photodiode array.

The photosensitivity in conjugated polymers can be further enhanced by excited-state charge transfer (CT); for example, by sensitizing a p-type polymer with acceptors such as C_{60} or its derivatives.[7] This discovery provided a molecular approach to high efficiency PV conversion.[8] Since the time scale for photoinduced CT is subpicosecond, more than 10^3 times faster than the radiative or nonradiative decay of photoexcitations, the quantum efficiency for CT and charge separation from donor to acceptor is close to unity.

The donor and the acceptor forms interpenetrating phase separated network in the CT blends, which are novel for photovoltaic applications.[7-10] Through

control of the morphology of the phase separation into an interpenetrating bicontinuous net-work of D and A phases, one can achieve high interfacial area within a bulk material: a "bulk D/A heterojunction" material. Because of the interfacial built-in potential, ultrafast photoinduced charge transfer and charge separation will occur with quantum efficiency approaching unity, leaving holes in the donor phase and electrons in the acceptor phase. The continuity of the donor phase and the acceptor phase provide the pathways for the separated carriers to be collected at the external electrodes. PV cells have been fabricated with the CT blends,[8] the carrier collection efficiency at zero bias and the energy conversion efficiency have been improved to ~45% el/ph and 3%, respectively.

By coupling a high efficiency polymer LED with a polymer photodiode, a polymer optocoupler was constructed with current transfer ratio >2×10^{-3},[11] comparable to that of commercial optocouplers made with inorganic semiconductors. These large size, flexible polymer optocouplers and their alternatives by integration with other optical devices provide opportunities of fabricating smart optoelectric devices and processors.

In summary, high performance photonic devices fabricated with semiconducting polymers have been demonstrated, including light emitting diodes, light emitting electrochemical cells, photovoltaic cells, photodiodes and optocouplers. The performance parameters have been improved to levels comparable to, or even better than, their inorganic counterparts. The processing advantages of polymers provide a unique opportunity to make large size, displays and image sensors, on flat, curved and even on flexible surfaces. The field of plastic electronics is moving rapidly from fundamental research to industrial research and development with many interesting and novel opportunities. The dream of using conducting and semiconducting polymers for fabricating novel displays and photosensors is becoming reality.

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Charge quantization effects in nanoscale Josephson devices.

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Current-voltage characteristics of series arrays of small capacitance Josephson junctions display a behavior which is dual to that of ordinary Josephson junctions. A model is derived to explain the experiments which builds on a duality between the Coulomb blockade and the Josephson effect.

I. INTRODUCTION

The Resistively shunted Josephson Junction (RSJ) is the standard model used to simulate the behavior of complicated circuits of Josephson elements. The model describes the lumped element junction as a capacitor in parallel with an ideal Josephson channel and in parallel with a resistor. The current and voltage relations for the ideal Josephson channel are given by the Josephson relations:

$$V = \frac{\Phi_0}{2\pi}\frac{d\phi}{dt} \qquad (1)$$
$$I = I_c \sin(\phi)$$

Where I_c is the critical current of the Josephson junction. The external current, I_{ext} is given by the sum of the currents in each of the three parallel channels. Summing these currents and applying the relations (1), we can derive the following equation.

$$\beta\ddot{\phi} + \dot{\phi} + \sin(\chi) = \frac{I_{ext}}{I_c} \qquad (2)$$

Here the dot means differentiation with respect to a dimensionless variable, which is time is measured in units of the inverse characteristic frequency, $\omega_c = \Phi_0/2\pi I_c R$. The parameter β_c is the Stewart-Mcumber parameter [1,2] , which is given by:

$$\beta_c = \frac{R^2}{C(\Phi_0/2\pi I_c)} \qquad (3)$$

For a given value of β_c , we can calculate the time average voltage (dc voltage) for a given external current, and thus derive the current-voltage (I-V) characteristic. For values of β_c >1 we can have a dc IV curve which is hysteretic -- i.e. it has a region of negative differential resistance [3]. This model and approach serve as the backbone of analysis of Josephson junction circuits.

In very small capacitance Josephson junctions, a different phenomena from the Josephson effect can occur. This phenomena, called the Coulomb blockade is a result of the quantization of electric charge. The Coulomb blockade occurs in small capacitance tunnel junctions, where the charging energy of a single electron, $E_C = e^2/2C$, is appreciable. The Coulomb blockade of Cooper pair tunneling (CBCPT) is relatively well understood for the case of a *single* small capacitance Josephson junction in an arbitrary linear electrodynamic environment (for a review see [4]). If the impedance of the environment at high frequency (GHz) is greater than the quantum resistance $R_Q = h/4e^2 = 6.45k$, the phase difference across the junction is no longer measurable due to large quantum fluctuations. In this case one measures the quasicharge difference across the junction, χ [5]. In terms of the quasicharge, the measured current and voltage are given by a set of relations which are dual to the Josephson relations

$$I = \frac{2e}{2\pi}\frac{d\chi}{dt} \qquad (4)$$
$$V = V_c saw(\chi)$$

Here, $saw(\chi)$ is a 2π periodic function and V_c is the critical voltage. The critical voltage is a function of the ratio E_J/E_C, where $E_J = \Phi_0/2\pi Ic$ is the Josephson coupling energy. An analytic expression for $V_C saw(\chi)$ can be derived from properties of the solutions of the Mathieu equation.

The dimensionless quasicharge, which is a continuous variable, is the quantum mechanical complement of the Josephson phase. comparison

of (1) and (4) shows that the quantum mechanical principal of *complementarity* has given rise to an interesting electrodynamic *duality* between phase and quasicharge, current and voltage, flux and charge, inductance and capacitance, etc. Here we describe experiments where χ is the measurable quantity, and a description of the electrodynamics of the circuit in terms of (4) is appropriate.

II. THE MODEL

Recent experiments [6] with *series arrays* of small capacitance Josephson junctions have demonstrated the CBCPT, even when the array is in a low impedance environment, $Re[Z_{env}] << R_Q$. We believe that this possible due to the considerable Josephson inductance of the array. Treating the Josephson tunneling as an effective inductance, $L_J = \Phi_0 / 2\pi I_c$, which is valid for small ϕ, we find that a semi-infinite 1D array has an impedance,

(5) $$Z_A(\omega) = R_Q \sqrt{\frac{4E_C}{E_J}} \sqrt{\frac{C}{C_0}}$$

$\omega^2 << 1/L_J C$

In order that the parameter V_C not to be too small, and in order to avoid Zener tunneling events [5], we require that $E_J/E_C = 1$. Equation (5) then shows that $Z_A > R_Q$ when $C_0 << C$. Thus our effect is purely one of scale and geometry. The junction capacitance must be small enough so that the charging energy $E_C > k_B T$, and the junctions closely spaced so that the capacitance to ground of each electrode is much smaller than the junction capacitance.

When the CBCPT is observed, equs. (4) are valid. Analysis of the series array then leads to a Sine-Gordon-like model [6] which is a nearly exact dual to the parallel array of ordinary Josephson junctions. If damping is included, in several important limits the model can be reduced to,

(6) $$\beta_L \ddot{\chi} + \dot{\chi} + saw(\chi) = \frac{V}{V_c}$$

Here the dot means differentiation with respect to a dimensionless variable, which is time is measured in units of the inverse characteristic frequency, $\omega_c = 2\pi V_c / 2eR$. Solutions to this equation depend the characteristic damping parameter,

(7) $$\beta_L = \frac{L}{R^2 (2e / 2\pi V_C)}$$

were L is an effective inductance per cell, and R is a phenomenological series resistance describing a complicated quasi-particle loss processes.

Equation (6) is valid when the number of junctions in the array is less than the soliton length, $N < (2e/2\pi V_c C_0)$, or when the solitons are closely spaced so that there is effectively a "traveling quasi-charge wave", as would be the case when the damping parameter is large enough. A straight forward derivation of (6) is to simply sum the voltages in a series circuit of a junction described by (4), a phenomenological inductance L, and a phenomenological resistance R. For the case of the single electron tunneling, this model has been called the "serial resistive junction" or SRJ model [7]. Equation (6) is the dual of the RSJ model [1,2] which is the basis of our understanding of the dc hysteretic current-voltage curves of ordinary Josephson junctions [3].

III. EXPERIMENTS

Several series arrays of $Al/Al_2O_3/Al$ junctions have been studied with the number of junctions in the range (1 - 255), with junction capacitance in the range 1fF - 3 fF, and resistance in the range 1k -10k .

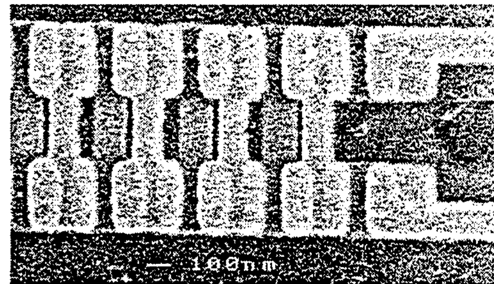

Fig. 1: An SEM micrograph of an array showing two connecting leads on the left side. The pitch between bottom and top electrode is 0.2μm.

The arrays were made using a mask defined with electron beam lithography, and an angle evaporation technique [8]. Nearest neighbor electrodes were actually two junctions in parallel. This SQUID geometry allowed for the tuning of the effective Josephson coupling energy with an external magnetic flux.

Typical current voltage characteristics of an array with E_J/E_C=4 is shown in fig. 2. A distinct zero

current state could be observed below a critical voltage. Above the critical voltage, a finite current state could be measured. That this current is due to Cooper pair tunneling can be proven, because the application of a magnetic field modulates the current (see fig. 2). The current above the critical voltage could be suppressed by the magnetic flux in a periodic way, going to zero when the flux in the SQUID loop was $\Phi_0/2$.

Except for the extreme limit $E_C >> E_J$ we can make a good approximation by replacing the saw function with a sine function. We then can copy the well known solutions to the RSJ model. When $\beta << 1$, analytical solutions of equation are possible [3]. Figure 1 shows a fit of the model with $\beta << 1$, to experimental IV curves for a 255 junction array, where the CBCPT was observed. The two different curves correspond to different values of the external magnetic field. The fit is a two parameter fit with R and V_c being adjusted for each value of the magnetic field. The critical voltage is indeed a function of E_J/E_C, which is tuned by magnetic field, and the phenomenological resistance R is also expected to be dependent on E_J/E_C if R arises from Zener tunneling. The model accurately reproduces the shape of the experimental curve for the higher magnetic field, but less so for the lower fields.

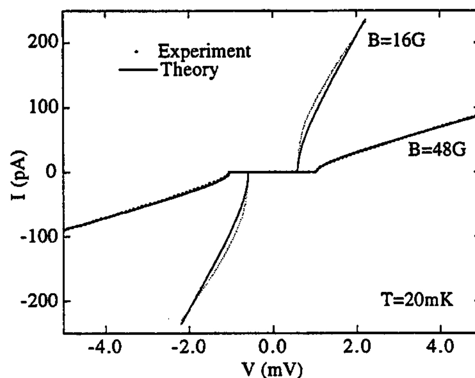

Fig. 2: Current Voltage characteristics for an array with 255 junctions in series, with E_J E_C, with a fit to the model.

When $\beta > 1$, numerical solutions must be found, and equ. (2) results in a hysteretic IV curve, where there is a region of voltage having two possible stable values of current. Fig. 3 shows an experimental IV curve of another 255 junction array, were hysteresis was observed. The shape of this curve is qualitatively very similar to that predicted by equ. (6) with $saw(\chi) = sin(\chi)$ [3].

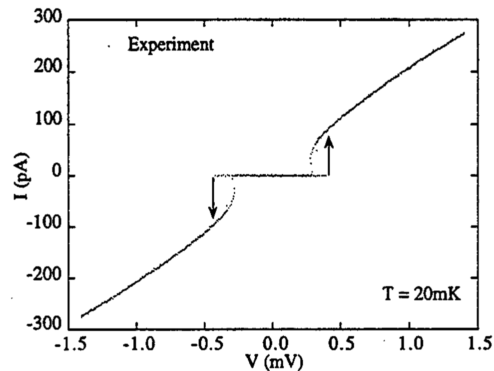

Fig. 3: For some arrays, hysteresis could be observed.

ACKNOWLEDGMENTS

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Charging Effects in Self-Assembled Dots

L. R. C. Fonseca, J. L. Jimenez, J. P. Leburton and Richard M. Martin

I. Introduction

A considerable effort has been devoted to the quest for small integrable optoelectronic devices. Self-assembled quantum dots seem to fit in that category of devices as demonstrated by its applications as lasers [1], spectral detectors [2], and optical memories [3]. In addition to that, quantum dots offer an excellent opportunity to study the physics of highly confined few electron systems [4].

In this paper we address the electron-electron interaction within a single dot using a realistic model with electron interactions treated within the spin density functional theory. The structure analyzed is a complete multilayer device containing one pyramidal InAs quantum dot embedded in a GaAs matrix (Fig. 1). The number of electrons in the dot is controlled by applying voltage to a metal gate on the top of the device. Strain in the pyramid, wetting layer (the thin InAs layer from where the quantum dots arise - see Fig.1), and surrounding GaAs matrix is calculated using a continuum model. The bulk electron effective mass and band diagram are considerably modified by the strain in the region of the dot, becoming position dependent. In order to determine accurately the bias voltage at which charging occurs, we have used the idea of transition state as defined by Slater [5] for shell filling in atoms. We have used the local spin density approximation (LSDA) to calculate the many-body interaction terms of the Hamiltonian. [6] We have been able to calculate the energies of possible spin configurations in the dot showing that the dot filling indeed follows Hund's rule. Comparison of the electron-electron energy obtained directly from our calculations and extracted from the experimental data by Fricke *et al.* [7] shows good agreement.

II. Model

Figure 1 shows the device used in our calculation and layers of different materials which make up the structure. The only doped materials are the GaAs substrate and cap, both doped with donors at a density of $10^{18}/\mathrm{cm}^3$. We have assumed a conduction band offset $\Delta E_c = 770$ meV between GaAs and InAs (ratio $\Delta E_c/\Delta E_g = 70\%$), and bulk electron effective masses in GaAs and InAs of 0.067 m_e and 0.023 m_e, respectively, where m_e is the bare electron mass. All the calculations were performed at 4.2 K.

The potential in the device is obtained by solving Poisson equation:

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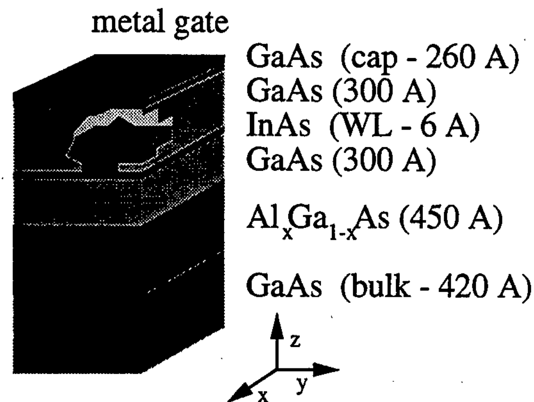

Fig. 1. Schematic representation of the self-assembled dot structure used in the present work.

$$\nabla^2\phi = -\frac{q}{\epsilon(\mathbf{r})}[p(\mathbf{r}) - n(\mathbf{r}) + N_D^+(\mathbf{r}) - N_A^-(\mathbf{r})], \quad (1)$$

where q is the electron charge and p, n, N_D^+, and N_A^- are the hole, electron, donor and acceptor densities. All the charge densities are calculated using the semi-classical Thomas-Fermi approximation for bulk charges in the region far from the dot, while in the region close to the dot (defined by a box containing the pyramid, the wetting layer, and some of the GaAs surrounding matrix) we have assumed no other charges but electrons with a concentration given by

$$n(\mathbf{r}) = \sum_{i=1}^{N} n_i |\psi_i(\mathbf{r}, s)|^2, \quad (2)$$

where ψ_i is ith solution of the stationary Schrödinger Eq. 3, n_i is the occupation number of level i, N is the number of electrons, and s denotes spin. The potential ϕ resulting from the solution of Eq. 1 is incorporated into Schrödinger equation, written in the envelope approximation as:

$$\left\{-\frac{\hbar^2}{2}\nabla\left[M^{-1}\nabla\right] + V(\mathbf{r})\right\}\psi_n(\mathbf{r}) = E_n\psi_n(\mathbf{r}). \quad (3)$$

In Eq. 3, M is the electron effective mass tensor (see below) and the potential energy V is given by

$$V(\mathbf{r}) = V_{ext}(\mathbf{r}) + V_H(\mathbf{r}) + V_c(\mathbf{r}) + V_{xc}(\mathbf{r}) + V_{off}(\mathbf{r}), \quad (4)$$

where $V_{ext}(\mathbf{r})$ is the potential due to externally applied voltage, $V_H(\mathbf{r}) = -q\phi(\mathbf{r})$ is the Hartree potential, $V_c(\mathbf{r})$

is the conduction band strain potential, $V_{xc}(\mathbf{r})$ is the exchange-correlation potential, and $V_{off}(\mathbf{r})$ is the conduction band offset.

The strain tensor has been obtained from the minimization of the elastic energy of the system. Since the dot is fully strained, the InAs band gap increases considerably, changing the electron effective mass in that material by roughly a factor of two. The piezoelectric potential has been neglected in this work as a result of its small effect on the eigenenergies of the dot [8].

Equations 1 and 3 are iterated until self-consistency is achieved. The Poisson equation is solved using the multigrid method [9], while the Schrödinger equation is solved using the iterative extraction-orthogonalization method (IEOM) [10].

The many-body interactions have been treated within the density functional theory [6], where the exchange-correlation potential $V_{xc}(\mathbf{r})$ is given by

$$V_{xc}(\mathbf{r}) = \frac{\delta E_{xc}}{\delta n(\mathbf{r})}. \qquad (5)$$

The exchange-correlation energy $E_{xc}[n]$ is given by

$$E_{xc}[n] = \int n(\mathbf{r})\epsilon_{xc}[n(\mathbf{r})]d\mathbf{r}, \qquad (6)$$

where $\epsilon_{xc}[n]$ is the exchange and correlation energy per particle of a uniform electron gas of density n. The functional $\epsilon_{xc}[n]$ can be separated into exchange and correlation contributions, where the exchange part is a well known expression [6], while accurate values of the correlation part $\epsilon_c[n]$ have been obtained from quantum Monte Carlo calculations [11] as parametrized by Perdew and Zunger [12].

A rigorous way of determining the number N of electrons in a quantum dot with the electron charge as a good quantum number is to minimize the total energy of the system $E_T(N)$, for $N = 1, 2, \ldots, N_{max}$. The use of just eigenvalues to determine the charge in the dot, where charging occurs whenever an eigenvalue crosses the Fermi level, is only correct in the limit of weakly interacting electron systems. The calculation of the total energy of the system involves terms of the order of meV's like the Hartree and exchange-correlation energies, and terms of the order of tens of eV's, like the electrostatic energy of the doping impurities and surface charges. The total energy of the system is of the order of tens of meV's, since the large terms mostly cancel out. Clearly such an accurate cancellation is difficult to obtain. The transition state concept offers an elegant solution to this problem [5]. Differentiating E_T with respect to the non-integer occupation number n_i of level i one obtains the so-called Janak theorem [13]

$$\frac{\partial E_T}{\partial n_i} = \epsilon_i. \qquad (7)$$

Integrating Eq. 7 between N and $N+1$ one finds the so-called Slater formula [5]:

$$E_T(N+1) - E_T(N) = \int_0^1 \epsilon_{LAO}(n)dn \approx \epsilon_{LAO}(\frac{1}{2}), \qquad (8)$$

where ϵ_{LAO} corresponds the eigenvalue of the lowest available orbital. The last step in Eq. 8 is exact if ϵ_{LAO} is a linear function of the occupation number. We have performed several numerical experiments which demonstrated a nearly linear relation, showing that the approximation used in Eq. 8 is very good.

In order to calculate the electron-electron interaction energy in the dot $E_{ee} = E_{xc} + E_H$, we have to determine the exchange-correlation E_{xc} and Hartree E_H energies, where E_{xc} was defined in Eq. 6 and E_H is given by

$$E_H = \frac{1}{2}\int \frac{n(\mathbf{r})n(\mathbf{r}')}{4\pi\bar{\epsilon}|\mathbf{r}-\mathbf{r}'|}d\mathbf{r}d\mathbf{r}', \qquad (9)$$

where $\bar{\epsilon}$ is the average dielectric constant, independent of position, which probably introduces only a small error to the value of E_H since the dielectric constants throughout the layers differ by less than 15%. Because direct solution of Eq. 9 is too time consuming, we have calculated the potential created only by the electrons in the dot V_e and then solved

$$E_H = \frac{1}{2}\frac{1}{4\pi\bar{\epsilon}}\int V_e(\mathbf{r})n(\mathbf{r})d\mathbf{r}. \qquad (10)$$

The potential V_e is obtained by solving Poisson equation with the density determined by the dot electrons and boundary condition calculated by multipole expansion (up to quadrupole) of the charge in the dot. This is a good approximation if the boundaries are far from the charge, which is the case in our device.

III. RESULTS

Figure 2 shows the first ten eigenvalues of empty dots as a function of dot base length (also called base diameter), keeping the wetting layer width fixed. The eigenvalues were calculated with respect to the average conduction band edge position in the dot. Figure 2 and inset also show the approximate depth of the well and the energy difference between the first (0 0 0) and second (1 0 0) states, and between the second and third (0 0 1) states. The notation $(n_i n_j n_k)$ corresponds to the number of nodes of the eigenfunction in the x, y, and z directions, respectively. The eigenvalues were only calculated while the states remained bound or quasi-bound. Notice in the inset that the energy separation between (0 0 0) and (1 0 0) is close to linear, while between (1 0 0) and (0 0 1) is almost a constant, reflecting the different confinement directions of the last two states. As the eigenvalues approach the top of the well, the slopes of the curves tend to decrease, as a result of deeper wave function penetration in the barrier region. For energies above the well height, the corresponding eigenfunctions spread over the wetting layer, becoming a 2-dimensional electron gas.

Figure 3 shows the charging of three quantum dots of different sizes as a function of bias in the metal gate on the top of the device (see Fig. 1). In all three staircases LSDA was used to treat the electron-electron interactions. The dots were charged up the maximum number of electrons they can fit. As expected, the step size becomes longer

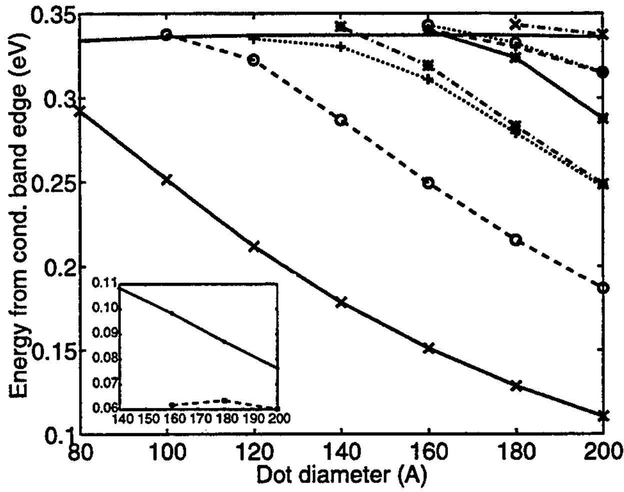

Fig. 2. Approximate well depth (thick solid line) and eigenvalues of the hamiltonian as a function of dot diameter d. The eigenvalues were calculated with respect to the average conduction band edge in the region of the pyramid. States represented, from low to high energy: (0 0 0), (1 0 0)/(0 1 0), (0 0 1), (1 1 0), (2 0 0)-(0 2 0), (2 0 0)+(0 2 0), (1 0 1)/(0 1 1), and (1 1 1). The notation $(n_1 n_2 n_3)$ denotes the number of wave function nodes in the x, y, and z directions. Degenerate states are separated by a slash. Inset: energy separation between states (0 0 0) and (1 0 0)/(0 1 0) (solid), and between states (1 0 0)/(0 1 0) and (0 0 1) (dashed). Pyramid height $h = d/2$. Lines are only guides for the eye.

as the dot size decreases as a result of the more widely spaced single-particle levels (steps corresponding to N = 2, 6, and 9, where N is the number of electrons in the dot) and the stronger electron-electron repulsion. However, the steps involving charging of degenerate levels (N = 3, 4, and 5) become more homogeneous for smaller dots. That results from the different dependencies of the Hartree and exchange-correlation energies on the charge density, thus in the dot volume. While the first increases as n^2, the second increases only as $n^{4/3}$. Thus the Hartree term, which only depends on the charge in the dot and not on the spin configuration, dominates for smaller dot sizes. The uneven steps observed for N = 3, 4, and 5 in the 200Å base diameter pyramid can be understood as follows. We have occupied the second (1 0 0)/(0 1 0) degenerate levels following Hund's rule, *i.e.* according to the spin sequence $2p_x^\uparrow 2p_y^\uparrow 2p_x^\downarrow 2p_y^\downarrow$, where the arrows pointing up and down correspond to spin orientation and the notation $2p_i$ means second level of type p oriented along direction i. In the next section we will show that this system indeed follows Hund's rule. The step corresponding to N = 3 is short because the third and fourth electrons occupy different orbitals (1 0 0) and (0 1 0). Even though the two electrons have the same spin, those orbitals have a node near the center of the pyramid, resulting in small wave function overlap. The step corresponding to N = 4 is long because the fifth electron is forced to share an orbital already half-occupied. There is strong wave function overlap and no exchange energy, since the fifth electron spin is different from the third and fourth electron spins. Finally, the step corresponding to N = 5 is short because, even though the sixth electron is repelled by all other three electrons, exchange between the sixth and the fifth electrons decreases the repulsion energy.

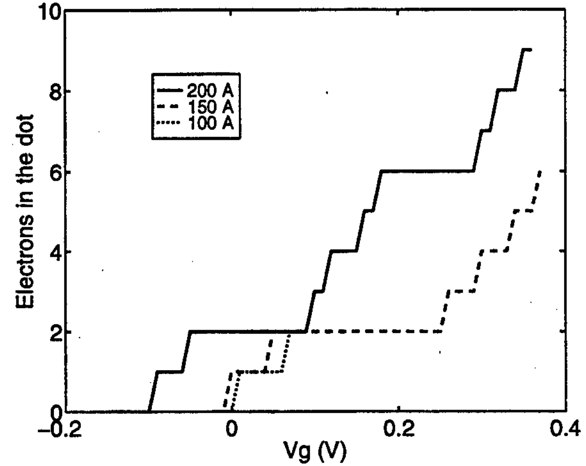

Fig. 3. Number of electrons in the dot as a function of applied voltage V_g for different pyramid diameters d. Pyramid height $h = d/2$.

In order to compare our results with those of Fricke *et al.* we have calculated the electronic structure of a 200Å base diameter and 70Å height pyramidal quantum dot. Figure 4 shows the number of electrons in such a pyramid as a function of gate voltage V_g. Two curves are shown, corresponding a charging sequence which follows or not Hund's rule. As already pointed, Hund's rule means that the charging of the four-fold degenerate second level follows the spin sequence $2p_x^\uparrow 2p_y^\uparrow 2p_x^\downarrow 2p_y^\downarrow$. The curve that does not follow Hund's rule was obtained by charging the second level according to the spin sequence $2p_x^\uparrow 2p_y^\downarrow 2p_x^\uparrow 2p_y^\downarrow$. The third possibility, namely the spin sequence $2p_x^\uparrow 2p_x^\downarrow 2p_y^\uparrow 2p_y^\downarrow$, was not considered because it will clearly be unfavorable due to the intense coulomb repulsion between the $2p_x^\uparrow$ and the $2p_x^\downarrow$ electrons resulting from their large wave function overlap. The step size obtained with LSDA corresponding to the charging of the fourth electron (N = 3) is longer for the charging the dot according to the spin sequence $1s^\uparrow 1s^\downarrow 2p_x^\uparrow 2p_y^\downarrow$ than for $1s^\uparrow 1s^\downarrow 2p_x^\uparrow 2p_y^\uparrow$, indicating that indeed Hund's rule is followed by this system. The electron-electron interaction energy difference between the two spin configurations for four electrons in the dot is ~ 3 meV.

The addition of the fourth electron following Hund's rule is less costly because of the presence of exchange interaction (attractive) in this case but not if the spin of the fourth electron is different from the spin of the third. Analogously, the step corresponding to the charging of the fifth electron (N = 4) is shorter for the sequence $2p_x^\uparrow 2p_y^\downarrow 2p_x^\uparrow 2p_y^\downarrow$ because the fifth electron, either in the $2p_x^\uparrow$ or $2p_y^\downarrow$ state, interacts by exchange with one of the two electrons already in the second level, while according to Hund's rule, the fifth electron does not interact by exchange with any of the other two because of their different spin states.

We now estimate pairwise electron-electron interaction energies. The so-called $s-s$ interaction between two s-electrons can be calculated directly from $E_{xc}(2)$ and $E_H(2)$ since for two electrons in the dot this is the only possible

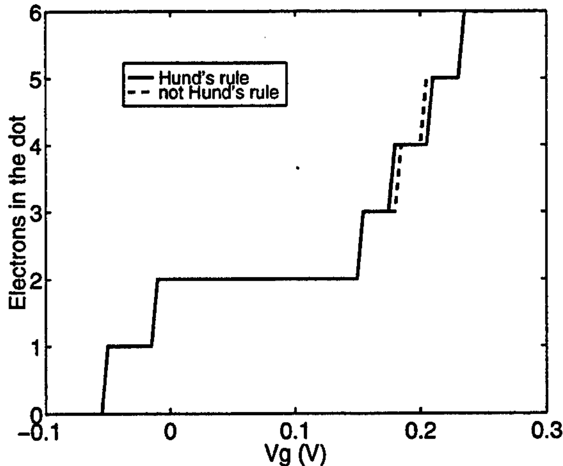

Fig. 4. Number of electrons in the dot as a function of gate voltage V_g using LSDA according to Hund's rule (second level population following the spin sequence $2p_x^\uparrow 2p_y^\uparrow 2p_x^\downarrow 2p_y^\downarrow$) and LSDA not following Hund's rule (second level spin sequence $2p_x^\uparrow 2p_y^\downarrow 2p_x^\uparrow 2p_y^\downarrow$). Pyramid diameter = 200Å and height = 70Å.

type of interaction. We have obtained $E_{ee}^{s-s} \sim 13$ meV, which is only the Hartree interaction since there is no exchange between the s electrons. Since experiments can only detect average electron-electron interactions, we will only calculate approximate values for the $p-s$ and $p-p$ interactions. The charging energy of the third electron contains one $s-s$ interaction and two $p-s$ interactions. Assuming that the $s-s$ interaction does not change much when the third electron is added, we have derived the average energy for the $p-s$ interaction to be $E_{ee}^{p-s} \sim 9$ meV. This result is an average because the p electron interacts by exchange with only one of the s electrons (the one with the same spin). Repeating the same argument for the next electrons, we obtained an average $p-p$ interaction of $E_{ee}^{p-p} \sim 9$ meV. Table III summarizes and compares those results with the values inferred from the capacitance data by Fricke *et al.*. Differences between energies obtained from calculation and inferred from measurement may result from our assumption that the different types of interaction ($s-s$, $p-s$, or $p-p$) remain unchanged as more electrons are added to the dot. A second source of error in our calculation is the exclusion of interdot repulsion, which should push the electrons closer together inside the dot. However, as we have already pointed, for dot densities of $10^{10}/\text{cm}^2$, the inclusion of interdot effects should change our results by less than 1 meV by pushing the electrons in the dot closer together. Finally, the approximation used to calculate E_H may lead to some correction in our calculation. As far as the analysis of the experimental data is concerned [7], it considered the image charge effect but excluded interdot repulsion. In fact these two competing effects nearly cancel each other for dot densities in range of $1-10 \times 10^{10}/\text{cm}^2$. The analysis of the experimental data also excluded the presence of a charged interface between the gates (the layer of dots charged with one electron each). Indeed, the presence of the layer of charged dots between the gates *decreases*

interaction type	calculated	measured [7]
s-s	13	~ 23
s-p	~ 9	~ 7
p-p	~ 9	~ 18

TABLE I

CHARGING ENERGY PER ELECTRON PAIR (IN MEV).

the electron-electron interaction energy by $\sim \gamma_{dot} \times 3$meV, where $\rho_{dot} = \gamma_{dot} \times 10^{10}/\text{cm}^2$ is the density of dots in the plane. Because this correction is considerably large and linear on γ_{dot}, it is clear that the extraction of the electron-electron energy from the experimental data requires precise knowledge of the dot density.

IV. SUMMARY

We have calculated the electronic structure of self-assembled InAs-GaAs quantum dots as a function of dot size and externally applied voltage. In order to account for the spin-polarization of the system depending on the number of electrons in the dot, we have used LSDA to calculate the electron-electron exchange-correlation energy. We have also used the concept of transition state [5] to determine the number of electrons in the dot which minimizes the total energy of the system. We have verified that Hund's rule applies to InAs QDs due to the small charging energy difference of ~ 3 meV between the spin configurations $1s^\uparrow 1s^\downarrow 2p_x^\uparrow 2p_y^\downarrow$ and $1s^\uparrow 1s^\downarrow 2p_x^\uparrow 2p_y^\uparrow$. We have estimated the charging energy per electron pair, in good agreement with experiment.

V. ACKNOWLEDGEMENTS

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To the theory of temperature dependence of threshold current density of a quantum dot laser

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One of the most important expected advantages of quantum dot (QD) lasers over the conventional quantum well (QW) lasers is the weak temperature sensitivity of the threshold current [1]. Ideally, threshold current of QD laser should remain unchanged with the temperature [1]. This would be so indeed if the overall injection current went entirely into the radiative recombination in QDs. In fact, because of the presence of free carriers in the in the optical confinement layer (OCL), a fraction of the injection current is wasted therein. This fraction goes into the recombination processes in the OCL [2]–[10]. Hence, recombination in the OCL gives rise to one more component of the threshold current [2]–[10]. Besides, the latter component, associated with the thermal excitation (leakage) of carriers from QDs to the OCL, depends strongly on the temperature. As a result the total threshold current should become temperature dependent [3]–[6], especially at high temperatures. This has been observed experimentally in [11].

In [4]–[10], a detailed theoretical analysis of the gain and threshold current density $j_{\rm th}$ of QD laser has been given having regard to inhomogeneous line broadening caused by fluctuations in QD parameters. Both of the radiative recombinations in QDs and in the OCL have been taken properly into account. The different cases of QD filling have been revealed to occur depending on temperature, QD size fluctuations and conduction and valence band offsets at the QD–OCL heteroboundary. In view of the strong dependence of $j_{\rm th}$ on the parameters of the structure, optimization of the laser structure has been carried out. The key dimensionless parameter controlling the magnitudes of the minimum threshold current density and of the optimum parameters of the structure has been revealed. This parameter is the ratio of the stimulated transition rate in QDs at the lasing threshold to the spontaneous transition rate in the OCL at the transparency threshold.

In this work, we give a detailed analysis (by reference to [4]–[10]) of the temperature dependence of $j_{\rm th}$. Temperature dependences of both of the components of $j_{\rm th}$ associated with the radiative recombination in QDs and in the OCL are calculated. The relative contribution of each component to $j_{\rm th}$ is analyzed as a function of T. Temperature dependences of the optimum surface density of QDs and the optimum thickness of the OCL are obtained.

The threshold current density of QD laser is the sum of the current densities associated with the radiative recombination in QDs and in the OCL [4]–[7], [9]

$$j_{\rm th} = j_{\rm QD} + j_{\rm OCL}. \qquad (1)$$

We consider relatively high temperatures when equilibrium filling of QDs is the case [4]–[6]. Under the conditions of the thermal equilibrium between the carriers confined in QDs and free carriers, $j_{\rm QD}$ and $j_{\rm OCL}$ are [4]–[7], [9]

$$j_{\rm QD} = \frac{eN_{\rm S}}{\tau_{\rm QD}} f_{\rm n} f_{\rm p} \qquad j_{\rm OCL} = ebBnp = ebBn_1p_1\frac{f_{\rm n}f_{\rm p}}{(1-f_{\rm n})(1-f_{\rm p})} \qquad (2)$$

where $f_{n,p}$ are the mean electron and hole level occupancies in QDs required for attaining the peak modal gain value of $g = N_S a^2 \Gamma g_0$ *at a given surface density of QDs*, N_S (g_0 is the material gain reduced to one QD [4]–[6]); a is the mean size of QDs, Γ is the optical confinement factor in a QD layer (along the transverse direction in the waveguide), τ_{QD} is the radiative lifetime in QDs [4]–[6], b is the OCL thickness and B is the radiative constant for the OCL material.

The free-electron and -hole densities in the OCL, n and p, are

$$n = n_1 \frac{f_n}{1-f_n} \qquad p = p_1 \frac{f_p}{1-f_p} \tag{3}$$

$$n_1 = N_c^{OCL} \exp\left(-\frac{\Delta E_{c1} - \varepsilon_n}{T}\right) \qquad p_1 = N_v^{OCL} \exp\left(-\frac{\Delta E_{v1} - \varepsilon_p}{T}\right) \tag{4}$$

where $N_{c,v}^{OCL} = 2(m_{c,v}^{OCL} T / 2\pi\hbar^2)^{3/2}$ are the conduction and valence band effective densities of states for the OCL, ΔE_{c1} and ΔE_{v1} are the conduction and valence band offsets at the QD–OCL heteroboundary, $\varepsilon_{n,p}$ are the quantized energy levels of an electron and hole in a mean-sized QD (measured from the corresponding band edges) and the temperature T being measured in terms of energy.

At the lasing threshold ($g = \beta$, where β is the total loss coefficient), [7]–[10]

$$f_n = \frac{1}{2}\left(1 + \frac{N_S^{min}}{N_S}\right) - \frac{1}{2}\Delta\left(\frac{N_S^{min}}{N_S}, T\right) \tag{5}$$

$$f_p = \frac{1}{2}\left(1 + \frac{N_S^{min}}{N_S}\right) + \frac{1}{2}\Delta\left(\frac{N_S^{min}}{N_S}, T\right) \tag{6}$$

where $N_S^{min}((\Delta\varepsilon)_{inhom}, \beta)$ is the minimum surface density of QDs required to attain lasing at given losses β and inhomogeneous line broadening $(\Delta\varepsilon)_{inhom}$ [4]–[7].

Here, Δ is the difference of the hole and electron level occupancies in QDs at the lasing threshold. The self-consistent consideration of the problem for the electrostatic field distribution across the junction reveals the temperature dependence of Δ and hence of f_n and f_p (which are the analogue of the threshold carrier densities for QW or bulk lasers).

Thus, the self-consistent consideration of the QD charge reveals the temperature dependence of j_{QD} by itself. It also leads to the extra temperature dependence of j_{OCL} through the such dependences of $f_{n,p}$ (in addition to the temperature dependence of j_{OCL} through the temperature dependence of Bn_1p_1).

It should be noted that the temperature dependences of $f_{n,p}$ are much weaker compared to that of the product Bn_1p_1 (which is the exponential, see (4)). Consequently, the temperature dependence of j_{QD} is much weaker compared to that of j_{OCL}. Nevertheless, the conclusion that j_{QD} does depend on the temperature may be of great importance. The matter is that, in the properly designed QD laser structures, the recombination channel through the OCL states (i.e., the leakage current) should be suppressed. This should be at least one way to optimize the performance of QD lasers. Even so, the threshold current density, being determined solely by the radiative recombination in QDs, should be temperature dependent.

The radiative recombination current density in the OCL, j_{OCL}, increases exponentially with T, being characterized by a high activation energy $\Delta E_{g1} - \varepsilon_n - \varepsilon_p$ (see (4)). Thus, to describe the T-dependence of $j_{th} = j_{QD} + j_{OCL}$, we can conveniently introduce the temperature T_d at which j_{OCL} reaches j_{QD}: $j_{OCL}(T_d) = j_{QD}(T_d)$.

For T fairly less than T_d, $j_{OCL} \ll j_{QD}$ and j_{th} depends only weakly on the temperature. Conversely, for T fairly greater than T_d, $j_{OCL} \gg j_{QD}$ and j_{th} depends strongly on T. With (2), the following equation may be written for T_d:

$$T_d = \frac{\Delta E_{g1} - \varepsilon_n - \varepsilon_p}{\ln \left[\dfrac{b\, N_{cv}^{OCL}(T_d)}{N_S\,(1 - f_n(T_d))\,(1 - f_p(T_d))} r \right]} \tag{7}$$

where $N_{cv}^{OCL}(T) = 2(m_{chh}^{OCL} T/2\pi\hbar^2)^{3/2} + 2(m_{clh}^{OCL} T/2\pi\hbar^2)^{3/2}$ is the effective reduced density of states of the conduction and valence bands for the OCL material, $m_{chh}^{OCL} = m_c^{OCL} m_{hh}^{OCL}/(m_c^{OCL} + m_{hh}^{OCL})$, $m_{clh}^{OCL} = m_c^{OCL} m_{lh}^{OCL}/(m_c^{OCL} + m_{lh}^{OCL})$, m_c^{OCL} is the electron effective mass and m_{hh}^{OCL} and m_{lh}^{OCL} are the heavy- and light-hole effective masses for the OCL material. The factor $r = \frac{1}{2}(E_g^{OCL}/E_0)(P_{OCL}/P_{QD})^2$, where E_g^{OCL} and P_{OCL} are the bandgap and Kane's parameter of the OCL material, is of the order of unity; for the specific structure considered below, $r \approx 0.564$.

There is certain analogy between T_d so defined and the temperature of depletion (ionization) of impurity centers. The numerator of (7) presents the energy of excitation of the electron-hole pair from a QD (an analogue of the impurity ionization energy), N_S/b is the QD number per unit volume of the OCL (an analogue of the impurity concentration).

With (2) and (7), the ratio of j_{OCL} to j_{QD} may be presented as

$$\frac{j_{OCL}(T)}{j_{QD}(T)} = \frac{j_{QD}(T_d) - \dfrac{eN_S^{min}}{\tau_{QD}}}{j_{QD}(T) - \dfrac{eN_S^{min}}{\tau_{QD}}} \left(\frac{T}{T_d}\right)^{3/2} \exp\left(\frac{\Delta E_{g1} - \varepsilon_n - \varepsilon_p}{T_d} - \frac{\Delta E_{g1} - \varepsilon_n - \varepsilon_p}{T}\right). \tag{8}$$

For $T < T_d$, $j_{OCL} < j_{QD}$; conversely, for $T > T_d$, $j_{OCL} > j_{QD}$.

To illustrate the results of analysis, we use a laser structure considered in [4,7]. Gaussian distribution of relative QD size fluctuations is supposed. The mean size of cubic QDs is taken to be $a = 150$ Å. The total loss coefficient, RMS of relative QD size fluctuations and OCL thickness are taken to be $\beta = 10\,\text{cm}^{-1}$, $\delta = 0.05$ and $b = 0.28\,\mu$m (which is the optimum value at $T = 300$ K), respectively. The corresponding value of N_S^{min} is $2.1 \times 10^{10}\,\text{cm}^{-2}$. The surface density of QDs is equal to its optimum value at $T = 300$ K ($N_S^{opt}/N_S^{min} \approx 3.70$, [7]).

Fig. 1 shows the temperature dependence of $\Delta = f_p - f_n$ and $f_{n,p}$ at the lasing threshold. The dashed line shows $f_{n,p}$ calculated disregarding the charge neutrality violation in QDs. Δ drops slowly with the temperature; f_n and f_p tend slowly to each other. Thus, violation of the charge neutrality in QDs is suppressed with T.

The free-carrier densities in the OCL are plotted in Fig. 2 versus T.

Fig. 3 shows j_{QD}, j_{OCL} and j_{th} against T. At $T = 300$ K, $j_{QD} = 6.2\,\text{A/cm}^2$ and $j_{OCL} = 2.0\,\text{A/cm}^2$; j_{QD} and j_{OCL} become equal to each other (and equal to $6.4\,\text{A/cm}^2$) at $T = 344$ K. At $T = 400$ K, $j_{QD} = 6.6\,\text{A/cm}^2$ and $j_{OCL} = 20.0\,\text{A/cm}^2$.

Shown in Fig. 4 are the ratios j_{QD}/j_{th} and j_{OCL}/j_{th} against T. At room temperature, the contribution of j_{OCL} to j_{th} still remains moderately small in comparison with that of j_{QD}. The former contribution increases with T. The contributions become equal to each other at $T = 344$ K (see also Fig. 3).

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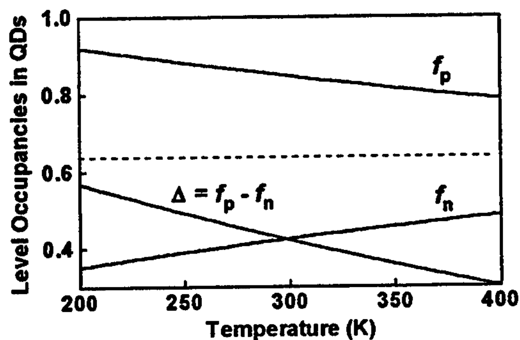

Figure 1. Electron and hole level occupancies in QDs at the lasing threshold and the difference of them *vs.* temperature.

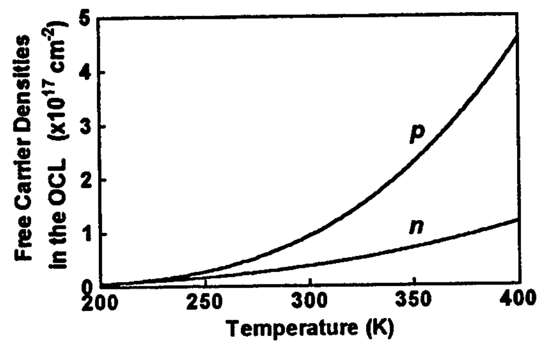

Figure 2. Free-electron and -hole densities in the OCL at the lasing threshold *vs.* temperature.

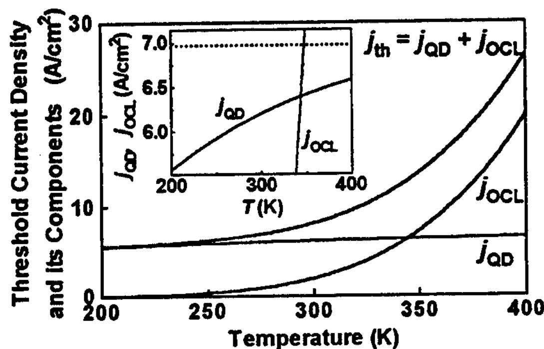

Figure 3. Threshold current density and current densities associated with the radiative recombination in QDs and in the OCL *vs.* temperature.

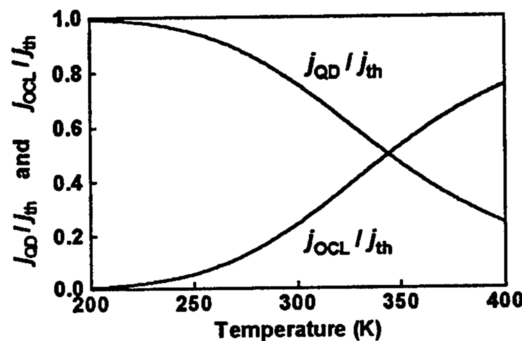

Figure 4. Temperature dependences of the relative contributions of the components to the threshold current density.

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Effects of Quantum Mechanical Coupling on the Filling of Electrons in Quantum Dot Molecules

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1.0 Introduction

Semiconductor quantum dots are often referred to as artificial atoms since their electronic properties for example the ionization energy and discrete excitation spectrum resemble those of real atoms. We have recently observed the atomic-like properties of artificial semiconductor atoms by measuring Coulomb oscillations in a clean disk-shaped vertical quantum dot containing a tunable number of electrons starting from zero[1]. The dot is strongly confined by heterojunction barriers in the vertical direction and parabolically confined by a Schottky gate induced potential in the lateral direction. Associated with the parabolicity as well as the rotational symmetry in the lateral confinement, a "shell structure" marked by "magic numbers" in the addition energy spectrum, a pairing of Coulomb oscillation peaks due to spin degeneracy, and modification of the pairing in line with Hund's rule are all observed. In this work we stack the disk-shaped dots vertically via a thin heterojunction barrier to fabricate a quantum dot (diatomic) molecule and study the filling of electrons in artificial semiconductor molecules. We use the artificial molecules with different central barrier thicknesses to study the effects of quantum mechanical coupling between dots.

2.0 Fabrication of Quantum Dot Molecules

A quantum dot molecule can be realized in the vertical geometry by placing a single gate around a submicron cylindrical mesa incorporating a $GaAs/Al_{0.2}Ga_{0.8}As/In_{0.05}Ga_{0.95}As$ triple barrier structure (TBS) specially designed to accumulate electrons in the linear transport regime. The InGaAs wells are 12 nm wide and the outer AlGaAs barriers are 7 nm wide. Details of fabrication are described elsewhere [2]. By changing the thickness, b, of the central AlGaAs barrier from 5.5 to 2.5 nm, we are able to increase the energy splitting between symmetric and antisymmetric states from about 0.4 to 3.2 meV. The drain current flowing through the two-dot system at a temperature of 0.1 K is measured as a function of drain voltage and gate voltage. By measuring the properties of the conductance oscillations as a function of electron number we are able to identify attributes of quantum dot molecules.

3.0 Filling of Electrons in Symmetric and Antisymmetric States

Quantum mechanical coupling between dots gives rise to two series of single-particle lateral states: symmetric and antisymmetric states. Filling of electrons in these states is determined by the energy splitting between the symmetric and antisymmetric states as well as the energies of lateral confinement and Coulomb interactions [3]. As a rough guide, a typical "bare" lateral confinement energy is 3 to 4 meV when the number

of electrons in the molecule is small and a typical average "classical" charging energy is 3 meV.

When the dots are quantum mechanically strongly coupled, the electrons in the system are delocalized (electrons are only filled in the symmetric states), and the addition energy spectrum of the artificial molecule resembles that of an artificial atom. This behavior is observed for a coupled dot with the thinnest central barrier of b=2.5 nm. The addition energy as a function of electron number, N, shows a large maxim at N=2 and 6 marking the complete filling of the first and second shells, respectively and only a small maxim at N=4 and 9, marking the half filling of the second and third shells, respectively (Hund's rule). The "magic numbers" of N=2 and 6 arise from the filling of electrons in the symmetric states. We see no evidence of filling of electrons in the antisymmetric states for N<10, despite the symmetric-antisymmetric splitting is comparable to the lateral confinement energy. This is probably because Coulomb interactions favor the filling of p-type electrons in the symmetric lateral states rather than that of s-type electrons in the antisymmetric lateral states. Hund's rule is significantly obscured due to the reduced Coulomb interactions in the increased system size.

When the energy of quantum coupling is significantly smaller than that of lateral confinement, the filling of electrons in the antisymmetric states is accessible. This is observed for a coupled dot with b>4 nm. A shell structure is modified, reflecting the filling of electrons in the symmetric and antisymmetric states. We identify attributes of the filling from measurements of Coulomb oscillations as a function of magnetic field. Hund's rule associated with the symmetric lateral states is more evident in the artificial molecule with a weaker quantum coupling.

4.0 Summary

We have shown that gated sub-micron vertical triple barrier structures have considerable promise for studying molecular-like properties of couple quantum dots, i.e. artificial semiconductor molecules. As a function of central barrier thickness, we can alter the degree of quantum mechanical coupling and Coulomb interactions in the two-dot system. For a strongly coupled dot, the lower energy states are symmetric and delocalized, and the attributes of the molecule resemble those of a single dot. When the coupling is significantly weaker than the lateral confinement and Coulomb interactions, a shell structure is modified, reflecting the filling of electrons in the antisymmetric states.

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Consequences of Confinement Effects in the Charging and Discharging of Nano-Crystal and Quantum-Dot Memories

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Abstract

For nanometer-sized floating gates, confinement and single-electron effects lead to slowing of the charging and discharging processes, and the reduction in electron statistics leads to larger relative fluctuations. We describe the quantum kinetic modeling of the injection process from a one-dimensionally confined electron gas to the three-dimensionally confined quantum dot, and of the ejection process from the quantum dot to the unconfined substrate. For silicon/silicon-dioxide based nanostructures, such as the nano-crystal and the quantum-dot memory, injection and ejection occur over 10's of nano-seconds to 10's of micro-seconds at useful bias voltages. Theoretical results largely substantiate the experimental results, and we discuss their consequences.

Introduction

Nano-crystal[1,2] (Figure 1) and quantum-dot[3,4] memories (Figure 2) are flash memory structures where the storage floating gate has been scaled to dimensions that make quantum-confinement and single electron effects significant. One consequence of this is in power through lowering of the amount of charge needed for operation and thus lowering of currents. This is largely a desirable attribute; the lowering of power with reduction in dimensions is a requirement of continuing improvements in integration. The undesirable consequence of this is in random fluctuations - through the storage of the charge as well as through the side-effects of charged defects. The second consequence of the reduced dimensions is in time-scales of operation through lowering of capture and emission rates, a process that slows the devices. We analyze these and compare the results with experimental observations.

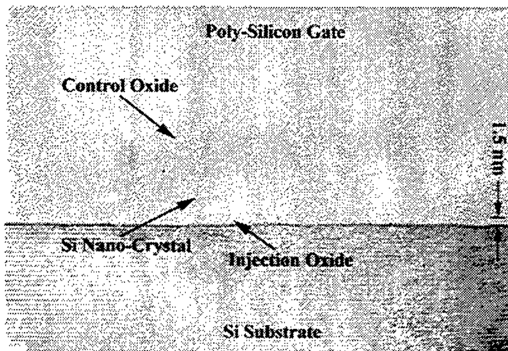

Fig. 1: A cross-section of a distributed floating gate consisting of silicon nano-crystals separated from the silicon channel and the poly-crystalline silicon gate by silicon dioxide. Three nano-crystal bubbles are shown in this cross-section.

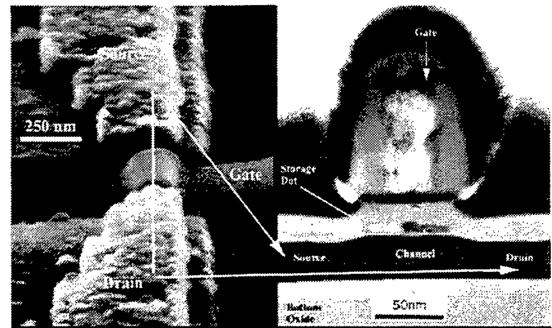

Fig. 2: A cross-section of a quantum-dot memory consisting of a small storage dot placed between a 30 nm length and 100 nm height poly-crystalline silicon gate and a silicon-on-insulator channel.

Quantum Kinetic Equation

We are interested in analyzing the electrical nature of the problem of a quantum-dot coupled to a channel and modulated by a gate. A simple electric interpretation of this is a quantum-dot coupled to the gate and the channel modeled by two capacitances (C_1 and C_2 to gate and channel respectively). The electrostatic energy change (ΔE_s) upon the addition of one electron to the N electrons already present is given by

$$\Delta E_s = \frac{Ne^2}{C} + \frac{e^2}{2C}. \tag{1}$$

Here, $C = C_1C_2/(C_1 + C_2)$. The Hamiltonian for the system is

$$H = H_{2deg} + H_{qd} + H_T, \tag{2}$$

where

$$\begin{aligned} H_{2deg} &= \sum_n (\epsilon_n + eV) a_n^\dagger a_n \\ H_{qd} &= E_s(N) + \sum_m \epsilon_m b_m^\dagger b_m \\ \text{and } H_T &= \sum_{n,m} T_{nm} a_n^\dagger b_m + c.c., \end{aligned} \quad (3)$$

with V as the potential difference between the dot and the two-dimensional electron gas in the absence of electrons in the dot, and n and m as the indices of the ladders in the two-dimensional electron gas and the dot respectively. The equation of motion of the density matrix $\hat{P}$ is

$$i\hbar \frac{\partial \hat{P}_H(t)}{\partial t} = \left[H, \hat{P}_H(t)\right]. \quad (4)$$

With the notation $H_0 = H_{2deg} + H_{qd}$, the interaction density matrix ($\hat{P}_I(t)$) is:

$$\hat{P}_I(t) = \exp\left[\frac{i}{\hbar}\int_{t_0}^{t} H_0 dt'\right] \hat{P}_H(t) \exp\left[-\frac{i}{\hbar}\int_{t_0}^{t} H_0 dt'\right] \quad (5)$$

and the equation of motion is

$$i\hbar \frac{\partial \hat{P}_I(t)}{\partial t} = \left[H_T(t), \hat{P}_I(t)\right] \quad (6)$$

with

$$H_T(t) = \exp\left[\frac{i}{\hbar}\int_{t_0}^{t} H_0 dt'\right] H_T \exp\left[-\frac{i}{\hbar}\int_{t_0}^{t} H_0 dt'\right] \quad (7)$$

and the solution

$$\hat{P}_I(t) = \hat{P}_I(t_0) - \frac{i}{\hbar}\int_{t_0}^{t} [H_T(t'), \hat{P}_I(t')] dt'. \quad (8)$$

The state of the system $|n_n, n_m>$ is characterized by the probability $p_{n_m}(t)$ for occupation number n_m at time t in the quantum dot, and is given by

$$p_{n_m}(t) = \sum_{n_n} < n_n, n_m | \hat{P}_I(t) | n_n, n_m > . \quad (9)$$

The probability $p_N(t)$ for N electrons in the dot can be found from this as a sum of all configurations for which $\sum_m n_m = N$. This lets us now write the transition equation covering the possibilities of losing or gaining an electron with transition rates expressed by summation over the distribution in the two-dimensional electron gas and coupling constants T_{nm}. The essence of this is that we now have a contained form

$$\frac{\partial \vec{P}(t)}{\partial t} = W.\vec{P}(t) \quad (10)$$

describing the probability vector $\vec{P}(t) = [p_0(t), p_1(t), \cdots]$, and it can be determined using the transition matrix W. Variance, mean, and time evolution follow from this.

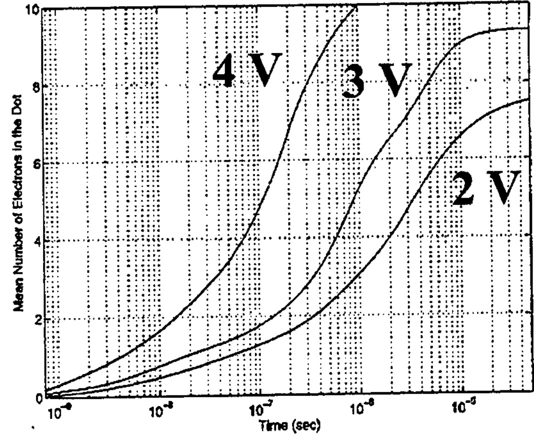

Fig. 3: The evolution of the mean number of electrons in a silicon quantum-dot (10 nm x 10 nm x 6 nm) from an inversion layer due to direct tunneling through an injection oxide of 1.5 nm at three different gate-to-inversion layer potentials.

Capture, Emission and Fluctuations

Figure 3 shows an evolution of electrons in a dot due to injection from inversion layer under three different bias conditions. At the 2 V bias condition, it takes nearly 100 ns before the average reaches one electron. The transition rates are too low because of the large oxide barrier height and small overlap. But, it changes rapidly with bias so that less than 10 ns is needed at 4 V bias. The saturation in number of electrons between 100's of ns to 10's of μs for the differing bias voltages represents the effect of reduced dimensions. As the charging process nears flat-band conditions, the injection process begins to slow down for the same reasons that slow the process at low bias voltages. Now consider the same structure during erasure (Figure 4) when a negative potential is applied at the gate to eject the electrons into the substrate. A number of starting electrons are considered for two differing voltages. The behavior does not have the detailed features of the injection process; the injection process reveals more of the details of the states being tunneled into. The time-constants of ejection are however quite similar to that of injection. At 2 V, not shown, the process has very appreciably slowed down. The lifetime in the dot has become very large.

These are calculated results for quantum-dot memories, i.e. involving only single dots. Experimentally, currently we can only compare this to results on nano-crystal memories which involve parallel injection into and out of many quantum-dots and where, during injection and erasure, consequences of changing threshold voltage with time and along the channel can be significant. But, rough comparisons can still be made for order of magnitude comparisons. Table 1 shows, for differing oxide thickness, the injection time constants for devices with approximately comparable nano-crystal density. The nano-crystal density and the observed threshold voltage shift corresponds to an average of 2 electrons per nano-crystal quantum dot. The simulated time for injection of 2 electrons with 1.5 nm

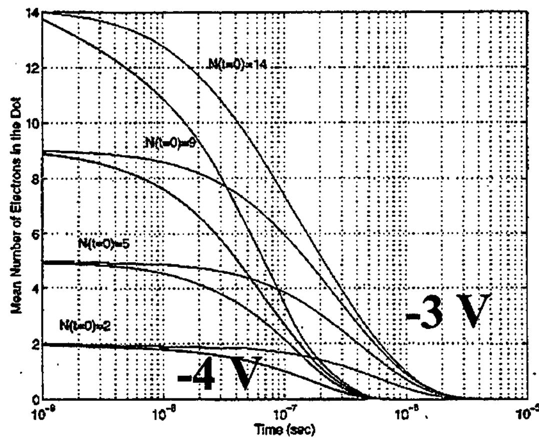

Fig. 4: The evolution of the mean number of electrons in a silicon quantum-dot (10 nm x 10 nm x 6 nm) due to ejection into the substrate upon the application of a repelling bias at the gate. The geometry is identical to the previous figure.

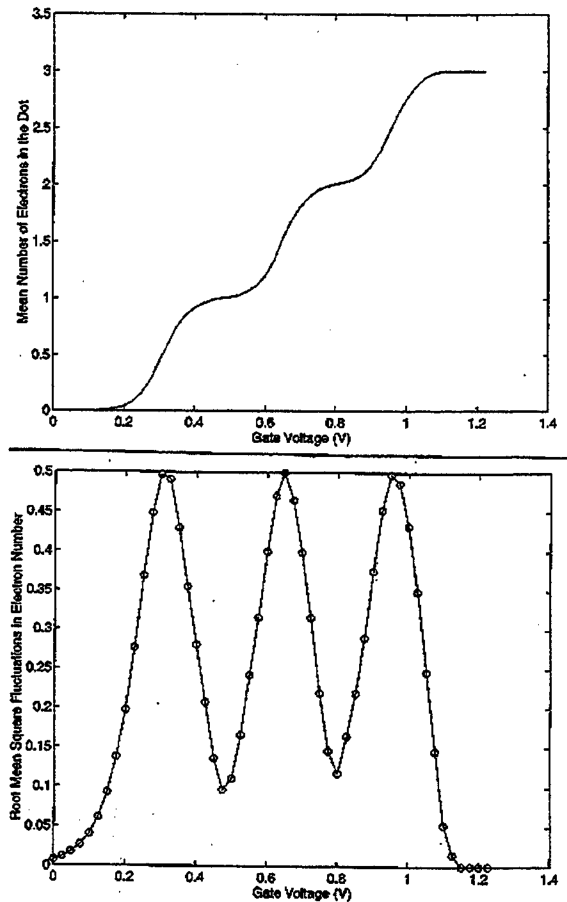

Fig. 5: The evolution of mean number of electrons in a silicon quantum-dot (10 nm x 10 nm x 6 nm) as a function of applied gate voltage and the corresponding variance. This calculation assumed an upper limit of electrons allowed as 3.

Oxide Thickness	Write Condition	ΔV_T
1.6 nm	200 ns, 3 V	≈ 0.65 V
2.1 nm	400 ns, 3 V	≈ 0.48 V
3.0 nm	1 μs, 3 V	≈ 0.55 V
3.6 nm	5 μs, 4 V	≈ 0.50 V

Table 1: Extrapolated time-constants for measured structures with comparable nano-crystal density.

thickness of injection oxide at 3 V bias is about 150 ns. Increasing thickness slows this injection process considerably with the largest effects taking place as thickness is increased beyond 2 nm. This is approximately where direct tunneling becomes inefficient in this large barrier system (≈ 3.15 eV).

These results stress that injection and extraction through large barriers, such as that of silicon dioxide, and in confined volumes naturally result in time-constants in 10's of ns or higher, but with longer erasure time and the benefit of long refresh times.

Applying a specific gate voltage results in a certain limited number of electrons in the quantum-dot, which in turn produces the threshold shift desired for memory through capacitive coupling. In Figure 5, at gate voltages where the mean number of electrons is an integer and a half, the variance is also a half as would be expected, because the system behaves as a two-level system and only an integer number of electrons is allowed. Reproducible memory states can only be detected if noise-margins are large enough. Due to the large variance, it is necessary to

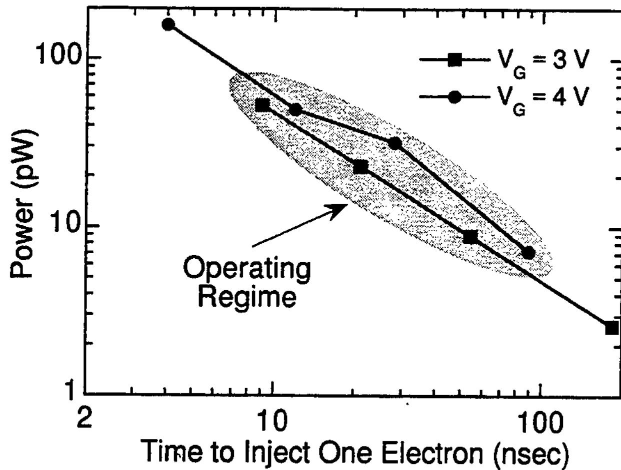

Fig. 6: Power required for injecting a single electron into the silicon dot as a function of the write speed.

provide sufficient statistical robustness. Thus, the need to use more than one electron even when single electron effects dominate.

The interaction of the confinement and operating voltages on the time-constants can best be summarized in the power-delay figure shown in Figure 6 for the write process. With the practical considerations of noise-margin taken into account through storage of more electrons, the figure points to large advantages in power density that accrue through limiting of the charge and at the expense of speed.

Conclusions

We have outlined some of the features of nano-crystal and quantum-dot memories that can be related to the quantum-confinement and small-dimensions of these structures. In particular, a remarkable consequence of the scaling of dimensions is the limited number of electrons needed to obtain observable memory behavior even at room temperature. However, the slowing of the injection process and increased effect of small charge variations must be considered in memory design.

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Performance and Long-Term Reliability of Multijunction
Amorphous Silicon Photovoltaic Modules

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Amorphous silicon (a-Si:H) photovoltaic technology has shown steady progress since the invention of the first a-Si:H solar cell in 1974 [1]. The first commercial a-Si:H solar cells were single-junction devices introduced by Sanyo in 1980 for solar-powered calculators. Recently, several organizations have constructed manufacturing facilities that are capable of producing multi-megawatt quantities of multijunction amorphous silicon PV modules. While the stabilized conversion efficiencies of commercial single-junction a-Si:H modules are only about 4 to 5%, the new multijunction modules exhibit stable efficiencies of about 8% [2].

The device structure of the new Solarex tandem modules is shown in Fig. 1. The total thickness of the a-Si:H alloy layers is about 400 nm while the tin oxide layer is about 600 nm thick, the zinc oxide layer about 100 nm and the aluminum about 300 nm. Thus, the total device thickness is only about 1.4 μm. The tandem structure consists of a front p-i-n junction with undoped a-Si:H in the i-layer and a back p-i-n junction containing an amorphous silicon germanium (a-SiGe:H) alloy in the i-layer. The p-layers are ~ 10 nm thick and consist of a boron-doped amorphous silicon carbon alloy. The n-layer in the first junction is actually a thin layer (~ 10 nm) of phosphorus-doped microcrystalline silicon while the n-layer in the back junction is a 30 nm thick layer of phosphorus-doped amorphous silicon.

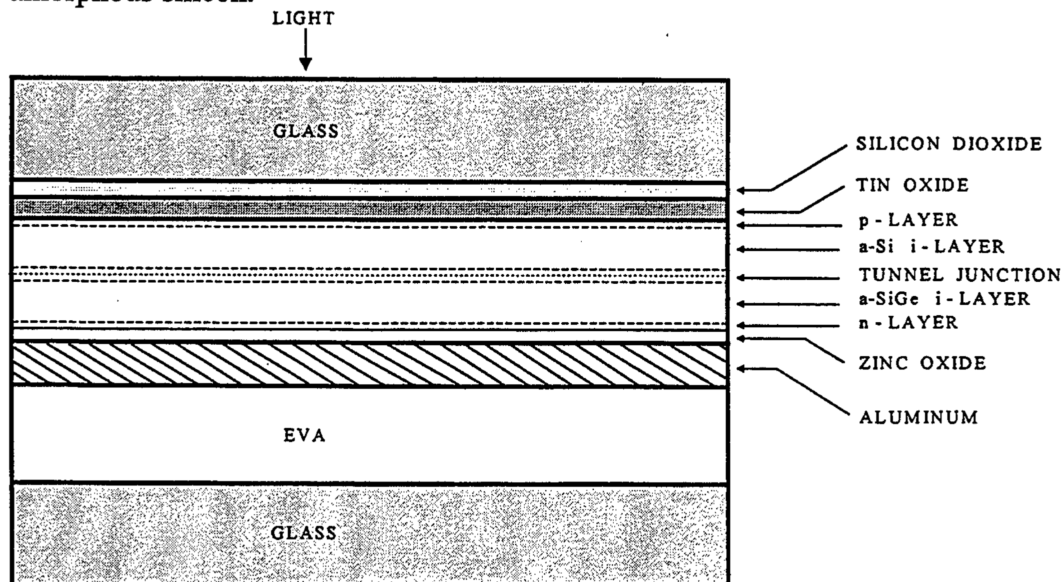

Fig. 1. A schematic of the Solarex tandem device structure.

The initial current-voltage characteristics of a 4 ft^2 tandem module under 1 sun illumination are shown in Fig. 2. The module was patterned into 40 series-connected cells by scribing the various layers during processing with computer-controlled Nd-YAG lasers coupled with a machine vision system. Thus, each tandem cell exhibits an open-circuit voltage of about 1.54 V and a short-circuit current density of about 9.4 mA/cm^2.

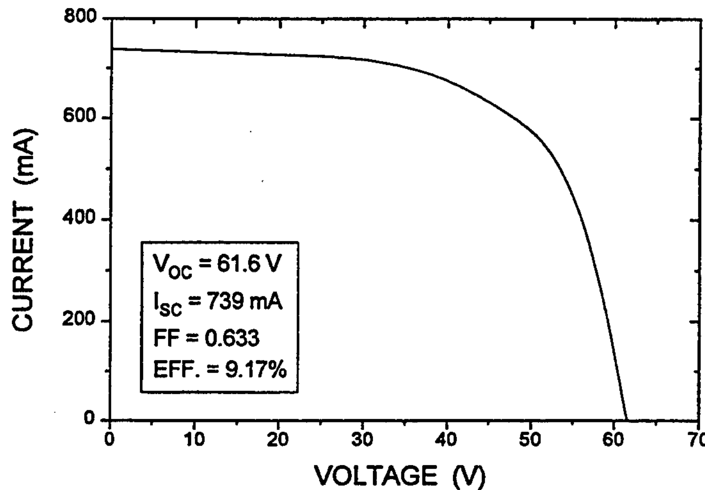

Fig. 2. Current-voltage characteristics of a 4 ft^2 tandem module (AM1.5 illumination).

The initial spectral response of a tandem junction solar cell is shown in Fig. 3. The front junction contains an undoped layer of a-Si:H that absorbs mainly the short-wavelength radiation (400 to 600 nm) while the back junction contains an a-SiGe:H alloy that can utilize the radiation mainly in the 600 to 900 nm wavelength regime. The optical gap of the a-Si:H in the front junction is about 1.75 eV while that of the a-SiGe:H layer in the back junction is about 1.45 eV.

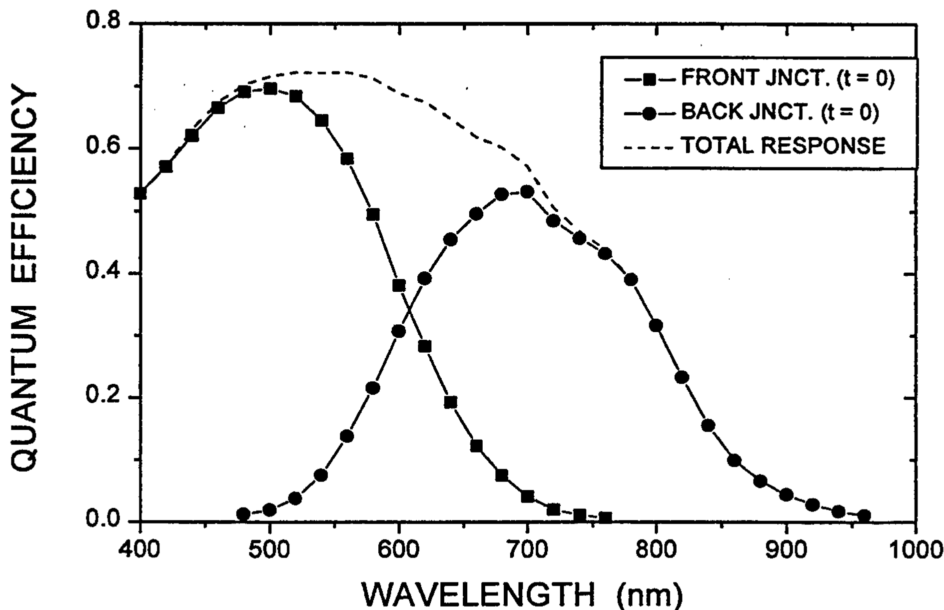

Fig. 3. The spectral response of a cell from a 4 ft^2 tandem module.

Even though the a-Si:H solar cell structure is very thin and is grown on a tin oxide surface with a sub-micron texture, relatively high production yields can be obtained on large-area substrates. Figure 4 shows a run chart for pilot production of 4 ft^2 tandem modules that were made over a period of a few weeks. The initial efficiencies during this period averaged about 9.0%, and there were no modules with efficiencies less than 7% so the manufacturing process appears to be quite robust. This is mainly due to the conformal coating capability of the plasma-enhanced chemical vapor deposition process that is used to deposit the a-Si:H alloys and to the reverse-bias curing process that burns out small defects in the films [3].

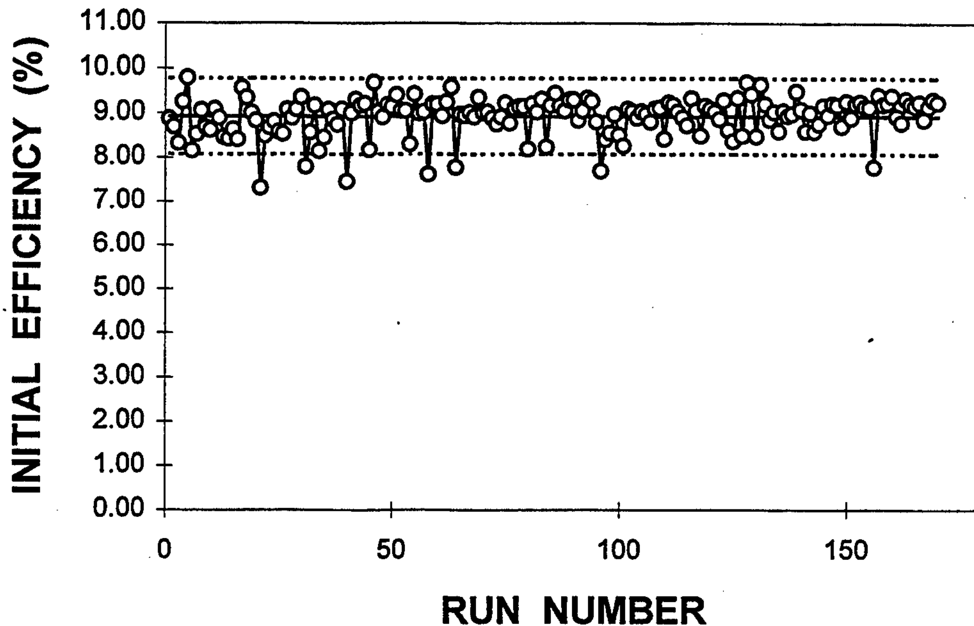

Fig. 4. A run chart showing initial efficiency of 4 ft^2 tandem modules vs. time.

All a-Si:H solar cells exhibit some degree of light-induced degradation in the first several months of exposure to sunlight. The performance of commercial single-junction a-Si:H solar cells typically degrades about 25% after exposure to sunlight before stabilizing. The Solarex tandem modules typically exhibit about 15% degradation before stabilizing.

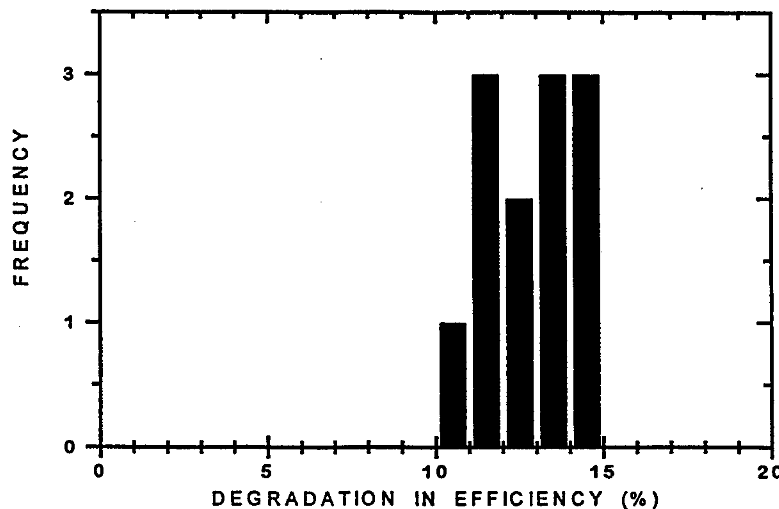

Fig. 5. A histogram showing the degradation experienced by twelve 4 ft^2 tandem modules after exposure to 600 hours of simulated sunlight.

Some representative data are shown in Fig. 5; in this case, the average degradation for twelve 4 ft^2 modules exposed to 600 hours of simulated sunlight at ~ 45°C was only about 13%. The degradation decreases as the ambient temperature increases so that at an operating temperature of 70°C, tandem cells stabilize after degrading about 9%.

Moreover, a-Si:H PV modules often show increased output when they operate at elevated temperatures unlike crystalline silicon solar cells. Figure 6 shows some data for the output of a 1 kW array of 4 ft^2 tandem modules at NREL (Golden, CO) as a function of operating temperature. The data collection started once the array had been outdoors for several months so that the modules were opertating in a steady state mode. Thus, tandem modules with a stabilized efficiency of 8.0% at 25°C would exhibit a value of about 8.7% at 60°C due to the effect shown in Fig. 6 and due to the reduced degradation at elevated temperatures. A polycrystalline silicon PV module with an efficiency of 11% at 25°C would also exhibit an efficiency of about 8.7% at 60°C [4].

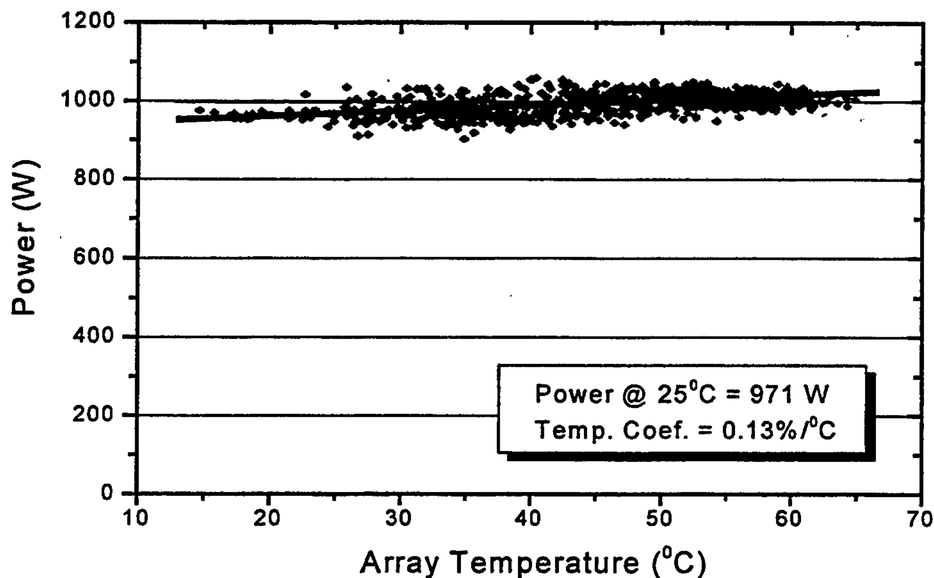

Fig. 6. DC power produced by an array of tandem modules as a function of temperature.

The newest Solarex tandem modules are 8.6 ft^2 in area and are protected from the environment by laminating the devices between two sheets of glass using an ethylene vinyl acetate encapsulant. Based on the results from a series of accelerated environmental tests, these modules should exhibit excellent long-term reliability.

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Amorphous Silicon Amplifiers: Is the Gain Worth the Pain?

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1. Introduction

In many ways, the technology of hydrogenated amorphous silicon (a-Si:H) can now be considered mature. The manufacture of millions of active matrix liquid crystal displays (AMLCDs) testifies to the commercial importance and performance of a-Si:H devices. Newer x-ray and optical large-area sensor arrays are also receiving widespread attention for medical and document imaging [1]. Yet, in all these applications, little or no signal processing is performed on the panel itself. For sensing applications in particular, focal-plane signal amplification or buffering would clearly be advantageous. So what are the challenges associated with incorporating circuits onto the sensor and how may they be overcome?

2. Circuit Issues

Currently, the only semiconductor practically available is a-Si:H, because the thin film deposition conditions are limited by the maximum temperature to which the glass substrate can be subjected. For the circuit designer, this enforced choice raises two primary issues; low electron mobility and device instability.

Field effect electron mobilities in a-Si:H are typically 1cm^2/Vs, approximately three orders of magnitude less than those for crystalline material. Consequently, the transconductance, g_m, of an a-Si:H thin film transistor (TFT) is also low, making significant gain more difficult to achieve. For a standard common-source configuration, the voltage gain is $\propto g_m R_D$ (where R_D is the drain resistance) so a low g_m forces the use large resistors and/or the cascading of several amplifier stages.

Gate-bias-induced instability in a-Si:H TFTs has been known for many years [2]. This effect causes the threshold voltage of the TFT to increase with time (perhaps by several hundred percent), when the device is subjected to a DC gate bias. At low gate voltages (<~20V), the threshold voltage shift (ΔV_T) appears to be the result of defect creation in the bulk a-Si:H [3]. TFTs used in display applications circumvent the issue of ΔV_T by the careful choice of materials and by subjecting the devices only to very low duty cycles. For a-Si:H amplifier circuits, the DC gate bias is required at all times during operation, potentially resulting in a large ΔV_T, and hence in a time-varying circuit gain.

A secondary concern is that the high R_D values required to overcome the low g_m can reduce the amplifier bandwidth, due to large RC time-constants. But what bandwidth is required? The application considered here is that of a column amplifier for an x-ray sensor array. A maximum

readout speed for such a sensor would be TV rate of 30 frames per second, which for 1000 rows would require a bandwidth of ~30kHz. A number of other issues (not least being patient exposure dose) effectively mean that the currently required bandwidth is likely to be lower than that above [4].

One approach to reducing the time-dependence of circuit gain might be to reset the ΔV_T *in situ*. However, this does not appear to be practical since, even with the application of a reverse gate bias, the reset process takes at least as long as the original shift [5]. Hence, we will consider two general approaches to circuit design that minimise the effect of ΔV_T on the gain.

3. Negative Feedback

In the first approach, we employ negative feedback to reduce the sensitivity of the closed loop gain (A_c) to variations in the open loop gain (A_o). The closed loop gain is given by

$$A_C = \frac{A_O}{1 + BA_O}, \qquad (1)$$

where B is the gain of the feedback loop. For sufficiently large A_o, $A_c \approx 1/B$, where B may be provided by stable passive circuit components. A disadvantage is that already scarce gain must be sacrificed in order to achieve this desensitivity. An example of such a negative feedback arrangement is shown in Fig.1, where gain is provided by three common-source stages, forming an inverting amplifier with $A_o \approx 10$. After a source-follower buffer, the output is fed back through R_f to obtain $A_c \approx 4$. Figure 2 shows the time-dependence

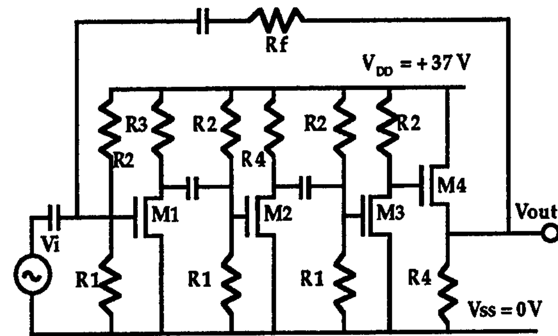

Figure 1. *Schematic of the a-Si TFT amplifier circuit. Components have the following values: R1 = 1.5MΩ, R2 = 5MΩ, R3 = 1MΩ, R4 = 2MΩ, Rf = 1MΩ, all capacitances are 1nF. The TFT (W/L) values for M1 – 4 are 40, 20, 10, and 20.*

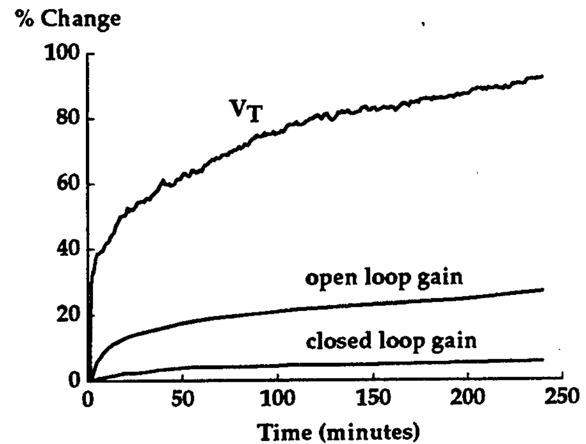

Figure 2. *Percentage changes in V_T, open loop gain, and closed loop gain as a function of operating time.*

of A_o, A_c, and the ΔV_T of an individual TFT. The use of negative feedback has reduced the variation of A_C to ~5%.

A drawback of this topology results from the AC-coupling capacitors required to isolate each stage; they are difficult to integrate owing to their large physical dimensions, and the circuit bandwidth is also adversely affected. Figure 3 shows the measured frequency response of the circuit from Fig.1, in which the low frequency roll-off due to the AC-coupling capacitors can be seen.

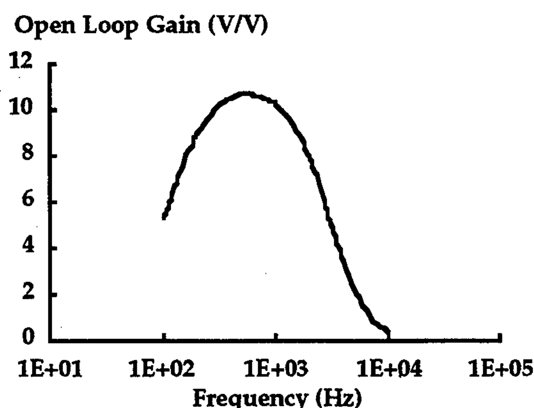

Figure 3. *Measured open loop frequency response of the amplifier in Fig. 1.*

4. Compensated Biasing

In this section we consider a more practical circuit using a differential pair, one of the basic building blocks of analog electronics. Here, the gain of the amplifier is constant, provided that the bias current is kept fixed (and assuming that other components are matched).

Referring to Fig.4, the voltage at node A increases as the threshold voltage of M1 shifts upwards. The biasing for M1 is designed such that $\delta V_A/\delta V_T \approx 1$ so, assuming that ΔV_T for M1 is equal to that of M2, $(V_{GS,M2} - V_{T,M2})$ is kept constant, resulting in a constant I_{bias}. The differential amplifier thus compensates internally for changes in V_T. Figure 5 shows the change of open loop gain as a function of the TFT V_T. A_o changes by less than 1.5% for a 250% change in V_T, corresponding to an operating time of about 4 hours. The nominal values for I_{bias} and A_o were 17μA and 4.4 V/V respectively.

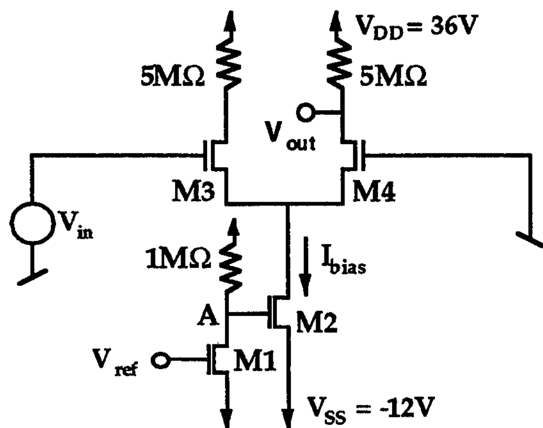

Figure 4. *Differential amplifier circuit using compensated biasing. For M1, W/L = 10, and for M2-4, W/L = 40.*

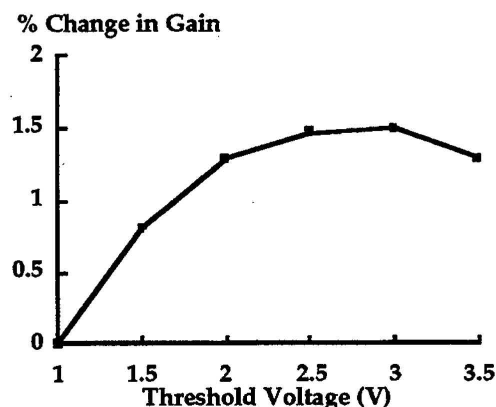

Figure 5. *Measured change of differential amplifier gain as a function of TFT threshold voltage.*

Owing to the absence of AC-coupling capacitors, this circuit displays an improved low frequency behaviour (see Fig.6), and is more suitable for full integration.

5. Discussion and Conclusions

In the preceding sections, we have demonstrated the feasibility of constructing a-Si:H amplifiers with a reasonable performance. The question of what constitutes a "reasonable performance" depends on the application. It is suggested here that column amplifiers providing some gain and buffering for the outputs from a sensor array before they are sent off-panel would be one valuable application. In this example, high voltage gain is not a prime requirement. Small, slow variations

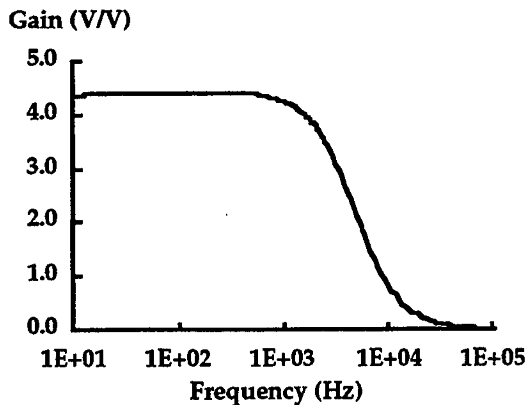

Figure 6. *Frequency response of the differential amplifier.*

in gain might also be acceptable, provided such changes are consistent between columns. Minimisation of the variations in gain for each amplifier is still important because this limits the range of possible differences between columns (and hence one source of fixed pattern noise in the sensor). The circuits presented here meet these requirements well.

For the column amplifier application, the area occupied on the panel by the circuit is not a significant concern. Each of the circuits discussed above requires several TFTs, each with an area of ~400µm x 10µm; this is small in comparison to the array area and comparable with the sensor pixels, which are typically >100µm square [4]. While the negative feedback topology presented here is not suitable for integration in its present form on account of the AC-coupling capacitors, the principle is nonetheless valid. Large value resistors can be fabricated in a reasonable area by using the microcrystalline silicon layer frequently used in the source and drain contact regions of the TFTs. Hence there is no fundamental hindrance to the fabrication of fully integrated amplifiers.

The present amplifier circuits were found to operate at frequencies of several kiloHertz. Here, the response was limited by the load of the measurement equipment on the output, a low noise amplifier with an input resistance and capacitance of 100MΩ and 15pF, respectively. Simulations suggest that fully integrated circuits could operate between 10kHz and 20kHz. While still short of the TV-rate scanning goal, the bandwidth is quite acceptable for present applications, where the capture rate is 4 frames per second [4].

In conclusion, two successful design approaches to the realisation of a-Si:H amplifiers have been presented, demonstrating the feasibility of incorporating a-Si:H circuits onto flat-panel sensors. So, while there is some "pain" to designing a-Si:H amplifiers, there are also significant "gains" to be achieved.

6. Acknowledgments

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Low-Temperature Poly-Si TFT Technology for Lightweight, High-Performance Displays

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Abstract

Polycrystalline silicon (poly-Si) thin-film transistor (TFT) technology is presently employed in high-density active-matrix liquid crystal displays (AMLCDs) because it provides superior device performance as compared with amorphous silicon (a-Si) TFT technology. With the trend in information display toward lightweight, low-power, rugged displays, there will be a need to adapt active-matrix technology to plastic substrates for high-performance, high-resolution, portable displays. Significant challenges exist in the development of a poly-Si TFT fabrication process which is compatible with plastic substrates. This paper discusses the technological approaches to surmounting these challenges and achieving high-performance TFTs for compact, lightweight AMLCDs in the future.

Introduction

There are several major and consistent trends in information display [1]. First is the ever increasing demand for higher display resolution and information content. Second is the evolution toward thin, lightweight, low-power displays. Third is the use of color for information coding and imaging, coupled with market demand for full-color high-performance systems. These trends have driven the development of display technology to the current state-of-the-art. Display technology today is dominated by self-luminous display devices such as cathode-ray-tubes (CRTs), back-lit active matrix liquid crystal displays (AMLCDs), electro-luminescent (EL) displays and plasma display panels (PDPs).

As requirements for displayed information burgeon in the future and the flat-panel display becomes a dominant electronic medium, there will be compelling reasons to shift from self-luminous displays to reflective displays. The most obvious one is that reflective displays utilize existing ambient illumination and thus do not require backlights, hence power and form factor can be significantly reduced. Another reason is that reflective images scale with the level of illumination and the human visual system, so that color gamut and contrast are maintained for all lighting conditions [2,3].

Reflective LC displays offer the possibility of extremely low power consumption and are therefore well-suited to portable applications. Reflective LC materials require a relatively large voltage difference between threshold and saturated states, so that simple multiplexed addressing cannot be used in high-resolution display applications, due to the Alt-Pleshko limit [4]. Therefore, active-matrix addressing will be essential for high-resolution reflective LC displays.

Poly-Si TFT Active Matrix Technology

Polycrystalline-silicon (poly-Si) thin-film transistor (TFT) technology provides the capability to monolithically integrate logic and control circuitry to achieve compact, highly reliable, lower-cost display modules. It is employed in high-performance AMLCDs [5], and can be used for active-matrix addressing of reflective displays as well. The integration of driver circuitry greatly reduces the number of connections which need to be made to the

display, and thereby can alleviate the issue of bonding to flexible substrates. In order to make this technology practical for compact, lightweight display systems in the future, it is necessary to develop a fabrication process which is compatible with plastic substrates: dramatic reductions in thermal-processing budget must be made, without accompanying sacrifices in TFT performance. The long-term stability of poly-Si TFTs is also a potential issue which must be assessed for active-matrix-addressed reflective LC displays. This is because higher voltages will be required to drive the new reflective LC materials (as compared with TN LC materials employed in AMLCDs today) and poly-Si TFTs are known to suffer increased degradation in performance with increasing biasing voltages [6].

TFT Fabrication Process Constraints

For reflective display applications, a variety of plastics can be used as a lightweight active-matrix substrate material, including polyimide or Kapton, which can withstand process temperatures up to 200°C. Lower-cost polyethylene terephthalate (PET, or polyester) can also be used, but with process temperatures limited to a maximum of 100°C [7]. In general, superior poly-Si TFT performance is achieved with higher-temperature fabrication processes, particularly because the quality of the critical gate-dielectric interface is very sensitive to process temperature. For lightweight, high-performance displays in which the optical transmission of the substrate is not a consideration, 200°C is a reasonable upper limit for the substrate temperature during the TFT fabrication process.

TFT Performance Requirements

In order to meet the drive requirements of the LC materials, the pixel TFTs must meet the following performance targets: effective electron mobility > 0.5 cm^2/Vs; leakage current < 1 pA/μm channel width (needed for gray-scale display applications); threshold voltage < 5 V; and breakdown voltage > 20 V. Higher mobilities (> 30 cm^2/Vs) are desirable for the integration of driver circuitry. In order to achieve uniform gray-scale images, TFT performance must not vary significantly across the display. Better than 10% uniformity in TFT drive current across a display is a minimal requirement.

Low-Temperature, High-Performance TFT Active-Matrix Technology

Channel-Film Formation

A poly-Si TFT channel film can be formed by either of two methods: amorphous-phase deposition and subsequent crystallization, or direct polycrystalline-phase deposition. The latter requires process temperatures >200°C and is therefore not compatible with plastic substrates. Low-pressure chemical vapor deposition (LPCVD) and plasma-enhanced chemical vapor deposition (PECVD) are the most commonly used techniques for depositing the precursor amorphous Si film. The LPCVD technique requires temperatures >400°C and is therefore not compatible with plastic substrates. The PECVD technique yields films which contain a significant amount (>10 atomic percent) of hydrogen; this leads to complications in processing (e.g. the films must be dehydrogenated prior to crystallization) as well as inferior poly-Si TFT performance [King95]. Therefore, low-hydrogen-content sputtered amorphous Si films are the preferred precursor channel film material for high-performance poly-Si TFTs.

Solid-phase crystallization techniques (furnace annealing or rapid thermal annealing) require process temperatures in excess of 450°C and hence are not compatible with plastic substrates. Pulsed excimer laser annealing is the only crystallization technique which is compatible with plastic substrates. (The pulsed laser energy is absorbed only by the Si film, locally melting the Si for a very short duration, e.g. 100 ns, with each shot, so that the substrate is not heated substantially overall in the process.) This technique has recently been employed in the fabrication of poly-Si TFTs on a plastic substrate coated

with a thin (<1 μm-thick) buffer layer of SiO_2 [Carey97]. The quality of a laser-crystallized Si film, hence TFT performance, is highly dependent upon the laser energy fluence as well as the thickness of the film. Because of inherent nonuniformities in laser-beam intensity and deposited film thickness, device performance uniformity can be a significant issue for the laser crystallization technique.

Gate-Dielectric Formation

Although trap states in the bulk of the channel poly-Si film tend to dominate TFT electrical behavior, a high-quality gate dielectric is critical for device performance and reliability. Silicon dioxide is the preferred material because it forms an excellent interface with Si. It can be formed by a variety of methods, including thermal oxidation, LPCVD, atmospheric-pressure CVD, PECVD, and electron-cyclotron resonance (ECR) CVD. The high temperatures required for thermal oxidation make it incompatible with plastic substrates; therefore, a deposited gate dielectric must be employed.

The LPCVD method requires temperatures >350°C is therefore not suitable for the proposed work. The PECVD method can be used to deposit films at temperatures down to 100°C, but the quality of the SiO_2 deteriorates rapidly with decreasing deposition temperature. This effect can be compensated by improving the quality of the Si/SiO_2 interface through a pre-deposition oxygen plasma treatment. The ECR method can be used to deposit films at very low (<100°C) temperatures, and it provides a high-quality SiO_2/Si interface as well as an additional benefit of defect passivation for underlying poly-Si layers [8,9]. Hence, it is the most attractive gate-dielectric formation method for low-temperature high-performance active-matrix technology. It should be noted that step coverage is an issue for ECR-CVD SiO_2 films, so that composite gate-dielectrics (e.g. an ECR-CVD SiO_2/PECVD SiO_2 stack) may ultimately prove to be optimal. Because high threshold voltage is often a problem for low-temperature poly-Si TFT technology, the use of composite oxide/nitride gate-dielectrics can also provide a means for adjusting threshold voltage [10].

Source/Drain Formation

A top-gate, self-aligned TFT structure achieves minimal parasitic capacitance between the gate and the source/drain regions, which is important for minimizing feedthrough voltages and feedthrough-voltage variations, for good display image quality. Any high-performance active-matrix TFT technology should be based on this structure. Ion implantation or ion-shower doping followed by laser annealing can be used to form low-resistivity (<1 kΩ/square) source/drain regions which are self-aligned to the gate electrode. Variations of the basic structure, such as multiple-gate and offset-drain structures, can be utilized as needed to achieve sufficiently low TFT leakage current and also to improve device reliability.

Defect Passivation/Device Reliability

The electrical behavior of a poly-Si TFT is dominated by the effects of defect states within the poly-Si film. The incorporation of hydrogen into the channel layer ("hydrogenation") to passivate the defect states significantly improves device performance, as well as the uniformity of device performance. An active-matrix technology which is adaptable to plastic substrates cannot afford a hydrogenation process, because of the high temperatures (typically >250°C) required. Hence, device performance uniformity issues will likely be exacerbated.

Long-term reliability is an important issue for poly-Si TFTs, which have been shown to suffer significant performance degradation under static (dc) bias stress. Most notably, the threshold voltage increases significantly under on-state stress conditions (high gate bias and high drain bias), so that the device eventually does not turn on properly. Circuit failure can therefore occur after prolonged operation. For future AMLCD technology, the reliability of integrated poly-Si TFT driver circuitry will be of major concern. Previous studies have

shown that the dominant degradation mechanism is trap-state generation at the gate-oxide interface near the drain and within the poly-Si channel film [6], which is attributed to the breaking of Si-H bonds formed as a result of a hydrogenation process. With the elimination of the hydrogenation process, device reliability issues will likely be assuaged.

Conclusion

A transition to reflective displays represents the next major paradigm shift in the development of display technology. In order to achieve a truly portable and capable reflective device, reflective LC materials must be integrated with state-of-the-art active-matrix technology adapted to lightweight (e.g. plastic) substrates. Significant challenges exist for the development of a practical poly-Si TFT technology for compact, lightweight displays, because of the severe constraint on process temperatures. The critical steps in the fabrication of high-performance TFTs are the channel formation (deposition and crystallization) and gate-dielectric formation processes. Device performance uniformity will likely be a more serious issue for ultra-low-temperature (<200°C) fabricated poly-Si TFTs because a hydrogenation process is precluded.

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High Performance Inverted Staggered a-Si TFT Obtained by Using Hydrogen Treatment

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Thickness of the a-Si:H layer in inverted staggered a-Si TFT was successfully reduced to less than 100nm, with an accompanying increase in the field effect mobility and a reduction in the threshold voltage. The improvement was due to the decrease in the surface defective states of the active layer generated during the n+ a-Si:H etching process realized by hydrogen treatment before the silicon nitride layer deposition.

1. INTRODUCTION

Amorphous silicon thin film transistors(a-Si TFTs) are important electronic devices with wide commercial application in liquid crystal displays, page-width printers, and matrix image sensors. However, many problems are to be solved. For example, during the n+ a-Si:H etching process, the surface defective states including Si dangling bonds are generated by ion bombardment[1] and they should cause pinning of the Fermi Level at the back channel surface and affect the carrier transport at the channel especially in the thin active layer region[2][3]. So in thin active layer a-Si TFT, the field effect mobility(μ_{FE}) usually decreases and the threshold voltage(V_{th}) increases[4].To keep good TFT performance, the thickness of the intrinsic a-Si:H layer(d_{Si}) is usually more than 200nm, but such a thick a-Si:H layer means disadvantages, i.e., a high photosensitivity and a long tact time in the a-Si:H deposition process.

H radical treatment is an effective way to etch out weak bonds and to terminate dangling bonds at the top surface of a-Si:H[5]. In this paper, to improve the performance of a-Si:H TFT, H radical treatment was adopted to terminate the surface defective states generated during the previous n+ a-Si:H etching process.

2. Experimental

The cross sectional view of inverted staggered a-Si TFT in our experiment is shown in fig.1. The process of preparing TFT is as follows. After the gate electrode pattering of Mo/Al film sputtered on Corning 7059 glass substrates, 300 nm thick a-SiN_x:H gate insulator, undoped a-Si:H from 80nm to 250 nm, and 30 nm P-doped n+ a-Si:H layer were continuously deposited in plasma enhanced chemical vapor deposition (PECVD)

system. After the n+ a-Si:H etching process, H radicals treatment was performed in PECVD system. The treating time was 60s. The deposition and H treating parameters of substrate temperature(T_s), radio frequency power density(P_{rf}), and pressure(P) were shown in Table 1. Finally, all the samples were annealed at 230°C for 1 h in N_2 atmosphere.

3. Results and Discussion

Fig.2 shows I_d-V_g curves in a-Si:H TFTs with d_{Si}=80nm. From it, in the H treated TFT, the on current and the threshold voltage are about 4×10^{-6} A higher and 1.5V lower than those of the untreated TFT, respectively.

Fig. 3 indicates a-Si:H layer thickness dependence of the field effect mobility(μ_{FE}) in the saturation region(Vd=10V). In the TFTs fabricated with and without H treatment, μ_{FE} increases to 0.86-0.91cm^2/Vs on decreasing d_{Si} to 130nm. However, when d_{si} is 80 nm, μ_{FE} increases to 0.94cm^2/Vs for the H treated TFT, whereas μ_{FE} decreases to 0.80cm^2/Vs for the untreated one.

In the inverted staggered TFT structure, the carrier transport is governed by two kinds of resistance, i.e., the channel resistance(R_{ch}) and the parasitic resistance (R_p)[6]. In the inverted staggered TFT, the thick a-Si:H layer between the source-drain electrodes and the channel induces the increases in Rp, as shown in Fig.4(A), limiting the carrier transport as the space charge limited current. In TFTs with H treatment or not, Rp monotonically decreased with reducing d_{Si} is shown in Fig.4(B). In the H treated TFT, the increase in μ_{FE} and decrease in V_{th} on reducing d_{Si} is attributed to the decrease in R_p without increasing R_{ch}. By contrast, in the TFT with no treatment, R_{ch} drastically increases on reducing d_{Si}, causing the decrease in μ_{FE} and increase in V_{th}.

During the n+ a-Si:H etching process, a large number of surface defective states is generated by the ion boadarment in plasma. They would cause the degradation in performance of TFT. After hydrogen plasma treatment, the surface defective states including Si-Si weak bonds and Si dangling bonds at the active layer surface are mostly eliminated. This would prevent the Fermi Level at the back channel surface from being pinned.

4. CONCLUSION

The effect of H treatment on the performance of silicon nitride passivated a-Si:H TFT has been investigated. From the results, the hydrogen treated a-Si TFTs with very thin active layer have advantages over the untreated TFT. The improvement was caused by the defect termination in H plasma.

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Table 1 Parameters of deposition and H treatment

Material	T_S(°C)	P_{rf}(W/cm^2)	P(Pa)
a-SiN$_x$:H	270	0.5	85
a-Si:H	220	0.1	80
n+ a-Si:H	220	0.2	80
H treatment	250	0.2	50

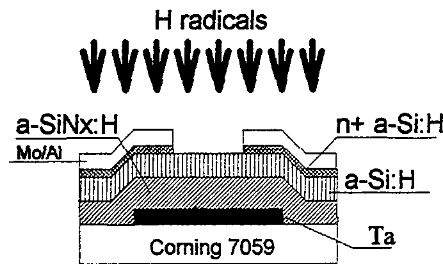


Fig.1 The cross section of the inverted staggered a-Si:H TFT

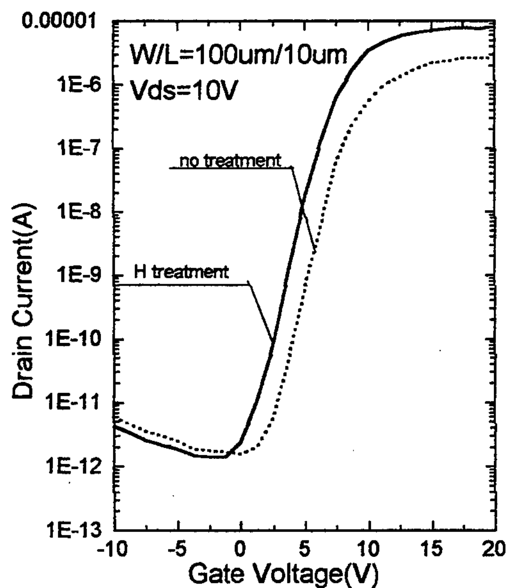


Fig.2 The Id-Vg characteristics of TFT before the top nitride deposition

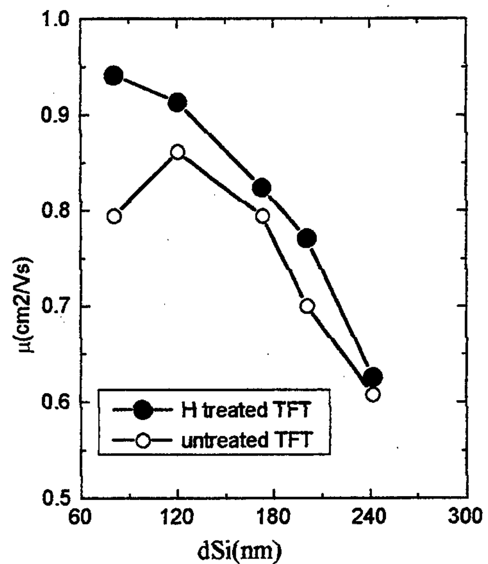
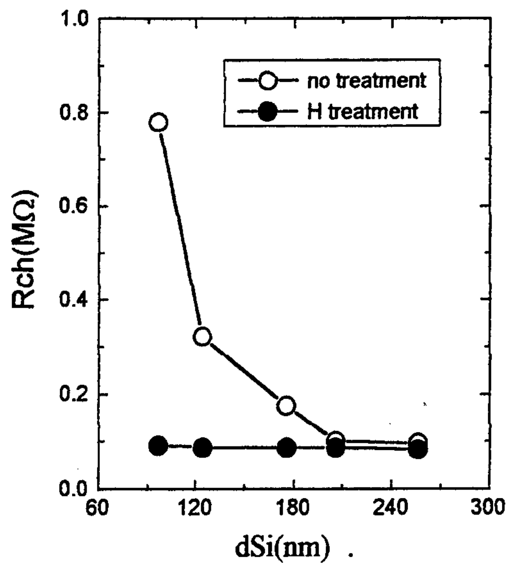
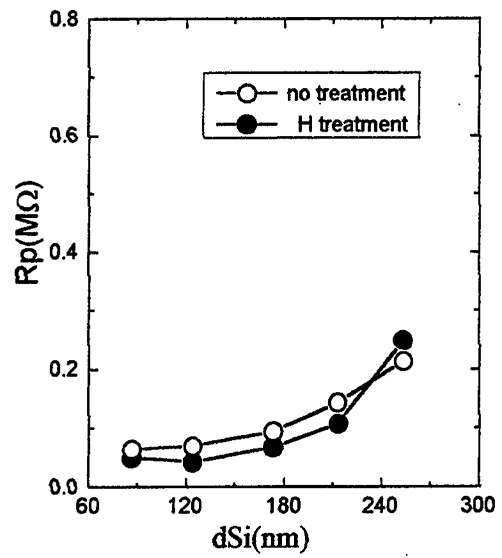


Fig.3 a-Si:H thickness dependence of field effect mobility



(A)



(B)

Fig.4 a-Si:H thickness dependence of (A)channel resistance(Rch) and (B)parasitic resistance(Rp)

Fabrication of Inverted-staggered Polycrystalline Silicon Thin Film Transistors by Employing Selective Laser Annealing

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I. INTRODUCTION

Polycrystalline silicon (poly-Si) thin film transistors (TFT) fabricated by the excimer laser annealing may be a promising device for various LCD application due to their low thermal budget.[1] Recently, much attention has been paid to the bottom-gate (BG) poly-Si TFT, which may be easily fabricated by the laser annealing of PECVD intrinsic a-Si:H and n^+ doped a-Si:H film, because the structure and fabrication process of BG-TFT are almost identical to those of the commercial a-Si:H TFT applicable for the low cost and large size LCD panels.[2][3] However, it may be rather difficult to fabricate the LDD-structured BG TFT in order to reduce the inherent large leakage current because its fabrication process are complicated due to the additionally required n^- a-Si:H deposition and photomask.

The purpose of our work is to report the new BG poly-Si TFT with local amorphous-Si (a-Si) channel region by employing the selective laser annealing. In the proposed device, the leakage current is decreased significantly like that of a-Si TFT while the ON current is almost identical to that of conventional poly-Si TFT. It should be pointed out that the total mask number and the fabrication process are almost identical to those of a commercial a-Si:H TFT because the proposed device does not require any additional LDD process and activation.

II. DEVICE STRUCTURE

The cross-section of the proposed etch-stopper BG poly-Si TFT is shown in Fig. 1. The major difference in the proposed TFT is the existence of the local a-Si region near the drain junction, if compared with the conventional etch-stopper BG poly-Si TFT with fully recrystallized poly-Si channel. The series resistance of conventional LDD TFT is not changed with gate voltage so that the tradeoff between the ON current and the leakage current should be reconsidered. However, the resistance of the local a-Si region is varied significantly with the gate voltage so that the effective suppression of leakage current may be allowed without sacrificing the ON current. Under the ON state, the resistance of a-Si is decreased significantly due to the electron inducement while under the OFF state, the local a-Si region plays an important role in suppressing the field emission of hole carriers.[4]

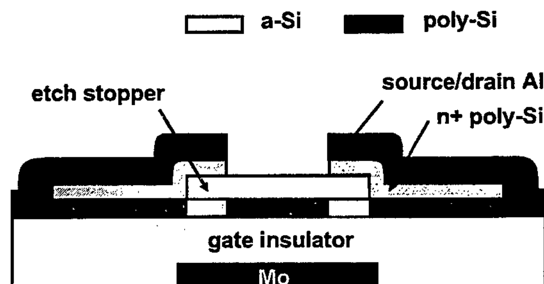

FIGURE 1. The cross-section of the proposed bottom-gate poly-Si TFT with the local a-Si region near the drain junction.

The process sequence of the proposed device is shown in Fig. 2. The key process step is the selective recrystallization of an active a-Si layer by employing the anisotropic properties of excimer laser annealing with no lateral thermal propagation. (Fig. 2b) [5] The n^+ a-Si layer for ohmic contact is used as a laser-absorbing layer, under which the local a-Si is never crystallized. Therefore, any additional mask and processes for the selective recrystallization are not required in the proposed device by employing the n^+ a-Si source/drain contact as the laser absorbing layer. Also, the simultaneous crystallization of active a-Si and n^+ source/drain contacts in the proposed device may reduce the fabrication cost and process sequence considerably.

III. EXPERIMENTALS

A 2000Å-sputtered Mo layer was deposited on an oxidized wafer and etched to define gate electrode. The 3000Å-thick SiN_x, 600Å-thick a-Si:H and 1000Å-thick SiO_2 are deposited subsequently as gate insulator, active layer and etch stopper by PECVD.

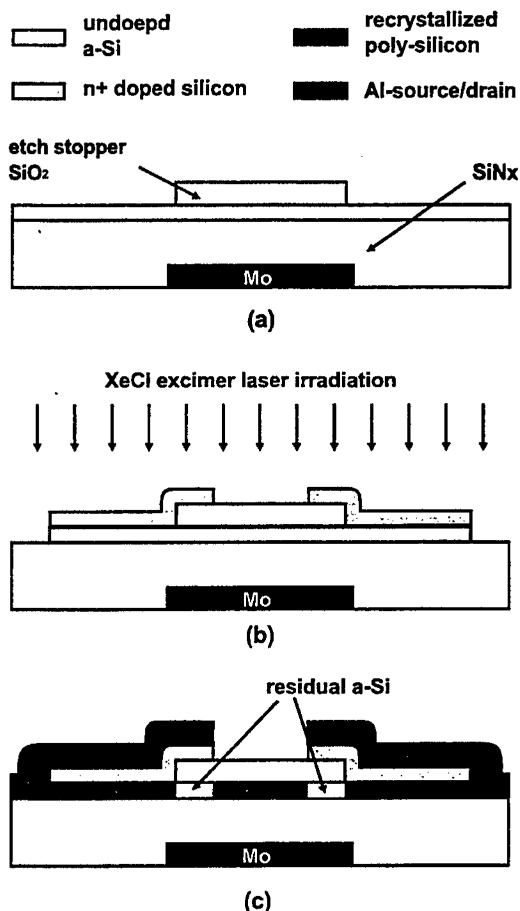

FIGURE 2. The key process sequence for the new BG TFT. (a) the definition of etch-stopper (b) the simultaneous fabrication of channel poly-Si and a-Si by one-step laser annealing after patterning of source/drain contacts (c) source and drain metallization

After patterning of etch stopper layer (Fig. 2a), a 400Å-thick n^+ a-Si:H is deposited by PECVD. The n+ a-Si:H layer and intrinsic a-Si:H layer are etched successively in the source/drain mask step so that the additional photomask for defining the active layer is not required (Fig. 2b). By XeCl laser irradiation of 300 mJ/cm^2, the a-Si channel region under the etch-stopper oxide without n+ a-Si layer is completely recrystallized but the a-Si region under the double layer of n+ a-Si/etch-stopper oxide remains to be unchanged due to the significant absorption of irradiating laser in the top n+ a-Si layer. The total number of mask is five which is identical to those of conventional etch stopper TFT.

III. RESULTS AND DISCUSSION

The measured I_D-V_G curves of the conventional BG TFT and proposed BG TFT are shown in Fig. 3. The leakage current of proposed BG TFTs with a-Si length of 1 μm is decreased by the magnitude of three orders, compared with those of conventional BG TFT.

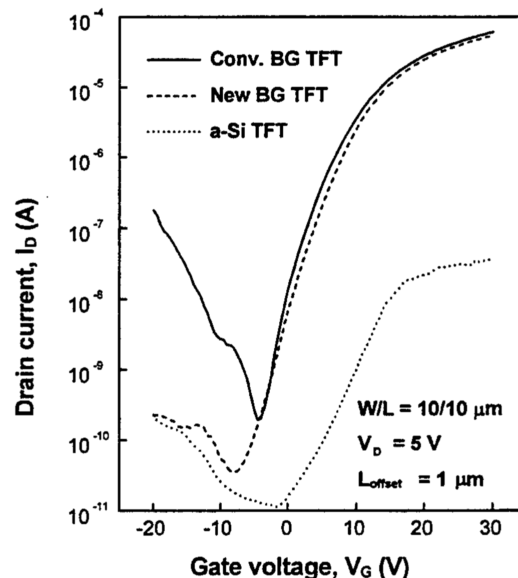

FIGURE 3. The I_D-V_G curves of the conventional BG TFT and proposed BG TFT, the length of a-Si region is 1μm. The dotted line is denoted to the a-Si TFT.

It should be noted that the leakage current due to the trap-assisted tunneling via grain boundary near the drain junction,[4] may be suppressed effectively by the amorphous-phase silicon region. On the other hand, he ON current of a new TFT is almost identical to that of conventional BG poly-Si TFT due to the significant decrease of surface resistance in the local a-Si region where the electron channel is formed by the overlapped gate field. By employing the new structure with a-Si region near the drain junction, the proposed device have shown the unique device characteristics

which are those of a-Si TFT under the OFF state but those of poly-Si TFT under the ON state. The field-effect mobility of new BG TFTs is about 27 cm^2/Vs which is comparable with 31 cm^2/Vs of conventional TFTs. In order to demonstrate the inversion effects of a-Si region on the device characteristics, the a-Si TFT with W/L = 10/10 μm has been fabricated. Although the subthreshold slope is worse than that of conventional a-Si:H TFT due to the dehydrogenation before the laser annealing, the drain current of dehydrogenated a-Si TFT is increased with gate voltage increase by more than the magnitude of three orders, as shown in Fig. 3.

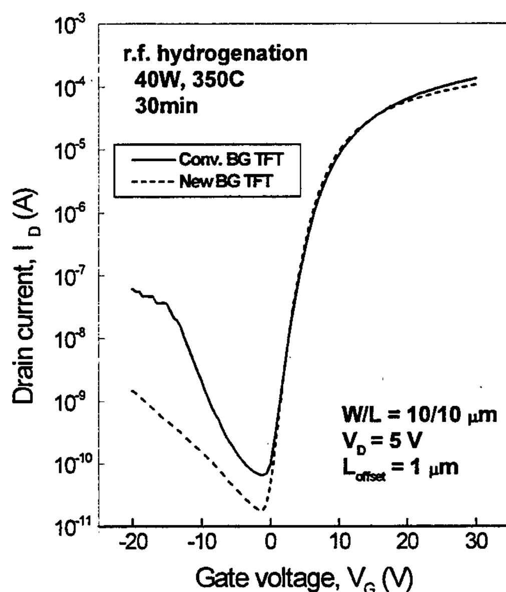

FIGURE 4. The I_D-V_G characteristics for the conventional and new BG TFT after 30 min hydrogenation.

The hydrogenated BG TFT exhibits the improvement of subthreshold slope due to the reduction of trap-states in the a-Si region as shown in Fig. 4. However, the field-effect mobility (45.6 cm^2/Vs) of a hydrogenated new BG TFT is much lower than 64.6 cm^2/Vs of conventional BG TFT due to the more significant improvement of poly-Si quality than a-Si quality by hydrogenation.

IV. CONCLUSION

We have fabricated the new BG poly-Si TFT with local amorphous-Si (a-Si) channel region by employing the selective laser annealing. Because of the local a-Si region near the drain junction, the leakage current of new poly-Si TFT is decreased significantly while the ON current is not decreased. The local a-Si region has been successfully fabricated without any additional mask and process.

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NANOLITHOGRAPHY FOR NANOSCALE AND QUANTUM DEVICES

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The rapid development of the field of nanometer science and technology has been driven to a large part by our increased ability to fabricate and characterize structures with nanometer scale dimensions. Lithography, the definition of an arbitrary pattern in a sample or a sacrificial layer on that sample, is one of the processes essential to the fabrication of nanostructures with atomic-scale precision This paper contrasts 'conventional' nanolithography where high energy focused particle beams are used as the lithographic tool with a proximal probe approach to nanolithography. A lithographic capability for device research requires more than a simple demonstration of feature sizes with a desired critical dimension. Rather one must have an understanding and control of such issues as process latitude, pattern fidelity and feature placement as well as the ultimate resolution of the lithographic technique.

Length Scales in Nanoelectronics

Looking into the future the point will eventually be reached when down scaling of existing silicon based metal-oxide-semiconductor transistor (MOSFET) technology will no longer be possible. The MOSFET scaling limit is currently believed to be 30-50 nm. Below this limit the physical phenomena which become dominant in the nanometer size regime become candidates for a device technology from which computational functional circuits could be fabricated. For example, if one makes a capacitor small enough, the energy needed to add an additional electron can be much greater than the thermal energy of the electron which, at room temperature, is 25 meV. A 'back of the envelope' calculation shows that this requires a capacitor with lateral dimensions of about 10 nm, i.e., some 30 atomic diameters.

Nanolithography with Electrons

A steered focused beam lithography is the preferred technique for nanolithography as well as mask making and prototyping in present day microelectronics processing. The technology of choice is high energy e-beam lithography as a wide range of tooling is available and the requisite expertise is well documented in the literature.

Over the past decade or so, the search for techniques to increase resolution has followed two paths. First, the spot size of the e-beam tool has been decreased by improved focusing usually accompanied by increasing the energy of the electrons. As a result, commercial tools operating at 100 keV and converted transmission electron microscopes operating at several hundred keV have all been used to push the resolution of

e-beam nanolithography. The second approach is to use extremely low voltages. Here the problems associated with electron scattering are avoided so the energy of the electrons can be deposited into a volume close to that defined by the spot size of the beam. The logical extension of this is to use essentially zero (<50 eV) incident energy. This can be achieved by using a scanning tunneling microscope (STM) to generate a spatially confined (although not focused) beam of electrons.

Modeling of e-beam Lithography

Accurate modeling of electron scattering has become increasingly important as more reliance is placed on Monte Carlo simulation to optimize e-beam lithography processes.. Our recent work has investigated the importance of the various physical mechanisms which are incorporated in a Monte Carlo code. Specifically, we have studied the inclusion of inelastic scattering (i.e., the creation of fast secondaries) and the form of the elastic scattering cross section on e-beam lithographic spread functions. Previous work of this type has highlighted the issue of resolution limits in e-beam lithography[1] and/or curve fitting approximations to lithographic spread functions.

Pattern Distortion (Proximity Effects)

In addition to affecting the resolution in e-beam lithography, electron scattering in the resist and substrate results in energy being deposited in the resist at points many microns remote from the point of impact of the primary electron beam. As a result, the size of a given feature is affected not just by the exposure dose given to that feature but also the exposure dose applied to areas of the sample in the vicinity of the feature. This phenomenon is referred to as 'Proximity Effects'.[2]

Correction of proximity effects is a mathematically ill posed problem because their exact correction requires the application of negative amounts of energy with the e-beam which is, of course, physically impossible. Research at NRL has concentrated on efficient algorithms for generating pixel by pixel dose adjustments.[3] The 'blurring' of the incident beam exposure profile can be characterized by a point spread function which is dependent only on the incident beam parameters. Thus the effect of the exposure blurring can be described as a convolution of the applied areal exposure dose, $\boldsymbol{D}$ and the point spread function $\boldsymbol{T}$. Thus the absorbed dose $\boldsymbol{A}$ is given by

$$\boldsymbol{A}=\boldsymbol{T} \otimes \boldsymbol{D}, \text{ where } \otimes \text{ represents the convolution operator.} \quad (1)$$

this can be inverted by treating it as a minimization problem, i.e., the solution for $\boldsymbol{D}$ is generated by minimizing:

$$|\boldsymbol{T} \otimes \boldsymbol{D} - \boldsymbol{O}|^2$$

The generation of negative dose values can be eliminated by the inclusion of a regularizer in the expression (shown above) to be minimized. The choice of a regularizer should reflect additional knowledge that is available about the solution which is not inherent in the minimization expression. We have based the regularizer on the informational or Shannon[4] entropy which is widely used as a metric of positive real valued distributions. Solving the resulting minimization problem generates an optimum (in the mathematical sense) solution to the correction of proximity effects.

Low Energy Electron Nanolithography

The advantage of a low voltage approach to e-beam lithography in resist materials is that a more spatially localized energy deposition can be achieved than with a focused high energy beam. As a result, proximity effects are virtually eliminated and enhanced resolution and superior pattern fidelity can be obtained. Proximal probes such as the STM or the atomic force microscope with a conductive tip, are convenient ways to realize such a low energy (<50 eV) electron beam with a diameter less than ten nanometers.

STM lithography results have been compared to lithography with a 50 kV e-beam tool which has a ~10 nm spot size. The exposure conditions for each tool were optimized but otherwise the resist films were prepared and processed identically. With the STM, smaller feature sizes and narrower pitch gratings are possible than by exposure with the 50 kV e-beam. In addition, STM lithography has a far greater process latitude, i.e., the sensitivity of feature size to incident dose is far less than with the 50 kV electrons.[5]

Feature Placement

The chief problem for e-beam nanolithography is not resolution but the precision with which a feature can be positioned, i.e., pattern placement. To put the requirements of pattern placement in perspective, the accuracy with which a feature must be placed on a work piece is typically required to be less than 15% of the minimum feature size. Thus for 50 nm features, a precision of 8 nm or ~22 atomic spacings is required. In current practice, the workpiece is mounted on a precision stage which is moved under interferometric control. The distortions of the e-beam deflection system are corrected by scanning precise calibration grids. The actual lithographic writing is performed by a process of dead reckoning assuming that the distortion calibration and stage positioning are exact. In practice this is not the case. Drift of the e-beam due to charging, inaccuracies in the correction of deflection distortions, turbulence in the interferometric path and distortions of the interferometer mirrors are just some of the issues that limit placement precision. Recently, Professor Henry Smith at MIT suggested that the workpiece itself incorporate a fiducial pattern so the position of the e-beam relative to the workpiece can be measured during the lithographic patterning.[6]

We have concentrated on the problem of pattern placement during e-beam lithography of membrane masks of the type currently envisioned for proximity x-ray and projection e-beam lithographies. During patterning, the majority of the electrons are transmitted through the membrane. So the position of the electron beam incident on the membrane can be measured with an electron detector placed immediately behind the membrane. As a detector, we have designed a reverse biased Schottky diode incorporating a fiducial grid in the form of a patterned absorber on the diode surface. A reverse bias current is induced by the energy deposited by the incident electron beam. This energy (and hence diode current) is reduced where the electron beam first passes through the absorber on the diode surface. Thus the diode current is modulated when the beam is scanned over the membrane/detector assembly. Using Fourier transform techniques one can then interpolate the position of the beam within the period of the patterned absorber layer.

Acknowledgments

We wish to acknowledge the support of the Office of Naval Research and the Defense Advanced Research Projects Agency. This work was performed in collaboration with colleagues at NRL, notably S.L. Brandow, J.M. Calvert, P.M. Campbell, E.A. Dobisz, F.K. Perkins and E.S. Snow.

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Prediction of Latchup Immunity of High Energy Ion Implanted CMOS Twin Well (Retrograde/BILLI/BL) Structures

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This paper describes how a properly calibrated simulation methodology could be used to investigate the latchup immunity characteristics among the various high energy ion implanted CMOS twin well (Retrograde/BILLI/BL) structures. To obtain the accurate quantitative simulation analysis of retrograde well, a global tuning procedure and a set of grid specifications for simulation accuracy and computational efficiency are carried out. The latchup characteristics of BILLI and BL structures as a function of layout spacing is well predicted by applying a calibrated simulation methodology for retrograde well. By exploring the potential contours and current flow lines at the holding condition, we have observed that the holding voltage of BL structure is more sensitive to the layout spacing (p+ to well edge space /n+ to well edge space) than to the retrograde well itself.

1.0 Introduction

With shrinking design rules to accommodate denser and faster circuits, optimization of latchup related to layout spacing and design of well profiles become more difficult. Informations such as the sensitivity of the triggering and holding condition to variations in the diffusion-to-well spacing and well structure cannot be easily obtained, reflecting the complicated nature of latchup [1]. The newly used high-energy ion-implanted well process has improved latchup immunity substantially; however, as lateral design rules shrink, its advantage becomes more subtle and requires sophisticated analysis for optimization.

In this study, we provide a properly calibrated simulation methodology that can be used to predict the latchup immunity characteristics of various high energy ion implanted CMOS twin well structures such as retrograde, BILLI(Buried Implanted Layer for Lateral Isolation), and BL(Buried Layer) structures. Our analysis is based on using two dimensional process simulator TSUPREM-4 [2] and device simulator MEDICI [3].

2.0 Experiments

The well structures used in this work were fabricated on (100) 9~12 Ω-cm, p-type Si wafers with 90 Å gate oxide. Retrograde p-well and n-well were formed after LOCOS isolation. The p-well implants were introduced by B at 500keV of a dose 3e13cm^{-2} and at 180keV of 4e12cm^{-2} respectively, and n-well implants by Ph at 800keV of 3e13cm^{-2} and 300keV of 4e12cm^{-2} respectively. BILLI well was formed through thick photoresist during the normal p-well masking step. B of 2MeV, 1.45MeV, and 1.1MeV with the same projected range as retrograde, were implanted in the p-well and buried p-layer under the n-well region. BL well was formed through B of 1.6MeV blanket implantation which means without masking step. The heat cycles after well implants were at 1000 ℃ for 30min.

The pnpn test structures were used for each MOSFET in the n-well and p-substrate. The distance between the n-well contact ant the p+ active in the n-well was fixed at 10.5um and the width of the structures at 100um. One of key layout design parameters, n+/p+ (p+ to well edge space/n+ to well edge space), was

varied with values of 3.5/4.5um, 2.4/2.4um, 1.8/1.8um and 1.2/1.2um. The parasitic bipolar current gains (β npn, β pnp) and the n+ and p+ injected latchup triggering, holding characteristics were investigated.

3.0 Simulations

The latchup simulations were observed to be strongly sensitive to grid, and it was necessary to optimize the grid for accurate and reliable simulations. Simulation accuracy requires the maximum number of grid points to be allocated in a simulation structure, on the other hand, computational efficiency requires the minimum number of grid points.

Figure 1 shows the test structure of grid specifications. The relative simulation error normalized with results of grid split condition (#8) for triggering and holding points (V_{trig}, I_{trig}, V_h, and I_h) is shown in Figure 2. With the view point of computational efficiency, the relative CPU time required to simulate the breakdown and triggering voltage is also compared as shown in Figure 2. From the results, we have set the grid specifications in such a way that the lateral grid spacing of 200 Å is necessary for region A, B, C, E and 250 ~ 500 Å for region D.

4.0 Results and Discussion

The models such as carrier-carrier scattering-, concentration-, and field- dependent mobility, Shockley-Read-Hall-, Auger recombination, bandgap narrowing, etc., have been considered and their default parameters were calibrated to match the latchup characteristics measured from retrograde well structure.

Figure 3 compares the measured and simulated latchup I-V characteristics under the condition of p+ and n+ triggering mode for retrograde well with the n+/p+ spacing of 8um and 2.4um, respectively. A comparison between measured and simulated parasitic bipolar current gains, β npn and β pnp as a function of collector current is also shown in Figure 4 for a n+/p+ spacing of 8um. It can be seen that a close correlation is observed between the measured and the simulated results.

Figure 5 shows that, when the calibrated latchup simulation models for retrograde well is applied to BILLI and BL, the simulated parasitic bipolar current gain, p+ and n+ injected triggering voltage and holding voltage as a function of layout spacing are well predicted against the measured values. It is seen that the holding voltage of BL is more sensitive to the influence of layout spacing than that of retrograde well. To understand this relative sensitivity of the holding voltage to layout spacing, the potential contours and current flow lines were investigated as shown in Figure 6 and 7. In case of retrograde well with 8um spacing, the current flow lines spread deeper into the bulk region and the length of flow lines increases. However, when the spacing is reduced to 2.4um, the flow lines are closely spaced under the field region. This reduction of current spreading in the bulk region indicates that the fractional increase of the electrical spreading resistance associated with the flowlines does not decrease and causes less influence of holding voltage. For BL case, the current spreading in the bulk region does not decrease as the spacing is reduced. This results in the increase of the spreading resistance and the subsequent reduction of holding voltage.

5.0 Conclusions

The good prediction of latchup immunity in BILLI and BL has been achieved using a properly calibrated simulation models for retrograde well. We have also explained the physical understanding of holding voltage sensitivity to the layout spacing between retrograde well and BL. The appication of simulations for latchup characteristics obtained through this study can be utilized to optimize latchup hardness as well as to determine the process/device design windows for latchup sensitivity.

6.0 References

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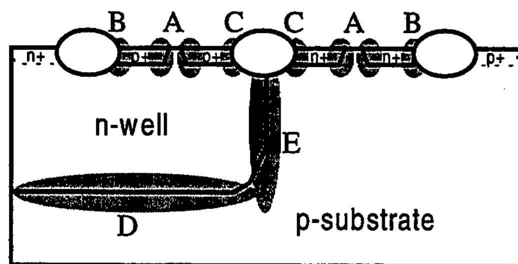


Grid split	A	B	C	D	E
1	200 Å	200 Å	200 Å	500 Å	200 Å
2	100 Å	200 Å	200 Å	500 Å	200 Å
3	100 Å	200 Å	200 Å	500 Å	100 Å
4	100 Å	100 Å	200 Å	500 Å	200 Å
5	50 Å	200 Å	200 Å	500 Å	200 Å
6	100 Å	100 Å	200 Å	250 Å	200 Å
7	50 Å	50 Å	200 Å	500 Å	200 Å
8	50 Å	100 Å	200 Å	250 Å	100 Å

Figure 1. Latchup structure of grid specifications.

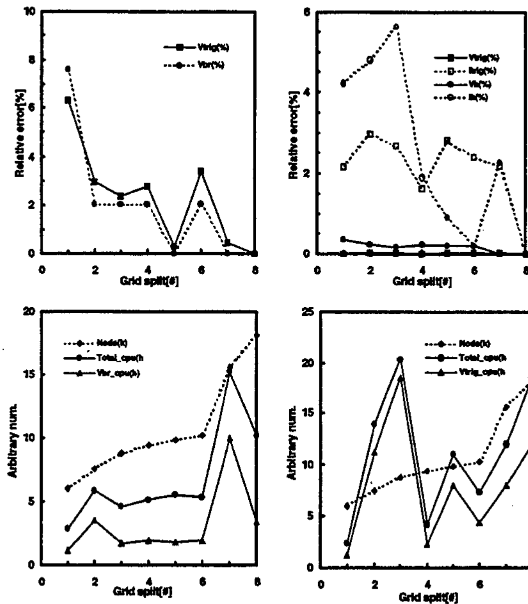
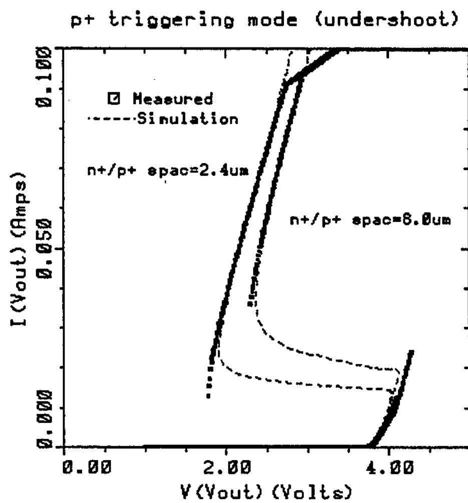


Figure 2. Simulation results of grid sensitivity.



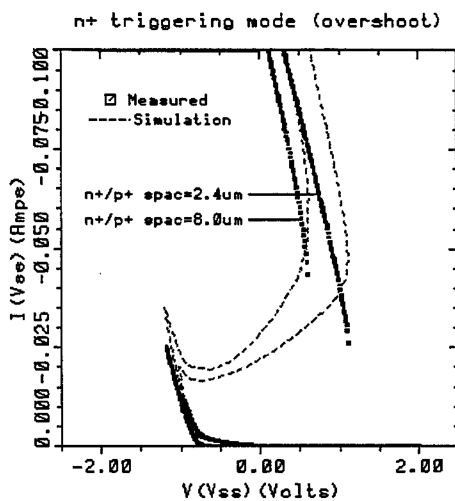
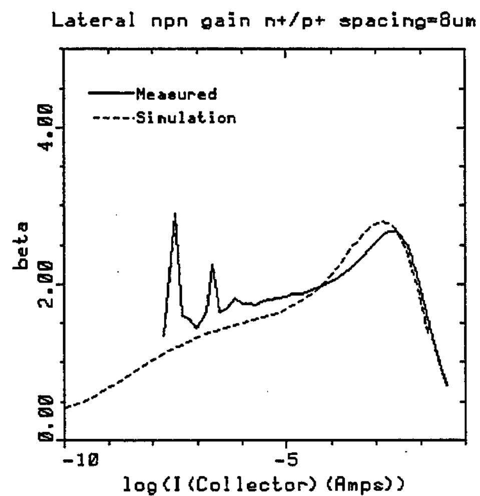


Figure 3. Comparison between measured and simulated latchup I-V characteristics of retrograde well structure.



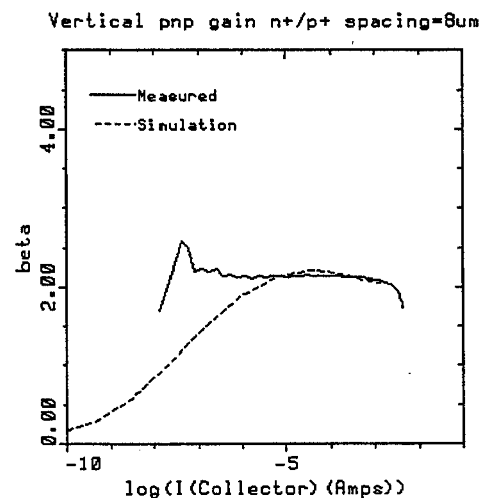


Figure 4. Comparison between measured and simulated β npn, β pnp vs. I(collector) of retrograde well structure.

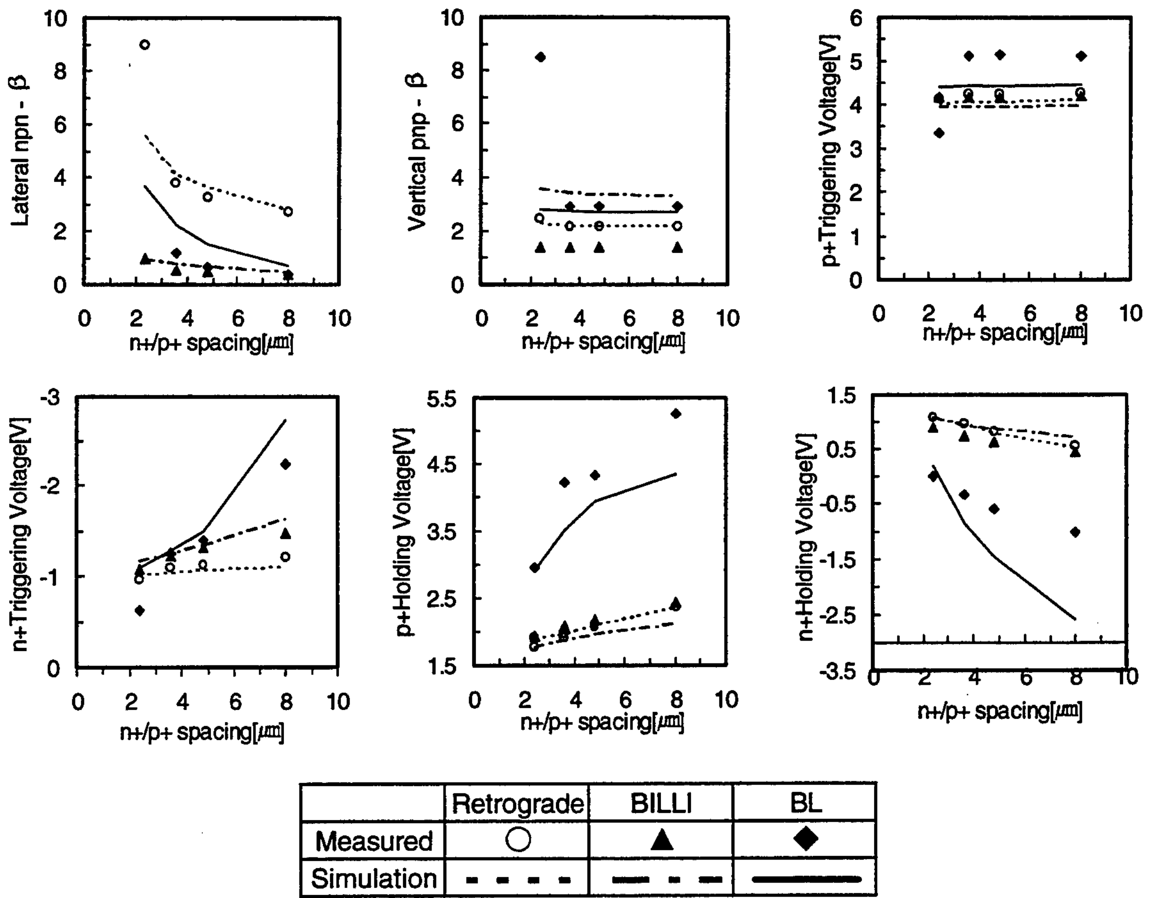


Figure 5. The comparison of measured and simulated β pnp, β npn, p+ and n+ injected triggering and holding voltage as a function of layout spacing.

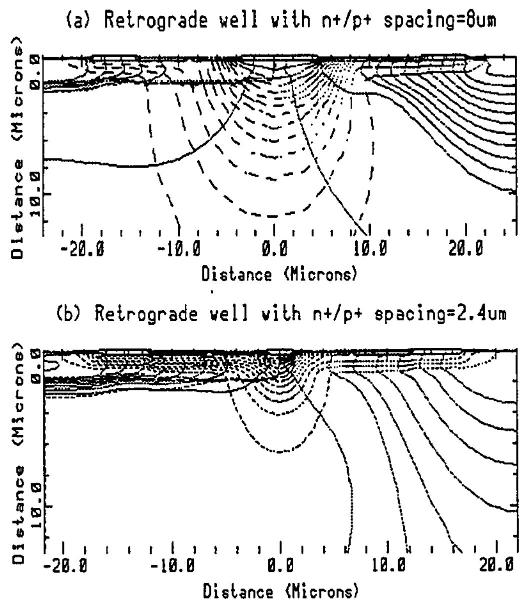


Figure. 6 Potential contours (continuos lines) and current flow lines (dashed lines) at holding point for retrograde well with (a) 8um and (b) 2.4um spacing.

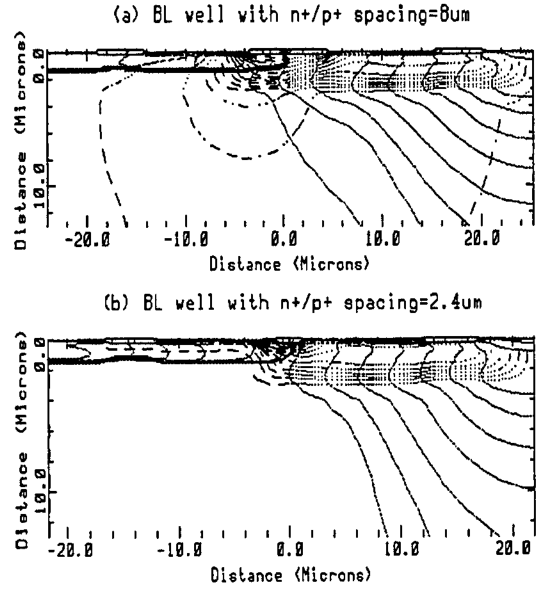


Figure. 7 Potential contours (continuos lines) and current flow lines (dashed lines) at holding point for BL well with (a) 8um and (b) 2.4um spacing.

Designing Compliant Substrates

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Experimental evidence has shown that it is possible to epitaxially deposit relatively high-misfit materials on thin compliant substrates without the generation of dislocations in the growing layer. This observation is in sharp contrast to the results from experiments in which the same high-misfit materials are grown to thicknesses exceeding the critical thickness on the same substrate material as the compliant substrate but in bulk form. The mechanisms by which these thin substrates avoid the generation of dislocations in the epitaxial deposits is not clearly understood, but experimentally there are several characteristics of the compliant substrate which lead to the desired result of high perfection in the epi-layer. The main characteristics are thinness of the compliant substrate and a high angle of misalignment between the compliant substrate and its underlying, bulk substrate. A Cornell group demonstrated proof-of-principal that a thin single crystal film of GaAs when twist-wafer bonded to a bulk single crystal substrate of GaAs will comply to the lattice constant of an epitaxially deposited layer of InGaP which has a 1% misfit with GaAs. The twist angle was nine degrees or higher. An earlier approach to designing compliant substrates was investigated by the same group using a free-standing thin substrate of GaAs. The free-standing layer was 60 nm thick; the twist-wafer bonded compliant substrate was 10 nm thick. Two design criteria were proposed by this group. First, the membranes are loosely bonded to, or released from, the material underneath; and second, the membranes are very thin. The fragility and non-planarity of the free-standing compliant substrates were cited as difficulties. By wafer bonding the epitaxial layer with a twist to the bulk substrate, the problem of fragility and planarity both are eliminated. It is the twist-wafer bonded compliant substrates that are addressed in the present paper.

The concept of a critical thickness above which it becomes energetically favorable to generate misfit dislocations at the substrate-epi-layer interface is valid for compliant substrates, whether free-standing or twist-wafer bonded. There is an additional interface to consider in the case of the twist-wafer bonded substrate. For a fixed misfit between epi-layer and compliant substrate, the stronger the bonding between bulk substrate and compliant substrate, the smaller the critical thickness. The interface between the compliant substrate and the bulk substrate of the same material will contain an array of screw dislocations whose number density increases with angle of twist. If the angle of twist is high the cores of the screw dislocations can overlap. Such a condition would likely correspond to decreased bonding between compliant substrate and bulk substrate thereby permitting the thin substrate layer greater freedom to change its lattice parameter when an epitaxial layer is deposited on it. Coincidence angles of twist should be avoided

as they likely increase the difficulty for the compliant substrate to adjust to the epi-layer. If the compliant substrate has a thickness below the critical thickness then it should deform to accommodate the misfit rather than the epi-layer deforming to accommodate the misfit. The calculation of the critical thickness will be modified from that of a free-standing bi-crystal (compliant substrate plus epi-layer) according to the nature of the twist-wafer bonding, however, in principle, the design criterion should be to select a compliant substrate whose thickness is below the critical thickness. This design may not be practical when the critical thickness is very small (say below 1 nm). Also, there will be handling difficulties and surface smoothness criteria that may set the minimum thickness of the compliant substrate to a value near several nm. Growing the epitaxial compliant substrate layer in a Volmer-Weber island mode should be avoided.

The remaining design characteristic of the twist-wafer bonded compliant substrate is the role of the array of pure screw dislocations in accommodating misfit. The idea is that the lattice parameter of the compliant substrate changes to match that of the epitaxial layer grown on it. In this way the lattice parameter of the compliant substrate matches that of the epi-layer thereby eliminating the need to generate misfit dislocations through a glide process in the epi-layer which leaves threading dislocations in the epi-layer. The interface between the epi-layer and the compliant substrate remains coherent. Following this idea, the change of lattice parameter in the compliant substrate changes the nature of the array of screw dislocations in the interface between the bulk substrate and the compliant substrate so that they are no longer pure screw dislocations but have an edge component as well as a screw component. The array of pure screw dislocations has become an array of mixed character dislocations in which the screw component of the Burgers vector accommodates the imposed twist and the edge component of the Burgers vector accommodates the lattice parameter misfit that now exists between the bulk substrate and the compliant substrate. The mechanism by which this happens has not been determined but there are two reasonable possibilities. In both cases the array of pure screw dislocations simply rotates the orientation of the dislocation line directions in the plane of the interface while maintaining the line directions of the dislocations along two orthogonal directions that are no longer <110>. This reorientation of the dislocation axes results in the Burgers vectors no longer being parallel to the dislocation axes so that the dislocations are of mixed character.

The first possibility is that the initial array of screw dislocations remains fixed in number in which case the reorientation of the line direction of the dislocation axes causes a change in the twist angle between the compliant substrate and the bulk substrate. The second possibility is that the twist angle remains constant curing the reorientation of the compliant substrate in which case the number density of dislocations would change. As this latter case requires the generation of new dislocations which may result in the generation of threading dislocations, the former possibility may be the one that preferentially operates.

In the presentation of this work, the details of the mechanisms for misfit accommodation by compliant substrates will be discussed in some detail.

Fabrication of a Novel Oxygen Sensor with CMOS Compatible Processes

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Abstract—**A novel miniature dissolved oxygen sensor as a transducer for medical and environmental measurements is fabricated with a CMOS compatible process. The sensor is designed as a three electrode system. It has a Pt recessed ultramicroelectrode array structure as working electrode, a Pt counter electrode and a Ag/AgCl reference electrode. The recessed ultramicroelectrode array is made with a lift-off method which follows a SiO_2 reactive ion etching process. Different recessed ultramicroelectrode arrays varying in diameter and spacing have been designed to study the diffusion characteristic in order to find the optimal values. The chip size is 1.5×4 mm^2, small enough to enable implantation.**

1. Introduction

DISSOLVED oxygen measurement is important for medical, chemical and environment analysis. Electrochemical oxygen sensors have shown to be a powerful tool for this measurement. Microelectronic fabrication technology made a considerable impact on the development of miniaturized electrochemical sensors. With this technology not only the sensor can be miniaturized, but also it can be made at a low price through mass production. This tremendous features make it very suitable for the usage in the biomedical field, in which the small size of the sensors enables an implantation in tissues. It can be also used as a transducer for environmental analyses that are based on the measurement of oxygen like BOD-sensors [1].

For the actual application, the electrode should have a negligible dependence on the flow-speed of a system in order to get a stable signal for the measured species in a short time. Traditional electrochemical oxygen sensors use macroelectrodes, their output signal will be disturbed due to the flow-stirring effect. In contrast, microelectrodes can reduce this effect because the smaller size electrode has only a shorter diffusion field [2,3]. Microelectrodes also have many other advantages such as fast response time, excellent signal-to-noise characteristics and high current-densities [4]. Recently several kinds of Clark-type oxygen sensors have been successfully fabricated with microelectronic technology [5,6,7]. However, because of shortcomings with the stability and the lifetime of the sensor made with thin-film technology there are still no dissolved oxygen microsensors available for the *in vivo* biomedical application.

To optimize the stability of their oxygen sensor, Y. Chen and G. Li established a new model with a recessed electrode array [8]. Recessed electrode arrays show a different diffusion characteristic leading to a further decrease of the flow error [9]. Through the proper choice of the ratio of the diameter to the depth of the recessed hole a good compromise between flow dependence, response time and sensitivity can be found. This paper presents a set of CMOS compatible processes used in fabrication of a recessed ultramicroelectrode array. The characteristics of the recessed ultramicroelectrode array have been determined and are also discussed in the following.

2. The Design and Fabrication

Due to the advantages of a three electrodes configuration, we designed the oxygen sensor having three electrodes. Twelve kinds of dissolved oxygen sensors differing in the dimensions of the ultramicroelectrode array structures are composed on a 8mm×9mm die chip. These different ultramicroelectrode array structures are designed to study the relationship between the sensor characteristics and the array structure. Each

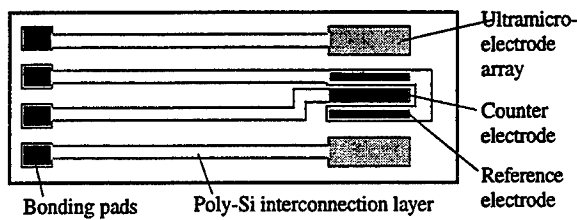

Fig. 1. Schematic set-up of the oxygen sensor.

electrode has the dimensions 1.5mm×4 mm which allows it to be put into an implantable catheter used in the biomedical field. Fig. 1 shows the basic sensor design, it has two identical ultramicroelectrode arrays (working electrodes), two Ag/AgCl reference electrodes, and one counter electrode in the center, both in long strip shape. The two reference electrodes are connected together in the interior of the chip. The reason for having 2 working electrodes is because it allows the simultaneous detection of 2 parameters in the biomedical field or the extension of the lifetime if the electrodes are used successively. The two working electrodes can also be used to measure the conductivity of the solution by switching them to a conductance measurement circuit.

We have developed a set of CMOS compatible processes used for the fabrication of the recessed ultramicroelectrode array. The details of the process flow are as follows: (1) Forming of the interconnection layer. We first used a field oxide process to grow 5000Å of SiO_2 as insulating layer on the silicon substrate. After that we used CVD to deposit a 3000Å poly silicon layer which was heavily doped with phosphorus for interconnection between the electrodes and the bonding pad. After using the first mask for the lithography we did a plasma dry etch process to pattern the doped poly silicon layer. (2) Forming of a thick insulation layer and a passivation layer. We used a LTO process to deposit about 4μm of SiO_2 on the surface of the poly-Si interconnection layer and then deposited 1500Å of silicon nitride used as a passivation layer (Fig. 2a). (3) Forming of the electrode cavity structure in the thick insulation layer. We used the second mask in the lithographic process to pattern the openings of the three electrodes. In the lithographic process it was important to choose the proper thickness of the photoresist, because it was necessary using a dry etch process to etch the thick SiO_2 layer in order to form a vertical sidewall of the cavity, which was very time consuming. If the photoresist is thin the remained thickness after etching may be too thin to do the metal lift-off process afterwards. On the other hand, if the photoresist is too thick it will be difficult to get the smaller size openings (2μm) made in the lithographic process. We chose a special type of photoresist achieving 3~4μm average thickness in our process. Before etching the thick SiO_2 layer, we first used plasma dry etch to remove the silicon nitride layer. For the SiO_2 etching process we used reactive ion etching (RIE) in order to get steep vertical sidewalls in the cavity. This step is important for the fabrication of the electrodes, optimized etching conditions should be

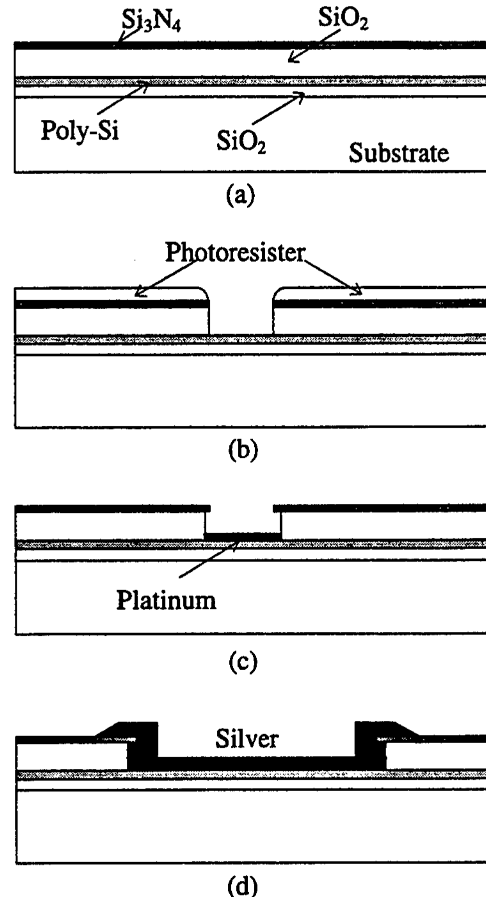

Fig. 2. Simplified fabrication processes.

chosen to obtain a suitable selectivity and fast etching rate for the SiO_2. With our conditions, a 5.0 selectivity and 370Å /min SiO_2 etch rate was achieved. For a 4μm SiO_2 thickness, the total etching time was 120min including 10min over-etching to overcome the deviation from the uniformity on the wafer scale (Fig2b). (4) Lift-off process. After the SiO_2 RIE process, the left photoresist has about 2~3 μm thickness. In order to

obtain a better lift-off effect, we used a method similar to the oxide- assisted lift-off method [10] and 2min wet etching in a buffered oxide etchant (HF/NH_4F=1:6) to form about 0.3µm undercut beneath the nitride layer. Then we used sputtering to form the metal electrodes. The target material was platinum, the thickness 1500Å. Between the metal electrodes and the poly-Si interconnection layer, a 500Å titanium- layer is sputtered as adhesion layer. After the metal deposition, the wafer is soaked in acetone to dissolve the photoresist and to lift-off the metal with ultrasonic agitation (Fig2c). (5) Lift-off process for the silver electrode. We used a third mask to define the opening of the silver electrodes with normal lift-off lithography. After the lithography, a Ti/Pd/Ag (500Å /500Å /8000Å) metal multilayer is sputtered on the wafer. The titanium and palladium layers serve as adhesion layers [10]. Then the wafer is put into acetone for dissolving the photoresist and the lift-off of the metal according to step (4) (Fig2d). (6) As the last step the wafer is diced into single dies. The SEM picture of the cross-section of the ultramicroelectrodes is shown in Fig 3.

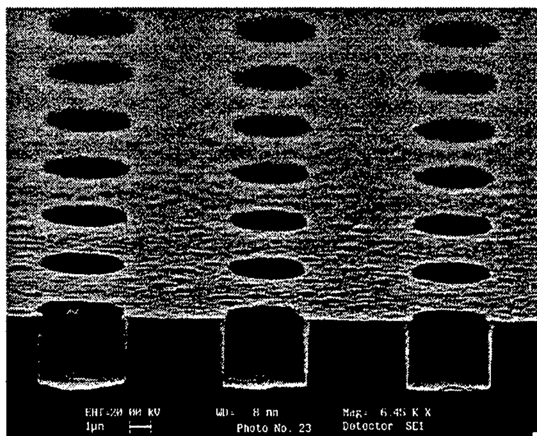

Fig. 3. SEM picture of Pt recessed ultramicro-electrode array.

Before the measurement the sensor die is mounted onto a specially designed PCB with epoxy glue and the chip electrode is connected to the PCB using wedge bonding. Then the pads and the bonding wires were also covered with epoxy.

3. Results

Electrodes with 12 different working electrode arrays have been produced (Tab. 1.).

no.	Ø [µm]	Spacing [µm]	Array
1	2	6	26 x 79
2	2	8	26 x 79
3	2	8	14 x 40
4	2	16	14 x 40
5	3	9	18 x 53
6	3	12	18 x 53
7	3	12	9 x 27
8	3	24	9 x 27
9	4	12	14 x 40
10	4	16	14 x 40
11	4	16	7 x 20
12	4	32	7 x 20

Tab. 1. Dimensions of the arrays.

The linear sweep voltammograms in Fig. 4 show clearly visible oxygen reduction plateaus. Arrays 1 to 4 have the same diameter of the single electrodes but differ in their distance (6µm, 8µm, 8µm and 16µm) and their geometry (26 x 79, 26 x 79,14 x 40, 14 x 40) It was found that the length of this reduction plateau decreases with the increase of the distance between the single electrodes in the array.

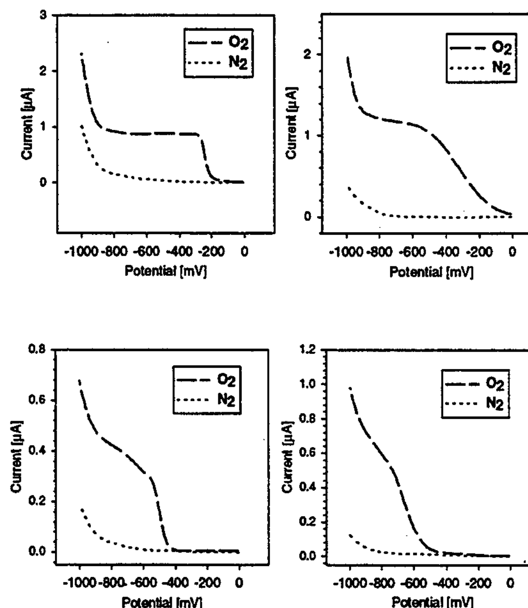

Fig. 4. Linear sweep voltammograms at 100 mV/s of arrays 1 to 4.

An increase in the current due to an increase in the distance between the single electrodes indicates that the diffusion fields were still overlapping at

the array with the smaller spacing. Since this has been the case with all recessed arrays we came to the conclusion that a further increase of the spacing is necessary.

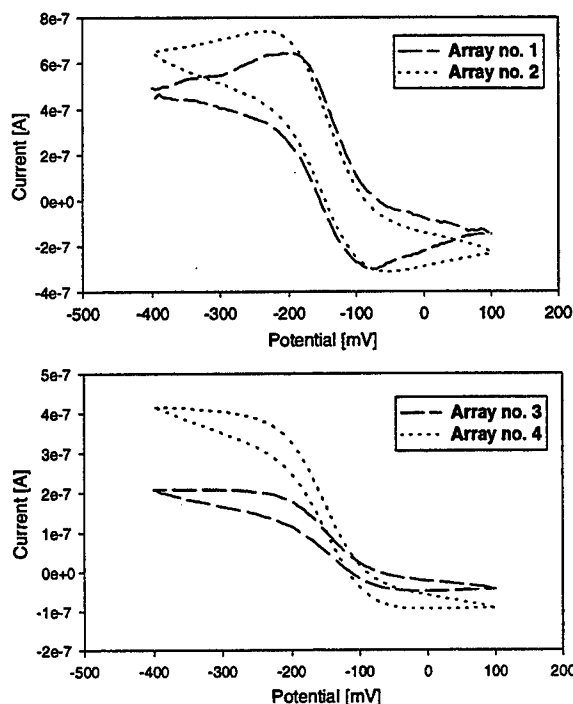

Fig. 5. Cyclovoltammograms at 100 mV/s of arrays 1 to 4 in 0.1 M KCl / 5 mM $Ru[(NH_3)_6]Cl_3$.

With increasing distance of the electrodes a gradual transition from a peak-shaped cyclovoltammogram to a sigmoidal one is visible indicating a change from a diffusion controlled to a kinetically controlled electrode process [11]. The voltammetric characteristic of array 4 shows steady-state current behavior meaning that the spacing between the single electrodes is sufficient to allow independent diffusion fields [12, 13].

The stirring effect was found to be much smaller with the recessed array. The flow-dependence was measured for a commercial Pt-electrode (BAS analytical systems) and the arrays using a magnetic stirrer . While the signal increase for the macroelectrode was found to be 620 % the increase for the arrays varied between 28 and 80 % depending on the spacing to diameter ratio.

4. CONCLUSION

A novel oxygen sensor with a Pt recessed ultramicroelectrode array has been fabricated with a CMOS compatible process. The process uses only three masks. The developed oxygen sensors based on the recessed ultramicroelectrode array have all the advantages of single microelectrodes while having a higher current. The smaller dependence on the flow makes them more suitable for the application in the *in vivo* monitoring of blood oxygen concentrations as well as for measurements in the environmental field.

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Magnetoelectronic Memory: Design and Processing Issues

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Abstract -- We present the design of a CPP-GMR magnetoelectronic memory and discuss the processing issues involved in it's realization. The steps include damascene processing of a buried Cu word line, ion-beam milling of metals using silicon nitride as an etch mask, and nitride chemical-mechanical polishing to produce ultra-low contact resistance between Cu-Cu interfaces.

I. INTRODUCTION

Discoveries in the late 1980's of the giant magnetoresistance effect [1] have spawned new approaches in the development of magnetoelectronic sensors and memory . For memory, the effort to marry the non-volatility of magnetic materials with electronic devices is driven by the need for robust systems that operate at low power and high density, with radiation-hardness, high-speed and mechanical rigidity. The potential applications are wide-ranging and include satellite systems, computers for military and commercial aircraft, and portable electronics such as laptop computers, digital cameras and cellular phones. Types of magnetoelectronic memory currently in use include magnetic bubble memory and AMR-based magnetic RAM. Magnetic multilayers showing giant magnetoresistance typically demonstrate room temperature resistance changes near ~10% -- a factor of three beyond previous signal levels. As expected, the added signal can be translated into higher capacity memory. Although work has been reported on developing nonvolatile memory based upon current-in-plane (CIP) GMR [2] and spin-polarized tunneling [3], this paper will focus on the design and processing issues required to implement the random-access memory we are pursuing at the Naval Research Laboratory -- CPP-GMR memory.

II. CPP-GMR MEMORY

Current Perpendicular-to-Plane Giant MagnetoResistance, CPP-GMR for short, contrasts with the more typical current-in-plane configuration for sensing giant magnetoresistance. As the label indicates, CPP-GMR is realized by passing current in the direction normal to the multilayer plane and takes advantage of the enhanced values of GMR that are measured in the CPP geometry. Gijs, et al [4] found CPP measurements on Fe/Cr multilayers to give nearly double the GMR values of CIP devices. The CPP approach is complicated , however, by the requirement of sensing the voltage across the thickness of a magnetic multilayer -- a value typically between 100 - 200 nm. It is, however, a promising method to pursue as the thin-nature of the films drives the requirement to produce smaller devices, which in turn plays to the need for high density.

Our approach to CPP-GMR is shown in Fig. 1. The diagram shows the metal layers of a magnetoelectronic memory consisting of a pair of buried word lines and an orthogonal set

of sense and bit lines. The bit, sense and word lines are electrically isolated from each other by an interlayer dielectric. The sense line is constructed of three layers, a copper bottom terminal (BT), a magnetoresistive layer (MR) composed of a [NiFeCo/Cu/CoFe/Cu]xN magnetic multilayer, and a copper top terminal (TT). These layers interconnect in a vertical serpentine pattern with one storage element composed of two MR stacks. The word (M1) and bit (M4) lines are made of copper and are pulsed appropriately to provide switching fields for the magnetic element. In the simplest mode of operation the switching fields rotate the soft layer (NiFeCo) to parallel or antiparallel directions relative to the hard magnetic layer (CoFe).

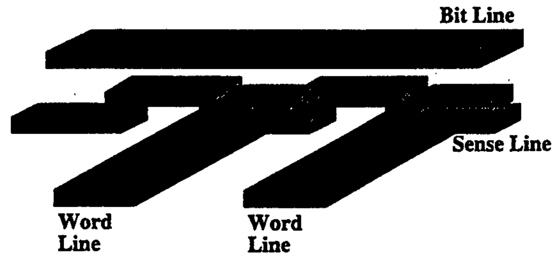

Fig. 1. Outline of the basic memory cell showing two GMR stacks per addressable cell.

A voltage is developed across the magnetoresistive stack by a current running the length of the sense line. The MR signal derives from the low resistance stack and must overcome the resistance of the BT and TT copper leads, forcing us to measure the voltage as near to the magnetic stack as possible. Our approach is to implement a Kelvin measurement as shown in Fig. 2. (The metal word and bit lines are removed for clarity.) As shown, we couple the ends of a storage element located along a central sense line to neighboring sense lines through Si FET's. For example, a current running the length of SL2, along with the activation of the transistors driven by PWL2 and PWL3, select a unique magnetic storage element consisting of 2 magnetic stacks.

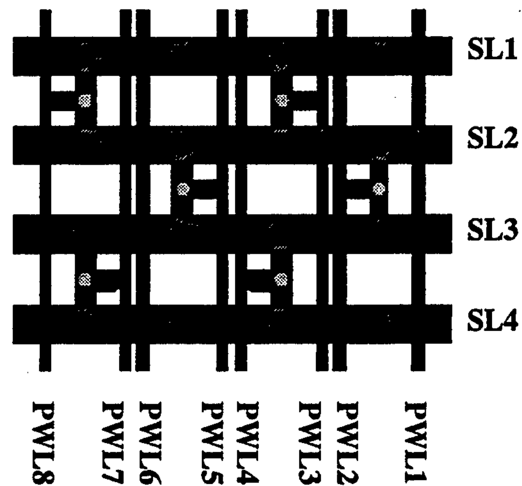

Fig. 2. Top view of CPP-GMR memory showing important components of the underlying electronics.

The voltage developed across the magnetic storage element propagates the length of the neighboring sense lines and is ported to a sense amplifier at the end of the sense line for conversion to standard levels.

III. METAL-LEVELS PROCESSING

We now turn to a description of the processing techniques used in successfully constructing the buried word line (M1), the bottom terminal (BT), magnetoresistive element (MR), top terminal (TT), and the bit line (M4). Processing steps were completed at the Naval Research Laboratory with the exception of depostion of the Cu/magnetic multilayer/Cu stack, which was performed at Nonvolatile Electronics.

A. Damascene Processing of M1 Word Line

Fig. 3 illustrates the steps used in patterning the buried M1 word line beginning with a 3" (001) Si wafer coated with 75 nm of native oxide and 200 nm of LPCVD nitride. The oxide is used in conjunction with standard photolithography and RIE as an etch stop to define a nitride trench following the work of [5]. We also found our processing control adequate to reliably stop at 200 nm trench depth using SF_6/O_2 chemistry. The wafers were subsequently stripped of photoresist and placed in a metals sputtering system for 4 nm Ta/400 nm Cu deposition . Ta is used as an adhesion layer. The resulting wafer is dipped in a room temperature, 0.4% solution of benzotriazole (BTA) in DI water to passivate the copper.

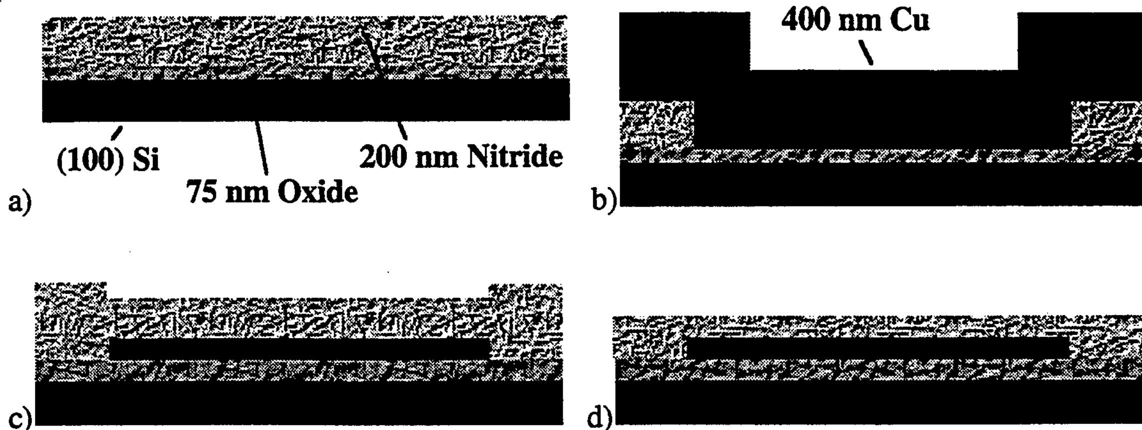

Fig. 3. Damascene processing of wafers for buried M1 word line showing a) starting wafer, b) after lithography/RIE/Ta-Cu deposition, c) after nitride deposition, d) after final nitride planarization.

The wafer is chem-mechanically polished using Rodel QTT 1010 slurry and a 12 inch Rodel IC-1400 pad at 4.8 psi and 48 RPM for both the pad and sample. After removal from the wheel the wafer is again dipped in 0.4% BTA and manually scrubbed with a sponge and DI water. The polish rate under these conditions is 180 nm/min and 10 μm lines were found to dish by 40 - 60 nm. A 600 nm reactively sputtered silicon nitride was then deposited to coat the M1 level. The resulting topography was polished back using CMP having identical conditions as above but for the use of Cabot SS-25 slurry diluted in a 1.5:1 ratio with DI water. Topography was reduced to 5 nm or less.

B. Magnetic Device Definition

Following the damascene steps to build in the buried M1 word line we deposit a 150 nm nitride/4 nm Ta/ 150 nm Cu/Magnetic Multilayer/ 150 nm Cu/ 200 nm nitride. Wafers subjected to e-beam lithography are also capped with 30 nm of W. The copper will become the BT and TT levels of the sense line after patterning. The magnetic multilayer is composed typically of (1.2 nm NiFeCo/5 nm Cu/1.1 nm CoFe/5 nm Cu)x8. The soft layer is an alloy of 65% Ni-15% Fe-20% Co and is used over standard 80% Ni-20% Fe permalloy to enhance the spin polarization and GMR. The hard layer is 95% Co-5% Fe alloy that enhances stability of the fcc phase over the hcp phase of pure Co. All materials are RF triode sputtered in UHP argon with base system pressure below 1.5×10^{-7} Torr.

The nitride cap is provided to protect the top copper layer and also to provide the first layer etch-mask. Our process utilizes nitride as an inorganic mask for ion-beam etching (IBE) of the metals. Such an approach allows fine device definition -- down to 0.4 μm -- and

prevents exposure of the photoresist to the ion-milling step. Our experience has shown it impossible to remove IBE-hardened photoresist in a manner that prevents degration of the exposed copper and transition metals in subsequent p/r strips. Photoresist strip solutions including TMAH were found to corrode exposed copper; plasma-ashing the resist produced similar results.

A typical layer cycle begins with photolithographic patterning using AZ 5209 photoresist, exposure using a Karl Suss MJB-3 with mid-UV optics, and development in 1:1 AZ Developer:DI H_2O followed by a 5% O_2/CF_4 RIE at 300V/30 mTorr. The copper serves as the RIE etch stop with no oxidation of the exposed copper visible. Line definition down to 0.4 μm is reliably achieved with careful monitoring of the nitride etch rate and resist exposure and develop times. Following removal from the RIE the sample is dipped in 0.4% BTA and the photoresist stripped in n-butyl acetate or acetone. Ion milling is performed using an 8 cm Commonwealth source running at 500V/150 mA and a distance of 13 inches. We utilize a mixture of 2.5% H_2 in Ar to prohibit edge-oxidation of the magnetic devices during the milling. We also limit the stage temperature to 130 C (maximum) by cycling the gun on and off. The final step in the basic cycle is to cap with 150 nm of reactively sputtered nitride that serves as an etch mask for the subsequent layer. This sequence is followed for the MR and BT layers. Following the BT IBE, a thick nitride is coated in preparation for the chem-mechanical polish to open the top copper layer of the device. CMP conditions are identical to the nitride polish discussed previously. We visually monitor several bond pads over the surface of the wafer to determine the CMP endpoint and verify the top copper is opened by dishing found using surface profilometry. The samples are dipped in BTA solution after each polish and cleaned with sponge and water when complete.

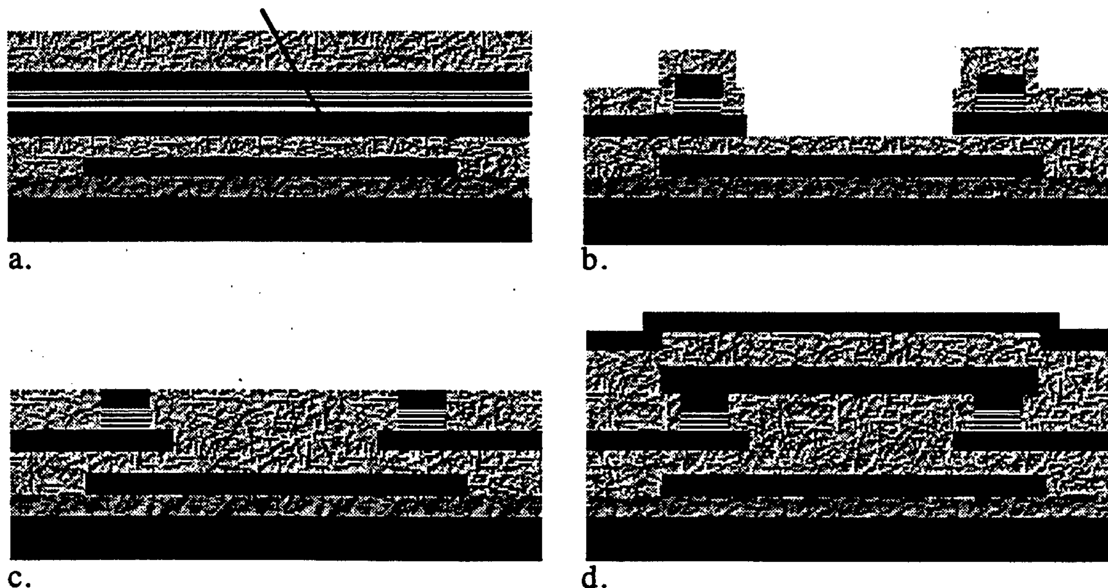

Fig. 4. Important steps in fabrication; a) starting wafer w/ magnetics, b) following MR litho/RIE/pr strip/IBE/nitride dep/BT litho/RIE/pr strip/IBE, c) following thick nitride dep/nitride CMP, d) following TT Cu & cap nitride dep/ TT litho/RIE/pr strip/TT IBE/ nitride, M4 Cu & cap nitride dep/ M4 litho/RIE/pr strip/IBE.

Following CMP the wafer is placed in a sputtering chamber, backsputtered using 2.5% H_2/Ar at 50V bias for eight minutes at a pressure of 3.0 mTorr, and capped with 150 nm Cu/150 nm silicon nitride. A hydrogen/argon mixture is used to reduce the oxides formed on the copper surface during CMP to copper metal, a necessary step to achieving low contact resistance. The standard lithographic cycle is repeated to define the TT layer, followed by a final deposition of 200 nm Cu and M4 lithography. Pad opening completes the construction of the device.

IV. SUMMARY

Rectangular structures ranging in size from 0.4 x 1.4 µm - 2.0 x 3.0 µm have been successfully constructed using the described process sequence. Chemical-mechanical polishing is used in planarazing topography detrimental to the magnetic performance of the storage elements and as part of the damascene process to produce the buried M1 word line. More critically , nitride CMP is used to provide a method of generating low contact resistance Cu-Cu contacts, demonstrated to show values below 5×10^{-10} Ω- cm^2. Lacking a reliable dry etch technology for the transition metals, ion beam etching is performed with silicon nitride as an etch mask. Future work will address further miniaturization using e-beam lithography and integration to underlying Si electronics.

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Novel Concepts in Quantum-Well Terahertz Emitters

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1. Introduction

The portion of the electromagnetic spectrum ranging from roughly one to several tens of THz is of interest in part because many molecules and solids have IR active rotational or vibrational resonances there; however, few convenient sources of coherent radiation in this regime exist. In particular, dynamical processes on the picosecond to subpicosecond timescale ocurring in this frequency regime have been difficult to access. Moreover, if one is to control processes in the THz regime, it will be necessary to generate experimenter specified shaped THz waveforms.

In this talk I review the physics of several standard semiconductor-based methods for the production of THz transients and why they are largely inadequate to meet the new needs. I then discuss physical mechanisms that hold the promise to circumvent difficulties with present-day methods. The two particular problems on which I focus are the requirement of obtaining THz transients in the tens of THz regime and the ability to generate shaped THz waveforms.

2. Generation of ~10 THz Transients

Several optically pumped THz emitters based on quantum-well-structures have been exploited to cover the range of sub-1 to 10 THz. These schemes typically lead to emission frequencies given by the bandwidth of the optical excitation pulse. Since for a transform-limited pulse the bandwidth is given by the inverse of the pulse duration, the upper end of this range is problemmatic since it requires 10 fs and even shorter pulses. Laboratory demonstrations have shown that using 10-fs pulses it is possible to produce narrowband picosecond 10 THz transients, but clearly this approach cannot be pushed much further since the optical cycle of the excitation pulses are in the 3 fs range. In any case, few researchers have access to 10-fs systems.

Clearly, what is required is a new physical mechanism for the generation of higher-frequency THz transients. One possibility, in which the foregoing bandwidth limitations do not apply, is to utilize multiphoton processes in the THz regime to upshift the emission energy. One particular process of this sort is well known from atomic physics, namely high-field harmonic generation.[1] Namely, subjecting atoms to intense pico- and femtosecond laser pulses yields a short burst of x-rays whose spectrum is composed of odd harmonics of the laser field to orders in excess of 100. High-field harmonic generation by atoms may be understood as a two-step process. First, the field ionizes the electron. Then, the ionized electron wavepacket in the field passes by the ion, generating a time-dependent dipole mo-

ment in turn giving the harmonic spectrum.[2] I have recently predicted that an analogous process in quantum wells can lead to picosecond transients containing significant emission in the tens of THz range.[3] This technique utilizes a quantum well in a cw ~1 THz field polarized in the plane of the quantum well. The quantum well is then optically excited by a ~100 fs optical pulse whose bandwidth spans both the lowest-lying exciton and the electron-hole continuum states. The coherent motion of the photoexcited wavepacket of electrons and hole driven by the low-frequency field results in a significant time-varying dipole moment with spectral components to a few tens of THz. The electromagnetic upshift is due to the interference between the exciton and the dynamically evolving continuum as it is driven by the field, and may be understood in terms of converting low-frequency driving-field photons via multiphoton absorption by the wavepacket into higher-frequency photons.

In the talk I will discuss the physical mechanism underlying this phenomenon and the expected limitations for the generation of electromagnetic transients.

3. THz Pulse Shaping

The technique outlined about will be of utility to carry out time-resolved spectroscopy in the far-infrared and we intend to explore the possibility of pushing this technique to the mid-infrared. One may turn this around and ask, how can we produce specially shaped THz waveforms in order to coherently control processes that occur in this spectral range? To date, little in the area of coherent control in the far- to mid-infrared has been achieved due to the difficulty in shaping THz waveforms. In this part of the talk I discuss one possible solution utilizing optical rectification in a dc-biased quantum well with shaped optical pulses. There are two basic problems to deal with. The first is that of achieving shaped THz waveforms. The second problem is to avoid saturating the quantum well with carriers when generating intense and long THz waveforms.

In particular, I illustrate these ideas with a theoretical exploration of how one can generate long and intense trains of ~1 THz quasi-half-cycle THz pulses at ~100 GHz repetition rates. Such pulse trains are of interest to drive ro-vibrational levels in molecules and solids toward some desired final state, can act to repetitively impact a system with an impulsive kick, or can act as a strobe.

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Influence of electron scattering on the current instability in a Ballistic Field Effect Transistor

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Summary

We consider the influence of scattering of carriers on the "shallow water wave" instability of surface plasma waves in a ballistic Field Effect Transistor. We show that scattering (which is analogous to friction in a shallow water channel) results in narrowing of the region of instability. Using an approximation analogous to the quasiclassical approach in quantum mechanics we calculate the instability increment and the critical value of the friction parameter at which the instability vanishes. The analytical results are in an excellent agreement with our computer simulations. Our calculation shows that this instability can be observed at room temperature in deep submicron devices and at cryogenic temperature in devices longer than one or two microns.

Introduction

Recently Dyakonov and Shur [1] described a mechanism of plasma wave generation in a ballistic Field Effect Transistor (FET). Neglecting carrier scattering, they showed that nonsymmetric boundary conditions with fixed voltage at the source and fixed current at the drain lead to the instability of stationary state with a dc current. The instability is a result of plasma wave amplification due to the reflection from the drain boundary of the device. As shown in Ref. 1, the 2D-electrons in a FET are described by equations which are similar to the hydrodynamic equations for shallow water, plasma waves corresponding to shallow water waves.

In this paper, we investigate the role of carrier scattering on the instability in the current carrying electron fluid. We find the instability increment for arbitrary currents and arbitrary electron momentum relaxation times. Since we use the hydrodynamic analogy, we refer to this scattering as to 'friction' of electronic fluid.

Instability Threshold

The electron fluid in a FET may be described[1] by the following equations, which are analogous to the hydrodynamic equations for shallow water:

$$\frac{\partial V}{\partial t}+\frac{\partial}{\partial x}\left(\frac{V^2}{2}+\frac{eU}{m}\right)+\frac{V}{\tau}=0 \qquad (1), \qquad \frac{\partial U}{\partial t}+\frac{\partial}{\partial x}(VU)=0 \qquad (2)$$

Here $U(x,t)=U_{gc}(x,t) - U_T$, U_{gc} is the local gate-to-channel voltage, U_T is the threshold voltage, $V(x,t)$ is the local velocity of the electron flow, m is the electron effective mass, τ is the momentum relaxation time due to collisions of electrons with phonons and (or) impurities. Eq.(1) coincides with the Euler equation for shallow water. The voltage swing U corresponds to the shallow water level. Eq.(2) is the continuity equation in which the Shockley gradual channel approximation[2] is taken into account.

As was shown in Ref.1 the steady electron flow is unstable under the following boundary conditions:

$$U(0,t)=U_s, \quad U(l,t)v(l,t)=j/C \quad , \qquad (3)$$

where U_s is the fixed potential at the source ($x=0$), C is the gate capacitance per unit area, j is the current per unit gate width fixed at the drain ($x=l$). In the steady state without friction V, U are constant along the channel: $U= U_s$, $V= V_s =j/(C\, U_s)$.

The friction of electron flow results in the coordinate dependence of both the voltage $U(\eta)$ and the velocity $V(\eta)$. Using Eqs.(1),(2) one can find the steady state spatial dependence of the Mach number $M= V/S$:

$$F(M_s)-F(M)=\frac{2\gamma}{M_s^{1/3}}\cdot\eta \qquad (4)$$

where $S=(eU/m)^{1/2}$ is the local plasma wave velocity, $\eta=x/l$ is the dimensionless coordinate, $F(y)=y^{-4/3}+2y^{2/3}$, $\gamma=l/(S_s\tau)$ is the friction parameter, S_s is the local plasma wave velocity at the source. The Mach number increases downstream from the initial value M_s at the source to $M(1)=M_d$ at the drain. At a fixed friction parameter, γ, the relationship between the Mach numbers M_d and M_s, is given by Eq.(4) with $\eta = 1$. At a certain value of γ the current through the transistor saturates: the electron velocity at the drain $V(1)$ becomes equal to the plasma wave velocity $S(1)$, i.e. $M_d =1$. This is the so-called "choking" of the electron flow, which was considered in Ref. 3.

We now study the stability of the steady state flow with velocity $V(\eta)$ and channel potential $U(\eta$ by investigating the temporal behavior of small perturbations $V_1(\eta)exp(-i\omega t)$, $U_1(\eta)exp(-i\omega t)$ superimposed on the steady flow. Linearizing Eqs.(1),(2),(3) with respect to V_1 and U_1 we obtain the following equation:

$$(1-M^2)w''+\frac{\gamma M}{s}\left(2i\Omega-\frac{1+2M^2}{1-M^2}\right)w'+\frac{\Omega\gamma^2}{s^2}\left(\Omega+i\frac{1+M^2}{1-M^2}\right)w=0, \qquad (5)$$

$$w'(0)=0, \quad w(1)=0,$$

where $s= S/S_s$, $w= UV_1+U_1V$ is the current perturbation, $\Omega=\omega\tau$ is the dimensionless frequency. The complex frequency $\Omega=\Omega' + i\Omega''$ should be determined by solving these equations. A positive imaginary part $\Omega''>0$ corresponds to instability. Thus, in the presence of friction, the problem of instability of the steady state becomes extremely difficult. One has to find the eigenvalues spectrum of a second order differential operator with variable coefficients.

The solution of Eq.(5) without friction ($\tau=\infty$, $\gamma=0$, $M_s=M_d=M$, $S_s=S_d=S$) coincides with the one found in Ref.1. The real and imaginary parts of ω are given by

$$\omega_n'=\frac{S}{2l}\cdot\left|1-M^2\right|\pi n, \quad \omega''=\frac{S}{2l}\cdot(1-M^2)\ln\left|\frac{1+M}{1-M}\right| \qquad (6)$$

where n is odd integer for $|M|<1$ and even integer for $|M|>1$.

The mechanism of instability in the device without friction of electron fluid is as follows.[1] Two different plasma waves with wave vectors $k_{1,2}=\pm\omega/(S(1\pm M))$ propagate downstream and upstream respectively. The plasma wave amplitude grows due to boundary reflections. The argument of the logarithm in Eq.(6) contains the round trip gain factor, $(1+M)/(1-M)$, which is equal to the product of the reflection coefficients at two boundaries. The perturbation wave w propagates downstream during the time $l/(s(1+M))$, while the back propagation takes a longer

time, $l/(s(1-M))$. When $M \rightarrow 1$, the wave round trip time becomes infinite and the instability increment vanishes.

The role of friction for small currents ($M<<1$) was considered in Ref.1. Small friction ($\gamma<<1$) results in an additional term, $-1/(2\tau)$, in the wave increment ω'' and all the modes are damped identically. It is evident that the instability should be completely suppressed if the scattering is strong enough ($\gamma>>1$). Therefore, a critical value of the friction parameter, γ_{cr}, must exist for a given Mach number M_s, such that for $\gamma>\gamma_{cr}$ the flow is stable. Thus, one can calculate the instability threshold diagram, $\gamma_{cr}(M_s)$.

Our approach to solving Eq. (5) utilizes the short wave length approximation analogous to the quasiclassical approximation in quantum mechanics. Then the solution of Eq.(6) yields an explicit expression for the increment Ω'':

$$\Omega'' = -\frac{1}{2} + \frac{3}{4}\frac{M_s M_d}{M_d - M_s} ln\left(\left|\frac{1+M_s}{1-M_s}\right|\right) \qquad (7)$$

Substituting $\Omega''=0$ into Eq.(7) and using Eq.(4) for the relationship between Mach numbers at the source and drain one can plot the threshold diagram $\gamma_{cr}(M_s)$ (see heavy line at Fig.1). The threshold curve is confined between two asymptotes. One of them (dotted line 1 in Fig.1) is given by $\gamma_{cr}=2M_s$, which is the result obtained in Ref.1 for small values of γ, when the spatial distribution of M is only slightly non-uniform. The other one (dotted line 2 in Fig.1) corresponds to the "choking" of the electron flow. On the other hand, we have determined γ_{cr} by numerical simulations[4] on the basis of Eq.(1) and (2). The results coincide with our theoretical curve within the errors of the numerical method. Since the numerical simulations give the threshold for the most unstable modes, this agreement with the results, obtained analytically for higher modes clearly demonstrates the validity of our approach.

The region of instability may be also replotted as a region in the I-V plot (Fig.2). The heavy curve confines the instability region. The parts of the current-voltage characteristics lying within this region correspond to unstable states (dashed lines in Fig.2). For $\gamma \geq 0.54$ the current-voltage characteristics are always stable.

In Fig.3 we establish the FET parameters required for the observation of this new instability. As seen from this figure, sub 0.1 micron, submicron and dimensions on the order of several microns are required for the lowest, intermediate, and the highest values of the electron mobility.

Conclusions

In conclusion, the region of the plasma instability is limited by scattering at small current values and by choking at large current values. These results are accurately described by our analytical theory that is based on the approach similar to the quasi-classical approximation. Our calculation shows that this instability can be observed at room temperature in GaAs-based deep submicron devices and at cryogenic temperature in devices longer than one or two microns.

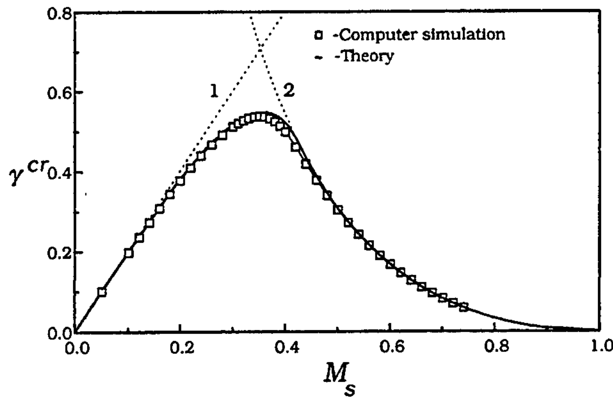

Fig.1. Diagram of instability threshold. The critical value of the friction parameter, γ_{cr}, as a function of Mach number at the source, M_s (heavy line). Asymptotic (dotted lines): 1- $\gamma_{cr} = 2M_s$, 2- choking threshold, determined by Eq.(4) with η=1 and $M = M_d = 1$.

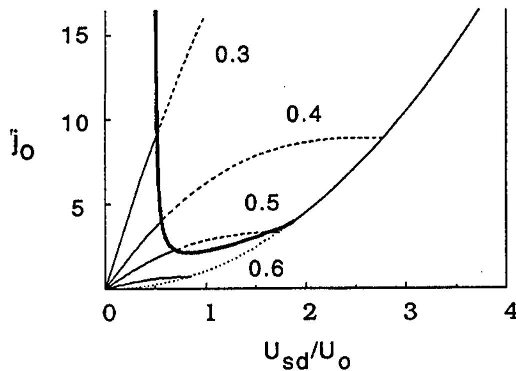

Fig 2. The region of instability on the I-V plot. The current-voltage characteristics in units $j_0 = Cm(l/\tau)^3/e$, $U_0 = m(l/\tau)^2/e$ are plotted for different values of parameter γ (shown near the curves.) The heavy line (corresponding to the heavy line in Fig.1), indicates the instability threshold. The dotted line corresponds to the choking threshold.[3] The unstable parts of the current-voltage characteristics are indicated by dashed lines.

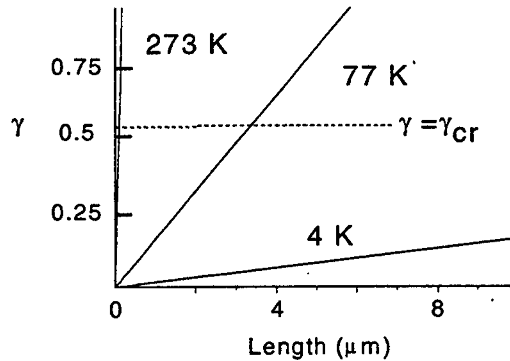

Fig.3. Length dependence of γ for GaAs for different values of the mobility. Parameters used in the calculation: parameter γ. The heavy line (corresponding to the heavy U=0.1V, m=0.063m_0. The dashed line represents the critical value of γ. For 273 K, μ = 9,000 cm^2/V-s; for 77 K μ = 300,000 cm^2/V-s; for 4 K, μ = 3,000,000 cm^2/V-s.

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A Power Balance Model for Hot-Electron Bolometric Mixers at THz Frequencies

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Introduction

In the following a complete nonlinear model for a hot electron bolometric (HEB) mixer valid in a frequency range from DC up to several THz is presented. The model is based on a power balance relation coupled with a lumped element circuit equation involving an empirical approximation function set for the device impedance as a function of frequency and electron/substrate temperature. Without linearization a complete big signal model is obtained from which a linear small signal approximation is derived. The large signal model yields general expressions for the bias points (currents and steady state electron temperature) as a function of bias voltage and substrate temperature and DC power dependent noise voltages. The small signal approximation yields then conversion gain and noise temperatures. Several shortcomings of existing model approaches have been improved: The experimental setup requires a constant bias voltage across a series inductance, series resistor and the device impedance. HEB device models usually assume a constant bias current [1] which is valid only for small signal approximations of heavily pumped HEBs. In this work parameters like self heating [1,2] and thermal conductivity between electrons and phonons are treated electron temperature dependent. Furthermore the bias point shift due to LO irradiation is fully taken into account. Therefore the model includes almost zero and negative differential resistance regions which typically lead to very small noise temperatures in unpumped or weakly pumped HEB devices.

Device Resistance model

A first order time dependent approximation for the resistance of a very short superconducting strip at nonzero frequencies has to show the following properties:

1. a smooth transition from superconducting to normal state at the quasiparticle bandgap frequency
2. a jump like transition for lower frequencies if the critical temperature is reached.

A simple relation to fulfill these requirements is

$$Z(\theta,\omega)=R_p+R_N(\theta_s)\cdot([1-t(\omega)]+\sigma(\theta-\theta_c)\cdot t(\omega))$$

where $t(\omega)$ denotes a first order low pass function with a time constant corresponding to the photon energy equivalent to the quasiparticle bandgap of the strip material and σ is the Heaviside unit step function.

To fit the experimentally obtained $R(T)$ relation to a curve template we assume the critical temperature of the superconducting strip to vary spatially and to be given by a

superposition of gaussian distributions. The probability density function to meet a certain critical temperature θ is thus given by:

$$p(\theta,\theta_c)=\frac{1}{N}\sum_{n=1}^{N}\frac{1}{\sqrt{\pi}}e^{-\left[\frac{\theta-\theta_c}{\sigma_n}\right]^2}$$

Integrating along a bolometer strip yields the following expressions for the device impedance:

$$Z(\theta,\omega)=R_p+[1+t(\omega)q(\theta)]\cdot R_N$$

with a transition function $q(\theta)$ and a low pass function $t(\omega)$:

$$q(\theta)=\frac{1}{2N}\sum_{n=1}^{N}\left[erf\left(\frac{\theta-\theta_{c,n}}{\sigma_n}\right)-1\right] \qquad t(\omega)=\frac{1}{1+i\omega\tau_1}$$

For high device currents above the optimal working point a current dependent correction of the resistance is needed. Then the device resistance takes the form:

$$Z(\theta,\omega,I)=R_p+[1+t(\omega)q(\theta)]\cdot R_N+t(\omega)q(\theta)\cdot R_v\cdot\frac{I-I_c(\theta)}{I_c(\theta)}\cdot\sigma(I-I_c(\theta))$$

Parameters extracted from measured iv curves (c.f. Fig. 1A) obtained at different ambient temperatures for NbN films with and without critical current correction are shown in Table 1. Figure 1B shows theoretical results obtained for the current corrected parameter set.

Power balance equation

The bolometer strip is assumed to be homogenously heated and irradiated.
In the temperature range studied the phonons are assumed to be in thermal equilibrium with the substrate. The only nonequilibrium particle species are electrons. They are described by an effective electron temperature which may exceed the substrate temperature. For constant bias voltage the following holds (c.f. [1]):

$$+c_pV\frac{d}{dt}\theta(t)=\alpha P_{rf}(t)+\frac{u_o^2}{R(\theta(t))}-B(R(\theta))\left[\theta(t)^v-\theta_c^v\right]$$

An equation for the bias point

A steady state solution of the above power balance equation yields the steady state electron temperature. This steady state temperature is in its turn inserted in the circuit relations to yield the bias points of the HEB mixer. Note that the radiation efficiency $B(R(\theta))$ depends on the device resistance since electron pairs in the superconducting state do not contribute to heat transport. Based on a two area model one expects a linear relationship of the form $B(R)=B_0+\beta\cdot R$. Results of $B(R)$-measurements at a 35Å thick NbN film for different substrate temperatures are shown in Fig. 2. It is crucial to include this relationship to be able to estimate the RF absorption coefficient α correctly by comparison of iv-characteristics with different RF powers at isothermal lines with $R=const.$ A comparison of measured and modelled ohmic heating powers for different device resistances and ambient temperatures are shown in Fig. 3. The steady state solution yields negative differential resistance for unpumped and weakly pumped HEB in accordance to the experimental results.
A two tone excitation (RF and LO frequency) of the device is modeled as an additive time dependent thermal heating term. Fourier series solution will yield a shift in bias current as a DC term (making it impossible to apply power series [4]) and an intermodulation term located at the difference frequency of the two tones. Its amplitude

is used to determine the conversion loss of the HEB mixer. Applying this device model to general expressions given in [3] one obtains for the self heating parameter C, the thermal conductivity between electrons and the substrate G and the conversion gain η:

$$C(\theta)=\frac{q(\theta)-1}{q(\theta)+1} \qquad G(\theta)=\frac{v_0^2}{R_p+R_n q(\theta)}\cdot\frac{q(\theta)-1}{q(\theta)+1}\cdot\frac{\partial}{\partial\theta}q(\theta)$$

$$\eta(\omega)=\alpha^3\frac{P_{LO}}{2R_L}\cdot\frac{(q(\theta)-1)^2}{1+\frac{1}{2}i\omega\tau(q(\theta)+1)}$$

Tables and Figures

Parameter		Value
T_c	Eff. Critical temperature *	9.6 K
σ	Eff. Transition width *	0.6 K
T_c	Corr. Critical temperature *	9.8 K
σ	Corr. Transition width *	0.05K θ_{sub} <7.95K 0.72K θ_{sub} >8.9K 0.876K - 7.71 θ_{sub} else
I_c	Critical current	0 θ_{sub} >8.9K 1542µA -173 µA/K* θ_{sub}
R_v	Resistance correction	7 Ω
R_n	Normal resistance **	271 Ω
R_p	Pad resistance **	11 Ω
η	Radiation exponent ***	3.6
B_0	Radiation efficiency *	0.0156 nW/K^3.6
β	Radiation coefficient *	0.0197 nW/(K^3.6 Ω)

Table 1: Parameter for the investigated NbN film obtained by
*) curve fit from measured iv characteristics,
) DC measurement *) Literature (e.g. [5]). "Eff."/"Corr" denotes parameters without/with current correction .

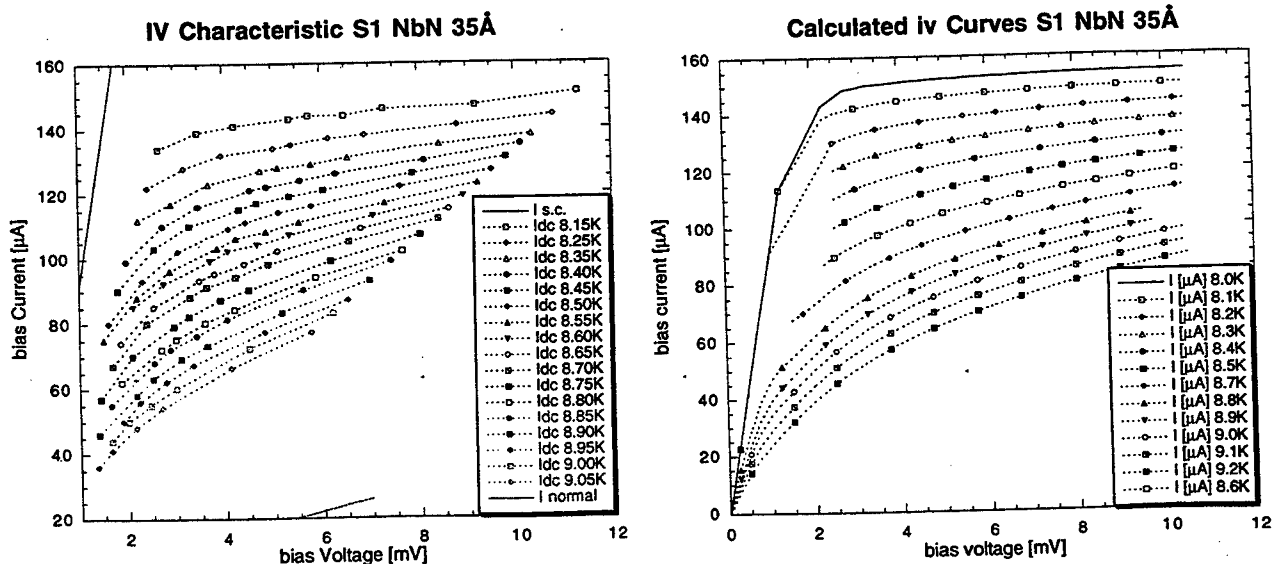

Figure 1: IV-Characteristics for different substrate temperatures

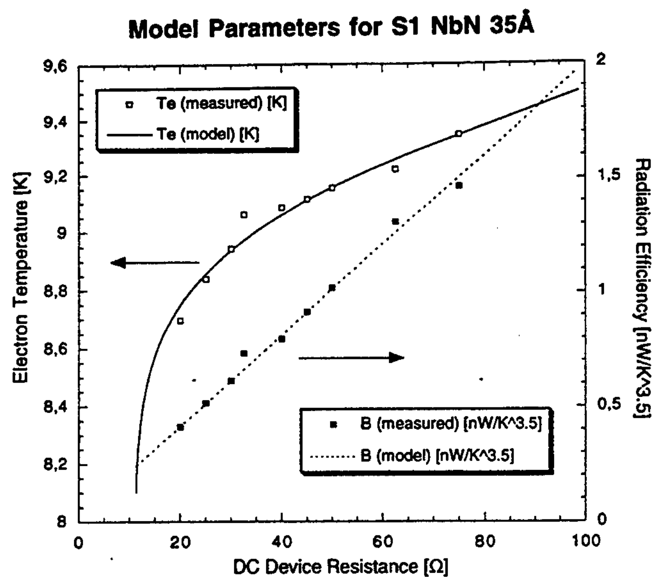

Figure 2: Extracted model parameters: R(T) and B(R)

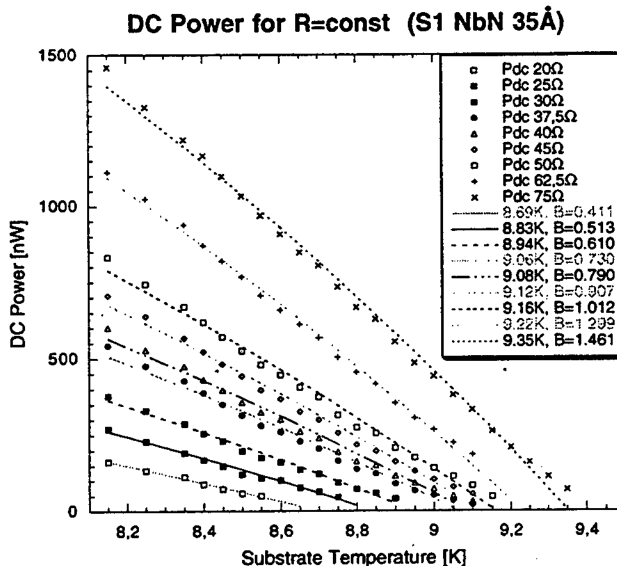

Figure 3: DC power for different device resistances. Constant device resistance leads to constant electron temperature and therefore identical losses

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Theory of spin-dependent transport in GaAs/AlAs/ErAs resonant tunneling diodes

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I. INTRODUCTION

Since the first observation of resonant tunneling through thin metallic layers[1], there has been a growing interest in electronic devices utilizing epitaxial metals integrated with semiconductors. Recently, resonant tunneling through semimetallic quantum wells of ErAs embedded in GaAs has been reported[2]. These experiments clearly demonstrate that spin polarization of carriers leads to a non-trivial dependence of the resonant tunneling on the magnitude and orientation of an external magnetic field. The spin polarization of the resonant channels in ErAs arises from a strong exchange coupling of valence electrons with localized 4f spins of Er atoms. This coupling leads to an increase of effective electron g-factor up to two orders in magnitude when the 4f spins are saturated by the magnetic field[4–6]. Spin-polarized transport has attracted much interest because of the discovery of giant magnetoresistance in magnetic multilayers[7]. This interest, in turn, has led to a design and fabrication of novel electronic devices such as spin-valve transistors[8]. The ErAs/GaAs heterostructure is a very interesting model system that displays both resonant tunneling which is feasible due to the close matching of ErAs and GaAs lattice constants[9], and spin-dependent transport which is due to the magnetism of Er 4f electrons[4–6]. It is conceivable that further study of this system (or similar systems) may lead to a development of novel devices that are based on spin-dependent resonant tunneling.

In this work we present a quantitative theory of the spin-dependent resonant tunneling through ErAs quantum wells observed by Brehmer et al.[2,3]. The experiments were carried out on resonant tunneling diode (RTD) structures consisting of semimetal ErAs quantum wells and AlAs barriers sandwiched between the $n+$ doped GaAs substrate and GaAs capping layers. The most extensive results and the once we focus on here were obtained for the (311) orientation of the films. The measurements of differential conductance indicate the presence of two different resonant channels[2,3] (peaks A and B in Fig.1).

The peak A splits in a magnetic field perpendicular to the layers while the channel B shows no observable splitting for either direction of the field, it is almost unresolved in zero or perpendicular field and is induced and enhanced by a field parallel to the film. A qualitative explanation of this phenomenon based on the Kohn-Luttinger model of ErAs valence states was given in[10] and can be understood with the help of the Fig.1(a) and

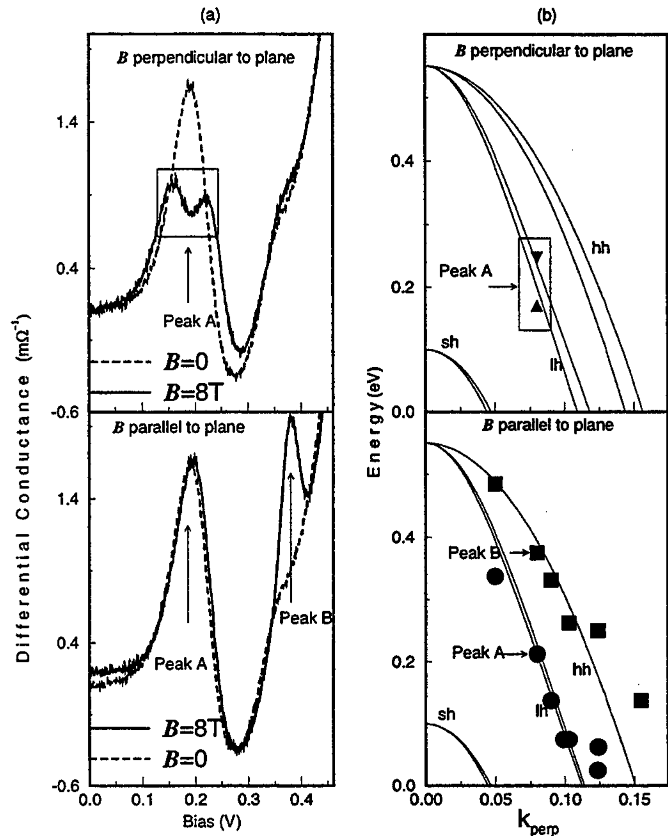

FIG. 1. Differential conductance of a 12-monolayer GaAs/AlAs/ErAs/AlAs/GaAs structure (Ref.[2]), exhibiting different behavior of resonant tunneling for magnetic fields perpendicular and parallel to the layers (a); and band structure of ErAs near the valence band maximum in the (311) direction in saturating magnetic fields of two orientations (Ref.[10]). Experimental resonance positions for different film thicknesses (or $k_\perp$ values) are indicated by circles for the A-channel and diamonds for the B-channel (b).

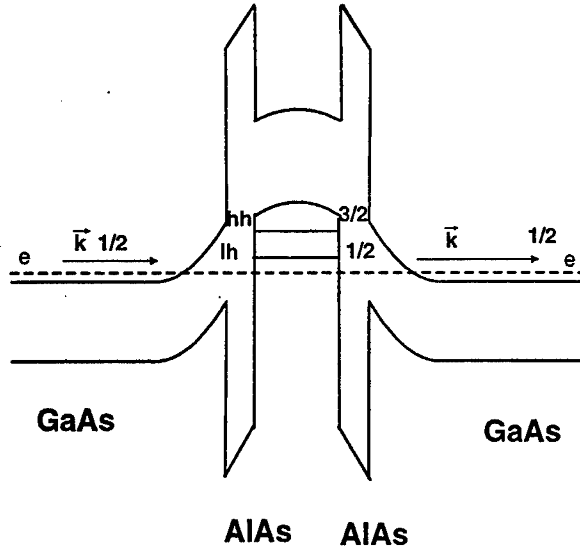

FIG. 2. Proposed schematic band diagram of GaAs/AlAs/ErAs/AlAs/ErAs RTD in (311) direction

Fig.2, where the band diagram of the structure in question is shown.

To summarize this explanation, we note that for the wave vector along (311) direction in semimetal ErAs unoccupied electron states are more than 1.5 eV above the Fermi level and there is a gap of about 1 eV between the unoccupied valence and conduction states.[5]. Therefore, the only states available for resonant tunneling are the ErAs confined hole states, since electrons tunneling from a vicinity of the Γ point of n^+ GaAs in the direction (311) must have their lateral momentum $k_{\parallel} \simeq 0$ conserved. In other words, the GaAs/ErAs RTD is an example of a system with Zener-like interband tunneling. For this system the potential across the junction is a barrier for electrons and, at the same time, it is a confining potential for holes (see Fig.2)

Since the structure of the valence band of ErAs is similar to that of GaAs one can expect a significant role of spin-orbit coupling and symmetry effects in the resonant tunneling[6,10]. The spin-orbit interaction couples the spin direction (determined by the magnetic field) to the direction of the orbital angular momentum of holes (determined by the normal to the interface). That is why the angular momentum conservation plays a crucial role for the interpretation of the experiment.

Namely, with the magnetic field absent or perpendicular to the layers, the projection of angular momentum onto the interface normal M_J is a good quantum number that must be conserved. The tunneling of s-like electrons with $|M_J| = 1/2$ from GaAs conduction band minimum into the heavy hole states with $|M_J| = 3/2$ (channel B) will be forbidden by symmetry. This explains why in that case the channel B is almost unresolved while the channel A (corresponding to the tunneling into the light hole states with $|M_J = |1/2)$ is quite pronounced. For in-plane fields, the states with $|M_J| = 1/2$ and $|M_J| = 3/2$ are mixed and the channel B becomes available for tunneling.

II. FORMULATION OF THE PROBLEM

Quantitatively, our system can be described by means of the following coupled Schrödinger equations:

$$H^e_\sigma|\psi^e_\sigma\rangle + \sum_m \hat{V}_{\sigma m}|\varphi^h_m\rangle = E|\psi^e_\sigma\rangle \tag{1}$$

$$\sum_{m'} H^h_{mm'}|\varphi^h_{m'}\rangle + \sum_\sigma \hat{V}^\dagger_{m\sigma}|\psi^e_\sigma\rangle = E|\varphi^h_m\rangle, \tag{2}$$

The equation (1) describes an electron (with spin $\sigma = \pm 1/2$ along the magnetic field) tunneling through the potential barrier (evanescent channel) which is coupled with the confined hole states φ^h_m by a mixing potential $\hat{V}_{\sigma m}$. The operator $\hat{V}_{\sigma m}$ is responsible for possible spin-flip processes since it may couple a given hole state $|\varphi^h_m\rangle$ with both states $|\psi^e_{\pm 1/2}\rangle$. The explicit form of this potential can be derived from the $\mathbf{k}\cdot\mathbf{p}$ perturbation theory and will be discussed below. An external magnetic field enters the Hamiltonians H^e_σ and $H^h_{mm'}$ only through the exchange field of 4f ions inside the barrier while a much smaller direct coupling of the spin and orbital momenta to the magnetic field is neglected. The basis of localized hole states $|\varphi^h_m\rangle$ is defined in terms of spherical harmonics with z axis always directed perpendicular to the interface rather than parallel to the magnetic field. That is why the matrix $H_{mm'}$ is non-diagonal for an arbitrary orientation of the magnetic field with respect to the interface.

In order to calculate the spin- dependent transmission amplitude we will generalize the scattering matrix technique developed by Gurvitz and Levinson[11]. It is convenient to start from a solution of the equation (1) with zero mixing potential:

$$H^e_\sigma \chi^\pm_{k_\perp\sigma}(z) = [-\frac{\hbar^2}{2}\frac{\partial}{\partial z}\frac{1}{m(z)}\frac{\partial}{\partial z} + U^e_\sigma(z)]\chi^\pm_{k_\perp\sigma}(z)$$
$$= E\chi^\pm_{k_\perp\sigma}(z), \tag{3}$$

where $k_\perp = \sqrt{(2m^*_e/\hbar^2)E - k^2_\parallel}$, and $\chi^\pm_{k_\perp\sigma}$ are the left incident and the right incident scattering solutions of the electron Schrödinger equation having asymptotics $\chi^\pm_{k_\perp\sigma} \overset{z\to\pm\infty}{\Longrightarrow} t_{0\sigma}\exp(\pm ik_\perp z)$, where $t_{0\sigma}$ is the transmission amplitude corresponding to a decoupled evanescent channel with the barrier $U^e_\sigma(z)$. We have introduced a z-dependent effective mass $m(z)$ in order to take into

account its different values in ErAs quantum well and in GaAs asymptotic regions, therefore we assume that $m(z) \stackrel{z\to\pm\infty}{\Longrightarrow} m_e^*$, where m_e^* is an effective mass of electrons in the conduction band of bulk GaAs.

The equations (1)-(3) allow one to construct the spin-dependent transmission matrix:

$$t_{\sigma\sigma'} = t_{0\sigma}\delta_{\sigma\sigma'} + \sum_{ij}\langle\chi^-_{k_\perp\sigma}|\hat{V}_{\sigma i}|\varphi_i^h\rangle G^h_{ij}(E)\langle\varphi_j^h|\hat{V}^\dagger_{j\sigma'}|\chi^+_{k_\perp\sigma'}\rangle \quad (4)$$

where G^h_{ij} is a Green's function of localized holes, which is renormalized due to the coupling with the evanescent channel:

$$(G^h(E))^{-1}_{ij} = E\delta_{ij} - H_{ij} - \sum_\sigma\langle\varphi_i^h|\hat{V}^\dagger_{i\sigma}G^e_\sigma\hat{V}_{\sigma j}|\varphi_j^h\rangle \quad (5)$$

The expression (4) is a central result of this work, which is an excellent starting point to analize spin-dependent tunneling transport through magnetic quantum wells with spin-flip processes taken into account. The details of its derivation will be published elsewhere[12].

III. RESULTS

While the complete analysis of the transmission probability in a tilted magnetic field will be published elsewhere[12], here we present the results for two particularly important cases corresponding to a magnetic field perpendicular and parallel to the layers. Since there are no spin-flip processes allowed for these two cases[12], the tunneling current is a superposition of two independent spin currents. As in our previous work[10] we will use $\mathbf{k}\cdot\mathbf{p}$ theory and the spherical Kohn-Luttinger Hamiltonian[13]. We will take into account the first two zero-field quantized hole levels $E_{1/2}$ and $E_{3/2}$ only. With the assumptions $t_{0\pm1/2} = t_0$ and $k_\| \simeq 0$, the final expression for the transmission coefficient is:

$$T(E,\vec{B}) = \frac{1}{2}T_0(E)\sum_{\sigma=\pm1/2}\frac{(\Sigma^\sigma_E(\vec{B}) - \Delta_E)^2}{(\Sigma^\sigma_E(\vec{B}) - \Delta_E + \delta_E)^2 + \Gamma^2_E} \quad (6)$$

where $T_0 = |t_0|^2$ is the "bare" transmission coefficient, describing non-resonant tunneling in the absence of the mixing potential, and the self-energy Σ^σ_E is given by:

$$\Sigma^\sigma_E = \begin{cases} E - E_{1/2} - \sigma\Delta_{xc}(\vec{B}_\perp), \\ \text{for } \vec{B}\perp \text{ to the interface;} \\ \\ E - E_{1/2} - \sigma\Delta'_{xc}(\vec{B}_\|) - \gamma^2_{xc}(\vec{B}_\|)/(E - E_{3/2}), \\ \text{for } \vec{B}\ \| \text{ to the interface} \end{cases} \quad (7)$$

The parameters Δ_{xc}, Δ'_{xc} and γ_{xc} describe the splittings and mixing of resonant channels by an exchange field of $4f$ Er ions. The magnetic field dependence of these parameters is assumed to follow the Brillouin theory of paramagnetic alignment of localized spins as it was established experimentally[4]. We also introduced elastic inverse life-times

$$\Gamma_E = \Gamma_+ + \Gamma_-, \qquad \Gamma_\pm = \frac{m_e^*}{2k_\perp\hbar^2}|\langle\chi^\pm_{k_\perp}|V_{mix}|\varphi_{1/2}\rangle|^2, \quad (8)$$

and energy shifts $\delta_E = (4\Gamma_+\Gamma_-/T_0 - \Gamma_E^2)^{1/2}$, and

$$\Delta_E = \frac{m_e^*}{k_\perp\hbar^2T_0}\int_{-\infty}^{\infty}\varphi_{1/2}(z)V_{mix}(z)dz \times \int_{-\infty}^{z}\varphi_{1/2}(z')V_{mix}(z')Im(\chi^+_{k_\perp}(z')\chi^{-*}_{k_\perp}(z'))dz', \quad (9)$$

where $\varphi_{1/2}(z) \simeq \cos(\pi z/L)$, $V_{mix}(z) = -ip(z)\cdot\partial/\partial k_\perp$, and the hole quantum well is assumed to be symmetric and located in the region $-L/2 \le z \le L/2$.

As can be seen from the formula (6) there is only one resonance-antiresonance pair per spin for $\vec{B}$ perpendicular to the interface (resonant channel A in the experiment[2,3]), while there are two such pairs per spin for in-plane $\vec{B}$ (resonant channels A and B). In other words, the in-plane field mixes the light and heavy hole states and "pumps" the resonant channel B. The antiresonances ($\Sigma_E = \Delta_E$) in (6) correspond to the total resonant reflection of an electron with a given spin, while the resonances ($\Sigma_E = \Delta_E - \delta_E/(1 - T_0)$) correspond to the total resonant transmission of this electron through a nearly symmetric barrier ($\Gamma^+ = \Gamma^-$). It can be shown[12] that the quantity

$$T = \sum_{\vec{k_\|}} T(k_\perp(E_F, \vec{k_\|}), E_F + eV), \quad (10)$$

approximately describes the dependence of the differential conductance through a semimetal (or metal) quantum well versus applied bias V in the vicinity of the resonances and, therefore, can be roughly compared with experiment. The summation in (10) is taken over all $k_\|$ belonging to the Fermi-sphere of n^+ GaAs. The transmission coefficient T as a function of V, calculated by means of the formula (10), is displayed in Fig.3 where we have taken into account the $k_\|$ dispersion of the quantized hole states $E_i = E_i^0 - (\hbar^2/m_{hi})k_\|^2$ and introduced inverse inelastic life-times $\Gamma_{scat} = \hbar/\tau_{scat} = \hbar k_\|/m_{hi}l^*_{scat}$ ($i = \pm1/2, \pm3/2$) which we attribute to the broadening of the quantized hole states due to the scattering of the lateral momentum at the ErAs/GaAs overgrowth interface. The model numerical calculations where performed for a 12-monolayer ErAs quantum well with a rectangular barrier of 1.5 eV height for electrons. The value of the

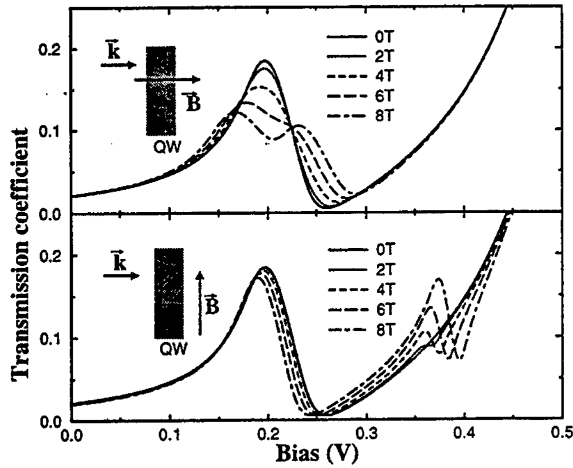

FIG. 3. Calculated transmission coefficients of a 12-monolayer ErAs quantum well for various magnitudes and two different orientations of the magnetic field

surface scattering length l_{scat} was fitted to reproduce the experimental width of the resonant channel A. Our estimate of l_{scat} is ~ 300 Å which is clearly an indication of rather poor quality of the interface at GaAs overgrowth.

To conclude we not that our model (Fig.3) qualitatively reproduces experimental behavior of spin-dependent resonant tunneling through ErAs quantum wells. It displays both rather strong dependence of the intensity of the heavy-hole channel on the magnitude of the external magnetic field and Zeeman splitting of the light-hole channel for magnetic fileds perpendicular to the layers. Further study will include realistic calculations of the electronic spectrum of a quantum well and a mixing potential across the interface as well as analysis of different scattering mechanisms

IV. ACKNOWLEDGMENT

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Field Plate Structure for High-Voltage SiC Power Devices

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1.0 Introduction

One important advantage of fabricating high-voltage power devices from 4H silicon carbide (bandgap = 3.3 eV) is the factor of ten larger breakdown field vis silicon. This permits 4H SiC power devices with much higher doping densities in the blocking epi-layer (10^{15} cm^{-3}) to have equivalent breakdown voltages with respect to existing silicon devices while having a much lower specific on-resistance. For example, it can be calculated using published data for the breakdown field of 4H SiC (3 MV/cm[1]) and the breakdown voltage versus doping density curves for silicon[2] that a donor concentration in the mid 10^{15} cm^{-3} range and a minimum width of 50 μm is required for a 5,000 V blocking layer, as is well known in the silicon carbide device community.[3] However, it is also well known that proper junction termination is critical for achieving in practice the theoretical breakdown voltage of a device containing a specific lightly doped epitaxial layer.[4]

In fact, the large breakdown field of silicon carbide with respect to silicon encourages a strategy of using more highly doped blocking layers than used in silicon for a given device voltage rating to take advantage of the resulting lower specific on-resistance, but this strategy implies that, by design, the maximum electric field will always be larger in the silicon carbide device than a comparable silicon device. However, the scaling of the bulk field in actual devices is almost always easier to accomplish than the scaling of the surface fields. In other words, if simultaneous and careful attention is not paid to surface issues, such as junction termination and passivation, then actual device voltage ratings will increase much more slowly than originally anticipated for silicon carbide. Issues such as soft breakdown, thermal runaway, and catastrophic failure at the device boundaries are always an issue in power electronic devices. Methods, strategies, and device design have evolved for silicon to address these issues. A comparable systems approach, emphasizing materials, device design, and device fabrication that are relevant to silicon carbide must be developed.

2.0 Junction Termination Strategy

In this paper we present our work to develop a class of innovative and manufacturable junction termination/passivation strategies based on the so-called "field-plate" junction termination with semi-insulating thin-film passivation.

This basic "systems" approach was originally developed for, and widely applied to, silicon-based high-voltage electronics devices, such as the Insulated Gate Bipolar Junction Transistor. In silicon, the well known "SIPOS" semi-insulating CVD process is often implemented.[5,6] A comparable CVD-based semi-insulating thin-film technology for silicon carbide is needed. Mississippi State University is working to achieve this technology using a co-doping process that will allow for the in situ growth of multiple epi layers consecutively during one growth "run." For example, one might start by growing an n^+ buffer layer on the substrate, followed by a lightly doped voltage blocking layer, followed by more heavily doped n- or p-type device layers, followed by one or more high-purity (lightly doped) compensated semi-insulating epitaxial films for passivation and field-plate junction termination, as shown in Figure 1.

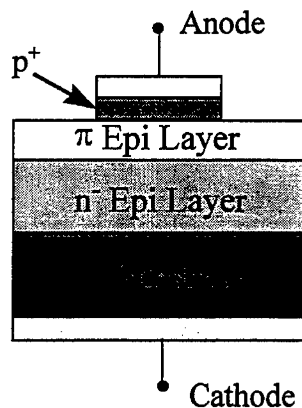

Figure 1. Field termination of pn-junction diode showing high-resistivity (π) layer which grades the potential to the device periphery.

Before discussing how the device structure in Figure 1 can be used to relax the surface fields, we will discuss the synthesis of the "π" layer, since it is the critical layer for this application.

3.0 Semi-Insulating Epitaxial Layer Synthesis

The key epitaxial layer in this system of epi layers is the high-resistivity or semi-insulating "π" layer. It is well known that substrate resistivities in SiC can approach 1 x 10^{15} Ω-cm by use of vanadium deep acceptors.[7] The use of a mid-gap impurity is acceptable for substrates, but use of such a deep-level in a device layer could severely degrade the minority carrier lifetime (MCL) and thus be unsuitable for a high-quality device layer. In addition, mobility degradation is possible. It is desirable to use a more suitable level for achieving compensation in device-quality epitaxial layers. The Emerging Materials Research Laboratory is exploring solid-source boron-doping of 6H-SiC such that the boron-related D-center[8] which has an activation energy of $E_A = E_V + 0.58$ eV, is used to compensate residual nitrogen donors. Since boron is present in all SiC material, the use of the D-center should result in negligible mobility and MCL degradation. A calculation of both the Fermi level position and resistivity for a D-center concentration of $1-100 \times 10^{14}$ cm^{-3} and a nitrogen concentration of 5×10^{14} cm^{-3} is available in the literature.[9] The calculation predicts that for a slightly over compensated layer (say $N_T = 1.0 \times 10^{15}$ cm^{-3}) a resistivity of approximately 3×10^7 Ω-cm is expected, which is high enough for junction termination, as will be shown later when we give an example of our technique for a pn-junction power diode.

Using a cold-wall chemical vapor deposition (CVD) system in our laboratory, we have carried out several growth experiments whereby a boron-nitride (BN) co-doping technique was used to incorporate boron in 6H-SiC epitaxial layers. Secondary ion mass spectroscopy (SIMS) data was taken by the Royal Institute of Technology in Kista, Sweden. SIMS data for our undoped epitaxial layers indicates a boron concentration at or below the detection limit of 4×10^{14} cm^{-3}, with an aluminum concentration of approximately 4×10^{15} cm^{-3}. Figure 2 shows a series of SIMS profiles for 6H-SiC epitaxial layers after several in-situ solid-source boron doping experiments. A summary of this work has recently been reported.[10] It is sufficient to note here that there is clear evidence of boron incorporation, with concentrations ranging from the detection limit to approximately 4×10^{17} cm^{-3}, with a corresponding increase in the aluminum incorporation of between approximately 4×10^{16} cm^{-3} and 1×10^{17} cm^{-3}. X-ray fluorescence spectroscopy performed on the BN solid source material indicates that the BN is the source of the excess aluminum. However, this has a beneficial effect since a majority of the compensation of the nitrogen donors will be accomplished with the shallow aluminum acceptor, and the D-center will be used to "finish off" the compensation process. Thus minimum deep-level incorporation will be used, ensuring that the compensated layer will have better transport properties.

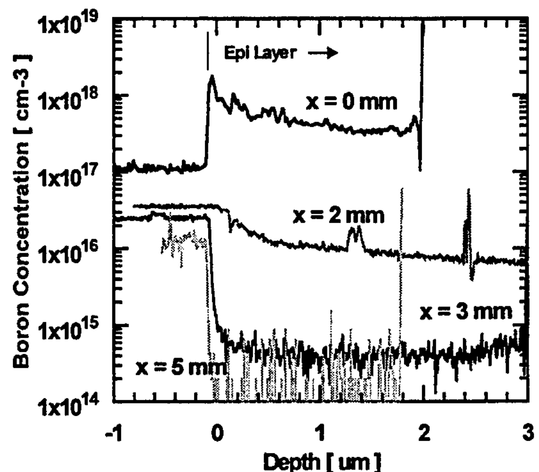

Figure 2. SIMS data showing B incorporation in boron-doped epitaxial layers as a function of BN co-doping source position x.

We have carried out several controlled boron doping experiments, and have achieved boron levels over a range from less than 4×10^{14} cm^{-3} to 1×10^{19} cm^{-3}, as determined by SIMS. In fact, a recent layer, when capacitance-voltage (C-V) measurements were made, was fully-depleted indicating either very low doping or perhaps even semi-insulating behavior. This layer also showed type conversion (i.e., was p-type) which leads us to believe that a high-degree of compensation by the aluminum acceptors and D-center was achieved. Hall measurements are planned to test this observation and determine if, in fact, semi-insulating material was grown.

4.0 Field Termination in a PN Junction Diode

The objective of this research is to demonstrate the feasibility for using a π layer as part of a system of epitaxial layers for high-voltage device fabrication. Since the major components of the "system" (i.e., the thick lightly doped voltage-blocking layer, n- and p-type device and buffer layers, and semi-insulating "π" passivation layer) can be grown in situ in one growth run, manufacturability and reliability are greatly enhanced. Using the compensation calculations described in the last section, we performed calculations of the reverse blocking and forward conduction modes for power pn junction diodes incorporating boron-compensated semi-insulating epi layers. We have reported in the literature[11] a simulation which shows the electrostatic potential distribution for a pn junction diode which incorporates a guard ring to prevent leakage currents from affecting adjacent devices. The device structure simulated consists of a 600 μm diameter anode contact surrounded by an annular guard ring with an anode-to-guard ring spacing of 600 μm. Beneath the anode contact is a thin p^{++} layer (to achieve ohmic contact to the pn junction). The remainder of the simulated device consists of a 4 μm thick π-layer placed on top of a 50 μm thick n^- (3×10^{15} cm^{-3}) voltage blocking layer. Finally the n^+ substrate supports the device layers just described. Thus the pn junction is formed by the p^{++} and n^- layers. The surface potential was calculated assuming cylindrically-symmetric ohmic conduction in the π layer, which is valid since the spacing between the anode and guard ring is many diffusion lengths ($L_n \approx 4$ μm for a resistivity of 1×10^8 Ω-cm). The potential across the pn junction was calculated using the junction space charge approximation, since in the vertical direction, the 4 μm π layer is on the order of less then the diffusion length. As demonstrated in that report, the incorporation of the high-resistivity π layer results in a surface field profile relaxed by more than an order of magnitude with respect to the junction electric field distribution.

Clearly the surface field is greatly relaxed due to the incorporation of the π layer. The next important question is the effect of the π layer on the forward voltage drop in the device. We performed a one-dimensional drift-diffusion calculation, the result of which is shown in Figure 3. For comparison, we also plot the forward voltage drop for a 4H-SiC Schottky diode reported in the literature.[12] Clearly the majority of the forward voltage drop is not attributed to the π layer, but rather the lightly-doped thick n^- layer, as expected given that the compensated p-layer is thin compared to a diffusion length.

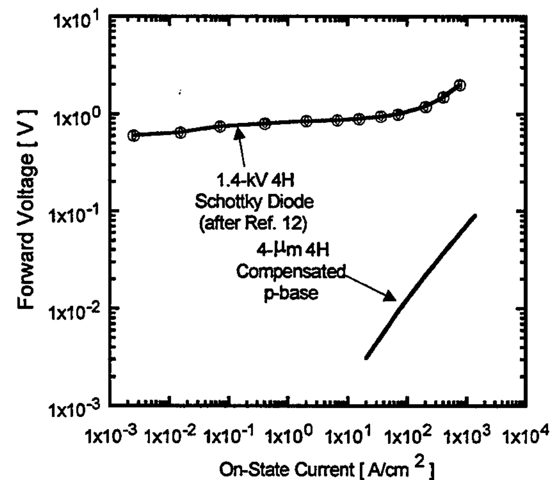

Figure 3. Calculated forward voltage drop for the device structure of Fig. 3 compared with experimental data for a Schottky diode. [Schottky data from ref. 12]

5.0 Conclusion

We have proposed a system of epitaxial layers whereby a semi-insulating "π" layer is incorporated into a power SiC device structure. We have reported calculations that indicate the "π" layer will relax the surface field, and thus when incorporated with an integral guard ring,

provide edge termination for SiC power devices. A proposal to use the D-center to achieve close compensation in device-quality epitaxial layers has been discussed and relevant work toward achieving this goal presented. In future work we will demonstrate repeatable "π" layer synthesis using this method, followed by the demonstration of the proposed field termination strategy.

6.0 Acknowledgment

The authors thank Adolf Schöner of the Industrial Microelectronic Center (IMC), Kista, Sweden for assistance in characterizing the boron-doped epitaxial layers as well as fruitful discussions relating to the use of the D-center for close compensation of these layers. We also thank Mike Okhuysen and Andrei Los, both of the Emerging Materials Research Laboratory, for assistance with the growth and characterization of the boron-doped epitaxial layers

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Examining the potential of SiGe epitaxial channels for CMOS

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Introduction: Searching for improvement in electrical performances of PMOSFET's many research labs consider the use of $Si/Si_{1-x}Ge_x/Si$ heterostructures [1] in CMOS. In this paper we report on our study of transport properties in SiGe heterostructure channels in function of temperature. Special emphasis is put on analysis of the band offset (ΔE_V) and mobility, as two factors determining the gain in electrical performances. Therefore in addition to having demonstrated the big potential of SiGe heterostructures to current improvement, we have also performed an in-depth analysis of the physics governing the ΔE_V and mobility. This has led us to propose a new method for extracting ΔE_V from the plots of threshold voltage versus temperature, this being much more straightforward than the commonly used Hall measurement method. We have also studied Germanium phonon and Si/SiGe interface scattering and revealed their role played in the determination of the mobility. This has led us to propose a simple and new method of extraction of scattering parameters related to the Ge phonon and interface states. Both ΔE_V and scattering parameters are thus extracted from the transistor without necessity special test structures.

Process : We have studied PMOS transistors with $Si/Si_{1-x}Ge_x/Si$ heterostructures, Fig 1. The Ge fraction is respectively 0; 15 or 30 percent. As a reference we have used devices with an As implanted pure-Si channel, fabricated using the same process except for epitaxy. All samples received strong retrograde implantation for punchtrough protection. An intrinsic unstrained silicon buffer of 35 or 60 nm thickness was then epitaxially grown to shift the channel away from the high doping region. The strained $Si_{1-x}Ge_x$ channel, 20 nm thick, was next grown and implanted to ensure its n-type. Finally, an intrinsic unstrained 6 nm thick Si cap layer was grown to separate the channel from the SiO_2/Si interface [2].

Investigating the band structure: The plots $V_{THSi_{0.7}Ge_{0.3}}(T)$, $V_{THSi_{0.85}Ge_{0.15}}(T)$ and $V_{THSi_{epi}}(T)$ Fig. 2 show a constant difference, independent of temperature. We have found that this difference should correspond to the valence band offset. Actually, let consider V_{TH} expressions [3] for the SiGe channel and the Si-epi one, shown in Fig. 2. Then, let us make the following simplifications: (i) take into account only the terms independent of temperature (since constant difference) and (ii) suppose that N_B variation with T is similar in both cases. Q_f and C_{ox} are taken into account in the ΔV_{FB} (flat band voltage), Fig 14. As a result, the difference between the relevant V_{th} plots turns out to be actually equal to the band offset plus the difference in V_{FB} $\Delta V_{TH} = \frac{\Delta E_V}{q} + \Delta V_{FB}$. In this way, we find ΔE_V = 307 meV and ΔE_V = 161 meV for 30% and 15% Ge fraction respectively, this being in good agreement with the results obtained via Hall measurements (320 mV and 160 mV) [4].

Electrical characteristic: The gain in drain current at V_d = -1.8 V, V_g-V_{th}=V_{gt}=-0.3 V at 80K resulting from the use of $Si_{.7}Ge_{.3}$ channel with respect to As-implanted channel (no epi) is as large as 354%. With respect to the Si-epi channel it becomes equal to 114% and finally, with respect to the $Si_{.85}Ge_{.15}$ it reads at 65%. Note that for V_{gt} =-1.8 V and T=80K (Fig 5 and Table 1) these gains read at 371%, 139% and 64% for $Si_{.7}Ge_{.3}$ with respect to As-implanted, Si-epi and $Si_{.85}Ge_{.15}$ channels respectively. All the gain with respect to the reference channel are in the Table 1. We can see that the majority of gain appears at V_{gt} =-0.3 V, and very little further improvement is observed, especially for the use of $Si_{.85}Ge_{.15}$ when increasing V_{gt} up to -1.8 V. This is attributed to insufficient band offset with 15% Ge, which leads to fulfilling of the quantum well and thus to an overflow of holes towards the Si/SiO_2 interface. This is because the

This work has been carried out within the GRESSI consortium between CEA LETI and France Telecom CNET

population of surface holes grows rapidly with increasing V_g-V_{th} bias whereas that of quantum well holes saturates once the well is fulfilled. Note that this scenario is well confirmed when examining deeper quantum wells. As shown in Table 1, the $Si_{.7}Ge_{.3}$ channels actually show much larger improvement attaining 185% at 300K if comparing the $Si_{.7}Ge_{.3}$ and As-implanted channels.

Physical study of mobility: The gain in drain current correlates very well with improvement in mobility (Fig 7). Indeed, we have an increase of 180% in mobility (175% in current, Table 1) for the $Si_{.85}Ge_{.15}$ as compared to the As-implanted channel at T=85K. The improvement in mobility with respect to the Si-epi channels is about 29%, Table 1, (30% in current). The same good correlation holds at T=300K, actually the mobility gain with the use of $Si_{.7}Ge_{.3}$ attains 183% knowing that the drain current gain is 185% at T=290K. In Table 1 we have summarized the evolution of the gain in mobility with different channel architectures, all with respect to the As-implanted channels. Our extractions of θ_g and μ_0 (Fig 8 and 9) show, as expected, an improvement in μ_0 when moving from As-implanted via Si-epi to SiGe channels. The behavior of θ_g shows, however, an anomaly in the case of As-implanted channels. A plausible explanation to the smallest value of θ_g in the latter case may be that the epitaxy can sometimes magnify surface roughness (see $\theta_g(T)$ for Si-epi, $Si_{.85}Ge_{.15}$ and $Si_{.7}Ge_{.3}$) and thus lead to an increase in θ_g, when still improving μ_0 (and also μ_{eff}) because of reduced impurity scattering. Usually, the improvement in mobility of the SiGe channel is attributed to four factors: (i) lower scattering on impurities (presence of the buffer), (ii) decrease of scattering on surface roughness (cap layer), (iii) lower transversal field, and (iv) lower hole effective mass in SiGe. Fig 10 shows, however, that these four mechanisms are insufficient to explain the SiGe channel mobility. Indeed, if we plot the difference between the inverse of μ_{SiGe} and μ_{Epi60} ($\Delta 1/\mu = 1/\mu_{Eff_{SiGe}} - 1/\mu_{Eff_{Si-epi}} = 1/\mu_{Ge} + 1/\mu_{Si/SiGe}$) in function of E_{eff} and T, Figs 10, 11 and 12, then we should have found a constant, reflecting a possible difference in the effective mass between Si and SiGe. Instead, however, we find a quantity varying as $E_{eff}^{(1/3)}$ for higher temperature (Fig 10) which can be associated with phonon type scattering ($\frac{1}{\mu_{PH}} = \gamma E_{eff}^{1/3} + \delta$), according to [5]. This means that phonon scattering in SiGe is different from that in Si, and suggests an active role played by the Ge phonon at room temperature. The plausible explanation is that the Ge phonons, lighter an thus less efficient in scattering than Si phonons, replace certain number of Si phonons (in proportion to Ge-to-Si fraction) thus reducing the phonon scattering component in SiGe channels. Note that without making this hypothesis, the empirical model of C.-L. Huang [5] is unable to fit the mobility curves in Fig 10. For lower temperature, Fig 12, we find a variation in E_{eff}^2 and, for moderate temperature (near 200K), Fig 11, a variation in E_{eff}. This behavior can be associated according to [5] ($\frac{1}{\mu_{SR}} = \beta E_{eff}$ or $\frac{1}{\mu_{SR}} = \beta' E_{eff}^2$), to the scattering on the Si/SiGe interface (see Fig 13).

Conclusion : In conclusion, large potential of Si-epi channels, and especially that of SiGe epi channels, to improved current drivability has been demonstrated. In depth physical analysis of the transport properties in SiGe channels has led us to propose a new method for extracting the valence band offset from V_{th} measurements in function of temperature. This method is much simpler and straightforward than the Hall method. We have also proposed a new method of extraction of scattering parameters related to Ge phonon and to Si/SiGe interface, which has to be included into the mobility model in order reconcile the theoretical predictions with experiment. These two techniques have the advantage of being applicable directly on the transistor (characterization *in situ*), and, therefore do not need special test devices (e.g. Hall measurement).

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$$V_{TH}(SiGe) = \phi_{MS} - \frac{Q_f}{C_{ox}} + 2\Phi_F + \frac{\Delta E_v}{q} - \frac{kT}{q}\ln\left(\frac{N_{V_{Si}}}{N_{V_{SiGe}}}\right) - qN_B\Delta d_{max}\left(\frac{1}{C_{ox}} + \frac{1}{C_{cap}}\right)$$

$$V_{TH}(Si_{epi}) = \phi_{MS} - \frac{Q_f}{C_{ox}} + 2\Phi_F - qN_B\Delta d_{max}\left(\frac{1}{C_{ox}}\right)$$

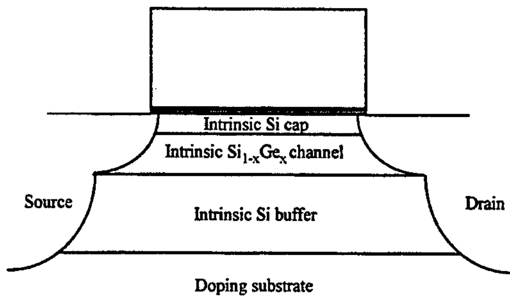

Fig1: Schematic of the SiGe channel structure.

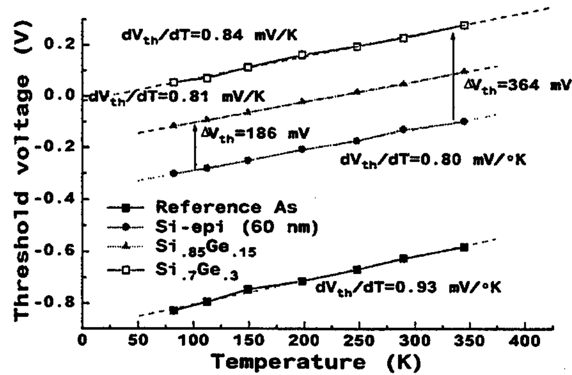

Fig 2: Temperature dependence of the threshold voltage for $Si_{.7}Ge_{.3}$, $Si_{.85}Ge_{.15}$, Si-epitaxial and Arsenic implanted channel.

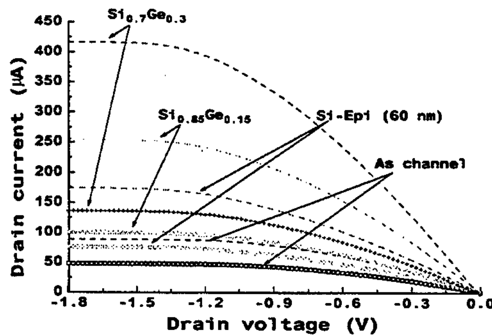

Fig 3: Output characteristics for long channel at V_{gt} =-1.8 V. Dotted line for T=85K and solid line for T=290K.

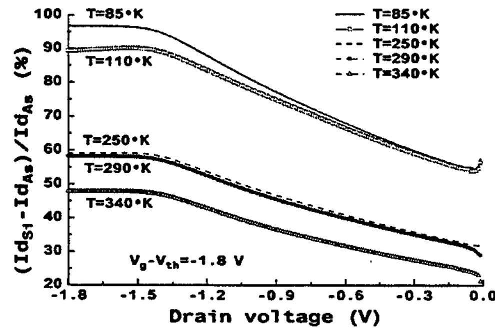

Fig 4: Drain current improvement with Si-Epi channel with respect to As implanted channel as a function of Vd for V_{gt} =-1.8 V.

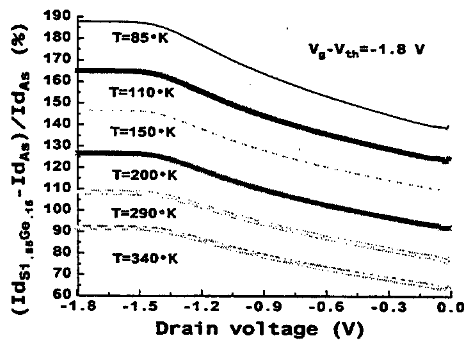

Fig 5: Gain in drain current with $Si_{.85}Ge_{.15}$ channel with respect to As implanted channel as a function of Vd for V_{gt} =-1.8 V.

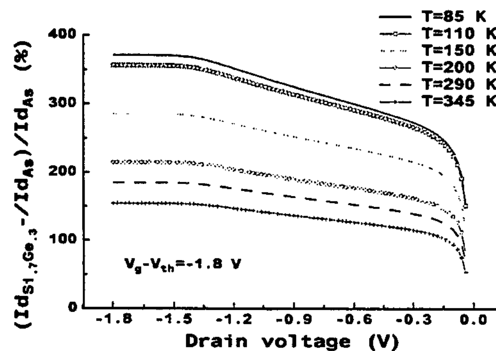

Fig 6: Increase in drain current with $Si_{.7}Ge_{.3}$ channel with respect to As implanted channel as a function of Vd for V_{gt}=-1.8 V.

Table 1: Mobility and drain current gain in percentage (reference = As implanted channel).

	T=290K			T=80K		
	Si-epi 60 nm	$6/20_{30}/35$	$6/20_{15}/35$	Si-epi 60 nm	$6/20_{30}/35$	$6/20_{15}/35$
Gain in mobility	87	183	119	118		180
Gain in drain current at V_{gt} =-0.3 V	54	155	97	97	354	175
Gain in drain current at V_{gt} =-1.8 V	59	185	109	112	371	188

*Mobility and drain current gains for various architectures. We note x / y_p / z, where x, y and z are cap layer, SiGe channel and buffer thickness, respectively. p is the Ge fraction in the channel.

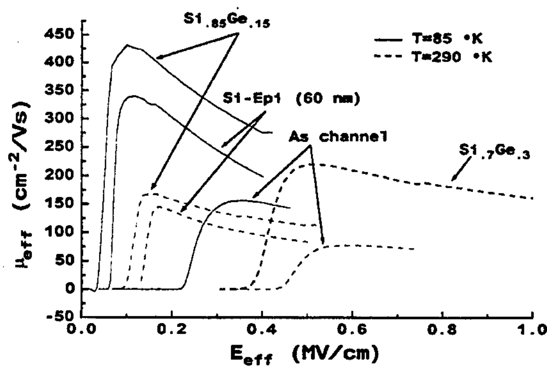

Fig 7: Extracted effective mobility by split-C(V) method for the As, Si-epi, $Si_{.85}Ge_{.15}$ and $Si_{.7}Ge_{.3}$ channels.

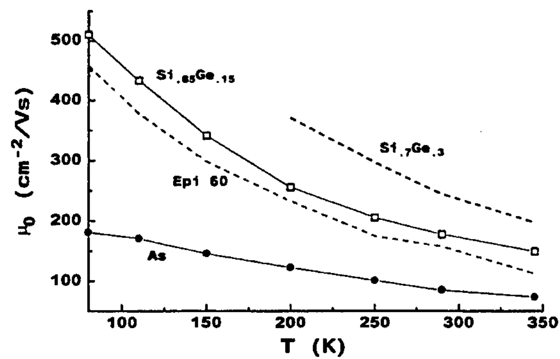

Fig 8: μ_0 (T) for As, Si-epi, $Si_{.85}Ge_{.15}$ and $Si_{.7}Ge_{.3}$ channel.

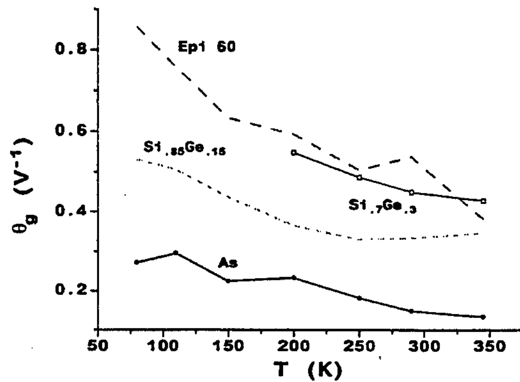

Fig 9: θ_g (T) for As, Si-epi, $Si_{.85}Ge_{.15}$ and $Si_{.7}Ge_{.3}$ channel.

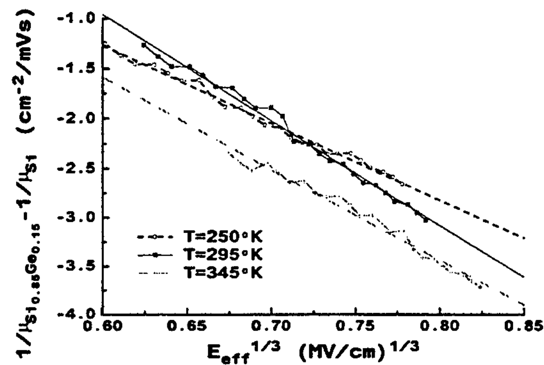

Fig 10: Mobility like-phonon behavior for T > 200K

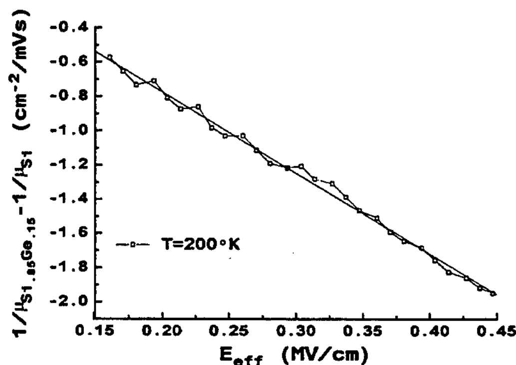

Fig 11: Singularity of the effective mobility, in a narrow range of temperature around 200K, a variation in E_{eff} is observed.

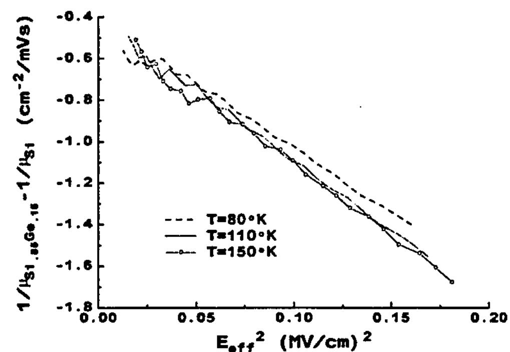

Fig 12: Behavior of the effective mobility for T < 200K

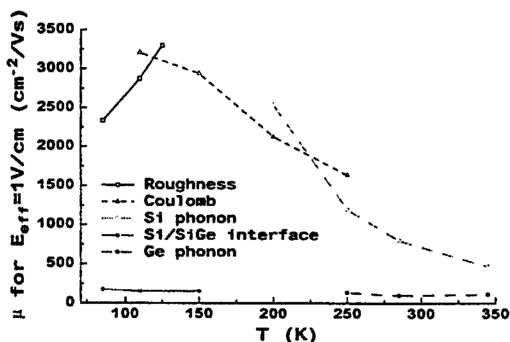

Fig 13: Mobility versus temperature (scattering mechanism) at E_{eff}=1V/cm. Open symbol results from [5], close symbol, our study.

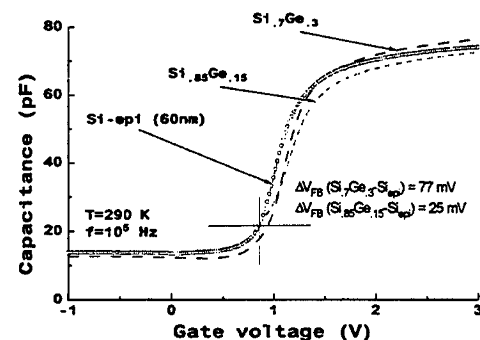

Fig 14: MOS capacitance of $Si_{.7}Ge_{.3}$, $Si_{.85}Ge_{.15}$ and Si-epi channel

Improvement of the Performance of a Gated Lateral Silicon Bipolar Device Through the Incorporation of SiGe

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I. INTRODUCTION

IN bipolar (npn) device technologies lateral pnp devices can be designed which can be used, for instance, as active loads, level shifters or complementary devices [1,2]. However, their performance is normally considerably inferior to the npn devices with which they share layers and processing. Within a BiCMOS process these transistors can be gated to produce 4 terminal devices, which have interesting characteristics. In the IBM SiGe technology these gated lateral transistors are Si devices and they do not use the SiGe layer [1]. In our simulations we wish to understand the basic operation of the devices and study how the incorporation of a Si-Ge layer could improve their performance.

II. DEVICE DESIGN AND OPERATION

Fig. 1 shows the schematic of the simulated lateral bipolar device, with top emitter (E), gate (G) and collector (C) contacts and a buried base (B) contact. The thicknesses of the layers were: gate oxide: 7 nm, Si cap: 5 nm, SiGe layer: 20 nm, n^- Si layer: 975 nm. The gate length was 0.8 μm. Two Ge profiles were examined. The 'uniform' profile had a 20% maximum Ge concentration over 15nm with a 2.5 nm grade to zero on each side. The 'triangular' profile had a maximum Ge concentration of 35 % with a 2.5 nm grade at the top and a 17.5 nm grade to zero after the maximum. The n^- doping of the layers was chosen to be 3 x 10^{16} cm^{-3}.

Depending on the choice of biases and currents at the contacts these devices can behave as predominantly field-effect transistors or as bipolar devices. Consider the case with no SiGe layer. Without the gate the device is a lateral bipolar transistor and there is no ambiguity about how it functions and what figures of merit should be used. With the gate present the situation is different. A negative bias on the gate assists the injection of holes into the region under it. This increases the output current but does not alter the base current. Thus it is the combination of the base and gate bias that controls the current.

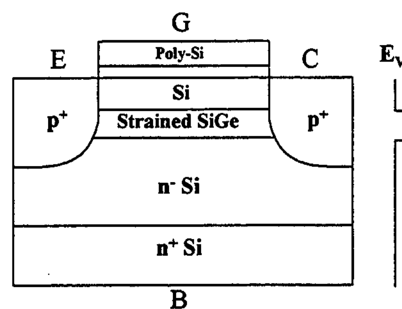

FIGURE 1. Schematic diagram of the structure of the simulated device. The diagram is not to scale. Right hand side shows the variation of the valence band energy. E: emitter, B: base, C: collector, G: gate.

If we re-label the emitter, gate and collector as source, gate and drain, and the base contact a body contact, then we can view the device as a MOS-FET, with a contact to vary the body voltage. In this view it is a DT-MOS device [3] i.e. a MOSFET with a variable threshold (*D*ynamic *T*hreshold). Such devices are possible in a standard CMOS technology [4]. The important difference in DT-MOS is that the body can be reverse-biased, meaning that current can flow from the body to the source. Standard MOSFET models such as the BSIM model do not allow the body to be forward-biased.

The apparent contradictory views of how to view the device have to be tempered with the observation that, below threshold, a FET exhibits bipolar-like behavior in that the current is mainly due to diffusion. To explain the characteristics of a purely silicon gated lateral bipolar transistor authors have used a model which involves a parallel combination of a bipolar transistor and a field effect transistor [1,2]. This approach can be justified theoretically by re-formulating [5] the

Pao-Sah theory [6] of FETs. This results in a decomposition of the Pao-Sah approach into a MOSFET charge-sheet model and a bipolar term. In the alternative theoretical treatment in [7] the approach is to view the device as a bipolar transistor. In this paper we use the language of bipolar devices in our examination of the characteristics of the simulated device, realizing that there is an alternate view as described above.

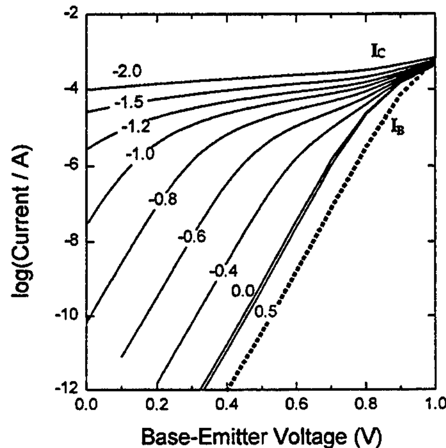

FIGURE 2. Simulated Gummel plot for a gated lateral bipolar device with no SiGe layer, for various gate voltages varying from -2.0 to 0.5 V. Solid lines: collector currents I_C, dotted line: base current I_B

III. SIMULATION RESULTS

We simulated the dc and ac behavior of the device in Fig. 1 using the Atlas/Blaze simulator [8] and incorporated a linear variation of the bandgap and hole mobility with Ge concentration. Other physical parameters and models were the default Silicon values. Fig. 2 shows simulated Gummel plots i.e. the variations of the collector current (I_C) and base current (I_B) with base-emitter bias (V_{BE}) for various gate voltages (V_G). For positive gate voltages the device behavior is similar to that of a normal bipolar transistor with the collector and base current curves being parallel over most of the base-emitter voltage range in the plot. This indicates that the gain is constant over a large current range. For increasing negative gate bias the collector current is proportional to the base current *only* at the lowest currents. The simulated results are similar to reported experimental results for Si gated lateral bipolar devices [1,2]. The simulated results for devices with SiGe layers give Gummel plots similar to those in Fig. 2.

It is more instructive to compare the differences in the gain of the devices rather than the Gummel plots. Thus Fig. 3 compares the dc gain (derived from the Gummel plots) for a device with the uniform SiGe layer with a reference device with only Si layers. The addition of SiGe shifts the gain curves to shift to lower V_{BE} values and increases the magnitudes at low V_{BE}.

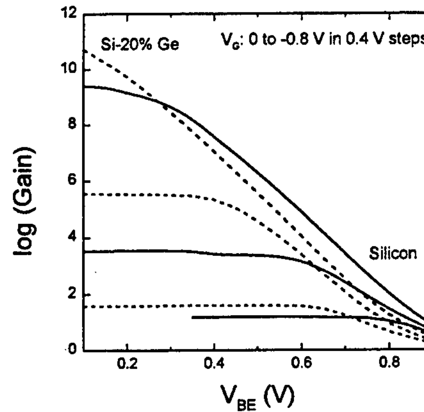

FIGURE 3. Simulated gain (I_C/I_B) of gated lateral bipolar devices as a function of the base-emitter bias V_{BE}, for a series of different gate biases from 0 V to - 0.8V. Dotted lines are for the case with a uniform SiGe layer and the solid curves for a reference device with only Si layers.

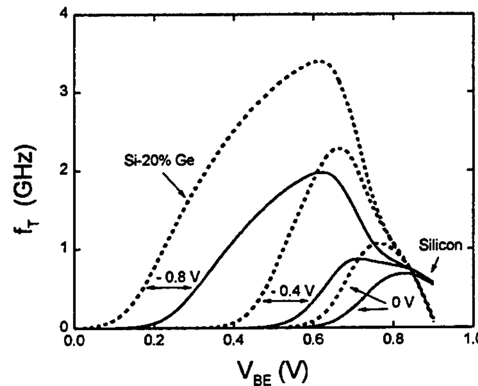

FIGURE 4. Simulated variation of the unity gain cut-off frequency, f_T, as a function of the base-emitter bias V_{BE}, for a series of different gate biases from 0 V to - 0.8V. Dotted lines are for the case with a uniform SiGe layer and the solid curves for a reference device with only Si layers.

The simulated high frequency performance for the devices is characterized by the unity-gain cut-off frequency, f_T. We have simulated the variation of f_T with V_{BE} i. e. along the curves of the Gummel plot (Fig. 2), applying the ac signal to the base. In Fig. 4 f_T increases with increasing negative V_G and the maximum in f_T moves to lower V_{BE}. The performance is improved by incorporating the uniform SiGe layer where the mobility is higher.

This improvement is related to the channeling of the hole current in the lower bandgap SiGe layer and the improved hole dynamics in SiGe. The channeling decreases the average transit time by suppressing the current that dips down into the n⁻ Si layer.

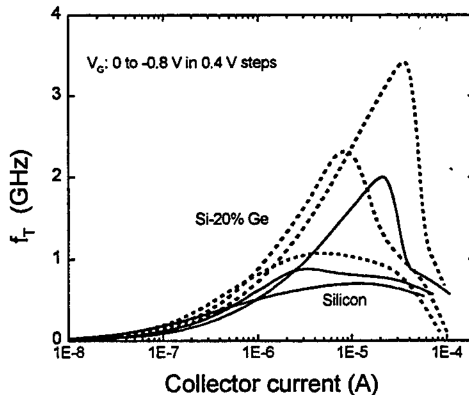

FIGURE 5. The same data as in Fig. 4 but plotted as a function of the collector current for the series of different gate biases from 0 V to - 0.8V. Dotted lines are for the case with a SiGe layer, the solid curves for a reference device with only Si layers. Lowest curves are for $V_G = 0$ V.

The shift of the maximum f_T to lower V_{BE} values does not mean a shift to lower collector currents. This is because with increasing negative V_G the gain and collector current also increase (Fig. 3). Fig 5 shows the same data as in Fig. 4 but now as a function of collector current. Now the maximum f_T occurs at increasing collector currents as the magnitude of V_G is increased. Thus the improvements in f_T do not come at lower power. The effect of the SiGe layer is to improve the device performance over a purely Si device through the channeling so that the holes in the SiGe layer benefit from the better mobility than in Si.

The total amount of Ge that can be incorporated in the SiGe layer is limited by the strain that the crystal can withstand without relaxing. Within these limits, however, we can modify the device performance by changing the Ge profile. Since mobility increases with Ge content, it should be advantageous to have a higher Ge content over a smaller distance. So, for comparison, we have simulated a device with the identical geometrical structure but with a triangular SiGe profile. (The 'uniform' and 'triangular' profiles have the same integrated amount of Ge.) The high frequency performance improves by altering the Ge profile (Fig. 6). The improvement by including the uniform SiGe layer to the Si device is reinforced by altering the Ge profile to a triangular one, to benefit from the channeling of the current even more. Again although the f_T maximum shifts to lower V_{BE} values with V_G, it is not to lower currents.

Fig. 7 shows the channeling of the holes by the SiGe layer. The Ge profile used was the 'uniform' case. The cross section of the normalized total hole current, at a point under the middle of the gate, shows the channeling effect is maximum near the gated top surface. This is similar to the case for a SiGe FET. The current that is maximum at the top of the SiGe layer would occur at the Si/SiO_2 interface in a purely Si device. The holes are kept away from the Si/SiO_2 interface because of the reduced bandgap in the SiGe, which appears nearly all as an offset in the valence band. Altering the Ge profile to a triangular one accentuates this feature even more.

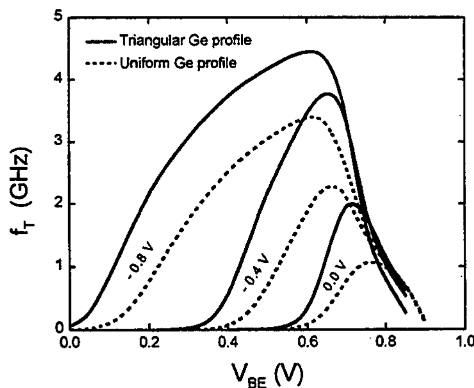

FIGURE 6. Similar to Fig. 4 but now the comparison is between devices incorporating a SiGe layer with the same integrated Ge content but with different Ge profiles.

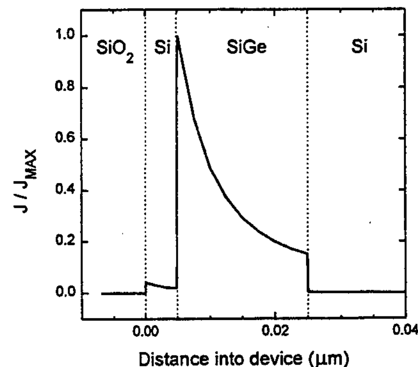

FIGURE 7. Simulated profile of the normalized lateral hole current density under the middle of the gate, showing the channeling of the current by the 20 nm SiGe layer. Ge profile was the uniform case : 20% Ge grade to zero over 2.5 nm on each side.

IV. CONCLUSIONS

Incorporating a SiGe layer into a lateral bipolar transistor will improve the dc and ac performance, because of the channeling effect of the SiGe layer and its better electrical properties. In particular f_T can be improved by a factor of 2-3 and a triangular Ge profile is preferable to a uniform Ge layer design.

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Effects of Channel Positioning on Low Frequency Noise in Si/Ge MOSFETs

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1.0 Introduction

It is known that the carrier mobility, μ, in bulk channel MOSFETs is significantly higher than that in surface channel devices. This is attributed to the suppression of surface scattering and scattering on charged interfacial oxide states. In p-type Si/Ge MOS devices the channel position coincides with the location of the Si/Ge layer in the substrate and can be, therefore, imposed in fabrication.

The purpose of this work is to examine the consequences of the channel positioning on the low frequency noise, LFN, properties of Si/Ge channel MOSFETs. As the arguments used for the μ increase with the channel shift away from the interface should also apply to the LFN, we expected the devices with higher μ to be also less noisy. Another interesting aspect for noise studies in SiGe MOSFETs is that of the noise origin. Quite generally, the LFN is generated by two distinct mechanisms (i) of mobility fluctuations, Δμ (due to scattering) and (ii) of carrier number fluctuations, Δn, (that originate from capture/release phenomena, involving oxide traps and/or near-interface states). Both mechanisms result in a 1/f-type noise and one of the key issues in the LFN studies is that of the origin of the LFN in various systems. In the MOSFET a relative contribution of either of the mechanisms should depend on the channel position, as more of the channel/interface charge exchange is expected in surface-channel devices. The Si/Ge MOSFET is therefore a very attractive object for the LFN research.

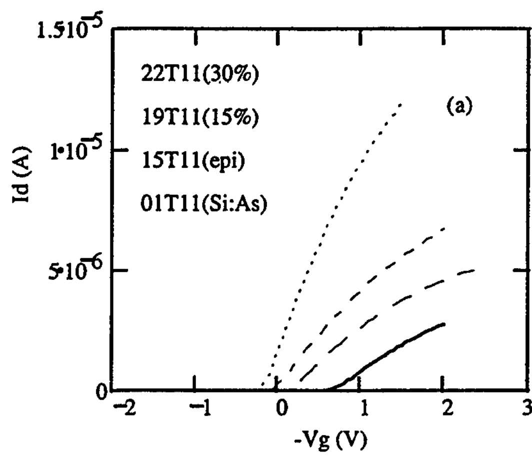
2.0 Devices studied

For the purpose of this work, we used 0.18μm (drawn) MOSFETs whose architecture and fabrication has been described elsewhere [1]. Several transistor batches with different channel architectures were used: (i) conventional, As (arsenic) - implanted, (ii) As-implanted + intrinsic Si epi layer (30nm thick), (iii) As-implanted + multilayer epitaxial stack consisting of: an intrinsic Si buffer, a Si/Ge (15 or 30% Ge) strained layer, and an intrinsic Si layer. Throughout this study, we used devices having the width, W, equal to 10μm and length, L, equal to 10μm. They devices are listed in Table I and their architecture is illustrated in Fig. 1, for all options, with enumeration of key points of the process used in their fabrication. Figure 2 shows a TEM photograph of a typical 0.18μm gate MOSFET thus obtained. An excellent oxide uniformity is to be noted.

Table I

Code name (comp)	Process key points; Max mobility (cm^2/Vs)
01T11 (Si:As)	As impl. 120keV, $1.2x10^{13}cm^2$ μ=65
15T11 (Epitaxial Si)	As + Epi Si, n_i 30nm; μ=90
19T11 (15% Ge)	As + Epi Si + 15% Si/Ge Epi; μ=120
22T11 (30% Ge)	As + Epi Si + 30% Si/Ge Epi; μ=255

Device characteristics and process key points



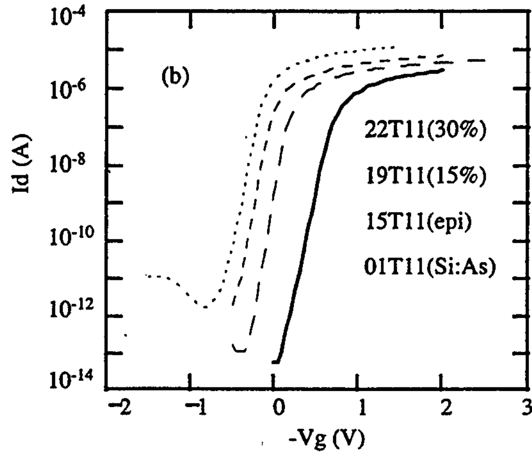


FIGURE 3. Transfer characteristics for devices with various architectures. The curves and their respective labels are in the descending order. $V_d = 50mV$.

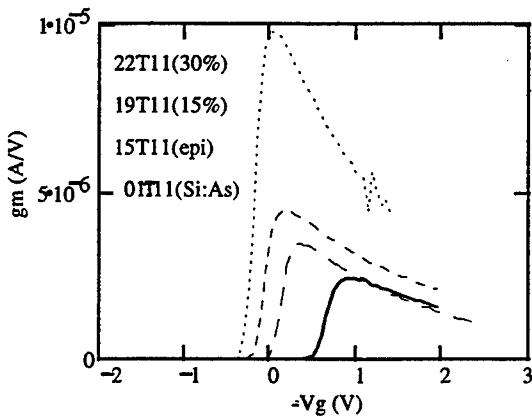


FIGURE 4. Variation of the transconductance g_m with gate voltage V_g for various MOSFET architectures.

4.2 Noise Data

Typical PSD *versus* I_d data for the set of devices listed above, obtained at f=10Hz in the ohmic region (V_d=50mV) is presented in Fig. 5. A nearly quadratic current dependence is observed, as expected. The less noisy are the epitaxial channel and the 15%Ge channel devices. The standard (arsenic-implanted) MOSFET is slightly noisier, but much less than the 30% Ge channel device. Contrary to our initial expectations, the LFN level in the devices, exhibiting the strongest μ increase, characteristic for the buried-channel architecture (Table I) was found to the highest. We attribute this effect to the appearance of process-generated defects in Ge-rich structures.

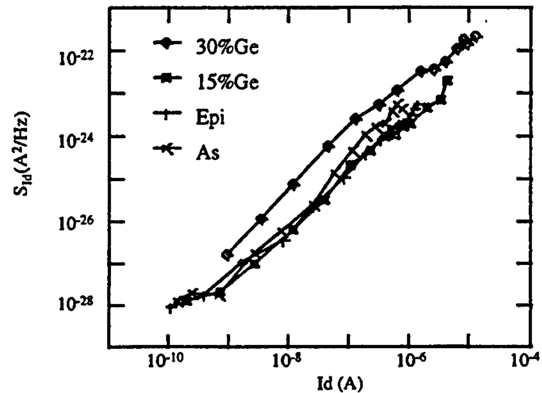


FIGURE 5. Variation of drain current PSD *versus* drain current for devices with various architectures.

A detailed diagnosis of the origin of noise sources is further carried out as outlined in [4]. It involves analyzing the normalized S_{Id}/I_d^2 as a function I_d. Figures 6a-6d show the evolution of S_{Id}/I_d^2 with the device technology. The $1/I_d$ behavior observed at low I_d is representative for the Hooge mobility fluctuations, whereas the shoulders appearing at intermediate I_d values originate from the onset of carrier number fluctuations [4].

In order to extract relevant noise parameters associated with each model, the noise data have been fitted with an expression combining the contributions of the carrier number and mobility fluctuations to the drain current noise, given, respectively by Eqs (1) and (2). The best fitting parameters for all the device architectures are listed in Table II (The Hooge parameter was found to be around 10^{-5} in all cases). For the arsenic-doped

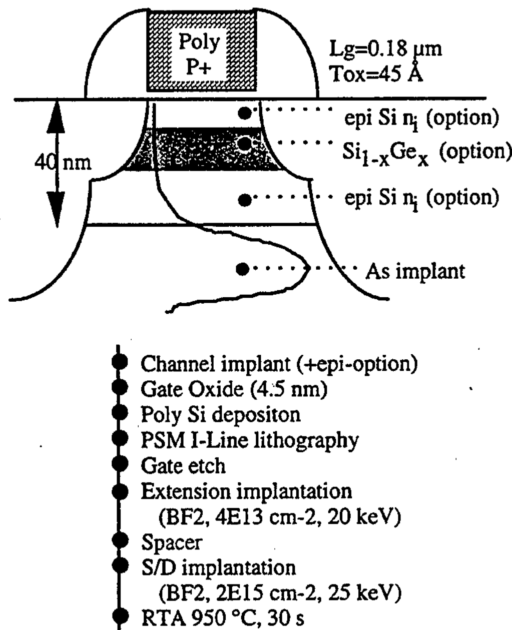


FIGURE 1. Si/Ge channel MOSFET (schematic diagram) a and key points of the device fabrication process flow.

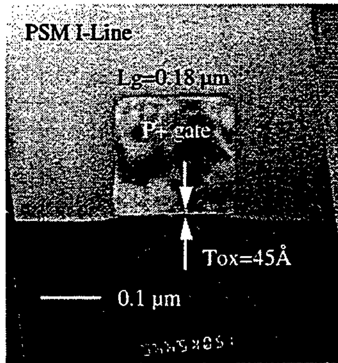


FIGURE 2. Si/Ge channel MOSFET (TEM picture)

3.0 Noise in drain currents

The quantity of interest for noise studies in MOSFETs is a normalized power spectral density, PSD, of drain current, I_d, fluctuations, denoted as S_{Id}/I_d^2.

The carrier mobility ($\Delta\mu$, or Hooge [2]) fluctuations are expected to prevail in buried channel devices and Δn fluctuation in surface-channel devices, as mentioned above. The Δn-related S_{Id}/I_d^2 can be expressed through the charge fluctuations at the interface or its vicinity. Denoting the total surface trap density by N_{st}, assuming that the gate-to-channel capacitance is dominated by that of the gate oxide, C_{ox}, and using the known McWhorter's [3] formalism, we obtain [4],

$$S_{Id}/I_d^2 = [q^2kTN_{st}/(WL\,C_{ox}^2f)](g_m/I_d)^2, \quad (1)$$

where g_m is the channel transconductance. For a fixed frequency, f, the factor in the square bracket of Eq. (1) is a constant.

For the $\Delta\mu$ model, the normalized PSD can be shown [2] to be inversely proportional to the total number of carriers thus,

$$S_{Id}/I_d^2 = q\alpha/(WLQ_if) = q\alpha V_d\mu_{eff}/L^2I_d, \quad (2)$$

where α is the Hooge parameter [2], usually comprised between 10^{-7} and 10^{-5}. The channel inversion charge Q_i, in Eq. (2) is evaluated for the ohmic region, through I_d, and drain voltage V_d and the effective mobility μ_{eff}.

Equations (1) and (2) give qualitatively different I_d behavior of the normalized LFN PSD. This will be further used for the diagnostics of noise sources in the discussion of the results.

4.0 Experimental Results

4.1 Static Data

Figure 3 shows typical static transfer characteristics for various types of MOSFETs listed in Table I. Satisfactory sub-threshold region behavior should be noted. Figure 4 shows g_m *versus* V_g dependence for the same set of devices. A dramatic increase of the maximum g_m in Ge/Si channel devices results from the increase in μ when the channel is shift away from the interface. For a discussion of other static data reference [1] should be consulted.

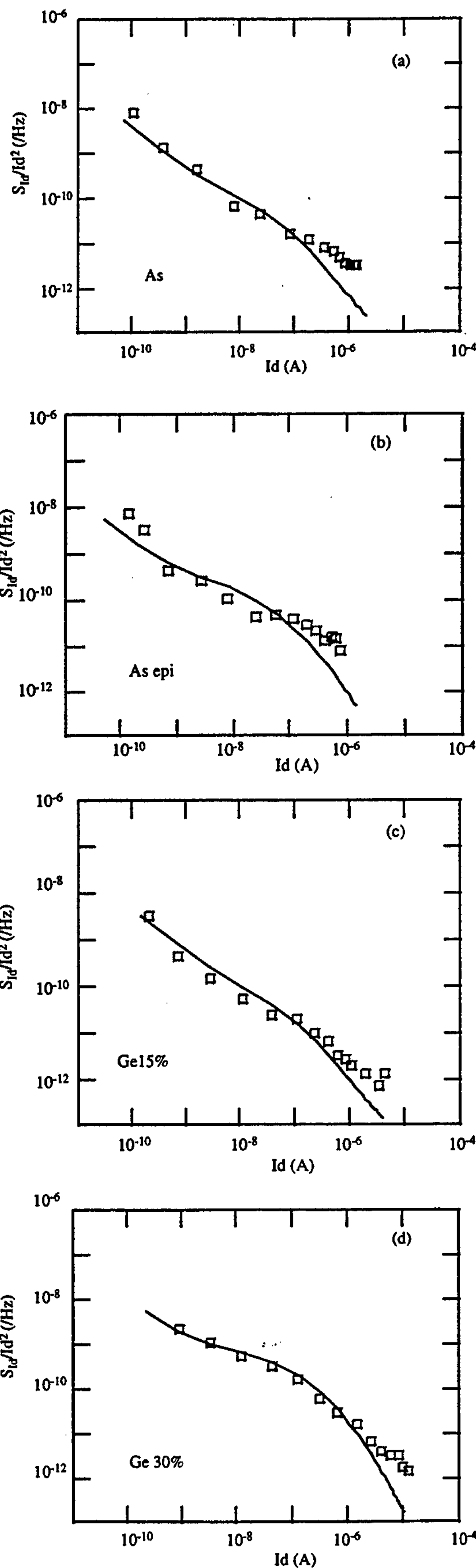


FIGURE 6. S_{Id}/I_d^2 *versus* drain current I_d for devices with various architectures (points: data; line: fit). a: 01T11(Si: As); b: 15T11(Si Epi); c: 19T11(15%Ge); d: 22T11(22%Ge).

Table II

Device code Channel	01T11 Si:As	15T11 Si Epi	19T11 15% Ge	22T11 30%Ge
N_{st} (10^8/eVcm^2)	9.1	2.0	1.7	18

Trap density extracted from LFN data for devices with various architectures.

devices, the surface trap density N_{st}, can be expressed through the bulk slow oxide trap density $N_t = N_{st}\,\lambda$, where λ is the tunneling attenuation constant [3]. Taking λ=1Å we obtain $N_t \approx 10^{17}$/eVcm^3, the value expected for the state-of-the-art gate dielectric MOSFETs. The surface trap density N_{st} is, however, lower in epitaxial and 15%Ge technology devices, than that in Si:As devices, implying a smaller Δn-related contribution to noise. The highest N_{st} and LFN in 30%Ge devices is attributed to the presence of process-induced neutral defects. They are located in the buffer or the interface regions, therefore contributing to the LFN but not to the channel carrier scattering.

5.0 Summary

No significant noise diminution in buried channel Ge/Si MOSFETs, all exhibiting the μ enhancement, is reported. However, the interface state density determined from the LFN in the 15% Ge devices is lower than that in standard devices. A significant noise increase reported in 30% Ge channel MOSFETs is attributed to the process-induced neutral defects.

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Impact of Poly-$Si_{0.8}Ge_{0.2}$-Gate Technology on Device Performance and Reliability

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Abstract
Poly-$Si_{1-x}Ge_x$ has recently been reported as a promising alternative CMOS gate material especially for application in submicron devices [1,2]. In this work, poly-$Si_{0.8}Ge_{0.2}$ and poly-Si gate capacitors with very thin gate oxide were fabricated. Device performance (poly-depletion effect (PDE), current drive) and reliability issues were assessed. It was found that both NMOS and PMOS poly-$Si_{0.8}Ge_{0.2}$-gated devices excel in current drive and resistance to PDE due to higher percentage of dopant activation [3] as compared to poly-Si-gated devices. Oxide reliability seems only to depend on oxide thickness and it was observed that the existence of Ge atoms at the poly/oxide interface does not degrade the oxide quality.

Introduction
New technical challenges emerge as the dimensions of semiconductor devices are continually being scaled to the deep sub-micron regime for higher levels of integration and performance. For process simplicity, the poly-Si gates are typically doped after patterning by the same ion implantation step used to form the source-drain regions. However, this doping method does not yield sufficiently high active dopant concentration, especially at the critical gate-dielectric interface, leading to problems associated with depletion of the gate under strong inversion bias [4]. The energy-band-bending in the poly-Si induces a voltage drop across the gate, which degrades MOSFET current characteristics as well [5]. Clearly, a means to achieve high active doping concentration in the gate without raising other issues (like cost and implantation damage) becomes necessary.
Currently, some CMOS processes have implemented silicon-germanium ($Si_{1-x}Ge_x$) as an ultra-shallow source/drain dopant diffusion source [6]. Poly-$Si_{1-x}Ge_x$ is also a promising alternative to poly-Si as a gate material due to its process compatibility and favorable electrical properties, such as lower sheet resistance, higher dopant activation rate, and tunable work function [1,3]. However, few detailed investigations have been carried out to consider the impact of a poly-$Si_{1-x}Ge_x$ gate on device performance and reliability.
In this work, poly-$Si_{0.8}Ge_{0.2}$-gate and poly-Si-gate MOS capacitors were fabricated. The specific Ge mole fraction was chosen to provide a high-activation rate [3] with small workfunction shift (found to be about 0.1V for PMOS, but negligible for NMOS). Both NMOS and PMOS CV characteristics for devices of different oxide thicknesses were obtained. Oxide reliability was measured in terms of T_{BD} (time-to-breakdown) and Q_{BD} (charge-to-breakdown). Comparisons were made between poly-$Si_{0.8}Ge_{0.2}$ and poly-Si MOS devices.

Experiment
NMOS and PMOS capacitors were fabricated on (100) p-type and n-type silicon wafers respectively with LOCOS isolation. After the definition of the active region, the channel implant (boron for NMOS and arsenic for PMOS) was performed through a 200Å sacrificial oxide. Wafers were then divided into twelve splits. Undoped poly-Si deposited at 600°C was applied to six of them with thermal gate oxide thicknesses of 35Å, 45Å and 65Å. Undoped poly-$Si_{0.8}Ge_{0.2}$ deposited at 550°C [7] (preceded by a thin Si adhesion layer of about 5Å) was applied to the other six groups which also had oxide thicknesses of 35Å, 45Å and 65Å. All gate films were deposited in a conventional LPCVD system with a final thickness targeted at 3000Å. Phosphorus was then implanted into three poly-Si and three poly-$Si_{0.8}Ge_{0.2}$ wafers at 60KeV, while boron was implanted into the other wafers at 20KeV. Gate-implant dosage of $3\times10^{15}cm^{-3}$ was used. After gate patterning, devices were annealed at 900 °C for 40min, followed by backside etching and finally a 400 °C forming gas anneal.

Result and Discussion
Figures 1 and 2 show the measured quasi-static CV curves of both poly-Si-gated and poly-$Si_{0.8}Ge_{0.2}$-gated devices for NMOS and PMOS capacitors, respectively. These devices feature different oxide thicknesses, but the same gate doping level. The following results are evident: 1) For both NMOS and PMOS poly-Si or poly-$Si_{0.8}Ge_{0.2}$ devices, the thinner the gate oxide, the more capacitance reduction in the inversion region. This is because a higher electric field will cause more depletion near the poly/SiO_2 interface. 2) Poly-$Si_{0.8}Ge_{0.2}$ devices

exhibit less capacitance reduction in the inversion region and therefore less poly-depletion effects (PDE). 3) As gate oxide becomes thinner, poly- $Si_{0.8}Ge_{0.2}$ devices significantly reduce PDE as compared to poly-Si. This is true for both N-channel and P-channel devices. 4) For phosphorus-doped gate, the flatband voltage (V_{FB}) shift between poly-Si and poly-$Si_{0.8}Ge_{0.2}$ gates is negligible, while for boron-doped gate, the shift is about 0.1V ($V_{FB,Si0.8Ge0.2} < V_{FB,Si}$). This observation is consistent with previous findings [1,8]. 5) No evident dopant-penetration is observed for both gate technologies in both NMOS and PMOS devices.

In order to predict the impact of PDE on current drive, the area under each CV curve was integrated from weak inversion into strong inversion to estimate the inversion charge density, Q_{inv}. The Q_{inv} ratio, ($Q_{inv,SiGe}/Q_{inv,Si}$) which is an indicator of the relative current of a poly-$Si_{0.8}Ge_{0.2}$-gated MOSFET compared to a poly-Si-gated MOSFET, is plotted vs. gate drive (V_g-V_t) in Figures 3 and 4. The ratio increases as (V_g-V_t) increases or as gate oxide thickness decreases.

Gate leakage current is plotted vs. stress voltage in Figures 5 and 6. NMOS devices with oxide thickness ~ 65Å (target) and PMOS devices with oxide thickness ~ 45Å (target) were measured for both gate technologies. As can be seen, the I_g-V_g characteristics are well predicted by the Fowler-Nordheim tunneling model. Leakage current shifts between the different gate technologies are simply due to small variations in oxide thickness. The actual oxide thicknesses as indicated in the Figures were extracted by fitting the data to the F-N model and were confirmed by optical measurement. There is no indication of stress-induced-leakage current (SILC) or damage for either poly-Si or poly-$Si_{0.8}Ge_{0.2}$ devices.

Reliability issues were also examined. Figures 7 and 8 illustrate the 10-year reliability projections for both gate technologies. Poly-$Si_{0.8}Ge_{0.2}$ devices were observed to endure higher V_g in NMOS but lower V_g in PMOS as compared to poly-Si devices. However, the difference in maximum V_g for 10-year lifetime (less than 0.1V) is believed to be due to the aforementioned variations in gate oxide thickness. This will lead to thicker oxide in NMOS and thinner oxide in PMOS for poly-$Si_{0.8}Ge_{0.2}$-gated devices, which is consistent with the findings from the I_g-V_g characteristics.

Time-to-breakdown (T_{BD}) is plotted as a function of 1/E where E is the electric field in the gate oxide. All curves feature linear dependence between T_{BD} and 1/E with similar slope values. Again, the difference between poly-Si and poly-$Si_{0.8}Ge_{0.2}$ devices is caused by variation in gate oxide thickness. Figures 11 and 12 illustrate charge-to-breakdown (Q_{BD}) as a function of 1/E. Similar Q_{BD} behavior was observed for both gate technologies. This also suggests that the oxide quality is not degraded in poly-$Si_{0.8}Ge_{0.2}$-gated devices.

Conclusion

Poly-$Si_{1-x}Ge_x$ is a promising CMOS gate material especially for application in submicron devices [1,2]. Device performance and reliability issues for poly-$Si_{0.8}Ge_{0.2}$-gated devices were reviewed. It was found that both NMOS and PMOS poly-$Si_{0.8}Ge_{0.2}$-gated devices excel in current drive and resistance to PDE due to higher dopant activation rates [3] as compared to poly-Si-gated devices. Oxide reliability seems only depend on oxide thickness and it was observed that existence of Ge atoms at the poly/oxide interface does not degrade the oxide quality.

Acknowledgment

This experiment was made possible with support through a NSF National Nanofabrication Users Network Grant.

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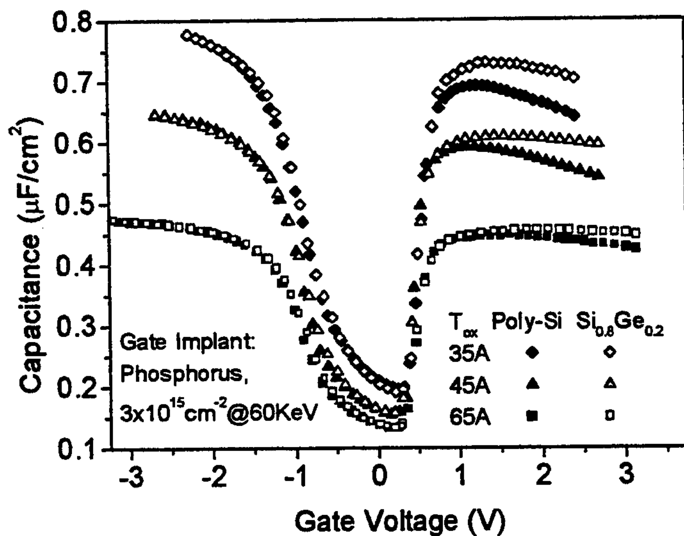

Fig. 1 Comparison of measured quasi-static CV curves for poly-Si and $Si_{0.8}Ge_{0.2}$ gate NMOS capacitors.

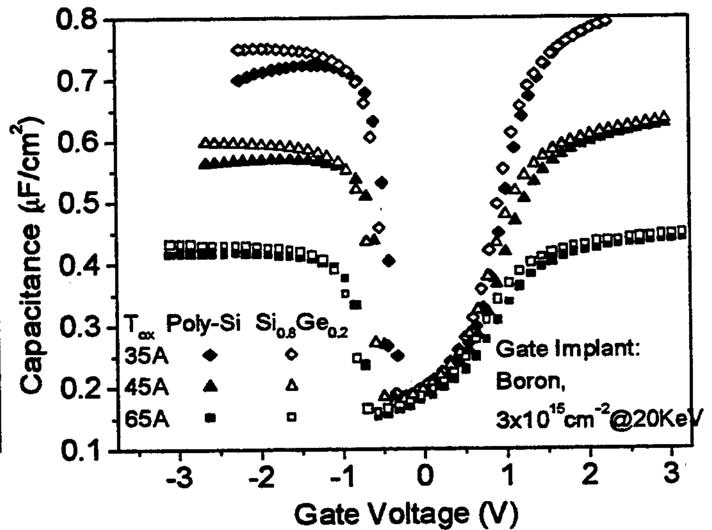

Fig. 2 Comparison of measured quasi-static CV curves for poly-Si and $Si_{0.8}Ge_{0.2}$ gate PMOS capacitors.

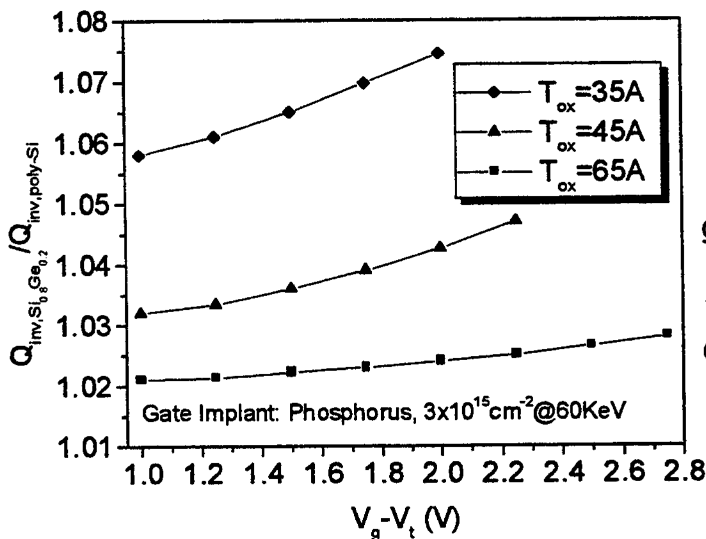

Fig. 3 NMOS inversion charge ratio ($Q_{inv,SiGe}/Q_{inv,Si}$) vs. (V_g-V_t) for various gate oxide thicknesses.

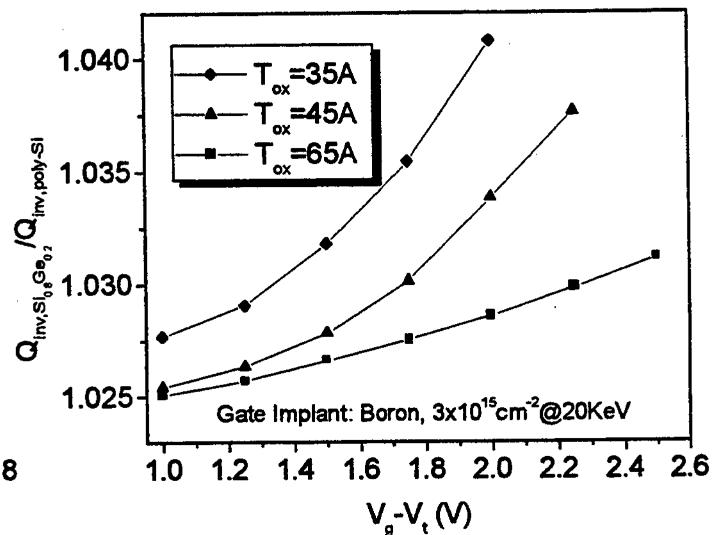

Fig. 4 PMOS inversion charge ratio ($Q_{inv,SiGe}/Q_{inv,Si}$) vs. (V_g-V_t) for various gate oxide thicknesses.

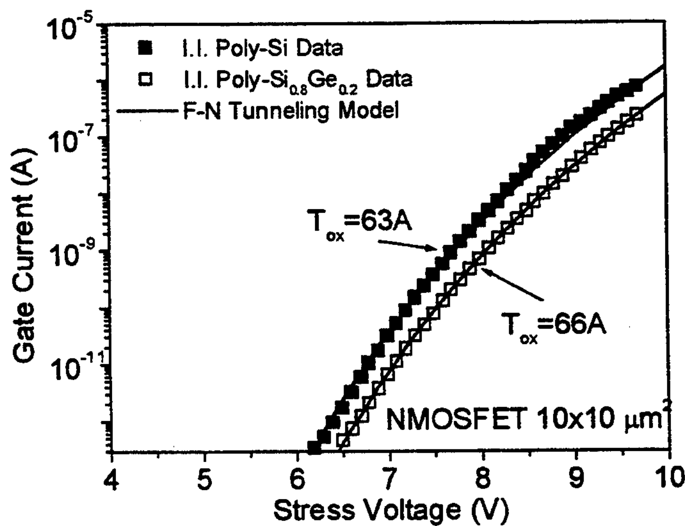

Fig. 5 Gate leakage current vs. gate voltage for poly-Si- and $Si_{0.8}Ge_{0.2}$-gated NMOS capacitors. T_{ox}≅65Å

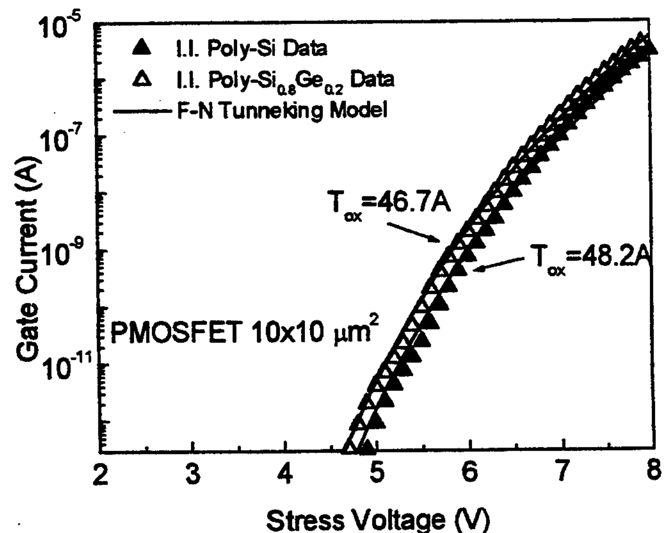

Fig. 6 Gate leakage current vs. gate voltage for poly-Si- and $Si_{0.8}Ge_{0.2}$-gated PMOS capacitors. T_{ox}≅45Å

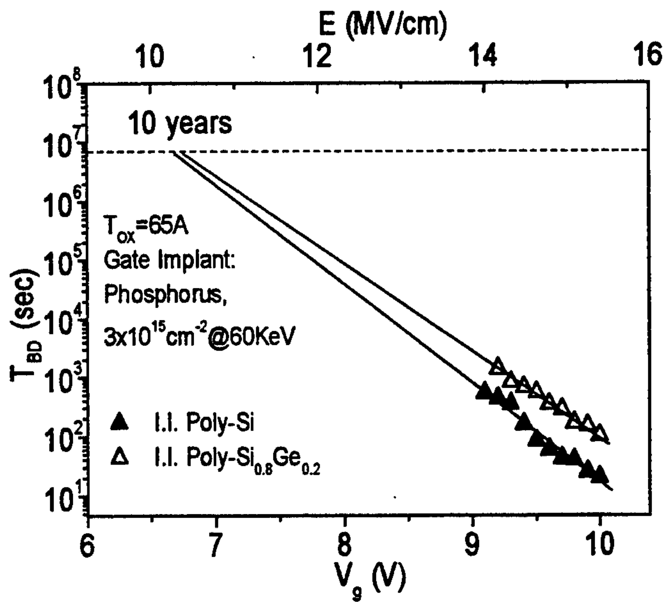

Fig. 7 T_{BD} vs. stress voltage and corresponding electric field for poly-Si- and $Si_{0.8}Ge_{0.2}$-gated NMOS capacitors.

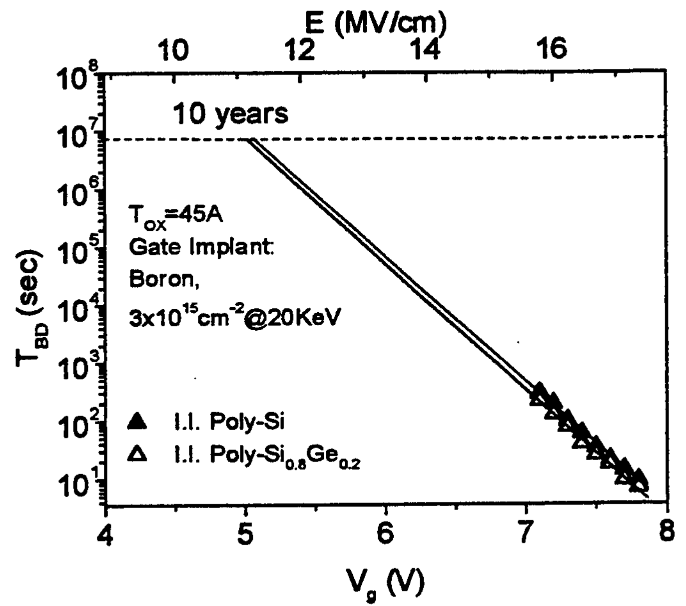

Fig. 8 T_{BD} vs. stress voltage and corresponding electric field for poly-Si- and $Si_{0.8}Ge_{0.2}$-gated PMOS capacitors.

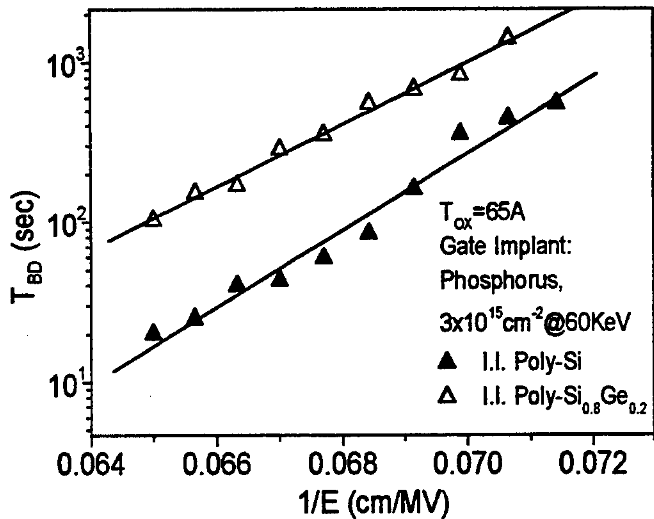

Fig. 9 T_{BD} as a function of 1/E for NMOS devices with different gate technologies.

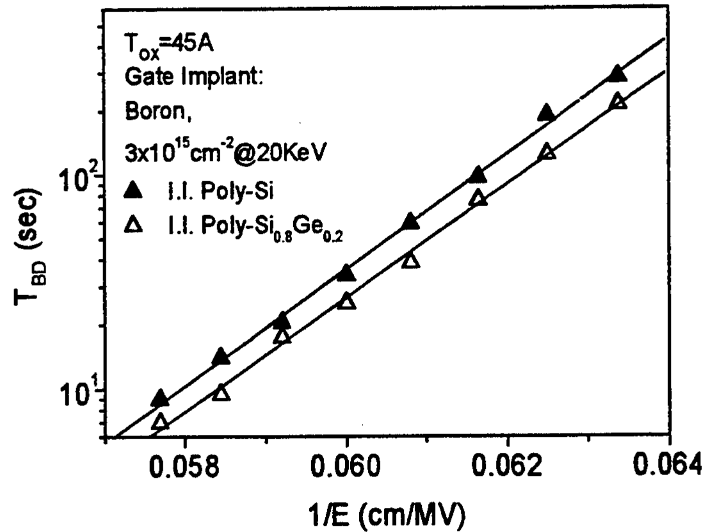

Fig. 10 T_{BD} as a function of 1/E for PMOS devices with different gate technologies.

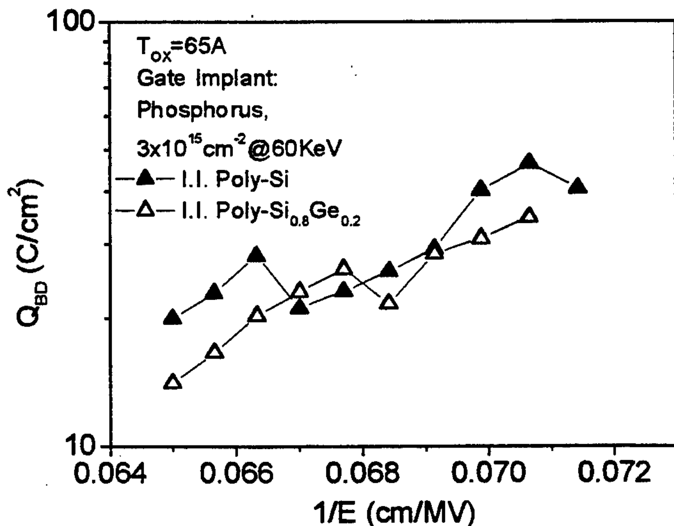

Fig. 11 Q_{BD} as a function of 1/E for NMOS devices with different gate technologies.

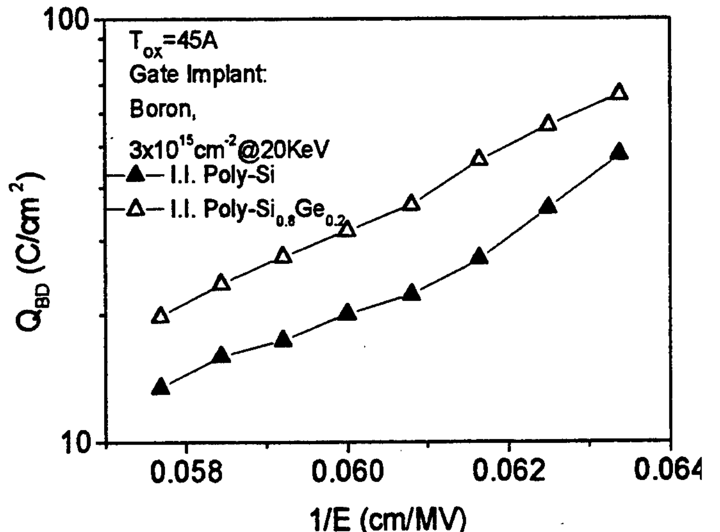

Fig. 12 Q_{BD} as a function of 1/E for PMOS devices with different gate technologies.

Current calculation of a submicron Si/SiGe heterojunction MOSFET

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Abstract-An analytical expression for the current of a Si/SiGe heterojunction MOSFET is derived and is used to demonstrate the advantages of this novel device. In this device the source/channel homojunction is replaced by an heterojunction to decrease the DIBL effect. The gate action on a lowly doped SiGe region of the source, near the channel, is used to lower the effective barrier for the carriers and to cause a large current to flow in the on-state of the MOSFET. The potential of the channel and of the SiGe source region is calculated from the Poisson equation. The continuity equation and drift-diffusion equation are used to calculate the carrier densities. Thermionic emission is used as a boundary condition at the heterojunction between source and channel.

1. Introduction

The development of heterostructure technology is one of the most active research areas [1]. The use of heterojunctions in semiconductor devices like bipolar transistors has proven its effectiveness in increasing the performance of these devices. Especially silicon germanium, which is compatible with a mainstream Si-technology, has gained a large interest. The use of SiGe in MOSFETs for reducing the short channel effect shows promising results [2,3]. The heterojunction pMOSFET [4], presented in this paper, uses a strained SiGe/Si structure to create a heterojunction between source and channel to reduce the DIBL effect. For the nMOSFET a SiGe/Ge heterojunction is to be used. Figure 1 shows the heterojunction pMOSFET. In a lateral homojunction MOSFET with very short channel lengths high off-state currents will flow due to DIBL. The off-state current is exponentially dependent on the source/channel barrier, formed by the built-in potential. If the channel length of the MOSFET is scaled down the electric field of the drain will influence the barrier at the source and will lower this barrier. In a heterojunction the barrier is a material constant, independent of channel length. It changes little with temperature and it cannot be changed by bias. The off-state current of the heterojunction MOSFET will be low. However, the ratio between on-state current and off-state current must be as high as possible. The gate action on a lowly doped SiGe source layer, just before the channel, is used to move the valence band (pMOSFET) or the conduction band (nMOSFET) in such a way that the effective barrier for the carriers is lowered. Figures 2, 3 and 4 show the valence band at different bias conditions. A lowering of the effective barrier can be seen. This barrier is defined as the difference between the hole quasi-Fermi level in the source and the lowest channel valence band (this is at the heterojunction interface).

In this paper the current expression for this device is derived and is used to discuss the advantages. The calculations are made for the pMOSFET but in an analogous way this can be done for the nMOSFET. In section 2 we derive the basic equations for the calculation of the potential, carrier and current densities. In section 3 the current equation is derived for three different doping situations of the SiGe layer. These equations are discussed in section 4 and in section 5 a summary is given.

2. Basic equations

Wherein a lateral homojunction MOSFET only the channel potential has to be considered, in this novel device the potential in the lowly doped SiGe source is a very important parameter. The influence of the gate potential on this region will lower the barrier and cause a large current to flow in the on-state. The potential can be calculated by solving the 2D Poisson equation. The electrostatic potential is defined as a local vacuum level which represents the potential of an electron at rest and free from the influence of the crystal potential [5]:

$$\frac{d}{dx}(\varepsilon\frac{d\psi}{dx})+\frac{d}{dy}(\varepsilon\frac{d\psi}{dy})=-q(p-n+N_D^+-N_A^-)\ (1)$$

1

The drift-diffusion equation is given by:

$$J_p = q\mu_p\left(-p\frac{d}{dx}(\psi + \chi) - V_{th}\frac{dp}{dx}\right) + q\mu_p\left(-\frac{p}{q}\frac{dE_g}{dx} + V_{th}p\frac{d\ln N_v}{dx}\right) \quad (2)$$

The hole continuity equation:

$$\frac{\partial J_p}{\partial x} = 0 \quad (3)$$

The thermionic boundary condition at the heterojunction interface is given by [6]:

$$J_{TE} = A_2^*\eta\left(\frac{p_2(0+)}{N_{v2}} - \frac{p_1(0-)}{N_{v1}}\exp\left(\frac{-E_B}{kT}\right)\right)$$
$$\eta = T^2\left(1 - \left(1 - \frac{m_{h1}^*}{m_{h2}^*}\right)\exp\left(\frac{-E_B}{kT\left(\frac{m_{h2}^*}{m_{h1}^*} - 1\right)}\right)\right) \quad (4)$$

where A_2^* represents the Richardson constant and E_B the barrier height. The subscript 1 is used for the SiGe region and subscript 2 for the Si channel region.

3. Calculation of the current expression

Starting from the Poisson equation the potential of channel and lowly doped SiGe region can be calculated. Two natural lengths λ_1 and λ_2 have to be considered. The model used for the dielectric constant, bandgap, density of states and mobility of SiGe can be found in [7]. Figure 5 shows the comparison between the analytical calculation for the potential and the results obtained by numerical simulation with the 2D device simulator PRISM [8] for the valence band of the heterojunction pMOSFET with no bias applied.

The continuity equation together with the modified drift-diffusion equation is used to calculate the carrier density and current density, using thermionic emission as a boundary condition at the hetero-junction interface (here taken as x=0). Using integral representations the current expression can be written as follows (eq. 5):

$$I_p = A_2^*\eta W\frac{N_{SD}}{N_{v1}}\exp\left(\frac{-V_{bi1}}{V_{th}}\right)\exp\left(\frac{-E_B}{kT}\right)\left(\exp\left(\frac{V_{DS}}{V_{th}}\right) - 1\right)\vartheta$$

$$\vartheta = \int_0^{\infty}\frac{\exp\left(\frac{-\psi_2(0,y)}{V_{th}}\right)dy}{1 + \frac{A_2^*\eta}{qV_{th}}\frac{1}{N_{v2}}\exp\left(\frac{-\psi_2(0,y)}{V_{th}}\right)\int_0^L\frac{1}{\mu_2}\exp\left(\frac{\psi_2(x,y)}{V_{th}}\right)dx}$$

where N_{SD} represents the source/drain doping, W the width of the transistor and V_{bi1} the built-in potential between lowly and highly doped source region.

4. Discussion

The current equation derived in the previous paragraph can be written in a more compact form. When the lowly doped SiGe-layer is a n-type layer, the built-in potential is given as $V_{bi1} = V_{th}\ln\left(\frac{N_{SD}N_1}{n_{i1}^2}\right)$ where N_1 represents the doping of the SiGe region. Using a n-type layer inside the source leads to a somewhat different transistor concept than the usual lateral pMOSFET where the source and drain are p-type doped. Evaluation of the different terms leads to the following form of the current equation (eq. 6):

$$I_p = A_2^*\eta W\frac{1}{N_{v1}}\frac{n_{i1}^2}{N_1}\exp\left(\frac{-E_B}{kT}\right)\left(\exp\left(\frac{V_{DS}}{V_{th}}\right) - 1\right)\vartheta$$

$$\vartheta = \int_0^{\infty}\frac{\exp\left(\frac{-\psi_2(0,y)}{V_{th}}\right)dy}{1 + \frac{A_2^*\eta}{qV_{th}}\frac{1}{N_{v2}}\exp\left(\frac{-\psi_2(0,y)}{V_{th}}\right)\int_0^L\frac{1}{\mu_2}\exp\left(\frac{\psi_2(x,y)}{V_{th}}\right)dx}$$

Comparison of the equation with the current expression of a lateral pMOSFET shows that some additional terms have to be taken into account: the ratio of the hole density of states, the exponential dependence on the barrier height, the doping and intrinsic concentration of the SiGe source layer. A higher molefraction will lead to a higher barrier but at the same time will lead to a higher intrinsic concentration and a lower hole density of states. It is to be expected that these effects will compete with each other and will not necessarily lead to a decrease in off-state current with increasing molefraction. Evaluation of the integral term shows that this term will only slightly decrease with increasing molefraction. When the barrier is

lowered, the increased intrinsic concentration and the decreased hole density of states will lead to a higher on-state current, but it will also increase the voltage at which the device will reach its on-state.

In case of a p-type doped SiGe-layer the situation is a bit different. The built-in potential is given by $V_{bi1} = V_{th}\ln\left(\frac{N_{SD}}{N_1}\right)$. The current equation is then given as follows (7):

$$I_p = A_2^*\eta W\frac{1}{N_{v1}}N_1\exp(\frac{-E_B}{kT})(\exp(\frac{V_{DS}}{V_{th}})-1)\vartheta$$

$$\vartheta = \int_0^{\infty}\frac{\exp(\frac{-\Psi_2(0,y)}{V_{th}})dy}{1+\frac{A_2^*\eta}{qV_{th}}\frac{1}{N_{v2}}\exp(\frac{-\Psi_2(0,y)}{V_{th}})\int_0^L\frac{1}{\mu_2}\exp(\frac{\Psi_2(x,y)}{V_{th}})dx}$$

There is no dependence on the intrinsic concentration anymore. One can expect a low off-state current if the doping of the SiGe-layer is not too high. However, the on-state current will be low. Figure 6 shows the dependence of the off-state current on the molefraction for both cases. In case of a n-type layer the off-state current goes up with increasing molefraction, but in case of a p-type layer the off-state current goes down with increasing molefraction. A comparison with a simplified form of eq. 6 and 7 where the term 1 in de denominator is omitted, is also made.

The dependence on the doping concentrations is quite important. A higher channel doping means a higher barrier because the Fermi-level lies closer to the conduction band. In case of a n-type SiGe-layer, a higher doping concentration in this layer will lead to a Fermi-level, lying closer to the conduction band and thus, a lower off-state current, but also lower on-state current. At the same time, the higher SiGe-doping will counteract the higher intrinsic concentration. In case of a p-type SiGe source layer an increase in doping concentration of that layer will lead to an increase in off-state current. The Fermi level lies close to the valence band. At the same time, however, the on-state current will be higher.

A compromise between both cases is the use of an intrinsic SiGe-layer. The current expression in that case will be (8):

$$I_p = A_2^*\eta W\frac{1}{N_{v1}}n_{i1}\exp(\frac{-E_B}{kT})(\exp(\frac{V_{DS}}{V_{th}})-1)\vartheta$$

$$\vartheta = \int_0^{\infty}\frac{\exp(\frac{-\Psi_2(0,y)}{V_{th}})dy}{1+\frac{A_2^*\eta}{qV_{th}}\frac{1}{N_{v2}}\exp(\frac{-\Psi_2(0,y)}{V_{th}})\int_0^L\frac{1}{\mu_2}\exp(\frac{\Psi_2(x,y)}{V_{th}})dx}$$

There is only a linear dependence of the current on the intrinsic concentration. The transistor can be easily put in its on-state because the gate action on the intrinsic layer is much higher then on a doped layer.

5. Summary

An analytical model for the current of a SiGe heterojunction MOSFET was derived. Evaluation of the expression shows a large difference in behaviour between devices with p-type and n-type SiGe-layer. The p-type layer shows off-state currents going down with increasing molefraction. However, the on-state current of the p-type case is low. The n-type case shows higher on-state currents but for the same molefraction also higher off-state currents. One can conclude that a compromise between both cases will lead to an optimal solution. From the analytical point of view, the use of an intrinsic SiGe-layer is the optimal case. There is only a linear dependence on the intrinsic concentration and the voltage at which the transistor is in its on-state can be much lower.
From these considerations it can be seen that the most important parameters in the design of the transistor are (this for a particular channel length): the molefraction of the SiGe layer, length and doping of the lowly doped layer, doping of source and drain regions and the oxide thickness. These parameters determine the barrier height and the voltage at which the transistor can be put in its on-state. The derived equations are an important tool for determining the optimal design parameters.

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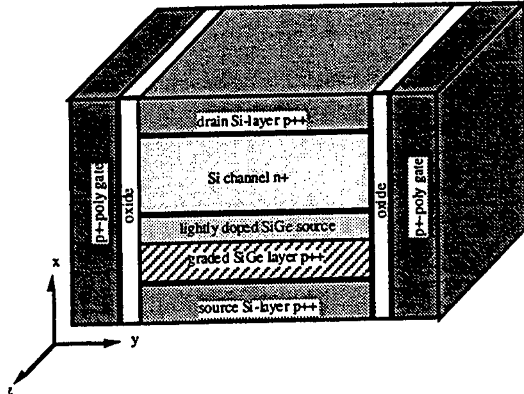

Figure 1: schematic view of the heterojunction pMOSFET

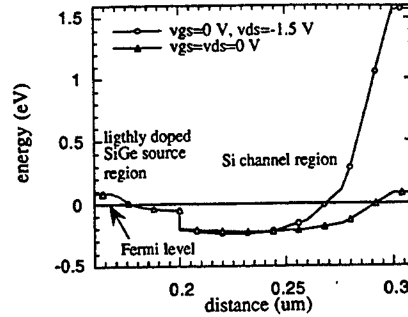

Figure 2: valence band at no bias and a drain bias of -1.5 V

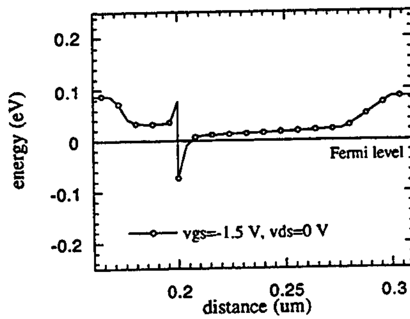

Figure 3: valence band at a gate bias of -1.5 V

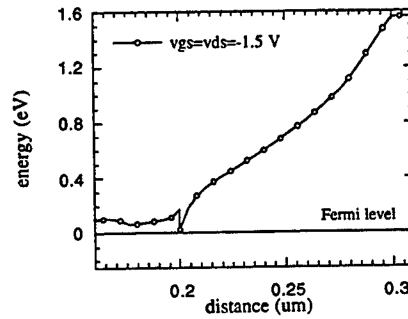

Figure 4: valence band at a gate and drain bias of -1.5 V

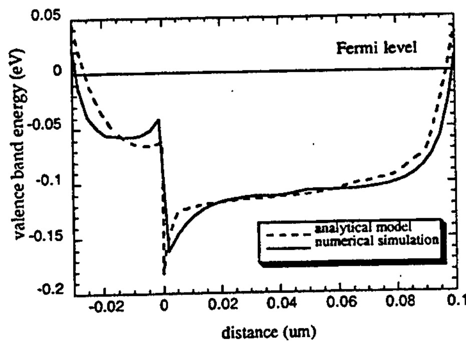

Figure 5: comparison between simulation and analytical model

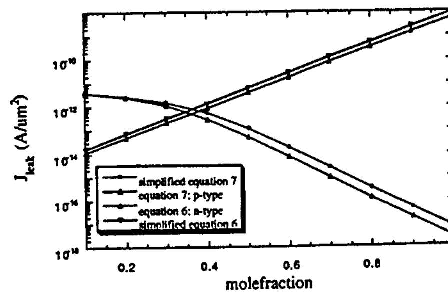

Figure 6: leakage current as a function of the SiGe molefraction

4

A New Carrier Mobility Model Using the Second and the Fourth Moment of the Boltzmann Transport Equation

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Abstract

We propose a mobility as a function of the average energy (W) and the average of energy square ($<\varepsilon^2>$) of carriers which are the second moment and the fourth moment of the Boltzmann Transport Equation(BTE), respectively. It is shown that the fourth moment can be expressed by the lower moments and the new mobility model can be adopted by the conventional Hydrodynamic(HD) Device Simulator without more computational burden and convergence problem.

1. Introduction

As the size of the semiconductor devices becomes smaller, the carrier system cannot obtain the static energy corresponding to the fast changing electric field. The HD model ,therefore, which considers local energy becomes popular instead of Drift-Diffusion(DD) model based on the local field. But even the local energy dependent mobility model loses its validity under various situations(steeply decreasing field region near the drain of MOSFET devices as an example) and various models considering non-locality have been proposed by several authors[1][2][3].

Fig.1 shows a typical example of the energy distribution and mobility distribution in a n-i-n diode obtained by a Monte Carlo(MC) simulation. We use the 1-dimensional MC-Poisson simulator which has the isotropic two band model and physical parameters adopted from Ref. [4]. It can be seen that at the same average energy points (A,B for example) , carrier mobilities are quite different. In this study, we will show that the carrier mobility can be well modeled as a function of both the local average energy (W) and the average of energy square ($<\varepsilon^2>$) using MC simulations. Also, we will show that the average of energy square can be parametrized by the lower moments, such as W, average velocity(V), average momentum(P) instead of solving the fourth moment HD equation and that the modified model implemented in the HD Simulator produces better result than the conventional model.

2. Mobility modeled by the effective average energy (W_{eff})

The physical reason for different mobilities and impact ionization rates for same average energy(W) is that carrier system may have different distribution functions for each case. Sonoda et al. showed that the impact ionization generation rate can be different at the two points where W is same[5] and proposed the impact ionization model using the average energy ,W, obtained by the second moment and the average of energy square , $<\varepsilon^2>$, obtained by the fourth moment of the Boltzman transport equation. We adopt a similar approach for modeling of the carrier mobility. A parameter ξ is defined to model the deviation from the ideal Maxwellian Distribution as follows[5],

$$\xi = \frac{\sqrt{\frac{3}{5}<\varepsilon^2>}}{W} \qquad (1)$$

Fig.2 shows the ξ extracted from the MC Simulation for the homogeneous bulk(ξ_h) case. The value of ξ is almost 1 at low energy (i.e. ideal Maxwellian distribution at low energy) and

decreases as the energy increases , which is a similar tendency reported in [5]. This result implies that even in the homogeneous bulk, the energy distribution is not Maxwellian at high field (so the high energy). Based on this result, we define another parameter Γ which is a barometer showing the deviation from the homogeneous bulk as,

$$\Gamma = \xi - \xi_h = \frac{\sqrt{\frac{3}{5}}\left(\sqrt{<\varepsilon^2>} - \sqrt{<\varepsilon^2>_h}\right)}{W} \quad (2)$$

where $<\varepsilon^2>_h$ is $<\varepsilon^2>$ value in homogeneous bulk .

The difference in the distribution function which causes the mobility difference for the same W points may be reflected by the parameter Γ.

Fig. 3 shows relationship between $\sqrt{<\varepsilon^2>}$ values and the average energy, which is obtained from the MC simulation of the n-i-n devices. As we can see in Fig.3, the $\sqrt{<\varepsilon^2>}$ in the region where W increases(denoted by upward arrow) is almost same as homogeneous case but it is much different where W steeply decreases(denoted by downward arrow). Hence, Γ in the latter case is much larger than zero showing that the large difference in the distribution from the homogeneous case.

Now we propose the concept of the effective average energy(W_{eff}) which can uniquely determine the mobility. W_{eff} should include the Γ parameter. We found that the function form as ,

$$W_{eff} = W \exp(\kappa\Gamma) \quad (3)$$

with κ =1.2 as a fitting parameter gives a unique mobility as shown Fig. 4. The data are obtained from the MC simulation of the n-i-n structure for wide range of anode voltages.

To apply this concept to macroscopic transport modeling, we need to obtain $<\varepsilon^2>$ from the fourth moment equation of the BTE (So the Γ value)[5]. Solution of the fourth moment equation of the BTE, however, needs additional computing time ,which is not practical. Therefore, in the following section, we show that the fourth moment can be expressed by the lower moments and the new mobility can be adopted by the conventional HD simulator without a numerical burden.

3. W_{eff} parametrized by the lower moments of BTE

As shown in Fig.3 , $<\varepsilon^2>$ cannot be uniquely determined by the average energy in the inhomogeneous situation in the device. $<\varepsilon^2>$ value in the decreasing W region is larger than the value in the increasing W region. The number of hot electrons is underestimated near n - n[+] junction (usually W decreases there) where the hot electrons heated are embedded in a large number of cold electrons under the conventional HD scheme. However, the hot electrons play important roles in the impact ionization and mobility[6]. The ratio of drift energy($=\frac{1}{2}mV^2$) to the total energy is smaller in the E-field decreasing region than in the E-field increasing region[7]. From this observation, we related $\sqrt{<\varepsilon^2>}$ with W and $\alpha\sqrt{WVP}$. (α is fitting constant 1.4 and V,P are the average velocity and the average momentum, respectively) As shown in Fig. 5, $\sqrt{<\varepsilon^2>}$ can be uniquely determined by the W,V,P for various bias conditions in n-i-n structure. Because $\sqrt{<\varepsilon^2>}$ is modeled as $\sqrt{<\varepsilon^2>} = f(W) - \alpha\sqrt{WVP}$ ($f(W)$ is a single valued function of W), Γ defined in eq. (2) can also be expressed as a function of W,V,P as ,

$$\Gamma = \frac{\sqrt{\frac{3}{5}}\left(\sqrt{<\varepsilon^2>} - \sqrt{<\varepsilon^2>_h}\right)}{W} = \frac{\alpha\sqrt{\frac{3}{5}}\left(\sqrt{V_h P_h} - \sqrt{VP}\right)}{\sqrt{W}} \quad (4)$$

where, V_h, P_h are values in the homogeneous bulk.

P can be expressed as m^*V(m^* being effective mass of electron) if the parabolic energy band is assumed. V_h is derived from the uniform bulk field-energy, energy-velocity relation.

As a result, the final expression of W_{eff} can be written as ,

$$W_{eff} = W \exp\left(\frac{\kappa\alpha\sqrt{\frac{3}{5}m}\,(V_h - V)}{\sqrt{W}} \right) \quad (5)$$

We implemented derived W_{eff} into the electron temperature dependent mobility model in the conventional HD simulator, SNU-2D[8].

New Mobility is formed by substituting W_{eff} for W in existing mobility model. Comparison of $\mu(W)$, $\mu(W_{eff})$, is plotted in Fig. 6.

4 . Conclusion

The derivation of the new carrier mobility using the effective carrier energy, W_{eff}, considering the fourth moment of the BTE is given in this study.

In order to reduce a computational burden, the modified W_{eff} is proposed and implemented in the 2-dimensional HD simulator, SNU-2D. This model uses only scalar quantity so that we believe that the new model can be applied in 2-D case in contrast to Lee and Tang's inhomogeneous mobility tensor $\hat{\mu}$ expressed as a function of ($\frac{\vec{S} \bullet \vec{V}}{V^2}$) which can be applied to only 1-D case[1][2][3].

Our mobility model does not require additional CPU time compared with the conventional local energy dependent model and it does not cause any convergence problem.

Acknowledgment

This work has been supported from ETRI (Electronics and Telecommunication Research Institute).

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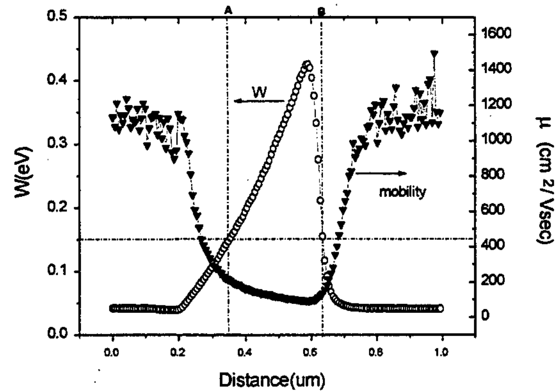


Fig. 1. The example of energy and mobility distribution extracted form the MC simulation of n-i-n diode (L=0.4um, n=2e17cm^{-3}, i=5e15 cm^{-3})

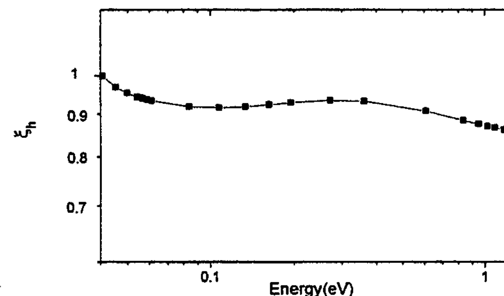
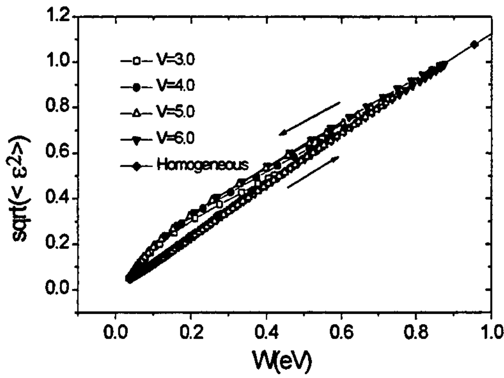


Fig. 2. ξ as a function of energy for the homogeneous bulk



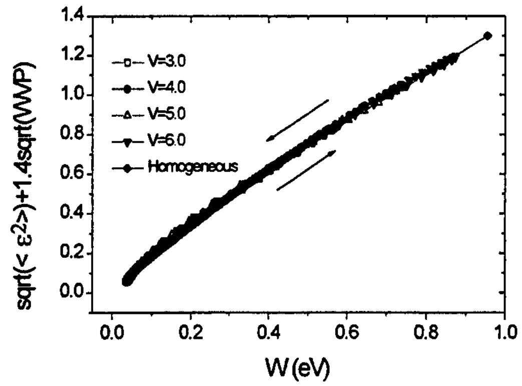


Fig. 3. $\sqrt{<\varepsilon^2>}$ **as a function of the average energy W for various biases.**

Fig. 5. $\sqrt{<\varepsilon^2>} + 1.4\sqrt{WVP}$ **as a function of average energy W.**

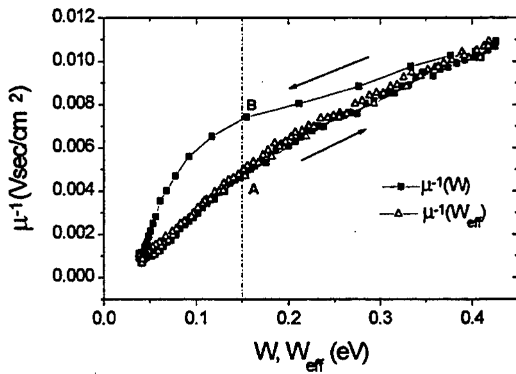


Fig. 4. The reciprocal mobility as a function of W and W_{eff}. A and B are the same W points(W=0.15eV) in the device of Fig. 1 (Vbias =3V).

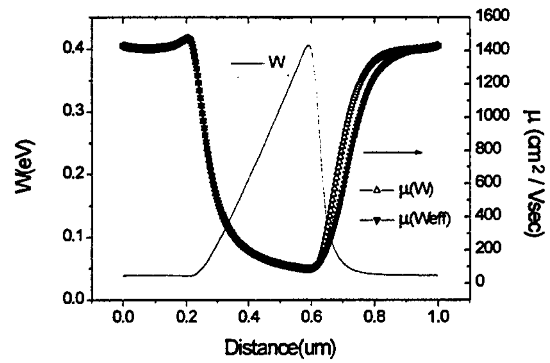


Fig. 6. Comparison of $\mu(W)$ and $\mu(W_{eff})$ in the HD simulation

A Physical Model of Ohmic Contacts[1]

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In the past most modellers of semiconductor devices treated the Ohmic contacts as ideal interfaces through which the carriers can pass in and out without any restraints. Scanning electron microscopy, however, has shown that an Ohmic contact is indeed a complex structure of grains of different stoichiometric composition. As the Fermi levels align over these grains we should expect barriers to be set up between them through which the electrons have to tunnel. This has prompted theorists to construct a barrier model in which the carriers enter the semiconductor through a tunnel barrier of height equal to the Schottky contact potential and a width depending on the local carrier concentration.

In this paper we shall present a physical model suitable for Monte Carlo particle modelling of semiconductor devices and apply it as an example to the heterojunction high electron mobility field effect transistor (HEMT) shown in Figure 1. In the metal, the concentration of electrons is several orders of magnitude larger than in the semiconductor. However, only those electrons near the Fermi level and above the bottom of the conduction band in the semiconductor can enter the semiconductor. Furthermore, due to conservation of energy and momentum only those electrons impinging the metal semiconductor interface within a cone of aperture

$$\phi = \arccos\{1/(1+\xi)^{1/2}\}$$

with

$$\xi = (m_S/m_M)/(E_C/E + 1 - m_S/m_M)$$

can be injected. Here m_S and m_M represent the effective electronic mass in the semiconductor and the metal, respectively; E_C the band gap energy in

[1] This work was supported in part by the US Office of Naval Research, the DoD High Performance Computing Program and the German Federal Ministry of Defence.

the semiconductor and E the kinetic energy of the electron in the metal. This implies that only a fraction of the electrons is available for injection into the semiconductor, amounting to a concentration of about an order of magnitude larger than that of the cap layer of the transistor.

To make contact with the conductive channel of the HEMT it is necessary for the Ohmic contacts to be alloyed at least down to it. During manufacture of the transistor polycrystalline alloy spikes of sufficient penetration are formed. Monte Carlo simulations show that the penetration depth has no influence on the current characteristics of the HEMT, Figure 2, if we neglect the tunnel barriers. Also the density of electrons in the contact area is of no significance to the electric currents.

The tunnel barrier potential has the shape

$$U(x) = (qx\sqrt{\frac{n}{2\varepsilon_0\varepsilon_r}} - \sqrt{B_H})^2 - \frac{q^2}{16\pi\varepsilon_0\varepsilon_s x}$$

where q represents the elementary electronic charge, n the local carrier density at the tunnel barrier, ε_0 the permittivity of vacuum, ε_r the static dielectric constant, ε_s the optical phonon frequency dielectric constant and x the co-ordinate perpendicular to the barrier, reckoned from the metal semiconductor interface. B_H and n will be referred to as the height and width parameters below. The first term describes the barrier shape in the absence of image forces and the second the correction due to them, which is significant. Indeed, barriers between metal grains will not contribute significantly to the contact resistance because the image forces will almost eliminate them.

Figures 3 and 4 show two possible contact topographies, one contact consisting of semiconductor material with a grain boundary through it, the other featuring metal diffused into it forming a thin metal layer next to the original metal face and a spike penetrating into the interior of the transistor. The barriers between the semiconductor grains will cause most of the contact resistance, and the drain current depends on where the barriers are located, Figure 5. Our simulations show that the reduction is most effective when the barrier is set up at the beginning and the end of the conductive channel. When tunnel barriers are present the carrier concentration in the contact has to be considered, Figure 6. The curves shown here have been obtained for different metal topographies but with the tunnel barriers at the

same place. This shows that all carriers available for injection have to be considered in the model. We recall that this was not necessary in the absence of barriers.

The transistor has a given demand for electrons defined by the conductivity of the channel and the bias of the gate and the drain. If this demand can be satisfied the contact resistance will not be of any hindrance to the operation of the transistor. Placing the tunnel barriers next to the metal boundary will not influence the contact resistance because there are enough electrons in the metal to satisfy this demand. Ideally the contacts should be manufactured such that the natural demand of the device can be satisfied. It may be possible to achieve this by placing the grain boundary tunnel barrier at the right places.

The study of a contact is also important in understanding deterioration of transistors with age as the topography of the contacts change by establishing wider tunnel barriers by atomic diffusion and trapping charges at the grain boundaries. This may already have happened to a small degree during manufacture, possibly explaining some of the observed spread in the transistor characteristics.

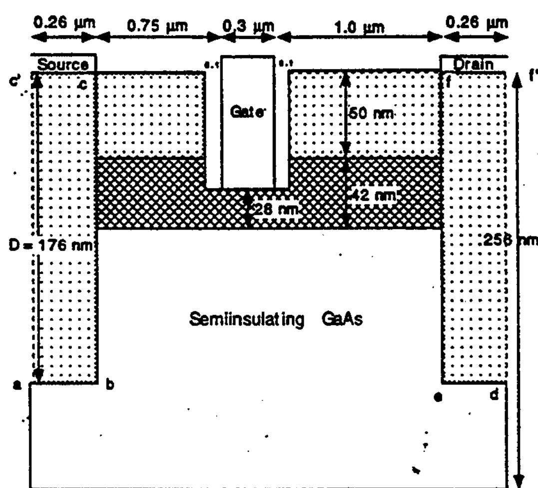

Figure 1: Transistor geometry. Dotted areas: cap layer n-doped at 7 x 10^{24} m^{-3} and Ohmic contact regions a-b-c-c' and d-e-f-f'. Cross-hatched area: $Al_{0.26}Ga_{0.74}As$ n-doped at 2 x 10^{24} m^{-3}. D represents the penetration depth of the Ohmic contact.

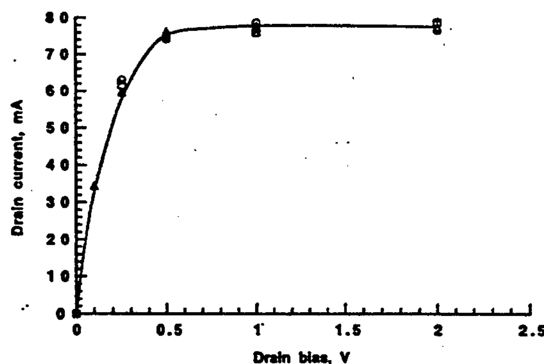

Figure 2: Forward characteristics calculated for different Ohmic contact penetration depth.. Gate bias 0 V. x: D=82 mn; o: 100 nm; : 132 nm; Δ: 176 nm and + : 256 nm.

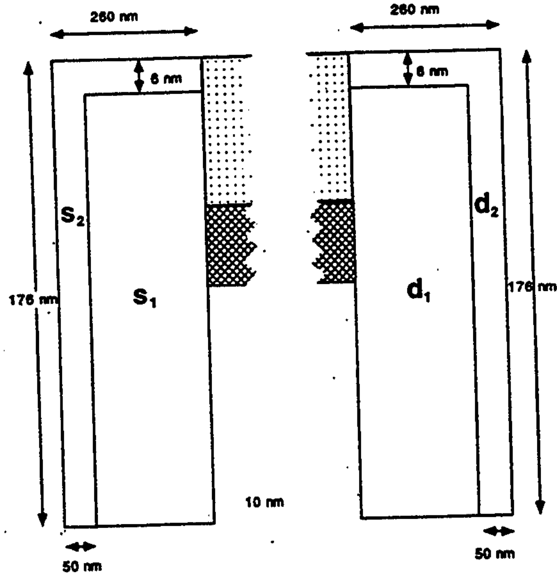

Figure 3: Details of Ohmic contact . Areas s_2 and d_2 are metallic, s_1 and d_1 semiconductor doped at 7×10^{24} m^{-3}.

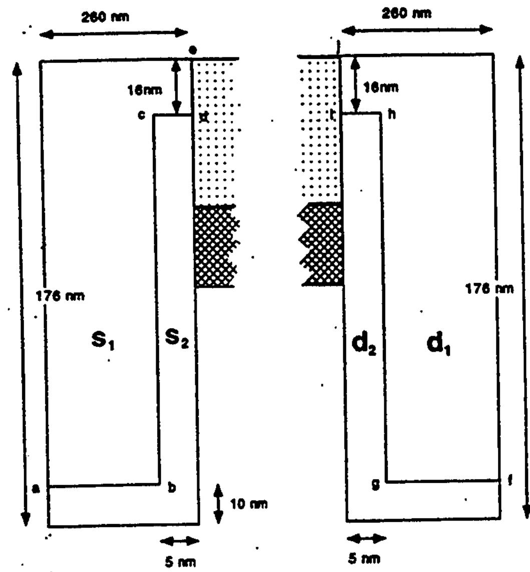

Figure 4: Details of Ohmic contact areas. All areas are semiconducting doped at 7 x 10^{24} m^{-3}. A tunnel barrier of height parameter BH = 0.75 eV and width parameter $n = 7 \times 10^{24}$ m^{-3} along the lines a-b-c-d-e and f-g-h-i-j.

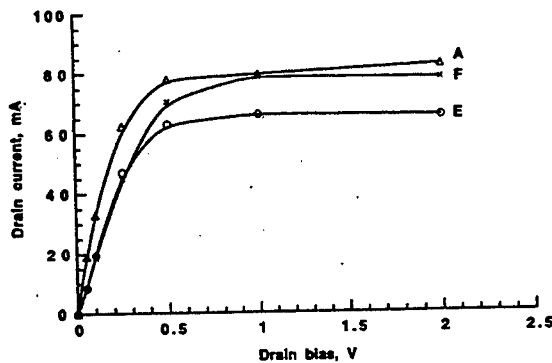

Figure 5: Calculated forward characteristics at zero gate bias with the entire contact areas semiconducting doped at 7 x 10^{24} m^{-3}.for A: no tunnel barriers (reproduced from Figure 2); F: with contact areas shown in Figure 4 and E: tunnel barriers at the edges of the contact areas (i.e. along a-b-c and d-e-f of Figure 1).

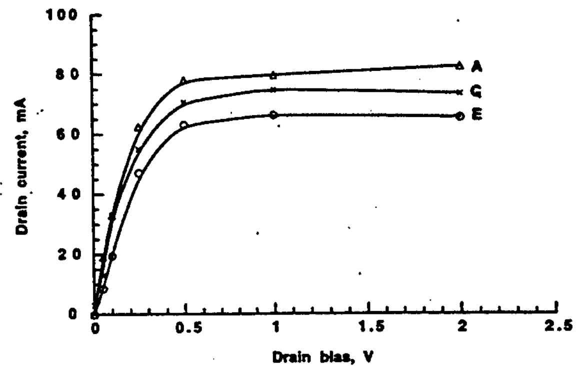

Figure 6: Calculated forward characteristics at zero gate bias for A: no tunnel barriers (reproduced from Figure 2), the other two curves apply to the case of tunnel barriers along the edges of the Ohmic contact areas. E: The entire Ohmic contact areas are semiconducting doped at density 7 x 10^{24} m^{-3}. G: contact as shown in Figure 3.

Charge Thickness Model - A Novel and Accurate Compact C-V Model for 2.5nm Gate Oxide Technology and Beyond

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1.0 Introduction

As the power supply voltage and gate oxide thickness are continuously scaled down, some physical effects such as inversion layer quantization and poly-silicon gate depletion can not be ignored any more for accurate device modeling [1-2]. In particular, due to the finite thickness of the inversion layer, the charge centroid on average location is some 20A from the interface and constitutes a significant part of the gate related capacitances. This work presents how the finite thinckess of inversion layer is incorporated in the compact model for the first time. A continuous Charge Thickness C-V model from accumulation through depletion to strong inversion including inversion layer quantization and polysilicon gate depletion effects is presented. This novel C-V model is implemented in BSIM3 and compared with measurement data. Significant improvement in the modeling accuracy is clearly shown. The exsiting IV model is adequate even for 2.5nm oxide MOSFETs although the new Charge Thickness Model can also be easily included in the IV model.

2.0 Model Equation

In order to accurately characterize the charge centroid, a 1-D simulator has been developed to solve self-consistently Schrodinger, Poisson equations with Fermi-Dirac statistics. Fig. 1 shows that the 1-D simulation is capable of matching measured gate capacitance *Cgg* very well over a wide range of *Tox*, and polysilicon and substrate doping concentrations.

Based on 1-D simulations, a universal semi-empirical formulation for the finite charge thickness *Tcentroid* in strong inversion is proposed

$$Tcentroid = 5.7\times10^{-7} \Big/ \left[1+\left(\frac{V_g+3V_T}{2T_{ox}}\right)^{0.7}\right] \qquad (1)$$

where $(Vg + 3VT)/2Tox$ represents the average of the electric field on either sides of the inversion layer. Fig. 2 demonstrates that (1) fits very well the simulated inversion charge thickness for different *Tox* and substrate dopings. Similarly, in accumulation and depletion regions, *Tcentroid* is found to follow

$$Tcentroid = 2.5\times10^{-7} + L_d(N_{sub})\exp\left[\left(\frac{N_{sub}}{2\times10^{16}}\right)^{-0.25}\frac{V_g-V_{fb}}{T_{ox}}\right] \qquad (2)$$

where *Ld* is the Debye length, as shown in Fig. 3. Considering the finite charge thickness, the equivalent gate oxide capacitance *Ceq* can be expressed as

$$\frac{1}{C_{eq}}=\frac{1}{C_{ox}}+\frac{1}{C_{centroid}} \qquad (3)$$

where *Ccentroid* is the capacitance of the finite charge thickness, which is equal to $\varepsilon_{Si}/T_{centroid}$.

This *charge thickness model* (**CTM**) has been implenmented in Berkeley SPICE3. The $\phi_s=2\phi_B$ approximation in traditional threshold voltage (V_T) model ignores the fact that surface potential changes with *Vg* when $Vg > V_T$, CTM does not assume constant ϕ_s as shown in Fig. 4. In addition, poly silicon gate depletion effects were

also accounted for in the model implementation.

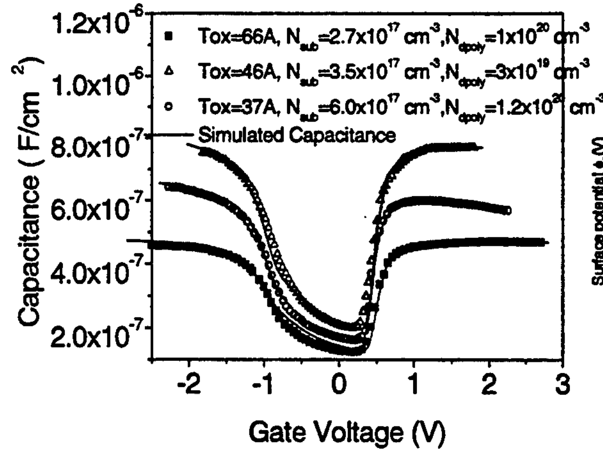


Fig.1. 1-D simulaton and measured *Cgg* for different *Tox*, substrate and poly gate doping concertrations.

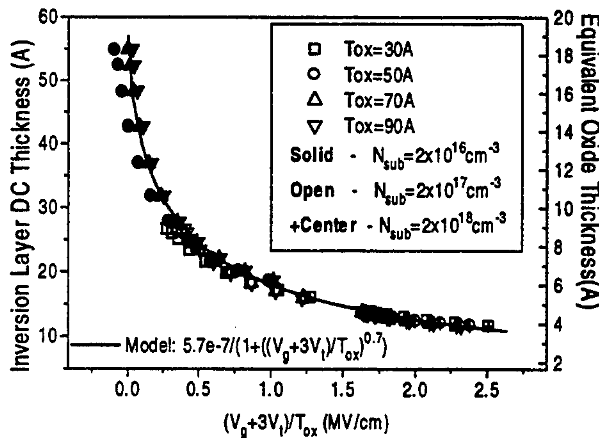


Fig. 2 Universal finite charge thickness in strong inversion region vs. *(Vgs+Vth)/Tox* for various *Nch* and *Tox.*

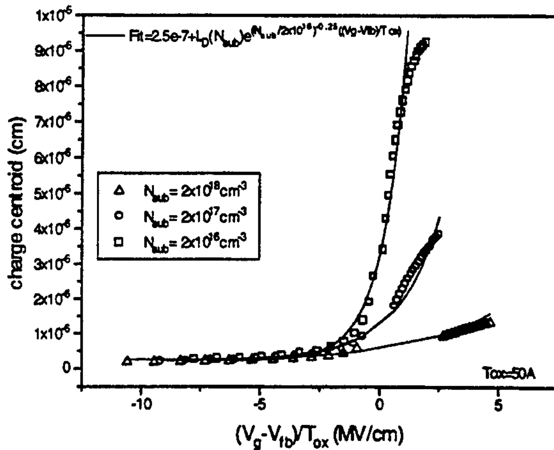


Fig. 3 Universal finite charge thickness in accumulation and depletion regions vs. *(Vgs+Vth)/Tox* for various *Nch.*

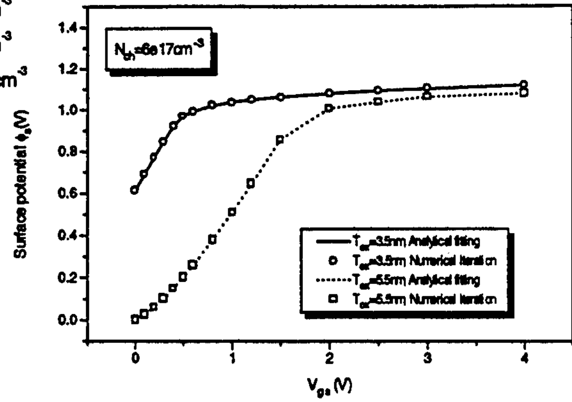


Fig. 4. Analytical fitting of bias dependent ϕ_s to numerical iteration results for different *Tox*, *Nsub*=6×10^{17}cm^{-3}.

3.0 Results and Discussion

Below is the comparison between modeling and measurement of gate-related capacitances for gate oxide thicknesses down to 2.5nm. In Fig. 5, CTM accurately reproduces *Cgg* measurement. The model shows excellent smothness from accumulation through depletion to strong inversion region. Note that the CTM model behaves very well in the transition regions. In addition, the poly silicon depletion effects is also well modeled.

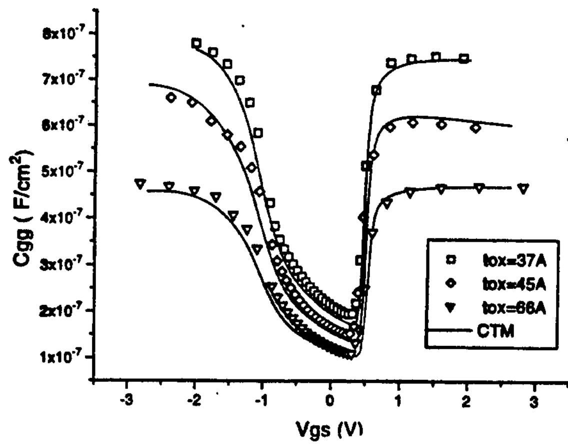


Fig. 5. Measured *Cgg* versus *Vgs* comparison with CTM.

Fig. 6 shows the comparison of gate-to-channel capacitance *Cgc* between CTM and existing BSIM3v3 for *Tox*=3.6 and 2.5nm. It can be seen that in the whole region CTM fits data better than BSIM3v3, especially in moderate and strong inversion regions where inversion layer quantization begins to show up. Figs. 7 and 8 presents the good agreement between the measured and simulated *Cgd* and *Cgs* versus *Vds* using CTM model. Fig. 9 shows CTM is also capable of accurately simulating *Cgb* at different *Vds*, and showing good smoothness near the flat-band and threshold voltages.

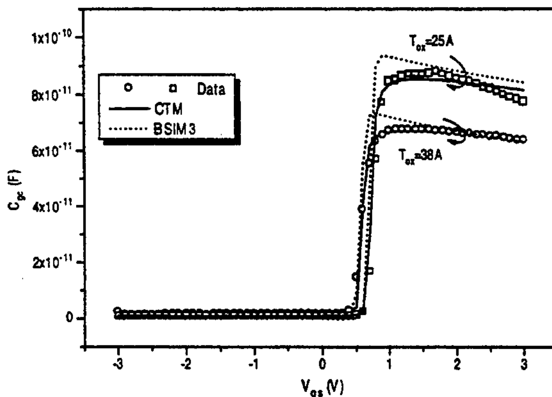


Fig. 6Comparison of CTM, BSIM3v3 and measurement data: *Cgc* vs. *Vgs*, *W/L*=100μm/100μm .

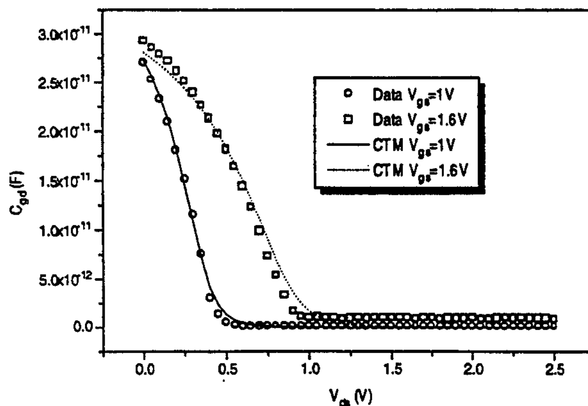


Fig. 7CTM model vs. measurement data: *Cgd* vs. *Vds*. *Tox*=4.5nm, *W/L*=100μm/100μm.

It is worthwhile mentioning that some transcapacitances in small MOSFETs may exhibit a small "negative" value (or change the sign) in some operation region. This is also visible in both BSIM3v3 and CTM. This is surprising and may be mistakenly regarded as non-physical. But 2-D simulation using MEDICI indeed shows that it is perfectly possible for some transcapacitance to change their signs as the channel length is scaled down. As an example, Fig.10 (a) and (b) demonstrate how *Cgd* goes negative under certain bias conditions using 2-D simulation. We will present a physical explanation based on the *Vds* dependence of *VT*.

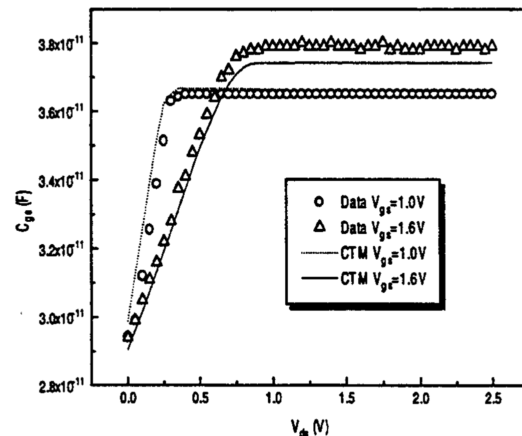


Fig. 8CTM model versus data: *Cgs* vs. *Vds*. *Tox*=4.5nm, *W/L*=100μm/100μm.

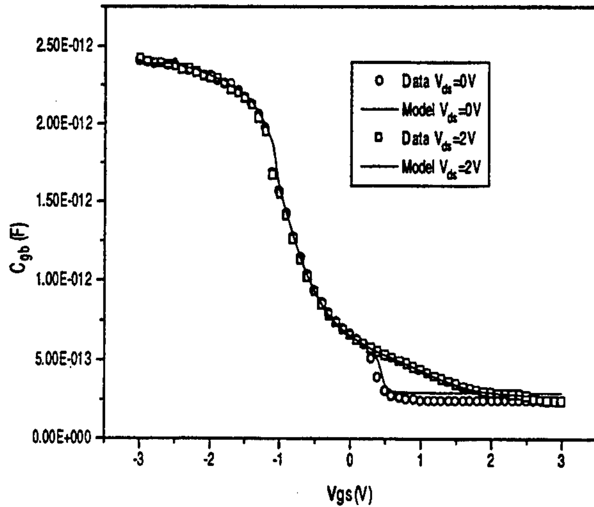
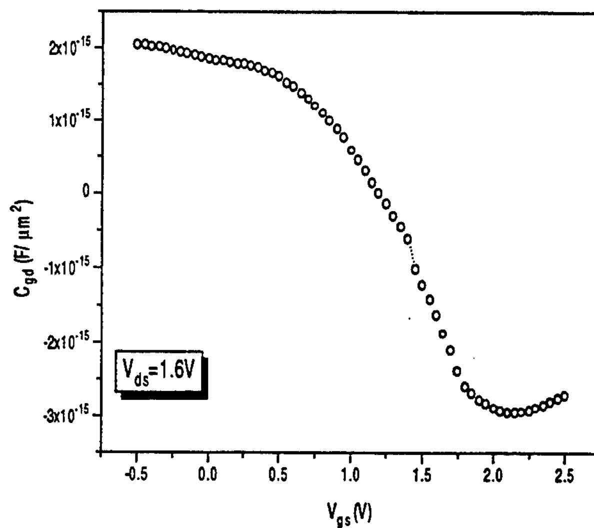
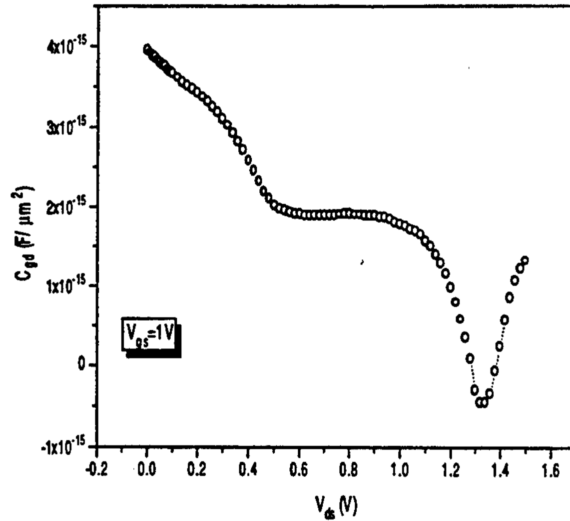


Fig. 9CTM model versus data: *Cgb* vs. *Vgs*, *Tox*=7.7nm, *W/L*=100µm/100µm.



(a) *Cgd* ~ *Vds*



(b) *Cgd* ~ *Vgs*

Fig. 10 Negative capacitance *Cgd* using 2-D simulation, *Tox*=6nm, channel length *L*=0.05µm.

4.0 Conclusion

In conclusion, a novel MOSFET intrinsic capacitance model was reported, which considers the finite charge thickness due to quantization effects. Compared with BSIM3v3, it was found that this model can fit data more accurately for thin gate oxide technologies, especially in the region around *Vfb* and *Vth*. In addition, because of its compact form, it can be easily implemented in CAD tools and can predict more accurate capacitance for CMOS circuit simulation.

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Enhanced lifetimes of Bloch oscillations by spatially selective photoexcitation

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Abstract - We show, by accurate numerical simulations, that large-amplitude quasi-periodic Bloch oscillations with enhanced lifetimes can be achieved using a spatially selective photoexcitation process in semiconductor superlattices. By modifying the composition of a single interior GaAs layer of a GaAs/$Al_xGa_{1-x}As$ superlattice with a low level (< 1%) of In atoms, it becomes possible to photoexcite electrons to a small number of In-perturbed Wannier-Stark localized states and thereby avoid the dephasing effects due to interface roughness.

The successful experimental observations[1] in recent years of Bloch oscillations (BO) in semiconductor superlattices (SL) subject to dc electric fields has convincingly laid to rest a long-standing controversy over their existence. However, the prospects that BO will provide a viable source of terahertz (THz) electromagnetic radiation might appear remote, since, to date, measured signals in epitaxial GaAs/AlGaAs SLs degrade significantly after at most ten, and typically fewer, periods of oscillation.[1] Reynolds and Luban[2] have recently presented evidence that the essential features of the observed decay of BO for low carrier densities can be attributed to the effects of unavoidable interface roughness (IR), where the epilayers of an epitaxial SL differ somewhat from the idealized picture of strictly planar layers. Thus, the degrading effects of IR can be avoided only by modifying the conventional photoexcitation method of producing BO, where conduction electrons and valence heavy holes are photoexcited in a nearly uniform manner throughout the entire SL by an ultrafast (~100 fs) laser pulse.

We present here a method for achieving spatially selective photoexcitation, of electrons within an epitaxial SL. This involves using a deliberately reduced band gap in one or a few GaAs layers in a GaAs/$Al_xGa_{1-x}As$ system, for example, by adding a low-level (<1%) of In atoms. Furthermore, as shown by our accurate numerical simulations, by photoexciting electrons within a *restricted* portion of a SL, it becomes possible to produce BO featuring significantly longer lifetimes than have been observed to date, despite the inevitable presence of IR.

Before discussing our proposal for achieving spatially selective photoexcitation it is essential to review the major physical ideas of the effects of a uniform dc electric field, F, on an ideal periodic SL. Under suitable conditions,[3] the field splits both the conduction and valence minibands into discrete uniformly-spaced, energy levels $E_n^e = E_0^e + neFa$ and $E_\alpha^h = E_0^h + \alpha eFa$, where a is the spatial period of the SL, e is the magnitude of the electron charge, and n and α are any integers. One commonly refers to these energy spectra as Wannier-Stark (WS) ladders. It is now well substantiated that the uniform spacing, eFa,

of the WS ladders gives rise to strictly time-periodic BO with frequency $\nu_B = eFa/h$. Each of the electron WS states is localized over several unit cells of the SL. By contrast, for an epitaxially-grown SL, it has been shown[2] that the effect of IR is to slightly shift, in essentially random fashion, each of the WS energy levels from its nominal value for the idealized periodic SL. The values of the frequencies, $\nu_l \equiv (E_{l+1} - E_l)/h$, associated with successive electron WS levels are typically spread $\pm 5\%$ about the mean value ν_B. The net result is a WS ladder of almost uniformly-spaced, yet *incommensurate* energy levels. By adopting parameters of experimental relevance[4], the net effect of IR (see the curves marked "unmodified" in Fig. 1) is that $z(t)$, the electron position expectation value, dephases during a time interval of order 10 ps, in agreement with experiment. Moreover, the effect of numerous participating frequencies ν_l in the immediate vicinity of ν_B is to provide THz radiation with a relatively large noise level.

Suppose now that we deliberately reduce the band gap in a single, interior GaAs layer, for example, by adding a low-level (<1%) of In atoms. We find, through detailed calculations, that the smaller band gap of the local InGaAs alloy causes a major shift of the electron and hole WS levels associated with that unit cell as well as the electron WS levels in the immediate vicinity of the modified cell. One can then exploit these energy shifts by using a laser pulse with an appropriately reduced excitation frequency and sufficiently narrow frequency width so as to excite electrons primarily in the near vicinity of the modified cell.

In the following we discuss our results for a SL whose parameters match those used in the experiments of Refs. 4 and 5. Thus the sample in our simulations consisted of 35 layers of GaAs, each of nominal width $w = 9.7$ nm, and 34 layers of $Al_{0.3}Ga_{0.7}As$ of nominal width $b = 1.7$ nm. To include the effects of IR we used the specific one-dimensional electron-superlattice potential of Ref. 2. Thus, in the vicinity of what would otherwise be an abrupt interface between GaAs and AlGaAs layers, we employ a smoothly varying term incorporating two parameters, chosen separately for each interface using a random number generator, one controlling the width of the interface region and the other defining its location. Additionally, we suppose that the central GaAs layer of the SL includes In atoms with concentration $x' \approx (0.5\text{-}0.75)\%$. The electron Hamiltonian operator H is developed in the effective-mass approximation. It is taken as the sum of the electron potential energy due to the superlattice, $V(z)$, which includes the effects of IR and the addition of In atoms; the electric field term eFz; an effective one-dimensional Coulomb potential energy[6] term due to the interaction of the electron with the photoexcited heavy hole; and the standard expression for the kinetic energy operator. We have analyzed in great quantitative detail the photoexcitation process so as to arrive at a realistic form of the initial wavefunction, $\psi(z,0)$. The evolution of the electron wavefunction subsequent to the photoexcitation process is then determined by solving the time-dependent Schrödinger equation, $i\hbar\partial\psi/\partial t = H\psi$, using a high accuracy Cayley integration routine.[2,3] Armed with numerical values of $\psi(z,t)$, we compute $z(t) \equiv \langle \psi(z,t)|z|\psi(z,t)\rangle$. The usefulness of this quantity stems from the fact that the transmittive electro-optic sampling (TEOS) method[4] and THz radiation experiments[1] measure BO signals which are proportional to this quantity.

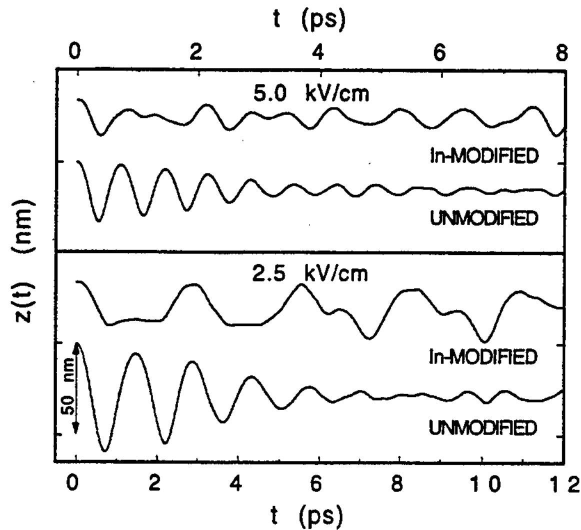

FIG. 1. Calculated position expectation value $z(t)$ for two values of the electric field for two samples of a $GaAs/Al_{0.3}Ga_{0.7}As$ superlattice. For each SL we have included interface roughness and they differ only in that In atoms (concentration $x' = 0.0075$) have been added to the central GaAs layer of one sample.

In Fig. 1 we display our results for $z(t)$ for the two different systems with F=2.5 and 5.0 kV/cm. In the sample without In, where electrons have been photoexcited in a nearly uniform manner throughout the sample, $z(t)$ subsequently exhibits monotonic decay due to the dephasing effects of IR. By contrast, in the case of the In-modified SL, where, it turns out, only two or three WS states are appreciably excited, there is practically no decay of $z(t)$ for times up to 15 ps.

In Fig. 2 we display the frequency power spectrum $|Z(\nu)|^2$, where $Z(\nu)$ is defined as the Fourier time transform of the computed values of $z(t)$ extending over a time interval of width 32 ps for the SLs with and without the addition of In for F = 2.5 and 5.0 kV/cm. For both field values, the SL which has been modified with In shows significantly reduced broadening in frequency space. That is, the THz radiation emitted by this SL would display *lower levels of noise than in the absence of In.*

The design discussed here, of adding In atoms in a single GaAs well, was chosen for its simplicity. A wider range of possibilities could perhaps be achieved by using multiple In-modified wells. In fact, we have extensively studied a case with two adjacent In-modified wells, but the resulting complexities do not appear to favor such a choice. In any event, it can be seen that numerical simulations of BO systems, such as exemplified by this work, provide an invaluable *tool* for the design of the superlattice. Indeed, given the complexity of superlattice systems and their apparent sensitivity to small perturbations of the epilayers, extensive theoretical modeling can be seen as the *only* practical means of producing a successful design.

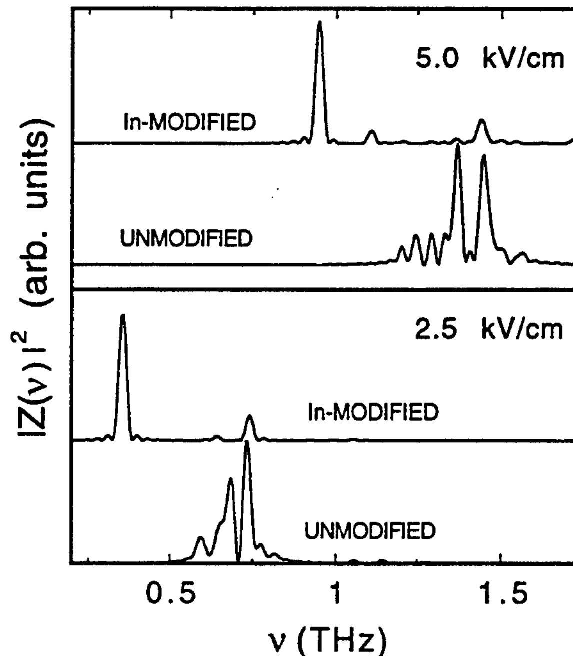

FIG. 2. Frequency power spectrum, $|Z(\nu)|^2$, where $Z(\nu)$ denotes the Fourier time transform of the computed values of $z(t)$ which is taken to be zero outside a 32 ps interval.

Although we have here discussed superlattice design in the context of reducing IR effects on BO, the ability to create isolated wave-packets within an extended superlattice may prove useful in a variety of other optoelectronic applications as well as for systems of basic interest.

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Self Assembled Semiconductor Structures: Carrier Dynamics and Optical Properties

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ABSTRACT

It is now known that when a semiconductor overlayer is deposited on a substrate with a high lattice mismatch, the initial growth produces 3-dimensional islands. This allows one to produce quantum dot structures by single step epitaxy. In the past few years such self assembled dots have improved (in uniformity) to an extent that several aspects of 0-dimensional physics have been observed in them. It is also known experimentally that these self assembled dots have a pyramidal shape and have a highly complex strain tensor. The strong strain tensor causes a very large change in the effective bandgap and transitions in the quantum dots. For example, in InAs quantum dots on GaAs substrates, the ground state transition energy is $\sim$ 1.1 eV even though the bandgap of InAs is 0.4 eV. This large strain driven effect suggests that the electronic spectra of the structure are strongly influenced by remote band interactions.

In this paper we will address the following issues:

i) What is the general nature of the strain tensor in self assembled quantum dots?

ii) What are the electron and hole spectra for InAs/GaAs dots?

(iii) What are the important inter-subband scattering processes? In particular we will discuss how the electron-phonon interactions are modified in the quantum dot structures and the role of carrier-carrier scattering. We will describe the conditions under which 0-dimensional physics can be exploited to increase the electron thermalization times.

(iv) what are the strengths of various optical transitions in the self assembled quantum dots? An important manifestation of the large strain in self assembled dots is the very large inter-subband optical matrix element.

Consequences of these effects for uncooled inter-subband devices such as lasers, detectors and quantum transistors will be discussed.

High Temperature Operation of 4H and 6H SiC High Voltage Schottky Diodes

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1. Introduction

Silicon carbide is foreseen to become the material of choice for high power and high temperature applications due to its excellent electronic and physical properties. Schottky barrier diodes (SBDs) on SiC can offer fast switching characteristics which can be coupled with the high power and high temperature capability. Therefore, they have the potential to be a valuable alternative to high power Si based switching devices. For this reason, considerable effort has recently been made to develop SiC-based high voltage Schottky barrier diode (SBD) rectifiers.

Several groups have reported SBDs on SiC using different metals as Schottky contacts. The first high voltage SiC Schottky diodes on 6H polytype were reported by Bhatnagar et *al.* [1]. These Pt/6H-SiC diodes had a blocking voltage in excess of 400 V. The reverse current density was ~7.3×10^{-3} A/cm^2 at a reverse bias of 400 V. High voltage Au/6H-SiC Schottky diodes were reported by Kimoto et *al.* [2]. These diodes had breakdown voltages exceeding 1100 V, but a forward current density of only 42 A/cm^2 at a forward voltage drop of 2V. Recently, there has been a trend towards the 4H-SiC polytype, since it has a higher electron mobility parallel to the c-axis, which is normally the direction of current flow in power devices [3]. Schottky barrier diodes on 4H SiC were reported by Itoh et *al.* [4] using Au, Ni and Ti. The breakdown voltage for these diodes was reported to be 800 V at 25°C. The leakage current at a reverse bias of 600V was ~1×10^{-5} A/cm^2. A current density of 100 A/cm^2 was obtained at a forward voltage drop of 1.67 V. Raghunathan et *al.* [5] also reported high breakdown voltage (1000 V) Ti/4H-SiC SBDs with a forward voltage drop of only 1.06 V at a forward current density of 100 A/cm^2. However, these diodes had a significantly higher leakage current of ~7×10^{-3} A/cm^2 at 600 V as a result of a lower Schottky barrier height for Ti on SiC (0.99 eV). Even though a few of the published results discussed above [1, 2, 5] have reported current-voltage characteristics of the devices at higher temperatures, a detailed analysis of the operation of SiC SBDs at higher temperatures has not been reported.

We have performed extensive studies on SBDs utilizing Ni for both ohmic and Schottky contacts on different polytypes of SiC. Ni is the metal of choice for ohmic contacts to SiC as it results in stable contacts with low specific contact resistance [6]. In our studies, Ni was selected for forming Schottky contact as well because as-deposited Ni always results in a Schottky contact to SiC with a relatively large barrier height (1.29 eV on 6H-SiC [7]). In addition, using a single metal simplifies the needs of the process.

We have previously shown Ni/3C-SiC Schottky diodes with Ni as both ohmic and Schottky contact metal [8]. In later studies we reported Ni/6H-SiC SBDs with a high breakdown voltage (>1000V) at both 25 and 300°C [9]. We have also investigated the current mechanisms for these diodes [10] in the temperature range from 100 K to 573 K. Recently we reported [11] SBDs on 4H-SiC using Ni and Pt for Schottky contact. Pt was used for the first time to form Schottky contacts on 4H-SiC. In this paper we report the successful operation of these diodes under forward bias conditions up to 450°C and under reverse bias conditions up to 300°C. The barrier heights for Ni and Pt on 4H-SiC have been characterized from analysis of I-V characteristics. The variation with temperature of other important parameters such as the current on/off ratio and the specific on-resistance has also been studied

for these diodes. The results of high temperature tests on Ni/4H-SiC SBDs have been compared with those on Ni/6H-SiC diodes reported earlier [9, 10].

2. Experimental Procedure

Schottky diodes with a vertical structure were fabricated on 10 μm thick n-type doped SiC epitaxial layers (nominal doping 6.1×10^{15} cm^{-3} for 4H and 7.2×10^{15} cm^{-3} for 6H polytype) grown on heavily doped (9.4×10^{18} cm^{-3} for 4H, 2×10^{18} cm^{-3} for 6H) n-type Si-face substrates commercially available from Cree Research [12]. The 6H-SiC wafer was from the "reduced cost" inventory of the manufacturer whereas the 4H-SiC wafer was "low-micropipe, production-grade" quality material. Fig. 1 shows a cross section schematic of SBDs fabricated on these wafers. A thermally grown oxide on the epi-layer served both as a passivation layer. A backside ohmic contact was formed by Ni sputter deposition followed by annealing. The circular Schottky contacts had diameters from 30 to 240 μm. The contacts were designed with the metal overlapping the field oxide by 10 μm to improve edge field termination. For Schottky contact formation, Ni was sputter-deposited, while Pt was deposited by electron beam evaporation.

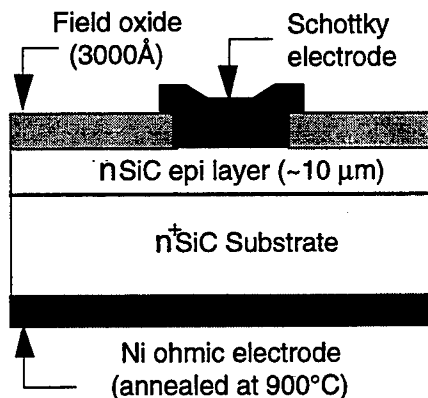

FIG 1. Schematic of SiC SBD with field oxide structure.

3. Results and Discussion

In this section we first discuss the room temperature results of Ni and Pt Schottky diodes on 4H-SiC. This is followed by a discussion on the high temperature performance of Ni SBDs on both 4H and 6H SiC.

The current voltage characteristics of typical Pt/4H SiC and Ni/4H SiC SBDs at room temperature are shown in Figs. 1 and 2. A forward current density (J_F) of 100 A/cm^2 was achieved at a forward voltage drop of 1.76 and 1.86 V, respectively. The ideality factors for these diodes were calculated from the forward J-V plots as 1.11 and 1.29, respectively.

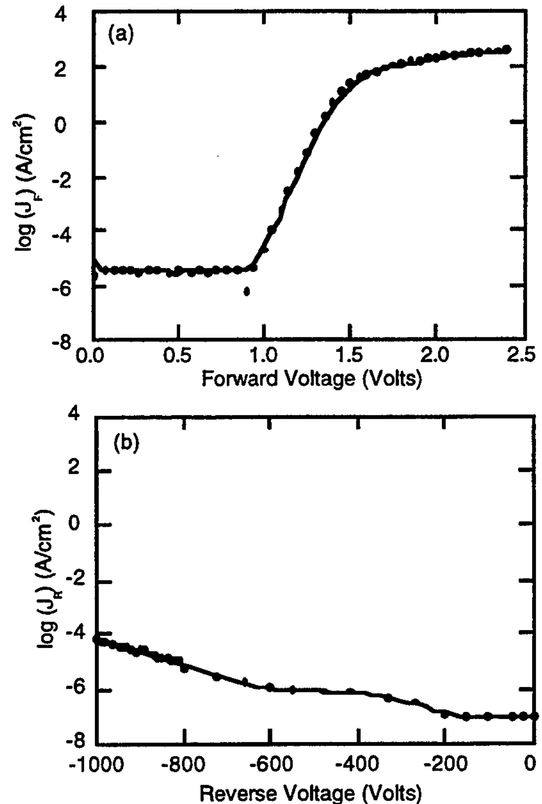

FIG 2. Current-voltage characteristics of a typical Pt/4H SiC SBD 25°C: (a) forward bias; (b) reverse bias.

The Schottky barrier height (ϕ_B) and the specific on-resistance (R_{on}) for the Ni/4H-SiC diodes was found to be 1.31 eV and 8 mΩ-cm^2, respectively. The saturation current density was found to be 4.7×10^{-15} A/cm^2. Both Ni and Pt diodes were able to withstand reverse voltages in excess of 1000 V. Some diodes had a breakdown voltage as high as 1200 V. Under reverse bias of 600 V, leakage current densities of 1.14×10^{-6} and 3.6×10^{-4} A/cm^2 were measured for the Pt and Ni diodes. The current "on-off" ratio (corresponding to

J_F at 2 V, divided by J_R at -600 V) was measured at 25°C to be 1.623×10^8 and 2.85×10^6 for the Pt and Ni diodes.

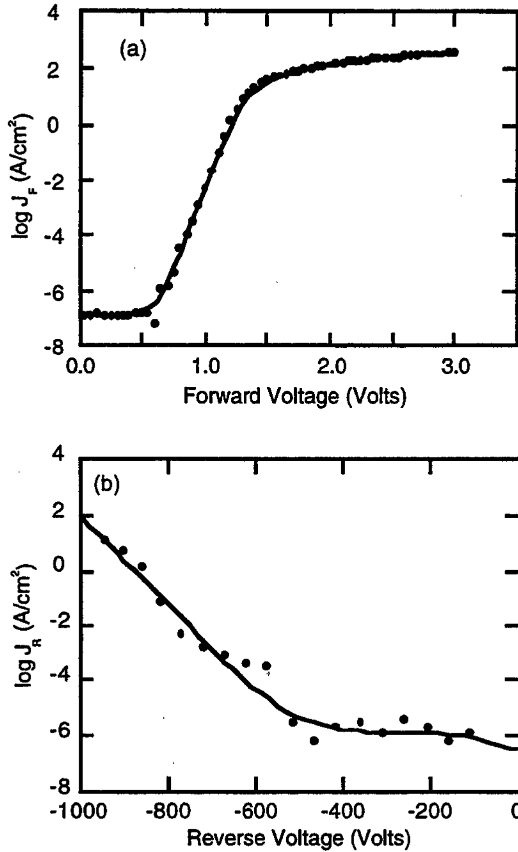

FIG 3. Current - voltage characteristics of a typical Ni/4H SiC SBD at 25°C: (a) forward bias; (b) reverse bias.

High temperature tests on Ni SBDs on both 4H and 6H have been performed. Fig. 4 shows the forward drop for these diodes versus temperature for current densities 1, 10 and 80 A/cm^2. Fig. 5 shows the current density at a reverse bias of 500 V versus temperature for Ni SBDs on 4H and 6H. The leakage current in SBDs on 4H is two orders of magnitude lower at both 25 and 300°C. As seen from Table 1, the current on-off ratio for the 4H SiC diodes does not show a significant reduction with temperature up to 300°C, where this ratio is still in excess of 10^6.

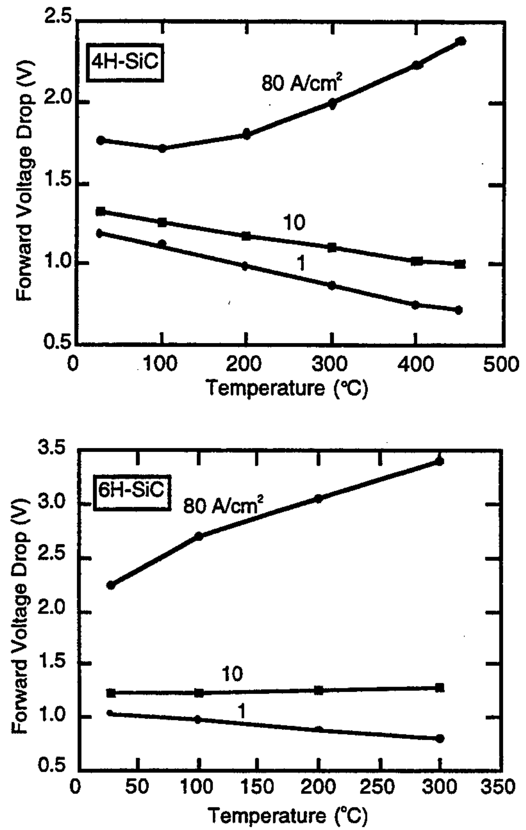

FIG 4. Forward voltage drop versus temperature for different current densities for Ni SBDs on 4H and 6H SiC.

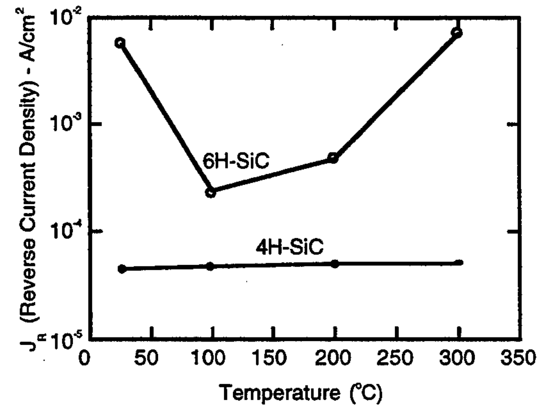

FIG 5. Current density at a reverse bias of -500 V as a function of temperature for Ni SBDs on 4H and 6H SiC.

Temperature (°C)	*J_{on} (2V)/J_{off} (-500V)*	
	4H-SiC	6H-SiC
27	2.85×10^6	324.3
100	2.69×10^6	7056.2
200	2.13×10^6	3221.2
300	1.59×10^6	208.5

TABLE 1. Current on-off ratio vs. temperature for Ni SBDs on 4H and 6H.

4. Summary and Conclusions

High breakdown voltage Schottky barrier diodes with on-off current ratio in excess of 10^8 at room temperature for Pt Schottky diodes and 10^6 for Ni Schottky diodes on 4H SiC has been reported. The 4H SiC diodes show a lower reverse leakage current and lower forward drop for a given current density than the 6H diodes. Furthermore, the leakage current at room temperature in Pt/4H SiC was found to be lower than Ni/4H SiC. An explanation for these observations could be offered based on the presence of surface inhomogeneities [13] at the metal/SiC interface that may be resulting in the reduction of the barrier height in localized regions. These inhomogenieties could be dependent on: (i) the quality of the material (6H and 4H-SiC wafers were graded differently by the manufacturer); (ii) the damage induced during the respective metallization procedures. Our study has clearly found that the Schottky diodes on 4H-SiC are far less leaky than those on the 6H polytype. However, further investigation is necessary to verify if this is indeed correct for devices on materials of identical grades. Furthermore, for the same polytype (4H) Ni deposition by sputtering seems to result in more surface damage than Pt deposition by e-beam evaporation.

Ni/6H SiC and Ni/4H SiC SBDs have also been tested at elevated temperatures and show satisfactory operation up to at least 300°C. Ni/4H SiC SBDs have been operated under forward bias at temperatures as high as 450°C and Ni/6H SiC SBDs have been operated up to 300°C. The current on off ratio for Ni/4H SiC diodes is several orders of magnitude higher than for Ni/6H SiC diodes at all temperatures.

Acknowledgments

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ADVANCED PROCESSING OF GaN FOR ELECTRONIC DEVICES: PROGRESS AND PROSPECTS

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Abstract- Rapid advances in GaN and related materials are enabling impressive photonic and electronic devices. The material advances, however, must be coupled with processing and device design improvements to achieve the full utility of these materials. In this paper, progress in ion implantation and thermally stable W contacts are presented. Select literature results for electronic devices are also given to show the great potential of these materials to meet advanced systems needs in high-power microwave generation and power switching.

I. INTRODUCTION

GaN and related materials are now being developed for application to both high-power and high-frequency electronic devices [1]. This work is predicated on the attractive materials properties of these semiconductors as summarized in Table I. The key properties are the high saturation drift velocity, high dielectric strength (breakdown field), and the applicability of heterostructures that yield high carrier mobility's and sheet charge.

TABLE I: List of key materials properties of semiconductors (after Ref 1).

	Si	GaAs	SiC	GaN	AlN	diamond
Band gap (eV)	1.1	1.42	2.2-2.3	3.45	6.2	5.45
electron saturation velocity (x10^7 cm/s)	1.0	1.0	2.0-2.2	2.2	?	2.7
dielectric constant	11.8	12.5	9.7-10	9	8.5	5.5
breakdown field (x10^5) V/cm	3	6	20-30	>10	?	100
Thermal conductivity (W/cm K)	1.5	0.46	4.9	1.3	3.0	22
electron mobility (cm^2/V s)*	1500	8500*	1000-1140	1250*	?	2200

* This is the bulk mobility. Heterostructure 2-DEG mobility's will be higher.

While GaN material was first investigated in the 1930's and the basic material properties have been know for many years, it has only been in the last several years that material quality has improved to the point where useful (and in fact now very impressive) devices could be realized [2, 3]. While continued material improvements will play a key role in additional device improvements, advances in device processing and novel device structures will also be required to achieve the full utility of this material system. In this paper, recent developments in two areas of process technology -- ion implantation and ohmic contacts -- will be discussed. Select electronic device results from the literature will then be reviewed to illustrate the potential for these materials. Future device directions will be suggested.

II. GaN PROCESSING

Si-implantation:

N-type implantation doping of GaN has been reported using both Si and O with initial results based on an activation anneal of ~1100 °C. Following the initial results it was discovered that although this anneal was sufficient to achieve electrical activity it did not significantly reduce the implantation induced damage in crystal the lattice [see Ref 2, p. 38]. It then became clear that to optimize this process to achieve higher carrier mobility's and lower sheet resistances, higher temperatures were required [5].

Unfortunately, GaN readily decomposes at temperatures above 1100 °C so a new approach to the annealing was needed. The two primary approaches to maintaining the GaN stoichiometry during heating are to encapsulate the sample with a suitable dielectric or to supply a high overpressure of activated nitrogen during the heating cycle. Both approaches have been investigated with electrical and structural results discussed here.

Previously it was reported that a sputtered AlN encapsulant is effective for maintaining the surface of GaN for annealing up to 1100 °C [6]. In that work the AlN deposition film had not been optimized for higher temperature annealing and started to fail (crack and blister) for temperatures of 1300 °C and higher [7]. Work is continuing on optimizing the AlN film with this approach expected to be the most manufacturable solution.

To explore the fundamental limits on implantation damage removal, unencapsulated, high-pressure annealing was studied. Si-implanted GaN was annealed for 15 min at up to 1500 °C and 15.6 kbar at the High Pressure Research Center at the Polish Academy of Sciences. The samples were implanted with Si at an energy of 100 keV and dose of $5x10^{15}$ cm^{-2}. This dose has been previously shown to introduce a high degree of lattice damage that can be observed by both channeling Rutherford Backscattering (C-RBS) and Cross-sectional Transmission Electron Microscopy (XTEM). The as-grown samples were highly resistive ($\rho_s > 10^8$ Ω/sq) and remained so after 1100 °C annealing. The samples were studied by Hall characterization and C-RBS before and after annealing.

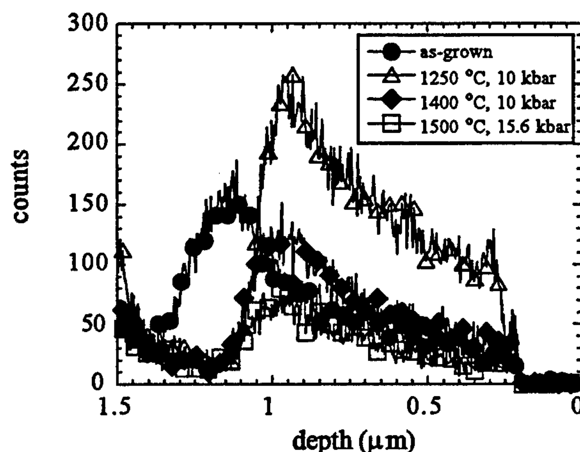

Fig 1. Aligned RBS spectra of three Si-implanted GaN samples annealed for 15 min at the conditions shown along with the spectra for a similar (but thicker) as-grown GaN sample.

Figure 1 shows a family of aligned C-RBS curves for as-grown and annealed samples. The as-grown samples had a minimum channeling yield of 2.0 to 2.4% while the as-implanted yield (not shown) increased to ~29%. The as-grown spectra in Fig 1 was for a 1.2 μm thick GaN film while the implanted samples where only 0.9 μm thick. This accounts for the difference in the trailing edge of the spectra. However, it is still appropriate to compare the minimum in each of the spectra to access the crystal quality of the samples. At the maximum annealing temperature of 1500 °C, the channeling yield of the implanted sample was reduced to 2.22%, equivalent to the as-grown material. The 1500 °C sample demonstrated a sheet electron concentration of $4.4x10^{15}$ cm^{-2} with a Hall mobility of 95 cm^2/Vs. This free electron concentration corresponds to 88% activation of the implanted Si and the electron mobility is in the range reported for epitaxially Si-doped GaN at this high concentration. This combination produces a sheet resistance of ~15 Ω/sq that, when applied to access regions, will markedly reduced the parasitic resistance of high power transistors.

Refractory Ohmic Contacts:

The realization of electronics that will operate under high current biases and/or high ambient temperatures will require robust Ohmic and gate contacts. Metallization schemes based on refractory metallization are attractive for these applications due to the high thermal stability of these materials. Tungsten has been used in various metallization approaches for GaAs and has recently also been the focus of a GaN contact study with a reported specific contact resistance of $4x10^{-5}$ Ω-cm^2 [8]. In this work, Si-

implantation doping is combined with sputtered W-metallization to produce low resistance, highly stable Ohmic contacts to GaN. GaN was implanted with Si-ions at dual energies (50 and 100 keV) and doses ranging from 5 to 100×10^{14} cm^{-2}. Samples were annealed at 1100 °C for 15 sec prior to sputter deposition of 300 nm of W. The tungsten was patterned into circular transmission line structures with a SF_6/Ar RIE plasma process. Figure 2 shows the current/voltage plot for W-contacts, as-deposited, on the different dose Si-implanted GaN. The two lowest dose samples are highly resistive and non-linear while the high dose samples demonstrated Ohmic behavior. The highest dose sample has a contact resistance of 0.54 Ω-mm, corresponding to a specific contact resistance of 5×10^{-6} Ω-cm^2, that remained unchanged to 700 °C. Testing to higher temperatures is underway and will be presented at the conference but earlier work of Cole, et al., suggests these contacts should survive heat treatments up to 1000 °C. As presented in the previous section, with an improved implantation activation anneal the sheet resistance in these samples will be further reduced and the specific contact resistance will similarly be reduced.

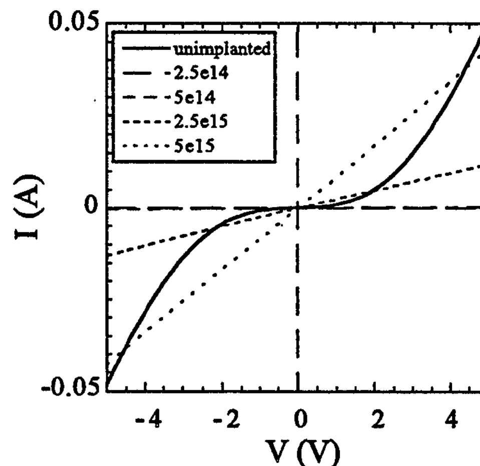

Fig 2. As-deposited W on Si-implanted GaN for different Si doses.

III. GaN-BASED ELECTRONIC DEVICE PROSPECTS: High-Power and High-Frequency

While the material quality of present state-of-the-art GaN is still far from ideal, very impressive electronic devices have been reported. A few key results from the literature are noted below to demonstrate the progress and potential in this area.

Microwave Power Devices:

The AlGaN/GaN heterostructure has been shown to yield a Two Dimensional Electron Gas (2-DEG) with very high carrier concentrations (~1×10^{13} cm^{-2}) and high mobilities (1700 cm^2/Vs) [9]. This has led to unity current gain curt off frequency up to ~50 GHz and a maximum frequency of oscillation approaching 100 GHz for a 0.12 μm gate length AlGaN/GaN FET[10]. Recently it has also been reported that the strain at this interface plays a key role, via the piezoelectric effect, of enhancing the sheet charge associated with conventional modulation doping (i. e. that due to the conduction band discontinuity of the heterostructure) to give the high sheet charge. Fortuitously, the piezoelectric effect also acts to expand the gate/drain depletion regions in AlGaN/GaN HEMTs and thereby reduce hot carriers in this region and increase the breakdown voltage [11]. This has led to the report of GaN-based pseudomorphic HEMTs with 2.57 W/mm of gate periphery at 10 GHz [12].

High-Power Switching:

Wide bandgap semiconductors are now being actively developed for high-power switching elements for applications such as electric vehicles, more electric aircraft, and onboard power conditioning. There is also increased demand for advanced power control for utilities. To date, these applications have been served by Si-based electronics. However, as the power levels (both current and voltage) are increased, Si-based technologies are not expected to be sufficient. Again GaN-based devices are expected to have impact in this

area but they will have to compete with silicon carbide devices. Presently, SiC-based power switching devices are well ahead of GaN-based devices partly due to the availability of SiC substrates that enables vertical device structures. An example of a vertical SiC switching device is the 1.1 keV UMOS FET [13]. Recently, a lateral SiC power switching device has also been developed, a SiC Lateral Depletion Metal Oxide Semiconductor Field Effect Transistor (LDMOS), that stands-off 2.6 kV [14]. SiC-devices clearly have a foothold in this area, however, if GaN substrates are developed; or lateral device structures are implemented; or faster switching speeds are needed; then GaN-based power switching will be attractive.

IV. CONCLUSION

Advances in material quality and device process technology are rapidly pushing GaN-based electronics to the forefront for microwave power generation. In particular, results were presented for work on n-type Si-ion implantation and low resistance W-ohmic contacts to GaN. Key results from the literature where summarize showing the progress of electronic device technologies. Future opportunities in this material system were also suggested.

V. ACKNOWLEDGMENT

The implantation and contact work was performed while one author (JCZ) was with Sandia National Laboratories. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy supported under contract #DE-ACO4-94AL85000.
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6H-SiC MOS STRUCTURES FOR HIGH TEMPERATURE APPLICATIONS

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Traditional integrated circuits use silicon devices. Silicon and silicon-on-insulator electronics together may be sufficient for some applications for temperatures up to 300°C [1]. Such applications might include digital logic, some memory technologies, and some power devices. Silicon-based technology will not be sufficient for many applications at the temperature above 250°C [1]. This temperature limitation will become lower when high temperature, high power, high radiation environment are combined in high-speed device operations. Wide bandgap semiconductors, however, are suitable for these types of applications [1].

Of all the wide bandgap semiconductors, silicon carbide has enjoyed the longest history and greatest development on both materials growth and device realization.

To investigate the possibility of using SiC MOSFETs for high-temperature applications, C-V characteristics of SiC MOS structures were studied in detail.

The 6H-SiC MOS structures used in this study were supplied by Ioffe Institute, Russia [1, 2]. The MOS structures were fabricated on 6H-SiC Lely crystals Russia [1, 2], the metal layer is aluminum, and the thermally grown SiO_2 layer is 81 nm thick [3].

C-V curves were measured for the 6H-SiC MOS structures under illumination at a frequency of 1 MHz and different DC ramp rates of 200, 50, 20 and 10 mV/sec as a function of temperature starting from 25°C up to 300°C. Illumination was required for enhancing the generation of minority carriers for creating the quasi- or effective inversion layer within reasonable amount of time; otherwise, in the absence of illumination, only the deep depletion C-V curve was observed.

Figures 1 and 2 show the effects of temperature on silicon MOS and silicon carbide MOS C-V characteristics, respectively. In these two figures, the curves from the forward sweep are denoted by the suffix "f" and those from the reverse sweep are denoted by the suffix "r". The number associated with the notation represents the temperature of the measurement. It can be observed from the C-V curves that the silicon MOS structures do not exhibit high frequency C-V characteristics beyond 175°C. Whereas, the 6H-SiC MOS structures retain high-frequency C-V characteristics in the entire temperature range tested.

Under illumination, the C-V characteristics of SiC MOS structures at 1 MHz and a very slow DC ramp rate resemble the high frequency C-V characteristics [4] and clearly show the regions of accumulation, depletion, and high-frequency inversion.

Figures 3 and 4 show hysteresis effects in the SiC MOS C-V characteristic. The hysteresis effect indicates the presence of mobile ionic charges or dipoles in the MOS structure [5]. These mobile charges (or, dipoles) in the oxide have low mobilities at room

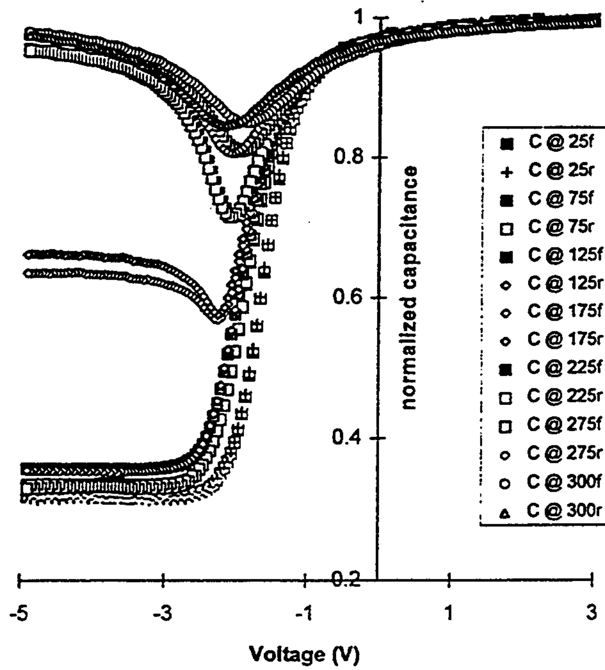

Fig. 1. The high-frequency normalized capacitance versus voltage (C-V) curve for silicon MOS structure as a function of temperature.

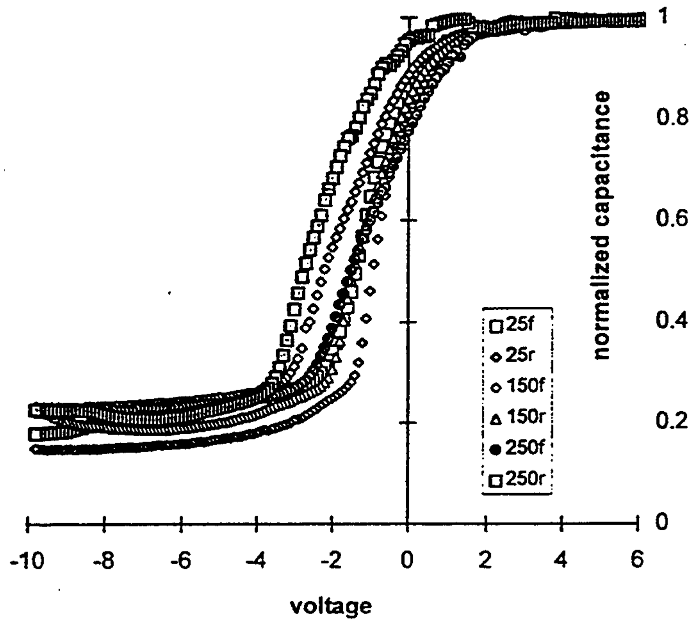

Fig. 2. The high-frequency capacitance versus voltage (C-V) curve under illumination for silicon carbide MOS structure as a function of temperature.

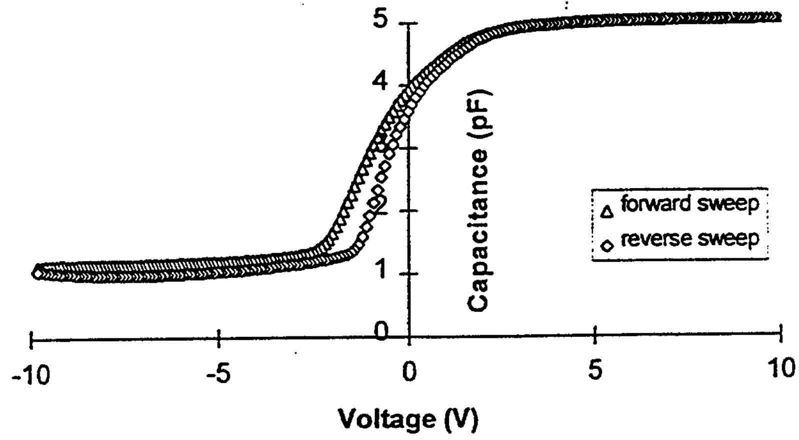

Fig. 3. The high-frequency C-V curve for SiC MOS structure at 25°C.

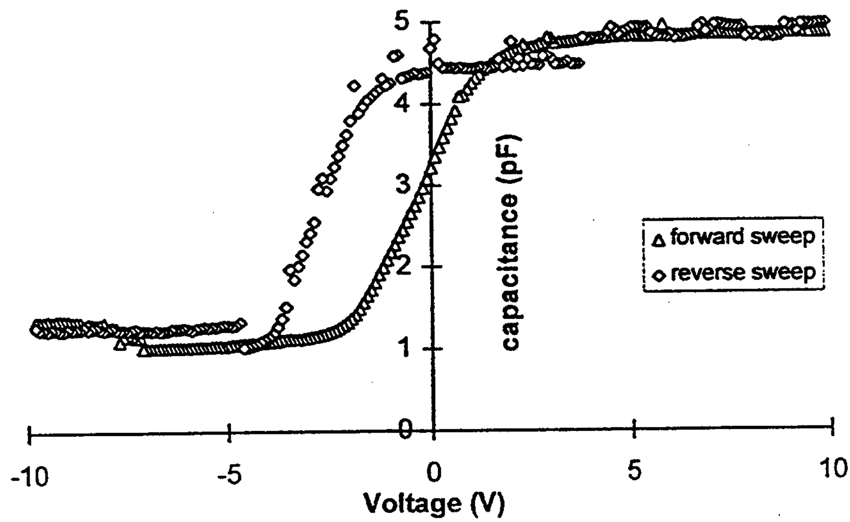

Fig. 4. The high-frequency C-V curve for the same device at 300°C.

temperature. However, temperature stressing causes the migration and redistribution of these mobile charges (or, dipoles), thus resulting in hysteresis effects in C-V characteristics [5].

It was observed that the SiC MOS structures have excellent thermal stability after pronged application of heat; but the existence of mobile ionic charges or dipoles in the oxide indicates that the oxide quality should be improved.

In conclusion, the SiC MOS structures are promising for high-temperature applications; however, the oxide and interface quality needs further improvement prior to he fabrication of SiC MOSFETs for high temperature applications.

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Innovative Approaches and Recent Progress in Doped Channel GaN/AlGaN Heterostructure Devices

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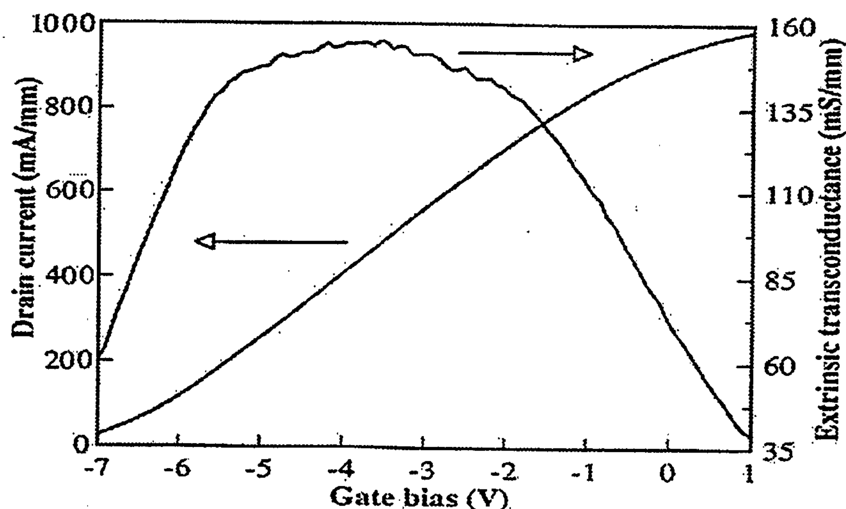
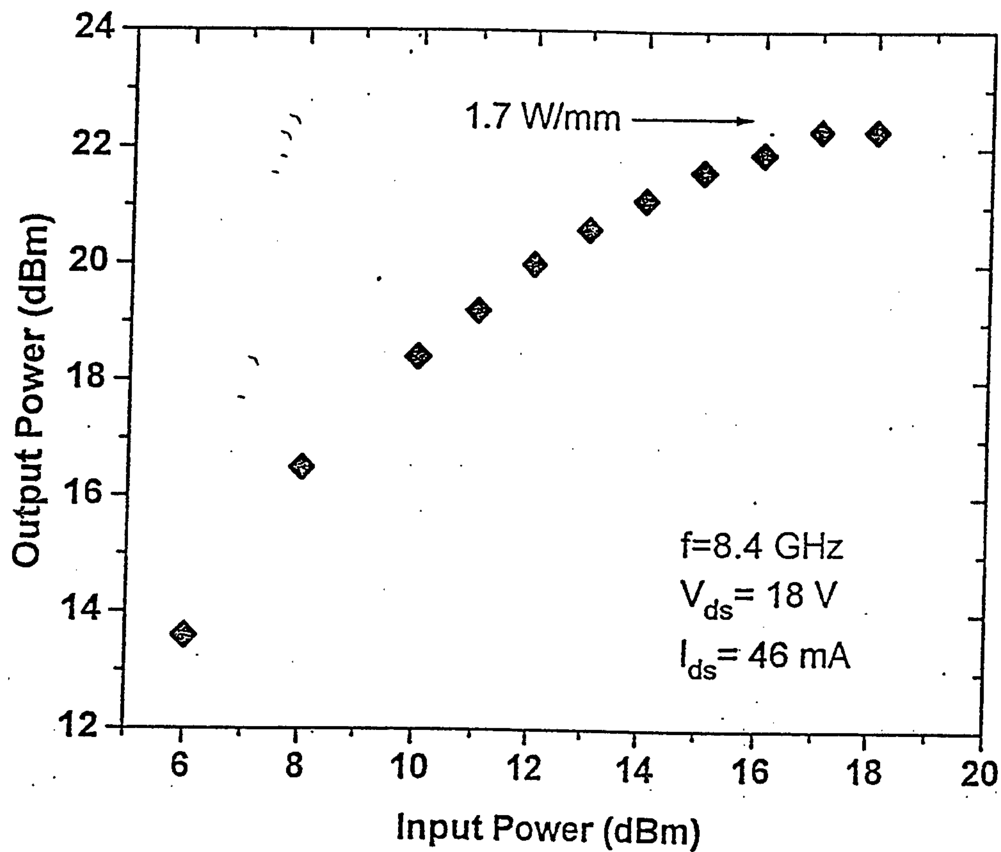
Due to their unique transport and optical properties, GaN/AlGaN heterostructures are currently under intense development for high-power microwave devices. In the past, Khan et.al. (c.f. MRS Bulletin, February 1997, page 44) demonstrated MESFETs, MISFETs and Heterojunction Field-Effect-Transistors (HFETs) based on unintentionally lightly doped GaN/AlGaN layers. They showed these devices to have transconductance values around 25-50 mS/mm. These low values were shown to be series resistance limited. Later using experimental results from optically illuminated HFETs Khan and Shur et.al postulated a doped channel design for these devices to be superior due to the potential lower series resistance and better contact formation due to the higher carrier densities.

Using the doped channel design, impressive rf and DC performance results were obtained for HFETs fabricated over sapphire substrates. In figure 1, we include the transfer characteristics for a 0.25 micron gate device (2 micron s-d opening). As seen, saturated



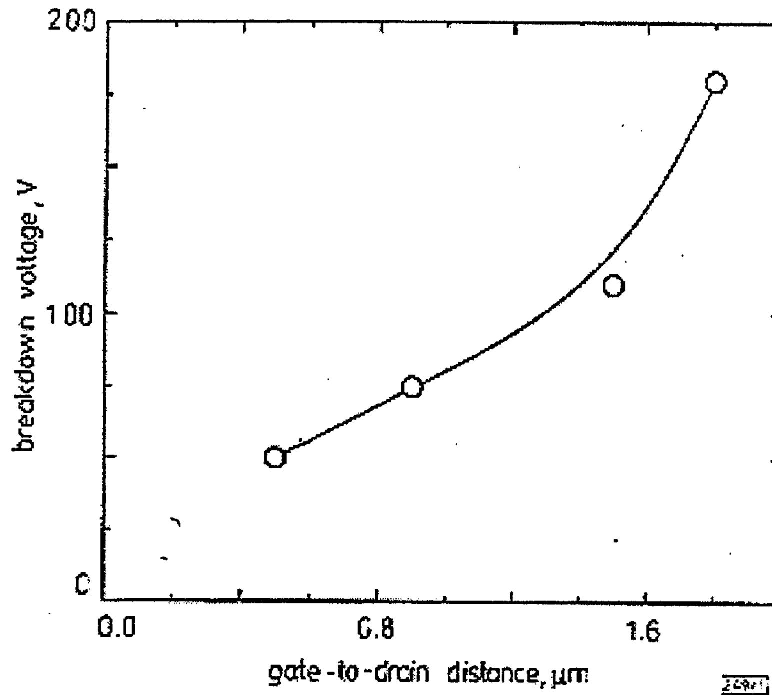
currents in excess of 1A/mm are obtained. The transconductance for these devices was measured to be in excess of 150 mS/mm. The ft and fmax values were measured to be

around 36 and 80 GHz. In figure 2, we show the rf power as a function of frequency for these devices with a value of 1.7 W/mm at 8 GHz. These devices also showed gain up to frequencies as high as 18 GHz. Two significant performance problems were encountered with these devices. First, the break-down voltages were invariably between 25-50 volts. Second, the source drain curves showed a negative output conductance at higher voltages. We identified this to be a result of heating affects due to the high dc power values.

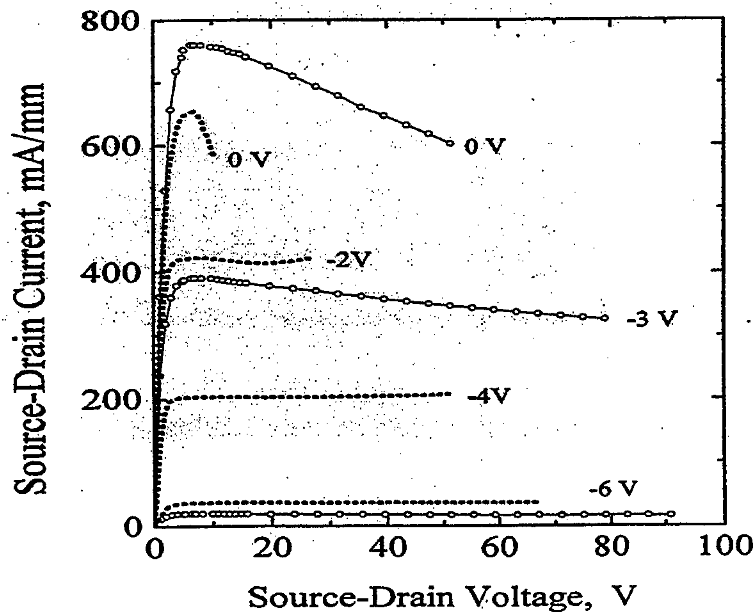


We then developed a unique off set gate design for the doped channel HFETs. Using this breakdown voltages as high as 200 volts were obtained for devices when a 4 micron source drain opening.

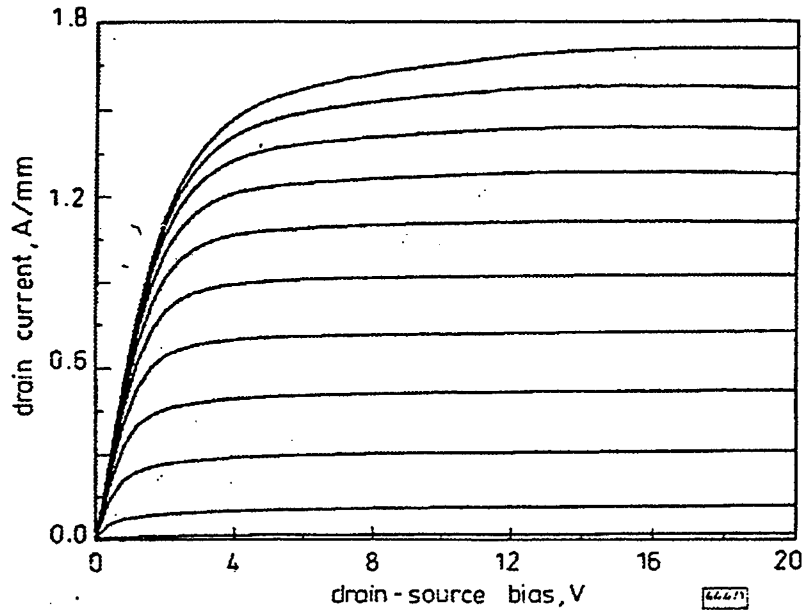
In figure 3 we show the variation of breakdown voltage as a function of gate-to-drain distance.

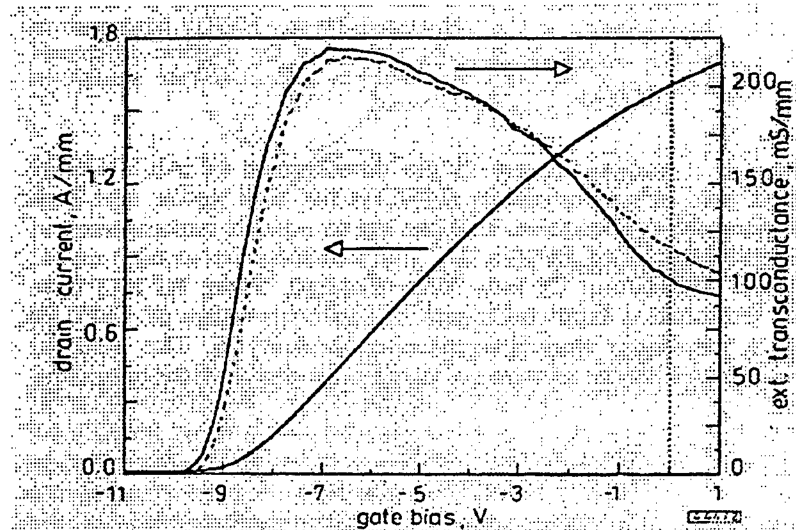


We identified the poor thermal conductivity of sapphire substrate to be the main cause of the device heating resulting in the negative conductance at high drain currents. To overcome this problem, we have recently developed GaN/AlGaN HFETs on high thermal conductivity 6-H SiC substrates. In figure 4 we include the s-d curves for 1.1 micron gate length HFETs on sapphire and silicon carbide substrates.



As seen the SiC based devices can withstand much higher dc powers without showing the negative transconductance. In figure 5a we include the s-d characteristics curves for a 0.25 micron gate HFET on SiC substrate. Saturated currents as high as 1.7 A/mm was measured. This represents one of the highest reported values to date. In figure 5b we include the transfer characteristics of this device. A maximum transconductance of 222 mS/mm was measured. This also is one of the highest values reported for SiC based GaN/AlGaN HFETs. In this presentation, we will discuss these results along with those from other research groups.





Transfer characteristics of HFET with offset gate

——— HFET with offset gate
- - - - HFET with symmetric gate
Both devices had the same S-D spacing (2μm)

Metal/Ferroelectric/Semiconductor (MFS) Diodes on SiC for Irradiation Hard Memory Applications

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1. INTRODUCTION

Both SiC and Ferroelectrics have been extensively studied in recent years for various applications. The lead base ferroelectric films are highly resistant to ionizing radiation and have high switching speeds (about 10 ns). They have been proposed to be integrated with existing Si and GaAs circuits for high speed, nonvolatile, random access memory applications [1, 2, 3]. In principle, a metal-ferroelectric-semiconductor (MFS) transistor should be particularly important for realizing non-destructive readout type nonvolatile RAM devices. However, the processing temperature for fabricating ferroelectrics is typically in the range of 500°C to 700°C, which can cause serious interdiffusion between the lead base ferroelectrics and Si or GaAs substrates [4, 5]. This reaction between ferroelectrics and Si or GaAs is a serious concern for the fabrication of MFS devices and non-destructive read-out MFSFET devices on these substrates. Therefore, a stable semiconductor substrate which could eliminate interdiffusion with the ferroelectric films is highly desirable.

SiC has a wide band gap, high saturation electron drift velocity, high thermal conductivity and very good chemical stability. The present development of SiC substrates make them very attractive for high frequency, high power, high temperature and irradiation hard environment applications. Single crystal 6H and 4H SiC substrates are commercially available [6]. However, thermal silicon dioxides on SiC are not good enough now because of too high levels of trapped charges. AlN is suggested as an alternative for gate material, but it is facing similar challenges in terms of high interface trap density. Accordingly, it is desirable to examine integration of other oxides on SiC. Ferroelectrics could be an interesting alternative. The large Si-C bonding energy of SiC ensures its stability at high temperatures. The reaction between ferroelectrics and the SiC is expected to be low at the ferroelectric film fabricating temperature. Furthermore, high dielectric constant of ferroelectrics ensures electric field in SiC is higher than that of in ferroelectrics at the interface, which is advantage to avoid breakdown of the dielectrics. Therefore, it is very interesting to investigate the properties of ferroelectrics on bare SiC substrates for high density, high speed and irradiation resistant devices. In this work, we first report the fabrication and properties of metal/PbTiO3/SiC diodes.

2. EXPERIMENTAL PROCEDDDURE

The pulsed laser deposition technique was used to deposit PTO($PbTiO_3$) films on SiC substrates. The substrates used in this study were n-type (N_d = $10^{18}cm^{-3}$) 4H SiC single crystal wafers. Before the deposition, the SiC substrates were degreased in organic solvents trichloromethyl, ethylene, propanol and acetone, followed by etching in H_2SO_4:H_2O_2(3:1) for 5 minutes and final a dip in diluted HF(10:1) solution for 30s. We list the deposition conditions in Table I. MFS diode structures were fabricated by evaporating gold dots ($2.8x10^{-3}cm^2$) through a shadow mask on top of the ferroelectric films acting as top electrodes, the bottom ohmic contact electrodes were made by

Substrate temperature(°C)	350 to 650
Energy density	2.5 J/cm^2
Substrate-target distance	55 mm
Oxygen gas flow	60 sccm
Laser wavelength	355 nm
Oxygen pressure	$280x10^{-3}$ mbar
Laser pulse frequency	10Hz
Cooling rate(in O_2)	60°C/min
Film thickness	450 nm

Table 1. Deposition conditions of PTO films on 4H-SiC (n-type)

pasting of InGa on the backside of the SiC for electric measurements. The schematic cross-section of the MFS diodes is shown in Fig. 1. In the following discussion, a positive voltage means a positive potential applied to the top gold electrode. The crystal structure of the films was examined by X-ray diffraction (XRD). The C-V curve and capacitance versus frequency measurements were carried on a HP 4284A LCR meter. The I-V curves were measured by a HP4145B parameter analyzer.

3. RESULTS AND DISCUSSIONS

The crystal structure of the PTO films vary with the film deposition temperature. For a substrate temperature less than 350°C, the films were mainly amorphous. With increasing substrate temperature, the films started to crystallize into a pyrochlore phase dominated structure. The films deposited at 550°C were a mixture of the pyrochlore phase and a perovskite phase. When the deposition temperature arise to 600°C or higher, the films with pure perovskite phase were obtained. Fig. 2 shows the X-ray diffraction (XRD) pattern of the PTO film deposited at 650°C. All X-ray diffracting peaks were identified belonging to the perovskite phase, there was no pyrochlore phase peak or unidentified peak observed. From the XRD data, we cannot find any observable interdiffusion between the PTO film and the SiC substrate. The crystal structure of the film was polycrystalline with random orientation.

As the voltage was swept from negative to positive voltage, the Au/PTO/SiC diodes show current-voltage characteristics similar to common p-n junction diode. Fig. 3 shows a typical leakage

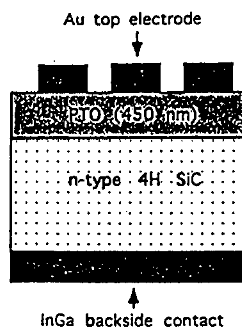

Figure 1. The schematic cross-section of the MFS diode structure.

current versus voltage curve for the Au/PTO/SiC diodes. The room temperature resistivity was in the region of 10^{10} to 10^{11} Ωcm up to 5V corresponding to a field of 110 kV/cm across the PTO layer. The leakage current exhibits ohmic behavior at low fields and nonlinear conductivity at high fields.

We would like to discuss various conduction mechanisms giving rise to the observed I-V characteristics. Since there are no highly mobile ionic species in our films and the thickness of the films is 450 nm, tunneling and ionic conduction can not be the main conduction mechanism in these diodes. The leakage current is extremely temperature dependent, this implies that a space-charge-limited-current conduction is not the dominant mechanism neither. The Schottky effect is the image-force induced lowering of the potential energy for charge emission when an electric field is applied. It will occur at the interface between the ferroelectric film and the electrode where the Schottky barrier is formed. If the top and bottom interfaces are not the same, then leakage current levels will be asymmetric for positive and negative voltage biases. Poole-Frenkel emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band of the n-type SiC, it could happen via trap levels in the bulk, so current conduction controlled by this mechanism will give symmetric current levels in both positive and negative polarities regardless of asymmetric contacts. The Au/PTO/4Hn-SiC diodes demonstrate obvious changes in the conductivity with changing polarity of the applied voltage as shown in Fig. 3, which indicated Schottky emission played a important role in the conduction process.

According to the thermionic emission theory [7], the forward current-voltage. characteristics of a Schottky diode can be expressed as

$$J=A^{**}T^2\exp(-q\varnothing_b/kT)\{\exp(qV/nkT)-1\} \quad (1)$$

where A** is the Richardson constant, q the electronic charge, $\varnothing_b$ the Schottky barrier height, V the voltage applied across the diode, k the Boltzman constant, T the absolute temperature, and n the ideality factor. For $V > 3kT/q$, equation (1) becomes

$$J = J_0\exp(qV/nkT) \quad (2)$$

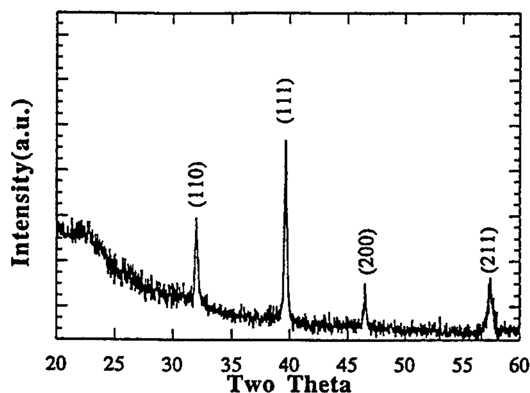

Figure 2. θ-2θ XRD pattern of the PTO film deposited at 650°C.

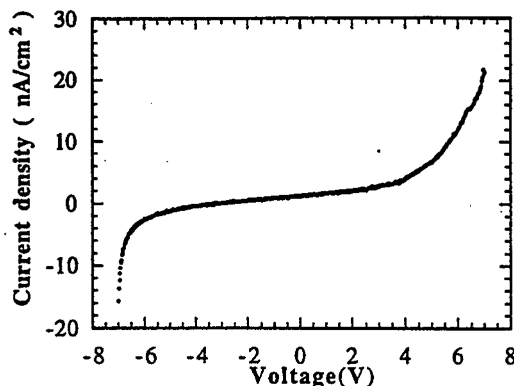

Figure 3. Bipolar leakage current density versus voltage showing an obvious asymmetry.

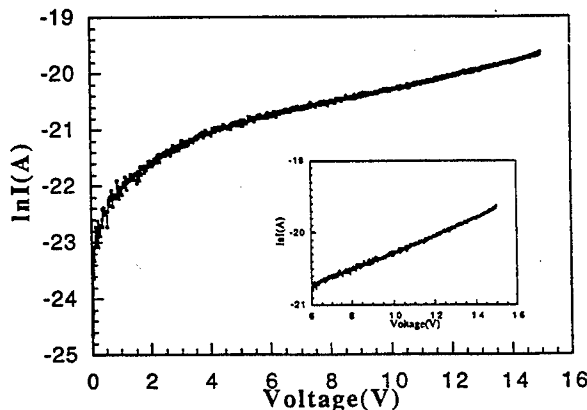

Figure 4. The lnI versus voltage curve demonstrates Ohmic behaviour in lower voltage region(<3V). The inset indicates in higher voltage region(>6V) the I-V curve follows Schottky relationship.

$$J_0 = A^{**}T^2\exp(-q\varnothing_b/kT) \quad (3)$$

In order to compare the experimental data with theory, the forward current-voltage characteristic curve obtained at room temperature is plotted semilogarithmicly in Fig. 4. There are two distinct I-V regimes existing in the curve. At low voltage region, the current is proportional to the applied voltage, this Ohmic behavior is common in ferroelectric films [8, 9, 10, 11]. However, at higher applied voltages, the leakage current is exponentially dependent on the applied voltage. The inset in Fig. 3 indicates that the current-voltage dependence in the high voltage regime follows a Schottky relationship quite well.

The capacitance-voltage (C-V) characteristics were measured by sweeping the voltage from negative bias to positive bias and back to negative bias. A typical C-V curve for these diodes is a hysteresis loop. With higher applied voltages, the loops have larger memory windows which is the difference of the bias voltage near the flat band capacitance. Fig. 5 shows the evolution of the hysteresis loops with the variation of the applied voltages, so the ferroelectricity of the PTO layer is confirmed. The direction of the hysteresis loops is clockwise, this indicates that the shift of the flat band voltage is due to carrier injection rather than a remnant polarization of PTO films [12]. The dielectric constant is about 32, which was calculated in the accumulation voltage region using a frequency of 1 MHz. This dielectric constant value is lower than the reported values (90 to 130) for PTO films [13, 14] in metal-ferroelectric-metal(MFM) structures, but it agrees well with the reported result for PTO with MIS structure [15]. The dielectric constant and the conductance of the diodes are frequency dependent. Fig. 6 shows the variation of the dielectric constant and the conductance with frequency. It is easy to see that the dielectric constant monotonously decreases with the increasing frequency, however, the conductance is almost linearly proportional to the frequency. There are many dipoles in the PTO layer, when they switch from one state to another, a relaxation time is necessary and it may vary from dipole to dipole. At lower frequencies, all dipoles will respond, but at higher frequency, dipole with larger relaxation time will not switch and the overall dielectric constant decreases.

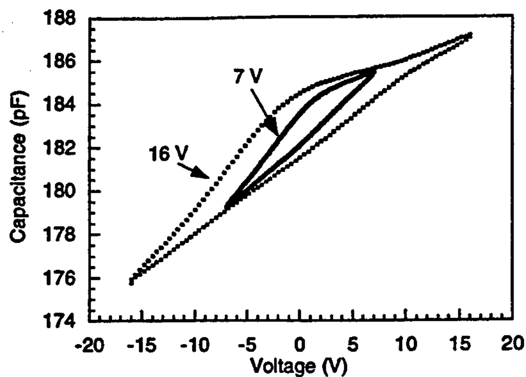

Figure 5. Evolution of the ferroelectric hysteresis loops at different applied voltages for PTO film deposited at 650°C.

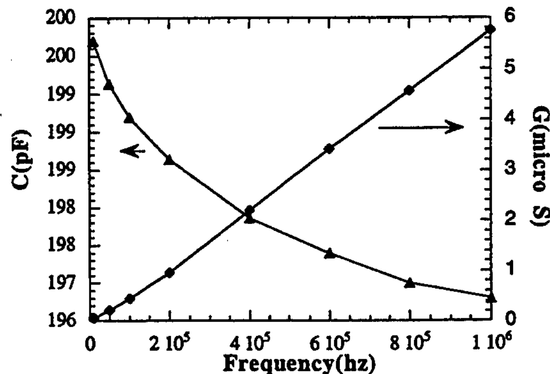

Figure 6. The frequency dependence of the dielectric constant and the conductance of the PTO film deposited at 600°C.

4. CONCLUSIONS

The crystal structure of PTO films are controlled by the deposition temperature. At a temperature window from 600°C to 650°C, polycrystalline PTO films with perovskite structure can be deposited in-situ on SiC substrates. XRD patterns indicate that interdiffusion between the PTO films and the SiC substrates is limited as expected. The dielectric constant and the resistivity of PTO films become smaller at higher frequency. The current-voltage characteristics at lower applied voltage exhibits Ohmic behavior, but at higher voltages, it becomes Schottky effect controlled. Typical hysteresis loops for MFS diodes were observed in the C-V measurements, thus the ferroelectricity and memory effect of the PTO films were confirmed. The carrier injection mechanism controlled the shift of the flat band voltage in these diodes. This study shows that PTO is a promising candidate to serve as gate oxide for a MFS field-effect-transistor (FET) or dielectrics for a MFS diode on SiC substrates.

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High-Speed Resonant Cavity Enhanced Schottky Photodiodes

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I. Introduction

Schottky photodiodes (PD) are very attractive for high-speed photodetection, because of their simple material structure and fabrication process. This enables easy integration with III-V discrete devices and integrated circuits [1]. With the increasing demand for higher bandwidth detectors, the optimized structure of a Schottky PD typically requires a thin absorption region. However, a thin absorption region necessarily results in a reduction in quantum efficiency at wavelengths where the absorption coefficient of the semiconductor material is relatively small. Although high performance Schottky photodetectors with semi-transparent metal contacts have been successfully fabricated [1,2], the bandwidth efficiency product has remained limited by the material properties.

Over the past several years a new family of optoelectronic devices has emerged whose performance is enhanced by placing the active device structure inside a Fabry-Perot resonant microcavity [3]. In such resonant cavity structures, the device functions largely as before, but is subject to the effects of the cavity. As a result, the bandwidth-efficiency product is drastically improved [3,4]. The resonant cavity enhanced (RCE) detection scheme is particularly attractive for Schottky type photodetectors, since the semi-transparent Schottky contact can also function as the top reflector [5]. RCE detectors with single layer top mirrors as opposed to utilizing multi-layer reflecting coatings such as distributed Bragg reflectors(DBR) also benefit from post-growth adjustment of the resonant wavelength by simply recessing the top layer [3,6]. Recently, we demonstrated RCE Schottky photodiodes with a 3-dB bandwidth of 100 GHz. In this paper, we present theoretical and experimental results on spectral and high-speed properties of RCE Schottky photodiodes with semi-transparent top metal contacts. The optimization of the device structure is discussed for quantum efficiency and response speed.

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II. Device Structure

We studied RCE Schottky diodes on GaAs operating at 900 nm wavelength. Similar principles may be applied to other III-V materials and different wavelength regions. A schematic representation of the layer structure is shown in Fig. 1. The device structures were grown on GaAs by molecular

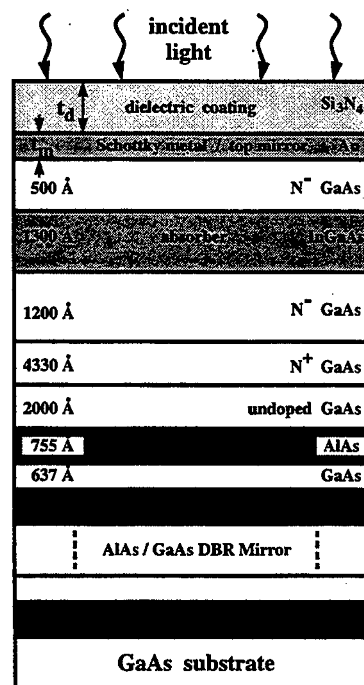

Fig. 1. Schematic representation of layer structure of RCE Schottky photodiodes with semi-transparent top metal contact.

beam epitaxy. The resonant cavity is formed by a GaAs/AlAs DBR bottom reflector and the semi-transparent Au contact on top. A 0.2 μm undoped GaAs region on top of the DBR mirror is utilized for electrical isolation. A thick n^+-GaAs layer is used for ohmic contact. The normally depleted region of the Schottky PD consists of a combination of lightly doped GaAs and InGaAs layers. The active absorption layer consists of InGaAs with an In mole fraction less than 10% to avoid misfit dislocations. At the operation wavelength, only this InGaAs region absorbs the optical excitation and the rest of the device structure is nearly lossless. The thickness of the InGaAs layer is 130 nm to eliminate the standing wave effect [3] in the cavity to assure wavelength independent quantum efficiency at resonance. The position of the absorption layer in the depletion region is optimized to yield minimum transit time for electrons and holes [3]. The interfaces between the InGaAs and GaAs regions are graded to avoid carrier trapping. The devices were fabricated by standard photolithography and mesa processes and the Schottky contact was formed by Au evaporation. On top of the Schottky metal, a dielectric layer (Si_3N_4) is used to optimize detector responsivity.

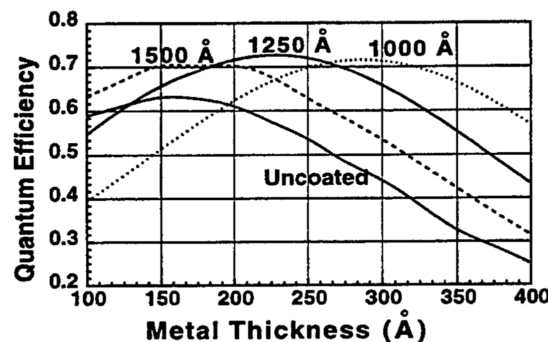

Fig. 2. Simulated quantum efficiencies of RCE Schottky photodiodes as a function of Au thickness, with no anti-reflection (bottom solid), 1000 Å(dotted), 1250 Å(top solid), 1500 Å(dashed) Si_3N_4 coatings.

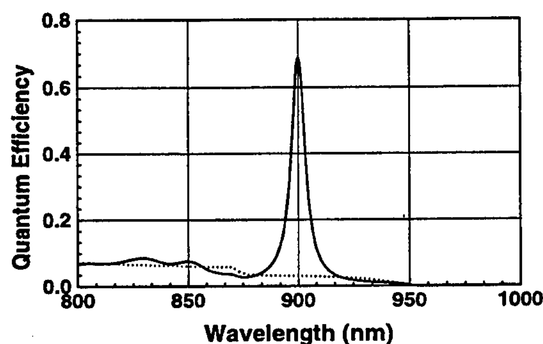

Fig. 3. Theoretical comparison of the quantum efficiency of an optimized RCE Schottky PD and a conventional Schottky PD with a thin absorber (dotted line).

III. Optimization of Quantum Efficiency

For thin absorption layer RCE Schottky PDs, a high top mirror reflectivity (around 70%) is required to obtain maximum quantum efficiency. The top mirror reflectivity can be controlled by the thickness of the semi-transparent Schottky metal. To obtain the optimal reflectivity a relatively thick metalization is needed. However the increasing optical losses in the semi-transparent metal layer lead to a reduction of the quantum efficiency for top illuminated devices. We analyzed the dependence of responsivity on the thicknesses of the metal contact and the dielectric coating . Via simulations, we demonstrated that these thicknesses can be optimized to yield nearly 75% quantum efficiency at resonance for the thin(130 nm) absorption region. Figure 2 illustrates the results of these simulations showing the variation of peak resonant quantum efficiency with the metal thickness for various dielectric coating thicknesses. It can be observed in Fig. 2 that dielectric coating on top of the Schottky metal allows for the use of thicker metalization for the optimized quantum efficiency of the RCE photodiode. As thick as 300 Å Au Schottky metal can be used without reducing the peak quantum efficiency. To emphasize the advantage of RCE detection, in Fig. 3, we plot the quantum efficiencies of an optimized RCE Schottky PD and a conventional (one-pass) detector with identical absorption layer and metal thickness. The RCE detector displays a 10 fold improvement in quantum efficiency.

The Schottky PDs designed for 900 nm operation were fabricated with 200 Å Schottky Au and 1250 Å Si_3N_4 anti-reflection layer using the optimum values obtained from the simulation results. The photodiodes of various sizes were fabricated by standard photolithography with mesa isolation and a Au airbridge connecting the top contact to a

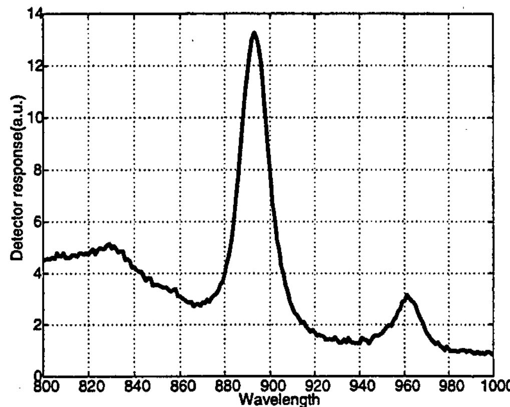

Fig. 4. Experimental spectral response of RCE Schottky photodiodes designed for 900 nm wavelength.

co-planar transmission line. The resulting devices showed breakdown voltages larger than 12 V. Large mesa devices were used in spectral response measurements using a monochromatic light source. The resonant peak is observed at 895 nm with a 6 fold resonant enhancement(See Fig. 4). The measured peak quantum efficiency was about 20% which is significantly less than the theoretical value. The discrepancy is due to the red shift in the center wavelength of the bottom DBR mirror resulting in a ~60% bottom reflectivity. Optimized device structure is expected to yield ~70% quantum efficiency. We have demonstrated quantum efficiencies as high as 46% on similar devices operating at 830 nm [7].

IV. High-Speed Performance

Intuitively, RCE photodetectors are expected to have improved speed compared to conventional photodetectors because of the reduced active layer thicknesses which can be used. The most important response speed limitations in PDs are drift time across the depleted region, charging and discharging times of inherent and parasitic capacitances, the diffusion time for the carriers generated in the undepleted regions, and charge trapping at the heterojunctions. Good detector design minimizes the latter two by incorporating non-absorbing contact regions, grading the absorbing region heterojunctions, and placing the active layer in the depleted region. For small devices, the transit time limitation dominates the high-speed performance.

The RCE PD structure can incorporate a thin absorption region placed in a depletion region at an optimized position determined by the relative velocities of electrons and holes[8]. In this case the photogenerated carriers do not have to traverse the entire depletion region and the transit time is significantly reduced while keeping the junction capacitance small.

High-speed measurements were carried out using a picosecond mode-locked Ti/Sapphire laser tuned to 895 nm. The devices were illuminated using a single mode fiber on a microwave probe station and the resulting pulses were observed on a 50 GHz sampling scope. Figure 5 shows the pulse response of a $10 \times 10 \mu m$ RCE Schottky PD at zero bias. The full-width-at-half-maximum (FWHM) was measured to be 10 ps. Considering a 9 ps FWHM for the 50 GHz scope [9], and the laser pulse width(1.5 ps), the device speed was estimated to be 4.3 ps corresponding to a more than 100 GHz 3-dB bandwidth. This is a conservative estimate since the microwave components and laser timing jitter also contribute to the measured pulse width. To verify the transit-time limited operation of these devices we measured the response speed of various size devices. The devices with mesa sizes less than $20 \times 30 \mu m$ were not capacitance limited and resulting in 10 ps FWHM measurements.

For a direct comparison of the high-speed response of RCE and conventional PDs we performed high speed measurements at two different wavelengths. A $18 \times 28 \mu m$ detector was studied for the excitation wavelength dependence of the impulse response. We measured a 10 ps FWHM at 895 nm

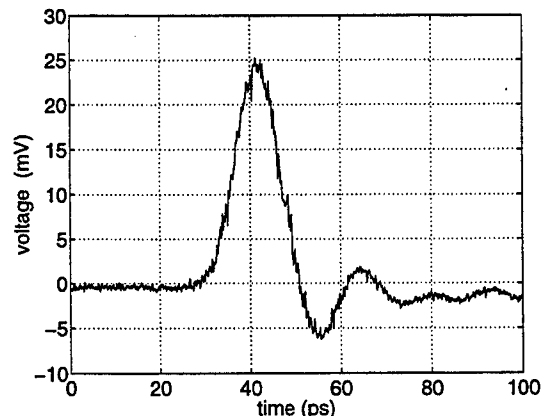

Fig. 5. Measured pulse response of the RCE Schottky PD measured at the resonant wavelength. The measured FWHM is 10 ps.

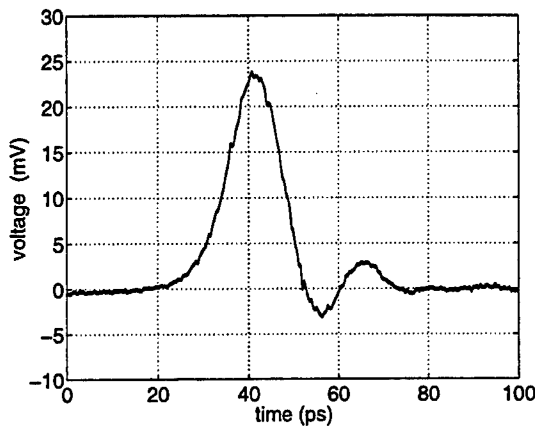

Fig. 6. Measured pulse response of the RCE Schottky PD measured at 845 nm wavelength. The measured FWHM is 13 ps.

where only the InGaAs region is absorbing the light excitation and the device functions as a RCE PD. The measured FWHM was 13 ps at 845 nm (see Fig. 6) where the entire InGaAs/GaAs region is photosensitive and the device functions largely as a conventional photodiode. When we deconvolve the measurement setup response, we obtain 4.3 ps at 895 nm and 9.2 ps at 845 nm . This demonstrates a bandwidth enhancement more than twice with the RCE detection scheme as predicted by numerical simulations [8]. Together with the ~4 fold increase in the efficiency (See Fig. 4), the bandwidth-efficiency product of the devices is improved by a factor of 8 at resonance.

IV. Conclusions

We have demonstrated studied high-speed top illuminated RCE Schottky PDs with semi-transparent Au contact. The quantum efficiency was optimized by utilizing a top dielectric coating. The measured high-speed response agrees with theoretical predictions of expected improvement by RCE detection scheme. The 10 ps FWHM pulses measured on the scope are estimated to represent 4.3 ps FWHM impulse response, corresponding to a 3-dB bandwidth of 100 GHz. The optimized structure is expected to yield a bandwidth-efficiency product larger than 70 GHz.

Acknowledgments

The results described in this paper represent a multi-institutional effort with significant contributions from various researchers. The author would like to thank graduate students Bora Onat and Mutlu Gökkavas at Boston University, Department of Electrical and Computer Engineering, Prof. Ekmel Özbay, and graduate students M. S. İslam, and E. P. Ata of Bilkent University, Department of Physics, Prof. Gary Tuttle of Iowa State University, Microelectronics Research Center, and Prof. Elias Towe of University of Virginia, Department of Electrical and Computer Engineering.

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Mid-infrared electroluminescence and lasing in AlGaAsSb/InGaAsSb double heterostructures with asymmetric band offset confinements

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Recently there has been intensive research in mid-infrared III-V (MIR) semiconductor diode lasers emitting from 3 to 5 μm. An important application of these lasers is ecological monitoring and tunable diode laser spectroscopy. Antimonide based lasers operating up to 180-200K in pulse mode and 110-120K in cw mode were realized [1-4]. Novel type II laser structures using intersubband transition were demostrated [3,4]. Further progress in improving MID-IR laser performances is connected with new physical approaches for optimization laser structure desing. So, Kazarinov and Belenky in [5] proposed to use so-called stopper confined layers for electrons and holes in laser structure that can lead to reducing thermoionic emission of carriers out of the active region and help to reduce the hole leakage.

We report here first electroluminescence (EL) and lasing in MIR laser structures with high Al-content (64%) cladding layers (Eg=1.5 eV) and narrow-gap InGaAsSb active layer (Eg=0.326 eV at T=77K) LPE grown lattice-matched to GaSb substrate ($\Delta a/a<0.3\%$). Two kinds of DH diode lasers were fabricated on N- and P-GaSb substrates respectively. Laser structures consisted of the following layers: structure **A** N-GaSb/N-$Al_{0.64}Ga_{0.36}AsSb$/n-$In_{0.94}Ga_{0.06}As_{0.82}Sb_{0.18}$/P-$Al_{0.64}Ga_{0.36}AsSb$/P-GaSb and structure **B** with inverted sequence layers, but growing with the same composition of quaternary solid solutions, P-GaSb/P-$Al_{0.64}Ga_{0.36}AsSb$/p-$In_{0.94}Ga_{0.06}As_{0.82}Sb_{0.18}$/N-$Al_{0.64}Ga_{0.36}AsSb$/N-GaSb. Band energy diagrams of the DH laser structures had strongly asymmetric band offsets (fig.1a,b). Heterojunction between high Al-content layer and narrow-gap active

layer have a type II broken-gap alignment at 300K [6]. Using high asymmetric band offsets as stopper confined layers we expected also to improve some performance of our longwavelength laser structures.

Mesa-stripe laser structures with stripe width 11-45 μm and cavity length ~300 μm were made from **A** and **B** heterostructures. In **type A** laser structure spontaneous emission was obtained at λ=3.8 μm (hv=326 meV at T=77K) and λ=4.25 μm at room temperature which corresponds to energy gap of the active layer (Eg=326 meV at T=77K). Full width of half maximum (FWHM) of emission band was 34 meV (77K) and broadened up to 90-115 meV at 300K (fig.2a). Emission intensity changed linearly with drive current and decreased by a factor 30 from T=77K up to 300K. Lasing with single dominant mode was achieved at λ=3.776 μm (T=80K) in pulse mode (pulse duration 2-5 μs and repetition rate 100kHz. In this structure radiative recombination occurs into the active layer that corresponds to bulk recombination. Threshold current as low as J_{th}~60 mA and characteristic temperature T_o=26K were obtained.

In turn, in the **B-structure** an intensive spontaneous emission and superluminescence were obtained. Electroluminescence with very narrow bands (FWHM~10 meV at 77K and 30 meV at 300K) was observed (fig.2b). A blue shift of the emission band maximum up to 60-70 meV was found, in comparison with the case of the **A**-structure(See fig.1). Maximum of EL photon energy was hv=380-402 meV (λ=3.08-3.26 μm), in depending on drive current. Strong distinction in appearance of EL spectra in **A** and **B** structures we explain by differ origin of radiative recombination transitions. We suppose that in **B**-structure radiative recombination transitions occurs at the P-AlGaAsSb/p-InGaAsSb interface. It was supported also by electron beam induced current measurement. It is important to notice that similar electroluminescence spectra with the narrow emission bands was recently observed by us on type II broken-gap p-GaInAsSb/p-InAs heterojunctions [7] and was explained by tunneling-assisted radiative recombination of spatially separated electrons and holes localized in the adjacent quantum wells on the both sides of the interface. Observed blue shift of the emission band maximum can be explained satisfactory by strong electron confinement and carrier accumulation in the quantum well near the p-p interface [8].

In conclusion, two kinds of diode laser structures with high Al-content asymmetric band offset confined layers and narrow-gap InGaAsSb active layers were first grown lattice-matched to GaSb substrate by LPE method. Single mode lasing (λ=3.776 μm) was achieved at T=80-120K at in pulse mode in structure grown on N-GaSb substrate. High spontaneous emission was observed in temperature range 77-300K in the spectral region 3.5-4.4 μm in DH diodes grown on N-GaSb substrate and 3.0-4.0 μm in structures grown on P-GaSb one that demonstrate good prospect as new light-emitting diodes for gas pollutant control applications. Substantial performance improvement are expected by further optimization of the proposed laser structures and growing conditions.

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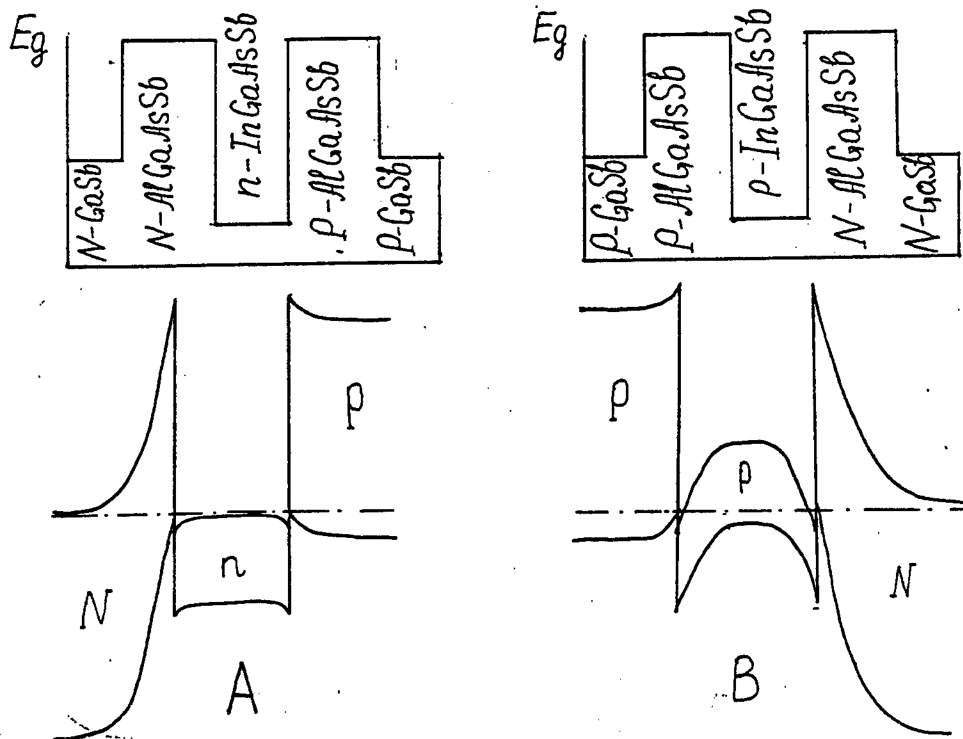

Fig.1. Schematic laser structures and energy band diagrams of **A** and **B** structures (See text)

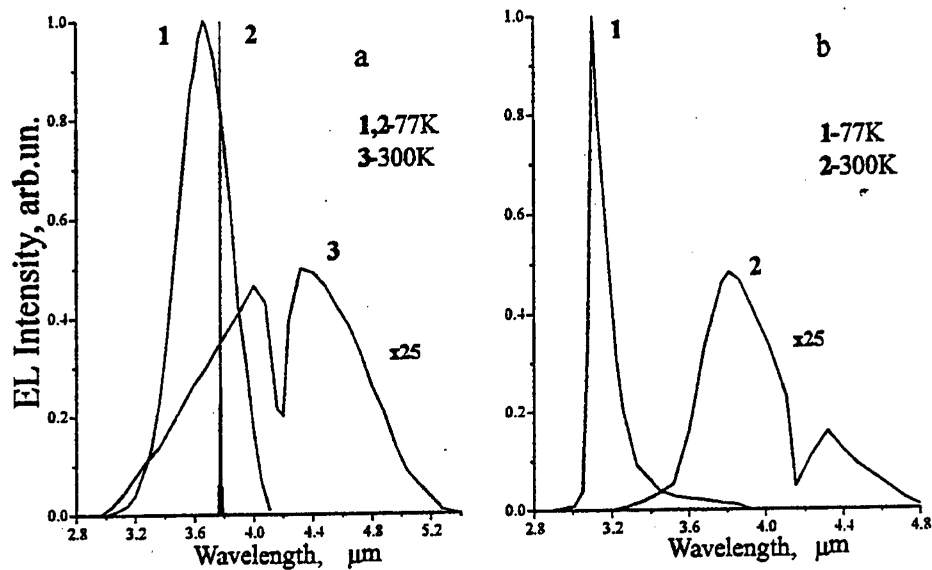

Fig.2, a) Spontaneous emission and lasing in **A** -structure; b) spontaneous emission in **B** -structure

Imaging of Spatial Modes of One Dimensional Photonic Band Gap Devices using Near-field Scanning Optical Microscopy

G. H. Vander Rhodes, J. M. Pomeroy, T. F. Krauss, M. S. Ünlü, and B. B. Goldberg

Abstract— **We have directly imaged the spatial modes inside a one-dimensional photonic band gap device using near-field scanning optical microscopy. Our results show large scattering at the transition between waveguide modes and lattice modes, as well as increased scattering for wavelengths within the stop band. Additionally, we present preliminary results on infrared imaging of the localized mode of a defect state at the center of the device. Eligible for Best Student Paper Award.**

Keywords— **photonic band gap, near-field scanning optical microscopy, spatial modes**

I. Introduction

The photonic band gap (PBG) approach to periodic dielectric structures provides a framework to explore optoelectronic devices using techniques that are familiar to workers in condensed matter physics and engineering[1]. Much of the motivation for this approach was developed through work done in inhibited spontaneous emission[2], where it was experimentally verified that an excited atom has a much longer decay constant when placed in a cavity that does not support the emitted photon[3][4]. Results in one-dimension were extended to two- [5] and three-dimensions [6], where it became useful to start applying concepts such as Brillouin zones, reciprocal lattices, and Bloch waves, familiar from basic condensed matter physics.

Inhibited spontaneous emission has led to application of PBG concepts to optoelectronic devices. In many devices, spontaneous emission plays an important role in limiting the overall efficiency of a device, and by using PBG techniques to reduce it, increases in efficiency of LEDs[7], and lasers[8][9] has been possible. An obvious use of a photonic crystal is that of a wavelength specific optical filter. Since the PBG will not support photon modes within the stop-band, a PBG structure could be incorporated into a waveguide to create a band reject filter.

An important concept easily transfered from atomic lattices and the electronic waves they support to periodic dielectric structures and their photon modes is the concept of a defect. As in electron systems, a defect in a photonic lattice is a slight disruption in the periodicity of the material. This defect can be the removal of a unit cell structure, or it can be a local shift in the lattice spacing. Both of these defects will have an effect on the band structure and hence transmission spectra. If properly designed, a local shift in the lattice spacing, like a $\lambda/4$ phase slip, can open up a very narrow transmission window inside the stop-band. This could be used in the manufacture of a specialized notch filter, made especially useful through the design of structures with the same stop band with slightly different defect peak spectral positions. At the defect wavelength, a photon state within the PBG structure closely localized about the defect. The concept of localization has led to the design of structures that guide light on the nanometer scale with closely spaced defects[10].

II. Devices and Growth

The devices studied were grown by molecular beam epitaxy (MBE), consisting of a 0.4 μm $Al_xGa_{1-x}As$ waveguide core ($x = 0.12$) cladded by an $Al_xGa_{1-x}As$ ($x = 0.35$) layer beneath and the air above. The one-dimensional waveguides and air gaps for the PBG structure were patterned using electron-beam lithography, and transferred into silica by dry etching with CHF_3. The silica pattern provided the template for reactive ion etching of the semiconductor waveguide with $SiCl_4$[11]. A scanning electron micrograph of a device with 10 air gaps and 460nm periodicity is shown in figure 1. A range of devices with between 3 and 10 air gaps, periodicities between 400nm and 480nm, and different defects were fabricated from the same wafer.

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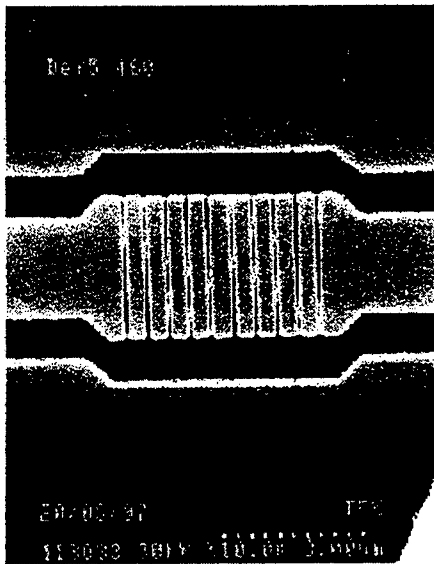


Fig. 1. Scanning electron micrograph of a device with 10 air gaps, 460 nm periodicity. Though indistinct in the micrograph, the spacing between the two central air gaps is 60 nm wider than the periodic spacing of 460 nm between all other air gaps.

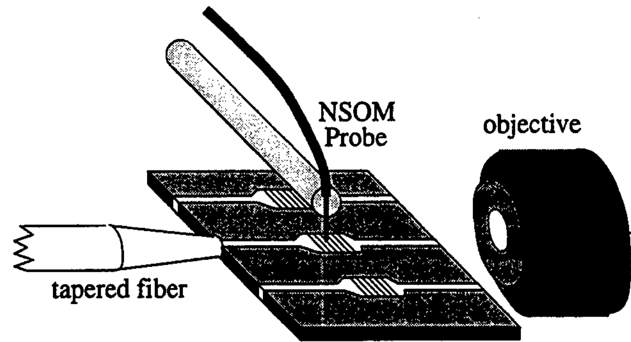


Fig. 2. A schematic diagram of the experimental setup used to measure the waveguides. Shown are the tapered fiber used to launch into the device, the NSOM probe used to collect the near-surface light, and the objective used to image the exit facet of the waveguide (not to scale). Not shown is the nanopositioning equipment used in scanning the tip over the sample.

III. Experiment

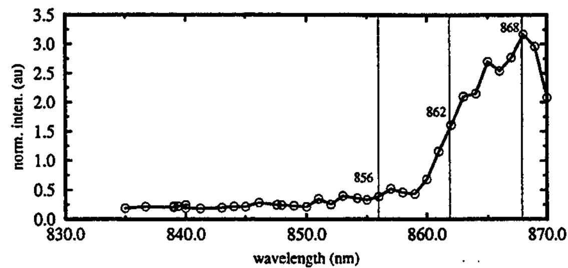
A schematic diagram of the experimental setup is shown in figure 2. The devices were measured using a tunable Ti:Sapphire laser launched into a single mode fiber whose end had been tapered slightly to a diameter of $\sim 30.0\mu m$ using a CO_2 laser and micropipette puller. Optical fields present at the surface of the device were detected using Near-field Scanning Optical Microscopy (NSOM)[12]. The NSOM probe consisted of a single mode fiber tapered to a diameter of $\sim 0.1\mu m$ and shadow coated with Al[13]. During scanning, the NSOM probe was held at a constant height of 10nm above the waveguide surface using the tuning fork shear-force feedback method[14]. Light collected by the NSOM probe was detected by an avalanche photodiode in single photon counting mode. An objective lens imaged the waveguide exit facet, and coupled with a pin-hole aperture was used to measure the transmitted light. In the input path, a 2x2 fiber coupler was used to simultaneously monitor the power incident on the sample.

IV. Band Edge Imaging

The stop-band transmission widths of the samples are broader than the tuning range of the Ti:Sapphire laser, so complete transmission curves for a single device could not be obtained. The 400nm periodicity sample was initially chosen since its low-energy band-edge is within our laser window, and we could study the changes in spatial modes between incident wavelengths within and outside of the stop-band. The sample consisted of 4 air gaps on each side of a central defect with a 400nm periodicity to the air gaps.

The transmission as a function of wavelength is displayed in the top of figure 3, showing the long wavelength band-edge and the three wavelengths for the near-field images below. The topographic shear-force image, taken simultaneously with the 856nm data set, is used to correlate the spatial modes to the PBG structure. While the air gaps are not visible in this reproduction, they are resolved in the shear-force data.

The incident beam enters the waveguide from the left in each image. The three near-field images are taken within the stop-band at 856nm, on the band-edge at 862nm, and within the transmission region at 868nm. The overall impression is of interference patterns typical of periodic structures. On closer inspection, the brightest regions are at the transition between the one-dimensional waveguide mode and the photonic crystal mode. This is likely due to the impedance mismatch at such an interface, where power is not only reflected back along the waveguide, but intensity is also scattered into both evanescent and propagating modes which are collected by the near-field probe. Also significant in this data set is the clear increase in penetration of the spatial mode along the length of the photonic crystal region for increasing wavelengths. Note the large increase in intensity on the right-hand side of the 868nm image compared to the 862nm image. As the band-edge is approached, the device becomes more transparent, and the one-dimensional waveguide modes couple more efficiently into the PBG modes and through the device.



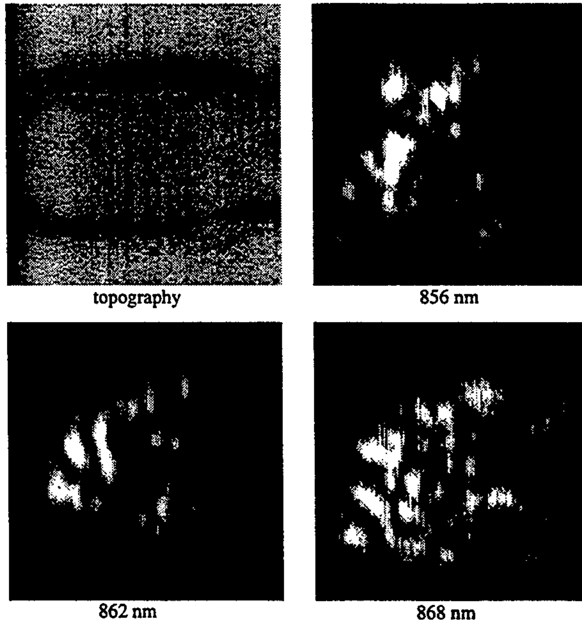


Fig. 3. Imaging of the band-edge modes. The top graph shows the transmission through the sample, clearly showing the position of the band-edge. The first image is that of the topography of the sample, obtained using the shear-force technique. The other three images are the spatial modes obtained using the NSOM probe and the avalanche photodiode, excited at the wavelengths as indicated on the transmission graph. Note the greater penetration into the device for longer wavelengths.

V. Defect Imaging

Of major interest in telecommunications and in the utilization of PBG devices for all optical switching and wavelength demultiplexing is the performance and characterization of defects deliberately introduced into PBG waveguide structures. Our intent with these devices is to simultaneously map the defect localized evanescent optical fields, and measure any changes in transmission through the structure caused by the presence of the additional dielectric of the NSOM probe. The results presented here are preliminary in nature.

Transfer matrix method (TMM) simulations of these devices indicated that there should not be a defect state in the stop-band of samples with the 400nm periodicity, while a defect should exist in the 440nm periodicity sample. Due to oxidation of the air gaps, however, it is difficult to precisely predict the wavelength of the defect state. Transmission spectroscopy scans found a possible candidate at 874nm in the 440nm period sample. Note that defect states, even in PBG structures with relatively few periods like these can be quite narrow. The TMM simulations estimated the defect width at $\sim$ 0.5nm. A transmission graph and a spatial mode image is shown in figure 4. We see a large localization of light in the area of the defect; quite different from the images taken at wavelengths about the band-edge in figure 3. The optical intensity detected in figure 4 appears to have a significant scattered component to it, indicating a propagating as well as evanescent mode. For a pure PBG crystal and defect, only an evanescent localized mode is expected[15]. We are in the process of additional measurements as well as improving our experimental setup to separate the scattered components from the localized ones.

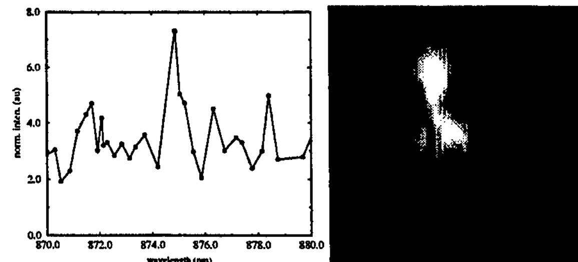


Fig. 4. Imaging of defect modes in the 440nm periodicity sample. The left graph shows a weak peak in the transmission spectra, about 0.5nm wide. The right image is a near-field scan taken at that peak in the transmission. The near-field scan for this launch wavelength is dramatically different than the scans taken about the band-edge in the 400nm sample. The lower of the two bright spots is within the local region of the defect. The upper spot is probably due to some slight roughness in the channel defining the waveguide, causing a great deal of scattered light to couple out of the structure.

VI. Conclusions

Using near-field scanning optical microscopy the spatial optical mode structure of a one-dimensional photonic band gap device operating in the near infrared has been measured for the first time. Clear indication of coupling to the transmitting modes of the PBG is evidenced by the greater penetration as the wavelength is tuned through the band-edge. Additional preliminary results are suggestive of a spatial map of a defect state. These measurements open up the possibility of directly determining the performance and efficiency of real PBG devices.

Acknowledgments

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THz Lasing due to Intracenter Optical Transitions in Ge

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Stimulated emission of far-infrared radiation has been observed in p-Ge at strong electric and magnetic fields [1] and shown to be due to population inversion of the valence subbands. We observed a stimulated emission in p-Ge without any magnetic field but under uniaxial stress [2]. In this report we present experimental evidence for population inversion of strain-split acceptor levels in uniaxially compressed p-Ge in strong electric fields. The stimulated far-IR emission arisen under resonance conditions is shown to be due to the intracenter population inversion.

Uniaxial deformation removes the degeneracy of the valence band of Ge at $k=0$ and splits it into two subbands separated by the energy gap proportional to the applied pressure P (the proportionality factor is about 4 and 6 meV/kbar for $\boldsymbol{P}$ parallel to [100] and [111] crystallographic directions, respectively [3]). The degenerate ground state of an acceptor is also split into two states. The energy separation $\delta\varepsilon$ between the split-off state and the ground state increases with strain. Fig.1 represents schematically the p-Ge valence band structure and the positions of the split-off and ground states for different pressures. At certain pressures ($P\approx4$ kbar for $\boldsymbol{P}\|[111]$ and $P\approx3$ kbar for $\boldsymbol{P}\|[100]$) the split-off state enters into the valence band continuum (band scheme for 4 kbar in Fig.1) and creates the resonance state while the ground state remains in the forbidden band. The series of exited states related both to ground and split-off states should exist also in the gap and the continuum, respectively. It will be shown that the stimulated emission of far-infrared radiation in heating electric fields is a result of an inverted population of the resonance states.

The gallium-doped Ge crystals with Ga concentration of $3*10^{13}$ to 10^{14} cm^{-3} were used in the experiment at liquid helium temperature. The samples of a square cross section of 0.5 to 1 mm^2 and 6 to 10 mm long were cut in the [111] or [100] crystallographic directions. Uniaxial pressure P and electric field E were applied along the samples. Voltage pulses of 0.2 to 1 μs duration were applied to two contacts positioned on the long (lateral) plane of the sample. The distance between the contacts was from 4 to 9 mm.

Far-infrared luminescence was registered by the cooled gallium-doped Ge photodetector. For the samples with planes parallel within 4`, the steep rise in radiation intensity up to 10^3 times was observed at some threshold stress P_c. The minimum P_c value was 4 kbar. The jump in radiation was accompanied by the jump-like rise in current (up to 10 times).

The existence of the threshold value of pressure for the appearance of intense emission points that it is stimulated. The resonator formed in our case by well-parallel

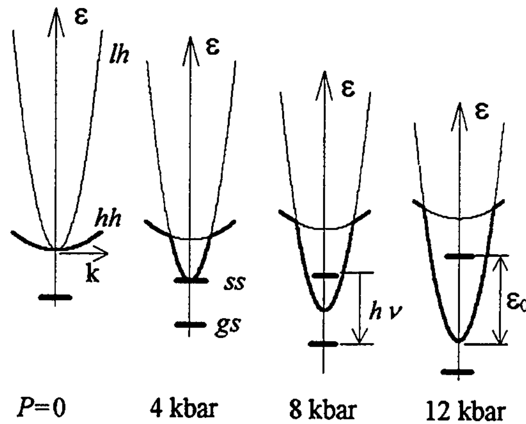

Fig.1. The valence band structure and the acceptor level positions for various values of P. Heavy-hole and light-hole bands are denoted by *hh* and *lh*, and ground and split-off acceptor states are denoted by *gs* and *ss*, respectively. ε_0 is the optical phonon energy. For convenience the hole subbands are shown here as for electrons.

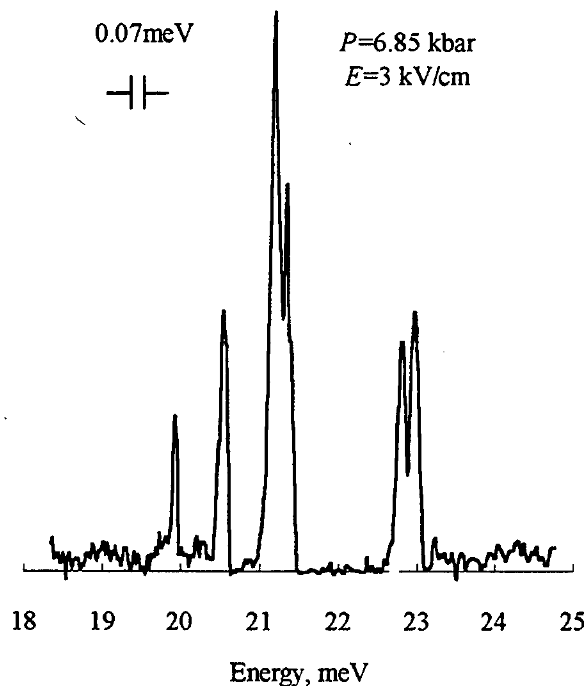

Fig.5. The spectrum of stimulated emission. $E||P||[111]$ The peak at 21.2 meV corresponds to the optical transitions between the resonance 1s and $2p_{\pm 1}$ acceptor states.

sample planes was necessary to obtain the stimulated emission. Indeed, the jump in emission (and in the current) disappeared after rough grinding of one of the long sample planes. Polishing and etching restored the resonator and the stimulated emission appeared again.

The spectrum of stimulated radiation from compressed p-Ge measured by the grating monochromator is shown in Fig.2. It consists of several peaks. The peak energies increased with pressure. The energy of the most intensive peak (21.2 meV in Fig.2) is varied from 21.2 to 42 meV by increasing pressure from 6.85 to 11 kbar at $P||[111]$ (see Fig.4).

The main peak measured in more details shows the structure caused by resonator modes (Fig.3). The line spacing (≈0.11 meV) for the specimen with the cross section of 1*1 mm^2 coincides with that found from the condition $N\lambda=nL$, where λ is the radiation wavelength, n is the refractive index (n=4 for Ge), L is the optical path length, and N is an integer. This shows that in our case, as in [4], the optical resonator is formed due to total internal reflection

from lateral crystal planes (see the insert in Fig.3).

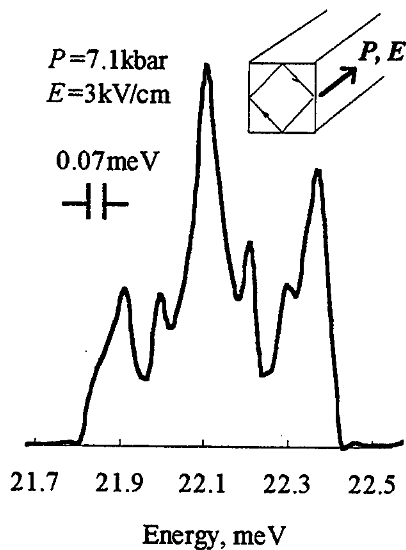

Fig.7. The mode structure of the main peak in the spectrum of stimulated emission. The sample cross section is of $1*1mm^2$.

The calculations of the spectrum of localized and resonance acceptor levels were performed by the variational method for high pressure limit (impurity states are considered in approximation of independent valence subbands). The calculated energies of optical transitions from the resonance 1s state to the localized 1s- and $2p_{\pm1}$ states and the experimental stress dependence of the energy of the main peak are shown in Fig.4. The comparison allows us to identify the main peak as the resonance -1s to $2p_{\pm1}$ transition and the peak at 19.2, 20.5, and 23 meV as the transitions from resonance 1s to $2p_0$, 2s, and ground -1s states, respectively. The linewidth for different peaks is of 0.2 to 0.5 meV. The reason for the wide spectral maxima may be the broadening of the resonance acceptor state being in the continuum [5].

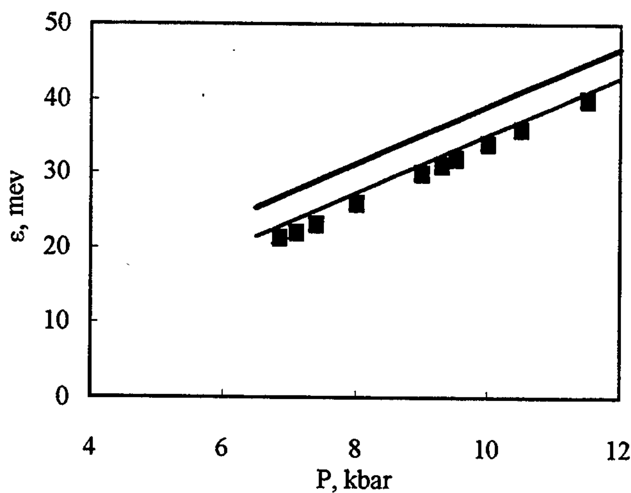

Fig.4. The energy of the main peak of stimulated radiation vs stress. Solid lines show the calculated energy of optical transitions from resonance -1s state to $2p_{\pm1}$ (lower line) and 1s localized states.

An inverted population of the split acceptor states should exist for stimulated intracenter optical transitions to take place. Indeed, in strong electric field the acceptor ground state located in the forbidden band becomes empty due to impact ionization while the split-off state is in the valence band continuum and should be filled to some degree. The inverted population of resonance states is proposed to be due to strong resonance scattering of free holes into these states. The necessary conditions for such inversion are derived. The minimum pressure for the stimulated emission to be observed is just that at which the resonance state appears (see band scheme in Fig.1). The energy splitting of the acceptor states is about 10 meV in this case (Fig.4). On the other hand, the stimulated radiation intensity decreases sharply [6] as the split-off acceptor state begins to depopulate via hole transitions to the valence band edge assisted by optical-phonon

emission (see the band scheme for 12 kbar in Fig.1). The value of $\delta\varepsilon$ for depopulating the split-off acceptor state is about 42 meV.

Thus, these data confirm that the intracenter inversion can arise as the split-off state enters into the valence band and exist until optical phonon-assisted hole transitions to the valence band edge depopulate the resonance state. The energy range of the stimulated emission is expected to be from 10 to 41 meV.

In summary, the data obtained show that the stimulated far-infrared emission in uniaxially compressed p-Ge is due to the electric field induced population inversion of strain-split acceptor states. The necessary condition for the inversion is the resonance state appearance. The possibility of a strong frequency tuning by stress is shown. The spectral lines connected with the exiting states referred to the ground acceptor state were observed in the spectrum of the stimulated emission. It should be noted that the mechanism of far-infrared stimulated emission in p-Ge based on the population inversion of strain-split acceptor states seems to be promising also for acceptor doped two-dimensional structures. In such structures the acceptor states are split by strain and/or space quantization without any external pressure.

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Single and Multi-Channel 1.55 μm Monolithically Integrated Photoreceivers

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1.0 Abstract

InP-based monolithically integrated p-i-n/HBT single- and multi- channel photoreceivers have been fabricated and characterized. The single channel photoreceivers demonstrated a 3 dB bandwidth of 17 GHz with an optimized peaking inductance of 1.4 nH, whereas the 16-channel arrays have a measured average bandwidth of 11.6 GHz. The adjacent channel crosstalk was improved from -25 dB to -35 dB with the implementation of a metal shield covering on top of the dual-biased photoreceiver arrays.

2.0 Introduction

There has been an explosion in the transmission and processing of information in recent years. Indeed, fiber communications coupled with microelectronics is believed to be a major driving factor in the advent of the optoelectronic information age. This idea is based on the fact that in certain applications, such as transmission of information, optics is superior to electronics, while in other applications, such as processing of information, electronics is superior. In the design of an optical-fiber communication system, whether for use in long distance communication or for bussing data over short distances, operating at low or high data rates, a key element is the receiver. The basic purpose of the receiver is to detect the incident light and convert it into an electrical signal containing the information impressed on the light at the transmitting end.

Opto-Electronic Integrated Circuit (OEIC) photoreceivers based on p-i-n photodetectors and Heterostructure Bipolar Transistors (HBTs) have demonstrated performance similar to or better than hybrid circuits in terms of sensitivity and bandwidth[1]. The use of a p-i-n diode and HBT as the active devices in the photoreceiver allows a simple scheme of monolithic integration with one-step epitaxy wherein the photodiode is realized using the base, collector and subcollector layers of the HBT structure. The important performance characteristics of a photoreceiver are the operating bandwidth and sensitivity. Sensitivity plays an important role in deciding the number of repeaters needed in a long-haul communication system. The receiver sensitivity is defined as the minimum amount of optical power level needed at the receiver input so that the signal-to noise ratio is greater than a given value. In digital communications systems, this translates to having a bit error rate less than a given value. To improve the sensitivity, noise and crosstalk should be minimized while designing a high performance photoreceiver array.

In this paper, we present the details of design, fabrication and characterization of high-speed InAlAs/InGaAs p-i-n/HBT photoreceivers and 16-channel low crosstalk photoreceiver arrays.

3.0 Design of Integrated Photoreceivers

The design sequence used for the design of the integrated photoreceiver has been described in an earlier publication[2]. The process starts with the fabrication of test HBT's to be integrated in the photoreceiver. Once these devices are characterized, small and large signal models, which are to be used

in dc and microwave circuit simulations, are developed.

The circuit topology is then defined and optimized for the desired characteristics. The optimized design should be consistent with the bias conditions chosen for each active device. Next, the layout of the passive components and interconnections are characterized and a simulation of the complete circuit, including parasitics, is performed. Once the simulated performance is satisfactory, the final mask set is designed and the circuit is fabricated.

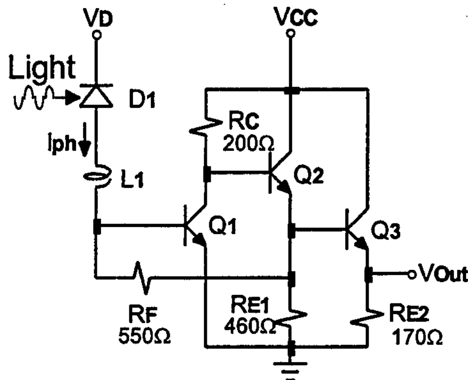
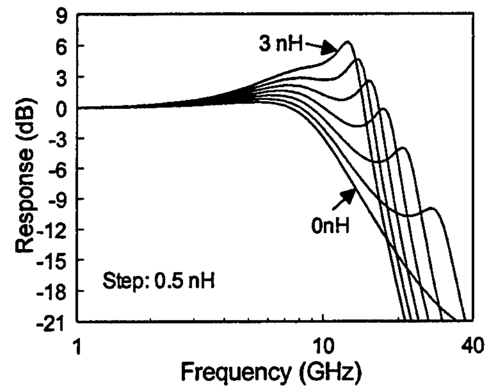


Figure 1. Circuit diagram of a 3-stage tranimpedance photoreceiver.

Figure 1 shows the circuit diagram of the photoreceiver. It consists of a 156 μm^2 p-i-n photodiode and a three stage transimpedance amplifier based on 5×5 μm^2 emitter area of HBTs with a feedback resistor 550 Ω and an output buffer stage which provides 50 Ω matching output impedance. The circuit could be either single- or dual-biased. It has been shown that with dual bias design, the crosstalk performance improves[3].

The inclusion of the base peaking inductance has shown to improve the signal-to noise ratio and enhance the overall bandwidth. The peaking effect uses an inductor, and sometimes a capacitor, to increase the bandwidth of the photoreceiver[4]. The inductor is connected in series with the photodiode at the input of the amplifier. For a multi-Gb/s photoreceiver, the value of the inductor is typically on the order of a few nH and depends on the circuit parameters and in particular on the value of the feedback resistance. The effect of the peaking inductor is to enhance the photoreceiver bandwidth with little degradation in the sensitivity. In other words, the peaking effect enhances the gain of the photoreceiver at high frequencies while introducing no additional noise. Therefore, the contribution from the different noise sources to the equivalent input noise current at high frequencies is reduced, since the enhanced gain is used to refer the output noise voltage to the input of the circuit.

For a simple bipolar transistor amplifier, there are three types of inductive peaking that can be used: base, collector and feedback. We will examine only the base peaking, in order to get a good understanding of the peaking effect, because the collector and feedback peaking are not as effective as the base peaking effect. The models used in the simulation have been shown elsewhere[3] and we assume ideal peaking inductors in the circuit, that is, no associated parasitic capacitance nor series resistance.



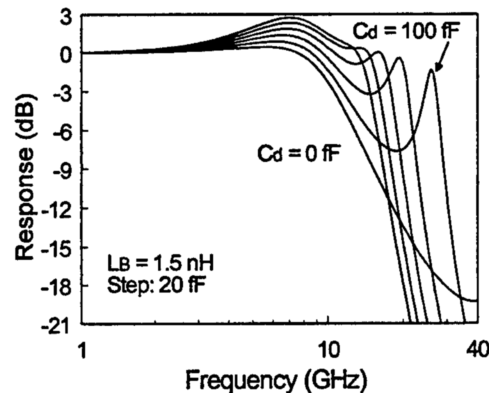


Figure 2. Simulated response of photoreceivers with different (a)peaking inductance and (b)photodiode junction capacitance.

Base inductor peaking effect originated from placing an inductor between the photodiode and the base. The simulated frequency response of the photoreceiver with base inductor peaking is shown in Fig. 2(a). It clearly shows that the 3 dB bandwidth of the amplifier increases with increasing inductance up to a certain point; increasing the inductance beyond that point results in a bandwidth decrease. The response also shows that the inductive peaking

causes a noticed loss of gain flatness at higher frequencies. For most applications, a small amount of gain peaking is tolerable up to 6 dB. It is clear that at high values of inductance, gain peaking becomes nonnegligible. For an inductance of 1.5 nH, Fig. 2(a) also predicts that only 1.7 dB gain peaking would occur. From the processing point of view, the inductance variation is tolerable up to 3 nH. Also, it is found that the peak frequency and the gain is sensitive to the photodiode junction capacitance. The frequency response of the photoreceiver with base peaking inductor 1.5 nH and different photodiode junction capacitors is shown in Fig. 2(b). The peak moves toward high frequencies as junction capacitance increases and the maximum 3 dB bandwidth is around 20 GHz for a photodiode with a junction capacitance of 70 fF.

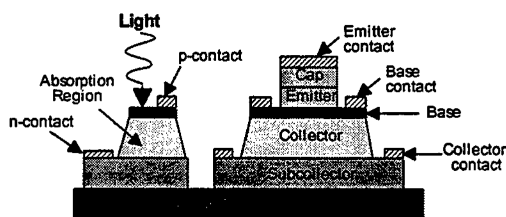


Figure 3. PIN-HBT integration scheme.

This observation suggest that the bandwidth can be optimized through tuning the area of the photodiode on condition that the response of the detector is limited by the transit time.

4.0 Experimental

The epitaxial heterostructure was grown by solid-source molecular beam epitaxy (MBE) on a Fe-doped semi-insulting InP (001) substrate and consists of a standard lattice matched $In_{0.52}Al_{0.48}As$ / $In_{0.53}Ga_{0.47}As$ HBT. It has a 4000Å Si-doped n^+ (1×10^{19} cm^{-3}) InGaAs subcollector, a 6500Å n^- (6.7×10^{15} cm^{-3}) InGaAs collector, which is also used as the absorption region of the p-i-n diode, a 750Å Be-doped p^+ (3×10^{19} cm^{-3}) InGaAs base, a 150Å p-type (2×10^{18} cm^{-3}) InGaAs to alleviate the doping compensation between base and emitter, a 1500Å n-type (8×10^{17} cm^{-3}) InAlAs emitter, a 700Å n^+ (1×10^{19} cm^{-3}) InAlAs layer for buffering the contact layer, and a 1000Å n^+ (1×10^{19} cm^{-3}) InGaAs contact layer. Base and collector thickness are optimized to achieve the high speed and sensitivity. Fig. 3 shows the PIN-HBT integration scheme in the photoreceiver. The circuit includes a 156 μm^2 p-i-n photodetector and a three-stage transimpedance amplifier based on 5 μm × 5 μm emitter area HBTs and a 550 Ω feedback resistor. The p-i-n photodiode, made with the base-collector layers of the HBT, demonstrated a measured optical bandwidth larger than 20 GHz and a responsivity of ~ 0.32 A/W at λ = 1.55 μm. Maximum cutoff frequencies of the fabricated 5 × 5 μm^2 emitter HBT's were f_T = 50 GHz and f_{max} = 80 GHz. The thin film resistors with 25 Ω/□ sheet resistance consist of 10 μm wide and 700Å thick evaporated 40% Cr-Ni alloy. The spiral peaking inductor was realized using Ti/Al/Ti/Au interconnection metallization. The fabrication of the integrated p-i-n/HBT with self-aligned emitter-base and SiO_x side-wall process is described in detail elsewhere[3].

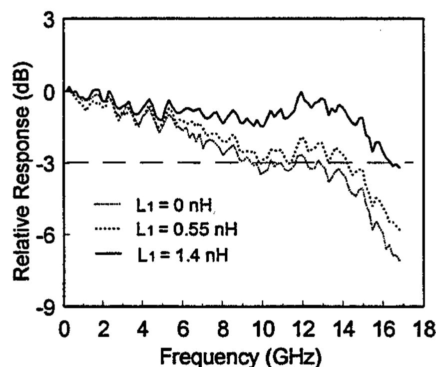


Figure 4. Measured optical response of 3-stage photoreceivers with different peaking inductance.

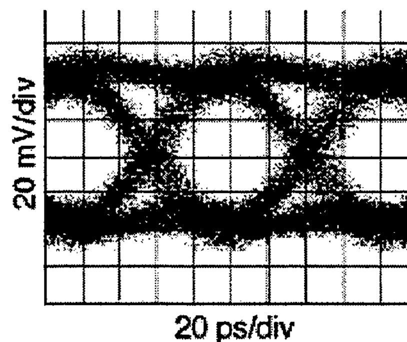


Figure 5. Measured eye diagram of a 3-stage photoreceiver with peaking inductance 1.4 nH at 12 Gb/s.

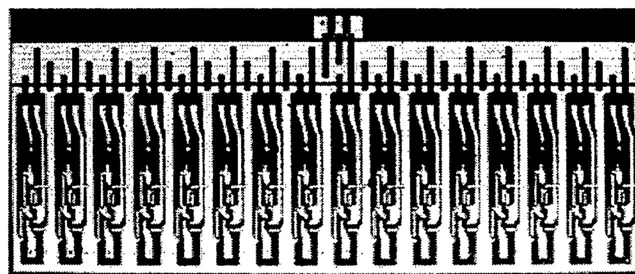
4.1 Single-Channel Photoreceivers

Fig. 4 shows the optical response of the 3-stage photoreceivers biased at 3 V with base peaking inductors. It is found that the peaking inductance improves the bandwidth without trading off the gain, which is in agreement with the simulation. The discrepancy between the simulated and experimental data results from ignoring the parasitics. It can be seen that a peak still exists even without base peaking inductor. The bandwidth is optimized to 17 GHz when the peaking inductance increases up to

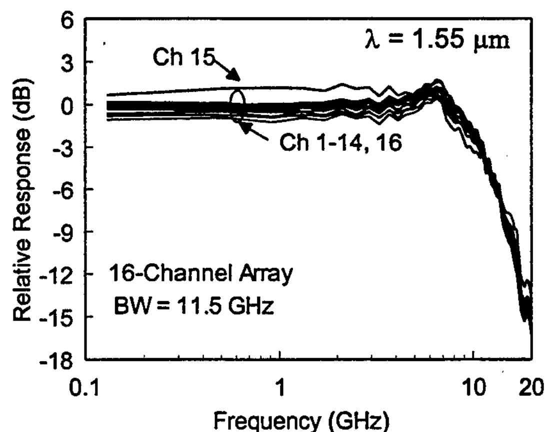
1.4 nH. Fig. 6 depicts such a photoreceiver response to 2^{31} - 1 NRZ pseudo-random binary sequences at a speed of 12 Gb/s. The eye diagram is clearly open with virtually no overshoot or undershoot. The sensitivity is estimated to be -19 dBm at the bit rate of 10Gb/s for a bit error rate of 10^{-9}. The photoreceivers demonstrate a transimpedance of 46 dBΩ.

4.2 Multi-Channel Photoreceiver Arrays

Figs. 7 shows the microphotograph and measured optical response of the fabricated 16-channel arrays with a pitch of 250 µm. The three-stage transimpedance amplifier used in each channel of the arrays demonstrated a typical gain of 48 dBΩ with an electrical bandwidth of 11.5 GHz. The bandwidth is uniform within 1.5 dB throughout all the channels. The adjacent channel crosstalk is measured to be less than -24 dB with dual bias. It should be noted that with a dual-biased scheme the crosstalk is significantly reduced, which is a result of the disappearance of feedback route. With a metal shield on top of the circuit, the crosstalk can even be suppressed down to -35 dB.



(a)



(b)

Figure 7. (a)Microphotograph and (b)measured optical frequency response of a fabricated dual-biased 250 µm pitch 16-channel photoreceiver array.

The shielding is fabricated using a two layer photoresist process either by thick metal lift-off or electroplating. The shield, shown in Fig. 8, has openings for bias, RF output, and photodiode optical coupling. Good uniformity between individual photoreceiver elements has been achieved and the yield of the discrete devices was about 96 percent, which resulted in 50 percent yield for the fabricated 16-channel arrays.

5.0 Summary

High performance 1.55 µm InP-based monolithically integrated single and 16-channel photoreceiver arrays are demonstrated. The single channel photoreceiver shows a 3 dB bandwidth 17 GHz with 1.4 nH base peaking inductance. The 16-channel photoreceiver arrays show uniform channel bandwidths as high as 11.5 GHz and adjacent channel crosstalk less than -24 dB. It is found that the adjacent channel crosstalk can be reduced to less than -35 dB by using a dual power supply and a metal radiation shield.

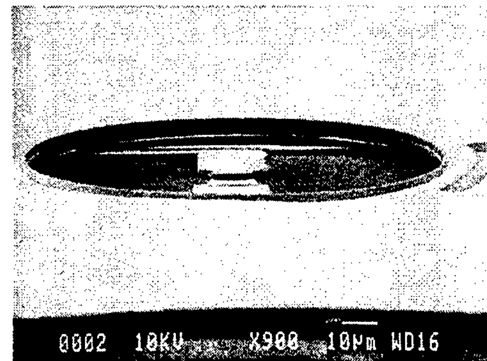


Figure 8. SEM picture of a fabricated radiation shield. The photodiode lies in the center of the hole.

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Patterned Semiconductor on Glass Photocathodes for High Throughput Maskless Electron Beam Lithography

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1.0 Introduction

In recent years, intense research has been devoted to increasing the throughput of electron beam lithography to levels that are competitive for wafer production at linewidths of 0.1 μm and below. Historically, these efforts have been limited by blurring due to Coulomb interactions at high currents. Several prototype systems, such as cell projection or SCALPEL, rely upon the generation of an extended, high-current (several microamps) exposing beam for image projection [1,2]. More recently, a system has been proposed in which multiplexed primary sources illuminate the wafer through the use of a simple, two lens, demagnifying raster projection system (Figure 1). This system has the advantage of being maskless; in addition, greater flexibility and process latitude are possible with a multiple beam, raster scan writing strategy. The enabling technology for this system is a negative electron affinity (NEA) photocathode technology currently under development at Stanford and Intevac ATD, which has been described elsewhere (Figure 2). [3,4] Baum *et al.* [5] have demonstrated excellent source properties experimentally in a new UHV electron gun system, with beam brightnesses of 2.2×10^7 A/(cm^2 sr); other workers [6] have reported picosecond-scale switching times for these cathodes.

2.0 Simulation Results

New modeling work has shown that for a 50 kV system, as much as 10 μA of current may be delivered to the wafer to achieve a throughput of 20 wafers/hour with 0.1 μm resolution (Figure 3). Achieving a small spot size at the emission surface of an NEA photocathode is crucial for several reasons. First, a small spot size may be used to maximize quantum efficiency and source brightness by minimizing the number of electrons trapped in surface states [7]. Second, and most relevant for electron beam lithography, a reduction of the emission source size allows for a reduction in the system demagnification necessary for 0.1 μm feature sizes. Less demagnification allows 100% of the current generated by the source to reach the wafer when 0.1 μm diameter emission areas are used, in sharp contrast to current electron beam instrumentation, which typically uses less than 1% of the emitted current. Since all current generated by the source contributes to space charge blurring of the beams, it is important to maximize the fraction of current delivered to the wafer by restricting the emission area.

3.0 Experimental Results

3.1 Cathode Evaluation and Description

The emission area may be reduced most easily by using a patterned cathode that can be fabricated by defining an array of small (0.1 μm) dots in a metal (TiW) layer. This layer may be placed, in general, anywhere within the GaAs active region of the photocathode (Figure 4). The photocathode is illuminated from the backside with a 638 nm diode laser focused to a diffraction limited spot that with a diameter of 0.5 μm.

Backside patterned cathodes, where the metal layer is directly above the glass substrate and serves as an optical proximity mask, have been recently fabricated and tested in the electron gun facility at Stanford. When the patterned cathode is flood illuminated from the backside using a expanded 633 nm laser spot, approximately one hundred parallel electron beams can be excited from a 150 μm diameter area on the cathode surface. Brightness measurements have been performed on this cathode, and are consistent with the previous results for unpatterned cathodes (8.0×10^6

A/(cm^2 sr) - 3.0x10^7 A/(cm^2 sr)). The minimum emission area observed from this cathode is 0.96 μm in diameter, generated from a 0.5 μm diameter patterned hole in the metal masking layer. The increase in spot size is consistent with carrier diffusion through the ~0.25 μm thick cathode tested. Carriers in a 0.5 μm diameter circle that are generated just on the active region side of the metal mask diffuse toward the surface where they are emitted. As they diffuse, the electron also move laterally, contributing to an increased spot size. There are, however, practical limits on the minimum size of spot that can be achieved using this backside masking technique. When the size of the apertures used is below one half the wavelength used, the incident beam power is greatly attenuated, as the size of the hole in the conducting plane is below the diffraction cutoff. This is similar to the problem encountered in near field scanning optical microscopy (NSOM), where a surface is imaged optically below the diffraction limit using a small pinhole with a large signal gain. The diffusion of carriers in the GaAs active region further exacerbates the problem of achieving a smaller spot size. For these reasons, the minimum spot size achievable with this method is on the order of 0.5 μm in diameter.

In order to further reduce the spot size, a buried patterned metal layer may be placed just below the emission surface, within the GaAs active region. Carriers are then excited to the conduction band in the GaAs active region, and begin to move due to diffusion. A fraction of these carriers will be passed by the small holes in the metal masking layer; they then diffuse to the surface, where they may be emitted. The rest of the carriers are intercepted by the metal layer, where they encounter an extremely high recombination velocity. In this way, the metal masking layer serves to produce smaller areas, even when the patterned features are exposed to a large-area optical excitation. Since the GaAs layer between the patterned layer and the emitting surface may be made very thin, diffusion does not contribute significantly to an increase in spot size. However, the structure requires that the GaAs be regrown into very small (0.1 μm) holes with very good interface quality. Cathodes of this type are currently being fabricated, and will be evaluated in the near future.

3.2 Device Fabrication

Patterned cathodes can also be fabricated by partially growing a standard photocathode structure on a GaAs substrate using MOCVD. Once the GaAs active region layer is grown, a RF-sputtered blanket TiW is deposited. This layer is patterned by first exposing a positive tone resist (ZEP 520-12) using electron beam lithography, and subsequently etching these features using an ECR plasma etcher. If a buried layer structure is desired, an additional GaAs regrowth step must be performed (Figure 5). After the MOCVD growth and patterning steps are completed, the entire structure is bonded to an 18 mm diameter glass substrate, which provides mechanical stability for the device. Finally, the substrate is then etched away to produce a finished device that may be activated to NEA, and later inserted into an electron beam system using the activation technique described elsewhere [5].

4.0 Summary

Electron beam lithography is a mature, very high resolution lithography technology that requires a drastic throughput increase in order to be competitive for sub - 0.1 micron wafer manufacturing. Using patterned negative electron affinity photocathodes with small emission areas, Monte Carlo simulations indicate that a system could be devised to deliver the required amount of current with acceptable beam blurring. A number of patterned cathode devices have been devised to achieve this goal. A backside patterned cathode has been tested, and approximately 100 parallel beams have been generated with 1.0 micron diameter emission areas. More advanced devices that will allow for further reduced emission areas are currently being fabricated.

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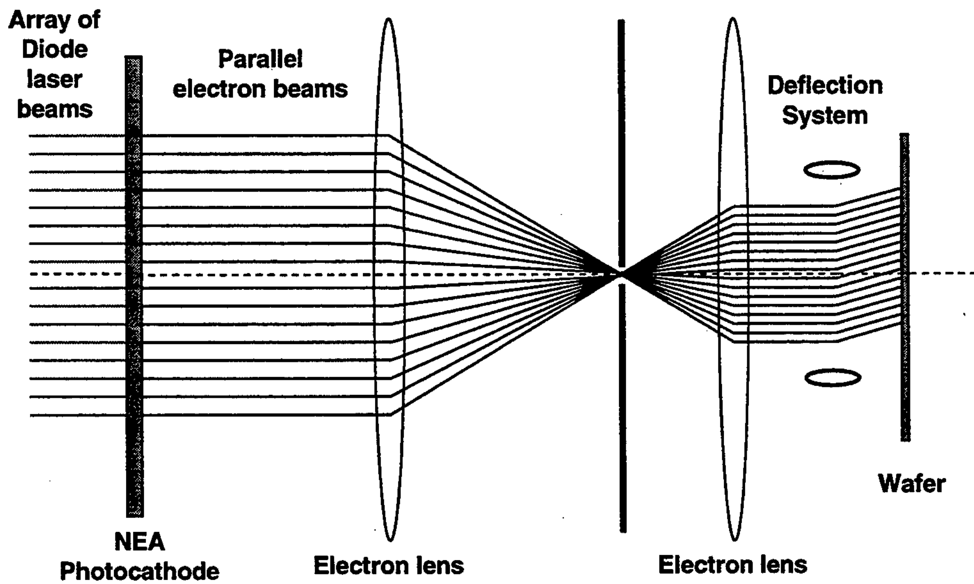


Figure 1. Proposed 50 kV parallel electron beam lithography system configuration based on a negative electron affinity (NEA) photocathode.

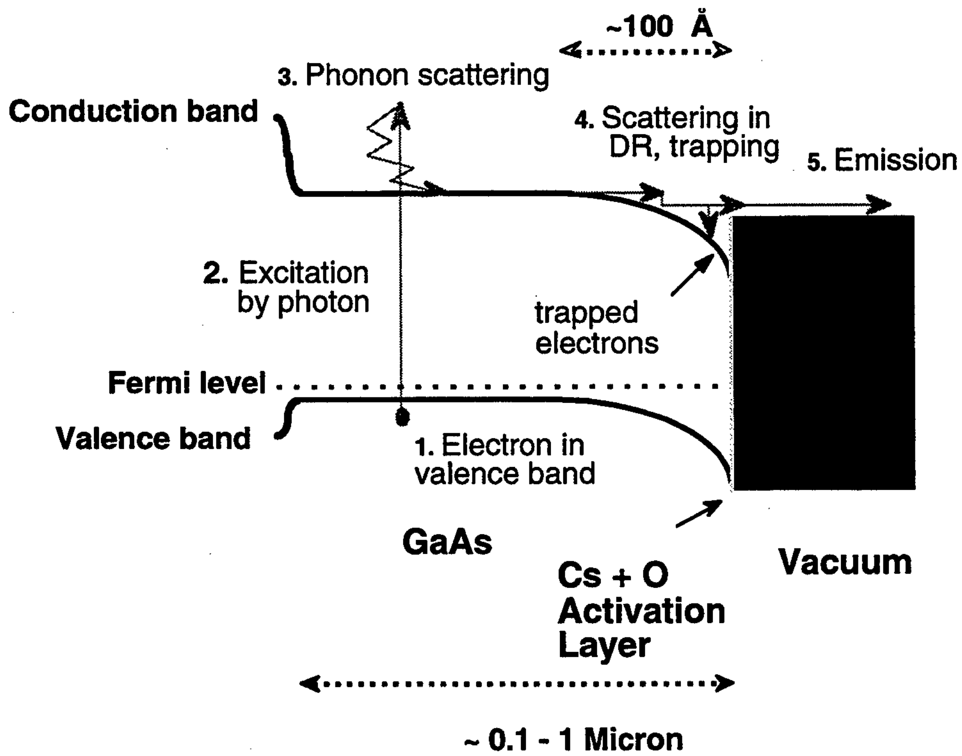
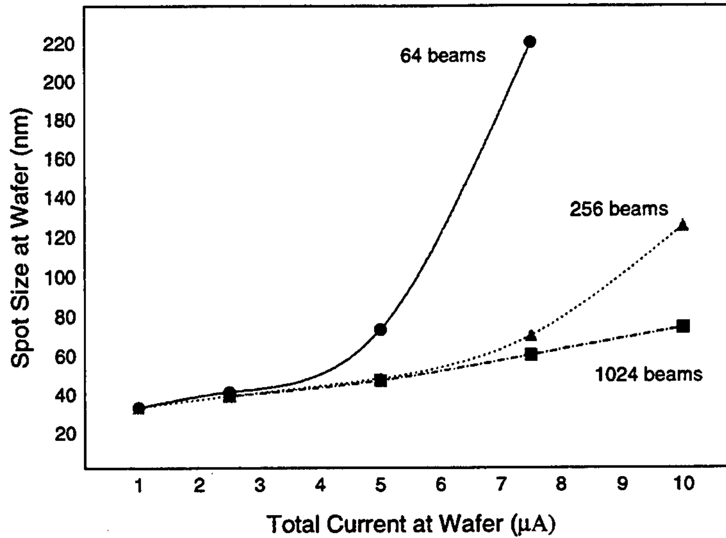


Figure 2. Band diagram of an NEA photocathode (unpatterned), illustrating the photoemission process.



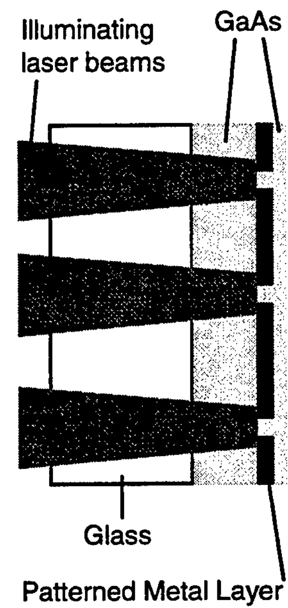


Figure 3: Results of Monte Carlo Coulomb interaction simulation. By increasing the number of beams in the system and spreading the current in the electron beam column over a wider field with 1024 beams at 10 nA per beam, the spot size at the wafer scales linearly with the current at the wafer.

Figure 4. Schematic of patterned photocathode structure.

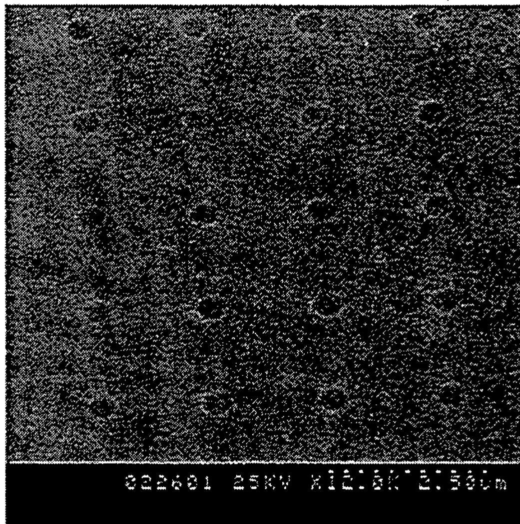


Figure 5. An array of 0.25 μm holes in the patterned TiW layer of an NEA photocathode. Holes as small as 80 nm have been resolved using this process.

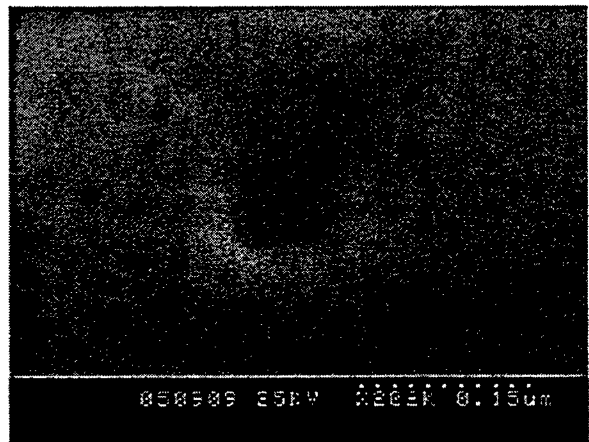


Figure 6. Cross-sectional SEM of regrown GaAs in a 0.1 μm patterned photocathode.

Non-linear plasma waves in the Field Effect Transistor structures

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Plasma excitations have been of considerable interest in recent studies of semiconductor quantum wells and quasi-two-dimensional (2D) conduction channels in FETs. The intrasubband plasmons that are associated with a single electron subband can be studied as collective excitations in a two-dimensional electron fluid. When the electron-electron collision time is much smaller then the collision times with impurities and phonons the hydrodynamic model should be applicable to the carriers in MOSFET and HEMT channels. The phenomena similar to wave and soliton propagation and hydraulic jump[1] was predicted for the electron fluid. Recently, Shur and Dyakonov[2] analyzed new effects related to plasma oscillations and proposed novel electronic devices based on their analysis: a terahertz HEMT oscillator, frequency mixer, and a detector operating in terahertz range. Shur and co-workers recently fabricated prototype detectors and observed the off-resonance detection of microwave radiation by the electron fluid[3]. They determined that hydrodynamic non-linearity is essential in the modeling of these devices.

In this work we consider the non-linear effects in hydrodynamic model with two different boundary conditions. The first one corresponds to a device with Schottky contacts and the second describes a device with Ohmic contacts with a zero DC bias. In addition to the effects of non-linearity in the hydrodynamic equations we also analyzed the effects of non-linear dispersion of the plasma waves. The principal partial differential equations are the equation of continuity and the Euler equation projected into 2D plane. The relation between electron charge in the 2D channel and the electric potential is determined by the three dimensional Poisson equation. We consider a 2D electron gas in the x-y plane and two gate electrodes at the distances d_1 and d_2 above and below the 2D gas. The gate electrodes are assumed to be at the same potential. The case of $d_2 \rightarrow \infty$ corresponds to FET structure while $d_2 \sim d_1$ corresponds to the three terminal Junction FET (JFET) structure. The electrostatic constants are ϵ_1 and ϵ_2 above and below the channel correspondingly. In the later case the gate to channel voltage is assumed to be less then the one required for the pinch-off[4]. We consider a one dimensional density fluctuation along the channel (x axis). Let n_0 be an equilibrium 2D density of electrons in the channel, determined by the gate voltages. We write the time and space dependent 2D density as $n(x,t) = n_0 + \delta n(x,t)$. The basic equations are

$$\frac{\partial n}{\partial t} + \frac{\partial (nv)}{\partial x} = 0 \qquad (1)$$

$$\frac{\partial v}{\partial t} + v\frac{\partial v}{\partial x} = -\frac{e}{m}\frac{\partial \phi}{\partial x} \tag{2}$$

$$\nabla^2 \phi = (4\pi e/\epsilon)\delta n(x)\delta(z) \tag{3}$$

where in eq. (3) the Laplacian is three dimensional, $\delta(z)$ is the Dirac delta function, ϵ is ϵ_1 for $z > 0$ and ϵ_2 for $z < 0$. For an infinitely long channel we can write the projection of eq. (3) in the x-y plane in an integral form:

$$\phi(x,z{=}0) = \int dx' K(x')\delta n(x-x') \tag{4}$$

The kernel K can be determined by the infinite system of gate images of the 2D charge distribution. Expanding $\delta n(x-x')$ in powers of x' we obtain a graduate channel approximation[1] from a zero order term. The next nonvanishing term comes from the second order in the expansion. We will keep only these two terms. The expansion only works if both d_1 and d_2 are finite as compared to the wave-lengths of the density fluctuations. The linear plasmon velocity is given by $s_0^2 = e^2 n_0/mC$ where $4\pi C = (\epsilon_1/d_1) + (\epsilon_2/d_2)$. We introduce dimensionless variables: x/L where L is the length of the channel, t/T where $T = L/s_0$, n/n_0, v/s_0. Equation 1 preserves its form and equation 2 takes the following form:

$$\frac{\partial v}{\partial t} + v\frac{\partial v}{\partial x} + \frac{\partial n}{\partial x} + \beta\frac{\partial^3 n}{\partial x^3} = 0$$

$$\text{where} \quad \beta = \frac{d_1 d_2}{3L^2}\frac{d_1\epsilon_1 + d_2\epsilon_2}{d_1\epsilon_2 + d_2\epsilon_1} \tag{5}$$

We consider two sets of boundary conditions:
(1) $v=0$ and $\beta\partial n/\partial x = 0$ at $x=0,1$; (2) $\delta n=0$ and $\beta\partial n/\partial x = 0$ at $x=0,1$.
The results for (1) are presented in Fig.1. At large times with $\beta=0$ the wave has a step-like shape (a shock wave), while with small non-zero β the result is anharmonic oscillations. The results for (2) are presented in Fig.2. In case (2) a small non-zero value of β turns a two-step shock wave into a smooth shape at very large times, Fig.3.
Acknowledgment: G.S. was supported by the U.S. Army European Research Office (London), contract No. N68171-97-M-5548.

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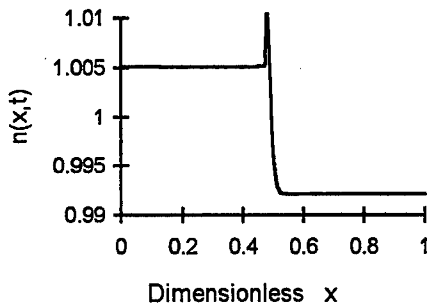

Fig.1a. Dimensionless time t $\approx$ 100,
dispersion coefficient β =0,
Initial amplitude A = 0.5.
Boundary conditions (1).

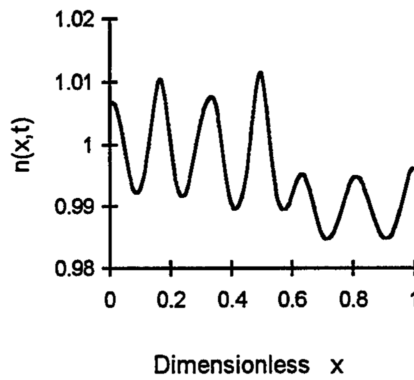

Fig.1b. Dimensionless time t $\approx$ 100,
dispersion coefficient $\beta/2 = 10^{-6}$,
Initial amplitude A = 0.5.
Boundary conditions (1).

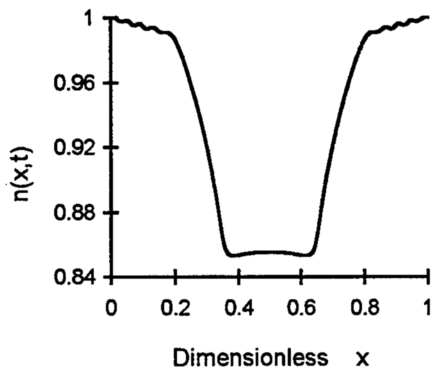

Fig.2a. Dimensionless time t $\approx$ 100,
dispersion coefficient β =0,
Initial amplitude A = 0.5.
Boundary conditions (2).

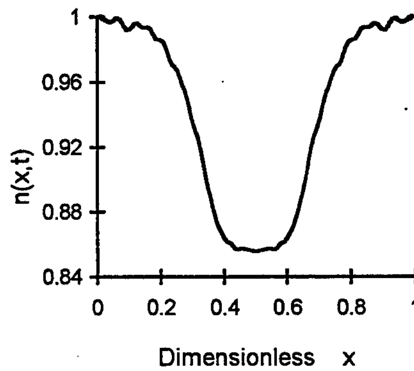

Fig.2b. Dimensionless time t $\approx$ 100,
dispersion coefficient $\beta/4 = 10^{-6}$,
Initial amplitude A = 0.5.
Boundary conditions (2).

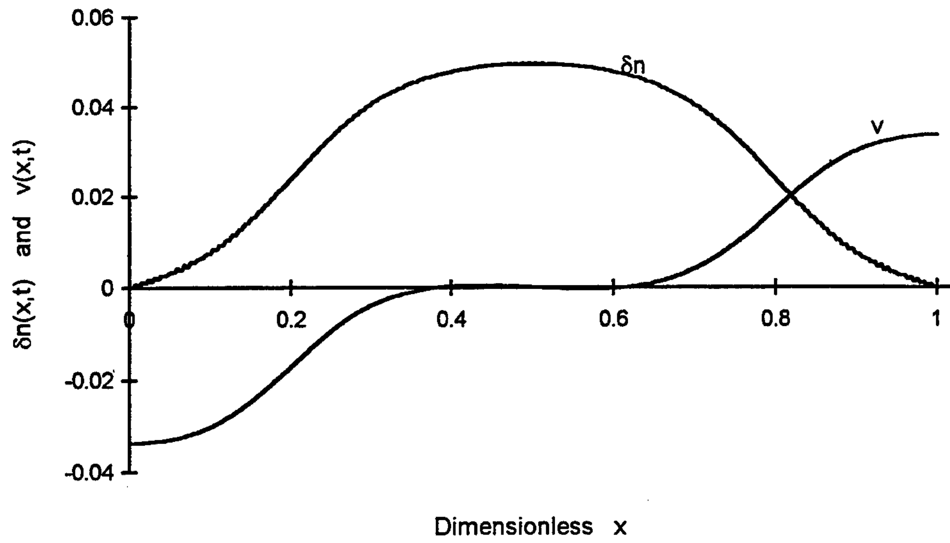

Fig.3. Dimensionless time $t \approx 1000$, Dispersion coefficient $\beta/4 = 10^{-6}$,
Initial amplitude $A = 0.5$. $\delta n = n - n_o$, v is the fluid velocity.
Boundary conditions (2).

Generation of Terahertz Oscillations in p – type Semiconductors

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In the series of papers [1-6], we have studied space charge limited ballistic transport of current carriers having a complicated dispersion relation with a domain where they have negative effective mass (NEM–domain) in a certain region of the wave vectors. Figure 1 shows an example of the dispersion relation $\varepsilon(k)$ with the NEM–domain which corresponds to the ground subband of hole size quantization in p–quantum well (p–QW). Velocity, $v(k)$, and the inverse effective mass, $m^{-1}(k)$, as a function of in–plane wave vector, k, are also shown in this figure. Peculiarities of ballistic transport arise when the ballistic carriers reach the energy of NEM–domain. A drifting ballistic plasma with carriers having NEM is convectively unstable [1]. In the diode loaded with a relatively small resistance, this drifting instability leads to current oscillations [2]. Figure 2 shows a relation between the current oscillations and the spectrum of carriers. The voltage at which the oscillations start, corresponds to the mean energy of the carriers with NEM. Current oscillations are accompanied by the plasma waves. The oscillation frequency is determined by the transit time of carriers having NEM, and this frequency is in the terahertz range for submicron ballistic structures. Numerical simulations indicate that in most cases spectrum of these oscillations is characterized by a main frequency which depends on the applied voltage. The variation of the frequency gives an opportunity of electrical tuning of the generation frequency in a wide range (up to 1.5 times). For long diode bases or for high voltages, when the base region with the carriers having NEM (NEM–region) becomes sufficiently long, the oscillation spectra are complicated due to excitation of the modes with higher frequencies.

Special consideration is needed when the layered bases are used. Because of the weak screening by two–dimensional carriers, details of a ballistic diode design strongly affect the current in the diode [7,8]. Therefore, to optimize the diode, it is necessary to determine an appropriate shape of the anode and cathode, as well as the Fermi–energy of the injected carriers. Numerical analysis shows that knife–shaped electrodes are more preferable because high electric field arises near the electrode edge, which results in shorter electrode–adjacent space charge regions and longer NEM–region [7]. The injection properties of the electrodes should provide a regime of space charge limited currents in the diode despite the weak screening and, as a result, high currents. This circumstance is a basis for choosing the Fermi–energy [7, 8]. If the Fermi–energy is small, the base is depleted at actual voltages, while the large Fermi–energy leads to widening of the space charge region and shortening of the NEM–region.

Since our first suggestion of a new mechanism of terahertz generation, based on ballistic transport of carriers with NEM [3], several different mechanisms of realization of the required dispersion relations with the NEM–domain are discussed and studied

from this point of view [4,5]. The first mechanism, described in detail in [4], is a hybridization of two electron dispersions with very different effective masses in an asymmetrical double quantum well (ADQW) or in a composite ΓX quantum well (ΓXQW). Using a model dispersion relation we show that the frequency of the current oscillations exceeds 1 THz if the length of the diode base is less than 0.5 μm, base doping is near $5 \cdot 10^{17}$ cm^{-3}, and the mean energy of the NEM–domain is greater than 0.1 eV. To form the dispersion relation with the NEM–part in an ADQW or ΓXQW, we need a heterosystem with sufficiently different electron effective masses. Actually, the mass ratio should be greater than 2. Taking into account effects of nonparabolicity, the ratio should be even greater than 2 with some excess.

The large mass ratio of the heavy and light holes makes the hole subsystem especially attractive to form a dispersion relation with the NEM–domain. As far as we know, there are two different mechanisms leading to the NEM–domain formation. They are the mixing of the light and heavy hole states along the direction of uniaxial compression in diamond-like or zinc-blende-like p-type semiconductors [5], and mutual size quantization of the light and heavy holes in a heterostructure p–QW (see [7,8,9]).

The hole dispersion relation for a uniaxially compressed semiconductor is strongly anisotropic with the longitudinal NEM in a narrow angle of wave vector directions near the compression direction. The effect of in–plane tension is similar to the uniaxial compression, therefore the pseudomorphic growth can also be implemented to form the required dispersion relation. This means that the transport along the direction of uniaxial compression, i. e. across the deformed layer, must be used. In this case, we deal with a transverse transport across the doped barrier, while the heavily doped well materials are used as contacts. The position of the NEM-domain (i.e. the mean energy of the NEM carriers) is controlled by the deformation value, and varies in a wide range. A variation of the NEM–domain position results in a variation of the voltage range of the oscillation regime in the ballistic diode, and the frequency of the oscillations.

The ballistic regime of carrier transport in the base of the diode occurs either in long weakly doped bases under the low biases (less than optical phonon energy) when the ballistic length is determined by the impurity scattering and may exceed a micron, or in short heavily doped bases under the high biases when the ballistic length is determined by the optical phonon scattering and is of the order of 0.1 μm for $p-Ge$ or 0.06 μm for $p-InAs$ [6]. Naturally, the former case occurs only at low temperatures while the latter takes place at room temperatures.

Here, we should emphasize that the easiest way to obtain the reported oscillations in the compressed semiconductors is to investigate a ballistic structure with long ($0.5 \div 1$ μm) weakly doped ($[0.5 \div 5] \cdot 10^{16}$ cm^{-3}) $p-Ge$ base with deformation near 0.5 %. The expected oscillation frequency is near 0.5 THz.

Special notes are required for the room temperature operation regime for the considered mechanism. As we found, to provide the oscillation regime in the diode with a short ballistic base (0.1 μm and less) the energy of the NEM carriers should be greater than 0.15 eV. It corresponds to the uniaxial compression of approximately 3 %. To produce such deformation pseudomorphic growth must be used, substituting

uniaxial compression by in–plane tension. We believe that the most promising heterosystems are $InGaAs$ (ballistic base)/$InAs$ (contacts), $InP/InAs$, $GaAs/InGaAs$ or $GaInP/InP$. The base length in this case must be less than 0.05 μm which might be fabricated under such tensions. Naturally, the expected oscillation frequencies are much higher and may exceed 10 THz.

Mutual size quantization of the light and heavy holes in a heterostructure p–QW leads to the formation of the NEM–domain in the ground subband of quantized hole spectra (Fig. 1). The NEM–domain arises due to the valence band discontinuities at the heterointerface, and its position depends on the well width. In this case the longitudinal transport through the p–QW must be used.

Traditional $p - GaAs$ QWs (of 10 nm width) provide the mean energy of the NEM–holes of the order of 20 meV, and these QWs may be used for low temperature implementations. For the base lengths of $0.1 \div 1.0$ μm and the doping of $(0.2 \div 1.0) \cdot 10^{11}$ cm^{-2} the oscillation frequencies are in the range of $0.25 \div 2.0$ THz. Numerical simulations show that amplitudes of the oscillations are sufficiently larger than in the case of deformation, and reach the value of 60 %. This is due to a larger size of the NEM–domain for the quantized holes. We should mention here that the currently measured hole mobilities in $p - GaAs$ QWs are $(0.25 \div 1.0) \cdot 10^6$ cm^{-2} V^{-1} s^{-1}, which correspond to ballistic lengths $L = 1.4 \div 5.6$ μm at 4.2 K. Therefore, ballistic transport condition is met in such structures.

The efficiency and output power of the generator depend on a load resistance. The maximum output is obtained when the inner resistance is equal to the outer resistance. For the model sample with the base length of 0.2 μm, the doping of 10^{16} cm^{-3}, the maximum power is about 2 W cm^{-2} and the efficiency is near 1 % when the load resistance is equal to $5 \cdot 10^6$ Ohm cm^{-2}. Despite a relatively small output power per one QW (10 nm width), we can significantly increase the output using multiwell structures.

For the room temperature implementations, we should increase the mean energy of the NEM–carriers up to 0.15 eV. The required heterosystem should provide a sufficiently deep hole well (0.6 eV and greater) with the width of $25 \div 35$ Å. Taking into account required band offsets, we should decline $GaAs/AlAs$ heterosystem, and pay attention to heteropairs with a common cation. In this case, the valence band discontinuities are greater than the discontinuities in the conduction bands, for example, $InAs$ (well)/InP (barrier). In contrast to the case of compressed semiconductor when the transport across the InP–barrier is considered, here we deal with the longitudinal transport in the $InAs$–well. Very promising heterosystems for this implementation are also type – II heterostructure $GaSb/InAs$ with the discontinuities in the valence bands $\Delta E_v = 0.51$ eV [10]. Even greater the valence band offsets are reported for matched $InAs_{0.95}Sb_{0.05}/GaSb$: $\Delta E_v = 0.67$ eV [11].

One of the main advantages of the QW structures is a possibility to use modulation doping to reduce ionized impurity scattering. This is especially important for the structures intended for room temperature operation when the doping concentration becomes high and the impurity scattering may significantly restrict the ballistic length.

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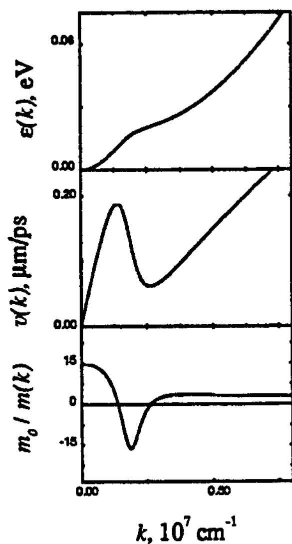

Fig. 1. $\varepsilon(k)$, $v(k)$, $m_0/m(k)$ for ground subband of hole size quantization in *p-Ge* QW of width 11 nm.

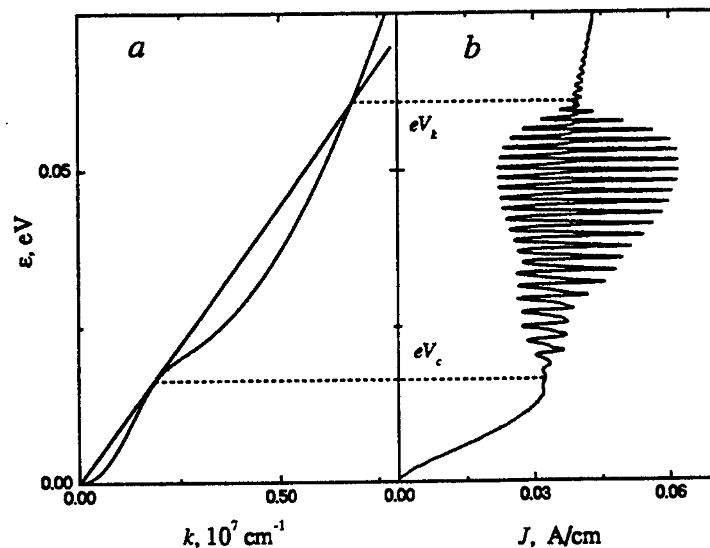

Fig. 2. Dispersion relation, $\varepsilon(k)$, and corresponding current oscillations as a function of applied voltage $eV_D = \varepsilon$ for *p-GaAs* QW of length 0.5 µm, width 11 nm, and the doping $2 \cdot 10^{10}$ cm^{-2}.

Extending the Force and Displacement of the Integrated Force Array

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1. INTRODUCTION

Integrated Force Arrays (IFAs) are MEMS actuators which powered by the electrostatic forces between the plates of many microscopic deformable capacitors arranged in monolithic arrays. IFAs are fabricated using standard techniques of VLSI electronics [1,2]. Following a short overview of the properties and operation of the IFA, and the method of fabrication, this paper will discuss measurements of IFA performance and methods to increase its force and displacement.

IFAs produce motion on a practical scale by adding the responses of many microscopic elements, and can be thought of as artificial muscle. The force of the IFA is from the electrostatic attraction due to the two oppositely charged plates contained in each cell. When voltage is applied, the IFA membrane contracts by more than 20% in one dimension, producing large macroscopic motions with high efficiency [2]. Integrated force array devices offer advantages such as greatly reduced power consumption, the absence of sliding friction, operation under a wide range of external conditions, precise positioning capability, and over two orders of magnitude reduction in weight when used as direct substitutes for existing mechanisms such as solenoids [2]. The IFA structure can be configured in ways more complex than simple one-dimensional motion, with applications ranging from integrated optical and flow control systems to biomedical actuators and prosthetics.

The IFAs fabricated and tested in this work were 3 mm wide and 10 mm long with approximately 200,000 cells. A wider array will produce correspondingly larger forces, and a longer array will produce correspondingly larger displacements. Figure 1 shows a small generic array as well as a detailed sketch of an individual cell. In the figure, the shaded metal bands along the sides of the deformable polyimide beams are charged with a voltage, V, to produce an attractive electrostatic force which results in the compression shown. At the ends of the single cell shown in the insert of Figure 1 are short polyimide beams that are half the height of the longer beams. These beams transmit the force generated by the electrostatic attraction through the array of cells. The beams are lower to allow the metal on the sides of the full height beams to be electrically continuous down the length of the taller beam.

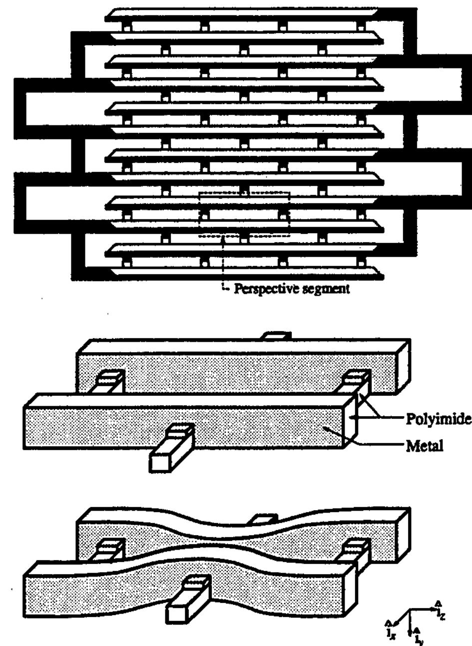

Figure 1. An IFA in a relaxed position, top, a relaxed and compressed unit cell, bottom.

2. IFA OPERATION

The electrostatic force in the cells is to first order proportional to the area of the plates divided by the square of the separation. Thus the force is independent of the scale of the cell dimensions. This independence of scale is an important reason for making the cells small. In any given array area, a greater number of cells

can be incorporated with a greater net force and range of compression

Due to the electrostatic operation of the IFA, electrical power is primarily consumed only when they are moving. When a voltage is applied, the cells begin to compress, and the force between them increases, causing further compression until the plates are fully closed. The initial range of applied voltages is insufficient to significantly bend the beams. A middle range of voltages provide a range of cell compressions that are stable (a decrease in the cell compression while maintaining the applied voltage results in a net force acting to compress the cell). Beyond a certain voltage, there is no stable equilibrium position and the cell closes. Because the goal of the IFA is to compress while acting on a load, the complete closure of the cell, which maintains the available force from the cell, does not degrade the overall capability of the IFA. It does put a limit on the range of compressions where there are stable equilibrium positions, which can be designed around by the overall dimensions of the IFA.

3. IFA FABRICATION

The most recent fabrication run used the fabrication method known as the embedded hard mask process [3]. The fabrication of the IFAs is shown in Figure 2. In this method a thermal oxide is grown on a 100 mm silicon wafer. Above the oxide, a layer of polyimide is applied and cured which will provide the half height connectors of the IFA. A thin layer of silicon is evaporated and patterned photolithographically with an I-line stepper, defining the locations of the half height connectors. A second layer of polyimide is then applied and cured with the total thickness of the two polyimide layers approximately 2.2 μm thick. Next is the deposition of a thin layer of plasma-enhanced chemical vapor deposition (PECVD) oxide. The PECVD oxide is patterned defining the full height regions of the IFA. An oxygen RIE of the polyimide is done next, with the etch stopping or being masked by the various inorganic layers. The small lateral etch component of the polyimide RIE produces a slight overhang of the PECVD oxide and a final thickness of the polyimide beams of approximately 0.3 to 0.35 μm. Chromium and gold are evaporated directionally (at 28°) to produce a thin film on the sidewalls. The overhang of the oxide cap separates the metal on the sidewall of the polyimide from the metal on the oxide cap. Finally the wafer is immersed in aqueous hydrofluoric acid (HF) that dissolves the PECVD oxide first, allowing the metal caps to be removed, followed by the dissolution of the thermal oxide and the array floats free of the substrate.

The embedded hard mask method has the advantage of well defined etch stops and planar surfaces during lithography but the alignment of the full height level to the half height level can be difficult due to the intermediate layer of polyimide between the hard mask layers. For this fabrication run, the mask design was altered to increase the allowable amount of lithographic misalignment.

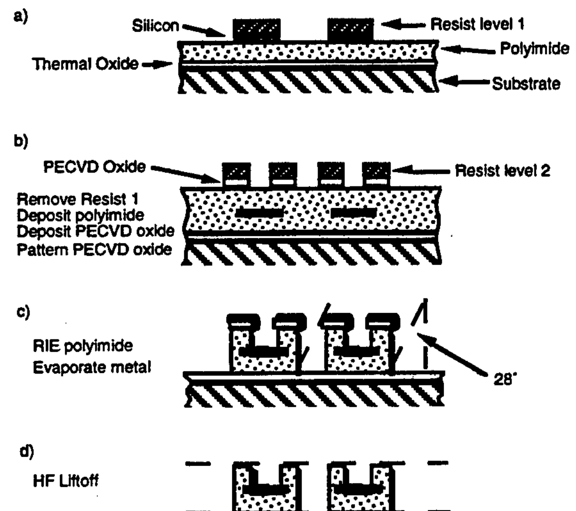

Figure 2. Process sequence with half height hard mask embedded in the polyimide film.

4. EXPERIMENTAL RESULTS

There is a complex relationship between the applied voltage, resulting displacement, and available force for the IFA due to the approximate inverse square law of the electrostatic force with plate separation [4]. As the plates approach each other, the electrostatic force increases as well as the amount of force required to deflect the beams. Because they increase at different rates, initially the available force decreases and then increases as the plates come closer. A miniature swing was machined to allow the

measurement of the exerted forces with the IFA contracting at the same time. One end of the IFA is attached to a fixed pedestal and the other end to the swing. As the IFA contracts, the swing is pulled toward the pedestal, which raises the center of gravity of the swing and the force exerted by the IFA can be calculated [3].

The mask set consisted of 4 IFA test structures and a yield test structure. The IFA test structures were approximately 3 mm wide and 10 mm long. The pitch of the IFA full height features was 1.7 μm and the length of the cells was either 20, 25, or 30 μm. The primary variation in these test structures was the length of the unit cells, the application of different techniques to minimize the weak cell effect, such as mechanical diodes and reduced number of rows of unit cells in each subarray, and the improved alignment structure of the half height connectors [5].

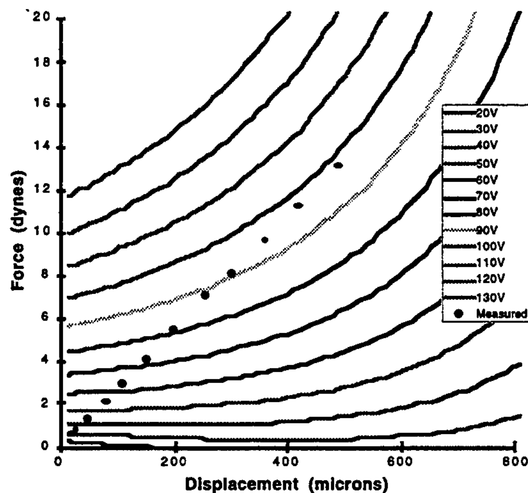

Figure 3. Calculated and measured force and displacement data. All data begins at 20V.

Displacements of 700 μm in an IFA with an 8 mm long active region were observed. Forces in excess of 12 dynes were measured which corresponds to a force/cross sectional area of over 3000 dynes/mm^2 and a work/volume ratio in excess of 15 ergs/mm^3. These values exceed those corresponding to other reported linear actuators [6,7]. Figure 3 shows the measured force and displacement data along with the calculated curves, with good agreement between the calculated and measured data up to 90V (7 dyne data point). Operation of over 20,000 cell closures per second were observed. Several samples were tested for the lifetime of the IFA. Typically the tests were stopped with the IFA still functioning, with several were still operating after 7X10^8 cycles. Repeated measurements of the force of the IFA indicate that the total variation at a given applied voltage was less than 4% of the average value at that voltage.

5. EXTENDING THE PERFORMANCE OF THE IFA

In its present form, the IFA is useful for certain very low mass actuator applications. Other applications require larger forces and displacements than are available from the current form of the IFA. Some of the recent work at MCNC has investigated creating stronger IFAs with larger displacements.

Stronger IFAs require increasing the cross-sectional area of the structure. Stacking the IFA is one method for achieving this, however, the handling of the IFA needs to be made more robust since the 2 μm thick IFA is fragile and difficult to handle. We have investigated adding monolithically a 25 μm thick polyimide frame around the IFA, with plated metal feedthroughs for electrical and mechanical connections. In addition, the frame will provide an automatic spacing between adjacent IFAs. A variety of polyimide frame test structures were fabricated with different frame and metal feedthrough dimensions. The polyimide frame was fabricated by wet etching a 25 μm deep trench into the silicon substrate, and then re-oxidizing the wafer. A chrome/gold plating base was evaporated on the wafers, and an 8 μm thick photoresist film deposited and exposed to open the locations of the metal feedthroughs. Approximately 27 μm of gold was then plated on the wafer. Since the plating thickness was greater than the photoresist thickness, the plated metal mushroomed over the photoresist opening, locking the feedthroughs into the 40 μm of polyimide subsequently deposited for the frame. At this point the wafers were ready for planarization and removal of the excess polyimide with CMP until the plated gold was exposed. The first attempt at planarization only removed approximately 10-15 μm of polyimide from the high areas of the wafer instead of the desired 37-38 μm. A second attempt of planarizing the wafers should

remove the correct amount of polyimide, and the last few microns of polyimide will be removed with an oxygen RIE. At this point the fabrication process for the IFA would begin with the thick polyimide frame completed and recessed into the substrate. Figure 4 shows a photograph of a released polyimide frame from the first fabrication effort. As expected, the released polyimide frames are very robust and easy to handle without any fear of damage.

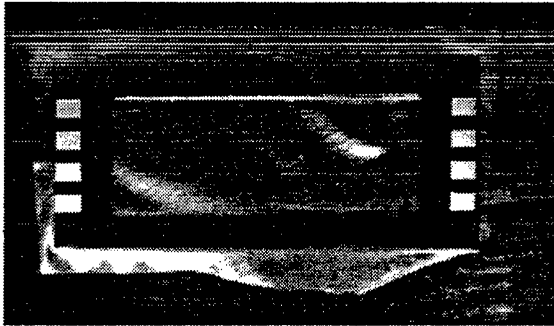

Figure 4. Photograph of a released polyimide framed membrane with gold feedthroughs.

The size of earlier IFAs was limited by the field size of the step and repeat photolithographic stepper. This mask design included an IFA test structure, that with the overlap of the exposure field edges during the stepping process, a longer IFA could be made without any major change in the fabrication technology. Because the alignment between adjacent fields is relatively poor (on the order of several microns) and because there is some overexposure of the edge features, the size of the overlapped edge features cannot be made as small as the features in the middle of the field. Since the electrical pads and interconnections at the ends of the IFAs are relatively large, overlapping these features is possible. By setting up the stepping program to make several passes on each wafer, a variety of different length IFAs were fabricated and released from the wafers. Figure 5 is a photograph of a four field IFA, 51 mm in length. To test the functionality of the overlapped pads, probes were placed in the long connecting pads between the IFAs, and the IFAs above and below the pads were examined for motion. The contracting motion was seen in both IFAs, indicating that the electrical connections were continuous from one IFA to the next. The success of the fabrication of longer IFAs indicates that the technique could also be applied to fabricate wider IFAs, or even a single IFA that uses most of the wafer surface area.

Figure 5. A photograph of a released four field IFA on foil.

6. CONCLUSIONS

Integrated force arrays are a new type of actuator that uses VLSI technology to fabricate large arrays of small force cells capable of large displacements and large forces. Forces have been measured in excess of 12 dynes and displacements of over 700 μm were also noted. The measured force/cross-sectional area of the IFA is 3000 dynes/mm^2, and the work done by the IFA divided by its volume is in excess of 15 ergs/mm^3. High speed operations are possible with an observed rate over 20,000 contractions/second, as well as lifetimes of greater than 10^8 contractions. Methods have been developed that can lead to stronger IFAs with greater displacements.

7. ACKNOWLEDGMENTS

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Coupling Effects of Tensile Strained GaAs/InAlAs Double Quantum Wells (DQWs)

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In recent years, optical properties of semiconductor microstructure based on double quantum wells(DQWs), especially asymmetrical ones (ADQWs), have attracted increasing attention because of the possibility of using such structure for new quantum electronic devices. Previous work has discussed the large refractive index change and the change in optical absorption under the electric field in the coupled GaAs ADQW structure, namely, quantum-confined Stark effect(QCSE)[1] and electron-hole overlap variations in symmetric coupled wells[2]. However, all quantum well structures based on conventional lattice-matched material systems exhibit polarization dependence of quantum-confined Stark effect(QCSE), which originates mainly from the splitting of heavy hole(hh) and light hole(lh) energy levels. One effective method of achieving total polarization independence characteristics is to bring the light hole (lh) energy level to the top of the valence band with tensile strain so that the electron-light hole transition (involved in both TE and TM modes) peak is the leading one.[3] The resultant polarization insensitivity of the tensile-strained double quantum well is the motivating feature for the development of polarization-independent detectors and modulators.

In this study, tensile strained GaAs/InAlAs DQWs and ADQWs on GaAs substrates prepared by molecular beam epitaxy (MBE) are investigated (Fig. 1). Coupling effects and electric-field-induced effects on energy levels in DQW structures with various barrier widths are analyzed within the framework of the Bastard envelope function approximation [4]. In this approximation, analysis is performed by assuming $K_x = K_y = 0$, which allows one to treat electrons, light holes and heavy holes separately. The rapid variations due to the periodicity of the hosts are ignored but are taken into account by using effective masses and band offsets. The simulation algorithm is based on Transfer Matrix Method (TAM)[5]. The Schrödinger equation is discretized by assuming a piece-wise constant potential profile and effective mass. Thereafter, the Schrödinger equation is solved in each piece of a given potential profile. One of simulation results is shown in Fig. 2. In this figure , solid lines represent the wave functions of electrons in each of single quantum wells and the dashed line gives the coupled wave function. For the sake of simplicity, only the ground states of each

case are shown.

The transition energies in DQW structures with various barrier widths and applied electric fields are demonstrated by photoluminescence (PL) measurement. The PL measurements were performed at approximately 30 K using an Ar^+ laser as the excitation source. The experimental data are compared with the results of modeling calculation.

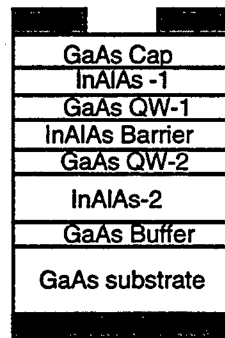

Figure 1 Schematic Of Structure

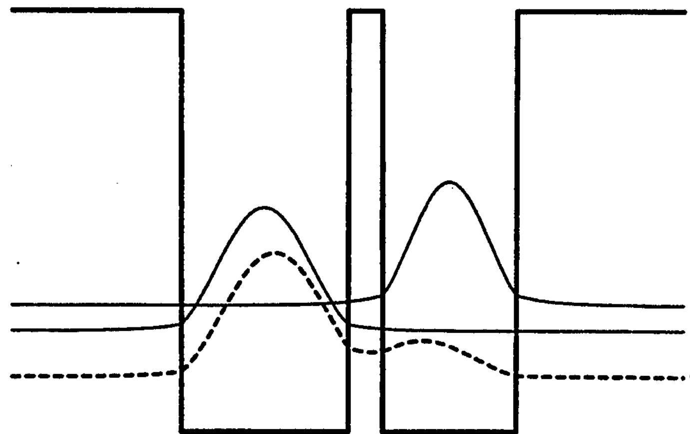

Figure 2 Coupling Effects in DQW

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InAs/GaAs Quantum Dot Active Regions in Oxide-Confined Vertical-Cavity Surface-Emitting Lasers

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The majority of the quantum dot (QD) research has focused on the physics and potential benefits of the 3-D confined density of states for edge-emitting lasers, but more recently several VCSELs have been demonstrated. Besides the interesting physics, a technologically more important characteristic of InGaAs QDs grown by strained-layer epitaxy on GaAs may be that they can achieve a high quality semiconductor energy gap corresponding to a wavelength significantly longer than 1.0 µm. Using an InAs/GaAs QD active region, we have demonstrated electroluminescence data peaked at 1.28 µm, and we have extended the lasing wavelength achieved on a GaAs substrate to 1.15 µm by placing the QDs in a low loss oxide-confined VCSEL structure. In addition, our initial results strongly suggest that with the same QD active region and proper cavity tuning, low threshold lasing can be obtained at wavelengths beyond 1.25µm.

A schematic illustration of the VCSEL is shown in Fig. 1. The 1.15µm VCSEL is grown by MBE on a GaAs substrate with 35 pairs of undoped GaAs/AlAs DBRs and 7 pairs of MgF/ZnSe high contrast top DBRs. The bottom mirrors are undoped to reduce free carrier absorption and improve the material quality as Si-doping in AlAs tends to cause roughening. The active region is 5 repetitions of a 1 monolayer InAs/ 1monolayer of GaAs cycle surrounded by GaAs barriers on top of a half-wave cavity n-GaAs spacer layer.

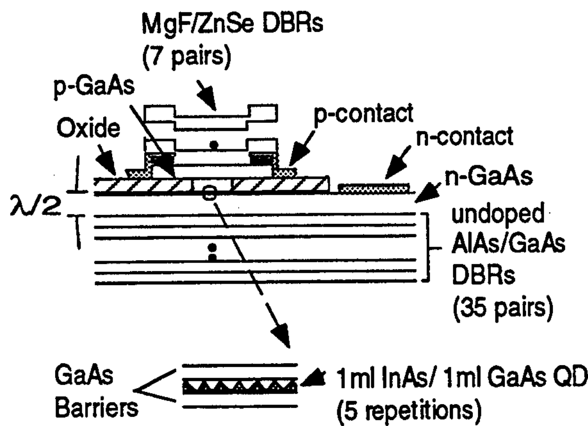

Figure 1: Schematic of 1.15µm oxide-confined VCSEL structure using intracavity contact and high contrast upper DBRs.

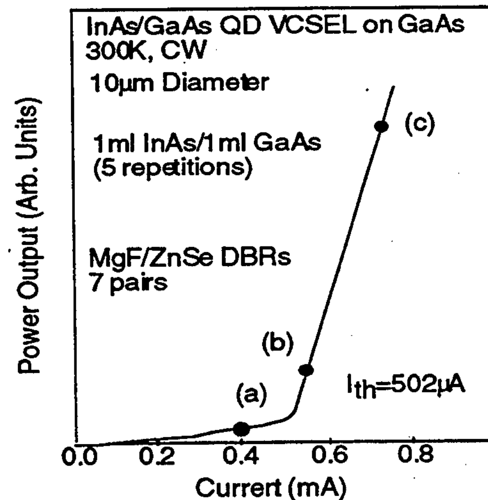

Figure 2: Light versus current curve showing CW lasing threshold of 502µA for a 10µm oxide aperture.

The p-type layers consist of quarter-wavelength AlAs and GaAs layers followed by highly p-doped AlGaAs and GaAs contact layers which are selectivity etched from the optical cavity. The p-AlAs is oxidized to provide lateral optical and electrical confinement. Figure

2 shows a light versus current (LI) curve of a 10μm device under continuous-wave (CW) room temperature operation with a lasing threshold of 502 μA. The LI curve is taken using a Si photodetector which has not been calibrated at the long wavelength. Figure 3 shows spectral data below and above threshold at 400μA, 580μA and 700μA. Below threshold the spectrum shows several transverse modes which may be due to polarization effects or the lateral dimension of the oxide-confined active region. Above threshold, at 700μA, the spectrum shows single mode lasing at 1154nm with a lasing linewidth of <0.50Å.

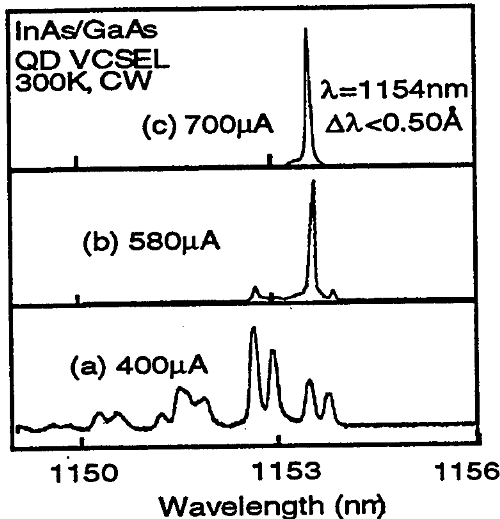

Figure 3: Spectral emission from QD VCSEL. Lasing wavelength is 1.154μm.

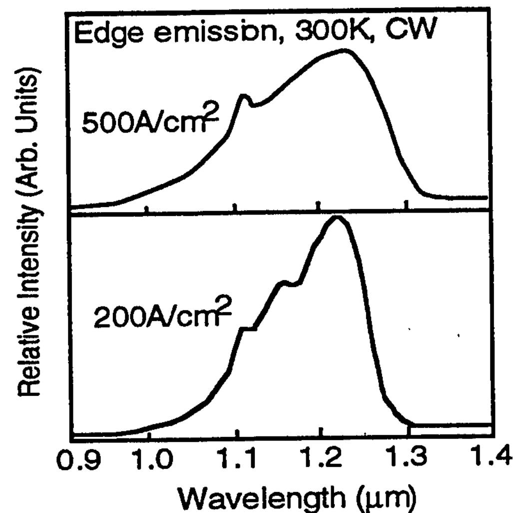

Figure 4: Electroluminescence from the edge of the QD VCSEL structure. Strong electroluminescence is achieved beyond 1.25μm.

Since the lasing wavelength of 1.154μm is predominantly set by the vertical cavity resonance as opposed to the QD transitions, we have also measured the electroluminescence from the edge of a 20μm x 300μm stripe device fabricated without the upper MgF/ZnSe DBR. This electroluminescence is shown in Fig.4 at a current density of 200A/cm^2 and 500A/cm^2. At 200A/cm^2 we see a dominant peak at 1.218μm, a second shorter wavelength peak at 1.134μm and a third even shorter wavelength peak at 1.109μm. Because of the prominence of the peak at 1.109μm at the higher current density, we believe that this is the wetting layer, the second peak (1.134μm) is the first excited state. Therefore, the lasing is attributed to energy levels between the ground and first excited electronic states of the QDs. This spectrum suggests that with the same QD active region and proper cavity tuning, low threshold lasing can be obtained at wavelengths beyond 1.25μm. By increasing the InAs/GaAs repetitions, we can further increase the QD emission wavelength to >1.3μm. However, due to limited gain in the QD ground states, it will be necessary minimize the optical cavity loss, perhaps by oxide/GaAs DBRs, in order to achieve 1.3μm GaAs-based VCSELs using InAs/GaAs QDs. These issues will be discussed further in this talk. We will also describe the low threshold CW lasing from InGaAlAs single layer QDs using oxide-confined half-wave cavity VCSELs tuned at 0.95μm.

InP-based multi-spectral quantum well infrared photodetectors

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Abstract
High-quality, lattice-matched multiple quantum well structures of InGaAs/InP and InGaAs/AlInAs grown on InP substrate by gas-source molecular beam epitaxy allow the fabrication of infrared photodetectors with simultaneous absorption in the mid-wavelength (3-5 μm) and long-wavelength (8-12 μm) infrared spectral bands. The gain measured is larger than equivalent GaAs/AlGaAs quantum well infrared detectors, indicating that improved transport and carrier lifetime are obtained in the InP-based materials. As a result, a large detectivity of 5×10^{11} cm $\sqrt{Hz}$ / W at 1.2 V was measured for the InGaAs/InP QWIP at T=80K Photoresponse spectra with FWHM of only Δv=0.13 μm demonstrate excellent capability for low-cross talk multi-spectral detection.

1.0 Introduction

The demand for automatic target detection, definition, and recognition is mandating the development of dual wavelength forward looking infrared (FLIR) sensor arrays. Two-color infrared detectors designed for dual band applications require mid-wavelength infrared (MWIR) and long-wavelength infrared (LWIR) focal plane arrays to be monolithically integrated on a single substrate. This objective has been difficult to achieve due to the lattice mismatch between commonly used interband MWIR and LWIR infrared materials such as InSb and HgCdTe. For this reason, stacks of lattice-matched multi-quantum well intersubband photodetectors have been proposed for use in multi-color infrared detectors.

Since infrared absorption due to intersubband transitions was first observed in multiple quantum well (MQW) structures[1], quantum well infrared photodetectors (QWIPs) and arrays based on this principle have become a competitive infrared technology.[2] Because of the extensive scientific and commercial exploration of the AlGaAs/GaAs material system over the past decades, the application of this technology to QWIPs has rapidly reached commercial maturity. However, in this system the perpendicular carrier transport rapidly degrades when the $Al_xGa_{1-x}As$ barrier becomes indirect gap (for $x > 0.45$). For this reason, the shortest wavelength infrared detector possible with this material system is ~ 6 μm.[3]

Thus, the need to achieve mid-wavelength absorption has lead to studies of other material systems such as $In_{0.2}Ga_{0.8}As/Al_{0.38}Ga_{0.62}As$[4], and $In_{0.53}Ga_{0.47}As/Al_{0.48}In_{0.52}As$[5]. These material systems avoid the use of indirect gap AlGaAs barriers.

For some applications, especially for tunneling devices, $In_{0.53}Ga_{0.47}As/Al_{0.48}In_{0.52}As$ MQWs lattice-matched to InP substrates have several advantages in comparison to structures composed of $InGaAs/Al_xGa_{1-x}As$, where x is small enough to ensure a direct energy gap in the AlGaAs barrier material:

(1) the effective mass of the electrons, which governs the drift mobility and tunneling properties, amounts to $0.041 \cdot m_o$ in InGaAs as compared to $0.053 \cdot m_o$ in $In_{0.2}Ga_{0.8}As$/AlGaAs, where m_o is the free-electron mass.

(2) The MWIR InGaAs/AlInAs quantum well detector is lattice matched with LWIR InGaAs/InP QWIP detectors, allowing a 2-color lattice-matched detector stack to be grown on InP. The InGaAs/AlGaAs QWIP is strained 7% to GaAs, which introduces dislocations into the growing layer and degrades its performance and that of the subsequent LWIR GaAs/AlGaAs detector.

In this paper, we demonstrate that high quality quantum well infrared photodetectors in both the 3-5μm and 8-12μm spectral bands can be grown on InP substrate using gas-source molecular beam epitaxy.

2.0 Experiment

The device parameters of the QWIPs studied are listed in Table I, where L_B represents the barrier width, L_W is the well width, and N_D denotes the donor doping concentration of the quantum wells. The wafers were grown using an EPI modular Gen-II gas-source molecular beam epitaxy system equipped with arsine and phosphine sources for As and P. Metallic gallium and indium were used for group III elements. The devices were grown on semi-insulating InP (100) substrates. After epitaxial growth, standard photolithographic process is used to fabricate mesa photodetectors. A square active area of 1.6×10^{-3} cm^2 was defined and 1600 Å-thick AuGe/Ni/Au ohmic contacts were deposited by electron beam evaporation and patterned using a lift-off process.

Table I. Device parameters for the measured QWIPs.

QWIP	A	B	C	D
Barrier material	InP	Al0.48In0.52As	Al0.48In0.52As	Al0.48In0.52As
L_B	500 Å	300 Å	300 Å	300 Å
Well material	In0.53Ga0.47As	In0.53Ga0.47As	In0.53Ga0.47As	In0.53Ga0.47As
L_W	56	30	35	40
N_D	$5x10^{17}$ cm^{-3}	$2x10^{18}$ cm^{-3}	$2x10^{18}$ cm^{-3}	$2x10^{18}$ cm^{-3}
Periods	20	25	25	25

3.0 Results

3.1 Long-wavelength Infrared InGaAs/InP QWIPs

The photocurrent in a QWIP is given by

$$I_{photo} = e\phi\eta\, g_{photo} \qquad (1)$$

where ϕ is the incoming photon flux, η is the quantum efficiency, e is the charge on an electron, and g_{photo} is the gain of the device. To determine g_{photo}, photocurrent or dark current noise measurements can be employed. The photocurrent method requires a measurement of the absorbed photon flux, i.e. the product $\phi\eta$. This measurement is complicated since a fraction of the incoming light is reflected and absolute power levels are difficult to measure accurately.

Noise measurements provide an elegant alternative. The spectral density of the dark current noise associated with the generation-recombination and trapping of carriers in a photoconductor is written as:[6]

$$i_n^2/\Delta f = S_{Idark} = 4e\, I_{dark}\, g_{noise} \qquad (2)$$

where g_{noise} is the noise gain and Δf is the measurement bandwidth. It has been shown[7] that $g_{noise} = g_{photo}$. Accepting this equivalence, the value of g_{photo} for QWIP A can be calculated from the data obtained from dark current and noise measurements. In order to determine the gain, the current and resistance were measured at T=80K as a function of applied voltage using an HP 4155A semiconductor parameter analyzer with the detectors shielded (i.e. dark). The current-voltage curve for QWIP-A is shown in Fig. 1. The noise measurements were made using a Stanford Research (SR770) FFT spectrum analyzer. In order to distinguish the noise of the photodetector from the noise of the amplifier and bias resistor contributions, four independent measurements are taken and then the results manipulated[8] to extract the noise of the photodetector. The noise and noise gain are shown in Figs. 2 & 3.

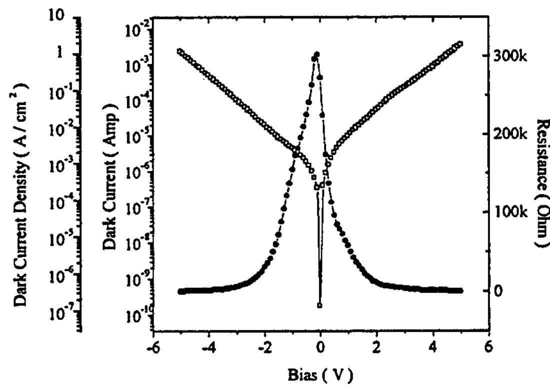

Fig. 1. The dark current and differential resistance vs. applied bias for QWIP-A at T=80K.

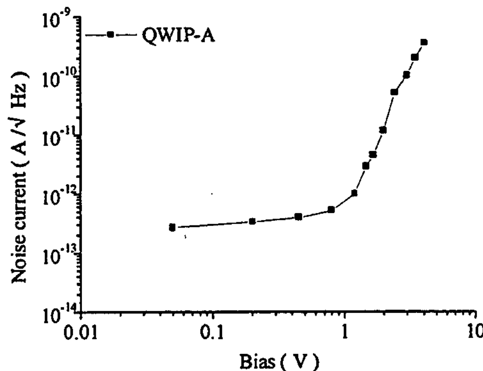

Fig. 2. Current noise at f=500Hz vs. applied bias voltage at T=80K.

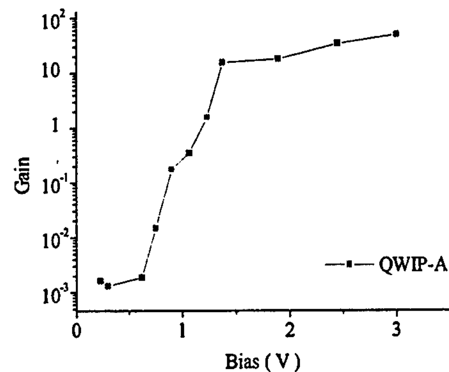

Fig. 3. Noise gain vs. applied reverse bias voltage at T=80K.

For this device, the noise gain increases with increasing bias voltage until a bias of ~ 3V is reached, at which point the gain saturates at a value near 50. This large gain is approximately 50 X larger than typically measured for AlGaAs/GaAs QWIP detectors[2]. As seen in Eq.(1), the photocurrent is proportional to the gain, while the noise current {Eq. (2)} is proportional to the square root of the gain. Thus the larger gain should result in higher detectivity in comparison to AlGaAs detectors. Possible reasons for high gain in comparison to AlGaAs/GaAs QWIPs include the higher mobility and higher saturation drift velocity of the binary InP barriers. The binary InP may also have a lower defect density in comparison to the ternary AlGaAs. Such defects can act as electrical traps and increase the capture probability.

The spectral response of QWIP-A at 80K is measured by using a Mattson Fourier transform IR spectrometer (GL3020). Absolute responsivity is measured using a Mikron blackbody source (M305) chopped at 500Hz and an EG&G 5209 lock-in amplifier. The blackbody temperature was 800K. Peak responsivity was calculated by integrating the normalized spectral response with the blackbody responsivity. The normalized spectrum under an applied electric field of 10 kV/cm is shown in Fig. 4. The photoresponse peak is found to be 8.1 μm and the cutoff wavelength is about 9 μm. The absolute responsivity is shown in Fig. 5 as a function of bias.

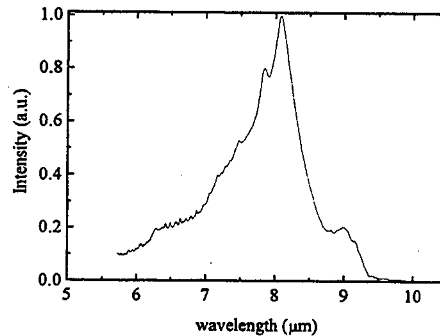

Fig. 4 Normalized spectral response at 80K with a peak of 8.1 μm.

The peak responsivity value of 7.5 A/W at 5 V reverse bias is approximately one order of magnitude higher than that typically obtained in AlGaAs/GaAs QWIPs. The specific detectivity (D*) and noise current of the QWIP at 80K are shown as a function of applied electric field in Fig. 3. The maximum D* of the QWIPs measured in this work was found to be 5×10^{11} cm $\sqrt{Hz}$ / W at 1.2 V.

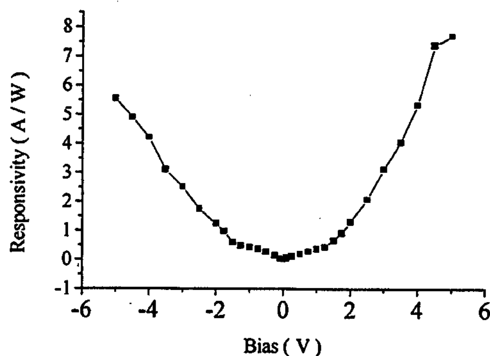

Fig. 5. Responsivity for InGaAs/InP QWIP as a function of bias.

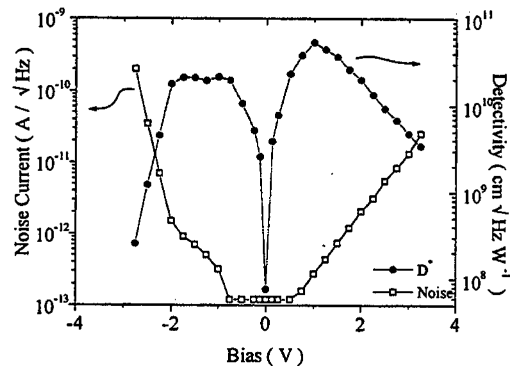

Fig. 6. Detectivity for InGaAs/Inp QWIP as function of bias.

3.2 Mid-wavelength Infrared InGaAs/AlInAs QWIPs

In order to determine the wavelength range at which InGaAs/InAlAs QWIPs can operate, we have calculated the energy levels in InGaAs/AlInAs MQW structures. For this calculation, we have assumed $m_{well} = 0.041 \cdot m_o$, $m_{barrier} = 0.075 \cdot m_o$, $Eg_{77Kwell} = 1.508$ eV, $Eg_{77Kbarrier} = 0.801$, and $\Delta Ec = 0.5$ meV. In Fig. 2 the n=1 and n=2 electron energy levels are plotted versus the well width. The n=2 level is confined to the well for well widths larger than 35 Å, and is an extended band for narrower wells. For wells thicker than 35 Å the intersubband absorption energy is plotted as an dashed line calculated from the energy difference between the n=1 and n=2 states. For narrower wells the absorption energy is plotted as a dotted line calculated from the difference in energy between the confined n=1 and the center of the continuum band. The experimental data points for samples A-C are also shown, demonstrating good agreement with our model calculations.

The relative spectral response for the three samples was measured using a Mattson Fourier transform infrared (FTIR) spectrometer. The measurements were made at T=77K under varying forward and reverse biases. No change in the shape of the spectral response occurred for ±5 V bias for these samples.

The result of the measurement is shown in Fig. 3. All three samples have significantly narrower spectrum than previously reported for $In_{0.2}Ga_{0.8}As/Al_{0.38}Ga_{0.62}As$[9]. The difference in spectral width when the well is changed from L_w = 30 Å to 40 Å is in excellent agreement with our theoretical calculations. According to the calculations, the first excited state for the 30 Å sample is in the continuum, resulting in a broad absorption spectrum. On the other hand, the excited state in the 35 Å sample is just slightly bound (quasi-bound), and in the 40 Å sample is more strongly bound. In either case, the intersubband absorption for both is narrow in excellent agreement with experiment. To our knowledge, the spectral width (Δv = 0.13 μm) of sample C is the narrowest reported for a QWIP.

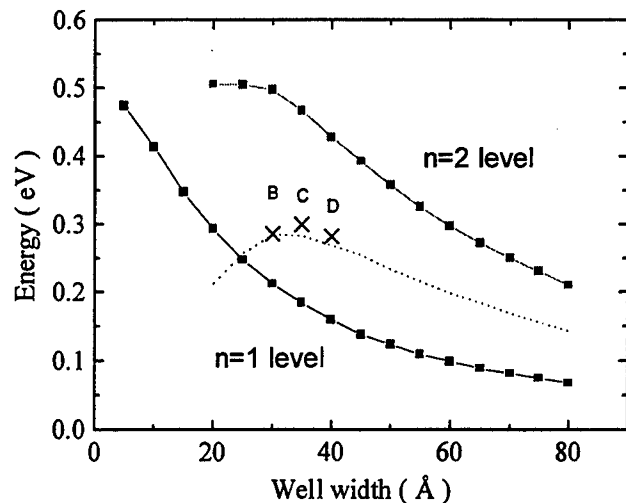

Fig. 7. The calculated two first electron levels in InGaAs/AlInAs quantum wells (solid lines) vs. well width. Experimental data points obtained for samples B-Dare shown as well.

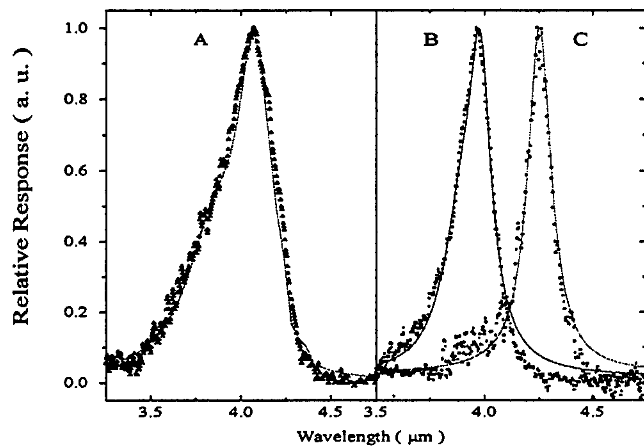

Fig. 8. Measured spectral responsivity of samples A-C at T=77K with 1 V reverse bias.

4.0 Summary

In conclusion, we report the largest reported QWIP photoconductive gain of 50, which is an improvement of 50X over typical values of GaAs/AlGaAs QWIPs. We have also demonstrated the narrowest spectral width (0.13 μm) reported for the MWIR quantum well detectors. As a result, a large detectivity of 5×10^{11} cm $\sqrt{Hz}$ / W at 1.2 V was measured for the InGaAs/InP QWIP at T=80K The results of these measurements indicate that integrating InGaAs/AlInAs and InGaAs/InP multi-quantum wells together on a single InP substrate offer a multi-spectral detector which can provide imaging in both MWIR and LWIR spectral bands on a monolithically integrated focal plane array.

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High Speed and High Gain-Bandwidth Product Resonant-Cavity Separate Absorption, Charge and Multiplication Avalanche Photodiodes

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1 Introduction

High-speed and high-sensitivity photodiodes are key components in long-haul, high-bit-rate optical communication systems. Avalanche photodiodes (APDs) are preferred for these systems because their internal gain provides higher receiver sensitivity than can be achieved with PIN photodiodes[1,2]. The key performance factors of APDs include high quantum efficiency, low dark current, high speed, a low multiplication noise, and a high gain-bandwidth product. It was previously reported that resonant-cavity separate absorption and multiplication (SAM) APDs can achieve all these requirements[3,4]. A peak external quantum efficiency of ~ 80% was achieved even though the $In_{0.1}Ga_{0.9}As$ absorption region was only 35 nm thick. These resonant-cavity SAM APDs also exhibited low dark current (< 10 nA at 90% breakdown), low multiplication noise (0.2 < k < 0.3), and low-gain bandwidth >20 GHz[3]. We describe a resonant-cavity SAM APD with an additional charge layer that provides better control of the electric field profile. By changing the doping levels in the charge layer, these SACM APDs have achieved record bandwidths (33 GHz at low gain) and gain-bandwidth products (290 GHz).

2 Design and Fabrication

The SAM APD structure was first developed to decrease the dark current because it permits a high field to be maintained in the multiplication region while keeping the field in the absorption region low[2]. More significantly, however, the SAM structure insures single-carrier injection into the multiplication region which leads to lower multiplication noise[4]. The resonant-cavity approach affords several benefits, one of which is that it decouples the optical and electrical path lengths[5]. This is a result of the fact that the photons in the cavity undergo multiple reflections between the top and bottom mirrors, thus increasing the effective absorption thickness. Consequently, resonant-cavity photodetectors can achieve high quantum efficiencies and wide bandwidths even for very thin absorption regions. While at high gains, the most significant limitation on the bandwidth of APDs is the avalanche buildup time, which depends on the gain, the thickness of the multiplication region, the electron and hole velocities, and the physics of the ionization process. It has been shown that the gain-bandwidth product can be increased by reducing the thickness of the multiplication region[3]. Based on these considerations, it would be expected that incorporating a SAM APD with a thin multiplication layer into a resonant-cavity structure should yield high bandwidths at low gain and high gain-bandwidth products at high gain. In order to utilize thinner multiplication layers, however, the doping level of the multiplication region of the SAM-APD structure must be increased. This can lead to band-to-band tunneling inside the high field region which can, in turn, produce excessive dark current. This problem can be effectively eliminated with the SACM APD structure that is described in this paper. With a

thin, uniformly-doped charge layer inserted between the intrinsic multiplication region and the absorption region, the high electric field inside the multiplication region becomes uniform compared to the spike profile of the SAM APD structure. In addition, it is easier to control the field in the absorption region. The structure and electric field profile of a resonant-cavity SACM APD are showed in Figure 1.

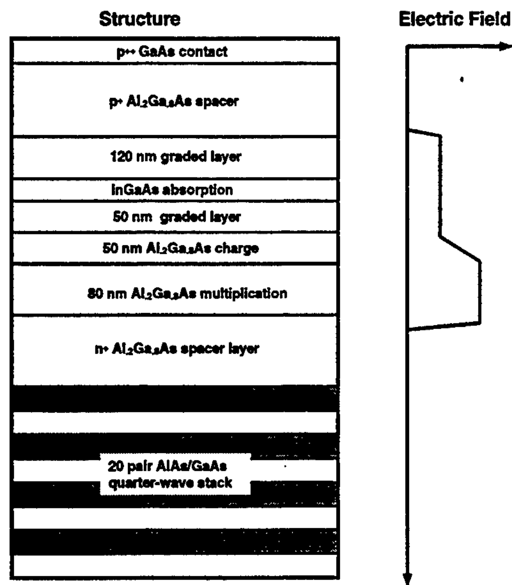

Figure 1. The structure and electric field profile of a resonant-cavity SACM APD.

The SACM APDs were grown by molecular beam epitaxy on semi-insulating GaAs (100) substrates. The bottom mirror consisted of a 20 pair n-type GaAs/AlAs $\lambda/4$ stack. An n^+ (4×10^{18} cm^{-3}) GaAs contact layer was grown after the bottom mirror layers. This was followed by three $Al_{0.2}Ga_{0.8}As$ layers, an n^+ spacer layer, a thin undoped multiplication region, and a uniformly-doped "charge" layer. A thin graded buffer region was then grown followed by the $In_{0.1}Ga_{0.9}As$ absorption layer. The composition was then graded back to $Al_{0.2}Ga_{0.8}As$ and a p^+ $Al_{0.2}Ga_{0.8}As$ top layer was grown to a thickness such that the cavity was resonant at the desired wavelength. Finally, a thin 30 nm thick p^+ (10^{19} cm^{-3}) GaAs layer is used for the top contact. In addition to RHEED growth-rate calibration, a Filmetrics optical monitoring system was used to ensure that the optical thickness of the cavity was correct.

The high-speed device fabrication has been described earlier[3]. The p-type contact was formed by first depositing two thin layers of Ni(5nm)/Pt(5nm) followed by conventional Ti-Pt-Au layers. From the transmission-line-method (TLM) patterns, the contact resistance was determined to be 1.5×10^{-6} Ωcm^2. Also, in order to balance the transit-time and RC components of the bandwidth, the intrinsic region of the device was chosen to be 450 nm. From impedance measurements, the forward-bias resistance of an SACM APD device with a diameter of 14μm was determined to be 30 Ω and the capacitance was 48 fF. Calculations show that the combined effect of the RC time constant and the transit time yield a bandwidth of 33 GHz. From the measured device capacitance, the parasitic capacitance was extrapolated to be 15 fF.

3 Results and Discussion

It was previously reported that thin multiplication regions exhibit lower noise[6] than conventional noise theories would predict[7]. Conventional theories assume that the impact ionization process is a continuous local process. This assumption is not valid for thin multiplication regions where non-local effects such as the "dead space"[8] effect become significant. In addition, Monte Carlo simulations show that the spatial distribution for ionization events is narrower for thin multiplication regions which leads to lower noise. This has been confirmed recently by investigating a series of GaAs and $Al_{0.2}Ga_{0.8}As$ PIN homojuction APDs. Width-dependent ionization coefficients were empirically determined, both for holes and electrons, by fitting the measured I-V characteristics and the multiplication noise. It was found that there is clear width dependence for the ionization coefficients of thin multiplication layers. The effective ionization coefficients are much lower than that of the bulk values that were reported by Bulman[9] and Robbins[10].

Using the effective ionization coefficients that were obtained from the GaAs and $Al_{0.2}Ga_{0.8}As$ homojuction APDs, the I-V characteristics of an SACM APD have been simulated. The SACM APD had an 80 nm multiplication region and a 50 nm charge layer with $7x10^{17}$ cm^{-3} p-type doping. Figure 2 shows simulated and experimental DC current-voltage curves. The simulated results, using the effective ionization coefficients, are reasonably close to the experimental results, while the simulated gain curve using the bulk ionization coefficients for GaAs[9] and $Al_{0.2}Ga_{0.8}As$[10] gives much lower breakdown voltage and the wrong curvature. Since the charge layer doping is $7x10^{17}$ cm^{-3}, the electric field in multiplication region is high. Notice that there is a gain of 1.2 even at the punchthrough voltage, i.e., the voltage at which the edge of the depletion region reaches the absorption layer. This was confirmed by the quantum efficiency measurement performed at the puchthrough voltage.

The frequency response of SACM APD

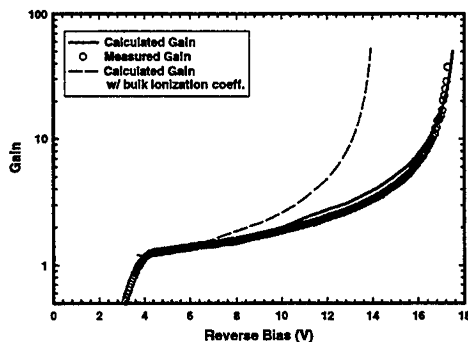

Figure 2. Measured and calculated DC current-voltage characteristics of an SACM APD with 80 nm multiplication layer, 50 nm p-type ($7x10^{17}$ cm^{-3}) charge layer and 300 nm low-field region.

devices was measured by analyzing the photocurrent spectrum with a microwave probe system and a 50 GHz spectrum analyzer[3]. A passively mode-locked Ti-sapphire laser with ~200 fs pulsewidth and 76 MHz pulse repetition rate was used as the optical source. The bandwidth versus DC avalanche gain of an SACM APD device is shown in Figure 3. A gain-bandwidth of 290 GHz is observed at high gains. These results take the gain at punchthrough of 1.2 into account. This gain-bandwidth product is the highest reported for an APD. Comparisons to the best Multiple Quantum Well (MQW) APD[11] and the planar SACM APD[12] are also shown. The speed in the low gain regime is determined to be 33 GHz, which is also the highest reported bandwidth for any type of APD.

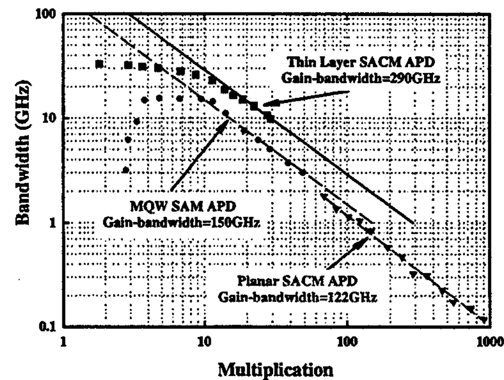

Figure 3. The measured bandwidth vs. DC gain for the same SACM APD structure as in Figure 2.

In the design of the SACM APDs the thickness of the absorption and multiplication regions and the doping of the charge layer are critical parameters. Regarding the thickness of the multiplication region, our noise measurements are consistent with reports that thinner multiplication regions yield higher gain-bandwidth products. In the charge layer increasing the doping will result in higher peak fields in the multiplication region and lower fields in the absorption region. The high multiplication-region field will give rise to a small gain at punchthrough, the voltage that is usually taken as the unity gain reference point. The primary concern for the absorption region and the adjacent intrinsic layers is to minimize unwanted multiplication. If there is even a small degree of multiplication in the absorption region, the resulting feedback process will significantly increase the avalanche buildup time and thus reduce the gain-bandwidth product. Higher doping levels in the charge region can decrease the field in the absorption region and thus minimize this

effect. Figure 4 shows the calculated gain-bandwidth product and the gain at

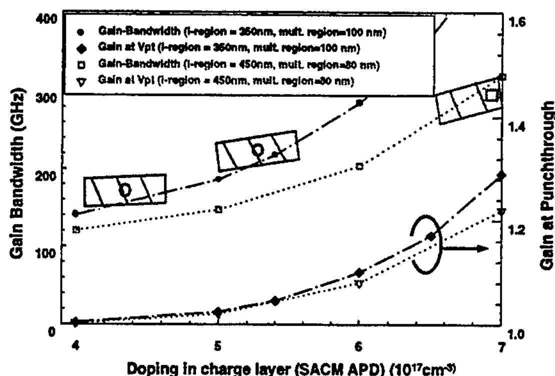

Figure 4. The calculated gain-bandwidth and gains at punchthrough for the SACM APDs as the function of doping levels in the charge region. The hollow symbols indicate the measured gain-bandwidth products and the larger boxes indicate uncertainty in the doping and speed measurements.

punchthrough versus doping levels in the multiplication region. The correlation between the doping level in the charge layer and the gain-bandwidth product has been confirmed by the experimental results. Three SACM APDs have been studied. For two of them the total thickness of the intrinsic region was 350nm. This included a 100nm multiplication layer and a 50nm charge layer (n~4.4×10^{17} cm^{-3} and 5.3×10^{17} cm^{-3}). The third wafer had a 450nm total intrinsic region with an 80nm multiplication layer and a 50nm charge layer (7×10^{17} cm^{-3}). There is a clear trend of increasing gain-bandwidth product with increasing doping levels in the charge region, an indication that the ionization in the low-field region is one of the primary limitations to the gain-bandwidth product of these devices. Even if the doping level of the multiplication region is the same, the simulation shows that the structure with a thinner intrinsic region has the higher gain-bandwidth product. While we report a record 290 GHz gain-bandwidth, simulation shows that even higher gain-bandwidths can be achieved with optimized absorption and spacer layer design.

4 Conclusion

In summary, we have designed and fabricated a record high-speed and high gain-bandwidth resonant-cavity SACM APD. The 3dB bandwidth in the low gain regime is 33 GHz and a gain-bandwidth product of 290 GHz is achieved. With width-dependent ionization coefficients, the current-voltage, gain and bandwidth characteristics of these devices have been simulated and confirmed by experiments. A correlation between the gain-bandwidth products and the doping levels in the charge layer has been observed and explained. It is believed that even higher gain-bandwidth products should be achievable.

This work has been supported by the Joint Services Electronics Program, the DARPA-sponsored Center for Optoelectronic Science and Technology and the National Science Foundation.

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Mid-Infrared Quantum Cascade Lasers Grown By Gas-Source Molecular Beam Epitaxy

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Intersubband semiconductor devices have been investigated for a variety of purposes. The quantum well intersubband photodetector (QWIP) has been the subject of at least 10 years of research, with the first publicized results appearing in 1987[1]. The counterpart to this device, based on intersubband emission, was proposed much earlier[2]. Both devices offer a way to access a wide range of infrared wavelengths using mature growth technology. Using quantum-size effects, the semiconductor crystals are no longer limited by their inherent band gaps. Because the QWIP has been so successful from both a research and industrial standpoint, it stands to reason that an intersubband laser is also an attractive candidate for development.

There are many proposed methods for producing optically pumped intersubband lasers[3][4], but much of the appeal of the semiconductor laser relies on its compact size. Towards this end, work is also being done on electrically injected intersubband lasers. One group has experimentally demonstrated[5] such lasers using solid-source molecular beam epitaxy. It has been dubbed the "quantum cascade laser" (QCL). The QCL has been proven to have a wide range of emission wavelengths (4-12 μm)using GaInAs/AlInAs as its basis. Also, this device can operate at room temperature, which no interband laser is able to do as of yet in this wavelength range, and which is a desirable trait for a portable laser source.

In this paper, the theory necessary to analyze the QCL design is presented. Excellent agreement is reached between this theory and experimental observations for both 8.5 and 5.1 μm QCL structures grown by gas-source molecular-beam epitaxy (GSMBE). Because GSMBE has both As and P sources readily available and easily controllable, it allows us to grow the QCL structure in a single growth step, with abrupt InP/GaInAs heterojunctions. This is important to minimize surface states and strain.

In an intersubband laser, light is emitted by electrons relaxing from upper to lower subbands in a quantum well active region. For the QCL, the second and third subbands are the lower and upper lasing levels respectively, while the first level is a drain for subband 2 electrons. The wavelength of the light emitted is dependent solely on the energy separation between the second and third subbands and can be changed with the width of the quantum wells.

Electrons are injected into the active region by a specially designed injector which surrounds the active region on both sides. This injector supplies high energy electrons to the upper lasing level on one side, and also removes low energy electrons from the first level on the other side. The combination of the active and injector regions as a unit allows many identical units to be stacked together in a single device. This allows a single electron to possibly emit many photons. The probability of an electron emitting a photon is proportional to the square of the optical matrix element, $|\langle 2|z|3\rangle|^2$, as well as the population inversion between levels.

The mechanism behind any lasing revolves around how population inversion is achieved. For the QCL, good coupling to the injector and polar optical phonon interactions establish the occupation probability among levels. The optical phonon scattering events, which are electron-lattice interactions, take place on an incredibly fast time scale. Starting with an energy resonant with the optical phonon, this lifetime is measured in hundreds of femtoseconds and it increases quickly for a larger momentum transfer. While electrons injected into the upper lasing level will relax via polar optical phonon emission to the second level, the electrons in the second level are evacuated to the first level as a much faster rate. This action allows a population inversion between the second and third levels.

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Our first task was to understand the QCL structure. Towards this end, the theoretical basis that allows us to analyze the active and injector regions will be explained. All the factors explained above come together for a specific structure at a designed electric field, which establishes energy lineup and electron distribution among adjacent layers. The active region of the QCL is a triple AlInAs/GaInAs quantum well structure that supports three bound states, or subbands. The injector region is composed of four coupled quantum wells and acts as an energy filter for electrons. The allowed electron wavefunctions and energy levels are obtained numerically with a shooting method and fourth-order Runge-Kutta solution to Schrödinger's equation in one dimension. Electron/light-hole band coupling and electron/split-off band coupling are taken into account by using an energy dependent effective mass, m(E,z)[6]. The energy dependent effective mass is applied both for the well and barrier material. The specific parameters used were: E_p(GaInAs)= 19.95 eV, E_v(GaInAs)= 0.858 eV, E_p(AlInAs)= 21.4 eV, and E_v(AlInAs)=1.605 eV. The results are shown in Fig. 1a for a 8.5 μm QC laser. The specific barrier/ well thicknesses of the active and injector regions, starting with the injector barrier, are (in nm): (4.0/2.1), (1.0/7.8), (1.3/5.7), (2.4/4.6), (1.4/3.8), (1.2/3.8), (1.7/4.0). Under an applied electric field of 64 kV/cm, the energy separation between the lasing levels is 145.1 meV. The optical matrix element for these two levels is calculated to be 2.35 nm. Similar calculations can be performed for any desired wavelength within the 4-12 μm range.

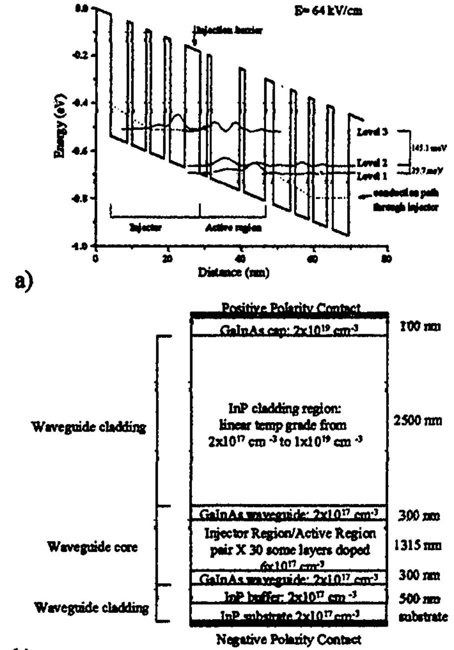

Fig. 1 (a) Conduction band schematic of an 8.5 μm quantum cascade active region surrounded by two injector regions at an electric field of 64 kV/cm. The squared moduli of wavefunctions involved in the lasing transition are shown as solid curves. Dashed lines indicate the conduction path of electrons through the injector regions. (b) Cross-section of laser structure grown by gas-source molecular beam epitaxy. All material is grown lattice-matched to the InP substrate with thicknesses and doping levels given.

Continuing analysis on the 8.5 μm laser structure, polar optical transition rates are calculated using the following expression[7]:

$$W_{ij}(k_i)=\frac{e^2\omega_0(n(\omega_0)+1)}{8\pi\varepsilon_\rho}\int\frac{\left|\langle j|e^{iq_z z}|i\rangle\right|^2}{\sqrt{\frac{\hbar^4 k_i^2 q_z^2}{m^{*2}}+\left(\frac{\hbar^2 q_z^2}{2m^*}+E_i-E_j-\hbar\omega_0\right)^2}}dq_z$$

where $n(\omega_0)$ is the optical phonon number, ω_0 is the longitudinal optical phonon frequency, k_t is the electron in-plane momentum, q_z is the z-component of the phonon momentum, E_i and E_j are the energy levels at k_t=0 of the ith and jth subband respectively, and ε_ρ is the reduced permittivity:

$$\varepsilon_\rho^{-1}=\varepsilon_0^{-1}+\varepsilon_\infty^{-1}$$

Using 77 K as the temperature, ω_0=5.16x10^{13} s^{-1}, and ε_ρ=6.217, inter- and intrasubband transition times were calculated for an isolated active region. The lifetime of an electron at k_t=0 in band 3 is:

$$\tau_3^{-1}\approx W_{31}+W_{32}$$

This τ_3 value, at 77 K equals 1.1 ps. The lifetime of a level 2 electron depends strongly on the electron momentum. After the large momentum transfer from subband 3, $W_{21}^{-1}(k_t\neq 0)$~ 1 ps. At k_t=0, however, the lifetime is much shorter ~ 0.3 ps. The net result at low temperature is that electrons will collect primarily in the first and third subbands, with the second subband remaining essentially empty. The absolute populations will depend on the rates of electron injection and removal. Assuming resonant tunneling is the primary injection and removal mechanism, these rates are sufficiently fast for population inversion.

The QC laser structures we tested were grown in a single growth step by an Intevac Modular Gen II GSMBE reactor. The active and injector regions are made of GaInAs and AlInAs lattice matched to n-type InP substrates at a growth temperature around 530° C. This particular heterostructure

(GaInAs/AlInAs) is ideal because of its large conduction band offset (~510 meV), which allows a wide range of intersubband emission wavelengths. The waveguide core consists of 25 or 30 active/injector pairs surrounded on both sides with n-type GaInAs. To increase the thermal conductivity of the device, a thick, 2.5 μm InP waveguide cladding region was grown directly on the core. Doping in this region was graded from $1x10^{17}$ to $1x10^{19}$ cm^{-3} Also, a cap layer of n+ GaInAs ($2x10^{19}$ cm^{-3}) was placed below the top contact of the 8.5 μm laser in an attempt to push the surface plasmon mode to longer wavelengths[2]. A cross-section of the 8.5 μm laser is shown in Fig. 1b.

Stripes of 15 μm width were processed in the cladding region to confine current with photolithography and wet chemical etching. The stripes were insulated from the surrounding surface with 2000 Å of Al_2O_3. The top and bottom contacts to the lasers were made with evaporated Ti/Pt/Au annealed at low (~200 °C) temperature. Two cavity lengths (1.5 & 2.0 mm) of the 8.5 μm laser were tested. The 5.1 μm laser was tested with 2 and 3 mm long cavities. The lasers were then mounted with In on copper heat sinks. The heat sinks were loaded in a temperature-controlled (77-300 K) Janis liquid nitrogen cryostat and driven with 1 μs pulses at a repetition rate of 200 Hz. Currently, we do not have the equipment to drive the lasers in continuous wave or with shorter pulses. Output from the 8.5 μm laser and 5.1 μm laser was collected through f/1.0 optics into liquid nitrogen cooled HgCdTe and InSb detectors respectively.

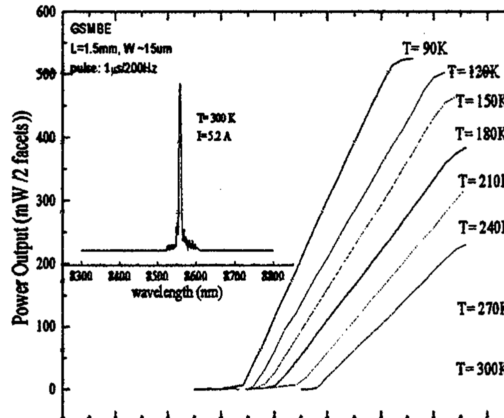

Fig. 2 Peak power vs. current as a function of temperature from 90-300 K. Cavity length is 1.5 mm and pulses are 1 μs long at a repetition rate of 200 Hz. Inset shows emission spectrum at 5.2 A and 300 K. Peak wavelength is 8560 nm.

Power output as a function of temperature for a typical 8.5 μm laser of 1.5 mm cavity is shown in Fig. 2. It operates up to room temperature in pulsed mode with power output exceeding 25 mW per 2 facets. This 1.5 mm cavity laser also emits over 500 mW per 2 facets at 79 K. A 2 mm long cavity shows higher power output, with a peak power at 79 K exceeding 700 mW per 2 facets. The threshold voltage for this structure is 12.2 volts. The inset shows the emission spectrum at 300 K, with a lasing wavelength of 8560 nm at 5.2 A. This corresponds to an emission energy of 144.9 meV which varies by only 0.2 meV from the theoretical prediction in Fig. 1a.

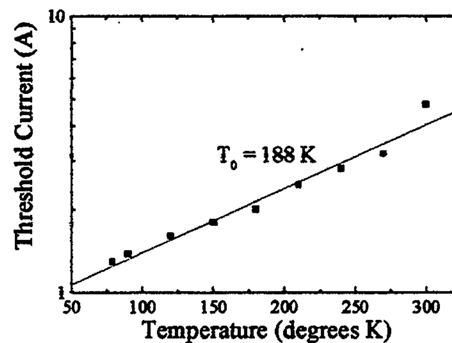

Fig. 3 Measured threshold current vs. temperature. Exponential fit of the form $\exp(T/T_0)$ from 80-300 K gives a T_0 of 188 K.

The current density as a function of temperature for an 8.5 μm laser is shown in Fig. 3. Fitting the threshold current as proportional to $\exp(T/T_0)$ gives a T_0 parameter of 188 K from 80-300 K. This is the highest T_0 for a QC laser reported to date. A higher T_0 implies slower degradation with temperature which is essential for high power applications at high temperatures.

We also have some preliminary results for a 5.1 μm laser structure. The theoretical predictions are shown in Fig. 4a. The structure consists of a 6 well injector and a 3 well active region. The power vs. current and emission spectrum for a 2 mm long cavity is shown in Fig. 4b. The observed emission wavelength centers around 5140.5 nm which corresponds to an energy of 241.2 meV, which is about 2.5 meV off the theoretical prediction.

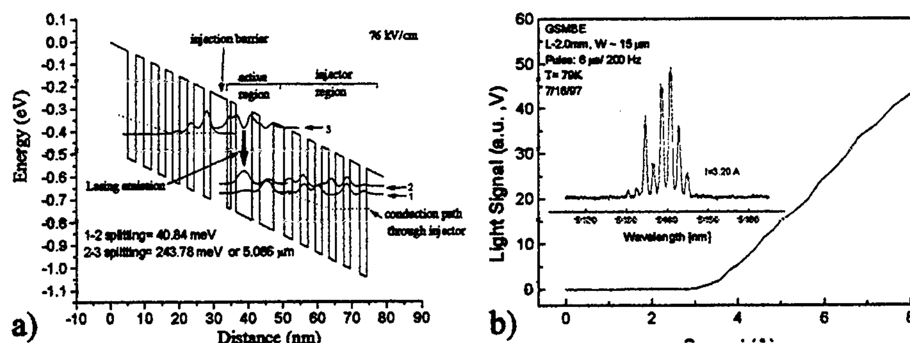

Fig. 4 (a) Conduction band schematic of an 5.1 μm quantum cascade active region surrounded by two injector regions at an electric field of 76 kV/cm. The squared moduli of wavefunctions involved in the lasing transition are shown as solid curves. Dashed lines indicate the conduction path of electrons through the injector regions. (b) Preliminary power vs. current and emission spectra for a 2mm long cavity at 79 K.

The basic theory of the QC laser has been discussed. It is shown to be a versatile technique for predicting intersubband emission wavelengths. We have now shown that is possible, even in a preliminary manner, for this type of laser to be produced using GSMBE. The laser structure has been simplified, and, in the case of the 8.5 μm laser, improved by use of this growth method. Output power exceeding 700 mW per 2 facets at 79 K and 25 mW at 300 K have been measured for an 8.5 μm laser. Also, the relative temperature insensitivity of threshold current shows potential for higher temperature operation (>300 K). The fact this type of laser is now shown to be repeatable regardless of wavelength or growth technique makes it a likely candidate for industrial production.

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Theoretical and Experimental Study of Near-Field Beam Properties of High Power Laser Diodes

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L. Brovelli, C. Harder

Abstract— **We present laser beam astigmatism results obtained by Near-field Scanning Optical Microscopy. Measurements made with this technique on the high reflecting facet of a Graded Index Separate Confinement Heterojunction laser diode indicate the lateral beam waist is outside of the device structure, seemingly in contradiction to far-field measurements made on the low reflecting output facet of the device. Our attempts to resolve the discrepancy by invoking thermal lensing due to a temperature gradient across the mirror facet is capable of partly generating the focusing required to explain the difference in observed beam waist position for the two separate measurements. Simulations which include inhomogeneities along the length of the device cavity may resolve the apparent discrepancy. This paper is eligible for best student paper.**

Keywords— **near-field scanning optical microscopy, astigmatism, laser diode**

I. Introduction

RECENTLY , using near-field scanning optical microscopy (NSOM) we observed focusing of the laser mode in the lateral dimension (in the plane of the p-n junction) outside of the device structure for a high power laser diode.[1]. The devices we studied are graded-index separate confinement heterojunction (GRINSCH) lasers diodes. These devices emit a nearly diffraction limited single lobe at 980 nm and are designed to pump Erbium doped fiber amplifiers for use in long distance telecommunication systems. The devices we studied were designed to be index guided in the lateral dimension. However, while predominately index guided, previous simulations and experimental evidence suggest that during high power output gain guiding contributes to the waveguiding of the laser mode.[2] Consistently, far-field studies on the low reflecting, output facet of similar devices show the lateral beam waist to be inside of the laser cavity as is expected for gain-guided devices.[3] Unlike the far-field studies, our NSOM results on the beam astigmatism of GRINSCH lasers diodes were carried out on the high reflecting facet of the device and found the device focusing outside of the mirror facet. In an effort to reconcile these facts, we have tried to simulate focusing of the laser mode outside of the laser cavity by means of an optical field induced temperature gradient on the high reflecting dielectric mirror stack.

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II. Device

We studied high power strained (In,Ga)As graded-index separate confinement heterojunction laser diodes. These devices emit a nearly diffraction limited single lobe at 980 nm and are designed to pump Erbium doped fiber amplifiers. The structure consists of a single InGaAs quantum well sandwiched in a symmetrical waveguide of graded AlGaAs cladding layers with parabolic refractive index variation. In the vertical dimension (along the crystal growth) the graded index of refraction provides guiding of the optical field. In the lateral dimension, a 5μm wide ridge is defined by wet etching to provide a step-index of refraction for optical guiding. The cavity facets are dielectric coated for front and rear reflectivities of 0.1 and 0.9, respectively.

III. Experiment

Near-field scanning optical microscopy and spectroscopy (NSOM) is a technique [4][5] where a small optical probe is placed within a fraction of a wavelength of a sample and scanned over the surface.[6] Typically an aluminum coated, tapered, single-mode optical fiber is used as the tiny aperture through which the light is coupled and yields a spatial resolution of order the tip size ($\sim$100 nm). The application of near-field imaging and spectroscopy to optoelectronic devices and laser diodes provides sub-wavelength information on device structure, performance, and output properties.[7][8] The emission profile is obtained by coupling the emitted radiation into the fiber-tip. We directly measure the optical

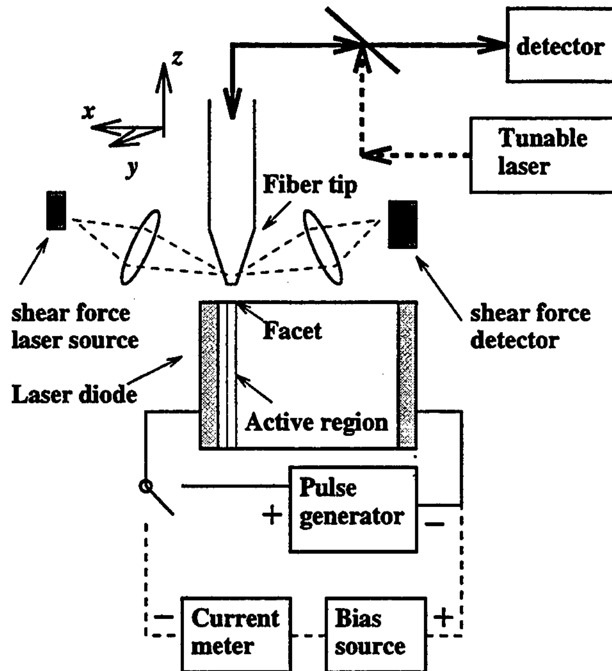

Fig. 1. Schematic of the experimental set-up.

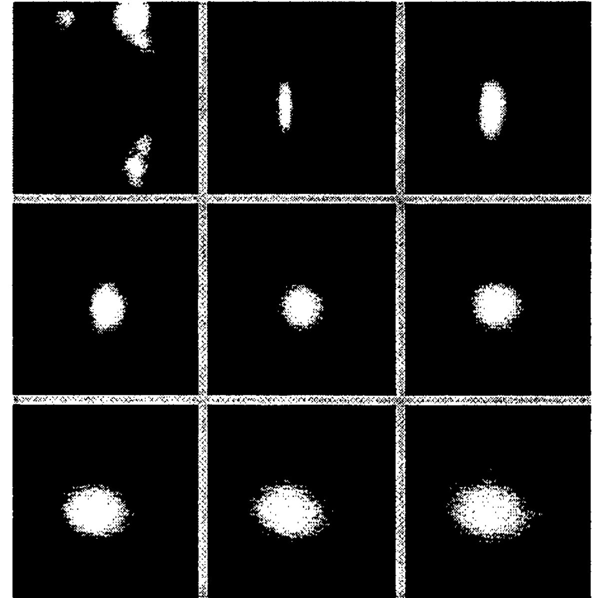

Fig. 2. Images of the beam propagation from the near-field to 7μm from the laser diode taken in 1μm steps. The top left image is the topography to provide the physical orientation for the laser emission images given in left to right sequence. All images are 6x6μm. The greyscale for each image is chosen to maximize contrast.

beam waist and astigmatism of high power strained (In,Ga)As quantum well lasers using the near-field tip to collect the output of the laser diode at various heights above the device facet.

The GRINSCH laser diode was mounted with its high reflecting mirror pointing up on a piezo actuated positioning stage and scanned beneath the probe of a near-field scanning optical microscope. Figure 1 is a series of high-resolution images of the laser mode intensity collected with the near-field probe as a function of height above the laser diode back facet. The laser is operated at a current of 100 mA. The first image was taken in the near-field ($z \sim$ 10nm). Each successive image is 1μm further from the facet with the last image at 7μm from the surface. As expected, the spreading of the beam is much faster in the vertical than the lateral dimension. The elliptical beam at the facet becomes a nearly circular beam at a height of 4μm. From this series of scans we determine the variation of the spot size of the mode along the optical axis. Figure 2 shows the spot size measurements as determined from the 1/e^2 intensity points of Gaussian fits to the measured beam profiles. The spot sizes in the lateral and vertical dimensions are shown by squares and circles, respectively. The position of the laser facet is set to the origin of the x-axis.

IV. Discussion

Previous studies of the astigmatism of these high power GRINSCH laser diodes found the devices typically have astigmatisms of 2-4 microns.[2] The far-field results find the lateral beam waist for the low reflecting facet occurring inside the device relative to the position of the vertical beam waist. With strong index guiding in the vertical dimension which is responsible for the vertical waist being fixed at the end of the heterojunction waveguide, the point at which the dielectric mirror stack begins, the lateral waist is expected to be inside the laser cavity.

Although these GRINSCH lasers were intended to be index guided in the lateral dimension, it was previously found that index guiding alone is not enough to confine the optical mode at high output powers. For a gain guided device, one expects to find the beam waist for both facets to occur inside of the device structure. However, carrier density inhomogeneity and temperature variations along the length of the cavity will probably result in different beam propagation parameters for the two output facets.[9]

Our NSOM studies of these devices have been mainly limited to studying the optical beam which exits the device through the high reflecting mirror due to difficulties probing the extremely high power density which exists at the low reflecting mirror facet. The continuous-wave power density on the output facet of the GRINSCH laser diodes is approximately 2 MW/cm^2. The NSOM tips are unable to probe this intense laser field. The high optical field damages the metal film of the NSOM probe which provides optical

confinement for the probe and hence the high resolution.

In an effort to reconcile the differences observed for the laser output from the two different mirror facets, we have begun to simulate focusing of the laser mode by an index variation across the mirror facet induced by the incident optical field. We have simulated the waveguide mode of the GRINSCH laser diode being focussed by the high reflecting dielectric stack due to a real index of refraction variation proportional to the local laser mode intensity. The focusing of the laser mode by a laterally graded index profile will have a more significant effect for the high reflecting facet due to the greater optical path length than that of the low reflecting facet.

In our model we stipulate that the beam focuses outside the cavity due to the heating of the dielectric mirror stack and consequently the variation in the refractive indices of the materials forming the stack. Such a graded index object might act as a thin lens and bend the phase front towards a focal point outside of the facet. We have applied the basic tools of Fourier optics to propagate the laser beam through the graded-index mirror and then in air.[10] It was assumed that the index variation due to heating is about the same shape as the mode, which is actually the source of the heating.

In figure 3 we compare the laser mode spot size along the optical axis as given by our simulation with the data collected by NSOM. The lateral beam spot size from the NSOM studies are plotted as squares while the simulation results are shown as triangles. For the simulation we required the initial waveguide mode have a spot size at the surface consistent with the NSOM data. Using the simulation, we tried to achieve a waist minimum at the same point along the optical axis at which the waist minimum is observed by the NSOM experiments. In order to achieve a focus at 4 microns from the laser facet, we see that the resultant beam has a smaller beam waist than found by NSOM. Of greater significance, a maximum in the index variation of 5% was necessary to achieve these results. Such a real refractive index variation requires facet temperatures an order of magnitude greater than is reasonably expected.

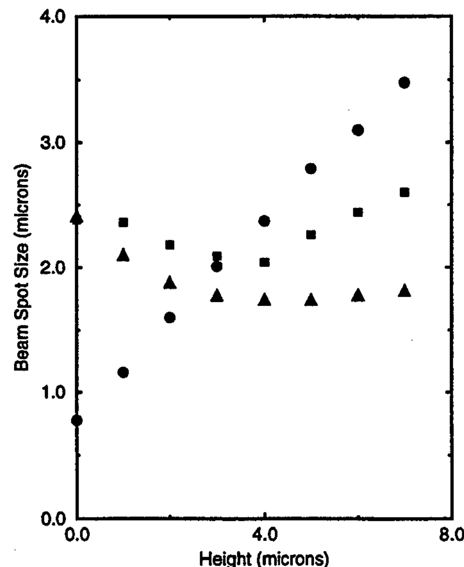

Fig. 3. Experimental measurements of the lateral (squares) and vertical (circles) spot size dependence on height above the laser diode facet. The spot sizes are determined by assuming and fitting a Gaussian distribution. Simulated data of the focusing effects of the graded index mirror facet are shown as triangles.

V. Conclusions

We have measured the position of the lateral beam waist of a GRINSCH laser diode for the high reflecting mirror facet by NSOM. Measurements made with this technique indicate the lateral beam waist is outside of the device structure, seemingly in contradiction to far-field measurements made on the low reflecting output facet of the device. Thermal lensing due to a temperature gradient across the mirror facet is incapable of generating the focusing required to explain the difference in observed beam waist position for the two separate measurements. In order to make a direct comparison with far-field results, we hope to obtain lateral beam waist measurements by NSOM for the low reflecting facet by driving the laser diode at very low duty cycles with pulse length significantly shorter than the heating cycle of the probe. Further simulations may be able to explain the apparent discrepancy if inhomogeneities in temperature or carrier concentration along the cavity are included.

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Scalable GM / I Based MOSFET Model

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1. Introduction

The continuing decrease of supply voltage to reduce power consumption of digital circuits strongly affects the design of the analog part of mixed analog/digital ICs. As a consequence, MOS transistors in analog circuits often operate in moderate inversion. Compact MOSFET models for deep sub-micron technologies therefore need to describe the full operating range from weak to strong inversion in a physical and continuous way. Scalability over the full range of available geometries is required without resorting to a large number of parameters or parameter "binning".

This paper describes a scalable and unified MOS transistor model based on the normalized transconductance-to-current characteristic, $g_{ms} \cdot V_t / I_D$, used in the 'EKV' model [1][2]. This approach describes the transistor behavior at different current levels from weak to moderate and strong inversion. The new features with respect to previous model versions are addressed here, in particular, a new universal mobility degradation model due to vertical field, reverse short-channel effect (RSCE), drain-induced barrier lowering (DIBL), and bias-dependent series resistance. The large-signal static model as well as the dynamic charges and thermal noise models are derived in a unified way and are valid in all modes of operation. The compact scalable model is a strong candidate for application to deep sub-micron technologies. It is efficient for parameter extraction and circuit simulation and, due to its continuity, alleviates convergence problems. A single set of as few as 25 process-related, intrinsic and extrinsic DC model parameters can be extracted for all geometries including short and narrow devices in a simple and straightforward sequence.

The drain current is derived under typical assumptions for charge-sheet models and includes drift and diffusion components [3] as well as major physical effects in a single equation:

$$I_D = I_S \cdot (i_f - i_r)$$

$$= \frac{2 \cdot n \cdot \mu_s \cdot C_{ox}' \cdot W_{eff} \cdot V_t^2}{L_{eff} - \Delta L + \delta_0 \mu_s V_{ds}' / v_{sat}} \cdot (i_f - i_r) \quad (1)$$

where μ_s is the surface mobility including vertical field dependence, C_{ox}' is the gate oxide capacitance, V_t is the thermal voltage, I_S is the specific current related to aspect ratio, i_f and i_r are symmetrical forward and reverse normalized currents [1], depending on $V_P - V_S$ and $V_P - V_D$, respectively, and n is the slope factor depending on V_P. The concept of the pinch-off voltage V_P [1], which is essentially a function of the gate voltage, is used to account for effects of doping concentration, such as threshold voltage, body effect, charge-sharing for short- and narrow-channel effects, RSCE, DIBL and non-uniform doping [4][5]. V_P represents the channel voltage at a given gate voltage for which the inversion charge density Q'_I in the channel becomes negligible with respect to the depletion charge density Q'_B. ΔL accounts for channel length modulation (CLM). Velocity saturation is handled similarly to [6]. The model is formulated symmetrically in terms of V_S and V_D and has a hierarchical structure. It also includes temperature effects and substrate current [7].

2. Long-Channel Model

A means of integration for the drain current is provided by the normalized conductance [1] $G(i) = g_{ms} V_t / I_D$ where $g_{ms} \equiv -\partial I_D / \partial V_S |_{V_G, V_D}$. A suitable function is needed to describe the behavior of $G(i)$ [1][8], with correct asymptotes, which are 1 in weak inversion and $1/\sqrt{i}$ in strong inversion, respectively. A simple and accurate analytical expression has recently been proposed [9]:

$$G(i) = \frac{g_{ms} V_t}{I_D} = \frac{di/dv}{i} = \frac{2}{1 + \sqrt{1 + 4i}} \quad (2)$$

Both (2) and the $g_{ms} \cdot V_t / I_D$ characteristic, calculated from the numerical solution of Poisson and Gauss equations under uniform doping and long-channel assumptions, are plotted in Fig. 1a, with respect to the normalized current $i_f \equiv I_D / I_S$ in saturation, and are found to match very well. The above numerical characteristic varies negligibly over a large range of doping levels and oxide thicknesses. The measured results from long-channel devices of three CMOS technologies, with minimum feature sizes ranging from 1 μm to 0.5 μm, are shown in Fig. 1b to match (2) very well from weak to strong inversion. For scaled deep sub-micron technologies, this characteristic is expected to remain sufficiently

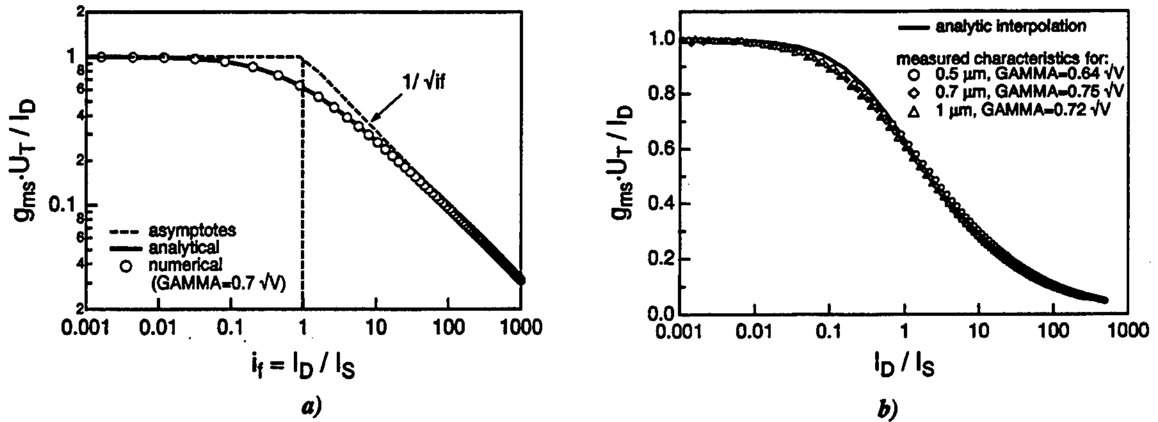

Fig. 1: *The normalized g_{ms}/I_D characteristics versus normalized current a) computed by numerically solving the Poisson equation for a long-channel device and interpolated by (2). b) measured on long n-channel devices for three different CMOS processes and analytical interpolation (2).*

unchanged and thus remain valid as a basis of this modeling approach. Integrating (2) yields the relation between normalized current i and voltage v:

$$v = \sqrt{1+4i} - 1 + \ln(\sqrt{1/4+i} - 1/2) \quad (3)$$

which unfortunately cannot be inverted analytically as would be required for the computation of i_f and i_r in (1). However a simple Newton-Raphson scheme allows an efficient inversion without loss of accuracy, such that the full drain current can now be expressed as a function of the terminal voltages.

If (2) is combined with the relationship between channel conductance and inversion charge density, $g_{mx}(V) = -\mu(x) \cdot Q'_I(V)$, where V is the channel potential at a given point x in the channel, the inversion charge density can be expressed as a function of the normalized current:

$$-Q_I'(x) = 2 \cdot n \cdot V_t \cdot C_{ox}' \cdot (\sqrt{1/4+i} - 1/2) \quad (4)$$

Integrating (4) allows us to formulate a consistent quasi-static charge/capacitance model. This approach has been used in the EKV model since the publication of [9], and has also been published in [10] recently. Thermal noise is simply proportional to the total inversion charge Q_I [1].

Using these derivations, the mobility reduction due to vertical effective field can be elegantly accounted for. A general expression for the localized mobility dependence on vertical field is given by:

$$\mu_s(x) = \mu_0 / \left[1 + \sum_k [E_{eff}(x)/E_k]^k\right] \quad (5)$$

where k is the order of effective field taken into account, and E_k is the kth-order parameter. The effective field dependence on inversion and depletion charge densities is commonly described by $E_{eff}(x) = |Q_B'(x) + \eta \cdot Q_I'(x)| / \varepsilon_0 \varepsilon_{si}$, where $\eta \approx 0.5$ for nMOS and $\eta \approx 0.3$ for pMOS [11] at room temperature. To account for the mobility reduction globally, (5) is interated along the channel:

$$\mu_s = \left[\int_0^L \frac{1}{\mu_s(x)} dx\right]^{-1} \quad (6)$$

$$= \mu_0 \int_0^L \left(1 + \sum_k \left[\frac{|Q_B'(x) + \eta \cdot Q_I'(x)|}{\varepsilon_0 \varepsilon_{si} E_k}\right]^k\right) dx$$

$$= \frac{\mu_0 L}{i_f - i_r} \int_{i_f}^{i_r} \left(1 + \sum_k \left[\frac{|Q_B'(i, V_P) + \eta \cdot Q_I'(i)|}{\varepsilon_0 \varepsilon_{si} E_k}\right]^k\right) di$$

Using the expressions for the charge densities $Q_I'(i)$ and $Q_B'(i, V_P)$ [1], this form can be easily integrated for any order of $k \geq 1$. To the authors' knowledge, this is the first time that such formulation was carried out. Integrating the 1st-order term yields

$$\mu_s = \mu_0 / \left[1 + \frac{|Q_B + \eta \cdot Q_I|}{\varepsilon_0 \varepsilon_{si} E_0 WL}\right] \quad (7)$$

For the purposes of this compact model, the 2nd-order model has been formulated and used. Unlike in other MOS models, the 2nd-order term used here represents the fully integrated form of the local effective field dependence.

Note that the above formulation also implies a dependence with the lateral field. The correlation between mobility reduction due to vertical field and velocity saturation [7] has to be carefully considered when formulating the global model (1) including both these effects.

The long-channel model described so far is valid and continuous among all operating regions, for static, dynamic and noise models. It needs now to be suitably complemented for short-channel effects.

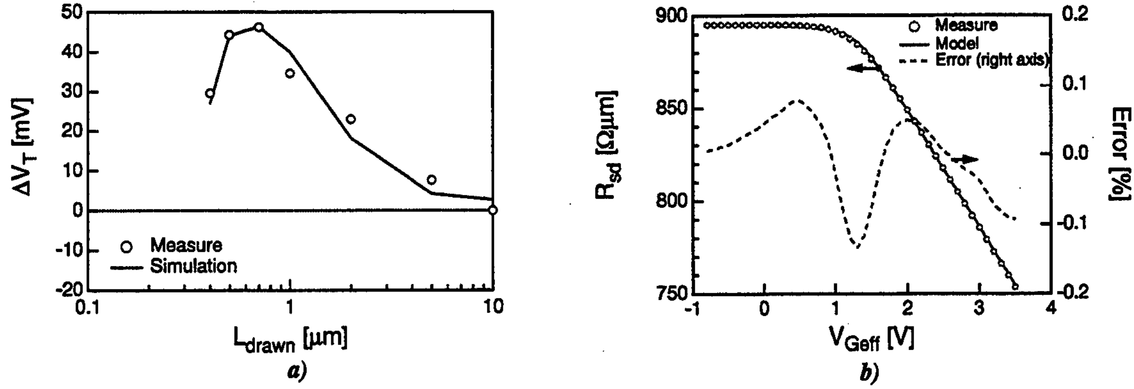

Fig. 2: *a) Variation of the threshold voltage with channel length due to RSCE for n-channel devices of a 0.5 µm standard CMOS process; b) gate bias dependence of series resistance [12] of a device from a 0.35 µm CMOS process.*

3. Short-Channel Model

Two short-channel effects, RSCE and DIBL, are included in the pinch-off voltage V_P [1] in addition to the charge-sharing concept to extend the model's range of applicability. Various models for RSCE have been proposed, and can be summarized as a correction either of substrate doping [12], or threshold voltage [13]. Both use CPU-expensive exponential terms, which also may lead to convergence problems during parameter extraction. A new simple yet accurate model is derived from [13], without the use of exponentials:

$$\Delta V_{fb_{RSCE}} = \frac{2 \cdot Q_0}{C_{ox}'} \cdot \left[1 + \frac{1}{2} \cdot \left(\xi + \sqrt{\xi^2 + 4 \cdot \varepsilon_1^2}\right)\right]^{-2} \quad (8)$$

where $\xi = C_1 \cdot (10 \cdot L_{eff}/L_k - 1)$, ε_1 and C_1 are constants. The parameters used are the peak charge density at the source/drain ends Q_0 and the characteristic length of charge distribution L_k. The current model for DIBL is a simplified form of [6]:

$$\Delta V_{fb_{DIBL}} = \sigma_0 \cdot (V_D - V_S) \cdot \left[\frac{\varepsilon_0 \varepsilon_{si}}{C_{ox}' \cdot L_{eff}}\right]^m \quad (9)$$

where σ_0 is the DIBL parameter and $m = 2$; it may be refined as discussed in [14]. The global threshold voltage is a superposition of the charge-sharing, RSCE and DIBL effects with geometry and bias [7], which can be strongly process-dependent. The threshold voltage variation as a function of drawn gate length is shown in Fig. 2a in the case of a 0.5 μm process displaying RSCE. Parameter extraction can follow the method of V_P vs. V_G measurement [4][5][15] at constant current.

Series resistance is a critical parameter for process engineering, device modeling and circuit design. Present CMOS technologies commonly use LDD structures with gate bias dependent resistivity. Although bias dependence of series resistance may decrease for very advanced technologies [16], even small variations may have a considerable effect on extracted channel length and series resistance. The existing models [12][17] typically use exponentials. The simple model for the bias dependent series resistance proposed in this paper avoids the use of exponentials without noticeable loss of accuracy,

$$R_{sd} = R_{sh0} \cdot \left[1 - \left(\frac{1}{2} \cdot r + \sqrt{r^2 + 4 \cdot \varepsilon_2^2}\right)\right] \quad (10)$$

where $r = S_{Vk} \cdot (V_{Geff}/V_k - 1)$, $V_{Geff} = V_G - V_{TO}$ is the effective gate voltage, and ε_2 is a constant. The parameters are sheet resistance R_{sh0} , characteristic voltage V_k and coefficient S_{Vk} . A comparison with the measured data [12] for a 0.35 μm process in Fig. 2b shows good agreement.

Note that if series resistance is to be explicitly accounted for in drain current and conductances, the following relations are used as discussed in [18]:

$$\frac{I_D}{I_{D0}} = \frac{g_m}{g_{m0}} = \frac{g_{ms}}{g_{ms0}} = \frac{g_d}{g_{d0}} \cong \frac{1}{1 + g_{ms0} R_S + g_{d0} R_D} \quad (11)$$

where the subscript '0' denotes current or conductances calculated without series resistance.

4. Results and Discussion

The new scalable model has been implemented as a compact model in the Eldo™ circuit simulator. The scaling performance with channel length is illustrated for a 0.5 μm process in Fig. 2a, where the simulated equivalent threshold voltage is shown to match the experimental data with a small maximum error of 6 mV, for drawn channel lengths ranging from 0.4 μm to 10 μm . For the same technology, the measured and simulated I_D vs. V_G characteristics in saturation for different V_S are compared in Fig. 3 for three different channel lengths. The fit is excellent for all channel lengths from weak to strong inversion. Fig. 3 also presents the output characteris-

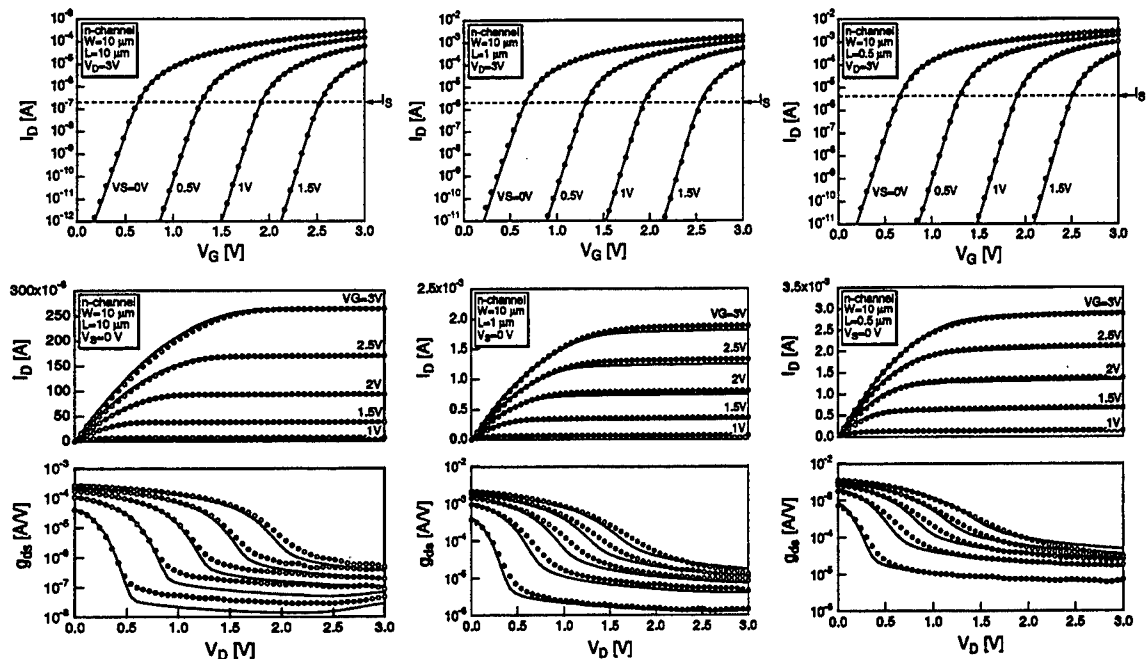

Fig. 3: *Comparison of measured (o) and simulated (-) characteristics I_D vs. V_G at different V_S; I_D and g_{ds} vs. V_D at different V_G. for n-channel devices of a 0.5 µm standard CMOS process, for long (L=10 µm), intermediate (L=1 µm) and short (L=0.5 µm) drawn channel lengths respectively.*

tics I_D and g_{ds} vs. V_D at different V_G. The output conductance g_{ds} is continuous and well modeled for all geometries both in conduction and saturation. These figures demonstrate the continuity among all operating regimes and the model's scalability, since a single parameter set has been used for all devices.

5. Conclusions

In summary, a unified, physical and scalable compact MOS transistor model based on a simple but accurate interpolation of the normalized g_{ms}/I_D characteristic has been presented. The model is symmetric and has a hierarchical structure. The long-channel static model, including mobility effects, the dynamic charge model as well as thermal noise model are derived in a unified and continuous way, valid from weak to strong inversion and from linear to saturation regions. Short-channel effects, such as RSCE and bias dependent series resistance, are included in the model to achieve scalability, and are formulated in an adequate and efficient way for parameter extraction and circuit simulation. Experimental results demonstrate the model's scalability for a 0.5 µm CMOS process using a single set of no more than 25 intrinsic and extrinsic DC parameters. The model is well suited for deep sub-micron analog and mixed-mode IC design.

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COMPLEMENTARY HETEROSTRUCTURE FIELD EFFECT TRANSISTOR MODELS FOR MIXED MODE APPLICATIONS

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INTRODUCTION

Recent applications of complementary heterostructure field effect transistor (CHFET) technology to wireless systems require new device models for *n*-channel and *p*-channel submicron devices, to allow designers to simulate digital, microwave, and mixed mode circuits. Here, we describe a new model for CHFETs, which, for the first time, allows us to accurately simulate the device characteristics of both *n*- and *p*-channel HFETs over the temperature range 250-450 K. Modeling in a wide temperature range is very important, since it allows us to account for the changes in the device characteristics with self-heating and accurately estimate power consumption of integrated circuits, which is crucial for wireless applications.

The present model accurately reproduces above-threshold and subthreshold characteristics of both *n*- and *p*-channel HFETs fabricated in different laboratories over the temperature range indicated. The current-voltage characteristics are described by a single, continuous, analytical expression for all regimes of operation, thereby improving the convergence properties of circuit simulations. Our physics-based model incorporates the following features:

* Drain induced barrier lowering.
* Velocity saturation, and finite output conductance in saturation.
* Subthreshold leakage modeling.
* Gate leakage current, including hot-carrier effects.
* Modeling of near-threshold operation.

These features were included earlier [1], [2]. The new features of our improved HFET model include:

* Temperature dependent model parameters.
* Frequency dispersion.
* Accurate modeling of output resistance and of differential, benchmark quantities such as g_m/I_d and g_d.
* Accurate modeling of microwave HFET *S*-parameters.

Also, the gate current leakage model has been further improved compared to that described in [1], [3].

We incorporated this model into the circuit simulator AIM-Spice [1], [2] (see http://www.aimspice.com/) for the simulation of mixed mode CHFET integrated circuits. All the equations of the model and parameter definitions are available on line via AIM-Spice help. An automatic parameter extraction routine has also been developed (see http://www.aimspice.com/ for details.)

Modeling Approach

Numerical simulations have shown that for HFETs, the sheet density of channel carriers can be accurately described in terms of the unified charge control model (UCCM) for all regimes of operation [4]. Based on the UCCM, precise

expressions are derived for the drain current in subthreshold, above-threshold linear and above-threshold saturation regimes, which can be combined into a universal FET drain current expression [1], [2], [5]. At sufficiently large gate bias, we also account for the transfer of charge carriers into the wide bandgap barrier layer, an effect that causes a saturation of the channel sheet carrier density and of the saturation current. (A concomitant increase in the carrier population of the wide bandgap layer contributes to the total gate capacitance.)

Our model also includes a precise model for the gate leakage current, including the effects of hot carriers near drain. For enhancement-mode HFETs, the gate current is of great concern since it degrades the *I–V* characteristics and the transconductance.

The HFET gate can be represented by a series combination of two diodes, one for the Schottky barrier and the other for the heterojunction, as shown in the equivalent HFET circuit of Fig. 1. This model can be further improved by using different electron temperatures at the source and the drain sides of the channel.

Measured and simulated characteristics of 0.7 μm *n*- and *p*-channel δ-doped HFETs fabricated by Honeywell Corp. are shown in Fig. 2a to d. The structure of both devices is as follows: Intrinsic GaAs cap layer: 30 Å, intrinsic AlGaAs barrier: 250 Å (Al mole fraction = 0.75), intrinsic GaAs spacer: 30 Å, intrinsic InGaAs channel: 150 Å (In mole fraction = 0.25), intrinsic GaAs buffer layer: 5000 Å. The threshold voltages are: 0.35 V (*n*-channel HFET) and –0.4 V (*p*-channel HFET.)

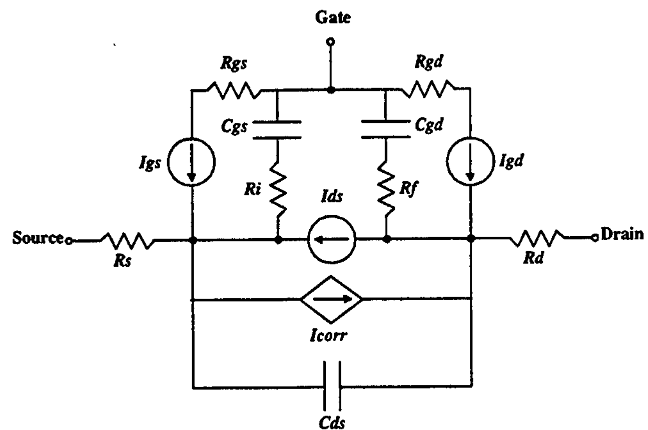

Fig. 1. HFET equivalent circuit including gate leakage.

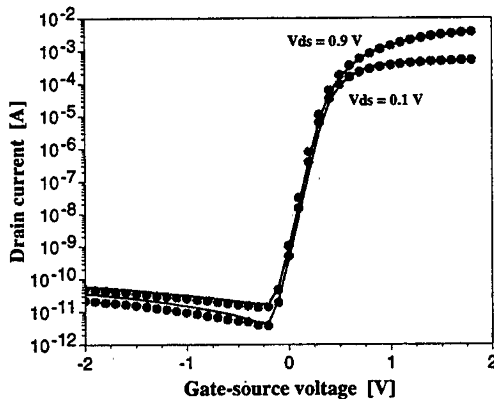

Fig. 2a. Measured (symbols) and modeled (lines) subthreshold characteristics of a 0.7 μm *n*-channel HFET from Honeywell.

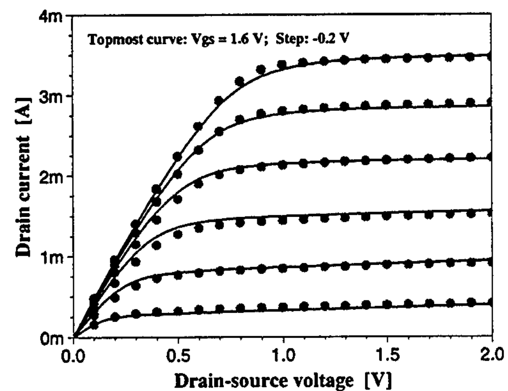

Fig. 2b. Measured (symbols) and modeled (lines) above-threshold characteristics of the same device as in Fig. 2a.

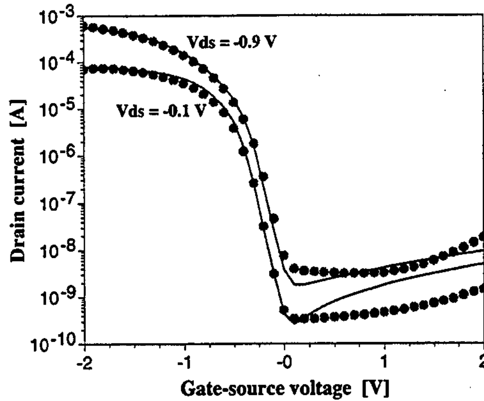

Fig. 2c. Measured (symbols) and modeled (lines) subthreshold characteristics of a 0.7 μm *p*-channel HFET from Honeywell.

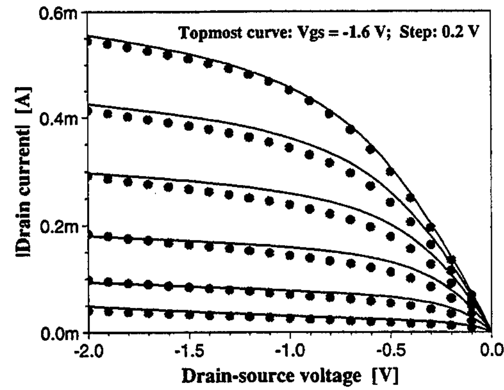

Fig. 2d. Measured (symbols) and modeled (lines) subthreshold characteristics of the same device as in Fig. 2c.

We observe an excellent agreement between measured and simulated characteristics in all regimes of operation, including the near-threshold regime, which is of particular importance in low-power operation. The deep subthreshold leakage current, shown as a low-level saturation of the subthreshold current, is related to the gate leakage. A reliable subthreshold current model is needed for simulation of standby power consumption in digital circuits.

The increased gate current caused by hot-electron emission at high drain voltage, observed in some HFET structures [3], can also be precisely modeled, as shown in Fig. 3.

Accurate simulation of analog HFET circuits, including microwave circuits, requires not only a good reproduction of *I–V* and *C–V* characteristics, but also a good description of differential quantities such as transconductance g_m and output conductance g_d, including frequency dispersion and geometry dependent effects. In the modeling of high-frequency *S*-parameters, these issues are particularly important. For example, S_{22} is closely related to g_d, while S_{21} is linked to both g_m and g_d. Examples of microwave HFET *S*-parameter modeling are shown in Fig. 4a to c.

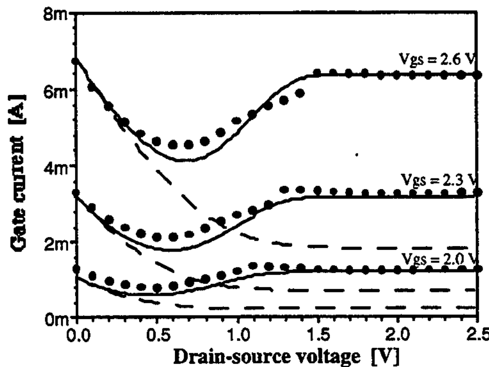

Fig. 3. Measured (symbols) and simulated gate current (solid lines) versus V_{ds} for a 0.8 μm long, 10 μm wide HFET. Dashed lines correspond to simulation results with the hot-carrier effect disabled in the model.

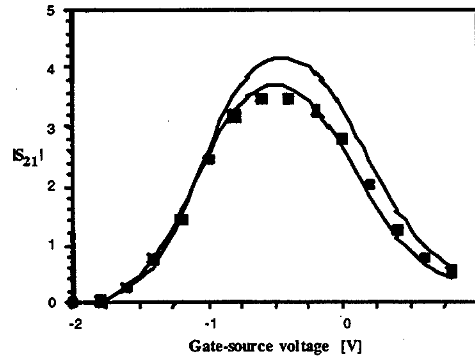

Fig. 4a. Measured (symbols) and simulated (solid lines) magnitude of S_{21} versus gate-source voltage at 1 GHz for a 0.3 μm long and 500 μm wide microwave HFET from Motorola Inc. biased in saturation. Lower and upper curves are simulations with and without inclusion of frequency dependence of g_d.

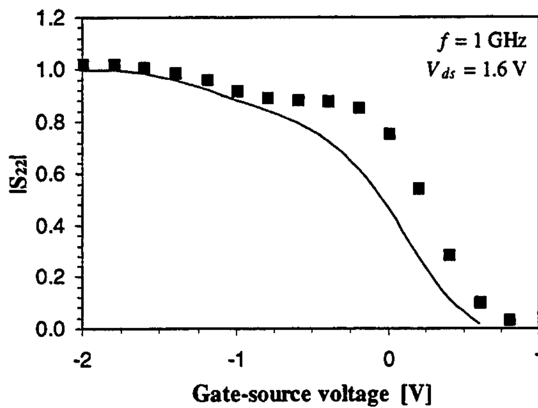

Fig. 4b. Measured (symbols) and simulated (solid lines) magnitude of S_{22} versus gate-source voltage of the same device as in Fig 4a.

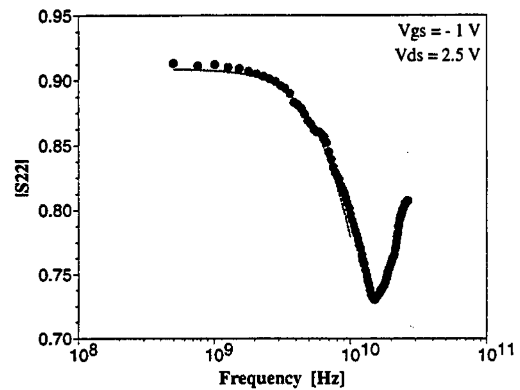

Fig. 4c. Measured (symbols) and simulated (solid lines) magnitude of S_{22} in the frequency range 500 MHz to 30 GHz for a 1 µm long and 100 µm wide microwave HFET from Motorola Inc. biased in the saturation regime.

CONCLUSIONS

We have presented an enhanced model for complementary heterostructure field effect transistors for use in mixed mode applications. The model has been implemented in the circuit simulator AIM-Spice. Specifically, we compared our new model with experimental *I–V* characteristics, gate leakage current, and *S*-parameters, and demonstrated a very good accuracy. A more comprehensive discussion of this HFET model will be published elsewhere [6]

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Ultra-Thin-Body Silicon-On-Insulator MOSFET's for Terabit-Scale Integration

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1. Introduction

Over the entire past two decades, physical gate length of CMOS transistor has been steadily reduced simply driven by the desire for IC performance and packing density. The industry is now confident that the transistor scaling down will continue until a physical gate length of 50nm is reached. However, it is still unclear whether further device shrinkage is feasible from the viewpoints of both device physics and process fabrication. This paper addresses the MOSFET architecture design - the major challenge for terabit-scale integration.

At a minimum feature size of 25nm, defining gate, contact, and silicide will be extremely challenging and innovative technical approach needs to be proposed. Meanwhile, in the effort to suppress the short-channel effects, either lateral channel doping engineering (pocket or halo implant) or vertical well doping engineering (retrograded-doping or δ-doping) will become much more difficult as the device dimensions decrease. From a comparative study of advanced MOSFET concepts [1], it is concluded that two approaches are capable of achieving 25nm physical-gate-length MOS devices without excessive DIBL, V_{th} roll-off, and subsurface punchthrough. The first is a SOI MOSFET with an ultra-thin-body (<10nm) (in the active channel region only) and the second is a double-gated MOSFET with <20nm silicon thickness which may take the form of planar, vertical, or surrounding-gate structures. The unique feature in both device architectures is that the gate (front and back)-to-channel distance must be no thicker that $L_{gate}/4$ in order to make the gate dominate over the drain in the fight for control over the carrier flow. The major challenges in designing these devices will be (1) how to effectively suppress the short-channel effects and (2) how to overcome the dopant number fluctuation in devices with such an extremely small body volume.

2. Device Structure

2.1 Sub-Lithographic Technique and Self-Limiting Recess-Channel Process

The schematic cross-section of the ultra-thin-body SOI MOSFET is shown in Fig.1. The ultra-thin silicon body is proposed to be fabricated by a self-limiting LOCOS recess-channel process [2] and the gate electrode is self-aligned to the body (Fig.2). The ultra-thin-body eliminates the punchthrough path and avoids the complicated channel or well doping profile engineering in the nanometer-scale devices. The relatively thicker source and drain regions are designed to reduce the series resistance which is one of the major challenges in implementing thin-film fully-depleted SOI MOSFET's.

The 25nm-length gate electrode, contact vias and silicide are proposed to be achieved by sub-lithographic techniques, such as photoresist ashing or metal-induced-lateral-crystallization, well before the photo lithography capability at these dimensions becomes widely available. Though the accurate control of SOI film thickness is a major process challenge, recent research work at NTT Lab demonstrated that the local uniformity of SOI film thickness is quite acceptable since the device dimension is far smaller than the SOI film thickness undulation period (~1μm).

2.2 Suppressing Dopant Number Fluctuation

One often-cited CMOS transistor scaling limitation is that the body doping concentration cannot exceed $N_{sub}=2\times10^{18}$ cm^{-3}, if excessive junction leakage is to be avoided. This leaves only 20 dopant ions in the depletion region of a 25nm device. Large fractional fluctuations in the depletion charge Q_B and therefore large fractional fluctuation in threshold voltage could be a serious problem because

$$V_{th} = \Phi_{FB} + 2\phi_B + Q_B / C_{ox}$$

where the first two terms on the right-side add to approximately zero for both n^+ gate n-MOSFET and p^+ gate p-MOSFET, leaving $V_{th} \sim Q_B$. A dramatic solution to this perceived scaling limitation is proposed by using a near-intrinsically-doped body ($<1x10^{15}cm^{-3}$) so that the contribution of Q_B to V_{th} is quite negligible. V_{th} will then be adjusted by the gate work function rather than by modifying the body doping concentration. The gate work function engineering provides another degree of freedom in the V_{th} control. On the other hand, low body doping concentration is also beneficial for both mobility and leakage.

3. Result and Discussion

The device simulation is performed with the aid of Silvaco 2D simulator. The studied device has dimensions of T_{ox}=2~4nm, T_{si}= 2.5~10nm, and T_{box}=50~100nm. The doping concentration in the body is $5x10^{14}cm^{-3}$. A 20A gate oxide is used for best performance without unacceptable tunneling leakage. Non-stationary carrier transport effect such as velocity overshoot and non-local impact ionization is included by solving energy-balance equation simultaneously with the Poisson equation and the carrier continuity equations.

3.1 Threshold Voltage Adjustment By Poly-$Si_{1-x}Ge_x$ Gate Work Function Engineering

The threshold voltage is adjusted by varying the Ge mole fraction in the poly-$Si_{1-x}Ge_x$ gate. For n-channel MOSFET, the threshold voltage shifts by ~150mV merely from the ϕ_{ms} variation at a Ge mole fraction of x=0.2 [4], which is adequate for V_{th} adjustment in the nanometer-scale MOS devices (Fig.3). For the near-intrinsically-doped body, p-type doped poly-$Si_{1-x}Ge_x$ gate is needed for n-MOSFET while n-type poly-$Si_{1-x}Ge_x$ gate is needed for p-MOSFET. Innovative process technique will be therefore demanded for the reversed gate doping.

3.2 Electrical Performance of MOS Transistor

At room temperature (300°K) the ultra-thin-body SOI n-MOSFET with a body thickness T_{si}=2.5nm delivers a drive current of ~0.68mA/μm and a transconductance of 0.2S/mm at a supply voltage of V_{dd}=1V (Fig.4). No obvious impact ionization is observed even at V_{ds}=1V attributed to the non-local effect. The worse-case subthreshold swing is 74mV/dec at a supply voltage of V_{dd}=1V. For a 25nm-wide device, the MOSFET off-state leakage current is <0.1pA (Fig.5). With a SOI film thickness of T_{si}<5nm, subthreshold swing and DIBL are quite satisfactory despite the ultra-short channel length (Fig.6,7). At a SOI film thickness of T_{si}=10nm, MOSFET current drive I_{dsat} is improved by 30% but subthreshold swing is degraded due to the subsurface punchthrough effect (Fig.8,9). It is also demonstrated that the utilization of near-intrinsically-doped body minimizes the dopant number fluctuation effect. Source and drain series resistance degrades both on and off performance therefore needs to to be minimized (Fig.10). It is demonstrated from the 2D electron flux density contour that punchthrough effect is successfully eliminated in a 2.5nm-thick ultra-thin-body SOI device (Fig.11).

4. Conclusion

For the first time, the possibility of achieving 25nm physical-gate-length MOSFET is demonstrated with 2D numerical simulation. The MOS transistor, featuring an ultra-thin body (2.5~10nm) and thicker source and drain regions, is proposed to be implemented by sub-lithographic technique and self-limiting LOCOS recess-channel process. The near-intrinsically-doped body avoids the dopant number fluctuation effect which imposes limit on transistor scaling. Threshold voltage is adjusted only by the work function engineering by applying poly-$Si_{1-x}Ge_x$ as the gate material. The 25nm MOS device demonstrates excellent on and off performance under a supply voltage of 1V. Punchthrough is successfully eliminated in the ultra-thin body.

Acknowledgment

The research was supported by the DARPA contract under the Advanced Microelectronics Program and the Air Force JSEP Program.

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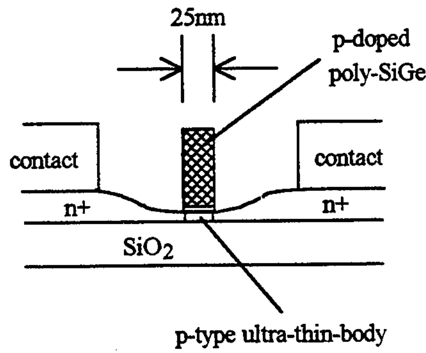


Fig.1 Schematic cross-section of ultra-thin-body (UTB) SOI MOSFET. The 25nm physical gate length is defined by sub-lithographic technique.

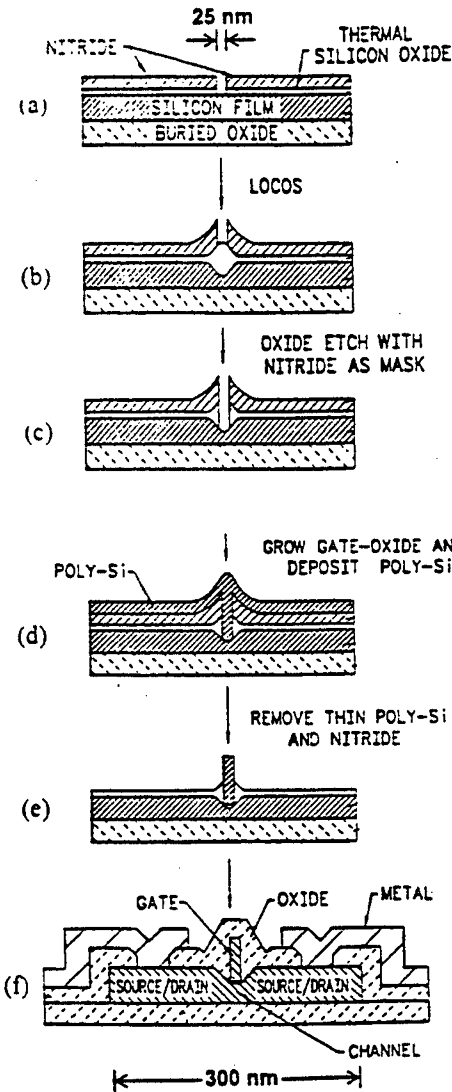
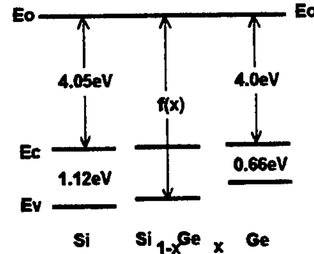
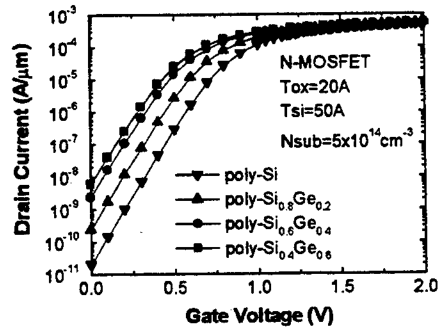


Fig.2 Self-aligned LOCOS recess-channel process for implementing UTB SOI MOSFET.





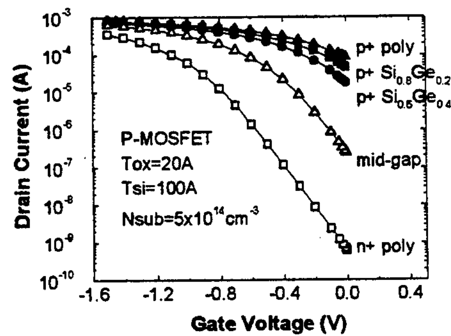


Fig.3 (a): Band structure of Si, Ge, and poly-$Si_{1-x}Ge_x$. (b) & (c): CMOS FET V_{th} adjustment by changing the Ge mole fraction x in the poly-$Si_{1-x}Ge_x$ gate.

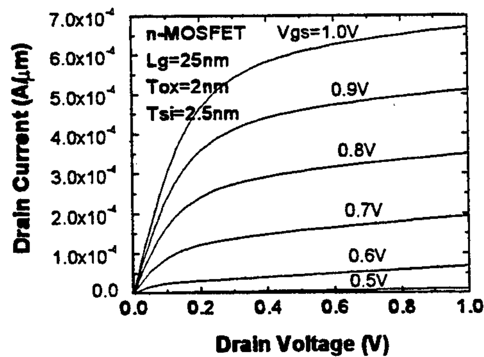


Fig.4 UTB SOI device I_{ds}-V_{ds} characteristics. L_g=25nm, T_{ox}=2nm, T_{si}=2.5nm. Velocity overshoot and non-local impact ionization effects are included.

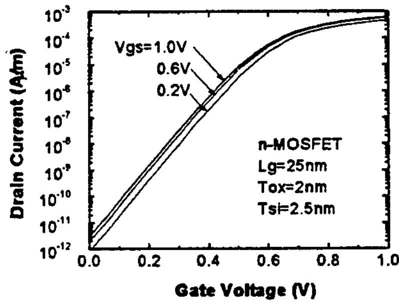


Fig.5 UTB SOI device I_{ds}-V_{gs} characteristics. L_g=25nm, T_{ox}=2nm, T_{si}=2.5nm.

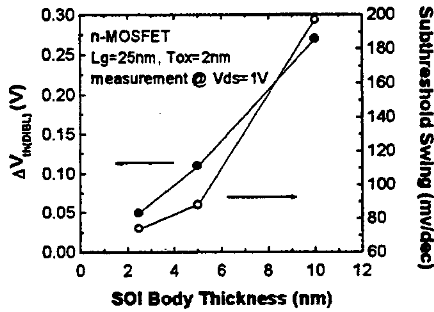


Fig.6 Impact of T_{si} on $\Delta V_{th(DIBL)}$ and subthreshold swing. The swing is measured @V_{ds}=1V.

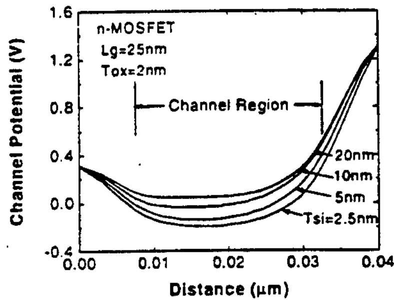


Fig.7 Channel potential with T_{si} as variable.

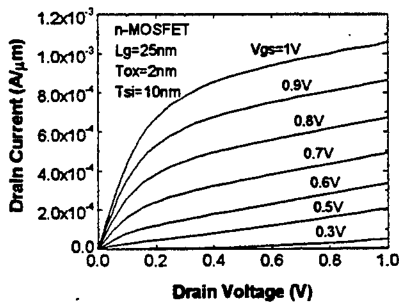


Fig.8 UTB SOI device I_{ds}-V_{ds} characteristics. L_g=25nm, T_{ox}=2nm, T_{si}=10nm.

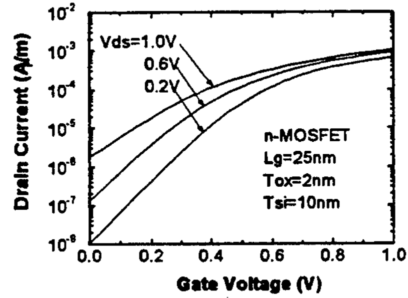


Fig.9 UTB SOI device I_{ds}-V_{gs} characteristics. L_g=25nm, T_{ox}=2nm, T_{si}=10nm.

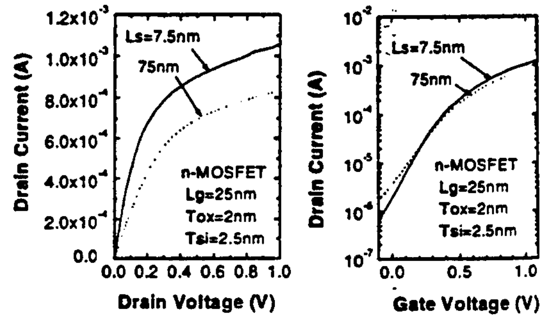


Fig.10 Impact of source and drain series resistance on (a) I_{ds}-V_{ds} and (b) I_{ds}-V_{gs} performance of UTB SOI MOSFET.

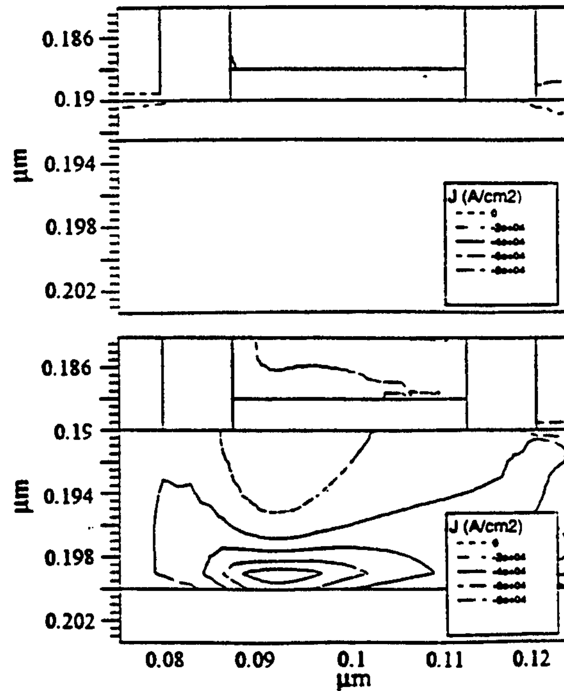


Fig.11 Carrier flux density contour at V_{dd}=1V and V_{gs}=0V for (a) T_{si}=2.5nm and (b) T_{si}=10nm UTB SOI MOSFET with noticeable leakage in the latter case but none in the former.

SIMOX SUBSTRATES AND MOSFET's FOR ENHANCED RELIABILITY AND PERFORMANCE

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Silicon on Insulator technology (SOI), and in particular Fully-Depleted (FD) SOI technology is emerging as the technology of choice for deep submicron CMOS and Low-Power Low-Voltage (LPLV) microelectronics and VLSI. SIMOX (Separation by IMplantation of OXygen) and the various forms of wafer bonding are currently the two main methods of SOI substrate preparation, SIMOX been the one considered by many to be the most well developed yet. Regarding the SIMOX quality, it is well known that excess silicon exists in the buried oxide (BOX) of SIMOX wafers, and that its presence introduces a variety of carrier traps at increased densities, as compared to thermal SiO_2. Regarding the SOI MOSFET design, two kinds of FD devices are in use, with corresponding advantages and shortcomings: inversion mode and accumulation mode SOI MOSFET's. In the present paper work aimed at improving the BOX quality and a new "mixed " mode FD SOI MOSFET are described, which should improve the reliability and performance of SOI technology.

To improve the BOX quality, a supplemental oxygen implantation [1] has been applied to finished SIMOX wafers for the reduction of excess Si in the BOX. Previous results from UV and VUV electron injection studies [2], and x-ray irradiation cryogenic detrapping studies [1] on SIMOX supplemental versus control wafers have indicated a reduction in both electron and hole trap levels for supplemental material. The difficulty in performing hole injection on SIMOX material has previously allowed only x-ray radiation work to study net hole trapping behavior of the BOX. The work presented here uses the recently discovered opposite channel based charge injection technique [3] which makes it now possible to inject "pure" hole pulses into the buried oxide, and thus to study the hole traps. Standard single implant as well as multiple implant thick SIMOX wafers (single: $1.8x10^{18}cm^{-2}$, 200 keV implanted at 600^0C and annealed at 1310^0C for 5 hr in Ar + 0.5% O_2; multiple 0.5 + 0.5) were implanted by an additional (supplemental) oxygen dose in the range $1\text{-}5x10^{17}cm^{-2}$ (with all the other conditions the same), followed by 1 hr annealing at 1000^0C. Following this, simple, relaxed geometry MOSFET's were fabricated for the measurements. For comparison, control MOSFET's were also fabricated in SIMOX wafers without supplemental oxygen.

Fig.1 shows a typical schematic set-up and bias levels to achieve hole injection into the buried oxide. By turning the opposite (front) channel [3], pure hole injection into the BOX can be achieved under appropriate stress conditions, as seen by the PISCES simulations of the injection currents in Fig.2. The resulting hole trapping was studied by monitoring the back gate threshold voltage shift (reduction) $V_{T2}(t)$ as a function of injection time. The results for a multiple implant sample are shown in Fig.3 for a period of hole injection equal to about 2000 seconds, while Fig.4 shows similar plots for a much longer period. It is seen that the density of both types of traps, i.e. those with a large hole capture cross section (controlling the initial part of the trapping curves, Fig.3), as well as those with a small hole capture cross section (Fig.4), is substantially reduced by the supplemental oxygen implantation.

From these results it is seen that the supplemental oxygen implantation process appears to reduce the densities of both types of hole traps, suggesting that they are related to excess silicon in BOX. The results point to the same direction as those on electron trapping described in [2].In both cases, supplemental oxygen implantation into SIMOX structures appears to remove the excess silicon, distributed in the form of small clusters over the buried oxide layer, and larger silicon clusters located near the Si/BOX interface. Opposite channel injection can also be used to study the electron traps by appropriately biasing the device so as to cause pure electron injection [3].

With regard to SOI devices, fully-depleted (FD) MOSFET's are considered by many as a very promising approach for high speed and low power applications, with simpler processing than partially

depleted SOI. However, because of the very thin silicon films involved rather high doping levels are required in order to achieve acceptable values of the threshold voltage in conventional inversion mode (INV) devices, which leads to substantial mobility (thus transconductance) degradation [4]. Since accumulation mode (ACC) devices do not suffer from this problem, there has recently been a considerable effort to explore them as a viable alternative to INV technology [5]. However, accumulation mode devices are not free from floating body related SOI device problems (which are better known to occur in inversion mode devices), such as early breakdown and single transistor latch-up, as it might at first be excepted [6]. In fact, the latch up voltage (V_{DLU}) of the accumulation mode devices (especially for shorter channels) tends to be lower than comparable inversion mode devices [7]. There is thus a trade-off between performance (i.e. transconductance) and latch up voltage (breakdown) with accumulation mode devices leading to better performance and inversion mode devices to higher breakdown voltages. In this paper, a new device is designed and analyzed, which combines the advantages of both the inversion mode and the accumulation mode devices: its performance is better than the inversion mode device, and its breakdown voltage higher than the accumulation mode device. Additionally, the new device results in better hot carrier reliability.

Fig.5 shows that the electrostatic potential in a typical accumulation mode structure biased near breakdown favors the accumulation of impact-generated holes near the corner of the source, body and buried oxide along the back interface. Following [6], if enough holes are generated, an inversion layer will form along the back interface, which will act as the p-type base of the parasitic bipolar "transistor". The situation becomes just like in the more conventional inversion mode case, except that because the p-type inversion layer is very thin, it is more difficult for the holes to move out of the body, into the source and recombine. It is thus interesting to see if this "hole removal" process can be accelerated by converting a thin section of the film along the back interface into p-type. A schematic illustration of the resulting structure is shown in Fig.6; this is a mixed accumulation/inversion mode (MIX) structure in the sense that the front channel is accumulation channel whereas the back channel is inversion channel.

To check out this idea numerical simulations have been carried out for the three structures, using the following parameters: L=0.8 m , t_{ox1}=20nm, t_{Si}=100nm, t_{ox2}=400nm. The channel doping (chosen for similar threshold voltages) was $N_D=1x10^{15}$ cm^{-3} (ACC), $N_A=2x10^{16}$ cm^{-3} (INV), and $N_D=2x10^{16}cm^{-3}$, t_{nSi}=70nm, $N_A=8x10^{16}cm^{-3}$, t_{pSi}=30nm (MIX). Fig.7 compares the transconductance characteristics of the three structures. It is seen that for the case in hand the transconductance of the MIX device is about 30% higher than that of the INV device. Fig.8 compares the latch up and breakdown voltages of the three devices. The latch-up voltages are 4, 5.5 and 7.2V (at I_D=1 A / m) and the breakdown voltages 9, 10 and 10.7V (at I_D=1mA/ m), for the ACC, MIX and INV device respectively. It can also be seen from Fig.7 that there is over an order of magnitude improvement in the MIX leakage current as compared to ACC. Fig.9 compares the electric fields of the three structures, which turn out to be in agreement with the results on performance (Fig.7) and breakdown (Fig.8). Finally the three structures were compared in terms of hot carrier reliability by calculating the hot electron (I_e) and hot hole (I_h) injection currents into front (1) and back (2) oxide. It is seen from TABLE I that I_{e1}, I_{h1}, I_{h2} are highest for INV and I_{e2} for ACC, in fair agreement with experiments [7], [8], and that overall the injection currents are lowest for MIX. More detailed combined SUPREM/PISCES calculations are currently in progress for fine-tuning this new structure and obtain the most appropriate structural parameters and doping profiles.

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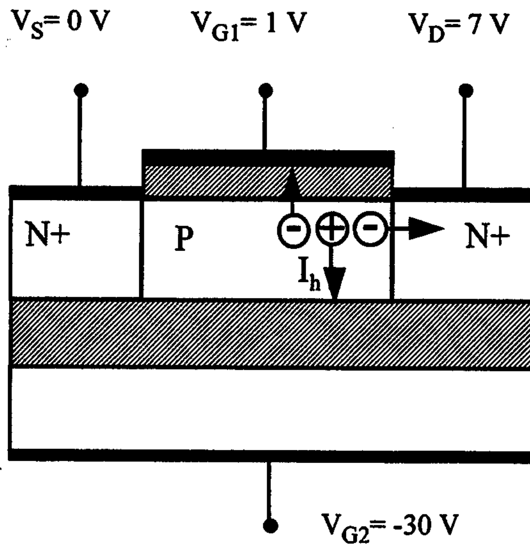

Fig. 1: Schematic set-up and bias levels of SOI-MOSFET for pure hole injection into the Buried Oxide (BOX).

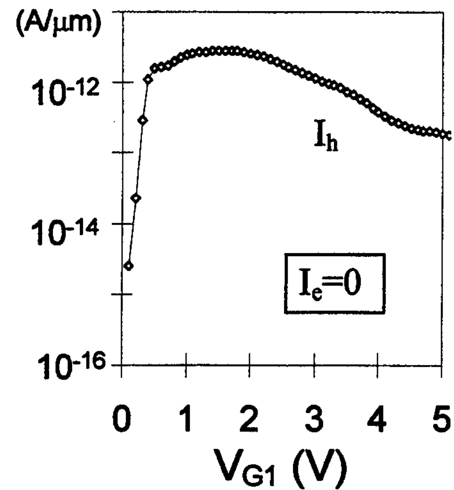

Fig. 2: Simulation of the pure hole injection current I_h as a function of V_{G1}. The corresponding electron injection current I_e into the BOX is practically zero. Injection conditions: V_S=0V, V_D=7V, V_{G2}=-30V.

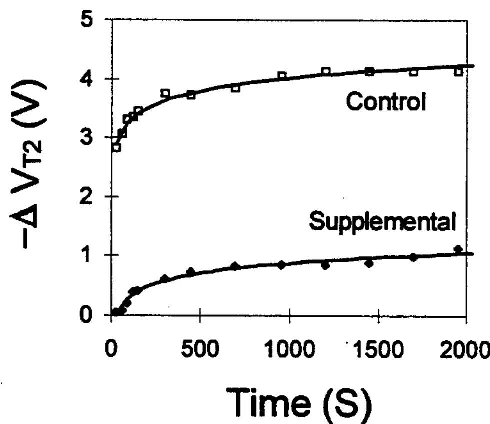

Fig. 3: Back threshold voltage shift (negative) $\Delta V_{T2}(t)$ as a function of time, for a relatively short time period. V_{T2} is the the voltage at which the drain current is equal to 1μA/μm for V_S=0V, V_D=0.1V and V_{G1}=-2V.

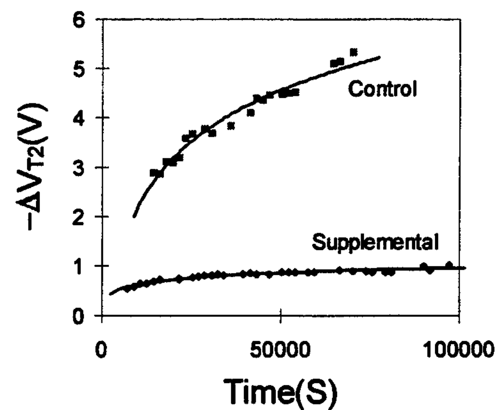

Fig. 4: Back threshold voltage shift, (negative) $\Delta V_{T2}(t)$ as a function of time, for a long time period. V_{T2} defined as in Fig.3.

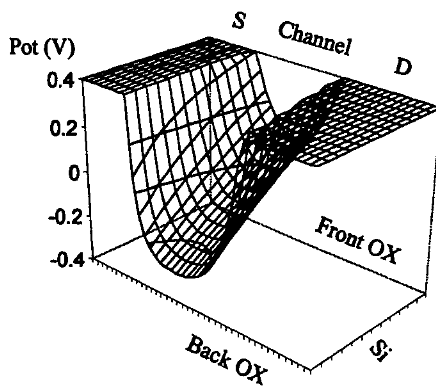

Fig. 5: Potential profile in accumulation mode device. V_{DS}=3V, V_{G1}=V_{G2}=0V.

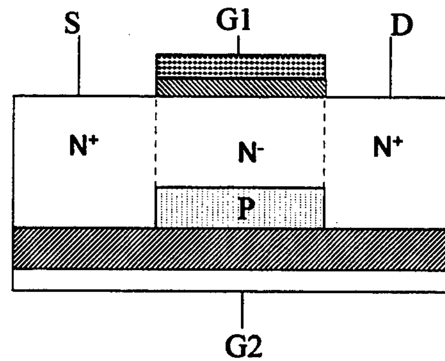

Fig. 6: Schematic diagram of the new mixed mode SOI MOSFET (not to scale).

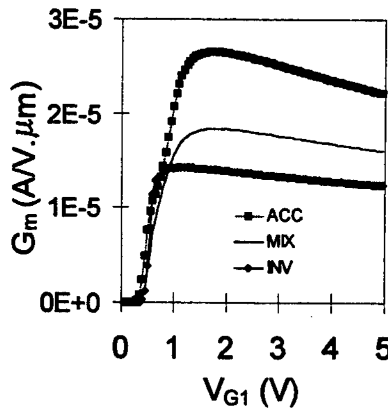

Fig. 7: Transconductance vs. gate bias at V_D=0.1V for the three devices.

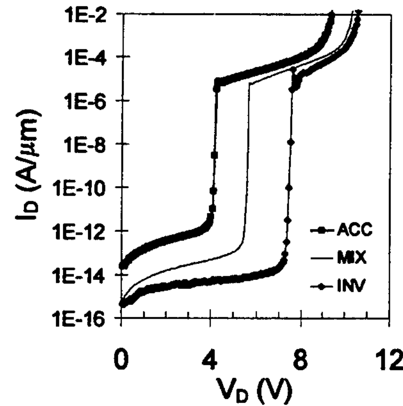

Fig. 8: Latch-up, breakdown and leakage current for the three devices with both gates grounded.

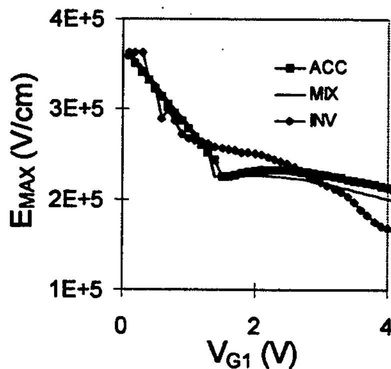

Fig. 9: Maximum lateral electric field at V_D=3V for the three devices as a function of gate bias.

	ACC	INV	MIX
Ie1	1.86E-16	1.08E-12	1.84E-16
Ie2	1.03E-14	3.86E-16	3.55E-15
Ih1	6.10E-17	1.33E-17	2.83E-17
Ih2	2.37E-18	3.30E-19	8.24E-19

TABLE I: Hot electron/hole injection currents (A/µm) into the front (1) and back (2) oxides for the three devices, at V_D=4V, V_{G1}=3V and V_{G2}=0V.

SELF-HEATING IN SOI MOSFETS AND THE EXTRACTION OF ISOTHERMAL CHARACTERISTICS FROM SMALL-SIGNAL MEASUREMENTS

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1. Introduction

The self-heating effect in SOI MOSFETs, is one of the problems indigenous to SOI technology. This effect is due to the inability of the buried oxide to dissipate the heat in the channel as efficiently as bulk Si, which results in negative output conductance in the DC IV characteristics of the device, and complex frequency behavior, where the thermal and electrical contributions are hard to distinguish [1][2][3].

The thermal effects are important whenever the channel temperature varies significantly on the time scale of the applied signal, in which case the instantaneous channel temperature is determined by a dynamic thermal model.The difficult task encountered then, is that of accurately extracting the isothermal characteristics from practical measurements. Some techniques have been developed to avoid this problem by extracting the isothermal electrical response from AC conductance measurements [2]. Our work proposes a new technique which includes measured thermal derivatives in the analysis to extract the isothermal response, and provides a more accurate small/large signal unified approach. The development of the small-signal model is based on thermal time constants [1], and provides accurate s-parameters for the development of the isothermal extraction technique and the large-signal model representation, appropriate for analog design.

2. Large Signal Model and Isothermal Extraction Technique.

For the development of the model a two-port device for small signal response is used, adding the self-heating effects assuming linearity of parameters with temperature (Fig. 1). Under these conditions a general expression for the conductance with thermal effects is derived and fitted with measured s-parameters from 1.2 μm gate fully depleted n-channel SOI MOSFETs, in order to determine the small signal parameters (thermal resistance and time constants) used as the basis to extract the output conductance needed for the isothermal characteristics which are necessary for the large signal model development and verification.

The large signal equivalent circuit is shown in Fig. 2 and it consists of two sections. The electrical response network consising of a *bias* and *temperature* dependent current source,

bias only dependent capacitances, and *fixed* external parasitic components, and the thermal network consisting of a nonlinear current source proportional to the instantaneous power dissipated in the device. As shown in the figure this current source drives an RC network which serves as the electrical analog to a single thermal time constant, but multiple time constants can be inserted to the right of the dashed line.

For the extraction of the isothermal characteristics we need the DC thermal resistance, α, which is derived below using the thermal derivative technique and can be calculated from realistic measurements to convert I_{DC} to its isothermal value I_d needed for the large signal:

$$\alpha = \{\partial I_{DC}/\partial V_{DS} - \partial I_d/\partial V_{DS}\} / \{\partial I_{DC}/\partial T_{amb} [V_{DS}(\partial I_d/\partial V_{DS}) + I_{DC}(V_{DS}, T_{amb})]\} \quad (1)$$

For large-signal verification 1.2 μm partially depleted MOSFETs with body ties to reduce floating body effects, were measured. Sinusoidal input signals were used for the test at high frequencies and pulse response at lower frequencies.

3. Experimental Results and Discussion.

Small-signal self-heating manifests itself mainly by changing the output conductance of the device, which corresponds to S_{22}. Fig. 3 shows the magnitude of S_{22} with frequency and the thermal time constant model fit along with the table of the time constants used. The thermal time constant model is applied using zero, one, and three time constants. It is evident that three time constants are sufficient for best fit with the measured S_{22}.This demonstrates that a multiple τ model is capable of accurately reproducing the small-signal thermal response.

For the large-signal model two sets of parameters were generated with one and two time constants. Fig. 4 shows the measured (solid) and extracted isothermal (dashed) DC output characteristics of a MOSFET.

The response of the drain bias to a pulse is shown in Fig. 5, at the low side of frequencies. Two time constants are sufficient in this case to give the best fit. The driving pulse form for the measurement was a 75 μs pulse from low 1.0 V to high 3.6 V and rise/fall times of 1 ns.

For the high frequency electrical response, a sine wave input with 2.7 V ptp at DC gate biases of 2.5, 2.0, and 1.5 V is used, yielding different levels of distortion at the output. At 2.5 V gate bias the MOSFETs are on over the entire cycle thus giving minimal distortion, while at 1.5 V the response is more distorted. Fig. 6 shows the response at intermediate gate bias of 2.0 V, where two time constants yielded excellent fit with the observed measured output.

4. Summary.

We present a new approach to incorporating the self-heating effects in SOI MOSFETs, using thermal time constants in the small-signal, and developing an isothermal extraction technique for the large-signal model. This allows both the small and large signal models to include thermal effects accurately.

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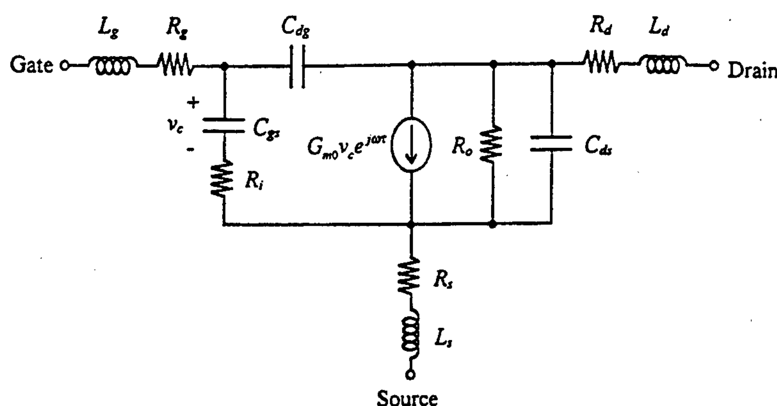

Fig. 1. Small-signal model equivalent circuit with external parasitics.

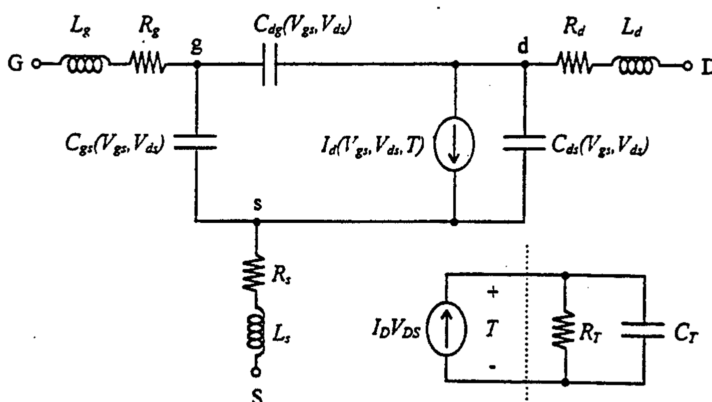

Fig. 2. Large-signal model equivalent circuit.

Number of Time Constants	tc_1	tc_2	tc_3	tc_4
1	58 ns			
2	209 ns	10.1 ns		
3	250 ns	16.7 ns	89 ps	
4	412 ns	75.4 ns	10.4 ns	85 ps

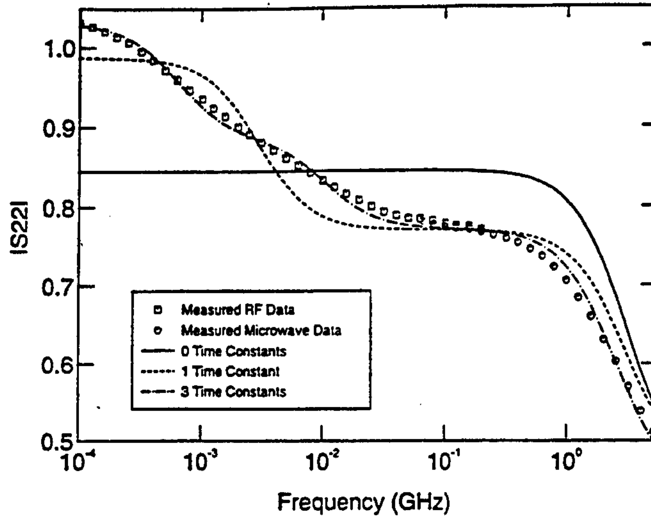

Fig. 3. Measured S_{22} and small-signal model fit with zero, one, and three time constants. Table shows the time constants used.

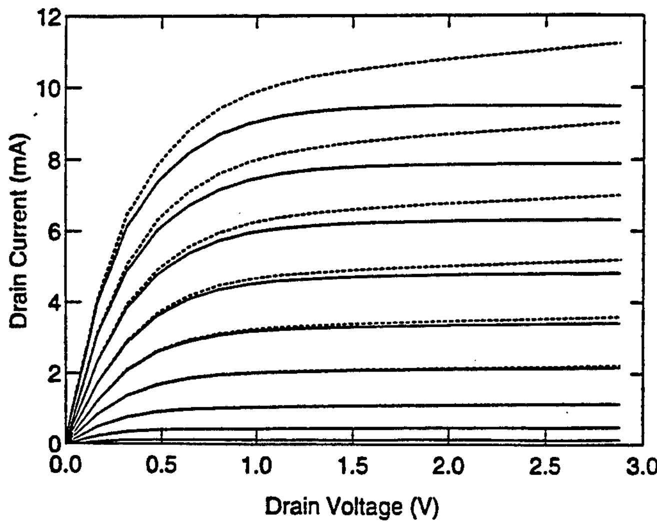

Fig. 4. Measured DC (solid) and extracted isothermal drain curren

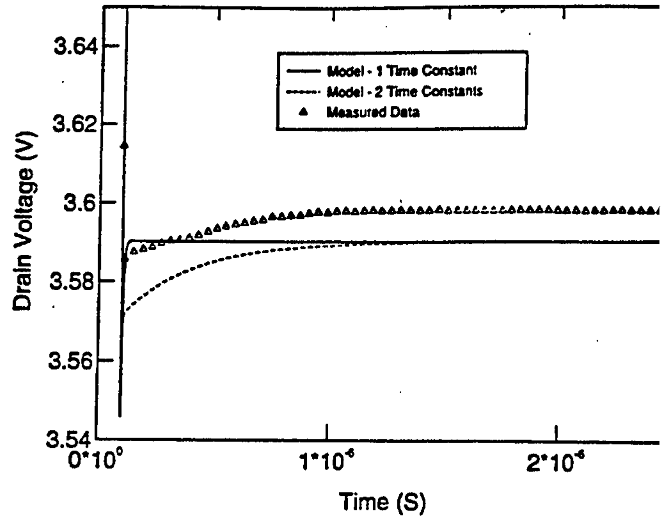

Fig. 5. Measured pulse response and large-signal fit with one and tw time constants.

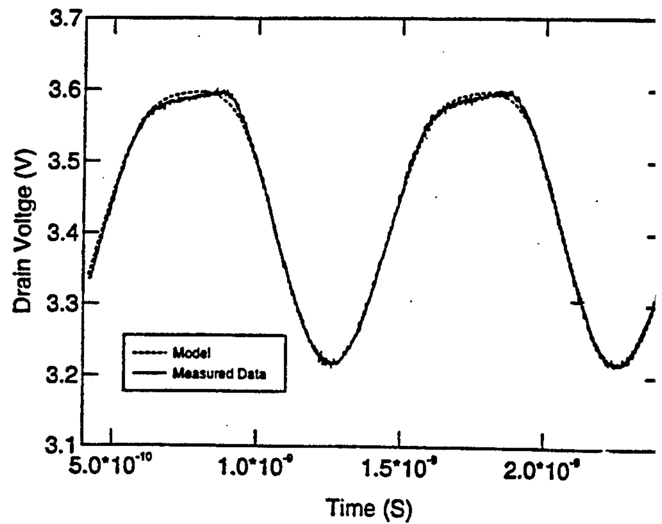

Fig. 6. Measured and fitted large-signal sine wave response. V_g =2.0

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