HIGH POWER, BROADBAND, LINEAR, SOLID STATE AMPLIFIER

2nd Annual Report
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September 1998

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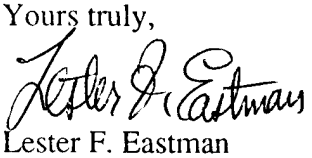

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13. ABSTRACT (*Maximum 200 words*)

Undoped, polarization-induced-electron HEMT's have been grown and processed on sapphire and SiC substrates. Devices with gate lengths between .15 and .75 μm have been fabricated. With .15 μm gates, f_t = 75 GHz and drain-source breakdown voltage of 35 V have been achieved. These values were 20 GHz and 140 V for .75 μm gates. Electron mobility values of 1,505 cm^2/V-s on SiC (OMVPE) and 1,232 cm^2/V-s on sapphire (MBE) have been obtained with 2 DEG density of `1.3-1.5 x $10^{13}/cm^2$. Optimum devices in 3 GHz operation yielded >70% power-added efficiency. The SIT device etching problem is solved using a combination of dry (ECR) and wet (hot KOH) etching. A traveling wave monolithic circuit will be used for our non-uniformly distributed power amplifier, with no backward wave. Large periphery (.5-1 mm) transistor "cells" are being tested, and for this circuit. Modeling of devices, Monte Carlo simulation of electron transport in short devices, and fundamental physics of GaN are all being undertaken, as is simulation of electron tunneling in from the Schottky gate. High resistivity V-doped SiC is supplied by Northrop Grumman, and bulk GaN growth is being developed. Using RHEED to obtain the correct (Ga) face, MBE growths of HEMT's is successful. An eight-wafer OMVPE reactor is operational, and refinements to yield increased uniformity and low output conductance are being developed.

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I. Overview of Cornell MURI Program on High Power, Broadband, Linear, Solid State Amplifier - L.F. Eastman

This is the second annual report on this MURI covering undoped AlGaN/GaN HEMT and doped GaN SIT devices and circuits. The design, fabrication, and characterization of the HEMT's have made very significant progress, yielding state-of-the-art results. With .15 μm gate length, f_t values of 75 GHz, and with .75 μm gate length, f_t values of 20 GHz have been obtained. The drain-source avalanche breakdown voltage was 35 V for .15 μm gates and 140 V for .75 μm gates, reflecting the 3 MV/cm breakdown field. The best power-added efficiency has been over 70% at 3 GHz in class A/B operation. Problems in gate leakage, with an associated kink in the drain current have occurred in many but not all cases. Means of eliminating this problem have been proposed and will be tested in the next quarter. Also, variable increased output DC and/or microwave conductance has been present in many, but not all cases. Again, new means of controlling this problem will be tested in the next quarter. The vertical FET, or SIT, devices encountered serious initial problems in obtaining good etch profiles. These problems have now been overcome, and working devices are expected in the next quarter.

The monolithic circuit, to yield the power, efficiency and bandwidths, is the Non-uniformly Distributed Power Amplifier (NDPA). It is a traveling wave structure with different impedance CPW transmission lines between the large periphery transistor power cells. The capacitor technology presently has low yield, but the use of thin Si_3N_4 dielectric deposited at low temperature, to lower the added strain on the GaN structure, is now expected to solve this problem. The heat flow in the multi-finger transistor power cell has been simulated for various pitches, and various substrate thickness. The advantage of SiC substrates is clear, compared with sapphire, and the heat power limits to limit the channel temperature to 500°K have been established. A range of theoretical studies have been made regarding electron transport in long and short channels, fundamental physics of GaN concepts, and HEMT device modeling. One study has been made to understand the thermionically assisted tunnel gate leakage current that can occur at pinch off, with added electric field from large drain-source voltage. Theoretically this does not yet appear to be a large problem, but with this computer program we can innovate on required future barriers.

The SiC high-resistivity substrates have been received in a timely fashion from Northrop Grumman, although a majority of the substrates being used are sapphire, for cost effectiveness. The GaN bulk growth program is proceeding slowly at Cornell, but pure GaN powder is ready, as are HVPE grown seeds. Exceptionally good progress has been made in the MBE growth of undoped AlGaN/GaN HEMT's on sapphire. A key aspect of this progress was the obtaining, and RHEED checking, of the Ga-face growth polarity. With this polarity, ultra smooth morphology, with 1,232 $cm^2/V\text{-}s$ electron mobility with $1.5 \cdot 10^{13}/cm^2$ electron sheet density have been achieved on sapphire. With lower dislocation density for growth on SiC, due to better lattice matching, better results are possible, and 1,505 $cm^2/V\text{-}s$ mobility has been gotten by OMVPE on SiC. The OMVPE reactor has been changed to allow eight 2-inch wafers to be grown at the same time. Means of adjusting the growth conditions for uniformity over the wafer, and from wafer to wafer have been established. A problem of undesired conduction in the region of the AlGaN nucleation layer and/or the GaN buffer layer has occasionally been encountered, and means of eliminating this problem will be developed. Using high resolution STEM samples, forbidden band states have been found near dislocations. Means of determining heterojunction planarity, and barrier strain will be developed, along with thickness calibration.

II. DISCRETE GAN TRANSISTORS

A. Summary - L.F. Eastman

The design, fabrication, and characterization of undoped $Al_xGa_{1-x}N$/GaN HEMT's on both sapphire and SiC substrates has advanced substantially in the past year. Most of the structures were grown by OMVPE, but lately MBE has been used successfully. Some of the processing difficulties have been overcome, and methods of obtaining faster, less expensive turn around are being pursued. Within the present technological limits in materials growth, and processing, frequency response and operating voltage limits have been found.

The present state-of-the-art for frequency response and source-drain breakdown voltage are 75 GHz and 35 V, respectively, for .15 μm gates. For .75 μm gates these values are ~ 20 GHz and 140 V, respectively. The state-of-the-art in efficiency was >70% for .3 μm gates, at 3 GHz, with ~ 1.5 W/mm output power using sapphire substrates. More recent devices on SiC have not yet been tested for maximum efficiency, but in DC tests of single gate devices with 1 A/mm current, steady performance at drain voltages above 20 V was obtained. Failure occurred for 25 V_{ds} and 1 A/mm drain current.

For the vertical FET, known also as the SIT, processing has been very difficult because of etch problems. A combination of ECR dry etch, followed by a hot KOH etch, has now been shown to give SIT ridges with the desired shape. SIT simulations have been extended to include LEO materials, although such LEO material is only contemplated as a backup in case the vertical electron transport is poor in normal epitaxial GaN.

B. Discrete Transistors: GaN HFET's - Ken Chu

In the past year progress was made in two major areas: the continued effort in fabricating and characterizing AlGaN/GaN HEMT's; and streamlining of the fabrication process for these transistors.

1. Typical layer structure

The AlGaN/GaN transistor heterostructure we have been using in the past year is depicted in Figure 1. It is noteworthy that the whole structure is undoped (or not intentionally doped), and it makes full use of the strong polarization effects in group-III nitrides to generate the 2-dimensional electron gas (2DEG) at the AlGaN/GaN interface.

A detailed discussion of the formation of the 2DEG in this layer structure is given in Ambacher *et al* [1]. In short, the discontinuity of the polarization field across the AlGaN/GaN interface (in Ga-face material) mandates a fixed positive sheet charge on the AlGaN side, and this positive sheet charge in turn induces electrons to be confined in the quantum well formed at the AlGaN/GaN hetero-interface.

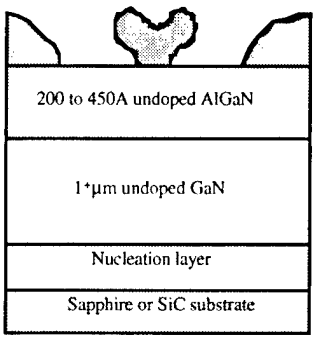

Figure 1 Layer structure of undoped AlGaN/GaN high electron mobility transistor.

2. Current transistor fabrication process

The current AlGaN/GaN HEMT fabrication process is as follows:

- Tungsten sputtering of alignment marks (e-beam lithography),
- Cl_2 based ECR mesa etching (optical lithography),
- Ti/Al/Ti/Au ohmic contact formation (e-beam lithography),
- Ti/Au overlayer metal deposition (e-beam lithography),
- Ni/Au gate deposition (e-beam lithography).

The ohmic contact formation includes an annealing step at 800°C for 1 minute, which generally gives contact resistivity in the range of 0.2 to 1 Ω-mm.

One obvious point about the above-mentioned fabrication steps is the extensive use of electron-beam lithography. The reason for this is that we discovered our dopant-free AlGaN/GaN layer structures are extremely sensitive to any surface treatment. Specifically any hydroxide based optical resist developer can reduce the sheet charge density by up to 80% if it touches the active device area. The consequence of this extensive use of e-beam lithography is a longer turn-around time from end of growth to finishing of transistor fabrication. This problem is currently being addressed and a solution is given at the end of this section.

3. Transistor results

There were 3 sources of AlGaN/GaN material in the past year, namely ATMI/Epitronics, Cornell OMVPE facility and Cornell MBE facility. The material was all processed to make transistors out of them and the results are as follows.

4. ATMI/Epitronics

Matrices of large periphery devices (300 µm ≤ gate width ≤ 4 mm) were fabricated on an undoped $Al_{.31}Ga_{.69}N$ (450 Å) / GaN (1^+ µm) / sapphire structure grown by ATMI. These air-bridged devices, with 4 to 16 gate fingers, each finger 75 µm to 250 µm long, all had a gate length of 0.3 µm. Microwave power measurements performed at

Sanders/Lockheed Martin demonstrated simultaneously a power output density of 1.55 W/mm, a large-signal gain over 12 dB and an excellent power added efficiency above 70% for a 0.3 x 500 μm^2 device at 3 GHz. At 10 GHz, P_{out} = 0.84 W/mm, G = 8 dB and PAE = 37% were obtained.

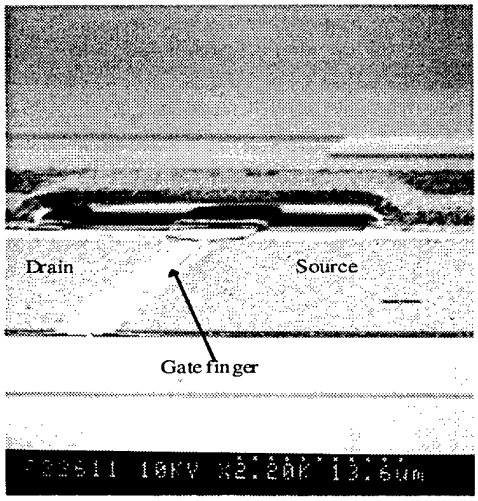

Figure 2 Air-bridge structure going over an underlying gate-feed.

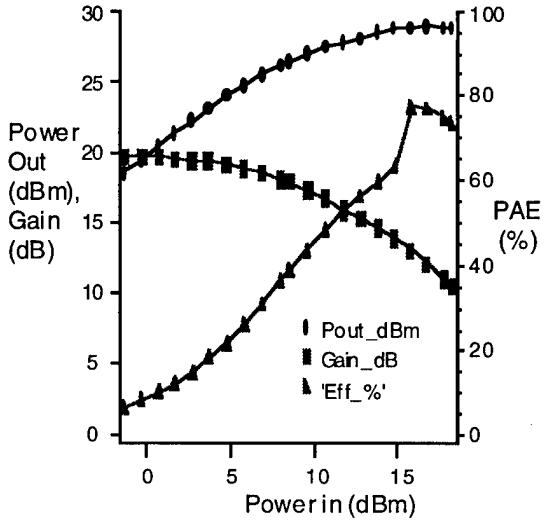

Figure 3 Microwave power performance for a 0.3 x 500 μm^2 device at 3 GHz.

The same layer structure was also used to fabricate small periphery ($\leq$ 150 μm) devices with gate lengths varying from 0.15 μm to 0.75 μm. These devices showed a maximum drain-source current over 700 mA/mm and an extrinsic transconductance above 220 mS/mm. For devices with 0.15 μm gates, then world-record results of f_T = 67 GHz and f_{max} = 140 GHz were obtained, while the gate-drain breakdown voltage was a modest 35 to 40 V. With 0.33 μm gates, breakdown voltage doubled to over 70 V but f_T and f_{max} dropped to 30 GHz and 100 GHz respectively. 0.75 μm gate devices demonstrated an f_T of 17 GHz with a gate-drain breakdown voltage of 140 V.

5. Cornell OMVPE

During the past year a lot of progress was made in the in-house OMVPE epitaxial growth of AlGaN/GaN layers on both sapphire and SiC substrates. These wafers have electron sheet densities near $1 \cdot 10^{13}$ cm^{-2} and mobilities ranging from 700 to 1,500 cm^2/Vs. With careful growth of both the AlGaN barrier and the nucleation layer, negligible unintentional doping in the barrier and the buffer layers was determined by capacitance-voltage measurements. Subsequent processing on these material produced results described below.

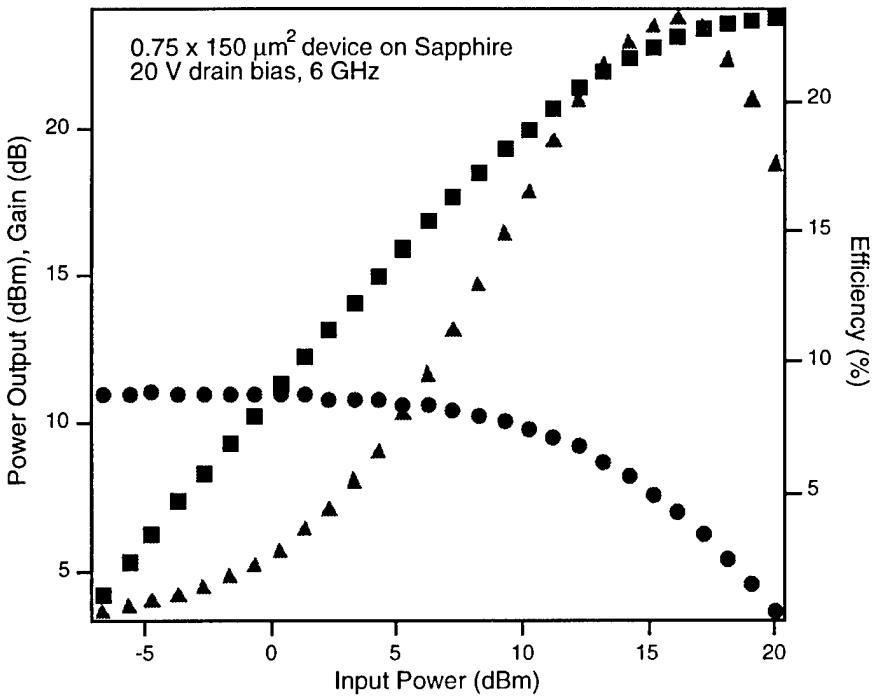

Figure 4 Microwave power measurement of a 0.75 μm gate length device on sapphire showing 1.6 W/mm output power.

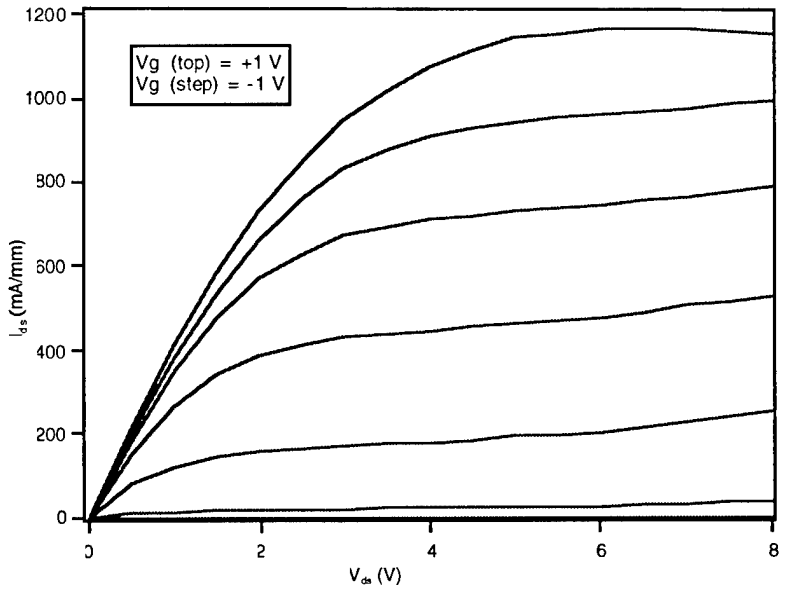

Figure 5 I-V characteristics of undoped AlGaN/GaN/SiC HEMT's.

Using sapphire as the substrate and processing techniques mentioned at the start of this section, transistors fabricated have shown maximum drain currents in excess of 900 mA/mm, peak transconductances over 200 mS/mm, and f_T as high as 50 GHz for 0.18 μm gates. Microwave power measurments showed, for a 0.75 μm gate length device,

a maximum power output of 1.6 W/mm with class A operation yielding over 23% power added efficiency.

SiC substrates, with its much higher thermal conductivity and better lattice match to GaN than sapphire, should yield improved AlGaN/GaN HEMT device performance. Measured I-V characteristics for fabricated AlGaN/GaN HEMT's on SiC are shown in figure 5 for a 0.3 μm gate length device. Peak drain current at +1 V gate bias was measured to be 1.16 A/mm. The slight drain current rise near pinch off, at drain-source voltage over 20 V, may have resulted from the gate tunnel current and subsequent multiplication. Measured extrinsic transconductance (g_m) ranged from 270 to 300 mS/mm. These extrnsic values, together with a total source resistance of 1.2 Ω-mm, yields intrinsic transconductance (g_{mi}) values ranging from 400 to 470 mS/mm.

From these DC results, one would expect the RF response to be excellent. Indeed this was the case. With a gate length of 0.15 μm and a gate periphery of 150 μm, small signal measurements demonstrated new state-of-the-art f_T of 75 GHz. 0.3 and 0.75 μm gate length devices also yielded f_T = 42.5 GHz and 19.2 GHz respectively. Large signal measurements were also performed on these transistors. As shown in Figure 6, a 0.75 x 100 μm^2 device yielded 2.45 W/mm and 18% power added efficiency in class A operation at 6 GHz. The small signal gain was 14 dB.

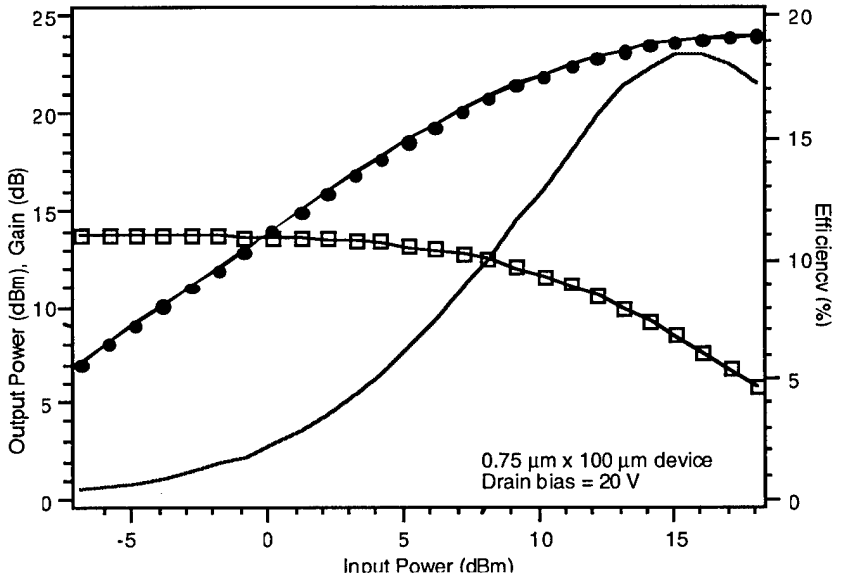

Figure 6 Power measurements on a 0.75 x 100 μm^2 AlGaN/GaN HEMT on SiC showing an output power density of 2.45 W/mm

6. Cornell MBE

In the past year the Cornell nitride MBE team has shown tremendous progress in understanding the growth requirements for device quality material, culminating in the first achievement of an AlGaN/GaN HEMT on sapphire. Peak drain current was over 750 mA/mm with +2 V on the gate with a peak transconductance over 200 mS/mm. Small

signal measurements yielded an f_T of 27 GHz for a 0.2 μm device, mainly limited by a small amount of parallel conduction in the buffer.

7. New transistor fabrication process

As mentioned earlier, to increase the throughput in our processing and quicken the feedback to the epitaxial growth, we need to switch from a predominantly e-beam lithography process to a predominantly optical lithography process in which only the gates are written with e-beam. However, since our layer structures are very sensitive to hydroxide based solutions (including all optical resist developers available at Cornell Nanofab), a multilayer resist scheme is proposed which consists of:

- PMMA as the bottom layer, flood exposed with deep UV,
- A thin metal (e.g. chrome) layer as the inter-diffusion barrier,
- Optical resist on top, patterned with a g-line stepper.

The pattern of the optical resist will be transferred to the metal using wet etch and then to the PMMA using toluene, which dissolves the exposed PMMA but not the optical resist on top. We will then have an undercut profile desirable for lift-off purposes. With this scheme we can shorten our exposure time per step by hours, saving both time and money. Actual utilization of this trilayer resist scheme will be carried out after further testing.

Figure 7 Multi-layer resist scheme for lift-off process using optical patterning.

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[1]O. Ambacher et al., "Two dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures", submitted to Journal of Applied Physics.

C. SIT Device - Nils Weimann

1. Device design and simulation

The epitaxial lateral overgrowth (ELO) of GaN leads to a threading dislocation density of almost zero. Using an offset pattern of overgrown stripes aligned to the multifinger SIT structure, the method can be used for ELO SITs. In Figure 8 (right), the effective current spreading in the highly doped buffer layer is shown. The thickness of the n^+ buffer is indicated by arrows.

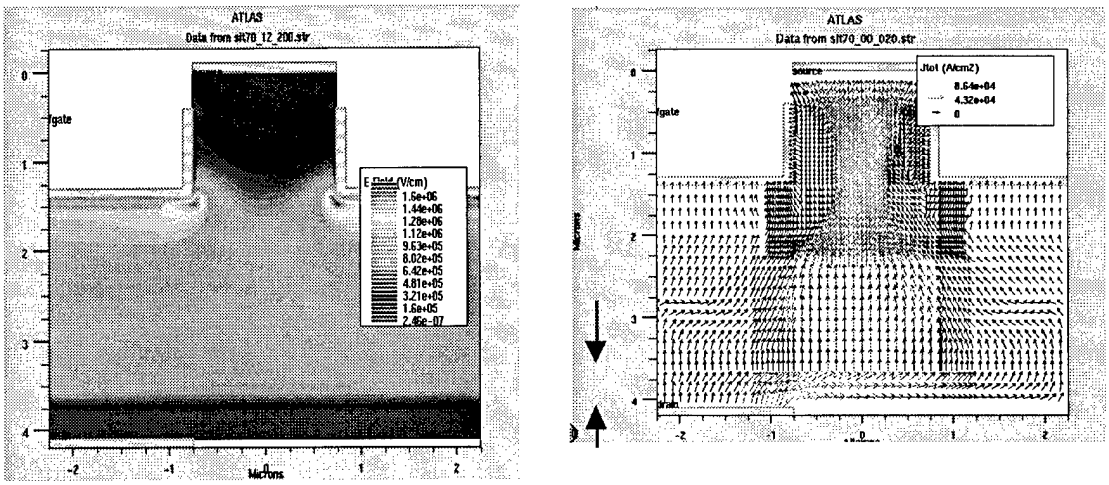

Figure 8 ELO SIT simulation: field at pinch-off (left) and current density in the on-state (right).

Thermal simulations of the entire device structure including the substrate were carried out. The decrease in thermal conductivity of the substrate and the epi-layer were modeled with a 1/T-dependence. Thermal conductivities of 1.3 and 5 W/cmK for the GaN epi material and the n^+ SiC substrate were assumed, respectively. The simulated current density in the on-state of a GaN SIT with a doping concentration of $3 \cdot 10^{16}$ cm^{-3} in the drift region translates into ohmic heating in the active channel region with a heat dissipation of 5 W/mm. This allows tighter finger density than in the case of the HEMT, since the heat is spread out more uniformly, and the decrease in thermal conductivity is less pronounced (see Figure 9).

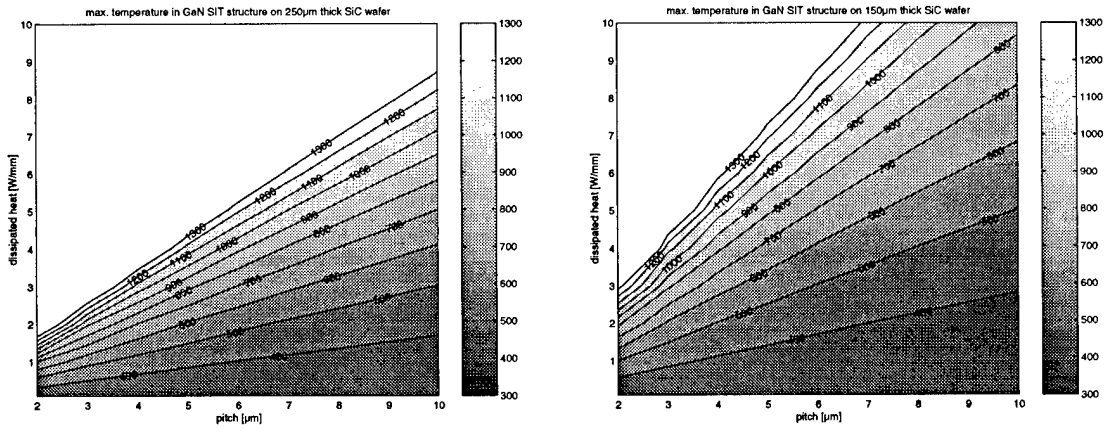

Figure 9 SIT heating.

Using a 150 µm thick wafer, a maximum temperature in the device structure of 500 K is attained at a heat dissipation of 5 W/mm and a pitch of 10 µm, meaning that the heat dissipation per unit area can be as high as 500 W/mm^2. However, this is a theoretical

maximum, since no effects of crystal imperfections and phonon reflection at the SiC/GaN interface were taken into account.

2. SIT layer epitaxy

We received shipment of two 2" sapphire wafers with MOCVD SIT epilayers from Fraunhofer-IAF, Freiburg, Germany, as well as two 1 3/8" SiC wafers with the same structures. However, growth of thick GaN layers on SiC is not optimized yet, the films cracked due to internal stress during the growth. The doping concentration in the GaN films could be reduced by a factor of 2 down to the low 10^{16} cm^{-3} range, permitting lower current densities and cw device operation of devices on SiC. Further SIT device development is ensured with this shipment, and development of thick crack-free GaN layers on SiC is underway at Fraunhofer-IAF.

3. Ohmic contacts to n^+ GaN

The ohmic source contact metallization is used as a self-aligned etch mask in the ECR etching of GaN. The high plasma density of the ECR etch leads to erosion of the contact metallization. Only Ni has proven high stability so far. Ti is heavily attacked in Cl plasma chemistry, even if a Ti/Ni stack is used with a layer thickness of 100 and 2000 Å, respectively. Initially used Ti/Ni on n^+ GaN contacts annealed at 600°C for 30 sec in N_2 atmosphere using a Rapid Thermal Annealer yielded a contact resistance of $< 10^{-6}$ Ωcm^2, as measured using circular TLM patterns. Recent investigations of masking metal stability revealed that Cr/Au/Ni layers, or alternatively Zr/Au/Ni layers, are stable during the ECR etch and the hot KOH chemical etch (see below). Selectivity of our smooth GaN etch over the Ni mask is as high as 8:1. Electrical data of the new contact methods is to be established yet.

4. Schottky contacts to n^- GaN

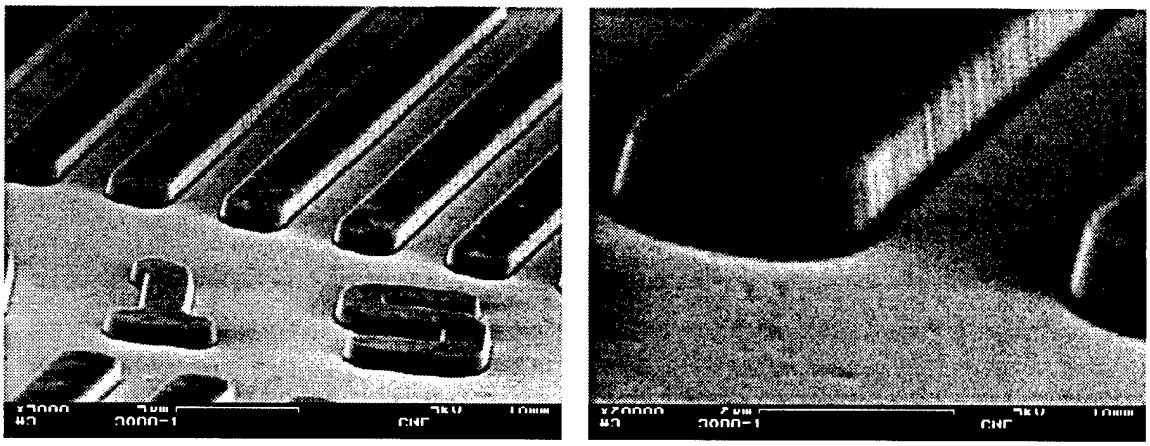

Figure 10 ECR etched test patterns, Ni mask.

Up to now, only Ni Schottky contacts to dry etched n^- GaN surfaces were measured. Typically, breakdown of these contacts occurs around –5 V. Schottky contacts to the wet etched surfaces need to be characterized yet. ECR dry etching of GaN ECR

etching of GaN with smooth etched surfaces was attained using a $Cl_2/CH_4/Ar/H_2$ process gas mixture at room temperature, producing a DC bias of –180 V at 150 W RF power and –220 V at 200 W RF power in the PlasmaQuest tool available at Cornell. The striations visible in Figure 10 (right) stem from the erosion of the Ni mask during the etch. Sidewall slopes of 70-80° were obtained. This etch chemistry has a selectivity to photoresist of 2:1. The etch rate is 900 Å/min.The steepness of the sidewalls of only ECR etched samples is still not sufficient for self-aligned evaporation of the gate metal in the gate trenches.

5. Hot KOH etching of GaN

Recently, the etching of GaN in hot KOH dissolved in Glycol was discovered by Stocker and Schubert at Boston University[1]. Their results for hot KOH and NaOH were reproduced at Cornell University using Fraunhofer's MOCVD material.

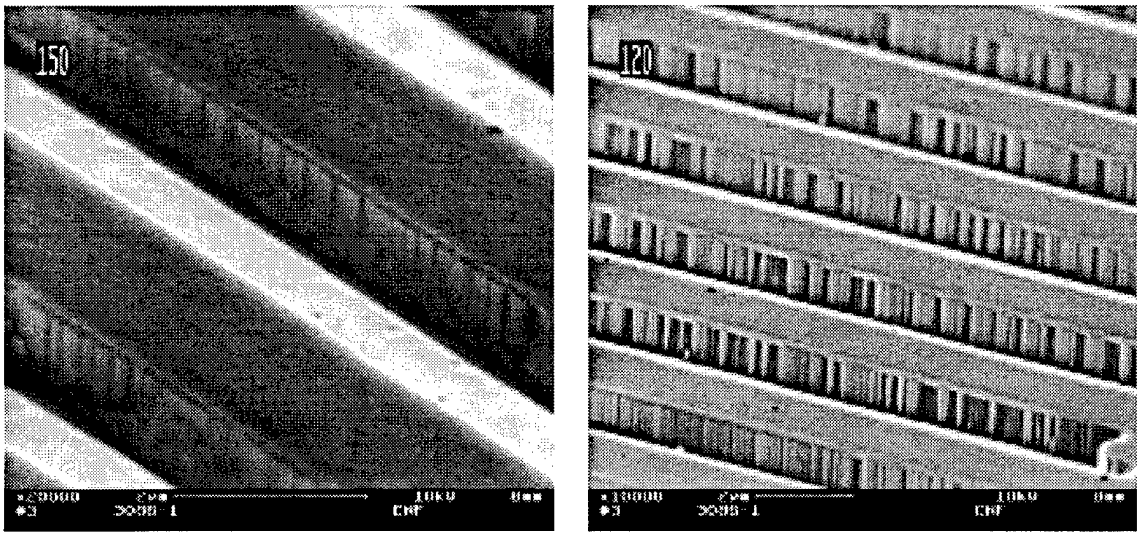

Figure 11 Effect of pattern orientation on sidewall smoothness: good alignment (left), 30° off (right).

We used the hot etches to "clean up" after an initial ECR dry etch. The hot KOH etch stops on the [0001]–plane, the depth of the etch is only determined by the initial dry etch. An investigation of etching using a Ni mask pattern at different angular orientation with respect to the a-axis of the hexagonal GaN crystal revealed that the etch stops on the a-plane, as well. If the etched wall is aligned to the a-face of the crystal, the hot etch results in a smooth, perfectly vertical sidewall, as shown in the etched device structure in Figure 12 (right). The undercut under the masking material is controlled via the etch duration and rate, which depends exponentially on the etchant temperature. The combination of available dry etches with sidewall slopes between 45 and 80° and the lateral undercut using the hot KOH etch is an extremely versatile tool to process GaN layers.

The fabrication of self-aligned gates by simple evaporation into the etched grooves is now possible. It is clearly visible in Figure 12 (left), that the gate metal does not cover the sidewall. The gate "length" can be easily controlled by the thickness of the evaporated metal. The source metallization used for the device structure shown in Figure 12 (right)

[1] D. A. Stocker, E. F. Schubert, and J. M. Redwing, Appl Phys Lett 73 (15), Oct 12, 1998

was Ti/Ni/Ti. The first Ti layer was undercut during the dry etch from the side, as can be seen in Figure 12 (left), and subsequently lifted off in the hot KOH etch.

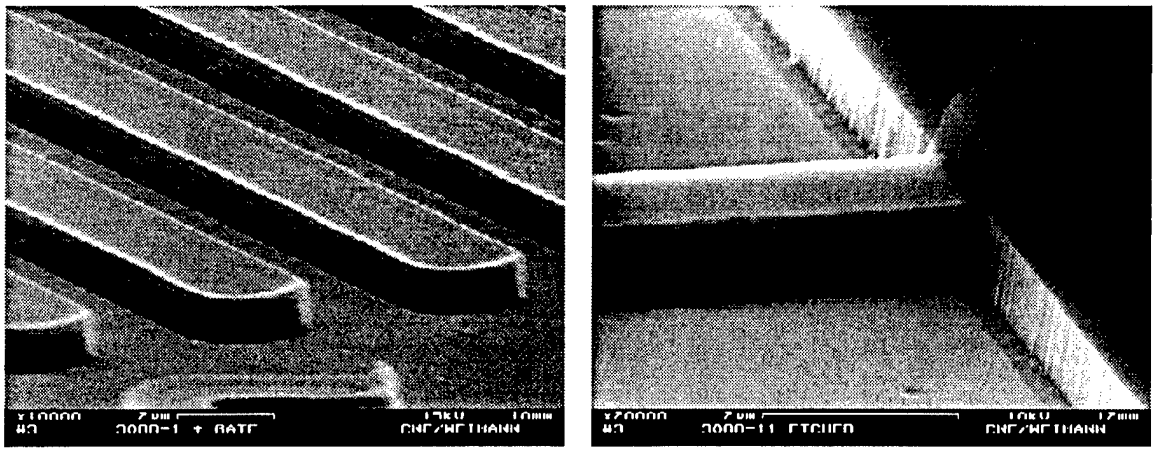

Figure 12 self-aligned evaporation of the gate metal (left), etched device structure (right).

6. Summary

With the discovery of the combined dry and wet etch, self-aligned SIT devices have become a possibility. Cr/Au/Ni layers on Si dummies have shown sufficient selectivity at optimized etch conditions. SIT device results are projected for the forthcoming quarter.

III. AMPLIFIERS AND HEAT SINKING

A. Summary - L.F. Eastman

Progress has been accelerated in the development of the design, simulation, and fabrication technology of a circuit configuration for high power, high efficiency, broad band operation. The traveling wave circuit, monolithically combines four power transistor cells in a non-informally distributed amplifier, with different impedance CPW's between successive cells. This eliminates the backward wave, substantially increasing efficiency. Capacitor technology has involved polymide dielectric to date, but will use Si_3N_4 as soon as ECR or related deposition equipment is available locally to deposit dense Si_3N_4 at low temperature. The low temperature is required to limit additional strain on the already strained nitride material.

The impact of the substrate thickness on the channel temperature rise in multi-finger HEMT's has been simulated. The thickness range of 100-330 μm for both sapphire and SiC were studied, along with different pitch between parallel channels. For 50 μm pitch, and 100 μm substrate thickness, heat power per mm of gate periphery necessary to reach 500°K channel temperature were found to be 1.7 W/mm for sapphire, and 11.5 W/mm for SiC. For 250 μm thick substrates, these values were .76 W/mm, and 6.5 W/mm respectively.

B. Monolithic Integrated Circuits - Bruce Green

1. Overview

This contract year is achievements include the design and layout of a monolithically integrated (travelling wave) non-uniformly distributed power amplifier (INDPA) along with the development of a AlGaN/GaN MMIC fabrication process. Goals for the third contract year include 1) completion of fabrication and testing of MMIC amplifier, 2) incorporation of high-efficiency gain cells into second amplifier iteration, and 3) fabrication of MMIC amplifier on AlGaN/GaN grown on SiC substrates to meet the power requirement.

2. Nonuniformly Distributed Power Amplifier

This form of amplifier circuit has also recently been chosen as the best candidate for high power, high efficiency, broad band operation by Sanders/Lockheed Martin.

The non-uniform impedance traveling wave amplifier layout shown in Figure 1 below eliminates the backward wave present in conventional TWA designs. The amplifier consists of four 500 μm AlGaN/GaN HEMTs cells combined using stepped-impedance transmission lines having characteristic impedances of 90 Ω, 45 Ω, 33 Ω, and 22.5 Ω. Two of these amplifiers will be combined and converted to 50 Ω input and output impedance using off-chip multi-section Wilkinson power combiners. Small signal simulations shown in Figure 2 show >10 dB of small signal gain. Harmonic balance simulations of the circuit shown in Figure 2 predict 30% peak power-added efficiency and 35 dBm of CW output power when the input and output are matched into 25 Ω. These simulations are based on models extracted from Cornell devices grown on sapphire.

Amplifiers fabricated on SiC substrates are expected to produce 45+ dBm of output power at 40-50% P.A.E.

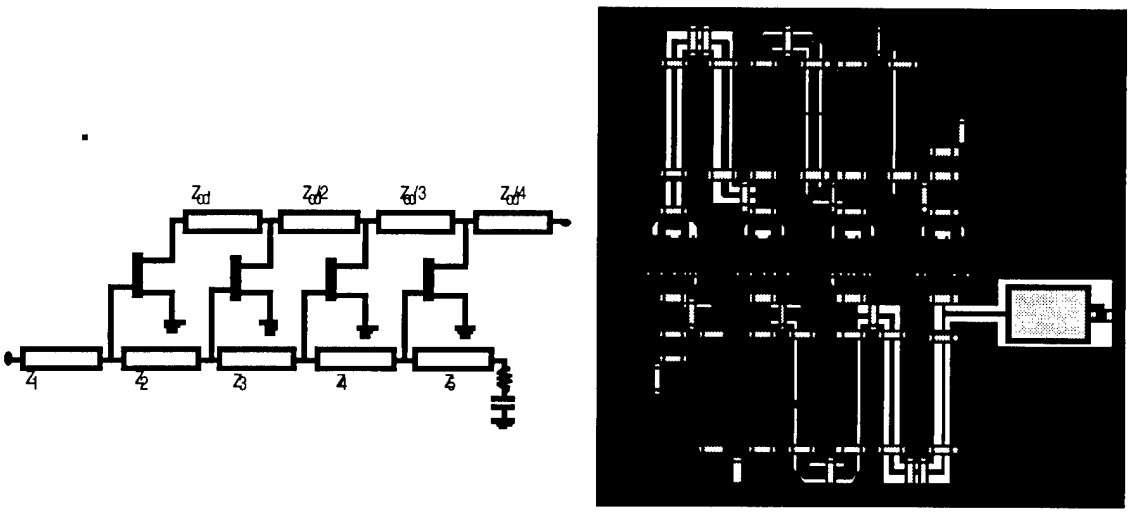

Figure 1 Circuit topology and layout of a four-cell non-uniformly distributed (travelling wave) power amplifier.

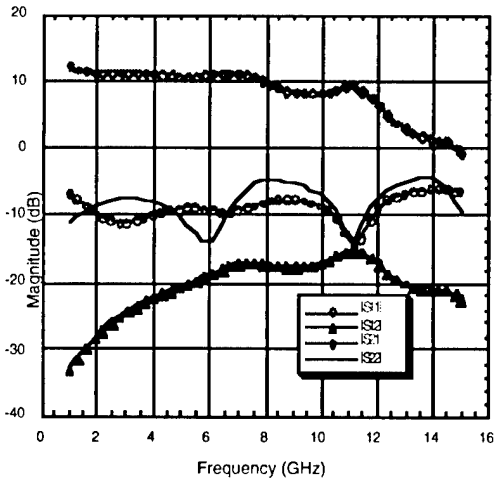

Figure 2 Simulated small signal frequency response of GaN MMIC amplifier.

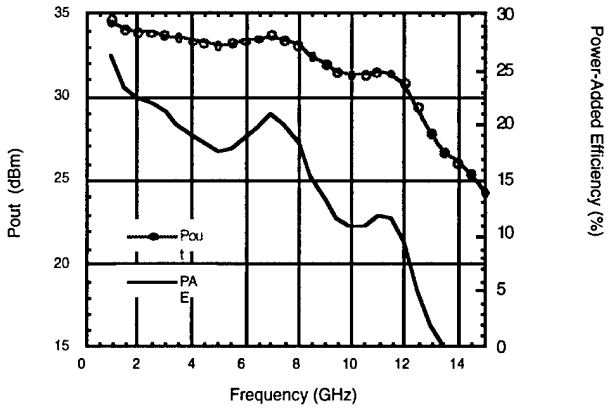

Figure 3 Simulated small signal frequency response of GaN MMIC amplifier.

3. GaN MMIC Process

Figure 4 shows a diagram of the process used for GaN MMIC fabrication that has been developed along with examples of integrated components fabricated during the development of this process. The process consists of eight mask levels. These levels include 1) mesa isolation etch, 2) ohmic contact formation, 3) gate metal deposition, 4) NiCr resistor formation, 5) base metal deposition, 6) polymide dielectric deposition, 7) airbridge via deposition, and 8) plated airbridge metallization. The MMIC process has to minimize the stresses presented to the already strained piezoelectrically induced active regions. For this reason, polymide is used as the dielectric for MIM capacitors and passivation rather than Si_3N_4. The use of coplanar waveguide (CPW) for the passive transmission lines obviates the need for backside via processing.

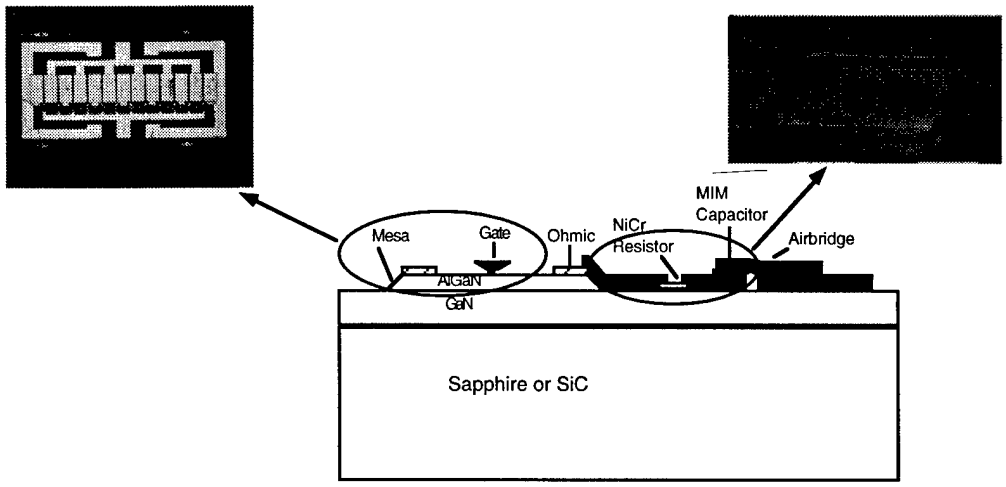

Figure 4 Diagram of MMIC process showing examples of fabricated devices and MIM capacitors.

4. Fabrication Progress and Outlook

An unforeseen processing irregularity halted the first process iteration at the gate level. At the time of writing, a second amplifier fabrication iteration is underway with measured results expected by mid-October 1998. As experience with the circuit processing increases, amplifier turn around times will be under two weeks.

During the remainder of the contract year, special emphasis will be placed on increasing the total gate periphery to 10 mm of the amplifier while maintaining the 1-12 GHz bandwidth. This will be accomplished using high-efficiency cascoded gain cells. After 2 circuit design/process iterations, a transition will be made from sapphire substrates to SiC substrates. Parallel to the design and fabrication efforts, improved models of the AlGaN/GaN HEMTs will be developed in collaboration with Michael Shur group at RPI.

C. GaN HEMT Thermal Simulations – Nils Weimann

In order to evaluate the thermal management of multifinger AlGaN/GaN HEMT devices, two-dimensional thermal simulations were performed using the Finite Element Method. Thinned SiC and Sapphire substrates are now readily available. The surface temperature was calculated for substrate thickness ranging from 330 µm down to 100 µm. In both cases of SiC and sapphire substrates, a 1/T dependence of the thermal conductivity is assumed. At 275 K, values for the thermal conductivity are 3.3 W/cmK in the case of SiC, and 0.3 W/cmK in the case of sapphire, respectively. The thickness of the GaN epilayer is 1 µm, and the length of the heat source, i.e. the length of the active channel region between source and drain, is 1.5 µm.

The nonlinearity of the thermal conductivity leads to the formation of a "hot spot" around the active channel region. An earlier comparison between simulations using a constant thermal conductivity and the nonlinear model showed an underestimation of the channel heating of up to 20%. This discrepancy increases with higher channel temperatures.

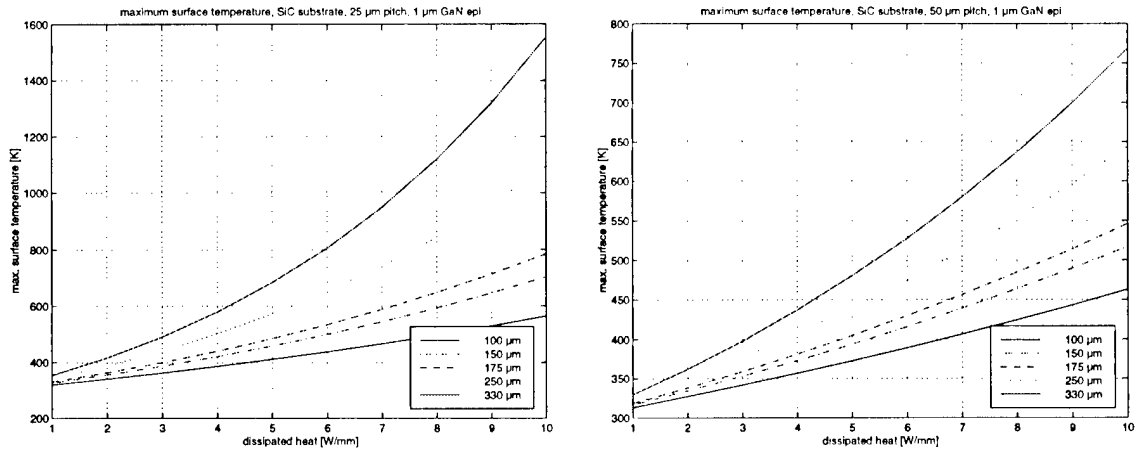

Figure 5 SiC substrate: 25 µm pitch (left) and 50 µm pitch (right).

To improve device reliability and contact metallization stability, and to account for reduced thermal conduction across the epilayer-substrate interface, we chose a channel operating temperature of 500K. At this channel temperature, and with a substrate thickness of 100 μm, from Figure 5, the maximum dissipated heat amounts to 8 W/mm at a pitch of 25 μm, and to 12 W/mm at a pitch of 50 μm.In the case of 100 μm thick sapphire, the maximum heat dissipation is less than 1 W/mm for 2.5 μm pitch and 1.7 W/mm for a 50 μm pitch (see Figure 6).

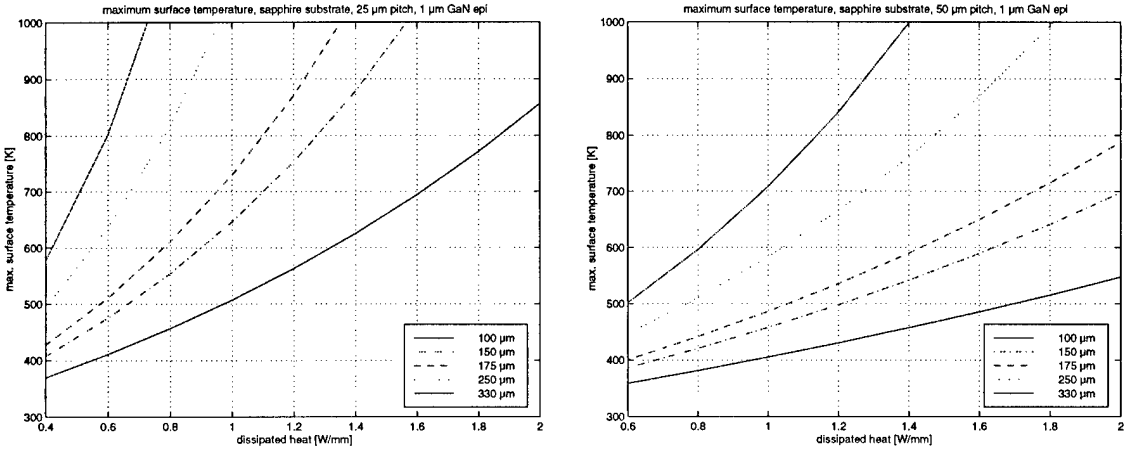

Figure 6 Sapphire substrate: 25 μm pitch (left) and 50 μm pitch (right).

IV. THEORETICAL STUDIES

A. Summary - L.F. Eastman

Doped HFET performance has been analyzed, as well as double channel HFET's. In addition, steady state electron transport has been studied in GaN, AlN, and InN, using the Monte Carlo method. The effect of doping and temperature have been included. Velocity overshoot effects have been studied with both thermal electrons and ballistically-injected electrons. Dimensions under .1 μm are required for substantial increases in average transit velocity for GaN. Thermally-assisted electron tunneling has been analyzed for Ni Schottky barriers on $Al_xGa_{1-x}N$/GaN HEMT's at pinch off for $.05 < x < .45$ at room temperature and at 500°K. The magnitude is below the $4 \cdot 10^6$ A/m^2 value that interferes with microwave performance for the assumed case of perfect material.

B. Design, characterization, and simulation of high-power AlGaN/GaN HEMT's - Michael Shur, B. Iniguez, J. Deng, A. Dickens, N. Dyakonova

This work was performed in collaboration with researchers at APA Optics, Cornell University, the University of Illinois at Urbana-Champaign, and the University of Virginia. We have reported on the DC and microwave performance of 0.25-micron gate doped channel $Al_{0.14}Ga_{0.86}N$/GaN HFETs. We have found a cutoff frequency of 37.5 GHz and a maximum frequency of oscillation of 80.4 GHz.

Calculations of the Fermi level position, and a comparison with the expected conduction band discontinuity, confirmed that the channel in these transistors was doped. The DC and microwave characteristics of these devices do not change much with temperature, at least up to 200°C and 90°C, respectively. In order to obtain a higher breakdown electric field, we have developed AlGaN-GaN DC-HFETs with offset gates. The breakdown voltage in these devices exhibited a strong dependence on the gate-to-drain separation, and the maximum transconductance increased almost linearly with the source-to-drain distance. A breakdown field of 1.3 MV/cm was obtained.

The offset design also resulted in a reduced gate leakage current. We have also found a high turn-on voltage (approximately 2.5 V) of the gate-source leakage current in AlGaN/GaN High Electron Mobility Transistors (HEMTs). A larger conduction band discontinuity and a higher electron effective mass (compared to AlGaAs/GaAs HEMTs) lead to a lower gate current and a higher turn-on voltage. The piezoeffect and the doping result in the electron sheet concentration up to 2×10^{13} cm^{-2}. In addition, we have reported on new AlGaN-GaN HFETs on SiC substrates. The devices exhibited a current of up to 0.95 A/mm with a stable performance up to 250°C with the current saturation up to 300°C. The maximum power dissipation at room temperature was found to be 6×10^5 W/cm^2.

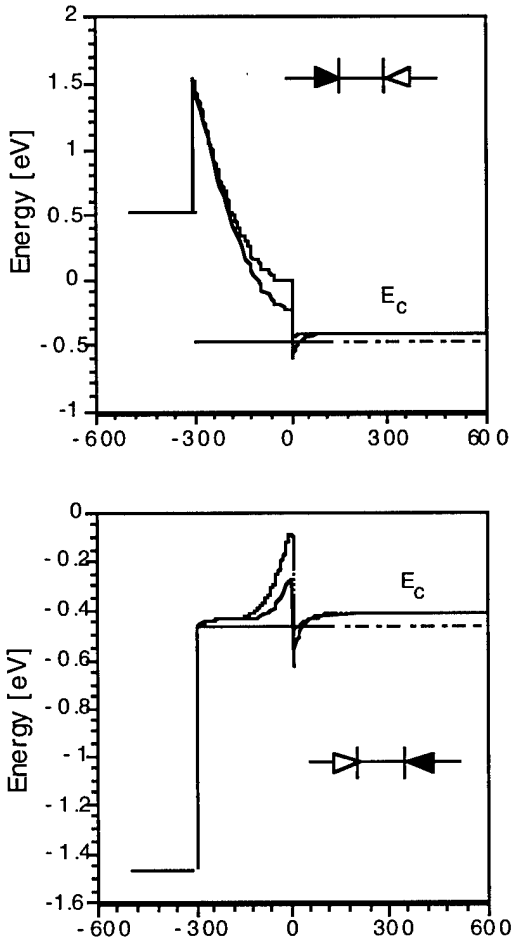

Figure 1 Calculated band diagrams of the $Al_{0.2}Ga_{0.8}N$/GaN HEMTs accounting for the piezoeffect (solid lines) and neglecting the piezoeffect (dotted lines) at gate voltages -1V (a) and +1V (b). Donor concentration in $Al_{0.2}Ga_{0.8}N$ is 10^{18} cm^{-3}. Also shown is the two-diode equivalent circuit. The equivalent circuit diode controlling the gate current is shown in black.

Modeling of Submicron GaN/AlGaN HFETs for Amplifier Design. The design of high power microwave GaN/AlGaN HFET amplifiers requires accurate and reliable mixed mode models that should describe both dc and ac characteristics over a large range of applied biases and device currents. The development of such a model presents a challenge. We first addressed this challenge for conventional AlGaAs/GaAs HFETs. Recently, we have been able to demonstrate such a model for the first time. Under the auspices of this MURI program, we developed such a model for 0.25-micron GaN/AlGaN HFETs. We simulated the microwave performance of this transistor and compared it with our experimental data (up to 1.7 W/mm) and started our analysis of the design trade-off. This included the analysis of the gate length and parasitic series resistance effects on the microwave performance.

1. Double Channel AlGaN/GaN HFET for Power Applications

We reported on a Doped Double Channel AlGaN/GaN Heterostructure Field Effect Transistor, where the bottom channel is formed by a GaN-AlGaN-GaN Semiconductor-Insulator-Semiconductor structure, see Fig. 2. The doped GaN channel increases the capacitance between the device gate and the bottom channel. The series resistance for the bottom channel is strongly dependent on the drain bias. This new design demonstrates that the current carrying capability of AlGaN/GaN HFETs can be enhanced using multi channel structures.

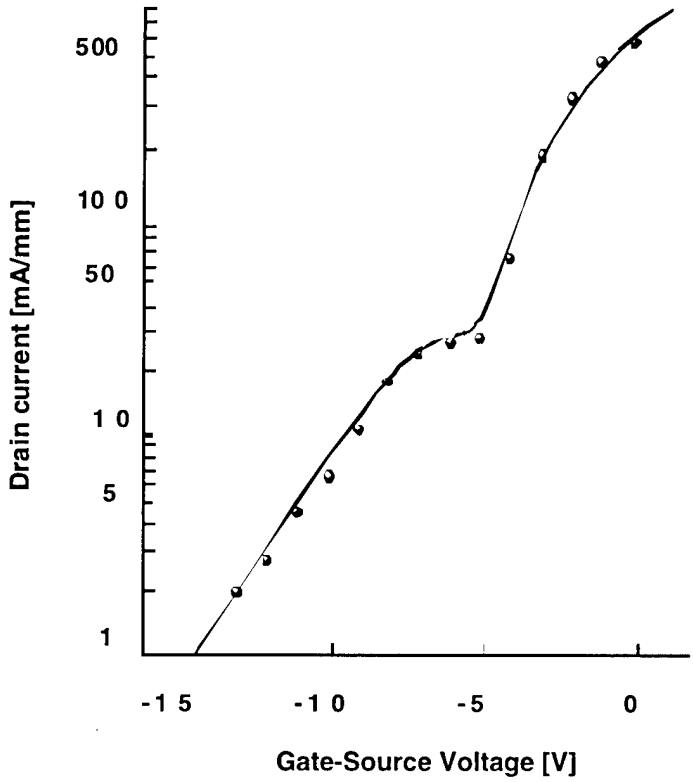

Figure 2 Measured (dots) and calculated (curve) transfer characteristics of the double-channel HFETs.

We also studied the behavior of hot electrons in GaN quantum channels and reached an important conclusion regarding the impact ionization rates in these devices related to the space dependence of the effective mass in these heterostructures. This dependence leads to a strong interdependence of the longitudinal and transverse motion in systems with heterointerfaces, such as quantum wells. Such interdependence results in additional non-parabolicity of the longitudinal motion in quantum wells. At large energies, comparable to or exceeding the depth of a quantum well, the effective mass changes sign and the longitudinal two-dimensional spectrum terminates at a certain critical value of the longitudinal momentum. The space dependence of the effective mass also strongly increases the transmission through a potential barrier for electrons with large incidence angles. These effects should have important consequences for impact ionization and tunneling phenomena in GaN-based heterostructures.

We predicted that n GaN/AlN-based systems, hot electrons with energies above the energy gap (that are responsible for impact ionization) are de-localized, and their wave functions are primarily located in cladding AlGaN layers. Hence, the impact ionization rates will be much smaller than those for the quantum well material and should approach those for the cladding, wider band gap layers. This might be especially important for InGaN/GaN and InGaN/AlGaN heterostructures, since this effect would allow us to combine a higher mobility in the quantum well material with a higher breakdown field of wider band gap cladding layers. This prediction might have very profound consequences for power devices implemented using InN/GaN/AlGaN material system.

Other important physical phenomena in quantum wells associated with the tail of the distribution function are inter-valley transfer, and real space transfer. In particular, the inter-valley transfer in the GaN-based quantum well should be less pronounced than in the bulk material. Therefore, the high-field drift electron velocity in quantum wells should be higher than in the corresponding bulk material.

2. Future Work

- We will further examine the role that the piezoelectric effect has on device design.
- We will develop a doped channel model in order to optimize the design of high-power GaN/AlGaN HEMTs.
- We will implement microwave models for power simulation and characterization both in AIM-Spice and in Libra.
- We will perform 2D simulations of AlGaN/GaN HEMTs.
- We will perform further detailed studies of 1/f noise in AlGaN/GaN HEMTs

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C. Electron Transport in GaN and Related Materials - Brian Foutz, Stephen O'Leary, and Michael Shur

The steady state and transient transport characteristics of a given semi-conducting material will ultimately dictate the performance of such a material in a device configuration. In order to establish these transport characteristics, the Monte Carlo simulation approach is often used. We have performed Monte Carlo simulations of electron transport in gallium nitride (GaN), indium nitride (InN), and aluminum nitride (AlN). We have also used several analytical methods to examine transport. We report on our steady-state results and on our transient transport results.

1. Steady-State Electron Transport

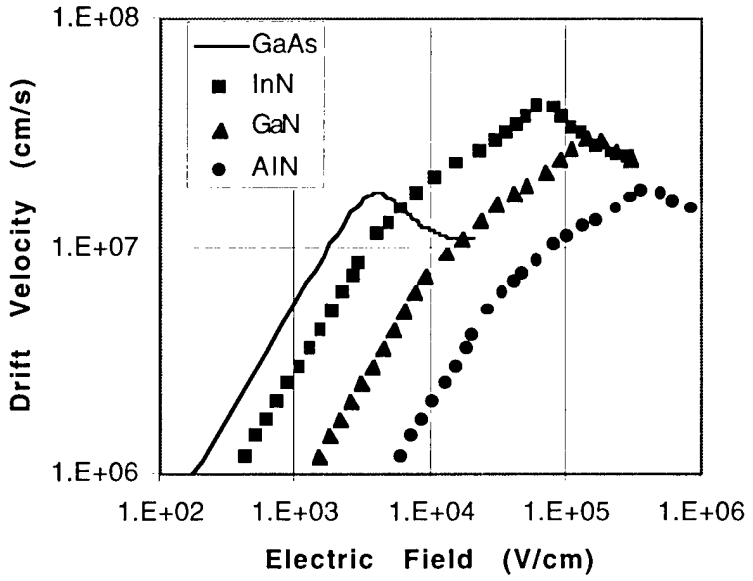

Figure 3 The steady-state velocity-field characteristics associated with GaN, InN, AlN, and GaAs. The GaAs plot is from J. M. Xu, *et. al.*, Appl. Phys. Lett. 49, 342 (1986).

We have determined the velocity-field characteristics of wurtzite GaN, InN, and AlN, using our ensemble Monte Carlo approach. In Figure 3, we contrast the characteristics associated with these materials with that associated with GaAs. For all cases, we set the temperature to 300 K and the doping concentration to 10^{17} cm^{-3}. We note that InN exhibits an extraordinarily high peak drift velocity, around 4.3×10^7 cm/s, at an electric field of 65 kV/cm. This represents one of the highest peak drift velocities ever reported for a III-V semiconductor. The sharp peak exhibited in the InN velocity-field characteristic contrasts dramatically with the broad peaks predicted for the GaN and AlN cases. In GaN, a peak drift velocity of 2.9×10^7 cm/s occurs at an electric field of around 140 kV/cm, while for AlN, a peak drift velocity of 1.8×10^7 cm/s occurs at an electric field of 450 kV/cm. It is noted that the drift velocity of InN exceeds that of GaN, or at the very least is close to that of GaN, for the entire range of electric fields considered, the saturation drift velocities of InN and GaN being comparable. While GaAs exhibits a much higher low-field mobility,

for comparable selections of temperature and doping, its peak drift velocity is only 1.7×10^7 cm/s, this peak occurring at a much lower electric field, 3.5 kV/cm.

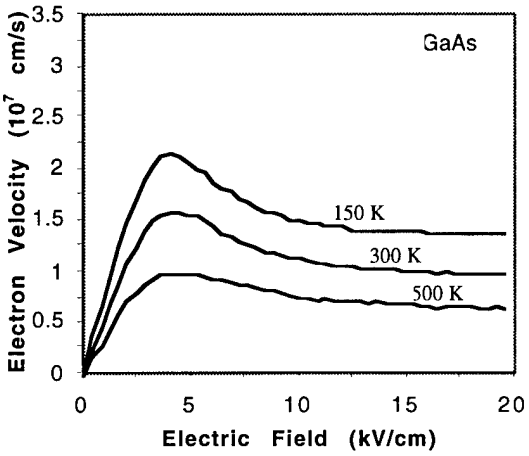

Figure 4 The steady-state velocity-field characteristic associated with GaAs at various temperatures.

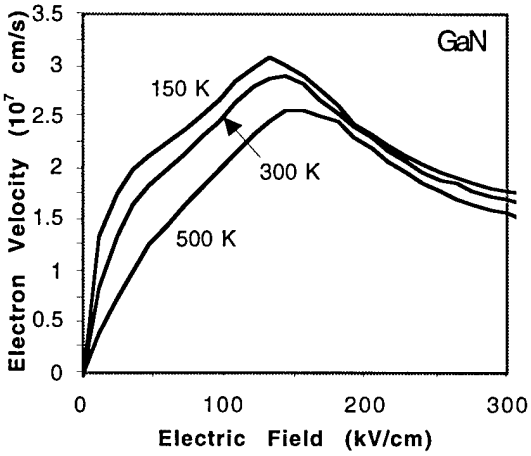

Figure 5 The steady-state velocity-field characteristics associated with GaN at various temperatures.

It is well known that temperature plays a decisive role in influencing the velocity-field characteristics of semiconductors. The dependence of the velocity-field characteristic of GaAs on temperature is well known. The peak drift velocity and the saturation drift velocity are found to decrease substantially with increased temperatures. Quantitatively, for a doping concentration equal to 10^{17} cm^{-3}, it is seen that the peak drift velocity at a temperature equal to 150 K is 2.2×10^7 cm/s, while that which occurs at 500 K is only 1.0×10^7 cm/s at 500 K; see Figure 4. The corresponding saturation drift velocity changes from 1.4×10^7 cm/s at 150 K to 0.7×10^7 cm/s at 500 K.

By way of contrast, the peak drift velocity associated with GaN only changes from 3.1×10^7 cm/s at 150 K to 2.5×10^7 cm/s at 500 K; see Figure 5. It is also seen that while the velocity-field characteristic associated with GaAs exhibits a dramatic change in form with variations in temperature, this is not observed for the GaN case. As with temperature, doping does not play as large a role in influencing the velocity-field characteristic of GaN as it does in GaAs. In particular, while the velocity-field characteristic associated with GaAs changes dramatically with dopant concentrations greater than 10^{17} cm^{-3}, for the case of GaN the dopant concentration must be in excess of 10^{18} cm^{-3} before substantial modifications in the velocity-field characteristic occur; see Figures 6 and 7.

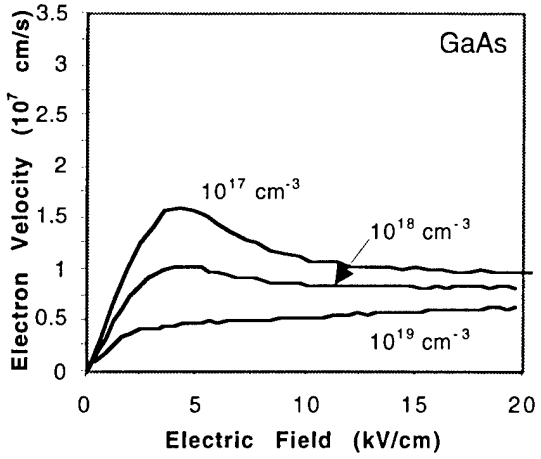

Figure 6 The steady-state velocity-field characteristics associated with GaAs at various doping concentrations.

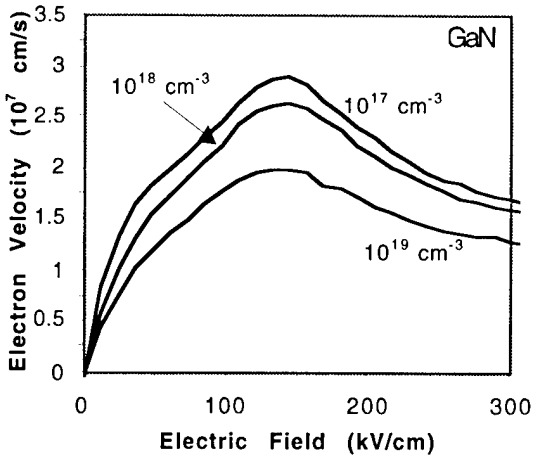

Figure 7 The steady-state velocity-field characteristics associated with GaN at various doping concentrations.

Our studies of electron transport have continued with AlN and InN. For both materials we find a similar robustness to temperature and doping, just as we found in the case of GaN. Figures 8 and 9 show the dependence of the velocity-field characteristic on temperature and doping concentration in AlN. Figures 10 and 11 show the temperature and doping concentration dependence in InN. Just like the case of GaN, we find InN and AlN are quite robust to chances in temperature and doping concentration.

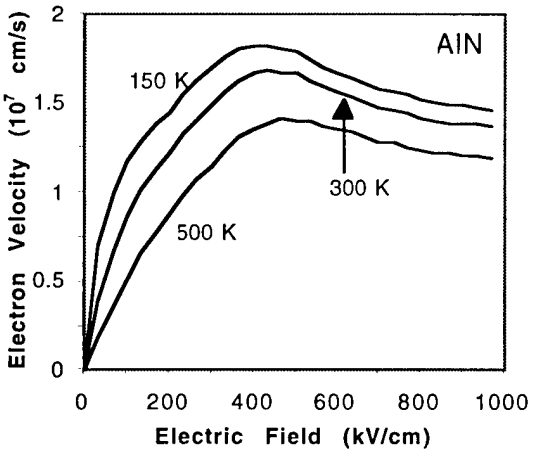

Figure 8 The velocity-field characteristics of AlN as various temperatures.

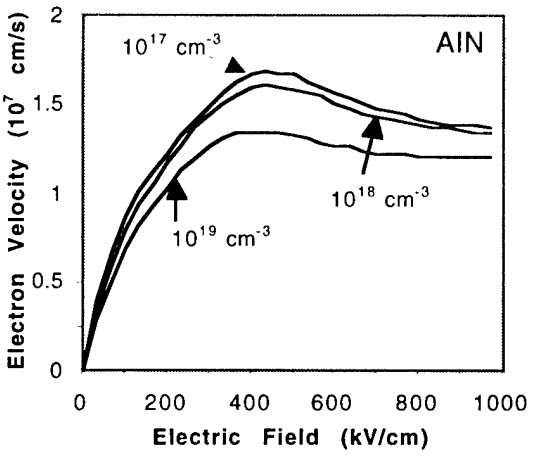

Figure 9 The velocity-field characteristics of AlN as various doping concentrations.

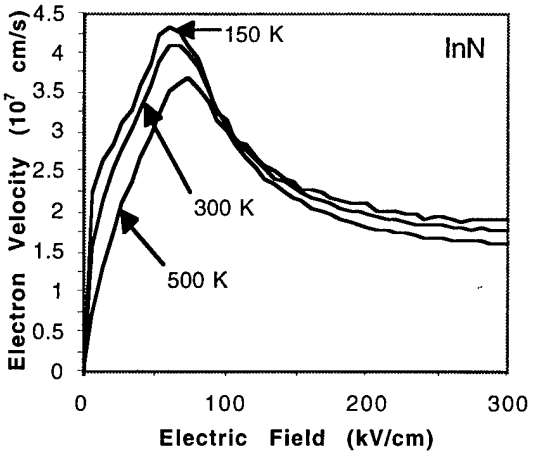

Figure 10 The velocity-field characteristics of InN at various temperatures.

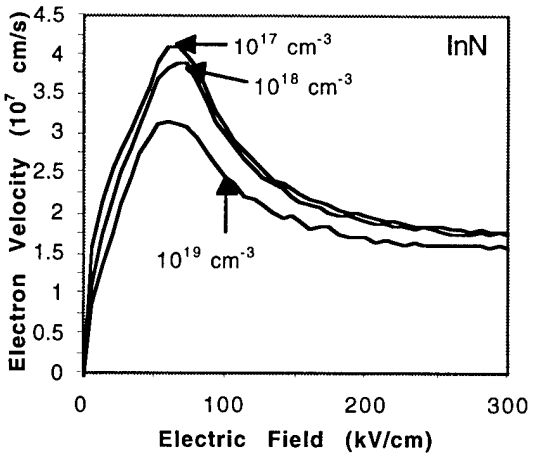

Figure 11 The velocity-field characteristics of InN at various doping concentrations.

To employ the Monte Carlo results into device simulations it is convenient to fit the resulting velocity-field characteristics to an analytical equation that can be used by device simulators such as Silvaco's Atlas. It has been found that a formula that fits the Monte Carlo results quite well is

$$v(E) = \frac{\mu_0 E + \mu_1 E(E/E_0)^{\alpha} + v_{sat}(E/E_1)^{\beta}}{1 + (E/E_0)^{\alpha} + (E/E_1)^{\beta}}.$$

When the temperature is set to 300 K and a doping concentration is set to 10^{17} cm^{-3} the parameters that fit the velocity-field curves for GaN, InN, and AlN are

	μ_0 (cm^2/Vs)	μ_1(cm^2/Vs)	E_0 (V/cm)	E_1(V/cm)	v_{sat} (cm/s)	α	β
GaN	720	234	3.36e4	9.80e4	1.40e7	2.44	7.45
AlN	129	32.5	1.18e5	3.43e5	1.33e7	1.58	6.88
InN	2620	762	1.31e4	4.02e4	1.74e7	2.48	6.80

At the 1998 American Physical Society Condensed Matter Spring Meeting and at the 1998 Materials Research Society Spring Meeting a one-dimensional model which provides insight into electron transport in the III-V nitrides was presented. This analytical model examines the balance between the energy gained from the applied field and the energy lost due to polar optical phonon scattering. In particular, we demonstrate that beyond a certain critical field that the energy gained from the field exceeded that lost due to scattering. This instability leads to a sharp increase in the average electron energy. Eventually, however, when the average electron energy approaches the inter-valley energy

separation, inter-valley scattering reestablishes equilibrium. We believe that this effect is the primary factor responsible for inter-valley transitions in the III-V nitrides and the III-V semiconductors, in general.

Transient Electron Transport and Overshoot Effects. As device dimensions shrink, short channel effects, such as electron velocity overshoot, become more important. Velocity overshoot occurs when the electric field changes faster than the relaxation time of the electron distribution. During the time it takes for the electron distribution to return to steady state, the transient drift velocity can exceed, by a factor of three or more, the steady-state drift velocity. These transient effects typically last for several picoseconds, which is enough time for the electron to travel several tenths of a micron. Our approach is to study and characterize these effects though Monte Carlo electron transport simulations. It has been shown that the nitride materials potentially demonstrate velocity overshoot and transient effects even more pronounced than those that occur in GaAs. In the nitrides, however, these effects occur at much higher applied biases than in GaAs. Therefore, we expect these effects to be important in high power, high frequency devices, such as those needed for this project.

In Figure 12, we examine velocity overshoot in InN, GaN, AlN, as well as GaAs. In all cases we set the temperature to 300 K and the electron doping concentration to 10^{17} cm^{-3}. To provide a reasonable means of comparing transient effects among the materials, the electric field is increased from 0 kV/cm to twice the peak field for that particular material. Note that the overshoot effects in InN have a higher velocity and extend over greater distances than all the other materials. AlN on the other hand has very small overshoot effects. This can be directly related to AlN's very short energy relaxation time and to AlN larger effective mass.

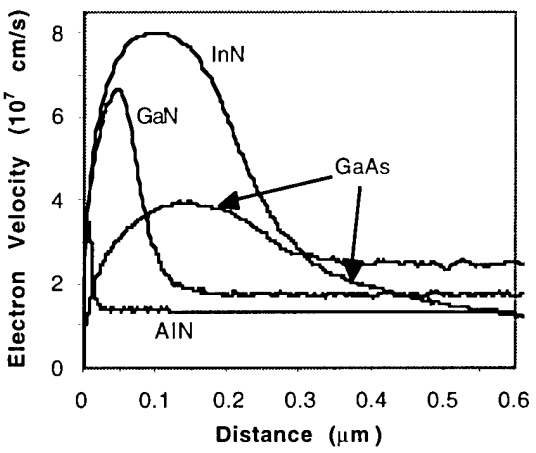

Figure 12 A comparison of the overshoot effects in the III-V nitrides and GaAs. The applied fields in GaN, InN, AlN, and GaAs are 280, 130, 900, and 8 kV/cm, respectively.

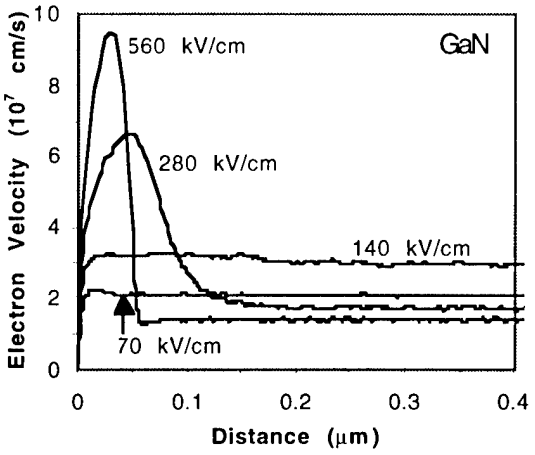

Figure 13 Velocity overshoot in GaN at various applied fields.

In Figure 13, we examine the effect of increasing the applied field from zero to a variety of final field strengths in GaN. GaN, which demonstrates a peak in the steady-state

velocity-field characteristics field value of 140 kV/cm, also does not demonstrate overshoot effects until the applied field is increased beyond this value. When the applied field is increased from zero to a value below 140 kV/cm, very little or no overshoot occurs. Just above the peak field, we find that the peak overshoot velocity is not very high. As the applied field is increased from 280 kV/cm to 560 kV/cm, the maximum overshoot velocity increases from 6.6×10^7 cm/s to 9.5×10^7 cm/s. However, the distance for overshoot decreases, from approximately 0.2 micron at 280 kV/cm to only 0.05 micron at 560 kV/cm

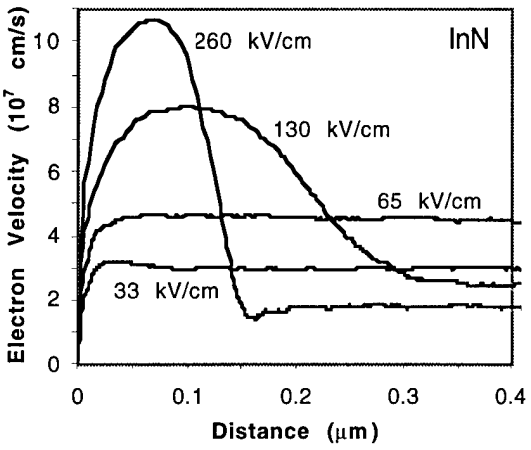

Figure 14 Velocity overshoot in InN at various applied fields.

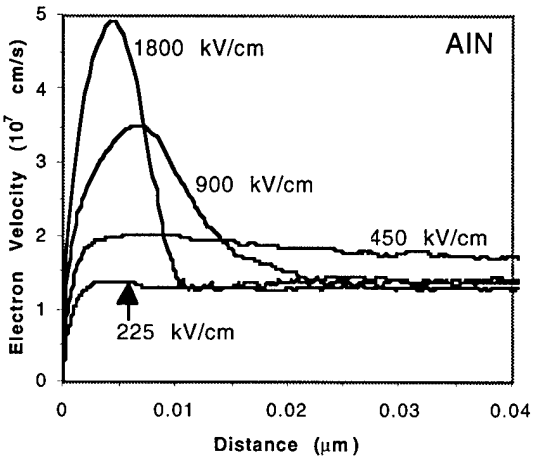

Figure 15 Velocity overshoot in AlN at various applied fields.

Transient effects in InN and AlN have been investigated further. As can be seen in Figures 14 and 15, we find many similarities to the overshoot properties of GaN. First, in both InN and AlN overshoot effects do not begin until the applied field is increased to a value beyond the field that yields in peak in the steady-state velocity-field characteristic. In InN, overshoot effects are not seen until the field increases past 65 kV/cm and in AlN overshoot effects are not seen until the field increases beyond 450 kV/cm. As noted earlier, the overshoot effects in InN are much larger than both GaN and especially AlN.

In InN, when the field is increased to 600 kV/cm in InN the peak velocity increases to 1.2×10^8 cm/s while the overshoot effects shorten to a distance of 0.1 micron. These results, along with InN large steady-state velocities (see Figures 9 and 10), suggest that using InN in the channels in field effect transistors could enhance performance over GaN based counterparts. These results were presented at the Fall 1998 Materials Research Society Spring Meeting.This year we have also studied heterojunction injection. As an electron passes over a drop in the conduction band its kinetic energy increases. This situation occurs, for example, when electrons travel from an alloy such as $Al_xGa_{1-x}N$ to GaN. The initial electron energy and velocity is very high upon entering the GaN, however, scattering quickly returns the electrons to a steady-state condition with the usual electron velocities. In Figure 16 we examine the effect of different injection energies and assume there is a local electric field of 140 kV/cm.

We see in all cases the extra velocity is quickly removed by scattering. However, there is a trade off as the injection energy is increased. Although the initial electron velocity is higher at higher injection energies, the time to return to steady-state occurs faster.

Indeed, at 2.0 eV there is even an "undershoot" effect as the average electron velocity briefly drops below its steady-state value. One may wonder if the overshoot effects that higher local electric fields bring will help the situation. In Figure 17 we show the results of setting the local field to 280 kV/cm. We see that at 0.5 and 1.0 eV, the electron velocity remains higher longer, but in all cases the steady-state electron velocity is achieved even faster. One alternative to studying transient electron transport with computer intensive Monte Carlo simulations is to use a semi-analytical energy-balance method. The details of this method and the results specifically dealing with the nitrides have been presented at the American Physical Society Condensed Matter Meeting, in March of 1998 as well as the Materials Research Society Spring Meeting 1998. As can been seen in Figures 18 and 19, reasonable agreement with Monte Carlo results can be obtained, but with significant savings in computer resources.

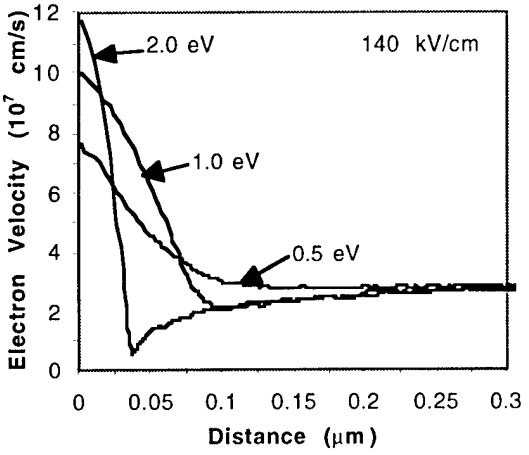

Figure 16 Heterojunction injection at various heterojunction step sizes with a local applied field of 280 kV/cm.

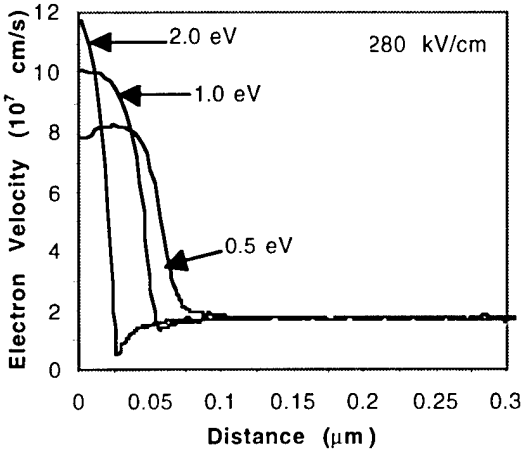

Figure 17 Heterojunction injection at various heterojunction step sizes with a local applied field of 140 kV/cm.

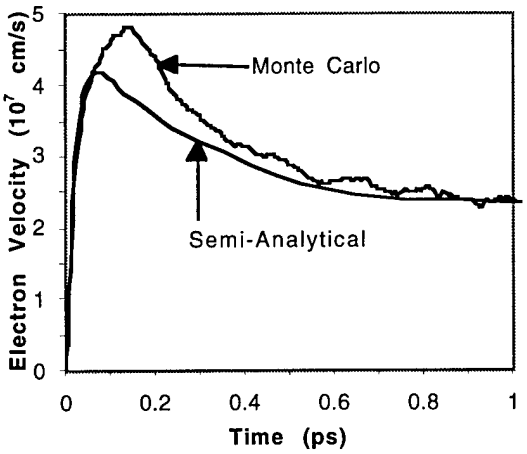

Figure 18 A comparison of Monte Carlo results and the semi-analytical method. In both cases the applied field is set to 200 kV/cm.

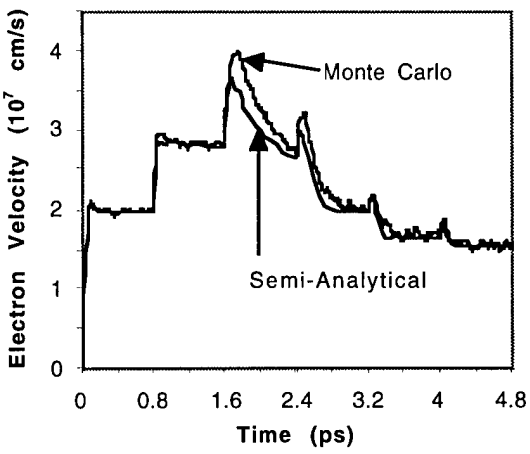

Figure 19 A comparison of Monte Carlo results and the semi-analytical method for an increasing applied field. A 60 kV/cm is applied at t=0 and is increased by 60 kV/cm every 0.8 ps.

2. Future Work

- To determine the effect of some of the lesser-known parameters on the velocity-field characteristics of GaN, InN, and AlN, we have started to examine the sensitivity of our results to variations in these parameters. This analysis should allow us to better understand the differences between the Monte Carlo predictions and experimental results.
- In MODFETs and quantum well transistors, where 2-D transport is important, mobility values over 2000 $cm^2/V\text{-}s$ at 300 K have been measured. It is currently uncertain why mobility values in the 2-D gas are so much higher than those predicted for bulk material, 1000 $cm^2/V\text{-}s$.
- Alloy scattering will be implemented into the Monte Carlo code and and the velocity-field characteristics of the alloy $Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$ will be determined.

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D. Analysis of Schottky Gate Electron Tunneling in Spontaneous and Piezoelectric Polarization, Ga-faced, Wurtzite, Ni/$Al_xGa_{1-x}N$/GaN HEMTs - Andrej Sierakowski and Lester F. Eastman

1. Abstract

Through simulations [2,3,8,9,11] we present calculated increase of gate leakage current associated with increasing mole fraction of aluminum in the $Al_xGa_{1-x}N$ layer of an Ni/$Al_xGa_{1-x}N$/GaN Ga face, wurtzite heterostructure in the pinchoff condition. The dominating current transport [4,13] mechanism is asserted to be thermionically assisted electron tunneling through the Schottky barrier. The structures considered in this letter have conduction band profiles modulated by Spontaneous and Piezoelectric polarization effects alone [7,10]. The WKB method [5, 12] is used to calculate the gate current in pinchoff. This method is seen to yield the trend that increasing the mole fraction of aluminum in the $Al_xGa_{1-x}N$ layer increases the gate leakage in the pinchoff condition. Higher gate leakage in turn results in undesirable, lower, power gain. Notation: x denotes the aluminum mole fraction in the $Al_xGa_{1-x}N$ layer. 2DEG denotes the two dimensional electron gas at the $Al_xGa_{1-x}N$/GaN interface.

2. Introduction

A general assumption found in the literature is that increasing the mole fraction, of aluminum in the AlGaN layer of Piezoelectric-HEMTs decreases the gate leakage current in pinchoff. This is in fact not the case. Increasing increases the sheet charge density at the AlGaN/GaN interface hence increasing the compensating 2DEG concentration present in equilibrium. To pinch-off, deplete, this 2DEG a larger electric field must be impressed via an negative applied bias to the gate with respect to the electron channel.

3. Simulations

Figure 20 below shows the structure under consideration and the associated conduction bands in the pinchoff condition for = 0.05, 0.25, 0.45. Figure 20 below shows the charge sheet concentration at the AlGaN/GaN interface due to Spontaneous and Piezoelectric polarizations for Ga faced material vs. the mole fraction of aluminum in the $Al_xGa_{1-x}N$ layer. Figure 22 below shows the total gate leakage current, J_g, due to thermionic emission over the barrier, J_E, and thermionically-assisted electron tunneling, J_T, giving a total of four current components contributing to Jg:

$$j_g = j_{E,ms} + j_{E,sm} + j_{T,ms} + j_{T,s} \quad (1)$$

The suffix, ms, denotes metal to semi-conductor, sm; semiconductor to metal. In pinchoff, the current component most dominant in J_g is J_{Tms}, the tunneling current through the barrier from metal to semiconductor.

Additional information contained in Figure 22 is:

- The two sets of curves correspond to lattice temperatures T = 300K, and 573K.
- The suffix WKB means that the thermionically assisted tunneling component of the gate current was computed using the WKB approximation.
- The top horizontal axis has values of the barrier width of the conduction band profile in the AlGaN associated with each Al concentration fraction on the lower axis.

The barrier width is defined to be in line with the fermi level in the metal = 0 eV in the right hand plot of Conduction Band Energy vs. distance in Figure 19.

4. Results and Discussion:

a) In Figure 20 increasing the aluminum fraction in the barrier layer (AlGaN) causes the barrier width at the OV Fermi energy to narrow, and the barrier height to increase. The dominant effect is the barrier with which causes increased gate leakage from metal to semiconductor in pinchoff.

b) In Figure 20 = 0.15 = 15% is the minimum value allowable if the electron mobility is to be maintained without degrading transistor performance, for frequencies of interest = 4 - 12 GHz. = 0.35 = 35% is the maximum allowable value without having structural failure [1] of the AlGaN/GaN metallurgical junction where the 2DEG forms and is responsible for current and hence power amplification by the device in Figure 20.

c) From Figure 22 The calculations for gate leakage yield the result: For every 0.2 = 20% increase in the gate leakage increases by an order of magnitude or more for temperatures as high as T = 573K or even more dramatically for room temperature T = 300K operation.

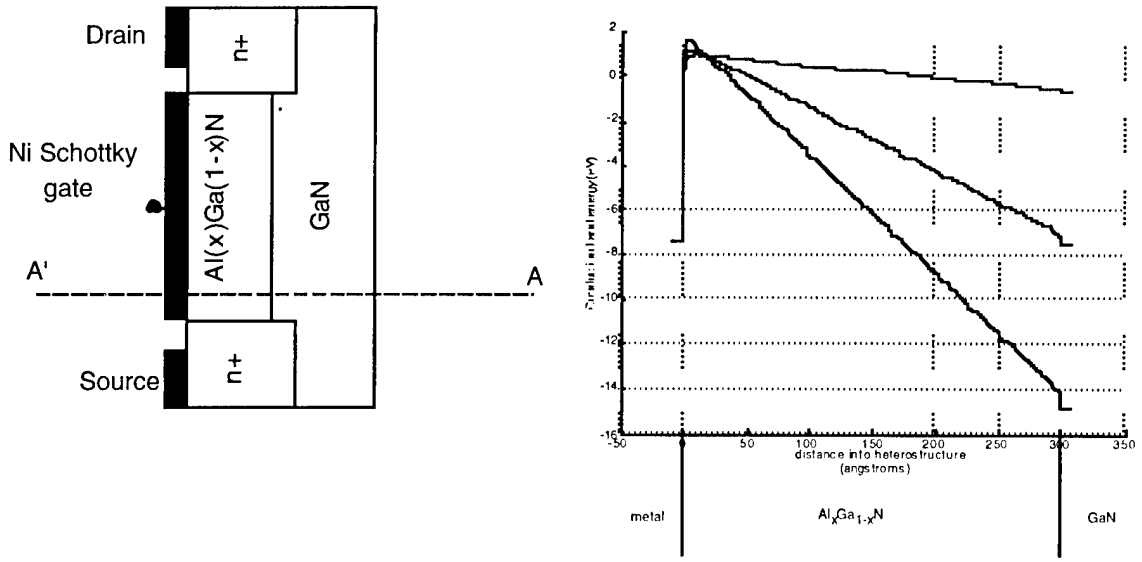

Figure 20 Left figure is the heterostructure for which gate current is simulated to flow along cross-section A'A. Right figure corresponds to conduction band profile for various mole fractions of Al in the $Al_xGa_{1-x}N$ layer in pinchoff. Top of barrier rounded off due to Schottky image charge lowering.

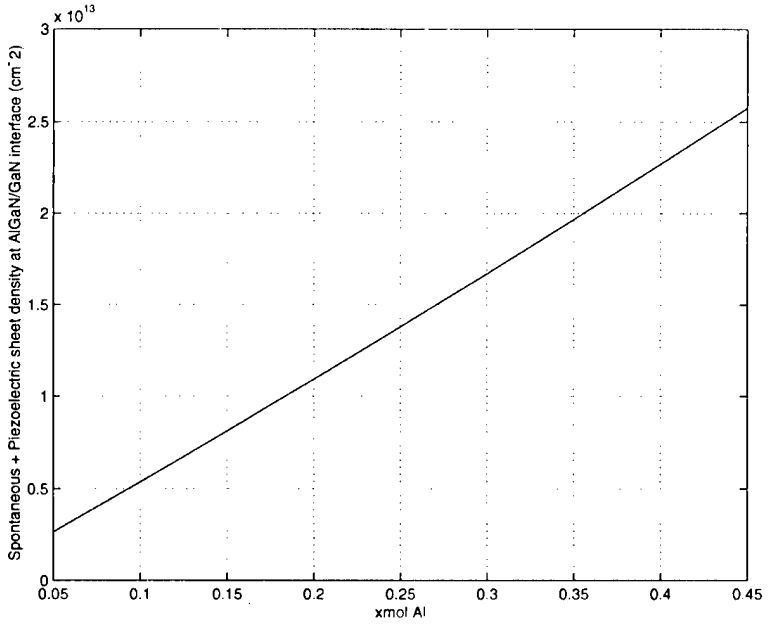

Figure 21 Sheet concentration of charge at the $_AI_xGa_{1-x}N$/GaN interface due to spontaneous plus piezoelectric effects vs. mole fraction of aluminum. At equilibrium the 2DEG (two dimensional electron gas) concentration will be similar in magnitude to the sheet density plotted above.

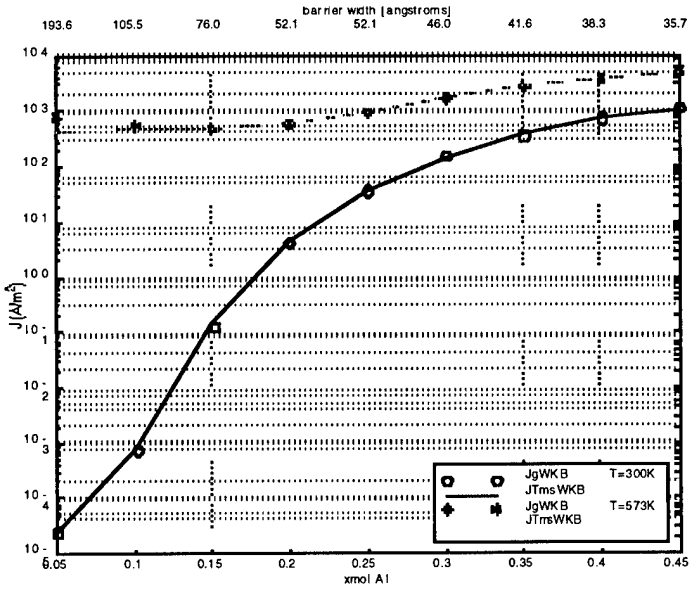

Figure 22 Total gate current, Jg, and dominant component from metal to semiconductor J_{Tms}, for two temperatures, T= 300 K and 573 K. through the $Al_xGa_{1-x}N$ barrier.

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E. GaN Fundamental Physics - B.K. Ridley

1. Low-Field Transport Theory

The main achievement was the development of a theory of low-field transport in n-GaN. The room-temperature mobility associated with polar-optical-phonon (PO) scattering was calculated by solving the Boltzmann equation using an exact method. It was found to be 2,200 cm^2/Vs ($m^* \geq 0.22\ m_0$) or 2,500 cm^2/Vs ($m^* = 0.20\ m_0$). The effect of increasing electron density into the degenerate regime was explored, and it was shown that the mobility dropped significantly [1]. A study of the effect of electron-electron scattering showed that electron-electron scattering tended to counteract the drop in mobility and it was concluded that the variation of mobility with increasing degeneracy was not large. A comparison of the predictions two simple analytic models of mobility with the exact result was also made [2].

2. Theory of Elastic Strain

The theory of elastic strain in adjacent lattice-mismatched layers was reviewed. The piezoelectric fields generated in the AlN/GaN and AlAs/GaAs systems were calculated for two cases a) a free-standing superlattice and b) a thick substrate [3]. An analytical model for the induced electron density was developed.

3. Yellow Luminescence

The problem of the origin of the yellow luminescence in GaN was briefly addressed. It was shown that the broad bandwidth was consistent with a polar-phonon coupling having a Huang-Rhys factor of 6.5 associated with a center situated about 0.6 eV above the valence band [4].

4. Phonon Modes in AlGaN/GaN Quantum Wells

A project put very much on the back burner was the description of phonon modes in a GaN quantum well. In the $Al_xGa_{1-x}N$/GaN system, unlike the AlAs/GaAs system, the frequencies of the optical modes in the barrier ovelrap with those in the well, thus reducing the degree of phonon confinement. In order to describe the hybrid and interface modes in this system it is necessary to solve the tough problem of boundary conditions for optical modes, something that has never been done accurately.

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V. Wide Bangap Semiconductor Materials Synthesis

A. Summary - L.F. Eastman

High-resistivity Vanadium-doped SiC, as well as N^+ SiC have been delivered to Cornell by Northrop-Grumman. 10^{15} Ω-cm at room temperature, and nearly 10^8 Ω-cm at 500°K have been measured by them on the high-resistivity SiC. The bulk GaN growth effort at Cornell is continuing, using high purity GaN powder grown at Cornell, and using thick HVPE grown material as a seed. Bulk growth using the pure GaN powder, and the thick HVPE GaN seed, is expected during the next year. The MBE growth has had outstanding advances. The importance of, the means of obtaining, and the characterizing of the proper Ga-face polarity have been established. Using piezoelectric and related polarization, with no doping, an electron mobility of 1232 cm^2/V-s with ~ $1.5 \cdot 10^3/cm^2$ electron density were obtained. The structure used had a thin GaN top layer, used as a piezoelectric barrier to reduce the electron tunneling current from the gate metal into the channel.

The OMVPE growth on SiC yielded 1,505 cm^2/V-s electron mobility with electron sheet density above $1 \cdot 10^{13}/cm^2$. DC and microwave conductance in the nucleation and buffer layers were problems with some growth parameter values, but not with others. The susceptor has been modified to hold eight two-inch wafer to increase throughput.

Finally, the UHV STEM studies have been used to study dislocations, and using EELS, states in the forbidden gap have been found at the dislocations. The high resolution STEM will be used to study the planarity of the heterojunction, along with the growth polarity.

B. Semi-insulating Silicon Carbide Wafers – Augustine and R. N. Thomas - Northrop Grumman STC

1. Introduction

In support of Cornell's Multidisciplinary Research Initiative Program to develop high power microwave transistors based on GaN and related compounds, the Northrop Grumman Science & Technology Center had proposed the following tasks:

- Provide single crystal 4H-SiC substrates for the development of GaN/AlN epitaxial growth technology on SiC substrates, and
- Design and fabricate microwave power transistor structures for use at frequencies up to X-band (10GHz) utilizing GaN-based epitaxial profiles provided by Cornell.

The goal of this program is to provide conductive and semi-insulating SiC substrates for the development of high quality GaN/AlGaN epitaxial structures and microwave devices at Cornell University. Since the beginning of this program eight SiC crystals have been grown most of which were semi-insulating material. From these growths total substrate area delivered to date equals that of 26 wafers of 1.375 inch

diameter which includes four semi-insulating 4H-SiC wafers and eleven semi-insulating 6H-SiC wafers. The rest of the material delivered were low resistivity n^+ and some high resistivity (200 to 2000 Ω-cm).

2. Program Spending vs Plan

As of September 1, 1998, about $160,000.00 has been spent from $200,000.00 allocated for this program. The remainder of the funding is expected to be spent by the beginning of October on growth, processing, and characterization of semi-insulating crystals for the final delivery of this program.

The spending plan for this program is shown in Figure 1.

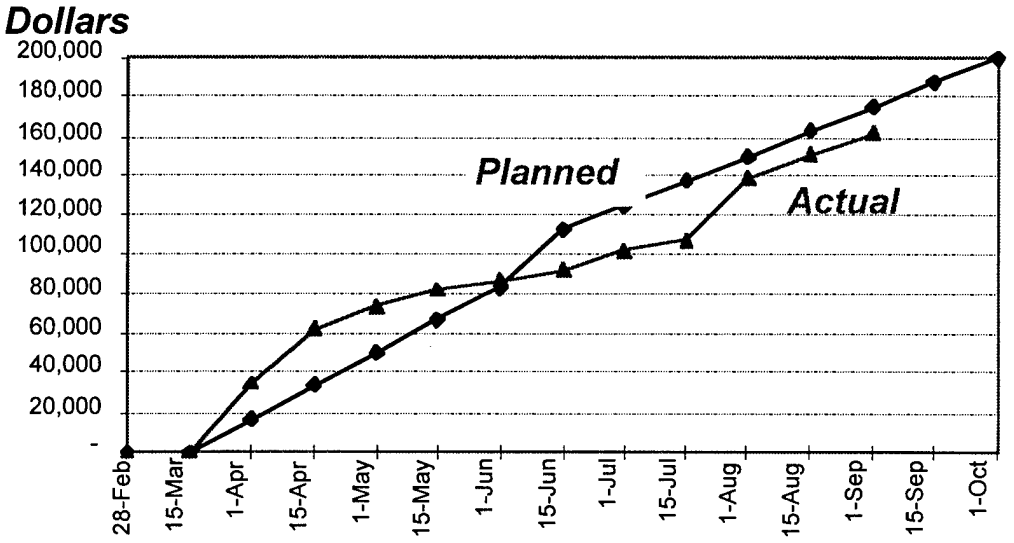


Figure 1 Actual spending vs Planned spending for the MURI program

3. Technical Progress

Significant progress was made with respect to crystal growth and material characterization during the course of this program.

4. Crystal Growth

Monocrystalline silicon carbide material was grown by the physical vapor transport (PVT) technique in which growth proceeds by the sublimation of a SiC source and deposition of the vapor species upon a high quality SiC monocrystalline seed wafer in an ultra-high purity inert ambient. N^+ crystals are prepared by adding controlled amounts of high purity nitrogen to the inert ambient. Undoped crystals are usually p-type due to residual boron in the starting source material which is known to create a shallow acceptor level in SiC. The resistivity of the undoped material varies in the range of 10^2 to 10^3 Ω-cm due to the variability in the contamination level of boron. To produce semi-insulating behavior, the SiC crystals have been intentionally doped with vanadium, which introduces

a deep-donor state lying near the middle of the band gap and compensate the acceptors due to residual boron. A significant increase in the resistivity of these vanadium-doped crystals is observed, as shown in Figure 2. Since direct measurements of the resistivity near room temperature are complicated by the exceedingly high sample resistance and spurious surface leakage effects, temperatures in the 160 to 470 °C range were used. A linear fit of the data over this temperature range yields an activation energy of approximately 1.48 eV, consistent with the expected energy of the vanadium deep-donor level. The extrapolated resistivity at 300 K is in the range of 10^{15} Ω-cm.

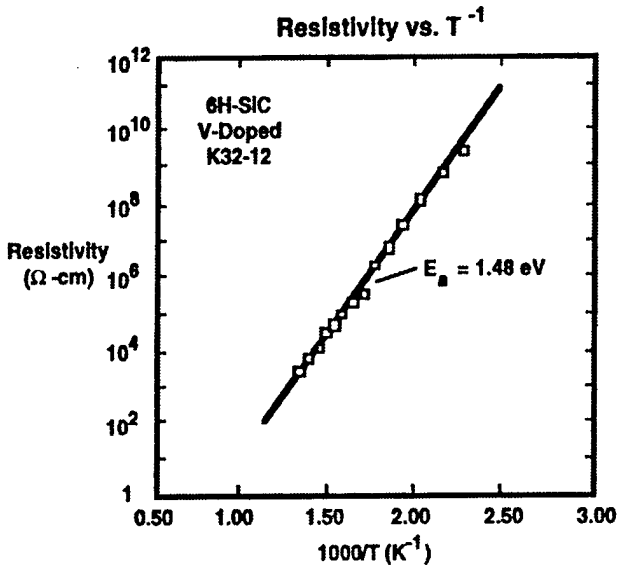


Figure 2 Resistivity as a function of reciprocal temperature for vanadium doped 6H-SiC

Since the beginning of this program eight SiC crystals have been grown most of which were semi-insulating material. From these growths total substrate area delivered to date equals that of 26 wafers of 1.375 inch diameter which includes four semi-insulating 4H-SiC wafers and eleven semi-insulating 6H-SiC wafers. The rest of the material delivered were low resistivity n^+ and some high resistivity (200 to 2000 Ω-cm).

5. Material Characterization

The substrate material is regularly characterized with respect to surface quality, micropipe density, and other crystallographic defects after growth and processing.

The quality of the wafer surfaces is routinely assessed after final polish and cleaning by dark field Nomarski optical microscopy under to ensure there are no residual scratches and pits on the wafer surface. Cross-sectional TEM, performed on selected wafers after final polish, revealed surface damage of less than 10 nm with no microcracks. The wafer thickness is also measured at several locations to check for taper in the wafer. The variations in the wafer thickness is usually under 5 mils. Process improvements are under way to further decrease the variation in the wafer thickness.

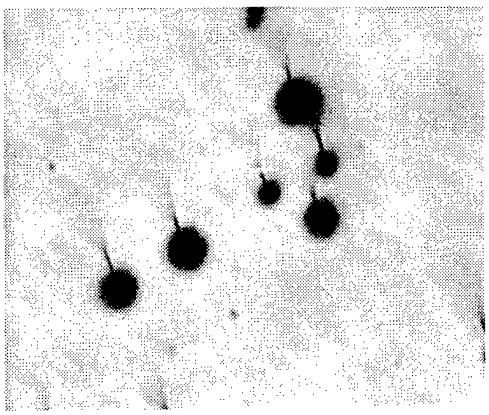


Figure 3 Precipitates formed during growth nucleate micropipes

Micropipe density of the wafers were determined using transmission optical microscopy and also by KOH etch. We have been successful in significantly reducing the micropipe density in our n^+ SiC crystals to about 2 cm^{-2} in the best material. However, in the semi-insulating material we noticed a significant increase in micropipe density. This was caused by the addition of vanadium during crystal growth to increase the resistivity of the material. It was determined that excess vanadium precipitated as vanadium-silicide or vanadium-carbide in the crystal and these precipitates acted as nucleation sites for the formation of micropipes as shown in Figure 3.

To prevent formation of precipitates the amount of vanadium used during crystal growth was decreased. However, if the amount of vanadium incorporated in the crystal is less than the level of residual boron, the resulting crystal is p-type. This results in lower yield of semi-insulating material. We have been successful in controlling the amount of vanadium doping necessary to produce high quality semi-insulating material. Typical micropipe density in the semi-insulating wafers is in the range of 100 to 500 cm^{-2}.

6. Future Plan

In the third year of this program we will deliver only semi-insulating 6H-SiC material. These wafers will be oriented along the <0001> c-axis direction. Also, we will focus on reducing the micropipe density of the semi-insulating to approach that of our n+ SiC material.

C. GaN Bulk Crystal Growth - A. Ruoff

Our program is a three step process with the final step being the growth of quality single crystals of GaN by the nutrient growth method. The first step, to produce high purity GaN powder, has been completed. The second step, to produce seed crystal by CVD has been successful but is not yet complete. The final step, to produce crystals by solution growth with a suitable solvent is underway.

1. Nutrient Syntheses

The motivation for us to synthesize GaN powder was based on the fact that no high purity GaN powder is commercially available. We did elemental analysis on GaN powder samples from two different companies. The N to Ga molar ratio is very much less than one and there are many other impurities, which makes them not ideal to be the nutrient for solution growth. We made high purity GaN powder with Ga and Li metal mixture at ~900° C under flowing NH_3 (Figure 4).

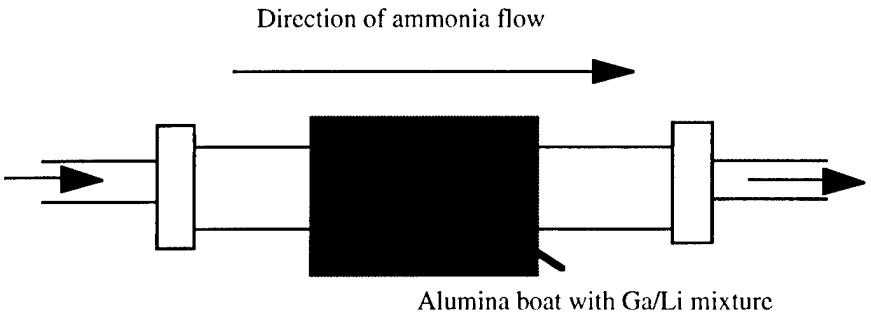


Figure 4 GaN powder synthesis apparatus

Lithium metal works as a fixant for the nitrogen-containing species. Mixing methods include physically mixing two metals and forming Ga-Li alloy. The most successful experiment used a Li: Ga non-alloyed mixture in a 1:1 ratio. At 1000 _C over 24 hr, the yield was 84%. The GaN was crystalline and the chemical composition was perfectly stoichiometric within the inherent error of the analysis method (Table 1). At the same time, the materials was white, demonstration purity greater than available commercial product. The particle size was on the order of 1 μm.

Element	Calculated	Our powder	Company A	Company B
Ga	83.3%	83.4%	83.8%	83.4%
N	16.7%	16.7%	15.4%	11.9%
Li	0 %	<0.05%	<0.05%	<0.05%
Al	0 %	<0.05%	<0.05%	<0.05%
Si	0 %	0.04%	0.03%	<0.03%

Table 1 Elemental analyses for various gallium nitride syntheses

It was concluded that the free lithium was fixing liquid ammonia (observed at room temperature) and forming a lithiated ammonia species as the temperature increased. This material and gallium interacted at a phase boundary, allowing small-scale crystal growth on the interfacial surface without mixing, thus forming small, lithium-free crystallites of Gallium Nitride. The paper is in press in the Journal of Chemistry Materials.

2. GaN seed crystal growth by CVD method

There are two reactions that occur in this CVD process. Helium gas is used as HCl carrier gas. During this CVD process, ultrahigh purity gases are used. Figure 5 shows the CVD process apparatus.

$$(1)\mathrm{HCl(g)} + \mathrm{Ga(l)} \rightarrow \mathrm{GaCl(g)} + \frac{1}{2}\mathrm{H_2(g)}$$

$$(2)\mathrm{GaCl(g)} + \mathrm{NH_3(g)} \rightarrow \mathrm{GaN(s)} + \mathrm{HCl(g)} + \mathrm{H_2(g)}$$

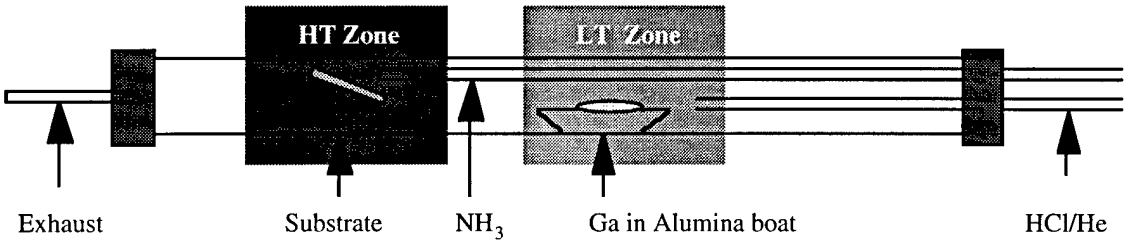


Figure 5 Schematic of CVD process apparatus

Gallium nitride was grown by the reaction of gallium chloride and ammonia flowing over a substrate. We usually choose sapphire (0001) wafer as the substrate for GaN growth. Tungsten (001) crystal and fused quartz plate, as well as sapphire (11-20) were also used as substrates. Crystal growth occurred over several hours (7-24hr.) with the high T zone at 1050°C to 1150°C and the low T zone at ~900°C.

The materials was grown as polycrystalline masses of hexagonal crystals. They appeared to be highly reflective and black in color due to internal cracking. The powder of these crystals shows color of from light to dark yellow. Compositional analysis gave perfectly stoichiometric result within the inherent error of the analysis method. The largest measurable crystal facet was a 3 mm x 1 mm prismatic face. The largest separable crystal was about 1 mm across its hexagonal basal plane. Rocking curve analyses for all CVD experiments show crystal perfection to be similar to that reported in the literature (90 arcsec FWHM). It has been concluded that crystal size is dependent mainly on the time of the experiment. Crystal size was drastically improved by tripling the run time from 8 to 24hr. The CVD process is easy to perform and is a very promising method for the supply of seed crystals on the millimeter scale.

We will continue to optimize experimental factors such as zone temperatures, flow rates of the reaction components. Geometrical concerns about the substrate holder need to be addressed. Several modifications have been made to minimize nucleation sites. Different substrates such as sapphire sputtered with AlN and sapphire with a GaN film grown by MBE will be used in further CVD reaction.

3. Future Approaches on Boule Growth

We have accomplished high purity GaN powder syntheses and GaN seed crystal growth. Work will continue on the boule growth.

The 3rd step, which is also the final step in our plan, will be solution-based GaN nutrient growth. This process is reintegration of the materials at a seed crystal, in a controlled fashion in order to produce gallium nitride boules. We chose lithium nitride (Li_3N) as solvent for crystal growth because lithium nitride is the only nitride that will melt under 1 atm N_2 atmosphere below GaN decomposition temperature. We have performed experiment that proved that GaN dissolves in Li_3N. The possible inclusion of Li is not a problem, because it can be removed by heat treatment. Boron nitride (BN) is used as reaction container due to its inert chemical property. TZM pressure vessels are used as pressure vessel under high-pressure growth. Currently this final step is being scrutinized. Temperature is the critical parameter so we will conduct further calibration on our system. We will also alter the pressure inside of container by adding hydrazine (N_2H_4) etc. to change the equilibrium condition for the crystal formation. From the knowledge gained and the developments of the past year, we are confident that we will succeed in growing GaN boules.

D. MBE growth of GaN for HFET applications - William J. Schaff, Michael Murphy, Tyler Eustis, Hong Wu, Wesley Yeo, Oliver Ambacher, Ken Chu, and Bruce Green

Progress in the MBE growth of GaN for HFETs has been substantial. The following milestones are all accomplishments within the last year:

- High mobility GaN 2DEG structures – 1,232cm^2/Vsec at 300K, 3,180cm^2/Vsec at 77K.
- Development of rules for polarity control of piezoelectric 2DEG structures.
- Microwave HFETs grown by MBE.

The present focus is on optimization of mobility, realization of low gate currents through GaN cap layers, and supply of reproducible quantities of wafers for amplifier demonstration. Optimization of growth on SiC has not begun.

Nucleation layer	Polarity	2DEG
GaN	N-face	Inverted
OMVPE GaN	Ga-face	Normal
AlN	Ga-face	Normal
AlGaN	Ga-face	Normal
Si-face SiC	Ga-face	Normal

Table 2 Effect of nucleation on growth polarity and interface for 2DEG

The key to moving from failure to successful growth of high mobility GaN 2DEG structures is understanding the importance of growth polarity on AlGaN/GaN properties.

We have verified experimental proof of theory for polarity dependence on piezoelectric charge two-dimensional gasses. A summary of results is seen in Table 2. The piezoelectric 2DEG required for this MURI program comes from AlGaN on GaN (the "normal" structure). This structure only produces a 2DEG when growth takes place in the Ga-face polarity.

Ga-face polarity is controlled by the nucleation layer grown on sapphire (or face of SiC substrate). The polarities shown above are observed in the RHEED patterns of GaN prior to depositing AlGaN which forms the carrier confining interface. Hundreds of wafers have been grown with the N-face polarity during the last 2 years. Not one exhibited a 2DEG for a normal structure. In contrast, every successful normal 2DEG structure was grown with Ga-face polarity. There has not been a single violation of these rules observed.

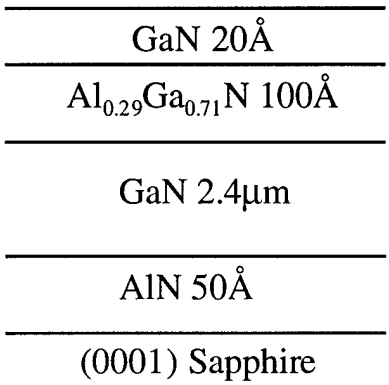


Figure 6 HFET grown by MBE at a growth rate of ~0.5μm/hr, substrate temperature ~800°C (GaN) and 850°C (AlGaN), RF power 350W, N_2 flow ~1.2 sccm

These observations resulted from the first attempts to grow a normal 2DEG GaN structure by MBE on a GaN layer prepared by OMVPE at Cornell. The RHEED pattern for a Ga-face growth polarity was seen here the first time. The first attempt to grow a normal HFET on these OMVPE buffers resulted in the first successful GaN 2DEG grown by MBE at Cornell.

The first attempts to create Ga-face polarity entirely within by MBE machine then were successful. Ga-face polarity was easily established with a 50 Å AlN buffer grown at the same nominal substrate temperature (800°C) as GaN. The HFET structure that exhibited the highest Hall mobility is seen in Figure 6.

At 300°K, the Hall mobility is 1,232cm^2/Vsec and at 77K mobility is 3,180cm^2/Vsec. When the GaN buffer thickness is reduced to 0.7μm, mobility falls by approximately 15%. Electron sheet density from both Hall and CV measurements is $1.5x10^{13}$ cm^{-2}. This value agrees with expected piezoelectric charge concentrations in this entirely undoped structure. A CV profile for this structure is seen in Figure 7. Analysis of this data indicates very low background carrier density and an exceptional sharp AlGaN/GaN interface (< 1ML variation).

The flatness of the interface following 2.4 μm of GaN growth indicates that it might be possible to grow substantially thicker GaN layers with Ga-face polarity which still have good 2DEG properties. Mobility might be improved with thicker GaN buffers while high

resistivity buffers for circuit applications could still be obtained. If so, MBE grown HFET structures would have significant advantages over OMVPE grown structures.

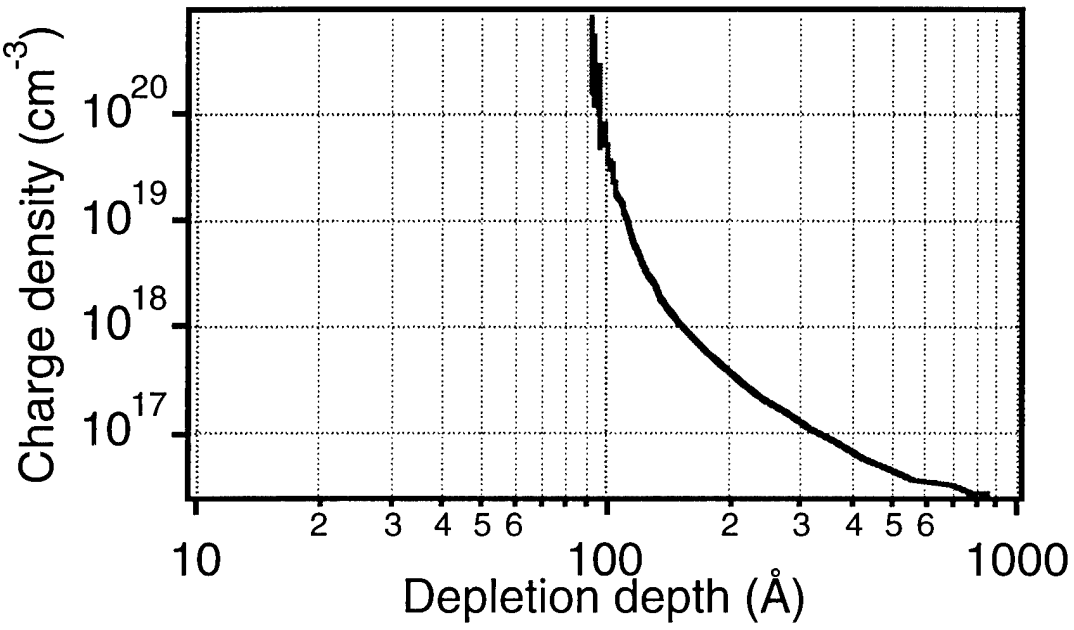


Figure 7 CV profile of HFET structure shown in Figure 6.

HFETs were made from MBE grown GaN. Structures with 0.7 μm thick buffers on AlN nucleation layers had mobility of 750 cm^2/Vsec. DC characterization of 0.75 μm gate length HFETs showed gm of 200 mS/mm which was significantly reduced by high contact resistances of 3ohm-mm. Peak Ids was 650 mA/mm at 1V V_{gs}. The gate could easily support +2V without significant conduction current. Ids was nearly 750mA/mm at 2V V_{gs}. Breakdown voltages for a 0.2μm gate length device were 43V V_{ds} and 50V V_{dg}.

Microwave measurements on the 0.2 μm gate length HFET showed 27 GHz f_t and 30 GHz f_{max}. Saturated output power was 1 W/mm. Contact resistance severely limited microwave frequency operation of these devices.

One important outcome of these devices was to observe reduced gate leakage currents, even though the AlGaN barrier was only 100 Å thick. Insertion of the 20 Å GaN layer at the surface as a piezoelectric barrier brought the gate current down approximately a factor of 5 compared to structures without it. A thicker GaN surface will be used in future device structures. In addition, thicker AlGaN supply layers will be used to reduce C_{gs} for ease in amplifier input impedance matching.

E. Flow Modulation Epitaxy of AlGaN/GaN Piezoelectric HEMT Structures J.A. Smart and J.R. Shealy

1. AlGaN/GaN buffer structures

Significant progress as been made this past year on the development and optimization of AlGaN/GaN buffer structures on both sapphire and SiC (4H and 6H) substrates. Initial investigations focused on employing the widely accepted "two-step" buffer formation techniques which involves a low temperature (500-700°C) GaN nucleation layer followed by a high temperature (1000-1100°C) GaN buffer. Although this process yielded planar growth, the surface morphology was poor with a high density of defects unsuitable for device applications. In addition, a large n-type background carrier concentration ($\approx 10^{17}$-10^{18} cm^{-3}) was measured within the GaN buffer layer forming parasitic current paths detrimental to the laterally conducting devices being developed for this program.

A new buffer formation technique was developed which uses a high temperature (above 1000°C) $Al_xGa_{1-x}N$ nucleation layer followed by a thick GaN buffer. This single temperature process allows atomically flat GaN layers with low background carrier concentrations ($<10^{13}$ cm^{-3}) to be routinely grown.

Both the composition and thickness of the $Al_xGa_{1-x}N$ nucleation layer were optimized in respect to get the highest mobility and sheet carrier density on undoped HEMT structures grown on each substrate. A minimum aluminum content in the $Al_xGa_{1-x}N$ layer is necessary to create sufficient nucleation sites on the substrates to wet the entire surface, resulting in planar growth within several hundred angstroms. Minimal compositions of 6% and 15% Al in the solid is required on SiC and sapphire, respectively, to achieve smooth layers. Thickness of the AlGaN nucleation also influences the material quality, especially on SiC were substrate surface scratches are present.

Apparently, when the AlGaN layer thickness is below 1800 Å on SiC, defects associated with the surface scratches are permitted to propagate throughout overlaying epitaxial layers, even after several microns of material is deposited. On sapphire, we were able to reduce the AlGaN thickness to 150 Å before adversely effecting the quality of the GaN overlayer. Either the absence of substrate damage (scratches) and/or the higher Al composition in the nucleation layer allows successful nucleation with thinner AlGaN layers on sapphire substrates.

2. AlGaN/GaN HEMT structures

After obtaining suitable buffer layers, growth efforts focused on producing undoped AlGaN/GaN transistors on both semi-insulating SiC and sapphire substrates. Device layers were designed to have a 250 Å $Al_xGa_{1-x}N$ barrier ($0.20<x<0.35$) deposited on a thick (>1 μm) GaN buffer layer. Structures grown on SiC exhibited room temperature mobilites as high as 1,505 /Vs with a 2DEG density of $1.3x10^{13}$ cm^{-2} and a record low channel sheet resistance of 275 Ω/sq. On sapphire, mobilities of 1,075 cm^2/Vs were measured with 2DEG sheet densities around $1.0x10^{13}$ cm^{-2} and typical channel sheet resistance's about 550 Ω/sq. RF performance was evaluated on devices fabricated with nominally .15 μm gate widths and lengths varying between 75 - 150 μm. To date, devices have yielded $f_t \approx$ 75 GHz on SiC and $f_t \approx$ 50 GHz on sapphire. Preliminary RF power testing on devices with 0.75 μm gates widths (class A operation) exhibited 2.5 watts/mm and 1.7 W/mm on SiC and sapphire, respectively.

The goal of this program is to fabricate linear amplifier circuits utilizing the field effect transistor mentioned above. This will require relatively large uniform areas of device quality GaN-based materials grown on sapphire and eventually on semi-insulating SiC. During initial transistor development (over this past year), device layers were deposited on quarter and half wafers which provided sufficient uniformity. Recently, considerable efforts have been directed on producing uniform epitaxial layers on 2" sapphire substrates. Reactor cell modifications included installation of a new susceptor capable of accommodating up to eight 2" wafers per run, and implementing an improved RF coil design giving better temperature uniformity and reproducibility.

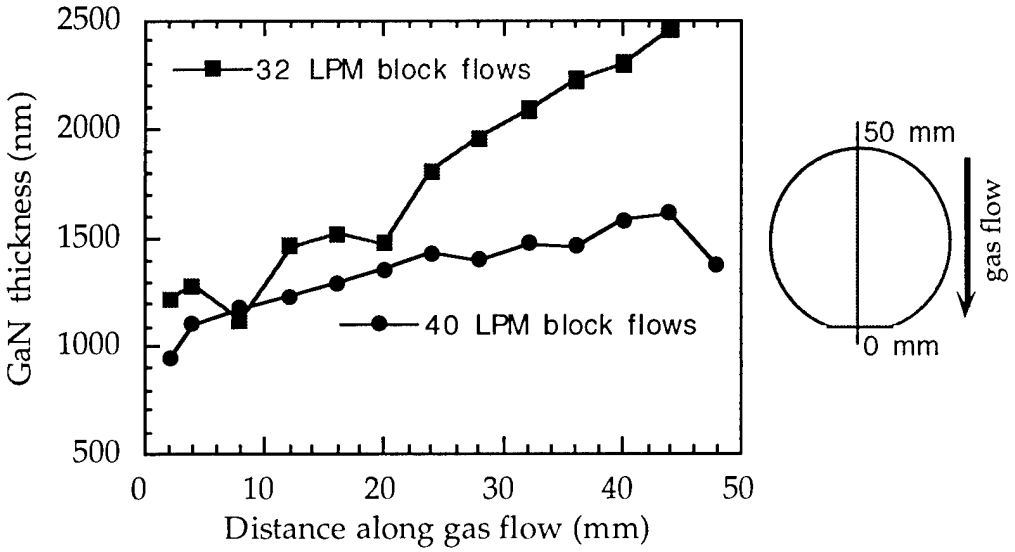
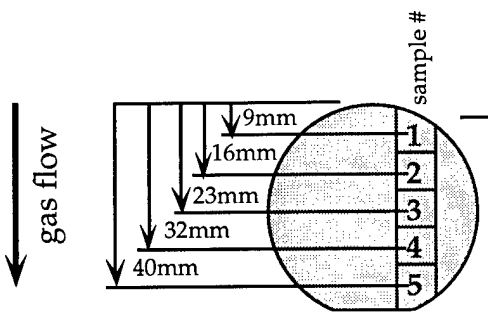


Figure 8 GaN layer thickness uniformity along the gas flow direction with different block flows. Deposited on 2" sapphire substrates.

First, variations in GaN thickness along the gas flow directions on 2" sapphire substrates was investigated. Using the previously established transport carrier flow of 32 LPM (through the block distribution system), a variation of ± 24 % was observed along the reactant flow direction. This difference in thickness is caused by gas phase depletion. By increasing the transport flow (gas velocity) to 40 LPM, we reduce this variation to about ± 12 % as shown in Figure 8. Experimentation is presently being conducted to further increase this flow to achieve uniformity less than ± 5 %. Thickness uniformity perpendicular to the gas flow is very good with variations below ± 2 %.

Transport properties of the 2DEG at the AlGaN/GaN interface were calculated from Hall measurements on the two different block flow wafers. The location of the Hall samples and a summary of the room temperature mobilities and 2DEG sheet concentrations are given in Figure 9. The higher block flows create more consistent results (± 9 % in mobility) and indicate a significant improvement in 2DEG mobilities compared to the lower flows. Mobilities values decrease by over a factor of 2 with the lower block flows (similar trends were observed on quarter and half wafers grown under comparable conditions). This decrease is caused by thickness and compositional (x_{Al}) variations across the wafer.



block flow 32LPM		block flow 40LPM	
μ	ns	μ	ns
838	0.68	875	1.15
761	0.78	985	1.04
678	0.99	950	1.03
603	1.00	995	1.02
414	0.95	1068	0.95

Figure 9 Room temperature Hall data for two different block flows on undoped HEMT structures across 2" sapphire substrates.

The aluminum uniformity of the pseudomorphic $Al_xGa_{1-x}N$ barrier layer was examined using PL on the Hall samples mentioned above. Although there was an improvement from ±1.5 % to ±0.7 % going from lower to higher flows, the variation is small and does not present a problem. Figure 10 gives the PL spectra on the five hall samples for the higher block flows. The point of interest is the increase in PL intensity as we move towards the top of the wafer. This indicates that the $Al_xGa_{1-x}N$ barrier thickness is increasing towards the top of the wafer, consistent with the results shown in Figure 8 for GaN thickness. Thicknesses derived from C-V measurements suggest that the barrier could be varying by as much as a factor of 2 from top to bottom. Since the barrier thickness is a critical design parameter, future epitaxial growth experiments to improve uniformity will be governed by this layer.

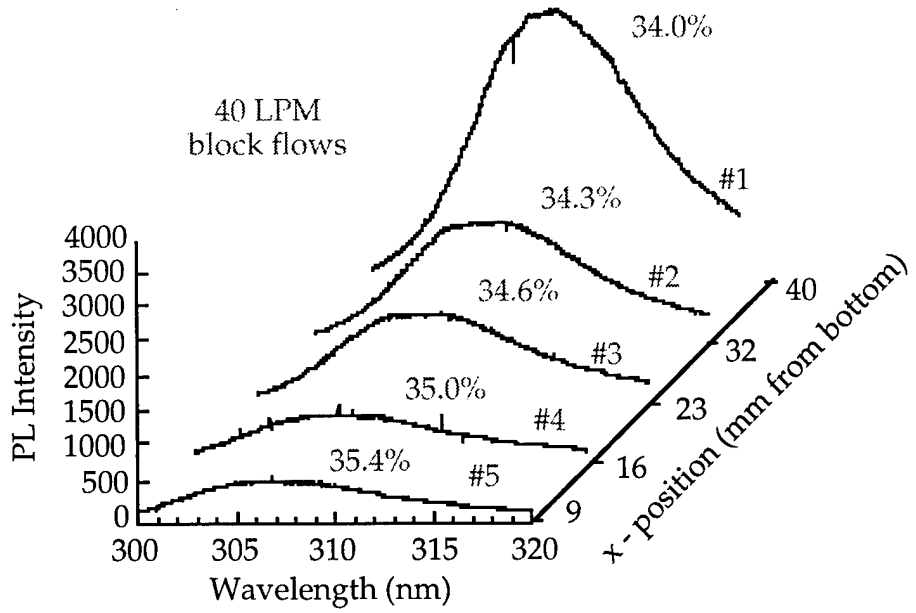


Figure 10 Room temperature PL data of AlGaN barrier layer on a HEMT structure grown on 2" sapphire with high block flows. Numbers on the right correspond to Hall samples referenced in text.

3. Future Studies

Significant advances have been made in the development of undoped AlGaN/GaN transistors deposited on a AlGaN nucleation layers by flow modulation OMVPE. To achieve the goals of this program, technology developed over the past year is being scaled up and refined to produce uniform GaN-based epitaxial layers over whole wafers (2" sapphire, and 1- 5/8" semi-insulating SiC). We will continue investigating uniformity issues, and growth optimization using our new susceptor capable of accommodating up to 8 whole wafers. With acceptable uniformity, various device structures will be investigated and provided for other program members.

F. UHV STEM Studies of Gallium Nitride Structures – Tyler Eustis and Prof. John Silcox

1. Introduction

The main focus over the last year has been the investigation into the affects of defects on the electronic structure of III-N. Calculations performed by Nils Weimann and supported by data in the literature show that the dislocation density of the film affects the bulk mobility of GaN as a function of n-type doping.[2] In addition, work performed in 1996-97, suggested a relationship between Si doping density and the intensity of the yellow luminescence. The common characteristic of saturation of a defect in the two above mentioned defects has led to the belief that dislocations are also related to yellow luminescence. For these reasons, a sample with a large yellow luminescence grown by MBE at Cornell University was selected for investigation.

In addition, samples obtained from HP containing InGaN quantum wells were used in a proof of concept experiment verifying the validity of Z-contrast imaging in Group III-Nitrides.

2. Results

A cross sectional sample was prepared by the wedge technique. The sample was then ion milled to electron transparency. Figure 11 is a bright field image of the GaN sample. A columnar structure can be seen extending along the growth direction from the bottom left to the upper right. The columns appear to be about 1000 ≈ in diameter. From what is known about nucleation of III-N, this observation is not surprising. The columns do appear to be in physical contact with each other but a boundary between the columns is plainly visible. In addition, stacking faults or twins parallel to the substrate occur at random intervals along the columns. Slight difference in orientation between grains will produce dislocation networks at the grain boundaries.

[2] Weimann, N.G., Eastman, L.F., Doppalapudi, D., Ng, H.M., Moustakas, T.D. "Scattering of electrons at threading dislocations in GaN," Journal of Applied Physics, vol.83, no.7, p. 3656-9

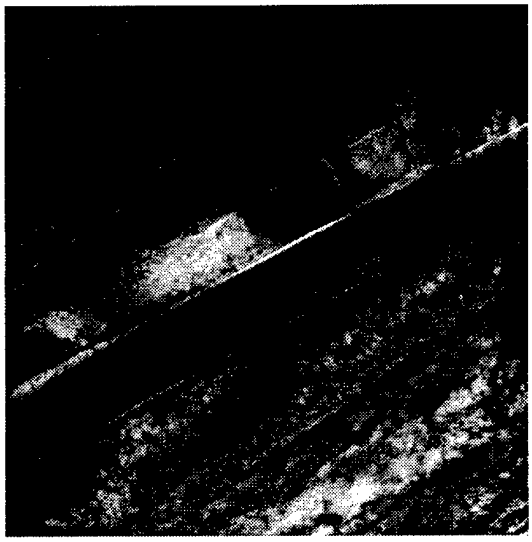


Figure 11 Cross Section bright field image of GaN sample. Full Scale is 6400nm.

Figure 12 Planview Bright Field Image of GaN Sample. Full Scale is 640nm

It is expected that these grain boundaries should be tilt boundaries creating threading edge dislocations. Initial EELS (Electron Energy Loss Spectroscopy) did not produce any signals related to defects, although probe size and signal to noise ratio could have been the problem.

A planview sample was prepared by the wedge technique. It was thought that a planview sample would improve the signal to noise ratio of signals coming from threading dislocation as the number of sites sampled by the probe would be much greater. Figure 12 is a bright field image of a grain boundary. The crosshatching through the middle of the image are threading dislocations. Initial EELS spectra suggested that these dislocation were producing electronic states within the bandgap of GaN. To investigate the possibility that the electronic states were caused by damage from the electron beam, nitrogen (N) K-edge spectra were obtain and high and low magnification.

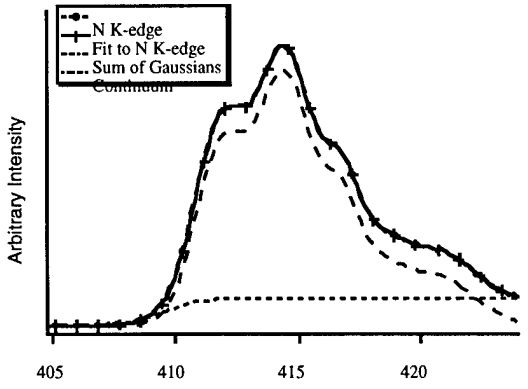


Figure 13 N K-edge of defect free GaN. Average of 15 scans.

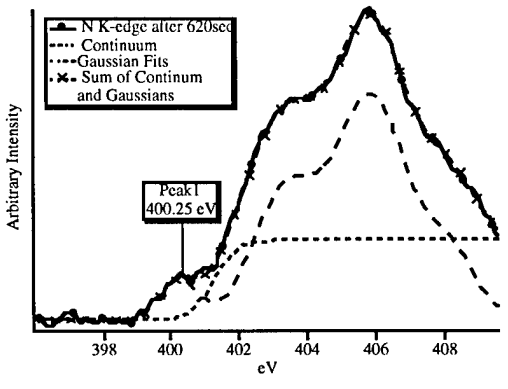


Figure 14 N K-edge of GaN after Damage.

The low magnification spectra taken over areas clear of any visible defects, provided a reference spectrum. An average of 15 N K-edge spectra obtained at a magnification of 500k is displayed in Figure 13. In addition, the fitted continuum (conduction band), the sum of five gaussians, and the fit to N K-edge (sum of the continuum and gaussians) are displayed. At a magnification of 10 million, multiple N K-edge spectra were obtained. However, the signal decreased with time indicating that damage was occurring. In addition, an additional peak appeared prior to the N K-edge. Figure 14 depicts a N K-edge from GaN after exposure to the electron beam for 620 sec. at a magnification of 10 million.

In Figure 14, the N K-edge, the fitted continuum (conduction band), gaussian fits, and the fit to the N K-edge (sum of gaussians and continuum.) In comparing Figure 13 and 14, notice the extra peak in Figure 4 labeled Peak 1. From the literature, it appears that this new peak is related to π^* state.[3,4] Notice that Peak 1 is about 2 eV from the true onset of the continuum (conduction band edge.) This all suggests that anti-bonding sites related to nitrogen are the cause of the yellow luminescence.

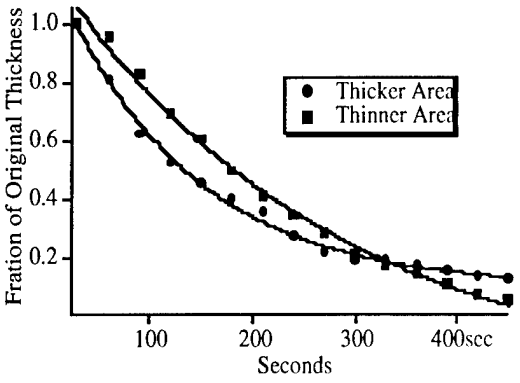


Figure 15 Fraction of thickness remaining vs. time for two different thickness.

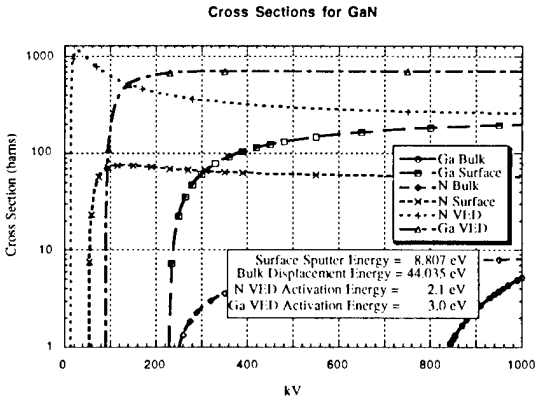


Figure 16 Cross-sections for Ga and N in GaN vs. voltage.

To more fully understand the nature of the defects causing Peak 1, and to determine which conditions cause damage and which does not, the EELS data was analyzed and compared with simulations. Figure 15 gives the fractional thickness vs. time. A model developed by Medlin et. al.[5,6] is being modified for the III-N system. As part of the simulation, election cross-sections had to be calculated using FORTRAN code developed by Bradley[7] and

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[3] π^* states are anti-bonding states. π bonds are bonds formed by the "lateral" overlap of p-orbitals. With the creation of π bonds, empty π^* (anti-bonding) states are created.

[4] Hitchcock, A.P., "Core Excitation and Ionization of Molecules," Physica Scripta Volume T, vol.T31, p. 159-70

[5] Medlin, D.L., Thomas, L.E.; Howitt, D.G. "Decomposition of Refractory Carbides in the Analytical Electron Microscope." Ultramicroscopy, vol.29, no.1-4, p. 228-32

[6] Medlin, D.L., Howitt, D.G. "The Role of Sputtering and Displacement Damage in the Electron SCRIBE Process." Philosophical Magazine Letters, vol.64, no.3, p. 133-41

[7] Bradley, C.R., "Calculations of Atomic Sputtering and Displacement Cross-sections in Solid Elements by Electrons with Energies from Threshold to 1.5MV." Argonne National Laboratory Report No. ANL-88-48

activation energies collected from the literature.[89] Figure 16 displays cross-sections vs. electron acceleration energy. Figure 17 displays the current results from simulations to-date. The simulations are still being modified to realistically model the system. While the model closely resembles the experimental data, some refinement is still required.

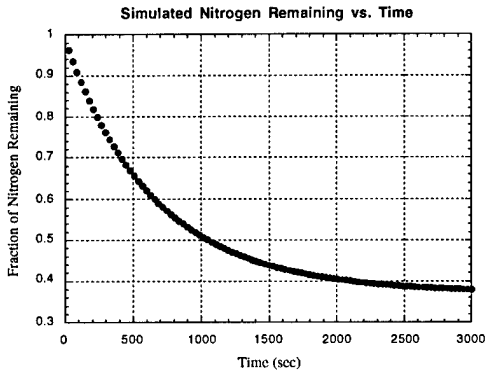

Figure 17 Simulated nitrogen remaining vs. time

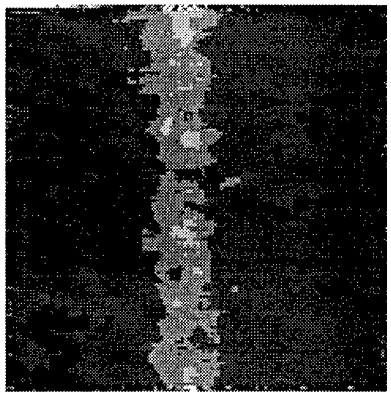

Figure 18 Z-contrast image of InGaN quantum well. Full Scale = 64nm

Samples containing InGaN quantum wells were obtained from HP. These samples were used as a proof of concept study for Z-contrast imaging in III-N. Figure 18 is an Annular Dark Field (ADF) image of one of the quantum wells after removal of thickness affects leaving only Z-contrast. Thickness affects are removed by dividing the ADF image by a thickness map obtained from the ratio of the plasmon image to the zero loss image.

3. Work in Progress

Planning of future work is evolving as new high priority problems in manufacturing of III-N FETs emerge. Current problems of low saturation velocity and poor 2DEG confinement will hopefully be solved through an investigation into the AlGaN/GaN heterojunction in the current MBE and MOCVD grown devices. With the recent dramatic improvement in the performance of MBE grown FETs, an investigation has begun to identify the cause in polarity change initiated by the buffer layer. In addition, items related to polarity will be investigated. Such items as changes in polarity within the films, and strain mapping will be addressed. Finally, LEO samples grown by MOCVD will be looked at and items related to dislocation propagation and heat transport through the silicon nitride mask will be addressed.

[8] Zapol, P.; Pandey, R., Gale, J.D., "An Interatomic potential Study of the Properties of Gallium Nitride." Journal of Physics: Condensed Matter, vol.9, no.44, p. 9517-25

[9] Willardson, R.K., Beer, A.C., "Semiconductors and Semimetals. Volume 4. Physics of III-V Compounds." Academic Press Inc., New York, New York. 1968.