MODULATION-DOPED FIELD EFFECT TRANSISTORS FOR HIGH-POWER MICROWAVE APPLICATIONS

BY

RONALD WALDO GRUNDBACHER

B.S., University of Illinois at Urbana-Champaign, 1991
M.S., University of Illinois at Urbana-Champaign, 1993

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Ronald Grundbacher

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1406 W. Green St.
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FOR HIGH-POWER MICROWAVE APPLICATIONS

Ronald Waldo Grundbacher, Ph.D.
Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign, 1997
I. Adesida, Advisor

The need for high-power, low-noise transistors operating at frequencies of 1 GHz and above has accelerated over the past several years, because applications in consumer markets, including telecommunications products, have increased dramatically. Transitors in the silicon system are having difficulty providing the high-power, low-noise characteristics at operation above 1 GHz. Transistors based on InP and GaAs, which include HBTs, MESFETs, and HEMTs, have proven to be excellent devices and can provide high-power, low-noise capabilities at frequencies of 100 GHz and beyond. Issues of importance for high-power microwave transistors include breakdown mechanisms , linearity, and material selection.

The effect of drain-side cap recess distance on InGaAs/GaAs PHEMT device performance at both dc and rf frequencies is investigated. This investigation is achieved though the development of a four-layer electron beam resist technique and sequential wet and dry selective etching. A high linearity of device characteristics is important to minimize intermodulation of high frequency signals under high-power operation. The linearity of device performance is investigated through the comparison of InGaAs/GaAs PHEMTs and doped channel FETs at dc and rf operation. InP is investigated as a channel material for use in high-power FETs due to the intrinsic properties including high breakdown voltage, high electron saturation velocity, high electron velocity at high electric field, and high thermal conductivity. Forming low-resistance ohmic contacts to modulation-doped InP channel heterostructures is a challenging issue and is investigated through the study of ion-implanted alloyed contacts and through cap layer design for nonalloyed contacts.

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CHAPTER 1
INTRODUCTION

1.1 Transistors for Telecommunications

The development of compound semiconductor transistors for use at microwave and mm-wave frequencies has accelerated over the past several years in expectation of new consumer markets. Previously, devices were developed for important yet limited areas, such as military and space applications. Military applications included missile and guided weapons applications at 18 GHz, jammers and decoys at 24 GHz, phased-array radar up to 40 GHz, and antitank weapons at 94 GHz. The devices are seeing continued use in their traditional military and space applications, but are also entering the growing consumer market. Consumer applications include direct broadcast satellites at 12 GHz, marine radar at 3 to 10 GHz, intruder alarms at 10 GHz, and instrumentation from 3 to 50 GHz. Presently, the largest consumer market may be in handheld telecommunications, such as cellular phones. Cellular phones have been operating at 900 MHz, but are now moving to 1.9 GHz and potentially higher frequency bands. Silicon devices are struggling to provide the high-power, low-noise characteristics at operation above the 900 MHz band. GaAs- and InP-based transistors, however, are quite capable of providing extremely low noise and high power at frequencies of 100 GHz and beyond. Several other consumer markets, including automotive radar and local area networks (LAN), are under study and may soon require devices that operate in the microwave and mm-wave range. Devices have also been utilized in fiber-optic communications systems. In these systems, the transistors are integrated with lasers and photodetectors to provide transmitters and receivers for optical links. Operation above 10 GHz provides a large bandwidth and allows for extremely rapid data transfer through the fiber-optic systems.

The GaAs- and InP-based devices that are capable of microwave and mm-wave frequency operation include metal-semiconductor field-effect transistors (MESFETs), heterojunction bipolar field-effect transistors (HBTs), and high electron mobility transistors (HEMTs). Recent literature [1.1] compares the three above mentioned devices on several merit parameters including power density, gain-bandwidth product, speed, and noise. HEMTs and HBTs are comparable in power density capabilities. HEMTs exhibit the highest gain-bandwidth product and appear to be the best devices for wideband applications at high frequencies. HEMTs have achieved the highest f_{max} (maximum frequency of oscillation), highest f_T (unity current gain frequency), and lowest noise figures. Because of the very low noise figures and high efficiencies, HEMTs are currently the main type of transistor being used in the microwave and mm-wave systems. In particular, GaAs-based pseudomorphic HEMTs (PHEMTs) have emerged as the device most used for power applications at the microwave and mm-wave frequencies [1.2]. In the discussion that follows, emphasis will be placed on examining critical features of HEMT technology.

1.2 Material Systems for HEMTs

The basic material structure and energy band diagram of a pulse-doped HEMT is shown in Figure 1.1. The layers include a highly doped narrow bandgap cap, a high bandgap Schottky layer, a doping plane, a high bandgap spacer layer, a narrow bandgap channel, a high bandgap barrier (buffer) layer, and the substrate. Each of the layers in Figure 1.1 is on the order of 100 to 500 Å, and requires very sophisticated growth methods. Progress in molecular beam epitaxy (MBE) and metallo-organic chemical vapor deposition (MOCVD) growth techniques has made it possible to obtain high-quality epitaxial layers with well-controlled thickness, composition, and uniformity.

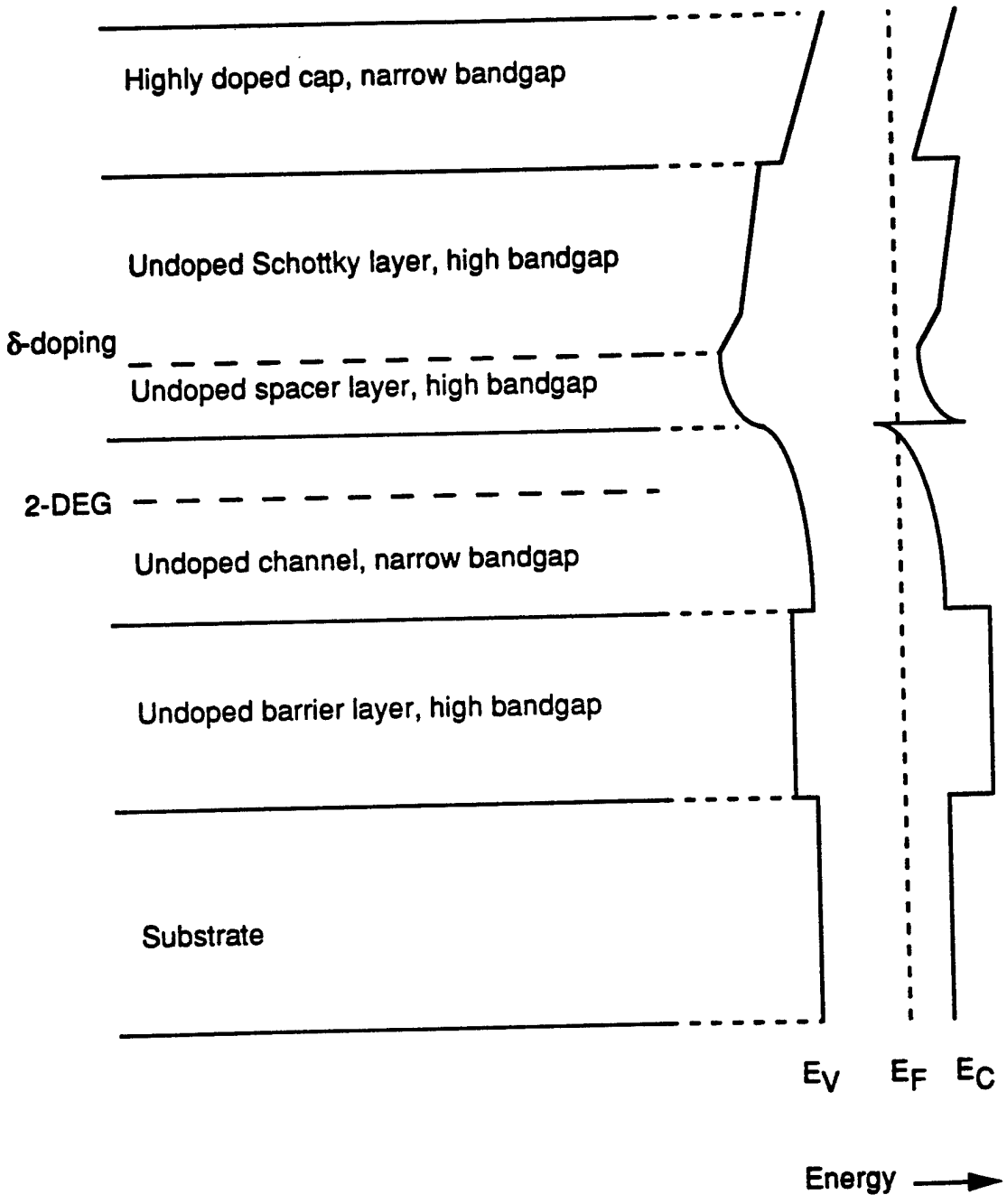

Figure 1.1. Schematic of a general layer structure for a pulse-doped (δ-doped) HEMT. A schematic of the energy band diagram with valence band (E_v), Fermi level (E_F), and conduction band (E_c), is shown to the right of the layer structure.

The HEMT is designed such that electrons, which are supplied by the donor atoms in the doping plane, reside in the channel and form a thin layer called a two-dimensional electron gas (2-DEG) near the spacer layer heterojunction. The 2-DEG of the HEMT improves electron transport characteristics and shows better noise characteristics than the MESFET, in which the donor ions occupy the same region as the free electrons. The improved electron transport in HEMTs is a direct result of the enhanced mobility of the electrons that are separated from the donor ions.

The first generation of HEMT employed a gallium arsenide (GaAs) channel and aluminum gallium arsenide ($Al_xGa_{1-x}As$) Schottky, donor, spacer, and barrier layers. The $Al_{0.3}Ga_{0.7}As$/GaAs heterojunction, with a conduction band offset of 0.22 eV, limits the sheet concentration of electrons in the channel (n_s) to ~$1x10^{12}$ cm^{-2}. High mobility and high n_s are desirable because as they are increased, lower source resistance and higher current density are obtainable. Introducing indium (In) into GaAs, forming $In_xGa_{1-x}As$ ($0<x<1$), increases the mobility of the electrons. An $In_xGa_{1-x}As$ channel has been used in AlGaAs/GaAs-based pseudomorphic HEMTs (PHEMTs). There is a lattice mismatch between the $In_xGa_{1-x}As$ and GaAs which increases with In content. The mismatch introduces strain in the crystal, and this strain may spoil the epitaxial layer if the In content is too high or the channel layer is too thick. The In content is limited to approximately 20% and the thickness is limited to approximately 150 Å, as determined by the critical thickness [1.3]. The n_s is increased to ~$2x10^{12}$ cm^{-2}, because the conduction band offset (0.42 eV) is greater than in the GaAs/AlGaAs system. The mobility of the electrons is also enhanced.

In an effort to exploit the enhanced mobility of higher In-containing compounds, the InP/$In_xGa_{1-x}As$/$InAl_{1-x}As$ system has also been investigated. This system has a conduction band offset of 0.51 eV and allows for an n_s of ~$3x10^{12}$ cm^{-2}. The highest speed and lowest noise HEMTs have been developed in this material system. The InP/$In_xGa_{1-x}As$/$InAl_{1-x}As$ system is also attractive from a material standpoint because

of the high thermal conductivity of InP. The high thermal conductivity aids in efficient heat dissipation from the transistors, which reduces thermal degradation and improves reliability and lifetimes. With the increasing In content of $In_xGa_{1-x}As$, the bandgap becomes smaller. The small bandgap of $In_{0.53}Ga_{0.47}As$ leads to lower breakdown voltage and higher output conductance when compared to PHEMTs with $In_xGa_{1-x}As$ (x=0.15-0.2) channels.

Another important material system issue is the stability of the aluminum-containing compounds. This is important in determining the lifetimes and reliabilities of FETs. The oxidation of Al at the surface can lead to the formation of surface states that degrade device performance and reliability [1.4]. Materials that do not contain Al have been investigated for use as the Schottky barrier layer. InGaP and InP have been used as the Schottky barrier layer for GaAs- and InP-based FETs [1.5], [1.6]. A passivation layer such as silicon nitride has also been used extensively to isolate the Al-containing compounds from oxygen at the surface.

1.3 Fabrication Issues

Device characteristics are greatly influenced by the processing used in their fabrication. Photolithography and electron beam lithography are used to pattern device dimensions including isolation regions, ohmic contacts, gates, passivation regions, and interconnect metal. Device isolation is necessary to avoid crosstalk and backgating effects between adjacent devices. Isolation is typically achieved through mesa etching or ion implantation. Low source and drain resistances, which are necessary for high-frequency, low-noise operation, require both small contact resistance and low sheet resistance. Ohmic contact formation at the source and drain contacts is typically performed by alloying a stack of evaporated metals consisting of Au, Ge, and Ni. Careful calibration of a rapid thermal annealing system or alloy furnace is necessary for reproducible low-resistance contacts. Degradation of ohmic

contacts has been noted as a primary cause of device failure in InP/InGaAs/InAlAs HEMTs [1.7].

Perhaps the most critical fabrication issue, is the process of gate formation. Because the speed improves as gate length is reduced, gate lengths of 0.25 μm and below are typical for state-of-the-art devices. Much effort has been expended in the area of gate lithography and gate recess etching. Optical lithography may be used for gates whose length is 0.5 μm and longer. Electron beam lithography is typically used for the definition of submicron gates. Electron beam lithography in multilayer (2,3, or 4) resists allows for the formation of a T-gate which has a short gate length (small footprint) and a large top. The small footprint allows for high frequency operation, and the large top reduces gate resistance, which is important for attaining high maximum frequency of oscillation by reducing the R-C time constant of the gate. As opposed to optical lithography, which is performed using parallel exposure, electron beam lithography must be sequentially performed. This limitation in throughput has restricted the large-scale use of electron beam lithography in production environments, but it is a valuable tool in fabricating limited numbers of high-performance devices.

Recessing of the cap layer before evaporation of the gate metal is the second crucial step in fabricating the gate. The threshold voltage, the gate voltage at which the device begins conducting current from the drain to source, is largely determined by the gate to channel distance [1.8]. Nonselective etches have been used for gate recess etching, but require extremely well-calibrated, reproducible, and carefully timed etches. For circuit applications, uniformity of device characteristics is extremely important, and thus, monolayer (5 Å) uniformity in gate recess is necessary. Both wet chemical and dry (plasma) selective etchants are used to obtain uniform etch depth across the wafer. These etchants etch one material (such as GaAs), but not another material (such as $Al_xGa_{1-x}As$). If the selectivity of the etchant is high enough, etch

depth uniformity approaches the growth-determined uniformity across the wafer. Gate recess techniques have been extended to include a two-step recess, which has been used to increase the breakdown voltages of PHEMTs [1.9].

1.4 Organization

Because of the current need for high-speed, high-power transistors for both military and commercial applications, the design of GaAs- and InP-based HFETs was investigated. The research focus is on the critical issues involved when designing the devices for high-power operation.

The basic theory of transistor operation is discussed in Chapter 2, along with a discussion of device figures of merit, which are important for high-power transistor operation. Chapter 3 presents a new four-layer resist technique used in the fabrication of double recessed gate PHEMTs. The four-layer resist technique allows for the study of dc and rf characteristics of devices with varying drain-side recess widths. Linearity of two-ports is important for high power applications, and Chapter 4 discusses the linearity of doped-channel FETs (DCFETs) and PHEMTs. The use of InP as the channel material of high-power HEMTs is investigated in Chapter 5. The main conclusions from the experimental results are reviewed in Chapter 6, and suggestions for future research directions are also offered in this final chapter.

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CHAPTER 2

GENERAL HEMT THEORY AND DESIGN

An HEMT consists of a modulation-doped heterostructure, as well as ohmic and Schottky metal contacts. A basic HEMT device is shown schematically in Figure 2.1. The heterostructure consists of several abrupt junctions between semiconductors having different energy gaps. The Schottky layer, which has the larger bandgap, contains an n-type doping plane. The channel layer, having the smaller bandgap, is undoped. The difference in the bandgaps between the semiconductors results in a discontinuity in the conduction and valence bands at the interface (see Figure 1.1, page 3). Electrons from the donor atoms diffuse into the channel and reside in the potential well at the interface, forming a two-dimensional electron gas (2-DEG). The separation of the electrons from the donor atoms reduces the ionized impurity scattering and enhances the mobility of the electrons, and confinement of the electrons in the potential well leads to the quantization of the energies in the direction perpendicular to the interface, leading to additional improvement in transport properties [2.1].

The ohmic and Schottky metals provide the means to control the movement of electrons in the device. The source and drain are typically low resistance ohmic contacts. With the source at ground potential (0 V) and the drain at a positive bias, electrons in the channel flow from source to drain. The gate contact is a Schottky barrier through which very little current flows (ideally, no current). The application of a voltage bias on the gate contact changes the potential distribution of the heterostructure below. As the gate potential is changed, the concentration of electrons in the channel is changed. As the number of electrons in the channel changes, so does the current that flows from the drain to source at a given drain bias.

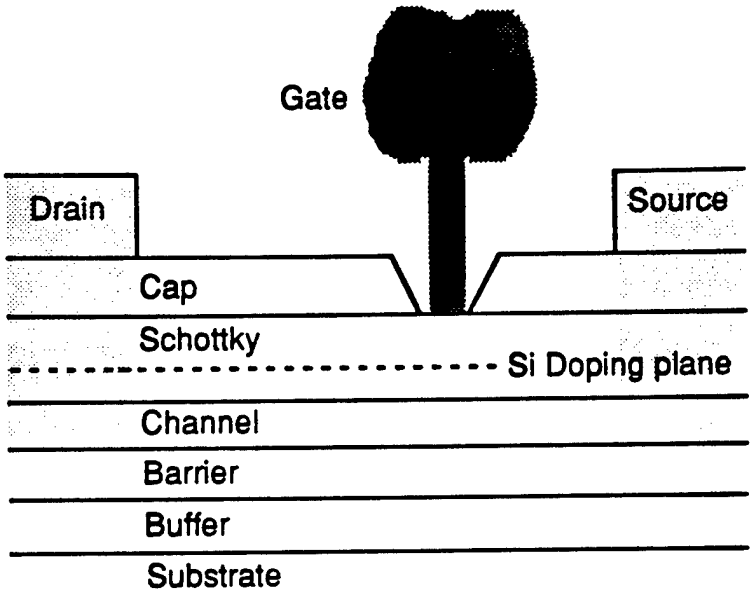

Figure 2.1. Schematic of a PHEMT device showing the heterostructure and metal contacts including the gate, drain, and source.

The basic operation of the transistor, including current flow, transconductance, and high-speed modulation, is described in this chapter. The governing equations of the transistor will be discussed. After the basic transistor operation has been presented, considerations for high-power transistor operation will be discussed. The criteria and trade-offs involved for both high-power and high-frequency operation will be presented.

2.1 Transistor Operation

The amplification and switching capabilities of the transistor depend on the effective modulation of the channel charge by the gate. The 2-DEG density can be varied between a maximum value of n_{so} to a minimum value of zero. If it is assumed

that the Schottky layer is completely depleted, then the 2-DEG concentration, n_s, as a function of gate bias, V_G, is given by the charge control model [2.2]

$$n_s = \frac{\varepsilon_o \varepsilon_s (V_G - V_T)}{q(d_d + d_i + \Delta d)} \tag{2.1}$$

where ε_o is the permittivity of free space, ε_s is the relative dielectric constant of the Schottky barrier material, d_d is the distance from the gate to the doping plane, d_i is the distance from the doping plane to the channel, and Δd is the average distance of the electron gas from the heterointerface (~8 nm). The threshold voltage V_T is the gate bias at which the channel starts to form and can be either positive or negative. If the required gate bias is positive, then the device is called an enhancement device. If the required gate bias is negative, then the device is called a depletion device. For PHEMTs, V_T is generally slightly negative. The threshold voltage for a PHEMT with planar doping is given by [2.3]

$$V_T = \phi_B - \Delta E_C - \frac{q n_d d_d}{\varepsilon_o \varepsilon_s} \tag{2.2}$$

where n_d is the δ-doping density in cm^{-2}. The Schottky barrier potential ϕ_B is on the order of 0.8 V for a Ti/Au gate on AlGaAs, and the conduction band discontinuity ΔE_C between AlGaAs and $In_{0.18}Ga_{0.82}As$ is 0.42 eV. The threshold voltage dependence is linear with respect to gate-to-doping plane distance for the case of the planar-doped HEMT. This is in contrast to the squared dependence of V_T on distance for the HEMT that has doping distributed through the Schottky layer [2.4]. The linear dependence of V_T on gate-to-channel distance (determined from gate recessing) is preferred, because uniformity in V_T is critical, especially for integrated circuit applications.

When a transistor is biased at low drain voltage (V_D), it is said to operate in the linear region. In the linear region ($V_D < (V_G - V_T)$), the drain current $I_{D,lin}$ is given by [2.5]

$$I_{D,lin} = \frac{\mu_n \varepsilon_0 \varepsilon_s w (V_G - V_T) V_D}{dL} \tag{2.3}$$

where μ_n is the mobility of the electrons in the channel, d is the gate-to-channel distance, L is the gate length, and w is the device width. The transconductance g_m is a measure of the effectiveness of V_G to modulate I_D and is defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{2.4}$$

The transconductance for low V_D is obtained from (2.3) and (2.4) and is given by

$$g_{m,lin} = \frac{\mu_n \varepsilon_0 \varepsilon_s w V_D}{dL} \tag{2.5}$$

For short gate length transistors operating at high drain bias, the carriers in the channel are traveling at the saturation velocity, and the current saturates with drain bias, V_D. The transistor is said to be operating in the saturation region. In this saturated state, the drain current $I_{D,sat}$ may be expressed as [2.6]

$$I_{D,sat} = \frac{\varepsilon_0 \varepsilon_s v_{sat} w (V_G - V_T)}{d} \tag{2.6}$$

where v_{sat} is the saturation velocity of the electrons. Note that the current is independent of the gate length, L. The relationship between I_D and V_D for various V_G is shown in Figure 2.2. The linear region (small V_D) and saturated region (large V_D) are labeled, and the independence of I_D ,with respect to V_D, is seen at large V_D. For the saturated condition, $g_{m,sat}$ is determined from (2.4) and (2.6) and is found to be

$$g_{m,sat} = \frac{\varepsilon_0 \varepsilon_s v_{sat} w}{d} \tag{2.7}$$

It is interesting to note that $g_{m,sat}$ is independent of L and V_G. However, the reduction in gate length is desirable because at shorter gate lengths, velocity overshoot and ballistic effects increase v_{sat}, and, therefore, a higher $I_{D,sat}$ and $g_{m,sat}$ are obtained. At large V_G, $g_{m,sat}$ begins to decrease, because n_s saturates in the channel. The additional charge induced with higher V_G resides in the Schottky layer instead of the

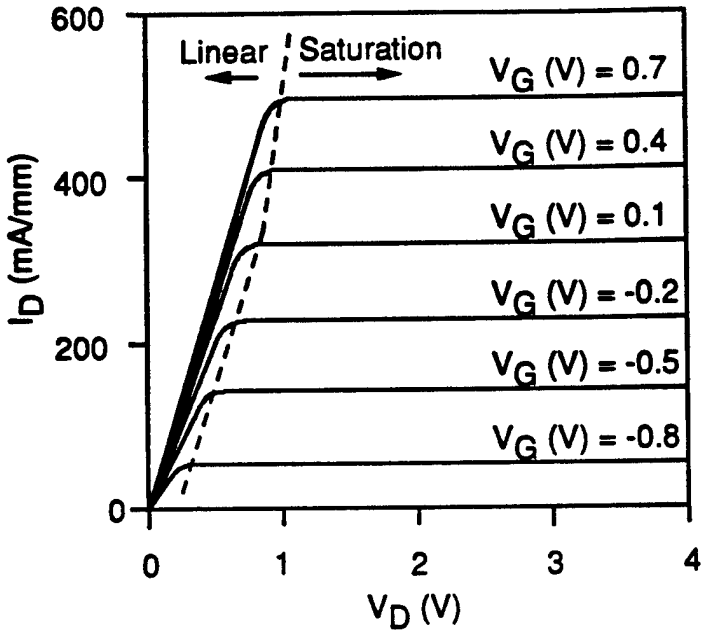

Figure 2.2. Schematic showing the ideal relationship between drain current (I_D) and drain voltage (V_D) at various gate biases (V_G).

channel. The mobility of the electrons in the Schottky layer is much lower than in the channel layer, and the velocity of the charge as a whole is reduced. The reduction in velocity leads to the reduction in g_m at high V_G. The g_m as a function of V_G is shown in Figure 2.3 for the ideal case, where carriers remain in the channel at high V_G, and the observed case, where electrons transfer into the Schottky layer at high V_G.

The importance of a small and well-controlled distance between the gate and channel can be further illustrated by examining the transistor unity current gain cutoff frequency, f_T, which is a figure of merit characterizing device speed and is approximately given by [2.7]

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_L)} \tag{2.8}$$

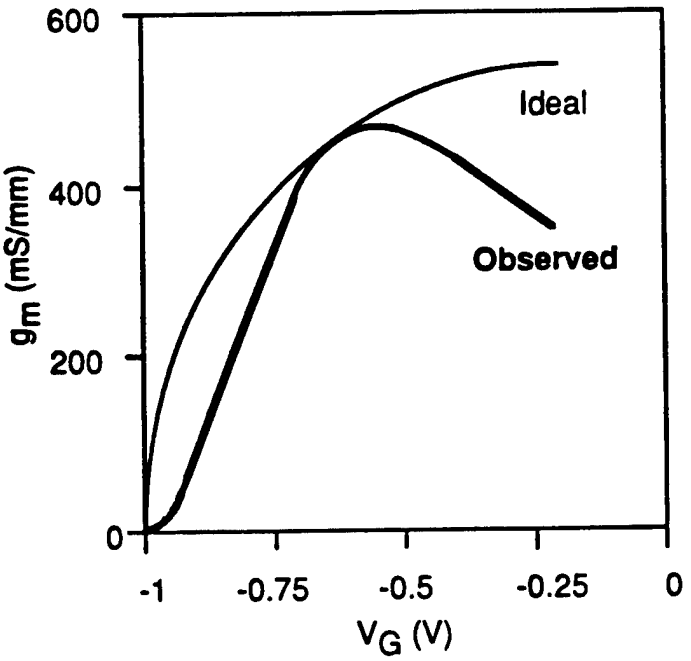

Figure 2.3. Schematic showing the ideal and observed relationship between transconductance (g_m) and gate bias (V_G).

where C_{GS} is the gate capacitance and C_L is the effective loading capacitance including fringing and parasitic capacitances. Equation (2.8) can be rewritten as

$$f_T = \frac{g_m}{2\pi\tau_t\left(1+\frac{C_L}{C_{GS}}\right)} \tag{2.9}$$

where τ_t is the intrinsic transit time of electrons in the channel under the gate and has been approximated by

$$\tau_t = \frac{L}{v} \tag{2.10}$$

Equations (2.8), (2.9), and (2.10) reflect the fact that the device transconductance is proportional to the electron velocity and the gate capacitance. Therefore, higher gate

capacitance and g_m lead to a higher device speed. In a typical integrated circuit with short gate length transistors, the dominant factor limiting speed is not the transit time of the electrons under the gate, but the C_L [2.8].

It has been argued that f_{max} (frequency of unity power gain) characterizes millimeter wave performance better than f_T [2.9], because f_{max} takes into account several additional important factors. The approximate equation for f_{max} is given by [2.10]

$$f_{max} = f_T \left(\sqrt{\frac{4g_o}{g_m}\left(g_m R_i + \frac{R_s + R_G}{\frac{1}{g_m} + R_s} \right) + \frac{4C_{GD}}{5C_{GS}}\left(1 + \frac{5C_{GD}}{2C_{GS}}\right)(1 + g_m R_s)^2} \right)^{-1} \qquad (2.11)$$

From the above equation for f_{max}, we see that losses associated with gate resistance R_g, source resistance R_s, and output conductance g_o, are taken into account. The contribution of gate-drain capacitance C_{GD} is also noted. The importance of f_{max} will be further discussed in Chapter 4.

2.2 Biasing of Power Devices

A simplified biasing scheme for Class A operation is shown in Figure 2.4. The resistor R_d connected to the drain is assumed to be an optimum resistance such that the maximum output power is extracted from the device when the dc source V_{dc} is used at the positive voltage rail. The load-line diagram for this biasing scheme is shown in Figure 2.5. The maximum output signal of the device swings from a fully-off condition with the drain-to-source voltage (V_D) equal to the drain-to-source breakdown voltage BV_{DS} and drain current (I_D) equal to $I_{pinchoff}$, to a fully-on position at V_D equal to V_{knee} and I_D equal to I_{max}. This output signal swing corresponds to an input voltage swing at the gate of $V_G = V_{pinchoff}$ to $V_G = V_{gsmax}$, which is about equal to the Schottky barrier height of the material under the gate. If V_G is driven more positive

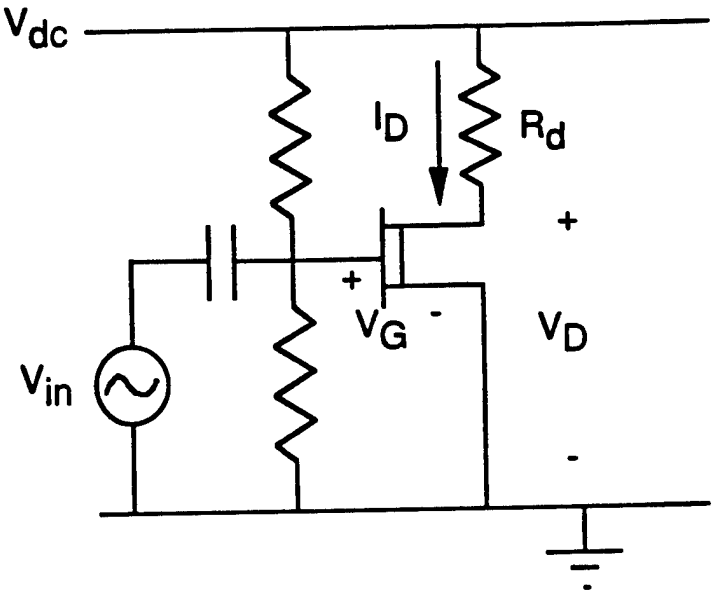

Figure 2.4. Biasing schematic for an HFET in the Class A mode of operation.

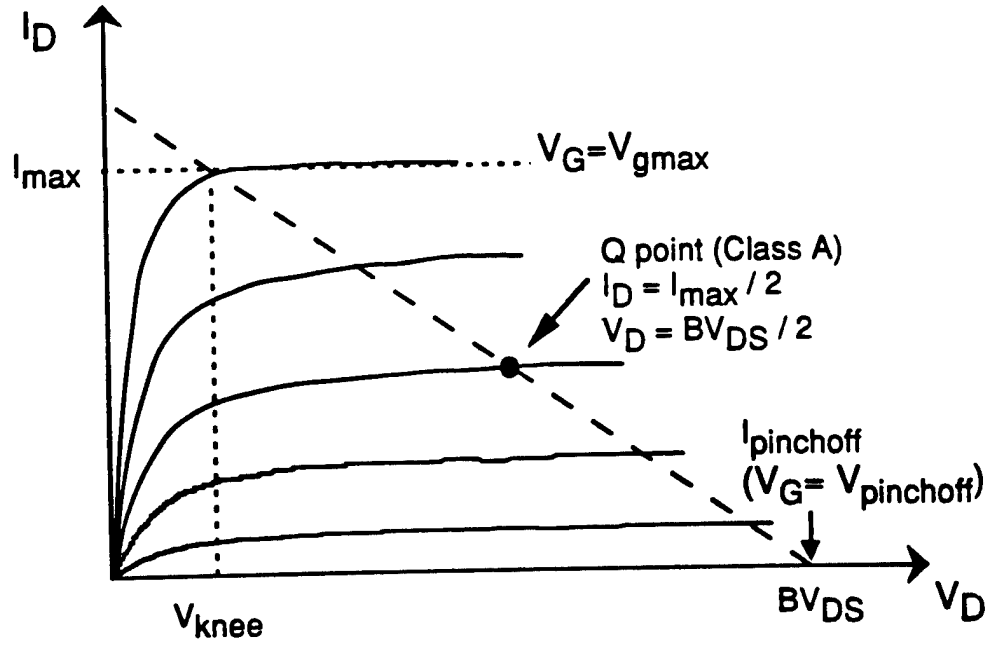

Figure 2.5. Load-line diagram for an HFET operating in the Class A mode.

than V_{gsmax}, excessive forward gate current will result and V_D will fall out of the linear amplification regime. If V_G is lower than $V_{pinchoff}$, the device enters the Class AB operation mode. If V_D is driven more positive than BV_{DS}, the device may undergo catastrophic breakdown due to the significant reverse gate current that results.

The quiescent dc bias point (Q point) is the median point between $I_{pinchoff}$ and I_{max} and the median point between BV_{DS} and V_{knee} as shown in Figure 2.5. Hence, the peak amplitude of the microwave current is $0.5(I_{max}-I_{pinchoff})$ and the microwave voltage is $0.5(BV_{DS}-V_{knee})$. Assuming the input signal is sinusoidal and the amplification is linear, the output signal is sinusoidal. Figure 2.6 shows the sinusoidal input and output signals. Because the signals are sinusoidal, an additional factor of 0.5 must be included to compute the time average power. Because the voltage and current waveforms at the output are 180° out of phase (Figure 2.6), the reactive power is zero, and the transistor is supplying the microwave power. The maximum microwave output power of the HFET in Class A operation is given by

$$P_{o\max} = \frac{1}{8}(I_{\max} - I_{pinchoff})(BV_{DS} - V_{knee}) \tag{2.12}$$

Maximum output power is an important quantity, but it does not provide information about the gain of the device. One could achieve high output power by simply making an HFET wider, therefore increasing I_{max}, or by combining the outputs of many low-power devices. The quantity termed power added efficiency (PAE) is a more significant measure of the device performance and is given by

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.13}$$

where P_{out} is the output microwave power, P_{in} is the input microwave power, and P_{dc} is the dc input power. PAE can be written in terms of the available microwave gain (G_a) of the device

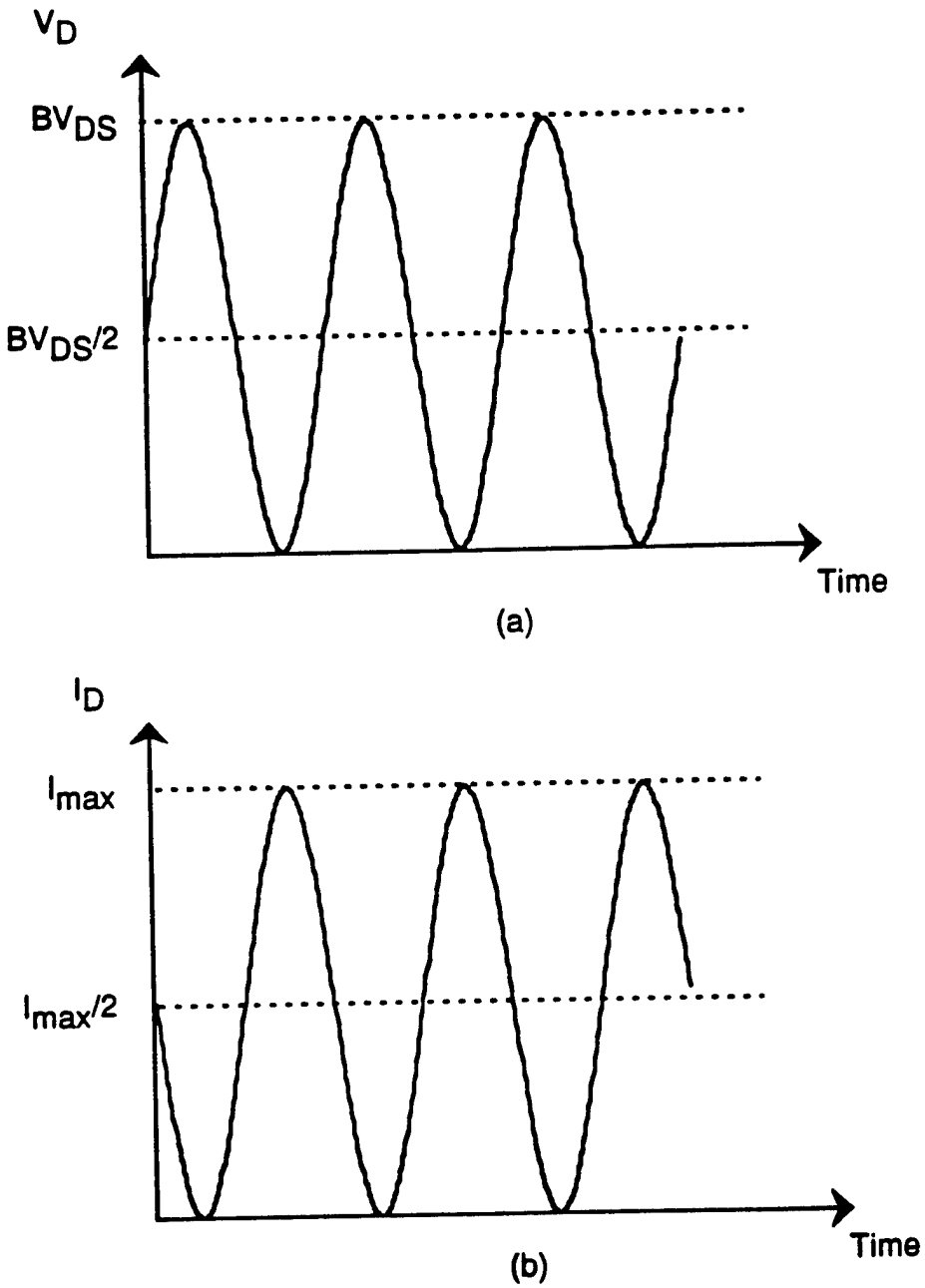

Figure 2.6. (a) Output voltage (V_D) and (b) output current (I_D) waveforms of an optimally biased HFET in the Class A mode of operation.

$$PAE = \frac{P_{out}}{P_{dc}}\left(1-\frac{1}{G_a}\right) \tag{2.14}$$

and in terms of drain efficiency (DE) by

$$PAE = DE\left(1-\frac{1}{G_a}\right) \tag{2.15}$$

where DE is defined as

$$DE = \frac{P_{out}}{P_{dc}} \tag{2.16}$$

When the gain of the device is very high, the maximum PAE is achieved and approaches DE given by (2.16).

If the ideal case of $V_{knee} = I_{pinchoff} = 0$ is considered, the dc input power of Class A is given by

$$P_{dc} = \frac{1}{4} BV_{DS} I_{max} \tag{2.17}$$

The maximum obtainable PAE for Class A operation can be found by using (2.12), (2.16), and (2.17) and is given by

$$PAE_{max\,A} = DE_{max\,A} = \frac{P_{o\,max\,A}}{P_{dc}} = \frac{1}{2} \tag{2.18}$$

where $V_{knee} = I_{pinchoff} = 0$ has been used. The maximum PAE for Class A operation is seen to be 50%. For operation in Class B, the PAE approaches $\pi/4$ [2.11].

2.3 Design Goals for Microwave High-Power HFETs

From the above discussion of the biasing of power devices, a list of desirable features for microwave high-power HFETs can be made. The voltage swing, current swing, and gain must be considered.

The voltage swing of the transistor should be maximized, which means that the knee voltage should be as small as possible, and the breakdown voltage should be as

large as possible. The knee voltage is made small by having a low contact resistance and a low sheet resistance. Low contact resistance is achieved by having a highly doped cap that facilitates the formation of ohmic contacts. Low sheet resistance is achieved by having a highly doped cap and a substantial charge (n_s) in the channel. Several factors help to increase the breakdown voltage. The larger the distance between the gate and channel, and between the gate and cap on the drain side, the higher the breakdown voltage [2.12]. As the distance is increased, the electric field between the gate and channel is lowered, and the breakdown occurs at a higher voltage. The larger distance also impedes undesired tunneling of carriers between the gate and channel, and between the gate and cap. Reducing the doping of the cap can also increase the breakdown voltage, but will also increase the source and drain resistances leading to reduced transconductance. Breakdown voltage may also be increased by reducing the thickness of the channel. As the channel thickness is reduced to ~10 nm, the effective bandgap increases as a result of energy quantization in the channel. The reduction in channel thickness, however, will lead to reduced transconductance and I_D as a result of reduced n_s and mobility [2.12]. The issue of increasing the breakdown voltage is discussed and investigated experimentally in Chapter 3.

The current swing of the transistor should be as large as possible. This requires a large full-channel drain current and a small drain current at pinchoff. A large full-channel drain current requires low source, drain, and contact resistances along with high n_s. A high Schottky barrier gate is also required so that the device can be modulated to a fully on state without excessive forward gate current. The high Schottky barrier at the gate is also beneficial in minimizing the drain current at pinchoff. Drain current in the off-state is also reduced by increasing the gate length, because subthreshold current is reduced and short channel effects become insignificant.

The last quantity of interest is the gain of the transistor, which should be maximized especially at high frequencies. A high gain is achieved by having a high transconductance. The transconductance is maximized by having a small gate-to-channel distance, short gate length, high n_s, and low parasitic resistances (source, drain, and contact). A low output conductance is also important for achieving high gain, because gain is the ratio of transconductance-to-output conductance. The output conductance is reduced by lowering the electric field in the channel. Increasing the gate length can also reduce the output conductance by reducing short channel effects. The relationship between gain and the linearity of device characteristics is discussed in Chapter 4.

Clearly, trade-offs are involved when designing high-power microwave transistors. Cap doping, channel charge, gate length, gate-to-channel distance, and channel thickness must be optimized to achieve the desired device performance.

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CHAPTER 3

INDIUM GALLIUM ARSENIDE / GALLIUM ARSENIDE PHEMTS

3.1 Introduction

As mentioned previously, GaAs pseudomorphic HEMTs (PHEMTs) are currently the dominant type of low-noise, high-power transistor in microwave and mm-wave systems and have shown the highest gain and power-added efficiencies for frequencies over 10 GHz [3.1]. A factor that had limited the use of PHEMTs to low-noise devices, operating under low current and voltage conditions, was the low gate-drain and source-drain breakdown voltages. Efforts to increase the breakdown voltages have been successful and have catapulted the PHEMT into the position of prominence for microwave and mm-wave power applications [3.2].

The use of an undoped cap has been suggested to alleviate the breakdown voltage limitation of PHEMTs [3.3]; however, this can increase both the source and drain parasitic resistances, leading to degraded microwave performance. A common technique used to improve the breakdown voltage, while maintaining low source resistance, is to use a doped cap and offset the gate towards the source side of a wide recess trench [3.4] and [3.5]. The wide drain-side recess leads to higher breakdown voltage by spreading out the space charge on the drain side of the gate, thereby reducing the electric field. A wide recess on the source side is not desirable, because this causes an increase in source resistance which degrades the transconductance. By combining a wide drain-side recess with a narrow recess, as shown in Figure 3.1, the advantages of a wide recess can be realized, while simultaneously preserving high modulation efficiency and reducing surface effects [3.6]. This process has traditionally required two lithography steps, one to define the large area where the doped cap is to be removed, and the other to define the much narrower region for gate recess and metallization. For this reason, the procedure has often been referred to as

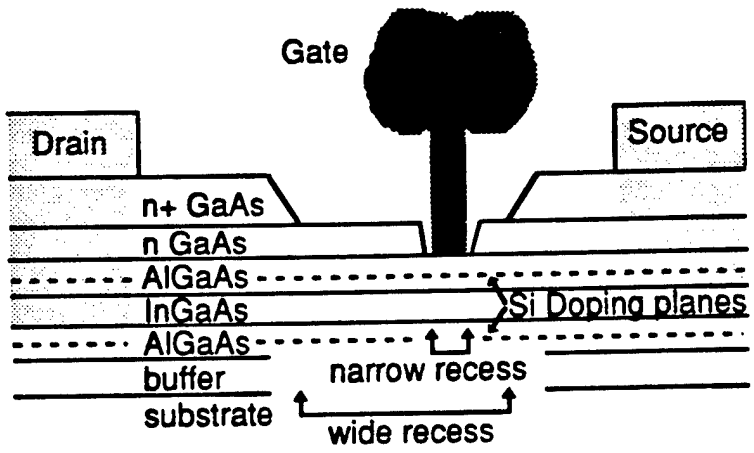


Figure 3.1. Schematic of a PHEMT device showing the wide and narrow gate recess trenches.

"double gate recess" and requires a critical alignment to be made during the second lithography step. This procedure has been applied to the fabrication of PHEMTs [3.7], MESFETs [3.8], and InP-based HEMTs [3.9]. The processes used in [3.10] and [3.11] to create a wide recess trench around the gate only require a single lithography step, but it is not possible to have an asymmetric recess around the gate with these techniques.

The fabrication of double-recessed gate PHEMTs using a four-layer resist technique will be presented in this chapter. The epitaxial structure of the PHEMT is shown in Figure 3.2. The PHEMT layer structure was grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. The epitaxial structure consisted of the following layers: 800 nm GaAs buffer, 100 nm GaAs/AlAs superlattice buffer, Si delta doping plane ($1x10^{12}$ cm^{-2}), 4.5 nm $Al_{0.25}Ga_{0.75}As$, 13 nm $In_{0.2}Ga_{0.8}As$ channel, 4.5 nm $Al_{0.25}Ga_{0.75}As$ spacer layer, Si delta doping plane ($4x10^{12}$ cm^{-2}),

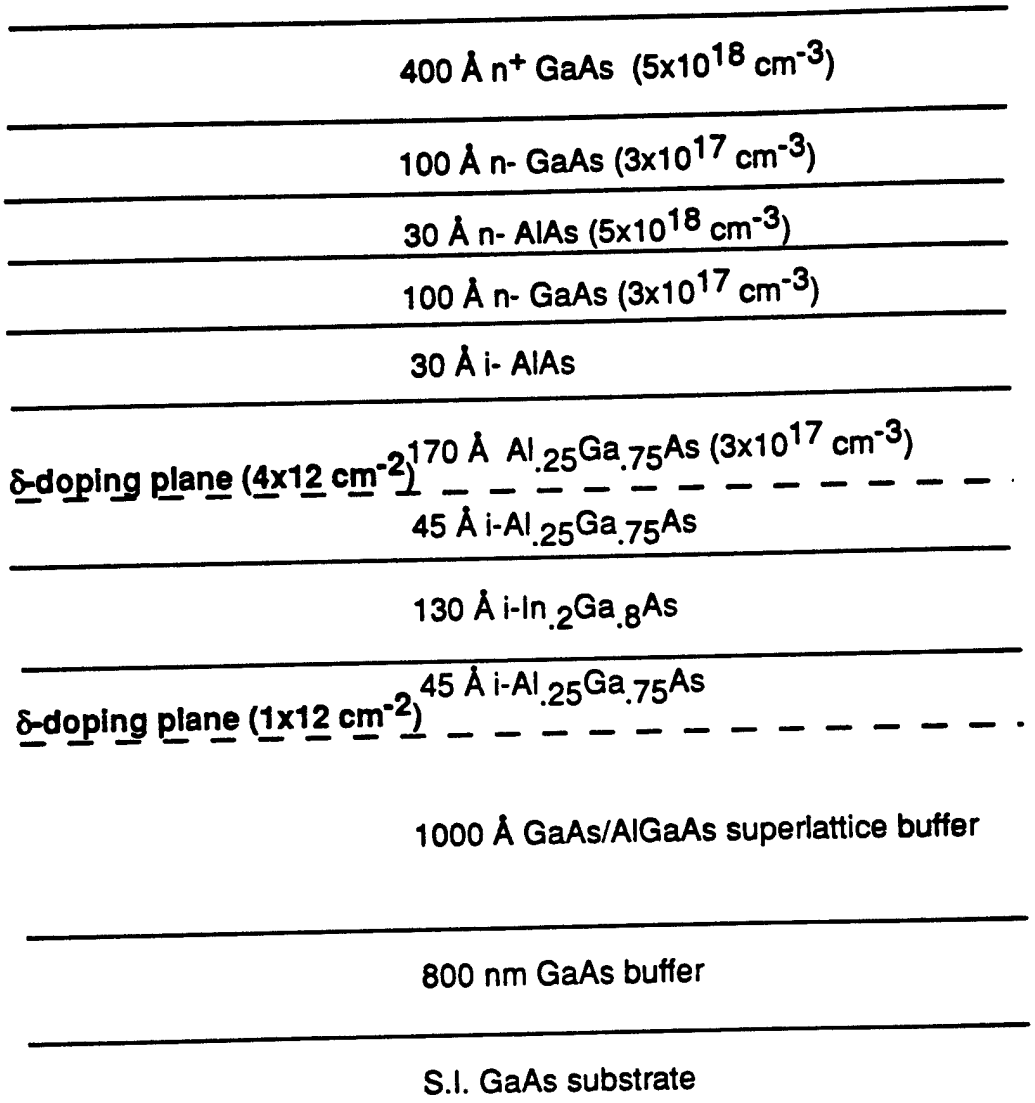


Figure 3.2. Schematic of the PHEMT layer structure used in the fabrication of devices in which the four-layer resist process was used.

17 nm $Al_{0.25}Ga_{0.75}As$ Schottky contact layer, 3 nm AlAs etch stop layer, 10 nm n^- GaAs sub-cap layer (Si, $3x10^{17}$ cm^{-3}), 3 nm AlAs etch stop layer, and 50 nm n^+ GaAs cap. Hall measurements at room temperature made with the GaAs cap and sub-cap removed yielded an electron sheet carrier density of $4x10^{12}$ cm^{-2} and mobility of 4000 cm^2/Vs, and at 77 K, the sheet carrier density and mobility were $3.8x10^{12}$ cm^{-2} and 7200 cm^2/Vs, respectively.

The first section of this chapter deals with the general fabrication issues including device isolation, ohmic contact formation, gate and overlay patterning, and gate recess. The second section presents an optimized four-layer resist process, which is capable of producing a profile that acts as both the etch mask for the asymmetric recess trench, as well as the liftoff mask for the T-shaped gate metal. The profile is achieved by using a single electron beam lithography exposure of poly(methylmethacrylate) (PMMA) and its copolymers P(MMA-MAA). The third section describes how the double-recessed gate is obtained through a sequential combination of wet and dry etching techniques. The final two sections of the chapter present the dc and rf results for PHEMTs that were fabricated using the double gate recess technique.

3.2 Fabrication

3.2.1 Device Isolation

The first step in the fabrication of PHEMTs is the isolation of the active area of the device. The active area is the region to which the current flow of the device is restricted; therefore, the device width is determined through definition of the active region. Mesa etching [3.12] and ion implantation [3.13] are the two methods that are commonly used to define the active areas of FETs. Mesa etching requires that the active semiconductor layers be removed everywhere except in the regions where the

device is to be defined. Ion implantation requires the implantation of an ion that gives the channel and doping layers semi-insulating properties.

Mesa etching was used to define the active areas of the PHEMTs. The mesa regions were patterned using optical lithography. The positive photoresist, which remained on the sample upon development, provided the etch mask in the regions where the active areas were to be defined. The requirements of the photoresist are that it is not etched by the etchant, and that it adheres well to the surface, so that the etchant cannot penetrate laterally and etch the active region. Wet chemical etching with nonselective, isotropic etching characteristics was chosen for the mesa etch. The isotropic etch ensured that the mesa had a gradually sloping profile; therefore, step coverage problems of subsequent metallizations that might result from the nonplanar surface were eliminated. A solution of H_3PO_4:H_2O_2:H_2O (3:1:50) with an etch rate of 14 Å/s was used to etch down to the semi-insulating superlattice buffer region. This ensured that there could be current flow only in the active region, because the doping and channel layers were removed outside of the active region.

3.2.2 Ohmic contacts

The formation of low-resistance ohmic contacts is very important for the dc and rf performance of PHEMTs. Low source resistance is necessary to achieve high transconductance. The source resistance R_S consists of the series combination of the contact resistance R_C and the sheet resistance R_{sh} of the semiconductor between the source and gate. The expression for R_S is given by

$$R_S = R_C + \frac{R_{sh} d_{sg}}{w} \tag{3.1}$$

where w is the width of the device, and d_{sg} is the distance between the source and gate. The extrinsic dc transconductance $g_{m,ext}$ is related to the internal transconductance $g_{m,int}$ by the expression

$$g_{m,ext} = \frac{g_{m,int}}{1 + R_s g_{m,int}} \tag{3.2}$$

Clearly, a low R_s is required to obtain high extrinsic transconductance. Equation (3.2) requires additional terms for the case of submicron gate length devices, where the output conductance $g_o = dI_D/dV_D$ can be large due short channel effects [3.14]. In the case where output conductance is substantial, $g_{m,ext}$ is expressed as

$$g_{m,ext} = \frac{g_{m,int}}{1 + (R_s + R_d) g_o + R_s g_{m,int}} \tag{3.3}$$

where R_d is the drain resistance, whose expression is very similar to (3.1), but d_{sg} is replaced by d_{dg}, the drain-to-gate distance.

A low R_c is also important for the rf performance of the PHEMTs. The unity current gain frequency f_T is directly related to the transconductance

$$f_T = \frac{g_{m,ext}}{2\pi(C_{GS} + C_L)} \tag{3.4}$$

with C_{GS} being the gate capacitance and C_L being the parasitic capacitance. From the above equation, one notices that as $g_{m,ext}$ increases, so does the speed (f_T) of the transistor.

The source and drain resistances depend on R_c and R_{sh}. The R_{sh} is dependent on the specific contact resistance ρ_c of the metal-semiconductor interface and on the sheet resistance of the semiconductor underneath the ohmic metal. The sheet resistance can be reduced by increasing the thickness and doping level of the cap layer. The ρ_c is dependent on the cap layer material and doping, ohmic metal types, and alloying process. Only R_c and R_{sh} are of interest for device characterization and were measured for the PHEMTs.

The ohmic pattern was aligned to the mesa regions and defined using an image reversal optical lithography process [3.15]. After resist development and immediately prior to loading the samples into an evaporator for metal deposition, the sample was

dipped into diluted HCl to remove any oxide that might hinder the formation of good ohmic contacts. A multilayer metal structure consisting of AuGe/Ni/Au was evaporated onto the sample with typical thicknesses being 2000 Å/350 Å/2000 Å. The samples were alloyed in both an alloy furnace with a nitrogen ambient and in a rapid thermal annealing system (RTA) with a nitrogen/hydrogen-forming gas ambient. It was found that the lowest R_c was obtained in the RTA. Also, better metal morphology resulted from the RTA annealing process. Good metal morphology is important, because if the height of the metal changes near the edge of the source and drain, variations in thickness of the resists that are spun on for gate definition may result. The variation in resist thickness would result in slight variations in gate length along the width of the transistor. Annealing for 20 s at 400 °C was the RTA process that yielded low R_c and good morphology. The values of R_c and R_{sh} were determined from transmission line model (TLM) measurements [3.16]. The typical normalized R_c was 0.1 Ωmm, and the measured R_{sh} was 148 Ω/square.

3.2.3 Gate and overlay definition

The gates were patterned with electron beam lithography using a Leica-Cambridge EBMF 10.5 system. The system is capable of exposing large numbers of patterns sequentially by using the software and automatic calibration routines. The automatic calibration routines require alignment marks near the transistors, and these metal marks were deposited with the ohmic metallization. Gate lengths of 0.1 μm are routinely achieved using multilayer resist processes. The specific resist structures and exposure details are presented in a following section.

Overlay metal patterns were exposed during the same electron beam writing step as the gates. The overlay metal patterns coincide closely with the ohmic metal region and are used for several reasons. First, upon the development of the gate and overlay patterns, the ohmic metal is exposed which allows the drain current I_D to be

monitored by means of a probe station during gate recess. Second, the metal that is evaporated to form the gate is also evaporated on top of the ohmic metal. This increases the metal thickness of the contact pads, reducing the resistance of the pads, as well as reducing the inductance at high frequencies. Also, the thick metal facilitates testing of the devices in that the probes used to test the devices make good contact to the pads. Figure 3.3 shows a fabricated PHEMT with a coplanar layout of the source, drain, and gate pads.

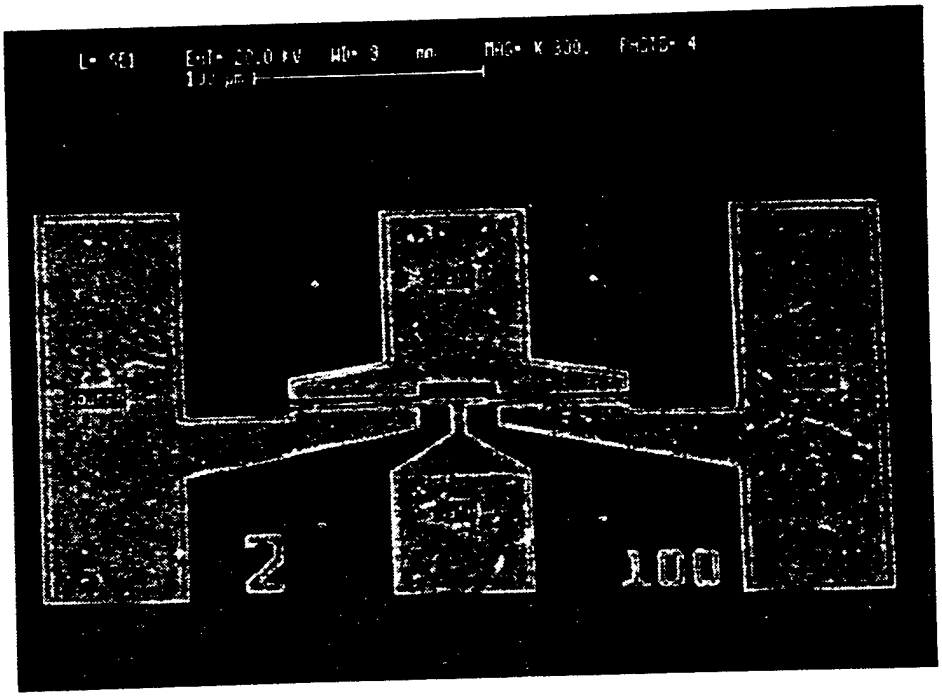


Figure 3.3. Scanning electron micrograph showing the coplanar layout of a PHEMT whose source-to-drain spacing is 2 μm and whose width is 100 μm. The source, drain, and gate contact pads are labeled.

3.2.4 Gate recess etch

After the development of the gate patterns in the resist, the GaAs cap is etched away from the gate regions. This allows the gate metal to be deposited on the underlying AlGaAs Schottky layer, which provides a high metal/semiconductor Schottky barrier height of ~0.8 eV [3.17]. The high Schottky barrier height limits gate current, thereby providing good modulation properties. The gate recess also provides high transconductance because the gate is moved closer to the channel, as was shown in Chapter 2. Recessing ensures that there is no parallel conduction path underneath the gate, and therefore, the carriers are restricted to the channel where they have the highest mobility. Finally, recessing determines the threshold voltage for the device.

For circuit applications, and device characterization in general, it is extremely important that uniformity in threshold voltage is obtained across the wafer and between wafer batches. Tong [3.18] has found that recess depth variations as small as 10 Å can cause threshold voltage discrepancies on the order of 0.1 V. The use of both wet and dry selective etchants with very high selectivities has reduced variations in etch depth and changed the main limiting factor for uniformity of devices from etching to epitaxial growth [3.19]. Wet etches that have been used in the fabrication of PHEMTs include citric acid:H_2O_2 [3.20] and NH_4OH:H_2O_2 [3.21] solutions. Dry etches that have been performed in a reactive ion etching chamber (RIE) include $SiF_4/SiCl_4$ [3.22] and CCl_2F_2 [3.23] plasmas. The citric acid:H_2O_2 and $SiF_4/SiCl_4$ etchants were used in the fabrication of the double-recessed gate PHEMTs. Before presenting the specific etch components and parameters for the gate recess, the four-layer resist scheme for the formation of the gates will be discussed.

3.3 Four-Layer Resist

The resists used were 950K PMMA and P(MMA-MAA) containing 7.5% and 18% MAA. The use of selective developers in conjunction with proper energy deposition was used to obtain the desired resist profile. In order to determine contrast and sensitivities of the resists, each of the four resists was spun on a clean wafer to a thickness of 400 nm, baked on a hot plate for two minutes, and exposed at multiple doses [3.24]. All exposures were performed using a Leica-Cambridge EBMF 10.5 system operating at 40 keV beam energy, 500 pA beam current, with a 60 nm beam diameter. Development of resists was carried out at 21 °C.

3.3.1 Resist characterization

Figure 3.4 shows the desired resist profile for attaining a T-shaped gate in an asymmetric recess trench. The bottom layer of resist defines the wide recess etch dimension and the top three layers combine to form the T-gate liftoff profile. The extent of the recess on the drain side (labeled L_{ud} in Figure 3.4) is larger than the extent of the recess on the source side (labeled L_{us} in Figure 3.4). The extent of L_{ud} is greater

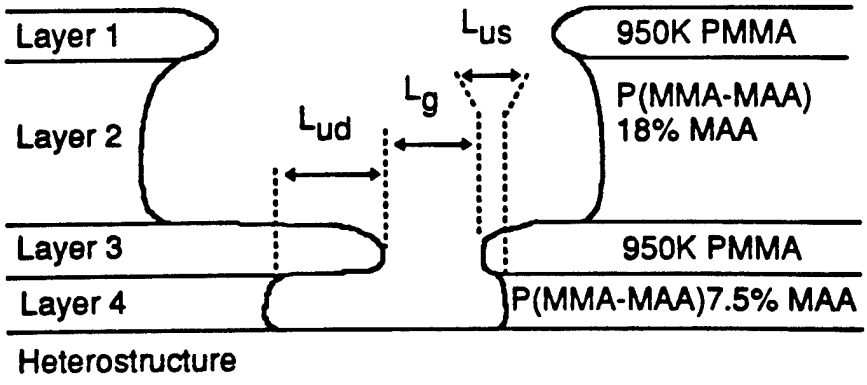


Figure 3.4. Schematic of the four-layer resist profile required for the formation of a T-gate in an asymmetric recess trench.

than L_{us} due to an area exposure (sidelobe) done on the drain side of the mainline exposure. The mainline exposure creates the gate footprint (labeled L_g in Figure 3.4).

In order to achieve the desired resist profile, it is important that each of the resists have reasonable contrast and a certain sensitivity. Contrast is a measure of the rate of resist chain scission and change of solubility, and sensitivity is a measure of the electron dose required for removal of the resist in a solvent. By using a sequential combination of developers, the resists may be selectively developed and the dimensions of L_t, L_{ud}, and L_g determined somewhat independently. The developers chosen were toluene, a mixture of isopropanol (IPA) and methanol, and a mixture of methylisobutylketone (MIBK) and IPA. The contrast curves for the relevant resist layers in the developers are shown in Figure 3.5(a)-(c). Toluene is used to develop the top resist layer (950K PMMA), leaving the second layer essentially untouched. A solution of IPA and methanol (1:1) is used to develop the second layer. Finally, a solution of IPA and MIBK (3:1) is used to develop the third and bottom layers. The IPA:MIBK solution offers the highest contrast and is used to accurately define L_g, L_{us}, and L_{ud}. By keeping L_{us} very small, low source resistance is maintained.

3.3.2 Resist profile dimensions

In order to characterize the dependence of L_g, L_{ud}, L_{us}, and L_t on various exposure parameters, gates were written, and upon development were inspected using a scanning electron microscope (SEM). Gates were written by performing a mainline exposure at a dose of 3.5 nC/cm followed by a sidelobe exposure on the drain side of the mainline. No sidelobe exposure was performed on the source side. The sidelobe area dose was varied from 40 to 160 $\mu C/cm^2$ and the mainline-to-sidelobe distance was varied from 0 to 0.15 μm. Sidelobes of widths 0.25 and 0.4 μm were patterned.

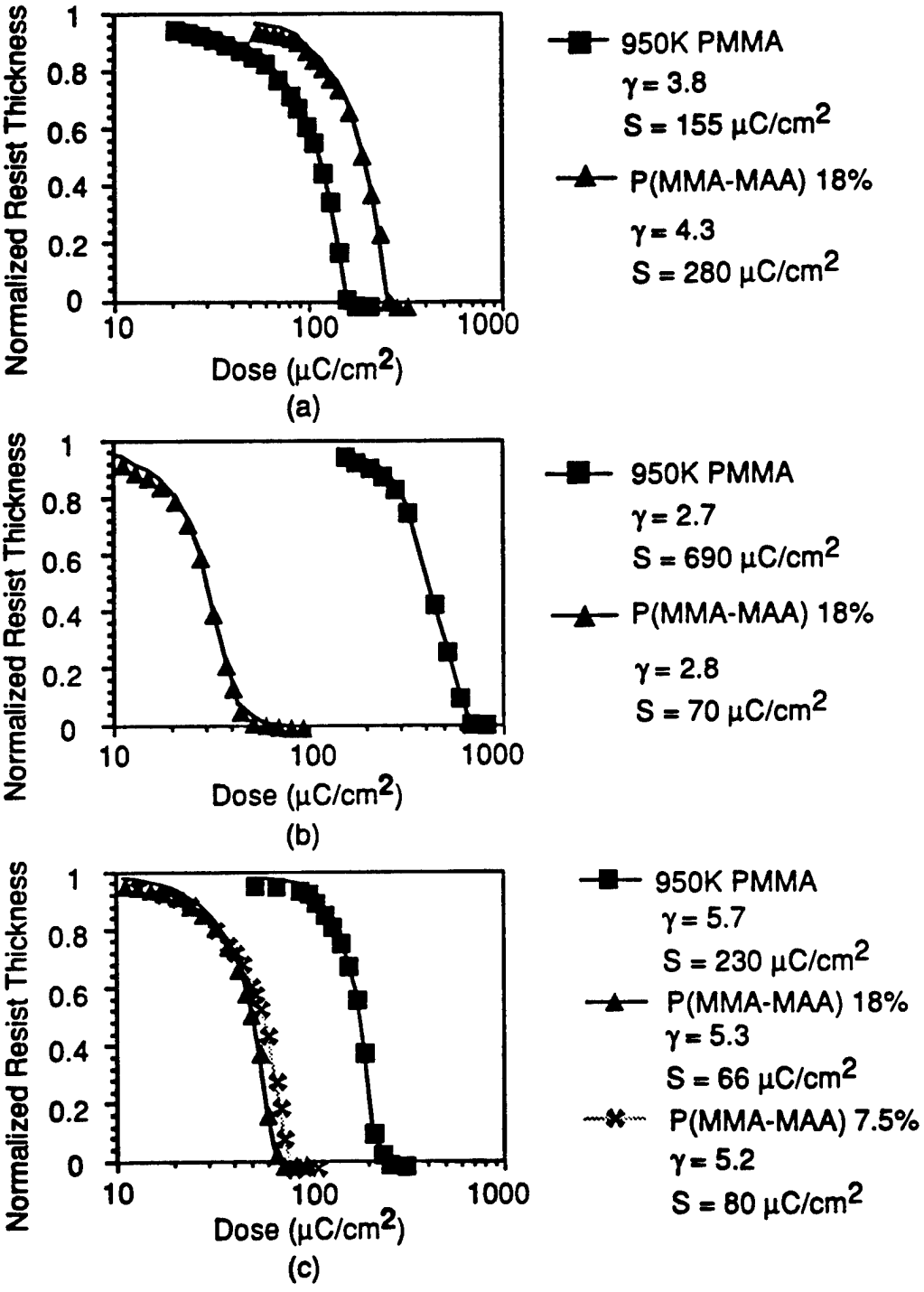


Figure 3.5. Contrast curves for each of the resists used in the four-layer process. Developers are (a) toluene, (b) IPA:methanol, and (c) IPA:MIBK. the contrast is γ, and S is the sensitivity of the resist.

Figure 3.6(a) illustrates the dependence of L_{ud} on sidelobe dose for various main-line-to-sidelobe distances for a sidelobe of width 0.25 μm, and Figure 3.6(b) is for a sidelobe width of 0.4 μm. There are several trends that are evident. The 0.4 μm-wide sidelobe creates a larger L_{ud} than the 0.25 μm-wide sidelobe for a given dose and mainline-to-sidelobe distance. As the mainline-to-sidelobe distance is increased from 0 to 0.1 μm, L_{ud} increases for a given sidelobe dose and width, but at a distance of 0.15 μm, L_{ud} decreases. For the distance of 0.15 μm, the proximity dose is too small to form the undercut in the bottom layer of resist between the mainline and sidelobe exposures. Even for certain sidelobe distances of 0.1 μm which are exposed at low dose (40 to 80 μC/cm^2), the proximity dose is too small to form the undercut, and L_{ud} is shorter than for cases of mainline-to-sidelobe distances of 0 and 0.05 μm.

Figures 3.7(a) and (b) show the dependence of L_g on the various exposure parameters. For a given sidelobe width, there is only a slight increase in L_g for sidelobe doses ranging from 40 to 120 μC/cm^2, but a noticeably greater increase at sidelobe doses of 160 μC/cm^2. For the sidelobe doses ranging from 40 to 120 μC/cm^2, L_g does not show a drastic increase at a particular mainline-to-sidelobe distance when sidelobe width is increased from 0.25 to 0.4 μm. For sidelobe doses of 160 μC/cm^2, the proximity effect of the sidelobe noticeably increases L_g. To study the effect of recess width on FET performance, it would be desirable to keep the sidelobe dose at or below 120 μC/cm^2 in order to have L_g remain nearly constant while L_{ud} varies.

The trends in L_t were similar to those of L_{ud}, and are shown in Figures 3.8(a) and (b). In all cases, L_{us} was found to be ~0.07 μm. Figure 3.9 shows the exposed and developed four-layer resist profile. The exposure parameters were a mainline dose of 4 nC/cm and a sidelobe of width 0.4 μm dosed at 80 μC/cm^2.

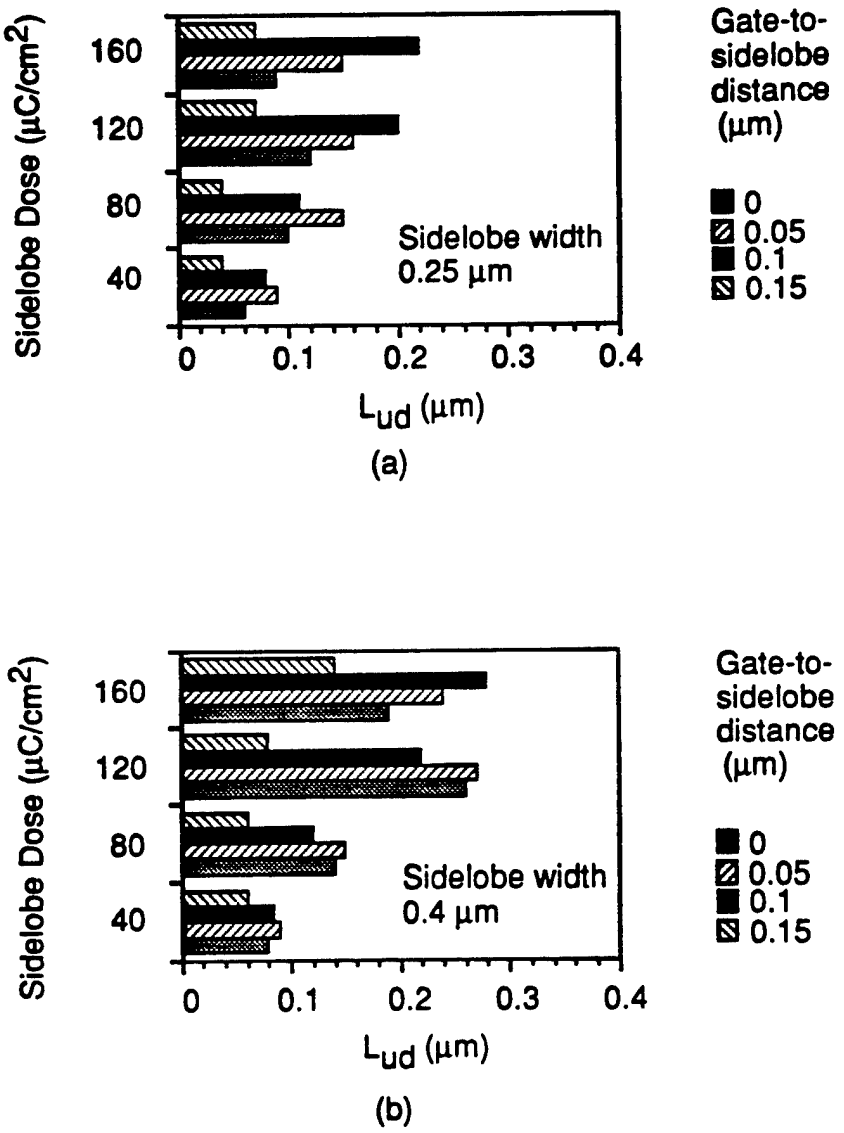


Figure 3.6. L_{ud} as a function of sidelobe dose and gate-to-sidelobe distance for (a) a sidelobe of width 0.25 μm, and (b) a sidelobe width of 0.4 μm. The mainline exposure dose is 3.5 nC/cm.

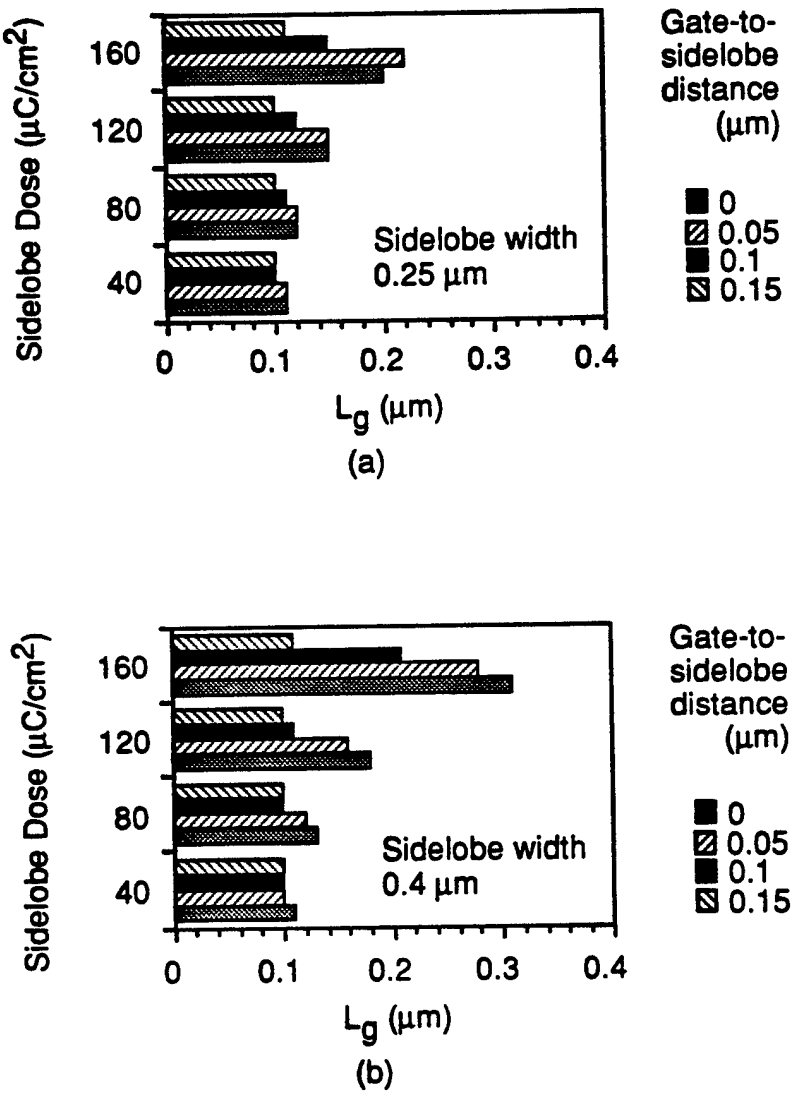


Figure 3.7. L_g as a function of sidelobe dose and gate-to-sidelobe distance for (a) a sidelobe of width 0.25 μm, and (b) a sidelobe width of 0.4 μm. The mainline exposure dose is 3.5 nC/cm.

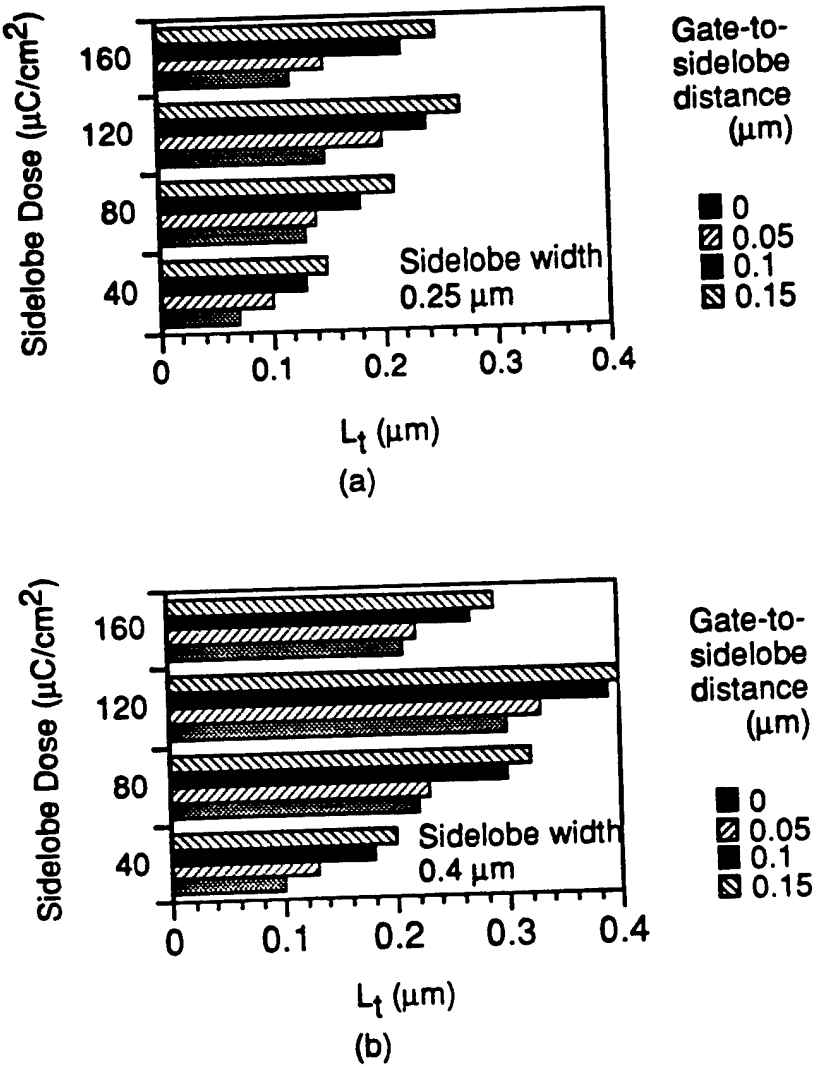


Figure 3.8. L_t as a function of sidelobe dose and gate-to-sidelobe distance for (a) a sidelobe of width 0.25 μm, and (b) a sidelobe width of 0.4 μm. The mainline exposure dose is 3.5 nC/cm.

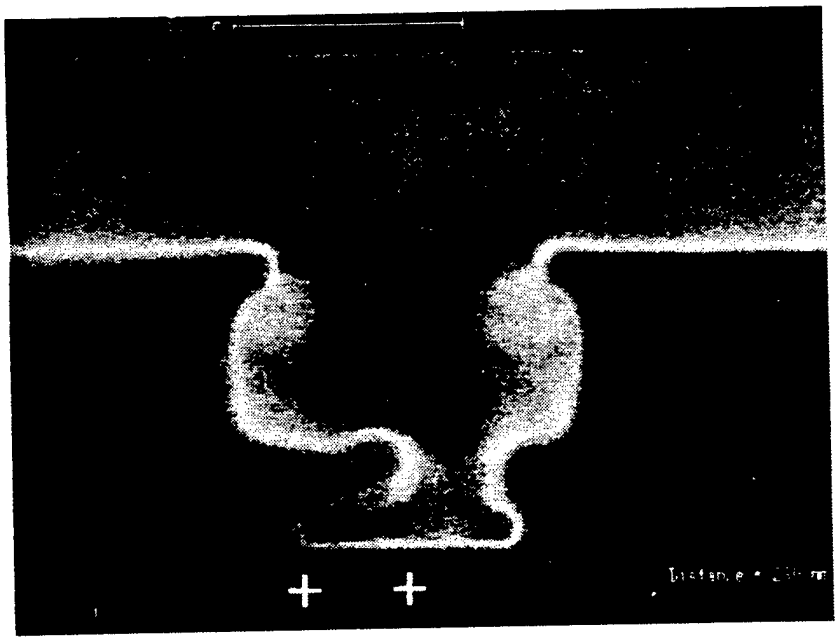


Figure 3.9. Scanning electron micrograph showing the developed four-layer resist profile.

3.3.3 Symmetric top and asymmetric recess

It is desirable for submicron gates to have a large Γ- or T-top in order to increase cross-sectional area, thereby reducing the end-to-end gate resistance and obtaining higher values of f_{max} [3.25]. By performing a weak sidelobe exposure on the source side of the mainline exposure, it is possible to increase the cross-sectional area of the top and obtain a symmetric T-top while having an asymmetric recess. The sidelobe on the source side was dosed at 30 to 40 $\mu C/cm^2$. This dose was high enough that the top two layers were developed, while the bottom two layers were not. An SEM micrograph of a symmetric T-top resist profile is shown in Figure 3.10. Upon metallization, end-to-end resistance of gates without the source sidelobe exposure were on the order of 28 Ω/mm, while the gates with the extra source sidelobe exposure were on the order of 16 Ω/mm.

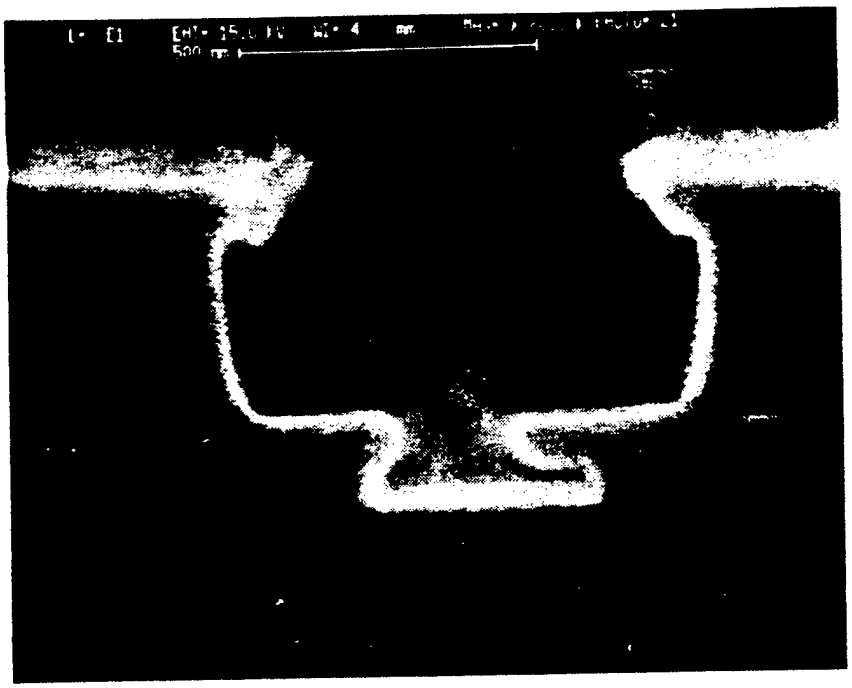
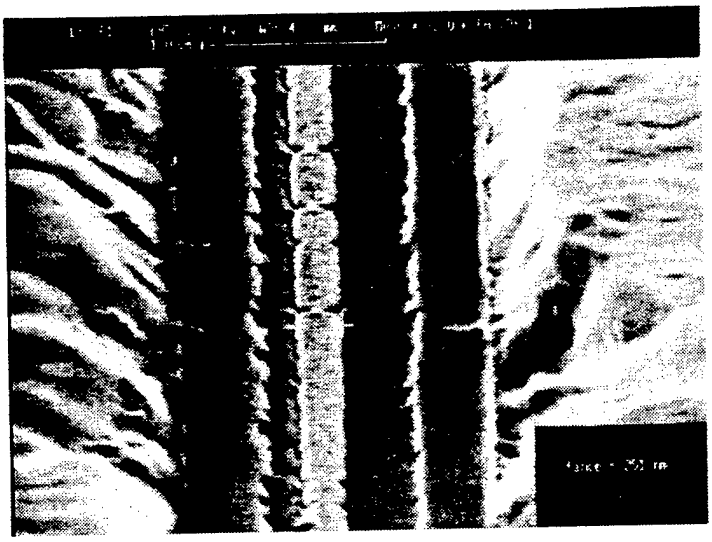


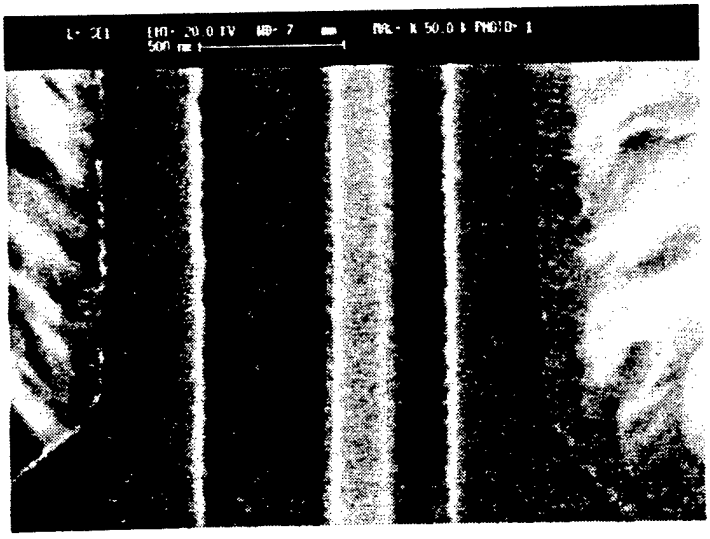
Figure 3.10. Scanning electron micrograph showing the developed four-layer resit profile with an asymmetric bottom layer of resist and a symmetric top (2 layers).

3.4 Gate Recess

Before performing the gate recess, the sample was placed in an oxygen plasma which removed the thin layer (<100 Å) of residual resist that might have remained on the developed gate regions [3.26]. Figure 3.11(a) shows a double recess trench that was performed without a prior oxygen plasma 'descum' and Figure 3.11(b) shows a double recess trench that was performed after the 'descum'. A thin layer of metal has been evaporated (400 Å) and covers the narrow recess etch trench in Figures 3.11(a) and (b). The sample that had no 'descum' performed (Figure 3.11(a)), has a rough etch edge profile, as well as inconsistent gate footprint metal coverage. The sample that had a 'descum' performed (Figure 3.11(b)), has good etch edge profile and gate footprint metal coverage. The 'descum' does lengthen the gate footprint by ~300 Å,



(a)



(b)

Figure 3.11. Scanning electron micrographs showing the double gate recess when performed (a) without prior oxygen plasma 'descum', and (b) with prior oxygen plasma 'descum'.

because the oxygen plasma attacks the resist; however, it is necessary to obtain a clean etch profile and gate footprint coverage. After the 'descum', the gate recessing was performed in two steps including a wet etch for the wide recess and a dry etch for the narrow recess and is described below.

A citric acid:H_2O_2 (4:1) solution [3.27] was used to selectively etch off the 50 nm n^+ GaAs cap. The etch defines the wide recess trench by penetrating under the lip created by the resist profile (layer 3). A concern was that air bubbles may be trapped under the Layer 3 resist lip and hinder the uniform etching of the cap. Therefore, the etch was performed in an ultrasonic bath to ensure that the etch penetrated uniformly under the Layer 3 resist lip. A weak ultrasonic bath was used to ensure that the resist profile and resist adhesion were not compromised. The etch rate of GaAs in the citric acid:H_2O_2 ultrasonic bath was found to be 55 Å/s, and the selectivity of GaAs over AlAs was found to be 1200. The cap was etched for 15 s to ensure complete removal, and the etch stopped on the AlAs layer. After the etch, the sample was dipped in dilute HCl to remove the AlAs etch-stop layer.

The sample was then loaded into a reactive ion etching (RIE) chamber for further etching in a $SiCl_4/SiF_4$ plasma [3.28]. The RIE etch is anisotropic and was used to create the narrow gate recess trench of width L_g, stopping on the second AlAs etch-stop layer. The composition of $SiCl_4$:SiF_4 was 1:9, and the chamber conditions were at a pressure of 90 mT with a plasma bias of -90 V. The resulting etch rate of bulk GaAs was ~1000 Å/min. The etch rate for the submicron structures, however, was slower and calibration on submicron structures was necessary to determine the time needed to etch the 100 Å thick GaAs subcap. After calibration, it was found that 45 s were needed to adequately perform the subcap etch.

By using the wet etch followed by the dry etch, the double-recessed profile is obtained. The final step before gate metal evaporation was the removal of the bottom AlAs etch-stop layer in dilute HCl. Figure 3.12 shows a four-layer resist profile with a

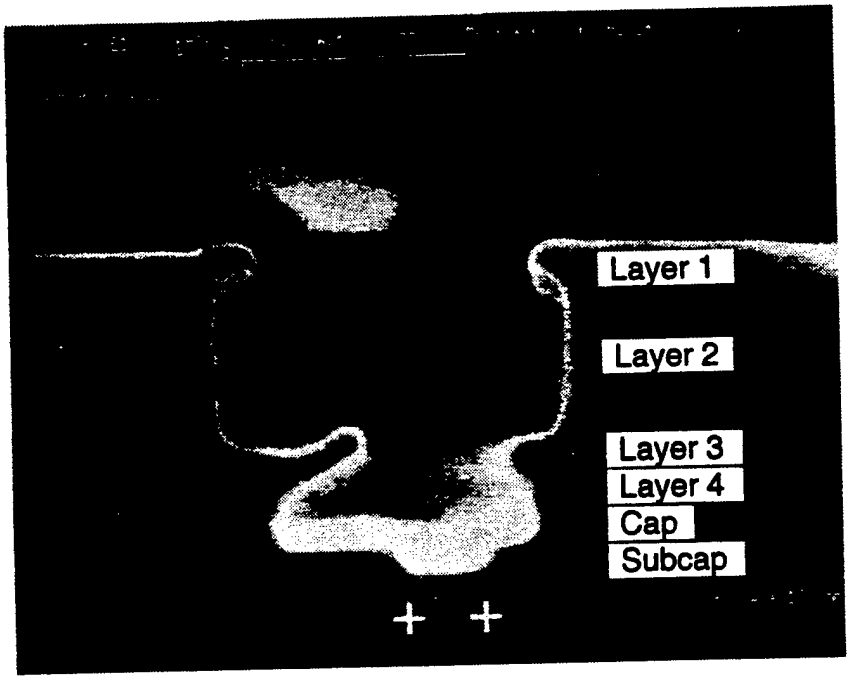
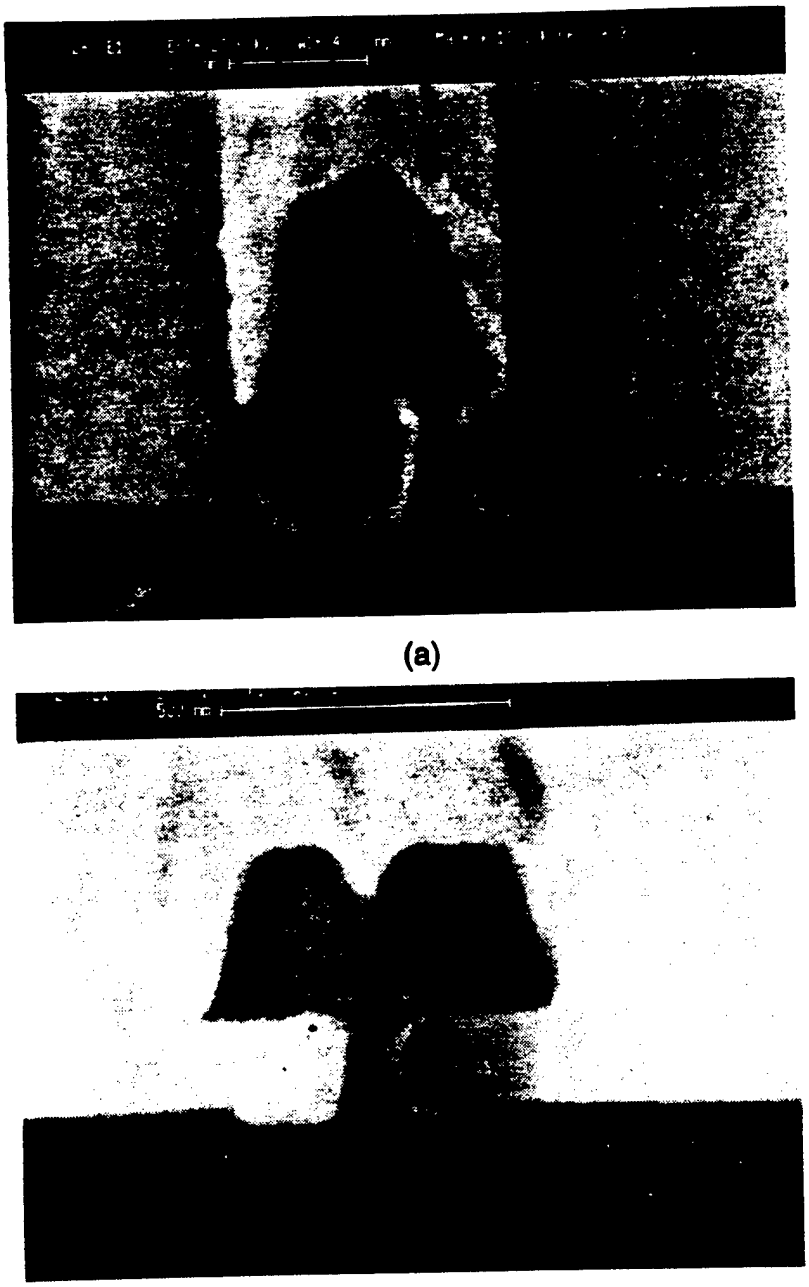


Figure 3.12. Scanning electron micrograph showing the four-layer resist and double-recessed heterostructure.

double-recessed heterostructure. The heterostructure in Fig. 3.12 was grown by MBE for purposes of characterizing the etching and consisted of (from top to bottom) 50 nm of n^+ GaAs, 3 nm of AlAs, 50 nm of n^- GaAs, 3 nm of AlAs, 100 nm $Al_{0.25}Ga_{0.75}As$, 800 nm GaAs buffer, and the GaAs substrate.

The evaporated gate metal consisted of a total of 3800 Å of Ti/Au. Figures 3.13(a) and (b) show a cross-sectional view of a gate on the double-recessed PHEMT epitaxial structure. The narrow recess is not easily seen because its recess depth is only 10 nm. After gate evaporation, parameters, L_g, L_{us}, and L_{ud} were thoroughly characterized using a scanning electron microscope. To assure accurate determination of L_g, L_{us}, and L_{ud}, chemically assisted ion beam etching (CAIBE) was used to etch through the gates and heterostructure and obtain an on-mesa



(a)

(b)

Figure 3.13. Scanning electron micrographs showing (a) an asymmetric T-gate, and (b) a symmetric T-gate on the double-recessed heterostructure.

cross-sectional view of the devices [3.29]. The inspection also revealed that the four-layer resist process was very reproducible for devices having similar layout and ohmic metal thickness.

3.5 Direct Current Characteristics

The dc device measurements were made using an Alessi REL-2100 probe station. An HP4142 dc Source/Monitor supplied all voltage biases to the devices. The HP4142 was controlled via an HP work station (bugsy), and IMA (Interactive Measurement and Analysis) software controlled bias conditions and performed data collection and analysis.

The source resistance (R_s) and drain resistance (R_d) were determined using the method described in [3.30]. In this method, drain-source, gate-drain, and gate-source I-V characteristics are used to evaluate R_s and R_d. The values of R_d and R_s are given in Table 3.1 for devices with varying L_{ud} and L_{us}. Only a slight increase in R_d was seen with increasing L_{ud}. Devices for which L_{ud}=0 μm and L_{us}=0 μm were fabricated using a trilayer resist instead of the four-layer resist. The trilayer resist was composed of the top three layers of the four-layer resist. The gate recessing was performed in the same way as the four-layer resist devices, which were described in the previous section.

Both on- and off-state breakdown voltages are of interest in the operation of PHEMTs. Figure 3.14 shows the reverse I-V characteristics between the gate and drain for varying values of L_{ud}. The measurement was made with the source floating, the drain held at 0 V, and the gate current swept from 0 to -1 mA/mm. The breakdown voltage, BV_{GD}, defined at a gate current of -1 mA/mm, increases with L_{ud} (from -8.2 V to -15.3 V) due to a reduction in the peak channel electric field at the drain edge of the gate [3.31], as well as a reduction in the surface leakage current between the increasingly distant highly-doped cap and the gate metal.

Table 3.1. Measured source resistance (R_s) and drain resistance (R_d) for PHEMTs with varying L_{ud}

Group	1	2
Gate resist process	Trilayer	Four layer with sidelobe exposure on drain side
Extent of recess towards drain, L_{ud}	0 μm	0.17 - 0.55 μm
Extent of recess towards source, L_{us}	0 μm	0.15 μm
Drain resistance, R_d	5.6 Ω	5.7 - 6.0 Ω
Source resistance, R_s	3.8 Ω	3.85 Ω

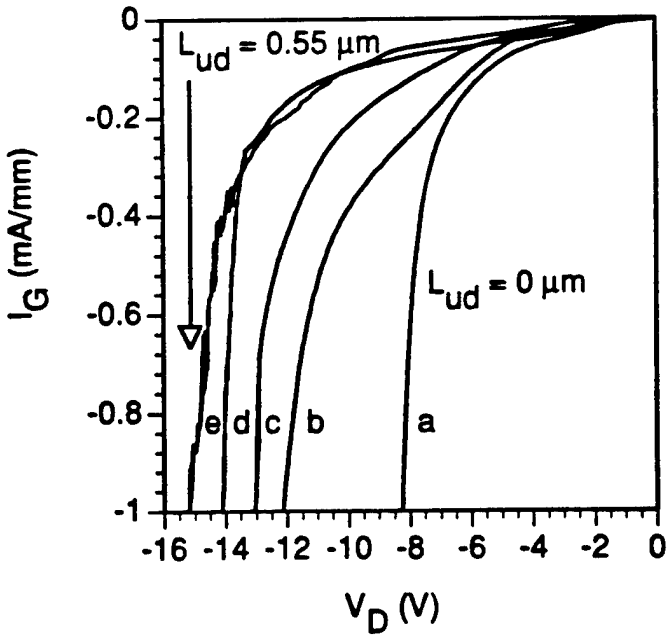


Figure 3.14. Reverse gate-drain breakdown characteristics evaluated at -1 mA/mm of gate current for PHEMTs with different values of L_{ud}. The successive curves are for L_{ud} of (a) 0, (b) 0.25, (c) 0.3, (d) 0.38, and (d) 0.55 μm.

All breakdown measurements were made on fresh devices to avoid the gate-drain breakdown walkout effect, which has been reported in both unpassivated [3.32] and passivated devices [3.33] and [3.34]. The gate drain breakdown walkout effect is the increasing of gate-drain breakdown voltage with the number of reverse gate voltage stress cycles. The effect has been attributed to a localized widening of the depletion region and subsequent reduction of the peak electric field on the drain side of the gate. The depletion region widening is due to either: (1) surface states that are caused by oxidation of AlGaAs/GaAs layers near the drain-side gate edge [3.32], or (2) a build up of negative charge at the semiconductor/passivation layer interface in the region between the gate and drain due to hot electrons in the channel [3.33].

Due to the significant increase in the two-terminal gate-drain breakdown voltage for the devices with large values of L_{ud}, it was necessary to investigate whether the device breakdown characteristics had such a marked improvement when the PHEMTs were biased as three-terminal devices. Figure 3.15 shows drain current versus drain-source voltage at pinchoff for devices with varying L_{ud}. The measurements were made with the source grounded, the gate biased slightly below pinchoff (-2.5 V), and the drain swept from 0 to 1 mA/mm. If the off-state drain-source breakdown voltage (BV_{DS}) is defined at 1 mA/mm of drain current, it can be seen that the asymmetric recess resulted in an increase in BV_{DS} from 5.2 V to 12.5 V when L_{ud} was increased from 0 to 0.55 μm.

The on-state drain-source breakdown voltage was also investigated for PHEMTs with varying L_{ud}. For this measurement, the source was held at 0 V, the drain voltage was swept from 0 to 10 V, and the gate was biased at a value that resulted in the drain current being half of the saturated drain current. The saturated drain current was defined as the drain current with a drain bias of 2.5 V and a gate bias of 0.7 V. The on-state drain-source breakdown measurement was a destructive measurement. Figure 3.16 shows the on-state drain-source breakdown characteristics for the

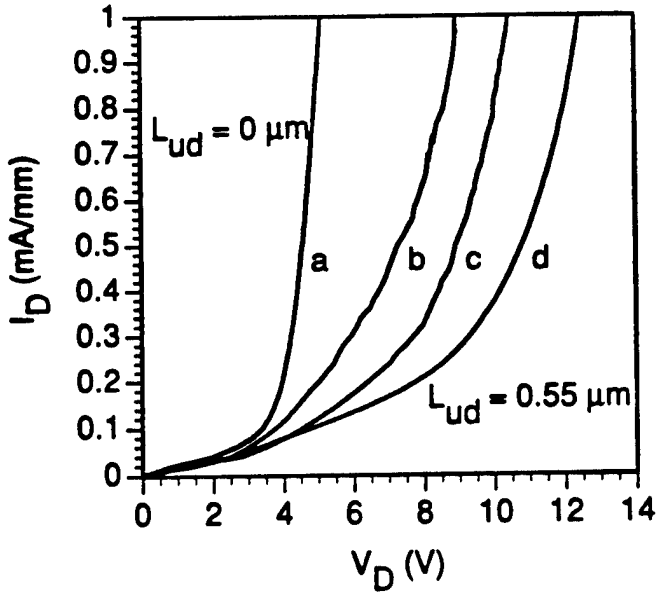


Figure 3.15. Off-state drain-source breakdown characteristics evaluated at 1 mA/mm of drain current for PHEMTs whose gate bias was such that devices were fully pinched off (V_G ~ -2.5V). The successive curves are for L_{ud} of (a) 0, (b) 0.3, (c) 0.43, and (d) 0.55 μm.

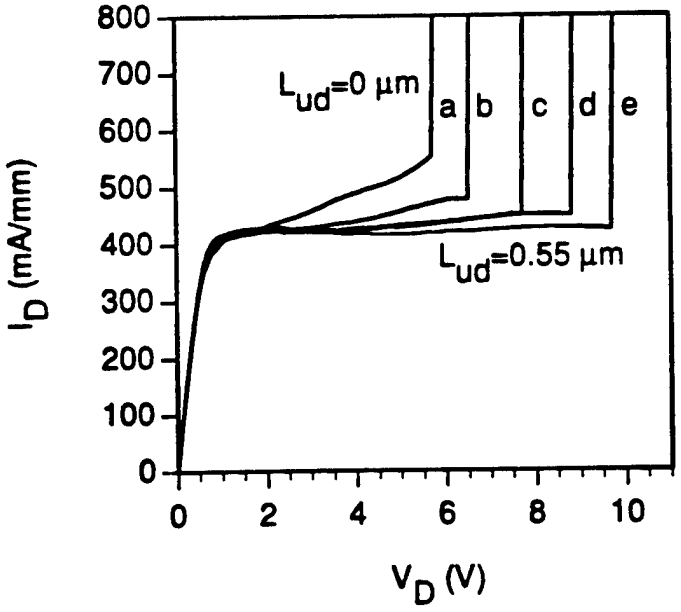


Figure 3.16. Drain current (I_D) vs. drain voltage (V_D) for PHEMTs with the gate biased such that the drain current is half of the saturated drain current value. The successive curves are for L_{ud} of (a) 0, (b) 0.17, (c) 0.3, (d) 0.43, and (e) 0.55 μm.

PHEMTs. The onset of breakdown was caused by impact ionization in the channel and was accompanied by a dramatic increase in drain current and gate current [3.5]. The on-state breakdown voltage increased from 5.6 V to 9.7 V for devices having L_{ud}=0 and 0.55 μm, respectively. The reduction in electric field strength in the channel with increasing L_{ud}, which resulted in reduced impact ionization, leads to the increase in breakdown voltage [3.35].

The maximum current capabilities of the devices were also of interest. Figures 3.17(a) and (b) display the I-V characteristics of devices with L_{ud} = 0 and 0.4 μm, respectively. From the plots, it is evident that the current levels for the asymmetrically recessed device are only slightly lower than those of the symmetrically recessed device. The current levels at a gate bias of 0.3 V and a drain bias of 2.5 V are 810 mA/mm, and 740 mA/mm for devices having L_{ud} of 0 and 0.4 μm, respectively. Figure 3.18 shows the decrease in the full-channel current density with increasing L_{ud} for the devices. Here, the full-channel current density is defined at a gate-source voltage of 0.7 V and a drain-source voltage of 2.5 V. The slight drop in current with increasing L_{ud} is primarily a result of the slight increase in R_s and R_d, and the relaxation of the electric field in the channel on the drain side of the gate.

From Figures 3.16 and 3.17(a) and (b), it is evident that PHEMTs with larger L_{ud} show improved (lower) output conductance, g_o ($g_o = dI_D/dV_D$). Low g_o is desirable because voltage gain increases as g_o decreases, assuming the transconductance (g_m) is constant. Figure 3.19 shows that the dc voltage gain, defined as g_m/g_o, increases steadily as L_{ud} increases, because g_m decreased only slightly, while g_o improved substantially. The improved g_o may be a result of: (1) a more effective screening of the source from the reduced drain field as L_{ud} is increased, and (2) a reduction of the number of electrons injected from the channel to the buffer regions due to the reduction of the electric field strength in the channel [3.36]. The increased

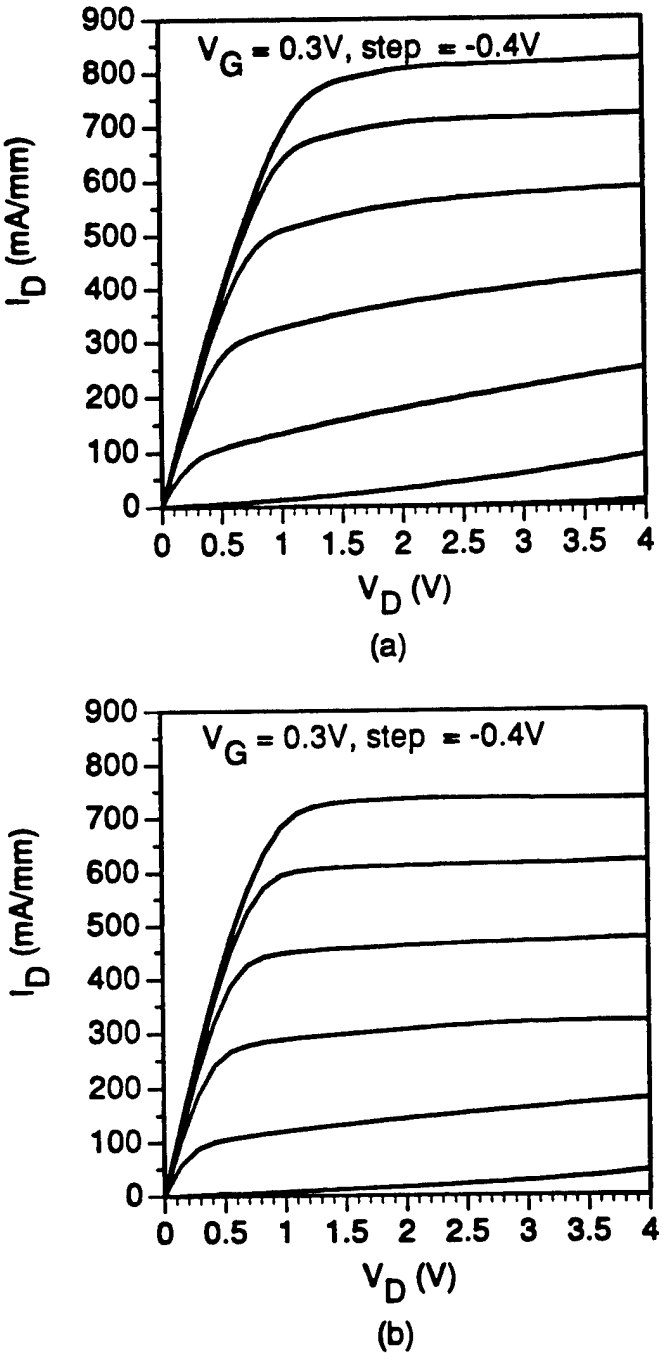


Figure 3.17. Drain current-voltage characteristics for PHEMTs that were (a) symmetrically recessed, and (b) asymmetrically recessed with L_{ud} of 0.4 μm. The gate bias is 0.3 V for the top curve and steps towards pinch-off in -0.4 V increments.

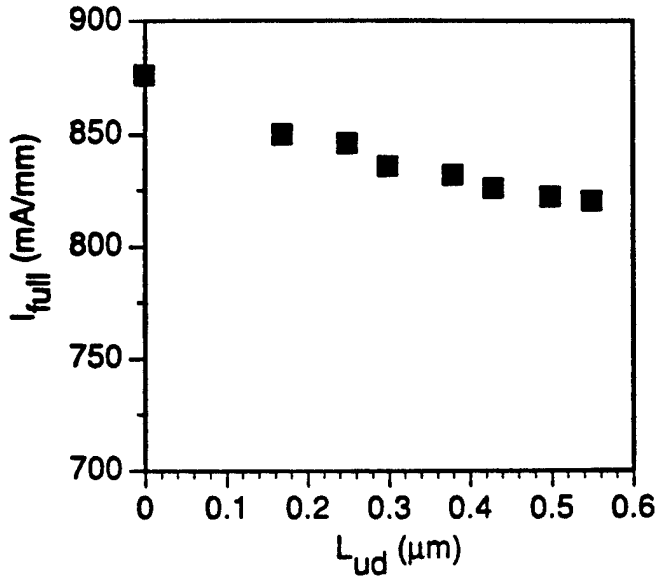


Figure 3.18. Full-channel current density (I_{full}) vs. L_{ud}. The full-channel current was defined at a gate-source voltage of 0.7 V and drain-source voltage of 2.5 V.

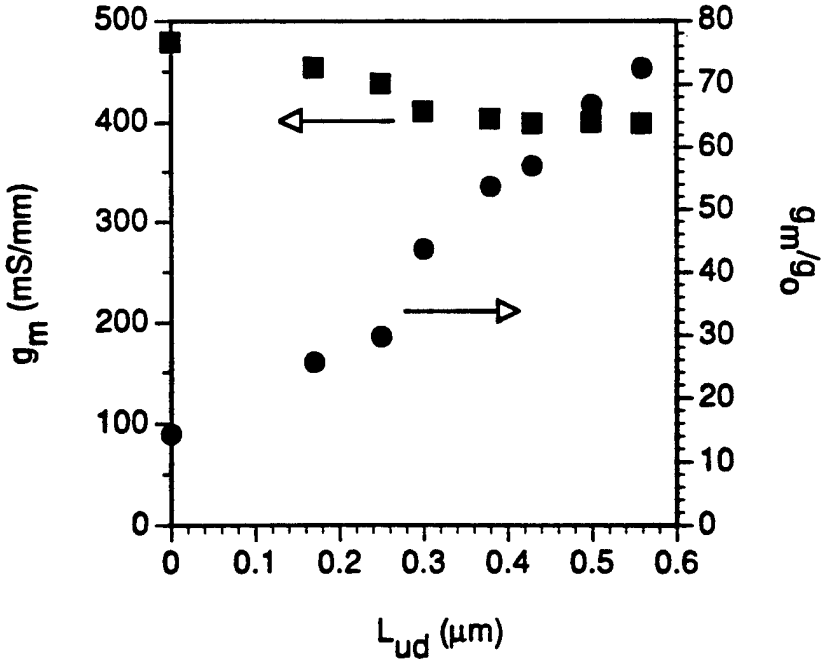


Figure 3.19. Extrinsic transconductance (g_m) and transconductance-to-output conductance ratio (g_m/g_o) vs. L_{ud}.

voltage gain observed with increasing L_{ud} is very desirable in that the number of stages in a specified power amplifier can be reduced.

When performing asymmetric recess, there is an inevitable trade-off involved even at dc; the reduction of the peak electric field increases the breakdown voltage and reduces g_o, but simultaneously decreases the full-channel current and g_m. The power capabilities of the devices are dependent on all of these quantities. Hence, it is important to determine what is being gained by using asymmetric recess, if the goal is to obtain a larger output power. A useful figure of merit is the product of off-state BV_{DS} and I_{full}, the full-channel current. This quantity is plotted in Figure 3.20. It can be seen that the asymmetric recess did improve this quantity by 100%, when comparing the PHEMTs with L_{ud} = 0 and 0.55 μm.

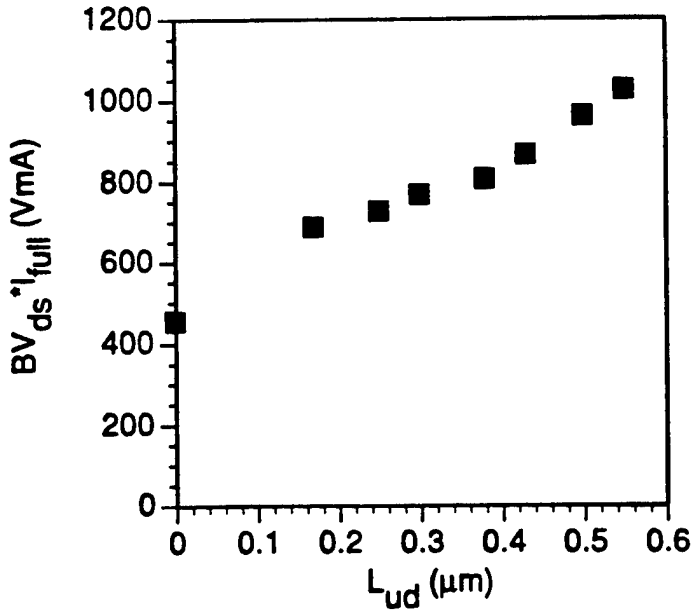


Figure 3.20. Plot of BV_{ds}*I_{full}, a figure of merit for high- power capability, vs. L_{ud}. BV_{ds} is the off-state drain-source breakdown voltage shown in Figure 3.15.

3.6 Microwave Characteristics

The microwave performance of the devices was evaluated by performing on-wafer scattering parameter (s-parameter) measurements from 1 to 35 GHz. The s-parameters are defined in terms of incident and reflected waves at the two ports, gate and drain. The s-parameters were measured using an HP 8510B Network Analyzer and a Cascade Microtech probe station equipped with 150 μm-period coplanar probes that fit the ground-signal-ground (GSG) layout of the devices. The bias voltages on the gate and drain were supplied by an HP4145 Semiconductor Parameter Analyzer and fed through the internal bias-T's of the test set. All of the instruments were controlled by an HP work station (escobar) and the ICCAP software. Before conducting measurements, the network analyzer, including the test set, rf signal generator, cables, and probes required calibration. The LRRM calibration method [3.37] was used to calibrate the output power level of the signal source, account for any attenuation or reflection in the system, and move the reference planes to the end of the probes.

The s-parameter measurements and HP MDS software were used to extract values of the intrinsic small-signal circuit model elements, where the model proposed by Hughes and Tasker shown in Figure 3.21 was used [3.25]. Intrinsic circuit element values were calculated after pad parasitics had been stripped from the raw s-parameter measurements. The parasitics include capacitances, inductances, and resistances. The parasitic capacitances were determined by performing s-parameter measurements on a passive structure (pads on semi-insulating GaAs) which had the same pad layout as the FETs [3.38]. To a first-order approximation, the input and output of the passive structure behave purely capacitively. The parasitic inductance was determined by performing s-parameter measurements on an FET that was biased in a cold-state [3.30]. In the cold-state bias condition, the drain and source are both held at 0 V, and a current is injected into the gate. All extrinsic parasitic values of

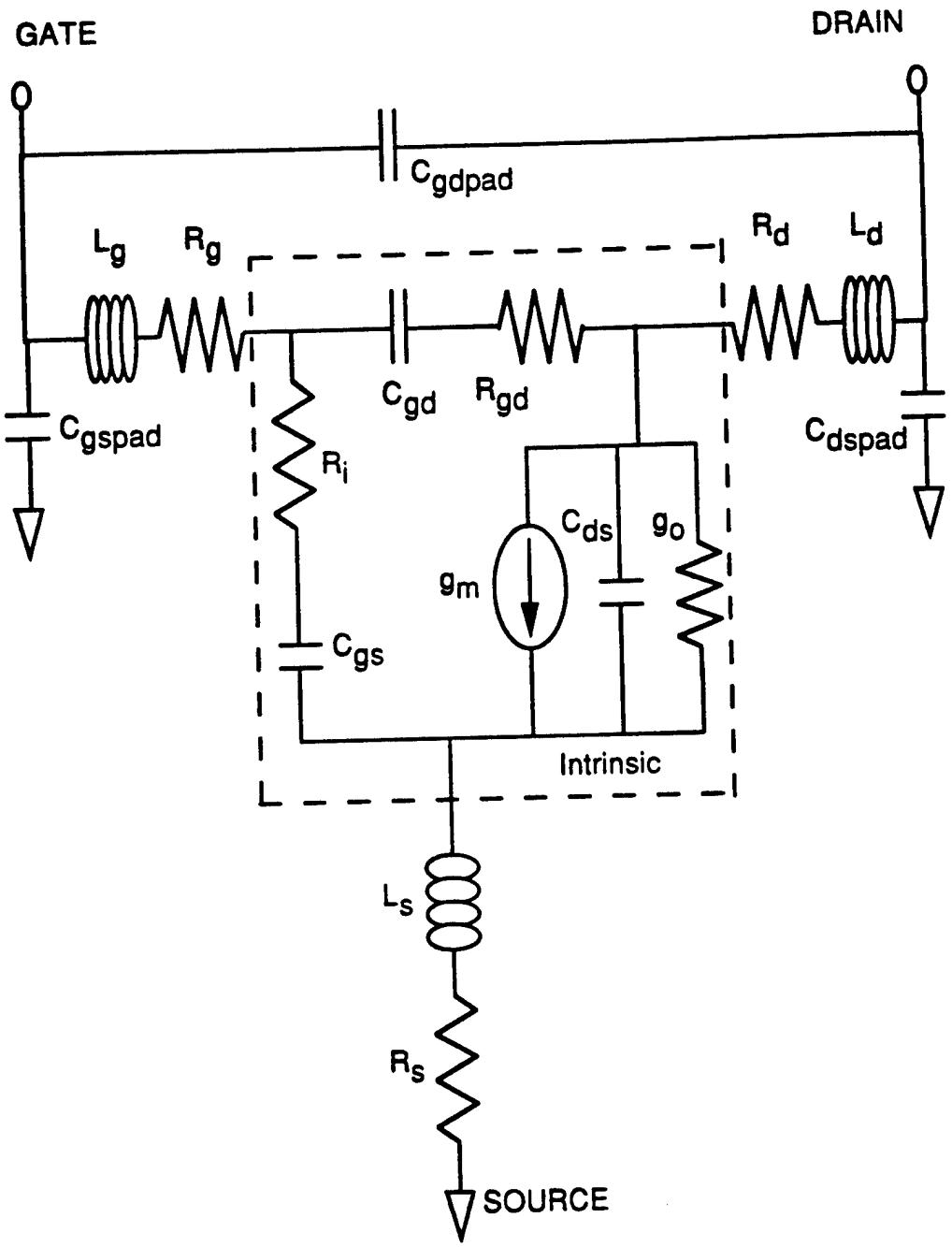


Figure 3.21. Small signal circuit of the PHEMT showing the intrinsic portion of the circuit within the dashed-line square. Extrinsic parasitic elements are outside the dashed-line square.

capacitance, inductance, and resistance are assumed to be independent of bias conditions [3.39]. The extrinsic element values of capacitances and inductances are given in Table 3.2, and those of resistance were shown previously in Table 3.1.

Upon calibration, s-parameter measurements were made on the PHEMTs. All devices displayed peak values of f_T, the unity current gain frequency, at a drain-source bias of ~1.1 V and peak values of f_{max}, the maximum frequency of oscillation, at a drain-source bias of ~4.0 V.

Table 3.2. Measured parasitic pad capacitances and inductances for PHEMTs fabricated using both the trilayer and four-layer resist processes.

Parameter	Measured value
Gate-source pad capacitance, C_{pgs}	15 fF
Gate-drain pad capacitance, C_{pgd}	4 fF
Drain-source pad capacitance, C_{pds}	15 fF
Drain inductance, L_d	40 pH
Source inductance, L_s	15 pH
Gate inductance, L_g	53 pH

Figure 3.22 shows the gate-drain feedback capacitance C_{gd} and the gate-source capacitance C_{gs} as a function of L_{ud}. These values were extracted from measurements taken at a drain-source bias of 4V. The general decrease in C_{gd} with increasing L_{ud} is to be expected, because the drain becomes increasingly isolated from the gate as the recess edge is moved away from the gate towards the drain. The decrease in C_{gd} saturated, because the capacitance is roughly inversely proportional to the effective gate-drain distance, and hence, for larger values of L_{ud}, there is a smaller change in C_{gd} for a fixed change in L_{ud}. The C_{gs} showed no clear dependence on L_{ud}, as would be expected, because it is largely determined by the gate length L_g, which is constant [3.40].

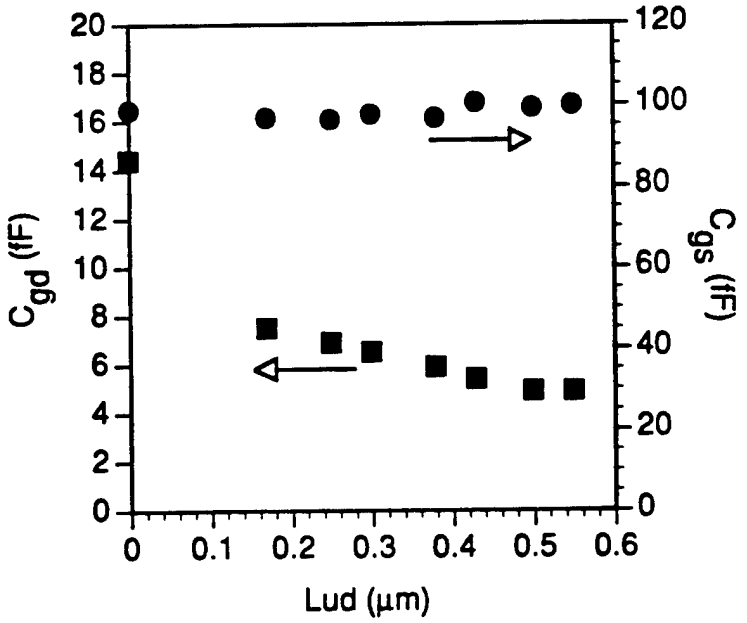


Figure 3.22. High frequency gate-drain (C_{gd}) and gate-source (C_{gs}) capacitances as a function of L_{ud}.

Figure 3.23 shows the intrinsic transconductance and transconductance-to-output conductance ratio as a function of L_{ud}. Again, values were extracted from the microwave measurements taken with a drain-source bias of 4 V. There was a decrease in the transconductance as L_{ud} was increased, primarily because the electric field profile in the channel spread out in the asymmetrically recessed devices causing deterioration in the modulation properties. However, the decrease in transconductance was accompanied by a decrease in the output conductance resulting in an increase in transconductance-to-output conductance ratio as L_{ud} was increased.

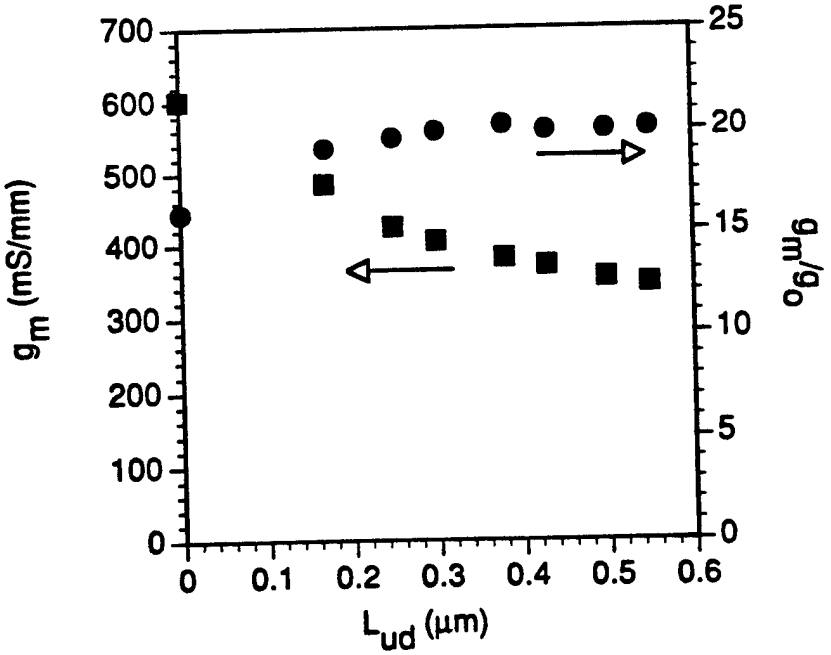


Figure 3.23. High frequency transconductance (g_m) and transconductance-to-output conductance ratio (g_m/g_o) vs. L_{ud}.

Figure 3.24 displays f_T and f_{max} versus L_{ud}, where f_T was measured at a drain-source bias of 1.1 V, and f_{max} was measured at a drain-source bias of 4 V. As shown in Figure 3.24, f_T decreased slightly as L_{ud} increased. This was primarily due to a decrease in the intrinsic high-frequency transconductance, as illustrated in Figure 3.23, as well as the increase in drain resistance which was shown in Table 3.1. A low drain resistance and high intrinsic transconductance are both necessary for a high value of f_T [3.41]. However, f_{max} increased slightly as L_{ud} increased. This was due to the reduced feedback capacitance C_{gd} and the improved g_m/g_o, which were obtained with increasing L_{ud} [3.42].

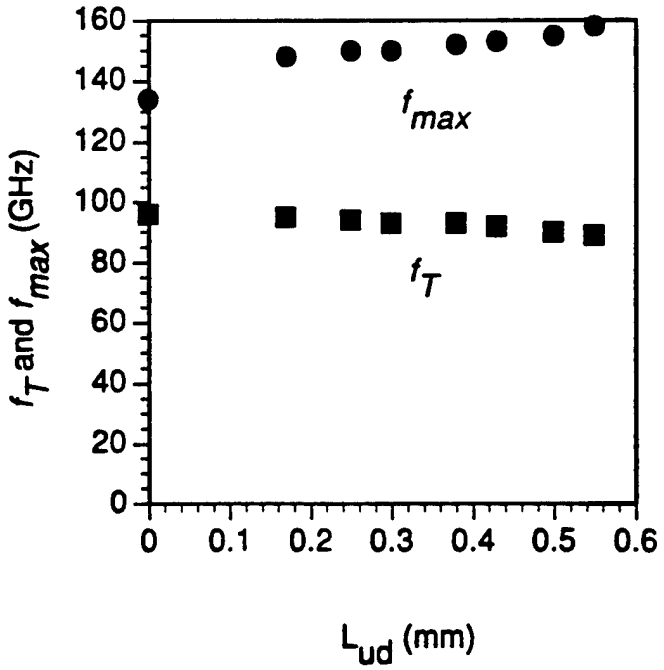


Figure 3.24. Unity current gain frequency (f_T) and maximum frequency of oscillation (f_{max}) vs. L_{ud}.

On-wafer power measurements were also performed at a frequency of 40 GHz. The input power was swept from -4 to 14 dBm, and the measurement system was tuned such that maximum power was delivered to and output from the device. The quiescent biasing conditions were a drain voltage (V_D) of 3 V and a gate voltage (V_G) of -0.025 V, which resulted in a drain current (I_D) of 630 mA/mm. The *PAE* (power added efficiency) and gain as a function of input power are shown in Figure 3.25, for a device whose L_{ud} is 0.4 μm. From the figure, it is seen that the maximum *PAE* is 12% and the maximum gain is 6.6 dB. It was also found that the output power at the point of maximum *PAE* was 295 mW/mm. The above figures of merit were on the lower edge the range of published results for similar devices. Published results of power characteristics at 40 GHz indicate *PAE*s of 15-25%, gains of 5-10 dB, and output power densities of 300-500 mW/mm [3.1].

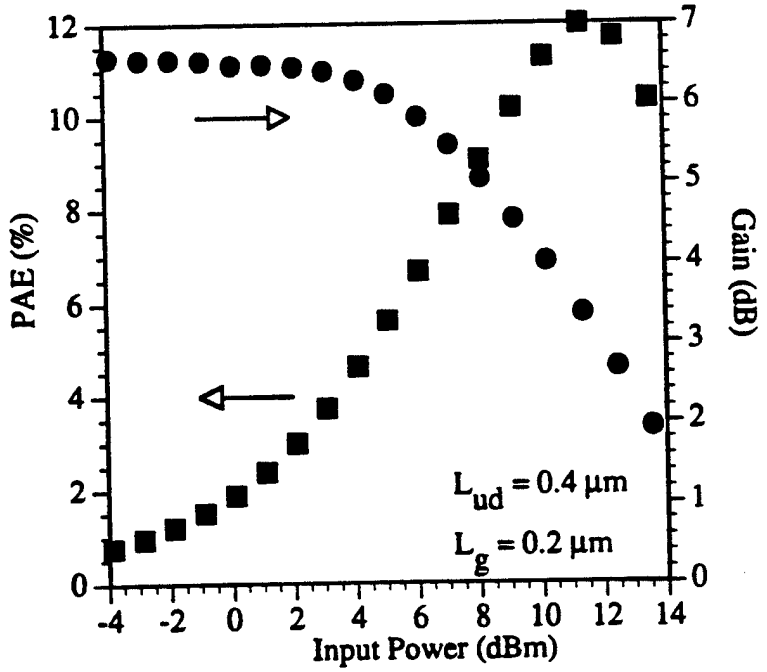


Figure 3.25. Power added efficiency (*PAE*) and gain as a function of input power. The characteristics shown are of a device whose gate length (L_g) is 0.2 μm and whose drain-side cap recess (L_{ud}) is 0.4 μm.

3.7 Pseudomorphic High Electron Mobility Transistor Synopsis

Both positive and negative effects of asymmetric gate recess on the performance of PHEMTs were observed. The primary positive effect of asymmetric recess was an increased gate-drain breakdown voltage, which was gained at the expense of the full-channel current. Other positive effects included a reduction of C_{gd} and g_o. The net result was an increase in the theoretical output power capabilities. A negative effect was the degradation of modulation properties (reduced g_m) as the extent of the recess toward the drain was increased. Ultimately, this led to a slight decrease in f_T for the asymmetrically recessed devices. Asymmetric recess led to an increase in f_{max}, presumably because the effect of the increased drain resistance was offset by the effect of an increased transconductance-to-output conductance ratio (g_m/g_o) and reduced feedback capacitance (C_{gd}). These effects have also been reported by Lester et al. [3.43]. In that work, an f_{max} of 350 GHz was obtained from an asymmetrically recessed 0.15 μm gate-length PHEMT. Although the high frequency performance of similar devices that were symmetrically recessed was not reported in that work, it is clear that high values of f_{max} are attainable when asymmetric recess is used.

The work presented here, in conjunction with [3.1], [3.4] and [3.5], has demonstrated the benefits of asymmetric recess to the realization of devices with larger breakdown voltages and potentially higher output power. Coupled with a judicious heterostructure layer design, asymmetric recess increased breakdown voltages in the on- and off-states with minimal degradation in full-channel drain current and transconductance. The single-step electron beam lithography process using the four-layer resist structure presented in this work, provided flexibility in asymmetric recess design; thereby, allowing an optimum power device to be fabricated.

3.8 References

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CHAPTER 4

LINEARITY OF PHEMTs AND DCFETS

4.1 Introduction

Linearity of device characteristics is an important issue for microwave power applications. A good linearity of the device characteristics can reduce the intermodulation of high frequency signals, thereby reducing the distortion problem under high power level operation [4.1]. As discussed previously, pseudomorphic GaAs/InGaAs high electron mobility transistors (PHEMTs) have demonstrated excellent characteristics for achieving high power and high frequency performance. For PHEMTs that have uniformly doped high bandgap donor layers, electrons can transfer into the donor layers under high current level operation and form a parallel conducting channel. This electron accumulation limits the linearity of the device I_D-V_G and I_D-V_D characteristics. Doped-channel field effect transistors (DCFETs) have demonstrated high linearity in device characteristics [4.2] and [4.3]. The parallel conduction can be minimized in the doped-channel approach because the high bandgap material is undoped.

Linearity studies have been made between DCFETs and PHEMTs with uniformly doped AlGaAs donor layers [4.4] and [4.5], but not between DCFETs and delta-doped PHEMT structures. The results comparing DCFETs and PHEMTs with uniformly doped AlGaAs donor layers seem to indicate that the DCFETs have more linear characteristics. Use of delta-doping planes instead of uniformly doped donor layers in PHEMTs may be helpful in improving the linearity of the devices. The double delta-doped PHEMT devices described in Chapter 3, showed extremely linear device characteristics. Figure 4.1 shows the characteristic for a PHEMT (described in Chapter 3) biased at V_D of 2.5 V with L_g of 0.2 μm and L_{ud} of 0.4 μm. Figure 4.1 also shows the characteristic for a 1 μm gate length DCFET that had an n_s of 7.9×10^{12} cm^{-2}

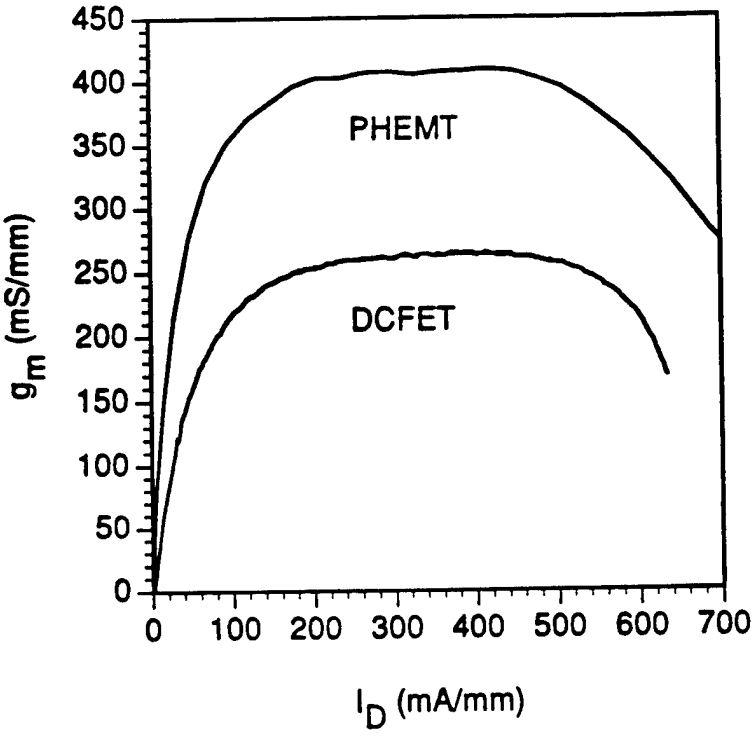

Figure 4.1. Transconductance (g_m) versus drain current (I_D) for a PHEMT with L_{ud} = 0.4 μm and L_g = 0.2 μm as described in Chapter 3, and for a DCFET from [4.1].

from [4.1]. Clearly, the curves of Figure 4.1 are quite comparable and show a large range of constant g_m, with respect to I_D. The question is whether the comparison is valid, because the devices have different carrier concentrations, gate-to-channel distances, and gate lengths. This question of validity in comparison is also a concern in the results presented in [4.4] and [4.5], where the DCFET and PHEMT devices in the comparison have different carrier concentrations and/or gate lengths.

This chapter examines the linearity characteristics of GaAs/$In_{0.2}Ga_{0.8}As$ DCFETs and PHEMTs. The heterolayers used in the study were designed such that

the carrier concentration below the gate was the same for both the DCFET and PHEMT. The heterolayers were also designed such that the gate-to-channel distance, Schottky barrier height at the gate electrode, and the gate lengths were the same. In this way, the dependency of linearity on the placement of the dopant atoms could be studied.

The first section of the chapter deals with the general theory of nonlinear effects in two-ports. The second section of the chapter examines the factors that contribute to nonlinearities in DCFETs and PHEMTs. The final section of the chapter presents the experimental results of the DCFET and PHEMT comparison.

4.2 Nonlinear Effects in Two-Ports

For small signal inputs, two-ports can often be modeled as linear. The relationship between the input $v_i(t)$ and the output $v_o(t)$ is given by

$$v_o(t) = k_1 v_i(t-\tau) \tag{4.1}$$

where k_1 is the magnitude of the small signal voltage gain, and τ is a delay representing a frequency-dependent phase shift. If the input is made up of two signals $v_{i1}(t)$ and $v_{i2}(t)$, superposition applies, and the relationship between the input and output is given by

$$v_o(t) = k_1 v_{i1}(t-\tau) + k_2 v_{i2}(t-\tau) \tag{4.2}$$

where k_1 and k_2 are the magnitude of the small signal voltage gain, and τ is a delay.

In general, for large input signals, the input-output relationship must be considered to be nonlinear. Ignoring frequency-dependent phase shifts, the general nonlinear input-output relationship is given by

$$v_o(t) = f(v_i(t)) \tag{4.3}$$

where $f()$ is a nonlinear function. In the case of $v_i(t) = v_{i1}(t) + v_{i2}(t)$,

$$v_o(t) = f(v_{i1}(t) + v_{i2}(t)) \neq f(v_{i1}(t) + f(v_{i2}(t)) \tag{4.4}$$

indicating that superposition does not apply. For large signals, an arbitrary nonlinear function can be expanded in a Taylor series about an operating point. If the total input signal is given by x_t

$$x_t = x_q + x \tag{4.5}$$

where x_q is the constant component, and x is the time varying component, and the total output signal is given by y_t

$$y_t = y_q + y \tag{4.6}$$

where y_q is the constant component, and y is the time varying component, then

$$y_t = f(x_t) = f(x_q) + f'(x_q) + \frac{1}{2}x^2 f''(x_q) + \ldots + \frac{1}{n!}x^n f^n(x_q) \tag{4.7}$$

The time varying part of the output can be written as

$$y(t) = k_1 x(t) + k_2 x^2(t) + k_3 x^3(t) + \ldots \tag{4.8}$$

where the first term represents the linear relationship existing under low-level conditions, and higher-order terms represent the nonlinear distortions. Allowing x and y to represent the input and output voltages of the system (for example the gate voltage and drain voltage of a FET), the relationship may be written as

$$v_o(t) = k_1 v_i(t) + k_2 v_i^2(t) + k_3 v_i^3(t) + \ldots \tag{4.9}$$

It is sufficient to consider only third-order terms and lower for most large input signals, and these terms will be considered in the analysis that is discussed below. The analysis follows that found in [4.6].

Considering a single input signal of the form

$$v_i(t) = A\cos\omega t \tag{4.10}$$

the output is given by

$$v_o(t) = \frac{1}{2}k_2 A^2 + \left(k_1 A + \frac{3}{4}k_3 A^3\right)\cos\omega t + \frac{1}{2}k_2 A^2 \cos 2\omega t + \frac{1}{4}k_3 \cos 3\omega t \tag{4.11}$$

If only the output component at the fundamental frequency (ω) is considered, detailed analysis shows that the coefficient k_3 will always have a sign that is opposite of k_1 [4.7]. The output term of (4.11) at the fundamental frequency is then given by

$$v_{o\omega}(t) = k_1 A\left(1 - \frac{3}{4}A^2\frac{|k_3|}{k_1}\right)\cos\omega t \tag{4.12}$$

The term in parenthesis will reduce the amplitude of the fundamental component due to the presence of the term containing k_3. This phenomenon is called gain compression [4.8]. Figure 4.2 shows the fundamental component of output power as a function of input power for the linear case (k_3 absent from (4.12)) and the nonlinear case (k_3 present in (4.12)). The power gain of the two-port is the slope of the curve, and the slope is reduced at higher values of input power. The gain compression of a two-port is often characterized by the input power level that causes the gain to be decreased from the linear case by 1 dB.

If we now consider two input signals that are closely spaced in frequency of the form

$$v_i(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t \tag{4.13}$$

then the output is given by

$$\begin{aligned} v_o(t) = {} & k_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) \\ & + k_2\left(\frac{1}{2}(A_1^2 + A_2^2) + \frac{1}{2}A_1^2\cos 2\omega_1 t + \frac{1}{2}A_2^2\cos 2\omega_2 t\right) \\ & + k_2(A_1A_2\cos(\omega_1+\omega_2)t + A_1A_2\cos(\omega_1-\omega_2)t) \\ & + k_3\left(\frac{3}{4}A_1^3 + \frac{3}{2}A_1A_2^2\right)\cos\omega_1 t + k_3\left(\frac{3}{4}A_2^3 + \frac{3}{2}A_2A_1^2\right)\cos\omega_2 t \\ & + \frac{1}{4}k_3A_1\cos 3\omega_1 t + \frac{1}{4}k_3A_2^3\cos 3\omega_2 t \\ & + \frac{3}{4}k_3A_1A_2^2(\cos(2\omega_2-\omega_1)t + \cos(2\omega_2+\omega_1)t) \\ & + \frac{3}{4}k_3A_1^2A_2(\cos(2\omega_1-\omega_2)t + \cos(2\omega_1+\omega_2)t) \end{aligned} \tag{4.14}$$

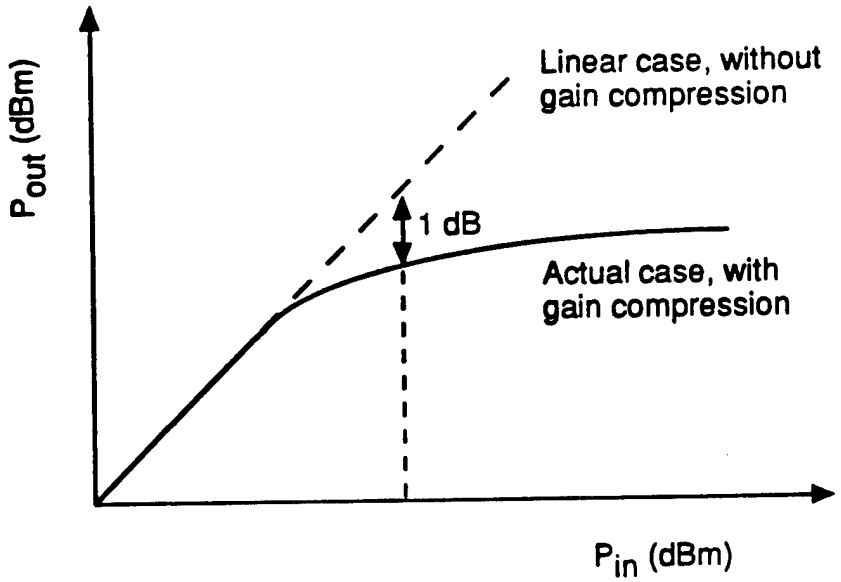

Figure 4.2. Fundamental component of output power as a function of input power for the linear and nonlinear case. Gain compression is seen in the nonlinear case.

Figures 4.3(a) and (b) show the input and output spectrums, respectively. In narrow band systems, most of the frequency components of the output spectrum will be filtered out. The in-band third-order terms ($2\omega_1$-ω_2 and $2\omega_2$-ω_1) cannot easily be filtered out, because they have frequencies that are close to the fundamental frequencies (ω_1 and ω_2). In wideband systems, all terms can become significant. For the following discussion, only the in-band terms will be considered. Suppose that $A_1\cos\omega_1 t$ is the desired small signal, but there is a strong signal $A_2\cos\omega_2 t$ at a neighboring frequency. The amplitude of the desired term is given by

$$v_{o\omega 1} = k_1 A_1 \left(1 - \frac{3|k_3|}{2k_1} A_2^2 \right) \tag{4.15}$$

which shows that the amplitude of the desired term will be reduced as the amplitude of A_2 increases. The presence of $A_2\cos\omega_2 t$ at the input effectively reduces the gain of the

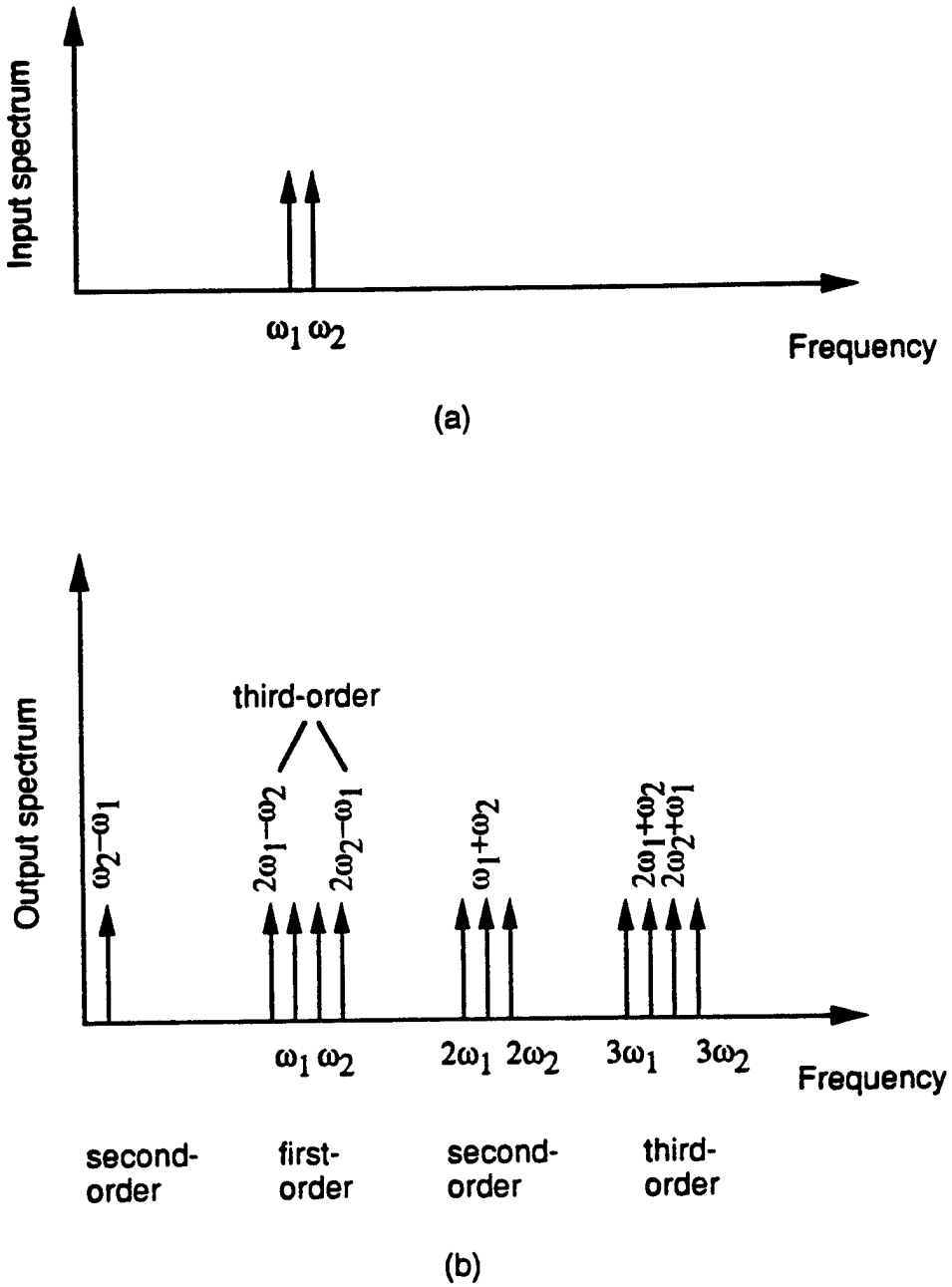

Figure 4.3. The (a) input spectrum, and (b) output spectrum of a two-port.

two-port, and this phenomenon is termed desensitization. In the extreme case where the amplitude of the $\cos\omega_2 t$ is very large, the desired signal can be completely blocked. If both input signals are modulated, another undesirable effect may result. Suppose that the input signals are amplitude modulated, and the signal at the input is

$$v_i(t) = A_1(1+m_1(t))\cos\omega_1 t + A_2(1+m_2(t))\cos\omega_2 t \tag{4.16}$$

The in-band components of the desired output signal are given by

$$v_{o\omega 1}(t) = k_1 A_1(1+m_1(t)) - \frac{3|k_3|}{2} A_1(1+m_1(t))A_2^2(1+m_2(t)) \tag{4.17}$$

showing that the amplitude modulation from signal two has been transferred to signal one. This effect is called cross-modulation.

The nonlinearity effects that are caused by the presence of multiple input signals at two-ports can be compared quantitatively using the two-tone intermodulation distortion test (IMD). Two input signals of equal amplitudes are applied

$$v_i(t) = A(\cos\omega_1 t + \cos\omega_2 t) \tag{4.18}$$

If the amplitude is small enough that gain compression does not occur, the in-band component at the output is given by

$$v_o(t) = k_1 A(\cos\omega_1 t + \cos\omega_2 t) + \frac{3k_3}{4} A^3(\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t) \tag{4.19}$$

Defining the input power of each signal as

$$P_{in} = \frac{1}{2} A^2 \tag{4.20}$$

The output power of the desired fundamental components is

$$P_d = \frac{1}{2} k_1^2 A^2 = k_1^2 P_{in} \tag{4.21}$$

The output power of the in-band third-order intermodulation products is

$$P_{im} = \frac{9}{4} k_3^2 P_{in}^3 \tag{4.22}$$

Notice that the undesired component of P_{im} increases as the cube of P_{in}. Figure 4.4 shows the relationship between P_{in} and the output components, P_d and P_{im}. Because P_{im} increases faster than P_d, P_{im} and P_d will intersect at some value of P_{in}. The input power at which P_d and P_{im} intersect is termed the input two-tone third-order intercept level. The intercept point is fictitious, because gain compression has been ignored, and in actuality, both the P_d and P_{im} curves would saturate. For matters of simply comparing two-ports, the saturation does not cause problems. The intercept point is important, because if it is known, a system can be designed to operate in the range where the third-order intermodulation will not significantly affect the system performance. The IMD test has been used to characterize the linearity of MESFETs [4.9] and DCFETs [4.10]. In the next section, factors that contribute to the linearity of DCFETs and HEMTs are considered.

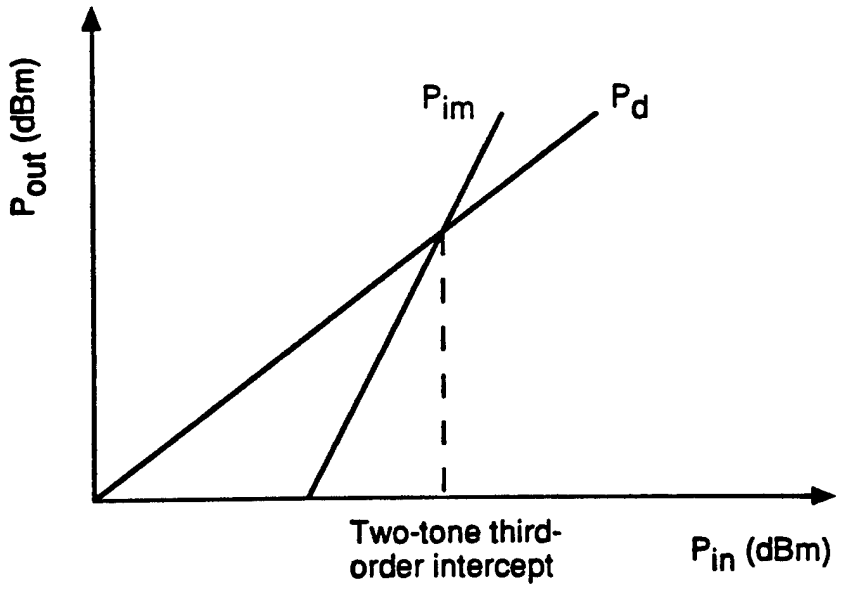

Figure 4.4. Schematic showing the relationship between the output power of the desired fundamental component (P_d) and the in-band third-order intermodulation product (P_{im}).

4.3 Nonlinearity of DCFETs and HEMTs

4.3.1 Background

The dominant contributions to nonlinear response of FETs come from the variation of transconductance (g_m) with gate voltage and from the variation of drain conductance (g_o) with drain voltage, with additional secondary contributions arising from the voltage dependence of the gate-source capacitance, C_{GS} [4.11]. In the low-power signal region, the contributions of the g_o variations dominate IMD, and as the power of the signal increases, the contributions of g_m variations dominate IMD. The goal in achieving good linearity is to have a device whose g_m is large and has a wide flat peak as a function of V_G, and whose g_o is low and slowly varying with V_D. This will ensure good linearity and high voltage gain over a large range of V_G and V_D.

Both the transconductance and gate-source capacitance are inversely proportional to the gate-to-2-DEG distance, d, as seen from (2.5) and (2.7). To reduce the input voltage-dependent nonlinearities, the relative change of d must be decreased. In MESFETs, it has been shown that the profile of the dopants plays an important role in IMD [4.12]. It was found that by inserting a low-doping region between the gate and highly doped channel region of an MESFET, the IMD could be reduced. The MESFET that had such a low-doped region between the gate and highly doped channel is essentially a DCFET.

In double pulse-doped PHEMTs, it has recently been shown that good linearity can be achieved by the optimization of the pulse profile [4.13]. The ideal profile minimizes the presence of parasitic charge in the wide bandgap material. Parasitic charge results in parallel conduction, which leads to nonlinearities. The following discussion presents the basic equations that relate gate voltage to the charge control in DCFETs and PHEMTs. The charge control in DCFETs and PHEMTs is also investigated through use of a one-dimensional Schrödinger-Poisson simulation program.

4.3.2 Basic theory of HFET linearity

In a conventional HEMT with the drain and source both grounded, n_s is given by [4.14]

$$n_s = \frac{\varepsilon_o \varepsilon_s}{qd}(V_G - V_T) \tag{4.23}$$

where ε_s is the relative permittivity of the Schottky layer, d is the gate-to-channel separation, V_G is the gate-to-channel voltage, and V_T is the threshold voltage. Clearly, n_s is linearly dependent on the gate-to-channel voltage V_G, and this holds true for V_G sufficiently greater than the pinchoff voltage, V_T. For DCFETs, expressions for n_s are not found in the literature and will be derived here.

Using the depletion approximation and assuming that the gate bias depletes the electrons from the doped channel, n_s can be expressed by

$$n_s = N_c(c - t_o) \tag{4.24}$$

where N_c is the density of donor atoms in the channel, c is the thickness of the channel, and t_o is the thickness of the depleted charge in the channel. The task is to find t_o. From energy band considerations (see Figure 4.5), the following can be written

$$\phi_B - V_G = V_s + \Delta E_c + V_c - V_o \tag{4.25}$$

where ϕ_B is the Schottky barrier height, V_G is the applied gate bias, V_s is the voltage drop across the Schottky layer, ΔE_c is the conduction band discontinuity between the Schottky and channel layer, V_c is the difference between the conduction band and Fermi level in the channel, and V_o is the voltage drop in the depletion region of the channel.

The electric field in the Schottky layer is constant and originates at the heterointerface between the Schottky and channel layers. The electric field at the

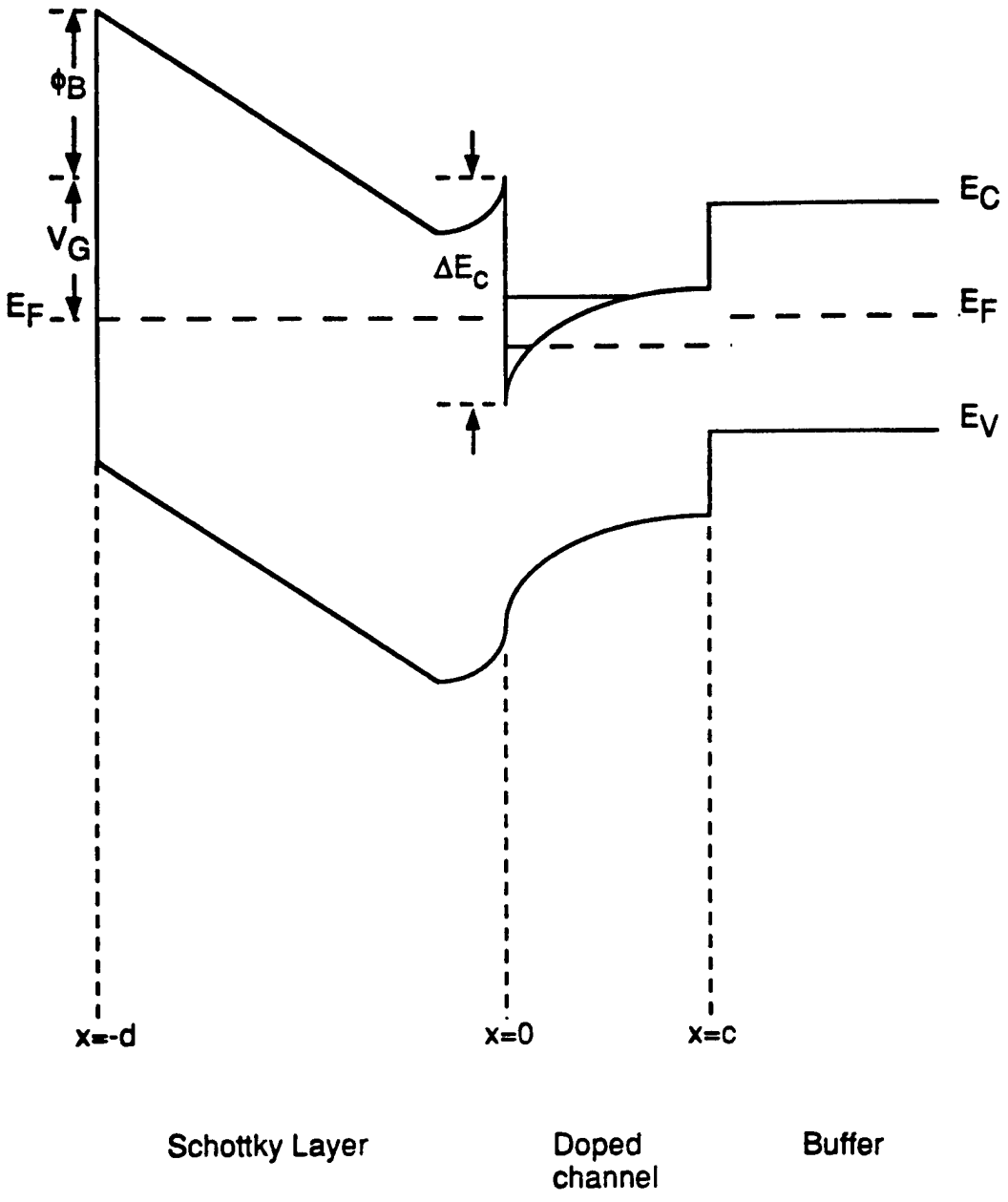

Figure 4.5. Schematic showing the energy bands of a PHEMT heterostructure including the Schottky, channel, and buffer layers.

interface is given by

$$E_o = \frac{qN_c t_o}{\varepsilon_o \varepsilon_c} \tag{4.26}$$

where ε_c is the relative permittivity of the channel layer. The voltage drop across the Schottky layer is then given by

$$V_s = \frac{qN_c t_o d}{\varepsilon_o \varepsilon_c} \tag{4.27}$$

Using the Poisson equation, the voltage drop in the depleted region of the channel is found to be

$$V_o = \frac{qN_c t_o^2}{\varepsilon_o \varepsilon_c} \tag{4.28}$$

Combining (4.24), (4.26), and (4.27) results in

$$\phi_B - V_G - \Delta E_c - V_c = \frac{qN_c d t_o}{\varepsilon_o \varepsilon_c} - \frac{qN_c t_o^2}{\varepsilon_o \varepsilon_c} \tag{4.29}$$

which is a quadratic equation for t_o and is solved using the quadratic formula. The solution is found to be

$$t_o = \frac{d - \sqrt{d^2 + \frac{4\varepsilon_o \varepsilon_c}{qN_c}(\phi_B - V_G - \Delta E_c - V_c)}}{2} \tag{4.30}$$

Combining (4.23) and (4.29) yields the expression for n_s which is given by

$$n_s = N_c\left(c - \frac{d}{2} + \frac{1}{2}\sqrt{d^2 + \frac{4\varepsilon_o \varepsilon_c}{qN_c}(\phi_B - V_G - \Delta E_c - V_c)}\right) \tag{4.31}$$

Clearly, this approximate relationship between n_s and V_G is not linear for the case of the DCFET.

4.3.3 One-dimensional charge control simulations

A one-dimensional Poisson-Schrödinger solver using the method of finite differences has been used to simulate the n_s under the Schottky gate of a DCFET and PHEMT. The solver was obtained from G. Snider and is an extension of his Ph. D. dissertation [4.15]. The solver was run on an Apple computer and is capable of generating the one-dimensional band diagram. The input to the solver is a text file that contains the information necessary to simulate the structure including thicknesses and types of materials. The parameters (energy gap, band offset, relative dielectric constant, effective masses of holes and electrons, etc.) for materials including $In_xGa_{1-x}As$ and $Al_xGa_{1-x}As$ are contained in the simulator.

The structures that were simulated are shown in Figure 4.6. They are the layer structures on which the devices were fabricated as described in the next section. To determine the n_s at varying gate bias, simulations were performed without the n+ GaAs cap and n- AlAs etch-stop layers present. The gate bias (V_G) was varied from pinchoff ($n_s = 0$) to saturation ($n_s = n_{so}$). The n_s as a function of V_G is shown in Figure 4.7 for both the PHEMT and DCFET. It is seen that the curves are comparable for the V_G, ranging from pinchoff to ~ 0.6 V. For V_G above 0.6 V, the DCFET shows continuing increase of n_s, while the n_s of the PHEMT begins to saturate. This compression of n_s modulation for the PHEMT can be attributed to the formation of a parallel electron region in the AlGaAs Schottky layer [4.2]. The parallel charge in the Schottky layer limits n_s modulation in the channel at high V_G.

The simple one-dimensional simulation of charge control shows a larger V_G range of linear n_s modulation for the DCFET. Effects of parasitic device parameters including the capacitance, inductance, and resistance associated with the source, drain, and gate were not considered, however. The next section shows experimentally the comparison of device characteristics which are important for linearity.

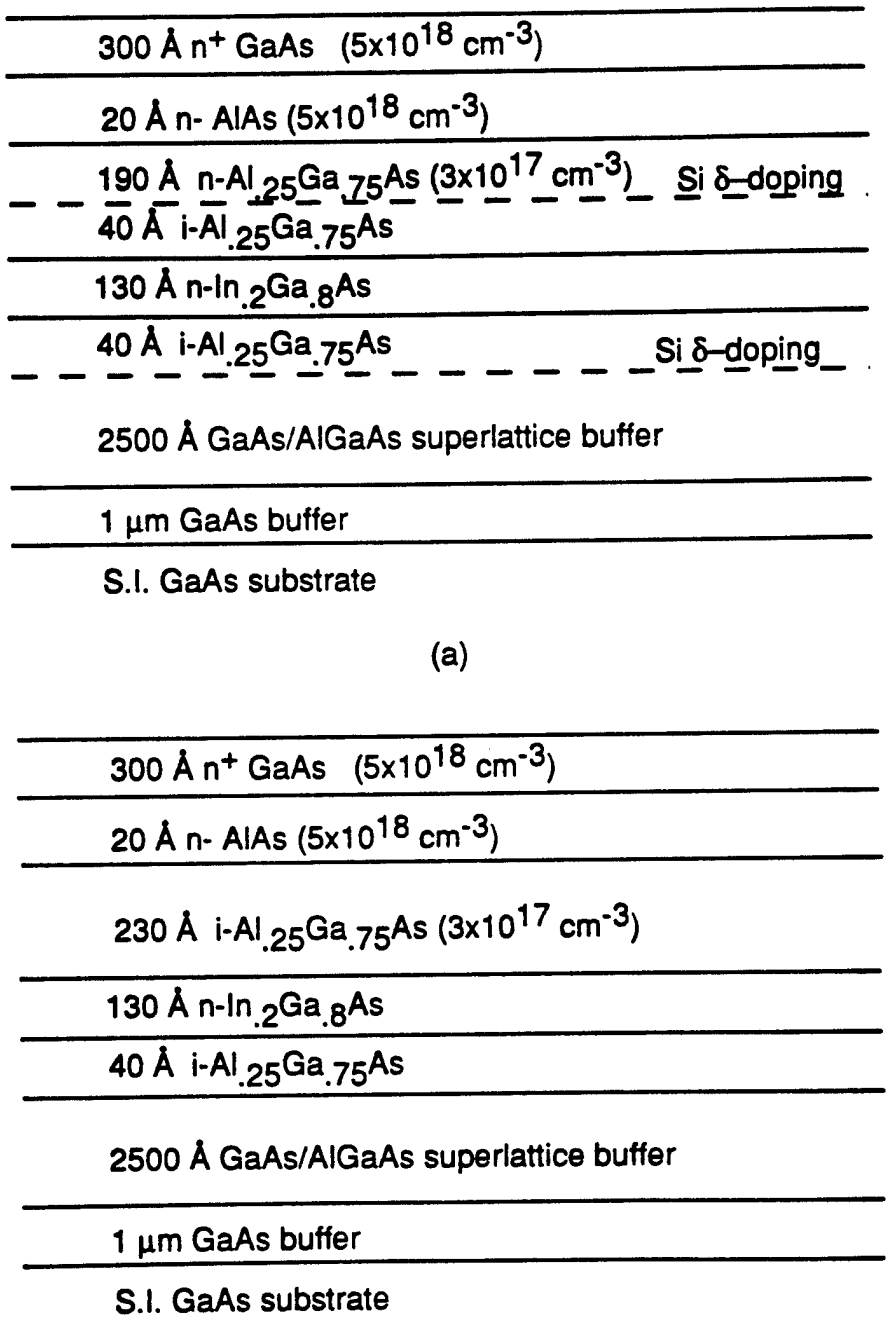

Figure 4.6. Schematic of the layer structures of the (a) PHEMT, and (b) DCFET used in the linearity study.

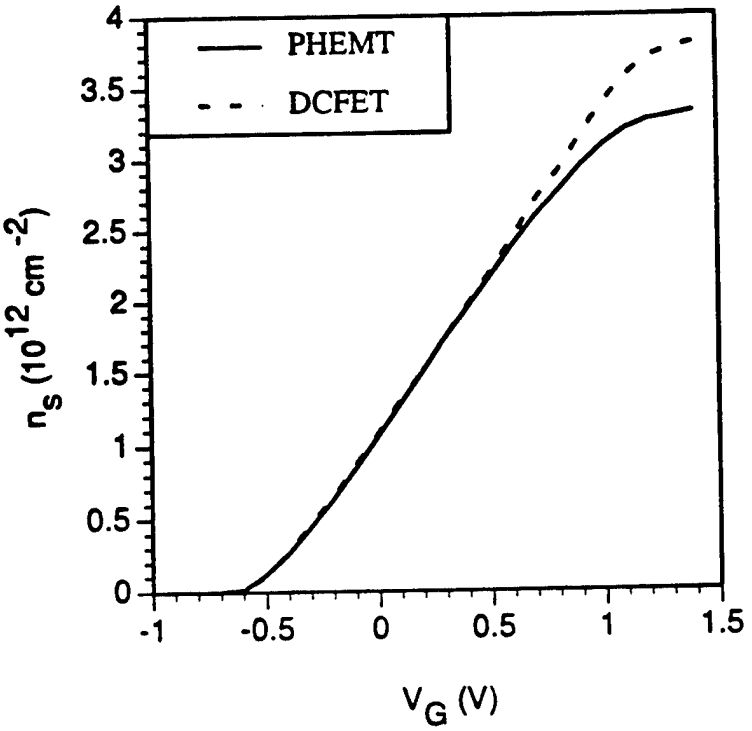

Figure 4.7. Simulated electron sheet charge density (n_S) as a function of gate bias (V_G) for the PHEMT and DCFET.

4.4 Experimental Comparison of DCFET and PHEMT

4.4.1 Layer structures and fabrication

The PHEMT and DCFET layer structures were grown by MBE and were shown in Figure 4.6. They were grown such that the carrier concentration in the channel, as measured by Hall with the cap removed, was the same for both layers. This ensured that the carrier concentration below the gate would be the same for both structures. The carrier concentration was 1.7 x 10^{12} cm^{-2}. The mobility was 1190 cm^2/Vs and 4650 cm^2/Vs for the DCFET and PHEMT, respectively. As can be seen in Figure 4.6, an etch-stop layer (AlAs) was present in both structures. The etch-stop layer was used during gate recess etching and ensured that the gate-to-channel distance was the

same for the PHEMT and DCFET, which is important because the distance plays an important role in charge modulation [4.14], [4.16].

The fabrication followed the procedure used for the PHEMTs described in Chapter 3, with a few modifications. The active area was patterned using positive optical photolithography, and wet chemical etching was used to define mesas. The width of the FETs was 100 μm, and the drain-to-source spacing was 2 μm (drain-to-source spacing was 3 μm for devices with gate lengths of 1 μm). The ohmic regions were defined using an image reversal optical lithography step coupled with metal evaporation (AuGe/Ni/Au) and liftoff. The ohmic contacts were alloyed in the RTA at 360 °C for 18s in a nitrogen/hydrogen forming gas and yielded a contact resistance of 0.1 Ωmm for both the PHEMT and DCFET. Overlay metal regions and T-gates of length 0.25, 0.3, 0.5, 0.7, and 1 μm were defined using electron beam lithography in a trilayer PMMA/P(MMA-MAA) resist. Ti/Au metal (220 Å/2480 Å) was evaporated as the gate and overlay metal.

4.4.2 Direct current characterization

Direct current measurements were made as described in Chapter 3. The measurements were made to compare the g_m, g_o, current drive, and breakdown voltage. The measurements discussed below are for devices whose gate length was 0.25 μm, unless otherwise stated.

The drain current (I_D) as a function of gate voltage (V_G) for the PHEMT and DCFET is shown in Figure 4.8. The first item to notice is that the threshold voltage (V_T), the voltage at which the two devices begin to conduct current, is the same. This resulted because the gate-to-channel distance, Schottky barrier height, and carrier concentration were the same for both layer structures. The second item to notice is that the saturated drain current is higher for the PHEMT than for the DCFET. This is a

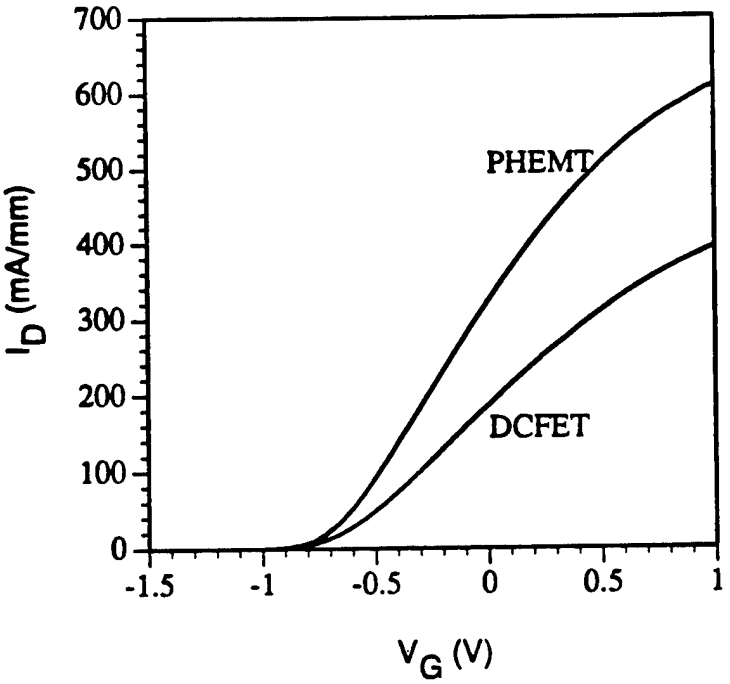

Figure 4.8. Drain current (I_D) versus gate voltage (V_G) for the PHEMT and DCFET.

result of the lower source and drain resistance of the PHEMT. The source resistance of the PHEMT was measured to be 5 Ω, and that of the DCFET was 10.5 Ω.

The g_m as a function of V_G at a V_D of 2.5 V for the PHEMT and DCFET is shown in Figure 4.9. The g_m is higher for the PHEMT than for the DCFET. The lower source resistance of the PHEMT is one cause of the higher g_m, as discussed in Chapter 3. Because a broad, flat peak is desired for good device linearity, the flatness of the peak was measured. This was done by determining the points at either side of the peak where the g_m fell to 90% of the peak value. The V_G range for which g_m is 90% of the peak value or greater was 0.61 V for the PHEMT and 0.66 V for the DCFET. This indicates only slightly better linearity characteristics in g_m versus V_G for the DCFET. The g_m as a function of I_D has also been used as a measure of linearity [4.1], [4.3]. The g_m versus I_D is shown in Figure 4.10 for devices biased at V_D = 2.5 V. The I_D range for

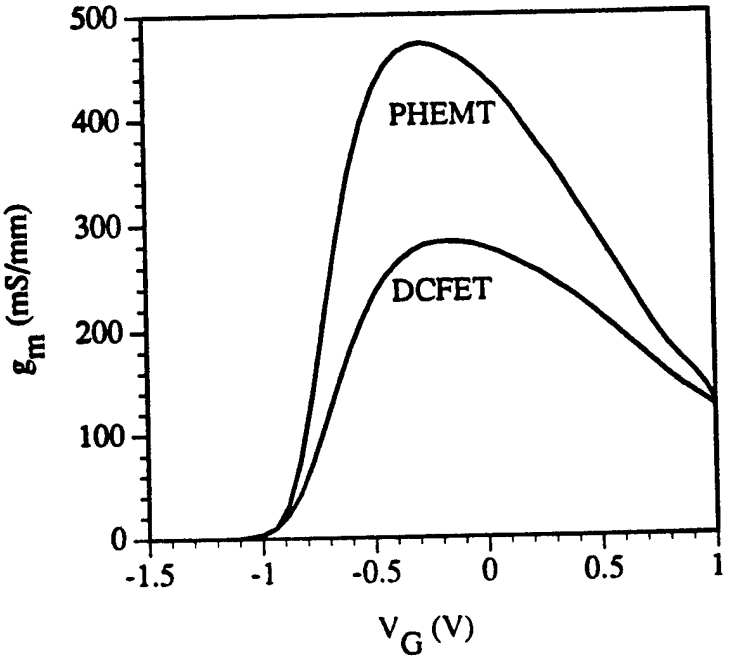

Figure 4.9. Transconductance (g_m) versus gate voltage (V_G) for the PHEMT and DCFET.

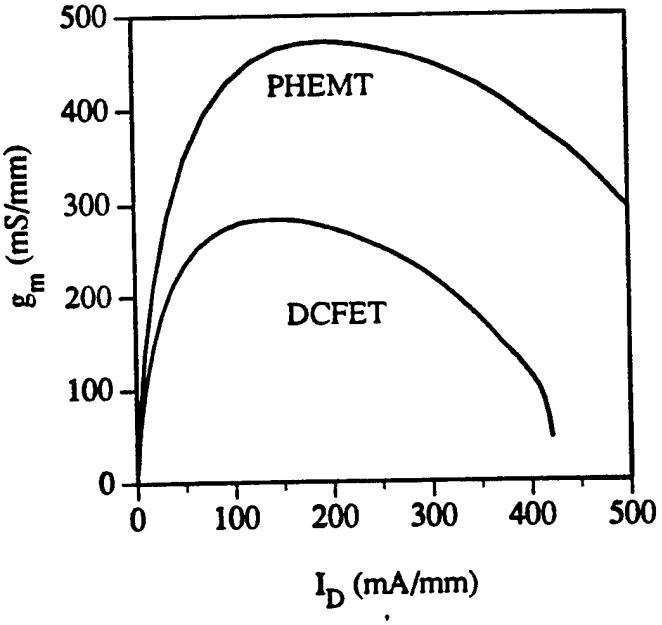

Figure 4.10. Transconductance (g_m) versus drain current (I_D) for the PHEMT and DCFET.

which g_m is 90% of the peak value or greater is 257 mA/mm for the PHEMT and 175 mA/mm for the DCFET. The carrier concentration and mobility are important parameters when considering the g_m versus I_D. Because the saturated drain current is higher for the PHEMT, the linear range of I_D versus V_G is higher, and therefore, the range over which g_m is constant as a function of I_D is larger. In [4.1] and [4.2], the comparison of g_m as a function of I_D was made between DCFETs and PHEMTs that had different n_s. In those comparisons, the DCFET had much higher saturated current, and therefore, g_m of the DCFET was found to be more linear with respect to I_D.

Figure 4.11 shows the I_D versus V_D for the PHEMT and DCFET. Both have relatively good output conductance characteristics. The output conductance for the PHEMT is 23.5 mS/mm and for the DCFET is 20.6 mS/mm. For both devices, the output conductance is constant with respect to V_D.

Figure 4.12 shows the off-state gate-drain breakdown voltage for the PHEMT and DCFET. The breakdown voltage is only slightly lower for the PHEMT. This is explained by the fact that the PHEMT has a doping plane in the AlGaAs Schottky layer which aids in tunneling between the gate and channel and, therefore, results in a slightly lower breakdown voltage [4.17].

4.4.3 Microwave characterization

Microwave measurements were made as described in Chapter 3. The measured f_T at a V_D of 4 V was 73 GHz and 50 GHz for the PHEMT and DCFET, respectively. The measured f_{max} at a V_D of 4 V was 129 GHz and 98 GHz for the PHEMT and DCFET, respectively. The f_{max} as a function of I_D at a V_D of 4 V is shown in Figure 4.13. The I_D span over which f_{max} has a value of 90% of the peak value or greater is 405 mA/mm and 263 mA/mm for the PHEMT and DCFET, respectively. The improved linearity of f_{max} versus I_D is a result of the higher current capability of the PHEMT as compared to the DCFET. The linearity of f_{max} versus V_G was comparable,

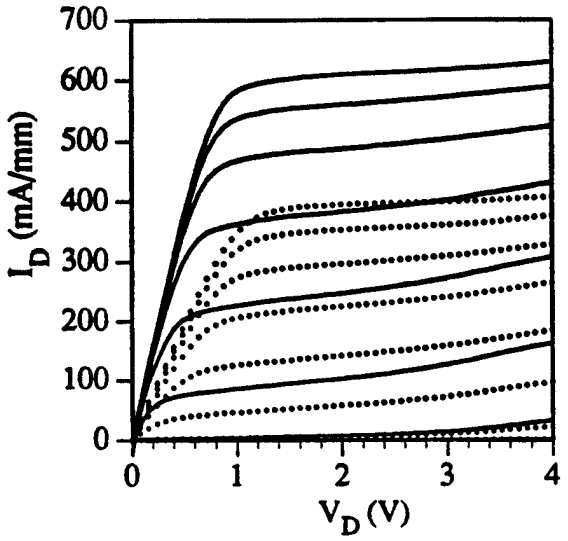

Figure 4.11. Drain current (I_D) versus drain voltage (V_D) for the PHEMT (solid lines) and DCFET (dotted lines). For both sets of curves, the gate voltage (V_G) is 1 V for the top trace and steps towards pinch-off in -0.3 V increments.

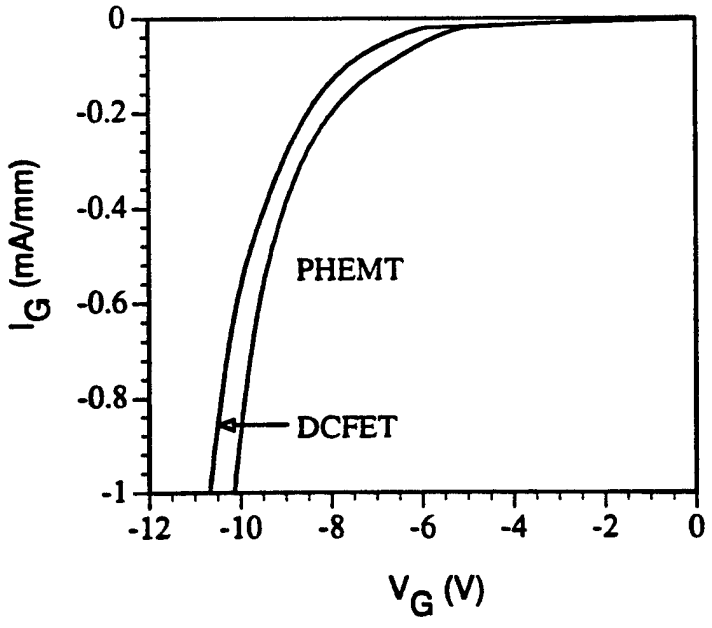

Figure 4.12. Reverse gate current (I_G) versus gate voltage (V_G) for the PHEMT and DCFET showing off-state breakdown at -1 mA/mm.

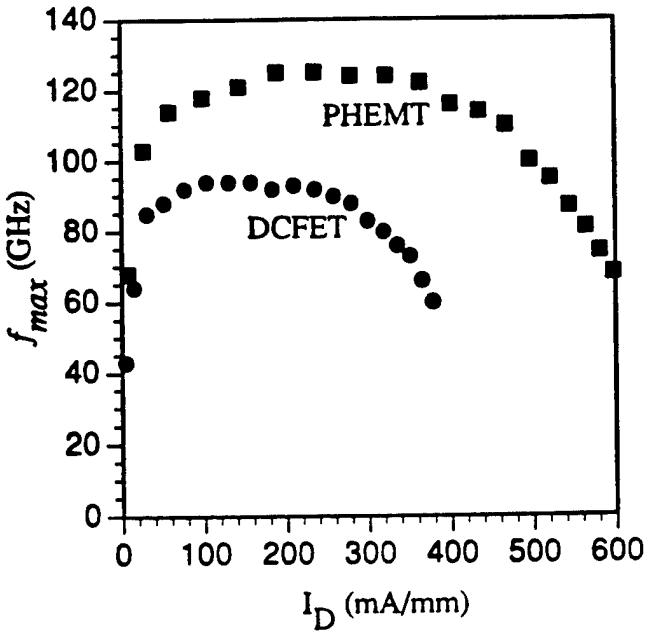

Figure 4.13. Maximum frequency of oscillation (f_{max}) versus drain current (I_D) for the PHEMT and DCFET.

with both PHEMTs and DCFETs having a V_G range of ~ 0.98 V for which f_{max} was 90% of the peak value or greater. The f_{max} versus V_G is shown in Figure 4.14.

4.4.4 Gate length dependencies

Finally, the device characteristics as a function of gate length L_g are shown in Table 4.1. It is seen that with increasing L_g the peak g_m decreases, but the range over which the g_m is flat (90% or greater than the peak) increases. The increase in R_s as the gate length is increased, or more specifically R_i, is the cause of the g_m dependencies on L_g which are observed [4.18]. The g_o improves and the rf performance is degraded with increasing L_g. When designing and fabricating circuits with specified frequency and power gain (linearity) performance requirements, it is

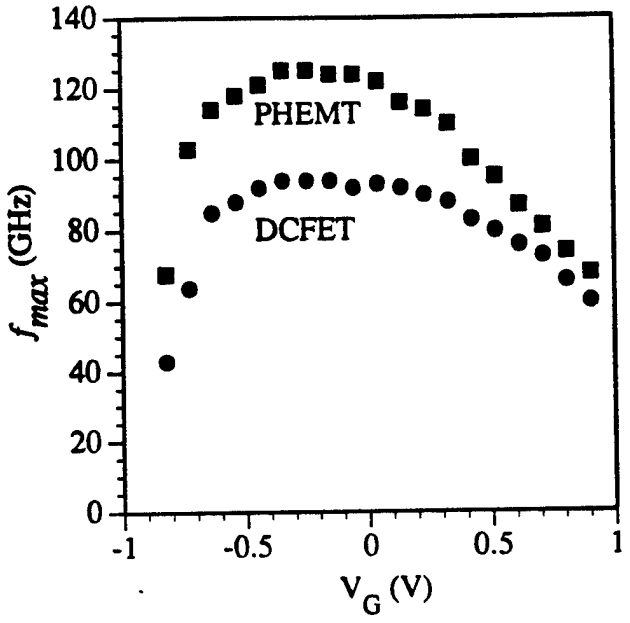

Figure 4.14. Maximum frequency of oscillation (f_{max}) versus gate voltage (V_G) for the PHEMT and DCFET.

necessary to consider the overall device performance. From a fabrication standpoint, one could have a PHEMT of longer L_g (easier to fabricate reproducibly and cost effectively) which is comparable in frequency and linearity performance to that of a DCFET with shorter gate length. The inherent properties of improved electron transport, lower R_S and R_D, and improved modulation properties (g_m), result in the performance improvement seen in the PHEMT. Therefore, the very slight improvement in dc g_m and g_o of the DCFET at a given gate length as compared to the PHEMT are offset by the inherent properties of the PHEMT, which allow comparable performance at longer L_g, with the rf performance being comparable.

Table 4.1. Device figures of merit as a function of gate length (L_g) for the PHEMT and DCFET.

Device parameter	L_g = 0.25 μm		L_g = 0.5 μm		L_g = 0.7 μm		L_g = 1 μm	
	PHEMT	DCFET	PHEMT	DCFET	PHEMT	DCFET	PHEMT	DCFET
g_o (mS/mm)	24.3	18.8	11.6	10.5	8.5	7.8	6.0	5.2
g_m (mS/mm) (maximum)	465	280	425	270	412	260	377	225
V_G range for g_m > or = 0.9 g_m maximum (V)	0.61	0.67	0.74	0.77	0.79	0.81	0.85	0.87
I_D range for g_m > or = 0.9 g_m maximum (mA/mm)	270	184	305	198	313	203	305	190
f_T (GHz)	73	50	40	32	33	21	20	13
f_{max} (GHz)	129	98	80	59	60	44	45	35

4.5 References

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CHAPTER 5

INDIUM PHOSPHIDE CHANNEL HEMTs

5.1 Introduction

Indium phosphide (InP), with inherent properties including high breakdown voltage [5.1], high electron saturation velocity [5.2], and high electron velocity at high electric fields [5.3], is an attractive material for use in high-power applications. For high-frequency, low-noise applications, $In_{0.53}Ga_{0.47}As$ has been used extensively as the channel material for InP-based HEMTs. Use of $In_{0.53}Ga_{0.47}As$ channel devices for high power has been limited, however, by the relatively low bandgap (0.75 eV) that leads to the inherent problems of impact ionization at relatively low fields and low breakdown voltage characteristics. Indium phosphide has a much higher bandgap (1.35 eV) than $In_{0.53}Ga_{0.47}As$, which implies that a given level of impact ionization will occur at a higher electric field than in $In_{0.53}Ga_{0.47}As$. The high thermal conductivity of InP is another property that makes it attractive for power applications. For comparison, Table 5.1 shows material properties of InP, $In_{0.53}Ga_{0.47}As$, and GaAs which are relevant for high-power considerations.

Both doped channel and modulation-doped HFETs with InP channels have been reported [5.4], [5.5], [5.6]. Perhaps the greatest obstacle in fabricating the devices is obtaining low-resistance ohmic contacts for the source and drain. As discussed in Chapters 2 and 3, low contact resistance leads to a low knee voltage, higher transconductance, and better power performance. A review of literature on the formation of alloyed ohmic contacts to n-type InP reveals that a portion of the InP is consumed (up to 60 nm) in the formation of the alloyed metal/semiconductor contact [5.7], [5.8], and [5.9]. The thickness of the n-InP channel has been varied to determine the effect on ohmic contact formation, and for InP-channel thicknesses of 6.5, 8, and 10 nm, the specific contact resistance was found to be 1, 0.57, and 0.21 Ωmm,

Table 5.1. Material properties for three different compound semiconductors at room temperature.

Property at 300 K	InP	GaAs	InGaAs
Energy bandgap (eV)	1.35	1.42	0.75
Γ-L valley energy separation (eV)	0.52	0.33	0.55
Thermal conductivity (W/(Kcm))	0.74	0.46	0.05
Peak electron velocity with donor density of 10^{17} cm^{-3} (10^7 cm/s)	2.5	1.7	2.6
Electron mobility with donor density of 10^{17} cm^{-3} (cm^2/(Vs))	3200	4000	7000
Electron effective mass to free mass ratio	0.079	0.066	0.043

respectively [5.5]. The results indicate that the ohmic contact resistance is indeed lower for a thicker n-InP layer. Formation of alloyed ohmic contacts to modulation-doped InP channels, however, has proven very difficult regardless of the channel thickness [5.5] and [5.10].

It would be desirable to take advantage of the superior transport properties of the modulation-doped InP channel, and also have the low contact resistance of the n-InP channel. A heterostructure that is modulation doped in the region between the source and drain contacts and n-type below the source and drain contacts is needed

to simultaneously achieve low-resistance alloyed contacts and superior transport properties. Alternatively, a method for achieving nonalloyed low-resistance contacts on a modulation-doped structure must be developed. The first part of this chapter discusses InP-channel HEMTs achieved through a method that uses ion implantation in the source and drain regions of a modulation-doped heterostructure to obtain low-resistance alloyed contacts. The second part of the chapter discusses the fabrication of InP-channel HEMTs using nonalloyed contacts.

5.2 Ion-Implanted InP HEMT

5.2.1 Concept

Implantation of Si in the source and drain regions of modulation-doped InP channel devices was studied in an attempt to achieve low-resistance alloyed contacts. The layer structure for the study is shown in Figure 5.1. From Hall measurements, it was found that the layer had a carrier concentration of $3x10^{12}$ cm $^{-2}$ and a mobility of 3000 cm/Vs at 300 K. The implanted Si, when properly activated, would provide an n-InP channel region below the source and drain ohmic contacts. The necessary dose and energy of the Si implant was determined from simulations using *Flash* by *Silvaco*. It was found that a dose of $2x10^{13}$ cm^2 at an energy of 60 KeV would be appropriate and result in a donor density of $2x10^{18}$ cm^{-3} when activated [5.11]. The peak of the Si implant distribution was found to be at a depth of 40 nm with a standard deviation of 20 nm. High temperature annealing is required to activate the implanted Si and to reduce the crystal damage caused by the implantation [5.12]. However, high temperature annealing can also cause outdiffusion of atoms as well as heterointerface degradation including intermixing and barrier lowering [5.13], [5.14]. The first step was to determine the maximum annealing temperature that could be used without destroying the heterointerface properties. The second step was to study the formation of alloyed ohmic contacts to the implanted, annealed InP heterostructure. The final

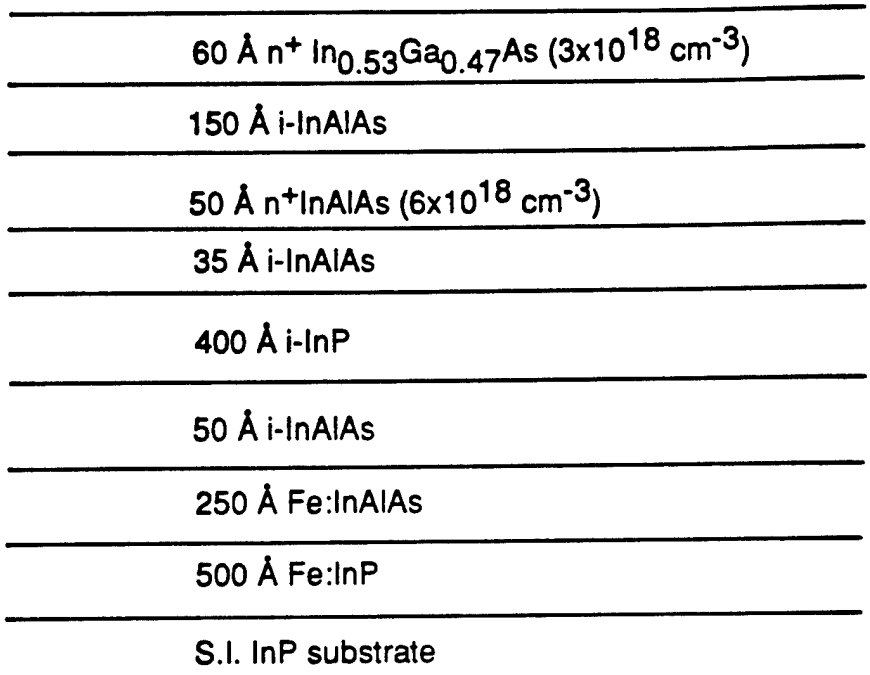

Figure 5.1. Schematic of the InP-channel heterostructure used for the ion-implanted HEMT.

step was the fabrication and testing of devices that used the ion-implanted source and drain contacts.

5.2.2 Annealing temperature study

Rapid thermal annealing was studied to determine which temperature could be used to activate the Si ions without destroying the integrity of the heterostructure layers. The annealing was performed in an Addax RX rapid thermal process chamber in a nitrogen ambient with the InP-channel wafer sandwiched between two

InP/$In_{0.53}Ga_{0.47}As$ wafers. The sandwich gave the effect of an As or P overpressure and hindered the outgassing of As or P from the InP channel wafer [5.15]. The temperature was varied from 600 °C to 800 °C in steps of 50 °C, and the time of the anneal was 7 s. The dependence of carrier concentration and mobility measured at 300 K and 77 K as a function of annealing temperature is shown in Figures 5.2 and 5.3, respectively. From Figure 5.2, it is seen that the carrier concentration measured by Hall at 300 K and 77 K drops dramatically for anneal temperatures of 750 °C and 800 °C. From Figure 5.3, it is seen that the mobility measured at 300 K drops substantially for an anneal temperature of 800 °C, and the mobility measured at 77 K drops noticeably at anneal temperatures of 700 °C and above.

The degradation in carrier concentration is more substantial at 300 K than at 77 K for a given anneal temperature, as seen in Figure 5.2. The degradation in mobility, however, is more pronounced at 77 K than at 300 K for a given anneal temperature, as seen in Figure 5.3. The likely explanation is as follows. The high temperature annealing causes the intermixing of atoms and reduction of the heterointerface potential barrier between the channel and barrier layers. Electrons in the channel have more thermal energy at 300 K than at 77 K. Therefore, at 300 K, proportionally fewer electrons reside in the channel, because they have enough thermal energy to surmount the potential barrier between the channel and barrier layers. At 77 K, the electrons that reside in the channel have less thermal energy, and therefore, the degradation in 2-DEG concentration is less pronounced than at 300 K. At 300 K, the dominant mechanism that limits electron mobility is phonon scattering, whereas at 77 K, the dominant mechanism that limits the mobility is electron interaction with ions and other scattering centers [5.16]. If the heterointerface is indeed degraded with increased annealing temperature, there would be an increased number of potential variations along the interface. This roughening of the interface would lead to more pronounced mobility degradation for the electrons at 77 K. Another factor that

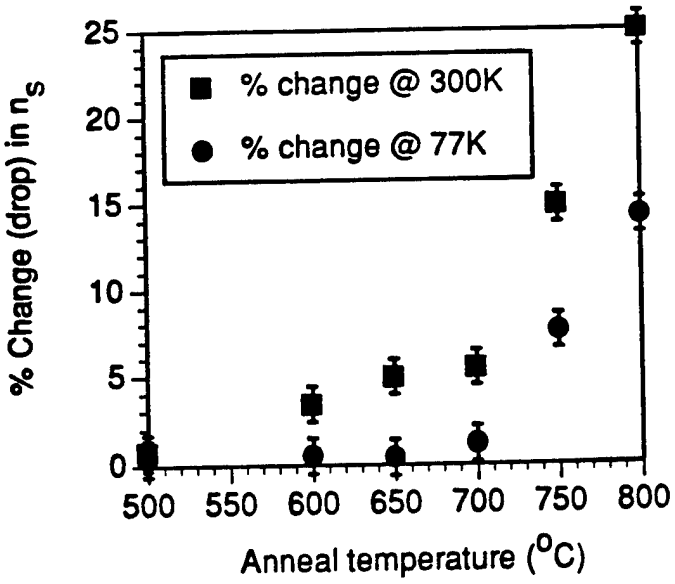

Figure 5.2. Variation of carrier concentration (n_s) as a function of anneal temperature. The carrier concentration was measured at both 77 K and 300 K using Hall measurements.

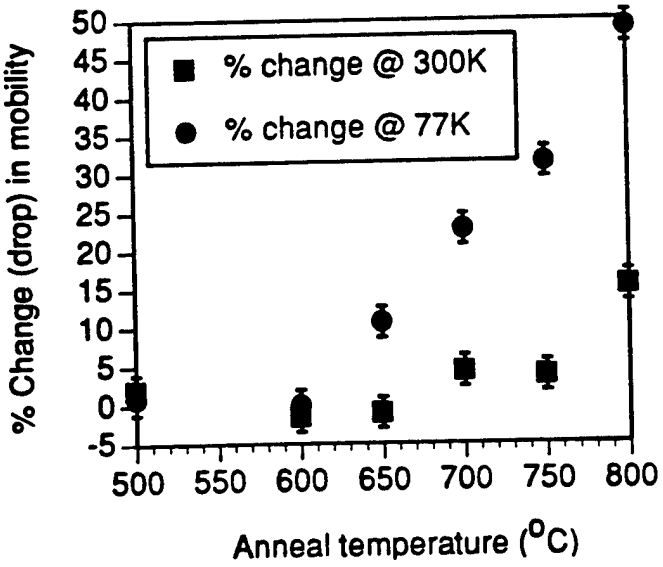

Figure 5.3. Variation of mobility as a function of anneal temperature. The mobility was measured at both 77 K and 300 K by Hall measurements.

may be leading to the more pronounced mobility degradation at 77 K, as compared to 300 K, is that the Si ions from the delta-doping plane may be diffusing towards the interface and leading to increased electron-ion interaction.

Samples that were annealed at various temperatures were analyzed by secondary ion mass spectroscopy (SIMS) [5.17] to determine whether there was indeed a migration of Si ions and other atoms including In, P, Al, and Ga. The results are shown in Figures 5.4-5.7. The SIMS profiles in Figures 5.4 and 5.5 were made by detecting positive secondary ions. This mode of detection gave the best depth resolution, but did not detect Si. Comparing Figure 5.4, the unannealed sample, to Figure 5.5, the sample that was annealed at 800 °C, the only noticeable difference is the phosphorus (P) concentration in the 0.0 to 0.04 μm range. The 800 °C sample shows higher P-concentration at the surface and lower P-concentration at 0.03 μm when compared to the unannealed sample. This may be indicative of P outdiffusion. The SIMS profiles in Figures 5.6 and 5.7 were made by detecting negative secondary ions. This allowed Si to be resolved from Al and H interference, but compromised depth resolution. Comparing Figure 5.6, the unannealed sample, to Figure 5.7, the sample that was annealed at 800 °C, it is noticed that the location of the peak Si concentration is the same at approximately 0.025 μm. The annealed sample, however, shows a broader Si peak. This could indicate Si diffusion. Unfortunately, the depth resolution of the SIMS profiles is on the order of 0.01 μm, which is on the same order of the length scales of interest, and therefore, the SIMS profiles only provide evidence of possible migration of P and Si.

In order to determine the quality of the two-dimensional electron gas (2-DEG) as a function of annealing temperature, Schubnikov de Haas (SDH) measurements were performed. The measurements were performed in a Janis cryostat using ac-lockin amplifier measurement techniques. The instrument control and data collection was controlled by an HP work station (capone). The SDH characteristics measured at

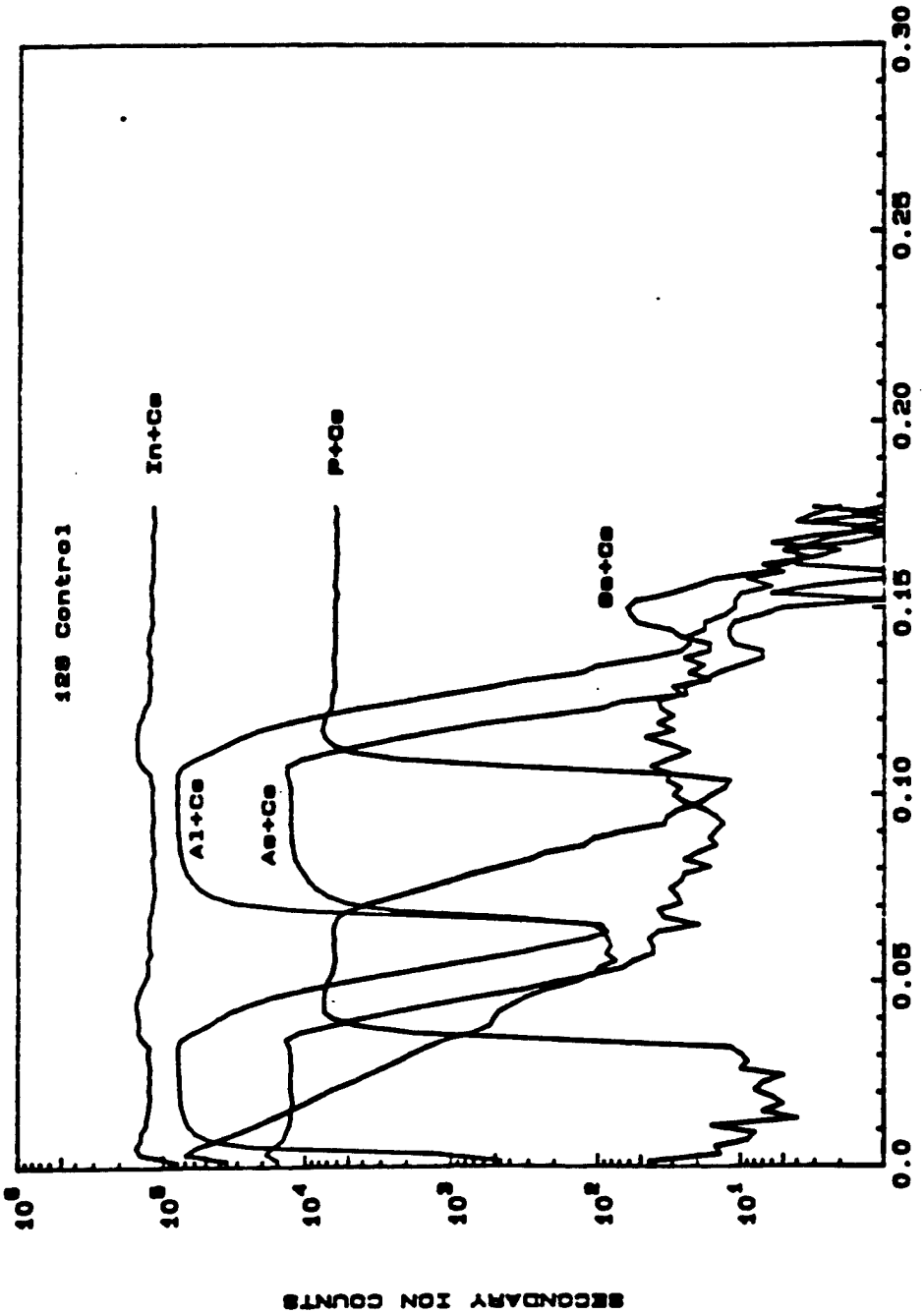

Figure 5.4. SIMS profile of the InP heterostructure that was not annealed. The profile was made by detecting positive secondary ions.

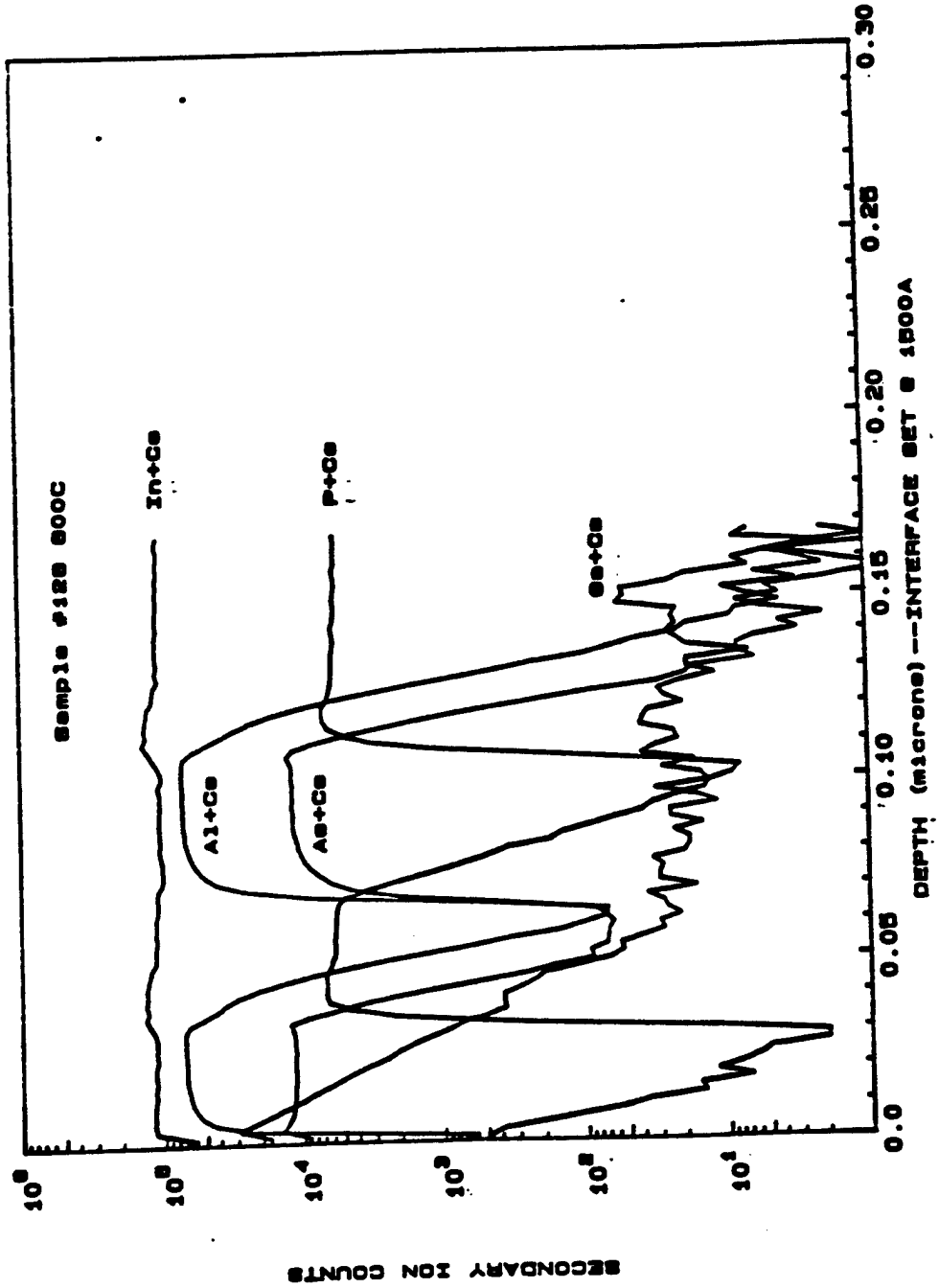

Figure 5.5. SIMS profile of the InP heterostructure that was annealed at 800 ^{o}C for 7 s. The profile was made by detecting positive secondary ions.

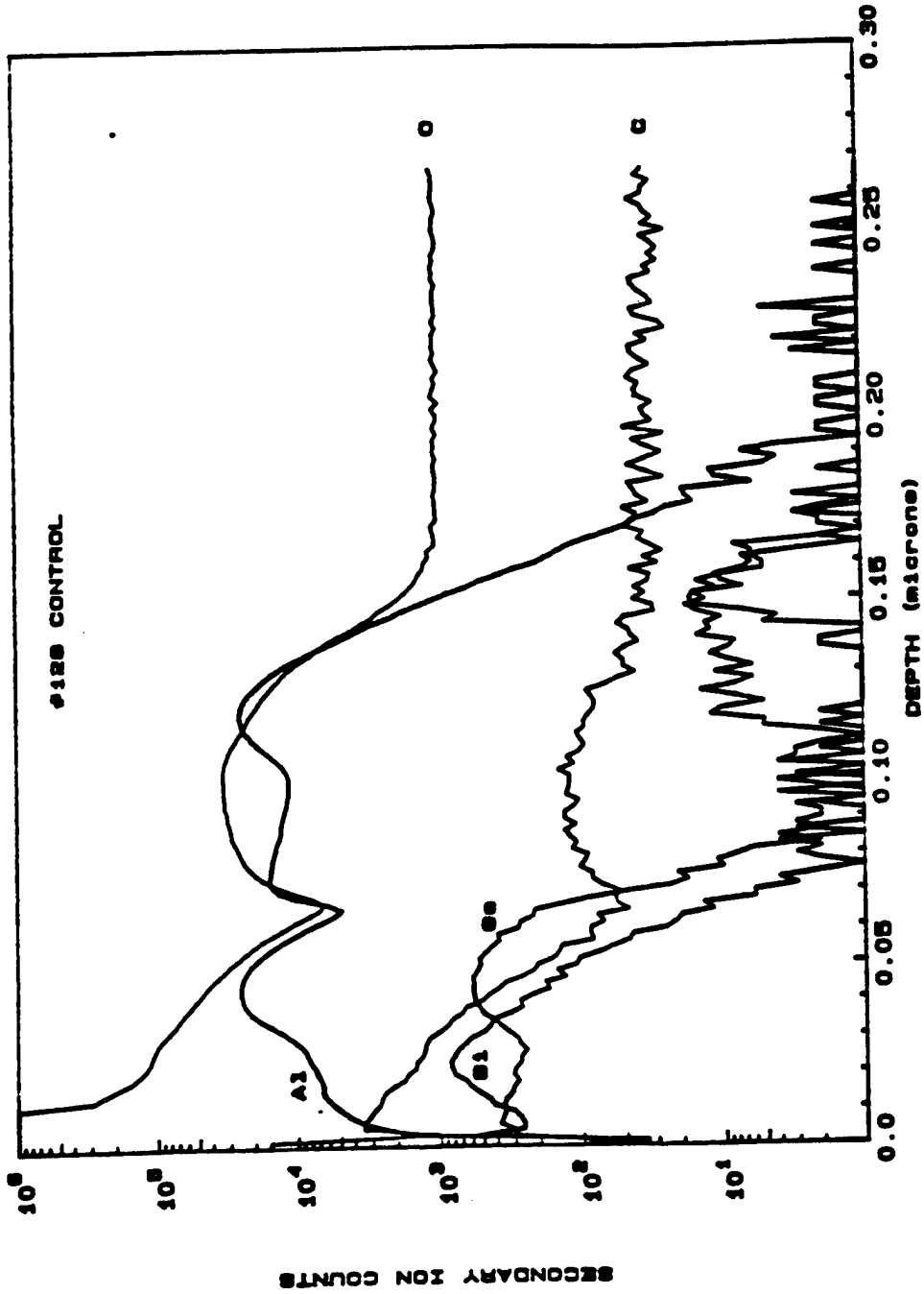

Figure 5.6. SIMS profile of the InP heterostructure that was not annealed. The profile was made by detecting positive secondary ions.

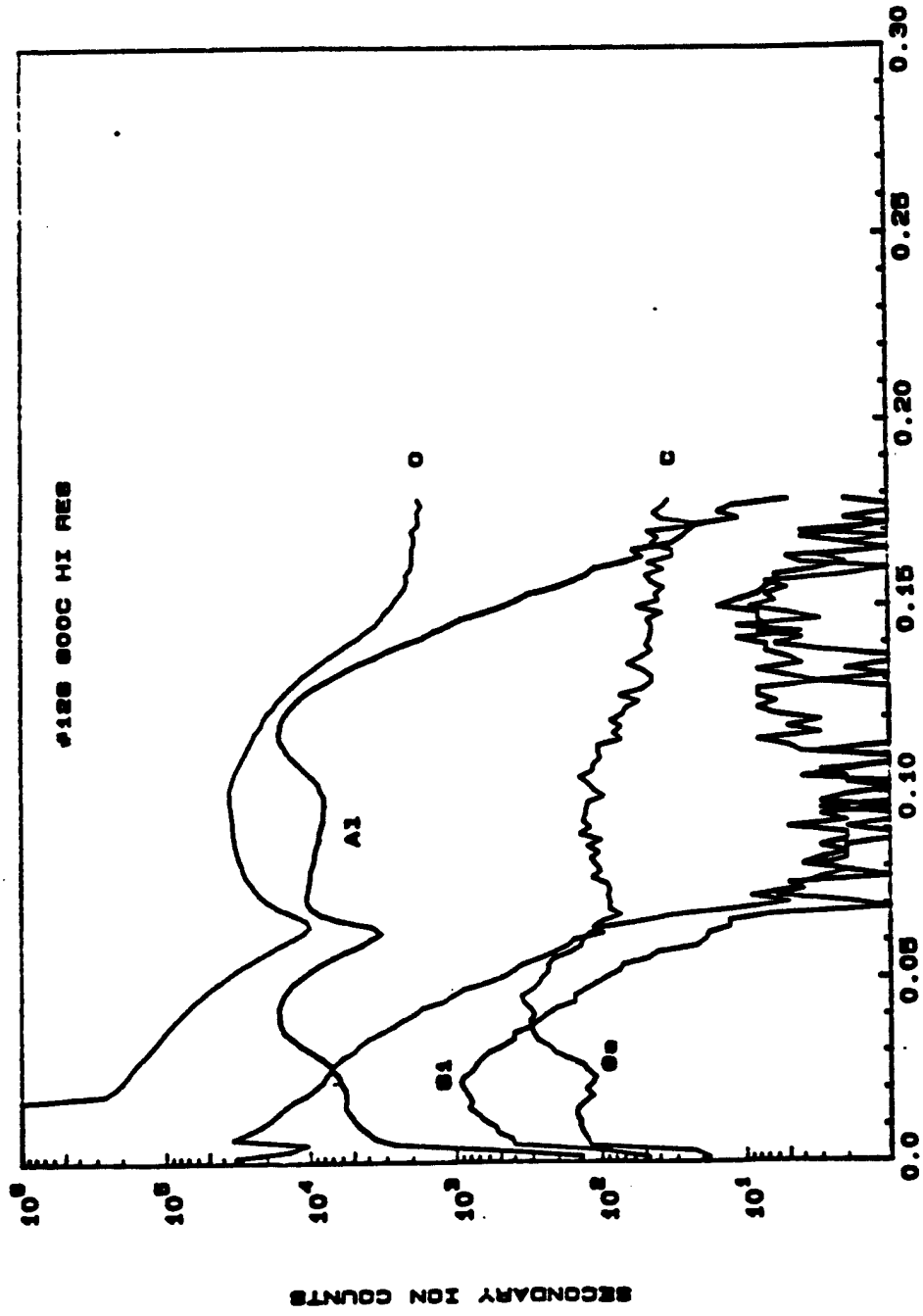

Figure 5.7. SIMS profile of the InP heterostructure that was annealed at 800 ^{o}C for 7 s. The profile was made by detecting negative secondary ions.

1.8 K are shown in Figures 5.8 and 5.9 for an unannealed and 800 °C annealed heterostructure, respectively. The multiple oscillations in the longitudinal resistance ρ_{xx}, as a function of magnetic field in Figure 5.8, indicate the presence of a high-quality 2-DEG [5.18]. The lack of oscillations in Figure 5.9 indicates the absence of the 2-DEG. The SDH characteristics for samples measured at temperatures of 600 °C to 750 °C displayed similar features as in Figure 5.8, indicating that the 2-DEG was maintained. The loss of the 2-DEG at an anneal temperature of 800 °C supports the conclusions from the mobility and carrier concentration studies. If there was substantial heterointerface barrier lowering and intermixing, then the potential well was lost, and with it, the 2-DEG. From the combined results of the mobility, carrier concentration, and SDH characteristics as a function of annealing temperature, it was determined that the maximum temperature that could be used for annealing without severe degradation of 2-DEG properties was between 700 °C and 750 °C.

5.2.3 Ohmic contact formation

A TLM (transmission line model) structure that was discussed in Chapter 3 was used to study the ohmic contact formation of the Si-implanted heterostructure as a function of annealing temperature. Before implantation, a suitable masking structure was deposited and patterned on the wafer. A combination of PECVD-deposited Si_3N_4 (silicon nitride) and photoresist was used. First, 200 Å of Si_3N_4 was deposited at a temperature of 250 °C. Afterwards, photoresist was spun on the Si_3N_4 covered wafer, and the TLM structure was patterned using optical lithography. The photoresist was 1.3 µm thick and served as the mask for the ion implantation [5.19]. The Si_3N_4 provided a convenient means for clean removal of the photoresist mask after the implantation. The complete removal of the photoresist after implantation could prove difficult if the Si_3N_4 were not used, because the photoresist can become hot during the

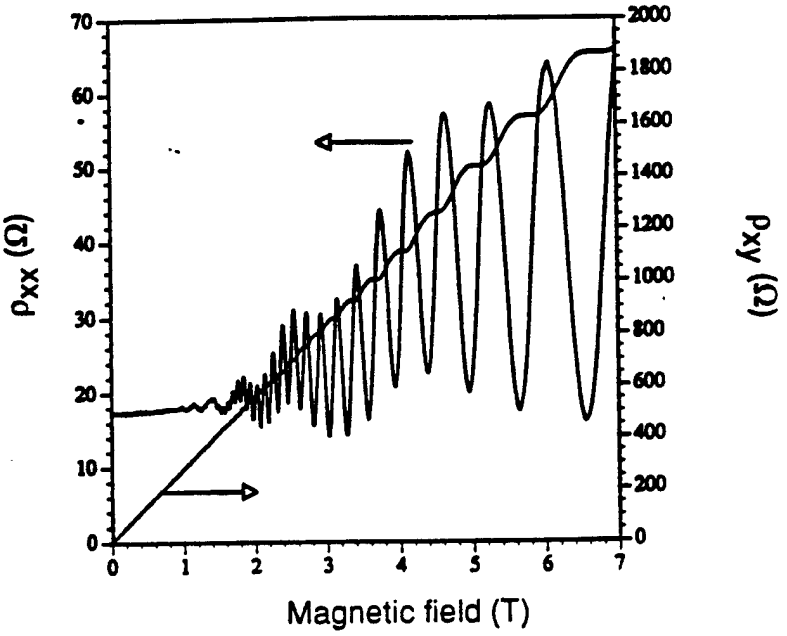

Figure 5.8. Shubnikov de Haas characteristics measured at 1.8 K for the unannealed InP channel heterostructure.

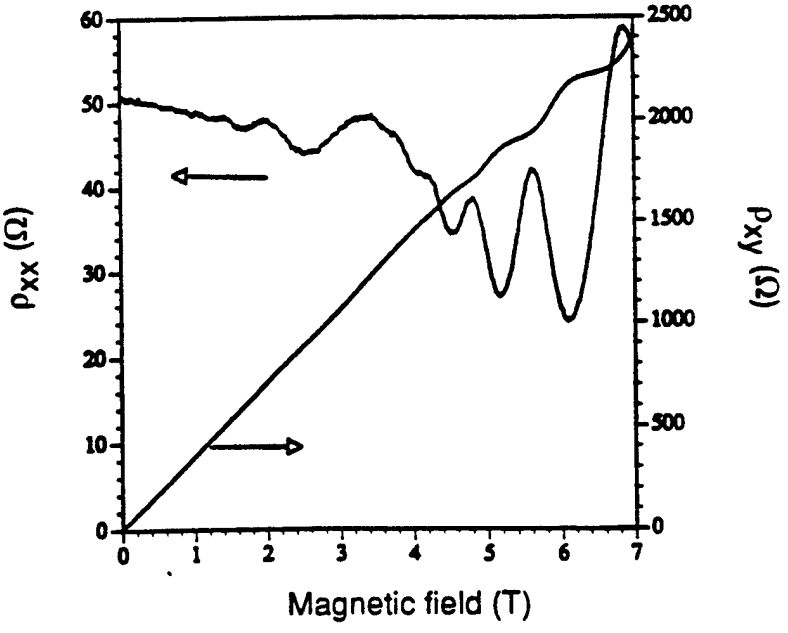

Figure 5.9. Shubnikov de Haas characteristics measured at 1.8 K for the 800 ^{o}C annealed InP channel heterostructure.

implant and, therefore, become very difficult to remove afterward [5.20]. The Si_3N_4 is cleanly removed from the wafer after implantation, and with it, the photoresist.

The wafer with the TLM-patterned mask was implanted with Si using the conditions given above, and afterwards, the Si_3N_4/photoresist mask was removed using buffered oxide etch (hydrofluoric acid-based solution). The wafer was then annealed in the RTA at various temperatures of 600 °C to 750 °C (as determined previously). After the annealing, the metal layers for alloyed ohmic contacts were evaporated in the TLM pattern. Three different metallization schemes were studied including AuGe/Ni:1370 Å/350 Å, AuGe/Ni/Au:650 Å/120 Å/650 Å, and Ni/Ge/Au: 250 Å/500 Å/400 Å. The contacts were alloyed in a nitrogen ambient furnace at temperatures varying from 350 °C to 500 °C and times varying from 20 to 180 s. Table 5.2 lists the best ohmic contact resistance values for the three metallization schemes. The best ohmic contact was achieved using the AuGe/Ni metal structure for a 60 s alloy at 480 °C on the sample that had been annealed at a temperature of 700 °C. The contact resistance was measured to be 0.18 Ωmm. For samples that were annealed below 700 °C, no alloy conditions were found that resulted in low contact resistance.

Table 5.2. Ohmic contact resistances and alloying conditions for three different metallization schemes on a 700 °C annealed Si-implanted InP-channel heterostructure.

Metallization	Metal thicknesses (Å)	Alloy temp. (°C)	Alloy time (s)	Contact resistance (Ωmm)
AuGe:Ni	1370:350	480	60	0.18
AuGe:Ni:Au	650:120:650	450	25	0.37
Ni:Ge:Au	250:500:400	480	45	0.29

5.2.4 Device performance

The final step in the study was the fabrication of transistors using the implantation method. The combined Si_3N_4/photoresist mask was patterned on the wafer and defined the source and drain regions of the FETs to be implanted. After implantation and mask removal, the processing was very similar to that described for the PHEMTs in Chapter 3. Photolithography and wet etching were used to pattern the mesa regions and provide device isolation. Photolithography and metal evaporation were used to define the source and drain contacts. After the ohmic metal was deposited, the contacts were alloyed, and the contact resistance was found to be 0.22 Ωmm. The final step in the device fabrication was the patterning of the gates, which was achieved through electron beam lithography, gate recess etch, and metal evaporation.

Devices with gate lengths of 0.25 μm that were fabricated using this method showed promising characteristics, including a saturated drain current ($I_{D,sat}$) of 300 mA/mm when biased at V_D=2 V and V_G=0.3 V, transconductance of 250 mS/mm at V_D=2 V, on-state source-drain breakdown voltage of 16 V when biased at V_G such that I_D=0.5$I_{D,sat}$, and an f_T of 52 GHz. Figure 5.10 shows the drain current (I_D) vs. drain voltage (V_D) at various gate biases (V_G) for a 0.25 μm gate length device. The off-state gate-drain breakdown voltage (defined at 1 mA/mm of gate current) was limited to -5 V. The drain current at pinchoff ($I_{pinchoff}$) was quite high and limited the off-state drain-source breakdown voltage (defined at 1 mA/mm of drain current) to 3.5 V. The relatively poor off-state breakdown performance and high output conductance are probably due to the heterointerface potential barrier lowering between the channel and barrier layers which occurs during the high temperature anneal. The ion-implanted FETs demonstrate the feasibility of using InP as a channel material for high-power applications, but the disadvantage of the technique is that it

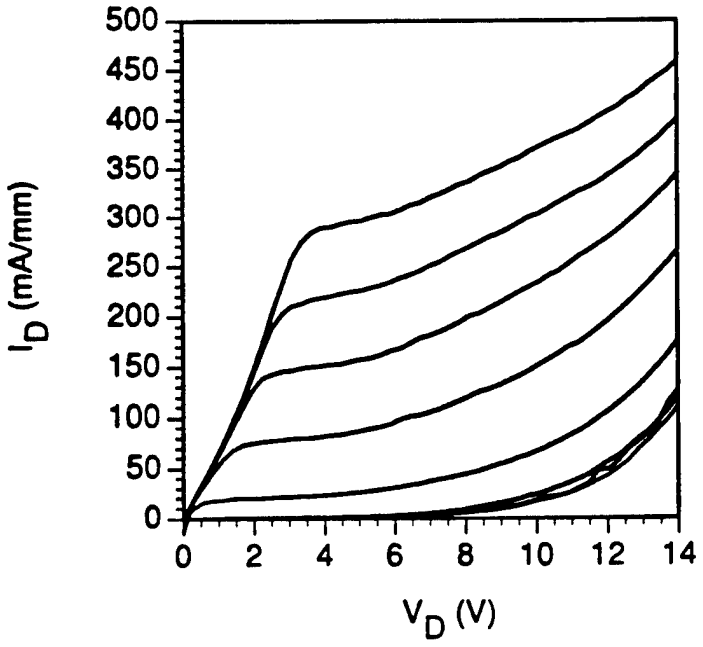

Figure 5.10. Drain current (I_D) versus drain voltage (V_D) for the InP-channel HEMT with annealed Si-implanted ohmic regions. The top curve is for V_G of 0.3 V and successive curves step toward pinch-off in -0.4 V increments.

requires several additional processing steps to achieve low-resistance alloyed ohmic contacts to the InP channel.

5.3 Indium Phosphide HEMT with Nonalloyed Contacts

5.3.1 Concept

Recent publications have advocated the use of nonalloyed contacts in the fabrication of $In_{0.53}Ga_{0.47}As$ channel HEMTs [5.21], [5.22]. The heterostructure used for the nonalloyed contacts coupled a highly doped InGaAs/$In_{0.52}Al_{0.48}As$ cap with an undoped $In_{0.52}Al_{0.48}As$ Schottky layer, and Ti/Pt/Au was used as the nonalloyed source and drain metal contacts. The heterobarrier between the InAlAs and InGaAs

layers in the cap is lowered, and the tunnel current at the barrier is increased by doping Si into the InAlAs underneath the InGaAs. Contact resistance was found to be less than 0.1 Ωmm [5.21]. Two heterostructures were designed to determine the possibility of using nonalloyed contacts with modulation-doped InP channel devices. The layer structures are schematically shown in Figure 5.11. Hall measurements on the layers showed a carrier concentration of $2x10^{12}$ cm^{-2} with a mobility of 2700 cm^2/Vs for the double delta-doped structure, and a carrier concentration of $2.3x10^{12}$ cm^{-2} with a mobility of 5000 cm^2/Vs for the single delta-doped structure at 300 K.

5.3.2 Ohmic contact formation

TLM patterns were used to determine the ohmic contact resistance to the InP heterostructures. The ohmic contact resistance for several different metallization schemes is shown in Table 5.3. Results are given for both nonalloyed and alloyed metals. The gated measurements were made by etching off the cap between the TLM metal pads. By removing the cap, it is ensured that the measured contact resistance is between the metal contact pad and the InP channel, as opposed to the contact resistance between the metal contact pad and the highly doped cap [5.18]. It is clear that the best ohmic contact is achieved for the nonalloyed Ti/Au. The Ti/Au metallization was used in the fabrication of devices.

5.3.3 Device performance

Devices were fabricated using the processing techniques that have been previously described. The processing included mesa etching and ohmic metal definition using optical lithography, and gate definition using electron beam lithography. The devices fabricated on the layer structure with one delta-doping plane showed better characteristics than devices fabricated on the layer that had two

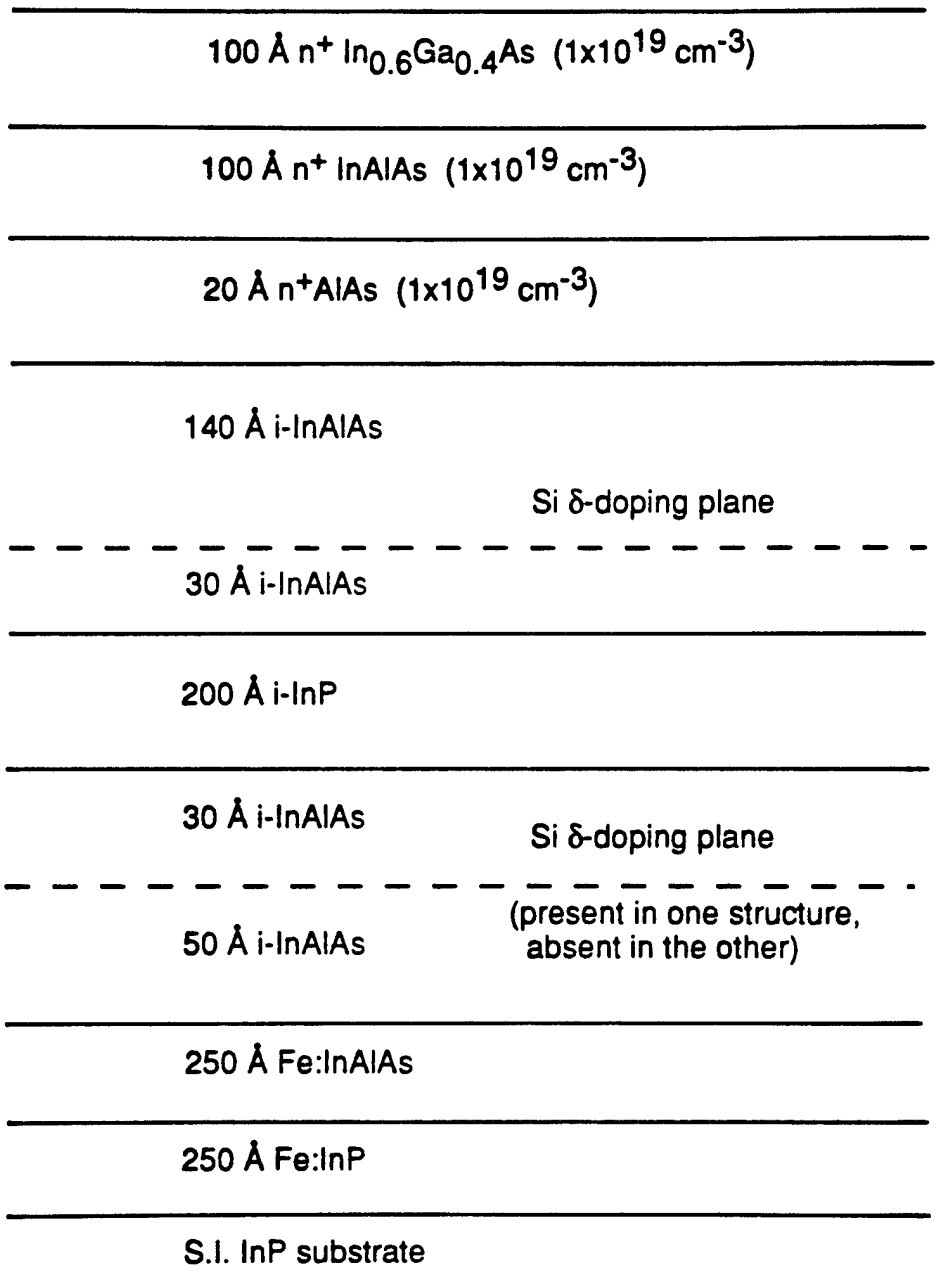

Figure 5.11. Schematic of the InP-channel modulation-doped heterostructure designed for nonalloyed ohmic contacts.

Table 5.3. Ohmic contact resistance (Ωmm) for three metallization schemes on the InP heterostructure.

Metallization	TLM conditions			
	As deposited	Gated	Annealed	Annealed & Gated
Ti/Au	0.1	0.12	----	----
Pd/Ge/Au	0.15	0.3	0.2	0.9
AuGe/Ni/Au	0.1	0.18	0.15	0.4

delta-doping planes (see Figure 5.11). The results that are discussed below are those of the devices that were fabricated on the layer having only one delta-doping plane.

The drain current (I_D) as a function of drain bias (V_D) for varying gate bias (V_G) of a 0.25 μm gate length device is shown in Figure 5.12. The knee voltage of the top trace in Figure 5.12 is approximately 1.2 V, which is lower than the knee voltage (~ 3 V) of the InP channel FET, which was fabricated using ion-implanted source and drain contacts shown in Figure 5.10. The lower knee voltage is largely due to the lower ohmic contact resistance, which was measured to be 0.1 Ωmm. The FET had a saturated drain current ($I_{D,sat}$) of 460 mA/mm when biased at V_D=2 V and V_G=0.3 V, and a transconductance of 285 mS/mm at V_D=2 V. The output conductance of the FET was also better than the FET with ion-implanted source and drain contacts (compare Figures 5.10 and 5.12). The off-state gate-drain breakdown voltage (defined at 1 mA/mm of gate current) was limited to -1.5 V. The drain current at pinch-off ($I_{pinchoff}$) was high and limited the off-state drain-source breakdown voltage (defined at 1 mA/mm of drain current) to 0.9 V. The poor off-state breakdown performance is a

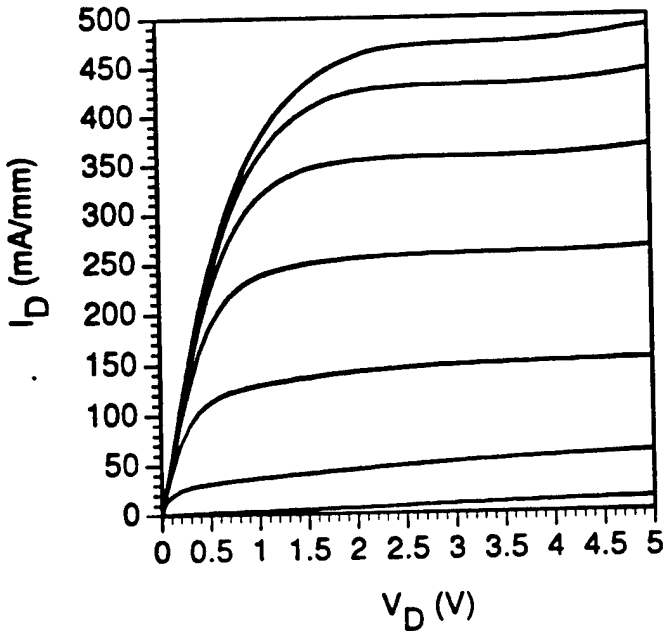

Figure 5.12. Drain current (I_D) vs drain voltage (V_D) for the InP-channel HEMT with nonalloyed ohmic source and drain contacts. The top curve is for V_G of 0.3 V and successive curves step toward pinch-off in -0.4 V increments.

result of a poor buffer layer. Because the source, drain, and gate pads rest on the buffer layer, it is crucial that the buffer be highly insulating to prevent current from passing between pads through the buffer layer. The pad-to-pad leakage current between adjacent devices was found to be 1 to 3 mA at a bias of 1 V, providing evidence that the buffer was 'leaky'. The 'leaky' characteristics of the buffer are a result of the incorporation of unwanted impurities in the buffer layer during growth. The devices did show, however, that it is possible to achieve low-resistance nonalloyed contacts to a modulation-doped InP channel structure by using the n^+ InGaAs/n^+ InAlAs cap structure.

5.4 Synopsis

The feasibility of using InP as the channel material for high-power HEMTs was investigated and demonstrated. The greatest obstacle in the fabrication of InP channel HEMTs, the realization of low-resistance ohmic contacts, was overcome through two techniques: (1) the use of Si-implanted source and drain regions, and (2) the use of an n^+ InGaAs/n^+ InAlAs cap. The use of Si-implanted source and drain regions resulted in an alloyed ohmic contact resistance of 0.18 Ωmm, and the use of an n^+ InGaAs/n^+ InAlAs cap resulted in a nonalloyed ohmic contact resistance of 0.1 Ωmm. Devices fabricated using both techniques showed promising characteristics necessary for high-power applications.

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CHAPTER 6
SUMMARY AND FUTURE RESEARCH

A number of the crucial features required of compound semiconductor transistors for use in high-power microwave applications have been presented. Design requirements, fabrication issues, and device characterization have been discussed in some detail, but many challenges remain. As a prelude for the future challenges, the conclusions that may be drawn from this work will be summarized, and a few suggestions for future research will be made.

Chapter 3 presented the asymmetrically double-recessed gate PHEMT, which has been developed to improve breakdown voltage, while keeping surface effects to a minimum and maintaining low source resistance and high modulation efficiency [6.1]. The development of the four-layer resist technique allowed for a comprehensive study of the effects of drain-side cap recess width, L_{ud}, on the dc and rf performance of PHEMTs. The study was possible because the four-layer resist process allowed L_{ud} to be varied from 0.17 to 0.55 μm while keeping the gate length fixed at 0.2 μm. The four-layer resist provided a 'self-aligned gate metal/recess' process and provided both a liftoff profile for T-gate metallization and an etching mask for sequential wet and dry selective etching, which define the wide and narrow recess trench. Both positive and negative effects of asymmetric recess on the performance of the PHEMTs were observed. The positive effects included an off-state source-drain breakdown voltage improvement of 5.2 to 12.5 V, an improvement in dc voltage gain from 16 to 73, a reduction in gate-drain capacitance of 14.2 to 5.4 fF, and an improvement in f_{max} from 135 to 158 GHz, as L_{ud} was increased from 0 to 0.55 μm. The negative effects of asymmetric recess included a reduction of saturated current from 880 to 826 mA/mm, a decrease of dc transconductance from 476 to 404 mS/mm, and a slight decrease in f_T from 95 to 92 GHz, as L_{ud} was increased from 0 to 0.55 μm.

There are several areas of the four-layer resist process that would be interesting to investigate further. It would be advantageous to achieve the double recess through sequential dry and wet recessing, as opposed to wet and dry recessing. This would reduce the potentially negative effects of damage caused by the bombardment of the gate region by the ions that are present in the RIE etching [6.2]. The lattice damage caused by the ion bombardment could be partially or completely removed by following the dry etch with the wet etch. The feasibility of following the dry etch with the wet etch was briefly investigated, but proved to be unreliable. This is thought to be due to electrochemical effects. Issues that could be investigated include the use of surfactants, photons, or different selective etches to obtain reliable dry/wet etching. If a dry/wet chemistry were developed, pulsed I-V measurements could be used to study the role that surface states play on the performance of the wet/dry and dry/wet recessed devices. Reliability tests and damage studies could also be made to compare the wet/dry and dry/wet recessed devices.

The issue of device linearity for high-power applications was presented in Chapter 4. The dc and rf characteristics of identically designed PHEMTs and DCFETs were compared to study the effect of dopant placement on linearity. It was shown that the PHEMT had substantially better linearity of transconductance and f_{max} as a function of drain current, the DCFET had slightly better transconductance as a function of gate bias, and the devices had comparable f_{max} linearity as a function of gate bias. The study of linearity as a function of gate length provided evidence that the PHEMT could provide superior linearity performance at a given frequency of interest due largely to the inherently superior electron transport properties when compared to the DCFET.

Further work should be carried out to clarify, in detail, the effects of doping density, carrier mobility, and extrinsic device properties (R_S) on the linearity of delta-doped PHEMT and DCFET device characteristics. Also, it would be useful to

investigate the importance of the placement of the doping plane of the PHEMT on linearity [6.3]. Several measurements could be made to qualify the large signal linearity of the devices. The possible measurements include two-tone intermodulation measurements (IMD), adjacent channel power ratio (ACPR), and noise power ratio (NPR) [6.4]. The IMD measurement is a good general purpose measurement of large signal linearity. The ACPR measurement has recently become very popular for quantifying the linearity of devices with applications to digital (cellular) telecommunications. The NPR is useful in qualifying systems that are to handle many frequencies or channels. Depending on the application, one or more of the above tests should be carried out.

Chapter 5 investigated the feasibility of using InP as a channel material for high-power microwave applications. It was found that achieving alloyed ohmic contacts to an undoped InP heterostructure through conventional layer design and alloying techniques was very challenging. Low-resistance alloyed contacts were achieved by implanting the source and drain regions of the device, thereby providing n-InP. The resulting devices showed good on-state drain-source breakdown, but poor output conductance and off-state breakdown due to the heterointerface barrier lowering, which was caused by the high temperature annealing used to activate the implanted ions. A method of achieving low-resistance nonalloyed contacts was achieved by adopting a novel cap design, which has been used for InGaAs channel devices [6.5].

The growing need in both military and commercial areas for GaAs- and InP-based transistors that operate at frequencies in excess of 1 GHz is sure to continue driving research in this area. The research will answer some of the many remaining questions involving the design, fabrication, and characterization of transistors that are used for high-frequency power applications.

6.1 References

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VITA

Ronald W. Grundbacher was born in Richmond, Virginia, on December 25, 1968. In August 1987, after graduating from Dunlap High School in Dunlap, Illinois, Mr. Grundbacher entered the Department of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. In the summer of 1989, he participated in a study-abroad program in Paderborn, Germany, which involved both coursework at the Universität-Gesemthochschule Paderborn and an internship at PESAG A.G., the utility company of northwestern Germany. In the summer of 1990, he participated in an internship program at the Microelectronics Laboratory at the University of Illinois, where he was involved with work on III-V semiconductor lasers. Mr. Grundbacher received the Bachelor of Science degree in Electrical and Computer Engineering with a minor in Germanic Studies in May, 1991. He graduated with highest honors as a Bronze Tablet scholar at the University of Illinois.

In the fall of 1991, Mr. Grundbacher joined Professor I. Adesida's Advanced Processing and Circuits research group in the Department of Electrical and Computer Engineering at the University of Illinois. Mr. Grundbacher received the Master of Science degree in August, 1993. The master's thesis work concentrated on the fabrication and characterization of quantum structures in AlGaAs/GaAs heterostructures. Mr. Grundbacher continued working in Professor Adesida's research group in pursuit of the Ph. D. degree. In the fall of 1994, Mr. Grundbacher received a three year Joint Services Electronics Program Fellowship for doctoral study. The main area of concentration for the Ph. D. research is in the design, fabrication, and characterization of III-V semiconductor-based transistors for high-power microwave applications.