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13. ABSTRACT *(Maximum 200 words)*

Identified a candidate algorithm suitable for imaging through trubulence. The phase diversity algorithm demonstrate good performance mapped the phase diversity algorithms onto an opto-electronic (OE) architecture. Developed in-house flip-chip bonding capability for MQW modulators on Silicon. Demonstrated a functional 4x4 array of MQW modulators designed, fabricated and characterized a dual focal lenght lens implemented with the two-substrate Birefingent Computer Generated Hologram (BCGH) technology. To simplify the design and fabrication of BCGH components, initiated the investigation of single-substrate BCGH using two approaches, a multiple-order delay (MOD) approach and Form Birefingent Computer Generated Holograms (FBCGH) approach a compact functional package of optically interconnected OE VLSI built of a polarization selective BCGH integrated into a standard PGA package was demonstrated.

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2. Objectives/Statement of work

A. Study fixed and adaptive filters and associated algorithms and their mapping onto the 3-D computer (collaborative effort between Hughes, ERIM, and UCSD).

B. Enhance the present state of the art of the optically interconnected 3-D computer by implementing the optoelectronic interface using MQW modulators.

C. Enhance the present state of the art of the optically interconnected 3-D computer by implementing the Optical Transpose Interconnection System (OTIS) system using birefringent computer generated holograms (BCGH).

3. Status of effort

A. We have identified jointly with the Hughes team a candidate algorithm suitable for imaging through turbulence. The identified phase diversity algorithm, developed by the ERIM team, demonstrate good performance for imaging through atmospheric-like turbulence. We have mapped the phase diversity algorithms of ERIM onto an opto-electronic (OE) architecture. To enable such mapping we have performed an in-depth OE FFT analysis.

B. We have developed in-house flip-chip bonding capability for MQW modulators on Silicon. Initially, we have demonstrated a functional 4x4 array of MQW modulators designed and fabricated at UCSD. The Au based flip-chip bonding process that we use, has the advantage that is cheap and reliable since it does not require extensive metallization steps prior to bonding and is, therefore, ideally suited for fast system prototyping. Furthermore, we have demonstrated in house 16x16 array operation and we also have designed and fabricated through the DARPA Coop an optoelectronic chip for implementing the OTIS system.

C. For packaging the optical interconnects of the OTIS system, we have designed, fabricated and characterized a dual focal length lens implemented with the two-substrate Birefringent Computer Generated Hologram (BCGH) technology. To even further simplify the design and fabrication of BCGH components, we initiated the investigation of single-substrate BCGH using two alternative approaches, a multiple-order delay (MOD) approach useful for heterogeneous OE systems integrations and Form Birefringent Computer Generated Holograms (FBCGH) approach suitable for monolithic integration of OE systems. For FBCGH approach, we successfully designed and fabricated a 500 nm deep microstructure of period 200 nm in a GaAs substrate. Such artificial anisotropic layers were used later to design, fabricate and test a FBCGH element useful for monolithic packaging applications. Furthermore, we extended our research on such polarization selective elements into design, fabrication and testing of double resonance structures. For heterogeneous packaging optoelectronic systems, we have designed, fabricated and characterized polarization selective computer generated holograms using MOD approach employing a single birefringent substrate of YVO_4 crystals. We have also completed the MOD design and fabrication of a polarization selective diffractive optical element that implements the OTIS optical interconnection architecture. The designed and fabricated BCGH implementing the OTIS optical interconnection architecture has been characterized and interfaced with the optoelectronic chip. Finally, a first compact functional package of optically interconnected OE VLSI built of a polarization selective BCGH integrated into a standard PGA package was demonstrated jointly with Bell Laboratories, Lucent Technologies.

4. Accomplishments/New Findings

A. Algorithm Mapping

The work on algorithm mapping has focused primarily on the phase-diverse-speckle approach developed by the ERIM team. This method is used for image restoration by finding the most likely image from the observed data. Early discussions with ERIM revealed that the algorithm would be difficult to apply to real-time problems because many iterations are required in order to find the most likely image.

Our research work addressed the following issues:

(i) Image Acquisition: Estimates suggest that, while not as time-consuming as the image reconstruction, image acquisition will take a noticeable amount of time using standard CCDs; time which might be saved by a better design of this subsystem. Also, it is possible that adding features to support preprocessing during data acquisition (oversampling followed by filtering) may assist in the reconstruction.

(ii) Hardware design: At present, we have estimated how many chips of different types (FFT, DSP) will be needed for real-time operation. Our next step focused on the communication between these chips and their memory requirements to ensure that sufficient bandwidth is available.

(iii) Algorithm: Once a detailed description of the operations necessary for the remaining portions (search direction computation and deconvolution) of the algorithm is available, these will need to be mapped onto the hardware. Also, it is possible that further study of the algorithm will lead to faster performance by making use of FFT symmetries, determining precisely how much precision is necessary in the computation, etc.

Further discussions with ERIM team led to algorithm modifications to meet real time operation requirements resulting in the following hardware system (see Fig. 1):

(i) Image acquisition: The phase-diverse-speckle image sets will be acquired by CCD cameras. A central 64x64 sub-image from each is being selected for determining the parameters of the turbulence.

(ii) Image reconstruction: This set of sub-images is reconstructed using the newly optimized phase-diverse-speckle algorithm. Since most of the image sets processing can be done independently, each image will be processed by separate, parallel hardware units. To perform the necessary calculations, both dedicated FFT and general-purpose DSP chips are required. Some additional sequential processing (e.g., calculating a new search direction for the optimization part of the algorithm) also needs to be addressed.

(iii) Deconvolution: The determined turbulence parameters are applied to the detected input image for restoration.

Even with the algorithmic improvements, it is difficult to envision a system which would be capable of achieving real-time reconstruction of images using current commercially-available technology. Projections have been made regarding next-generation DSP and FFT chips, and a more detailed outline of the system design has been performed. In particular, the time needed to perform the computationally-intensive reconstruction step was analyzed in detail. Using 1 FFT chip and 4 DSPs to perform the computations on each image, we estimate that most of the calculations needed to reconstruct the sub-image can be performed in approximately 25 msec, suggesting that video or near-video frame rates may be achievable. This analysis does not include the time necessary to compute the search direction, which is still under investigation.

We also investigated Auslander algorithm. Auslander's algorithm is based on distributed matrix transpose, however we did not find how it can benefit our approach. It's useful to him because his data sets are larger than the main memory, such that by organizing data correctly,

one can reduce the amount of paging to (very slow) disks. However, we do not need such memory hierarchy; DRAM is a slow memory for us, which is 6X slower than the processor rather than the 1,000,000X slower for disks. In particular, in our case, we are always looking at images of less than 256x256x8 bytes/pixel = 0.5 Mbyte, or about the size of the cache (faster SRAM memory) that most PCs have.

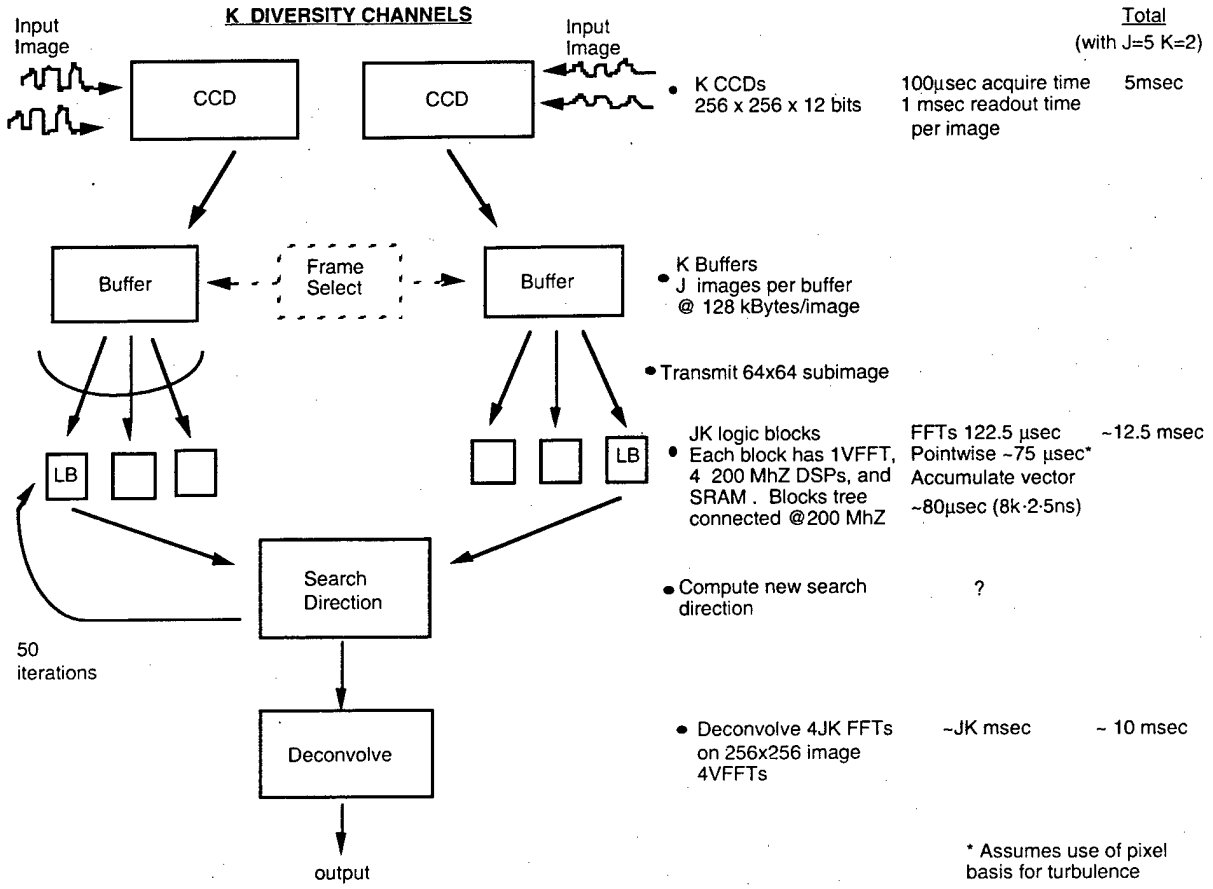

Fig. 1. Schematic diagram of the image restoration system

FFTs for sparse arrays: This issue is important for convolutions with masks that are only non-zero on small circular regions corresponding to the aperture. We had a naive solution, which was based on skipping computations of FFTs of all-zero regions. For example, every column which is all zeros does not need to be transformed. However, rows which were all zero before, might not be all zero after the FFTs along the columns, such that FFT need to be applied to every row, and thereby does not lead to any computation savings. If the aperture were an N/2xN/2 square, brute force FFT would take order of 2NlogN oprerations, the small improvement mentioned above would reduce it only to 1.5NlogN, and the best possible would be NlogN. It is possible that a more sophisticated FFT algorithm making use of circular symmetries would offer some improvement, but the returns seem relatively small. Also, this simple algorithm maps nicely onto dedicated FFT hardware (it just requires doing different sets of smaller FFTs), which most likely will not be true for more complex algorithms.

A comprehensive study of OTIS-based FFT systems has been also performed. OE solutions have been compared to existing and future electronic FFT systems. The study shows that OE solutions will bring at least a factor of 10 improvement in terms of power, volume, and speed over the state of the art technology.

Additional details on this part of the research can be found in the Hughes as well as ERIM Technical Reports.

B. MQW Modulators

An optimization study has been performed for the asymmetric Fabry-Perot (ASFP) multiple quantum well (MQW) absorption modulator. MQW material parameters of importance are the residual absorption (α_o) and the electroabsorption ($\Delta\alpha$). Cavity parameters are the front and back mirror reflectivities, Rf and Rb, and the cavity thickness Lc. Contrast ratio and insertion loss are two properties of the modulator to be optimized together. For a given back mirror reflectivity, both contrast ratio and insertion loss are functions of front-mirror reflectivity and residual absorption. The electroabsorption coefficient, $\Delta\alpha=\alpha_H-\alpha_o$, has an effect on contrast ratio only.

The asymmetric Fabry-Perot cavity is used to improve the contrast ratio over that of a two-pass modulator. The peak contrast ratio in an ASFP modulator is also associated with high insertion loss. Thus there is a trade-off between contrast ratio and insertion loss in ASFP modulator design. The optimum conditions depend heavily on the modulator material properties.

Reflective two pass modulators were used in the preliminary flip-chip bonding study. The material structure is as follows: n-GaAs substrate; a two step InAlGaAs n-doped buffer for dislocation filtering and strain relaxation; 50 pairs of InAlGaAs/InGaAs MQWs, and a p-type cap layer. The modulators are in a p-i-n diode configuration. The backside of the wafer is chemically polished and AR coated with SiO_2. The operating wavelength is near 1.06 μm. Since the GaAs substrate is transparent at this wavelength, the modulators can be fabricated on the front side, flip-chip bonded to silicon driving and logic circuitry, and then optically addressed through the back surface of the wafer.

Initially, 4x4 arrays (pitch of 500 μm) of reflective modulators have been bonded to test substrates. The test substrates consist of thermally evaporated aluminum patterned in a corresponding 4x4 array. There are nine pads for the ground connection. The Al was annealed to the glass surface at 400°C to prevent liftoff. Gold balls of approx. 100 μm diameter. were placed on the test substrate pads with a thermocompression ball bonder. The bonder was adjusted to leave no Au wire tail.

After the gold balls were placed, the MQW array was flip-chip bonded to the test substrate. During the bonding process, the temperature was ramped quickly to 300 °C, then contact was made and pressure was applied by hand. After the bond was complete, the temperature was lowered as rapidly as possible to room temperature. A transparent epoxy was applied between the GaAs and the test substrate (through capillary action) for added mechanical stability.

The flip-chip bonded array was placed in a simple one to one optical system shown in Fig. 2.

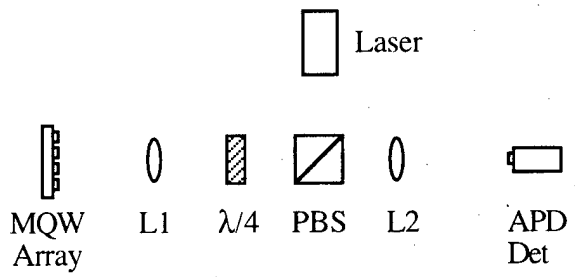

Fig. 2. Single link optical system for characterization and testing the MQW modulator arrays

The laser used in the experiment is a diode pumped Nd:YLF laser (λ=1.047 μm). Not shown on this picture is an imaging system used for alignment. A silicon APD was used to detect the modulated signal.

Alignment of the MQW modulator to the input beam is a several step process. First a small mirror is placed in the position of the modulators. An identical ceramic carrier is used to hold the mirror so that it is at approximately the same position as the MQWs. The pitch, yaw, and z position of the stage which holds the mirror (and MQWs) is adjusted through auto-collimation. Once these adjustments are made, the mirror is removed and the MQW modulator array is placed back in the system. The imaging system is placed into the system in front of the APD detector and the input beam is aligned to a single diode in the array. The imaging system is then removed. The modulated signal is detected on the APD and final small adjustments are made to optimize the signal.

A Tektronix DAS 9100 was used to drive the modulator, supplying a 256 bit long pseudo random bit sequence at 25 Mb/s. The voltage applied to the modulators was 14.5V at an optical input intensity of 500 μW. Under these conditions an eye-diagram was recorded. From the eye diagram, a bit error rate was extracted. The difference in the means divided by the sum of the standard deviations, or

$$BER = Q\left(\frac{m1 - m2}{\sigma 1 + \sigma 2}\right)$$

and a plot of BER as a function of Q was used to estimate the BER. From the recorded eye diagrams, a BER of less than 10^{-15} was estimated.

The large voltage swing required for the particular material used in this study posed a problem. Since a tunable laser at the necessary wavelength was not available, the optimum wavelength for the modulator material was not used. Because of this, a large applied bias was required to shift the exciton peak to the laser wavelength. The large bias also limited the speed at which the measurements were made. The DAS 9100, which can supply the required voltage swing, runs at a maximum of 25 Mb/s.

Another major problem encountered is the difficulty in reproducing materials obtained from the MBE system. Unexpected variations in growth rate and composition make the modulator material growth somewhat unpredictable. The percentage of time that the MBE is up and running is also a problem. Long delays occur while the machine is down undergoing maintenance.

The flip-chip bonding process is not optimized, and this may have caused problems. We encountered open connections as well as shorts on a particular flip-chip bonded array used in the experiments. It has not yet been determined if these are bonding problems or MQW material problems.

The same MQW material structure used for modulation can also be used for detection. The properties of these MQW detectors are studied and a system integrating both modulators and detectors on the same substrate, possibly even the same device, is being investigated. This technology greatly expands the utility of the systems in which the flip-chip bonded devices can be used. Because of the problems encountered with the reliability of the test devices, some study should be performed into thermal and mechanical stresses and long term operation.

During the second part of the program, we investigated the hybrid integration of III-V based optical devices, such as modulators, LEDs, and lasers, with silicon VLSI technology. Such approach is a promising cost effective solution to many optoelectronic challenges. It combines the low cost, high density, and high yield of silicon circuitry with the unique optical properties of III-V devices. Flip-chip bonding is a mature and commercial technology. It provides a means of reliable, rapid integration of these two types of devices. We report the

results of a technological investigation of the integration of AlGaAs/GaAs and InAlGaAs/InGaAs multiple quantum well (MQW) modulators with silicon CMOS circuitry using flip-chip bonding. A 16x16 array of multiple quantum well (MQW) modulators and Si driver circuitry has been designed and fabricated. The devices are flip-chip bonded using gold balls as the bump technology. The gold ball technology is reliable and widely available. It can be readily used for hybrid integration on Si circuitry without any alteration of or addition to existing silicon IC fabrication processes. We have investigated the epitaxial lift off (ELO) and total substrate removal (TSR) of AlGaAs/GaAs MQWs onto quartz substrates in the context of flip-chip bonding. Issues regarding the processing of modulator devices both before and after the thin film procedure have been examined. The InAlGaAs/InGaAs modulators, which operate near 1.06μm, are flip-chip bonded directly to silicon drivers as the GaAs substrate is transparent at this wavelength.

Various bump technologies were evaluated, with strong emphasis on rapid development and ease of prototyping. Many bump technologies require complex metallurgy and/or processing on the silicon and III-V circuitry. For instance, in order to use indium bumps on foundry fabricated silicon circuitry, additional metallization layers must be deposited on the silicon IC for use as a solder wetting surface. However, reflowable flip-chip bumps such as indium have the advantage of self-alignment, allowing for accurate placement of large arrays. Additionally, indium or solder bumps can be fabricated to small dimensions, yielding high density interconnects.

Gold balls can be quickly placed on standard silicon VLSI I/O pads with no extra silicon process steps. A common commercially available thermocompression ball bonder, adjusted to leave no wire tails, can be used to place the balls. This process has been shown to be reliable and quite cost effective. A major drawback of gold balls is their size, generally 50-100μm, depending upon the ball bonding technology. The size of the bumps in this case will determine the minimum pitch and minimum pixel size of the bonded devices. Correspondingly, the capacitances for the bump and modulator will be high, a total of 4.2pF in our work, so the driver dimensions must also be made large in order to drive this load capacitance.

To evaluate the density limitation of hybrid device arrays, the emphasis on the design of the modulator driver circuit was to minimize the Si area used. Besides driving a capacitive load with a small photocurrent component (our high fill factor SLM has relatively low light input intensities), another requirement of the driver is a large voltage swing. Our modulator driver, therefore, consists of only four transistors, a two stage CMOS inverter with V_{dd} at 10V (Fig. 3). A 10V output swing is possible using standard 5V technology since the V_{GS} breakdown is typically above 12V with the 2μm CMOS technology used.

The first inverter is driven by the five volt input signal. With the supply at 10V, an input high state will cause a weak output low state, since P1 as well as N1 will turn on. This first inverter stage is designed so that the output low state is low enough to ensure that N2 in the second stage does not turn on under this condition. When the input to the first stage is low, the first stage output reaches the rail voltage of 10V since N1 is completely off. The second stage inverter, therefore, has a rail to rail output swing of ten volts. This stage drives the MQW modulator. The silicon chip was fabricated through the MOSIS foundry service.

Flip-chip bonded modulators must have light incident from the back side, since the front is in contact with the silicon driver and logic circuitry. A transparent substrate, or removal of an opaque substrate, is therefore required. We have investigated several material systems and processing approaches which address this requirement.

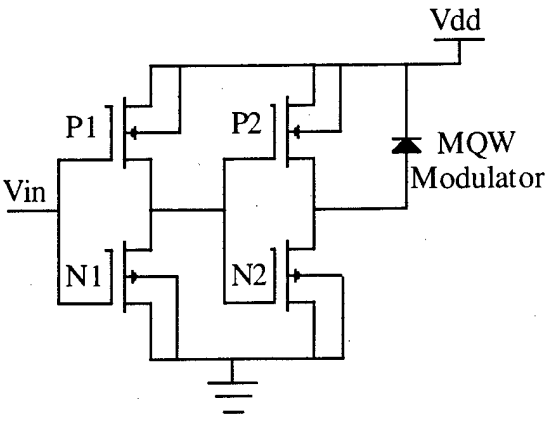

Fig. 3 Schematic of single driver

We have experimentally investigated strained well InAlGaAs/InGaAs MQW modulators operating at 1.06μm. The MQWs are grown atop a step graded, strain relaxing buffer layer to compensate for lattice mismatch between the MQWs and the GaAs substrate. Since GaAs is transparent at 1.06μm, after device processing, the modulator array is bonded directly to the Si driver. The lattice mismatch between substrate and MQWs is a disadvantage, however, since dislocations generated in the buffer layer may propagate to the MQWs, degrading modulator performance. The linewidth of the InAlGaAs/InGaAs exciton peak is generally wider than that of AlGaAs/GaAs MQWs. The full-width at half maximum of the exciton peak in our InAlGaAs/InGaAs material is around 20meV at room temperature.

AlGaAs/GaAs MQW material is lattice matched to the GaAs substrate. Hence, high quality modulator materials are more easily obtained. However, electroabsorption modulation occurs at a wavelength below the GaAs band edge, so the substrate is opaque. To separate the GaAs substrate and MQW material, epitaxial lift off (ELO) and total substrate removal (TSR) techniques have been investigated.

The ELO process involves a highly selective etch through a sacrificial AlAs layer. The lifted-off GaAs film is then bonded to a transparent substrate, in this case quartz. Large area high quality films are difficult to obtain due to water which remains between the substrate and the lifted off films, and surface contamination on the substrate. These can both result in poor bonding and affect the flip-chip process.

In the TSR technique, the GaAs wafer is first bonded to the transparent substrate. The GaAs substrate is then etched away, with a GaAs selective etch being stopped at an AlAs layer. However, the selectivity of the etchant is rather weak compared to AlAs selective etching. This places a tight constraint on the processing. In other words, either the AlAs etch stop layer has to be very thick, which degrades the quality of the device material on top of it, or the backside of the GaAs wafer has to be carefully lapped to be parallel with the AlAs layer.

Presently, bonding techniques using palladium, UV curable epoxy, and Van der Waals bonding are being investigated for the large area thin film process. The details and results of these experiments will be presented.

The modulator material is processed into P-I-N diodes, with the N layer being common to all modulators in the array. This common layer approach reduces the number of bump interconnects required. This, in turn, increases the array density. Mesa isolation is used to electrically separate modulators. Due to the large size of the gold balls, planarization of the modulator array is not required. The distance from the top of the mesa to the bottom is small compared to the diameter of the balls. This simplifies the integration process.

The modulator array has the mirror image of the silicon driver bond pads for flip-chip bonding. The gold p-type contact on top of the mesa also serves as the reflector for the

modulator. Mirror surface roughening, and hence degraded modulator performance, from the annealed contact is avoided through the use of a thin SiO_2 layer between the gold reflector and the GaAs. Windows in the SiO_2 are opened for electrical contact. The efficiency of the Au/SiO_2 mirror have been evaluated.

We have also fabricated through the DARPA Coop an optoelectronic chip for implementing the OTIS system. This chip integrates electronic switches with MQW light modulators and detectors. The chips have been electrically tested and found fully operational.

C. Birefringent Computer Generated Holograms

One of the most significant applications of Birefringent Computer Generated Holography (BCGH) is the packaging of opto-electronic devices and systems. Such systems as OTIS use Computer Generated Holograms (CGH) for beam forming (spot array generation) and optical interconnection between planes of processing element arrays. A single BCGH replaces two conventional holograms and avoids the weight and volume of the polarizing cube beamsplitter. Optical alignment and system assembly are two of the most difficult tasks in constructing functional OE systems. A major advantage of BCGH for these applications is that the widely spaced (i.e., distributed in the volume of the system) conventional CGH are combined into a single pre-aligned planar component which can be located close to the processor array, dramatically simplifying alignment and potentially increasing system reliability, weight, etc. One of our research goals is directed towards even further simplifying the BCGH fabrication process and reducing the cost of two substrate BCGH towards developing a single substrate BCGH with increased spatial resolution using either multi-order BCGH or Form Birefringent CGH (FBCGH). We have developed three different approaches to construct polarization selective birefringent computer generated holograms (BCGHs): two substrate approach, multiple order delay (MOD) approach and form birefringent CGH (FBCGH) approach. These approaches either utilize natural birefringence of the birefringent crystal (first two approaches) or employ subwavelength structures that modify the optical properties of the material (third approach) to achieve polarization selectivity.

For the implementation of the optical interconnects of the OTIS system it is necessary to construct two-dimensional array of optical elements each implementing a dual focal length lens depending on the polarization of the incident light. Initially, we have implemented a single pixel of such an element. We designed and fabricated a BCGH lens with dual focal lengths for the two orthogonal linear polarizations: f_h, for horizontal polarization, was 200 mm, while focal length f_v, for vertical polarization, was 100 mm. When this element is placed 200 mm from an input plane, then the output plane 200 mm beyond the BCGH contains either the image or the Fourier transform of the input image depending on input light polarization. If a large aperture polarization rotator is placed in front of the BCGH, then the output can be switched between the two states depending on whether the polarization is rotated or not. Experimental results demonstrate good performances. Only slight crosstalk between the Fourier transform and the zero order can be seen in the image plane.

Our research goals were directed towards even further simplifying the BCGH fabrication process and reducing the cost of two substrate BCGH towards developing a single substrate BCGH with increased spatial resolution using either MOD-based BCGH or a FBCGH. We consider a single substrate BCGH that utilizes form birefringence and AntiReflection (AR) properties of high spatial frequency (HSF) gratings. Motivated by advantages of a single substrate BCGH, we focus on investigation of HSF gratings in terms of design and optimization of their form birefringence and antireflection properties.

HSF gratings with periodicities much smaller than the wavelength of incident light have been studied because of their many unique and interesting properties which distinguish them from other diffraction gratings. The general behavior of HSF grating appears to be very similar to the one of thin-films, because only the zeroth diffracted order is allowed to propagate. Hence,

HSF gratings can be used as alternatives for single or multiple layers of thin films, allowing more flexibility in design and fabrication processes. Unlike bulk birefringence, caused by anisotropic electrical properties on a microscopic scale, form birefringence arises on scales much larger compared with these microscopic dimensions but smaller than the wavelength of incoming light. The form birefringence phenomenon can be characterized by the phase difference obtained between the transmitted TE and TM polarized light waves, similarly to the optical anisotropy observed in a slab of a uniaxial crystal. Another important feature of HSF gratings is their antireflection property. In comparison with standard optical thin film coating technologies, the HSF antireflection microstructure provides the advantages of durability, damage resistivity, and the ability to substitute materials of specific characteristics that are unsuitable or unavailable in thin-film form.

We choose to investigate two approaches for modeling HSF microstructures. The first approach, known as the effective medium theory (EMT), solves the grating diffraction problem by dividing the grating profile into a stack of multiple layers and substituting each layer with a homogeneous anisotropic material of equivalent dielectric constants for normal incidence TE (electric field vector perpendicular to the grating vector) or TM (electric field parallel to the grating vector) polarized field. Since only the zeroth diffractive order is assumed to propagate, the optical properties of HSF grating are determined using wave propagation in stratified media. The second approach is based on rigorous electromagnetic wave theory, known as differential and integral methods. The design approach we used in this investigation is based on a differential method, called the rigorous coupled wave analysis (RCWA).

One of the objectives of this investigation is to compare the TE and TM wave phase difference and reflectivity characteristics of HSF gratings calculated using the EMT and RCWA, and to determine when it is possible to rely on the results obtained from using EMT, and when it is necessary to use RCWA. We summarize our initial results: the phase difference between transmitted TE and TM polarized waves and reflectivities for TE and TM polarizations are calculated as a function of different HSF grating parameters, including certain grating profiles, grating thickness, angle of incidence, and duty cycle.

We made significant progress in research towards using the form birefringence for construction of a single substrate form birefringent CGH. Form birefringence is a well known effect of subwavelength periodic microstructures. The electric fields parallel to the grating grooves (TE polarization) and perpendicular to the grating grooves (TM polarization) need to satisfy different boundary conditions, resulting in different effective refractive indices for TE and TM polarized waves. Many researchers have demonstrated this effect in the far infrared (IR) region. Recently, with the help of the advances in nanofabrication, 200 nm period gratings were fabricated in GaAs substrate showing strong form birefringence in near IR. Furthermore, these results were found to be in agreement with the numerical simulation results obtained using rigorous couple wave analysis (RCWA). Design optimizations were performed for BCGH using form birefringence.

We designed, fabricated and experimentally evaluated such a binary phase level BCGH element using form birefringent nanostructures (or form birefringent CGH, FBCGH) fabricated on a GaAs substrate using electron beam lithography and dry etching techniques for operation at near infrared wavelength range. For simplicity, the FBCGH element is designed to transmit the TE polarization straight and deflect the TM polarization at an angle. The period of the diffractive grating T is 10 μm. The period of HSFG Λ is 0.3μm and the fill factor of the HSFG F is 0.35. The fabricated element has an etch depth of 0.75μm for the HSFG. Fig. 4 shows the scanning electron micrograph of the fabricated element.

The FBCGH was reconstructed using a He-Ne laser operating at 1.523μm. The measured diffraction efficiency, excluding reflection, and the polarization contrast ratios (PCRs) are

summarized in Table 1. The diffraction efficiency of Table 1 was calculated as the ratio between the intensity measured at a certain diffraction order to that of the total transmitted light through GaAs substrate without FBCGH. These measured results show that the FBCGH has good polarization selectivity (large PCRs) and close to theoretical limit diffraction efficiencies. Note that the form birefringent structure also serves as an antireflection coating, explaining the slightly higher measured diffraction efficiencies compared to that predicted by scalar diffraction theory for a binary phase element (40.5%). The slight asymmetry between the ±1st diffraction orders is due to non-perfect normal incidence.

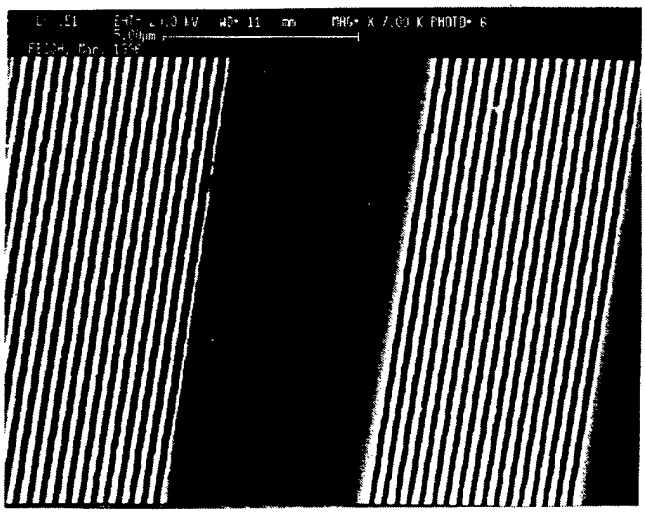

Fig. 4. SEM micrograph of the fabricated FBCGH.

	0-th order	1st order	-1st order
TE efficiency	0.86%	41.4%	44.2%
TM efficiency	75.5%	0.15%	0.44%
PCR	88.2:1	275:1	99.2:1

Table 1 Measured results of the fabricated FBCGH.

In summary, the FBCGH element was designed using effective medium theory and verified to be valid by using the rigorous vector field theory. The design and the experimental evaluations are found in good agreement. The fabricated element shows large polarization contrast ratio (as large as 275:1) and high diffraction efficiencies (>40% for the first diffraction orders). Such element may be useful in making compact and efficient free space transparent photonic switching fabric, as well as monolithic packaging optoelectronic devices and system.

We also investigated the MOD approach for design of BCGH elements fo heterogeneous integration of optoelectronic devices and systems. The MOD approach is based on multiple periods of phase delays (also called modular 2π) using a single birefringent substrate. Such approach may reduce the cost and simplify the fabrication process of such polarization selective diffractive optical elements. The required etch depth is much deeper than that in a normal DOE. In the following we report the first experimental demonstration to our knowledge of a polarization selective birefringent CGH (SSBCGH) using single birefringent substrate.

The ideal substrate material suitable for this application should have large birefringence to assure that the required etch depth d can be fabricated with high accuracy. We used a new type of birefringent crystal, yttrium orthovanadate (YVO_4), which has large birefringence and can be relative easily processed using microfabrication techniques. The birefringent substrates are x-cut YVO_4 grown by Castech-Phoenix, Inc. The refractive indices are $n_o = 2.0241$ and $n_e = 2.2600$ at wavelength of 0. 5145 μm. We find all the possible combinations of Φ_o and Φ_e , the phase of ordinary and extraordinary wave at each pixel, for construction of a binary phase levels SSBCGH (see Table 2). In Table 2, d_l and d_m are the exact etch depths required to obtain the desired phase delays with integer l and m. From Table 2, we observe that the approximation errors are less than 5% for all cases except one. This can be solved by taking the value d as the weighted average of d_l and d_m instead of one half of the summation. Some other optimizations such as choosing a different set of phase quantization bases may also reduce the approximation errors. Because the absolute phase in diffractive optics is of no concern, we can remove an etch depth bias of 1.013 micrometers without affecting the desired relative phase values between different pixels. The new real values of the etch depths d_r are also listed in Table 2. We can also observe that only two distinct etches are needed to construct a binary phase level SSBCGH. (s and t in Table 2.)

		d_l, d_m	$d = (d_l + d_m)/2$	$d_r = d - 1.013$	error (%)	
Φ_o, Φ_e	l, m	(μm)	(μm)	(μm)	δ_l/Φ_o^*	δ_m/Φ_e^*
0, 0	4, 5	2.010, 2.042	2.0260	1.0130 (= s)	+3.27	-3.9
0, π	2, 2	1.005, 1.021	1.0130	0.0000	+1.63	-3.8
π, 0	2, 3	1.256, 1.225	1.2406	0.2276 (= t)	-6.1	+3.8
π, π	4, 5	2.261, 2.246	2.2535	1.2405 (= s+t)	-2.9	+3.8

Table 2 Design results and the real etch depth required for a binary phase single substrate BCGH. (* When Φ_o and/or Φ_e are zero, they are taken to be 2π when calculating the errors.) d_l and d_m are the exact etch depths required to obtain the desired phase delays with integer l and m

For experimental demonstration and characterizations of such a SSBCGH, we constructed a diffractive polarization beam splitter that diffracts one polarization while transmitting the other. This is a special case of the dual function element. The experimental evaluation of the element showed 70.8% diffraction efficiency and 79.7:1 PCR into the zero order, 37.4% diffraction efficiency and 33.0:1 PCR into the +1-st order and, 38.9% diffraction efficiency and 32.5:1 PCR into the -1-st order.

We also used rigorous coupled wave analysis (RCWA) to simulate the performances of our fabricated SSBCGH element. Fig. 5 shows the simulation results for diffraction efficiencies and PCRs as functions of etch depth. From the simulation results, we can observe that, the good performance (41.6% diffraction efficiency and over 100:1 PCR) can be obtained from the ideal case, which is close to our geometrical optics design. The experimental performance of the second element is very close to that predicted by the RCWA (See Fig. 5). From the simulation, we can also see that the performance of a SSBCGH can still be improved with more accurate etch depth.

We designed, fabricated and evaluated experimentally the polarization selective computer generated holograms using a single birefringent substrate. The fabricated elements show close to the theoretical limit diffraction efficiency and large polarization contrast ratio. The duty ratio and the shape of the grating change the performance of the SSBCGH and need to be controlled accurately. A Cr layer is useful in achieving linewidth control. Such elements are useful in packaging optoelectronic devices and system.

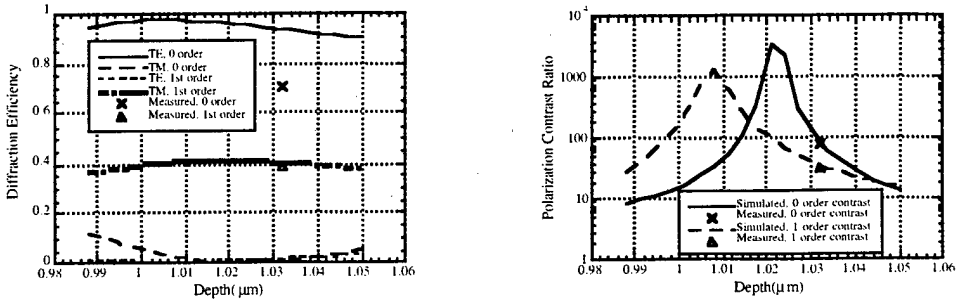

Figure 5. Simulated (curves) and measured (data points) (a) diffraction efficiencies, and (b) polarization contrast ratios of an ideal SSBCGH

We have also completed a design of the SSBCGH that is implementing OTIS. The optical system consists of two BCGH elements, two quarter-wave retardation plates for polarization control, a polarizing beam splitter to couple light into the system, and two opto-electronic chips which were Bell Labs' GaAs MQW modulators integrated with Si CMOS. The circuitry on the chip contains an array of local electronic switches which, combined with the global OTIS interconnects, provide full routing between all processing elements in both directions. The two independent polarization functions allow for compact packaging of the system. One of the polarization functions of the BCGH element is used for interconnections, while the other function is used for illumination of the modulator arrays. The interconnection and illumination paths are 'folded' onto one another substantially reducing the system size and hardware complexity. Two BCGH elements and the corresponding systems have been designed with 10μm and 5 μm minimum feature size, respectively. The BCGH elements have been fabricated and are being evaluated (i.e., spot size, diffraction efficiency, polarization contrast ratio, etc.).

Recently, we have explored the applications of such polarization-multifunctional DOEs in packaging optoelectronic-VLSI chip. Increasing demand for data transmission and processing has spurred development of silicon VLSI devices with parallel optoelectronic (OE) input and output (I/O). OE chips with photodetector receivers and laser or optical modulator transmitters can support large-scale high-speed parallel communication over short distances using free space optical interconnects. The optical signals are routed to photodetectors and transmitted from the modulators or laser devices using arrays of DOEs or micro-optics components. In general, optical input and output signal paths are different, which implies that the optics must provide dual functionality in implementing the communication links. Since conventional DOE or micro-optics components do not have this dual functionality, additional components such as polarization beam splitters are required to separate the input and the output signals. The unique capability of BCGH elements enables more compact and reliable packaging. This is the first integration of diffractive beam-forming optics with optoelectronic (I/O) devices flip-chip bonded to CMOS VLSI electronics, and the first integration of a BCGH with any optoelectronic device.

Packaging OE VLSI

For our experiment we use BCGH to package an OE-VLSI chip fabricated through the Bell Labs / GMU Co-Op Foundry. The chip I/O consists of 20×10 MQW diodes flip-chip bonded onto silicon VLSI electronics. Half of the diodes that function as photodetectors for receiving input data interleaved in space with the other half that function as optical modulators for transmitting output data. The MQW modulators require 850nm optical input power. The principle advantage of this approach is that it replaces a distributed bulk optics system with a compact and rugged OE-VLSI module that has beam forming optics permanently aligned to a chip mounted in a standard electronic ceramic pin grid array (PGA) package.

The BCGH element was designed and fabricated as a binary phase level 10×10 off-axis diffractive lenslet array for extraordinary polarized illumination while remaining an optical flat under ordinary polarized illumination. We employ the design and fabrication based on multiple order delay approach on a 10mm×10mm x-cut YVO_4 substrate. The first order diffraction efficiency (excluding reflection loss) of the fabricated element was measured to be 35% with an average polarization contrast ratio (defined as the ratio between intensities measured under two orthogonal polarization for a certain diffraction order) of 40:1.

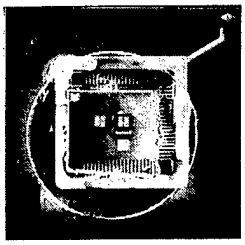

Fig. 6 packaged OE-VLSI module.

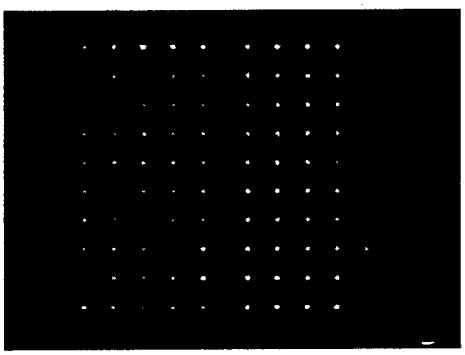

Fig. 7 Spot array generated by BCGH lenslet and reflected from the MQW modulators

The packaged module (see Fig. 6) was tested by illuminating the system with a collimated beam and imaging the reflected output onto a CCD using a 4F telescope imaging setup that also included an iris that acted as a spatial filter, reducing background light that results from surface reflections and the BCGH higher diffraction orders. Fig. 7 shows an image of the generated spot array reflected off the modulators array demonstrating good BCGH performance, except the fact that the spot array reflected from the modulator array consists only of 10 rows and 9 columns. Due to an inversion in the chip layout, the 10th column lands on a row of detectors rather than on an active row of modulators. The CCD camera output was collected by a Macintosh computer running VIDSCOPE, a real-time image analysis program. With a pulsed

input, this program can be operated as a sampling oscilloscope to obtain high speed measurement of repeated data patterns.

The modulator array was modulated at low speed to test the array uniformity rather than device frequency response. The reflected intensity at each of the output modulators was measured and plotted as a function of time, allowing simultaneous measurement of the entire array. Each measurement of the entire array is obtained by integrating the light intensity on a 3×3 pixels square on the CCD. Fig. 8 shows the output that indicates traces of each of the 90 optical output channels of the packaged BCGH and OE VLSI chip. These results show that BCGH element works correctly as designed. The spots are uniformly generated (within ±20% deviation from the average). These spots registered with the modulators with good accuracy across the entire array. The two functions of the BCGH do not interfere with each other. The modulation contrast of 1.5:1 was less than the 2:1 measured with a tightly focused (5μm FWHM) beam, which indicates that lower F/# lenslet array could improve performance.

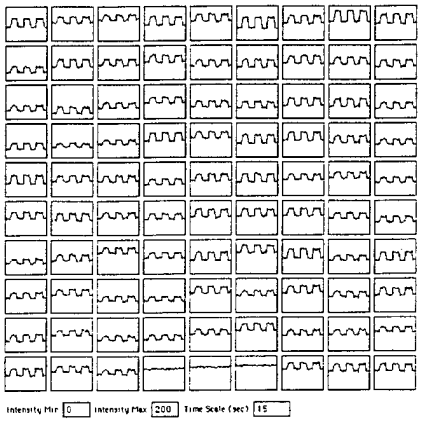

Fig. 8 Intensity vs time traces of all 90 modulator outputs.

OTIS /BCGH Interconnects

The optical transpose interconnection system (OTIS) is a simple means of providing a transpose interconnection using only a pair of lenslet arrays. This system has been shown useful for shuffle based multi-stage interconnection networks, mesh-of-trees matrix processors, and hypercube interconnections. The transpose interconnection is a one-to-one interconnection between L transmitters and L receivers, where L is the product of two integers, M and N. To implement the interconnection a $\sqrt{N} \times \sqrt{N}$ array of lenslets is placed in front of the input plane, and a $\sqrt{M} \times \sqrt{M}$ array of lenslets is located before the output plane. The $M \times N$ transpose is equivalent to a k-shuffle, where k equals N. For example, a 4096 channel ($M = N = 64$) interconnection can be implemented with two 8×8 lenslet. An interesting application occurs when $k = \sqrt{L}$; in this case only one stage of optics and two stages of optoelectronic switches are required for full routing between the input and output channels. If $M = N$, then both lenslet planes are identical; and with minor modifications, such as opaque areas on the lenses to prevent cross-talk, the system can be made bi-directional.

If normally illuminated optical modulators are used as the transmitters, there will be light losses in the OTIS system due to vignetting (clipping of the light cones reflected from the modulators) since the OTIS lenslets do not extend to the edge of the chip (the losses amount to 89% for a corner modulator). In order to achieve good light coupling into the interconnect lenslets, the modulators require directed illumination. This can be achieved by using off-axis

(decentered) area-multiplexed diffractive lenslet arrays. Both the illumination and interconnection optics can be combined into the same optical element using the BCGH.

A system implementation of OTIS using GaAs modulators, operating at 850 nm, integrated with Silicon CMOS and binary phase Birefringent Computer Generated Holograms has been performed. Optical power enters the system from the sides and is redirected by a Polarizing Beam Splitter towards the opto-electronic chips. Diffractive micro-optics focus the light onto the optical modulators, and after reflection from the modulators route the light to detectors on the opposite chip. Quarter-wave retardation plates are also needed for polarization control.

The transmitter technology used is the AT&T GaAs on Si CMOS. The process involves flip-chip solder bonding GaAs Multiple Quantum Well (MQW) modulators directly onto finished Silicon CMOS circuitry. As GaAs is opaque at 850 nm, it is necessary to remove the substrate; this is accomplished by flowing an epoxy etch protectant between chips and removing the GaAs substrate with a chemical stream etch.

Each optoelectronic chip has 64 GaAs devices on it. These are divided into a 4 X 4 array where each element of array consists of two GaAs modulators and two MQW diode modulators used as optical photodetectors. The optical system implements an OTIS connection between the elements of the array providing two channels of communication in each direction. In addition to the modulator drivers and receiver circuits, the circuitry on the chips contains local bypass-and-exchange switches which, with the optical interconnects, allow bi-directional, full routing between all inputs and outputs.

System:	**1**	**2**
BCGH Minimum Feature Size:	10 μm	5 μm
Illumination Lens focal length:	12.50 mm	6.20 mm
Interconnection Lens focal length:	4.17 mm	2.07 mm
Total system length:	50.00 mm	24.80 mm
F.W.H.M. Spot Size on Modulator Plane:	38 μm - 50 μm	25 μm - 37 μm
Maintains proper OTIS geometry to eliminate crosstalk:	No	Yes

Table 3. System Design Characteristics

No one optical system could meet all of the design criteria (diffracted spot size, system length, proper OTIS system geometry, etc.). Initially, two systems were designed, corresponding to a minimum feature size (MFS) for the BCGH of 5μm and 10μm. Tables 3 and 4 illustrate the design and characterization of the two systems.

The system performance was severely hampered by the low diffraction efficiency of binary phase diffractive elements. Further adding to this difficulty is the OTIS geometry, which requires a wide variation in lenslet f-numbers. The fastest lenslets are limited by the fabrication technology, which results in the slower ones having a limited number of fringes and, consequently, even poorer diffraction efficiency. To alleviate this problem, two new systems were designed.

The 10μm MFS system was re-designed for fabrication at four phase levels. The theoretical diffraction efficiency of a four phase level diffractive element is over 80%. Because

the three passes through the BCGH are involved, this should result in a eight-fold increase in system power throughput , and an even greater S/N, as the stray (undiffracted) light has been reduced.

This second system involved a re-working of the OTIS geometry. The system is based on OTIS-VE [M. Blume, G. Marsden, P. Marchand, and S. Esener, "Optical Transpose Interconnection System for Vertical Emitters," *OSA Technical Digest Series* **8**, p.233 (1997)]. The illumination array now consists of a uniform array of on-axis lenslets, while the interconnect lenslets have been fabricated off axis and their apertures have been expanded. The system was also designed at four phase levels, except for the outer periphery of the interconnect optics which would have had a much too close fringe spacing. This region was designed as binary phase.

	System 1	System 2
Illumination Focal Length	12.40mm (12.5mm)	6.20mm (6.20mm)
Interconnection Focal Length	4.51mm (4.17mm)	2.08mm (2.07)
Illumination Spot Size Range	40-46μm (38-50 μm)	28-35μm (25-37 μm)
Diffraction Efficiency (fast lenslet)	35% (40%)	36% (40%)
Polarization Contrast Ratio	>20 : 1 (extinguished below noise	~ 2 : 1

Table 4. System Characterization Results

The new designs are currently being fabricated and will be implemented in an experimental set-up along with the OTIS chips as soon as possible.

5. Personnel Supported

Y. Fainman

S. Esener

P. Marchand

Fang Xu

Lee Hendrick

Francis Zane

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Y. Fainman, " Optics in computing and communications," presentation and participation on the pannel "Potential Roles of Ultrafast Optics in Communications and Information Processing" at the 10-th Annual Meeting of IEEE/LEOS, 1997 (invited)

Y. Fainman, "Real-time optical analog-to-digital (ROAD) converters, presented at the DARPA/ETO Workshop on A/D Converter Technology, October 1-2, Crystal City, VA, 1997

Y. Fainman, "Optoelectronic System for Space-Variant Signal and Image Processing," presented at the 1998 DARPA's Optoelectronic Program Review, February 9-12, Reston, VA, 1998

Y. Fainman, P. C. Sun, Y. Mazurenko, K. Oba, D. Marom, " Storage formats for ultrahigh speed communication and processing, presented at the AFOSR Workshop on Applications of Spectral Hole Burning, March 8-11, Montana State University, Bozman, Montana, 1998.

8. New discoveries: None

9. Honors/Awards: Y. Fainman became a Fellow of the Optical Society of America, 1995