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Paul Bernard Fischer

and have found that it is complete and satisfactory in all respects,
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examining committee have been made.

Prof. Stephen Y. Chou

Name of Faculty Advisor

Signature of Faculty Advisor

Date

GRADUATE SCHOOL

NANOSTRUCTURE ENGINEERING USING ELECTRON BEAM LITHOGRAPHY

A THESIS
SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL
OF THE UNIVERSITY OF MINNESOTA
BY

Paul Bernard Fischer

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FOR THE DEGREE OF
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Abstract

This Ph.D. thesis addresses nanostructure fabrication techniques based on electron beam lithography and their application to: the creation of ultra-fast metal-semiconductor-metal photodetectors and quantum effect transistors, the investigation of light emission from silicon, and the enhancement of resolution in magnetic force microscopy.

Specifically, this thesis covers the following topics. (1) The implementation and characterization of an ultra-high resolution electron beam lithography (EBL) system created by modifying a scanning electron microscope. (2) The exploration of minimum achievable feature sizes using ultra-high resolution EBL and a lift-off process with polymethyl-methacrylate resists. 10 nm features, which are among the smallest ever achieved using EBL, have been obtained using a double shadow evaporation technique, a ultra-high resolution EBL technique, and a technique utilizing EBL, reactive ion etching, and subsequent wet etching. (3) The application of ultra-high resolution EBL technology to the fabrication of ultra-fast metal-semiconductor-metal (MSM) photodetectors. The fastest response time reported to date has been achieved in this project. (4) The fabrication and characterization of modulation doped field effect transistors. Quantum effects have been observed in a point contact device. (5) The fabrication of sub-50 nm Si structures using EBL, reactive ion etching (RIE) and subsequent wet etching for the study of photoluminescence (PL) from Si. PL has been observed from an array of 20 nm diameter pillars. And finally, (6) the application of high resolution EBL to the study of magnetic materials. Single domain magnetic particles and novel MFM tips have been fabricated.

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Mark Liu is responsible for the theoretical analysis of the metal-semiconductor-metal photodetectors that appear in this thesis. It has been a great pleasure to work with Yun Wang, who provided a lot of theoretical insight into the physics of quantum effect devices. The photoluminescence measurements of silicon nanopillars were performed by Erli Chen and Kevin Dai. I am grateful for insightful conversations with Dr. Edgar Steigmeier at the Paul Scherrer Institute in Zurich concerning light emission from silicon and photoluminescence measurements in general. Special thanks are also due to Dr. Tom Chang, Mark Lagerquist, and Mark Wei, with whom I worked closely on the application of nanofabrication techniques to magnetic force microscopy.

Professors S. Chou, S. Campbell, and W. Zimmermann critically read this thesis. The quality and accuracy of this thesis has improved considerably thanks to their efforts.

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Chapter 1

Introduction

Since the invention of the integrated circuit in 1959 [1], the semiconductor industry has achieved amazing improvements in speed and packing density through the steady down-scaling of device dimensions. The first devices featured dimensions on the order of one hundred microns. Recently, prototype 64 M-bit dynamic random access memories have been demonstrated which utilize 0.3 μm linewidths and cells covering a mere 1.3 μm^2 of surface area.[2]

If this trend is to continue beyond 0.1 μm linewidths, new processing techniques will have to be developed, as this region is relatively unexplored. Another issue at hand is that devices will begin to deviate drastically from their long channel behavior in the sub 0.1 μm regime. Classical transport models will no longer be valid when device feature sizes become comparable to the electron mean-free-path and Fermi wavelength. Quantum interference effects and single electron effects will have to be considered. As researchers push into the 0.1 μm and sub-0.1 μm realm, nano-adjectives, like nanotechnology, nanofabrication, nanostructures, and nanodevices have appeared to denote not only a distinction in size, but also a distinction in fabrication techniques as well as device characteristics.

Several important questions arise from this trend. For example, how small can semiconductor devices be fabricated? How will non-classical effects alter device performance? Can new operating principles be implemented in nanoscale devices? What

other applications exist for nanofabrication techniques? The goals of this Ph.D. thesis research were three-fold. First, to implement and characterize a scanning electron microscope (SEM) for electron beam lithography and to extend existing fabrication techniques and develop new ones. Second to establish baseline fabrication processes for high speed and quantum effect devices. And third, to explore novel applications for nanofabrication techniques. The following topics will be discussed in this thesis:

i) Minimum achievable feature sizes using EBL. Minimum achievable feature sizes were experimentally explored using ultra-high resolution electron beam lithography (EBL) and lift-off processes with polymethyl methacrylate (PMMA) resists. Dense 10 nm features, which are among the smallest ever reported, have been achieved using three distinct techniques. By opening a 40 nm wide trench in a single layer of PMMA using EBL and by double shadow evaporations and a lift-off, two 15 nm wide metal lines 10 nm apart were fabricated on a bulk GaAs substrate. The pitch size of the double lines is 25 nm and is a factor of two smaller than the previous smallest pitch on bulk GaAs substrates. Gratings of 10 nm wide metal lines 30 nm apart, and quantum transistor gates with 10 nm wide gaps over 300 nm long between two metal rectangles were achieved on thick GaAs substrates using a modified scanning electron microscope operated at 35 keV and lift-off of Ni/Au. Lastly, free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15 were fabricated using a novel process consisting of electron beam lithography, chlorine based reactive ion etching, and subsequent HF wet etching.

ii) Fabrication processes for high speed and quantum effect devices. Ultra-high resolution EBL was applied to fabrication of ultra-fast metal-semiconductor-metal (MSM) photodetectors. Response times as short as 87 ps have been achieved with these devices. They are the fastest of their kind reported to date. A process sequence was also developed to create quantum effect modulation doped field effect transistors (MODFETs). Since only the gates of these transistors have stringent nanoscale

requirements, EBL with lift-off was used to fabricate the gates but optical lithography was used for the remainder of the process steps. Although point contact transistors were previously reported [3,4], they were implemented here to verify the process and subsequent analysis techniques and to fertilize the ground for subsequent projects. Quantization of conductance was observed in these devices.

iii) novel applications for nanofabrication techniques Nanofabrication techniques were applied to two novel applications of nanofabrication techniques: the investigation of photoluminescence from silicon, and resolution enhancement in magnetic force microscopy. Despite the fact that silicon, being an indirect bandgap semiconductor, should not be an efficient light emitter, efficient luminescence has recently been reported in porous silicon.[5] Although still controversial, a quantum confinement model has been suggested to explain this phenomenon.[5,6] Ordered arrays of silicon pillars sculpted using EBL, reactive ion etching, and subsequent HF etching were prepared to evaluate this model. Photoluminescence with a peak at 720 nm was repeatedly observed from an array of nanoscale pillars with ~ 20 nm diameters, suggesting that the quantum model cannot easily explain the results.

Nanofabrication techniques were also used to minimize the effect of tip volume on resultant magnetic force microscope (MFM) images. Two approaches have been investigated. In the first approach, tip effects are removed from MFM images by deconvolving the impulse response of the tip from the MFM image. The tip impulse response was determined by imaging the ends of long but narrow, single domain, nanoscale nickel bars. A second approach was to apply contamination lithography and shadow evaporation techniques to fabricate a novel MFM tip that consists of a long non-magnetic pillar of nanoscale diameter and a ferromagnetic film covering only part of the pillar but not the rest of a MFM tip. Such an MFM tip has three advantages. First, because of the nanoscale size and shape anisotropy, the magnetic tip is single domain.

Second, due to the sharpness and small effective magnetic cross section of the tip, it offers higher resolution. Third, due to the small magnetic charge, it is less likely to alter the magnetic properties of the sample.

The core of this thesis has been devided into three main chapters. Since electron beam lithography is the cornerstone of this effort, chapter 2 presents some background concepts that are implicit to the achievements presented in later chapters. A description of the EBL system that has been developed by members of the NanoStructure Laboratory is also provided. Chapter 3 is devoted to three distinct 10 nm fabrication techniques that have been developed. A collage of nanofabrication applications is presented in chapter 4, which covers high speed and quantum effect devices, as well as the investigation of photoluminescence from silicon and resolution enhancement in magnetic force microscopy. As such, chapter 4 demonstrates the utility of nanofabrication technologies. Finally, a summary is presented in chapter 5.

Chapter 2

High-resolution Electron Beam Lithography

2.1 Introduction

Lithography is a process by which a pattern is defined onto a sample surface and is accomplished in semiconductor processing by exposing a radiation sensitive resist with electrons, ions, or photons. After development the resist pattern is transferred to the substrate by etching or deposition techniques. Electron beam lithography (EBL) was utilized extensively in this thesis work and thus will be the focus of this chapter. For a general discussion of the sub-micron issues and capabilities of different lithographic techniques, see ref. [7].

Figure 2.1 shows a schematic of an electron beam lithography system. In the general case an electron beam is deflected to a desired location and maintained there long enough to chemically modify the resist. The beam would then be blanked, moved to a new location, and the blanking would be turned off to again expose the resist. This process can then be repeated until the desired pattern has been fully exposed. The process is analogous to drawing a picture on a piece of paper with an extremely sharp pencil and is therefore highly flexible. Another advantage of EBL, as will be shown in chapter 3, is that it is capable of achieving approximately 10 nm resolution. However,

exposures are done serially, drastically reducing throughput and limiting the applicability to research environments and mask making efforts.

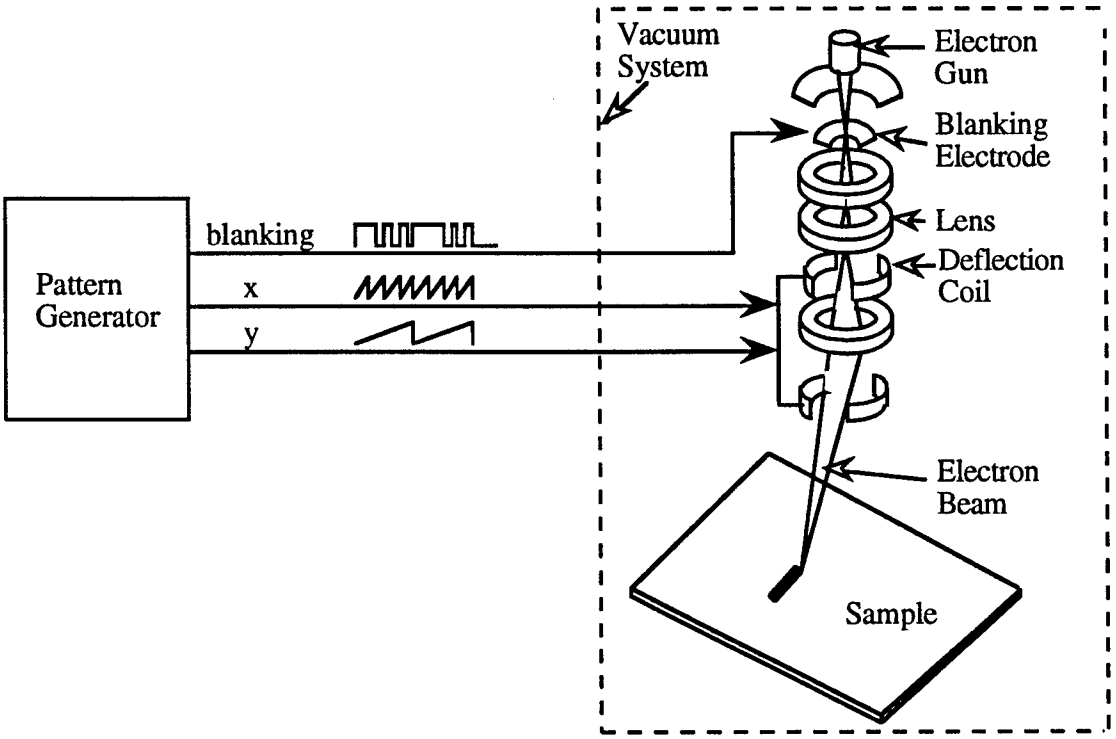


Figure 2.1. Schematic of a electron beam lithography system.

2.2 Fundamentals of Electron Beam Lithography

2.2.1 Electron Sources

Although the electron source is not usually a variable once the EBL system has been specified, it is useful to understand the advantages and limitations of the various sources. A common electron source emits electrons by thermionic emission (Fig. 2.2). In addition to the current source for heating the tungsten filament to approximately 3000 °K, the gun consists of a Whenelt electrode which electrostatically focuses the emitted

electrons to a crossover point. The crossover point is typically 10 μm in diameter and is defocused by subsequent electron lenses to form the final electron probe.

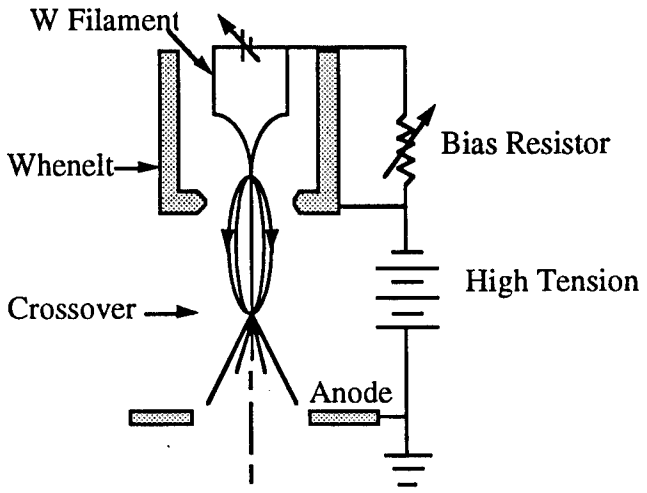


Figure 2.2. Schematic of an electron gun with a thermionic source.

The main characteristic used to evaluate an electron source is its brightness, β, which is defined as the current emitted per unit area per unit solid angle. Brightness determines the maximum current density one can achieve at the image plane. For thermionic emission the brightness can be shown to equal:

$$\beta = J_0 \frac{(-q)\phi}{k_B T}$$

where J_0 is the peak current density at the crossover, q is the electron charge, ϕ is the accelerating potential in volts, k_B is Boltzman's constant, and T is the emitter temperature. The significance of brightness is that it determines the maximum current density that be obtained at the image plane. The current density in the focused spot at the image plane, J_i, is limited by the Langmuir equation [8]

$$J_i = J_0 \frac{(-q)\phi}{k_B T} \alpha^2 = \pi \beta \alpha^2$$

where α is the semi-angle of convergence of the beam. As will be discussed in section 2.2.2 it is desirable to make the semi-angle of convergence as small as possible to minimize chromatic and spherical aberrations, making the source brightness the main variable to increase the current density at the image plane. The brightness of tungsten emitters operating at 40 kV is about 2×10^5 A/cm^2•Sr. One approach to improve source brightness has been to search for materials with a lower work function. Such materials require a lower operating temperature and thus an increased brightness can be obtained. The most common such material is LaB_6 which has a brightness of about 3×10^6 A/cm^2•Sr.[9] The drawbacks for thermionic emitters are a relatively large energy width, ΔE (0.5 - 2 eV), and low source brightness for low accelerating potentials.

An alternative to thermionic emitters are field emitters which operate at room temperature by electron tunneling through the work function barrier in the presence of a high electric field. Field emission guns are more complex than the thermionic emission gun. The advantage of field emission sources is an extremely high brightness, ~10^9 A/cm^2•Sr, and a low energy width, ΔE (0.2 -0.5 eV). Furthermore, the high brightness can still be achieved using accelerating voltages as low as several kV. The disadvantage of the field emitters is a relatively small emission cone angle leading to reduced total current capabilities (10 μA is typical for commercial SEMs).

2.2.2 Limitations on Electron Beam Spot Size

The purpose of the electron lenses in a SEM is to demagnify the crossover formed by the electron gun. The ideal electron beam diameter at the sample surface, d_o, neglecting aberrations, is [10]:

$$d_o^2 = \frac{I}{0.15\ \pi^2\ \beta\ \alpha^2}$$

where I is the beam current. Several aberrations will further distort the final spot size. Of the possible aberrations, spherical and chromatic aberrations are the most significant for electron microscopy.[11] Spherical aberrations cause electrons passing through the outer zones of an electron lens to be focused to a shorter focal length. The minimum beam diameter in the presence of spherical aberrations, d_S, is given by:

$$d_s^2 = 0.5\ C_s\ \alpha^3$$

Here C_S is the coefficient of spherical aberration. For a well designed lens, C_S is equal to the focal length.[12]

Variations in electron energy as well as fluctuations in the lens supply current will also lead to focal length variations. The minimum beam diameter in the presence of chromatic aberrations, d_C, is given by:

$$d_c^2 = C_c \frac{\delta V}{V} \alpha$$

where V is the accelerating potential, and C_C is the coefficient of chromatic aberration and is also approximately equal to the focal length of the lens for a well designed lens.

The final beam diameter , d_i, is approximated by assuming a purely Gaussian beam and adding the components in quadrature:

$$d_i^2 \approx d_o^2 + d_s^2 + d_c^2$$

For high resolution imaging and lithography, it is necessary to minimize the resultant beam diameter, d_i. Once a system has been specified, including the gun type and brightness, the beam diameter can be controlled by adjusting the beam current, accelerating voltage, and lens-to-sample spacing (thus focal length of lens and finally the aberration coefficients!). For high resolution electron beam lithography, this means using the highest reasonable accelerating voltage, lowest beam current, and smallest lens-to-

sample spacing. As an example, the commercial SEM that was modified for the nanofabrication work presented in this thesis, a JEOL 840-A, features a tungsten filament gun, a maximum stable accelerating potential of 35 kV, and minimum reasonable lens-to-sample spacing of 5 mm. A minimum beam diameter of about 4 nm can be achieved using a beam current of approximately 4.5 pA, an accelerating voltage of 35 kV, and a lens-to-sample spacing of 5 mm. Under certain considerations it is desirable to perform EBL at low accelerating voltages (1-10 kV). This is possible, but high resolution results require the use of a field emission source.

2.2.3 Resists, Developers, and Contrast

Almost all semiconductor fabrication techniques delineate features in the substrate through an intermediate resist layer. Lithography is used to pattern the resist, and then the resist serves as a mask for the subsequent process steps. There are two types of resists, positive and negative (Fig 2.3). In a positive resist the region

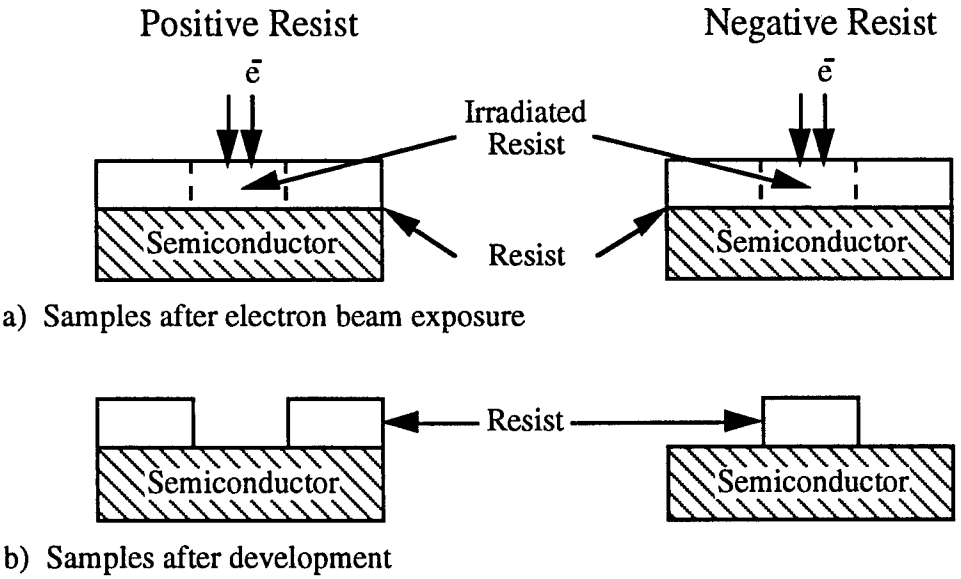


Figure 2.3. Schematic of (a) positive and (b) negative resists.

chemically modified during the exposure is removed by the developer. In a negative resist, the chemically modified material remains after development.

Resists are characterized by such properties as: resolution, contrast, sensitivity, and etch resistance. Resolution describes the smallest features that can be defined in the resist. Contrast, γ, is a measure of the change in dose necessary for the resist to go from fully unexposed to fully exposed as defined as

$$\gamma = \frac{1}{log\left(D_f / D_i\right)}$$

where D_f and D_i are defined in figure 2.4. For high resolution work, the highest possible contrast is desirable since it becomes possible to develop out only the regions directly exposed by the electron beam. Sensitivity is the minimum dose required to fully expose a region. This important parameter not only limits the throughput but also indicates the susceptibility of the lithography tool to drift during exposure. The ability of the resist to protect the substrate during etching is described by the etch resistance. Other parameters such as the toxicity, pinhole density, and adhesion also determine the suitability of a resist.

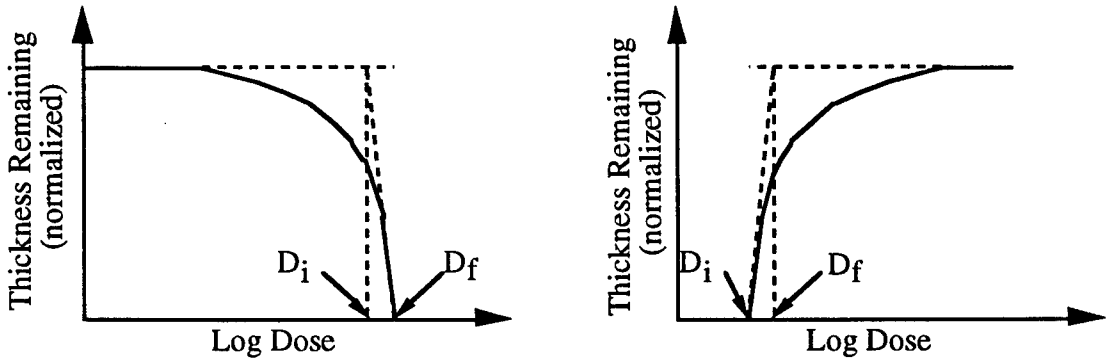


Figure 2.4. Determination of contrast and sensitivity for (a) positive and (b) negative resists

Polymethyl methacrylate (PMMA), also known under the trade names of 'Lucite' and 'Plexiglas', has the highest resolution of all the conventional positive organic resists for electron beam lithography. Features as small as 5 nm have been obtained in PMMA resists using a 80 keV beam.[13] The main disadvantage of PMMA is its low sensitivity. A dose of 50 to 500 $\mu C/cm^2$ is required to expose the resist. Also, its reactive ion etch (RIE) resistance is on the order of 1:1 (PMMA:material) for materials like SiO_2 and Si_3N_4.

Upon exposure to high-energy radiation, PMMA undergoes polymer chain scission and decomposition of its ester side groups. The results is a reduction in molecular weight and formation of volatile products such as CO_2, CO, and CH_4. The release of volatile products increases the polymer's free volume and greatly enhances the diffusion rate of the developer into the polymer.[14] Furthermore, the developers are designed such that lower molecular weight fragments have higher dissolution rates relative to the unmodified polymer chains. The main PMMA developers fall into two categories, cosolvent and solvent-precipitant systems. Cosolvent developers, like isopropanol/water, consist of a mixture of two pure non-solvents that when combined form a solvent.[15] In solvent-precipitant systems, the polymer is dissolved in the solvent and precipitated by the addition of a non-solvent. Methyl ethyl ketone:methanol and Cellosolve:methanol are two examples of solvent-precipitant systems.

PMMA is available in a large variety of molecular weights with the different molecular weights exhibiting different sensitivites. For example, 350 K PMMA is less sensitive than 185 K PMMA by a factor of about 1.3.[16] Although the sensitivity difference is not large, it does provide flexibility in the lithography process. An alternative approach to improving the sensitivity of PMMA has been to copolymerize PMMA with another more sensitive monomer.[17]

High-resolution, negative-tone EBL resists are also available. Of the available resists, SAL-603 [18] (Shipley) offers the highest resolution. Although features as small as 50 nm have been achieved in this resist [19], the resolution appears slightly lower than PMMA. SAL-603 is a three component resist consisting of a novolak resin, an acid activatable cross linker, and a photo acid generator. The exposure process selectively converts some of the photo acid generator to acid. During a post exposure bake the acid aids in forming covalent bonds between the novolak resin and the cross linker. The resultant cosslinked resist is relatively insoluble in a aqueous alkaline developer.

The two step development process for SAL-603 resist has been mapped out and it has been determined that a contrast as high as 8 is obtainable in this resist.[20] The result is a resist with a relatively high sensitivity of about 5 $\mu C/cm^2$ which is about a factor of 40 more sensitive than PMMA. Another advantage of SAL-603 is its etch resistance. Since it is a novolak resin based resist, its etch resistance is similar to that of standard photoresists and etches at a rate of about 300 Å/min for common Si dry etching processes.[18]

Other high-resolution EBL materials have also been studied. For example patterns on the order of 2 nm have been written in NaCl [21] and B-aluminas.[22] CaF_2 [23], LiF [24], AlF_3 [25], and SiO_2 [26] have also been investigated and show promise for high-resolution lithography. However, these materials require high doses, and more complex preparation techniques, and questionable pattern transfer techniques.

2.2.4 Electron Scattering and the Proximity Effect

Energetic electrons penetrating into a solid undergo elastic and inelastic scattering. Such scattered electrons can be sorted into two groups, those scattered through angles less than 90°, and those scattered through angles greater than 90°. The

groups are referred to as forward and backscattered electrons, respectively. Thus, the exposure from an incident electron beam is not spatially limited to the initial beam distribution. The effect of electron scattering can be characterized by the double-Gaussian model [27]

$$exposure(r) = \frac{1}{\pi(1+\eta)}\left[\frac{1}{\beta_f^2}\,exp\left(\frac{-r^2}{\beta_f^2}\right) + \frac{\eta}{\beta_b^2}\,exp\left(\frac{-r^2}{\beta_b^2}\right)\right]$$

where r is the radial distance from the beam position, β_f is the forward scattered electron range (finite incident beam diameters are also modeled in β_f), η is the ratio of integrated exposure from backscattered electrons relative to forward scattered electrons, and β_b is the backscattered electron range. Parameters for this model depend on the incident beam energy, spot size, and the resist and substrate materials. However, if the desired patterns are on the order on 0.1 μm, the exposure distribution is more accurately approximated by a double Gaussian plus an additional exponential term.[28] Several experimental techniques have been developed to determine these parameters.[28,29]

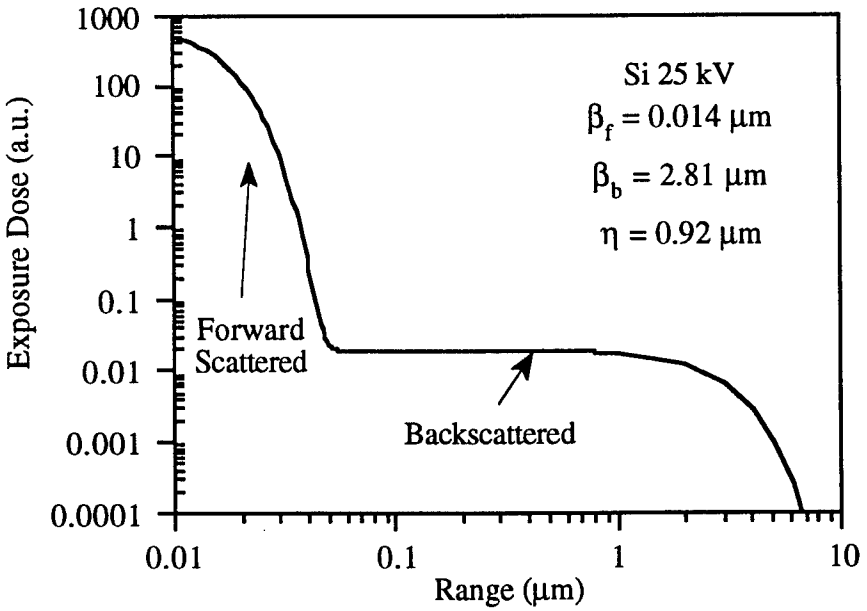


Figure 2.5. Double Gaussian model describing the scattering of electrons from a finite size source (parameters from [28]).

Figure 2.5 illustrates the double Gaussian model for a 25 kV beam incident on silicon (parameters used are from [28]). The model represents the impluse response of the exposure process. The true exposure distribution is found by convoluting the point exposure response with the desired exposure pattern. Since regions not directly exposed by the incident beam are exposed by scattered electrons, the effect is referred to as the proximity effect. The convolution of the double-Gaussian exposure function with a grating exposure pattern consisting of infinitesimally narrow lines is shown in figure 2.6. The grating in this example is 10 μm by 10 μm, and the exposure dose is plotted for a diagonal path starting at a corner. Backscattered electrons create an appreciable increase in the background dose in the center of the grating relative to the corner. In addition, the modulation function, defined as $(D_{max} - D_{min})/(D_{max} + D_{min})$, where D_{max} is the maximum local exposure dose and D_{min} is the minimum local exposure dose, is greatly reduced at higher densities due to the proximity effect.

An experimental demonstration of the proximity effect is shown in figure 2.7 which consists of (a) a grating pattern defined using electron beam lithography, (b) an enlarged view of a corner, and (c) an enlarged view of the center. All images are from the same structure. The metal lines in the center are about twice as wide as the metal lines at the corner of the feature.

The proximity effect can be minimized by working on thin substrates to reduce backscattered electron contributions and using thin resists to reduce forward scattering, or by using sparsely spaced patterns which are smaller than the backscattered electron range. Alternatively, proximity effects can be compensated for by adjusting the exposure doses, but cannot be completely eliminated because negative exposure doses are not available. Another technique for minimizing the proximity effect utilizes a second exposure which equalizes the background exposure.[30] Yet another approach to proximity effect

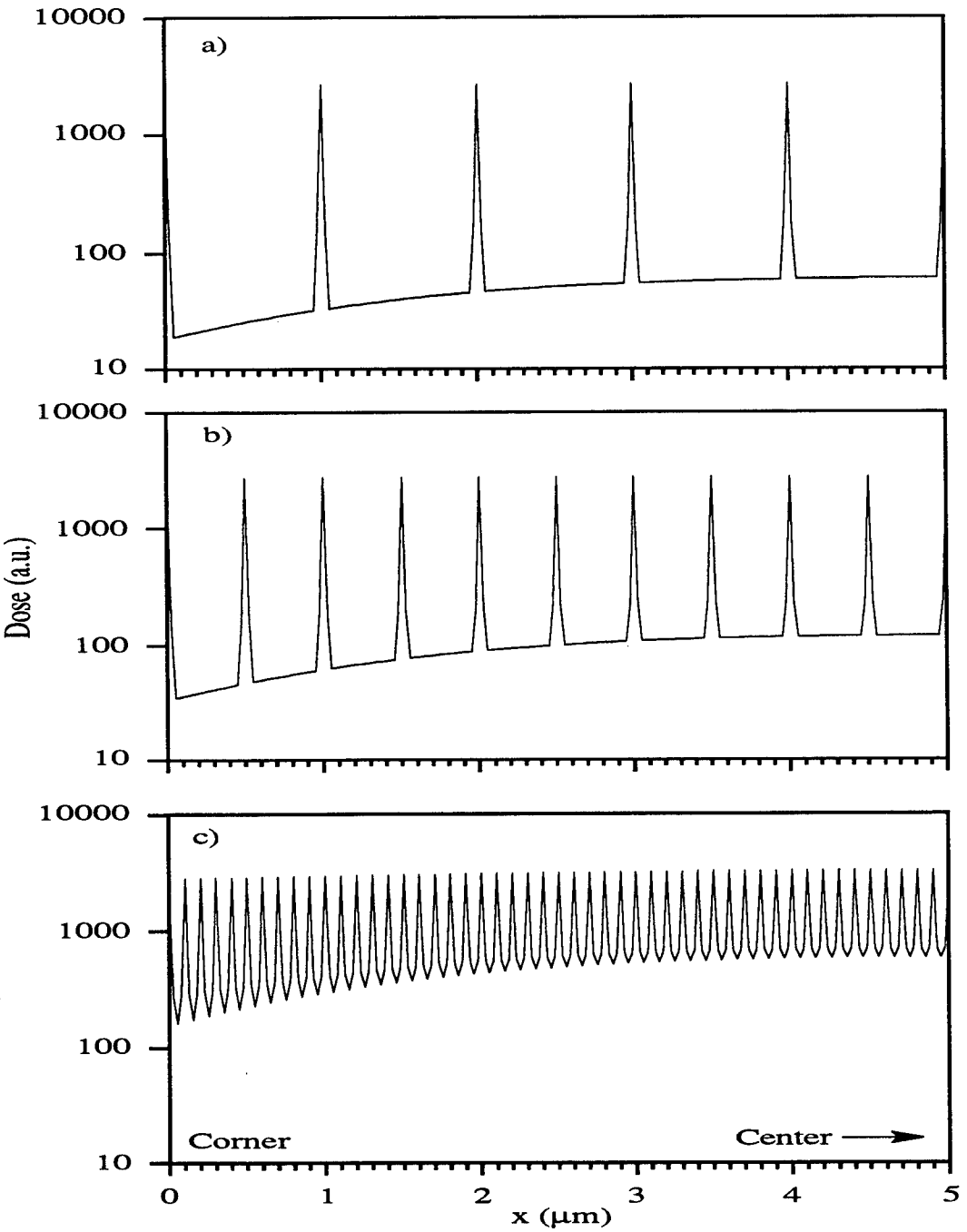


Figure 2.6. Simulation of the proximity effect in which a 10 μm x 10 μm grating pattern with infinitesimally narrow lines is convolved with the double Gaussian scattering model. Scattering parameters were the same as in figure 2.5. Three grating periods were modeled: (a) 1 μm, (b) 0.5 μm, and (c) 0.1 μm. The area of the grating is 10 μm x 10 μm.

reduction utilizes either extremely high [31] or low [32-34] accelerating voltages to control the backscattered electron range and hence proximity effects.

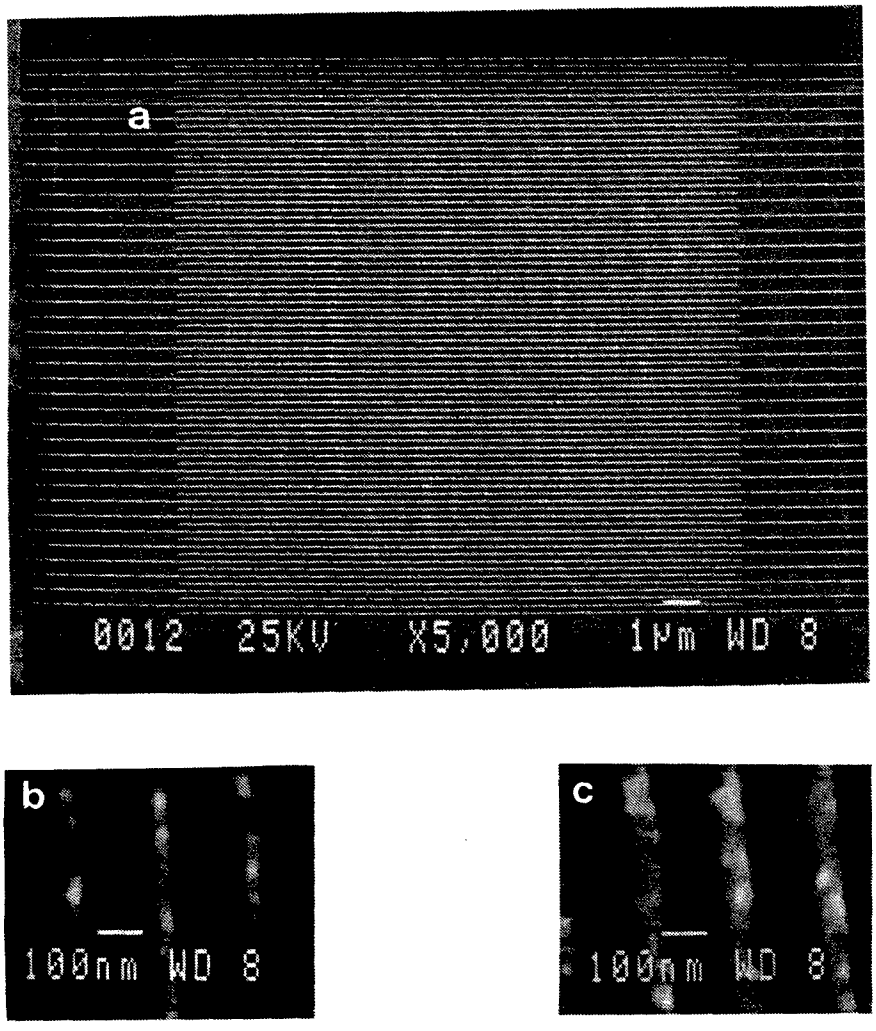


Figure 2.7. Demonstration of the proximity effect: (a) a grating pattern, (b) an enlarged view of a corner, and (c) an enlarged view of the center.

2.2 Pattern Transfer Using Lift-Off

Once the desired pattern has been defined in the resist it can be transferred into the substrate using a variety of techniques. The most straightforward techniques use the resist directly as a mask for wet or dry etching or for an implantation barrier. Since PMMA is a relatively poor dry etch mask and gold, a material difficult to etch chemically, is commonly used in nanofabrication, lift-off (figure 2.8) is a common nanofabrication technique. The process consists of four main steps: (a) resist deposition, (b) electron beam exposure, (c) development and metal evaporation, and (d) lift-off of unwanted metals.

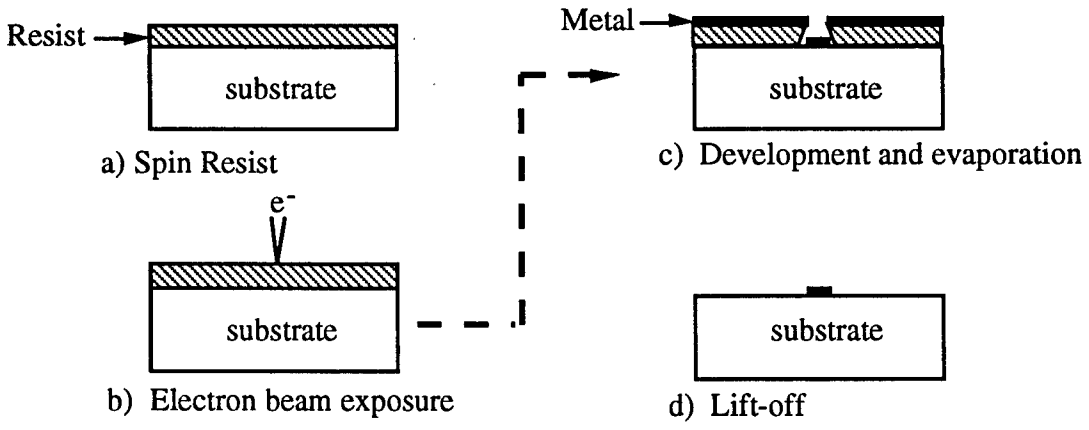


Figure 2.8. Lift-off technique

An undercut resist profile after development is necessary to prevent metal on the surface of the resist to connect with metals on the semiconductor surface. This can be achieved by slightly overexposing the resist [35], or by desensitizing the surface layer of resist, which for the case of SAL-603 can be achieved by adjusting the post exposure bake conditions.[36] Alternatively, undercut profiles can be achieved using a multilayer resist scheme in which a lower layer is chosen to be more sensitive than the upper layers. Common approaches for PMMA involve using a lower molecular weight PMMA beneath

a higher molecular weight PMMA[37], or using a copolymer of PMMA beneath a layer of PMMA [37-39] .

Metal deposition should be from a normal angle of incidence to further ensure that incident metals do not coat the resist sidewalls. A distant point source evaporation technique, like a thermal or electron beam evaporation, is usually used. Under ideal conditions, metal films approaching twice the resist thickness can be lifted off.[40]

The final lift-off step is performed by soaking the sample in a solvent for the resist. For the case of PMMA, acetone is the most commonly used solvent. If processing conditions are not ideal, additional persuasion may be required. The lift-off process used in the work presented in later chapters consisted of two or three cycles of a warm acetone soak followed by a thorough acetone spray using an airbrush. This process may be excessive, but it is effective.

Numerous other pattern transfer techniques are also available. For example, patterns defined in the resist can be used as a plating mask. In this case resist sidewall profiles can be tailored to achieve the desired pattern profiles. Another elegant technique for fabricating nanostructures, like tunnel junctions, is to create a stencil mask and then perform several shadow evaporations through the stencil mask to create devices like tunnel junctions.[41]

2.3 Review of Ultra-high Resolution Electron Beam Lithography

The first demonstration of using a scanned electron beam for lithography purposes occurred in 1960 when Mullenstadt and Speidel patterned 20 nm features on a thin substrate.[42] Most of the high resolution lithography work has utilized PMMA. In 1978 Broers *et al* demonstrated 25 nm linewidths at a period of 50 nm on a thin Si_3N_4 film

using 110 nm of PMMA and a lift-off of 20 nm of AuPd.[43] The thin film substrate was used to minimize the backscattered electron effects. An analysis of the expected minimum pitch size achievable using electron beam lithography with PMMA resists determined that 45 nm is the minimum achievable pitch on thin substrates.[44] This estimate was again closely supported when 10 nm wide lines with a period of 40 nm were achieved on a 50 nm thick Si_3N_4 membrane using a lift-off technique.[16]

10 nm wide lines with a period of 50 nm have also been patterned on a bulk GaAs substrate using a 50 keV beam.[45] Features slightly smaller than 10 nm have also been achieved in PMMA resists. For example, a claim of 8 nm wide lines patterned in PMMA on a bulk Si substrate has been reported.[46] More recently 5-7 nm wide lines have not only been patterned in PMMA using a 100 keV beam, but they have also been transferred into the bulk Si substrate using $SiCl_4$.[13]

Other resists have demonstrated better resolution than PMMA but are rarely used due to extremely high dose requirements and complicated sample preparation techniques. One of the most famous examples is contamination resist in which contamination is deposited on the sample due to electron beam assisted molecular deposition of residual pump oils and other materials. The deposition requires a dose on the order of 1 C/cm^2 and can be used as an etch mask. Using this technique 8 nm AuPd lines have been formed of a thin film substrate.[47]

2.4 Nanostructure Laboratory's High-resolution Electron Beam Lithography System

The electron beam lithography system used for this thesis investigation consists of a modified JEOL 840A SEM with a tungsten gun, 40 keV maximum accelerating potential, a minimum spot size of about 4 nm, a beam blanking unit, and manually

controlled stage micropositioners. The modifications are such that the SEM can be used in either regular SEM mode or lithography mode and consist of four electrical signals: (1) A digital signal forcing the input to the beam deflection amplifiers to come from an external source. (2) A digital signal controlling the beam blanking unit. And (3) and (4), two analog signals which to control the positioning of the beam. The exposure field size is controlled by adjusting the magnification of the SEM.

Two pattern generator systems, a raster scan and a vector scan system (figure 2.9), have been designed and built to control the SEM. In the raster scan system (figure 2.9a), the beam is swept horizontally. If a pixel is to be exposed, the beam blanking is turned off and the beam is held at that point for the specified period of time. Otherwise the beam blanking remains on and the beam is quickly scanned to the next pixel. This process continues until the end of the horizontal scan is reached at which time the vertical position is incremented and the process begins anew.

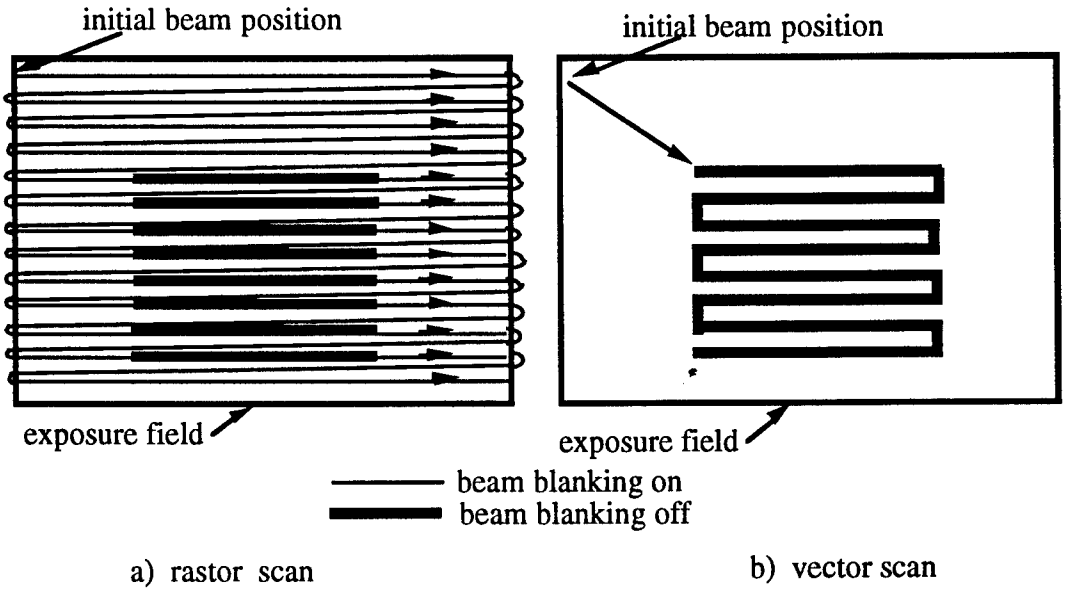


Figure 2.9. Illustration of (a) raster and (b) vector scan approaches.

The raster scan approach minimizes inductive delay effects in the scan coils except when the beam jumps from the end of a line to the beginning of the next, but this

is avoided by inserting an extra delay at the beginning of each new line. One drawback of this approach is that even the unexposed points are scanned, which slows down the exposure. The raster scan system used for this thesis work (designed by S.Y. Chou and built by J. Boetcher [48]) consists of a 12 bit digital hardware system with 12 bit digital to analog converters to generate the analog beam position signals. The system uses a 1 MHz clock and a 255 μsec delay at the beginning of each new scan line. Patterns are specified using a series of DIP switches. The system is capable of producing periodic arrays of rectilinear objects and has been used to define features as small as 10 nm wide metal lines with a 30 nm spacing on bulk GaAs using PMMA and lift-off (section 3.3).

A second, more flexible, computer controlled pattern generator has also been developed (by J. Boetcher, P.B. Fischer, and P. Gaard) which is a vector scan system (figure 2.9b). In this case, the beam is swept to the starting position of the vector to be exposed. After a delay comparable to the inductive delay of the scan coils, the vector is exposed as a sequence of pixel exposures. The particular implementation has the flexibility to write each vector using a different dose which makes proximity effect correction techniques possible. Furthermore, this technique does not require that unexposed points be scanned.

The vector scan pattern generator is a computer controlled system which consists of: a commercial CAD package to specify the exposure patterns, DesignCAD[49]; a custom computer program, Pattern Generator (designed by P. Gaard [50]), to read the DesignCAD output files, generate the exposure coordinates, and control data output to the hardware; and custom hardware (developed by J. Boetcher, P.B. Fischer, and P. Gaard [51]) designed to interface between the computer and the SEM. Arbitrary patterns of lines, rectangles, polygons, circles, arcs, and text can be exposed using this system. Further details can be found in appendix A. It is possible to achieve sub-50 nm interlevel

alignment accuracy with this system (section 3.3). Using this system, transistor gates, such as that shown in figure 2.10 have been routinely defined.

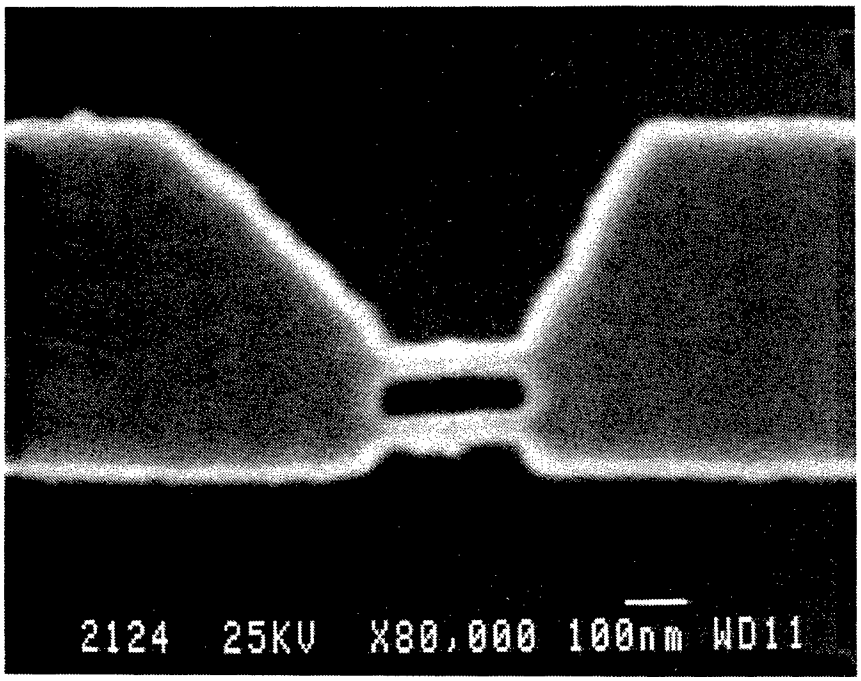


Figure 2.10. Scanning electron micrograph of a poly-silicon gate for a studying quantum effects using a field effect transistor. The gate is 575 nm long, and features a constriction with two bars, each 50 nm long, that are spaced by 60 nm. The gate was fabricated using the vector scan electron beam lithography system.

Chapter 3

10 nm Fabrication Techniques

3.1 Introduction

As a result of the improved semiconductor device performance and packing densities that are achieved by decreasing device sizes, many investigators are searching for new fabrication techniques to achieve 0.1 μm and sub-0.1 μm structures. The fabrication of sub-50 nm structures is the corner stone of this thesis. In this chapter, three nanostructure fabrication techniques capable of achieving 10 nm feature sizes are explored. Electron beam lithography using NanoStructure Laboratory's modified scanning electron microscope is a common denominator to the three techniques.

The first technique utilizes shadow evaporation of metals and a lift-off process to achieve metal lines spaced by distances as small as 10 nm (section 3.2).[52] Direct lift-off techniques have also been optimized to achieve 10 nm linewidths with only a 35 KeV beam (section 3.3).[53] The last 10 nm fabrication technique explored the use of reactive ion etching and subsequent wet etching to achieve pillars and ridges as small as 10 nm (section 3.4).[54]

3.2 Shadow Evaporation

3.2.1 Introduction

Fabrication of lateral dual-gate quantum-interference transistors requires not only that width of gate-metal lines be narrow, but also that separation of the two gates be small and uniform since the separation determines width of a quantum well, and that thickness of the gate-metal lines be large since it determines gate resistance and therefore high frequency performance of the devices [55,56]. Previously, 8 nm wide metal lines 10 nm apart and 10 nm thick have been fabricated on an ultra-thin carbon membrane using contamination resists, a high voltage, high resolution electron beam system, and reactive ion etching.[47] However, the finest metal lines with the smallest separation on a bulk GaAs substrate are 10 nm wide, 40 nm apart and 15 nm thick [45]. This section describes a process which can fabricate double 15 nm-wide metal lines 10 nm apart on a bulk GaAs substrate [52]. The pitch size of the double metal lines is 25 nm. This is a factor of 2 smaller than the previous smallest pitch size on bulk semiconductors. It is found that the width and spacing of the two lines are uniform over tens of microns. The method involves high resolution electron beam lithography, a single layer polymethyl methacrylate (PMMA) resist, double shadow-evaporations, and a lift-off process.

Although the shadow-evaporation technique has been used to fabricate small metal structures on a bulk substrate for many years, it was limited to cases where metals were shadow-evaporated from a fixed angle toward one sidewall of a trench structure [57-60]. Furthermore, a lift-off process was not used in cases where metals were shadow-evaporated on a resist step which has a relatively straight sidewall, since it was believed that metal on the sidewall would be continuously connected to the metal on top of the resist and therefore the lift-off would fail. In the novel process described in this section,

metals were shadow-evaporated twice from two nearly opposite angles toward both sidewalls of a resist trench. Moreover, a lift-off process is used to remove the metals on top of the resist, leaving two fine metal lines of a very small spacing on the substrate. Use of lift-off instead of reactive ion etching or ion milling can avoid ion bombardment of semiconductors and therefore preserves high electron mobility of semiconductor materials.

3.2.2 Fabrication Theory and Technique

The processing sequence for fabricating double metal lines is illustrated schematically in Fig 3.1. Bulk GaAs substrates were spin-coated with a single layer 950,000 molecular weight PMMA. While two thickness of PMMA were used, 38 nm and 70 nm, 70 nm thick resist was used in most of the experiments. After spinning the resist, samples were baked at 160 C for about 12 hours. Line patterns were exposed into resists using Nanostructure Laboratory's modified SEM electron beam lithography system with a beam energy of 35 KeV and various doses, and were developed in cellosove:methanol (3:7) developer. Metals (Ti/Au) were then evaporated onto the resists profiles at angles varying from normal incident to 36 degrees from the normal direction. For some samples metals were shadow-evaporated only once from a fixed angle toward one sidewall of resist trench; for other samples metals were shadow-evaporated twice from two nearly opposite angles toward both sidewalls of a resist trench. Thus two fine metal lines separated with a narrow gap are formed in the same resist trench. Finally, the metals on top of the resists were lifted off in acetone solvent.

In the double shadow-evaporations as depicted in Fig. 3.2, the linewidth of a metal line on a GaAs substrate from the first shadow-evaporation, LW_1, is given by $LW_1 = W - H \tan \theta_1$, where W is the width of the trench, H is the thickness of the resist, and θ_1

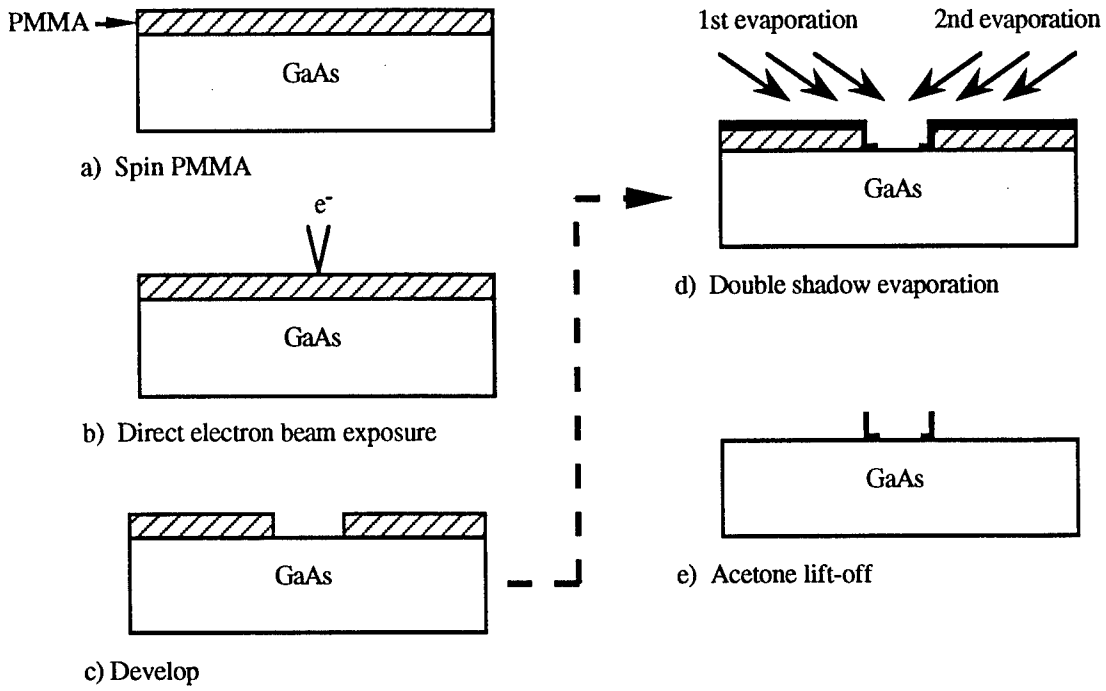


Figure 3.1. Basic steps for fabricating double fine metal gates with a small spacing on GaAs substrate.

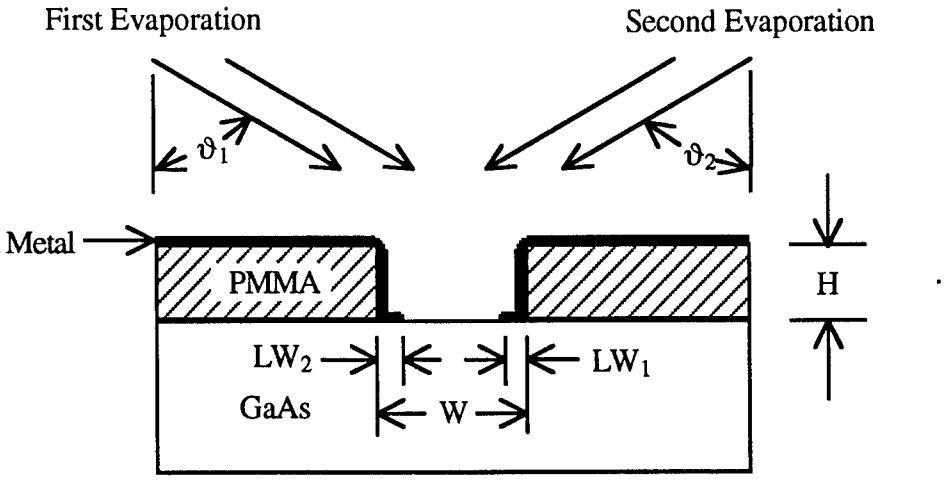


Figure 3.2. Schematically illustration of double shadow-evaporations of metals.

is the angle of incidence from the normal during the shadow-evaporation. Width of upper portion of the metal line is given by t $\sin\theta_1$, where t is the thickness of the metal if it is deposited from the normal. Linewidth from the second shadow-evaporation is given by $LW_2 = W - t \sin\theta_1 - H \tan\theta_2$, where θ_2 is the angle in the second shadow-evaporation. Clearly, in order to make linewidths of the two metal lines the same, the incident angle in the second evaporation should be slightly smaller than the first one. The thickness of metal lines fabricated in this way is approximately equal to the thickness of the resist. The important advantage of the double shadow-evaporations process is that the widths and the separation of two metal lines can be smaller than the resolution of resist, and yet thickness of metal lines--therefore the aspect ratio--can be very large, and the width and the separation are very uniform. These features are very desirable for metal gates in lateral dual-gates electron quantum-interference devices.

3.2.3 Results and Discussion

As the first step, we characterized linewidth of resist profiles written by electron beam lithography at different doses, by evaporating Ti/Au of a thickness of 15 nm/15 nm from normal incidence onto the substrate and lifting off the metals outside of the resist trenches in acetone.

The process was examined to determine if lift-off would work for metals that were evaporated from an angle toward a resist trench. Two identical samples were prepared, both having 70 nm thick PMMA on GaAs substrates. Trenches with widths ranging from 30 nm to 70 nm were made in the samples by electron beam lithography. One sample was evaporated with metal at a normal incidence and the other was evaporated with metal at the 36 degrees from the normal. Metals on the top of the resist were lifted off in acetone. For the 36 degree angle evaporation, no metal lines were left

after lift-off for trenches of width less than 50 nm, while a metal linewidth of 25 nm resulted from the 70 nm wide resist trench. The results from the shadow-evaporation is consistent with the calculations using the equations given in section II. Fig. 3.3 shows the metal lines resulting from the normal evaporation and the 36 degree angle evaporation of metal using a 70 nm wide resist trench. It is quite surprising that lift-off is successful even though the metals in the resist trenches were connected to the metals on top of the resist. Two possible reasons might contribute to this: it would be quite likely the sidewalls of the resist trenches are curved slightly and therefore the metals over the convex corners of the resist profile are thinner and weaker than other part of the metal film, or metal films deposited using an electron beam evaporator have a weak link at sharp convex corners.

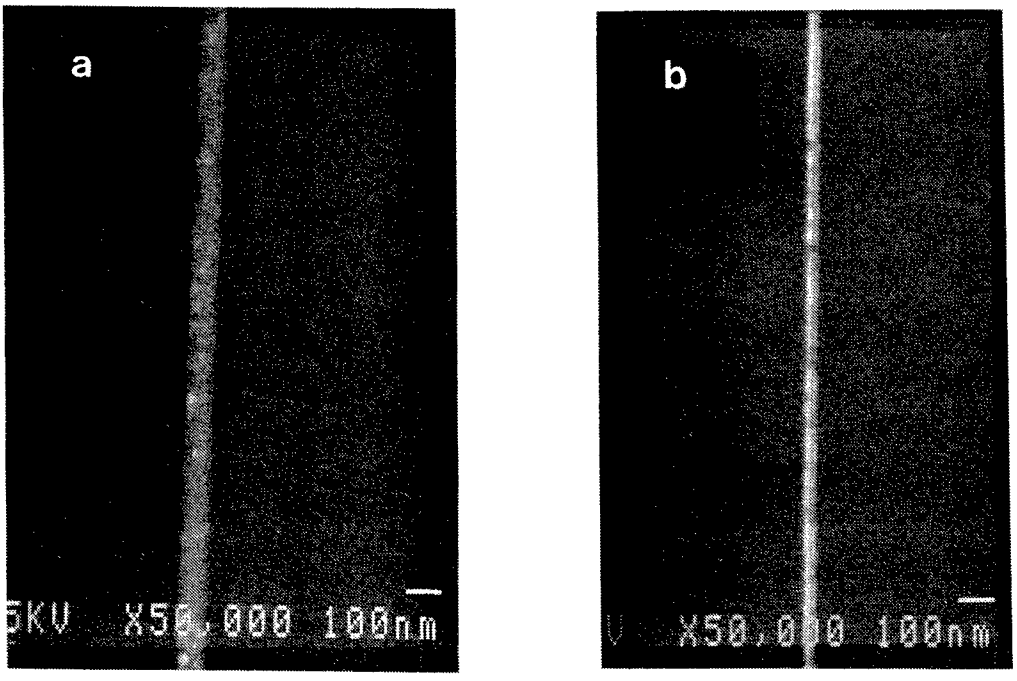


Figure. 3.3. The Ti/Au lines resulted from evaporation of Ti/Au from (a) the normal, and (b) 36 degrees angle, into a 70 nm-wide PMMA resist trench.

To achieve closely spaced double fine metal lines, metals were shadow-evaporated twice from two nearly opposite angles toward both sidewalls of a resist trench having a width of 40 nm. In the first evaporation, Ti/Au with a thickness 5 nm/5 nm were evaporated at an angle of 28 degrees. And in the second, Ti/Au with a thickness 5 nm/5 nm were evaporated from negative 26 degrees. The slightly smaller angle in the second evaporation takes into account the trench narrowing effect of the first shadow-evaporation to achieve almost equally spaced double lines. After lift-off, two 15 nm-wide Ti/Au metal lines of 10 nm apart are left on a GaAs substrate, as shown in Fig 3.4. The pitch size of the double metal lines is 25 nm. This is 2 times smaller than the previous smallest pitch size on bulk semiconductors. Examination using a SEM also showed that the linewidth and line spacing are uniform over tens of microns.

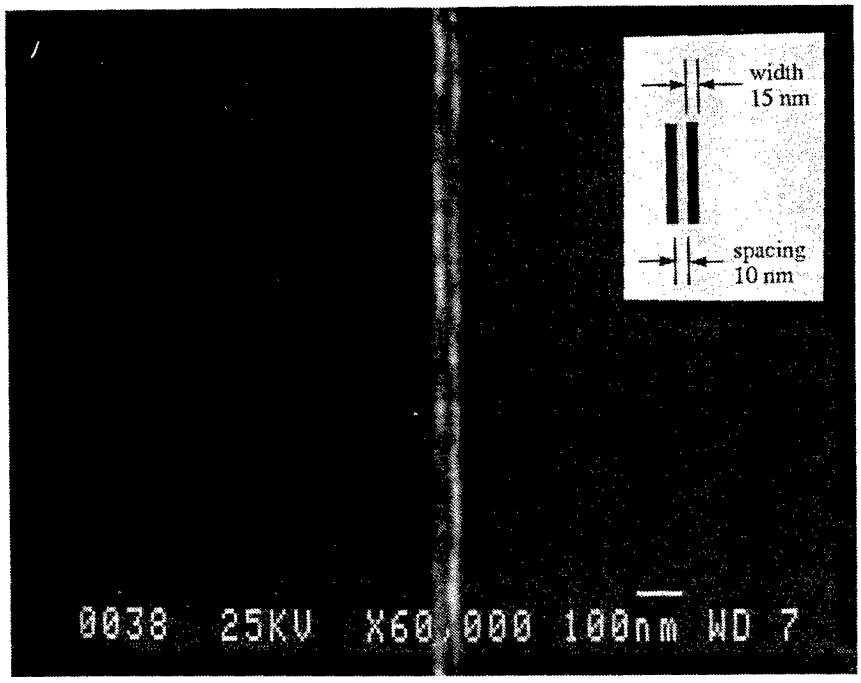


Figure 3.4. Double 15 nm-wide Ti/Au metal lines 10 nm apart on GaAs made by double shadow-evaporations onto a PMMA resist trenches of width of 40 nm. The evaporation was first from an angle 28 degrees from the normal, and then from negative 26 degrees. The Ti/Au thickness for each evaporation was 5 nm/5 nm. The PMMA resist was 70 nm thick.

Figure 3.5 shows two 15 nm-wide Ti/Au metal lines of 40 nm apart and 70 nm thick on GaAs made by double shadow-evaporations onto the sidewalls of a 70 nm wide resist trench. We also successfully applied this double shadow-evaporation technique to thinner (37.5 nm) PMMA resist. Figure 3.6 shows double 17.5 nm-wide Ti/Au metal lines 15 nm apart on GaAs made by double shadow-evaporations. The Ti/Au thickness for each evaporation was 10 nm, and the opening of PMMA trench was 50 nm wide.

Experiments have been repeated several times and results were consistent. To further investigate linewidth, spacing and straightness of the metal lines, crossection SEM examination is needed.

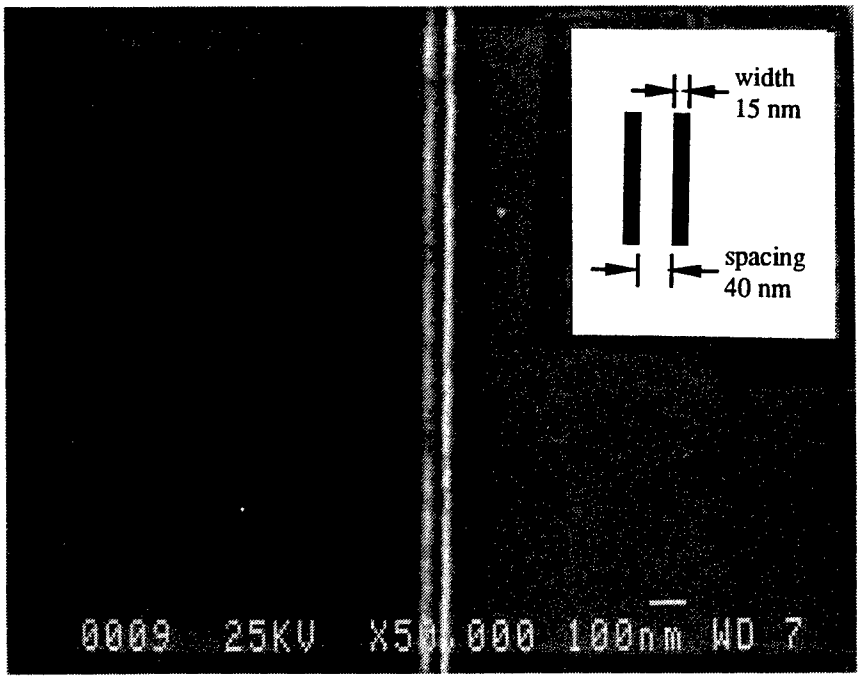


Figure 3.5. Double 15 nm-wide Ti/Au metal lines 40 nm apart on GaAs made by two shadow-evaporations. The opening of PMMA trench was 70 nm wide, and the thickness of the resist was 70 nm.

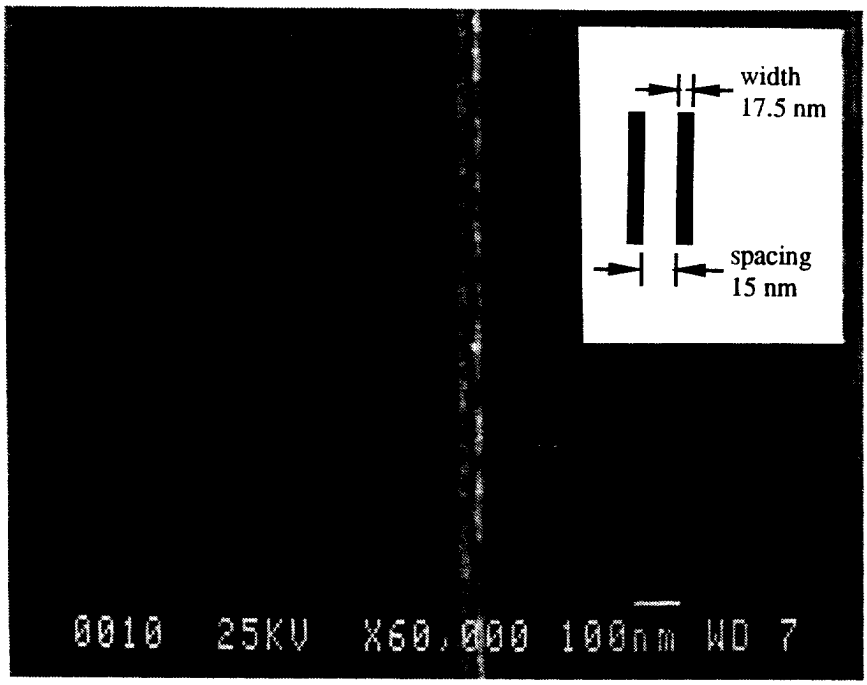


Figure 3.6. Double 17.5 nm-wide Ti/Au metal lines 15 nm apart on GaAs made by two shadow-evaporations. The Ti/Au thickness for each evaporation was 10 nm. The opening of PMMA trench was 50 nm wide and the resist was 37.5 nm thick.

3.3 10 nm Electron Beam Lithography and Sub-50 nm Overlay Accuracy

3.3.1 Introduction

The desire to study quantization effects and high-speed capabilities of semiconductor devices has motivated research on the fabrication of 10 nm lateral structures. For example, lateral quantum effect devices require ultra-small gate geometry [61], and metal-semiconductor-metal photodetectors require extremely dense patterns of

very fine interdigitated metal fingers for high performance.[62] The lithography for some novel semiconductor devices requires not only high resolution, but also high overlay accuracy. Modified SEMs are ideal for nano-fabrication and nano-device research due to their high resolution, high flexibility, and low cost, but offer no direct means for high-accuracy multi-level overlay.

Previously, modified SEMs have been used to produce 10 nm wide isolated lines and gratings of 40 nm period with 12 nm linewidth on membranes [16], as well as 10 nm wide isolated lines and gratings of 40 nm period with 10 nm linewidths on bulk GaAs substrates using a 250 keV beam and chemically assisted ion beam etching [63]. However, little work has been reported on ultra-high overlay accuracy in multi-level e-beam lithography using a modified SEM.

This section presents the study of lithographic resolution and overlay capability using Nanostructure Laboratory's modified SEM EBL system operated at 35 kV. 10 nm metal features, either isolated or periodic with periods as small as 40 nm, have been consistently achieved on bulk GaAs substrates. Sub-50 nm overlay accuracy has also been accomplished using a lift-off technique with polymethyl methacrylate (PMMA) resists.

3.3.2 Fabrication Theory and Technique

In order to achieve ultra-small structures in PMMA, the exposure of the resist by backscattered and laterally scattered electrons must be minimized. This can be accomplished by using thin resists and minimizing the exposure area to areas smaller than the backscattered electron range. In this experiment, GaAs wafers were coated with a 45 nm thick layer of 950 K PMMA by spinning a 1.6% solution of 950 K PMMA (in

chlorobenzene) at 6.0 krpm for 60 sec. The samples were then baked for 12 hrs at 165 °C to achieve the highest possible contrast.[64]

Exposures were performed with an accelerating voltage of 35 kV, a beam current of 4.5 pA, and a corresponding beam diameter of about 4 nm. In order to achieve densely packed, ultra-small features, a high contrast developer-resist system must be used. When a high contrast system is used, slight variations in the exposure dose result in large changes in resist thicknesses. Development was done at 23 °C using 2-ethoxyethanol:methanol (3:7) for 7 sec, methanol for 10 sec, and isopropanol for 30 sec.

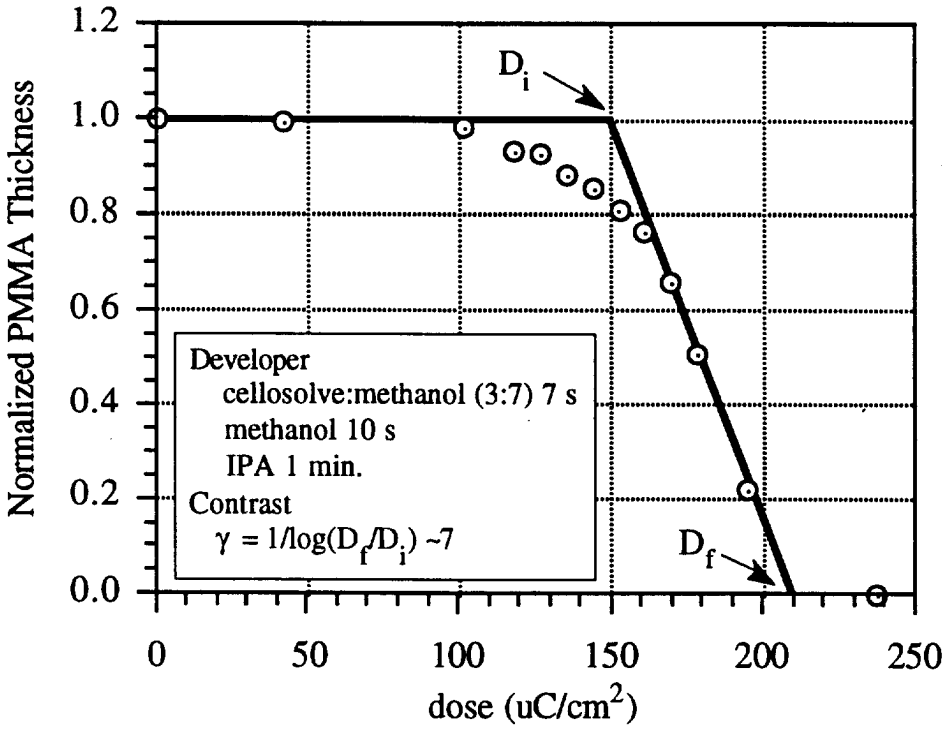


Figure 3.7. Contrast calibration data for 950 K PMMA using 2-ethoxyethanol:methanol (3:7) for 7 sec.

The contrast of this developer was measured in order to verify its suitability (this experiment was performed by B. Guibord and P. Krauss). To determine the contrast of this resist/developer system, samples were prepared with 0.5 μm of 950 K PMMA by spin coating and baking at 165 °C for 10 hours. 15 x 15 μm^2 areas were then exposed

with a 35 keV beam using a range of doses. After development, the depth was measured using a Digital Instruments Nanoscope III atomic force microscope. The data in figure 3.7 demonstrates that the contrast for this process is 7, which is sufficient for high resolution work.

After development, metals were deposited by e-beam evaporation. Lift-off was performed by alternately soaking in warm acetone and spraying with a pressurized acetone jet.

To use a modified SEM to achieve high overlay accuracy, we selected a writing field size of 12 x 9.3 μm^2, corresponding to a magnification of 10,000. The writing field is further divided into (a) the "device" area of 9 x 9.3 μm^2 located in the middle of the field, and (b) two alignment areas of 1.5 x 9.3 μm^2 located on each side of the "device" area.

In the first level of the multi-level e-beam lithography, test patterns consisting of paired nanoscale metal squares with various separations were defined in the central 9 x 9.3 μm^2 "device" area by a lift-off process, and 4.5 μm x 0.5 μm metal alignment marks for the second level e-beam lithography were defined in the alignment areas. When gold was used for the alignment marks, a total metal thickness of 50 nm was sufficient for later alignment.

As illustrated in figure 3.8, in the second level of lithography, rectangular viewing windows were opened in the alignment area. The windows have a size which is just 0.1 μm larger than each edge of the alignment mark produced in the first level of the lithography. For perfect alignment, each alignment mark from the first level should be centered in each viewing window. The alignment marks were detected using a backscattered electron detector. Coarse alignment was performed using the SEM stage micrometers; final alignment was achieved using electronic image shifts and electronic rotation.

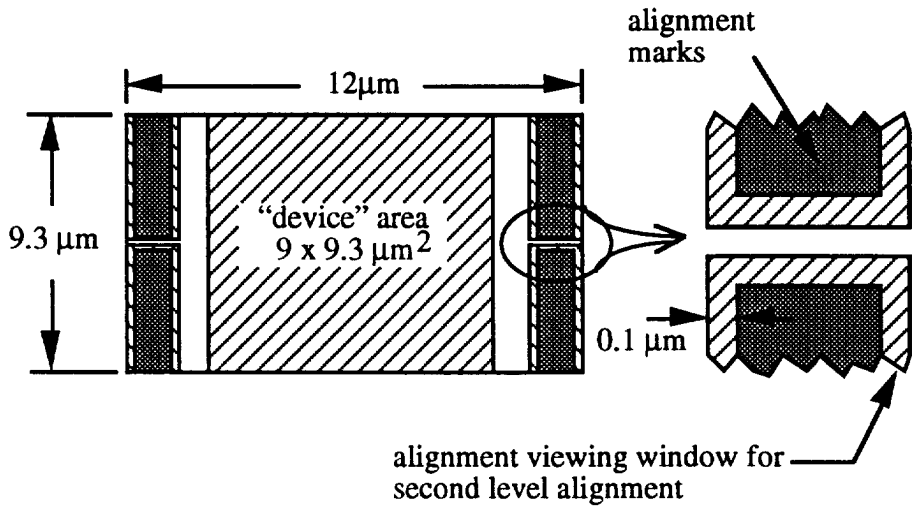


Figure 3.8. Schematic of the alignment scheme.

The "device" area was blanked during the alignment. Even so, the resist in the device area is indirectly exposed by backscattered electrons from the alignment areas since the alignment windows are only 0.8 μm away from the device area. To minimize such proximity effects, the pixel resolution was reduced to 2^{10} x 2^{10}, to reduce the exposure intensity while still maintaining sufficient resolution for the alignment. The corresponding direct exposure dose was an order of magnitude lower than the minimum dose required to expose PMMA.

3.3.3 Results and Discussion

Both isolated and densely spaced patterns with 10 nm features have been obtained. Figure 3.9 shows a scanning electron micrograph of a 40 nm period grating with 10 nm linewidths on bulk GaAs. In this particular example only 3.5 nm of Ni and 4 nm of Au have been used, but lift-off is still possible with total thicknesses of at least 15 nm. The dose for the grating was 0.9 nC/cm and must be carefully controlled. The

exposed grating lines were 2 μm long and lift-off of metal lines was successful for areas as wide as 1.3 μm. Gratings with a smaller period did not lift-off properly.

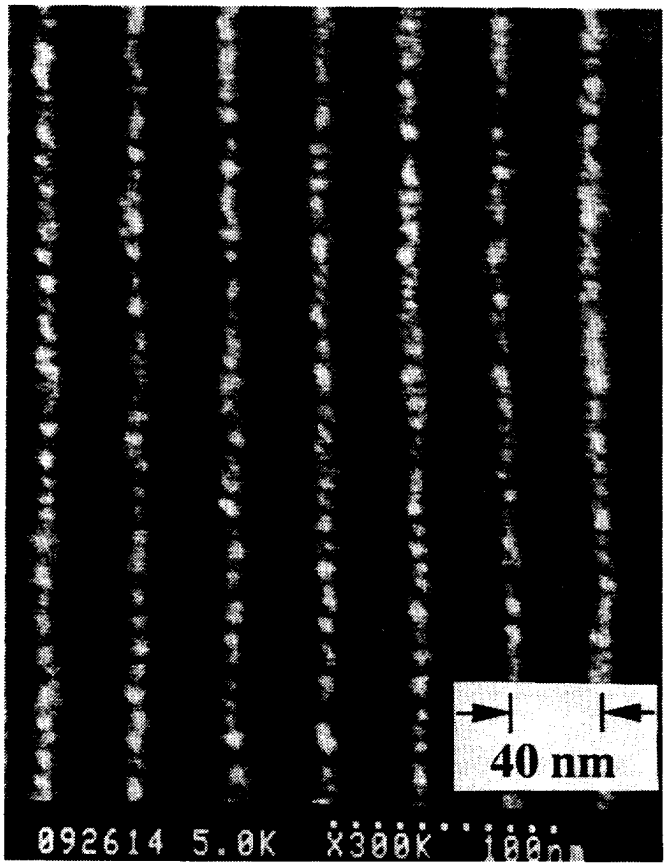


Figure 3.9. Scanning electron micrograph of a 40 nm period Ni/Au grating with 10 nm linewidth.

Figure 3.10 shows a scanning electron micrograph of a Ni/Au (7 nm/8 nm) constricted gate with a gap of 10 nm and a gate length of 330 nm on bulk GaAs. The constricted gate was exposed with a dose of 480 $\mu C/cm^2$. This demonstrates that not only 10 nm lines but also 10 nm spaces can be achieved using a modified SEM operated at 35 kV with PMMA lift-off techniques. We believe that the ability to repeatedly achieve such 10 nm results using a 35 kV exposure and direct lift-off techniques is due in part to the stability of our electronic system and the lift-off techniques that have been employed.

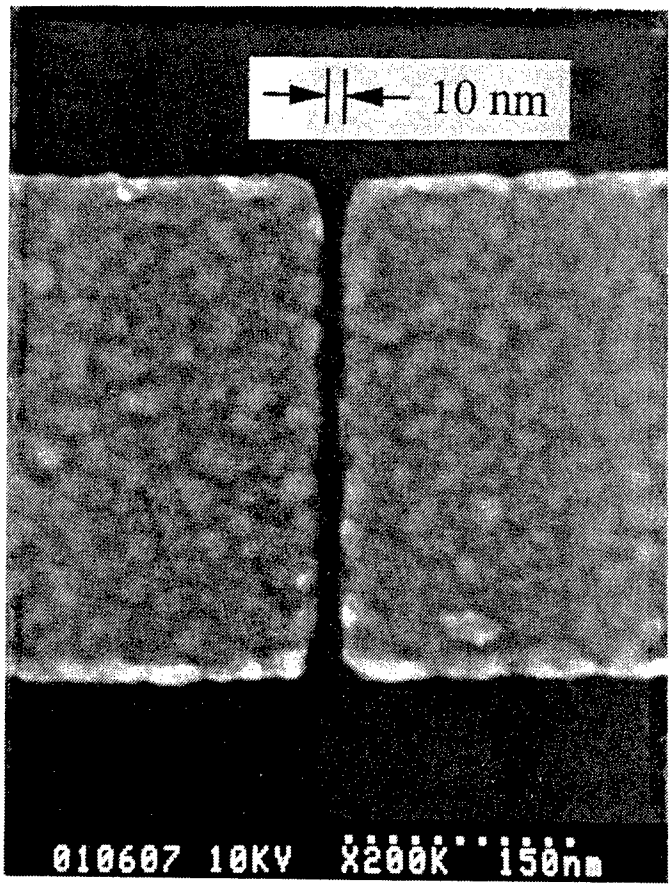


Figure 3.10. Scanning electron micrograph of a Ni/Au constricted gate structure with a gap of 10 nm and a length of 330 nm, both are on bulk GaAs.

To check the overlay accuracy of the second level of the lithography, paired metal lines of nanoscale linewidth were defined in the "device" area, after alignment, exposure and lift-off. With perfect alignment, one end of each metal line in the second level should lay in the center of the squares placed by the first level. Figure 3.11 is a scanning electron micrograph showing typical results. The four unintended dots were due to a software error in the second level of lithography. Figure 3.12 is the summary of 19 alignment tests, indicating that the standard deviation of the overlay accuracy is 17 nm. Both x and y results have been superimposed on the same plot due to the limited number

of data points. The results show that high overlay accuracy can be achieved with a modified SEM.

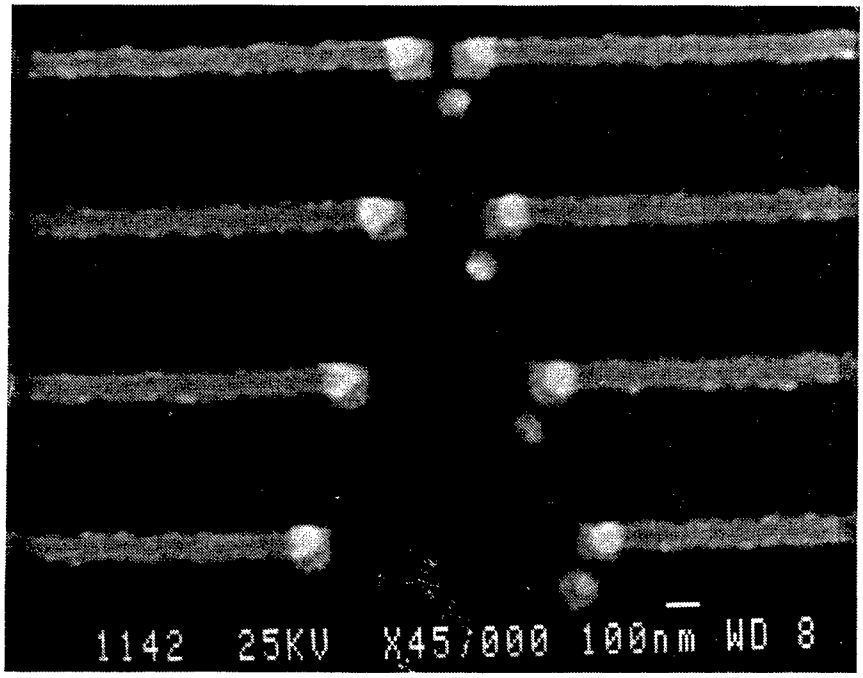


Figure 3.11. Scanning electron micrograph of two e-beam lithography levels with 20 nm accuracy.

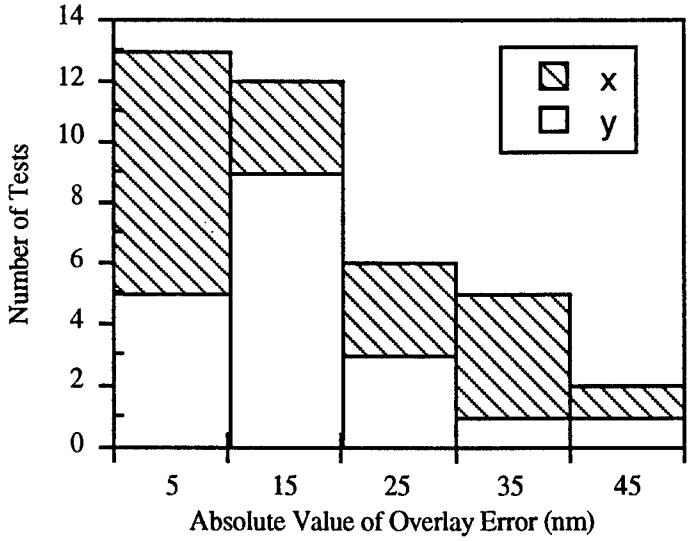


Figure 3.12. Histogram showing the overlay accuracy in the x and y directions vs. the number of tests. The standard deviation is 17 nm.

3.4 10 nm Si Structures Using Reactive Ion Etching and Subsequent HF Etching

3.4.1 Introduction

The ability to etch nanoscale features in Si is of great interest for trench isolation [65] and trench capacitors[66] in very large scale integrated circuits, and for novel quantum effect Si devices. Techniques such as wet chemical etching are not suitable for etching nanoscale, high aspect-ratio Si structures due to undercutting of the mask and sloped sidewalls. Chlorine based reactive ion etching (RIE), however, is well suited for etching nanoscale Si features with good control of undercutting and etch profiles.[67]

Previous reports have addressed various aspects of Cl-based RIE of Si such as: the role of chemistry in highly anisotropic Si trench etching [65], elimination of mask undercutting[67], mechanisms leading to RIE etch lag [68], and the relationship between the RIE process and physical and electrical trench capacitor characteristics[69].

This section focuses on the minimum achievable feature sizes in Si using Cl-based RIE. With an optimized composition of Cl_2 and $SiCl_4$ sub-50 nm diameter pillars 500 nm high at a pitch of 100 nm, and gratings with a spacing of 30 nm and a linewidth of 50 nm which are 500 nm deep can be readily and repeatedly achieved. One specific application of this controlled approach to Si nanostructure fabrication, the investigation of light emission from silicon, will be discussed in section 4.4.

3.4.2 Sub-50 nm Si Structures Using Reactive Ion Etching

The starting Si wafers, *p*-type with a 10 Ω•cm resistivity and a (100) orientation, were first cleaned using H_2SO_4:H_2O_2:H_2O (1:1:5) for 10 min at 120 °C, DI rinse for 5 min, and buffered HF:H_2O (1:9) for 30 sec. Then a layer of 950 K molecular weight

poly methyl methacrylate (PMMA), 70 nm thick, was spun on the sample and baked at 165 °C for 12 hours. Arrays of dots and lines were exposed in the PMMA using Nanostructure Laboratory's modified JEOL-840A SEM and developed in a mixture of 2-ethoxyethanol and methanol. Cr, 50 nm thick, was then deposited via electron beam evaporation at a rate of 0.1 nm/sec. A lift-off process left arrays of Cr dots and lines on the Si wafers, which were used as the mask for RIE. Figure 3.13 shows 30 nm thick metal dots with 25 nm diameters and 25 nm spacings on a bulk semiconductor substrate that were fabricated using this technique. Final surface cleaning, prior to RIE, consisted of an O_2 plasma etch and an HF dip.

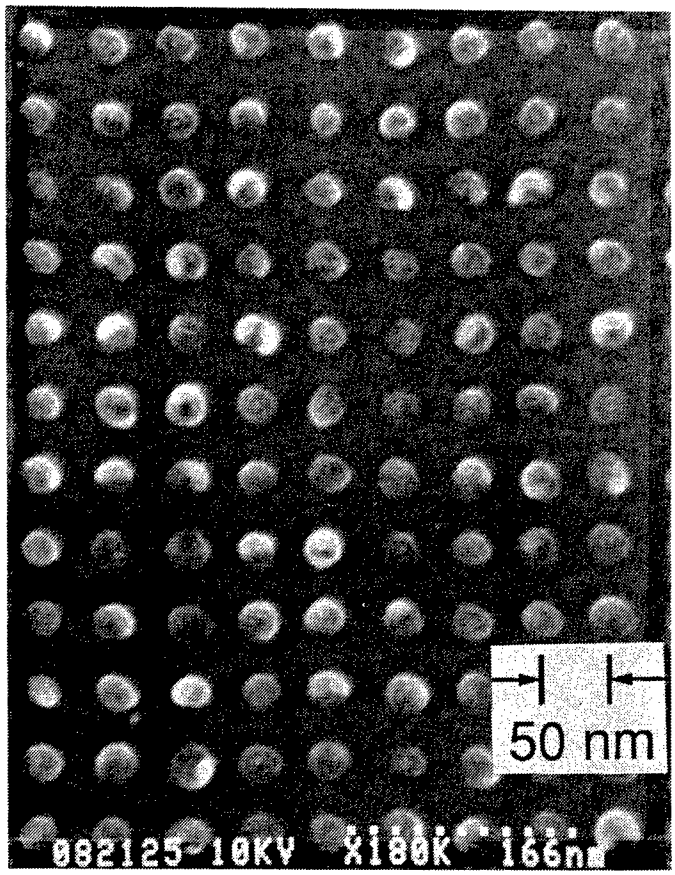


Figure 3.13. Array of Ti/Au dots with 25 nm diameter and 25 nm spacing on a bulk semiconductor substrate.

RIE was performed using a Plasma-Therm parallel plate RIE system operated at 13.56 MHz. A variety of recipes consisting of Cl_2, $SiCl_4$, and He gases were tested. Chlorine was used because it has been shown to produce vertical sidewalls[67] due to the ion assisted etching mechanism[70], but has the drawback of producing trenches in the bottom corners. $SiCl_4$ and He were added to control trench formation by simultaneous re-deposition[71]. Prior to etching the chamber was always cleaned for 10 min with an Ar plasma, and then pre-conditioned for 10 min using the same etching recipe that was to be used. After inserting the sample, the chamber was pumped below 2×10^{-5} torr.

All samples were etched with the same Cl_2 and $SiCl_4$ flow rates, 76.6 and 13.3 sccm respectively, a power density of 0.32 W/cm^2, and a pressure of 40 mtorr. These parameters were found to produce the sidewall profiles necessary for high aspect ratio nanoscale features without trenching at the bottom corners. The He flow rate was varied from 0 to 60 sccm to further optimize the etch parameters, but no change in profile was observed and He was not included in the final recipe. After etching, the samples were analyzed using high-resolution scanning electron microscopy.

Previously, when etching with Cl_2 chemistries, the formation of roughened Si surfaces, "black Si[1]", was reported.[67] The appearance of "black Si" has been attributed to the presence of SiO_2 micro-masks. Maluf *et al*[72], also using mixtures of Cl_2, $SiCl_4$, and He, only observed "black Si" with high He flow rates. We found that proper cleaning of the sample and chamber resulted in relatively smooth surfaces with profile variations of 10 - 30 nm.

Figure 3.14 shows an array of etched Si pillars having diameters of about 40 nm, a period of 100 nm, and a height of 520 nm. The hemispherical Cr dots were not removed for this picture; no undercutting of the mask or trenching at the bottom corners has

[1]Black silicon refers to reactive ion etched silicon surfaces on which pillars are formed due to contamination during etching.

occurred. Figure 3.15 shows 50 nm wide Si ridges spaced by 30 nm and 520 nm high. The Cr mask has been left in place to verify that no undercutting of the mask occurred during etching. In both cases the aspect ratio is in excess of 10. Si pillars, trenches and ridges which are, to the best of our knowledge, smaller than that previously reported have been achieved.

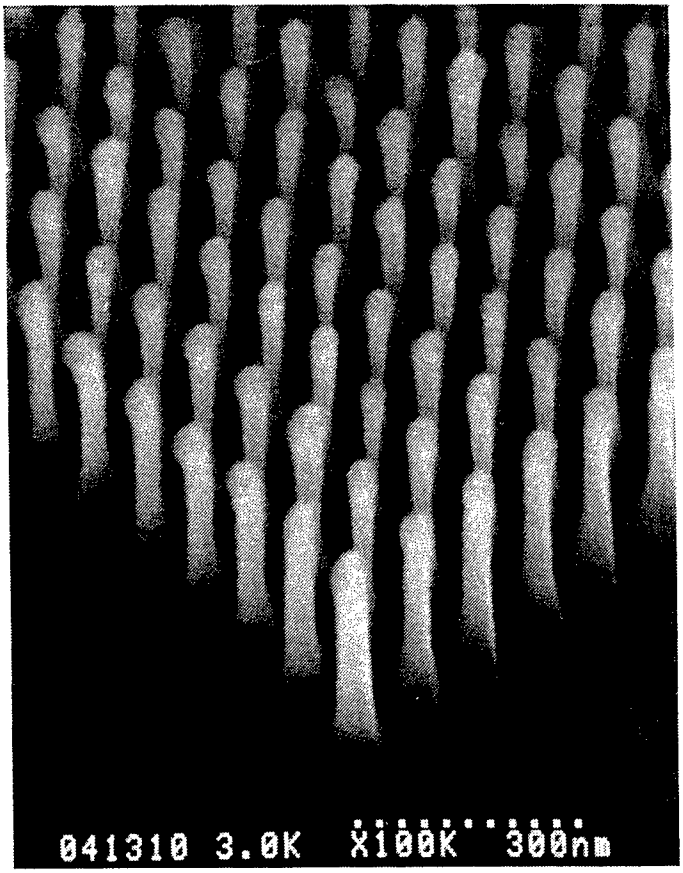


Figure 3.14. Scanning electron micrograph of sub-40 nm diameter Si pillars with a period of 100 nm and height of 520 nm. Sample tilt is 40°.

It is clear that highly uniform sub-50 nm features with near vertical profiles can be achieved using this technique. These results suggest that the ultimate limit on etched feature size is determined by the ability to pattern nanoscale masks and the fundamental mechanical stability of Si, rather than by the etching mechanism itself.

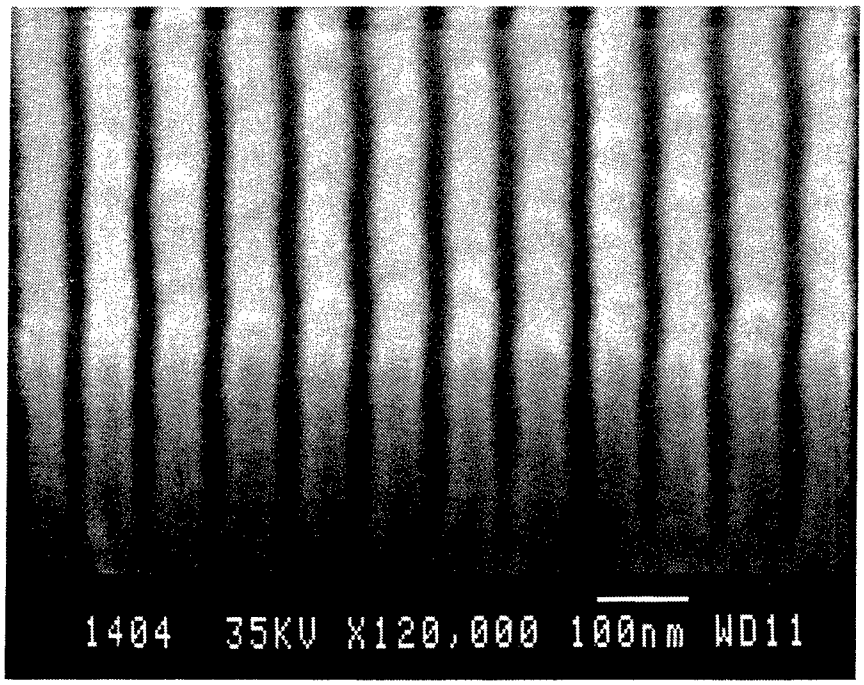


Figure 3.15. Scanning electron micrograph of 50 nm wide Si ridges spaced by 30 nm with a height of 520 nm. Sample tilt is 40°.

3.4.3 Subsequent Size Reduction Using HF Etching

Previously, oxidation techniques have been employed to further reduce the size of silicon pillars for fabricating field emitters and microsensors [73] and for studying luminescence.[74] The oxidation process has two drawbacks. First, it is a stress dependent process, therefore is non-uniform and significantly changes the original shape of the pillars. Second, it is a high temperature process which could pose problems in some applications.

Here, a different approach to fabricating free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15 was utilized. The 10 nm Si pillar fabrication process consists of three main steps: etch mask definition using electron beam lithography (described in section 3.3), RIE (as described in section 3.4.2), and HF etching to reduce the size of the pillars. HF etching offers several advantages. First, HF etching is a relatively stress independent process and therefore preserves the original shape of the structure. Secondly, it is a room temperature process, making it a much more versatile process than high temperature oxidation. Thirdly, it has a very controllable etch rate, ~1.9 nm/hour. And finally, it can remove RIE damage and passivate the Si surface.

Chlorine-based RIE was used to transform sub-50 nm diameter Cr dot patterns into Si pillars as described in section 3.4.2. The last step of the fabrication process utilizes aqueous HF acid etching (49%) to further reduce the size of the pillars and passivate the Si surface.[75]

The effect of HF etching on pillar geometry was systematically studied. Figure 3.16 shows scanning electron micrographs of pillars at different stages of the etching process. Figure 3.16a shows a pillar just after RIE with the Cr mask still in place but before any HF etching. The pillar is approximately 45 nm in diameter and about 450 nm tall. The top of the pillar widens slightly due to sidewall deposition during RIE which has been observed before and can be readily removed by HF.[71] The bottom of the pillar widens out to form a pedestal due to the chosen RIE parameters. Figure 3.16b shows a pillar after removing the Cr and etching in HF for 4 hours. The mushroom cap has been removed, resulting in a uniform Si pillar 25 nm in diameter. The overall height of this pillar is now about 350 nm. Figure 3.16c shows a pillar after a total of 8 hrs in HF. The pillar has been transformed into a nanoscale filament with a uniform diameter of about 10 nm and a length of 150 nm on top of a pedestal. The overall height is about 350

nm. It is possible to further reduce the size below 10 nm using this technique, but free standing Si pillars may become mechanically unstable at such small sizes. The array of pillars used for this study has an area of 34 μm x 26 μm and a period of 0.5 μm.

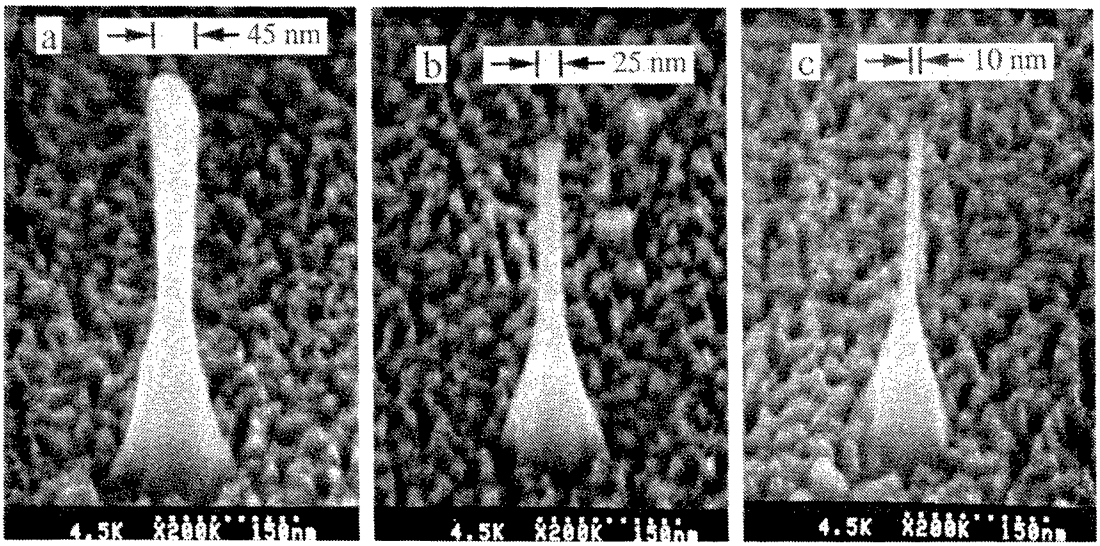


Figure 3.16. Reduction of Si pillar diameters using HF etching: (a) No HF etching. The Cr mask is still in place. The pillar is 45 nm in diameter and 450 nm tall. (b) After removal of Cr and etching in HF for 3 hours. The pillar is 25 nm in diameter and 350 nm tall. (c) After a total of 7 hrs in HF. The pillar is 10 nm in diameter and 350 nm tall. The top of the pillar is very uniform in width and has an aspect-ratio in excess of 15.

It should be pointed out that the pillars shown in Fig. 3.16 are different pillars from the same array to avoid problems caused by contamination during the SEM analysis. However, Fig. 3.16 should represent the actual evolution of a pillar during the processing, since the diameter of the pillars from the same array was found to be uniform to within about 6 nm as described in section 3.4.4.

The silicon pillar etch rate in HF was calibrated using a high-resolution low voltage SEM before and at intervals after HF etching. To avoid complications of sample modification during SEM analysis, only virgin pillars were sampled at each time interval. It was found that HF etched Si pillar diameters at a constant rate of ~3.9 nm/hr

(corresponding to a single-sided etch rate of ~1.9 nm/hr), as shown in figure 3.17. The results demonstrate that the HF etching process is very controllable. The error bars in Fig. 3.17 come from the variation of the Cr masks.

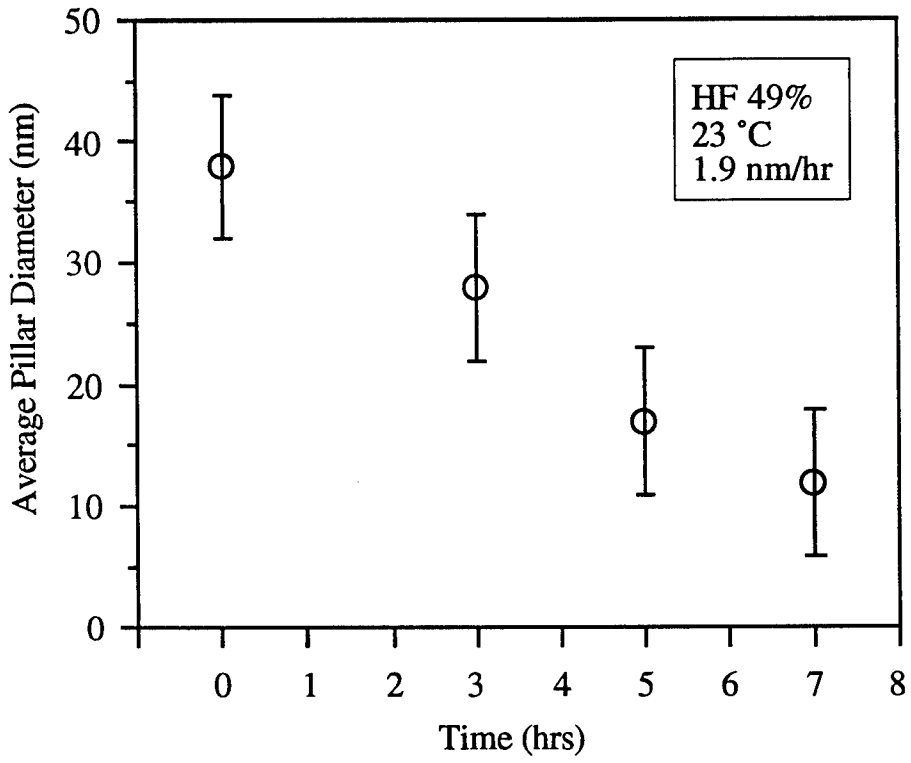


Figure 3.17 Change in diameter with respect to time. The pillar diameters decrease at a rate of 3.8 nm/hr. The error bars arise from variations of the Cr masks.

3.4.4 Uniformity

The uniformity of this fabrication process was also studied. To determine the uniformity of the first step, the Cr mask definition, an array of Cr dots with a period of 500 nm was examined using an atomic force microscope (AFM). Such a large period was used to avoid the effects of the AFM tip size. A histogram of the dot diameters from a random sample of 187 dots (Fig. 3.18) shows that the average diameter of the dots is 57 nm with a standard deviation of 6.5 nm. The deviation in dot diameters most likely

comes from noise in the beam deflection system. For the given exposure conditions, a beam deflection noise of 6.5 nm would translate to 3.6 mV of electronic noise. The pattern generator used for this project has a noise output of about 2 mV, and the SEM electronics could likely contribute an additional 1.6 mV of noise to the beam deflection signal. Another factor that might affect the variation in dot diameters is statistical variations of exposure dose, but this has been ruled out because the exposure dose is well above the threshold, and because of the relatively large number of electrons used at each point (>$6x10^4$). Proximity effects could be another factor that causes variations in dot diameters, but a detailed analysis indicates that the effect of proximity is rather negligible for the 500 nm period arrays exposed under the given conditions.

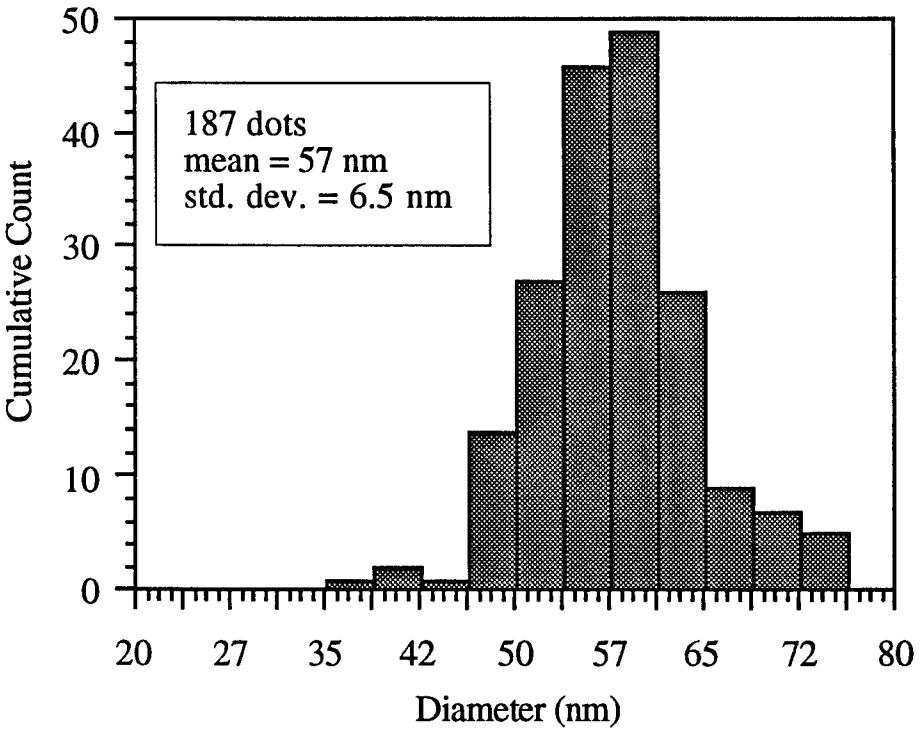


Figure 3.18. Histogram of dot diameters from a 500 nm period test array.

However, proximity effects are not negligible for denser arrays. For example, to achieve the same dot diameter the required exposure dose in the center of a large area array of 150 nm period is 50% lower than that for a 500 nm period array. In the 150 nm

period array, dots that are within the backscattered electron range (about 5-6 μm for the given conditions) from the edges of the exposure area will receive fewer backscattered electrons than those in the central region and hence have smaller diameters. This will tend to increase the variations of dot diameters. However, for an exposure area of 400 x 650 μm^2, 95% of the total exposure area is not affected by the edge effects and has uniform pillars diameters.

To determine the combined uniformity of the RIE and HF etching steps, a Si sample was patterned with arrays of Cr dots and etched using RIE and HF for 5 hours. Subsequent measurements using a high resolution low voltage SEM of 23 pillars determined that the standard deviation of pillar diameters was 5.7 nm. This deviation is very close to 6.5 nm -- the standard deviation of the mask definition step -- indicating that the RIE and HF processes are uniform and the definition of Cr masks is the factor limiting the uniformity of this process.

3.5 Summary

Three nanostructure fabrication techniques capable of achieving 10 nm features were discussed. We have demonstrated that by opening a 40 nm wide trench in a 70 nm thick single layer of PMMA on GaAs using e-beam lithography, and by double shadow-evaporations and lift-off, two metal lines of 15 nm wide and 10 nm apart were fabricated on thick GaAs substrate. The pitch size of the double metal lines is 25 nm. This is a factor of 2 smaller than the previous smallest pitch size on bulk semiconductors. We have found that the width and spacing of the two lines fabricated using this method are uniform over tens of microns. We also have found that metals deposited by shadow-

evaporation can be successfully lifted off . This suggests that using this method, metal lines with even finer linewidth (<15 nm) can be achieved on bulk semiconductor substrate. We believe this method is useful for fabricating various lateral dual-gate quantum-interference transistors.

In addition, a modified SEM has been used to fabricate ultra-small features and achieve ultra-high overlay accuracy using optimized lithography coupled with normal incidence evaporation and lift-off techniques. By using thin resists and minimizing exposure areas, gratings of 10 nm wide lines 30 nm apart, and quantum field-effect-transistor gates with 10 nm wide gaps over 300 nm long have been repeatedly defined on bulk GaAs substrates using a modified SEM operated at 35 keV, and lift-off of Ni/Au. Sub-50 nm overlay accuracy in multi-level e-beam lithography has also been achieved using the same modified SEM. The results demonstrate the effectiveness of modified SEMs in cutting-edge nanoscale device research in general, and the resolution that can be achieved using NanoStructure Laboratory's modified SEM lithography system in particular.

Lastly, a novel technique for fabricating free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15 using electron beam lithography, RIE, and subsequent HF wet etching was also presented. Using high resolution electron beam lithography and RIE with Cl_2 and $SiCl_4$ gases we have etched sub-50 nm Si pillars, trenches and ridges with aspect ratios greater than 10. These are among the smallest features fabricated using these techniques. We believe that the size of these Si features etched with the recipe described here is limited by the size of the etching mask, rather than the etching process itself. The uniformity of this fabrication process was investigated. It was found that the standard deviation of pillar diameters can be controlled to within $\pm$ 6 nm and is limited by the etch mask definition.

Si pillars were subsequently further reduced in size using HF etching. HF etching offers several advantages: it is a relatively stress independent process and therefore preserves the original shape of the structure; it is a room temperature process, making it a much more versatile process then high temperature oxidation; it has a very controllable etch rate (1.9 nm/hr); and it can remove RIE damage and passivate the Si surface.

Chapter 4

Applications of Nanostructure Engineering

4.1 Introduction

In this chapter, four nanofabrication applications demonstrating the utility of nanofabrication techniques are described. EBL was applied to the creation of ultra-fast metal-semiconductor-metal (MSM) photodetectors. The fastest MSM photodetectors reported to date have been achieved (section 4.2).[62,76,77] EBL was also applied to the creation of quantum effect transistors. Conductance quantization was observed in a point contact device (section 4.3). Nanofabrication techniques are also applied to evaluate the quantum confinement model that has been suggested to explain light emission from porous silicon (section 4.4).[54] Photoluminescence has been observed from an ordered array of nanosculpted silicon pillars. Finally, nanofabrication techniques were used to minimize the effect of tip volume on resultant magnetic force microscope images using two distinct approaches (section 4.5). In the first approach, tip effects are removed from MFM images by deconvolving the impulse response of the tip from the MFM image.[78] In the second approach, tip effects are removed from MFM images by minimizing the magnetic tip volume in the first place.[79]

4.2 500 GHz Metal-Semiconductor-Metal Photodetectors

This section describes the application of nanofabrication techniques to metal-semiconductor-metal photodetectors (MSM PDs) on high quality GaAs. Nanoscale finger spacing was utilized to decrease the transit time and increase detector speed. Detectors with finger spacings and widths as small as 25 nm have been created.[62,76] Previously, the fastest transit-time-limited GaAs MSM PD had a finger width of 0.75 μm and finger spacing of 0.5 μm, an impulse response of 4.8 ps full width at half maximum (FWHM), and a 3-dB bandwidth of 105 GHz.[80] By decreasing the finger width and spacing to 100 nm, an impulse response of 1.5 ps full width at half maximum (FWHM), and a 3-dB bandwidth of 300 GHz was obtained.[81]

4.2.1 Scaling Rules - Why Smaller is Better

Metal-semiconductor-metal photodetectors (MSM PDs) are very attractive for many optoelectronic applications, such as optical communication, future high-speed chip-to-chip connection because of their high sensitivity-bandwidth product and compatibility with large-scale planar integrated circuit (IC) technology. A MSM PD consists of interdigitated metal fingers on a semiconductor, and it detects photons by collecting electric signals generated by photoexcited electrons and holes in the semiconductor which drift under the electrical field applied between the fingers (Fig. 4.1).

MSM PDs can be classified according to whether their speed is intrinsically limited by the carrier transit time between the fingers or the carrier recombination time. Certainly, the speed of the detector will be limited by the RC time constant if it is larger than the transit time or the recombination time. Usually, transit-time-limited detectors

are fabricated on high-quality semiconductors and have a sensitivity several orders of magnitude higher than that of recombination-time-limited MSM PDs. Furthermore, their fabrication technology is very compatible to field effect transistor (FET) fabrication. However, in the past, the transit-time-limited MSM PDs generally were much slower than the recombination-time-limited MSM PDs, because it used to be difficult to make the finger spacing small. In the recombination-time-limited MSM PDs, shorter recombination time and therefore higher speed are achieved through introducing high-density recombination centers into semiconductor that drastically lower sensitivity and make their fabrication less compatible with FET IC fabrication.

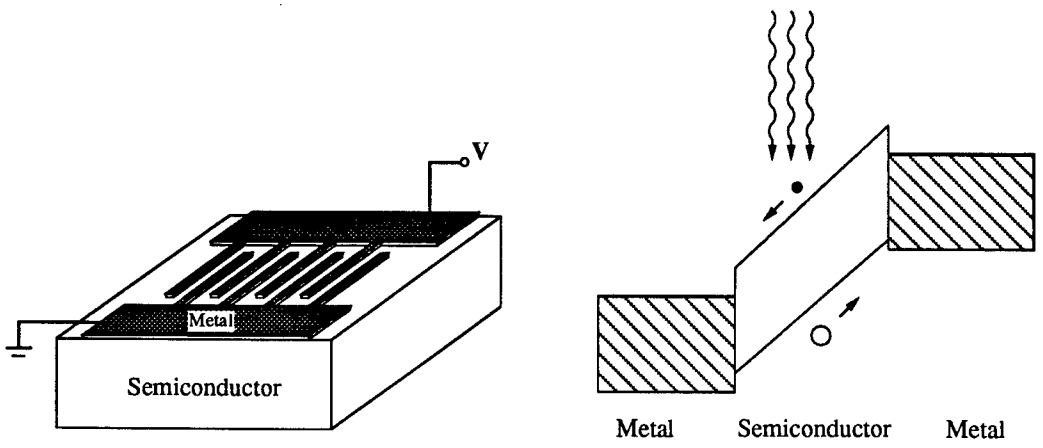


Figure 4.1. Schematic view and band diagram of a MSM photodetector.

In general, the smaller the finger spacing, the shorter the intrinsic response time for the transit-time-limited MSM PDs. Figure 4.2 shows a Monte Carlo simulation of the intrinsic response time versus the finger spacing of a transit time limited MSM PD on high quality GaAs (simulation performed by M.Y. Liu [76]). By decreasing the finger spacing from 1 μm to 0.1 μm the intrinsic response is decreased by an order of magnitude. Thus, significant speed advantages can be obtained by using ultra-small MSM PDs.

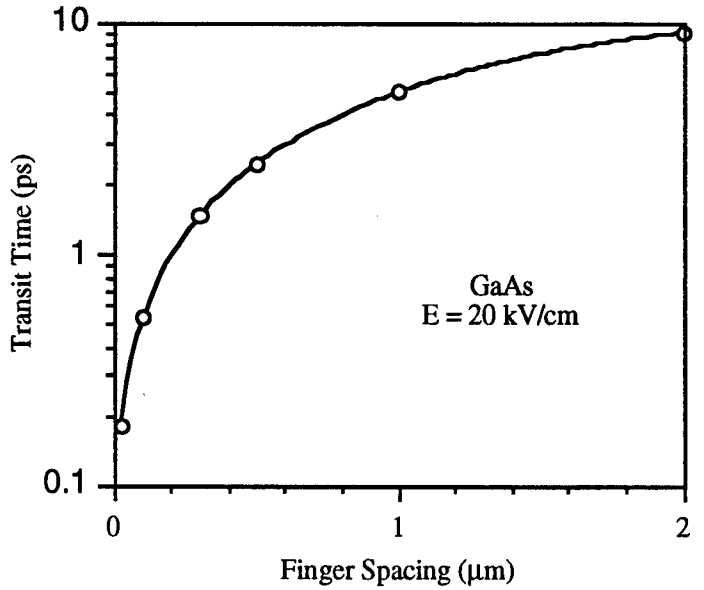


Figure 4.2. Calculated intrinsic response time versus finger spacing for a GaAs MSM PD. Simulation courtesy of M.Y. Liu.[76]

However, capacitance cannot be ignored in real devices. Scaling guidelines for designing high-speed MSM PDs have been determined by S.Y. Chou and M.Y. Liu through experimental data, the simulation of impulse response, and the calculation of device capacitance and can be summarized by four points.[77] The guidelines state that the intrinsic response time of transit-time-limited MSM PDs can be decreased by reducing the finger spacing in accordance with figure 4.2. Furthermore, the capacitance per unit finger length, and hence RC time constant, can be decreased by reducing the ratio of finger width to the finger spacing.

4.2.2 Device Fabrication

A three step nanoscale MSM PD fabrication process has been developed. First, alignment marks are patterned (Fig. 4.3a), then nanoscale MSM PDs are defined (Fig. 4.3b), and the process is finished by creating a transmission line to facilitate high speed

measurements (Fig. 4.3c) The fabrication was performed on a semi-insulating wafer GaAs with a carrier concentration of ~1.5 x 10^7 cm^{-3}, an electron mobility of 6,500 $cm^2/V \cdot sec$, and a resistivity of 5 x 10^7 $\Omega \cdot cm$. Since only the interdigitated fingers of the MSM PD have nanoscale dimension requirements, a mixed lithography scheme was used. Optical lithography with lift-off was used to define the alignment patterns.

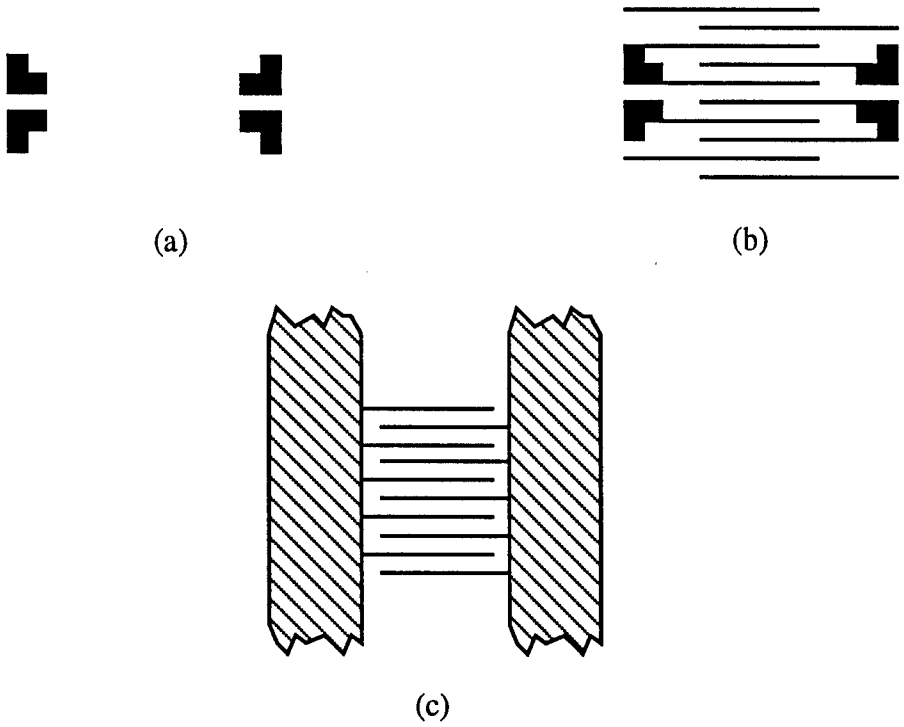


Figure 4.3. Schematic of the MSM PD fabrication process. Alignment marks were produced using photolithography and lift-off (a), nanoscale MSM PDs were fabricated using electron beam lithography and lift-off (b), and waveguides were created using optical lithography.

The nanoscale interdigitated metal fingers are fabricated on the semiconductor substrate by using electron beam lithography and a lift-off technique. Coarse alignment to the previous pattern is accomplished using first the guide marks to locate the desired position of the MSM PD. This was done using the EBL system in SEM mode and using the manual stage micrometers. Once near the desired position the guide marks are used to focus the beam. Fine alignment is performed by exposing only the left and right edges of the exposure field as shown in figure 4.4. Electronic image shift controls are used to

during the fine alignment process. Interlayer alignment accuracy of approximately 0.25 μm is typical for this technique.

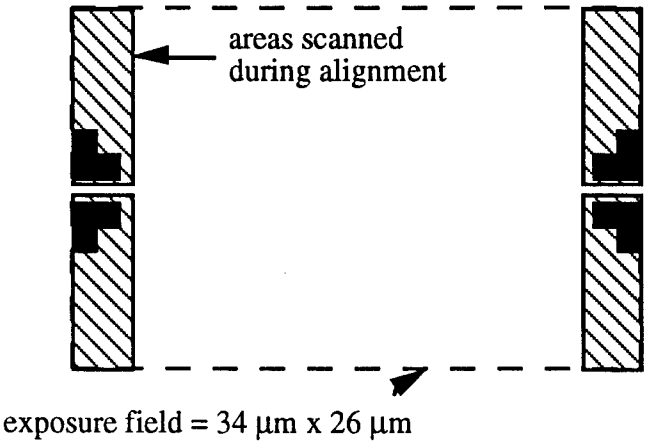


Figure 4.4. Fine alignment technique to align electron beam lithography exposures to optical lithography layers.

Sample preparation for electron beam lithography consists of first, spinning polymethyl methacrylate (PMMA) on the substrate. For MSM detectors with finger spacing smaller than 50 nm, a single layer 70 nm PMMA was used; for finger spacing and width larger than 50 nm, double layer PMMA was used, with a 70 nm thick layer of 100 K molecular weight PMMA on the bottom and a 70 nm thick layer of 950 K molecular weight PMMA on the top. The single layer resist is used to improve the mechanical stability of the resultant narrow PMMA features. The double layer scheme is designed to achieve undercut in the resist for easier lift-off than that of a single layer PMMA. The resist was exposed and developed as described in section 3.3. After exposure and development, metals (Ti/Au) were evaporated onto the samples and were lifted off in acetone. Figure 4.5 shows scanning electron micrographs of (a) a picosecond MSM PD with 40 nm finger width and 160 nm finger spacing and a detection area of 14.5 μm x 15 μm, and (b) a MSM PD with finger spacing and width of 25 nm.

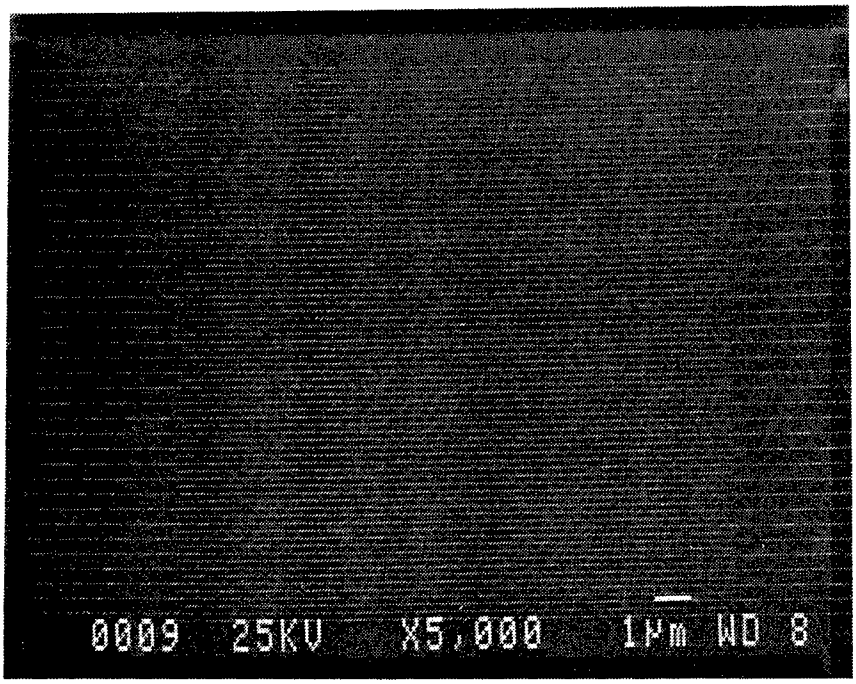


Figure 4.5a. Scanning electron micrograph of a picosecond MSM photodetector with 40 nm finger width and 160 nm finger spacing. The metals are Ti/Au.

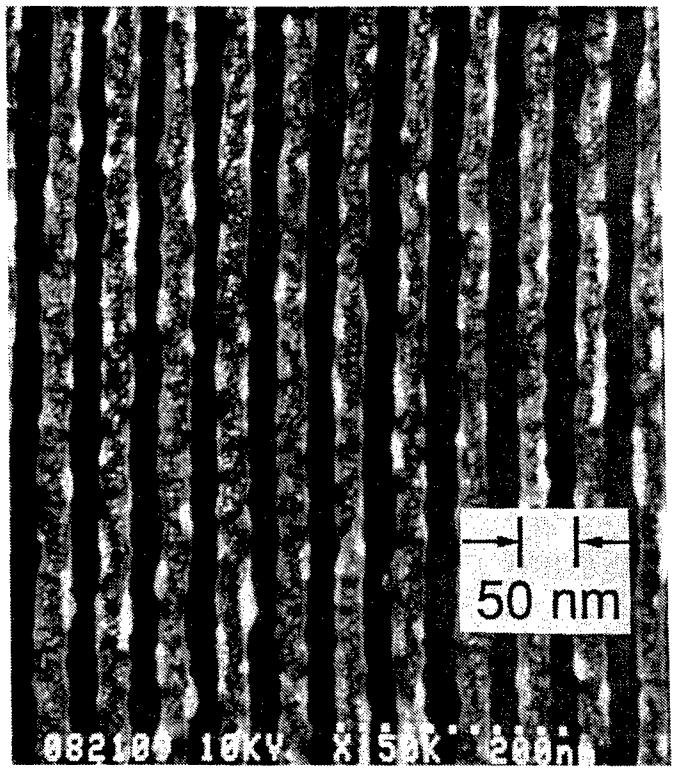


Figure 4.5b. Scanning electron micrograph of a MSM photodetector with 25 nm width and 25 nm spacing. The metals are Ti/Au.

After defining the MSM PDs, transmission lines with a linewidth of 16 μm and a spacing of 9 μm are defined (figure 4.3c). Optical lithography with a lift-off of Ti/Au (50 nm/200 nm thick) was used. The characteristic impedance of the striplines on GaAs substrate is 75 Ω.

4.2.3 Electrooptic Measurement Results

High frequency measurements were performed using a high-speed electrooptical sampling system consisting of a 100 fs colliding-pulse mode-locked dye laser with a wavelength of 620 nm and a repetition rate of 100 MHz.[82] The response of the MSM PDs was measured using a $LiTaO_3$ tip probe placed 250 μm from the detector. A MSM PD on bulk GaAs with 100 nm finger spacing and width and a detection area of 10 μm x 10 μm was tested. The impulse response has a FWHM of 1.5 ps and 3 dB bandwidth of 300 GHz.[81] To the best of our knowledge, this is the fastest MSM PD on bulk GaAs reported to date. Calculations indicate that this response is limited by the RC time constant. If the RC time constant can be reduced to a value less than the intrinsic transit time, the speed and the 3-dB bandwidth of the 100 nm MSM PD can be increased by a factor of 4.

4.3 Point Contact Quantum Effect Device

Historically, the first suggestion that a narrow confinement potential in a semiconductor structure inversion layer might lead to non-classical transport was in 1959.[83] Since the characteristic scale for achieving quantum confinement is the Fermi wavelength, which is on the order of 50 nm for semiconductor inversion layers, it was not

until the demonstration of advanced fabrication techniques that such structures could be defined and analyzed on a routine basis. For example, the advent of epitaxial growth techniques in which thin alternating layers of wide and narrow bandgap semiconductors can be grown made it possible to demonstrate vertical (relative to the semiconductor surface) quantization effects.[84] Nanofabrication techniques, like those described in chapter 3, have enabled experimentalists to investigate lateral as well as vertical quantization effects in a multitude of structures (see for example the many articles in ref [85]).

This section describes the application of nanofabrication techniques to the point contact quantum effect transistor. Although point contact transistors were previously reported [3,4], they were implemented here to verify fabrication and subsequent analysis techniques and to fertilize the ground for subsequent projects. One great advantage of the fabrication techniques described in this section is that they are sufficiently flexible to create a wide variety of devices. For example, this fabrication process was modified to fabricate a transistor whose characteristics are controlled by single electron charging events.[61]

4.3.1 Theoretical Background

The two dimensional electron gas (DEG) between the source and drain in a point contact quantum effect transistor is electrostatically pinched to form a one dimensional electron waveguide in which the conductance is quantized in steps of $2e^2/h$.[3,4] A point contact quantum effect transistor implemented using a modulation doped field effect transistor (MODFET) is shown in figure 4.6a. Modulation doping is achieved by growing a wide bandgap material (here $Al_{0.3}Ga_{0.7}As$) on top of a more narrow bandgap semiconductor (here GaAs). Due to electron affinity differences, and hence a conduction

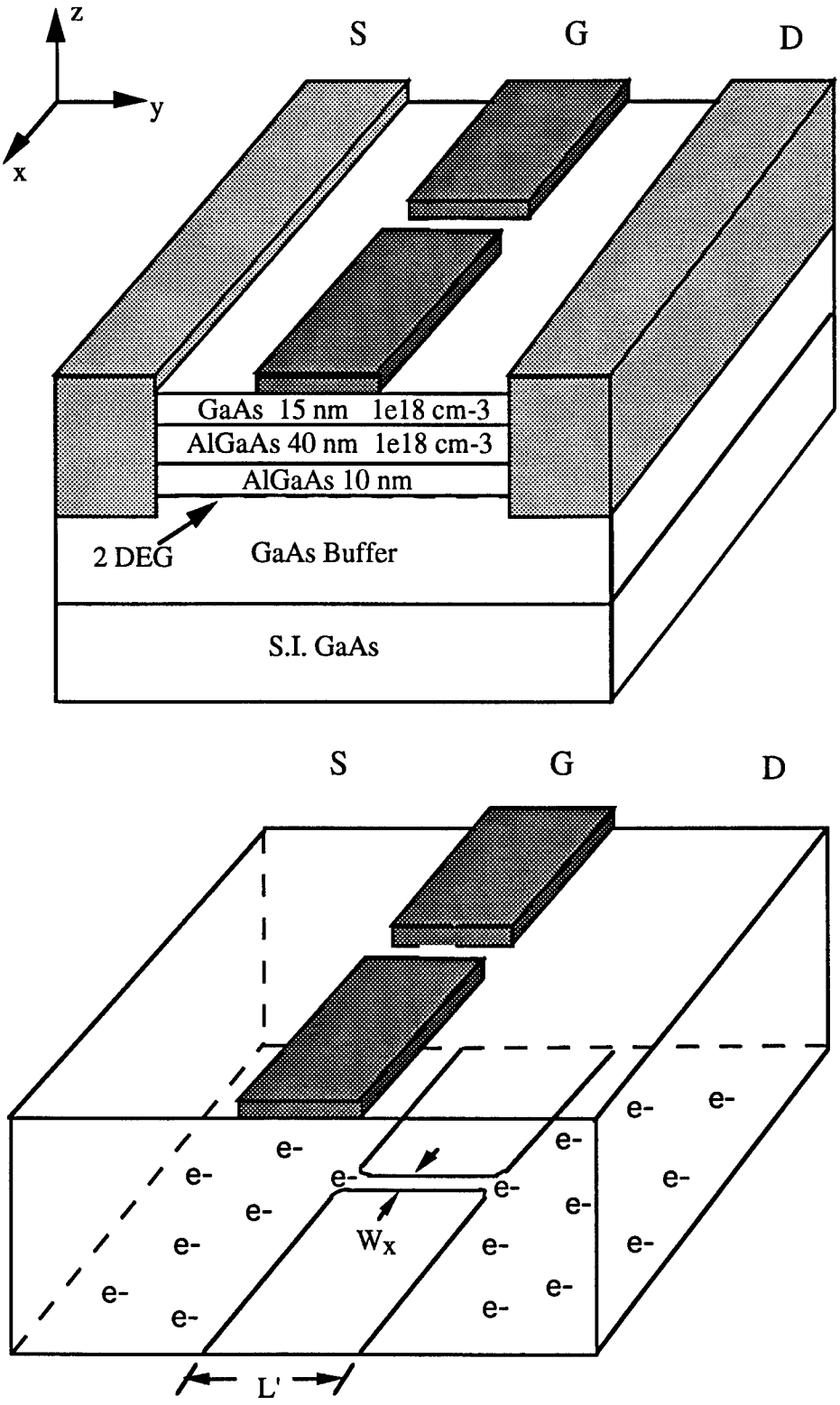


Figure 4.6. The point contact quantum effect device implemented using a MODFET (a), and a schematic view of the constriction in the 2 DEG (b).

band discontinuity, electrons from the doped $Al_{0.3}Ga_{0.7}As$ layer diffuse into the GaAs layer. The spatial separation of electrons from donors results in exceedingly high mobilities, especially at low temperatures. In addition, a strong local electric field is developed which causes a sharp triangular shaped potential well to form at the $Al_{0.3}Ga_{0.7}As$/GaAs interface. Calculations of the energy spacings in the well indicate that the first energy level, $E_{1,z}$, is 20-40 meV above the conduction band, and the second energy level, $E_{2,z}$, is about 20 meV higher, assuming a charge density appropriate for a well designed MODFET of 1-5x10^{11} cm^{-2}.[86] Thus, especially at low temperatures, electrons reside in the lowest subband and a two dimensional electron gas is formed at the $Al_{0.3}Ga_{0.7}As$/GaAs interface.

A one dimensional electron waveguide can be electrostatically induced by applying a negative bias on the gate electrodes (Fig. 4.6b). If the width of the constriction, W_x, is comparable to the Fermi wavelength, the transverse electron momentum will be quantized. W_x can be modulated by adjusting the gate potential. However, electrons can still move ballistically (i.e. encounter no scattering events to randomize the quantum order) in the longitudinal (y) direction as long as $L' \ll$ the electron mean free path, L_e. Typical values of λ_f and L_e are 50 nm and 5-10 μm (at low temperatures), respectively

Assuming infinite square confining potentials, the energy of an electron in such a waveguide can be written as

$$E = \frac{h^2}{8m^*}\left(\frac{n_x^2}{W_x^2} + E_{1,z}\right) + \frac{h^2 k_y^2}{8\pi^2 m^*}$$

where m^* is the conduction effective mass, n_x is the quantum level in the x direction and k_y is the wavevector in the unconstrained direction (y).

The effect of different values of W_x for the electron waveguide is sketched in figure 4.7. For a very narrow constriction, it is possible that only one subband will

contribute to the conduction process (Fig. 4.7a). If the constriction is widened, it is possible that additional subbands will contribute to the conduction process (Fig. 4.7b). This behavior would account for the observed quantization of conductance if each subband is characterized by a constant conductance. The total conductance is then found by multiplying the number of subbands participating to the current flow by the conductance of a subband.

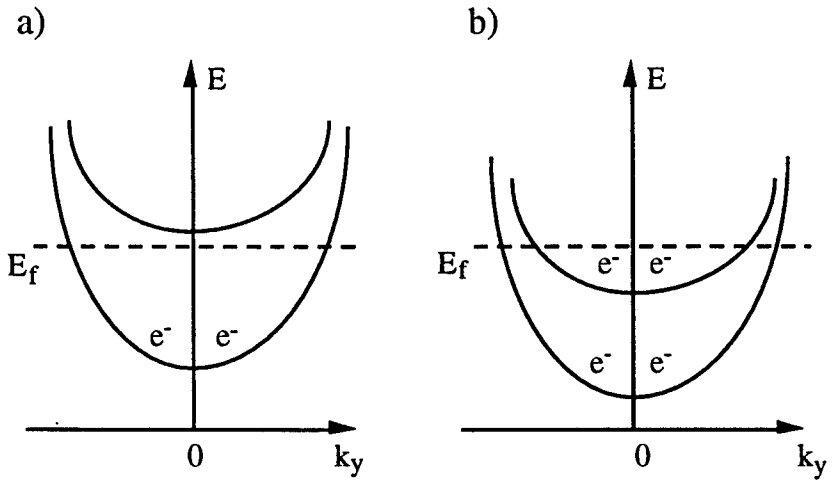


Figure 4.7. Energy vs. wavevector in the electron waveguide showing the dependence on confinement width, W_x. Narrow constrictions reduce the number of subbands participating in conduction (a), while wider constrictions will increase the number of subbands contributing to the conduction process.

It can be shown using classical arguments that each subband in the electron waveguide does contribute a quantized conductance.[4] This argument is valid assuming that the Fermi wavelength is much smaller than the width of the confining potential, and that the length of the constriction much smaller than the mean free path. Beginning with a general expression for current traversing through a single conductive channel

$$I_y = en\langle v\rangle$$

where e is the electron charge, n is the number of carriers per unit length, and $\langle v\rangle$ is the mean carrier drift velocity. n is determined by:

$$n = \int_0^{E_f} D^{1D}(E)dE \quad \text{(valid at T = 0 K)}$$

Here $D^{1D}(E)$ is the density of states per unit length in the interval E to $E + dE$ for a system with one degree of freedom, which is given by:

$$D^{1D}(E) = \frac{g_s}{h}\sqrt{\frac{m^*}{2E}}$$

Where g_s is the spin degeneracy and m^* is the effective electron mass. After integration and simple substitution for E_f, n is found to be:

$$n = \frac{g_s m^* v_f}{h}$$

Now <v> can be related to the applied voltage, V, by:

$$qV = \frac{1}{2}m^*(v_f + \langle v \rangle)^2 - \frac{1}{2}m^* v_f^2$$

If $v_f >> \langle v \rangle$ then this can be reduced to

$$qV \approx m^* v_f \langle v \rangle$$

A final equation for I_z is then given by:

$$I_z = q\frac{g_s m^* v_f}{h}\frac{qV}{m^* v_f} = \frac{g_s e^2}{h}V = \frac{2e^2}{h}V$$

It is clear from this argument, then, that the conductance for a single subband is indeed a constant and is given by:

$$G_{classical} = \frac{I_z}{V} = \frac{2e^2}{h}$$

and the total conductance is then the increased according to the number of channels participating in the conduction process, N_C:

$$G_{classical} = N_C\frac{2e^2}{h}$$

As previously mentioned, the above classical analysis is valid as long as $\lambda_f << W_x$ and $L' << L_e$. However, it is possible to violate the first assumption by biasing the gate near pinch-off. In this case a more accurate description requires a quantum

mechanical framework. Such an analysis results in the multichannel Landauer formula [87,88]

$$G_{Quantum} = \frac{2e^2}{h} \sum_{i,j=1}^{N_c} |t_{i,j}|^2$$

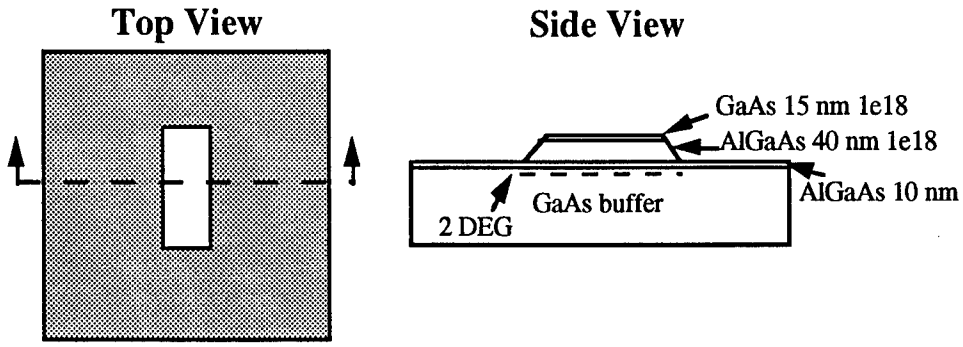
where $t_{i,j}$ is the transmission coefficient from subband j into subband i.

So, assuming perfect transmission, the result is the same as that for the classical analysis. One noteworthy aspect of this is that the conductance for a given subband can never be greater than $2e^2/h$, even in the presence of ballistic transport! It can be lower if the transmission coefficient is less than 1, as would be the case if scattering is present. If the transmission in each subband were perfect, the net conductance would simply be an integer multiple of $2e^2/h$. The existence of the finite conductance implies dissipation. In the case of the point contact device the finite conductance is attributed to electrons scattering at the 1D channel entrance.[89]

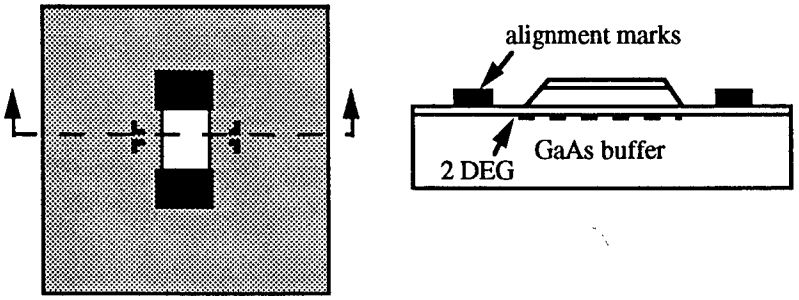
There is one fine point in both the classical and quantum mechanical approaches that should be stated. Both approaches make use of the concept of the Fermi energy, which is an equilibrium construct. A system which is under bias and current is flowing is certainly not in equilibrium, so there are some subtle problems with the analysis. Nonetheless, both approaches agree well with experiment.

4.3.2 Fabrication Using Mixed Lithography

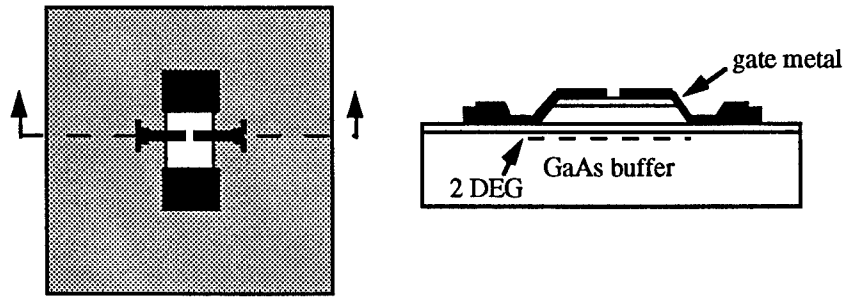
Since only the gate of the point contact has stringent dimension requirements, a mixed lithography technique was implemented. As shown in figure 4.8, optical lithography was utilized for device isolation, ohmic contact and alignment mark definition, and final metalization, and electron beam lithography was used to define the gate. The devices were fabricated from an MBE grown sample consisting of a (100)



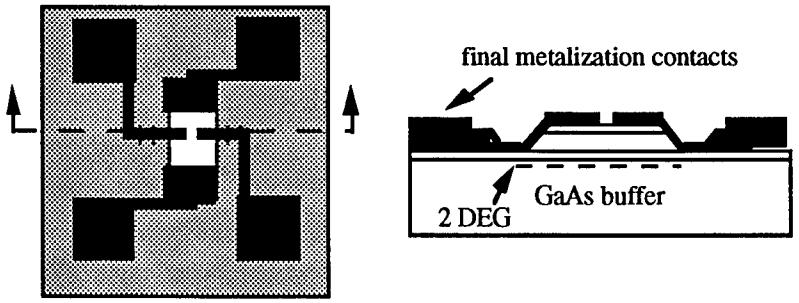
a) Device Isolation - Optical Lithography



b) Ohmic Contacts - Optical Lithography



c) Gate Definition - Electron Beam Lithography



d) Final Metalization - Optical Lithography

Figure 4.8. Process flow for fabricating point contact quantum effect transistors. The process features electron beam lithography for the nanoscale gate which is aligned to non-critical lithography levels patterned with optical lithography.

semi-insulating GaAs substrate, 0.5 μm undoped GaAs, 15 nm undoped $Al_{0.3}Ga_{0.7}As$, 45 nm Si doped (1 x 10^{18} cm^{-3})$Al_{0.3}Ga_{0.7}As$, and 15 nm Si doped (2.8 x 10^{18} cm^{-3}) GaAs cap layer. At room temperature the mobility and carrier concentration were measured via the Hall technique to be 5700 $cm^2/V\cdot s$ and 7.6 x 10^{11} cm^{-2} respectively. At 77 °K the mobility and carrier concentration were 145,000 $cm^2/V\cdot s$, and 6.4 x 10^{11} respectively.

Mesa isolation was performed using optical lithography. Since the metal gates are only 15 to 30 nm thick, and since the mask set used requires that the gates must pass over the mesa edge, an overcut etch profile is necessary to ensure that the gate metal is continuous over the mesa edge. Since {111} Ga planes of GaAs crystals typically etch more slowly than the {111} As planes in the presence of reaction limited etching processes [90], the reaction limited H_2SO_4:H_2O_2:H_2O (1:8:1000) etchant was used. By aligning the channel with the $[01\bar{1}]$ direction, an overcut profile was achieved.

Optical lithography was again used to pattern Ni/Au/Ge contacts using a lift-off technique (Fig 4.8b). The mask was aligned to the isolation pattern using standard alignment patterns, but included in the pattern are alignment marks for the EBL gate. The contacts were annealed at 420 °C for 1.5 minutes.

Electron beam lithography using a 35 kV, 4.5 pA beam was used to pattern a 70 nm thick layer of 950 K PMMA (Fig. 4.8c). The gate was aligned to previous layers with an alignment accuracy of 0.25 μm using the same technique described in section 4.2.2. The accuracy is more than sufficient to place nanoscale gates between ohmic contacts defined using optical lithography. More accurate alignment techniques have been demonstrated for this system as discussed in section 3.3. A 14 nm gate recess etch in $H_2SO_4/H_2O_2/H_2O$ to control the threshold voltage was performed prior to the Ni/Au (15 nm/ 15 nm) gate metal deposition and lift-off.

Optical lithography was again used to define the final metal contact pads (Fig. 4.8d). Devices were then cleaved and mounted with epoxy into 8-pin TO-5 packages for subsequent measurements. Further process details are given in Appendix B.

4.3.3 Measurement and Discussion

Since the spacing between subbands is only on the order of one millivolt, these devices must be measured at low temperature and with low biases to avoid broadening effects. The measurement set-up that was developed is shown in figure 4.9. A computer program was developed to control the gate bias and monitor the drain current. The drain was biased with a 30 μV rms, 140 Hz signal that was passed though a blocking capacitor to suppress any DC offset of the signal generator. Measurements were performed at 0.5 °K using an Oxford Instruments He^3 dewar.

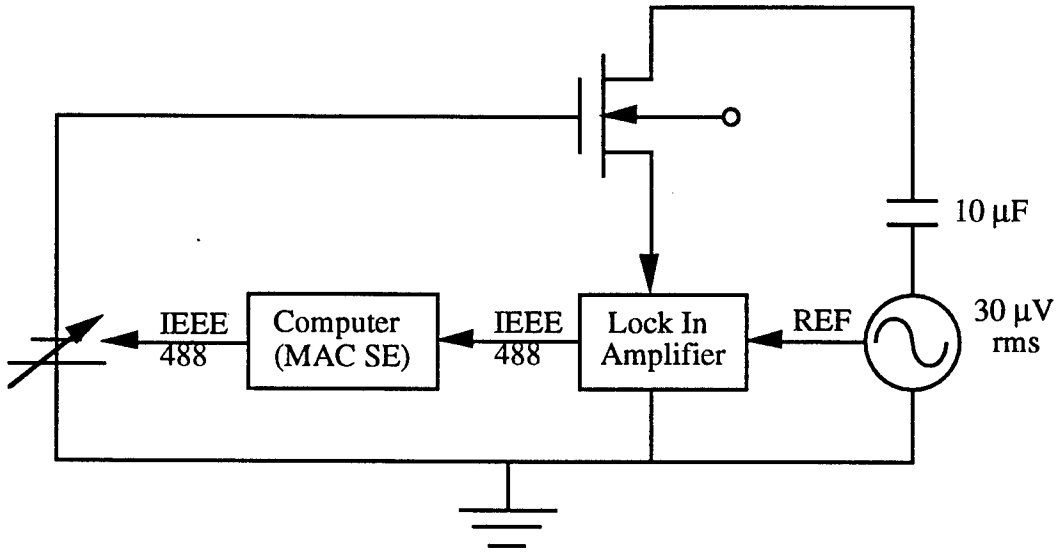


Figure 4.9. Circuit diagram for conductance measurement.

An example of the quantization in the conductance of a 1D channel connecting two 2 DEG reservoirs is shown in figure 4.10. The gate length for the device was 200

nm, and the gap was 100 nm (insert of Fig. 4.10). Both of these dimensions meet the theoretical criteria for transverse confinement and longitudinal ballistic transport. The data shows 4 steps in the conductance, each step corresponding to a constant increase on the order of $2e^2/h$. The deviations of the steps from exact multiples of $2e^2/h$ is most likely due the interband impurity scattering. The mobility in this sample was not measured at 0.5 °K, so it is difficult to closely estimate L_e for this sample. Furthermore, L_e in the 1 dimensional electron waveguide may well be almost an order of magnitude smaller than L_e in the 2 DEG since the 1 DEG ineffectively screens potential fluctuations.[91]

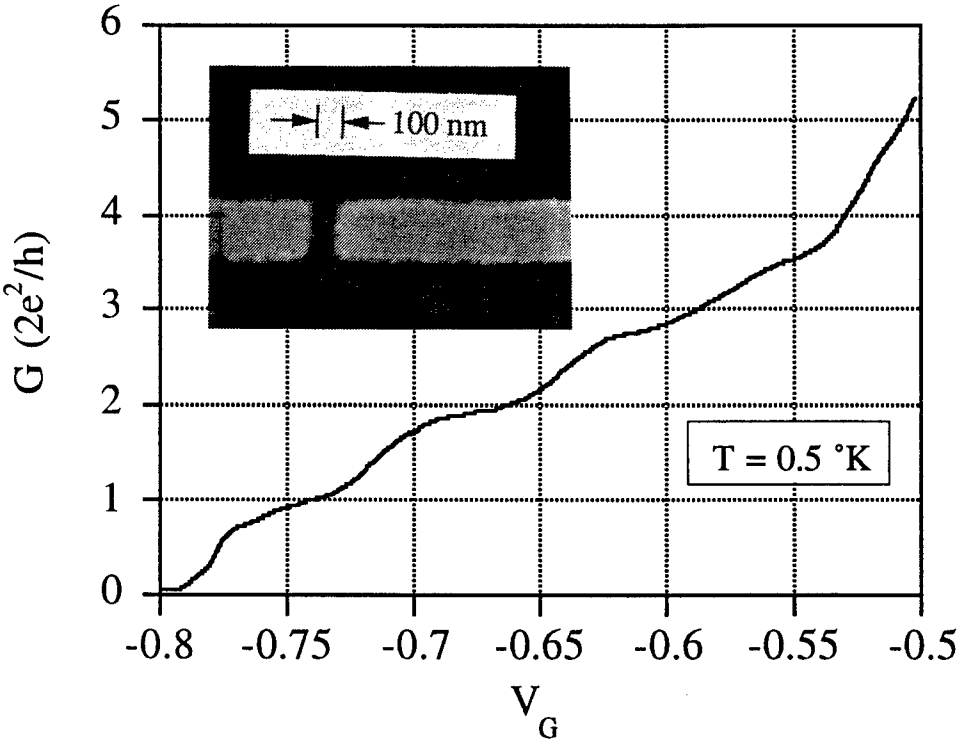


Figure 4.10a. Conductance vs. gate bias for a point contact quantum effect MODFET at 0.5 °K. The gate length is 0.2 μm, and the gap is 0.1μm.

Assuming ballistic transport remains valid, the quantization of conductance should increase as the constriction is lengthened and the degree of evanescent tunneling

through the constriction is reduced. Just the opposite effect was observed. For example, the strongest conductance quantizations was observed in devices with gate lengths of 200 nm, but have not observed quantized conductance in devices fabricated on the same substrates with gate lengths ≥ 500 nm. This is possibly also due to the fact that the 1 DEG screens the potential fluctuations more ineffectively than 2 DEG-based calculations suggest.[91]

One noteworthy problem with delicate gate structures like that of the point contact quantum effect transistor is that they are extremely susceptible to electrostatic discharge as evidenced in figure 4.10b. This can be minimized by bonding both gate pads to the same pin.

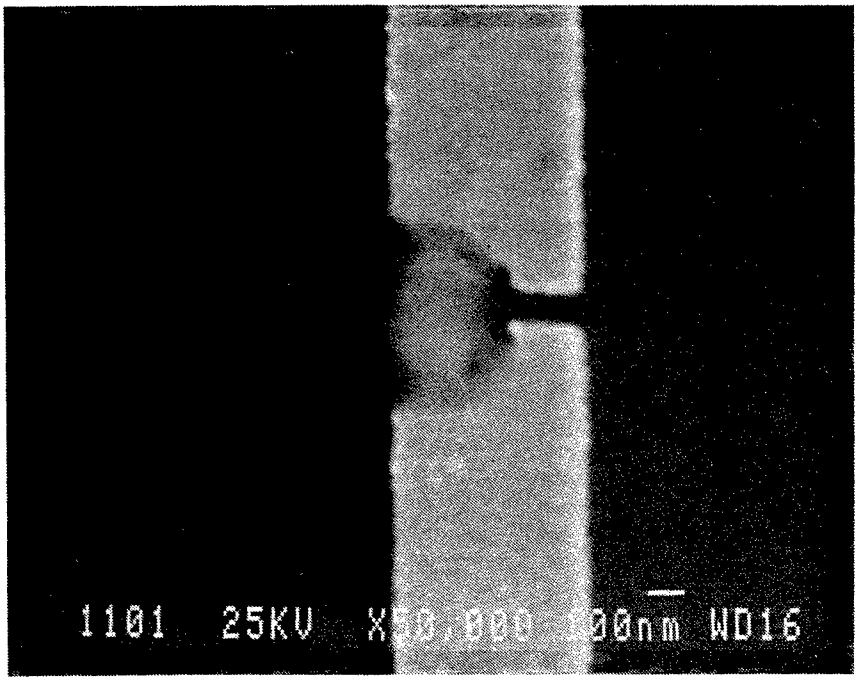


Figure 4.10b. Point contact gate after an encounter with electrostatic discharge.

4.4 Investigation of the Origin of Light Emission from Si

Recently, efficient luminescence from porous silicon was reported.[5] As yet there exists no satisfying explanation for the origin of the photoluminescence signal, though explanations in terms of quantum confinement and surface chemistry have been suggested. Conventional tests to verify or disprove quantum confinement, such as polarization dependence, transport, and magneto-optic measurements have been inconclusive in the case of porous silicon. Presumably, this is due to the isotropic nature of porous silicon.[92] This section demonstrates that nanofabrication techniques can be used to controllably prepare ordered silicon pillar arrays that exhibit PL.

4.4.1 Review of Theories

Silicon has long been the material of choice for the electronics industry. However, due to its indirect bandgap, silicon is not directly suitable for optoelectronics applications. Because the integration of optical sources onto silicon chips potentially offers higher functionality and further miniaturization, numerous attempts have been made to achieve efficient luminescence from silicon. A number of approaches have been investigated. One approach has been the introduction of impurities, like Er, into the Si crystal.[93] The introduction of impurity centers that localize the electron hole pairs tends to relax the wavevector selection rules. This enhances the probability for radiative recombination. However, luminescence through impurity centers is still vanishingly weak at room temperature.

An alternative approach to achieve light emission from silicon is through quantum confinement. As the particle size decreases, the values of the allowed energy levels

increases, analogous to a particle in a quantum mechanical box. The effect is illustrated for a one-dimensional box in which the conduction effective mass of an electron was used (Fig. 4.11). An exact calculation of the bandstructure in such a small semiconductor

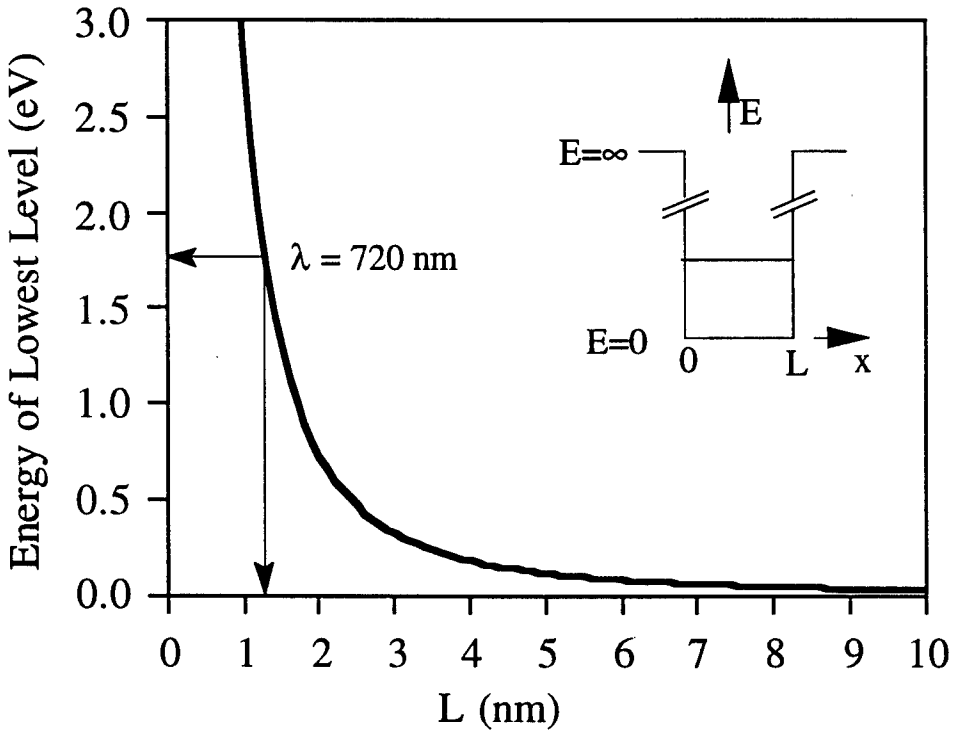


Figure 4.11. The energy of the allowed minimum energy level in a one-dimensional quantum box as a function of confining dimension.

particle is highly complex, but first order bandstructure calculations show that a direct transition with an optical gap of about 2 eV can be achieved in a silicon particle about 1.5 nm in diameter.[94,95] One experimental approach to achieve quantum confinement involved silicon rich SiO_2 in which silicon islands, approximately 50 Å in diameter, were formed by annealing.[96] Another approach involved planar magnetron radio frequency sputtering of a silicon target in ultra-pure hydrogen gas.[97] However, in both of these examples, the observed luminescence has been weak and not exhaustively proven to be due to quantum confinement.

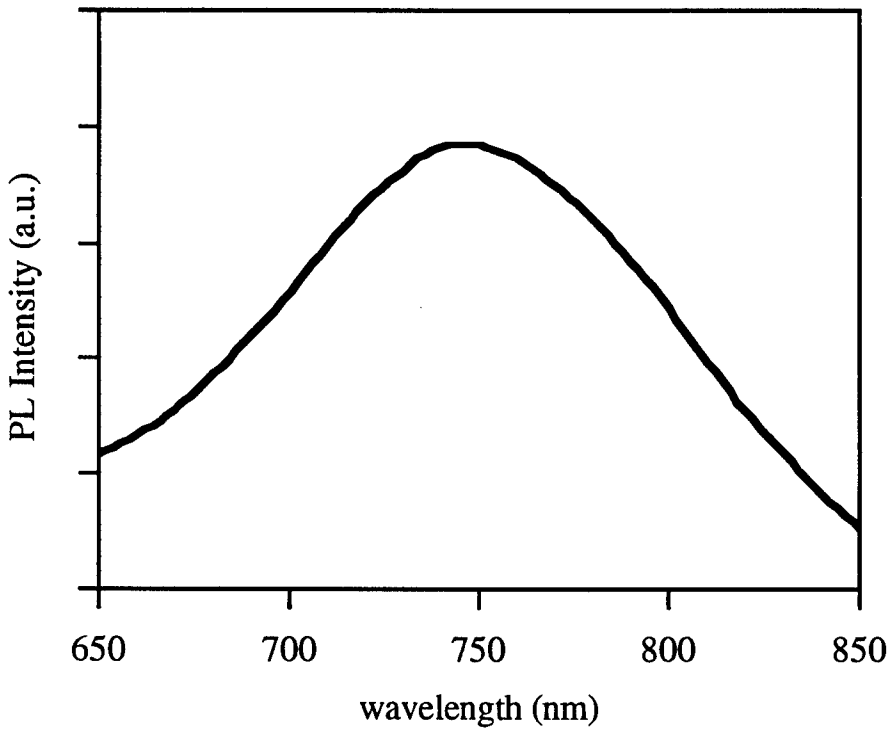


Figure 4.12. Photoluminescence signal from porous silicon.

Porous silicon is the latest approach to achieve light emission from silicon. Efficient luminescence was first reported in this material by Canham in 1990 [5], and an independent investigation at the same time found that the absorption edge of porous silicon was 0.5 eV higher than that for regular silicon [6]. An example of the photoluminescence spectra from porous silicon is shown in figure 4.12 (sample prepared by X. Zheng [98]). Porous silicon forms on crystalline silicon wafers in hydrofluoric acid under anodic bias.[99] High resolution transmission electron microscopy has shown porous silicon to be a labyrinth of interconnecting silicon columns with a crystalline skeletal structure.[100] In the same work, evidence of silicon wires approximately 3 nm in diameter was also presented. The integrated intensity of this material is actually comparable to that of the direct bandgap material GaAs.

A controversy presently exists concerning the origin of luminescence from porous silicon. Some investigators suggest that the luminescence is due to quantum confinement due to the small size of the silicon filaments and due to experimental data which shows a blue shift for decreasing wire size.[5,6] However, measurements of the dependence of photoluminescence on temperature in which the PL intensity is found to decrease with decreasing temperature below about 200 °K, suggesting that the PL is phonon assisted.[101]

Other origins for the PL observed from porous silicon have also been suggested. One intriguing observation is that the PL signal from porous silicon is quite similar to the chemical compound siloxene ($Si_6O_3H_6$).[102] The direct drawback for this model is that oxygen needs to be present, and groups have demonstrated PL from porous silicon that shows almost no trace of oxygen.[103] An alternative model suggests that the PL is due to surface chemistry, in particular polysilanes (not siloxene), with the PL energy being a function of H content and polysilane chain length and the intensity a function of surface area.[104] The model is based on an experiment in which porous silicon is annealed in ultra-high vacuum to produce silicon particles approximately 100 nm in diameter, which still exhibit PL.

4.4.2 Experiment

Here, an approach to fabricating ordered nanoscale silicon pillars for studying PL is demonstrated. The Si pillar fabrication process consists of three main steps: etch mask definition using electron beam lithography (sec 3.3), RIE (sec 3.4.2), and HF etching to reduce the size of the pillars and passivate the Si surface (sec 3.4.3). Previously, PL has

been observed from "black silicon[1]" with features as small as 40 nm (from SEM measurements).[105] Unfortunately, PL was only observed from a small percentage of samples, and processing details have been lost.[106] Another approach has involved a fabrication process utilizing electron beam lithography, Cl-based RIE, and subsequent size reduction using an oxidation technique.[74] One drawback of the oxidation process is that it is a stress dependent process and is non-uniform and significantly changes the original shape of the pillars. However, HF etching is a relatively stress independent process and therefore preserves the original shape of the structure. Also, the HF process more closely mimics the processes presently used for porous silicon studies. Furthermore, subsequent size reduction using room temperature HF etching will tend to remove outer silicon layers that have been damaged or implanted during the RIE process.

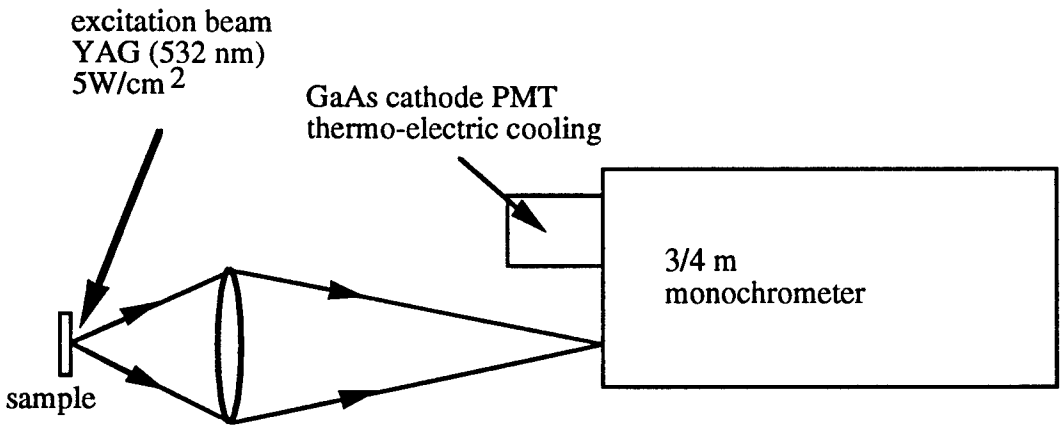


Figure 4.13. Schematic of PL measurement set-up.

PL measurements were performed at room temperature using an excitation wavelength of 532 nm from a Nd^{3+}:YAG laser using the set-up in figure 4.13 (measurements were performed by E. Chen and K. Dai). The beam was focused to a spot of about 100 μm diameter and had a power density of 5 W/cm^2. The photoluminescence

[1]Black silicon refers to reactive ion etched silicon surfaces on which pillars are formed due to contamination during etching.

was analyzed using a 3/4 meter monochrometer and was detected by a thermo-electrically cooled photomultiplier tube with a GaAs cathode. An initial sample had Si pillars with 50 nm diameters, a period of 150 nm, and a length of 450 nm over an area of 600 x 450 μm^2. The pillar diameters were subsequently reduced using HF etching. PL measurements were done at various stages of the pillar diameter reduction process.

4.4.3 Results and Discussion

No photoluminescence was observed in the sample just after RIE or after removing the Cr and 4 hours of HF etching. After 4 hours of HF etching, SEM analysis found the pillar diameters to be 35 nm. After 8 hours of HF etching, however, PL peaks centered at 720 nm were observed repeatedly from part of the pillar region but not from the bulk region of the same sample (Fig. 4.14). SEM analysis at this stage of the experiment found the smallest section of the pillars to be about 20 nm in diameter (Fig. 4.15).

One criticism of the pillars (Fig. 4.15) used for this investigation is that the filament dimensions are not well defined as the pillars consist of a small filament resting on top of a pyramidal base. An improvement to the fabrication technique would be to etch with NF_3 which has been shown to produce more uniform columns.[107] The general feature sizes of the pillar array ($\geq$ 20 nm) are too large to expect confinement effects. While these data alone are insufficient to definitively identify the true origin of the PL signal, it is another powerful demonstration of the utility of nanofabrication techniques.

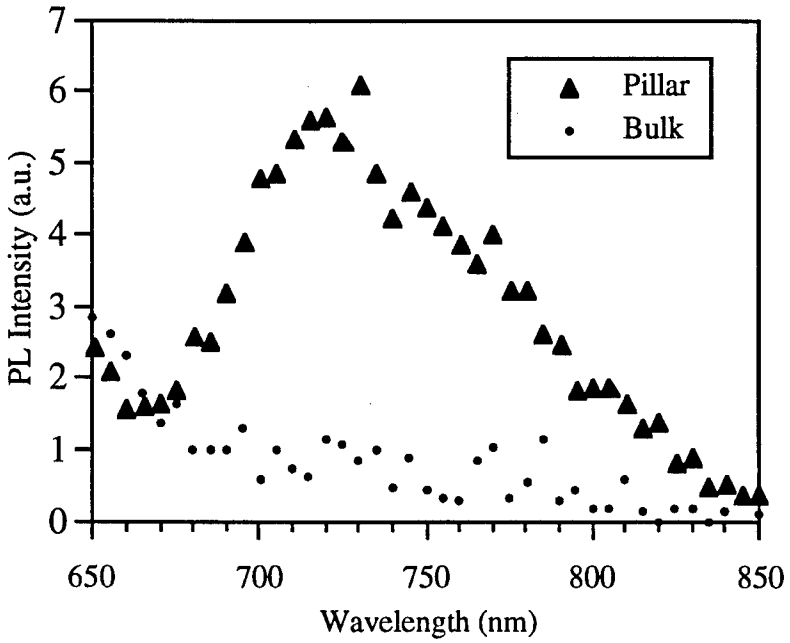


Figure 4.14. The PL spectrum obtained from an array of nanoscale Si pillars. The PL peak is centered at 720 nm. The PL signal from the bulk was obtained from an unpatterned region near the pillar array.

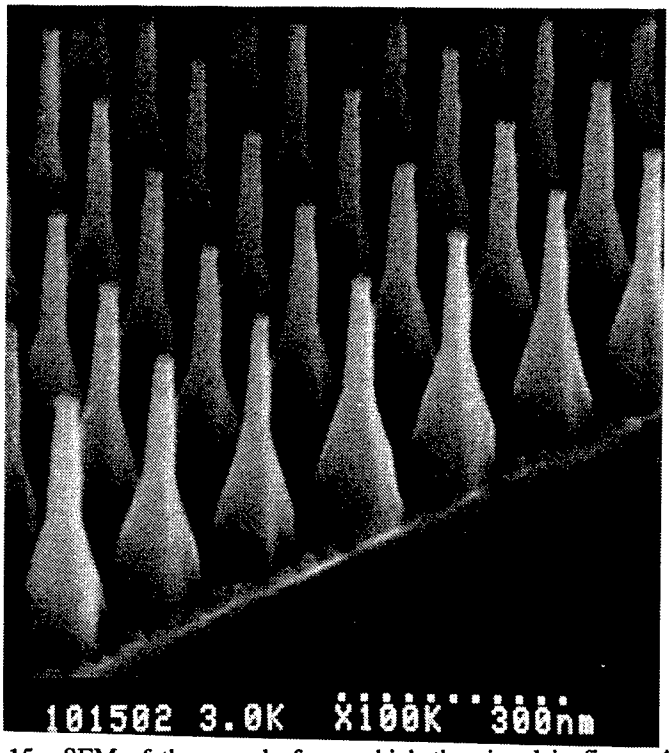


Figure 4.15. SEM of the sample from which the signal in figure 4.14 was obtained. The sample was etched in HF for 8 hours.

4.5 Nanoscale Magnetic Structures

4.5.1 Introduction

Magnetic force microscopy (MFM) has recently gained significant attention as a magnetic imaging technique which is non-destructive and is capable of sub-micron resolution.[108-111] The MFM tip is one of the most important elements in determining the resolution and sensitivity of an MFM since the final image is formed by measuring the interaction between a sharp magnetic tip and the surface fields which arise from the divergence of the sample magnetization (magnetic charge). The tip dependence translates into MFM images which varies significantly when different tips are used, even though the same sample is imaged.[111,112] After briefly mentioning some first principles of magnetic force microscopy, subsequent sections will discuss two approaches, based on nanolithography techniques, that can be used to minimize tip dependencies. One was pointed out by Chang and Zhu [113] and the other devised by Chou [114].

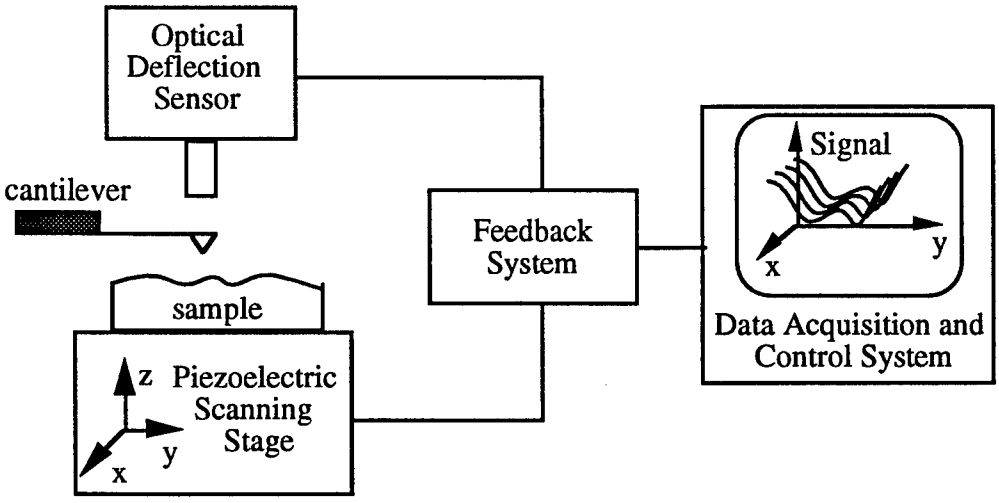


Figure 4.16. Conceptual diagram of a Magnetic Force Microscope (MFM).

Conceptually, an MFM consists of five main components (Fig. 4.16): a small force sensor attached to the end of a cantilever with a spring constant of approximately 1 N/m, a cantilever deflection sensor, a feedback network, a piezoelectric scanning stage, and a data acquisition system. Magnetic force microscopes are operated in a non-contact mode in which the tip-to-sample spacing typically ranges from 50 to 200 nm to avoid the short-range van der Waals forces. The cantilever is mounted on a piezoelectric bimorph which is typically oscillated at a frequency just above the resonant frequency of the cantilever, ω_O, and an amplitude of approximately 10 - 100 Å. Force gradients can be detected through their effect on the spring constant of the cantilever, k. In the presence of a force gradient, F', the cantilever exhibits the properties of an effective spring constant, k_{eff},

$$k_{eff} = k - F'$$

The new resonant frequency of the cantilever, ω'_O, then becomes

$$\omega'_O = \omega_O(1-F'/2k)$$

Since F' contains information concerning the divergence of the sample magnetization, magnetic properties of the sample are encapsulated in the resonant frequency shift (= $\omega_O F'/2k$). The resonant frequency shift can then be detected by the cantilever deflection system and utilized by the feedback and data acquisition systems to maintain stable operation and develop a picture of the sample's magnetic properties, respectively. Unfortunately, the total force gradient is obtained by integrating over the magnetic tip volume.[115] The integration leads to an image smoothing effect and a subsequent decrease in spatial resolution when tips with a significant effective volume are used.

Previously, nanofabrication techniques have been used to study hysterisis effects [116] and switching fields [117] in controlled arrays of approximately 0.15 μm wide permalloy bars. Here, nanofabrication techniques are used to minimize the effect of tip volume on resultant MFM images. In section 4.5.2, nanofabrication techniques are

applied to the fabrication of nanomagnetic bar arrays. Such arrays have been utilized to remove tip effects from raw MFM images.[78] In section 4.5.3, tip effects are minimized using a novel MFM tip designed to minimize the magnetic tip volume in the first place.[79]

4.5.2 Nanomagnetic Bar Arrays

In the past, numeric calculations of the interaction between the tip and the sample field has been the only means to interpret MFM images.[112,118-120] Unfortunately, these calculations require *a priori* knowledge of the tip geometry and its magnetic properties, which are difficult if not impossible to obtain. Conceptually, the MFM image can be considered as being formed point by point by a convolution of a tip impulse response function with the magnetic charge distribution of the sample. The tip dependence translates into MFM images which varies significantly when different tips are used even though the same sample is imaged.[111,112]

As pointed out by Chang and Zhu [113] nanofabrication techniques can be used to create single domain nanomagnetic bars, which can subsequently be used to determine the impulse response of the tip. Knowing the tip's impulse response allows tip dependent images to be deconvolved into a mapping of the "true" magnetic charge distribution of the sample. For this novel application, arrays of narrow nickel strips were fabricated on a Si substrate using electron beam lithography and a lift-off technique (section 3.3). Each Ni strip used for obtaining the tip response function is about 1 μm long, 90 nm wide, and 20 nm thick. Figure 4.17 displays an AFM image of such an array of Ni strips.

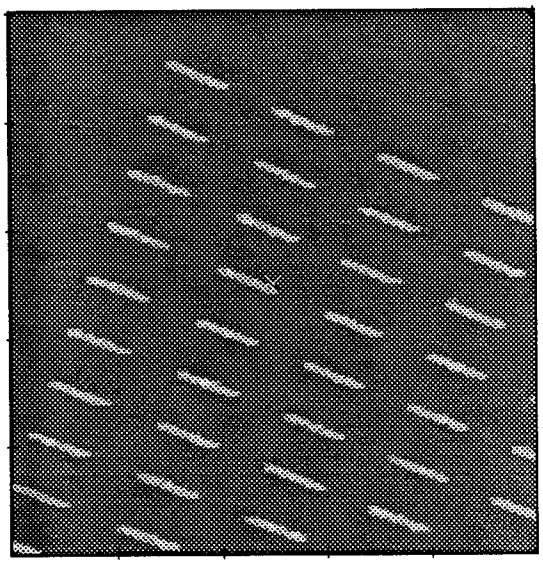


Figure 4.17. 10 μm by 10 μm AFM image of nanoscale nickel strip array elements used to acquire the experimental tip response function. Each array element is 1 μm long, 90 nm wide, and 20 nm thick. (AFM image courtesy of T. Chang)

Because of size and shape anisotropy the bars are single domain. The step discontinuity of the magnetization at the end of the strip approximates a "point" magnetic charge. By imaging the ends of the nickel strip a close approximation to the impulse response of the tip can be obtained. Magnetic force microscopy of the array shown in figure 4.17 by T. Chang verified that the bars were single domain (Fig. 4.18). The dark and light features are the response due to the positive and negative magnetic charges located at the end of the Ni strips. Also shown in figure 4.18 is a detailed mesh plot of the tip impulse response obtained from imaging one end of a nickel strip. The MFM system used in this experiment was developed by T. Chang.[121] It implements a fiber-optic interferometer detection system very similar to the one described in [122]. The probes used are electrochemically etched Ni wires bent into a tip/cantilever configuration.

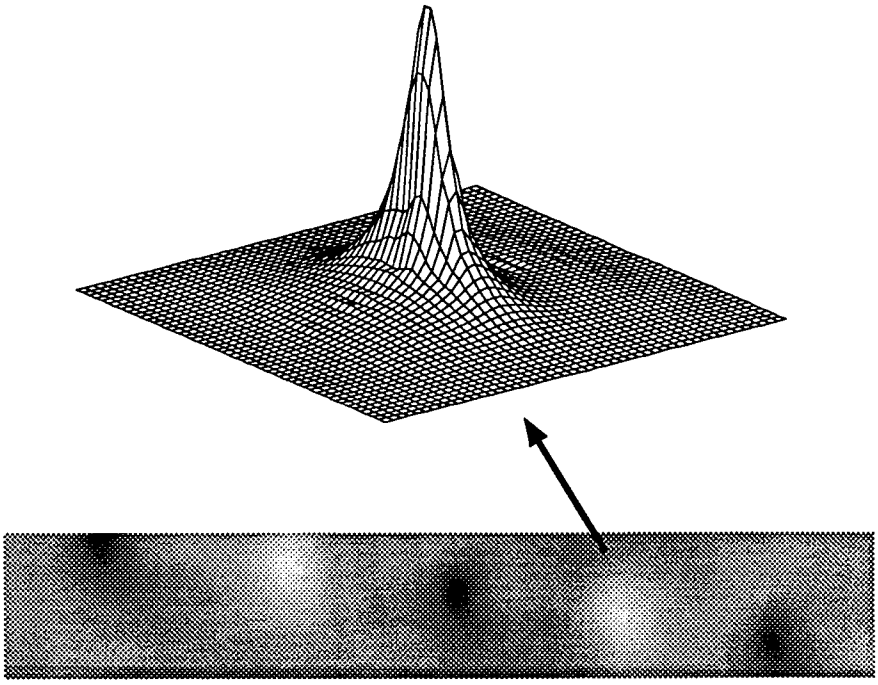


Figure 4.18. 1 μm by 5 μm MFM image of nanoscale nickel strips and the detail mesh plot of the tip response function. Measurement courtesy of T. Chang.[78]

Such a tip impulse response has been used to remove tips volume effects from a raw MFM image to significantly improve the image resolution.[78] This deconvolution technique appears to be a step towards the quantitative analysis of raw MFM images and demonstrates another application of nanostructure fabrication techniques.

4.5.3 Single-domain Magnetic Spike Tips

An alternative approach to minimizing tip dependent effects is to use nanofabrication techniques to accurately control the magnetic properties of the tip. Previously, sharpened Ni wires[108] and magnetically coated atomic force microscope

tips[123] have been used as MFM tips. Such tips suffer from several drawbacks. First, the tips may consist of multiple magnetic domains, and are large in area therefore having a broad distribution of magnetic charge. These all result in poor spatial resolution. Second, the tips have a significant magnetic charge that can alter the magnetic properties of the magnetic material under inspection. To avoid such interference, the tip has to be kept rather far away from the sample surface, hence drastically reducing the MFM's resolution.

To overcome these problems, Chou has proposed a novel MFM tip that consists of a long non-magnetic pillar of nanoscale diameter and a ferromagnetic film that covers only part of the pillar but not the rest of a MFM tip.[114] Such an MFM tip has three important advantages. First, because of the nanoscale size and shape anisotropy, the magnetic tip is single domain. Second, due to the sharpness and small effective magnetic cross section of the tip, it offers higher resolution. Third, due to the small magnetic charge, it is less likely to alter the magnetic properties of the sample. We refer to this tip as the single-domain magnetic spike (SMS) tip. In this section we present one embodiment of such a tip, its fabrication technology, and evaluate its performance.[79]

4.5.3.1 Tip Fabrication

The SMS tip fabrication process consists of two main steps (Fig. 4.19). (1) The non-magnetic pillar was fabricated by contamination electron beam lithography on top of the pyramid of a commercial scanning force microscope (SFM) tip. (2) Ferromagnetic

materials, such as nickel or cobalt, were coated on one side of the pillar. In the first step,

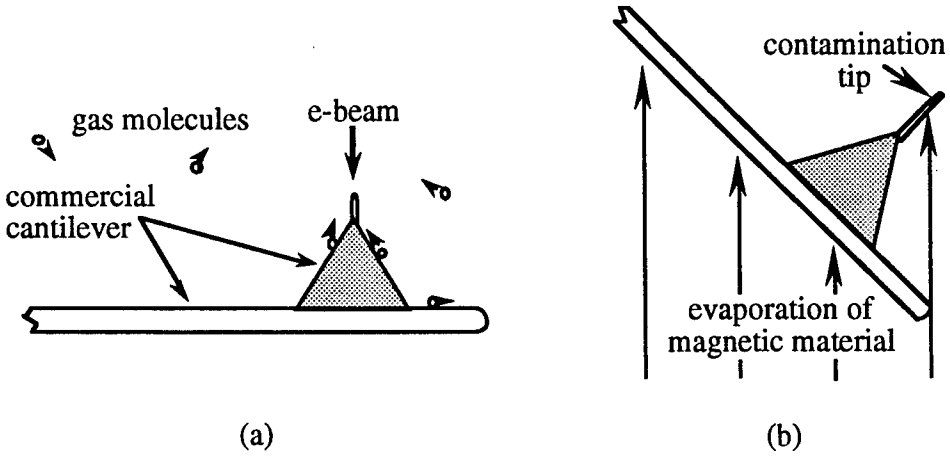


Figure 4.19. Schematic of the two step fabrication process consisting of (a) tip growth using contamination lithography, and (b) shadow evaporation.

SFM cantilevers were first sputter coated with 20 nm of gold to prevent charging during the electron beam contamination lithography and to facilitate subsequent focusing on the apex. The tips were then mounted and inserted into a JEOL-840A SEM with a diffusion pump vacuum system and a tungsten filament gun. A contamination pillar was then grown on the apex by exposing the tip in spot mode for a specified length of time. Growth is due to electron beam assisted molecular deposition onto the cantilever surface. The deposited material was not intentionally introduced, but originates primarily from the background of the SEM vacuum chamber and from the sample surface itself. Similar contamination deposits have been shown to be mainly composed of carbon and oxygen.[124]

The growth process was optimized to produce long but narrow pillars with small tip radii. Such pillars would fulfill the requirements for high resolution MFM tips. The accelerating voltage and beam current were the most influential parameters in the growth process. Figure 4.20 shows the tip length with respect to exposure time for a beam current of 10 pA and an accelerating potential of 15, 25, and 35 kV. In all three cases the

growth rate becomes relatively constant after an initial transient. The growth rate for 35 kV was found to be the highest (0.1 μm/min. after the initial transient).

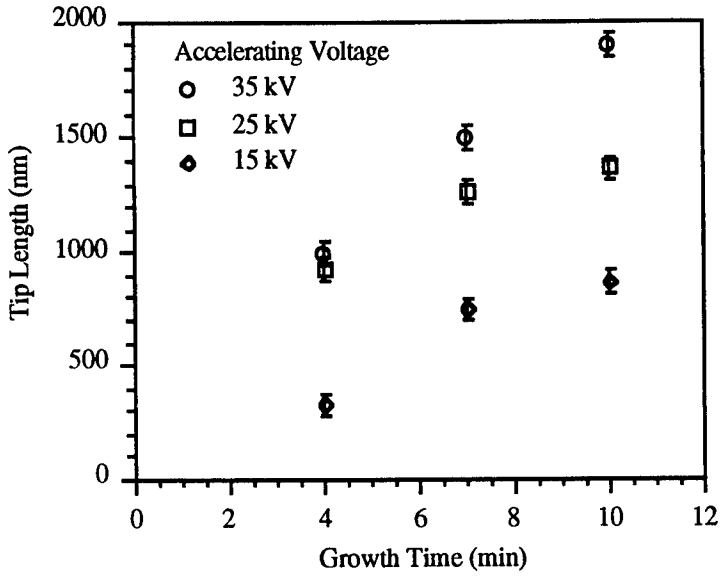


Figure 4.20. Tip length with respect to exposure time for a beam current of 10 pA and an accelerating potential of 15, 25, and 35 kV.

With lower beam currents there was a dramatic increase in growth rate. Figure 4.21 shows the resulting tip length with respect to beam current when a 25 kV beam is focused onto the apex for 7 min. The higher growth rate at a lower beam current is possibly due to reduced local heating, in accordance with condensation theory.[125]

The accelerating voltage was found to affect the average pillar tip radius. The average pillar tip radius was observed to decrease from 30 nm to 19 nm as the accelerating voltage increased from 15 to 35 kV (Fig. 4.22). This is possibly due to the convolution of decreased beam diameter and decreased beam broadening at higher accelerating potentials. According to Monte Carlo simulations, an infinitesimally small 15 kV beam is broadened to a radius of 20 nm after traversing through 50 nm of carbon, while an infinitesimally small 35 kV beam is broadened to only 10 nm after traversing the same amount of carbon.

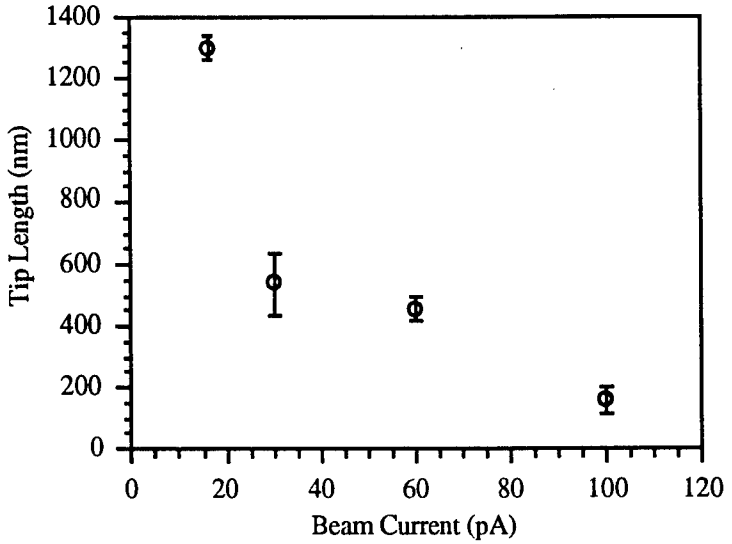


Figure 4.21. Characterization of tip length with respect to beam current for a 7 minute exposure with a 25 kV beam.

From these pillar growth studies, the pillars used for making SMS tips were grown with a beam current of 10 pA, an accelerating potential of 35 kV, and growth times ranging from 7 to 10 min. The beam current of 10 pA can maximize the growth rate while maintaining sufficient signal to readily focus on the tip apex. An accelerating potential of 35 kV was chosen to obtain the smallest tip radius and obtain the highest growth rates to avoid any system instabilities during the growth. The working distance and magnification for the growth were not found to have a major effect and were maintained at 10 mm and 30,000 X respectively.

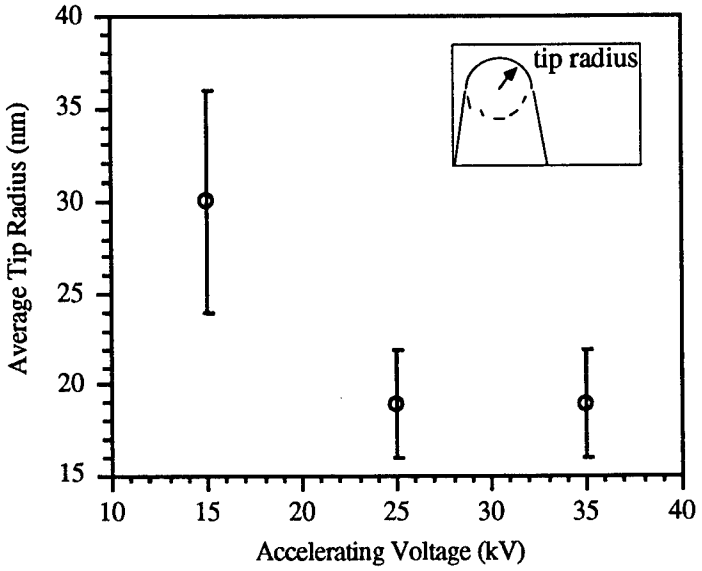


Figure 4.22. Characterization of tip radius with respect to accelerating voltage. The insert defines the tip radius. The growth time and beam current were fixed at 10 pA and 7 minutes respectively.

After growing the non-magnetic contamination pillar, the magnetic spike was formed by an evaporation of nickel or cobalt from an angle as illustrated in figure 4.19. The sample is held at an angle with respect to the evaporation source in an electron beam evaporator so that only the pillar but not the pyramid of the tip is coated with ferromagnetic material. In this way, a controllable portion of the tip can be coated with the desired metal. One advantage of this fabrication process is that the thickness of the magnetic material, and thus the effective cross section of the magnetic spike, can be accurately controlled and can be kept small. Figure 4.23 shows a completed MFM tip with a nanoscale nickel magnetic sensor at the tip. The nickel spike, which is trough shaped with a tapered end, is 30 nm thick, 1.4 μm long, and has an average width of about 150 nm and a 10 nm tip radius. The non-magnetic contamination pillar is approximately 1.7 μm long, has an average diameter of about 150 nm. The curvature in the tip is due to intrinsic tensile stress which is present in evaporated nickel.

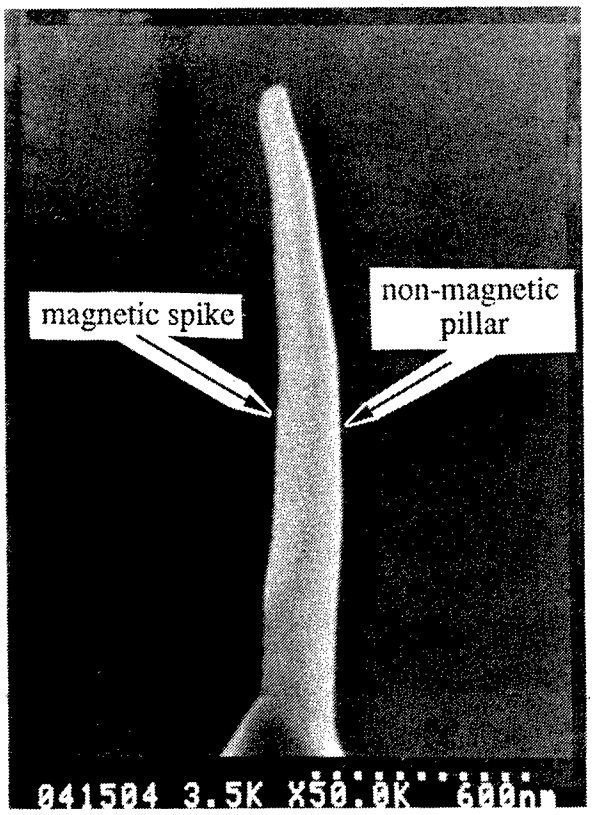


Figure 4.23. Completed SMS tip with a nanoscale nickel magnetic sensor at the tip. The Ni spike, which is trough shaped with a tapered end, is 30 nm thick, ~150 nm wide, 1.4 μm long, and has a 10 nm tip radius. The non-magnetic contamination pillar is ~150 nm wide and 1.7 μm long. Intrinsic stress in evaporated Ni bends the tip.

4.5.3.2 Expected Performance

Calculations, performed by M. Wei, are included here to demonstrate the anticipated performance of the novel SMS tips. The response of the SMS tip to a magnetic dipole was compared to a standard Ni wire tip (Fig. 4.24). The full width at half maximum (FWHM) response for the SMS tip is 40 nm whereas the FWHM response for a standard Ni wire tip is 60 nm. The calculation was performed at a tip-to-sample

spacing of 50 nm. It also assumes the SMS tip to be rectangular with a thickness of 15 nm, width of 80 nm and a tip length of 1 μm, and the Ni wire tip to be cylindrical with a radius of 35 nm and a length of 1 μm. In both cases the magnetization was assumed to be parallel to the tip's axis due to shape anisotropy.

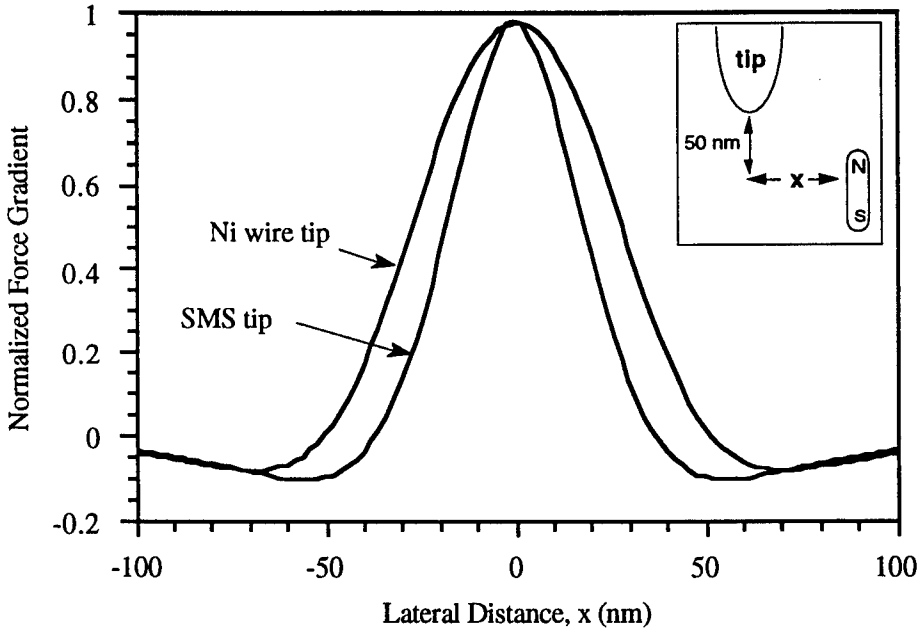


Figure 4.24. Response to a magnetic dipole for the SMS tip and a standard Ni wire tip. The FWHM responses are 40 and 60 nm for the SMS and Ni wire tips respectively. Simulation courtesy of M. Wei.[79]

The MFM imaging resolution can be further improved by reducing the tip-to-sample spacing. Figure 4.25 shows the FWHM response of the SMS and Ni wire tips (using the same geometry as before) to a magnetic dipole vs. the tip-to-sample spacing. For tip-to-sample spacings greater than about 100 nm, the responses of the two tips are similar. At a tip-to-sample spacing of 20 nm, however, the FWHM response of the SMS tip is nearly 20 nm, whereas the Ni wire tip is still ~70 nm. This demonstrates that the ultimate resolution of an MFM tip is limited by its size. The improved resolution of the SMS tip is a direct result of the reduced cross section of the magnetic tip and illustrates the significance of being able to control the size of the magnetic spike.

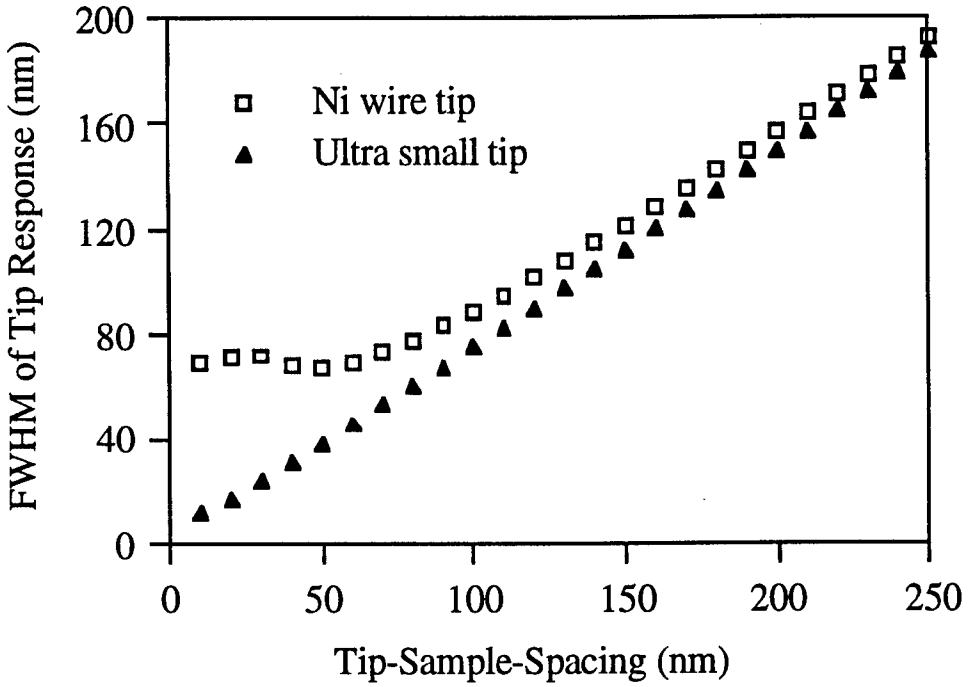


Figure 4.25. FWHM response of the SMS and Ni wire tips to a magnetic dipole for different values of tip-to-sample spacing. Simulation courtesy of M. Wei.[79]

Another advantage of the SMS tip is a smaller stray field compared to a conventional Ni wire tip (Fig. 4.26). The greatly reduced volume of magnetic material of the SMS tip results in a stray field of only 150 Oe at a distance of 50 nm, making the SMS tip better suited for studying soft magnetic material. Although conventionally coated tips in general also have a stray field smaller than that of a Ni wire tip due to a reduced magnetic volume [126], the SMS tips offer at least a 50% further reduction.

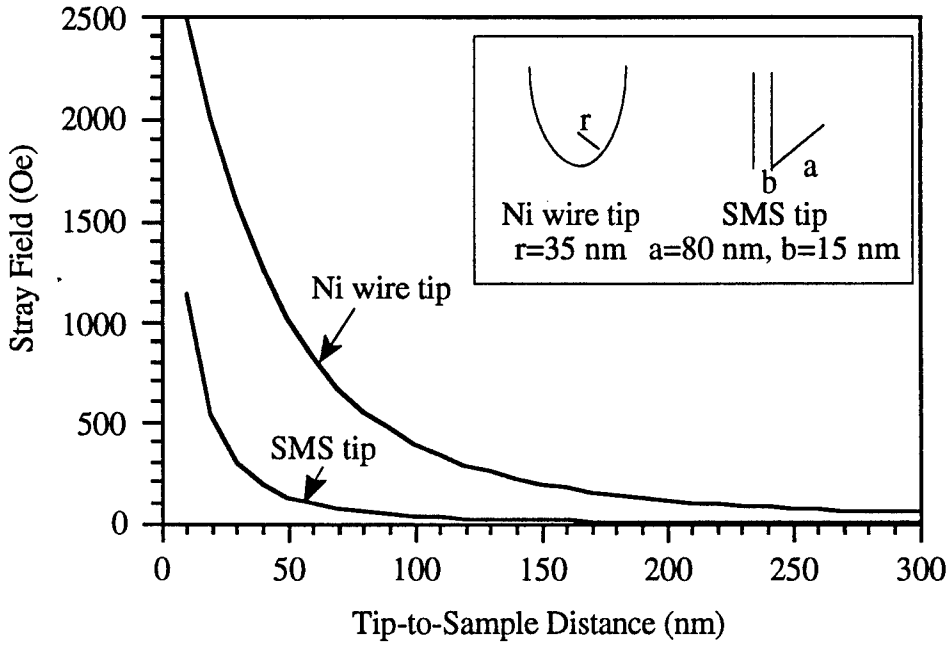


Figure 4.26. Stray field of SMS and Ni wire tips. Simulation courtesy of M. Wei.[79]

4.6 Summary

The utility of nanostructure engineering techniques was demonstrated by describing four distinct applications: the fabrication of quantum effect transistors, the fabrication of high speed photodetectors, the fabrication of 10 nm Si pillars to investigate light emission from silicon, and finally, the fabrication of test structures and novel tips for magnetic force microscopy.

Point contact quantum effect transistors have been fabricated using a mixed lithography scheme featuring electron beam lithography for the gate definition.

Quantization of the conductance of a one dimensional electron waveguide in units of $2e^2/h$ has been observed.

Nanofabrication techniques were also applied to the investigation of light emission from silicon. An experiment using sub-50 nm silicon pillars was conducted to ascertain the validity of the quantum model. Initial results show that it is possible to obtain photoluminescence from 20 nm diameter silicon pillars which are too large to expect appreciable confinement.

Lastly, the application of nanostructure engineering techniques to enhance the resolution in MFM images was also described. One approach is to deconvolve the tip response from the MFM image to enhance image resolution when tips with a large interaction volume, like etched wire tips, are used. The technique utilizes sub-100 nm wide, single domain nickel bars to obtain the tip impulse response. An alternative approach is to strictly limit the interaction volume of the tip in the first place. Electron beam deposition and shadow evaporation were used to fabricate single-domain magnetic spike tips.

These examples demonstrate the utility of nanostructure engineering using electron beam lithography not only to the creation of quantum effect and high speed electrical devices, but to the investigation of physical phenomena as well.

Chapter 5

Conclusions

This work has provided experimental techniques for fabricating structures as small as 10 nm using processes based on electron beam lithography. The utility of such fabrication techniques was evidenced by their application to such topics as high speed photodetectors, point contact quantum effect transistors, light emission from silicon, and magnetic force microscopy.

Three nanostructure fabrication techniques capable of achieving 10 nm features were described. Using electron beam lithography in conjunction with double shadow-evaporations and lift-off, two metal lines of 15 nm wide and 10 nm apart were fabricated on thick GaAs substrate.[52] The pitch size of the double metal lines is 25 nm, a factor of 2 smaller than the previous smallest pitch size on bulk semiconductors. This method is applicable for the fabrication of various lateral dual-gate electron quantum-interference transistors. A modified SEM has been used to fabricate gratings of 10 nm wide lines 30 nm apart, and quantum field-effect-transistor gates with 10 nm wide gaps over 300 nm long on bulk GaAs substrates using normal incidence evaporation and lift-off techniques.[53] Sub-50 nm overlay accuracy in multi-level e-beam lithography has also been achieved using the same modified SEM. The results demonstrate the effectiveness of modified SEMs in cutting-edge nanoscale device research in general, and the

resolution that can be achieved using NanoStructure Laboratory's modified SEM lithography system in particular. Lastly, a novel technique for fabricating free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15 using electron beam lithography, RIE, and subsequent HF wet etching was also presented.[54] These are among the smallest features fabricated using these techniques. It was found that the standard deviation of pillar diameters can be controlled to within ± 6 nm and is presently limited by the etch mask definition.

Nanofabrication techniques based on electron beam lithography have been applied to the creation of the fastest metal-semiconductor-metal photodetectors reported to date. Nanofabrication techniques are necessary to achieve the ultra-small finger spacings which allows such high speeds to be obtained. Using electron beam lithography with PMMA resists, normal evaporation, and lift-off techniques, MSM photodetectors with finger linewidths and spacings as small as 25 nm have been achieved.[62] Response bandwidths of up to 300 GHz have been achieved for transit time limited MSM photodetectors.

Point contact quantum effect transistors have been fabricated using a mixed lithography scheme featuring electron beam lithography for the gate definition. Quantization of the conductance of a point contact quantum effect transistor has been observed. Although the results are not unique, the emphasis here was on implementing a process sequence and measurement techniques for future projects.

Nanofabrication techniques were also applied to the investigation of light emission from porous silicon. An experiment using sub-50 nm silicon pillars was conducted to ascertain the validity of the quantum model. Photoluminescence was obtained from an ordered array of approximately 20 nm diameter silicon pillars.[54] This initial result suggests that the quantum model alone cannot fully account for PL from porous silicon.

Lastly, novel nanofabrication techniques were applied to fabricate nanoscale magnetic structures and a novel MFM tip. Arrays of nanoscale nickel bars were fabricated to remove tip effects from MFM images.[78] In addition, electron beam deposition and shadow evaporation were used to fabricate single-domain magnetic spike tips to improve MFM image resolution by strictly limiting the tip interaction volume in the first place.[79]

References

1. J. S. Kilby, "Semiconductor solid circuits", *Electronics* **32**, 110 (1959).

2. G. Watson, "Technology 1991 the main event", *IEEE Spectrum* **28**, 30 (1991).

3. B. J. v. Wees, H. v. Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouenhoven, D. v. d. Marel and C. T. Foxon, "Quantized conductance of point contact in a two-dimensional electron gas", *Phys. Rev. Lett.* **60**, 848 (1988).

4. D. A. Wharam, T. J. Thornton, R. Newbury, M. Pepper, H. Ahmed, J. E. F. Frost, D. G. Hasko, D. C. Peacock, D. A. Ritchie and G. A. C. Jones, "One-dimensional transport and the quantization of the ballistic resistance", *J. Phys. C* **21**, L209 (1988).

5. L. T. Canham, "Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers", *Appl. Phys. Lett.* **57**, 1046 (1990).

6. V. Lehmann and U. Gosele, "Porous silicon formation: A quantum wire effect", *Appl. Phys. Lett.* **58**, 856 (1991).

7. H. I. Smith, "A review of submicron lithography", *Supperlattices and Microstructures* **2**, 129 (1986).

8. D. B. Langmuir, "Theoeretical limitations on cathode ray tubes", *Proc. IRE* **25**, 977 (1937).

9. A. N. Broers, "Electron gun using long-life LaB6 cathode", *J. Appl. Phys.* **38**, 1991 (1967).

10. R. F. W. Pease, "Electron Beam Lithography", *Contemp. Phys.* **22**, 265 (1981).

11. L. Reimer, *Transmission Electron Microscopy* (Springer-Verlag, New York, 1989).

12. G. Leibmann, "A unified representation of magnetic electron lens properties", *Proc. Phys. Soc.* ***LXVIII*** , 737 (1955).

13. W. Chen and H. Ahmed, "Fabrication of 5-7 nm wide etched lines in silicon using 100 keV electron beam lithography and polymethylmethacrylate resist", *Appl. Phys. Lett.* **62**, 1499 (1993).

14. A. C. Ouano, in '*Polymers in Electronics* ', ACS Symp. Ser. No. 242, American Chem. Soc., Washington D.C., 1984, pp. 79.

15. M. A. Mohsin and J. M. G. Cowie, "Enhanced sensitivity in the electron beam resist poly (methyl methacrylate) using improved solvent developer", *Polymer* **29**, 430 (1988).

16. S. Mackie and S. P. Beaumount, "Materials and processes for nanometer lithography", *Solid State Technol.* **August**, 1985 (1985).

17. C. G. Wilson, in *'Introduction to Microlithography* ', ACS symp. Ser. No. 219, American Chem. Soc., Washington D.C., 1984, pp. 87.

18. H. Y. Liu, M. P. deGrandpre and W. E. Feely, "Characterization of a high-resolution novolack based negative electron-beam lithography resist with 4 $\mu C/cm^2$ sensitivity", *J. Vac. Sci. Technol. B* **6**, 378 (1988).

19. G. H. Bernstein, W. P. Liu, Y. N. Khawja, M. N. Kozicki and D. K. Ferry, "High-resolution electron-beam lithography in negative organic and inorganic resists", *J. Vac. Sci. Technol. B.* **6**, 2298 (1988).

20. L. Blum, M. E. Perkins and H. Y. Liu, "A study of key processing variables on the lithographic performance of microposit SAL601-ER7 resist", *J. Vac. Technol. B* **6**, 2280 (1988).

21. M. Isaacson and A. Murray, *J. Vac. Sci. Technol* **19**, 1117 (1981).

22. M. E. Mochel, C. J. Humphreys, J. A. Eades, J. M. Mochel and A. M. Petford, "Electron beam writing on a 20Å scale in metal B-aluminas", *Appl. Phys. Lett.* **42**, 392 (1982).

23. P. M. Mankiewich, H. G. Craighead, T. R. Harrison and A. H. Dayem, "High resolution electron beam lithography on CaF_2", *Appl. Phys. Lett.* **44**, 468 (1984).

24. W. Langheinrich, B. Spangenburg and H. Beneking, "Nanostructure fabrication using lithium fluoride films as an electron beam resist", *J. Vac. Sci. Technol. B* **10**, 2868 (1992).

25. E. Kratschmer and M. Isaacson, "Nanostructure fabrication in metals, insulators, and semiconductors using self-developing metal inorganic resist", *J. Vac. Sci. Technol. B* **4**, 361 (1986).

26. D. R. Allee and A. N. Broers, "Direct nanometer scale patterning of SiO_2 with electron beam irradiation through a sacrificial layer", *Appl. Phys. Lett.* **57**, 2271 (1990).

27. T. H. P. Chang, "Proximity effect in electron-beam lithography", *J. Vac. Sci. Technol.* **12**, 1271 (1975).

28. S. A. Richston and D. P. Kern, "Point exposure distribution measurements for proximity correction in electron beam lithography on a sub-100 nm scale", *J. Vac. Sci. Technol. B* **5**, 135 (1987).

29. S. V. Dubonos, B. N. Gaifillin, H. F. Raith, A. A. Svintsov and S. I. Zaitsev, "Evaluation, verification and error determination of proximity parameters alpha, beta, and eta in electron beam lithography", *Microelectronic Engineering* **21**, 293 (1993).

30. G. Owen and P. Rissman, "Proximity effect correction for electron beam lithography by equalization of background dose", *J. Appl. Phys.* **54**, 3573 (1983).

31. G. A. C. Jones, S. Blythe and H. Ahmed, "Very high voltage (500 kV) electron beam lithography for thick resists and high resolution", *J. Vac. Sci. Technol. B* **5**, 120 (1987).

32. Y.-H. Lee, R. Browning, N. Maluf, G. Owen and R. F. W. Pease, "Low voltage alternative for electron beam lithography", *J. Vac. Sci. Technol. B* **10**, 3094 (1992).

33. P. A. Peterson, Z. J. Radzimski, S. A. Schwalm and P. E. Russell, "Low-voltage electron beam lithography", *J. Vac. Sci. Technol. B* **10**, 3088 (1992).

34. M. A. McCord and T. H. Newman, "Low voltage, high resolution studies of electron beam resist exposure and proximity effect", *J. Vac. Sci. Technol. B* **10**, 3083 (1992).

35. W. M. Moreau, *Semiconductor Lithography Principles, practices, and materials* (Plenum Press, New York, 1988).

36. K. G. Chiong, M. B. Rothwell, S. Wind, J. Bucchignano and F. Hohn, "Resist contrast enhancement in high resolution electron beam lithography", *J. Vac. Sci. and Technol. B* **7**, 1771 (1989).

37. C. M. Horwitz, *Appl. Phys. Lett.* **32**, 803 (1978).

38. A. Ketterson, M. Tong, J.-W. Seo, K. Nummila, K. Y. Cheng, J. Morikuni, S. Kang and I. Adesida, "Submicron modulation-doped field-effect transistor/metal-semiconductor-metal optoelectronic integrated circuit receiver fabricated by direct-write electron-beam lithography", *J. Vac. Sci. Technol. B* **10**, 2936 (1992).

39. R. E. Howard, E. L. Hu and L. D. Jackel, *Appl. Phys. Lett.* **36**, 141 (1980).

40. R. Williams, *Modern GaAs Processing Techniques* (Artech House, Norwood, MA, 1990).

41. G. J. Dolan and J. H. Dunsmuir, "Very small ($\geq$ 20 nm) lithographic wires, dots, rings, and tunnel junctions", *Physica B: condensed matter* **152**, 7 (1988).

42. G. Mollenstadt and R. Speidel, "ElekronenoptischerMikroscreiber unter elektronenmikroskopischer Arbeitskontrolle", *Physikalische Blatter* **16**, 192 (1960).

43. A. N. Broers, J. M. E. Harper and W. W. Molzen, "250Å linewidths with PMMA electron resist", *Appl. Phus. Lett.* **33**, 392 (1978).

44. A. N. Broers, "Resolution limits of PMMA resist for 50 kV electrons", *J. Electrochem. Soc.* **12**, 166 (1981).

45. H. G. Craighead, R. E. Howard, L. D. Jackel and P. M. Mankiewich, "10-nm linewidth electron beam lithography on GaAs", *Appl. Phys. Lett.* **42**, 38 (1983).

46. F. Emoto, K. Gamo, S. Namba, N. Samoto and R. Shimizu, "8 nm wide lines fabricated in PMMA on Si wafers by electron beam exposure", *Jap. J. Appl. Phys.* **24**, L809-L811 (1985).

47. A. N. Broers, W. W. Molzen, J. J. Cuome and N. D. Wittels, "Electron-beam fabrication of 80 Å metal structures", *Appl. Phys. Lett.* **29**, 596 (1976).

48. S. Y. Chou and J. Boetcher, University of Minnesota, 1990.

49. 'DesignCAD', American Small Business Computers Inc.

50. P. Gaard, University of Minnesota, 1991-92.

51. J. Boetcher, P. B. Fischer and P. Gaard, University of Minnesota, 1991-1993.

52. S. Y. Chou and P. B. Fischer, "Double 15-nm wide metal gates 10 nm apart and 70 nm thick on GaAs", *J. Vac. Sci. Technol.* **B 8**, 1919 (1990).

53. P. B. Fischer and S. Y. Chou, "10 nm electron beam lithography", *Appl. Phys. Lett.* **62**, 2991 (1993).

54. P. B. Fischer, K. Dai, E. Chen and S. Y. Chou, "10 nm Si pillars fabricated using e-beam lithography, reactive ion etching, and HF etching", *J. Vac. Sci. Tecnol. B* **in press**, (1993).

55. S. Y. Chou, J. S. Harris and R. F. W. Pease, "Lateral resonant tunneling field-effect transistor", *Appl. Phys. Lett.* **52**, 1982 (1988).

56. S. Y. Chou, D. R. Allee, R. F. W. Pease and J. S. Harris, "Observation of electron resonant tunneling in a lateral dual-gate resonant tunneling field-effect transistor", *Appl. Phys. Lett.* **55**, 176 (1989).

57. D. C. Flanders, *J. Vac. Sci. Technol.* **16**, 1615 (1980).

58. D. C. Flanders, *Appl. Phys. Lett.* **36**, 93 (1980).

59. E. H. Anderson, C. M. Horwitz and H. I. Smith, *Appl. Phys. Lett.* **43**, 874 (1983).

60. D. E. Prober, M. D. Feuer and N. Giordano, *Appl. Phys. Lett.* **37**, (1980).

61. S. Y. Chou and Y. Wang, "Single-electron coulomb blockade in a nanometer field-effect transistor with a single barrier", *Appl. Phys. Lett.* **61**, 1591 (1992).

62. S. Y. Chou, Y. Liu and P. B. Fischer, "Tera-hertz GaAs metal-semiconductor-metal photodetectors with 25 nm finger spacing and finger width", *Appl. Phys. Lett.* **61**, 477 (1992).

63. A. Scherer and B. P. Van der Gaag, "Ion etching of ultra-narrow structures", *SPIE* **1284**, 149 (1990).

64. B. P. V. d. Gaag and A. Scherer, "Microfabrication below 10 nm", *Appl. Phys. Lett.* **56**, 481 (1990).

65. I. W. Rangelow and A. Fichelscher, "Chlorine or bromine chemistry in RIE Si-trench etching", *Proc. of SPIE* **1392**, 240-245 (1990).

66. M. Engelhardt, "Single crystal silicon trench etching for fabrication of highly integrated circuits", *Proc. of SPIE* **v. 1392**, 210 (1990).

67. G. C. Schwartz and P. M. Schaible, "Reactive ion etching of silicon", *J. Vac. Sci. & Technol.* **16**, 410 (1979).

68. A. Kassam, C. Meadowcroft, C. A. T. Salama and P. Ratnam, "Characterization of BCl3-Cl2 silicon trench etching", *J. Electrochem. Soc.* **137**, 1613 (1990).

69. M. Sato, S. Kato and Y. Arita, "Effect of gas species on the depth reduction in silicon deep-submicron trench reactive ion etching", *Jap. J. Appl. Phys.* **30**, 1549 (1991).

70. J. W. Coburn and H. F. Winters, "Ion- and electron-assisted gas-surface chemistry - An important effect in plasma etching", *J. Appl. Phys.* **50**, 3189 (1979).

71. M. Sato and Y. Arits, "Etched shape control of single-crystal silicon in reactive ion etching using chlorine", *J. Electrochem. Soc.* **134**, 2856 (1987).

72. N. I. Maluf, S. Y. Chou, J. P. Mcvittie, S. W. J. Kuan, D. R. Allee and R. F. W. Pease, "Effects of chromium on the reactive ion etching of steep-walled trenches in silicon", *J. Vac. Sci. & Technol. B* **7**, 1497 (1989).

73. T. S. Ravi, R. B. Marcus and D. Liu, "Oxidation sharpening of silicon tips", *J. Vac. Sci. Technol. B* **9**, 2846 (1991).

74. H. I. Liu, N. I. Maluf, R. F. W. Pease, D. K. Biegelsen, N. M. Johnson and F. A. Ponce, "Oxidation of sub-50 nm Si columns for light emission study", *J. Vac. Sci. Technol.* **B 10**, 2846 (1992).

75. C. Tsai, K. H. Li, D. S. Kinosky, R. Z. Qian, T. C. Hsu, J. T. Irby, S. K. Banerjee, A. F. Tasch, J. C. Cambell, B. K. Hance and J. M. White, *Appl. Phys. Lett.* **60**, 1700 (1992).

76. S. Y. Chou, Y. Liu and P. B. Fischer, "Fabrication of sub-50 nm finger spacing and width high-speed metal-semiconductor-metal photodetectors using high-resolution electron beam lithography and molecular beam epitaxy", *J. Vac. Sci. Technol. B* **9**, 2920 (1991).

77. S. Y. Chou and M. Y. Liu, "Nanoscale tera-hertz metal-semiconductor-metal photodetectors", *IEEE J. Quantum Electronics* **28**, 2358 (1992).

78. T. Chang, M. Legerquist, J.-G. Zhu, J. H. Judy, P. B. Fischer and S. Y. Chou, "Deconvolution of magnetic force images by fourier analysis", *IEEE Trans. Mag.* **28**, 3138 (1992).

79. P. B. Fischer, M. S. Wei and S. Y. Chou, "An ultra-high resolution magnetic force microscope tip fabricated using electron beam lithography", *J. Vac. Sci. Technol. B* **in press**, (1993).

80. B. J. v. Zeghbroeck, W. Patrick, J. M. Halbout and P. Vettiger, "105-GHz bandwidth metal-semiconductor-metal photodiode", *IEEE Electron Dev. Lett.* **9**, 527 (1988).

81. S. Y. Chou, Y.Liu, W. Khalil, T. Y. Hsiang and S. Alexandrou, "Ultra-fast nanoscale metal-semiconductor-metal photodetectors on bulk and low-temperature-grown GaAs", *Appl. Phys. Lett.* **61**, 819 (1992).

82. T. Y. Hsiang, S. Alexandrou, R. Sobolewski, S. Y. Chou and Y. Liu, Sub-picosecond characterization of nanometer-scale metal-semiconductor-metal photodiodes, CLEO'92 Anaheim, CA, May 1992),

83. J. R. Schreifer, in '*Semiconductor Surface Physics* ', University of Pennsylvania Press, Philadelphia, 1959, pp. 55.

84. R. Dingle, W. Wiegmann and C. H. Henry, "Quantum states of confined carriers in very thin $Al_xGa_{1-x}As$-GaAs-$Al_xGa_{1-x}As$ heterostructures", *Phys. Rev. Lett.* **33**, 827 (1974).

85. M. A. Reed and W. P. Kirk, Eds., *Nanostructure Physics and Fabrication* (Academic Press Inc., Boston, 1989).

86. D. Delagebeaudeuf and N. T. Linh, "Metal-(n) AlGaAs-GaAs two dimensional electron gas FET", *IEEE Trans. Electron Devices* **ED-29**, 955 (1982).

87. R. Landauer, "Can a length of perfect conductor have a resistance?", *Phys. Lett.* **85A**, 91 (1981).

88. M. Buttiker, Y. Imry, R. landauer and P. Pinhas, "Generalized many-channel conductance formula with application to small rings", *Phys. Rev. B* **31**, 6207 (1985).

89. C. W. J. Beenakker, H. v. Houten and B. J. v. Wees, "Skipping orbits, traversing trajectories, and quantum ballistic transport in microstructures", *Supperlattices and Microstructures* **5**, 127 (1988).

90. S. D. Mukherjee and D. W. Woodard, in *Gallium Arsenide* M. J. Howes, D. V. Morgan, Eds. (John Wiley & Sons, New York, 1985) pp. 119.

91. J. H. Davis and J. A. Nixon, "Fluctuations from random charges under a short gate in a narrow-channel MODFET", *Phys. Rev. B* **39**, 3423 (1988).

92. S. S. Iyer and Y.-H. Xie, "Light emission from silicon", *Science* **260**, 40 (1993).

93. H. Ennen, G. Pomrenke, A. Axmann, K. Eisele, W.Haydle and J. Schneider, "1.54 μm electroluminescence of erbium-doped silicon grown by molecular beam epitaxy", *Appl. Phys. Lett.* **46**, 382 (1985).

94. P. Buda, J. Kohanoff and M. Parrinello, "Optical properties of porous silicon: a first principles study", *Phys. Rev. Lett.* **69**, 1272 (1992).

95. A. J. Read, R. J. Needs, K. J. Nash, L. T. Canham, P. D. J. Calcott and A. Qteish, "First-principles calculations of the electronic properties of silicon wires", *Phys. Rev. Lett.* **69**, 1232 (1992).

96. D. J. Dimaria, J. R. Kirtly, E. J. Pakulis, D. W. Dong, T. S. Kuan, F. L. Pesavento, T. N. Theis, J. A. Curto and S. D. Brorson, "Electroluminescence studies in silicon dioxide films containing tiny silicon islands", *J. Appl. Phys.* **56**, 401 (1984).

97. S. Furukawa and T. Miyasato, "Quantum size effects on the optical band gap of microcrystalline Si:H", *Phys. Rev. B* **38**, 5726 (1988).

98. X.-l. Zheng, Dept. of Physics, SUNY Albany, 1992.

99. A. Uhlir, "Electrolytic shaping of germanium and silicon", *Bell System. Tech.* **35**, 333 (1956).

100. A. G. Cullis, L. T. Canham and O. D. Dosser, "The structure of porous silicon revealed by electron microscopy", *Mater. Res. Soc. Proc.* **256**, 7 (1992).

101. E. Basseous, M. Freeman, J.-M. Halbot, S. S. Iyer, V. P. Kesan, P. Munguia, S. F. Pesarcik and B. L. Williams, "Characterzation of microporous silicon fabricated by immersion scanning", *Mater. Res. Soc. Symp. Proc.* **256**, 23 (1992).

102. H. D. Fuchs, M. S. Brandt, M. Stutzmann and J. Weber, "Optical characterization of the visible photoluminescence from porous silicon", *Mat. Res. Soc. Proc.* **256**, 159 (1992).

103. R. P. Vasquez, R. W. Fathauer, T. George, A. Ksendzov and T. L. Lin, "Visible photoluminescence from silcon wafers subjected to strain etches", *Appl. Phys. Lett.* **60**, 1004 (1992).

104. S. M. Prokes, "Study of the luminescence mechanism in porous silicon structures", *J. Appl. Phys.* **73**, 407 (1993).

105. E. F. Steigmeier, B. Delley and H. Auderset, "Optical Studies on Silicon 'Quantum Wires'", *Physica Scripta* **T45**, 305 (1992).

106. E. Steigmeier, private communication, 1992.

107. H. I. Liu, D. K. Biegelsen, N. M. Johnson, F. A. Ponce and R. F. W. Pease, "Self-limiting oxidation of Si nano-wires", *J. Vac. Sci. Technol. B* ***in press***, (1993).

108. Y. Martin and H. K. Wickramasinghe, "Magnetic imaging by "force microscopy"with 1000 Å resolution", *Appl. Phys, Lett.* **50**, 1455 (1987).

109. F. Saurenbach and B. D. Terris, "Imaging of ferroelectric domain walls by force microscopy", *Appl. Phys. Lett.* **56**, 1703 (1990).

110. P. Gruetter, E. Meyer, H. Heinzelmann, L. Rosenthaler, H.-R. Hidber and H.-J. Gutherodt, "Application of atomic force microscopy to magnetic materials", *J. Vac. Sci. Technol. A* **6**, 279 (1988).

111. D. Rugar, H. J. Mamin, P. Guethner, S. E. Lambert, J. E. Stern, I. McFadyen and T. Yogi, "Magnetic force microscopy: General principles and application to longitudinal recording media", *J. Appl. Phys.* **68**, 1169 (1990).

112. C. Schoenenberger and S. Alvarado, "Understanding force microscopy", *Z. Phys. B* **80**, 373 (1990).

113. T. Chang and J.-H. Zhu, private communication, 1992.

114. S. Y. Chou, private communication, Oct. 1992.

115. D. Rugar, H. J. Mamin and P. Gruetter, "Magnetic force microscopy: general principles and application to longitudinal recording media", *J. Appl. Phys.* **68**, 1169 (1990).

116. J. F. Smyth, S. Schultz, D. R. Fredkin, D. P. Kern, S. A. Richston, H. Schmid, M. Cali and T. R. Koehler, "Hysteresis in lithographic arrays of permalloy particles: Experiment and theory (invited)", *J. Appl. Phys.* **69**, 5262 (1991).

117. G. A. Gibson, J. F. Smyth, S. Shultz and D. P. Kern, "Observation of the switching fields of individual permalloy particles in nanolithographic array via magnetic force microscopy", *IEEE Trans. Mag.* **27**, 5187 (1991).

118. A. Wadas, P. Gruetter and H. Guntherodt, "Analysis of bit patterns by magnetic force microscopy", *J. Vac. Sci. Technol. A* **8**, 416 (1990).

119. A. Wadas and P. Gruetter, "Theoretical approach to magnetic force microscopy", *Phys. Rev. B* **39**, 39 (1989).

120. U. Hartmann, "Theory of magnetic force microscopy", *J. Vac. Sci. Technol. A* **8**, 411 (1990).

121. T. Chang, M. Lagerquist, J.-H. Zhu and J. H. Judy, '1992.

122. D. Rugar, H. J. Mamin and P. Gruetter, "Improved fiber-optic interferometer for atomic force microscopy", *Appl. Phys. Lett.* **55**, 2588 (1989).

123. Y. Honda, S. Hosaka, A. Kikugawa, S. Tanaka, Y. Matsuda, M. Suzuki and M. Futamoto, "A Magnetic Force Microscope Using an Optical Lever Sensor and its Application to Longitudinal Recording Media", *Jpn. J. Appl. Phys.* **31**, L1061 (1992).

124. Y. Akama, E. Nishimura, A. Sakai and H. Murakami, "New Scanning Microscopy tip for measuring surface topography", *J. Vac. Sci. Technol. A* **8**, 429 (1990).

125. A. E. Ennos, "The origin of specimen contamination in the electron microscope", *Brit. J. Appl. Phys.* **4**, 101 (1953).

126. P. Bryant, S. Schultz and D. R. Fredkin, "Modeling the behavior of the magnetic force microscope", *J. Appl. Phys.* **69**, 5877 (1991).

Appendices

A. Computer Controlled Pattern Generator

This appendix describes some design details of the computer controlled vector scan pattern generator which consists of: a commercial CAD package to specify the exposure pattens, DesignCAD[49]; a custom computer program, Pattern Generator [50], to read the DesignCAD output files, generate the exposure coordinates, and control data output to the hardware; and custom hardware[51] designed to interface between the computer and the SEM. The system is based on a 50 MHz personal computer with 4 Mbytes of random access memory and MetraByte PDMA-32 direct memory access (DMA) card. The custom interface hardware (figure A.1) has a 14 bit achievable resolution. Exposure patterns can consist of arbitrary arrangements of lines, rectangles, polygons, circles, arcs, and text.

During an exposure, the Pattern Generator program reads the description of the next object to be exposed from the DesignCAD output file, generates a list of the pixels that need to be exposed, and stores these in a continuous block of random access memory. Once 8,000 coordinates have been calculated, or the object has been fully specified, the block of coordinates along with the exposure dose data, is passed to the DMA card. Since the DMA card is capable of transferring the coordinates to the interface hardware without directly involving the microprocessor, the computer program is able to calculate the second block of exposure coordinates while the first block is being exposed.

Three time constants are used to control the exposure process. The first is the object delay time. When the beam is moved to the starting point of a new vector, a object

delay is used to account for the inductive delay of the deflection. Experimentally, this delay is 4 msec. When new coordinate values are sent to the digital to analog converters (DAC), a second delay is used to allow the DACs to settle. This delay is 10-20 μsec. Once the beam has been moved to the desired location, the beam blanking is turned off for the specified exposure time, the third time constant.

The DMA card consists of two 8 bit digital memory output ports (A and B), three program controllable digital output lines (Aux1-3), and various handshaking lines for asynchronous data transfer (TimerGate, TimerOut, xfer. ack., and xfer. req.). The process of exposing a block of an object's coordinates is as follows. First, the exposure time to be used for the object is loaded into the DMA card's timer by program control. Next, the point settle time is output on port A of the DMA card, again through software control. Aux1 is then toggled to latch the value into the hardware. Then the data transfer is initiated by toggling Aux2 and then Aux3 through program control. At this time the computer program and microprocessor are no longer directly involved with the exposure process, and are free to calculate the next set of exposure points.

After Aux2 and 3 have been toggled, an asynchronous data transfer process between the interface hardware and the DMA card is started. As a result of Aux2 and 3 being toggled, the interface hardware toggles the transfer request line. The DMA card then loads the x coordinate onto the memory output ports, half on port A and half on port B, and toggles the data transfer acknowledge. The first time the data transfer acknowledge line is toggled, x coordinate is latched into the interface hardware's x-coordinate memory cell, and the data transfer request line is toggled once again. This time the y-coordinate of the data point is loaded onto the DMA output ports. The DMA card toggles the data transfer acknowledge line a second time which causes the y-coordinate to be latched into interface hardware's memory cell. In addition, the point settle circuit is activated.

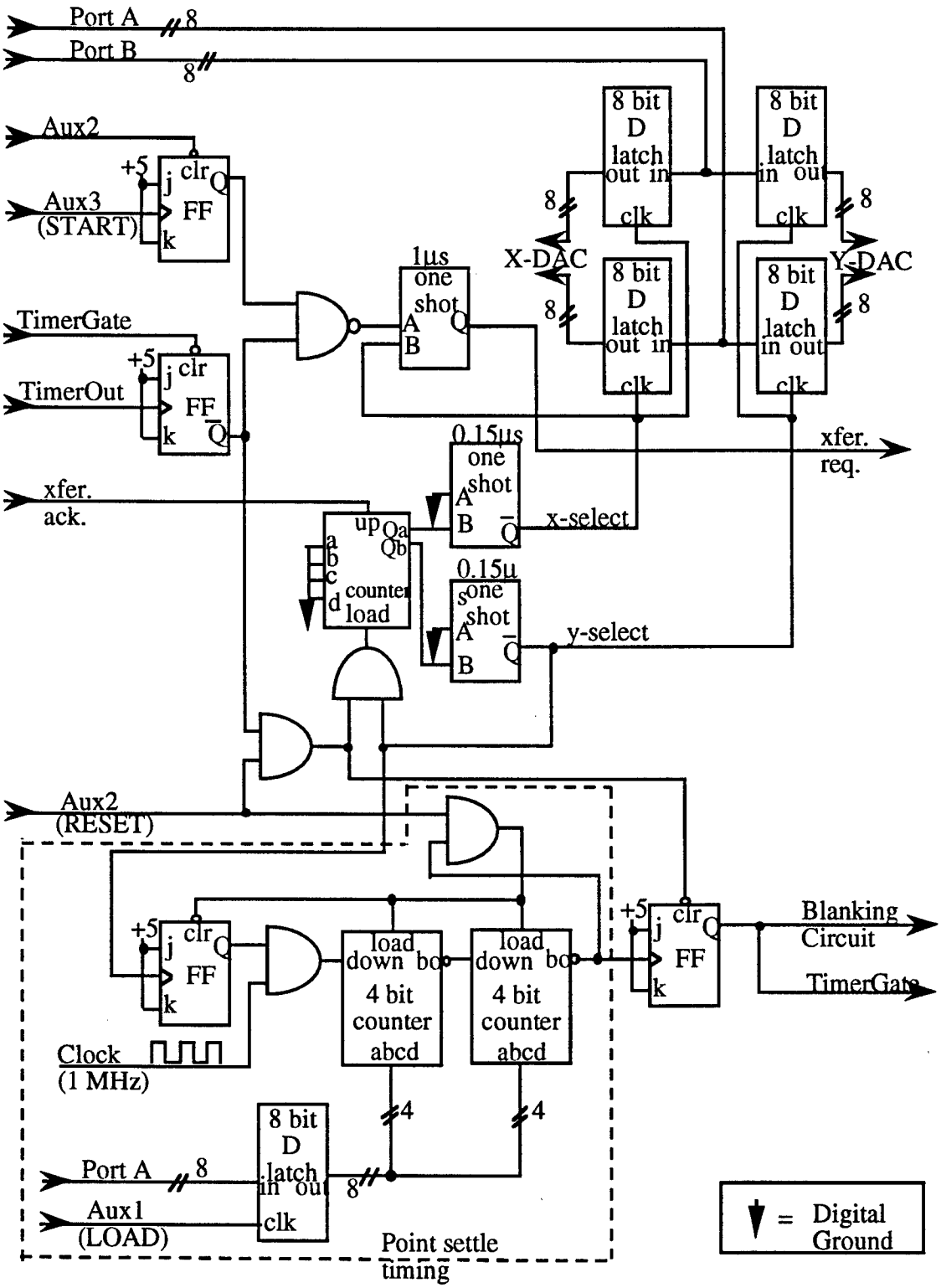


Figure A.1. Simplified schematic of DMA card interface circuitry. The Y-DAC and X-DAC outputs control the positioning of the electron beam. The beam blanking signal turns the beam synchronizes the beam blanking with the exposure process. All inputs are from the DMA card.

The point settle circuit consists of two four bit count down timers with a 1 MHz clock. Once this timer is activated, the rest of the circuit remains fixed until the timers reach zero. At that time the point settle counters are reset, the beam blanking is turned off, and the exposure timer (located on the DMA card) is activated. At the end of the exposure time, the DMA card toggles the TimerOut line which causes the interface hardware to blank the beam and toggle the data transfer request line. This causes the process to begin all over again. Once the DMA card has output all of the specified exposure points, it will stop toggling the data transfer acknowledge line and the process will stop.

B. MODFET Process Schedule

A. MBE Growth of Epitaxial Layers

Wafer Identification:_____

Location of flats:

Draw as wafer will be placed in aligner.
The flat should be vertical.

A1. Blank Etch

1. Wafer clean: trichloroethylene:acetone:methanol, 5 min each
2. Wet Etch: H_2SO_4:H_2O_2:H_2O 1:8:1000, 23°C, 591.7Å/min
   desired etch depth: _____
   etch time: _____
3. DI rinse 1 min.
4. Blow Dry, N_2

A2. Isolation

1. Wafer clean: trichloroethylene:acetone:methanol, 5 min each
2. photoresist AZ1400-31 5000 rpm 30 sec (1.6 μm)
3. prebake 20 min. 85-90 C
4. align and exposure: Karl Suss (___ sec) intens 1
   (0n 400 nm line)
5. develop 1:1 AZ developer: H_2O
   (20 sec after clearing)
   DI rinse 60 sec.
6. postbake 10 min. 90 C
7. Wet Etch: H_2SO_4:H_2O_2:H_2O 1:8:1000, 23°C, 591.7Å/min
   desired etch depth: _____
   etch time: _____
8. Strip resist with warm acetone/methanol.

B. Ohmic Contacts

1. Wafer clean: trichloroethylene:acetone:methanol, 5 min each
1. photoresist AZ1400-31 5000rpm 30s (1.6 μm)
3. prebake 15 min 90 C
4. chlorobenzene soak 5 min
5. Expose Karl Suss (___ sec) intens 1

6. develop AZ developer 1:1
   20 sec after clearing
7. HCL:H_2O (1:1) dip 30 sec.
   DI rinse 1 min.
8. metal evap: (see Ismail thesis)
   Ni 5 nm
   Au 5 nm
   Ge 25 nm
   Au 45 nm
   Ni 10 nm
   Au 50 nm
9. liftoff acetone squirt bottle (Methanal rinse), 2 cycles
10. annel ____°C for 1.5 min, Bio Rad Anealer (420 °C typical)

C. Nanometer Gate Fabrication
1. wafer clean, Tri/Acetone/Methanol
2. Bake Dry, 10 min 90C
3. Hexamethyldisilazane (HMDS) surface flood, 5,000rpm spin, 30 sec
4. Spin PMMA:

   Single layer, 950K, 2% PMMA 7000rpm, 60 sec 12 hour bake at 160°C
   OR
   Bilayer, 100k 3% PMMA 7000rpm 60 sec, 12 hour bake at 160°C
   950k 2% PMMA 7000rpm, 60 sec 12 hour bake at 160°C

5. UHREBL exposure, DO NOT USE B5 OR C5.

The following steps are to be performed immediately before depositing gate metal.

6. develop. 3:7 cellosolve:methanol 7 sec (critical) Temp: _____°C
   methanol 10 sec.(critical)
   iso 30 sec
7. Gate recess H_2SO_4:H_2O_2:H_2O 1:8:1000
   Rate = 575Å/min at 23°C
   Time: _____
   Temp: _____°C
8. Clean exposed surface: HCL:H_2O (1:1) 20 sec
   DI rinse, 30 sec
9. gate metal deposition (e-beam)
   Ti 15nm
   Au 15nm
10. acetone spray liftoff, methanol rinse

D. Final Metalization
1. wafer clean if necessary
2. photoresist Shipley 1400-31 5000rpm 30 sec (1.6 μm)
3. prebake 15 min 90°C
4. chlorobenzene soak 5 min
5. align and expose Carl Suss 17 sec , intesity 2
6. develop 1:1 AZ developer
   20 sec after clearing

The following step is to be performed immediately before depositing gate metal.

7. Clean exposed surface: HCL:H_2O 1:1 30 sec

DI rinse, 1 min

8. metal evap
   Ti 25nm
   Au 500nm
9. liftoff acetone squirt bottle, methanol rinse