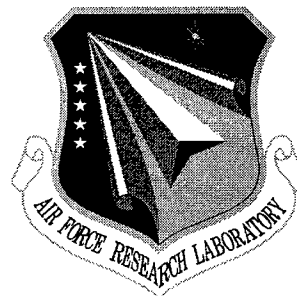


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OPTOELECTRONIC SYSTEMS FOR SPACE-VARIANT SIGNAL AND IMAGE PROCESSING

University of California, San Diego

Yeshaiahu Fainman and Paul E. Shames

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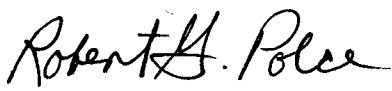
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OPTOELECTRONIC SYSTEMS FOR SPACE-VARIANT SIGNAL
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Yeshaiahu Fainman
Paul E. Shames

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Principal Investigator: Yeshaiahu Fainman
Phone: (619) 534-8909
AFRL Project Engineer: Kevin J. Whitcomb
Phone: (315) 330-8909

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1 Overview

This final report outlines the past year's study of an Optoelectronic system for space variant image and signal processing.

Space-variant transforms (SVT), such as the Hough transform¹ (HT), are useful in many image processing applications including radar detection² and data fusion³, topographical map analysis⁴ and autonomous robot control⁵. However, the implementation of SVT is computation and memory intensive⁶. Therefore, for efficient processing, all-electronic implementations have been developed using parallel multi-processor, such as pyramid⁷, mesh⁸, multi-ring⁹ and systolic array¹⁰, computer systems.

For SVT an attractive alternative to such all-electronic systems are optical systems that take advantage of the inherent parallelism of optics. Several such systems have been proposed, including the use of cylindrical¹¹ and micro-lenses¹², rotationally multiplexed³ and computer generated holograms¹⁴ (CGH). For digital processing, these systems utilize spatial light modulator (SLM) and detector (e.g. CCD) arrays for image input and output (I/O), respectively. We have implemented such a HT processing system using a matrix of CGH¹⁵. Each hologram in the array is designed to map a specific image pixel, displayed on an SLM, to the entire CCD pixel array. The HT for the entire image is pre-computed and pre-stored in the form of a CGH array, which is later accessed in parallel as an array of space-variant impulse response holograms. Therefore, the optical interconnection hologram can be seen as a page oriented optical memory. The speed and efficiency of the SLM and detector technology utilized dictate the SVT image processing time.

The realization of high-resolution real-time systems may require optoelectronic (OE) processing systems that utilize fast CMOS driver technology. In such a system, a VCSEL array and a smart-pixel focal plane array can be used for I/O, respectively, at high clock rates. In this report we investigate the practical implementation of such a system. In Section 2 we review space variant transforms and line detection using the Hough transform. In Section 3 we discuss a high-speed optoelectronic implementation of such transforms and in Section 4 we define the performance metrics we use to characterize the system. In Section 5 we compare the optoelectronic system to all-electronic parallel systems. In the last section we present a summary and conclusions.

2 Space Variant Transforms

A SVT affects each input point differently, and can be defined by a 2-D superposition integral

$$F(x,y) = \int \int_{-\infty}^{+\infty} f(\xi, \eta) h(x,y; \xi, \eta) d\xi d\eta, \quad (1)$$

where $f(\xi, \eta)$ is the input image to the SVT filter, $F(x,y)$ is the output image and $h(x,y; \xi, \eta)$ is the SVT filter impulse response. For SVT, the filter is dependent on the *absolute* position in the input plane and varies in the observation output plane. Examples of SVT used in machine vision and pattern recognition include the log-polar¹⁶, reciprocal wedge¹⁷ and HT.

2.1 Straight Line

In the HT each point from the image (input) domain is mapped into a parametric curve in the output (parameter) domain. As an example, we review a HT employed for detection of a straight line in normal parameterization. A straight line in the input domain is described by

$$f(x,y) = \begin{cases} 1, & (x,y) \in \rho_0 = x \cos \theta_0 + y \sin \theta_0 \\ 0, & \text{othe rwise} \end{cases}, \quad (2)$$

where ρ_0 is the shortest distance to the origin and θ_0 is the direction of ρ_0 (see Figure 1a). Therefore, the parameter domain is the distance-angle plane (θ, ρ) with Cartesian coordinates axes ρ and θ (see Figure 1b). In this case each input plane point (x_i, y_i) will be mapped into a sinusoidal curve in the (θ, ρ) domain

$$\rho = x_i \cos \theta + y_i \sin \theta. \quad (3)$$

Put in terms of the SVT of, Using Eq. (3) for designing the SVT filter, Eq. (1) can be rewritten yielding output parameter domain,

$$F(\rho, \theta) = \iint_{-\infty}^{\infty} \delta(\rho - x \cos \theta - y \sin \theta) f(x, y) dx dy. \quad (4)$$

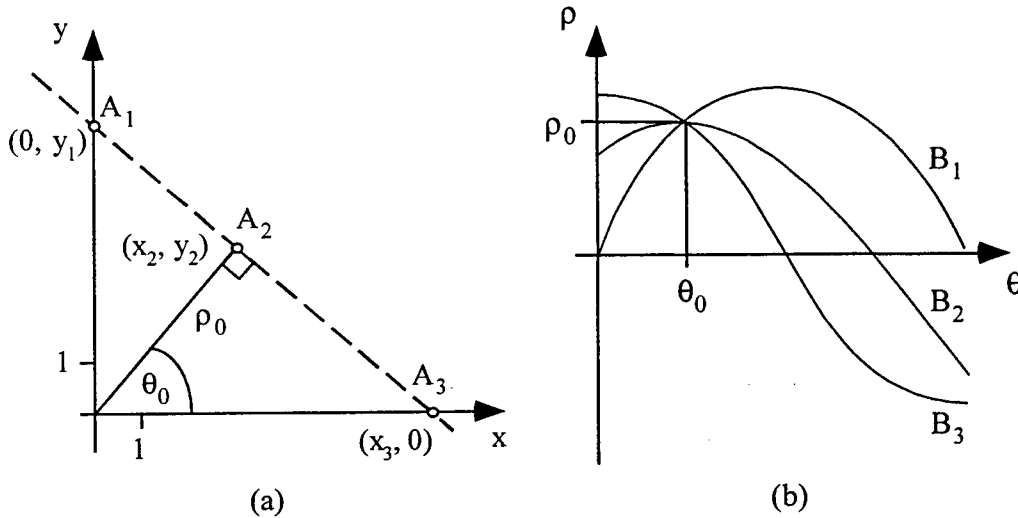


Figure 1. Normal parameterization of a straight line where the (a) input image plane has three points along a line and the (b) parameter plane has three corresponding curves intersecting at (θ_0, ρ_0) .

Each point in the input plane generates a sinusoidal curve in the output domain that spans all of the lines that may pass through that point. Sinusoidal curves that intersect in the parameter plane describe a line passing through at least two points in the input plane (see Figure 1b). Therefore, multiple points lying along the same line described by (θ_0, ρ_0) in the input will result in multiple curves intersecting in the parameter plane at the point (θ_0, ρ_0) . By taking the sum of the intersecting points, which corresponds to a measurement of intensity in an optical system, the strength (or number of points) on that line is determined.

2.2 General Ellipse

Parametric curves of more than two parameters will usually require a higher dimensional parameter domain. For example a circle is defined by three parameters (i.e. the coordinate of the center and the radius) so that the parameter domain is a 3-D space. Moreover, for the detection of a general ellipse which is a parametric curve described by five parameters (i.e. the coordinates of the center (x_0, y_0) the length of the two axis and the orientation, see Figure 2a), the parameter domain is a 5-D space. In this case, digital

computer implementations of the HT can become even more computing and memory intensive.

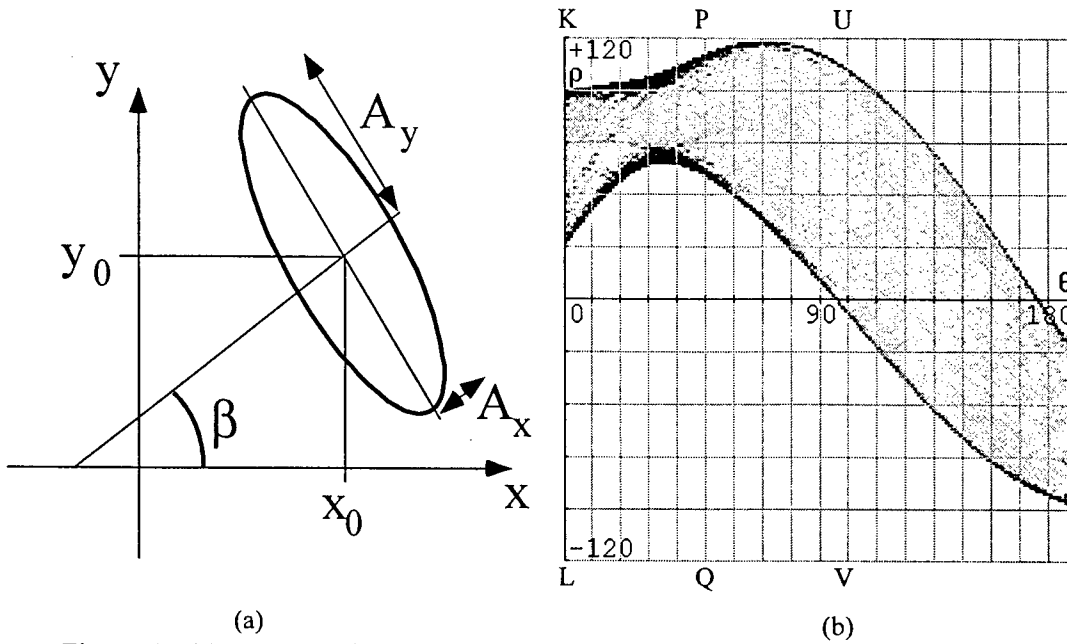


Figure 2. (a) Parameterization of a general ellipse. (b) Simulation of the HT parameter plane for $\theta = 0^\circ$: $\rho_K = 95$, $\rho_L = 25$; $\theta = 45^\circ$: $\rho_P = 110$, $\rho_Q = 60$; $\theta = 90^\circ$: $\rho_U = 113$, $\rho_V = 7$. Solving for the parameters using Eqs. (10) to (14) gives $x_0 = 60$, $y_0 = 60$, $\beta = 30^\circ$, $A_x = 20$ and $A_y = 60$.

We have recently demonstrated that it is possible to evaluate all five parameters of the general ellipse in a 2-D plane¹⁸ using a 2-D filter that implements the HT transform of a straight line in normal parameterization (Eq.(3)). An ellipse can be described by the following equations:

$$\begin{aligned} x &= x_0 + A_x \cos\beta \cos\alpha - A_y \sin\beta \sin\alpha \\ y &= y_0 + A_x \sin\beta \cos\alpha + A_y \cos\beta \sin\alpha \end{aligned} \quad (5)$$

where A_x and A_y are the two axis and x_0 and y_0 are the coordinates of the center of the ellipse, α is a parameter and β is the angle between the A_x axis of the ellipse and the x axis. We apply the HT for detection of a straight line in normal parameterization to this parametric equation by substituting Eq.(5) into Eq. (3) to get

$$\begin{aligned} \rho = & (x_0 + A_x \cos\beta \cos\alpha - A_y \sin\beta \sin\alpha) \cos\theta \\ & + (y_0 + A_x \sin\beta \cos\alpha + A_y \cos\beta \sin\alpha) \sin\theta. \end{aligned} \quad (6)$$

For detection, the amplitude distribution in the parameter domain consists of a superposition of curves that is described by Eq. (6) and is evaluated at α , which varies from 0 to 2π . Since ρ is a function of both θ and α for any given curve segment, the envelopes of the HT in the (θ, ρ) domain correspond to the extreme values, described by $\frac{\partial \rho}{\partial \alpha} = 0$ where ρ is given by Eq. (6), that are obtained by changing α at each θ . Evaluating this derivative and solving the resultant equation with respect to α we obtain:

$$\tan\alpha = \frac{A_y \tan(\theta - \beta)}{A_x}. \quad (7)$$

The equations of the curves that describe the envelopes (upper and lower) of the HT domain are obtained by substituting Eq. (7) in Eq. (6):

$$\rho_{envel} = x_0 \cos\theta + y_0 \sin\theta \pm \left[A_x^2 \cos^2(\theta - \beta) + A_y^2 \sin^2(\theta - \beta) \right]^{\frac{1}{2}}. \quad (8)$$

To solve for the 5 unknown parameters we evaluate Eq. (8) at three independent values of θ_i (where $i=1,2,3$) to obtain 6 independent equations. Here we choose $\theta_i = 0^\circ, 45^\circ, 90^\circ$ with the six corresponding points on the envelope K, L, P, Q, U, V:

$$\begin{aligned} \theta_0: \rho_{K,L} &= x_0 \pm \left[A_x^2 \cos^2\beta + A_y^2 \sin^2\beta \right]^{\frac{1}{2}} \\ \theta_{45}: \rho_{P,Q} &= \frac{\sqrt{2}(x_0 + y_0)}{2} \pm \left[\frac{A_x^2 + A_y^2}{2} + \frac{(A_x^2 - A_y^2)\sin 2\beta}{2} \right]^{\frac{1}{2}} \\ \theta_{90}: \rho_{U,V} &= y_0 \pm \left[A_x^2 \sin^2\beta + A_y^2 \cos^2\beta \right]^{\frac{1}{2}}, \end{aligned} \quad (9)$$

where ρ_K is the distance to the top and ρ_L to the bottom of the superposition envelope when $\theta = 0^\circ$ (see Figure 2b). Solving for the parameters we get five equations:

$$x_0 = \frac{\rho_K + \rho_L}{2} \quad (10)$$

$$y_0 = \frac{\rho_U + \rho_V}{2} \quad (11)$$

$$\beta = \frac{1}{2} \tan^{-1} \left[\frac{2(\rho_P - \rho_Q)^2 - (\rho_K - \rho_L)^2 - (\rho_U - \rho_V)^2}{(\rho_K - \rho_L)^2 - (\rho_U - \rho_V)^2} \right] \quad (12)$$

$$A_x = \left[\frac{(\rho_K - \rho_L)^2 \cos^2 \beta - (\rho_U - \rho_V)^2 \sin^2 \beta}{4 \cos 2\beta} \right]^{\frac{1}{2}} \quad (13)$$

$$A_y = \left[\frac{(\rho_U - \rho_V)^2 \cos^2 \beta - (\rho_K - \rho_L)^2 \sin^2 \beta}{4 \cos 2\beta} \right]^{\frac{1}{2}}. \quad (14)$$

One of the advantages of this parameterization is that for the detection of a general ellipse only three angles need to be sampled in the parameter plane. This parameterization and the corresponding detection is further simplified when $A_x = A_y$, i.e. the ellipse becomes a circle and when one of the axes goes to zero, e.g. $A_x = 0$, i.e. the ellipse becomes a line segment.

Parameterizations have also been developed that allow for the 2-D detection of a variety of geometric shapes, e.g. hyperbolic curves¹⁹, as well as the 2-D iterative detection of 3-D geometric shapes²⁰. The Generalized Hough Transform (GHT) has been developed for the detection of shapes that cannot be described analytically²¹. The GHT has also been developed for recognition of 3-D objects²².

3 Optoelectronic System Implementation

We have demonstrated an OE processing system using a 256x256 matrix of CGH filters for Hough transform, coordinate transform, and optical interconnects⁵. To construct the matrix of holograms, the CGH encoding of the SVT for each pixel position was displayed on a Hughes liquid crystal light valve (LCLV) and optically recorded, in the Fourier transform plane, onto Silver Halide holographic film. The image processing system, shown in Figure 3, used the LCLV to generate the input image plane, which is

imaged onto the matrix of holograms. The output is reconstructed onto the CCD camera using a Fourier lens.

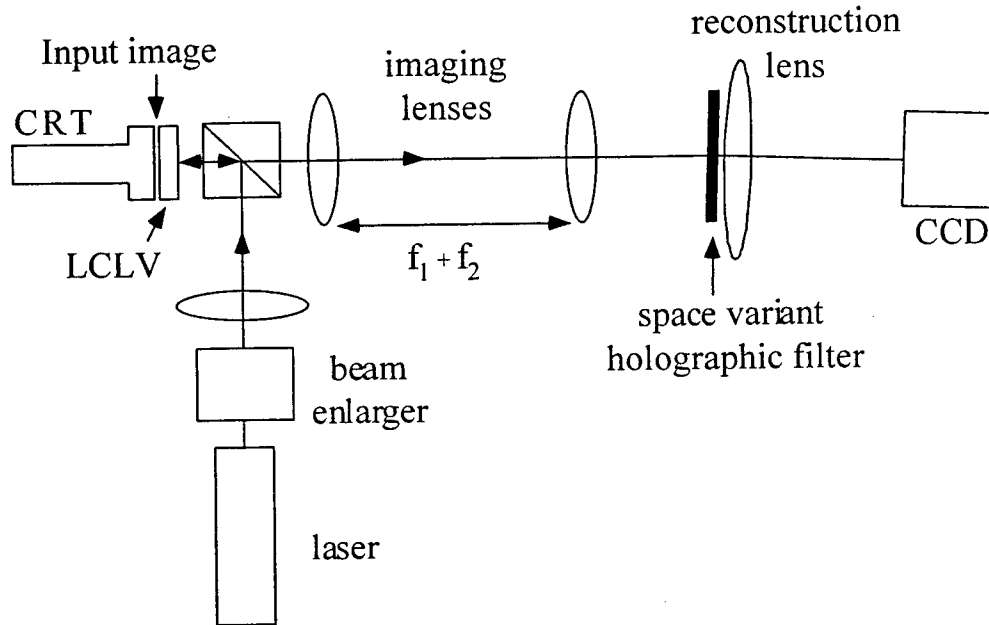


Figure 3. Optoelectronic system for space-variant image processing. A CRT and laser are used to generate the real-time image from the LCLV. The outputs from the holograms are reconstructed off-axis onto the CCD camera using a Fourier lens.

We have also demonstrated an OE HT image processing system, for detection of straight lines and ellipses, using a 64×64 matrix of computer generated holograms constructed using standard micro-lithography and fabrication techniques²³. To efficiently encode each CGH for the Fourier transform of the desired filter, we used a modified version of the direct binary search (DBS) method combined with the iterative Fourier transform algorithm²⁴. The four-phase level CGH was fabricated using a combination of e-beam and photo-lithography and chemically assisted ion beam etching. Each hologram contains 128×128 pixels, which are each $5 \mu\text{m} \times 5 \mu\text{m}$ (see Figure 4). The micro-fabricated CGH have the advantage of uniform holographic recording of each pixel as well as flexibility of CGH design, e.g. allowing for on-axis reconstruction.

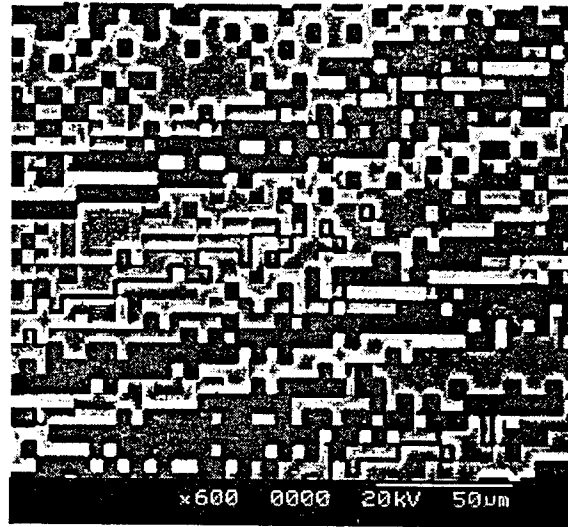


Figure 4. SEM micrograph of a portion of a CGH shows the 4-phase level structure fabricated on a quartz substrate.

Figure 5a-d show some example experimental results for our CGH based HT image-processing system. Figure 5a shows the video image of multiple 45° lines and Figure 5b shows the CCD image of the output plane of the CGH HT filter. The intensity maxima of the superposition of the multiple HT curves all lay on the $\theta = 45^\circ$ line and at the various values of ρ coinciding with the normal parameterization of each line. Figure 5c shows the video input image of an ellipse centered at the origin and Figure 5d shows the CCD image of the parameter plane. Notice the superposition envelope is symmetric about the θ -axis, which correctly corresponds to $x_0 = 0$ and $y_0 = 0$. The presence of a zero-order component in the center output images (bright spot) indicates imperfect reconstruction of the HT holograms due to CGH fabrication errors.

Next generation of optoelectronic systems will require fast I/O to perform real-time processing of high-resolution images on the order of 1024×1024 input pixels. Using VCSEL and smart focal plane arrays flip-chip bonded to CMOS drivers allow operation at low power with I/O clock rates greater than 150 MHz^{25} . The SVT of the input image to the output image is performed using diffractive and micro-optics. By using the same element spacing, the VCSEL and hologram arrays can be placed directly next to each other (see Figure 6). The refractive lens may also be replaced with an array of microlenses. Therefore, the components and subsystems can be packaged into a compact and

rigid optoelectronic system. Efficient packaging will also be able to take advantage of in-situ recording and self-assembly techniques.

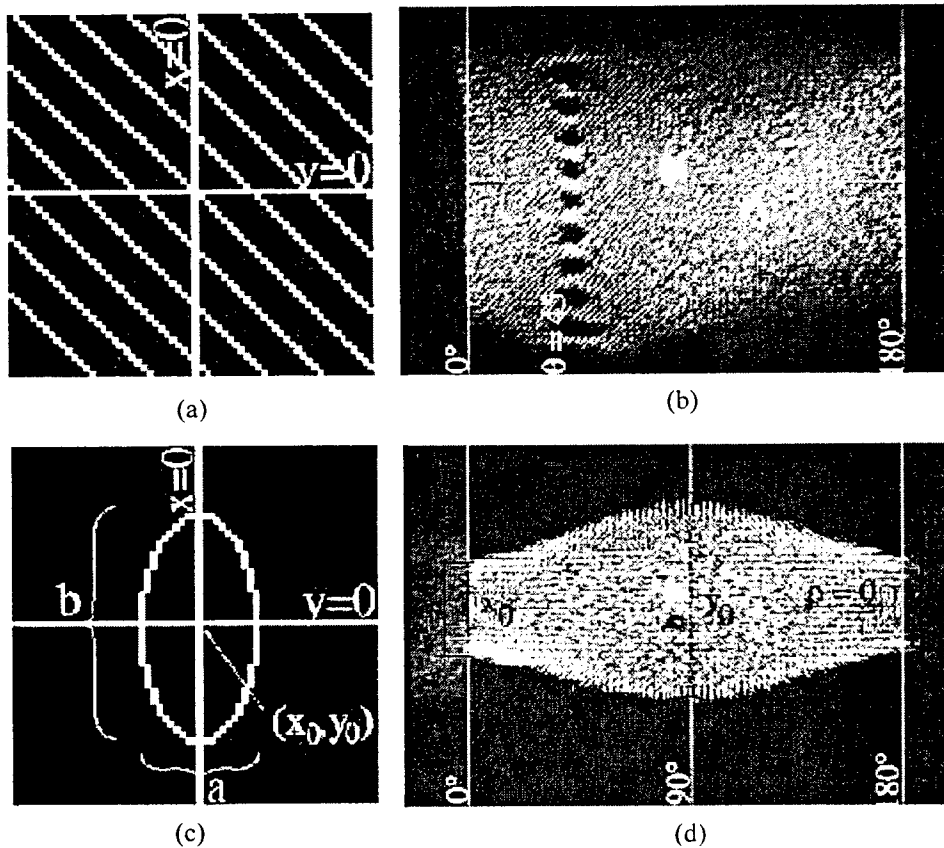


Figure 5. (a) Video input image shows multiple 45° lines and (b) output plane CCD image shows superposition of HT curves intersecting at $\theta = 45^\circ$. (c) Video image of ellipse centered at origin and (d) CCD output image.

The VCSEL array is expected to act as a partially spatially coherent quasi-monochromatic source. A unique feature of using these VCSEL arrays, as opposed to traditionally employed SLM implementations, is improvement of the SNR performance due to incoherent superposition at the output (e.g. reduced speckle noise). Tunability of VCSEL arrays would also enable using wavelength multiplexing of volume holography to pre-store multiple transforms, thereby allowing reconfiguration for efficiently implementing a number of SVT algorithms. Since such systems are generally used for line and shape detection (where missing pixels have a small effect on detection

efficiency), relatively low yield VCSEL arrays can be tolerated allowing for the use of large-scale arrays.

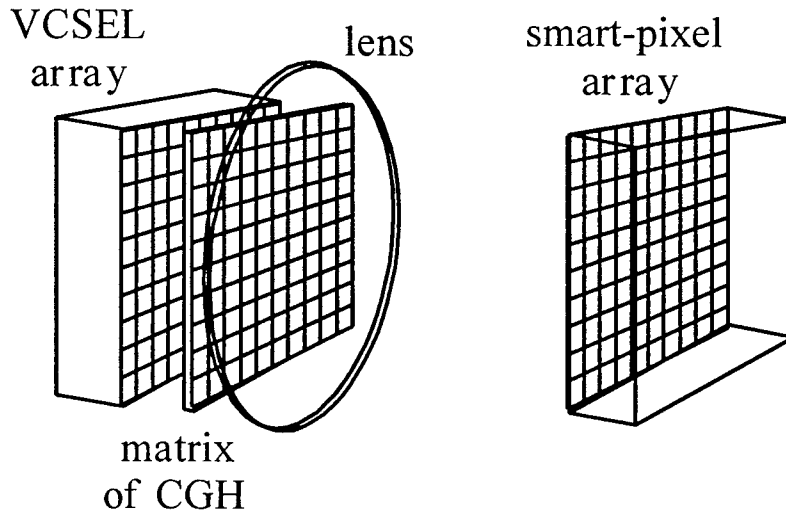


Figure 6. Optoelectronic SVT image processing system uses VCSEL and smart-pixel arrays bonded to CMOS drivers for fast I/O. The reconstruction lens can be replaced by diffractive micro-lenses, allowing for a more integrated and compact package.

4 Performance Metrics

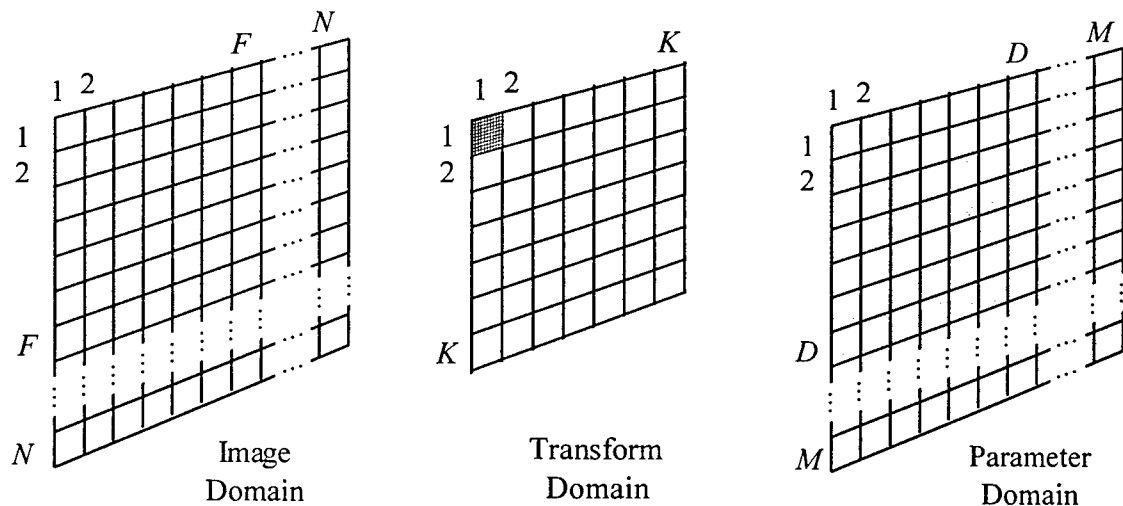


Figure 7. Dimensions of the image, transform and parameter domains. The dimension of the input image N can be greater than the VCSEL array dimension F . Likewise the output domain can be larger than the detector array, requiring some form of block-serial mapping.

In order to analyze the capabilities of such an OE processing system we define a set of performance metrics that can be compared to other existing SVT image processing systems. We begin by defining the dimensions of our system. Let the image (input) domain be of size $N \times N$, the transform domain is $K \times K$ and the parameter (output) domain be of size $M \times M$ (see Figure 7), where for simplicity we have assumed symmetric arrays. The VCSEL (SLM) array is of size $F \times F$ (i.e. the input image can have a different dimension than the VCSEL array) and the smart-pixel (detector) array is $D \times D$, then for a fully space variant transform $F = K$ and $F \leq D$.

4.1 Space Bandwidth Product

The dimensions F and K , the input image and output planes, will be constrained by the attainable pixel size of the CGH elements. Assuming the output from each VCSEL fills the area of its corresponding CGH, then the 2-D space bandwidth product (SBWP) of a single hologram can be given by $\text{SBWP}_{\text{single}} = D^2 C^2$ where C is the spatial encoding (e.g. for a 64×64 image, a single hologram with 128×128 pixels results in a spatial encoding $C = 2$). Therefore, for the entire matrix of holograms we obtain

$$\text{SBWP} = K^2 D^2 C^2. \quad (15)$$

We can also define the SBWP in terms of the physical dimensions of the matrix of holograms so that

$$\text{SBWP} = \left(\frac{l_h}{\delta} \right)^2, \quad (16)$$

where l_h is the length of the hologram matrix and δ is the size of each pixel in the CGH (minimum feature size). If we assume a SVT where $K = D$, then we can say

$$K = \sqrt{\frac{l_h}{C\delta}}. \quad (17)$$

For example, if we assume that the matrix of holograms has a length $l_h = 100$ mm, a minimum feature size $\delta = 1 \mu\text{m}$ and encoding $C = 6$, then $K, D \approx 128$ (i.e. the input/output can be of maximum dimension 128×128).

4.2 Footprint Area and Volume

The length of the system will depend on the size of each component as well as the distance between components. Assume each VCSEL has an aperture a and a pitch p , then the distance between the VCSEL array and holograms can be approximated by

$$z_{\text{CGH}} = \frac{p \cdot a}{2\lambda} \quad (18)$$

(assuming the VCSEL array pitch is equal to the pitch of the hologram array, then $p = \frac{l_h}{K}$). The distance from the reconstructing lenses to the output plane is given by

$$z_o = f = dF/\#, \quad (19)$$

where f is the focal length (if we assume a refractive lens, then the diameter $d > \sqrt{2}l_h$). Since each pixel is Fourier transformed onto the output plane, we can describe the size of the detector array by the relation $l_d = \frac{\lambda f}{\delta}$. The size of each detector in the smart-pixel array is $\delta_d = \frac{l_d}{D}$ and the active detection area is restricted to $\leq \delta_d^2$ (we assume a densely packed detector array with processing performed outside the detection area).

The product of its overall length and width gives the footprint of the system

$$S_F = z \cdot l = \left\{ (t_V + z_{\text{cgh}} + t_h + t_R + z_o + t_d)(l_{\text{max}}) \right\}, \quad (20)$$

where t_V , t_h , t_d and t_R are the thickness of the VCSEL, hologram and smart-pixel detector arrays and the refractive lens, respectively. Substituting from the relations above we get

$$S_F = \left\{ \left(t_V + \frac{\sqrt{l_h C \delta a}}{2\lambda} + t_h + t_R + \sqrt{2} l_h F/\# + t_d \right) (l_h) \right\}, \quad (21)$$

where we assume the maximum width to be of order l_h . If we continue to assume a symmetric system, then the volume of the system is defined by

$$S_V = \left\{ \left(t_V + \frac{\sqrt{l_h C \delta a}}{2\lambda} + t_h + t_R + \sqrt{2} l_h F/\# + t_d \right) (l_h)^2 \right\}. \quad (22)$$

Let's assume the VCSEL and smart-pixel arrays have thickness of 0.5 cm (including CMOS layer), the holographic array has thickness 0.1 cm and the refractive lens has a thickness of 1.0 cm. Also, we assume $F/1$, $\lambda = 0.980 \mu\text{m}$, $\delta = 1 \mu\text{m}$, $K, D = 128$ and $C = 6$. The hologram width will be $l_h = 10 \text{ cm}$, which gives a focal length $f \approx 14 \text{ cm}$. If the VCSEL diameter is $a = 3 \mu\text{m}$, then the distance between the VCSEL and hologram array $z_o = 1.1 \text{ mm}$. The total length of the system is $z \approx 16 \text{ cm}$, which results in a footprint of $S_F \approx 160 \text{ cm}^2$ and volume of $S_V \approx 1600 \text{ cm}^3$. From Eq. (21) we see that the system dimensions primarily depend on the size of each pixel, dictated by the minimum attainable feature size of the diffractive optical element (DOE), along with the $F/\#$ of the reconstruction lens. For example, reducing the pixel size to $\delta = 0.5 \mu\text{m}$ will reduce the total length to $z \approx 9 \text{ cm}$, the footprint to $S_F \approx 45 \text{ cm}^2$ and the volume to $S_V \approx 225 \text{ cm}^3$. On the other hand, using a $F/2$ lens will almost double the system dimensions. An attractive alternative to the thick refractive lens is to use a relatively thin diffractive lens (i.e. CGH) to perform the Fourier transform from the HT plane to the output plane.

4.3 Power Dissipation

To analyze the power requirements of the system we begin with the smart-pixel detectors. We can approximate the power requirements of each pixel by the relation

$$P_{\text{det}} = \frac{1}{R} \left(\frac{C_{\text{det}} dV}{dt} + I_{\text{leak}} \right), \quad (23)$$

where R is the responsivity. If we assume a leakage current $I_{\text{leak}} = 100$ pA, detector capacitance $C_{\text{det}} = 30$ fF and responsivity $R = 0.3$ A/W, then to get 10 mV at 500 MHz clock rate should require an incident optical power of $P_{\text{det}} \approx 0.5$ μ W. Dines²⁶ has shown that smart pixels operating at greater than 100 MHz clock rate require a detector area of only $50 \mu\text{m} \times 20 \mu\text{m}$ and less than 10 fJ of incident energy. At a 500 MHz clock rate this corresponds to $P_{\text{det}} \approx 5$ μ W. Since each VCSEL needs to power a minimum of 128 smart-pixels in the detector array, then assuming 50% efficiency of the DOE, the required optical power from the VCSEL is between $P_V = 0.1$ -1.0 mW. For low threshold VCSELs we can assume²⁷ a slope efficiency of 55% and a threshold current $I_T = 212$ μ A. Using the conservative upper-bound estimate $P_V = 1$ mW, then the required current per VCSEL is $I = 760$ μ A. Using 3V CMOS driving circuitry would require 2.3 mW of driving power. Since only one row is addressed at any one time, then for $N = 128$ where every pixel is in the 'on' state this corresponds to $P < 0.3$ W.

To determine the thermal performance of such a system we assume that the 0.3 W of power will need to be dissipated on the end surfaces. For $l_h = 10$ cm, the surface area of each end is $S_E = 100$ cm². Therefore the VCSEL array will need to dissipate approximately $3 \frac{\text{mW}}{\text{cm}^2}$. We can assume that the smart-pixel array will need to dissipate the same order of power²⁸ over a similar surface area (on the opposite side of the OE system).

4.4 Processing Time

The performance metric that can most easily be compared to alternative systems is the amount of time required to SVT process a single input image. For a CMOS driver operating at clock rate f , we can assume that the VCSEL response time is on the order of $\tau = \frac{1}{f}$. Using parallel-matrix addressing, i.e. where only one pixel per row can be

addressed at a time, then the load time of an input image is $\tau_K = \frac{K}{f}$. The smart-pixel

detection time can be described by $\tau_D = \frac{D+P}{f}$, where D is the number of rows in the

detector and P is the number of clock cycles required to perform some local processing and A-D conversion. The total processing time for $N = K$ is then given by the sum

$$T' = \frac{K + D + P}{f} \quad (24)$$

For a system where the dimension of the input domain is greater than the filter domain, $N > K$ (e.g. a large input image or wavelength multiplexed processing), then the system must perform some block-serial mapping and can be described by

$$T'' = \frac{K + D + P}{f} \left(\frac{N}{K} \right)^2. \quad (25)$$

Similarly, for a parameter domain larger than the filter domain, $M > D$ (e.g. for an asymmetric SVT), then the total processing time can be given by

$$T = \frac{K + D + P}{f} \left(\frac{NM}{KD} \right)^2. \quad (26)$$

For large image sizes we can assume that the number of clock cycles required for local processing is small compared to the image size, i.e. $P \ll K, D$. There are three cases that we will examine:

1. The input and output dimensions are equal to (or smaller) than the filter domain, i.e. $N = K = D = M$, then the total processing time reduces to

$$T_1 \approx \frac{2N}{f}. \quad (27)$$

2. The input dimension is larger than the filter dimension, i.e. $N > K$, then

$$T_2 \approx \left(\frac{N}{K} \right)^2 \frac{2K}{f}. \quad (28)$$

3. The input and output dimensions are larger than the filter dimension, i.e. $N > K$ and $M > D$. However, we will assume that the input and output are of the same dimension, i.e. $N = M$ and $K = D$, then

$$T_3 \approx \left(\frac{N}{K}\right)^4 \frac{2K}{f}. \quad (29)$$

In Figure 8 we have plotted the processing time for each of the three cases discussed and we see that there is an exponential increase in the processing time when the input/output sizes are larger than the holographic filter. For example, assume an input image of 512×512 and CMOS clock rate of 500 MHz. If the matrix of holograms is also 512×512 then the total processing time will be $T_1 = 2.0 \mu s$. However, for a SVT filter of size 128×128 , the processing time is increased to $T_3 = 130 \mu s$ (where the output is of dimension 512×512).

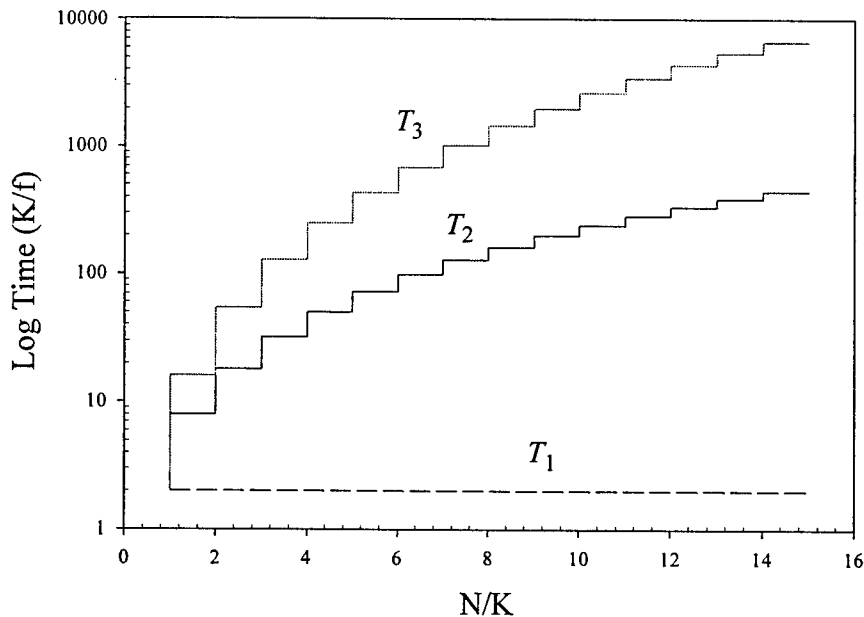


Figure 8. Log of computing time in units of K/f as a function of N/K .

4.5 Throughput

Another convenient measure of performance is throughput or the number of binary operations per second. Each bit (pixel) in the input plane is SVT mapped onto every pixel in the output plane, so the total number of operation can be described by

$$O = \frac{N^2 M^2}{T} = N^2 M^2 \left(\frac{f}{K+D+P} \right) \left(\frac{KD}{NM} \right)^2. \quad (30)$$

If we assume that $K = D$ and $P \ll K, D$, then this simplifies to

$$O \approx \frac{K^3 f}{2}. \quad (31)$$

For a filter of size 128×128 image and 500 MHz clock rate the number of binary operations is $O = 5.2 \times 10^{14} \frac{\text{bits}}{\text{sec}}$. This large bandwidth is representative of the parallelism of an optics-based processing system.

5 Comparison

For comparison of our proposed OE SVT image processing system to all-electronic systems, we will assume a relatively conservative OE system configuration that has a 128×128 VCSEL array for input, a 128×128 array of holograms for SVT filtering, a 128×128 smart-pixel detector array and CMOS circuitry operating at a 500 MHz clock rate. For such a system a 512×512 image will be SVT processed in approximately $130 \mu\text{s}$ and a 1024×1024 input image will be processed in 1.0 ms. A proposed OE system using ferroelectric liquid crystal¹¹ (FLC) input devices and CGH encoded HT filters is capable of processing a 512×512 image in 1 ms, limited by the speed of the SLM.

The all-electronic SYMPATI2, developed in 1992 by CEA/LETI/DEIN, which uses the single instruction multiple data (SIMD) architecture, employs 128 parallel processing elements (PE) reporting²⁹ the HT image processing of a 512×512 input image (for 512 angles) in approximately 1 second. CEA has also developed the second-generation SIMD

device. SYMPHONIE. Using 256 PE it is unofficially reported to be able to HT a 256×256 input image (for 256 angles) in 30 ms. There is also a 1024 PE SYMPHONIE, however no performance data is available on this device.

More recently, a HT board, utilizing a reconfigurable parallel architecture and two content addressable memory (CAM) chips, reported⁹ line extraction of a 256×256 input image in 76 ms. Using a reconfigurable multi-ring network (RMRN) architecture where each node is a T9000 transputer, the HT operation on a 1024×1024 input image is estimated⁹ at 14 seconds, using 128 nodes. Performing the HT for straight-line detection in a 512×512 input image (with 2048 angles) using the *Systola 1024*, a systolic array of 1024 processors implemented on a standard PCI board, took¹⁰ 0.25 seconds. This corresponds to a processing time of 62.5 ms for 512 angles.

An alternative to these electronic DSP methods for HT processing is a strictly memory lookup method. To analyze the performance for a HT processing system that uses a lookup table, i.e. storing the HT (θ, ρ) results for all (x, y) input points, we begin by defining the dimensions of the storage required. Assuming a binary $N \times N$ input image, then the input is N^2 bits. Each input point maps a sinusoidal curve to the output, i.e. N angles θ . For θ each we need a word of length $\log_2 N$ to distinguish between N possible ρ . Therefore, the total storage required is

$$S = N^3 \log_2 N \text{ Bits.} \quad (32)$$

Since each angle is independent, we divide the transforms by angle into multiple memory chips (R) (i.e. each chip determines $\theta = \frac{N}{R}$ angles), giving the storage for each chip

$$S = \frac{N^3 \log_2 N}{R} \text{ Bits.} \quad (33)$$

For $N = 1024$, the storage required is $S = \frac{10^{10}}{R}$ bits.

For a lookup method, the HT can be described by an algorithm consisting of the following steps:

1. Read input (x, y) value, assume 1 clock cycle.
2. Read HT (θ, ρ) value, 1 clock cycle.
3. Read existing output array value $(\theta_{old}, \rho_{old})$, 1 clock cycle.
4. Increment output array value $(\theta_{old}, \rho_{old})$, assume 2 clock cycles.
5. Write new output array value $(\theta_{new}, \rho_{new})$, 1 clock cycle.

In the steps described above we use assume that reading the input and memory resident values of the HT can be done in one clock cycle. Steps 3-5 can be described together as writing the new value to the correct position in the output array (see Figure 9). In total, we assume only six clock cycles at every angle for each input point.

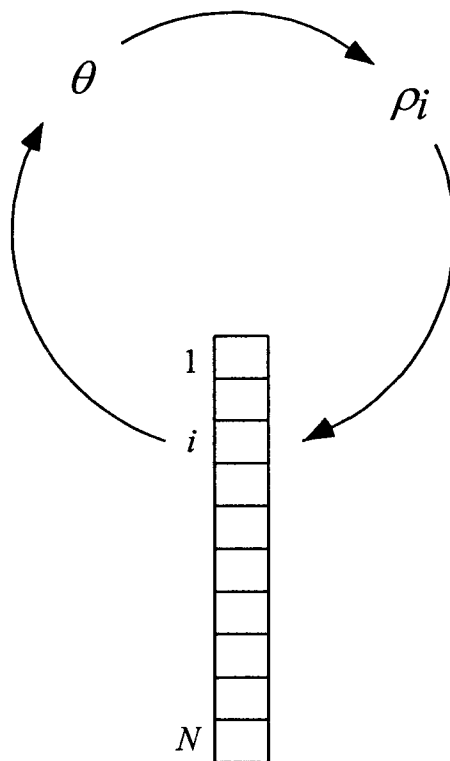


Figure 9. Increment of output array for each angle. The initial or existing array value is read, incremented and the new value written to the output array.

Therefore, we can estimate the total time required processing of an $N \times N$ input image to be

$$T = \frac{6N^3 \log_2 N}{Rf}, \quad (34)$$

where f is the clock rate of the memory chips and we assume that $R \leq N$. For comparisons to alternative systems we will assume our memory to be Rambus RDRAM chips, capable of operating on a word ($\sim \log_2 N$) in parallel at 1 Giga word per second average clock rate. Therefore, for $N = 512$, and assuming $R = 16$, the total processing time is $T \approx 0.05$ seconds and for $N = 1024$ the processing time is $T \approx 0.4$ seconds. To compare this lookup method with our proposed OE system we plot the processing times, using Eqs. (27), (28) and (34), in Figure 10. Comparing ideal systems, where $N = K, R$ the OE system increases its advantage in processing speed as the dimensions of the input image increase. However, for an OE system with a small number of holograms, the exponential increase in processing time decreases its advantage over the strictly memory lookup table system with a limited number of memory chips.

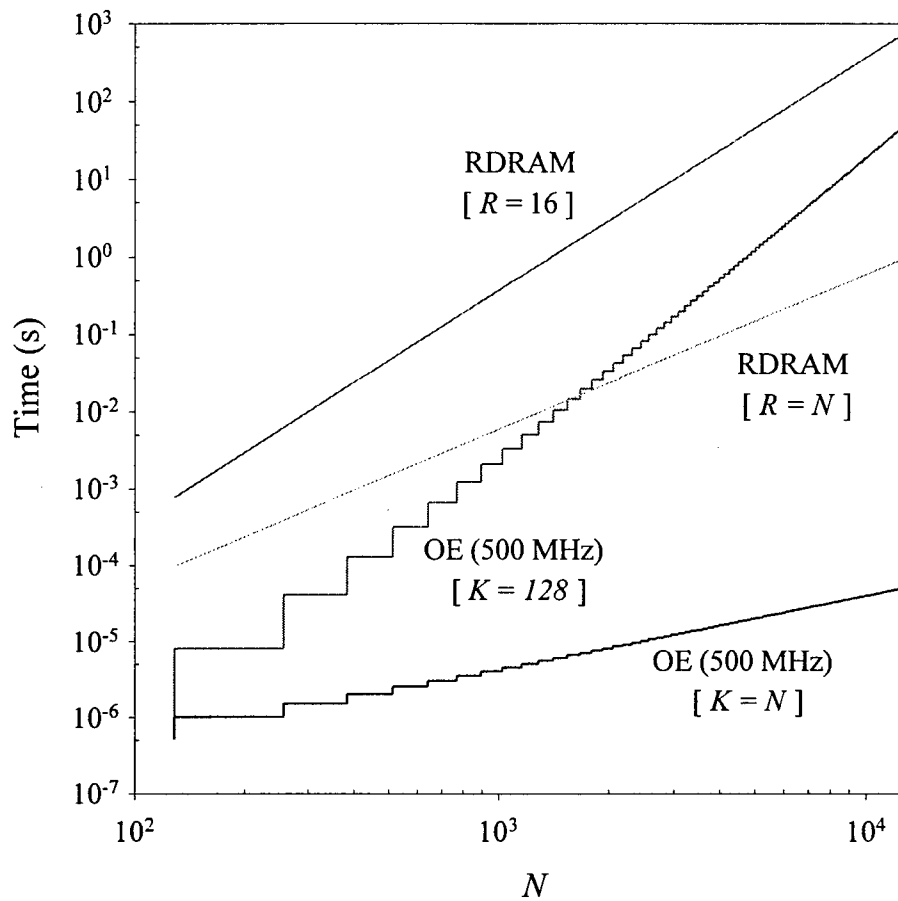


Figure 10. Log plot shows processing times for RDRAM memory resident and OE processing systems as functions of input image dimension.

| <i>N</i> | <i>128</i> | <i>256</i> | <i>512</i> | <i>1024</i> |
|--------------------|------------|------------|------------|-------------|
| SunSPARC20 | 15 s | | | |
| SYMPATI2 | 24 ms | | 1.5 s | |
| SYMPHONIE | | 30 ms | | |
| CAM | | 76 ms | | |
| RMRN | | | | 14 s |
| Systola 1024 | | | 62 ms | |
| RDRAM <i>R</i> =16 | 0.79 ms | 6.3 ms | 50 ms | 0.40 s |
| OE <i>K</i> =128 | 0.51 μs | 8.2 μs | 0.13 ms | 2.1 ms |

Table 1. Processing times, given in seconds, for various SVT image-processing systems. For comparison we computed a serial implementation of the HT on a SunSPARC20 workstation with a 100 MHz processor.

In Table 1 we compare the processing times for the various systems discussed above. The all-electronic systems can perform the HT on the order of milliseconds for images of

size up to 512×512 and on the order of seconds for larger input images. On the other hand, our proposed OE system can perform the HT on images of dimension 1024×1024 in a few milliseconds, required for real-time processing.

6 Conclusions

The research results of this study can be summarized as follows:

1. An optoelectronic SVT image processing system, using CMOS driven VCSEL and smart-pixels for I/O and a filtering performed by a matrix of computer generated holograms, has been presented.
 - The incoherence between pixels of a VCSEL based SLM can *improve* the SNR of the OE processing system compared to coherent SLM.
2. We have identified three SVT considered highly useful for image and signal processing: the Log-Polar, Reciprocal Wedge and Hough Transforms.
3. In order to analyze the strengths and weaknesses of our proposed OE system we defined a set of performance metrics. From this analysis we find:
 - The dimensions of the OE system are primarily constrained by the minimum feature sizes attainable using micro-fabrication techniques. However, using relatively conservative estimates our proposed system is highly compact ($S_F \approx 45 \text{ cm}^3$, $S_V \approx 225 \text{ cm}^3$) and can easily fit onto a portion of PC add-on board.
 - Since only one row is addressed at any one time, the power consumption of a 128×128 VCSEL array is a relatively low value of 0.3 W.
 - Using currently available VCSEL, smart-detector and CMOS technology our proposed OE processing system can perform HT on a 128×128 image in 0.51 μs . For larger images block-serial mapping can be used. Therefore, for a 1024×1024 input image a HT would take only 2.1 ms.

4. The exponential growth of the processing times for an OE system using relatively small arrays is the greatest limitation to SVT processing of very-large and high-resolution images.
 - However, since these systems can tolerate low yield VCSEL arrays, or even stitching of multiple small arrays, it may be feasible to have VCSEL or detector arrays on the order of 1024×1024 .
 - For an input image size of 1024×1024 into a SVT on an OE processing system with VCSEL, hologram and smart-pixel arrays all of dimension 1024×1024 (stitched or low-yield), the processing time is estimated at only 4.1 μ s.

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Appendix

A. 1. A matrix of 64x64 CGH for an optical Hough transform processor

S. Laut, F. Xu, P. Ambs and Y. Fainman

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A matrix of 64x64 Computer Generated Holograms for an optical Hough transform processor

Sophie Laut, Fang Xu*, Pierre Ambs, Yeshaiahu Fainman*

Université de Haute Alsace,
École Supérieure des Sciences Appliquées pour l'Ingénieur - Mulhouse (ESSAIM)
12, rue des Frères Lumière, 68093 Mulhouse cedex, France
e-mail : S.Laut@essaim.univ-mulhouse.fr, P.Ambs@essaim.univ-mulhouse.fr

*University of California, San Diego,
Dept. of Electrical and Computer Engineering
La Jolla, CA 92093-0407, USA
e-mail : fainman@ece.ucsd.edu

ABSTRACT

An optical implementation of the Hough transform (HT) based on a matrix of 64x64 four-level phase computer generated holograms (CGH) is described. The HT holograms are designed using a novel algorithm that combines the high speed of convergence of iterative Fourier algorithm (IFTA) with the high precision of the direct binary search (DBS) algorithm. The matrix of holograms was fabricated using standard microfabrication techniques: E-beam lithography, photolithography and chemically assisted ion beam etching. The fabricated elements were characterized experimentally and used in the HT processor, demonstrating practical application examples as real-time straight line, ellipse, circle detection, and other pattern recognition tasks.

Keywords: Hough transform, pattern recognition, computer generated holograms

1. INTRODUCTION

Hough transform (HT) techniques are widely used in pattern recognition tasks for detecting parametrized templates such as lines, line segments, circles and ellipses in binary edge images. A survey of the HT applications and realizations are presented by Illingworth *et al.*¹ and by Leavers². The HT maps the image space into a parameter space such that a peak occurring in the output parameter space means possible occurrence of a specific sought pattern in the input picture. The advantage of the HT in contrast to classical correlation techniques is its stability against noise and occlusion arising in digitized images. Although invented in 1962³, the HT method is still an active topic of research in the scientific community with more than 50 papers published in 1996. They concern military applications (such as target tracking⁴, robotics vision and autonomous vehicle navigation^{5,6}, etc.) as well as civil applications (such as medical imaging^{7,8}, geological analysis of grounds⁹, character recognition tasks¹⁰, supervision of the quality in industrial production¹¹, etc.).

The main part of these publications aims at improving time/memory space requirements that are consumed when pure electronic implementation is used for realization of the HT algorithm. Special mathematical techniques that reduce computation complexity have been developed to increase the speed of realizing the HT algorithm electronically (e.g., direction and amplitude gradient operators, contour following, etc.). However, as a consequence, such mathematical techniques may cause loss of accuracy in the results and lead to a coarser resolution. Some electronic implementations use specialized chips or specialized computers leading to high performance HT¹². However these processors not only remain expensive, but they are also slow when applied to large size images, thereby, limiting various real time applications. For example, implementation of HT for an image size $N \times N$ using a serial electronic computer will require thresholding a composite image resulting from a superposition of $N \times N$ images, each of size $N \times N$, thereby requiring $O(N^4)$ operation and $O(N^4)$ storage. A more expensive but better performing solution uses a parallel computer. A parallel electronic computer implementation of HT on a single instruction multiple data (SIMD) machine with a single processing element (PE) for each input image pixel will speedup the HT calculation by a factor of $O(N^2)$. However it is not realistic to assume that an array of PEs equal to the number of pixels in a high resolution will be realistic. For example, the SIMD machine SYMPATI2 designed by CEA/LETI/DEIN has an SIMD architecture with 128 PEs with an original concept of data distribution on the processors (helical addressing). In this configuration for a 512x512 pixel image the HT in 1 angular direction (angle θ fixed) is computed in 3 ms and for 256

directions this computing time becomes 0.5 sec. In comparison, the proposed optical implementation can achieve a higher processing speed. The input plane spatial light modulator (SLM) can be replaced by a ferroelectric SLM operating at 10 kHz and the output camera by an array of photodetectors. In contrast, optical implementation of HT algorithm is attractive because it resolves computation speed problems due to its inherent advantages in implementing interconnections in parallel and at very high speed. This paper describes an optical implementation of the HT using a matrix of computer generated holograms (CGH). The next Section briefly introduces the HT generally used for detecting straight lines in input patterns, followed by a review on optical implementations of HT. The design, fabrication and testing of the HT CGH are presented in Section 3. The optical HT processor employing the HT CGH as well as the experimental results are provided in Section 4, followed by concluding remarks in Section 5.

2. PRINCIPLE OF HOUGH TRANSFORM

2.1. Detection of a straight line

For detecting lines in the input images, a mapping between a Cartesian input plane (x,y) and a Cartesian normal parametrization output plane (θ,ρ) is used. The main advantage of this mapping lies in the regularity and uniformity of the parameters space in comparison with the slope-intercept representation.

Figure 1 illustrates the principle of normal parametrization of a straight line $f(x,y)$ defined in the input image plane by

$$f(x,y) = \begin{cases} 1, & (x,y) \in \rho_0 = x \cos \theta_0 + y \sin \theta_0 \\ 0, & \text{otherwise} \end{cases} \quad (1)$$

where ρ_0 is the shortest distance from the line to the origin and θ_0 is the angle of ρ_0 with respect to the x-axis.

The HT image $F(\theta,\rho)$ corresponding to input image $f(x,y)$ is defined by the equation

$$F(\rho,\theta) = \iint_{-\infty}^{+\infty} f(x,y) \cdot \delta(\rho - x \cos \theta - y \sin \theta) dx dy \quad (2)$$

where $\delta(\rho - x \cos \theta - y \sin \theta)$ is a delta-function describing the HT point spread function (PSF).

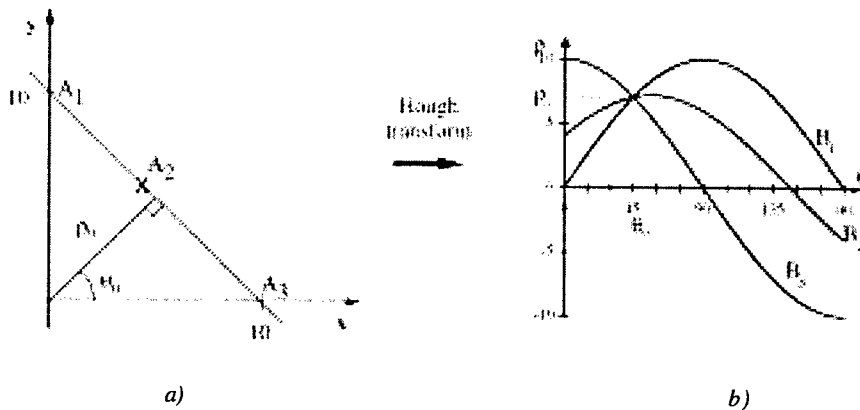


Figure 1: Principle of the straight-line HT in normal parametrization: a) input plane b) parameter domain plane

The principles of HT are summarized in Figure 1 where for each point A_i with coordinates (x_i, y_i) in the image space, there is a corresponding sinusoidal curve B_i in the (θ, ρ) parameter space. Collinear points A_1, A_2, A_3 give rise to curves that intersect in the output plane at one point (θ_0, ρ_0) , which characterizes the parameters of a line defined by these collinear points. This intersection is counted in an array of accumulator cells that performs quantization and storage of the parameter space. Thus, the parameters of a line in the input plane are detected using a thresholding operation in the parameter domain.

1.2. Detection of higher order parametric curves

Parametric curves described by more than two parameters will usually require a higher than two dimensional parameter domain. For detecting a general ellipse described by five parameters (i.e., the coordinates of the center (x_0, y_0) , the length of the two axis a, b , and the orientation ϕ), the parameter domain requires a 5-D space. In the same way, a circle needs a 3-D parameter space (i.e., the coordinates of the center (x_0, y_0) and the radius r). However it has been shown¹³ that a 2-D mathematical description of higher order parametric curves such as ellipse or circle is possible in a Cartesian normal parametrization output plane (θ, ρ) . In that case, the superposition of the sinusoidal curves no longer intercepts in one point. They rather form a pattern with an envelope that needs to be analyzed at different positions in the output plane to extract the parameters of the input template curve. However we choose to restrict our present study to detection of circles and ellipses oriented at 0° or 90° ; the general case of an ϕ -oriented ellipses detection is explained in¹³. The four parameters of such an ellipse, i.e. coordinates of the center (x_0, y_0) and the two axis a and b are determined from the four measured coordinates of the two envelopes in the HT plane at two θ -locations : $\theta=0^\circ$ and $\theta=90^\circ$ (see Figure 2). For the circle case, the two ellipse axis parameters will appear equal, $r=a=b$.

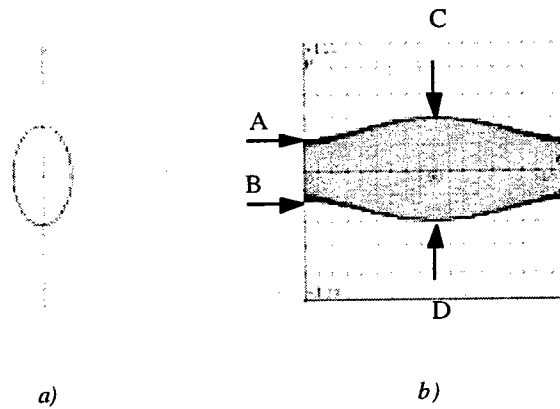


Figure 2: HT for detecting an 90° -oriented ellipse: a) input ellipse b) simulation of the HT parameter plane. Coordinate of the center: $x_0 = (A + B)/2$, $y_0 = (C + D)/2$; Length of the two axis: $a = (A - B)/2$, $b = (C - D)/2$.

1.3. Optical implementation of the Hough transform

Various methods for the optical implementation of the HT have already been described in the literature. One type of implementation uses mechanically rotating parts which are limiting the processing speed^{14,15}. Roux has introduced a HT processor based on a coordinate transform CGH¹⁶. Casasent *et al.* have proposed several optical systems for the implementation of the HT^{17,18,19}. One of these implementations uses a CGH consisting of pairs of cylindrical lenses oriented at different angles^{20,21}. In this case, each pair of lenses is computing the HT in one specific angular position. The parameter domain is in a polar coordinates format which may cause difficulty for practical realizations using conventional optoelectronic detector arrays. Moreover, this output plane format makes any cascading unrealistic. However this implementation needs a smaller space bandwidth product (SBWP) for the CGH, although it introduces a disadvantage of variable resolution in θ and ρ in the parameter domain.

In this manuscript, we focus on the principle and the realization of the HT using a two-dimensional array (i.e., matrix) composed of CGHs. In this case, for each input pixel with coordinates (x_i, y_j) , we use a corresponding CGH which reconstructs in the Hough transform plane the corresponding sinusoidal curve,

$$\rho = x_i \cos \theta + y_j \sin \theta \quad (3)$$

Thus the HT of an input image is obtained from intensity summation of the PSFs reconstructed from the hologram corresponding to each input image pixel (see Figure 3). Since the HT is a space-variant transformation, each hologram in the array is different from its neighbors.

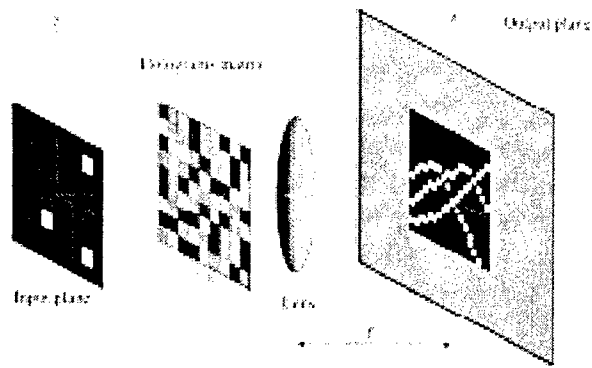


Figure 3: Principle of the optical HT processor using a CGH matrix.

Our approach is unique because it introduces an advantageous solution to the computation intensive procedures involved in implementing electronically space-variant transformations in general, and HT in particular. Such an optical processor represents a compact and motionless implementation, involving a simple and packageable optical system. This implementation is the most closely related to the numerical implementation on electronic computers. With our approach, we anticipate obtaining results similar to electronic realizations in terms of accuracy, but at a much higher speed.

The main advantage of our processor lies in its flexibility and versatility. Such a matrix can implement detection of numerous primitive patterns (e.g., circles, ellipses, and straight lines) by properly analyzing the parameter domain. Furthermore, detection of an object in specific angular positions can be achieved by a local observation in the parameter domain. Cascadability of the processor is also possible because the output parameter domain can be arbitrarily tailored at the design stage to meet the requirements of the next stage in the cascade. Ambs *et al.*^{13,22,23} have already presented an optical HT implementation using a two-dimensional array of holograms. However, the quality of the optically recorded holograms (i.e., uniformity of the diffraction efficiency for each hologram) was not easy to control. In order to solve this problem, we propose and report in this paper the design fabrication and testing of a matrix of 64x64 CGHs using a novel encoding method. In the following section, we describe the realization of the HT CGH array.

3. DESIGN AND FABRICATION OF THE HT CGH MATRIX

3.1. Principle of HT CGH design

Diffraction optics has made significant progress during the recent years due to the advances in microfabrication technologies and developments in rigorous numerical modeling as well as CGH iterative design algorithms such as iterative Fourier transform algorithm (IFTA)^{24,25} and direct binary search (DBS)²⁶. These advances make high performance diffractive optical elements possible.

The HT implementation using an array of CGH elements imposes some constraints. For example, each hologram must have the same performance characteristics (diffraction efficiency, uniformity of the reconstructions in intensity, and high contrast); for most applications, the number of holograms must be equal to the input plane resolution, with the size of each hologram determined by the chosen resolution in the parameter plane. For this research, a 64 x 64 CGH matrix was realized, reconstructing a 65x65 parameter space, enabling a larger domain of application in comparison with other studies²⁷. In order to obtain a maximal diffraction efficiency, four-phase level Fourier transform holograms have been employed. The absence of the complex conjugate order in the reconstructions allows us to use a smaller space-bandwidth product of the holograms (128x128 pixels for a 65x65 pixel reconstruction size). These holograms were designed by a computer using a novel method based on combining the advantages of the iterative algorithms IFTA and DBS.

IFTA is an iterative technique based on the Gerchberg & Saxton algorithm²⁸. The principle of this method^{24,25} consists in performing successive iterations between the object image plane and the spatial spectrum plane, each followed by a constraint on the CGH. To make the spectrum quantization process easier, it needs to be uniform, which is achieved in our algorithm by employing an equalizer. The equalizer uses the degrees of freedom in space and phase²⁹.

The DBS algorithm presented by Seldowitz *et al.*²⁶ is based on the optimization of an error criterion using a Monte Carlo technique. At the initial stage we generate a random hologram and compute the error between the desired image and the reconstruction of this hologram. The pixels of the random CGH are then scanned and changed in a certain order and a new error is computed. The pixel's value modification is retained only if the error decreases and the error criterion is therefore minimized. In comparison with IFTA, the DBS algorithm gives better results in term of the error of reconstruction. However it is much more time consuming than IFTA (by a factor of 20 approximately). In fact, for the HT holograms calculations, we combine the speed of convergence of IFTA with the accuracy of the DBS techniques. The algorithm for HT CGH design can be summarized as follows : first an iterative spectral equalizer is applied to the desired reconstruction of the CGH. Then the hologram is calculated using IFTA followed by a few DBS iterations which allow to increase the signal to noise ratio (SNR). The total time required for the computation of a 64x64 array of holograms is about one month with an IBM RS 6000 340 workstation, with the mean time for one hologram of about 700 sec. Computer simulation results provide a mean diffraction efficiency of about 50%, with a standard deviation of 1.8% and an SNR in intensity of 250, with a standard deviation of 87. Figure 4 shows one hologram of the matrix and the simulation of its reconstruction.

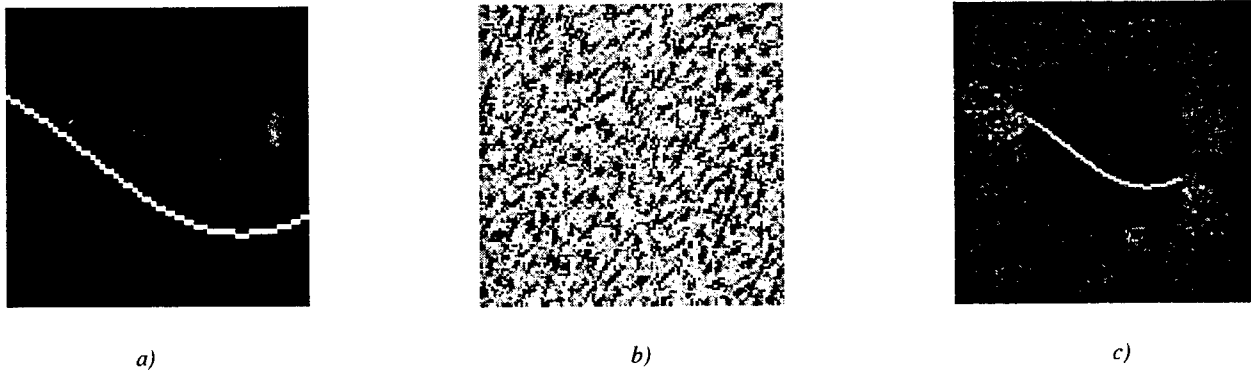


Figure 4: a) a specific PSF of the HT matrix. Desired reconstruction of the CGH corresponding to the illumination of one specific point with coordinates (18,15) with respect to the origin located in the center of the input plane. b) 4-level-phase CGH. c) Simulation of the CGH reconstruction.

3.2. Fabrication of the HT matrix of CGHs

The 4-phase-level Hough transform matrix hologram was fabricated on a quartz substrate ($n=1.457 @ 0.633 \mu\text{m}$) using standard microelectronics fabrication technologies: electron beam lithography defined the two mask patterns that are necessary to make the 4-phase-level elements, photolithography transferred the mask patterns into photoresist that served as etching masks. The surface relieves in the quartz substrate was etched using chemically assisted ion beam etching with CHF_3 in the etching chamber. The two etch depths were measured to have less than 2% errors. The feature size of each pixel is $5 \mu\text{m}$ and the misalignment between the two patterns was about $0.2 - 0.4 \mu\text{m}$. Figure 5 shows the micrographs of the fabricated CGH taken by a scanning electron microscope. The main fabrication error was due to over exposure/development for the second pattern (π phase delay). This error caused the linewidth reduction of the second pattern (see Figure 5) and increased the unwanted zero order efficiency.

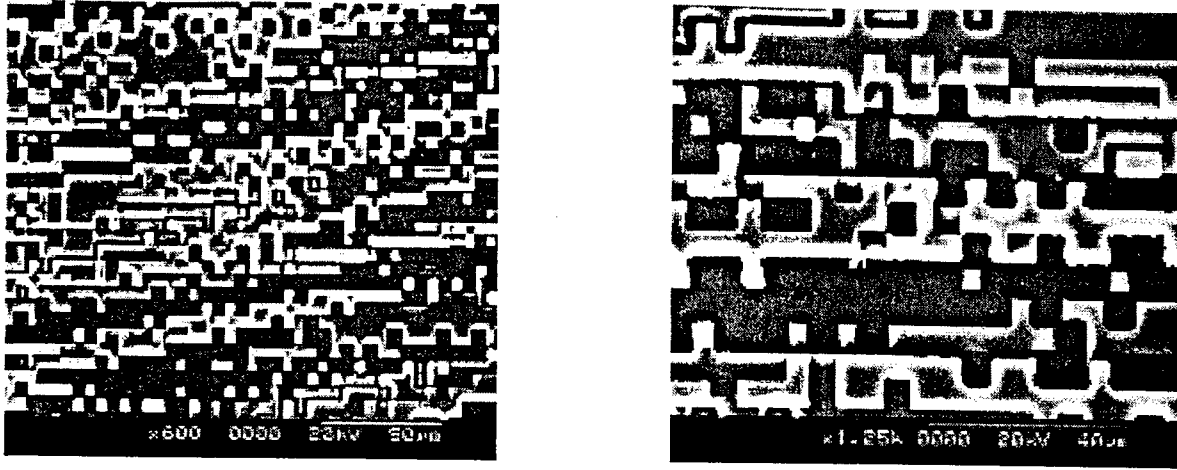


Figure 5: SEM micrograph of the fabricated Hough Transform hologram.

4. EXPERIMENTAL RESULTS

The experimental set-up for testing the matrix of HT holograms is shown schematically in Figure 6. A twisted nematic liquid crystal spatial light modulator (SLM) controlled by a VGA signal is used to introduce the input image into the system. The input image display with this SLM is more accurate in comparison with a RGB-video, because all the pixels are individually addressed. A system of imaging lenses is also used to magnify and display the input plane onto the HT matrix of CGHs. A Fourier Transform lens reconstructs the holograms and an acquisition system, consisting of a CCD camera and a PC with a digital frame grabber, is used to visualize resulting reconstructions in the output parameter plane.

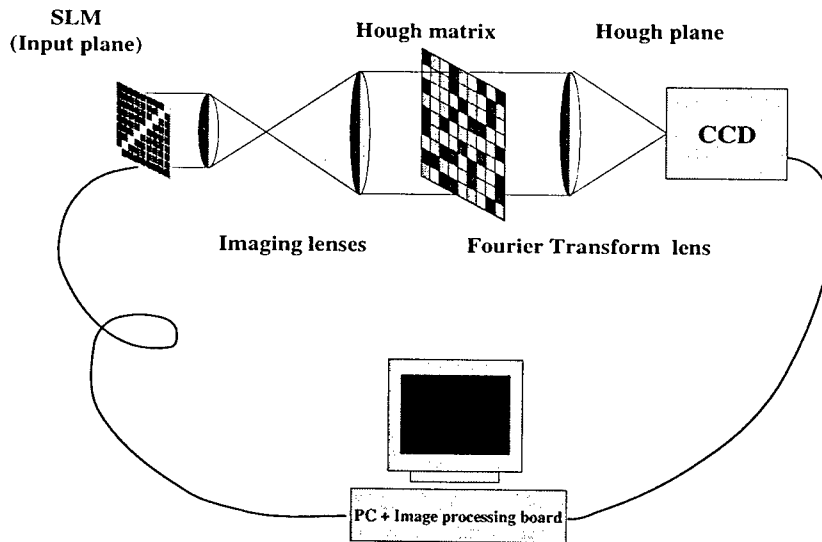


Figure 6: Experimental set-up of the optical HT processor.

The resulting output parameter domain is in Cartesian coordinates format (θ, ρ) , where θ and ρ vary in ranges $[0, \pi]$, and $[-\sqrt{2}D, \sqrt{2}D]$ respectively, where D is the half size of the input image. For an input plane consisting of 64×64 pixels, the output plane is a 65×65 accumulator cell array where the range of variation for ρ is $[-45.25, 45.25]$, and the ρ and θ resolution values are $\sqrt{2}$ and $\pi/64$ (2.81°) respectively.

Figure 7 shows experimental results on generation of HT for various examples of the input patterns. Each output picture displays undesirable zero order resulting from imperfections in the hologram reconstruction. In fact, the presence of this peak is due to etching errors during the fabrication process. It should also be noted that the CGHs were designed such that the central order is not located on the central accumulator cell position in the reconstruction. Figures 7a and 7b show the reconstruction of a single hologram. Figure 7a, shows the reconstruction of the CGH corresponding to the central position in the input plane ($x_0=0$, $y_0=0$). In this case, the sinusoidal curve described by the equation $\rho = x_0 \cos \theta + y_0 \sin \theta$ becomes a horizontal line defined by the relation $\rho=0$. Figure 7c displays the reconstruction of the global parameter plane when the entire matrix of CGHs is illuminated. The intensity distribution in the output plane is the sum of all the reconstructed holograms. The intensity is higher near the central axis of the matrix because it is the location where a maximum of curves are superimposed. It should be pointed out that as expected the parameters domain is regularly mapped of illuminated square cells. Figures 7d and 7e show a centered straight line with a 135° slope and its HT response, respectively. All the sinusoids intersect in the same point with coordinates $\theta=45^\circ$ and $\rho=0$, correctly determining the parameters of the normal vector to the single input line. Figure 7g shows the parameter domain for a series of parallel straight lines of different lengths shown in Figure 7f. We notice, in this case that the different points are aligned on a vertical line corresponding to $\theta=45^\circ$ and that the light intensity is varying proportionally to the length of the straight lines in the input plane, indicating that with variable threshold, we can detect lines of variable length and also estimate the length of each line from the values of these thresholds. Figures 7h to 7k provide an example of a generating HT for higher order parametric curves. The summation of the sinusoidal curves forms in the output plane a specific pattern: a circle generates a slack strip (Figure 7i), whereas a centered ellipse generates a flattened strip (Figure 7k). The evaluation of the ρ mean positions and the width of the strip on the $\theta=0^\circ$ and $\theta=90^\circ$ columns gives information about the location of the center in the input plane as well as the diameter or dimensions of the ellipse axis. We notice that our optical HT processor detects circle as well as ellipse with good accuracy (see Figures 7i and 7k).

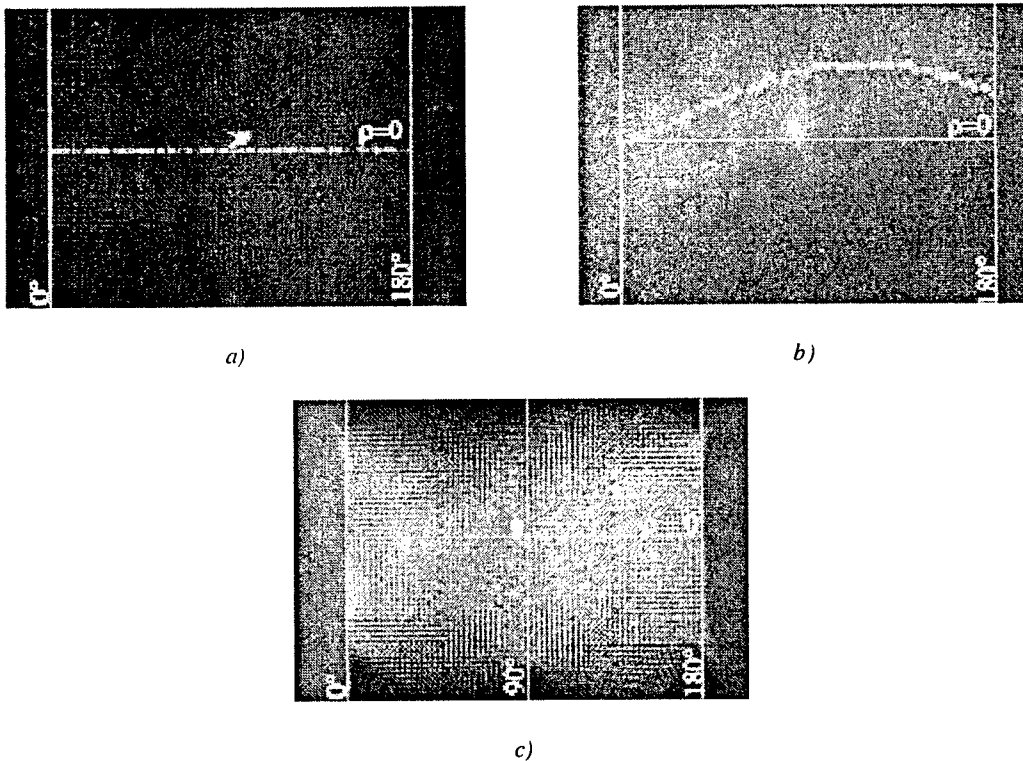
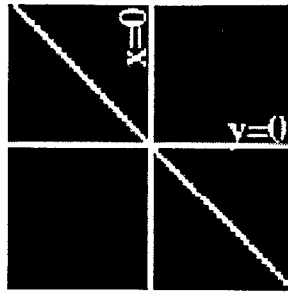
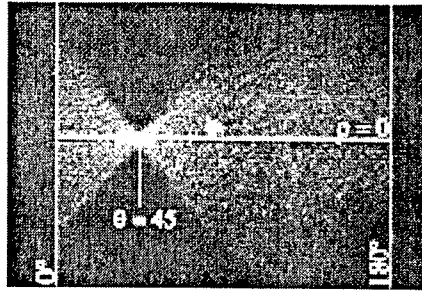


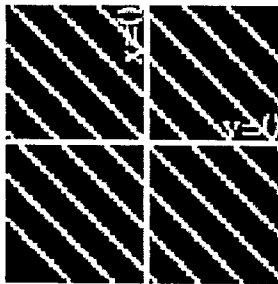
Figure 7: Output planes for different input images: a) PSF of the hologram of coordinate (0,0) in the matrix; b) PSF of one single hologram in the array; c) global illumination of holograms matrix.



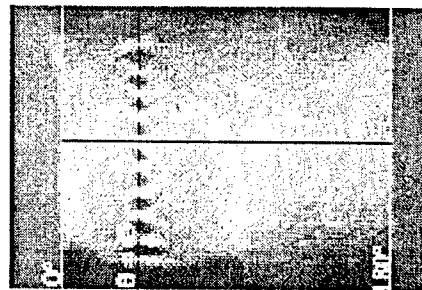
d)



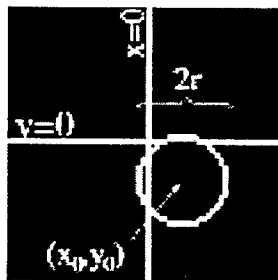
e)



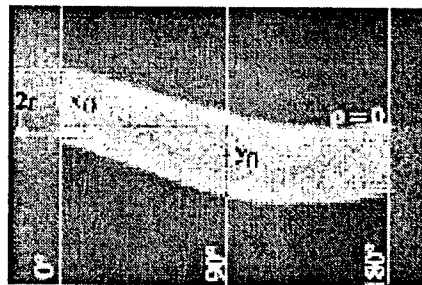
f)



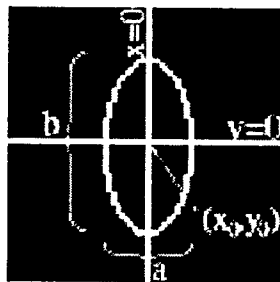
g)



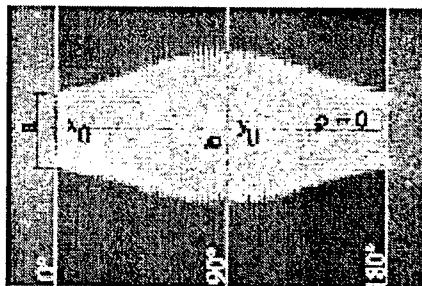
h)



i)



j)



k)

Figure 7 (cont'd): Output planes for different input images : e) photograph of the parameter domain for a straight line with parameters $\theta=45^\circ$ and $\rho=0$ in the input plane (d); f) series of parallel straight lines with a 135° slope in the input plane; g) HT of the series of straight lines of (e) ; h) circle in the input plane : $x_0=8$, $y_0=-9$, $2r=21$; i) output plane for a circle in (h), the width of the pattern for $\theta=0^\circ$ corresponds to the diameter of the circle. The measured parameters : $x_0=7.1$, $y_0=-8.5$, $2r=19.8$; j) ellipse in the input plane: $x_0=0$, $y_0=-1$, $a=20$, $b=40$; k) output plane for an ellipse in (j). The dimensions of the axis (a,b) are read on the 0° and 90° -columns, whereas the location of the ellipse center (x_0, y_0) is determined by the ρ -mean position of the strip on the 0° and 90° columns. From the measured parameters, we estimate : $x_0=0$, $y_0=0$, $a=19.8$, $b=41$.

5. CONCLUSION

An optical HT processor that uses a four-level-phase matrix of 64x64 CGHs is presented. Each element in the array is a 128x128 pixels CGH which is designed using a novel algorithm that combines the high speed of convergence of iterative Fourier algorithm (IFTA) with the high precision of the direct binary search (DBS) algorithm. Compared to off-axis optically recorded thick holograms, the on-axis 4-level-phase CGHs matrix introduces a great advantage into our system: the absence of complex conjugate orders in the reconstruction allows for a smaller space bandwidth requirements from the holograms and simpler system packaging. The holograms were fabricated using micro-lithography and chemically assisted ion beam etching techniques. The holograms generate a normal parameter HT space (ρ, θ) with resolution of 65x65 pixels. The detection of line segments within a 0° to 180° angle range is performed with a 2.81° resolution. The HT processor was applied to extract parameters of various parametric curves such as single lines, parallel lines, circle, ellipse. The measured parameters are found in excellent agreement with the actual inputs. This 41 x 41 mm diffractive optical element is one of the largest size matrix of space variant CGHs ever created until now. The experimental results show that our on-axis processor is an attractive alternative to existing optical and electronic architectures for implementing HT algorithms for real time applications.

6. ACKNOWLEDGMENTS

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A. 2. Optoelectronic System for Space Variant Signal and Image Processing

P.E. Shames, S. Laut, P. Ambs and Y. Fainman

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Optoelectronic System for Space Variant Signal and Image Processing

Paul E. Shames, Sophie Laut*, Pierre Ambs* and Yeshaiahu Fainman

Department of Electrical and Computer Engineering, UCSD
La Jolla, CA 92093, USA

*Université de Haute Alsace, ESSAIM
F-68 093 MULHOUSE, France

ABSTRACT

We present a study on a high-speed optoelectronic system for implementing space variant transforms (SVT) in image and signal processing using a Hough Transform (HT) as an example. The HT has been found to be highly useful in applications requiring detection of lines, ellipses and hyperbolic shapes, such as radar detection and data fusion, topographical map analysis, etc. However, the implementation of a SVT such as HT, is computation and memory intensive, e.g. HT of an image of dimension $N \times N$ requires greater than N^3 operations. All-electronic systems remain inadequate when real time SVT processing of large data sets is required. In this paper we show that an optoelectronic (OE) system employing parallel processing can perform such SVT requiring on the order of only N steps. We show that our proposed OE system can HT an input image of dimension $N = 1024$ in 2.1 ms.

Keywords: Space-variant transforms, Hough transforms, optoelectronic system, computer-generated hologram, image and signal processing.

1. INTRODUCTION

Space-variant transforms (SVT), such as the Hough transform¹ (HT), are useful in many image processing applications including radar detection² and data fusion³, topographical map analysis⁴ and autonomous robot control⁵. However, the implementation of SVT is computation and memory intensive⁶. Therefore, for efficient processing, all-electronic implementations have been developed using parallel multi-processor, such as pyramid⁷, mesh⁸, multi-ring⁹ and systolic array¹⁰, computer systems.

For SVT an attractive alternative to such all-electronic systems are optical systems that take advantage of the inherent parallelism of optics. Several such systems have been proposed, including the use of cylindrical¹¹ and micro-lenses¹², rotationally multiplexed¹³ and computer generated holograms¹⁴ (CGH). For digital processing, these systems utilize spatial light modulator (SLM) and detector (e.g. CCD) arrays for image input and output (I/O), respectively. We have implemented such a HT processing system using a matrix of CGH¹⁵. Each hologram in the array is designed to map a specific image pixel, displayed on an SLM, to the entire CCD pixel array. The HT for the entire image is pre-computed and pre-stored in the form of a CGH array, which is later accessed in parallel as an array of space-variant impulse response holograms. Therefore, the optical interconnection hologram can be seen as a page oriented optical memory. The speed and efficiency of the SLM and detector technology utilized dictate the SVT image processing time.

The realization of high-resolution real-time systems may require optoelectronic (OE) processing systems that utilize fast CMOS driver technology. In such a system, a VCSEL array and a smart-pixel focal plane array can be used for I/O, respectively, at high clock rates. In this paper we investigate the practical implementation of such a system. In Section 2 we review space variant transforms and line detection using the Hough transform. In Section 3 we discuss a high-speed optoelectronic implementation of such transforms and in Section 4 we define the performance metrics we use to characterize the system. In Section 5 we compare the optoelectronic system to all-electronic parallel systems. In the last section we present a summary and conclusions.

2. SPACE VARIANT TRANSFORMS

A SVT affects each input point differently, and can be defined by a 2-D superposition integral

$$F(x, y) = \iint_{-\infty}^{+\infty} f(\xi, \eta) h(x, y; \xi, \eta) d\xi d\eta, \quad (1)$$

where $f(\xi, \eta)$ is the input image to the SVT filter, $F(x, y)$ is the output image and $h(x, y; \xi, \eta)$ is the SVT filter impulse response. For SVT, the filter is dependent on the *absolute* position in the input plane and varies in the observation output plane. Examples of SVT used in machine vision and pattern recognition include the log-polar¹⁶, reciprocal wedge¹⁷ and HT.

In the HT each point from the image (input) domain is mapped into a parametric curve in the output (parameter) domain. As an example we review a HT employed for detection of a straight line in normal parameterization. A straight line in the input domain is described by

$$f(x, y) = \begin{cases} 1, & (x, y) \in \rho_0 = x \cos \theta_0 + y \sin \theta_0 \\ 0, & \text{othe rwise} \end{cases}, \quad (2)$$

where ρ_0 is the shortest distance to the origin and θ_0 is the direction of ρ_0 (see Figure 1a). Therefore, the parameter domain is the distance-angle plane (θ, ρ) with Cartesian coordinates axes ρ and θ (see Figure 1b). In this case each input plane point (x_i, y_i) will be mapped into a sinusoidal curve in the (θ, ρ) domain

$$\rho = x_i \cos \theta + y_i \sin \theta. \quad (3)$$

Put in terms of the SVT of, Using Eq. (3) for designing the SVT filter, Eq. (1) can be rewritten yielding output parameter domain,

$$F(\rho, \theta) = \iint_{-\infty}^{\infty} \delta(\rho - x \cos \theta - y \sin \theta) f(x, y) dx dy. \quad (4)$$

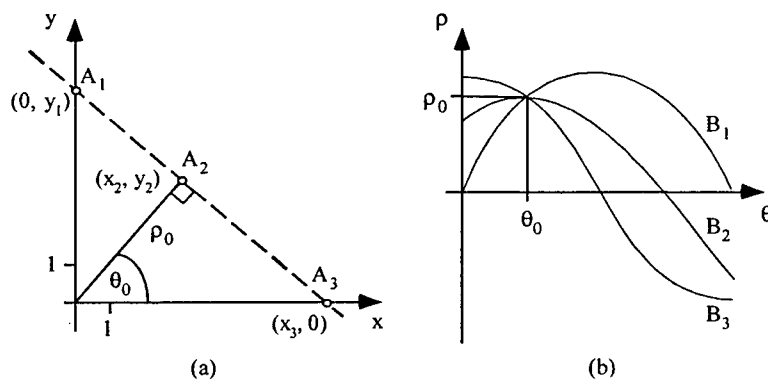


Figure 1. Normal parameterization of a straight line where the (a) input image plane has three points along a line and the (b) parameter plane has three corresponding curves intersecting at (θ_0, ρ_0) .

Each point in the input plane generates a sinusoidal curve in the output domain that spans all of the lines that may pass through that point. Sinusoidal curves that intersect in the parameter plane describe a line passing through at least two points in the input plane (see Figure 1b). Therefore, multiple points lying along the same line described by (θ_0, ρ_0) in the input will result in multiple curves intersecting in the parameter plane at the point (θ_0, ρ_0) . By taking the sum of the intersecting points, which corresponds to a measurement of intensity in an optical system, the strength (or number of points) on that line is determined. Higher order parameterizations have also been developed that allow for the 2-D detection of a variety of geometric shapes such as ellipses¹⁸ and hyperbolic curves¹⁹ as well as the iterative detection of 3-D objects²⁰.

3. OPTOELECTRONIC SYSTEM IMPLEMENTATION

We have demonstrated an OE processing system using a 256×256 matrix of CGH filters for Hough transform, coordinate transform, and optical interconnects¹⁵. To construct the matrix of holograms, the CGH encoding of the SVT for each pixel position was displayed on a Hughes liquid crystal light valve (LCLV) and optically recorded, in the Fourier transform plane, onto Silver Halide holographic film. The image processing system, shown in Figure 2, used the LCLV to generate the input image, which is imaged onto the matrix of holograms. The output is reconstructed onto the CCD camera using a Fourier lens.

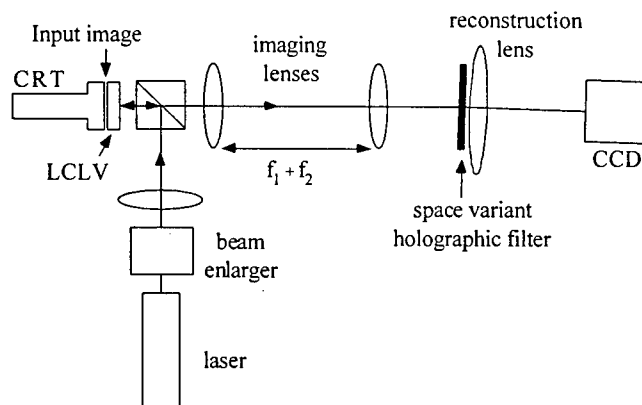


Figure 2. Optoelectronic system for space-variant image processing. A CRT and laser are used to generate the real-time image from the LCLV. The outputs from the holograms are reconstructed off-axis onto the CCD camera using a Fourier lens.

We have also demonstrated a HT image processing system, for detection of straight lines and ellipses, using a 64×64 matrix of computer generated holograms constructed using standard micro-lithography and fabrication techniques²¹. To efficiently encode each CGH for the Fourier transform of the desired filter, we used a modified version of the direct binary search (DBS) method combined with the iterative Fourier transform algorithm²². The four-phase level CGH was fabricated using a combination of e-beam and photo-lithography and chemically assisted ion beam etching. Each hologram contains 128×128 pixels, which are each $5 \mu\text{m} \times 5 \mu\text{m}$. The micro-fabricated CGH have the advantage of uniform holographic recording of each pixel as well as flexibility of CGH design, e.g. allowing for on-axis reconstruction.

Next generation of optoelectronic systems will require fast I/O to perform real-time processing of high-resolution images on the order of 1024×1024 input pixels. Using VCSEL and smart focal plane arrays flip-chip bonded to CMOS drivers allow operation at low power with I/O clock rates greater than 150 MHz ²³. The SVT of the input image to the output image is performed using diffractive and micro-optics. By using the same element spacing, the VCSEL and hologram arrays can be placed directly next to each other (see Figure 3). The refractive lens may also be replaced with an array of micro-lenses. Therefore, the components and subsystems can be packaged into a compact and rigid optoelectronic system. Efficient packaging will also be able to take advantage of in-situ recording and self-assembly techniques.

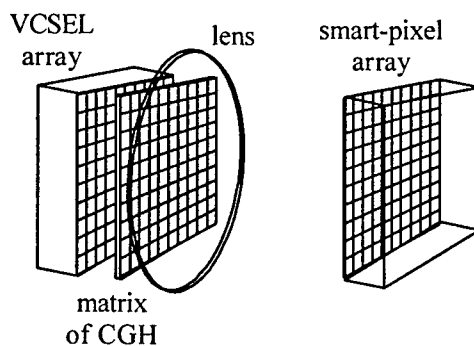


Figure 3. Optoelectronic SVT image processing system uses VCSEL and smart-pixel arrays bonded to CMOS drivers for fast I/O. The reconstruction lens can be replaced by diffractive micro-lenses, allowing for a more integrated and compact package.

The VCSEL array is expected to act as a partially spatially coherent quasi-monochromatic source. A unique feature of using these VCSEL arrays, as opposed to traditionally employed SLM implementations, is improvement of the SNR performance due to incoherent superposition at the output (e.g. reduced speckle noise). Tunability of VCSEL arrays would also enable using wavelength multiplexing of volume holography to pre-store multiple transforms, thereby allowing reconfiguration for efficiently implementing a number of SVT algorithms. Since such systems are generally used for line and shape detection (where missing pixels have a small effect on detection efficiency), relatively low yield VCSEL arrays can be tolerated allowing for the use of large scale arrays.

4. PERFORMANCE METRICS

In order to analyze the capabilities of such an OE processing system we define a set of performance metrics that can be compared to other existing SVT image processing systems. We begin by defining the dimensions of our system. Let the image (input) domain be of size $N \times N$, the transform domain is $K \times K$ and the parameter (output) domain be of size $M \times M$ (see Figure 4), where for simplicity we have assumed symmetric arrays. The VCSEL (SLM) array is of size $F \times F$ (i.e. the input image can have a different dimension than the VCSEL array) and the smart-pixel (detector) array is $D \times D$, then for a fully space variant transform $F = K$ and $F \leq D$.

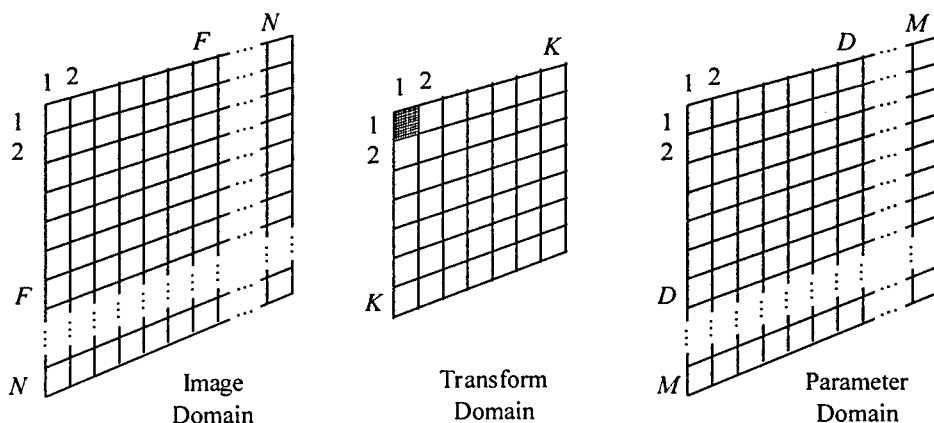


Figure 4. Dimensions of the image, transform and parameter domains.

The dimensions F and K , the input image and output planes, will be constrained by the attainable pixel size of the CGH elements. Assuming the output from each VCSEL fills the area of its corresponding CGH, then the 2-D space bandwidth product (SBWP) of a single hologram can be given by $SBWP_{\text{single}} = D^2 C^2$ where C is the spatial encoding (e.g. for a 64×64 image, a single hologram with 128×128 pixels results in a spatial encoding $C = 2$). Therefore, for the entire matrix of holograms we obtain

$$SBWP = K^2 D^2 C^2. \quad (5)$$

We can also define the SBWP in terms of the physical dimensions of the matrix of holograms so that

$$SBWP = \left(\frac{l_h}{\delta} \right)^2, \quad (6)$$

where l_h is the length of the hologram matrix and δ is the size of each pixel in the CGH (minimum feature size). If we assume a SVT where $K = D$, then we can say

$$K = \sqrt{\frac{l_h}{C\delta}}. \quad (7)$$

For example, if we assume that the matrix of holograms has a length $l_h = 100$ mm, a minimum feature size $\delta = 1 \mu\text{m}$ and encoding $C = 6$, then $K, D \approx 128$ (i.e. the input/output can be of maximum dimension 128×128).

The length of the system will depend on the size of each component as well as the distance between components. Assume each VCSEL has an aperture a and a pitch p , then the distance between the VCSEL array and holograms can be approximated by

$$z_{\text{CGH}} = \frac{p \cdot a}{2\lambda} \quad (8)$$

(assuming the VCSEL array pitch is equal to the pitch of the hologram array, then $p = \frac{l_h}{K}$). The distance from the reconstructing lenses to the output plane is given by

$$z_o = f = dF/\#, \quad (9)$$

where f is the focal length (if we assume a refractive lens, then the diameter $d > \sqrt{2}l_h$). Since each pixel is Fourier transformed onto the output plane, we can describe the size of the detector array by the relation $l_d = \frac{\lambda f}{\delta}$. The size of each detector in the smart-pixel array is $\delta_d = \frac{l_d}{D}$ and the active detection area is restricted to $\leq \delta_d^2$ (we assume a densely packed detector array with processing performed outside the detection area).

The product of its overall length and width gives the footprint of the system

$$S_F = z \cdot l = \left\{ (t_V + z_{\text{cgh}} + t_h + t_R + z_o + t_d)(l_{\text{max}}) \right\}, \quad (10)$$

where t_V , t_h , t_d and t_R are the thickness of the VCSEL, hologram and smart-pixel detector arrays and the refractive lens, respectively. Substituting from the relations above we get

$$S_F = \left\{ \left(t_V + \frac{\sqrt{l_h C \delta a}}{2\lambda} + t_h + t_R + \sqrt{2}l_h F/\# + t_d \right) (l_h) \right\}, \quad (11)$$

where we assume the maximum width to be of order l_h . If we continue to assume a symmetric system, then the volume of the system is defined by

$$S_V = \left\{ \left(t_V + \frac{\sqrt{l_h C \delta a}}{2\lambda} + t_h + t_R + \sqrt{2}l_h F/\# + t_d \right) (l_h)^2 \right\}. \quad (12)$$

Let's assume the VCSEL and smart-pixel arrays have thickness of 0.5 cm (including CMOS layer), the holographic array has thickness 0.1 cm and the refractive lens has a thickness of 1.0 cm. Also, we assume $F/1$, $\lambda = 0.980 \mu\text{m}$, $\delta = 1 \mu\text{m}$, $K, D = 128$ and $C = 6$. The hologram width will be $l_h = 10 \text{ cm}$, which gives a focal length $f \approx 14 \text{ cm}$. If the VCSEL diameter is $a = 3 \mu\text{m}$, then the distance between the VCSEL and hologram array $z_o = 1.1 \text{ mm}$. The total length of the system is $z \approx 16 \text{ cm}$, which results in a footprint of $S_F \approx 160 \text{ cm}^2$ and volume of $S_V \approx 1600 \text{ cm}^3$. From Eq. (11) we see that the system dimensions primarily depend on the size of each pixel, dictated by the minimum attainable feature size of the diffractive optical element (DOE), along with the $F/\#$ of the reconstruction lens. For example, reducing the pixel size to $\delta = 0.5 \mu\text{m}$ will reduce the total length to $z \approx 9 \text{ cm}$, the footprint to $S_F \approx 45 \text{ cm}^2$ and the volume to $S_V \approx 225 \text{ cm}^3$. On the other hand, using a $F/2$ lens will almost double the system dimensions. An attractive alternative to the thick refractive lens is to use a relatively thin diffractive lens (i.e. CGH) to perform the Fourier transform from the HT plane to the output plane.

To analyze the power requirements of the system we begin with the smart-pixel detectors. We can approximate the power requirements of each pixel by the relation

$$P_{\text{det}} = \frac{1}{R} \left(\frac{C_{\text{det}} dV}{dt} + I_{\text{leak}} \right), \quad (13)$$

where R is the responsivity. If we assume a leakage current $I_{\text{leak}} = 100 \text{ pA}$, detector capacitance $C_{\text{det}} = 30 \text{ fF}$ and responsivity $R = 0.3 \text{ A/W}$, then to get 10 mV at 500 MHz clock rate should require an incident optical power of

$P_{\text{det}} \approx 0.5 \mu\text{W}$. Dines²⁴ has shown that smart pixels operating at greater than 100 MHz clock rate require a detector area of only $50 \mu\text{m} \times 20 \mu\text{m}$ and less than 10 fJ of incident energy. At a 500 MHz clock rate this corresponds to $P_{\text{det}} \approx 5 \mu\text{W}$. Since each VCSEL needs to power a minimum of 128 smart-pixels in the detector array, then assuming 50% efficiency of the DOE, the required optical power from the VCSEL is between $P_V = 0.1 - 1.0 \text{ mW}$. For low threshold VCSELs we can assume²⁵ a slope efficiency of 55% and a threshold current $I_T = 212 \mu\text{A}$. Using the conservative upper-bound estimate $P_V = 1 \text{ mW}$, then the required current per VCSEL is $I = 760 \mu\text{A}$. Using 3V CMOS driving circuitry would require 2.3 mW of driving power. Since only one row is addressed at any one time, then for $N = 128$ where every pixel is in the 'on' state this corresponds to $P < 0.3 \text{ W}$.

To determine the thermal performance of such a system we assume that the 0.3 W of power will need to be dissipated on the end surfaces. For $l_h = 10 \text{ cm}$, the surface area of each end is $S_E = 100 \text{ cm}^2$. Therefore the VCSEL array will need to dissipate approximately $3 \frac{\text{mW}}{\text{cm}^2}$. We can assume that the smart-pixel array will need to dissipate the same order of power²⁶ over a similar surface area (on the opposite side of the OE system).

The performance metric that can most easily be compared to alternative systems is the amount of time required to SVT process a single input image. For a CMOS driver operating at clock rate f , we can assume that the VCSEL response time is on the order of $\tau = \frac{1}{f}$. Using parallel-matrix addressing, i.e. where only one pixel per row can be addressed at a time, then the load time of an input image is $\tau_K = \frac{K}{f}$. The smart-pixel detection time can be described by $\tau_D = \frac{D+P}{f}$, where D is the number of rows in the detector and P is the number of clock cycles required to perform some local processing and A-D conversion. The total processing time for $N = K$ is then given by the sum

$$T' = \frac{K + D + P}{f} \quad (14)$$

For a system where the dimension of the input domain is greater than the filter domain, $N > K$ (e.g. a large input image or wavelength multiplexed processing), then the system must perform some block-serial mapping and can be described by

$$T'' = \frac{K + D + P}{f} \left(\frac{N}{K} \right)^2 \quad (15)$$

Similarly, for a parameter domain larger than the filter domain, $M > D$ (e.g. for an asymmetric SVT), then the total processing time can be given by

$$T = \frac{K + D + P}{f} \left(\frac{NM}{KD} \right)^2 \quad (16)$$

For large image sizes we can assume that the number of clock cycles required for local processing is small compared to the image size, i.e. $P \ll K, D$. There are three cases that we will examine:

1. The input and output dimensions are equal to (or smaller) than the filter domain, i.e. $N = K = D = M$, then the total processing time reduces to

$$T_1 \approx \frac{2N}{f} \quad (17)$$

2. The input dimension is larger than the filter dimension, i.e. $N > K$, then

$$T_2 \approx \left(\frac{N}{K} \right)^2 \frac{2K}{f} \quad (18)$$

3. The input and output dimensions are larger than the filter dimension, i.e. $N > K$ and $M > D$. However, we will assume that the input and output are of the same dimension, i.e. $N = M$ and $K = D$, then

$$T_3 \approx \left(\frac{N}{K} \right)^4 \frac{2K}{f} \quad (19)$$

In Figure 5 we have plotted the processing time for each of the three cases discussed and we see that there is an exponential increase in the processing time when the input/output sizes are larger than the holographic filter. For example, assume an input image of 512×512 and CMOS clock rate of 500 MHz. If the matrix of holograms is also 512×512 then the total processing time will be $T_1 = 2.0 \mu\text{s}$. However, for a SVT filter of size 128×128 , the processing time is increased to $T_3 = 130 \mu\text{s}$ (where the output is of dimension 512×512).

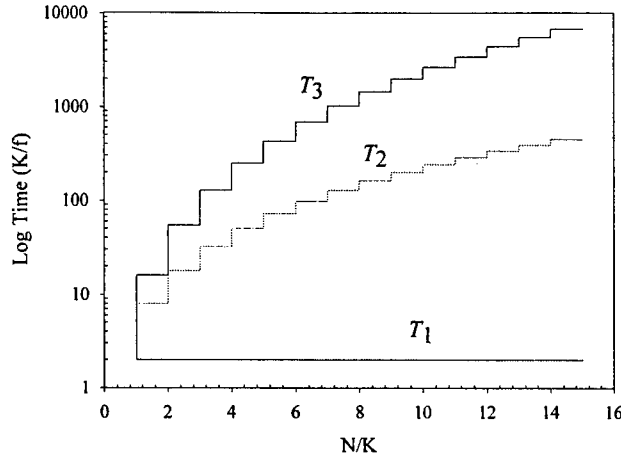


Figure 5. Log of computing time in units of K/f as a function of N/K .

Another convenient measure of performance is throughput, which is defined as the number of pixels processed per second and for an $N \times N$ image can be given by

$$Th = \frac{N^2}{T} = N^2 \left(\frac{f}{K+D+P} \right) \left(\frac{KD}{NM} \right)^2. \quad (20)$$

Again we assume $P \ll K, D$, where our three cases are:

1. $N = K = D = M$, then the throughput reduces to

$$Th_1 \approx \frac{1}{2} Nf. \quad (21)$$

2. $N > K$, then

$$Th_2 \approx \frac{1}{2} Kf. \quad (22)$$

3. $N > K$, $M > D$, $N = M$ and $K = D$, then

$$Th_3 \approx \frac{1}{2} \left(\frac{K}{N} \right)^2 Kf. \quad (23)$$

Using the same example as above, i.e. 512×512 image and 500 MHz clock rate, if the matrix of holograms is also 512×512 then the total throughput will be $Th_1 = 1.2 \times 10^{11} \frac{\text{pixels}}{\text{sec}}$ and for a filter of size 128×128 , the throughput is $Th_3 = 2.0 \times 10^9 \frac{\text{pixels}}{\text{sec}}$.

Finally, for a binary input image we can describe the number of binary operations per second or bandwidth by the relation

$$O = \frac{N^2 M^2}{T} = N^2 M^2 \left(\frac{f}{K+D+P} \right) \left(\frac{KD}{NM} \right)^2 \quad (24)$$

and if we assume that $K = D$ and $P \ll K, D$, then this simplifies to

$$O \approx \frac{K^3 f}{2} \quad (25)$$

For a filter of size 128×128 image and 500 MHz clock rate the number of binary operations is $O = 5.2 \times 10^{14} \frac{\text{bits}}{\text{sec}}$. This large bandwidth is representative of the parallelism of an optics-based processing system.

5. COMPARISON

For comparison of our proposed OE SVT image processing system to all-electronic systems, we will assume a relatively conservative OE system configuration that has a 128×128 VCSEL array for input, a 128×128 array of holograms for SVT filtering, a 128×128 smart-pixel detector array and CMOS circuitry operating at a 500 MHz clock rate. For such a system a 512×512 image will be SVT processed in approximately 130 μs and a 1024×1024 input image will be processed in 1.0 ms. A proposed OE system using ferroelectric liquid crystal¹¹ (FLC) input devices and CGH encoded HT filters is capable of processing a 512×512 image in 1 ms, limited by the speed of the SLM.

The all-electronic SYMPATI2, developed in 1992 by CEA/LETI/DEIN, which uses the single instruction multiple data (SIMD) architecture, employs 128 parallel processing elements (PE) reporting²⁷ the HT image processing of a 512×512 input image (for 512 angles) in approximately 1 second. More recently, a HT board, utilizing a reconfigurable parallel architecture and two content addressable memory (CAM) chips, reported²⁸ line extraction of a 256×256 input image in 76 ms. Using a reconfigurable multi-ring network (RMRN) architecture where each node is a T9000 transputer, the HT operation on a 1024×1024 input image is estimated⁹ at 14 seconds, using 128 nodes. Performing the HT for straight-line detection in a 512×512 input image (with 2048 angles) using the *Systola 1024*, a systolic array of 1024 processors implemented on a standard PCI board, took¹⁰ 0.25 seconds. This corresponds to a processing time of 62.5 ms for 512 angles.

An alternative to these electronic DSP methods for HT processing is a strictly memory lookup method. To analyze the performance for a HT processing system that uses a lookup table, i.e. storing the HT (θ, ρ) results for all (x, y) input points, we begin by defining the dimensions of the storage required. Assuming a binary $N \times N$ input image, then the input is N^2 bits. Each input point maps a sinusoidal curve to the output, i.e. N angles θ . For θ each we need a word of length $\log_2 N$ to distinguish between N possible ρ . Therefore, the total storage required is

$$S = N^3 \log_2 N \text{ Bits.} \quad (26)$$

Since each angle is independent, we divide the transforms by angle into multiple memory chips (R) (i.e. each chip determines $\theta = \frac{N}{R}$ angles), giving the storage for each chip

$$S = \frac{N^3 \log_2 N}{R} \text{ Bits.} \quad (27)$$

For $N = 1024$, the storage required is $S = \frac{10^{10}}{R}$ bits.

For a lookup method, the HT can be described by the following steps:

1. Read input (x, y) value, assume 1 clock cycle.
2. Read HT (θ, ρ) value, 1 clock cycle.
3. Read existing output array value $(\theta_{\text{old}}, \rho_{\text{old}})$, 1 clock cycle.
4. Increment output array value $(\theta_{\text{old}}, \rho_{\text{old}})$, assume 2 clock cycles.
5. Write new output array value $(\theta_{\text{new}}, \rho_{\text{new}})$, 1 clock cycle.

Therefore, we can estimate the total time required processing of an $N \times N$ input image to be

$$T = \frac{6N^3 \log_2 N}{Rf}, \quad (28)$$

where f is the clock rate of the memory chips and we assume that $R \leq N$. For comparisons to alternative systems we will assume our memory to be Rambus RDRAM chips, capable of operating on a word ($\sim \log_2 N$) in parallel at 1 Giga word per second average clock rate. Therefore, for $N = 512$, and assuming $R = 16$, the total processing time is $T \approx 0.05$ seconds and for $N = 1024$ the processing time is $T \approx 0.4$ seconds. To compare this lookup method with our proposed OE system we plot the processing times, using Eqs. (17), (18) and (28), in Figure 6. Comparing ideal systems, where $N = K, R$ the OE system increases its advantage in processing speed as the dimensions of the input image increase. However, for an OE system with a small number of holograms, the exponential increase in processing time decreases its advantage over the strictly memory lookup table system with a limited number of memory chips.

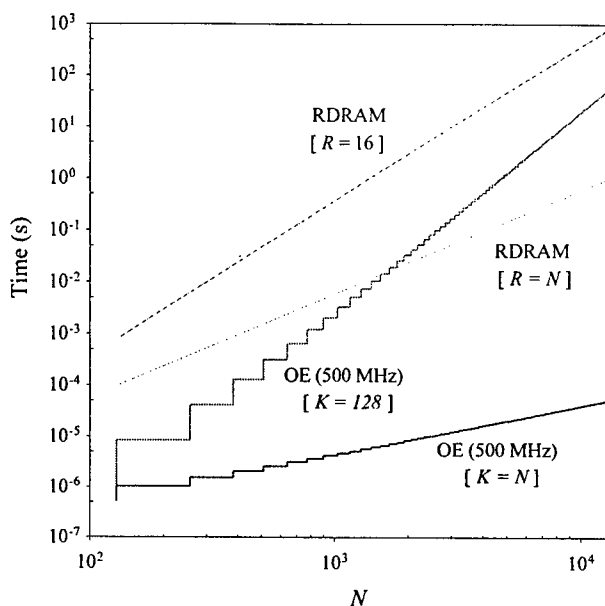


Figure 6. Log plot shows processing times for RDRAM memory resident and OE processing systems as functions of input image dimension.

In Table 1 we compare the processing times for the various systems discussed above. The all-electronic systems can perform the HT on the order of milliseconds for images of size up to 512×512 and on the order of seconds for larger input images. On the other hand, our proposed OE system can perform the HT on images of dimension 1024×1024 in a few milliseconds, required for real-time processing.

| N | 128 | 256 | 512 | 1024 |
|--------------|--------------|-------------|---------|--------|
| SunSPARC20 | 15 s | | | |
| SYMPATI2 | 24 ms | | 1.5 s | |
| CAM | | 76 ms | | |
| RMRN | | | | 14 s |
| Systola 1024 | | | 62 ms | |
| RDRAM $R=16$ | 0.79 ms | 6.3 ms | 50 ms | 0.40 s |
| OE $K=128$ | 0.51 μ s | 8.2 μ s | 0.13 ms | 2.1 ms |

Table 1. Processing times, given in seconds, for various SVT image-processing systems. For comparison we computed a serial implementation of the HT on a SunSPARC20 workstation with a 100 MHz processor.

6. CONCLUSION

An optoelectronic SVT image processing system, using CMOS driven VCSEL and smart-pixels for I/O and a filtering performed by a matrix of holograms, has been presented. In order to analyze the strengths and weaknesses of such a system we defined a set of performance metrics. The dimensions of the OE system are primarily constrained by the minimum feature

sizes attainable using micro-fabrication techniques. However, using relatively conservative estimates our proposed system is highly compact. Using currently available technology our proposed OE processing system can perform HT on a 128×128 image in 0.51 μ s and using block-serial mapping for on a 1024×1024 input image a HT would take only 2.1 ms.

The exponential growth of the processing times for an OE system using relatively small arrays is the greatest limitation to SVT processing of very-large and high-resolution images. However, since these systems can tolerate low yield VCSEL arrays, or even stitching of multiple small arrays, it may be feasible to have VCSEL or detector arrays on the order of 1024×1024. For an input image size of 1024×1024 into a SVT on an OE processing system with VCSEL, hologram and smart-pixel arrays all of dimension 1024×1024 (stitched or low-yield), the processing time is estimated at only 4.1 μ s.

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AIR FORCE RESEARCH LAB/SNHC
HANSCOM AFB, MA 01731-5000

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HANSCOM AFB, MA 01731-5000

ALBERT A. JAMBERDINO 1
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JOANNE L. ROSSI 1
AIR FORCE RESEARCH LAB/SNW
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