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13. ABSTRACT *(Maximum 200 words)*

How to integrate optoelectonic devices with Si ICs is the key to the success of the optical interconnect technology. The substrate removal technique uses mechanical polishing and wet chemical etching to remove the substrate. After removal of the substrate, metal layers are deposited on the backside of the wafer and the VCSEL devices are ready to be mounted onto SI chips. The removal of the substrate enables the flip-chip bonding for 850 nm VCSELs and reduces the height of the defices.

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Final Report of the DARPA program:

Vertical Cavity Lasers Integrated onto Silicon Circuits

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A. Statement of the problem studied

As the speed of CPUs in personal computers is getting faster and faster, the electrical interconnects may become a potential bottleneck for the further improvements in overall system performance of computers. Hybrid integration of III/V semiconductor Vertical Cavity Surface Emitting Lasers (VCSELs) with Si chips for free space interconnects is a very promising approach that may provide a solution to the bottleneck problem for electrical interconnects. This technology may find tremendous applications not only in computers but also in intra-satellite communications and high-speed data links. However, a reliable and manufacturable approach was not available at the time when the program started. The main goals of this program were:

1. Develop a reproducible III/V epilayer reattachment technique to other substrates
2. Demonstrate successful integration of VCSEL with Si ICs and other electronic devices (GaAs FETs)
3. Investigate packaging issues of integrated photonic/electronic devices for optical interconnects
4. Transfer the technology to industries for commercialization

B. Summary of the most important results

Substrate removal technology

How to integrate optoelectronic device with Si ICs is the key to the success of the optical interconnect technology. Fig. 1 illustrates the idea of the substrate removal technology. Vertical cavity surface emitting lasers (VCSELs) are first grown on GaAs substrates and then transferred to Si IC chips. The detailed steps of the processes are shown in Fig. 2.

The substrate removal technique uses mechanical polishing and wet chemical etching to remove the substrate. After removal of the substrate, metal layers are deposited on the backside of the wafer and the VCSEL devices are ready to be mounted onto Si chips. The removal of the substrate enables the flip-chip bonding for 850 nm VCSELs and reduces the height of the devices, which is important from the system-design point of view sometimes. Most of the VCSELs used in this study were grown in house using MBE. Both proton bombardment and thermal oxidation techniques have been successfully demonstrated to provide current VCSELs. Submilliamp threshold for a single VCSEL has been realized after the substrate removal. The devices are mounted topside up for easier and more accurate alignment.

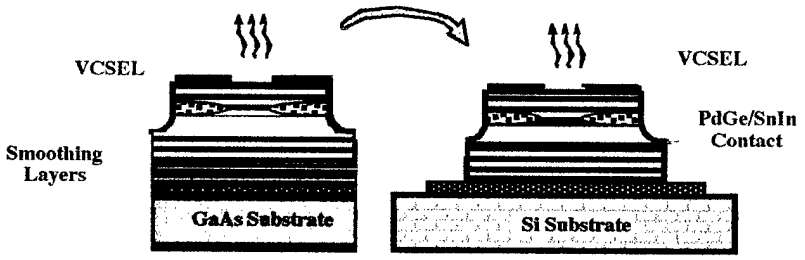

Fig. 1 Illustration of the idea of substrate removal technology.

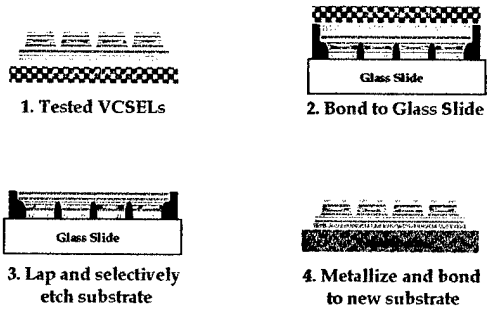

Fig. 2 Processing steps of the substrate removal technique.

As shown in Fig. 2, the VCSELs are first processed on the GaAs substrate. The finished VCSELs can be tested to select the good ones to proceed with further steps. Using black wax, the wafer is bonded to glass substrate. Then the substrate is first mechanically thinned and then chemically etched. The discrete VCSELs are then bonded onto the Si IC chips.

To test these processing steps, Cu heat sinks are used. Discrete VCSELs are transferred to copper heat sinks after the removal of the substrate. As shown in Fig. 3, the L-I curve exhibits an increase of more than a factor of two in laser power output without any degradation of threshold current. The spectra reveal that VCSELs on a heat sink have a shorter lasing wavelength, i.e. blue shift in energy, than those on GaAs substrate. This observation clearly shows that the active-region temperature of the VCSEL on a copper heat sink has been reduced. All these facts indicate that the processing steps work well and do not cause obvious damage to the devices.

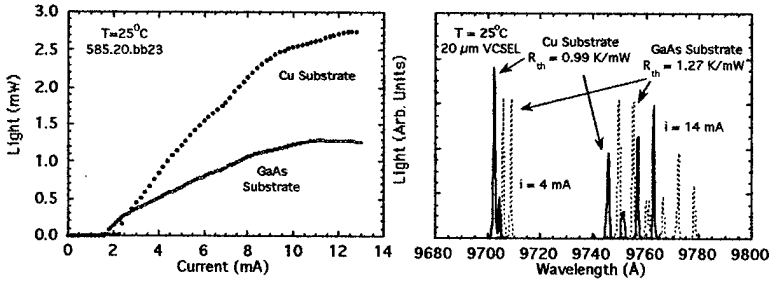

Fig. 3 L-I curves and lasing spectra of VCSELs before and after they were transferred from the GaAs substrate to copper heat sinks.

As a concept demonstration, we have successfully integrated discrete VCSELs on bonding pads of a bare Motorola HEX AC04 inverter chip. As shown in Fig. 4, the VCSEL bonded on the contact pad is probed from the top. By applying modulation voltage to the input of the inverter chip, the light output of the VCSEL is modulated. The on-set of the optical output is approximately 100 ns, which is very close to the on-set of the electrical signal. The maximum modulation speed here is limited by the probe station and the inverter chip, which are not designed for high-speed operation.

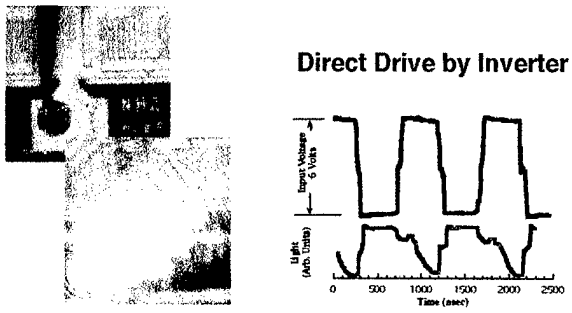

Fig. 4 VCSEL integrated on a commercial Motorola HEX AC04 inverter. The VCSEL output is directly modulated by the input to the inverter.

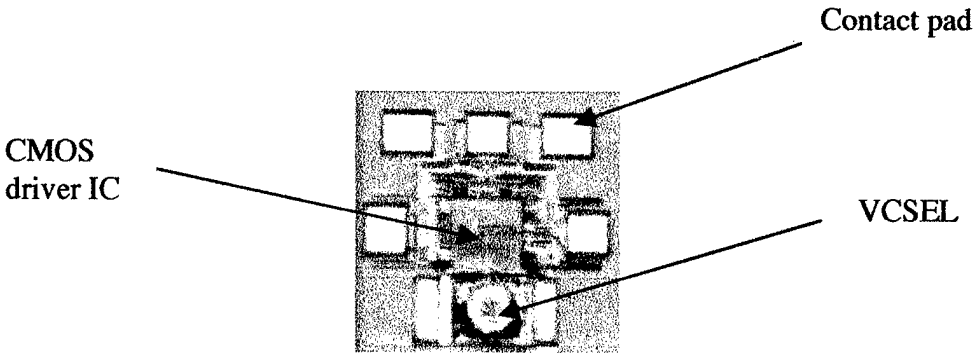

Fig. 5 VCSEL integrated with a custom designed CMOS driver.

Custom CMOS driver ICs have also been designed for VCSEL arrays. These CMOS chip were fabricated using 0.8 μm technology by MOSIS foundry service. As shown in Fig. 5, a discrete VCSEL is integrated with a custom designed CMOS laser driver chip. The measured modulation speed of this package is >250 MHz, a record speed of a packaged VSCEL with CMOS driver.

Most of the possible future applications involving VCSELs require a 2D array. To properly address each individual VCSEL, we have developed a special glass technology that enables the integration of 2D VCSELs with Si array drivers. Glass slides with deposited metal lines have also been developed for high speed VCSEL arrays integrated on Si ICs. As shown in Fig. 6, in this package, the VCSELs are sandwiched between the Si IC chip and the glass slide. Micro bumps are etched on the glass to feed the electrical contacts back to the Si chip. The advantage of this package is that it facilitates easy alignment to the layout of the laser driver ICs. Our theoretical modeling shows that this package has a superior performance at very high frequencies because glass is a better insulator than a Si substrate.

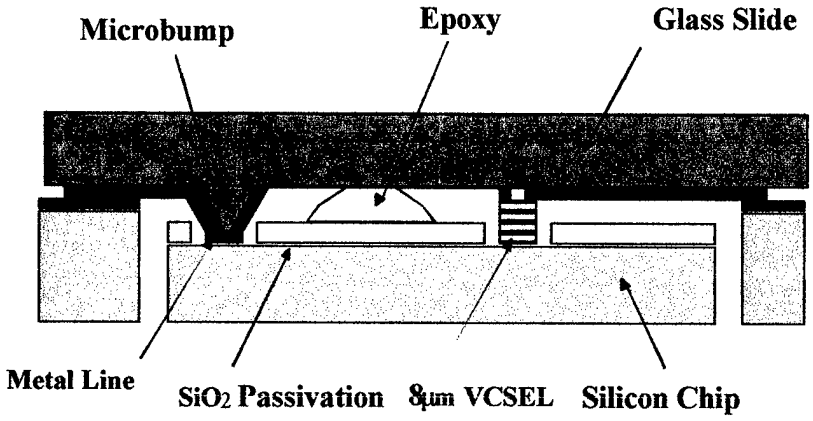

Fig. 6 Schematic drawing of a glass technology enabling the addressing of a VSCEL array.

A finished package is shown in Fig. 7, as seen through the glass slide. At the bottom is the Motorola HEX AC04 converter chip. Discrete VCSELs are bonded on to the contact pads of the inverter chip. This technology has a great potential for even larger arrays. It is especially important when 850 nm VCSELs have to be used for the optical interconnect due to the requirement for the top-emitting configuration to avoid light absorption in GaAs substrates.

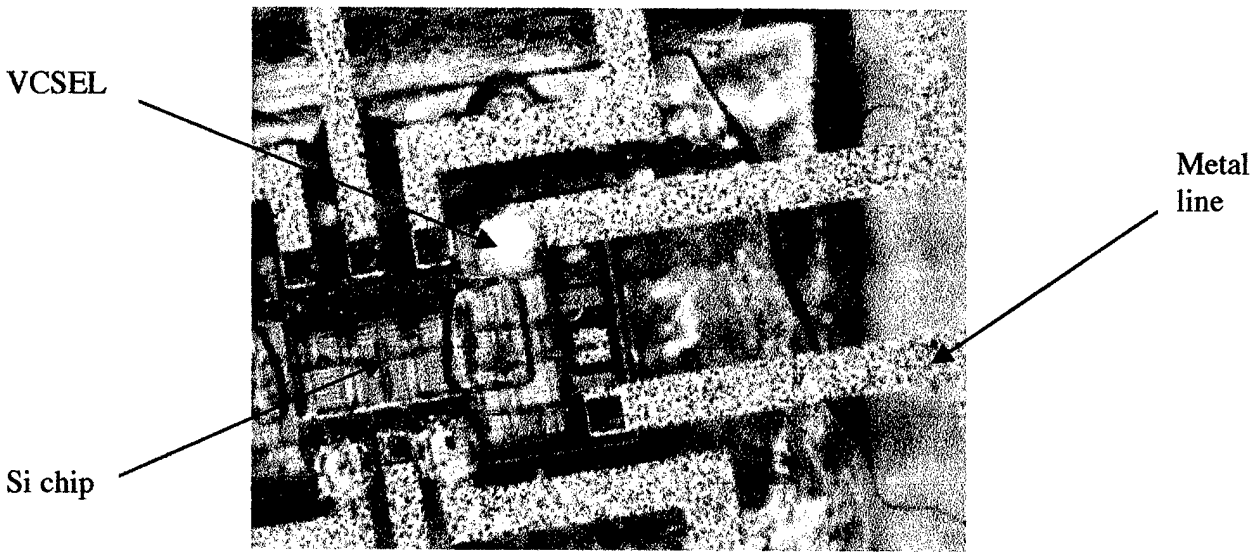

Fig. 7 A finished package of an integrated VCSEL addressed using the glass technology. The viewer sees through the glass slide on which metal lines are deposited.

Monolithic Integration of VCSELs, FETs and photodetectors

As our CMOS IC simulations show that the potential speed limit of the optical interconnect using a VCSEL/CMOS driver and photodetector/CMOS preamplifier configuration is not the CMOS driver but the preamplifier. To overcome this bottleneck,

we proposed the use of GaAs FETs as the first stage preamplifier for photodetectors. Starting from this idea, we extended our approach to an integration on chip with all critical components including VCSELs, MESFETs, resonant-cavity photodetectors (RC-PDs).

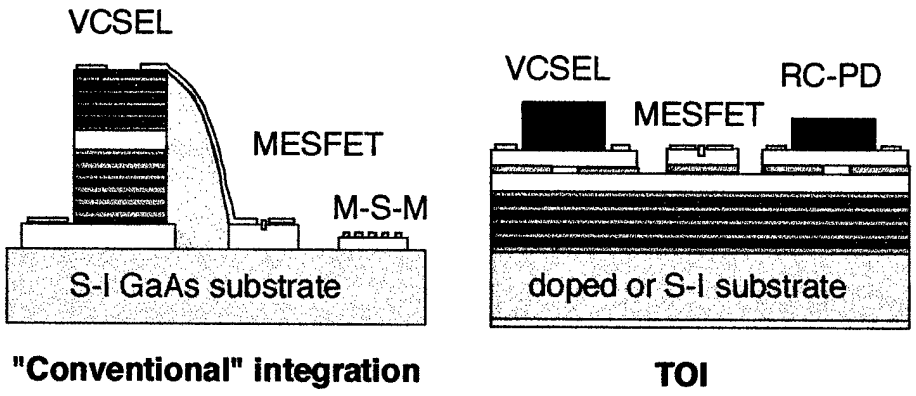

Fig. 8: A schematic diagram to compare our thermal oxide insulation (TOI) technology with "conventional" ones.

The basic idea is to integrate VCSELs, GaAs MESFETs, and RC-PDs on a single epitaxial wafer using planar process and thermal oxidization of AlAs. The idea is summarized in Fig. 8. The sample structure consists of a bottom DBR and an active region sandwiched by GaAs layers. Underneath the top final GaAs layer, a thin AlAs layer was grown to be oxidized later for current confinement and insulation of the MESFET from the conducting bottom mirror stack.

The general processes for the monolithic integration of these three major components are as follows. On the as grown wafer, MESFETs were first processed and then two types of dielectric mirror stacks were deposited for VCSEL and RC-PD, respectively. Reasonably high performance MESFETs (g_m=133 mS/mm with a gate length of 3 μm) on AlAs oxide layer, RC-PDs, and their integration with VCSELs were demonstrated. The experimental

results are given in Fig. 9 and 10. These devices provide building blocks on a single wafer and enable the integration of optoelectronic circuits in the future. One of the many advantages of this design is that the RC-PD has a narrow response spectrum that overlaps

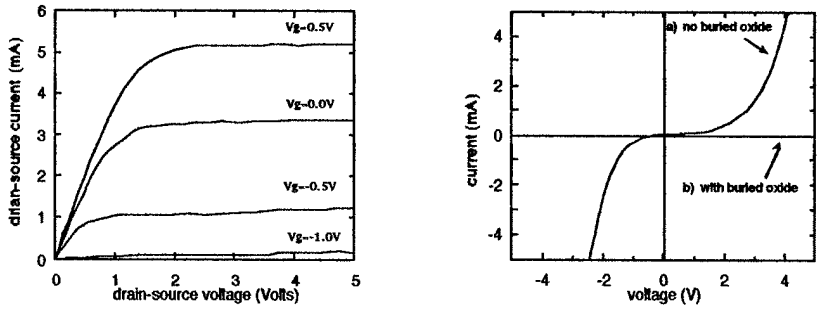

Fig. 9 I-V characteristics of the GaAs MESFET on AlAs thermal oxide. The leakage current was high (shown in the right hand side figure). After the oxidation of the AlAs layer, it becomes unnoticeable. This finding is explained in terms of the high resistivity of AlAs oxides.

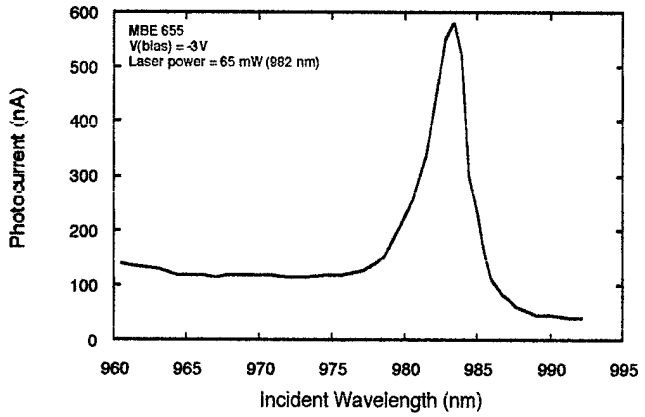

Fig. 10 The spectral response curve of a RC-PD made in this program. It shows at least a factor of 5 increase in the detectivity at the resonant frequency.

with the lasing wavelength of the VCSEL because of the use of the same active region. They are expected to have the identical temperature behavior, which is desirable for many applications.

Administrative summary of the program

The program started on 3/31/93 and ended on 5/31/97. Although during the course of the program the PI was changed twice, the program progressed very healthily. All the above mentioned goals have been met. An industrial partner was identified by the PI and a team formed that has been awarded a new DARPA program, Free Space Optical Interconnect Accelerator, to explore this technology further in order to make it used in real applications.

C. List of all publications

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Prof. George Maracas (3/94-1/95), PI.

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Jeff C.P. Chuang, PhD 5/98.

Hasan Fathollenhnejad, PhD, 8/5/94.

Intae Kyong, PhD student. Left for Motorola in 1997.

Chuck Wheeler, PhD, 5/98

Fan Yu, PhD student.

Martin David Boonzaayer, MS, 12/96.

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Erini Balanis, BS student

Robert Davis, BS student

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Ann Marie Kubes, BSE-EE, 12/15/95

Report of Invention

None.