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APPENDIX 29

SC PROGRAM TEST PLAN

FINAL SOFTWARE REPORT

DATA ITEM NO. A005

INTEGRATED ELECTRONIC WARFARE SYSTEM
ADVANCED DEVELOPMENT MODEL (ADM)

PREPARED FOR:

NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PENNSYLVANIA

CONTRACT N62269-75-C-0070

RAYTHEON
ELECTROMAGNETIC
SYSTEMS DIVISION

1 OCTOBER 1977

UNCLASSIFIED

APPENDIX 29

SYSTEM CONTROLLER SOFTWARE TEST PLAN

FINAL SOFTWARE REPORT

DATA ITEM A005

INTEGRATED ELECTRONIC WARFARE SYSTEM (IEWS)
ADVANCED DEVELOPMENT MODEL (ADM)

Contract No. N62269-75-C-0070

Prepared for:

Naval Air Development Center
Warminister, Pennsylvania

Prepared by:

RAYTHEON COMPANY
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6380 Hollister Avenue
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1 OCTOBER 1977

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LEXINGTON, MASS. 02173

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TYPE OF SPEC

SOFTWARE UNIT TEST PLAN

TITLE OF SPEC

SYSTEM CONTROLLER PROGRAM TEST PLAN, IEWS, ADM

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	George D. Thompson Jr.	12/27/76			

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REVISION																					
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SYSTEM CONTROLLER PROGRAM TEST PLAN, IEWS, ADM

1.0 SCOPE

This test plan defines the requirements for the integration testing of the system controller program as a stand-alone unit. The test plan will include tests of the self-loading capability of the system controller, the ability of the program to interface with test equipment simulating external devices, and the integration of each functional group of the program.

2.0 APPLICABLE DOCUMENTS

The following documents, of the latest issue in effect, form a part of this specification to the extent specified herein. In the event of conflict, the requirements of this specification shall govern.

53959-GT-0301	System Controller, ADM, IEWS, Unit Hardware Development Specification
061290529	Computer Program Performance Specification for System Controller Unit, ADM, IEWS
53959-JK-1002	System Controller-Sorter Interface Control Document, IEWS, ADM

The following documents have been used specifically in the formation of the requirements for these tests.

53959-GT-0756	Computer Subprogram Design Document, Executive, IEWS, ADM
53959-GT-0755	Computer Subprogram Design Document, Sorter Message Processing, IEWS, ADM
53959-GT-0754	Computer Subprogram Design Document, Analysis Return Processing, IEWS, ADM
53959-GT-0752	Computer Subprogram Design Document, CSDD, Emitter Classification 1, Processing, IEWS, ADM

53959-GT-0760	Resource Management Processing, IEWS, ADM
53959-GT-0753	Computer Subprogram Design Document, Display/Control Processing, IEWS, ADM
53959-GT-0757	Computer Subprogram Design Document, System Management 2 Processing, IEWS, ADM
53959-GT-0754	Computer Subprogram Design Document, ABI Management, IEWS, ADM

3.0 TEST REQUIREMENTS

This test plan provides the test requirements to integrate the functional groups of the system controller (SC) program into a fully functioning unit. The tests shall begin with fully tested and debugged functional group programs and shall test and verify their operation as a unit program. The tests shall also verify that the SC will load programs and will communicate with simulated external devices.

3.1 INTRODUCTION

The program tests shall be those defined in this paragraph. For the purposes of clarity the tests are classified as loading, static, and dynamic tests. In all cases, the level of testing shall be to determine that the subprogram or subprograms perform the overall function required. Detailed testing of the internal operation of the subprograms will not be required.

3.1.1 Loading Tests

The SC will have the capability of loading from either the special test equipment (STE) or directly from a peripheral input device such as a paper tape reader. The purpose of these tests shall be to verify that the loaders can load programs and/or data without error and in the correct memory locations. The loading tests shall be as defined in Table I.

Table I

LOADING TESTS

Test No.	Test	Subprograms Involved	Test Method	System Environment
L-1	Load RMP	Hierarchical Loader	Load directly from paper tape reader. Verify load by reading memory locations with control panel.	SC, paper tape reader, control panel.
L-2	Load CP	Hierarchical Loader	Same as test 1	Same as test 1
L-3	Load AP	Hierarchical Loader	Same as test 1	Same as test 1
L-4	Load SC	Hierarchical Loader	Same as test 1	Same as test 1
L-5	Load RMP	Hierarchical Loader	Load from STE shared memory. Verify load by reading memory locations with control panel.	SC, STE, Control Panel.
L-6	Load CP	Hierarchical Loader	Same as test 5	Same as test 5
L-7	Load AP	Hierarchical Loader	Same as test 5	Same as test 5
L-8	Load SC	Hierarchical Loader	Same as test 5	Same as test 5

RMP = Resource Management Processor
CP = Classification Processor
AP = Analysis Processor

3.1.2 Static Tests

Static testing of the SC program shall be accomplished by stimulating the SC with an input and allowing the program to run to a specified end point in the processing. The final state of the machine shall then be examined to verify that the desired processing took place. Static tests are further classified as Classification Processor (CP) tests, Resource Management Processor (RMP) tests, Analysis Processor (AP) tests, and System Controller (SC) tests.

3.1.2.1 Classification Processor Tests

The CP tests shall first integrate the Executive functional group with each of the background functional groups in turn. Functional groups shall then be integrated together until the entire CP software has been integrated as a whole. The CP tests shall be as defined in Table II. All of the tests shall be run with Micro debug from the software development center (SDC). The final CP static integration tests shall be repeated in the SC with the STE providing the stimuli and the data output capability.

3.1.2.2 Resource Management Processor

The RMP tests shall first integrate the Executive functional group with each of the background functional groups in turn. Functional groups shall then be integrated together until the entire RMP software has been integrated as a whole. The RMP tests shall be as defined in Table III. All of the tests shall be run with Micro debug from the software development center (SDC). The final RMP static integration tests shall be repeated in the SC with the STE providing the stimuli and the data output capability.

TABLE II

CLASSIFICATION PROCESSOR STATIC TESTS

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-1	Exec/SONE1 Interface	Verify Msg Xfer from Exec to SONE1	EXCP, SODR, SONE1	Place NE Alrt Msg on EXCP FIFO, Start Exec, stop execution at call to SONE1	SDC: RP-16, paper tape reader, terminal
CP-2	Exec/SONE1 end-to-end	Verify ETF loaded and Anal Req Msg generated	EXCP, SODR, SONE1, SOGET, SOLB, SOLA, SOIAL, SOPT1, SOQUT	Place NE Alrt Msg in simulated SS buffer, start Exec, stop at SODR rtn to Exec	Same as test 1
CP-3	SONE1 poor PRI quality	Verify that EFAVPI is given invalid ind	Same as test 2	Same as test 2	
CP-4	Azimuth Link Formation	Verify that az links are made correctly			
CP-5	Exec/SOUP Interface	Verify Msg xfer from Exec to SOUP	EXCP, SODR SOUP	Place PTDW Msg on EXCP FIFO, start Exec, stop at call to SOUP	
CP-6	Unclas Update	Verify unclass rtn from SOUP	Same as test 5	Place PTDW Msg in simulated SS buffer, start Exc, stop at return to Exec	
CP-7	SONA1 within limits	Verify NOFA1 within limits update	EXCP, SODR, SOGET, SOUP, SONA1, SOLA, SOLC, SOLT	Same as test 6	
CP-8	SONA1 out of limits	Verify NOFA1 out of limits update	Same as test 7 plus SOLB		

Table II - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-9	SON21 out of limits	Verify NOFA2 out of limits updated	EXCP, SODR, SOGET, SOUP, SON21, SONA1	Same as test 6	Same as test 1
CP-10	SON21 No scan req	Verify NOFA2 no scan update	Same as test 9		
CP-11	SON21 scan request	Verify NOFA2 scan update request			
CP-12	SOOC1, no candidates	Verify EOC update producing no Cand.	EXCP, SODR, SOGET, SOUP, SOOC1, SOLA, SOLB, SOLC, FCLV1		
CP-13	SOOC1 no scan req	Verify EOC no scan update	Same as test 12 plus ECST1		
CP-14	SOOC1 scan request	Verify EOC scan update request	Same as test 13		
CP-15	Exec/SODEL Interface	Verify Msg xfer from Exec to SODEL	EXCP, SODR, SOGET, SODEL	Place Inact File Msg in EXCP FIFO, start Exec, stop at call to SODEL	
CP-16	SODEL deletion	Verify ETF deletion processing	EXCP, SODR, SOGET, SODEL, SOIE	Place Inact File Msg in simulated SS buffer, start Exec, stop at return to Exec	
CP-17	Exec/SOMFF Interface	Verify Msg xfer from Exec to SOMFF	EXCP, SODR, SOMFF	Place MFF Msg in EXCP FIFO, start Exec, stop at call to SMFF	

Table II - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-18	Set EFMF	Verify that EFMF bit changes from 0 to 1	Same as test 17 plus SOGET	Place MFF Msg in simulated SS buffer, start Exec, stop at rtn to Exec	Same as test 1
CP-19	Leave EFMF	Verify that EFMF bit remains set		Same as test 18	
CP-20	Exec/SOSM1 Interface	Verify Msg xfer from Exec to SOSM1	EXCP, SODR, SOSM1	Place Sys Mng Msg in EXCP FIFO, start Exec, stop at call to SOSM1	
CP-21	SOSM1 Process	Verify that Sys Mng Msg are passed to RMP	Same as test 20	Place Sys Mng Msg in simulated SS buffer, start Exec, stop at rtn to Exec	
CP-22	Exec/SOTHR Interface	Verify msg xfer from Exec to SOTHR	EXCP, SODR SOTHR	Place TH Alrt Msg in EXCP FIFO, start Exec, stop at call to SOTHR	
CP-23	SOTHR process	Verify that TH Alrt parameters are loaded into ETF	EXCP, SODR, SOTHR	Place Th Alrt Msg in simulated SS buffer, start Exec, stop at rtn to Exec	
CP-24	Exec/SOINS Interface	Verify msg xfer from Exec to SOINS	EXCP, SODR, SOINS	Place Instru Msg in EXCP FIFO, start Exec, stop at call to SOINS	

Table II - continued -

Test No.	Test	Purpose	Subprograms Involved	Test Method	System Environment
CP-25	SOINS process	Verify that Instru Msgs passed to RMP	EXCP, SODR, SOINS	Place Instru Msg in simulated SS buffer, start Exec, stop at rtn to Exec	Same as test 1
CP-26	Exec/Anal Ret Interface	Verify msg xfer from Exec to Level 1 subprogram	EXCP, ANDR, ANNE2, ANNE3, ANNA2, ...	Place Anal Ret Msgs with RMC = 1, 2, . . . 9 in EXCP FIFO, start Exec, stop at call to Level 1 subprogram	
CP-27	ANNE2 proc	Verify NE process of PW validation	EXCP, ANDR, ANNE2, SOGET, ANPT2, ANPWT, ANHP1	Input Anal Ret Msg to EXMSG, stop at return to EXEC	
CP-28	Good qual freq validation	Verify NE validation of good freq data	EXCP, ANDR, ANNE3, SOGET, ANHP2, ANFQT, SOQUT	Same as test 27	
CP-29	Bad qual freq validation	Verify NE validation of bad freq data	Same as test 28		
CP-30	Anal Ret NE process	Verify end-to-end NE process in Anal Ret	Test 27 U Test 28	Input Anal Ret Msg to EXMSG, stop at end of ANNE3	
CP-31	ANNA2 null meas.	Verify NOFA2 null meas anal return	EXCP, ANDR, ANNA2, SOGET	Same as test 27	
CP-32	ANNA2 sdlb within limits	Verify NOFA2 sdlbe meas anal return	EXCP, ANDR, ANNA2, SOGET		

Table II - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-33	ANNA2, Level 1 No Cand.	Verify NOFA2 Level 1 search with no Cand.	Same as test 31	Same as test 27	Same as test 1
CP-34	ANNA2, Level 2 No Cand.	Verify NOFA2 Level 2 search with no Cand.			
CP-35	ANNA2, Level 2 Cand.	Verify NOFA2 Level 2 search with Cand.			
CP-36	ANNA3 proc	Verify NOFA2 final reclassification	EXCP, ANDR, ANNA3, ANEL2, ANFAM, ANAMB		
CP-37	NOFA2 Anal Ret proc	Verify NOFA2 end-to-end Anal Ret process	Test 31 U Test 36	Same as test 30	
CP-38	ANOC2, Level 2 No Cand.	Verify EOC Level 2 Search with no Cand.	EXCP, ANDR, ANOC2, SOGET, ANST2, ANLV2	Same as test 27	
CP-39	ANOC2, Update link	Verify EOC update link request	Same as test 38 plus ANUL1		
CP-40	ANOC2, NE Link	Verify EOC NE Link request	Same as test 38 plus ANEL1		
CP-41	EOC update end-to-end	Verify EOC Anal Ret update processing	EXCP, ANDR, ANOC2, SOGET, ANST2, ANLV2, ANOC4, ANUL2	Input Anal Ret Msg to EXMSG, stop at end of ANOC4	
CP-42	EOC Reclass end-to-end	Verify EOC Anal Ret Reclass processing	Same as test 40 plus ANOC3, ANEL2, ANFAM, ANAMB	Input Anal Ret Msg to EXMSG, stop at end of ANOC3	

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Table II - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-43	ANEC2 Proc	Verify Emit Class Lev 2 Search	EXCP, ANDR, ANEC2, ANST2, ANLV2, ANEL1	Same as test 27	Same as test 1
CP-44	ANEC3 Proc	Verify Emit Class Final decision	EXCP, ANDR, ANEC3, ANEL2, ANFAM, ANAMB		
CP-45	Emit Class Anal Ret proc	Verify Emit Class Anal Ret end-to-end	Test 43 U Test 44	Input Anal Ret Msg to EXMSG, stop at end of ANEC3	
CP-46	Exec/ECDR Interface	Verify msg xfer from Exec to ECDR	EXCP, ECDR	Place Class Msg on EXCP FIFO, start Exec, stop at call to ECDR	
CP-47	Level 1 Search no Cand.	Verify no Cand rtn from Emit Class, Lev 1	EXCP, ECDR, ECLV1	Input Class Msg to EXMSG, stop at return to Exec	
CP-48	Lev 1 Search Cand, no scan	Verify Emit Class, Lev 1, no scan req	EXCP, ECDR, ECLV1, ECST1	Same as test 47	
CP-49	Lev 1 Search Cand, scan	Verify Emit Class, Lev 1, scan req	Same as test 48		
CP-50	Lev 1 Search Unclass	Verify unclass rtn from Lev 1 Search	Same as test 47		
CP-51	NE Proc end-to-end normal	Verify total NE process end-to-end normal data	Test 2 U Test 27 U Test 28	Place NE Alrt Msg in simulated SS buffer, start Exec, stop at end of ANNE3	

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Table II - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-52	NE Proc end-to-end invalid	Verify total NE process end-to-end invalid data	Same as Test 51	Same as Test 51	Same as Test 1
CP-53	Emit Class end-to-end	Verify Emit Class process end-to-end	Test 48 U Test 42 U Test 43	Input class msg to EXMSG, stop at end of ANEC3	
CP-54	NE Proc/Emit Class, unclass	Verify NE Proc/ Emit Class, unclass rtn	Test 51 U Test 53	Place NE Alrt Msg in simulated SS buffer, start Exec, stop at end of ECDR	
CP-55	NE Proc/Emit Class total	Verify total NE Proc/Emit Class, end-to-end	Same as test 54	Place NE Alrt Msg in simulated SS buffer, start Exec, stop at end of ANEC3	
CP-56	Update NOFA2 within limits	Verify NOFA2 within limits proc	Test 9 U Test 32	Place PTDW Msg in simulated SS buffer, start Exec, stop at end of ANNA2	
CP-57	Update NOFA2 become EOC	Verify NOFA2 re-class processing	Test 9 U Test 32 U Test 36	Same as Test 56 except stop at end of ANNA3	
CP-58	Update EOC No scan reclass	Verify total EOC. updated, reclassify	Test 13 U Test 42	Same as Test 56 except stop at end of ANOC3	
CP-59	Update EOC, scan, same ID	Verify total EOC update, same ID	Test 13 U Test 41	Same as Test 56 except stop at end of ANOC4	

Table II - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
CP-60	Same as Test 51			Use SS buffer	STE
CP-61	Same as Test 52				
CP-62	Same as Test 53				
CP-63	Same as Test 54				
CP-64	Same as Test 55				
CP-65	Same as Test 56				
CP-66	Same as Test 57				
CP-67	Same as Test 58				
CP-68	Same as Test 59				
CP-69	No Anal wtd processing	Verify null anal rtn when no anal wtd request is made	EXCP, SODR, ANDR, ECDR, AB1DR	Place NE Alrt Msg in simulated SS buffer, start Exec, stop at rtn from AB1DR	Same as Test 1

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Table III

RESOURCE MANAGEMENT PROCESSOR STATIC TESTS

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
RMP-1	Exec POVR Interface	Verify Msg xfer from Exec to POVR	RMDR, RMPOVR, EXRM	Place Prior. Override Msg on EXRM FIFO, start Exec, stop excition at call to RMPOVR	SDC: RP-16, PTR, terminal
RMP-2	RM/DC Interface Priority Over.	Verify Msg xfer DC to RM	DCANST, EXRM RMDR, RMPOVR	Start at call to EXMES, stop at call to RMPOVR	
RMP-3	Priority Override end-to-end	Verify Priority Override	DCANST, EXRM RMDR RMPOVR, RMBUSO	Start at DCANST Stop at RMDR Return to Exec	
RMP-4	Exec/RMPRTN Interface	Verify msg xfer from Exec to PRTN	RMDR, RMPRTN EXRM	Place Prior. Return Msg. on EXRM FIFO Start Exec, stop at call to PRTN	
RMP-5	RM/DC Interface Priority Return	Verify Msg. xfer DC to RM	DCANST, EXRM RMDR, RMPRTN	Start at call to EXMES, Stop at call to RMPRTN	
RMP-6	Priority Return end-to-end	Verify Priority Return	DCANST, EXRM RMDR, RMPRTN RMBUSO	Start at DCANST, Stop at RMDR Return to Exec.	
RMP-7	Exec/RMTOVR Interface	Verify Msg xfer from Exec to RMT RMTOVR	RMDR, RMTOVR EXRM	Place Tech. Override Msg. on EXRM FIFO, Start Exec, Stop execution at call to RMTOVR	

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Table III - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
RMP-8	RM/DC Interface-Tech. Override	Verify msg. xfer DC to RM	DCANST, EXRM RMDR, RMTOVR	Start at call to EXMES, stop at call to RMTOVR	SDC:RP-16, PTR, Terminal
RMP-9	Tech. Override end-to-end	Verify Tech. Override	DCANST, EXRM, RMDR, RMTOVR, RMRAI, RMRAE	Start at DCANST Stop at RMDR Return to Exec	
RMP-10	Exec/RMTRTN Interface	Verify msg. xfer from Exec to RMTRTM	RMDR, RMTRTM, EXRM	Place Prior. Override Msg. on EXRM FIFO start Exec, stop execution at call to RMTRTN	
RMP-11	RM/DC Interface-Tech Return	Verify Msg. xfer DC to RM	DCANST, EXRM RMDR, RMTRTN	Start at call to EXMES, stop at call to RMTRTN	
RMP-12	Tech. Return end-to-end	Verify Tech. Return	DCANST, EXRM, RMDR, RMTRTN RMRAI, RMRAE, RMOPAS	Start at DCANST, stop at RMDR return to Exec	
RMP-13	Exec/RMPRIN Interface	Verify Msg. xfer from Exec to RMPRIN	RMDR, RMPRIN, EXRM	Place ET Interrupt Msg. on EXRM FIFO, start Exec, stop execution at call to RMPRIN	
RMP-14	ET Interrupt End-to-End	Verify ET Interrupt	EXRM, RMDR, RMPRIN, RMETPA	Start in ET Interrupt Routine, stop at call to RMETPA	
RMP-15	Exec/RMUP Interface	Verify Msg. xfer DC to RM	EXRM, RMDR, RMUP	Place ETF Update Msg. on EXRM FIFO, Start Exec, Stop Execution at call to RMUP	

Table III - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
RMP-16	ETF Update End-to-End	Verify ETF Update	EXRM, RMDR, RMUP, RMEMAS, RMOPAS, RMCALE, RMARPR, RMREA RMREI, RMBUSO	Plase ETF Update Msg. in IP Buffer Start Exec, stop at RMDR return to Exec	SDC:RP-16, PTR, Terminal
RMP-17	Exec/RMRAI Interface	Verify Msg. xfer from RMRAI to Exec	EXRM, RMRAI	Start at call to EXMES (SS Message) Stop after SS Message in IP Buffer	
RMP-18	SS Message End-to-End	Verify SS Message	EXRM, RMRAI	Start at RMRAI, Stop after SS Message in IP Buffer	
RMP-19	Exec/DCDR Interface	Verify Msg. xfer from Exec to DCDR	EXRM, DCDR, DCANUP	Place Modify Msg. in EXRM FIFO, Start Exec, Break point at DCANUP	
RMP-20	Exec/RMDR Interface (Modify Msg.)	Verify Msg. xfer from RMDR to Exec	RMDR, EXRM	Start at call to EXMES, stop at call to DCDR	
RMP-21	Modify Msg. End-to-End	Verify Modify Msg.	DCANST, EXRM, RMDR, DCDR, DCANUP, DCMLMC	Start at DCANST, break point at DCMLMC	
RMP-22	Exec/DCSEND Interface	Verify Msg. xfer from Exec to DCSEND	EXRM, DCSEND	Place Send Data Msg in EXRM FIFO, Stop at call to DCSEND	
RMP-23	DCSEND/DCANUP Interface (Send Data Msg.)	Verify Msg. xfer from DCANUP to DCSEND	DCANUP, DCSEND, EXRM	Start at call to EXMES, stop at call to DCSEND	

Table III - Continued

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
RMP-24	Send Data end-to-end	Verify Send Data	DCANUP, EXRM DCSEND	Start at DCANUP, Stop at DCSEND Return to EXRM	SDC:RP-16. PTR, Terminal
RMP-25	DCPOU/Exec Interface (Master Clear)	Verify Msg. xfer from DCPOU to Exec	DCPOU, EXRM	Start at call to EXMES, stop after Master Clear Sent to other Processors	
RMP-26	Master Clear end-to-end	Verify Master Clear	DCPOU, EXRM	Start at DCPOU, Stop after Master Clear Sent to other Processors	
RMP-27	DCPOU/Exec Interface (System Test Start)	Verify Msg xfer from DCPOU to Exec	DCPOU, EXRM	Start at call to EXMES, stop after System Test Msg in STE Data Buffer	
RMP-28	System Test Start end-to-end	Verify System Test Start	DCPOU, EXRM	Start at DCPOU, stop after System Test Msg. in STE Data Buffer	
RMP-29	DCPOU/Exec Interface (System Test End)	Verify Msg. xfer from DCPOU to Exec	DCPOU, EXRM	Start at call to EXMES, Stop after System Test Msg. in STE Data Buffer	
RMP-30	System Test End End-to-End	Verify System Test End	DCPOU, EXRM	Start at DCPOU, Stop after System Test Msg. in STE Data	
RMP-31	Priority Override	Verify Priority Override	EXRM, DCDR, DCANST, RMDR, RMPOVR, RMBUSO DCANUP	Start, type P___ .	

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Table III - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
RMP-32	Priority Return-Overall	Verify Priority Return	EXRM, DCDR, DCANST, RMDR, RMPRTN, RMBUSO DCANUP	Start, Type P	SDC:RP-16, PTR, Terminal
RMP-33	Tech. Override - Overall	Verify Tech. Override	EXRM, DCDR, DCANST, RMDR, RMTOVR, DCANUP	Start, Type T____	
RMP-34	Tech. Return - Overall	Verify Tech. Return	EXRM, DCDR, DCANST, RMDR, RMTRTN, RMOPAS DCANUP	Start, Type T	
RMP-35	Return All	Verify Return All	EXRM, DCDR, DCANUP, DCANST RMDR, RMPRTN, RMBUSO, RMTRTN, RMOPAS	Start, Type R	
RMP-36	Modify - Overall	Verify Modify	EXRM, DCDR, DCANST, RMDR, DCANUP	Same as 31-35	
RMP-37	Send Data Overall	Verify Send Data	EXRM, DCDR, DCSEND, DCANUP	Same as 31-35	
RMP-38	Display Update - Overall	Verify Display Update	EXRM, DCDR DCSEND, DCANUP	Same as 31-35	
RMP-39	Master Clear Overall	Verify Master Clear	EXRM, DCDR, DCANST	Start, Type M, Stop	

Table III - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
RMP-40	Same as 14				SC w/PTR, Terminal
RMP-41	Same as 16				
RMP-42	Same as 18				
RMP-43	Same as 28				
RMP-44	Same as 30				
RMP-45	Same as 31				
RMP-46	Same as 32				
RMP-47	Same as 33				
RMP-48	Same as 34				
RMP-49	Same as 35				
RMP-50	Same as 36				
RMP-51	Same as 37				
RMP-52	Same as 38				
RMP-53	Same as 39				

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3.1.2.3 Analysis Processor Tests

The AP tests shall first integrate the Executive functional group with each of the background functional groups in turn. Functional groups shall then be integrated together until the entire AP software has been integrated as a whole. The AP tests shall be as defined in Table IV. All of the tests shall be run with Micro debug from the software development center (SDC). The final AP static integration tests shall be repeated in the SC with the STE providing the stimuli and the data output capability.

3.1.2.4 System Controller Tests

The SC tests shall first integrate the executives in each of the three processors with each other. The processing between pairs of processors shall then be integrated and finally all three processors shall be integrated together. The SC static tests as defined in Table V shall be executed in the SC unit.

3.1.3 Dynamic Tests

The dynamic testing of the SC program shall use the STE and the Signal Sorter (SS) as part of the system environment. The STE shall generate pulse trains (Pulse Descriptor Words (PDW's)) to the SS and the SS shall in turn exchange messages with the SC. The STE shall also be used for displaying and storing instrumentation data. The dynamic tests shall test end-to-end processing first for a single emitter and then build gradually up to four emitters. Overload conditions shall be simulated in so far as possible. The dynamic tests shall be as defined in Table VI.

TABLE IV

Analysis Processor Static Tests

TBD

Table V

SYSTEM CONTROLLER STATIC TESTS

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
SC-1	CP/RMP Msg Transfer	Verify msg xfer from CP to RMP	EXCP, EXRMP	Send IP Msg to EXMSG in CP, Stop RMP after Msg xfer to data storage	SC, paper tape reader, CRT terminals on CP, RMP, control panels as required
SC-2	Repeat Test 1 for RMP to CP Msg. transfers				
SC-3	Repeat Test 1 for CP toAP Msg. transfers				
SC-4	Repeat Test 1 for AP to CP Msg. transfers				
SC-5	Repeat Test 1 for RMP to AP Msg. transfers				
SC-6	Repeat Test 1 for AP to RMP Msg. transfers				
SC-7	RMP/CP/SS Msg. transfer	Verify msg. xfer from RMP to SS	EXCP, EXRMP	Send IP Msg. to EXMSG in RMP, stop CP after msg. xfer to SS buffer	Same as Test 1
SC-8	SS/CP/RMP Msg. transfer	Verify Msg. xfer from SS to RMP	EXCP, EXRMP	Place IP Msg. in SS buffer, start EXCP, stop RMP after Msg xfer to data storage	Same as Test 1
SC-9	Repeat Test 7 for AP to SS Msg. transfers				
SC-10	Repeat Test 8 for SS to AP Msg. transfers				
SC-11	CP/RMP/STE Msg. transfer	Verify msg. xfer from CP to STE	EXCP, EXRMP	Send IP Msg. to EXMSG in CP, Stop RMP after Msg. xfer to STE buffer	Same as Test 1

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Table V - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
SC-12	STE/RMP/CP Msg transfer	Verify msg xfer from STE to CP	EXCP, EXRMP	Place IP msg in STE buffer, start EXRMP, stop CP after msg xfer to data storage	Same as Test 1
SC-13	Repeat Test 11 for	AP to STE Msg transfers			
SC-14	Repeat Test 12 for	STE to AP Msg transfers			
SC-15	CP/RMP Multi-Msg xfer	Verify multiple-msg xfer	EXCP, EXRMP	Queue IP msgs in CP, stop RMP, verify multi-msg xfer to data storage	Same as Test 1
SC-16	Repeat Test 15 for	RMP to CP msg transfers			
SC-17	Repeat Test 15 for	CP to AP msg transfers			
SC-18	Repeat Test 15 for	AP to CP msg transfers			
SC-19	Repeat Test 15 for	RMP to AP msg transfers			
SC-20	Repeat Test 15 for	AP to RMP msg transfers			
SC-21	RMP/CP/SS Multi-msg xfer	Verify multiple-msg xfer from RMP to SS	EXCP, EXRMP	Queue IP msgs in RMP, dummy routine empties SS Buffer, verify msg xfer	Same as Test 1
SC-22	Repeat Test 21 for	AP to SS msg transfers			
SC-23	CP/RMP/STE multi-msg xfer	Verify multiple-msg xfer	EXCP, EXRMP	Queue IP msgs in CP, stop RMP, verify multiple msg in STE buffer	Same as Test 1

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Table V - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
SC-24	Repeat Test 23 for AP to STE msg. transfers				
SC-25	SC end-to-end NE Alrt, lethality = Ø	Verify NE Alrt process with lethality = Ø	EXCP, SODR, ANDR, ECDR, AB1DR, EXRM, RMDR, DCDR	Input NE Alrt Msg from SS buffer, note display, ET, TG outputs	Same as Test 1
SC-26	SC end-to-end NE Alrt, lethality = Ø, E2PLAT = MSEA	Verify NE Alrt process with lethality = Ø and platform type = NAVY (Sea)	Same as Test 25	Same as Test 25	
SC-27	SC end-to-end PTDW update lethality = Ø	Verify PTDW update with lethality = Ø		Repeat Test 25 then insert PTDW, note display, ET, TG outputs	
SC-28	SC end-to-end PTDW update, no match lethality = Ø	Verify PTDW update/ drop of emitter no longer of concern		Same as Test 27	
SC-29	SC end-to-end NE Alrt, lethality ≠ Ø	Verify NE Alrt proc with lethality ≠ Ø		Same as Test 25 plus note output buffer to SS	
SC-30	SC end-to-end PTDW update lethality, ≠ Ø	Verify PTDW update with lethality ≠ Ø		Repeat Test 29 then insert PTDW, note display, ET, TG outputs	
SC-31	SC end-to-end PTDW update lethality, ≠ Ø no match	Verify PTDW update/drop of emitter no longer of concern		Same as Test 30	

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Table V - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
SC-32	SC end-to-end Inact File Alrt	Verify inactive file alert processing	Same as Test 25	Repeat Test 29 then insert inact file alert, note display, ET,. TG outputs	Same as Test 1
SC-33	SC end-to-end SS buffer msgs.	Verify processing of SS buffer msgs.	EXCP, SODR, SOSM1, EXRM, SMDR, SMOFP	Input SS buffer msgs from SS buffer, note data extraction output	
SC-34	CP/AP aux bus set-up	Verify CP/AP process through set-up of aux bus interface	EXCP, SODR, AB1DR, EXAP, AB2DR, ABIDR	Input NE Alrt msg from SS buffer with TPAMP > ATC, stop when start SPDW Msg rcvd from AP, examine ABI control words	

Table VI

DYNAMIC TESTS

Test No.	Test	Purpose	Subprograms Involved	Test Method	System Environment
D-1	Single emitter, stdy scan, NOFA1	Verify CP NOFA1 processing	EXCP, SODR, ANDR, ECDR	Input single train of PDW's to SS, display/record data extraction points	SC, STE, SSS
D-2	Delete single emitter	Verify CP deletion processing	Same as Test 1	Repeat Test 1, then stop PDW's, display/record deletion msgs	Same as Test 1
D-3	Single emitter, stdy scan, NOFA2	Verify CP NOFA2 processing	Same as Test 1 plus AB1DR	Same as Test 1	
D-4	Single emitter, stdy scan, EOC	Verify CP/RMP EOC process, lethality = Ø	EXCP, SODR, ANDR, ECDR, AB1DR, EXRM, RMDR, DCDR		
D-5	Single emitter, stdy scan, vary parameters EOC → NOFA1	Verify CP/RMP process for EOC → NOFA1	Same as Test 4	Input single train of PDW's with varying param., display/record data extraction points	
D-6	Single emitter, stdy scan, vary parameters NOFA1 → EOC	Verify CP/RMP process for NOFA1 → EOC		Same as Test 5	
D-7	Single emitter, stdy scan, vary param., EOC_1 → EOC_2	Verify CP/RMP process for EOC_1 → EOC_2			

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Table VI - continued -

Test No.	Test	Purpose	Subprograms Involved	Test Method	System Environment
D-8	Single emitter, stdy scan, EOC, vary azimuth	Verify CP/RMP angle tracking	Same as Test 4	Input single PDW train with varying azimuth, note display output angle tracking	Same as Test 1
D-9	Single emitter, stdy scan, lethality $\neq \emptyset$	Verify CP/RMP resource management		Same as Test 1	
D-10	Repeat Test 9 then stop PDW train	Verify CP/RMP deletion processing		Same as Test 1 then stop PDW train, note commands to ET, TG, SS	
D-11	Repeat Test 9, vary param. EOC → NOFA1	Verify CP/RMP drop track processing		Same as Test 5	
D-12	Repeat Test 6 with lethality $\neq \emptyset$	Verify CP/RMP pick up track			
D-13	Repeat Test 1 for two trains	Verify CP NOFA1 proc for two emitters		Input two PDW trains to SS, display/record data extraction points	
D-14	Repeat Test 2 for two trains	Verify CP deletion process for 2 emitters		Repeat Test 13 then stop PDW's; display/record deletion msgs	
D-15	Repeat Test 4 for two emitters				
D-16	Repeat Test 4 for three emitters				
D-17	Repeat Test 4 for four emitters				
D-18	Repeat Test 5 for two emitters				

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Table VI - continued -

Test No.	Test	Purpose	Subprogram Involved	Test Method	System Environment
D-19	Repeat Test 6 for two emitters				Same as Test 1
D-20	Repeat Test 9 for two emitters				
D-21	Repeat Test 9 for three emitters				
D-22	Repeat Test 9 for four emitters				
D-23	Repeat Test 10 for four emitters, drop one at a time				
D-24	Single emitter, priority logic	Verify RM priority logic	Same as Test 4	Load up jam status & resource files & repeat Test 1	
D-25	Repeat Test 24 for two emitters, lethality 2 > lethality 1 > lowest lethality in priority table				
D-26	Repeat Test 25 for three emitters, lethality 3 > lethality 2				
D-27	Repeat Test 26 for four emitters, lethality 4 > lethality 3				
D-28	Single emitter, steady scan analysis	Verify scan analysis for steady scan	Same as Test 4 plus EXAP, AB2DR, ABIDR, ABRDR, ABDDR	Same as Test 1	Same as Test 1
D-29	Single emitter, conscan analysis	Verify scan analysis for conscan	Same as Test 28		
D-30	Single emitter, sector scan analysis	Verify scan analysis for sector scan			
D-31	Single emitter, circular scan analysis	Verify scan analysis for circular scan			
D-32	Repeat Test 28 for two emitters				

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Table VI - continued -

Test No.	Test	Purpose	Subprograms Involved	Test Method	System Environment
D-33	Repeat Test 29 for two emitters				
D-34	Repeat Test 30 for three emitters				
D-35	Repeat Tests 29 and 30 for two emitters each				
D-36	AP buffer over-load/time-out proc	Verify AP buffer overload/time-out processing	Same as Test 28 plus ABTCK	Load up AMT and AAT in AP, and repeat Test 29	Same as Test 1

3.1.4 Schedule

The schedule for the tests specified in this test plan shall be as shown in Figure 1. The Analysis Processor (AP) tests and the System Management 2 Tests in the Resource Management Processor (RMP) shall be of lower priority and hence shall be integrated later in the schedule. However, given that the Classification Processor (CP) and the RMP are integrated as shown by week 11, system integration may proceed on its schedule.

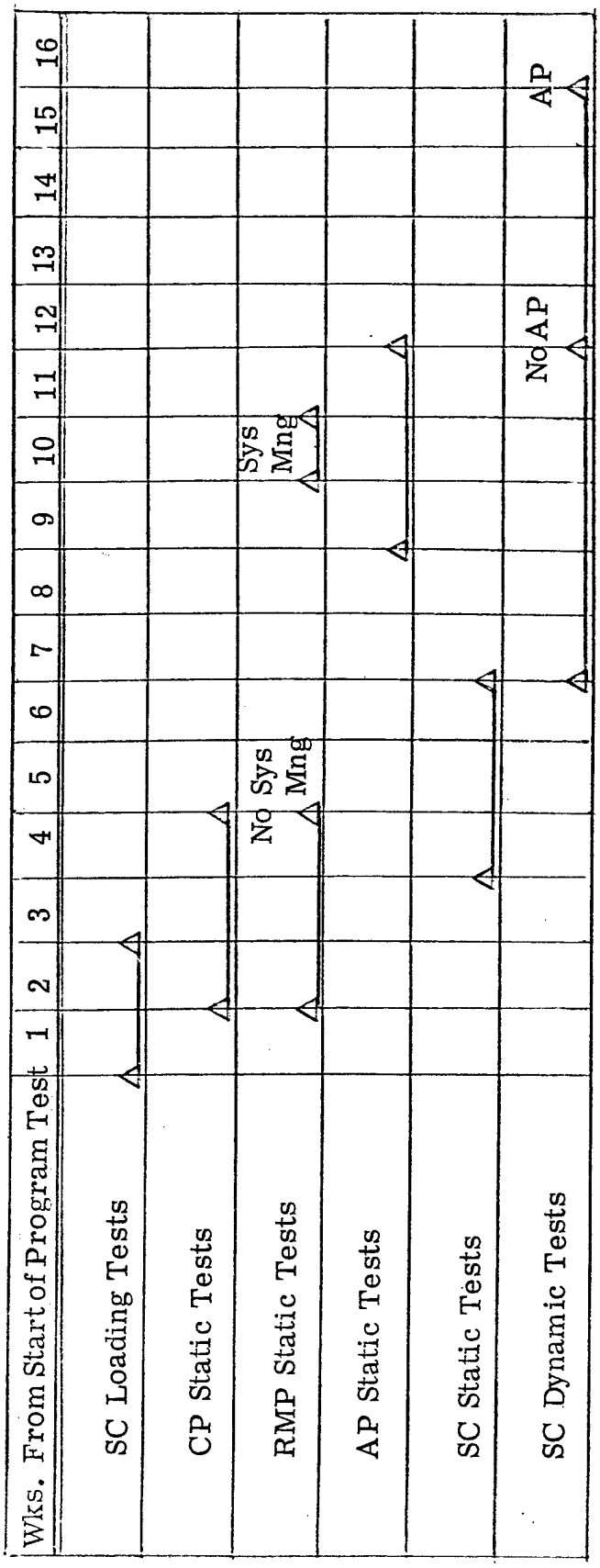

Figure 1. Program Test Schedule

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3.2 REFERENCE DOCUMENTS

The documents used specifically in the formation of the requirements for these tests are so designated in Section 2.0.

3.3 DETAILED REQUIREMENTS

3.3.1 Test Management

The total responsibility for testing the SC program shall reside with the contractor. The software manager shall have direct responsibility for establishing test requirements, writing test procedures, performing tests, and documenting results. All documentation and test results shall be available for review by the procuring agency.

3.3.2 Personnel Requirements

All personnel required for program testing shall be provided by the contractor. The number of personnel, the job classification, and their duties shall be as given in Table VII.

Table VII

PROGRAM TEST PERSONNEL REQUIREMENTS

Classification	Number Required	Duty Requirements	Period Required
Test Director	1	Organize and manage the development of acceptance test plan procedures and be responsible for insuring that these plans conform to the requirements of this specification.	Full time, 2 months
Test Programmer	3	Perform actual tests and determine that test results conform to requirements.	Full time, 2 months
Support Hardware Coordinator	1	Be responsible for securing all support hardware and maintaining such hardware during acceptance tests.	Full time, 1 month. Part time, 1 month.
Support Software	1	Be responsible for specifying & generating all support software and maintaining such software during acceptance tests.	Part time, 2 months
System Controller Maintenance	1	Be responsible for system controller maintenance during acceptance tests.	Part time, 2 months.

3.3.3 Hardware Requirements

Two hardware configurations shall be required for program test. The Software Development Center (SDC) configuration shown in Figure 2 shall be used for tests that do not require execution in the actual SC hardware. The configuration involving the Special Test Equipment (STE) shown in Figure 3, shall be used for tests that execute in the SC itself. The detailed requirements for the hardware shall be as specified in Table VIII.

3.3.4 Supporting Software Requirements

The supporting software programs required for SC program tests shall consist, as a minimum, of those programs listed in Table IX.

3.3.5 Functional Test Design

The functions defined in Section 3.1 shall be tested according to the specifications of this paragraph. The tests are classified as loading, static, and dynamic tests. In all cases the method of data collection shall be CRT, flexible disc, or both.

3.3.5.1 Loading Tests

The inputs and the outputs for the loading tests shall be as specified in Table X.

3.3.5.2 Static Tests

3.3.5.2.1 Classification Processor Tests - The inputs and the outputs for the CP Static Tests shall be as specified in Table XI. The default ETF entry shall be as shown in Figure 4 and the default NE Alert message and the default PTDW message shall be as shown in Figure 5.

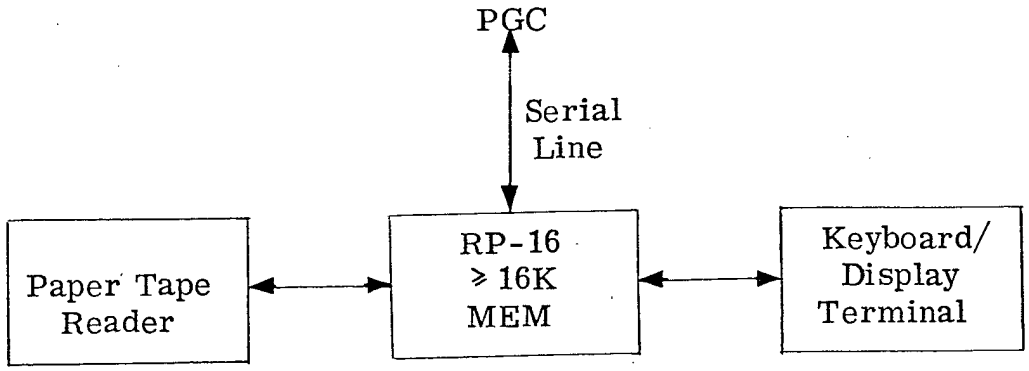

Figure 2. Software Development Center Hardware Configuration

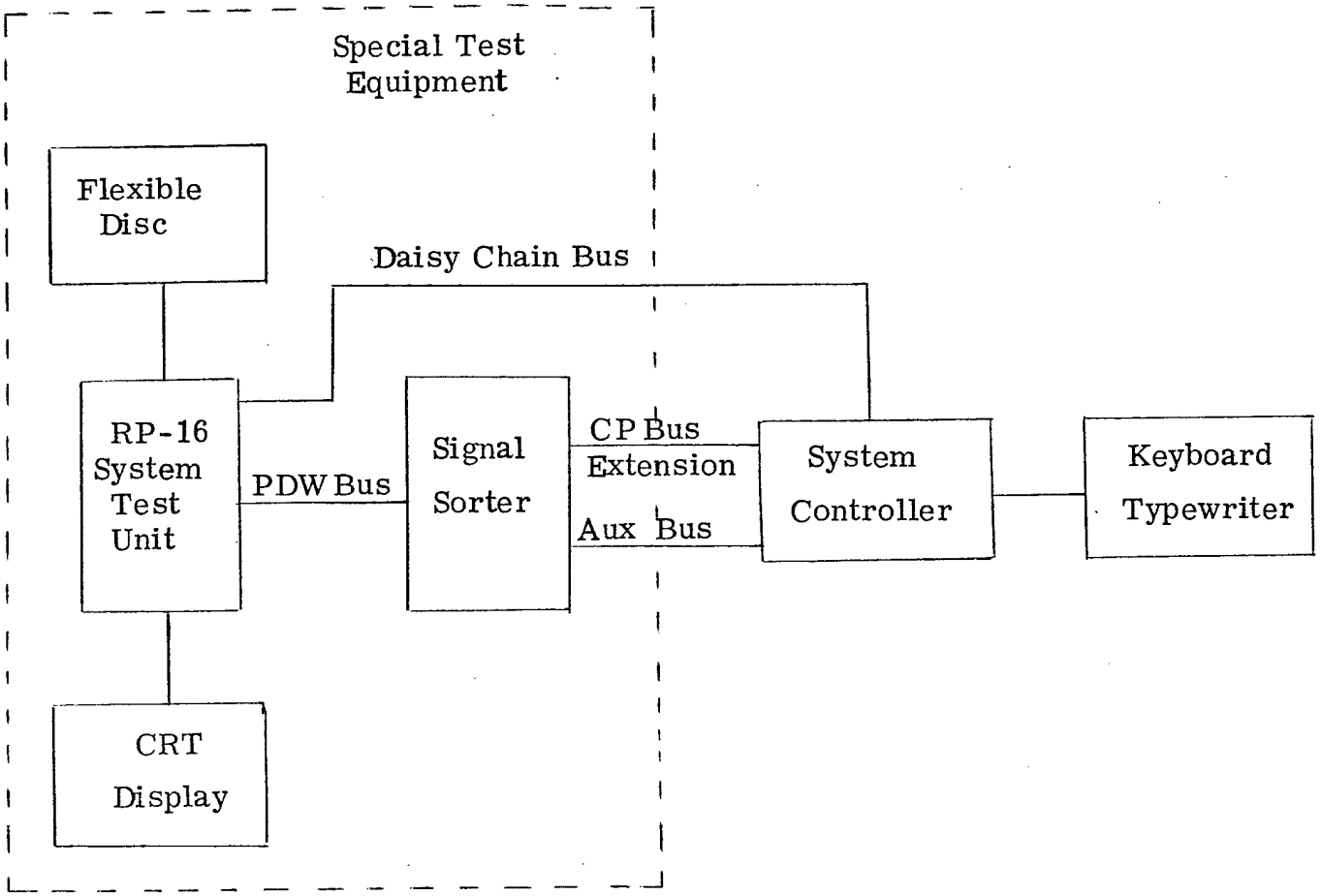

Figure 3. STE Hardware Configuration

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Table VIII

HARDWARE REQUIREMENTS FOR PROGRAM TEST

Config-uration	Item	Model	No. Req'd.	Period of Usage	Source
SDC	RP-16, 16K MEM	Special	2	3 months	ESD
	LSI Display	ADM-3	2	3 months	ESD
	Paper Tape Reader	Remex	1	3 months	ESD
	Serial Line	Special	1	3 months	ESD
STE	System Controller	Special	1	2 months	EDL
	Decwriter	LA36/ NF02	1	2 months	ESD
	RP-16 Test Unit	Special	1	2 months	STE
	Remex Disc	RFS7400BA	1	2 months	STE
	LSI Display	ADM-3	1	2 months	STE
	Signal Sorter	Special	1	2 months	EDL

Table IX

SUPPORT SOFTWARE REQUIREMENTS

Support Program	Description	Resident In
Linking Loader	Provides control and program data to loader in SC to input SC programs.	STE
Data Extraction	Provides capability to output computer status and data from data extraction points in the operational software.	SC
System Test	Provide capability to display data on CRT and/or to record data on disc file. Accept operator commands. Provides capability to accept messages from the SC simulating the interfaces to Sorter, PE/ET, Tech Gen, and Display/Control.	STE
PDW Generator	Provide capability to input PDW's to the SS for up to 4 emitters. Provide capability to vary parameter values dynamically.	STE
Operating System	Provides capability to execute loader and other programs in STE.	STE
Microde-bug	Provides capability to single step programs, to run all or part of the program, to modify memory locations, to trace program steps, to examine register contents, and to exit at breakpoints.	SC
Debug	Provides capability to single step programs, to run all or part of the program, to modify memory locations, to trace program steps, to examine register contents, and to exit at breakpoints.	STE

Table X

LOADING TEST DESIGN REQUIREMENTS

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
L-1	None	Memory patterns	RMP Loader direct	Same as input
L-2	None	Memory patterns	CP Loader direct	Same as input
L-3	None	Memory patterns	AP Loader direct	Same as input
L-4	None	Memory patterns	SC Loader direct	Same as input
L-5	None	Memory patterns	RMP Loader/STE	Same as input
L-6	None	Memory patterns	CP Loader/STE	Same as input
L-7	None	Memory patterns	AP Loader/STE	Same as input
L-8	None	Memory patterns	SC Loader/STE	Same as input

Table XI

CP STATIC TEST DESIGN REQUIREMENTS

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-1	None	NE Alrt default, exec FIFO	Exec/SMP interface	Stop at SONE1 call X = ptr to NE Alrt msg. A = EFN
CP-2	ETF storage defined ALT no links	NE Alrt default, SS buffer	Exec/SMP end-to-end SONE 1	Stop at SODR Rtn to exec ETF loaded correctly EFPIV = 1 Anal req msg. DI = 1 Anal request return
CP-3	Same as test 2	NE Alrt: TQPRI = 13, SS buffer	Same as test 2	Same as test 2 except DI= 1 in Anal Req Msg EFPIV = Ø
CP-4	ETF storage defined ALT with Az links	Same as test 2	Same as test 2	Stop at return to Exec Az links patched corr-ectly
CP-5	None	Default PTDW in exec FIFO	Exec/SMP Interface	Stop at SOUP Call X = ptr to PTDW A = EFN
CP-6	Default ETF entry except EFID←EUCLS ALT, single link to EFN	Default PTDW in SS Buffer	SOUP unclass Rtn	Stop of return to Exec Check that ETF contents unchanged-immediate rtn. No analysis req rtn
CP-7	Default ETF entry except EFID ← ENA1 ALT, single link to EFN Δ F = X'3Ø' Δ PW = X'2' Δ PRI = X'4Ø'	Same as test 6	SONA1 within limits pro-cessing	Stop at return to Exec No analysis req return EF AZ, EFPAMP updated ALT updated - link moved to new azimuth

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Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-8	Default ETF entry except EFID ← ENA1 ALT, single link to EFN ΔF = ΔPW = ΔPRI = Ø	Same as test 6	SONA1 out of limits processing	Stop at return to Exec No alaysis req return EF AZ, EFPAMP, EFAVPI, EFREQ, EFPW updated Class Msg. on FIFO
CP-9	Same as test 8 except EFID ← ENA2	Same as test 6	SON21 out of limits processing	Same as test 8
CP-10	Same as test 7 except EFID ← ENA2 ATC = X'1F'	Same as test 6	SON21 within limits, TPAMP < ATC processing	Stop at return to Exec No analysis req return EFAZ, EFPAMP updated
CP-11	Same as test 10 except ATC ← X'1Ø'	Same as test 6	SON21 within limits, TPAMP > ATC processing	Stop at return to Exec Analysis request rtn Anal request msg. on FIFO
CP-12	Default ETF entry EL1 without input emitter included	Same as test 6	SOOC1 no Cand processing	Stop at return to Exec No Analysis request rtn EFAZ, EFPAMP, EFID EFAVPI, EFREQ, ELN EFPW, EFDISP updated Update Msg. on FIFO
CP-13	Default ETF entry EL1 with input emitter ATC ← X'1F'	Same as test 6	SOOC1 Cand, TPAMP < ATC processing	Stop at return to Exec Anal req return Analysis is not wanted EFSTYP ← ECIR EFSPRD ← All 1's EFSIND ← Ø

Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-14	Same as test 13 except ATC←X'1Ø'	Same as test 6	SOOC1 Cand, TPAMP > ATC processing	Stop at return to Exec Anal Req return Analysis wanted EFSTYP, EFSPRD unchanged
CP-15	None	Inactive File Alrt SFN = EFN	Exec/SMP Interface	Stop at call to SODEL X = ptr to Inact File Alrt A = EFN
CP-16	Default ETF entry	Same as test 15	SODEL processing	Stop at return to Exec No Anal request rtn ETF entry initialized Delete File Msg in SS buffer, update Az links Update Msg in IP buffer
CP-17	None	MFF Message SFN = EFN	Exec/SMP Interface	Stop as SOMFF call X = ptr to MFF Msg A = EFN
CP-18	Default ETF entry	Same as test 17	SOMFF processing to set EFMF	Stop at return to Exec No anal request rtn EFMF = 1
CP-19	Default ETF entry except EFMF = 1	Same as test 17	SOMFF processing for already set EFMF	Same as test 18
CP-20	None	IB <1/4 full OR IB >3/4 full OR Files Full OR Th Files Full	Exec/SMP Interface	Stop at SOSM1 call X = ptr to SS Msg

Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-21	None	Same as test 20	SOSM1 Processing	Stop at return to Exec No analysis request rtn SS Msg in IP buffer
CP-22	None	Throttle Alert	Exec/SMP Interface	Stop at SOTHR call X = ptr to Th Alrt Msg A = EFN
CP-23	Default ETF entry	Throttle Alert SFN = EFN TFN, RF Non-zero TFA, TFF don't care	SOTHR Processing	Stop at return to Exec No Anal Request rtn EFTH = 1 EFRF, EFTFN updated
CP-24	None	Cam File Dump OR AOA Readout OR Conf File Creation OR Error Alert OR Long Pulse Param OR Bus Hung OR Watchdog Timer OR ALR-50 OR NPDW Msg OR Memo Dump OR BIT Status	Exec/SMP Interface	Stop at SOINS call X = ptr to SS Msg A = EFN (if applicable)
CP-25	Initialize IP Buffer	Same as test 24	Exec/Data Extraction end-to-end test	Stop at return to Exec No Anal Request rtn SS Msg in IP buffer

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Table XI

CP STATIC TEST DESIGN REQUIREMENTS

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-26	None	Analysis Return Msgs with RMC = 1, 2, . . . , 9 as input to EXMSG	Exec/Anal Ret Interface	Stop at Call to ANNE2, ANNE3, ANNA2, . . . X = ptr to Anal Ret Msg A = EFN
CP-27	Default ETF entry except EFPWX = Ø	Analysis Ret Msg with RMC = 1 as input to EXMSG	ANNE2 Processing	Stop at rtn to Exec Anal Request rtn No Anal wanted EFPWV = 1
CP-28	Default ETF entry except EFV = Ø	Anal Ret Msg with RMC = 2 as input to EXMSG	ANNE3 Processing with EFQF good quality	Stop at rtn to Exec No Anal Req rtn EFV = 1
CP-29	Default ETF entry except EFQF = 14	Same as test 28	ANNE3 Processing with EFQF bad quality	Same as test 28 except EFV = Ø Class Msg on FIFO
CP-30	Default ETF entry except EFV = EFPWV = Ø Dummy AB1DR	Anal Ret Msg with RMC = 1 as input to EXMSG	ANNE2, ANNE3 Processing	Stop at end of ANNE3 No Anal Req rtn EFPWV = EFV = 1 Class Msg on FIFO
CP-31	Default ETF entry Dummy AB1DR with STY ← NULL	Anal Ret Msg with RMC = 3 as input to EXMSG	ANNA2 NUL Meas processing	Stop at rtn to Exec No Anal Request rtn ETF entry unchanged
CP-32	Default ETF entry except EFSTY ← ECIR	Anal Ret Msg with RMC = 3 as input to EXMSG ANSTY = ESDLB ANSPR = X'4Ø'	ANNA2 SDLB meas processing, within limits	Stop at rtn to Exec No Anal request rtn ETF entry unchanged EFSIND Complemented

Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-33	Default ETF entry EL1 without Cand. for ETF entry	Anal Ret Msg with RMC= 3 as input to EXMSG ANSTY = ECIR ANSPR = X'4Ø'	ANNA2, Level 1 no Cand. return	Stop at rtn to Exec No Analysis request rtn EFID ← ENA1 EFSTYP ← ECIR EFELN, ← Ø EFDISP ← EUNK
CP-34	Default ETF entry EL1 with Cand. for ETF entry, EL2 without Cand. for ETF entry Δ SPRD = Ø EFSTYP = ESDLB	Anal. Ret Msg with RMC= 3 as input to EXMSG ANSTY = ESECT ANSPR = X'41'	ANNA2, Level 1 Search Cand return, Level 2 no Cand return	Stop at rtn to Exec No analysis request rtn EFID ← ENA2 EFSPRD ← X'41' EFELN ← Ø EFDISP ← EUNK
CP-35	Same as test 34 except EL2 has Cand for ETF entry, EFSTYP = ECIR	Same as test 34	ANNA2, Level 2 Cand return	Stop at rtn to Exec Analysis request rtn Analysis is not wanted Anal req Msg on FIFO
CP-36	Candidate list with more than one Cand with diff E2 WTFACT in EL2 Default ETF entry	Anal Ret Msg with RMC= 4 as input to EXMSG	ANNA3 Processing	Stop at return to EXEC No anal request rtn EFID, EFDISP correspond Correct EFELN Update Msg in FIFO
CP-37	Same as test 35 with more than one Cand with diff E2WTFACT in EL2 Dummy AB1DR	Same as test 34 except ANSTY = ECON	ANNA2, ANNA3 Processing	Stop at end of ANNA3 No anal request rtn EFID, EFDISP correspond EFSTYP ← ECON, EFSPRD ← X'41' Correct EFELN Update Msg in FIFO

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Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-38	Default ETF entry Cand list EL2 without matches for Cand List	Anal Ret Msg with RMC= 5 as input to EXMSG ANSTY ← NUL	ANOC2, Level 2 no Cand processing	Stop at rtn to Exec No Anal request rtn ETF unchanged Update Msg on FIFO
CP-39	Default ETF entry Cand list with EFELN EL2 with matches for Cand list	Same as test 38 except ANSTY ← ESECT	ANOC2, update Link processing	Stop at rtn to Exec Anal request rtn Anal not wanted Anal Req Msg in FIFO RMC = 7 ETF unchanged
CP-40	Same as test 39 except EFELN not in Cand List	Same as test 38 except ANSTY ← ECON	ANOC2, NE link processing	Stop at rtn to Exec Anal request rtn Anal not wanted Anal Req Msg in FIFO RMC = 6 EFSTYP ← ECON
CP-41	Same as test 39 except add Dummy AB1DR	Same as test 39	ANOC2, ANOC4 Process	Stop at end of ANOC4 No analysis request rtn Update Msg in FIFO ETF unchanged
CP-42	Same as test 40 except add Dummy AB1DR	Same as test 40	ANOC2, ANOC3 Process	Stop at end of ANOC3 No anal request rtn Update Msg in FIFO EFSTYP ← ECON New EFID, EFELN
CP-43	Default ETF entry Cand List EL2 with matches for Cand list	Anal Ret Msg with RMC= 8 as input to EXMSG ANSTY ← ECIR	ANEC2 Processing	Stop at rtn to Exec Analysis request rtn No anal wanted Anal Req Msg on FIFO EFSTYP ← ECIR

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Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-44	Cand List with more than one Cand with diff E2WTFACT in EL2 Default ETF entry	Anal Ret Msg with RMC= 9 as input to EXMSG	ANEC3 Processing	Stop at rtn to Exec No anal request rtn EFID, EFDISP correspond Correct EFELN Update Msg in FIFO
CP-45	Same as test 43 with more than one Cand with diff E2WTFACT in EL2 Dummy AB1DR	Same as test 43	ANEC2, ANEC3 Process	Same as test 44 except stop at end of ANEC3
CP-46	None	Class Msg on FIFO	Exec/ECDR Interface	Stop after call to ECDR X = ptr to Class Msg
CP-47	Default ETF entry EL1 with no Cand for ETF entry	Class Msg as input to EXMSG	ECLV1 no Cand return	Stop at return to Exec EFID ←—ENA1 EFDISP←—EUNK
CP-48	Default ETF entry EL2 with Cand for ETF entry ATC = X'1F'	Same as test 47	ECLV1 Cand return EFPAMP < ATC	Stop at return to EXEC Anal Req Return No Anal wanted Correct Cand list
CP-49	Same as test 48 except ATC = X'ØØ'	Same as test 47	ECLV1 Cand return EFPAMP > ATC	Stop at return to EXEC Anal Req Return Analysis wanted
CP-50	Default ETF entry except that EFPWV = EFV = EFPIV = Ø	Same as test 47	ECLV1 unclass return	Stop at return to Exec No anal request return EFID←—EUCLS EFDISP←—EUNK

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Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-51	ETF storage defined ALT with no az links Dummy AB1DR	Default NE Alrt Msg as input in SS buffer	NE Processing end-to-end, normal SONE1, ANNE2, ANNE3	Stop at end of ANNE3 ETF loaded correctly EFPIV = EFPWV = EFV = 1 Dummy AB1DR called twice. No Anal Req rtn. Class Msg on FIFO
CP-52	Same as test 51	Same as test 51 except TQPRI = TQPW = TQF = 15	NE Processing end-to-end, invalid SONE1, ANNE2, ANNE3	Same as test 51 except EFPIV = EFPWV = EFV = Ø
CP-53	Default ETF entry EL2 with Cand for ETF entry ATC = X'1Ø' Dummy AB1DR	Class Msg as input to EXMSG	Emitter Class end-to-end ECDR, ANEC2, ANEC3	Stop at end of ANEC3 No Anal request rtn Dummy AB1DR called twice. EFID, EFDISP correspond Correct EFELN Update Msg in FIFO
CP-54	ETF storage defined ALT with no Az links EL2 with Cand for ETF entry. ATC = X'1Ø' Dummy AB1DR	Same as test 52	NE Proc/Emit Class, unclassified processing SONE1, ANNE2, ANNE3, ECDR	Stop at end of ECDR No Anal request rtn ETF loaded correctly. EFPIV = EFPWV = EFV = Ø EFID ← EUCLS EFDISP ← EUNK Dummy AB1DR called two times
CP-55	Same as test 54	Same as test 51	NE Proc/Emit Class, Total processing SONE1, ANNE2, ANNE3 ECDR, ANEC2, ANEC3	Stop at end of ANEC3 No Anal request rtn ETF loaded correctly. Dummy AB1DR called four times Update Msg on FIFO

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Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-56	Default ETF entry except EFID ← ENA2 ALT, no links Δ F = X'3Ø' Δ PW = X'2' Δ PRI = X'4Ø' ATC = X'1Ø' Scan Anal Ret: STY = ESECT	Default PTDW in SS buffer	Update processing, NOFA2; within limits SON21, ANNA2	Stop at end of ANNA2 No anal request rtn EFAZ ← TAZ EFPAMP ← TPAMP ALT updated
CP-57	Same as test 56 except STY ← ECIR plus EL2 has Cand for ETF entry Dummy AB1DR	Same as test 56	Update processing, NOFA2, scan type changed, SON21, ANNA2, ANNA3	Stop at end of ANNA3 No anal request rtn EFID, EFDISP correspond EFSTY ← ECIR Correct EFELN Update Msg in FIFO Dum. AB1DR called twice
CP-58	Default ETF entry EL2 with input emitter included. ATC = X'1F' EFELN not in Cand list Dummy AB1DR	Same as test 56	Update processing, EOC, PAMP < ATC, Reidentify SOOC1, ANOC2, ANOC3	Stop at end of ANOC3 No anal request rtn Update Msg in FIFO EFSTY ← ECIR EFSPRD ← All 1's New EFID, EFELN
CP-59	Same as test 58 except ATC = X'1Ø', EFELN in Cand list	Same as test 56	Update processing, EOC, PAMP > ATC SOOCI, ANOC2, ANOC4	Stop at end of ANOC4 No anal request rtn Update Msg in FIFO ETF unchanged
CP-60	Same as test 51			
CP-61	Same as test 52			
CP-62	Same as test 53			

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Table XI - continued -

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
CP-63	Same as test 54			
CP-64	Same as test 55			
CP-65	Same as test 56			
CP-66	Same as test 57			
CP-67	Same as test 58			
CP-68	Same as test 59			
CP-69	EL1 entries	NE Alrt Msg with TPAMP < ATC	Null anal rtn from AB1DR when no anal wtd request is made	Null analysis return msg from AB1DR

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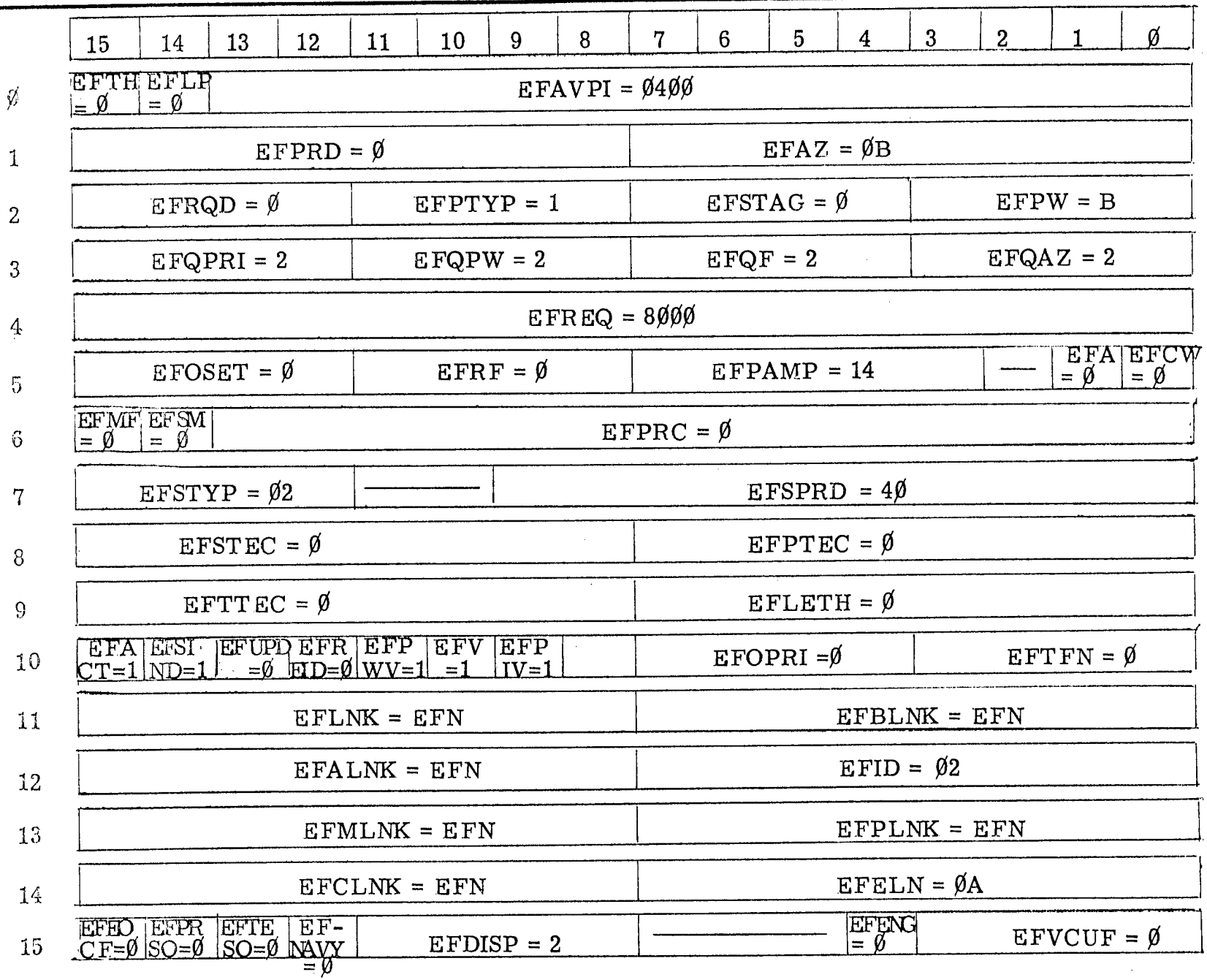

Figure 4. Default ETF Entry

Note: All numbers in hexidecimal

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BIT POSITION

15 — 8	7 — 0
OP CODE	SFN = EFN

15 — 12	11	10	7 — 0
LTOA 4 MSB = Ø	N S Ø	P P Ø	TAZ = Ø C

15 — 0
LTOA (LS 16 BITS) = Ø

15	14 — 0
SCH R Ø	Ø PRIA = Ø42Ø

15 — 0
ØØ PRIB = Ø38Ø

15 — 8	7 — 4	0
TCODE = Ø	TTAMP = Ø	TPW = C

15 — 12	7 — 4	0
TQPRI = 2	TQPW = 2	TQF = 2	TQAZ = 2

15 — 0
TRACK FREQUENCY = 8Ø2Ø

15 — 13	9 — 4	3	2	1	0
	TCOUNT = Ø	TPAMP = 15	TV 1	TA Ø	TCW Ø	TT Ø

OP Code = 8 Ø PTDW Message

OP Code = 8 1 NE Alert Message

Note: All numbers in hexidecimal

Figure 5. Default PTDW or NE Alert Message

3.3.5.2.2 Resource Management Processor Tests - The inputs and the outputs for the RMP Static Tests shall be as specified in Table XII.

3.3.5.2.3 Analysis Processor Tests - The inputs and the outputs for the AP Static Tests shall be as specified in Table XIII.

3.3.5.2.4 System Controller Tests - The inputs and the outputs for the SC Static Tests shall be as specified in Table XIV.

3.3.5.3 Dynamic Tests

The inputs and the outputs for the SC Dynamic Tests shall be as specified in Table XV.

Table XII

RMP STATIC TEST DESIGN REQUIREMENTS (1 of 4)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
RMP-1	None	Priority Override Msg.	Exec/RMPOVR Interface	Stop at call to RMPOVR. X = ptr. to Priority Over. Msg., (X) + 2 = EFN, (X) + 3 = PRIO
RMP-2	EFN, PRIO in Priority Over. Msg.	EXMES call	DC/RMPOVR Interface	Same as 1
RMP-3	Priority File, Lethalities in ETF, Threat Total	Start DCANST	Priority Override	Priority File correctly ordered
RMP-4	None	Priority Return Msg.	Exec/RMPRTN Interface	Stop at call to RMPRTN. X = ptr. to Priority Over. Msg., (X) + 2 = EFN, (X) + 3 = PRIO
RMP-5	EFN, RALL in Priority Return Msg.	EXMES call	DC/RMPRTN Interface	Same as 4
RMP-6	Priority File, Lethalities in ETF, Threat Total	Start DCANST	Priority Return	Priority File correctly ordered
RMP-7	None	Tech. Over. Msg.	Exec/RMTOVR Interface	Stop at call to RMTOVR, X = ptr. to Tech. Over. Msg., (X) + 2 = EFN, (X) + 3 = TECH.
RMP-8	EFN, TECH in Tech. Over. Msg.	EXMES call	DC/RMTOVR Interface	Same as 7
RMP-9	TESO = 0	Start DCANST	Tech. Override	TESO = 1, correct lethality

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Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
RMP-10	None	Tech. Return Msg.	Exec/RMTRTN Interface	Stop at call to RMTRTN, X = ptr. to Tech Return Msg., (X) + 2 = EFN, (X) + 3 = TALL
RMP-11	EFN, TALL in Tech Return Msg.	EXMES call	DC/RMTRTN Msg.	Same as 10
RMP-12	TESO = 1, Lethalities in EL2	Start DCANST	Tech. Return	TESO = 0, correct lethality
RMP-13	None	ET Interrupt Msg.	Exec/RMPRIN Interface	Stop at call to RMPRIN. X = ptr. to ET Intpt Msg. (X) + 2 = Drop-Track Word
RMP-14	Drop-Track Word in Register	Start after Drop-Track Word Read	ET Interrupt Processing	Stop at call to RMETPA, correct CNUM
RMP-15	None	ETF Update Msg.	Exec/RMUP Interface	Stop at call to RMUP X = ptr to ETF Update Msg., (X) + 2 = EFN, delete flag
RMP-16	Dummy ETF	ETF Update Msg. in IP Buffer	ETF Update	Correct Leth, Tech, Priority File order
RMP-17	Data in SS Mesg.	Start at call to EXMES	SS Message	Correct Msg. and data in IP buffer
RMP-18	Dummy ETF, PF PRIO, TECH	Start at RMRAI	SS Message	Correct Msg. and data in IP buffer
RMP-19	None	Modify Msg.	Modify, Display Update	DMODI= 1 1st time, then = 0
RMP-20	None	Modify Msg.	Modify Msg.	Modify Flag = 1

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Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
RMP-21	PIF, Hook 0 → 1, Cursor	Start at DCANST	Modify Msg.	1st B. P. < 1 sec, none others in 1st 10 sec.
RMP-22	None	Send Data Msg.	Exec/DCSEND Interface	Stop at call to DCSEND
RMP-23	None	Start at call to EXMES	Send Data Msg.	Stop at call to DCSEND
RMP-24	Dummy ETF, PF, Threat Total	Start at DCANUP	Send Data	Data display present
RMP-25	None	Start at call to EXMES	Master Clear Msg.	Master Clear sent
RMP-26	Master Clear 0 → 1	Start at DCPOU	Master Clear	Master Clear sent
RMP-27	None	Start at call to EXMES	System Test Start Msg.	System Test Start Msg. in STE Data Buffer
RMP-28	System Test 0 → 1	Start at DCPOU	System Test Start	Same as 27
RMP-29	None	Start at call to EXMES	System Test End Msg.	System Test End Msg. in STE Data Buffer
RMP-30	System Test 1→0	Start at DCPOU	System Test End	Same as 29
RMP-31	Dummy ETF: Lethalities Dummy PF, Threat Total Hook I. D.	Type P (priority)	Priority Override	Correctly ordered PF, PRSO = 1 ETF, PF
RMP-32	Same as 31, PRSO = 1 Lethality in EF2 Hook I. D.	Type P	Priority Return	Correctly ordered PF, PRSO = 0 in ETF, PF
RMP-33	Hook I. D., TESO = 0	Type T (tech.)	Tech. Override	Correct Tech., TESO = 1
RMP-34	Hook I. D., TESO = 1	Type T	Tech. Return	Correct Tech., TESO = 0
RMP-35	Same as 32, TESO = 1 all for several files	Type R	Return All	Correctly ordered PF, Correct Techs., all TESO = 0

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Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
RMP-36	Same as 31-35	Same as 31-35	Modify	Only Parameters updated
RMP-37	Same as 31-35	Same as 31-35	Send Data	All A/N Data Sent
RMP-38	Same as 31-35	Same as 31-35	Display Update	Immediate update after command, every 10 sec thereafter
RMP-39	None	Type M	Master Clear	Master clear sent
RMP-40	Same as test 14			
RMP-41	Same as test 16			
RMP-42	Same as test 18			
RMP-43	Same as test 28			
RMP-44	Same as test 30			
RMP-45	Same as test 31			
RMP-46	Same as test 32			
RMP-47	Same as test 33			
RMP-48	Same as test 34			
RMP-49	Same as test 35			
RMP-50	Same as test 36			
RMP-51	Same as test 37			
RMP-52	Same as test 38			
RMP-53	Same as test 39			

TABLE XIII

AP Static Test Design Requirements

Table XIV

SC STATIC TEST DESIGN REQUIREMENTS (1 of 4)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
SC-1	None	IP Msg.	CP/RMP Msg. xfer	IP Msg. in RMP data store
SC-2	None	IP Msg.	RMP/CP Msg. xfer	IP Msg. in CP data store
SC-3	None	IP Msg.	CP/AP Msg. xfer	IP Msg. in AP data store
SC-4	None	IP Msg.	AP/CP Msg. xfer	IP Msg. in CP data store
SC-5	None	IP Msg.	RMP/AP Msg. xfer	IP Msg. in AP data store
SC-6	None	IP Msg.	AP/RMP Msg. xfer	IP Msg. in RMP data store
SC-7	None	IP/SS Msg.	RMP/CP/SS Msg. xfer	IP/SS Msg. in SS buffer
SC-8	None	IP/SS Msg.	SS/CP/RMP Msg. xfer	IP/SS Msg. in RMP data store
SC-9	None	IP/SS Msg.	AP/CP/SS Msg. xfer	IP/SS Msg. in SS buffer
SC-10	None	IP/SS Msg.	SS/CP/AP Msg. xfer	IP/SS Msg. in AP data store
SC-11	None	IP/STE Msg.	CP/RMP/STE Msg. xfer	IP/STE Msg. in STE buffer
SC-12	None	IP/STE Msg.	STE/RMP/CP Msg. xfer	IP/STE Msg. in CP data store
SC-13	None	IP/STE Msg.	AP/RMP/STE Msg. xfer	IP/STE Msg. in STE buffer
SC-14	None	IP/STE Msg.	STE/RMP/AP Msg. xfer	IP/STE Msg. in AP data store

Table XIV - continued - (2 of 4)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
SC-15	None	Multiple IP Msgs.	CP/RMP multi-msg. xfer	IP Msgs. in RMP data store
SC-16	None	Multiple IP Msgs.	RMP/CP multi-msg. xfer	IP Msgs. in CP data store
SC-17	None	Multiple IP Msgs.	CP/AP multi-msg. xfer	IP Msgs. in AP data store
SC-18	None	Multiple IP Msgs.	AP/CP multi-msg. xfer	IP Msgs. in CP data store
SC-19	None	Multiple IP Msgs.	RMP/AP multi-msg. xfer	IP Msgs. in AP data store
SC-20	None	Multiple IP Msgs.	AP/RMP multi-msg. xfer	IP Msgs. in RMP data store
SC-21	None	Multiple IP/SS Msgs.	RMP/CP/SS multi-msg. xfer	IP/SS Msgs. received by dummy
SC-22	None	Multiple IP/SS Msgs.	AP/CP/SS multi-msg. xfer	IP/SS Msgs. received by dummy
SC-23	None	Multiple IP/STE Msgs.	CP/RMP/STE multi-msg. xfer	IP/STE Msgs. in STE buffer
SC-24	None	Multiple IP/STE Msgs.	AP/RMP/STE multi-msg. xfer	IP/STE Msgs in STE buffer
SC-25	EL1 & 2 entries	NE Alert Msg. matching parameters of EL2 entry with lethality = $\emptyset$ and TPAMP < ATC	NE Alert process end-to-end thru SC	Correct emitter parameters, & type from EL2, tech = blank on CRT display, no commands to ET, TG

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Table XIV - continued -

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Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
SC-26	EL1 & 2 entries	NE Alrt Msg. matching parameters of EL2 entry with lethality = Ø, TPAMP < ATC, and plat type = NAVY (MSEA)	Same ast test 25	Same as test 25 with addition of NAVY designator
SC-27	EL1 & 2 entries NE Alrt Msg. as in test 25	PTDW Msg with changed, but still matching, parameters from NE Alrt Msg.	PTDW update/tracking of emitter parameters	Same as test 25 except emitter parameters are updated
SC-28	Same as test 27	PTDW Msg with changed parameters from NE Alrt Msg. producing no match in Level 1 Search	PTDW update/drop of emitter no longer of concern	Display blanked
SC-29	EL1 & 2 entries	NE Alrt Msg matching parameters of EL2 entry with lethality ≠ Ø and TPAMP < ATC	Same as test 25	Correct emitter parameter and type, tech from EL2, commands to ET, TG with emitter parameters SPDW request msg to SS
SC-30	EL1 & 2 entries NE Alrt Msg as in test 29	PTDW Msg with changed, but still matching parameters from NE Alrt Msg.	Same as test 27	Updated emitter parameters, type, tech from EL2 on CRT display, updated commands to ET, TG
SC-31	Same as test 30	PTDW Msg with changed parameters from NE Alrt Msg producing no match in Level 1 Search	Same as test 28	Display blanked; drop commands to ET, TG; Stop SPDW Msg to SS

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Table XIV - continued - (4 of 4)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
SC-32	Same as test 30	Inactive File Alrt Msg.	Clearing inactive emitter commands & display	Same as test 31
SC-33	None	SS IB < 1/4 full SS IB >3/4 full SS Files Full SS Throttle Files full	Sys Mng 2 SS buffer msg. processing	SS buffer msg. output to STE instrumentation buffer
SC-34	EL1 entries	NE Alrt Msg with TPAMP > ATC	CP/AP processing through set-up of ABI	Anal Req Msgs., Anal Start Msg. AP Aux Bus Cntrl, Start SPDW Msg.

Table XV

DYNAMIC TEST DESIGN REQUIREMENTS (1 of 5)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
D-1	EL1 entries	PDW train, fixed parameter with no match in EL1, AMP < ATC	CP NOFA1 processing	ETF entry established Correct emitter parameters EFID = ENA1 No update msg to RMP
D-2	EL1 entries, repeat test 1 test inputs	Stop PDW train	CP deletion processing	ETF entry deleted, delete file msg. to SS
D-3	EL1 & 2 entries	PDW train, fixed param. with match in EL1, AMP < ATC	CP NOFA2 processing	Same as test 1 except EFID = ENA2
D-4	Same as test 3	PDW train, fixed param. with EOC match in EL1 & 2, AMP < ATC, leth = Ø	CP/RMP EOC processing with lethality = Ø	ETF entry established with correct emitter parameters EFID, EFDSIP correspond with EOC, update msg. to RMP, Display output for EOC
D-5	Same as test 3	PDW train, vary param. of FREQ, PRI, PW from EOC in-limits to NOFA1, AMP < ATC, lethality = Ø	CP/RMP procressing of change from EOC to NOFA1	ETF entry changes EFELN will change to Ø Display of EOC will disappear
D-6	Same as test 3	PDW train, vary param. of FREQ, PRI, PW from NOFA1 to in-limits for EOC, AMP < ATC lethality = Ø	CP/RMP processing of change from NOFA1 to EOC	ETF entry changes EFELN changes from Ø to correspond with EOC Display shows EOC

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Table XV - continued (2 of 5)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
D-7	Same as test 3	PDW train, vary param. from in-limit for EOC_1 to in-limit for EOC_2 AMP < ATC, lethality = Ø	CP/RMP processing of change from EOC_1 to EOC_2	ETF entry changes EFID, EFDISP changes from EOC_1 to EOC_2 Display follows change
D-8	Same as test 3	Same as test 4 except vary azimuth	CP/RMP angle tracking	ETF entry steady except for angle, display tracks angle
D-9	Same as test 3	Same as test 4 except EOC has leth ≠ Ø	CP/RMP resource manage	ET, TG set-up commands with emitter parameters Start SPDW Msg. to SS
D-10	Same as test 3, repeat test 9 test inputs	Stop PDW train	CP/RMP deletion process	Drop Trk Msg. to ET, delete command to TG, Stop SPDW & Delete File Msg. to SS
D-11	Same as test 3	PDW train, vary FREQ from EOC in-limits to NOFA1, AMP < ATC, lethality ≠ Ø	CP/RMP drop track processing	Same as test 10 except no Delete File Msg. to SS
D-12	Same as test 3	PDW train vary FREQ from NOFA 1 to in-limits for EOC, AMP < ATC, lethality ≠ Ø	CP/RMP pick up track	No display or ET, TG outputs, then test 9 outputs appear
D-13	Same as test 1	Same as test 1 for each PDW train	CP NOFA1 process for two emitters	Same as test 1 for each emitter
D-14	EL1 entries, repeat test 13 test inputs	Stop PDW trains	CP deletion process for two emitters	Same as test 2 for each emitter
D-15	Repeat test 4 for two emitters			

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Table XV - continued - (3 of 5)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
D-16	Repeat test 4 for three emitters			
D-17	Repeat test 4 for four emitters			
D-18	Repeat test 5 for two emitters			
D-19	Repeat test 6 for two emitters			
D-20	Repeat test 9 for two emitters			
D-21	Repeat test 9 for three emitters			
D-22	Repeat test 9 for four emitters			
D-23	Repeat test 10 for four emitters, drop one at a time			
D-24	EL1 & 2 entries; Priority, Jam Status & Resource Files full so that extra emitter exercises priority logic	PDW train, fixed parameters with EOC match in EL1 & 2, AMP < ATC, leth = high value	Res Msg priority logic	Priority File shows input emitter at proper level, resources reallocated to accommodate input emitter
D-25	Repeat test 24 for two emitters, leth 2 > leth 1 > lowest leth in priority table			
D-26	Repeat test 25 for three emitters, leth 3 > leth 2			

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Table XV - continued - (4 of 5)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
D-27	Repeat test 26 for four emitters, leth 4 >leth 3			
D-28	EL1 & 2 entries	PDW train, fixed parameters with EOC match in EL1 & 2, AMP>ATC, leth = Ø	Scan Analysis for Steady Scan	ETF entry established EFSTYP = ESTDY Display output for EOC
D-29	Same as test 28	PDW train, conscan amp variation, EOC match in EL1 & 2, peak AMP > ATC, leth = Ø	Scan Analysis for Conscan	Same as test 28 except EFSTYP = ECON
D-30	Same as test 28	Same as test 29 except sector scan amp variation	Scan Analysis for Sector scan	Same as test 28 except EFSTYP = ESECT
D-31	Same as test 28	Same as test 29 except circular scan amp variation with period >2 seconds	Scan Analysis for Circular scan	Same as test 28 except EFSTYP = ECIR after 2nd update
D-32	Repeat test 28 for two emitters			
D-33	Repeat test 29 for two emitters			
D-34	Repeat test 30 for three emitters			
D-35	Repeat tests 29 & 30 for two emitters each			

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Table XV - continued - (5 of 5)

Test No.	Pretest Inputs	Test Inputs	Function Tested	Expected Outputs
D-36	EL1 & 2 entries, dummy entries in ETF with EFSIND = 1, AMT and AAT in AP indicating full analysis capability utilized	Same as test 29	AP buffer overload and time-out process	One dummy analysis bumped, input emitt ETF entry established, EFSTYP = ECON, timed-out dummy ETF entries have EFSTYP = ECIR, bumped entry has same EFSTYP

4.0 QUALITY ASSURANCE

TBD