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Addendum to Conceptual Memory Technology Study

For the E2C A/C Data Processing System, Final Repo

GRUMMAN

Report # 75-148-20 ADDENDUM NO. 1

Addendum to Conceptual Memory Technology Study

For the E2C A/C Data Processing System, Final Report

Prepared by:

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August 1976

Prepared for:

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Naval Air Systems Command
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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Anticipated future changes will exceed the capability of the L304 data processor in the E-2C aircraft AEW (Airborne Early Warning/System). The initial study examined various memory technologies; core and semiconductor memories were recommended for further study as the means whereby memory and processing time could be increased to meet future system needs. This formed the basis of the extension study to select one technology for further development. The addendum study provides specific recommendation that a 16K x 32 bit core memory be developed for the E-2C A/C.

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Forword

This report covers work performed under Navy Contract N62269-76-C-0124 Amendment P00001 for the period May 1976 to August 1976.

The work was performed by Grumman Aerospace Corporation, Bethpage, N.Y. (GAC) under the direction of M. Lewis. The purpose of this contract was to extend the memory technology study performed under the basic contract, to permit specific recommendation of one technology approach for improvement of the E-2C A/C L304 Data Processing system.

The contributors to this report at GAC were M. Liss, L. Guido, T. Zumpano, J. Rom and D. Carter and GAC subcontractor Litton Data Systems.

The Navy program monitors were Roman Fedorak, NADC and Peter Luppino, NAVAIR.

1.0 Introduction

1.1 Summary

The recommendation resulting from the careful study of the candidate technologies for the prototype program to provide faster, double density memory modules for the E-2C L304 computer is a 16K, 32 bit magnetic core memory. Supporting this recommendation are the results of the following tasks:

- Mechanical layouts for 16K and dual 8K core memories and dual 8K CMOS and NMOS memories were prepared to have the same form factor and electrical interface as the current 8K x 32 Memory Module. The results indicated that both dual 8K and 16K core memory configurations are feasible with the 16K being most reliable. All memory candidates satisfied the functional requirements imposed e.g. cycle/access of 800/600 nanoseconds.
- Block diagrams showing the memory configuration of each of the above core and semiconductor memory technologies and the parts list for same were developed
- MTBF predictions were performed using parts failure rates for each of the above technology approaches. The results show that MTBF Reliability estimates of all memories are better than the current 8K memory; both 16K Core and NMOS can satisfy the 10K hour goal.

- Production cost predictions were estimated for the core and semiconductor memories. The cost of the dual 8K core is estimated to be about the same as the production cost of the present 8K. The MOS semiconductor memories and the 16K core estimated costs are all less than the present 8K.
- Power demands were calculated for each configuration to determine the required modifications the the current power supply. The results indicate that power requirements for all memory approaches are within system allowances. With some redesign, the power supply can be configured in the existing space for all technologies. A complete redesign is not required.
- A Tradeoff evaluation of memory technologies was performed resulting in the 16K core recommendation. Although semiconductor memories utilizing batteries were excluded for the E2C application by direction as reported during the June 3 meeting at NAVAIR, this investigation included consideration of CMOS and NMOS designs for possible future military aircraft use in accordance with contract requirements. Results for both the CMOS and NMOS memories are consistent with the previous study conclusions, NMOS battery drain is more severe and requires a secondary rechargeable battery. CMOS, however, can meet the data retentivity utilizing a lithium primary battery.

1.2 Background and Results

In previous presentations and in study report #75-148-20, the problems of saturation both time and memory, of the E-2C A/C L304 data processing capability were described. The incorporation of ARPS/MODEL 4, plus other tactical programs modification contemplated by FCDSSA are about all the present system can handle. The projected processing requirement described in E2C growth program planning addressed improvdements in many areas, e.g., radar array processing, passive ranging, communications net control and surface surveillance etc. The recommendation was made and approved by NAVAIR to implement a new 16K memory development program as the first priority item in expanding the data processing capability to support growth planning.

The initial Memory Technology study that was completed under Contract N62269-76-C-0124 examined various memory technologies available and resulted in three memory candidates suitable for application to the E-2C aircraft, i.e., Core, NMOS static and CMOS semiconductor memories. This report also noted that I^2L might be the most viable for future application in the 1980's together with bubble memory for providing a fast reload capability in the order of 1 to 2 seconds.

This extension study was undertaken, under Amendment P00001, to recommend the one current memory approach (of the three technology candidates) most suitable for the imminent memory design phase. The key constraints such as maintaining form-fit factor, minimal impact on weight, power, software, cost and an increase in reliability, with low risk as defined in the previous report apply to the approach selection.

During the course of the program visits were made to core memory manufacturer e.g. Ampex, Electronic Memories (EMM) and Data Products by Grumman and its subcontractor Litton Data System. Litton DSD was tasked with the detailed mechanical and electrical design of the memories during this extension study program. Detailed design reviews were held with Litton DSD and Navy during the course of the program wherein the power, thermal and reliability analyses were discussed and concurrence obtained with GAC analyses. The design details are contained in this report.

A summary of the characteristics of the dual 8K and 16K core, CMOS and NMOS (4K static) memories is shown in Table 1.1.1. Throughout this report the terms dual 8K and 16K shall be assumed to mean dual 8K x 32 bit and 16K x 32 bit memories unless otherwise stated. The details supporting these data are shown in section 2 and appendices. The baseline's and assumption common to all design approaches are also contained in Table 1.1-1. The detailed results were obtained as follows:

- Mechanical Design - An existing 8K x 18 bit core storage module must be repackaged by the core stack vendor (e.g., Ampex, EMM or Data Products) to achieve the proper form factor for the 8K x 32 bit memory. A production version is available for the 16K x 32 bit core memory, utilizing dual 16K x 18 bits Ampex MESA9. In all cases throughout the report "off-the-shelf" is intended to mean a 16K x 18 bit MESA9 modified to the 16K x 16 bit configuration. The packaging approach for core was changed from an enclosed housing as shown in figure 3.4.3 of the preliminary report to an open

frame housing as shown in figure 2.1-2 and 2.2-2 of this report. This concept change accounts for a gain of 0.312 inches of width in packaging space, allowing for the use of existing core mechanical configurations as exemplified by the Ampex EM & M Sems 9P1 and Ampex MESA9. The Ampex MESA9 was used in this design study since it satisfied the 800 nanosecond cycle time. As a result of the packaging approach shown in section 2, there has been and improvement in the thermal efficiency to permit operations at lower temperatures.

- Power Supply - All power demands are less than currently available from the current E2C Memory Power Supply. Modifications to the current power supply design are necessary and can be provided to satify either semiconductor or core memory requirements. The power supply packaging is essentially the same as that for the current 8K memory. As noted in Table 1.1-1, all power descriptions shown are worst case, 50% duty cycle which would apply to the base memories.
- Reliability - Based on the power requirements, temperatures defined by the thermal analysis and detailed parts list failure analysis, shown in Appendix A, the inherent reliability of the core and semiconductor memories were determined. Based on the constraints shown in the reliability section and with the current 8K memory inherent MTBF of approximately 7500 hours, used as 1.0 the relative improvement in reliability is estimated as follows:

	Improvement Ratio				
	MTBF (Hrs)		8K MTBF (Hrs)		
Dual 8K core	8,278	÷	7500	=	1.10
16K core	10,085	÷	7500	=	1.34
CMOS	7,246	÷	7500	=	0.97
NMOS	11,684	÷	7500	=	1.58

All failure rates used in the MTBF calculation were in accordance with MIL Handbook 217B with the exception of the Monolithic NMOS and hybrid CMOS microcircuits. Failure rates for these devices are based on vendor life data since there are RADC acknowledged deficiencies in the 217B Models for these devices. Further discourse on this subject is given in Section 2.7.

- Maintainability - The double density memory modules do not introduce any material changes in maintainability except that the solid state designs, which require batteries, introduce a battery monitoring and periodic replacement factor. Maintainability of the solid state designs is therefore a negative factor in the consideration of their use.
- Cost Ratio - Compared to the current 8K memory, the anticipated recurring cost ratio is approximately as follows:

	Cost Ratio
CMOS	0.7
NMOS	0.6 *
Dual 8K core	1.0
16K core	0.92

The NMOS design based on the use of the AMD AM91L40, which provides operation over the MIL temperature range, may be represented on the basis of todays cost at 0.8 of the current 8K core memory. The NMOS cost ratio shown above, *, is based on anticipated improvement in cost when using the militarized SEMI M4200 chip, which EMM forecasts to be available the end of 1976. Future cost trends for the semiconductor memories continue to show a decrease aspecially for NMOS and I^2L.

- Software - When considering the difference in software efforts between dual 8K memory and a 16K memory configuration, there are three significant areas that are evident
  a) the operational program restrictions
  b) the time loss because of simultaneous addressing
  c) the impact on programming modifications.

  In the previous report, it was noted that utilizing a 16K x 32 bit memory in lieu of dual 8K memory might result in addressing restriction, program level lockout, program change and loss of real time. In this report, an attempt was made to show that where provision is made to have memories addressable as pairs, the impact on programming restrictions and change would be reduced as compared to the previous concerns. Concerning the question of loss of real rime, a laboratory test was made to assess the loss of real time with the 16K as compared to operation with two addressable 8K memories. The preliminary test described in Appendix F indicates that there is a minor impact, i.e., only a maximum of 10 milliseconds per

is lost out of the expected 4.5 seconds real time gain resulting from the new faster memory configuration.

While there may be additional programming e.g. in the IFPM, EXEC, and display and degraded mode programs, that is necessary with the 16K configuration, it has negligible impact on the total software effort associated with the incorporation of new systems capability. In separate discussions, FCDSSA was in general agreement concerning the minor software impact of the 16K version.

Considering battery limitation, and based on evaluation of reliability, mechanical fit, software impact and cost, the 16K core memory is the technology recommended for double density, fast acting memory module development for E-2C aircraft application. The 16K memory will provide the following:

1. Utilization of a modified "off-the-shelf" memory module e.g. Ampex MESA9.
2. Satisfaction of the inherent reliability design goal of 10,000 hours MTBF.
3. Cost savings compared to the current 8K core.
4. Minimal software modification.

TABLE 1.1-1 SHEET 1 OF 2

MEMORY SYSTEMS COMPARISON CORE/C-MOS/N-MOS

SPEC DESCRIPTION	PRESENT E2C 8K MEMORY SPEC	NEW E2C 16K MEMORY SPEC	AMPEX-MESA 9 (MOD.) NEW CORE MEMORY DUAL 8K X 32	AMPEX-MESA 9 NEW CORE MEMORY 16K X 32	NEW C-MOS MEMORY DUAL 8K X 32	AM 91L40 NEW N-MOS MEMORY DUAL 8K X 32
CAPACITY	8192 WORDS X 32 BITS	16,384 WORDS X 32 BITS	DUAL 8192 WORDS X 32 BITS	16,384 WORDS X 32 BITS	DUAL 8192 WORDS X 32 BITS	DUAL 8192 WORDS X 32 BITS
STORING DEVICE	22 MIL CORE, 3D, 4 WIRE	FOR E2C = CORE MEMORY FOR OTHER APPLICATIONS NOT RESTRAINED.	13 MIL CORE, 3D, 3 WIRE	13 MIL CORE, 3D, 3 WIRE	8192 X 3 HYBRID FABRICATED USING 24 - 1024 X 1 MONOLITHIC RAM CHIPS.	4096 X 1 MONOLITHIC STATIC N-MOS RAM.
ACCESS TIME	1.1×10^{-6} SEC (INCLUDING TWO PORT LOGIC)	$.6 \times 10^{-6}$ SEC	$.575 \times 10^{-6}$ SEC	$.575 \times 10^{-6}$ SEC	$.600 \times 10^{-6}$ SEC	$.600 \times 10^{-6}$ SEC
CYCLE TIME	2.3×10^{-6} SEC	$.8 \times 10^{-6}$ SEC	$.800 \times 10^{-6}$ SEC	$.760 \times 10^{-6}$ SEC	$.800 \times 10^{-6}$ SEC	$.800 \times 10^{-6}$ SEC
INTERFACE	T^2L, 2 PORT	T^2L, 2 PORTS EACH 8K	T^2L, 2 PORTS EACH 8K	T^2L, 2 PORTS PER 16K	T^2L, 2 PORTS EACH 8K x 32	T^2L, 2 PORTS EACH 8K x 32
OPERATION MODES	READ/RESTORE, CLEAR/WRITE, READ ONLY, WRITE ONLY	SAME AS PRESENT MEMORY OR PROVISION TO CONVERT PRESENT MEMORY MODES TO R/R, C/W ONLY	READ/RESTORE, CLEAR/WRITE	READ/RESTORE, CLEAR/WRITE	READ/RESTORE, CLEAR/WRITE	READ/RESTORE, CLEAR/WRITE
POWER REQUIRED OPERATE	APPROX 100 W 25°C	100 WATTS, 25°C	93 WATTS	97 WATTS	27 WATTS	54 WATTS
STANDBY	28 WATTS		55 WATTS	80 WATTS	27 WATTS	54 WATTS
SIZE	L = 9,26" MAX, H = 9.71"MAX W = 3.14 MAX (WITHOUT FRONT PANEL)	9.26" X 9.71" X 3.14 MAX WITHOUT FRONT PANEL	9.26" X 9.71" X 3.14 MAX WITHOUT FRONT PANEL	9.26" X 9.71" X 3.15" WITHOUT FRONT PANEL	9.26" X 9.71" X 3.14" MAX WITHOUT FRONT PANEL	9.26" X 9.71" X 3.14" MAX WITHOUT FRONT PANEL
WEIGHT	15 LBS MAX	15 LBS MAX	15 LBS ESTIMATED	15 LBS ESTIMATED	12 LBS ESTIMATED	15 LBS ESTIMATED
MTBF	7500 HRS	10,000 HRS (DESIGN GOAL)	8278	10,085	7276	11,684
VOLATILITY	NON-VOLATILE	CORE = NON VOLATILE SEMI CONDUCTOR = 2 HRS MIN (DESIGN GOAL)	NON-VOLATILE	NON-VOLATILE	MULTI-YEARS USING 2 NON-RECHARGEABLE LITHIUM "AA" SIZE CELLS INTERNALLY	1.28 HRS USING 6 RECHARGE-ABLE NI-CADMIUM "C" SIZE CELLS INTERNALLY
PS VOLTAGES REQUIRED	±5V, +12V, -26A, -26B		+5V, -12V, +15V	+5V, -12V, +15V	+5 VOLTS, +6 VOLTS	+5 VOLTS
BATTERY POWER RETENTION			NA	NA	.158 MILLIWATTS AT +3V	5.2 WATTS AT 2.3V
RECURRING COST RATIO (% OF EXISTING)	100		100	92	70	80

TABLE 1.1-1 SHEET 2 OF 2

MEMORY SYSTEMS COMPARISON CORE/C-MOS/N-MOS

SPEC DESCRIPTION	SEM M4200 UMC DEVICE NEW N-MOS MEMORY DUAL 8K X 32
CAPACITY	DUAL 8192 WORDS X 32 BITS
STORING DEVICE	4096 X 1 MONOLITHIC STATIC N-MOS RAM (SEMI M4200 UMC)
ACCESS TIME	$.600 \times 10^{-6}$ SEC
CYCLE TIME	$.800 \times 10^{-6}$ SEC
INTERFACE	T^2L, 2 PORTS EACH 8K X 32
OPERATION MODES	READ/RESTORE, CLEAR/WRITE
POWER REQUIRED	OPERATING = 48 WATTS (50% DUTY CYCLE) STANDBY = 37W
SIZE	9.26" X 9.71 X 3.14"
WEIGHT	15 LBS MAX
MTBF	12024
VOLATILITY	3.4 HRS USING 6 RECHARGEABLE Ni-CAD "C" SIZE CELLS INTERNALLY
PS VOLTAGES REQUIRED	$\pm$5, +12V *
BATTERY POWER RETENTION	.92W at -4.8V 1.64W at +4.8V
RECURRING COST RATIO (% OF EXISTING)	60 **

*+5V VERSION AVAIL 1977

**Based on anticipated cost estimated for EMM SEMI M4200 to be available by end of 1976.

BASELINE ASSUMPTIONS

A set of baseline and assumptions were made that are common to all approaches. They are

1. Loading of the processor-memory bus by the new memories shall be equivalent to the present design to the extent possible.
2. Noise immunity of the processor-memory bus receivers of the new memories shall be equivalent to the present design to the extent possible.
3. Low power Schottky devices will be used if memory cycle time, memory read-restore access time on items 1 and 2 above are not adversely impacted.
4. A 40 ns period crystal clock oscillator is assumed for generating timing for all approaches.
5. All power numbers shown are worst case. For the core storage modules vendor furnished worst case numbers are used. For all othermodules 120% of calculated typical power was used. Operate power is based on 50% duty cycle, 1/2 one's and 1/2 zero's.
6. When the computer system is expanded to 128 K w rds (16 banks of 8K) there will be 6 new design 16K units located in the lower section of the computer cabinet and 4 present design 8K units located in the middle section of the computer cabinet.
7. For purposes of calculating the computer cabinet power dissipation (for thermal analysis and the reliability analysis) the same memory operation mix was used as had been previously used for the the thermal analysis using the present 8K memory. The only difference from the previous analysis will be that when using the new 16K memories the total memory capacity is assumed to expand from 64K to 128K words.

2.0 Technical Description

In general a common set of requirements was imposed on all four memory approaches selected as candidates to satisfy the E-2C requirement for memory expansion and system throughput improvement. These requirements are as follows:

- Provide a momory unit that has a 16K x 32-bit storage capacity, 800 nanosecond cycle time, 600 nanosecond access time and is form-fit and function pin for pin compatible with the present E2 8K memory
- Provide a power supply that furnishes power to two memory units that utilizes existing prime power and is form-fit and function compatible with the present E-2C memory power supply
- Utilize existing methods for module insertion, interconnection and cooling. Provide a dual set of bank assignment switches so that the 16K of new memory is addressable without restriction as two independent 8K x 32-bit memory banks.

The technical information that follows provide the mechanical and electrical design details, power, thermal, reliability analysis for each of the core and semiconductor technologies.

The mechanical design of the memory units is basically the same for all of the approaches. The units consist of a front panel, a rear panel, top and bottom guides and a wire-wrapped backplane. Layout drawings are included for each memory approach in the detailed discussions. A good deal of commonality exists in the electrical designs for the four approaches in that the requirements at the processor-memory bus interface are identical. Differences in

the four system designs are due to differences in requirements of the four storage modules. In addition, for the 16K core, a full dual two-port interface is not required since any one access to a 16K core storage module will require that the memory appear busy for both 8K banks.

Additional technical information e.g., parts lists, analyses, plus test data are contained in the appendices to this report.

2.1 Dual 8K x 32 Bit Core Memory

The dual 8K by 32 bit core memory design doubles the storage capacity of the memory by packaging two 8K modules into a single WRA. This design maintains present availability to the two processors; that is, one processor can access one 8K module while the second processor can access the other 8K module without a timing interference.

2.1.1 Electrical Design

The proposed design, shown in the block diagram of Figure 2.1-1, consists of two 8K core storage assemblies and two logic card assemblies packaged in the present 8K memory volume. The core storage assembly is a modification of a current design and is available from a number of sources. The logic card assemblies interface the core assemblies with the processors.

2.1.1.1 Core Storage Assembly, 8K by 32 Bit

The core storage assembly is available from three sources, Ampex, EM & M, and Data products. The Ampex version was utilized for the purpose of this design study.

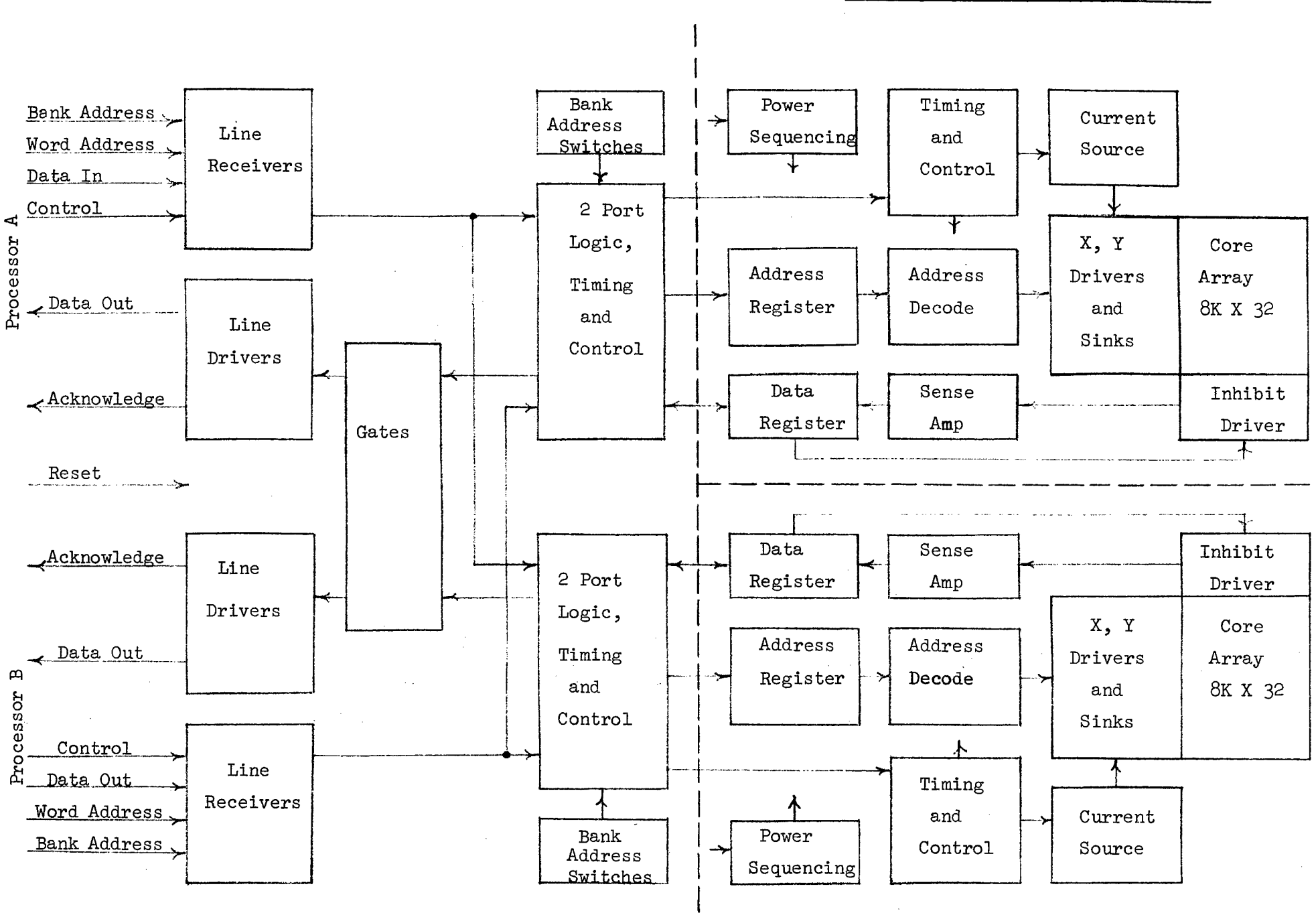


FIGURE 2.1-1 DUAL 8K BY 32 BIT CORE MEMORY

The proposed Ampex core module, shown in Figure 2.1-1, is a modification of the present MESA-9 airborne core memory unit. The MESA-9 exists as a 16,384 word by 18 bit module and will be reconfigured to an 8,192 word by 32 bit module. The data registers and the input/output circuits will be increased to accommodate the change from an 18 to a 32 bit data word, but fewer address circuits are required. The assembly operates in two modes, clear-write and read-restore; the memory will, however, satisfy the four modes of processor operation. Data access is 575 nanoseconds and the full cycle operation is 800 nanoseconds.

The core storage module is organized as a 3D, 3 wire memory consisting of two functional assemblies, a storage assembly and an electronics assembly. The storage assembly contains the core arrays and all stack associated circuits. The Ampex 13 mil-temperature independent (TIN) cores are used in the stack. The electronic assembly contains the input-output interface, timing, control, address register, current sources, inhibit current control and power sequencing functions. The input and output signals are compatible with TTL circuits, series 5400.

2.1.1.2 Logic Card Assembly, Dual 8K by 32 Bit Core Memory

The logic card assembly consists of a double multilayer board assembly that contains the interface, two port logic, timing, control and bank address functions that allow the operation from both processors to either of the two 8K storage assemblies. These functions are shown in Figure 2.1-1.

During operation, the bank address lines "set-up" a request for memory service for the processor and also select the 8K storage assembly to be accessed according to the setting of the bank address switches. For the clear-write mode, data is gated from the selected memory bus and stored in a data register as it is loaded into the core storage module. For the read-restore mode, data from the core storage module is gated to the memory bus of the requesting processor. The mode control logic converts the four processor modes read-only, write-only, clear-write and read-restore to two modes of clear-write and read-restore.

The active circuits contained on the logic card assembly include a 25 MHz oscillator as a basic source for the timing circuits, high speed TTL (54H series), Schottky TTL (54S series) and the Schottky low power TTL (54LS series) devices. In addition, the bank address switches and capacitors are mounted on the assembly. A parts list is contained in the Appendix A of this report.

2.1.1.3 Power Requirements, Dual 8K by 32 Bit Core Memory

The TTL microcircuits on the logic card assembly operate from a single +5 volt power supply. The core storage assemblies operate from voltages of -12, +15, and +5 volts.

The 16K memory WRA's are operated in pairs from a common power supply. The current drains vary with the duty cycle and the data format. Since the two port logic allows access by two processors, a maximum of two of the four 8K core storage assemblies can be operating at the same time while the other two are in a standby condition. Table 2.1-1 lists the current requirements for the

two conditions: two 8K core assemblies operating at an 800 nanosecond cycle time, all zero pattern with the remaining two assemblies in standby and all four assemblies in standby.

Table 2.1-1

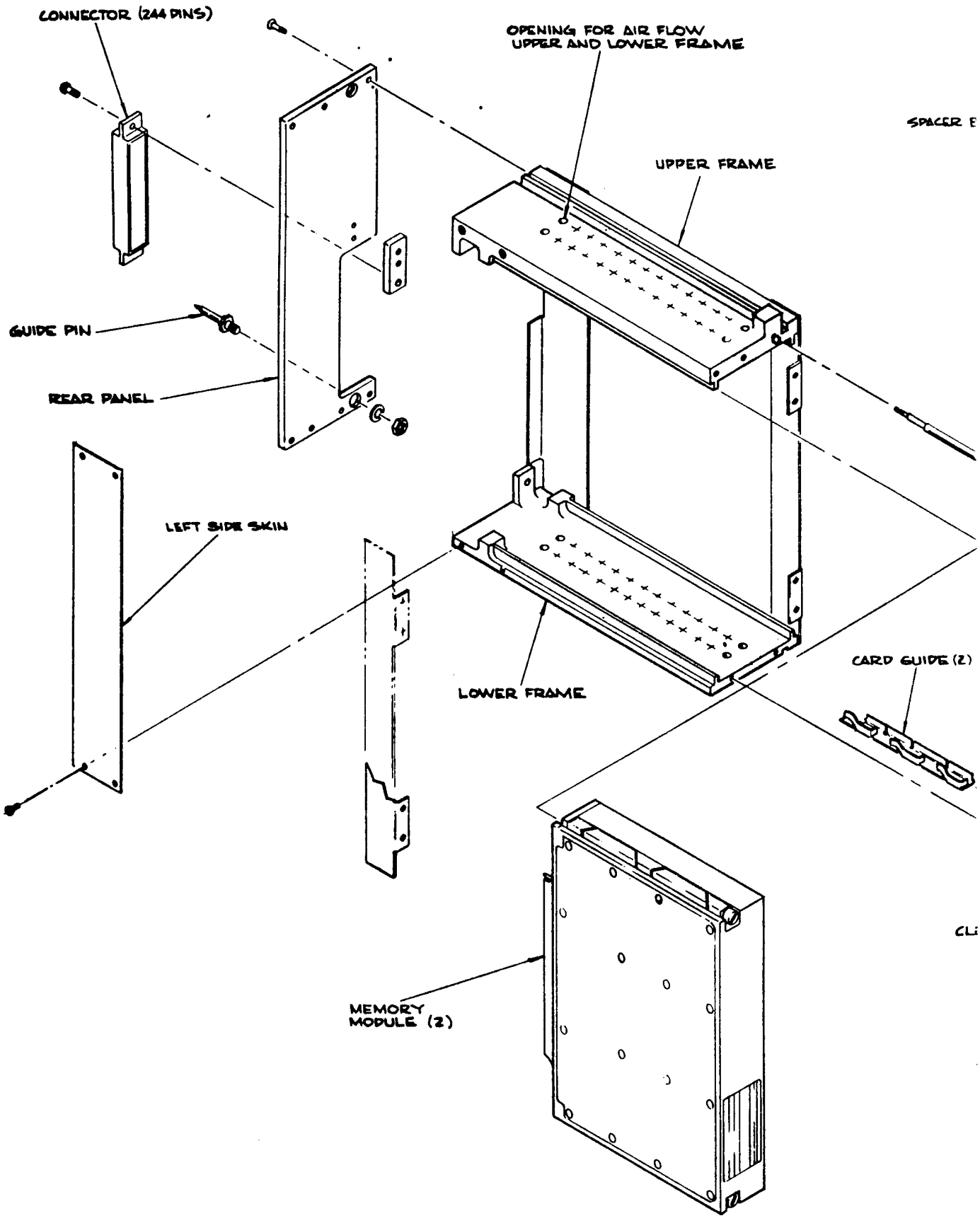
Power Requirements for the Dual 8K by 32 Bit Core Memory

Voltage	Current Drain (4 Assemblies in Standby)	Current Drain (2 Assemblies in Standby)
+5 Volts	15.8 Amps.	16.8 Amps
+15	0.8	2.2
-12	1.6	17.0

2.1.2 Core Packaging Dual 8K

An exploded view of the dual 8K core assembly is shown in Figure 2.1-2. The housing consists of an upper and a lower frame with openings to allow for air passage through the memory assembly and over the circuit cards. The draw bolt is permanently secured to the upper frame. The two sides consist of modified Ampex MESA 9 core memory plug-in modules. The remainder of the housing consists of a rear panel, two rear side plates and a removable front panel for logic card and core module access. The connector plate for the cricuit cards and the external interface connector are wired as a separate subassembly prior to installation into the main frame.

The logic module consists of two logic multi-layer circuit cards mounted back-to-back on a common frame. Each card consists of 84 flat-pack integrated circuits, a connector, and associated



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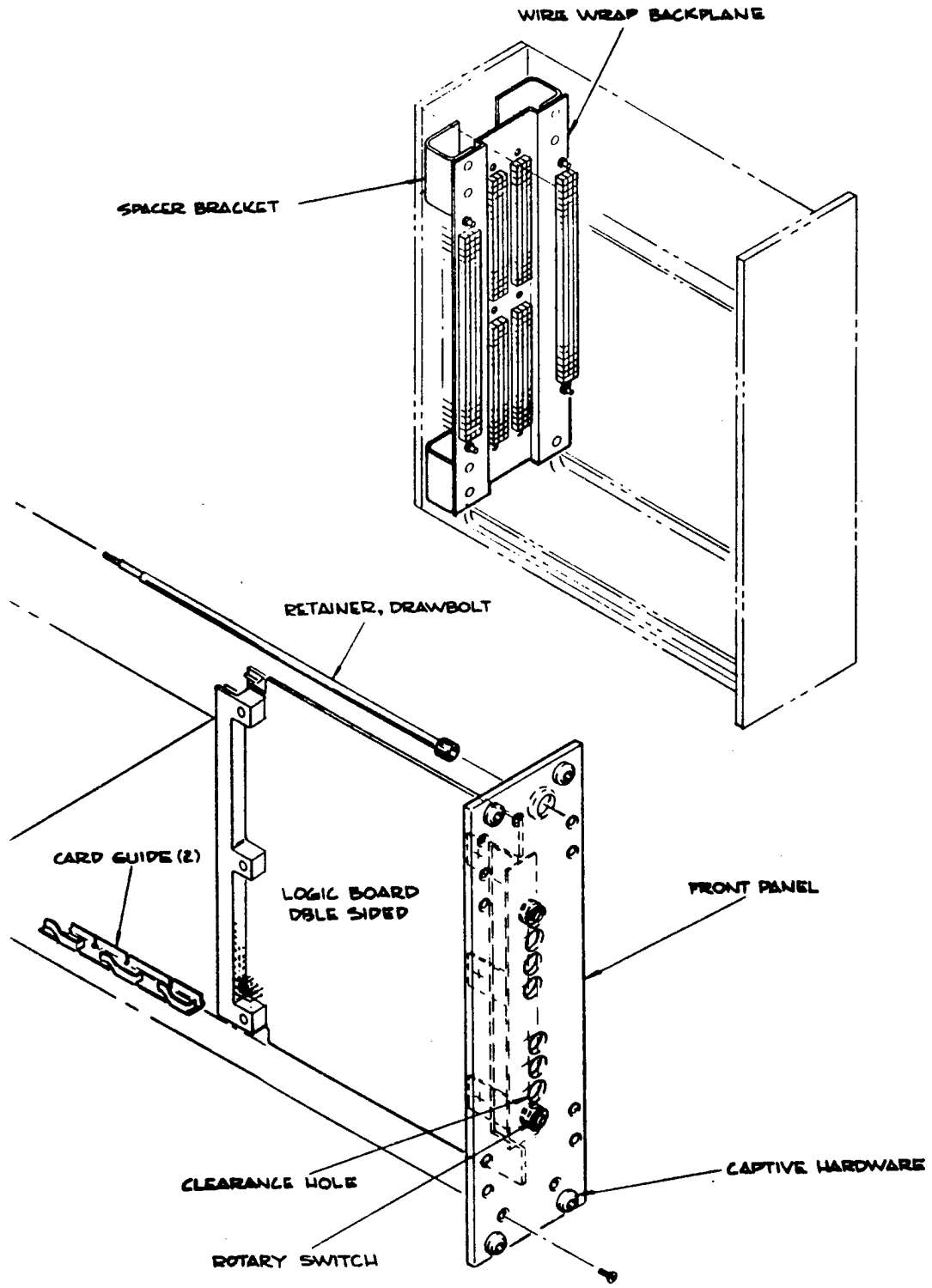

EXPLODED VIEW

DUAL 8KX32 CORE M

FIG. 2.1-2

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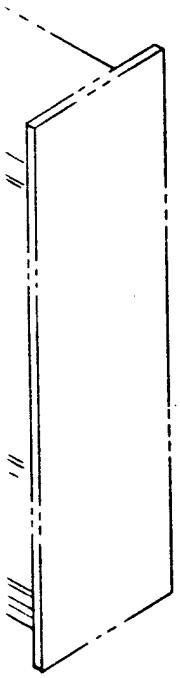


ONT PANEL

- CAPTIVE HARDWARE

EXPLODED VIEW

DUAL 8KX32 CORE MEMORY

FIG. 2.1-2

discrete components. Mounted to this plug-in module are the eight bank address switches. Access to these switches is through openings in the front panel.

The weight of the entire assembly is estimated to be 15 pounds. Power dissipation is 93 watts when operated at 1/2 one's, 1/2 zero's, a 50% duty cycle, and when one memory module serves as the base memory.

2.1.3 Thermal Analysis

MTBF calculations are based on mounting rail temperatures of the memory modules. Therefore, the temperatures defined as surface temperatures for the memory module in the thermal analysis shown in Appendix D are considered the same as rail temperatures for the memory modules. Logic card surface temperatures are surface temperatures. Rail temperature of the memory card is 59°C and the surface temperature of the logic card is 27°C, as shown in the thermal summary in Appendix D, rounded-off to the nearest degree.

2.2 16K by 32 Bit Core Module

The 16K by 32 bit core memory, like the dual 8K version, doubles the storage capacity of the memory WRA. However, the availability of the contents to each processor is reduced since access to the memory by one processor prevents the second processor from gaining access to the full 16K words, until the first processor is through.

The 16K memory design can be accomplished in a number of configurations. One approach considered using a pair of 16K by 18 bit core modules, with each module providing half the required 32 bits for the data word. The Ampex MESA-9, the EM & M SEMS 9PI and

SEMS-13P, with modifications, fits this design. Another approach considered a single core module containing the full 16K by 32 bit storage capacity. The EM & M SEMS-14, with modifications, satisfies this design. At present, the SEMS-13P and SEMS-14 modules are not fully developed and the SEMS-9PI is not adequate in cycle time. While the MESA-9 was selected as the core module for this design evaluation, SEMS-13P and 14 may be considered as alternate/second source.

2.2.1 Electrical Design

The proposed design is shown in the block diagram of Figure 2.2-1. It consists of two core memory assemblies, 16K by 16 bits, and one logic card assembly packaged in the present 8K memory volume.

2.2.1.1 Core Memory, 16K by 16 Bit

The core assembly described is the Ampex MESA-9, modified to a 16K by 16 bit configuration. The MESA-9, a 16K by 18 bit memory, is a unit that is presently in production.

The proposed core memory assembly is organized as a 3D core assembly utilizing 13-mil-cores. The assembly operates in two modes, clear-write and read-restore. Data access is 575 nanoseconds and full cycle time is 760 nanoseconds.

The core memory assembly, shown in Figure 2.2-1, is similar to the one described in paragraph 2.1.1.1. The major differences are the data loops and input/output circuits to accommodate the 16 bit data word instead of the 32 bit data word.

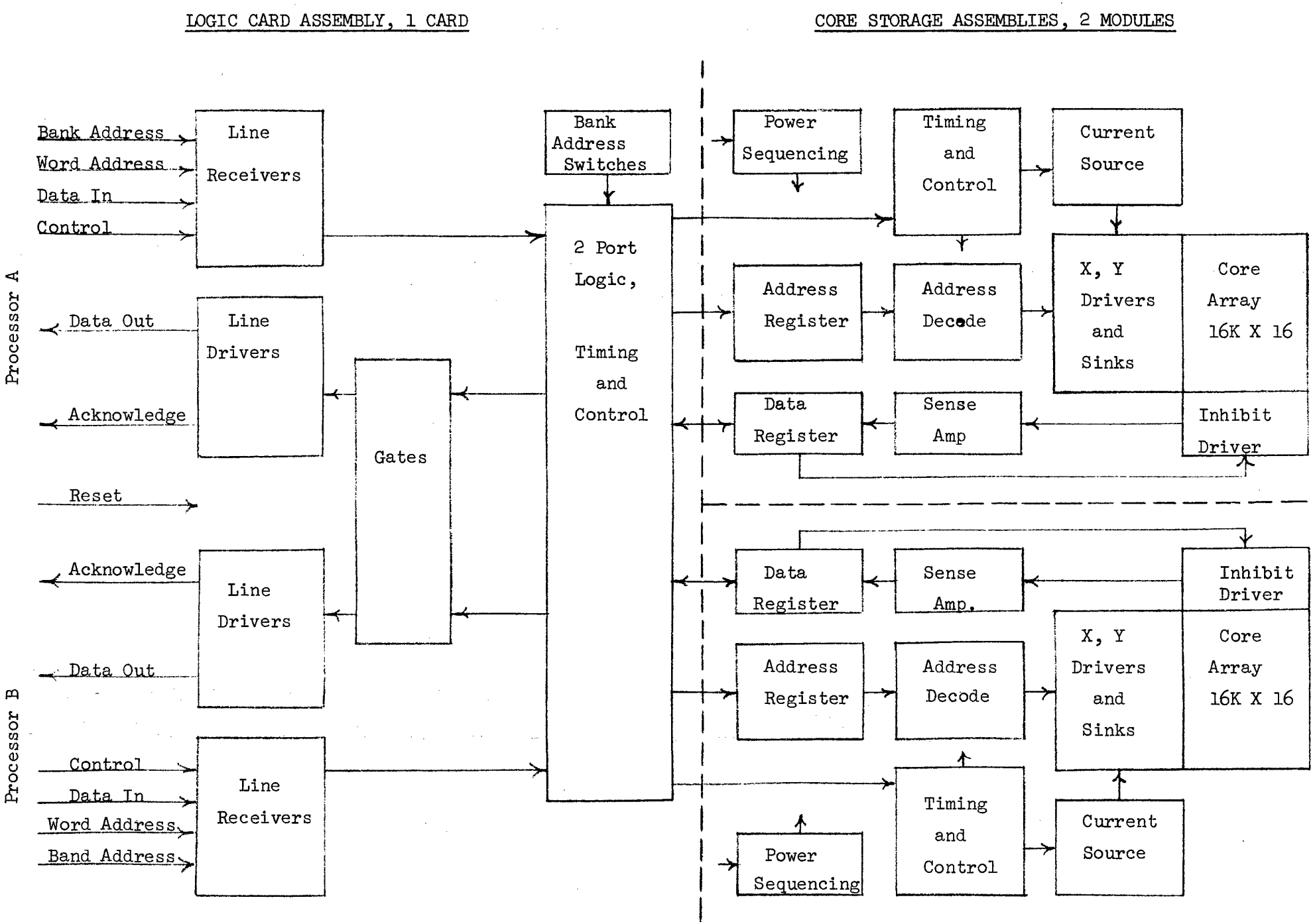


FIGURE 2.2-1 16K BY 32 BIT CORE MEMORY

2.2.1.2 Logic Card Assembly, 16K by 32 Bit Core Memory

The functions contained on the logic card assembly are shown in the block diagram of Figure 2.2-1. The single card contains the interface, two port logic, timing, control and bank address functions that allow operation of the two core memory assemblies with two processors.

When the memory is accessed by a processor for service, the two port logic prevents the second processor from access until the first processor has completed its function. During operation, the logic card combines 16 bits from each core assembly to construct the complete 32 bit word.

The bank address logic allows the 16K core memory to appear as two separate addressable 8K modules to the requesting processor.

The mode control logic converts the four processor modes of read-only, write-only, clear-write, and read-restore to two core memory modes of clear-write and read-restore functions.

The circuits contained on the logic card assembly include a 25 MHz oscillator, high speed TTL (54H series), Schottky TTL (54S series) and Schottky low power TTL (54S series) active devices. Bank address switches and capacitors are also contained on this card assembly. A parts list is contained in Appendix A to this report.

2.2.1.3 Power Requirements, 16K by 32 Bit Core Memory

The logic card circuits operate from a single +5 volt power supply. There are a total of 125 active components, including the oscillator on the card. The two core assemblies require voltages of +15, +5 and -12 volts.

In the computer, the 16K memory WRA's will be installed in pairs and operate from a common power supply. For the dual processor configuration, then, both memory WRA's can operate simultaneously. The current drains vary with the duty cycle and the data pattern. The current drains for the 16K memories are shown in Table 2.2-1 for the standby and operate conditions. In the standby condition there is no access by either processor. Operation is shown for both memories operating at a 760 nanosecond cycle time with an all zero data pattern, which requires maximum current for a 3D organization.

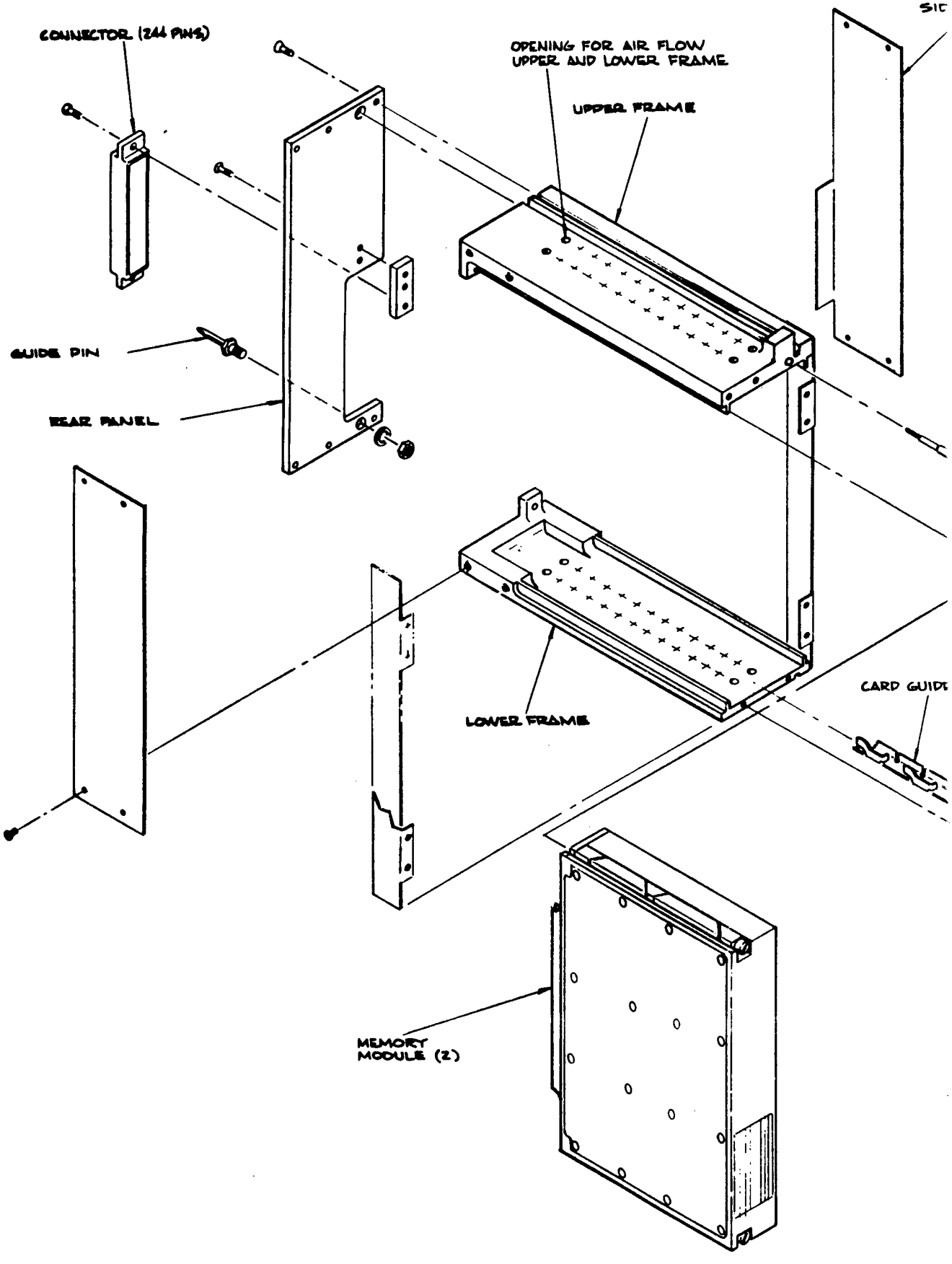
Table 2.2-1

Power Requirements for the 16K by 32 Bit Core Memory

Voltage	Current Drain (2 memories in Standby)	Current Drain (2 Memories operating at 750 nsec cycle time, all zero)
+ 5 Volts	11.8 Amps	15.4 Amps
+15	0.8	4.0
-12	1.0	23.2

2.2.2 Core Packaging 16K

An exploded view of the 16K core assembly is shown in Figure 2.2-2. The housing consists of an upper and a lower frame with openings to allow for air passage through the memory assembly and over the circuit cards. The draw bolt is permanently secured to the upper frame. The two sides are made up of modified MESA-9 core memory plug-in modules. The remainder of the housing consists of a rear panel, two rear side plates and a removable front panel



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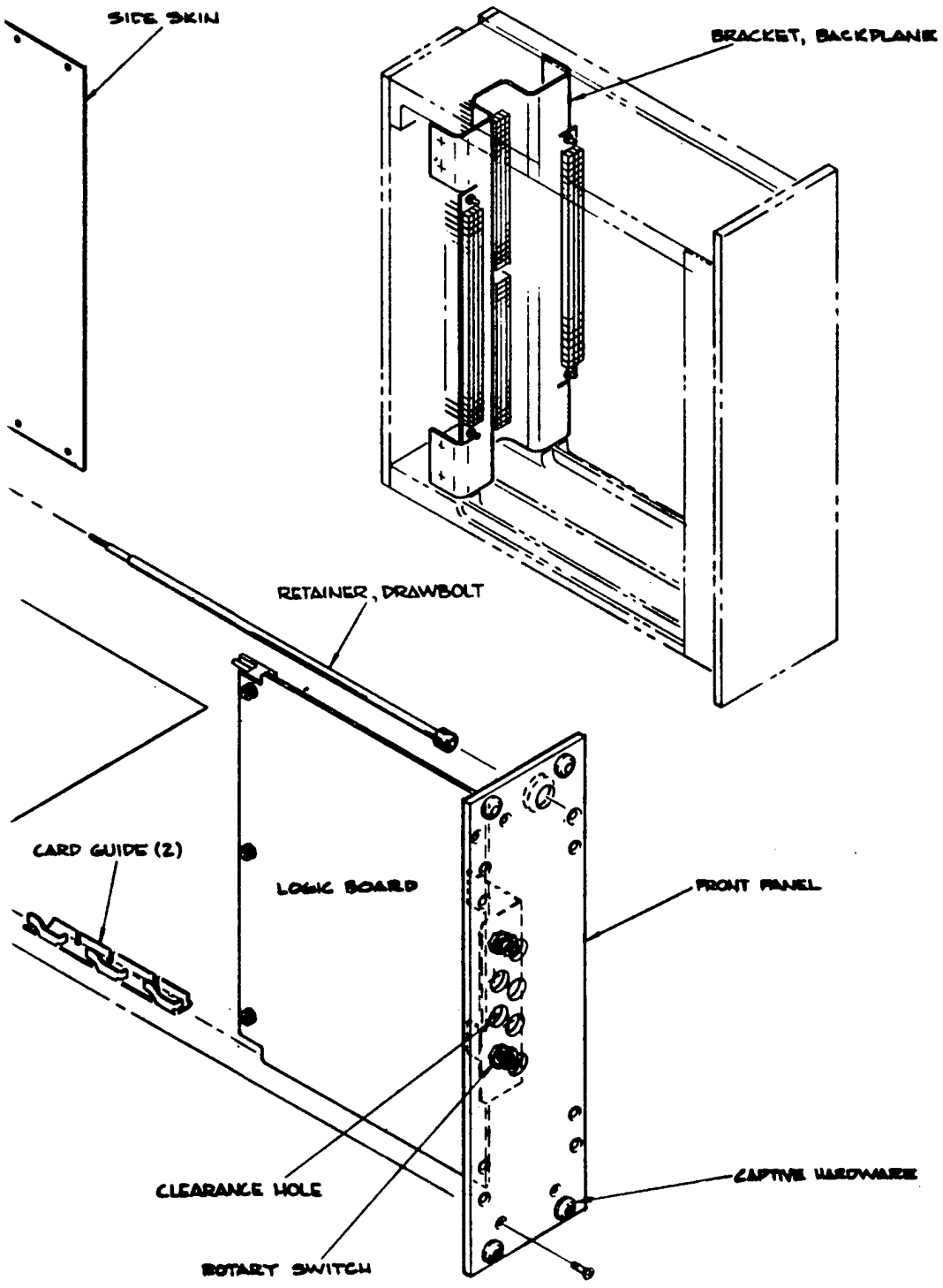

EXPLODED VIEW

16X32 CORE MEMOI

FIG. 2.2-2

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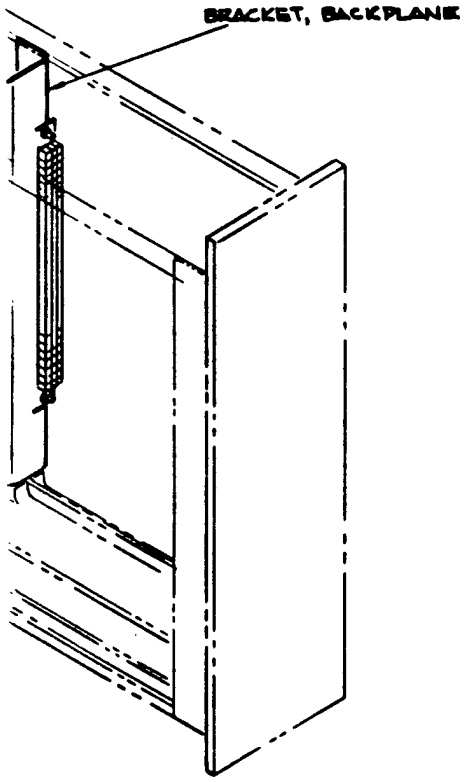
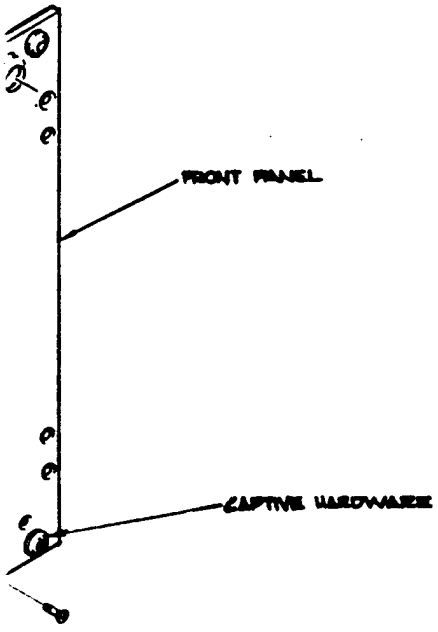




EXPLODED VIEW

16X32 CORE MEMORY

FIG. 2.2-2

for circuit card and core module access. The connector plate for the circuit cards and the external interface connector are wired as a separate subassembly prior to installation into the main frame.

The logic module consists of one logic multi-layer circuit card. The card consists of 124 flat pack integrated circuits, a connector, and associated discrete components. Mounted to the plug-in module are the eight bank address switches which are accessible through openings in the front panel.

The weight of the entire assembly is estimated to be 15 pounds. Power dissipation is 97 watts when operated at 1/2 one's, 1/2 zero's, and a 50% duty cycle.

2.2.3 Thermal Analysis

The thermal analysis for the 16K x 32 bit memory configuration is similar to that for the Dual 8K x 32 bit memory. Rail temperature for the memory modules is 52°C and the surface temperature for the logic card is 24°C as shown in the thermal summary in Appendix D, rounded-off to the nearest degree.

2.3 NMOS Memory System (Dual 8K x 32)

2.3.1 Electrical Design

2.3.1.1 General

Utilizing the updated memory requirements of the E-2C L304F Computer as a model, a study was performed regarding the feasibility of using NMOS Static Semi-Conductor RAM devices in a memory system. Table 1.1-1 contains the pertinent characteristic data for a Semi-Conductor Ram Memory utilizing Static NMOS (4096 x 1) devices. Table 1.1-1 also compares the NMOS Memory specification to the new L304F Computer Memory Specification.

2.3.1.2 Functional Description

A functional block diagram of a Dual 8K x 32 Memory System is contained in Figure 2.3-1. The Memory/Central Processor interface signals are noted on the left side of the diagram. The Port A input/output signals refer to those signals transmitted to or from the L304F "A" Central Processor. Similarly, the Port B input/output signals refer to those signals transmitted to or from the L304F "B" Central Processor. Regarding the signals interfacing the Memory WRA and the A & B Central Processors, the functional system operation is the same as currently exists in the E-2C L304F Computer.

The Dual 8K x 32 configuration will permit a central processor to access one 8K x 32 section while a second processor accesses the other 8K x 32 section i.e. both sections can be accessed simultaneously.

Each 8K x 32 memory section will have its own 2 port logic and timing circuitry. The 2 port logic interfaces the NMOS 8K x 32 memory section to either of two central processors and services them on a first come first served basis. The timing circuit "sets-up" the proper timing relationship of the NMOS RAM device interface signals i.e. address, input/output data, chip enable, chip select, and read/write enable. It also controls the output transmission of data to either of the two central processors.

A simplified block diagram of a single 8K x 32 Memory Card is shown in Figure 2.3-2.

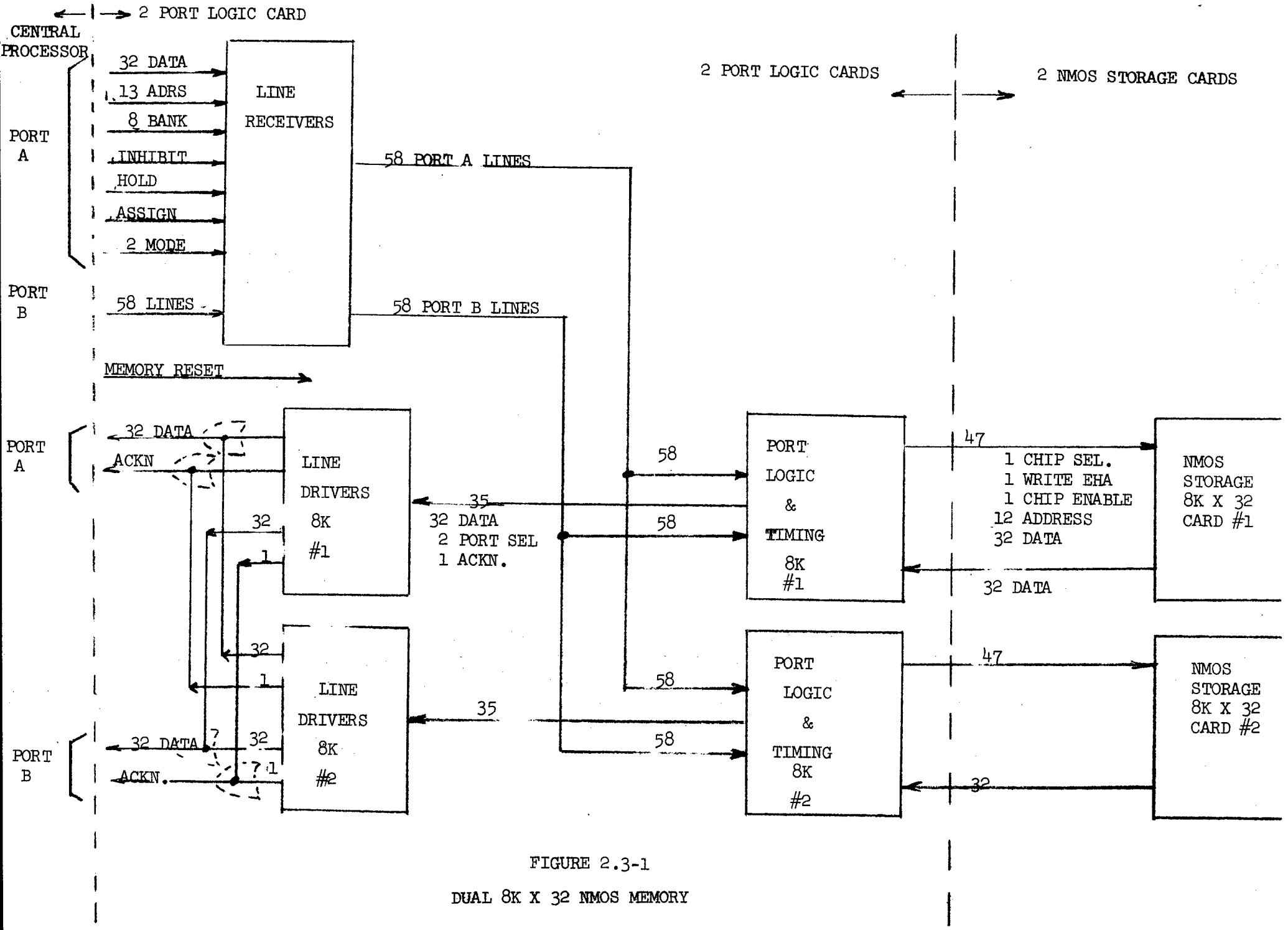


FIGURE 2.3-1

DUAL 8K X 32 NMOS MEMORY

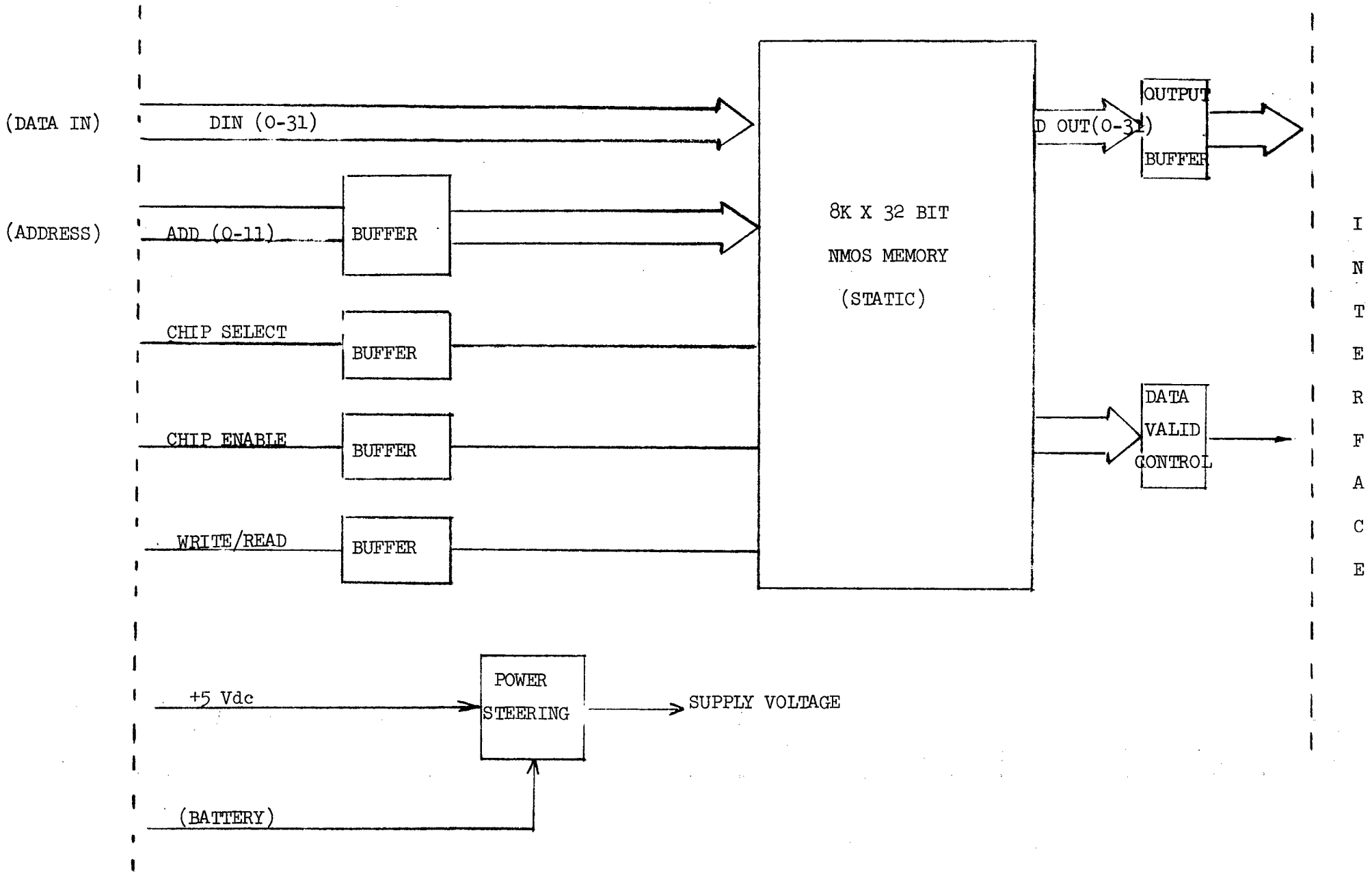


FIGURE 2.3-2

BLOCK DIAGRAM (8K X 32 BIT STATIC NMOS MEMORY CARD)

In the event of a +5V power "turn-off" the power steering circuitry shown in Figure 2.3-3 provides an automatic Control which enables the application of a battery voltage to the IC Memory Devices. This enables the semiconductor memory to become non-volatile for a prescribed period of time.

2.3.1.3 System Characteristics

The memory capacity is a Dual 8192 word x 32 Bit memory. This provides an effective total memory capacity of 16K x 32. The Dual 8K Configuration permits one central processor to access an 8k x 32 section while the second central processor accesses the other section 8K x 32 section i.e. both sections can be accessed simultaneously. The access and cycle times for each 8K x 32 section of the Dual 8K x 32 section of the Dual 8K x 32 memory system are 600 nanoseconds and 800 nanoseconds respectively.

The memory devices either the SEMI M4200 UMC or the AM91L40 Monolithic IC. These are 4096 word x 1 bit static NMOS RAMS. The 91L40 requires only +5V. The SEMI M4200 UMC requires $\pm$ 5V, and +12 Volts. The devices are specified to operate over the full Military temperature range of $-55^{\circ}C$ to $+125^{\circ}C$. The package type is a 22 pin hermetically sealed Dual-In-Line package (DIP). Table 2.3-2 provided additional details and updates Table 3.2.5 of the previous report with the latest information available to date. Further detail discussions concerning these devices are provided in Appendix B. The memory WRA interface with the outside world is T^2L compatible. Each 8K x 32 memory bank contains Dual Port logic which will service either of the two central processors on a first come first served basis. The operating modes of the memory will effectively be a

Read/Restore or Clear/Write. The present L304F operation modes are Read/Restore, Clear/Write, Read-Only and Write-Only. The Read-Only and the Write-Only operations will be interpreted by the semiconductor memory as Read/Restore and Clear/Write respectively.

2.3.1.3.1 Power Required

Table 2.3-3 contains a summary of the power requirements for the Dual 8K x 32 NMOS memory using either of the AMD 91L40 BDM, EMM SEMI 4801 (MIL VERSION), and EMM SEMI M4200 UMC RAM memory devices. The calculations for Table 2.3-3 are contained in Appendix B. It should be noted that using the SEMI M4200 UMS device in the Dual 8K x 32 memory results in a WRA dissipation of 48 watts (operating at 50% Duty Cycle) and a WRA stand-by power dissipation of 37 watts. Thus, using the SEMI M4200 UMC in the Dual 8K x 32 memory WRA results in the lower power dissipation and lower temperature; which will improve reliability as shown in Table 1.1.1 compared to the AMD device.

2.3.1.3.2 Volatility

As a design goal, the NMOS volatility requirement of 2 hrs minimum. That is, was considered applicable to the E-2C A/C. The data contained within the NMOS Dual 8K x 32 semiconductor memory should remain for a period of 2 hrs following the removal of the normal operating supply voltage. When the supply voltage (or voltages) are removed the secondary rechargeable Ni-Cad Batteries (6 cells) supplies the required DC voltage and provides for data retention. Table 2.3-3 contains the data retention time (time to discharge the battery) for the NMOS Dual 8K x 32 memory.

Figure 2.3-3 contains a simplified schematic of a secondary battery charging circuit and automatic memory chip voltage control circuitry. Diode D1 prevents the battery voltage from feeding back into the timing control & selection circuitry when primary power is removed. R_1 limits the maximum initial charging current into the battery. Diodes D1 and D2 perform a logic "or" function so that when primary power is available it is transmitted to the memory chips via D2. D3 is reversed biased and automatically removes the battery from supplying current to the memory chips. In the event of primary power removal D2 opens because it is reversed-biased by battery current through Diode D3.

2.3.2 Packaging NMOS

An exploded view of the NMOS memory assembly is shown in Figure 2.3-4. The housing consists of an upper and a lower frame with openings to allow for air passage through the memory assembly and over the circuit cards. The draw bolt is permanently secured to the upper frame. The two side plates are finned heat sinks to which the memory and drive circuit multi-layer cards are attached. Both of these subassemblies plug into the backplane connector plate. A rear panel, a removable front panel for circuit card access, and a removable plate in the rear for battery access comprise the remainder of the housing. The backplane connector plate for the circuit cards and the external interface connector are wired as a separate subassembly prior to main frame installation.

FIGURE 2.3-3

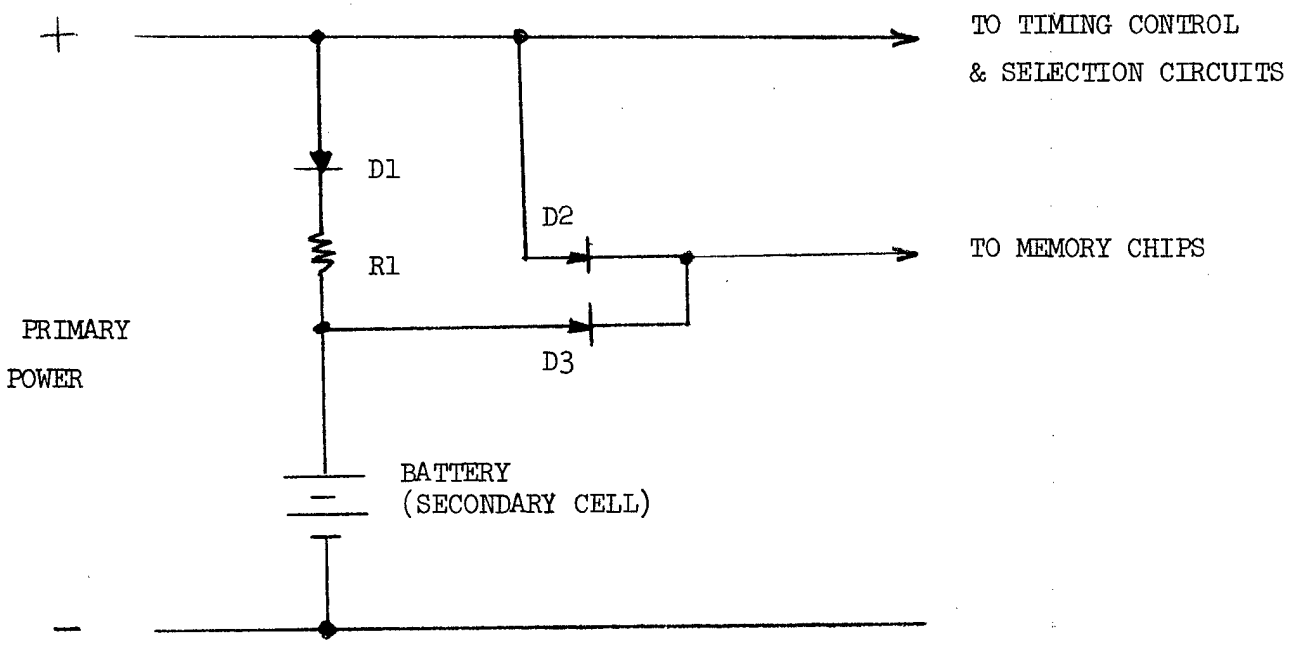

+
TO TIMING CONTROL
& SELECTION CIRCUITS
D1
D2
R1
TO MEMORY CHIPS
PRIMARY
POWER
D3
BATTERY
(SECONDARY CELL)
–

TABLE 2.3-2 (Sheet 1 of 3)

4 K STATIC N-CHANNEL RAM

TYPE	MANUFACTURER	DEVICE NO.'	DENSITY	ACCESS TIME	CYCLE TIME	TEMP RANGE	SUPPLY VOLTAGE	POWER DISSIPATION	PRICE PER CHIP	PRICE PER CHIP BURN-IN	AVAILABILITY
N-channel MOS static Ram	Advanced Micro devices (AMD)	AM9140 -BDM	4096 x 1	400 NS (MAX)	690 NS (MIN)	- 55°C + 125°C	+ 5V	350 MW (Typical)	SEE NOTE 1	SEE NOTE 1	SEE NOTE 1
N-channel MOS static RAM	Advanced Micro devices (AMD)	AM9140 - CDM	4096 x 1	300 NS (MAX)	530 NS (MIN)	- 55°C + 125°C	+ 5V	350 MW	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2
N-channel MOS static RAM	Advanced Micro Devices (AMD)	AM91L40 - BDM	4096 x 1	400 NS	690 NS	- 55°C + 125°C	+ 5V	195 MW	SEE NOTE 3	SEE NOTE 3	SEE NOTE 3
N-channel MOS static RAM	Advanced Micro Devices (AMD)	AM91L40 - CDM	4096 x 1	300 NS	530 NS	- 55°C + 125°C	+ 5V	195 MW	SEE NOTE 4	SEE NOTE 4	SEE NOTE 4
N-channel MOS static RAM	EMM	SEMI M4200 UMC	4096 x 1	250 NS	400 NS	- 55°C + 125°C	± 5V, + 12V	450 MW operating (typical) 110 MW (standby)	SEE NOTE 5	SEE NOTE 5	SEE NOTE 5
N-channel MOS static RAM	EMM	SEMI 4801 (SEE NOTE 7)	4096 x 1	500 NS	500 NS	- 55°C + 125°C	+ 5V	375 MW (Typical)	---	$30-$40 per device Qty= 10K - 25K (estimated)	Not Available until First Qtr 1977

NOTES

1.

QTY	AM9140 BDM PRICE/DEVICE (DOLLARS)	PRICE/DEVICE BURN IN	AVAILABILITY WEEK ARO	AVAILABILITY WEEKS ARO BURN-IN
1000-4999	47.50	50	3	6
5000-9999	42.50	45	5	8
10K-24999	37.50	40	7	10
25K-49999	34.40	36.90	9	12
50K-100K	31.25	33.75	11	14

The manufacturer expects to reduce above prices 5-10% by 11/76.

2.

QTY	AM9140 CDM PRICE/DEVICE (DOLLARS)	PRICE/DEVICE BURN IN	AVAILABILITY WEEK ARO	AVAILABILITY WEEKS ARO BURN-IN
1000-4999	51.75	54.25	3	6
5000-9999	46	48.50	5	8
10K-24999	40.25	42.75	7	10
25K-49999	37.40	39.90	9	12
50K-100K	33.60	36.10	11	14

The manufacturer expects to reduce above prices 5-10% by 11/76.

TABLE 2.3-2 (Sheet 2 of 3)

NOTES (CONTINUED)

3. AM 91L40 BDM

QTY	PRICE/DEVICE (DOLLARS)	PRICE/DEVICE BURN-IN	AVAILABILITY WEEKS ARO	AVAILABILITY WEEK ARO BURN-IN
1000-4999	54.65	57.15	8	12
5000-9999	48.90	51.40	12	16
10K-24999	43.10	45.60	16	20
25K-49999	39.55	42.05	20	24
50K-100K	35.95	38.45	24	28

The manufacturer expects to reduce above prices 5-10% by 11/76.

4. AM 91L40 CDM

1000-4999	59.50	62	8	12
5000-9999	52.90	55.40	12	16
10K-24999	46.30	48.80	16	20
25K-49999	43	45.50	20	24
50K-100K	38.65	41.15	24	28

The manufacturer expects to reduce the above prices by 5-10% by 11/76.

5. EMM SEMI M4.200 UMC

1000-4999	45.75	48.00	6	10
5000-9999	39.00	41.00	12	16
10K-24999	36.20	38.00	16	22
25K-49999	32.85	34.50	20	28
50K-100K	30.50	32.00	24	34

6. EMM SEMI 4801

1000-4999	---	---	---	---
5000-9999	---	---	---	---
10K-24999	---	$30-$40 estimated	---	NOT AVAILABLE UNTIL FIRST QTR 1977.
25K-49999	---	---	---	---
50K-100K	---	---	---	---

TABLE 2.3-2 (Sheet 3 of 3)

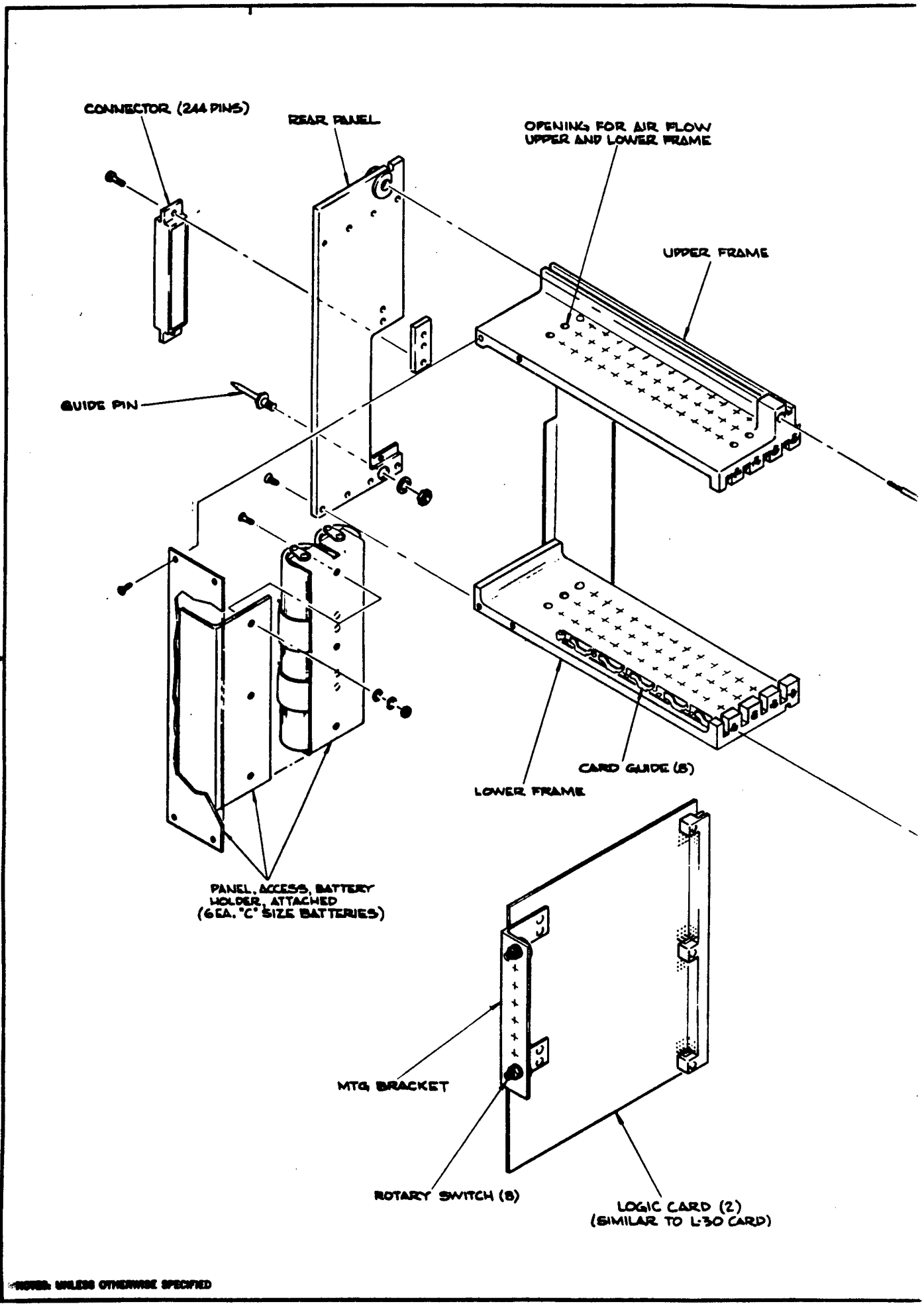
NOTES (CONTINUED)

7. The SEMI 4801 Device will not be available until the First Quarter of 1977. The ELECTRICAL CHARACTERISTICS COST AND AVAILABILITY Listed in this table for the device is based upon preliminary ADVANCE Engineering information received from the vendor.

TABLE 2.3-3

	91L40 BDM	SEMI 4801 (MIL Version)	SEMI M4200 UMC
Power Diss Dual 8K x 32	54W at + 5V	75 Watts at + 5V	OPERATING 50% Duty Cycle = 48 Watts STANDBY = 37W
DATA RETENTION BATTERY POWER DUAL 8K x 32	7.9W at 2.3V	4.45 Watts at 2.3V	.922W at (-4.8V) 1.64 Watt(+4.8V)
TIME TO DISCHARGE Ni-Cad BATTERIES	1.28 HRS	2.28 HRS	3.6 HRS (-4.8V) 3.43 HRS (+4.8V)
DEVICE OPERATING VOLTAGE	+ 5V	+ 5V	± 5V, + 12V
DEVICE DATA RETENTION VOLTAGE	+ 1.5V	+ 1.5V	- 4V, + 4V

NOTE: The characteristics shown above are at room temperature condition.



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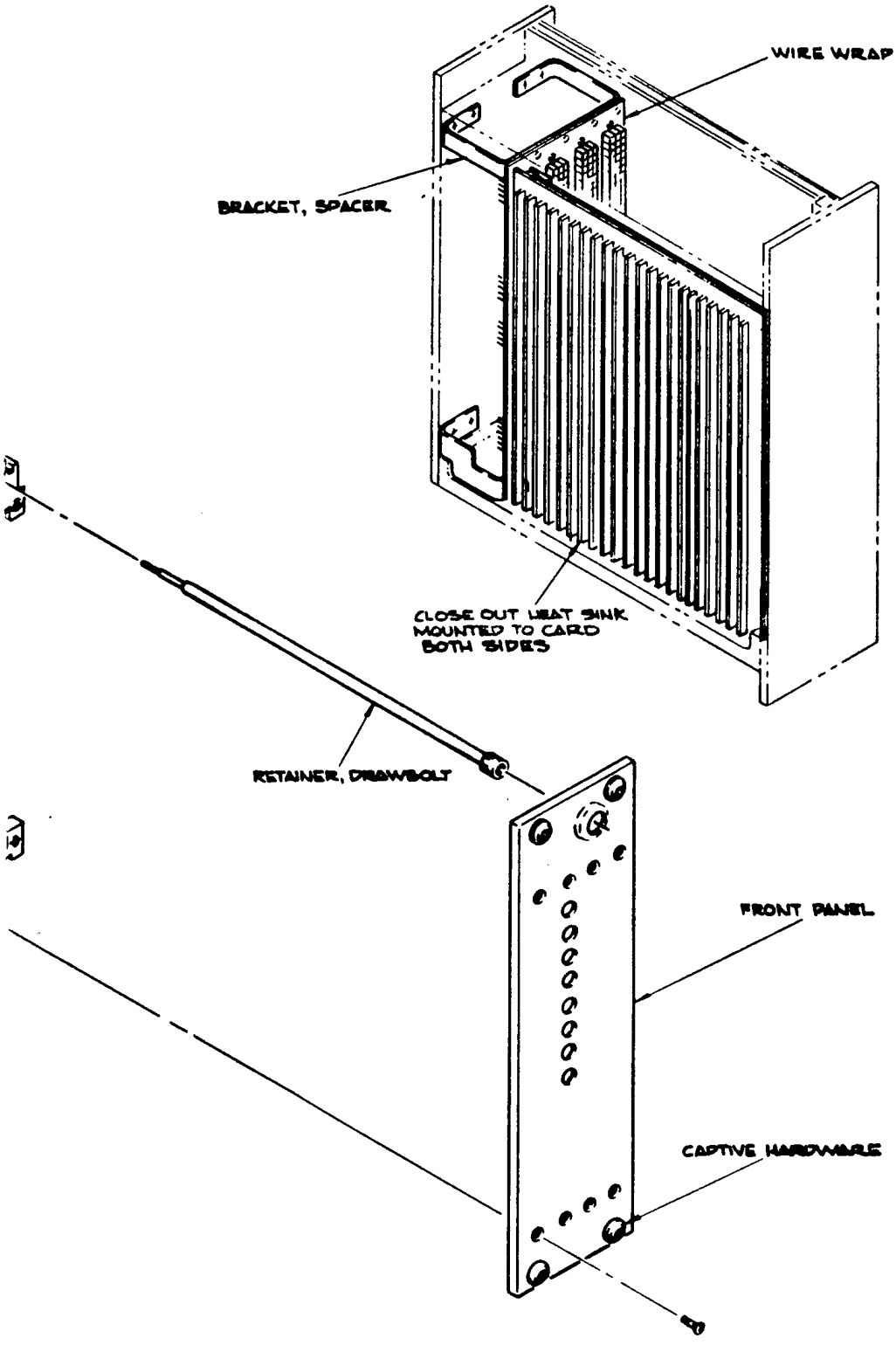

EXPLODED V

16KX32 N-MOS

FIG. 2.3-4

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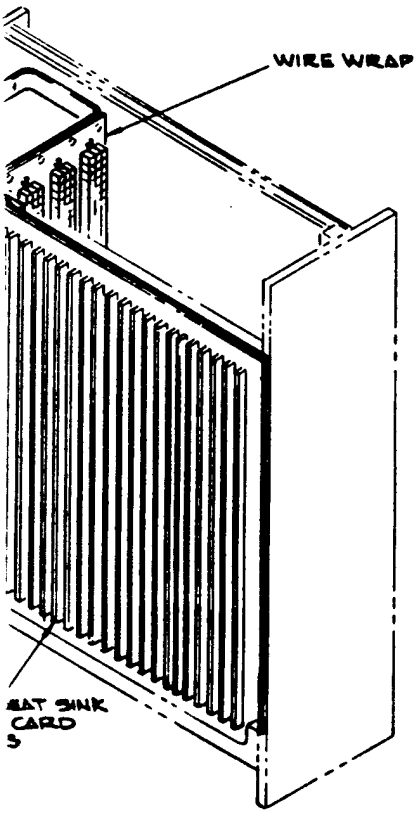
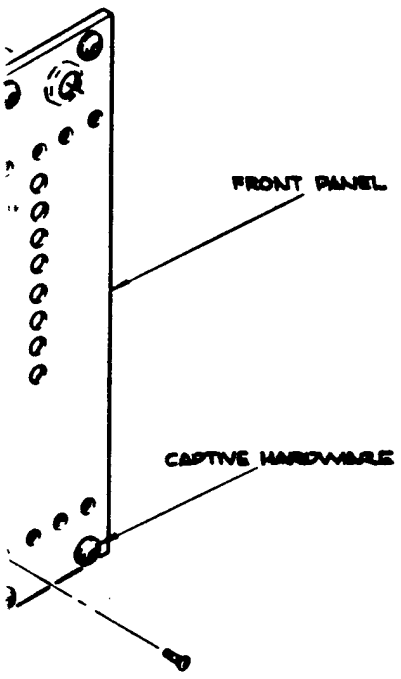




EXPLODED VIEW

16KX32 N-MOS MEMORY

FIG. 2.3-4

Each memory card contains sixty-four (64) 4K x 1 bit dual-in line integrated circuits and associated discrete components.

There are two logic cards; i.e., one for each memory. One logic card consists of 84 flat pack integrated circuits, a connector, eight bank address select switches and associated discrete components. The second card is similar to the first except there are no bank address select switches. All circuit cards are front removable and ride on guide rails. Access to the cards is via a removable front panel. Together, the circuit cards comprise two separate 8K x 32 bit memories giving a 16K x 32 bit memory assembly.

Six "C" size cells are required for the non-volatility requirement and are contained in a compartment in the rear of the assembly.

The weight of the entire assembly is estimated to be 15 pounds. Power dissipation is 54 watts.

2.3.3 Thermal Analysis NMOS

In a similar manner to that of the dual 8K core it can be shown that the surface temperature of the memory card to be 32°C and the surface temperature of the logic card to be 22°C if the AM91L40 device is used. If the SEMI-M4200 UMC device is used, memory card temperature is 29°C and the logic card temperature is 20°C, as shown in the thermal summary in Appendix D, rounded-off to the nearest degree.

2.4 CMOS Memory System (Dual 8K x 32)

2.4.1 Electrical Design

2.4.1.1 General

Utilizing the updated memory requirements of the E-2C L304F Computer as a model, a study was conducted on the feasibility of using

CMOS static semi-conducter RAM devices in a memory system. Table 1.1-1 contains characteristic data for a semi-conductor RAM memory using 24 static CMOS (1024 x 1) chips to form a hybrid Dual 4K x 32 CMOS RAM Device. Table 1.1-1 also compares the CMOS memory specification to the new L304F Computer specification.

2.4.1.2 Functional Description

A functional block diagram of a Dual 8K x 32 memory system is shown in Figure 2.4-1. The functional operation of the memory system is essentially the same as that described for the NMOS system in paragraph 2.3.1.2. Regarding the signals interfacing the memory WRA and the A & B Control Processors, the functional system operation is the same as the present E-2C L304F computer.

A simplified block diagram of a single 8K x 32 memory card is shown in Figure 2.4-2. The block diagram containing the 8K x 32 bits is comprised of 11 CMOS hybrid devices (each hybrid device 8K x 3). The hybrid device contains 24 Monolithic CMOS RAM chips. These chips contain a 1024 x 1 memory matrix. All the hybrids have external corresponding order address bits wired in parallel (12 bit address). The chip select 1 input signal on all 11 hybrids are wired in parallel and the same applies to the chip select 2 signal. The chip select 1 signal controls the selection of one 4K x 32 section and the chip select 2 signal controls the selection of the second 4K x 32 section. The output of the Bank Address Comparator is the initiating signal for the chip select 1 & 2 signals. Only one of these signals is conditioned at any one time or both of these signals are not activated at any one time. By initiating these signals

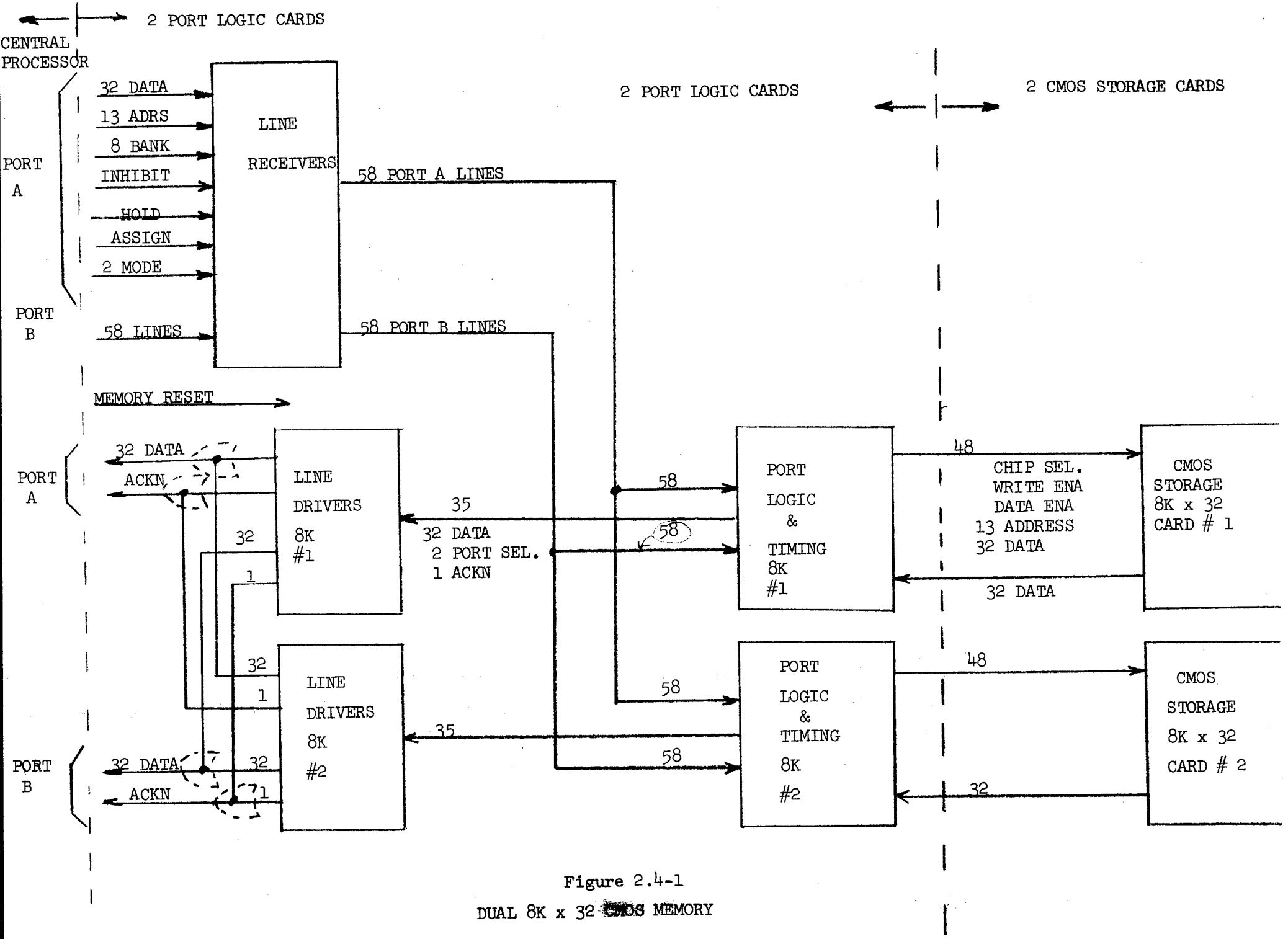


Figure 2.4-1

DUAL 8K x 32 CMOS MEMORY

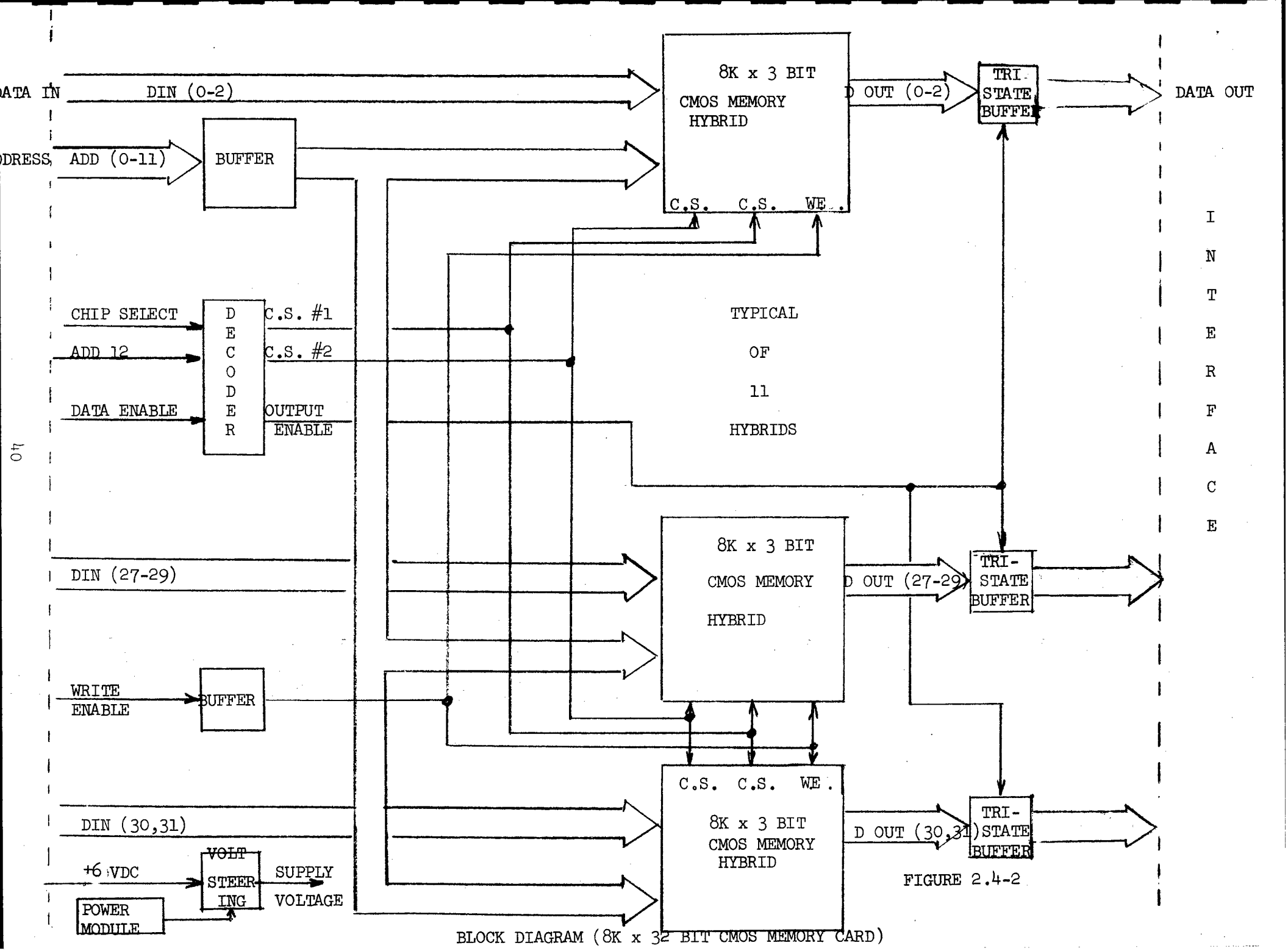


FIGURE 2.4-2

BLOCK DIAGRAM (8K x 32 BIT CMOS MEMORY CARD)

the Bank Address Comparator is able to select a particular 8K x 32 bit section. The write enable signal logic defines a Wire or Read operation. All Write enable signals of the 11 hybrids (8K x 32 memory) are wired in parallel.

Each of the 3 data output lines from each hybrid are wired to the input of Tri-State Buffers whose outputs are wired "Ored" to the corresponding order data outputs of the second 8K x 32 memory bank.

In the event of +6V power turn-off the Power Steering Circuitry provides an automatic control which eanables the battery voltage to the memory devices. This will enable the semiconductor memory to become non-volatile for a prescribed period of time.

2.4.1.3 System Characteristics

The memory capacity is a Dual 8192 word x 32 Bit Memory. This provides an effective total memory capacity of 16K x 32 bit. The Dual 8K x 32 bit configuration permits one central processor to access an 8K x 32 bit section while the second central processor to access the other 8K x 32 bit section; i.e., both sections can be accessed aimultaneously. The access times and cycle for each 8K x 32 bit section of the Dual 8K x 32 bit memory system are 600 nanoseconds and 800 nanoseconds respectively. The interface and operating modes are the same as described for NMOS in Section 2.3.1.3 above.

The basic storage device is a monolithic 1024 Word x 1 bit CMOS RAM Chip. Twenty-four of these chips are connected together within a 34 pin hermetically sealed package to form a dual 4096 x 3 hybrid RAM requiring +5, and +6 Volts. The monolithic Chip will be either the Harris or Intersil 6508 (see Table 2.4-1).

These devices are described further in Appendix C.

TABLE 2.4-1

1K C-MOS RAM STATIC

TYPE	MANUFACTURER	DEVICE NO.	DENSITY	ACCESS TIME	CYCLE TIME	TEMP RANGE	SUPPLY VOLTAGE	POWER DISSIAPTION	PRICE PER CHIP	PRICE PER CHIP BURN-IN	AVAILABILITY
C-MOS STATIC RAM	INTERSIL	1M6508 -1	1024 x 1	300NS	390NS	-55°C to +125°C	+5V	8.8MW	---	SEE NOTE 2	SEE NOTE 2
C-MOS STATIC RAM	HARRIS	HM6508	1024 x 1	400NS	650NS	-55°C to +125°C	+5V	15.3MW			
C-MOS STATIC RAM	INTERSIL	1M6508 (SPECIAL) SEE NOTE 1	1024 x 1	500NS at +5V 400NS at +6V	500NS at +5V 400NS at +6V	-55°C to +125°C	+5V	8.8MW at +5V 13.5MW at +6V (FROM DATA SHEET CURVE)	--	SEE NOTE 1	SEE NOTE 1

NOTES

1. IM 6508 (SPECIAL)

This unit is special because it will be the IM 6508 screened to obtain DATA RETENTION CURRENT = .1 MICROAMP

QTY	PRICE/DEVICE DOLLARS	PRICE/DEVICE BURN-IN	AVAILABILITY WEEKS ARO	AVAILABILITY WEEKS ARO BURN-IN
1000-4999	32.50	33.75	-----	6
5000-9999	29.20	30.45	-----	8
10K - 24999	27.40	28.65	------	12
25K - 49999	22.10	23.35	------	20
50K - 100K	19.50	20.75	-----	20

2. IM 6508 - 1

1000-4999	30.80	32.80	-----	6
5000-9999	27.20	29.20	-----	8
10K - 24999	25.45	27.45	----	12
25K - 49999	23.65	25.65	-----	20
50K - 100K	22.20	24.20	-----	20

2.4.1.3.1 Power Required

The following are the power requirements for the Dual 8K x 32 CMOS Semiconductor Memory based on the hybrid using the Intersil IM6508 (special). This device is special because it will be the IM6508 selected to obtain a data retention current equal to 0.1 microamps. Appendix C contains the supporting calculations.

- Power Dissipation (Dual 8K x 32) = 27 Watts
- Data Retention Battery Power = 158 microwatts at +3 Volts (Dual 8K x 32)
- Time to discharge Lithium Batteries = several years
- Device Operating Voltage = +5V, +6V
- Device Data Retention Voltage = +2.2 Volts.

2.4.1.3.2 Volatility

The CMOS volatility requirement is 2 hrs minimum (Design Goal). That is, the data contained within the CMOS Dual 8K x 32 semiconductor memory must be retained for a period of 2 hours following the removal of the normal operating +5V, and +6V supply voltages. When the +6V is removed, the Lithium Batteries (2 cells) supply 3 Volts d.c. required for data retention.

The CMOS Dual 8K x 32 memory described herein requires a power retention equal to 158 microwatts. Thus, a Lithium Battery supply would be discharged in 60,379 hrs or 6.8 years.

If Figure 2.3-3 is modified as that Diode D1 and Resistor R1 are eliminated and the Lithium Battery (primary cell) is substituted for the secondary cell, then the circuit will provide the required "ORING" action that will enable the selection of either +6 Volts d.c. or 3 Volt Battery.

2.4.2 Packaging CMOS

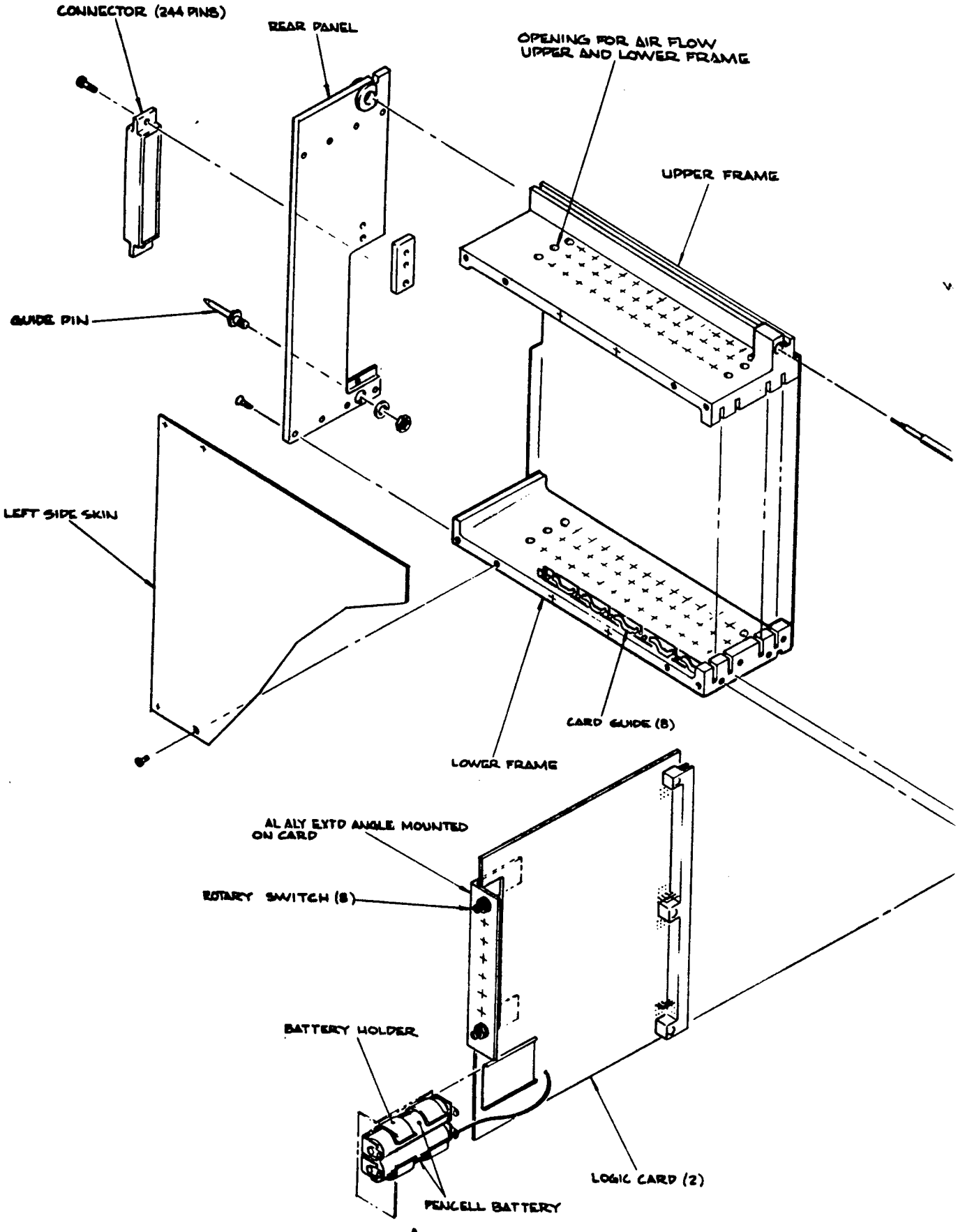
An exploded view of the CMOS memory assembly is shown in Figure 2.4-3. The physical description of the packaging arrangement is identical to that described for the NMOS memory assembly which is described in Section 2.3.2.

There are four removable plug-in multi-layer circuit cards. Two cards are for the memory functions and two for the logic functions, and are guided into place via card guides secured to the upper and lower frames. Together, these circuit cards comprise two separate 8K x 32 bit memory functions giving a 16K x 32 bit memory assembly.

Each memory card consists of eleven hybrid assemblies; i.e., an assembly comprised of 24 1K x 1 bit CMOS chips, a connector and associated discrete components. One logic card consists of 94 flat pack integrated circuits, eight address bank select switches, associated discrete components, and a connector. The second logic card is similar to the first except there are no bank address switches.

For the non-volatility requirement batteries can either be secured to one of the logic cards or they can be a separate plug-in cartridge, accessible from the front of the memory assembly. For purposes of illustration Figure 2.4-3 shows two AA cells that are front removable through an access plate.

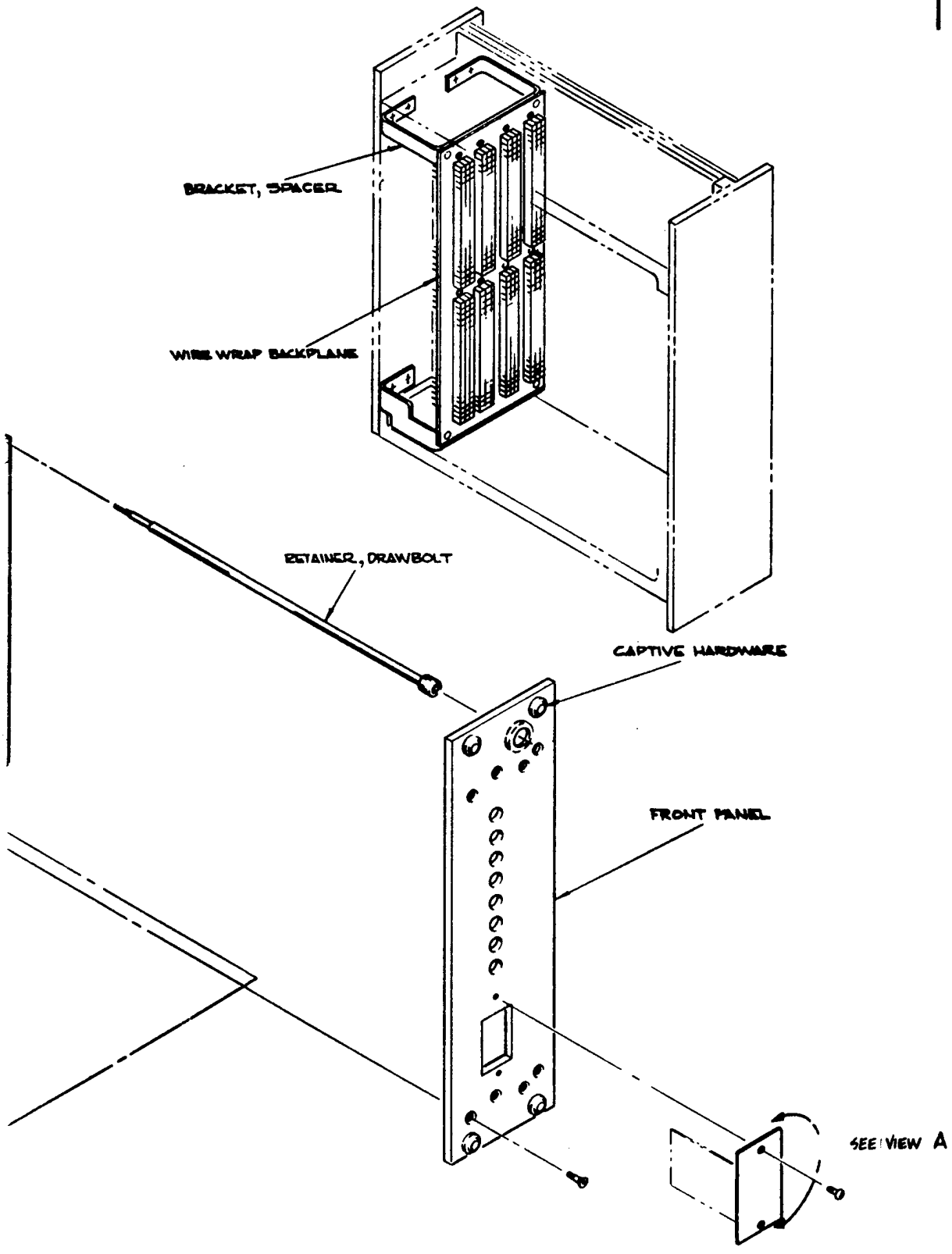
The weight of the entire assembly is estimated to be 12 pounds. Power dissipation is 27 watts.



VIEW A

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS		
ZONE	LTR	DESCRIPTION

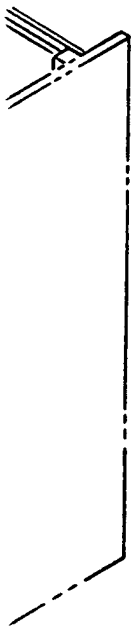


EXPLODED VI

16KX32 C-MOS

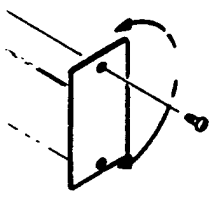
FIG. 2.4-

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



: HARDWARE

NT PANEL



EXPLODED VIEW

16KX32 C-MOS MEMORY

FIG. 2.4-3

2.4.3 Thermal Analysis CMOS

In a similar manner to that of the 8K core it can be shown that the surface temperature of the memory card is $15^{\circ}C$ and the surface temperature of the logic card is $20^{\circ}C$. This is shown in the thermal summary in Appendix D, rounded to the nearest degree.

2.5 Software

2.5.1 Memory Configuration

The software considerations described in the preliminary study report were based on two memory configurations; a dual 8K module operating functionally and electrically as two separate 8K memories, and a single 16K module addressable as two 8K memories but electrically configured to operate as a single 16K module. In the preliminary report the second (16K module) configuration led to a number of uncontrollable variables because of the independent addressing feature (i.e., both base memories could be in the same module, or the track file and the 4K duplicate could be in the same module, etc.). With the dual 8K memories programmers have complete control of dual processor memory access and can establish the memory address configuration which best minimized dual processor access of any single 8K memory address. However, the 16K module with independent 8K addressing allows programmer to pair any two memory addresses in the same module and requires the system to be designed and tested to operate in a worst case address mix.

Since completion of the preliminary report a third configuration has been considered, whereby the 16K module is addressable only as a pair of 8K modules. This allows the address switches to control only the three MSB's of memory address. This configuration completely eliminates uncertainty about dual access since the programmers know, by design, that address 0-1, 2-3, 4-5, etc. are single 16K modules. The system can be initially organized in the most efficient manner possible and not be subject to change except during reprogramming.

This configuration therefore eliminates a need for a worst case address mix for MAX load testing and allows all timing analysis and testing to be done with a single hardware configuration.

There is no apparent advantage to independent addressing, and there is software cost savings if memories are addressed only in pairs. This configuration will be used as a basis for comparison with the dual 8K in subsequent paragraphs.

2.5.2 Configuration Comparisons

Regardless of configuration, dual 8K or 16K, the associated software tasks are categorized into three basic groups:

- System Design/Requirements
- Program Design and Coding
- System Test and Evaluation.

The complexity, and thus the cost and risk, of the tasks in each of the above areas is somewhat greater for the 16K module than for a dual 8K configuration. Howerver, in both cases changes are relatively minor when compared to the total complexity of programs requiring modification.

For the dual 8K configuration the software effort in all areas is limited to changes required due to the decreased instruction execution time. While a system and program design effort are required to locate potentially critical timing loops, the major portions of this effort are coding changes and system test.

The 16K module requires, in addition to timing changes, tactical program functional modifications in the IFPM, Executive, and Display programs. This configuration also requires more testing

to evaluate tactical program operation with different memory address mixes (e.g., operation may be satisfactory with memory address of 0-1 and 2-3 as new memories and 4 to 9 as old, but not satisfactory with some other mix. Additional consideration must be given apropos the memory mixes in regard to degraded mode operation. With the existing 8K memory, a one module (8K) and a two module (16K) program has been developed. This must be modified to accommodate the new 16K memory module configuration.

2.5.3 Estimate of Processing Time Improvement 16K vs Dual 8K

There has been some question concerning the effect on real time gained if a 16K memory were used in lieu of a dual 8K memory. A test was performed in the laboratory as shwon in Appendix F with a tactical situation setup using tape N24. Various memory pairs were used to obtain Min and Max time loss. The result of using a 16K memory indicated that there is at most a 10 millisecond difference relative to the anticipated 4.5 to 5 second real time gain when compared to use of a dual 8K. This 10 millisecond time loss is considered negligible.

2.5.4 Overall Software Impart on Program

The introduction of additional memory into the E-2C will undoubtedly be accompanied by the simultaneous introduction of new functional capability. As a result a software redesign and check out will be a natural consequence of the change. The use of faster operating 16K blocks of memory in place of the current 8K modules may incur some slight extra cost in the generation of the revised software, but the major cost areas such as system test and documentation would be unaffected by the difference.

To minimize software costs and to maximize the benefits of replacement of 8K modules with 16K modules it will likely be preferred to require that the replacement modules be used in specific memory slots.

2.6 Power Supply Design

The present memory power supply, Litton part number 546176, provides power for two 8K by 32 bit core memory WRA's. The inputs to the power supply are unregulated d.c. voltages of 60 (floating), +30 and -12.5 volts obtained from an AC/DC converter WRA, Litton part number 546141. The outputs are regulated d.c. voltages of +5, +12, and -5 volts and a temperature controlled voltage for core writing that varies between -23 and -31.5 volts.

Table 2.6-1 lists the voltage and current requirements for the four 16K memory versions comparted to the present 8K memory. The power requirements for the proposed memories are less than those of the present 8K memories. However, the voltages and currents available from the power supply are not compatible with the proposed memories. The power supply must be modified to the requirements of the selected memory.

Figure 2.6-1 shows the present power supply block diagram and the modifications required to power the new memories.

The physical size and shape is identical to the existing memory power supply. The existing switching regulator is proposed for the new design. This technique provides high efficiency for the low voltage and high current power requirements and results in a lower power dissipation within the supply.

The core memory power supply utilizes the +30 volts and the floating 60 volts from the AC/DC converter WRA as inputs. The 60 volts is converted to -12 volts through a switching regulator that is similar in complexity to the existing card, part number 547571, in the present power supply. In addition to supplying the core

Table 2.6-1

Power Supply Requirements For 2 Memory WRA's

Current (AMPS)

VOLTAGE (VOLTS)	CMOS DUAL 8K by 32	NMOS DUAL 8K by 32		CORE DUAL 8K by 32	CORE 16K x 32	PRESENT CORE 8K by 32
		AM91L40	M4200			
+ 6	.33					
+15				2.2	4.0	
-12				17.0	23.2	
+ 5	10.4	23	10	16.8	15.4	11
- 5			0.5			1
-26						13
+12			4			2
POWER (WATTS)	54	115	100.5	321	415	422

switching current, the -12 volt regulator drives a +15 volt DC/DC converter. This converter card is also similar in complexity to the existing 547571 card. A new +5 volt regulator card is required, equal to the present card and a new logic card, similar to the present 547575 logic card. These changes, along with necessary components can be accommodated in the present memory power supply volume.

The design for the NMOS and CMOS memory power supplies also use the switching regulator. The CMOS memory requires two voltages, a +5 volt and a +6 volt supply. One version of the NMOS design, using the AM91L40 memory device requires a single +5 volt supply. The second NMOS version, using the EMM SEMI M4200 memory device, requires three voltages, +12 volts, +5 volts, and -5 volts.

For the CMOS design, the +5 volt supply is derived from the floating 60 volt input using the technique shown in Figure 2.6-1. Here, the 60 volts drives a +12 volt regulator card which in turn drives a DC/DC converter to produce the +5 volt output. The +6 volt supply is produced from the +30 volt input by employing a regulator card.

The power supply for the AM91L40 memory device is derived in a manner similar to that described for the +5 volt section of the CMOS memory power supply.

The supply for the M4200 memory device is required to produce three voltages. These are shown in Figure 2.6-1. The techniques are similar to the other power supply designs.

The regulator and converter cards along with the new filter capacitors and inductors which replace the present circuits, are easily contained in the present memory power supply volume.

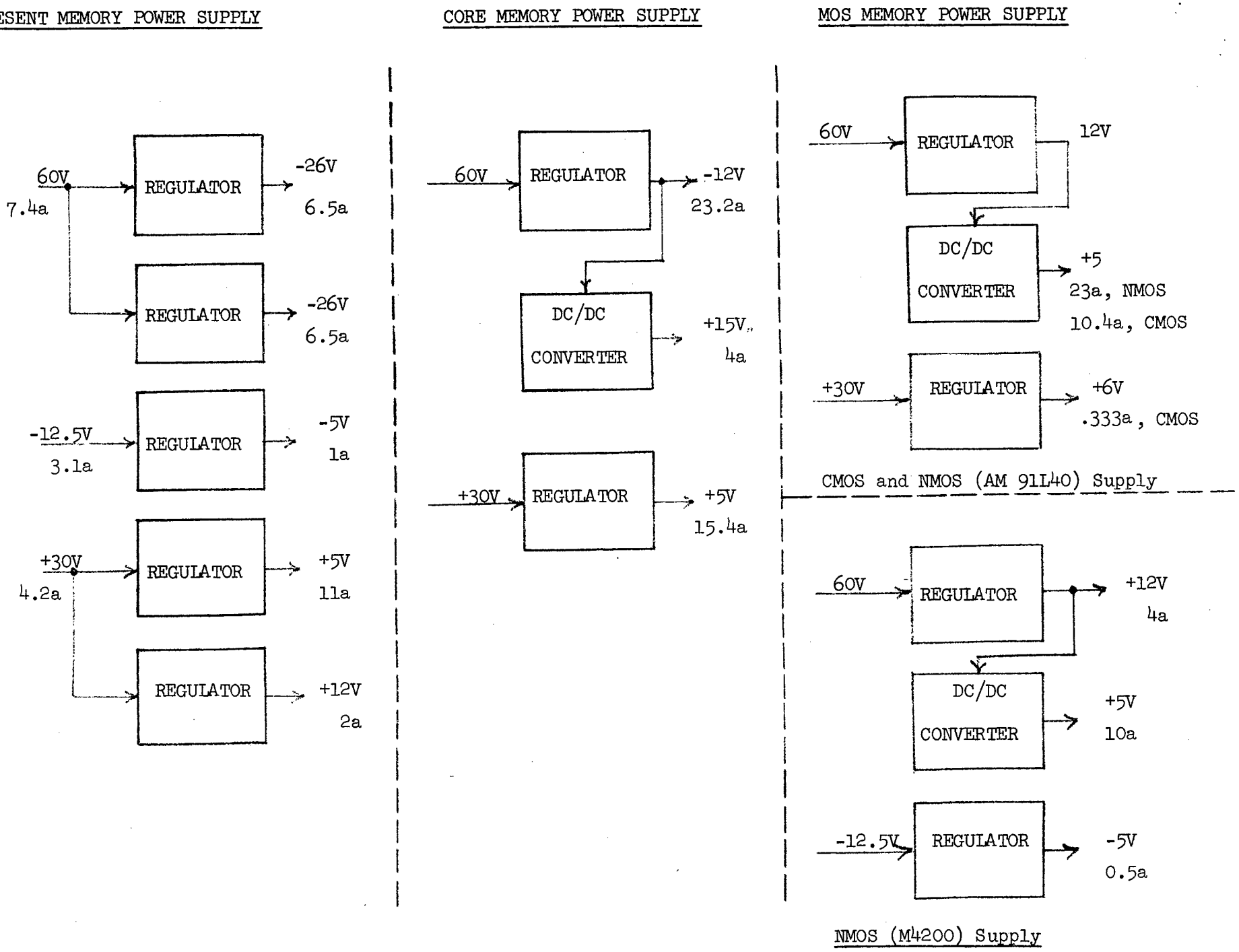


Figure 2.6-1 MEMORY POWER SUPPLY

For the new memory power supply design, no power sequencing required to retain memory contents during power transitions. The L304 Computer has a power transient interrupt and it goes through a power down sequence. The MOS memory designs use the power supply coupled with battery back-up power to retain memory contents during power down conditions.

Further details on the memory power supply design is shown in Appendix E.

2.7 Reliability

2.7.1 Introduction

This section provides the additional reliability study work performed for the addendum to the Conceptual Memory Technology Study. Reliability tasks performed for the initial study were reviewed and new inherent reliability predictions were calculated based on more detailed design configurations and thermal analyses.

2.7.2 Conclusions

Reliability predictions were made in accordance with the procedures and techniques of MIL-HDBK-217B (except where failure rates based on vendor life test date have been used for certain parts as noted below and in Appendix A). A summary of the results is given in Table 2.7-1 below.

Table 2.7-1

		Predicted MTBF (Hours)	
Configuration	Technology	Using Vendor Data for MOS Devices	Using MIL-HDBK-217B
A	CMOS Hybrid Dual 8K x 32	7,246	8,068
B	NMOS Monolithic Dual 8K x 32		
	- 4K RAM: AMD 9140	11,684	4,329
C	Core Dual 8K x 32 (Ampex)	-	8,278
D	Core 16K x 32 (Ampex)	-	10,085

Table 2.7-1 shows two different MTBF values for the MOS designs, one based on vendor data for the MOS devices and the other using the MIL-HDBK-217B monolithic microcircuit model (for NMOS) or the MIL-HDBK-217B hybrid microcircuit model (for the CMOS hybrid). The monolithic MOS and the hybrid microcircuit models of MIL-HDBK-217B are considered deficient by RADC, the preparing activity of this handbook. To correct these deficiencies, RADC has recently let a contract and has requested industry's assistance in updating & improving the hybrid model (Reference: Department of the Air Force Letter No. RBRAC/4151 dated 7/22/76.) In addition, the MOS monolithic model is currently being refined (Reference: Appendix IV of RADC Technical Report No. RADC TR-76-72 dated 3/76), however, additional empirical data is still required. For these reasons, and also that MIL-HDBK-217B does not differentiate between CMOS and NMOS, failure rates for the CMOS and NMOS devices were based on vendor life test data (Reference: Intersil CMOS RAM Reliability Report dated 5/76 and Intel Report No. RR-7 dated 9/75). This data represents the most meaningful and realistic source of such failure rate data currently available. This data was extrapolated to the required temperatures using the Arrhenius expression given in Intel Report RR-7. Telephone conversation with RADC personnel has endorsed GAC's approach regarding the use of vendor MOS data in light of the current 217B inadequacies. Revision of MIL-HDBK-217B was also verified to be in progress but was not expected to be completed for at least another year.

It should be noted that Litton DSD was contracted by GAC to calculate the MTBF for each of the four design configurations using MIL-HDBK-217B. The Litton DSD results were within 3% of the GAC values.

The data in Table 2.7-1 indicates that all of the designs are capable of meeting the existing system reliability requirement of 7500 hour MTBF with the exception of the CMOS hybrid design.

As seen in Table 2.7-1, the NMOS design has the highest inherent MTBF with the 16K core memory second. The CMOS hybrid and dual 8K core designs have significantly lower MTBF's. In the case of the CMOS design this is because of the risk factor and high failure rate associated with the use of high complexity hybrids requiring a very large number of internal thermocompression bonds (approximately 200) in their assembly. Monolithic NMOS does not present this risk, however, both MOS designs require the use of batteries to retain memory information in the event of power loss. Battery reliability was considered in the predictions; additionally their use necessitates maintenance not necessary with the core memory designs.

The reliability of the Dual 8K Core Memory design is less than the 16K core design because of the higher parts count and higher average part surface temperature.

The 16K core design is recommended from a reliability viewpoint considering the high MTBF and the absence of batteries.

2.7.3 Differences From Earlier Study

Reliability estimates for the four proposed computer memory designs have been further refined as a result of more accurate definition of thermal profiles and design configurations. The reliability prediction for the CMOS design increased considerably from the previous estimate due to the lower average part surface temperature as determined from current thermal analyses.

The predicted MTBF for the Dual 8K Core design increased significantly to almost double the original values due to lower calculated ambient temperatures based on more detailed mechanical design layouts.

Since the initial study, ambient temperatures for the NMOS design also decreased resulting in an increase in MTBF even though there was an increase in battery cell count from 3 to 6.

The predicted MTBF of the 16K core design decreased by approximately 11% due to an increased parts count resulting from refinement of the bill of material.

2.7.4 Data Sources and Assumptions

The predicted inherent reliabilities for the four design configurations, to the part level, are given in tables A-1 through A-5. Parts count and temperature information were obtained from current configurations and thermal analyses contained in this report. All failure rate calculations, except as noted, were in accordance with MIL-HDBK-217 revision B methods and failure rate data for an airborne inhabitated environment. The predictions were based on the assumption of mature devices and equipments, use of MIL-M-38510, level B microcircuits, JAN TX semiconductor, and ER level M parts, or their equivalent.

The failure rates for transistors, diodes, resistors, and capacitors of the semiconductor memories and for all of the logic boards were based on an electrical (power or voltage, as applicable) stress level of 30% which is the design goal which is considered suitable derating for high reliability applications. The failure rate of these parts for the Ampex memories, where derating could not be as conservative because of packaging constraints, was based on an average electrical stress level of 45%. There are peak stresses that are higher in the Ampex units, however, considering duty cycle the average stress is always less than 45%. This is still considered to be a reasonable stress level as verified by the high resultant reliability.

Failure rates for memory cores and batteries are not given in MIL-HDBK-217B therefore vendor data was used in the calculations. Battery failure rates were determined from field data and a survey of data from battery manufacturers performed during the initial Memory Technology Study. Based on that survey, nickel-cadmium battery failure rates varied between two failures per million (FPM) hours/per cell for manufacturer's data to 36 FPM/Cell for CAINS field data. For the E-2C application which considered standby power for a solid state memory, it was estimated that a failure rate of 5 FPM/cell could be achieved. It was estimated that the lithium battery with its longer shelf life and low current drain application would be more reliable than NiCd with a failure rate of 3 FPM/cell. It is assumed that previous safety hazards of lithium batteries have been eliminated by safety venting and power limiting designs.

3.0 Updated Tradeoff of Memory Approaches and Conclusion

The tradeoff factors shown in the Grumman Report #75 148-20 of February 1976 have been retained for this evaluation, Table 3.1 provides a reevaluation of the memory design based on the utilization of either 13 or 14 MIL core (dual 8K and 16K configurations), CMOS hybrid and NMOS static 4K chip semiconductor technologies. The revised table results from changes made in the areas of reliability, packaging, software, cost and power supply requirements, and refinements resulting from the more detailed analysis of the above areas. The basis for these changes is provided in the previous sections.

3.1 Semiconductor Memory

From the view point of future growth capability, semiconductor memories are still acceptable for future military applications. This is consistent with the previous findings and includes consideration of data retentivity. This study effort substantiated that CMOS required considerably less power than NMOS. However, special consideration must be given to the problem of excessive hybrid failures that Grumman has encountered in the past and at the present. The actual MTBF that results reflects a lower reliability in CMOS, not withstanding the lower power demands and lower temperature anticipated in operation compared to previous estimates.

In the case of NMOS, based on the use of the AMD 91L40 chip, MIL qualified, operating and data retentivity power as well as cost factors are higher than for the EMM #M4200 device. The

TABLE 3.1

Memory Tradeoff Evaluation

Factor	Weight (CW) (e)	16K x 32 Bit 14K Mil Core Value(V)	WXV	Dual 8K (14 MIL) Core Value (V)	WXV	4K NMOS* (a) Value(V)	WXV	CMOS Hybrid Value(V)	WXV
EMC	8	9	72	9	72	6	48	7	56
Software	7	7	49	8	56	8	56	8	56
Available	6	9	54	7	42	7	42	9	54
Qual.	4	7	28	6	24	5	20	7	28
Reliabil.	10	10	100	8	80	10	100	7 (d)	70
Rel.Wt.	3	7	21	6	18	7	21	10	30
Power/P.S.	5	6	30	5	25	8	40	9	45
Packaging	8	7	56	5	40	9	72	10	80
Maintain	8	7	56	6	48	9	72	7 (b)	56
SUBTOTAL			459		405		471		475
Battery	10	10	100	10	100	3	30	6	60
Sub Total			566		505		501		535
Rel Cost	10	6	60	5	50	9 (c)	90	7	70
			626		555		591		605

Note (a) Dual In Line Package (no hybrids)

(b) Assumes hybris is throwaway, hybrid replacement cost not accounted for in this table.

(c) Based on EMM Cost; costs with AMP 91640 chip is somewhat higher.

(d) Failure rates for hybrids in MTBF calculations is for devices manufactured by vendors of of average quality.

(e) Weight (W) numbers assigned according to selective importance to E-2C, Value (V) numbers estimate of technology compleaned for each factor.

militarized version EMM #M4200 will be available within the next few months. The relative cost shown is based on NMOS device forecast by EMM. Because NMOS can attain greater density and is a less complex process compared to CMOS, the manufacturing costs will be consistently lower for NMOS. As shown in Table 2.3.3, data retentivity with batteries can be provided for more than 2 hours utilizing the EMM device. Lower power demands, lower temperatures and a higher reliability are estimated when using the EMM design due to a reduction in the standby mode. Further power reduction are indirected in this design in proportion to the % duty cycle. While semiconductor memories are presently excluded for the E2C application by Navy, in view of the need for batteries, combinations of non-volatile storage for program memory such as Bubble or MNOS in conjuction with volatile RAM memory such NMOS, SOS or I^2L still appears to be a viable approach for future military A/C application (beyond the time frame for the planned E2C revision).

3.2 Core Memory

In the utilization of core memory, both the dual 8K and 16K configurations are feasible. The software impact of going to a 16K as compared to a dual 8K is described in section 2.5. When the effect of addressability in pairs is considered, the problem associated with the software change is not as extensive as indicated in the prior report. Hence, the increase value of 7 was made as shown in table 3.1 for the 16K core. It is also significant that the 16K reliability will increase with the new packaging config-

uration, described in Section 2, which permits the use of a modified off-the-shelf memory such as the 16K c,18 bit AMPEX MESA9.

3.2 Conclusion

Table 3.2 Summarizes some of the more pertinent points of the study and reflects an update of the previous study report results. The conclusion reached is that the 16K core memory now appears as most effective approach for the E2C application. While the recurring cost is higher for core compared to the semiconductor memories, the risk is lower for E2C application.

Table 3.2

Summary of Memory Study Results

Core

- 16K, MIL "off-the-shelf" designs can fit in allowable space based on the new packaging approach.
- Dual 8K core and 16K core designs appear feasible.
- The use of a core memory provides a non-volatile memory without the need for a battery backup.
- Power supply must be redesigned.
- Core technology is a proven technique; qualifying a new design should be readily achieveable.
- The 16K core memory provides nominal risk.
- Software changes are feasable with a 16K configuration with allowance for addressability as pairs.
- > 10K hour of inherent reliability provided by 16K

Solid State

- Dual 8K designs are readily feasible.
- Solid state designs offer advantages in cost, size, weight, and power.
- For CMOS a primary battery is preferred e.g., Lithium or Silver Oxide; NMOS secondary, battery should be used e.g., Nickel Cadmium. Both will exceed a 2 hour non-volatility requirement.
- Power supply redesign appears necessary

  NMOS provides the best potential of the three technology candiates for future growth in speed improvement.
- Based on the use of actual vendor test data NMOS reliability is better than CMOS.
- Lowest power, data retentivity (> 1 year) and less weight provided by CMOS.

4.0 APPENDICES

A. RELIABILITY

B. NMOS

C. CMOS

D. THERMAL ANALYSIS

E. POWER SUPPLY

F. PRELIMINARY LABORTORY TESTS FOR COMPUTER PROGRAMMER 16K MEMORY STUDY

APPENDIX A

RELIABILITY

Table A-1

Failure Rate Summary

CMOS Dual 8K x 32 Memory

Memory Cards (2) (Note 1)

Part Name & Type	Quantity (N)	λ X 10^{-6} (Note 2)	N λ X 10^{-6}
Multi-Layer Board	2	0.6175	1.234
Microcircuit (CMOS Hybrid)	22	4.2540	93.588
Microcircuit (54S04)	6	0.0601	0.361
Microcircuit (54S366)	12	0.0634	0.761
Microcircuit (54LS156)	2	0.0856	0.171
Microcircuit (54LS04)	4	0.0601	0.240
Microcircuit (54LS00)	2	0.0518	0.104
Transistor (2N3457)	2	0.112	0.224
Diode (1N914A)	6	0.0452	0.271
Resistor Network	2	0.1040	0.208
Resistor (RLR)	30	0.0104	0.312
Capacitor (CK05)	60	0.0156	0.936
Connector (210 Pin)	2	2.4000	4.800
Solder Connections	1206	0.00012	0.145
		SUBTOTAL	103.356

Dual 2 Port Logic Cards (2) (Note 4)

Part Name & Type	Quantity (N)	λ X 10^{-6} (Note 2)	NλX 10^{-6}
Multi-Layer Board	2	0.7710	1.542
Microcircuit (54LS04)	7	0.0603	0.422
Microcircuit (54LS00)	24	0.0521	1.250
Microcircuit (54LS10)	9	0.0463	0.417
Microcircuit (54LS20)	17	0.0405	0.689
Microcircuit (54LS74)	4	0.0603	0.241
Microcircuit (54LS298)	16	0.1156	1.850
Microcircuit (54LS75)	2	0.0778	0.156
Microcircuit (54H04)	17	0.0603	1.025
Microcircuit (54S04)	8	0.0603	0.482
Microcircuit (54S00)	4	0.0521	0.208
Microcircuit (54S10)	3	0.0463	0.139
Microcircuit (54S30)	4	0.0315	0.126
Microcircuit (54S74)	2	0.0603	0.121
Microcircuit (54S74)	4	0.1159	0.464
Microcircuit (54S64)	8	0.0562	0.450
Microcircuit (54S157)	24	0.0861	2.066
Microcircuit (Lamp Driver)	33	0.0521	1.719
Capacitor (CK)	26	0.0156	0.406
Connector (210 Pin)	2	2.8000	5.600
Oscillator (25 MHZ)	1	0.9000	0.900
Switch (Rotary)	8	1.0000	8.000
Battery (Lithium)	2	3.0000 (Note 5)	6.000
Solder Connectors	3114	0.00012	0.373
		SUBTOTAL	34.647
		TOTAL	138.003
		MTBF	7246 HOURS

NOTES:

1. 14.8°C average part surface temperature and 30% electrical stress used in calculations.
2. Failure rate per MIL-HDBK-217B unless otherwise noted.
3. Failure rate based on Intersil CMOS RAM Reliability Report (5/76).
4. 19.6°C average part surface temperature and 30% electrical stress used in calculations.
5. Failure rate per GAC industry survey.

Table A-2

Failure Rate Summary

NMOS (AMD9140) Dual 8K x 32 Memory

Memory Cards (2) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	2	0.7710	1.542
Microcircuit (4K RAM)	128	0.1120 (Note 3)	14.336
Microcircuit (54LS04)	24	0.0613	1.471
Microcircuit (54LS366)	12	0.0647	0.776
Microcircuit (54LS00)	2	0.0528	0.106
Microcircuit (54LS30)	8	0.0318	0.254
Diode (1N645)	2	0.0222	0.044
Resistor (RLR)	8	0.0117	0.094
Capacitor (CK05)	80	0.0164	1.312
Connector (210 Pin)	2	3.8400	7.680
Solder Connections	4236	0.00012	0.508
		SUBTOTAL	28.123

Dual 2 Port Logic Cards (2) (Note 4)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	2	0.7710	1.542
Microcircuit (54LS04)	7	0.0604	0.423
Microcircuit (54LS00)	24	0.0522	1.253
Microcircuit (54LS10)	9	0.0464	0.418
Microcircuit (54LS20)	17	0.0406	0.690
Microcircuit (54LS74)	4	0.0604	0.242
Microcircuit (54LS298)	16	0.1161	1.858
Microcircuit (54H04)	17	0.0604	1.027
Microcircuit (54S04)	8	0.0604	0.483
Microcircuit (54S00)	4	0.0522	0.209
Microcircuit (54S10)	3	0.0464	0.139
Microcircuit (54S30)	4	0.0316	0.126
Microcircuit (54S74)	2	0.0604	0.121
Microcircuit (54S174)	4	0.1164	0.466
Microcircuit (54S64)	8	0.0562	0.450
Microcircuit (54S157)	8	0.0863	0.690
Microcircuit (Lamp Driver)	33	0.0522	1.723
Capacitor (CK)	26	0.0160	0.416
Connector (210 Pin)	2	2.9600	5.920
Oscillator (25 MHZ)	1	0.9000	0.900
Switch (Rotary)	8	1.0000	8.000
Battery (Ni Cad)	6	5.0000 (Note 5)	30.000
Solder Connections	3086	0.00012	0.370
		SUBTOTAL	57.466
		TOTAL	85.589
		MTBF	11,684 HOURS

NOTES:

1. 31.8°C average part surface temperature and 30% electrical stress used in calculations.
2. Failure rate per MIL-HDBK-217B unless otherwise noted.
3. Failure rate per Intel Reliability Report RR-7 (9/75)
4. 21.9°C average part surface temperature and 30% electrical stress used in calculations.
5. Failure rate per GAC industry survey.

Table A-3

Failure Rate Summary

NMOS (SEM M4200) Dual 8K x 32 Memory

Memory Cards (2) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	2	0.7710	1.542
Microcircuit (4K RAM)	128	0.1010 (Note 3)	12.928
Microcircuit (54LS04)	24	0.061	1.464
Microcricuit (54LS366)	12	0.0644	0.773
Microcircuit (54LS00)	2	0.0526	0.105
Microcircuit (54LS30)	8	0.0317	0.254
Diode (IN645)	2	0.0195	0.039
Resistor (RLR)	8	0.0116	0.093
Capacitor (CK05)	80	0.0163	1.304
Connector (210 pin)	2	3.5200	7.040
Solder Connections	4236	0.00012	0.508
		SUBTOTAL	26.050

Dual 2 Port Logic Cards (2) (Note 4)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	2	0.7710	1.542
Microcircuit (54LS04)	7	0.0603	0.422
Microcircuit (54LS00)	24	0.0521	1.250
Microcircuit (54LS10)	9	0.0463	0.417
Microcircuit (54LS20)	17	0.0405	0.689
Microcircuit (54LS74)	4	0.0603	0.241
Microcircuit (54LS298)	16	0.1156	1.850
Microcircuit (54H04)	17	0.0603	1.025
Microcircuit (54S04)	8	0.0603	0.482
Microcircuit (54S00)	4	0.0521	0.208
Microcircuit (54S10)	3	0.0463	0.139
Microcircuit (54S30)	4	0.0315	0.126
Microcircuit (54S74)	2	0.0603	0.121
Microcircuit (54S174)	4	0.1159	0.464
Microcircuit (54S64)	8	0.0562	0.450
Microcircuit (54S157)	8	0.0861	0.689
Microcircuit (Lamp Driver)	33	0.0521	1.719
Capacitor (CK)	26	0.0160	0.416
Connector (210 pin)	2	2.8000	5.600
Oscillator (25 MHz)	1	0.9000	0.900
Switch (Rotary)	8	1.000	8.000
Battery (Ni Cad)	6	5.000 (Note 5)	30.000
Solder Connections	3086	0.00012	0.370
		SUBTOTAL	57.120
		TOTAL	83.170
		MTBF	12,024 hours

NOTES:

1. 29°C average part surface temperature and 30% electrical stress used in calculations.
2. Failure rate per MIL-HDBK-217B unless otherwise noted.
3. Failure rate per Intel Reliability Report RR-7 (9/75).
4. 19.5°C average part surface temperature and 30% electrical stress used in calculations.
5. Failure rate per GAC industry survey.

Table A-4

Failure Rate Summary

Core Dual 8K x 32 Memory (Ampex)

Drive Boards (4) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	4	0.3000	1.200
Microcircuit (5437)	4	0.0564	0.226
Microcircuit (55326)	28	0.0662	1.854
Microcircuit (55237)	28	0.0662	1.854
Microcircuit (54145)	12	0.1024	1.229
Microcircuit (55236)	32	0.2860	9.152
Microcircuit (54H04)	28	0.0660	1.848
Microcircuit (5438)	16	0.0564	0.902
Quad Transistor (NPN)	84	0.1050	8.820
Quad Transistor (PNP)	28	0.1680	4.704
Diode Array	36	0.0333	1.199
Resistor Network	64	0.0370	2.368
Resistor (RNC 50)	8	0.0160	0.128
Resistor (RWR 81)	4	0.0594	0.238
Capacitor (CKR11)	72	0.0392	2.822
Capacitor (CKR06)	32	0.0392	1.254
Capacitor (CSR 23)	16	0.0480	0.768
Capacitor (CY 12)	52	0.0420	2.184
Inductor	16	0.0330	0.528
Solder Connections	5216	0.00012	0.626
		SUBTOTAL	43.904

Timing/Control Boards (2) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	2	0.765	1.530
Microcircuit (54S02)	2	0.0564	0.113
Microcircuit (54H20)	2	0.0433	0.087
Microcircuit (54H74)	2	0.0660	0.132
Microcircuit (54H00)	14	0.0564	0.790
Microcircuit (54H04)	4	0.0660	.0264
Microcircuit (54S175)	8	0.1341	1.073
Microcircuit (5409)	4	0.0564	0.226
Microcircuit (52711)	2	0.2088	0.418
Microcircuit (52747)	4	0.2214	0.886
Microcircuit (52723)	2	0.1274	0.255
Microcircuit (5475)	8	0.1230	0.984
Quad Transistor (NPN)	6	0.1050	0.630
Quad Transisitor (PNP)	12	0.1680	2.016
Transistor (2N3740)	2	0.0840	0.168
Diode Array	8	0.0333	0.266
Diode (1N749A) & (1N746A)	4	0.1675	0.670
Diode (1N829A)	2	0.2513	0.503
Resistor Network	24	0.0370	0.888
Resistor (RNC50)	104	0.0160	1.664
Resistor (RNC55)	24	0.0160	0.384
Resistor (RWR81)	12	0.0594	0.713
Capacitor CKR11	24	0.0392	0.941

Table A-4 continued

Part Name & Type	Quantity (N)	λ X 10^{-6} (Note 2)	Nλ X 10^{-6}
Capacitor CKR06	8	0.0392	0.314
CSR23	18	0.0480	0.864
CCR75	12	0.0594	0.713
CY12	28	0.0420	1.176
Inductor	2	0.0330	0.066
Delay Line	2	0.0400	0.080
Solder Connections	1878	0.00012	0.225
		SUBTOTAL	19.039

Stack Boards (4) (Note 1)

Part Name & Type	Quantity (N)	λ X 10^{-6} (Note 2)	Nλ X 10^{-6}
Multi-Layer Board	4	0.2880	1.152
Diode Array	72	0.0333	2.398
Resistor Network	96	0.0370	3.552
Core (Ferrite)	590K	1.2 X 10^{-6} (Note3)	0.708
Solder Connections	3888	0.00012	0.467
		SUBTOTAL	8.277

Interconnects

Part Name & Type	Quantity (N)	λ X 10^{-6} (Note 2)	Nλ X 10^{-6}
Connector (External)	1 (mtd pair)	5.400	5.400
Connector (Internal)	10 (mtd pairs)	1.6100	1.6100
		SUBTOTAL	21.500

Dual 2 Port 8K Logic Cards (2)(Note 4)

Part Name & Type	Quantity (N)	λ X 10^{-6} (Note 2)	NλX 10^{-6}
Multi-Layer Board	2	0.6990	1.398
Microcircuit (54LS04)	7	0.0608	0.426
Microcircuit (54LS00)	24	0.0525	1.260
Microcircuit (54LS10)	9	0.0466	0.419
Microcircuit (54LS20)	17	0.0408	0.694
Microcircuit (54LS74)	4	0.0608	0.243
Microcircuit (54LS298)	16	0.1173	1.877
Microcircuit (54H04)	17	0.0608	1.034
Microcircuit (54S04)	8	0.0608	0.486
Microcircuit (54S00)	4	0.0525	0.210
Microcircuit (54S10)	3	0.0466	0.140
Microcircuit (54S30)	4	0.0317	0.127
Microcircuit (54S74)	2	0.0608	0.122
Microcircuit (54S174)	4	0.1177	0.471
Microcircuit (54S64)	8	0.0566	0.453
Microcircuit (54S157)	8	0.0870	0.696
Microcircuit (Lamp Driver)	33	0.0525	1.733
Capacitor (CK)	24	0.0150	0.360
Connecotr (210 Pin)	2	3.3600	6.720

Dual 2 Port 8K Logic Card (2) (Note 4) continued Table A-4

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Oscillator (25 MHZ)	1	0.9000	0.900
Switch (Rotary)	8	1.0000	8.000
Solder Connections	2640	0.00012	0.317
		SUBTOTAL	28.086
		TOTAL	120.806
		MTBF	8278 hours

NOTES:

1. 59.2°C average part surface temperature and 45% electrical stress used in calculations.
2. Failure rate per MIL-HDBK-217B unless otherwise noted.
3. Failure rate based on Ampex experience.
4. 27°C average part surface temperature and 30% electrical stress used in calculations.

Table A-5

Failure Rate Summary

Core 16K Memory (Ampex)

Drive Boards (4) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	4	0.2520	1.008
Microcircuit (5437)	4	0.0551	0.220
Microcircuit (55326)	32	0.0636	2.035
Microcircuit (55327)	32	0.0636	2.035
Microcircuit (54145)	12	0.0987	1.184
Microcircuit (55236)	20	0.2520	5.040
Microcircuit (54H04)	20	0.0643	1.286
Microcircuit (5438)	16	0.0551	0.882
Microcircuit (54LS138)	16	0.0551	0.882
Micorcircuit (54S00)	4	0.0551	0.220
Microcircuit (54S03)	12	0.0551	0.661
Quad Transistor (NPN)	52	0.0924	4.805
Quad Transistor (PNP)	20	0.1470	2.940
Diode Array	36	0.0327	1.177
Resistor Network	40	0.0337	1.348
Resistor (RNC 50)	8	0.0145	0.116
Resistor (RNC 55)	36	0.0145	0.522
Resistor (RWR 81)	4	0.0540	0.216
Resistor (RLR)	32	0.0169	0.541
Capacitor (CKR 11)	12	0.0356	0.427
Capacitor (CKR 06)	32	0.0356	1.139
Capacitor (CSR 23)	16	0.0460	0.736
Capacitor (CY 12)	52	0.0312	1.622
Inductor	12	0.0300	0.360
Solder Connections	4616	0.00012	0.554
		SUBTOTAL	31.956

Timing/Control Boards (2) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	2	0.627	1.254
Microcircuit (54S02)	2	0.0551	0.110
Microcircuit (54H20)	2	0.0425	0.085
Microcircuit (54H74)	2	0.0643	0.129
Microcircuit (54H00)	14	0.0551	0.771
Microcircuit (54H04)	4	0.0643	0.257
Microcircuit (54S175)	8	0.1285	1.028
Microcircuit (5409)	4	0.0551	0.220
Microcircuit (52711)	8	0.1864	1.491
Microcircuit (52747)	6	0.1972	1.183
Microcircuit (52723)	2	0.1224	0.245
Microcircuit (5475)	8	0.1182	0.946
Microcircuit (54367)	16	0.0719	1.150
Quad Transistor (NPN)	6	0.0924	0.554
Quad Transistor (PNP)	12	0.1470	1.764
Transistor (2N3740)	2	0.0462	0.092
Transistor (2N5582)	4	0.0462	0.185

Table A-5 --- cont'd

Timing/Control Boards --- cont'd

Diode Array	8	0.0327	0.262
Diode (1N746A)	2	0.1500	0.300
Diode (1N749A)	2	0.1500	0.300
Diode (1N829)	2	0.2250	0.450
Diode (1N4150)	4	0.0431	0.172
Resistor Network	26	0.0337	0.876
Resistor (RNC 50)	104	0.0145	1.508
Resistor (RNC 55)	24	0.0145	0.348
Resistor (RWR 81)	6	0.0540	0.324
Capacitor (CKR)	44	0.0356	1.566
Capacitor (CSR 13)	18	0.0460	0.828
Capacitor (CCR 75)	4	0.0480	0.192
Capacitor (CY 12)	28	0.0312	0.874
Inductor	2	0.0300	0.060
Solder Connections	1906	0.00012	0.229
Delay Line	2	0.0400	0.080
		SUBTOTAL	19.830

Stack Boards (4) (Note 1)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	4	0.2880	1.152
Diode Array	128	0.0327	4.186
Resistor Network	60	0.0337	2.022
Core (Ferrite)	590K	1.2×10^{-6} (Note 3)	0.708
Solder Connections	4136	0.00012	0.496
		SUBTOTAL	8.564

Interconnects

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Connector (External)	1 (mtd pair)	4.800	4.800
Connector (Internal)	10 (mtd pairs)	1.3560	13.560
		SUBTOTAL	18.360

2 Port-Pseudo Dual 8K Logic Card (1) (Note 4)

Part Name & Type	Quantity (N)	$\lambda \times 10^{-6}$ (Note 2)	$N\lambda \times 10^{-6}$
Multi-Layer Board	1	0.593	0.593
Microcircuit (54LS04)	5	0.0610	0.305
Microcircuit (54LS00)	21	0.0526	1.105
Microcircuit (54LS10)	7	0.0467	0.327
Microcircuit (54LS20)	17	0.0409	0.695
Microcircuit (54LS74)	2	0.0606	0.121
Microcircuit (54LS298)	8	0.1165	0.932
Microcircuit (54H04)	17	0.0606	1.030
Microcircuit (54S04)	5	0.0606	0.303
Microcircuit (54S00)	3	0.0526	0.158

Table A-5 --- cont'd

2 Port-Pseudo Dual 8K Logic Card (1) (Note 4) --- cont'd

Microcircuit (54S10)	2	0.0467	0.093
Microcircuit (54S30)	4	0.0316	0.126
Microcircuit (54S74)	2	0.0606	0.121
Microcircuit (54S174)	2	0.1168	0.234
Microcircuit (54S64)	8	0.0564	0.451
Microcircuit (54S157)	4	0.0871	0.348
Microcircuit (Lamp Driver)	17	0.0526	0.894
Capacitor (CK)	18	0.0148	0.266
Connector (210 pin)	1	3.200	3.200
Oscillator (25 MHz)	1	0.9000	0.900
Switch (Rotary)	8	1.0000	8.000
Solder Connections	2052	0.00012	0.246
		SUBTOTAL	20.448
		TOTAL	99.158
		MTBF	10,085 hours

NOTES:

1. 51.6°C average part surface temperature and 45% electrical stress was used in calculations.

2. Failure rate per MIL-HDBK-217B unless otherwise noted.

3. Failure rate based on Ampex experience.

4. 23.5°C average part surface temperature and 30% electrical stress was used in calculations.

APPENDIX B

NMOS

APPENDIX B

NMOS MEMORY DEVICES

The NMOS (N-Channel Metallic Oxide Semiconductor) memory devices, offer the greatest bit density of any RAM (Random Access Memory) technology. This will remain true until toher technologies, such as I^2L (Integrated Injection Logic) are developed.

The two versions of the 4K NMOS RAMS that are available are the static and dynamic devices. The difference between the two types is based on the memory cell structure. The dynamic memory device employs a one transistor cell and a capacitor as its storage element. This capacitor will discharge over a period of time depending on its geometry and junction temperature thus requiring refreshing in order to maintain the stored data. The static memory device employs a six transistor cell, which functions in a similar manner to a flip-flop. Because the static cell latches the data instead of storing it as a charge on a capacitor, the static device is less temperature sensitive, needs no refreshing and no error correction for soft errors. Consequently, the static RAM requires a larger die area for its memory array and dissipates more power than does the dynamic RAM.

There are two static 4K NMOS RAMS currently available. Electronic Memories and Magnetics (EMM) has in production SEMI 4200 and AMD has the Am 9140 which differ significantly. The SEMI 4200 RAM was designed to be a pin for pin replacement for the standard 22 pin 4K dynamic NMOS RAM and requires three voltage forms, +12.0 volts, +5.0 volts and -5.0 volts. The Am 9140, also in a 22 pin package, has a different pin out and requires +5.0 volts only.

National Semiconductor has recently announced MM5257 4K static NMOS RAM in an 18 pin package requiring +5.0 volts. Intel has also announced a version of the 4K static RAM (2114), in an 18 pin package and the +5.0 volt power form. EMM is currently working on a second version of the 4K static RAM which will also be in an 18 pin package and require only +5.0 volts.

All of the 4K static NMOS RAMS are completely TTL compatible on the inputs and outputs with the exception of the EMM device, the present semi 4200, which has a high capacitance MOS input on the chip select pin and requires a +12 volt transition.

The only manufacturer that presently has a device available over the military temperature range (-55°C to +125°C) is AMD. The Am 9140 is available over both the commercial and military temperature range with four selected performance categories. EMM has indicated that the SEMI M4200 would be available over the military temperature in a few months, it is not available as such at this time. National Semiconductor and Intel will be announcing commercial temperature range 4K static RAMS only with the possibility of going to military temperature at some later date.

The 4K static NMOS RAM gives the user the capability of developing a high speed memory because of the fast access and cycle times available at the device level. The access time of the AMD device (Am 9140) is 300 nanoseconds and the cycle time 530 nanoseconds. These times reflect the worst case condition for the device over the full military temperature range and over the voltage range of +5.0 volts ± 10%. The EMM device has an access and cycle time of 225 nanoseconds and 400 nanoseconds respectively.

The power requirements for the AMD device must be handled differently from the EMM device because EMM's Semi 4200 has a reduced power requirement when not selected. The power requirement of the AMD device is constant whether or not the device is selected. The typical power of the AMD device is 250 milliwatts while that of the select EMM device is 432 milliwatts. The maximum power of both the AMD and EMM device is 600 milliwatts. The power dissipation of the EMM device when not selected is typically 25 milliwatts with a maximum dissipation of 60 milliwatts. Values given are at 25°C.

Back up batteries are required during power down for data retention. Secondary batteries are preferred over primary batteries in this application because of the extensive current requirement and the limited amount of space allocated to the batteries. Nickel-cadmium cells presently lead in cost-power trade-offs. Ni-cads have high current capabilities, are in volume production and can be charged and discharged several hundred cycles. Space within the NMOS memory system is such that a maximum of six "C" size can be installed and still leave sufficient space for efficient flow of cooling air. Calculations of data retentivity with batteries are shown below.

APPENDIX B

1. Dual 8K X 32 N-MOS memory utilizing AMD AM 91L40 BDM RAM memory device

   - Operating Voltage = +5V
   - Dual 8K X 32 Memory Dissipation = 54 Watts at +5V
   - Data Battery Retention Voltage = 1.5V + Diode drop = 1.5V + .8V = 2.3V supplied by 6 secondary (recharageable) cells internal to the memory WRA.
   - Data Rentention Power for 128 Memory Devices = 5.2 Watts at +1.5 Volts

   Battery Quantity = 6 "C" cells (Ni-Cad); vol/"C" cell = 1.249 in^3

   Watt HRS/in^3 for Ni-Cad = 1.2 to 1.5 Watt HRS (1.35 WH Average, from previous report)

   $$\text{Watt HRS/"C" Cell} = \frac{1.249\ in^3}{\text{"C" Cell}} \times \frac{1.35WH}{in^3} = \frac{1.69WH}{\text{Cell}}$$

   $$\text{Watt HRS/6 "C" Cells} = \frac{1.69WH}{\text{Cell}} \times 6\ \text{Cells} = \frac{10.14WH}{\text{6 "C" Cells}}$$

   The Data Retention Power for 128 Memory devices = 5.2 Watts

   The Power dissipation in the "or" diode = .8V X $(\frac{5.2W}{1.5V})$ = 2.7 Watts

   The total required Battery Power = 5.2W + 2.7W = 7.9 Watts at (1.5V + .8V = 2.3V).

   The time to discharge the 6 cells = $\frac{10.14WH}{7.9\ \text{Watts}}$ = 1.28 HRS ~ 1.3 HRS

2. Dual 8K X 32 N-MOS memory utilizing EMM SEM M4200 UMC RAM memory Device.

   - Operating Voltage = + 5 Volts (VRF), -5V (VSX)

     +12 Volts (VDD)
   - Dual 8K X 32 Memory Dissipation = 48 Watts operating 50% Duty Cycle

     Standby Dual 8K X 32 Memory Diss = 37W
   - VDD Battery Data Retention Voltage = (+4V) + Diode Drop

     = +4V + .8V = +4.8V
   - VSX Battery Data = (-4VO + Diode Drop)

     Retention Voltage

     = -4V + (-.8V) = -4.8 Volts

- Data Retention Power for 128 Memory Devices = 2.41W; VSX Data retention Power = $\frac{6MW}{Chip}$ X 128 CHIPS = .768 watts at -4 Volts

  VDD Retention Power = $\frac{12.8MW}{Chip}$ X 128 Chips = 1.64 Watts at +4 Volts.

Total data retention Power for 128 Devices = 1.64 + .768

= 2.41 watts

Battery Quantity = 6 "C" Cells (Ni-Cad)

Vol/"C" = 1.249 in^3

Watt HRS/in^3 for Ni-Cod = 1.2 to 1.5 Watt HRS (1.35WH Average - from previous report)

Watt HRS/"C" Cell = $\frac{1.249\ in^3}{"C"\ Cell} \quad \frac{X\ 1.35WH}{in^3} \quad = \frac{1.69WH}{Cell}$

Since the power ratio between the two batteries is $\frac{1.64W}{.768W}$ = 2.1:1 we will use 2 "C" cells for - 4.8V battery and 4 "C" Cells for + 4.8V battery.

The power dissipation in the - 4.8V "or" diode = .8V X $\frac{.768W}{(-4V)}$ = .154 Watts

The total required -4.8V Battery Power = .768W + .154W = .922 W

The time to discharge the two "C" cells bank =

$\frac{1.69WH}{"C"\ Cell} \quad \frac{2\ "C"\ Cells}{Bank} \quad \frac{1}{.922W}$ = 3.6 HRS/2 Cell Battery Bank

The power dissipation in the +4.8V "or" diode = .8V X $\frac{1.64W}{(+4V)}$ = .328W

The total required +4.8V Battery Power = 1.64W + .328W = 1.97 Watts

The time to discharge the 4 "C" Cell Bank =

$\frac{1.69WH}{"C"\ Cell} \quad \frac{4\ "C"\ Cells}{Bank} \quad \frac{1}{1.97}$ = 3.43 HRS

Thus the time to discharge the battery set is = 3.43 HRS

APPENDIX C

CMOS

APPENDIX C

CMOS MEMORY HYBRID

CMOS (Complimentary Metallic Oxide Semiconductor) memory devices offers the advantage to military systems of lowest standby and operating power, and the widest operation temperature of any RAM.

The greatest density available for CMOS RAMS is 1024 bits. Intersil and Harris both produce the IM6508 1KX1 RAM which is compatible with the industry's standard 93415 1KX1 bipolar RAM. The cell structure used is the standard 6 transistor cell used in most static memories.

The IM6508 requires a single +5.0 volt power supply for oepration. The device is specified from 4.5 volts to 5.5 volts although it will run from 4.0 volts to 7.0 volts. The maximum current requirement for the device is under 2 milliamps at 1 MHz operating rate. The stand-by current for the IM6508 is typically 10 namoamps at 3.0 volts which makes it ideal for battery back-up.

The IM6508 is specified over the full military temperature range ($-55^{\circ}C$ to $+125^{\circ}C$).

CMOS RAMS are capable of operating at moderate speeds over the voltage and temperature extremes. The IM6508 has a worse case access time of 460 nanoseconds and cycle time 730 nanoseconds. The exception to this case is the SOS (Silicon on Sapphire) CMOS RAM which is capable of access and cycle times under 100 nanoseconds. The major disadvantage to SOS CMOS RAMS is their relatively high leakage currents.

Most military applications require memories with extreme densities. The 1K semiconductor device is not capable of offering a very dense memory. This can be overcome by hybridizing the 1K CMOS RAM (LPN 8391149 Spec enclosed).

The organization of the hybrid memory is "Dual 4K x 3" bits. This permits the hybrid to be used as either a 4K x 6 bit memory or an 8K x 3 bit memory.

Low-power Schottky devices are used to buffer all inputs to the hybrid and decode the two most significant address bits for an internal chip select signal. The low fan in (.36 ma) of the low power Schottky devices allow one high speed Schottky device to drive over 12 Hybrids or 8K x 32 bits of memory.

The access and cycle time of the hybrid is 510 and 840 nanoseconds respectively which relflect the worse case condition of temperature (-55°C to +125°C) and voltage (4.5 Volts to 5.5 Volts).

The hybrid requires a single +5.0 volts for normal operation and +3.0 volts for stand-by when powered down. The typical power requirement from the +5.0 volt supply is 210 milliwatts and the maximum is 405 milliwatts. The hybrid has been configured internally with two separate power forms to minimize the data retention current. The only devices on one power form are the CMOS RAMS and pull-up resistors associated with the write enable signal and the chip select signal. The typical leakage current required to maintain stored data is 240 nanoamps with a maximum of 2.4 microamps.

The hybrid package has the dimensions 1.3 inches by 1.8 inches. Two rows of pins are located on the bottom, each row containing 17 pins. The pins are on 100 Mil centers and are mounted on a card in a similar manner as I.C.'s. The hybrid is soldered on the card and not welded.

The data retention mode is implemented by isolating the power for the CMOS RAMS from the rest of the logic. The CMOS hybrids have a maximum current requirement of 2.4 ua per hybrid at 65°C. Normally during power down the temperature will be lower than 65°C in which case the current requirement will decrease. Eleven hybrids will be on each memory card and there are two memory cards. The total current requirement is 52.8 microamps. Calculation for data retentivity using Lithium batteries is as follows:

1. Dual 8K x 32 C-MOS memory utilizing Intersil IM 6508 (Special) Ram memory Device. Twenty-Four of these memory chips are mounted in a package to form a Dual 4K x 3 Hybrid memory Device.

- Operating Voltage = +5V
- Dual 8K x 32 Memory Dissipation = 27 Watts at +5V
- Battery Data retention voltage = 2.2V + Diode Drop = 2.2V + .8 = 3 Volts supplied by two Lithium primary (non-rechargeable) "AA" size cells mounted internally in the WRA.
- Data retention power = $\frac{.1 \text{ Microamp}}{\text{Chip}}$ X 528 Chips x 2.2V (for 22 Hybrids (528 Chips))

  = .116 Milliwatts

  Battery Quantity = 2 "AA" Cells (Lithium) • $\frac{\text{Volume}}{\text{"AA" Cell}} = \frac{.415 \text{ in}^3}{\text{Cell}}$

  $\frac{\text{Watt Hours}}{\text{in}^3}$ for Lithium = 8 - 15 (11.5 average)

  $2 \frac{\text{Watt Hours}}{\text{"AA" Cell}} = \frac{.415 \text{ in}^3}{\text{"AA" Cell}} X \frac{11.5 \text{ Watt HRS}}{\text{in}^3} X \text{ 2 Cells} = 9.54 \text{ Watt HRS}$

  The Data Retention Power for 528 chips RAM chips (contained in 22 Hybrids)

  = .116 Milliwatts

  The Power dissipation in the "or" Diode = .8V X $\left(\frac{.116 \text{ MW}}{2.2\text{V}}\right)$ = .042 Milliwatts

  The total required Battery Power = .116MW + .042MW = .158 Milliwatts at 3 Volts (2.2V + .8V)

  The time to discharge the 2 "AA" Cells = $\frac{9.54 \text{ Watt HRS}}{.000158 \text{ Watt}}$

  = 60,379 HRS or 6.8 years based upon 8760 HRS/Year

APPENDIX D

THERMAL ANALYSIS

THERMAL ANALYSIS

During normal aircraft operation the air flow into the computer programmer cabinet is 13.5 pounds per minute at $46^{\circ}F$ ($7.7^{\circ}C$), and is used as the basis for the thermal analysis for the dual 8K core that follows.

This 13.5 pounds per minute is divided into four channels as shown in figure D-3. A mix of new 16K and existing 8K memory modules is also shown. For the E-2C cabinet configuration, the following will be assumed:

(a) Six new 16K memories and four existing 8K memories will be used in the positions shown in figure D-3.

(b) The memory and power supply assemblies are ported as previously described.

(c) The equivalent port size is $\frac{1}{4}$ x 7.00 inches (.021 x .583 Feet).

(d) Channel #3 with a flow rate of 2.7 #/min at $46^{\circ}F$ will be used. Twenty percent (20%) leakage from the cabinet will also be assumed to give a flow rate W of 2.2 #/min at $46^{\circ}F$ (132 #/hr at $46^{\circ}F$), after air entry.

(e) No heat is absorbed from the environment and no heat is lost to the environment.

(f) Air temperature at the output of the memory-power supply compartment will be the temperature to which heat is transferred to.

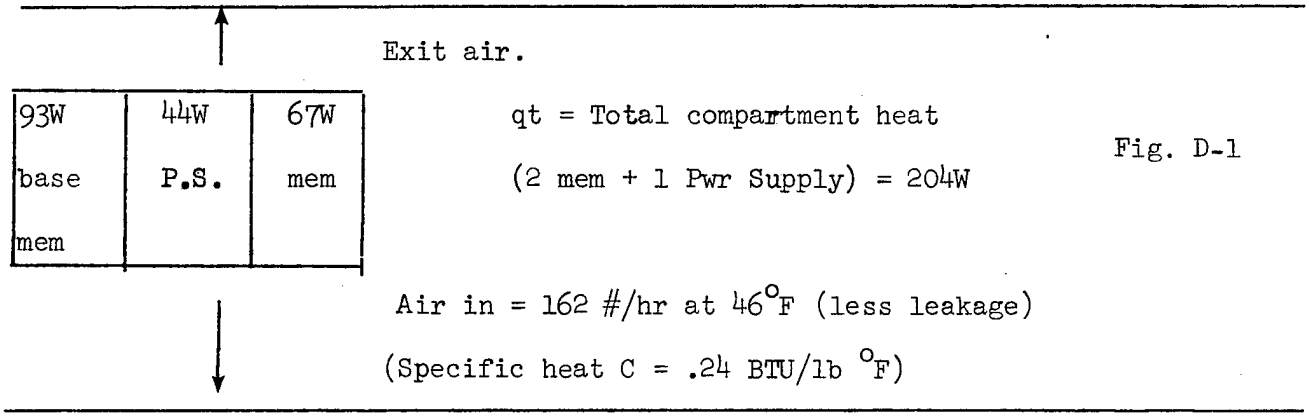


Fig. D-1

$$T_{out} = \frac{qt\ (3.41\ BTU/hr)}{Flow\ (C)} + T_{in}$$

$$T_{out} = \frac{qt\ watts\ (3.41\ BTU/hr)}{162\ \#/hr\ (.24\ BTU/lb^{\circ}F)} + 46^{\circ}F$$

$$= .088\ qt + 46^{\circ}F$$

$$= .088\ (204) + 46^{\circ}F = 64^{\circ}F$$

Properties of air at $64^{\circ}F$

(a) Specific heat C = .24 BTU/lb$^{\circ}$F

(b) Density P = .076 lb/ft^3

(c) Thermal conductivity k = .015 BTU/Hr-Ft-$^{\circ}$F

(d) Viscosity U = .043 lb/ft-Hr

For the dual 8K memory there are 8 flow channels per compartment (with 2 per each memory assembly. Therefore - $W_s = \frac{132\ \#/hr}{8} = 16.5\ \#/hr$ per port, including 20% leakage.

The value of the Reynolds number will determine the type of flow, i.e. laminar or turbulent.

$$Re = \frac{4W_s}{U\ (Perimeter)} = \frac{4\ (16.5)}{.043\ (2)\ (.583 + .021)} = 1270$$

The Reynodls number indicates laminar flow.

The film coeficient h for laminar flow is:

$$h = .38\ \frac{K}{b}\ \sqrt[3]{1 + .20\ \frac{Ws\ b}{x\ y}}$$

$$h = 3.8\ \frac{.015}{.021}\ \sqrt[3]{1 + .20\ \frac{(.021)}{80\ (.583)}}$$

$$= 2.7\ \sqrt[3]{1 + .009\ W_s}$$

y = Length of port = $\frac{7}{12}$ = .583 ft

b = Width of port = $\frac{.25}{12}$ = .021 ft

x = Height of port = $\frac{9.6}{12}$ = .80 ft

When W_s = 16.5 #/hr, h = 2.84

The base memory will dissipate more power as shown in figure D-2 and will be used to calculate the card surface temperature.

Mem	Logic	Logic	Base
27.3	6.1	6.1	mem
			53.9

$$T\ surface = T\ out + \frac{qc}{h\ A_c}$$

q Logic = 12.2 watts

q mem. = 54 watts

Ac = (2 sides) X (area of one side)

Fig. D-2 Memory Assy Power Distribution

$$T_{surface\ (Logic)} = 64^{\circ}F + \frac{12.2\ (3.41)\ (144)}{2.84\ (2)\ (9.2)\ (7)}$$

$$= 64^{\circ}F + 16.37^{\circ}F = 80.37^{\circ}F$$

$$= 27^{\circ}C$$

$$T_{surface\ (Memory)} = 64^{\circ}F + \frac{54\ (3.41)\ (144)}{2.84\ (2)\ (9.7)\ (6.5)}$$

$$= 64^{\circ}F + 75^{\circ}F = 139^{\circ}F$$

$$= 59.2^{\circ}C$$

In a similar manner, card surface temperature can be calculated for the 16K core memory, the dual 8K N-MOS and the dual 8K C-MOS semi-conductor memories. The table that follows list the results.

Thermal Summary TABLE D-1

Technology & Card	Dissipated Power (Watts)	Card Surface Temp.
Dual 8K Mem.	27.3, 53.9 (base)	59.2
Logic	6.1 each	27
16K Mem.	44.6 each	51.6
Logic	4.0 each	23.5
N-MOS AM91L40 Mem.	19.8 eacn	31.8
Logic	7.3 each	21.9
C-MOS Mem.	3.7 each	14.8
Logic	9.3 each	19.6
N-MOS Mem. (M4200 UMC)	17.5 each	29°C
Logic	6.5 each	19.5°C

The surface temperature defined in the preliminary report were based upon an assumed mechanical configuration and power dissipations originally supplied by memory suppliers, and are different from the temperatures noted in the above thermal survey.

The memory assembly was assumed to be totally enclosed and allowed for air passage around the outside of the memory assembly only. Since then, detailed layouts were made. Porting of the assembly allowing for air passage thru as well as around the assembly was accomplished. This greatly increased the thermal efficiency of the system lowering all temperatures.

Power dissipations were also adjusted and also contributed to a difference in surface temperatures.

The following table compares final and preliminary predictions.

Table D-2

Memory Technology	Final Prediction Pwr. disip.	card temp°C	Preliminary Prediction Power disip.	Avg. temp.°C
8K core mem	93.4 W	59.2°	112W	83°
Logic		27°		
16K core Mem.	97.2W	51.6°	56W	38°
Logic		23.5°		
N-MOS Mem.	54.4W	31.8	37.4W	34°
Logic		21.9		
C-MOS Mem.	26.6W	14.8°	21.3W	32°
Logic		21.9		

The final report predicts surface temperatures for each type of circuit card within the memory assembly. The preliminary report predicted the total average surface temperature within the assembly.

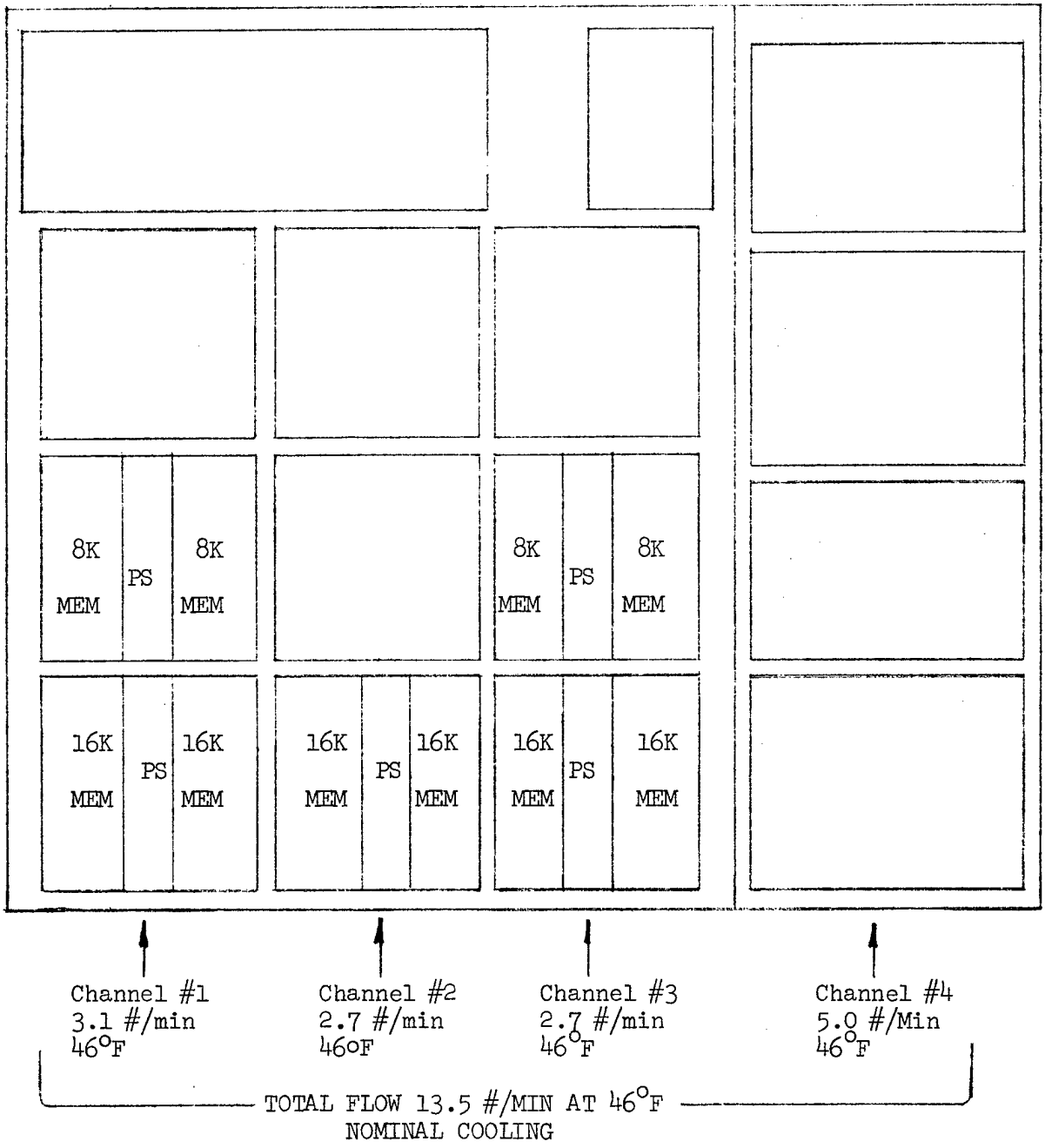

8K MEM
PS
8K MEM
8K MEM
PS
8K MEM
16K MEM
PS
16K MEM
16K MEM
PS
16K MEM
16K MEM
PS
16K MEM
Channel #1
3.1 #/min
46°F
Channel #2
2.7 #/min
46°F
Channel #3
2.7 #/min
46°F
Channel #4
5.0 #/Min
46°F
TOTAL FLOW 13.5 #/MIN AT 46°F
NOMINAL COOLING

Figure D-3

APPENDIX E

POWER SUPPLY

APPENDIX E

MEMORY POWER SUPPLY

POWER SUPPLY DESIGN

Due to the low output voltage (+5V) and high current requirements associated with each of the four proposed memory units, the existing switching regulator approach that has been reliably used in the E2 system for several years is preferred. This approach yields the high efficiency which is especially desirable at low voltage and high current power forms.

After a thorough review of the power requirements in conjunction with the two types of prime power that are available to drive the proposed power supply, the most feasible design and also cost-effective approach is to use, at most, two of the three AC/DC converter output voltages to drive the proposed power supply.

The AC/DC DC outputs are:

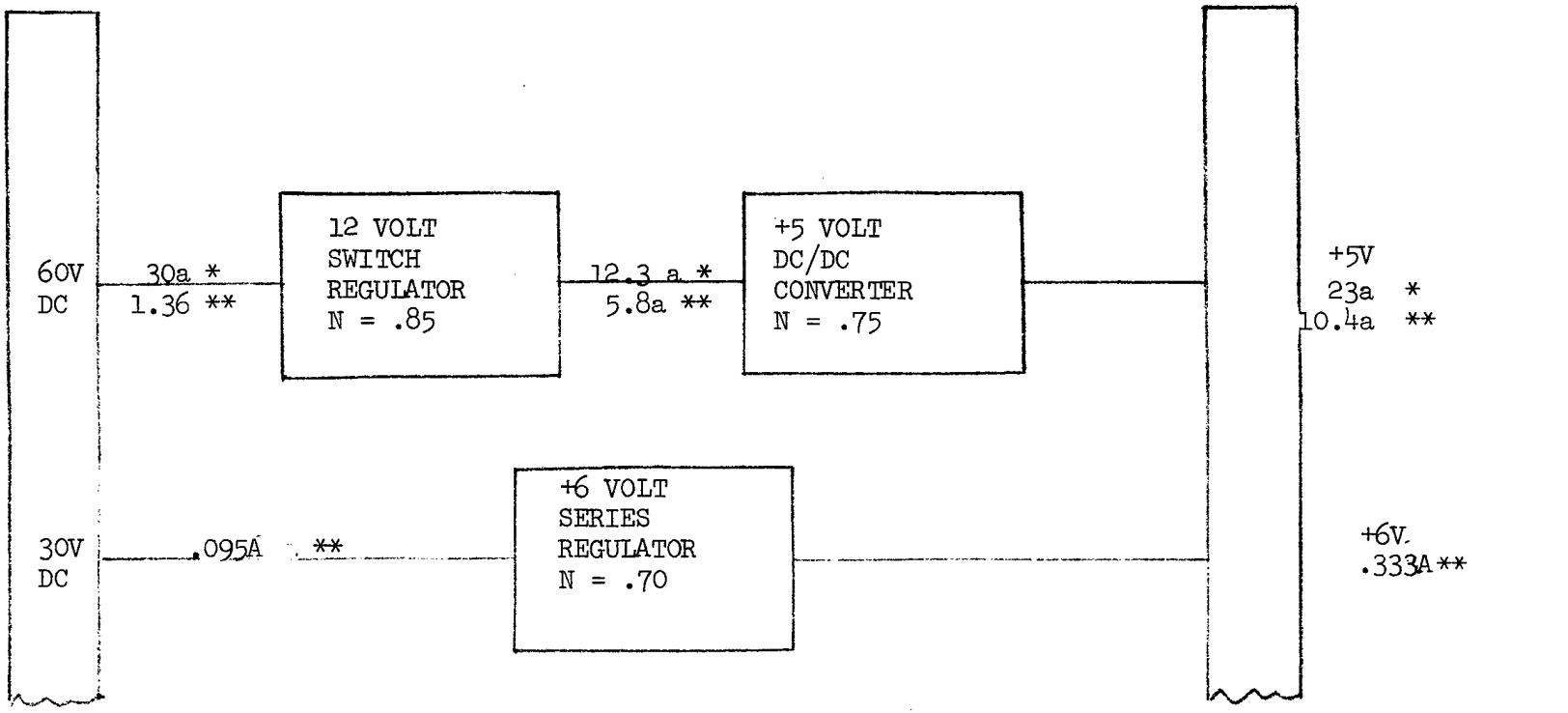
1.	+30 VDC at 4.2 amps	VA = 126.00
2.	-12.5 VDC at 3.1 amps	VA = 38.75
3.	60 VDC (Floating) at 7.4 amps	VA = 444.00
	TOTAL	VA = 608.75

MOS MEMORY POWER SUPPLY

The approach for both the NMOS and CMOS power supply designs will be identical, since the output voltage requirements are identical. The only areas where the two supplies will differ is in the type of power transistor that is required for the two applications, and the addition of a +6 Vdc low current series regulator for the CMOS design. The CMOS Memory requires 10.4 amperes at +5 Vdc and .333A at +6V, whereas, the NMOS Memory requires 23 amperes at +5 Vdc. Thus, lower power transistors and associated output filter capacitores will be used in the CMOS applications.

Only the 60 Vdc (floating) output voltage from the 546141 AC/DC converter will serve as the prime power input to the NMOS version of the MOS Memory Power Supply (MMPS). Both 60 Vdc and 30 Vdc will be used for the CMOS version of the MMPS.

The MMPS, as shown in Figure E-1, is not only the most cost-effective approach, but yields the highest efficiency and thus reducing the internal dissipation in the MMPS.



	POWER IN (WATTS), PIN		POWER OUT, (WATTS), P OUT		EFFICIENCY, P OUT/ PIN
	60V	30V	+5V	+6V	
* NMOS	180		115		64%
** CMOS	81.6	2.86	52	2W	64%

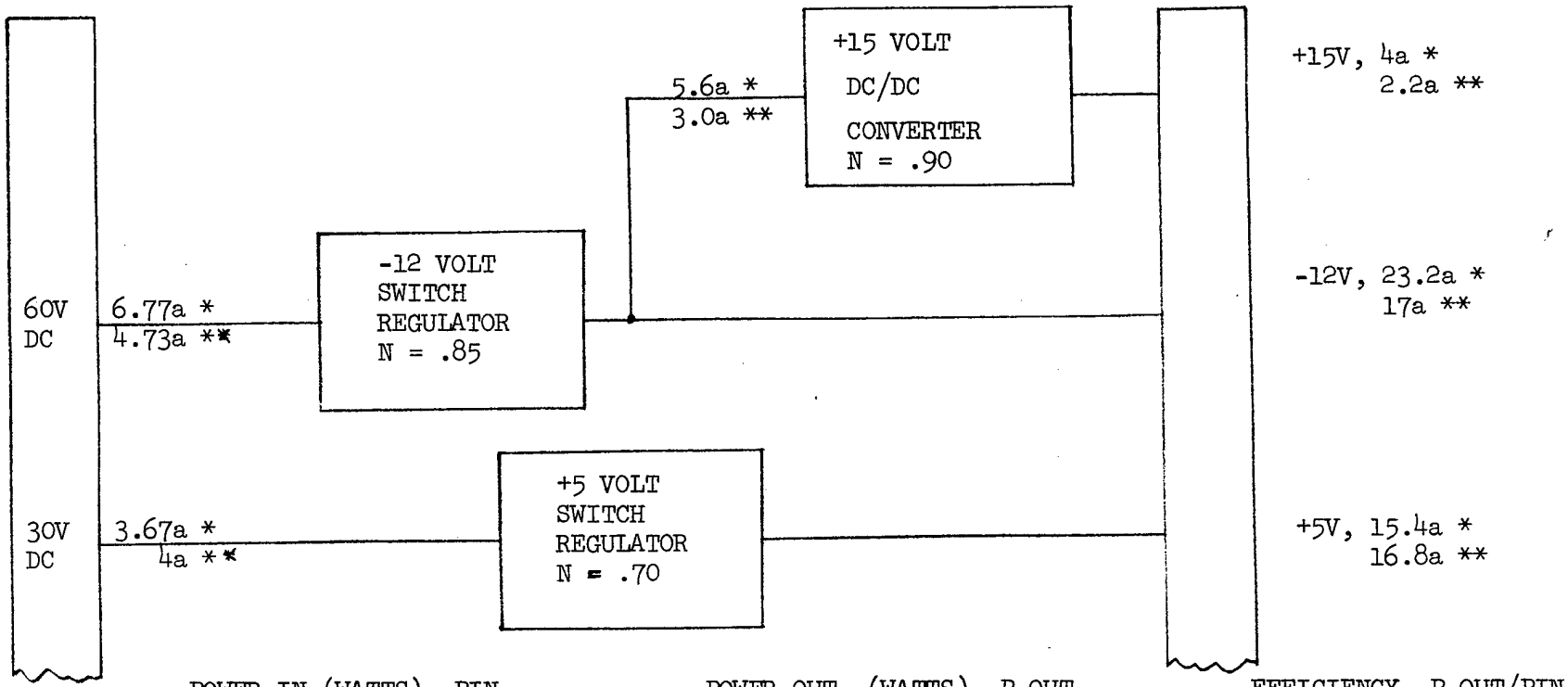
FIGURE E-1, MOS MEMORY POWER SUPPLY

CORE MEMORY POWER SUPPLY

Power dissipation in the Core Memory Unit depends on temperature, operating rate, and data pattern. The worst case power supply requirement is at -55°C, 800 nanosecond cycle rate with an all zero data pattern. Two of the four 8K x 32 core memories that the power supply services are assumed to be operating, as stated above, and two 8K x 32 core memories, are assumed to be at standby for the power supply design requirement.

The preferred power supply design approach for both the 16K and 8K core memories will use only the +30V and the floating 60V from the 546141 AC/DC converter as inputs to the proposed power supply.

The approach depicted in Figure E-2 yields the best efficiency and cost-effective combination. This same approach will be used for both CORE memory applications as the output voltages are identical and the current value associated with each output voltage is very similar. The -5V power form, as required by the Ampex memory modules, is derived internally from the -12V input.



	POWER IN (WATTS), PIN		POWER OUT, (WATTS), P OUT			EFFICIENCY, P OUT/PIN
	60V	30V	+15V	-12V	+5V	
* 16K CORE P.S.	406	110	60	278	77	80.5%
** DUAL 8K CORE P.S.	283.5	120	33	204	84	79.7%

FIGURE E-2, CORE MEMORY POWER SUPPLY

APPENDIX F

PRELIMINARY LABORTORY TESTS FOR COMPUTER PROGRAMMER 16K MEMORY STUDY

APPENDIX F

PRELIMINARY LABORTORY TESTS FOR COMPUTER PROGRAMMER 16K MEMORY STUDY

PURPOSE OF TEST

GAC's proposal for the new 16K memory has consistently addressed the desirability of having two independent addressable 8K memories in an L304F 8K memory form factor. One reason for this selection was to maximize the real time saved per scan. It was felt that the lost real time due to a processor waiting for servicing was the key factor. The test was designed to determine the number of times in a ten second interval the two processors simultaneously accessed selected pairs of memories.

CONDUCT OF THE TEST

Eight 8K memories were wired so that the outputs from the Bank Address Comparator were brought to external two-input "AND" gates. Four were A processor comparators and four were B processor comparators and each "AND" gate was wired with one A and one B comparator. The outputs of each "AND" gate triggered a counter (See Figure 1.) The result of this setup was to count the number of times the processors were simultaneously requesting service from a pair of 8K memories. A tactical situation was setup using tape N24 with the following conditions:

Type of Tracks	No. of Tracks
Radar/IFF	276
Geographic Points	38
PDS	149
Link 11	135
Link 4	73
Link 4 (outgoing)	32

RESULTS OF THE TEST

The 8K memories were paired in combinations based on an estimate of processor usage presented in Table 1. Three combinations of memory pairing were tested at maximum loading of the program. These readings are presented in Table 2 and show a maximum, minimum and average number of simultaneous requests for the 8 memory configuration during fiteen ten-second time samples.

In calculating the total processor wait time, it was estimated that:

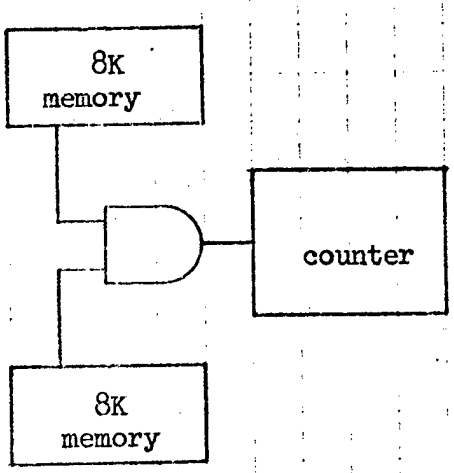
1. The duration of the bank address signal with the new fast 16K memory will be approximately one half of the present 8K memory reducing the number of simultaneous requests by a factor of two.
2. The average processor wait time for the present 8K memory is approximately 600 nanoseconds considering the acknowledge response in the four modes of operation. Based on this, we estimate the average acknowledge response for a fast 16K memory at 300 nanoseconds.

Table 2 is the compilation of the expected real time loss for the noted combination of 8K memory addresses. The loss of porcessor real time due to a 16K module should be weighed against the expected real time gain of 4.5 seconds per scan when a fast memory is utilized.

The estimate of time improvement per scan for the fast 16K memory is an approximation only but should be the same for either solid state or core Technology while operating at the present processor clock rate of 4.8 Mhz.

It should be noted that this test was run to achieve a "ball park" number. If so desired, more detailed tests and/or analyses should be performed to confirm our initial results.

A. PROCESSOR BANK ADDRESS COMPARATOR



B. PROCESSOR BANK ADDRESS COMPARATORS

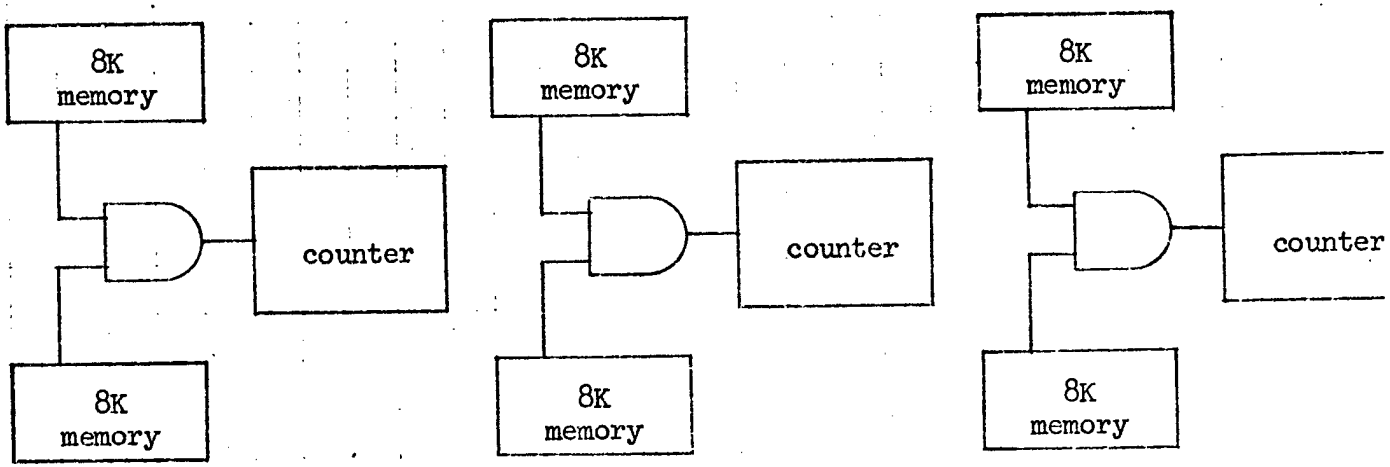


Figure 1

TABLE 1

DUAL ACCESS STUDY

MODULE	%A	%B	NOTES & CONDITIONS
1	98%	2%	SCRAM/EXEC & DISPLAY - ALL A
2	100%	0%	DISPLAY ONLY
3	80%	20%	DISPLAY AND INTERCEPT FILE ON A-FILE CONTROL ON A/B. INCREASE B ACTIVITY WITH MORE LINK 4
4	20%	80%	TRACK INPUT PROCESSING ON B & NAV ON A
5	30%	70%	ASSOC/CORR & TRACKING ON B. EXEC A/B, IFPM B, NAV A
6	50%	50%	TRACK FILE & OTHER MISC UNIVERSAL FILES
7	60%	40%	PDS ON A, TRACKING FILE ON B
8	30%	70%	LINK 4/11 ON B VECTORING ON A

TABLE 2

SIMULATED 16K MEMORY TEST

MEMORY PAIRS CPU-A	MEMORY PAIRS CPU-B		NO. OF SIMULTANEOUS REQUESTS PER SCAN (10 SEC.) FOR 8K PAIRS	PRORATED EXPECTED SIMULTANEOUS REQUESTS PER SCAN FOR 16K MEMORY	ESTIMATED TIME LOSS PER SCAN FOR 16K MEMORY
3	7				
4	5	MAX	71,568	35,784	10.7 m sec
6	8	MIN	47,917	23,958	7.1
2	1	AVE	55,194	27,597	8.2
7	3				
5	4	MAX	52,988	26,494	7.9
8	6	MIN	33,512	16,756	5.0
1	2	AVE	48,235	24,117	7.2
4	3				
8	7	MAX	37,246	18,623	5.5
5	6	MIN	18,709	9,354	2.8
1	2	AVE	26,310	13,155	3.9