Abstracts

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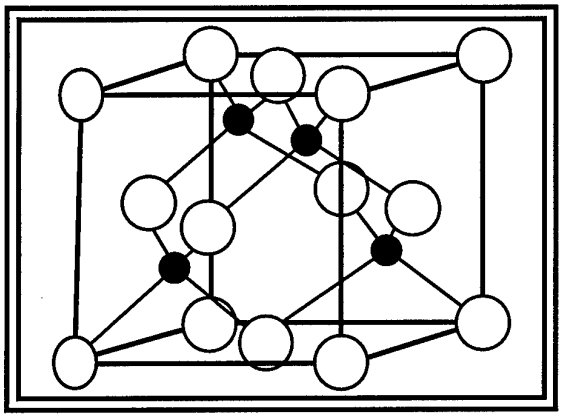

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September 2 - 4, 1998 - Montpellier, France

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Université Montpellier II , FRANCE

Centre National de la Recherche Scientifique

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Montpellier - France
2 - 4 september, 1998

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INTRODUCTORY TALKS

PROGRESS IN SiC: FROM MATERIAL GROWTH TO COMMERCIAL DEVICE DEVELOPMENT

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Silicon carbide technology has made tremendous strides in the last several years, with a variety of encouraging device and circuit demonstrations in addition to volume production of nitride-based blue LEDs being fabricated on SiC substrates. The commercial availability of relatively large, high quality wafers of the 6H and 4H polytypes of SiC for device development has facilitated these exciting breakthroughs in laboratories throughout the world. These have occurred in numerous application areas, including high power devices, short wavelength optoelectronic devices, and high power/high frequency devices. This paper will describe progress made in increasing the quality and size of SiC wafers, advances in SiC epitaxy and some of the resulting device demonstrations and commercialization by Cree Research.

To meet the challenges required for commercialization of SiC semiconductors, we have made specific efforts towards larger diameter high quality substrates which have led to production of 50 mm diameter 4H and 6H wafers for fabrication of LEDs and the demonstration of 75 mm wafers. Despite the growing interest in SiC, the micropipe defects that occur to a varying extent in all wafers produced to date are seen by many as preventing the commercialization of many types of SiC devices, especially high current power devices. Although several mechanisms, or combinations of mechanisms, cause micropipes in SiC boules grown by the seeded sublimation method, results at Cree have allowed us to reduce micropipe densities by over an order of magnitude. The continuing improvement of our wafers and the production of wafers with micropipe densities of less than 1 cm^{-2} (with 1 cm^2 areas void of micropipes), indicate that micropipes will be reduced to a level that makes high current devices viable and that these defects may be totally eliminated in the next few years. Figure 1 shows a digitized image of a KOH etched 35 mm 4H-SiC wafer from a low micropipe density 4H-SiC boule. This wafer contains a total of 7 micropipes, yielding a density of 0.7 cm^{-2}.

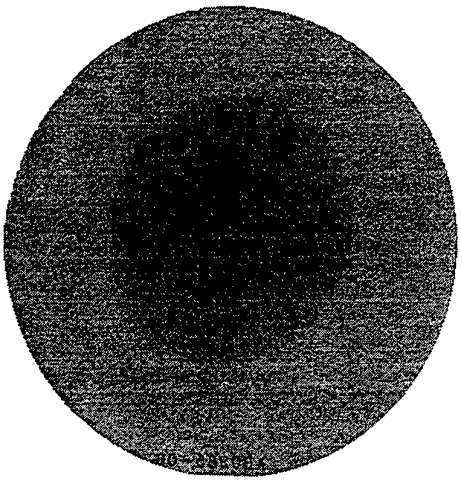

Figure 1: Digitized image of 35 mm etched 4H-SiC wafer with total of 7 micropipes.

Thick, high quality 4H-SiC epilayers suitable for high power devices have been grown by CVD in a hot-wall reactor. Thicknesses in excess of 100 μm and n-type doping levels between 1×10^{14} cm^{-3} and 2×10^{19} cm^{-3} have been achieved. The recent improvements of the growth process have improved our thickness uniformity over a 50 mm wafer to less than 3% (Figure 2) and the doping uniformity to approximately 5%, both values expressed as σ/mean. The PL data from intrinsic films confirm the

high quality of the layers, showing strong free exciton luminescence and little or, typically, no contribution from unwanted impurities such as Al, B and Ti.

High voltage P-i-N diodes have been fabricated from hot-wall grown epitaxy using junction termination extension (JTE) edge termination. The highest breakdown voltage achieved for these diodes is >5.5 kV as shown in Figure 3, which is a new world record for blocking voltage for a SiC device. The diodes were fabricated using an epitaxial layer 85 mm thick which was doped ~5×10^{14} cm^{-3}. Since these diodes were fabricated with a ~3 kV optimized mask set, the achieved voltage is not as high as the capability of the epitaxial layers used to fabricate them. The on-state voltage drop of these diodes was about 5.4 V at a current density of 100 A/cm^2, which indicates that the carrier lifetime in the epitaxial layers is in excess of 1 msec, further demonstrating the quality of Cree's epitaxial growth process.

In the microwave device area, a SiC MESFET with 42 mm of gate periphery on a single die which had a maximum RF output power of 53 watts CW with 37% power-added efficiency (PAE) at 3.0 GHz has been demonstrated (Figure 4). This unprecedented power from a die with an area of only 3 mm^2 demonstrates the extremely high power handling capability of SiC microwave devices. Additionally, the SiC MESFET characteristics in Figure 5 showing 2.5 W/mm with 41% PAE at 8 GHz, demonstrate the utility of this technology at X-band. The MESFETs were fabricated on 35 mm diameter semi-insulating 4H-SiC substrates. The ability to yield devices with a gate periphery of 42 mm with breakdown voltages >100 V attests to the quality of the substrates and the uniformity of the SiC epitaxial layers

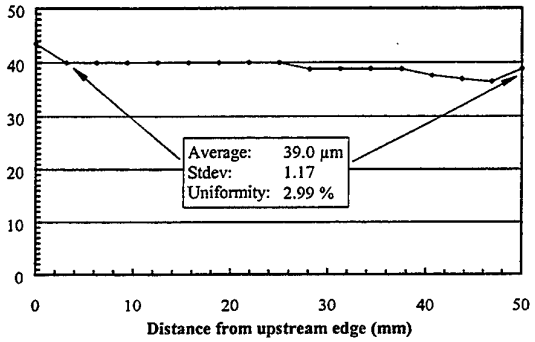

Figure 2: Thickness uniformity over 50 mm wafer grown in hot-wall CVD reactor.

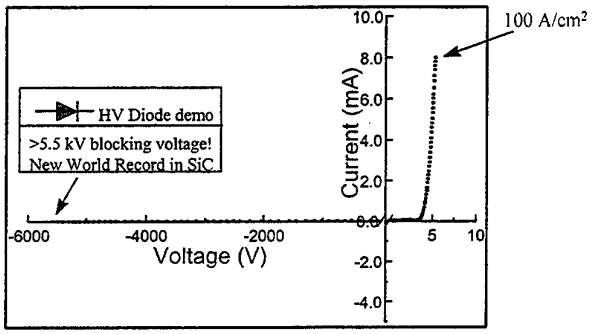

Figure 3: Measured characteristics of JTE terminated >5.5 kV P-i-N diode.

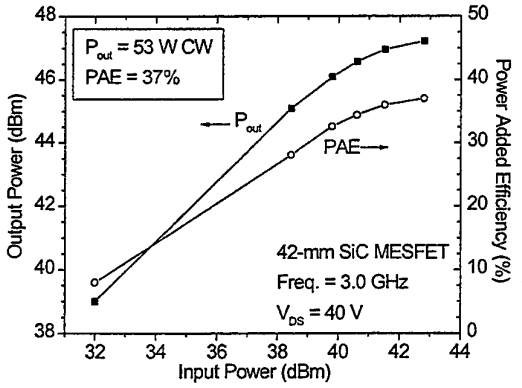

Figure 4: 3-GHz power sweep for a 42-mm SiC MESFET exhibiting 53 W CW at 37% PAE.

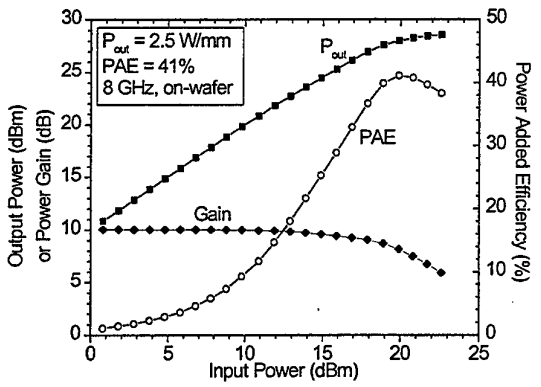

Figure 5: On-wafer power performance at 8 GHz for SiC MESFET with 0.45 × 250 mm gate.

Title "ADVANCES IN SIC MATERIALS AND DEVICES: AN INDUSTRIAL POINT OF VIEW"

Author(s) Siergiej, R. R., Clarke, R. C., Sriram, S., Agarwal, A. K., Bojko, R. J., Morse, A. W., Balakrishna, V., MacMillan, M. F., *Burk, A. A, Jr., and Brandt, C. D.

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Wide bandgap semiconducting materials are promising candidates for high-power, high-temperature, microwave devices because of their superior thermal and electrical properties in comparison to conventional semiconductors. Silicon Carbide is an emerging wide bandgap semiconductor which has proven itself especially well suited to high temperature power switching and high frequency power generation. In this work we examine recent advances in materials development and device performance.

In boule growth we have focused on increasing boule diameter and reducing defect counts. Two conductivity types have been developed consisting of undoped semi-insulating wafers for MESFETs and nitrogen doped highly conducting wafers for SITs and power switching devices. Crystals are produced by the physical vapor transport (PVT) technique in which growth proceeds by the sublimation of a SiC source upon a high-quality SiC seed in a high purity ambient (Figure 1)[1].

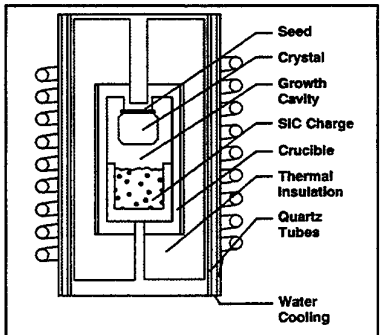

Figure 1. SiC physical vapor growth cavity (schematic).

The most successful methods for SiC device active layer fabrication have been vapor phase techniques. SiC epitaxial layer background doping densities less than $1x10^{14}$ cm^{-3} and n and p-type intentional doping from $1x10^{15}$ cm^{-3} to over $1x10^{19}$ cm^{-3} have been reported [2]. Very uniform, planetary multi-wafer epitaxial layer growth will be described, in which specular, epitaxial layers have been obtained with growth rates of 3-5 μm/hr and room temperature Hall mobilities of ~1000 cm^2/Vs.

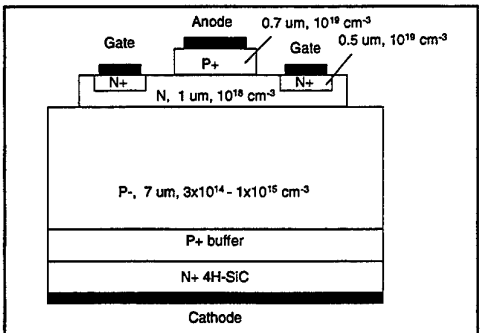

Figure 2. A schematic cross-section of the SiC asymmetrical GTO cell.

SiC finds application in high temperature power switching devices. We have investigated a hybrid MOS Turn-Off Thyristors (MTO™) technology utilizing a high power Gate Turn of Thyristor (GTO) shown in Figure 2 and a low power MOSFET. These power switches offer ease of turn-off, high temperature operation, and reduced cooling requirements.

In the fabrication of high power, high frequency transistors at UHF, L-band, S-band and X-Band, SiC has been found superior to both silicon and GaAs. The Static Induction Transistor (SIT) shows best performance for high peak power applications up to 4 GHz [3],[4],[5]. The SiC MESFET structure complements this performance for higher frequency operation through 10 GHz, and operates well under pulse or CW conditions.

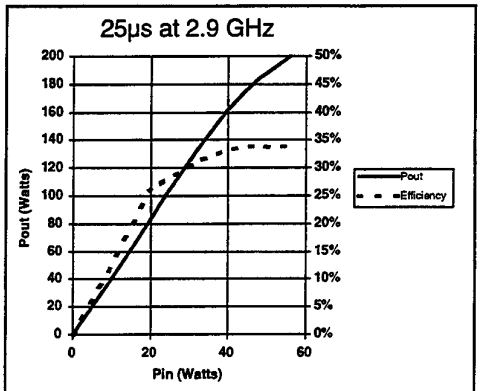

Figure 3. Short pulse operation of a 19 cell SIT.

SiC MESFETs with cut-off frequencies of 42 GHz and power densities as high as 3.3 W/mm at 10 GHz have been demonstrated [6]. The power density is more than six times higher than typically obtained with current GaAs MESFETs. Recently, over 6 Watts output power at X-band has been demonstrated with the SiC MESFET.

SiC SITs with 4 GHz cut-off frequencies have been developed from VHF through S-Band, exhibiting over four times the power density of silicon power transistors at S-band [7]. A 4H-SiC UHF television module utilizing SiC SITs has demonstrated good signal fidelity at the 2000 Watt PEP level and individual S-Band transistors have been tested over 200 Watts pulsed output power level (Figure 3).

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[3] R. R. Siergiej, R. C. Clarke, A. K. Agarwal, C. D. Brandt, A. A. Burk Jr., A. W. Morse, IEDM Tech. Digest, Washington D. C., 353 (1995)

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[5] R. R. Siergiej, R. C. Clarke, A. W. Morse, L. S. Chen, J. A. Ostop, R. R. Barron, C. D. Brandt, GOMAC (1997)

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BULK SiC GROWTH 1

STATE OF THE ART IN THE MODELLING OF SIC SUBLIMATION GROWTH

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During the last five years, significant progress has been made on the modelling of sublimation growth of silicon carbide single crystals [1-9]. The different computational tools have allowed to obtain further information to experimental knowledge. The need for such an effort was primarily motivated by a better control of the local temperature field inside the reactive cavity, an environment of strong thermal radiation in which the SiC boule growth process occurs. The computed temperature distribution can aid to qualitatively obtain the growth history in relation to process parameters and geometry. Global heat transfer phenomena were the most studied and must include conduction, convection, radiation and induction heating as well as heat of crystallisation and sublimation at the interfaces. Is was found that local temperature fluctuations over the seed can be one of the causes of defect formation as we have recently shown [10] (figure 1). Thermal data, mainly emissivity and conductivity of SiC source powder, single and poly-crystalline SiC are under study. Their accurate knowledge still remains a challenge. In addition, during the sublimation growth of crystals with significant length, the temperature distribution inside the cavity changes owing to an increase of crystal size, deposition on crucible walls and modifications of the volume, porosity and properties of the SiC powder. The simulation of only heat transfer does not allow directly the determination of the growth rate and the shape of the crystal. But, this first step has proved its efficiency for the optimization of the local temperature field and to provide material transport, predominantly to the seed by suppressing deposit formation [4].

Heat transfer must be coupled with gaseous species transport and reactivity. The highly coupled model must take into account the geometric modification of the cavity owing to crystal growth. Recent studies [2,5] have shown that local thermochemical equilibrium linked to heat and mass transfers can give the magnitude of the growth rate and the shape of the crystal at the beginning of the growth. Raback et al. [5], by using a virtual crystal growth model, showed that the shape of the growing ingot and the powder evolution are determined by the features of the temperature distribution. We have also shown that the feature of powder consumption and graphitization are directly linked to the global heat transfer. Karpov et al. [4] have proposed more advanced models on diffusion of silicon and carbon containing species in porous media. Egorov et al. [7] showed that at low temperature (< 2500 K) and subsequent low vapor

pressures, Stefan flow, i.e., velocity due to reaction rate, has to be taken into account. The flow velocities can be high enough to transport SiC particles of microscopic size from the source to the seed opposite to the gravitational force. An accurate modelling and simulation of the sublimation growth process needs a software taking into account highly coupled phenomena, fluid mechanics with Stefan flow, convective, conductive and radiative heat transfer, electromagnetic, multicomponent species transport, homogeneous and heterogeneous thermochemical equilibrium and finally accurate thermal and transport databases. Ideally the stress field in the growing crystal should be also computed to relate some of the features of defects formation to thermo-mechanics.

This modelling field is too young to propose such a code as a black box. We think that some parts of the modelling work have anyhow reached maturity like magnetic and thermal modelling coupled with simplified chemical models. We propose in this paper what kind of information can be routinely available by simulation, how to control defects formation and pave the routes to computer design of the growth process.

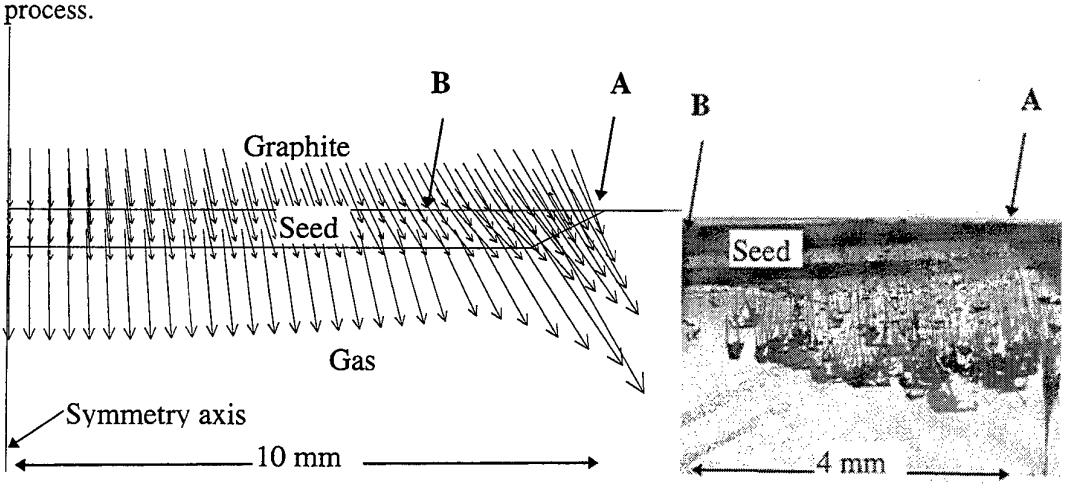

Figure 1 : Local thermal gradient near the seed-graphite interface at the beginning of the growth and associated macro-defects. The position of macro-defects is in the area of higher thermal gradients.

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MATHEMATICAL SIMULATION OF MASS TRANSFER, THERMAL TRANSFER, AND STRESS FORMATION UNDER SILICON CARBIDE BOULES GROWTH

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Silicon carbide is gaining more and more importance as a material for severe environments (high temperature, high radiation, chemical hazards etc.) electronics. Improvement of structural properties of SiC wafers is the key area of the SiC-based devices development. Mathematical simulation is an effective method of technology optimization. Last time modelization of SiC sublimation growth is being rapidly developed by different groups [1, 2 etc.]. The problems which are noted for currently produced SiC wafers are the presence of micropipes, dislocations and slightly misoriented (less than 1 degree) comparatively large areas in the silicon carbide boules. Stress formation under the crystal growth is one of the reasons of different defects commencement. The aim of the present work is to analyze heat- and mass-transfer, stress formation under SiC crystals sublimation growth under different growth conditions.

For better understanding of our experimental results mathematical simulation of the SiC bulk growth have been employed. Initial results on the simulation of heat and mass transfer under SiC crystal growth are presented in [3]. At this paper we present a detailed study. Mass- and thermal transfer under SiC crystal sublimation growth have been simulated. Heat transfer in the SiC sublimation growth reactor have been numerically analysed. Distribution of main gaseous components in the crucible have been calculated. Stress formation have been considered using these results. The simulation have been made for the growth of SiC crystals 20-50 mm in diameter, growth temperatures in the range 2170-2670 K and different gas phase compositions. Stress distribution in SiC crystal, distribution of Si/C ratio in the gas phase near to the growth front and radial distribution of the growth rate at the different stages of growth in vacuum and different inert gases (Ar and H_2) have been calculated on the base of this modeling and considered in the paper in details.

Stress is formed due to nonuniformity of temperature distribution in the growing crystal. Real dislocation structure of the SiC crystal is formed due to movement and multiplication of dislocations. One of the reasons of dislocations formation is glide caused by tangential stress. As it was shown in [4] 6H-SiC crystals can be plastically deformed via relatively modest resolved shear stresses on the basal plane even at temperatures as low as 550°C. The primary dislocations slip system in the 4H- and 6H-SiC crystals is (0001)<11 $\bar{2}$0>. So the average square tangential stress have been calculated.

Some results as an example of our numerical modeling of stress distribution in the SiC crystal are shown in fig. 1 a, b for 1" and 2" boules correspondingly. Line A is a center of the crystals, line I – graphite-crystal interface, r – crystal radius (r axis correspond to the growth front), z – crystal length. Maximal and minimal stress data in the legends are given in MPa with the constant difference between neighbouring stress lines from maximum to minimum value.

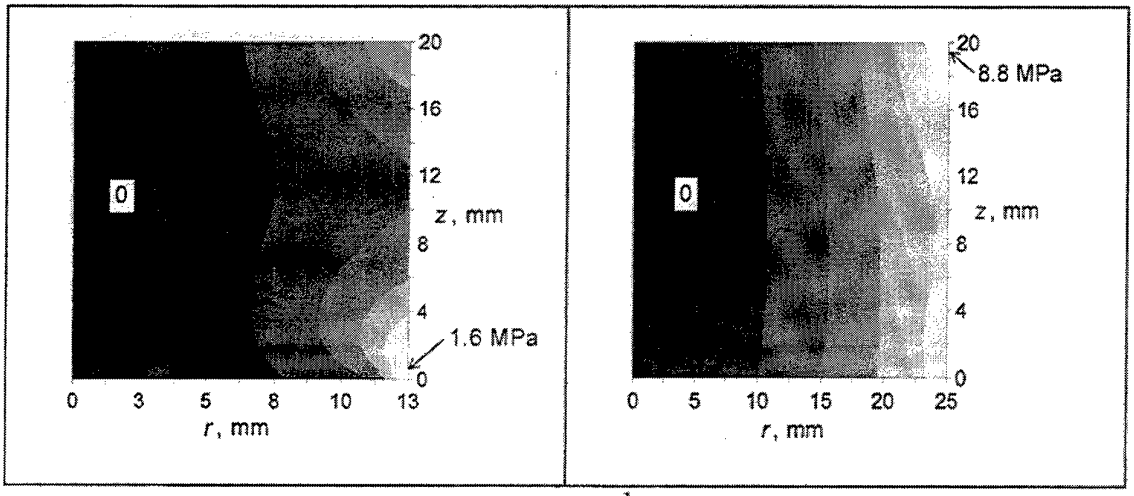

Fig. 1 a, b. Stress distribution in 1" and 2" in diameter crystals correspondingly.

Analysis of the numerical modelling results has shown that the stress values are increasing from the center to marginal parts of the crystal. The crystal diameter increase causes increase of the maximal values of stress as well as stress redistribution. For crystals with smaller diameter maximal stress is localized in the marginal areas of the growth front. For crystals with bigger diameters the maximal stress area is shifted to the crystal-substrate interface. Maximal values of stress decrease with increase of the crystal height. Localization of heat transfer in the center of the crucible (for instance using a hole in the part of the substrate holder) leads to the increase of the stress values and to the shift of the maximal value of stress to the substrate-crystal interface. Results of the theoretical study are in a good agreement with experimental results on defect formation (dislocations, stress) under different conditions of crystal growth.

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TRANSPORT PHENOMENA DURING SUBLIMATION GROWTH OF BULK SiC CRYSTALS

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Increasing of the species transport rate during sublimation growth of bulk SiC is necessary for successful use of this technique for mass production of high-quality SiC substrates. In the present paper results of modeling analysis are reported showing possible ways to increase the growth rate of SiC crystals.

The adequate model of SiC sublimation growth has been proposed in [1]. It includes the main specific features of the process -

- significant role of convection (Stephan flow) in the transport mechanism of reactive gaseous species,
- essentially multicomponent diffusion of the species in the vapor phase,
- influence of temperature on the total pressure in the growth chamber.

In addition, an exchange by the gaseous species between the growth chamber and the surrounding atmosphere (with controlled gas pressure and composition suitable for doping of the grown SiC crystal) is introduced into the model.

It is shown in Fig.1 that dilution degree of the main Si- and C-containing species depends remarkably on the pressure of inert gas (Ar) surrounding the growth container (the temperature dependence is important for dilution process as well). This can alter diffusion coefficients of the reactive species and, therefore, influence the growth rate of SiC. Lowering of the external inert gas pressure results also in enhancement of role of the convection in the species transport to the growth surface (see Fig.2). This fact can explain frequently observed in experiments transfer of solid particles from the source to the seed.

Drastic changes in the transport mechanism (Fig.4) are found in the "closed" growth system where initial vapor composition is conserved for a long time of the growth process. In this case growth rate can be significantly increased due to proper choice of initial vapor phase composition. The nearly "closed" system can be formed either by SiC coated container walls (under certain growth conditions) or by using tantalum container for SiC growth.

Our analysis shows that SiC growth rate up to several millimeters per hour can be reached by use the sublimation technique (Fig.3). The theoretical predictions are in reasonable agreement with available experimental data.

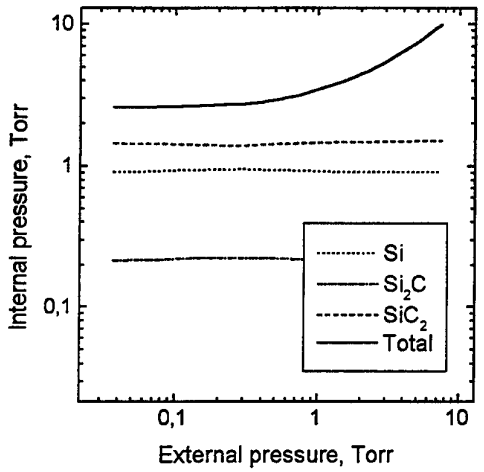

Fig 1. Species partial and total pessures inside the growth cell vs. external pressure

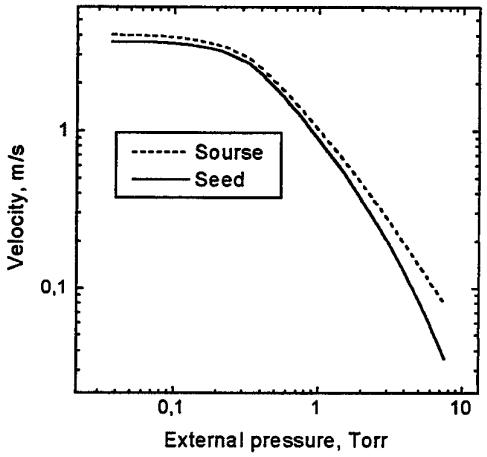

Fig 2. Flow velocity at the source and the seed vs. external pressure

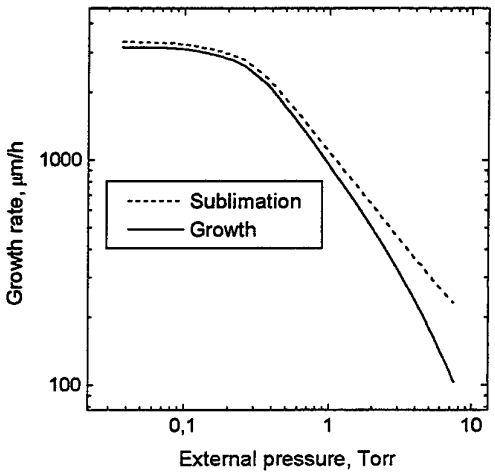

Fig 3. Sublimation and growth rates vs. external pressure

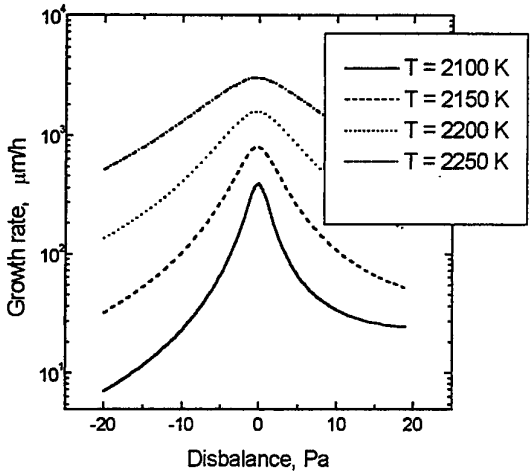

Fig. 4. Growth rate vs. disbalance at different seed temperaure (T)

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NEAR-THERMAL EQUILIBRIUM GROWTH OF SIC BY PHYSICAL VAPOR TRANSPORT

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Silicon carbide of various polytypes has been grown by using the modified Lely technique (physical vapor transport (PVT)). In contrast to former experiments [1,2] this paper deals with the SiC crystal growth at conditions where the growth chamber is close to thermal equilibrium during the entire growth process. Average thermal gradients between seed and source of less than 7.5 K/cm have been applied. Fig. 1 shows the temperature at the top (T_{seed}) and at the bottom (T_{source}) of the crucible as well as the argon pressure (p_{Ar}) inside the crucible as a function of time during a near-thermal equilibrium growth process; a sequence of different growth runs (denoted by step 1 to step 4) is displayed. Subsequent to each growth run the crucible was opened and the grown SiC crystal was characterized. Step 1 results in the annealing of all surface defects like polishing scratches and voids. A lateral SiC transport at the seed surface is observed resulting in a surface shape which corresponds to the radial temperature profile. Although no thermal gradient is applied during step 2 a significant transport (≈0.9 mm) from the source to the seed occurs within the first hour; then the transport stops. The adjustment of a thermal gradient ΔT = 5 K/cm at the beginning of step 3 raises the growth rate again up to about 0.1 mm/h; a further increase of ΔT to 7.5 K/cm and a simultaneous decrease of p_{Ar} to 5 mbar (step 4) results in a growth rate of 0.35 mm/h.
Using a 6H-SiC Lely platelet (without micropipes) as a seed crystal step 3 results in micropipe-free growth of 6H-SiC (on both the C- and Si-face) and at the beginning of step 4 a strong defect formation is observed (micropipe density > 200 cm^{-2}) [3]. We assume that the micropipes emerge from carbon-rich inclusions. These inclusions can be avoided if ΔT is not increased at the beginning of step 4. In this way, micropipe-free 6H-SiC bulk material can be grown with growth rates up to 0.27 mm/h.
The growth of 4H-SiC by a process as shown in Fig. 1 was conducted by using a 4H-SiC seed crystal (C-face) grown by PVT due to the lack of a 4H-SiC Lely platelet. Micropipes already incorporated in the PVT-seed crystal continued into the grown 4H-SiC layer. In addition, micropipes are generated close to the interface seed/grown crystal. This interface shows polytype fluctuations on a μm scale as observed by Raman spectroscopy. Fig. 2 displays the relative intensity of a 6H- and a 4H-TA-phonon mode (at about 148 cm^{-1} and 204 cm^{-1}, respectively) when scanning across the interface 4H-seed/4H-grown crystal. Both peaks appear simultaneously in a zone of about 10 μm, then the 4H-polytype stabilizes. Furthermore, the 4H Raman peak shifts by about 0.4 cm^{-1} in the region were the 6H-polytype occurs (not shown here). This shift may be due to internal stress at the interface acting as a source for micropipes.
Using 15R-SiC Lely platelets as seed crystals we succeeded in growing 15R bulk material by the near-thermal equilibrium process. However, the growth of 15R-SiC could not be stabilized for the entire boule. After a few millimeters, the polytype turned over to 6H- or 4H-SiC. The interface seed/grown

crystal showed polytype fluctuations (similar to Fig. 2) on a larger scale (50 - 100 μm) as characterized by optical microscopy. Micropipe generation is observed in the neighborhood of all these polytype transitions.

4H-, 6H- and 15R-samples grown by the near-thermal equilibrium process have been investigated by Hall effect measurements. The evaluation of the Hall effect data results in nitrogen donor concentrations and concentrations of the compensation in the range of 5.9×10^{17} cm^{-3} to 1.5×10^{18} cm^{-3} and 3×10^{17} cm^{-3} to 6×10^{17} cm^{-3}, respectively. The maximum of the electron Hall mobility is about 200 cm^2/Vs (6H-SiC) and 300 cm^2/Vs (4H- and 15R-SiC).

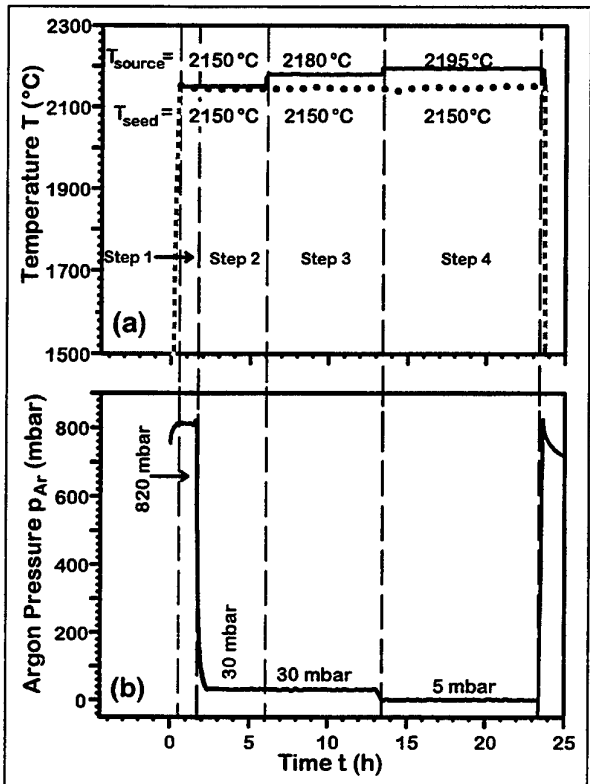

Fig. 1: (a) Temperature at the top (T_{seed}/dotted line) and at the bottom (T_{source}/solid line) of the crucible and (b) argon pressure p_{Ar} as a function of time during a near-thermal equilibrium process.

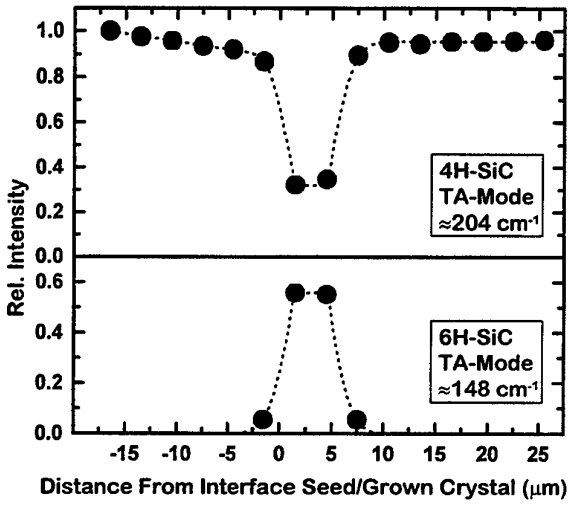

Fig. 2: Relative intensities of TA-modes of 4H- and 6H-SiC as a function of distance from the interface seed/grown crystal. Negative and positive values denote points in the seed and the grown crystal, respectively.

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ANALYSIS ON DEFECT GENERATION DURING THE SIC BULK GROWTH PROCESS

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The availiability of low defect, large diameter SiC substrate crystals represents a prerequisite for the further development of SiC-based power electronics, high temperature electronics and III-nitride optoelectronics and its commercialization. Despite the recent improvements concerning the reduction of micropipes and increase of crystal diameter SiC wafers still contain micropipes, high dislocation densities and inhomogeneities in doping and polytype. This status is partly due to the fact that aspects of the growth method by physical vapor transport are not fully understood. But there exist also deficiencies in the knowledge of defect formation mechanisms in SiC.

In this paper a systematic study on the defect generation in SiC bulk crystals in dependence of process conditions will be presented. Besides thermal boundary conditions we focussed our analysis on the impact of polytype and polarity of the seed, pumping rate and system pressure on crystal quality. The crystals have been prepared by the Modified Lely method. Special emphasis has been made to analyse the seeding process and the crystallization of subsequent layers. After growth the crystals have been sliced along the growth direction and polished to reveal the defect occurence in dependence of crystal length. Besides optical microscopy characterization techniques like scanning eelectron microscopy and Auger have been applied.
The 4H- and 6H-SiC crystals show depending on the polarity a different growth morphology. 2D island growth occurs on the Si-side. The C-side is characterized by anisotropic spiral growth. 4H material is found to have in general a lower defect density. Various defects, micropipes of different density 100 $cm^{-2} \leq 500\ cm^{-2}$, macropipes, inclusions attributed to C precipitates and Si droplets have been found. The micropipe formation is revealed to be closely related to the occurence of second phases and parasitic polytype formation. Although the seeding process was found to occur without defect formation in all crystals investigated, the generation of precipitates and micropipes appeared in subsequent crystalline layers. Micropipes present in the seed penetrate also into the bulk area of the crystal.
The results of occurence of second phases are discussed in respect to the onset of constitutional supercooling (CS) during the growth process. Models of different complexity are assumed. First the classical formulation of the CS criteria is applied which is predicting unstable growth behavior at process conditions when second phase formation is observed. In addition we present a model formulation addressing aspects of dynamical morphological stability including besides the concentration gradients of species and temperature distribution kinetic and capillar effects. With this approach growth stability is investigated in dependence of crystal length and compared to the experimental results of inclusion generation.

This work is supported by the Bavarian Research Foundation under contract 176/96.

BULK SiC GROWTH 2

PROSPECTS IN THE USE OF LIQUID PHASE TECHNIQUES FOR THE GROWTH OF BULK SILICON CARBIDE CRYSTALS

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At present the physical vapor transport technique (PVT) represents the standard method of research, development and production for the preparation of SiC bulk crystals as substrate material in respect to SiC and III-nitride based devices. Although significant progress has been achieved recently in defect reduction PVT grown crystals exhibit still a considerable number of defects, micropipes, dislocations and parasitic polytypes. Presently the SiC material system is the only area of commercially relevant materials processing where substrate crystals are grown from the vapor phase. The important semiconductors like Si, GaAs and InP are manufactured from the liquid. Because of the many years of experience strategies for defect reduction and diameter enlargement are much more developed than in sublimation growth.
Liquid phase techniques played a role in the earlier period of SiC development (1960-1975). Several groups tried to grow SiC bulk material from Si melt and other solutions e.g. Cr/Si. The published results must be considered as very unsatisfactorly and the liquid phase activities stopped in the mid 70´s.
Several issues have been regarded as critical for a successful development of SiC bulk growth techniques from the liquid:

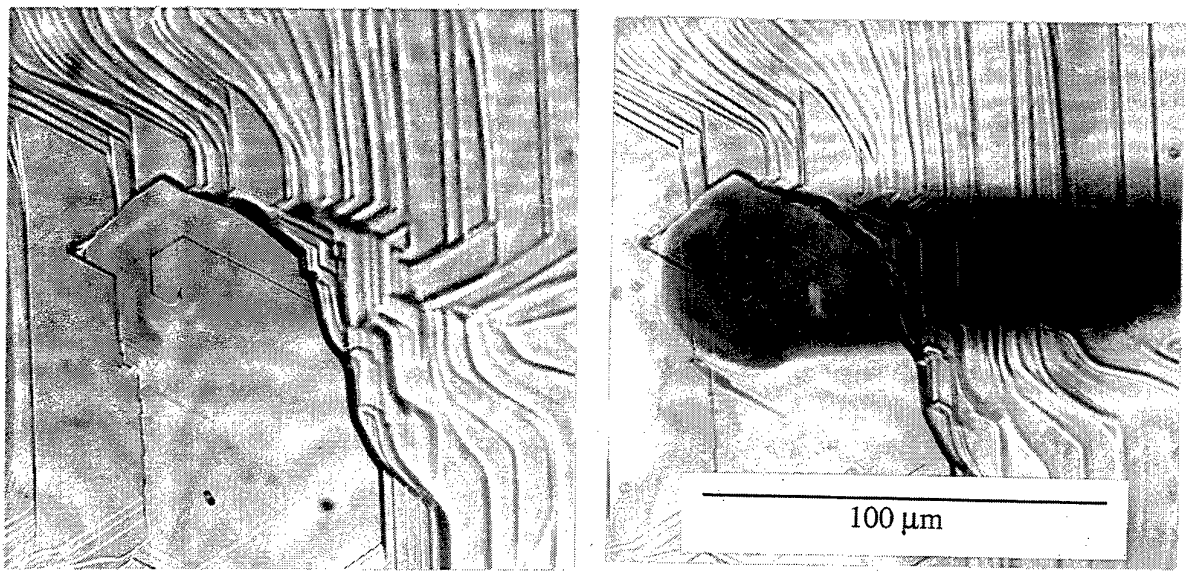
(i) Low solubility of SiC in Si limiting the growth rate
(ii) High vapor pressure of Si at increased growth temperatures T> 1800 °C
(iii) High solubility of metal solvents in the growing crystal
(iv) Increased complexity of growth apparatus at T> 1800 °C and high pressures
(v) Uncontrolled feeding of C containing species
(vi) Morphological instabilities due to lack of control measures
(vii) Deficiency of inert crucible material

In the last years a few research groups [1-3] restarted studies on SiC liquid phase crystallization oriented both for the preparation of epitaxial layers and growth of bulk crystals.

In this paper first the critical issues (i)-(vii) are discussed. Phase diagramms are analyzed and presented in terms of suitable temperatures and pressures for SiC liquid phase growth. The morphological stability of SiC solution growth is studied in detail. Different theoretical models with increasing complexity are applied with the aim to evaluate the maximum growth rate and crystal diameter for stable (inclusion free) SiC liquid phase crystallization. This analysis reveals the importance of active fluid flow control in the liquid.

Experimental results of SiC growth runs from the liquid phase are presented. The crystals have been analyzed by defect etching, x-ray diffraction, optical microscopy etc. Rocking curves show that the solution grown SiC layers exhibit a much better crystallinity than material grown from the vapor phase. A detailed defect analysis reveals that several micropipes present in the seed crystal (grown by PVT) are covered during liquid phase crystallization and do not penetrate the growing crystal (Fig. 1). Partly they end as screw dislocations. This mechanism of micopipe elimination also verified by other groups [1-2] is considered as a very important advantage of liquid phase crystallization as it can not be observed during SiC vapor growth.

Finally growth equipment for SiC liquid phase growth is discussed. Construction and control needs are addressed. As an example the performance of our high pressure (200 bar) and high temperature (≤ 2300 °C) apparatus for SiC solution growth is presented.



(a) (b)

Fig. 1 a) Liquid phase grown SiC observed in reflection light microscopy showing no micropipe.
b) The same region as in a) in transmission light showing a micropipe.

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SEEDED SUBLIMATION GROWTH OF 6H AND 4H-SiC CRYSTALS

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SiC can occur in many different crystallographic modifications but 4H and 6H polytypes are the most interesting from the device point of view. Since the quality of the epitaxial layers needed for device manufacturing depends on the quality of the substrate it is important to have SiC bulk crystals with low density of defects such as micropipes, domain boundaries and probably dislocations.

SiC sublimation growth is a complex process in which a number of parameters has to be controlled. The crystal growth is driven by the shift along a temperature gradient of the equilibrium between the solid SiC and its vapor. The vapor is produced via decomposition of SiC source material and reactions with the environment. The highest partial pressure is that of Si up to 2400°C. By changing the environment, whether graphite or TaC, one can change the system equilibrium from SiC-C to SiC-Si.

Here we present results of 6H and 4H-SiC crystal growth with seeded sublimation technique. Since most of the defects occur already in the beginning of the growth the initial stage of crystal formation has been of a particular interest in this study. Special attention is given to the process parameters enabling growth of large area micropipe free material.

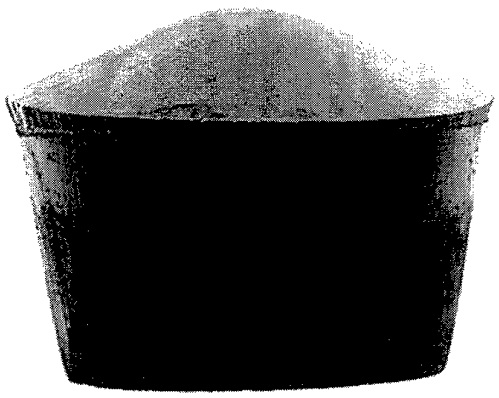

Fig. 1. A 6H-SiC crystal with size 25 mm in height

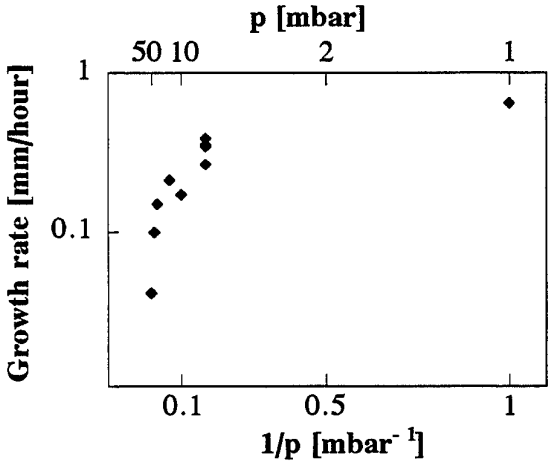

Fig. 2 Growth rate dependence on pressure

and 36 mm in diameter (2450°C, 24 hr)

The growth equipment is a vertical quartz reactor with inductively heated graphite susceptor (crucible). The growth is performed in the temperature range of 2250-2500°C at a reduced Ar pressure. SiC powder along with polycrystal boules were used as source material. Growth rate strongly depends on temperature distribution, growth pressure, and source to seed distance. The effect of these along with the seed quality on the growth process and defect formation is studied.

6H-SiC crystals up to 36 mm in diameter and 25 mm in length were grown, Fig. 1. The main parameters under consideration were: Si-loss, growth rate vs process gas pressure, and backside evaporation from the seed. Growth rate dependence on growth time was studied and it was found that the growth conditions were maintained nearly constant during 24 h growth and no growth limiting graphitization occurred. By controlling the crucible weight before and after growth the Si-loss was estimated. Thus in the crucible configuration the Si loss is not substantial and a reasonable vapor composition is kept during long-term growth.

The growth rate is dependent on the inert gas pressure. With decreasing the process pressure the growth rate increases and tends to saturate at 5-10 mbar, Fig. 2. By varying the Ar pressure in the beginning of the growth and by applying TaC environment we have succeeded in diminishing the backside evaporation and in extending the micropipe free area to 1 cm^2. It is worth noting that the micropipe free area is limited by the seed quality. By using large area seeds large wafers are possible to obtain but a compromise must be made in the micropipe density. The average micropipe density in these wafers is less than 50 cm^{-2}.

Compared to 6H SiC growth of 4H SiC crystals is performed at modified growth conditions since to achieve a single polytype material, lower temperatures and higher supersaturation are needed.

Another complication arises if a polytype transformation is expected in the beginning of the growth. We have observed that on on-axis seeds the growth starts at the edges where some steps exist, Fig. 3(a). Collected data of growth at different growth rates suggest that with increasing growth rate terrace nucleation may be initiated, Fig. 3(b). The growth rate is affected by both temperature and source to seed distance.

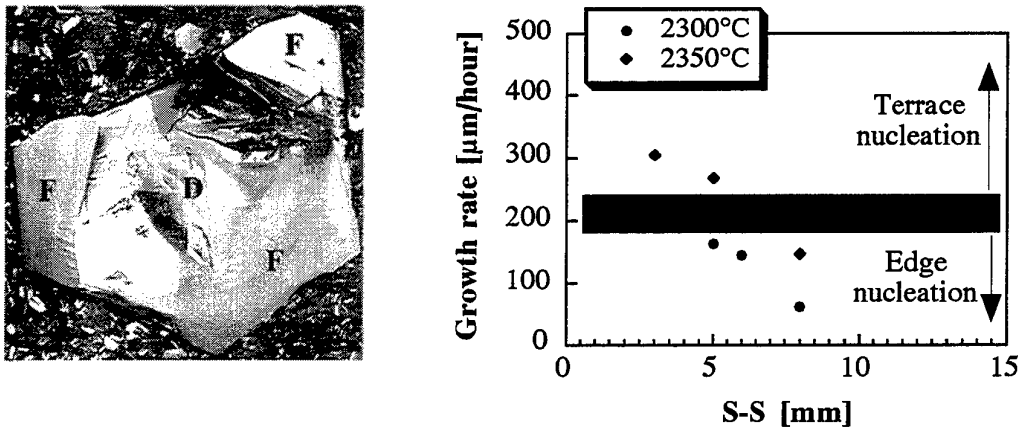

Fig. 3. (a) Nucleation at edges of Lely seed gives facetted areas (F) and a depression (D) in the center; (b) Observation of terrace nucleation and edge nucleation.

To select proper growth conditions we have studied growth rate vs temperature dependences from which apparent activation energies of growth and sublimation are derived. A pronounced effect of the uniformity of source evaporation on the crystal quality has been observed. The grown material was investigated by an optical microscope with Nomarski interference contrast and crossed polarizers, and by high-resolution X-ray diffraction. The results are used to optimize the growth crucible geometry.

INFLUENCE OF REACTOR CLEANNESS AND PROCESS CONDITIONS ON THE GROWTH BY PVT AND THE PURITY OF 4H AND 6H SIC CRYSTALS.

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The physical vapour transport method, used for the growth of large SiC wafers, takes usually place in a furnace which has a graphite crucible and a thermal shield (usually a carbon felt) in a vacuum chamber[1,2,3,4]. The graphite used for the crucible can be purified by a process that takes place before machining and commercial products commonly exhibit a typical purity of 10 ppm ash content with a maximum of 20 ppm acceptable [5]. However it is very important to treat the graphite crucible in order to recover the initial purity. The carbon felt used for the thermal insulation is generally a less pure material and it is also very important to degas it with the best conditions.

We have build a growth apparatus at our laboratory with the goal of fabricating higth purity monocrystalline SiC. We have investigated the influence of the thermal treatment of both crucibles and thermal insulation on the purity of the grown crystals. Influence of the temperature and duration of the degasing process has been studied. A quadrupole residual gas analyser has been used to monitor the degas stage of the growth system. SIMS measurements were used to study the purity of the graphite at different stages of the thermal treatment and to study the transfer of impurities into the grown crystals. Static and dynamic degas conditions under continuous argon flow have been compared and the influence of the thermal process and vacuum quality on the evolution of the insulation properties of the carbon felt has been studied. Crystals prepared in the better conditions were n-type with an excess donor concentration of about $2\ 10^{16}\ cm^{-3}$ to $5\ 10^{16}\ cm^{-3}$.

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GROWTH OF LARGE-DIAMETER 6H SiC BOULE.

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Development and adoption of SiC for high-temperature and high-power electronic devices makes it necessary to developthe production of wafers of high quality and largest possible diameter. A few groups have reported fabrication of high quality wafers, however so far the only report on large-diameter wafers (75mm) was presented by Cree Researchat the ICSC III-N'97 Conference in Stockholm. There is no doubt that it is necessary to develop the technologies of growing of small high quality crystals as well as crystals with diameter of 80mm and higher. This paper presents the recent experiments at FTIKKS on production of large-diameter 6H SiC wafers with diameter of 80mm and larger.

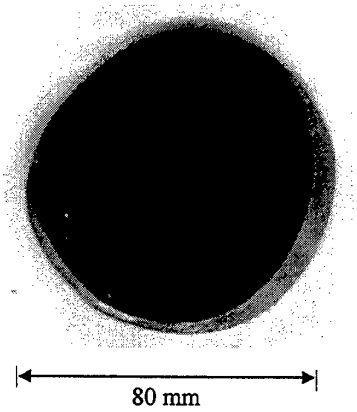

Fig.1 Large-area wafer.

SiC boules were grown by sublimation, using the modified Lely-process. This paper discusses the peculiarities of the process for production of 80mm and larger wafers. The major problem with large-size crystals is the formation of low-angle grain boundaries in grown crystals. Computer simulation of the growth process was employed to optimize the growth conditions. A computer model of crystal growth featuring simulation of temperature and strain

fields in crucible and growing crystal was implemented. Application of physical and geometrical conditions suggested by the model allows to achieve the desired sizes.

An image of large-area such wafer shown in Fig. 1. A method using crossed polarizing filters was used to determine the density of low-angle boundaries. The density of low-angle grain boundaries was found to significantly depend on the growth ratio for vertical and horizontal directions. Appropriate choice of this ratio is very important for successful production of super-large crystals. The density of micropipes and dislocations in the central part of the boule is reduced as the diameter increases, however many samples grown using a large expansion of initial diameter tend to crack. The work is currently under way to solve this problem.

PHASE CONTRAST IMAGING INVESTIGATION OF GROWTH DEFECTS ON SIC

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Nowadays, in order to satisfy the micro-electronic requirements, a big effort is addressed to produce single crystalline wafers of SiC of large-area and free from structural defects.
The interesting properties appear to be very sensitive to the crystalline quality of the SiC wafers, and, more particularly, the performances are mainly reduced by the occurrence of new kinds of defects, the macro-defects and the micropipes. It seems essential therefore to study the nature and the evolution of these defects during the growth process by means of a high sensitive and non-destructive technique.
X-ray diffraction topography, well adapted to study typical defects (dislocations, subgrains inclusions..) in semiconductors, is not able to detect such small defects in highly deformed regions. For this reason we have chosen X-ray phase contrast imaging technique.

We have applied this study to SiC samples obtained by a modified Lely method proposed by Anikin and Madar [1,2], where the growth rate is determined by the growth temperature, temperature gradient, distance between the source and seed, pressure inside the crucible and purity and grain size of the SiC powder, while the shape of the ingot is mainly function of the radial thermal gradient. The as-grown ingot of 2.5 cm diameter, was cut in several slices corresponding to a different moment of the growth. Each slice was examined by recording phase contrast image.

The X-ray experiments were performed at ID-19 Beamline, ESRF. Due to the large sample-to-source distance (145 m) combined to the small size (120 x 30 micrometers) of the source, a highly spatial coherent beam is produced. This beam is characterized by its transverse coherence length $l_c=\lambda/2\alpha$, where α is the divergence of the beam as seen from any point in the specimen. Local variations in the X-ray optical path-length in the sample, i.e. phase variations across the beam, then produce contrast through Fresnel diffraction. In the case of negligible absorption the image is uniform when the detector (X-ray film in our case) is close to the sample. As the detector is moved further away, contrast builds up, and features on different length scales are brought out more conspicuously depending on the specimen-distance D. The edges of an inhomogeneity of size s are outlined when $D < s^2/\lambda$, whereas interference fringes occur, the image being a hologram, for further increase of D.

Working in the 'edge-outline' regime, by setting the film few centimeters far away from the sample, we could observe, in agreement with a model of growth recently proposed [3], two distinct regions: an external one with a discontinuous density, corresponding to the boundaries between the polycrystals, and a central one, with a more uniform density.
In the central part we observed several defects which decrease in number going up along the growth direction. By changing the orientation of the sample with respect to the beam, it was possible to define the mutual position of these defects and their orientation.
We could in this way mainly identify three kinds of defects
a) hexagonal tubes, with edges of about 20 microns, elongated along the c axis (about 100 microns) which gradually close (Fig.1)
b) hexagonal tubes along c with added small (5-10 microns) pipes, which sometimes ramify along the direction of the temperature gradient imposed during the growth (Fig.2)
c) micropipes along c (Fig.3).
These observations indicate that the macrodefects are related to the sublimation at the level of the seed holder, and that the ramified pipes act as 'pumping' tubes. The upper part of our samples appear to be clean of these type of defects.

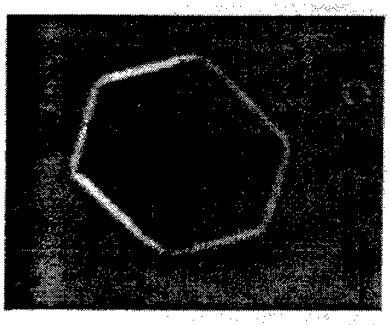

Fig.1 *Hexagonal tubes,*

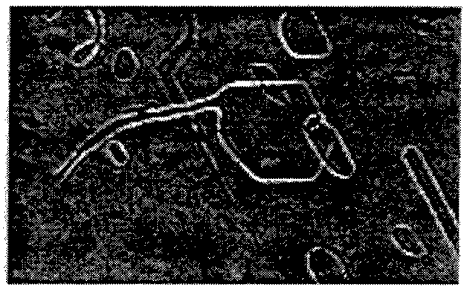

Fig.2 *Tubes along c with connected small (5-10 micrometers) pipes*

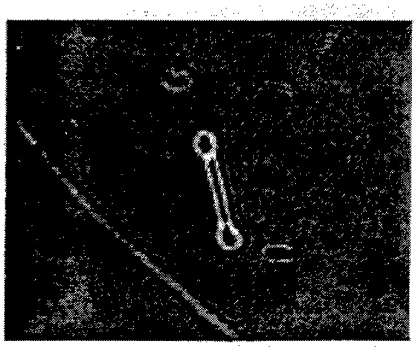

Fig.3 *Micropipes along c (less than 5 micrometers)*

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HOMOEPITAXY

HIGH TEMPERATURE CVD GROWTH OF SiC

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Introduction

The continuous progress in SiC Physical Vapour Transport (PVT) crystal growth has made substrates with increasing size and quality available, enabling further advancement in device technology. Even though several issues remain to be improved, these developments trigger higher demands on the throughput capacity of the SiC epitaxial growth process. The demands are most stringent for high-power, low-frequency applications, where thick epilayers with good morphology, low doping and defined carrier-lifetime are required. In this paper, we present growth results of two High Temperature CVD (HTCVD) techniques. The first one, described as a chimney reactor, enables both a doubled capacity of the standard hot-wall CVD process and increased growth rates, while still allowing to reach material quality standards required for high-power devices. The second one is an inverted stagnant flow reactor suited for growth rates of interest for bulk growth applications.

Epitaxial growth: the HTCVD chimney reactor concept

Simply described, the chimney system is a *vertical* hot-wall reactor, where the substrates are placed along both faces of the susceptor. This reactor concept, first proposed for III-V MOCVD [1], where the carrier and source gases flow upwards along the susceptor, combines both forced and free-convection, thus enabling increased mass transport due to a thinner boundary layer.

Growth system and results

Our development of this concept for SiC epitaxy enabled growth of mirror-like 4H epilayers with deposition rates of 10 to 30 μm/hr. The influence of process parameters as temperature (1750-1900 °C), pressure and C/Si are investigated. In particular, when using Hydrogen as carrier gas, the surface morphology depends to a large extent on the choice of the growth temperature which, for a given feed of source gases, affects the balance between deposition and etching processes. 4H-SiC epilayers free of macroscopic step bunching, with reasonable deposition uniformity, are obtained at low pressures, the remaining defects being pits essentially attributed to selective etching during the growth, as suggested by structure differences observed on Si- and C-face substrates. As described in [2] the process parameters controlling the doping have been systematically investigated, leading to N-doping as low as $2\text{-}3.10^{14}$ cm^{-3} and $5\text{-}6.10^{14}cm^{-3}$ on Si- and C-face substrates, respectively. Doping levels determined by CV and photoluminescence correlate well down to the $5\text{-}7.10^{14}$ cm^{-3} range. However, epilayers with lower doping

are generally compensated by Al or B (the lowest net carrier concentrations are in the mid 10^{13} cm^{-3} range). Provided care is taken in avoiding release of impurities from the graphite susceptor, these results should lead to device-quality material. Minority carrier lifetimes of the order of 150 ns (as measured by time resolved PL in high injection mode) can even be obtained using partly in-situ coated susceptors. Preliminary measurements on MOS edge terminated Schottky rectifiers show non-destructive voltage breakdowns higher than 1100 V with improved yield as compared to earlier HTCVD results [4].

Stagnant flow HTCVD reactor: from epitaxial to crystal growth

The stagnant flow HTCVD, where growth is carried out at temperatures in the range of 2000-2300 °C, proved to obtain much higher growth rates, up to hundreds of μm/hr [3,4], which motivates further investigation of the potential of this technique for SiC boule growth. The use of high process temperatures, together with high precursor concentration, sets a few challenges in the design of a stable open system, namely in respect with the thermal and flow stability, the gas-phase chemistry and its interaction with the crucible walls. We will describe process aspects leading to growth of 6H- and 4H-SiC with growth rates of 400-500 μm/hr. The influence of the involved growth mechanisms on the surface morphology, structural quality and purity of the grown material is discussed.

Growth process

Increased deposition rates are in HTCVD chiefly obtained with increased supersaturation and temperatures. However, as described earlier [4], the use of high concentrations of Si- and C-precursors can lead to homogeneous nucleation in the gas-phase, eventually limiting the growth rate and its uniformity. Experimental investigation shows that both formation of Si-clusters, and their subsequent stabilisation by the C-precursor, take place in the gas-phase. Process parameters such as the growth pressure, temperature and carbon precursor choice are found to enable decomposition of these clusters before reaching the crystal growth front. Further insight into the involved mechanisms is obtained from a comparison with a one-dimensional chemical model of formation, transport and decomposition of Si-clusters under typical process conditions.

Growth mechanisms: structural characterisation

A well designed HTCVD system can provide high flexibility in maintaining adequate growth species fluxes in the gas-phase. However, as the PVT technique, CVD is a vapour phase growth process, and thus certain similarities are to be expected. We describe here some structural properties using surface characterisation and X-ray diffraction techniques.

Depending on the surface termination (Si- or C-), growth on (0001) oriented surfaces leads to differing spiral structures, which can be related to the differences in surface diffusion lengths, as observed for conventional CVD and PVT growth. Both control of the supersaturation and the C/Si are essential in avoiding defects formation. A too high feed C/Si ratio can lead to formation of domains separated by deep grooves, while smooth mirror-like surfaces are obtained in more Si-rich, otherwise identical conditions. Formation of defects such as cavities at the seed-layer interface can be eliminated provided a proper supersaturation ramp is applied at the initial stages of the growth. Under prolonged growth conditions, formation of micropipes and cavities due to secondary evaporation may take place under improper temperature gradients.

Purity control

The use of pure source gases enables in principle a few orders of magnitude improved purity as compared to non-purified solid SiC sources, thus ultimately providing a finer control on the conductivity of the grown material. In agreement with previous results, PL measurements show an increased Nitrogen incorporation on C- vs. Si-face, while the opposite is observed for metallic impurities. As determined by SIMS analysis, when system auto-doping takes place, the main residual impurities are B and Ti in the 10^{15} cm^{-3} and mid 10^{14} cm^{-3} ranges, respectively.

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Epitaxial Growth of 4H-SiC by Sublimation Close Space Technique

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SiC is expected for power devices and high quality SiC epitaxial layers having high breakdown voltage is needed. For device applications, thick epilayer is indispensable. In conventional CVD method, growth rate of SiC is only about 3 μ m/h. In this study, we used CST method (Close Space Technique) which enable us to obtain thick epitaxial layers safely, simply and faster. In CST method , epilayer is grown by sublimation and SiC source and the substrate are closely spaced by graphite spacer as shown in Fig.1. This method is basically same as conventional sublimation method for boule growth of SiC. One big difference of configuration is the distance between source and substrate[1-8]. By using such a configuration, unwanted free carbon from graphite wall are minimized and growth are promoted under quasi-equilibrium condition . We used 3C-SiC polycrystalline plate with high purity as source material and Acheson and commercially available wafers with 3.5° and 8° off (0001) toward <11$\bar{2}$0>.

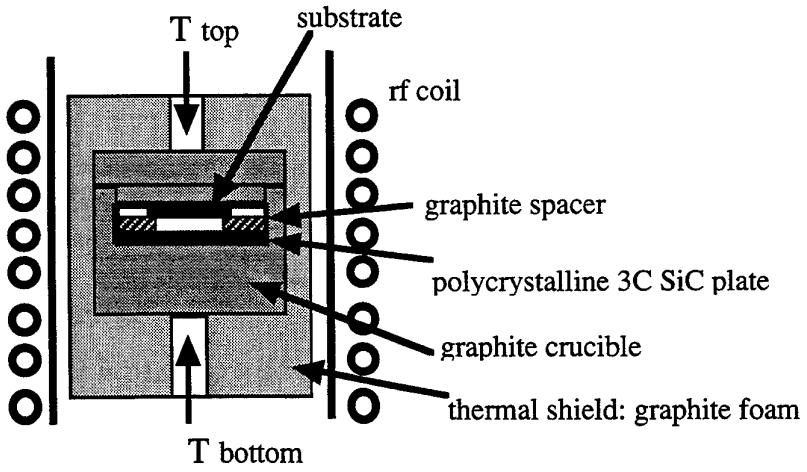

Fig.1 Congiguration of crucible in CST

On on-axis substrate, the surface morphology depended on polarity of the substrate and supersaturation near the substrate. Surface morphology of epitaxial layers grown on Si-face was

smoother compared to C-face. Though growth rate on C-face was slightly higher than on Si-face as shown in Fig.2. This is explained by the difference of vapor pressure on C-face and Si -face. In this experiment, growth rate was limited by surface reaction [4]. On off-axis substrate, surface became rather smooth compared with on-axis substrate. Under growth pressure 760 Torr and growth temperature 2200-2400℃, growth rate was about 40～200 μ m/h. In our growth system, activation energy calculated from Arrhenius plot was 147 kcal/mol. On off-axis substrate, mirror like morphology was observed all over the epitaxial layers. However, stripe-like morphology perpendicular to <11$\bar{2}$0> off-direction was observed, which is called "step-bunching" . Wavy-like morphology was also observed. We investigated surface morphology dependence on growth parameter such as temperature and distance between source and substrate . Since wavy-like morphology was often observed with high supersaturation, it is said that wavy-like morphology is appeared due to island growth on terrace. When Ta-foil was set in the reaction space, step-bunching was disappeared. Excess C-species was thought to be adsorbed by Ta-foil and stoichiometric vapor phase was achieved in the reaction space. 4H-SiC was grown homoepitaxially. According to photoluminescence, R0 and S0 lines, which are related excitons bound to neutral N donors, were observed. It means epitaxial layers are of high quality. These lines were especially observed epitaxial layers with high growth rate such as more than 100 μ m/h. It indicates that high growth rate relates with decreasing carrier density doped in epitaxial layers. Electrical properties of the epilayer and properties of Schotky diode are also discussed.

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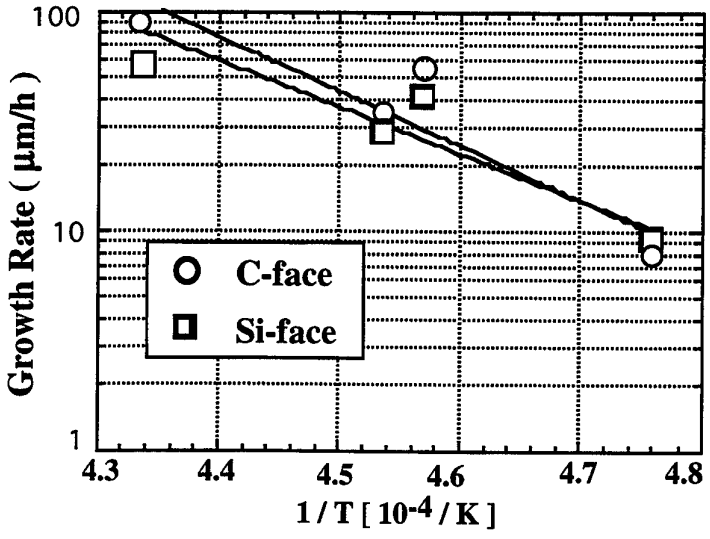

Fig.2 Growth rate dependence on polarity of the substrate

EPITAXIAL GROWTH OF SIC IN A SINGLE AND A MULTI WAFER VERTICAL CVD SYSTEM: A COMPARISON.

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Although there has been significant progress in SiC epitaxial technology within the last years, it is still a long way to go to make it a production suited process. In addition there is only a very limited commercial availability of high quality epitaxial layers at affordable prices.
Driven by these circumstances we have built up a SiC epitaxial growth activity of our own in order to be independent from external sources and to produce tailored epitaxial layers for our device research work. The aim of this in house effort is to provide layers with high purity and crystal quality for the development of SiC based high voltage devices. It is also an important goal to achieve these results reproducibly and to evaluate whether this epitaxial process can be scaled up to a production process.

For that reason we installed a single-wafer epitaxial system 5 years ago (EMCORE D 75). Within 1500 growth runs in this time frame we were able to collect a lot of experimental experience, and together with a numerical process simulation including even chemical reactions, we gained a deep insight into the growth process. Results achieved with this single-wafer system have been published already elsewhere. Achievements include residual impurity levels below 10^{14} cm^{-3} and excellent performance of both Schottky- and pn-diodes manufactured on this layers. These results encouraged us to scale this vertical epitaxial reactor concept up to a system designed for simultaneous growth on six 2 inch SiC wafers. The principal setup of this system, which was recently installed in our laboratory, is sketched in fig. 1.

The aim of this publication is to compare characteristics of the single and the multi-wafer system not only with respect to global process behavior like flow dynamics and gas phase reactions, but also looking at specific growth results like purity and homogeneity.
Similar to the case of the single-wafer system, it is possible to observe a cloud formed by silicon supersaturation and clustering above the wafer plate, and again the stability of the flow inside the reactor can be judged by observing the stability of this cloud. A stable time independent cloud with sharp boundaries usually is a necessary precondition for good growth results. Preliminary results show that, with a total hydrogen flow which is about three times as high as in the single-wafer reactor, it is possible to achieve very stable flow conditions at 1500 °C and a pressure of 300 mbar.
It is the most striking difference between the two systems, that the wafer position is out of the center of rotation for the multi-wafer system (comp. fig. 1). This has severe consequences for the homogeneity and the purity of the layers. Opposite to the single wafer system, the gas partly passes the plate material before reaching the wafer surface. Thereby the gas flow can be enriched with impurities outgasing of the plate

material and these impurities will then be incorporated in the epitaxial layer. As a consequence, choice of plate material and flow management are even more important in the multi-wafer system, and it will be quite unlikely to achieve impurity levels below 10^{14} cm^{-3}. Nevertheless our recent results, showing purity of less than 10^{15} cm^{-3} on 80% of the wafer area, are a very encouraging result for a multi wafer machine.
The homogeneity of thickness and doping in our single wafer system was quite high (Δ thickness: < 5%, Δ doping < 25%). The achievement of these data was supported by the fact that in the absolute center of rotation there is a minimum or a maximum of these properties and their radial slope intrinsically is not too high in the direct vicinity of such an extrema. This does not hold for the multi wafer system. Here a significant gradient in flow velocities and chemical gas composition exists without additional precautions. Therefore our system allows control of the radial distribution of Silane, Propane and dopants. With this we are able to achieve homogeneity values close to the results in our single wafer system.

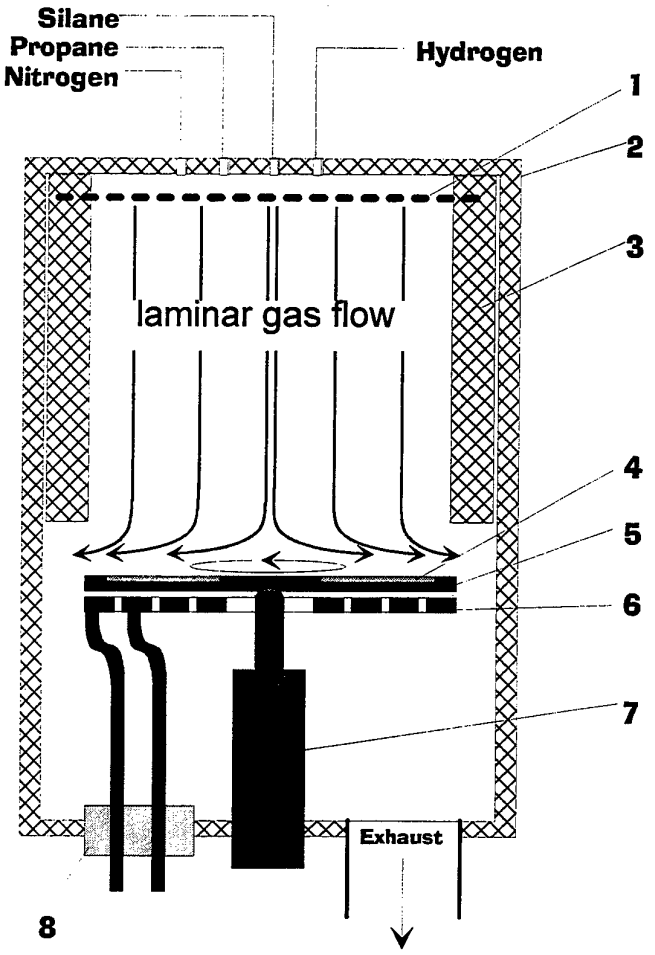

Fig. 1:
Sketch of principle of the vertical CVD system suited for six 2 inch SiC-wafers.
(1) radial gas distribution system; **(2)** double wall stainless steel chamber (water cooled); **(3)** cylindrical water cooled insert (purpose: diameter reduction, flow stabilization); **(4)** 2 inch SiC-wafer; **(5)** wafer plate (can be transferred via loadlock); **(6)** HF-coil (max. power 100 kW); **(7)** water cooled rotating feedthrough; **(8)** coil feedthrough.

EQUILIBRIUM CRYSTAL SHAPES FOR 6H AND 4H SiC GROWN ON NON-PLANAR SUBSTRATES

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Crystal growth is the main technology for formation of SiC layers with controlled doping and thickness for device applications. In order to understand this process, it is important to investigate the mechanisms for nucleation and growth. An illustrative approach is to perform growth on substrates where mesas have been formed, in order to expose lattice planes other than the c-plane. The shape of the crystal grown on a non-planar substrate will be determined not only by the planes which are revealed, but also by the diffusion of reactants and the nucleation probability at different planes. When crystals are grown at low supersaturation conditions, the growth habit is most sensitive to the bonding at the crystal surface, while the limited mobility of reactants determines the growth habit at high supersaturation [1].

We have studied growth around stripe mesas formed by reactive ion etch (RIE) oriented parallel to the $[11\bar{2}0]$ and $[1\bar{1}00]$ lattice directions and to the intermediate direction rotated 15° from those, on the Si face of 4H and 6H substrates. The samples were grown by vapor phase epitaxy (VPE) under low supersaturation conditions, i.e., at low C:Si ratio or under addition of HCl during growth. Silane and propane were used as the growth precursors, with N_2 or trimethylaluminum added for doping. The samples were cleaved and observed by scanning electron microscopy (SEM) perpendicular to the mesas. Alternating n- and p- doped layers were used as marker layers in order to temporally resolve the progress of growth.

From the crystal shapes as observed in SEM we determine the relative growth rates of the slow growing planes, exposed close to the convex top of the mesas, as well as the fast growing planes, which are revealed at the concave base of the mesas. By depicting the growth rates in polar Wulff plots, the relative growth rates are easily compared. In addition, growth rates at other planes could be interpolated assuming that the intermediate planes will not form growth facets [2]. In this way we model the relative growth rates in the half sphere of the SiC lattice projected on the [0001] axis. From this the equilibrium crystal shape at the actual growth parameters could be determined.

As the growth habit is investigated at low supersaturation, the growth rates are mainly determined by the bonding strength at the respective lattice plane. From a simple stick-and-ball model of the SiC lattice the relative growth rates could be correlated to the bonding configuration at different lattice planes, illustrating the nucleation process during SiC growth.

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EPITAXIAL GROWTH OF SiC-HETEROSTRUCTURES ON α-SiC(0001) BY SOLID-SOURCE MOLECULAR BEAM EPITAXY

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For future new applications, heterostructure of different SiC-polytypes or modulation-doped low-dimensional structures of SiC with confined electrons in a two-dimensional gas are expected to be of importance. In this context, thin epitaxial films of SiC on SiC(0001) substrates with a definite layer structure are of interest. Molecular beam epitaxy (MBE) is an attractive method to prepare such structures. First of all, however, conditions stabilizing the growth of certain polytypes have to be determined, which was not achieved by solid-source MBE so far.

We report on the epitaxial growth of SiC on α-SiC(0001) performed between 900 and 1350 °C by means of solid-source MBE. In dependence on the growth conditions, different growth modes were realized. Moreover, our results also demonstrate that the control of the Si/C ratio and the adatom concentration of Si and C is essential for the growth mode and the kind of grown polytype realized in the solid-source MBE.

On vicinal substrates (3-8.5° off-axis) of both 4H- and 6H-SiC, SiC films have been grown via step-flow growth mode at temperatures down to 1050 °C and growth rates typical in the range of 30 nm/h. Epitaxial growth of 3C-SiC on α-SiC with a sharp 3C-SiC/α-SiC interface has only be achieved at low temperatures (T<1000 °C) by an alternating supply of Si and C under surface-stabilized conditions using surface superstructures. On on-axis substrates (terrace length > 1 μm), 3C-SiC growth via two-dimensional (2D) nucleation has been realized at T = 1150 °C. Here, the epitaxial growth of 3C-SiC was found to be significantly improved by an alternating supply of C.

Performing experiments on on-axis substrates at higher temperatures (T > 1200 °C) and conditions near the equilibrium, we have realized different growth modes and conditions stabilizing the growth of certain polytypes, dependent on the temperature, terrace length and supersaturation. The supersaturation has been variied also as a function of the Si flux (Fig.1a). At higher supersaturations (> 25) always 3C-SiC has been grown, nucleated on terraces and defects. At lower supersaturation (< 25), step-flow growth mode of both 4H- and 6H-SiC has been obtained at 1300 °C and terrace length up to 3 μm (Fig.1b). At even lower supersaturations (< 15), 1D-nucleation on steps edges (Fig.1c) and homoepitaxial growth of 4H-SiC via 2D-nucleation (Fig.1d) under conditions stabilizing a C-rich surface superstructure were found.

Based on these results, we have realized for the first time a 4H/3C/4H-double-hetero transition (Fig.2) by a two step procedure. In a first step, 6 monolayers 3C-SiC have been grown on 4H-SiC(0001) by an alternating supply of both Si and C at 1000 °C. In a second step, 4H-SiC was grown on top of this 3C-SiC film than under more C-rich, near equilibrium conditions at 1300 °C.

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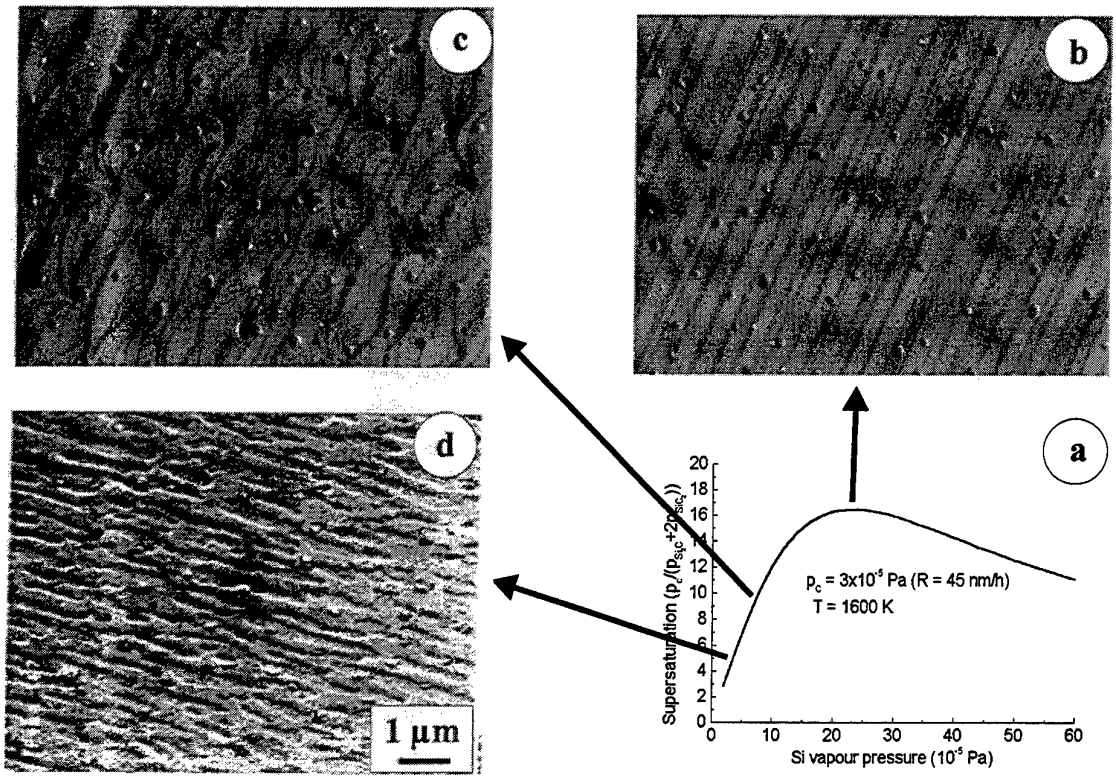

Fig.1 Scanning electron microscopic images of surfaces of 4H-SiC films grown on 4H-SiC(0001) with different supersaturations at 1600K

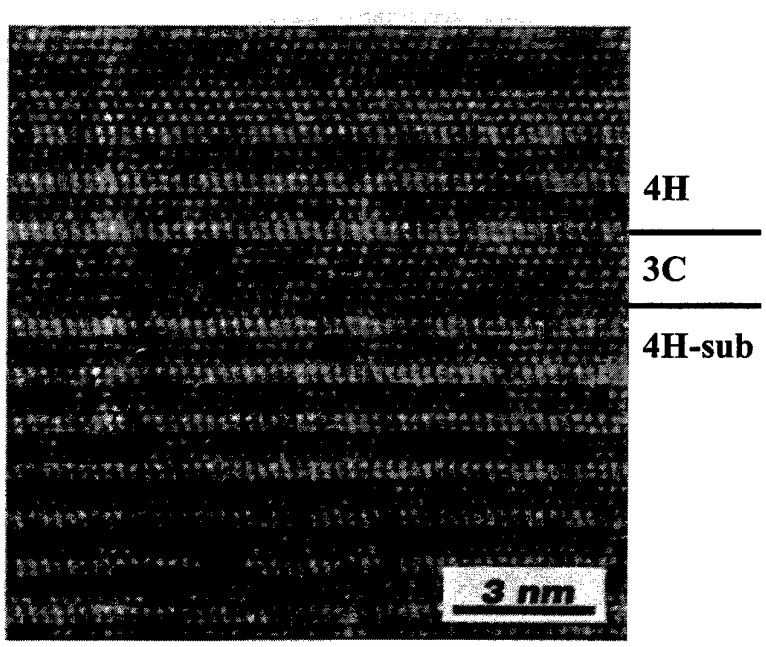

Fig.2 High-resolution TEM image of a 4H/3C/4H-SiC double-hetero transition

MATERIAL CHARACTERIZATION

OPTICAL PROPERTIES OF SILICON CARBIDE POLYTYPES: CLASSICAL RESULTS AND NEW DEVELOPMENTS

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Interest in the optical properties of SiC goes back to the early part of this century. Examples of pioneering work include the infrared transmission and reflection measurements performed by William W. Coblentz (1906-1908), the observation of electroluminescence by H. J. Round (1907), and careful measurements of the absorption of visible light, the wavelength dispersion of the ordinary and extraordinary indices of refraction, and their temperature dependence from room temperature to about 1000°C by O. Weigel (1915). As the twentieth century ends, we shall soon witness a public appreciation of the optical properties of SiC through its use as the gemstone Moissanite.

This talk will focus on what can be learned about the intrinsic band structure of the technologically important SiC polytypes as well as extrinsic donor and acceptor impurities through the investigation of optical properties, and will include a review of "classic" results as well as recent work in our laboratory.

As a result of progress in the growth of large area single crystal homoepitaxial films, there has been renewed interest in the measurement of the visible and ultraviolet reflectivity of SiC in the 1990's. Results such as our work in the 1-10 eV region [1,2] for 3C, 4H, 6H and 15R SiC are not readily interpreted by the classic methods of critical point analysis. A detailed analysis using state of the art band structure calculations, requiring a close collaboration between theorists and experimentalists, is necessary to elucidate the observed spectral features.

A detailed understanding of the band structure at the conduction and valence band edges is necessary for the interpretation of transport measurements such as the temperature dependent Hall effect and for the simulation of devices. The effective mass parameters of conduction electrons have been measured by optically detected cyclotron resonance, and may also be extracted from an analysis of the line spectra of shallow donors measured by infrared absorption. The latter method is less direct since it requires a model relating the effective masses to the level structure. For 3C SiC, the classic case, there is agreement between three different measurements: two-electron transitions observed using low temperature photoluminescence, far infrared cyclotron resonance, and infrared absorption by shallow donors, based on Faulkner's model, originally developed for Si and Ge. For the hexagonal polytypes 4H and 6H SiC, the electron pockets have lower symmetry, and the development of models is just beginning [3].

The presence of additional conduction bands with energetically small separations from the conduction band minima introduces additional complexity to the theoretical treatment of shallow donor states. Recently, Ballistic Electron Emission Microscopy (BEEM) has been applied to Pt and Pd Schottky barriers for 4H, 6H [4-6] and 15R SiC [6,7]. In 4H SiC evidence of a second conduction band minimum about 0.14 eV below the lowest conduction band minimum is observed. For 15R SiC the corresponding measured value is 0.5 eV. In both cases calculated band structures support the identifications.

The electronic structure of the top of the valence bands is also a topic of considerable current interest and importance. At present there is a lack of data for most of the important polytypes. We are presently performing careful absorption experiments, particularly wavelength modulated absorption spectroscopy, in the wavelength region near the absorption edge to measure valence band parameters such as the spin orbit and crystal field splittings. We will discuss results on 6H SiC and the more challenging case of 4H SiC.

Regarding shallow donors, we have learned much from optical measurements, particularly low temperature photoluminescence, about nitrogen, the classic example. Recently we have studied optical recombination at silicon site phosphorus donors, introduced during CVD growth of 6H SiC homoepitaxial films. Use of photoluminescence magneto-optics provides additional insight into the nature of the electronic processes giving rise to the spectra.

Optical donor-acceptor pair and free to bound recombination associated with the acceptors aluminum, gallium and deep boron has been studied in SiC for at least thirty years. The observation by low temperature photoluminescence of the optical recombination of neutral acceptor four particle complexes has been observed only within the last ten years for Al, Ga, and most recently the shallow boron acceptor. The no-phonon spectra at low temperatures tend to be more complex than for donors, and very little is understood concerning the origin of these details. We shall discuss photoluminescence magneto-optical spectra for 4H and 6H SiC:Al, 6H SiC:Ga and 4H SiC:B.

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BAND EDGE OPTICAL ABSORPTION, CARRIER RECOMBINATION AND TRANSPORT MEASUREMENTS IN 4H SiC EPILAYERS

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Different setups of the probe-pump technique based on time- and depth-resolved free carrier absorption (FCA) have been carried out to characterize unknown optical and electrical properties of n-type 4H SiC epilayers. We have investigated samples grown by chemical vapour deposition on highly nitrogen doped substrates.

For studies of temperature dependence of the band-to-band optical absorption at 3.5 eV photon energy, the depth-resolved FCA measurements have been performed in the perpendicular geometry with a spatial resolution of a few microns. Absorption coefficient is determined throughout the instant gradient of photoexcited electron-hole (*e-h*) pairs. We show that valuable anisotropy of the absorption can be detected with various polarization of the excitation light. Another finding is that absorption coefficient is nearly independent on the injection level in the range 10^{15}-10^{18} cm^{-3}.

Excess carrier diffusivity in 4H SiC is measured, for the first time, using FCA-detected transient grating (TG) technique. Analysis of TG Fourier spectrum has been performed to extract diffusion coefficient from the decay of TG erasure at various injection levels. The experimental data is compared with theoretical curves taking into account the published anisotropic mobility values of 4H SiC. Minority carrier diffusivity and ambipolar diffusivity has been determined at room temperature at the injection limits of low- and high-injection regime, respectively.

Finally, using measured *e-h* pair distribution profiles near bare 4H SiC surface and obtaining from the corresponding FCA decay lifetime, we have calculated carrier diffusion length and its variation with injection. At a constant high-injection level of 10^{17} cm^{-3} dependence of carrier recombination lifetime versus the thickness of different 4H SiC epilayers is also presented. This dependence has been analyzed in terms of bulk and surface recombination terms. Room temperature value of the true bulk recombination lifetime is extracted to be in the microsecond range.

CARBON-VACANCY RELATED DEFECTS IN 4H AND 6H SiC

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Intrinsic defects in SiC have been studied for many years. However, little is known about carbon-vacancy related defects in the material, including 4H and 6H SiC—the two most common and important polytypes. So far, the isolated carbon vacancy (V_C) was identified only for the 3C SiC.

In this work, electron paramagnetic resonance (EPR) was used to study intrinsic defects in p-type 4H and 6H SiC irradiated with 2.5 MeV electrons. Several EPR spectra were detected in samples irradiated with different doses ranging from 1×10^{17} cm^{-2} to 2×10^{18} cm^{-2}. Among these, the most dominant EPR signal (Fig.1) associates with a defect center, which has C_{1h} symmetry and an electron spin S=1/2. For both polytypes, its g-tensor was determined as g_z=2.0015, g_x=1.9962 and g_y=2.0019, where g_z and g_x lie in the $(11\bar{2}0)$ plane and g_y is perpendicular to that plane. The angle between the z-axis of the center and the c-axis of the hexagonal crystal has also the same value of about 41 degrees for the two polytypes. Clear hyperfine structure due to the interaction between the electron spin and the nuclear spin of two equivalent ^{29}Si atoms in the nearest neighbour shell was detected, confirming that the defect resides at the carbon site. A resolved hyperfine structure due to the interaction with the next nearest neighbours atoms was also observed. The structure of the defect is similar to that of the carbon vacancy in 3C SiC, but its symmetry is lowered to C_{1h} due to the lower symmetry of the hexagonal lattice. The defect is annealed out at temperatures around 200 °C, which is similar to the annealing temperature of the V_C in 3C SiC. The spectrum was not observed in n-type material. Its strength correlates with the dose of radiation and no characteristic hyperfine structure from common impurities in SiC such as Al, B, N and H was detected. Based on its electronic structure, annealing behaviour and formation condition, the defect is suggested to be the isolated carbon vacancy in the positive charge state.

A new EPR spectrum appears in 4H and 6H SiC samples when the dose of irradiation reaches the range of 10^{18} cm^{-2} (Fig.1). The spectrum associates with a defect, which has a low symmetry and an electron spin S=1. For both polytypes, the g-value is isotropic, g=2.0063, and the crystal field parameter characterised for the spin-spin interaction is determined as $|D|=5.52\times10^{-2}$ cm^{-1}. The principal axis of the crystal field tensor D lies in the $\{11\bar{2}0\}$ planes and makes an angle of ~46 degrees with the c-axis. The hyperfine structure due to the interaction between the electron spin and the nuclear spin of ^{29}Si atoms in the nearest neighbours was detected. The defect was also annealed out at temperatures around 200 °C. A carbon-vacancy pair model is proposed to explain the electronic structure of the defect.

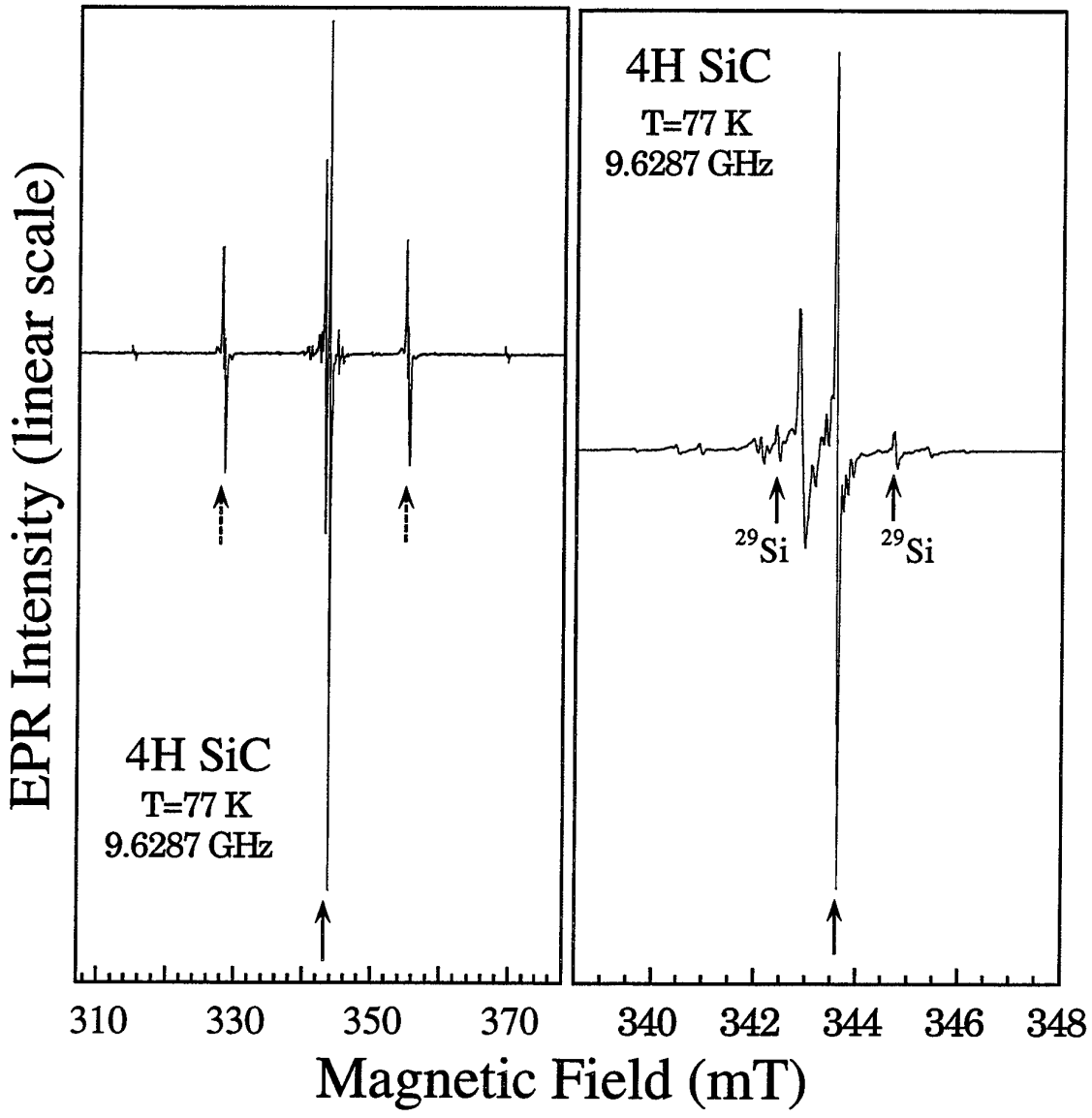

Figure 1: EPR spectrum recorded at 77 K for p-type 4H SiC irradiated with 2.5 MeV electrons with a dose of 1×10^{18} cm^{-2} for the magnetic field **B** along the c-axis. The EPR line from the spin S=1/2 center and its hyperfine structure due to the interaction with two equivalent ^{29}Si atoms in the nearest neighbour are indicated by solid arrows. Resonance lines indicated by dashed arrows belong to the spin S=1 center. The microwave frequency is ν=9.6287 GHz.

DEEP LUMINESCENCE CENTRES IN 6H- AND 4H-SILICON CARBIDE

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So-called D centres are observed in 6H-SiC crystals, which were grown with excess of Si and additionally diffused with B, or, which were B implanted and subsequently annealed at T > 750°C. In such crystals, which have a strong yellow luminescence, a deep level at about E_{VB}+600 meV is observed, which turned out to be B-related. In order to determine the microscopic structure of the D centre several magnetic resonance investigations were published so far (see e.g. [1,2]). However, the microscopic structure is not clear up to now. Electron paramagnetic resonance (EPR) and photoluminescence detected EPR (PL-EPR) spectra observed at 9 GHz and at 35 GHz show different spectra in different publications and were all ascribed to the D centre [1,2]. We performed PL-EPR measurements at 24 GHz and high field PL-EPR measurements at 72 GHz, in order to have a better resolution for g factors. At both frequencies we observed different new PL-EPR spectra in the luminescence of the D centre. From the set of EPR spectra measured at 9 GHz, 24 GHz, 35 GHz, and 72 GHz we are now able to show that all lines observed belong to only one centre. So far Baranov [2] observed only axial D centres, which now turned out to be only a subset of the four orientations of the D centre and which were all observed in our experiment. A microscopic model for the D centre is discussed.

Other defects of technologically importance observed after annealing of SiC bulk samples above 750°C are the so-called Z centers. They were also observed in irradiated SiC and in ion implanted SiC. From those defects only energy levels at E_{CB} - 620 meV and E_{CB} - 640 meV [3] in 6H-SiC and at about E_{CB} – 670 meV in 4H-SiC are known [4]. The Z centres are stable up to temperatures of 1700°C. So far no optical data are available, except for 6H-SiC where some absorption lines were observed and attributed to the Z centre because they show up at the energies given above.

In a 4H-SiC epitaxial layer (7 μm) which was He-implanted and annealed at 1000°C for 10 min. and at 1700°C for 15 min. [5] we measured a new PL band between 620 and 670 nm. The onset of the PL band corresponds to the energy level known for the Z centre in 4H-SiC. The EPR spectrum measured as PL-EPR in this band consists of two line sets. One line set is due to the known nitrogen donor, the other is a single line showing no resolved hf structure and is so far due to an unknown defect. The optical absorption spectrum consists of two bands with onsets at about 0.66 eV and at 2.5 eV. The observation, that the PL-EPR observed is due to a negative PL-EPR signal will be discussed in a level scheme together with the levels known for the Z centre and the nitrogen donors. The PL and absorption spectra could be understood assuming a defect level at about E_{CB} – 0.66 eV.

In order to obtain more information on the microscopic structure of the Z centre we performed electrically detected EPR (ED-EPR) measurements. Conventional EPR measurements were not successful in the thin epitaxial layer. They only show the known nitrogen donor EPR signals from the substrate. With ED-EPR we observed a new spectrum consisting of two lines. One line is due to the nitrogen donor and could be understood within a variable range hopping model, which will be explained in detail. The nature of the second line, different from that observed with PL-EPR, is not yet known and the subject of further investigations. However we can give a detailed model of the spin-dependent processes observed.

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POLYTYPE-DEPENDENCE OF V- AND Cr-RELATED DEEP LEVELS IN SiC (4H,6H,15R)

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Supplementing the already known deep level data of Cr and V in the polytypes 4H and 6H [1,2,3,4], bandgap states of these elements are identified in the polytype 15R by Radiotracer-Spectroscopy. Epitaxial layers of n-type 15R-SiC were recoil implanted with the radioactive tracer isotope ^{51}Cr (decay to ^{51}V) and Deep Level Transient Spectroscopy (DLTS) measurements were performed repeatedly during the elemental transmutation. The DLTS-spectra reveal two levels in the bandgap of 15R-SiC with decreasing concentration and three levels with increasing concentration (see Fig.). The splitting of the Cr peak is not well-resolved in the DLTS-spectra. Therefore, the evaluation is performed by fitting a sum of exponential functions along the digitised capacitance transients. The concentration changes of the observed defects directly reflect the half-life of the isotope incorporated. This leads to a definite assignment of the defects to the elements: For chromium, two slightly split levels (centred at $E_C - 0.43$ eV) are detected. For vanadium, three levels (centred at $E_C - 0.76$ eV) are resolved. The splitting is attributed to the occupation of non-equivalent lattice sites in 15R-SiC.

The level positions of Cr and V in 15R-SiC are compared to those in the bandgap of 4H- and 6H-SiC considering the Langer-Heinrich rule.

For all polytypes investigated (4H,6H,15R), the splitting of the V levels is greater than for Cr and is increasing from 4H, 6H to 15R-SiC. The same tendency is observed for Cr where a splitting is resolved by DLTS in the polytype 15R only.

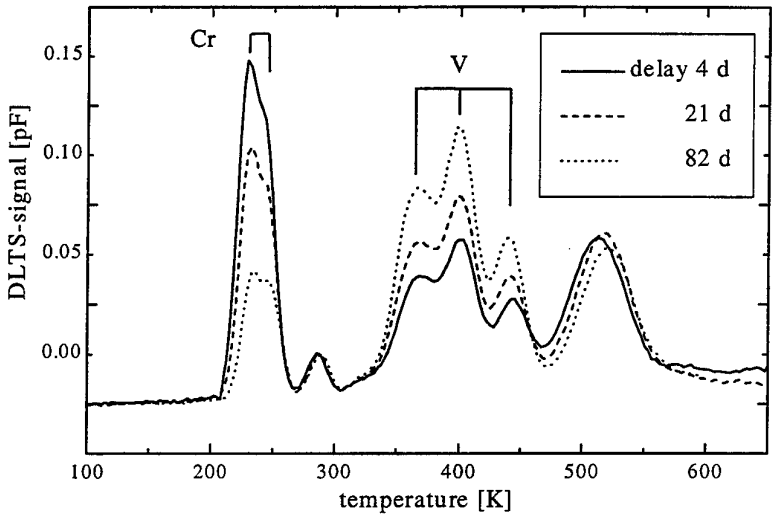

Fig.: *DLTS-spectra of n-type 15R-SiC measured during the elemental transmutation of* ^{51}Cr *to* ^{51}V

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PROCESSING

State of the Art of SiC Microwave Power devices

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Advantages of wide bandgap semiconductors in the area of high frequency power amplification have been identified for long. Still true demonstrations confirming the theoretical predictions have only be obtained recently with the arrival of the first Silicon Carbide prototype devices. The pioneering device structure has been the Static Induction Transistor which still performs today's best records and whose champions are Westinghouse and more recently Northrop Grumann. Outstanding results have been obtained, especially in pulse mode with peak results of 1750 W at 0.6 GHz and nearly 200W at 3 GHz. However, the fabrication of this kind of devices with the highest level of performance requires very complex process steps and simpler structures seem to be prefered, at least for the high frequency end.

This is probably the main reason why the other players in this area have chosen less exotic structures inspired from existing technologies. On one hand GaAs-like Mesfets are being developped by Cree, Motorola, Thomson CSF and two or three other players that have not published yet. On the other hand, more Si-like JFETs are studied essentially by NASA with promising power density but still limited total available power today.

For all those devices, the availability of 4H material has allowed to gain a few dB in global performances over the 6H demonstrators, and there subsists no doubt about the favored polytype for SiC microwave devices. If cubic stays out of reach, 4H will be the universal choice. It is very important for the developement of SiC high frequency industry that the material of choice for power electronics is also 4H, which means that microwave power area will benefit from works essentially oriented towards this area, presently considered to yield a much wider applications range in the future.

SiC MOS, and especially LD-MOS, which would be the most favored structure for the 0-2 GHz devices, is still not mature, due to unsolved interface problems, especially on p-type material. Channel mobilities are unsufficient ($< 70\ cm^2.V^{-1}.s^{-1}$) for horizontal MOS on <0001> surface and especially catastrophic for vertical channels ($< 10\ cm^2.V^{-1}.s^{-1}$). Clever accumulation mode structures recently published may open an opportunity to get working RF MOS devices sooner.

For bipolar structures, it seems that there is no more published work on homojunction transitor and that the promising SiC Heterojunction Bipolar Transistor with GaN emitter published by Pankove and al. in 1995 has not yet been transformed into a successful microwave device.

Still those two structures: HBT and LD-MOS stay as a long term target for many of the players in the SiC microwave power area.

For most of the horizontal devices like the JFET and MESFET presently developped, the availability and usability of semi-insulating substrates is required. Such substrates have been available on the free market for two years now, but their price (> 500$ / usable cm^2) still keep them out of reach for most potential users.

The happy few that have access to such substrates, and especially those who produce them, have now reached excellent pulse mode results. The brightest examples today are Northrop Grumann's 6.3 W @ 10 GHz Mesfet results.

However, similarly to what has been experienced on early GaAs technology, trapping problems still impede most devices performance, especially in CW mode. The recent announcement by Cree about transitors giving 50 W @ 3 GHz in CW mode shows a great progress of the available power - a factor of 3 in one year time - but the power density (1,2 W/mm for 50 W, 2 W/mm for 20 W) is far from the hopes (about 4W/mm at this frequency) and there is still place for coming research and results.

Looking at the road towards industrialisation, we have to point out that there is no reliability data published for SiC microwave power devices, although preliminary studies seem to show robustness of the tested samples throughout the measurement cycles, sometimes quite unfair for the device under test.

On the other hand, as possible outsiders, group III Nitride devices are showing up as a spin-off from the tremendous excitation on UV and visible opto-electronics. Excellent power density at high frequencies have been measured, still on quite small HFET devices. It is however clear that microwave power applications of nitrides will require substrates with good thermal conductivity, - which seems to discard sapphire if heat has to cross it in the final device - and favors either the use of SiC as the substrate, or the transportation of the nitride layer on a thermally conductive material.

No one seems to know now what will be the respective places of pure SiC and nitrides in the microwave power arena. It will depend a lot on the reliability study and the real influence of crystal defects on the aging behavior of the devices. Moreover, each device topology may react differently and there is a great risk that the final answer about the main possible technlogies will not be obtained before ten years from now. Good surprises are possible and it still may happen that a performant and reliable Nitride technology will take over all pure SiC ones, owing to the remarquable robustness suspected for nitrides

Finally, looking at the time schedule, it seems realistic to state that SiC microwave devices will be sampled to selected potential customers before year 2000 and that, depending on the price of semi-insulating material, a first generation of MESFET devices will be available on the free market by years 2001-2002.

PHYSICAL PRINCIPLES OF FORMATION OF OHMIC CONTACTS TO SILICON CARBIDE

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By now most papers concerned with ohmic contacts to SiC are focused on studying concrete systems (elemental and chemical composition of contact coatings, determining the specific contact resistance, etc.). The experimental data is accumulated for various systems, including the most perspective systems such as contact coatings based on Ni for n-6H-SiC and on Ti-Al for p-6H-SiC. The formal attempts are performed in some cases to connect the results obtained for such systems with some theoretical models. However, practically no attempts have been undertaken to generalize the experimental material and to reveal the main physical mechanisms which underlie of formation of ohmic contacts to silicon carbide. Nevertheless, such examinations are necessary both for constructing models that describe adequately the contact behaviour and for optimizing fabrication procedures to obtain stable reproducible contacts with the minimum possible specific resistance (ρ_c) value.

On the base of experimental investigations of various contact systems (such as Mo, W, Ni-based contacts to n-6H-SiC; silicon-containig, Ti-Al, Mo-Au-Al, W-Au-Al - based contacts to p-6H-SiC and some others) and of surface-barrier structures and also on published data, we make an attempt in this work to generalize consistently the data with purpose to reveal the general physical regularities and processes providing the non-rectifying current-voltage characteristics of contacts to silicon carbide. We consider mainly the ohmic contacts to SiC with doping level less than $1x10^{19}$ cm^{-3} since the task of contact fabrication is more easy at the higher doping level due to substantial influence of tunnel currents. Besides, our consideration is connected with ohmic contacts prepared with using the annealing procedure, since such contacts are most interesting with practical standpoint and only in this case the low-resistance contact can be fabricated to not very high doped epitaxial layers and substrates.

The main conclusions were formulated on the base of experimental data obtained:

1. Chemical interactions in the contact coatings studied do not lead directly to formation of a non-rectifying contact in the all investigated cases. Nevertheless, these processes may exert indirect influence via accelerating or reducing of the surface SiC dissociation at the annealing. It can caused, e.g., the different annealing temperatures necessary for fabricating non-rectifying contacts based on different contact coatings.

2. At the annealing the silicon carbide dissociation is observed always. This dissociation leads, firstly, to forming the of layer enriched by carbon on the interface region the silicon carbide - contact coating, and, secondly, to formation of subsurface silicon carbide layer containing the point defects or their clasters caused by the silicon egress from the SiC crystal lattice. We suppose that formation of such type defects is a main factor which determines the appearance of the ohmic or rectifying current-voltage characteristic of contact.

3. Formation of this subsurface layer leads to opposite consequences at the formation of contact to n-6H-SiC and p-6H-SiC: to non-rectifying current-voltage characteristic of contact in case of n-6H-SiC (for example due to effective recombination channel caused by the formation of considered defects) and also determines the specific resistance of contact and to rectifying current-voltage characteristic in case of p-6H-SiC. Therefore, the appearance of subsurface layer enriched by carbon is a negative factor at the ohnic contacts fabrication to SiC p-type. This layer is formed always due to SiC dissociation if additional actions are not undertaken. It can explain difficulties at the fabrication of ohmic contacts to p-6H-SiC with using of single-component contact coating (with the exception of aluminum).

4. For fabrication of contacts to p-6H-SiC with non-rectifying current-voltage characteristic it is necessary to provide additional actions which will be able to compensate the silicon egress from crystal lattice. Such actions can be: introducing of silicon or component corresponding to doping impurity (aluminum, boron) into the composition of contact coating. In the last case the contact system is less sensitive to silicon egress since the doping impurity occupies the silicon site in silicon carbide crystal lattice in subsurface SiC layer providing the layer with higher concentration after the annealing. It can be noted that only in this cases the low-resistance ohmic contacts to p-6H-SiC were fabricated.

Thus, we suppose that Si/C ratio in the interface region and in subsurface silicon carbide layer is the most important factor at the ohmic contacts formation. The above approach provides a consistent explanation of practically the all available data on ohmic contacts to SiC-6H. Note also that, since the above features are not specific to 6H-SiC, it would be expected that the considered aspects of ohmic contact formation will be valid for other SiC polytypes.

This work was partly supported by Schnider Electric (France) and by Arizona University (USA).

CHARACTERIZATION OF SPUTTERED TITANIUMSILICIDE OHMIC CONTACTS ON N-TYPE 6H-SILICON CARBIDE

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The development of superior high-power, high-temperature and high frequency devices based on SiC with its excellent physical properties, demands for thermodynamically stable ohmic contacts with low specific contact resistance [1]. Various metallizations for ohmic contacts have been examined until today [2] but though the commonly used Ni-contacts reveal a low contact resistance on n-type SiC, excessive carbon accumulates at the metal-semiconductor interface during the annealing for contact fabrication thus jeopardizing the long-term stability of the contacts. Therefore, the search for appropriate metallizations is still of great interest.

In this work we report on the characterization of titaniumsilicide contacts which are sputter deposited from a $TiSi_2$ target onto p-type SiC-wafers carrying one 5µm thick nitrogen-doped n-type (N_A-N_D=$5 \cdot 10^{18}$ cm^{-3}) epitaxial layer. We quantitatively considered the systematic error of the electrical measurement technique to determine a reliable value for the specific contact resistance ρ_c and correlated this value with the chemical reaction between metallization and semiconductor during contact formation.

While the as-deposited contacts revealed rectifying behavior, the current-voltage characteristic became ohmic after treating the samples by rapid thermal annealing (RTA) in Ar at temperatures above or equal to 1000°C (Fig. 1). To determine ρ_C the common linear transmission line method (TLM) [3] was used (Fig. 2). The TLM is based on a simplified model of the metal-semiconductor contact assuming zero semiconductor thickness and zero gap width between the contact pads and the edge of the mesa (t=0 and δ=0 in figure 2).

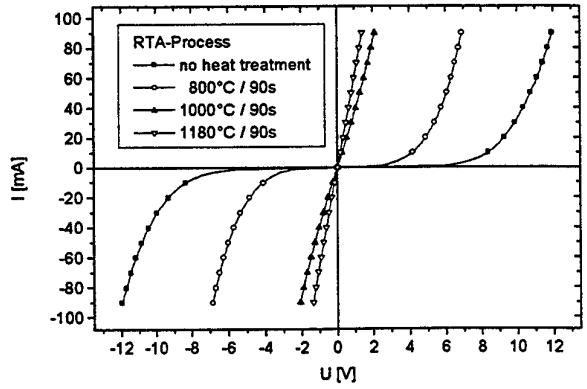

Fig. 1: Current-Voltage-Characteristics of $TiSi_X$-contacts on SiC after different RTA processes

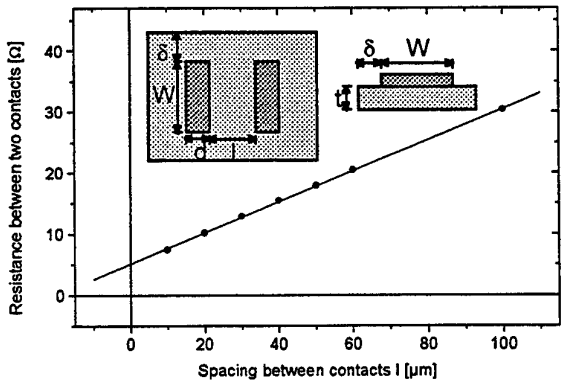

Fig. 2: Determination of R_C from TLM-measurements

Because such conditions cannot be achieved for real contacts, the extracted ρ_c-values are subjected to systematic errors (finite depth effect, current crowding effect, gap effect [3]). To quantify these errors three-dimensional finite element models of TLM-structures with various geometries were created with the FEM-software ANSYS®. Choosing a certain *actual* specific contact resistance $\rho_{c,Act}$ as material constant for the FEM-model, the current and voltage distributions of the TLM structures was simulated. From these data, the different resistance-values measured for real TLM-structures were calculated. These resistance-values lead to a value for ρ_c which differs from $\rho_{c,Act}$ because of the systematic errors. By comparing $\rho_{c,Act}$ and ρ_c the systematic error for a certain TLM-structure can be quantified. This procedure has been applied to the experimental TLM-geometries for $\rho_{c,Act}=1\cdot10^{-5}$ $\Omega\cdot cm^2$ and $\rho_{c,Act}=1\cdot10^{-6}$ $\Omega\cdot cm^2$. The results are displayed in figure 3. Because of the systematic errors inherent in the TLM model ρ_c differs from the *actual* value $\rho_{c,Act}$. The relative difference increases with increasing contact length and decreasing specific contact resistance.

The ρ_c-values obtained from different lengths of $TiSi_X$ contacts after annealing at 1180°C agree well with the simulation. By interpolating between the experimental results and the FEM-simulation, a specific contact resistance of $\rho_c \leq 8\cdot10^{-6}$ $\Omega\cdot cm^2$ on n-type 6H-SiC with a doping concentration of $5\cdot10^{18}$ cm^{-3} can be extracted for the titaniumsilicide contacts. This value compares very well with the best results published so far.

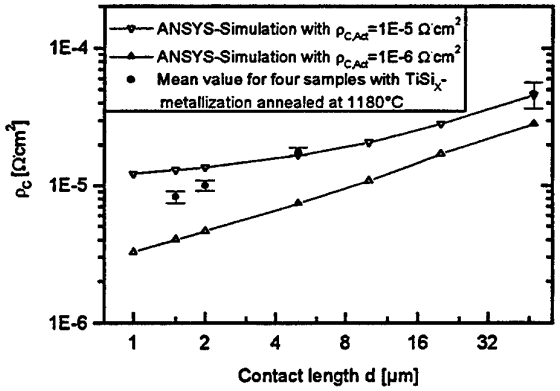

Fig. 3: Comparison between ρ_c measured for $TiSi_X$ contacts (after annealing at 1180°C) and ρ_c calculated from FEM-simulations for two different material parameters $\rho_{c,act}$.

In addition to the electrical characterization of the contacts, secondary neutral mass spectrometry (SNMS) was used to elucidate the reaction between titaniumsilicide and SiC during RTA [4]. Plotting the SNMS-data for an as-deposited sample and a sample annealed at 1180°C into a simplified isothermal section of the Ti-Si-C-phase diagram reveals that the as-deposited layer of understochiometric $TiSi_{1.7}$ turns into a $TiSi_2$-layer by the RTA treatment (Fig. 4). Because all datapoints of the annealed sample are located within the three-phase-field $TiSi_2$-SiC-Ti_3SiC_2, the SNMS depth profile can be converted into a chemical depth profile demonstrating that the ternary phase Ti_3SiC_2 grows at the interface between $TiSi_2$ and SiC (Fig. 5).

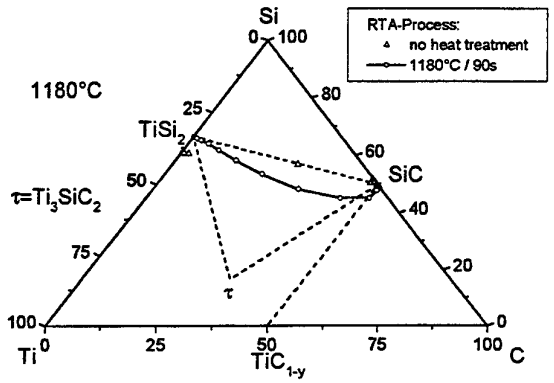

Fig. 4: SNMS depth profiling data displayed in a simplified isothermal section (1180°C) of the ternary Ti-Si-C phase diagram

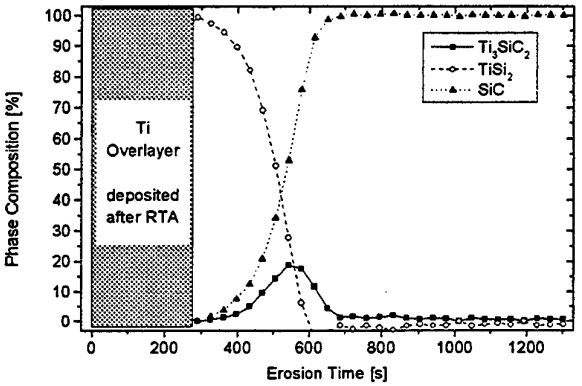

Fig. 5: Phase composition of a $TiSi_X$-film on SiC (after annealing at 1180°C) extracted from SNMS concentratio depth profiling

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DIFFUSION OF LIGHT ELEMENTS IN 4H- AND 6H-SiC

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Most impurities exhibit negligible diffusion coefficients at temperatures applicable to SiC device processing except for atoms with very small atomic radii like hydrogen, lithium and beryllium. Acceptor and donor impurities as well as deep-level defects can react with these fast diffusing species and form complexes. Hydrogen and lithium are known to passivate dopants in semiconductors[1,2].
In this work we have studied diffusion of deuterium and lithium in 4H and 6H SiC. Concentration versus depth profiles of the dopants are obtained by secondary ion mass spectrometry (SIMS). Deuterium (^{2}H) is employed instead of ordinary hydrogen (^{1}H) to increase the sensitivity in the SIMS measurements. Epitaxially grown SiC layers containing a boron "spike" as well as n- and p-type substrates have been used. The diffusion source of deuterium and lithium are introduced into the samples by implantation with 20 keV $^2H^+$ ions and 30 keV $^7Li^+$ ions, respectively, to a dose of $1x10^{15}$ cm^{-2}. The sample are heat treated at temperatures between 400 and 1000°C in a vacuum furnace for 0.25 to 16 h.
Deuterium and lithium will readily decorate the bombardment-induced defects in the vicinity of the ion implantation profile. Hence, these profiles are limited as diffusion source and only a small amount is "free" to migrate into the sample. At temperatures exceeding 900°C the complexes formed in the implanted region start to break up[3] and release large amounts of deuterium or lithium. Diffusion characteristics for deuterium and lithium show many similarities but the temperature range of interest is shifted to higher values for lithium. Comparing the diffusivity in n- and p-type material gives a much higher value for p-type materials. For both deuterium and lithium the degree of trapping depends on the boron concentration. In fig. 1 depth profiles are shown for an implanted p-type 6H-SiC substrate heat treated at 600°C at times ranging from 0.25 to 16h. The sample contains aluminium and boron to a concentration of $1x10^{18}$ and $3x10^{17}$ cm^{-3}, respectively. The total amount of mobile lithium remains constant at 1, 4 and 16h and the lithium atoms have only rearrange and moved deeper into the sample as the time increases. The shape of the curves can be explained in terms of formation and dissociation of lithium containing complexes. Comparison will be made with numerical and analytical calculations of the reaction kinetics assuming a single trap model.

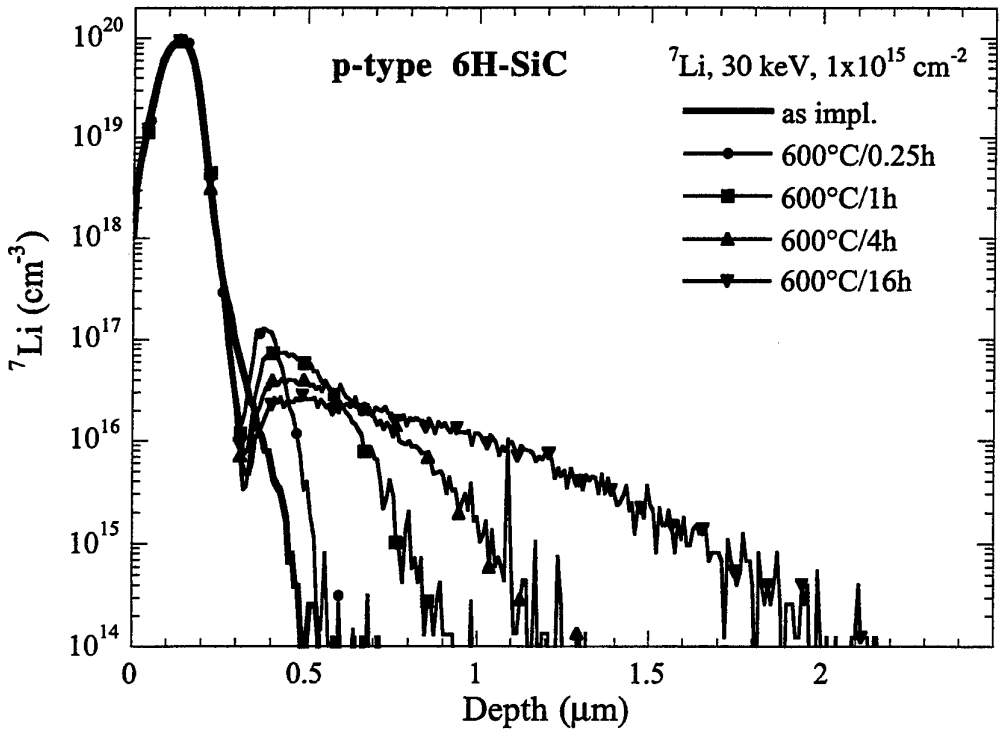

Fig. 1. Lithium concentration versus depth of a p-type 6H-SiC sample implanted with 30 keV $^7Li^+$ ions to a dose of $1x10^{15}$ cm^{-2} after 600°C anneal at 0.25, 1, 4 and 16 hours.

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ANNEALING ION IMPLANTED SiC WITH AN AlN CAP

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Comprehensive ion implantation technologies have been developed for silicon and GaAs. However, this technology is still in its infancy for SiC primarily because the wafer has to be raised to such high temperatures - $\geq$ 1500°C to activate the implant. At these temperatures silicon preferentially evaporates destroying the surface in a short period of time. This process can to some extent be mitigated by heating the wafer in the presence of SiC powder, or covering the wafer with another sacrificial SiC wafer. The latter has produced better results, but some silicon still escapes because a hermetic seal has not been formed; it is also expensive. The dielectrics used to form hermetic seals on GaAs - SiO_2 and Si_3N_4 - also cannot withstand the high annealing temperatures required for implant activation. However, we have recently shown that AlN can withstand the high annealing temperatures, and we as well as others have demonstrated that the AlN can be selectively removed by both dry and wet etches. In this paper we show that AlN can be used as an effective encapsulate for SiC implanted with nitrogen and describe some of the problems associated with using it.

4H-SiC films doped to 6×10^{16} cm^{-3} with aluminum were grown 8.5° off axis on SiC substrates 1.375 inches in diameter by Cree Research. The as grown films were structurally characterized by x-ray diffraction (XRD) and RBS, and then were ion implanted at 700°C at energies between 15 and 180 keV with doses between 3.3 and 34×10^{13} cm^{-2} that resulted in approximately creating a layer 0.3 μm thick uniformly doped to 10^{19} cm^{-3}. The wafers were cut into pieces ~ 8 mm on a side, and were divided up into adjacent pairs - one piece was used for structural studies and the other was used for electrical measurements. For the structural studies the base line x-ray, RBS, and SIMS spectra were recorded, and one piece was set aside for TEM studies. All but the TEM sample were coated with an AlN film ~ 150 nm thick by pulsed laser deposition (PLD) at 700°C in a vacuum of 1×10^{-7} Torr, and the surface morphologies were examined in an SEM. Pairs were annealed at 1400, 1500, 1600 and 1700°C for 30 min and at 1600°C for 15, 30, 60 and 120 min. SEM, XRD, RBS, and SIMS measurements were made on one sample in the pair, and electrical measurements were made on the other sample. Most of the measurements were made after the AlN cap had been removed, but some SEM and XRD measurements were made prior to removal.

The SEM micrographs show little change in the AlN annealed at 1400°C, but show that the grain size in all of the other films appear to increase in size, but the films remain contiguous. Also, some etch pits are produced on the SiC surface by the KOH based etch used to remove the AlN. XRD rocking curves show that the ion implant damage is reduced more for the higher temperature and longer time anneals as the 6H (0006) or 3C (111) peaks present in the as-deposited sample become more distinct. However, their relative peak heights appear to change in some instances suggesting that some material transforms at these elevated temperatures. The RBS results show increased channeling for the higher temperature and longer time anneals, and χ approaches the value for the as grown sample. The SIMS results show that there is detectable in-diffusion of the nitrogen especially for the higher annealing temperatures and longer annealing times, and we are currently attempting to extract the effective diffusion coefficients by modeling the profiles. Now that the contacting problems have been solved, Hall measurements are being made on the samples, and the results will be reported at the meeting.

NITRIDES ON SiC

GaN From Fundamental Physics to Device Applications

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Abstract

This presentation will review fundamental properties of GaN, highlight its technology, summarize problems of crystal growth and doping, and discuss several applications: emitters, detectors and high temperature devices.

Industrial aspects of GaN/SiC LED's in Europe

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The market for light emitting devices is continously growing approx. 17% per year. Main applications are automotive, displays, illumination, back lighting, traffic signals etc. Within this market a good portion is covered by blue light emitting diodes, being used in all types of full color application arround 8% of the LED market are blue diodes.
To realize blue light emitting devices, GaN is todays material of choice. The spectral range possible covers a wide range from 363nm to 530nm, theoretically even further to 650nm. Beside blue and green the short wavelength emission of around 370nm is extremly interesting for luminescence conversion leading to almost any color include single chip white light emitting devices.

Production of Ga(In,Al)N-devices are mainly carried out in MOVPE-systems using two types of substrate: sapphire and SiC
Even though Sapphire is of higher quality and the less expensive material, SiC has an increasing market share for blue light emitting diodes. The advantage of SiC is mainly based on its conductivity leading to vertically structured devices with front and back side contacts. Devices made on sapphire suffer from two top contacts, consuming chip size, whereas on SiC size is limited only by light output and chip handling for packaging. Especially for mass production the advantage of number of chips per square inch will become a continuously growing argument to use SiC as a substrate.

HIGH TEMPERATURE CVD SYSTEMS TO GROW GaN OR SiC BASED STRUCTURES

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Silicon Carbide is presently gaining much attention as a material for high temperature, high speed and high power devices. However, fabricating epitaxial SiC or GaN films is still a challenge since very high growth temperatures (up to 1600 °C) must be used. This requires a carefully adapted design of reactors to ensure laminar flow conditions and a controlled depletion of the reactants inside the reactor. A second class of materials that is also playing a more and more important role today are the III nitrides (AlN, GaN, InN and alloys consisting of these). These materials are also at high deposition temperatures (up to 1300 °C). Furthermore, these materials are grown on special buffer layers grown at much lower temperatures and are typically part of complex heterostructures which require abrupt changes of the growth temperature to realize sophisticated optoelectronic and electronic devices. As an example our high quality InGaN layers were grown at about 700 °C and the AlGaN cladding layer of a laser or a LED require temperatures higher than 1100 °C. In general, both nitrides and SiC are similar in their challenges to the growth equipment. This study uses a family of high temperature reactors to grow SiC and Nitrides.

We describe the use of high temperature reactors to grow SiC and Nitrides. The load capacity ranges from single wafer machines to multiple wafer mass production reactors. All these reactors have a two flow injection system allowing a separated inlet of the various reactants. To achieve maximum uniformity of the growth, the Gas Foil Rotation® Principle is applied. The multiwafer reactors are Planetary Reactors with double rotation of substrates. Extensive modeling has been used in order to find the optimum reactor geometries. Gas flow dynamics, temperature management and the physical and chemical properties of the precursors were considered in these models. Thus an optimization of uniformity and efficiency and a minimization of undesired parasitic reactions has been obtained. This contribution will work out the differences and the similarities of the high temperature growth of both material systems in AIXTRON reactors already established in production. Results on the growth of SiC and GaN will be presented.

DEVICES

SiC Power Devices for High Voltage Applications

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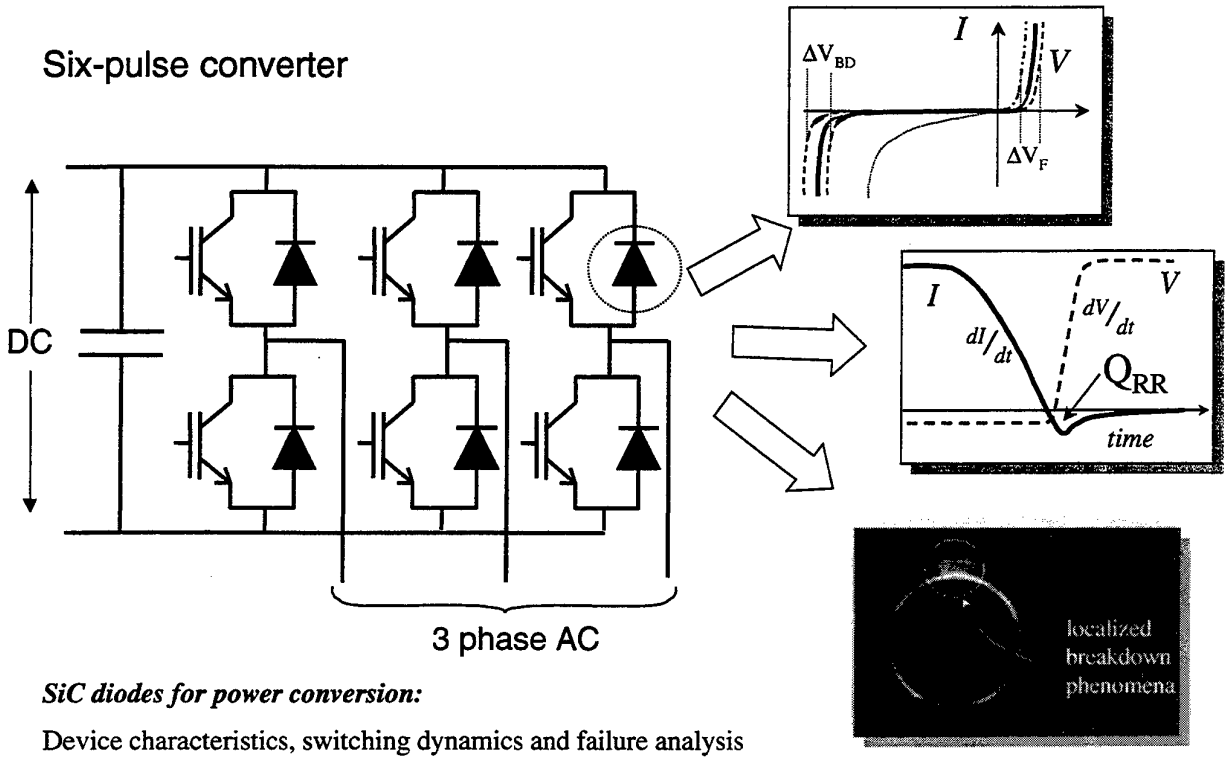
Silicon Carbide device technology is evolving from a vision to a real alternative to silicon devices. The feasibility of using SiC has been shown for many types of devices, the development of a production technology has started, where yield, reliability and costs are now the key issues. At present the high substrate prices keep the manufacturing costs of SiC making it very difficult to enter the device market with SiC on economic terms.

Targeted Applications: Traction, Transmission and Distribution
Prime applications are where SiC offers substantial benefits or even a technological breakthrough on the system level. The main application is power conversion where the latest development efforts on power switches (e.g. IGBT) allow utilization of much higher switching frequencies, putting very high demands on the free wheeling diode. The system performance is to a large extent limited by reverse recovery charge - a major source of switching losses.

Device concepts: JBS and PN diodes
Depending on the voltage range different device concepts are of interest. In the lower voltage range at about 1.7kV the Junction-Barrier-controlled-Schottky device is a promising candidate. It combines the low on-state losses of a unipolar device with the excellent blocking capability of a pn junction. The switching characteristics of such a device is shown to be close to ideal. At voltages beyond 2.5 kV the pn diodes is the best choice, as the on-state of a Schottky device suffers from the absence of conductivity modulation in the drift region. Different system requirements – e.g. surge current capability – make the pn junction superior to a Schottky device. Even for bipolar diodes the switching losses generated by the reverse recovery are only a very small fraction of a comparable Si device.

Technology development: Failure analysis and Variations
With the progress in the development the "best of all" result is becoming less important and reproducibility is the issue.
With a high number of defects, still an obstacle in SiC, failure analysis of dysfunctional devices needs to be established. High leakage / soft reverse characteristics are often encountered and can usually be attributed to localized defects. It is important to identify their origin to and separate process induced defects from those already present in the epilayers/substrates.
A powerful and non-destructive method to detect local field peaks and carrier multiplication is the Optical-Beam-Induced-Current method. With OBIC it is possible to image the electrical field distribution under reverse bias conditions to monitor the junction termination/passivation. In addition the spatial

distribution of the carrier multiplication can be extracted qualitatively to identify defects in the material giving rise to excess leakage current and premature breakdown.
In order to use the high power handling capabilities of SiC the reduction of the margins (e.g. in epilayer thickness and doping) is necessary. This requires narrow bandwidth of process and material variations. For parallel devices equal current sharing under static and dynamic conditions is a fundamental requirement from the system side. Top-down calculation gives material specifications, which the supplier has to meet.



SiC diodes for power conversion:

Device characteristics, switching dynamics and failure analysis

PROGRESS IN THE USE OF 4H-SIC SEMI-INSULATING WAFERS FOR MICROWAVE POWER MESFETs

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Semi-insulating (SI) 4H-Silicon Carbide wafers are a key requirement for the development of SiC microwave power devices and especially MESFETs. At present, the best results published show excellent power density (> 3.2 W/mm @ 10 GHz by Northrop Grumann) but in pulse mode (100µs, 10%). In CW, trapping phenomena have limited so far the best published power density on 4H SI SiC to < 1 W/mm @ 2.1GHz (by Cree Research) instead of the predicted 4-5 W/mm. In this work, we present improvements of the power density following the optimization of the epitaxial buffer design on a set of structures purchased from Cree Research. Power density as high as 2W/mm @ 2 GHz @ 80V biais has been obtained on structures with reduced current drift . A second buffer optimization has led to essentially current-drift-free devices whose microwave power results will be presented at the conference.

THE EFFECT OF SURFACE INHOMOGENEITY ON FORWARD I-V CHARACTERISTICS OF SIC SCHOTTKY BARRIER DIODES

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The physical parameters of SiC make it an attractive material for the fabrication of high power, high frequency Schottky Barrier Diodes. Good forward and reverse characteristics are vital to ensure optimal device performance. The effect of surface inhomogeneities on the reverse characteristics of Schottky barrier diodes has been described by Bhatnaghar et al. [1]. In this paper we describe and model non-ideal behaviour in the forward bias characteristic of Ti-Au Schottky Barrier Diodes on n-type 4H-SiC (epilayer doping $10^{16}cm^{-3}$).

Simple thermionic emission theory was shown to be the dominant current transport mechanism. The majority of the diodes produced using pure metals (Au, Ti, Pd, Pt) showed good agreement with this theory. However, Ti-Au diodes exhibited an anomalous step in the forward bias I-V characteristic. A model is described to explain this irregularity. An inhomogeneous interface with two phases having different barrier heights and different areas is modelled as an equivalent circuit consisting of two diodes in parallel. The parasitic resistance of the Schottky contact is included in the model as the diode internal resistance. One diode represents the bulk barrier height and area and the other diode represents a 'defect' region with a lower barrier height. The area of the 'defective' phase is defined as a fraction of the bulk area. PSPICE software is used to simulate this equivalent circuit (Fig 1).

Theoretical data is fitted to the experimental data by varying the parameters of each diode. Barrier height and ideality are estimated from the experimental results. The lower voltage region (<0.6V) of the diode characteristic is fitted by varying the ideality, barrier height, fractional area and internal resistance of the smaller area 'defect' diode. In the high current region, the I-V characteristic is dominated by the effect of the bulk diode. The barrier height, ideality and parasitic resistance of the bulk diode were altered to achieve good fit (Fig. 2). The extracted parameters provide estimates of the electrically active area of the 'defect'. For the diode of Fig. 2 a barrier height of 0.66eV and a fractional area of $5x10^{-4}$ were determined. The model has been used to simulate Schottky diode I-V characteristics between 25°C and 200°C. A good fit between the experimental data and simulated results was obtained over the full temperature range (Fig. 2).

In this sample, the Ti layer was extremely thin representing a 'flash' of perhaps 2nm thickness to enhance adhesion of the Au. It seems quite likely that the Ti was discontinuous and hence the two phases were due to Schottky contacts to Ti islands (the 'defect' regions) and Au infill (the bulk phase). The barrier heights inferred are quite consistent with the barriers found using CV on diodes with thick layers of Ti (0.56eV) and Au (1.27eV) where good ideality factors were observed.

Reference

M. Bhatnagar, B.J. Baliga, H.R. Kirk and G.A. Rozgonyi "Effect of Surface Inhomogeneities on the Electrical Characteristics of SiC Schottky Contacts", IEEE Transactions on Electron Devices, Vol 43, No.1, pp150 1996

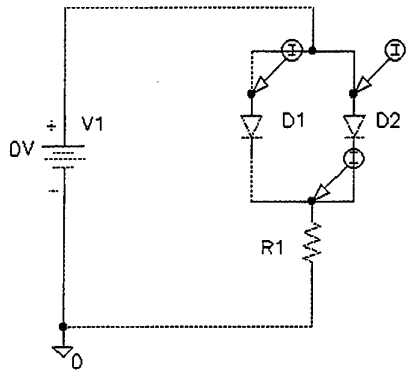

Fig1: Schematic of equivalent circuit used to simulate Schottky barrier diode with surface defects. Diode D1 represents the bulk of the Schottky diode and diode D2 represents the "defect" diode. R1 is resistance of the substrate. The area of this diode is expressed as a fraction of the bulk area. Each diode is characterised by thermionic emission and includes a parasitic series resistance.

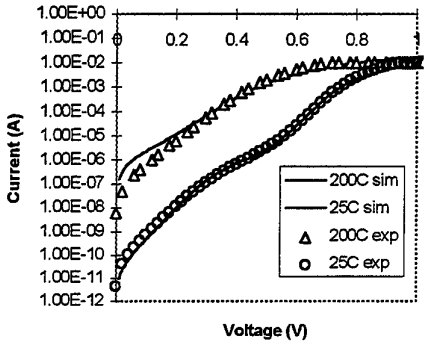

Fig 2: I-V characteristics of experimental and theoretical data.. The extracted parameters for D1 and D2 are n_1=1.3, ϕ_1=0.96eV, r_1=0.01Ωcm^2, n_2=1.3, ϕ_2=0.66eV, r_2=0.02Ωcm^2, where n is the ideality, ϕ is the barrier height and r is diode internal resistance. The extracted fractional area was $5x10^{-4}$.

EFFECTS OF SURFACE DEFECTS ON THE PERFORMANCE OF 4H- AND 6H-SiC PN JUNCTION DIODES

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Unique potential of SiC has been demonstrated in prototype devices projected to high-power, high-frequency, and high-temperature applications. Although micropipes have been claimed to degrade high-voltage blocking capability of SiC devices [1], it is still not clear what kind of defects adversely affect the SiC device performance. In SiC bipolar devices, major mysteries include large leakage current, at least several orders of magnitude higher than simple theoretical prediction and too fast switching characteristics (short minority carrier lifetime) in bipolar devices. In this paper, we reveal that surface recombination/generation governs the current conduction and switching behavior of SiC pn junction diodes. New insights on defects harmful to the diode performance are given.

4H- and 6H-SiC mesa pn diodes were fabricated with $p^+/p/n^-$ CVD epilayers grown on n^+-substrates in our group [2]. The net donor concentration of 12μm-thick N-doped n^- layers was determined to be $4\sim9\times10^{14}cm^{-3}$ by C-V measurements. Diodes were processed into a mesa structure, and the surface was passivated with thermal oxides formed by wet oxidation at 1150℃. The diode size was varied over a wide range from 60μm to 1200μm in diameter to investigate size effects.

Typical I-V characteristics of a 4H-SiC diode at room temperature are shown in Fig.1. The diode exhibited both a low on-resistance of $1.09m\Omega cm^2$ and a high blocking voltage of 1744V. Those of a 6H-SiC diode were $6.05m\Omega cm^2$ and 2022V. In semi-logarithmic I-V plots, the forward current was clearly divided into recombination (n=2) and diffusion (n=1) current components. Figure 2 depicts the perimeter-area (P/A) ratio dependence of the saturation current density of recombination current, revealing that major recombination occurs at the perimeter (sidewall of mesa) and not at the junction interface (bulk), especially in small diodes.

We made mapping of several different surface defects such as pits, hillocks, scratches on the epilayer surfaces, and investigated how each defect affect the reverse leakage and blocking voltage. We found that "triangular-shaped" surface defects cause severe increase of leakage current, but small round pits and scratches do not give direct impact on the reverse characteristics. Figure 3 demonstrates the P/A ratio dependence of the leakage current density at −100V of good 4H-SiC diodes without triangular-shaped surface defects at two different temperatures. The leakage current is proportional to the P/A ratio, indicating that the perimeter generation is responsible for the leakage. The almost zero intercept of the plot means that the bulk generation process via deep defect centers is negligible. Thermal activation of the perimeter generation results in the steeper slope at high temperature.

The authors also succeeded to separate bulk and perimeter contribution to minority carrier lifetime (τ), which was estimated from a reverse recovery switching analysis, as shown in Fig.4. This P/A ratio dependence of $1/\tau$ revealed that perimeter recombination is dominant in small diodes, in agreement with a recent work [3]. The bulk minority carrier (hole in this case) lifetime, which reflects the intrinsic material quality, was determined to be 0.33~0.39μs from the $1/\tau$ intercept. The slope of the plot yielded a surface recombination velocity of $3\sim5\times10^4$cm/s. Polytype dependencies of carrier lifetime and surface recombination velocity seemed to be small.

The present study has strongly demonstrated that surface or perimeter properties can limit SiC device performance, since the material quality of SiC epilayers has been improved to a high level. Surface passivation together with device-structure design may become a critical issue to extract the intrinsic potential of SiC in real devices.

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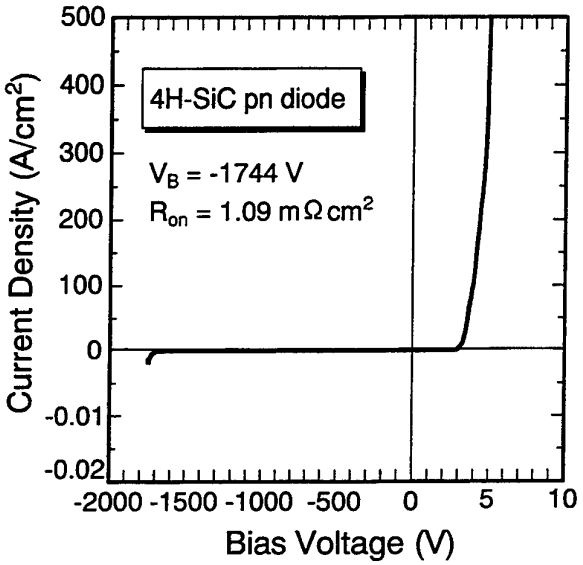

Fig.1 I-V characteristics of a 4H-SiC pn diode at room temperature.

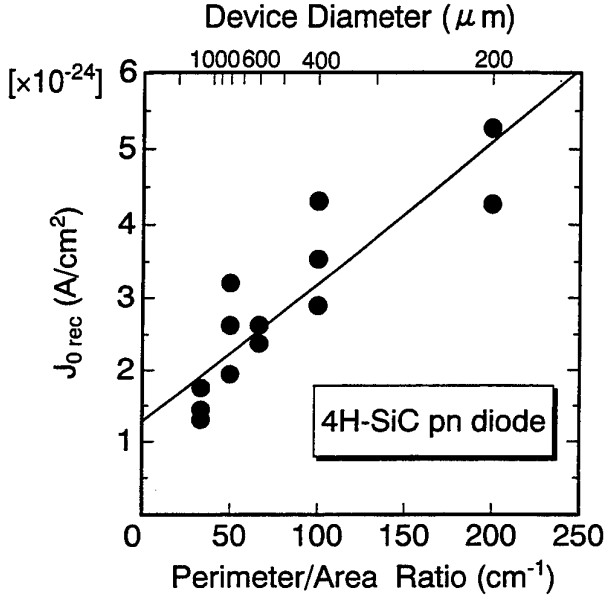

Fig.2 P/A ratio dependence of the saturation recombination current density ($J_{0\,rec}$) of 4H-SiC diodes.

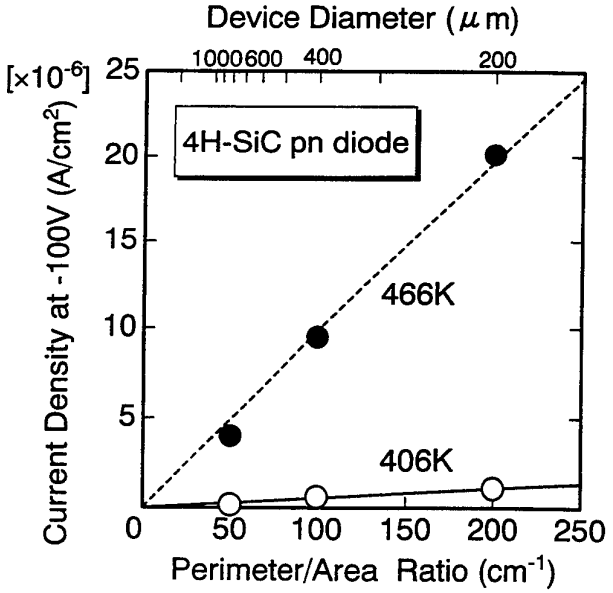

Fig.3 P/A ratio dependence of the leakage current density at –100V of good 4H-SiC diodes at two different temperatures.

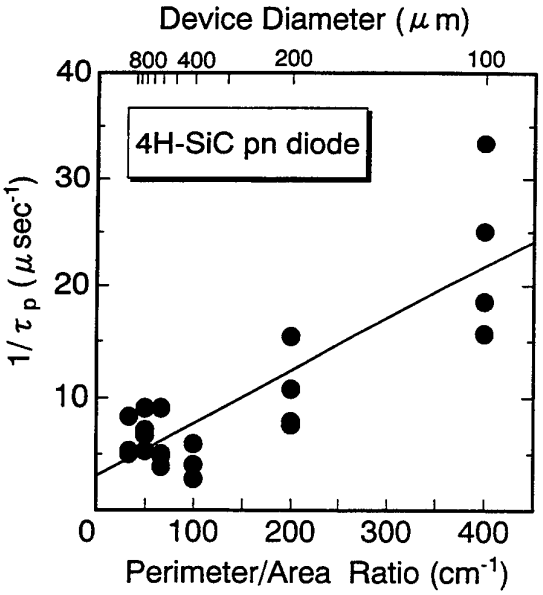

Fig.4 P/A ratio dependence of $1/\tau$ obtained for 4H-SiC pn diodes.

TEMPERATURE SENSORS BASED ON SIC PN-JUNCTION DIODES

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We describe here commercially available silicon carbide pn-junctions [1] tested as temperature sensors [2]. The pn-junctions are produced as ultraviolett photodetectors based on 300 x 300 μm dies. The devices have an epilayer of p-type SiC on a 250 μm n-type substrate. There are bond pads of gold 100 x 100 μm on the p-type epilayer and on the back of the device. The devices are glued by ceramic glue onto a ceramic heater, which is mounted with an air gap for thermal insulation on a 16 pin holder, see Fig. 1.

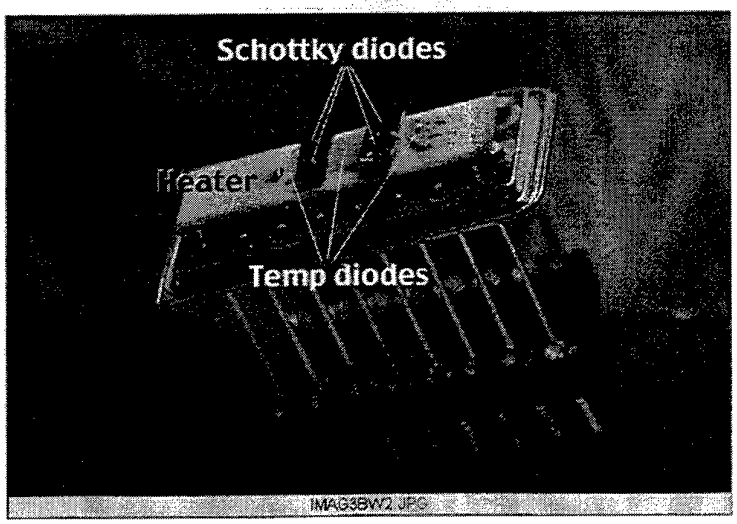


Fig. 1. The 16 pin holder with a heated ceramic substrate. The pn-junctions are used for temperature control of the ceramic substrate. Schottky diodes used as gas sensors are also mounted on the subsltrate.

The IV characteristics are close to ideal, see Fig. 2. About ten devices have been tested from RT to 600°C. The voltage at a constant current, 0.5 mA and 0.1 mA, versus temperature is linear and very similar for all tested devices. Figure 3 shows calibration curves performed by heating the sensors in an oven. The temperature versus voltage curves for the two current levels are not totally parallel. For a chosen current level the sensors are very similar, however, and only one calibration at RT is needed.

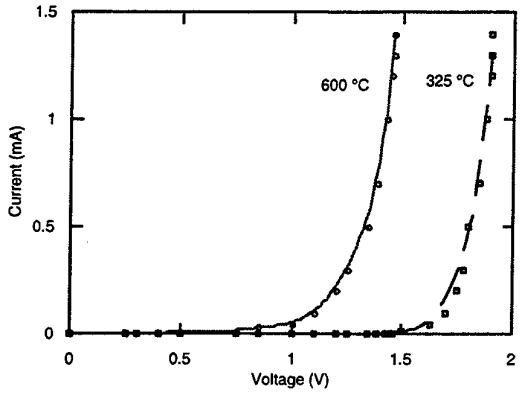
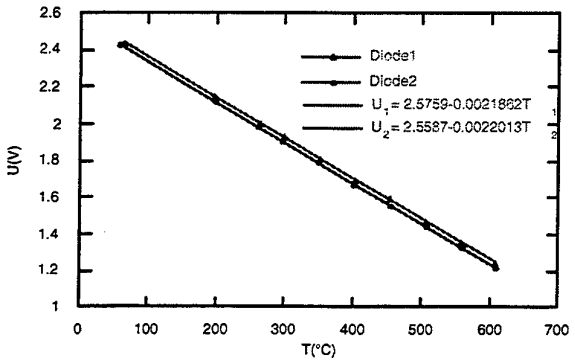
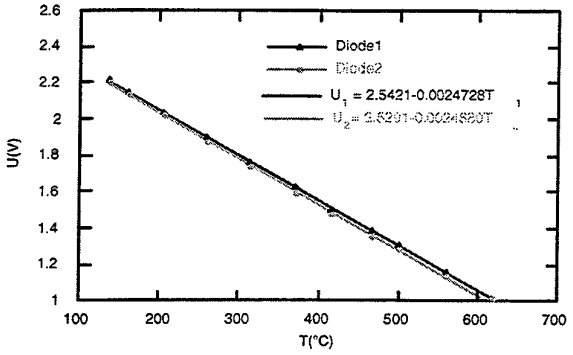


Fig. 2 The IV curves of a pn-junction used as a temperature sensor.



(a)



(b)

Fig. 3. The calibration curve for two pn-junctions mounted on a 16 pin holder. The voltage at (a) 0.5 mA and (b) 0.1 mA is measured. The calibration is performed in an oven. The equations for the calibration lines are:
(a)
$U_1=2.5759-0.0021862T_1$
$U_2=2.5587-0.0022013T_2$
(b)
$U_1=2.5421-0.0024728T_1$
$U_2=2.5291-0.0024880T_2$

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OXYGEN, OXYDATION
and
MOSFET APPLICATIONS

OXYGEN IN 6H SILICON CARBIDE: SHALLOW DONORS AND DEEP ACCEPTORS

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The presence of oxygen (O) in the growth ambient especially of sublimation techniques and its possible incorporation into the grown crystals drives the interest in the characterization of O in silicon carbide (SiC). In this paper, studies on O^+-implanted 6H SiC samples are reported.

N- and p-type CVD grown epitaxial layers [1] (N_D–N_A~$1\cdot10^{16}cm^{-3}$ to $8\cdot10^{16}cm^{-3}$ and N_A–N_D~$1\cdot10^{16}cm^{-3}$, respectively) were implanted with multiple O^+ profiles with a mean implanted O concentration varying from $3\cdot10^{15}cm^{-3}$ to $1\cdot10^{19}cm^{-3}$ to achieve a box profile to a depth of 1.1μm or 1.4μm; the implantations were conducted at a temperature of 300°C to avoid amorphization. The noble gas neon (Ne) was used as a reference implant to separate damage-induced defects from those related to O. Subsequent to the implantations, the epilayers were annealed up to 1650°C for 15min.

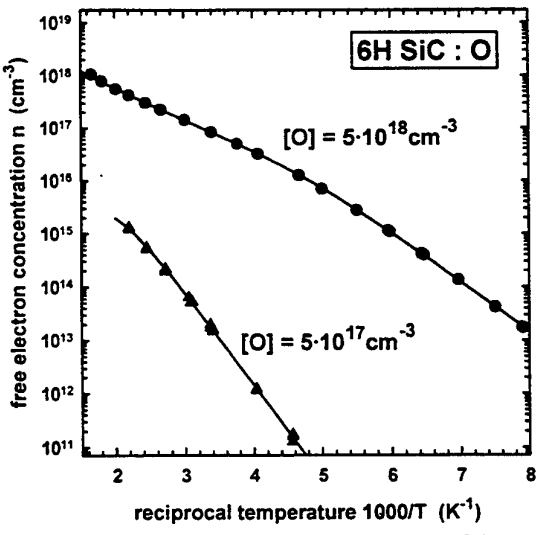

Fig. 1 Free electron concentration n(1/T) of the two O^+-implanted 6H SiC CVD epilayers.

The electrical and optical properties of O-related defect centers in 6H SiC were characterized by Hall effect and capacitance-voltage (C-V) measurements, admittance (AS) and deep level transient spectroscopy (DLTS) as well as by low temperature photoluminescence (LTPL).

Fig. 1 depicts results of Hall effect measurements taken on two O^+-implanted 6H SiC epilayers; the previously p-type epilayers (N_A–N_D~$1\cdot10^{16}cm^{-3}$) change their conductivity-type into n-type. Tab. I lists the defect parameters used for the fit of the neutrality equation to the experimental data points (circles and triangles). Two energy levels (O_{Ia}, O_{II} and O_{Ib}, O_{II}, respectively) are necessary for an adequate least-squares fit (solid lines in Fig. 1). The concentration of center O_{II} is about one order of magnitude greater than the concentration of centers O_{Ia} and O_{Ib}.

In addition, the formed total concentration of O-related defects does not linearly depend on the mean implanted O concentration.

Admittance spectra (not shown here) of O^+-implanted ([O]~$2\cdot10^{18}cm^{-3}$ to $1\cdot10^{19}cm^{-3}$) n-type 6H SiC epilayers reveal one main and two smaller O-related conductance peaks providing ionization energies of (145±8)meV, (242±12)meV and (352±18)meV, respectively, which correspond to the ionization energies

obtained by the Hall effect analysis. These peaks change their temperature positions and heights with differing implanted mean O concentrations.

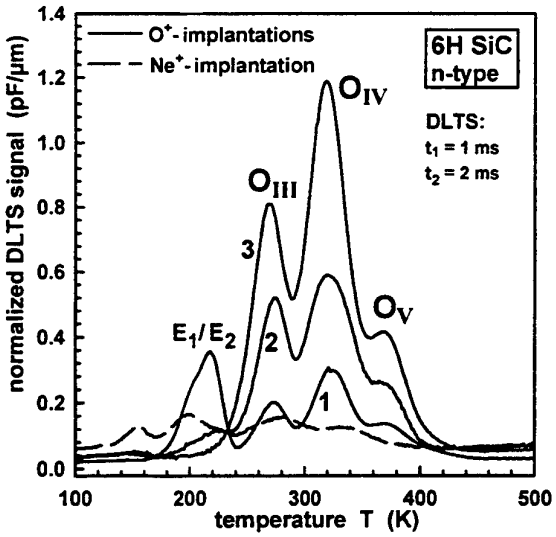

Fig. 2 Normalized DLTS signal as a function of temperature. The spectra are taken on O^+-implanted samples (solid curves 1 to 3) and on a Ne^+-implanted sample (dashed curve, [Ne]~$4\cdot10^{16}cm^{-3}$).
Curve 1: [O]~$3\cdot10^{15}cm^{-3}$, curve 2: [O]~$8\cdot10^{15}cm^{-3}$, curve 3: [O]~$4\cdot10^{16}cm^{-3}$.

Normalized DLTS spectra taken on n-type 6H SiC epilayers implanted with O^+ (solid curves 1 to 3) and Ne^+ (dashed curve, [Ne]~$4\cdot10^{16}cm^{-3}$), respectively, are shown in Fig. 2. Three peaks termed O_{III}, O_{IV}, and O_V are found; they increase in concentration with increasing mean implanted O concentration for low- to mid-fluences. Their concentration saturates at around $3\cdot10^{17}cm^{-3}$ for high-fluences ([O] up to $1\cdot10^{19}cm^{-3}$, not shown here). Clear-cut peaks at corresponding temperature positions could not be detected in DLTS spectra of Ne^+-implanted epilayers. Therefore, these three peaks are assigned to deep O-related centers; their ionization energies are: $\Delta E(O_{III})$=(478±23)meV, $\Delta E(O_{IV})$= (558±28)meV, and $\Delta E(O_V)$=(610±30)meV. Double-correlated DLTS measurements indicate an acceptor-like behavior of these deep O-related defect centers.

We like to point out that in the 4H polytype also two types of O-related centers (shallow donors and deep acceptors) have been observed [2]. Based on the Hall effect analysis there is experimental evidence that the shallow centers O_{Ia}, O_{Ib} and O_{II} do not consist of simple point defects, but of more complex defects like the "Thermal Oxygen Donors" in silicon. This suggestion is supported by the fact that the concentration ratio of O_{Ia} to O_{II} and O_{Ib} to O_{II} centers, respectively, is not identical with the ratio of inequivalent cubic to hexagonal lattice sites in the 6H polytype (equal to 2:1) and that the total concentration (O_{Ia}+O_{II} and O_{Ib}+O_{II}, respectively) does not linearly scale with the mean implanted O concentration. With respect to the chemical nature of the deep centers O_{III}, O_{IV} and O_V, we favor the same model as for the deep defects in 4H SiC, namely, that they are complexes consisting of oxygen and vacancies/interstitials, possibly similar to the A-center in Si.

In addition to the electrical investigations, LTPL spectra have been taken on all twenty O^+-implanted 6H SiC samples; it appears as if a number of strong LTPL lines, in the spectral range from ~8000Å to 10000Å, can be associated with oxygen by means of a mechanism which remains to be elucidated.

Tab. I Ionization energies and concentrations of shallow O donors, compensation and total donor concentration used to fit the neutrality equation to the experimental Hall data of Fig. 1.

[O] (cm^{-3})	$\Delta E(O_{Ia})$ (meV) $N(O_{Ia})$ (cm^{-3})	$\Delta E(O_{Ib})$ (meV) $N(O_{Ib})$ (cm^{-3})	$\Delta E(O_{II})$ (meV) $N(O_{II})$ (cm^{-3})	N_{comp} (cm^{-3})	N_{tot} (cm^{-3})
$5\cdot10^{18}$	167 $3.5\cdot10^{17}$	– –	255 $3.15\cdot10^{18}$	$2.3\cdot10^{16}$	$3.5\cdot10^{18}$
$5\cdot10^{17}$	– –	350 $5.4\cdot10^{15}$	260 $4.86\cdot10^{16}$	$5\cdot10^{16}$	$5.4\cdot10^{16}$

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QUALITY AND RELIABILITY OF WET AND DRY OXIDES ON N-TYPE 4H SiC

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Early work on thermal oxides on SiC showed a relatively poor quality oxide on p-type material as opposed to n-type. Following extensive study the quality of oxides on p-type has improved rapidly, whereas by contrast the less frequently studied oxide on n-type has shown little or no improvement in recent years. Most researchers investigating the SiO_2/SiC interface have chosen the MOS capacitor, with a large area front substrate contact as their characterisation structure[1]. However, the simple and fast fabrication process for this device does not subject the oxide to the subsequent processing steps required for actual power device production. Here we report on the quality and reliability of wet and dry oxides thermally grown on n-type 4H SiC, with the characterisation vehicle being an MOS capacitor with a full ohmic back contact.

All the oxide samples described here have used production grade 4H-SiC substrates purchased from Cree Research Inc. The wafers were 35mm in diameter and have an n-type doping of about $9x10^{18}cm^{-3}$, with a 3μm thick $2x10^{16}cm^{-3}$ n-type epitaxial layer. The wafers were cleaned in a FSI centrifugal spray cleaner using the B-clean and then either oxidised to a thickness of 20nm by dry oxidation at 1050°C or to a thickness of 25nm in pyrogenic steam also at 1050°C. A polysilicon/low temperature oxide (LTO) sandwich was then deposited onto the oxide by low pressure chemical vapour deposition to protect the gate oxide during ohmic contact formation. The backs of the wafers were etched clean and an ohmic contact formed by e-beam evaporation of 200nm Ni/580nm Au and annealed at 950°C in N_2 for 60seconds. The LTO and polysilicon were then etched from the front surface and a range of different area aluminium gates were finally formed using photolithography.

All measurements reported here were carried out on wafer using a hot chuck to obtain a maximum operating temperature of 200°C. Ramp IV measurements to breakdown were performed for 20 capacitors both at 25°C and 200°C; typical IV curves are seen for the dry and wet oxides in figures 1 & 2 respectively. The main feature of these curves is the shoulder seen in the IV data taken at 25°C. This is likely to be due to electron trapping in the oxide, field induced de-trapping at high fields returns the curve to the conventional Fowler-Nordheim tunnelling characteristic before breakdown (barrier height of ~2.8eV). The cumulative distribution of the catastrophic breakdown fields is plotted in a Weibull plot as figure 3. The dry oxide breakdown fields were higher than those for the wet oxides with an apparently intrinsic failure distribution seen for most capacitors. Similarly, charge to breakdown (Q_{BD}, figure 4) shows the superiority of the dry oxides. It should be noted that the Q_{BD} values for the dry oxides are not unreasonable as compared to metal gated Si capacitors, where values of 0.1-1C/cm^2 are typical. Time dependent dielectric breakdown (TDDB) was performed at the indicated applied fields and used to extrapolate a maximum operating field of ~5MV/cm for ten year lifetime at 25°C, figure 5. The AC conductance technique at 200°C was used to accurately extract the interface state density (D_{IT}) close to the conduction band edge. Figure 6 shows that there were no significant differences in D_{IT} between the wet and dry oxides, with values falling to ~$5x10^{15}m^{-2}eV^{-1}$ at 0.9eV

below the conduction band edge.

We have presented results on quality and reliability of both wet and dry thermal oxides grown on n-type 4H-SiC. It was shown that the number of interface states for both samples were very similar but that the high field reliability of the dry oxides was better than that of the wet oxides. This is in contrast to previous reports where wet oxides have been shown to have better quality than dry oxides[2]. The most likely explanation is that the post processing required to form ohmic back contacts, has resulted in the degradation of the quality and reliability of the wet oxides described here, indicating the desirability of carrying out SiC/SiO_2 research in a whole process context.

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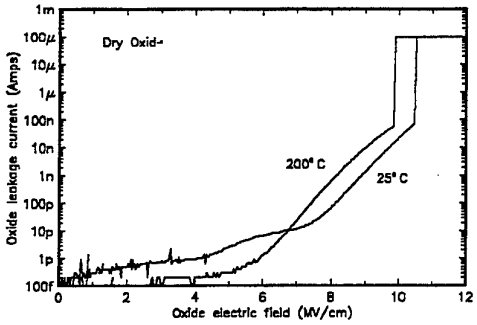

Figure 1; Ramp IV at 2 temperatures for dry oxide.

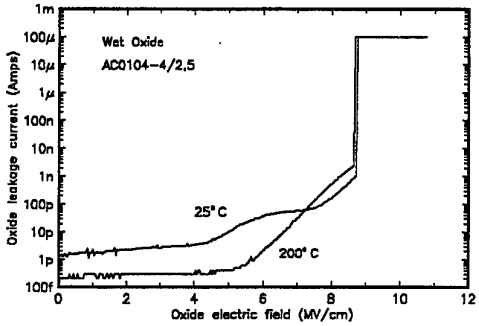

Figure 2; Ramp IV at 2 temperatures for wet oxide.

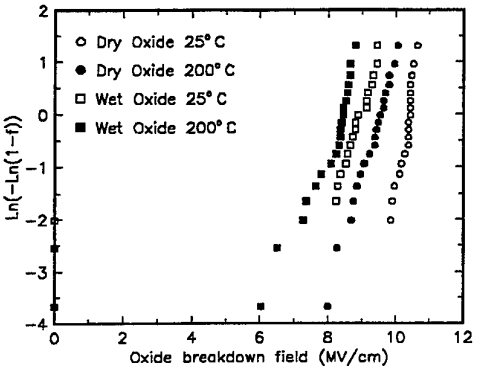

Figure 3; Weibull plot of ramp IV breakdown field

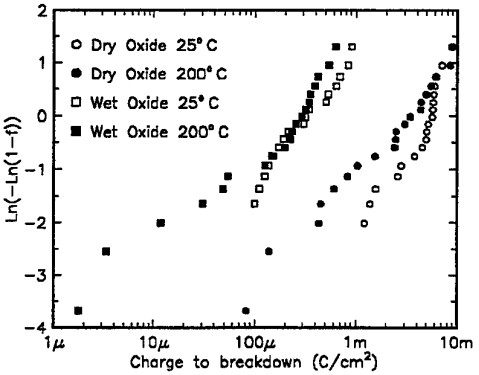

Figure 4; Weibull plot of ramp IV charge to breakdown

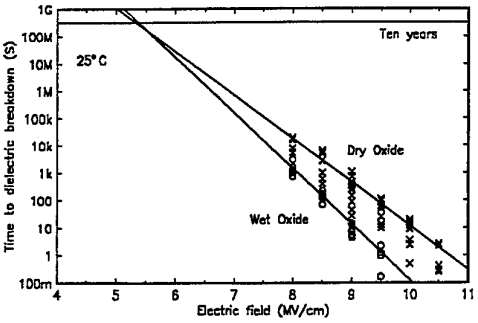

Figure 5; Constant voltage time to dielectric breakdown.

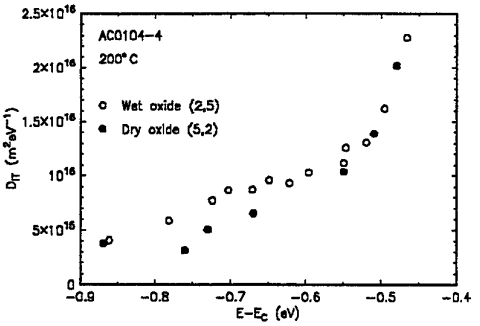

Figure 6; Interface state density from conductance measurement.

Structural Defect Visualization and Oxide Breakdown in SiC Wafers after Thermal Oxidation

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Experimental results of structural defect visualization and oxide breakdown in SiC wafers after thermal oxidation is presented. The experimental approach is based on the delineation of variations in structural homogeneity, polytypism, or doping concentration due to their strong influence on oxide growth velocity which results in a color contrast map in the SiC wafers due to variations in oxide thickness. Our experiments indicate that while bulk defects seem to have a long-range influence on the oxidation characteristics of the C-face of the SiC wafers, no apparent influence of the bulk defects is evident on the Si-face oxidation. However, defects such as polishing marks, which are present on the surface, clearly influences the Si-face oxidation process. Also, the oxide breakdown in MOS capacitor structures, fabricated on SiC wafers, indicates a clear correlation between the location of breakdown and the presence of structural defects in SiC wafers. The oxide breakdown under high applied fields, in the accumulation regime of the MOS capacitor structure, is observed to occur at locations corresponding to the edge of bulk structural defects in the SiC wafer such as polytype inclusions, regions of crystallographic mis-orientation, or different doping concentration. Breakdown measurements on more than 50 different MOS structures did not indicate any failure of the oxide exactly above a micropipe. The scatter in the oxide breakdown field across a 10mm x 10mm square area was about 50%, and the highest breakdown field obtained was close to 8 MV/cm.

MECHANISTIC MODEL FOR OXIDATION OF SiC

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It is now well established that different crystal faces of SiC oxidise at different rates resulting (for example) in uneven oxide thickness around an etched trench. The lowest/highest oxidation rates are observed on the so-called silicon/carbon faces (the $0001/000\bar{1}$ planes respectively) with an approximately linear increase in oxidation rate for planes between the two extremes. Dependency of oxidation rate on crystallographic plane is also observed in silicon where it is often explained by arguments based on the number of silicon-silicon bonds exposed to various crystal faces. As $0001/000\bar{1}$ planes have the same number of surface bonds but widely differing oxidation rates, such an explanation is not sufficient for SiC. This paper proposes a simple mechanistic model which predicts the oxidation rate at different crystal faces.

The crystal structure and proposed bonding of 4H-SiC is shown schematically in Figure 1 (with the z-axis scale greatly exaggerated for clarity). From the point of view of the proposed oxidation model, the important structural characteristic of all the hexagonal SiC structures is the absence of inversion symmetry along the z-axis of the chemical bonding between Si and C atoms. To explore the consequences of this on oxidation, consider oxygen molecules interacting with the crystal structure at the Si-face. The first stage of oxidation is oxygen atoms bonding to the Si atoms outside the crystal. The high electronegativity of the oxygen atoms will make the bond between the surface Si atoms and the back-surface C atoms (labelled α in Figure 1) less ionic and hence lower the bond energy. At the second stage of oxidation, the α-bond will be broken by the incoming oxygen resulting in a Si-O-C bond and further oxidation will then attack the C-Si bonds on the next layer (labelled β in Figure 1). The high electronegativity of the oxygen atom now in the α-bond position will increase the ionic nature of C-Si β-bonds which will be consequently strengthened. At the Si-face then, there are one weakened and three strengthened bonds resulting in an overall increase in the amount of energy that must be supplied by the oxidation process (i.e. the average activation energy of the process is increased). Subsequent oxidation of other layers can proceed by the same mechanism with CO being released from the structure as the oxidation of the bonds around each C atom is complete. At the C-face however, such a mechanism results in three weakened and one strengthened bond resulting in a lowering of the activation energy of the oxidation process. At other crystal faces, the proportion of weakened to strengthened bonds will be between these two extremes producing consequent intermediate oxidation rates. An quantitative test of the proposed model can be made by comparing the effect of this bond weakening with the activation energies for oxidation extracted from experimental data using a linear rate model. Figure

2 shows such a comparison in which the good agreement between the proposed model and observed oxidation data can be clearly seen.

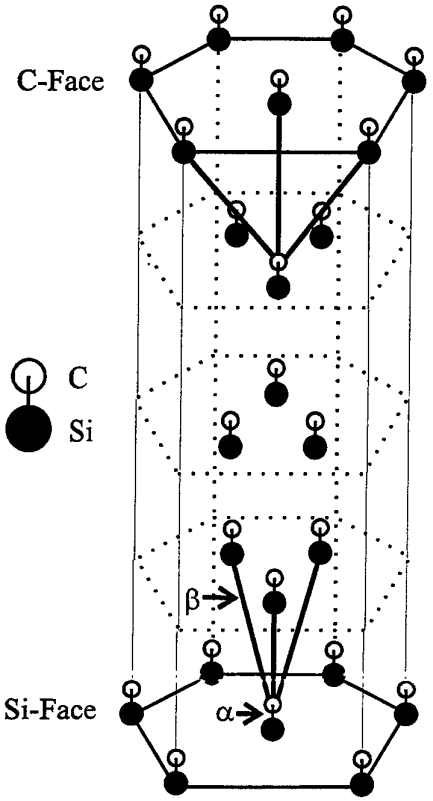

Figure 1: a schematic diagram of the crystal structure of 4H-SiC in which the z-axis (shown vertical in the diagram) is greatly exaggerated. The layer nature of the crystal is obvious with each layer corresponding approximately to one of the three stacking positions (traditionally labelled ABC) of hexagonal layer structures. The 4H-SiC structure shown is given by the stacking sequence ABCB with other polytypes built up from different stacking sequences (e.g. 6H-SiC ≡ ABCACB).

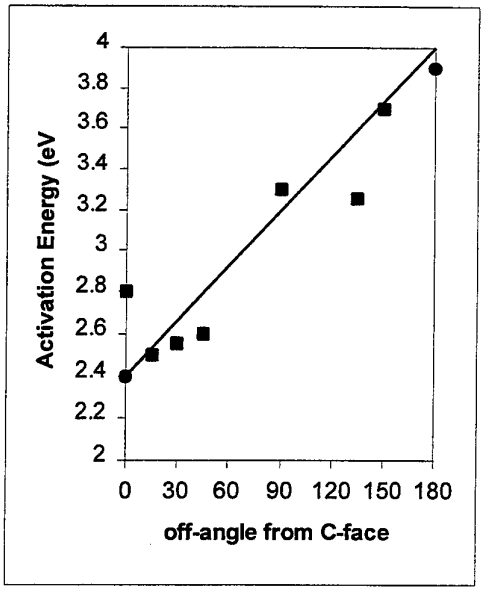

Figure 2: a graph illustrating a comparison between the observed dependency of oxidation rate with angle of crystallographic plane (from the C-Face) and that predicted by the proposed model (shown as solid line). Experimental data from [1] ■ symbol and [2] ● symbol.

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H_2 SURFACE TREATMENT FOR GATE-OXIDATION OF SiC MOSFETs

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I.INTRODUCTION

The oxidation process is very important for the formation of the SiC and SiO_2 interface for the application of MOSFETs. So far, we have shown that the wet cooling-off process after thermal oxidation is effective to reduce the interface state-density and have achieved good channel mobility in 6H-SiC MOSFETs[1]. Zetterling *et al.* have found that the surface pre-treatment by O_2 plasma before oxidation affects the *C-V* characteristics[2], which is considered to be mainly due to the removal of the residual carbon atoms on the surface. This indicates that the initial surface is important for the oxidation. On the other hand, Tsuchida *et al.*[3] have found that the wet-cleaning process cannot obtain the hydrogen-terminated surface on the SiC (0001) surface unlike silicon (111). They also pointed out that H_2 annealing over 800°C can get the atomically flat surface with hydrogen-termination in 6H-SiC (0001). We have adopted the H_2 treatment as the pre-cleaning for the gate oxidation of MOSFETs, and have achieved a high channel mobility 20cm^2/Vs in 4H-SiC MOSFETs.

II.EXPERIMENTAL

6H and 4H-SiC p-type epitaxial wafers were purchased from CREE research Inc. The acceptor concentration was around 2~3x$10^{16}cm^{-3}$. The gate oxidation was performed at 1100°C for 5 hours to grow 30nm oxide film. The aluminum was used as the gate electrode. The source and drain regions were formed by the nitrogen implantation at room temperature followed by 1300°C annealing. The channel length and width of the MOSFETs in the mask pattern were 100/150 μ m in order to neglect the process errors, such as the lateral spread of the ion-implanted impurities, or the photo-process. The H_2 treatment was performed just before the gate oxidation at 1000°C for 30min.

III.RESULTS AND DISCUSSIONS

The high-frequency *C-V* characteristics of the MOS diodes fabricated on the same chips of the MOSFETs are shown in figure 1. The *C-V* measurement was done at RT with the photo-induced method[4]. The net interface-state density (*Dit*) is estimated from the histeresis of the *C-V* characteristics. From fig,1, the extraction of *Dit* is difficult because the inversion region was not observed as the flat region of the *C-V* curve. Figure 2 shows the output characteristics of the MOSFETs with the different pre-treatment. The fact that the threshold voltage is higher in the device without H_2 treatment corresponds to the existence of the negative charges. The channel mobility was estimated from the transconductance in fig.2. As can be seen in fig.2, the steeper increase of the drain current in the sample with H_2 treatment indicates effectiveness of the surface treatment, and has achieved the channel mobility of $20cm^2/Vs$ at a peak. It is not uncertain for the physical reason that the higher channel mobility has achieved in the devices with relatively large *Dit* unlikely to 6H-SiC [1]. One reason might be due to the difference of the crystal quality between 6H- and 4H-SiC. These results show that the pre-treatment for the gate-oxidation is one of the important factors to control the interface character other than the oxidation process.

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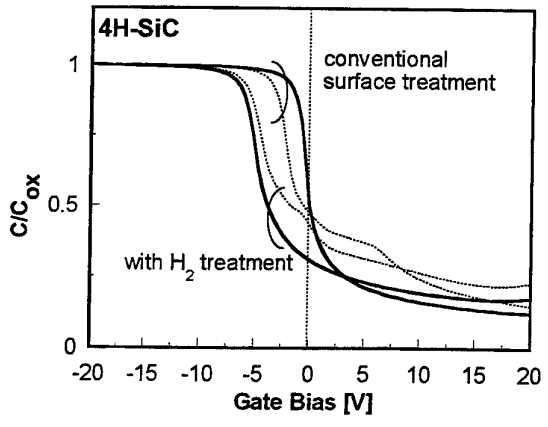

Figure 1 *C-V* characteristics by photo-induced method

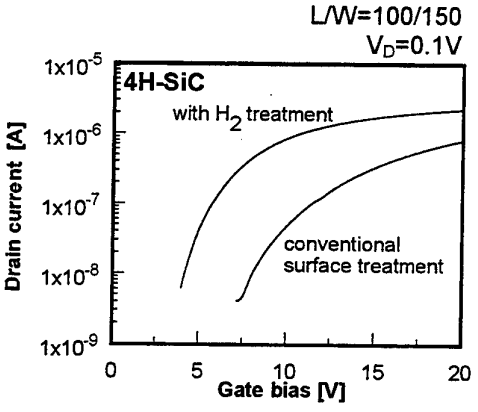

Figure 2 Comparison of the output characteristics of MOSFETs with differently processed

CUBIC SiC

Cubic Silicon Carbide Surface Reconstructions: from Atomic Control to Self-Organized Atomic Lines

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The atomic geometry of β-SiC(100) surface reconstructions is investigated by i) atom-resolved scanning tunneling microscopy and spectroscopy (STM, STS) from 25°C to 900°C, ii) core level and valence band photoemission spectroscopies using synchrotron radiation, iii) state-of-the-art STM image simulations and iv) *ab-initio* total energy DMol calculations using the LDF approach. The results reveal that, contrary to previous beliefs, it is possible to grow high quality (100) surfaces.

The β-SiC(100)3x2 reconstruction exhibits a low density of defects with first identification of individual Si atoms and dimers. Si-Si dimers form rows perpendicular to the dimer direction in a (3x2) atomic arrangement with clear evidence of asymmetric dimers all tilted in the same direction (i.e. not anticorrelated). Several types of defects are identified including primarily missing dimers and dimer pairs. Additional Si is grown epitaxially with two dimensional island formation having the (3x2) reconstruction [1].

STM also provides the first direct observation of a β-SiC(100) c(4x2) surface reconstruction. Individual Si-dimers are identified to form a centered pseudo-hexagonal pattern giving a c(4x2) array. Further support for Si-dimer identification is provided by theoretical STM image calculations. The results suggest a model of dimer rows having alternatively up- and down-dimers (AUDD) within the row, in an "undulating" type of arrangement reducing the very large surface stress [2]. Hence, the β-SiC(100)- and Si(100)-c(4x2) surface reconstructions are very different. A reversible temperature-dependent phase transition from a semiconducting c(4x2) surface at 25°C to a metallic 2x1 structure at 400°C is observed using STM. This transition results from temperature-induced disruption of the c(4x2) structure composed of alternately up- and down-dimers (AUDD model) into a structure having all dimers at the same height giving a 2x1 symmetry. This arrangement favors electronic orbital overlap between Si top surface atoms leading to surface metallization [3].

The discovery of self-organized Si atomic lines having fascinating characteristics will also be described. These sub-nanostructures are i) very stable up to ≈ 900°C, ii) very straight, iii) very long (> 1000 Å) with a length limited by the substrate only, iv) made of Si-Si dimers and v) result from selective Si atom elimination and/or organization. Their number and spacing could be mediated by annealing time and temperature leading to surface ordering ranging from a large superlattice to a single isolated atomic line. All these characteristics, which are of strong interest for nanotechnologies, are unprecedented [4].

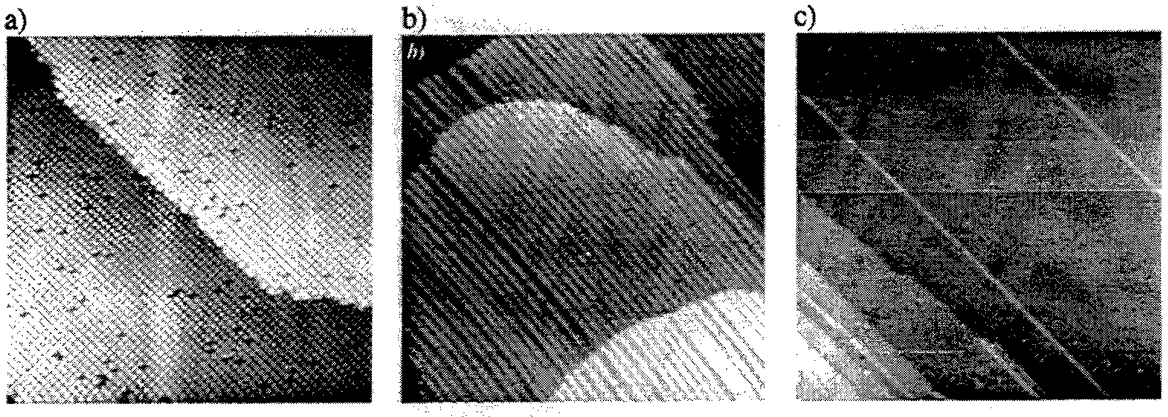

Fig. 1: STM topographs of **a)** β-SiC(100)3x2 surface (200 Å x 200 Å) **b)** Si atomic lines forming a superlattice (800 Å x 800 Å) and **c)** isolated Si atomic lines on a β-SiC(100) c(4x2) surface (800 Å x 800 Å).

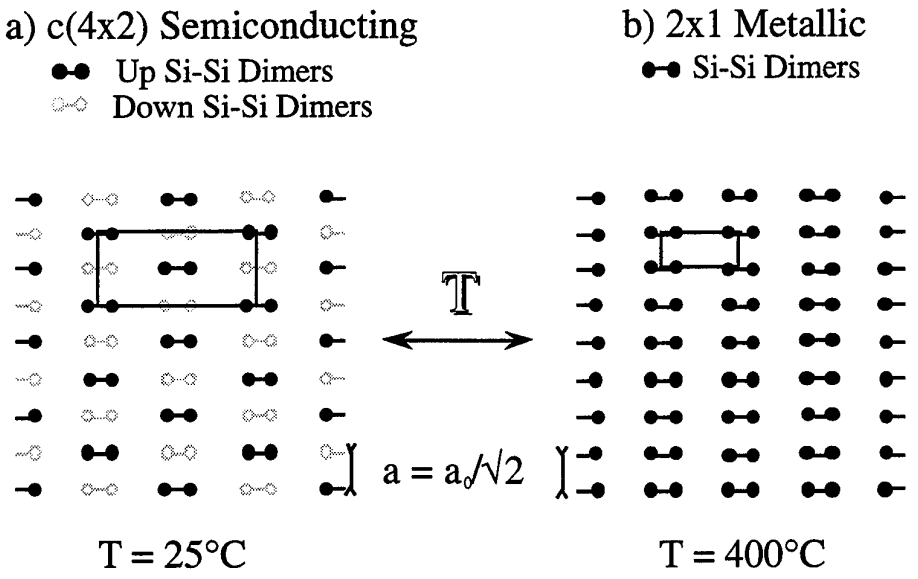

Fig. 2: Schematic of the temperature-induced semiconducting c(4x2) ⇔ metallic 2x1 reversible phase transition on the β-SiC(100) surface with **a)** dimer rows of up- and down-dimers (AUDD) at 25°C to **b)** all dimers at the same height at 400°C. The corresponding surface unit cells are also indicated.

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HETEROEPITAXIAL GROWTH OF 3C-SIC ON SOI FOR SENSOR APPLICATIONS
(invited)

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Modern automotive and aerospace engine control systems increasingly require sensors capable for the application at high temperatures or in otherwise harsh environments [1]. Typical examples are high temperature pressure sensors for combustion pressure based engine management, diesel peak pressure control, closed loop regulation of turbo chargers with variable geometry and jet turbine control systems, high temperature mass flow sensors for measuring exhaust gas recirculation rates and fast exhaust gas sensors for the cylinder specific regulation of emissions. The present paper will give an overview of these applications. The interplay of packaging and chip technologies will be demonstrated on the example of a combustion pressure sensor. Fig. 1 summarises the maximum operating temperatures depending on packaging and chip technologies and the influence of these on price, life and reliability. It shows, that sensors based on SiCOIN (SiC on Insulator) technology are predicted to be the best alternative for applications above 350°C medium temperature concerning price, life and reliability aspects.

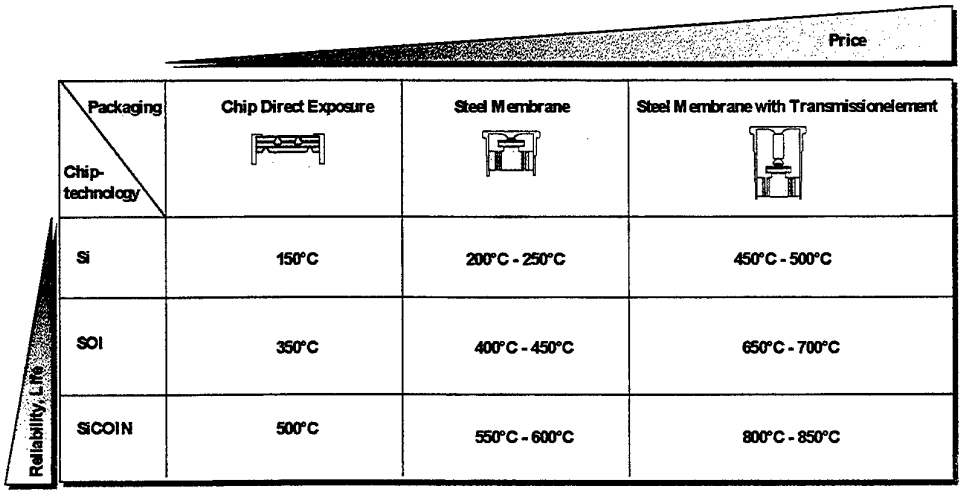

Fig. 1 Summary of different high temperature packaging and chip technologies in the case of pressure sensors

The application in commercial sensors requires that SiCOIN substrates are available with high quality and reasonable sizes and prizes. Recently at Daimler Benz a low temperature growth process for 3C-SiC was developed, having the potential to become a production process for SiCOIN substrates [2,3]. This will be described in detail at the conference and an overview concerning the electrical, structural and sensorial data of the material will be given. At Daimler Benz a 4" deposition system for ß-SiC was developed [4] and presently the SiCOIN deposition process is adapted to this. A forecast of commercial availability and price of 4" SiCOIN substrates will be tried.
As a first pilot application within a German/Swiss consortium a combustion pressure sensor based on SiCOIN substrates was developed. Fig. 2 gives an overview of the design of this sensor [5,6]. Results gained from engine test stand measurements will be presented at the conference.

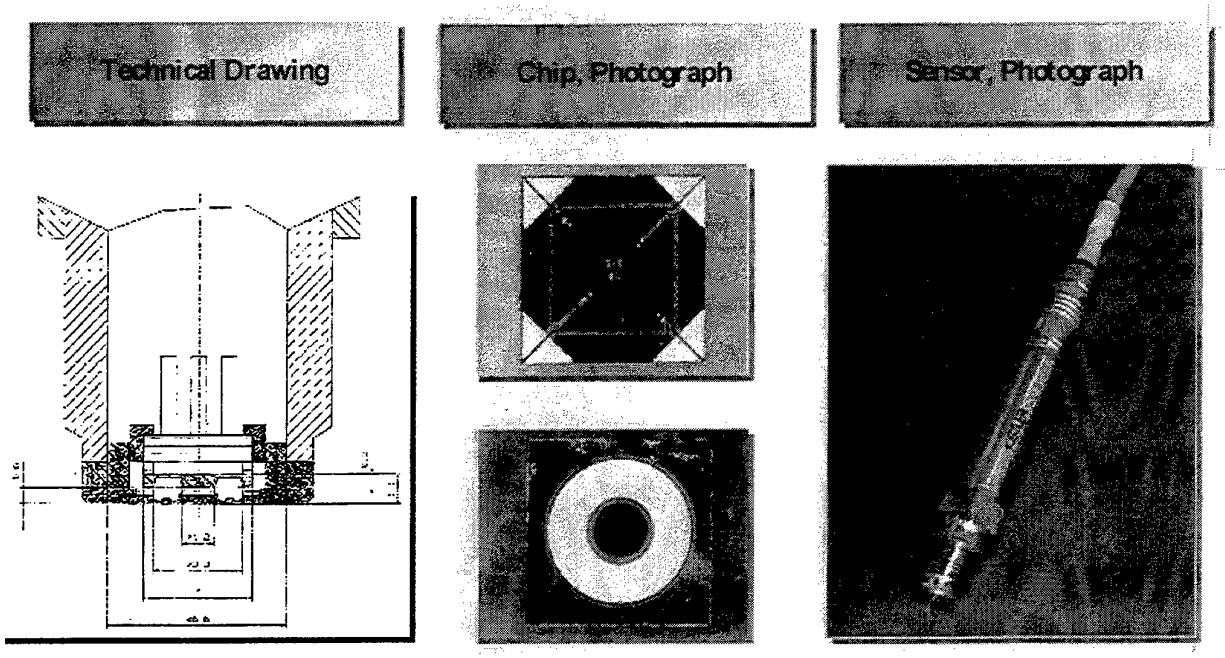

Fig. 2 Combustion Pressure Sensor [5,6]

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Surface modification of Si substrate for 3C-SiC growth

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The heteroepitaxial growth of cubic silicon carbide (β -SiC) on a Si substrate has been drawing much attentions because the growing technology makes it possible to supply large area SiC wafers at low cost. Silicon carbide films were epitaxially grown on Si substrate whose surface was modified with SiN_x and TiC buffer layers. The structure quality and morphologies of SiC films grown at various growth parameters were extensively investigated using XRD, SEM, TEM, FTIR, Raman spectroscopy.

SiN_x was formed on Si substrate by nitriding Si surface at 1050℃ in a mixed gas of 1000sccm NH_3 and 500sccm H_2 for 60min as shown in Fig. 1. XPS spectra of O(1s), N(1s), and Si(2p) are observed from the surface of Si(111) after the nitridation for 60 min. The peak of the chemical shift of Si(2p) can be decomposed into two peaks at 103.2 and 102.1 eV as shown in Fig. 1(b), which are equivalent to the reported binding energies of Si(2p) in SiO_2 and Si_3N_4 which are 103.4 and 101.9 eV, respectively.

3C-SiC(111) films were epitaxially grown on SiN_x/Si and TiC/Si substrates at 1250℃ for 30min in a RF-induction heated CVD reactor as shown in Fig. 2. Although voids were formed in the silicon side of the SiC/Si interface for SiC film grown on pure Si

substrate, the nitrided Si substrate accommodated the growth of SiC film with a flat and smooth film/substrate interface without the formation of voids. SiC film grown on Si substrate nitrided with NH_3 has better crystalline quality rather than that on pure Si substrate. SiC film grown on the nitrided Si substrate appeared to be n-type with the carrier concentration of 1.5×10^{17} cm^{-3}, and the electron mobility of 358 $cm^2/V \cdot s$.

The mechanism of void formation was extensively discussed in this paper. TiC buffer layers were deposited on Si substrate by RF-magnetron sputtering. The growth of SiC films on Si substrate whose surface was modified with TiC was also investigated to examine the crystal quality of the films. We observed the growth of void free SiC film with a flat and smooth film/substrate interface and the great improvements in the electrical and crystalline properties of the films grown on surface modified Si substrates.

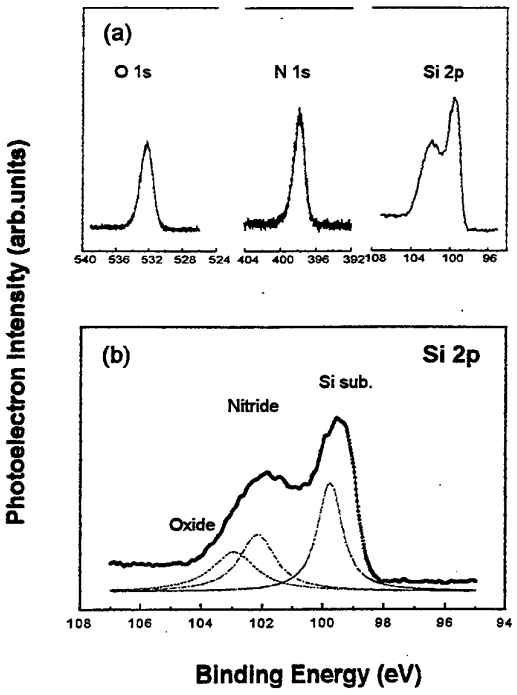

Figure 1. XPS spectra of Si(2p), N(1s), O(1s) from the surface of Si substrate after the nitridation for 60min at 1050℃ with 1000 sccm NH_3 and 500sccm H_2 flow.

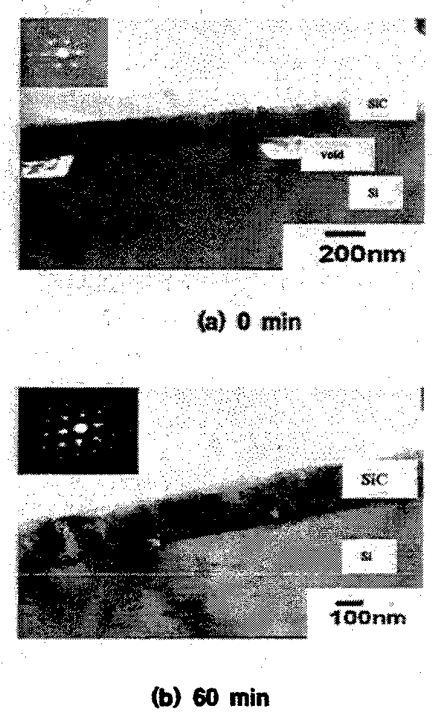

Figure 2. Cross-sectional TEM micrographs and TED patterns of 3C-SiC films grown at 1250℃ and 10torr for 30min. (a) before nitridation and (b) after nitridation.

Title STABILIZATION OF THE 3C-SiC/SOI SYSTEM BY AN INTERMEDIATE Si_3N_4 LAYER

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The development of sensor devices based on 3C-SiC epitaxially grown on Silicon On Insulator (SOI) is very attractive because the SiC/SOI system combines high temperature capabilities with easy micromachining processing which permits the development of sensors for operating temperatures up to 500°C [1,2]. Epitaxial growth of 3C-SiC on Si by atmospheric CVD occurs around 1350°C which results in instability of the SOI structure and the formation of very large cavities in the Si overlayer (SOL) which are extended in the buried oxide layer (BOX) [3]. The instability increases, as the thickness of the SOL is reduced.
The cavities are formed due to Si migration from the SOL to the surface in order to form SiC [4-6]. The SOL is the Si supplier for the formation of SiC, whereas the buried oxide layer (BOX) acts as a barrier for Si migration from the substrate. Therefore the cavities are extended laterally into the Si-overlayer. In addition significant redistribution of Si in the SOL occurs at the edge of the cavities due to the poor wetting of the Si at high temperatures on the SiO_2. A wetting angle of 87° is experimentally observed at the Si melting temperature between Si and SiO_2 [7], which renders wetting possible but extremely unstable since at 90° the Si-overlayer is beading up. This explains the significant ball up of the SOL at the edges of the cavities in the 3C-SiC/SOI system, as shown in the cross-section transmission electron micrograph (TEM) in Fig.1. In contrast, the wetting angle of silicon on silicon nitride is much lower, 25°. Therefore if an intermediate thin Si_3N_4 layer, about 5nm thick, is formed between the SOL and the BOX the stability of the SOI structure will be substantially improved [7].

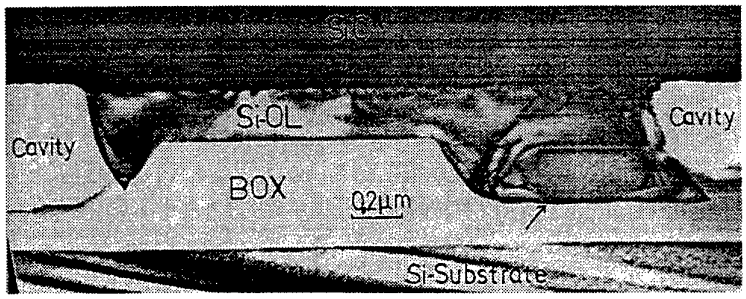

Fig.1: The BOX (buried oxide layer) of a UNIBOND wafer is damaged during SiC deposition. Cavities are formed which extend into the BOX. Due to the poor wetting of Si on SiO_2, a ball up of the silicon overlayer (SOL) can be observed at the edges of the cavities.

In this contribution the formation of a thin Si_3N_4 layer at the SOL/BOX interface is discussed and preliminary results on the stability of the 3C-SiC/SOI system are shown.
In order to form the thin Si_3N_4 layer, four samples (A-D) were implanted with nitrogen with different doses and different energies at 500°C (Table 1).

Table 1: N-implantation parameters for UNIBOND samples (SOL thickness: 200nm, BOX thickness: 400 nm)

		sample A	B	C	D
dose	[cm^{-2}]	2E16	5E16	1E17	1E17
energy	[keV]	80	80	80	180
expected depth of N-concentration maximum (as implanted)	[nm]	200	200	200	400
thickness of oxynitride-layer after annealing (at 1100°C) (SOL/BOX interface)	[nm]	not detectable	2	2 + 4.5	4.5

After the deposition of a 150 nm thick PECVD SiO_2 capping layer, the implanted samples were annealed for two hours at 1100°C in a nitrogen atmosphere. The energy of 80 keV resulted in a maximum N-concentration directly at the interface SOL/BOX. The energy of 180 keV led to a maximum N-concentration in the centre of the BOX, possibly allowing to form Si_3N_4 layers at both interfaces by diffusion of nitrogen through the BOX. SIMS analyses of the as-implanted and the annealed samples will be presented, showing the redistribution of nitrogen after annealing and the formation of the nitride layers. As can be seen in the TEM micrograph in Figure 2, a continuos intermediate layer was successfully formed.

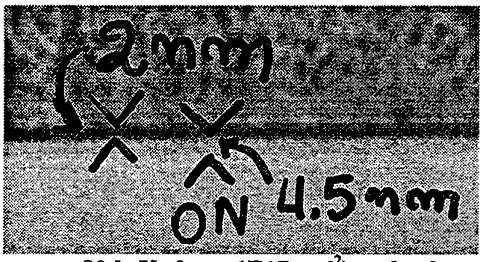

Fig.2: N-implantation at 500°C (energy: 80 keV, dose: 1E17 cm^{-2}) and subsequent annealing at 1100°C for two hours in nitrogen atmosphere produced a 4.5nm thick oxynitride layer and an additional 2nm thick layer (most likely silicon nitride) at the interface SOL/BOX of a UNIBOND wafer.

After having removed the SiO_2 capping layer, a 3C-SiC film 2µm thick was deposited at 1200°C in a LPCVD reactor using methylsilane [8] on a 200nm thick Si-overlayer (SOL) of a UNIBOND wafer, in which a 6nm thin Si_3N_4 layer was formed at the back side of the SOL. In this case very few cavities were formed in the Si-overlayer. When they appear they do not deeply extend into the BOX because the thin Si_3N_4 layer acts as barrier. In some cases the SOL was completely consumed and replaced by SiC. However the Si_3N_4 layer and the BOX remained intact revealing the enhanced stability of the SiC/SOI system due to the Si_3N_4 intermediate layer. Details on the structural characteristics of the SiC/SOI system stabilized by Si_3N_4 will be presented in this contribution.

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POSTER SESSION 1

INFLUENCE OF DIFFERENT GROWTH PARAMETERS AND RELATED CONDITIONS ON THE 6H-SiC CRYSTAL GROWTH BY THE MODIFIED LELY METHOD

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To improve the yield of high quality large diameter 6H- SiC single crystals grown by the Modified Lely Method it is necessary to investigate the interaction of different growth parameters. Beside the quality of the seed crystal the stoichiometry of the vapour phase and the thermal conditions inside the growth chamber have to be carefully controlled.
Especially, the growth rate of the crystal is determined by the growth temperature, the temperature gradient, the distance between source and seed, the pressure inside the crucible, the stoichiometry and grain size of the SiC-source.
Crystals of about 1 inch diameter were grown in an inductive heated furnace in a temperature range of 2200-2400°C. The argon pressure varied between 5 and 100 mbar. The growth rate was investigated in dependence of the growth time, the seed temperature, the temperature difference between source and seed and the system pressure. Using the method of marking the phase boundary by doping marks[1] the growth rate was determined for different pressures within one and the same growth run.
It was found that the growth rate strongly increases with the seed temperature and the temperature difference between seed and source while the growth rate decreases with the growth time. Furthermore, we found an anomalous behaviour of the growth rate in dependence of the pressure. It could be explained by an overcompensation of the pressure effect by the stoichiometry influence in the first part of the growth time.

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Influence of the growth conditions on the defect formation in SiC ingots.

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1 inch SiC ingots have been grown by the Modified Lely Method (MLM)[1-3]. A set up with inductive heating was used. A temperature gradient controlled by inductor position was changed during the growth process: inversion of the temperature gradient resulted in "in situ" etching of the seed. High purity green SiC powder used as the source. To eliminate the contamination of the seed surface by contaminants contained in the powder, etching of the powder in the acid and than washing and annealing was used.

Influence of the growth rate at the beginning of the growth process has been investigated. As it was shown earlier, pyramidal holes was formed at the interface (Fig.1) [1]. These defects can be explained by island growth mechanism. Decrease in growth rate at the beginning allowed to decrease the height and the number of pyramidal holes. As it known pinholes starts at the interface seed-ingot. Pinhole density depended on the interface quality. If the number of defects at the interface increased , pinhole density was also increased. Growth process consisted of the growth with small temperature gradient at the beginning and than increase in temperature gradient allowed to improve the interface and decrease the pinholes density.

Macrodefects (MD) formation has also been investigated. MD-hollow defects started at the interface seed-graphite lid, with enlargement at the end have also been investigated. MD formation depended on the temperature gradient in the growing crystal. In some cases MD grow in parallel axe (0001)C in other cases they leave the crystal near the seed (Fig.2). MD formation depended on the geometrie of the crucible, temperature gradient in the crystal and the temperature gradient seed-graphite lid.

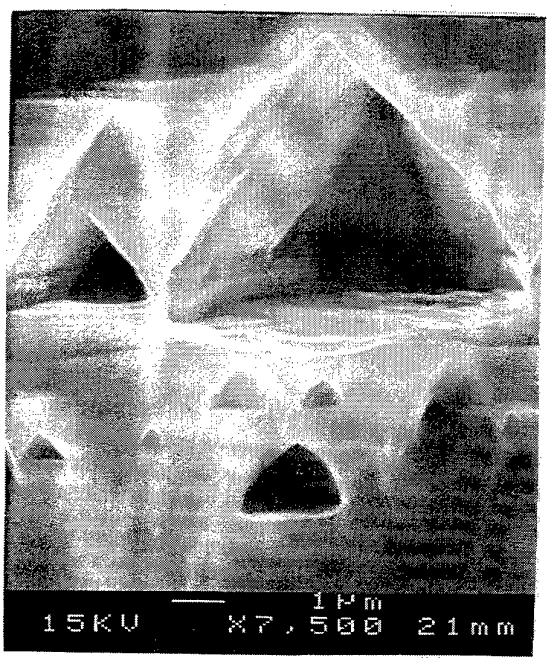

Fig1 Interface seed-ingot

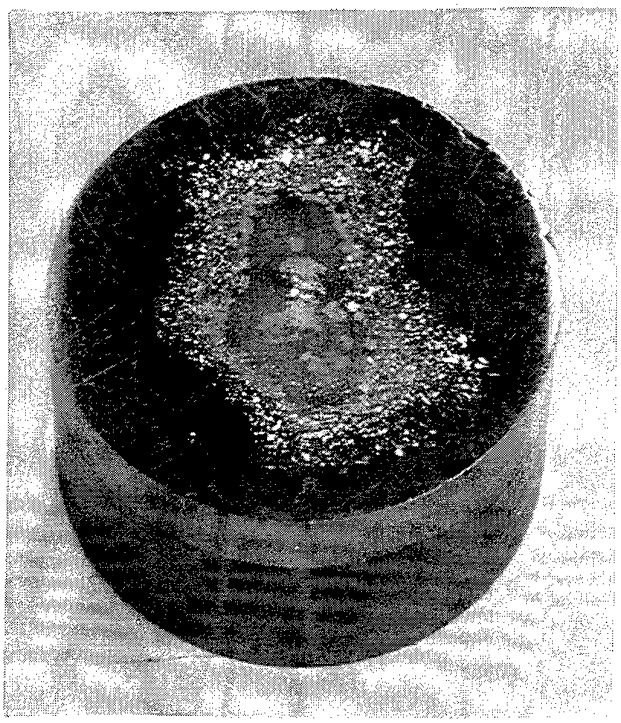

Fig 2 MD at the interface mono-poly SiC

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FEATURES OF SIC SINGLECRYSTALS GROWTH IN VACUUM BY THE LETI METHOD

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Introduction

The silicon carbide monocrystals appear to be a basis of substrates manufacturing for creation of extreme electronics semiconductor devices and number of sensors. Such substrates are perspective as a basis for manufacturing of devices on a basis of Ga and Al nitrides. For today the basic method of such crystals preparing is the LETI method [1].

One of the ways of singlecrystals by the LETI method preparing is the growth in vacuum (range of pressure of 10^{-3}-10^{-5} mm Hg). The growth of low doped crystals, and crystals, doped by aluminium [2] is most perspective on this direction. Low doped silicon carbide is also a basis for preparing of semiinsulating silicon carbide by doping it during growth by vanadium.

Physico-chemical features of growth and doping of monocrystals by aluminium

During growth of silicon carbide monocrystals by the LETI method the basic constructional material of the high-temperature furnace and growth cell is the graphite. The research of silicon carbide monocrystals growth processes in vacuum with use of graphite of various density has allowed to reveal optimal kinds of graphite by density and structure for manufacturing of growth cells.

The growth process of silicon carbide monocrystals, doped by aluminium, requires introduction of this element into the volume of growth cell. The physico-chemical phenomena accompanying doping process of silicon carbide monocrystals by aluminium are considered proceeding from thermodynamic representations about structure of a vapour/gas phase in Si-C-Al system [3].

The practical research has shown, that the introduction of metallic Al into a growth cell results in sharp deterioration of quality of grown crystals. The reception of aluminium doped SiC monocrystals by the LETI method lays on a way of using of doped by Al silicon carbide as a growth source. The influence of aluminium contents in a growth source on an impurity concentration in a grown monocrystal is investigated in the given work.

The following problem is a unity of monocrystal's doping. The basic kinds of heterogeneity doping, connected with orientation of monocrystal growth front and loss of aluminium in a growth cell, are investigated. The essential role of quality of graphite used for manufacturing of growth cells for the decision of the given problems is shown.

Polytypes and features of monocrystal's growth and doping

Under growth of monocrystal ingots by the LETI method the greatest interest is really represented only by two of them: 6H and 4H.

The physico-chemical features of polytypes impose the certain requirements of their growth conditions. At the same time the growth conditions create the preconditions for the certain restrictions, putted on levels of doping by that or other element, or promote amplification of overcompensation processes.

In this work the doping processes of silicon carbide monocrystals are considered under growth in vacuum. The connection of polytype structure of growing monocrystals with crystallographic orientation of growth front is shown. In this connection it is shown, that the polytype structure of growing in vacuum crystals appears to be connected with a doping level and conductivity type of growing crystals. For example strongly doped 4H-SiC monocrystals of p-type conductivity managed to be received only under growth from prismatic sides.

Studying of overgrowth processes with traditionally guided front of growth ((0001) Si and (0001) C) there was not observed any features connected with a polytype. Under growth of 4H polytype monocrystals from prismatic sides the phenomenon of polytype heterogeneity of overgrowing areas in directions (0001) Si and (0001) C was observed. As well as under growth of SiC crystals with growth front orientation (0001) C-sides expanded keeping a polytype 4H, while Si-side expanded, having polytype structure 6H, that has shown by x-ray difractometry analysis.

The electrical characteristics of growing crystals

The electrophysical characteristics of growing monocrystals were investigated by a Hall method, definition of specific resistance in a temperature range of 100-800 K, and also C-V-characteristics. The results of research of samples of different polytypes and types of conductivity will be submitted in the report.

Conclusion

Thus, the growth of silicon carbide crystals in vacuum allows to receive a substrate material of 6Í and 4H polytypes n and p-type conductivity by the appropriate selection of a constructional material, doping conditions and crystallography orientation of growing surface.

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STATE-OF-THE-ART OF DEFECT CONTROL UNDER 6H- AND 4H-SiC BOULES SUBLIMATION GROWTH

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Silicon carbide is gaining more and more importance as a material for severe environments (high temperature, high radiation, chemical hazards etc.) electronics. Improvement of structural properties of SiC wafers is the key area of the SiC-based devices development. The main problem which prevents breakthrough in the SiC based devices mass production is growth of large high quality silicon carbide boules for manufacturing of 2" and 3" substrates. At present commercially available substrates are produced by sublimation growth method. First results on the silicon carbide sublimation growth using Modified-Lely method elaborated at the St.Petersburg Electrotechnical University were reported by Yu.M.Tairov and V.F.Tsvetkov in 1976 [1]. But till now the problem of defects formation control is not solved. Micropipe defects in silicon carbide single crystals are performance limiting defects for devices on their base and micropipe defects in substrates serve as the sources for the formation of defects in epitaxial layers grown on them. At present micropipes are referred as the main obstacle. The next issues are dislocations, misoriented areas and strain. The above mentioned defects are interdependent. For instance one of the types of micropipes is formed by the accumulation of vacancies by the core of super screw dislocation. Deviation from the stoichiometry causes vacancies, misfit, strain, stacking faults. Strain relaxation causes dislocations formation. All these problems must be taken into account to develop missing models and to make growth, doping, annealing of SiC a completely controllable process.

The aim of the present work is to discuss our results of growth of large up to 40 mm in diameter 6H- and 4H-SiC crystals for further substrates manufacturing. Some our recent results on the simulation of heat- and mass-transfer, temperature and strain distribution in the crystals are also considered with respect to the experimental results. Problems connected with the enlargement of SiC crystals up to 40 mm in diameter as well as growth of large boules without enlargement are discussed. Polytype stability and transformations, formation of defects, nonuniformity of doping are considered.

The sublimation growth was carried out by the Physical Vapour Transport (Modified-Lely method) [2, 3]. The growth temperatures were in the range 1800-2500°C. The crystals were grown in vacuum or argon atmosphere. The crystal growth was carried out either with or without enlargement. The influence of the growth temperature, vapour phase composition, dopants, substrate preparation on the formation and behaviour of different types of defects in crystals grown on a different SiC faces was considered. Polytype control was carried out using the crystallization kinetics or by introduction of

certain dopants. Al, Sn, Pb, Sc and some other rare-earth metals promote the 4H-SiC formation. Further growth of certain polytype depends also on kinetics of further growth and polytype transformation can be caused be inatability of growth parameters and doping.

Optical microscopy, scanning electron microscopy, selective etching, X-ray topography, selective etching in molten KOH, and photoluminescence mapping were employed for investigations of samples obtained.

Micropipes formation in SiC bulk crystals can be caused by the defects of graphite substrate holder and inhomogeniety of substrate attachment to the holder, micropipe reproduction from the substrate, contamination of the growth surface, unoptimized mechanism of epitaxy at the initial stages of growth, substrate's surface processing (before growth and "in situ"), instabilities of the growth process parameters. Initial stages of growth at the growth temperature as well as nucleation of initial layers under the lower temperatures during temperature increase up to the growth one have been investigated. The nucleation of the initial layers before the required growth temperature is reached was observed even at high Ar pressures up to 200 mbar if positive temperature gradient is applied. Samples were investigated by optical microscopy, scanning electron microscopy , x-ray topography, selective etching. Special method of substrate processing and further growth at the initial stage have been developed [4, 5]. The results obtained make also possible to reduce replication of micropipe defects from the substrate to the growing crystal. Using approach elaborated in [4, 5] we reduced micropipes reproduction from the substrate and low micropipe density material (under 80 cm^{-2}) on substrate with micropipe density as high as 300-600 cm^{-2} have been grown (such low micropipe density was revealed already in the wafer sliced from the boule just after the substrate). Scanning electron microscopy was employed for undestructive observations of micropipes on both SiC (0001) sides. Results of micropipe observation by both methods were compared to justify correctness of the KOH etching conditions micropipe density definition by the KOH etching. X-ray diffractometry investigations were also employed for structural quality characterization of the crystals grown. Crystals with the values of N_d-N_a in the range 5 10^{15} cm^{-3} - 10^{19} cm^{-3} have been obtained.

Mapping of the samples was performed using cathodoluminescence, photoluminescence, and x-ray topography. Formation of misoriented areas for crystals with diameters up to 26 mm was prevented. It is still not obvious that such slightly misoriented marginal areas in the substrates influence operation of devices formed in the epitaxial layers grown on such substrates.

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MODELLING OF SIC SUBLIMATION GROWTH PROCESS: POWDER GRAPHIZATION AND SUBLIMATION

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The modified Lely method is based on mass transport using thermal sublimation from a solid source and crystallisation on a suitable seed crystal. The growth takes place at temperatures above 2500 K in a crucible which is usually made of graphite. An accurate modelling and simulation of the sublimation growth process needs a software taking into account highly coupled phenomena, fluid mechanics with Stefan flow, convective, conductive and radiative heat transfer, electromagnetic, multicomponent species transport, homogeneous and heterogeneous thermochemical equilibrium and finally accurate thermal and transport databases [1-8].

In this paper we demonstrate that the features of powder consumption and graphitization are directly linked to the global heat transfer and that the heats of sublimation and condensation are of minor importance in our apparatus.

Sublimation of the SiC powder is not congruent. Its graphitization is then expected. Thermodynamic modelling showed that, when the temperature increases the Si/C ratio decreases (figure 1). Experimentally, during the growth of SiC ingots, the source material, i.e., the powder, partially carbonizes and recrystallizes (figure 2a). Some experiments leading to higher temperature in the powder have shown that, in accordance to thermodynamics, the graphitization is replaced by local congruent sublimation of the powder as the Si/C ratio is close to one (figure 2b). We have focused our attention on the relationship between the thermal field obtained in the first step of the growth process and the features of the powder after a five hours processing. It clearly appears that, in case (a), periphery of the powder is carbonized. In case (b), empty cavities are formed in the powder. The associated thermal fields show that, when increasing temperature, the Si/C ratio decreases leading to the occurrence of sublimation of the powder. These results allow us to predict the main feature of the powder and to validate some aspects of our software and thermal database.

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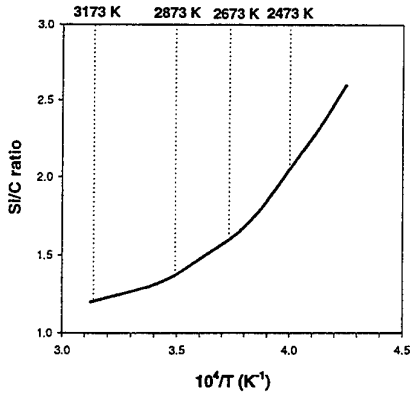

Figure 1 : Theoretical Si/C ratio as a function of 1/T

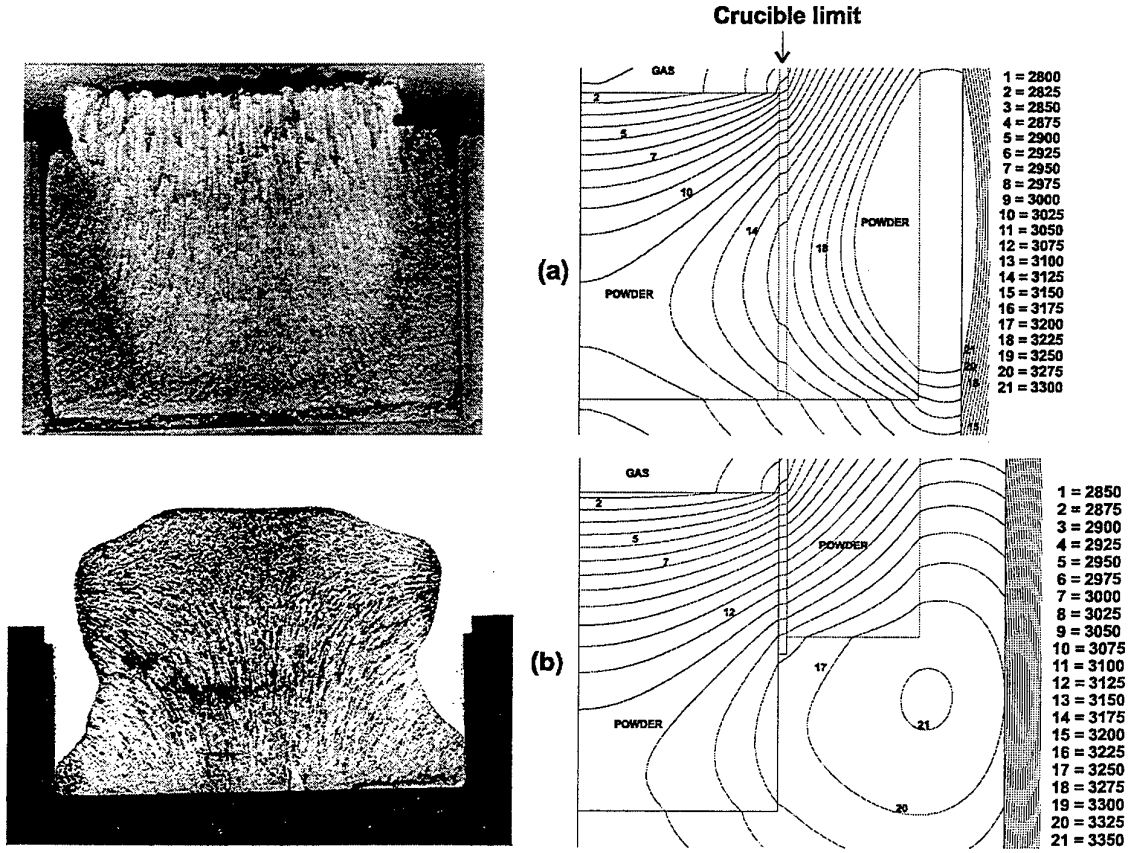

Figure 2 : Cross-sections of the powder with associated thermal field (a) lower temperature than (b).

MODELLING OF SIC SUBLIMATION GROWTH PROCESS: TRENDS IN MACRODEFECTS APPEARENCE

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Heat transfer is the most studied modelling route for the SiC sublimation process [1-10]. The aim was to better understand the different phenomena involved during the growth process and to pave the routes of its computer design. The need for such a research effort was motivated by the fact that the primary obstacle to the production of large-area SiC-based devices is the presence of hollow defects which, till now, have occurred in virtually all seeded sublimation-grown boules. It was found that local temperature fluctuations over the seed can be one of the causes of hollow defects formation [10-11]. We only study in this paper the so-called macrodefects which are large vertical holes with horizontal enlargement at the end. They start at the holder-seed interface and may penetrate deep into the growing crystal. The formation of these defects have been explained by backside local sublimation of the growing ingot seed due to the attachment technique [11-12] and not as the result of instabilities at the growth interface.

As the macrodefects formation involves backside sublimation from the seed, both temperature and its gradient are important keys to control the occurrence of the macrodefects in SiC boules. We have studied various crucible designs, growth chamber geometries and seed attachment techniques in relation with macrodefects profile. Figure 1 shows the temperature gradient profile and the corresponding SiC ingots for two different configurations. There is a strong correlation between the temperature gradient at the back of the seed and the macrodefects distribution. In the case (a), the maximum concentration of macrodefects is reached where the temperature gradient is maximum. In the case (b), the homogeneity of the temperature gradient at the graphite-seed interface leads to an uniform macrodefect profile. We will thus discuss the influence of the temperature gradient at the backside of the seed, and the different ways to suppress this kind of defects.

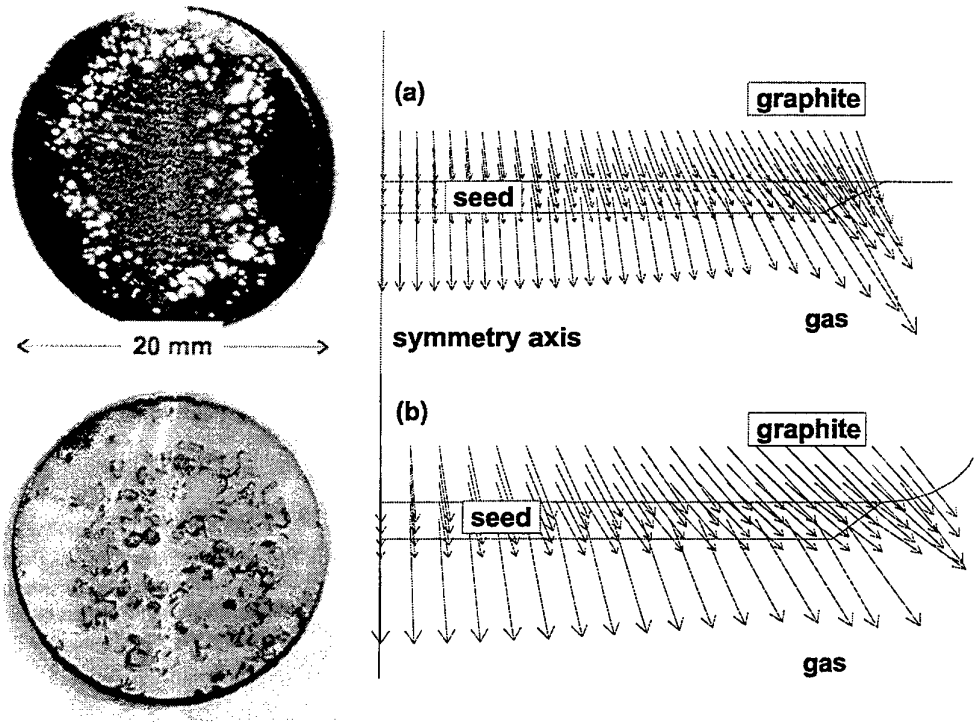

Figure 1: Temperature gradient profile and corresponding SiC wafers for two different configurations.

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THE INFLUENCE OF EXCESS SILICON ON SURFACE MORPHOLOGY AND DEFECT STRUCTURE DURING THE INITIAL STAGES OF SiC SUBLIMATION GROWTH

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Defect density, surface quality and polytype of the seed as well as the vapour phase stoichiometry are important parameters in order to control the crystalline perfection of sublimation grown SiC. Therefore by varying the excess silicon content in the SiC source growth experiments have been carried out to investigate the initial stage of crystal growth.
1"-6H-SiC wafers polished on both sides have been used as seeds, which were not intentionally doped. The orientation of the seed was on-axis <0001> on the Si-terminated face.
The surface morphology of the grown SiC crystals in the initial stage was compared in relation to the relative silicon content of the SiC source. By means of optical and atomic force microscopy it is shown that there exist a distinct difference in some features of surface morphology. These differences are correlated to the stoichiometry of the SiC source. With increasing excess of Si in the SiC source the morphology of the grown SiC crystals tends to a pronounced stepped morphology characterized by flat treads and steep riser (step flow growth mode). In contrast a depletion of Si in the SiC source is responsible for uncontrolled growth of three dimensional SiC islands. Investigations by cathodoluminescence on cleaved surfaces of SiC samples show that there exists a correlation between the defect structure at the interface between seed and grown crystal and the content of Si. This defect structure can be a source of defects (micropipes) in the growing crystal. This confirms the significant role of the stoichiometry not only for the first layer to grow but on the whole crystal growth process.

A PRACTICAL MODEL FOR ESTIMATING THE GROWTH RATE IN SUBLIMATION GROWTH OF SiC

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One of the most important parameters in a crystal growth process is the growth rate since it is closely related to the material quality and process yield. In sublimation growth of SiC the growth rate is very difficult to keep in strict control. It can not be measured during the process, but must be determined afterwards. In order to achieve reproducible growth results, a mathematical model that estimates the growth rate is of great practical use. A model also clarifies the growth rate dependence on specific parameters with a faster feedback than obtained by experimental means.

In the paper we present a model for the growth rate of SiC sublimation growth process in an idealized one-dimensional case. The model is therefore best applicable to sublimation epitaxy where the geometry is quite close to the ideal case and mass transfer from the source to the seed can be quite accurately evaluated. This is a consequence of the small source-to-seed distance compared to the system diameter. A one-dimensional case enables analytical formulas for the growth rate and parametric dependencies become more obvious.

Models for one-dimensional sublimation process have been presented also before, *e.g.* [1,2]. Most of them consider obvious parameters such as temperature, temperature gradient, vapor pressure of the different Si and C containing species, etc. In this paper we pay attention to some additional details. The growth rate is usually assumed to be created by a fixed temperature gradient. However, the heat of crystallization decreases the temperature gradient. In the presented model the heat of crystallization is taken into account. It is shown that with a constant heat flux there is a maximum growth rate that can not be exceeded by decreasing the source-to-seed distance. This phenomena is demonstrated in the sublimation epitaxy. At larger distances the growth rate is inversely proportional to the source-to-seed distance.

Often the growth rate is known as a function of the temperatures measured by the pyrometers. These temperatures are unfortunately not the true temperatures determining the driving force in the crystal growth process. In the paper we try to analyze how the real temperatures inside the crucible are related to the measured ones. With the help of simulations the true axisymmetric geometries are characterized using the parameters of the idealized one-dimensional geometry. The model is applied to several different cases. The results are compared to experiments and also some predictions are made.

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MISORIENTED AREAS FORMATION UNDER LARGE SILICON CARBIDE BOULES GROWTH

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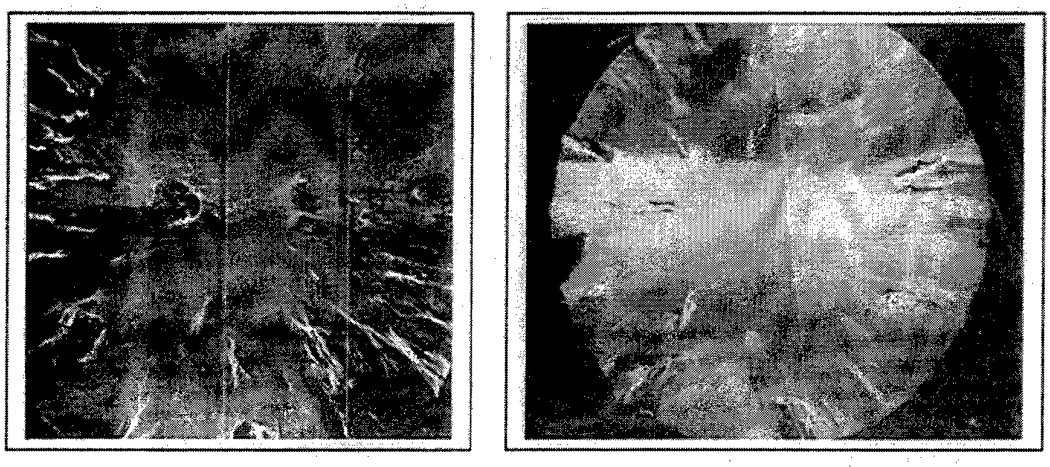
Silicon carbide is gaining more and more importance as a material for severe environments (high temperature, high radiation, chemical hazards etc.) electronics. Commercial use of SiC for device applications especially for high power devices is still seriously limited by the not high enough quality of substrate material. Improvement of structural properties of SiC wafers is the key area of the SiC-based devices development. Formation of small misoriented areas (mosaicity) in SiC crystals grown by sublimation method was reported in [1]. One of the problems which was noted at our lab as well as at other labs (for instance at Nippon Steel [2]), is the presence of slightly misoriented (less than 1 degree) comparatively large areas in the silicon carbide boules. Presence of slightly misoriented (less than 1 degree) comparatively large areas in the silicon carbide boules grown by sublimation method is one of the types of defects which can limit operation of the devices based upon such material. The aim of the present work is to investigate formation of strain and misoriented areas in SiC crystals and development of the nondestructive techniques of such materials characterization.

The 6H- and 4H- SiC crystals 20-50 mm in diameter were grown by sublimation method [3, 4, 5] elaborated at the St.-Petersburg Electrotechnical University. Samples have been investigated using X-ray diffractometry and X-ray topography (Berg-Barrett and Lang methods). Selective etching in molten KOH and photoluminescence mapping using UV irradiation at room and liquid nitrogen temperatures have been also employed for express observation of misoriented areas in the wafers.

Some of the results of the x-ray topography study of 1 inch 6H-SiC substrates cutted along (0001) plane are shown in Fig. 1a. Presence of slightly misoriented strained peripheral areas was typical for initial 6H- and 4H-crystals . SEM studies, optical investigations of KOH etched surfaces revealed comparatively low density of micropipes and dislocations - about 80 cm^{-2} and 10^4-10^5 cm^{-2} correspondingly.

The influence of the growth conditions, crystal enlargement, pregrowth treatment, dopants on the formation of misoriented areas and dislocations have been investigated. Results obtained gave possibility to diminish formation of misoriented areas in SiC crystals. X-ray topography image of 30 mm in diameter 6H-SiC substrates cutted along (0001) plane from the boule grown on the substrate shown in Fig. 1a is shown in Fig. 1b. As it is clearly seen from the Fig.1a, b the presence of misoriented areas was significantly reduced under one growth process using specially elaborated

methodology of growth. Formation of misoriented areas for crystals with diameters up to 26 mm was prevented. For crystals 28-40 mm in diameter misoriented areas in the peripheral parts of the boule were observed. For most cases misorientation did not exceed 1′ and several angle minutes for crystals 28-32 mm and 32-40 mm in diameter correspondingly.



a b

Fig. 1. X-ray topography images of the 6H-SiC substrates cutted along (0001) plane:
a-initial substrate 26 mm in diameter
b-substrate 30 mm in diameter cutted from the boule grown on the substrate shown in Fig. 1a.

Dislocations and pinholes can be caused by the defects of graphite substrate holder and inhomogeniety of substrate attachment to the holder; micropipe reproduction from the substrate; contamination of the growth surface; unoptimized mechanism of epitaxy at the initial stages of growth; substrate's surface processing; instabilities of the growth parameters [6, 7]. Etching in molten KOH was employed for revealing of micropipes and dislocations including the dislocations forming low angle boundaries of the misoriented areas. Some of our recent results of x-ray topography and selective etching investigations of the influence of growth parameters on the dislocation and pinhole structure will be considered and discussed.

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NUMERICAL SIMULATION OF GLOBAL HEAT TRANSFER IN REACTORS FOR SIC BULK CRYSTAL GROWTH BY PHYSICAL VAPOR TRANSPORT

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Bulk growth of SiC crystals by the physical vapor transport technique (PVT) is a complex process. The growth reactor is heated by induction at low frequencies (≈10 kHz). Temperatures between 2100 °C and 2400 °C have to be established in the growth chamber driving the sublimation of SiC powder, mass transport and crystallization at a SiC seed. The absolute temperature and its axial and lateral distribution are of key importance for the magnitude of growth rate and especially the defect generation in the growing crystal. As the detection of temperatures during a growth run is rather limited the development of tools for the simulation of heat transfer inside the SiC growth arrangement is very important for the optimization of the SiC bulk growth process.

In this paper the recently developed code for the simulation of heat transfer in inductively heated reactors is introduced. The calculations are performed in two separate steps. First the induced heat sources are computed by solving the Maxwell-equations describing the periodic electromagnetic field. In the second step transport equations are solved resulting in the temperature distribution.
The solution of the Maxwell equations is conducted with a finite element solution procedure. An unstructured grid approach is used. The distribution of the Joule heat sources produced by the field are computed taking into account the material properties in the different parts of the reactor. For the simulation of the heat transport a finite volume algorithm is applied. The governing equations are discretized on a block-structured grid which allows to treat different parts of the reactor like solid/gas or solid/solid regions with different temperature-dependent material properties. The solution procedure is based on a multigrid solver.
First a comparative study of numerical and experimental results for the experimental verification of the code is presented. Analysis on the influence of control parameters, e.g. power, position of induction coil, and geometry of the crucible on the thermal process conditions are conducted and its impact on the process conditions is demonstrated. It is shown that axial and radial temperature profiles are highly sensitive to the applied power and location of the inductor. Under non-optimized conditions radial temperature gradients of up to 10-15 K/cm and large temperature differences are found in the seed area and in the SiC powder, respectively which can be considered as too high for low defect SiC growth. The limits of temperature control due to power and coil location variations are investigated. Further optimization of thermal growth conditions is evaluated to be correlated with improvements of crucible design.

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HIGH RESISTIVITY SIC CRYSTALS DOPED WITH MOLYBDENUM AND VANADIUM

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New data on highly resistive 6H- and 4H-SiC crystals grown by sublimation sandwich technique and doped by molybdenum and vanadium are presented. The peculiarities of doping by these elements and some crystalline properties are described. P- and n-type conductivity is obtained in these crystals. It is shown that both molybdenum and vanadium favor formation of the compensated material. This is related to the fact that these dopants create deep levels located in the middle of the forbidden gap of SiC.

Comprehensive study of 6H-SiC doped by molybdenum is carried out using different characterization techniques – Electron Paramagnetic Resonance and Optically Detected Electron Paramagnetic Resonance. Two charged state of dopant are identified: Mo^{4+} and $Mo^{3+}(4d^3)$. It is shown that molybdenum is multi-charge dopant and can form both acceptor and donor levels in the upper part of the forbidden gap. That is why this element is suitable for growth of semi-insulating SiC. On the other hand this element is responsible for degradation of semiconductor devices having molybdenum contacts.

THERMODYNAMICAL CALCULATIONS ON THE CHEMICAL VAPOUR TRANSPORT OF SILICON CARBIDE IN A CLOSED TUBE

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Silicon carbide is a wide gap semiconductor which exhibits outstanding electronic properties associated with chemical and thermal stability. The obtention of a good quality SiC is of great interest and many laboratories are studying the SiC growth by differents means. Chemical Vapour Deposition, Molecular Beam Epitaxy and sublimation process have been reported for epitaxial growth of thin films and bulk SiC respectively. However, to our knowledge, Chemical Vapour Transport process in a closed tube has never be performed for the growth of SiC. Thermodynamic calculations have been carried out for different chemical systems in order to select the best transporting agent for silicon carbide and to foresee the nature of the deposits with varying parameters.

The thermodynamic calculations based on the total Gibbs free energy minimization were obtained from the GEMINI1 computer program from scientific group Thermodata (S.G.T.E. Saint-Martin d'Heres, FRANCE) and a coherent set of thermodynamical data from JANAF. All these calculations were accomplished in isochore conditions. The parameters involved in this process are temperatures of the source and the substrate and initial amount of the transporting agent.

First, we have investigated the SiC etching at one end of the tube called the source zone by calculating the equilibrium partial pressures of gases so as to show silicon and carbon behaviour with the transporting agent. Second, with the assumption that the diffusion rate of each gases species is the same in a temperature gradient, we have examined the solid phases deposited at the other end of the tube, called substrate zone.

For this two types of simulations, we have studied the Si-C-X systems where X is an halogen (F, Cl, Br, I). As results, we have shown that the classical halide process is not usable for the SiC transport. Indeed, silicon can easily be transformed in silicon halides, but carbon can give halides only if Si is entirely consumed, i.e if halogen is in excess. This is not possible for a CVT process because an excess of halogen involves too high total pressure. Then, we have studied the Si-C-H-X systems in order to investigate the hydrogen influence in the CVT process. As silicon forms halides, carbon gives hydrocarbons which are able to transport the carbon from the source zone to the

substrate zone. The gas phases obtained are more complex but show very interesting results. SiC alone can be deposited through a large range of temperature gradients with HCl (figure1) and HBr transporting agents.

It is important to note that the transport is performed from the low temperature zone to the hot zone of the tube with the hydrogen halides, excepted for HF which has a marginal behaviour compared to the hydrogen halides serie. This point is very interesting in so far as high temperatures are needed to obtain a good quality of SiC.

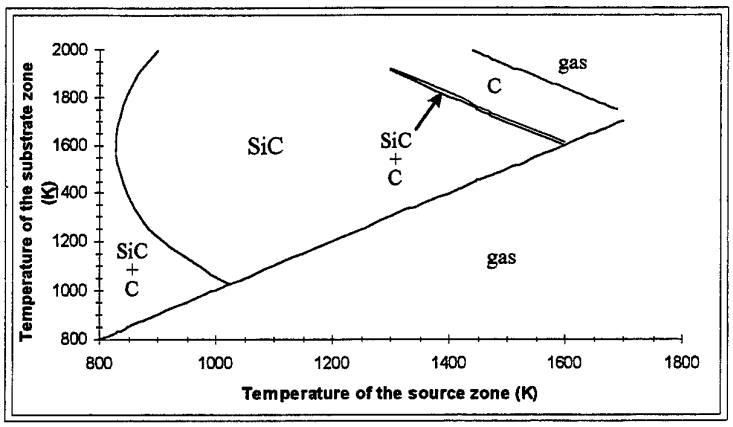

figure 1 : nature of the deposits in a Si-C-H-Cl system for a CVT process in a closed tube.

ANALYSIS OF ELECTRONIC LEVELS IN SIC:V POWDERS USING THERMALLY STIMULATED LUMINESCENCE

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Semi-insulating silicon carbide is an attractive substrate material for high power microwave applications due to its combination of high thermal conductivity with low dielectric loss. Its availability is of key importance to the development of SiC-based lateral devices like metal-insulator field effect transitors (MESFET). Substrates with high electrical resistivity can be achieved by compensation of residual impurities like nitrogen, aluminium and boron with deep levels introduced via intentional doping with vanadium. An analysis of impurities producing electronic levels in SiC is hence necessary for powders used as source material for the physical vapour transport (PVT) crystal growth process.

Vanadium in silicon carbide provides two near midgap states: The deep donor $V_{Si}^{5+/4+}$ is able to compensate acceptors like boron and aluminium whereas the acceptor $V_{Si}^{4+/3+}$ compensates residual donors, e.g. nitrogen. Due to the limited solubility of vanadium in silicon carbide, the control of compensation of shallow donors and acceptors is the main challenge to achieve semi-insulating properties. Common methods to perform analysis of compensation like C(U) or DLTS afford preparation of electrical contacts on bulk material. Hence, there is a lack of determination methods for powders.

In the present work, thermally stimulated luminescence (TSL) is introduced as a qualitative method to distinguish powder samples of different compensation as has been performed before on single crystals by *Stiasny et al.* [1],[2]. TSL glow curves are taken from electrically precharacterized nitrogen, boron and aluminium doped SiC samples of different compensation and of SiC:V-powders of unknown compensation. Shallow donators and acceptors are revealed to act as electron/hole traps charged after illumination with X-rays. In the glow curve recorded during the heating progress with linear heating rate β several peaks are observed. The peak temperature is correlated with trap energy E_T, frequency factor s and heating rate β.

INVESTIGATION STRUCTURAL PERFECTION OF SiC BOULES GROWN BY SUBLIMATION METHOD

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Results of SiC boule initial stage growth are presented. Crystal was grown by modified Lely method using 6H-SiC seed crystals with (0001) base plane. The size of a seed was about 8*8 mm^2. The seeds were etched in the KOH melt (T=600 C, t=3-5 min). The orientation of (0001)Si and (0001)C type plane was determied by this process. As a source meterial we used polycrystalline SiC powder of p- or n-type conductivity, which was obtained by Achesson's method. The crystal growth was carried out in the temperature range 2200÷2500°C and at the pressure of Ar in the range 2÷40 bar. The rate of growth varied from 0,3 to 1,5 mm/hour in the direction of the **C** axis. Time of the growth process itself was usually 5-6 hours. At the time of growth about 10 hours we obtained the boules with 25 mm useful diameter.

To determine SiC boules polytypic composition we used the Raman scattering technique. The structural defects were investigated by means of X-ray topography Leng's method and also by means of light microscope on reflection and transition. We used $MoK_{\alpha 1}$ radiation and reflexes of {1120}, {1100} and {1011} type, wich have the highest reflexive abilities. With the purpose of studing of boule parameters they were cut into plates in two different crystalographical directions: parallel and perpendicular to the **C** axis. The thickness of the plates varied from 0,5 to 1,0 mm. Crystalographical planes {0001},{1120}, {1100} type were the facets of those plates.

The dislocations, dislocation loops blocks and micropipes were found to be the main defects of on structure of boules. The concentration of these defects depends mainly on the structural quality of seed, its preparation and initial growing conditios. The shape of the boules is conditioned by the configuration of thermal field around the seed. Main structural defects (as micropipes, dislocationc) emerge on the surface of a seed, spread in the direction which coincide with the vector gradT and are perpendicular to the surface of the boule. In the best boules the concentration of dislocations did not exceed 10^2 cm^{-2}, micropipes – 10-20 cm^{-2} and blocks were completely absent.

The polarity of SiC influences the polytype structure of growing crystals. This property of SiC permits to control the polytypic composition of boules. Using the charge doped by boron on the surface of seed (0001)C we obtained the 4H-SiC boules, while on the (0001)Si surface we always got the 6H polytype. This took place at several dozents experiments at the temperature of growth T≤ 2400 C. However, increasing the temperature to 2500 C on the (0001)C we obtained 6H-SiC polytype boules.

OPTIMIZATION OF SUBLIMATION GROWTH OF SiC BULK CRYSTALS USING MODELING

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Sublimation growth of bulk SiC crystals is used in industry for manufacturing of SiC wafers. Optimization of the growth process is performed usually by trial and error. Modeling is a promising tool to study global heat transfer and mass transport during the sublimation growth and to optimize the process [1]. In the present paper new results of modeling analysis of the sublimation growth in Ta container are presented.

Global heat transfer in the growth system heated by inductive coil is modeled by taking into account the Joule heat sources, heat conduction and radiative transport. Knowledge on heat conductivities of different materials used in the growth system is important for accurate prediction of the temperature distribution. Heat conductivity of SiC powder is calculated using the model proposed in [2]. An approach similar to that used in [2] is adjusted for analysis of heat conductivity of the graphite insulation.

Using the modeling of global heat transfer, possibilities to optimize the temperature distribution inside the crucible are studied. In particular, it is found that geometry of some parts of the crucible influence significantly the temperature distribution and optimization of design of these elements can be used for control of the temperature distribution inside the crucible.

Evolution of the temperature profiles inside the crucible during the growth is studied with the goal to keep the surface temperatures of the seed and source constant. In Fig. 1 the computed temperature distributions in the beginning and end of the growth process are shown.

The computed temperature distributions inside the crucible are used to predict the SiC growth rate. For this an advanced model proposed in [1] is used. The model predicts reasonably the growth rates of SiC crystals in Ta system (see Table 1). In the present paper analysis of species transport in Ta container during the sublimation growth under low external pressure of inert gas is performed. It is shown that extremely high velocity up to 50 m/s of macroscopic flow of Si-C species from the source to the seed occurs which can transport particles in direction opposite to the gravitation. Analysis of mass exchange between the crucible and the external atmosphere is studied. The coupled software tool for modeling of global heat transfer and species transport allows optimizing the sublimation growth process.

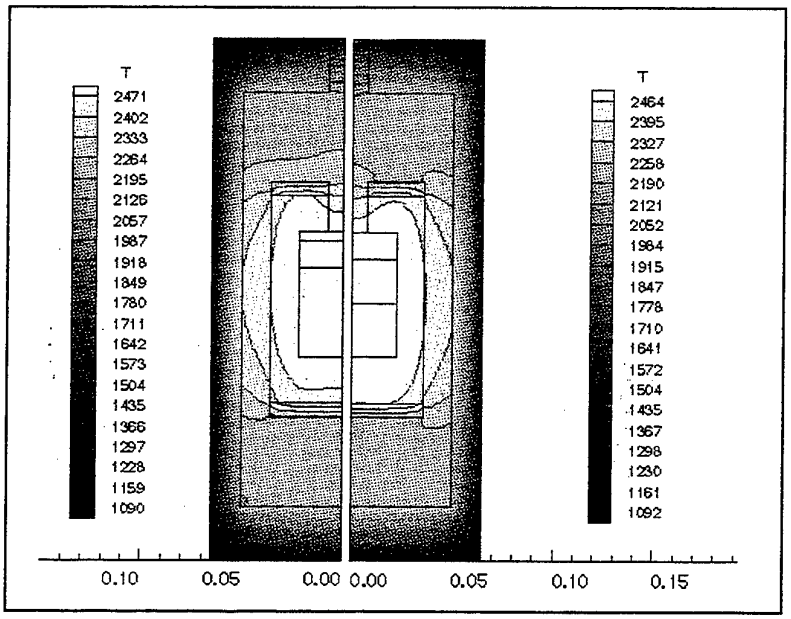

Fig. 1. Temperature distribution in growth system at the beginning (left) and at the end (right) of the bulk crystal growth process.

Clearance, Mm	Mass losses, percents	Crystal diam., mm	Temperat. range, ^{0}C	Calculated growth rate, mm/h	Experiment. growth rate, mm/h
6	8.2	43	2005-1975	0.825	0.86
8	12.0	43	2010	0.870	0.5
8	9.1	43	2010-2005	0.852	0.6
7	11.6	43	2010-2005	0.838	0.5
4	6.4	43	2010-2000	0.778	0.64
7	6.2	35	2005	0.842	0.77
7	7.0	35	2000-1995	0.758	0.62

Table 1. Comparison of the experimental data and theoretical prediction of the growth rate

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HIGH-TEMPERATURE SURFACE STRUCTURE TRANSITIONS AND GROWTH OF α-SiC (0001) IN ULTRAHIGH VACUUM

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Growth mechanisms of α-SiC (4H- and 6H-SiC) homoepitaxy have been revealed for chemical vapor deposition (CVD) [1]. Though growth on an α-SiC substrate by molecular beam epitaxy (MBE) has been tried [2,3], few reports are available on surface structures during the growth. In this paper, surface structure transitions on α-SiC (0001) in a high vacumm at high temperatures above 1150°C are presented based on an *in-situ* reflection high-energy electron diffraction (RHEED) observation : a change of surface structure from (3×3) to (1×1) is newly observed. Crystallographic characteristics of SiC epilayers formed by gas source MBE are studied.

CVD grown α-SiC (0001) Si-faces with 3.5~8° off-orientation toward the [11$\bar{2}$0] direction were used as substrates. After a substrate was loaded in a gas source MBE system, a clean surface showing a (3×3) structure was obtained at 1000°C in a low flux of disilane (Si_2H_6) through the surface structure change of (1×1) → ($\sqrt{3}\times\sqrt{3}$). Subsequently after, the substrate temperature was settled at a given value to grow a SiC layer. Pure Si_2H_6 and acetylene (C_2H_2) were used as source gases. Typical flow rates of Si_2H_6 and C_2H_2 were 0.6 sccm and 0.004 sccm (C/Si=0.0067), respectively. Growth of SiC was carried out for 60 min. Crystallographic features of growing surfaces were analyzed using an *in-situ* RHEED system. Surface morphology was observed by a Nomarski microscope.

Figure 1 (a) shows an *in-situ* RHEED pattern of an α-SiC (3×3) structure, which is very stable below 1100°C in an ultrahigh vacuum ($\sim 1\times10^{-9}$ Torr). The observation of α-SiC (3×3) structures has been reported by an annealing experiment under a Si flux in the range of 850 ~ 1150°C [4] and by 6H-SiC homoepitaxy using gas source MBE at 1050°C [3]. Among many models for the α-SiC (3×3) structure, an adsorbed Si layer model was proposed based on scanning tunneling microscope images [5].

With the increase of substrate temperature above 1150°C in a high vacuum ($<10^{-8}$ Torr) without Si_2H_6 supply, the α-SiC (3×3) structure changed to a (1×1) structure (Fig. 1 (b)). A graphite-related structure due to the desorption of Si atoms from the surface did not appear in the (1×1) structure, when the substrate was kept at 1200°C in a high vacuum even without Si_2H_6 supply. With the decrease of substrate temperature below 1150°C in a high vacuum, the (1×1) structure returns to the (3×3) structure, indicating Si atoms exist on the surface at 1200°C. The surface structure transition between (3×3) $\rightleftharpoons$ (1×1) occurs on α-SiC (0001) at around 1150°C, and it

is reversible. It can be considered that migration of Si atoms on the surface is enhanced above 1150°C, and Si atoms forming the (3×3) structure may migrate to form the (1×1) structure.

Gas source MBE growth of α-SiC was investigated at different growth temperatures. In the case of growth above 1150°C, the (1×1) structure was kept during the growth. After the growth, the surface structure transition from (1×1) to (3×3) was observed at 1150°C during temperature decrease. Figure 2 (a) shows surface morphology of the SiC layer grown at 1200°C. A featureless surface was obtained, indicating homoepitaxy of α-SiC.

On the other hand, in the case of growth below 1000°C, many islands were observed on the surface (Fig. 2(b)). During the growth of SiC, the starting (3×3) structure changes to a spotty RHEED pattern (Fig. 3), showing a three-dimensional growth mode. The spotty RHEED pattern of Fig. 3 corresponds to a β-SiC (3C-SiC) (111) double-domain twin structure [2] : islands on the surface consist of β-SiC. Since the migration of Si atoms on the growing surface are insufficient at 1000°C, three-dimensional growth occurs and low-temperature stable β-SiC islands are formed.

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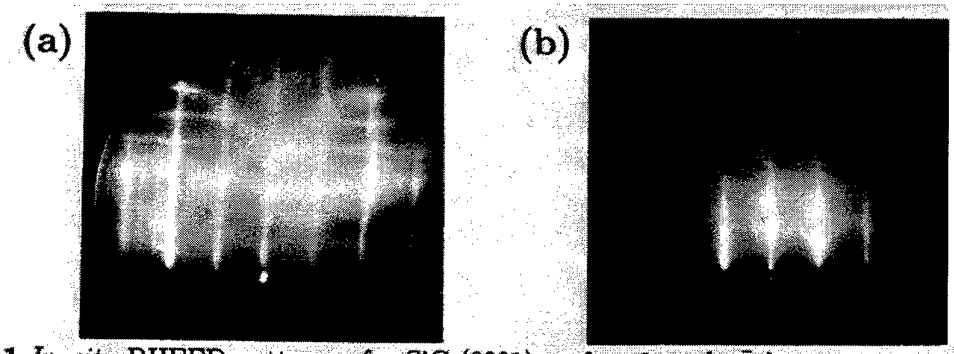

Fig. 1 *In-situ* RHEED patterns of α-SiC (0001) surface from [11$\bar{2}$0] azimuths. (a) (3×3) and (b) (1×1) structures.

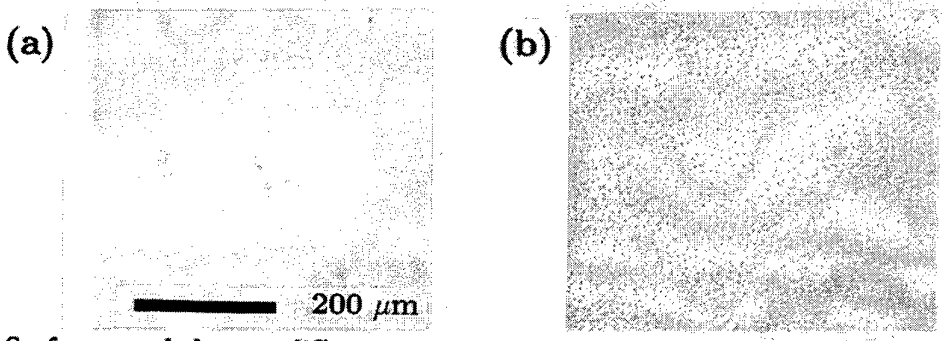

Fig. 2 Surface morphology at different growth temperatures of (a) 1200°C and (b) 1000°C.

Fig. 3 RHEED pattern of a layer grown on α-SiC (0001) substrate at 1000°C.

EPITAXIAL GROWTH OF SIC IN A NEW MULTI-WAFER VPE REACTOR

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The interest in Silicon Carbide as a material for production of semiconductor devices is increasing. The epitaxial growth of SiC is an important technology to form device layers with controlled thickness and doping levels. So far, with a few exceptions, growth of SiC has been done on a research level using single wafer reactors. Now when the properties of the epitaxial layers are approaching industrial needs it is time to take the next step. However going from research into production will be impossible unless SiC VPE reactors for production featuring high throughput of high quality material with tight specifications of doping and thickness uniformity, and background doping are realized. Until now only results from one multi-wafer reactor has been reported [1].

We have grown SiC using a commercial multi-wafer reactor from Emcore inc. The design is based on their MOCVD reactors for growth of III/V materials but modified for high temperature capability. The reactor is vertical with a wafer carrier that can be rotated up to 1000 rpm supporting up to six 50 mm wafers. It is capable of growing SiC at temperatures between 1480°C and 1650°C and at pressures between 200 and 350 mbar. A similar design for single wafer growth has been successfully developed and reported on before [2].

The SiC layers we have grown show mirror like surfaces with excellent morphology as seen with optical microscope and Atomic force microscope (AFM). Defects other than substrate related ones are almost non-existent. The material has been grown with growth rates of 3-5μm/h. The unintentional background doping is p-type in the mid-10^{15} range at C/Si=1 in the gas phase, appears to be due to Al originating from the susceptor and is currently under investigation. The concentrations were measured using Secondary ion mass spectrometry (SIMS) and CV. Results from the two measurement techniques were consistent also when measuring on intentionally doped n (N) and p-type (Al) layers indicating full dopant activation. SIMS was also used to investigate uniformities. 35 mm wafers with thickness uniformities well within 5% has been grown. Finally both n and p type dopant uniformity within a wafer will be presented.

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PURITY AND SURFACE STRUCTURE OF THICK (>100 μm) 6H AND 4H-SiC LAYERS GROWN BY SUBLIMATION EPITAXY

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Epitaxial layers of Silicon Carbide (SiC) have an excellent potential in high-power, high-temperature, and high-frequency applications. Chemical vapor deposition (CVD), is the only established method for epitaxial growth of device quality SiC. For applications like very high-voltage power devices, substantial layer thicknesses are required and the CVD method is then inconviniently slow due to the low growth rate (2-6 μm/hour). As a complementary technique, sublimation epitaxy is suitable for growth of high-quality thick layers with a high growth rate. For subsequent device processing after epitaxy, it is important that the surfaces are smooth and the layers are pure. In this study, the as-grown surfaces and purity of thick (>100 μm) 6H and 4H-SiC layers grown by sublimation epitaxy have been investigated.

The layers were grown on the Si and C-face of 6H and 4H-SiC substrates by sublimation epitaxy with an average growth rate of 120 μm/hour. The substrates were off-oriented 3.5° or 8° from the basal plane in the $< 11\bar{2}0 >$ direction for 6H and 4H-SiC substrates, respectively. The growth method has been described elsewhere [1]. The as-grown surfaces were studied by using optical microscopy with Nomarski interference contrast and atomic force microscopy (AFM). The epitaxial layers were also investigated with capacitance-voltage (C-V) and low-temperature photoluminescence (PL) measurements.

C-V and low-temperature PL measurements

From C-V measurements, epitaxial layers grown on the Si-face of 6H-SiC at 1700°C were found to be n-type with a net donor carrier concentration of 3×10^{15} cm^{-3}. The low value of the measured carrier concentration is partly due to unintentional compensation since free excition related luminescence is very weak in low-temperature PL measurements (Fig. 1) and peaks related to the Al acceptor bound exciton recombination are resolved in the near band gap region (Fig. 1). No donor-acceptor pair luminescence is observed. The no-phonon lines of the nitrogen bound exciton recombination (P_0, R_0, S_0 in Fig. 1) are very narrow which indicates high crystalline quality. The temperature dependence, effect of substrate polarity and how the growth environment affects the doping are reported. The results are compared with impurity concentrations as measured by SIMS.

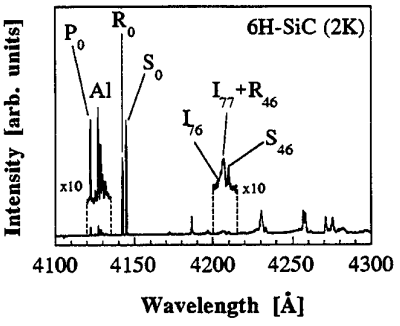


Fig. 1. Near band gap region of low-temperature photoluminescence of a thick 6H-SiC epitaxial layer grown by sublimation epitaxy.

Optical microscopy

In optical microscopy, the morphology of the specular surfaces was smooth and it was difficult to observe growth steps (Fig. 2). It is reasonable to expect the appearance of large steps on thick epitaxial layers due to the phenomena of step bunching which generates an increasing step size with increasing layer thickness. A smooth morphology can only be achieved on very thick layers if the growth mechanism is stable.

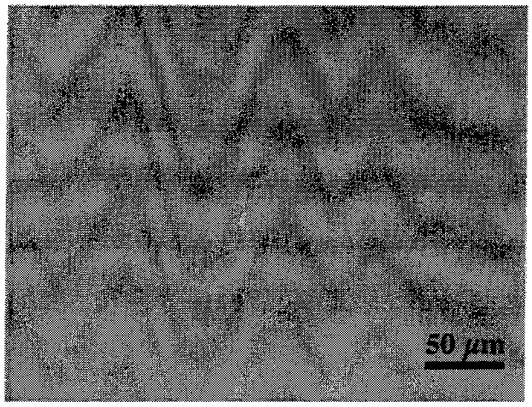
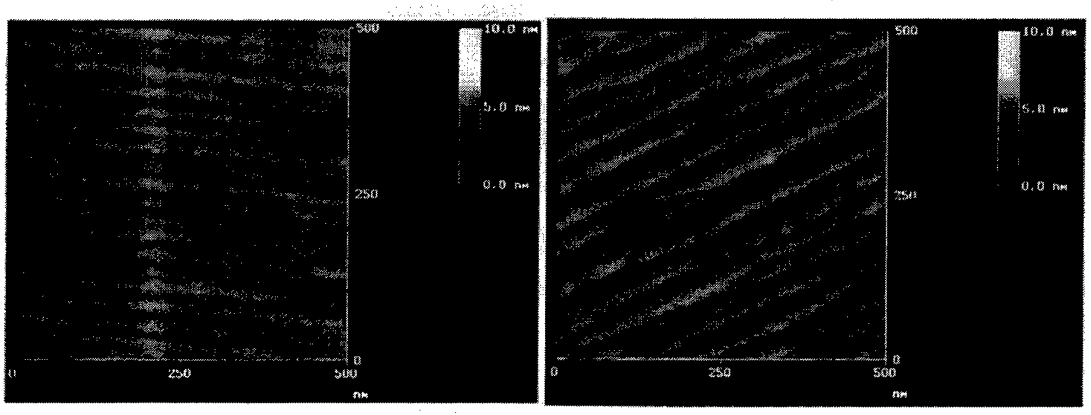


Fig. 2. Surface morphology of epitaxial layer (thickness ~120 μm) grown on the C-face of 6H-SiC.

Atomic force microscopy

By AFM a clear distinction of the surface structure of epitaxial layers grown on the Si and C-face is observed. On the C-face the steps are very regular and straight (Fig. 3a). On the Si-face (Fig. 3b) the steps are not as regular and the appearance is more roundish. The terrace widths varies. Evidently the widths are smaller and the step density is higher on the C-face compared with the Si-face. The average terrace widths on the C-face and on the Si-face are presented. The results might be compared with an AFM study on epitaxial layers grown by CVD [2] where the average terrace widths on the Si-face of 6H-SiC layers grown on substrates off-oriented 3.5° were 280 nm whereas the surface appearance on the C-face was flat. It has to be noted that the CVD layer thickness was only 5-10 μm but to our knowledge a similar study on thick epitaxial layers has not been reported. The difference in the surface structure of layers grown by sublimation epitaxy on the Si and C-face might be related to the difference in the surface free energy on the two faces, which affects the step-flow growth mechanism. A similar appearance occurs on the Si-face of 4H-SiC epilayers off-oriented 8° as for the 6H-SiC layers off-oriented 3.5°, i.e. the steps are not very regular and with a roundish appearance.



(a) (b)

Fig. 3. AFM image of vicinal 6H-SiC(0001) epitaxial layer surfaces. (a) C-face and (b) Si-face. Layer thickness ~120 μm.

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IMPURITY INCORPORATION BEHAVIOUR IN A CHIMNEY HTCVD PROCESS: PRESSURE AND TEMPERATURE DEPENDENCE

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Introduction

Silicon carbide has been recognised as a promising material for high-voltage devices, for which low-doped, thick epitaxial layers with good morphology are required. Within this goal, the use of a high temperature chimney reactor is proposed to increase the throughput of the SiC chemical vapour deposition (CVD) process. Simply described, the chimney system is a vertical hot-wall reactor, where the carrier and source gases flow upwards along the walls of the susceptor. In this paper, the influence of various process parameters, such as pressure, temperature and input C/Si ratio on the residual doping is investigated.

Experimental

The epitaxial growth was performed in the chimney reactor at high temperature (1750 - 1900°C) and reduced pressure. Growth rates in the range of 10 to 30 μm/hr have been achieved and mirror-like layers with N-doping within low 10^{14} to 10^{15} cm^{-3} range have been reproducibly obtained. A more detailed description of this system is given elsewhere [1]. The precursor gases were SiH_4 and C_3H_8 diluted in a H_2 carrier gas. A graphite susceptor in-situ coated by SiC on at least 60% of the total surface was used. Epitaxial layers were grown on commercial 4H-SiC substrates (8° off-axis towards $\langle 11\bar{2}0 \rangle$) of about 1x2 cm^2 in area, mounted on the inner walls of the susceptor. For comparison purpose, a Si-face and a C-face substrate were placed at the same height along the susceptor for each run. The input C/Si ratio was varied between 0.1 and 0.5 with the SiH_4 flow kept constant, and the pressure between 80 and 300 mbar at each C/Si ratio. The net-carrier concentration of the epitaxial layers was obtained by capacitance-voltage measurement (CV) on Au- or Ni-Schottky diodes and the N-doping was determined using photoluminescence (PL) at 2K by a PL-fitting method described previously [2]. The results from both methods agree well with each other for uncompensated n-type layers.

Results and discussion

Figure 1 shows the residual N-doping dependence on the total pressure for three C/Si ratios, with the growth temperature kept constant around 1860 ± 15°C. For comparison, the results from both C- and Si-faces are displayed in the same plot. A clear doping decrease on both Si- and C-face samples with decreasing total pressure is observed for all C/Si ratios. This effect can be attributed to a decrease of the residual nitrogen partial pressure with decreasing total pressure. The doping on Si-face samples decreases with increasing C/Si ratio under otherwise identical conditions, which agrees well with the

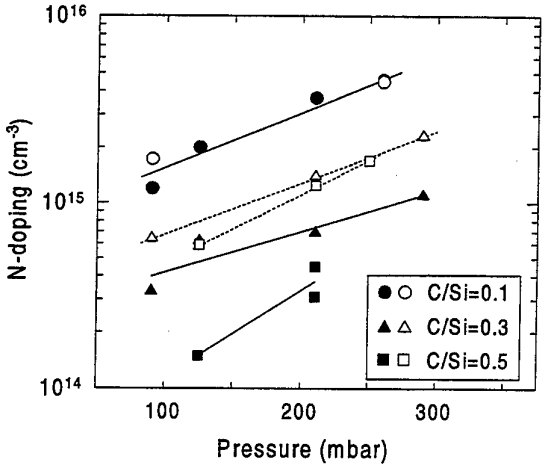

Fig.1 Nitrogen doping vs. growth pressure at constant T for three different C/Si ratios for epilayers grown on Si-face substrates (closed symbols) and C-face substrates (open symbols).

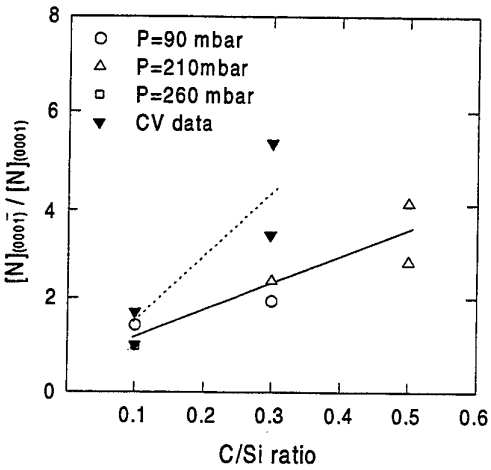

Fig.2 Ratio of the N-doping of the C-face to the Si-face epilayers grown during the same run as measured by PL fitting (open symbols) and CV (closed symbols).

site-competition principle [3, 4], where N-atoms occupy the C-lattice sites, and a higher concentration of C competes out N, thereby reducing the N-doping. Our results on the C-face (Fig.1, open symbols) show a similar N-doping decrease with increasing C/Si ratio, which differs from the previous observations [3, 4]. This may be related to the different growth conditions and doping range in the chimney system. Except for low C/Si ratios, the nitrogen incorporation is higher on the C-face than on the Si-face (Fig. 2). Moreover, higher C/Si ratios lead to an increased difference in N-doping between the Si-face and the C-face. This can be attributed to the larger effect of the C/Si ratio on the surface termination of the Si-face than that of the C-face [4].

Another leading parameter controlling both doping and growth rate is the process temperature. As shown in Fig. 3, a substantial decrease in the residual N-doping with increased growth temperature is observed. The apparent activation energy is of 200 kcal/mol, a value considerably higher than the one reported in [5]. The doping decrease may still be related to a surface process such as the nitrogen desorption rate, however superimposition of other effects cannot be ruled out: within the T range investigated here, the chemistry in the gas phase is observed to be shifted along the susceptor, and thus the effective C/Si ratio on the substrate surface is also varied.

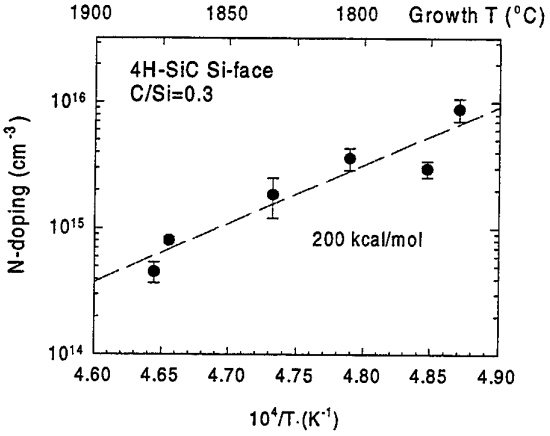

Fig. 3 N-doping vs. growth temperature in 4H-SiC epilayers grown on Si-face substrates at 210 mbar.

A qualitative understanding of the incorporation behaviour of other impurities such as Al and Ti is obtained by comparing the PL-spectra and the net carrier concentration measured by CV (Fig. 2). The most intensive Al and Ti related PL lines were observed for the samples grown with high C/Si ratio, which is consistent with the site-competition theory. When occuring, the incorporation of both Al and Ti is found to be significantly less on the C-face than that on Si-face, which can be related to the different surface termination.

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CLOSE COMPENSATION OF 6H AND 4H SILICON CARBIDE BY SILICON-TO-CARBON RATIO CONTROL

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Experimental results are reported for boron-doping of 6H and 4H silicon carbide epitaxial layers from a solid boron-nitride source. The purpose of these experiments is to demonstrate close compensation of the resulting CVD grown epitaxial layers by adjusting a single growth parameter, namely, the average ratio of silicon to carbon in the precursor gases during growth (i.e., site-competition epitaxy). Net doping concentrations from more than 10^{17} cm^{-3} n-type to more than 10^{17} cm^{-3} p-type are observed. Type conversion is principally correlated with the silicon-to-carbon ratio, while the precise degree of compensation is also determined by the proximity of the boron-nitride solid source to the heat source controlling the temperature of the boron nitride during CVD growth of the 6H and 4H SiC. Secondary Ion Mass Spectroscopy (SIMS) indicates that this is most likely due to source-limited doping of both aluminum and boron. The n-type compensating species is assumed to be nitrogen. At intermediate values of silicon-to-carbon ratio (typically between 0.11 and 0.2 for our particular conditions) close compensation is observed, and, possibly, semi-insulating behavior.

We have already reported that boron doping of SiC epilayers can be achieved by substantially heating solid boron-nitride wafers,[1] such as are commonly used in silicon processing as a boron diffusion source, upstream of a silicon carbide epitaxial film during growth via chemical vapor deposition (CVD). In those experiments, the silicon-to-carbon ratio was held constant. In these follow-on experiments, we grew a new set of samples at fixed spacings for the boron-nitride solid source, but adjusted the silicon-to-carbon ratio over a wide range ($0.066 \leq Si/C \leq 0.5$). The precursors used are silane and propane in a carrier of hydrogen. The silicon-to-carbon ratio is adjusted by fixing the flow of a gas mixture of 3% silane in hydrogen at 15 sccm, and then adjusting the flow of a gas mixture of 3% propane in hydrogen to achieve the desired Si/C ratio. The Si/C ratio was held constant by mass flow controllers throughout the growth run. The growth temperature for both 6H and 4H samples was approximately 1550°C.

Nine operating points in 6H and two in 4H have been investigated. An "operating point" is an ordered pair consisting of the position of the BN solid source with respect to the edge of the heated susceptor (in mm) and the silicon-to-carbon ratio. Figure 1 illustrates the doping matrix for 6H thus far completed. Also indicated are approximate boundaries for the p-type, n-type, and closely compensated or "*i*" regions. Also indicated by points in either the n or p-type regions are the approximate net doping densities as determined by capacitance voltage (CV) profiling. CV measurements were made with both the mercury probe technique and with nickel Schottky contacts, with generally good agreement. All samples in the matrix were grown on n-type substrates, but similar results are obtained for p-type substrates. SIMS measurements (not shown) generally confirm the strong dependence of both boron and aluminum dopant incorporation on silicon-to-carbon ratio first reported by Larkin.[2] Aluminum is a significant, but minority dopant species, probably arising from the aluminum oxide used as a sintering agent to form the BN wafers from powder. The x = 4.5 mm position produced results virtually identical to samples grown without BN, thus indicating that at this range no significant doping can be attributed to the BN solid source. At closer ranges ($x \leq 3$ mm) the BN contributes sufficient boron and aluminum doping to affect type conversion. At Si/C ratios of approximately 0.16, close compensation was repeatably observed. Very low capacitance was measured and profiling indicated virtually complete depletion of the 2-μm thick epi layer at zero bias. This indicates a net doping density of less than 10^{14} cm^{-3}, and possibly even semi-insulating material. Similar results have been observed with the two 4H samples prepared so far.

We continue to explore the "*i*" region for evidence of semi-insulating behavior. Two experiments are in progress, the results of which will be reported when available: (1) Admittance spectroscopy to determine the pinning of the Fermi level in the epi layers grown on conducting substrates, and (2) the growth of "*i*" epi layers on semi-insulating 4H substrates to permit unambiguous Hall measurement of the free carrier concentration.

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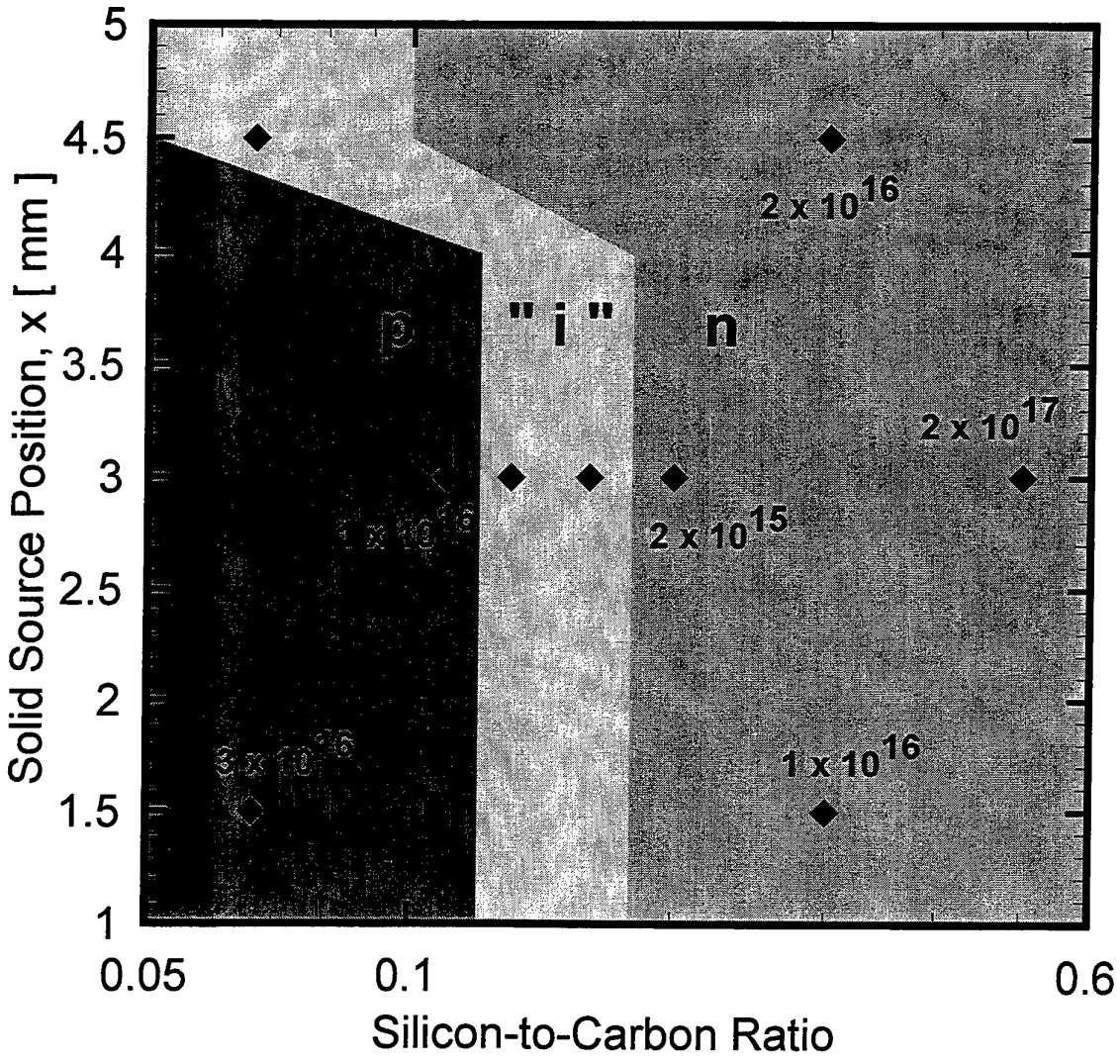

SILICON CARBIDE CVD HOMOEPITAXY ON WAFERS WITH REDUCED MICROPIPE DENSITY

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Reduced micropipe density substrates are important for improving SiC devices due to the reduction in catastrophic device failures caused by these defects. One technique for reducing the micropipe density has been developed and demonstrated.[1] This technique involves a two-step process: first the micropipes are filled using a slow growth technique, after which a layer is deposited using liquid phase epitaxy (LPE) to prepare the surface for subsequent device fabrication. It is well known that LPE layers grown on SiC result in poor surface morphology, with a high degree of step-bunching and related defects affecting the surface morphology. Reduced micropipe density substrates whose surface morphology contains this degree of surface features are clearly not optimal for subsequent SiC device manufacture; a method for improving the surface prior to the deposition of device layers is clearly needed.

CVD growth experiments have been performed using a cold-wall chemical vapor deposition (CVD) reactor at the Emerging Materials Research Laboratory (EMRL). Epitaxial layers of thickness on the order of 6-8 μm were deposited using a Si to C ratio of 0.3. SiC epitaxial wafers with reduced micropipe density (<10 cm^{-2}) manufactured by TDI, Inc. were used as substrates for CVD growth. Scanning electron microscopy (SEM) was performed before and after CVD epitaxial layer deposition to monitor changes in the surface morphology resulting from CVD growth. Figure 1 shows a SEM micrograph on one of the 4H-SiC reduced-micropipe density substrates before CVD. Clearly visible is the large degree of step-bunching (i.e., macrosteps) resulting from the LPE process. In addition, triangular defects also decorate the surface of the substrate which may also have resulted from the formation of macrosteps. Figure 2 shows the resulting surface quality after CVD growth; a clear reduction in the surface roughness is visible along with a reduction in the defects associated with the triangular features noted in the micrograph of Figure 1.

The CVD experiments were repeated on reduced micropipe density 6H-SiC substrates with a similar, but not as dramatic, reduction in the surface roughness. This paper will present both the preliminary results described above and future CVD experiments that are planned to optimize the surface texture. It is believed that a CVD buffer layer, similar to the layers grown during these preliminary experiments, could serve to finish the process of eliminating micropipes from the substrate that was begun with the initial micropipe filling and LPE capping of the micropipes. Device fabrication on these CVD layers are also planned to determine the degree of improvement achieved in device performance resulting from micropipe-reduced substrate density substrates with CVD buffer layers.

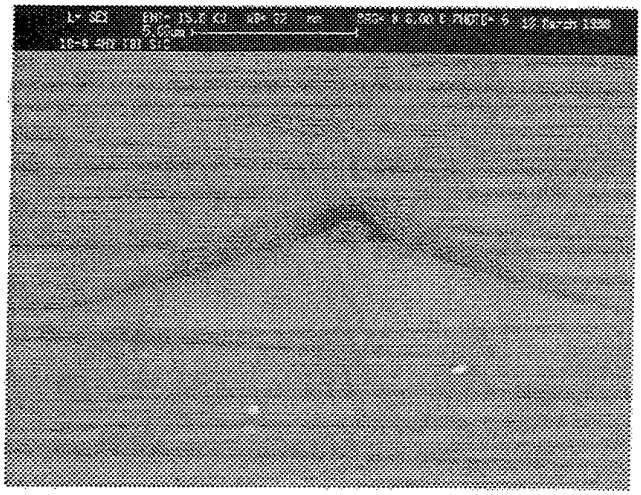

Figure 1 SEM micrograph of a 4H-SiC low micropipe-density substrate. Large degree of step-bunching and triangular defects decorate surface.

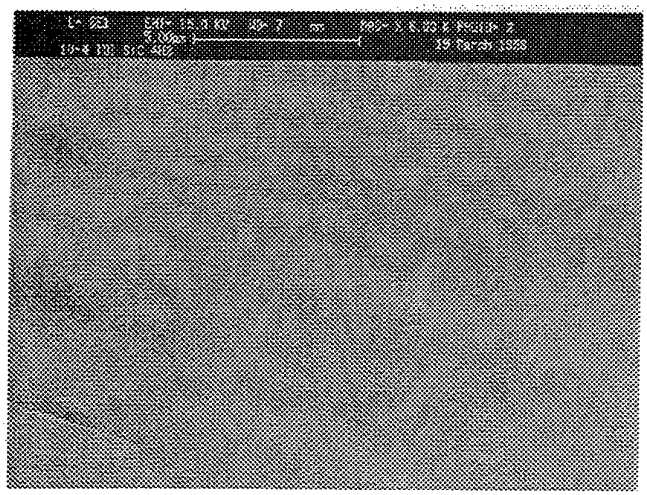

Figure 2 SEM micrograph of the low micropipe-density substrate of Figure 1 after 3 hours of CVD growth. Note greatly reduced surface roughness after CVD growth.

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KINETICS AND MORPHOLOGICAL STABILITY IN SUBLIMATION GROWTH OF 6H AND 4H-SiC EPITAXIAL LAYERS

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Silicon carbide (SiC) is an excellent semiconductor for use in high-power, high-frequency, and high-temperature devices due to its superior material properties. It has been demonstrated that high growth rates with a stable growth mechanism are possible to achieve by sublimation epitaxy [1]. The method offers an alternate technique for epitaxial growth of very thick layers with high structural quality and specular surfaces. The surface morphology is depending on the growth kinetics which determines the growth conditions and consequently the quality of the epitaxial layer. In this study the growth kinetics and morphological stability in sublimation epitaxy on vicinal 6H and 4H-SiC substrates are investigated.

Growth was carried out on the Si-face of quarter sections of Ø35mm 6H and 4H-SiC wafers. The wafer surfaces were 3.5°_or 8° off-oriented from the basal plane in the <11$\bar{2}$0> direction. Growth was performed at a reduced argon (ultra pure N60) pressure. The source to substrate distance was 1 mm and the growth time one hour. The sublimation epitaxy growth furnace used has been described elsewhere [1].

The layer thicknesses and interfaces were revealed by cleavages. An optical microscope with Nomarski interference contrast was used for studying the as-grown surfaces and the substrate/layer interfaces.

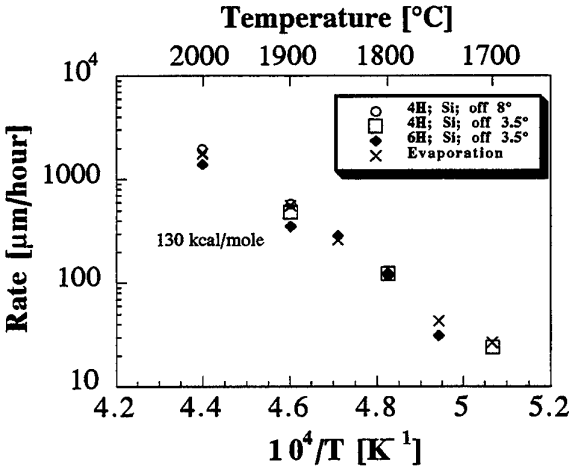

Fig. 1. Arrhenius plot of the growth rate of layers grown on different SiC substrates and sublimation rate of the source.

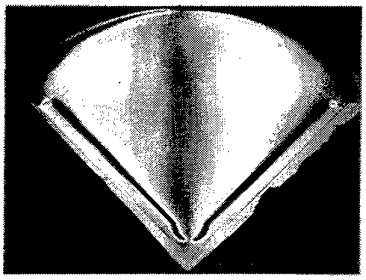

Fig. 2. Epitaxial layer grown by sublimation epitaxy.

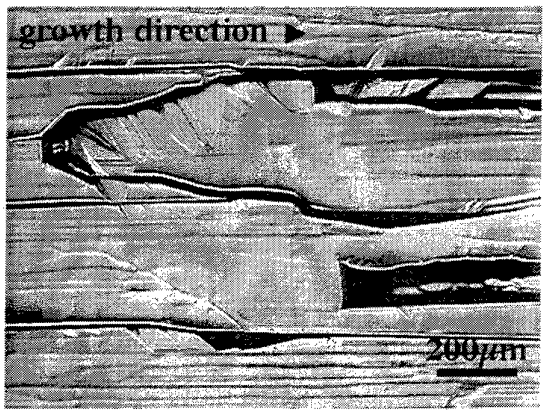

Fig. 3. Morphology roughening due to nucleation on terraces.

The Arrhenius plot of the growth rate is shown in Fig. 1. The dependence yields an apparent activation energy of 130 kcal/mole for both 6H and 4H-SiC independent of the substrate off-angle. This value is attributed to the sublimation process of the SiC source material. The growth rate clearly follows the sublimation rate of the source, Fig. 1. Thus the rate determining step is determined by the source surface kinetics. The value of the activation energy for the growth process is discussed in relation to the activation energy for sublimation of the main Si and C containing species from SiC.

With proper growth parameters the as-grown surfaces are specular and the morphology is smooth, Fig. 2. However, under certain conditions the morphology may deteriorate. The window for morphological stability is given by the substrate (off-orientation and polytype), the growth environment and the growth temperature (rate). On 6H-SiC substrates off-oriented 3.5°, the morphology is smooth for growth temperatures up to 1950°C but at this temperature growth disturbances appear. For 4H-SiC substrates off-oriented 3.5° the growth becomes disturbed to a large extent at 1900°C, Fig. 3. If the off-orientation increases, the probability of growth disturbances decreases. For 4H-SiC substrates off-oriented 8° no growth disturbances have been observed up to temperatures as high as 2000°C which is very remarkable when considering the growth rate at this temperature. The critical temperatures and growth rates for maintaining morphological stability are collected in Table. 1.

Table 1. Critical temperatures and growth rates for occurrence of growth disturbances.

Substrate	Temperature [°C]	Growth rate [mm/hour]
6H; Si; off 3.5°	~1950	~1.0
4H; Si; off 3.5°	~1800	~0.1
4H; Si; off 8°	>2000	>2.0

4H-SiC(0001) vicinal surfaces have a shorter terrace width than 6H-SiC due to the different values of the c-axis. For CVD growth it has been observed by TEM that the terrace width of epitaxial layers grown on 3.5° off-oriented substrates is larger for 4H-SiC than for 6H-SiC [2] as a consequence of the step-bunching phenomena. Our results are compared with growth conditions for 2D nucleation appearance on terraces in CVD step-flow growth. Even though CVD and sublimation epitaxy are different growth techniques, the results are reasonably close to the observed growth disturbances in our work. These facts suggest that two-dimensional nucleation on the terraces may also be responsible for morphological disturbances in sublimation epitaxy.

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TEM study of SiC layers grown by LPE in microgravity and on ground conditions

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Liquid Phase Epitaxy (LPE) is a suitable method to grow SiC layers. High quality 6H and 4H SiC layers and p-n junctions have been grown by LPE (1) in the temperature range of 1600-1800°C. The choice of this technique can be advantageous when thick epitaxial layers are needed as for example for fabrication of high power SiC devices. Pure SiC layers were grown by LPE from silicon solvent (2), but the growth rate is limited to a few micrometer per hour because the solubility of carbon in a silicon melt is low. By introducing scandium into the silicon melt the solubility of carbon is increased and growth rates as high as 350 μm/h have been achieved (3) in the Si-Sc-C system. However, growth from solution with high growth rate may result in morphological instabilities and defect formation due to the gravitation-induced convection. LPE growth under reduced gravity gives the possibility to eliminate a growth parameter which is not possible to control under normal conditions.

The aim of the present study is to describe the structure of SiC layers grown at microgravity conditions and to give a comparison to the layers grown at identical conditions in the laboratory, on ground.

Liquid phase epitaxy of 4H- and 6H-SiC was performed by using a modified travelling solvent method (4). The growth utilized a container-free sandwich configuration with a Si-melt between a SiC source material and a SiC substrate. To obtain layers with reasonable thickness during several minutes in microgravity, 40 % of Sc was alloyed with the Si solvent. (0001) oriented, Si face 6H-SiC and 4H-SiC substrates were used for the LPE experiments. The SiC layers were grown at 1750°C for 240 seconds.

The grown layers were characterised by Transmission Electron Microscopy (TEM).

The layers grown at microgravity followed the polytype of the substrate in all of the cases. No other polytypes have been found in 4H layers grown on 4H substrate and in 6H layers grown on 6H substrate. The grown layers are macro defect free and the original substrate/layer interface can hardly be detected by TEM. The surfaces of the grown layers are always faceted showing larger and smaller steps (Fig. 1). This is explained by the minimisation of the surface free energy during growth.

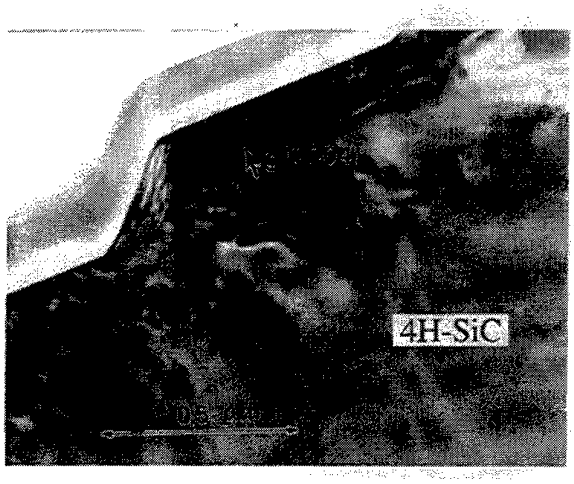

Fig. 1: Surface region of a 4H-SiC layer, grown at microgravity, in cross section showing a step on the surface and defects in the near surface region.

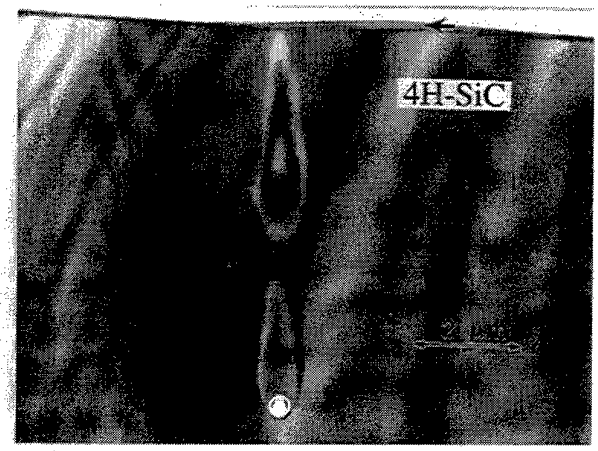

Fig. 2: Cross section of a 4H-SiC layer grown by LPE on ground showing a small micropipe which pierces the foil at about the depth of 7 μm.

In the 6H and 4H SiC layers grown on ground as control samples the extended defects described below were observed although the grown layers followed the polytype of the substrate again.

- In a 6H-SiC layer an elongated cavity has been found. The internal wall of the cavity is buried by nanocrystalline 3C-SiC. Our explanation for this is that the cavity was formed during the growth of the 6H SiC layer and the 3C polytype nucleated during the cooling down process at low temperature.
- In the 4H layers grown onto 4H-SiC substrate some holes were found and identified as micropipes which lay in the TEM foil, elongated to the [0001] direction and pierce the foil at a certain depth (Fig. 2).
- Scandium carbide precipitates were also found in 4H layers grown on ground and were identified as $Sc_{15}C_{19}$ grains by electron diffraction.

6H and 4H-SiC layers have been grown by LPE at microgravity conditions and on ground as well. The surface of the layers is always stepped. There are more defects, mainly dislocations in the near surface region of the layers than in the deeper regions. Scandium carbide precipitates, micropipes, cavities are found in the SiC layers grown on ground, but none of them were traced in the layers grown at microgravity conditions. This shows that the quality of the hexagonal SiC layers grown at microgravity conditions in this experiments was better than the quality of the layers grown on ground.

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NEW RESULTS IN SUBLIMATION GROWTH OF THE SIC EPILAYERS.

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The method of sublimation growth was one of the first techniques which enabled obtaining epitaxial SiC layers of device quality [1]. This method and also some of its modifications [2] have been used to fabricate quite a number of semiconductor devices [3]. In the present work, a modification of the sublimation sandwich method in an open system [2] was used. N-SiC epilayers were grown in vacuum on (0001)Si surface of 6H-SiC Lely substrates. Growth temperature was ~ 2000 ^{o}C. It was used Ta growth cell, which was carbonized in high vacuum. Vapour source - polycrystalline SiC powder-occupied in growth cell volume equal to ~ 1 cm^{-3} .

Investigations of the influence of Si vapour pressure and the temperature gradient inside the growth cell on the background doping level, morphology, and polytype homogeneity of growing epitaxial layers enabled optimizing the temperature regime of "in situ" etching of the substrate and the layer growth (decreasing of the temperature gradient between source and substrate). Changing of the growth cell annealing regime led to changing phase contents of SiC vapour source. Phase contents was tested by electron spectroscopy method (ESCA) and X-ray difractometry (XRD) before and after optimisation of the growth cell annealing regime. This reduced the background doping level of the obtained epitaxial layers. As a result of the modification performed, we obtained n-type epitaxial 6H SiC layers with an Nd-Na concentration of ~1 10^{15} cm^{-3}.

X-ray studies have shown that the structural perfection of the obtained n-type layers compares well with that of Lely substrates used in growth (dislocation density ~ 10^{2}-10^{3} cm^{-2}) [4].

Layers of n-type were used to fabricate Schottky diodes for which C-U measurements indicated homogeneous doping of the layers across their whole thickness (~5 μm)(see figure).The figure shows that at reverse voltage about 60 volt the thickness of space charge region (SCR) is practically equal to thickness of the epilayer. After father increasing of reverse voltage SCR is extended to the substrates (Nd-Na ~ 3 10^{18} cm^{-3}). Breakdown of this Schottky diodes (diameter 1200 μm, without any periphery protection) take place at ~400 V.

DLTS measurements done on diodes fabricated on the basis of the given layers have shown that the concentration of (deep acceptors (L and D centres) is by approximately an order of magnitude lower than in epitaxial layers grown by the same method prior to modifying the growth technique. The diffusion length of holes in the layers under study was 1.2 - 1.4 μm, which, firstly, is a record-breaking value for SE layers and, secondly, confirms the low degree of compensation of the layers.

The investigations carried out show that the method of sublimation epitaxy can be used to obtain layers nearly as good (as regards the background doping level and degree of compensation) as those grown by the CVD technique.

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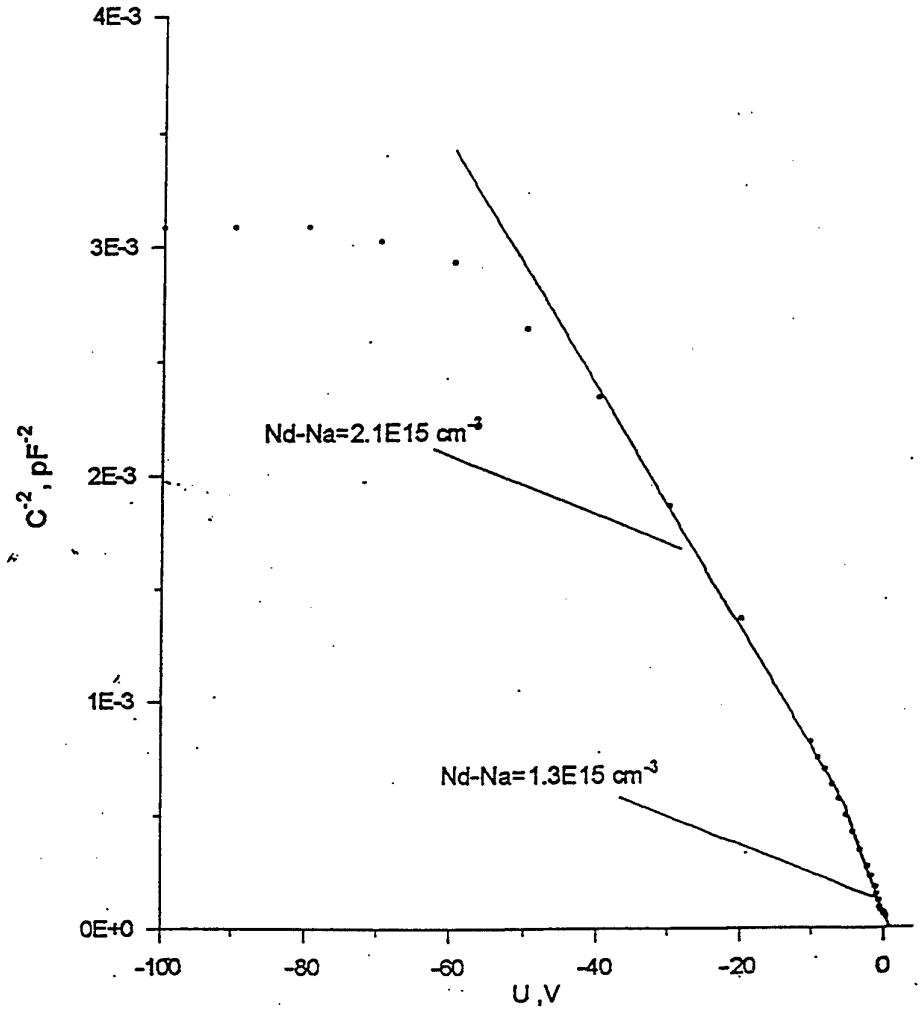

C-V characteristic of the Schottky diode (Diameter 1200μm) formed on base of sublimation grown epilayer.

DOMAIN MISORIENTATION IN SUBLIMATION GROWN 4H-SiC EPITAXIAL LAYERS

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One of the major reasons for macro-defects and domain formation in sublimation grown SiC material is the curvature and thus, misorientation in the material. The domain structure in the epi-layers is usually inherited from the substrate. The development of the domain structure will naturally depend on the growth conditions, but also to a large extent on the stresses in the substrate and on the bending of the substrate. It is essential to obtain information on the domain misorientations and bending existing in the substrate in order to understand domain formation in the epitaxial growth.

In the present work, thick 4H SiC epilayers and the substrates were studied. The growth was performed using sublimation epitaxy [1]. Quarter sections of a commercially available ϕ 35 mm Cree wafer were used as substrates. The wafer was double-side polished research grade (0001) wafer of 4H polytype, cut 8° off towards $<11\bar{2}0>$ direction. Doping of the wafer was $2.9\text{x}10^{19}$ cm^{-3} and the micropipe density was between 31-100 cm^{-2}. The wafer was divided into quarter sections by cutting along and perpendicular to the $<11\bar{2}0>$ direction. On two of the wafers growth was performed on the Si-face and on two of them on the C-face. On both faces 1 and 2 h growth runs at 1800°C at an Ar pressure of less than 1 mbar were performed. The layer thicknesses were approximately 100 and 200 μm, respectively. The morphology of the layers were smooth, mirror like. Occasionally stripe like defects along off-axis direction $<11\bar{2}0>$ were observed. The good morphology and absence of large defects indicate stable growth conditions.

The 4H SiC substrates and epi-layers were studied with high resolution X-ray diffraction. The measurements were performed with a Philips MRD 1880/HR diffractometer with a 3 kW Cu source (λ=1.54Å) at 45 kV and 40 mA. The triple-axis configuration was utilized using Ge(220) monochromator and analyzer crystal in front of the detector. The triple-axis mode provides a good resolution which enables separation between diffraction peaks of the different domains. Rocking curves, $2\theta/\omega$ scans and reciprocal space maps were recorded. The overall bending of the samples were measured and diffraction topographs were recorded placing the film behind the analyzer crystal to determine which parts of the sample were diffracting revealing the domain shape and size. Two different beam sizes were utilized. The X-ray beam hitting the sample was approximately 1x9 mm^2 or 1x4 mm^2. The beam was elongated perpendicular to the diffraction plane.

To study the domain structure occurrence the measurements were first conducted on the substrates. The whole wafer had a higher doped area in the middle in which the domains were less bent compared to each other resulting in a curvature of hundreds of meters. The rocking curves exhibited a single peak with relatively narrow full widths at half maximum (FWHM) of typically 12". On the Si-face the wafer was convex on the left side and concave on the right side. The bending was measured by comparing the change in the peak position of the rocking curve with change of the beam position in respect to middle of the wafer (Fig. 1). The higher doped area on the left side seemed to have different curvature than the right side.

Towards the edges of the wafer the rocking curve FWHM broadened and more peaks appeared, especially if there were macro-defects as revealed by crossed polarizer optical images.

The quarter of wafers were also separately studied after cutting but before the growth run. In the growth experiments on the Si-face the misorientation was increased especially in the case of the thinner epilayer. When the layer thickness increased in the 2 h growth run the domain structure and misorientation were more comparable to the substrate. This improvement with increasing layer thickness along with the high growth rate indicates that sublimation epitaxy is suitable for growth of very thick layers.

In the growth runs performed on C-face the epilayer domain structure resembled that one of the substrate. In the rocking curve there was one broader peak instead of separated peaks from different domains. This indicates smaller misorientation between the domains. However, the epilayers were much stronger curved which also increased the FWHM of the rocking curve.

The results are further discussed in terms of domain and structure evolution in the epi-layer due to substrate domain structure and polarity.

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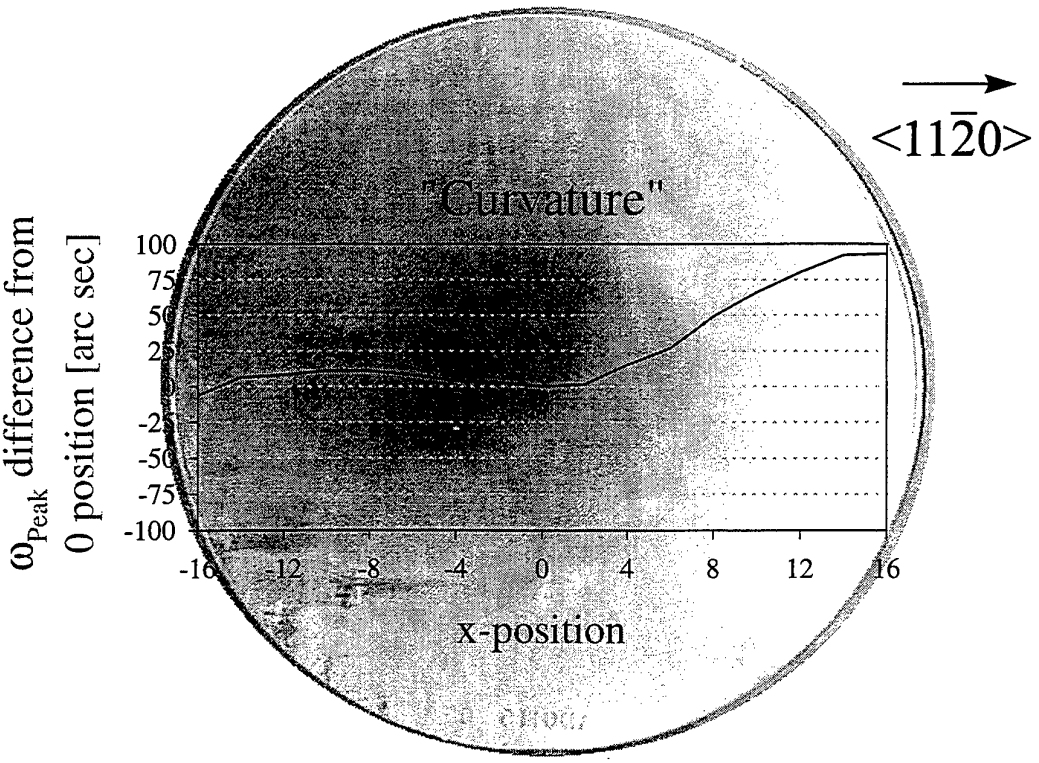

Fig. 1. A crossed polarizer image from the Si side of the 4H SiC substrate used in the growth experiment. A darker area in the middle shows the higher doped area and especially on the lower left corner a couple of macro-defects are seen. The curve shows the difference in the peak position of the rocking curve compared to the center of the wafer, i.e. x-position 0.

CONCENTRATION TRANSITION LAYERS IN SIC EPITAXIAL LAYERS DOPED BY ALUMINUM

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Concentration transition layers arising in SiC epitaxial structures grown by sublimation sandwich method are studied. Two kinds of structures are examined. One of the structures includes, first, low-doped ($N_D=10^{16}$–10^{17} cm^{-3}) n_--type SiC layer, and second, p^+-epilayer doped by aluminum ($N_A=10^{20}$–10^{21} cm^{-3}). As a result a n_--p^+ (Al)-structure is formed. The second structure is obtained by growing Al doped layer on the p-doped substrate followed by deposition of n_--type SiC epilayer (the p^+ (Al)-n_--structure).

Low-doped n_--epilayers are grown at temperature of 1800-1900°C in vacuum. p^+-SiC layers doped by Al are grown at higher (>2200°C) temperature in argon atmosphere.

Dopant distribution over transition area is characterized by CV-technique using the p-n-junctions formed in the structures and Schottki barrier formed on the surface of the structures in combination with its etching.

It is shown that high-quality sharp p-n-junctions ($t_{tr} < 0.1$ μm) can be formed only by growing p^+ (Al)-n_--structures at high (>2400°C) temperatures. At lower temperatures increase of donor concentration near p-n-junction is accompanied by defect cathodoluminescence with specific D_1 spectrum.

The results obtained allow determination of the diffusion coefficient of Al in solid SiC which is found to be 2-3 order of magnitude less than in the case of Al diffusion into SiC from the vapor phase. The peculiarities of Al diffusion in SiC are explained by existence of two different states of Al in SiC crystalline matrix. One of them is substitution of Si atoms by Al (Al_{Si}) and another is the complex of Al and carbon vacancy (Al-V_C). Existence of the later complex has been recently confirmed by Electron Paramagnetic Resonance (EPR). The complex Al-V_C is stable at least up to temperature of 2400°C and is a deep acceptor ($E_A \cong 0.5$ eV). It is assumed that at lower temperatures these complexes are injected into the crystal from the vapor phase. Due to partial dissociation of these complexes a high concentration of the vacancies near p-n-junction is created that is registered by photoluminescence. However, in the case of solid-phase diffusion from the Al-doped layer concentration of such complexes is lowered drastically. This results in lower migration rate of Al in SiC crystal.

In n_--p^+ (Al)-structures considerably thicker transition layer with non-uniform dopant distribution is observed. The thickness of this layer is 2-3 μm on (0001)C and 4-5 μm on (0001)Si substrates, respectively. To analyze the nature of these transition layers not only the value of Al diffusion coefficient is taken into account, but also the efficiency of dopant transport through the vapor phase and due to surface diffusion while growing undoped epilayer on the highly-doped substrate. These results show an important role of surface diffusion in autodoping of SiC epilayers.

MODELING OF SILICON CARBIDE CHEMICAL VAPOR DEPOSITION IN A VERTICAL REACTOR

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Chemical Vapor Deposition (CVD) of Silicon Carbide (SiC) epitaxial layers is important technique to manufacture electronic devices for different applications.

The vertical CVD reactor considered in the present paper consists of rotating bell-jar-like graphite susceptor heated by inductive coil, a SiC-coated substrate holder on the top of the bell-jar, and a water cooled wall made out of stainless steel [1]. Optimal CVD process has to provide possibility to grow reproducibly epitaxial layers with uniform distributions of properties - thickness, doping concentrations, etc. For this control of transport of Si- and C-containing species to the growing layer and Si/C ratio over the wafer is of crucial importance. It was shown in [2] that chemical processes in the reactor especially the gas phase nucleation of Si-droplets are critical to control the Si/C ratio over the growing epilayer. In the present paper new results of modeling of the deposition and the gas phase nucleation in the vertical CVD reactor are presented.

Velocity vectors and temperature distribution are shown in Figs. 1 and 2 for a typical growth process. One can see a stable flow pattern and temperature isolines parallel to the susceptor surface in the vicinity of the wafer.

The calculated growth rates (dashed lines) are shown in comparison to experimental values (solid lines) in Fig.3 and Fig. 4. Varying the propane inflow results in the calculations in a linear dependence of the growth rate on propane supply until C/Si ratio becomes close to unity. A good agreement between experimental and numerical results is obtained only at a C/Si input ratio less than 0.6 corresponding to the values of propane inflow less than 3.3 sccm (see Fig. 3). It is obtained in the calculations that the SiC growth rate is increasing linearly with silane inflow until the input C/Si ratio becomes equal to one and the theoretical and experimental values of the growth rate are different in the whole range of variation of silane flow rate. In the present paper a detailed model of chemical processes during CVD of SiC is proposed. It is shown that the gas phase nucleation of Si-droplets occurs over the wafer during the deposition. This explains the difference in the experimental and theoretical results obtained without taking into account the nucleation. When the deposition process is performed under significant excess of silane supply and the growth is limited by carbon, the nucleation is not critical and experimental

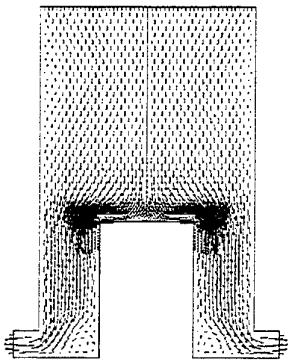

Fig.1 Velocity vectors

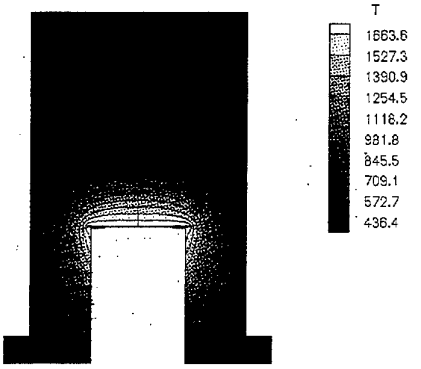

Fig.2 Temperature distribution

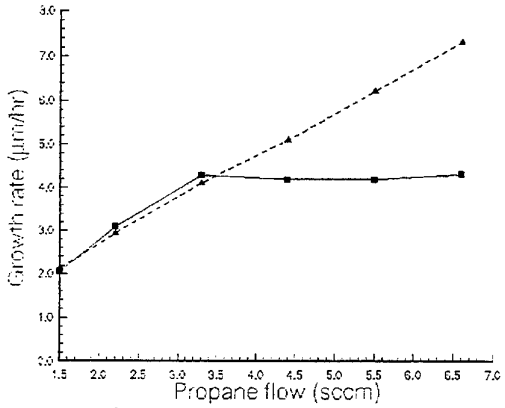

Fig.3 Growth rate vs propane flow

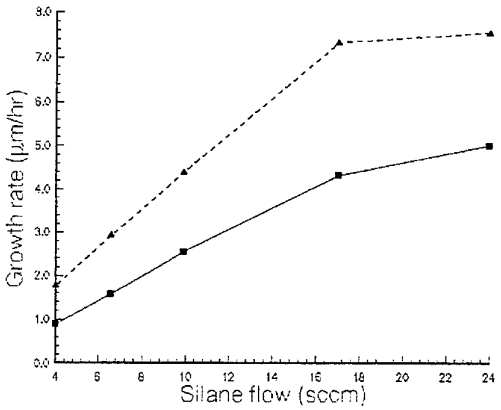

Fig.4 Growth rate vs silane flow

and modeling results are in good agreement (Fig. 3). But, by exceeding the C/Si ratio 0.6 one can see lack of Si at the growing layer which is result of the gas phase nucleation and transport of the Si-droplets outside from the wafer. Taking into account the gas phase nucleation improves accuracy of the modeling results.

In the present paper a modeling analysis of formation and transport of Si-droplets is performed and it is shown that the gas phase nucleation is affected by total pressure, flow rates of the carrier gas and precursors, and growth temperature. Possibilities to control the nucleation in the vertical reactor are studied by using modeling.

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MODELLING ANALYSIS OF GAS PHASE NUCLEATION IN SILICON CARBIDE CHEMICAL VAPOR DEPOSITION

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Chemical Vapor Deposition (CVD) is an important industrial technology for growth of silicon carbide (SiC) epitaxial layers for making different devices. It was found that silicon droplets appear over the wafer due to gas phase nucleation during which can be seen via viewport of the reactor as an irradiating layer [1]. In Fig. 1 a photo is shown where the irradiating layer over the susceptor can be seen. Some amount of silicon atoms is stored in the form of the clusters and does not participate in the growth. This effect changes the C/Si ratio over the growing epitaxial layer and, therefore, properties of the epilayer. Thus, it is important to reduce the silicon droplet formation by selection the appropriate process parameters. In the present paper a mathematical model of the gas phase nucleation is proposed which can be used for modeling analysis of the SiC deposition process.

The model is based on Navier-Stokes equations for flow, heat- and mass transfer with taking into account gas phase chemical reactions and spontaneous condensation of Si-droplets. The value of the rate of formation of the droplets of critical radius is determined from the classical theory by Zel'dovich and Frenkel. Transport of the condensed droplets is described by the conservation equation for the condensed phase.

Modeling of the nucleation process has been performed for the case of the vertical CVD reactor for the process conditions close to that used in [1]. Temperature distribution along the streamline is an important parameter determining the chemical processes and the gas phase nucleation. On the axis of the reactor the temperature changes from 300 K at the inlet to the value of the temperature at the surface of the wafer T_m. The calculated axial distributions of Si-vapor and amount of Si in condensed phase are shown in Figs. 2 and 3 for different values of T_m. One can see that for the case of growth temperature 1800K all the silicon vapor formed in the gas due to decomposition of silane is condensed and only Si-droplets are present in the gas phase over the wafer. Further increase of the growth temperature results in decomposition of the Si-droplets in the heated area over the susceptor and for the temperatures larger than 2100K the droplets fully decompose in the vicinity of the wafer.

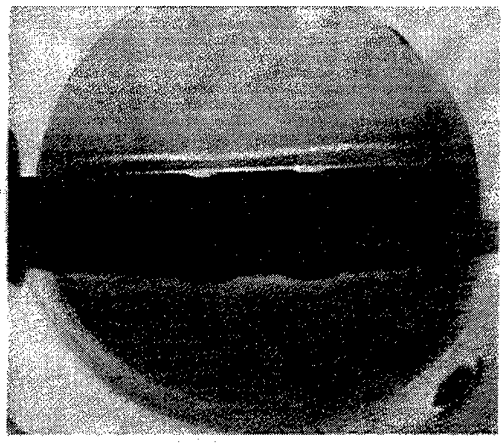

Fig.1 Photo of irradiating layer over the susceptor

Input flow rate of silane is important parameter determining the gas phase nucleation. It is obtained in the calculations that for every deposition process there exists a boundary value of supply of silane which, to be exceeded, results in start of the nucleation. The explanation is quite transparent. The gas phase nucleation is driven by supersaturation of the Si-vapor over the liquid Si-phase which has to be exceeded to start the nucleation process. It is shown also that increase of total pressure during the deposition results in more intensive gas phase nucleation.
Detailed analysis of the nucleation process and its dependence on the process parameters is presented in the paper.

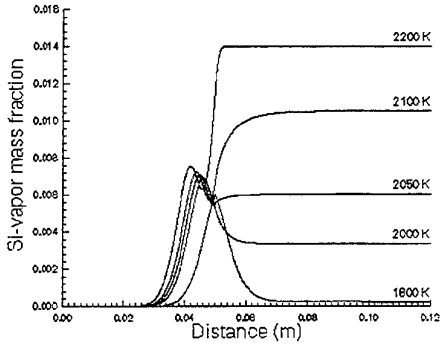

Fig.1 Axial silicon vapor distribution

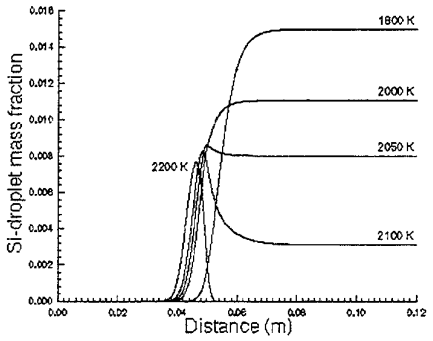

Fig.2 Axial silicon droplets distribution

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DOPING OF SILICON CARBIDE BY NITROGEN DURING SUBLIMATION GROWTH

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Sublimation sandwich method is one of effective techniques for growing of single crystal and epitaxial layers of SiC doped by different elements. It provides well controllable growth of the crystals with extremely high doping level.

In this work growth and doping of 6H- and 4H-SiC by nitrogen is investigated. Growth is carried out in the temperature interval of 1900-2400°C. Temperature drop between the source and the substrate is varied from 10 to 100°C. Normally gaseous nitrogen is served as the dopant source. The nitrogen partial pressure is varied in the range of 10^{-7}-1.5 atm. Hall concentration of dopant is measured in the temperature interval of 77-1100 K.

It is found out that nitrogen lowers growth rate of SiC crystal. This effect is the most pronounced while SiC growing on (0001)C surface with low supersaturation. We give detailed analysis of influence of nitrogen on the growth rate. We derive the following relationship between donor concentration and nitrogen partial pressure: $N_D = 10^{18}\sqrt{P}\exp\left(1146\frac{\text{kJ}}{\text{mole}}/RT\right)\ \text{cm}^{-3}$, where P is the nitrogen partial pressure. The dependence $N_D \propto \sqrt{P}$ is valid in the whole range of pressure variation. There is no saturation even at the pressure as high as 1-1.5 atm. Adding into the growth system other nitrogen compounds (such as acetonitrille) does not result in the increase of the doping level under these conditions.

The doping level increases with lowering of SiC growth rate. Variation of the growth temperature from 2400°C down to 1900°C leads to increasing of the maximum dopant concentration from $1.8\cdot10^{20}$ cm^{-3} to $4.8\cdot10^{20}$ cm^{-3}. Therewith electron Hall mobility remains between 30 and 35 $cm^2/V\cdot s$ in 6H-SiC.

Analogous behavior is exhibited in the case of growth on (0001)Si substrates, although nitrogen concentration is in this case 1.5-2 times lower. Dependence of the doping level on substrate orientation is also essential for small (<1°) misorientation of growing surface from the singular plane.

It is shown that introduction of Si vapor in the growth chamber results in a weaker dependence of the growth rate on the substrate orientation.

The coefficients of nitrogen incorporation by crystalline SiC matrix as a function of nitrogen partial pressure, temperature and surface orientation is determined.

At low pressure ($P<10^{-5}$ atm) decrease of the nitrogen incorporation efficiency under growth rate increasing is observed. This effect is quantitetively explained by nitrogen adsorption kinetics.

Mechanisms of nitrogen incorporation into SiC crystal from the vapor phase is discussed.

X-RAY INVESTIGATIONS OF MBE-GROWN HETEROEPITAXIAL SIC LAYERS ON 6*H*-SIC SUBSTRATES

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3*C*- and 4*H*-SiC thin films have been investigated by means of high resolution X-ray diffraction techniques (ω/2Θ-scan, ω-scan, φ-scan) and X-ray topography. The SiC films were grown in a solid source molecular beam epitaxy (MBE) system on 6*H*-SiC substrate crystals at depositions temperatures in the range from 780°C to 950°C and growth rates in the range from 30 nm/h to 120 nm/h.

The symmetric high resolution X-ray diffractogram shows two clearly separated family reflections (6*H*-SiC: 00.12; 3*C*-SiC: 222), which have their origin in the 6*H*-SiC substrate and SiC thin film, respectively. This indicates a significant difference of the c/q lattice parameter (q - number of Si-C double layers per unit cell) in the order of $0.252 \cdot 10^{-3}$ nm (Fig.1).

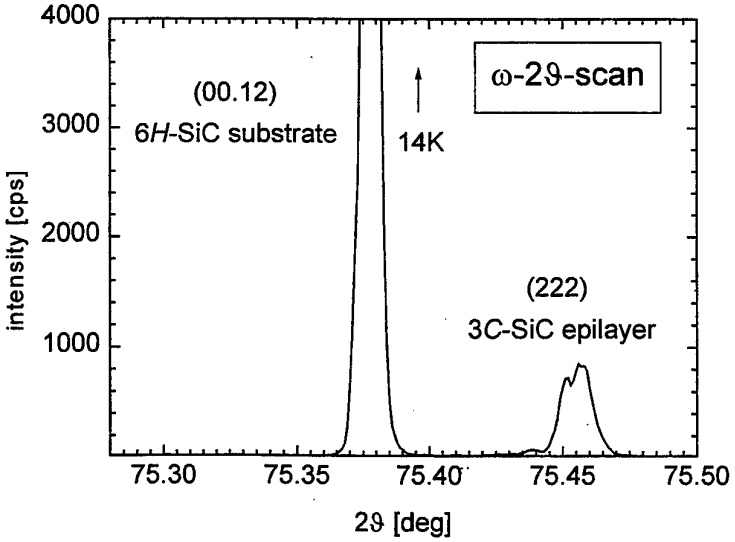

FIG. 1: High resolution X-ray diffractogram of MBE deposited 3C-SiC thin film on 6H-SiC substrate. ω-2ϑ-scan of the symmetric 6H-SiC 00.12 and the 3C-SiC 222 reflection, respectively.

We also investigated the lattice mismatch parallel and perpendicular to the [0001]-direction. For this we used the so called "reciprocal space mapping" technique. Rocking curves were measured at several fixed 2ϑ-positions. We got a two-dimensional image of the reciprocal space close to a reciprocal lattice point (Fig 2). In the case of 3*C*-SiC on 6*H*-SiC the epilayer had crystallographic pseudomorph structure (lateral lattice fit, normal allowed lattice difference) i.e. there is almost no lateral lattice mismatch. The mismatch parallel to the *c*-axis $\Delta c/c$ was $8.7 \cdot 10^{-4}$.

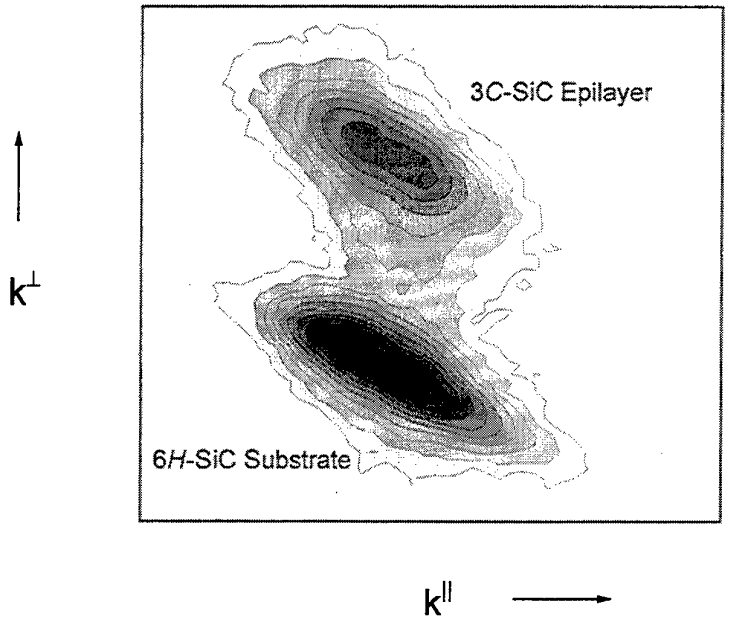

FIG. 2: Reciprocal space mapping of the asymmetric 11.12 reflection of a 1.2 μm MBE grown 3C-SiC layer on a 6H-SiC Substrate.

When 3*C*-SiC films were grown on 6*H*-SiC substrates, double position boundaries (stacking sequence ACB instead of ABC) were frequently observed. For the visualization of this effect high resolution X-ray topographic measurements are investigated at 3*C*-SiC layers on 6*H*-SiC substrates. We find, that the domains of different stacking sequences are equally distributed in the 3*C*-SiC epilayer. The size of this domains is approximately $200 \times 200\ \mu m^2$.

6H-SiC site competition epitaxy in silan-metan-hydrogen gas system

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The majority of works concerned with epitaxial growth of SiC have been carried out in the system silan- propan-hydrogen. However another interesting possibility is to use silan-methan-hydrogen system [1]. Methan behaves much different from propan as carbon precursor for CVD growth of SiC layer[2].In this work we report on an investigation of 6H-SiC epitaxial layers grown by using atmospheric pressure CVD with a CH_4-SiH_4-H_2 gas system. A distinctive feature of our reactor is that the reactor heater are made of glassy carbon tube, instead of graphit. This a high purity matherial has a density of glass and conductivity of graphite. The glassy carbon was not covered with SiC intentionally. In this study were used p+ substrates from Cree.Under a fixed growth condition, background doping strongly depends on the C/Si ratio of source gases. With an increase of C/Si ratio in gas phase ther is a tendency to discrease concentration N_D-N_A up to 10^{15}-10^{13} cm^{-3} (site competition epitaxy) [3].Experiment on site competition were performed in two temperature intervales:(1)1420-1450 and (2)1580-1620 ^{0}C..The growth was performed in a horisontal reactor with a hot wall. Methan (10%inAr) and silan (5% in Ar) were used as sources gases and hydrogen was used as a carrier gas.The epilayers are characterised by volt-capacitence measurments and results of i-DLTS spectroscopy. Depending on the C/Si ratio in the gas phase epitaxial layers exhibited (or not) condaction type inversion.When the C/Si ratio was increased from 1 to 5 ,the N_D-N_A value changed from $3*10^{18}$ to $4*10^{15}cm^{-3}$. Further increase in the C/Si ratio from 5 to 15 changed the type of conduction with the N_A-N_D concentration increase from $8*10^{15}$to $5*10^{17}$ cm^{-3}. At T=1580-1620^{0}C the conduction type inversion occured at C/Si ~0.5. The shift of the inversion point towards lower C/Si rations with increasing temperature may be due to an increase in the activity of methan molecules. Investigation of the concentration dependency N_D-N_A (N_A-N_D) on the C/Si ratio in the gas phase and comparision of technological conditions of growth clearly divided samples studied into two categories; a) etched "in situ" with H_2,

b) not etched with H_2.A pregrowth treatment of 6H-SiC substrates in hydrogen was performed at $T=T_D$ for 1-2h. Etching in hydrogen improves the surface perfection and half-width of the rocking curve becomes narrower[1,4].Expet the etching action such a prolonged purging of the reactor at high temperature presumably reduce the amount of adsorbed nitrogen. Thus, "in-situ" etching with H_2 prior to epitaxial growth allows one to reduce the concentration in a growing layer by an order of magnitude.

Here we present too, the preliminary result obtained by current spectoscopy method (i-DLTS).The measurment were mainly perfomed at low temperature, which enabled us to detect deep centers with energies <0,5 eV.All the detected donor-like deep centers can be divided into three groups: $Ed_1 \Rightarrow$ (0.1-0.13) eV, $Ed_2 \Rightarrow$ (0.17-0.23) eV, and $Ed_3 \Rightarrow$ 0.35-0.42) eV and acceptor-like deep centers can be divided into two groups: $E_{A1} \Rightarrow$0.10-0.12eV, $E_{A2} \Rightarrow$0.17-0.24eV. A comparison of technological conditions under which samples with different trap depths were grown showed that pregrowth treatment correlates with the trap depths for both the donors and acceptors. A trap depth is shallower if an epitaxial layer is grown on a substrate subjected to "in situ" etching with H_2. Such a correlation is presumably due to inheritance of the more ordered substrate surface structure obtained as a result of prolonged etching at high temperature.

Investigation has shown that layer conductivity is governed at any of the observed N_A-N_D values by the presence of deep acceptor centers lying in the energy interval E_V+(0.10-0.24)eV whose parameters are close to those of structural defects (for exampl, E_V+0.24eV always present in sublimation grown 6H-SiC layers [5].This resalt does not agree very well with the physical model given in[3]. From our point of view, changes in the N_D-N_A value in epilayers, occuring when the C/Si ratio is varied ,can also be explained by changes in the concentration of acceptor-like defects, as it was shown for sublimation grown epitaxial laers.

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STABLE SURFACE RECONSTRUCTIONS ON THE 6H-SiC($000\bar{1}$) SURFACE

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The (0001)-orientation of SiC crystals is the most commonly used in growth experiments and therefore important in all other kinds of research concerning SiC. Several groups have studied these surfaces extensively with a variety of surface-sensitive techniques (for a more recent review see [1]). The aim is to identify the electronic and atomic structure of the surfaces, which may affect their behavior as an interface in many different situations, e.g. during growth or metallization or in hetero-polytype junctions. Significant progress has recently been achieved in clarifying the stable configurations on the Si-terminated surfaces. Our group succeeded in solving the complex Si-rich (3×3)-reconstruction [2]. With this result it seems possible to explain that this structure promotes the polytype reproduction during crystal-growth as previously reported. The reverse crystal orientation, i.e. ($000\bar{1}$) for hexagonal polytypes, is known to exhibit a different behaviour in all aspects. In particular, growth experiments result in different polytypes on the two surfaces. Differences are also expected for the stable surface structures, yet, only few studies were performed on this topic.

In this paper we present a compilation of low-energy electron diffraction (LEED) and Auger electron spectroscopy data (AES) of four well ordered structures, namely the ($\sqrt{3}\times\sqrt{3}$)-R30°, (2×2), (3×3) and (1×1)-high temperature phases (STM-studies are currently in progress). The first structure was prepared *ex-situ* by means of a microwave-powered hydrogen plasma. A different phase exhibiting a (1×1)-LEED pattern resulted from an oxidation and subsequent removal of the sacrificial oxide with hydroflouric acid (HF). A close relationship between these structures is indicated by the similarity of integer-order beam intensities recorded for samples prepared with either method. The other surface phases were prepared *in-situ* by heating the sample with or without additional Si-flux generated by an electron-beam evaporator.

Starting from a thick Si-film ($d_{Si}\geq 10$Å) deposited on the SiC surface at room temperature, several phases can be prepared by subsequent heating (Typical LEED patterns are shown in fig. 1). At substrate temperatures around 700°C the silicon film desorbs completely, revealing an intermediate (1×1)-phase. The Si/C-ratio derived from AES data of this phase are somewhat uncertain and depend strongly on the cumulative heating time, but the Si/C ratio is always ≥2 (see tab. 1). Heating the Si-covered substrate at T=1250°C-1300°C for max. 60 s results in (2×2)-ordered surfaces, while (3×3)-ordering is achieved when using T≥1350°C for 60 s. However, the best ordered (2×2)-phases resulted from heating the surface at T~1100°C while simultaneously exposing the sample to a silicon-flux (15-20nA) for typically 15 min. The (2×2)-structure can be transformed into the (3×3)-structure when applying T≥1350°C for 30 s or

lower temperatures at longer times (e.g. T=1250°C for several minutes). Further heating with T≥1400°C for several minutes leads to a (1×1) high temperature phase. This behaviour is in close analogy to that observed for the Si-terminated surfaces, i.e. heating at higher temperatures and longer times results in depletion of silicon at the surface. However, preparation parameters and resulting periodicities are different for both orientations. Also, on the $(000\bar{1})$-surface, we often observe a coexistence of (2×2)- and (3×3)-phases over a wide temperature range, which cannot be explained simply by a temperature gradient on the sample. This indicates a rather high and similar stability of these phases. Furthermore we found by AES measurements, that heating the surface at T~1000°C results in a silicon enrichment, which is in sharp contrast to the behaviour of the Si-terminated surfaces. Occasionally, we observed a transition from a (Si depleted) (3×3)- to a (Si rich) (2×2)-phase during these experiments. Possibly, these surface structures are energetically very stable and Si-desorption is kinetically limited.

These remaining questions could be solved, if the structures of the surface phases were known. Until now, neither structure is completely determined. A comparison of the integer-order LEED-I(E)-diffraction intensities indicates, that the (2×2)-structure is similar to that of the ex-situ prepared $(\sqrt{3}\times\sqrt{3})$-R30°, the disorderd (1×1) and intermediate (1×1) phases. In contrast the (3×3)-spectra are significantly different in the low energy range implying a massive reconstruction of this surface. This is supported by STM-data of other groups [3].

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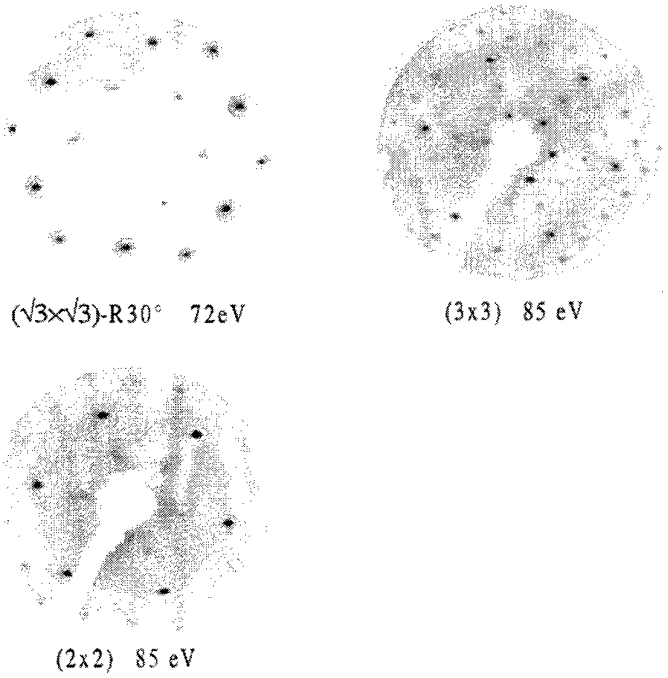

fig. 1
LEED patterns of the investigated structures

Surface phase	Si/C ratio
$(\sqrt{3}\times\sqrt{3})$-R30° / disordered (1×1)	**0.44** (O/C ratio **0.15**)
(1×1) intermediate	≥2
(2×2)	**1.94**
(3×3)	**0.50**
(1×1) high temp.	**0.41**

tab. 1
Si/C ratios derived for the different investigated surface phases

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WEAK PHONON MODES OBSERVATION USING INFRARED REFLECTIVITY FOR 4H, 6H AND 15R POLYTYPES.

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[33] 04 76 82 63 78 [33] 04 76 82 63 94

Beyond its technological interests for the high frequency and/or high power electronic applications, SiC presents a great scientific interest driven by its prolific polytypism. The origin of the polytypes, their structural and electrical properties, have attracted many theoreticians and experimenters along this century [1 - 4]. Because the band gap energy and the electrical properties differ from one polytype to an other, these two interests in SiC are meeting. This makes polytypes identification a crucial point for the SiC crystal growth.

In this paper, Infrared reflectivity is presented as a powerful tool for SiC polytype identification. Indeed, the weak folded modes, commonly observed in Raman spectroscopy [5 - 8], can be found using IR reflectivity for the extraordinary ray. This was first reported in the pioneer work of Spitzer et al. [9] who has observed a weak mode on top of the Reststrahlen band for 6H-SiC. More recently, a detailed study for 6H-SiC has been published [10], but no results for other common polytypes are still available. We present here IR reflectivity spectra of 4H, 6H and 15R SiC grown by the modified Lely method. The sample were cut parallel to the c axis. In this configuration, the weak modes with A_1 symmetry arising from the folding of the axial optic branch (see Table 1), can be observed on the top of the Reststrahlen band between TO and LO frequency (Figure 1). Just as it was reported for Raman spectroscopy [7], the number and the position of these folded modes is characteristic of the polytype. Using a classical Lorentz oscillator model, firstly reported by Spitzer et al. [9] for 6H-SiC, the oscillator fit parameters (frequency, oscillator strength and broadening) of these A_1 modes have been determined for the 6H polytype and, for the first time, in the case of 4H and 15R polytypes.

Table 1 : Phonon symmetry at Γ point for 4H, 6H and 15R polytypes. x represents the reduced wave number of the phonon modes in the large Brillouin zone [5].

4H		6H			15 R	
x = 0.5	x = 1	x = 0.33	x = 0.67	x = 1	x = 0.4	x = 0.8
2 B_1 (silent)	A_1	2 B_1 (silent)	$2A_1$	2 B_1 (silent)	2A	2A

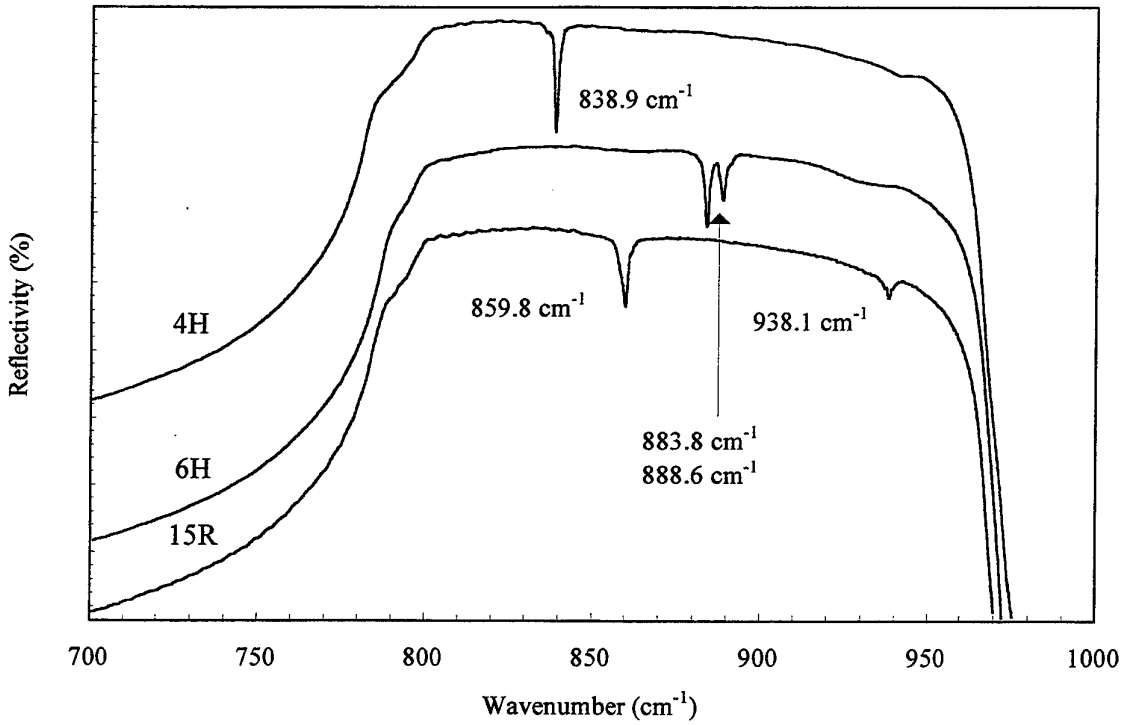

Figure 1 : Infrared reflectivity spectra of 4H, 6H and 15R SiC for the extraordinary ray. The frequency of the weak folded modes are reported on the graph. The spectra have been shifted for clearness.

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EFFECTIVE MASSES OF 6H AND 4H-SiC - CYCLOTRON RESONANCE EXPERIMENTS

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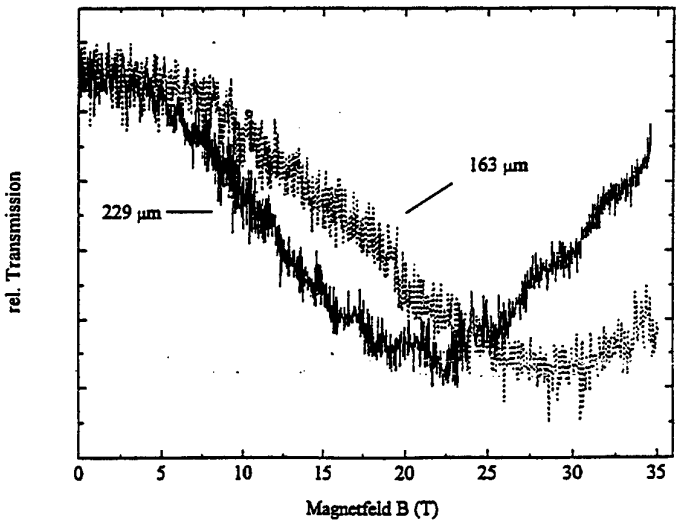
We report on the first high magnetic field cyclotron resonance measurements in high quality 6H and 4H-SiC single crystals. The experiment were carried out under pulsed magnetic fields up to 50T, successively oriented along the three principal axes of the single crystals. In the case of 6H polytype, when the magnetic field is set parallel to the c axis the magneto-transmission leads to cyclotron mass equal to $m^* = (0.45\pm0.02)$ m_o. For two directions of the magnetic field perpendicular to the c axis, the magneto-transmission spectra clearly evidence the anisotropy of the effective masses in the M-Γ-K plane of the Brillouin zone. In the case of the 4H polytype, the measurements give a cyclotron mass of $m^* = (0.42\pm0.02)$ m_o for B∥c and a lower mass is determined for B⊥c. The mobility and the scattering time of the electrons were obtained from the fits of the cyclotron resonance line shapes for 6H and 4H-SiC.



The cyclotron resonance in 6H-SiC (B∥c) at T = 180 K.

HIGH-PRECISION DETERMINATION OF ATOMIC POSITIONS IN 4*H*- AND 6*H*-SIC CRYSTALS

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The atomic structure of the two SiC polytypes, 4*H*- and 6*H*-SiC, differs by the stacking sequences of the Si-C bilayers in the [0001] direction. The stacking arrangement for these polytypes is shown in Fig. 1. Both polytypes belong to the hexagonal crystal system. The space group for both polytypes, 4*H* and 6*H*, is $P6_3mc$ (C_{6v}^4).

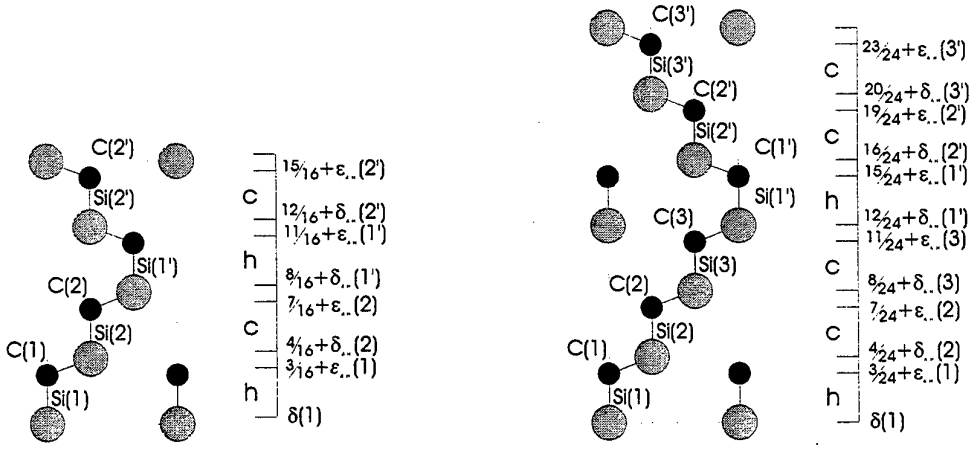

FIG. 1: The atomic structure of 6H- and 4H-SiC. The atomic coordinates in c-direction are given in terms of the basic vector. δ(i) and ε(i) are the relative atomic displacements of the Si atoms and C atoms respectively. These relative displacements are in the order of 10^{-4}.

Conforming with the space group symmetry, the atoms are in principle allowed to move freely in [0001]-direction. The bonding tetrahedra are pressed or stretched (atomic relaxations). These atomic relaxations are determined by means of high-precision X-ray diffraction measurements and *ab-initio* calculations. The calculations were performed in the framework of pseudopotential-density-functional theory in the local density approximation.

For the experimental determination of these atomic relaxations it is necessary to measure very weak reflections, so called "quasiforbidden" reflections. For these reflections, the structure factor *F(hkl)*, where *(hkl)* are the Miller indices of a corresponding lattice plane, is different from zero only for nonvanishing atomic relaxations. Using the "quasiforbidden" reflections has the following advantages: In contrast to the strong reflections, the "quasiforbidden" reflections are very sensitive to changes of the relaxation model. The kinematic approximation and the strict dynamic calculation have almost the same values for the integrated reflectivity. Consequently a correction of extinction is not necessary. Moreover the integrated intensity of the "quasiforbidden" reflexes does not depend on the crystal perfection. The structure factors of the "quasiforbidden" reflections are determined by the integrated intensities of measured rocking curves. The refinement parameters (atomic relaxations) are calculated from the structure factors by using a linear equation system.
The measured and calculated data are compared and discussed in detail. A comparison of the measured structure factors with those for calculated geometries is given. The atomic relaxations within the unit cell are derived from the calculations as well as from the X-ray measurements. We find a good agreement between the calculated and the experimental data.

REFLECTION AND TRANSMISSION X-RAY TOPOGRAPHIC STUDY OF SiC CRYSTAL AND EPITAXIAL WAFER

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We have studied defects in SiC crystals by transmission and reflection X-ray topography. The specimens are commercially available 4H-SiC wafers with 5μm N-doped epilayers.

Figure 1 shows an X-ray transmission topograph by a conventional Lang method. White broad lines shown near the wafer periphery of the upper part of the specimen are dislocation bundles which are probably induced by heavy thermal stress during crystal growing. Other dislocations are distributed homogeneously in the whole wafer except some regions of the wafer center, in which dislocation density seems to be smaller. Small dots shown in the whole region of the wafer are confirmed to be due to the line defects penetrated along the perpendicular of the specimen surface as explained below.

Figure 2 shows an O.M.D. (Oscillating method using Monochromatic Divergent beam)[1)] reflection topograph taken from the epitaxial surface of the other specimen. Many fine lines and sharp wide lines shown in Fig.2 are corresponding to dislocations and grain boundaries, respectively. Small black dots surrounded by white circular rings correspond to the white dots shown in Fig.1. It is shown that the distribution of the dots in Fig. 2 is the same as that of the reflection topograph taken from the rare surface of the same specimen. Therefore, the dots are due to the line defects which penetrate perpendicular to the specimen surface. Some grain boundaries are shown to be induced from the dot defects. This result

shows that the large stress accompanied with the defects is released by introduction of the grain boundaries. The dot defects are thought to be the same one called as the micropipes.

Thus, the O.M.D. topograph gives clear topographic image of the specimen surface. The defect structure and the origin will be discussed based on the reflection topographic images in comparison with the transmission ones.

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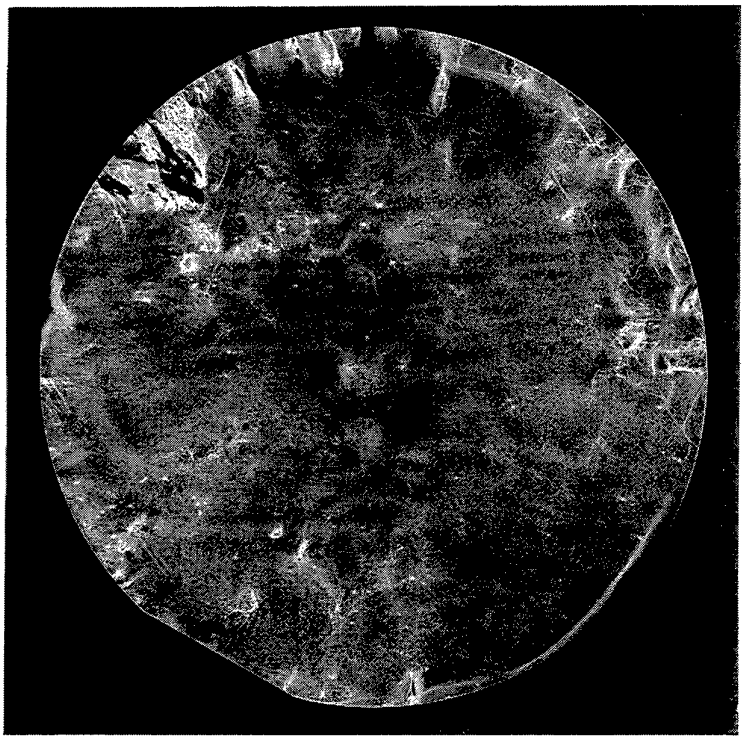

Fig. 1 X-ray transmission topograph. **g**=(1 0 -1 0).

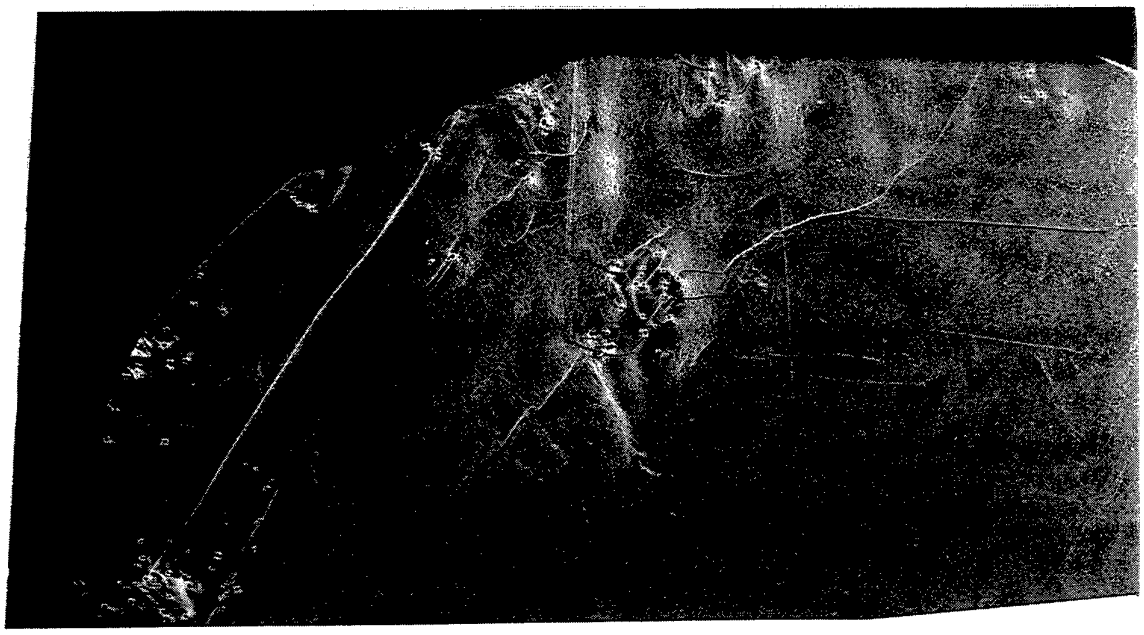

Fig. 2 X-ray reflection topograph. **g**=(1 0 -1 9).

A MODEL FOR DOPING-INDUCED BANDGAP NARROWING IN 3C-, 4H-, AND 6H-SiC

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In devices containing adjacent layers or regions with different types doping concentrations, doping induced band edge displacements may greatly influence device behavior. This is so because the shifts in band edges represent a potential barrier which influences carrier transport across the junctions. In this paper, a model for doping-induced band edge displacements and band gap narrowing will for the first time be derived for the polytypes 3C, 4H, and 6H of SiC.

The physical basis for band edge displacements is quite easy to understand. In an undoped and otherwise defect-free semiconductor, the energy gap corresponds of course to the energy needed to promote one electron from the completely filled valence band to the completely empty conduction band. In a doped semiconductor, however, there are interactions which are not present in the perfect crystal but which affect the band gap. These interactions are, in the case of n-type dopants, (i) the interaction between a conduction band electron (e) and the "gas" of conduction band electrons introduced by the doping (giving the energy contribution $\hbar\Sigma_c^{ee}$), (ii) the interaction between a conduction band electron and the ionized donor (d) ions, screened by the majority carriers ($\hbar\Sigma_c^{ed}$). These two types of interactions will shift the conduction (c) band edge. Since any measurement of the band gap involves an electron-hole pair, one must also consider (iii) the interactions between a (minority) hole (h) with the gas of conduction band electrons ($\hbar\Sigma_v^{he}$), and (iv) the interaction between a (minority) hole and the (screened) ionised donor ions ($\hbar\Sigma_v^{hd}$). (We neglect the interaction between a hole and other minority holes because of their low concentration.) These latter types of interactions will displace the valence (v) band edge. The case of p-type material is completely analogous. The contributions to the electron and hole energies stemming from these interactions (i.e., the $\hbar\Sigma$'s) are usually called self-energies. The calculation of the various self-energies have been based on ideas presented by Jain and Roulston[1] and by Berggren and Sernelius[2], and assumes zero temperature.

To simplify the mathematics, both the conduction bands and the two valence bands (heavy-hole and light-hole bands) are assumed to be parabolic. The valence bands are furthermore treated in a spherical approximation.

n-type SiC: The changes in conduction band minimum and valence band maximum, respectively, can be expressed as

$$\Delta E_c = \hbar\Sigma_c^{ee} + \hbar\Sigma_c^{ed} \quad \text{and} \quad \Delta E_v = \hbar\Sigma_v^{he} + \hbar\Sigma_v^{hd} \qquad (1)$$

and the bandgap narrowing ΔE_g is defined as $\Delta E_g = -\Delta E_c + \Delta E_v$. Following Ref.1 the self-energy $\hbar\Sigma_c^{ee}$ is approximated with 0.75 times the Hartree-Fock exchange energy, assuming the general case of three different electron effective mass components[3,4]. To calculate the self-energies $\hbar\Sigma_c^{ed}$ and $\hbar\Sigma_v^{hd}$ a random distribution of donor ions is assumed[2]. The self-energy $\hbar\Sigma_v^{he}$, describing a minority hole moving in the electron gas, has been considered by Mahan[5], using the plasmon-pole approximation for the electron screening. We have essentially followed Mahan's prescription, but performed the algebraic manipulations in a more careful way.
The results can be summarized with the formulas

$$\Delta E_c = A_{nc}\cdot\left(\frac{N_D^+}{10^{18}}\right)^{1/3} + B_{nc}\cdot\left(\frac{N_D^+}{10^{18}}\right)^{1/2} \quad \text{and} \quad \Delta E_v = A_{nv}\cdot\left(\frac{N_D^+}{10^{18}}\right)^{1/4} + B_{nv}\cdot\left(\frac{N_D^+}{10^{18}}\right)^{1/2} \qquad (2)$$

where N_D^+ is the density of ionized donors, hence explicitly taking into account incomplete ionization of donors. The coefficients A and B can be expressed in terms of fundamental material parameters. The resulting band edge displacements are shown in Fig.1.

p-type SiC: The treatments of p-type and n-type semiconductors are very similar. In the present contribution we have, however, improved the description of the hole gas dielectric function, and based the evaluation of the self-energy for a minority electron moving in the gas of majority holes on a two-band dielectric function for a hole gas in the plasmon-pole approximation. The final results can be expressed in the same way as eq.(2) but with N_D^+ replaces by N_A^-, the density of ionized acceptors. The band edge displacements are plotted in Fig.2.

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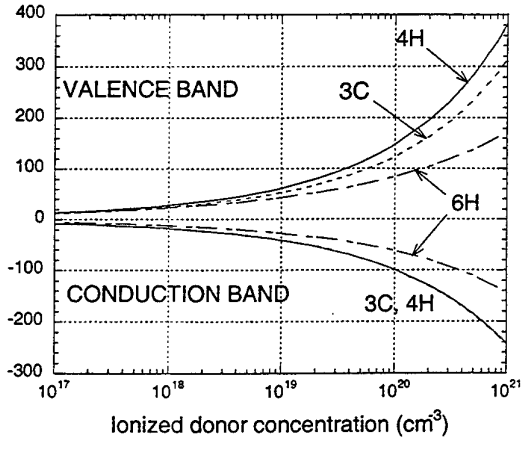

Fig.1

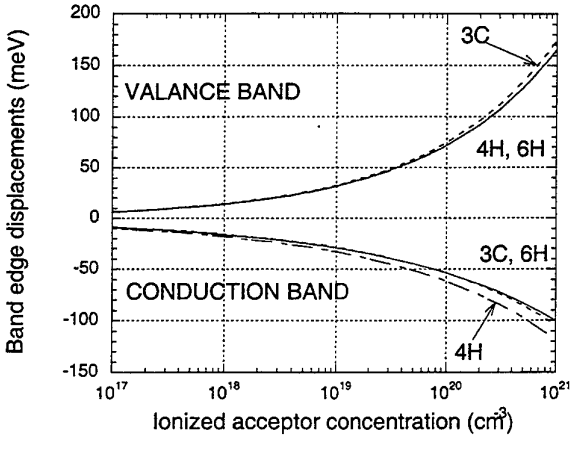

Fig.2

ACCURATE PENETRATION DEPTHS IN THE ULTRA VIOLET FOR 4H SILICON CARBIDE AT SEVEN COMMON LASER PUMPING WAVELENGTHS

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It has been recognized for some time that in carrying out low temperature luminescence studies on expitaxial layers of SiC that substrate interference can be a major concern. An accurate knowledge of the penetration depths of the various lasers commonly used to pump the specimens, especially in 4H SiC, is not available in the literature to date. The lack of data for 4H SiC is due to the fact that suitably pure and thick specimens have only become available in recent years.

In this report we focus on 4H SiC and give values of the penetration depth (α^{-1}) for seven commonly used laser wavelenths. The range of observations reported here is from 3900Å to 3250Å. We have carefully measured the absorption coefficient α (cm^{-1}) in this range using two specially prepared 4H SiC crystals of high purity. One crystal was thinned to 64μm and the other to 399μm. Several light sources and detection techniques were employed. Measurements were carried out at 300K and the estimated error in the determination of the absorption coefficient at 300K is about one percent. For luminescence measurements the penetration depth of the laser light at 2K is more relevant. We therefore have estimated the absorption coefficient at 2K by shifting the absorption curve at 300K by 30meV to higher energy. 30 meV is roughly the shift in the band gap from 300K to 2K [3]. Table 1 gives our results for seven laser wavelengths commonly used to study 4H SiC.

It should be pointed out that that the penetration depth of the laser light may not be the only reason for the observation of spurious signals from the bulk substrates. The phenomenon of photon recycling has been studied by us in $Al_xGa_{1-x}As$ / GaAs [1,2] and may be equally applicable to very pure epitaxial layers of SiC on boule wafers of SiC. In those studies we showed that in MBE $Al_xGa_{1-x}As$ / GaAs grown layers of high purity photon recycling is responsible for producing luminescent signals from depths more than one hundred times the penetration depth of the exciting light. Several groups, including our own, have observed signals from the substrates of epitaxial SiC when the thickness of the epilayers was several times the penetration depth of the exciting light. However, photon recycling has not, as yet, been proven to be responsible for this additional luminescence.

Table 1: Absorption coefficient of 4H SiC at seven common laser wavelengths for 300K and 2K.

	T=300K		T=2K	
Wavelength Å	α cm^{-1}	Penetration Depth (α^{-1}) μm	α cm^{-1}	Penetration Depth (α^{-1}) μm
3250 : He-Cd Laser	1354	7.4	1156	8.6
3336 : Ar^+ ion Laser	864	11	750	13
3371 : N_2 gas Laser	720	14	617	16
3511 : Ar^+ ion Laser	289	35	225	44
3540 : He-Cd Laser	228	44	169	59
3550 : 3 X Q / Nd :YAG Laser	209	48	155	64
3564 : Kr^- Laser	184	54	133	75

In the talk, if time allows, we shall also discuss the issues involved in the phenomenon of photon recycling as it might apply to luminescence studies of pure epitaxial SiC films on boule SiC substrates.

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PHOTOLUMINESCENCE OF 4H-SIC : SOME REMARKS

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4H-SiC has a potential as a material for high power device applications. Improvement of the material quality has been made and low temperature photoluminescence (LTPL) measurement has proven to be a useful method to evaluate the quality of the material. However, the understanding of a LTPL spectrum is not straight forward, specially for the characterization of films grown on substrate. In this paper we will present some typical examples such as LTPL spectra from n-type substrates, epilayers with various quality, as well as the temperature dependence of the near bandgap emission. We will show that both the wavelength of the excitation source and the quality of the layer influence the interpretation of the LTPL data.

First we will report on the various spectra which could be obtained from substrates (see fig 1). At low nitrogen concentration ($< 2 \cdot 10^{18}$ cm^{-3}) the near bandgap emission is dominated by the well-known N bound-exciton (N-BE)[1]. The relative intensity of the two N-BE, P_0 and Q_0, and their phonon replicas varies with the nitrogen doping. When the doping level increases the LTPL spectrum changes dramatically and is more looking as the recently reported broad spectrum of the shallow boron acceptor[2].The possible recombination channels are addressed.

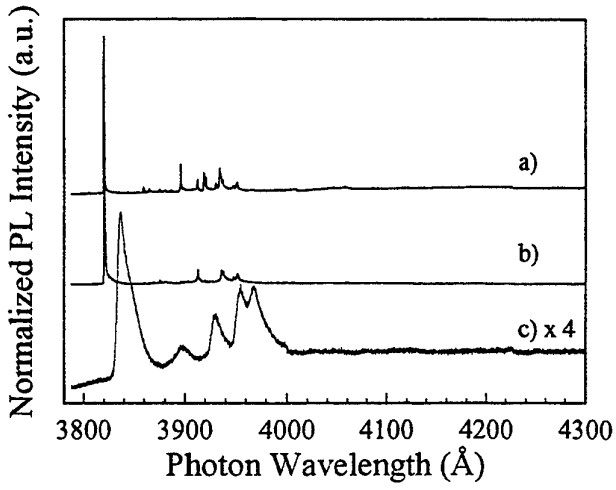

Fig.1 : Low temperature (2K) spectra of n-type 4H substrates with nitrogen doping concentration of $3.2 \cdot 10^{17}$ cm^{-3} a), $1.3 \cdot 10^{18}$ cm^{-3} b) and $6.5 \cdot 10^{18}$ cm^{-3} c), respectively.

When epilayers are grown on these various substrates the use of LTPL for the characterization of the layers should be done with precaution. First the penetration of the laser line used as excitation source is of importance, however, the depth or volume of characterized material is also depending on its purity. If using the 351 nm of an Ar ion laser as excitation line, luminescence from the substrate appears easily from a spectrum recorded from thin layer (few microns thick), whereas this feature is not observed (or less observed) using the 244 nm frequency doubled line of an Ar^+ ion laser (FReD). The choice of the 244nm line should be thus ideal for the characterization of thin layer. However we will show that even with this excitation line, features coming from the substrate (such as the broad spectrum shown in fig 1) can be observed in the LTPL spectra recorded from epilayers as thick as 20 microns when their net doping concentration is very low (see Fig.2). To illustrate this behaviorepilayers with original thickness of about 35 microns were polished with an small angle which allowed to have a variable thickness from 0 to 35 microns.

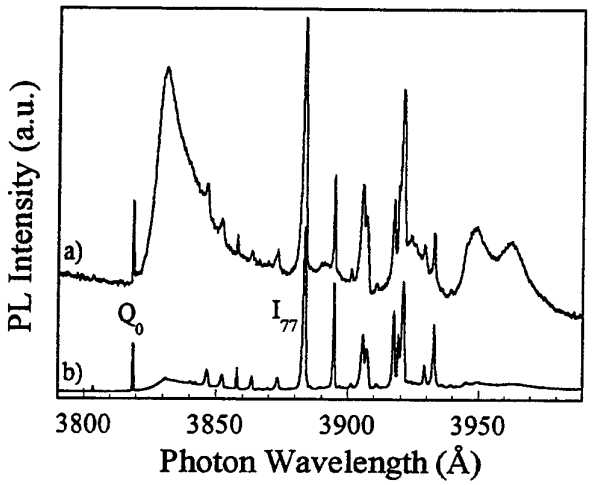

Fig.2 : Low temperature (2K) spectra of 22 µm thick n-type low-doped 4H epilayer and recorded with excitation source the 351 nm line a) and the 244 nm line, respectively.

Finally, the temperature dependence of the near band gap emission for high quality 4H epilayer, has been investigated from 2K to room-temperature (see Fig.3). When the temperature is increased additional N-BE lines are observed due to the structure of the valence band as well as an increasing of the width of the free-exciton (FE) lines: These lines are still visible at room-temperature which has implications on carrier recombinations. A reduction of the total intensity is also observed. Again the choice of the excitation line and of the sample under study is important to be able to record correctly the PL spectra, without additional feature than the near-band gap, as for example donor-acceptor pair from substrate.

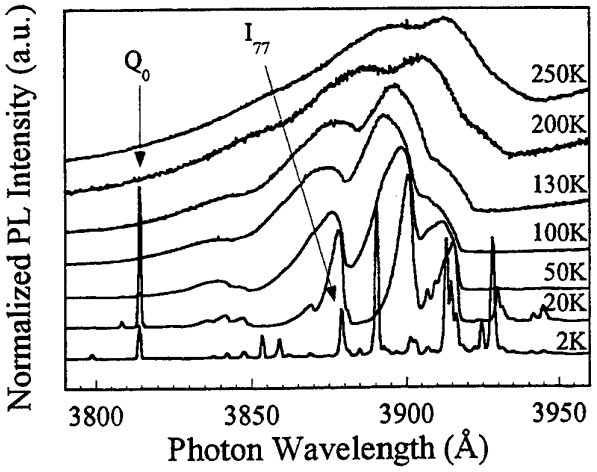

Fig.3 : PL spectra recorded at various temperatures in the near band gap emission of high quality 4H-SiC.

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TWO-PHOTON SPECTROSCOPY OF 6H SiC SINGLE CRYSTAL

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Two-photon absorption was investigated on an instrument in which a 12-nsec pulse I_L from neodymium laser (Nd: YAG) and a 1.5-μsec probe light pulse I_P from xenon flash lamp were simultaneously passed opposite to one another through a SiC sample. A modulation signal ΔI in the form of a "trough" , caused by an increase in the total absorption due to two-photon transitions appeared on the probe pulse. The probe light I passed through monochoromater into a photomultiplier. The laser pulse I_L was monitored with a photocell. The signals from the multiplier and photocell were fed through a delay line into a special three-channels gated detector combined with a pulse analogue computer. During each cycle (the frequency of measuring cycle was 12.5 Hz) the detector measured the amplitude of the laser pulse I_L and the lamp pulse I_P (the gate width was 4.5 nsec). The probe pulse I_P was gated twice, immediately prior to the trough I_P and under the though $I_P - \Delta I$. These signals I_L , I_P and $I_P - \Delta I$ were expanded stroboscopically in time up to 7 msec and fed into computer, where the two-photon absorption coefficient was determined according to the formula

$$\beta = \Delta I / d,$$

where d is the length of the beam interaction region in the crystal. The values obtained for ß were then averaged over 5000 - 20000 pulses. The sensitivity of this arrangement was $\sim 2 \cdot 10^{-7}$cm/Mw. The 6H SiC single crystal grown by modified sublimation method was oriented along the principal axes and the corresponding dimensions were 5x5x5 mm. When the linear-polarisation vectors of the laser beam and the lamp beam are parallel to one another and to the axis of the crystal the two-photon absorption spectrum starts near 3.2 eV. In the energy range 3.8-4.04 eV two peaks are observed. The highest values of ß reached $\sim 1.8 \cdot 10^{-4}$ cm/Mw at the energy $hw_L + hw_P = 4.035$ eV. A similar picture is observed when $e_L \| e_P \perp c$. In this case not two but three peaks located at ~3725 eV, 3805eV and 3905 eV are observed and ß reach $\sim 2.6 \cdot 10^{-4}$ cm/MW at the 3.905 eV. The observed anisotropy of the two-photon absorption is discussed taking into account the specific energy band structure of SiC crystal.

INVESTIGATION OF SURFACE RECOMBINATION AND CARRIER LIFETIME IN 4H/6H-*SiC*

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Appliance of thin *SiC* epilayers in electronic designs generally implies that both surface and interface properties may considerably affect the overall device characteristics. Hence, direct evaluation of carrier leakage at the differently processed surfaces constitutes an important issue for practical applications.

In this work excess carrier transport in 4H and 6H-SiC epilayer-substrate structures is studied applying an optical pump-and-probe free carrier absorption technique. The exercised different optical configurations of the experiment have provided both a general outlook of the statistical lifetime variation over large areas of SiC wafers (*collinear* pump-probe beam geometry) and the explicit picture of in-depth carrier distribution and relaxation (*perpendicular* pump-probe beam geometry) [1].

Carrier recombination in the substrate material was investigated separately. Clearly, two different time components can be distinguished in sub-nanosecond and microsecond range, respectively. The observed surprisingly high lifetimes (up to tens of μs) are attributed to a trap-assisted recombination in substrate.

We found the average carrier lifetime in the epilayer related directly to its thickness, thus pointing out a notable contribution from carrier leakage through the surface and interface. To quantify surface recombination losses as compared to the bulk, a high spatial resolution investigation of the carrier in-depth distribution and relaxation has been accomplished. 40 μm-thick epilayers with as-grown, mechanically polished and top-oxide passivated surfaces were examined. The revealed carrier lifetime variations across the epitaxial layers are discussed in terms of crystalline quality and surface treatment properties.

We also present direct experimental evidence of the excess carrier behavior at the epilayer-substrate interface, i.e. in the vicinity of the n^-n+ (6H-SiC) and n^-p+ (4H-SiC) junctions, respectively. Figure 1 illustrates typical excess carrier dynamics in the 4H-SiC structure,

constituted by the *n*-type epilayer and *p*-type substrate. Note a characteristic carrier concentration pit at the interface, which appears as a consequence of electron-hole charge separation and subsequent fast recombination in the space charge region of a *pn* junction.

Furthermore, depth-resolved measurements have revealed a carrier density-dependent surface recombination in samples with top oxide layers. In some cases, a restrained carrier diffusivity was observed in the adjacent to surface and interface regions, presumably originated by local structural imperfections. Surface recombination velocities in epilayers with differently processed surfaces were extracted by fitting experimental distributions with those simulated numerically. Surface treatment is found to be a substantial factor in limiting the effective carrier lifetime in epilayers. Typically, the as-grown bare surface of both 4H and 6H-SiC epilayers is characterized by a 10^4 cm/s surface recombination velocity. No clear passivation effect of the 6H-SiC surface by oxide film was observed, whereas an unexpectedly high surface recombination velocity up to 10^5 cm/s has been detected after dry oxidation in 4H-SiC. Further studies of surface passivation applying different oxide deposition methods are underway.

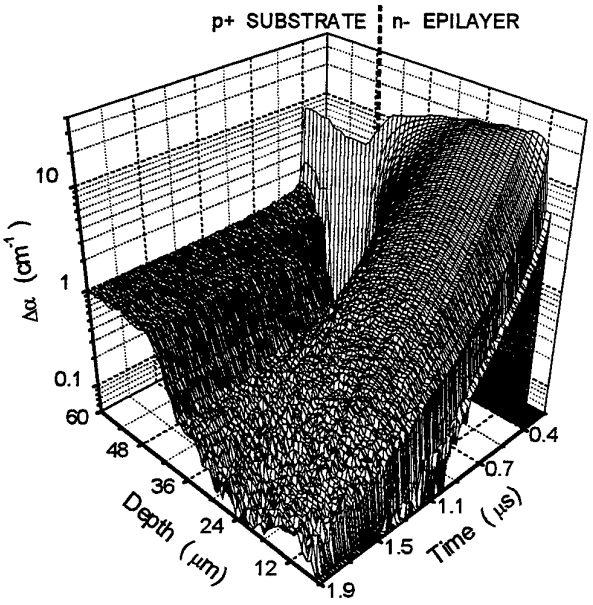

Fig. 1. *3D* layout of carrier temporal and spatial distribution in 4H-SiC epilayer-substrate structure with top oxide layer. The peak value of photoinduced absorption in the plot corresponds to 5×10^{17} cm^{-3} excess carrier density.

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MONOVACANCIES IN 3C AND 4H SiC

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We present results of *first–principles* calculations of the atomic and the electronic structure of neutral and charged C and Si monovacancies in 3C and 4H SiC. It turns out that the qualitative results are mostly identical for 3C and 4H SiC. Even the quantitative differences between 4H and 3C SiC remain often small. This holds especially for the formation energies. It is no surprising result considering the small binding energy differences between the different poltypes. Even the electronic structures are not too different taking into account the differences in the bulk fundamental gaps of 3C and 4H SiC. For that reason, we mainly discuss the physics of monovacancies in SiC in the case of the 3C polytype. A discussion of the differences between the 3C and 4H polytype and the inequivalent sites in 4H SiC is given where necessary. The results are compared with experimental data.

The general findings are that at realistic preparation conditions the formation energies of C vacancies are smaller than the formation energies of Si vacancies. This is reasonable considering the chemical trend for the formation energies in elemental group–IV semiconductors being aware of the fact that the surroundings of a C (Si) vacancy in SiC is similar to that of a vacancy in pure Si (diamond) apart from a difference in the lattice constant of SiC compared to Si (diamond). Therefore, we find a lot of similarities between the behaviour of C (Si) vacancies in SiC and vacancies in pure Si (diamond) which have been studied as well. This holds especially for the structural but to a certain extent also for the electronic properties. A certain puzzle is the determination of the correct ground states. Except for the 2+ charge states the creation of a vacancy in 3C SiC implies a degenerate ground state if the T_d symmetry of the ideal lattice is kept. The degeneracy results from a partial occupation of a threefold (including the spin even sixfold) degenerate t_2 defect state. Therefore, all vacancies in group–IV semiconductors crystallizing in the zinc–blende (or diamond) structure exhibit a Jahn–Teller instability. In the case of 4H SiC the symmetry is already lowered to C_{3v}. However, a twofold (including spin fourfold) degenerate state remains. Therefore, at least for the case of negatively charged defects a Jahn–Teller instability has to be expected even for 4H SiC (and also for any other hexagonal or rhombohedral polytype). The degeneracy can be lifted either by symmetry breaking structural

distortions or (for certain charge states) by electronic symmetry breakings, e.g., via spin alignment (spin dependent exchange–correlation interactions) or maybe even by spin–orbit coupling effects. We are not able to include spin–orbit coupling into our calculations, but we discuss in detail the energetically most important structural symmetry breaking and spin polarization effects.

Like vacancies in elemental Si the C vacancy in SiC exhibits a considerable structural Jahn–Teller effect resulting in a symmetry breaking to D_{2d} symmetry. A significant energy gain is achieved by formation of new (weak) bonds out of the dangling bonds left back at the Si atoms neighbouring the vacancy, i.e., Si dimers are formed. Whereas this pairing mechanism is the main driving force for a symmetry reduction lifting the degeneracy of the ground state the situation is quite different for the case of Si vacancies in SiC (and vacancies in diamond). Here the corresponding energy gain is extremely small due to the too weak overlap of the dangling bonds at the C atoms neighbouring the vacancy. Therefore, there is only a weak structural symmetry breaking towards D_{2d} symmetry approaching the accuracy of our calculations. Since the potential formation of Si pairs by forming new bonds is in general an efficient mechanism for reducing the total energy, it is no surprise that a considerable pairing of Si atoms neighbouring a C vacancy is also found for 4H SiC. This holds even for those charge states which should not exhibit any Jahn–Teller instability according to the lower initial symmetry.

For Si vacancies in SiC a symmetry breaking due to spin–dependent exchange interactions (lifting at least the spin degeneracies) leads to much larger energy gains than any structural symmetry breakings, i.e., whereas spin effects are less important for the C vacancies in SiC, they are essential for the Si vacancies in SiC (and also for vacancies in diamond). In some cases like the singly negatively charged Si vacancy (S=3/2 ground state) these spin effects lead already to a complete removal of any degeneracy. In those cases where a certain (reduced) degeneracy is left, the symmetry breaking may occur due to weak additional structural symmetry breakings. However, as already stated these structural symmetry breakings are extremely weak since the driving forces are extremely weak. Hence, their accompanying energy gains should be negligible. One might speculate whether level splittings due to spin–orbit coupling effects might not result in much larger energy gains.

Similar to the case of vacancies in pure Si, C vacancies in 3C SiC seem to exhibit a negative–U behaviour. The only difference, compared to vacancies in pure Si, is that the absolute value of U is significantly smaller in SiC. This is traced back to the smaller energy gains resulting from the atomic relaxations which are finally responsible for the occurrence of a negative–U behaviour. The smaller energy gain can be explained by the fact that the SiC lattice constant is smaller than the Si lattice constant and therefore in SiC the Si-Si distances are already closer to typical Si-Si single bond lengths than in Si. For that reason, already in the unrelaxed configuration there is a considerable (bonding) interaction between Si atoms neighbouring the vacancy. Hence, the energy of the unrelaxed geometry is already much closer to that of the relaxed configuration.

According to the vacancy levels derived from total energy differences for the different charge states of the vacancies, one finds that C vacancies act as (double) donors whereas Si vacancies act as acceptors, i.e., there is a clear energetical preference for positive (negative) charge states in the case of C (Si) vacancies in SiC in undoped or weakly doped material. Hence, both types of vacancies represent "intrinsic dopants" limiting the doping efficiency in SiC.

ELECTRICAL AND OPTICAL CHARACTERISATION OF VANADIUM IN 4H AND 6H-SIC

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Vanadium (V) is an often-encountered residual impurity in bulk grown SiC materials and recently V doping has been employed to obtain semi-insulating SiC wafers for high frequency devices. It is known that vanadium acts as an amphoteric impurity causing both deep donor states ($V^{4+}(3d^1)/V^{5+}(3d^0)$) and deep acceptor states ($V^{4+}(3d^1)/V^{3+}(3d^2)$). $V^{4+}(3d^1)$ charge state of vanadium has been intensively studied by optical characterisation techniques but few is known about the $V^{3+}(3d^2)$ charge state.

Non intentionally vanadium doped 4H and 6H n type SiC grown by the Lely modified method have been investigated by electrical and optical measurements.

Deep Level Transient Spectroscopy measurement on 6H-SiC reveal two levels which can be related to the vanadium acceptor state (V^{3+}/V^{4+}) in cubic sites and hexagonal site at respectively Ec - 0.68 eV and Ec - 0.74 eV. On the other hand, one level is detected in 4H-SiC at Ec - 0.85 eV and can be related also to the V^{3+}/V^{4+} acceptor state.

Optical absorption measurement on 6H SiC reveal classical absorption spectrum of $V^{4+}(3d^1)$ and additional lines between 4500 cm^{-1} and 5000 cm^{-1}. On n-type 4H-SiC, absorption results show a line at about 5400 cm^{-1} and other structured bands at higher wave number. For 4H-SiC, a line at 5500 cm^{-1} has been detected for the first time by photoluminescence measurements. We tentatively attribute these lines to the internal transitions of $V^{3+}(3d^2)$ charge state of vanadium.

For the first time, we report Deep Level Optical Spectroscopy (DLOS) measurements on these deep levels. This technique allows us to measure unambiguously the photoionisation cross section $\sigma_n^0(h\nu)$ of a level detected by DLTS in a wide range of energy. Spectra of the optical ionisation cross section of a transition metal (TM) can then be interpreted as transition towards the different minima of the conduction band and towards the TM excited states which can be near or resonant with the conduction band.

The optical ionisation cross sections of the levels detected by DLTS are well correlated with the shape of absorption spectra measured on the same materials. Owing to the internal transitions detected in the DLOS spectra, we confirm unambiguously the presence of the acceptor level (V^{3+}/V^{4+}) at Ec - 0.68 eV and Ec - 0.74 eV for the cubic and hexagonal sites respectively in 6H-SiC and at Ec - 0.85 eV in 4H-SiC. In this last case, the energy separation between cubic and hexagonal sites is certainly too small to be detected by DLTS.

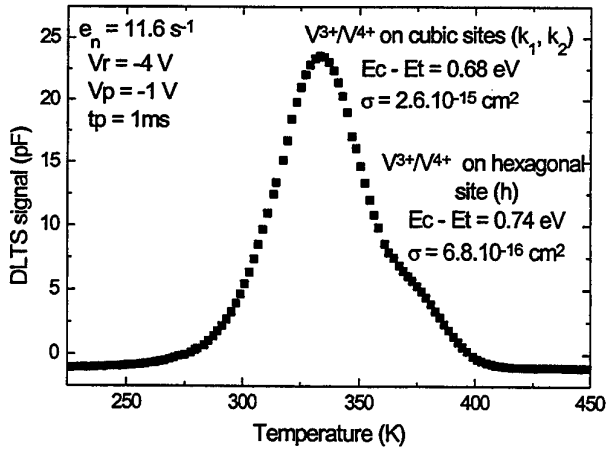

fig. 1 : DLTS spectrum on non intentionally V doped 6H n type SiC consisting of two overlapping V-related levels located at Ec - 0.68 eV for cubic sites and at Ec - 0.74 eV for hexagonal site. The concentration ratio is about 2 : 1.

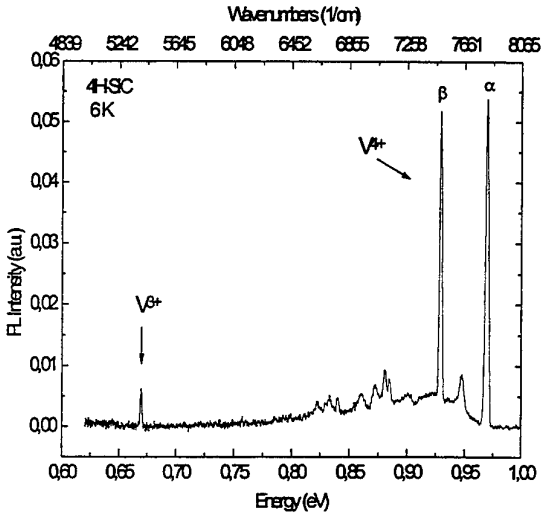

fig. 2 : Low temperature photoluminescence spectrum of vanadium in 4H-SiC exhibiting characteristic luminescence from intra-3d-shell transitions $^2T_2 \rightarrow {}^2E$ of $V^{4+}(3d^1)$ and a new line at about 5400 cm^{-1} attributed to V^{3+} internal transitions.

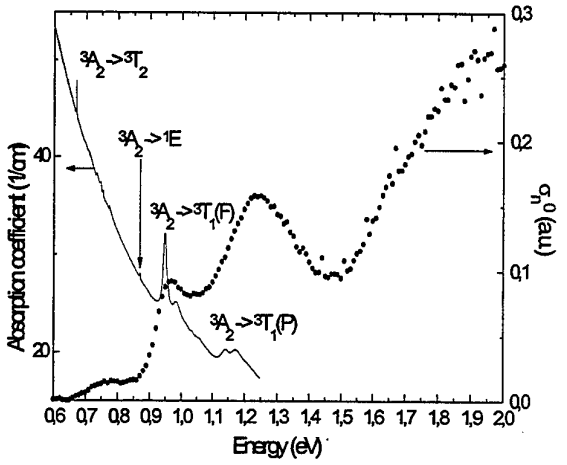

fig. 3 : Comparison of DLOS spectrum (300 K) and optical absorption spectrum (6 K) measured on the same n type 4H-SiC. Spectra show correlation between absorption lines attributed to V^{3+} internal transitions and resonance band of optical ionisation cross section We try to label absorption lines in term of transitions between ground and excited states of V^{3+}.

ELECTRON PARAMAGNETIC RESONANCE OF THE SCANDIUM ACCEPTOR IN 6H SILICON CARBIDE

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It is known that transition metal ions play an important role in silicon carbide as they do in silicon. Recently a great deal of attention was paid to Sc which is expected to act as an acceptor in SiC [1-7]. 6H-SiC doped with Sc was first investigated with luminescence. It has a luminescence band with an onset at about 2.55 eV and a maximum at about 2.2 eV [1-4]. With optically detected electron paramagnetic resonance (ODEPR) [1-4] via the luminescence several EPR lines were observed [1-4]. Three EPR spectra are expected for an impurity in 6H-SiC, due to the three possible inequivalent defect sites in 6H-SiC (two with quasi-cubic symmetry, k_1, k_2, and one with hexagonal symmetry, h). The origin of the observed ODEPR lines was not clear, since no hyperfine (hf) structure was resolved. The angular dependence of the strongest line was explained by Baranov et al. [2] to be due to Sc with $S = 1/2$, $g_{\|} = 1.97$ and $g_{\perp} = 2.49$ observed at $\nu_{ODEPR} \approx 35$ GHz. It was claimed that two additional lines having a similar angular dependence belong to the two remaining sites in 6H-SiC. Lines observed at somewhat higher magnetic fields were attributed to a high spin state of Sc in analogy to V in SiC. It was speculated that the observed high field transitions belong to multiquantum transitions. However, no angular dependence of those transitions was reported [1-3]. Their assignment to Sc could not be proved unambiguously.

Recently, 6H-SiC doped with Sc was re-investigated with luminescence, ODEPR and EPR [4] in order to examine the origin of the luminescence and of the ODEPR lines observed in such samples [1-3]. The main result was the observation of new EPR lines showing well- resolved hf structures. The EPR could unambiguously be assigned to isolated Sc on the three inequivalent sites in 6H-SiC having $S = 1/2$. The analysis of the EPR spectra showed that Sc resides on carbon sites. The assignment was corroborated by ab-initio total energy calculations for Sc on the lattice site for silicon [4,5]. It was concluded, that the previous assignment of the ODEPR spectra [1,2] to the isolated Sc acceptor is doubtful. With ODEPR at $\nu_{ODEPR} \approx 35$ GHz the new EPR spectra were not observed in the luminescence at 2.2 eV [1-4].

Very recently Baranov and Mokhov [6,7] published new EPR measurements on Sc-doped SiC, where EPR transitions explained earlier as being due to forbidden transitions [4] were now assigned to a further new Sc centre. However, only one spectrum for each Sc defect was observed instead of three which are expected for 6H-SiC because of the three inequivalent lattice sites.

So far all magnetic resonance measurements have been made below 35 GHz. In the case of Sc in 6H-SiC März et al. [4] showed, that these frequencies were not sufficiently high to resolve all features of the Sc defect. We therefore performed ODEPR measurements on Sc-doped 6H- and 4H-SiC at 24 GHz and at 72 GHz, which showed even more and new details of the complicated Sc EPR spectra in the luminescence due to the high resolution for g factors at 72 GHz. It will be shown now unambiguously, that the conventional EPR of the isolated Sc acceptors observed previously [4] is connected with the luminescence at 2.2 eV. Further ODEPR signals measured at 24 GHz and 72 GHz also seen in the luminescence at 2.2 eV are also due to the isolated Sc defect. A model of one isolated Sc defect on all inequivalent lattice sites will be proposed which explains all features observed by EPR and ODEPR.

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OPTICAL INVESTIGATION OF RESIDUAL DOPING IN 6H AND 4H-SIC LAYERS GROWN BY CVD

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In order to increase the layer thickness (and then the high voltage capability) more and more homoepitaxial layers of 4H and 6H-SiC are grown at high rate, using a substrate temperature which sometimes exceed 1800°C (see, for instance, Ref.1). Such requirements are not necessary for high frequency applications, and there is still need for epitaxial layers grown at (relatively) low rate (~ 1 μm/hr) with a well controlled level of doping.

In this work we report on the growth of 6H and 4H-SiC epitaxial layers in a home-made " cold wall " AP-CVD (Atmospheric Pressure Chemical Vapor Deposition) reactor, using propane and silane active gas species. All substrates were n-type, <0001>-oriented, 6H and 4H-SiC wafers from Cree Research Inc. with doping level in the range 1.5 - 8 10^{18} cm^{-3}. They were respectively cut 3.5° and 8° off toward the <11$\bar{2}$0> direction. The growth runs were performed in the temperature range 1400 - 1500°C and, within the gas stream, the C/Si ratio was varied from ~ 3 to 10.

We have found the following :

i°) starting from ~ 1430°C, there is always a vary narrow range of C/Si ratio which allows to grow good quality SiC layers. The typical window is between 3 to 5 ;

ii°) depending on either the susceptor is SiC-coated or not, the main residual impurity(ies) is nitrogen or (are) aluminum and nitrogen. This is clear from the consideration of low temperature PL spectra and clearly suggests that, in our case, most of the aluminum contamination comes from the use of uncoated graphite susceptors ;

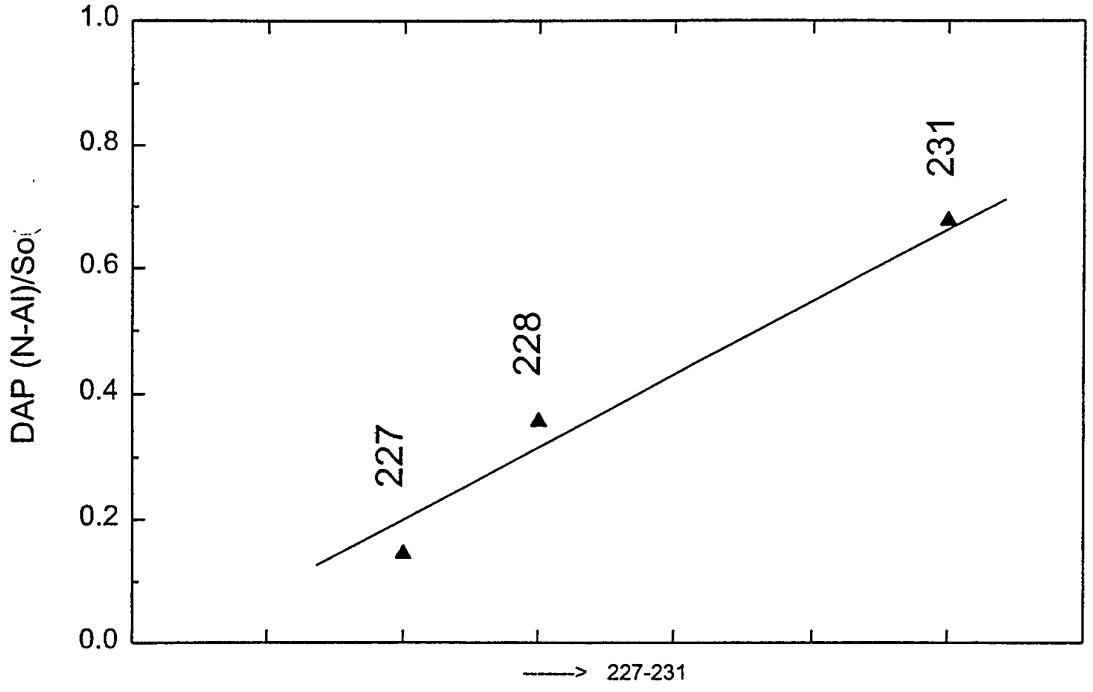
iii°) to further check this point we have considered, in the case of a SiC-coated graphite susceptor, the change in intensity of the Al-related donor-acceptor pair (DAP) as a function of the growth run. We have found that aging the susceptor makes the relative intensity of the DAP more and more intense. This confirms the graphite origin.

iv°) Using uncoated graphite susceptors the residual doping level is p-type, with a residual carrier concentration in the range 7 10^{14} to 2 10^{16} cm^{-3}. By adding nitrogen during the growth run, intentionally compensated layers could be grown. From C(V) measurements performed with a Hg-probe, we have found residual (compensated) carrier concentrations in the range of 3-4.5 10^{16} cm^{-3}. ;

iv°) the growth rate (1 μm/hr) was systematically checked by collecting infrared reflectivity spectra in the 400 - 4000 cm^{-1} range. Indeed, besides the well known SiC restrhalen band, we find in all samples a weak system of interference fringes which resolves in the 1000 - 4000 cm^{-1} range. It comes from the (weak) difference in refractive index which separates the low-doped SiC layers and the highly-doped n-type SiC substrates. ;

v°) using the same growth conditions we could deposit either 6H or 4H, or both polytypes simultaneously (in the same run). In this case the two different layers had similar crystal quality and, from Hg probe, similar carrier concentrations ;

[1] A. Ellison, Invited paper, this conference.



OPTICAL ASSESSMENT OF PURITY IMPROVEMENT EFFECTS IN BULK 6H AND 4H-SIC WAFERS GROWN BY PVT

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Up to now Physical Vapor Transport (PVT) is the only available technique to grow bulk SiC wafers. In the recent years tremendous improvements have been made [1] but, still, a constant requirement for high power switching devices and/or high power high frequency MESFET transistors is the purity of the starting material [2].

In this work, we compare results obtained with two different home-made PVT reactors. The first reactor (reactor 1) has been described at length in Refs [3,4]. It uses a modified-Lely design, with in situ sublimation etching, and crucibles made of standard graphite. Usual crystals exhibit Full Width at Half Maximum (FWHM) for double diffraction X-ray (DDX) rocking curves of (30 +/- 5) arc sec, which agree well with experimental values collected for Lely crystals. However in this case the residual doping level is still high and, from Low Temperature Photoluminescence (LTPL) measurements, no fine structure can be found in the near band edge (NBE) energy range [5].

The second reactor (reactor 2) is described in a companion paper [6]. While basically similar, it uses improved out-gazing procedure and purified graphite for the crucible material [7]. The resulting wafers are 10 mm long with 25 mm diameter. They are grown at a speed of 0.5 mm/hr and exhibit also FWHM for DDX rocking curves of (30 +/- 5) arc sec. The nice point is that, in this case, all LTPL measurements exhibit for 6H and 4H polytypes a very reach fine structure in the NBE energy range which indicates a drastic improvement in residual purity of the material. This is shown in Fig.1-a for a 4H crystal where mainly intrinsic and N-bound exciton lines manifest.

To demonstrate that using purified graphite was the key parameter, we came back to reactor 1 and used purified graphite crucibles. This resulted also in a fine structure (shown in Fig.1-b) while using standard graphite on the reactor 2 the fine structure disappeared. This is shown in Fig.1-c.

Concerning the effect of seed purity we have also found that, in the case of SiC grown using heavily-doped seed material, there is evidence of an in-situ auto-doping phenomenon. This comes for instance when a relatively impure crystal from reactor 1 with typical LTPL signature is used as a seed in reactor 2. In this case, part of the specific DAP spectrum of material 1 migrates and reveals in the LTPL spectrum of material 2. This is clear evidence of in-crucible auto-doping by seed impurities.

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[6] P.Grosse et al., this conf.
[7] Groupe Carbone-Lorraine, Solutions for the Semiconductor Industry.

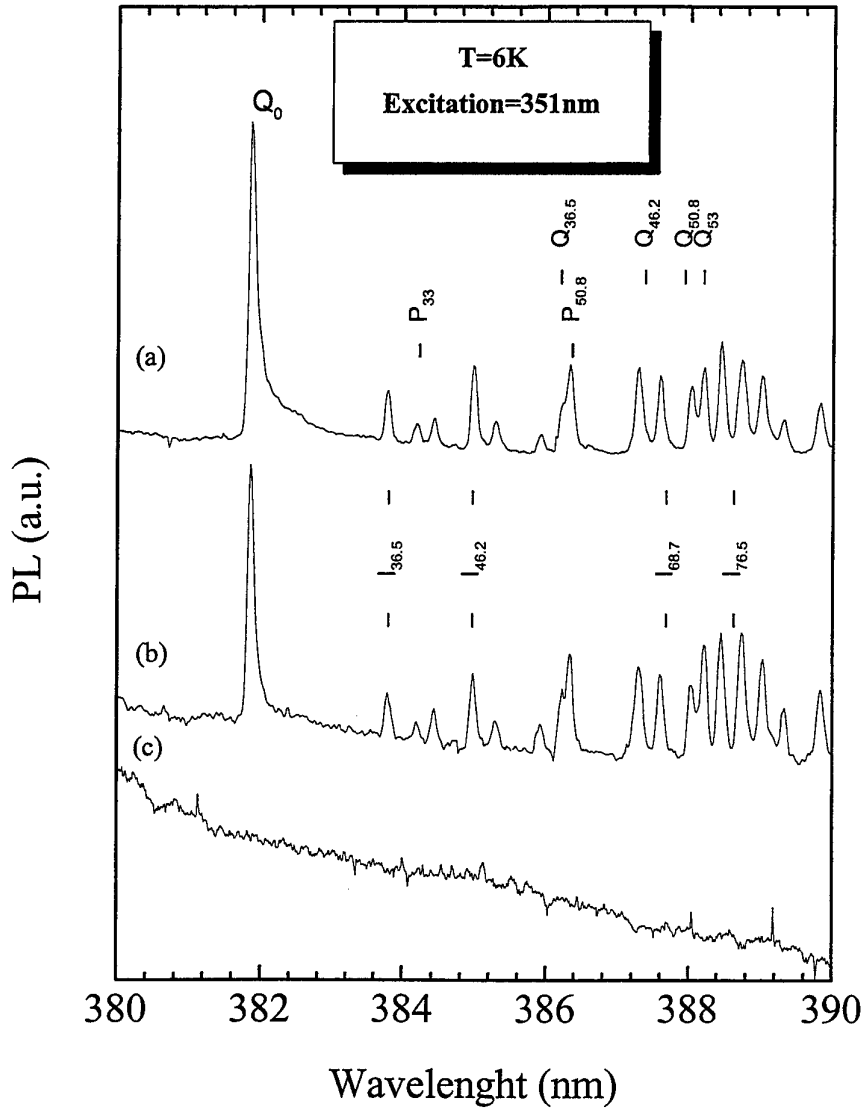

Figure 1: Photoluminescence measurements obtained at 6K on (a) and (b) 4H crystals grown using crucibles made of purified graphite and (c) a crucible made of standart graphite

MONTE CARLO SIMULATION OF THz FREQUENCY POWER GENERATION IN n^+-n-n^+ 4H-SiC STRUCTURES

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A number of theoretical publications show the negative differential velocity (NDV) in n - type 4H-SiC at electric fields over 600 kV/cm due to the conduction band nonparabolicity. The presence of NDV leads to the current instability in n^+-n-n^+ structures. Usually the instability appears at fields considerably over the NDV threshold. In the case of 4H-SiC the high NDV threshold requires a very high electric field for instability to appear. Therefore, the analysis of microwave power generation in n^+-n-n^+ 4H-SiC structures has to account for impact ionization processes and the hole transport as well. This report is the first attempt to investigate theoretically the microwave power generation possibility in 4H-SiC n^+-n-n^+ structures.

Theoretical investigation is performed using Monte Carlo Particle (MCP) technique for solution of coupled Boltzman and Poisson equations for electron and hole transport in 4H-SiC n^+-n-n^+ structures. The band structure for electrons consists of a single equivalent nonparabolic valley. Anisotropy is taken into account. Electron scattering by acoustic phonons, polar optical phonons, zero and first order intervalley phonons and ionized impurities have been included in the model. The band structure for holes consists of a single nonparabolic valley. Hole scattering by acoustic phonons, polar and deformation optical phonons and ionized impurities is taken into consideration. The model also accounts for the impact ionization and Shockley-Hall-Read and Auger recombination. The microwave power generation is investigated directly in MCP simulations by connecting the n^+-n-n^+ structure in the parallel resonant circuit. The standard R = 50 Ω load resistor is used along with an inductor L and a capacitor C.

The simulation shows that at electric fields over 750 kV/cm (the NDV threshold is at about 600 kV/cm) the current oscillations arise in 4H-SiC n^+-n-n^+ structures due to the formation and drift of space charge accumulation layers. As shown in Fig.1 the current is simulated as a function of ramping voltage at 0.1 V/ps for an n^+-n-n^+ structure with 0.5 μm active n-region doped to 1.5×10^{18} cm^{-3}. Fig.2 illustrates the current oscillation at about 0.45 THz. It must be stressed that this is not the Gunn effect where the NDV is caused by the electron transfer into the upper valleys with larger effective masses. The NDV in 4H-SiC is the result of nonparabolicity of the valley. The MCP simulation of the carrier transport in 4H-SiC n^+-n-n^+ structures with parabolic valley shows no instability. The investigation of n^+-n-n^+ microwave device performance in the parallel resonant circuit shows that THz frequency power generation is possible due to the short energy relaxation times in 4H-SiC. The highly doped 4H-SiC n^+-n-n^+ submicron structures can generate tens of milliwatts at frequencies up to 1.5 terahertz. The generation power grows with the voltage

applied to the circuit. The uncontrolled hole multiplication due to the impact ionization sets the upper limit of the voltage. The high microwave power generation is possible at temperatures up to 800 K.

Fig. 1

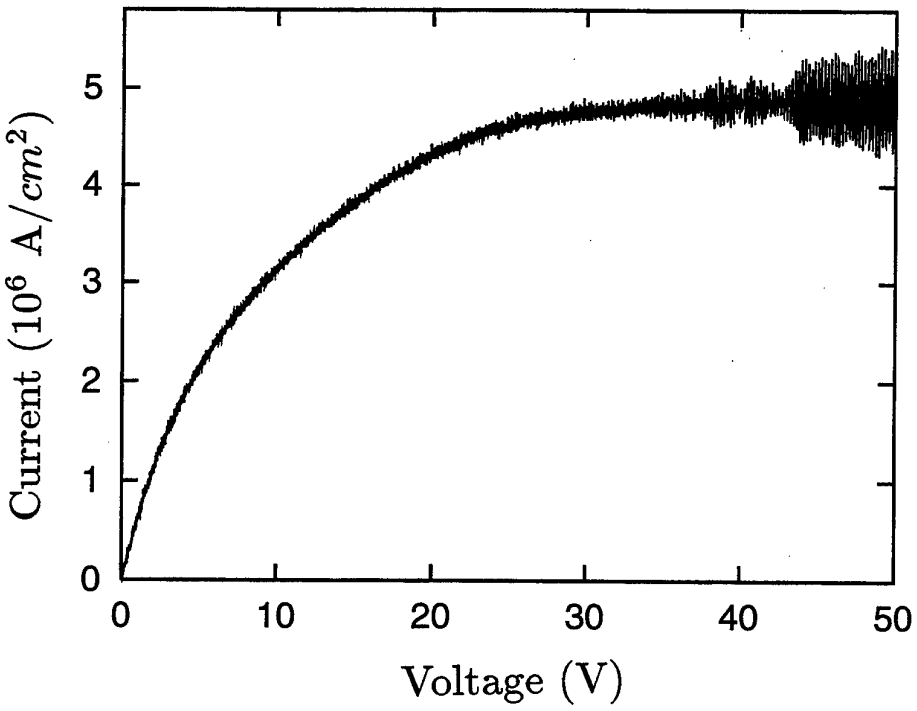
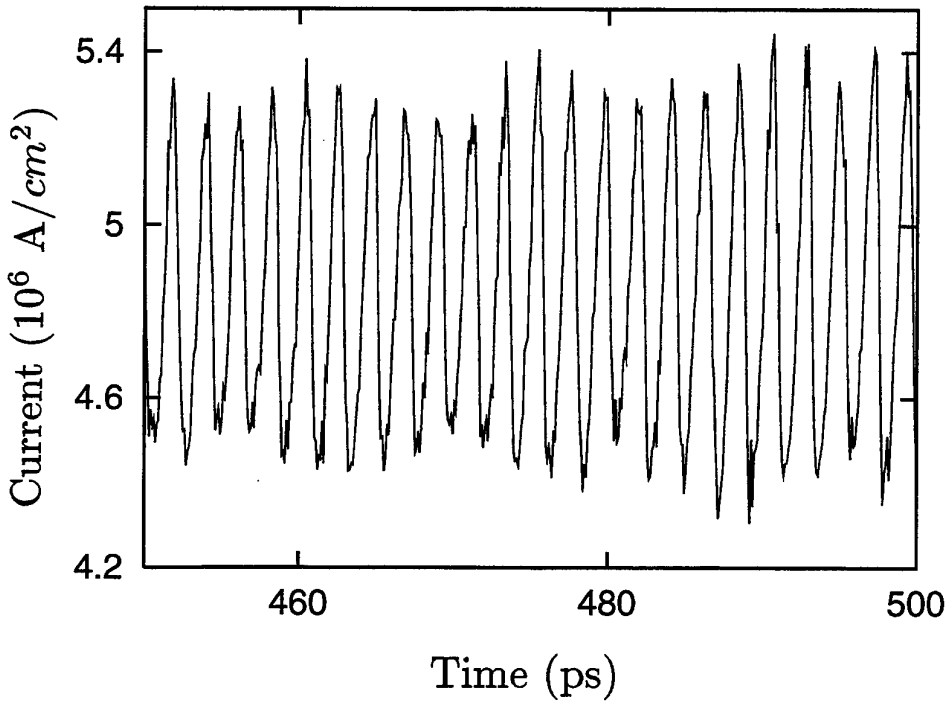


Fig. 2



STUDY OF ELECTRICAL, THERMAL AND CHEMICAL PROPERTIES OF Pd OHMIC CONTACTS TO P-TYPE 4H-SIC AND THEIR DEPENDENCE ON ANNEALING CONDITIONS

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The properties of SiC such as wide band gap, chemical inertness, high thermal conductivity and high electron mobility, make it a desirable semiconductor for high temperature and high power microelectronics. The reliability of devices operated at high temperatures is largely dependent upon the thermal stability of the ohmic contacts. Commonly, thermostable ohmic contacts are annealed at high temperatures. In device technology where lower annealing temperatures are required, the stability of the contact may become a problem. Therefore the production of thermostable ohmic contacts with low contact resistivity that are annealed at low (<750 ^{0}C) temperatures is of prime interest.

In this work we present palladium ohmic contacts to p-type 4H-SiC. The contacts were annealed in the temperature range 600 ÷ 700 ^{0}C. Electrically they were characterised by their I-V characteristics and contact resistivity measured by the TLM method. The as-deposited contacts formed Schottky barriers, while the annealed contacts demonstrated ohmic behaviour. The dependence of the contact resistivity on the annealing conditions have been studied. The contact resistivity values decreased from $3.2\text{x}10^{-4}$ $\Omega.\text{cm}^2$ to $5.5\text{x}10^{-5}$ $\Omega.\text{cm}^2$ as the temperature increased (fig.1).

The thermal stability of the Pd/SiC contacts formed at different temperatures was investigated by two temperature tests (fig.2): an ageing test which was carried out at 500 ^{0}C, and a contact resistivity temperature dependence test performed at elevated temperatures from 25^{0}C to 450 ^{0}C. The results from the ageing test showed that only the contacts annealed at 700 ^{0}C were stable. The resistivity of the contacts annealed at lower temperatures was degraded after 8 hours heating. The results from the temperature dependence test showed that unprotected palladium contacts were stable at operating temperatures up to 350 ^{0}C, while protected ones were stable up to 450 ^{0}C.

Pd/p-SiC contacts annealed at different temperatures were examined by X-ray photoelectron spectroscopy. An as-deposited structure was also analysed for comparison. The element distribution in the structures under consideration and their chemical state in the contact layers have been

determined. The XPS spectra showed that Pd reacts with Si from SiC during annealing. We suggests that palladium silicides are formed and are responsible for the ohmic behaviour.

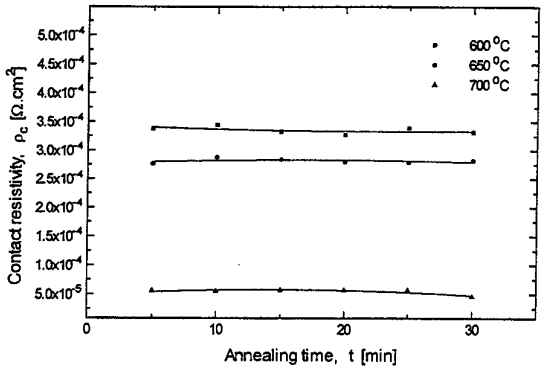

Fig. 1 Dependence of contact resistivity of Pd/SiC contacts on annealing conditions.

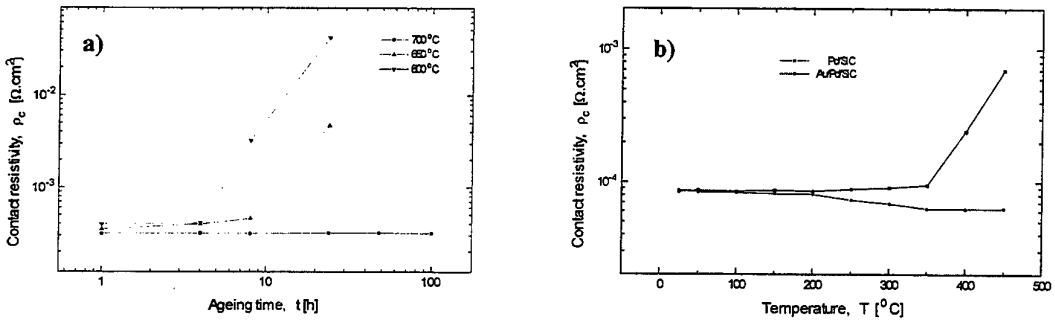

Fig.2 Dependence of contact resistivity of Pd/SiC contacts on ageing time at 500 °C (a) and temperature (b).

Acknowledgements

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SILICON-CONTAINING OHMIC CONTACTS TO P-6H-SIC

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The possibility of ohmic contacts fabrication to p-6H-SiC with the use of silicon-containing systems is considered in this work. About possibility of fabrication of low-resistance ohmic contacts based on Co-Si system to high doped (N_a-N_d=2 10^{19} cm^{-3}) p-6H-SiC have been reported earlier [1]. We made attempt to develop technology of ohmic contact formation to p-6H-SiC epilayers with lower doping level (N_a-N_d= (1-3)x10^{18} cm^{-3}). Epitaxial layers were grown by vacuum sublimation technique. The Ti-Si contact covering as well as the pure metals (Ti, Ni) were tested for the ohmic contact formation.

The components of contact coating were deposited by magnetron sputtering in argon plasma (Ti) or by electron-beam evaporation (Ni, Si). The samples were heated up to 300°C before deposition. Silicon layer of 0.3-0.6 μm was deposited additionally on the 0.1 μm Ti film for formation of Ti-Si-based contact coating. The contact area of required configuration was patterned by photolitography. Then the structures were annealed in a vacuum with using of electron-heating system. The annealing temperature range was 800-1100°C. In the final stage the surface between contact areas was treated with argon or SF_6 plasma to prevent surface leakage at the measuring of specific contact resistance (ρ_c). Value of ρ_c was estimated by transmission line method. Structure and composition of contact coating were examined layer-by-layer analysis and X-ray diffractometry.

It was found that using of pure metals does not allow to obtain ohmic I-V characteristic of contacts. Moreover, Ti and Ni -based contacts demonstrate good quality barrier characteristics after annealing. In contrast, Ti-Si -based contact shows near-linear (at T_a > 1000°C and T_a < 900°C) or linear (at T_a=950°C) I-V characteristics. The specific resistance values of fabricated ohmic contacts were in range (3-10)x10^{-3} Ohm cm^2.

For contacts based on Ti-Si the experimental results obtained by layer depth profile technique show that the components of a contact coating practically do not react with one another or with silicon carbide prior to annealing: there are abrupt boundaries between Si and Ti layers

and silicon carbide. The distribution of elements across the thickness of the contact coating upon annealing shows the presence of several characteristic regions. Near to the surface lies a silicon layer with oxidized upper part. Below is a layer composed mainly of titan and silicon. The type of distribution of these elements and the fine structure of Auger-lines indicate that these elements form titan silicides. The composition of the interface region testifies that no excess carbon is present in this region, i.e., introduction of silicon into the composition of the contact coating does prevent effectively silicon egress from silicon carbide into the contact coating material. It can be noted that under the same conditions, use of pure metals (Ti, Ni) for fabricating the contacts fails to produce of the ohmic I-V characteristic. Therefore, elimination of defects related with silicon loss from SiC favors formation of a nonrectifying contact to p-6H-SiC. An improvement of contact characteristics was also observed [1] in the Si-Co system, provided that carbon inclusions at the contact coating/p-6H-SiC interface were eliminated.

Investigations of the phase composition of the contact coating by X-ray diffraction methods confirm the formation of titan silicides (in form $TiSi_2$ and Ti_5Si_3) in the coating.

The presence in the contact coating of poorly controllable oxygen-containing admixtures presumably accounts for a significant scatter of specific contact resistance values obtained on different samples. Note that the depth to which reactions with silicon carbide in Si-Ti-based contacts extend is preliminarily estimated to be less than 0.1 μm, which is less than the corresponding value, for example, for Ni-based ohmic contacts to n-6H-SiC. Therefore, the condition of the surface may be a critical factor also in fabricating contacts based on the Si-Ti system.

Thus, using of Si in contact coating allows to fabricate ohmic contacts to p-6H-SiC. However, fabricating of good reproductivity contacts is difficult due to poorly controlled factors during formation.

The work was partly supported by Arizona University (USA) and by Schneider Electric (France).

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FABRICATION AND ADVANCED STUDY OF HIGH TEMPERATURE TI-AL-BASED OHMIC CONTACTS TO P-6H-SIC

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Aluminum is introduced usually into the contact coatings for ohmic contacts fabrication to p-6H-SiC [1,2] since it is used as acceptor doping impurity. Recent investigations have shown that Ti-Al composition is one of the most suitable contact coating [2,3]. However, dependence of specific contact resistance on annealing temperature and thermal and current stability of such contacts has been not reported.

The goal of this work was to study electrical characteristics of Ti-Al-based contacts at the high temperatures up to 550°C and high current densities (up to 10 kA/cm^2). The structure and composition of Ti-Al-based contact coating was studied. The dependence of specific resistance value for this contact on annealing temperature in range T_a=800° - 1400°C and on the uncompensated acceptor concentration in p-6H-SiC was examined also.

The ohmic contacts were fabricated both on the CREE Research p-type substrates having doping level N_a-N_d = (2-3)x10^{18} cm^{-3} and on the epitaxial layers grown by liquid-phase epitaxy and by vacuum sublimation. Doping level in epitaxial layers was in range 1x10^{17} - 2x10^{19} cm^{-3}. The films of aluminum and titan were consistently deposited on the p-6H-SiC surface by magnetron sputtering in argon plasma. The required contact area patterns were formed by photolitography. Then the structures were annealed for 2 min in vacuum with using a special electron-gun system. In some cases, the aluminum film was deposited additionally after annealing to decrease the spreading resistance in contact coating. Specific contact resistance (ρ_c) was then measured by transmission line method (in case of epitaxial layers) or by use of two-dimentional model for numerical calculations of semiconductor resistance [4] (in case of substrates). The SiC surface between contact plates was short-time treated with argon plasma to prevent surface leakage.

The following results were obtained at the contact characteristics examination:

- Contacts with non-rectified current-voltage characteristics can be formed after annealing of samples at the temperature range 800° - 1400°C. The minimum value of the specific contact resistance (1-2)x10^{-4} Ohm cm^2 (at the room temperature) was achieved at the N_a-N_d = 1x10^{19} cm^{-3}. There was no dependence of ρ_c value on annealing temperature in the investigated range.
- Examination of structure and composition of contact coating by AES and X-ray phase analysis shows that the components of a contact coating practically do not react with one another or with silicon carbide prior to annealing. The main component of contact coating after annealing was titan carbides. Small amount of aluminum in the annealed contact coating as well as the excess of aluminum (as compared with the bulk of sample) was observed in subsurface SiC layer.

- Obtained data testified that chemical interactions in the contact coating during annealing are not responsible for formation of non-rectifying current-voltage characteristic of Ti-Al-based contact.
- Degradation of structures was not observed at the high environment temperatures (up to 550°C). The heating of samples was performed in air. It was found that ρ_c value was decreased with increase in temperature of structure (Fig.1) so that after 150-200°C it was lower than initial value by nearly an order of magnitude. Specific contact resistance returns back to initial value after cooling for all investigated samples.
- The fabricated contacts were subjected to testing by direct current with density up to 10 kA/cm^2 without degradation in contact resistance value. Good stability of fabricated contacts was observed (Fig.2).
- The specific resistance of Ti-Al-based contacts is decreased from (4-5)x10^{-3} to (1-2)x10^{-4} (at the room temperature) with increasing in p-6H-SiC doping level from 1x10^{17} to 2x10^{19} cm^{-3}. Obtained dependence of ρ_c value on p-6H-SiC doping level is in a good agreement with results reported by Crofton et.al in Ref.3.

This work was partly supported by Schnider Electric (France) and by Arizona University (USA).

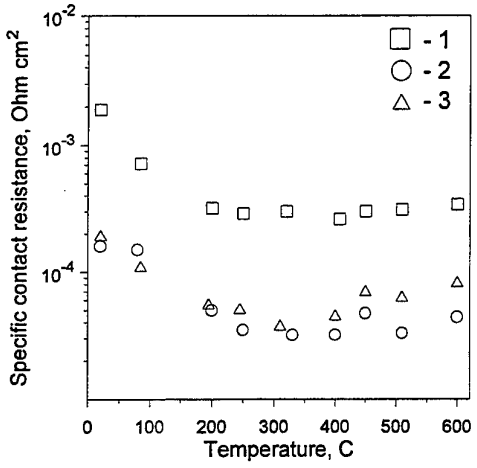

Fig.1.
Dependence of specific resistance on environment temperature for Ti-Al-based contacts fabricated on: 1 - CREE Research substrate with N_a-N_d = 2.7x10^{18} cm^{-3}, T_a=800°C; 2 - sublimation epilayer with N_a-N_d = 1x10^{19} cm^{-3}; T_a=1400°C; 3 - liquid-phase epilayer with N_a-N_d = 1x10^{19} cm^{-3}, T_a = 1400°C.

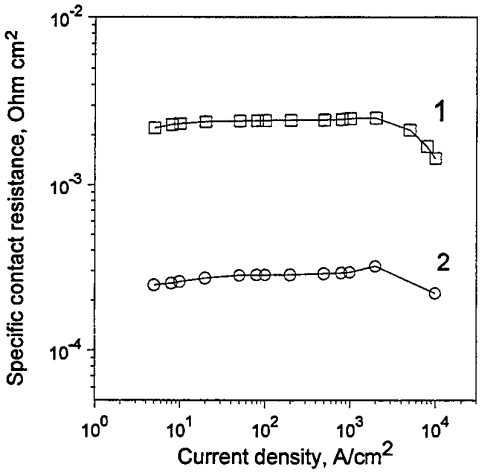

Fig.2.
Dependence of specific contact resistance on current density for Ti-Al-based ohmic contacts fabricated on: 1 - CREE substrate (N_a-N_d = 2.7x10^{18} cm^{-3}, T_a = 800°C); 2 - liquid-phase epilayer (N_a-N_d = 1x10^{19} cm^{-3}, T_a = 1400°C).

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THE INFLUENCE OF N-6H-SIC SURFACE ORIENTATION ON THE CHARACTERISTICS OF NI-BASED OHMIC CONTACTS

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Low-resistance termostable ohmic contacts based on nickel can be prepeared on n-6H-SiC [1,2]. Besides, such contacts have some another advantages [2]. Therefore Ni-based ohmic contact is one of the most suitable for SiC device applications.

In this work we report a new results connected with correlation between specific contact resistance value and contact coating composition near the Ni_2Si/SiC interface. The study of this correlation was carried out on the 6H-SiC polar faces at the various annealing temperatures. The dependence of specific contact resistance on uncompensated donor concentration (N_d-N_a) was studied also. Fabricated structures were tested at the heating up to 550°C and current density up to 10 kA/cm^2.

Ohmic contacts were prepared both on the Si and C-faces of 6H-SiC Lely substrates with N_d-N_a = (3-5)x10^{18} cm^{-3} as well as on the epitaxial layers with (0001) surface orientation and N_d-N_a = 3x10^{17} - 1x10^{20} cm^{-3} grown by sublimation epitaxy. The fabrication procedures required for ohmic contact formation have been reported earlier [2,3]. In the present work the annealing temperatures (T_a) ranged from 800° to 1350°C. Specific contact resistance was determined taking into account current spreading effect in semiconductor. This method has been described in [4]. Composition of contact cover was monitored by Auger electron spectroscopy layer-depth profile technique.

The following results will be presented and discussed in this report.

1. It was found that the dependence of specific contact resistance (ρ_c) on annealing temperature has a minimum (fig.1). The optimal temperatures as well as values of specific resistance are differed for contacts fabricated on Si- and C-faces, as can be seen from fig.1.

2. Presence of layer essentially enriched by carbon near the Ni_2Si/SiC interface has been reported earlier. Now we examined the dependence of ratio of intensity of C(KLL) and Si(LMM) Auger peaks at a point corresponding to maximum carbon concentration on annealing temperature for the both 6H-SiC faces (fig.2). It was found that this dependence is correlated well with dependence $\rho_c = \rho_c(T_a)$ for both substrate surface orientations, i.e. ρ_c value is decreased with increase in C(KLL)/Si(LMM) value.

3. Measurements of specific contact resistance show practically constant value of ρ_c up to T_{env}=550°C at the heating of fabricated structures in air. Typical variation in ρ_c was from $9x10^{-5}$ to $1x10^{-4}$ Ohm cm^2 . Nevertheless, the spreading resistance in contact coating was slightly increase starting from T_{env}~300°C. It can testify the starting of oxidation processes in the contact coating.

4. It was found that Ni-based contacts can be operated at the high current densities (no less than 10^4 A/cm^2) without degradation in contact resistance value. Measurements were performed by direct current.

5. It was found that specific contact resistance value was decreased from $3x10^{-4}$ to $(8-9)x10^{-6}$ when doping level was increased from $3x10^{17}$ to $1x10^{20}$ cm^{-3} (data for contacts formed on Si-face at T_a=1000°C).

The work was partly supported by Schneider Electric (France) and by Arizona University (USA).

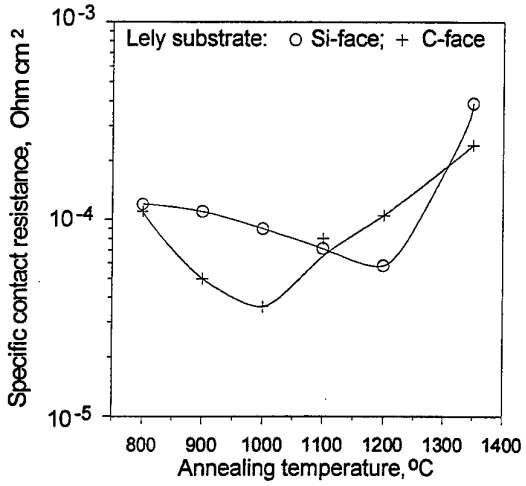

Fig.1.
Specific contact resistance of Ni-based ohmic contacts vs. the annealing temperature for Si- and C-surface orientations.

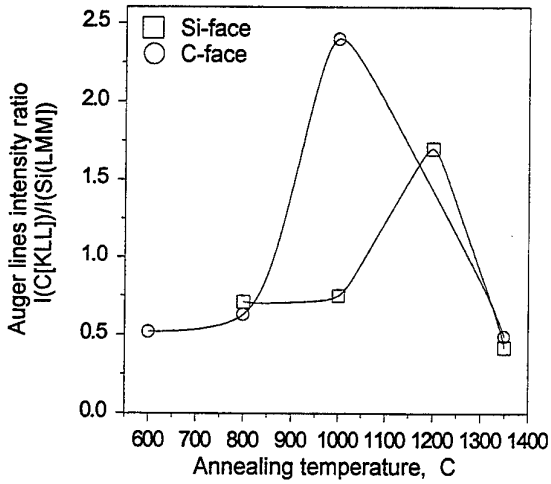

Fig.2.
Intensity ratio of C(KLL) and Si(LMM) Auger peaks vs. annealing temperature at a point of interface corresponding to the maximum carbon content for Ni-based ohmic contacts.

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STUDY OF ANNEALING CONDITIONS ON THE FORMATION OF OHMIC CONTACTS ON P+ 4H-SiC LAYERS GROWN BY CVD AND LPE

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It is difficult to form ohmic contacts to p-type SiC because of its large band gap and work function. Indeed, it is impossible to fabricate an enhanced p-type SiC contact because there is no metal or metal-like material known with a work-function of about 6 eV. Thus, the application of all known metals to p-type SiC will always result in a depleted p-type contact. To obtain an ohmic contact, the barrier should be thin enough to permit tunneling of the carriers. For this purpose very highly doped layers should be used as well as metals which act as dopants for SiC. Thus, aluminum is conventionally used either in pure form or as an alloy (usually Al-Ti). Very low resistance (Å10^{-5} ø.cm^2) ohmic contacts were fabricated [1] by depositing an alloy of Al and Ti. However, high annealing temperatures are required and high vacuum annealing is necessary in this case to avoid oxidation. Other metals have been also used. Thermally stable ohmic contacts have been developed on the basis of Al/Si and Pd metallization schemes[2]. Despite the above promising results, the formation of reproducible thermally stable and low resistivity ohmic contacts on p-type SiC is still an open issue.

In this work, we report on Ti/Al based contacts formed on medium and extremely highly doped 4H-SiC and the annealing conditions were varied significantly. The use of extremely highly doped (>10^{20} cm^{-3}) layers resulted in reproducible ohmic contact (R_c=1x10^{-4} ø.cm^2) and the effect of annealing environment on metallization quality was thoroughly investigated.

The medium doped (Å1x10^{18} cm^{-3}) CVD-grown layers (hereby denoted samples C) were grown on Si-face, 8Æ off 4H-SiC wafers and were commercially purchased. Special care was taken for obtaining wafers with layers from the same batch of epitaxial run. Following, on one wafer an extremely highly doped (>10^{20} cm^{-3}) and thin (Å0.2Ìm) layer (sample C) was deposited by LPE [3] according to a well established procedure[4]. Metal deposition was performed by e-gun evaporation in a vacuum chamber on both medium doped CVD and highly doped LPE grown epilayers. Metallizations consisting of Al/Ti (50nm/100nm) and Al/Ti/Pd/Ni (50nm/100nm/10nm/50nm) were investigated. Circular TLM patterns have been formed by standard photolithography. Annealing of the contacts was performed in three different chambers. One is a conventional RTA chamber where annealing is performed by lamps under flow of forming gas or Ar. One is a quartz chamber pumped down by a rotary pump and the annealing is performed by inductive heating under a flow of H_2. The third chamber is a diffusion-pumped bell-jar vacuum system and the annealing is performed by resistive heating and in an argon ambient at a pressure of 10^{-5} Torr.

Consecutive 3min. annealings from 700 C up to 1300 C in steps of 100 C were performed in high vacuum furnace. The contacts on the highly doped samples exhibited ohmic behavior following the annealing at 1100 C while the contacts on medium doped samples had a clear

rectifying behavior up to 1200 C and only following annealing at 1300 C they exhibited an almost linear I-V characteristic.

The same trend between medium and highly doped samples was observed for the annealing performed in the simple vacuum furnace. In this case, the temperature of annealing was fixed at 1130 C and the duration was varied from 30 sec up to 11min. Figures below show the I-V characteristics.

RTA annealing under Ar or forming gas resulted in all cases in degradation of the metallization. Apparently the extra cap layers of Ni and Pd did not prevent the oxidation of the layers. Therefore, a modification of the RTA chamber has been performed permitting the pumping of the chamber during annealing. The first results following this modification are very promising as degradation of the metallization has not been observed.

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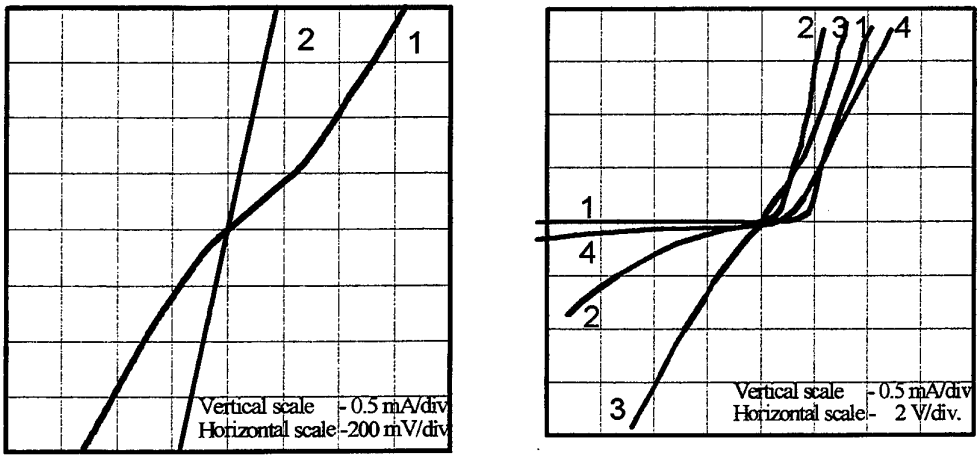

a b

Fig. I-V characteristics of (a) T-sample and (b) C-sample: 1 - as deposited; 2 - anneal for 50 sec at 1130°C in 500 Pa of H_2 at 340 sccm; 3 - anneal for 6 min at 1130°C in 500 Pa of H_2 at 340 sccm; 4 - anneal for 11 min at 1130°C in 500 Pa of H_2 at 340 sccm.

SHALLOW AND DEEP DONORS IN TRANSPORT PROPERTIES OF N-IMPLANTED 6H-SIC

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Due to low diffusion coefficients of the main dopant impurities in 6H-SiC, the ion implantation is the most effective technique to control depth profiles and impurity densities in this material. This is important in the production of reproducible planar devices.

Two different series of samples have been prepared. They correspond to two targeted values around 1×10^{19} to 8×10^{19} cm^{-3} for the first series, and 1×10^{17} to 2×10^{19} cm^{-3} for the second one. For a given series, four different samples were implanted in order to achieve uniform concentration depths of 1000 Å and 2000 Å, respectively.

Transport properties of these N-implanted 6H-SiC samples have been studied between 30 K and 1000 K. Hall effect and mobility have been interpreted in the framework of a two impurity level model. The two activation energies correspond to the hexagonal lattice site (h) and the average of the two cubic lattice sites (k_1,k_2). It has been already shown that the k_1 and k_2 sites cannot be resolved in energy by the Hall analysis [1], and we follow the same approach. We assume that ratio of hexagonal to cubic impurity densities (N_{d1} and N_{d2} respectively) is like 1 to 2. Fitting simultaneously the mobility and the Hall coefficient as a function of temperature [2], we determine N_{d1}, N_{d2}, the corresponding activation energies and the compensation ratio $N_a / (N_{d1}+N_{d2})$. For all studied samples the compensation ratio does not exceed 75 %.

Our results show that the level corresponding to the hexagonal site behaves as an hydrogenic center : its binding energy decreases with the implantation dose. The activation energy of the second one, corresponding to the cubic site, does not vary when the dose increases. This result confirms previous Raman observations [3].

The temperature dependence of mobility is calculated including all scattering processes which are of importance for SiC : deformation potential (acoustic and optic non polar), piezoelectric, polar optical, neutral impurity and ionized impurity modes.

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Electronic structure of the anti-structure pair in 3C-SiC

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We have studied the anti-structure pair (adjacent carbon C_{Si} and silicon antisite Si_C) in 3C-SiC using the plane-wave pseudopotential method, where the exchange-correlation functional is described within the local spin-density (LSD) approximation. We report results regarding formation energies, the ionization levels and the geometry of the relaxed structures of the defect in its all possible charge states. The calculated properties are compared with the pseudopotential results for the isolated antisites C_{Si} and Si_C [1], and it is found that the defect complex exhibits similar behavior. In some extent, the electronic structure of the anti-structure pair is discussed with the former data obtained for the anti-structure pair [2], as well as with some relevant experiments [3].

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PHOTOLUMINESCENCE EXCITATION SPECTRA OF THE FREE EXCITON EMISSION IN 6H-SIC

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The photoluminescence excitation spectroscopy (PLE) is a powerful tool for experimental investigation of the electronic states of impurity atoms or defects in semiconductors. Whereas the usual low-temperature photoluminescence (PL) provides mainly information about the ground states in the bandgap due to the presence of crystal imperfections, the PLE is able to access the excited states, which provides important information about the structure of their electronic levels. The manifold of lines in the conventional PL spectrum can be rather easily sorted out by means of selective PL excitation [1], which greatly simplifies the identification of the lines and their attribution to different defects. Besides, the PLE spectroscopy of the exciton-related emission, when excited with photons with energy close to the bandgap can provide important information about the structure of the valence band or the conduction band near the edge.

This paper presents PLE spectra of the free exciton (FE) emission in 6H-SiC obtained with different polarization of the exciting light with respect to the optical axis of the crystal. We show that the PLE of the FE and the conventional absorption spectra near the bandgap are rather similar. Since 6H-SiC is an indirect bandgap semiconductor, with the valence band maximum at the centre Γ, and the conduction band minimum at a point U between the high symmetry M- and L-points of the Brillouin zone, the direct light absorption into the ground or excited states of the free exciton is forbidden by the momentum conservation law, and only phonon assisted transitions are allowed [2]. Thus, the spectra exhibit a "step-like" structure due to the principal phonons involved in the absorption process in order to conserve the momenta of the excited particles (see [2,3] for the discussion of the absorption spectrum). However, some important differences between the PLE and the absorption spectroscopies if applied for studying the absorption edge are pointed out.

First, the PLE technique does not necessarily require thick samples in the region of very low absorption, that is, near the absorption edge. This makes possible measurements on very thin (tens of microns) epitaxially grown layers of very low doping level and high quality.

Second, and especially near the absorption edge, the signal background in the PLE technique is practically zero, which enables detection of very weak luminescence signals (due to very weak absorption), by using the photon counting technique. Thus, the PLE technique yields high sensitivity and high signal-to-noise ratio in this special region, which is otherwise difficult for the conventional absorption spectroscopy. On the contrary, far from the absorption edge when the absorption is rather considerable, as well as the excited free-exciton luminescence, the absorption spectrum is expected to provide better signal-to-noise ratio. In this sense the two techniques can be considered as complementary to each other.

And finally, the resolution of an absorption spectrum, as well as a PLE spectrum, is determined by how monochromatic the light source is. Since we have used a tuneable dye laser for exciting the PLE spectra, the resolution is of order of 0.1 Å (0.1 meV) in our spectra (see Fig.1).

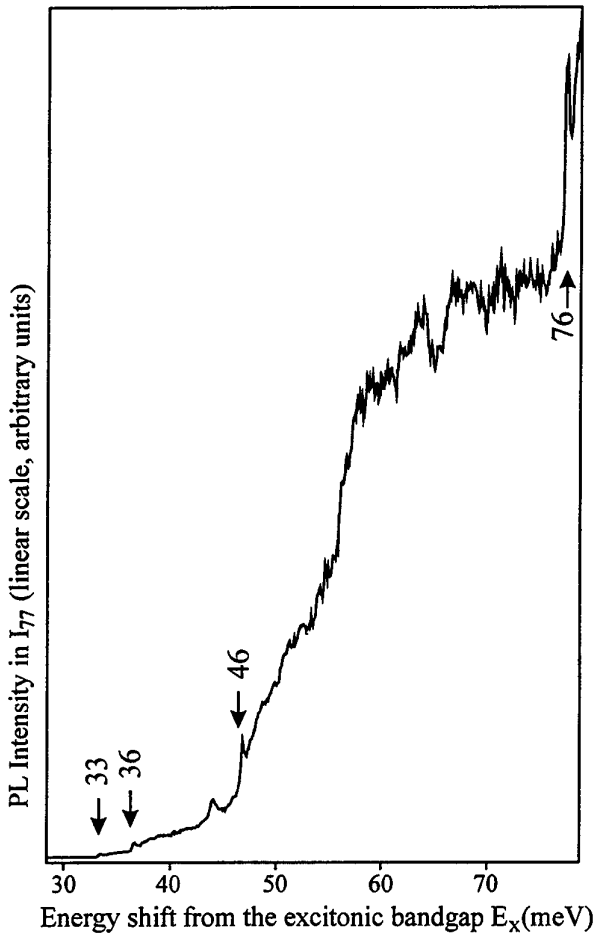

Fig.1 shows the PLE spectrum, obtained by monitoring the 77 meV phonon replica of the free exciton emission excited by a tuneable dye laser. The sharp peaks preceding each step arise from the phonon-assisted absorption. To are knowledge such peaks have not been observed in usual absorption spectra, only the steps are prominent [3]. Peaks are observed by derivative absorption spectroscopy [4], however, they do not look sharp since they are essentially the derivative of the steps. Thus, the resolution, as well as the sample quality becomes a crucial factor in obtaining the correct shape of the internal absorption spectrum. The absorption mechanism will also be discussed in details.

Fig.1. The PLE spectrum of the FE emission in 6H-SiC at 2K. The arrows denote the sharp peaks due to absorption assisted by the principal phonons with energies (in meV) as denoted aside each arrow. The data is not corrected for the change in the intensity of the dye laser.

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POSTER SESSION 2

ALUMINUM NITRIDE LAYERS GROWN on SiC SUBSTRATES by HYDRIDE VAPOR PHASE EPITAXY

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Aluminum nitride layers on silicon carbide substrates are being considered as interesting objects for various electronic applications including MIS structures, UV photodetectors, and substrate materials for III-V nitride epitaxy for high-power devices. Growth of AlN layers on SiC substrates by metal organic chemical vapor deposition (MOCVD) has been reported [1,2]. In this paper, we report on growth of AlN layers by hydride vapor phase epitaxy (HVPE). This method has a high potential for the commercial applications due to low cost and high growth rate. Recently, we reported on the HVPE growth of high quality thin GaN and AlGaN layers on SiC substrates [3,4], and on the fabrication of the first 30 mm diameter GaN bulk wafers using HVPE technique [5].

In this work, AlN layers were grown by HVPE on on-axis 6H-SiC wafers (35 mm in diameter). Layers were deposited on the (0001)Si face of the substrates at atmospheric pressure. The growth temperature was kept between 1000 and 1150°C. AlN growth rate was about 0.3 μm/min. The thickness of the AlN layers ranged from 0.1 to 5 μm. Samples were characterized in terms of surface morphology, crystal structure, composition, and optical properties.

For AlN deposition, the horizontal hot-wall quartz flow reactor was employed. The reactor has two temperature zones. Metallic Al was placed in the source zone of the reactor, where Al reacted with hydrogen chloride to form Al chloride ($AlCl_3$). In the growth zone, Al chloride reacts with ammonia forming AlN layer via the reaction

$$AlCl_3 + NH_3 \rightarrow AlN + 3HCl.$$

X-ray diffraction measurements showed that grown layers have high crystal quality even at rather small thicknesses of AlN layer (<0.5 μm). The minimum value of the full width at a half maximum of □-scan x-ray rocking curve for (0002) reflection was 120 arcsec. This value indicates that the crystal quality of AlN layers grown by HVPE is comparable to that for MOCVD grown materials. Auger electron spectroscopy (AES) detected oxygen and carbon on as-grown surface of AlN layers. After a few seconds of Ar ion beam sputtering, no traces of oxygen or carbon were detected by AES (Fig. 1).

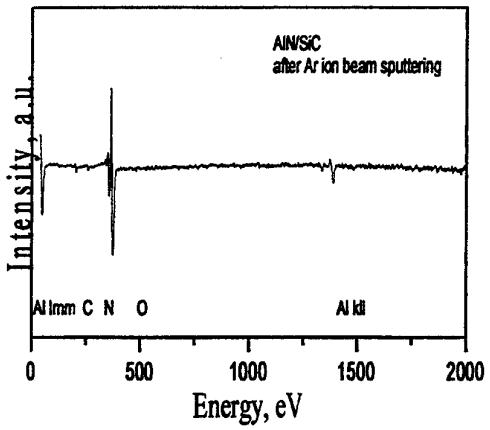

Figure 1. AES spectrum for AlN film grown on SiC by HVPE.

The AlN layers had mirror like surface. Results of surface analysis, which was performed using high-energy electron diffraction and atomic force microscopy, will be presented.

Cathodoluminescence of AlN layers was studied at room temperature. Edge peak at photon energy of 5.9 eV has been detected in the spectrum indicating high quality of the grown material.

Temperature dependencies of specific resistivity of AlN films and dielectric breakdown field were measured in the temperature range from 300 to 700 K. Mesa-structures (200 μm diameter) were formed by reactive ion etching [6] using dichlor-difluoromethane (CCl_2F_2). The evaporated Ni was used as the contact to AlN and as a mask for AlN plasma etching. Ni metallization was also used as a backside contact to silicon carbide substrate. The results of these measurements will be presented.

Presented results on HVPE growth of AlN opened an opportunity to make AlN bulk crystals by HVPE and use HVPE technique for AlN/GaN and AlN/SiC device structure fabrication.

This work was partly supported by the Russian Foundation for Basic Research (Grant N 97-02-18057), INTAS Program (Grants 96-1031 and 96-2131), and the Arizona State University.

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Infrared investigation of $Al_xGa_{1-x}N$ epitaxial layers deposited on 6H-SiC substrates.

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$Al_xGa_{1-x}N$ is well known for applications related with light emission and detection in the ultraviolet range and also with high power, high temperature and high frequency electronic devices. However the knowledge of many basic properties of $Al_xGa_{1-x}N$ is still relatively poor. Particularly little is known about the vibrational properties of this alloy. Most of the existing information are based on Raman experiments, not so easy to interpret specially for crystals with a high aluminum content. In this work we show that the use of 6H-SiC substrates offers a unique possibility of having a simple phonon structure.

Epitaxial layers of $Al_xGa_{1-x}N$ were deposited on 6H-SiC(0001) substrates, at 1050-1150°C and 45Torr in a cold-wall, vertical, RF inductively heated OMVPE system. Triethylgallium (TEG), triethylaluminum (TEA) and ammonia (NH_3) with H_2 diluent were used as source materials. In the case of the sample $Al_{0.12}Ga_{0.88}N$ 800Å thick AlN buffer layer was used.

The infrared reflectivity spectra measured for $Al_xGa_{1-x}N$ layers with composition ranging from pure AlN to $Al_{0.12}Ga_{0.88}N$ deposited on 6H-SiC have been displayed in Fig.1. They clearly show an evidence of two transverse frequencies in the range 500-700 cm^{-1} and one (small) LO frequency around 850 cm^{-1}. They have been noticed A, B and C, respectively.

By fitting the spectra with the help of a transfer matrix method, we obtain all phonon frequencies and oscillator strengths for the AlN-like and GaN-like long wavelength $E_1(TO)$ modes listed in Table 1. The oscillator strengths of AlN-like and GaN-like frequencies in the $Al_xGa_{1-x}N$ alloys scale proportionally to the corresponding Al and Ga mole fractions. This is shown in Fig.2. This clearly establishes the so-called two-mode behavior of the transverse E-like frequencies.

Finally, we find values of 622cm^{-1} for the impurity mode of Ga in AlN and 645cm^{-1} for the impurity mode of Al in GaN.

Table 1.

Sample number	composition [-]	d [μm]	ω_{TO1} [cm^{-1}]	f_1 [cm^{-2}]	γ_1 [cm^{-1}]	ω_{TO2} [cm^{-2}]	f_2 [cm^{-2}]	γ_2 [cm^{-1}]	ω_{FE} cm^{-1}]	Γ_{FE} [cm^{-1}]
1	0	-		1.23E6	-	-	0	-	-	-
2	0.12	0.6	560	1.1E6	5	645	6E4	20	600	500
3	0.39	0.25	585	7E5	25	655	7E5	10	500	500
4	0.68	0.2	605	4.5E5	35	653	1.1E6	35	0	-
5	0.95	0.15	618	5E4	15	665	1.5E6	10	0	-
6	1	0.22	-	0	-	665	1.6E6	5	0	-

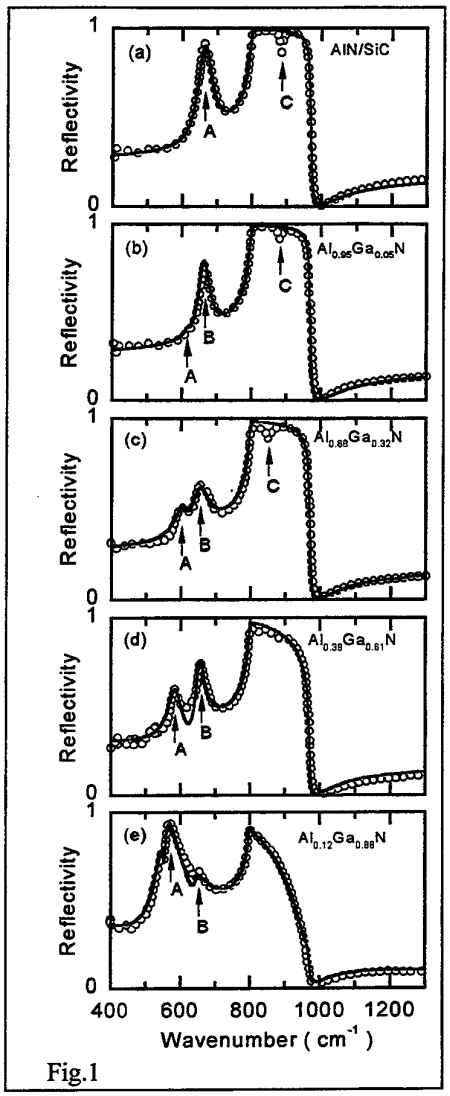
(a)
AlN/SiC
(b)
$Al_{0.95}Ga_{0.05}N$
(c)
$Al_{0.68}Ga_{0.32}N$
(d)
$Al_{0.39}Ga_{0.61}N$
(e)
$Al_{0.12}Ga_{0.88}N$
A
B
C
Reflectivity
0
1
400
600
800
1000
1200
Wavenumber (cm^{-1})

Fig.1

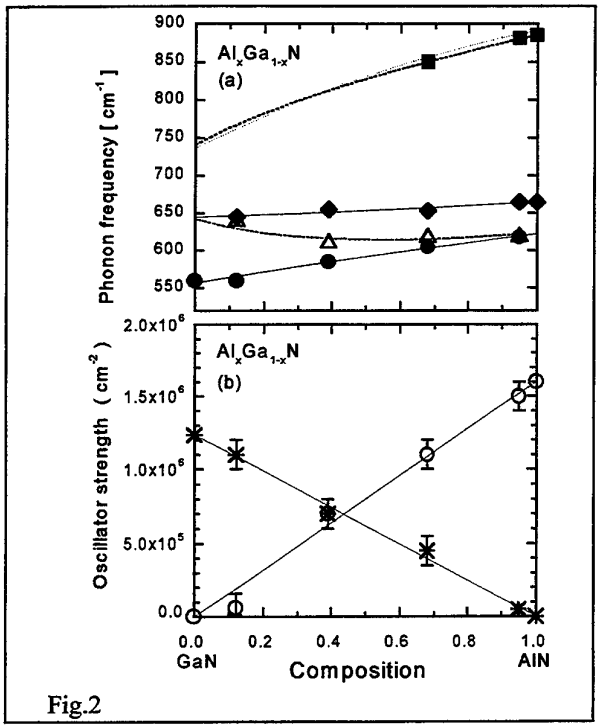
$Al_xGa_{1-x}N$
(a)
Phonon frequency [cm^{-1}]
900
850
800
750
700
650
600
550
$Al_xGa_{1-x}N$
(b)
Oscillator strength (cm^{-2})
$2.0x10^6$
$1.5x10^6$
$1.0x10^6$
$5.0x10^5$
0.0
0.0
0.2
0.4
0.6
0.8
1.0
GaN
Composition
AlN

Fig.2

SIMULATION AND ELECTRICAL CHARACTERIZATION OF GAN/SIC AND ALGAN/SIC HETERODIODES

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Heterojunctions on SiC is an area in rapid development, and several interesting works have been published recently[1, 2]. These are heterojunction bipolar transistors (HBTs) with a GaN emitter on a SiC base and collector, mainly for high frequency applications. In this work numerical device simulation was compared to electrical characterization of processed heterodiodes. Two different approaches of the heterojunction formation were investigated. The first approach used molecular beam epitaxy (MBE) to grow n-type GaN with a polycrystalline GaN buffer for relaxation. The second approach used chemical vapor deposited (CVD) n-type $Al_xGa_{1-x}N$ (x~0.1) with an AlN buffer. Both structures were grown on p-type 6H-SiC. Mesa structures were formed using Cl_2 reactive ion etching of GaN/AlGaN[3], which showed good selectivity on SiC (about 1:6). As cathode metallization sputtered Ti was used with a rapid thermal anneal to establish a good ohmic contact[4]. As backside anode contact to SiC liquid InGa was used. Figure 1 shows the mesa structure of the heterodiodes.

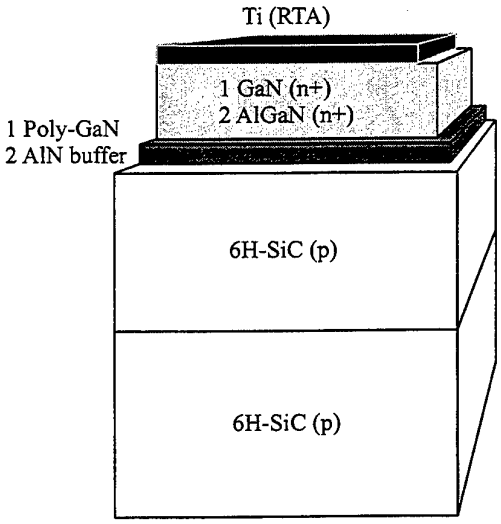

Figure 1. The heterodiode structures have a 0.5 μm GaN or an AlGaN cathode with a 20 nm polycrystalline GaN buffer or a 12 nm AlN buffer respectively. RTA titanium was used as cathode contact, and InGa as anode contact Both GaN and AlGaN have an unintentional n-type doping[5], but since carrier concentration decreases strongly with Al content the AlGaN samples were Si doped to the mid 10^{18} cm^{-3}. Along with the heterodiode structures TLM structures were fabricated for cathode contact characterization.

IV-characterization on the heterodiodes will be presented, in comparison to numerical simulations of the electrical properties of the heterojunctions and buffer layers. TLM structures were used to measure the cathode contact resistance and to give an estimate of the electrical doping of the cathode material (GaN or AlGaN). The measurements were performed up to 300 °C. From simulations it is seen that the IV-characteristics are strongly affected by the choice of buffer layer and band alignment across the heterojunction, see Figure 2.

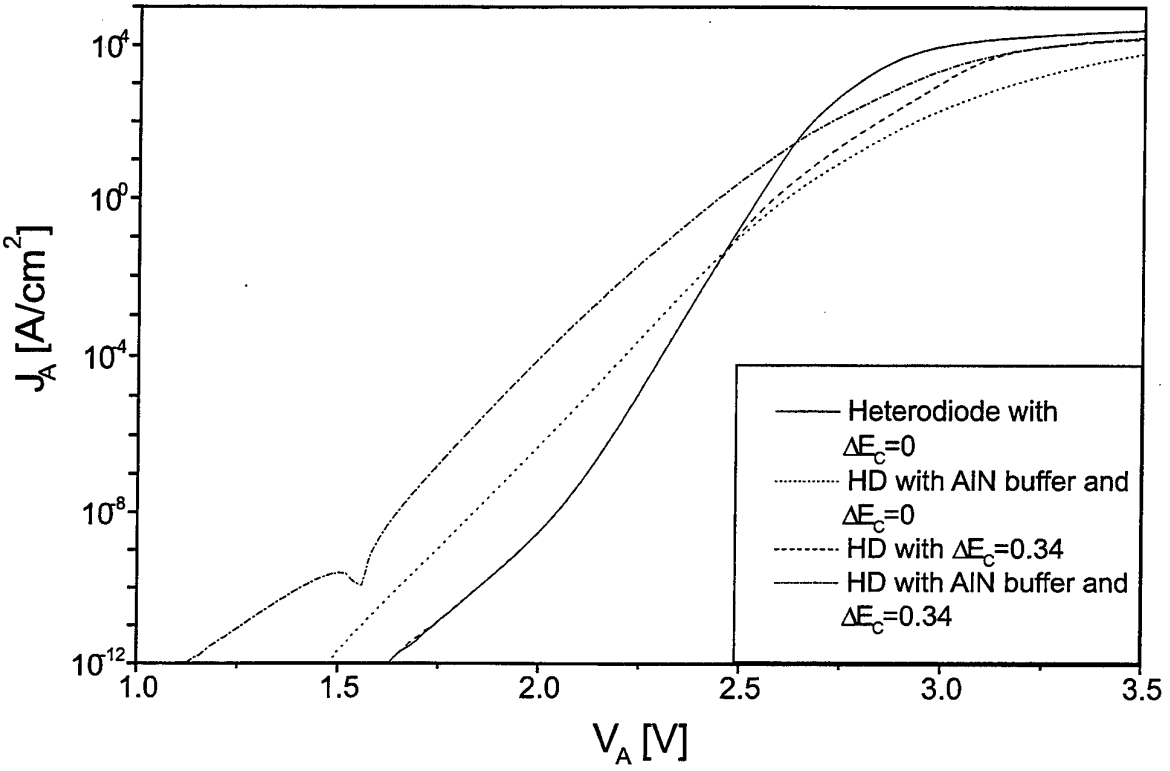

Figure 2. Simulation of the heterodiode with different conduction band discontinuities. The influence of the AlN buffer layer was also simulated.

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DISLOCATION STRUCTURE OF GAN BULK CRYSTALS GROWN ON SIC SUBSTRATES BY HVPE

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Recently we reported on the fabrication of 30 mm diameter GaN wafers [1]. These wafers were fabricated using hydride vapor phase epitaxy (HVPE) of thick GaN layers on 6H-SiC substrates and subsequent removal of the silicon carbide substrate by reactive ion etching [2]. In this paper, structural defects of these GaN crystals were investigated by transmission electron microscopy (TEM).

TEM (cross-section) images taken from the regions near the former GaN/SiC interface clearly shown highly defective initial layer approximately 100nm thick, which is typical for heteroepitaxial growth. Some separated small grains (~12 nm), grown preferentially in the [0001] direction were observed inside this region.

The boundaries between neighboring grains and dislocations lying inside every grain and parallel to the (0001) plane, were observed in plan-view TEM images. These grains were identified with nucleation islands arising during the initial stage of GaN growth on SiC substrate. Dislocations, lying on basal plane, were assumed to be due to relaxation of lattice mismatch between the layer and the substrate.

Three types of dislocations were found at a distance of 5 microns from the former GaN/SiC interface: (1) threading dislocations (TDs) surrounded by powerful stress fields; (2) dislocation half-loops lying on prism planes, and (3) dislocations lying on (0001) basal planes and located near TDs.

At a distance of more than 20 microns away from the former interface, the density of TDs decreased by a factor of 10. Dislocations half-loops lying on prism planes were not detected. We also observed increase in the distance between dislocations lying on (0001) basal planes in the direction from former interface to the surface.

Based on these results, it was assumed that TDs and dislocation half-loops lying on prism planes, were initiated at the interface during the initial stage of the growth as a result of coalescence of GaN islands. During post-growth cooling the stresses, located near TDs, increased considerably due to the addition of thermal stresses. The relaxation of these stresses occurred through the formation of cracks and dislocations lying on (0001) planes.

The influence of initial nucleation stage of heteroepitaxial growth on dislocation distribution in bulk GaN crystals and process of stress relaxation will be discussed.

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ANNEALING AND RECRYSTALLIZATION OF AMORPHOUS SILICON CARBIDE PRODUCED BY ION IMPLANTATION

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Being one of the most promising semiconductor materials for high-temperature, high-frequency and high-power electronic devices, SiC has attracted considerable interest during the last few years.[1,2] In search of a processing technology, practicable for industrial scale SiC-device production it turned out, that conventional diffusion-based techniques fail due to the low atomic mobilities in SiC below 1700°C.[3] However, also ion implantation doping suffers from this problem.[4] For instance, radiation damage in SiC becomes extremly stable and the material is easy to amorphize. This amorphization is accompanied by strong volume swelling.

Unfortunately, there was only limited success in thermal annealing of amorphized SiC, which led to contradictory results in the literature. A temperature of 1450°C[5] was commonly accepted as the threshold temperature for the epitaxial recrystallization of implantation-amorphized SiC, whereas more recent investigations[6,7] have shown, that recrystallization can be achieved already at about 1000°C. On the other hand densification of a-SiC after thermal annealing at 500°C was reported recently.[8] The authors inferred the existance of a relaxed amorphous state from this behaviour.

In order to reveal the reason of this low temperature densification and to elucidate the thermal recrystallization behaviour of amorphized SiC we performed step height measurements and X-ray diffraction after thermal annealing of amorphous SiC layers produced by Si MeV-implantation into 6H-SiC. The shrinking behaviour of the step height shown in Fig. 1 enables to identify two stages of annealing. At temperatures between 250 and 700°C a specific densification of the amorphous layer occurs after the first annealing period of 5 min. The density increase can be described by an Arrhenius law with an activation energy of about 184 meV. Further isothermal annealing up to 10 h leads only to minor density changes. Therefore, it can be concluded that the structure obtained after low temperature annealing is metastable. Both the rapidity and the low activation energy of the densification suggest that defect annealing processes taking place in this temperature range should be responsible for the densification. Furthermore, partial crystallization and changes of the amorphous network structure can be excluded as possible reason for low temperature densification on account of our X-ray diffraction results. Consequently, amorphous states with continuously varying densities can be produced by low temperature annealing of amorphous SiC.

The annealing behaviour at temperatures above 700°C is rather complex. It is characterized by a combination of defect annealing and recrystallization. The analysis of the crystallization kinetics in terms of the Johnson-Mehl-Avrami theory shows that the crystallization mode changes with increasing temperature. The decreasing slope of the transformation curve from about 2.5 at 800°C to about 1 at 1000°C can be interpreted as the transition from nucleated to epitaxial growth. The recrystallization generates stress in the layer which leads to surface cracking if the layer exceeds a critical thickness.

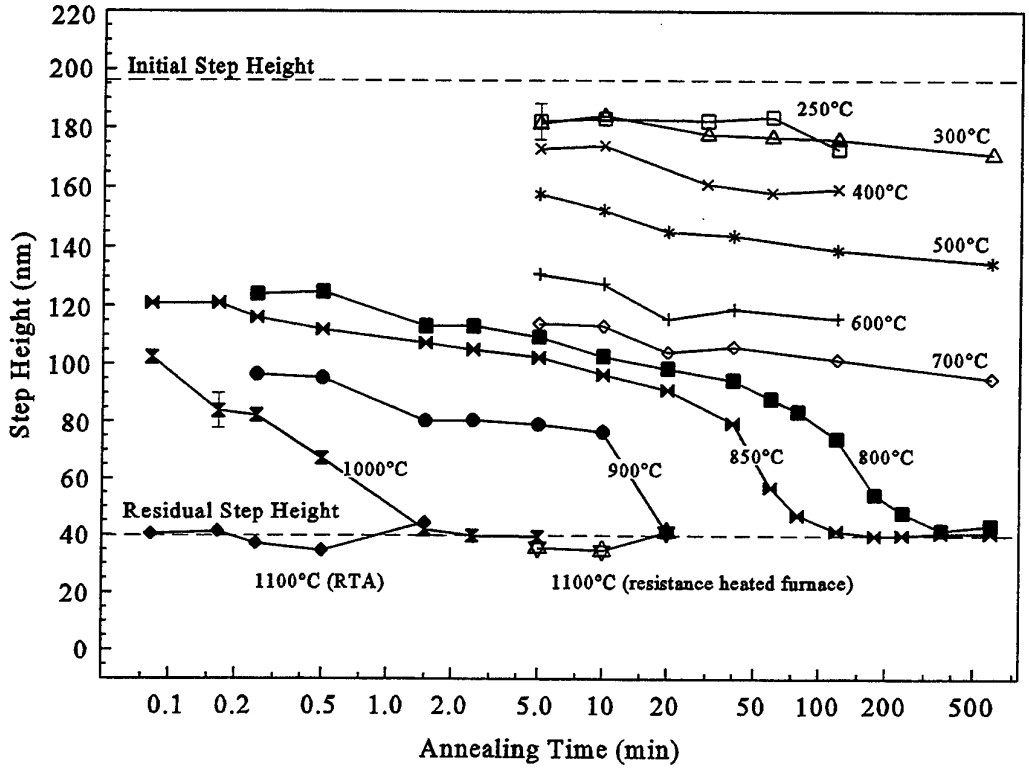

Fig. 1 Step height of the annealed samples as function of the annealing time. Each curve corresponds to a sequence of isothermal annealing steps of one sample. The initial step height after amorphization and the residual step height after recrystallization are marked by dashed lines.

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CRYSTALLIZATION AND SURFACE EROSION OF SIC BY ION IRRADIATION AT ELEVATED TEMPERATURES

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SiC is a wide band-gap semiconductor with excellent properties for applications in the field of high-temperature, high-frequency and high-power electronics. In order to exploit this potential selective doping of SiC substrates is necessary which can be carried out only by ion implantation because of the low dopant diffusivities at temperatures below 1800°C. However, ion implantation into SiC produces severe radiation damage up to amorphicity which has to be annealed in order to receive optimal electrical properties. This was the main driving force for many studies of ion implantation and damage annealing in SiC performed in the previous decade [1].

Because of the serious problems associated with the thermal annealing of amorphous SiC, like imperfect regrowth and/or surface degradation, an alternative process was searched in order to recrystallize SiC. It is known that ion beam irradiation can stimulate epitaxial regrowth in Si as well as in III-V-compound semiconductors at temperatures well below the threshold temperature of thermally induced solid phase epitaxy (SPE). Moreover, ion beam induced epitaxial crystallization (IBIEC) of compound semiconductors often produces better crystal quality than thermal annealing. Therefore the recrystallization behavior of amorphized 6H-SiC layers under ion irradiation at elevated temperatures was investigated in a series of experiments [2-6].

Indeed, recrystallization of amorphous SiC could be obtained during ion irradiation at temperatures as low as 300°C. However, the recrystallization of SiC under ion irradiation is much more complex than known from Si and cannot be described by the simple models developed for IBIEC of Si [7]. Recent unexpected and contradictory results on ion beam induced crystallization made questionable some conclusions drawn in our previous papers [2-6]. In particular, we learned that effects like material swelling, densification [8] and enhanced surface erosion play an important role during ion irradiation of SiC and can lead to misinterpretations of measurement results. Unfortunately, the magnitudes of these effects are not exactly known and, therefore, reliable conclusions have not been possible until now. Two different schemes for the interpretation of our previous results are shown in Fig. 1. The main goal of this paper is to find out which of these interpretations is correct. The effects which can influence the shift of the amorphous/crystalline interface should be determined quantitatively. For this purpose a special experiment was performed. 200 keV Ge^+ implantation at liquid nitrogen temperature was used in order to form an amorphous layer with a sharp interface. The recrystallization process was stimulated by 350 keV $1\times10^{17}cm^{-2}$ Al^+ implantation at 500°C either into the bare sample surface or through a 90 nm thick Si capping layer. The specimens were characterized by RBS/C, cross-section TEM and step height measurements.

As reported recently [6] an improved crystal quality of SiC is apparently achieved by ion irradiation at a temperatures of 1050°C. Unfortunately, the necessary IBIEC dose of $1\times10^{17}cm^{-2}$ is still too high for practical application. Therefore, it will be examined whether complete IBIEC is possible with lower ion doses if the temperature is increased.

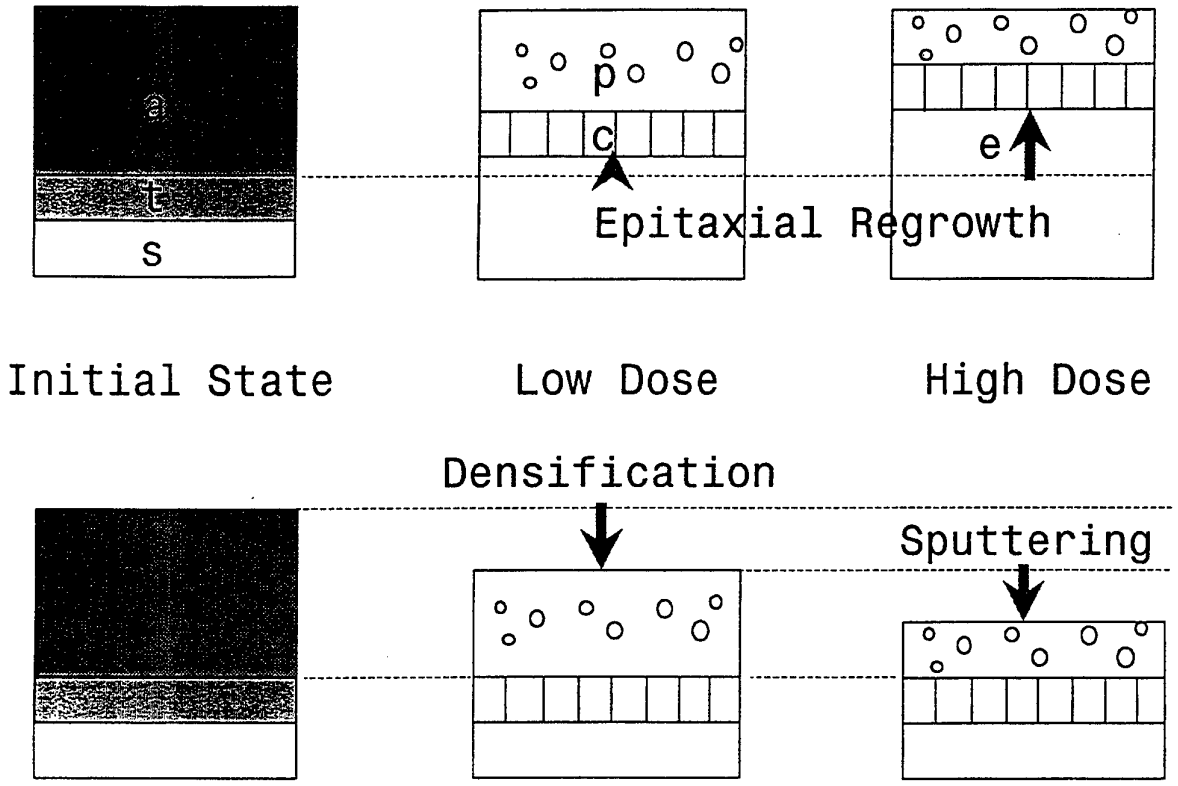

Fig.1: Schematic of cross section views of amorphized SiC layers before and after Si^+ ion irradiation at 480°C [4]. From left to right: As amorphized state with amorphous surface layer (a), broad damaged transition region (t) and single crystalline 6H-SiC substrate (s). After irradiation crystalline layers with columnar (c) and polycrystalline (p) structure are observed. The upper row corresponds to the interpretation in terms of partially epitaxial regrowth (e). The lower row explains the observed interface movement in terms of densification and surface erosion.

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CORRELATION OF ELECTRICAL AND MICROSTRUCTURAL PROPERTIES AFTER HIGH DOSE ALUMINIUM IMPLANTATION INTO 6H-SiC

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One of the problems of ion implantation doping of SiC is the electrical activation of high concentrations of p-type dopands like aluminium. In this paper we report for the first time about a thorough study of high dose Al-implantation into SiC by correlating of microstructural and electrical properties. In this connection, we did also investigate the influence of insitu annealing during ion implantation.

The 6H-n-type epitaxial layers are implanted by multiple energies and doses to form a 500 nm thick homogeneously doped layer. The Al concentration was investigated in the range of 5E19.....5E21 cm^{-3}. The implantation temperature is varied from room temperature up to 1300°C. The annealing is carried out at temperatures between 1500°C and 1750°C in vacuum and Ar ambient, respectively.

The as-implanted samples are characterized regarding the implantation damage and the electrical state. The implantation damage, measured by RBS and RAMAN, decrease with increasing implantation temperature up to 1000°C. Using XTEM the room temperature implanted samples show an amorphized layer with destroyed long range order. For implantation temperatures up to 800°C a defective layer with homogeneous tension contrast is found probably caused by point defects. For higher temperatures dislocation loops are observed. Using Hall effect measurements p-type conductivity is observed only for an implantation temperature above 1200°C.

The annealed state is characterized by Hall effect measurements and XTEM. The amorphized layer of the room temperature implanted sample was recrystallized. Dislocations near the surface and dislocation loops in the deeper regions are observed. The samples implanted at higher temperatures show a lower density of defects whereas there size increases. A p-type conductivity is obtained for all implantation temperatures after annealing at temperatures above 1400°C. The lowest carrier concentration is observed for the room temperature implanted sample. The implantation temperature of 400°C represents an optimum temperature relating to the electrical parameters. With increasing annealing temperature the carrier concentration increases. The maximum value of 1.1E20 cm^{-3} is found for the Al concentration of 5E21 cm^{-3} after annealing at 1700°C.

A simple correlation between structural and electrical properties is not detected.

The Al distribution as determined by SIMS remains unchanged up to annealing temperatures of 1750°C.

NITROGEN IMPLANTATION IN 4H AND 6H-SIC

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Silicon Carbide is a promising material for high power, high temperature, high frequency applications. Ion implantation of SiC is a key process for producing devices such as diodes and planar field effect transistors. Ion implantation is the currently technique used to create selective area of doping. However, the conductivity and mobility obtained by this method are not fully established.
In this study, we have performed several nitrogen implantations in Si-faced (0001) 6H-SiC and 4H-SiC for a large variety of experimental conditions. Different box profiles were carried out ranging from 110 to 260 nm with the doses ranging from 10^{13} to 3.10^{15} cm^{-2}. The 6H-SiC and 4H-SiC samples were implanted at room temperature or at 650 °C. The samples were annealed at temperatures between 1100 and 1300 °C with different annealing times. The as-implanted and annealed samples were characterized by Secondary Ion Mass Spectrometry (SIMS) to determine nitrogen concentration profile before and after annealing [Fig.1]. A comparison was made with TRIM calculations to adjust the range parameters. TEM analysis of the same samples showed that the defect distributions obtained after room temperature and 650 °C implantation follow the "damage profile" (given by a TRIM Monte-Carlo simulation) and the "dopant profile", respectively.
Van Der Pauw test patterns were realised with a MESA structure and annealed ohmic contacts. Some of the samples were analysed with a Hall effect equipment in the temperature range 20 K to 420 K to extract the thermal dependencies of the resistivity and mobility. A modelisation of the doping levels is given to evaluate the activation and ionisation rate in this temperature range [Fig.2]. The low temperature mobility measurements give the compensation of the material. A comparison with the conductivity and mobility obtained on films doped during epitaxy and implanted films is done. It is shown that in the lower dose ranges, the ionisation and activation does not depend on implantation temperature. 4H and 6H-SiC materials have approximately the same ionisation rate. These results are discussed and a comparison between theory and experimental results is made.

This work was supported in part by DGA/DSP grant n°93-34-311-00028 and SGS THOMSON Microelectronics

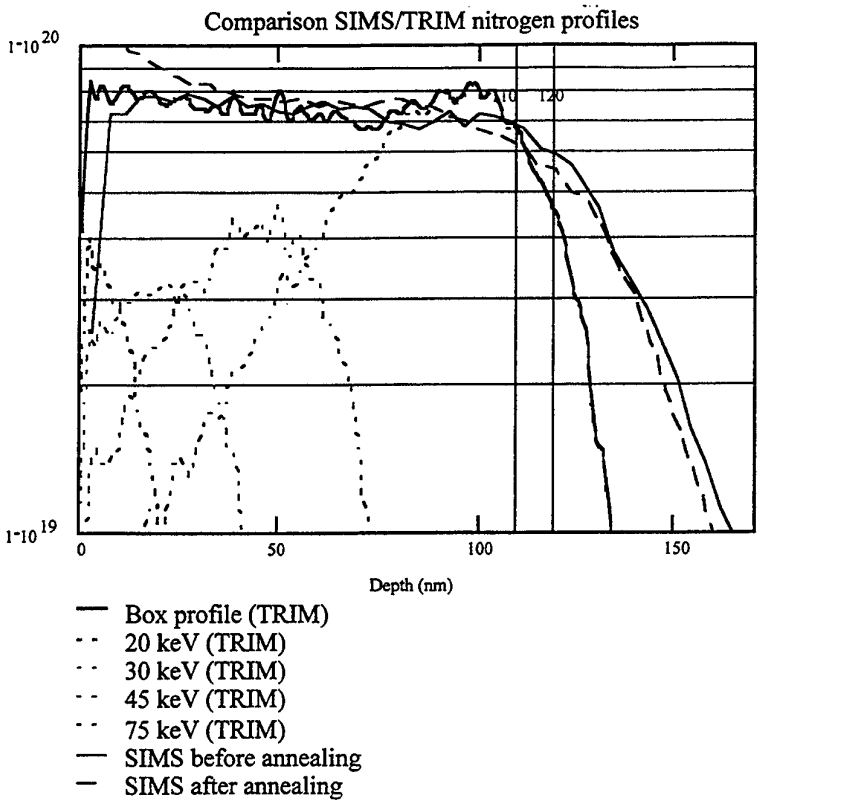

Fig. 1 : TRIM and SIMS nitrogen profiles

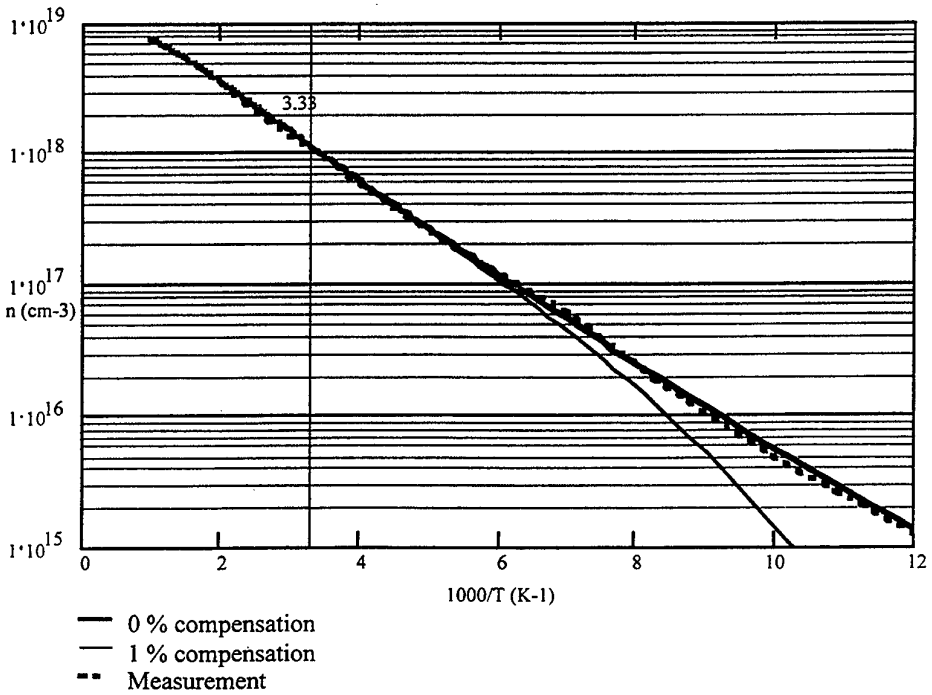

Fig. 2 : Modelisation and measurement of the doping level of a nitrogen implanted layer ([N] = 1E19 cm^{-3})

Lateral spread of implanted ion distributions in 6H-SiC : simulation.

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Multiple implantation has become a widely used process for device fabrication in Silicon Carbide (SiC). With this technique, appropriate flat shaped depth profiles can be obtained without the need of very high temperature redistribution annealings, which are not compatible with the overall device process. SIMS profiling technique is a powerfull tool for caracterizing such implantations. It shows well behaved impurity depth profiles with uniform concentrations from the crystal surface to a depth corresponding to the maximum implantation energy. Moreover, for device fabrication, the knowledge of lateral distribution of implanted ions at the mask edge is also of importance since it determines the geometry of lateral junctions. However, the lateral spread of the ions are much more difficult to measure than depth profiles. For this reason, simulation has been used successfully to determine tridimensional implanted ion distributions into Silicon. For SiC, this is an even more critical issue, first because diffusion is very low during the activation annealings, leaving the as-implanted profile unchanged and secondly because channelling is expected to influence the lateral spread of the ions, as much as it influences the depth profile. To date, no attempt has been made to study this phenomenon in SiC. In this work we use a home-made Montecarlo simulator to investigate the features of the 3D ion distribution in 6H-SiC. This hexagonal crystal contains critical planar and axial channels which cause distortions in the 3D distributions of the implanted ions. The use of enhanced models for electronic stopping, including a precise description of the map of valence electrons, increases the confidence in the simulation results. The models and their performaces are discussed in this paper. A systematic study is made in terms of implantation doses and energies. Practical cases are examined and possible improvements of the implantation conditions are proposed. The results of this study should be used for device performance analysis and for the description of the device structure in electrical simulations. Figure 1 shows an example of 2D profile obtained in the case of Aluminum implantation into 6H-SiC (Al 40 keV & $3.10^{13}cm^{-2}$, 150.000 ions trajectories). In this plot, one can see the lateral spread of the implanted ions. Some channelling effect can also be observed. The figure 2 is the corresponding 1D Depth profile.

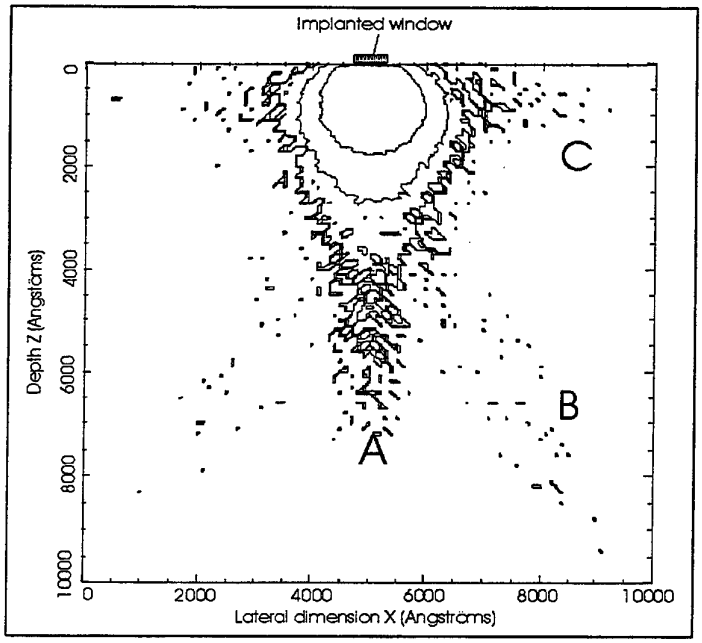
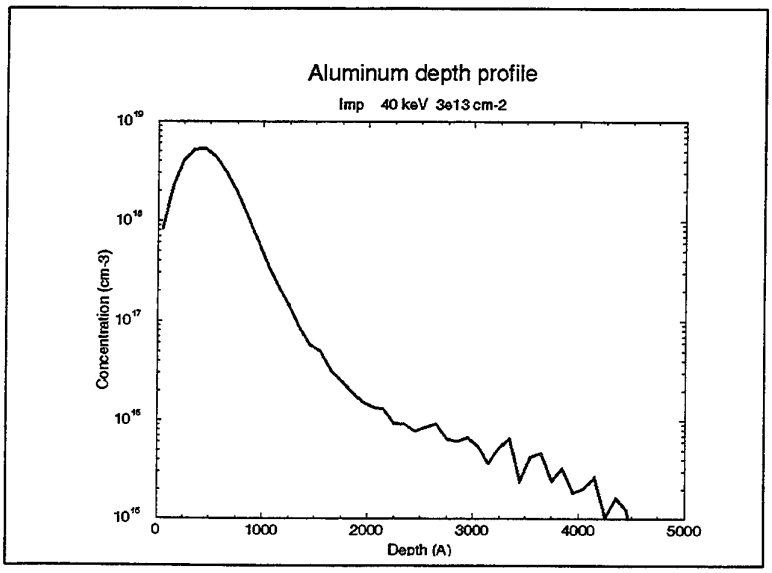


Fig. 1: Bidimensionnal Al distribution obtained by simulation of 150.000 ion trajectories. Al has been implanted at 40 keV/3.10^{13} cm^{-2} **A**: channelling along the <0001> axis, **B**: secondary axial channelling and **C**: axial channelling parallel to the surface.

Fig. 2: Simulated depth profile of Aluminum, corresponding to the implantation of figure 1 (Al 40 keV 3.10^{13} cm^{-2}).



ION IMPLANTATION INDUCED DEFECTS IN EPITAXIAL 4H SiC

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Thick epitaxial layers of 4H SiC are implanted with MeV He and B ions at low doses. The epi layers are nitrogen doped and has donor concentrations between 5×10^{14} and 1×10^{15} cm^{-3}. The ion energies are chosen to give a mean projected range of 4 μm for both He and B (1.7 and 5.0 MeV, respectively) and the implantation are performed both at nominal room temperature and 700 °C. After the implantation Schottky junctions are formed by evaporation of 1 mm diameter Au dots, and capacitance-voltage and deep level transient spectroscopy measurements are done. The low ion doses are estimated from previous implantations of silicon, where the defect concentration never exceeded the background doping. This makes it possible to study the samples with electrical techniques. According to these estimates the doses suitable for the doping of the present SiC samples range from 2×10^{8} to 1×10^{10} cm^{-2}.

Selected SiC samples were at the implantation accompanied by silicon $p^{+}n$ diodes with n doping of 9×10^{14} cm^{-3}. For lower doses these silicon diodes show no sign of compensation, as expected, implying that the concentration of defects is well below the doping concentration, even at the peak of elastic energy deposition at around 4 μm. However, the SiC samples implanted with the same dose are clearly compensated. This suggests that the interstitials and vacancies formed in the collisions with the incident ions to a large extent survive the immediate recombination and forms stable defects. In silicon this prompt vacancy-interstitial recombination is known to reduce the number of free migrating interstitials and vacancies with around 90% and the resulting concentration of deep level defects becomes much lower than in SiC.

Majority carrier DLTS temperature scans performed up to 375 K show two peaks visible at around 80 K and 280 K for a rate window of 400 ms. These two peaks are present before the implantation, but grow with increasing dose and/or ion mass. The dominating peak at 280 K is broad, which suggest that it consists of contributions from more than one deep level. The high temperature implantation seems to result in a shift in peak temperatures for the 280 K peak and also a narrowing of the peak width, which is in accordance with results from high energy electron irradiated samples.

DEEP LEVEL DEFECTS in H^+ IMPLANTED 6H-SiC EPILAYERS and in SILICON CARBIDE on INSULATOR STRUCTURES

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The IMPROVE* process has been applied to SiC to form Silicon Carbide On Insulator (SiCOI) structures [1,2]. With one SiC wafer (diameter : 35 mm), it is possible to obtain several SiCOI structures on 100 mm (or more) wafers. Hence common silicon processing line could be used for device processing on these structures. Nevertheless, the large dose (10^{16} to $10^{17}H^+.cm^{-2}$), needed for the transfer (as described on figure 1), creates defects which modify the electrical behaviour of the film transfered.

The aim of the present study is the investigation on defects which are responsible for the high electric compensation ($10^{17}cm^{-3}$ range) introduced in SiC during the hydrogen implant and anneal process. We have followed the evolution of these defects during annealing up to 1300°C by Low Temperature PhotoLuminescence (LTPL) and Deep Level Transient Capacitance Spectroscopy (C-DLTS) techniques on H^+ implanted 6H-SiC epilayers and on 6H-SiCOI structures. By LTPL, only the D_1-center -observed at 4720Å(L1-line), 4780Å(L2-line) and 4825Å(L3-line)- is detected as can be seen on figure 2. By C-DLTS, two centers are found on H^+ implanted 6H-SiC : P-center with an activation energy at E_a=0,35eV and a capture cross section $\sigma=3.10^{-19}cm^2$ and Z_1/Z_2-centers with E_a=0,65eV and $\sigma=3.10^{-16}cm^2$. Annealing of SiC during transfer process and post-transfer treatment increase Z_1/Z_2-centers concentration and introduces other deeper levels as shown on figure 3. The deepest defect level 'C' revealed by C-DLTS in 6H-SiCOI thermally reaches the highest concentration ($\approx 10^{17}cm^{-3}$) : E_a=0,85eV and $\sigma=1.10^{-18}cm^2$. This C defect could be a stable complex defect resulting from the clustering of simple intrinsic defects during annealing. Z_1/Z_2-centers observed by C-DLTS seem to be similar to the D_1-center observed by LTPL and could be a non-axial nearest-neighbour V_{Si}-V_C as proposed by several authors [3,4]. The growth of Z_1/Z_2 and C levels could be correlated with the decrease of P level. Eventually, we can conclude that at temperatures below 1300°C, P is a mobile point defect whereas Z_1/Z_2 and C defects are more complex ones.

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(*) IMPROVE (IMplanted PROton Void Engineering) is the generic name for transfer of thin films based on proton implantation and wafer bonding. The process is used by the SOITEC company under the registered name Smart-Cut® to produce SOI wafers and is called SiC Transit for the transfer of SiC films.

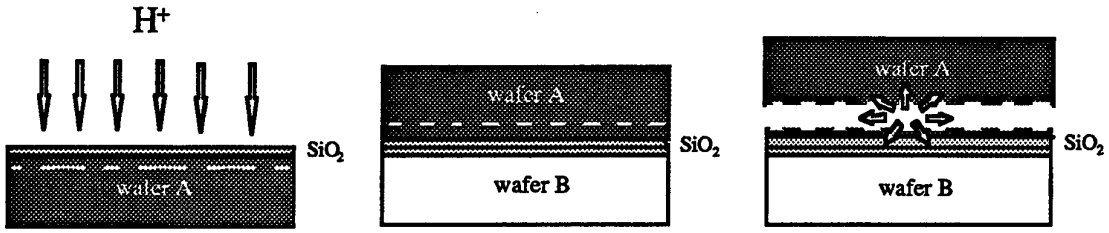

figure 1 : Principle of the IMPROVE process

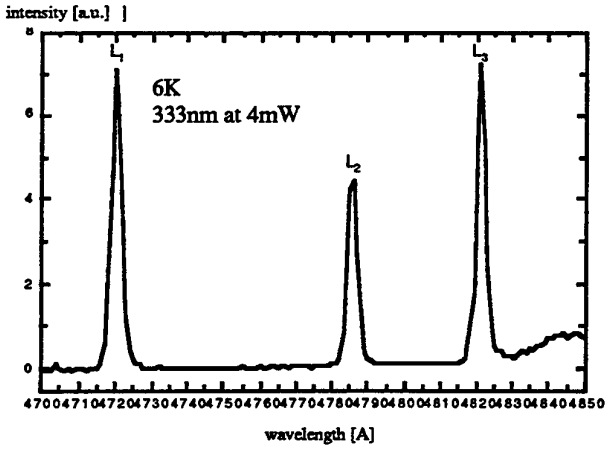

figure 2 : 6H-SiCOI PL spectra

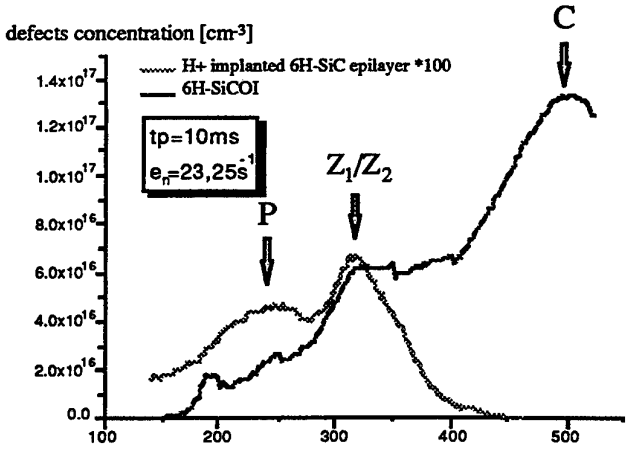

figure 3 : H+ implanted 6H-SiC epilayer and 6H-SiCOI DLTS spectra

SYNCHROTRON RADIATION DIFFRACTION IMAGING INVESTIGATION OF THE SiCOI STRUCTURE ELABORATED BY THE IMPROVE(*) PROCESS

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Recently, an original method to elaborate SOI (Silicon on Insulator) materials has been proposed by Bruel [1]. This process developped at LETI under the name IMPROVE(*) has two key steps, H^+ ion implantation and wafer bonding.

Hydrogen is implanted not as an impurity but as the element that induces, through the formations of microbubles, the splitting. For silicon, a dose of 10^{16}-10^{17} cm^{-2} and a thermal treatment are necessary to obtain these microbubbles. Associated to a stiffener these microbubbles create an in-depth splitting of the semiconductor so that the upper layer of the implanted wafer can be transferred onto the bonded wafer. This process has been successfully adapted to the Silicon Carbide material [2,3] to elaborate SICOI structure (SiC 5000 Å - SiO_2 - SiO_2 - Si).
We studied by synchrotron radiation diffraction imaging (X-ray topography), at the ID19 beamline of the ESRF, the quality of the wafer bonding before the transfer and the effects of the annealing on the SICOI structure.

Before thermal treatment, the variation of the contrast on the images from the silicon substrat allows to distinguish the regions where the bonding is successful from those where this bonding is imperfect. These last regions are mainly at the boundary of the SiC wafer, but also occur as circular areas inside the SiC wafer. After annealing, these regions are not transferred.
Defects induced by the thermal treatment have been observed and characterised (direction, Burger vectors,...). Misfit dislocations clearly appeared in the Si wafer around the SiC boundaries wafer mainly where the transfer does not occur. The center of the wafer is practically free from this type of defects.

(*) IMPROVE (IMplanted PROton Void Engineering) is the generic name for transfer of thin films based on proton implantation and wafer bonding. The process is used by the SOITEC company under the registered name Smart-Cut® to produce SOI wafers and is called SiC Transit for the transfer of SiC films.

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HALL EFFECT INVESTIGATIONS OF 4H-SIC EPITAXIAL LAYERS GROWN ON SEMI-INSULATING AND CONDUCTING SUBSTRATES

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Hall effect measurements on epitaxial or implanted layers result often in overestimated concentrations, if the resistance of the pn-junction used to insulate the layer from the substrate is low or comparable to the layer resistance. An alternative way to accurately determine the electrical properties of implanted or grown layers, is the use of semi-insulating layers or substrates, which are now available for SiC in the 4H polytype.

We have performed temperature dependent Hall effect measurements applying the van der Pauw technique on epitaxial 4H-SiC layers doped with aluminum or nitrogen. The layers were grown simultaneously on semi-insulating and conducting substrates (conductivity type opposite the conductivity type of the layer) in a horizontal reactor for vapor phase epitaxy (VPE). Besides the standard precursors silane and propane, trimetylaluminum and nitrogen gas were used as precursors for aluminum and nitrogen doping to achieve p- and n-type conductivity, respectively.

In addition to the Hall effect measurements, we used secondary ion mass spectrometry (SIMS) to determine the atomic aluminum and nitrogen concentrations and the thickness of the epilayers. The net doping concentration was measured by the capacitance voltage (CV) technique.

Comparing the results from SIMS, CV and Hall effect for the epilayer grown on semi-insulating substrates we found that the electrically active doping concentrations are equal to the atomic concentrations within the accuracy of the measurement techniques, indicating that the doping atoms are mostly incorporated on a lattice site and that the compensation is significantly lower than the doping concentration. For n-type epilayers we could determine by SIMS the concentration of compensating aluminum and boron atoms in the layer. The result is in agreement with the compensation obtained from the fit of the neutrality equation to the free carrier concentration, as measured by Hall effect.

For the growth of epilayers on conducting substrates we obtained, although grown in the same run, different results than for the growth on semi-insulating substrates. The fit of the neutrality equation resulted in an underestimation of the ionization energy for the shallow nitrogen level (nitrogen on a hexagonal lattice site) by about 15meV. For p-type epilayers on n-type substrates a clear p-type behavior was no longer observed in the low temperature range. Both observations indicate that the measured Hall voltage is most likely a combination of the Hall voltages created in the epilayer and in the substrate and that the substrate cannot be neglected for the calculation of the carrier concentration from the Hall coefficient. In addition we observed in the low temperature range for epilayers grown on conducting substrates a faster drop of the Hall mobility compared to epilayers on semi-insulating substrates.

In conclusion, to get the real electrical properties of thin layers with a standard van der Pauw Hall effect technique semi-insulating layers or substrates should be used to avoid an influence of the substrate on the results. The insulation of the layer by a pn-junction is in many cases not sufficient enough and can lead to erroneous results for ionization energy, doping concentrations, compensation and mobility.

INFLUENCE OF INHOMOGENEITIES ON THE ELECTRICAL CHARACTERISTICS OF TI/4H-SIC SCHOTTKY RECTIFIERS

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The high breakdown electric field of Silicon Carbide is of great interest for high power electronics. More precisely, in power conversion applications, the opportunity to use high voltage Schottky rectifiers with low series resistance can be investigated for the first time. The lack of reverse recovery phenomenon in such unipolar devices can be used to increase the frequency of operation in order to improve the conversion yield. As a first step, it is necessary to master the metal-semiconductor interface in order to obtain reproducible diodes.

Electrical characterization of Ti/4H-SiC Schottky rectifiers has been performed.

Significant dispersion is observed on the room temperature forward I(V) characteristics. Some of the rectifiers show good agreement with the thermoionic model. For these "normal" samples whose plot remains linear over 8 orders of magnitude, the barrier height F_b, the ideality factor n, and the series resistance can be extracted using the classical model. Other samples present excess current density for low voltage. For these rectifiers we have been able to fit the experimental characteristics assuming the coexistence of low (F_{bl}) and high (F_{bh}) barrier heights areas. In this model, the forward current results from the addition of the thermoionic currents provided by the two parallel diodes. The ideality factors are higher than those measured on "normal" rectifiers. Plotting the barrier height versus ideality factor for both kind of rectifiers reveals a linear trend. Extrapolation to n=1 gives a barrier height value F_{b0}.

Forward I(V) measurements as a function of temperature have been performed from 100 to 600K. On a given diode, a transition between one barrier and two barriers behaviors can be evidenced as temperature changes. Variations in the calculated barrier height and ideality factor are therefore evidenced. Plotting the extracted high barrier height versus ideality factor at various temperatures reveals a linear behavior with an extrapolated F_b value for n=1 very close to F_{b0} (agreement better than 10 mV), verified on more than 5 diodes. Material inhomogeneity is one possible explanation for the existence of inhomogeneous barrier height on the Ti/SiC contact.

However, the two parallel diodes model is not sufficient to explain the temperature dependence of Schottky barrier height or ideality factor observed on "normal" rectifiers for example. We used the Werner model of barrier height inhomogeneities to explain these phenomenon. It implies a Gaussian distribution of the Schottky barrier height around an average value calculated by C(V) measurement.

To sum up, a thermoionic current model considering two Schottky diodes connected in parallel has been developed and seems to fit experimental data. It shows that the scattered characteristics may be related to the relative proportions of the low and high barrier phases. The temperature variations of barrier heights and ideality factors extracted from classical thermoionic model have been explained using the Werner model.

Electrical noise used as a tool for assessing the defectivity of SiC Schottky diodes

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One of the main drawbacks which actually limits mass production of power SiC Schottky diodes is the unability to provide very large defect-free areas in a reproducible way. The residual density of micropipes or major defects in commercialized layers does not allow one to produce components exhibiting a high total current. Since such components are expected to play a major role in the field of fast power switches [1], it is therefore highly desirable to select already-existing analysis techniques, which can indicate whether a given component will fail or can be safely used in a system. In addition, one needs to use a non-destructive measurement method. In this paper we wish to report experimental results obtained with one of such techniques, which is the analysis of electrical noise in the low voltage range. This method cumulates several advantages: on one hand, it avoids any stressing of the devices; on the other hand, the sensitivity of the method to any kind of defect is much better than a simple measurement of excess current (the difference may indeed reach several orders of magnitude, see Fig.1). Eventually, that the detected defects are highly localized or not can be simply proved, inasmuch as the nature of the noise itself depends on the spatially localized character of a defective area.

In a preliminary report, we have observed discrete time switching events when measuring the current of SiC Schottky diodes [2]. These Random Telegraph Signals (RTSs) occur whenever an excess current is measured (Fig.2). Indeed, such a noise has already been extensively studied in other kind of devices. RTSs were observed very early in silicon diodes, at a time when Si substrates were still subject to metallic contamination, and were called burst noise. The origin of the RTS was soon attributed to the single trapping/detrapping of an electron in a centre located in the neighbourhood of a defective current path [3]. Here, we report various observations of RTS noise in large area Ti SiC Schottky diodes. The epilayer thickness was 6μm, the doping level was $3\times10^{16}cm^{-3}$ and the area ranged from 10^{-4} to $2.6\times10^{-4}cm^2$. Some diodes were defect-free whereas others exhibited one or a few RTSs. Summarized below are some experimental results obtained by measuring the noise of these diodes:

- Diodes without excess current exhibit noise characteristics qualitatively compatible with generation-recombination processes.

- The effective barrier height is considerably reduced in the defective zone (around 0.5eV), and the barrier height modulation causing the RTS is of the order of 1meV.
- Although one could only give an order of magnitude, the density of defective current paths roughly corresponds to that of the micropipes, suggesting that micropipes might be at the origin of such a noise.
- The behaviour of single electrical traps is different from one diode to another. A centre can be either a trap exchanging an electron with the conduction band, or can act as a generation-recombination (GR) centre. In the first case, only the average pulse time τ_U varies (exponentially) with V_F (Fig.4). In the second case (GR), both τ_U and τ_D vary, but in an opposite way, and their product remains roughly constant (Fig.5).

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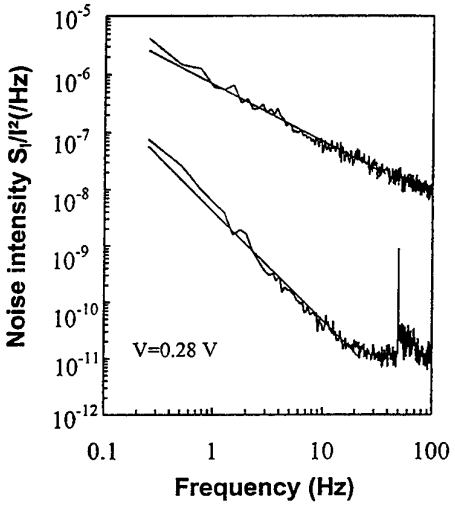

Fig.1: Noise spectra of a defect-free diode (lower curve) and of a diode exhibiting an excess current.

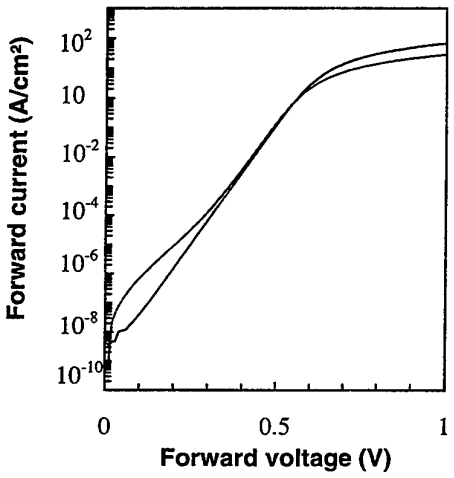

Fig.2: I-V curve of a defect-free diode (lower curve) and of a defective diode.

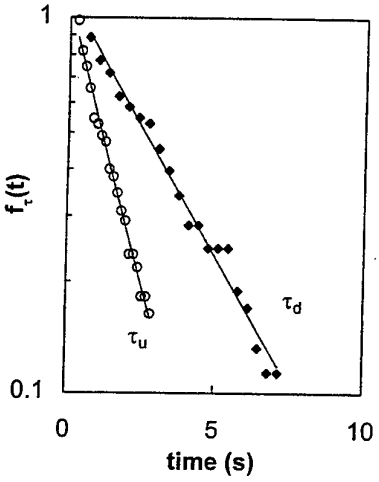

Fig.3: Exponential histogram of the RTS pulse times.

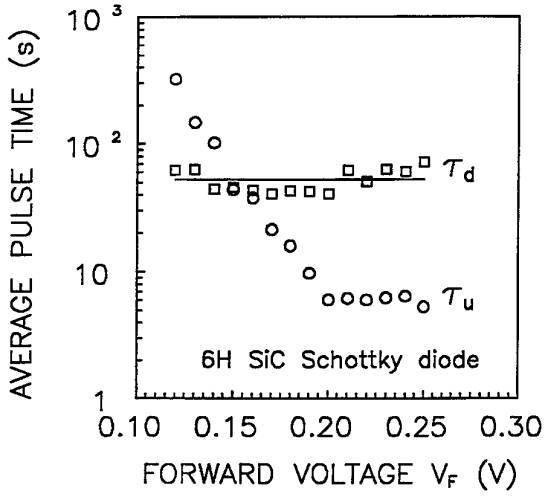

Fig.4: Average pulse times versus V_F of an RTS corresponding to an electron trap.

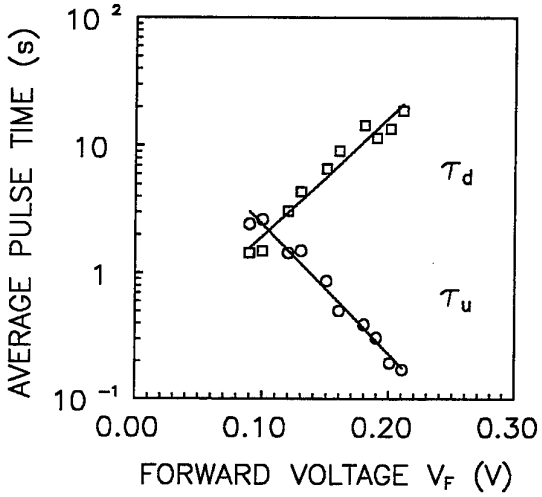

Fig.5: Average pulse times versus V_F of an RTS corresponding to a GR center.

Improvements in Pt-based Schottky contacts to ß-SiC

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The thermal stability of ohmic and rectifying contacts of SiC electronic devices is of extreme importance. In the case of ß-SiC/Si, the fabrication of good quality Schottky contacts is hindered by the large concentration of stacking faults, associated with the low stacking energy of this polytype, as well as with twins and threading dislocations occuring in heteroepitaxial films. Thus, the mediocre quality of ß-SiC heteroepitaxial material and the availability of good quality 4H and 6H SiC substrates has turned the mainstream SiC research towards these SiC polytypes. However, there are still active research groups in ß-SiC with the emphasis on high temperature sensors since the fabrication of sensing elements (e.g. membranes) can be achieved easier due to the etching selectivity between Si and SiC.
Several metals have been used as Schottky contacts to ß-SiC [1] and Platinum is one of them. In the present study, Platinum (Pt) contacts and Platinum/Silicon (Pt/Si) multilayer contacts have been compared. Pt/Si multilayer contacts (MLS) were employed to allow the formation of a platinum silicide layer at the top of the SiC with negligible consumption of the top SiC layer.
The material used was a 4 μm thick n-type CVD grown ß-SiC on Silicon, unintentionally doped, with a donor concentration of $3x10^{17}cm^{-3}$ (SiC1) [2].
A Chromium/Titanium/Platinum/Molybdenum/Gold metallisation strip on the one side of sample (SiC1) was used as the ohmic contact metallisation system [3]. Schottky circular dot arrays of 100 μm and 500 μm in diameter were then fabricated using standard contact positive resist photolithographic technique. On the one half of the sample 1000A of Pt were deposited while during a second evaporation, the Pt/Si multilayer system (Pt 95A / Si 250A / Pt 180A / Si 250A / Pt 95A) was deposited (Fig.1). Sample (SiC2) was placed together with (SiC1) and half of it was totally covered by Pt while the other half was covered by the MLS (Fig.2). During both evaporations the samples were kept at 110°C to ensure good adhesion between the SiC surface and Platinum.
The contacts (SiC1) were then sequentially annealed for 1 hour from 200°C - 700°C at 100°C steps under nitrogen flow. After each annealing step the I-V characteristics of the diodes were measured.
Sample (SiC2) was scribbed in three pieces initially. One piece was annealed at 200°C and the other was annealed at 700°C, both for 1 hour under nitrogen flow. The third piece was kept as reference. Then each one of the three pieces was again scribbed into two for TEM and XRD investigation respectively.

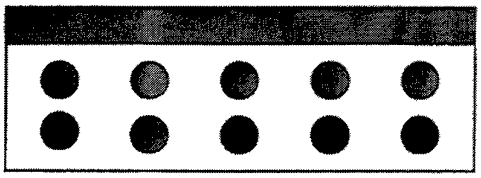

Fig.1: (SiC1) sample

ohmic contact
Platinum Schottky
MLS Schottky

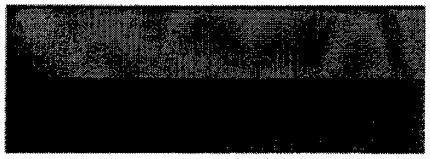

Fig.2: (SiC2) sample

Platinum region
MLS region

The Pt diodes exhibited best results regarding both the ideality factor and the leakage current after annealing at 300C. The multilayer diodes exhibited best results for ideality factor at 300C while best results for leakage current were obtained at 400C. The multilayer diodes remained rectifying up to annealing at 700C while the Pt diodes exhibited ohmic like behaviour following annealing at 500C.
XRD analysis of samples annealed at 700C showed the formation of different PtS_x phases for each case. TEM analysis of the same samples showed that for the Pt case, the SiC surface is burried with a thin metal layer and at some places large grains are grown into the SiC while for the multilayer case the SiC surface is intact.

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FORWARD CURRENT-VOLTAGE CHARACTERISTICS OF SILICON CARBIDE THYRISTORS AND DIODES AT HIGH CURRENT DENSITIES

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Forward current-voltage characteristics have been calculated for the 4H-SiC n-p-n-p thyristors with the breakover voltages of 400V and 700V in the temperature range of 300 - 500K up to current densities $\geq 10^4$A/cm^2. The calculations were made in the frame of the theory which takes into account the decrease of the emitter injection coefficient at high current densities [1]. The calculated results were compared with the experimental data.

To compare correctly the calculated and experimental characteristics, the lifetimes of minority carriers τ_n and contact resistivity R_c have been measured for the structures of both types. The $\tau_n \approx 80$ns at T = 300K, and $\tau_n \approx 280$ns at T = 500K. The W/L ratios estimated from the measured τ_n values agree reasonable with the values and temperature dependencies of the critical charge densities measured in these structures earlier [2]. (W is the width of the blocking p-base, L is the ambipolar diffusion length). The Rc falls within the range of $(1.5 - 4)\times 10^{-4}\ \Omega$ cm^2 and practically temperature independent.

Calculated and experimental results agree well within the wide range of current densities and temperatures (Fig. 1)

Fitting parameter of the theory is the saturation leakage current density j_s. The values of j_s were defined for SiC p-n junction for the first time: $j_s \cong \cdot 10^{-46}$-10^{-45} A/cm^2 at 300K, $j_s \cong \cdot 10^{-22}$ -10^{-23} A/cm^2 at 500K, and $j_s \cong \cdot 10^{-18}$ - 10^{-17} A/cm^2 at 600K (at 300 K the values of j_s for Si p-n junctions falls in the range of $j_s \cong \cdot 10^{-14}$ - 10^{-12} A/cm^2, for GaAs p-n junctions- in the range of 10^{-18} - 10^{-16} A/cm^2 [3]).

In the frame of such calculations, the related contributions of contact resistivity and non-ideality of the emitter junctions to the voltage drop on the thyristor structures may be considered (Fig. 2):

It is seen that even with the same quality of junctions , the voltage drop may be reduced essentially (Curve 2). "Ideal" junctions (Curve 3) may be practically considered as a very high doped emitter layer with the high enough values of τ_n and diffusion coefficient D_p. One can see that the combination of such an "ideal p-n junction and contacts with low resistance may provide the voltage drop values across the SiC p-n junctions at high current densities which is sufficiently less than across identically rated Si and GaAs thyristors [4]

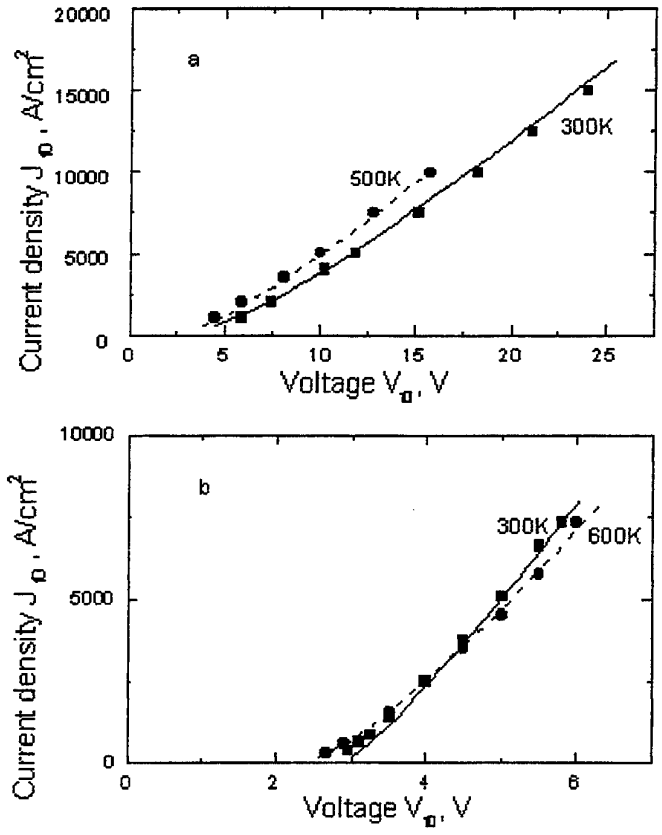

Fig. 1. The current-voltage characteristics of the thyristor structures. Curves are calculated dependencies; marks represent the related experimental data.

a. 700 V thyristor

T=300K:

$R_c = 4 \cdot 10^{-4}\ \Omega \cdot cm^2$, $\tau_n = 80ns$.

$j_s = 1.1 \cdot 10^{-45}\ A/cm^2$

T=500K:

$R_c = 4 \cdot 10^{-4}\ \Omega \cdot cm^2$, $\tau_n = 280ns$,

$j_s = 1.5 \cdot 10^{-23}\ A/cm^2$

b. 400V thyristor

T=300K:

$R_c = 1.5 \cdot 10^{-4}\ \Omega \cdot cm^2$, $\tau_n = 80ns$.

$j_s = 1.5 \cdot 10^{-46}\ A/cm^2$

T=600K:

$R_c = 1.5 \cdot 10^{-4}\ \Omega \cdot cm^2$,

$\tau_n = 280ns$.

$j_s = 4 \cdot 10^{-18}\ A/cm^2$

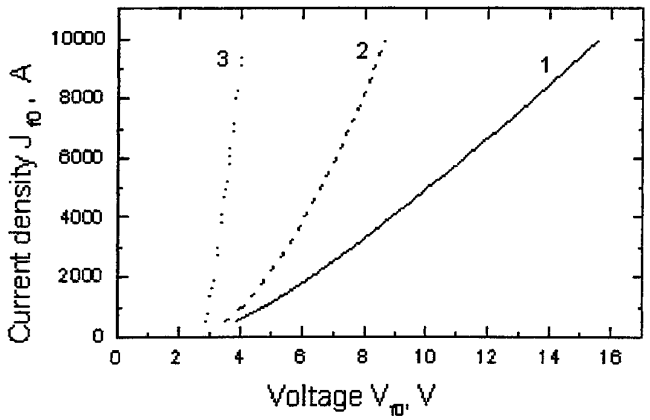

Fig 2. Calculated current-voltage characteristics of 700 thyristor.

1. Current-voltage characteristic reproduces solid curve of Fig. 1a.
2. Calculation for the same set of the parameters but with $2R_c = 10^{-4}\ \Omega \cdot cm^2$ (instead of $2R_c = 8 \cdot 10^{-4} \Omega \cdot cm^2$ as it has been taken for the curve 1).
3. Calculation for the case of $2R_c = 10^{-4}\ \Omega \cdot cm^2$ and " ideal" junctions ($j_s = 0$).

Acknowledgments

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OPTIMISATION OF A POWER 4H-SIC SIT DEVICE FOR RF HEATING APPLICATIONS

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For many RF heating applications, a power device (high voltage ≥ 600 V, high current density : 0.5-1 kA/cm^2) able to work at the industrially reserved frequency of 27.12 MHz is required. Silicon carbide could be a suitable material because of its high critical electric field and good electron mobility. These features allow minimisation of the epitaxial layer resistivity and active device area. A vertical structure such as a SIT (Static Induction Transistor) provides more efficient use of device area than lateral MESFET structures at high voltage levels. In this paper, the optimisation procedure for a SIT design is described and its application in a typical RF heating circuit is presented. Static and transient optimisation studies are carried out by means of TCAD simulation using MEDICI. It is demonstrated that the SiC SIT could become a viable alternative to the vacuum tube triode valve in high power RF power supplies.

Optimisation of the SIT design is achieved by varying the epitaxial layer thickness and doping, the device geometry and the design of edge termination within known technological constraints (c.f. Figure 1). In the current work, these constraints include a minimum feature size of 2μm and a maximum pinch-off gate voltage of 20V. The structure and the physical parameters used in simulations are described, in particular those associated with the ionisation coefficients and mobility models. A field plate edge termination is optimised for a 10μm thick epitaxial layer with doping of 10^{15}cm^{-3}. Results show a breakdown voltage of 1300V with breakdown located at the end of the field plate, corresponding to 69% of the theoretical value.

DC reverse and forward characteristics are optimised (c.f. Figure 2) by altering the epi-layer doping level to achieve maximum current density without degrading the pinch off performance. A doping level of $5\text{x}10^{15}$cm^{-3} is revealed to offer the best compromise, allowing pinch off of over 600V from a 20V gate drive and achieving a current density of 10μA/μm^2 at an on-state voltage of less than 1V.

SIT device behaviour in an inductive load switching circuit is studied (c.f. Figure 3) by using the Circuit Analysis Advanced Application Module (CAAAM). The effect of the field plate is analysed and is shown to severely degrade the potential high frequency performance. This is due to the additional capacitance of the MOS structure, which must be driven from the gate. It is of greatest significance in small devices where the ratio of junction periphery to active source area is relatively large. Other field termination techniques (e.g. implanted p-type guard rings, floating metal rings, high resistivity region formed by implanting argon or boron) will be considered in the final paper. Further work will concentrate on issues of device layout, practical realisation of the structure and simulation of a RF heating circuit employing 4H-SiC SITs.

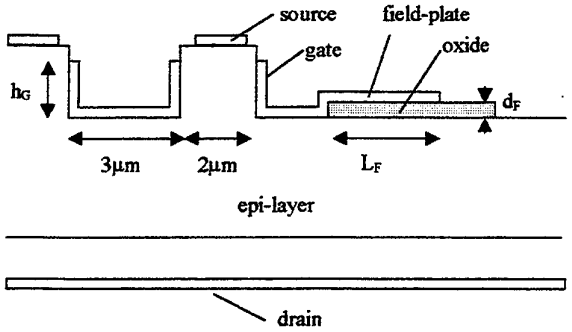

Figure 1: Structure of SIT showing technological constraints on gate and source geometry. L_F, d_F and h_G are the geometrical parameters varied during optimisation.

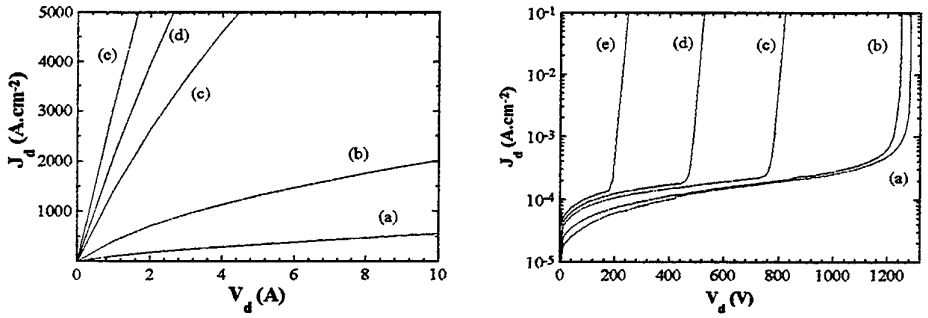

Figure 2: On-state current density (a) and blocking capabilities (at -20V applied gate-source voltage) (b) versus the n-type doping level of the epilayer : (a) : 10^{15} cm^{-3}, (b) : $2x10^{15}$ cm^{-3}, (c) : $5x10^{15}$ cm^{-3}, (d) : $7x10^{15}$ cm^{-3}, (e) : 10^{16} cm^{-3}

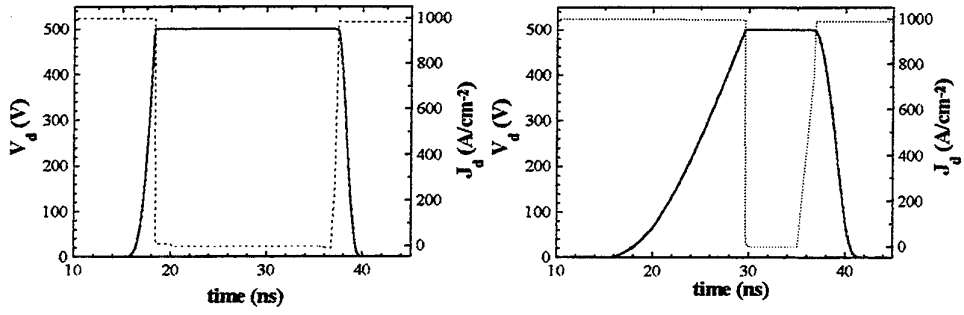

Figure 3: Inductive load switching waveform without (a) and with (b) edge termination (— : V_d vs. t, — : I_d vs. t). In each case the simulation includes one source finger. Applied gate voltage has 5ns rise and fall times.

NUMERICAL SIMULATION OF IMPLANTED TOP-GATE 6H-SiC JFET CHARACTERISTICS

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Introduction: In recent years, a large variety of promising SiC-devices have been realized in the fields of high power, high temperature, and high frequency device applications. To date, numerical simulation of SiC-devices have been used mostly for developing new device concepts as well as to investigate principal physical mechanisms governing the device characteristics. With the view of exploring the feasibility of a quantitative comparison of simulated and measured device characteristics, numerical simulations of several high temperature top-gate junction field-effect transistors have been performed across a temperature range of 300 - 673 K and various bias conditions.

Device structure and electrical characterization: The fabrication and electrical characterization of the investigated devices is reported in [1]. Fig. 1 shows the cross-section of the depletion mode, implanted top-gate JFET, giving basically separate control of top and bottom gates.

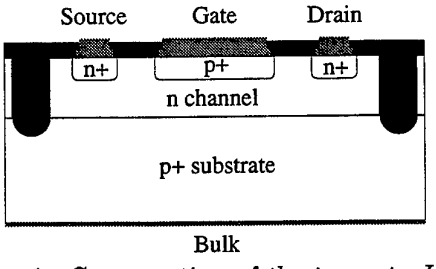

Figure 1: *Cross section of the top gate JFET.*

Five devices have been investigated with different ratios of channel width W to channel length L.

Simulation results: The results are based on numerical isothermal drift-diffusion simulations [2] with 6H-SiC material parameters as reported in [3] that were carefully updated with respect to recently published experimental data.

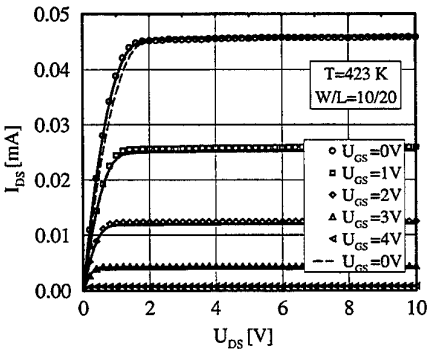

Figure 2: *Measured (symbols) and simulated output characteristics excluding (dotted lines) and including (full lines) non-uniform channel doping concentration.*

Together with measured values (symbols), the simulated transfer and output characteristics at $U_{BS} = 0\,\mathrm{V}$, based on analytically extracted device parameters as reported in [1], are shown as dotted lines in Fig. 2 and Fig. 3. The transconductance $g_{mT}(U_{GS})$ is very sensitively influenced

by the channel thickness t_n and doping concentration N_{epi}. Therefore, these two parameters are not independent of each other. Assuming a $t_n = 500\,\text{nm}$, N_{epi} can be very accurately extracted by fitting the simulated transfer characteristics to the linear plot of the measured data (Fig. 3). However, with a constant value $N_{epi} = 7.4 \cdot 10^{16}\,\text{cm}^{-3}$, a slightly different on-resistance (Fig. 2) and a significant disagreement of the exponential part of the transfer curve in the vicinity of the threshold voltage (Fig. 3) are observed.

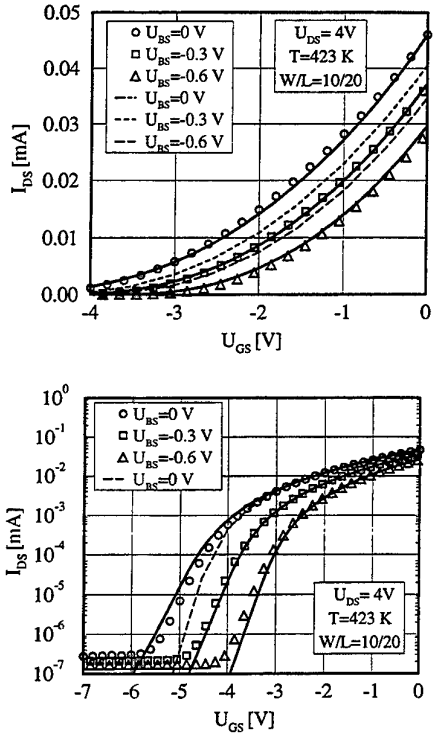

Figure 3: *Linear and Logarithmic plot of measured (symbols) and simulated transfer characteristics excluding (dotted lines) and including non-uniform channel doping concentration.*

Additional information about the channel device parameters can be obtained by measuring the transfer characteristics at different substrate potentials. In this case, the simulation strongly disagrees with the measured data (Fig. 3). The variation of the measured $I_D \sim \sqrt{U_{BI} - U_{BS}}$ confirms that the channel is controlled by the space charge region at the substrate junction w_B. However, any readjustment of N_{epi} and t_n in order to fit to the bottom-gate transfer characteristic $g_{mB}(U_{BS})$ would result also in an additional change of the simulated top gate control characteristics $g_{mT}(U_{GS})$. An analysis of all relevant device parameters proves that only a non-uniform effective channel doping concentration $N_{epi,eff}$ can explain this finding. By readjusting the transfer characteristics including this effect, an excellent agreement of all curves is obtained (Fig. 2,3).

Subsequently, the temperature dependent device characteristics have been investigated in the range of 300 - 623 K (Fig. 4). A temperature coefficient $\alpha = -1.77$ for the channel mobility $\mu(T) = \mu_n \cdot (T/300K)^{\alpha}$ is obtained, which has been reported for high quality epitaxial material [4].

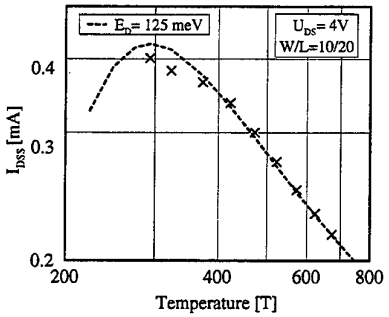

Figure 4: *Measured (symbols) and simulated temperature dependent drain saturation current.*

Assuming that the measured distribution of the threshold voltage of the devices is due to a variation of t_n across the wafer, all investigated structures can be simulated with quantitative agreement to measured data without the need of adjusting any other device or material parameter (Fig. 5).

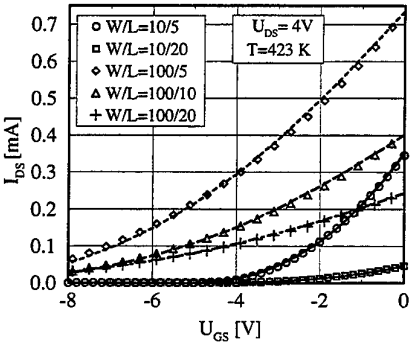

Figure 5: *Measured (symbols) and simulated transfer characteristics scaled at $W = 10\mu\text{m}$.*

Conclusion: It is demonstrated by numerical simulations of well-characterized 6H-SiC JFET structures that the concept of inverse modeling is applicable to present-state SiC devices. This can lead to a significant improvement of process and device development.

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WIDE BANDGAP MICROWAVE POWER MESFET PERFORMANCE POTENTIAL

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Introduction

This paper evaluates the theoretical potential of the wide bandgap (WBG) semiconductors SiC and GaN for microwave power MESFET devices. Their performance is compared to a baseline model of the current GaAs capability. The expected power and frequency performance is modelled and, in contrast to most previous studies, the impedance matching and associated stability issues arising when deploying the devices in a microwave power amplifier are examined.

High Power Potential

There is substantial evidence for the high power capability of the WBG materials [1-5]. The likely potential capability may be estimated by considering the limits imposed by their respective thermal conductivities and electrical breakdown fields. Table 1 projects the output powers expected for devices, integrated circuits and modules. The thermal limits are obtained from a 3D finite-difference multifinger power device model. The fingers are spaced by 30μm on 100μm substrates and a peak temperature of 150°C with 40% efficiency is assumed. The electrical power limits are scaled from that currently achieved by GaAs technology at 10GHz by the ratio of their breakdown fields. The chip and module-level combination factors are taken to be the same as for the current GaAs technology. It is found that the 10GHz output power capabilities for SiC and GaN-on-SiC are expected to exceed 40W for microwave integrated circuits and 200W for multi-chip modules.

High frequency potential

In order to provide effective performance at microwave frequencies, the devices must also have adequate gain. This aspect of performance has been investigated using an analytical physical model [6] of a 0.5μm gate device. The model is appropriate for the purpose of exploring the microwave circuit implications and allows rapid variation of device parameters to be performed.

A comparison of the expected frequency performance of the devices is given in figure 1. The figure shows the figures of merit f_T and f_m (unity current gain and unity Maximum-Available-Gain frequencies) plotted against mobility. The mobilities appropriate for GaAs, 6H and 4H SiC, and GaN are marked. The figure gives insight into the device operation with the key observation that, unlike GaAs, the power gain of the WBG devices is strongly dependent on the mobility. However, for relatively modest values of mobility the predicted gain approaches and even exceeds that for GaAs. A similar plot against saturated velocity shows that GaAs device performance, unlike SiC and GaN, is limited by the saturated velocity.

Microwave transistors are generally potentially unstable and measures must be employed to prevent unwanted oscillations. A feature which strongly influences their propensity to oscillate is their internal

output conductance. High voltage devices have a low output conductance in order to hold off the high voltage and to deliver power effectively into the high resistance load. For this reason WBG devices are inherently less stable than their lower voltage GaAs counterparts. Consequently more extreme measures are required to prevent oscillation. This gives rise to a fundamental trade-off between input impedance and gain which allows the circuit designer some freedom to select the most appropriate combination.

The input impedance is of great concern for power devices since the difficulty in matching to low impedances often limits the maximum size of a power transistor. Furthermore, a low finger impedance gives rise to loaded-line effects which degrade the performance when fingers are combined to form a power device. The low mobility of WBG materials suggests that an improved input impedance can be expected. This is quantified by comparing models of 300μm wide power-cells operated at 10GHz. A number of such cells would be connected in parallel to form a power transistor. The results of the comparison are given in table 2. Maximum drain voltages of 16V for GaAs and 100V for SiC/GaN are assumed. A peak current of 300mA/mm is used throughout. The table shows: the Sterne stability factor, k, of the devices (where k<1 indicates potential oscillation); the apparent load resistance, R_{LI}, applied to the device; the expected output power; the small-signal gain for the appropriate high power load and the input match resistance. The results suggest that the WBG MESFETs are expected to be highly effective as microwave power devices. For a given gate width, the WBG devices offer gain within 1dB of that of GaAs, an input impedance of the order of a factor of two higher, together with an increase in output power of approximately a factor of six.

Conclusions

Intrinsic electrical and thermal limits suggest that WBG power MESFETs can provide >40W microwave integrated circuits and >200W modules. The effect of low mobility in WBG materials is offset by a high saturated velocity and for similar gate lengths, it is shown that WBG devices can deliver similar gain with improved input impedance compared to GaAs. WBG devices are intrinsically more unstable and more careful stabilization is required to achieve these enhanced benefits.

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	GaAs	SiC	GaN	GaN on SiC	Key:
Device (W/mm)	0.75	6.6	6.6	6.6	Electrically limited
	0.70	9.6	2.5	7.7	Thermally limited
MMIC (W)	5.0	43.8	43.8	43.8	
	4.7	64.0	16.7	51.3	
Module (W)	25.0	218.8	218.8	218.8	
	23.0	320.0	83.3	257.0	

Table 1: Projected WBG 10GHz power performance.

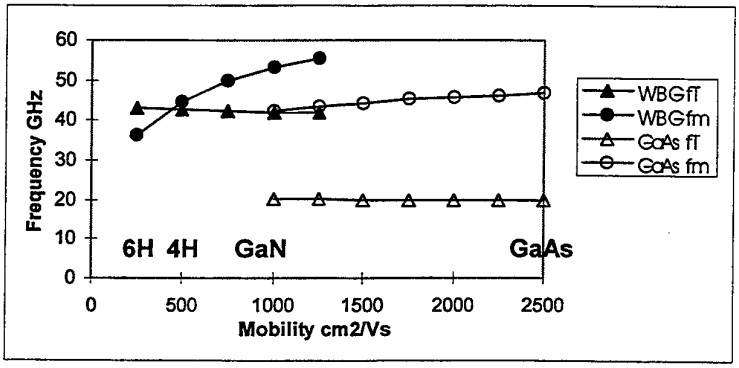

Figure 1: Modelled mobility dependence of frequency performance.

	k	R_{LI} Ω	Power W	Gain dB	Input Match Ω
GaAs	0.74	160	0.23	11.4	4.4
SiC	0.49	1100	1.4	10.6	7.9
GaN	0.46	1100	1.4	12.0	7.5

Table 2: Comparison of 300μm MESFET power-cell performance at 10GHz.

P-N JUNCTION CREATION IN 6H-SiC BY ALUMINUM IMPLANTATION

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Introduction

Ion implantation is a necessary process for the creation of localized p-n junctions in SiC, since the low diffusion coefficients of the main dopant impurities prevent from thermal diffusion techniques. The most commonly used p-type dopants are aluminum and boron, due to their low ionization energies. Each of these group-III elements has a double energy level above the valence band. We performed aluminum implantations at room temperature into n-type 6H-SiC epilayers, in order to create a 0.5 μm depth box profile p^+-region at a concentration of $4x10^{19}$ cm^{-3}. The implantations were followed by high-temperature furnace annealings, aiming at reordering the crystal and activating the dopants. This paper is focused on the annealing optimization to obtain the best electrical results, with the lowest thermal budget.

Experiment

Five Al implantations were performed at RT, into a n-type epilayer (10 μm - $3.8x10^{15}$ cm^{-3}) deposited on a n^+ substrate (300 μm - $1.5x10^{18}$ cm^{-3}). The implantation energies and corresponding doses are shown in Table 1, with the projected ranges Rp and straggles ΔRp issued from TRIM'94 data. The total dose is $1.75x10^{15}$ cm^{-2}, so above the critical threshold for amorphization. The tilt and rotation angles are 7° and - 90° respectively ; they are chosen to minimize the channeling effect.

Results

Fig.1 compares two impurity profiles : one is obtained with TRIM code calculations, and the other is from SIMS analyses. We observe an extension of the distribution tail in volume, due to channeled ions issued from the first implantation at 300 keV. The associated fluence with 300 keV is $8x10^{14}$ cm^{-2}, and the material is probably not yet amorphized. The point where implant damage is maximum must be situated at 0.7xRp [300 keV] = 234 nm. The zone between the surface and this point probably becomes amorphous just after the following implantations, due to the accumulation of their related defects (interstitial dopants, recoiled atoms).

Fig.2 displays several RBS/C signals (Rutherford Backscattering Spectrometry in Channeling geometry). First, the as-implanted material signal is compared with the random signal (corresponding to amorphous SiC). Assuming a constant SiC density of 3.2 $g.cm^{-3}$, we determine an amorphous/crystalline interface depth of 0.25 μm (close to 234 nm). Second, the signal of the same material after an annealing under argon atmosphere at 1700°C during 30 minutes is shown. This annealing was performed in the best furnace configuration, which leads to no surface dissociation (in terms of stoichiometry and chemical bonds). The annealed signal is compared with the virgin signal. We can deduce a perfect recrystallization of the material.

This result is confirmed by the sheet resistance measurements at RT (four probe configuration), which give a surface resistivity of $6.6x10^{-3}$ Ω.cm, and so an electrical activation of about 60 %.

In order to reduce the thermal budget, different annealings were carried out. Fig.3a shows the variation

of some RBS/C signals with temperature, and Fig.3b depicts the dechanneling yield comportment with the annealing duration. The final paper will analyze the relations between these effects and the electrical activation variation.

Table 1 *Implantation characteristics*

Energy	Dose	Rp	ΔRp
300 keV	$8x10^{14}cm^{-2}$	335 nm	77.9 nm
190 keV	$3.9x10^{14}cm^{-2}$	211 nm	56.6 nm
115 keV	$2.8x10^{14}cm^{-2}$	127 nm	38.5 nm
60 keV	$1.9x10^{14}cm^{-2}$	66 nm	22.8 nm
25 keV	$9.0x10^{13}cm^{-2}$	29 nm	11.0 nm

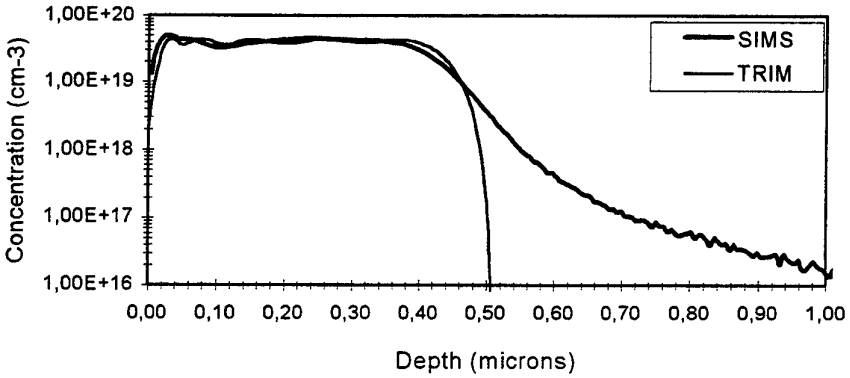

Fig.1 *Impurity profiles*

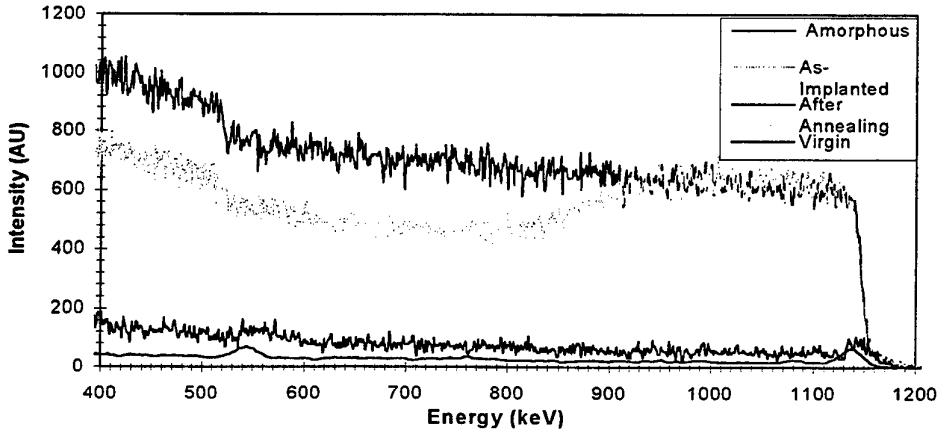

Fig.2 *RBS/C signals*

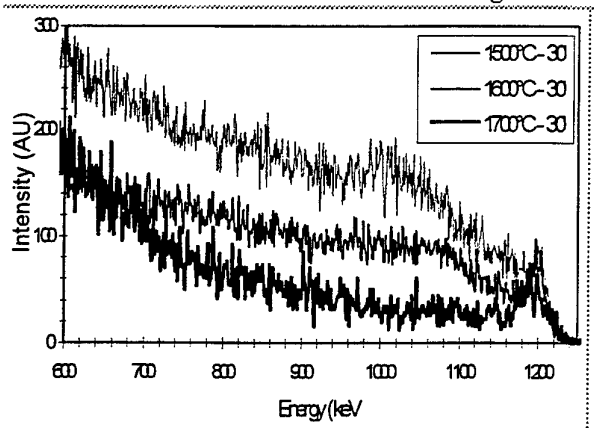

Fig.3a *RBS signals vs annealing temperature*

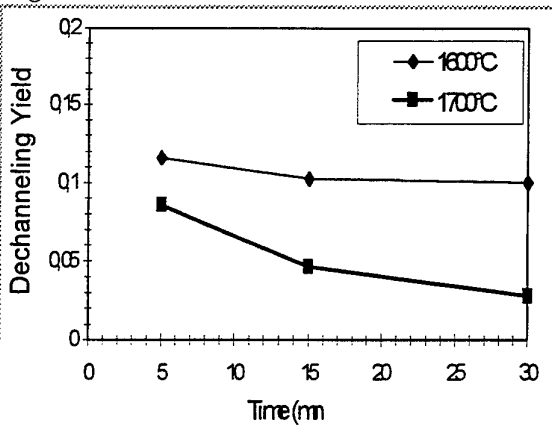

Fig.3b *Dechanneling yield vs annealing time*

ON THE INTERPRETATION OF HIGH FREQUENCY CAPACITANCE DATA OF 6H-SiC BORON DOPED $P^+N^-N^+$ JUNCTION

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INTRODUCTION. Silicon carbide having unique electrical and thermal properties, is a very promising material for high-temperature, high–power and high-frequency applications. In order to produce high voltage silicon carbide pn diodes, one uses boron doping for compensating the n epitaxial layer. As a result of the boron diffusion, the high frequency C(V) characteristic can no more be interpreted by the use of a conventional model. The aim of this paper is to propose a new complete model for the high frequency C(V) curves of the 6H-SiC boron doped $p^+n^-n^+$ junction.

DEVICE DESCRIPTION. The structure is made on n^+ substrate doped with nitrogen and realized by the Lely method. A n-type layer (base), followed by an Al-doped p^+-type layer are grown by sublimation epitaxy on the substrate. Then, the structure is diffused with boron at high temperature (2000°C) for base doping compensation. Finally the conventional steps for mesa diode structure preparation are achieved.

RESULTS AND DISCUSSION. High frequency (1 MHz) C(V) measurements at room temperature are used to evaluate the parameters of the structure. Fig. 1 presents the normalized C(V) curves measured on a boron doped (BD) structure in comparison with the boron undoped (BU) one. The BU junction shows a "classical" C(V) characteristic for the whole voltage domain and C^{-2} dependence on V is linear (Fig. 2a). In contrast, on the C(V) curve of the BD structure we identify three regions (Fig. 2b) related to the expansion of the depletion region in an totally compensated layer (I) and in the transition zone (II and III). The last zone is also due to the boron diffusion. In every region C^{-2} varies linearly on the applied voltage, with a decreasing slope from region I to III (Fig. 2b). For modeling the C(V) behavior we propose the equivalent circuit from Fig. 3. C_i represents the capacitance of the totally compensated layer. The latter being fully depleted for $V<0$, C_i is a constant capacitance. C_b is the barrier capacitance of the depletion region in the n^+ substrate (Fig. 3). C_p is the parasitic capacitance of the measurement system. The model evinced in Fig. 3 serves to the accurate estimation of technological data of the structure by using an optimal extraction program. The values of the parameters, together with the region where their value is extracted from are presented Table 1. $N_{D,i}$, w_i are the parameters of the totally compensated layer (Fig. 3b). $N^{II}_{D,med}$ and $N^{III}_{D,med}$ are the average ionized impurity concentration in the transition zone, extracted in region II and III respectively. V_{bi} is the built-in voltage of the p^+n^- junction (Fig. 2a) and V_i the forward voltage up to which the compensated layer is completely depleted. The forward characteristics in Fig. 4 confirm the extracted V_i value from Table 1. The extracted $N_{D,i}$ and w_i values confirm the very weak base net doping resulted from the boron diffusion.

Table 1

Parameter	N_A^+ (cm^{-3})	C_I (pF/cm^2)	w_i (μm)	V_{bi}(V)	V_i(V)	$N_{D,i}$ (cm^{-3})	$N^{III}_{D,med}$ (cm^{-3})	$N^{III}_{D,med}$ (cm^{-3})
Deduced from	Region I	Region II	$w_i = \frac{\varepsilon}{C_i}$	Region I	$V_i = V_{bi} - \frac{q \cdot N_{D,i}}{2\varepsilon} w_i^2$	Region I	Region II	Region III
Value	$3x10^{17}$	787	10.9	2.51	1.5	10^{13}	$6.5x10^{14}$	$3.6x10^{15}$

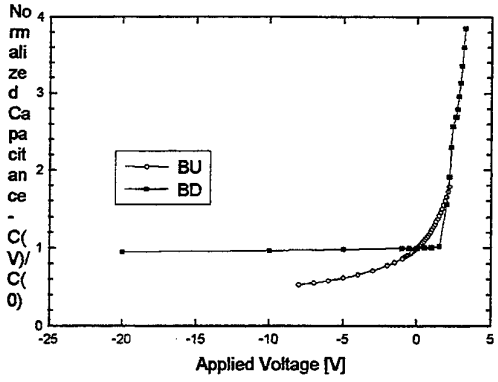
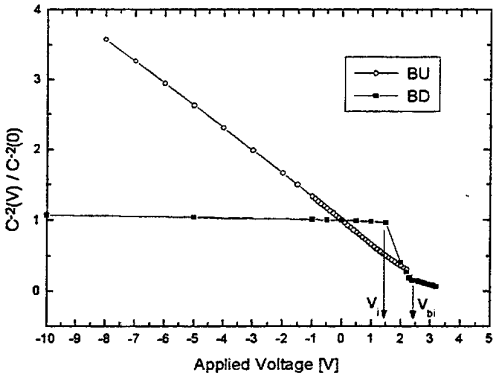


Fig. 1 Normalized C(V) characteristics



(a)

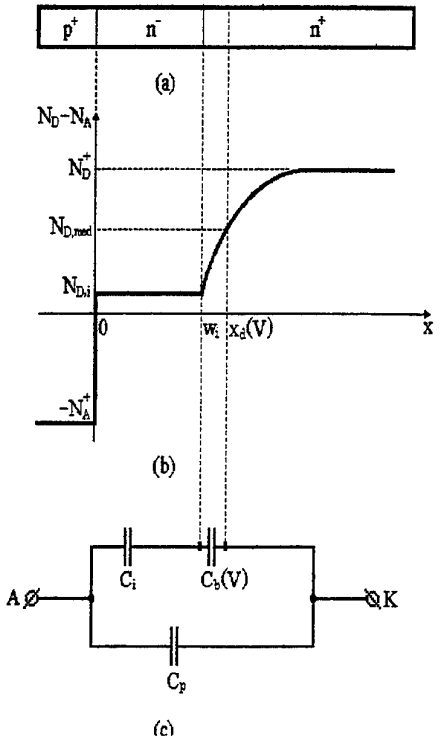
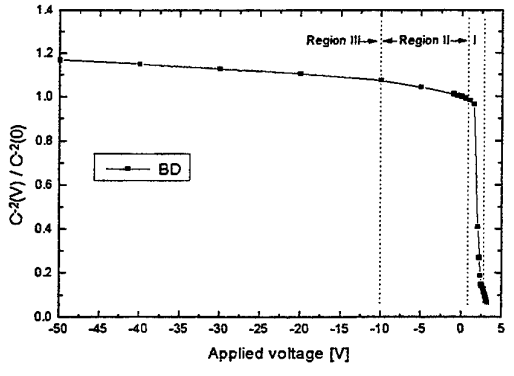


Fig.3 (a) – $p^+n^-n^+$ structure;
(b) - ionized impurity distribution;
(c) – equivalent circuit.



(b)

Fig. 2 Normalized $C^{-2}(V)$ curves. C(0) represents the measured capacitance at zero bias.

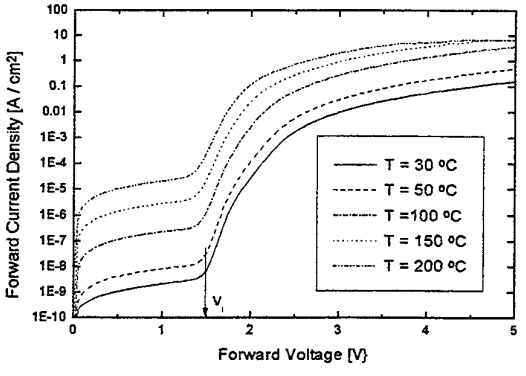


Fig. 4 Measured forward characteristics at different temperatures on BD diode.

ACKNOWLEDGEMENTS. This work was supported by the European Community, under the INCO-COPERNICUS 96-0211, PODILESCA project.

CURRENT-VOLTAGE CHARACTERISTICS OF LARGE AREA 6H-SiC $p^+v^-n^+$ DIODES

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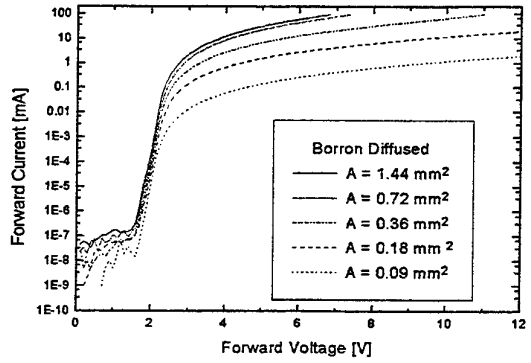
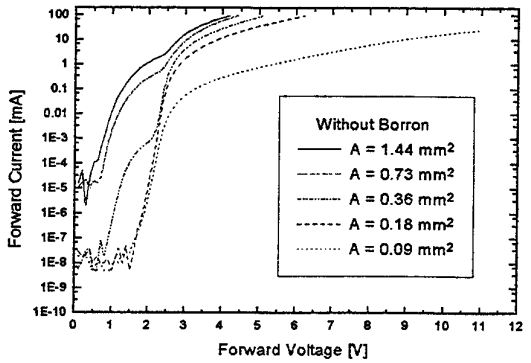
INTRODUCTION. Up to now SiC high breakdown voltage (kV) pn diodes have been reported, but having small area, due to the high material defect density [1]. This paper presents and models the I-V characteristics of large area 6H-SiC $p^+v^-n^+$ diodes with reverse voltage up to 950 V at room temperature.

DEVICE FABRICATION. The structure is made on n^+-substrate prepared by the Lely method. A n-type layer, followed by a Al-doped p^+-type layer, are grown by sublimated epitaxy on the substrate. The doping of the base layer is controlled by boron diffusion at high temperature (2000 °C). As a result, a low-doped (quasi-intrinsic) base layer with $N_{D,i}=10^{13}cm^{-3}$ doping and $w_i=10.9\mu m$ thickness is produced. Diodes with different areas (0.18 – 1.44mm^2) were defined by mesa etching to a depth of about 7μm using planar CF_4 plasma and then passivated by APCVD PSG. Al and Ni ohmic contacts were realized on the p^+-layer and on the n^+-substrate respectively.

RESULTS AND MODELING. Typical I-V measured characteristics are presented Figs. 1-2. The diodes without boron diffusion show a distorted I-V curve, especially for large areas (Fig. 1b). This effect is vanished in the case of boron doped (BD) ones. BD diode has a typical *pin* electrical behavior [2]. The 950V maximum experimental breakdown voltage of such punch-through devices is in good agreement with the calculated value V_{PT}=990V [2]. The reverse characteristics depend on temperature with a 0.68eV thermal activation energy (Fig. 2). For estimating the room temperature DC parameters of BD diodes we implemented an extended PSPICE model in an optimal extractor [3]. The model includes low level recombination and diffusion currents, and has been extended with a square law $I_F(V_F)$ dependence at high injection level, specific to the *pin* diodes [2]. As a result, this model allows a very good fit between measured and calculated forward characteristics (Fig. 3). At high forward voltages, the linear variation of the diode's conductance is correctly predicted. For the lower forward voltage range, the best fit to the experimental data can be achieved by extracting the recombination emission coefficient n_r (corresponding to the typical value 2.35). However, imposing the theoretical value n_r=2 leads to an extracted value of the recombination saturation current density J_{or} ($0.8\times10^{-21}A/cm^2$) in excellent agreement with the theoretical one ($10^{-21}A/cm^2$) [2]. Figs. 4-5 show the extracted parameter dependence on the device area. All the extracted currents (the recombination saturation current I_{or} (Fig. 4), the diffusion saturation current I_{od} and the knee current I_K (Fig. 5)) increase linearly with area. This confirms the accuracy of the extended model. On the other hand, the dependencies shown Figs. 4-5, evince the benefic effect of boron diffusion for obtaining predictable large area devices. Therefore the parameter values (J_{od}, J_{or}, J_K) can be used in the design of SiC $p^+v^-n^+$ diodes.



(a)



(b)

Fig. 1 Measured forward characteristics on 6H-SiC diodes: (a) – boron doped; (b) –boron undoped.

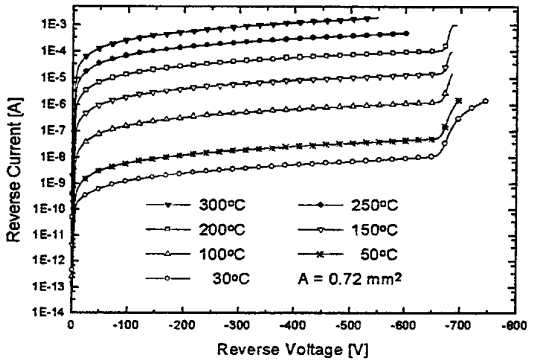


Fig.2 Measured typical reverse characteristics on boron doped 6H-SiC diodes. V_{PT} = 700V at room temperature.

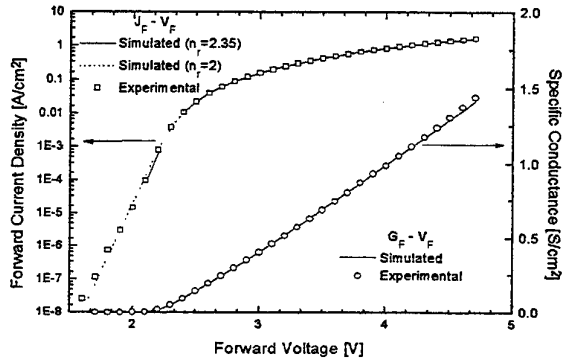
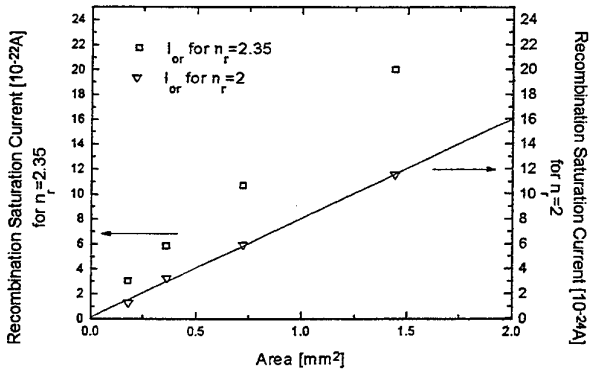
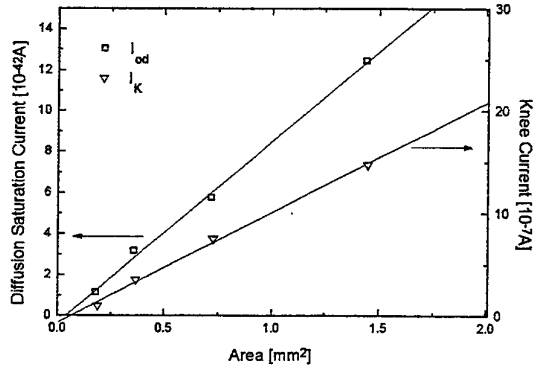


Fig.3 Comparison between simulated J_F-V_F and G_F-V_F curves with extracted parameters and experimental data .



(a)



(b)

Fig. 4 Extracted parameter's dependence on device area: (a) – recombination saturation current deduced for n_r=2.35 and n_r=2 respectively; (b) – diffusion saturation current and knee current.

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THERMAL INJECTION CURRENT IN 3C-SiC pn STRUCTURES

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We present the results of a systematic investigation of the current-voltage (I-V) characteristics of forward biased pn structures based on cubic silicon carbide (3C-SiC). We used n-type crystals with average value of the uncompensated donor concentration N_d-N_a=(0.5-1) 10^{17} cm^{-3} and with area 4-10 mm^2 grown by thermal decomposition of methyl trichlorsilane in hydrogen atmosphere [1]. Preliminary the crystals were ground and polished on the A(111) face and then etched in a NaOH melt (600°C, 5 min). The p-n structures were prepared by Al diffusion. Diffusion was made in He atmosphere at temperatures 1700-1800°C for 1-4 hrs. Contacts to n-region were prepared by consecutive evaporation of titanium and nickel, to p-type by evaporation of aluminum. Mesa-diodes etcheig was done using NaOH, with Al serving as a mask. The diameter of the pn structures was about 130 - 160 μm.

I-V characteristics at forward bias of pn structures fabricated on five different substrates have been measured. Some structures had linear I-V characteristics, others displayed non-linearity. Structures showing a large voltage drop, presumably because of essentially non-ohmic contacts, were excluded from the study. Selected structures had the most pronounced I(V) dependence, of the type $I=I_o \exp(qV/nkT)$. The parameters (I_o, n) were determined. Currents were identified which had close values of n and a large scatter in I_o values. Again, structures were selected which displayed green injection electroluminescence, characteristic of 3C-SiC pn structures [2], and in which the green electroluminescence was most intensive and uniform and could be observed at the lowest currents (in such structures the voltage drop value was usually small).

Among the selection three structures had extremely close I-V characteristics, with n value in the range 1.9-2.2 and the room temperature preexponential factor for current density J_o in the range 10^{-18} - 10^{-17} A/cm^2. For one of these structures I-V characteristics in a temperature range 300-540 K were measured (Fig. 1). It was found that the value of n varied in the range 1.8-

2.1 and the dependence of the preexponential factor on the reciprocal temperature was exponential: $J_o=J_o^* \exp(-E_a= /kT)$, with an activation energy E_a about 1.2 eV.

Since n≈2, the Sah-Noyce-Shockley (SNS) model could be used. In this case, it describes currents due to carrier recombination and generation in the space charge region of a pn junction through a deep level [3]. According to this model the value of E_a was taken (to a first approximation) as half the value of the semiconductor energy gap E_g (2.4 eV for 3C-SiC).

The results of this study were compare with those of earlier investigations [4,5]. It can be presumed that in 3C-SiC pn structures the thermal injection SNS current has been observed for the first time.

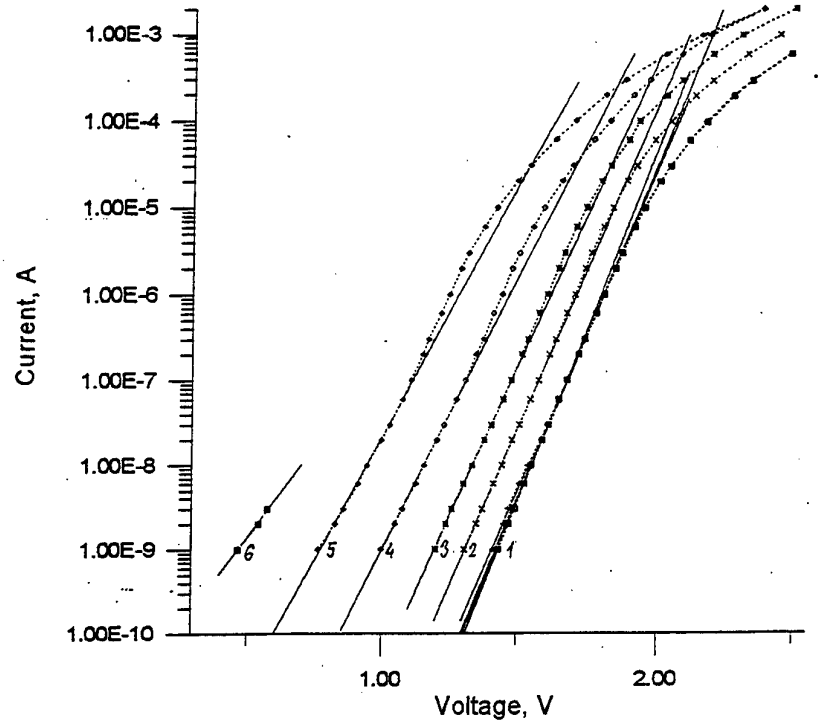

Fig.1. Forward current-voltage characteristics of a 3C-SiC pn structure in the region of weak currents at various temperatures in range 294 (curve 1) - 540 K (curve 6).

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INFLUENCE OF PROTON IRRADIATION ON RECOMBINATION CURRENT IN 6H-SiC pn STRUCTURES

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The effect of proton bombardment on forward current in the range of low currents has been investigated for 6H-SiC pn structures having sharp asymmetric p^+n junctions. Epitaxial layers of p^+- and n-type conductivity were grown by sublimation in an open growth cell [1] on the Si faces of silicon carbide single crystal substrates prepared by the Lely method. The concentration of uncompensated donors in the n-type layer was $N_d-N_a=4\ 10^{16}$ cm^{-3}. The thickness of the n-type layer was about 5 μm, and that of the p^+(Al)-type layer about 1 μm. Contacts to the p^+-layer were made by deposition and annealing of Al-Ti, contacts to the substrate by deposition and annealing of Ni. Mesas of an area ~$7\ 10^{-4}$ cm^2 were formed by reactive ion-plasma etching. The wafer with mesas was cut into 4 parts and structures displaying no excess (leakage) currents at forward bias (current range 1 nA and higher) were selected. The structures were irradiated with 8 MeV protons in MGTs-20 cyclotron with doses $3.6\ 10^{14}$ cm^{-2} (low dose), $1.8\ 10^{15}$ cm^{-2} (medium dose) and $5.4\ 10^{15}$ cm^{-2} (high dose).

The I-V characteristics of the structures to be irradiated were typical of structures prepared by sublimation in an open growth cell. Prior to irradiation the forward current-voltage (I-V) characteristics for current densities $J=10^{-6}$ - 1 A/cm^2 in the temperature range 300-800 K had two portions of thermal injection current. They can be described by formula $J=J_o \exp(qV/nkT)$, where $J_o=J_o^* \exp(-E_a/nkT)$, n is a temperature-independent coefficient, $E_a \approx E_g/n$ is the activation energy and E_g is the band gap. In the lower current range ($J<10^{-3}$ A/cm^2) currents were detected with n=2, J_o(293 K)=$(0.4\text{-}1)10^{-22}$ A/cm^2, $E_a \approx 1.6$ eV and $J_o^* \sim 10^5$ A/cm^2 [2,3]; at higher currents n had a value between 1 and 2. To describe the thermal injection current of the lower exponential portion of the I-V characteristic (n=2), we have used a model suggested for currents due to recombination in the space-charge region of a pn junction through a single-level deep center [4]. The lifetime of the nonequilibrium carriers in the space charge region for deep-level recombination in a steady-state regime is a parameter

of the model [4]. The lifetime was found to be about 3 10^{-10} s at room temperature and N_d-N_a=(0.4-1)10^{17} cm^{-3} and increased with temperature [2,3].

After irradiation with the low dose (3.6 10^{14} cm^{-2}), the current at fixed voltage increased, so that the lower portion of the I-V characteristics shifted upwards and the exponential portion with n=2 became dominant over the entire current range. Annealing the pn structures at temperatures 300-800 K (for 1-1.5 hrs) had no effect on the current value. The parameters of the current were as follows: n=2, J_o(293 K)=(3-5)10^{-21} A/cm^2, E_a≈1.6 eV and J_o^*~10^7 A/cm^2. The medium and especially high dose of irradiation increased considerably the voltage drop across the structure and, even at the lowest currents, the exponential portion the of I-V characteristic could not be observed. Annealing the pn structure at a temperature 500 K or higher after the medium irradiation dose restored the exponential portion of the I-V characteristic. The parameters of this exponential portion at room temperature were approximately the same as the one after the low irradiation dose and were also not affected by temperature treatment (at 500-800 K).

In terms of the model of Ref.4, the parallel upward shift of the I-V characteristics after irradiation is the evidence of a change in the carrier lifetime assuming that the band gap and doping level in irradiated pn structures remain the same or change but a little. Thus we can suggest that even the low irradiation dose (3.6 10^{14} cm^{-2}) affected (decreased) the lifetime of nonequilibrium carriers for deep-level recombination in the space charge region by up to 1.5 - 2 orders of magnitude. The medium irradiation dose of 1.8 10^{15} cm^{-2}, and anneal in the range 300-800 K had no effect on the lifetime. A preliminary study of the influence of the electron irradiation on the thermal injection current in 6H-SiC pn structures showed that electron irradiation caused qualitatively the same effects as the proton irradiation. On the contrary, neutron irradiation caused transformation of the forward current from thermal injection current to thermally assisted tunnel current [5].

This work was supported in part by Arizona University (USA) and Schneider Electric (France).

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NON-ISOTHERMAL 2D DEVICE MODELLING OF SiC MESFETs

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Over the past few years, many advances have been made in SiC devices, especially field effect transistors with moderate frequency (1 to 10 GHz) and a few Watts of output power. For these applications, SiC offers several highly desirable qualities: A high breakdown voltage, a high saturation velocity, good high temperature characteristics as well as a thermal conductivity comparable those of a metal (at least at 300 K). In order to take full advantage of these qualities though, it is necessary to apply relatively high voltages to the device. This in turn produces a significant amount of heat, which must somehow be dissipated from the device. Particularly in the case of 3C SiC grown on Si substrates in order to save the very high cost of SiC substrates (and be able to use the much larger Si wafers), the device performance may suffer significantly from this self heating [1].

The in house 2D device simulator PROSA [2], is used to simulate SiC MESFET structures both with and without self heating. The necessary non-isothermal semiconductor models are based on various published data, and hopefully give a reasonable indication of how the various material parameters behave at temperatures above 300 K.

3C SiC MESFET structures with various active layer doping and size are simulated and compared. Variations in the thickness of the underlying substrate are considered (for both Si and 6H SiC substrates), as well as the effects of variations in the quality of the ohmic contacts. Considerable performance degradation can result from self heating, depending on the configuration used, especially for Si Substrates. The results of similar simulations done on 6H and 4H SiC MESFETs (on SiC substrates) are presented as well, although here the performance degradation is far less significant due to the better thermal conductivity of the substrates.

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LARGE AREA SILICON CARBIDE DEVICES FABRICATED ON SiC WAFERS WITH REDUCED MICROPYPE DENSITY

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High defect density in commercially available silicon carbide substrates is one of the main obstacles limiting the size of SiC devices. As a result, the area of SiC devices usually does not exceed 1 mm^2 [1]. Forward current of bipolar SiC devices, being proportional to the device area, is less than 10 A at forward voltage drop of 4 V [2]. In order to fabricate high-power SiC devices, operating at currents of 100 A and higher, the device area must exceed 10 mm^2.

Recently, TDI, Inc. have reported on the fabrication of silicon carbide epitaxial wafers with reduced micropipe density [3]. The best R&D wafers, both 6H and 4H polytypes, have no micropipes and dislocation density has also been reduced [4]. These wafers were proposed to be used as substrates for SiC high-power devices [5].

In this paper, we report on characteristics of SiC devices (Schottky and pn diodes) fabricated on SiC wafers with reduced micropipe density. Average micropipe density in these wafers ranged from 0 to 10 cm^{-2}. The concentration Nd-Na in the wafers with reduced micropipe density was in the range of 10^{18} – 10^{19} cm^{-3}. Device structures were fabricated on the (0001)Si face of the wafers. The missorientation angle was 3.5 degrees and 8 degrees for 6H-SiC and 4H-SiC wafers, respectively. Device structures were grown by sublimation sandwich method and liquid phase epitaxy (LPE) [6].

Sublimation growth was carried out in a vacuum at 2000°C. The growth rate was 1.5 micron per hour. Liquid phase epitaxial growth was performed from Si melt at 1600°C. The growth rate was approximately 0.3 microns per hour. Crystal structure and defect density in the grown epitaxial layers were studied by chemical etching in molten KOH at 500°C. Results of material characterization will be presented.

Schottky barriers were fabricated on 6H-SiC epitaxial structure grown by sublimation. Concentration Nd–Na in sublimation epitaxial layer was about $1x10^{16}$ cm^{-3}. The layer thickness was about 3 microns. The barriers were made by vacuum evaporation of Ni on as grown SiC surfaces. The barrier area ranged from 0.3 to 6 mm^2. Preliminary investigation of the Schottky barrier's characteristics performed without any edge termination precautions gave us the following results. Small area Schottky diodes had sharp breakdown at reverse voltage of 250 V. This voltage value probably corresponds to punch-through of 3 microns thick low doped layers grown by sublimation. The Schottky barrier having 6 mm^2 area had breakdown voltage of 150 V (Fig. 1). To the best of our knowledge, this is the largest SiC device fabricated to date.

Pn structures were grown by LPE. Undoped 4H-SiC layers with concentration Nd-Na ranged from $8x10^{16}$ to $3x10^{17}$ cm^{-3} were deposited on 4H-SiC wafers with reduced micropipe density. Aluminum doping was employed to grow p-type layers on the top of the undoped layers in separate epitaxial runs.

Mesa diodes were fabricated using reactive ion etching technique. Detailed device characteristics will be reported.

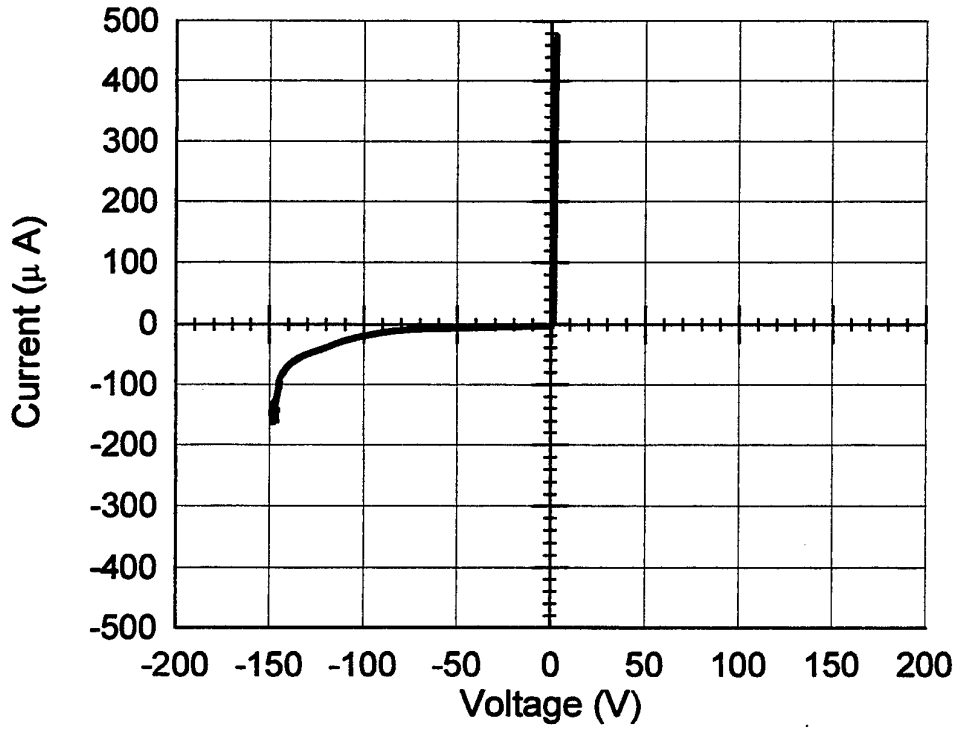

Figure 1. Current-voltage characteristics of 6 mm^2 Ni/6H-SiC Schottky barrier fabricated on 4H-SiC epitaxial layer grown by sublimation on 4H-SiC epitaxial wafer with reduced micropipe density.

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SIC SCHOTTKY DIODES WITH CATALYTIC GATE METALS USED AS GAS SENSORS FOR EXHAUST GASES

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Silicon carbide Schottky diodes with catalytic metal gates, e. g. platinum and iridium, changes IV characteristics due to a change in the ambient and are thus used as gas sensors [1,2]. The IV curve of thick metal gate diodes (>100 nm) are displaced to lower voltages when the ambient changes from an excess of oxidizing gases like oxygen and nitric oxide to an excess of reducing gases like hydrogen and hydrocarbons, that is, the ambients found in petrol engine exhaust. Thin porous metal gate Schottky diodes are sensitive to changes in reducing gases even if the overall ambient contains excess oxygen, like in diesel exhaust or flue gases. It seems to be necessary to have an insulator between the SiC and the catalytic metal to have a proper gas sensing behaviour, see Fig.1. Ozone cleaning of the SiC surface before the deposition of the catalytic metal seems to give an appropriate insulator.

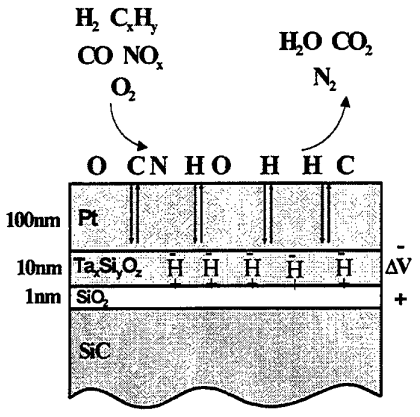

Fig. 1. Schematic drawing of Schottky diodes with a native oxide.

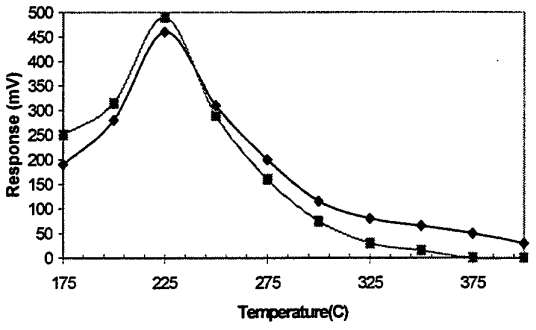

Fig. 2. The response of two Schottky diodes with 20 nm Pt gates to 30 second pulses of 250 ppm ammonia in 20 % oxygen in nitrogen. The voltage shift at a constant current, 0.5 mA, of the IV curve is defined as the gas response. Positive response means a shift from higher to lower voltage.

Schottky diodes with thick platinum gates and an adhesion layer of $TaSi_x$ between the metal and SiC, see Fig. 1, showed a very fast response to a change between reducing and oxidizing ambient in car exhaust [3]. Cylinder specific control has been demonstrated for this kind of sensors [4]. The sensing mechanism is here suggested to originate from hydrogen atoms, which are released from gas molecules that dissociate on the metal surface. The hydrogen atoms give rise to an electrically polarised layer at the metal insulator interface, see Fig. 1. The polarised layer shifts the IV characteristics of the Schottky diode towards lower voltages.

Schottky diodes with thin porous gates of platinum and iridium show a response to ammonia in synthetic air with a maximum response at 225°C, see Fig. 2. Reducing gases like ammonia and hydrogen shift the IV characteristics of the diodes mostly towards lower voltages as expected, but sometimes towards higher voltages. The mechanism for the gas detection of the thin film sensors will therefore be studied in detail.

The sensors with porous metal gates have been operated at around 400°C for quite long in the laboratory, but they fail rather quickly at temperatures around 600°C. Thick film sensors based on Schottky diodes fail at about 800°C. An understanding of the failure mechanism is of crucial importance for the possibility to create long term stable high temperature sensors.

We have identified two reasons for why the sensors fail, they become ohmic or they get a very high threshold voltage, more than 10 V. The reason for an ohmic behaviour is supposed to be mixing of metal and SiC at the interface. This has to be avoided for high temperature operation of Schottky diode sensors. There is a possibility that a tunneling layer of some diffusion preventing material can be used. For the high resistive sensors it is not clear whether they also fail due to mixing of the metal and SiC, or if the catalytic metal is oxidized, or if there is a failure between the gate and the contact pad. This will be studied by electrical measurements as well as by auger electron spectroscopy analysis.

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ELECTRICAL CHARACTERIZATION OF A PLATELET CUT FROM p-6H-SiC BULK CRYSTAL USING Au SCHOTTKY DIODES

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Schottky contacts have important effects on a variety of electronic devices. Besides study of Schottky contacts allows to determine some material parameters and to estimate for the material to be suitable for device applications.

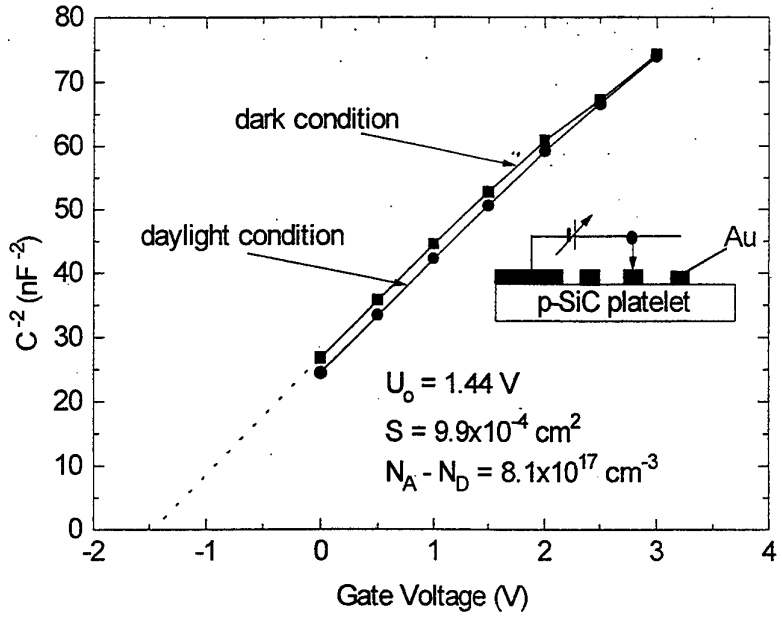

Figure 1. Typical C-V characteristics of an Au Schottky contact to p-6H-SiC(0001).

6H-SiC(0001) platelets cut from aluminum-doped p-type 6H-SiC bulk crystal were used for Au Shottky contact depositions and meaurements. After polishing, the substrates were cleaned using organic solutions, HF/water (1:10) and DI water before metal deposition. Au circular Shottky contacts (355 mm in diameter) together with a large Au contact were deposited

by thermal evaporation in vacuum through a mask. The I-V and C-V measurements of the as-deposited samples were taken on a probe station. I-V characteristcs were measured at room temperature and 470 K. The frequency used in room temperature C-V measurement was 1 kHz.

Some parameters of grown p-6H-SiC material were extracted from C-V measurements. Figure 1 shows typical C-V characteristics of an Au Schottky contact measured under dark and daylight conditions. The C^{-2} - V plots show good linearity, resulting in the voltage axis intercept is 1.44 V for dark condition. Under daylight, the capacitance slightly increased leading to some decrease in voltage intercept value. We have explained this effect by the presence of deep level impurities in our p-type material (an additional ionization of these impurities near SCR edge takes place under illumination).

The slopes of C^{-2}-V plots measured on different contacts provided us with distribution of N_A - N_D concentration over the platelet's surface (see Figure 2). As it seen, the average N_A - N_D is of about 7.5×10^{17} cm^{-3} while the non-uniformity in acceptor density does not exceed 20 % (there is slight decrease of N_A - N_D away from the platelet's center). We have attributed such behaviour in Al-doping to the proper temperature gradient existing in the growth chamber.

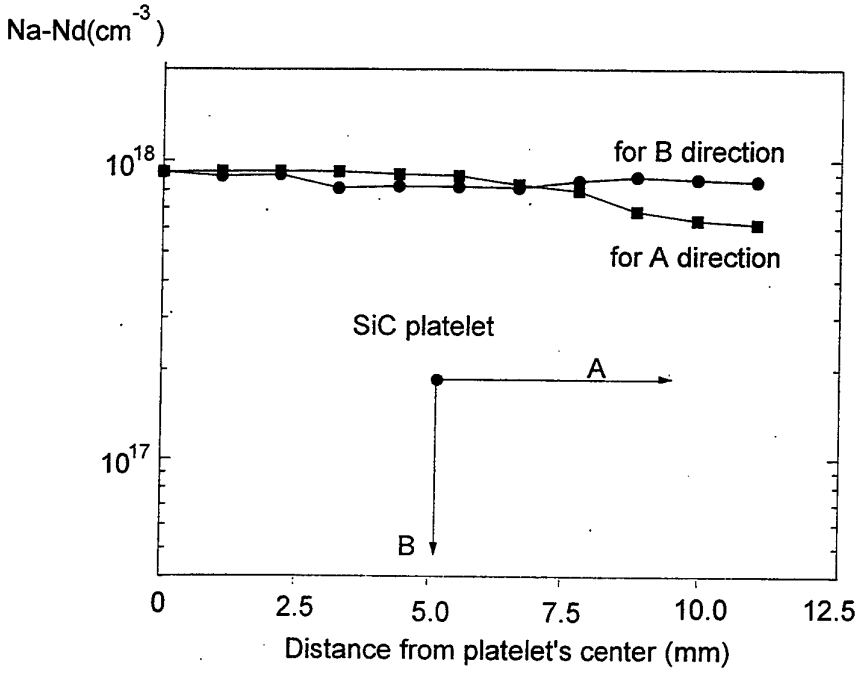

Figure 2. Distribution of N_A - N_D density over the platelet's surface for two perpendicular directions.

The as-deposited Au contacts show rectifying character with a factor $I_f/I_r \approx 1000$, i.e. approximately the same value as for Shottky contacts formed on commercially available Cree's substrates of n-type conductivity [***Y.G.Zhang et all. Characterization of Schottky contacts on n-type 6H-SiC. - In "Silicon Carbide and Related Materials 1995", ed. by S.Nakashima, H.Matsunami, S.Yoshida, and H.Harima (Inst. Phys. Conf. Ser. No 142; Inst. Phys. Publishing, Bristol and Philadelphia), p. 665-668 (1996).***]. Figure 3 presents the I-V characteristic measured at room temperature. As it seen the forward characteristic exhibits rather power than exponential I_f versus V_f.

STUDIES OF THE EFFECT OF PROTON IRRADIATION OF 6H SIC PN JUNCTIONS PROPERTIES.

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In the present paper influence of proton irradiation on current-voltage characteristics, Nd-Na value and parameters of deep centres in 6H SiC pn structures (Nd-Na = 4 10^{16} cm^{-3}) grown by sublimation epitaxy [1, 2] has been studied. Irradiation with 8 MeV protons was performed on a MGTs-20 cyclotron at a doses: $3.6 \cdot 10^{14}$ cm^{-2} (1^{st} dose), $1.8 \cdot 10^{15}$ cm^{-2} (2^{nd}) and $5.4 \cdot 10^{15}$ cm^{-2} (3^{rd}).

Prior to irradiation structures exhibited standard I-V characteristics with weak leakage currents. After first irradiation the average series resistance of the structures presumably increased somewhat. After a second, and especially third irradiation dose, the forward current decreased drastically (by orders of magnitude) (Fig. 1); the effect of irradiation on the reverse current is not so dramatic.

DLTS spectra in the temperature interval 300-700 K, i-DLTS spectra at 77-350 K and C-U characteristics were registered for unirradiated samples, samples which received first irradiation dose and also samples which received first or second irradiation dose and were then annealed at 500°C. Studies of C-U characteristics have shown that increasing the irradiation dose makes higher the degree of compensation of the base layer. In addition, after a layer receives the first irradiation dose and is then annealed, the concentration of uncompensated impurity in the base was equal to that in a sample not subjected to irradiation.

Investigations of DLTS and i-DLTS spectra have shown that irradiation increases the concentrations of the R centre and Z1/Z2 centre, which was previously observed in 6H SiC layers grown by the CVD method [3]. In addition it was found that upon irradiation the concentration of the D centre increases (see Table) and a great number of deep centres appears in the lower half of the forbidden gap.

In the present work it was established that irradiation with protons with doses exceeding $5.4 \cdot 10^{15}$ cm^{-2} results in the formation of high resistive 6H SiC layers whose resistance remains practically unchanged after annealing at a temperature of 500°C. This result can be used in silicon carbide device technology.

Also is very interesting increasing concentration of R-centre in sublimation grown SiC epilayers under proton irradiation. Because in this type of epilayers this levels is main centre of radiation-free recombination [4], and this results shows a way for lifetime control in SiC devices.

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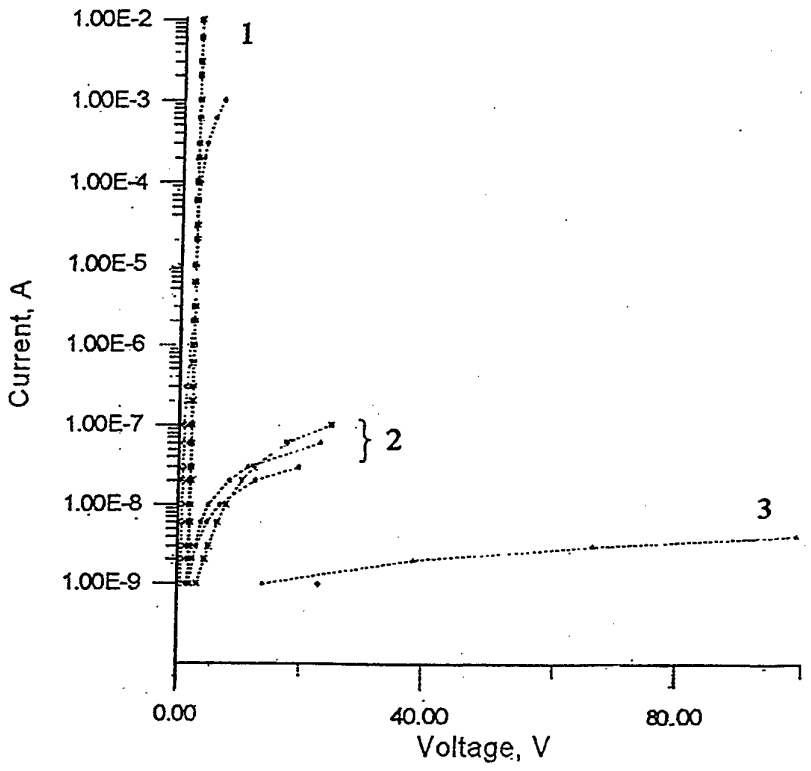
Table . Concentration of the R, Z1/Z2 and D deep centers and Nd-Na value in the samle after different stages of irradiation and anneling.

Sample	Nd-Na, cm^{-3}	Concentration of deep centers, cm^{-3}		
		R	Z1/Z2	D
unirradiated	$4.2 \cdot 10^{16}$	—	$1.5 \cdot 10^{15}$	—
1-st dose	$3.6 \cdot 10^{16}$	$3.8 \cdot 10^{15}$	$2 \cdot 10^{15}$	—
first dose and annealing at 500°C	$4.1 \cdot 10^{16}$	$3.8 \cdot 10^{15}$	$4 \cdot 10^{15}$	—
second dose and annealing at 500°C	$2.7 \cdot 10^{16}$	$9 \cdot 10^{15}$	$5 \cdot 10^{15}$	$5 \cdot 10^{15}$



Forward current-voltage characteristics of different pn structures after 1,2 and 3 doses of irradiation, respectively.

A STUDY ABOUT THE WET OXIDATION OF CRYSTALLINE AND ION AMORPHIZED 6H-SiC

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The oxidation rate of ion amorphized SiC wafers is substantially higher than that of on-axis Si terminated 6H-SiC wafers[1]. In the aim to produce LOCOS structures on the top of SiC wafers in ref.[2] the exploitation of such a difference is proposed. The SiC amorphization by ion implantation produces a surface swelling that was quantitatively studied in ref. [3]. The present study investigated the effect of such a swelling on the planarity and on the oxide film structure when SiC wafers with selected amorphized area are submitted to a wet oxidation process.

<0001>, n-type, on-axis and Si terminated 6H-SiC wafers were amorphized on half an area by implanting Ar^+ ions with energy, average beam current and fluence values equal to 170 KeV, 2 mA and 1.1 10^{15} cm^{-2}, respectively. After that the wafers were processed in a steam oxygen atmosphere at 1100 C for different times, the 240, 300 and 360 min samples will be shown.

The thickness of the amorphized layers were measured by the light ion Rutherford Back-Scattering (RBS)- channeling technique. The step height at the border between crystalline and amorphized areas before the oxidation, after the oxidation and after the etching of the oxide films were measured by a Technor Alfa-Step-200 stylus profilometer.

Figure 1 shows the <0001> aligned and random RBS spectra of the as implanted sample obtained by a 2 MeV, 10 nA He^+ beam backscattered at an angle equal to 170°. The edges of the Si and C signals are indicated by arrows. The overlap between the two spectra in the near surface region guarantees that the

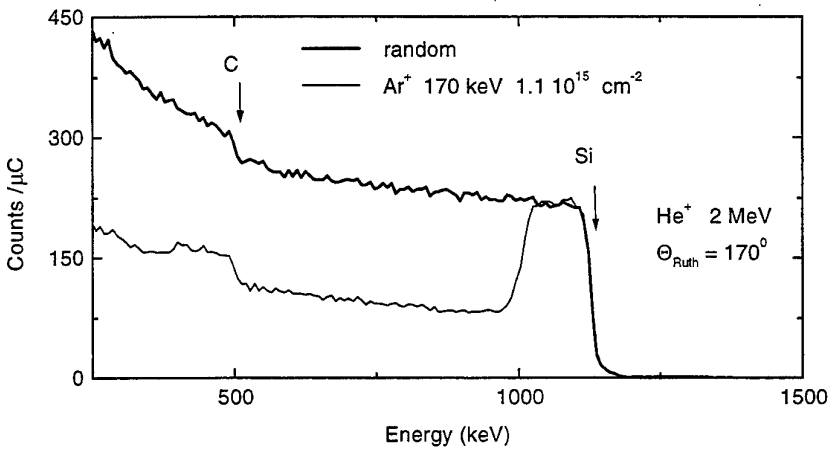

Fig. 1

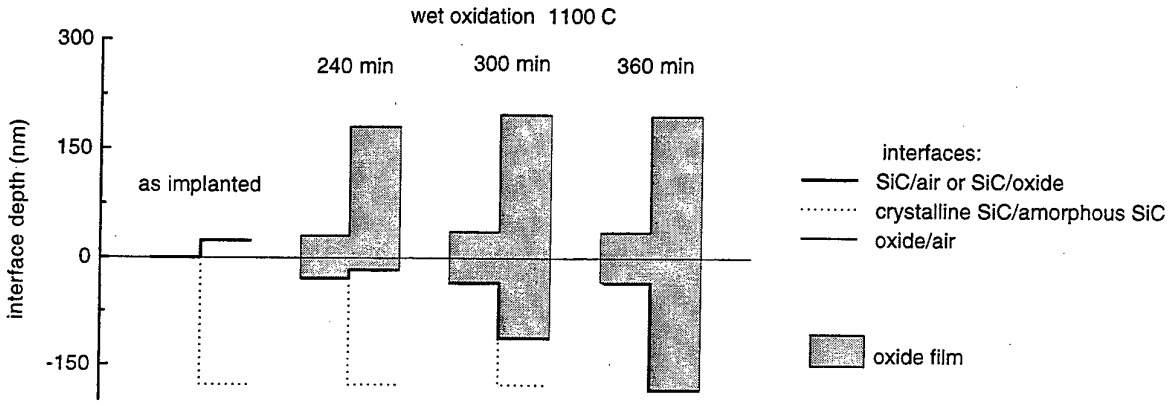

Fig. 2

crystal is amorphized across the whole implanted thickness. This thickness is equal to $(1.72 \pm 0.05)\ 10^{18}$ at cm^{-2} if measured by RBS units on the Si signal. Such a thickness corresponds to 180 nm of crystalline SiC, using a mass density equal to 3.2 $gr \cdot cm^{-3}$ for the 6H politype, and to 200 nm of amorphous SiC if the swelling factor measured in the case of Al^+ implantation [3] is assumed. The step height at the border between the perfect and the amorphous crystal was measured equal to (23 ± 5) nm. The agreement between the evaluated and the experimental data shows that the swelling phenomenon due to the ion damage in 6H-SiC is linked to the amount of damage and is independent on the implanted ion species.

A schema of the sample surface cross section topographies at the border between virgin and implanted area both for the as implanted and for the oxidized samples is shown in Fig. 2. The relative positions of the interfaces between SiC and air, SiC and oxide, oxide and air were derived from the step height measurements after the implantation, the oxidation and the oxide etch processes. The interfaces between crystal and amorphous phases was drawn in agreement with the RBS and step height data of the as implanted sample. The position of such an interface was assumed unchanged during any thermal oxidation process because the following experimental result: the swelling value of an implanted sample remained unchanged after a 1 h thermal treatment at 1100 C in N_2 flux, in spite of the quite important optical change of the implanted area. Such a result differs from what expected taking into account the results of ref. [4]. The reasons of such a difference will be not investigated in this paper.

Taking into account the thickness values of the oxide films formed on the virgin and damaged SiC and the fact that one unit length of oxide consumes 0.46 unit length of crystalline 6H-SiC and 0.52 unit length of amorphous SiC, the evaluation of the relative position of the oxide/bulk interfaces is quite different from the experimental data shown in Fig. 2. The diffusion mechanisms as well as a different dissolution mechanisms of the crystalline phase with respect to the amorphous one might be responsible of that.

Looking at the oxide structures the 300 min sample reproduces a case already shown in the literature [2], but the 240 and the 300 min samples are new configurations. In fact, for the 240 min treatment the SiC/oxide interface at the border between damaged and undamaged regions has a shape similar to that of the as implanted case; the step value is different. While, during the 360 min treatment all the amorphized thickness was consumed and an oxide film with a sharp thickness change on the top of a crystalline bulk SiC was produced. These two structures indicates that a flat interface with the bulk SiC can be obtained and that a single step LOCOS technology can be proposed for SiC once the implantation and the thermal treatment steps will be correctly calibrated. The trimming of the oxide thickness proposed in ref. [2] might be avoided.

The conclusion of this study is: in spite of the fact that the basic mechanism of the oxide growth on virgin and ion amorphized 6H-SiC requires further investigations, the selective area ion damage at the surface of SiC wafers can be usefully proposed for the application of the LOCOS technology to SiC.

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GAMMA-RAY IRRADIATION EFFECTS ON 6H-SiC MOSFET

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Because Silicon carbide, SiC, has a strong radiation tolerance[1] in addition to excellent thermal and electrical properties[2], it is expected that SiC will be applied to not only high-power and high-frequency devices but also electronic devices used in ionizing radiation fields. For the application of SiC to radiation resistant devices, it is very important to understand the response of these devices to radiation. In this study, we fabricated enhancement-type *n*-channel metal-oxide-semiconductor field effect transistors, MOSFETs, on 6H-SiC and investigated the influence of γ-ray irradiation on the gate oxide of these.

Figure 1 shows subthreshold-current curves for 6H-MOSFET irradiated with γ-rays. The MOSFETs were fabricated on p-type 6H-SiC epitaxial films (~4μm) grown on p-type 6H-SiC substrates (Cree Research Inc.). The net acceptor concentration of the epitaxial films was $3x10^{15}$ /cm^3. Source and drain were formed by nitrogen ion implantation at 1200 °C without subsequent thermal annealing. Gate oxide with a thickness of 20 nm was formed by pyrogenic oxidation at 1100 °C. Gamma-ray irradiation to the MOSFETs was performed up to ~70 kGy(SiO_2) at a rate of 8.8kGy/h at room temperature. During the irradiation, no electrical voltage was applied to gate, or between source and drain. The subthreshold-current curves are shifted toward lower gate voltage by the irradiation. According to McWhorter *et al.*[3], the shift of threshold voltage, ΔV_{th}, by irradiation is attributed to the generation of interface traps and oxide-trapped charge ($\Delta V_{th} = \Delta V_{it}+\Delta V_{ox}$, where ΔV_{it} and ΔV_{ox} are voltage shifts due to the generation of interface traps and oxide-trapped charge, respectively). Furthermore, ΔV_{ox} is represented by the voltage shift at midgap condition, ΔV_{mid} (i.e., $\Delta V_{ox} = \Delta V_{mid}$). As the result, ΔV_{it} can be determined from the relation of $\Delta V_{it} = \Delta V_{th} - \Delta V_{ox}$. Figure 2 shows absorbed dose dependence of ΔV_{th}, ΔV_{it} and ΔV_{ox} for 6H-SiC MOSFET. The threshold voltage was determined from the intersection between V_G-axis and the line extrapolated from the curve of the square root of drian current versus gate voltage. The midgap current was calculated from the formula of subthreshold current as a function of surface band bending[4]. Using obtained midgap current, the midgap voltage was determined from the subthreshold-current curve. The procedure of this analysis has been reported in ref. 3 in detail. The result of ΔV_{ox} is attributed to the fact that positive charge is generated in gate oxide by irradiation. The result of ΔV_{it} suggests that the acceptor traps are generated in the upper half of the bandgap by irradiation.

We have also studied radiation-induced interface traps and oxide-trapped charge in the gate oxide from *C-V* measurements of 6H-SiC MOS capacitors. Comparing the result for MOS capacitors with those of MOSFETs, we go on to discuss radiation-induced interface traps and oxide-trapped charge in MOSFET in more detail.

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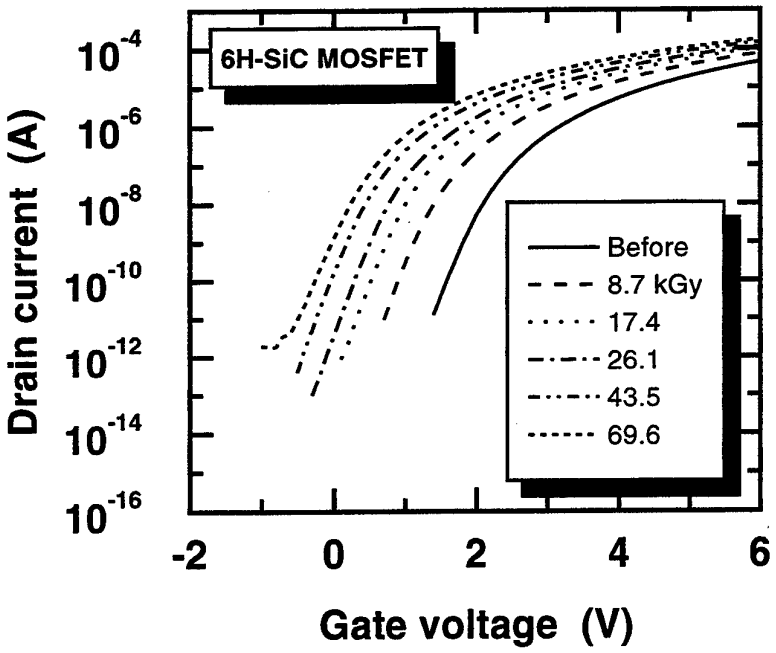

Fig. 1 Subthreshold current curves for 6H-SiC MOSFET (gate length: 10μm) irradiated with γ-rays.

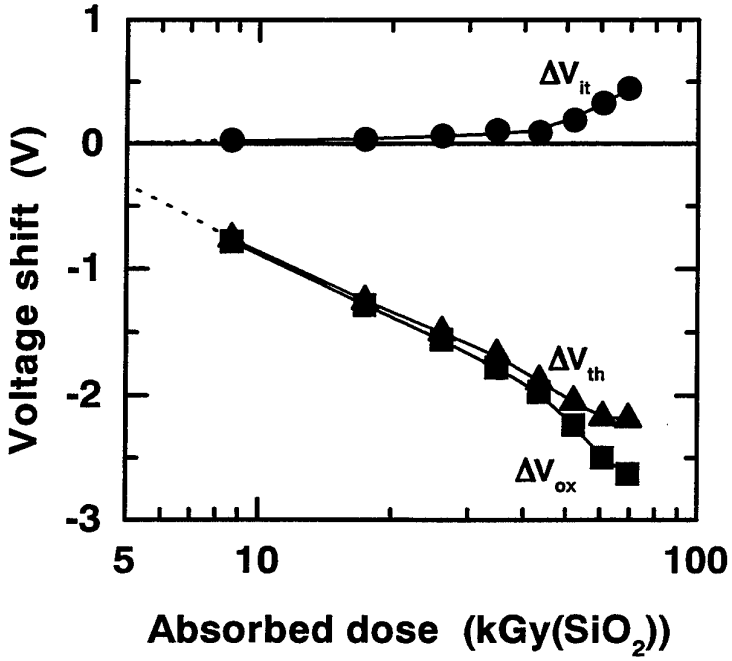

Fig. 2 Absorbed dose dependence of ΔV_{th}, ΔV_{it} and ΔV_{ox} for 6H-SiC MOSFET.

NONSTOICHIOMETRIC OXIDATION OF 6H SILICON CARBIDE WITH CO AND CO_2

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The understanding of the oxidation process is important for the promotion of the quality of the SiC/SiO_2 interface in a SiC-based MOS device. Compared to the Si/SiO_2 interface the density of states at the SiC/SiO_2 interface is by at least one order of magnitude higher [1]. From their investigations of the SiC/SiO_2 interface Afanas'ev et al. [1] have inferred a model suggesting that the enhanced interface state density is due to carbon clusters at the SiC/SiO_2 interface. These clusters are supposed to be originated in residual carbon from the reaction of O_2 with SiC. Most of the carbon of the oxidation reaction of SiC diffuses out of the oxide in form of CO or CO_2 [2]. In the present work we influenced the stoichiometry of the oxidation process of SiC by using CO and CO_2 for the oxidation.

We used n-type 6H-SiC with an n-type epitaxial layer with a net donor concentration of $3x10^{16}$ cm^{-3}. The oxidations were performed at 1120°C in dry atmosphere for 24h with a post oxidation annealing step in Ar for 1h at the same temperature. As process gases we used CO and CO_2 with Ar as carrier gas in the ratio of one to one. For reference measurements we conducted oxidations in dry O_2 (reference for interface state density) and Ar (reference to determine the oxidation rate due to the residual oxygen in the furnace). For electrical measurements we thermally evaporated gold contacts (Ø=0.57 mm). The SiC/SiO_2 interfaces were characterized by capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) measurements .

Figs. 1 to 4 show the C-V and G-V characteristic of samples oxidized with O_2, CO_2, CO and Ar, respectively. The oxide thicknesses as calculated from the capacitance in accumulation of the oxides are 123±6nm (O_2), 29±3nm (CO_2), 7±1 (CO) and 24±2nm (Ar), respectively. The oxide thickness of the CO_2 oxidation is comparable to the oxide thickness of a reference oxidation in Ar (c.f. Figs. 2 and 4). This can be explained by the fact that the reaction $CO_2 \rightarrow CO + ½O_2$ supplies almost no additional O_2 to the system, since the equilibrium is strongly shifted to CO_2 (the ratio CO/CO_2 is 0.03 % at 1206°C). Therefore we suppose that the oxidation is in both cases, for CO_2 and for Ar, determined by the residual oxygen in the furnace. The oxidation with CO results in an even lower oxide thickness. This is probably due to the strongly exothermal reaction $CO + ½O_2 \rightarrow CO_2$ (with the enthalpy ΔH=-67.635 kcal/mol), wherefore CO is gettering the residual oxygen in the oxidation furnace. The I-V characteristics (not shown here) of the oxidations with CO and CO_2 reveal an increased current of I≈1nA at 5V in accumulation in contrary to the reference oxidations with O_2 and Ar (I≈1pA at 5V) meaning that the oxidation with carbon containing oxidants leads to a „leaky" oxide.

Calculating the interface state density from the conductance peak at 1kHz (also shown in the respective Figs. 1 to 4) we obtain the following results in the energy range from E_C to E_C-(0.4±0.1)eV: $D_{it}(O_2)=1x10^{11}cm^{-2}eV^{-1}$, $D_{it}(CO_2)=1.6x10^{12}cm^{-2}eV^{-1}$, $D_{it}(CO)=1.4x10^{12}cm^{-2}eV^{-1}$ and $D_{it}(Ar)=6.9x10^{11}cm^{-2}eV^{-1}$.

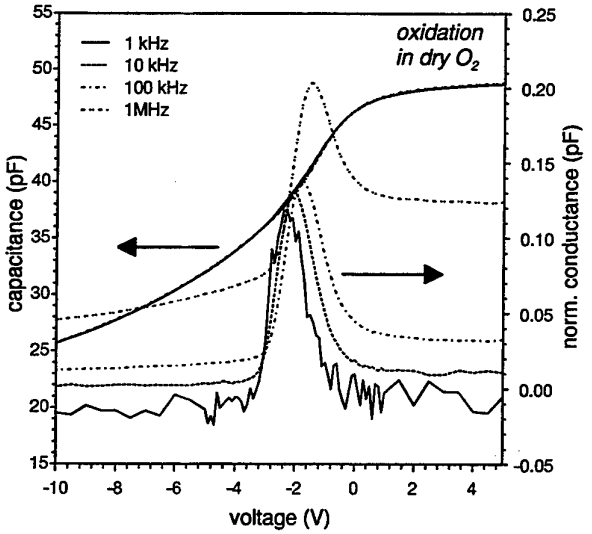

Fig. 1 C-V and G-V characteristics of SiC/SiO_2 MOS structures prepared by oxidation in dry O_2

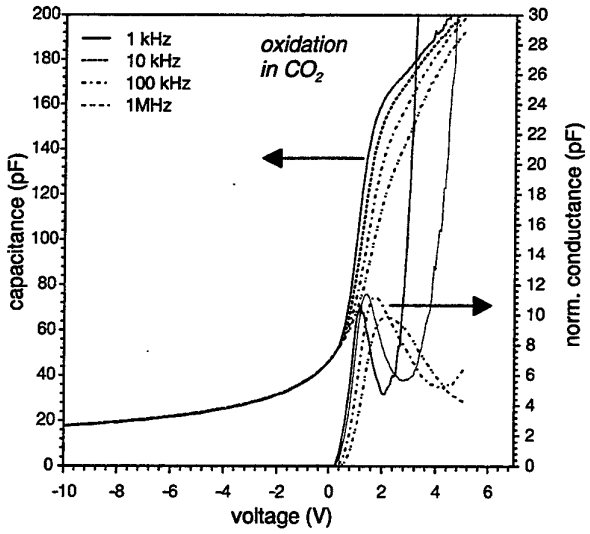

Fig. 2 C-V and G-V characteristics of SiC/SiO_2 MOS structures prepared by oxidation in dry CO_2

The reference oxidation with O_2 in dry atmosphere shows the lowest interface state density. The oxides grown with carbon containing oxidants reveal interface state densities which are higher by approximately one order of magnitude as compared to the O_2 reference oxidation. An intermediate value of D_{it} is found for the Ar reference oxidation. Three different oxidation conditions can be distinguished:

- oxidation in dry O_2: the oxygen surplus leads to a D_{it} which corresponds to the values found in [1].
- oxidation in CO/CO_2: the surplus of carbon containing species shifts the chemical equilibrium at the interface towards the formation of C-C bonds. This is in accordance with the "carbon cluster model" of [1]. In addition the carbon containing species may prevent the outdiffusion of CO and CO_2, respectively.
- oxidation in Ar: The lack of oxygen and of an additional supply of carbon species in the oxidation ambient results in an intermediate position of the equilibrium and, therefore, leads to a higher D_{it} as compared to the reference O_2 oxidation, but to a lower D_{it} as compared to the CO/CO_2 oxidations.

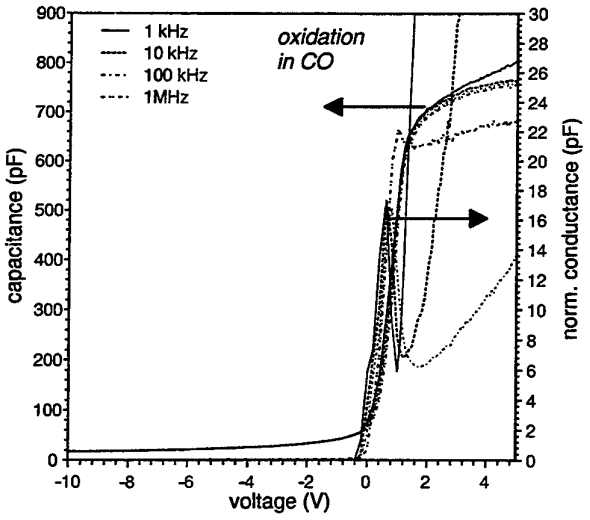

Fig. 4 C-V and G-V characteristics of SiC/SiO_2 MOS structures prepared by oxidation in dry CO

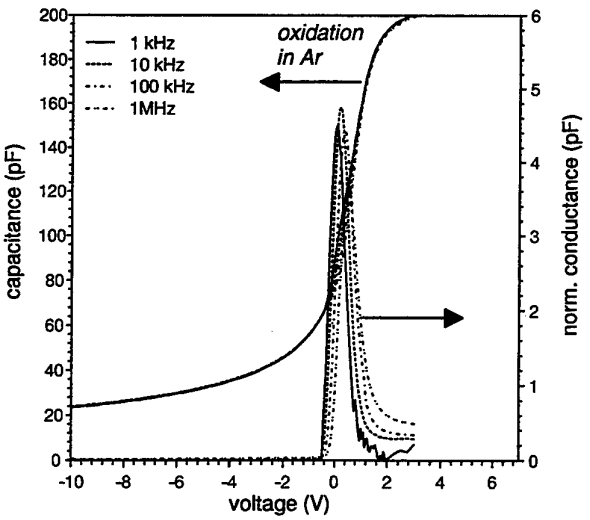

Fig. 3 C-V and G-V characteristics of SiC/SiO_2 MOS structures prepared by oxidation in dry Ar

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LONG-TIME CONSTANT-CAPACITANCE DLTS INVESTIGATIONS OF 6H SiC/MOS STRUCTURES: COMPARISON OF DRY AND WET OXIDATION

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The electronic properties of SiC/SiO_2 interfaces are of substantial interest for the performance of SiC-based MOS devices. The interface state density D_{it} at MOS structures can be characterized by a number of electrical methods. In order to determine energy states in the middle of the SiC band gap either high sample temperatures, which may degrade the oxide quality or extremely long time constants, which frequently are limited by the measurement equipment, are required.

It is the aim of this paper to introduce a modified Constant-Capacitance Deep Level Transient Spectroscopy (CC-DLTS) method, which allows the use of remarkable long time constants (in practice up to 1h). This method has been employed to monitor D_{it} of MOS structures fabricated by dry or wet oxidation. The differences in D_{it} are discussed in the framework of the "Carbon-Cluster-Model" [1].

MOS structures were prepared on n-type and p-type 6H-SiC epilayers with net concentrations N_N-N_{Comp}=$2x10^{16}cm^{-3}$ and N_{Al}-N_{Comp}=$1x10^{16}cm^{-3}$, respectively. The samples were subjected to a pre-oxidation surface cleaning described elsewhere [2]. The oxidation was conducted either dry or wet at 1120 °C for 24h (d_{oxide}=120nm) and 15h (d_{oxide}=90nm), respectively. The samples were subsequently exposed to a post oxidation anneal in Ar at 1120 °C for 1 h. Gold contacts (∅ = 0.5 mm) were prepared by thermal evaporation.

The MOS capacitors were investigated

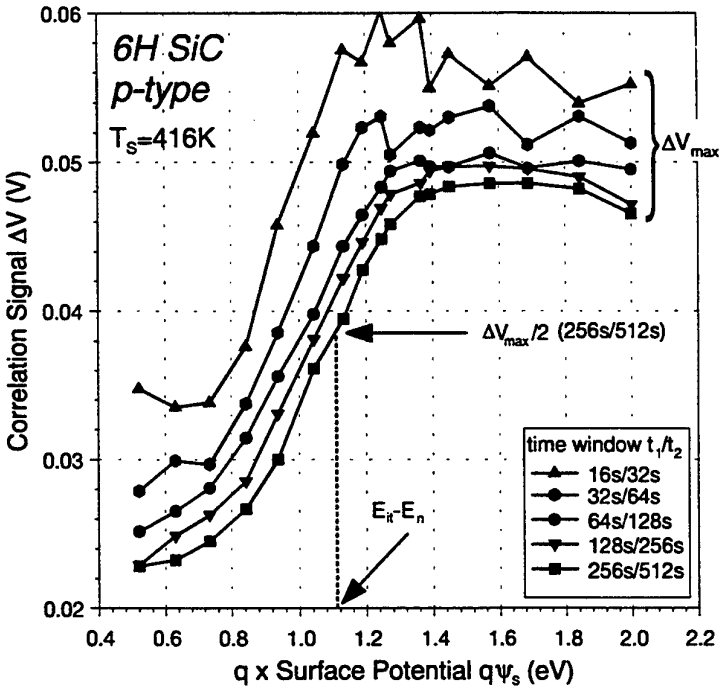

Fig. 1 Correlation signal ΔV as a function of the product of elementary charge q and surface potential ψ_s for different rate windows taken on a p-type 6H SiC MOS structure. The product $q\psi_s(t_1/t_2)$ at half maximum voltage $\Delta V_{max}(t_1/t_2)/2$ determines the energy position $E_{it}(t_1/t_2)$ of the corresponding interface state density $D_{it}(t_1/t_2)$; $E_n = E_C - E_{Fermi,\ bulk}$.

by C-V, admittance spectroscopy (AS) and CC-DLTS measurements in a temperature range from 294 K to 480 K.
At constant sample temperature T_S, the modified CC-DLTS methods provides voltage transients $V_R(t)$ necessary to keep the capacitance constant. For particular rate windows t_1/t_2, the correlation signal $\Delta V = V_R(t_2) - V_R(t_1)$ is determined as a function of the surface potential ψ_s, which is obtained from a fit to the corresponding C-V characteristic. The energy position E_{it} of interface traps is given by $E_{it} = q\psi_s + (E_C - E_{Fermi,\,bulk})$ and D_{it} is determined by the maximum correlation signal ΔV_{max}.
As an example Fig. 1 displays the correlation signal ΔV as a function of $q\psi_s$ for different rate windows; the measurements were taken on a p-type 6H SiC MOS structure, which was fabricated by wet oxidation. The correlation signal drops down to $\Delta V_{max}/2$, when the Fermi energy crosses the emitting interface states. At this point, the corresponding energy position E_{it} can be determined according to the relation

$$E_{it}(t_1/t_2) = q\psi_s(t_1/t_2) + E_C - E_{Fermi,\,bulk},$$

which is indicated in Fig. 1.

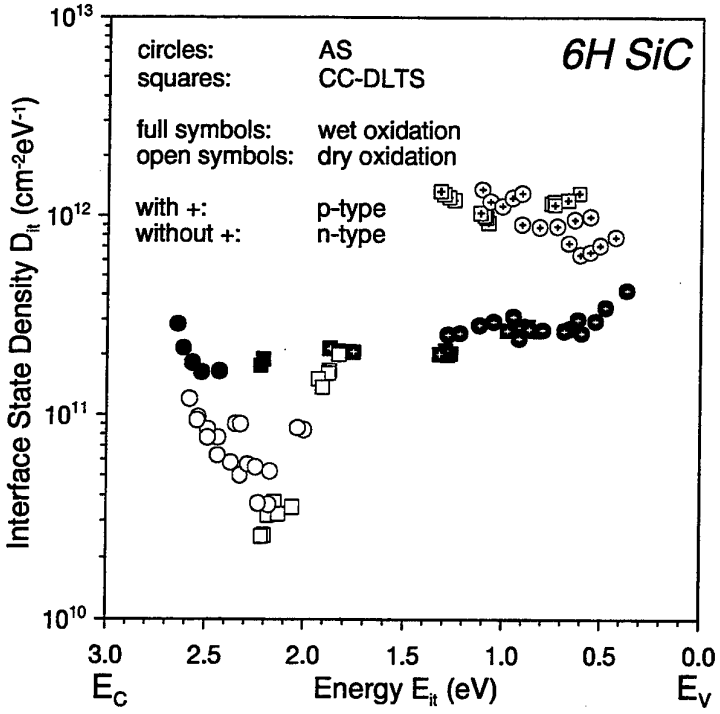

Fig. 2 Interface state density D_{it} as a function of energy E_{it} compared for dry (open symbols) and wet (full symbols) oxidation. The data are obtained from AS (circles) and CC-DLTS (squares). P-type 6H-SiC is marked with +; symbols without + represent n-type 6H-SiC.

The interface state density D_{it} as a function of the interface trap energy E_{it} for n-/p-type 6H-SiC MOS structures prepared by dry/wet oxidation is shown in Fig. 2. The processing and measurement techniques are explained in the figure. Wet oxidation reduces D_{it} in p-type MOS structures (lower half of the bandgap) compared to dry oxidation. For n-type MOS structures (upper half of the band gap), the opposite behavior is observed. In the framework of the "Carbon-Cluster-Model" two conclusions can be made:

1. Compared to dry oxidation, the number of sp^3-bonded graphite-like carbon clusters providing states in the upper half of the band gap is increased by wet oxidation (full symbols); since D_{it} is almost constant over the entire band gap, it is assumed that all the interface states are caused by these graphite-like carbon clusters.
2. Compared to wet oxidation, the number of sp^2-bonded rings, which predominantly provide states in the lower half of the band gap, is strongly increased by dry oxidation.

We assume, that the surplus of hydrogen introduced during the wet oxidation leads to an increased/reduced formation of sp^3/sp^2-bonded carbon by breaking the C-C double bond and terminating the dangling bond.

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ELECTRICAL CHARACTERIZATION OF 6H-SIC METAL-OXIDE-SEMICONDUCTOR STRUCTURES MADE BY REMOTE PLASMA ENHANCED CHEMICAL VAPOUR DEPOSITION

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We report high frequency capacitance-voltage (HF CV) analysis of Metal-Oxide-Semiconductor (MOS) structures where the SiO_2 layer is deposited by remote plasma enhanced chemical vapour deposition (RPECVD). Presently, the deposited oxides contain higher density of interface states (D_{it} in the 10^{12} -10^{13} cm^{-2} range) than our thermally grown oxides. The results agree with the study of Gölz et al [1] who found that a hydrogen plasma precleaning of the SiC surface improves the oxide quality. Our best deposited oxides so far are obtained using sacrificial oxidation which indicates poor quality of the initial SiC surface.

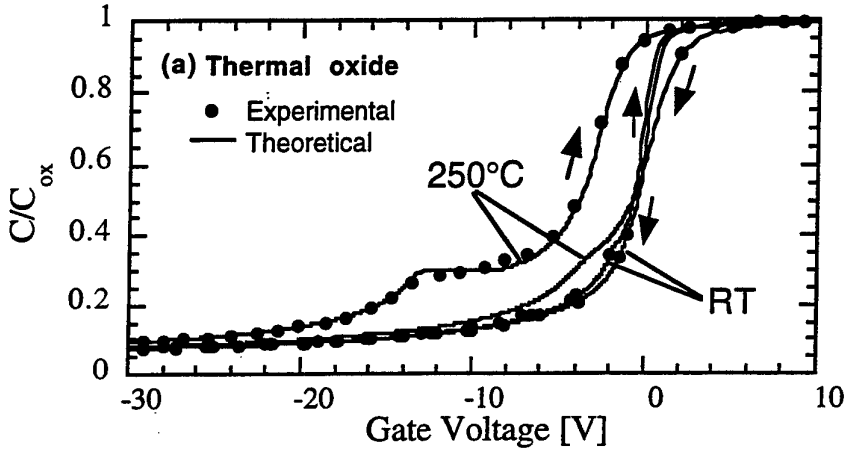
The substrates are n- and p-type 6H-SiC with a net doping concentration of 7.1 10^{15} and 1.1 10^{16} cm^{-3} for the epitaxial layers, respectively. The samples received standard RCA cleaning before loading into the RPECVD chamber. Prior to SiO_2 deposition, the surface of some samples was exposed to a H_2/He plasma followed by an O_2/He plasma for 5 minutes each. The plasma power was 200 W and the substrate temperature was 300°C. The deposition time was 12 minutes using 10% SiH_4 as a precursor to form SiO_2 with the resulting SiO_2 films with thicknesses of 400-500 Å. Thereafter, a 0.5 μm thick aluminum layer was evaporated on the oxidized side of the samples and lithographically patterned to form small- and large-area capacitors (100-1000 μm in diameter). The usual ohmic back-contact was replaced by a very large (>20 times the gate dimension) capacitive contact on the front side directly in contact with the epilayer.

The thermal oxidation was conducted, after a standard RCA clean, at 1150°C in dry O_2. The final thickness of SiO_2 was estimated to 40-50 nm from the value of C_{ox}. The device fabrication process is discussed in more details elsewhere [2].

Figure 1 shows the high frequency (1MHz) C-V measurements on n-type 6H-SiC capacitors for both thermally grown and RPECVD deposited oxides. The typical ledge and hysteresis indicate the presence of high interface state density in both cases. However, in the case of thermal oxides, one has to use a higher temperature in order to observe the effect of deep interface states on the CV curves. These interface states are located approximately at the middle of the SiC bandgap [2]. They are inactive at room temperature but are responsible for the ledge appearing at approximately -13 V in fig 1(a) when the CV data is collected at 250 °C. This can lead to an underestimation of the value of interface state density if the samples are only examined at room temperature. The high frequency CV curves are analyzed by numerical simulations (labelled theoretical in Fig. 1) using a non-equilibrium model which is described elsewhere [2,3].

For plasma deposited oxides, the density of interface states is higher ($\approx 10^{13}$ cm^{-2} range) and already at room temperature a ledge is observed in both voltage sweep directions. Post metallization annealing at 350-400°C did not have any significant effect on the oxide quality. The large flatband shift ($\approx$ +10 V in Fig. 1 b) agrees with the previously reported results by Gölz et al. [1]. So far we have concentrated on the effect of plasma precleaning prior to deposition. Even though the oxides are in general of poor quality we find that the best oxides are currently obtained by sacrificial oxidation. After depositing an oxide of $\approx$ 40 nm the oxide is etched away and a new layer is deposited after using H_2/He and O_2/He plasma precleaning.

It should be pointed out that we have thus far not performed high temperature annealing of the samples after deposition. Gölz et al [1] reported that the relative shift of the ledge in the CV characteristics, which is an indication of the density of interface states, can be effectively reduced by annealing at 1150°C for 50 minutes. We expect further reduction of the density of interfacial defects after optimization of the various process parameters during RPECVD as well as the introduction of high temperature annealing after the SiO_2 deposition.



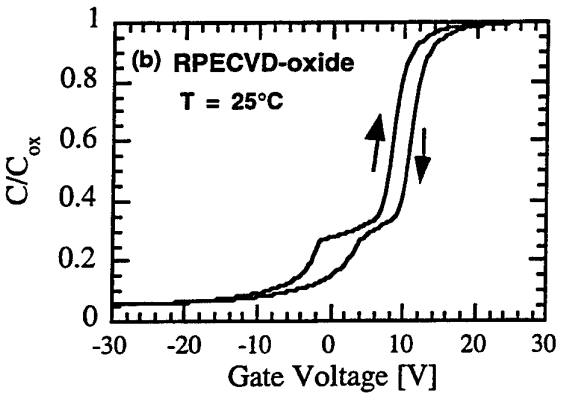


Fig. 1. Experimental (dots) and simulated (Solid line) HF CV curves of n-type SiC MOS structure, in both voltage sweep directions:
(a) Thermal oxides at 25°C (RT) and 250°C,
(b) RPECVD oxides at T= 25°C.

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ELECTRICAL CHARACTERIZATION OF 6H-SiC ENHANCEMENT-MODE MOSFETs AT HIGH TEMPERATURES

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The rapid commercial development of inversion-channel MOSFETs in 6H-SiC has been hindered by low inversion mobility and the poor oxide stability at elevated temperatures. Fortunately, promising results on oxide reliability and increased inversion mobility, as well as the reduction of interface states, have been achieved in recent years. [1, 2].

Here, we report the dc characteristics of lateral, small-signal 6H-SiC inversion MOSFETs from 303 K to 673 K. Fig. 1 shows a generalized cross-section of the device. The output characteristics of a linear 100/20 µm MOSFET at 303 K is presented in Fig. 2, which shows a linear slope at small V_{DS} (< 1V) and an excellent saturation behaviour with a drain-to-source saturation current I_{DSS} of 1.53 mA/mm at V_{DS} = +10V and V_{GS} = +9V.

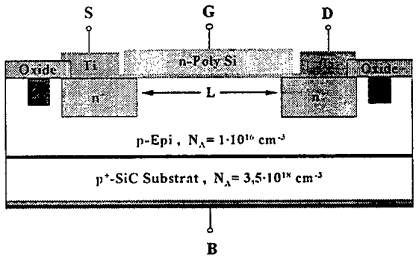

Fig. 1: Cross-section of a four terminal, n-channel inversion MOSFET. The Source/Drain n^+- contacts are achieved by ion implantation of nitrogen and the p^+- channel stopper by aluminum.

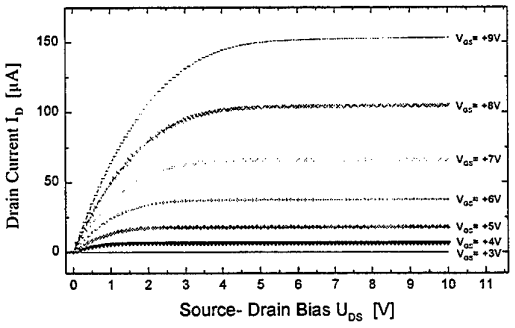

Fig. 2: Output curves of a 100/20 µm MOSFET at 303 K.

As it is one of the most important parameter of a MOSFET, the threshold voltage V_T is extracted from a plot of sqrt (I_{DSS}) versus V_{GS} in the saturation region (V_{DS}= +8V)[3]. A straight line should result giving V_T as the intercept on the V_{GS}-axis. Fig. 3 shows the temperature dependence of V_T. The inversion layer mobility μ_n of electrons is extracted by plotting the channel conductance g_D in the linear regime (V_{DS}= 100 mV) as a function of V_{GS}. It is possible to deduce μ_n from the slope of such a plot, if the oxide capacitance in strong accumulation C_i is known. C_i= $6{,}5\times10^{-8}$ F/cm^2 yields an oxide thickness d_i of about 53 nm measured on a MOS-capacator. We believe that the difference in V_T and μ_n comparing both devices is due to oxide and surface inhomogenities and also series resistance effects.

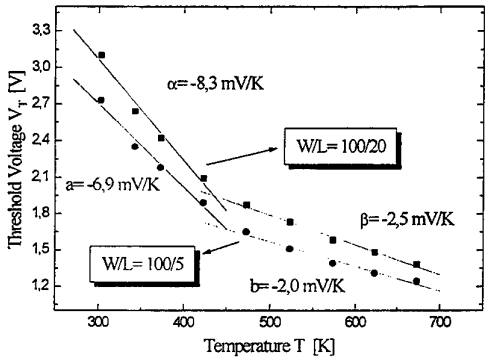

Fig. 3: Threshold voltage versus temperature. To estimate the decrease of V_T with temperarure, two linear fits are added to the curves, as reported in previous studies [4].

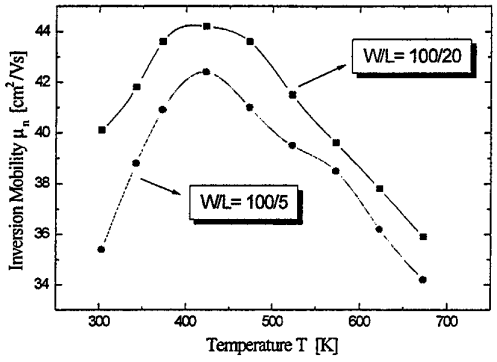

Fig. 4: μ(T) curve for 6H-SiC inversion MOSFETs with a thermally activated mobility up to 423 K and a thermally degraded mobility above 423 K due to phonon scattering.

With the help of Fig. 3 and Fig. 4 one can understand the temperature behaviour of the output characteristics shown in Fig. 5. Given the square law dependence, equation [3], I_{DSS} increases with temperature because μ_n increases and V_T decreases. At T= 573 K, the I_{DSS} peaks and begins to decline because of the strong decrease in mobility with further increase in temperature. The temperature dependence of the ratio I_{ON}/I_{Off} is shown in Fig. 6 with an excellent ratio of 10^8 at 303 K and 10^5 at 673 K. Below V_T one can see the expected exponential relationship between I_{DSS} and V_{GS} with a slope of 170 mV per decade at 303 K and the current at V_{GS}= 0V has a thermal activation energy of about 1.3 eV.

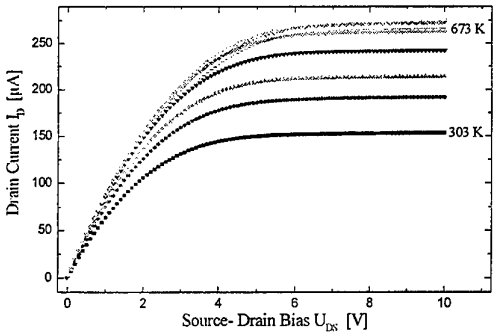

Fig 5: Output characteristics of a 100/20 μm MOSFET at V_{GS}= +9V with varying temperature from 303 K to 673 K.

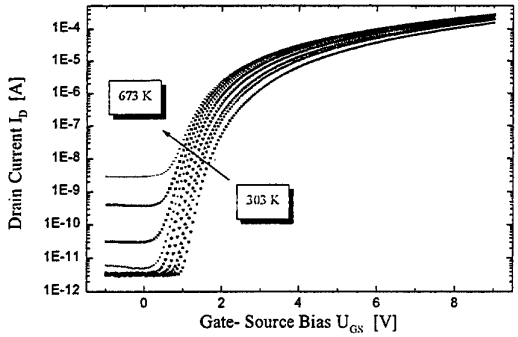

Fig 6: The temperature dependence of the transfer characteristics of a 100/20 μm MOSFET.

The gate leakage currents as a function of temperature were measured with an applied electrical field $\vec{E}_{OX}$ well below the onset of Fowler-Nordheim tunneling ($\vec{E}_{ox} \leq 6\,MV/cm$). The Arrhenius Plot of I_G vs. reziprocal temperature at V_{DS}=100 mV exhibits an activation energy of 670 meV which we attribute to defect-assisted conduction mechanisms.

In conclusion, we report 6H-SiC MOSFETs that show excellent characteristics in the temperature regime up to 673 K. These devices are well suited for integration with sensors or actuators for high temperature industrial applications.

Acknowledgements:

The authors wish to thank Prof. Dr. W. Aßmus (University of Frankfurt/Main) and Dipl.- Phys. F. Wischmeyer (Daimler-Benz AG, Frankfurt) for valuable discussions. This work was partially supported by the BMBF under contract number 16 SV 020.

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DESIGN OF A 600 V SILICON CARBIDE VERTICAL POWER MOSFET

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Introduction

This paper will present simulated electrical characteristics using Medici software of two different MOSFET structures for both commercially available silicon carbide polytypes (6H-SiC and 4H-SiC). The aim is to achieve a realistic estimation of the electrical performance of a 600 V SiC power MOSFET, combining at best the good silicon carbide properties and the current technology constraints.

Structure design

Due to the lack of dopants diffusion into silicon carbide, non-classical ways for the realization of such vertical transistors must be used. Figure 1 presents the U-MOSFET structure. Two successive epitaxial (n- and p-type) layers are grown on a highly doped substrate. Nitrogen implantation is required to realize the source. Trench is realized thanks to plasma etching before the gate oxide deposition and the gate metallization. The main technology factor is the slope of the trench sidewall. In agreement with our etching results [1] the slope could be varied in the range 15 to 65°. Another important technological parameter is the length at the bottom of the trench, depending mainly on the lithography performance.

The second structure consists in a double implanted MOSFET structure, shown on figure 2. After the growth of the n-type epitaxial layer, p-wells are implanted, and then n-type implantation is required to make the source. In this case, the major technological points are the distance between the p-wells and the depth of the p-well.

Both structures have been simulated using Medici software taking into account the limitations due the technological constraints and the best experimental values found in the literature relative to 6H and 4H-SiC. Band-gap energy and mobility are the main parameters for the two polytypes. Simulations take into account the degradation of the mobility in the MOSFET channel area. The design is optimised for a forward blocking voltage of 600 V, taking into account a maximum electric field value in the oxide layer of 3×10^6 V/cm.

Main results

The forward current density is considered under a forward voltage drop V_{DS} of 1 V and V_{GS} = 15 V.

For the U-MOSFET structure, the maximum electric field is located at the corner of the trench. In such conditions, the maximum electric field in the SiC is about 8×10^5 V/cm which is far beyond its critical electric field (2×10^6 V/cm). The forward blocking voltage increases while the slope decreases (as shown on fig. 3), in the meantime and due to a longer length of the channel, the forward characteristics performance decrease, as it is plotted on fig. 4.

For the U-MOSFET, the doping of the drift region must be lower and the thickness higher than for the DI-MOSFET structure. The epitaxial layer for the drift region is 2.6×10^{15} cm^{-3} with a thickness of 10.6 µm, while for the DI-MOSFET, a thickness of 6.4 µm with a doping level of 7.7×10^{15} cm^{-3} is sufficient for a 600 V device. Table 1, presents the considered mobilities and also the current density for the optimized structure for both polytype.

Conclusion

Although 4H-SiC has a better bulk mobility than 6H-SiC, its performance are strongly altered by the extremely low channel mobility. It results in the fact that a 6H U-MOSFET remains more interesting than a 4H DI-MOSFET. An estimation of the required channel mobility will be given in the final paper. The 6H DI-MOSFET has better performance that the U-MOSFET but it strongly depends on the feasibility of a deep implanted p-well, as shown on fig. 5 and 6.

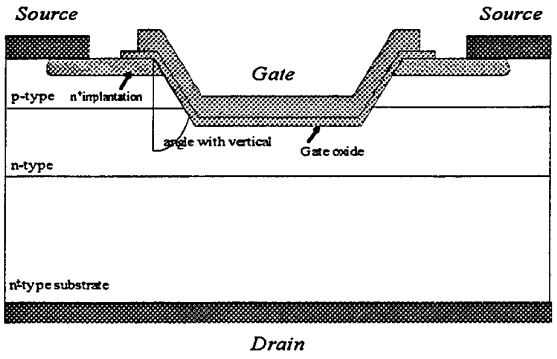

figure 1 : U-MOSFET transistor structure

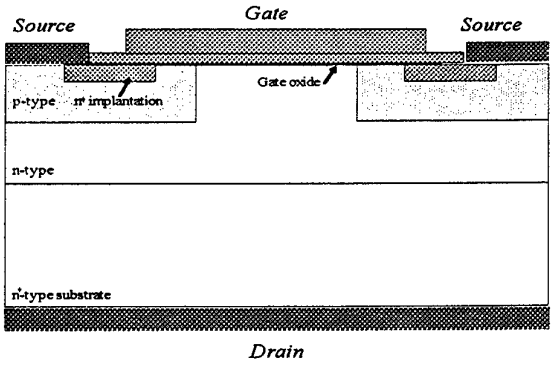

figure 2 : DI-MOSFET transistor structure

	U-MOSFET (600 V)		DI-MOSFET (600 V)	
material polytype	4H-SiC	6H-SiC	4H-SiC	6H-SiC
electron channel mobility	1.5 cm²/V.s	70 cm²/V.s	1.5 cm²/V.s	70 cm²/V.s
electron vertical mobility	700 cm²/V.s	100 cm²/V.s	700 cm²/V.s	100 cm²/V.s
current density	1.4 A/cm²	15 A/cm²	1.35 A/cm²	32 A/cm²

Table 1 : forward current density characteristics versus the transistor structures and SiC polytypes

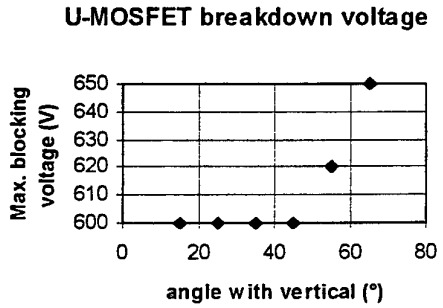

Figure 3 : forward characteristics for both polytypes

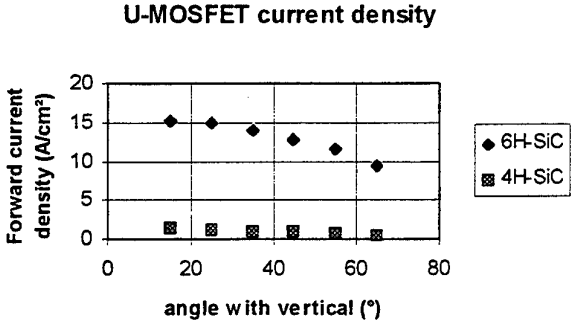

Figure 4 : forward characteristics for both polytypes

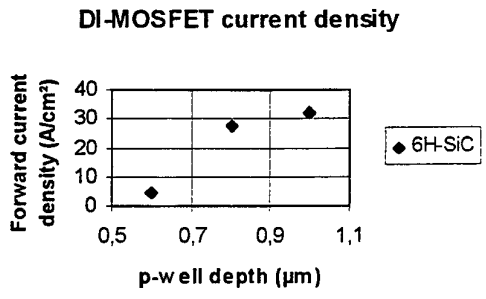

Fig. 5 : 6H-SiC forward characteristics

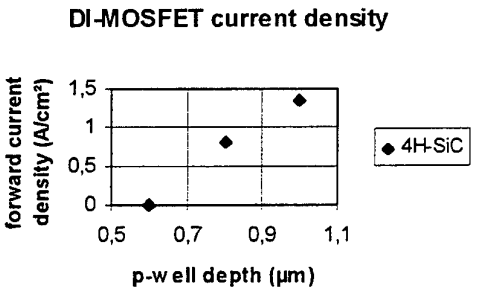

Fig. 6 : 4H-SiC forward characteristics

Reference : [1] F. LANOIS, D. PLANSON, M.L. LOCATELLI, J.P. CHANTE : *"Angle etch control for silicon carbide power devices"* 1996 - Applied Physics Letters - Vol. 69, n°2, July, pp. 236 - 238

SPECTROSCOPIC ELLIPSOMETRY OF HETEROEPITAXIALLY GROWN CUBIC SILICON CARBIDE LAYERS ON SILICON

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Variable angle spectroscopic ellipsometry is a very sensitive method to investigate thin layers. It measures the change in the polarization state of light reflected from the sample. The measured values are expressed as Ψ and Δ. These values are related to the ratio of the Fresnel reflection coefficients r_p and r_s for p- and s-polarized light, respectively. Because ellipsometry measures the ratio of two values it is usually accurate and very reproducible. Because the ratio is a complex number, it also contains phase information, which makes the measurement very sensitive. The technique allows in a simple way the determination of the layer thickness and the optical constants of the material and was used here in a spectral range from the near infrared up to the near ultraviolet.
For the determination of the optical constants of cubic silicon carbide we used a CVD grown SiC film sample on (100) orientated silicon substrate from Hoya. The film thickness of silicon carbide is nearly one micrometer. The interference maxima of the reflectivity touch the reflectivity curve of a silicon substrate. This means, that the interface between the silicon substrate and the silicon carbide layer is nearly smooth and flat. Therefore a 2-layer model could be used to determine the thickness and optical constants of silicon carbide. A small surface roughness was simulated with the Bruggemann effective medium approximation (EMA) and was verifyed by AFM measurements. The determined spectral course of the optical constants of silicon carbide was compared with data from Palik [1] and Adolph *et al.* [2]. The difference to the data from Palik is particularly in the extinction coefficient k. The data from Adolph *et al.* was calculated using an *ab initio* pseudopotential-plane-wave method and random-phase approximation and show nearly the same dispersion but differences in the absolute values of n and k.

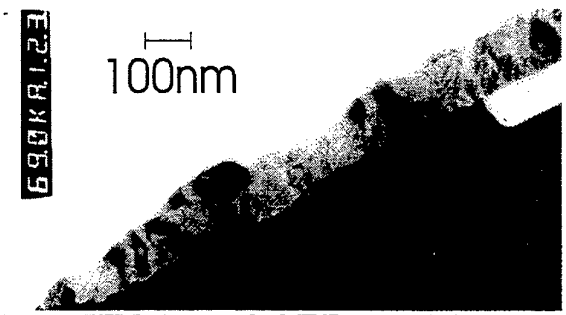

Fig. 1: TEM picture of a MBE grown SiC film on Si

These optical constants were used to determine the layer structure of thin MBE grown silicon carbide films on silicon. The MBE grown silicon carbide layers have a non ideal interface and a high surface roughness (Fig. 1). Furthermore the SiC layers may contain inclusions of other SiC modifications and an excess of silicon or carbon. Therefore a simple 2-layer model is not sufficiant to fit the experimental data. We used a 3-layer model with the Bruggemann effective medium approximation (Fig. 2). In the case of the Bruggemann model the effective medium itself is the host medium for the separate mixing compounds in opposite to the Maxwell-Garnet model, where one compound is the host material for the other phase.

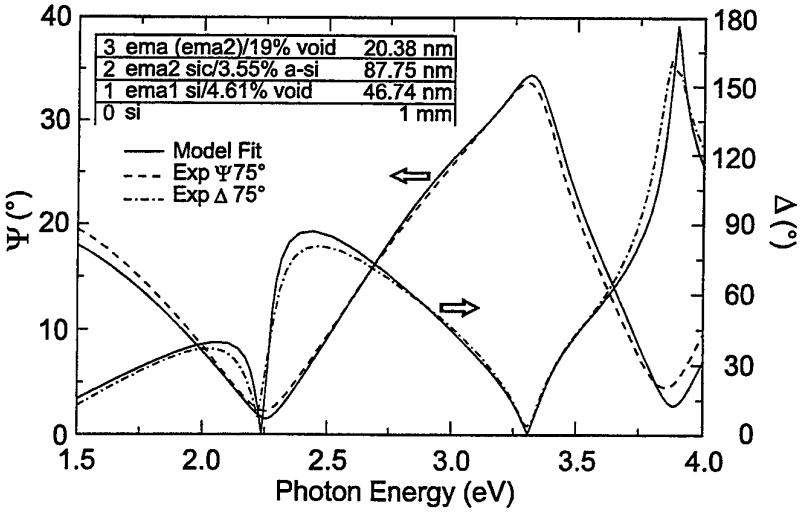

Fig. 2: Results from spectroscopic ellipsometry of MBE grown sample mt 24

In order to verify the fit results of the spectroscopic ellipsometry we used further methods to characterize the samples. The thickness of the top EMA layer was compared with the results of AFM measurements. Information about the width of the interface and composition of the silicon carbide layer was obtained from AES measurements and was used for the fit of the model to the ellipsometric data. The measured excess silicon was simulated by a mixture of amorphous silicon and stoichometric 3C-SiC with the Bruggemann effective medium approximation. A big problem for the fit procedure is the interface between the silicon substrate and the SiC layer. Often very large void inclusions exist here, which originate from the diffusion of silicon to the surface during the growth process. This interface was fitted also using a EMA-mixed layer, although the validity range of the effective medium approximation is clearly exceeded here. Nevertheless the fit results show a good agreement with results from transmission electron microscopy of the samples. The void inclusions are clearly visible on these micrographs (Fig. 1).
Summarizing we can establish, that it's possible to use the spectroscopic ellipsometry for the investigation and the characterization of SiC/Si samples with non ideal interfaces.

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VIBRATIONAL STUDY OF THE CARBONIZATION OF Si SURFACE

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The 3C-SiC is the only polytype that can be formed on an Si substrate. If the crystallinity of the grown heteroepitaxial layer is improved, it will have great advantages to develop large size devices. To improve the quality of the 3C-SiC crystal, it is important to control the carbonization process.

The Fourier-transformed infrared attenuated total reflection (FT-IR-ATR) spectroscopy has abilities to distinguish the absorbed species and structures of Si and SiC surfaces. We studied the carbonization of Si substrate by proving changes of surface Si-H stretch modes using FT-IR-ATR.

Si wafers faced on (1 1 1) and (1 0 0) were cut into 10 x 50 x 1 mm. Shorter edges were beveled at 45 $^{\circ}$. Infrared light is internally reflected 100 times on both faces of the sample (Fig. 1). The measurements were carried out after H_2 annealing and after the carbonization. H_2 annealing which is typically included before the carbonization, was performed in H_2 ambient at 1000 C for 10 min. The carbonization was carried out at 1000 C in a concentration of C_3H_8 at 0.05 % for 0 to 15 min.

Fig. 1. (a) shows the ATR spectra of Si (1 1 1) after H_2 annealing. A narrow Si-H stretch mode directed normal to the surface was observed at 2083 cm^{-1}. This indicates that surface was ideally terminated by silicon monohydride (SiH) with three Si-Si back bonds. Therefore the H_2 annealing procedure prior to the carbonization produces an atomically flat surface with (1 x 1) H structure.

Fig. 1. (b) shows the spectra obtained from the carbonized Si (1 1 1). Several Si-H stretch modes appeared at higher than 2083 cm^{-1} after the carbonization. It is well known that Si-H stretching frequency becomes higher when the sum of the electron negativity on its back bond is increased. Thus observed spectral changes suggest a formation of Si-C bonding. From the reported vibrational frequency of Si-H stretch mode on 6H-SiC (0 0 0 1) [1], we attribute the observed mode at 2120 cm^{-1} after the carbonization as SiH with three Si-C back bonds. The vibrational modes between 2090 ~ 2120 cm^{-1} indicate SiH which was bonded both Si and C at an intermediate state. Also the vibrational mode above 2135 cm^{-1} indicates a presence of silicon dihydride (SiH_2) and / or silicon trihydride (SiH_3). If the carbonized Si (1 1 1) surface is atomically flat with (1 x 1) structure, the SiH with three Si-C back bonds can be observed only for p-polarization, and also the SiH_2 and / or SiH_3 are absent. Therefore, observed spectral feature indicates the carbonized surface was microscopically rough in this situation.

Fig. 2. (a) shows the spectra of Si (1 0 0). The sharp peaks at 2099 and 2087 cm^{-1} indicates symmetric and asymmetric Si-H stretch mode. The symmetric mode (2099 cm^{-1}: electric field is in the plane of incidence) is observed for only p-polarized radiation. Also the asymmetric mode (2087 cm^{-1}: electric field is orthogonal to the plane of incidence) is observed for both p- and s-polarized radiation. Therefore the H_2 annealed Si (1 0 0) surface was reconstructed into well ordered H terminated (2 x 1).

Fig. 2. (b) shows the spectra obtained from the carbonized Si (1 0 0). The mode at 2124 cm^{-1} indicates the Si-H with three Si-C back bonds, and the mode above 2130 cm^{-1} indicates the $Si-H_2$ and /or $Si-H_3$. If the carbonized (1 0 0) surface has ordered structure, significant spectral difference will be observed between p- and s-polarization, whereas the noticeable difference was not obtained in this situation.

From these results; (1) atomically flat and H terminated (1 x 1) and (2 x 1) surfaces could be prepared on Si (1 1 1) and (1 0 0) by *in-situ* H_2 annealing prior to carbonization. (2) Si-H mode was changed by carbonization. It indicated that a formation of Si-C bonding. (3) the carbonized surfaces were microscopically rough in this situation.

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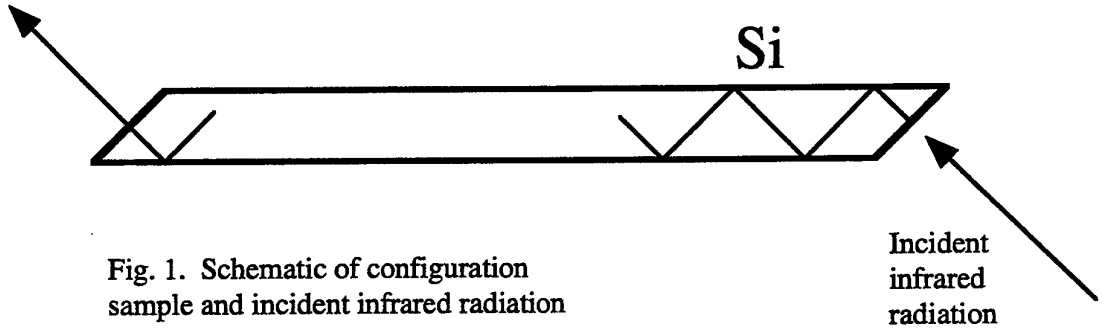

Fig. 1. Schematic of configuration sample and incident infrared radiation

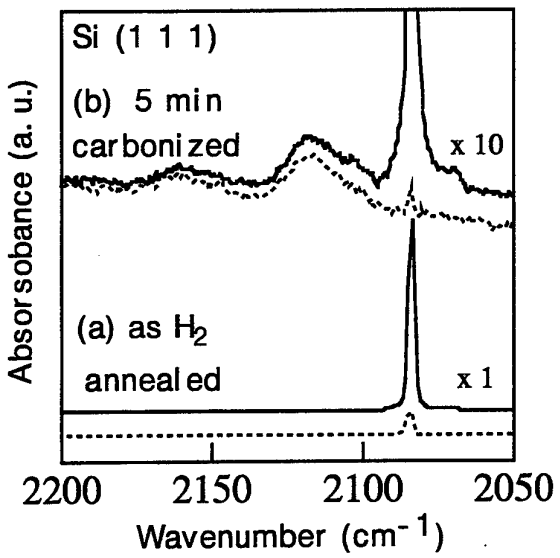

Fig. 2. Polarized IR spectra of silicon-hydrogen stretching vibrations for Si (1 1 1).
—— p-polarization, ---- s-polarization

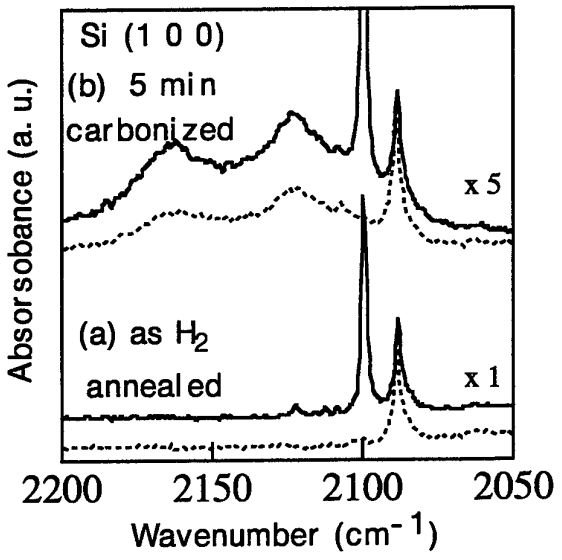

Fig. 3. Polarized IR spectra of silicon-hydrogen stretching vibrations for Si (1 0 0).
—— p-polarization, ---- s-polarization

THE PHYSICS OF HETEROEPITAXY OF 3C-SiC ON Si : ROLE OF Ge IN THE OPTIMIZATION OF THE 3C-SiC/Si HETEROINTERFACE

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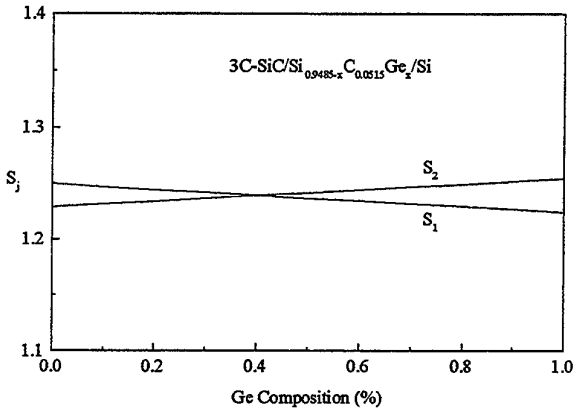
Silicon carbide is a promising material for high-temperature and high-power electronic devices. The elaboration of high quality layers, as the active part of a device, is strongly dependent on substrate quality. Homoepitaxial growth of SiC layers is actually facing the fundamental problem of wafer surface crystalline quality. In order to obtain layers of electronic quality, it is necessary to carry out the epitaxy on substrates with a low defect density. Although the reduction of wafer structural defect density is a research area in progress, the availability of substrates presenting a large surface area free of structural defects (micropipes, dislocations) is still lacking. The state of art corresponds to micropipe density ~ 1 cm^{-2} for wafer size ~ 35 mm, with a lower density (~ 0.2 cm^{-2}) near the centre of the wafer.

The alternative is to use Si wafers which exist with a high surface crystalline quality and with large surface area free of extended defects. However, such an alternative presents a disavantage due to the mismatch of geometric and thermal properties of SiC and Si host materials. Indeed, the lattice parameter mismatch between 3C-SiC and Si is around 20 % and the thermal expansion coefficients are different by 8 %. For such a heterosystem, one could expect to obtain strained interfaces and, as we know, interface strains can no longer supports lattice mismatch when layer thickness exceeds growth critical thickness. For large layer thickness, extended defects as dislocations damage the interface crystalline quality and, because they can propagate into the growing film , they lead to active layers of poor crystalline quality. These extended defect-related processes are inherent to any modern growth technique, seeing that mismatched host materials are involved in the heterosystem.

Among the different techniques which can smooth out the effect of large lattice mismatch, the buffer layer technique has been widely used to assist heteroepitaxial growth. The carbonization of clean Si surface using hydrocarbon radicals is generally performed at the early stage of the growth process. Gas source molecular beam epitaxy (GSMBE) experiments [1] have shown that when one uses $(CH_3)_2GeH_2$ (DMGe) as carbon source, the morphology of the carbonized surface layer improves when compared with the one without Ge (carbon is then provided by hydrocarbon radicals from cracked $-C_3H_8$). The thickness of the smooth carbonized layer is ~ 40 Å with a Ge concentration showing a saturation around 0.4 % , and the purpose of using DMGe is to introduce a large size atom at the heterointerface.

This study, based upon the S-correlated theory of interface optimisation [2], is a part of a programm which aims to optimize heterointerfaces by suitable choices of host materials, of precursor chemical species and of buffer layers. In this communication, we discuss the physics which is behind the improvement of the crystalline quality of the heterointerface through the incorporation of bigger atoms (Ge). If the atom size is

indeed one of the important parameters, it is however worth noticing that this parameter has a local effect and can not on its own explain the whole mechanism which triggers such a long range heterointerface improvement . We claim that elastic as well as dynamical properties must be involved because they are are inherent to growth process at temperatures as high as 650 °C which is the growth temperature reported in ref.1. A suitable approach can be based on the use of the elasticity theory equations [3] which relate strain and dynamics. From these equations, two parameters can be identified : (i) the square of the angular frequency ω of acoustic phonons which is introduced by the second derivatives of atomic displacements with respect to time when a Fourier analysis of lattice dynamics is carried out because of lattice periodic conditions. This analysis implies that the symmetry of the lattice unit cell (we consider here a two-dimensional unit cell associated with the interface lattice and consequently its corresponding two-dimensional Brillouin zone 2DBZ) is implicitly present in these equations as well as phonon wave vectors which are related to geometric parameters as the extension of the interface unit cell in the direct lattice space. The ensuing interface unit cell, which is associated with a misfit induced interface superstructure (MIIS) in the case of an interface j (B/A) made of two host materials A and B, must accomodate the lattices of A and B in the sense of an interface optimisation. This MIIS can be considered as a precursor geometric configuration of nucleation centers for misfit dislocations network (NCMDN) induced by the relaxation of interface strains for layer thickness beyond the growth thickness. (ii) The ratio $S_m=[f(C_{ij})/\rho]_m$, i.e. the elastic-density factor associated with material m (A or B), affects the strain terms in the elasticity equations and has a long range effect: $f(C_{ij})$ and ρ are respectively the effective elastic constants and the atomic density. The basic equation of the interface optimization theory with respect to the S factors is the continuity of S_j throughout the heterosystem [2], i.e. $S_1=S_2$ if two heterointerfaces are created when the heterosystem C/B/A is elaborated (interface 1 : B/A; interface 2 : C/B).



We have applied our theory to the heterosystem 3C-SiC/$Si_{1-y-x}C_yGe_x$/Si (C/B/A) where $Si_{1-y-x}C_yGe_x$ is introduced as a buffer layer to take account of the carbonization of Si in presence of Ge. In that case, interfaces 1 (S_1) and 2 (S_2) correspond respectively to $Si_{1-y-x}C_yGe_x$/Si and 3C-SiC/$Si_{1-y-x}C_yGe$. The results, shown on the above figure, demonstrate that the continuity condition on S_j can be fulfilled for Ge composition as low as 0.4 % , in agreement with the experimental results [1]. This composition corresponds to the first stage of the carbonization process, as C composition is $\cong$ 5 %.. Let us notice that the carbonization of Si without Ge has also been aimed by molecular beam epitaxy [4] with an alloy composition $Si_{0.95}C_{0.05}$. In that case, our approach predicts a large NCMDN spacing $L_{MD}\cong$ 19 Å (low defect density). By increasing the C composition up to 9.5 %, L_{MD} is equal to 14 Å, in agreement with the theoretical value predicted by a different approach [5], although TEM results [6] may give a larger value ($\cong$ 15.6 Å) for the 3C-SiC/Si interface. This discrepancy can be explained on the basis of a remaining misfit of 1 % due to residual strain in the TEM samples. One must bear in mind that the C composition of the buffer layer at the early stage of carbonization must remain low (5 % is a reasonable value) because of the distortions introduced by C in the Si lattice. Then, a gradual increase of C composition must be attempted in order to meet the conditions of a pseudomorphic growth of 3C-SiC layer [7]. Ge is probably not the only host atom which can improve the 3C-SiC/Si heterointerface and several alternatives must be investigated.

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THE EVOLUTION OF CAVITIES IN SI AT THE 3C-SIC/SI INTERFACE DURING 3C-SIC DEPOSITION BY LPCVD

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To optimize combustion processes in industry, a large number of process parameters must be accurately determined. This is usually done by sensors, which are increasingly based on semiconductor systems. Since most of these processes occur at high temperatures and in harsh environments, cubic silicon carbide (3C-SiC) on silicon is the compound semiconductor system, which will make possible the development of sensors for such extreme range applications [1]. The epitaxially grown 3C-SiC on Si has the advantage of bulk micro-machining processing facility and large wafer size capability.

One substantial step of the epitaxial growth of 3C-SiC on Si by CVD is the carbonization process at the early stage of growth. During this process only hydrocarbon is released, which reacts with the Si at the surface, forming a very thin SiC layer which acts as seed for the subsequent growth of the 3C-SiC film. The carbonization process is not a simple epitaxy but a strong, chemical reaction where a significant mass transport from the Si substrate to the SiC surface occurs [2, 3]. Due to this mass tranport cavities are formed in the Si substrate at the Si/SiC interface [4, 5]. The presence of the cavities at the interface may cause serious implications during micro-machining process as well as in the reliability of the sensor.

In the present work the evolution of cavities due to Si migration from the substrate to the surface in order to form SiC is investigated by Transmission Electron Microscopy (TEM) and Atomic Force Microscopy (AFM).

During the carbonization process on Si wafers, the Si substrate is the reservoir for the Si supply. In order to study easier the evolution of the cavities, the bulk Si was replaced by Silicon On Insulator (SOI) wafers. In this case only the Si-overlayer (SOL), which is less than 200 nm thick, is the Si supplier for the formation of SiC, where the buried oxide layer (BOX) acts as a barrier for the Si migration from the substrate. Therefore, the cavities are extended laterally in the Si-overlayer, as shown in the cross-section TEM micrograph in Fig. 1.

For the SiC deposition commercially available UNIBOND wafers from SOITEC were used. The SOI wafers were sacrificially oxidized in order to form SOLs with different thickness. The 3C-SiC deposition was carried out in a low pressure CVD reactor at 1200°C using methysilane. Details on the quality of the 3C-SiC overgrown will be presented in another contribution in this conference [6].

Carbonization at 1220°C for 30 s results in a SiC buffer layer about 7 nm thick and a SiC/Si interface free of cavities, as shown in Fig. 2. However, as the epitaxial growth proceeds with a growth rate 73 nm/min, cavities appear. In order to study the evolution of the cavities the following experiments were performed.

a) SiC films of the same thickness were deposited on SOI wafer with different SOL thickness. The density and the size of the cavities were measured, by combined cross-section and planar view TEM. Subsequently the uncovering of the surface at the SiC/Si interface due to the cavities was estimated versus the thickness of the SOL.
b) Using the results of paragraph (a), the volume of Si that was released from the SOL was calculated. In all the cases, the missing volume was larger than the Si consumed for the formation of the SiC buffer layer. This strongly suggests that significant portion of silicon was out-diffused during the growth, revealing a high diffusion driving forces during the CVD process, as was proposed by Ferro et al. [7].
c) SiC film with different thickness were deposited on SOI wafers having the same SOL thickness. The density and the size of the cavities were determined and their total volume was estimated. It was shown that the volume of the cavities for SiC films thicker than 700 nm remains constant.
d) Redistribution of the size of the cavities is observed after annealing at 1200°C. When a large cavity is formed the area around it is denuded from the small cavities, as shown in Fig. 3, resembling an Oswald ripening mechanism.

Finally, conditions to suppress the formation of cavities during growth of SiC films on SOI structures will be discussed.

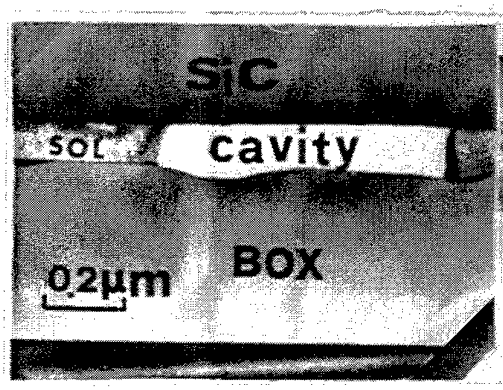

Fig. 1

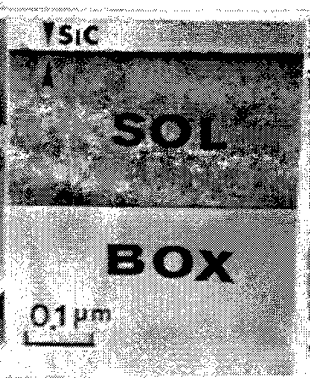

Fig. 2

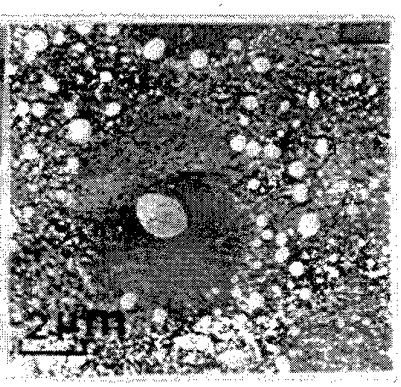

Fig. 3

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STRONG PHOTOLUMINESCENCE FROM 3C-SIC/SI HETEROINTERFACES

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Single crystal 3C-SiC epitaxial films are grown on Si(111) surfaces using tetramethylsilane by rapid thermal chemical vapor deposition. A strong and broad photoluminence (PL) peak was observed at room temperature from free standing films of SiC prepared by etching the Si substrate, in contract to the as grown epilayer of SiC/Si which does not show any noticeable PL peak.[1] The energy of the main PL peak varies from 2.1 to 2.4 eV depending on the excitation wavelength and excitation light intensity, and the full width at half maximum of the PL peak is about 450 meV. The luminescent property also changes with the initial growth condition such as the carbonization or nitridation of Si surface, the substrate temperature and the source gas feeding condition. It has been normally observed that voids are formed on the Si side of the SiC/Si heterointerface during the initial growth due to the outdiffusion of Si atoms at high growth temperature of SiC.The formation of voids are shown to be controlled by the initial growth condition; it can be prevented by feeding the source gas before heating the substrate[2] or brief nitridation of the Si surface. Since voids generate microstructural defects and roughness in the SiC/Si interface, electrical properties of the SiC layer deterioate with increasing size and density of voids. Table I summarizes results of Hall effect measurement for SiC grown by flowing the source gas before heating the substrate

up to the growth temperature (type A) and that by flowing the gas after heating the substrate. (type B) The PL peak of the type A sample possessing few voids at the interface appears at higher energy than that of type B with many voids. The origin of the strong photoluminescence will be discussed in view of the localization of carriers at the interfacial disorder and the strain relaxation by removal the Si substrate.

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Table 1. Electrical properties of 3C-SiC grown on Si(111).

	Tape A[a]	Tape B[b]
Mobility	884 $cm^2/V \cdot s$	464$cm^2/V \cdot s$
Carrier concentrations	1.48×10^{16} cm^{-3}	2.78×10^{16} cm^{-3}
Resistivity	0.462 $\Omega \cdot cm$	0.480 $\Omega \cdot cm$

[a]SiC grown on Si by heating the substrate after starting the gas flow
[b]SiC grown on Si by heating the substrate before the gas flow

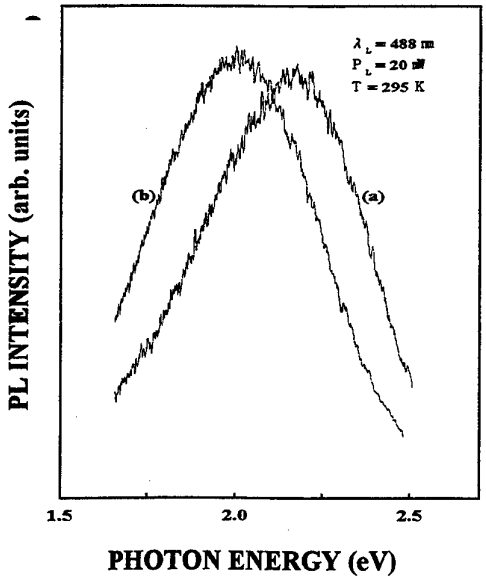

Figure 1. Room temperature PL spectra of free-standing SiC films grown by two different processes ; (a) substrate heating up to growth temperature after starting the flow and (b) substrate heating before the gas flow

STRUCTURAL AND MORPHOLOGICAL INVESTIGATIONS OF THE INITIAL STAGES IN SOLID SOURCE MOLECULAR BEAM EPITAXY OF SIC ON (111)SI

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The lack of commercially available bulk crystals of 3C-SiC have retained over the years the interests to the thin film heteroepitaxy on silicon substrates. The most successful method is the chemical vapour deposition by a two step technique where first an initial layer is grown by carbonisation. Additionally to the large lattice mismatch the high temperatures above 1000°C necessary for that technique can cause detoriation of the SiC films. These are structural defects like twins and antiphase boundaries and morphological defects like the out diffusion related voids in the silicon substrate beneath the layer. At least an internal strain remains due to the large differences in thermal expansion. Meanwhile various efforts were made to minimise these problems, for example to lower the temperature using high reactive compounds or elemental sources in molecular beam epitaxial growth. In every case, however, the initial growth on the silicon substrate will be a variant of the carbonisation.

The carbonisation is a chemical reaction between a silicon substrate and carbon containing molecules from the gaseous phase forming a thin crystalline SiC layer. For these reaction a diffusion of silicon from the substrate to the surface is necessary which is highly suppressed in single crystalline SiC due to the low diffusion coefficient. The silicon transport can occur only at defects, for example grain boundaries. This local mechanism causes additional defects, both in the substrate and in the layer. Consequently the quality of the SiC layers will be essentially determined already by the nucleation.

In this work we investigated the nucleation and the initial SiC growth by solid source molecular beam epitaxy which is known to allow the lowest process temperatures. The carbon was supplied by electron gun evaporation of pyrolytic graphite. The morphological and structural evolution during growth were investigated by high resolution TEM, AFM, and RHEED. A growth model in dependence on the temperature and the carbon supply and the main differences to the carbonisation by hydrocarbons will be presented.

At very low temperatures (<700°C) we observed an incubation time prior to the occurrence of the first SiC nuclei. In this time a near surface silicon carbon alloy was formed. The SiC nucleation takes place with a high nucleation density and the grown layers are smooth, have small grains (10 ... 20 nm) and non cubic inclusions. The high number of defects allows a nearly homogeneous silicon out diffusion which results in far-reaching voids in the substrate. On top of it a bridge-like homogeneous and stable SiC layer grows (Fig. 1). The bottom and a part of the side walls of the voids are expected to be (111) planes. The angle between the bottom and the SiC layer is close to the off angle of the virgin silicon substrate. The voids are expected to nucleate at defects on the substrate. At the columns

between the voids the Si-SiC-interface is very smooth, however, a step can be seen between the left and the right bridge segments (fig. 1). The height of these steps is close to the height of the macrosteps on the silicon substrate due to step bunching after a non-optimised pretreatment. Similar steps also visible on top of the surface of the grown SiC layers as examined by AFM. If these steps are not present the extension of the voids are much larger. At longer processing times the voids can touch once another and the layer will peel off. Increasing the temperature the nucleation density became smaller and the grain size larger. Here the silicon diffusion occurs preferred more local on the grain boundaries. This results in deep trenches between the nuclei. At this places an epitaxial growth will be impossible and consequently a polycrystalline part is growing around a strongly oriented SiC nucleus. The deep trenches prevent a coalescence and the grown layers have a high surface roughness and partially unprotected silicon.

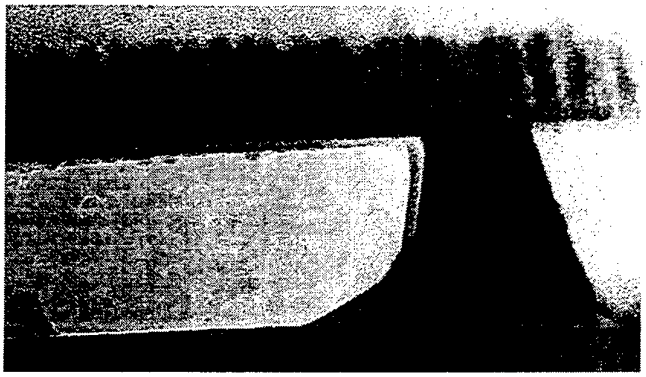

Fig. 1 X-TEM micrograph of a thin SiC bridge over large voids in the silicon substrate after carbonisation at 660°C

LOW TEMPERATURE SiC GROWTH BY LPCVD ON MBE CARBONIZED Si(001) SUBSTRATES

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3C-SiC on Si substrates is very attractive for the fabrication of robust sensors operating at high temperatures and harsh environments. Moreover, SiC is a very convenient substrate for GaN epitaxy. However, the diameter of commercially available SiC substrates is at maximum 2" and their cost is still extremely high. Thus, SiC/Si seems very interesting for subsequent GaN growth. In this work we combine the advantages of MBE and LPCVD to grow thick (≈1-2 μm) SiC films on 2" Si wafers misoriented 2-4° towards [110]. The aim of the work is to characterize and determine the mode of growth of the LPCVD SiC films.

Solid source MBE using pure pyrolitic graphite or Gas source MBE using acetylene were employed as C precursors to form the carbonization layer on Si. Substrate temperatures ranged from 700-950°C. The growth process was controlled by RHEED and the samples were characterized by TEM, AFM and Infrared Transmitance.

The CVD film growth was carried out in a hot-wall Low Pressure CVD reactor at temperatures between 1050-1100°C. An alkyl-silicon compound (tetramethylsilane, $(Si(CH_3)_4)$ with a low decomposition temperature was used as a single precursor. Three types of substrates were employed for comparison: 1) SiC(MBE)/Si(001) off-axis, 2) bare Si(001) and 3) a-SiO_2/Si(001). Prior to the LPCVD growth the MBE carbonized films and Si(001) wafers were *in-situ* etched in H_2 atmosphere during 5 min at 1100°C and 200 Torr. Besides removing the native oxide layer, H_2 also favors the elimination of any excess C present on the surface of the carbonized films. Characterization of the LPCVD thin films was performed by SEM, TEM, X-ray diffraction and Microprobe analysis.

Since conventional X-ray θ-2θ scans do not clearly differentiate between polytypes in the SiC system, special emphasis is put into the X-ray texture measurements to determine the crystallinity and preferred orientation of the grown films. As expected, under the same CVD growth conditions the mode of growth of the LPCVD/MBE samples proceeds dramatically different than previously reported samples grown on Si(001) substrates (Fig. 1a). In those samples a thin SiO_2 buffer layer was introduced to reduce and control the stress of the SiC films. The {111} pole figure of a typical polycrystalline SiC film grown on a-SiO_2/Si(001) shows a pronounced maximum at the center of the stereographic plane indicative of preferential

orientation of the {111} planes induced by twinning in this direction. The distribution of crystal orientation exhibits rotational symmetry about an axis normal to the substrate surface. On the contrary, the pole figure of the first diffraction peak of a typical LPCVD/MBE sample (Fig. 1b) shows a remarkably different pattern with intensity maxima in well defined angular locations due to the in-plane orientation of the sample. A preliminary analysis of the pole figures of the hkl Bragg planes present in the θ-2θ scans is compatible with a heavily twinned cubic structure and with the presence of 3C and 6H polytypes. A combination of both cases seems to be the most probable since twinning may be enhanced by the carbonized layer and the existence of a 6H polytype in these samples is unambiguously confirmed in the X-ray pole figure of the (10-11) diffraction peak of the 6H structure (Fig. 2).

The influence of the MBE process parameters on the LPCVD mode of growth and quality of the SiC films will be discussed.

Financial support from CICYT Project MAT95-0875 and from Spanish-Greek Agreements is acknowledged.

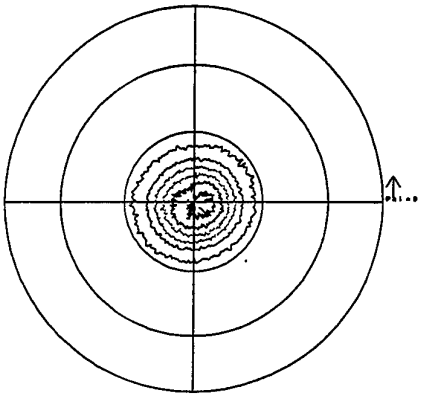

Fig. 1a. {1 1 1} pole figure of a SiC film on a-SiO_2/Si(100)

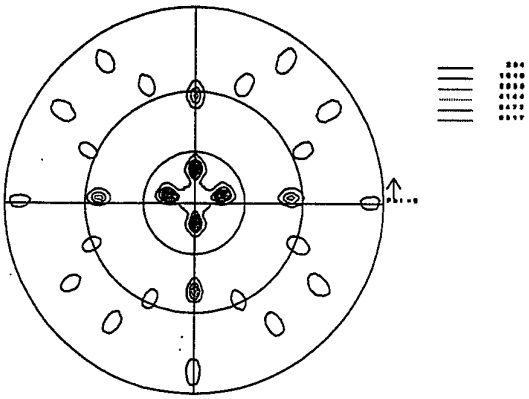

Fig. 1b. {1 1 1} pole figure of a SiC film on carbonized Si

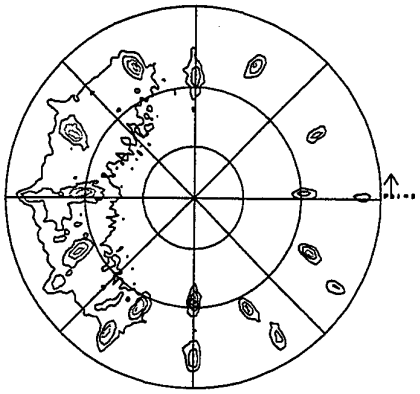

Fig. 2 {1 0 -1 1} pole figure of a SiC film on carbonized Si

INFLUENCE OF THE HEATING RAMP ON THE HETEROEPITAXIAL GROWTH OF SIC ON SI

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The carbonisation of silicon substrates prior growth as a separate process or during the heating-up cycle is common method in deposition of heteroepitaxial SiC layers. Despite the formed ultra thin film is often called "buffer layer", its main task is the formation of a diffusion barrier for silicon. Actually these layers were not able to compensate the large mismatch, especially the differences in thermal expansion. A diffusion of silicon from the substrate to the growth surface causes a wide variety of defects, most striking are the well known voids beneath the layer. It can occur only at defects due to the low diffusion coefficient. Consequently a "good" layer has to prevent such a diffusion process and the diffusion coefficient of silicon is a criterion for the quality of the grown layer (fig. 1).

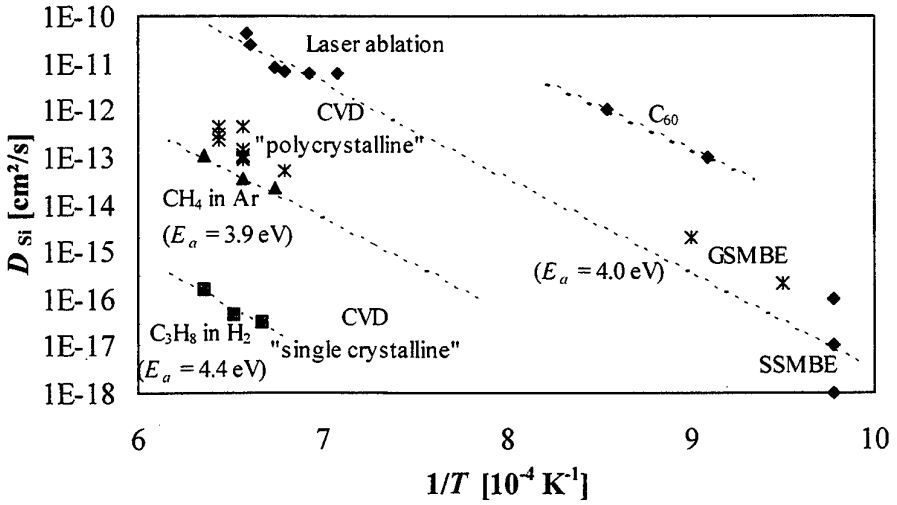

Fig. 1 Comparison of the diffusion coefficients of Si in the grown SiC layers as estimated from the layer growth kinetics at growth temperatures for different deposition techniques

In most cases the grain boundaries are the largest defects acting as diffusion paths. To grow a diffusion barrier a two dimensional nucleation and growth is expected to be necessary. However, for the existing large lattice mismatch two dimensional nucleation is unlikely. Nevertheless the

possibility to grow ultrathin atomically flat layers by different techniques was already shown. Such a growth occurs only at high supersaturations (low temperature / high carbon flux) which represents a very narrow range of process parameters, most of all the growth temperature. In some cases they were not reproducible adjustable and in dependence on the reactivity of the carbon source there is the probability of unwanted graphite deposition. An alternative is to go through the critical conditions with a well defined heating-up velocity. However, there are only few systematically investigations. In this work we compare the influence of the heating cycle in a (hydro-) carbon flux for two with regard to the process conditions very different techniques: (i) rapid thermal chemical vapour deposition (RTCVD) using propane in hydrogen at normal pressure and high temperatures (1200 ... 1300°C) and (ii) solid source molecular beam epitaxy (SSMBE) with pyrolytic graphite in an electron gun evaporator at low temperatures (500 ... 800°C) and an effective carbon flux to the silicon surface which is some order of magnitudes lower as in the case of the RTCVD conditions. There exists another peculiarity for the SSMBE conditions. The application of hydrocarbons allows to use a self limiting process in carbon incorporation because of the high ratio between the reaction probabilities on a silicon or carbon site. In contrary, these ratio in the reaction probability and/or sticking coefficient for elemental carbon is much smaller. Therefore hydrocarbons can be supplied with excess for the growth of SiC while the flux of elemental carbon has to be adjusted very accurately. For that case we will present a method to determine a temperature-time programme in dependence on the carbon flux.

SURFACTANT-MEDIATED MBE GROWTH OF SiC ON Si (100) SUBSTRATES

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Heteroepitaxial growth of cubic (β) SiC on Si substrates has been widely investigated in the past. The large mismatches in lattice parameter (about 22%) and thermal expansion coefficient (about 8%) precludes any conventional solution and leads to the growth of poor quality β-SiC layers. Crack-free films were produced by the two step growth approach i.e. conversion, at low temperature, of Si surface to β-SiC by exposing it to a carbon-containing precursor (carbonization process) followed by a normal deposition step at higher substrate temperature. The driving idea was the formation of an initial continuous and epitaxial layer of β –SiC in which the resulting strain is released through misfit dislocations. In this case, an extra β-SiC plane is introduced in every four silicon lattice planes thus creating a misfit dislocation. The localization of the misfit dislocations is considered to occur at the interface where there are anchored. The second step could be considered as an homoepitaxial growth step resulting in improved material quality. However, a simple calculation of the misfit shows that it is not completely removed by the above procedure and residual strain is present during the initial stages of growth. The local variations of the strain at the SiC/Si interface result in a high number of stacking faults and twins and in most cases in a small-angle misorientation of the initial β-SiC island nuclei [1,2]. Moreover, it has been shown theoretically [3] and experimentally [1] that the carbonization process is not a single epitaxial process but rather a strong chemical reaction where interdifffusion plays an important role. «Deceleration» of this chemical reaction during the carbonization step by chemical passivation of the Si surface would resolve many of the above problems. For this purpose, it is proposed hereby to apply the surfactant-mediated growth approach [4]. Hereby, the term surfactant do not refer only to materials wetting the substrate's surface and thus reducing the surface tension, but more generally to materials that lower the surface energy and change the kinetics of growth while they float on top of the growing material. More precisely, it is proposed to perform Ge monolayer coverage of the Si (100) surface.

There are a few requirements for a material to act as a good surfactant[5]: (a) the binding of the surfactant atoms to the substrate should not be so strong as to cause them difficulty in segregating to the surface during growth, (b) the surfactant must produce a chemically passive surface and (c) the surfactant should enhance surface diffusion of the newly deposited atoms.

It is well known that Ge forms dimers on the Si (100) surface and (2x1) is the more stable reconstruction. Thus, the Ge atoms have strongest bonds with the other Ge atoms than with the Si atoms of the substrate. This implies that the Ge atoms will not have, in principle, any difficulty in segregating to the surface during growth on top of the newly deposited carbon atoms. Furthermore, C atoms are smaller than Ge ones and it has been theoretically shown [6] that there is a repulsive Ge-C interaction and a preferential C-C interaction in a Si-Ge-C lattice.

Moreover, the Si-Ge system produces a lattice constant larger than that of Si and results in a smaller bandgap than that of Si. When grown on Si, these layers are under compressive strain.

Therefore, use of SiGe or $Si_{1-x-y}Ge_xC_y$ layers could accommodate elastically the above mentioned residual strain following the carbonization process.

Eventual partial incorporation of Ge atoms would not affect the electronic properties of the grown films as it is isovalent alloying element with C and Si. Therefore, no extra-doping is expected in this case.

The structure that it is proposed to grow by solid source MBE is the following:

- Monolayer deposition of Ge atoms on Si(100) surface for the reasons explained above.
- Deposition of carbon atoms for the formation of 5-6 monolayers of β-SiC by the carbonization process. The thickness of the carbonization layer should not exceed this value in order to limit the interdiffusion and avoid the formation of pits[1]. The growth temperature should be a trade-off between the minimum temperature for obtaining the carbidic phase and the maximum one for effective surfactant effect. A temperature of 750-800 C should satisfy the above requirements.
- An optional step of $Si_{1-x-y}Ge_xC_y$ layer formed at 500 C would accommodate the residual strain. A typical value of the residual-strain induced misfit is 1% and the minimum value of Ge composition x~0.25 for y=0 would be necessary.
- The final step of β-SiC deposition by simultaneous supply of silicon and carbon should start at 900 C as the alloys of the $Si_{1-x-y}Ge_xC_y$ type exhibit a thermal stability up to this temperature only [7]. However, use of higher temperatures will not introduce dislocations at this level because it is well known that strain relaxation proceeds in this case by the formation of SiC precipitates [7].

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CVD GROWTH OF 3C-SIC ON SOI(100) SUBSTRATES WITH OPTIMIZED INTERFACE STRUCTURE

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Heteroepitaxially grown 3C-SiC on silicon is considered to be suitable for high temperature sensor applications like pressure sensing in combustion engines [1]. In addition to the lattice and thermal mismatch of the material system the electrical properties of 3C-SiC on Si suffer from significant substrate leakage currents at elevated temperatures. Therefore, the usage of SOI (Silicon On Insulator) substrates is favourable due to the insulating properties of the buried oxide layer.

Outdiffusion effects of Si from substrate leading to cavities at the interface are commonly reported for 3C-SiC heteroepitaxy [2]. This cavity formation can be increased using SOI substrates, because the thin Si layer on top of the buried oxide can be locally consumed through the whole layer thickness using non optimized carbonization conditions. Hence, decomposition of the underlaying oxide causes an extension of the cavity into the oxide.

We succeeded in growing 3C-SiC on SOI(100) substrates with an essential defect-free interface structure. As substrates 4 inch bonded SOI-wafer from Soitec S.A., France, were used. Prior to growth they were cut to 22*44 mm samples. After a standard wet chemical etching step they were loaded into a horizontal water-cooled LPCVD-reactor made of fused silica [3]. Carbonization of the Si top-layer surface was performed by applying a relative slow temperature ramp of 200°C/min from 600°C to 1280°C under a constant flow of 1 sccm propane in 7 slm hydrogen at a total pressure of 150 mbar. Subsequently, 3C-SiC was grown from silane and propane diluted in hydrogen with an atomic ratio of Si/C=0.3 at the carbonization temperature.

From cross-sectional TEM (Transmission Electron Microscopy) investigations the sequence of the different layers is clearly depicted in Fig. 1. The thickness of the 200 nm Si top-layer after carbonization and growth of the epitaxial layer remains almost unchanged. During the carbonization step only about 30 nm of the Si top-layer is consumed and a high density of SiC nuclei is formed resulting in a rapid sealing of the surface as reported for Si substrates [4]. Consequently, the formation of voids is suppressed completely.

In the Si top-layer dislocations (D) can be detected. They are induced by the strain relaxation of the mismatched 3C-SiC/Si(100) system. But the buried oxide is not affected by the growth procedure. The 1.3 µm thick 3C-SiC CVD-layer reveals typical defects of 3C-SiC grown on on-axis Si(100). Antiphase boundaries (APB) are propagating through the thin film. Microtwins (µT) along inclined {111} planes can be observed. The defect density substantially decreases with increasing layer thickness because of an annihilation of APBs at twin boundaries.

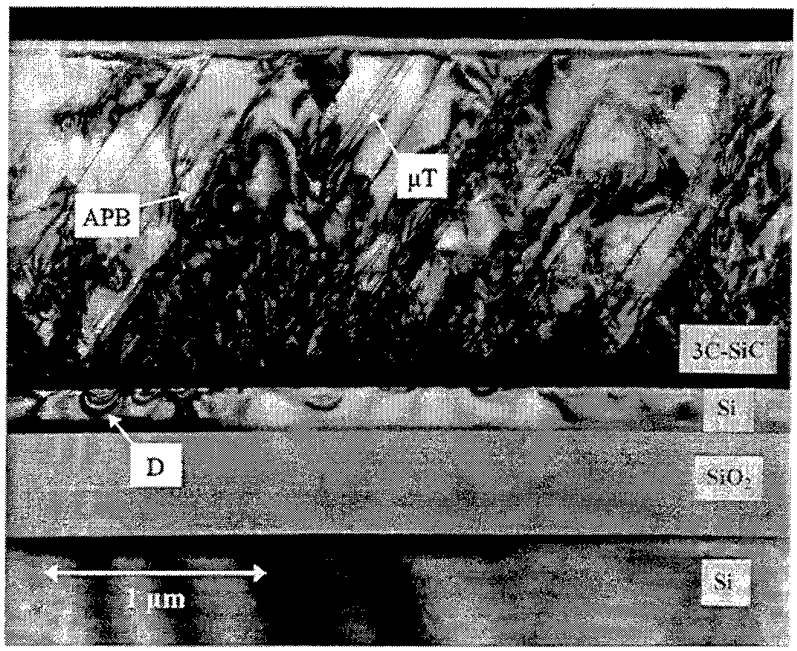

Fig. 1: Cross-sectional low-magnification TEM image of 3C-SiC on SOI(100) with optimized interface structure. No voids in the Si layer and the oxide can be detected.

In conclusion, we have shown that with appropriate carbonization conditions void free 3C-SiC can be grown on SOI(100) substrates. The defect structure and density are comparable to state of the art heteroepitaxially grown 3C-SiC thin films on Si. The buried oxide is totally unaffected by the SiC growth which is the requirement for the desired vertical electrical insulation at high temperatures.

Acknowledgements:

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INFLUENCE OF THE SILICON OVERLAYER THICKNESS OF SOI UNIBOND SUBSTRATES ON β-SIC HETEROEPITAXY

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Introduction

Cubic Silicon Carbid (SiC) thin films exhibit extraordinary electronical and chemical properties. In combination with micromachined silicon structures they yield the realisation of robust sensors operating at high temperatures and in chemical harsh environments. For the application of SiC as piezoresistors e.g. in high temperature pressure microsensors dielectric insulation to the substrate is necessary to eliminate the influence of the silicon and to avoid short circuits. To achieve this, SiC was deposited on thin crystalline Silicon (Si) overlayers (SOLs) on SiO_2.

The present paper describes a material preparation process for SOI to get a SOL thickness variation between 15nm and 205nm and a low temperature growth process based on the precursor gas methylsilane. Structural and electrical properties of SiC were compared applying different thick SOLs.

Preparation of SOI substrates

Commercial available standard UNIBOND SOI substrates from SOITEC [1] were used for the experiments. The original SOLs of the SOI material system were 205nm thick, [100] orientated and have a boron doped p-type resistivity of 15-22 Ωcm. The buried oxide layer (BOX) was 400nm and the bulk silicon 500μm thick. Different series of thinning experiments were performed to investigate the influence of silicon overlayer thicknesses on the quality of the subsequent deposited SiC films.

The original 205nm thick SOL was oxidised in a wet oxidation process at 1050°C in an Eurotherm tube furnace at atmospheric pressure. The thickness ratio of the SiO_2 layer to the consumed Si is known to be 2.273 to 1 [2]. The oxide is removed by a subsequent wet etching process in a HF etchant mixture (Merck: Silicon dioxide etchant, Nr.: 1.07944) at room temperature. The thinned crystalline SOLs are very homogeneous, show a mirror like surface and are smooth over the whole substrate. No defects could be observed using XTEM analysis. Ultrathin SOLs with minimal thickness down to 15nm can be prepared using this sacrificial oxidation technique.

Growth process

A low temperature growth process with methysilane [3][4] was applied. Details are described elsewhere [5]. The native oxide was removed by an HF dip followed by a water rinsing step. No further cleaning step was applied and the substrate was inserted directly into the cold reactor chamber. To achieve high quality SiC on SOI layers the conventionally used hydrogen cleaning-step was left out whereas fast heating and cooling ramps within the process turned out to be necessary. The deposition process starts with a 30sec

carbonisation step in an ethylene/argon gas mixture at 1220°C and 0.2mbar. This results in a 7nm thick crystalline buffer layer. The subsequent deposition took place at 1200°C and 0.5mbar with a resulting growth rate of 4.4µm per hour. A dilution ratio of methysilane/hydrogen of 2/100 was applied.

Results and discussion

Figure 1 shows the 3D texture in [111] direction of a SiC-film, grown as described above. Four peaks, which are evident for a cubic material, were obtained. The absence of any further reflexes shows that there are no disorientations. The SiC films are single crystalline. The films appear mirror like and exhibit a roughness of about 50nm, obtained by AFM.

Figure 2 shows the FWHM of the 200 reflex of 2.3µm thick SiC on 18nm, 100nm and 200nm thick SOLs. Using a 200nm thick SOL, a FWHM of 0.311° was obtained. This value is slightly higher than 0.269°, measured on SiC, grown on bulk Si [5]. Using a 100nm thick SOL, a FWHM of 0.263° was obtained. This value is smaller than the FWHM of SiC on bulk Si. By decreasing the SOL thickness to 18nm, the FWHM increases drastically to 0.51°.

This results could be explained by two opposite effects. On the one hand the growth on thin SOLs is preferred due to decreasing tensile strain and a decreasing influence of the lattice mismatch. On the other hand SOLs show increasing temperature instabilities with decreasing layer thickness. This gives evidence for the existence of a SOL thickness optimum, which strongly depends on the growth parameters.

Series of SiC deposition experiments on SOLs from ultrathin to bulk material with carbonisation layers of different thicknesses and varying growth parameters were performed. Comprehensive data using X-ray, AFM, Hall and Constant Photocurrent Method (CPM) analysis will be presented at the conference.

The development of a smarter deposition process, not affecting even ultrathin SOLs of SOI substrates, is in good progress and appears to be a promising technique to achieve further improvement of β-SiC heteroepitaxy.

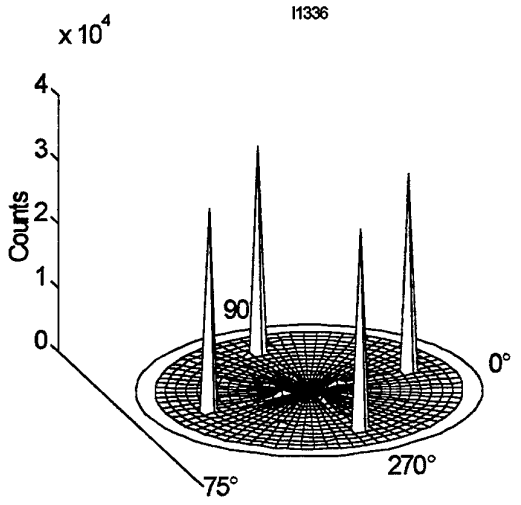

Figure 1

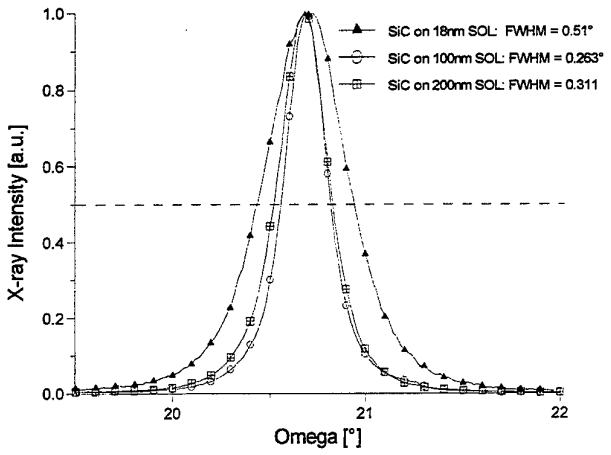

Figure 2

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Investigation of porous silicon as a new compliant substrate for 3C-SiC deposition.

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In order to master the growth of cubic SiC on large size silicon wafers, the need for an efficient compliant substrate is now a well established matter [1]. This would help producing 3C-SiC/Si sensors for the automotive industry as well as hetero-epitaxial layers of GaN/SiC/Si [2] with improved optical properties. Along this line, 3C-SiC on SOI (Silicon On Insulator) material has been very much investigated but, still, has demonstrated limited success.

Basically this is because of the poor thermal stability of the SOL/BOX (Silicon OverLayer / Buried Oxide Layer) material system in the temperature range requested for 3C-SiC deposition [1]. As a consequence, while still allowing a limited amount of stress relaxation, in many cases the oxide starts to decompose and numerous cavities appear. In a few cases, the full layer even peals off.

An interesting way to remain compliant without using any BOX would be to use porous silicon (p-Si). However, up to now, no investigation of 3C-SiC deposited on p-Si has been reported and no comparison with 3C-SiC deposited on SOI has been made. This is done in this work.

3C-SiC was grown under atmospheric pressure conditions by carbonization and chemical vapor deposition (CVD) using propane and silane with a SiC-coated graphite susceptor. The deposition temperature ranged from 1330 to 1350°C and the typical growth rate was ~2 μm/hr. For comparison purpose, cubic SiC was also grown on standard SIMOX and bulk silicon using the same experimental protocol.

At Spire, samples were analyzed using H^+ and He^+ RBS, SIMS, TEM, and X-ray diffraction techniques. In Montpellier, selected samples were also characterized by double X-ray diffraction, infra-red reflectivity, micro-Raman spectroscopy, and low-temperature photoluminescence. Altogether our experimental results show the following :

- Focusing on the DDX rocking curves collected for the {200} reflection of SiC and the {400} reflection of Si and comparing with the standard case of 3C-SiC/Si, we find a net improvement in the relative values of Full Width at Half Maximum (FWHM). Indeed, starting from usual (heteroepitaxial) material, both values decrease when going to 3C-SiC/p-Si.

• Most of the improvement comes from the narrowing of the substrate {400}-Si reflection. This shows that the finite porosity of the starting material acted like a dislocation filter and helped protecting the bulk of the Si wafer.

Inspection of the SiC layer morphology evidences growth irregularities which resulted in large rectangular terraces of micrometric size. This is best seen in Fig.1. Such mesa-like structures are usually not found on 3C-SiC/Si or 3C-SiC/SIMOX and we believe that they come from a non homogeneous carbonization process of the porous Si layer.

To get an average of flat and step-like structures, infrared reflectivity measurements have been done. They were modeled using a standard transfer matrix method and, from the comparison between theory and experiment, we find about 25% flat and 75 % rough.

To get a closer look into the strain repartition in this new type of hetero-epitaxial material, micro-Raman spectra have been collected in the transverse <X(Y-)-X> configuration. Comparing with 3C-SiC/Si and 3C-SiC/SOI, we have found results intermediate between 3C-SiC/Si and 3C-SiC/SIMOX. This confirms the results of the DDX investigation.

Finally, we have focused on the best samples and performed LTPL (Low Temperature PhotoLuminescence) experiments. We resolved broad near-band-edge (NBE) structures with defect-related (W) bands but no real fine structure. The nice point is the improvement noticed when going from 3C-SiC/Si to 3C-SiC/SIMOX.

To conclude, we believe that we have demonstrated the feasibility of 3C-SiC/p-Si hetero-epitaxial deposition. Better results can still be found when using SIMOX substrates but, when properly optimized, we believe that this may result in SiC layers with state of the art morphology.

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Fig. 1: Plane view of 3C-SiC deposited on porous silicon.

INTRINSIC STRESS MEASUREMENT OF AS-DEPOSITED POLYCRYSTALLINE SILICON CARBIDE THIN FILMS

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Controlling the final stress of a thin film is of crucial importance for micromachining purposes and for membranes fabrication. Polycrystalline 3C-SiC layers, 0.5-2 μm thick, have been deposited on a-SiO_2/Si(001) substrates in a hot wall LPCVD reactor using tetramethylsilane (TMS) as an organometallic precursor diluted in H2. The deposition temperatures have been varied in the narrow range of 1050 °C-1150 °C. A microstructural characterization of the films has been performed by using SEM, TEM, XPS, XRD and texture analysis by means of pole figures. Two techniques have been used to measure the average stress in the SiC films: a laser deflection technique based on determining the change in curvature induced on the substrate due to the grown film and a strain measurement technique based on direct measurements of interplanar spacings in the film using the so-called x-ray diffraction $\sin^2\psi$ method.

SiC thin films are stoichiometric and present a columnar morphology with grain diameter in the range of 100-400 nm at the top surface. Films grown at low (1080 °C) temperatures show a strong preferred orientation along the (111) direction, but as the growth temperature is increased (1105 °C, 1130 °C), the XRD θ-2θ scans and the pole figures reveal a loss of texture which is related to a change in the growth regime.

For a direct comparison of the stress results obtained with both techniques, some considerations have to be taken into account. For instance, the presence of texture and shear stresses introduces deviations from the ideal linearity of the strain vs. $\sin^2\psi$ plot, difficulting an interpretation of the X-ray stress measurements.

It is observed that the average stress in the SiC films can be varied from compressive (-300 MPa) to tensile (300 MPa) by changing the deposition conditions, mainly temperature and gas flow. In particular, textured films are compressively stressed and as the preferred orientation disappears, the films become tensile. The thermal mismatch between the SiC layer and the substrate induces a relatively constant tensile contribution to the total stress over the temperature range investigated. This suggests that film growth and thus, the induced intrinsic stress are extremely sensitive to small variations of the deposition parameters.

The authors are indebted to the Centro Nacional de Microelectrónica (CNM-CSIC) for the laser deflection stress measurements and to the Serveis Cientificotècnics of the Universitat de Barcelona for the TEM, XPS and XRD measurements. Financial support from CICYT by Project No MAT95-0875 is acknowledged.

HIGH TEMPERATURE PIEZORESISTIVE ß-SIC-ON-SOI PRESSURE SENSOR WITH ON CHIP SIC THERMISTOR

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Cubic silicon carbide, heteroepitaxially grown on SOI (Silicon On Insulator), is a promising material for the development of micromechanical high temperature devices such as pressure sensors [1]. Using single crystalline ß-SiC piezoresistors, which have a higher Gauge factor than polycrystalline SiC [2,3], provide a high output signal of the pressure sensor. However, for the operation of the pressure sensor over a wide temperature range it is necessary to compensate for the temperature dependence of sensitivity and offset voltage. Therefore the measurement of the temperature is necessary on the sensor chip. This paper reports about a piezoresistive ß-SiC-on-SOI pressure sensor with an on chip polycrystalline SiC thermistor.

For the fabrication of the SiCOI-material system (Silicon Carbide On Insulator), a n-type ß-SiC film with a thickness of 1.1 µm was deposited by Daimler-Benz Frankfurt on a <100>-oriented SOI substrate (UNIBOND) from SOITEC, France,. The ß-SiC film was characterized by Hall measurements, TEM-analysis and X-ray diffraction. The investigations show a good single crystal quality of the ß-SiC film and a reliable electrical isolation by the buried oxide layer from the substrate at temperatures up to 673K. However, the ß-SiC film proved not to be applicable to on chip temperature measurements. The sheet resistance decreases at temperatures between 100K and 400K, but increases for higher temperatures (Figure 1). In comparison, the temperature coefficient of the sheet resistance of a polycrystalline SiC film is negative between 273K and 673K (Figure 1). Therefore a 2.5 µm thick polycrystalline SiC film was deposited on the thermally oxidized SiCOI substrate by Daimler-Benz Munich. The temperature coefficient of the sheet resistivity between 273K and 673K is $-1.63 \cdot 10^{-3} K^{-1}$.

Based on these layer structures a piezoresistive pressure sensor has been developed using Finite Element Analysis (FEA). The design was optimized for a circular diaphragm with center boss (Figure 2). Standard technologies were used to fabricate the SiCOI sensor chip. Characterization of the sensor up to 673K is currently in progress. Results of the characterization oft the sensor at temperatures up to 673K will be presented.

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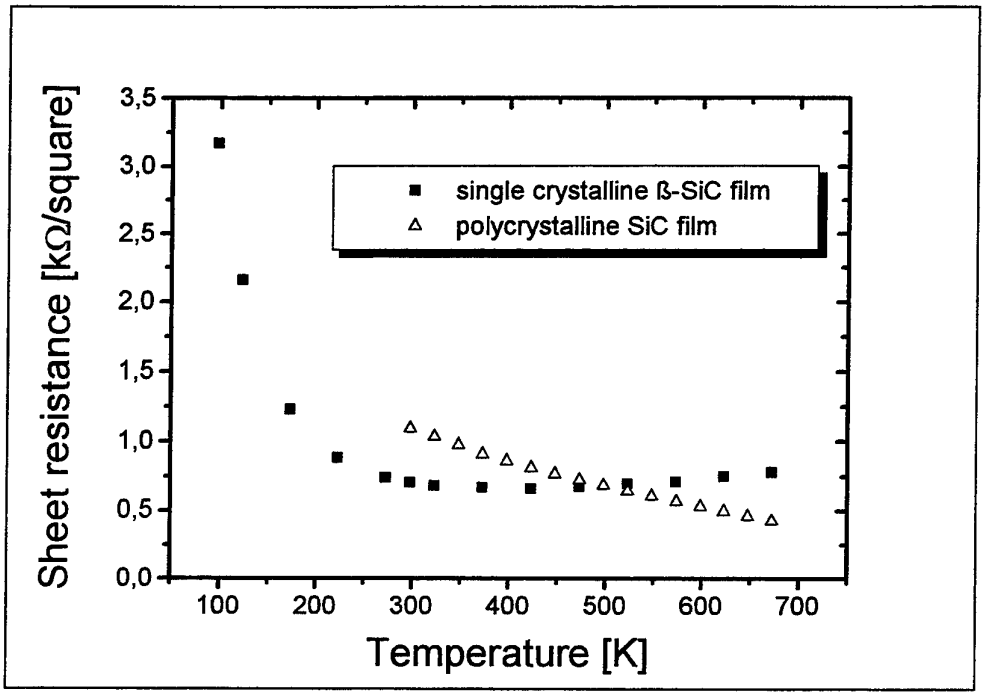

Figure 1: Temperature dependence of the sheet resistance of single crystalline ß-SiC and polycrystalline SiC films up to 673K.

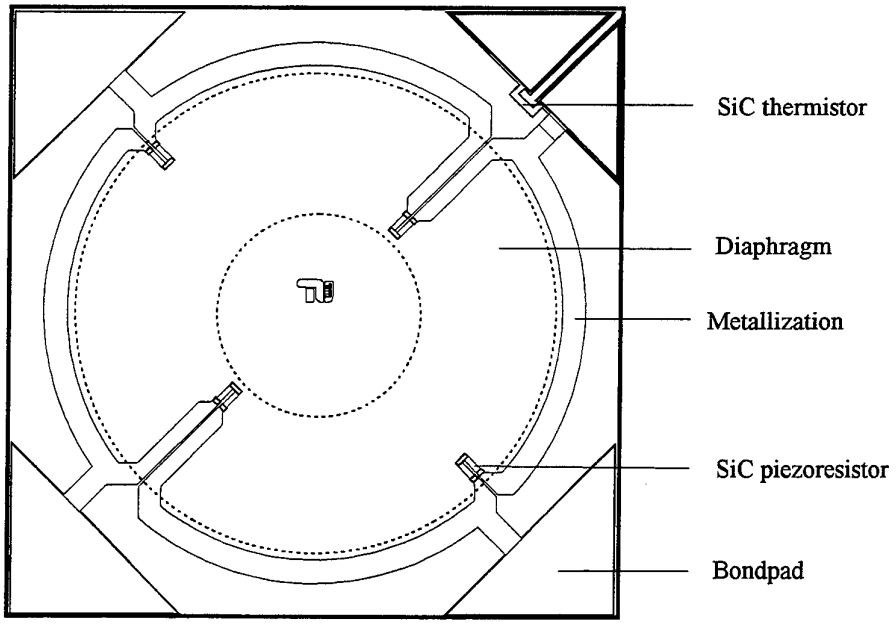

Figure 2: Design of the SiCOI pressure sensor chip with on chip polycrystalline SiC thermistor.

The characterization of the enhanced thermal oxide layer on 6H-SiC by ion irradiation

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Thermal Oxidation is an essential technique in processing of SiC devices. Up to now, several investigations have been made on the thermal oxidation for the Si- and C-faces of SiC(0001). It was reported that a high dose ion-irradiation into the Si-face of 6H-SiC caused the increase of the oxidation rate [1-3]. In the present work, we studied the characterization of enhanced thermal oxide layer on ion-irradiated 6H-SiC.

We employed commercially available n-type 6H-SiC(0001) wafers with 10 μm thick epitaxial layer. The donor densities of the epitaxial layers and substrates are 1.8×10^{18} and 8.0×10^{15} N/cm^3, respectively. $^{18}O^+$ ions with energy of 30 keV and $^{28}Si^+$ ions with energy of 25keV were irradiated the Si-face of 6H-SiC with doses of 5.0×10^{16} ions/cm^2 at RT. The irradiated samples and non-irradiated sample were thermally oxidized in a quartz tube at 1100℃ for 60-300 min under the wet oxygen atmosphere. The post oxidation anneal was performed at 1200℃ for 30 min in Ar ambient.

The thickness of oxide grown layer on non-, Si^+- and O^+-irradiated SiC, which were then thermally oxidized for 180 min, was found to be 35nm, 120nm and 187nm respectively by using an ellipsometer. The thickness of the oxide layers were not changed independent on oxidation time for 60-300 min. Fig. 1 and 2 shows the SIMS measurement and the cross sectional TEM image for the sample irradiated with a dose of 5×10^{16} O^+/cm^2 and then oxidized at 1100℃ for 60 min, respectively. SIMS analysis shows that within SiO_2 layer the ^{18}O isotopic ratio, i.e., the intensity ratio ($^{18}O/(^{18}O+^{16}O)$), is flat and around 0.2 %, the natural isotopic abundance. An abrupt interface and a good crystallinity of the substrate near the interface are shown in Fig.2. The disorder image in surface region of SiC layer is possibly artifact due to the sample preparation and/or the residual damage induced by ion-irradiation after thermal oxidation.

In order to study the electrical properties of the oxide, MOS capacitors were formed by evaporation of aluminum dots with 300 μm diameter. An ohmic contact of nickel was evaporated on the backside of wafer. The breakdown voltage and the resistivity of the enhanced oxide layers were 1-4 V/cm and $1\text{-}5\times10^{12}$ Ωcm,

respectively. C-V characteristic of the MOS structures were measured at frequency 1 MHz at room temperature. Fig.3 and 4 shows C-V plots measured for the oxide layer on Si^+-irradiated SiC without and with post oxidation annealing and the oxidation time dependence of enhanced thermal oxide layer on Si^+-irradiated SiC with post oxidation annealing, respectively. The post oxidation annealing was effectively improved the electrical properties of enhanced oxide layer on irradiated SiC sample. And the oxidation time also contribute the effective improvement of electrical properties for these samples. This result means that the residual damage induced by ion irradiation after oxidation exists in the SiO_2/SiC interface and this damage have a bad effect on the electrical properties of the oxide. Therefore, the post oxidation annealing and thermal oxidation for long time cause the removal and oxidation of residual damage to improve the electrical properties of the enhanced oxide layer.

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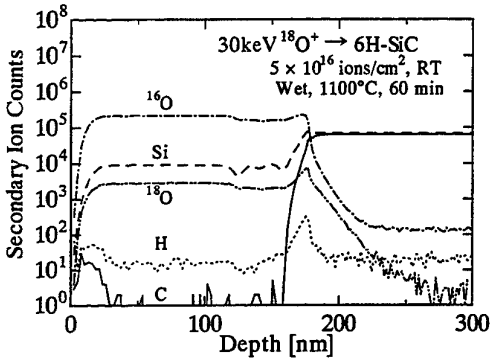

Fig.1 Elemental depth profiles measured by SIMS for 6H-SiC irradiated by 30 keV $^{18}O^+$ with a dose of 5×10^{16} ions/cm^2 and sub-sequently annealed at 1100℃ for 60 min.

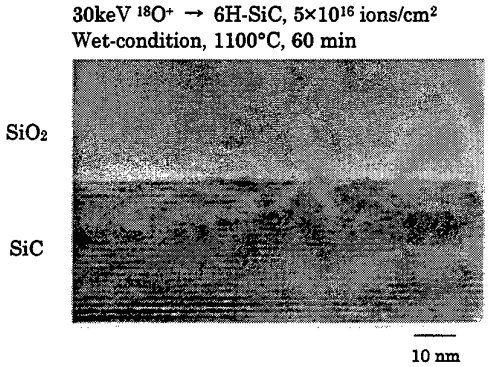

Fig.2 High resolution XTEM photograph of oxide/SiC interface for the sample irradiated by 30 keV $^{18}O^+$ with a dose of 5×10^{16} ions/cm^2 and then annealed at 1100℃ for 60 min.

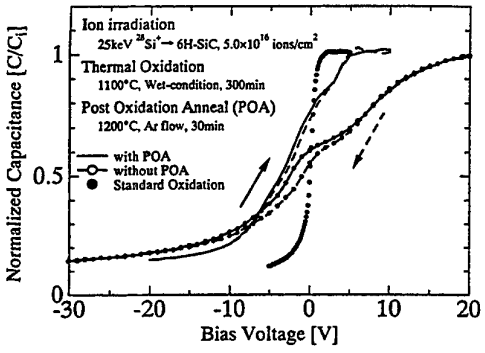

Fig.3 C-V plots of enhanced thermal oxide layer on Si^+-irradiated SiC without and with post oxidation annealing.

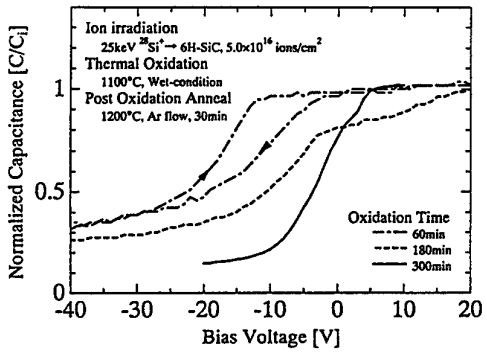

Fig.4 Oxidation time dependence of C-V plots of enhanced thermal oxide layer on Si^+-irradiated SiC with post oxidation annealing

Deep Level States at SiO_2/SiC Interface (•Si≡Si_3 Defect?)

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In this work, high temperature C-V and C-t measurements on 6H-SiC based MOS capacitors have been performed to reveal deep level states at the SiO_2/6H-SiC interface and to determine their possible role in surface carrier generation. The nature of surface traps revealed is discussed.

The samples used were n-type 6H-SiC epi-films grown by sublimation onto (0001)Si-faced Lely-type substrates. The carrier density in epi-films is about 10^{16} cm^{-3}. The films grown were oxidized at 1100°C using "chlorine" technique reported elsewhere [1]. Ion beam sputtered molybdenum and tungsten were used to form gate electrodes and back contacts, respectively.

C-t characteristics were recorded at different temperatures after switching the MOS capacitor from accumulation into deep depletion. The total time of inversion layer formation varied from several hours to several seconds with temperature increasing from 477 K to 546 K. To determine mechanisms of carrier generation, C-t curves were analyzed following the well known Zerbst technique. An electron-hole generation process in the semiconductor space-charge region has been detected, with an activation energy to be closed to the half-width of the 6H-SiC bandgap. Besides the generation with a lower activation energy of about 1.16 eV has been distinguished, which can be explained by the surface generation via deep level interface states, with density-of-state maximum to be at $E_C - 1.16$ eV.

To reveal deep level states at the SiO_2/6H-SiC interface, high-frequency C-V characteristics were measured at a high temperature (600 K) and analyzed by the Terman technique. The analysis showed that there exist deep acceptor-like interface traps with energies above the 6H-SiC midgap. The trap energy distribution is approximated well by a Gaussian peak with $D_t^{max} = 2\times10^{12}$ cm^{-2} eV^{-1} at $E_C - 1.16$ eV. One may conclude that these traps are responsible for the surface carrier generation in deep depleted MOS capacitor.

If it is assumed that there is a symmetrical peak below the midgap (such a peak was detected when studying SiO_2/p-SiC structures [2]) then the difference between the two maxima is about 0.55 eV. It is known that for SiO_2/Si system, the density of states associated with amphoteric •Si≡S_3- "oxidation defects" (P_b-centers) has two peaks in the Si bandgap that are located nearly symmetrically relative the midgap, namely acceptors at $E_V + 0.85$ eV (minus → 0 electron transition) and donors at $E_V + 0.25$ eV (0 → plus electron transition), with the correlation energy (i.e. the difference between the detachment energies of the first and second electrons) of about 0.55 eV [3]. It is reasonable to assume that the correlation energy for P_b-center is determined by its inherent structure. Then we may conclude that the deep surface states revealed in the present study for the SiO_2/6H-SiC system are similar in nature to the P_b-centers in the SiO_2/Si system.

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Hetero - epitaxial Growth of 3C-SiC Using HMDS by Atmospheric CVD

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Cubic silicon carbide (3C-SiC) possesses large energy gap, high electron mobility, high breakdown field, high saturation drift velocity, temperature stability, and chemical inertness. These excellent physical properties make 3C-SiC a promising material for electronic and optical devices under severe conditions, such as high temperature and high radiation environment. Due to the large mismatch (about 20%) between the lattice constants for 3C-SiC and Si, it is difficult to grow the large single crystal of SiC on Si substrate. But in recent years, single crystal of cubic SiC has been obtained on Si wafers.(1-3) In our experiment, reproducible single crystal heteroepilayer of cubic SiC has been successfully grown on n-type Si(100) ($2.5\times2cm^2$) by HMDS($Si_2(CH_3)_6$) + H_2 in atmospheric CVD system.(4) The heteroepitaxial growth process consists of three procedures. (a): Si substrate was etched by heating at 1175°C in HCl (9.5sccm) + H_2 (1SLM). (b): Si substrate was carbonized at 1350°C in C_3H_8(0.1sccm) + H_2 (1SLM). This procedure provides a so-called "buffer layer " for subsequent CVD. (c): After carbonization, HMDS gas was quickly introuduced for CVD at 1350°C. HMDS flow rate was 0.5sccm and H_2 flow rate was 2.5SLM. The growth rate of 3C-SiC film was 4.3μm/h. The CVD 3C-SiC epilayer on Si(100) were characterized and studied by X-ray diffraction (XRD), Raman scattering and photoluminecence(PL). The epilayer surface orientations of each sample were characterized by XRD, and were the same as the substrate (100) . The full width at half maximum(FWHM) of X-ray rocking curves became from 0.9 to 0.6 degree with increase of the film thickness dsic from 1.2 to 9.1μm, and indicated that the crystallinity of 3C-SiC epilayer became better with increase of film thickness.

Raman scattering and PL measurement are useful, senstive, precise, and nondestructive techniques for characterization and study of semiconductor materials. A great deal of information about stress, impurities, structural defects, energy band structure, and strains can be obtained from Raman scattering and PL. Fig.1 shows the Raman spectra for CVD 3C-SiC / Si (100) samples with a variation of dsic from 1.2 to 9.1μm. Raman scattering measurements(an argon-ion laser: 5145 Å) were performed at room temperature . For every sample, both the 3C-SiC TO(Γ) phonon near $796cm^{-1}$ and 3C-SiC LO(Γ) near $973\pm1cm^{-1}$ were recorded. With increase of dsic, LO(Γ) band becomes sharper and stronger, which is characteristic of single crystal SiC.(5) Fig.2 shows the Raman spectra of 9.1μm CVD film 3C-SiC / Si(100) and free standing film 3C-SiC / air without Si substrate. The line position of 3C-SiC LO(Γ) phonon shifts from $973.2075cm^{-1}$ to $974.5238cm^{-1}$ after Si substrate has been removed. This means that a lattice mismatch of 20% between 3C-SiC and Si results in that the tensile biaxial stress exists in CVD film on Si substrate, because a tensile stress in 3C-SiC film on Si(100) shifts the LO(Γ) phonon to lower enregy, and 3C-SiC film is nearly stress free when Si substrate is etched away. Raman shift between 3C-SiC on Si and free 3C-SiC film is $\leqq 2cm^{-1}$, it corresponds to a biaxial stress of 0.4 -1.0 GPa and an inplane strain of about 0.1% - 0.2%.(6)

Fig.3 shows the CVD 3C-SiC / Si PL spectra for dsic from 3.6 to 9.1μm at 11K. A He-Cd laser with a line at 3250Å was used for excitation source. The spectra have a nitrogen-bound-excition (N-BE) zero phonon line N0, one-, two-, and three replicas as well as D1 line.(7) The appearance of three-phonon replicas attests the high quality of these films. The D1 center no-phonon line at 1.97 eV appears and becomes stronger with increasing dsic , which is caused by divacancy related center.(7) It indicates that a large number of dislocations and other extended defects at interface region are reduced, and recombination due to point defect complexes becomes more prominent gradually. A broad band at ~2.15 eV (W band) is observed in each sample, which is resulted from the dislocation and extended defects near the interface region and a heavy deformation in these films.(7) The N-BE line structure is developed and becomes stronger in the greater film thickness, which demonstrates that the 3C-SiC film became complete with increase of film thickness.(7)

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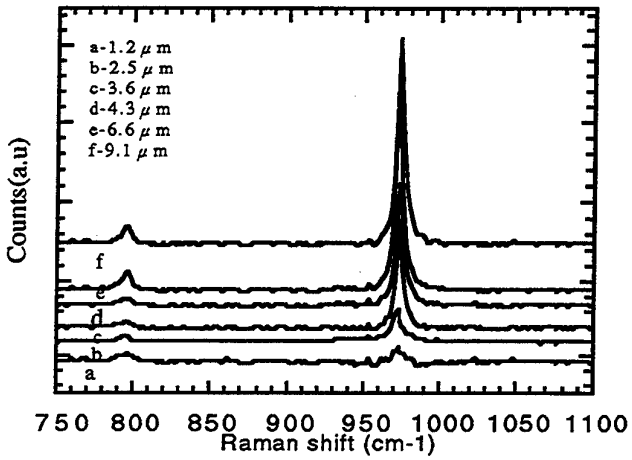

Fig.1The spectra of CVD 3C-SiC film on Si with a variation of d_{SiC} from 1.2 to 9.1μm

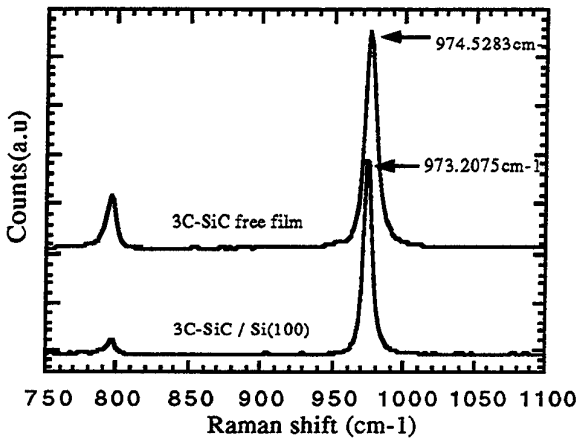

Fig.2 The Raman spectra of CVD film 3C-SiC / Si and free 3C-SiC film

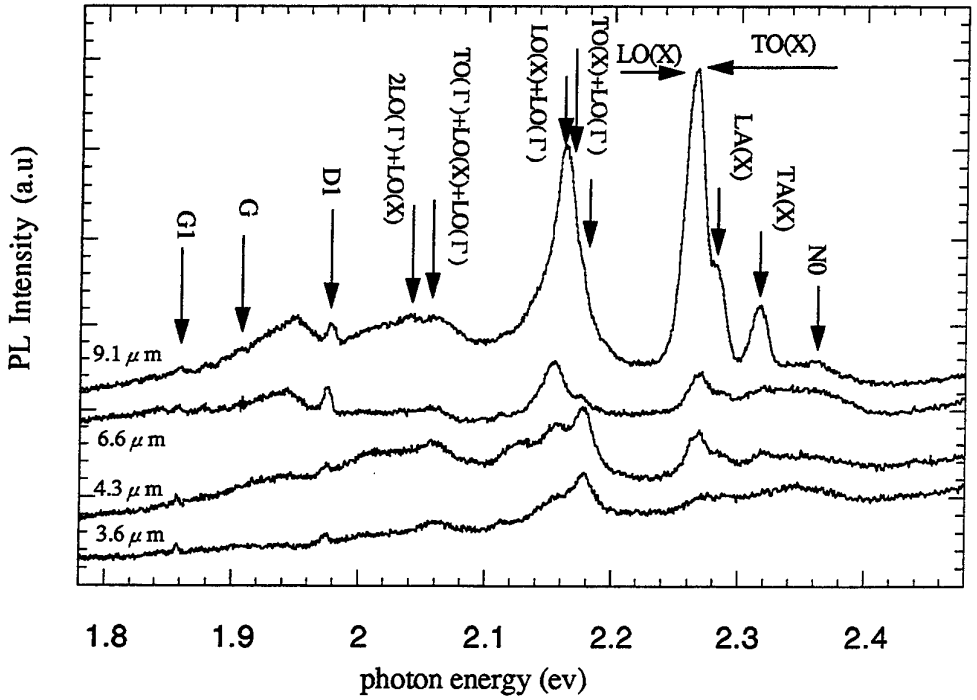

Fig.3 PL spectra of the CVD 3C-SiC/Si at 11K

Growth of Beta SiC on a Ceramic SiC Substrate a Thin Si Intermediate Layer

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Abstract

A major issue in the heteroepitaxial growth of 3C-SiC is the stress generated by the lattice and thermal mismatch of the substrate. We report on the growth of beta SiC on ceramic (polycrystalline) SiC. This substrate is thermally matched to single crystal SiC and allows the SiC to grown at temperature of 1500-1600C. Therefore, this substrate offers a significantly wider parameter space for optimization of cubic growth. In order to provide a crystalline template for growth, a novel wafer bonding scheme was used to produce ultra thin Si layers, which were wafer bonded to the ceramic substrate. Using this technology, single crystal layers as thin as 50nm can be produced. It should be noted that the ceramic substrates are inexpensive and this technique is easily scaleable up to 4 and 6 inches in diameter. Using this material, we have carbonized the thin Si layer and grown 3C-SiC at temperatures of 1350° C and higher. Details of the process for producing the SiC epitaxial layers as well as results of structural and electrical characterization of the films will be presented.

A new method for the electrical characterization of SiC films on SIMOX substrates

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The Silicon-On-Insulator materials are a promising and attractive alternative of substrates suitable for growing SiC layers [1]. The thin SOI films offer various advantages over the other substrates. Using SOI materials to grow SiC, we take advantage of their own features for high temperature electronics [2].
High dose and Low dose SIMOX substrates used for SiC film growth using a reactor CVD based method. The films have a thickness 2-3ìm and exhibit n type conductivity. The net doping concentration is nearly 10^{18} cm^{-3}. Ohmic dot-contacts with different diameters placed at different distances were deposited (Chromium/Titanium/Platinum/Molybdenum/Gold).
The characterization new method is based on the idea of pseudo-MOSFET technique [3] used to characterize Si films on SOI sunstrates. We replaced the two probes by ohmic contacts (Fig. 1). So, problems related with the surface roughness, cleanness and probe pressure are elinimated. The current between two ohmic contacts is measured as a function of the substrate bias keeping as parameters the bias between the contacts, the area and the distance between them. The substrate bias, playing the role of the gate bias in standard MOSFET, must be large enough in order to deplete and invert the interfaces.

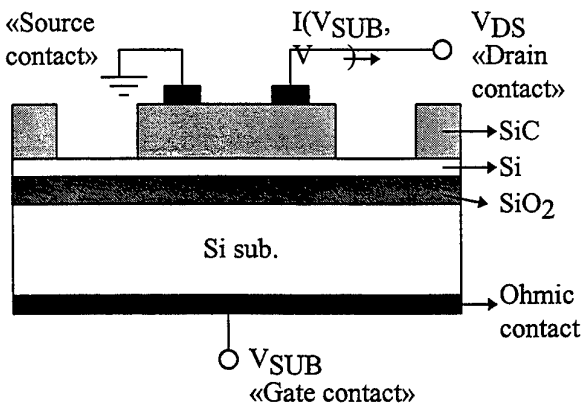

Figure 1. The schematic of the structures used in our studies.

Extending our technique, the current is measured as a function of temperature. By these measurements the «drain current's» activation energy is calculated, offering an indication about the mechanim which is responsinble for the layer's conductivity.

Minority and excess carrier characteristics of the SiC films were studied by utilizing white light illumination.

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Role of SIMOX Defects on the Structural Properties of β-SiC/SIMOX.

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To investigate the role of microscopic defects localized in the SOL (topmost Silicon OverLayer of SIMOX) on the structural properties of β-SiC on SIMOX, we have used three different wafers with SOL thickness ~ 150, 100 and 50 nm, respectively. As revealed by HF attacks, this modifies the initial concentration of defects in the SOL by orders of magnitude.

After SiC deposition, we have found that there is an increase of the density of cavities in the BOX (Buried OXide) layer which, roughly speaking, follows the trend in concentration of initial HF-defects.

In some cases, holes are also found. They appear at the center of rosette-like defects (located on top of BOX cavities) and run through the entire SiC layer. Finally, for the thinnest (initial) SOL thickness, the BOX and SOL become so severely damaged that in many cases they become indistinguishable.

Taking into account the diffusion of atomic species and various possible chemical reactions, the microscopic mechanism of holes and cavity formation is discussed.

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