

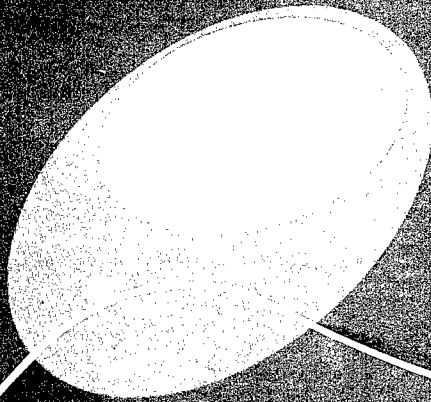
# LOAN DOCUMENT

DTIC ACCESSION NUMBER		PHOTOGRAPH THIS SHEET																					
	LEVEL		INVENTORY																				
DOCUMENT IDENTIFICATION																							
DISTRIBUTION STATEMENT																							
<table border="1"><tr><td colspan="2">ACCESSION BY</td></tr><tr><td>NTIS</td><td>GRAM</td></tr><tr><td>DTIC</td><td>TRAC</td></tr><tr><td>UNANNOUNCED</td><td><input checked="" type="checkbox"/></td></tr><tr><td>JUSTIFICATION</td><td><input type="checkbox"/></td></tr><tr><td colspan="2">BY</td></tr><tr><td colspan="2">DISTRIBUTION/</td></tr><tr><td colspan="2">AVAILABILITY CODES</td></tr><tr><td>DISTRIBUTION</td><td>AVAILABILITY AND/OR SPECIAL</td></tr><tr><td>A-1</td><td></td></tr></table>		ACCESSION BY		NTIS	GRAM	DTIC	TRAC	UNANNOUNCED	<input checked="" type="checkbox"/>	JUSTIFICATION	<input type="checkbox"/>	BY		DISTRIBUTION/		AVAILABILITY CODES		DISTRIBUTION	AVAILABILITY AND/OR SPECIAL	A-1		DATE ACCESSIONED	
ACCESSION BY																							
NTIS	GRAM																						
DTIC	TRAC																						
UNANNOUNCED	<input checked="" type="checkbox"/>																						
JUSTIFICATION	<input type="checkbox"/>																						
BY																							
DISTRIBUTION/																							
AVAILABILITY CODES																							
DISTRIBUTION	AVAILABILITY AND/OR SPECIAL																						
A-1																							
DISTRIBUTION STAMP																							
DATE RECEIVED IN DTIC																							
		DATE RETURNED																					
		REGISTERED OR CERTIFIED NUMBER																					
PHOTOGRAPH THIS SHEET AND RETURN TO DTIC-FDAC																							

H  
A  
N  
D  
L  
E  
  
W  
I  
T  
H  
  
C  
A  
R  
E

19981223 075

UNCLASSIFIED



NO DISTRIBUTION  
STATEMENT

NAVAL  
Tech. Rep.

APPENDIX 18

TECHNIQUES GENERATOR SOFTWARE DESIGN SPECIFICATION

FINAL SOFTWARE REPORT

DATA ITEM NO. A005

Reproduced From  
Best Available Copy

**INTEGRATED ELECTRONIC WARFARE SYSTEM  
ADVANCED DEVELOPMENT MODEL (ADM)**

7800987-18

PREPARED FOR  
NAVAL AIR DEVELOPMENT CENTER  
WARMINSTER, PENNSYLVANIA  
CONTRACT N62269-75-0070



ELECTROMAGNETIC  
SYSTEMS DIVISION

1 OCTOBER 1977

UNCLASSIFIED

APPENDIX 18  
TECHNIQUES GENERATOR SOFTWARE DESIGN SPECIFICATION  
FINAL SOFTWARE REPORT  
DATA ITEM A005

INTEGRATED ELECTRONIC WARFARE SYSTEM (IEWS)  
ADVANCED DEVELOPMENT MODEL (ADM)

Contract No. N62269-75-C-0070

Prepared for:

Naval Air Development Center  
Warminster, Pennsylvania

Prepared by:

RAYTHEON COMPANY  
Electromagnetic Systems Division  
6380 Hollister Avenue  
Goleta, California 93017

1 OCTOBER 1977

# RAYTHEON

RAYTHEON COMPANY  
LEXINGTON, MASS. 02173

CODE IDENT NO.

49956

SPEC NO.  
53959-HM-0412

SHEET  
1 OF

REV

TYPE OF SPEC

UNIT SOFTWARE DEVELOPMENT SPECIFICATION

TITLE OF SPEC

COMPUTER PROGRAM DESIGN SPECIFICATION FOR IEWS TECHNIQUES  
GENERATOR

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	H. McQuillen	8/5/76			

REVISIONS

CHK	DESCRIPTION	REV	CHK	DESCRIPTION	REV
9/13/76	Update Some Addresses In Flow HRM Charts & Add List III.	A			
12/20/76	Changes are made in two modules, SC Technique-Channel Assignment, and SC Technique-Channel Parameter Change or Dismiss. The updated flow charts are: Figure 7: Pg. 1-Added temporary storage (clear) for CFN. Pg. 2-Added insertion of CHAN in word 9, and insertion of CFN in word 12. Pg. 3-Added insertion of FN into CFN. Pg. 4-Added restore of FM generator status when RR/RGPO Gen. unavailable. Figure 8: Pg. 1-No change. Pg. 2-No change. Pg. 3-Added dismiss for RR/RGPO Gen., and for FM Gen. Pg. 4-Added insertion of CHAN in word 9, and of FM Gen no.	B		in word 12. Table A gives address and data for eight Technique programs to be stored in the Techniques Program memory. These are selected samples used during TGU integration and test.	

REVISION																				
SHEET NO.																				
REV STATUS OF SHEETS	REVISION																			
	SHEET NO.																			

**RAYTHEON**RAYTHEON COMPANY  
LEXINGTON, MASS. 02173

CODE IDENT NO.

49956

SPEC NO.

53959-HM-0412

SHEET

2 of 7

REV

IEWS SOFTWARE SPECIFICATION - COMPUTER  
PROGRAM DESIGN SPEC FOR TECHNIQUES GENERATOR

- 1.0 Scope
- 2.0 Applicable Documents
- 3.0 Requirements
  - 3.1 Function/Allocation Description
  - 3.2 Functional Descriptions
    - 3.2.1 Initialize Module
    - 3.2.2 Loop Module
    - 3.2.3 SC Write Fault Module
    - 3.2.4 SC Assignment-Frequency, ACN Module
    - 3.2.5 SC Technique-Channel Assignment Module
    - 3.2.6 SC Technique-Channel Parameter Change or Dismiss Module
    - 3.2.7 SC Program Control Module
    - 3.2.8 Channel-VCO Frequency Set-On Module
    - 3.2.9 Auxiliary Bus Frequency Module
    - 3.2.10 RAN-RAP Cover Module
    - 3.2.11 RAN-RAP Cover and Early Module
    - 3.2.12 RAN-RAP Cover and Late Module
    - 3.2.13 RAN-RAP Cover, Early and Late Module
    - 3.2.14 RGPO Module
    - 3.2.15 Frequency Update Subroutine
    - 3.2.16 Convert and Load Tuning Subroutine
    - 3.2.17 RAN-RAP A Version Subroutine
  - 3.3 Storage and Processing Allocation
  - 3.4 Computer Program Functional Flow
  - 3.5 Programming Guidelines

1.0 SCOPE

The computer program specified herein shall be entitled IEWS Techniques Generator Controller Program. The Techniques Generator Unit is part of the Integrated Electronics Warfare System, IEWS, being developed for test and evaluation to determine operational usefulness for advanced combat aircraft.

2.0 APPLICABLE DOCUMENTS

The following documents, form a part of this specification to the extent specified herein. In the event of conflict, the requirements of this specification shall govern.

AETD-XAV-1000

Experimental and Developmental  
Specification IEWS (Integrated Electronic  
Warfare System)

WS-8506

Requirements for Digital Computer  
Program Documentation

RAYTHEON SPECIFICATIONS

53959-HM-0410

Unit Hardware Development Specification -  
IEWS Hardware Spec. - Techniques  
Generator

53959-HM-0411

Unit Hardware Development Specification -  
IEWS Hardware Spec. - Transmitter  
Control - MAAS

53959-CD-1401

Interface Control Document Spec. -  
Daisy Chain Bus ICD

53959-JK-1003

Interface Control Document Spec. -  
Auxiliary Bus ICD

Eqpt. Division I

RP-16 Microprocessor

Eqpt. Division II

Computer Program Package Specification  
Raytheon RP-16 Relocatable Macro  
Assembler Functional Specification

### 3.0 REQUIREMENTS

#### 3.1 FUNCTION/ALLOCATION DESCRIPTION

The IEWS Techniques Generator Controller Program shall be the software portion of Techniques Generator. It shall run in the T.G. Controller/Processor hardware which is implemented with an RP-16 Microprocessor. Together with the hardware, the program shall provide the overall T.G. functions described in paragraph 3.1.1, and the Controller/Processor functions described in paragraph 3.1.2.1, both of applicable document 53959-HM-0410, T.G. hardware specifications.

The TG Controller Program shall be structured in the modules and relationships as shown in Figure 1. Basically, once initialized, the program shall be interrupt-driven. The two hierarchy modules are Initialize (INLZ), and Loop (LOOP). At power up or as required, the System Controller, SC, or a Local Control Panel, LCP, shall be able to put the program to start of INLZ. Either of the two shall be able to command run.

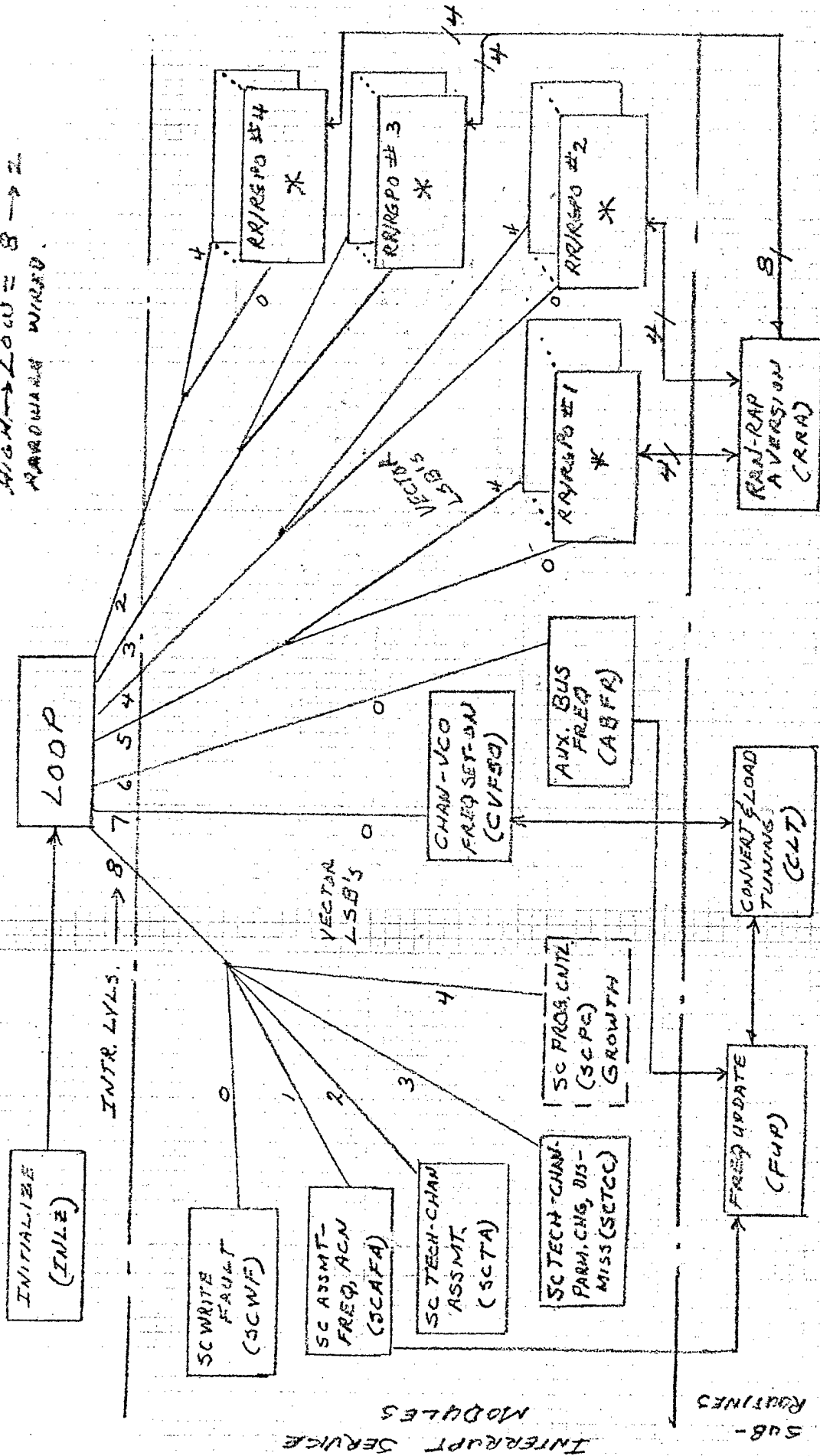
INLZ shall initialize all variables, assignments and generators and transfer to LOOP. LOOP shall basically enable interrupts and run in an idle loop awaiting interrupts. All service routines shall return to LOOP to await further interrupts.

There shall be twelve types of interrupt service modules as shown in Figure 1 and Figure 2, VIZ.,

SC Write Fault (SCWF)

SC Assignment - Frequency, ACN (SCAFA)

INTR. LVL. PRIORITY  
HIGH → LOW = 8 → 2  
HARDWARE WIRED.



INTERRUPT SERVICE  
MODULES

SUB-  
ROUTINES

\* see Fig. 2

FIG. 1. TECH GEN. UNIT CONTROLLER SOFTWARE

PAGE 1 of 2

Handwritten notes:  
1/22/70  
1/22/70

H. McArthur  
7/22/60

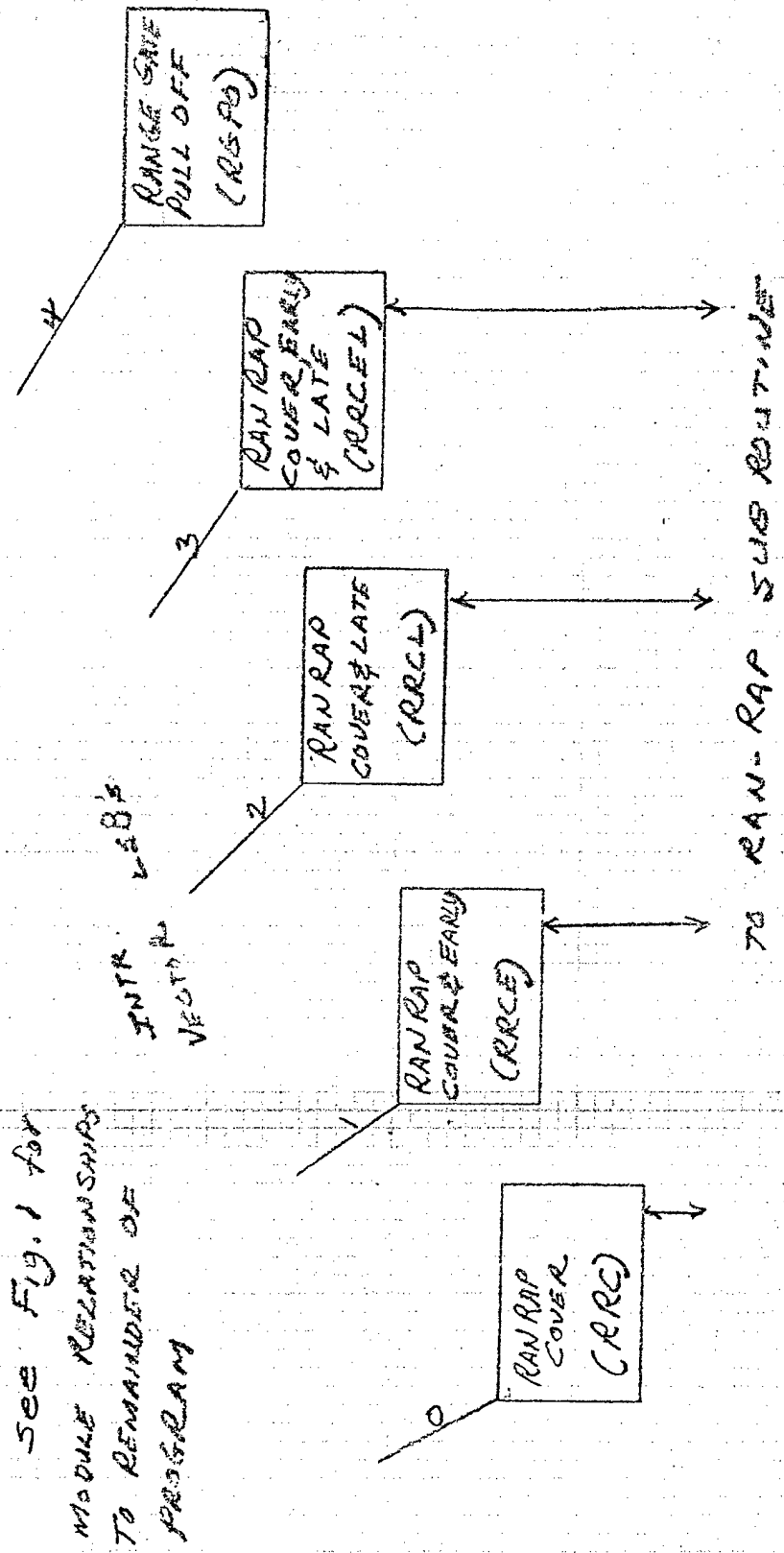


FIG. 2 RR/RSPO MODULE TYPES

SC Technique-Channel Assignment (SCTA)  
SC Technique-Channel Parameter Change, Dismiss (SCTCC)  
SC Program Control (Currently Growth) (SCPC)  
Channel-VCO Frequency Set-On (CVFSO)  
Auxiliary Bus-Frequency (ABFR)  
RAN-RAP Cover (RRC)  
RAN-RAP Cover and Early (RRCE)  
RAN-RAP Cover and Late (RRCL)  
RAN-RAP Cover, Early, Late (RRCEL)  
Range Gate Pull-Off (RGPO)

Note in Figure 1 that the last five module types shall service four RAN-RAP RGPO Technique Generators. Interrupt level selects the general service. Within the interrupt level the three least significant bits, LSB's, of the hardware interrupt vector shall identify a particular service module. Within any of these levels, the device requesting service determines the vector, only one vector per service request.

Interrupt services have horizontal modularity, i. e., service routines are independent of one another.

Finally, there are three subroutines:

Frequency Update (FUP)  
Convert and Load Tuning (CLT)  
RAN RAP -A Version (RRA)

Relationships of subroutines to service module users are shown in Figures 1 and 2.

At the end of any service-routine execution, the program shall return to LOOP. For this development the software shall enable interrupts only during LOOP. Nesting of interrupt services is a software growth capability. The hardware is capable of supporting such nesting.

### 3.2 FUNCTIONAL DESCRIPTIONS

Each IEWS T.G. Controller Program module shall implement the corresponding flow diagram given herein. Each flow diagram shows the fixed hardware addresses involved. Externally interchanged word formats shall be as specified in the referenced, associated document, 53959-HM-0410, "Unit Hardware Development Specification - IEWS Hardware Spec. - Techniques Generator". Programmable variables within programs shall have the values given on the diagrams. Some of these modules might change as a result of development tests. Internal word formats can vary from those herein if more practical. Program Tables are given in paragraph 3.3

#### 3.2.1 Initialize (INLZ) Module

INLZ shall be as given in Figure 3. Controls and address to set and run INLZ are given in notes thereon. INLZ clears all assignments, if any, and flags. It initializes all internal tables.

#### 3.2.2 Loop (LOOP) Module

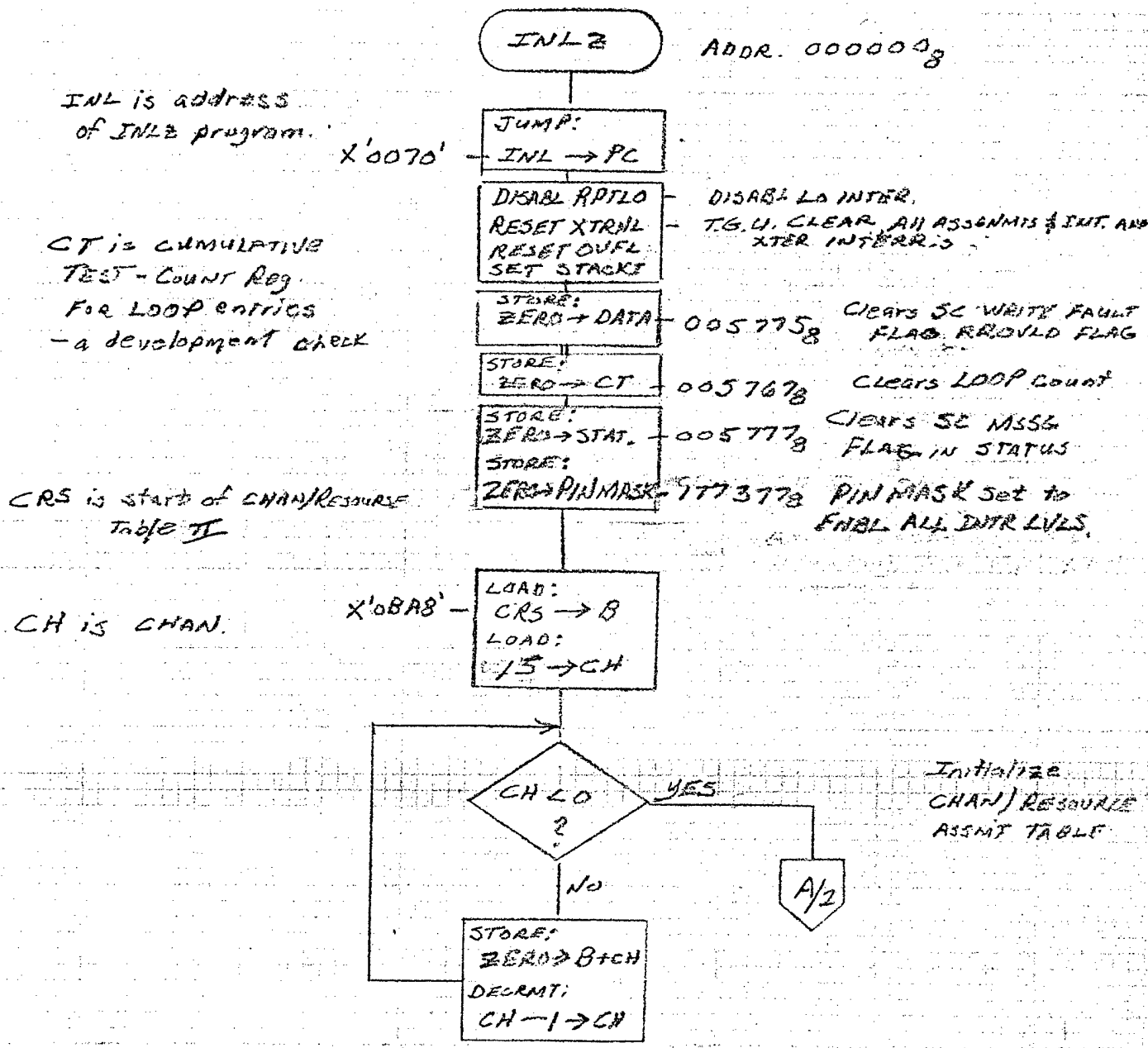
LOOP shall be as given in Figure 4. Background testing can be added to this at any time as growth software.

#### 3.2.3 SC Write Fault (SCWF) Module

SCWF shall be the interrupt routine of Figure 5. Hardware interrupt vectors and addresses are given. This routine endeavors notify the SC if a write is attempted to T.G. instruction memory during times of memory-protect. The T.G. RP-16 4K word memory is two-port, one for the Daisy Chain (DC) bus, and the other for the T.G. RP-16. The memory is

# FIG. 3 INITIALIZE

PAGE 1 OF 3



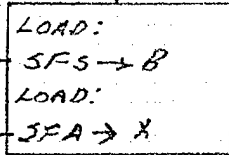
- NOTES:
- INITIALIZE address 0000H is set for any:
    - SC Daisy Chain Master Clear - DEMACL
    - LCP Master Clear - M1STCL
    - SC TG External Control "Initialize"
    - LCP Control "STOP" and by inputting Addr. 0000H.
  - Subsequent Jump to INITIALIZE RUN either:
    - SC TG External Control "NEWSTART"
    - LCP Control "START" (02 Addr. 0000H)

*H. Macmillan  
7/28/76*

FIG. 3 (CONT'D) INITIALIZE  
ADDED 11/27/74

SFS IS START OF  
FM GEN PRE-OPER.  
STATUS TABLE I/A

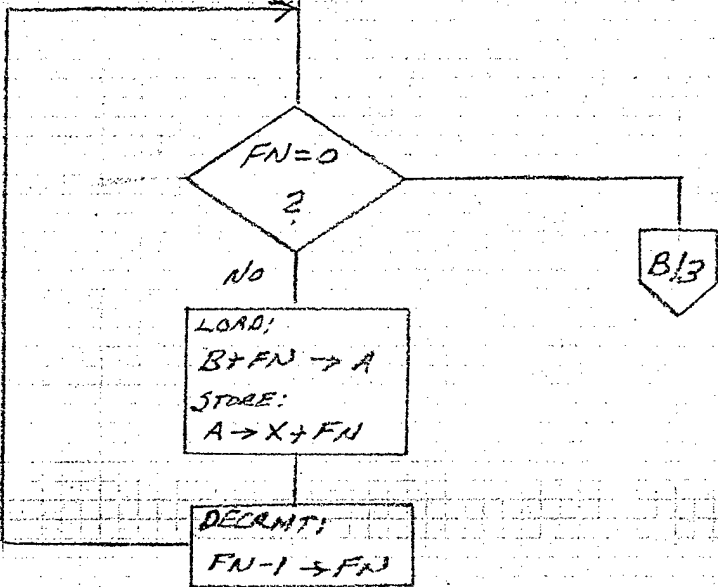
X'0BBB'



SFA IS START OF  
FM GEN ALLOCATION  
(OPER.) TABLE I/A

X'0BBB'

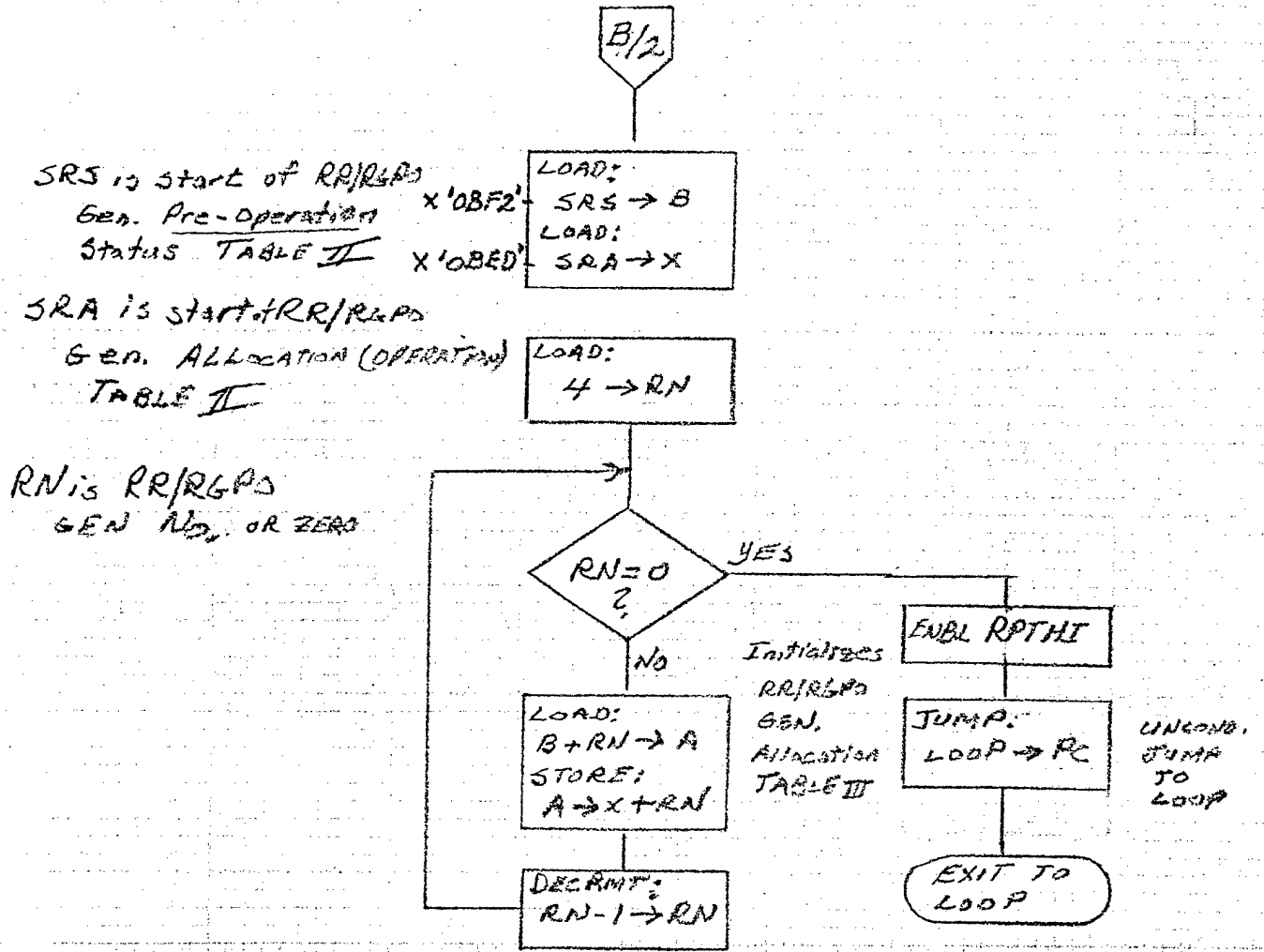
FN IS FM GEN No.



11/29/75  
Howard McQuilley

FIG. 3 (CONT'D) INITIALIZE

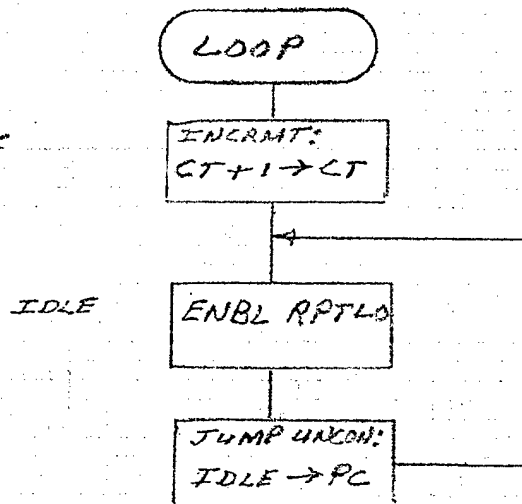
PAGE 3 OF 3



7/29/76  
H. Medsker

# FIG. 4 LOOP

CT is cumulative  
test



NOTES: 1. LOOP IS ENTERED WITH  
JUMP FROM:

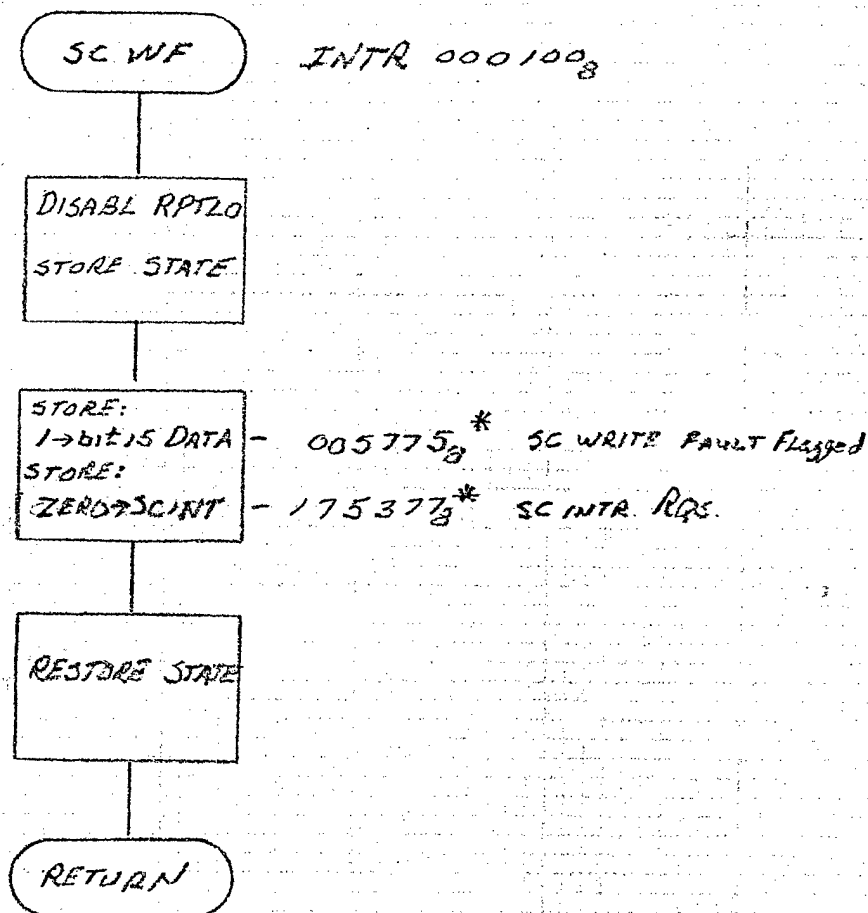
- a. INITIALIZE (ENLZ),
- b. Return from any  
OTHER INTERRUPT  
ROUTINE MODULE

2. Cumulative Test is  
Count of Loop Entries  
Subsequent to ENLZ.

This is a check during  
DEVLPMT. TESTS

H. McZanler  
7/28/76

FIG. 5 SC WRITE FAULT



## \* NOTE:

1. 175377<sub>B</sub> Addr. sets SC  
INTR (B) on the DAISY CHAIN  
B-15. The BUS has no  
INTR ACK. Hence -

2. The INTR RQS (B) remains  
Set until:

- a) SC addresses 005775<sub>B</sub>, or
- b) SC issues DC MCL, or
- c) If programmed, TG  
RP-16 "RESET INTRNL", i.e.  
OPRST.

7/26/70  
R. The Fault

partitioned with T.G. instructions, data, and working space in all but 8 locations. It is the bulk of this memory except the 8 locations for SC messages that is at times protected to DC writes. An SC Daisy Chain Master Clear, DCMCL always opens all memory to DC write. Any time a message is transferred through any of the 8 message locations the bulk of memory is protected from DC writes. If while protected a DC write is attempted, DC ACKnowledge is hardware returned to prevent hanging the bus, even though data is not written. The T.G. RP-16 receives the interrupt and in turn attempts to notify the SC as shown in Figure 5. The 4K memory is open to DC read all the time. The two port is used to facilitate loading T.G. RP-16 program directly from the DC bus.

#### 3.2.4 SC Assignment-Frequency, ACN (SCAFA)

SCAFA shall be the interrupt routine of Figure 6. Note that the Frequency Update Subroutine (FUP) is used in this service. Return to LOOP is from FUP.

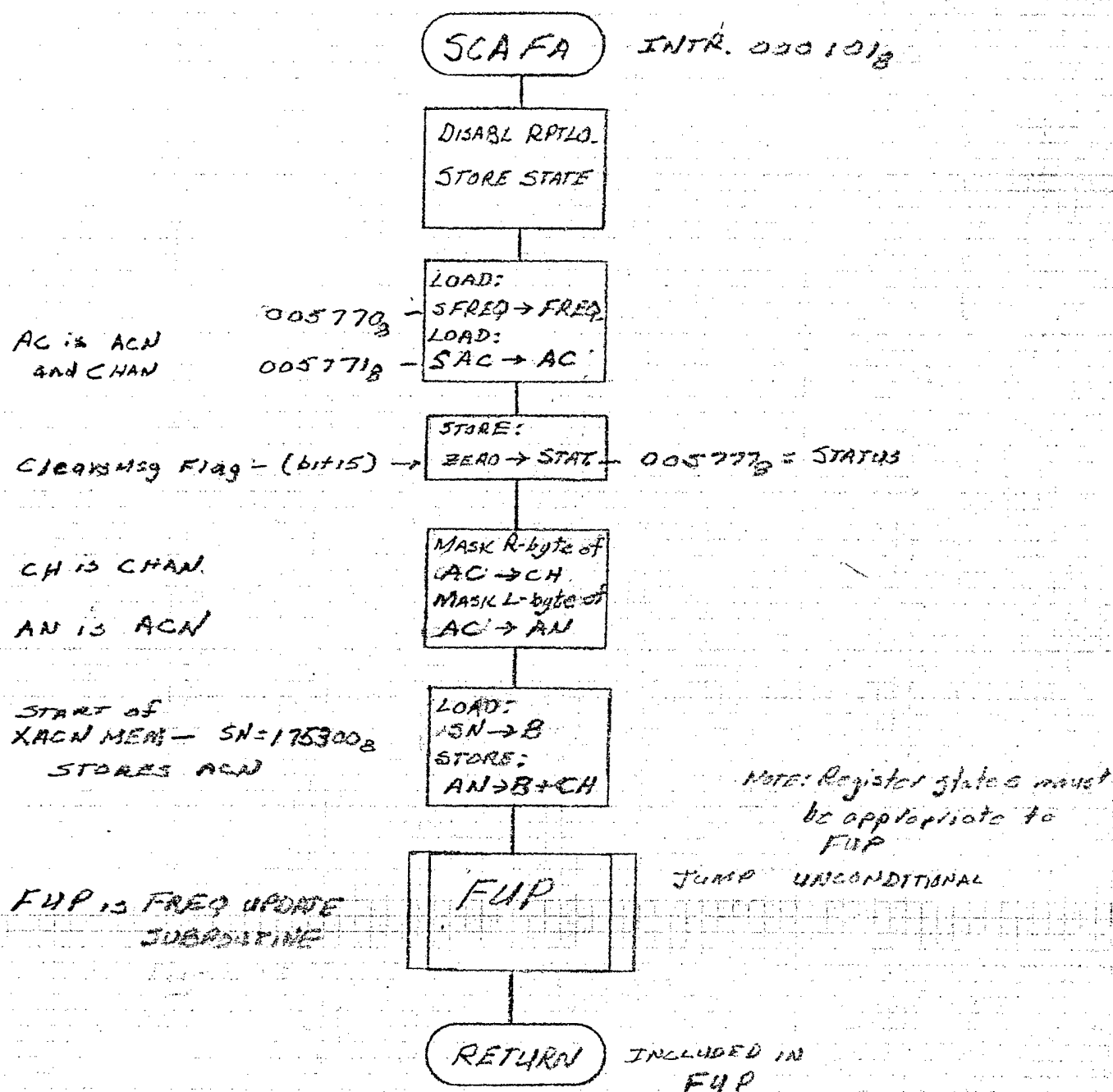
#### 3.2.5 SC Technique-Channel Assignment (SCTA) Module

SCTA shall be the interrupt routines of Figure 7. This module retrieves all generator parameters from T.G. Techniques Program memory and loads the proper generators. Where the limited number of RAN-RAP/RGPO generators are needed, the routine performs a resource management allocation by finding an unused generator for the current program. It remembers to which channel the generator is assigned.

#### 3.2.6 SC Technique-Channel Parameter Change or Dismiss (SCTCC) Module

SCTCC shall be the interrupt routines of Figure 8. This module changes any parameters of a currently assigned Technique Program per the SC message. The Technique Program stored in Technique Program memory remains as originally loaded. If the change is in use of the Auxiliary Bus for Frequency and/or ACN, the routine fills in the balance of the word as stored in Techniques

# FIG. 6 SC ASSIGNMENT - FREQ, ACN



7/26/76  
H.R. McQuinn

# FIG. 7 SC TECHNIQUE - CHANNEL ASSIGNMENT

REDONE REWISED  
11/30/76 12/10/76

PAGE 1 of 4

TO ADD TWO FM  
SEN'S.

SCTCA INTR 0001023

CFM IS CONNECTION  
MEMORY FM GEN NO.  
TEMP. STORAGE LOCATION

DISABL RPTLD  
STORE STATE  
CLR CFM

TW IS TECH. WORD

005772<sub>8</sub>

LOAD & STORE:  
JTW → TW  
STORE:  
ZEROS → STAT

bit 15 →

005777<sub>8</sub>

CHGGS SC MSG  
Flag-bit 15

CH IS CHANNEL  
TN IS TECH. NO. X2

MASK R-BYTE:  
TW → CH  
MASK L-BYTE:  
TW → TN

TECH NO. # B -

ROTATE:  
TN left 2 places  
LOAD:  
PS → B

PS IS (TECH) PROG START-006000<sub>8</sub>

LOAD:  
GL → X  
ADD:  
X + CH → X

GL IS SEN. LOAD ADDR-175000<sub>8</sub>

PW IS  
PARAMETER WORD

D/2

LOAD & STORE:  
B + TN → PW  
MASK bit 15-12  
of PW → CD

CD IS (SEN) CODE

CD = 8 ?

YES

FM GEN NEEDED

B/3

CD = 10 ?

YES

RR/RSA GEN  
NEEDED

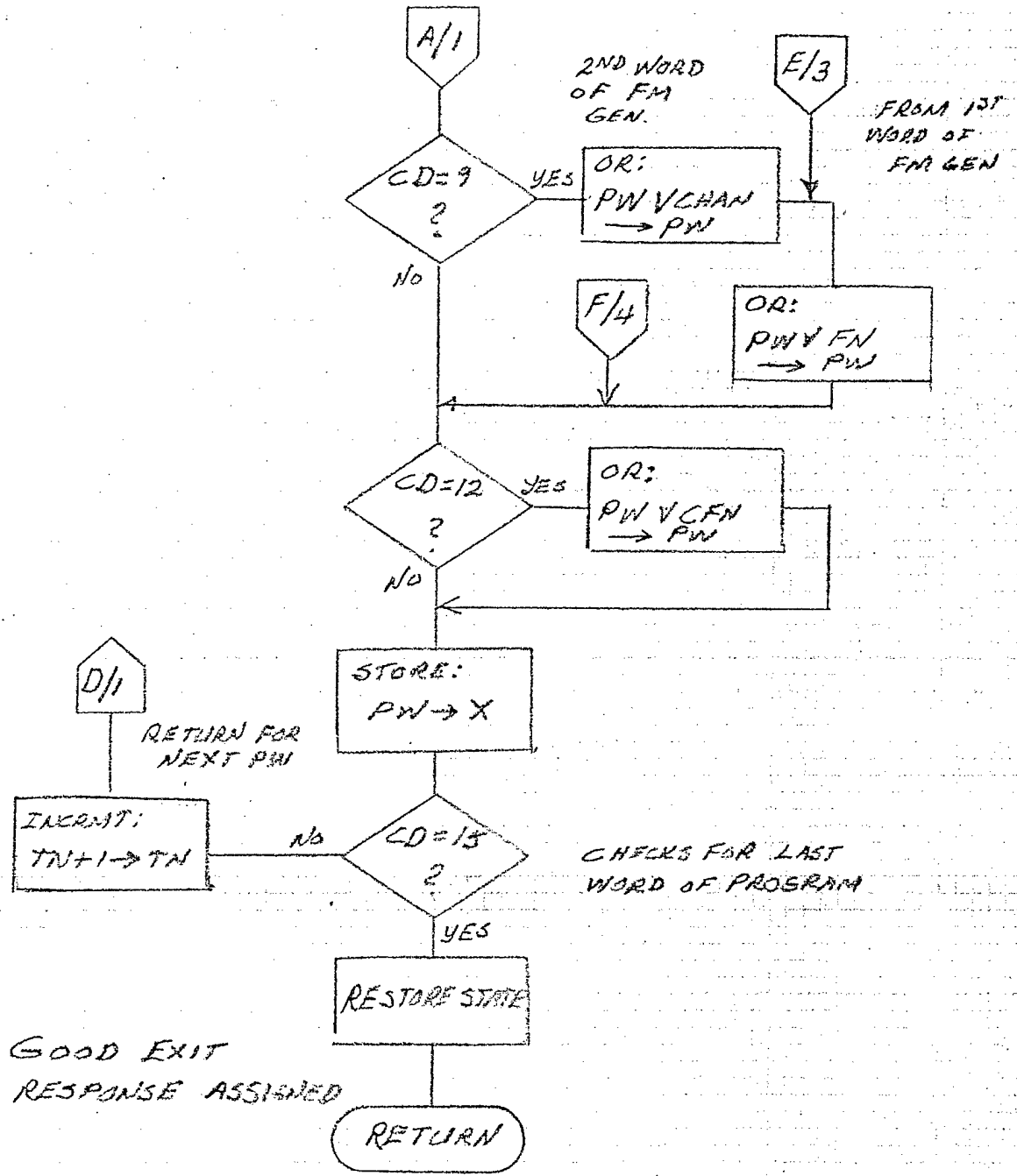
C/4

A/2

Howard M. Zuller  
11/30/76

# FIG. 7 SE TECH-CHAN ASSAULT (CONT'D)

REDONE 12/10/76



Howard McQuinn  
12/10/76

# FIG. 7 SC TECHNIQUE - CHANNEL ASSMT (CONT'D)

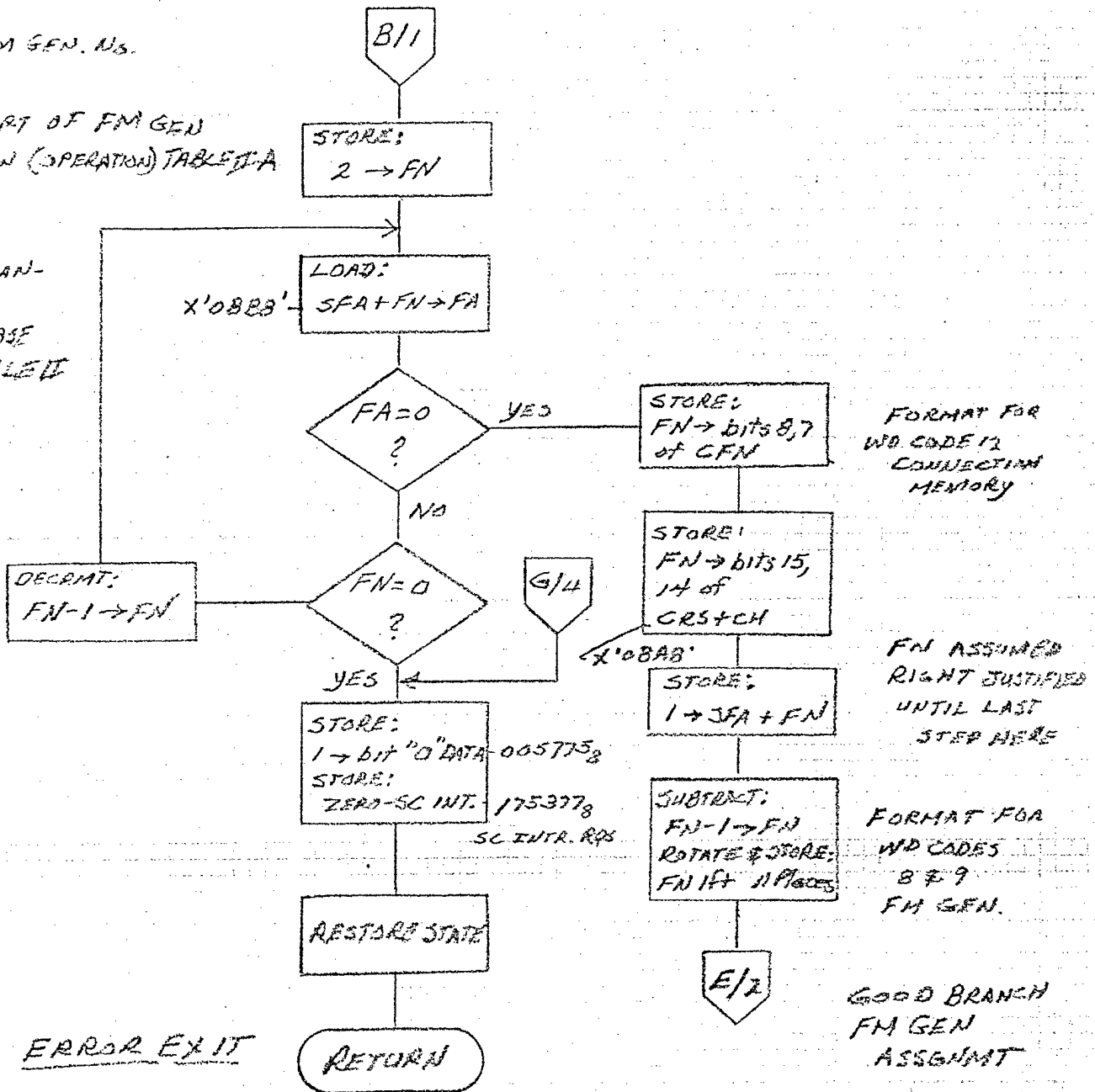
REDONE 11/30/76

REDONE 12/10/76

FN IS FM GEN. NO.

SFA IS START OF FM GEN ALLOCATION (OPERATION) TABLE I/A

CRS IS CHAN-RESOURCE STATUS BASE ADDR. TABLE II



FORMAT FOR WD CODE 12 CONNECTION MEMORY

FN ASSUMED RIGHT JUSTIFIED UNTIL LAST STEP HERE

FORMAT FOR WD CODES 8 & 9 FM GEN.

GOOD BRANCH FM GEN ASSGMENT

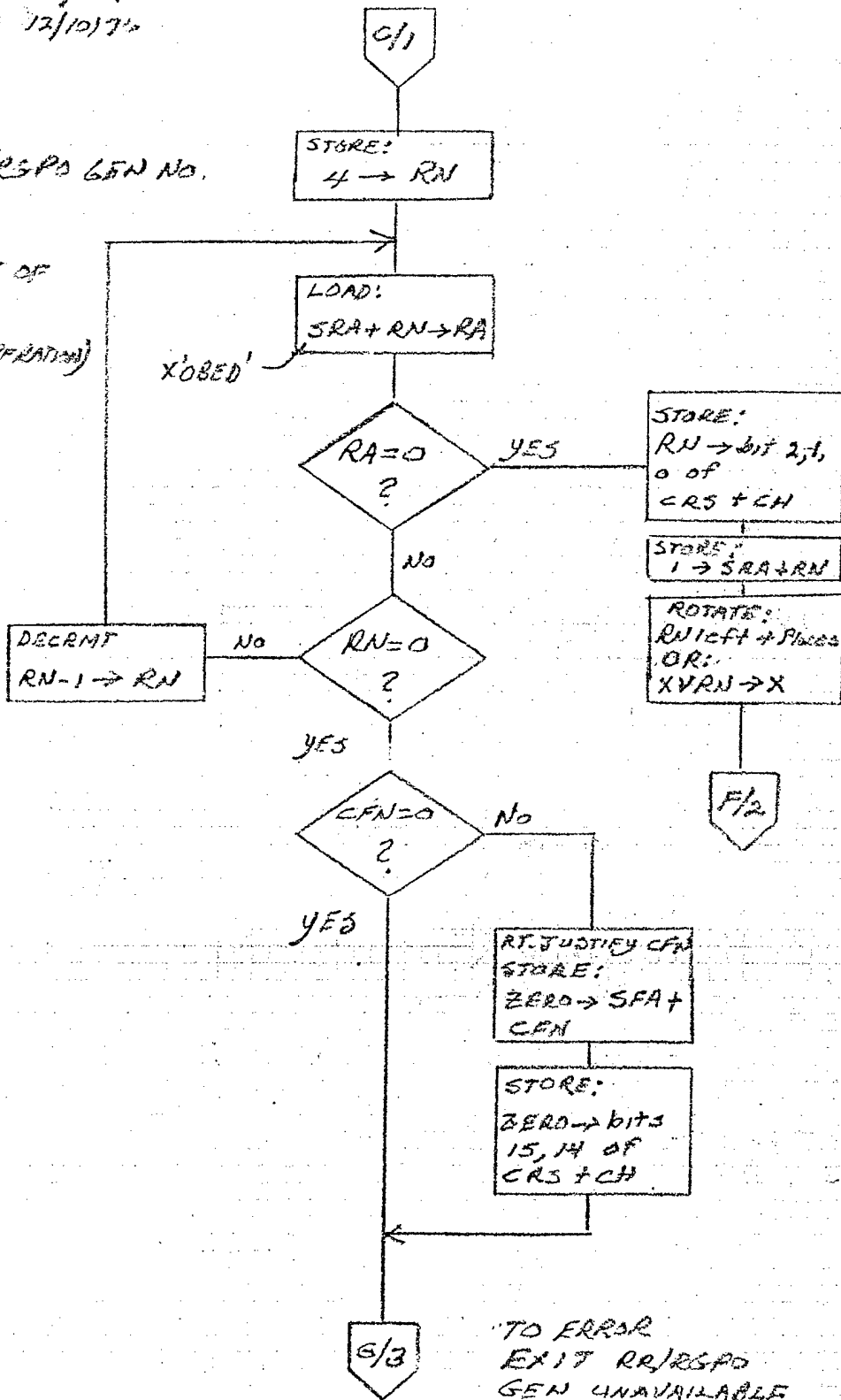
*Howard McZuller*  
12/10/76

# FIG. 7 SC TRAIL-CHAN ASSIGN (CONT'D)

REDONE 11/30/76  
REVISED 12/10/76

RN IS RR/RSPD GEN NO.

SRA IS START OF  
RR/RSPD SEN.  
ALLOCATION (OPERATION)  
TABLE II



RN ASSUMED  
RIGHT  
JUSTIFIED  
GOOD  
BRANCH  
RR/RSPD  
GEN  
ASSIGNED

TO ERROR  
EXIT RR/RSPD  
GEN UNAVAILABLE

Howard McJannet  
11/30/76  
12/10/76

FIG. 8 SC TECHNIQUE-CHANNEL PARAMETER CHANGE OR DISMISS PAGE 1 of 4

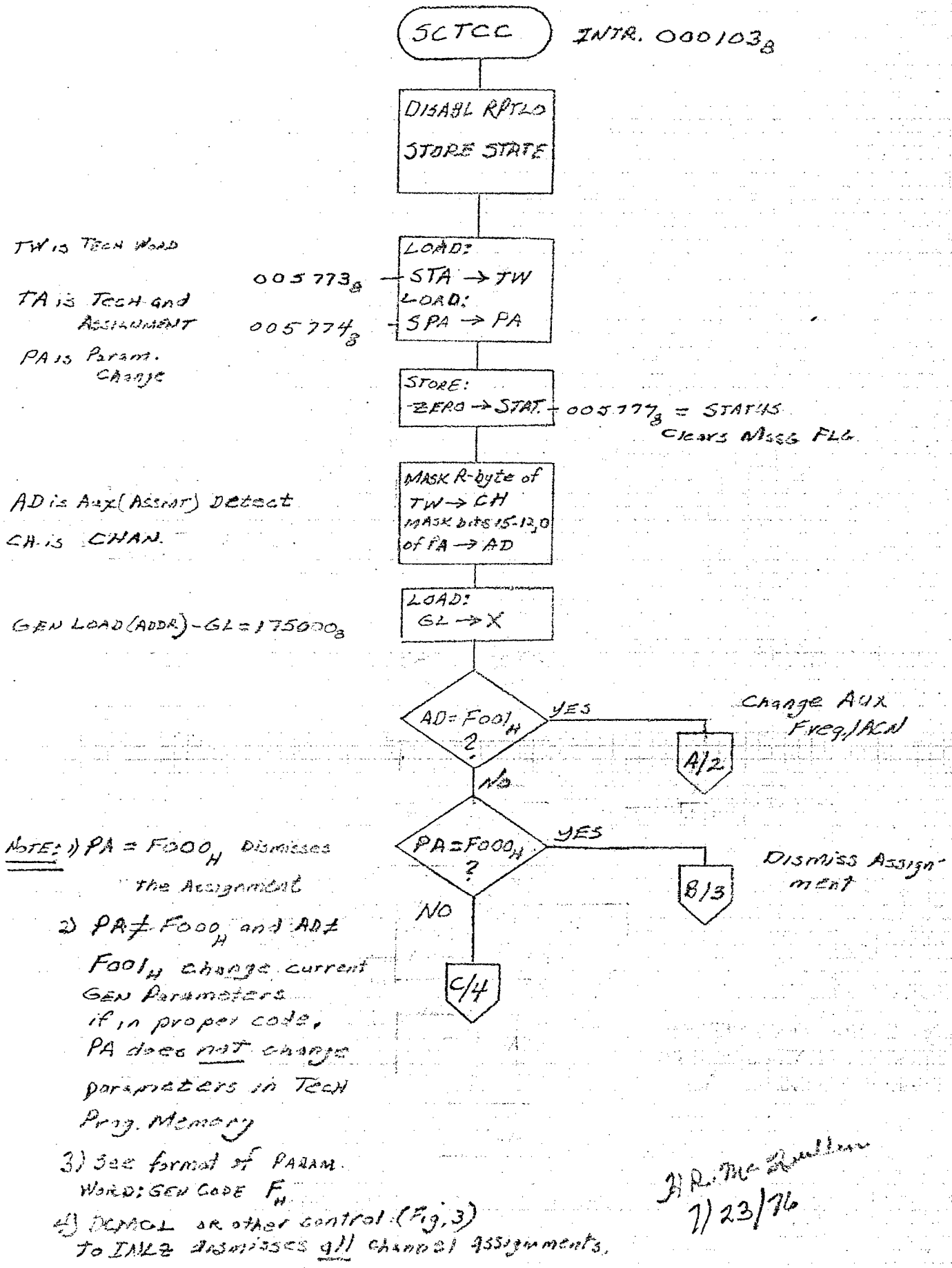


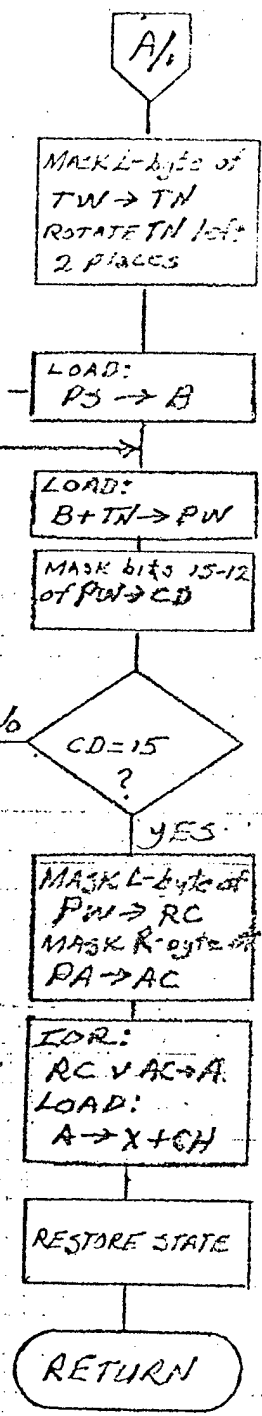
Fig. 3  
SCTEC (CWR15) PAGE 2 of 4

TN is Tech. No. \* 2 -  
TN is Tech. No. \* 3 -

(TECH) PWR START - PS = 006503<sub>8</sub>

PW is Param. Word  
CD is (Gen) Code

RC is Response Command  
AUX (Bus) COMMAND - AC



This routine changes AUX BUS ASSIGN - ACN OR PFR FOR THIS CHANNEL PFR SC COMMAND

Fetch Techn. Memory END word.

Combine Techn. Memory XPDR, RPFR, & CW bits of END word with new AUX BUS ASSIGNMENT of PA

A.R. McDowell  
1/23/76

FIG. 8 SL TECH-CHAN PARAM. CHG OR DISMISS  
SETCC (CONT'D)

PAGE 3 OF 4

THIS ROUTINE DISMISSES  
A CHAN ASSMT INCLUDING  
RESOURCES REPRSED AND/OR  
FM GEN IF ASSIGNED

REDONE 12/10/76

CRS IS CHAN-RESOURCE  
STATUS ADDR BASE  
TABLE II

RN IS RPRSPD GEN NO.  
ASSIGNED TO THIS  
CHAN

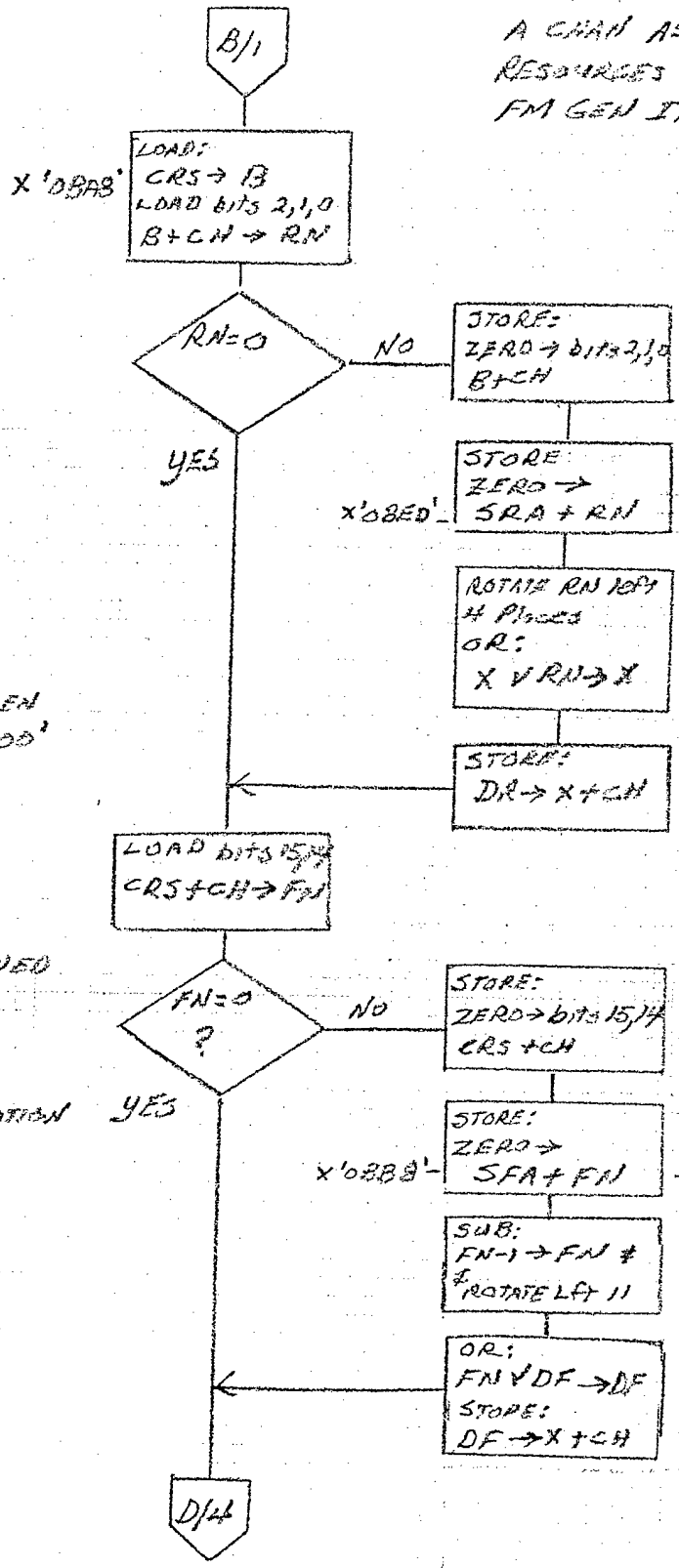
SRA IS RPRSPD GEN  
ALLOCATION TABLE II

DR IS DISMISS RPRSPD GEN  
AND EQUALS X'8000'

FN IS FA GEN NO. ASSIGNED  
TO THIS CHANNEL

SFA IS FM GEN ALLOCATION  
TABLE II A

DF IS DISMISS FM GEN  
AND EQUALS X'8000'



Howard McQuillen  
12/10/76

FIG. 8 SC TECH-CHAN PARAM. CHG OR DNM/SS  
SCTEC (CONT'D)

REDONE 12/10/76

PAGE 4 OF 4

CD IS (GEN) CODE

CRS IS CHAN-RESOURCE  
STATUS ADDR. BASE  
TABLE II

FN IS FM GEN. No. ASSIGNED  
TO THE CHAN.

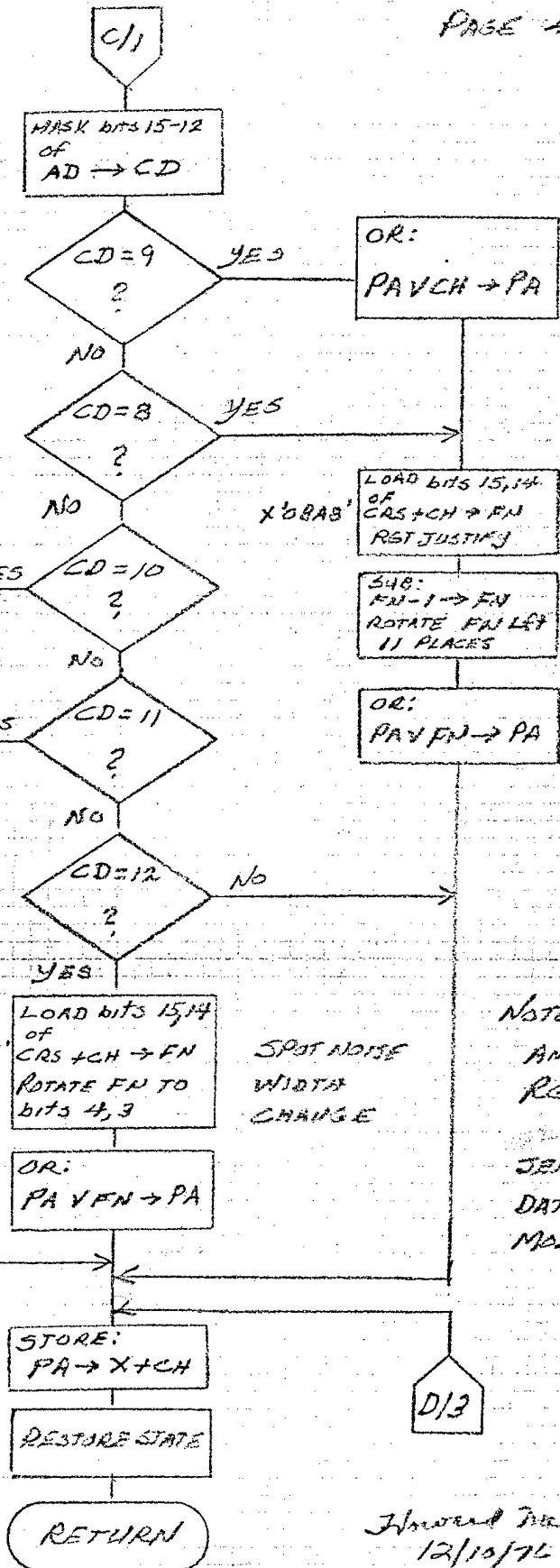
RN IS RR/RGPs GEN. No.  
ASSIGNED TO THE CHAN.

FM GEN  
PARAM. CHANGE

RR/RGPs GEN.  
PARAM. CHANGE

SPOT NOISE  
WIDTH  
CHANGE

NOTE: CHANGE FOR:  
ANGLE TECHN'S,  
RGN TECHN'S,  
ARE  
SERVICED WITHOUT  
DATA OR ADDR  
MODIFICATION(S)



Approved by [Signature] 12/10/76

Program memory. This module alternatively dismisses a particular Channel-Technique assignment. See notes of Figure 8 for codes. The routine for channel-technique dismissal also performs the resource management update of RAN-RAP/RGPO generator allocations.

### 3.2.7 SC Program Control (SCPC) Module

This module is a growth module to allow great flexibility to enable the TG RP-16 to execute instructions sent by the SC. The hardware is designed to accomodate this, but currently the SC External Control via hardware address is sufficient. See Figure 10 of 53959-HM-0410.

### 3.2.8 Channel-VCO Frequency Set-on (CVFSO) Module

CVFSO shall be the interrupt routines of Figure 9. This routine is requested every 0.1 second by each channel-technique assigned. It currently is a linear integration of error correction. Growth software could provide other correction to include even a transfer table for VCO tuning command to frequency output. The routine calls subroutine Convert and Load Tuning (CLT) to select VCO subband and tuning, within subband.

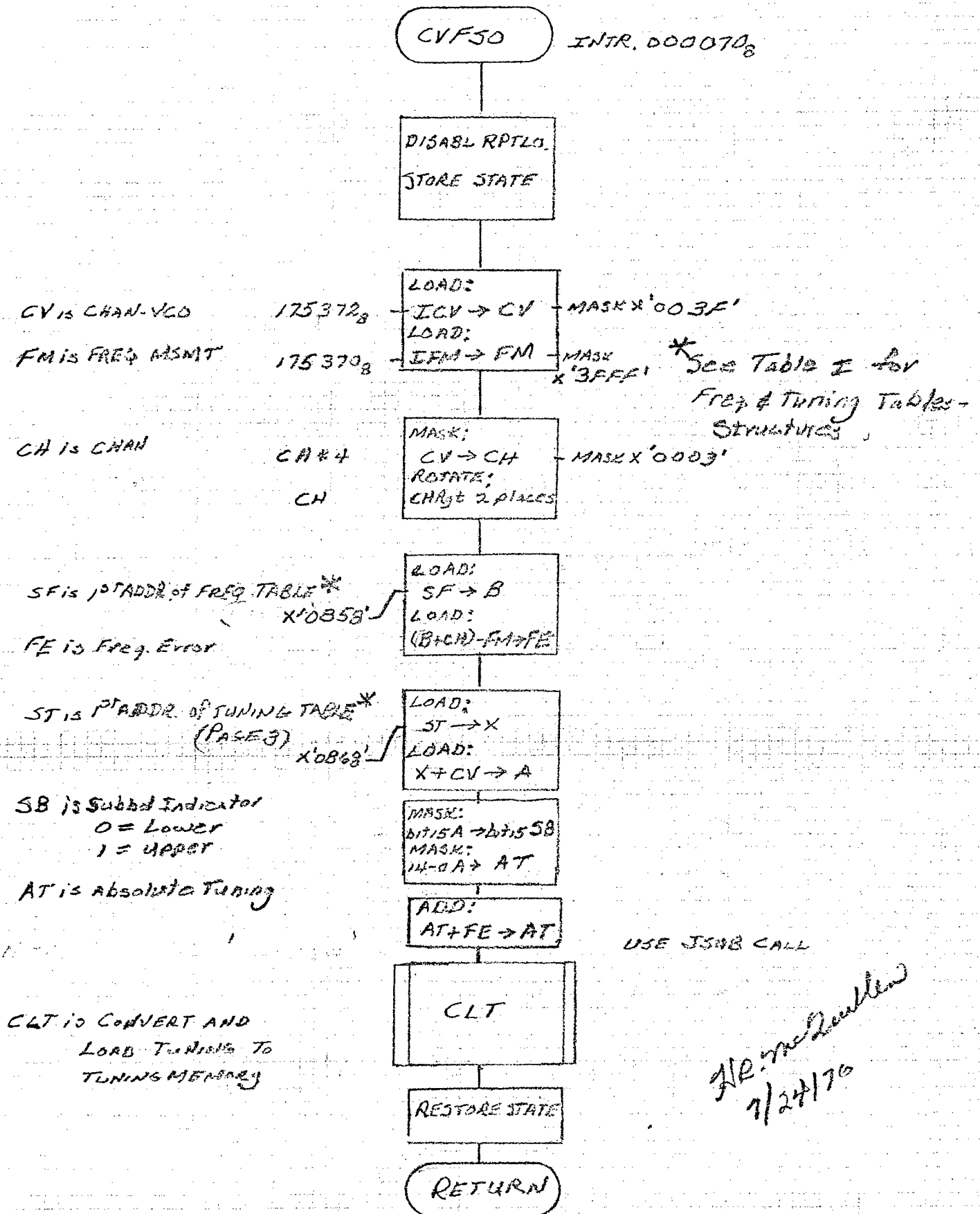
### 3.2.9 Auxiliary Bus Frequency (ABFR) Module

ABFR is the interrupt routine of Figure 10. This routine services frequency assignment updates for response-assigned channels, whose assignment includes Auxiliary bus update enable. The module uses the Frequency Update (FUP) subroutine which exits directly to LOOP.

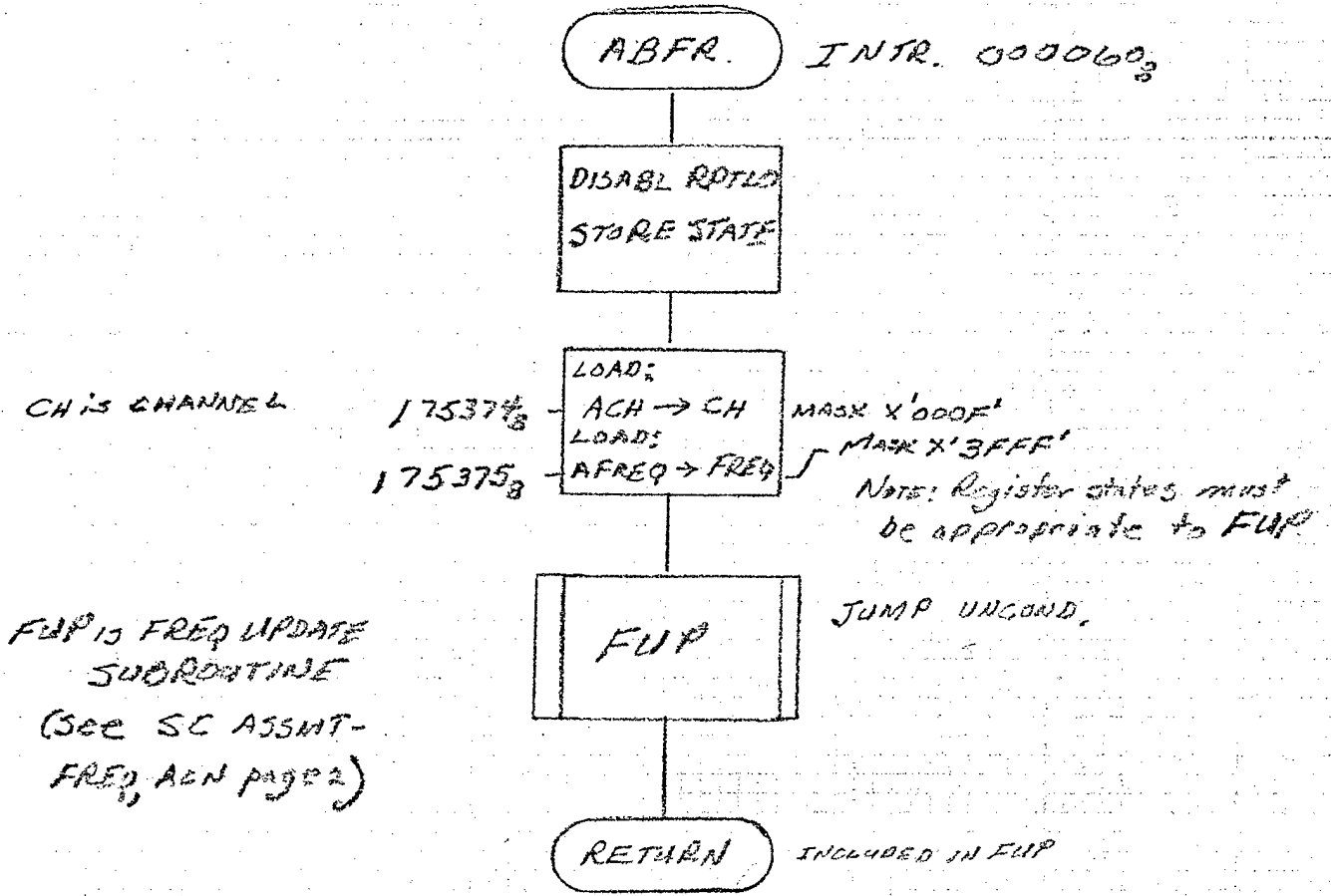
### 3.2.10 RAN-RAP Cover (RRC) Module

RRC is the interrupt module of Figure 11. As noted thereon, this function is performed for each of the four RAN-RAP/RGPO generators. List I of paragraph 3.3 gives the priority level and least significant octal addresses for each generator service module. This module uses RAN-RAP A version (RRA) subroutine and generates a single element RAN-RAP. Internal

FIG. 9 CHANNEL-VCO FREQUENCY SET-UP



# FIG. 10 AUX BUS FREQUENCY



*J. Medinilla*  
7/24/76

# FIG. 11. RAN RAP COVER

NOTES: 1. There is one of these programs for each of 4 RR/RSP Gen's  
 2. See LIST I for LVL, EVEN, ODD ASSNTS.

WA is Word A  
 WB is Word B

RRC INTR 0000 (LVL) 08

DISABL RPTLO  
 STORE STATE

LOAD:  
 RWA → WA  
 LOAD  
 RWB → WB

17534 (EVEN) 8

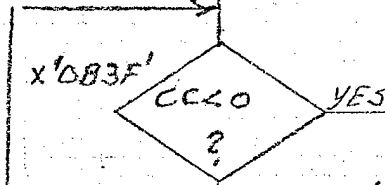
17534 (ODD) 8

USE JSUB CALL

RRA

RRA is RAN RAP - A VERSION

CC is COUNTER SET by RRA subroutine



x'0840'

STORE:  
 PL + CC → RS  
 DECRMT:  
 CC - 1 → CC

17534 (EVEN) 8

RS is RR Gen pulse delay mem. addr

x'083D'

STORE:  
 EG → RG  
 STORE:  
 LG → RG

17534 (ODD) 8

17534 (ODD) 8

RG is RR Gen Commit Gate Mem. Addr.

x'083E'

RESTORE STATE

RETURN

{ PL is pulse storage start addr. \*

{ CC is relative storage cell location of a pulse-delay

EG is EARLY COMMIT GATE DELAY

LG is LATE COMMIT GATE DELAY

\* SEE TABLE III

AR. McQuinn  
 7/29/76

pulse delay storage shall be as in Table III.

### 3.2.11 RAN-RAP Cover and Early (RRCE) Module

RRCE is the interrupt module of Figure 12. The description of paragraph 3.2.10 is generally the same except these routines generate a two-element RAN-RAP.

### 3.2.12 RAN-RAP Cover and Late (RRCL) Module

RRCL is the interrupt module of Figure 13. This is another two-element RAN-RAP similar to paragraph 3.2.11.

### 3.2.13 RAN-RAP Cover, Early and Late (RRCEL) Module

RRCEL is the interrupt module of Figure 14. This is a three-element RAN-RAP built up from the single element of paragraph 3.2.10. Note that growth software can have many variations in delay pulse configurations for this RRCEL as well as for RRC, RRCE, and RRCL.

### 3.2.14 Range Gate Pull Off (RGPO) Module

RGPO is the interrupt module of Figure 15. As noted thereon this function shall be performed for each of four RR/RGPO generators. List I gives the priority levels and addresses.

### 3.2.15 Frequency Update (FUP) Subroutine

FUP is the subroutine of Figure 16. As noted thereon frequency assignment modules SCAFA and ABFR shall use the subroutine. Internal tables used are those of Table I. Essentially this subroutine shall update the tuning of each of four VCO's by the same amount the channels assigned frequency is changed. Growth software can have a more complex tuning update if tests with MAAS equipment indicate a need. FUP uses the subroutine Convert and Load Tuning (CLT).

# FIG. 12 RAN RAP COVER AND EARLY

NOTES: 1. There is one of these programs for each of 4 RR/RGen Sigs  
 2. See TABLE III for LVL, EVEN, ODD ASSM'Y

WA is word A

WB is word B 17534(EVEN)<sub>8</sub>  
 17534(ODD)<sub>8</sub>

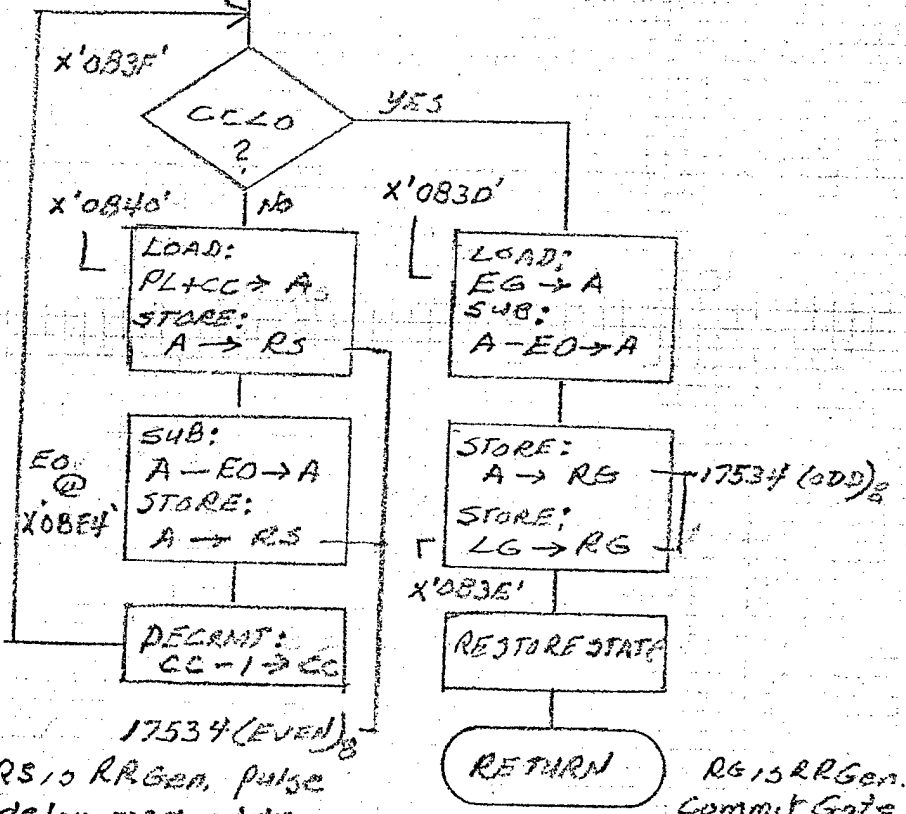
RRA is RAN RAP A VERSION

RRCE INTR. 0000 (LVL)<sub>8</sub>

DISABL RPTLO  
 STORE STATE

LOAD: RWA → WA  
 LOAD: RWB → WB

RRA USE JSUB CALL



CC is CELL COUNT, set by RRA

PL is pulse storage start addr. \*

CC is also relative storage cell location of pulse delay

EG is EARLY Commit Gate delay

LG is Late Commit Gate delay

EO is Early (Element) Offset, currently 4 usec

RS is RGen. pulse delay mem. addr.

RG is RGen. Commit Gate Mem. Addr.

\* SEE TABLE III

HR no. 12/10  
 7/30/70

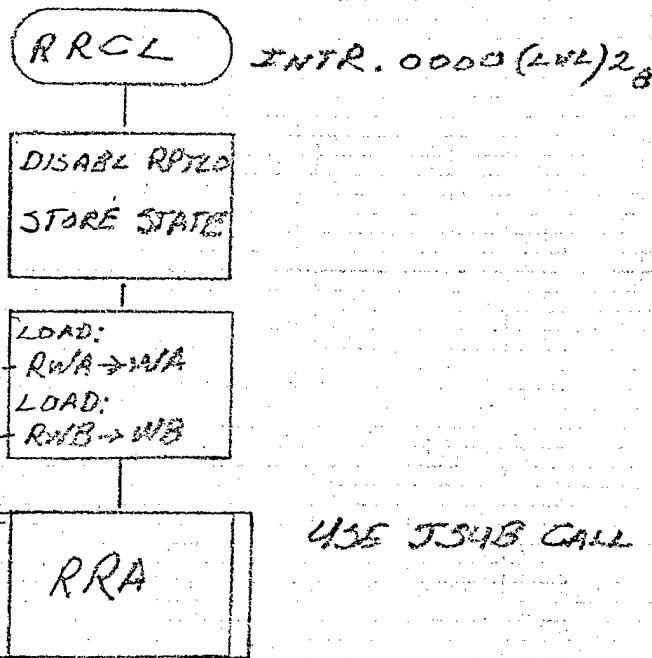
# FIG. 13 RAN RAP COVER AND LATE

NOTES: 1. There is one of these programs for each of 4 RR) RGEN GENs.  
 2. See LIST I for LVL, EVEN, ODD ASSMYS.

WA is word A  
 WB is word B

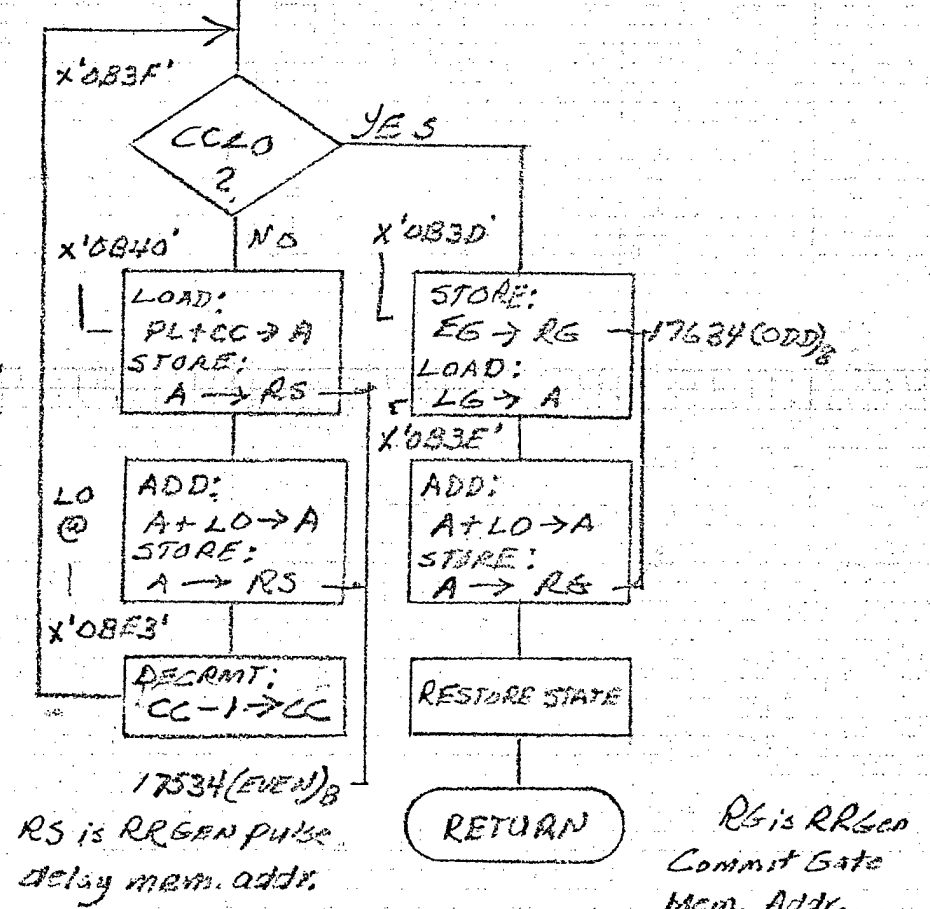
17534(EVEN)<sub>B</sub>  
 17534(ODD)<sub>B</sub>

RRA is RAN RAP  
 A VERSION



CC is Cell Count Set by RRA  
 PL is pulse storage start addr. \*  
 CC is also relative storage cell location of pulse delay

EG is Early Commit Gate delay  
 LG is Late Commit Gate delay  
 LO is Late (Element) Offset, currently 4 = 6 usec



\* SEE TABLE III

NR McQuillen  
 7/30/73

# FIG. 14 RAN RAP - COVER, EARLY AND LATE

Page 1 of 2

NOTES: 1. There is one of these programs for each of 4 RR/RSP's GERS.

a. See LIST I for LVL, EVEN, ODD ASSMNTS

WA is word A

WB is word B

RRA is RAN-RAP  
A VERSION

17534 (EVEN) → B  
17534 (ODD) → B

RRCEL

INTR. 0000 (LVL) 3<sub>B</sub>

DISABL RPTLO  
STORE STATE

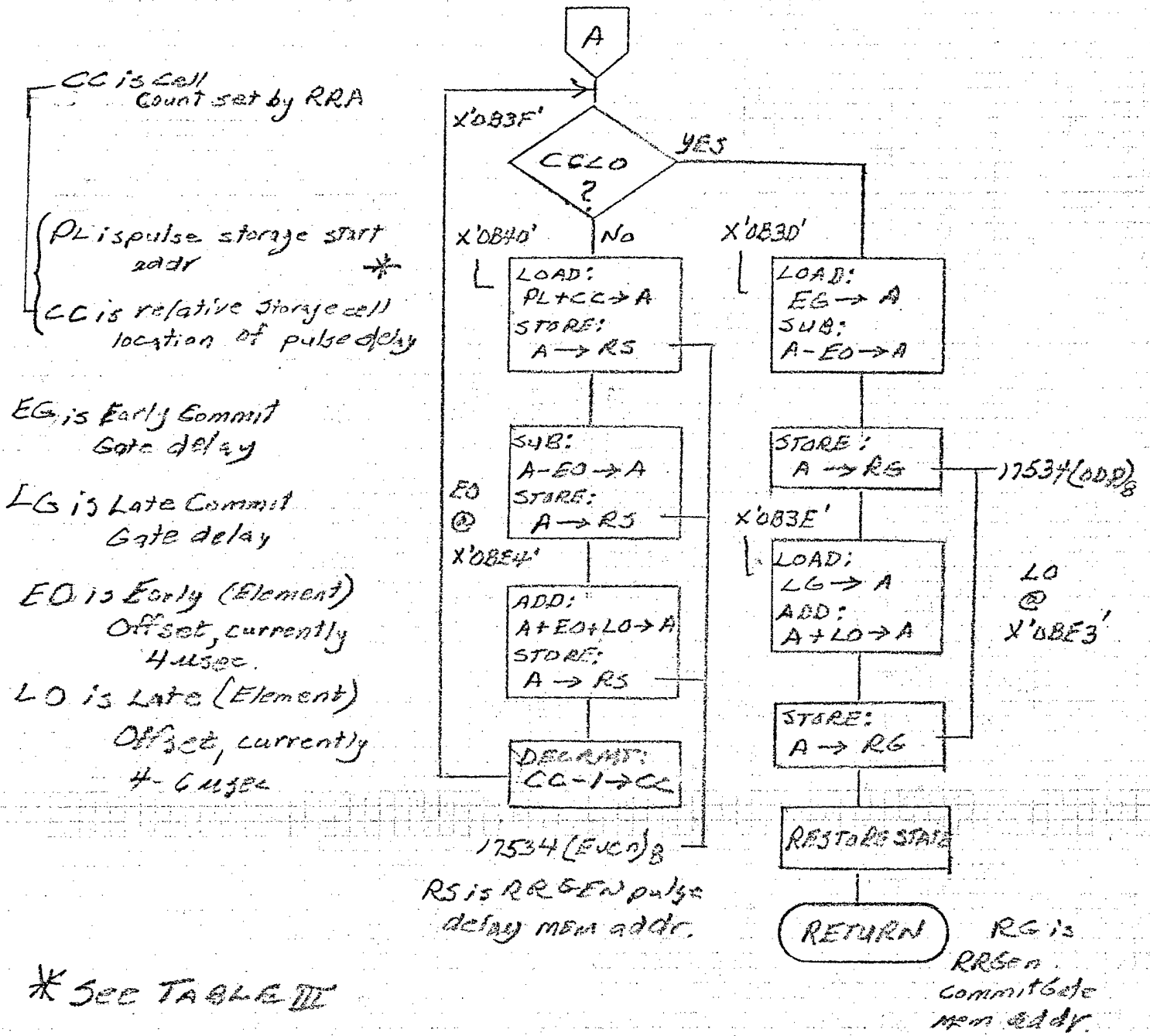
LOAD: RWA → WA  
LOAD: RWB → WB

RRA

A

AR. M. Zeller  
7/30/76

FIG 14 RAN RAP-COVER, EARLY, AND LATE (CONT'D) PAGE 2 of 2



\* SEE TABLE III

J.R. McQuillen  
7/30/75

# FIG 15 RANGE GATE PULL OFF

Page 1 of 2

- NOTES: 1. There is one of these programs for each of HRR/R&P GEN'S.  
 2. See LIST I for LVL, EVEN, ODD ASSEMBLIES

WB is WORD B

WA is WORD A

PW is Pulse Width

PWS is Start of pulse width conversion table.

PR is pretrigger,

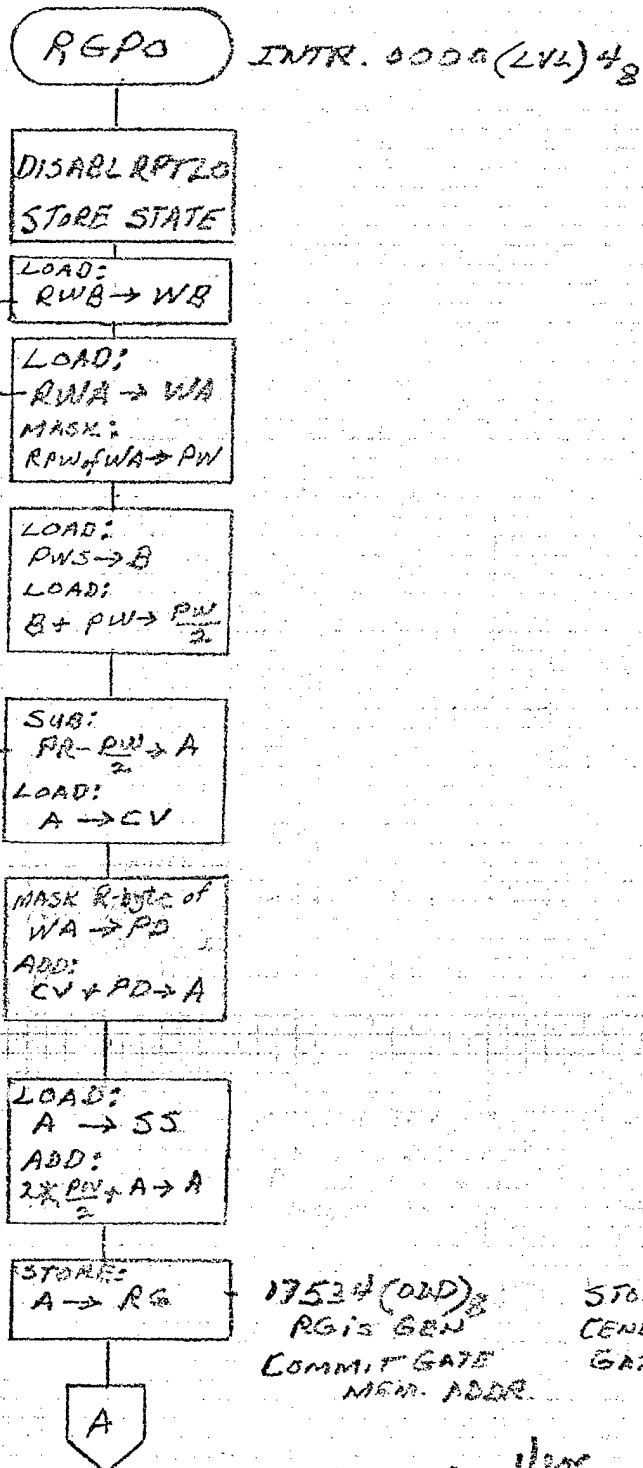
currently 25.6 usec.

LSB = 62.5 nanosec. X'0BE1'

CV is Cover Plus Delay

PD is Pull-off Delay

SS is SCRATCH-PAD delay STROBE



17534(ODD)B  
 RG'S GEN  
 COMMIT GATE  
 MEM. ADDR.

STORES LATE  
 (END OF) COMMIT  
 GATE

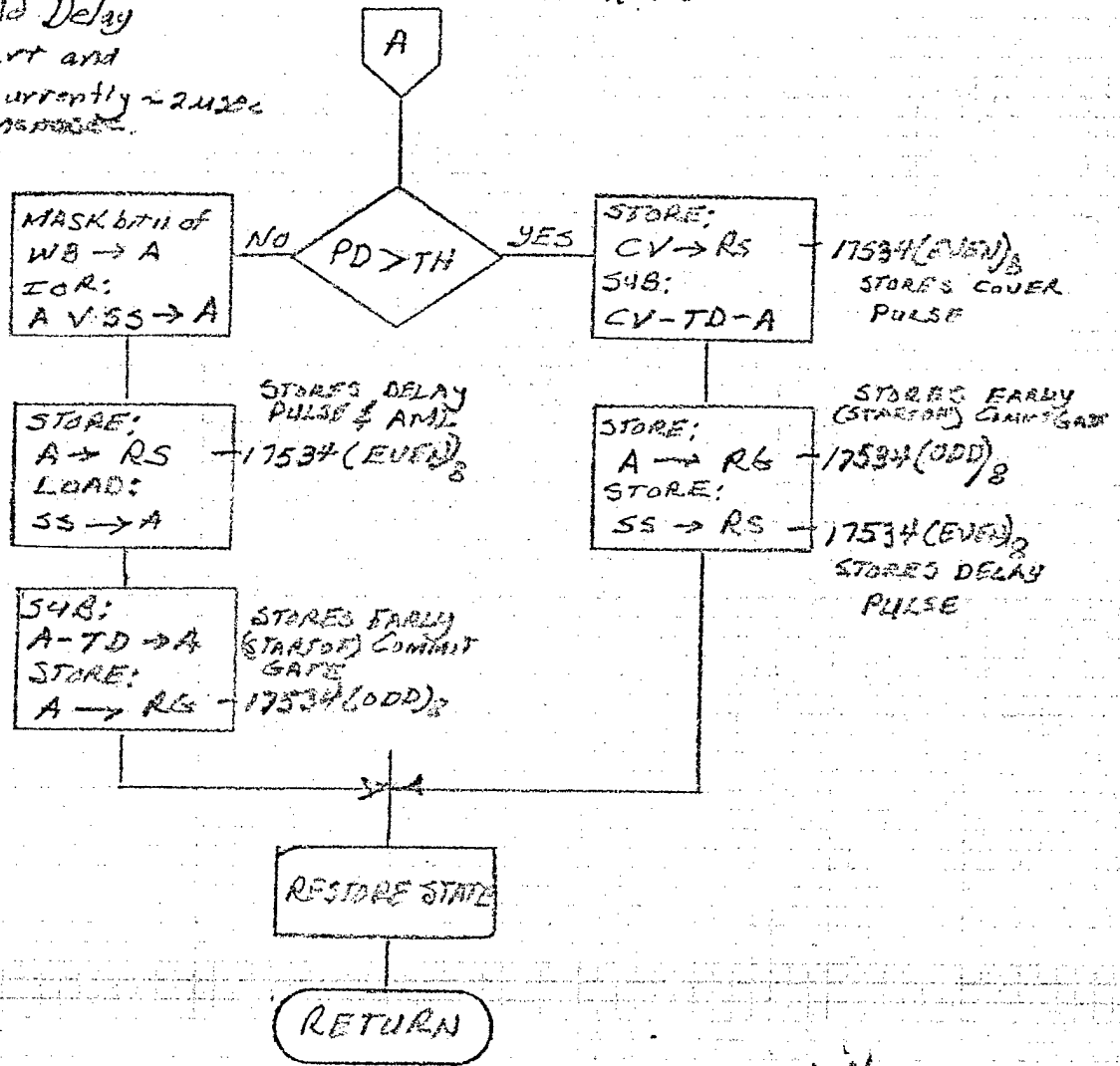
H.R. Mueller  
 7/26/76

FIG. 15 RANGE GATE PULL-OFF  
(CONT'D)

PAGE 2 of 2

TH is Threshold Delay  
for Cover Start and  
AMI check, currently ~ 2.4 usec  
LSB = 62.5 nanosec.

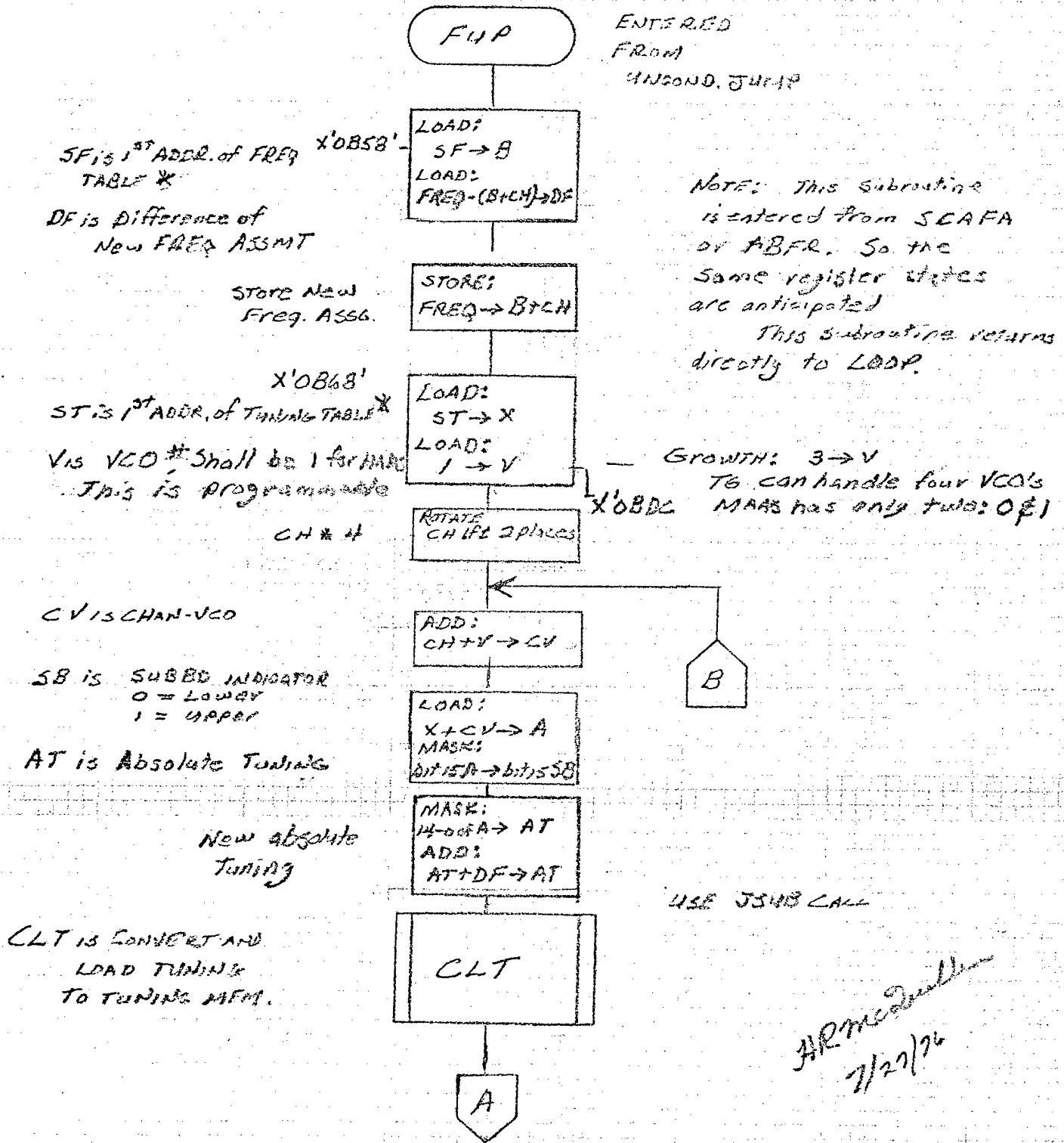
TD is TUNING  
Delay, CURRENTLY  
~ 10.4 usec.  
LSB = 62.5 nanosec.  
bit 11 of WB is  
AMI bit  
1 → AMI  
0 → AMI



HR McQuillen  
7/26/76

# FIG. 16 FREQUENCY UPDATE

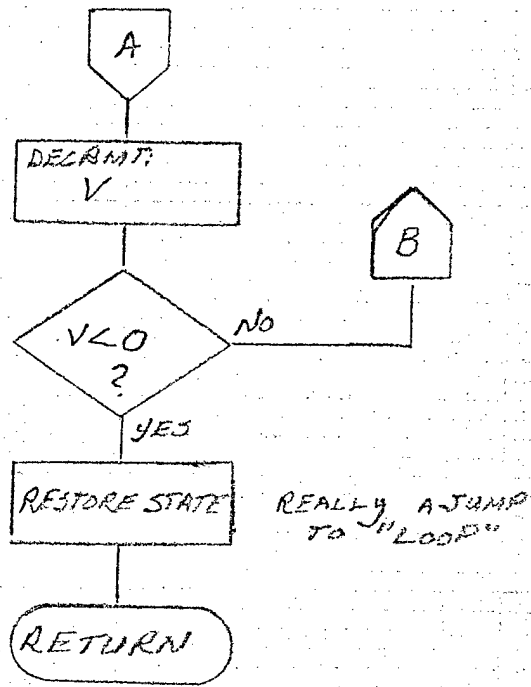
SUBROUTINE Page 1 of 2



\* See TABLE I for Freq & Tuning Tables - Structures.

FIG. 16 FREQUENCY UPDATE SUBR. (CONT'D)  
FUP

Page 2 of 2



HR 202/76  
7/27/76

### 3.2.16 Convert and Load Tuning (CLT) Subroutine

CLT is the subroutine of Figure 17. This subroutine shall convert the calculated absolute tuning frequency to tuning frequency by subband designation and relative subband tuning command. This routine assumes an upper subband VCO in the MAAS transmitter. It includes hysteresis for overlap of subbands, and assumes subband tuning is proportional above a lower value for each subband. The overlap and the lower values of each subband are programmable.

### 3.2.17 RAN-RAP A Version (RRA) Subroutine

RRA is the subroutine of Figure 18. This subroutine sets up the basic element pulse delay patterns for all RAN-RAP programs. It also sets up the basic commit gate start and end.

## 3.3 STORAGE AND PROCESSING ALLOCATION

The Technique Generator RP-16 Controller memory allocations are given in Figure 15 of reference 53959-HM-0410. Of the 4K-word memory, the upper 1K is currently allocated to T.G. Techniques Program memory. Within the remaining 3K, the software instructions and data objects of this CPDS are to fit. All other addresses are given in the cited reference and listed herein where needed.

Tables I through III are the important internal data-object tables for the T.G. Controller Program. Use of these tables is given in the appropriate functional description of paragraph 3.1. List I gives the RR/RGPO Generators priority and address assignments. List II summarizes important program data objects. List III allocates total RP-16 address space, including programs and data.

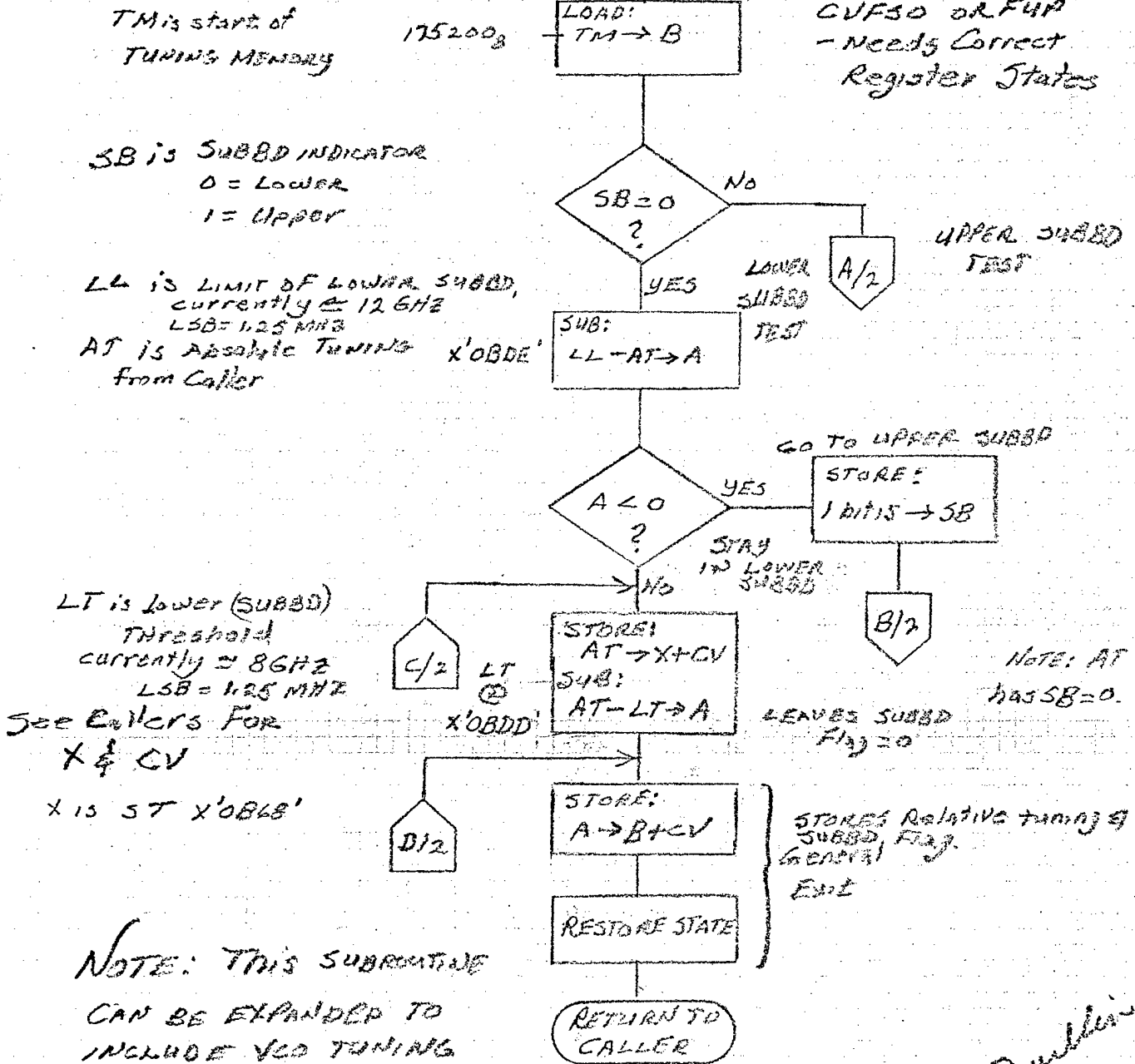
## 3.4 COMPUTER PROGRAM FUNCTIONAL FLOW

Program flow is described in paragraph 3.1 and Figure 1, and 2. Interrupt levels and assignments are given therein.

FIG. 17 CONVERT AND LOAD TUNING  
(TO TUNING MEMORY) SUBROUTINE

Page 1 of 2

SUBROUTINE IS ENTERED FROM CALLERS CVFSO OR FHP - Needs Correct Register States



NOTE: THIS SUBROUTINE CAN BE EXPANDED TO INCLUDE VCO TUNING CURVES IF LATER VCO TESTS SO INDICATE

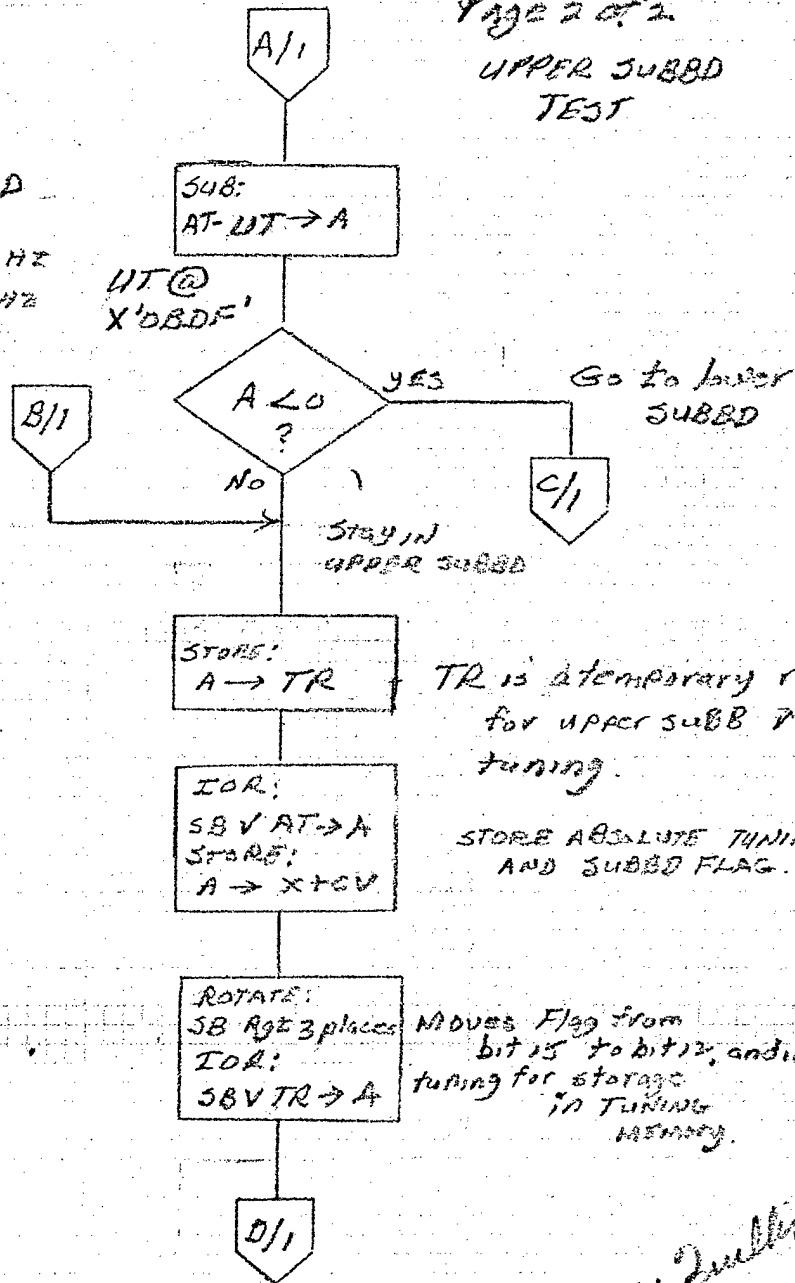
*J.R. McDaniel*  
7/27/76

# FIG 17 CONVERT AND LOAD TUNING SUB ROUTINE (CONT'D)

Page 2 of 2  
UPPER SUBBD TEST

UT IS UPPER SUBBD THREE  
Should be  $\approx 11.85$  GHz  
LSB = 1.25 MHz

UT @ X'DBDF'



X is from Caller,  
X = 3T

TR is a temporary register for upper subbd relative tuning.

STORE ABSOLUTE TUNING AND SUBBD FLAG.

MOVES Flag from bit 15 to bit 12, and includes rel. tuning for storage in TUNING MEMORY.

JR m. Sullivan  
7/27/76

# FIG. 18 RAN RAP A VERSION

SUBROUTINE

Page 1 of 3

RRA

SUBROUTINE  
ENTERED FROM  
CALLER ROUTINES  
RRC, RRCF, RRCL,  
OR RCCL  
Needs correct  
Register states.

MASK X'0E00'

MASK:  
RPW of WA → PW  
LOAD:  
PWS → B

PW is pulse width

X'0BES'

PWS is start of pulse width  
conversion table  
TABLE III

LOAD:  
B + PW → PW

X'0BE1'

PR is pretrigger,  
currently = 25.6 nSEC  
LSB = 62.5 nanosec

SUB:  
PR - PW → A  
LOAD?  
A → CV

CV is cover pulse  
start

STORE:  
A → PL

STORES COVER PLS

CC is CELL COUNT

PD is Primary Delay

PP is Primary Pull direction

MASK R-byte of  
WA → PD  
MASK bit 3 of  
WA → PP

FG is Fixed Gate delay

MASK from WA  
RFG → FG  
SHIFT FG Lft  
3 bits → FG

MASK X'F000'

FG \* 8

PL is pulse storage start X'0B70'

LOAD:  
1 → CC

X'0B3F'

ADD:  
CV + FG → A  
STORE:  
A → PL + CC

YES  
FG < PD ?

No  
PULL  
OUT

PP = 1 ?

YES  
PULL  
IN

FG < PD ?

YES

SUB:  
CV - FG → A  
STORE:  
A → PL + CC

STORES  
DROP  
PLS  
- PRIM.

INCRMT:  
CC + 1 → CC

No

No

No

No

No

No

INCRMT:  
CC + 1 → CC

STORES  
DELAY PLS  
- PRIM NEG

ADD:  
CV + PD → A  
STORE:  
A → PL + CC

STORE  
DELAY PLS  
- PRIM POS

SUB:  
CV - PD → A  
STORE:  
A → PL + CC

STORES  
DELAY PLS  
- PRIM NEG

EP is Early Primary  
Pulse  
Delay

LP is Late Primary  
Pulse  
Delay

ADD:  
2 \* PW + A → A

STORE:  
A → AP  
STORE:  
CV → EP

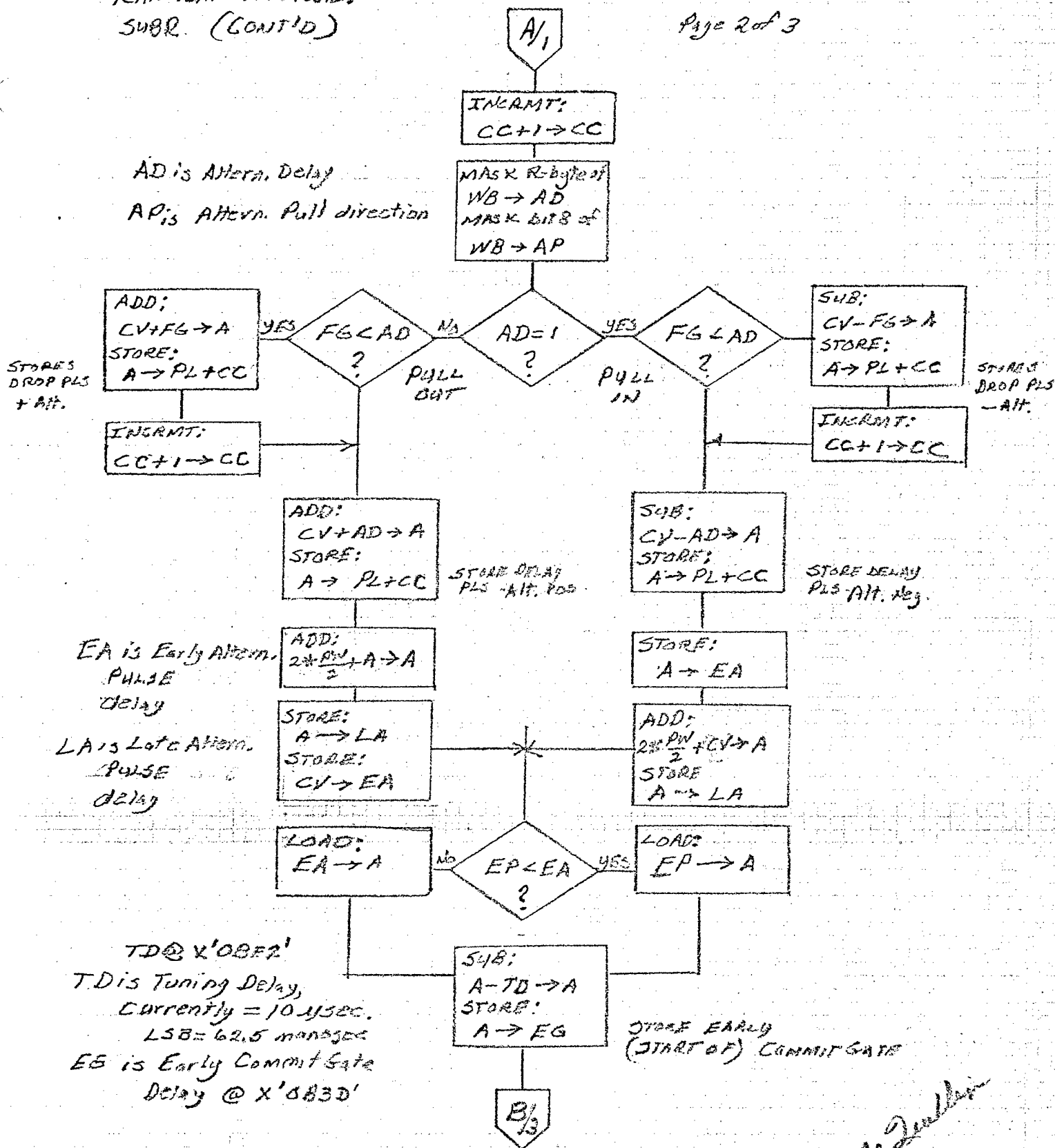
STORE:  
A → EP

ADD:  
2 \* PW + CV → A  
STORE:  
A → LP

A/2

H.R. McQuinn  
7/29/76

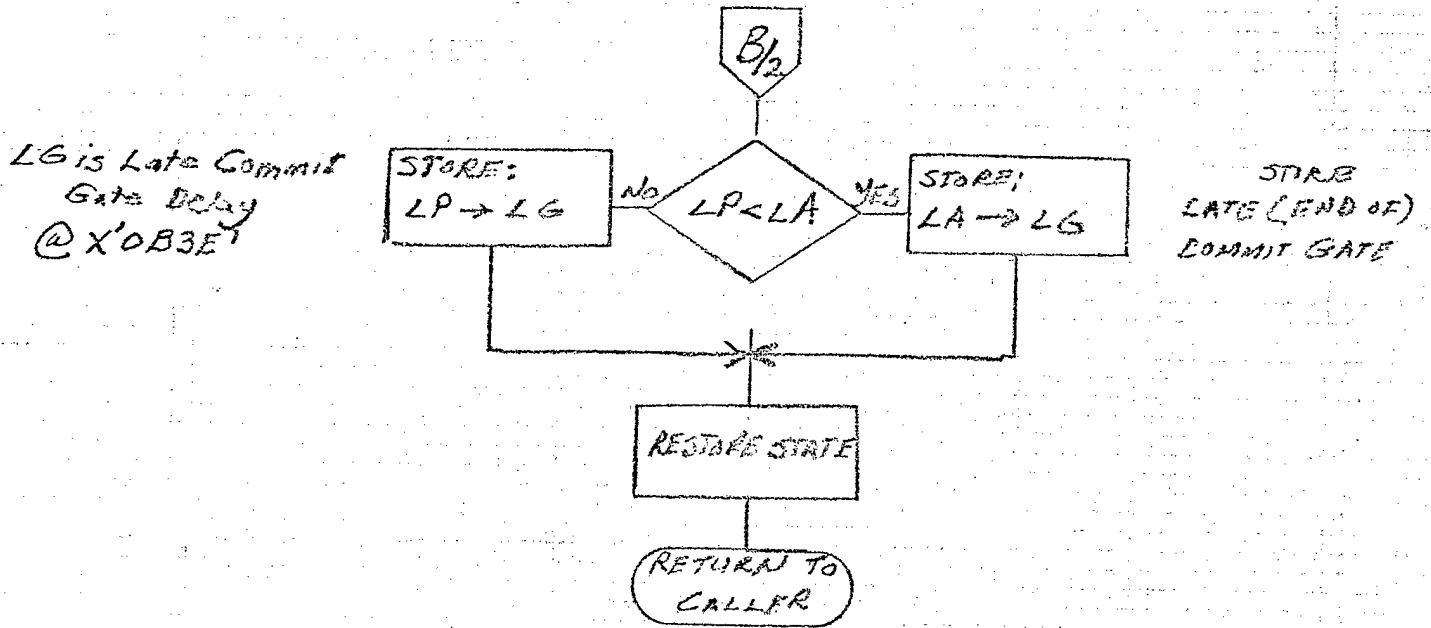
FIG. 18  
RAN-RAP A VERSION  
SUBR. (CONT'D)



HR McQuinn  
7/29/76

FIG. 1B  
RAN-RAP A VERSION  
SUBR (CONT'D)

Page 3 of 3



J.R. McQuillan  
7/29/76

TABLE I FREQUENCY AND TUNING LOCAL DATA STRUCTURES

SF IS FREQ ADDR. BASE	ADDRESS	DATA
	CH	LSB = 1.25 MHz
	SF + O <sub>H</sub>	FREQ (O <sub>H</sub> )
	• • •	• • •
	SF + F <sub>H</sub>	FREQ (F <sub>H</sub> )

14bits

ASSIGNED FREQUENCY TABLE

ST IS Tuning Addr. BASE	ADDRESS	DATA is AT = Absolute Tuning
	CV	LSB = 1.25 MHz AND
	ST + O <sub>H</sub> 0 <sub>B</sub>	TUN (O <sub>H</sub> 0 <sub>B</sub> )
	ST + O <sub>H</sub> 1 <sub>B</sub>	TUN (O <sub>H</sub> 1 <sub>B</sub> )
	ST + O <sub>H</sub> 2 <sub>B</sub>	TUN (O <sub>H</sub> 2 <sub>B</sub> )
	ST + O <sub>H</sub> 3 <sub>B</sub>	TUN (O <sub>H</sub> 3 <sub>B</sub> )
	• • •	• • •
	ST + F <sub>H</sub> 0 <sub>B</sub>	TUN (F <sub>H</sub> 0 <sub>B</sub> )
	ST + F <sub>H</sub> 1 <sub>B</sub>	TUN (F <sub>H</sub> 1 <sub>B</sub> )
	ST + F <sub>H</sub> 2 <sub>B</sub>	TUN (F <sub>H</sub> 2 <sub>B</sub> )
	ST + F <sub>H</sub> 3 <sub>B</sub>	TUN (F <sub>H</sub> 3 <sub>B</sub> )

bit = 15  
0 → SUBSD 1-LOWER  
1 → SUBSD 2-UPPER

TUNING TABLE

ALSO SEE LIST III

NOTE: THESE ARE USED IN FREQ UPDATE (FUP) SUBROUTINE, AND CHANNEL-VCO FREQ SETTING (CVF20) MODULE.

AR. Macmillan  
7/30/76

TABLE II CHANNEL-RESOURCE, AND RESOURCES LOCAL DATA STRUCTURES

CRS is CHAN-RESOURCE STATUS ADDR. BASE	ADDRESS CH	DATA-bits			FN - OCTAL
		15,14	13-3	2-0	0 - NONE 1 - GEN #1 2 - GEN #2
USED BY INITIALIZATION (INLZ) MODULE, SC TECH ASSMT (SCTA) MODULE AND SC TECH-CH PARM. CHS OR DISMISS MODULE (SCTEC).	CRS + 0H	FN	ZERO	RN	RN - OCTAL 0 - NONE 1 - GEN 1 2 - GEN 2 3 - GEN 3 4 - GEN 4
	CRS + FH	FN	ZERO	RN	

CHANNEL-RESOURCE TABLE

SRS is RR/RGPO GEN STATUS ADDR. START	ADDRESS RN RR/RGPO GEN #	DATA - HEX	HEX	
			SH	MEANING
USED BY INITIALIZATION (INLZ) MODULE	SRS + 1B	0005H	0	AVAILABLE
	...	...	1	NOT AVAILABLE
	SRS + 4B	0005H		

RR/RGPO GENERATOR PRE-OPERATION STATUS TABLE

SRA is RR/RGPO GEN. ALLOCATION ADDR.	ADDRESS RN RR/RGPO GEN #	DATA - HEX	HEX	
			AH	MEANING
USED BY INITIALIZATION (INLZ) MOD, SC TECH ASSMT. (SCTA) MODULE, AND SC TECH-CH DISMISS (SCTEC) MODULE	SRA + 1B	000AH	0	NOT ALLOCATED
	...	...	1	ALLOCATED
	SRA + 4B	000AH		

RR/RGPO GENERATOR ALLOCATION (OPERATION) TABLE

ALSO SEE LIST III

RR THE 2nd Edition  
7/30/76  
REVISED 11/29/76

TABLE II A RESOURCES LOCAL DATA STRUCTURE CONTINUED

SFS IS FM GEN STATUS ADDR START	ADDRESS		DATA HEX	HEX	
	+	FN FM GEN #		HEX	MEANS
	SFS	+	1	0005 <sub>H</sub>	0 AVAILABLE
	SFS	+	2	0005 <sub>H</sub>	1 NOT AVAIL ABLE

USED BY  
INLE MOD.

FM GENERATOR PRE-OPERATION  
STATUS TABLE

SFA IS FM GEN ALLOCATION ADDR	ADDRESS		DATA HEX	HEX	
	+	FN FM GEN #		HEX	MEANS
	SFA	+	1	000A <sub>H</sub>	0 AVAILABLE
	SFA	+	2	000A <sub>H</sub>	1 NOT AVAIL ABLE

USED BY  
INLE, SFTA,  
SCTE, MADS

FM GENERATOR ALLOCATION  
(OPERATION) TABLE

Howard McQuillan  
11/29/76

TABLE III RAN-RAP PULSE DELAY STORAGE AND PULSE WIDTH CONVERSION TABLE

	ADDRESS CC CELL COUNT	DATA bits 7-0 USED LSB = 22.5 microsec.
PL's pulse storage start CC is cell count	PL + 0	PULSE DELAY (1)
Used by All RAN-RAP MODULES AND SUB ROUTINE.	PL + 5	PULSE DELAY (4)

NOTE:  
ALLOW FOR 2 1/12 LOCATIONS

RAN-RAP PULSE DELAY TABLE

	ADDRESS PW PIS Width Code	DATA - $\frac{PW}{2}$ bits 5-0 LSB = 62.5 microsec
Puls is Pulse Width Conversion	PWS + 18	1.5 usec = 30
	+ 38	1.0 usec = 20
	+ 58	0.5 usec = 10
	+ 68	0.25 usec = 5

PULSE WIDTH CONVERSION TABLE

ALSO SEE LIST III

A.R. McZullin  
1/30/74

LIST I RR/RGPO GENERATORS-  
PRIORITY LEVEL, AND ADDRESS  
LSB ASSIGNMENTS

GEN#	(PRIORITY) LVL <sub>8</sub>	WRITE ADDRESS 3 LSBs	
		* EVEN <sub>8</sub>	# ODD <sub>8</sub>
1	5	0	1
2	4	2	3
3	3	4	5
4	2	6	7

HIGHER  
NUMBER  
= HIGHER  
PRIORITY

\* PULSE STROBE DELAY MEMORY

# COMMIT GATE DELAY MEMORY

J.R. McQuillan  
7/30/76

## LIST III IMPORTANT DATA - OBJECTS AND USERS

REF	DATA ITEM	DESCRIPTION	USING MODULE(S) OR SUBROUTINE(S)
CT	Count - No. Loop entries after INLE		INLE, LOOP
CRS	Channel Resource Table Start		INLE, SCTA, SCTCE
SRS	Start of RR/RGPs Status Table - Programmable	Pre-Run	INLE
SRA	Start of RR/RGPs Allocation Table - During Run		INLE, SCTA, SCTCE
PS	(Technique) Program Start - 0060000 Program 1.	Pre-Run	SCTA, SCTCE
SF	Start of Frequency (Assignment) Table		CVF30, FUP
ST	Start of Tuning (Absolute) Table		CVF30, FUP
PL	Pulse Storage Start		RRC, RRA, RRCE RRC4, RRCE4
EG	Early (Commit) Gate - start		RRC, RRA, RRCE RRC4
LG	Late (Commit) Gate - end		RRC, RRA, RRCE RRC4, RRCE4
TD	Tuning Delay	Pre-Run Programmable	RRA
PR	Pre-trigger Delay	Pre-Run Programmable	RRA

A. L. Mc. Dunderlin  
7/20/76

LIST II (CONT'D) IMPORTANT DATA-OBJECTS AND USERS

REF.	DATA ITEM	DESCRIPTION	USING MODULE(S) OR SUBROUTINE
EO	Early (Element) Offset	Pre-Run Programmable	RRCE, RRCEL
LO	Late (Element) Offset	Pre-Run Programmable	RRCL, RRCEL
PWS	Pulse Width Conversion Star Table	Pre-Run Programmable Table F1110	RRA
CH	Channel	VARIABLE 0 thru 15	INLE, SGAFA, SCTCE, CUF50, ABFR
RN	RR/RGPO.GEN. NO.	VARIABLE 1 thru 4	INLE, SGAFA, SCTCE, CUF50, ABFR
AN	ANGLE CELL NO.	VARIABLE 0 thru 31	SGAFA
TN*8	Technique No.	VAR. 0000 thru 1770 <sub>B</sub> with LS <sub>B</sub> always 08	SCTA, SCTCE
CC	Cell Count-RAN-RAP Delay	Pulse No. VARIABLE	RRC, RRA, RAGE, RRCL, RRCEL
TH	Threshold Delay for Coverinsert	Pre-run Programmable	RGPO
LL	Lower Subband Limit Tune	Pre-run Programmable	CLT
LT	Lower Subband Threshold Tune Freq.	Pre-run Programmable	CLT
UT	Upper Subband Thres; Tune (confid)	Pre-run Programmable	CLT


RR, RRCE, RRCEL  
1/30/76

### 3.5 PROGRAMMING GUIDELINES

Object program shall be machine code suitable for loading from the System Controller (SC) via the Daisy Chain (DC) bus. During development object program shall be available on paper tape for loading via a TTY terminal directly into the T.G. The latter includes an Asynchronous Line Control Module (ALCM) for TTY interface and a Hardware Loader program to accept inputs. Word formats and addresses are given in Figures 15, 16 and 17 of reference 53959-HM-0410.

Source programming can be in assembly language. The source program can be converted to object program using either the RP-16 Assembler, reference Equipment Division II, or the ESD Nova Cross-Assembler for the RP-16. RP-16 instructions and functions are described in reference Equipment Division I.

LIST III TGU RP-16 ADDRESS SPACE PAGE 1 OF 4

LOCATION HEX	DATA	DATA TYPE
0000	VECTOR ADDR. "INLZ" = X'0050'	(START OF 4K MEM.) DEFINED 110
0001 ... 006F	INTERRUPT VECTOR ADDR'S CURRENT & GROWTH SEE TGU HARDWARE SPEC	DEFINED DURING CODING & ASSEMBLY 11110
INLZ = 0070	T.G. PROG INSTR'S & START INLZ & PROG. DATA NOT ELSEWHERE	INSTR & DATA 91210
...		
03FF	ESTIMATED LIMIT OF PROG INSTR/DATA	
0400	GROWTH 	185310
STACKI-1 = 083C	↑ STACK TOP OF STACK USED	VAR.

TOTAL = 2877

HR. m. d. w. l. n.  
9/5/76

LIST III TGU RP-16 ADDRESS

REVISED  
11/27/76

SPACE (CONT'D) PAGE 2 of 4

LOCATION HEX	DATA	DATA TYPE	
EG = 0B3D	EARLY GATE - RAN-RAP	VAR	1 <sub>10</sub>
LG = 0B3E	LATE GATE - RAN-RAP	VAR	1 <sub>10</sub>
CC = 0B3F	CELL COUNT - #RR PL'S	VAR	1 <sub>10</sub>
PL = 0B40	PULSE STORAGE FOR	VAR	
...	RAN-RAP		24 <sub>10</sub>
0B57			
SF = 0B58	FREQ (ABSOLUTE) FOR	VAR	
...	CHANNEL ASSIGNMENTS		15 <sub>10</sub>
0B67	- TABLE I		
ST = 0B68	TUNING (ABSOLUTE) FOR CHAN-	VAR	
...	VCO ASSGNMTS - TABLE I		64 <sub>10</sub>
0BA7			
CRS = 0BAB	CHANNEL-RESOURCE TABLE	VAR	16 <sub>10</sub>
0BB7	- TABLE II		
SFA = 0BB8	BASE } FM GEN. CURRENT	VAR	3 <sub>10</sub>
0BB9	GEN#1 } OPERATION ALLOCATION		
0BBA	GEN#2 } TABLE IIIA		
SFS = 0BB8	BASE } FM GEN. PRE-OPER.	PRE-PROG'D	3 <sub>10</sub>
0BBC	GEN#1 } STATUS TABLE IIIA		
0BBD	GEN#2 }		
0BBE			
0BDB	NOT USED - RESERVE		30 <sub>10</sub>
V = 0BDC	HIGHEST No.'s VCO. For MMS enter 1.*	PRE-PROGRAM	1 <sub>10</sub>

\* Note: TGU can handle 3, i.e. four VCO's TOTAL 153<sub>10</sub>  
VCO's are numbered: 0, 1, ...

J.R. McQuinn  
7/8/76  
REV 11/27/76

LIST III TGU RP-16 ADDRESSES  
SPACE (CONT'D) PAGE 3 OF 4

LOCATION HEX	DATA	DATA TYPE	
LT = 0BDD	LOWER SUBBD THRES. TUNE	PRE-PRGMD	
LL 0BDE	LOWER SUBBD HI LIMIT TUNE	(USE VALUES IN P2310 CHARTS)	
LIT = 0BDF	UPPER SUBBD THRES TUNE		
TH = 0BE0	THR. DELAY FOR COVER, AMI RSPD		
PR = 0BE1	RR/RSPD PRE-TRIG DELAY		8 <sub>10</sub>
TD = 0BE2	RR/RSPD TUNING DELAY		
LO = 0BE3	RR LATE OFFSET		
EO = 0BE4	RR EARLY OFFSET		
PWS = 0BE5	PULSE WIDTH CONVERSION TABLE - RR/RSPD	PRE-PRGMD (USE TABLE III Now)	8 <sub>10</sub>
...			
0BEC			
SRA = 0BED	NOT USED - GROWTH		1 <sub>10</sub>
OBEE	GEN#1	RR/RSPD GEN. CURRENT OPERATION ALLOCATION	VAR. 4 <sub>10</sub>
...	...		
OBFI	GEN#4		
		TABLE II	
SRS = 0BF0	NOT USED - GROWTH		1 <sub>10</sub>
0BF3	GEN#1	RR/RSPD GEN. PRE-OPER. STATUS TABLE II	PRE-PRGMD (PRG. ALL AVAILBL Now)
...	...		
0BF6	GEN#4		
0BF7	SC-TG MESSAGE REG'S	VAR.	
...	SEE TGU HARDWARE SPEC		9 <sub>10</sub>
0BFF			

ALM 2/11/75  
9/8/75  
TOTAL 35<sub>10</sub>

LIST III TGU RP-16 ADDRESS SPACE (CONT'D) PAGE 40FF

LOCATION HEX	DATA	DATA TYPE	
0C00	TECHNIQUE PROGRAM	PRE-PRGMD	
...	MEMORY	(TO BE SUPPLIED)	102 <sub>10</sub>
4095 <sub>10</sub> 0FFF	SEE TGU HARDWARE SPEC FOR FORMAT	(END OF 4K MEM.)	
1000			
...	GROWTH PERIPH.		59,904 <sub>10</sub>
F9FF			
64,000 <sub>10</sub> FA00	TG INTERNAL PERIPHERALS	VAR.	
...	SEE FLOW CHARTS AND TGU HARDWARE SPEC.		256
FAFF			
FB00			
	GROWTH		256
FBFF			
64,512 <sub>10</sub> FC00	ALCM STATUS/ENTRL REG	VAR.	1 <sub>10</sub>
	ALCM DATA REG.	VAR.	1 <sub>10</sub>
FC02			
	GROWTH		765 <sub>10</sub>
FEFE			
FEFF	PIN DISABL. REG.	VAR.	1 <sub>10</sub>
FF00	FIRMWARE PROGRAM - PIN	FIXED	
...	HARDWARE LOADER	INSTR.	256 <sub>10</sub>
65,535 <sub>10</sub> FFFF			

TOTAL = 62,464<sub>10</sub>  
 H. M. ...  
 9/8/76

TABLE A. TCU SOFTWARE-TECHNIQUES  
PROGRAM MEMORY DATA

PROGRAM	ADDRESS	DATA
No. 9	0C48	0021
XILM, RGN	9	1D82
	A	2140
	B	3000
	C	C004
	D	DB96
	↓ E	F330
No. 13	0C68	0020
XICS-1, RGN	9	1CA4
	A	21A2
	B	3080
	C	C004
	D	D933
	↓ E	F830
No. 31	0CF8	0020
XICS-2, RGN	9	1524
	A	2142
	B	30C1
	C	C003
	D	DF54
	↓ E	F830

TABLE A. TGU SOFTWARE TECHNIQUE'S  
PROGRAM MEMORY DATA

PROGRAM	ADDRESS	DATA
No. 41	OD48	0020
XASWM-C, RGPD	9	1692
	A	2142
	B	3061
	C	A61C
	D	B347
	E	C005
	Y F	F830
No. 53	ODA8	0020
XASWM-C, RGN, FM	9	1A82
	A	2505
	B	3126
	C	84D4
	D	93C0
	E	C002
	Y F	D947
	ODBO	F830
No. 65	OE08	000C
XSSWM, RR-3	9	1208
	A	2000
	B	3086
	C	A31B
	D	B99C
	E	C004
	Y F	F830

TABLE A. TCU SOFTWARE TECHNIQUES PROGRAM MEMORY DATA

PROGRAM	ADDRESS	DATA
No. 73	0E48	0020
XASUM-T, RR-3	9	1708
	A	2040
	B	3035
	C	A31B
	D	B99C
	E	C004
	V F	F830
No. 91	0ED8	0020
RCW, ASUM-C	9	1480
	A	2281
	B	3147
	V C	F520