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Moderated Degradation Enhancement of Lateral Pnp Transistors Due to Measurement Bias

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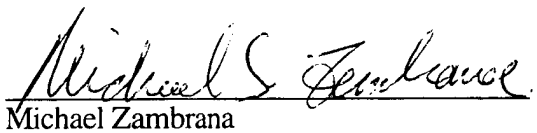

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Enhanced low-dose-rate gain degradation of ADI RF25 lateral pnp transistors is examined as a function of the bias at which the gain is measured. Degradation enhancement at low dose rates diminishes rapidly with increasing measurement bias between the emitter and the base. Device simulations reveal that interface trap charging, field effects from oxide trapped charge and emitter metallization, base series resistance and high-level carrier injection all contribute to this behavior. As a practical consequence, accelerated hardness assurance tests of this device require higher irradiation temperatures or larger design margins for low power applications.

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Moderated Degradation Enhancement of Lateral pnp Transistors Due to Measurement Bias

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Abstract

Enhanced low-dose-rate gain degradation of ADI RF25 lateral pnp transistors is examined as a function of the bias at which the gain is measured. Degradation enhancement at low dose rates diminishes rapidly with increasing measurement bias between the emitter and the base. Device simulations reveal that interface trap charging, field effects from oxide trapped charge and emitter metallization, base series resistance and high-level carrier injection all contribute to this behavior. As a practical consequence, accelerated hardness assurance tests of this device require higher irradiation temperatures or larger design margins for low power applications.

I. INTRODUCTION

Radiation-induced degradation of many types of bipolar transistors[1,2] and circuits[3] is more severe following low dose rate exposure than following high dose rate exposure. Since microelectronics devices in space are generally subjected to low dose rate irradiation, this complicates the hardness assurance testing of linear circuits and can lead to an overestimation of device lifetimes in space. Of the various approaches tried for hardness assurance testing, the most promising has been high dose rate irradiation at elevated temperature with some measure of design margin to account for in situ annealing[1,2].

Due to their keen sensitivity to radiation, lateral pnp transistors have been the focus of much of the recent work in this area. Ionizing radiation degrades the current gain of lateral pnp transistors primarily by introducing interface traps into the oxide overlying the emitter-base junction[4]. The interface traps increase surface recombination in the base by acting as generation-recombination centers. Conversely, radiation-induced net positive oxide trapped charge can moderate gain degradation as it accumulates the surface of the n-type base. Since recombination is at a maximum when the concentrations of conduction electrons and holes are equal, positive oxide trapped charge reduces recombination in the base by creating an imbalance in carrier concentrations near the surface.

The amount of design margin required to bound low-dose-rate gain degradation of bipolar transistors is known to depend on total dose[2], irradiation temperature[1,2], device geometry[1], irradiation bias[3] and the dose rate at which testing is performed[5]. In this work, we report that the amount of design margin required to bound radiation-induced gain degradation of lateral pnp transistors also depends on the bias at which the gain is *measured*. This dependence results from a moderation in low-dose-rate degradation enhancement as the emitter-to-base bias is increased. Mechanisms contributing to this behavior include interface trap charging, field effects from oxide trapped charge and emitter metallization, base series resistance and high-level carrier injection.

II. EXPERIMENT

This work draws on an extensive data set introduced elsewhere[1,2] that relates gain degradation of the Analog Devices RF25 lateral pnp transistor to dose rate and irradiation temperature. This device is fabricated in a Si bipolar process with a highly doped emitter (~9×10^{19} cm^{-3}) and a base oxide thickness of 570 nm[6]. All irradiations were performed using a ^{60}Co γ-source with the device terminals grounded. Lids on the device packages were removed to avoid dose enhancement from photon scattering[7], and Pb-Al shields were used to filter low energy photons and electrons. Further details concerning the experimental procedure are provided elsewhere[1].

A typical example of the effect of dose rate on excess base current is shown in Fig. 1(a)[1], where excess base current is defined as the increase in base current due to radiation exposure. The excess base current is plotted as a function of emitter-to-base voltage for devices irradiated to 20 krad(Si) at four dose rates between 0.001 and 294 rad(Si)/s. Base recombination increases monotonically with decreasing dose rate for any emitter-to-base voltage examined. However, the *magnitude* of this increase diminishes rapidly with increasing bias. Furthermore, the slope of the excess base current characteristics at any given dose rate decreases with bias. This

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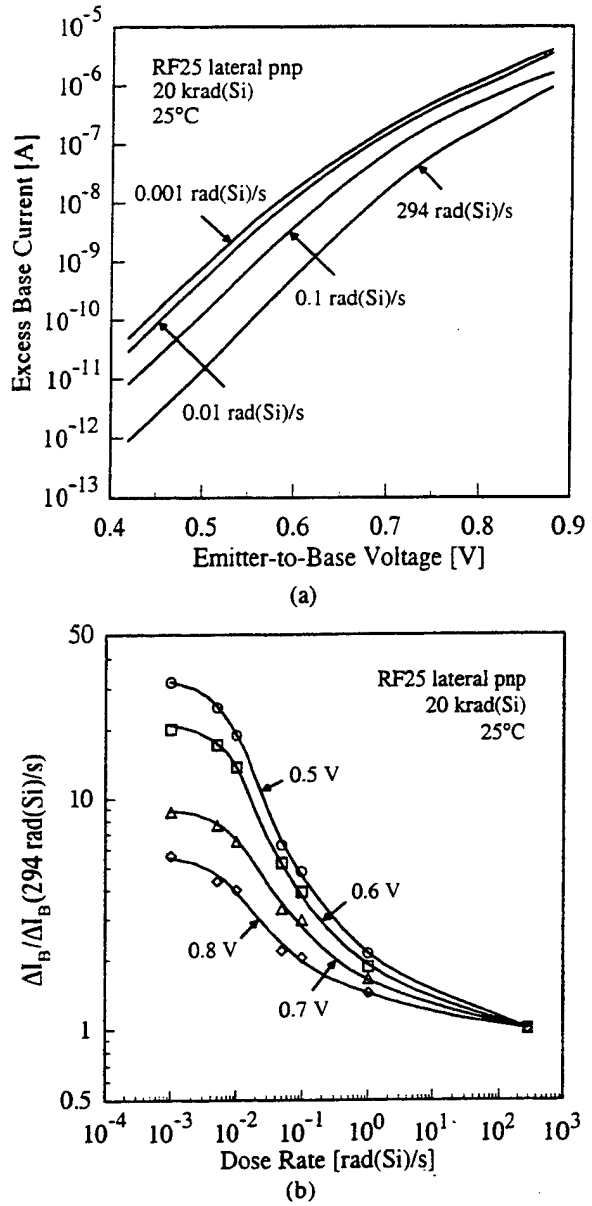

Fig. 1. Effect of (a) emitter-to-base voltage on excess base current, where dose rate is a parameter (after [1]), and (b) dose rate on excess base current, where emitter-to-base voltage is a parameter. The sensitivity of excess base current to dose rate diminishes with increasing measurement bias between the emitter and the base.

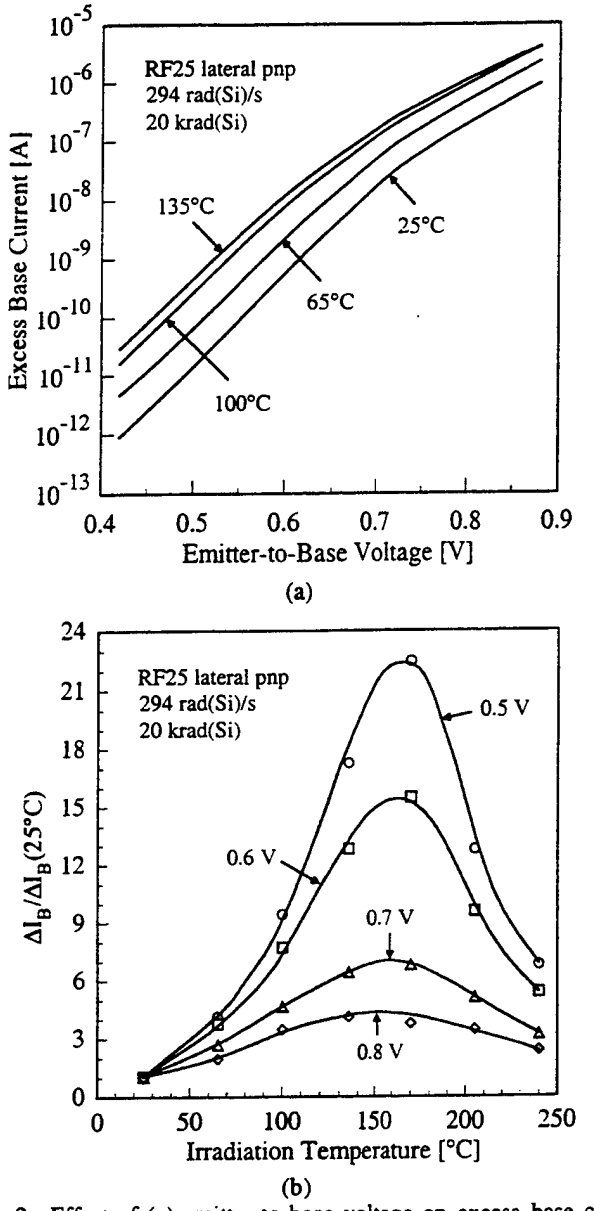

Fig. 2. Effect of (a) emitter-to-base voltage on excess base current, where irradiation temperature is a parameter (after [1]), and (b) irradiation temperature on excess base current, where emitter-to-base voltage is a parameter. The sensitivity of excess base current to irradiation temperature diminishes with increasing measurement bias between the emitter and the base.

dependence on measurement bias is illustrated more clearly in Fig. 1(b), where excess base current, normalized by its value at 294 rad(Si), is plotted as a function of dose rate for four emitter-to-base voltages between 0.5 and 0.8 V. The ratio of excess base currents at the extreme dose rates increases from approximately six at 0.8 V to more than 30 at 0.5 V.

In Fig. 2(a), representative excess base current characteristics are shown for lateral pnp devices irradiated to 20 krad(Si) at four temperatures between 25 and 135°C[1], where the dose rate is fixed at 294 rad(Si)/s. For any emitter-to-base voltage examined, degradation increases monotonically with temperature. However, similarly to the case for dose rate, the *amount* of degradation enhancement diminishes rapidly with increasing bias. This result is illustrated more clearly in Fig. 2(b), where normalized excess base current is plotted as a function of irradiation temperature for four emitter-to-base voltages between 0.5 and 0.8 V. The enhancement in degradation due to temperature is moderated by in situ annealing such that a distinct peak in the excess base current occurs for a given bias[1,2,8]. This peak moves to lower irradiation temperatures with increasing bias. The factor by which excess base current is maximally enhanced increases from less than five at 0.8 V to approximately 23 at 0.5 V. Qualitatively similar trends in the measurement bias dependence of degradation enhancement were observed at other total doses examined through 200 krad(Si).

III. MECHANISMS

A. Oxide Trapped Charge

Excess base current in the lateral pnp transistor results primarily from surface recombination within the emitter-base depletion region. The amount of excess base current flowing at the Si surface is obtained from

$$\Delta I_B = q\int_S U\,dS, \tag{1}$$

where q is the electronic charge, U is the recombination rate per unit area, and S is the surface area over which recombination takes place. The rate of recombination typically is at a maximum near the emitter-base metallurgical junction, where the carrier concentrations are comparable.

When the surface recombination is formulated from Shockley-Read-Hall recombination statistics[9], integration of (1) yields a bias dependence for excess base current that can be approximated by[4]

$$\Delta I_B \propto \exp\left[\frac{(V_{EB}-V_{acc})}{mV_{th}}\right], \tag{2}$$

where $V_{th} = kT/q$ is the thermal voltage, V_{EB} is the applied emitter-to-base voltage, V_{acc} represents the potential drop across the accumulation layer in the neutral base, and m is defined as the ideality factor. Recombination far from the emitter-base junction contributes an ideality factor of one. For recombination occurring at the maximum rate (near the emitter-base junction), an ideality factor greater than one results. The excess base current, therefore, exhibits a weaker dependence on applied bias when the function U is more sharply peaked near the emitter-base junction.

In Fig. 3, recombination rates along the Si surface are shown for several densities of positive oxide trapped charge.

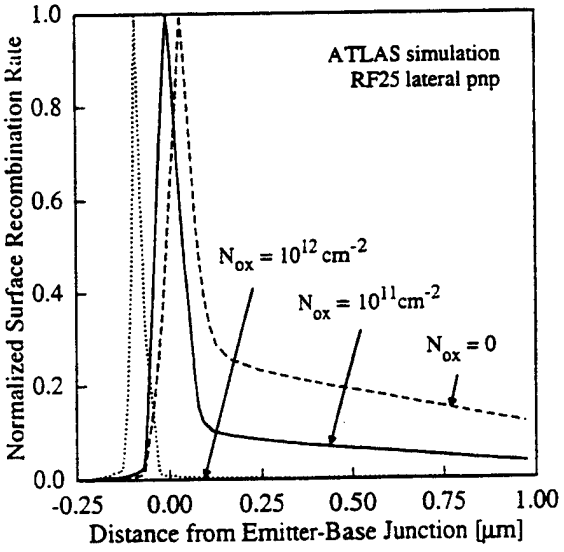

Fig. 3. Effect of positive oxide trapped charge on the surface recombination rate near the emitter-base junction. Positive oxide trapped charge moderates recombination at the base surface while reducing the emitter-base depletion width.

The recombination rates were obtained from two-dimensional computer simulations[10] of the test device and are normalized by the peak rate for constant values of surface recombination velocity and emitter-to-base voltage. Negative abscissas in the figure correspond to locations within the emitter, whereas positive values are located within the base. Positive oxide trapped charge reduces both the emitter-base depletion width and recombination in the neutral base by increasing the difference in carrier concentrations near the base surface. Since reduced recombination in the neutral base leads to a larger ideality factor, the enhancement in excess base current at low dose rates is reduced with increasing emitter-to-base voltage.

B. Interface Trapped Charge

Radiation-induced changes in the surface recombination rate are determined by the sum of bulk oxide trapped charge and charged interface traps. As shown in Figs. 4(a) and 4(b), the net charge contributed by interface traps varies with emitter-to-base bias. The conduction and valence band edges are represented by E_c and E_v, respectively, and E_i denotes the intrinsic energy. The Fermi energy, E_F, indicates the energy below which most of the interface traps are occupied at thermal equilibrium. Under forward bias, the trap occupancies are implied by an effective Fermi energy, F_{eff}, defined as the mean of the carrier quasi-Fermi energies, F_N and F_P.

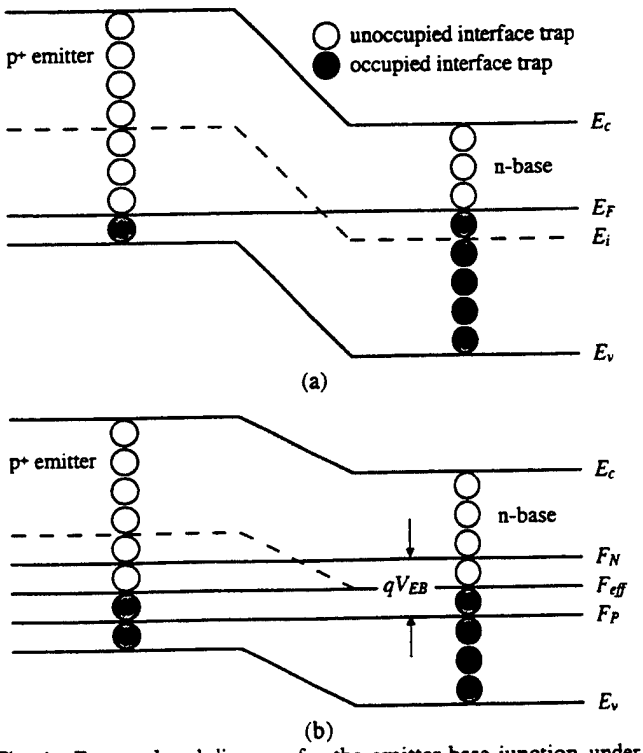

Fig. 4. Energy band diagram for the emitter-base junction under (a) thermal equilibrium and (b) forward bias. A forward bias moderates carrier recombination along the surface by charging interface traps positive in the base and negative in the emitter.

Under forward bias, the quasi-Fermi energies split by an amount proportional to the applied bias, such that F_N increases in the emitter, and F_P decreases in the base[11]. Some of the interface traps in the base become more positively charged as they emit electrons (or capture holes), while some of the interface traps in the emitter become more negatively charged as they capture electrons (or emit holes). The additional charge above the base moderates base recombination by complementing positive charge trapped in the oxide bulk. The negative charge above the emitter further reduces recombination by mitigating depletion of the emitter. Since the amount of interfacial charge trapping increases with bias, the excess base current characteristics tend to fall off at large biases. Because the doping concentrations in the regions differ, the impact of interface trapped charge on recombination is greater in the base than in the emitter.

C. Emitter Metallization

In most bipolar devices, the emitter metallization covers the base oxide over a portion of the emitter-base depletion region. This overlap functions as a field plate similar to a gate electrode in an metal-oxide-silicon capacitor[12]. As the emitter-base junction is forward biased, charge added to the metal layer reduces the region of high recombination in the underlying depletion region while increasing the potential drop across the accumulated neutral base (V_{acc} in (2)). The excess base current, therefore, is reduced to a value below that which would exist without the presence of the field plate. Since the relative reduction increases with the amount of charge on the field plate, the excess base current characteristics are stretched out for large emitter-to-base voltages. The effects of the field plate and positive oxide trapped charge are conceptually the same; that is, each acts to moderate the effect of near-midgap interface traps by increasing the surface potential in the Si.

D. High-Level Injection and Base Series Resistance

At large forward currents, such that the number of minority carriers injected into the base approaches the majority carrier concentration, non-negligible electric-fields can result in significant ohmic drops across the bulk emitter and base regions[11]. The amount of potential drop increases with current so as to limit further injection of carriers. Since the rate of recombination in the depletion region depends on the concentration of injected carriers, excess base current increases more slowly with emitter-to-base voltage at large levels of current. Sufficiently high-level injection can yield an ideality factor that approaches two.

Base series resistance also contributes to the convergence of excess base current at large biases. An appreciable distributed resistance generally is present in the quasi-neutral region of the base[11]. This resistance often is significant in lateral pnp transistors due to the separation of the base electrode from the device active region. Since majority carriers in the base must flow into the active area to facilitate recombination and back-injection into the emitter, the applied emitter-to-base voltage is divided across the emitter-base depletion region and the base bulk. The metal-to-silicon contact at the base terminal likewise behaves like a small resistor that adds to the voltage drop. The effect of series resistance is represented in (2) by expressing the junction voltage as $V_{EB} - V_{acc} - I_B R_B$, where $I_B R_B$ represents the potential drop across the base.

IV. HARDNESS ASSURANCE IMPLICATIONS

Fig. 5 illustrates the relationship between irradiation temperature and design margin required to bound low dose rate degradation of the test device at 20 krad(Si), where emitter-to-base voltage is a parameter. The figure was constructed by comparing excess base currents obtained at 294 rad(Si)/s and elevated temperatures to those acquired at 0.001 rad(Si)/s. The ordinates represent safety factors by which the high-temperature data must be multiplied in order to approximate the low dose rate response. Because gain degradation and the underlying mechanisms can vary widely among technologies and device types, it should be emphasized that the optimum values of temperature and design margin implied by this figure apply strictly to the device studied.

At any irradiation temperature considered, the amount of design margin required to bound low dose rate degradation decreases with measurement bias. The dependence of design margin on bias generally grows stronger as the irradiation temperature moves away from its range of optimum values.

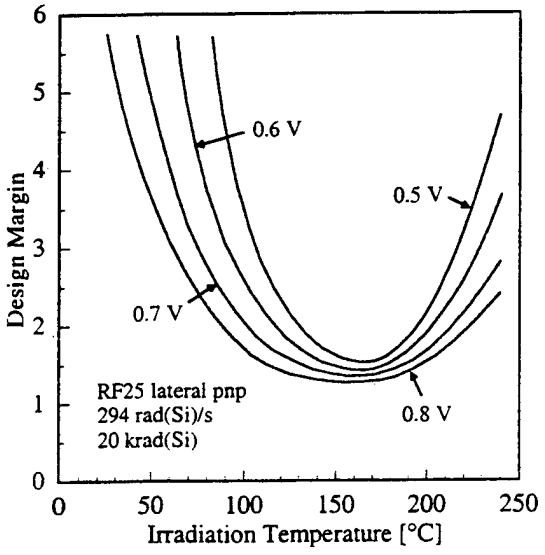

Fig. 5. Relationship between irradiation temperature and design margin required to bound low dose rate degradation of the RF25 lateral pnp transistor. At any given irradiation temperature, the required design margin decreases with measurement bias.

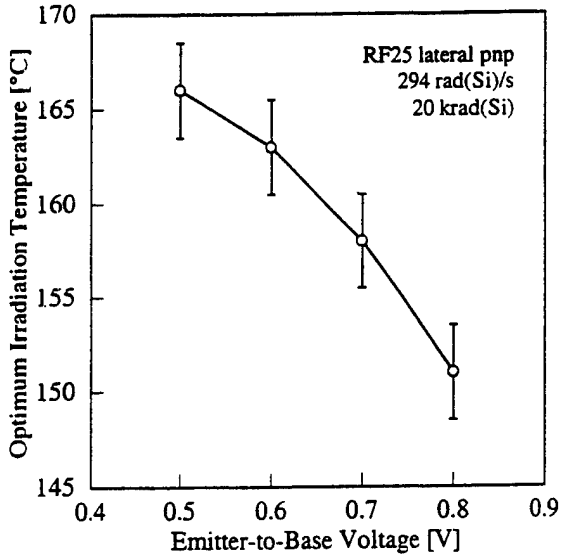

Fig. 6. Effect of emitter-to-base voltage on the optimum temperature for enhanced radiation-induced gain degradation of the RF25 lateral pnp transistor. The optimum irradiation temperature decreases with measurement bias.

As shown in Fig. 6, the irradiation temperature corresponding to maximum degradation decreases from approximately 165°C at 0.5 V to approximately 150°C at 0.8 V. Larger design margins and smaller irradiation temperatures are required for hardness assurance testing at larger total doses[1,2]. The fact that the design margin and optimum irradiation temperature vary with measurement bias potentially complicates the development of a hardness assurance methodology for linear circuits. These trends suggest that design margins required to bound degradation of relevant circuit level parameters may be larger when the transistor is used for low power applications than when biased for optimum performance.

V. CONCLUSION

Enhanced low-dose-rate gain degradation of the ADI RF25 lateral pnp transistor was examined as a function of measurement bias. Degradation enhancement at low dose rates or elevated temperatures is more severe when measured at low emitter-to-base biases than when measured at high emitter-to-base biases. Mechanisms contributing to this bias dependence include interface trap charging, field effects from oxide trapped charge and emitter metallization, base series resistance and high-level carrier injection. As a result, larger design margins or higher irradiation temperatures are required to bound low-dose-rate degradation when the degradation is measured at low power.

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