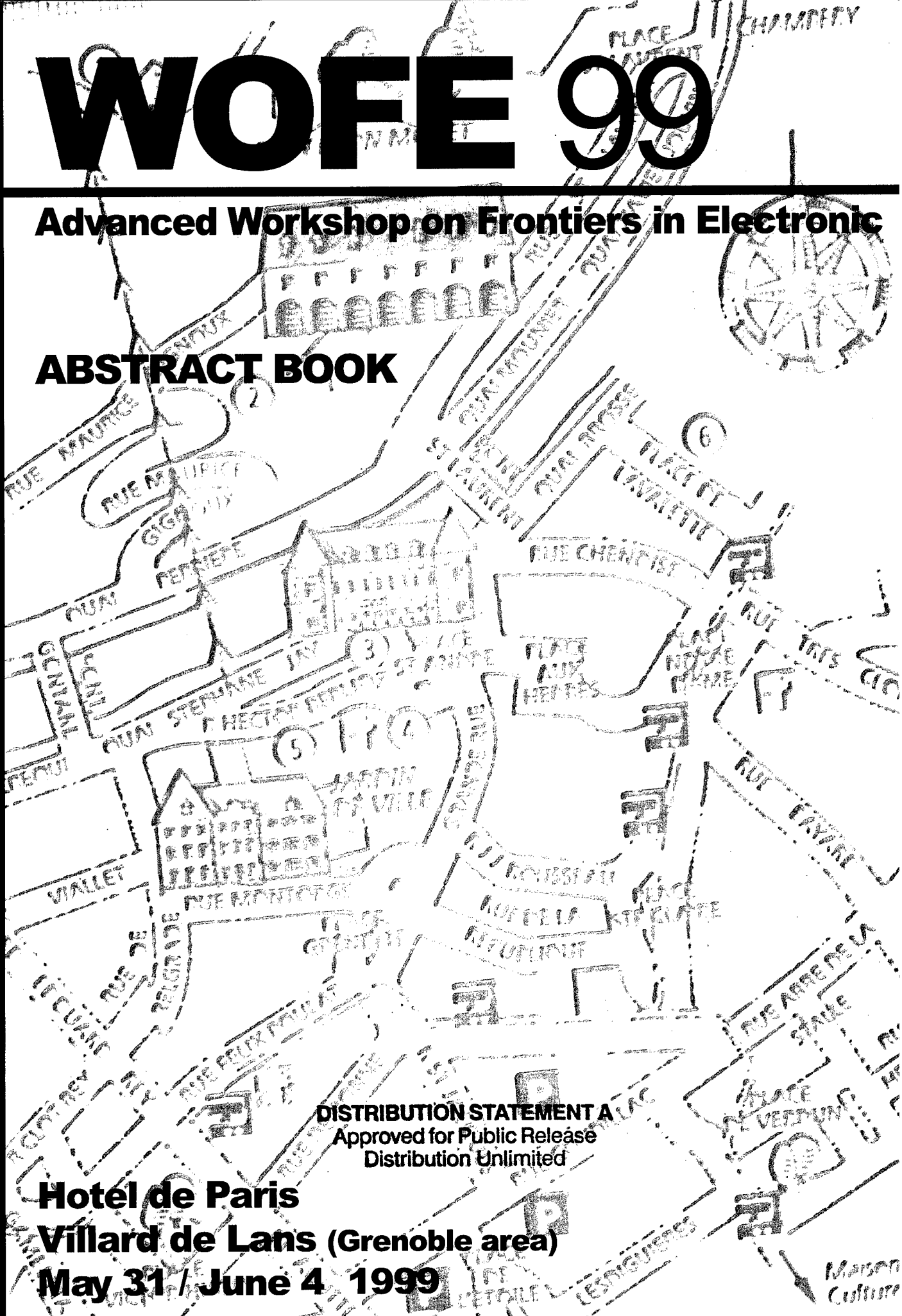
WOFE 99

Advanced Workshop on Frontiers in Electronic

ABSTRACT BOOK



Hotel de Paris
Villard de Lans (Grenoble area)
May 31 / June 4 1999

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	19 June 1999	Conference Proceedings

4. TITLE AND SUBTITLE

International Workshop on New Frontiers in Electronics (WOFE)

5. FUNDING NUMBERS

F61775-99-WF014

6. AUTHOR(S)

Conference Committee

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Lecce, Department of Material Science
Via Arnesano
Lecce 73100
Italy

8. PERFORMING ORGANIZATION REPORT NUMBER

N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

EOARD
PSC 802 BOX 14
FPO 09499-0200

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

CSP 99-5014

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

A

13. ABSTRACT (Maximum 200 words)

The Final Proceedings for International Workshop on New Frontiers in Electronics (WOFE), 31 May 1999 - 4 June 1999

This is an interdisciplinary conference with a major theme emphasizing materials to systems. Material topics include emerging microelectronic materials, physical phenomena and quantum devices, nanoelectronics, silicon-on-insulator (SOI) and MEMs; systems topics include computers, sensors, telecommunications, and consumer electronics. There will also be panels on (1) materials and devices and (2) systems.

14. SUBJECT TERMS

EOARD, Sensor Technology, Electronic Devices, Semiconductors, Semiconductor materials

15. NUMBER OF PAGES

130

16. PRICE CODE

N/A

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

WOFE 99
PROGRAM

Advanced Workshop on Frontiers in Electronics

May 31 / June 4, 1999

Hotel de Paris
Villard de Lans
(Grenoble area)
France

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AIXTRON

PROGRAM

May 30

Registration

May 31

Plenary Session
Organizer: Yoon-Soo Park
Chair: Max Yoder

9:30 - 9:35	Welcome & Introduction, Park
9:35 - 9:45	Opening Remarks, v.Klitzing
9:45 - 10:25	Quantum Nanostructures and Their Potential for Infrared and Terahertz Applications, Sakaki
	Break
10:50 - 11:30	Emerging Trends in Semiconductor and Nanoscience Research, Trew
11:30 - 12:10	Nitride based LED and lasers, Nakamura

ULSI - 1
Organizers: Toshiaki Ikoma, Y. Kado, Simon Sze, Hiroshi Iwai
Chairs: Alex Zaslavsky, Dae Mann Kim

14:00 - 14:30	History of non Von-Neumann and parallel computation algorithms, Muraoka
14:30 - 15:00	Frontiers in electronic noise: from submicron to nanostructures, Reggiani
	Break
15:30 - 16:00	Innovative Integration based on Silicon-Core Technologies for Sensor and Communications Applications, Nagatsuma
16:00 - 16:30	The DRAM Odyssey: from Kilobits to Gigabytes and Beyond, Lee
16:30 - 17:00	Ultimate MOSFETs on SOI: Ultra Thin, Single Gate, Double Gate or Ground Plane, Cristoloveanu

Panel Session: Limitation of ULSI
Organizers: K. Takeya and H. Iwai
Moderators: T. Ikoma and S.M. Sze

17:00 - 18:40	Panelists include: Takeda, Maes, Nishi, TBD
	Discussion

June 1

ULSI - 2
Organizers: T.Ikoma, K.Takeya , S.M. Sze, and H.Iwai
Chairs: Trey Smith, Enrico Sangiorgi

9:00 - 9:30	Limitations of (and off) the SIA Roadmap Trends, Doering
9:30 - 10:00	To fill the gap between Si-ULSI and nanodevices, Hiramoto
	Break
10:30 - 11:00	Current status and future directions for Asian semiconductor industry, Chang
11:00 - 11:30	Layered tunnel barriers for ULSI applications, Likharev
11:30 - 12:00	Vertically integrated SRAM structures, Mastrapasqua

Optoelectronics and Photonics - I
Organizer: Joe Campbell and Dan Dapkus
Chairs: Letitia Paige Harrison and Elias Towe

14:00 - 14:30	Photonic Bandgap Lasers and Nanocavities, Scherer
14:30 - 15:00	Progress in Femtosecond Semiconductor Optoelectronic Devices, Wada

15:00 - 15:30 Quantum Cascade Lasers, Sirtori
Break
16:00 - 16:30 Nano-Optoelectronics in Technology Roadmap, Arakawa
16:30 - 17:00 High Speed Resonant-Cavity InGaAs/InAlAs Avalanche Photodiodes, Campbell
17:00 - 17:30 Vertical Cavity Lasers and Microresonators, Dapkus

Conference Banquet

June 2

SOI and MEMs
Organizer: Sorin Cristoloveanu
Chairs: Enrico Zanoni and Eugenio Moreno

9:00 - 9:30 Why can Smart Cut® change the future of microelectronics?, Auberton-Hervé
9:30 - 10:00 Advanced Sensors and Microsystems on SOI, Mokwa
Break
10:30 - 11:00 Challenges in Mainstreaming SOI Technology, Shahidi
11:00 - 11:30 Optimized Design of Subband Structure in MOS InversionLayer for Realizing High Performance and Low Power Si MOSFET's, Takagi

Emerging Microelectronic Materials
Organizers: Mitra Dutta and Suk-Ki Min
Chairs: Colin Wood and Tor Fjeldly

14:00-14:30 Carbon Nanotubes, Lee
14:30-15:00 Metal Induced Crystalization of Amorphous Silicon, Jang
15:00-15:30 Heterogeneously Integrated Circuits Using Wafer Bonding and Compliant Substrate Technologies, Lo
Break
16:00-16:30 Polarization Issues in GaN and Related Heterostructures in the Context of Devices, Morkoc
16:30-17:00 Ihm, *withdrawn*
17:00-17:30 MOCVD - The Key Technology for Industrial Applications of Quantum Devices, Juergensen

June 3

Panel Session: Materials and Devices "After CMOS"
Moderator: Paul Solomon

Physical Phenomena and Quantum Devices
Organizers: Manijeh Razeghi and Jimmy Xu

Physical Phenomena in Semiconductor Compounds
Chairs: Herb Goronkin and TBA

9:00-9:40 The Role of Scanning Probe Microscopes for Characterization of Physical Phenomena in Quantum Devices, Narayanamurti
9:30-10:00 Quantum Dot Lasers: Theoretical Analysis of Performance, Suris
10:00-10:30 Spin-filter effects in transmission of free spin-polarized electrons through ultra-thin magnetic layers, Lampel
Break
11:00-11:30 Current State of the Theory of the Quantum Hall Effect, Dyakonov
11:30-12:00 Observation of Multiple Excitonic Optical Rabi Oscillations in a Semiconductor, Peyghambarian

Quantum Devices and Materials
Chairs: Fritz Schuermeyer and Arnoldo Majerfeld

14:00-14:30	High Power 3-12 um Semiconductor Lasers: Roadmap for the 21st Century, Razeghi
14:30-15:00	Coherent Coupling in Multiwavelength Modelocked Semiconductor Diode Lasers - Physics and Applications, Delfyett
15:00-15:30	Heterostructure Devices in Infrared Detector Technology, Rogalski
	Break
16:00-16:30	Materials for the Next Generation of Long Wavelength Infrared Detectors, Brown
16:30-17:00	MOCVD Growth of High-Quality Gallium Nitride Based Electronic and Photonic Devices, DenBaars
17:00-17:30	Fundamental Limits of Performance of AlGaN/GaN HEMT's, Eastman

Poster Session
Chairs: Usha Varshney and Edgar Martinez

Effect of Electron Electron-Cloud Interaction on Schottky Metal Barrier Height to Two Dimensional Electron Gas, Anwar

Optical absorption modulation in heterodimensional devices, Castro

Optimal Control Theory for Optical Waveguide Design: Application to Y-branch Structures, Coalson

Carrier screening and polarization fields in nitride-based heterostructure devices, Della Sala

CAD Tools and Optical Device Models for Mixed Electronic/Photonic VLSI, Deng

Generalized Monte Carlo simulations for quantum transport in nanostructured semiconductor devices, Di Carlo

Why is 2D high-field electron drift velocity smaller than for 3D electrons?, Dmitriev

100-GHz Superconductor Processors for a Petaflops Computer: Design Phase 2, Dorojevets

Quantum 1/f stability optimization of quarz resonators, THz generators and other resonant systems, Handel

Quantum 1/f optimization of antennas, Handel

Epitaxial GaN Films Grown on ZnO/GaN-Buffered Si Substrates, Kim, HK

Stress-Induced Confinement of Light in GaN, GaAs and Si, Kim, HK

Ferroelectric Nonvolatile Memory Field-Effect-Transistors Based on a Novel Buffer Layer Structure, Kim, HK

A Stenographic Character Recognition Algorithm in Neural Networks, Kim, SK

Robust Recognition of the II-Pa Stenographic Character Images by Using Neural Networks, Kim, SK

Migrating to submicron display technology: Schottky source/srain thin film transistor, Lam

Reduction of Coupling Noise in Data-Line Arrays, Langer

Scalability of SOI into future deep submicron CMOS technology, Leobandung

Long Wavelength (1.3 μm) QD VCSELs on GaAs Substrates, Lott

MOVPE Growth, Piezoelectric and Optical Properties of Strained <111>-Oriented InGaAs/AlGaAs MQWs and their Possible Application to Optoelectronic Devices, Majerfeld
Wide-Angle, Low-Loss Y-Branch Waveguide for Integrated Optics, Min

Novel AlGaN-based UV photodetectors bridge biology and electronics, Munoz

Monte Carlo Simulation of Impact Ionization and Light Emission in Pseudomorphic HEMT's, Rossi

SPM Assisted Nanofabrication for Nanoelectronics, Safarov

Automated Internet Measurement Laboratory AIM-Lab, Shen

Obtaining High Purity 6H-SiC Single Crystals by Annealing, Shin

Two Dimensional Hole Gas Induced by Piezoelectric and Pyroelectric Charges, Shur

An Advanced Approach to Extracting Small Signal Model Parameters of MOSFETs from Measured S-Parameters, Tian

Applying Selective Liquid-Phase Deposition to the Fabrication of FETs with Excellent Characteristics, Yeh

Factors limiting the maximum operating voltage of microwave devices, Zanoni

VLSI-Compatible Multiemitter Heterojunction Bipolar Transistors with Enhanced Logic Functionality, Zaslavsky

June 4

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Organizer: Konstantin Likharev
Chair: Tetsuhiko Ikegami

9:00 - 9:30	SCALPEL: The cutting tool for sub-0.1 um lithography, Gibson
9:30 - 10:00	Prospects of quantum devices based on III-V compound semiconductors, Hasegawa
10:00 - 10:30	Room-temperature single-electron devices by scanning probe process, Matsumoto
10:30 -11:00	Straddle-gate transistor: Transistors in the limit of useful field-effect, Tiwari
	Break

Optoelectronics and Photonics - II
Organizer: Joe Campbell and Dan Dapkus
Chair: Paul Tasker

11:30 - 12:00	Towards Quantum Structure Based Terahertz Source, Andronov
12:00 - 12:30	High frequency circuits based on GaAs-PHEMT technology for modern sensor and communication systems, Schlechtweg
12:30 - 13:00	Distributed Balanced Photodetectors for RF Photonic Applications, Wu

Conference Closing Remarks: Yoon-Soo Park

WOFE 99
ABSTRACT

PREFACE

WOFE-99 will be held in Villard de Lans (Grenoble area - France). The workshop is a sequel to WOFE-97 held January 1997 in Puerto de La Cruz, Tenerife, Spain.

The aim of the workshop is to bring together leading scientists and engineers who work at the frontiers of electronic devices and circuits, yet emerging from traditionally separated fields with different professional background. Rapid pace of electronic technology evolution compels a merger of such technical areas as low-power digital electronics, microwave power circuits, optoelectronics, etc., which collectively have become the foundation of today's electronic technology. The Workshop aims at encouraging active cross-fertilisation of the different "species" in this electronic planet.

The WOFE will gather experts from academia, industry, and government agencies to review the recent exciting breakthroughs and their underlying physical mechanisms.

The program committee invites discussions of controversial issues, provocative views, and visionary outlooks. Debates on the future trends and directions and the market pulls as well as the necessary policy and infrastructure changes are encouraged. Attempts will be made by the committee to solicit alternative views and rebuttals.

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PLENARY SESSION

Recent Advances and Future Trends in Modern Electronics

Yoon-Soo Park

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Development of electricity and electronics has greatly influenced the everyday human life. It made human life much more comfortable by providing the ability of easy transfer and control of the power. In addition, electronics has greatly improved our capability in many areas such as computation, communication, and information technology. These days, we are always surrounded by various electronic devices that have critical influences on our life. The electronic and optoelectronic devices have been developed at an enormous rate in recent few decades since the first invention of transistor in 1947 and semiconductor laser in 1962. The development of these devices has been continuously accelerated by various needs in our life. This trend didn't show any saturation until the last decade and we expect to see more rapid development in the 21st century. In this article, most recent development in electronics and optoelectronics in the last decade will be briefly reviewed.

First trend in modern electronics is the modern silicon-based ultra large scale integrated circuit (ULSI) technology that has given rise to dramatic progress in computers and telecommunications, bringing them much closer to cost-effective consumer electronics. It is essential to develop low-cost and low-energy-consumption components and systems by taking full advantage of today's established leading-edge semiconductor technologies, which provide both economic and ecological benefits. This effort has led to the development of various Si-based devices and integrated circuits such as MOSFET on silicon on insulator (SOI) with various gate structures, gigabytes DRAMs, and vertically integrated SRAM structures.

Among them, SOI is very important technology developed in the last decade to improve the performance of Si microelectronic devices. In conventional bulk CMOS technology below 0.1 µm, conventional ways to increase the drain current, reduction in the channel length and/or the gate oxide thickness would be limited more and more, because of the short channel effect, the difficulty in the lithography and direct tunneling current in ultra-thin gate oxide. In addition, the severe influence of inversion-layer capacitance on low voltage operation of scaled MOSFETs requires the reduction in carrier concentration in the channel and the increase in carrier velocity, in order to reduce the power consumption. To overcome these problems, the two promising device structures, SOI MOSFETs with SOI thickness thinner than the inversion layer of bulk MOSFETs and strained-Si MOSFETs, have been researched. Especially, the feasibility of SOI CMOS technology is high considering the recent advances. The researchers have developed various SOI fabrication technologies such as direct bonding of Si on quartz/glass and oxygen implantation to Si substrates to form a SiOx insulating layer. Researchers claim that the first microprocessor using SOI technology will be shipped in 1999. The main attraction of SOI technology is its performance advantage of 20-35% over bulk CMOS of the same generation. SOI also offers key advantage in power consumption. The increased performance and decreased power consumption of SOI CMOS technology is a very attractive feature.

Another trend in electronic devices is their decreased size and fast speed. The new quantum nanostructure and terahertz devices have been developed with the help of various growth, processing and characterization techniques such as metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), e-beam lithography, x-ray lithography, transmission electron microscope (TEM), scanning tunneling microscope (STM), and atomic force microscope (AFM). The primary barriers to continued scaling of CMOS technology are currently seen as resulting from limitations in lithography, gate dielectrics, and interconnects. In optical lithography, moving to the shorter wavelengths (193 to 130 nm) will be possible. However beyond this, another solution (perhaps AFM-based or e-beam lithography) will need to be developed as we approach 10-nm feature sizes. At the same time, the researchers are investigating on new high-K gate dielectric materials which may enable tunneling to be overcome in high-performance, very short-channel MOSFETs. Another possible way of manufacturing nanoelectronics is by using "DNA and enzymes" (or whatever the appropriate "biotechnology" might be) to perform the processing in a "beaker" rather than in the many separate multi-million dollar tools that we use for discrete process steps today. Although we are presently a long way from such a vision, initial collaborative efforts now underway are likely to germinate new objects which fundamentally influence future nano/bio/electronics technology.

The nanoscale devices utilize the quantum effect of electronic states and can achieve operational characteristics orders of magnitude beyond the capability of current devices. Quantum devices have great

advantages over the classical devices such as high integration density, extremely low power consumption, and very high speed. Major issues related with the quantum functional devices are the techniques to obtain the quantum structures. Two dimensional quantum wells, one dimensional quantum wires, and zero dimensional quantum dots are the quantum structures currently being investigated. The first example of these devices is a single electron transistor in which one bit of information can be carried by a single electron. This device is based on the Coulomb blockade and quantum size effect and the electronic switch using this transistor has also been demonstrated. Other novel devices based on the quantum structures include resonant tunneling double barrier diode and resonant hot electron transistor (Single device operation up to 120 GHz demonstrated). From 1994, semiconductor detectors (1~20 µm) and lasers (0.7~1.3 µm) fabricated from quantum wires and quantum dots have been reported. They were fabricated either by self-organized growth or lithography. Using these quantum devices, the concept of few electron quantum computing structures has also been developed. The development of quantum devices will make the future electronic devices closer to the level of human brain.

Still these nanodevices are not necessarily practical and it is necessary to fill the gap between the present ULSI and the nanodevices. At this stage, the nanodevice is just a subject of the research. The quantum and single electron effects are troublesome in practical ULSI because they degrade the device performance and often increase fluctuations of device characteristics. As a step to overcome this problem, researchers have been trying to utilize the quantum and single electron effects positively in ULSI to improve the performance. The final step will be the realization of silicon nanodevices that fully utilized the quantum and single electron effects.

There have also been outstanding developments in the optoelectronics and photonics area in last decade. One of the major inventions is the development of nitride based LEDs and lasers. Using InGaN quantum-well (QW) structures on sapphire substrates, Japanese researchers were able to obtain the LEDs emitting ultraviolet (UV), blue, green, amber and red light. More recently, they obtained high quality GaN films on sapphire substrate using lateral epitaxial overgrowth (LEO) techniques. The recent device structures were grown on top of this thick LEO GaN films. A violet InGaN multi-quantum-well (MQW)/GaN/AlGaN separate-confinement-heterostructure laser diode (LD) grown on the LEO GaN on sapphire showed low threshold current density, high output power, and estimated lifetime of ~3,000 ours.

Other than the success of nitrides, the optoelectronics and photonics business has been grown at a considerable rate. One of the most important photonics business is the optical telecommunications. The rapid development of erbium-doped fiber amplifiers has changed the concept of fiber telecommunications significantly. Soon we will discuss long-distance signal transmission systems that can cover thousands of kilometers without using regenerative repeater stations. Erbium-doped fiber amplifiers, when used in conjunction with soliton pulses, can bridge oceans in high-bit-rate transmissions. Interconnections within integrated circuits may also adopt the optical route soon. In fact, the major impact of photonic technology in this information age of the 1990s may be increased optical means of information processing and data transmission. The trend will soon spill over into both the home and business. Local area networks (LANs) have exploited the use of synchronous optical networks (SONETs) to take advantage of the high speed and broad bandwidth of optical signaling services. More and more devices will be designed using photons as signal carriers. This is only the beginning. New developments arise daily including high speed optoelectronic devices. Ultrafast optoelectronic devices will be a key to the development of telecommunication systems exhibiting a throughput beyond 1 Tb/s. Semiconductors-based optoelectronic devices are aiming for the operation in the sub-picosecond and femtosecond time domain. These ultrafast devices will greatly increase the capacity of current telecommunication systems.

Other major developments in optoelectronics in the last decades include quantum cascade lasers, nanocavity lasers, quantum well infrared photodetectors, mid to long wavelength infrared lasers, and uncooled photodetectors. Even though their commercial market is not big at the moment, their potential application is huge in the future.

Although most developments in the last decades relied on the conventional material systems, the researchers have been continuously pursuing the new material systems. Carbon nanotubes are one of the new systems that showed the feasible applications for flat panel display, memory devices, and electrodes. GaN is one of the good example that revolutionized the world of blue and UV business in 1990s. For the integration of optical, mechanical, chemical, biological, and electrical signal processing on the same chip, the technology of integrating various semiconductors with Si becomes the corner stone for the new generation ICs. To overcome the problems of current conventional flip-chip bonding technologies, people have been actively seeking new material integration technologies that are more versatile and scalable than the current technologies including wafer bonding and compliant substrates.

As the electronic devices are trying to achieve the lower dimension, less power consumption, and high speed, the physics governing these advanced devices should be studied. As we approach the nanometer scale, the electronic levels are quantized and quantum effects are always coming into play. So quantum physics should be applied to the understanding of the device behavior. In these novel devices, the classical theory describing the conventional electronic devices might fail to explain the behaviors. In the last decades, physicists have developed various tools to better explain the device behaviors. They were used in evaluating the performance of novel devices such as quantum cascade lasers, type-II superlattice lasers, and quantum dot lasers. These developed physics has also been used to develop the concepts for the new devices.

Through this article, we have discussed the recent advances in various fields of modern electronic and optoelectronic devices. The major direction in electronics in the 1990s can be characterized by the nanoscale, giga to terahertz operation, and very low power consumption. And these developments required the utilization of advanced physics, device processing and characterization technologies. Various new novel material systems have also been researched. These approaches have greatly improved the performance of the electronic devices and it is being continued. These electronic devices will further improve the level of human life as they did before.

Quantum Nanostructures and Their Potential for Infrared and Terahertz Applications

Sakaki

The Abstract is not available.

Emerging Trends in Semiconductor and Nanoscience Research

R.J. Trew

Director of Research
ODUSD(S&T)
U.S. Department of Defense
Arlington, VA

The Department of Defense invests about $1.1B annually into basic research, with the majority of these funds supporting research performed at academic institutions. The basic research program is implemented through the Services' core programs and the University Research Initiative (URI), which is managed by the Research Office in the Office of the Deputy Under Secretary of Defense for Science and Technology. The URI includes a variety of programs such as the Multi-Disciplinary University Research Initiative (MURI), the Defense University Research Instrumentation Program (DURIP), the Presidential Early Career Awards in Science and Engineering (PECASE), and several other programs. These programs are executed through the Services? research offices, with management oversight by the DUSD(S&T) Research Office. The basic research program provides support for long term research in areas of interest for future military systems as described in the Basic Research Plan (BRP) published by Office of the Secretary of Defense.

In this presentation the structure and management of the DoD basic research program will be described. DoD support for academic research will be placed in a historical perspective and factors influencing funding and program development will be presented. Emerging topic areas of interest in semiconductor materials and devices research will be discussed. There is a shift in emphasis in DoD support for long range materials and electronics research and support programs are becoming increasingly focused upon nanoscience and nanotechnology topics. Advances in understanding fundamental physics and engineering on the nanoscale are viewed as critical to development of next generation devices and systems. Progress in nanotechnology is enabled by remarkable success in semiconductor materials growth technology, nanoscale patterning resolution, and device fabrication technology. It is now possible to fabricate, literally atom-by-atom, semiconductor materials that do not exist in nature and with properties that are near ideal for application in electronic and optical applications. These materials are being used to fabricate devices that may have operational characteristics orders of magnitude beyond the capability of current devices. This research is expected to provide the basis for next generation systems. DoD interests and related program support for work in these areas will be discussed.

Nitride-Based LEDs and Lasers

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Highly efficient light-emitting diodes (LEDs) emitting ultraviolet (UV), blue, green, amber and red light have been obtained through the use of InGaN quantum-well (QW) active layers instead of GaN QW active layers [1]. Red LEDs with an emission wavelength of 675 nm, whose emission energy was almost equal to the band-gap energy of InN, were fabricated. The dependence of the emission wavelength of the red LED on the current (blueshift) is dominated by both the band-filling effect of the localized energy states and the screening effect of the piezoelectric field. In the red LEDs, a phase separation of the InGaN layer was clearly observed in the emission spectra, in which blue and red emission peaks appeared. In terms of the temperature dependence of the LEDs, InGaN LEDs are superior to the conventional red and amber LEDs due to a large band offset between the active and cladding layers. The localized energy states caused by In composition fluctuation in the InGaN active layer contribute to the high efficiency of the InGaN-based emitting devices, in spite of the large number of threading dislocations and a large effect of the piezoelectric field [2].
A 4-µm-thick GaN layer was grown on a (0001) C-face sapphire substrate with an off-angle of 0.2 degrees toward <1-100. The off-angle sapphire substrate was used to obtain a step growth surface of GaN. After the growth, the silicon dioxide (SiO2) mask was patterned to form 3-µm-wide stripe windows with a periodicity of 10 µm in the GaN <1-100 direction. Next, a 4-µm-thick GaN layer of the window region was etched out by dry etching until the sapphire substrate appeared. After removing the SiO2 mask, the GaN growth was performed again on these rectangular GaN films. In this growth process, the growth rate of the GaN initiated from the etched surface of both sides was much faster than that from the top surface of each rectangular GaN film. Thus, following 20-µm-thick GaN growth, the coalescence of the GaN from both sides of the rectangular GaN made it possible to achieve a flat GaN surface over the entire substrate. There was no GaN growth directly from the etched surface of the sapphire substrate. The defect density of the epitaxially laterally overgrown region, as determined by plan-view transmission electron microscopy (TEM), on the etched region of the underlayer GaN with a width of 7 µm, was lower than 1x106 cm-2. The defect density on the un-etched region was on the order of 1x1010 cm-2. This coalesced GaN is referred to as epitaxially laterally overgrown GaN (ELOG). A violet InGaN multi-quantum-well (MQW)/GaN/AlGaN separate-confinement-heterostructure laser diode (LD) was grown on the ELOG on sapphire [3]. The threshold current density was 2-4 kAcm-2. The LDs with cleaved mirror facets showed an output power as high as 30 mW under room-temperature continuous-wave (CW) operation. The stable fundamental transverse mode in the near-field patterns was observed at an output power up to 30 mW. The lifetime of the LDs at a constant output power of 5 mW was more than 1,000 hours under CW operation at an ambient temperature of 50?C. The estimated lifetime was approximately 3,000 hours under these high-power and high-temperature operating conditions.

References

[1] S. Nakamura and G. Fasol: The Blue Laser Diode, 1st ed. (Springer-Verlag, Heidelberg, 1997).
[2] S. Nakamura: Science 281 (1998) 956.
[3] S. Nakamura, M. Senoh, S. Nagahama, T. Matsushita, H. Kiyoku, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sano, and T. Mukai: Jpn. J. Appl. Phys. (in press).

ULSI-1

History of non Von-Neumann and parallel computation algorithms

Yoichi Muraoka

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In this talk, I would like to review the history briefly, and put more emphasis on the future.
The modern history of parallel computation started from Illiac-IV. But we had to wait until very recently to see fully successful systems. Among many important reasons for this to happen, we cannot ignore the advancement of microprocessor technologies.
We will present the status of the current art, and discuss the technical issues to be solved from the computer architecture's standpoint, including the latency hiding problem.
Then we will discussour vision of the future. Among many possibilities, we would like to introduce a Petaflop computer project to build a future high-end system.

Frontiers in electronic noise: from submicron to nano structures

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Noise is a key feature of any electronic device because it gives the intrinsic limit of the performance through the signal-to-noise ratio figure of merit. However, besides hindering the signal detection, noise is also a relevant probe of the microscopic phenomena at hand thus providing information not otherwise available from the study of average quantities, like conductance. When moving toward nanostructures new phenomena have been found to arise and innovative concepts should be introduced.

As a result of an international scientific collaboration carried out in recent years among several European groups, below we summarize what we consider to be the main issues to be addressed and which in our opinion deserve to be presented and discussed at this workshop.

Shot noise and its deviation from the Poissonian statistics of independent current pulses, the so-called suppressed and enhanced shot-noise regimes.

Shot noise as detector of the quantum of charge responsible of transport (integer and fractional).

Generalization of the impedance field method to include non- local effects in the analysis of current and voltage spectral densities of non-homogeneous structures in the deep sub-micron range.

Noise spectra: what can we expect from its analysis.

Which theoretical formalism is better appropriate to study noise.

Most of the above items are at present still controversial issues, once for all the supposed universality of the 1/3 shot-noise suppression factor in disordered conductors.

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Innovative Integration based on Silicon-Core Technologies for Sensor and Communications Applications

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Silicon-based ULSI technology has given rise to dramatic progress in computers and telecommunications, bringing them much closer to cost-effective consumer electronics. As we approach the 21st century, it is essential to develop low-cost and low-energy-consumption components and systems by taking full advantage of today's established leading-edge semiconductor technologies, which provide both economic and ecological benefits. This paper presents an innovative system integration scheme wherein heterogeneous materials and devices, including photonic devices as well as electronics, are organically integrated on a silicon-core circuitry to achieve better performance, higher functionality and lower cost. First, state-of-the-art silicon-based technologies (such as low-power CMOS digital/analog circuits [1], micro-machined switches and high-performance optical/electrical interconnects) are reviewed. Then, after a discussion of the main issues in heterogeneous integration schemes, the application of this new approach to an integrated fingerprint sensor/identifier [2], and a photonic receiver/transmitter for future millimeter-wave measurement and communication systems [3] is described.

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The DRAM Odyssey: from Kilobits to Gigabytes and beyond

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Since the invention of 1K DRAM in 1970, the DRAM industry has grown rapidly to become a $16 billion global industry in 1998. During the last decade, the total DRAM bits produced world-wide have increased a steady 55% to 70% per year, even in times of severe business difficulties, and the price of a DRAM bit has been reduced to 1/100 of what it was 10 years ago. The factors that have enabled such phenomenal developments are: technological advancements and breakthroughs that resulted in improved circuit performance and reduction in manufacturing costs, the popularity of new PC operating systems and many software applications that require larger memory than their predecessors, strong growth of PC industry, and the competition in this commodity business by many companies which accelerated the pace of new technology developments.

As the society becomes more and more information and knowledge based, the capability to produce, modify, transfer, store and retrieve large amount of information is highly crucial in all aspects of the society. DRAM is currently a major technology for the systems contributing to such needs. Due to the explosive growth of Internet based activities, PC or PC-like information appliances will become ubiquitous, and the growth of DRAM industry, however cyclical, will very likely be continued for many years to come.

From technological aspects, the silicon VLSI technology has evolved steadily, a trend forecasted and updated in the SIA technology roadmap. The adoption of new technology and shrink technology would be unavoidable if justified by the economics. The challenges we face in the development of shrink technology are by no means trivial: however, the advancements suggested in the SIA technology roadmap for the next decade will most likely be realized. Therefore, we expect to see production of 16 Gigabit DRAM chips using sub-0.1um technology before the year 2010. New process technologies on the horizon will be discussed in this paper.

The business question is: what applications will justify the costly development and production of such large DRAMs in big volume that may require multi-billion dollar facilities. Based on our familiarity of PC's with 64Mega Bytes of main memory today, it is hard to envision why we would need two or more Giga Bytes of main memory--provided by a single 16 Gigabit chip--for an average PC. On the other hand, we remember the PC of 15 years ago, when 256 kilobytes of main memory--1/256 of today's PC-- was regarded adequate! We should never underestimate the strong appetite for ever larger memory capacity in new computer applications.

On the other hand, it is also quite possible to see many new inventions of some popular digital boxes that need smaller DRAM capacity than can be provided by multi-gigabit technology. Further the high-bandwidth performance advantage of putting DRAM and logic on one chip may generate more demand of Embedded DRAM technology in the future. The technology and cost issues which prohibit today's Embedded DRAM business from growing more rapidly will have to be solved in the next decade.

Looking back the past of global DRAM industry, we see many exciting turns of events in both technological as well as business aspects. Armed with all the wisdom from history, however, predicting the future of DRAM industry is still illusive. So comes the title of this presentation: the DRAM Odyssey, to be continued into the next decade.

Ultimate MOSFETs on SOI: Ultra Thin, Single Gate, Double Gate or Ground Plane

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The Silicon On Insulator (SOI) technology has become rather mature and attracts industrial interest for many applications, including low-power/low-voltage, high frequency, and high temperature circuits. In addition, SOI MOSFETs show enhanced tolerance to short-channel effects, being capable of extending the frontiers of the silicon-based transistors. However, several
problems, such as the series resistance, film thickness control, fringing fields, etc have still to be solved. In this work, we consider and compare various innovative architectures for sub-0.1µm fully-depleted SOI MOSFETs.

Conventional single-gate SOI MOSFET. The scalability of this device is discussed as a function of doping and thickness fluctuations. We analyze the effect of the buried oxide thickness and various gate materials as well as the role of elevated source and drain.

Extremely thin SOI MOSFET. Although the normal device thickness is considered to be in the range 20-50 nm, the current technology is already capable of producing much thinner transistors 1-5 nm thick. We investigate the thickness-related effects on carrier mobility, threshold voltage, subthreshold swing, and interface defects. The advantage of the special carrier confinement is discussed based on the coupling of Poisson and Schrodinger equations. Preliminary experiments in 1-nm thick transistors show that the ID(VG) characteristics are still MOS-like and well behaved.

Double-gate SOI MOSFET. These transistors have either two gates biased simultaneously or one surrounded gate. They take advantage of the concept of volume inversion which offers additional current, enhanced transconductance , and attenuated short-channel effects. The practical manufacturability of this structure is also examined.

Ground-plane SOI MOSFET. A compromise between single-gate and double-gate MOSFETs is the use of a ground-plane, located underneath a thin buried oxide or within a thick buried oxide. Numerical simulations indicate that the drain-induced barrier lowering (DIBL) is drastically reduced in short-channels due to the attenuation of the fringing fields within and underneath the buried oxide.

Dynamic-threshold SOI MOSFET. This device has the transistor body internally connected to the gate or to the drain. A nearly ideal coupling develops between the gate voltage and the channel for the benefit of fast, low-voltage integrated circuits. The performance and limitations of DT-MOSFETs are critically explored.

The discussion of the above structures is based on simulation results, physics-based models, and exhaustive experimental data obtained on preliminary devices.

ULSI - 2

Limitations of (and off) the SIA Roadmap Trends

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Since 1992, the SIA has sponsored a process for building consensus on the principal R&D needs of the silicon microelectronics industry out to a 15-year horizon. The outcome of this process is a "Technology Roadmap for Semiconductors," which has most recently been updated through the 1998 revision. Currently, work on the 1999 edition is in progress, and it will be the first version with full international participation (from the U.S., Europe, Japan, Korea, and Taiwan).

The basic premise of the Roadmap is that continued scaling of microelectronics will further reduce the cost per function (historically, ~25%/year) and promote market growth for integrated circuits (averaging ~15%/year). Thus, the Roadmap is put together in the spirit of a challenge -- essentially: "What technical capabilities need to be developed for us to stay on Moore's Law?" During the 1980s and '90s, this challenge has become so formidable that more and more of the development effort has been shared in a precompetitive environment including consortia and collaboration with suppliers. In this process, the Roadmap serves as a guide to the principal technology needs. It does this in two ways: (1) showing the relatively near-term "targets" that need to be met by "technology solutions" currently under development, and (2) indicating where there are no "known (reasonable confidence) solutions" to continued scaling in some aspect of the semiconductor technology. This lattersituation is highlighted as "red" on the Roadmap. The "red" is officially "on" the Roadmap to clearly warn where scaling might end if some real breakthroughs aren't achieved in the future. Such breakthroughs would result in the "red" turning to "yellow" and, ultimately, "black" in future editions. Thus, a very conservative interpretation of the utility of the Roadmap would view parameters in the "red" as effectively "beyond" or "off" the Roadmap.

The primary barriers to continued scaling of CMOS technology are currently seen as resulting from limitations in lithography, gate dielectrics, and interconnects. In each case, there are precompetitive R&D programs responding to the associated "red" on the Roadmap. In optical lithography, moving to the next shorter wavelength (193 nm) is beginning to allow the IC industry to continue Moore's Law for another few years, through scaling down to at least the 130-nm "technology node." International SEMATECH has already begun a program in support of 157-nm lithography as a possible bridge to either EUV or SCALPEL as the "Next Generation Lithography," beyond which another solution (perhaps AFM-based lithography) will need to be developed as we approach 10-nm feature sizes. At the same time, the SRC and SEMATECH are jointly supporting university research on new high-K gate dielectric materials which may enable tunneling to be overcome in high-performance, very short-channel MOSFETs. For the next few years, the interconnect RC time constants with copper metallization and "low-K" inter-metal dielectrics will help keep pace with the decreasing gate delays of the transistors. However, as we continue to scale-down the feature size, the SIA and its partner sponsors are looking to the MARCO Focus Centers in Interconnect and Circuit Design for new paradigms in providing higher performance (i.e., circuit speed) and lower power.

Even before we move beyond the horizon of the current Roadmap into "nanoelectronics," the most significant challenge may be in reducing the growth of capital cost associated with manufacturing integrated circuits, which many people feel will be more limiting than any purely technical barrier to continued device scaling and/or perpetuation of Moore's Law. A new manufacturing approach could represent "partial change," such as resulting from the aforementioned AFM-based lithography; or, it could be "sweeping," such as the final conjecture in an article written in 1997 on the "Future of Microelectronics" [1]. The last part of this article speculates on a far-future vision of eventually manufacturing nanoelectronics very cheaply using "DNA and enzymes" (or whatever the appropriate "biotechnology" might be) to perform the processing in a "beaker" rather than in the many separate multi-million dollar tools that we use for discrete process steps today. Although we are presently a long way from such a vision, initial collaborative efforts now underway are likely to germinate new p rojects which fundamentally influence future nano/bio/electronics technology.

From the general perspective of what is today "the IC industry," the goal of any "integrated nanotechnology R&D strategy" should be to work toward low-cost, flexible manufacturing of the widest possible range of useful "atomically perfect" nanostructures. Of course, there are many intermediate steps/areas that one might envision. For example, a few suggestions for fairly broad-area interdisci-

plinary research are:
(1) Should commercial-scale nanofabrication be based on "wet" or "dry" processing?
(2) How should nanofabrication be "controlled"? For example,
(a) Is it feasible to "program" DNA (or another type of molecular template) to control nanofabrication?
(b) Should nanostructures be manufactured by "self-replication"? or
(c) Is some other form of "self-assembly" practical?
(3) Investigate the applicability of biochemical mechanisms to the fabrication of inorganic structures (e.g., metal lines on Si/SiO2 substrates), especially those normally made with relatively high-temperature processes. Can some form of "catalysis" substitute for the high energy?
(4) Investigate "growth, placement, and connection/integration" of nanotubes with controlled properties (e.g., helicity, electrical conductivity) made from carbon, boron nitride, and other materials. Note that nanotubes could eventually become the "key link" between semiconductor technology and biotechnology.
Hopefully, the R&D synergy between nanoelectronics and biochemistry as elements of "nanotechnology" will continue to grow for many years and ultimately lead to very fundamental and exciting changes in society.

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To fill the gap between Si-ULSI and nanodevices

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Recently, silicon-related nanodevices have attracted considerable attention for future low power and functional ULSI devices. The nanodevice is defined in this study as a device that utilizes new physical phenomena in nanostructures such as quantum effects and single electron charging effects. However, these nanodevices are not necessarily practical and it seems that the more the research of nanodevices advances, the more the gap between the present ULSI and nanodevices is widened.

There would be three phases in the development of silicon nanodevices. In the initial phase where we are now, the nanodevice is just a subject of the research. Quantum devices are single electron transistors are fabricated and evaluated. On the other hand, the quantum and single electron effects are troublesome in practical ULSI because they degrade the device performance and often increase fluctuations of device characteristics. These effects should be studied to avoid the unfavorable influences. In this phase, however, the gap between the ULSI and nanodevices would not be filled.

In order to fill the gap, we have to enter the second phase where the quantum and single electron effects are positively utilized in ULSI to improve the performance and break the scaling limit. Although the present ULSI has lots of serious problems, new physical phenomena in nanostructures have a potential of solving a part of them. The favorable influences include small size and high endurance of single electron memory cells [1], the mobility enhancement by the subband control, suppression of device fluctuations by single electron charging effects, and the fine tuning of ULSI device parameters using memory effects. We have already proposed the control and tuning of silicon nanodevices using a memory effect by silicon floating nano-crystals [2], which will be also applicable to ULSI devices.

The final phase is the realization of silicon nanodevices that fully utilized the quantum and single electron effects. This would be the final target of the research of silicon nanodevices. However, the most critical and important phase is the second one, in which the ULSI devices and nanodevices are merged. When we reach the second phase, the paradigm of the way of scaling ULSI devices will be changed, and that would be the final goal of the research of ULSI devices.

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Present status and Future Trend of Asian Semiconductor Industry

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The present status and future trend toward the year 2010 of Asian Semiconductor industry is still in rapid growth. The major players are Japan, Korea, Taiwan, China and Singapore. Among them, Taiwan is the fastest-growing country. Taiwan has a strong demand for I. C. because of her NO.1 in P. C. manufacturing capability. Japan is still the leader and the major technology driver. Korea will still keep No. 1 in DRAM manufacturing. Taiwan is No. 1 in foundry service. The enterprise infrastructure is vertically disintegrated but corporative, which is dynamic, flexible and quick responsive.
China has a hung market of 3C. No.1 in TV production. Singapore is an excellent bridge between Europe, US. and Asian. Hong Kong has a promising future of software and EDA development business. The rest of Asia has a tremendous opportunity of software development and export processing.
The strategies for entrepreneurship and R & D development in the coming decades will be addressed. Getting away from 1998?s south East Asia economic crisis, the whole Asia will have a bright future in Semiconductor industries and entrepreneurships.

Layered Tunnel Barriers for ULSI Applications

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I will discuss the recent suggestion [1] to use layered tunnel barriers for a radical speed-up of read/erase processes in floating-gate devices. Preliminary calculations indicate that these barriers may be used for the implementation of nonvolatile random-access memories with integration scale up to 16Tb, even denser hybrid SET/FET memories [2], and electrostatic data storage systems with recording density up to 1 Tb/in2. As a by-product, resonant Fowler-Nordheim electron emission from layered barrier cathodes may open a way to chip cooling all the way down to 10 Kelvin, which would allow to integrate ultrafast RSFQ logic circuits into digital systems, without liquid coolants or moving parts.

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Vertically Integrated Structures for high density SRAM

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Static random access memory (SRAM) cells are commonly used as embedded memory because they are fast, dissipate low power, and are easy to use since they do not require the overhead circuitry of DRAM or flash EPROM. The main disadvantage of SRAM is the large cell size (six transistors per cell compared to only one transistor and one capacitor for DRAM). One viable approach to decrease the SRAM cell size is vertical integration, as is the case of polysilicon load resistors and thin film p-MOSFET loads fabricated on top of the bulk n-MOSFETs.

In this talk we will present a novel approach to the vertical integration of SRAM, which combines the self-aligned nature of the MOSFET process with a relative small number of process steps.

A schematic circuit representation of a six-transistor SRAM is sketched in Fig. 1. Notice that the common drain of the left inverter D1 is connected to the common gate of the right inverter G2 and vice versa. Normally such a connection is made with a metal via contacting the drain and the gate polysilicon. A much more compact arrangement can be achieved by building two transistors on opposite sides of the gate oxide, as shown for the n-type drive transistors M1 and M2 in Fig. 2. In this vertical integration scheme, the connection between the drain of one transistor and the gate of the other is not necessary because the drain replaces and acts as the gate of the other transistor.

Given the SRAM circuit connections, the same vertical integration scheme of Fig. 2 can be adopted for the two p-type load transistors M3 and M4. Eliminating the drain-to-gate connections combined with the vertical integration structure will definitely reduce the cell size. Likewise, other combination of n-MOSFETs and p-MOSFETs are considered.

We will discuss two major problems facing the practical realization of the structure sketched in Fig. 2, i.e. the epitaxy of the multilayer structure and the realization of the necessary doping profiles.

As for this latter issue, we will propose the use of a single implant mask to self align the source and drain of the bottom transistor with the drain of the top one, which is essential for the correct operation of the vertical structure. Moreover, the n+ layers in both the epi-Si and the bulk-Si should have high concentrations at the Si/SiO2 interface, while keeping the concentrations of n-type dopant at the opposite side of the oxide negligible. We will show by Monte Carlo process simulation that both conditions can be obtained by channeling implantation along <110 directions.

Using 2D drift-diffusion simulations, we will show the static and dynamic characteristics of the proposed vertical SRAM cell. The results indicate that the cell functionality is demonstrated and that the symmetrical behavior can be obtained by leveraging on doping engineering optimization.

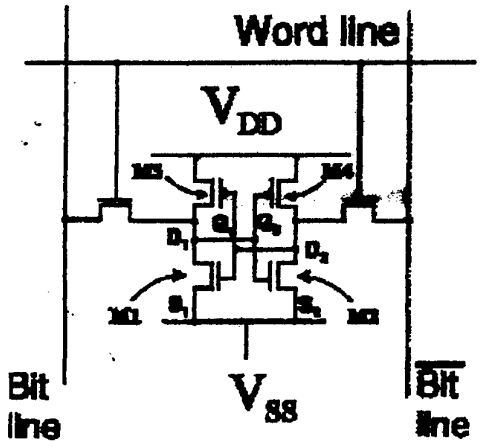

Figure 1. Schematic representation of a CMOS SRAM cell.

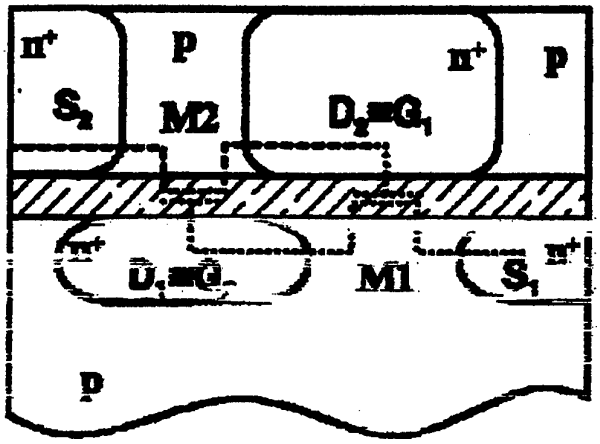

Figure 2. Schematic representation of the vertical integration of the two nMOS (M1 and M2) of Fig. 1. The shaded area is a gate oxide separating the two channels. The drain of the M1 transistor, D1, acts as the gate of M2; while the drain of the M2 transistor, D2, acts as the gate of M1.

OPTOELECTRONICS AND PHOTONICS-I

Photonic Band-Gap Lasers and Nanocavities

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We demonstrate a new nanocavity laser formed from a single defect in a two-dimensional photonic crystal fabricated into InGaAsP quantum well active material. The optical microcavity forms a mode volume of only 0.3 cubic wavelengths, the smallest reported laser cavity to date. Pulsed lasing has been observed at a wavelength of 1.5 microns at 150 K. We also describe the design and performance of this design and larger room temperature laser cavities.

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Progress in Femtosecond Semiconductor Optoelectronic Devices

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Ultrafast optoelectronic devices will be a key to the development of telecommunication systems exhibiting a throughput beyond 1 Tb/s. This talk describes the recent progress in semiconductors-based optoelectronic devices for the operation in the sub-picosecond and femtosecond time domain, focusing on the work being carried out in the Femtosecond Technology project. Present status and prospects of ultrashort-pulse light sources and ultrafast all-optical switches are discussed.
Recent monolithic mode-locked semiconductor lasers have exhibited a high (200 GHz) repetition rate and a ultrashort (500 fs) pulse width. A variety of ultrafast phenomena and device structures are being studied for ultrafast all-optical switches. They include ultrafast electron spin relaxation and intersubband transition in multi-quantum well (MQW) structures. A different approach using Mach-Zehnder interferometer switch structure has shown femtosecond operation. Prospects of new semiconductor materials and devices including nanostructures and quantum wires and dots are discussed in view of the femtosecond applications.

Quantum Cascade Lasers

Sirtori

The Abstract is not available

Nano-Optoelectronics in Technology Roadmap

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With the dramatic success of communication & computer technologies, information industries has been growing on a global scale. In the 21st century, the role of electronics, computer, and communication technologies will be more important for the contribution to human society. To accelerate the progress of such technologies, both market-based free competition and strong leadership conducted by the government are indispensable.

In this paper, we discuss an impact of nano-technologies and nano-optodevices on the info-com society in the 21st century on the basis of the technology roadmap for optoelectronics. The technology roadmap has been drawn for telecommunications, data storage, and display technologies made by the Optoelectronic Industry and Technology Development Association (OITDA) in Japan since 1996. One of key messages of the roadmap is that nanodevices, such as quantum dot lasers and all-optical switching devices, are targeted technologies.

We also discuss our recent research progress on nitride VCSELs and quantum dot lasers and single quantum dot near-field spectroscopy.

High Speed Resonant-Cavity InGaAs/InAlAs Avalanche Photodiodes

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The evolution of long-haul optical fiber telecommunications systems to bit rates greater than 10 GB/s has created a need for avalanche photodiodes (APDs) with higher bandwidths and higher gain-bandwidth products than are currently available. It is also desirable to maintain good quantum efficiency and low excess noise. At present, the best performance (f3dB ~ 15 GHz at low gain and gain-bandwidth product ~ 150 GHz) has been achieved by AlInAs/InGaAs(P) multiple quantum well (MQW) APDs. Previously, we have demonstrated a record bandwidth (33 GHz at low gain) and gain-bandwidth product (290 GHz) using an AlGaAs/GaAs/InGaAs resonant-cavity APD with separate absorption, charge and multiplication (SACM) regions[1]. While these APDs also achieved a high external quantum efficiency of ~70% and low multiplication noise ($k < 0.3$), the spectral response was limited to the wavelength range near $\lambda \sim 0.9\ \mu m$ which, in turn, restricted their use for long-haul high-bit-rate systems. Recently, we have extended this work to wavelengths near 1.55 μ m with a resonant-cavity InAlAs/InGaAs APD. A unity-gain bandwidth of 24 GHz and a gain-bandwidth-product of 290 GHz were achieved. These are both the highest reported values for APDs operating at 1.55 μ m.

The APDs that have been widely deployed for high-bit-rate optical fiber systems utilize an In0.53Ga0.47As absorption region with InP as the multiplication region. However, the gain-bandwidth-product and unity-gain bandwidth, which are typically below 100 GHz and 6-8 GHz, respectively, for commercially available devices, are both insufficient for 10 GB/s applications. In addition, the multiplication noise is characterized by a k value of ~0.5. The low gain-bandwidth product and relatively high noise are due, in large part, to the fact that the electron and hole ionization rates in InP are comparable, which results in a symmetric multiplication process that exacerbates the noise and contributes to long avalanche build-up times. A number of approaches, including multiple quantum well multiplication regions, have been investigated to improve the noise characteristics and frequency performance of APDs [2]. Recently, we have reported that APDs with very thin In0.52Al0.48As multiplication regions exhibit lower multiplication noise than would be predicted by conventional noise theories. The resonant-cavity SACM APDs described in this talk utilize a 200 nm-thick InAlAs multiplication region and have exhibited very low multiplication noise ($k = 0.18$). The excellent noise performance will be discussed in terms of a new theory that utilizes history-dependent ionization coefficients[4]. For 170 μ m-diameter mesa-isolated devices, the dark current was <5nA biased at 90% of breakdown. The spectral response shows the peak quantum efficiency was ~70% at unity-gain bias. For devices with a 200 nm-thick InAlAs multiplication region and a 150 nm InAlAs charge layer, a gain-bandwidth of 290 GHz was achieved, which is in good agreement with simulations. These devices also show a unity-gain bandwidth of 24 GHz.

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Vertical Cavity Lasers and Microresonators

Dapkus

The Abstract is not available

SOI and MEMs

Why can Smart-Cut® change the future of microelectronics

A. J. Auberton-Hervé
President Corporate SOITEC

Smart Cut® technology offers the engineering tool to change the semiconductor material world. Based on hydrogen induced splitting and atomic bonding, very thin film of any semiconductor material can be cut and moved to a mechanical support compatible with the microelectronic. The first examples of products showing the variety of the Smart Cut® technology application are SOI (Silicon on Insulator), Silicon on quartz or Glass. In both cases a monocrystalline silicon film in the range of 100nm is transferred on a non-crystalline support. Many other use of the Smart Cut principle have been demonstrated, including 3D packaging, MEMS, or other semiconductor material than silicon as a transfer layer. However the technical interest of this technology is not the only one which justify the title of this talk. Smart Cut® provides an economical solution for large wafer size (i.e. 300mm and beyond) through the SOI approach which potentially could be cheaper than standard silicon approach.

Advanced Sensors and Microsystems on SOI

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In the recent decade microsystem technologies have become a very important field. A lot of miniaturized sensors and microsystems based on silicon technologies have been developed and are in production now. Airbag control for example is mostly based on silicon acceleration sensors. Besides the existing products new products are emerging like drug delivery systems, labs on chip for DNA-analysis or electronic noses.
Using SOI new sensor and actuator concepts have become possible. Dielectric insulation offers new possibilities concerning mechanical, thermal or electrical behaviour. Microsensors for high temperature application including CMOS electronics are under development. This paper will give examples of pressure and acceleration sensors based on SIMOX and on bonded wafer technology. In addition examples of more complex microsystems like a retina implant system will be given.

Challenges in Mainstreaming SOI Technology

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The first microprocessor (for mainstream use) using SOI technology will be shipped in 99. This is the first application of a mainstream SOI CMOS technology that is developed and installed in manufacturing line. The main attraction of SOI technology is its performance advantage of 20-35% over bulk CMOS of the same generation (equivalent to 1-2 years of bulk CMOS). SOI also offers key advantage in power consumption. In this paper some of the key challenges in material, device, circuit, and manufacturing issues that had to be overcome, before SOI became a "mainstream" CMOS technology, are reviewed. Key results (including applications to large processors) from 0.22, 0.18 and 0.15 _m SOI CMOS technology are presented. SOI will replace bulk Si for deep sub-micron CMOS technologies.

Optimized Design of Subband Structure in MOS Inversion Layer for Realizing High Performance and Low Power Si MOSFET's

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Higher current drive is always a strong demand for advanced Si MOSFETs. In less than 0.1 um MOSFETs, however, conventional ways to increase the drain current, reduction in the channel length and/or the gate oxide thickness would be limited more and more, because of the short channel effect, the difficulty in the lithography and direct tunneling current in ultra-thin gate oxide. In addition, the severe influence of inversion-layer capacitance on low voltage operation of scaled MOSFETs requires the reduction in carrier concentration in the channel and the increase in carrier velocity, in order to reduce the power consumption. Therefore, the enhancement of inversion-layer mobility in Si MOSFETs, which leads to the significant velocity overshoot, is a quite important issue.

In this paper, an engineering scenario of the subband structure in inversion layer to enhance electron mobility in Si MOSFETs will be presented. It will be shown that a key in the design of the subband structure is to enlarge the energy difference in the subband energy of the 2-fold and the 4-fold valleys and, as a result, the electron occupancy of the 2-fold valleys. The electrical characteristics of two promising device structures, SOI MOSFETs with SOI thickness thinner than the inversion layer of bulk MOSFETs and strained-Si MOSFETs, which can realize this engineering, will be shown through theoretical calculations. The significant modulation of the subband structure in such thin SOI films will be shown to provide higher current drive than bulk MOSFETs, because of the increase in both the inversion-layer mobility and the inversion-layer capacitance. Advantages and disadvantages of these device structures will be addressed from the viewpoint of the applicability to CMOS and possible modified structures will also be discussed.

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EMERGING MICROELECTRONIC MATERIALS

Applications of Carbon Nanotubes and New Functional GaN Nanotubes

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Carbon nanotubes have been synthesized during the formation of fullerenes using arc discharge of graphite rod. Recently single-wall carbon nanotubes have been produced with very high yields by the laser vaporization of graphite powders mixed with small amount of transition metals[1]. Strong field emission from carbon nanotubes have been observed, suggesting the applicability to flat panel displays. Despite such efforts, applications to memory devices and several functional devices are still challenging. In this report, we will demonstrate that carbon nanotubes, instead of metal alloys, can be easily applied to an electrode of the secondary battery. Carbon nanotubes electrodes have several advantages over the existing metal electrodes. H storage ability and the stability of carbon nanotubes during repetition of charging and discharging will be compared to those of metals. The results will be analyzed both experimentally and theoretically by density-functional atomistic calculations.

With an advent of epitaxial growth techniques for GaN, efficient blue light-emitting InGaN has been tried for band gap engineering by varying In compositions. However, it is still difficult to grow and control high In composition due to the strain between InGaN and substrate. Therefore a new form of GaN is always desirable if possible. In this report we propose a new phase of GaN, a nanotube. Our assertion is based on the density-functional calculations[2]. We will show that GaN nanotubes are as stable as carbon nanotubes and can be synthesized under some extreme conditions. Pure boron-nitride and boron-carbon-nitride nanotubes have been successfully produced by arc discharge. The existence of BN nanotubes suggests the possibility of other nitride nanotube synthesis such as CN and GaN. The present calculations show that the strain energies, the energy costs to wrap up graphitic GaN sheets into nanotubes, are comparable with those of carbon nanotubes, ensuring again the possibility of GaN nanotube formation. Yet, the initial nucleation seeds for GaN nanotube formation will play a crucial role for growth. The band gap and the effective masses vary with the diameters, exhibiting the quantum confinement effect.

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A novel crystallization method of amorphous silicon

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A new crystallization process of amorphous silicon has been developed for low temperature, large-area electronics on glass substrate. Amorphous silicon (a-Si) was crystallized by metal induced crystallization (MIC) using a very thin-layer of Ni or Co[1-3]. The density of the metal particles on the a-Si surface was less than 1018 cm-2. The crystallization temperature can be lowered to 380C and a high performance thin-film transistor has been developed at the process temperature of less than 450C. A large continuous grain of higher than 50um has been grown using this technique. The growth kinetics for the MIC poly-Si will be discussed with the structural and physical properties of the poly-Si films.

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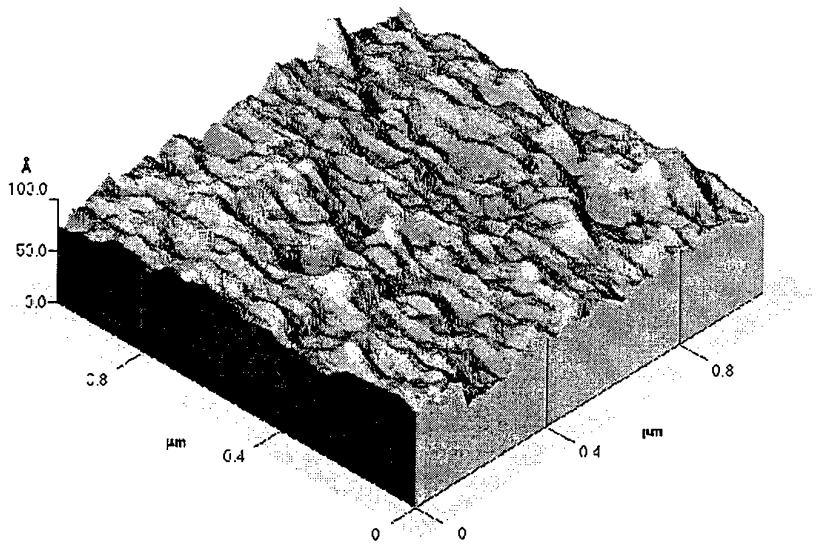

Heterogeneously Integrated Circuits Using Wafer Bonding and Compliant Substrate Technologies

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Mixed signal circuits represent an important trend for the development of new generation integrated circuits. In the foreseeable future, circuits will deal with not only different electronic signals (digital, analog, RF) but also non-electronic signals such as optical, mechanical, chemical and biological signals. It is expected that the entire systems that can fulfill complicated functions will be integrated on a single chip and Si will be the platform for the new circuits. However, other materials such as compound semiconductors will have to be integrated with the Si-based microelectronic circuits to provide functions that can not be achieved by silicon. The technology of integrating various semiconductors with Si becomes the corner stone for the new generation ICs. Conventional flip-chip bonding and technologies evolved from flip-chip bonding will be increasingly difficult to meet the stringent requirements for such complex heterogeneously integrated systems. Hence people are actively seeking new material integration technologies that are more versatile and scalable than the current technologies. In this talk, we will discuss several promising approachess, including wafer bonding and compliant substrates, to integrate III-V materials with Si. Optical interconnect and optical MEMS circuits will be discussed as examples and test vehicles for these new technologies.

Brief bio sketch of the author:
Professor Yu-Hwa Lo received his Ph. D. in 1987 from U. C. Berkeley. He worked for Bellcore as a Member of Technical Staff before he joined the faculty of Cornell University in 1991. His research interests are in semiconductor materials, optoelectronic devices and circuits, and MEMS. He has published more than 100 journal articles and 130 conference papers and authored two book chapters. He has edited one book and several special issues including the special issue on optoelectronics technologies for the IEEE Proceedings. He has served on the technical committees for EMC, MRS meetings, IEEE LEOS conferences, OSA meetings, SPIE meetings, and many other international conferences and workshops. He holds 8 patents and has 10 applications pending. He received several teaching awards, the UC regent fellowship (1983), Lilly foundation fellowship (1996), and the outstanding paper award from the Indium Phosphide and Related Materials (IPRM) conference (1998).

Polarization Issues in GaN and Related Heterostructures in the Context of Devices

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Wide bandgap nitride semiconductors have recently attracted a great level of attention owing to their direct bandgaps in the visible to ultraviolet regions of the spectrum as emitters and detectors. Moreover, this material system with its favorable heterojunctions and transport properties began to produce very respectable power levels in microwave amplifiers. If and when the breakdown fields achieved experimentally approaches the predicted values, this material system may also be very attractive for switching power devices. In addition to the premature breakdown, a number of scientific challenges remain including a clear experimental investigation of polarization effects. Being non-centro-symmetric and various binaries having different ionicities, nitrides exhibit large piezoelectric effects when under stress along the c-direction, and spontaneous polarization when heterostructures are formed. Polarization causes a sizable red shift (Stark Effect) in transition energies in InGaN/GaN and AlGaN/GaN quantum wells. Polarization and pyroelectric effects due to heterointerfaces in an ionic crystal, misfit and thermal strain, anisotropy, and temperature gradients have important ramifications in electronic devices, particularly in modulation doped FETs. For example, electric field caused by polarization effects can increase or decrease interfacial free carrier concentrations. As in the case of quantum wells, the literature interpretation of polarization effects in devices has so far been lumped into piezoelectric effects. In this presentation, polarization effects vis a vis devices will be treated.

MOCVD - The Key Technology for the Industrial Application of Quantum Devices

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Zero threshold quantum dot as well as quantum cascade laser, single electron circuits and photonic bandgap materials are upcoming technologies which will dominate the electronic and optoelectronic market in the next century. All these devices realized in various material systems e.g. GaAs/AlGaAs, InP/InGaAsP, InSb/AlInSb, GaN/AlInGaN rely on ultrathin layers, sharp interfaces and precise doping profiles.
MOCVD is the only epitaxial growth technology which fulfills all requirements of the advanced layer structures including sufficient homogeneity in the terms of layer thickness, composition and conductivity control on large wafer areas, that means multiple 2", 4" or 6" wafer, handling of phosphorus materials and abrupt interfaces. The main properties can be reproducibly controlled with the respective standard deviation of less than 1%. The current understanding of the growth process and the available multiwafer Planetary Reactors® will be discussed with respect to the growth of quantum structures. InGaAsP/InGaAsP-, InGaN/GaN-, InPSb/InAsSb/InAs- multiquantum well structures demonstrate the unique properties of MOCVD. Recently discovered selforganization phenomena like Stranski-Krastanow growth or spinoidal decomposition of strained structures or surface selective growth show new and industrial relevant ways to achieve useful quantum devices on production scale. The available hardware based on the developed understanding of the physics and chemistry of the growth and the achieved results on quantum structures allows a detailed forecast on future trends and market shares of the MOCVD technology for quantum devices.

Brief bio sketch of the author:
Dr Holger Juergensen is active in compound semiconductors since 1977. He received his M.S. degree in Physics in 1981 and his Ph.D. in 1985, both from the Technical University of Aachen, Germany. In 1981-1986 he was senior staff member specializing in MOCVD and epitaxy research at the Institute of Semiconductor Technologies at Aachen University. He received awards for Technology Transfer in 1986 from the German Federal Secretary of Culture and Science, and for Innovations in 1988 from the German Minister for Research and Technology. He is the author of over 100 scientific papers, mainly on MOCVD. He is member of the IEEE, SEMI, SPIE, MRS and DGKK.
From 1983 to July 1997, Dr Juergensen was President and Technical Director of AIXTRON Semiconductor Technologies GmbH, Aachen, Germany, and, amongst other duties, responsible for all compound semiconductor MOCVD technology development. Since August 1997 he is President (Vorstand) of AIXTRON AG, Aachen, Germany. Since 1986 he is also President of AIXTRON Inc., Atlanta GA, USA.

PHYSICAL PHENOMENA AND QUANTUM DEVICES

Physical Phenomena in semiconductor compounds

The role of Scanning Probe Microscopes for Characterization of Physical Phenomena in Quantum Devices

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The measurement of the physical properties of individual semiconductor quantum objects at a length scale corresponding to the de Broglie wavelength of electrons in most semiconductors (a few nm) is a difficult challenge. Determination of spectroscopic properties of individual quantum objects buried below the surface is particularly daunting. In this paper we will review recent progress in the use of Scanning Tunneling Microscopy (STM) based techniques, such as BEEM (Ballistic Electron Emission Microscopy) for the study of novel quantum objects will be reviewed. Examples of the use of this technique for studying heterojunction band offsets and resonant tunneling through quantum dots will be presented. The use of this technique to image current transport on a local scale through GaN films will show the power of imaging buried defects such as threading dislocations in the material. Potential modifications of the technique for imaging the optical emission under conditions of Ballistic Electron injection will also be discussed.

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Brief bio sketch of the author:
Venkatesh ("Venky") Narayanamurti is Dean of the Division of Engineering and Applied Sciences and Gordon McKay Professor of Engineering and Applied Sciences at Harvard University. From January 1992 to September 1998 he served as the Richard A. Auhull Professor and Dean of Engineering, as well as Professor of Electrical & Computer Engineering, at the University of California at Santa Barbara. He was Vice President of Research and Exploratory Technology at Sandia National Laboratories, Albuquerque, NM, from May 1987 to January 1992. He obtained his Ph.D. in Physics from Cornell University in 1965. Between 1965 and 1967 he served as Assistant Professor of Physics, Indian Institute of Technology, Bombay. He joined AT&T Bell Laboratories in 1968 as a Member of Technical Staff, and became Director of Solid State Electronics Research in 1981. He has published widely in the areas of low temperature physics, superconductivity, semiconductor electronics and photonics. He is credited with developing the field of phonon optics-the manipulation of monoenergetic acoustic beams at terahertz frequencies. He is currently very active in the field of Ballistic Electron Emission Microscopy and Spectroscopy of semiconductor nanostructures.
Narayanamurti is a member of the National Academy of Engineering. He is also a Fellow of the American Physical Society, the American Association for the Advancement of Science, the IEEE, the Royal Swedish Academy of Engineering Sciences, the Indian Academy of Sciences, and Sigma Xi, the Scientific Research Society. He is currently chair of the National Research Council (NRC) Panel on the Future of Condensed Matter and Materials Physics and chair of the U.S. Department of Energy?s Review Committee on the Accelerated Strategic Computing Initiative; and he serves on numerous committees of the NAS/NAE/NRC, American Physical Society, IEEE and professional technical conferences. In addition to his duties as Dean and Professor, Narayanamuri lectures widely on solid state, computer, and communication technologies, and on the management of science, technology and public policy.

Quantum Dot Lasers: Theoretical Analysis of Performance

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Quantum Dot Lasers (QDLs) are very promising devices. They should have extremely low values of threshold currents and show week temperature dependence of basic characteristics. These properties are due to their very narrow gain spectral functions. Actually, QDLs combine the advantages of high efficiency of direct electric pumping and the high tunability of characteristic of semiconductor heterolasers with narrow gain spectral lines. We will present a theoretical analysis of the following operating characteristics of QDLs:
(i) threshold current density and its temperature dependence,
(ii) threshold current density for multiple mode generation due to spatial hole burning,
(iii) linewidth enhancement factor caused be phase-amplitude modulation.
All of these issues are of great importance for QDLs applications. The main point of our analysis is the careful consideration of the consequences of the inhomogeneous broadening of the gain spectrum due to technological dispersion of the quantum dot parameters.

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Employment: 1960-1988 - researcher at Research Centers of Microelectronics Industry in Moscow, 1988-present - Head of Laboratory and Head of Solid State Electronics Division at the A. F. Ioffe Physical-Technical Institute
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Spin-filter Effects in Transmission of Free Spin-polarized Electron Through Ultra-Thin Magnetic Layers

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Spin-filter effects (at work in giant magneto-resistance for instance) have raised a broad interest in view of their promises of application for high density recording or magnetic nano-sensors. Particularly appealing appears the conjunction of magnetic layers associated with very thin isolating tunnel barriers or deposited on semiconductors. The concept of spin electronics has emerged from these ideas and spin polarized electron scanning tunnel microscopes have provided some results dealing with the spin-filter effects, on a nanometric scale.
We shall present spin-dependent transmission experiments where free spin-polarized electrons, are injected in vacuum through thin magnetic layers at energies between 2 and 100 eV. These very thin layers are either embeded in self-supporting gold foils (200 Å thick) or deposited on a semiconductor substrate. The transmission asymmetry arising when incident and target spins are either parallel or antiparallel is measured. The electronic current is detected as a collector current in the semiconductor substrate or in a Faraday cup after energy analysis in the case of self-supporting foils. Some considerations will be given about the dynamics of the "spin tagged" electrons in the solids.

Current State of the Theory of the Quantum Hall Effect

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While the present understanding of the Integer Quantum Hall Effect is satisfactory, at least at the qualitative level, this is not the case for the Fractional QHE, which still remains a mystery after 15 years of extensive experimental and theoretical investigations. I will give a critical review of the existing ideas for explaining the observed singularities at rational filling factors, especially the widely accepted concept of "composite fermions". Although it seems, that this concept is strongly supported by many striking experimental facts, it has no sound theoretical foundation, it leaves many simple qualitative questions unanswered, and should be replaced by a better theory. The understanding of the Fractional QHE, which is yet to come, may have an important impact on the future development of solid state elctronics.

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Observation of Multiple Excitonic Optical Rabi Oscillations in a Semiconductor

Peyghambarian

The Abstract is not available

PHYSICAL PHENOMENA AND QUANTUM DEVICES

Quantum Devices and Materials

High Power 3-12 um Semiconductor Lasers: Roadmap for the 21st Century

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Since the discovery of infrared light by Sir William Herschel in 1800, a lot of effort has been devoted to the research on infrared radiation. Following the works of Kirchhoff, Stefan, Boltzmann, Wien and Rayleigh, Max Planck culminated the effort with the well-known Planck's law.

Although infrared emitters and detectors are still in the stage of development, they have wide potential applications in various areas of technologies as well as basic research. Infrared lasers have many military, medical, and industrial applications like infrared countermeasure, infrared-based surgery, and material cutting and processing in industry. Infrared detectors are also widely used for applications like night vision, target detection, and infrared thermal sensors.

There are also many important applications where both infrared lasers and detectors are required as the source and sensor. Some of these applications are: high resolution molecular spectroscopy, ultra low loss (less than 2.5x10-4 dB/km), optical fiber (fluoride based glasses) communication, trace gas monitoring, air pollution analysis (since a variety of molecules, including all hydrocarbon, have strong absorption lines in this band), and none invasive medical diagnostics. Military applications such as: laser radar system, also utilize this region (3 to 5 um and 8 to 14 um) because it is highly transmissible.

In all these areas, semiconductor infrared lasers and detectors are the ideal candidates due to their intrinsic advantages of wide wavelength coverage, low cost, simplicity of operation and possibility of hybrid systems and compact packages. Unfortunately, after several decades of progress, currently available infrared lasers and detectors still require low temperature operation because of some basic limitations as Auger recombination and high thermal generation rate. However, in most of the applications the cryogenic coolers are not desirable because of their short lifetime and the added power consumption, weight, volume and costs. Therefore, uncooled and multi-spectrum semiconductor lasers and detectors are highly demanded.

In this talk, the status of the currently available infrared lasers will be discussed, and the advantages and disadvantages of each of these methods will be presented. Then the basic physical limitation of the current technology to achieve high operating temperature will be addressed. As a future direction, we will show that lower dimension devices, like quantum wire and quantum dots, can dramatically improve the performance of infrared lasers for uncooled multi-color devices of the next century.

Acknowledgement

This work is supported through the Defense Advanced Research Projects Agency (DARPA) and the U.S. Army Research Office (ARO) with the support and encouragement of Dr L. N. Durvasula and Dr H. Everitt.

Coherent coupling in multiwavelength modelocked semiconductor diode lasers: physics and applications

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Multiwavelength generation from semiconductor diode lasers will play critical roles in a variety of optical communication, newtorking and signal processing. Recently, we have demonstrated the generation of 20 wavelength channels from a novel modelocked semiconductor diode laser, at rates of 5 GHz. Careful examination of the temporal and spectral output from this source exhibits unique behavior which can be attributed to nonlinear effects, such as four wave mixing, that occur within the semiconductor diode laser under modelocked conditions. We will show that these effects can be exploited to establish broadband spectral coupling between the independent modelocked channels, and may lead to novel methods for arbitrary waveform generation from modelocked semiconductor diode lasers. Applications of this laser source in the areas of high speed optical links and analog to digital converters will also be discussed.

Heterostructure devices in infrared detector technology

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Lockheed Martin has also fabricated dual-color FPAs by stacking quantum well layers with the desired spectral responses. As the IR technology continues to advance, there is a growing demand for multi-spectral detectors for advanced IR systems with better target discrimination and identification. One of such two-color HgCdTe detector that has been recently reported is the bias-selectable back-to-back photodiode.

At present efforts in infrared (IR) detector research are directed towards improving the performance of single element devices, large electronically scanned arrays and to achieve higher operating detector temperature. Another aim is to make IR detectors cheaper and more convenient to use. Recent progress in IR photon detector technologies is connected with using sophisticated heterostructure devices. HgCdTe remains to be the most important material for infrared photodetectors despite of numerous attempts to replace it with alternative materials [Schottky barriers on silicon, doped silicon detectors, GaAs/AlGaAs multiple quantum wells, GaInSb strain layer superlattices, and especially two types of thermal detectors: pyroelectric detectors and silicon bolometers]. None of these competitors can compete in terms of fundamental properties. In addition, HgCdTe exhibits nearly constant lattice parameter that is of extreme importance for new devices based on complex heterostructures. Examples of novel devices based on three-dimensional heterostructures are presented.

As the IR technology continues to advance, there is a growing demand for multispectral detectors for advanced IR systems with better target discrimination and identification. The performance of two-color detectors are presented: back-to-back HgCdTe photodiodes, and stacked quantum well GaAs/AlGaAs quantum well photoresistors.

Materials for the Next Generation of Long Wavelength Infrared Detectors

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New infrared (IR) detector materials with high sensitivity, multi-spectral capability, improved uniformity and lower manufacturing costs are required for numerous space-based infrared imaging applications. To meet these stringent requirements, new materials must be designed and grown using semiconductor heterostructures, such as quantum wells and superlattices, to tailor new optical and electrical properties unavailable in the current semiconductor repetoire. Two approaches to designing the next generation of IR materials are being pursued in the Sensor Materials Branch of the Air Force Research Laboratory. One of these approaches is a strained layer superlattice (SLS) composed of thin InAs and GaInSb layers. While this material shows theoretical promise, there are still several materials growth and processing issues to be addressed before this material can be transitioned to the next generation of infrared detector arrays. The second approach utilizes p-type GaAs/AlGaAs multi-quantum wells. In this case the growth technology is more mature, but optimizing the sensitivity of these materials is still an issue. Our research is focused on addressing the basic materials design, growth, optical properties, and electronic transport issues of these superlattices and multi-quantum wells. The physics of optimized materials designs and the current status of MBE grown materials for IR detection will be reviewed.

Brief bio sketch of the author:
Dr. Gail J. Brown is a senior Research Leader in the the Sensors Materials Branch of the Materials & Manufacturing Directorate of the Air Force Research Laboratory. She leads a team of over 50 researchers working in the area of semiconductor materials development. This research group is mainly focused on III-V semiconductor materials for microwave and infrared detection and laser devices. Dr. Brown's own research interests are in the area of quantum structures for infrared detectors. Dr. Brown has authored/co-authored over seventy papers and two book chapters on optical properties of various semiconductor materials ranging from extrinsic silicon in the early 1980s to multi-quantum well and superlattice heterostructures at present. Dr. Brown's special emphasis has been photoresponse studies of these materials.
Dr. Brown received a Master's in Physics in 1979 from Wright State University and a Doctorate in Materials Engineering in 1994 from the University of Dayton. She has worked as a research physicist at the Air Force Research Laboratory since 1980.

MOCVD Growth of High Quality Gallium Nitride Based Electronic and Photonic Devices

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MOCVD growth conditions have been found to have a critical influence on the performance of electronic and optoeletronic devices. The deposition conditions of the low temperature buffer layer was found to highly influence the performance of GaN/AlGaN modulation doped field effect transistors (MODFETs) and blue laser diodes (LDs). Using optimized growth conditions we have observed high 2DEG mobilities of 1700 cm2/V*sec and 6000 cm2/V*sec at 300 K and 20 K, respectively. These materials have been incorporated into modulation doped field effect transistors (MODFETs) which displayed high transconductance (240 mS/mm), and large gate to drain break down of 340 V for Lgd = 3 microns. Microwave power performance of 3 W/mm at 20 GHz was measured, which is quite promising given that the device was uncooled and deposited on sapphire.

Room temperature (RT) pulsed operation of blue (420 nm) nitride based multi-quantum well (MQW) laser diodes grown on a-plane and c-plane sapphire substrates have also been demonstrated. This device is desirable for optical storage systems (e.g. high density digital versatile disk, HD-DVD), printing, display technology, medical surgery and chemical monitoring. Blue laser structures investigated include etched and cleaved facets as well as doped and undoped quantum wells. Metal organic chemical vapor deposition (MOCVD was employed to grow the MQW active region. The laser exhibited narrow (0.1 nm linewidth and strongly TE polarized emission at 419 nm. Threshold current densities as low as 9.2 kA/cm2 were observed for GaN MQW lasers with uncoated reactive ion etched (RIE) facets on c-plane sapphire. Cleaved facet lasers were also demonstrated with similar performance on a-plane sapphire. Threshold current increased with temperature with a characteristic temperature, T0, of 114 K.

Acknowledgement. The author would like to acknowledge the support of DARPA (Bob Leheny), ONR (Yoon Soo Park), and HP (SY Wang).

Fundamental Limits of Performance of AlGaN/GaN HEMT's

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The dominant effect of electrical polarization in undoped AlGaN/GaN HEMT's is presented. The experimental dependence of the drain-source avalanche breakdown voltage on device geometry will be given. Optimum frequency response is obtained using .30-.35 aluminum fraction in the 200-300 Å thick barrier, which induces ~ 1 x 1013/cm2 2DEG sheet density. Mobility values in the range of 1,000-1,500 cm2/V-s are obtained both by OMVPE and MBE, and the saturation velocity is ~ 1.2 x 107 cm/s. This yields an intrinsic Yt value of 94 GHz for a gate with .15 µm physical length. These devices with a 1 µm gap between gate and drain have 35 Vds breakdown voltage, while .75 µm gate devices have breakdown voltages above 140 Vds. On sapphire substrates, a 1.5 mm periphery devices with .32 µm gate length have yielded 2.7 W at 78% optimized power-added efficiency at 10 Vds at 4 GHz. The single gate, .32 µm x 150 µm, device at 10 GHz yielded 2.4 W/mm at 36% power-added efficiency at 18 Vds. The average power is expected to increase 10:1 in the future, using SiC substrates. It is predicted that 100 W average power, at 60% power-added efficiency, can be delivered at 10 GHz using a pair of circuits operated in class B/Push-pull, with a low-loss balun in the output.

Acknowledgement:
This research is funded by ONR contract # N00014-96-1-1223, Dr. John Zolper, monitor.

Brief bio sketch of the author:
BIO - LESTER F. EASTMAN: B.S. 1953 Cornell University; M.S. 1955 Cornell University; Ph.D. 1957 Cornell University. Since 1965 he has been doing research on compound semiconductor materials, high speed devices, and circuits, and has been active in organizing workshops and conferences on these subjects at Cornell from 1967-1991. Over the years his students and former students have made significant contributions and won national and international prizes by advancing the state of the art of molecular beam epitaxy and microwave transistors, and more recently optoelectronic devices. In 1977 he joined other Cornell faculty members in obtaining funding and found the National Research and Resource Facility at Cornell (now Cornelll Nanofabrication Facility). He initiated the Joint Services Electronics Program at Cornell in 1977 and directed it for ten years. During the 1978-1979 year he was on leave at MIT's Lincoln Laboratory, and during the 1985-86 year he was at IBM Watson Research Laboratory. During 1983 he was the IEEE Electron Device Society National Lecturer. He was a member of the U.S. Government Advisory Group on Electron Devices from 1978-1988, and serves as a consultant to industry. He has been a Fellow of IEEE since 1969. He has been a member of the National Academy of Engineering since 1986, and the Electromagnetics Academy since 1990, and has been appointed the John L. Given Foundation Professor of Engineering at Cornell in January 1985. In 1991 he was awarded the Welker Medal and Annual Award of the International Symposium on Gallium Arsenide and Related Compounds, in 1994 he was made a Humboldt Senior Fellow, and in 1995 he was given the Aldert van der Ziel Award, in 1999 IEEE Graduate Teaching Award

POSTER SESSION

Effect of Electron Electron-Cloud Interaction on Schottky Metal Barrier Height to Two Dimensional Electron Gas

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Reduced dimensional nature of confined two dimensional electron gas (2DEG) substantially affects its transport properties particularly when contact is made to a three dimensional (3D) system. Previous work [1,2], has shown that in a Three-dimensional (3D) to two-dimensional (2D) contact system, the quantized nature of the energy of the 2D system imposes important changes on thermionic emission of carriers from a 3D metal to 2DEG. The suggested effects include changes in the Richardson constants, temperature dependence behavior, and metal to semiconductor barrier height. The latter is particularly relevant to optical and electronic device behavior since Schottky metal is comonly used in field effect devices and in photodiodes. Interestingly in actual devices, barrier heights higher than what is theorized based on the first confined state, are measured. In this paper we propose an additional mechanism of barrier height enhancement in 3D-2D contacts which is due to the repulsive Coloumbic force that is exerted by the 2DEG on the thermionically emitted electrons. An analytical derivation of the barrier height due to this effect is given which parallels that of image force barrier lowering mechanism. Thermionic current conduction is then derived based on this enhanced barrier height as well as 3D-2D transport. This electron-2DEG interaction can have as much influence as the confined states do on the barrier height enhancement and helps explain discrepency between theorized and measured 3D-2D barriers. Experimental examples of current changes due to change of carrier concentration in the 2DEG will be given in which increase in 2DEG decreases current conduction; an observation that is opposite of what is seen in HEMT-like devices. Finally, this suggests a mechanism for barrier height modulation in 3D-2D contacts despite Fermi level pinning.

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Optical Absorption Modulation in Heterodimensional Devices

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Efforts to develop a comprehensive body of work on the theory and modeling of heterodimesional devices are currently focused on microwave and low-power electronic applications. In this paper we suggest embedding such structures into the construct of photonic devices in order to gain additional design flexibility and enhanced performance by leveraging the quantum nature of their physical behavior. Heterodimensionality is achieved by placing a metal electrode in direct contact with the two-dimensional electron gas (2DEG) of an AlGaAs/GaAs heterojunction. The quantum confinement produced by the transferred charge accumulation at the heterojunction's interface results in a strong non-uniform electric field which extends far into the GaAs material. The field strength can be controlled by the heterodimensional structure's construction and operation. We have developed closed-form analytical expressions which describe the behavior of the electric field by accurately calculating the sheet carrier density value in these structures. These strong fields produce variations to the complex dielectric permittivity of the GaAs through the Franz-Keldysh effect leading to modulation of the optical absorption characteristics of the device. Both narrow and wide spectral bandwidth photoresponse measurements under different temperautes have been performend in order to analyze and compare the empirical behavior to that expected by numerical computations and device simulations. These results thus allow more accurate modelling of optical response in modulation doped devices and, on the other hand, allow the band structure and the effects of reduced dimensioanlity to be analyzed through optical probing.

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Optimal Control Theory for Optical Waveguide Design: Application to Y-branch Structures

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A recently developed optimal control theory method for optical waveguide design [D. K. Pant, R. D. Coalson, M. I. Hernandez and J. Campos Martinez, ``Optimal control theory for the design of optical waveguides", J. Lightwave Technology 16, p. 292 (1998)] is applied to Y-branch waveguides and Mach-Zehnder modulators. The method, which was adapted from optimal control schemes introduced for quantum control of quantum molecular dynamics using ultrafast light pulses [S. Shi, H. Rabitz, ``Quantum mechanical optimal control of physical observables in microsystems ", J. Chem. Phys. 92, p. 364 (1990)], simultaneously optimizes many parameters in a chosen design scheme; computational effort scales mildly with the number of parameters considered. Significant improvement in guiding efficiency relative to intuitively reasonable initial parameter choices is obtained in all cases.

Carrier screening and polarization fields in nitride-based heterostructure devices

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One of major recent breakthrough in semiconductor physics is the realization of blue lasers based on III-V nitride heterostructures technology, However, several puzzling issues remain unsettled, such as (i) the exact mechanism responsible for laser action and the unusually high threshold densities required, (ii) the blue shift of the transition energy for increasing excitation powers, (iii) the red shift of the transition energy is observed for increasing well width. These phenomena are related to the peculiarity of wurtzite nitrides in having a non-zero macroscopic polarization, comprising both a spontaneous and a piezoelectric component.

In this contribution, we identify both theoretically and experimentally the central reason for these unusual behaviors, namely the interplay of free-carrier screening, well width and macroscopic polarization fields. To account for screening effects, we have developed a self-consistent tight-binding (TB) approach which enables us to describe polarization fields, dielectric screening, and free-carrier screening in a fully self-consistent and non-perturbative way. Optical properties, such as luminescence or gain, is accounted in the TB context without introducing additional fitting parameters. The developed approach has been used to investigate both AlGaN/GaN and GaN/InGaN single/multi quantum well systems.

We shown that free carriers can effectively screen macroscopic polarization fields in nitride quantum wells, resulting in a non-vanishing recombination rate for large wells in normal laser operation. A rather high sheet density is needed to achieve these conditions. We also explained the red shifts vs well width and blue shifts vs sheet density as resulting from the interplay of free-carrier screening and polarization fields. For the GaN/AlGaN quantum wells we shown that the optical properties are strongly affected by the built-in electric field originated by the spontaneous polarization charge, and, to a minor extent, by strain. Indeed, the experimental photoluminescence data obtained can only be explained by accounting for the spontaneous polarization field. We further study the use of doped active region to screen the polarization field and thus increasing the radiative recombination rate.

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CAD Tools and Optical Device Models for Mixed Electronic/Photonic VLSI

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The recent interest in development of photonic VLSI is based on the prospect of a successful heterogeneous integration of digital, optoelectronic, and high-speed analog technologies. This challenge makes computer aided design (CAD) tools to be even more important for the optimal design and ultimate success of mixed technology photonic VLSI than for conventional VLSI, where such tools have long since become an integral part of the technology, as essential as device and circuit fabrication.
Circuit simulation tools such as SPICE have been around since the early seventies, and have contributed in a fundamental way to the phenomenal growth in conventional VLSI over the last decades. We propose to develop similar tools for mixed photonic/electronic VLSI, which will be enhanced to handle the added dimension represented by photonic signals, devices and interconnects.
Two major sets of tasks need to be undertaken to achieve such an objective. First, a new generation of accurate and reliable models for photonic devices, describing the interrelations of optical and electrical inputs and outputs. These models should be compatible with modern circuit simulators, i.e., with response functions preferably described by analytical expressions. Second, to fully utilize the advanced algorithms of existing circuit simulators, all optical signals and interconnects should be described in terms of equivalent electrical signals and interconnects, obeying the basic laws of circuitry imbedded in the simulators, such as Kirchoff's current and voltage laws. Also, since photonic VLSI eventually will evolve to a high integration scale and device density, issues related to the role of the interconnects, limited voltage swing, device-circuit and electronic-optical device-interaction, stray light effect, power budget, etc. will be crucial in determining the success of the photonic VLSI technology [1].
In this paper, we will present a basic approach to establishing a mixed electronic/photonic circuit simulator [1] based on our circuit simulator AIM-Spice [2,3], and present preliminary results on the compact modeling of vertical-cavity surface emitting lasers (VCSELs). The VCSEL model is based on first-order rate equations [4] that can be expressed in terms of an electrical equivalent circuit suitable for implementation in SPICE.

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Generalized Monte Carlo Simulations for Quantum-Transport In Nanostructured Semiconductor Devices

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The Monte Carlo (MC) method, which has been applied for more than 25 years for calculation of semiclassical charge transport in semiconductors, is the most powerful numerical tool for microelectronics device simulation [1].
However, it is well known that the present-day technology pushes device dimensions toward limits where the traditional semiclassical transport theory can no longer be applied, and a more rigorous quantum transport theory is required. This is already the case for, HEMT's with channel length less than 0.1 micron, for superlattices for THz generation where the current flows in the growth direction and for resonant tunneling diodes.
In this contribution, a generalized MC approach for the analysis of hot-carrier transport and relaxation phenomena in quantum devices is proposed [1]. The method is based on a generalized MC solution of the set of kinetic equations describing the time evolution of the single-particle density matrix. The simulation scheme is based on a time-step separation between coherent and
incoherent dynamics. The former, treated within a density matrix picture, accounts in a rigorous way for all quantum phenomena induced by the potential profile of the device as well as for the proper boundary conditions. The latter, described within the basis given by the eigenstates of the potential profile (which includes the applied bias), accounts for all the relevant scattering mechanisms by means of a conventional MC simulation.
Compared to more academic quantum-kinetic approaches, whose application is still limited to highly simplified situations, the proposed simulation scheme can be applied to realistic cases, allowing on the one hand a proper description of quantum-interference phenomena induced by the potential profile and on the other hand maintaining all the well known advantages of the conventional MC method.
As a first application of the above algorithm, we will discuss the scattering-induced suppression of Bloch oscillations in semiconductor superlattices .
As a second example, we will discuss the strong interplay between coherence and relaxation within a resonant tunneling diode, which clearly shows the failure of any pure coherent or incoherent approach in describing such quantum-transport regime. In both cases we investigate the use of such devices as sources for tunable THz radiation.
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Why is 2D high-field electron drift velocity smaller than for 3D electrons?

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A peak electron drift velocity in most compound semiconductors is determined by the intervalley transition. This transition takes place when electrons are heated by the electric field. The electron heating is very effective when the dominant scattering mechanism is polar optical scattering. Theoretically, in a strong electric field, the electron temperature determined by this scattering mechanism can increase indefinitely (electron temperature runaway). In practice, other scattering mechanisms, such as deformation potential optical and acoustical phonon scattering prevent such a runaway for three-dimensional (3D) semiconductors.

Electron scattering in two-dimensional (2D) systems is quite different because of the reduced dimension of the phase space. A remarkable feature of 2D systems is that, for 2D electrons, the runaway effect takes place for scattering on deformation optical and acoustical phonons as well. In this paper, we show that, as a consequence, the dependence of electron drift velocity on a strong electric field changes drastically. The intervalley transition occurs in a lower electric field, and the high-field electron drift velocity is substantially smaller than in 3D semiconductors.

This result is obtained for the simplest model of two-valley semiconductor by solving the coupled system of two Boltzmann equations, describing the electron distribution in the two valleys. The model assumes that the intervalley scattering time is much shorter than the scattering time in the central valley. Our analysis shows that the qualitative results obtained using this model are more general and do not depend on the model assumptions. The prediction of a smaller high-field drift velocity for the 2D electrons agrees with the results of Monte-Carlo simulations for the 2D electrons at the GaAs/GaAlAs heterointerface and with the experimental measurements of the peak velocity in InGaAs/InAlAs quantum wells.

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100-GHz Superconductor Processors for a Petaflops Computer: Design Phase 2

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A multiprocessor COOL system based on superconductor Rapid Single-Flux-Quantum (RSFQ) technology is being developed at Stony Brook within the framework of the Hybrid Technology Multithreaded (HTMT) architecture project. The objective of the current (second) phase of the project is the proof-of-concept design study of a computer that would utilize novel electronic and optoelectronic technologies to achieve petaflops-scale performance (~1015 floating-point operations per second) by 2007. The concept system has multiple levels of distributed memory, namely holographic HRAM, semiconductor SRAM and DRAM, and cryo-memory (CRAM), as well as three types of processors: SRAM- and DRAM-based Processor-In-Memory (PIM) elements operating at room temperature, and RSFQ Superconductor Processors (SPELLs) operating at the temperature of liquid helium (4.2 Kelvin).

Two-level multithreading combined with thread context prefetching (called parcel percolation) are the key techniques of hiding huge SRAM and pipeline latency visible to SPELL processors. According to the HTMT model, a program consists of (coarse-grain) threads (e.g., representing parallel functions) and (medium-grain) parallel instruction streams (e.g., representing parallel loop iterations) created inside threads. Each ultrapipelined SPELL processor has 16 multistream units (MSUs), 5 pipelined floating-point units operating with an average cycle time of 15 ps, and an 8-ported pipelined CRAM with a 30 ps cycle time. The peak CRAM bandwidth is eight 64-bit words per 30-ps cycle, i.e., ~ 2 TB/s. MSUs communicate with the shared floating-point functional units and CRAM via an intra-processor interconnect (PNET).

Each MSU executes control, integer, and floating-point compare operations of up to eight parallel instruction streams. The first stream is created by MSU hardware in response to a special (?start thread?) message from SRAM PIM. Other streams can be created and terminated using "create/terminate stream" instructions whose execution requires neither involvement of the runtime system on SRAM PIMs nor allocation of any CRAM resources. All 8 parallel streams inside one MSU share: a 2-KB multi-port instruction cache, 64 general-purpose registers (each of which is able to hold either 64-bit long integer or double-precision floating-point data), a 64-bit integer arithmetic unit, a 32-bit address adder, and a PNET interface unit. All the units within MSU are pipelined and have a 15-ps cycle time (for 0.8-m m technology). Although the performance of any individual stream is limited by this 15-ps cycle (equivalent to a 66-GHz clock rate), other logic providing access to shared resources (registers and units) inside MSU can work at a much higher rate of up to 160 GHz. The hardware supports flexible partitioning of each register file into variable-size register frames assigned to instruction streams and provides relative and absolute register addressing at run-time. As a result, different instruction streams running simultaneously within the same processor can use a single copy of program code.

Communication between each SPELL/CRAM module and local SRAM is provided through a room-temperature interface with two ports (in and out) consisting of almost 1K signal and 1K ground wires and 8-10 Gb/s bandwidth per each signal wire. This gives a bandwidth of one 64-bit data (with additional bits for address and control) packet every 30 ps, i.e., ~512 GB/s in each direction. SPELL communicates with remote CRAM/SRAM modules through superconductor network (CNET) to be implemented either as a Banyan network or a multi-dimensional pruned mesh built of 2´ 2 switches with credit-based flow control. Each SPELL can send and receive a packet containing 64-bit-data to CNET each 30 ps, so the peak data bandwidth of one CNET port is ~ 256 GB/s in each direction.

We have found that the COOL system with 4,096 SPELL processors and 4 GB CRAM can achieve near-petaflops performance, while occupying a physical space of ~ 0. 6 m3 and dissipating ~400-500 Watts at 4 Kelvin (~150 KW at room temperature).

Acknowledgements

We would like to credit contributions from Dima Zinoviev, Paul Bunyk, and other members of our

SUNY team. Useful discussions with Burton Smith, Thomas Sterling, Peter Kogge, and other members of the HTMT project are gratefully acknowledged.

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Quantum 1/f Stability Optimization of Quartz Resonators, THz Generators, and other Resonant System

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The quantum 1/f theory, as applied to bulk acoustic wave (BAW) and surface acoustic wave (SAW) resonators, is compared with experimental results obtained by F.L. Walls et al., T. Parker et al., J.R. Vig et al., as well as other research groups. The theory has recently been generalized to the case of an arbitrary coherence length of the phonons, which may be large or small compared with the size of the resonator. The theory has further been extended to include defect scattering along with the phonon scattering case exclusively considered earlier.
Our recent theoretical results [1], [2] can be written in the form

S(f) = b'V/fQ4, for V3/4e, (1)
and

S(f) = b'e6/fVQ4, for V"e, (2)
where, with
<w=108/s, with n=kT/h? <w, T=300K and kT = 4 *10-21 J b' =(N/V)ah? <w/12npg2mc2 =1022(1/137)(10-27108)2/12kTp10-27 9 1020 =1. (3)
For the case of defect scattering, a two-phonon process takes place. A phonon from the main resonator mode scatters on a defect and a phonon of comparable frequency emerges into another mode with much smaller phonon occupation number nw=kT/h? w. In this case we have to replace <w by w and n<w with nw, which gives a b-value which is (<w/w)2 smaller, i.e. 104-106 times smaller. In general, therefore, writing G=G' + G", we obtain for the combined phonon and defect scattering case, in general,
b=b'[G'2 + (<w/w)2G"2]/G2. (4)

Though the defect scattering term is small at room temperature, it may become dominant at low temperatures, when the phonon scattering rate G' becomes smaller than the defect scattering rate G".
The form of Eqs.(1-4) shows that the level of 1/f frequency noise depends not only as Q-4 as previously proposed for quartz [3], but is a non-monotonous function of the volume of the active region. The noise first increases with volume, then after reaching a maximum of the order of the phonon-coherence volume, it decreases with size. For quartz, this theory fits the data of Gagnepain who varied the Q-factor with temperature in the same quartz resonator (but not frequency or volume), the data of Walls who considered several quartz resonators which differ in volume and frequency, and the data of Parker for SAW resonators, with their relatively low Q values. Indeed, according to [4], the median value of the PM noise L(10 Hz) in dBc/Hz for 12 unswept quartz resonators is -103.1, -101.6 and -97.7 for small, medium and large electrodes respectively, in reasonable agreement with the proportionality with V, which requires a 6 dB difference between the groups with large and small electrodes. The electrode diameters of the 3 size groups were 2.16 mm, 3.05 mm, and 4.32 mm. The volumes were thus approximately proportional with the numbers 4.67, 9.30 and 18.66, and therefore with the measured median values. The remaining scatter present in the data [4], [5], is analyzed in terms of the defect contributions and coherence corrections given by Eqs. (2)-(4).
The theory also predicted from first principles, with no free parameters, the stability of other resonators, generators and detectors. This included stimulated THz photon emission and absorption in resonantly enhanced, phonon-assisted tunneling between adjacent wells in MQW superlattices [6]. The quantum 1/f theory allowed optimization of the frequency stability of these THz sources and of their sideband emission. It also allowed laser-giro and maser optimizations.
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Quantum 1/f Optimization of Antennas

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It is well known that kinetic coefficients such as the electrical resistance of conductors and semiconductors exhibit quantum 1/f fluctuations caused by the quantum 1/f effect in the scattering cross sections of the current carriers. Is the radiation resistance of antennas an exception? The present paper tries to answer this question, and to suggest ways in which the quantum 1/f noise in the radiation resistance can be experimentally verified.

According to the general quantum 1/f formula [1]-[13] the spectral density of fractional fluctuations in any physical cross section or process rate G is

G-2SG(f)=2aA/f (1)

with a=e2/h? c =1/137 and A=2(DJ/ec)2/3p. This is the quantum 1/f effect in any physical scattering rate G, and J=ev is the current of the scattered particles of charge e and velocity v. The "physical" rates are defined by us to contain the quantum 1/f fluctuations in addition to the quantum mechanical expectation value. DJ denotes the current change caused by the scattering process. In the case of an antenna, the collective "scattering" process affected by quantum 1/f fluctuations is the process of radiation of one quantum of the antenna's oscillation energy quanta e=h? w. Setting

aJ = dP/dt = P* , (2)

where P is the vector of the dipole moment of the antenna of length a, we obtain for the fluctuations in the rate G of oscillation energy quanta e=h? w removal from the main antenna oscillation mode the spectral density

SG(f) = G24a(DP*)2/3fpe2c2, (3)

where (DP*)2 is the square of the dipole moment rate change associated with the process causing the radiative removal of a quantum e=h? w from the main oscillation mode. To calculate it, with Ja = dP/dt, we write the energy W of the antenna mode in the form

W ? nh? w = (1/2a2)Leff(dP/dt)2 = (1/2a2)Leff(P*)2; (4)

The factor two including the potential (capacitive) energy contribution is automatically included because we define P* here to represent precisely the amplitude of the antenna dipole moment rate of change, rather than the oscillating instantaneous value. Here Leff is the effective inductance of the antenna dipole. Applying a variation Dn=1 which corresponds to the spontaneous emission of one quantum, we get Dn/n = 2IDP* I/IP* I, or DP* =P* /2n. Solving Eq. (4) for P* and substituting, we obtain

IDP* I = (h? wa2/2nLeff)1/2 (5)

Substituting DP* into Eq. (3), we get

4a(h? w/2nLeff)/3pe2c2 G-2SG(f) = 2ah? wa2/3npc2fLeffe2 ? L/f . (6)

This result is applicable to the fluctuations in the radiative loss rate G of the antenna. The corresponding fluctuations in the resonance frequency of the antenna are given by

w-2Sw(f) = (1/4Q4)(L/f) = ah? wa2/6npc2fLeffe2Q4, (7)

where Q is the quality factor of the single-mode antenna considered. Eq. (7) implies fluctuations of the radiation resistance of the antenna, defined by

Rr =h? wG/I2;

Rr-2SRr(f) = 2ah? wa2/3npc2fLeffe2 ? L/f =[2npftw]-1=[2npfw/2g]-1= [2npfQ]-1.(8)

Here we used the attenuation coefficient g=1/2t and the antenna quality factor Q = w/2g = wt.

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Epitaxial GaN Films Grown on ZnO/GaN-Buffered Si Substrates

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Growth of GaN films on Si has been studied for many years, motivated by the unique advantages offered by Si over other substrates (primarily, the availability of low price, high quality and large-size wafers). It would also be an interesting theme to combine various functional devices that can be obtained from the wide bandgap semiconductor with the advanced silicon electronics on the same substrates. Epitaxial growth of GaN on Si has been reported by many researchers with variable success. Two major problems can be identified in pursuit of these goals. First, the quality of GaN films grown on silicon is far inferior to that of films grown on other commonly used substrates such as sapphire or silicon carbide. Second, the growth conditions that have been used for GaN on Si are not compatible with standard silicon processes (basically the growth temperature is too high).

In this work, we have investigated the use of a ZnO/GaN buffer layer structure in growing highly epitaxial GaN films on Si substrates. First, an epitaxial GaN film was grown directly on Si(111) substrates as an initial buffer layer. It has been reported that direct growth of GaN on Si(111) usually results in phase-mixtured films and therefore a proper buffer layer (such as AlN or GaAs) has been used to obtain single-phase films. It should be mentioned that our GaN films, directly grown on Si, are of a single-phase monocrystalline hexagonal structure. After this GaN layer growth, an epitaxial ZnO film was grown on the GaN-buffered Si substrate. A main GaN layer was then grown on this ZnO/GaN-buffered Si substrate. X-ray diffraction analysis shows that all the three layers (i.e., the GaN buffer, ZnO buffer and GaN main layer) are of a monocrystalline hexagonal structure with their epitaxial relationship of GaN(0001) (1120)//ZnO(0001) (1120)//GaN(0001) (1120)//Si(111). This two-layer-buffer structure offers unique advantages over other buffers reported so far (such as AlN and GaAs): good lattice match between GaN and ZnO (less than 2 % mismatch), and the controllability of electrical conductivity of ZnO and GaN films in a broad range, which will allow for more flexibility in device design. All these films were grown at temperatures of 650 - 750 oC using a plasma sputtering technique. X-ray diffraction analysis confirms a dramatic improvement in the epilayer quality of GaN films grown on the ZnO/GaN-buffered Si in comparison with that of GaN films directly grown on Si. Details of characterization results (structural, electrical, and optical) will be discussed.

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Stress-Induced Confinement of Light in GaN, GaAs and Si

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We have investigated the effects of thin-film-induced stress on the refractive indices of GaN, GaAs and Si. The stress-induced index change (i.e., primarily the photoelastic effect) is found to be significant in those semiconductors and itself can allow for strong confinement of light in the stressed region. Based on this phenomena, we have developed optical waveguides that are formed on bulk semiconductor substrates without requiring any epitaxial or separate cladding layers for vertical confinement of light. In the structures developed, vertical confinement of light is achieved via a photoelastic effect in semiconductor induced by thin-film stress, and lateral confinement is obtained by a semiconductor mesa or a photoelastic effect. We have also carried out numerical analyses on the stress distribution, dielectric constant changes, and mode profiles at 1.3 µm or 1.55 µm wavelength in GaAs or Si substrates. The simulation results clearly support the experimental results that two-dimensional confinement of light can be achieved in bulk GaAs and Si substrates using thin-film-induced stress.
In the case of GaN, we have investigated the stress-induced index change using epitaxial GaN films grown on sapphire substrates. SiO2 or Si3N4 films were deposited-as a stripe or window pattern on GaN as a stress-inducing film. The stripe or window pattern runs along the (1120) direction of a GaN(0001) film that was epitaxially grown on a c-plane sapphire substrate. The waveguide measurement result shows a clear confinement of light in the window region. This implies that the effective guide index of GaN in the window region, which is under compressive stress, is higher than that of the outer region, and suggests that the amount of stress-induced index change overcompensates the negative loading effect of the stressor layer. The photoelastic coefficients of GaN were estimated from this measurement result. The stress-induced confinement of light is promising as a simple and economical method for forming optical waveguides without requiring etching of GaN. Details of the measurement result will be compared with the simulation results.

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Ferroelectric Nonvolatile Memory Field-Effect-Transistors Based on a Novel Buffer Layer Structure

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A ferroelectric field-effect transistor (FEFET) consists of an FET whose gate dielectric is comprised of a ferroelectric material or a stack of dielectrics with a ferroelectric layer. The application of a voltage pulse to the gate sets the direction of the ferroelectric polarization. The polarization direction controls the electrical conductance of a channel under the ferroelectric, and this can be used for nonvolatile memory devices that allow for nondestructive readout operation. Although the FEFETs offer such a unique advantage (i.e., the simplicity of its structure and operation) over the conventional approach (i.e., a structure that has a ferroelectric storage capacitor connected to a pass-gate transistor), there has been no report of realization of commercially viable FEFETs. This is attributed to the various issues related to the structure, material, and/or fabrication processes that have been investigated so far, and a major issue being the difficulty of growing electrically switchable ferroelectric films on Si substrates with good interface/channel properties and long retention time.

We report FEFET memory devices that incorporate a thin, magnesium oxide (MgO) buffer layer between a ferroelectric layer and an oxidized silicon substrate. The idea of using this two-layer-buffer structure (i.e., MgO/SiO2) for a ferroelectric gate is based on the following reasons. First, it was found that most ferroelectric films can be grown highly oriented on MgO-buffered oxidized silicon substrates. Second, MgO has been widely used as a diffusion barrier for various materials systems, because of its refractory nature. The use of a MgO buffer, therefore, is expected to result in protecting the silicon FET channel region from interdiffusion or reaction with a ferroelectric layer during device processing. Third, thermal oxidation of Si has been known to be one of the best ways of passivating silicon surfaces. Therefore, the use of a (thermally grown) SiO2 buffer in conjunction with a MgO buffer will allow us to produce (and keep) FET channels of good quality.

The proposed memory devices were successfully fabricated on the MgO/SiO2-buffered Si substrates with major ferroelectric films such as Pb(Zr,Ti)O3 and BaTiO3. The fabricated devices show excellent performance in ferroelectric polarization switching and memory retention, and demonstrate the scalability in device dimension and operation voltage, i.e., the devices are suitable for low voltage operation (i.e., 3 - 5 V or below) showing a sufficient memory window (1 - 2 V). The on-state channel current was found to reach a steady state after an initial, slight reduction (less than 5 percent) during the first one or two days. The off-state channel current does not show any noticeable change during this period. Retention tests over longer periods (over several weeks) were also carried out and no further degradation was detected. Regarding the fatigue of our ferroelectric films, the films do not show any noticeable degradation even after 1012 cycles of polarization switching.

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A Stenographic Character Recognition Algorithm in Neural Networks

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In this paper, we would study the application possibility of neural networks to the recognition process of stenographic character, applying the classification function, which is the greatest merit of those of neural networks applied to the various parts so far, to the stenographic character recognition which is relatively simple classification work. Stenographic character recognition algorithms, which recognize the characters by using some methods, have a quantitative problem that while its structure is simple, a lot of basic characters are impossible to classify into a type and qualitative one that it is not easy to classify characters for the delicacy of the character forms. In this paper, it performs a recognition of basic 126 characters and after preprocessing to the stenographic character input first, it performs learning, extracting 104 DC component and inputting them to the neural networks. The character learning outputs the character whose degree of the similarity is the highest of all, compared with the standard pattern.

Character image data which performed preprocessing procedure perform a feature extraction appropriate to the neural networks learning. That is, it exacts total 104 input DC elements considered to include data of stenographic character to some extent not to use binary data of 26 X 26 pixel into input directly. The research of using such an algorithms is that we can reduce node numbers in the middle layer more than when we use 26 X 26 pixel into input as it is, therefore we can reduce training time greatly and besides the input data, after feature extraction, can be more effective than original 26 X 26 image data in representing a feature of stenographic character. This algorithms, which had been ever applied to dynamic character like Korean languages, is considered to have more powerful effect in recognizing stenographic characters, than in the dynamic characters, to represent the core of recognition as only DC elements being extracted in the angle of four direction.

In this paper, after searching the present situation of the general research in the characters recognition by neural networks and the background of stenographic character recognition, we present the recognition system of stenographic characters by using EBP neural networks which is one of representative neural network modes. Even though this is the result of experiment under the limited environment of the basic characters, this shows the possibility that the stenographic characters can be recognized effectively by neural network system. In this system, we got 95.86% recognition rate as an average.

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Robust Recognition of the Il-Pa Stenographic Character Images by Using Neural Networks

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In this paper, we would study the application possibility of neural networks to the recognition process of stenographic character image, applying the classification function, which is the greatest merit of those of neural networks applied to the various parts so far, to the stenographic character recognition which is relatively simple classification work.
Stenographic recognition algorithms, which recognize the characters by using some methods, have a quantitative problem that while its structure is simple, a lot of basic characters are impossible to classify into a type and qualitative one that it is not easy to classify characters for the delicacy of the character forms. Even though this is the result of experiment under the limited environment of the basic characters, this shows the possibility that the stenographic characters can be recognized effectively by neural network system. In this system, we got 90.86% recognition rate as an average.

1. INTRODUCTION

As we are living in the information age in which much information is deluged, we need to develop the ability to process much information quickly. Here, the media which are able to record, keep, and process every information are essential to the information age, however media held in common by both human and machine are not numerous so much. So operative work input by keyboard may be an obstacle to promote informationalization, but it must be essential work. In selecting the way held in common by both human and machine, if it is obviously impossible to make human read disks or tapes which are exclusive for machine, it will be far easy and appropriate to make machine read printing media exclusive for human. In this meaning, it is very important task to make a computer recognize character automatically. Also neural networks, analyzing the structure of human brain as an human intellect scientific approaching way, making clear the mechanism of that process and making a computer which has a structure like it is appeared as calculation paradigm and researched for over the last 40 years to imitate the human ability image recognition part [1]. Neural network has powerful classification function and recognition ability in addition that it has the simplicity in structure, and it is expected to present a new way as a parallel data preprocessing system of "all-at-once" way in the part where the existing computer of Von Neuman pattern does not fulfill its function [2], [3], [4].
So recently the research carrying out character recognition by neural networks with powerful pattern recognition ability and fault tolerance is in progress actively. Human is able to recognize character easily but if performing this by using the present computer system, it will be very complicated exorbitantly, therefore the research area of character recognition like this is a typical example to make good use of a merit of neural network. The good results of research by neural networks with an object to English characters, figures, Japanese KANA characters were not only published abroad but also in the practicalization state and it was reported to achieve high recognized rate over 98% by neural networks in printed Hangul Korean character recognition in Korea [1].

2. THE PURPOSE OF RESEARCH AND EXPECTED EFFECT

Recently the research to the development in the device of character recognition to process many documents automatically according to the information socialization is in progress actively. Also the neural networks which have a powerful function of pattern classification as a model for an artificial realization of human brain, overcoming the limit in the structure of the present computer are in the limelight [5]. Clustering or pattern recognition is defined as classifying data sets into each class according to the degree of similarity. One of the pattern recognition is the character recognition, whose methods are a template matching method, a statistical method and a structural method [6]. However a template matching method has a problem in selecting a special template for the variety of character form and a statistical method in the recognition of characters whose space between consonants and vowels is delicate, and a structural method in forming structural rule of character recognition. Recently the way by using neural networks model in character recognition is used a lot as a way of solving these problems [1]. Among some researches by neural networks, various methods in the Hangul Korean character recognition are developed as mentioned above, and it is almost in the practicalization state, but it is necessary to develop many algorithms for improvement of recognized rate in case of hand written style recognition. Also there are some researches in progress in the application part for the necessity, which are car number recognition, zip code recognition and etc., but there is not any research in the steno-

graphic character recognition except some cases [7], [8]. In this paper we would study the application possibility of neural networks to the recognition process of stenographic character image, applying the classification function, which is the greatest merit of those of neural networks applied to the various parts so far, to the stenographic character recognition which is relatively simple classification work.
Stenographic recognition algorithms, which recognize the characters by using some methods, have a quantitative problem that while its structure is simple, a lot of basic characters are impossible to classify into a type and qualitative one that it is not easy to classify characters for the delicacy of the character forms. In this paper, it performs a recognition of basic 126 characters and after preprocessing to the stenographic character input first, it performs learning, extracting 104 DC component and inputting them to the neural networks [9]. The character learning outputs the character whose degree of the similarity is the highest of all, compared with the standard pattern.

3. AN OUTLINE OF RECOGNITION SYSTEM

The whole process of character recognition is shown as the Figure 1. Character image input by scanner is represented as 26 X 26 character image through binary process. A 26 X 26 character image deletes a noise and an isolated pixel due to the fallacy of input system, performing smoothing procedure. And then after extracting a feature of target character through feature extraction procedure, the system uses these features as neural network input data and recognizes the target character through neural networks learning.

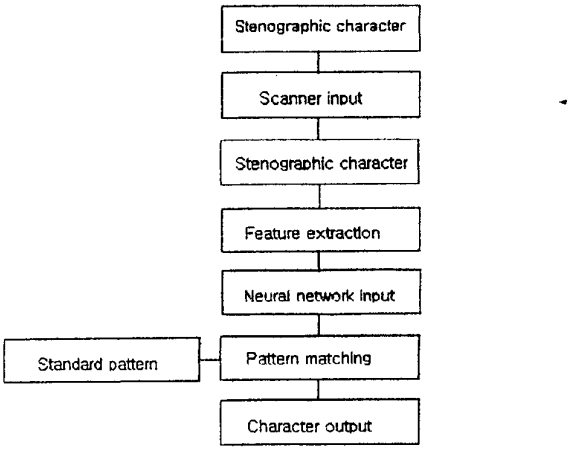

Fig. 1 Processing Procedure of Character Recognition

3-1. The Procedure of Preprocessing

The binary character image input by scanner is not able to extract feature correctly for an isolated pixel and a noise of hole or convex. It is because neural networks would be disturbed in case of such a data being made to learn a neural network as it is. Therefore it performs smoothing as a preprocessing procedure.
The original purpose of neural networks is to make neural networks recognize in the environment identical with visual data of human, so we make it a rule to preprocess input data as little as possible[10]. Therefore thinning procedure is skipped because it is considered not to affect the recognized rate or the decrease of general data number. Additionally pattern normalization as a process of input pattern is not performed, because the characteristics of stenography are considered to lose its function as a character with data in case of the change character's size and the degree of bias.
Simple smoothing methods to delete noise are a spatial filter, a nonlinear filter, a median filter and a frequency filter[9]. In this paper median filter to represent various functions, not taking a long process time. Arranging the intensity of each pixel in 3 X 3 mask in an order of size with some spot (i, j) in the center as following figure 2, we substitute the intensity located in the center for a new one of (x, y) pixel. This is shown as the following formula (1)

(i-1, j-1) (i, j-1) (I+1, j-1)
(i-1, j) (i, j) (I+1, j)
(i-1, j+1) (i, j+1) (I+1, j+1)

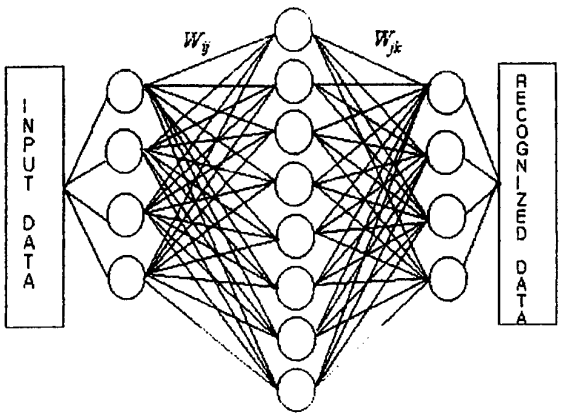

Fig. 2 3 X 3 Mask Performing Smoothing Operation

f(i, j) = g (i, j) ? M (i,j) (1)
Only, M (i,j) = 1 1 1
1 1 1
1 1 1
We use 12 masks of thin-line preservation to prevent the thin lines are not preserved, which is the problem of multi-logical smoothing as mentioned above. The following figure 3 shows the mask for a thin-line pattern confirming.

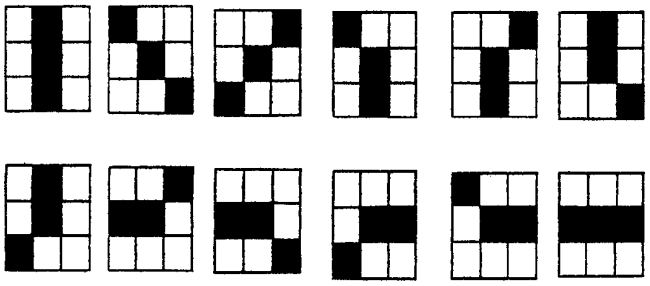

Fig. 3 12 Thin Line Preservation Masks
This filter is very effective to preserve the change of intensity observed in the end of the character, deleting noise, not losing the sharpness of original image at the same time [11].

3-2. The Procedure of Extracting Feature
Character image data which performed preprocessing procedure perform a feature extraction appropriate to the neural networks learning. That is, it exacts total 104 input DC elements [9] considered to include data of stenographic character to some extent not to use binary data of 26 X 26 pixel into input directly.
The research of using such an algorithms is that we can reduce node numbers in the middle layer more than when we use 26 X 26 pixel into input as it is, therefore we can reduce training time greatly and besides the input data, after feature extraction, can be more effective than original 26 X 26 image data in representing a feature of stenographic character. This algorithms, which had been ever applied to dynamic character like Hangul, is considered to have more powerful effect in recognizing stenographic characters [12], than in the dynamic characters, to represent the core of recognition as only DC elements being extracted in the angle of four direction.

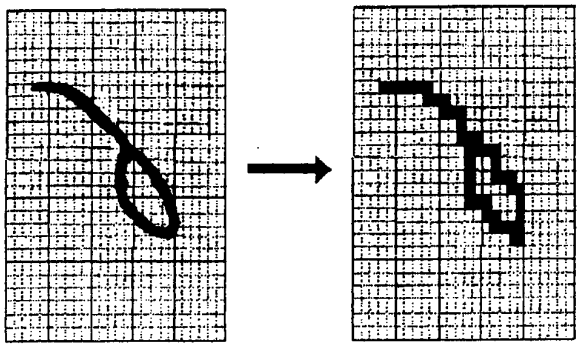

Fig. 4 The Example of DC Element Extraction for Stenographic Character " RU "

Figure 4, one of 104 DC element extraction procedures, shows the relative size of 104 DC elements for stenographic character " RU ". 104 data produced thus extract DC elements of 0, 45, 90, 135 direction, if actually we try to do a second-dimension FFT with special characters, we confirm DC elements to form a feature of that character[13]. DC element values are obtained through this procedure being integer values from 0 to 26 and we divided a value into 26 and normalized from 0.00 to 1.00 value to get a real input value.

3-3. Neural Networks

Neural Networks used in this paper is Feed-forward style network as a structure of multi-layer networks with one hidden-layer including input and output layer and the signal in each layer is toward only to the upper layer as following 5. Each node is set by the product sum of the output and the weight in the lower node, which is output to the upper layer by sigmoid function with the characteristic of non-linear asymmetric increase [2], [4], [14], [15].

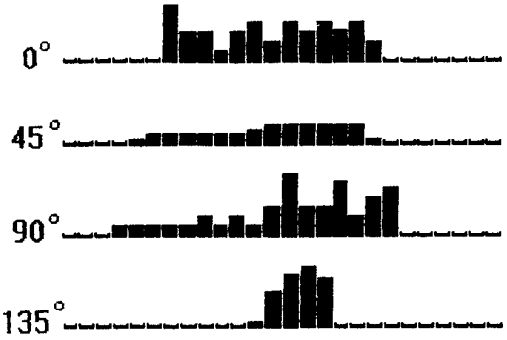

Fig. 5 Feed-forward Neural Networks

BEP(Back Error Propagation) learning way of generalized data rule is used in neural networks learning. This is shown as follows in brief. Delta rule which represents learning procedure is

?pWji =?(tpj - Opj) ipi =??pj ipi (1)

In case of error Ep being defined as formula 2, Delta rule of formula (1) becomes the gradient descent algorithm [14] in the spatial domain of weight error.

Ep = 1/2 ?(tpj - Opj)2 (2)

We could obtain a proportioned relation as formula (3) between the change in a degree of weight ?pWji and the differential value of error.

?Ep

?pWji ? -

(3)

?Wji

To apply the above formula (2) to the multi-layer networks, the differential value to the weight of error must be calculated. If total input value of node j is netpj, this is shown as follows (4). netpj = ?Wji Opi + bias j (4)

When the output value of node j, activation function is f j is shown as following formula (5).

Opi = f j(netpj) (5)

Differential calculus of error is shown as follow by the Chain rule.

?Ep ?Ep ?netpj

= ? (6)
?Wji ?netpj ?Wji
The result of second calculation among two differential calculus formulas appeared in the left side of formula (6) is shown as output value of node i like formula (7).
?netpj ?
= ?Wjk Opk = Opi (7)
?Wji ?Wji
If we define ?pj as formula (8).
?Ep
?pj = - (8)
?netpj
Thus formula (8) is considered to be associated with formula (1), hereupon ?pj is, when j is a node belonging to the output layer, is represented as formula (9) and when j is one belonging to the hidden layer, as formula (10).
?pj = (tpj - Opj) f j(netpj) (9)
?pj = f j(netpj) ??pj Wkj (10)
Using a linear function as an activation function, it is possible to transform multi-layer into single-layer of equal value, therefore we could not make good use of the merit of multi-layer. So nonlinear function as an activation function is used. Also activation function must be a sigmoid function possible to differentiate for it is necessary to differentiate in the procedure of calculating ?pj.
The characteristic of using the sigmoid function are that first, it is possible to estimate a result for output is represented as value between 0 and 1, second, differential calculus is possible and the pattern of result is very simple, thereof easy to obtain transition function for each connected line. And third, with the function of automatical gain control, when input value is small, it changes greatly, and when input value large, it changes a little [14], [15], [17]. Actually the formula used in realization is represented as follows.
?Wji(n+1) = ??pj ipi + ??Wji(n) (11)
?bias j(n+1) = ??j + ??bias j(n) (12)
Hereupon, the parameter ? is the learning rate and ? is the momentum. Controlling learning rate and momentum, we could reach the global minima effectively, reducing learning time. Also bias formula is changed as formula (12).
In this paper, learning rate 0.45 and momentum 0.7 are used and the one chooses the value used frequently in BEP algorithms, while the other chooses the optimal value within the scope of vibration not being produced through the procedure of recognition experiment.

3-4. Stenographic Character
Stenography was studied first in Rome in about BC 63, and in the country Korean style stenographic way called " the stenographic way of Cho-sun language" originated first in 1909. But the research of stenography had been almost discontinued by the Korean-Japanese annexation, after Liberation, it has been developed and pervaded as various stenography rule, passing by the transformation of various pattern. The stenographic marks are composed of a straight line, a curved one and a spot, which contain a peculiar character data in accordance with the size and the direction. Stenographic character of Il-pa style, recognition object in this paper, forms a basic frame as figure 6, which each stroke as a petal represents one character. For the characteristic of stenographic character, the length and the angle of one character should follow a regular rule. That is, the initial sound is classified into each character in accordance with the angle of stroke and its kind that is curved or straight line. The middle sound except fold vowels is classified into each character in accordance with the length of the stroke (0.5cm, 1cm, 1.5cm) and the circle size included in the stroke. Also, fold vowels and final sounds are formed in accordance with the position in which a spot and 2mm brush is added and the direction of brush specify the character feature.

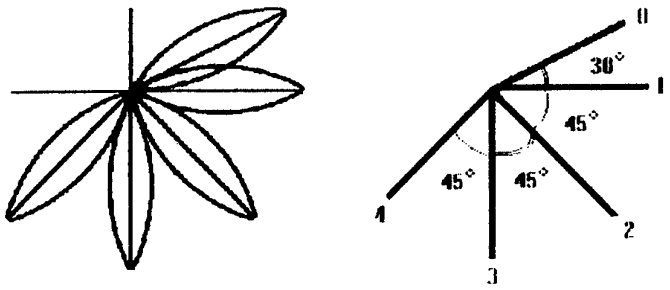

Fig. 6 The Basic Form of Stenographic Character

Among 126 representative stenographic characters, the above figure 7 represents 84 characters patterns except 42 ones of "?" line characters, "?" line characters and "?" line characters. Here, we write "?" line characters to the middle of stenographic mark with setting a circle of "?" line character apart about 45 degrees, "?" line characters with the 15mm size of "?" line characters and "?" line characters with the double size of "?" line characters in figure 8.

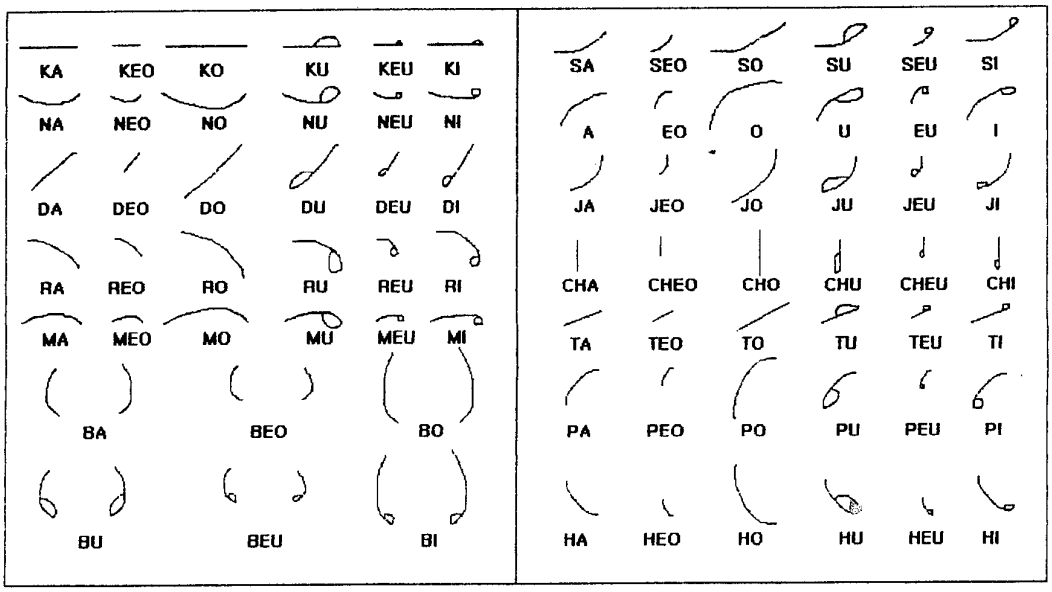

Fig. 7 The Representative Stenographic Characters

Fig. 8 "?" Line Character Image : The Example of the Character "Kae"

4. THE RESULT AND ANALYSIS OF EXPERIMENT

In this paper, after modifying character image input by scanner with 600 DPI of 300 pixel per inch by using Global Lab image board in the aspect of IBM/PC-586, we performed a recognition experiment by neural networks embodied as "C" language.
As an input of the system we used stenographic characters from which we selected 126 basic characters used basically most in the list on the actual condition of Hangul frequency published by the department of Education in 1955 and they were written by 5 non-specialist to whom we requested in accordance with the stenographic grammar.
Data of input character are distributed and input in 104 input layer nodes and hidden layer node is made to obtain optimum node number, being changed and experimented many times. Figure 9 shows the relation of recognized rate and the learning time when we make hidden layer number increase.

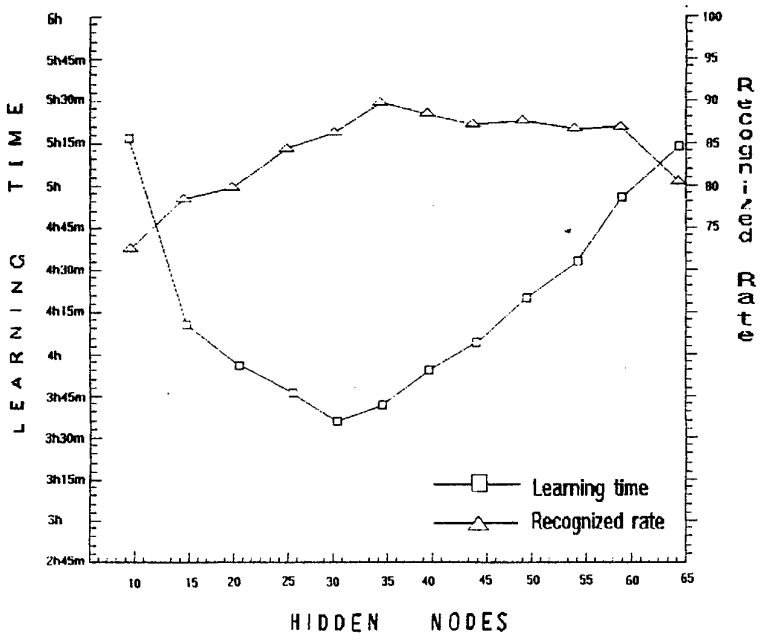

Fig. 9 The Recognized Rate and Learning Time in Accordance with Node Number of Hidden Layer

Figure 9 shows that recognized rate does not get higher any more over a certain node number. Also the node numbers in hidden layer of neural networks are very associated with one of input or output layer and treated as a parallel processing so learning time is reduced somewhat, however it is analyzed that learning time increases when exceeding a proper node number. 378 characters by 3 persons among 630 characters written by 5 persons are used in the learning procedure and the rest characters which are not used in learning procedure are used in our experiment. Output node sets are coded to 7, because 126 stenographic characters represent properly. As a result of our experiment, the recognized rate of each consonant and vowel is represented in table 1.

Table 1 Each Consonant Recognized Rate for Each 6 Line Character
The examples of representative fault-recognition which recognition are not performed correctly, one of which is to recognize " ?, ?, ? " characters of " ?, ?, ? " line characters as " ?, ?, ? " characters, which means that the recognition about a delicate angle difference is not achieved because the data of the initial point and the last one is not known for the characteristic of off-line.

5. CONCLUSIONS

In this paper, after searching the present situation of the general research in the characters recognition by neural networks and the background of stenographic character recognition, we present the recognition system of stenographic characters by using BEP neural networks which is one of representative neural network modes. Even though this is the result of experiment under the limited environment of the basic characters, this shows the possibility that the stenographic characters can be recognized

effectively by neural network system. To practice this system, it should be able to make fold vowels, finals, connected typing and sentence omission besides basic character recognize and also we expected to achieve a lot if applying the additional algorithms to this work in accomplishing classification working in the general image. Therefore now the research of the supplement of algorithms and the reduction of fault-recognized rate or the improvement of the learning speed of BEP should be achieved simultaneously and first of all the unity of stenography style should be preceded.

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Migrating to Submicron Display Technology: Schottky Source/Drain Thin Film Transistor

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High performance, system-integrated poly-Si TFTs are required for high resolution LCD and OLED display [1]. In such displays, micron sized transistors are required to achieve good aperture ratios. There are at least two concerns in shrinking the TFTs.

The first concern in fabricating small poly-Si transistors is that as channel length shrinks to dimensions comparable to grain size, increased fluctuations in the electrical performance are expected. To reduce these fluctuations, several techniques have been reported, e.g. controlling of the morphology and location of grain boundaries in the channel via masked laser annealing [2] or removing grain boundaries altogether from the active region through seeding grains in controlled locations [3].

The second concern and also a fundamental problem is that similar to MOSFETs, short channel effects are expected to occur in micron sized poly-Si transistors. Empirically, it is found that the onset of short channel effects scales with the triple product of junction depth, gate insulator thickness, and the squared sum of the depletion layer width at source and drain [4]. This last factor is large in poly-Si thin film transistors, which typically use undoped channels.

The use of Schottky contacts on source and drain renders the junction depth, effectively, zero and thus minimizes short channel effects. Comparable shallow junctions would be difficult to fabricate via doping, since at low temperatures dopant move preferentially along grain boundaries.

Schottky source and drain, S-S/D, MOSFETs [5] have several additional advantages over conventional diffusion source and drain transistors including a simple, low cost process, low source and drain sheet resistance, immunity to latchup and superior scalability to submicron dimensions. However, S-S/D devices have lower on-currents and larger leakage current especially if the device is operated at room temperature.

Recently, Snyder el al [6], using single crystal Si, attempted to increase the on-current by using a self-aligned process, and achieved on-currents comparable to those of conventional TFTs. Nevertheless, their devices still exhibited a high leakage current when operated at room temperature. Hattori et al [7] simulated the electrical performance of S-S/D poly-Si channel Thin Film Transistors. This simulation showed that it should be possible to build devices with a very low leakage current. However, no experimental data have been reported to date for poly-Si S-S/D TFTs.

We fabricated self-aligned S-S/D TFTs using nickel-induced lateral crystallization, MILC, to form the channel [8,9,10,11]. The fabrication used a three-mask, low temperature, glass-substrate compatible, self-aligned fabrication process.

The devices, tested at room temperature, exhibited normal TFT I-V characteristics. The leakage current of 7*10-10 Amp per micron gate width prior to hydrogenation was similar to that measured in conventional poly-Si TFTs, but the on-current was a factor 10 lower.

The devices fabricated to date have gate lengths from 5um to 30um. To investigate scaling to smaller dimensions, we are now fabricating TFTs with a gate length down to 0.25 um and below. In addition, we are attempting to fabricate MILC-TFTs in which the location of the grain boundary is controlled. We will report on the results of both efforts at the meeting.

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Reduction of Coupling Noise in Data-Line Arrays

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The continuos drive to increase the density of integration necessitates among others the scaling down of the pitch of data-line arrays, e.g. the pitch of bit-lines (BL) and word-lines (WL) in DRAMs. A scaled down pitch, however, increases the coupling capacity between data-lines and increases therefore the induction of spurious signals - or noise - in those lines, which are adjacent to one, that carries a signal. This problem has been well recognized and, in order to overcome it for BL arrays, several line-twisting techniques have been proposed. In particular, one method (1) is presently utilized to suppress inter-BL coupling noise by twisting BLpais (TBL). This method, however, does not at all reduce intra-BLpair noise, which in memories of Gbit-density is more dominant than the inter-BL noise. Furthermore, additional chip-area is needed for at least four twists and four dummy cells - thus reducing the area that was gained due to the smaller pitch.

We propose a novel method for twisting multiple BL-pairs (MTBL) that is superior to all previously proposed methods (2). In particular, it alleviates both inter-BL and intra-BL noise and needs a smaller additional area for twisting when compared to the conventional TBL method (3). Our method can also be extended to WL arrays (4).

The advantage that our method of twisting data lines has, was explored by HSPICE simulations and it was validated by soft-error rate measurements on appropriately fabricated test chips. DRAM test chips with different BL pitches were designed and fabricated utilizing both the conventional TBL and our proposed MTBL schemes. Each test chip was comprised of a 256-Mbit memory array with non-COB type stacked capacitor memory cells. BLs are made of polycide and another layer of polycide is used for the crossing portion in the BL twisting area. BL layer thickness is also varied according to the BL pitch to implement the exact ratio of the coupling capacitance to the total BL capacitance for each DRAM generation. For example, BL layer thicknesses of 0.18-um (256-Mbit DRAM) and 0.14-um (1-Gbit DRAM) are used for the BL pitch of 0.6-um and 0.28-um, respectively.

At the 1-Gbit level of integration, in our MTBL scheme - compared to the conventional TBL scheme - the chip area penalty due to twisting is reduced from 6.5% to 2.3% and the BL coupling noise is reduced by 45%. At the 256-Mbit level, when the proposed technique is applied to both the BL and WL structures, we achieved a 64% coupling noise reduction compared to the conventional TBL and WL schemes. Faster data access time can also be expected when the proposed technique is applied to BL and/or WL structures.

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Scalability of SOI into future deep submicron CMOS technology

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Scalability of SOI into deep submicron CMOS technology is discussed. Issues that are unique to SOI such as saturated threshold voltage lowering and ac switching characteristics, and their relations to technology scaling, will also be discussed. We will show that as the technology is scaled to high performance and lower operating voltage, SOI maintains its advantage over comparable bulk technology. A design point for 0.13 um SOI technology is presented to show the SOI advantages. Using the same off-current criteria, it is shown that SOI have 25% faster inverter and 40% faster NAND compared to bulk technology. Also for the comparable speed, SOI offers 50% power savings compared to the bulk technology.

Long Wavelength (1.3 µm) Quantum Dot Vertical Cavity Surface Emitting Lasers Grown Directly on GaAs Substrates

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We have designed, grown, fabricated, and characterized vertical cavity surface emitting lasers (VCSELs) containing quantum dot (QD) active regions. Our VCSELs are grown directly on GaAs (100) substrates and contain AlAs-GaAs and AlO-GaAs distributed Bragg reflectors (DBRs). They are the first GaAs-based VCSELs to emit near 1.3 µm.

Future generations of optical interconnect, switching, and optical processing systems will require large and dense monolithic arrays of efficient, ultra-low threshold current VCSELs. Ultra-low threshold currents

in the nano-Ampere range are necessary to reduce heat dissipation and cross talk in large 2D arrays, as well as to increase the modulation bandwidth of the devices. Long wavelength (1.3 µm and 1.55 µm) VCSELs could potentially serve as low-cost and high-performance light sources for long-haul networks, as well as for high-speed optical data links. However, the performance of today's long wavelength VCSELs still lags behind that of their shorter wavelength (0.85 and 0.98 µm) counterparts. In fact, a severe problem for long wavelength VCSELs is the lack of suitable lattice-matched DBRs. For example, mirrors composed of InGaAsP/InP layers have a small index contrast and rather poor thermal properties as compared to GaAs/AlAs mirrors. For emission at 1.3 µm, an InGaAsP/InP Bragg mirror with 50 or more periods is

required to achieve the mirror reflectivity required for lasing. Although it is possible to construct long wavelength VCSELs by fusing AlGaAs DBRs to an InGaAsP active region, the fabrication process is complicated and the overall device efficiency remains poor.

A promising approach for the realization of high efficiency, long wavelength VCSELs is the use of QDs as the active gain media [1]. Quantum dots provide the ultimate limit of size quantization in solids. Their quasi-delta function density of states and strong confinement of electron and hole wavefunctions results in increased exciton oscillator strength and ultra-high material gain and differential gain. In theory, QD lasers should have the lowest threshold current densities and highest temperature stabilities. Quantum dots composed of InAs or InGaAs surrounded by GaAs or AlGaAs, and grown directly on (100) oriented GaAs substrates can emit in the range 0.8 to 1.8 µm [2]. In contrast, InGaAs quantum wells are limited to about 1.1 µm. Quantum dot edge-emitting lasers with room temperature (RT), continuous wave emission at 1.2 µm have recently been demonstrated [3]. In parallel, we have now developed and demonstrated RT VCSELs grown directly on GaAs substrates that emit at wavelengths up to 1.3 µm.

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MOVPE Growth, Piezoelectric and Optical Properties of Strained <111 -Oriented InyGa1-yAs/AlxGa1-xAs MQWs and their Possible Application to Optoelectronic Devices

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The growth of compound semiconductor structures oriented in the <111 crystallographic directions has received increasing attention due to the special properties of these structures, particularly for strained Quantum Well (QW) structures. The presence of a Piezoelectric (PE) field inside the QWs and an opposite field in the barriers provide additional parameters to engineer the potential profile of the QWs and the drift field in the barrier regions. Thus, the PE field alters the optical and transport properties of both electrons and holes. In addition, the strain in the well regions modifies substantially the confined energies and effective masses of the heavy and light hole states and the split-off valence band states. We have recently reported the achievement of very high quality GaAs/AlGaAs MQW structures grown by MOVPE on (111)A oriented substrates [1]. In this paper we report on the piezoelectric and optical properties of the first strained InGaAs/GaAs and InGaAs/AlGaAs QW structures grown on (111)A substrates by MOVPE. This advance in the fabrication and physics of <111 strained QW structures opens new possibilities for their incorporation in various devices. The application of such QW structures exploiting the piezoelectric effect for novel optoelectronic devices will be discussed.

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Wide-Angle, Low-Loss Y-Branch Waveguide for Integrated Optics

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A new wide-angle, low-loss, symmetrical Y-branch waveguide is proposed and verified using beam propagation method (BPM) and optical beam shape measurements. The waveguide configuration utilized GaAs-AlGaAs multiple quantum well (MQW) ribs for lateral confinement in the planar guiding region underneath. This Y-branch structure was fabricated easily without any additional process step. Together with utilization of the multi-mode interference effect, a local decrease of the waveguide ridge in the wedge part of the Y-branch reduces the radiation loss. The design of the Y-branch lead us to expect a radiation loss of 2.2 dB at a branch angle of 6(with the index difference ((n/n) as small as 7.1 (10-4 at a wavelength of 870 nm in the TE fundamental mode. The actual measurement indicated a loss of 3.9 dB. This value has to be compared with the expected loss in a conventional Y-branch, which amounts to 12.6 dB. The proposed method yields corresponding advantages for waveguide designs with higher (n/n ratio and can also be adapted in combination with S-branch designs.

Branching of waveguides is essential in integrated optics. It is used in power dividers/combiners in modulators, switches, interferometric devices, and semiconductor laser arrays. Both geometrical size and radiation loss of optical waveguide devices are critically determined by the bend and branch requirements. Therefore, design and realization of compact and low-loss branches are of great interest in integrated optics applications.

Conventional single mode Y-branches are widely used because of the simplicity of their fabrication. However, they suffer severe radiation losses in excess of 3 dB at branch angles greater than 2((3(resulting in poor device performance in contrast ratio and cross talk. Consequently, proper separation of the interacting waveguide arms demands very long dimensions with these narrow branch angles. On the other hand, compact Y-branches, which are necessary for high-density integrated optics, incur unacceptable losses.

Previously we proposed and evaluated a novel Y-branch rib-waveguide structure using two different numerical approaches (1). Our innovation utilizes simultaneously the multi-mode interference effect to convert the input single-mode to a double-mode near the Y-branch region and the refraction of electromagnetic plane waves, which are obliquely incident upon a planar interface between two dielectric regions, by means of a refractive index change at the Y-junction area, which in turn is caused by a local decrease of the waveguide ridge.

Now we compare the expected results with our actual experimental results for branching angles of 4, 6 and 7 degrees and for conventional and our innovative branching structures.

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Novel AlGaN-based UV photodetectors bridge biology and electronics

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In the recent years, the depletion of the stratospheric ozone layer has alerted the scientific community about the risks of a solar ultraviolet (UV) radiation overexposure. Biological and medical research have confirmed the very important role of the UV-B (320-280 nm) and UV-A (400-320 nm) bands on the Earth biosystem, and on human health. The biological action of the solar UV radiation has a strong dependence with the wavelength. The details of such biological damage function depend on the specific biological process being studied (erythema or skin-sunburn, DNA damage, plant damage, germicidal effects, bacteria killing, skin cancer, etc.). There are also well known cases where the UV exposure produces very beneficial effects (UV therapy, vitamin D production, etc.), and again these positive UV effects are wavelength dependent.

It is thus very important to assess the biological and medical effects of the UV radiation by using accurate, low cost UV detectors. The required bio-UV detector should have a spectral response to match the selected action spectrum. Until now, action fitting has been pursued by using low gap semiconductor detectors and by inserting optical filters and phosphor layers in the optical path. This approach implies filter solarization, temperature and stability effects, and bulky an expensive solar UV detector heads.

Recently, it has been recognized that AlGaN-based photodetectors are excellent candidates for the detection of the UV radiation (3.5 eV to 6.2 eV range). In this paper it will be shown that AlGaN-based UV photodetectors for biomedical and environmental applications can be fabricated. AlGaN alloys were grown on sapphire substrates by low-pressure metalorganic vapor phase epitaxy at CRHEA-CNRS (Valbonne), and on [111] Si substrates by gas-source molecular beam epitaxy (Madrid).

Because of its practical importance for human beings, the erythema (skin sunburning) action has been extensively studied (three exponential segments), and we will take this response to illustrate our approach. This erythema biological action is fitted by selecting the proper Al mole fraction, and absorption slope and tail. The below-the-gap spectral response is now quite important. Al0.34Ga0.66N photodiodes show a very good approximation to the erythema response. Besides, GaN/AlGaN photodiode arrays, with different Al mole fractions, can be fabricated and weighted electronically to fit practically any UV biological action weight function. These novel AlGaN UV detectors will help to conduct biomedical and environmental research on the action of the solar UV radiation on living species.

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MONTE CARLO SIMULATION OF IMPACT IONIZATION AND LIGHT EMISSION IN PSEUDOMORPHIC HEMT's

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We have developed a Monte Carlo code to simulate hot carrier effects in pseudomorphic high electron mobility transistors (PM-HEMT).
We show that, under bias conditions close to the breakdown of the device, there is generation of holes due to impact ionization processes. Such phenomena occur under the gate and close to the gate-drain region.
We show that, under bias conditions close to the breakdown of the device, there is generation of holes due to impact ionization processes. Such phenomena occur under the gate and close to the gate-source region. The generated hole radiatively recombine with electrons (electroluminescence) in the gate-source region. In order to calculate the HEMT electroluminescence we have developed a self-consistent tight-binding approach.[1] This allows us to describe electronic and optical properties of nanostructured devices beyond the usual envelope function approximation and to account for strain, band non-parabolicity, and indirect band gap at the same time. Optical properties within the tight-binding approach are obtained by using a recent developed theory which allows to calculate those properties without introducing new fitting parameters.
By using the distribution function as obtained by the MC simulation and the TB calculation we are able to calculate the electroluminescence spectra of the HEMT and to show how the bias induced bending of the quantum well forming the channel allows radiative recombinations of electrons and holes even from levels normally forbidden under flat band condition. The calculated electroluminescence agree well with experimental data. Furthermore, we observe that the emitted light is mainly polarized in the in-plane direction since the levels have essentially a heavy-hole character.
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SPM-Assisted Nanofabrication for Nanoelectronics

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The techniques of nanofabrication based on the use of Scanning Probe Microscopes (STM,AFM) are presented.
The first one is related to the bottom-up technology and consists in direct patterning by local decomposition of a gaseous compound under the tip of a scanning tunnel microscope. The technique does not require UHV environment and allows the deposition of metallic nanowires and dots as small as 2 nm and separated by less than 2 nm which fits the requierments for fabrication of Single Electron Transistors working at room temperature.
The second one is up-bottom technology and consists in local oxidation of silicon or metallic layers by an AFM. In the case of H-passivated Si the oxide patterns serve as masks for the pattern transfer into the substrate by selective etching. In the case of thin metallic films (Ti, Nb) the oxide is formed on whole thickness of the film and serves to isolate the structures and to create the tunnel junctions.
The electrical characteristics of nanoFET fabricated on SOI and of a quantum point contact on Nb films are presented.

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Automated Internet Measurement Laboratory AIM-Lab

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The emergence of the Internet as a recognized medium of the information exchange has opened up new opportunities for remote operation of electronic equipment and for sharing not only data or text but also samples over the WEB. Remote-distance interactive learning is another important emerging trend. The Internet is an ideal medium for remote instruction purposes. Its ubiquity and protocol standards make data communication and front-end graphical user interfaces (GUIs) easy to implement. The use of the Internet in remote education can be greatly enhanced by adding an experimental component, i.e., running experiments over the Internet.

Here we discuss the development of an Internet-based remote laboratory on semiconductor device characterization. This laboratory, named Automated Internet Measurement Lab (AIM-Lab) [1], together with our circuit simulator AIM-Spice [2], is used in conjunction with courses on semiconductor devices and circuits [3]. These courses might be offered to remote students on a global scale allowing them to obtain hands-on experience in semiconductor device characterization. This removes a major obstacle for establishing a boundless and complete remote engineering education curriculum. As an added benefit, AIM-Lab technology offers the students the opportunity to work with sophisticated equipment, of the kind they are more likely to find in an industrial setting, and which may be too expensive for most schools to purchase and maintain.

The implementation of AIM-Lab is based on a client/server architecture. The server, written in Microsoft Visual C++, includes two main components. One of them is a TCP/IP (Transmission Control Protocol/Internet Protocol) server socket that receives commands sent over the Internet. The second component, the Hardware Abstraction Layer (HAL) interfaces between the instrument driver and the higher levels of the server. It sends the commands to the instrument driver, which uses the HPIB IEEE 488.2 standard protocol to drive the instruments.

Java is the programming language of choice on the client side, since it offers the flexibility of a GUI design, convenient network programming, and platform independence. The client has a pop-up window that provides GUI interactions to the user, and also handles communication directly with the server. All the user has to do is to access the Web site [1], open the client window, and set the parameters for the experiment. The experimental specifications are then transferred via the TCP/IP client socket to the server, and the measurement results are returned to the client for graphical presentation. We plan to expand the AIM-Lab into a network of lab-sites where the collaborating groups develop different lab modules to be shared between the universities within the network.

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Obtaining High Purity 6H-SiC Single Crystals by Annealing

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6H-SiC single crystals grown by sublimation Lely method or Tairov method generally have high impurity concentrations due to unintended nitrogen dopants. Available doping concentrations of n-type 6H-SiC wafers range from mid 1017cm-3 to 1019cm-3 while for p-type 6H-SiC the minimum doping concentration is even higher. On the other hand, higher purity 6H-SiC single crystals are desirable for many device applications. For example, high purity 6H-SiC single crystals will allow fabrication of Schottky diodes with very large breakdown voltage since the breakdown voltage is limited by the thickness of the voltage blocking layer. Currently, the high purity voltage blocking layers are grown by epitaxy and hence they are limited in thickness.

We have studied the annealing behavior of 6H-SiC single crystals at high temperature. Heavily nitrogen doped (ND-NA ~ 1019cm-3) 6H-SiC crystals were annealed in yacuum at 1870-2270K. The physical properties of the initial and the annealed crystals have been studied using Hall effect measurements, optical transmission, and photoluminescence. When the crystal was annealed for 90min at 2220K, the carrier concentration was reduced from 1018-1019cm-3 to 1015-1016cm-3 and the mobility was increased accordingly from 40-60cm2/Vs to 100-200cm2/Vs. The reduction of carrier concentration is caused by the diffusion of the impurity atoms from the bulk to the surface which are then removed by evaporation. It has been also observed that the main donor level is changed from 0.1eV to 0.7eV after annealing. The new deep donor level is attributed to the Si vacancies or to the nitrogen atoms replacing Si atoms in the SiC lattice.

The result may be used to produce 6H-SiC crystals of very low impurity concentrations which are desirable for many device applications.

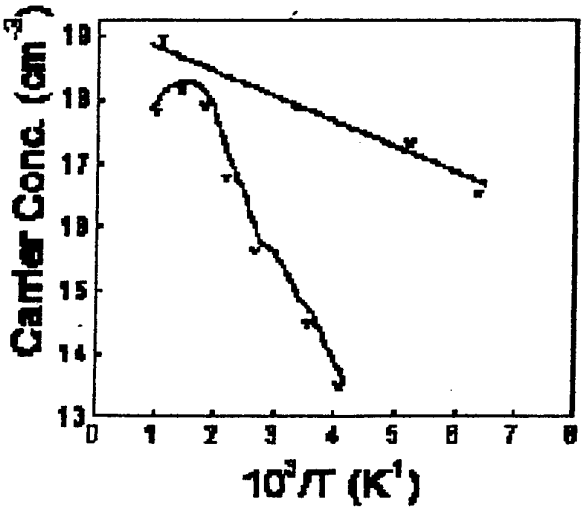

Fig. 1. Temperature dependence of the free carrier concentrations in 6H-SiC crystal before annealing (curve 1) and after annealing at 2220K for 2hrs (curve 2).

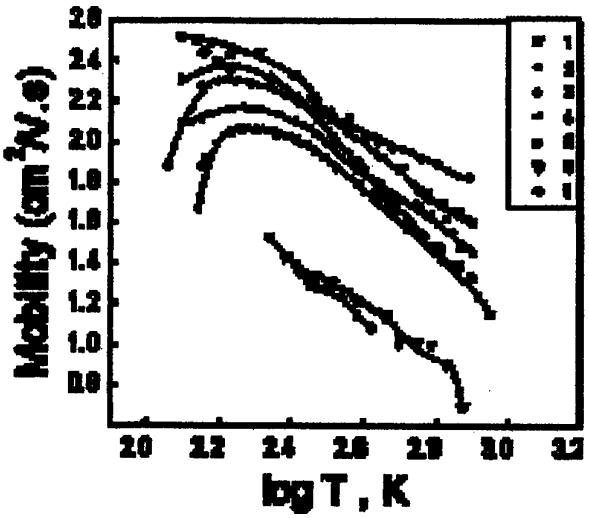

Fig. 2. Temperature dependence of the mobility of 6H-SiC crystal before annealing (curve 1) and after annealing at 2220K for 2hrs. (curve 2).

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Two Dimensional Hole Gas Induced by Piezoelectric and Pyroelectric Charges

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The pyroelectric and piezoelectric effects play an important role in AlGaN/GaN/InGaN based heterostructures [1-3]. Very high values of the two-dimensional (2D) electron sheet density (up to 3x1013 cm-2) have been both predicted theoretically and demonstrated experimentally in AlGaN/GaN Heterostructure Field Effect Transistors. Recently, it was suggested that piezoelectric effects could induce the 2D-hole gas [4]. We will present the results of the band structure calculations for a gated AlGaN/GaN heterostructure with undoped AlGaN layer and a lightly doped p-type GaN layer. These calculations are based on the analytical self-consistent solution of the Poisson and Schrödinger equations at the heterointerface and on the calculations of the spontaneous and piezoelectric polarization as functions of the lattice mismatch based on the theory of elasticity. The results confirm that piezoelectric and pyroelectric charge can induce the 2D-hole gas at the AlGaN/GaN heterointerface. The densities of the 2D-hole gas exceeding 1013 cm-2 can be obtained in a p-type or even in nominally undoped GaN. (Our calculations show that in an n-type GaN, the hole 2D-gas might be very difficult to induce.) The metal/AlGaN/GaN band structures have been calculated for different doping levels with and without accounting for the effects of spontaneous polarization. The results suggest that piezoelectrically induced 2D-hole gas can be used for the reduction of the base spreading resistance in AlGaN/GaN-based Heterostructure Bipolar Transistors.

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Acknowledgement
The Office of Naval Research (Project Manager J. Zolper) has supported this work.

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An Advanced Approach to Extracting Small Signal Model Parameters of MOSFETs from Measured S-Parameters

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By the aid of the open-structure and normal structure measurements, not only the intrinsic parameters but also the extrinsic inductances, resistances and capacitances of the small signal equivalent circuit of MOSFETs are extracted from the measured S-parameters. Especially, taking the parasitic capacitances in consideration should make the extracted intrinsic parameters more accurate. The reliability of the approach is verified through the correspondence between measured and modeled S-parameters in GHz regime.

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Applying Selective Liquid-Phase Deposition to the Fabrication of FETs with Excellent Characteristics

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This work emphasizes on the application of a novel techinique- selective liquid-phase deposition (S-LPD) to the source/drain contact hole formation for FET devices. Because of the demands on the damage-free metal/semiconductor interface, we have developed the S-LPD to replace the conventional reactive ion etching (RIE). The n+/p junction diode has been found having low reverse leakage[1]. The S-LPD method is also proved able to form submicron contact holes as well as RIE. In addition to the low cost in apparatus, the device processes can be simplified and reliable much more than conventional processes. The MOSFET devices fabricated with the S-LPD process have shown the excellent device performance as following: relatively low gate leakage, high output characteristics, low subthreshold swing and high effective mobility. These results are all attributed to the plasma-free process in S-LPD.

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Factors limiting the maximum operating voltage of microwave devices

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The University of Padova, in collaboration with the University of Rome II has carried out a study of hot electron effects, breakdown and reliability in FETs, HEMTs and HBTs. The work has provided new data, obtained by means of experimental techniques and Monte Carlo simulations, concerning the maximum voltage limitations of advanced microwave devices.

The breakdown behaviour of pseudomorphic GaAs-based HEMTs, InP-based HEMTs and HBTs and of SiC JFETs has been studied in detail using DC electrical measurements, frequency dispersion of transconductance, Deep Level Transient Spectroscopy (DLTS), electroluminescence. In particular, electroluminescence measurements have demonstrated that the on-state breakdown of HEMTs is due to a positive feedback mechanism triggered by the holes generated by impact-ionization: (i) generated holes travel in the channel, in the AlGaAs layers and in the substrate, from the high electric field region near the drain towards the source; (ii) once they reach the source region, they thermalize and recombine with electrons, giving rise to emission of photons having the bandgap energy; (iii) the holes accumulated in the source access and substrate region enhance the injection of electrons from the source into the channel; (iv) this enhanced electron current at its turn enhances impact-ionization, leading eventually to on-state device breakdown.

This effect is particularly dangerous in InP-based HEMTs, which adopt In0.53Ga0.47As as channel material: the narrow bandgap of In0.53Ga0.47As induces significant impact-ionization even at low applied voltages. Moreover, the electron impact-ionization coefficient of In0.53Ga0.47As does not follow the usual linear dependence on exp (1/F) (F = electric field) , so that ionization is not negligible even at low F. Finally, the thermal coefficient of the impact-ionization is positive, thus leading to potential electro-thermal positive feedback mechanisms which can induce premature breakdwon and burnout. Despite these limitations, brakdown voltages of InP-based HEMTs can be improved by a clever design of the device (i.e. by adoption of high barrier Schottky layers, InGaAs/InP composite channels, recessed gate structures, p-buffers with backside contacts for removing generated holes).

Impact-ionization effects have been studied also in high breakdown voltage 6H SiC JFETs. Results show that the multiplication factor IG/ID decreases at increasing temperature (the usual behaviour observed in both Si and GaAs); however, several anomalous effects have been observed, such as: frequency dispersion of the transconductance and kink effects at low temperature, decrease of off-state breakdown voltage at increasing the temperature. These effects have been correlated with the presence of incompletely ionized impurities and of deep levels, as suggested by DLTS.

Reliability problems can also limit the applicability of all kind of FET devices at high voltages, due to failure mechanisms induced by hot carriers. During this work we have carried out extensive device accelerated testing and we identified failure mechanisms induced by hot carriers in both GaAs-based pseudomorphic HEMTs and InP-based HEMTs. In particular, trap creation in the gate recess region of pseudomorphic HEMTs has been observed after hot carrier testing, giving rise to kinks in the output I-V characteristics, drain current and transconductance decrease, increase of transconductance frequency dispersion. Drain resistance increase and degradation of the access regions has been found in InAlAs/InGaAs HEMTs on InP. InAlAs surface degradation with trap creation seems to be responsible for the damage. In general, a careful control of the characteristics of surfaces and interfaces seems to be crucial for a good hardness against hot carrier degradation, the most critical region being the recessed gate area, where surface damage may also be induced by plasma treatments and/or wet etching. The adoption of an InP 'passivation' layer on top of the InAlAs greatly improves the reliability of InP HEMTs.

The research also addressed pulsed testing of microwave devices. A Transmission Line Pulse (TLP) system has been implemented, which provides square current pulses of <1ns risetime, 100 ns and 500 ns duration. The system is completely computer controlled and allows recording of current and voltage during the pulse by means of fast oscilloscopes and current probes. Several experiments can be done using this set-up: (i) the output characteristics of power microwave devices can be measured in a avoiding or reducing self-heating effects, thus approximating as much as possible ideal isothermal measurements; (ii) triggering of on-state and off-state breakdown phenomena can be studied and 'snap-back' (negative resistance) of I-V characteristics can be observed; (iii) by increasing the amplitude of the current pulse, failure mechanisms induced in microwave devices by Electrical OverStress

(EOS) and ElectroStaticDischarge (ESD) can be emulated and studied. GaAs-based and InP-based HEMTs, as well as power MESFETs have been TLP tested. Results confirm the positive feedback mechanism previously described, which determines on-state breakdown behavior. Monte Carlo simulations show that accumulation of holes and modulation of drain current requires 10ps - 200ps to take place. In the following, the research will analyze both experimentally and theoretically these dynamic breakdown effects.

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VLSI-Compatible Multiemitter Heterojunction Bipolar Transistors with Enhaced Logic Functionality

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As microelectronic circuits progress towards greater integration, increasing device functionality and decreasing fabrication complexity is crucial. Many proposed systems-on-a-chip integrate standard CMOS transistors with enhanced functionality single-electron or tunneling devices, without addressing the fabrication issues or the disparate operating regimes (such as cryogenic temperatures) that some of these devices require. This work presents multiemitter Si/SiGe npn heterojunction bipolar transistor (HBT) with enhanced logic (an exclusive or gate in a single device) that works at room temperature and is fully VLSI-compatible, as it can be fabricated in a technological BiCMOS process.

The key idea in our multiemitter HBT is to replace a real base contact with a second emitter.1 The n-Si/p-Ge0.2Si0.8 emitter-base junction is doped heavily, while the narrow SiGe base is left floating. The emitter-base diode I(V) characteristic allows emitter contacts to extract the base majority carriers under reverse bias by interband tunneling. Transistor operation is obtained by grounding one of the emitter contacts and biasing the other one high: the small tunneling current flowing in the reverse-biased emitter-base junction controls the large injected electron current in the other, forward-biased emitter-base junction. Excellent transistor characteristics are observed, with dc current gain _ = 400 in large-area devices, identical to HBTs with a standard base fabricated from the same material.2

Emitter contact symmetry leads to enhanced logic functionality, as a single device suffices for an exclusive or function. With one of the emitters biased low (grounded) and the other high (VE2 = 2.5 V), the collector current is high (in the mA range) regardless of which emitter is low, whereas biasing both emitters high leads to a negligible collector current characteristic of a floating base transistor. More than two symmetric emitter contacts can lead to more complex logic, such as the ornand function in a single, three-emitter device.

The multiemitter HBT is compatible with the BiCMOS process using lateral etching and selective regrowth of the base-emitter SiGe/Si layer sequence reported in the literature.3 The only required modification is that, instead of a single emitter stripe, two emitter stripes separated by the minimum lithographic distance are opened simultaneously. The lateral etching and regrowth with p-SiGe results in a connected base that fills the laterally etched cavity, while the n-Si emitter growth follows in the emitter stripes. All other HBT processing steps remain unchanged, as does the compatibility with the CMOS process flow. Consequently, the multiemitter HBT appears particularly promising for BiCMOS circuits: it offers enhanced logic functionality without any penalty in process complexity or operating conditions.

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NANOELECTRONICS

SCALPEL - the Cutting Tool for Sub-0.1 µm Lithography

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Serious difficulties lie on the road to sub-0.1 µm manufacturing, and lithography is prime amongst these. SCALPEL is an electron projection lithography technique which promises a solution. It uses differential electron scattering by a mask and a SCALPEL aperture (Scattering with Angular Limitation Projection Electron Lithography) to obtain contrast. Because it is a projection technique, it allows much higher speed than direct-write. Major progress has been made by the group at Lucent Bell Laboratories and their collaborators, and I will review this. My own group has worked on space charge issues and is now working on novel electron-optical designs for SCALPEL. In my talk I will discuss the progress and future issues.

Prospects of Quantum Devices Based on III-V Compound Semiconductors

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The purpose of the paper is to discuss the prospects of the quantum devices based on III-V compound semiconductors as the key devices for the next generation electronics. The paper reviews recent results obtained on Si-based and III-V based quantum devices, including those obtained in SED project (a Japanese national project on "Single Electron Devices and High Density Integration" for 1996-2,000, Head Investigator H. Hasegawa), and those obtained by the author's group at RCIQE. Then, their future prospects are discussed.

Recent developments have emphasized room-temperature or near room-temperature operations of metal-based single electron transistors (SETs) and Si-based SETs. However, not much attention has been paid so far to the prospects of their high-density integration. Attention has been paid neither to basic circuit performances like voltage gain, although almost all the SETs reported previously exhibited voltage gains below unity.

For realization of ULSIs based on quantum devices, several material and device related key issues should be addressed in addition to issues related the system architecture. First, a suitable technology for formation of high-density arrays of position- and size-controlled ultrasmall wires or dots should be established. Second, a suitable device technology for the construction of quantum devices on these structures should be created. Secondly, these devices should operate room temperature with acceptable high performances. Additionally, the structure of these devices should be suited for planar integration.

From these viewpoints, it is discussed in this paper that the prospects of the III-V quantum devices are good and worthwhile further pursuing toward key devices in future electronics. Use of selective MBE or MOVPE growth technique now allows self-organized formation of high density arrays of ultrasmall wires and dots. Use of new gate structures such as Schottky in-plane gate (IPG) and wrap gate (WPG) has realized high temperature operating GaAs and InGaAs SETs with voltage gain larger than unity[1]. IPG quantum wire transistors(QWTrs) can realize logic circuits near the quantum limit near room temperature. IPG QWTrs with single electron charging by suitable dots promise low power, high speed and large scale memory[2].

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Room-Temperature Single Electron Devices by Scanning Probe Process

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In order to attempt room temperature operation of single electron devices, fabricating feature sizes on the order of a few nanometers is required. Developing this capability is a challenging issue in current nanoelectronics research. For this purpose a new nano-fabrication process that surpasses the resolution of conventional techniques has been invented. This process utilizes the conducting probe of an atomic force microscope(AFM) as an ultra-small cathode to anodize the surface of a 2 nm thick titanium layer which has been evaporated on top of an atomically flat sapphire substrate. Using this technique 10 nm wide lines of titanium oxide have been written, and these lines have been utilized as planar tunnel junctions. Subsequently, single electron transistor, and single electron memory devices were fabricated with minimum feature sizes of 8 nm. The single electron transistor shows one by one electron transfer through the nanostructure at room temperature. Coulomb blockade phenomena such as Coulomb gap, staircase, and oscillation have also been observed. In the single electron memory, 10 electrons have been stored in the memory node for as long as 600 seconds at room temperature, and a hysteresis loop has been observed. This implies that room temperature operation of a memory device which utilizes only a few electrons is now possible at room temperature. These results demonstrate that practical use of such devices may be possible in the near future, and further demonstrate the considerable potential in using a scanned-probe based process for nanofabrication.

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Straddle-Gate Transistor: Transistors in the Limit of Useful Field-Effect*

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Tunneling between the source and the drain is shown to limit the channel length of ann-channel MOSFET to approx-imately 10 nm for a stand-by current- and power-constrained design. This limit is a fundamental constraint in the use of field-effect and similar to the length scale of a ballistic FET 1 . We show, using theoretical simulations and experi-mental measurements, that by changing the electrical length of the transistor between the off-state and the on-state, it is possible to make low power devices that are useful down to approximately 10 nm. Straddle-gate transistors 2 are examples of such a device and they are compatible with ultra-small memory structures such as the quantum-dot memory 3 .

Straddle-gate transistors employ a gate structure with multiple threshold voltage: lower adjacent to the source and drain (the straddle regions) and higher in the control channel (the inner gate region). When the device is off, both regions are off and channel length is longer. When the device is on, the higher threshold voltage controls the device operation. The threshold voltage modulation can be achieved by having a thi ner oxide under the straddle region or by employing multiple work-functions, e.g., metals or SiGe in combination with poly-silicon. During the on-state, the inversion channel under the straddle regions provide carriers. This replacement of the extrinsic doped region by an inversion region leads to improvement in planarity of the conduction close to the surface/oxide interface and hence also improved sub-threshold conduction and output conductance. A straddle region with a threshold voltage ~ 4kT lower than the control gate is necessary for operation with acceptable resistance. I will summarize theoretical results from a straddle-gate design coupled to the back-plane approach 4 in order to achieve an efficient electrostatic design capable of reaching the
10 nm gate length. Much of the discussion will be w.r.t. a structure consisting of a 10 nm tungsten gate, 10 nm poly-silicon side-wall straddles, a 1.8 nm oxide on a 16 nm thick silicon with a 6 nm back oxide between the silicon and the back-plane and simulated using DAMOCLES 5 - a Monte Carlo Boltzmann Transport Equation solver. Simulations of the structures show 4-5 x 10 12 cm -2 sheet carrier density in the on-state in the region under the straddle gate. The con-ductivity of this region is better than that of the doped regions used currently. Thus, source resistance from the inversion region remains controlled. Also, since it is very thin, the electrostatics of the structure are akin to that of a 30 nm gate length structure. Even with a threshold voltage of ~0.6 V, consistent with low intra-band tunneling, transconductances exceeding 1000 mS/mm are obtained together with very low output conductance (75 mS/mm), low threshold voltage change with channel length, linear transfer characteristics, and low sub-threshold conduction. The straddle gate regions behave like the screen electrode of a pentode isolating the inner gate region and confining the carrier-transport close to the oxide/silicon interface.

I will also report experimental results on structures where the oxide thickness was changed in order to achieve the straddle action. These measurements confirm the suppression of off-state current in a straddle-gate transistor due to the modulation of the channel length. They also show improvement in properties that can be directly ascribed to the injection from a thin inversion region rather than a thicker doped region.

This paper will summarize the nature of the tunneling limits in the operation of the field-effect device, the unique char-acter of the straddle-gate transistor in having a modulatable channel length without sacrificing output conductance and gate control, and the scaling of its dynamic behavior for low power.

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*Work partially supported by DARPA through grant N66001-97-1-8908 and by IBM Corporation. This work is a col-laboration
with J. J. Welser, A. Kumar, P. Solomon, and the Silicon Laboratory of IBM and is gratefully acknowledged.

OPTOELECTRONICS AND PHOTONICS - II

Toward mid and far IR intraband lasers based on hot carrier phenomena in quantum wells and superlattices

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For many applications there is a need of semiconductor sources in the range from far to mid IR. Existing and emerging semiconductor lasers of the sort: p-Ge hot hole FIR lasers , mid IR quantum cascade lasers and quantum fountain laser do not meet many of the application needs. In particular they do not operate in the region between far and mid IR.

I will give a review of new approaches to achieve intraband far and mid IR lasing based on hot carrier phenomena in MQW structures under lateral transport. The idea is to achieve lasing due to hot carrier accumulation in the upper higher mass states (like in the Gunn effect) and to the existence of allowed optical transitions between the upper and lower states.

I will discuss the results for the emission and transport properties of three different types of MQW structures: p-type strained InGaAs/GaAs structures with delta doped barriers, p-type strained InGaAs/GaAlAs structures, and n-type
GaAs-AlAs structures. In the latter case, the laser mechanism is related to hot electron accumulation in X-valleys of AlAs. A detailed evaluation of the parameters of this Hot Electron Intervalley Transfer Quantum Well Laser, based on Monte-Carlo simulations, will be presented.

Attempts to achieve lasing in MQW structures and related problems will be discussed.

Brief bio sketch of the author:
Dr. Alexandre A. Andronov is a Corresponding Member of the Russian Academy of Sciences and a Member of the American Physical Society. He is the Deputy Director and Head of the hysics of Superconductivity Department at the Institute for Physics of Microstructures of the Russian Academy of Sciences. He is also Professor and Chair in Quantum
Radiophysics of the Nizhny Novgorod State University. Dr Andronov graduated from the Radiophysical Faculty of Gorky (Nizhny Novgorod) State University. His first Russian scientific degree (Candidate of Science) was received in 1969 from The Radiophysical Faculty of the Gorky (Nizhny Novgorod) State University for the work in theoretical plasma physics (theory of antenna and cyclotron instabilities in plasmas) under supervision of Vitaly L. Ginzburg. Since 1970 Dr Andronov is involved in studying different types of instabilities in the solid state (in semiconductors and superconductors) and also in hydrodynamics. His second Russian Scientific Degree (Doctor of Science) received in 1987 from the Ioffe Institute for works on population inversion and stimulated FIR emission of hot holes in germanium. Dr Andronov is the recipient of the 1987 State Prize for works on population inversion and stimulated FIR emission of hot holes in germanium. His main current scientific interests are in the creation of Far and Mid IR lasers based on hot carrier nonequilibrium phenomena in semiconducting quantum wells and superlattices and in particular in the development of Hot-Electron Intervalley Transfer Quantum Well Lasers.

High frequency circuits based on GaAs-PHEMT technology for modern sensor and communication systems

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Past high frequency systems have been driven mainly by technology push rather than by market pull. However, the demands of todays communication and sensor systems are driving the technologies to the limits. Terrestrial and satellite data links operating in the millimeter-wave range from 20 GHz to 60 GHz are emerging as a powerful means to bring a wide range of services to homes and businesses. Automotive sensors at 77 GHz are going to set new standards in terms of driving comfort and safety. Fiber-optic data transmission systems operating at 40 Gb/s are under intensive investigation.
For related applications, Monolithic Integrated Circuits based on PHEMT technology feature performance, functionality, reliability, and competitive price. In this presentation, the potential of PHEMT ICs for communication and sensor applications up to 100 GHz is discussed. The following topics will be addressed:

- PHEMT characteristics
- Application of coplanar waveguide technology for RF ICs
- Millimeter-wave multifunctional ICs and power amplifiers
- Mixed-Signal ICs and OEICs

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Distributed Balanced Photodetectors for RF Photonic Applications

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Balanced photodetectors are of great interest to analog fiber optic links because they can suppress the relative intensity noise (RIN) of lasers and the amplified spontaneous emission noise (ASE) from erbium-doped fiber amplifiers (EDFA). When used in conjunction with an external modulator with complementary outputs, shot noise-limited system performance can be achieved [1]. In order to fully exploit the advantages of the balanced systems, balanced photodetectors with high saturation photocurrents and broad bandwidth are required. Monolithically integrated balanced photodetectors offer superior performance (broader bandwidth, better matching of photodiodes) and reduced packaging cost. However, most of the integrated balanced photodetectors reported to date have low saturation photocurrents and are not suitable for analog applications.

Previously, we have reported a novel distributed balanced photodetector [2] in the InP/InGaAs material system. It integrates two velocity matched distributed photodetectors (VMDP) with a microwave coplanar waveguide (CPW). This new device inherits the basic advantages of the VMDP, namely, broad bandwidth and high saturation photocurrent [3]. In this paper, we reported on the optimized performance of the monolithic balanced distributed photodetector. A high signal-to-noise (SNR) and large suppression of the laser RIN over a broad range of input powers has been observed in the RF photonic links employing the balanced VMDP. The relative intensity noise (RIN) of a semiconductor distributed feedback laser has been suppressed by 17 dB, and the RF signal has been enhanced by 6 dB. A common mode rejection ratio greater than 27 dB has been achieved. To the authors? knowledge, this is the first report of monolithic distributed balanced photodetectors. The experimental results indicate that the distributed balanced photodetector will have a major impact on most RF photonic systems.

This project is supported in part by ONR MURI on RF Photonics, National Radio Astronomy Observatory, and UC MICRO.

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