

AFRL-SN-RS-TR-1999-167
Final Technical Report
August 1999



REAL-TIME MULTICHANNEL AIRBORNE RADAR MEASUREMENT INTERFACE

ITT Systems

Dan Snell

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

19990907 124

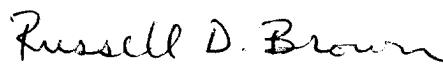
AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE
ROME RESEARCH SITE
ROME, NEW YORK

DTIC QUALITY INSPECTED 4

This report has been reviewed by the Air Force Research Laboratory, Information Directorate, Public Affairs Office (IFOIPA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

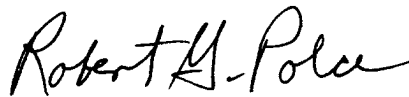
AFRL-SN-RS-TR-1999-167 has been reviewed and is approved for publication.

APPROVED:



RUSSELL D. BROWN
Project Engineer

FOR THE DIRECTOR:



ROBERT G. POLCE, Acting Chief
Rome Operations Office
Sensors Directorate

If your address has changed or if you wish to be removed from the Air Force Research Laboratory Rome Research Site mailing list, or if the addressee is no longer employed by your organization, please notify AFRL/SNRT, 26 Electronic Pky, Rome, NY 13441-4514. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE August 1999	3. REPORT TYPE AND DATES COVERED Final Mar 95 - Sep 97
----------------------------------	-------------------------------	---

4. TITLE AND SUBTITLE REAL-TIME MULTICHANNEL AIRBORNE RADAR MEASUREMENT INTERFACE	5. FUNDING NUMBERS C - F30602-95-C-0223 PE - 0602702F PR - 4506 TA - 11 WU - P7
--	--

6. AUTHOR(S) Dan Snell	
---------------------------	--

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) ITT Systems 775 Daedalian Dr. Rome NY 13441	8. PERFORMING ORGANIZATION REPORT NUMBER N/A
---	---

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Air Force Research Laboratory/SNRT 26 Electronic Pky Rome NY 13441-4514	10. SPONSORING/MONITORING AGENCY REPORT NUMBER AFRL-SN-RS-1999-167
--	---

11. SUPPLEMENTARY NOTES
Air Force Research Laboratory Project Engineer: Russell D. Brown, SNRT, 315-330-2661

12a. DISTRIBUTION AVAILABILITY STATEMENT Approved for public release; distribution unlimited	12b. DISTRIBUTION CODE
---	------------------------

13. ABSTRACT (Maximum 200 words)
A real-time data interface was developed for the MCARM (Multi-Channel Airborne Radar Measurement) program. This report documents the interface hardware which was successfully developed, installed, and operated during flight tests to demonstrate onboard STAP (Space-Time Adaptive Processing). After installation on the BAC-111 flight test aircraft, the interface unit worked as designed without modifications.

14. SUBJECT TERMS Airborne Radar, MCARM, Data Interface	15. NUMBER OF PAGES 32
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT UL
---	--	---	----------------------------------

Executive Summary

ITT Systems is submitting this Final Report for Real-Time Multichannel Airborne Radar Measurement Interface. The results of this work allow processing of Multichannel Airborne Radar Measurement (MCARM) data through the use of specially designed hardware and software interfacing to UNIX hosts as well as other high performance computers.

ITT Systems assisted AFRL/Rome in developing the Real-Time MCARM interface board. This board provides a path from the VME-based host processor to a HIPPI interface. The HIPPI interface provides a generic connection to other boards and/or high performance computers. The HPC enables advanced algorithms to execute in real-time or near real-time on actual measurement data. This effort included the following tasks:

- Development of hardware for a VME to HIPPI interface
- Development of software for the VME based UNIX host
- Development of High Performance Computer (HPC) application software
- Development of network maintenance procedures and software

1. TECHNICAL APPROACH

1.1. Technical Discussion

The Multichannel Airborne Radar Measurement (MCARM) program allows AFRL/Rome to collect quality multichannel radar data from an airborne platform, for the study of clutter and adaptive processing algorithms. Real-time MCARM is AFRL/Rome in-house program for developing hardware and software to collect and process data in real-time or near real-time.

ITT Systems assisted AFRL/Rome in developing the Real-Time MCARM interface board that provides a path from the VME-based host processor to a HIPPI interface. The HIPPI interface provides a generic connection to other boards or high performance computers. The HPC enables studies of advanced algorithms executing in real-time or near real-time on actual measurement data. The following tasks were performed:

- Development of a printed circuit board for the interface between the VME based host processor and the HIPPI interface
- Development of software for the UNIX host
- Development of application software for the HPC
- Development of network maintenance procedures and software to permit the location and correction of network errors and topology

1.1.1. Technical Summary

ITT Systems accomplished the effort as follows:

1.1.2. Task 1: Hardware Development

A 9U VME card hosted the new printed circuit board developed for this project. The circuit for this board consists of an external input circuit, two memory buffers, a VME interface circuit, a Xilinx control circuit, and an external output circuit per channel (Figure 1-1). The MCARM board contains circuitry for four channels.

The input circuit receives 32 bits of synchronous data at a rate of 20 MHz. For the MCARM application, the data from a FFT board are considered 16I and 16Q data bits. However, this circuit can receive any 32 bit data words up to a 20 MHz rate. The incoming data is stored in a memory buffer. This buffer can be as large as 4 MegaWords, each word being 32 bits wide. When the buffer is full, a second memory buffer is switched in to handle the incoming data. This ping pong effect allows input data to be input continuously without interruption.

After a memory buffer is filled and switched to the output mode the VME host computer is notified. The VME host computer can manipulate the data as necessary. When the data is ready to be output the VME host computer starts the HIPPI data output interface. The data is sent to the HIPPI circuitry from the output memory buffer. The HIPPI interface circuit adds all the handshaking needed to implement the HIPPI data transfer.

The Xilinx Control circuit is the traffic cop of the interface. This circuit provides the control logic to store all the incoming data, switches the memory buffers when needed, directs data to and from the VME host, and controls the data going to the HIPPI interface. This circuit is programmable and has the capability to change how the interface works, thus allowing adaptability for other appellations.

The VME interface is provided to allow data manipulation during normal operation. It is also available for diagnostic testing. The VME host can read from any memory buffer or write data to any buffer for testing purposes. The VME bus can also write data to the HIPPI interface.

The MCARM interface card has 2 main modes of operation. These modes are set by a control word from the VME interface. The first mode is the normal data transfer mode. The other mode of operation is the diagnostic testing mode. The normal data transfer mode takes data from the FFT

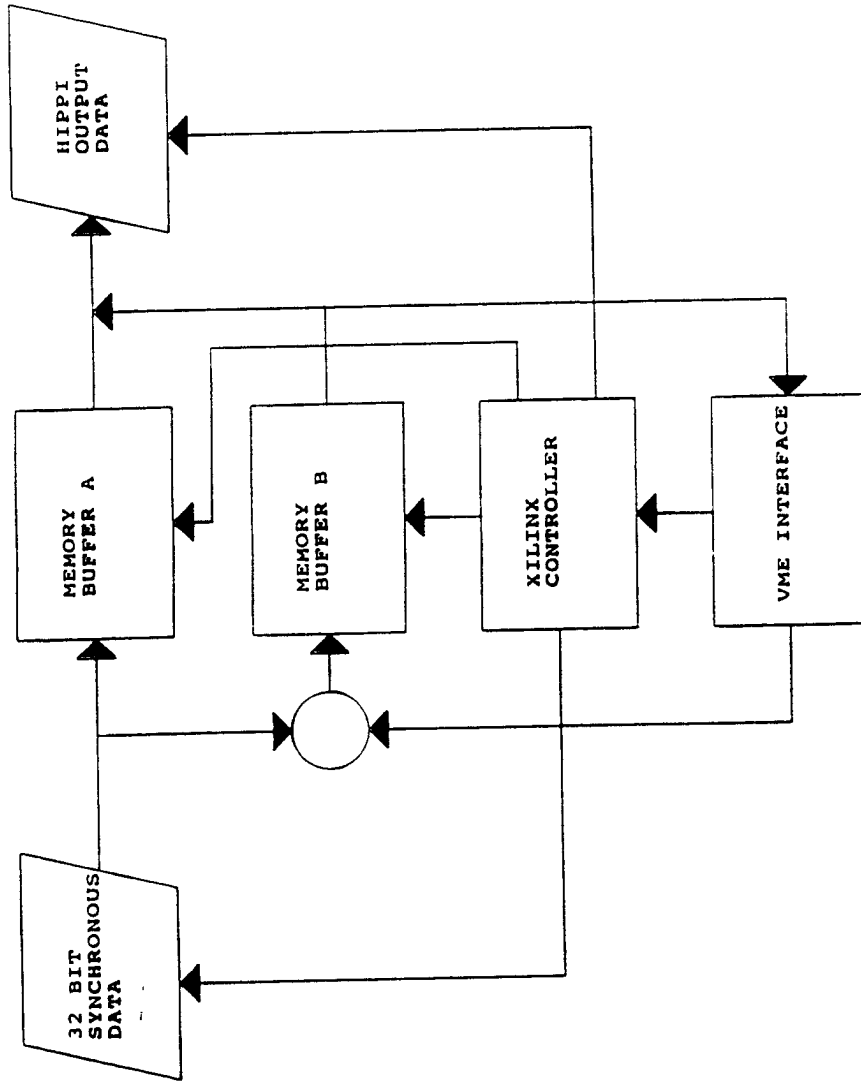


Figure 1-1: MCARM Printed Circuit Board Overview

board, buffers the data, adds control information to the data, and outputs the data to the HIPPI interface.

The diagnostic test mode actually consists of several modes. These diagnostic test modes are listed in the table below:

DIAGNOSTIC TEST MODES
▪ Read data from Memory Buffer A
▪ Read data from Memory Buffer B
▪ Write data to Memory Buffer A
▪ Write data to Memory Buffer B
▪ Reset circuit
▪ Write data to HIPPI Interface

The MCARM board detailed block diagram (Figure 1-2) is discussed in the following paragraphs. The 32 bit input data Catalina board is clocked into a data latch with the input clock. The inputs come into the board through an IDC connector – P50E-100P1-S1-TG at the end of the board. This connector is shared between 2 channels. The input data is sent to a data selector for data memory buffer A and B. The Xilinx Controller selects which Memory Buffer receives the data.

The Xilinx Controller also generates the address to the Memory Buffer for the incoming data. The Data in the other buffer is output to the HIPPI data buffer. The Xilinx Controller generates the Memory addressing and data selection for this output data. The XILINX controller initiates the data out to the HIPPI interface and monitors the status of the HIPPI interface. The XILINX controller monitors the control register generated by the VME interface and updates the VME status register as needed.

VME address and data can be selected for the Memory Buffers to allow reading and writing of data between the VME Bus and the Memory Buffers. Data is output through the HIPPI interface. The HIPPI data and controls signals are output on the same type 100 pin connector as the input data uses. The HIPPI interface does not share a connector between channels.

The Electrical Design and layout of this circuitry and assembly were performed by ITT Systems, State College, PA facility.

The PLD (22V10) and XILINX design was also performed by ITT Systems, State College.

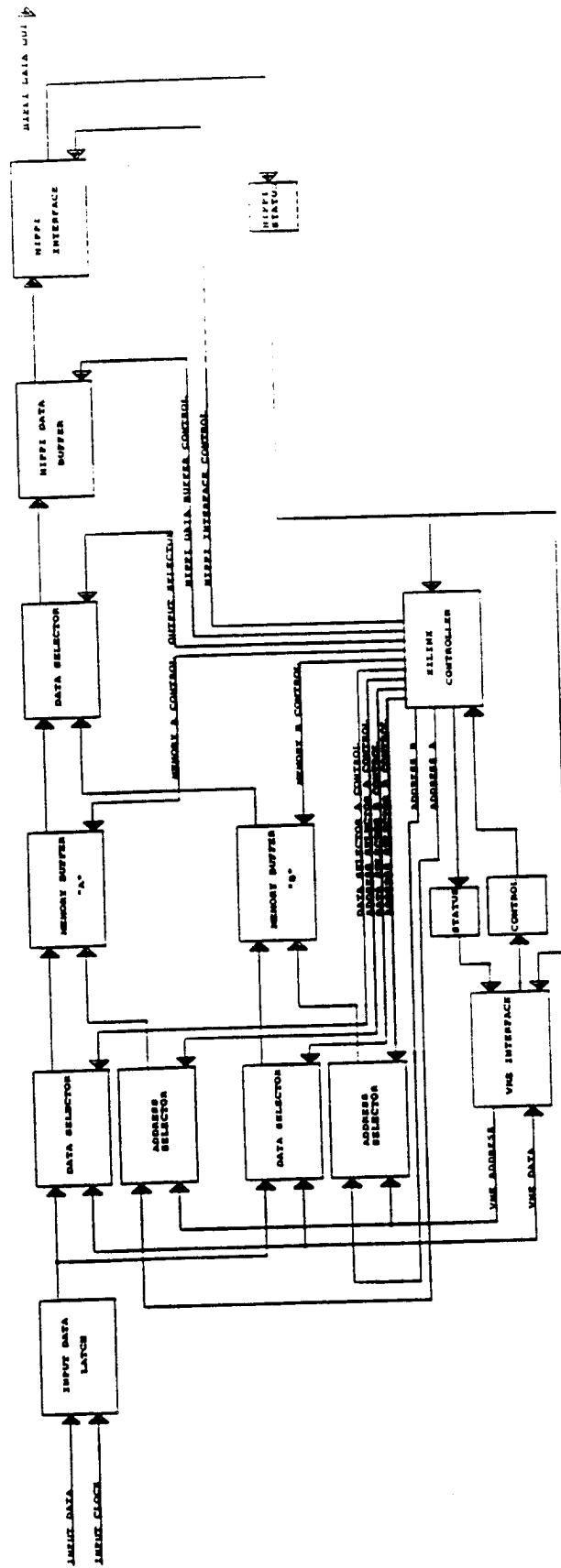


Figure 1-2: MCARM Printed Circuit Board Detailed Block Diagram

1.1.3. Task 2: Software Development

ITT Systems developed the software for the VME host computer to coordinate data transfer between the MCARM PCB data buffers and the HIPPI interface. The software was developed to take full advantage of the MCARM PCB's double memory buffers, thus allowing an uninterrupted 32 bit synchronous data flow.

The VME host software performs required data manipulation as well as monitoring status, mode selection and control of the MCARM PCB.

Diagnostic software was developed to test the operation of the MCARM PCB using the diagnostic mode feature of the board. Tests included read/write memory test of the A and B buffers, reset test, and HIPPI interface test.

Additional VME host computer software was also developed to interface with PCB's other than the MCARM PCB. An example of this is the FFT board that was used in conjunction with the MCARM PCB to provide the 32 bit synchronous data to be processed by the MCARM board.

1.1.4. Task 3: High Performance Computer Interface

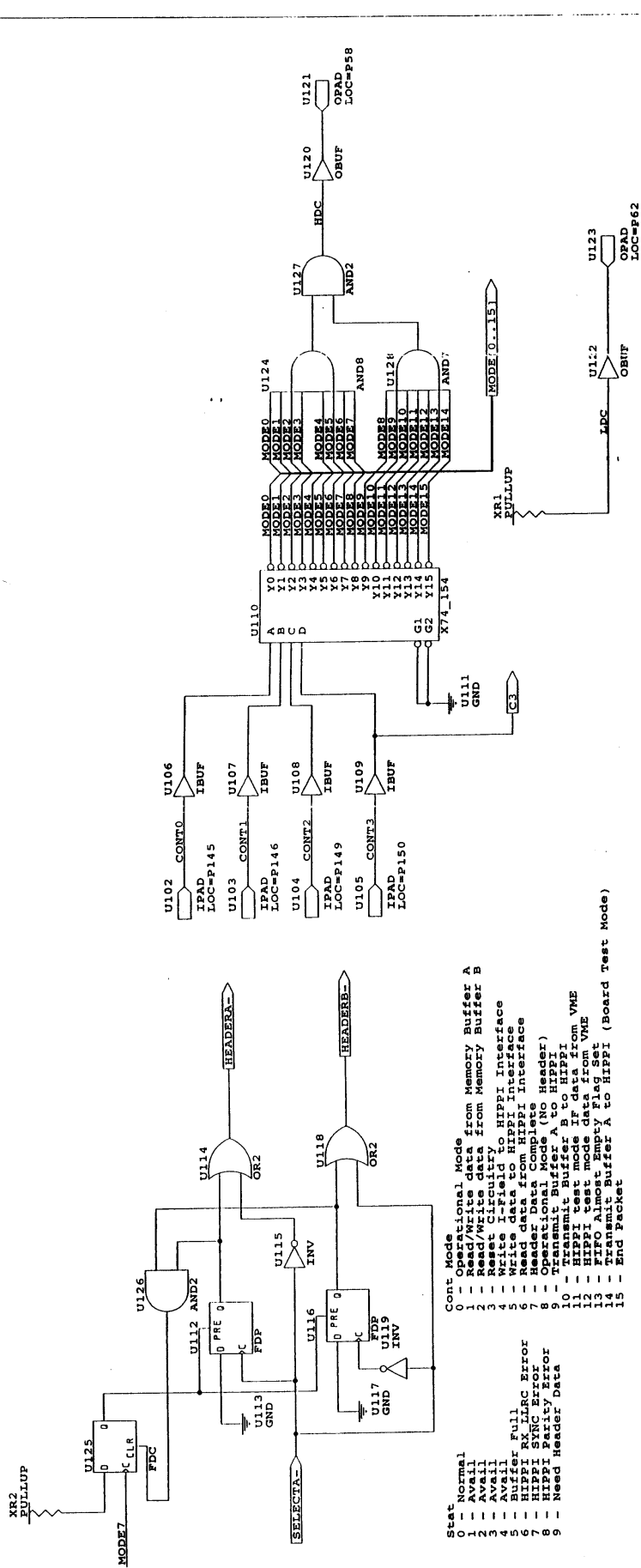
The MCARM PCB HIPPI was interfaced with the HPC. Required software was developed for the AFRL/Rome HPC to support the MCARM PCB to HPC interface.

1.1.5. Task 4: Network Maintenance

ITT Systems supported the integration of the HPC onto the AFRL/Rome network. This included the configuration of the network, and development of procedures and software to ensure proper network operation, and to isolate and fix network problems as they arise.

Appendix A

FPGA Schematics

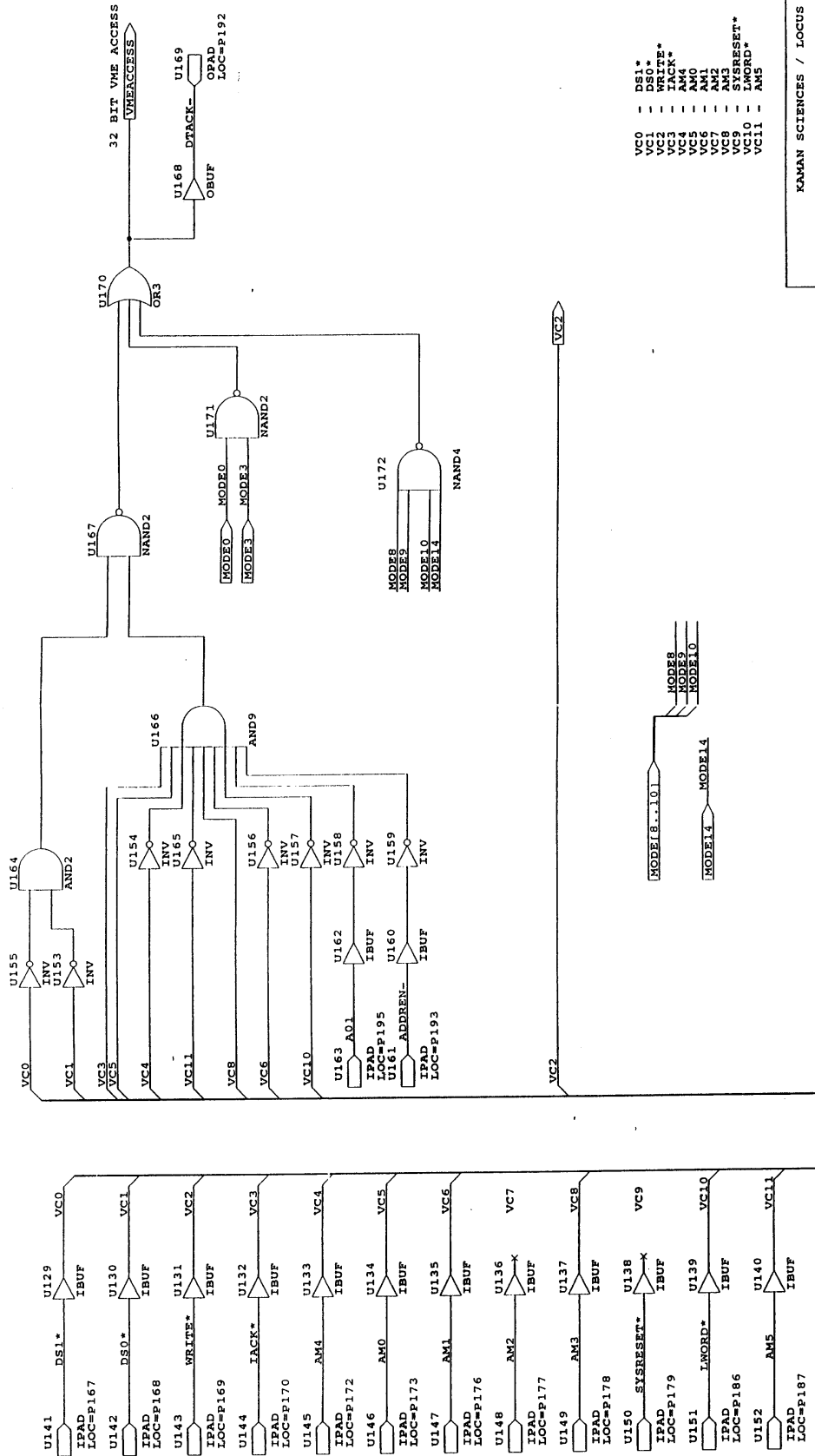


- Stat
- 0 - Normal
 - 1 - Avail
 - 2 - Avail
 - 3 - Avail
 - 4 - Avail
 - 5 - Buffer Full
 - 6 - Buffer Sync Error
 - 7 - HIPPI Parity Error
 - 8 - HIPPI Parity Error
 - 9 - Need Header Data
- Cont Mode
- 0 - Operational Mode
 - 1 - Read/Write data from Memory Buffer A
 - 2 - Read/Write data from Memory Buffer B
 - 3 - Reset Circuitry
 - 4 - Write I-field to HIPPI Interface
 - 5 - Write data to HIPPI Interface
 - 6 - Header Data Complete
 - 7 - Header Data Complete
 - 8 - Operational Mode (No Header)
 - 9 - Transmit Buffer A to HIPPI
 - 10 - Transmit Buffer B to HIPPI
 - 11 - HIPPI test mode IF data from VME
 - 12 - HIPPI test mode IF data from VME
 - 13 - FIFO Almost Empty Flag Set
 - 14 - Transmit Buffer A to HIPPI (Board Test Mode)
 - 15 - End Packet

KAMAN SCIENCES / LOCUS
P. O. BOX 740
STATE COLLEGE, PA. 16804

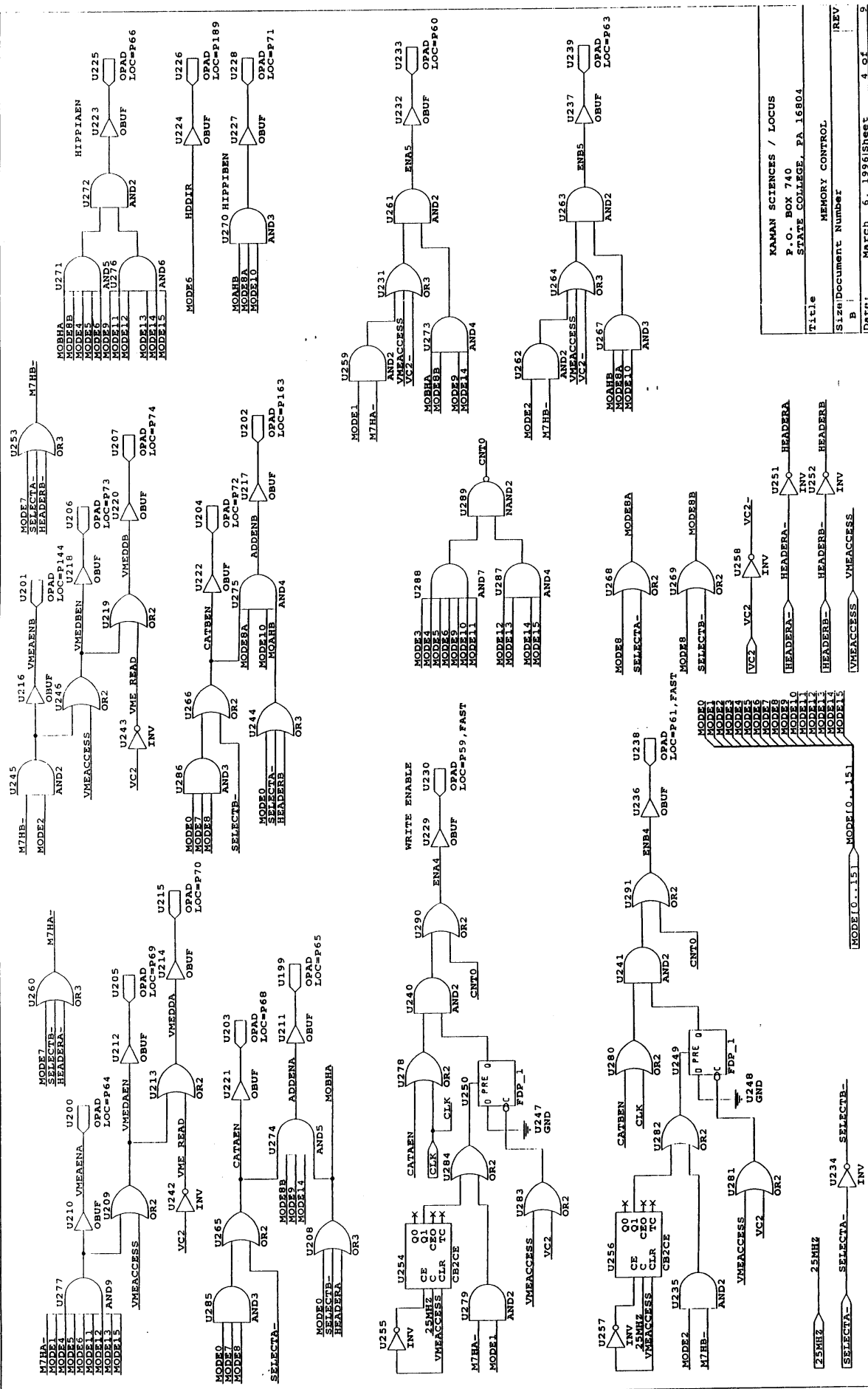
Title	MODE
Size	Document Number
B	REV
Date:	December 11, 1995 Sheet 2 of 2

VMEACCESS = !DS1* & !DS0* & !ACK* & ((!AM[5..0]==001001b) & (AM[5..0]==001101b) & !LWORD* & !A01 & !ADDREN*

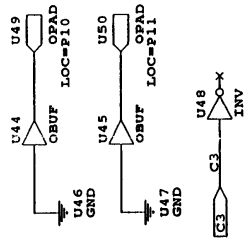
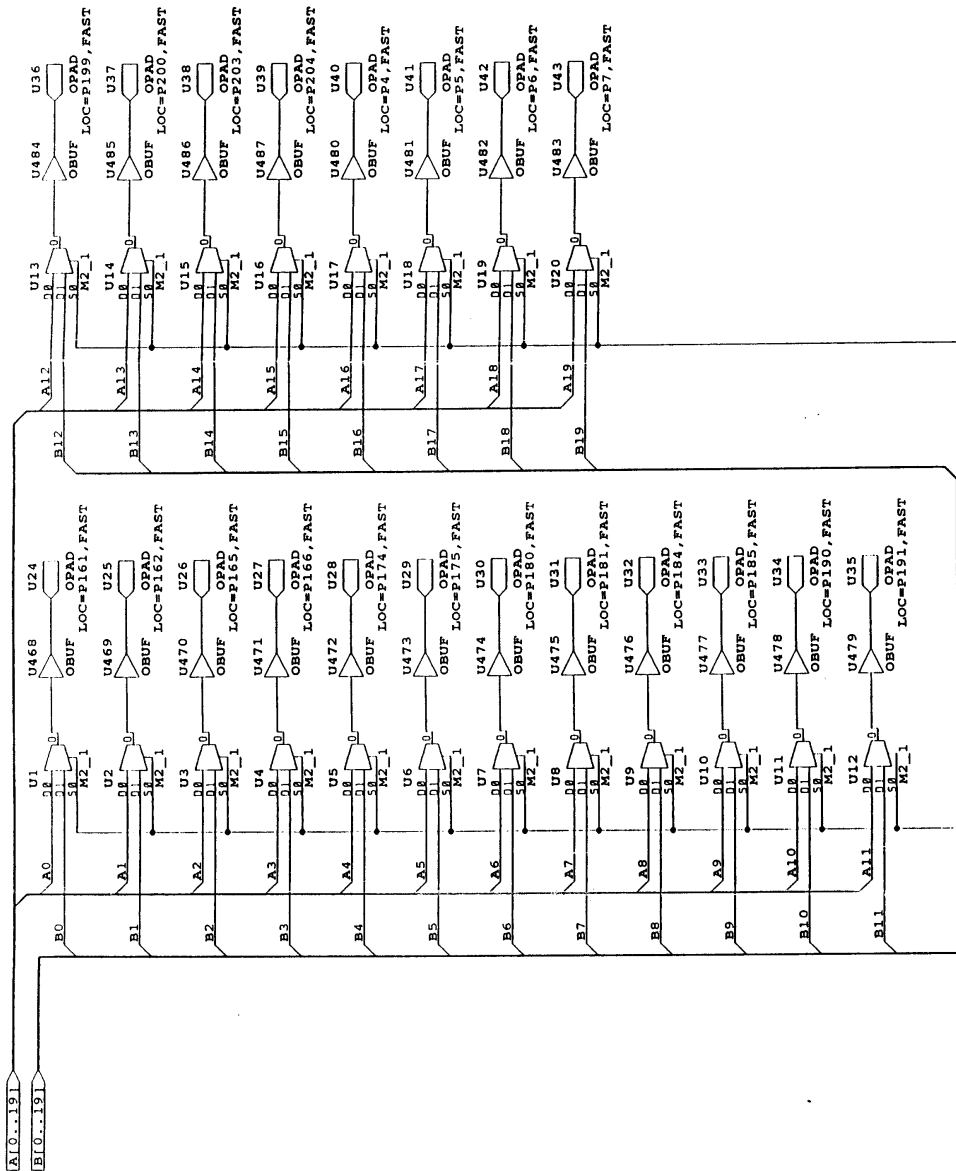


- VC0 - DS1*
- VC1 - DS0*
- VC2 - WRITE*
- VC3 - IACK*
- VC4 - AM4
- VC5 - AM0
- VC6 - AM1
- VC7 - AM2
- VC8 - AM3
- VC9 - SYSRESET*
- VC10 - LWORD*
- VC11 - AM5

KAMAN SCIENCES / LOCUS	
P.O. BOX 740	
STATE COLLEGE, PA 16804	
Title	VME ADDRESS CONTROL
Size/Document Number	
B	REV
Date: December 11, 1995	Sheet 3 of 9



KAMAN SCIENCES / LOCUS
 P. O. BOX 740
 STATE COLLEGE, PA 16804
 Title
 Size Document Number
 B
 Date: March 6, 1996 Sheet 4 of 9

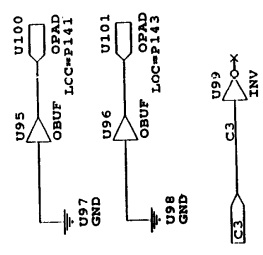
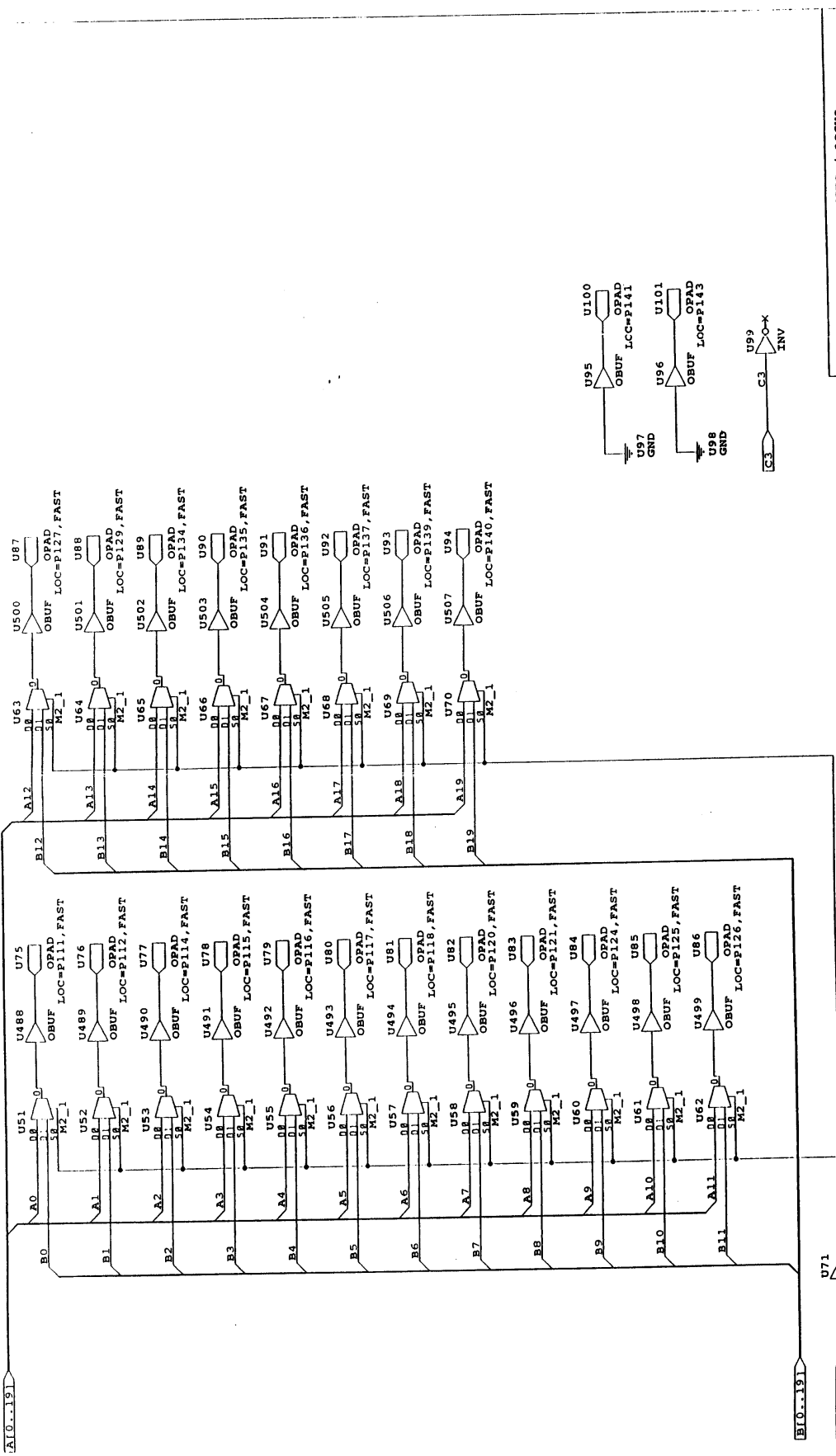


KAMAN SCIENCES / LOCUS
 P.O. BOX 740
 STATE COLLEGE, PA 16804

Title: BUFFER A ADDRESS DRIVER

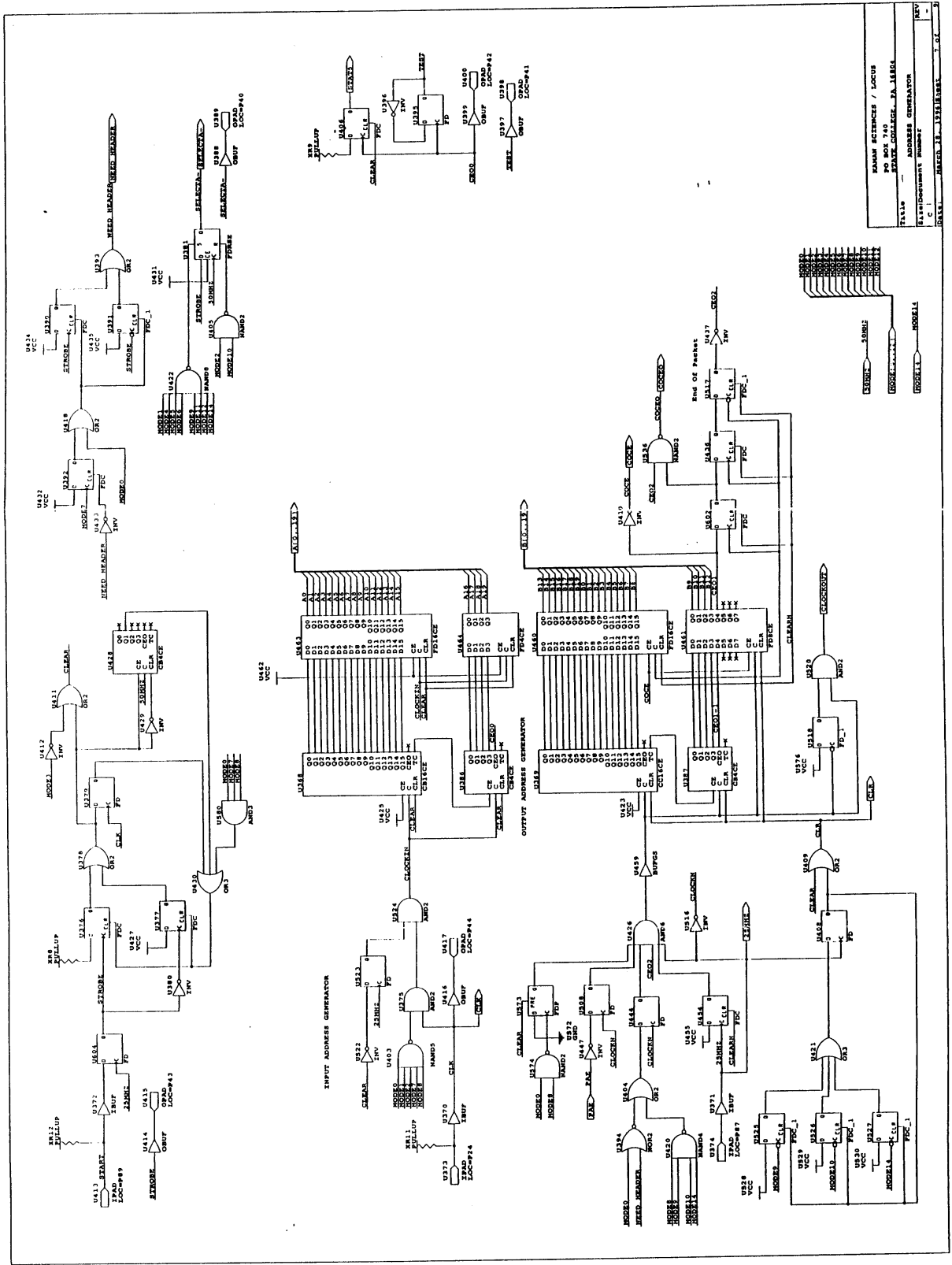
Size/Document Number: B | REV

Date: December 21, 1995/Sheet 5 of 9

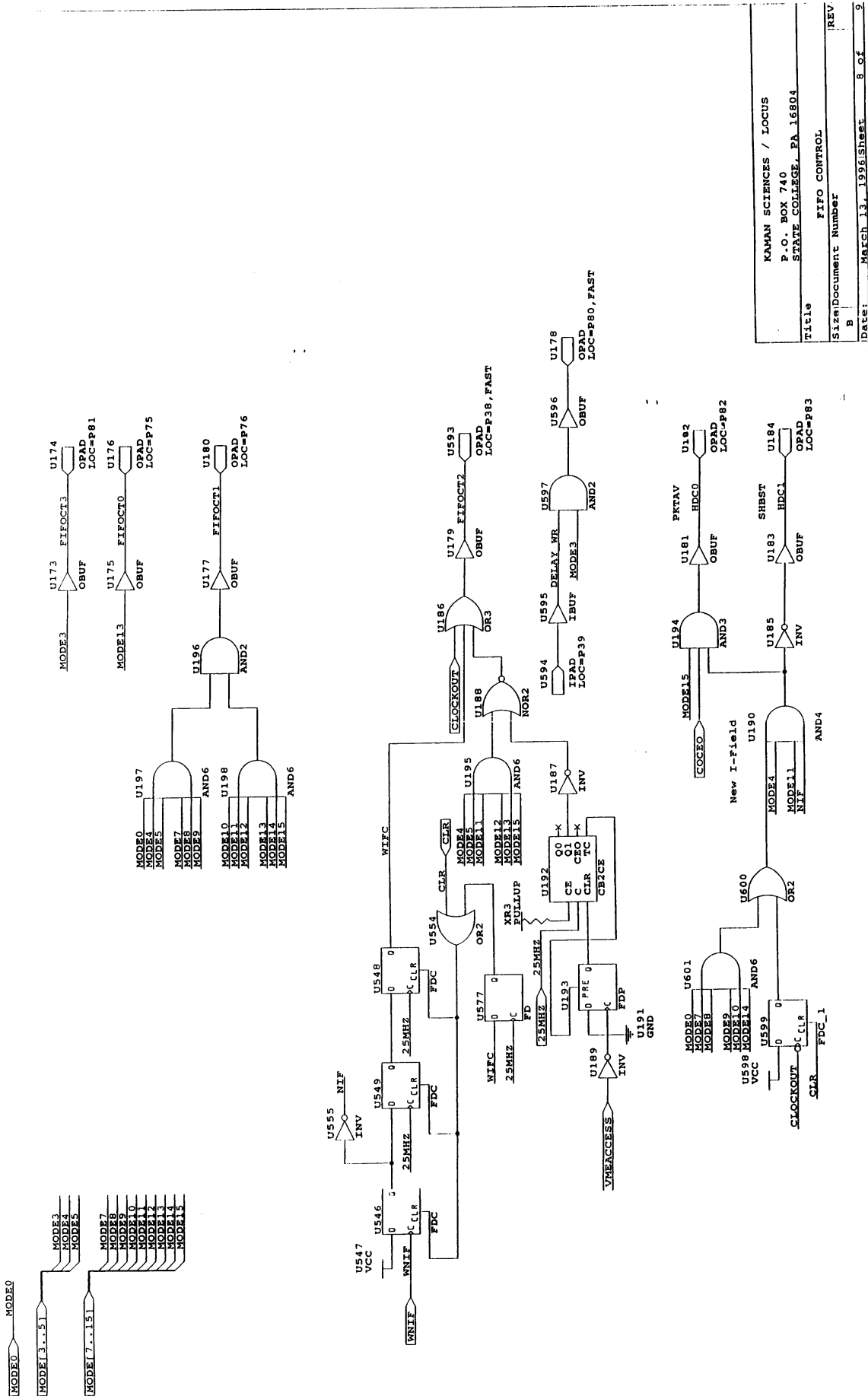


KAMAN SCIENCES / LOCUS
 P.O. BOX 740
 STATE COLLEGE, PA 16804

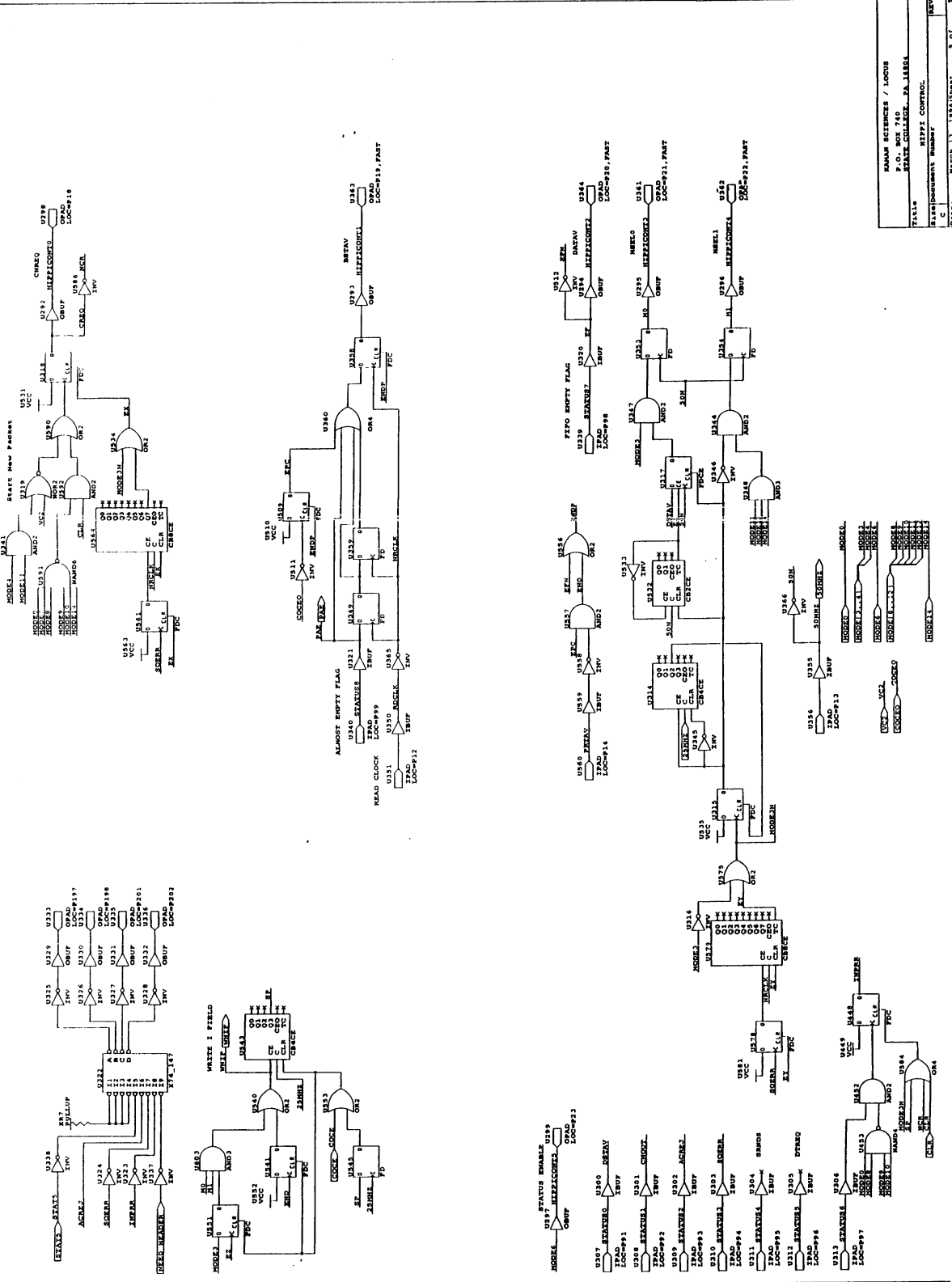
Title: BUFFER B ADDRESS DRIVER
 Size: Document Number
 B
 Date: December 21, 1995 Sheet 6 of 9



HAWAII STATE COLLEGE / LOCUS
 PO BOX 740
 HONOLULU, HAWAII 96813
 TEL: 808-955-1111
 FAX: 808-955-1111



KAMAN SCIENCES / LOCUS	
P.O. BOX 740	
STATE COLLEGE, PA 16804	
Title	FIFO CONTROL
Size/Document Number	
B	REV
DATE: MARCH 13, 1986	SHEET 8 OF 9



KAMAN SCIENCES / LOCUS
 P.O. BOX 740
 STATE COLLEGE, PA 16801
 Title: NIPPI CONTROL
 Part/Document Number: C
 DATE: MARCH 13, 1978