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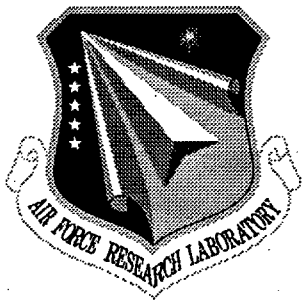

MIXED SIGNAL BUILT-IN SELF-TEST FOR ANALOG CIRCUITS

University of Kentucky Research Foundation

Charles E. Stroud and Eugene B. Bradley

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13. ABSTRACT *(Maximum 200 words)*

A Built-In Self-Test architecture was developed for testing analog circuits in mixed-signal systems. The Built-In Self-Test circuitry primarily resides in the digital portion of the mixed-signal system in order to minimize performance impact on the analog circuitry. The test pattern generation portion of the Built-In Self-Test circuitry produces a number of different test waveforms found to be effective in detecting faults in the analog circuitry. The output response analysis function consists of a double-precision accumulator that facilitates determination of the faulty/fault-free status of an analog circuit with acceptable component parameter variations. Ten benchmark circuits were established for the evaluation of analog testing approaches along with acceptable component parameter variations and a standard set of faults and fault models for each benchmark circuit. Finally, an equation was developed for the calculation of analog fault coverage that takes into consideration the probability of potential detection of faults due to component parameter variation. Evaluation of the Built-In Self-Test architecture via analog fault simulation using the benchmark circuits and the fault coverage equation indicates that the approach is effective in detecting catastrophe and parametric faults in a wide variety of analog circuits.

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MIXED-SIGNAL BASED BUILT-IN SELF-TEST FOR ANALOG CIRCUITS

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FINAL REPORT

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1. Introduction and Overview

Mixed-signal circuits and systems provide a good environment for the development of Built-In Self-Test (BIST) approaches for analog circuits and systems by allowing the experience and expertise of BIST development in digital circuitry to be used as a platform for the investigation of analog BIST techniques. In particular, the basic components of most BIST structures may be incorporated into the digital portion of the design without adverse effects on the analog circuit performance. These digital components include the test pattern generator (TPG) and output response analyzer (ORA) functions as well as the necessary test controller function to initialize and control the BIST sequence and to provide system level access to the test circuitry [1][2]. However, there are aspects of analog BIST which prevent the straight forward application of conventional digital TPG and ORA functions. For example, traditional syndrome analysis and signature analysis using Linear Feedback Shift Register (LFSR) based Signature Analysis Registers (SARs) and Multiple Input Signature Registers (MISRs) are unsuitable for application to analog BIST since the good circuit signature for these digital ORA functions is based on the assumption that an exact output response sequence is assumed in every fault-free execution of the BIST sequence [3]. In a mixed-signal circuit, the sampling noise in the Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) as well as component parameter (i.e., tolerances) and environmental (i.e., temperature and voltage) variations in the analog circuitry will prevent an exact output response sequence (and, therefore, reproducible BIST signatures) from one execution of the BIST sequence to the next. Similarly, traditional digital pseudorandom TPGs based on LFSRs will produce an analog signal that is similar to noise after passing through a DAC. However, ramp input test signals have been used in analog testing techniques and have been found to provide good fault detection results and, in some cases, better results than sinusoidal test signals [4][5]. It has been observed that faults in analog circuits can cause detectable variations in output response delay, rise/fall times, and overshoot when stimulated by certain input test signals. However, it has also been observed that the detectability of faults with respect to the input test signal can vary with the type of analog circuit under test [5].

While some promising BIST approaches for analog circuits have been proposed [4][6], in most cases these approaches are oriented toward the testing of specific classes of analog circuits

and may not be generally applicable to a wide range of analog circuits. In addition, the effect of incorporating BIST circuitry within the analog domain is of concern since it may have adverse effects on the performance of the analog circuit [7]. The intent and purpose of this project was the development of a BIST approach for analog circuitry which resides in the digital portion of mixed-signal VLSI devices and systems in order to minimize any adverse effects on the analog domain while providing a BIST approach capable of detecting faults in a wide variety of analog circuits under test. We begin this report with an overview of the architecture and operation of the mixed-signal based BIST approach for analog circuits in Section 2. In Section 3, we describe the simulation environment used to evaluate the BIST approach and propose a method for calculating fault coverage for analog circuits. We discuss the problems we encountered during fault simulations using the ITC'97 (1997 IEEE International Test Conference) analog benchmark circuits [9] in Section 4 and expand the set of benchmark circuits with additional circuits, and more importantly, with component parameter variations for the benchmark circuits as well as a standardized set of faults and fault models. We then present the fault simulation and fault coverage results for the mixed-signal based BIST approach using the set of benchmark circuits in Section 5. The design, implementation and operation of a prototype unit used to demonstrate the feasibility of the mixed-signal BIST approach is described in Section 6. Finally, the participants that contributed to the project as well as the publications that have thus far resulted from the project are summarized in Section 7, and the report is concluded in Section 8 with guidelines and suggestions for the practical application and implementation of this mixed-signal BIST approach.

2. BIST Architecture

The basic BIST architecture is shown in Figure 1 where the digital BIST circuitry that has been added to the mixed-signal circuitry is shown in bold black and the analog circuitry under test is shown in shades of grey. The normal mixed-signal system components include the digital system functions as well as the analog system functions along with the DACs and ADCs that are required to convert the digital signals to analog waveforms and vice versa. The BIST circuitry additions include the digital TPG and ORA functions as well as a digital test controller and analog loopback capabilities. The analog loopback functions (analog multiplexers) are the only circuits associated with the BIST approach to be inserted in the analog domain and, as a result, minimize the impact of the BIST approach on the operation and performance of the analog circuity. The purpose of the analog loopback is to facilitate the return path for the test signals from the TPG, through the analog circuitry under test, and back to the ORA. An additional multiplexer (MUX) is required for the insertion of the digital test patterns into, and isolation of unknown system data from, the input data stream to the DAC. Since the target circuitry under test is the analog system circuits, including the DACs and ADCs, we incorporate the digital TPG and its associated MUX immediately prior to the digital inputs of the DAC. Similarly, we incorporate the digital ORA at the output of the ADC.

In order to make the BIST circuitry usable during system-level operation for off-line testing and system diagnostics, the BIST circuitry must be capable of proper initialization of the analog circuitry under test, isolation of system data inputs, and reproducible results from one execution of the BIST sequence to the next in the same manner as is required in digital systems [3]. The length of the initialization sequence must be sufficient to clear the effects of previous system signals in the analog circuitry. Faults can be effectively isolated to a given section of analog circuitry within the diagnostic resolution of the analog loopbacks multiplexers. For example, with the left-hand

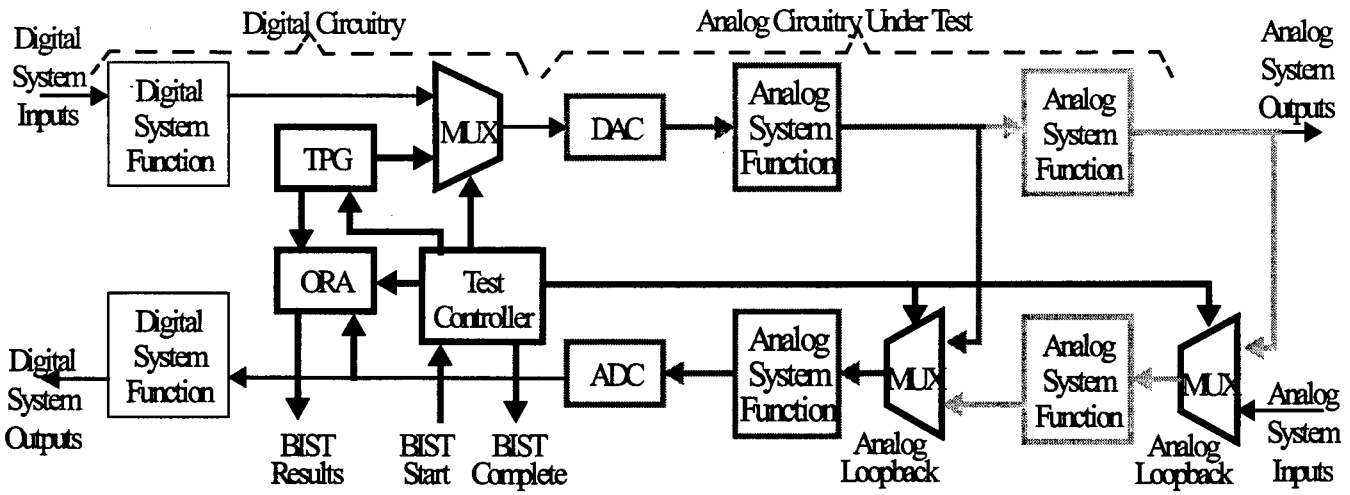

Figure 1. BIST Architecture for Mixed-signal Systems

analog loopback in Figure 1 activated, any faults detected are isolated to that path from the TPG to the ORA (indicated by the dark grey bordered analog circuitry and paths in Figure 1). If the BIST sequence indicates a good circuit, then the left-hand analog loopback can be deactivated while the right-hand loopback function can be activated and the BIST re-executed. Faults detected during this second BIST sequence would be isolated to the analog circuitry shown in light grey in Figure 1. Therefore, the selection of the sites for the analog loopback functions can be based on the desired diagnostic resolution versus the impact on the analog circuit in terms of performance.

The TPG (illustrated in Figure 2) is an 8-bit design which includes a binary up/down counter that also functions as an LFSR with a programmable characteristic polynomial. The counter operates in different modes to provide a variety of analog test patterns. For example, a single pass through the up-count range produces a ramp signal while multiple passes through the up-count range produces a saw-tooth analog test signal. Combining a series of up-counts followed by down-counts generates a series of triangular waveforms at the output of the DAC. The LSFR mode of operation in the TPG, on the other hand, produces an analog signal that is more noise-like in its properties. The bit reversal MUX reverses the order of bits to the DAC (MSB becomes LSB and vice versa) and has the effect (particularly for the counter modes of operation) of producing test patterns that look like noise [8]. During any of these modes of operation, the outputs of the programmable shift registers are logic ones such that the count value holding register is always loaded and its output is always enabled to the DAC.

Since the frequency response of analog circuits is important in terms of fault detection capability, waveforms that sweep through a frequency range are produced from the TPG design. The frequency sweep mode of operation in the TPG provides a square wave test pattern which progressively increases in frequency. The square wave begins with a half period of 255 clock cycles and decreases by N clock cycle during each subsequent half cycle of the square wave until the last half period is one clock cycle in duration. At the same time, the amplitude increases by a value of N with each cycle of the square wave. In both the amplitude and period, the value of N is controlled by programmable shift registers where $1 \leq N \leq 8$. This is illustrated in Figure 3 for a simple 4-bit counter design and N=1. When the frequency sweep function is enabled, the AND gates are used

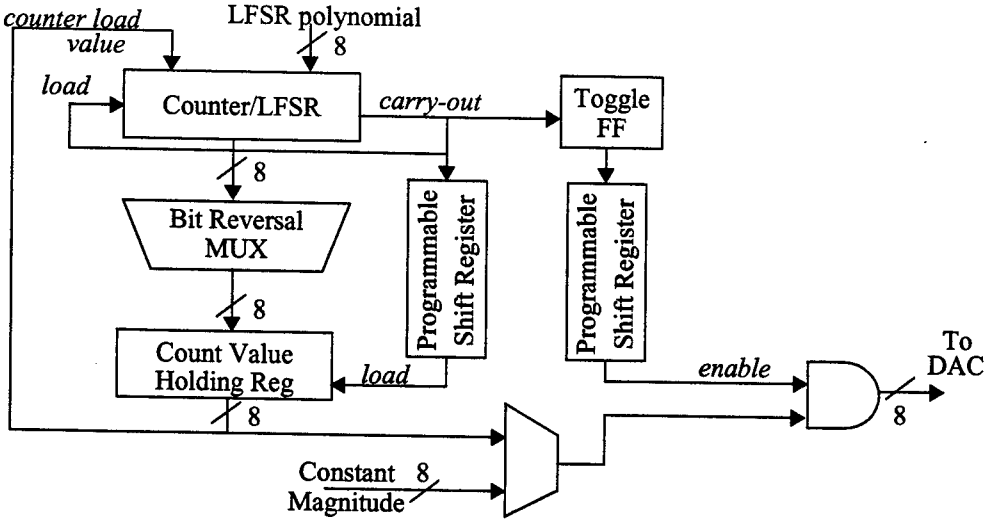

Figure 2. TPG Block Diagram

to set the magnitude of the square wave generated whenever the output of the toggle flip-flop and programmable shift register is a logic one (otherwise the magnitude is zero). The count value holding register is initialized to a value of all zeros at the beginning of the frequency sweep. *N* clock cycles after the counter is loaded as a result of the carry-out, the count value holding register is loaded with the contents of the counter due to the carry-out shifting through the programmable shift register. Consequently, the count value is incremented *N* times by the counter prior to being loaded into the holding register, where it is held until the end of the current count cycle. The square wave generated progressively becomes shortened in terms of the period. Enabling the bit reversal during a frequency sweep mode will load non-sequential values into the counter value holding register such that the frequencies and amplitudes will appear to be random. Alternatively, a constant magnitude for both the regular frequency sweep or the frequency sweep bit reversal functions can be obtained by the multiplexer in conjunction with a magnitude register (or a hard-wired magnitude value rather than a register to reduce area overhead). The various test waveforms produced by the TPG are summarized in Table 1.

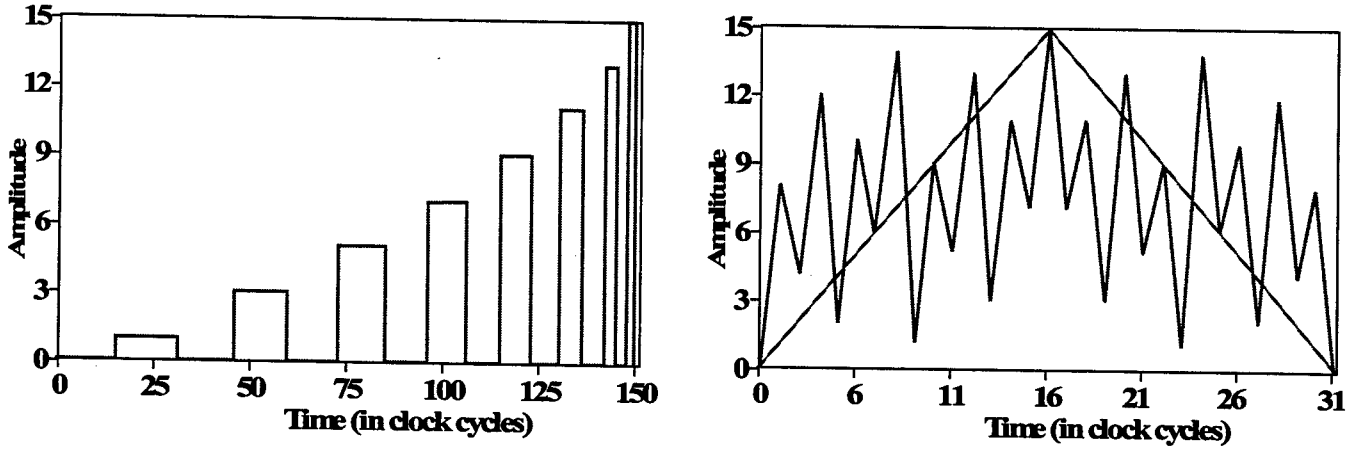

Figure 3. Frequency Sweep and Count-Up/Down Bit Reversal Waveforms

Table 1: Summary of test waveform produced by TPG

Digit pattern	Analog Waveform	Pictorial	Bit Reversal Waveform
count-up	saw-tooth		noise
count-down	saw-tooth		noise
count-up/down	triangular wave		noise
LFSR	noise		noise
Frequency Sweep (varying amplitude)	increasing amplitude decreasing period	see Figure 3	random amplitudes random periods
Frequency Sweep (constant amplitude)	constant amplitude decreasing period	see Figure 3 but with constant amplitude	constant amplitude random period

The ORA, illustrated in Figure 4 consists of a double-precision digital accumulator used to sum the magnitudes of the sampled output responses from the analog circuitry under test. The accumulator-based ORA facilitates the determination of the pass/fail status of the BIST by expecting the final sum to be within a predetermined range of values to account for acceptable variations in the analog component parameters, voltage, and temperature as well as quantization noise in the DAC and ADC. Determination of the range of resultant values which indicates that the circuit is fault-free is based on specifications of the analog circuit responses to the various input signals produced by the TPG (as will be discussed in the subsequent sections). An analog checksum circuit has been previously proposed for BIST of analog circuits [4], but the advantage of a digital ORA is that the results can be read directly through system digital interfaces during system level testing without the need for additional ADCs to retrieve the BIST results. Simply summing the magnitudes of the output responses of the analog CUT may not detect faults that could result in phase shifts or faults which result in the superposition of noise on the analog signal. In the first case, summing the magnitudes of the sampled analog signal may only detect the fault at the beginning and end of the BIST sequence. In the latter case, the noise could average to zero such that there is no change in the resultant accumulator value from that of the fault-free circuit. However, summing the absolute value of the difference between the input test signal (from the TPG) and the output response of the analog circuit (from the ADC) facilitates detection of both of these fault cases. As a result, we have included an absolute value subtracter circuit in the ORA design which can be selected via BIST control signals for this phase shift and noise detection.

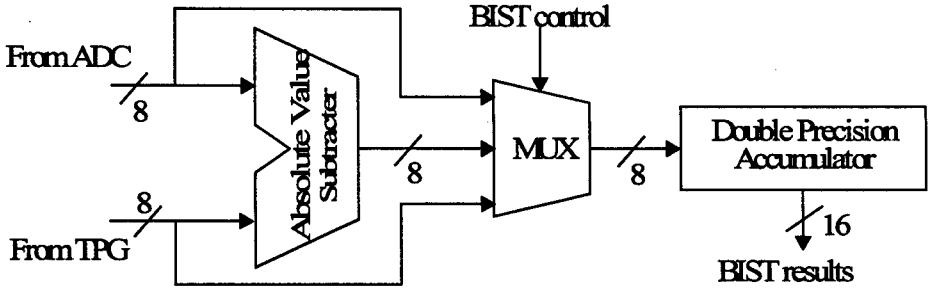

Figure 4. ORA Block Diagram

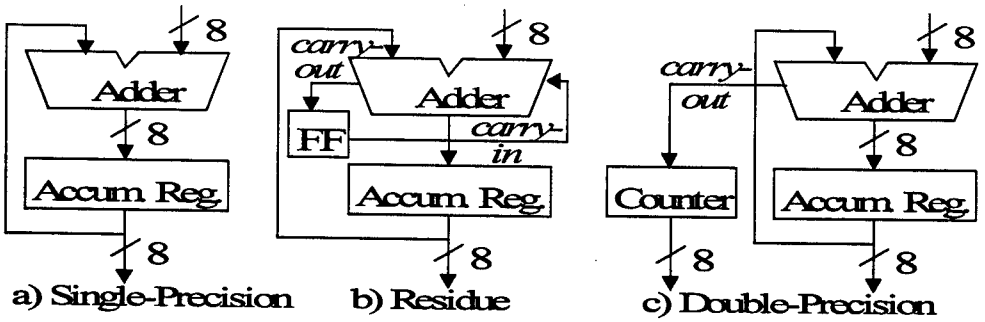

Figure 5. Accumulator-Based ORAs

During the initial stages of the project, two other accumulator designs were studied in addition to the double-precision accumulator; these include a single-precision accumulator and a residue accumulator as illustrated in Figure 5. However, the single-precision and residue accumulators were found to work well only for output response waveforms with small amplitudes and/or short test sequences. Otherwise, the acceptable range of good circuit signatures grew to use the entire range of these smaller accumulators such that fault detection capability was lost. Therefore, for very long test sequences with large amplitude output responses, a triple-precision accumulator (using $3M$ bits, where M = the number of bits coming from the ADC) could provide improved fault detection capability over that of the double-precision accumulator at the expense of additional BIST circuitry area overhead.

The complete BIST session consists of three separate test phases. During each test phase, the various test waveforms are produced by the TPG and the resultant ORA value is read to determine the pass/fail status of each waveform. If any of the test waveforms within each of the three test phases fails to produce the correct accumulator value (or a value within the acceptable range of values in the last two test phases) for that waveform, the circuit is considered to be faulty. The three test phases include:

1) loopback of the TPG output directly to the ORA input to test the digital BIST circuitry,
2) summing the magnitudes of the analog output response to test the analog circuitry, and
3) summing the absolute value of the difference between the input test pattern and the analog output response, again to test the analog circuitry (here, the analog faults targeted are those that lead to noise or phase shifts in an otherwise good analog circuit response).

Initially we had assumed that the digital BIST circuitry would be tested during the two analog circuit test phases. However, when we investigated the digital fault coverage as a function of the range of good analog circuit signatures, it was observed that digital fault coverage quickly dropped as the range of good circuit signatures increases. Therefore, it was decided that the best testing methodology was to first determine the fault-free or faulty status of the digital BIST circuitry before proceeding to the analog test phases. This requires the expansion of the ORA multiplexer from 2-inputs to 3-inputs as illustrated in Figure 4. Although, this caused a small increase in area overhead, yet ensured greater than 97% single stuck-at gate level fault coverage of the digital BIST circuitry (excluding the absolute value difference circuit) as determined by digital fault simulation. With the 8-bit design for the BIST architecture used for this investigation, the good circuit signature for the count-up, count-down, count-up/down, and LFSR test waveforms along with their bit

reversal counter-parts is hexadecimal FD00 for the digital only test phase (this is performed with the ORA in the magnitude summing mode). The good circuit signature is significant since it indicates that the single-precision and residue accumulators would have "rolled-over" 253 times which indicates that the BIST sequence length and amplitudes exceed the capabilities of these types of accumulators. The frequency sweep test waveforms produce different good circuit, digital-only BIST signatures due to their longer test sequence lengths.

3. Evaluation Technique and Software

The principle fault simulation tools used for this analysis include SPICE and the Statistical Fault Analyzer (SFA) [10][11][12]. We used SFA to perform the initial analog fault simulations using the test patterns produced by the TPG. SFA performs Monte Carlo simulations via SPICE of the faulty and fault-free circuits using the specified tolerances of the analog components with a normal distribution for component parameter variations. SFA is a single stuck-at fault simulator where the fault list is simulated one fault at a time with the fault or faulty component value specified in the fault list. This faulty value remains fixed during that faulty circuit simulation. SFA also facilitates the determination of which faults in the analog circuit are undetectable. We use the test waveforms produced by the TPG for all simulations. These test waveforms are produced by a program developed during this project which produces SPICE PWL statements for each TPG test waveform as a function of the TPG clock frequency specified by the program user. This option facilitated the investigation of the fault detection capabilities of the test waveforms as a function of frequency and assisted in determining the optimal TPG and ORA clocking frequency (including the sampling rate of the DAC and ADC) for any given analog CUT. As will be shown in this report, the appropriate selection of this clock frequency is essential in obtaining maximal fault detection for different analog CUTs.

We made a number of minor modifications to SFA in order to accommodate our simulation environment. First, we included a option to specify the seed to the random number generator in SFA from the command line. This enabled us to execute SFA in a single iteration run mode yet still ensuring that SFA did not select the same component values from one run to the next by applying a different seed during each simulation. This made SFA more compatible with the software we were developing for analysis of the BIST architecture since the output of each simulation had to be post-processed by our ORA emulation software (as will be described in the next paragraph and subsection). In addition, this enabled the resimulation of a given seed value in the event that a particular simulation warranted further investigation. We also found that the Gaussian distribution random number generator sometimes produced a negative number of component parameter values which resulted in simulation problems in SPICE. As a result, we modified the SFA source code to use the absolute value of component parameters produced by the random number generator. Finally, we modified the SFA source code to generate an input netlist file and command line options (for batch mode simulation) which were compatible with the version of SPICE3 that we had running on a multitude of HP workstations in the College of Engineering at the University of Kentucky. This facilitated having multiple simulations running in parallel on many different HP workstations as opposed to being limited to SUN workstations running the SUN OS operating system (we were ultimately limited to only one such SUN workstation). We also attempted to modify he SFA source code to be compatible with the output of the version of SPICE3 we were running on the HP workstation, but this development effort has not been completed to date. Therefore,

when we wanted to verify the detectability of a given fault via traditional SFA hypothesis testing analysis, we would use the SUN OS workstation.

After each simulation of one of the TPG waveforms, we applied the output responses obtained from the SFA Monte Carlo simulations in SPICE for the fault-free analog circuit to the ORA to determine the resultant signatures (values obtained in the double precision accumulator) that were due to the component parameter variations. This was performed by a program developed as part of this project which post-processed SFA simulation output files to determine the resultant signature for both the magnitude summing and difference summing modes of operation of the double-precision accumulator. By comparing all of the resultant signatures, we established the range of acceptable values for the BIST sequence from the maximum and minimum signature values. This procedure was performed with each test waveform for both the analog BIST phases (summing the magnitudes or summing the difference in magnitudes) to determine the acceptable ranges of fault-free circuit values for each of these ORA modes of operation. The acceptable signature ranges for each test waveform in both test phases are then used to determine the detection of faulty circuits.

3.1 External Control Software for SFA

Although SFA is an effective fault analyzer, external software was needed to fully emulate the mixed-signal BIST architecture for evaluation of its fault detection capabilities. Since work began on this project, the external software has been modified and updated to ensure consistent results and to create greater autonomy for the simulation procedures. Figure 6 illustrates the current flow of the simulation environment. The ADC and DAC between the analog and digital circuitry were assumed to be ideal in all simulations.

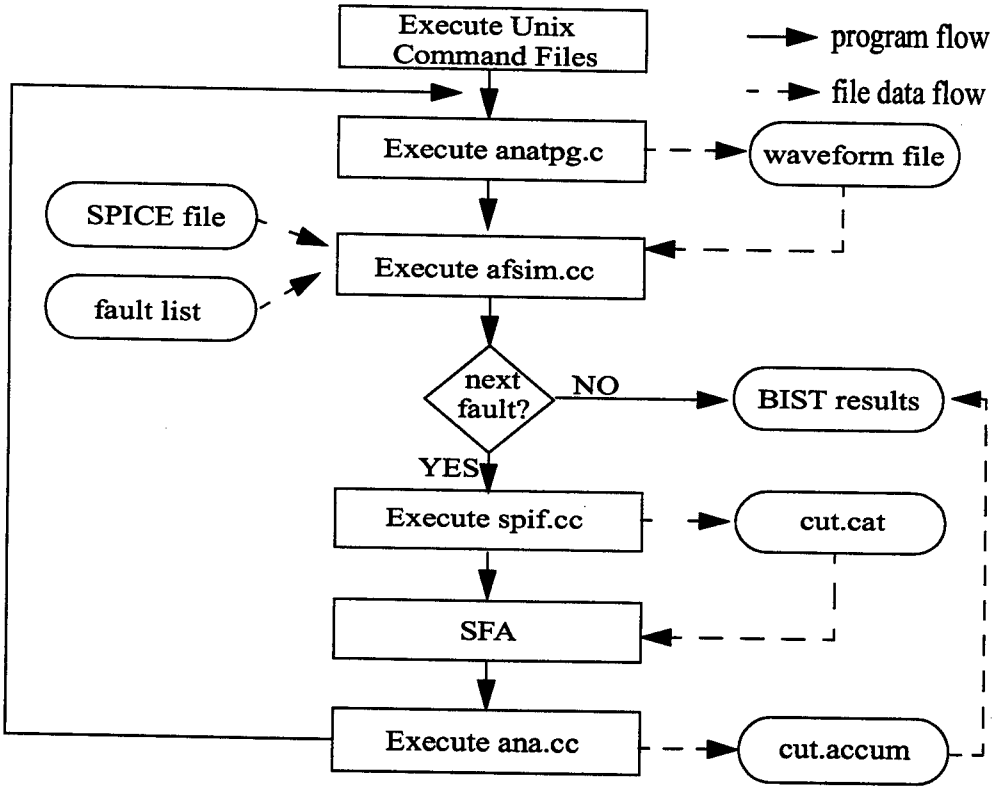

Figure 6. Program Flow for Simulation Environment

Before the input file is in sufficient form for SFA, several steps are taken. First a program (*anatpg.c*) generates a waveform file that contains the clock pulse, the TPG waveform and the .trans statement at a particular frequency all specified by the user. Look again at lines 3-5 of the sample circuit. Notice the bold, italicized parts of these lines. This information is stored in the file generated by *anatpg.c*. The waveforms generated by the *anatpg.c* program are equivalent to those that are generated by the BIST TPG, with one addition that is discussed later. This program allows the waveforms to be run at any clock frequency.

Line 3: vck 100 0 ***pulse(0 5 0s 0.001us 0.001us 0.004us 0.01us)***
Line 4: vin 10 0 ****TPG waveform inserted****
Line 5: ***.tran 0.005000us 12.800000us***

At this top most level, the SPICE file, the TPG waveform, and the fault list are in three separate files. Next the program *spif.cc* copies the SPICE file to a generic file *cut.cat*, where a single fault from the file containing the fault list and the waveform to be simulated are inserted into the SPICE file by the program *afsim.cc*. The first line inserted from the fault list is always the parameter "GOOD", which instructs the SFA to conduct a simulation of the circuit under fault-free conditions. This "GOOD" circuit simulation is used to determine the detectability of the circuits with faults inserted.

With all parts of the input file to SFA included, SFA runs its procedures as described in the previous section. For each Monte Carlo simulation, the external program *ana.cc* accumulates the data in the training set using both the magnitude summing method and the difference summing methods of the ORA described in Chapter 2. *Ana.cc* generates a file called *cut.accum*, which is read by the program *afsim.cc*. *Afsim.cc* records the maximum and minimum values for the BIST results from the *cut.accum* file. When the "GOOD" circuit is run, this maximum and minimum becomes the range of acceptable circuit outputs. For each simulation per fault, the accumulated values in *cut.accum* are compared against the acceptable range to determine whether the circuit passes or fails, which is discussed in greater detail later.

The execution of the programs and SFA is also controlled by the *afsim.cc* program. *Afsim.cc* also provides a seed value to SFA that initializes the random number generator in SFA, which controls the component variation in the SPICE file. The highest level of hierarchy is controlled by UNIX command files. Using a single command line, the user can specify the circuit to be simulated, the waveforms to be run, the frequency of the waveforms, the number of Monte Carlo simulations to be run per fault, as well as specific TPG parameters for the frequency sweep modes of operation, such as the amplitude of the frequency sweep or the N parameter of the programmable shift register.

3.2 Fault Detection and Fault Coverage

In the same manner as the fault-free circuit, the various test waveforms are applied to the faulty circuit during multiple SFA simulations in SPICE. The digital values obtained from each faulty circuit simulations are applied to the ORA in each of its two summing modes of operation. If the resultant signature lies outside the acceptable range for the fault-free circuit for that test waveform, the fault is considered to be detected. The fault is considered to be undetected if the resultant signature of the faulty circuit falls within the range of acceptable values for the fault-free circuit. Since we perform multiple Monte Carlo simulations in SFA where the fault-free components are allowed

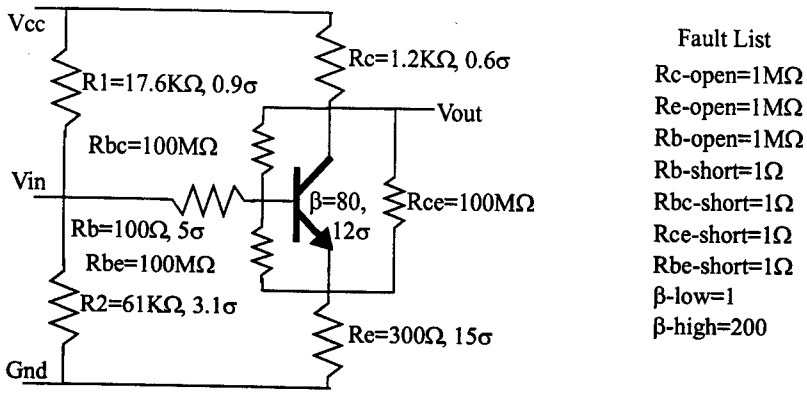

Figure 7. Single Stage Amplifier

to vary within the specified range we must consider the complete set of simulations for the determination of fault detection. If all signatures for a given fault were outside the good circuit range, the fault is always detected. If none of the signatures fall outside the good circuit range, the fault is never detected. But if some of the signatures fall outside and some fall inside the good circuit range, we consider the fault to be potentially detected with the probability of detection proportional to the percentage of faulty circuit signatures that lie outside the acceptable range of values for the fault-free circuit.

Due to the probability of potential detection of faults as result of acceptable component parameter variations, we propose and use the following expression for the determination of fault coverage for an analog circuit, given a set of test patterns and output response analysis technique:

$$FC = \frac{\left(\sum_{\text{all faults}} P_{D_i} \right)}{\text{total number of faults}} \qquad \text{where } P_{D_i} \text{ is the probability of detection for fault } i$$

This equation for evaluating fault coverage for analog circuits gives the ability to consider potentially detected faults. For example, a circuit with 10 faults, of which 5 faults are always detected and 5 faults are never detected would yield a fault coverage of 50%. On the other hand, a circuit with 10 faults with all of those faults being potentially detected and having a potential detect probability of 0.5 would also yield a fault coverage of 50%. As another example, the single stage common emitter amplifier circuit, shown in Figure 7 (this circuit is used as a benchmark circuit in all SFA documentation [10][11]), was simulated using the process described above for all of the test waveforms produced by the TPG. The allowable variations of the analog component parameters are specified by the 1-σ variation next to each component value. For example, consider the specification for β in Figure 7; the nominal value of β is 80 while the 1-σ variation 12 which means that the normal distribution for β will have its mean at 80, 1-σ points at 68 and 9 with the normal distribution extending out to the 3-σ points of 44 and 116. The set of nine faulty circuit components and their faulty values are also given in Figure 7. SFA hypothesis testing indicated that all nine faults are detectable. The fault simulation results are given in Table 2 for each of the TPG test waveforms for both the magnitude summing as well as the sum of the absolute value of the difference between input and output waveforms. The values given in the table are the percentage of 10 simulations (with component parameter variations) per fault in which the fault was detected.

Cumulatively over all testing, all of the faults simulated were detected with the exception being the β-high fault which was potentially detected with a cumulative detection probability of 90% (this detection probability is cumulative across both the magnitude summing and the difference summing in the ORA). It should be noted that the common emitter amplifier was designed to tolerate β variations which explains why this particular fault is more difficult to detect. Then, from the fault simulation results, we find the overall fault coverage to be 98.9% using the equation given above.

A few other observations are worth comment at this point. As can be seen in Table 2, some of the test patterns proved to be less effective in detecting faults than others. Specifically, the bit reversal for some of the test waveforms (including bit reversal for count-up, count-down, and LFSR) were ineffective in detecting any additional faults. However, we did find these waveforms to be effective in detecting faults in other circuits. We also observed different fault detection capabilities with different characteristics polynomials for the LFSR and, as in the case of digital circuits, we found primitive polynomials to provide the best fault detection capabilities in general. We found the fault detection was frequency dependent, as one would expect. For example, the simulations for the data given in the table were at a TPG clock frequency of 100MHz but we were able to find TPG clock frequencies at which we obtained 100% fault coverage. Finally, without considering component parameter variation of the fault-free components, we were able to detect all faults including the β-high fault. Therefore, it is important to include acceptable component variations to obtain an accurate indication of the fault coverage.

Table 2: BIST Fault Simulation Results for Common Emitter Amplifier

Fault	Count Up	Count Up Bit Rev	Count Down	Count D Bit Rev	Cnt Up/ Down	Cnt U/D Bit Rev	LFSR	Freq Sweep	Freq Swp Bit Rev	Freq Swp Fix Amp	
Magnitude Summing											
Rc open	100%	100%	100%	100%	0%	100%	100%	0%	0%	50%	
Re open	0%	100%	100%	50%	0%	100%	100%	0%	0%	10%	
Rb open	100%	40%	100%	100%	0%	20%	100%	0%	0%	10%	
Rb short	100%	100%	40%	20%	0%	100%	40%	40%	10%	0%	
Rbc short	100%	50%	100%	100%	0%	100%	100%	0%	10%	10%	
Rce short	100%	40%	100%	100%	0%	40%	100%	0%	20%	0%	
Rbe short	0%	100%	100%	0%	0%	100%	100%	0%	0%	0%	
β low	100%	50%	100%	40%	0%	90%	100%	10%	10%	20%	
β high	10%	20%	60%	10%	10%	20%	60%	20%	10%	10%	
Difference Summing											Cumulative
Rc open	90%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
Re open	100%	100%	100%	30%	100%	100%	100%	10%	0%	30%	100%
Rb open	100%	100%	100%	100%	100%	100%	100%	0%	90%	10%	100%
Rb short	100%	100%	40%	20%	100%	100%	30%	10%	20%	0%	100%
Rbc short	90%	100%	100%	100%	90%	100%	100%	20%	30%	10%	100%
Rce short	100%	50%	100%	100%	100%	60%	100%	0%	0%	100%	100%
Rbe short	100%	100%	100%	0%	100%	100%	100%	0%	0%	0%	100%
β low	100%	100%	100%	20%	100%	100%	100%	20%	20%	20%	100%
β high	70%	10%	80%	10%	70%	10%	80%	10%	10%	10%	90%

4. Benchmark Circuits

The ITC'97 analog benchmark circuits consist of a set of seven analog circuits and are

described in [9]. We began using the ITC'97 benchmark circuits for initial evaluation of the mixed-signal based BIST approach and ran into a number of problems. These included discrepancies between the schematics and the output response waveforms reported in [9] as well as the SPICE files distributed on the web home page for the benchmark circuits. For example, the first benchmark circuit described in [9] is an OpAmp which consists of 8 MOSFETs in the schematic but the SPICE file contains 9 MOSFETs. Similarly, the Leapfrog Filter has 12 resistors in the schematic but 13 in the SPICE model. Aside from these problems, which can be easily overcome by selecting either the schematic or the SPICE file as the "real" circuit, we ran into more serious problems in our use of the benchmark circuits. These problems primarily center around the fact that there are no component parameter variations specified for the benchmark circuits and there are no specified set of faults or fault models for these circuits. A final problem encountered was that some of the benchmark circuits are functional models as opposed to a netlist of components that can be directly faulted for simulation and analysis of the BIST approach. Therefore, we eliminated from consideration those benchmark circuits that were composed of functional models (such as the ADC circuit [9]) as well as benchmark circuits that did not have a SPICE file available on the IEEE Mixed-Signal Benchmark Circuit home page (www.ee.uwashington.edu/mad/benchmarks/benchmarks.html). In their stead, we obtained benchmark circuits from SFA documentation and other sources. The set of benchmark circuits we used in our evaluation are summarized in Table 3 in terms of the benchmark circuit and its source, along with the number of components and a break down of those components.

Table 3: Summary of Analog Benchmark Circuits

Benchmark Circuit (Source)	Total No. of Components	No. Resist	No. Caps	Other Components	Hard Faults	Soft Faults
OpAmp #1 (ITC'97 [9])	11	2	1	8 N&P MOSFETs	22	6
Continuous Time State Variable Filter (ITC'97 [9])	42	7	2	3 OpAmp #1s	84	36
OpAmp #2 (ITC'97 [9])	10	0	1	9 N&P MOSFETs	20	2
Leapfrog Filter (ITC'97 [9])	77	13	4	6 OpAmp #2s	154	46
Low Pass Filter (Lucent Tech)	15	3	1	1 OpAmp #1	30	14
Elliptical Filter (SFA [12])	45	15	7	3 OpAmp #1s	90	62
Comparator (SFA [12])	13	3	0	1 OpAmp #2	26	8
Differential Pair (SFA [12])	9	5	0	4 BJTs	34	18
Single Stage Common-Emitter Amp (SFA [10])	6	5	0	1 BJT	16	12

As mentioned in the previous section, faults were easily detected during fault simulations by the mixed-signal BIST approach when no component parameter variations were specified for the analog CUT. In this case there is no range of good circuit signatures such that any deviation of the analog output response is seen as a detection of the fault being emulated in the circuit. But for any practical implementation, components will have variation due to tolerance, voltage, temperature, etc. Therefore, we established an acceptable range of component parameter variations for those circuits that did not already have component variations specified (which was all of the ITC'97 benchmark circuits and the Low Pass Filter). To set the range of component variations, we limited output phase and gain variation to +/-10% of the output response using the nominal component values. The SFA benchmark circuits had parameter variations specified which met the +/-10% output phase and gain variation. Following the SFA convention, we specified the 1-σ value and used the normal distribution in HPSICE for Monte Carlo simulations. These component variations are given

along with SPICE source files, schematics, and phase/gain vs. frequency plots for the nominal component values and the component variations on our web page at www.engr.uky.edu/EE/Stroud/anabckts.html. Another benchmark circuit not included in Table 3 but included in our web pages include the ITC'97 DAC.

Similar to the component parameter variations, there were no faults or fault models specified for the ITC'97 benchmark circuits. In the SFA benchmark circuits, there was no standard set of faults or fault models; each circuit had its own set of faults and these were not consistent from one circuit to the next. We began by establishing a set of catastrophic faults (also called hard faults [9]) and a set of parametric faults (also referred to as soft faults [9]) for each benchmark circuit. The hard faults consist of stuck-open and stuck-short faults for all resistors and capacitors, stuck-on and stuck-off faults for all MOSFETs, and stuck-open and stuck-short for each terminal of all BJTs. Therefore, there are $2M+2R+2C+6B$ hard faults in the analog circuit where M is the number of MOSFETS, R is the number of resistors, C is the number of capacitors, and B is the number of BJTs in the circuit. The soft faults consist of the +/- 6-σ values for all resistors and capacitors as well as the β for all BJTs. Therefore, there are $2R+2C+2B$ soft faults in an analog circuit. The number of hard and soft faults for the benchmark circuits are included in Table 3. While the soft faults are modeled by simply changing the value of the component, we have modeled the hard faults with a series resistor (Rs) to model the stuck-open/stuck-off fault and a parallel resistor (Rp) to model the stuck-short/stuck-on fault. For the fault-free case, Rs=1Ω and Rp=100MΩ. For the stuck-open/stuck-off fault, Rs=100MΩ and for the stuck-short/stuck-on fault, Rp=1Ω. A list of the hard faults and soft faults are included on our web pages for the benchmark circuits, as well as the HSPICE source files. We should point out that all simulations used to establish acceptable component parameter variations were done with the fault models in the SPICE source file (using the fault-free case values for Rs and Rp) so that the phase and gain vs. frequency response would not change once the fault models were introduced.

In summary, the ten proposed benchmark circuits for analog and mixed-signal testing that we have made available at www.engr.uky.edu/EE/Stroud/anabckts.html consists of the following information for each benchmark circuit:

- A schematic diagram of the benchmark circuit with component labels,
- A table listing the number of components along with their nominal parameter values,
- A plot of the gain and phase frequency response for the benchmark circuit with nominal component values,
- A table with the acceptable component parameter variations that ensure less than 10% variation in the output response of the circuit with these parameter variations specified at the +/- 1σ point,
- A plot of the gain and phase frequency response from the Monte Carlo simulations used to establish the acceptable component parameter variations to show those regions where the 10% variation in the output response of the circuit was obtained,
- A list of the catastrophic (hard) faults modeled for the circuit,
- A list of the parametric (soft) faults for the circuit along with the faulty parameter values specified at the +/- 6σ points (for high/low parametric faults, respectively), and
- The HSPICE netlist source file, with the hard fault models included (using the fault-free values), that was used to obtain the two gain and phase frequency response plots.

5. Experimental Results

The results of fault simulations for benchmark circuits using the hard faults models are summarized in Table 4 in terms of the number of faults simulated, the number of faults detected and the overall fault coverage with and without component parameter variation. The simulation results without component parameter variation are denoted in the table as "no-var". For the benchmark circuits with component parameter variation, the number of faults that were potentially detected has been included. The overall fault coverage was calculated using the equation presented in Section 3. As can be seen from the table, all faults were detected when component variation was not simulated, which suggests that realistic component variation is necessary for accurate evaluation and comparison of analog testing techniques. This is further illustrated with the drop in fault coverage for some circuits when component variation is simulated. However, even with component variation, all faults were either detected or potentially detected; no faults were found to be undetectable. In addition, the mixed-signal based BIST approach was able to obtain fault coverage of greater than or equal to 95% for all benchmark circuits. It should be noted that the components simulated for the Leapfrog Filter and Elliptical Filter were the components external to the OpAmps while in all other circuits the components internal to the OpAmps were simulated along with the external components. A more detailed discussion of the fault simulation results for the proposed set of benchmark circuits is presented in the following subsections with particular emphasis on results which lend insight into the analysis and optimization of the BIST architecture. Fault simulations for were performed using test waveforms produced by the TPG running at clock frequencies from 100Hz to 1GHz with the highest fault coverage reported in Table 4.

Table 4: Summary of Analog Benchmark Circuit Fault Simulations

Benchmark Circuit (Source)	Faults Simulated	Faults Detected (no-var)	FC (no-var)	Faults Potentially Detected	Faults Detected	FC
OpAmp 1 (ITC'97 [9])	22	22	100%	1	21	98.6%
Continuous Time State Variable Filter (ITC'97 [9])	84	84	100%	20	64	97.4%
OpAmp 2 (ITC'97 [9])	20	20	100%	0	20	100%
Leapfrog Filter (ITC'97 [9])	34	34	100%	2	32	98.8%
Differential Pair (SFA [12])	42	42	100%	9	33	95.0%
Elliptical Filter (SFA [12])	18	18	100%	0	18	100%
Comparator (SFA [12])	26	26	100%	2	24	95.4%
Single Stage Common-Emitter Amp (SFA [10])	16	16	100%	0	16	100%
Low Pass Filter (Lucent Tech)	30	30	100%	0	30	100%

5.1 Operational Amplifier No. 1 (OpAmp1)

The operational amplifier (denoted as OpAmp1) used in the Continuous Time State Variable filter is illustrated in Figure 8. This OpAmp was the first of the original ITC'97 benchmark circuits. The SPICE file and the detailed results from fault simulations are included in Appendix 1. The fault simulation results indicate that fault detection is a function of the clock frequency of the BIST system. To illustrate this, look at the fault simulation results for OpAmp 1. OpAmp 1 had an overall fault coverage of 100% with no parameter variation. The faults considered in OpAmp 1 included eight transistor stuck-off (simulated by a 10MΩ resistor in series with either the drain or the source) and stuck-on (simulated as 1Ω across the source and drain). The only other components are 2 resis-

tors and 1 capacitor with stuck-open and stuck-short faults for each. For OpAmp 1, fault coverage increases from 90% at a clock frequency of 100Hz to 100% at clock frequencies of 100KHz and beyond, as shown in Figure 9.

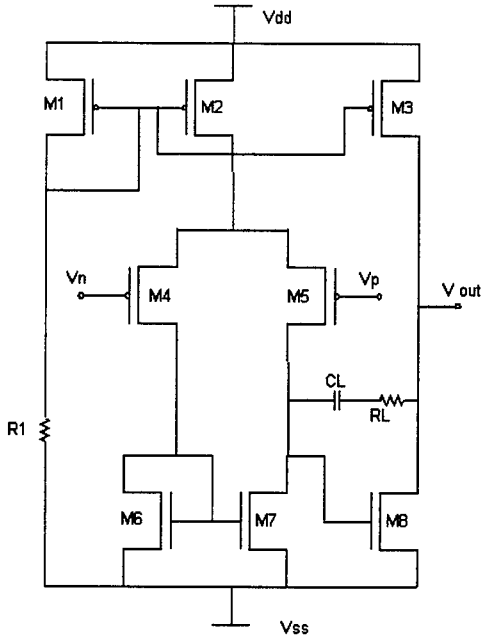

Figure 8. Operational Amplifier 1 (OpAmp1)

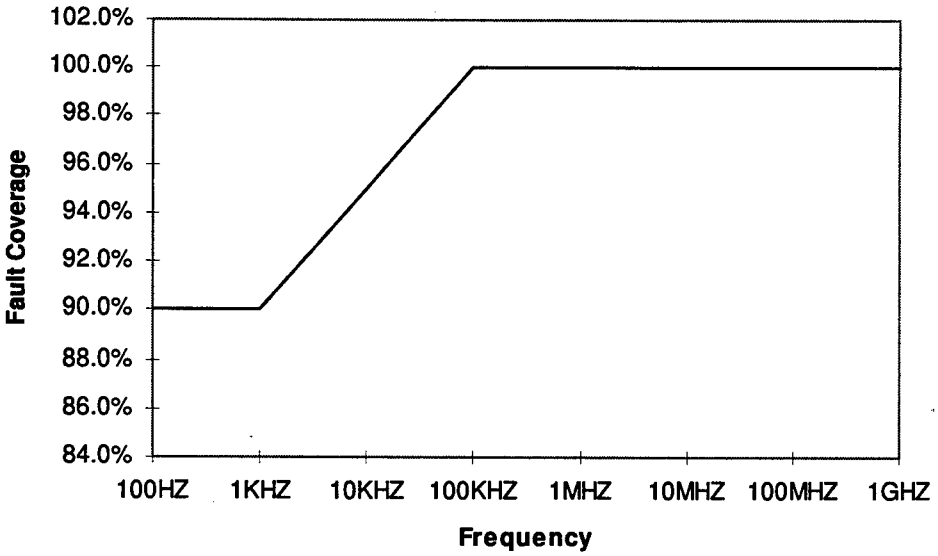

Figure 9. OpAmp1: Fault Coverage Versus Frequency

The fault simulation results also indicate that there is a correlation between the type of test waveform and type of CUT in terms of the resultant fault coverage. Looking at the results of the simulations for OpAmp1 with component variation in Appendix 1, this trend in the relationship between waveform and fault coverage is noticeable. The count waveforms, LFSR and the bit reversal of these waveforms, in general, acquire higher fault coverage per fault than the frequency sweep waveforms. This has been observed as a general trend for amplifier type circuits.

5.2 Continuous Time State Variable Filter

The Continuous Time State Variable filter (denoted as CTfilter) was the second of the original ITC'97 benchmark circuits and is illustrated in Figure 10. The SPICE file and detailed results from fault simulations are included in Appendix 2.

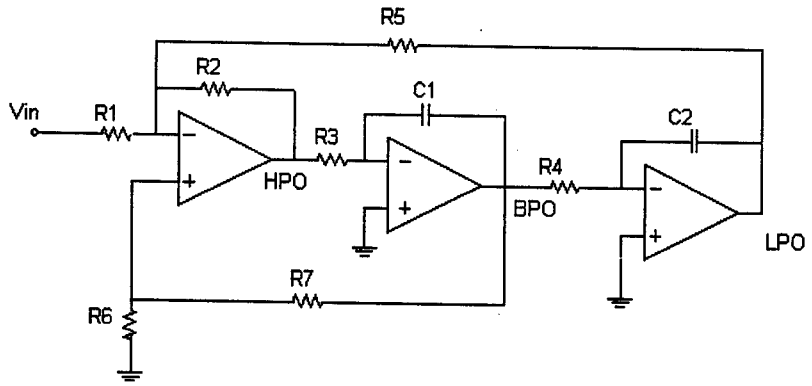

Figure 10. Continuous Time State Variable Filter

The CTfilter proved to be one of the most interesting benchmark circuits to study. While the CTfilter yielded an overall fault coverage of 100% on external components with no component variation, the detection of faults in this circuit was much more sensitive to clock frequency than any other. In addition, the use of the frequency sweep waveforms was much more effective in detecting faults than other waveforms used, as can be seen in Appendix 2 and in Figure 11 where the fault coverage is plotted as a function of BIST system clock frequency for each test waveform. The only waveforms to detect all the external faults in the CTfilter was the frequency sweep waveform with constant amplitude and its bit reversal at a clock frequency of 100MHz. This was observed to be a general trend in filter type circuits. Figure 12 shows the cumulative fault coverage (across all test waveforms) for the CTfilter as a function of the BIST system clock frequency.

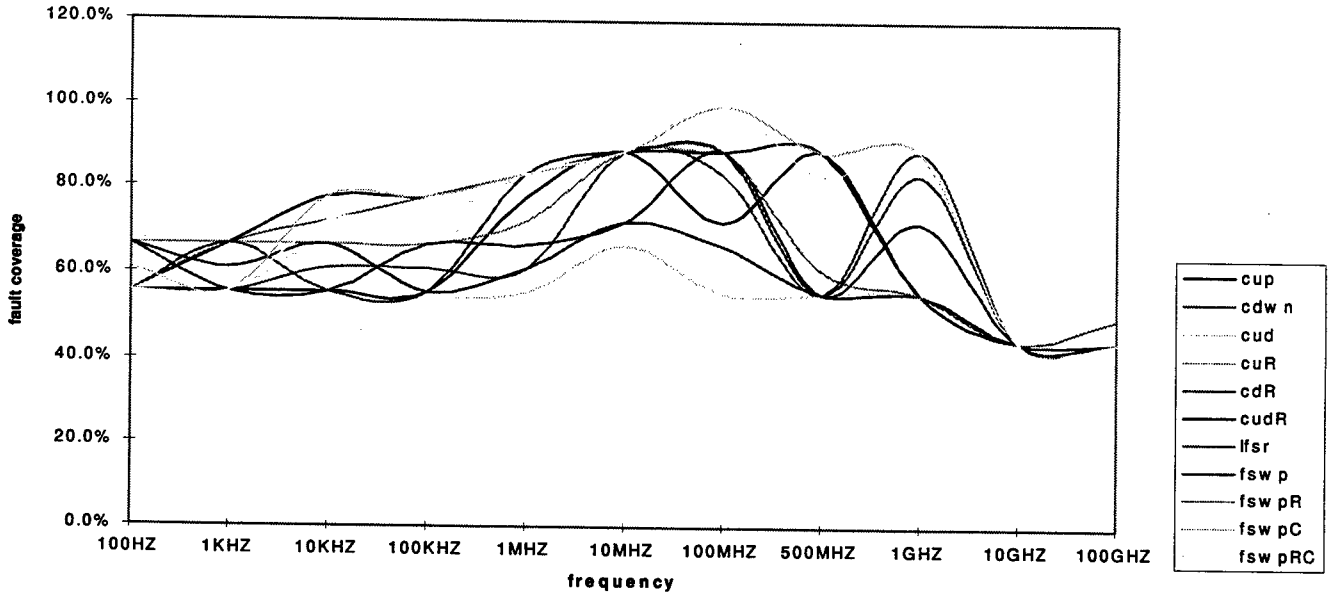

Figure 11. Fault Coverage Per Waveform Versus Frequency for CTFilter

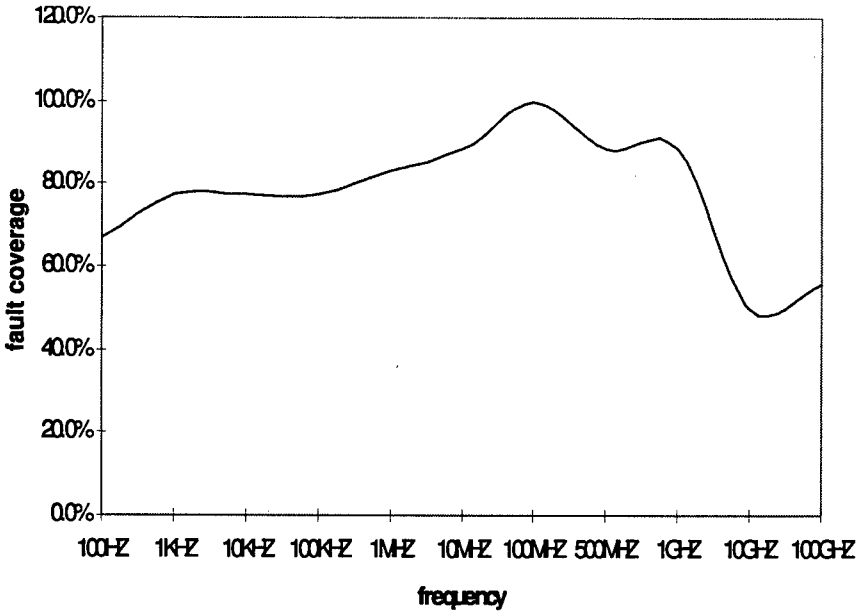

Figure 12. Overall Fault Coverage Versus Frequency for CTFilter

Although the frequency of the clock driving the TPG and ORA (as well as the DAC and ADC) in the system effected the fault coverage of the CTfilter, the *N* parameter that controls programmable shift registers for the frequency sweep waveforms had no effect on fault coverage. In the varying amplitude frequency sweep, the value of *N* controls the amount the amplitude increases and the period decreases each half cycle of the square wave, while *N* controls only the period in the constant amplitude frequency sweep. This data can be seen in Appendix 2.5.

The CTfilter was the largest circuit in which all hard faults, external and internal, were simulated. As mentioned before, SFA needs a flattened circuit in order to perform valid fault simulations. Therefore, Appendix 2.6 gives the flattened version of the CTFilter and Appendix 2.7 gives the complete list of the 84 hard faults in this circuit. Appendices 2.8 and 2.9 give the fault simulation results. With component parameter variation, the full CTFilter circuit had a fault coverage of 97.4%, almost as high as the external components alone. One important note in this simulation is that the constant amplitude frequency waveform and its bit reversal mode detected almost all simulations of all faults. The fault coverage with only these two waveforms exceeded 95% for all hard faults in the CTFilter, which re-enforces the trends seen in the fault simulation results with the external components alone.

5.3 Operational Amplifier No. 2 (OpAmp2)

The operational amplifier used in the leap frog filter (denoted as OpAmp2) is illustrated in Figure 13. This OpAmp by itself was not considered as one of the original ITC'97 benchmark circuits but we included it since it is a common OpAmp design used in many analog circuits. As in the case of OpAmp1, the counter-based test waveforms and the LFSR test waveform obtained higher fault coverage than the frequency sweep waveforms. However, OpAmp2 appeared to be less sensitive to the BIST system clock frequency than OpAmp1. The SPICE file and detailed results from the fault simulations are located in Appendix 3.

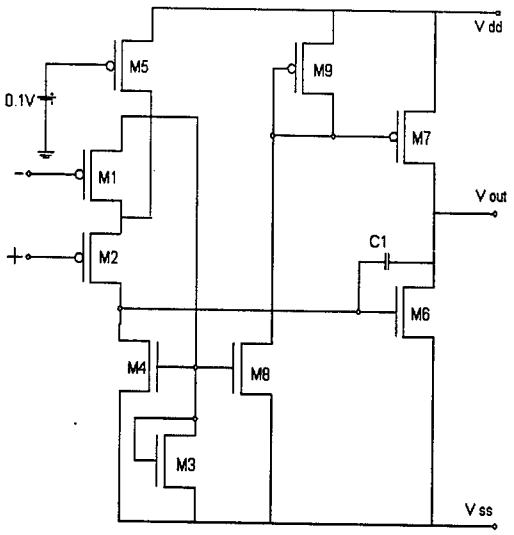

Figure 13. Operational Amplifier 2 (OpAmp2)

5.4 Leap Frog Filter

Another ITC'97 benchmark circuit studied and included in the proposed set of benchmark circuits was the Leap Frog filter. This circuit is a large circuit with six OpAmps (all of which are the design used in OpAmp2) as illustrated in Figure 14. The SPICE file and detailed results from the fault simulations are located in Appendix 4. The Leap Frog filter was much less sensitive to clock frequency than the CTfilter. With no variation, all faults were detected at every clock frequency run, but the importance of the various test waveforms is evident for the Leap Frog filter, as well. Observing the fault coverage per waveform for different frequencies in Appendix 4.2, it can be seen that the frequency sweep test waveforms consistently provide higher fault coverage than the counter/LFSR functions for the Leap Frog filter as was the case with the CTfilter. Here again the trend is observed - frequency sweep waveforms provide higher fault detection capabilities for filter circuits.

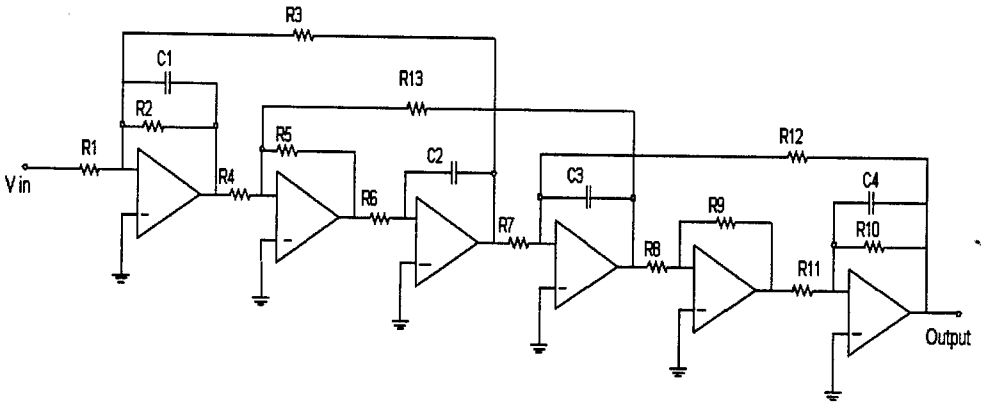

Figure 14. Leap Frog Filter

5.5 Differential Pair Circuit

The differential pair benchmark circuit was obtained from the SFA documentation and is

shown in Figure 15. It is one of two circuits included in the proposed set of benchmark circuits that incorporates BJTs instead of MOSFETs. The SPICE file and detailed results from the fault simulations are located in Appendix 5. Looking at the data in Appendix 5.4 for fault simulations with component parameter variation for the frequency 100Hz, the same trend is observed as seen with the OpAmps. Specifically, the frequency sweep test waveforms overall have a much lower fault coverage when compared with the counter and LFSR test waveforms. Although this tends to be true for most amplifier type circuits, the importance of the frequency sweep test waveforms in amplifier circuits cannot be ruled out completely; especially in this circuit where there are many faults that are only potentially detected. The count and LFSR waveforms may detect a majority of the faults per waveform, but the frequency sweeps tend to help in detecting simulation iterations per fault that no count or LFSR test waveform can detect. Take the fault *q2lowbf* at 100KHz for both magnitude and difference summing together as an example (see Appendix 5.4.3). The highest detection probability for this fault is 40% with the constant amplitude frequency sweep test waveform, but the cumulative detection probability is 75%. This is because some waveforms detect different iterations for the *q2lowbf* fault. Faults like *q2lowbf* represent cases where the frequency sweep test waveforms may play a part in helping increase fault detection (and fault coverage) in amplifier type circuits, although not a major part of the fault coverage.

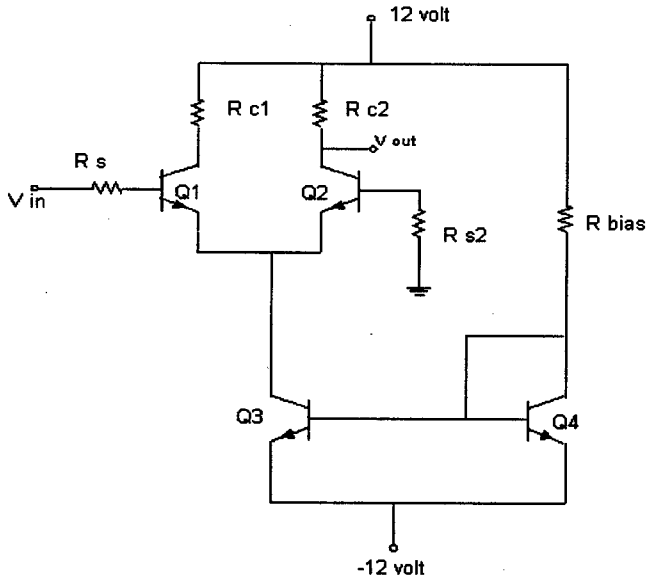

Figure 15. Differential Pair Circuit

5.6 Elliptical Filter

Another SFA circuit included as a benchmark circuit is the elliptical filter, shown in Figure 16. The SPICE file and detailed fault simulation results are located in Appendix 6. In the elliptical filter, only external hard faults have been simulated at this time, but consistent trends with the other filter circuits are evident. For example, in Appendix 6.3 with no component variation, much greater fault detection occurs with the frequency sweep test waveforms. At 1KHz, all four frequency sweep waveforms obtain 100% fault coverage of all external hard faults, but only two of the other seven counter/LFSR based test waveforms obtain 100% fault coverage.

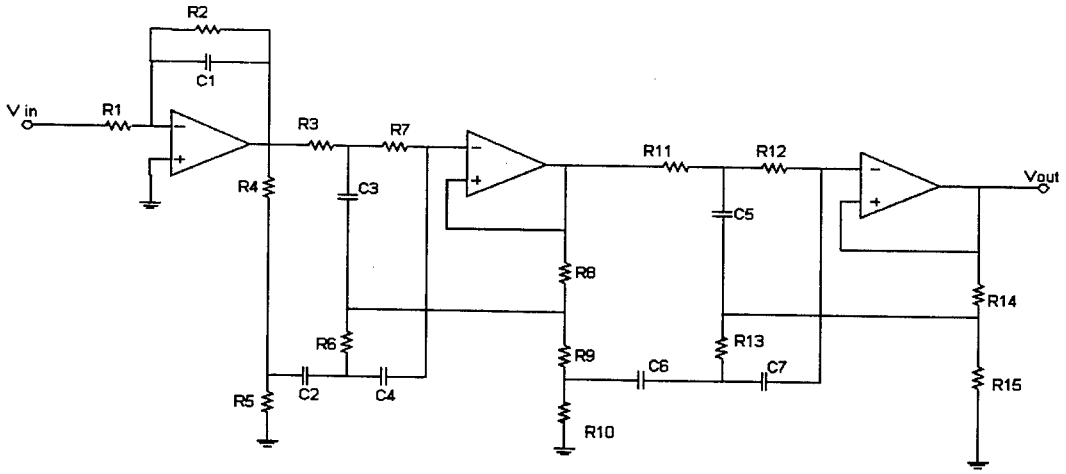

Figure 16. Elliptical Filter

5.7 Comparator

The next SFA benchmark circuit studied was the comparator, shown in Figure 17. The SPICE file and detailed results from simulations are located in Appendix 7. The comparator is of particular significance as part of the benchmark circuits since it represents one of the basic analog components in most ADC designs along with the basic DAC design that is included in the ITC'97 benchmark circuits (the remaining ADC components are all digital circuits). The comparator uses OpAmp2 as its base component, with the addition of three external resistors. As in the case of amplifier circuit, the counter and LFSR based test waveforms provided higher fault coverage results for the case with component parameter variation. But also of interest is how poorly the original frequency sweep waveforms (with varying amplitude) performed compared to the constant amplitude frequency sweep test waveforms. The constant amplitude frequency sweep obtained fault coverage practically as high as the other waveforms, while the original frequency sweep contributes very little to fault coverage. This is a tendency that is also evident in other circuits and may lead to the conclusion that the original frequency sweep waveforms could be eliminated from the digital BIST circuitry in most cases.

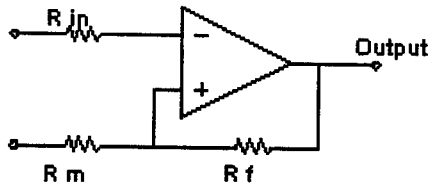

Figure 17. Comparator

5.8 Single Stage Common Emitter Amplifier

The last benchmark circuit obtained from the SFA documentation is the single-stage common-

emitter amplifier, shown in Figure 7. This circuit is the second of two BJT-based designs we have included the set of benchmark circuits. The SPICE file and detailed results from the fault simulations are included in Appendix 8. With the single stage amplifier, we investigated the effect of the number of Monte Carlo simulations per fault where we ran 10 in one case and 50 in the other. We found the number of Monte Carlo iterations have no effect for faults that were always detected. However, for potentially detected faults, we found the probability of detection to be higher for only 10 Monte Carlo iterations than for 50 iterations. Also we saw no significant change in the probability of detection beyond 50 iterations. While the probability of fault detection is optimistic for only 10 iterations, it is still gives a reasonable indication of the fault detection capability of the BIST approach and can be used for general analysis. Another observation is that some of the test waveforms proved to be less effective in detecting faults than others. Specifically, the bit reversal for some of the test waveforms (including bit reversal for count-up, count-down, and LFSR) were ineffective in detecting any additional faults. However, these waveforms were effective in detecting faults in other circuits.

5.9 Low-Pass Filter

The final benchmark circuit was a Low-Pass filter obtained from Lucent technologies and shown in Figure 18. The SPICE file and detailed results from fault simulations for this circuit are included in Appendix 9.

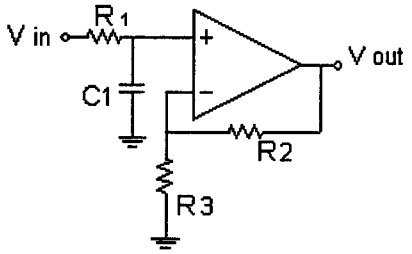

Figure 18. Low Pass Filter

The low-pass filter demonstrates how important it is to know what frequency to test a specific circuit at or to know to test specific circuits at a variety of frequencies. With component variation, the fault coverage goes from 83.7% at 1KHz to 100% at 1MHz. Notice that at 1KHz, the frequency sweep waveforms perform below average at detecting faults, but at 1MHz, the constant amplitude frequency sweep waveforms have the highest fault coverages per fault while the original frequency sweep waveforms have almost no fault detection capabilities. This suggests that the original frequency sweep should be replaced in the TPG design with the new constant amplitude waveforms.

5.10 Detection of Faults Causing Noise and Phase Shifts

The ORA mode of operation which sums the absolute value of the difference between the input (from the TPG) and output (analog CUT response) was intended to detect faults which lead to phase shifts and noise in an otherwise good circuit response. We investigated this by injecting a noise signal source in the CUT and varying the amplitude of the noise source with respect to the

amplitude of the input test waveform. Multiple Monte Carlo simulations were performed for each noise amplitude setting to facilitate component parameter variation. We compare the fault detection probability of the magnitude summing and the difference summing modes of operation in Figure 19. As can be seen, the difference summing mode can always detect noise greater than 5% of the input signal amplitude, while at the 5% noise amplitude, the magnitude summing mode has only about a 20% probability of detecting the fault causing the noise. Similarly, the difference summing mode can always detect phase shifts greater than 8% of the input period (or greater than 14 degrees or 0.25 radians).

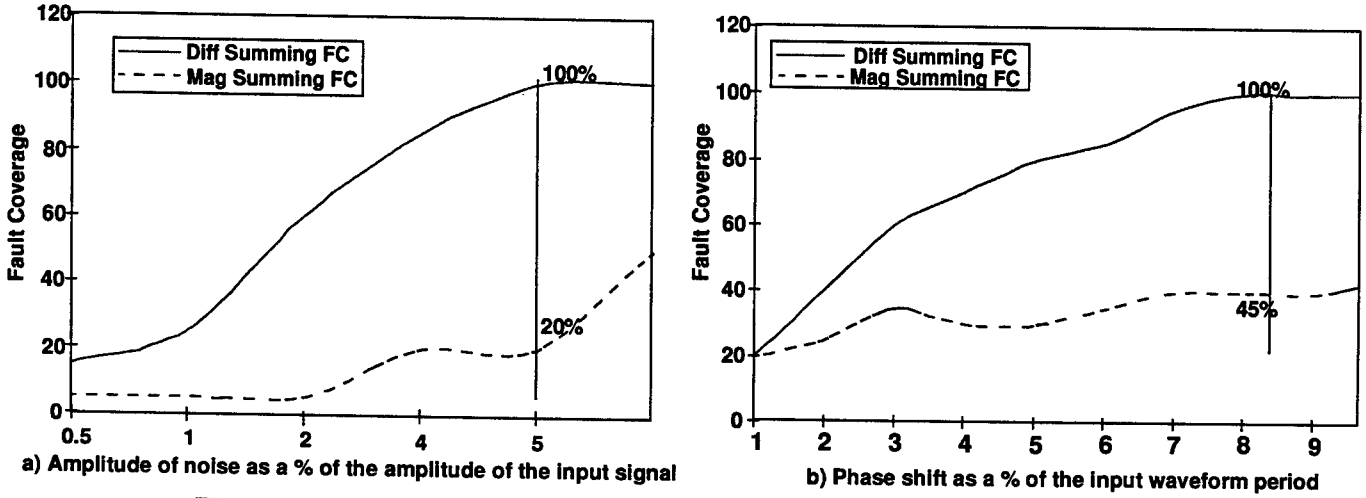

Figure 19. Noise and Phase Shift Detection with Difference Summing Mode

5.11 Summary of Experimental Results

The results discussed in this section and in shown in greater detail in the fault simulation data contained in the appendices showed that this BIST approach obtains high fault coverage on a variety of circuit types. A few of the major findings are the following:

- Including component variation is an important part of real-world testing of analog circuits.
- Analog circuits are sensitive to the clock frequency of the test waveforms.
- In general, filters obtain higher fault coverage with frequency sweep waveforms; however, amplifier type circuits obtain higher fault coverage with ramp and LFSR signals.
- The addition of the constant amplitude frequency sweep waveforms was an improvement and may suggest the replacement of the original frequency sweeps.
- The programmable shift register that controls the frequency sweep waveforms may be eliminated.
- The difference summing mode of the ORA provides much better detection of faults that cause noise or phase shifts on the output signal of the analog circuitry than the magnitude summing mode; however, both the magnitude summing and difference summing appear to be important in detecting catastrophic component faults.

6. Prototype Unit

A prototype unit was constructed to demonstrate the feasibility and viability of the mixed-signal BIST approach, to collect data that may be difficult to simulate, and to correlate physical data

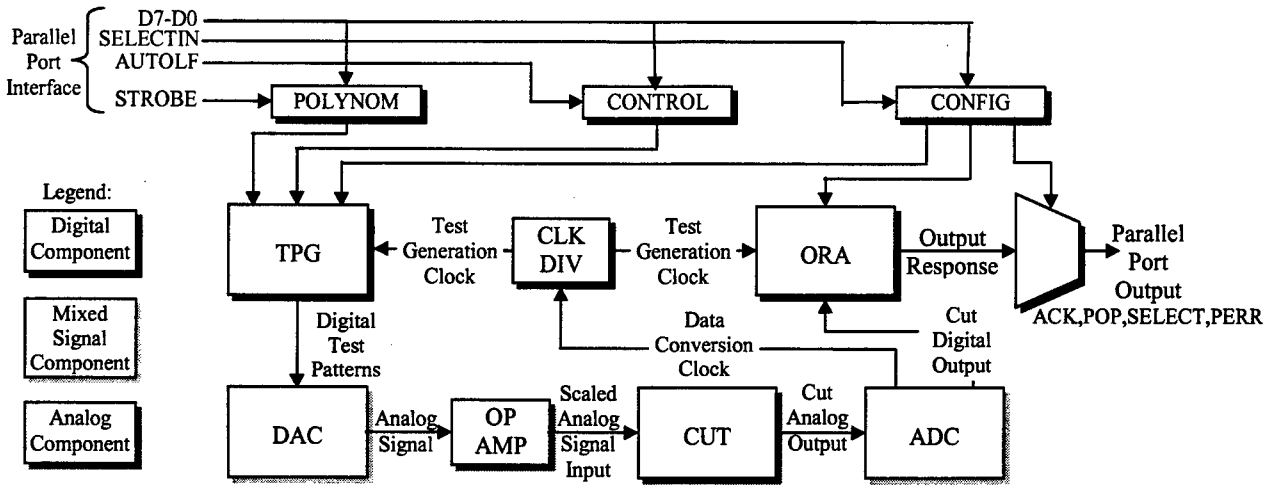

Figure 20. Block Diagram of Prototype Demonstration Unit

with simulation data. The prototype system integrates TPG and ORA 2 micron MOSIS TinyChips developed by students in an introductory VLSI design and testing class at the University of Kentucky. These ASICs are combined with off-the-shelf DAC and ADC and other basic digital components to provide the complete analog BIST prototype assembly. A control and observation interface has been included that allows two way communication between the prototype and a PC via a parallel port connection as illustrated in Figure 20. The prototype unit and the test sequences being applied to analog circuits under test are controlled by the user through the PC software by writing to one of three control registers whose bit maps are given in Table 5. These registers are written by applying the data to the data bus (D7-0) of the PC parallel port and activating the enable associated with that particular register.

Table 5: Prototype Unit Register Bit Maps

Register	Polynomial	Control	Configuration
Enable	Strobe	AutoLF	SelectIN
Bit 7 (msb)	P7	-	-
Bit 6	P6	Frequency Sweep	MSEL0
Bit 5	P5	Count down	MSEL1
Bit 4	P4	Bit reversal	M0
Bit 3	P3	Count up	M1
Bit 2	P2	Clear TPG	PSR0
Bit 1	P1	Counter/LFSR	PSR1
Bit 0 (lsb)	P0	Enable test	PSR2

The contents of the Polynomial register define the coefficients (P7-0) of the characteristic polynomial of the Linear Feedback Shift Register (LFSR) used to generate noise-like analog test patterns. The configuration is used to control the programmable shift register in the TPG for the frequency sweep function, the modes of operation of the ORA, and which nibble of the 16-bit accumulator will be read back by the PC. The value of PSR0-2 determines the length of the programmable shift register from 1 to 7 bits, which in turn controls the rate at which the frequency sweep generator sweeps through the frequencies. The value of M0-1 controls the mode of the ORA (00=clear ORA, 01=difference summing test, 10=magnitude summing test, and 11=digital test).

With this arrangement, analog test circuits can be subjected to the complete battery of test patterns available in the BIST circuitry.

The analog circuits under test that were implemented on the prototype unit include the DAC benchmark circuit in conjunction with an OpAmp and an ADC that uses the comparator benchmark circuit with an adaptive counter and a second DAC. The output of the DAC is fed through the single stage Common-Emitter Amplifier benchmark circuit and the Low Pass filter benchmark circuit. From there the output of any one of the three CUTs can be fed into the ADC for compaction by the ORA. The resultant BIST signatures for the three benchmark circuits implemented on the prototype unit fell within the range of good circuit signatures obtained from the simulation environment. Similarly, the BIST signatures obtained for stuck-open and stuck-short faults injected into components of the three circuits on the prototype unit also fell within the range of the faulty circuit signatures obtained from the simulation environment for each corresponding fault. Stuck-open faults were injected into the prototype unit by disconnecting a component terminal while stuck-short faults were emulated by placing a jumper wire across the terminals of a given component. These physical results support the validity of the results obtained from the simulation environment.

7. Participants and Publications

During the course of this project, the participants included two Dept. of EE faculty, three MSEE graduate students and three BSEE undergraduate students. Both faculty were US citizens while one of the graduate students was a US citizen with the other two graduate students being citizens of Sri Lanka and India, respectively. Two of the undergraduate students were US citizens with the third undergraduate student being a citizen of Malaysia. These participants are summarized below in terms of their contribution to the project as well as the time period during which they made their contribution:

Charles E. Stroud (Associate Professor) was responsible for the overall project coordination with particular emphasis on the BIST architecture, design, and evaluation throughout the entire project.

Eugene Bradley (Professor) was responsible for the analog and mixed-signal benchmark circuits used during evaluation of the BIST approach throughout the entire project.

Piyumani Karunaratna (Graduate Student under the direction of Charles Stroud) was responsible for the implementation and initial evaluation of the BIST architecture, helping to develop the overall test evaluation approach as well as developing software for the evaluation of the BIST approach. She joined the project in January of 1997 and received an MSEE degree in May 1998.

Kristi Maggard (Graduate Student under the direction of Charles Stroud) was responsible for the detailed evaluation of the BIST approach as well as contribution to the collection of the mixed-signal and analog benchmark circuits used to evaluate the BIST approach. She joined the project in January of 1998 and will receive an MSEE degree in May of 1999.

Ramakanth Kondigunturi (Graduate Student under the direction of Eugene Bradley) was responsible for the development of the mixed-signal and analog benchmark circuits that were used to evaluate the BIST approach. He joined the project in May of 1998 and will receive an MSEE degree in May of 1999.

Robert Puckett (Undergraduate Student under the direction of Charles Stroud) was responsible for the design and implementation of the Digital-to-Analog Converter (DAC) to be used in the prototype unit. He worked on the project from August 1997 to December 1997.

Brandon Lewis (Undergraduate Student under the direction of Charles Stroud) was responsible for the final design and implementation of the hardware and software for the prototype unit. He worked on the project form August 1998 to December 1998.

Sheac Yee Lim (Undergraduate Student under the direction of Charles Stroud) was responsible for the selection, implementation, and evaluation of three different analog benchmark circuits for the prototype unit. She worked on the project from November 1998 to March 1999.

The project has resulted in a number of paper and presentation submissions to conferences and workshops. The papers and presentations are summarized below along with invited presentations at industrial locations:

Conference Papers & Presentations:

1. C. Stroud, P. Karunaratna, and E. Bradley, "Digital Components for Built-In Self-Test of Analog Circuits", Proc. IEEE International Application Specific Integrated Circuits Conf., pp. 47-51, 1997.
2. K. Maggard and C. Stroud, "Built-In Self-Test for Analog Circuits in Mixed-Signal Systems", Proc. IEEE Southeast Regional Conf., pp. 225-228, 1999.
3. R. Kondagunturi, E. Bradley, K. Maggard, and C. Stroud, "Benchmark Circuits for Analog and Mixed-Signal Testing", Proc. IEEE Southeast Regional Conf., pp. 217-220, 1999.
4. B. Lewis, S. Lim, R. Puckett, and C. Stroud, "A Prototype Unit for Built-In Self-Test of Analog Circuits", Proc. IEEE Southeast Regional Conf., pp. 221-224, 1999.
5. C. Stroud, K. Maggard, P. Karunaratna, and R. Kondagunturi, "A Mixed-Signal Based Built-In Self-Test Approach for Analog Circuits", submitted to IEEE International Test Conf., 1999.

MSEE Theses:

1. P. Karunaratna, "Digital Components for Built-In Self-Test of Analog Circuits", MSEE Thesis, University of Kentucky, May, 1998.
2. K. Maggard, "A Mixed-Signal Based Built-In Self-Test Approach for Analog Circuits", MSEE Thesis, University of Kentucky, to be published May, 1999.
3. R. Kondagunturi, "Benchmark Circuits for Analog and Mixed-Signal Testing", MSEE Thesis, University of Kentucky, to be published May, 1999.

Workshop Presentations:

1. C. Stroud, P. Karunaratna, K. Maggard, and E. Bradley "A Mixed-Signal Based Built-In Self-Test Approach for Analog Circuits", presentation at Southeast Workshop on Mixed-Signal VLSI and Monolithic Sensors, Oak Ridge National Laboratory, April, 1998.
2. K. Maggard and C. Stroud, "Built-In Self-Test for Analog Circuits in Mixed-Signal Systems", presentation at Southeast Workshop on Mixed-Signal VLSI and Monolithic Sensors, Oak Ridge National Laboratory, April, 1999.
3. C. Stroud, R. Kondagunturi, K. Maggard, and E. Bradley, "Benchmark Circuits for Analog and Mixed-Signal Testing", presentation at Southeast Workshop on Mixed-Signal VLSI and Monolithic Sensors, Oak Ridge National Laboratory, April, 1999.

Invited Presentations:

1. C. Stroud, P. Karunaratna, K. Maggard, and E. Bradley, "A Mixed-Signal Based Built-In Self-Test Approach for Analog Circuits", presentation at Cypress Semiconductor, San Jose, CA, April, 1998.
2. C. Stroud, K. Maggard, P. Karunaratna, and E. Bradley, "A Mixed-Signal Based Built-In Self-Test Approach for Analog Circuits", presentation at Lucent Technologies Engineering Research Center, Princeton, NJ, November, 1998.

Journal Papers:

1. C. Stroud, P. Karunaratna, and K. Maggard, "A Mixed-Signal Based Built-In Self-Test Approach for Analog Circuits", in preparation for submission to either IEEE Design & Test of Computers or Journal of Electronic Testing: Theory and Applications.

8. Summary and Conclusions

The mixed-signal BIST architecture developed and evaluated during the course of this project has proven to be a viable solution to many of the problems that have been associated with analog testing in the past. This BIST approach, described in Section 2, has low area overhead and avoids performance penalties by modifying the analog CUT minimally, unlike many other analog DFT/ BIST testing methods. The proposed fault coverage formula for analog circuits in Section 3 provides a general method for analog fault coverage calculations, considers component parameter variation, and will allow easier and more accurate comparisons of future analog testing methods.

The fault simulation results in Section 5 using the benchmark circuits described in Section 4 lend insight to the practical applications of the BIST approach. First, this BIST method has proven to be an effective method for fault detection in a wide variety of analog circuits. The analog benchmark circuits under test allow for analog component parameter variation, which is an important and essential part of analog test evaluation. It was shown that without component variation, 100% of all faults simulated in the benchmarks were detected but when acceptable component parameter variations were added, the fault coverage of some circuits dropped. Even though this drop was observed, fault coverage remained above 95% in all circuits using the mixed-signal BIST approach. In digital systems, the typical minimum goal for manufacturing defect fault coverage is 95% of all single stuck-at gate level faults for most industrial applications. Therefore, the experimental analog fault coverage results obtained with this mixed-signal BIST approach are comparable to those sought and accepted in digital systems.

Fault simulation results also indicated that fault detection in analog circuits is a function of the clock frequency used to produce the test waveforms, compact the output responses, and for sampling in the DAC and ADC. This was observed in most circuits, but most obviously in the CTFilter where the only frequency at which 100% fault coverage was obtained was at 100MHz. In addition, 100% fault coverage was obtained only by the constant amplitude frequency sweep in this circuit. In all the benchmarks tested, a general trend emerged. Filter type circuits obtained higher fault coverage with frequency sweep waveforms, primarily the constant amplitude frequency sweep, while amplifier type circuits obtained higher fault coverage with the counter and LFSR based test waveforms. All of the test waveforms are important for general testing but, if area overhead in an ASIC becomes an issue, it might be beneficial to use a TPG design consisting of only the counter and

LFSR waveforms (along with their bit reversal modes) for amplifier type CUTs. Since the frequency sweep requires a majority of the TPG hardware and requires the longest testing time, including the entire TPG is the best choice for implementation of the BIST approach with filter type circuits; eliminating the counter and LFSR functions would only slightly reduce the area overhead but may also reduce total fault coverage. Furthermore, the constant amplitude frequency sweep should be implemented in place of the varying amplitude frequency sweep function. The constant amplitude can be implemented as a programmable value through the use of a magnitude register for greater testing flexibility or as a hard-wired value to minimize area overhead.

The effect of changing the *N* parameter that controls the programmable shift register in the frequency sweep hardware was studied mainly through the CTFilter. Since the CTFilter was the most sensitive of the benchmark circuits to changes in frequency and to waveform type, it was originally thought that it would also be sensitive to changes in this *N* parameter. However, the *N* parameter had no effect on the fault detection capabilities of the frequency sweep test waveforms. In order to make the decision of whether the shift register can be completely eliminated from the TPG, the relationship between test time and area overhead should be considered. As *N* and area overhead increases, test time decreases, as shown in Figure 21 such that a trade-off can be made between the area overhead and test time based on system objectives (from the table, *N*=3 appears to be the best choice in general).

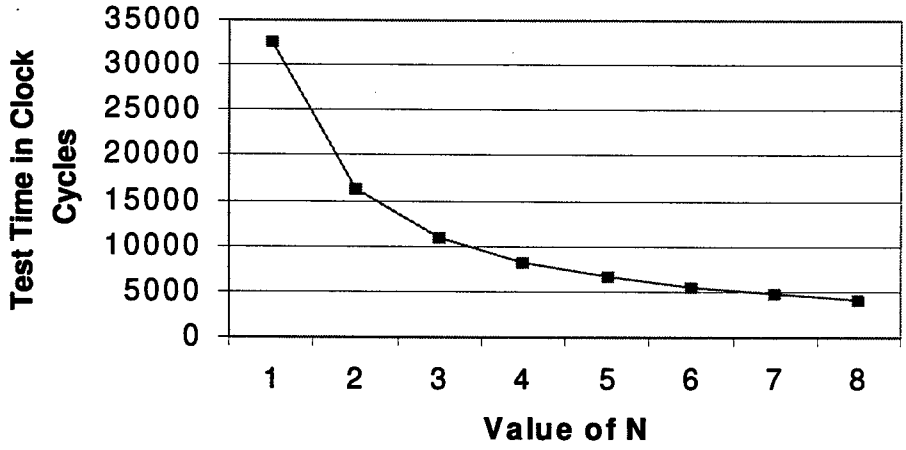

Figure 21. Test Time vs. Value of *N*

One final observation in architecture efficiency involves the ORA modes of operation. The difference summing mode of the ORA provides high detection probability for faults that cause noise or phase shifts in the analog output signal. However, both the magnitude summing and difference summing appear to be important in detecting catastrophic and parametric component faults. There were no outstanding cases where one mode of operation detected far more faults than the other mode, but the combination of both did produce higher fault coverages overall. Since both modes are important, one suggestion to reduce area overhead of the BIST circuitry is illustrated in Figure 22. In this modified BIST architecture, a differential amplifier in the analog domain would calculate the absolute value difference of the input test waveform and the output response of the analog CUT before the waveform reaches the ADC, and ultimately the ORA. This would reduce the area overhead of the ORA by eliminating the absolute value difference circuit (which consists of a full adder, a half adder, and an exclusive-OR gate for each bit of the ORA design). The addition

of an analog MUX before the ADC would allow the test controller to specify whether the difference summing mode or the magnitude summing mode would be chosen.

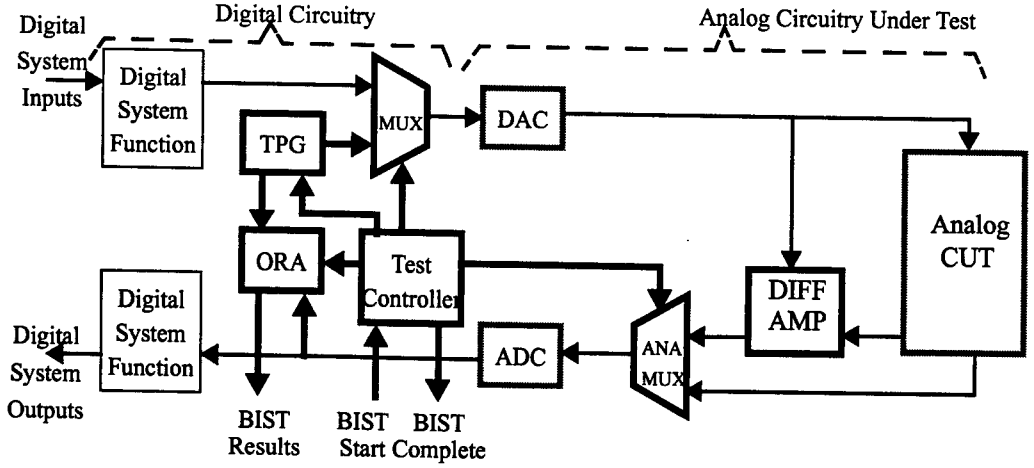

Figure 22. BIST Architecture for Mixed-Signal

In conclusion, the mixed-signal based BIST approach for analog circuits appears to be effective in detection of faults in analog circuits and ready for implementation in actual system applications. There are a number of areas that could be explored further for a better understanding of the potential capabilities and possible limitations of the technique. These include the following:

- Since the TGA and ORA functions could be used for digital BIST as well, there is potential for this BIST approach to be extended to provide complete testing of a mixed signal system including the digital domain as well as the analog domain.
- A more detailed investigation of soft faults could be undertaken to study the fault detection capability vs. the deviation from the acceptable parameter variation range (in other words, how "soft" of a fault can be detected).
- Functional fault models for OpAmps would significantly improve the fault simulation and analysis times. On possible approach would be pin faults using the series and parallel resistors for the hard fault models we included in the benchmark circuits. This would allow functional models to be used for OpAmp simulations in large circuits, like the Leap Frog filter. A detailed investigation of the correlation between this type of pin fault with hard and soft faults within the OpAmp would be needed to determine the validity of such as functional fault model.
- A standardized fault model for noise injection in analog circuits would be of value given that noise is of particular concern in mixed signal ASICs along with flicker noise in CMOS ASICs.
- Using the prototype demonstration unit we observed variations in the resultant good circuit signatures as a function of ambient temperature. This should be investigated more closely to determine if temperature changes cause the signature range to shift or to spread out. A similar situation was observed with changes in the power supply. Since these environmental variations can be expected to occur in a working system, the impact on the fault detection capability of this approach would provide valuable knowledge.

- The implementation of the BIST architecture as an Digital Signal Processor (DSP) algorithm is of interest (as suggested by engineers at Lucent Technologies Engineering Research Center as a result of the invited presentation) and may be one of the best implementation media for this BIST approach since the DAC/ADC are already contained on the device and the only area overhead for the approach would be the program memory need to implement the TPG and ORA algorithms.

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Appendix 1

OpAmp in Continuous Time State Variable Filter - OpAmp 1 (ITC'97)

A.1.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
*Operational amplifier
vck 100 0
vin 9 0
%dc 100 11 9
R1 1 14 [110,6.6]k
M1 1 1 99 99 modp1 L=4U W=150U
R2 99 13 1
R3 1 13 [100,0]meg
.model modp1 pmos(RS=[0,0])
M2 3 1 98 98 modp2 L=4U W=35U
R4 98 13 1
R5 3 13 [100,0]meg
.model modp2 pmos(RS=[0,0])
M3 9 1 97 97 modp3 L=4U W=100U
R6 9 13 1
R7 9 13 [100,0]meg
.model modp3 pmos(RS=[0,0])
M4 4 12 96 96 modp4 L=4U W=60U
R8 3 96 1
R9 4 96 [100,0]meg
.model modp4 pmos(RS=[0,0])
M5 5 11 95 95 modp5 L=4U W=60U
R10 95 3 1
R11 5 95 [100,0]meg
.model modp5 pmos(RS=[0,0])
cl 5 16 [1.27,.0762]pf
R12 5 16 [100,0]meg
R13 16 6 1
Rl 6 9 [8.75,0.525]k
M6 4 4 94 94 modn6 L=4U W=27.5U
R14 94 14 1
R15 4 94 [100,0]meg
.model modn6 nmos(RD=[0,0])
M7 5 4 93 93 modn7 L=4U W=27.5U
R16 93 14 1
R17 5 93 [100,0]meg
.model modn7 nmos(RD=[0,0])
M8 9 5 92 92 modn8 L=4U W=100U
R18 92 14 1
R19 9 92 [100,0]meg
.model modn8 nmos(RD=[0,0])
```

```
VDD 13 0 5
VSS 14 0 -5
RL 18 0 0
Co 16 0 2e-12
.print tran v(100) v(11) v(9)
.options nopage noecho nomod numdgt=3
.end
```

A.1.2 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the OpAmp1 circuit.

```
#R1 .01 1 R1_short
#R1 1e7 1 R1_open
#RL .01 1 RL_short
#RL 1e4 1 RL_open
#CL 1e4f 1 C1_open
#CL .001nf 1 C1_short
#modp1 1e7 1 m1_off RS
#modp2 1e7 1 m2_off RS
#modp3 1e7 1 m3_off RS
#modp4 1e7 1 m4_off RS
#modp5 1e7 1 m5_off RS
#modn6 1e7 1 m6_off RD
#modn7 1e7 1 m7_off RD
#modn8 1e7 1 m8_off RD
#R3 1 1 m1_on
#R5 1 1 m2_on
#R7 1 1 m3_on
#R9 1 1 m4_on
#R11 1 1 m5_on
#R15 1 1 m6_on
#R17 1 1 m7_on
#R19 1 1 m8_on
```

A.1.3 Soft Fault List Supplied to SFA

This fault list is used to simulate all soft faults in the OpAmp1 circuit.

```
#C1 1.143e-11 1 c1_low
#C1 1.379e-11 1 c1_high
#RL 8225 1 RL_low
#RL 9275 1 RL_high
#R1 70400 1 R1_low
#R1 149600 1 R1_high
```

A.1.4 Simulation Results with No Component Variation - Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	10KHZ	100KHZ	1MHZ	10MHZ	100MHZ	1GHZ
R1short	0	0	1	1	1	1	1	1
R1open	0	0	0	1	1	1	1	1
RLshort	1	1	1	1	1	1	1	1
RLopen	1	1	1	1	1	1	1	1
CLshort	1	1	1	1	1	1	1	1
CLopen	1	1	1	1	1	1	1	1
M1off	1	1	1	1	1	1	1	1
M2off	1	1	1	1	1	1	1	1
M3off	1	1	1	1	1	1	1	1
M4off	1	1	1	1	1	1	1	1
M5off	1	1	1	1	1	1	1	1
M6off	1	1	1	1	1	1	1	1
M7off	1	1	1	1	1	1	1	1
M8off	1	1	1	1	1	1	1	1
M1on	1	1	1	1	1	1	1	1
M2on	1	1	1	1	1	1	1	1
M3on	1	1	1	1	1	1	1	1
M4on	1	1	1	1	1	1	1	1
M5on	1	1	1	1	1	1	1	1
M6on	1	1	1	1	1	1	1	1
M7on	1	1	1	1	1	1	1	1
M8on	1	1	1	1	1	1	1	1
	90.9%	90.9%	95.5%	100.0%	100.0%	100.0%	100.0%	100.0%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	Cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100Hz	90.9%	90.9%	90.9%	90.9%	90.9%	90.9%	86.4%	90.9%	90.9%	90.9%	90.9%
1KHz	90.9%	90.9%	90.9%	90.9%	90.9%	90.9%	86.4%	90.9%	90.9%	90.9%	90.9%
10KHz	95.5%	90.9%	90.9%	95.5%	95.5%	95.5%	90.9%	95.5%	95.5%	95.5%	95.5%
100KHz	95.5%	95.5%	95.5%	95.5%	95.5%	95.5%	90.9%	95.5%	95.5%	100%	100%
1MHz	100%	100%	100%	95.5%	100%	100%	95.5%	100%	100%	100%	100%
10MHz	95.5%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100MHz	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1GHz	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.1.5 Simulation Results with No Component Variation - Soft Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100KHZ
C1low	1
C1high	1
RLlow	1
RLhigh	1
R1low	1
R1high	1
	100%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	Lfsr	fswp	fswpR	fswpC	fswprc
100KHz	100%	100%	66.7%	100%	100%	100%	100%	100%	100%	100%	100%

A.1.6 Simulation Results with Component Variation - Hard Faults

A.1.6.1 Simulation Results at 100KHz, 10 seeds

Overall Fault Coverage = (21*1+.7)/22 = 98.6%

Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fspwr	fswpc	fswprc
R1short	0%	0%	0%	40%	100%	40%	0%	10%	10%	10%	10%
R1open	10%	40%	10%	100%	100%	100%	100%	0%	0%	10%	0%
RLshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	0%	100%	30%	100%
CLshort	20%	0%	20%	30%	30%	30%	20%	0%	0%	10%	0%
CLopen	30%	20%	0%	80%	100%	70%	0%	30%	30%	10%	30%
M1off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	50%	100%	10%	50%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%
M5off	100%	100%	100%	100%	100%	100%	100%	0%	100%	10%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	40%	70%	10%	100%
M8off	100%	100%	100%	100%	40%	100%	100%	0%	100%	0%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
R1short	0%	0%	0%	40%	100%	40%	0%	10%	10%	10%	10%
R1open	10%	40%	10%	100%	100%	100%	100%	0%	20%	30%	20%
RLshort	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	30%	100%
CLshort	20%	0%	20%	30%	30%	30%	20%	0%	10%	10%	0%
CLopen	30%	20%	0%	80%	100%	70%	0%	30%	0%	20%	30%
M1off	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	50%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	0%
M5off	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	100%
M8off	100%	100%	100%	100%	40%	100%	100%	0%	0%	0%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	90%	0%	0%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc	total
R1short	0%	0%	0%	40%	100%	40%	0%	10%	20%	10%	10%	100%
R1open	10%	40%	10%	100%	100%	100%	100%	0%	20%	30%	20%	100%
RLshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	100%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	0%	100%	30%	100%	100%
CLshort	20%	0%	20%	30%	30%	30%	20%	0%	10%	10%	0%	70%
CLopen	30%	20%	0%	80%	100%	70%	0%	30%	30%	20%	30%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	50%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	0%	100%	10%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	100%	70%	10%	100%	100%
M8off	100%	100%	100%	100%	40%	100%	100%	0%	100%	0%	100%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Appendix 2
Continuous Time State Variable Filter (ITC'97)

A.2.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
*Continuous-time state-variable filter
vck 100 0
vin 14 0
%dc 100 14 13
.subckt OpAmp 9 11 12 13 14
R1 1 14 [110,6.6]k
M1 1 1 99 99 PMOS L=4U W=150U
R2 99 13 1
R3 1 13 1meg
M2 3 1 98 98 PMOS L=4U W=35U
R4 98 13 1
R5 3 13 1meg
M3 9 1 97 97 PMOS L=4U W=100U
R6 97 13 1
R7 9 13 1meg
M4 4 12 96 96 PMOS L=4U W=60U
R8 3 96 1
R9 4 96 1meg
M5 5 11 95 95 PMOS L=4U W=60U
R10 95 3 1
R11 5 95 1meg
cl 5 16 [1.27,0.127]pf
R12 5 16 1meg
R13 16 6 1
RL 6 9 [8.75,.525]k
M6 4 4 94 94 NMOS L=4U W=27.5U
R14 94 14 1
R15 4 94 1meg
M7 5 4 93 93 NMOS L=4U W=27.5U
R16 93 14 1
R17 5 93 1meg
M8 9 5 92 92 NMOS L=4U W=100U
R18 92 14 1
R19 9 92 1meg
.MODEL NMOS NMOS LEVEL=3
+VTO=.79 GAMMA=.38 PHI=.53 RD=63 IS=1E-16 PB=.8 CGSO=1.973E-10
+CGDO=1.973E-10 RSH=45 CJ=0.00029 MJ=.486 CJSW=3.3E-10 MJSW=.33 JS=0.0001
+TOX=2.5E-08 NSUB=8.7E+15 NFS=8.2E+11 TPG=1 XJ=1E-07 LD=7E-08 UO=577
+VMAX=150000 FC=.5 DELTA=.3551 THETA=0.046 ETA=.16 KAPPA=0.05
.MODEL PMOS PMOS LEVEL=3
+VTO=-8.40000000E-01 GAMMA=.53 PHI=.58 RD=94 RS=94 IS=1E-16 PB=.8
```

```
+CGSO=3.284E-10 CGDO=3.284E-10 RSH=100 CJ=0.00041 MJ=.54 CJSW=3.4E-10
MJSW=.3
+JS=0.0001 TOX=2.5E-08 NSUB=1.75E+16 NFS=8.4E+11 TPG=1 XJ=0 LD=6E-08 UO=205
+VMAX=500000 FC=.5 DELTA=.4598 THETA=.14 ETA=.17 KAPPA=10
.ends OpAmp

*EXTERNAL CIRCUIT
Vss 0 18 5.0
Vdd 19 0 5.0
Xopamp1 11 2 1 19 18 OpAmp
Xopamp2 12 0 3 19 18 OpAmp
Xopamp3 13 0 4 19 18 OpAmp
R1 14 1 [10,0.3]k
R2 1 11 [10,0.3]k
R3 11 3 [10,0.3]k
R4 12 4 [10,0.3]k
R5 1 13 [10,0.3]k
R6 2 0 [3,0.09]k
R7 12 2 [7,0.21]k
C1 3 12 [20,1.6]n
C2 4 13 [20,0.6]n
.print tran v(100) v(14) v(13)
.options nopage noecho nomod numdgt=3
.end
```

A.2.2 Hard Fault List Supplied to SFA

This fault list is used to simulate *only external* hard faults in the Continuous Time Filter; no soft faults have been simulated at this time.

```
#R1 1e7 1 r1_open
#R1 .01 1 r1_short
#R2 1e7 1 r2_open
#R2 .01 1 r2_short
#R3 1e7 1 r3_open
#R3 .01 1 r3_short
#R4 1e7 1 r4_open
#R4 .01 1 r4_short
#R5 1e7 1 r5_open
#R5 .01 1 r5_short
#R6 1e7 1 r6_open
#R6 .01 1 r6_short
#R7 1e7 1 r7_open
#R7 .01 1 r7_short
#C1 1e4f 1 c1_open
#C1 .001nf 1 c1_short
#C2 1e4f 1 c2_open
#C2 .001nf 1 c2_short
```

A.2.3 Simulation Results with No Component Variation - External Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	10KHZ	100KHZ	1MHZ	10MHZ	100MHZ	500MHZ	1GHZ	10GHZ
r1open	1	1	1	1	1	1	1	1	1	1
r1short	1	1	1	1	1	1	1	1	1	1
r2open	1	1	1	1	1	1	1	1	1	1
r2short	1	1	1	1	1	1	1	1	1	1
r3open	1	1	1	1	1	1	1	1	1	1
r3short	1	1	1	1	1	1	1	1	1	1
r4open	1	1	1	1	1	1	1	1	1	0
r4short	0	1	1	1	1	1	1	1	1	0
r5open	1	1	1	1	1	1	1	1	1	1
r5short	1	1	1	1	1	1	1	1	1	1
r6open	0	0	0	0	1	1	1	1	1	1
r6short	0	0	0	0	0	1	1	1	1	0
r7open	0	1	1	1	1	1	1	1	1	0
r7short	1	1	1	1	1	1	1	1	1	0
c1open	0	0	0	0	0	0	1	0	0	0
c1short	0	0	0	0	0	0	1	0	0	0
c2open	1	1	1	1	1	1	1	1	1	0
c2short	1	1	1	1	1	1	1	1	1	0
FC	66.7%	77.8%	77.8%	77.8%	83.3%	88.9%	100.0%	88.9%	88.9%	50.0%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswpRC	Total
100HZ	56%	56%	56%	67%	67%	67%	56%	56%	56%	61%	56%	66.7%
1KHZ	56%	56%	56%	67%	56%	61%	67%	67%	67%	56%	56%	77.8%
10KHZ	56%	61%	67%	67%	56%	67%	56%	78%	72%	78%	72%	77.8%
100KHZ	56%	61%	56%	67%	67%	56%	56%	78%	78%	78%	72%	77.8%
1MHZ	78%	61%	56%	72%	67%	61%	83%	83%	83%	83%	83%	83.3%
10MHZ	89%	89%	67%	89%	72%	72%	89%	89%	89%	89%	89%	88.9%
100MHZ	72%	83%	56%	89%	89%	67%	89%	89%	89%	100%	100%	100.0%
500MHZ	89%	56%	56%	89%	56%	56%	56%	89%	61%	89%	83%	88.9%
1GHZ	56%	89%	56%	56%	72%	56%	83%	56%	56%	89%	89%	88.9%
10GHZ	44%	44%	44%	44%	44%	44%	44%	44%	44%	44%	44%	50.0%

A.2.4 Simulation Results with Component Variation - External Hard Faults

A.2.4.1 Simulation Results at 100KHz, 10 seeds

Overall Fault Coverage = (12*1+2*0.7+4*0.8)/18 = 88.3%
Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fswpr	fswpc	fswprc
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	10%	10%	10%	10%	10%	20%	10%	10%	10%	0%	50%
r4short	10%	10%	10%	10%	10%	20%	10%	10%	10%	0%	50%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r6open	10%	0%	10%	20%	0%	20%	0%	0%	0%	0%	50%
r6short	10%	0%	10%	20%	0%	20%	0%	0%	0%	10%	50%
r7open	10%	0%	10%	20%	0%	20%	0%	0%	0%	0%	50%
r7short	10%	0%	10%	10%	0%	20%	0%	0%	10%	10%	50%
c1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	30%
c1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	80%	30%
c2open	80%	70%	20%	20%	70%	10%	70%	20%	20%	20%	100%
c2short	80%	70%	20%	20%	70%	20%	60%	20%	20%	20%	100%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	100%
r2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	80%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	70%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	70%	100%	100%
r4open	30%	30%	10%	10%	10%	20%	10%	40%	40%	30%	20%
r4short	30%	30%	10%	10%	10%	20%	10%	40%	40%	30%	20%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5short	100%	70%	100%	100%	100%	100%	100%	100%	100%	80%	100%
r6open	20%	10%	20%	20%	0%	10%	20%	10%	20%	10%	30%
r6short	20%	10%	20%	20%	0%	10%	20%	10%	20%	10%	30%
r7open	20%	10%	20%	20%	0%	10%	20%	10%	20%	10%	30%
r7short	20%	10%	20%	10%	0%	10%	20%	10%	20%	10%	30%
c1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	20%	20%
c1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	20%	20%
c2open	100%	100%	80%	100%	100%	100%	100%	100%	100%	90%	100%
c2short	100%	100%	80%	100%	100%	100%	100%	100%	100%	90%	100%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	Total
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	30%	40%	10%	10%	10%	20%	10%	50%	50%	30%	50%	70%
r4short	30%	40%	10%	10%	10%	20%	10%	50%	50%	30%	50%	70%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	20%	100%	100%	100%
r5short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r6open	20%	10%	20%	20%	0%	20%	20%	10%	20%	10%	50%	80%
r6short	20%	10%	20%	20%	0%	20%	20%	10%	20%	20%	50%	80%
r7open	20%	10%	20%	20%	0%	20%	20%	10%	20%	10%	50%	80%
r7short	20%	10%	20%	10%	0%	20%	20%	10%	30%	20%	50%	80%
c1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	50%	100%
c1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	50%	100%
c2open	100%	100%	80%	100%	100%	100%	100%	100%	100%	90%	100%	100%
c2short	100%	100%	80%	100%	100%	100%	100%	100%	100%	90%	100%	100%

A.2.4.2 Simulation Results at 100MHz, 10 seeds

Overall Fault Coverage = (14*1+4*0.9)/18 = 97.8%

Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	90%	100%	100%	90%	100%	100%	100%	20%	70%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	0%	10%	0%	0%	10%	0%	0%	0%	0%	50%	50%
r4short	0%	10%	0%	0%	0%	0%	0%	0%	0%	50%	50%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%
r5short	100%	20%	100%	100%	20%	100%	20%	100%	100%	100%	100%
r6open	10%	10%	0%	20%	0%	10%	10%	10%	10%	50%	50%
r6short	20%	10%	0%	20%	0%	10%	10%	20%	10%	50%	50%
r7open	10%	10%	10%	20%	0%	10%	10%	20%	10%	50%	50%
r7short	10%	10%	0%	20%	0%	10%	10%	10%	10%	50%	50%
c1open	0%	30%	0%	0%	30%	0%	30%	0%	0%	30%	30%
c1short	0%	30%	0%	0%	30%	0%	30%	0%	0%	30%	30%
c2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	80%	100%
c2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	80%	100%

Difference in Input and Output Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fswpr	fswpc	fswprc
c1low	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1open	100%	0%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	0%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	0%	100%	100%	100%	100%	100%	100%	40%	30%	100%
r2short	90%	0%	100%	90%	100%	100%	100%	80%	10%	30%	100%
r3open	100%	0%	100%	100%	100%	100%	100%	100%	100%	30%	100%
r3short	100%	0%	100%	100%	100%	100%	100%	100%	100%	30%	100%
r4open	0%	10%	0%	0%	0%	0%	0%	50%	0%	30%	20%
r4short	0%	10%	0%	0%	0%	0%	10%	50%	0%	50%	20%
r5open	100%	0%	100%	100%	0%	100%	100%	100%	100%	100%	100%
r5short	100%	40%	100%	100%	20%	100%	20%	100%	100%	100%	100%
r6open	10%	10%	0%	20%	0%	10%	10%	60%	20%	40%	30%
r6short	20%	10%	0%	20%	0%	10%	10%	20%	20%	40%	30%
r7open	10%	10%	10%	20%	0%	10%	0%	30%	30%	40%	30%
r7short	10%	10%	0%	20%	0%	10%	10%	50%	20%	40%	30%
c1open	0%	40%	0%	0%	30%	0%	30%	60%	10%	60%	20%
c1short	0%	40%	0%	0%	30%	0%	30%	60%	0%	50%	20%
c2open	100%	0%	100%	100%	30%	100%	0%	100%	100%	100%	100%
c2short	100%	0%	100%	100%	20%	100%	40%	100%	100%	100%	100%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	total
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	90%	100%	100%	90%	100%	100%	100%	80%	70%	100%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	0%	20%	0%	0%	10%	0%	0%	50%	0%	80%	50%	100%
r4short	0%	20%	0%	0%	0%	0%	10%	50%	0%	80%	50%	90%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5short	100%	60%	100%	100%	20%	100%	20%	100%	100%	100%	100%	100%
r6open	10%	20%	0%	20%	0%	10%	10%	70%	20%	60%	50%	100%
r6short	20%	20%	0%	20%	0%	10%	10%	40%	20%	60%	50%	90%
r7open	10%	20%	10%	20%	0%	10%	10%	50%	30%	60%	50%	90%
r7short	10%	20%	0%	20%	0%	10%	10%	60%	20%	60%	50%	90%
c1open	0%	70%	0%	0%	30%	0%	30%	60%	10%	70%	30%	100%
c1short	0%	70%	0%	0%	30%	0%	30%	60%	0%	70%	30%	100%
c2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.2.5 Simulation Results for Varied Values of *N* in FSWP modes

A.2.5.1 Simulation Results at 100MHz - External Hard Faults Only

Fault Coverage with Individual Fault Versus Value of *N*

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

N	1	2	3	5	6	7
r1open	1	1	1	1	1	1
r1short	1	1	1	1	1	1
r2open	1	1	1	1	1	1
r2short	1	1	1	1	1	1
r3open	1	1	1	1	1	1
r3short	1	1	1	1	1	1
r4open	1	1	1	1	1	1
r4short	1	1	1	1	1	1
r5open	1	1	1	1	1	1
r5short	1	1	1	1	1	1
r6open	1	1	1	1	1	1
r6short	1	1	1	1	1	1
r7open	1	1	1	1	1	1
r7short	1	1	1	1	1	1
c1open	1	1	1	1	1	1
c1short	1	1	1	1	1	1
c2open	1	1	1	1	1	1
c2short	1	1	1	1	1	1
FC	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Fault Coverage with Value of *N* Versus Waveform

	cup	Cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswpRC
1	72.2%	83.3%	55.6%	100.0%	88.9%	66.7%	88.9%	88.9%	88.9%	100.0%	100.0%
2	72.2%	83.3%	55.6%	100.0%	88.9%	66.7%	88.9%	88.9%	88.9%	100.0%	100.0%
3	72.2%	83.3%	55.6%	100.0%	88.9%	66.7%	88.9%	88.9%	88.9%	100.0%	100.0%
5	72.2%	83.3%	55.6%	100.0%	88.9%	66.7%	83.3%	88.9%	88.9%	100.0%	100.0%
6	72.2%	83.3%	66.7%	100.0%	88.9%	66.7%	88.9%	88.9%	88.9%	100.0%	100.0%
7	72.2%	83.3%	55.6%	100.0%	88.9%	66.7%	88.9%	88.9%	88.9%	100.0%	100.0%

A.2.5.2 Simulation Results at 100Hz - External Hard Faults Only

Fault Coverage with Individual Fault Versus Value of *N*

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

N	1	3	7
r1open	1	1	1
r1short	1	1	1
r2open	1	1	1
r2short	1	1	1
r3open	1	1	1
r3short	1	1	1
r4open	1	1	1
r4short	1	1	1
r5open	1	1	1
r5short	1	1	1
r6open	0	0	0
r6short	0	0	0
r7open	1	1	1
r7short	1	1	1
c1open	0	0	0
c1short	0	0	0
c2open	1	1	1
c2short	1	1	1
FC	77.8%	77.8%	77.8%

Fault Coverage with Value of *N* Versus Waveform

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswpRC
N=1	56%	61%	56%	67%	67%	56%	78%	78%	78%	78%	72%
N=3	56%	61%	56%	67%	67%	56%	56%	78%	78%	78%	72%
N=7	56%	61%	56%	67%	67%	56%	61%	78%	78%	78%	72%

A.2.6 Spice File with Fault Models for Simulation for flattened CTFilter

This file has been modified from the Hspice version on the UK VLSI Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer. The Continuous Time Filter has been flattened in order to use SFA to simulate all faults internal to the opamps; thus component names are different.

```
continous state time variable filter flattened
vck 100 0
vin 9 0
%dc 100 9 7

**************************************************
** opamp 1
c11 142 143 [1.27,.127]pf
r114a 138 145 [110,6.6]k
r114b 143 3 [8.75,0.525]k
*Transistor declarations
* with parallel resistors for short faults and RS/RD parameter for open faults
m117 139 138 137 137 modp1 L=4.0u w=35u
rm117 137 139 [1e20,0.0]
.model modp1 pmos(RS=[0,0])
m118 138 138 137 137 modp2 L=4.0u w=15u
rm118 137 138 [1e20,0.0]
.model modp2 pmos(RS=[0,0])
m119 3 138 137 137 modp3 L=4.0u w=100u
rm119 137 3 [1e20,0.0]
.model modp3 pmos(RS=[0,0])
m120 141 8 139 137 modp4 L=4.0u w=60u
rm120 141 139 [1e20,0.0]
.model modp4 pmos(RS=[0,0])
m121 142 2 139 137 modp5 L=4.0u w=60u
rm121 142 139 [1e20,0.0]
.model modp5 pmos(RS=[0,0])
m123 141 141 145 145 modn1 L=4.0u w=27.5u
rm123 141 145 [1e20,0.0]
.model modn1 nmos(RD=[0,0])
m124 142 141 145 145 modn2 L=4.0u w=27.5u
rm124 142 145 [1e20,0.0]
.model modn2 nmos(RD=[0,0])
m125 3 142 145 145 modn3 L=4.0u w=100u
rm125 3 145 [1e20,0.0]
.model modn3 nmos(RD=[0,0])
*Other declarations
V1DD 137 0 5
V1SS 145 0 -5
```

```
**************************************************
**************************************************
** Opamp 2
c21 242 243 [1.27,.127]pf
r214a 238 245 [110,6.6]k
r214b 243 5 [8.75,0.525]k
*Transistor declarations
* with parallel resistors for short faults and RS/RD parameter for open faults
m217 239 238 237 237 modp1 L=4.0u w=35u
rm217 237 239 [1e20,0.0]
.model modp6 pmos(RS=[0,0])
m218 238 238 237 237 modp2 L=4.0u w=15u
rm218 237 238 [1e20,0.0]
.model modp7 pmos(RS=[0,0])
m219 5 238 237 237 modp3 L=4.0u w=100u
rm219 237 5 [1e20,0.0]
.model modp8 pmos(RS=[0,0])
m220 241 4 239 237 modp4 L=4.0u w=60u
rm220 241 239 [1e20,0.0]
.model modp9 pmos(RS=[0,0])
m221 242 0 239 237 modp5 L=4.0u w=60u
rm221 242 239 [1e20,0.0]
.model modp10 pmos(RS=[0,0])
m223 241 241 245 245 modn1 L=4.0u w=27.5u
rm223 241 245 [1e20,0.0]
.model modn4 nmos(RD=[0,0])
m224 242 241 245 245 modn2 L=4.0u w=27.5u
rm224 242 245 [1e20,0.0]
.model modn5 nmos(RD=[0,0])
m225 5 242 245 245 modn3 L=4.0u w=100u
rm225 5 245 [1e20,0.0]
.model modn6 nmos(RD=[0,0])
*Other declarations
VDD 237 0 5
VSS 245 0 -5

**************************************************
**************************************************
** Opamp 3
c31 342 343 [1.27,.127]pf
r314a 338 345 [110,6.6]k
r314b 343 7 [8.75,0.525]k
*Transistor declarations
* with parallel resistors for short faults and RS/RD parameter for open faults
m317 339 338 337 337 modp1 L=4.0u w=35u
rm317 337 339 [1e20,0.0]
.model modp11 pmos(RS=[0,0])
m318 338 338 337 337 modp2 L=4.0u w=15u
rm318 337 338 [1e20,0.0]
.model modp12 pmos(RS=[0,0])
m319 7 338 337 337 modp3 L=4.0u w=100u
```

```
rm319 337 7 [1e20,0.0]
.model modp13 pmos(RS=[0,0])
m320 341 6 339 337 modp4 L=4.0u w=60u
rm320 341 339 [1e20,0.0]
.model modp14 pmos(RS=[0,0])
m321 342 0 339 337 modp5 L=4.0u w=60u
rm321 342 339 [1e20,0.0]
.model modp15 pmos(RS=[0,0])
m323 341 341 345 345 modn1 L=4.0u w=27.5u
rm323 341 345 [1e20,0.0]
.model modn7 nmos(RD=[0,0])
m324 342 341 345 345 modn2 L=4.0u w=27.5u
rm324 342 345 [1e20,0.0]
.model modn8 nmos(RD=[0,0])
m325 7 342 345 345 modn3 L=4.0u w=100u
rm325 7 345 [1e20,0.0]
.model modn9 nmos(RD=[0,0])
*Other declarations
VDD 337 0 5
VSS 345 0 -5

**************************************************
R1 9 2 [10,0.3]k
R2 2 3 [10,0.3]k
R3 3 4 [10,0.3]k
R4 5 6 [10,0.3]k
R5 2 7 [10,0.3]k
R6 8 0 [3,0.09]k
R7 8 5 [7,0.21]k
*5% on c1
C1 4 5 [20,1.6]nf
C2 6 7 [20,0.6]nf
.print tran v(100) v(9) v(7)
.options nopage noecho nomod numdgt=3
.end
```

A.2.7 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the Continuous Time Filter circuit; no soft faults have been simulated at this time.

```
#GOOD 1
#R1 1e7 1 r1_open
#R1 .01 1 r1_short
#R2 1e7 1 r2_open
#R2 .01 1 r2_short
#R3 1e7 1 r3_open
#R3 .01 1 r3_short
#R4 1e7 1 r4_open
#R4 .01 1 r4_short
#R5 1e7 1 r5_open
#R5 .01 1 r5_short
#R6 1e7 1 r6_open
#R6 .01 1 r6_short
#R7 1e7 1 r7_open
#R7 .01 1 r7_short
#C1 1e4f 1 c1_open
#C1 .001nf 1 c1_short
#C2 1e4f 1 c2_open
#C2 .001nf 1 c2_short
#r114a .01 1 r114a_short
#r114a 1e7 1 r114a_open
#r114b 1e4 1 r114b_open
#r114b .01 1 r114b_short
#c11 1e4f 1 c11_open
#c11 .001nf 1 c11_short
#modp1 1e7 1 m117_off RS
#rm117 1 1 m117_on
#modp2 1e7 1 m118_off RS
#rm118 1 1 m118_on
#modp3 1e7 1 m119_off RS
#rm119 1 1 m119_on
#modp4 1e7 1 m120_off RS
#rm120 1 1 m120_on
#modp5 1e7 1 m121_off RS
#rm121 1 1 m121_on
#modn1 1e7 1 m123_off RD
#rm123 1 1 m123_on
#modn2 1e7 1 m124_off RD
#rm124 1 1 m124_on
#modn3 1e7 1 m125_off RD
#rm125 1 1 m125_on
#r214a .01 1 r214a_short
#r214a 1e7 1 r214a_open
#r214b 1e4 1 r214b_open
#r214b .01 1 r214b_short
```

#c21 1e4f 1 c21_open
#c21 .001nf 1 c21_short
#modp6 1e7 1 m217_off RS
#rm217 1 1 m217_on
#modp7 1e7 1 m218_off RS
#rm218 1 1 m218_on
#modp8 1e7 1 m219_off RS
#rm219 1 1 m219_on
#modp9 1e7 1 m220_off RS
#rm220 1 1 m220_on
#modp10 1e7 1 m221_off RS
#rm221 1 1 m221_on
#modn4 1e7 1 m223_off RD
#rm223 1 1 m223_on
#modn5 1e7 1 m224_off RD
#rm224 1 1 m224_on
#modn6 1e7 1 m225_off RD
#rm225 1 1 m225_on
#r314a .01 1 r314a_short
#r314a 1e7 1 r314a_open
#r314b 1e4 1 r314b_open
#r314b .01 1 r314b_short
#c31 1e4f 1 c31_open
#c31 .001nf 1 c31_short
#modp11 1e7 1 m317_off RS
#rm317 1 1 m317_on
#modp12 1e7 1 m318_off RS
#rm318 1 1 m318_on
#modp13 1e7 1 m319_off RS
#rm319 1 1 m319_on
#modp14 1e7 1 m320_off RS
#rm320 1 1 m320_on
#modp15 1e7 1 m321_off RS
#rm321 1 1 m321_on
#modn7 1e7 1 m323_off RD
#rm323 1 1 m323_on
#modn8 1e7 1 m324_off RD
#rm324 1 1 m324_on
#modn9 1e7 1 m325_off RD
#rm325 1 1 m325_on

A.2.8 Simulation Results with No Component Variation at 100MHz
- All Hard Faults, internal and external to opamps

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

FAULT	100MHZ		FAULT	100MHZ		FAULT	100MHZ
r1open	1		M119off	1		M223off	1
r1short	1		M119on	1		M223on	1
r2open	1		M120off	1		M224off	1
r2short	1		M120on	1		M224on	1
r3open	1		M121off	1		M225off	1
r3short	1		M121on	1		M225on	1
r4open	1		M123off	1		R314aopen	1
r4short	1		M123on	1		R314ashort	1
r5open	1		M124off	1		R314bopen	1
r5short	1		M124on	1		R314bshort	1
r6open	1		M125off	1		C31open	1
r6short	1		M125on	1		C31short	1
r7open	1		R214aopen	1		M317off	1
r7short	1		R214ashort	1		M317on	1
c1open	1		R214bopen	1		M318off	1
c1short	1		R214bshort	1		M318on	1
c2open	1		C21open	1		M319off	1
c2short	1		C21short	1		M319on	1
R114aopen	1		M217off	1		M320off	1
R114ashort	1		M217on	1		M320on	1
R114bopen	1		M218off	1		M321off	1
R114bshort	1		M218on	1		M321on	1
C11open	1		M219off	1		M323off	1
C11short	1		M219on	1		M323on	1
M117off	1		M220off	1		M324off	1
M117on	1		M220on	1		M324on	1
M118off	1		M221off	1		M325off	1
M118on	1		M221on	1		M325on	1
						TOTAL	100%

A.2.9 Simulation Results with Component Variation at 100MHz, 10 seeds - All Hard Faults, internal and external to opamps

Overall Fault Coverage = (64*1 + 19* 0.9 + 1*0.7)/84 = 97.4%

FAULT	100MHZ		FAULT	100MHZ		FAULT	100MHZ
r1open	100%		M119off	100%		M223off	100%
r1short	100%		M119on	100%		M223on	90%
r2open	100%		M120off	100%		M224off	100%
r2short	100%		M120on	100%		M224on	90%
r3open	100%		M121off	100%		M225off	100%
r3short	100%		M121on	100%		M225on	90%
r4open	100%		M123off	100%		R314aopen	100%
r4short	100%		M123on	100%		R314ashort	100%
r5open	100%		M124off	100%		R314bopen	100%
r5short	100%		M124on	100%		R314bshort	100%
r6open	70%		M125off	100%		C31open	100%
r6short	90%		M125on	100%		C31short	100%
r7open	100%		R214aopen	90%		M317off	90%
r7short	100%		R214ashort	100%		M317on	100%
c1open	100%		R214bopen	100%		M318off	90%
c1short	100%		R214bshort	100%		M318on	100%
c2open	100%		C21open	90%		M319off	90%
c2short	100%		C21short	90%		M319on	100%
R114aopen	100%		M217off	100%		M320off	90%
R114ashort	100%		M217on	100%		M320on	100%
R114bopen	100%		M218off	100%		M321off	90%
R114bshort	100%		M218on	100%		M321on	100%
C11open	90%		M219off	100%		M323off	90%
C11short	100%		M219on	90%		M323on	100%
M117off	100%		M220off	100%		M324off	90%
M117on	100%		M220on	90%		M324on	100%
M118off	100%		M221off	100%		M325off	90%
M118on	100%		M221on	90%		M325on	100%
						TOTAL	97.4%

Appendix 3
Op Amp Component in Leap Frog Filter - Op Amp 2 (ITC'97)

A.3.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
*operational amplifier 2 (Leap frog opamp)

vck 100 0
vin 5 0
%dc 100 5 8
R1a 6 66 1
R1b 66 3 [100,0]meg
M1 66 4 3 3 MODP1 w=20u l=10u
.MODEL MODP1 PMOS(RS=[0,0.0])
R2a 7 77 1
R2b 77 3 [100,0]meg
M2 77 5 3 3 MODP2 w=20u l=10u
.MODEL MODP2 PMOS(RS=[0,0.0])
R3a 6 67 1
R3b 67 11 [100,0]meg
M3 67 6 11 11 MODN3 w=36u l=10u
.MODEL MODN3 NMOS(RD=[0,0.0])
R4a 7 78 1
R4b 78 11 [100,0]meg
M4 78 6 11 11 MODN4 w=36u l=10u
.MODEL MODN4 NMOS(RD=[0,0.0])
R5a 3 33 1
R5b 33 1 [100,0]meg
M5 33 2a 1 1 MODP5 w=30u l=10u
.MODEL MODP5 PMOS(RS=[0,0.0])
R6a 8 88 1
R6b 88 11 [100,0]meg
M6 88 7 11 11 MODN6 w=100u l=10u
.MODEL MODN6 NMOS(RD=[0,0.0])
R7a 8 89 1
R7b 89 1 [100,0]meg
M7 89 2 1 1 MODP7 w=42u l=10u
.MODEL MODP7 PMOS(RS=[0,0.0])
R8a 2 22 1
R8b 22 11 [100,0]meg
M8 22 6 11 11 MODN8 w=60u l=10u
.MODEL MODN8 NMOS(RD=[0,0.0])
R9a 2 23 1
R9b 23 1 [100,0]meg
```

```
M9 23 2 1 1 MODP9 w=30u l=10u
.MODEL MODP9 PMOS(RS=[0,0.0])
Rc 7 76 1
C1 76 8 [6,0.3]p
Rs 76 8 100meg
vbias 2a 0 .1
VDD 1 0 5
VSS 11 0 -5
R1 4 0 0
Co 8 0 2e-12
.print tran v(100) v(5) v(8)
.options nopage noecho nomod numdgt=2
.end
```

A.3.2 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the Op Amp2 circuit.

```
#C1 1e4f 1 C1_open
#C1 .001nf 1 C1_short
#R1b 1 1 M1_on
#R2b 1 1 M2_on
#R3b 1 1 M3_on
#R4b 1 1 M4_on
#R5b 1 1 M5_on
#R6b 1 1 M6_on
#R7b 1 1 M7_on
#R8b 1 1 M8_on
#R9b 1 1 M9_on
#MODP1 1E10 1 M1_off RS
#MODP2 1E10 1 M2_off RS
#MODN3 1E10 1 M3_off RS
#MODN4 1E10 1 M4_off RS
#MODP5 1E10 1 M5_off RS
#MODN6 1E10 1 M6_off RD
#MODP7 1E10 1 M7_off RD
#MODN8 1E10 1 M8_off RD
#MODP9 1E10 1 M9_off RD
```

A.3.3 Soft Fault List Supplied to SFA

This fault list is used to simulate all soft faults in the Op Amp2 circuit.

```
#C1 4.2e-11 1 C1_low
#C1 7.8e-11 1 C1_high
```

A.3.4 Simulation Results with No Component Variation - Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	10KHZ	100KHZ	1MHZ	10MHZ	100MHZ	1GHZ
C1open	1	1	1	1	1	1	1	1
C1short	1	1	1	1	1	1	1	1
M1on	1	1	1	1	1	1	1	1
M2on	1	1	1	1	1	1	1	1
M3on	1	1	1	1	1	1	1	1
M4on	1	1	1	1	1	1	1	1
M5on	1	1	1	1	1	1	1	1
M6on	1	1	1	1	1	1	1	1
M7on	1	1	1	1	1	1	1	1
M8on	1	1	1	1	1	1	1	1
M9on	1	1	1	1	1	1	1	1
M1off	1	1	1	1	1	1	1	1
M2off	1	1	1	1	1	1	1	1
M3off	1	1	1	1	1	1	1	1
M4off	1	1	1	1	1	1	1	1
M5off	1	1	1	1	1	1	1	1
M6off	1	1	1	1	1	1	1	1
M7off	1	1	1	1	1	1	1	1
M8off	1	1	1	1	1	1	1	1
M9off	1	1	1	1	1	1	1	1
	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100HZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1GHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.3.5 Simulation Results with No Component Variation - Soft Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100KHZ
C1low	1
C1high	1
	100%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100KHz	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.3.6 Simulation Results with Component Variation - Hard Faults

A.3.6.1 Simulation Results at 100KHz, 10 seeds

Overall Fault Coverage = 100%

Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
C1open	100%	100%	100%	100%	100%	100%	100%	10%	10%	10%	10%
C1short	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	0%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	0%	100%	30%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	0%
M4on	100%	100%	100%	100%	100%	100%	100%	30%	30%	10%	30%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	50%	100%	10%	50%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%
M9on	100%	100%	100%	100%	100%	100%	100%	0%	100%	10%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	40%	70%	10%	100%
M3off	100%	60%	100%	100%	60%	100%	100%	0%	100%	0%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M9off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Difference in Input and Output Magnitude Summing

	Cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	Fspwr	fswpc	fswprc
C1open	100%	100%	100%	100%	100%	100%	100%	10%	10%	10%	10%
C1short	100%	100%	100%	100%	100%	100%	100%	0%	20%	30%	20%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	0%	0%	30%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	10%	10%	0%
M4on	100%	100%	100%	100%	100%	100%	100%	30%	0%	20%	30%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	50%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	0%
M9on	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%	100%
M3off	100%	60%	100%	100%	60%	100%	100%	0%	0%	0%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	90%	0%	0%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%
M9off	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc	total
C1open	100%	100%	100%	100%	100%	100%	100%	10%	20%	10%	10%	100%
C1short	100%	100%	100%	100%	100%	100%	100%	0%	20%	30%	20%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	0%	100%	30%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	10%	10%	0%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	30%	30%	20%	30%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	50%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
M9on	100%	100%	100%	100%	100%	100%	100%	0%	100%	10%	100%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	100%	70%	10%	100%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M9off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Appendix 4
Leap Frog Filter (ITC'97)

A.4.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
Leapfrog filter
vck 100 0
vin 20 0
%dc 100 20 19
.Subckt opamp 4 5 8 1 11
.MODEL mosn NMOS
+ vto=1 kp=17u gamma=1.3 lambda=0.01 phi=0.7
+pb=0.8 mj=0.5 mjsw=.3 cgso=350p cgdo=350p cgbo=200p
+cj=300u cjsw=500p ld=0.8u tox=80n
.MODEL mosp PMOS
+ vto=-1 kp=8u gamma=.6 lambda=0.02 phi=0.6
+pb=0.5 mj=0.5 mjsw=.25 cgso=350p cgdo=350p cgbo=200p
+cj=150u cjsw=400p ld=0.8u tox=80n
R1a 6 66 1U
R1b 66 3 100g
m1 66 4 3 3 mosp w=20u l=10u
R2a 7 77 1U
R2b 77 3 100g
m2 77 5 3 3 mosp w=20u l=10u
R3a 6 67 1U
R3b 67 11 100g
m3 67 6 11 11 mosn w=36u l=10u
R4a 7 78 1U
R4b 78 11 100g
m4 78 6 11 11 mosn w=36u l=10u
R5a 3 33 1U
R5b 33 1 100g
m5 33 2a 1 1 mosp w=30u l=10u
R6a 8 88 1U
R6b 88 11 100g
m6 88 7 11 11 mosn w=100u l=10u
R7a 8 89 1U
R7b 89 1 100g
m7 89 2 1 1 mosp w=42u l=10u
R8a 2 22 1U
R8b 22 11 100g
m8 22 6 11 11 mosn w=60u l=10u
R9a 2 23 1U
```

```
R9b 23 1 100g
m9 23 2 1 1 mosp w=30u l=10u
Rc 7 76 1U
cc 76 8 [6,0.3]p
Rs 76 8 100g
vbias 2a 0 .1
.ends

*EXTERNAL CIRCUIT
R1 20 2 [10,0.2]K
R2 2 4 [10,0.2]K
R3 10 2 [10,0.2]K
R4 4 5 [10,0.2]K
R5 5 7 [10,0.2]K
R6 7 8 [10,0.2]K
R7 10 11 [10,0.2]K
R8 13 14 [10,0.2]K
R9 14 16 [10,0.2]K
R10 17 19 [10,0.2]K
R11 16 17 [10,0.2]K
R12 19 11 [10,0.2]K
R13 13 5 [10,0.2]K
C1 2 49 [0.01,0.002]uf
R49 49 4 1U
R50 2 4 100g
C2 8 59 [0.02,0.004]uf
R59 59 10 1U
R60 8 10 100g
C3 11 69 [0.02,0.004]uf
R69 69 13 1U
R70 11 13 100g
C4 17 79 [0.01,0.003]uf
R79 79 19 1u
R80 17 19 100g
xop1 2 0 4 VCC VEE opamp
xop2 5 0 7 VCC VEE opamp
xop3 8 0 10 VCC VEE opamp
xop4 11 0 13 VCC VEE opamp
xop5 14 0 16 VCC VEE opamp
xop6 17 0 19 VCC VEE opamp
Vdd VCC 0 15.0V
Vss VEE 0 -15.0V
.print tran v(100) v(20) v(19)
.options nopage noecho nomod numdgt=2
.end
```

A.4.2 Hard Fault List Supplied to SFA

This fault list is used to simulate *only external* hard faults in the Leap Frog Filter circuit; no soft faults have been simulated at this time.

#R1 1e7 1 r1_open
#R1 .01 1 r1_short
#R2 1e7 1 r2_open
#R2 .01 1 r2_short
#R3 1e7 1 r3_open
#R3 .01 1 r3_short
#R4 1e7 1 r4_open
#R4 .01 1 r4_short
#R5 1e7 1 r5_open
#R5 .01 1 r5_short
#R6 1e7 1 r6_open
#R6 .01 1 r6_short
#R7 1e7 1 r7_open
#R7 .01 1 r7_short
#R8 1e7 1 r8_open
#R8 .01 1 r8_short
#R9 1e7 1 r9_open
#R9 .01 1 r9_short
#R10 1e7 1 r10_open
#R10 .01 1 r10_short
#R11 1e7 1 r11_open
#R11 .01 1 r11_short
#R12 1e7 1 r12_open
#R12 .01 1 r12_short
#C1 1e6 1 C1_open
#C1 .001 1 C1_short
#C2 1e6 1 C2_open
#C2 .001 1 C2_short
#C3 1e6 1 C3_open
#C3 .001 1 C3_short
#C4 1e6 1 C4_open
#C4 .001 1 C4_short

A.4.3 Simulation Results with No Component Variation-External Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	100KHZ	1MHZ	10MHZ	100MHZ	500MHZ	1GHZ	10GHZ	100GHZ
r1open	1	1	1	1	1	1	1	1	1	0
r1short	1	1	1	1	1	1	1	1	1	0
r2open	1	1	1	1	1	1	1	1	1	0
r2short	1	1	1	1	1	1	1	1	1	0
r3open	1	1	1	1	1	1	1	1	1	0
r3short	1	1	1	1	1	1	1	1	1	0
r4open	1	1	1	1	1	1	1	1	1	0
r4short	1	1	1	1	1	1	1	1	1	0
r5open	1	1	1	1	1	1	1	1	1	0
r5short	1	1	1	1	1	1	1	1	1	0
r6open	1	1	1	1	1	1	1	1	1	0
r6short	1	1	1	1	1	1	1	1	1	0
r7open	1	1	1	1	1	1	1	1	1	0
r7short	1	1	1	1	1	1	1	1	1	0
r8open	1	1	1	1	1	1	1	1	1	0
r8short	1	1	1	1	1	1	1	1	1	0
r9open	1	1	1	1	1	1	1	1	1	0
r9short	1	1	1	1	1	1	1	1	1	0
r10open	1	1	1	1	1	1	1	1	1	0
r10short	1	1	1	1	1	1	1	1	1	0
r11open	1	1	1	1	1	1	1	1	1	0
r11short	1	1	1	1	1	1	1	1	1	0
r12open	1	1	1	1	1	1	1	1	1	0
r12short	1	1	1	1	1	1	1	1	1	0
c1open	1	1	1	1	1	1	1	1	1	0
c1short	1	1	1	1	1	1	1	1	1	0
c2open	1	1	1	1	1	1	1	1	1	0
c2short	1	1	1	1	1	1	1	1	1	0
c3open	1	1	1	1	1	1	1	1	1	0
c3short	1	1	1	1	1	1	1	1	1	0
c4open	1	1	1	1	1	1	1	1	1	0
c4short	1	1	1	1	1	1	1	1	1	0
	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	0.0%

Fault Coverage Per Waveform Versus Frequency

	cup	Cdwn	cud	cuR	cdR	CudR	lfsr	fswp	fswpR	fswpC	fswpRC
100HZ	81%	88%	84%	100%	94%	100%	97%	100%	91%	100%	100%
1KHZ	94%	97%	97%	100%	100%	100%	100%	100%	94%	100%	100%
100KHZ	100%	100%	100%	100%	97%	100%	100%	100%	100%	100%	100%
1MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100MHZ	100%	16%	100%	100%	94%	100%	50%	100%	100%	100%	100%
500MHZ	100%	6%	100%	3%	9%	44%	0%	13%	100%	100%	100%
1GHZ	28%	0%	31%	28%	0%	28%	6%	100%	100%	100%	100%
10GHZ	0%	0%	0%	44%	0%	3%	0%	100%	13%	13%	13%
100GHZ	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

A.4.4 Simulation Results with Component Variation - External Hard Faults

A.4.4.1 Simulation Results at 100KHz, 10 seeds

Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r6open	50%	90%	30%	70%	100%	100%	100%	100%	100%	100%	100%
r6short	10%	20%	10%	20%	50%	20%	50%	50%	50%	50%	50%
r7open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r7short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r8open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r8short	100%	80%	100%	100%	90%	100%	100%	100%	100%	100%	100%
r9open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r9short	100%	80%	100%	100%	90%	100%	100%	100%	100%	100%	100%
r10open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r10short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r11open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r11short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r12open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r12short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c1short	10%	100%	0%	20%	100%	20%	20%	20%	20%	20%	20%
c2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c2short	70%	90%	50%	80%	100%	100%	100%	100%	100%	100%	100%
c3open	100%	100%	100%	90%	100%	90%	100%	100%	100%	100%	100%
c3short	100%	100%	70%	100%	100%	100%	100%	100%	100%	100%	100%
c4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c4short	10%	40%	10%	10%	20%	10%	20%	20%	20%	20%	20%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r6open	10%	90%	20%	70%	100%	100%	100%	100%	100%	100%	100%
r6short	20%	50%	10%	20%	50%	20%	50%	50%	50%	50%	50%
r7open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r7short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r8open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r8short	100%	70%	100%	100%	90%	100%	100%	100%	100%	100%	100%
r9open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r9short	100%	70%	100%	100%	90%	100%	100%	100%	100%	100%	100%
r10open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r10short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r11open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r11short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r12open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r12short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c1short	10%	100%	0%	20%	100%	20%	20%	20%	20%	20%	20%
c2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c2short	10%	90%	30%	80%	100%	100%	100%	100%	100%	100%	100%
c3open	100%	100%	100%	90%	100%	90%	100%	100%	100%	100%	100%
c3short	80%	100%	10%	100%	100%	100%	100%	100%	100%	100%	100%
c4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c4short	10%	50%	0%	10%	20%	10%	20%	20%	20%	20%	20%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc	total
r1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r1short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r2short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r4short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r5short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r6open	50%	100%	30%	70%	100%	100%	100%	100%	100%	100%	100%	100%
r6short	20%	50%	10%	20%	50%	20%	50%	50%	50%	50%	50%	100%
r7open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r7short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r8open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r8short	100%	80%	100%	100%	90%	100%	100%	100%	100%	100%	100%	100%
r9open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r9short	100%	80%	100%	100%	90%	100%	100%	100%	100%	100%	100%	100%
r10open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r10short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r11open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r11short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r12open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
r12short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c1open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c1short	10%	100%	0%	20%	100%	20%	20%	20%	20%	20%	20%	100%
c2open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c2short	70%	90%	50%	80%	100%	100%	100%	100%	100%	100%	100%	100%
c3open	100%	100%	100%	90%	100%	90%	100%	100%	100%	100%	100%	100%
c3short	100%	100%	70%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
c4short	10%	50%	10%	10%	20%	10%	20%	20%	20%	20%	20%	100%

Appendix 5
Differential Pair Circuit (SFA)

A.5.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
Differential pair w/ active current source
vck 100 0
vin 5 0
%dc 100 5 1
.SUBCKT QT1 1 2 3
RB1 2 12 [100.0,0]
RC1 1 11 [1.0,0]
RE1 3 13 [1.0,0]
RBC1 11 12 [10000.0,0]K
RBE1 12 13 [10000.0,0]K
RCE1 11 13 [10000.0,0]K
Q1 11 12 13 QNL1
* Q1 1 2 3 QNL1
.MODEL QNL1 NPN (BF=[80,12] CCS=2PF
+ TF=0.3NS TR=6NS CJE=3PF CJC=2PF VA=[50,8])
.ENDS QT1
**
.SUBCKT QT2 1 2 3
RB2 2 12 [100.0,0]
RC2 1 11 [1.0,0]
RE2 3 13 [1.0,0]
RBC2 11 12 [10000.0,0]K
RBE2 12 13 [10000.0,0]K
RCE2 11 13 [10000.0,0]K
Q2 11 12 13 QNL2
* Q2 1 2 3 QNL2
.MODEL QNL2 NPN (BF=[80,12] CCS=2PF
+ TF=0.3NS TR=6NS CJE=3PF CJC=2PF VA=[50,8])
.ENDS QT2
**
.SUBCKT QT3 1 2 3
RB3 2 12 [100.0,0]
RC3 1 11 [1.0,0]
RE3 3 13 [1.0,0]
RBC3 11 12 [10000.0,0]K
RBE3 12 13 [10000.0,0]K
RCE3 11 13 [10000.0,0]K
Q3 11 12 13 QNL3
```

```
* Q3 1 2 3 QNL3
.MODEL QNL3 NPN (BF=[80,12] CCS=2PF
+ TF=0.3NS TR=6NS CJE=3PF CJC=2PF VA=[50,8])
.ENDS QT3
**
.SUBCKT QT4 1 2 3
RB4 2 12 [100.0,0]
RC4 1 11 [1.0,0]
RE4 3 13 [1.0,0]
RBC4 11 12 [10000.0,0]K
RBE4 12 13 [10000.0,0]K
RCE4 11 13 [10000.0,0]K
Q4 11 12 13 QNL4
* Q4 1 2 3 QNL4
.MODEL QNL4 NPN (BF=[80,12] CCS=2PF
+ TF=0.3NS TR=6NS CJE=3PF CJC=2PF VA=[50,8])
.ENDS QT4
**
* MAIN CIRCUIT
* .DC VIN -0.25 .25 0.005
RC1DP 3 4 [10,.5]K
RC2DP 1 4 [10,.5]K
RS1 5 2 [1,.05]K
RS2 6 0 [1,.05]K
RBIAS 4 7 [20,1]K
XQ2 1 6 10 QT2
XQ1 3 2 10 QT1
VCC 4 0 12
VEE 8 0 -12.0
XQ3 10 7 8 QT3
XQ4 7 7 8 QT4
.print tran v(100) v(5) v(1)
.options nopage noecho nomod numdgt=3
.END
```

A.5.2 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the Differential Pair circuit; no soft faults have been simulated at this time.

#GOOD 1
#RB1 1.0e6 1 RB1_open
#RC1 1.0e6 1 RC1_open
#RE1 1.0e6 1 RE1_open
#RBC1 0.01 1 RBC1_short
#RBE1 0.01 1 RBE1_short
#RCE1 0.01 1 RCE1_short
#QNL1 1 1 Q1_low BF
#QNL1 200 1 Q1_high BF
#RB2 1.0e6 1 RB2_open
#RC2 1.0e6 1 RC2_open
#RE2 1.0e6 1 RE2_open
#RBC2 0.01 1 RBC2_short
#RBE2 0.01 1 RBE2_short
#RCE2 0.01 1 RCE2_short
#QNL2 1 1 Q2_low BF
#QNL2 200 1 Q2_high BF
#RB3 1.0e6 1 RB3_open
#RC3 1.0e6 1 RC3_open
#RE3 1.0e6 1 RE3_open
#RBC3 0.01 1 RBC3_short
#RBE3 0.01 1 RBE3_short
#RCE3 0.01 1 RCE3_short
#QNL3 1 1 Q3_low BF
#QNL3 200 1 Q3_high BF
#RB4 1.0e6 1 RB4_open
#RC4 1.0e6 1 RC4_open
#RE4 1.0e6 1 RE4_open
#RBC4 0.01 1 RBC4_short
#RBE4 0.01 1 RBE4_short
#RCE4 0.01 1 RCE4_short
#QNL4 1 1 Q4_low BF
#QNL4 200 1 Q4_high BF
#RC1DP .01 1 R1_short
#RC1DP 1e7 1 R1_open
#RC2DP .01 1 R1_short
#RC2DP 1 1e7 1 R1_open
#RS1 .01 1 R1_short
#RS1 1e7 1 R1_open
#RS2 .01 1 R1_short
#RS2 1e7 1 R1_open
#Rbias .01 1 R1_short
#Rbias 1e7 1 R1_open

A.5.3 Simulation Results with No Component Variation - Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	10KHZ	100KHZ	1MHZ	10MHZ	100MHZ	1GHZ
RB1open	1	1	1	1	1	1	1	1
RC1open	1	1	1	1	1	1	1	1
RE1open	1	1	1	1	1	1	1	1
RBC1short	1	1	1	1	1	1	1	1
RBE1short	1	1	1	1	1	1	1	1
RCE1short	1	1	1	1	1	1	1	1
Q1lowbf	1	1	1	1	1	1	1	1
Q1highbf	1	1	1	1	1	1	1	1
RB2open	1	1	1	1	1	1	1	1
RC2open	1	1	1	1	1	1	1	1
RE2open	1	1	1	1	1	1	1	1
RBC2short	1	1	1	1	1	1	1	1
RBE2short	1	1	1	1	1	1	1	1
RCE2short	1	1	1	1	1	1	1	1
Q2lowbf	1	1	1	1	1	1	1	1
Q2highbf	1	1	1	1	1	1	1	1
RB3open	1	1	1	1	1	1	1	1
RC3open	1	1	1	1	1	1	1	1
RE3open	1	1	1	1	1	1	1	1
RBC3short	1	1	1	1	1	1	1	1
RBE3short	1	1	1	1	1	1	1	1
RCE3short	1	1	1	1	1	1	1	1
Q3lowbf	1	1	1	1	1	1	1	1
Q3highbf	1	1	1	1	1	1	1	1
RB4open	1	1	1	1	1	1	1	1
RC4open	1	1	1	1	1	1	1	1
RE4open	1	1	1	1	1	1	1	1
RBC4short	1	1	1	1	1	1	1	1
RBE4short	1	1	1	1	1	1	1	1
RCE4short	1	1	1	1	1	1	1	1
Q4lowbf	1	1	1	1	1	1	1	1
Q4highbf	1	1	1	1	1	1	1	1
RC1DPshort	1	1	1	1	1	1	1	1
RC1DPopen	1	1	1	1	1	1	1	1
RC1DPshort	1	1	1	1	1	1	1	1
RC2DPopen	1	1	1	1	1	1	1	1
RS1short	1	1	1	1	1	1	1	1
RS1open	1	1	1	1	1	1	1	1
RS2short	1	1	1	1	1	1	1	1
RS2open	1	1	1	1	1	1	1	1
Rbiasshort	1	1	1	1	1	1	1	1
Rbiasopen	1	1	1	1	1	1	1	1
FC	100%	100%	100%	100%	100%	100%	100%	100%

Fault Coverage Per Waveform Versus Frequency

	Cup	Cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100HZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1GHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.5.4 Simulation Results with Component Variation - Hard Faults

A.5.4.1 Simulation Results at 100Hz, 10 seeds

Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswpcr
RB1open	100%	100%	100%	90%	100%	90%	100%	0%	30%	50%	20%
RC1open	100%	100%	100%	90%	100%	100%	90%	20%	30%	10%	90%
RE1open	100%	100%	100%	100%	100%	100%	100%	90%	90%	90%	100%
RBC1short	30%	30%	30%	60%	20%	30%	70%	0%	20%	40%	30%
RBE1short	100%	100%	100%	100%	100%	100%	100%	30%	20%	40%	20%
RCE1short	70%	70%	70%	10%	30%	70%	20%	20%	10%	50%	10%
Q1lowbf	100%	100%	100%	10%	90%	40%	90%	20%	20%	60%	50%
Q1highbf	10%	10%	10%	10%	10%	10%	10%	10%	20%	10%	40%
RB2open	70%	90%	70%	100%	100%	100%	100%	20%	20%	10%	40%
RC2open	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
RE2open	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%
RBC2short	100%	100%	100%	100%	100%	100%	100%	30%	60%	40%	30%
RBE2short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%
RCE2short	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	0%
Q2lowbf	20%	20%	20%	10%	20%	10%	10%	20%	20%	20%	20%
Q2highbf	10%	10%	10%	10%	70%	20%	10%	10%	30%	20%	30%
RB3open	100%	100%	100%	20%	90%	100%	100%	10%	10%	30%	20%
RC3open	100%	100%	100%	20%	100%	100%	100%	10%	0%	10%	0%
RE3open	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%
RBC3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RBE3short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%
RCE3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Q3lowbf	90%	90%	90%	20%	20%	20%	20%	0%	30%	30%	20%
Q3highbf	50%	50%	50%	50%	50%	40%	50%	20%	30%	40%	20%
RB4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RC4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RE4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RBC4short	10%	10%	10%	10%	10%	10%	10%	0%	30%	40%	40%
RBE4short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%
RCE4short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%
Q4lowbf	100%	100%	100%	100%	100%	90%	100%	20%	10%	20%	50%
Q4highbf	10%	10%	10%	10%	10%	10%	10%	10%	0%	40%	50%
RC1DPshort	10%	10%	10%	10%	10%	10%	10%	20%	30%	30%	20%
RC1DPopen	100%	100%	100%	100%	100%	100%	100%	20%	20%	0%	90%
RC2DPshort	10%	10%	10%	10%	10%	10%	10%	0%	20%	50%	30%
RC2DPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	0%
RS1short	20%	20%	20%	20%	10%	20%	20%	10%	10%	10%	20%
RS1open	100%	100%	100%	100%	100%	100%	100%	70%	70%	80%	90%
RS2short	10%	10%	10%	10%	10%	10%	10%	20%	30%	60%	20%
RS2open	100%	100%	100%	100%	100%	100%	100%	10%	20%	40%	50%
Rbiasshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Rbiasopen	100%	100%	100%	30%	100%	100%	100%	100%	0%	100%	0%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswpcr
RB1open	80%	80%	80%	100%	100%	100%	80%	10%	30%	0%	40%
RC1open	100%	100%	100%	90%	100%	100%	90%	50%	0%	80%	90%
RE1open	90%	90%	90%	100%	100%	100%	100%	0%	10%	0%	100%
RBC1short	30%	30%	30%	60%	20%	30%	70%	30%	10%	30%	50%
RBE1short	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	20%
RCE1short	70%	70%	70%	10%	30%	70%	20%	20%	10%	10%	10%
Q1lowbf	100%	100%	100%	10%	90%	40%	90%	60%	10%	10%	70%
Q1highbf	10%	10%	10%	10%	10%	10%	10%	20%	10%	20%	0%
RB2open	70%	90%	70%	100%	100%	100%	100%	50%	10%	10%	60%
RC2open	100%	100%	100%	100%	100%	100%	100%	100%	20%	0%	0%
RE2open	100%	100%	100%	20%	100%	100%	100%	0%	0%	0%	0%
RBC2short	100%	100%	100%	100%	100%	100%	100%	20%	20%	10%	30%
RBE2short	100%	100%	100%	20%	100%	100%	100%	0%	0%	0%	0%
RCE2short	100%	100%	100%	100%	100%	100%	100%	90%	0%	0%	0%
Q2lowbf	20%	20%	20%	10%	20%	10%	10%	10%	10%	20%	30%
Q2highbf	10%	10%	10%	10%	70%	20%	10%	40%	0%	30%	0%
RB3open	100%	100%	100%	20%	90%	100%	100%	40%	0%	20%	50%
RC3open	100%	100%	100%	20%	100%	100%	100%	90%	80%	0%	0%
RE3open	100%	100%	100%	20%	100%	100%	100%	0%	0%	0%	0%
RBC3short	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
RBE3short	100%	100%	100%	20%	100%	100%	100%	0%	0%	0%	0%
RCE3short	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
Q3lowbf	90%	90%	90%	20%	20%	20%	20%	50%	20%	10%	20%
Q3highbf	50%	50%	50%	50%	50%	40%	50%	10%	10%	20%	10%
RB4open	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
RC4open	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
RE4open	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
RBC4short	10%	10%	10%	10%	10%	10%	10%	50%	10%	20%	40%
RBE4short	100%	100%	100%	20%	100%	100%	100%	0%	0%	0%	0%
RCE4short	100%	100%	100%	20%	100%	100%	100%	0%	0%	0%	0%
Q4lowbf	100%	100%	100%	100%	100%	90%	100%	40%	0%	30%	50%
Q4highbf	10%	10%	10%	10%	10%	10%	10%	30%	20%	20%	20%
RC1DPshort	10%	10%	10%	10%	10%	10%	10%	30%	20%	10%	0%
RC1DPopen	100%	100%	100%	100%	100%	100%	100%	60%	20%	80%	0%
RC2DPshort	10%	10%	10%	10%	10%	10%	10%	50%	20%	10%	20%
RC2DPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
RS1short	20%	20%	20%	20%	20%	20%	20%	30%	0%	0%	10%
RS1open	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
RS2short	10%	10%	10%	10%	10%	10%	10%	30%	30%	20%	10%
RS2open	100%	100%	100%	100%	100%	100%	100%	40%	0%	20%	10%
Rbiasshort	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%
Rbiasopen	100%	100%	100%	30%	100%	100%	100%	100%	0%	0%	0%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fswpr	fswpc	fswpcr	Total
RB1open	100%	100%	100%	100%	100%	100%	100%	10%	60%	50%	50%	100%
RC1open	100%	100%	100%	90%	100%	100%	90%	70%	30%	90%	20%	100%
RE1open	100%	100%	100%	100%	100%	100%	100%	90%	100%	90%	100%	100%
RBC1short	30%	30%	30%	60%	20%	30%	70%	30%	30%	70%	80%	80%
RBE1short	100%	100%	100%	100%	100%	100%	100%	30%	20%	50%	10%	100%
RCE1short	70%	70%	70%	10%	30%	70%	20%	40%	20%	60%	20%	80%
Q1lowbf	100%	100%	100%	10%	90%	40%	90%	80%	30%	70%	80%	100%
Q1highbf	10%	10%	10%	10%	10%	10%	10%	30%	30%	30%	40%	60%
RB2open	70%	90%	70%	100%	100%	100%	100%	70%	30%	20%	60%	100%
RC2open	100%	100%	100%	100%	100%	100%	100%	100%	20%	0%	0%	100%
RE2open	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%	100%
RBC2short	100%	100%	100%	100%	100%	100%	100%	30%	60%	50%	10%	100%
RBE2short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%	100%
RCE2short	100%	100%	100%	100%	100%	100%	100%	90%	0%	10%	10%	100%
Q2lowbf	20%	20%	20%	10%	20%	10%	10%	30%	30%	40%	30%	70%
Q2highbf	10%	10%	10%	10%	70%	20%	10%	50%	30%	50%	30%	100%
RB3open	100%	100%	100%	20%	90%	100%	100%	50%	10%	50%	100%	100%
RC3open	100%	100%	100%	20%	100%	100%	100%	100%	80%	10%	0%	100%
RE3open	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%	100%
RBC3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RBE3short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%	100%
RCE3short	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Q3lowbf	90%	90%	90%	20%	20%	20%	20%	50%	50%	40%	0%	100%
Q3highbf	50%	50%	50%	50%	50%	40%	50%	30%	40%	60%	30%	100%
RB4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RC4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RE4open	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
RBC4short	10%	10%	10%	10%	10%	10%	10%	50%	40%	40%	40%	80%
RBE4short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%	100%
RCE4short	100%	100%	100%	20%	100%	100%	100%	100%	0%	100%	0%	100%
Q4lowbf	100%	100%	100%	100%	100%	90%	100%	20%	10%	50%	40%	100%
Q4highbf	10%	10%	10%	10%	10%	10%	10%	40%	20%	60%	70%	80%
RC1DPshort	10%	10%	10%	10%	10%	10%	10%	50%	50%	40%	20%	80%
RC1DPopen	100%	100%	100%	100%	100%	100%	100%	80%	40%	80%	90%	100%
RC2DPshort	10%	10%	10%	10%	10%	10%	10%	50%	40%	60%	50%	80%
RC2DPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	0%	100%
RS1short	20%	20%	20%	20%	20%	20%	20%	40%	10%	10%	30%	80%
RS1open	100%	100%	100%	100%	100%	100%	100%	70%	70%	80%	90%	100%
RS2short	10%	10%	10%	10%	10%	10%	10%	50%	60%	80%	30%	100%
RS2open	100%	100%	100%	100%	100%	100%	100%	50%	20%	60%	60%	100%
Rbiasshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Rbiasopen	100%	100%	100%	30%	100%	100%	100%	100%	0%	100%	0%	100%

Appendix 6
Elliptical Filter (SFA)

A.6.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
Elliptical Filter
vck 100 0
vin 1 0
%dc 100 1 15
.Subckt opamp 4 5 8 1 11
.MODEL mosn NMOS
+ vto=1 kp=17u gamma=1.3 lambda=0.01 phi=0.7
+pb=0.8 mj=0.5 mjsw=.3 cgso=350p cgdo=350p cgbo=200p
+cj=300u cjsw=500p ld=0.8u tox=80n
.MODEL mosp PMOS
+ vto=-1 kp=8u gamma=.6 lambda=0.02 phi=0.6
+pb=0.5 mj=0.5 mjsw=.25 cgso=350p cgdo=350p cgbo=200p
+cj=150u cjsw=400p ld=0.8u tox=80n
R1a 6 66 1
R1b 66 3 [100,0]meg
m1 66 4 3 3 mosp w=20u l=10u
R2a 7 77 1
R2b 77 3 [100,0]meg
m2 77 5 3 3 mosp w=20u l=10u
R3a 6 67 1
R3b 67 11 [100,0]meg
m3 67 6 11 11 mosn w=36u l=10u
R4a 7 78 1
R4b 78 11 [100,0]meg
m4 78 6 11 11 mosn w=36u l=10u
R5a 3 33 1
R5b 33 1 [100,0]meg
m5 33 2a 1 1 mosp w=30u l=10u
R6a 8 88 1
R6b 88 11 [100,0]meg
m6 88 7 11 11 mosn w=100u l=10u
R7a 8 89 1
R7b 89 1 [100,0]meg
m7 89 2 1 1 mosp w=42u l=10u
R8a 2 22 1
R8b 22 11 [100,0]meg
m8 22 6 11 11 mosn w=60u l=10u
R9a 2 23 1
R9b 23 1 [100,0]meg
m9 23 2 1 1 mosp w=30u l=10u
Rc 7 76 1
```

```
C1 76 8 [6,0.3]p
Rs 76 8 [100,0]meg
vbias 2a 0 .1
.ends
**Capacitor Block:
.SUBCKT CNET 1 2 3 4 5 6 7 8 9 10 11 12 13 14
CM1 1 2 [2.6667,0.13]NF
CM2 3 4 [2.6667,0.13]NF
CM3 5 6 [2.6667,0.13]NF
CM4 7 8 [2.6667,0.13]NF
CM5 9 10 [2.6667,0.13]NF
CM6 11 12 [2.6667,0.13]NF
CM7 13 14 [2.6667,0.13]NF
.ENDS CNET
*Capacitor fault block:
.SUBCKT RNET 1 2 3 4 5 6 7 8 9 10 11 12 13 14
RF1 1 2 1.0e8
RF2 3 4 1.0e8
RF3 5 6 1.0e8
RF4 7 8 1.0e8
RF5 9 10 1.0e8
RF6 11 12 1.0e8
RF7 13 14 1.0e8
.ENDS RNET
*MAIN CIRCUIT
X1 2 0 3 77 44 opamp
R1 1 2 [19.6,1]K
R2 2 3 [196.0,9.8]K
X2 9 7 9 77 44 opamp
R3 3 5 [147.0,7.4]K
R4 3 10 [1.0,0.05]K
R5 10 0 [71.5,3.6]
R6 6 8 [37.4,1.9]K
R7 5 7 [154.0,7.7]K
X3 15 14 15 77 44 opamp
R8 9 8 [260.0,13]
R9 8 4 [740,37]
R10 4 0 [402.0,20]
R11 9 11 [110.0,5]K
R12 11 14 [110.0,5]K
R13 12 13 [27.4,1.4]K
R14 15 13 [40.0,2]
R15 13 0 [960.0,48]
V2 44 0 -15
V3 77 0 15
X4 2 3 10 6 5 8 6 7 4 12 13 11 12 14 CNET
X5 2 3 10 6 5 8 6 7 4 12 13 11 12 14 RNET
.print tran v(100) v(11) v(9)
.options nopage noecho nomod numdgt=3
.end
```

A.6.2 Hard Fault List Supplied to SFA

This fault list is used to simulate *only external* hard faults in the Elliptical Filter circuit; no soft faults have been simulated at this time.

```
#GOOD 1
#R1 1e7 1 R1_open
#R1 .01 1 R1_short
#R2 1e7 1 R2_open
#R2 .01 1 R2_short
#R3 1e7 1 R3_open
#R3 .01 1 R3_short
#R4 1e7 1 R4_open
#R4 .01 1 R4_short
#R5 1e7 1 R5_open
#R5 .01 1 R5_short
#R6 1e7 1 R6_open
#R6 .01 1 R6_short
#R7 1e7 1 R7_open
#R7 .01 1 R7_short
#R8 1e7 1 R8_open
#R8 .01 1 R8_short
#R9 1e7 1 R9_open
#R9 .01 1 R9_short
#R10 1e7 1 R10_open
#R10 .01 1 R10_short
#R11 1e7 1 R11_open
#R11 .01 1 R11_short
#R12 1e7 1 R12_open
#R12 .01 1 R12_short
#R13 1e7 1 R13_open
#R13 .01 1 R13_short
#R14 1e7 1 R14_open
#R14 .01 1 R14_short
#R15 1e7 1 R15_open
#R15 .01 1 R15_short
#CM1 1e4f 1 CM1_open
#CM1 .0001nf 1 CM1_short
#CM2 1e4f 1 CM2_open
#CM2 .0001nf 1 CM2_short
#CM3 1e4f 1 CM3_open
#CM3 .0001nf 1 CM3_short
#CM4 1e4f 1 CM4_open
#CM4 .0001nf 1 CM4_short
#CM5 1e4f 1 CM5_open
#CM5 .0001nf 1 CM5_short
#CM6 1e4f 1 CM6_open
#CM6 .0001nf 1 CM6_short
#CM7 1e4f 1 CM7_open
#CM7 .0001nf 1 CM7_short
```

A.6.3 Simulation Results with No Component Variation-External Hard Faults

Fault Coverage Per Waveform Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	1KHz	10KHZ	1MHZ			1KHZ	10KHZ	1MHZ
R1open	1	1	1		R12open	1	1	1
R1short	1	1	1		R12short	1	1	1
R2open	1	1	1		R13open	1	1	1
R2short	1	1	1		R13short	1	1	1
R3open	1	1	1		R14open	1	1	1
R3short	1	1	1		R14short	1	1	1
R4open	1	1	1		R15open	1	1	1
R4short	1	1	1		R15short	1	1	1
R5open	1	1	1		CM1open	1	1	1
R5short	1	1	1		CM1short	1	1	1
R6open	1	1	1		CM2open	1	1	1
R6short	1	1	1		CM2short	1	1	1
R7open	1	1	1		CM3open	1	1	1
R7short	1	1	1		CM3short	1	1	1
R8open	1	1	1		CM4open	1	1	1
R8short	1	1	1		CM4short	1	1	1
R9open	1	1	1		CM5open	1	1	1
R9short	1	1	1		CM5short	1	1	1
R10open	1	1	1		CM6open	1	1	1
R10short	1	1	1		CM6short	1	1	1
R11open	1	1	1		CM7open	1	1	1
R11short	1	1	1		CM7short	1	1	1
					Totals	100.0%	100.0%	100.0%

Fault Coverage Per Waveform

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpr	fswpc	fswprc	total
1KHZ	100%	2.3%	11.4%	18.2%	11.4%	20.5%	100%	100%	100%	100%	100%	100%

A.6.4 Simulation Results with Component Variation – External Hard Faults

A.6.4.1 Simulation Results at 100Hz, 10 seeds

Total Coverage - Both Magnitude and Summing Overall Fault Coverage = 100%

	cup	cud	cur	cudr	lfsr	fswp	fswpr	total
R1open	100%	0%	0%	0%	0%	0%	100%	100%
R1short	100%	100%	100%	100%	0%	0%	100%	100%
R2open	100%	100%	100%	100%	0%	0%	100%	100%
R2short	100%	0%	0%	0%	0%	0%	100%	100%
R3open	80%	40%	60%	60%	0%	50%	100%	100%
R3short	10%	0%	0%	0%	0%	100%	0%	100%
R4open	10%	0%	0%	0%	20%	100%	10%	100%
R4short	80%	0%	0%	0%	0%	100%	0%	100%
R5open	70%	0%	0%	0%	0%	100%	0%	100%
R5short	10%	0%	0%	0%	20%	100%	10%	100%
R6open	100%	0%	0%	0%	0%	100%	90%	100%
R6short	20%	0%	0%	0%	0%	100%	20%	100%
R7open	0%	100%	100%	100%	0%	100%	100%	100%
R7short	40%	0%	0%	0%	0%	100%	100%	100%
R8open	100%	0%	0%	0%	0%	100%	100%	100%
R8short	100%	0%	100%	100%	100%	100%	100%	100%
R9open	100%	20%	100%	100%	100%	100%	100%	100%
R9short	100%	0%	0%	0%	0%	100%	100%	100%
R10open	100%	20%	20%	80%	100%	100%	100%	100%
R10short	80%	0%	0%	0%	0%	100%	40%	100%
R11open	100%	100%	100%	100%	0%	100%	100%	100%
R11short	90%	0%	0%	0%	0%	100%	100%	100%
R12open	100%	100%	100%	100%	0%	100%	100%	100%
R12short	80%	0%	0%	0%	0%	100%	100%	100%
R13open	100%	0%	0%	0%	0%	100%	100%	100%
R13short	100%	0%	0%	0%	0%	100%	100%	100%
R14open	100%	0%	0%	0%	0%	100%	100%	100%
R14short	40%	20%	20%	20%	70%	90%	50%	100%
R15open	40%	20%	20%	20%	70%	100%	100%	100%
R15short	100%	0%	0%	0%	0%	100%	100%	100%
CM1open	70%	0%	0%	0%	60%	100%	100%	100%
CM1short	70%	0%	0%	0%	60%	100%	100%	100%
CM2open	30%	0%	0%	0%	0%	100%	100%	100%
CM2short	30%	0%	0%	0%	0%	100%	100%	100%
CM3open	30%	0%	0%	0%	0%	100%	100%	100%
CM3short	30%	0%	0%	0%	0%	100%	100%	100%
CM4open	30%	0%	0%	0%	0%	100%	100%	100%
CM4short	30%	0%	0%	0%	0%	100%	100%	100%
CM5open	90%	0%	0%	0%	0%	100%	100%	100%
CM5short	90%	0%	0%	0%	0%	100%	100%	100%
CM6open	10%	0%	0%	0%	20%	100%	100%	100%
CM6short	10%	0%	0%	0%	20%	100%	100%	100%
CM7open	80%	0%	0%	0%	0%	100%	100%	100%
CM7short	90%	0%	0%	0%	0%	100%	100%	100%

Appendix 7
Comparator (SFA)

A.7.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
*comparator circuit -AC analysis
vck 100 0
vin 12 0
%dc 100 12 8
*operational amplifier 2
R1a 6 66 1
R1b 66 3 [100,0]meg
M1 66 4 3 3 MODP1 w=20u l=10u
.MODEL MODP1 PMOS(RS=[0,0.0])
R2a 7 77 1
R2b 77 3 [100,0]meg
M2 77 5 3 3 MODP2 w=20u l=10u
.MODEL MODP2 PMOS(RS=[0,0.0])
R3a 6 67 1
R3b 67 11 [100,0]meg
M3 67 6 11 11 MODN3 w=36u l=10u
.MODEL MODN3 NMOS(RD=[0,0.0])
R4a 7 78 1
R4b 78 11 [100,0]meg
M4 78 6 11 11 MODN4 w=36u l=10u
.MODEL MODN4 NMOS(RD=[0,0.0])
R5a 3 33 1
R5b 33 1 [100,0]meg
M5 33 2a 1 1 MODP5 w=30u l=10u
.MODEL MODP5 PMOS(RS=[0,0.0])
R6a 8 88 1
R6b 88 11 [100,0]meg
M6 88 7 11 11 MODN6 w=100u l=10u
.MODEL MODN6 NMOS(RD=[0,0.0])
R7a 8 89 1
R7b 89 1 [100,0]meg
M7 89 2 1 1 MODP7 w=42u l=10u
.MODEL MODP7 PMOS(RS=[0,0.0])
R8a 2 22 1
R8b 22 11 [100,0]meg
M8 22 6 11 11 MODN8 w=60u l=10u
.MODEL MODN8 NMOS(RD=[0,0.0])
R9a 2 23 1
R9b 23 1 [100,0]meg
M9 23 2 1 1 MODP9 w=30u l=10u
.MODEL MODP9 PMOS(RS=[0,0.0])
Rc 7 76 1
```

```
C1 76 8 [6,0.3]p
Rs 76 8 [100,0]meg
vbias 2a 0 .1
VDD 1 0 5
VSS 11 0 -5
R1 4 0 0
Co 8 0 2e-12
*end opamp2
*MAIN CIRCUIT
VCC 1 0 15.0
VEE 11 0 -15.0
Rin 12 4 [10.0,.5]K
Rm 5 0 [20.0,1]K
Rf 5 8 [20.0,1]K
.print tran v(100) v(12) v(8)
.options nopage noecho nomod numdgt=2
.end
```

A.7.2 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the Comparator circuit.

```
#GOOD 1
#Rin 1e4 1 rin_open
#Rin .01 1 rin_short
#Rm 1e4 1 RM_open
#Rm .01 1 RM_short
#Rf 1e4 1 Rf_open
#Rf .01 1 Rf_short
#C1 1e4f 1 C1_open
#C1 .001nf 1 C1_short
#R1b 1 1 M1_on
#R2b 1 1 M2_on
#R3b 1 1 M3_on
#R4b 1 1 M4_on
#R5b 1 1 M5_on
#R6b 1 1 M6_on
#R7b 1 1 M7_on
#R8b 1 1 M8_on
#R9b 1 1 M9_on
#MODP1 1E10 1 M1_off RS
#MODP2 1E10 1 M2_off RS
#MODN3 1E10 1 M3_off RS
#MODN4 1E10 1 M4_off RS
#MODP5 1E10 1 M5_off RS
#MODN6 1E10 1 M6_off RD
#MODP7 1E10 1 M7_off RD
#MODN8 1E10 1 M8_off RD
#MODP9 1E10 1 M9_off RD
```

A.7.3 Soft Fault List Supplied to SFA

This fault list is used to simulate all soft faults in the Comparator circuit.

#Rin 7000 1 Rin_low
#Rin 13000 1 Rin_high
#Rm 14000 1 Rm_low
#Rm 26000 1 Rm_high
#Rf 14000 1 Rf_low
#Rf 26000 1 Rf_high

A.7.4 Simulation Results with No Component Variation - Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	100KHZ
Rinopen	0	0	1
Rinshort	0	0	1
Rmopen	1	1	1
Rmshort	1	1	1
Rfopen	1	1	1
Rfshort	1	1	1
C1open	1	1	1
C1short	1	1	1
M1on	1	1	1
M2on	1	1	1
M3on	1	1	1
M4on	1	1	1
M5on	1	1	1
M6on	1	1	1
M7on	1	1	1
M8on	1	1	1
M9on	1	1	1
M1off	1	1	1
M2off	1	1	1
M3off	1	1	1
M4off	1	1	1
M5off	1	1	1
M6off	1	1	1
M7off	1	1	1
M8off	1	1	1
M9off	1	1	1
	92.3%	92.3%	100%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	Fswp	fswpR	fswpC	fswpRC
100HZ	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	0%	53.8%	11.5%	46.2%
1KHZ	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%
100KHZ	92.3%	92.3%	92.3%	92.3%	92.3%	92.3%	100%	92.3%	92.3%	92.3%	92.3%

A.7.5 Simulation Results with No Component Variation - Soft Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100KHZ
Rinlow	0
Rinhigh	0
Rmlow	1
Rmhigh	1
Rflow	1
Rfhigh	1
	66.7%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100KHz	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%

A.7.6 Simulation Results with Component Variation - Hard Faults

A.7.6.1 Simulation Results at 100KHz, 10 seeds

Overall Fault Coverage = 95.4%

Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
Rinopen	10%	0%	10%	0%	0%	10%	0%	0%	10%	10%	10%
Rinshort	10%	0%	10%	0%	0%	10%	0%	0%	10%	10%	10%
Rmopen	100%	50%	100%	0%	50%	100%	60%	0%	0%	100%	100%
Rmshort	100%	80%	100%	100%	80%	100%	70%	0%	10%	100%	100%
Rfopen	100%	40%	100%	100%	40%	100%	60%	0%	100%	100%	100%
Rfshort	100%	80%	100%	100%	80%	100%	70%	10%	80%	100%	100%
C1open	100%	100%	100%	100%	100%	100%	100%	0%	40%	100%	100%
C1short	100%	100%	100%	100%	100%	100%	100%	0%	40%	100%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	10%	40%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	70%	100%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	10%	10%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M6on	90%	100%	100%	70%	100%	100%	100%	10%	60%	90%	90%
M7on	100%	100%	100%	0%	100%	100%	100%	0%	0%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M9on	100%	100%	100%	100%	100%	100%	100%	40%	0%	100%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	10%	40%	100%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	40%	0%	100%	100%
M4off	80%	100%	100%	60%	100%	100%	100%	30%	40%	80%	80%
M5off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	10%	80%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	40%	0%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	50%	10%	80%	100%	100%
M9off	100%	100%	100%	100%	100%	100%	100%	10%	70%	100%	100%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
Rinopen	10%	0%	10%	10%	0%	10%	0%	10%	10%	10%	0%
Rinshort	10%	0%	10%	10%	0%	10%	0%	10%	10%	10%	0%
Rmopen	100%	50%	100%	0%	50%	100%	60%	0%	0%	100%	100%
Rmshort	100%	80%	100%	0%	80%	100%	70%	90%	0%	100%	100%
Rfopen	100%	40%	100%	0%	40%	100%	60%	0%	0%	100%	100%
Rfshort	100%	80%	100%	0%	80%	100%	70%	100%	0%	100%	100%
C1open	100%	100%	100%	0%	100%	100%	100%	100%	40%	100%	100%
C1short	100%	100%	100%	0%	100%	100%	100%	100%	40%	100%	100%
M1on	100%	100%	100%	0%	100%	100%	100%	0%	0%	100%	100%
M2on	100%	100%	100%	0%	100%	100%	100%	40%	0%	100%	100%
M3on	100%	100%	100%	0%	100%	100%	100%	80%	0%	100%	100%
M4on	100%	100%	100%	0%	100%	100%	100%	10%	0%	100%	100%
M5on	100%	100%	100%	0%	100%	100%	100%	100%	0%	100%	100%
M6on	100%	100%	100%	0%	100%	100%	100%	80%	0%	90%	90%
M7on	100%	100%	100%	0%	0%	100%	100%	0%	0%	100%	100%
M8on	100%	100%	100%	0%	100%	100%	100%	100%	0%	100%	100%
M9on	100%	100%	100%	0%	100%	100%	100%	0%	100%	100%	100%
M1off	100%	100%	100%	0%	100%	100%	100%	90%	0%	100%	100%
M2off	100%	100%	100%	0%	100%	100%	100%	0%	0%	100%	100%
M3off	100%	100%	100%	0%	100%	100%	100%	0%	100%	100%	100%
M4off	100%	100%	100%	0%	100%	100%	100%	80%	0%	80%	80%
M5off	100%	100%	100%	0%	100%	100%	100%	0%	0%	100%	100%
M6off	100%	100%	100%	0%	100%	100%	100%	0%	0%	100%	100%
M7off	100%	100%	100%	0%	100%	100%	100%	0%	100%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	50%	80%	20%	100%	100%
M9off	100%	100%	100%	80%	100%	100%	100%	90%	30%	100%	100%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc	total
Rinopen	10%	0%	10%	10%	0%	10%	0%	10%	20%	10%	10%	40%
Rinshort	10%	0%	10%	10%	0%	10%	0%	10%	20%	10%	10%	40%
Rmopen	100%	50%	100%	0%	50%	100%	60%	0%	0%	100%	100%	100%
Rmshort	100%	80%	100%	100%	80%	100%	70%	90%	10%	100%	100%	100%
Rfopen	100%	40%	100%	100%	40%	100%	60%	0%	100%	100%	100%	100%
Rfshort	100%	80%	100%	100%	80%	100%	70%	100%	80%	100%	100%	100%
C1open	100%	100%	100%	100%	100%	100%	100%	100%	80%	100%	100%	100%
C1short	100%	100%	100%	100%	100%	100%	100%	100%	80%	100%	100%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	40%	40%	100%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	80%	70%	100%	100%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	20%	10%	100%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%	100%
M6on	100%	100%	100%	70%	100%	100%	100%	80%	60%	90%	90%	100%
M7on	100%	100%	100%	0%	100%	100%	100%	0%	0%	100%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%	100%	100%
M9on	100%	100%	100%	100%	100%	100%	100%	40%	100%	100%	100%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	90%	40%	100%	100%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	40%	100%	100%	100%	100%
M4off	100%	100%	100%	60%	100%	100%	100%	80%	40%	80%	80%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	10%	80%	100%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	40%	100%	100%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	50%	80%	80%	100%	100%	100%
M9off	100%	100%	100%	100%	100%	100%	100%	100%	70%	100%	100%	100%

Appendix 8
Single Stage Amplifier (SFA)

A.8.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
Single stage amplifier
vck 100 0
vin 1 0
%dc 100 1 3
VCC 8 0 5.0
R1 1 0 [17.6,0.9]k
R2 8 1 [61.0,3.1]K
R3 8 3 [1.2,.06]k
R4 7 0 [300.0,15]
RE 4 7 [1.0,0]
RC 3 6 [1.0,0]
RB 1 5 [100.0,0]
Rbc 5 6 [1.0E8,0]
Rbe 5 4 [1.0E8,0]
Rce 6 4 [1.0E8,0]
Q1 6 5 4 QNL
.model QNL NPN(beta=80 cap_csb=2PF Cap_be=3PF Cap_ibc=2PF )
.print tran v(100) v(1) v(3)
.options nopage noecho nomod numdgt=2
.end
```

A.8.2 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the Single Stage Amplifier circuit.

```
#RC 1.0E6 1 RC_OPEN
#RE 1.0E6 1 RE_OPEN
#RB 1.0E6 1 RB_OPEN
#Rbc 1.0 1 RBC_Short
#Rbe 1.0 1 RBE_Short
#Rce 1.0 1 RCE_Short
#QNL 1.0 1 Q_low BF
#QNL 200.0 1 Q_hi BF
#R1 1.0E6 1 R1_OPEN
#R1 1.0 1 R1_Short
#R2 1.0E6 1 R2_OPEN
#R2 1.0 1 R2_Short
#R3 1.0E6 1 R3_OPEN
#R3 1.0 1 R3_Short
#R4 1.0E6 1 R4_OPEN
#R4 1.0 1 R4_Short
```

A.8.3 Soft Fault List Supplied to SFA

This fault list is used to simulate all soft faults in the Single Stage Amplifier circuit.

#QNL 6 1 Q_low2 BF
#QNL 152 1 Q_hi2 BF
#R1 12200 1 R1_low
#R1 23000 1 R1_high
#R2 42400 1 R2_low
#R2 79600 1 R2_high
#R3 840 1 R3_low
#R3 1560 1 R3_high
#R4 210 1 R4_low
#R4 390 1 R4_high
#RB 70 1 R5_low
#RB 130 1 R5_high

A.8.4 Simulation Results with No Component Variation - Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100HZ	1KHZ	10KHZ	100KHZ	1MHZ	10MHZ	100MHZ	1GHZ
Rcopen	1	1	1	1	1	1	1	100%
Reopen	1	1	1	1	1	1	1	100%
Rbopen	1	1	1	1	1	1	1	100%
Rbcshort	1	1	1	1	1	1	1	100%
Rbeshort	1	1	1	1	1	1	1	100%
Rceshort	1	1	1	1	1	1	1	100%
Qlow	1	1	1	1	1	1	1	100%
Qhi	1	1	1	1	1	1	1	90%
R1open	1	1	1	1	1	1	1	100%
R1short	1	1	1	1	1	1	1	100%
R2open	1	1	1	1	1	1	1	100%
R2short	1	1	1	1	1	1	1	100%
R3open	1	1	1	1	1	1	1	100%
R3short	1	1	1	1	1	1	1	100%
R4open	1	1	1	1	1	1	1	100%
R4short	1	1	1	1	1	1	1	100%
	100%	100%	100%	100%	100%	100%	100%	100%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswpRC
100HZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100KHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
500MHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
1GHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
10GHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
100GHZ	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.8.5 Simulation Results with No Component Variation - Soft Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100KHZ
Qlow	1
Qhigh	1
R1low	1
R1high	1
R2low	1
R2high	1
R3low	1
R3high	1
R4low	1
R4high	1
R5low	1
R5high	1
	100%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100KHz	100%	91.7%	100%	100%	83.3%	100%	100%	100%	100%	100%	100%

A.8.6 Simulation Results with Component Variation (10 seeds) - Hard Faults

A.8.6.1 Simulation Results at 100Hz, 10 seeds

Overall Fault Coverage = 99.4%

Magnitude Summing

	Cup	Cdwn	cud	cur	Cdr	cudr	lfsr	fswp	Fswpr	fspwc	fswprc
Rcopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
Rbopen	100%	100%	100%	100%	100%	100%	100%	10%	30%	0%	0%
Rbcshort	50%	100%	100%	100%	90%	100%	100%	0%	20%	0%	40%
Rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
Rceshort	100%	100%	100%	100%	100%	100%	100%	10%	10%	0%	30%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
Qhi	40%	60%	60%	30%	40%	30%	40%	20%	10%	20%	20%
R1open	100%	100%	100%	100%	100%	100%	100%	0%	0%	20%	100%
R1short	100%	100%	100%	100%	100%	100%	100%	30%	90%	10%	40%
R2open	100%	100%	100%	100%	100%	100%	100%	0%	0%	30%	90%
R2short	100%	100%	100%	100%	100%	100%	100%	0%	0%	70%	100%
R3open	100%	100%	10%	100%	100%	100%	100%	10%	80%	40%	20%
R3short	10%	20%	100%	80%	20%	80%	20%	20%	20%	40%	0%
R4open	100%	100%	100%	100%	100%	100%	100%	10%	10%	40%	40%
R4short	100%	0%	100%	100%	100%	100%	90%	30%	0%	0%	60%

Difference in Input and Output Magnitude Summing

	Cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fspwc	fswprc
Rcopen	100%	60%	100%	100%	100%	100%	100%	40%	30%	0%	0%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
Rbopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	50%
Rbcshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	0%
Rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
Rceshort	100%	100%	100%	100%	60%	100%	100%	50%	10%	0%	0%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
Qhi	20%	70%	30%	30%	20%	20%	30%	10%	0%	0%	80%
R1open	100%	100%	100%	100%	100%	100%	100%	20%	10%	0%	40%
R1short	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	20%
R2open	100%	100%	100%	100%	100%	100%	100%	20%	10%	0%	0%
R2short	100%	100%	100%	100%	100%	50%	100%	0%	0%	0%	0%
R3open	100%	100%	100%	70%	100%	100%	100%	0%	0%	0%	90%
R3short	30%	10%	40%	20%	20%	30%	30%	20%	30%	30%	50%
R4open	100%	100%	100%	100%	100%	100%	100%	10%	10%	10%	30%
R4short	100%	70%	100%	100%	100%	100%	90%	0%	60%	0%	20%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fspwc	fswprc	Total
Rcopen	100%	100%	100%	100%	100%	100%	100%	40%	30%	100%	100%	100%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%	100%
Rbopen	100%	100%	100%	100%	100%	100%	100%	10%	30%	10%	50%	100%
Rbcshort	100%	100%	100%	100%	100%	100%	100%	0%	20%	100%	40%	100%
Rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%	100%
Rceshort	100%	100%	100%	100%	100%	100%	100%	50%	10%	0%	30%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%	100%
Qhi	40%	80%	80%	50%	50%	50%	60%	30%	10%	20%	80%	90%
R1open	100%	100%	100%	100%	100%	100%	100%	20%	10%	20%	100%	100%
R1short	100%	100%	100%	100%	100%	100%	100%	30%	90%	20%	60%	100%
R2open	100%	100%	100%	100%	100%	100%	100%	20%	10%	30%	90%	100%
R2short	100%	100%	100%	100%	100%	100%	100%	0%	0%	70%	100%	100%
R3open	100%	100%	100%	100%	100%	100%	100%	10%	80%	40%	100%	100%
R3short	30%	20%	40%	80%	20%	90%	30%	40%	50%	50%	50%	100%
R4open	100%	100%	100%	100%	100%	100%	100%	20%	20%	40%	40%	100%
R4short	100%	70%	100%	100%	100%	100%	90%	30%	60%	0%	60%	100%

A.8.6.2 Simulation Results at 1KHz, 10 seeds

Overall Fault Coverage = 98.1%

Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
Rcopen	100%	100%	100%	100%	100%	100%	100%	10%	0%	0%	100%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
Rbopen	90%	100%	100%	100%	100%	100%	100%	0%	40%	0%	100%
Rbcshort	100%	100%	100%	100%	100%	100%	100%	10%	30%	10%	50%
Rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
Rceshort	100%	100%	100%	80%	90%	100%	100%	10%	20%	0%	60%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	40%
Qhi	40%	70%	40%	30%	50%	50%	60%	10%	0%	0%	50%
R1open	100%	100%	100%	100%	100%	100%	100%	0%	0%	20%	100%
R1short	100%	100%	100%	100%	100%	100%	100%	30%	90%	10%	40%
R2open	100%	100%	100%	100%	100%	100%	100%	0%	0%	30%	90%
R2short	100%	100%	100%	100%	100%	100%	100%	0%	0%	70%	100%
R3open	100%	100%	100%	100%	100%	100%	100%	10%	80%	40%	20%
R3short	40%	20%	10%	80%	20%	80%	20%	20%	20%	40%	0%
R4open	100%	100%	100%	100%	100%	100%	100%	10%	10%	40%	40%
R4short	100%	10%	100%	100%	100%	100%	90%	30%	0%	0%	60%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
Rcopen	100%	100%	100%	100%	0%	0%	100%	0%	0%	0%	100%
Reopen	100%	100%	100%	100%	0%	0%	100%	0%	0%	60%	100%
Rbopen	100%	100%	40%	100%	0%	0%	100%	20%	0%	80%	100%
Rbcshort	100%	100%	100%	100%	0%	0%	100%	10%	20%	0%	10%
Rbeshort	100%	100%	100%	100%	0%	0%	100%	0%	0%	0%	50%
Rceshort	100%	100%	100%	100%	0%	0%	100%	30%	10%	0%	100%
Qlow	100%	100%	100%	100%	0%	0%	100%	0%	100%	0%	60%
Qhi	100%	50%	20%	20%	0%	10%	40%	10%	0%	40%	20%
R1open	100%	100%	100%	100%	100%	100%	100%	20%	10%	0%	40%
R1short	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	20%
R2open	100%	100%	100%	100%	100%	100%	100%	20%	10%	0%	0%
R2short	100%	100%	100%	100%	100%	50%	100%	0%	0%	0%	0%
R3open	100%	100%	100%	70%	100%	100%	100%	0%	0%	0%	90%
R3short	30%	10%	40%	20%	20%	30%	30%	20%	30%	30%	50%
R4open	100%	100%	100%	100%	100%	100%	100%	10%	10%	10%	30%
R4short	100%	70%	100%	100%	100%	100%	90%	0%	60%	0%	20%

Total Coverage - Both Magnitude and Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	Total
Rcopen	100%	100%	100%	100%	100%	100%	100%	10%	0%	0%	100%	100%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	60%	100%	100%
Rbopen	100%	100%	100%	100%	100%	100%	100%	20%	40%	80%	100%	100%
Rbcshort	100%	100%	100%	100%	100%	100%	100%	20%	40%	10%	80%	100%
Rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%	100%
Rceshort	100%	100%	100%	100%	90%	100%	100%	40%	30%	0%	100%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	100%	100%
Qhi	50%	70%	60%	40%	50%	60%	60%	20%	0%	40%	60%	70%
R1open	100%	100%	100%	100%	100%	100%	100%	20%	10%	20%	100%	100%
R1short	100%	100%	100%	100%	100%	100%	100%	30%	90%	20%	60%	100%
R2open	100%	100%	100%	100%	100%	100%	100%	20%	10%	30%	90%	100%
R2short	100%	100%	100%	100%	100%	100%	100%	0%	0%	70%	100%	100%
R3open	100%	100%	100%	100%	100%	100%	100%	10%	80%	40%	100%	100%
R3short	30%	20%	40%	80%	20%	90%	30%	40%	50%	50%	50%	100%
R4open	100%	100%	100%	100%	100%	100%	100%	20%	20%	40%	40%	100%
R4short	100%	70%	100%	100%	100%	100%	90%	30%	60%	0%	60%	100%

A.8.6.3 Simulation Results at 100KHz, 10 seeds

Overall Fault Coverage = 100%

Magnitude Summing

	cup	cdwn	cud	Cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
Rcopen	0%	100%	0%	100%	100%	100%	100%	20%	10%	50%	30%
Reopen	0%	100%	0%	100%	100%	100%	100%	0%	0%	70%	100%
Rbopen	0%	100%	0%	100%	0%	100%	100%	0%	0%	10%	90%
Rbcshort	0%	100%	0%	100%	100%	100%	100%	0%	50%	50%	60%
Rbeshort	0%	100%	0%	100%	0%	100%	100%	0%	0%	0%	100%
Rceshort	0%	100%	0%	100%	100%	60%	100%	30%	30%	50%	60%
Qlow	0%	100%	0%	100%	100%	100%	100%	10%	30%	10%	10%
Qhi	10%	60%	20%	10%	40%	10%	50%	40%	0%	10%	0%
R1open	10%	100%	0%	100%	100%	100%	100%	0%	0%	20%	100%
R1short	0%	100%	0%	100%	100%	100%	100%	30%	90%	10%	40%
R2open	0%	100%	0%	100%	100%	100%	100%	0%	0%	30%	90%
R2short	0%	100%	0%	100%	100%	100%	100%	0%	0%	70%	100%
R3open	0%	100%	0%	100%	100%	100%	100%	10%	80%	40%	20%
R3short	10%	20%	10%	80%	20%	80%	20%	20%	20%	40%	0%
R4open	0%	100%	0%	100%	100%	100%	100%	10%	10%	40%	40%
R4short	0%	0%	0%	100%	100%	100%	90%	30%	0%	0%	60%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
Rcopen	20%	40%	30%	70%	100%	100%	70%	10%	20%	0%	60%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
Rbopen	10%	100%	100%	90%	0%	100%	100%	10%	60%	0%	40%
Rbcshort	100%	100%	90%	90%	100%	90%	100%	10%	40%	40%	0%
Rbeshort	100%	100%	100%	100%	0%	100%	100%	0%	0%	0%	100%
Rceshort	100%	100%	100%	100%	100%	100%	100%	20%	40%	40%	20%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	20%	0%	80%
Qhi	40%	80%	60%	40%	40%	50%	80%	10%	10%	20%	20%
R1open	100%	100%	100%	100%	100%	100%	100%	20%	10%	0%	40%
R1short	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	20%
R2open	100%	100%	100%	100%	100%	100%	100%	20%	10%	0%	0%
R2short	100%	100%	100%	100%	100%	50%	100%	0%	0%	0%	0%
R3open	100%	100%	100%	70%	100%	100%	100%	0%	0%	0%	90%
R3short	30%	10%	40%	20%	20%	30%	30%	20%	30%	30%	50%
R4open	100%	100%	100%	100%	100%	100%	100%	10%	10%	10%	30%
R4short	100%	70%	100%	100%	100%	100%	90%	0%	60%	0%	20%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fswpr	fswpc	fswprc	Total
Rcopen	20%	100%	30%	100%	100%	100%	100%	30%	30%	50%	60%	100%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	70%	100%	100%
Rbopen	10%	100%	100%	100%	0%	100%	100%	10%	60%	10%	90%	100%
Rbcshort	100%	100%	90%	100%	100%	100%	100%	10%	90%	70%	70%	100%
Rbeshort	100%	100%	100%	100%	0%	100%	100%	0%	0%	0%	100%	100%
Rceshort	100%	100%	100%	100%	100%	100%	100%	50%	70%	80%	80%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	10%	50%	10%	80%	100%
Qhi	40%	80%	70%	50%	40%	50%	80%	50%	10%	30%	20%	100%
R1open	100%	100%	100%	100%	100%	100%	100%	20%	10%	20%	100%	100%
R1short	100%	100%	100%	100%	100%	100%	100%	30%	90%	20%	60%	100%
R2open	100%	100%	100%	100%	100%	100%	100%	20%	10%	30%	90%	100%
R2short	100%	100%	100%	100%	100%	100%	100%	0%	0%	70%	100%	100%
R3open	100%	100%	100%	100%	100%	100%	100%	10%	80%	40%	100%	100%
R3short	30%	20%	40%	80%	20%	90%	30%	40%	50%	50%	50%	100%
R4open	100%	100%	100%	100%	100%	100%	100%	20%	20%	40%	40%	100%
R4short	100%	70%	100%	100%	100%	100%	90%	30%	60%	0%	60%	100%

NOTE: The remaining fault coverage results do not contain results for the 8 hard faults for R1, R2, R3, R4. These faults were not in the original fault list used.

A.8.6.4 Simulation Results at 1MHz, 10 seeds (original 8 faults only)

Overall Fault Coverage = 100%

Magnitude Summing

	cup	cdwn	Cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	100%	100%	0%	100%	100%	100%	100%	30%	20%	50%	0%
reopen	0%	100%	0%	100%	100%	100%	100%	0%	0%	0%	70%
rbopen	100%	100%	0%	100%	100%	100%	100%	0%	0%	10%	30%
rbcshort	100%	100%	0%	100%	100%	100%	100%	50%	50%	40%	10%
rbeshort	0%	100%	0%	100%	100%	100%	100%	0%	0%	0%	0%
rceshort	100%	100%	0%	50%	100%	10%	100%	40%	30%	40%	20%
Qlow	100%	100%	0%	100%	100%	100%	100%	40%	30%	20%	10%
Qhi	10%	60%	10%	10%	40%	10%	60%	0%	30%	50%	10%

Difference in Input and Output Magnitude Summing

	Cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	90%	100%	100%	90%	100%	100%	100%	20%	10%	50%	10%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	0%
rbopen	100%	100%	100%	100%	100%	100%	100%	40%	10%	30%	0%
rbcshort	90%	100%	90%	100%	100%	100%	100%	0%	0%	30%	0%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	0%
rceshort	100%	100%	100%	100%	100%	100%	100%	50%	0%	20%	0%
Qlow	100%	100%	100%	100%	100%	100%	100%	40%	0%	10%	20%
Qhi	70%	80%	70%	60%	40%	60%	80%	50%	10%	50%	0%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	Total
rcopen	100%	100%	100%	100%	100%	100%	100%	50%	30%	80%	10%	100%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	70%	100%
rbopen	100%	100%	100%	100%	100%	100%	100%	40%	10%	30%	30%	100%
rbcshort	100%	100%	90%	100%	100%	100%	100%	50%	50%	40%	10%	100%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	0%	100%
rceshort	100%	100%	100%	100%	100%	100%	100%	90%	30%	40%	20%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	50%	30%	30%	30%	100%
Qhi	80%	80%	80%	60%	40%	60%	80%	50%	40%	80%	10%	100%

A.8.6.5 Simulation Results at 100MHz, 10 seeds (original 8 faults only)

Overall Fault Coverage = 98.8%

Magnitude Summing

	cup	Cdwn	cud	Cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
Rcopen	100%	100%	0%	100%	100%	100%	100%	0%	0%	50%	0%
Reopen	0%	100%	0%	100%	50%	100%	100%	0%	0%	10%	50%
Rbopen	100%	100%	0%	40%	100%	20%	100%	0%	0%	10%	30%
rbcshort	100%	100%	0%	50%	100%	100%	100%	0%	10%	10%	40%
rbeshort	0%	100%	0%	100%	0%	100%	100%	0%	0%	0%	0%
rceshort	100%	100%	0%	40%	100%	40%	100%	0%	20%	0%	40%
Qlow	100%	100%	0%	50%	40%	90%	100%	10%	10%	20%	30%
Qhi	10%	60%	10%	20%	10%	20%	60%	20%	10%	10%	20%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fswpr	fswpc	fswprc
rcopen	90%	100%	100%	100%	100%	100%	100%	0%	100%	0%	10%
reopen	100%	100%	100%	100%	30%	100%	100%	10%	0%	30%	20%
rbopen	100%	100%	100%	100%	100%	100%	100%	0%	90%	10%	10%
rbcshort	90%	100%	90%	100%	100%	100%	100%	20%	30%	10%	10%
rbeshort	100%	100%	100%	100%	0%	100%	100%	0%	0%	100%	0%
rceshort	100%	100%	100%	50%	100%	60%	100%	0%	0%	0%	20%
Qlow	100%	100%	100%	100%	20%	100%	100%	20%	20%	20%	0%
Qhi	70%	80%	70%	10%	10%	10%	80%	10%	10%	10%	20%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	total
rcopen	100%	100%	100%	100%	100%	100%	100%	0%	100%	50%	10%	100%
reopen	100%	100%	100%	100%	50%	100%	100%	10%	0%	40%	70%	100%
rbopen	100%	100%	100%	100%	100%	100%	100%	0%	90%	20%	40%	100%
rbcshort	100%	100%	90%	100%	100%	100%	100%	20%	40%	20%	50%	100%
rbeshort	100%	100%	100%	100%	0%	100%	100%	0%	0%	100%	0%	100%
rceshort	100%	100%	100%	60%	100%	60%	100%	0%	20%	0%	60%	100%
Qlow	100%	100%	100%	100%	60%	100%	100%	20%	30%	30%	30%	100%
Qhi	80%	80%	70%	20%	20%	20%	80%	30%	20%	20%	40%	90%

A.8.6.6 Simulation Results at 1GHz, 10 seeds (original 8 faults only)

Overall Fault Coverage = 100%

Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	50%	0%
reopen	0%	100%	0%	100%	100%	100%	100%	0%	0%	0%	30%
rbopen	100%	100%	100%	0%	100%	10%	40%	10%	30%	10%	0%
rbcshort	100%	100%	100%	50%	100%	100%	100%	10%	30%	40%	10%
rbeshort	0%	100%	0%	100%	100%	100%	100%	10%	10%	0%	0%
rceshort	70%	100%	100%	40%	100%	30%	100%	20%	0%	30%	10%
Qlow	100%	100%	100%	100%	100%	90%	100%	0%	30%	50%	0%
Qhi	10%	70%	10%	20%	50%	20%	80%	20%	10%	10%	0%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	20%	100%	100%	100%	100%	100%	100%	70%	0%	0%	0%
reopen	100%	60%	100%	100%	100%	100%	100%	0%	0%	20%	0%
rbopen	100%	10%	100%	100%	100%	100%	100%	20%	20%	70%	40%
rbcshort	100%	100%	90%	100%	100%	100%	100%	30%	20%	0%	0%
rbeshort	100%	100%	100%	100%	100%	100%	100%	20%	0%	0%	0%
rceshort	100%	100%	100%	70%	100%	80%	100%	0%	0%	0%	30%
Qlow	100%	50%	100%	100%	100%	100%	100%	10%	20%	0%	20%
Qhi	90%	30%	70%	10%	40%	10%	70%	10%	20%	10%	20%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	Cudr	lfsr	fswp	fswpr	fswpc	fswprc	total
rcopen	100%	100%	100%	100%	100%	100%	100%	70%	0%	50%	0%	100%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	20%	30%	100%
rbopen	100%	100%	100%	100%	100%	100%	100%	20%	40%	70%	40%	100%
rbcshort	100%	100%	100%	100%	100%	100%	100%	40%	30%	40%	10%	100%
rbeshort	100%	100%	100%	100%	100%	100%	100%	30%	0%	0%	0%	100%
rceshort	100%	100%	100%	70%	100%	80%	100%	20%	30%	30%	30%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	10%	20%	50%	20%	100%
Qhi	90%	80%	80%	20%	50%	20%	80%	20%	40%	20%	20%	100%

A.8.7 Simulation Results with Component Variation (50 seeds) - Hard Faults

A.8.7.1 Simulation Results at 100Hz, 50 seeds (original 8 faults only)

Overall Fault Coverage = 96.5%

Magnitude Summing

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswpRC
rcopen	100%	100%	100%	100%	100%	100%	100%	0%	4%	0%	0%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
rbopen	100%	100%	100%	100%	100%	100%	100%	4%	22%	0%	0%
rbcshort	52%	100%	100%	100%	64%	100%	98%	0%	2%	0%	6%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
rceshort	100%	100%	100%	100%	100%	100%	100%	14%	6%	0%	16%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	2%	0%	0%
Qhi	8%	54%	8%	4%	10%	8%	12%	4%	4%	2%	10%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswpRC
rcopen	100%	30%	100%	100%	100%	100%	100%	0%	8%	0%	0%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
rbopen	100%	84%	86%	100%	100%	100%	100%	0%	0%	0%	0%
rbcshort	96%	100%	100%	100%	100%	100%	100%	0%	0%	20%	0%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
rceshort	100%	100%	100%	100%	42%	100%	98%	0%	8%	0%	0%
Qlow	100%	100%	90%	100%	100%	100%	100%	0%	2%	0%	0%
Qhi	0%	32%	26%	4%	2%	2%	4%	0%	0%	0%	6%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cuR	cdR	CudR	lfsr	fswp	fswpR	fswpC	fswpRC	Total
rcopen	100%	100%	100%	100%	100%	100%	100%	0%	12%	0%	0%	100%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%	100%
rbopen	100%	100%	100%	100%	100%	100%	100%	4%	22%	0%	0%	100%
rbcshort	96%	100%	100%	100%	100%	100%	100%	0%	2%	20%	6%	100%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%	100%
rceshort	100%	100%	100%	100%	100%	100%	100%	14%	8%	0%	16%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	2%	0%	0%	100%
Qhi	8%	64%	32%	12%	12%	10%	16%	4%	4%	2%	10%	72%

A.8.7.2 Simulation Results at 1KHz, 50 seeds (original 8 faults only)

Overall Fault Coverage = 93.5%

Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	Fswpr	fswpc	fswprc
rcopen	100%	100%	100%	100%	100%	100%	100%	10%	0%	0%	68%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
rbopen	84%	100%	100%	100%	100%	100%	100%	0%	16%	0%	16%
rbcshort	100%	100%	100%	100%	100%	100%	100%	2%	10%	0%	48%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%
rceshort	100%	100%	100%	68%	92%	100%	100%	2%	18%	0%	44%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	10%
Qhi	14%	22%	6%	18%	18%	8%	22%	4%	6%	0%	4%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	100%	100%	100%	100%	0%	0%	100%	0%	0%	0%	0%
reopen	100%	100%	100%	100%	0%	0%	100%	0%	0%	0%	0%
rbopen	100%	100%	18%	100%	0%	0%	100%	4%	0%	10%	92%
rbcshort	100%	100%	100%	100%	0%	0%	100%	4%	0%	0%	20%
rbeshort	100%	100%	100%	100%	0%	0%	100%	0%	0%	0%	0%
rceshort	100%	100%	100%	100%	0%	0%	100%	0%	16%	0%	2%
Qlow	100%	100%	100%	100%	0%	0%	100%	0%	56%	0%	30%
Qhi	4%	14%	10%	4%	0%	6%	14%	0%	4%	8%	0%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	Total
Rcopen	100%	100%	100%	100%	100%	100%	100%	10%	0%	0%	68%	100%
Reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%	100%
Rbopen	100%	100%	100%	100%	100%	100%	100%	4%	16%	10%	100%	100%
Rbcshort	100%	100%	100%	100%	100%	100%	100%	6%	10%	0%	60%	100%
Rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	100%	100%
Rceshort	100%	100%	100%	100%	92%	100%	100%	2%	34%	0%	46%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	0%	56%	0%	40%	100%
Qhi	18%	22%	16%	22%	18%	14%	22%	4%	10%	8%	4%	48%

A.8.7.3 Simulation Results at 1MHz, 50 seeds (original 8 faults only)

Overall Fault Coverage = 96%

Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	0%	100%	0%	100%	100%	100%	100%	0%	0%	24%	10%
reopen	0%	100%	0%	100%	0%	100%	100%	0%	0%	2%	26%
rbopen	0%	100%	0%	100%	0%	96%	100%	0%	0%	6%	20%
rbcshort	0%	100%	0%	100%	100%	100%	100%	4%	0%	14%	8%
rbeshort	0%	100%	0%	100%	0%	100%	100%	0%	0%	0%	0%
rceshort	0%	100%	0%	40%	100%	20%	100%	4%	0%	12%	4%
Qlow	0%	100%	0%	100%	0%	100%	100%	0%	0%	2%	10%
Qhi	4%	42%	4%	6%	48%	6%	42%	4%	0%	14%	12%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	28%	96%	34%	66%	100%	98%	100%	0%	6%	6%	0%
reopen	100%	100%	100%	100%	0%	100%	100%	0%	2%	4%	4%
rbopen	98%	100%	100%	100%	100%	100%	100%	2%	8%	2%	0%
rbcshort	42%	100%	52%	100%	100%	100%	100%	4%	4%	4%	0%
rbeshort	100%	100%	100%	100%	0%	100%	100%	0%	0%	0%	0%
rceshort	100%	100%	100%	100%	100%	100%	100%	2%	0%	2%	0%
Qlow	100%	100%	100%	100%	0%	100%	100%	2%	0%	0%	2%
Qhi	20%	40%	20%	20%	48%	18%	40%	0%	4%	4%	0%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	total
rcopen	28%	100%	34%	100%	100%	100%	100%	0%	6%	28%	10%	100%
reopen	100%	100%	100%	100%	0%	100%	100%	0%	2%	6%	30%	100%
rbopen	98%	100%	100%	100%	100%	100%	100%	2%	8%	8%	20%	100%
rbcshort	42%	100%	52%	100%	100%	100%	100%	6%	4%	16%	8%	100%
rbeshort	100%	100%	100%	100%	0%	100%	100%	0%	0%	0%	0%	100%
rceshort	100%	100%	100%	100%	100%	100%	100%	6%	0%	14%	4%	100%
Qlow	100%	100%	100%	100%	0%	100%	100%	2%	0%	2%	12%	100%
Qhi	24%	42%	24%	22%	48%	22%	42%	4%	4%	18%	12%	68%

A.8.7.4 Simulation Results at 10MHz, 50 seeds (original 8 faults only)

Overall Fault Coverage = 95.3%

Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	0%	100%	0%	100%	100%	100%	100%	0%	0%	6%	0%
reopen	0%	100%	0%	0%	100%	0%	100%	0%	0%	0%	0%
rbopen	0%	100%	0%	100%	100%	100%	100%	0%	0%	0%	0%
rbcshort	0%	100%	0%	100%	100%	100%	100%	0%	2%	0%	0%
rbeshort	0%	100%	0%	0%	100%	0%	100%	0%	0%	0%	0%
rceshort	0%	100%	0%	52%	100%	42%	100%	0%	2%	0%	4%
Qlow	0%	100%	0%	100%	100%	100%	100%	2%	6%	2%	0%
Qhi	6%	42%	6%	2%	48%	4%	42%	0%	2%	2%	0%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc
rcopen	28%	100%	34%	12%	100%	46%	100%	0%	6%	0%	12%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	6%
rbopen	100%	100%	100%	100%	100%	100%	100%	4%	8%	4%	0%
rbcshort	66%	100%	66%	100%	100%	100%	100%	2%	4%	0%	4%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%
rceshort	100%	100%	100%	100%	100%	100%	100%	0%	2%	2%	10%
Qlow	100%	100%	100%	100%	100%	100%	100%	2%	0%	8%	6%
Qhi	20%	40%	20%	18%	6%	18%	40%	2%	6%	8%	2%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fswpr	fswpc	fswprc	total
rcopen	28%	100%	34%	100%	100%	100%	100%	0%	6%	6%	12%	100%
reopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	10%	6%	100%
rbopen	100%	100%	100%	100%	100%	100%	100%	4%	8%	4%	0%	100%
rbcshort	66%	100%	66%	100%	100%	100%	100%	2%	4%	0%	4%	100%
rbeshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	0%	0%	100%
rceshort	100%	100%	100%	100%	100%	100%	100%	0%	4%	2%	14%	100%
Qlow	100%	100%	100%	100%	100%	100%	100%	4%	6%	10%	6%	100%
Qhi	26%	42%	26%	20%	48%	20%	42%	2%	8%	10%	2%	62%

Appendix 9
Low Pass Filter (Lucent Tech.)

A.9.1 Spice File with Fault Models for Simulation

This file has been modified from the Hspice version on the UK VLSI-FPGA Design & Test web site in order to facilitate the use of the Statistical Fault Analyzer.

```
*Lowpass RC filter
vck 100 0
vin 2 0
%dc 100 12 2
*opamp1
R1 1 14 [110,6.6]k
M1 1 1 99 99 modp1 L=4U W=150U
R2 99 13 1
R3 1 13 [100,0]meg
.model modp1 pmos(RS=[0,0])
M2 3 1 98 98 modp2 L=4U W=35U
R4 98 13 1
R5 3 13 [100,0]meg
.model modp2 pmos(RS=[0,0])
M3 9 1 97 97 modp3 L=4U W=100U
R6 9 13 1
R7 9 13 [100,0]meg
.model modp3 pmos(RS=[0,0])
M4 4 12 96 96 modp4 L=4U W=60U
R8 3 96 1
R9 4 96 [100,0]meg
.model modp4 pmos(RS=[0,0])
M5 5 11 95 95 modp5 L=4U W=60U
R10 95 3 1
R11 5 95 [100,0]meg
.model modp5 pmos(RS=[0,0])
cl 5 16 [1.27,.0762]pf
R12 5 16 [100,0]meg
R13 16 6 1
Rl 6 9 [8.75,0.525]k
M6 4 4 94 94 modn6 L=4U W=27.5U
R14 94 14 1
R15 4 94 [100,0]meg
.model modn6 nmos(RD=[0,0])
M7 5 4 93 93 modn7 L=4U W=27.5U
R16 93 14 1
R17 5 93 [100,0]meg
```

```
.model modn7 nmos(RD=[0,0])
M8 9 5 92 92 modn8 L=4U W=100U
R18 92 14 1
R19 9 92 [100,0]meg
.model modn8 nmos(RD=[0,0])
VDD 13 0 5
VSS 14 0 -5
RL 18 0 0
Co 16 0 2e-12
*end opamp1
*MAIN CIRCUIT
VCC 13 0 15.0
VEE 14 0 -15.0
R1LP 2 11 [1.0,0.07]K
R2LP 9 12 [1.5,0.105]K
R3LP 9 0 [15.0,2.25]K
C1LP 33 [0 0.01,0.7]uf
Rcse 11 33 1
Rcpl 33 0 [100,0]meg
.print tran v(100) v(12) v(2)
.options nopage noecho nomod numdgt=3
.end
```

A.9.2 Hard Fault List Supplied to SFA

This fault list is used to simulate all hard faults in the Low-Pass Filter circuit.

```
#R1LP 1e4 1 R1LP_open
#R1LP .01 1 R1LP_short
#R2LP .01 1 R2LP_short
#R2LP 1e7 1 R2LP_open
#R3LP .01 1 R3LP_short
#R3LP 1e7 1 R3LP_open
#C1LP 1e4f 1 C1LP_open
#C1LP .001nf 1 C1LP_short
#R1 .01 1 R1_short
#R1 1e7 1 R1_open
#RL .01 1 R1_short
#RL 1e4 1 R1_open
#CL 1e4f 1 C1_open
#CL .001nf 1 C1_short
#modp1 1e7 1 m1_off RS
#modp2 1e7 1 m2_off RS
#modp3 1e7 1 m3_off RS
#modp4 1e7 1 m4_off RS
#modp5 1e7 1 m5_off RS
#modn6 1e7 1 m6_off RD
#modn7 1e7 1 m7_off RD
#modn8 1e7 1 m8_off RD
#R3 1 1 m1_on
#R5 1 1 m2_on
#R7 1 1 m3_on
#R9 1 1 m4_on
#R11 1 1 m5_on
#R15 1 1 m6_on
#R17 1 1 m7_on
#R19 1 1 m8_on
```

A.9.3 Soft Fault List Supplied to SFA

This fault list is used to simulate all soft faults in the Low-Pass circuit.

```
#R1 580 1 R1_low
#R1 1420 1 R1_high
#R2 870 1 R2_low
#R2 2130 1 R2_high
#R3 1500 1 R3_low
#R3 28500 1 R3_high
#C2 5.8e-9 1 C2_low
#C2 14.2e-9 1 C2_high
```

A.9.4 Simulation Results with No Component Variation -Hard Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	10KHZ	1MHZ	100MHZ
R1LPopen	1	1	1
R1LPshort	1	1	1
R2LPopen	1	1	1
R2LPshort	1	1	1
R3LPopen	1	1	1
R3LPshort	1	1	1
R1open	1	1	1
R1short	0	1	1
RLshort	1	1	1
RLopen	1	1	1
C1open	1	1	1
C1short	0	1	1
C1LPopen	1	1	1
C1LPshort	1	1	1
M1off	1	1	1
M1on	1	1	1
M2off	1	1	1
M2on	1	1	1
M3off	1	1	1
M3on	1	1	1
M4off	1	1	1
M4on	1	1	1
M5off	1	1	1
M5on	1	1	1
M6off	1	1	1
M6on	1	1	1
M7off	1	1	1
M7on	1	1	1
M8off	1	1	1
M8on	1	1	1
	93.3%	100.0%	100.0%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	Cud	cuR	cdR	CudR	lfsr	fswp	fswpR	fswpC	fswpRC
10KHZ	87%	90%	90%	93%	93%	90%	90%	90%	90%	90%	90%
1MHZ	97%	97%	97%	100%	100%	97%	100%	97%	100%	100%	100%
100MHZ	100%	100%	97%	100%	100%	100%	100%	0%	7%	0%	0%

A.9.5 Simulation Results with No Component Variation - Soft Faults

Individual Fault Detection and Overall Fault Coverage Versus Frequency

NOTE: On this chart, a 1 indicates 100% fault detection; a 0 indicates 0% fault detection.

	100KHZ
R1low	1
R1high	1
R2low	1
R2high	1
R3low	1
R3high	1
C1low	1
C1high	1
	100%

Fault Coverage Per Waveform Versus Frequency

	cup	cdwn	cud	cuR	cdR	cudR	lfsr	fswp	fswpR	fswpC	fswprc
100KHz	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.9.6 Simulation Results with Component Variation - Hard Faults

A.9.6.1 Simulation Results at 1KHz, 10 seeds

Overall Fault Coverage = 83.7%

Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
R1LPopen	100%	100%	100%	100%	100%	100%	100%	60%	80%	20%	40%
R1LPshort	30%	30%	30%	50%	50%	50%	30%	50%	50%	0%	50%
R2LPopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	20%	30%
R2LPshort	100%	100%	100%	100%	100%	100%	100%	50%	100%	20%	0%
R3LPopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	10%
R3LPshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
R1open	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
R1short	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
RLshort	100%	100%	100%	100%	100%	100%	100%	60%	100%	0%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
C1open	20%	20%	20%	10%	10%	10%	10%	10%	20%	0%	20%
C1short	20%	20%	20%	10%	10%	10%	10%	10%	20%	0%	20%
C1LPopen	20%	20%	20%	10%	20%	20%	20%	10%	20%	10%	20%
C1LPshort	20%	20%	20%	20%	20%	20%	20%	10%	20%	10%	20%
M1off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	3%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M2off	20%	20%	20%	20%	20%	20%	20%	30%	20%	0%	0%
M2on	100%	100%	100%	100%	100%	100%	100%	100%	100%	20%	10%
M3off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	0%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	30%	30%
M4on	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%
M5off	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	90%	90%	20%	0%
M6on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	40%	40%	20%	10%
M7on	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%
M8off	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Difference in Input and Output Magnitude Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
R1LPopen	100%	100%	100%	100%	100%	100%	100%	100%	40%	40%	0%
R1LPshort	50%	50%	50%	50%	60%	50%	50%	50%	50%	20%	0%
R2LPopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	40%	0%
R2LPshort	100%	100%	100%	100%	100%	100%	100%	60%	100%	0%	0%
R3LPopen	100%	100%	100%	100%	100%	100%	100%	100%	70%	80%	0%
R3LPshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%
R1open	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
R1short	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
RLshort	100%	100%	100%	100%	100%	100%	100%	60%	100%	0%	30%
RLopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
C1open	0%	0%	0%	10%	10%	10%	10%	10%	0%	0%	0%
C1short	0%	0%	0%	10%	10%	10%	10%	10%	0%	0%	0%
C1LPopen	0%	10%	0%	10%	10%	20%	0%	20%	10%	0%	20%
C1LPshort	0%	10%	0%	20%	10%	20%	0%	20%	10%	0%	20%
M1off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
M2off	20%	20%	20%	20%	10%	20%	20%	10%	10%	0%	0%
M2on	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	20%
M3off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	0%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	10%	0%
M4on	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	0%
M5off	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	0%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
M6off	100%	100%	100%	100%	100%	100%	100%	90%	90%	30%	10%
M6on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%
M7off	100%	100%	100%	100%	100%	100%	100%	30%	100%	10%	20%
M7on	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	0%
M8off	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	0%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	0%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc	total
R1LPopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	50%	40%	100%
R1LPshort	50%	50%	50%	50%	60%	50%	50%	50%	50%	20%	50%	60%
R2LPopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	60%	30%	100%
R2LPshort	100%	100%	100%	100%	100%	100%	100%	60%	100%	20%	0%	100%
R3LPopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	80%	10%	100%
R3LPshort	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	100%
R1open	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
R1short	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
RLshort	100%	100%	100%	100%	100%	100%	100%	60%	100%	0%	100%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
C1open	20%	20%	20%	10%	10%	10%	10%	10%	20%	0%	20%	40%
C1short	20%	20%	20%	10%	10%	10%	10%	10%	20%	0%	20%	40%
C1LPopen	20%	30%	20%	20%	20%	20%	20%	20%	20%	10%	40%	70%
C1LPshort	20%	30%	20%	20%	20%	20%	20%	20%	20%	10%	40%	70%
M1off	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%	30%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M2off	30%	30%	30%	20%	20%	20%	30%	30%	20%	0%	0%	30%
M2on	100%	100%	100%	100%	100%	100%	100%	100%	100%	30%	30%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	100%	0%	0%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	100%	100%	40%	30%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	90%	90%	50%	10%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	40%	100%	30%	3%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	90%	90%	0%	20%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

A.9.6.2 Simulation Results at 1MHz, 10 seeds

Overall Fault Coverage = 100%

Magnitude Summing

	cup	cdwn	Cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
R1LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R1LPshort	100%	100%	100%	100%	100%	100%	100%	0%	10%	100%	100%
R2LPopen	100%	100%	100%	100%	100%	100%	100%	20%	0%	100%	100%
R2LPshort	100%	100%	100%	100%	100%	100%	100%	10%	0%	100%	100%
R3LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R3LPshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
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R1short	100%	100%	0%	100%	100%	0%	0%	0%	0%	0%	0%
RLshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
C1open	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
C1short	0%	0%	0%	100%	100%	100%	0%	0%	0%	100%	100%
C1LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
C1LPshort	100%	100%	100%	100%	100%	100%	100%	0%	20%	100%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%

Difference in Input and Output Magnitude Summing

	cup	Cdwn	cud	cur	cdr	cudr	lfsr	fswp	fspwr	fswpc	fswprc
R1LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R1LPshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R2LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R2LPshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R3LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
R3LPshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
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R1short	100%	100%	0%	100%	100%	100%	0%	0%	0%	0%	0%
RLshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
C1open	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
C1short	0%	0%	0%	100%	100%	100%	0%	0%	0%	100%	100%
C1LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
C1LPshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
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M2on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M3off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M3on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%

Total Coverage - Both Magnitude and Summing

	cup	cdwn	cud	cur	cdr	cudr	Lfsr	fswp	fspwr	fswpc	fswprc	total
R1LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
R1LPshort	100%	100%	100%	100%	100%	100%	100%	0%	10%	100%	100%	100%
R2LPopen	100%	100%	100%	100%	100%	100%	100%	20%	0%	100%	100%	100%
R2LPshort	100%	100%	100%	100%	100%	100%	100%	10%	0%	100%	100%	100%
R3LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
R3LPshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
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R1short	100%	100%	0%	100%	100%	100%	0%	0%	0%	0%	0%	100%
RLshort	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
RLopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
C1open	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
C1short	0%	0%	0%	100%	100%	100%	0%	0%	0%	100%	100%	100%
C1LPopen	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
C1LPshort	100%	100%	100%	100%	100%	100%	100%	0%	20%	100%	100%	100%
M1off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M1on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M2off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M2on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
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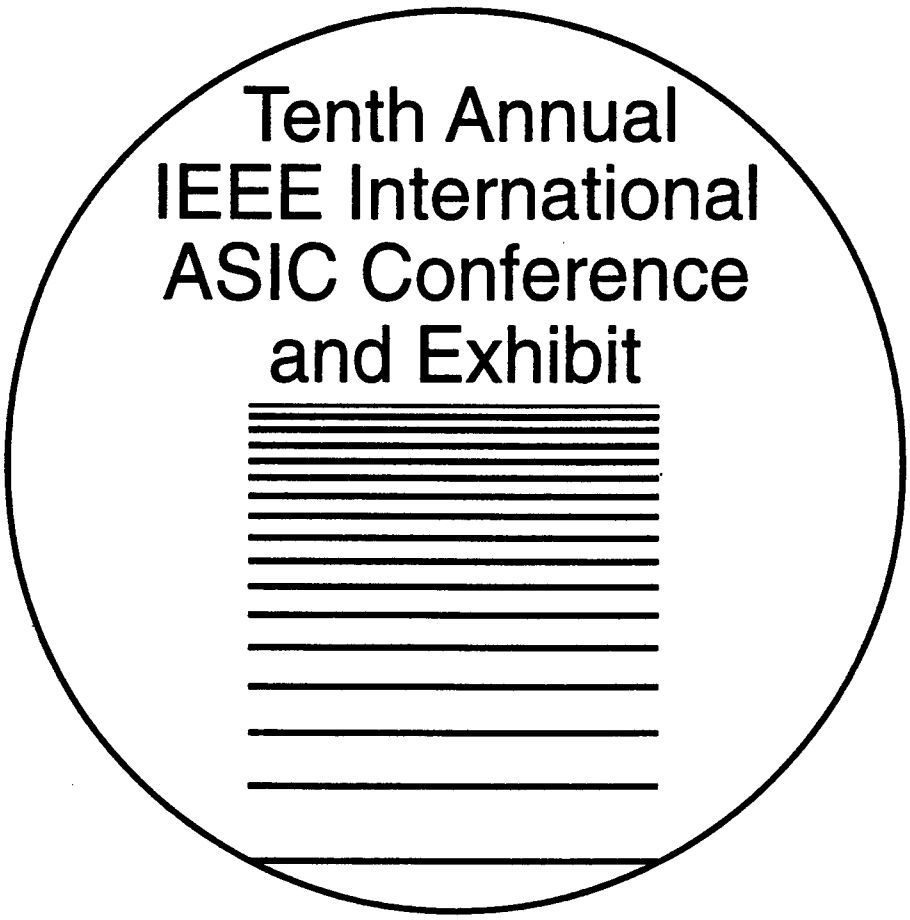
M3on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M4off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M4on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M5off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M5on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M6off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M6on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M7off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M7on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M8off	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%
M8on	100%	100%	100%	100%	100%	100%	100%	0%	0%	100%	100%	100%

Attachments

Published conference papers in the following order

- C. Stroud, P. Karunaratna, and E. Bradley, "Digital Components for Built-In Self-Test of Analog Circuits", Proc. IEEE International Application Specific Integrated Circuits Conf., pp. 47-51, 1997.
- R. Kondagunturi, E. Bradley, K. Maggard, and C. Stroud, "Benchmark Circuits for Analog and Mixed-Signal Testing", Proc. IEEE Southeast Regional Conf., pp. 217-220, 1999.
- B. Lewis, S. Lim, R. Puckett, and C. Stroud, "A Prototype Unit for Built-In Self-Test of Analog Circuits", Proc. IEEE Southeast Regional Conf., pp. 221-224, 1999.
- K. Maggard and C. Stroud, "Built-In Self-Test for Analog Circuits in Mixed-Signal Systems", Proc. IEEE Southeast Regional Conf., pp. 225-228, 1999.

PROCEEDINGS



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Digital Components for Built-In Self-Test of Analog Circuits

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Abstract: We describe the design and operation of a digital test pattern generator (TPG) along with three accumulator based output response analysis (ORA) circuits that are targeted for implementing Built-In Self-Test (BIST) for analog circuits in mixed signal based ASICs. The test patterns produced by the TPG include ramps, triangle and square waves, pseudo-random noise, and a frequency sweep capability for testing the frequency response of the analog circuit under test. The ORA circuits include single and double precision as well as residue accumulators for magnitude and phase measurements. We include an overview of the complete mixed signal based BIST architecture and simulation system along with the results of our initial application of the BIST architecture to an analog circuit under test.[1]

1. Introduction

The overall objective of this research and development project is to investigate, develop, and evaluate a Built-In Self-Test (BIST) approach for analog circuitry which resides in mixed signal VLSI devices and systems. Mixed signal circuits and systems provide an excellent environment to develop Built-In Self-Test (BIST) approaches for analog circuits and systems. Mixed signal environments allow the experience and expertise that has been gained over the past 17 years of BIST development in digital circuitry to be used as a platform for the investigation of analog BIST techniques. In particular, the basic components of most BIST structures may be incorporated into the digital portion of the design and without adverse effects on the analog circuit performance that would be incurred if the BIST circuitry were to be inserted in the analog portion of the design. These digital components include test pattern generator (TPG) and output response analyzer (ORA) functions as well as the necessary test controller function to initialize and control the BIST sequence and provide system level access for off-line testing of the circuit or system [1-3]. However, it is important to note that there are different requirements that must be considered in analog BIST which prevent the straight forward application of conventional digital TPG and ORA functions. In this paper, we discuss those issues with respect to the design of digital TPGs and ORAs targeted for the testing of analog circuits. We begin with the overview of the proposed mixed signal based BIST architecture for analog circuits in Section 2 followed by a more detailed discussion of issues associated with the TPG design in Section 3. In Section 4, we discuss ORA design issues and we present an overview of the BIST simulation environment in Section 5. The paper concludes in Section 6 with a summary of the results obtained with our initial application of the BIST approach to an analog circuit.

2. BIST Architecture

The proposed mixed signal based BIST architecture for analog circuits is shown in Figure 1 with the additional BIST circuitry shown in bold and the analog circuitry under test shown in shades of grey. The normal system components include the digital system functions (here we assume two-way transmission of both digital and analog signals) as well as the analog system functions along with the Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) that would normally be required to convert the digital signals to analog waveforms and vice versa. The proposed additions to the mixed signal system include the digital TPG and ORA functions as well as a digital test controller and analog loopback capabilities to facilitate the return path for the test signals to the ORA. An additional multiplexer (MUX) is required for the insertion of the digital test patterns into the data stream. Since the target circuitry under test is the analog system circuits, including the DACs and ADCs, we incorporate the digital TPG and its associated MUX immediately prior to the digital inputs of the DAC.

One of the principle specifications that should be adhered to in order to maximize the value and effectiveness of this approach is that the complete BIST system be accessible and usable during system-level operation for off-line testing and system diagnostics. This, in turn, requires that the BIST circuitry be capable of proper initialization of the circuitry under test, isolation of system data inputs, and reproducible results from one execution of the BIST sequence to the next in the same manner as is required in digital systems [3]. These essential functions are typically governed by the test controller which is often implemented as part of or in conjunction with the TPG. The test controller, although often overlooked, is an important circuit in terms of its effect on analog BIST. Aside from controlling the length of the BIST sequence to ensure reproducible results, particularly during system level testing, the initialization sequence, also a function of the test controller, is just as important to obtaining reproducible results during system-level testing.

1. Effort sponsored by Rome Laboratory, Air Force Material Command, USAF, under agreement number F30602-97-1-0042. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright annotation thereon.

The length of the initialization sequence should be a function of the longest time constant in the analog circuit as well as the length of time required to clear the effects of previous system signals in the feedback circuits in the analog circuitry.

Control of the analog loopback function(s) may be assigned to the test controller, however, it is often best to control these loopback functions independently in order to achieve optimal diagnostic resolution in the analog circuit under test. For example, with the left-hand analog loopback shown in Figure 1 activated, any faults detected are isolated to the path from the TPG to the ORA, as shown by the dark grey bordered analog circuitry and paths in Figure 1. If the BIST sequence indicates a good circuit, then the left-hand analog loopback can be deactivated while the right-hand loopback function can be activated further down the output signal path and the BIST re-executed. Faults detected during this second BIST sequence would be isolated to the analogi circuitry shown in light grey in Figure 1. In this manner, the BIST sequence can be executed any number of times with various configurations of loopback functions to effectively isolate the fault(s) in the system to a given section of analog circuitry. However, to ensure that this diagnostic resolution can be realized, the length of the initialization sequence must be sufficient to accommodate the longest analog path in the circuit with its associated time constants and feedback circuits considered.

Within the constraints of the objective of accessibility and use of the BIST circuitry during system-level testing, high fault coverage along with minimal area overhead and performance penalties are critical for the practical application of this BIST approach [7]. In the subsequent sections, we describe the design and operation of the TPG and ORA functions we have designed and are currently evaluating for this BIST approach

3. Test Pattern Generation

Digital TPG functions offer a wealth of types of test patterns to evaluate for their effectiveness in mixed signal based analog BIST applications. We have designed, simulated, and verified an 8-bit TPG circuit that is modular such that it can be easily modified to create a TPG of any desired bit size. Our basic TPG design includes a binary counter and a Linear Feedback Shift Register (LFSR). The counter operates in a number of different modes to provide a variety of analog test patterns. For example, a single pass through the up-count range of the binary counter produces a ramp signal. Ramp input signals have been used in recent analog testing techniques and have been found to provide good fault detection results, in some cases, better results than sinusoid test signals [4,5]. It has been observed that faults in analog circuits can cause detectable variations in output response delay, rise/fall times, and overshoot when stimulated by certain input test signals. But it has also been observed that the detectability of faults with respect to the input test signal can vary with the type of analog circuit under test [5]. Multiple passes through the up-count or down-count range produces a saw-tooth analog test signal; combining the up-count and down-count generates a triangular waveform at the output of the DAC.

The LSFR mode of operation in the TPG, on the other hand, produces an analog signal that is more noise-like in it's properties. During analysis of the analog test patterns produced by internal and external feedback LFSRs, we found no significant difference in the two types of LFSR implementations. We had originally thought there would be a noticeable difference due to the way in which the feedback implementation of the two types of LFSRs differ. As a result, we concluded that only one type (we chose the internal-type feedback) LFSR with a programmable characteristic polynomial would be incorporated in the TPG design. In order to take into consideration the shifting of data values in the LFSR, we investigated the reversal of the ordering of the bits applied to the DAC for generation of the analog test patterns; in other words, the most significant bit of the binary value of the test pattern produced by the TPG becomes the least significant bit and vice versa. But, we found nothing of significance with respect to the LFSR test patterns. However, when we investigated the same bit reversal effect for the counter modes of operation we found that the test patterns looked much more like white noise. This is illustrated in Figure 2 where the triangular wave produced by a 4-bit up-down counter is shown along with the waveform produced by the reversal of the bits in the binary count value when applied to the DAC. As a result, we have included the bit reversal for all modes of operation of the TPG in order to study the fault detection capability of these patterns in the analog circuitry under test.

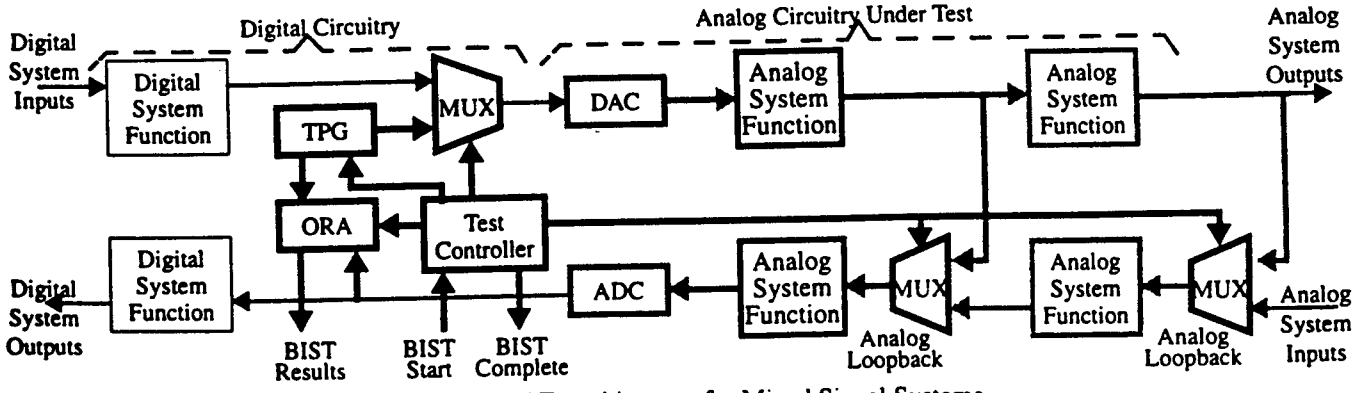

Figure 1. BIST Architecture for Mixed Signal Systems.

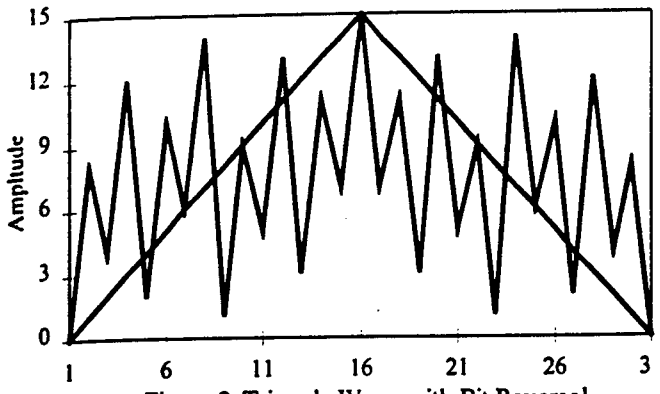

Figure 2. Triangle Wave with Bit Reversal

Since the frequency response of analog circuits can be expected to be important in terms of fault detection capability, square waves that span a wide frequency range are also produced from the TPG design. The frequency sweep mode of operation in the TPG provides a square wave test pattern which progressively increases in frequency. The square wave begins with a half period of 255 clock cycles and decreases by one clock cycle during each subsequent half cycle of the square wave until the last half period is one clock cycle in duration. At the same time, the amplitude increases by a value of 2 with each cycle of the square wave. This is illustrated in Figure 3 for a simple 4-bit counter design and can be understood more clearly from the following description of the TPG design.

The main components of the TPG design are shown in the block diagram of Figure 4 and include the 8-bit counter/LFSR, an additional 1-bit counter, multiplexers for bit reversal, multiplexers for the frequency sweep capability, and a count value holding register (also for the frequency sweep). The ordering of the bits of any set of test patterns can be reversed using the control input to the bit reversal multiplexer. The counter outputs (either reversed or not via the bit reversal multiplexer), are used to generate the frequency sweep. When the frequency sweep function is enabled, the TPG output multiplexer selects the outputs of the AND gates. These AND gates are used to set the magnitude of the square wave generated whenever the output of the 1-bit counter is a logic one. The output values of the count value holding register are loaded into the counter/LFSR and enable the TPG to generate a square wave which sweeps through a variety of

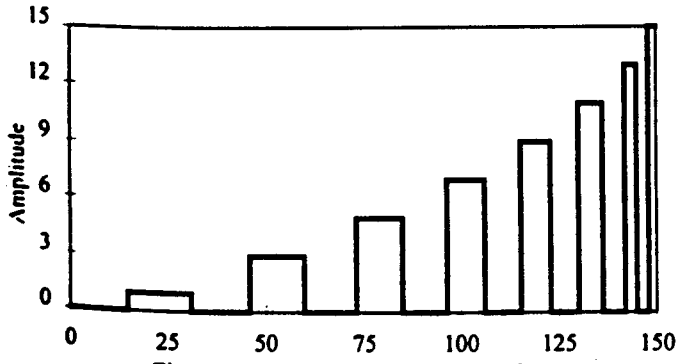

Figure 3. Frequency Sweep Waveform

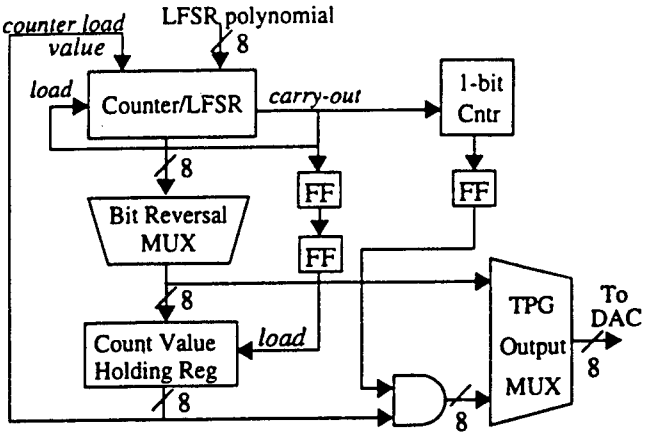

Figure 4. TPG Block Diagram

frequencies. The count value holding register is initialized to a value of all zeros at the beginning of the frequency sweep. Two clock cycles after the counter is loaded as a result of the carry-out of the counter, the count value holding register is loaded with the contents of the counter such that count value is incremented by the counter prior to being loaded into the holding register where it is held until the end of the current count. As a result, the square wave generated progressively becomes shortened in terms of the period. Enabling the bit reversal during a frequency sweep mode will load non-sequential values into the counter value holding register, instead of consecutively increasing numbers, such that the frequencies and amplitudes of the square wave signal being generated will appear to be more random in nature.

4. Output Response Analyzers

It is evident that traditional signature analysis using LFSR-based Signature Analysis Registers (SARs) and Multiple Input Signature Registers (MISRs) is unsuitable for application to analog BIST since the good circuit signature is based on the assumption that an exact sequence of output patterns is produced in every fault-free circuit. Similarly, traditional syndrome analysis, such as ones counting or transition counting, is also unacceptable since an exact output response sequence is assumed in every fault-free execution of the BIST sequence. In an analog circuit, the sampling noise in the DACs and ADCs as well as processing (i.e., tolerances) and environmental (i.e., temperature and voltage) variations in the analog circuitry will prevent reproducible traditional BIST signatures from one execution of the BIST sequence to the next.

A digital accumulator, on the other hand, can be used to obtain the sum of the magnitudes of the sampled output responses from the analog circuitry under test. The accumulator-based ORA facilitates the determination of the pass/fail status of the BIST by expecting the final sum to be within a predetermined range of values. Determination of this range of resultant values, which indicate that the circuit is fault-free, is based on specifications of the analog circuit responses to various input signals produced by the TPG under acceptable analog component parameter variations. An analog checksum circuit has been previously proposed for BIST of analog

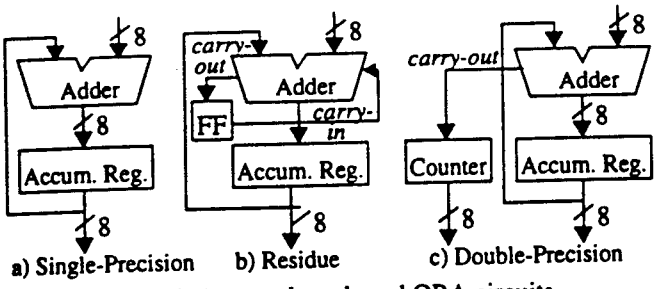

Figure 5. Accumulator based ORA circuits.

circuits [4] but the advantage of a digital ORA is that the results can be read directly through system digital interfaces without the need for additional ADCs to retrieve the BIST results during system level testing.

Three types of 8-bit accumulator based ORA circuits were designed, simulated, and verified; these are illustrated in Figure 3 and include: a) single-precision, b) residue, and c) double-precision accumulators. The design of each ORA is modular such that it can easily be modified to create an ORA of any desired size. Each ORA circuit has three modes of operation including clear, hold, and accumulate. In the single-precision accumulator, the 8-bit incoming binary value is added to the contents of the 8-bit accumulator register with the carry-in set to zero and the carry-out ignored. In the double-precision accumulator, the 8-bit incoming binary value is added to the contents of a 16-bit accumulator register with the carry-in set to zero; note that the carry-out of the 8-bit addition is not ignored but is accumulated by the additional 8-bit incrementing register. In the residue accumulator, the 8-bit incoming binary value is added to the contents of the 8-bit accumulator register while the carry-out is delayed by one clock cycle and used as the carry-in during the next addition.

5. BIST Simulation Environment

Digital fault simulations of the TPG with each of the three different ORAs provided greater than 96% single stuck-at gate level fault coverage in each case with the undetected faults resulting from invalid combinations of TPG control inputs. High fault coverage of the TPG/ORA combination ensures that the additional BIST logic is being thoroughly tested. However, in the application to analog circuitry, we expect that a range of resultant BIST values will be acceptable to account for variations in the analog components. This lead us to investigate how many (if any) of the faults in the TPG/ORA will go undetected as a result of considering a range of acceptable BIST result values and how the digital circuitry fault coverage will change with changes in the range of acceptable BIST result values. During digital fault simulation of the TPG and ORA (which is equivalent to assuming no variation in the analog circuit), we recorded the resulting ORA signature for each digital fault detected and compared the fault coverage to a possible range of acceptable BIST resul values to determine whether TPG/ORA faults will be detected. The results of these simulations are illustrated in Figure 6 where the fault coverage for the digital BIST circuitry is given as a function of the difference between the faulty circuit accumulator value and the fault-free circuit

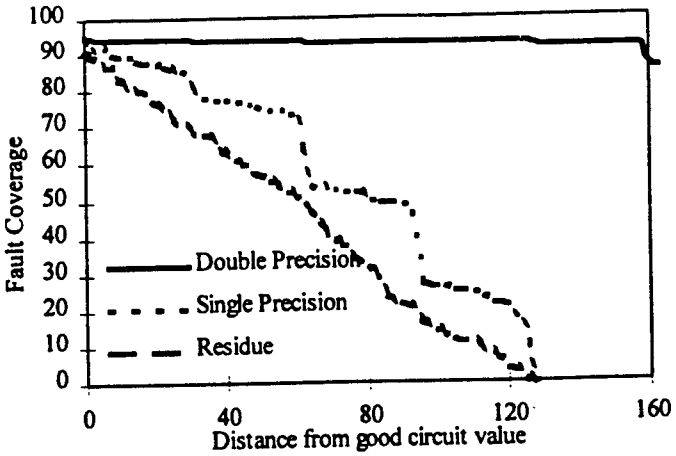

Figure 6. Digital Fault Coverage vs. Accumulator Value

accumulator value. As can be seen from the graph, the residue ORA is the worst performer with an almost linear decrease in fault coverage vs. the distance from the good circuit accumulator value. Conversely, the double precision ORA looses very little fault coverage within a range of +/-150 of the good circuit accumulator value, however, this is out of a possible range of +/-32,768 for the 16-bit double precision accumulator. As a result, we inserted a loopback multiplexer at the input to the ORA to facilitate testing the BIST circuitry independent of the analog circuitry (as shown in Figure 7). With this capability, the digital and analog fault simulations can be separated in order to use tools which are designed specifically for digital or analog simulation, but not necessarily for both.

Additional considerations related to the ORA design include detecting faults which result in phase shifts as well as faults which result in the superposition of noise on the analog signal. In the first case, summing the magnitudes of the sampled analog signal may only detect the fault at the beginning and end of the BIST sequence. In the latter case, the noise could average to zero such that there is no change in the resultant accumulator value from that of the fault-free circuit. However, summing the absolute value of the magnitude of the difference between the input test signal and the output response should allow detection of both of these cases. As a result, we have included a subtracter circuit in the ORA design which can be selected via BIST control signals for phase shift and noise detection. Therefore, the complete BIST session would consist of: 1) loopback of the TPG output directly to the ORA input to test the digital BIST circuitry, 2) summing the magnitudes of the analog response, and 3) summing the absolute value of the difference between the input test pattern and the analog output response. If any of the three

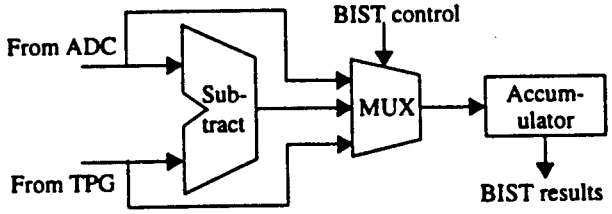

Figure 7. ORA Block Diagram

test sequences fails to produce the correct accumulator value (or a value within the acceptable range of values in the last two tests), the circuit is considered to be faulty.

We have developed a program which converts the digital output of the TPG simulation to SPICE signal statements which are then incorporated with the SPICE models for the analog circuitry under test (including the DAC and ADC) during analog simulation, verification, and fault simulation. We use the Statistical Fault Analyzer (SFA) from Rome Laboratory [8-11] to perform the analog fault simulations using the test patterns produced by the TPG. SFA performs Monte Carlo simulations of the faulty and fault-free circuits using the specified tolerances of the analog components. SFA also facilitates the determination of which faults in the analog circuit are detectable, however, we are most concerned with those detectable faults that may not be detected by the BIST approach. Therefore, we apply the output responses obtained from the SFA simulations of the fault-free analog circuit (these will be digital voltage levels since they have been produced by the ADC SPICE model) to the various ORAs (via an analysis program we developed) to determine the range of acceptable values for the BIST sequence. Similarly, we apply the digital values obtained from the faulty circuit SFA simulations to determine the range of values produced by the faulty circuit. For either of the analog BIST sequences (summing the magnitudes or summing the difference in magnitudes), if the two ranges do not overlap, the fault is considered to be detected, while the fault is considered to be undetected if the range of values of the faulty circuit falls within the range of acceptable values for the fault-free circuit. If the range of values for the faulty and fault-free circuit partially overlap, the fault is considered to be potentially detected with the probability of detection proportional to the percentage of resultant values of the faulty circuit that lie outside the range of values for the fault-free circuit.

6. Experimental Results and Summary

In the analog work thus far, we have investigated, selected, modeled, and simulated DAC and ADC designs for CMOS implementation. In addition we have obtained a number of circuits from analog testing literature and analog research projects to serve as the analog circuits under test in the SFA simulations. We have recently begun the analog fault simulation process with analysis of the ORA results and we include the following example or our preliminary results.

The single stage amplifier circuit shown in Figure 8 was simulated using the process described in the previous section using the triangular wave input test pattern. The allowable tolerances of the analog components are specified by the sigma variation next to each component value in the figure. The nine faulty circuit values are listed in the table; SFA simulations indicated that all nine faults are detectable. Eight of the nine faults were detected by the trianlgular wave in conjunction with the double-precision based ORA summing only the magnitudes of the sampled output response of the analog circuit under test (this does not include summing the absolute values of the difference in the magnitudes of the input test pattern and output response). The β-high fault was potentially

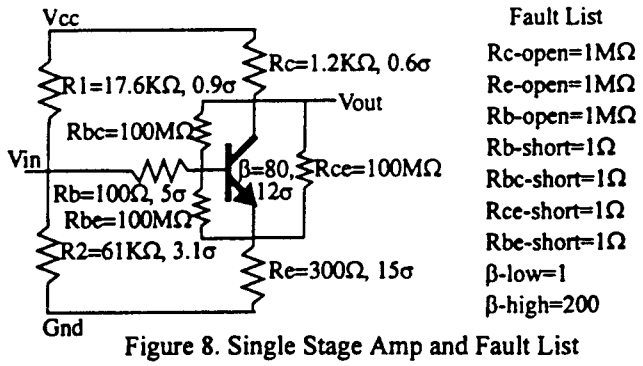

Figure 8. Single Stage Amp and Fault List

detected with a detection probability of 50%. These initial results indicate that the BIST approach presented in this paper offers considerable potential for testing analog circuits at all levels of testing from wafer through system level.

Acknowledgments

We wish to acknowledge the contributions of Chris Flynn, Paul Ratazzi, and Warren Debaney of Rome Laboratory for helpful suggestions and discussions regarding the TPG and ORA implementations as well as the future directions of this project. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either express or implied, of Rome Laboratory or the U.S. Government.

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BENCHMARK CIRCUITS FOR ANALOG AND MIXED-SIGNAL TESTING

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Abstract: This paper proposes a standard set of fault models and establishes acceptable component variations for a new set of benchmark circuits used to evaluate analog and mixed-signal testing techniques. [1]

1. INTRODUCTION

The growing need of analog electronics in communication, multimedia and information technology industries has called for the development of analog and mixed-signal integrated circuits with both analog and digital circuits on the same chip. To improve testing capabilities, the IEEE mixed-signal testing committee has been developing a set of benchmark circuits to serve as a reference for performance, comparison of results in fault modeling, testing and other related areas. This set of analog and mixed-signal benchmark circuits was presented at the 1997 IEEE International Test Conference in [1] and are referred to as the ITC'97 mixed-signal benchmark circuits. Additional information regarding these benchmark circuits, including SPICE source files, have been made available on the IEEE mixed-signal benchmark circuit home page (at *www.ee.washington.edu/mad/benchmarks/benchmarks.html*). Our experience with these benchmark circuits in [2] and [3] has shown that the fault models for these circuits, along with a standard list of faults to be simulated, and the range of acceptable component variations were not specified. In addition, other problems were encountered when using the circuits.

In this paper, we propose fault models for the ITC'97 benchmark circuits as well as a standard set of faults and establish the ranges of acceptable component variations for these circuits. Some of the ITC'97 benchmark circuits are omitted due to insufficient model information on the IEEE mixed-signal benchmark circuit home page and in [1]. The omitted benchmark circuit have been replaced and the database has been extended with other circuits from various sources. We begin with an overview of the ITC'97 mixed-signal benchmark circuits in Section 2 and a discussion of the problem encountered with their use. In Section 3 we present the proposed new set of benchmark circuits. The fault model descriptions for the components are described in Section 4. Section 5 gives overview of the simulation method used to establish the component parameter ranges. An example benchmark circuit with brief description, circuit schematic, nominal component values, frequency response of the circuit with out and with variations, set of acceptable parameter variations and soft faults is given in Section 6. Summary and conclusions are presented in Section 7.

2. ITC'97 BENCHMARK CIRCUITS

The ITC'97 benchmark circuits [1] include an operational amplifier, continuous-time state-variable filter (CT filter), a leapfrog filter, digital-to-analog converter, analog-to-digital converter, six^{th} order band-pass fully-differential filter and a charge-pumped phase lock loop. These circuits are commonly used components in analog and mixed signal circuit design and are intended to be used for comparison of different testing methodologies. However, fault model information including a list of standard faults to be simulated was not presented in [1]. Additional information (such as SPICE source files) for some of the circuits were not available on the IEEE Mixed signal benchmark circuit home page. Therefore, these circuits were discarded in our work as sufficient model information could not be found.

An other difficulty with the ITC'97 circuits is the schematics and spice files do not exactly represent each other for some circuits. For example, the operational amplifier schematic present in [1] illustrates a design with 8 MOSFETs while the Hspice netlist shows a design with 9 MOSFETs. As the operational amplifier is used in the Continuous-time sate-variable filter, we simulated both designs using the both Op Amp models and found that Hspice produced the same outputs for all low-pass, band-pass and high-pass modes. Therefore, we have chosen the model corresponding to the circuit schematic presented in [1]. In another example, there are two different component values specified for the same resistor in the Continuous-time state-variable filter in [1]. Finally, the Hspice source file for

[1] Effort sponsored by Air Force Research Laboratory, Rome Research Site, Air Force Material Command, USAF, Rome, NY, under agreement number F30602-97-1-0042. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright annotation thereon.

Leapfrog filter is modeled with 13 resistors, but circuit schematic shows only 12 resistors.

Analog components are expected to vary in their parameter values as a result of manufacturing tolerances, voltage, temperature, etc. These variations in component values will cause variation in the output response of the analog circuit to test waveforms. In turn, these variations in output response must be considered in testing to determine whether a fault has been detected or not. But none of the ITC'97 benchmark circuits have tolerances associated with their component values. Similarly, a set of benchmark circuits should have a standard set of faults and fault models so that comparison between testing techniques can be accurate. Such a standard set of fault models and fault sets for the ITC'97 benchmark circuits were not presented in [1]. Therefore, there is a need to have a new set of benchmark circuits with fault models and acceptable component variations specified.

3. Proposed New Set of Benchmark Circuits

The proposed new set of benchmark circuits consists of some of the circuits taken from ITC'97 benchmark circuits along with others from different sources like Statistical Fault Analyzer (SFA) [5][6]. These circuits are listed in Table 1 along with their source and the number of components (Rs, Cs, BJTs, and MOSFETs) and number of operational amplifiers that constitute the benchmark circuit.

Table 1: List of new benchmark circuits

Name of the circuit	Source	Number of components
Operational amplifier 1	ITC'97 [1]	11
CT filter	ITC'97 [1]	9 & 3 opamps
Operational amplifier 2	ITC'97 [1]	10
Leapfrog filter	ITC'97 [1]	17 & 6 opamps
Digital to analog conv.	ITC'97 [1]	34 & 1 opamp
Differential amplifier	SFA [5][6]	9
Comparator	SFA [5][6]	3 & 1 opamp
Single stage amplifier	SFA [5][6]	6
Elliptical amplifier	SFA [5][6]	22 & 3 opamps
Low-pass filter	Lucent	4 & 1 opamp

4. Fault Models

Fault models for analog and mixed signal circuits can be classified into two categories: catastrophic faults (sometimes called hard faults) and parametric faults (sometimes called soft faults). A catastrophic fault model is analogous to the stuck-at fault model in the digital domain in that the terminals of the component can be stuck-open or stuck-short. Parametric faults, on the other hand, are deviations of component parameters that result in performance out of acceptable limits. Parametric faults can be simulated as a variation of a component parameter which is out of specified tolerance limits. As will be discussed in Section 5, we establish acceptable component parameter variations using a normal distribution and specify the 1-σ value (expecting the acceptable variation to be up to 3-σ). Therefore we specify parametric faults at the +/- 6-σ values for high and low parametric fault values, respectively. The catastrophic fault models for individual components are described below.

Stuck-open faults are hard faults in which the component terminals are out of contact with the rest of the circuit creating a high resistance at the incident of fault in the circuit. These faults can be simulated by adding a high resistance in series (Rs=100megΩ) with the component to be faulted. A stuck-short fault, on the other hand, is a short between terminals of the component (effectively shorting out the component from the circuit). This type of fault can be emulated by connecting a small resistor in parallel (Rs=1Ω) with the component. Stuck-open and stuck-short faults can be emulated in a resistor or capacitor as illustrated in Figure 1. A MOSFET stuck-on and stuck-off fault can be emulated using this the stuck-open and stuck-short fault model as shown in Figure 1. For the fault-free case Rs=1Ω and Rp=100megΩ.

Another fault model is used for bipolar junction transistors (BJTs). The BJT can have 3 stuck-open faults (at the base, collector, and emitter terminals) 3 stuck-short faults (between base-collector, base-emitter, and collector-emitter). These stuck-open and stuck-short faults are emulated in the same manner using 3 series resistors R_b, R_c, and R_e, for the stuck-open fault (like Rs above) and 3 parallel resistors R_{bc}, R_{be} and R_{ce} (like Rp above), as shown in the Figure 1. In addition, the BJT has two soft faults for the value of β.

With this standard set of faults models we also obtain a standard set of faults. The total number of hard faults in an analog circuit is:

$$N_{HF} = 2(R+C+M)+ 6B \qquad \text{Equation (1)}$$

where R= number of resistors, C= number of capacitors, M= number of MOSFETs and B = number of BJTs in the given circuit. The number of soft faults is:

$$N_{SF} = 2(R+C)+ 2B \qquad \text{Equation (2)}$$

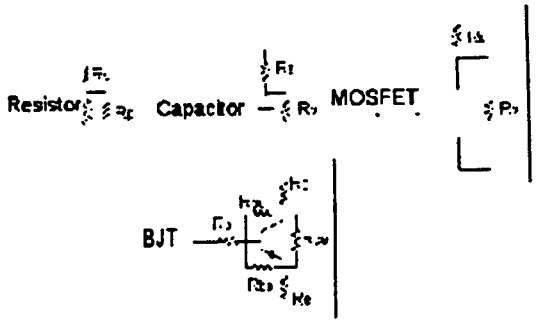

Figure 1. Hard Fault Models

5. Simulation Method

A circuit should be designed to meet the tolerance associated with the specific requirement. Due to the very nature of the manufacturing process and working environment of the designed circuit, the value of the parameters often change. These variations are acceptable as long as circuit response is within specified limits. A known range of acceptable values for a circuit component parameter is necessary to establish the fault-free behavior for a given circuit, which can then be used to detect a fault. To analyze the effects of circuit component parameter variations on the behavior of a circuit, Mote-Carlo analysis is performed.

Monte-Carlo analysis uses a random number generator to generate different kinds of functions like normal and uniform distributions. The normal distribution was chosen to generate statistical variation of component values in order to specify the amount of acceptable variation on each component using standard deviation or 1σ. This specification, in turn, assumes the component will vary up to 3σ yet the analog circuit will continue to operate within the system specification. We chose as a default system specification, a maximum deviation in the gain and phase response of the circuit to be within 10% of the gain and phase response of the circuit when using nominal component values.

In order to facilitate comparison of results like fault coverage through different testing methods for the parametric faults, we propose to use standard soft faults. The 6σ point on the either side of the nominal value is defined as a standard parametric fault or soft fault for each component, where 1σ point represents the amount of acceptable variation in Gaussian distribution. The representation of soft faults is shown in figure 3

6. Example Benchmark Circuit

In this section we illustrate the information contained in our new benchmark circuit database which can be found at www.engr.uky.edu/EE/Stroud/anabckts.html. For each benchmark circuit we include the following information:

1. Schematic diagram
2. Nominal component values
3. Frequency response (gain and phase) using nominal component values
4. Acceptable component parameter variations
5. Frequency response (gain and phase) using acceptable component variations
6. Catastrophic (hard) fault list
7. Parametric (soft) fault list
8. Hspice/SPICE netlist source file with fault models (with fault-free values) included

We will use operational amplifier 1 (Op Amp 1) from Table 1 as an example circuit to show the format of the information listed above. The schematic diagram of the CMOS two stage operational amplifier is shown in Figure 2 and the nominal component values for each component in Op Amp 1 are listed in Table 2. The frequency response of the circuit using the nominal component values is given in Figure 3 for both gain and phase. It is important to note that the operational amplifier was simulated in Hspice with fault models for its component included and that the fault-free values were used for the nominal frequency response simulation. The unity gain bandwidth and open-loop gain are 16.5MHz and 77.5 db respectively.

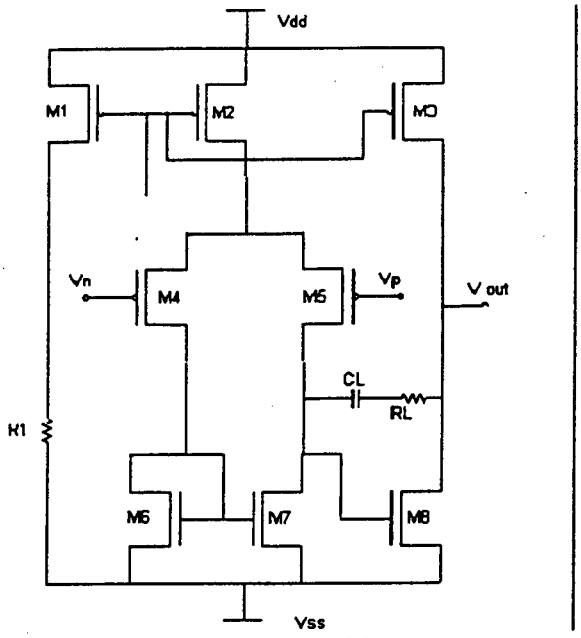

Figure 2: Schematic Diagram.

Table 2: Component table with nominal values

Component: number of each	Nominal Value
MOSFETs: 8	M1-M8
Capacitor: 1	CL=1.27pF
Resistors: 2	R1=110KΩ, RL=8.75KΩ

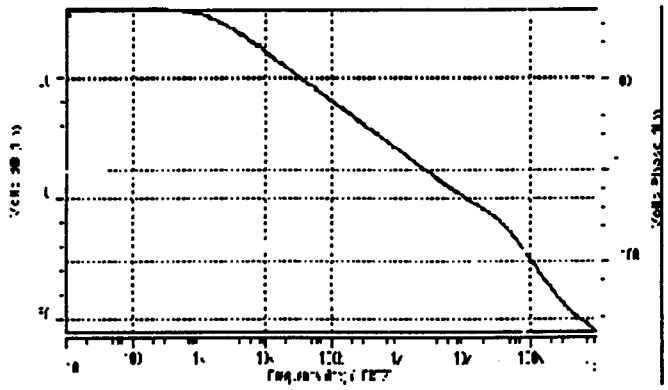

Figure 3: Frequency response with nominal components

The information presented thus far was obtained from the benchmark circuit source (with the exception of the fault models incorporated in the Hspice/SPICE netlist source file.

Having described the method for modeling the hard and soft faults for the benchmark circuit, we summarize the fault data presented in our benchmark circuit database. The set of catastrophic (or hard) faults for Op Amp 1 are summarized in Table 3. The total number of hard faults according to Equation 1 is 22 for Op Amp 1. Similarly the soft faults are summarized in Table 4 where the total number of faults given by Equation 2 is 6.

Table 3: Hard faults and number of faults

Component	Faults	No. of faults
M1-M8	Stuck-open/stuck-short	2x8=16
R1,RL	Stuck-open/stuck-short	2x2=4
CL	Stuck-open/stuck-short	1x2=2

Table 4: Soft faults component values

Component	Nominal value	-6σ	+6σ
R1	110KΩ	70.4KΩ	149.6Ω
RL	8.75KΩ	5.6KΩ	11.9KΩ
CL	1.27pF	0.3556pF	2.1844pF

The acceptable component parameter variations that were established via the Monte-Carlo analysis described in the previous section are summarized for Op Amp 1 in Table 5. Although each component variation is specified at the 1σ point in the table, we emphasize that the component can vary in value by as much as 3σ from the nominal value. With the specified component variations, the gain and phase response of the analog circuit will remain within 10% of the gain and phase response of the circuit using only nominal component values. This frequency response with component variation is shown in Figure 4 for Op Amp 1.

Table 5: Acceptable component parameter variations

Component	Nominal value	1σ point value
R1	110KΩ	6.6KΩ
RL	8.75KΩ	525Ω
CL	1.27pF	0.1524pF

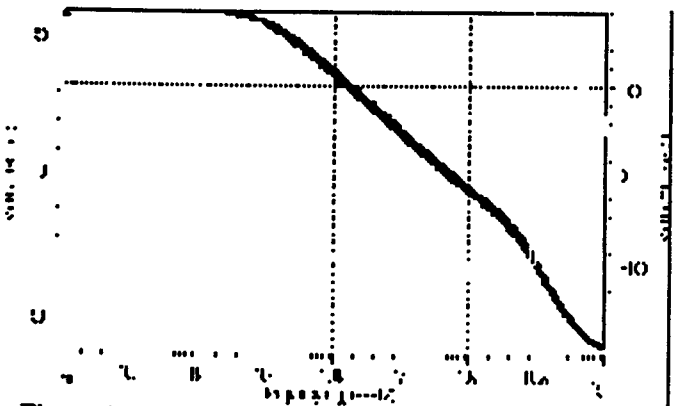

Figure 4: Frequency response with component variation

7. SUMMARY AND CONCLUSIONS

A standard set of faults and fault models for analog and mixed-signal benchmark circuits have been presented and proposed that can be applied to any analog circuit. This set of faults and fault models includes hard and soft faults for the evaluation and comparison of different analog and mixed-signal testing approaches. The set of analog and mixed-signal testing benchmark circuits originally described in [1] has modified and expanded with new benchmark circuits from other sources. Acceptable component parameter variations is established for each benchmark circuit which ensures no more than a 10% variation in the analog circuit gain and phase frequency response. A web site (www.engr.uky.edu/EE/Stroud/anabckts.html) was prepared to make this information readily available on-line to the public and to other researchers.

ACKNOWLEDGEMENTS

The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the Air Force Research Laboratory or the U.S. Government.

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A PROTOTYPE UNIT FOR BUILT-IN SELF-TEST OF ANALOG CIRCUITS

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Abstract: The design, implementation, and operation of a prototype assembly used to evaluate and demonstrate a mixed-signal based Built-In Self-Test approach for analog circuits is described. Experimental results obtained from testing benchmark circuits using the prototype assembly are presented to illustrate results that cannot be easily obtained from a simulation environment.[1]

1. INTRODUCTION

By capitalizing on well established methods employed in Built-In Self-Test (BIST) for digital systems, an effective and economic strategy for BIST of analog circuits in mixed signal systems has been proposed [1,2]. Utilization of the basic components used in digital BIST structures grants the advantage of providing the required test capability without compromising the integrity of the analog domain. This is achieved by restricting the test circuitry to the digital domain and relying on the digital-to-analog and analog-to-digital converters of the mixed-signal system to provide a non-intrusive interface to the analog domain. Analog BIST, however, does require application of unique digital Test Pattern Generator (TPG) and Output Response Analyzer (ORA) functions that differ in design and capabilities from the conventional TPG and ORA functions in digital BIST. These specific designs and capabilities have been developed and studied in [1] and are applicable to a wide range of analog circuitry residing in mixed signal VLSI devices and systems [2,3].

Traditionally, logic simulations of systems, including BIST features and capabilities, have been accurate and sufficient for the determination of correct design, fault coverage, and good circuit signatures in the digital world. Analog circuits, on the other hand, have often required prototype units in order to collect information that cannot be easily obtained from current simulation environments. This is particularly true when developing a BIST approach for analog circuits. Parameter variations with local temperature and voltage changes affect the results of the BIST sequence and are difficult to simulate. A prototype unit facilitates the collection of such data, demonstrates the feasibility of the BIST approach, determines the fault detection capability, and physically corroborates simulation results. This paper describes the operation and implementation of a prototype unit that is specifically designed to evaluate the mixed-signal based BIST approach for analog circuits described in [1,2]. An overview of the mixed-signal based BIST architecture is given in Section 2 with particular emphasis on those characteristics of the architecture that warranted the development of the prototype unit. A detailed description of the architecture and operation of the prototype unit, including both hardware and software, is given in Section 3. A sample of the data collected with the working prototype unit is presented in Section 4 and the paper is summarized in Section 5.

2. OVERVIEW OF ANALOG BIST ARCHITECTURE

A block diagram of the BIST architecture is given in Figure 1. The digital TPG supplies various test waveforms, specifically tailored for use in analog BIST, to the Digital-to-Analog Converter (DAC). These waveforms, when converted to their analog counterparts, have been shown to sufficiently detect faults in analog circuits. Together, the digital TPG and DAC produce ramp, triangular waves, noise type waves, and frequency sweep functions [1]. These test waveforms from the digital TPG are inserted into the outgoing digital signal path via the multiplexer at the input to the DAC which, in turn, converts the digital patterns to the analog test waveforms for testing the analog circuitry. Analog multiplexers are strategically located in the analog circuitry. During test mode, the analog multiplexers configure the analog circuit for testing and return the output to the ADC for conversion back into the digital domain. The ORA is a double precision accumulator. It operates in two modes: 1) to sum the magnitudes of the analog circuit responses to the test waveforms or 2) to sum the absolute values of the difference in magnitude between the outgoing digital test waveform and the incoming analog circuit test response. Mode 2 enables detection of faults that result from excessive noise or an inappropriate phase shift in an

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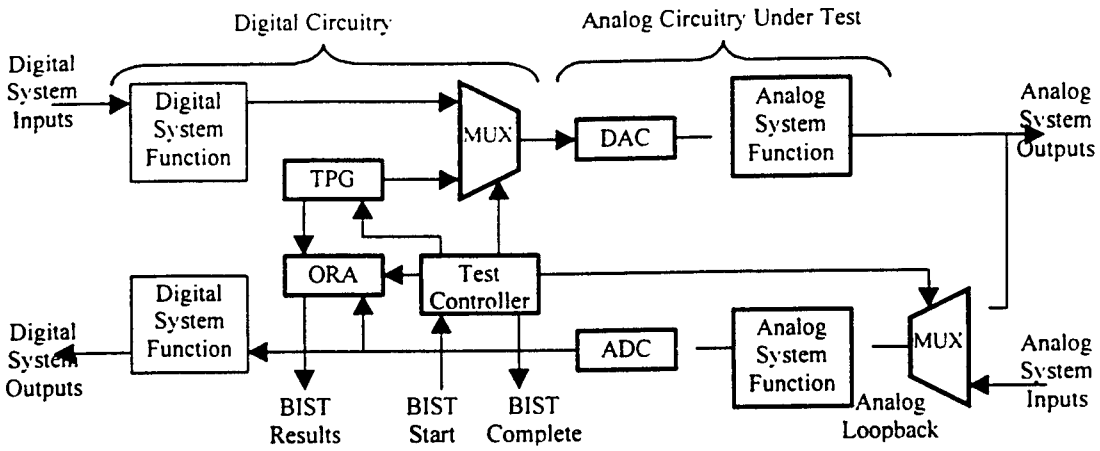

Figure 1. Analog BIST Architecture in a Mixed-Signal System

otherwise good test response [4]. Finally, a test controller is incorporated to coordinate the initialization sequence for the analog circuitry under test and the length of the test sequence for each waveform to ensure reproducible BIST results during system operation.

The accumulator-based ORA portion of the BIST architecture is an essential component that differentiates this approach from traditional ORA circuits used in digital BIST systems. This ORA approach can accommodate for typical variations in the test response such as temperature and voltage fluctuations as well as quantization elements introduced by the DAC and ADC. Such variations can cause the resulting BIST signature to vary from one execution of the BIST sequence to the next. As a result, an exact BIST signature cannot be obtained for a "good" circuit and, in fact, the resulting BIST signature may vary from one execution of the BIST sequence to the next. Traditional digital BIST ORAs, such as signature analysis registers, provide no mechanism to determine the degree of variation in the analog test response. The summing property of the accumulator, on the other hand, facilitates the determination of a range of "good" circuit signatures that can account for acceptable variations in the analog test response. Using this method, a fault is then detected when a BIST signature lies outside the range of good circuit BIST signatures.

An acceptable range of good circuit signatures can be determined from an analog simulation environment (such as SPICE or HSPICE) using Monte Carlo analysis with appropriate variations in component and environmental parameters. Conservative simulation with larger parameter variation lead to a wide range of good circuit signatures, making fault detection difficult. Likewise, optimistic simulations with small parameter variations can generate a range of circuit signatures that incorrectly identify a fault in a good circuit. For large analog circuits, these simulations are time consuming; particularly with the large number of test waveforms produced by the TPG and the length of these waveforms. Finally, it is difficult to simulate shifts in active device junction temperatures and/or changes in power dissipation that result from the signal processing performed by the analog circuitry. In many of these cases, a prototype unit facilitates a more efficient method for collecting the data of good and faulty circuits. The prototype unit demonstrates the range of BIST signatures that result from typical parameter variation during normal analog system operation. It also demonstrates the feasibility of this BIST approach and its fault detection capabilities.

3. Description of Prototype Unit

The prototype system utilizes TPG and ORA integrated circuits developed by students in an introductory VLSI design and testing class at the University of Kentucky. These application specific integrated circuits are combined with off-the-shelf DAC and ADC and other basic digital components to provide the complete analog BIST prototype assembly. A control and observation interface has been included that allows two way communication between the prototype and a PC via a parallel port connection as illustrated in Figure 2. The prototype unit and the test sequences being applied to analog circuits under test are controlled by the user through the PC software by writing to one of three control registers whose bit maps are given in Table 1. These registers are written by applying the data to the data bus (D7-0) of the PC parallel port, and then activating the write enable associated with the target register.

The software required for operating the prototype unit via the PC parallel (printer) port consists of a number of subroutines that configure the ORA in its basic modes of operation: reset, digital test, magnitude summing test, and difference summing test. The software can force the TPG to generate basic waveforms: count-up, count-down, count up/down, LFSR, frequency sweep, and bit reversal for each wave form type. These subroutines configure the three registers with appropriate data sequences for the desired BIST sequence. Once a given BIST sequence is complete, the 16-bit ORA accumulator output is read 4 bits at a time to

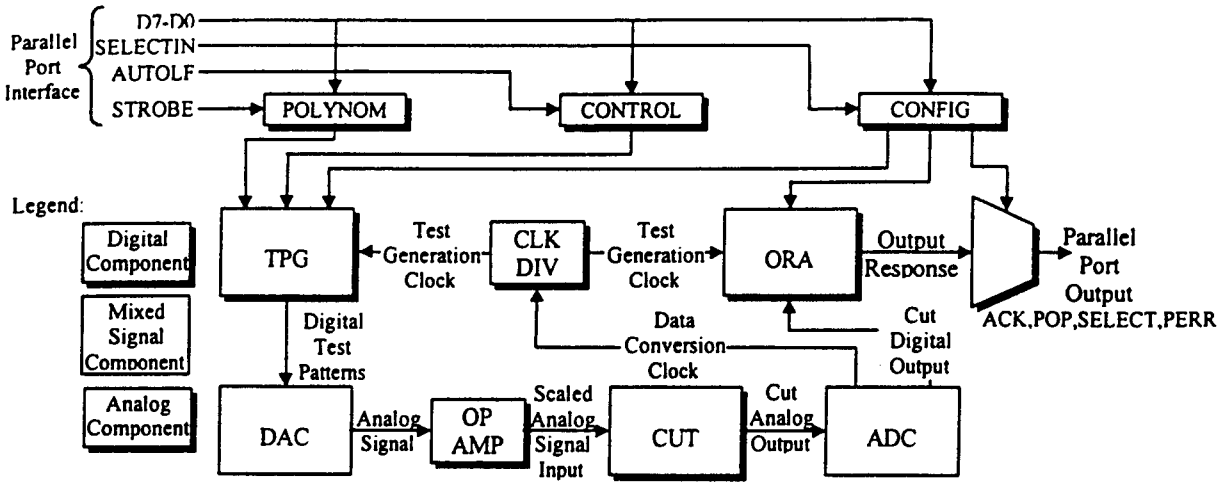

Figure 2. Top Level Block Diagram

obtain the resultant BIST signature. A high level routine can, for each of the three ORA modes, execute the complete set of 10 test waveforms and retrieve the resultant BIST signatures.

Table 1. Register Bit Maps

Register	Polynomial	Control	Configuration
Enable	Strobe	AutoLF	SelectIN
Bit 7 (msb)	P7	-	-
Bit 6	P6	Freq sweep	MSEL0
Bit 5	P5	Count down	MSEL1
Bit 4	P4	Bit reversal	M0
Bit 3	P3	Count up	M1
Bit 2	P2	Clear TPG	PSR0
Bit 1	P1	Count/LFSR	PSR1
Bit 0 (lsb)	P0	Enable test	PSR2

The contents of the Polynomial (POLY) register define the coefficients (P7-0) of the characteristic polynomial used by the Linear Feedback Shift Register (LFSR) to generate pseudo-random noise patterns [1]. The configuration (CONFIG) register is used to configure the frequency sweep function, the modes of operation of the ORA, and which nibble of the 16-bit accumulator is read back by the PC. The value of PSR0-2 determines the rate at which the frequency sweep generator sweeps through the frequencies [1], M0-1 configures the mode of the ORA (00=clear ORA, 01=difference summing test, 10=magnitude summing test, and 11=digital test), and MSEL0-1 selects which nibble to read from the ORA output. The Control CTRL) register dictates which basic waveform is generated by the TPG. With this arrangement, analog test circuits can be subjected to the complete battery of test patterns available in the BIST circuitry.

The analog circuits under test that were implemented on the prototype unit include three of the benchmark circuits described in [3]. The first circuit is the DAC benchmark circuit in conjunction with an ADC that uses the comparator benchmark circuit with an adaptive counter and a second DAC. The output of the DAC can optionally be fed through the single stage Common-Emitter Amplifier benchmark circuit or the low pass filter benchmark circuit. The actual prototype unit, as implemented, is shown in Figure 3.

4. Data Collection Results

A consistent digital BIST signature of 0xfd00 was obtained for waveforms sharing a common cyclic pattern. The count-up, count-down, count-up/down, LFSR with primitive polynomial, and bit reversals (for each of those waveforms) cycle from 0 to 255 in their respective ways. The frequency sweep and its bit reversal counterpart were the two exceptions and did not share this digital BIST signature with the others. This consistent BIST result obtained for the cyclic waveforms verified that the digital portion of the prototype was fully functional.

When the complete battery of test waveforms was repeatedly applied to the analog benchmark circuits, the range of good circuit signatures was obtained for each benchmark circuit. These are presented in Table 2. It should be noted that these acceptable circuit signature ranges were generated from tests that included the complete mixed-signal system (DAC, ADC, digital, and analog test circuitry). As a result, these ranges accounted for variations caused by quantization error of the DAC and ADC, system noise, and instantaneous temperature and voltage changes in the complete analog system under test. These are factors that cannot be easily or accurately simulated in an analog simulation environment. In addition to this, the results of Table 2 corroborate the results of simulations in [3] which suggested that single precision and residue accumulators (8-bits each in this case) are insufficient to contain the complete range of good circuit signatures that are generated for actual analog circuits under test.

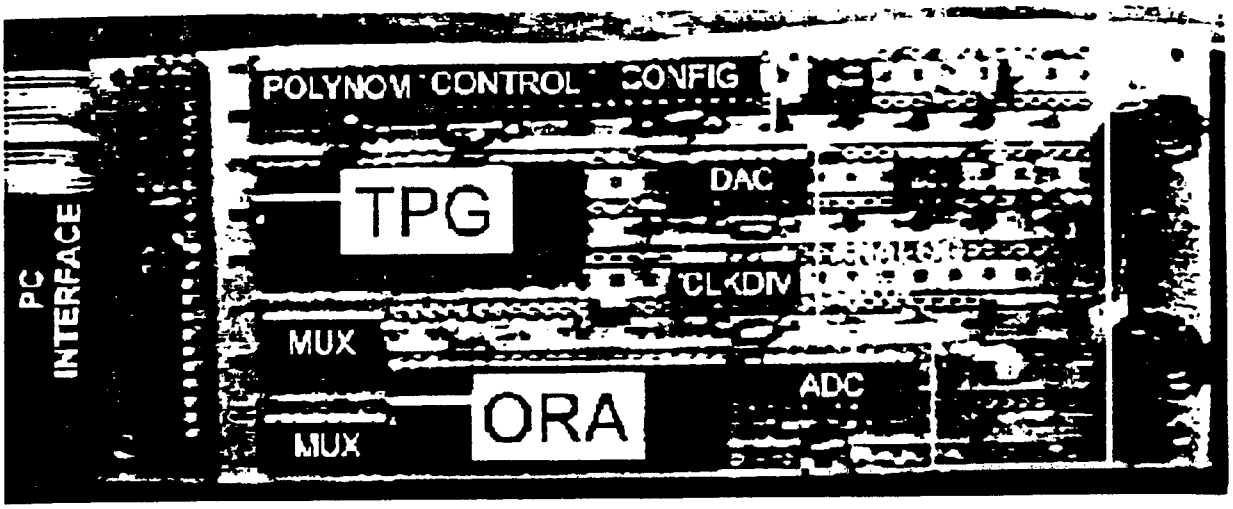

Figure 3. Photograph of Actual Prototype Unit

Table 2. BIST Signature Range for Benchmark Circuits

TPG (ORA) mode	DAC-ADC	C-E Amp	Low-pass
Cnt-up (mag)	015C	0153	006D
Cnt-dwn (mag)	00F0	016E	0035
Cnt-u&d (mag)	0097	0098	0066
LFSR (mag)	0239	060D	011B
Freq-sweep (mag)	174D	0B3C	0315
Cnt-up (diff)	014D	0197	008D
Cnt-dwn (diff)	00EC	00E4	002D
Cnt-u&d (diff)	0058	02E0	008D
LFSR (diff)	02C7	0202	00FF
Freq-sweep (diff)	043A	0218	0092

In general, the frequency sweep test pattern produced the largest range of good circuit signature values for the magnitude test due to longer test lengths compared to the other four test waveforms. Generally there was a smaller range of good circuit signatures for the various waveforms when the ORA was used to sum the absolute value of the difference in magnitudes between the input test waveform and output response (diff mode). Additionally, the range of good circuit signatures are smaller for filter (low-pass filter benchmark circuit [3]) when compared to amplifier functions (OpAmp with the DAC-ADC and Common-Emitter Amplifier benchmark circuit [3]). This also corroborates the simulation results obtained in [2].

Faults were emulated in the prototype in several ways. Components were shorted by placing a jumper wire between two terminals. Resistive topological shorts were obtained by placing a resistor between two nodes. Stuck-open faults were emulated by disconnecting a component's terminal on the board. Finally, voltage source values and temperature of the unit could be varied for environmental faults. Thus far, we have primarily worked with shorting the components and changing the values of resistors in the analog circuits by placing another resistor in parallel with the target resistor.

5. CONCLUSIONS

Although the construction of analog and mixed-signal prototype units are more time consuming than digital circuits, they are usually worth while due to the valuable information they provide about the target system. In this paper we have given an overview of a prototype unit that was constructed to verify a BIST approach for testing analog circuits in mixed-signal systems. Not only did the data collected from operation of the prototype unit corroborate the results of simulations, but it also provided information that was not obvious or easily obtained through traditional analog simulation tools. Finally, the prototype demonstrated the feasibility, utility, and practicality of the mixed-signal BIST approach for analog circuits.

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BUILT-IN SELF-TEST FOR ANALOG CIRCUITS IN MIXED-SIGNAL SYSTEMS

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Abstract: A Built-In Self-Test (BIST) approach is presented which is designed to test the analog portion of mixed-signal systems. The BIST approach is evaluated using fault simulation with analog benchmark circuits and is found to consistently provide high fault coverage of all stuck-open and stuck-short faults in the circuit under test.[1]

1. INTRODUCTION

Mixed signal systems provide a good environment for the development of Built-In Self-Test (BIST) approaches for analog circuits by allowing the experience and expertise of BIST development in the digital domain to be used as a platform for the investigation of analog BIST techniques. Specifically, the basic components of most BIST structures can be incorporated in the digital portion of the mixed-signal design without adverse effects on the analog circuit performance. These digital components include the test pattern generator (TPG) and output response analyzer (ORA) functions as well as the necessary test controller function to initialize and control the BIST sequence and provide system level access to the BIST circuitry [1]-[3].

It is important to realize that there are aspects of analog BIST which prevent the straight forward application of conventional digital TPG and ORA functions. Traditional signature analysis is unsuitable for application to analog BIST since the good circuit signature is based on the assumption that an exact output response sequence is obtained for every fault-free execution of the BIST sequence [2][3]. In a mixed-signal system, the sampling noise in the Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) as well as processing (i.e., tolerances) and environmental (i.e., temperature and voltage) variations in the analog circuitry will prevent an exact output response sequence from one execution of the BIST sequence to the next. As a result, reproducible BIST signatures cannot be obtained for the fault-free circuit. Similarly, digital pseudorandom TPGs based on the Linear Feedback Shift Register (LFSR) will produce an analog signal that is similar to noise after passing through a DAC. However, ramp input signals have been used in analog testing and have been found to provide good fault detection results and, in some cases, better results than sinusoid test signals [4][5]. It has been observed that the detectability of faults with respect to the input test signal can vary with the type of analog circuit under test [5].

We have developed a Built-In Self-Test (BIST) approach for analog circuitry, which resides in mixed signal VLSI devices and systems [6][7]. In this paper, we investigate the fault detection capabilities of the BIST approach for a number of benchmark circuits used for evaluating analog testing techniques. We begin with an overview of the architecture and operation of the mixed-signal based BIST approach in Section 2. In Section 3, we describe the fault simulation environment used to evaluate the BIST approach. The results of fault simulations using the 1997 IEEE International Test Conference (ITC'97) mixed-signal and analog benchmark circuits[8], as well as additional benchmark circuits [9], are presented in Section 4, and the paper is summarized in Section 5.

2. OVERVIEW OF BIST ARCHITECTURE

The BIST architecture is shown in Figure 1 with the digital BIST circuitry that has been added to the mixed signal circuitry shown in bold and the analog circuitry under test shown in shades of grey. The normal mixed-signal system components include the digital and analog system functions as well as the DACs and ADCs that are required to convert the digital signals to analog waveforms and vice versa. The digital BIST circuitry added to the mixed-signal system includes the digital TPG and ORA functions as well as a digital test controller. An additional multiplexer (MUX) is required for the insertion of the digital test patterns into, and isolation of unknown system data from, the data stream at the input of the DAC. The only BIST circuitry added to the analog domain is the loopback capabilities (analog multiplexers) needed to facilitate the return path for the test signals to the ORA. Since the target circuitry under test is

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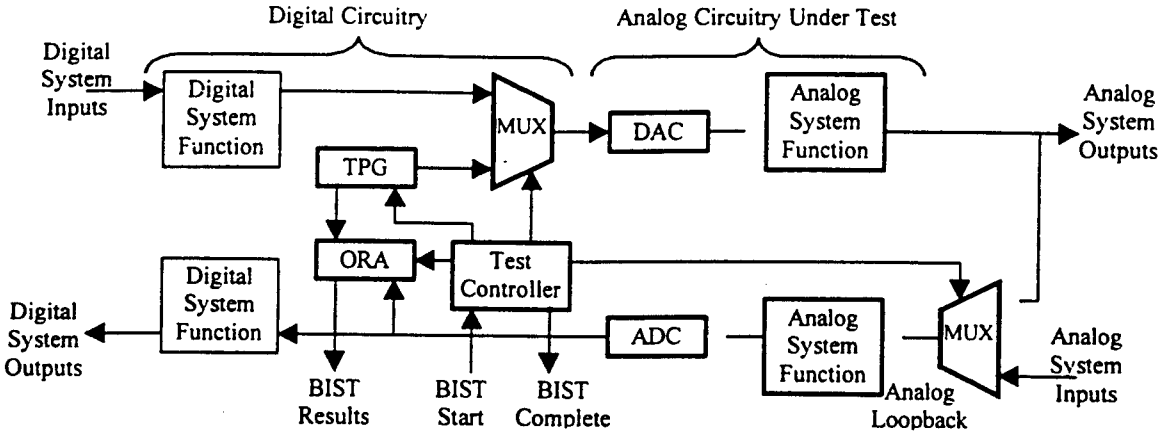

Figure 1: BIST Architecture for Mixed Signal Systems

the analog system circuits, including the DACs and ADCs, we incorporate the digital TPG and its associated MUX immediately prior to the digital inputs of the DAC. Similarly, we incorporate the digital ORA at the output of the ADC.

The TPG consists of an up/down counter, a Linear Feedback Shift Register (LFSR), and various multiplexers and registers to produce a wide variety of analog test waveforms [6][7]. These waveforms include the following: count-up, count-down, count-up-down, pseudo-random patterns, square wave frequency sweep with increasing amplitude and decreasing period, square wave frequency sweep with constant amplitude and decreasing period, and the bit reversal of each of those waveforms. The counting waveforms (up, down, and up-down) produce saw-tooth and triangular waveforms when converted to analog signals while the LFSR and the bit reversals of the counting waveforms produce noise-like waveforms.

The ORA is a double precision accumulator that is capable of summing the output response of the analog circuit in one of two modes [6][7]. In one mode the magnitude of the analog circuit output response is summed in the ORA. In the second mode, the ORA sums the absolute value of the difference between the analog test waveform (output from the TPG) and the analog circuit output response (output from the ADC). This second accumulation mode is useful in detecting faults which cause noise or phase shift in an otherwise good analog circuit response.

During system-level testing, the BIST circuitry must be capable of proper initialization of the analog circuitry under test, isolation of system data inputs, and reproducible results from one execution of the BIST sequence to the next in the same manner as is required in digital systems [3]. The length of the initialization sequence must be sufficient to clear the effects of previous system signals in the analog circuitry. Faults can be effectively isolated to a given section of analog circuitry by executing the BIST sequence with various configurations of analog loopbacks.

3. Fault Simulation Environment

The principal fault simulation tools used for this analysis include SPICE and the Statistical Fault Analyzer (SFA) [10][11]. SFA was used to perform the initial analog fault simulations using the test patterns produced by the TPG. SFA performs Monte Carlo simulations via SPICE of the faulty and fault-free circuits using the specified tolerances of the analog components. The Monte Carlo simulations account for specified component variation in the fault-free components. SFA is a single stuck-at analog fault simulator where the fault list is simulated one component at a time with the faulty component value specified in the fault list and fixed during that faulty circuit simulation. SFA also facilitates the determination of which faults in the analog circuit are undetectable.

For each Monte Carlo simulation with one of the TPG waveforms, we apply the output responses obtained from the SPICE simulation for the fault-free analog circuit to the ORA to determine the resultant signature (the final value obtained in the double-precision accumulator). By considering all of the resultant signatures we establish the range of acceptable values (from the maximum and minimum signature values) for the BIST sequence applied to the fault-free circuit. This procedure is performed for each test waveform for both of the analog BIST ORA modes of operation (summing the magnitudes and summing the absolute value difference in magnitudes) to determine the acceptable range of fault-free circuit signatures. These signature ranges for each test waveform in both test phases are then used to determine the detection of faulty circuits.

In the same manner as the fault-free circuit, the various test waveforms are applied to the faulty circuit during multiple SFA simulations in SPICE. The digital values obtained from each faulty circuit simulations are applied to the ORA in each of its two summing modes of operation. If the resultant signature for the faulty circuit lies outside the acceptable range of signatures for the fault-free circuit for that test waveform, the fault is considered to be detected.

The fault is considered to be undetected if the resultant signature of the faulty circuit falls within the range of acceptable signatures for the fault-free circuit. Since we perform multiple Monte Carlo simulations in SFA where the fault-free components are allowed to vary within the specified tolerances, we must consider the complete set of simulations for the determination of fault detection. If all signatures for a given fault are outside the good circuit range, the fault is always detected. If none of the signatures fall outside the good circuit range, the fault is never detected. But, if some of the signatures fall outside and some fall inside the good circuit range, we consider the fault to be potentially detected with the probability of detection proportional to the percentage of faulty circuit signatures that lie outside the acceptable range of signatures for the fault-free circuit.

4. Results with Analog Benchmark Circuits

The ITC'97 mixed-signal/analog benchmark circuits consist of a set of eight circuits used to evaluate analog testing techniques [8]. Problems have been experienced when using these benchmark circuits, the most serious of which is that there are no tolerances specified for components in these circuits and there are standard sets of fault models specified for the circuits. As a result, we have established a set of ten benchmark circuits with specified component variations and standardize fault models [9]. At present, we have performed fault simulations for nine of these circuits for the BIST approach described in this paper. A summary of the discrete components (Resistors, Capacitors, and Other Components) along with the total number of faults and the number of faults we have simulated in each circuit is given in the first section of Table 1.

To illustrate the importance of including component parameter variations in the analog benchmark circuits, we ran the fault simulations without component variations. Overall, in every circuit, 100% of all of the faults simulated were completely detected as shown in the second portion of Table 1 (denoted 'no-var'). At this point, only external component faults have been simulated in some of the large circuits, such as the continuous time filter, the leap frog filter and the elliptical filter as seen in Table 1. When the specified component variations are included in the fault simulations, we find that some faults are potentially detected and, as a result, the fault coverage (FC) is reduced for some circuits. Therefore, for an accurate analysis of a given analog testing approach, it is important that component parameter variation be considered and included.

We found that fault detection is a function of the clock frequency of the BIST system. To illustrate this, we begin with the fault simulation results for Op Amp 1. Op Amp 1 had an overall fault coverage of 100% with no parameter variation. The faults considered in Op Amp 1 included eight transistor stuck-off (simulated by 10MΩ resistor in series with either the drain or the source) and stuck-on (simulated as 1Ω across the source and drain). The only other components are 2 resistors and 1 capacitor with open and short faults for each. Similarly, the fault simulation results for Op Amp 2, the Comparator, the Single Stage Amplifier, and the Differential Pair Circuit indicated every fault could be detected for 100% fault coverage. The components included in these circuits can be seen in Table 1. The fault coverage results for these circuits were identical at all system clock frequencies simulated from 100Hz through 1GHz, in intervals of powers of ten. For Op Amp 1, though, fault coverage increases from 90% at a clock frequency of 100Hz to 100% at clock frequencies of 100KHz and beyond.

The filter circuits, including the Continuous Time Filter, the Leap Frog Filter, the Low-Pass Filter, and the Elliptical Filter, also yielded an overall fault coverage of 100%. Each filter circuit uses Op Amps as the main components. It should be noted that, in general, the detection of faults in these type circuits was much more sensitive to clock frequency, especially in the Continuous Time Filter. Thus the use of the frequency sweep waveforms was much more efficient in detecting faults than other waveforms used. For example, the only waveform to detect all the faults included in the Continuous Time Filter was the frequency sweep waveform with constant amplitude and decreasing period at a clock frequency of 100MHz. Figure 2 shows the sensitivity of the Continuous Time Filter to the clock frequency. Although the frequency of the clock driving the TPG and ORA in the system effected the fault coverage of the filter circuits, the parameter that controls the amount the amplitude increases and the period decreases each clock cycle of the frequency sweep waveforms did not have any such effects. The other filter circuits, with no component variation, were less sensitive to frequency than the Continuous Time Filter, but exhibited similar properties.

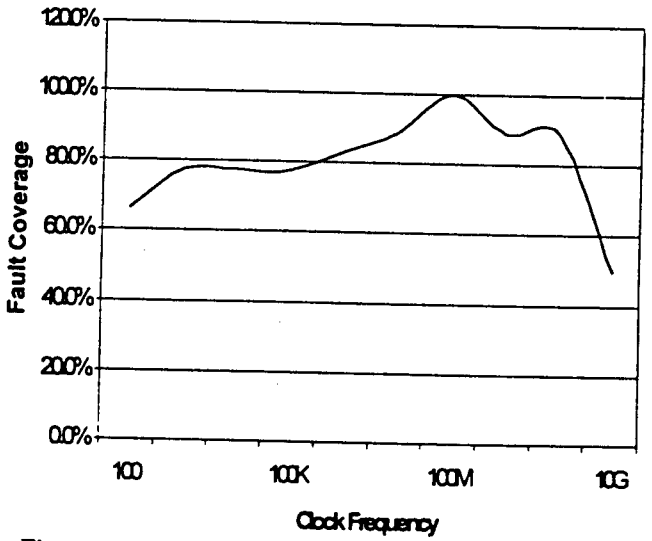

Figure 2: Fault Coverage of Continuous Time Filter

Table 1: Summary of Benchmark Circuits and Fault Coverage

Benchmark Ckt	Rs	Cs	Other Components	Total Faults	Faults Simulated	Faults Detected	FC no-var	Faults Detected	Potentially Detected	FC with var
ITC'97 Circuits										
OpAmp 1	2	1	8 N/PMOS	22	22	22	100%	21	1	98.6%
CT Filter	7	2	3 opamp1s	84	18	18	100%	14	4	97.8%
OpAmp 2	0	1	9 N/PMOS	20	20	20	100%	20	0	100%
Leap Frog Filter	13	4	6 opamp2s	154	34	34	100%	32	2	98.8%
Other Circuits										
Single Stage Amp	4	0	1 BJT	18	18	18	100%	18	0	100%
Comparator	3	0	1 opamp2	26	26	26	100%	24	2	95.4%
Low-Pass Filter	3	1	1 opamp1	30	30	30	100%	30	0	100%
Differential Pair	5	0	4 BJTs	42	32	32	100%	23	9	92.0%
Elliptical Filter	15	7	3 opamp1s	104	22	22	100%	22	0	100%

5. SUMMARY AND CONCLUSIONS

We have presented the results of the evaluation of a BIST architecture for incorporation in mixed-signal based ASICs with the primary test target being the analog portion of the mixed-signal ASIC. One advantage of this approach is that it does not require modification of the analog circuitry other than the insertion of analog loopback functions for improved fault isolation and diagnostic resolution. Based on fault simulations of analog benchmarks, the approach has been shown to be effective for all faults in the benchmark circuits. As a result of the variety of test waveforms produced, the approach appears to be applicable to analog circuits in general and not restricted to specific applications or classes of analog circuits.

The significant findings of this investigation include the need for component parameter variations (tolerances) specified for analog benchmark circuits to accurately evaluate analog testing techniques. Another finding includes the fact that the clock frequency to the digital BIST circuitry (TPG and ORA) has an impact on the fault detection capability of this BIST approach for some circuits (filter functions in particular). We are currently looking for design guidelines to assist designers in determining the best clock frequency to choose for high fault coverage in their mixed-signal system.

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