REPORT DOCUMENTATION PAGE

Form Approved
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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT DATE	3. DATES COVERED *(From - To)*
31-10-99	Navy SBIR Program Phase I Final Report	01-05-99 to 31-10-99

4. TITLE AND SUBTITLE

Very High-Performance Advanced Filter Bank Analog-to-Digital Converter (AFB ADC) Project

5a. CONTRACT NUMBER
N00014-99-M-0166

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

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5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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8. PERFORMING ORGANIZATION REPORT NUMBER

Final Technical Report: 31 October 1999

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

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10. SPONSOR/MONITOR'S ACRONYM(S)

ONR

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT

Approved for public release; SBIR report, distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Report developed under SBIR contract for topic BMDO99-001 Directed Energy Concepts and Components. See attached abstract.

19991029 056

15. SUBJECT TERMS

High-speed, high-resolution, analog-to-digital conversion, radar, RF communications, COTS A/D conversion, ADC

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
None	None	None	UU	35	19b. TELEPONE NUMBER *(Include area code)*

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI-Std Z39-18

REPORT DOCUMENTATION PAGE

14. ABSTRACT

Report developed under SBIR contract for topic BMDO99-001 Directed Energy Concepts and Components. This Phase I project demonstrated a breakthrough approach to very high-speed, high-resolution analog-to-digital conversion which improves the speed of conversion by four to six times the state-of-the-art by using a parallel array of individual commercial off-the-shelf converters. The significant performance improvements afforded by the Advanced Filter Bank Analog-to-Digital Converter (AFB ADC) architecture were verified in Phase I by successfully building and testing a pre-prototype breadboard implementation of the front-end electronics of a 12-bit AFB ADC system with 260 MHz sample rate, spurious free dynamic range of greater than 70 dB, and analog sampling bandwidth of 130 MHz. Test results confirm that the architecture works because the signal processing significantly reduces the sensitivity to analog mismatches (e.g., phase distortion, clock skew, temperature drift) which prohibit existing parallel conversion methods (e.g., Time-Interleaving) from achieving high resolution. The AFB ADC architecture will always exceed the state-of-the-art because it can easily be upgraded as new, more powerful ADC products become available. By eliminating racks of analog electronics, the high-performance AFB ADC can significantly reduce the size, power, and cost of radar systems and RF receivers by performing more of the processing digitally in reconfigurable software.

Very High-Performance Advanced Filter Bank Analog-to-Digital Converter (*AFB ADC*) Project

SBIR Phase I Project

Contract N00014-99-M-0166

Item No. 0001 AD

Final Technical Report: 31 October 1999

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Table of Contents

1. Introduction

This report was developed under an SBIR contract for topic BMDO-001 Directed Energy Concepts and Components. This Phase I project demonstrated a breakthrough approach to very high-speed, high-resolution analog-to-digital conversion which improves the speed of conversion by four to six times the state-of-the-art by using a parallel array of individual commercial off-the-shelf converters. The significant performance improvements afforded by the Advanced Filter Bank Analog-to-Digital Converter (***AFB ADC***) architecture were verified in Phase I by successfully performing the following: demonstrating an ***AFB ADC*** system design methodology, including testing and selecting suitable commercial off-the-shelf ADCs for inclusion in the architecture, analyzing test results to resolve trade-offs in the design of the signal splitter circuitry, and using computationally-efficient calibration algorithms to optimize the digital signal processing; and building and testing a pre-prototype breadboard implementation of the front-end electronics of a 12-bit ***AFB ADC*** system with 260 MHz sample rate, spurious free dynamic range of greater than 70 dB, and analog sampling bandwidth of 130 MHz. Test results confirm that the architecture works because the signal processing significantly reduces the sensitivity to analog mismatches (e.g., phase distortion, clock skew, temperature drift) which prohibit existing parallel conversion methods (e.g., Time-Interleaving) from achieving high resolution.

Based on the positive results of the Phase I project, it is expected that by using commercial off-the-shelf part, the ***AFB ADC*** architecture can provide 14-bit resolution, 400 MHz sample rate, and intermediate frequency (IF) sampling up to 300 MHz, in a compact, low-power package for use in the next generation of high-performance radar systems and RF receivers. The ***AFB ADC*** architecture will always exceed the state-of-the-art because it can easily be upgraded as new, more powerful ADC products become available. The theory was developed as a Ph.D. dissertation at the Massachusetts Institute of Technology. By eliminating racks of analog electronics, the high-performance ***AFB ADC*** can significantly reduce the size, power, and cost of radar systems and RF receivers by performing more of the processing digitally in reconfigurable software.

In Section 2. Background, the ***AFB ADC*** architecture is described. In Section 3. Overview of AFB ADC System Design, a description of the methodology used to design the architecture is presented. In Section 4. Channel ADC Selection, this first step in the design of the architecture is detailed, including specific results for testing commercial off-the-shelf ADCs for inclusion in the pre-prototype hardware example system. In Section 5. AFB ADC Pre-Prototype Hardware, the procedure for making design decisions for the hardware example system is described. In Section 6. AFB ADC System Calibration, the procedure for optimizing the digital signal processing in the architecture is described. In Section 7. 12-bit, 260 MHz AFB ADC Hardware Testing Results, a full battery of test measurements to verify the performance of the example system is presented. In Section 8. Conclusions, the Phase I project is summarized and directions for the Phase II project are discussed.

2. Background

AFB ADC Overcomes the Critical A/D Conversion Bottleneck

High-speed, high-resolution analog-to-digital (A/D) conversion is a critical technology in many modern electronic systems, such as radar systems and digital receivers for wireless communications. In general, high-speed, high-resolution ADCs enable wide bands of analog data to be converted to digital form to be processed more accurately and efficiently than is possible in analog form. Systems can be updated as requirements change and new standards arise by simply updating software to change the digital signal processing. A high-performance ADC would significantly reduce the cost, size, and power consumption of systems by eliminating much of the analog circuitry while improving versatility and performance.

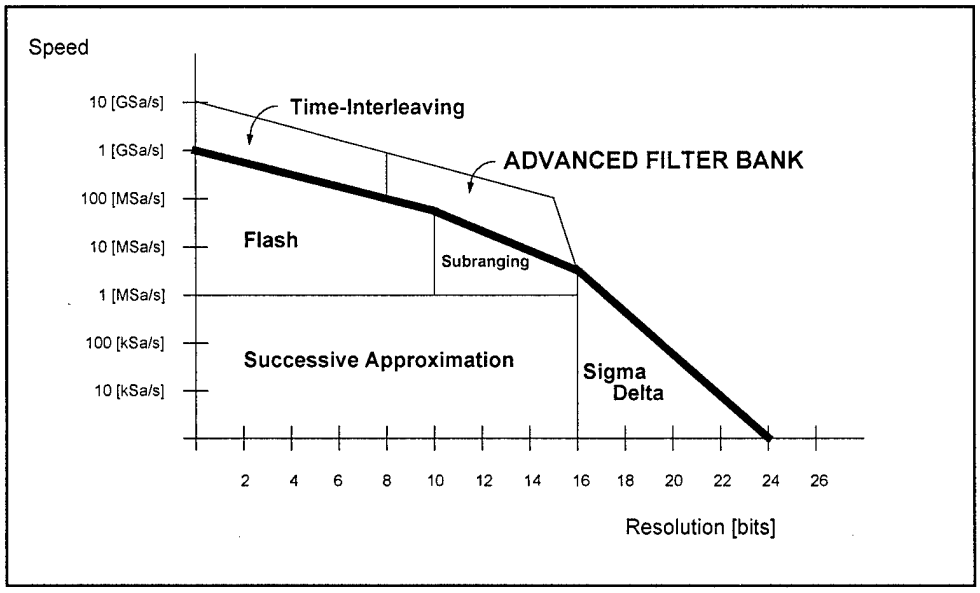

Figure 2-1. Speed versus resolution for analog-to-digital converter architectures. The thick line indicates the state-of-the-art in single-chip ADCs.

ADC performance is typically quantified by two parameters, speed (in samples per second) and resolution (in bits). Designers face the challenge of trading off the resolution of the conversion with its speed. Figure 2-1 illustrates the trade-off between speed and resolution of the most popular single-chip ADC architectures currently available. The thick line in Figure 2-1 indicates the state-of-the-art in single-chip ADCs.

Parallel Processing to Achieve High-Speed, High-Resolution Performance

The ***AFB ADC*** employs Decomposition splitters, D_k, to divide the wideband analog input signal into M channel signals. The channel signals are sampled at $1/M$ the effective sample rate of the system and converted to digital signals with n-bit ADCs. The digitized channel signals are upsampled by M and reconstructed via the digital Recombination Filters, $R_k(z)$. Note that

polyphase structures can be used to filter the signals at the lowest possible rate. The effective sample rate of the system is M times that of the channel ADCs in the array, and the resolution is n bits, the same as that of the channel ADCs in the array. The ***AFB ADC*** architecture is illustrated in Figure 2-2. The ***AFB ADC*** is well-suited for very high-resolution, very high-speed systems. High-speed, high-resolution digital-to-analog conversion is accomplished with the reverse structure, the Advanced Filter Bank Digital-to-Analog Converter (***AFB DAC***).

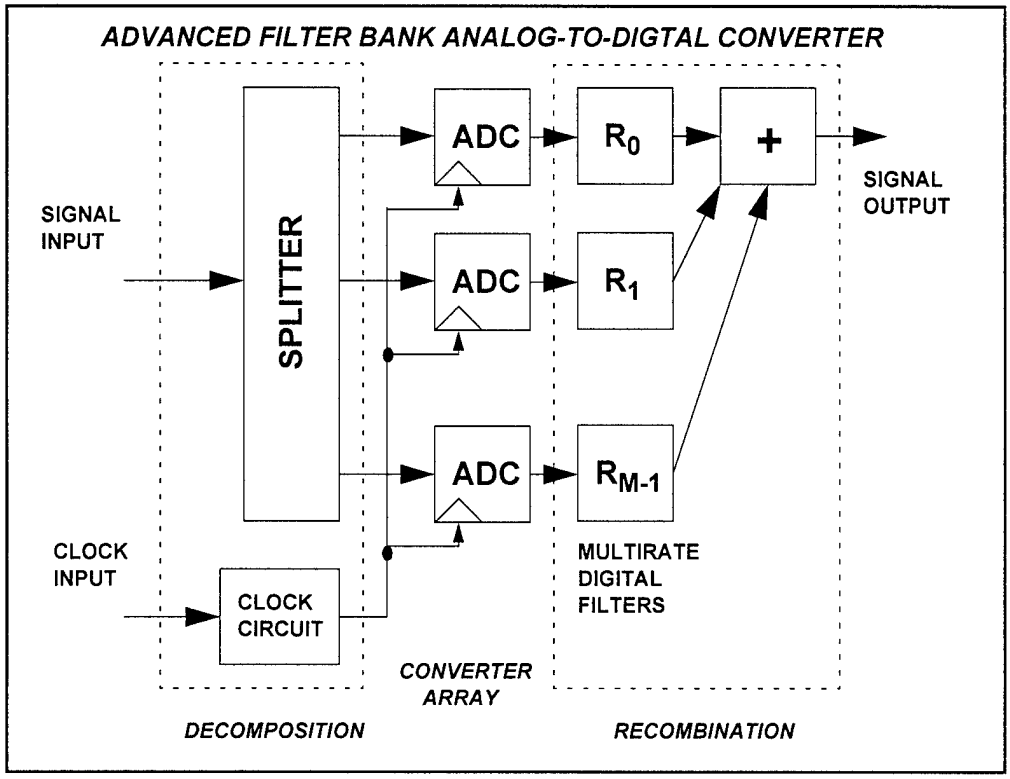

Figure 2-2. Advanced Filter Bank Analog-to-Digital Converter (*AFB ADC*).

Manufacturers such as Burr-Brown and Analog Devices have been incorporating high-precision sampling circuitry in their ADC chips which extends the sampling bandwidth of the device by up to six times the Nyquist bandwidth. Therefore, these commercially-available chips may be used in the ***AFB ADC*** configuration to improve the speed of the conversion by up to six times without necessitating the use of additional sampling circuitry. Linearity error compensation techniques may be employed to extend the dynamic range at high IF even further.

Multi-Rate Filter Bank Processing Significantly Reduces Sensitivity to Analog Mismatches

Using a filter bank for analog-to-digital conversion is an unconventional application of the architecture that improves the speed and resolution of the conversion over the Time-Interleaved array conversion technique. The ***AFB ADC*** splits the input to each ADC in the array and digital filters reconstruct the digitized signal. The ***AFB ADC*** significantly improves the speed and resolution of the conversion by attenuating the effects of analog mismatches (e.g., gain mismatch, phase distortion, clock skew, and jitter caused by imprecise analog component values, line length

mismatches, and other variations over time and temperature in the analog front-end electronics) which otherwise severely limit the resolution of the system and which prohibit existing parallel architectures (such as Time-Interleaving) from achieving high-resolution. To achieve high-resolution (greater than 12 bits), conventional parallel approaches such as Time-Interleaving require phase matching on the order of a few picoseconds and gain matching to less than -80 dB, which is very difficult (if not impossible) to achieve. However, the AFB provides very high-resolution performance with phase distortion on the order of nanoseconds and gain mismatches of approximately -50 dB, which is relatively straightforward to achieve. Since the ***AFB ADC*** architecture is insensitive to analog mismatches, it maintains optimal performance over time and across a wide range of temperatures.

The filters in the AFB significantly reduce the sensitivity to mismatch errors for two reasons: (1) the filters compensate for mismatches in the array by 20-30 dB, and (2) the filters can be used to attenuate the errors caused by mismatches in the array. The powerful digital Recombination Filters, $R_k(z)$, correct for frequency-dependent gain and phase mismatch errors between the ADCs in the array. Special calibration routines are used to design the filters to accurately match the channels. For example, if a system has mismatches which cause aliasing errors in the output at -50 dB (approximately 8 bits resolution), then the digital filters can provide channel matching to reduce the aliasing errors to approximately -75 dB. If the filters are chosen to have stopband attenuation of 15-20 dB, then aliasing errors are attenuated to below -90 dB, which would be suitable for 14-bit performance.

By using time-skewed channel clock signals for time-division multiplexing, the Decomposition splitters can simply be implemented as a simple splitter network. If more frequency-division multiplexing is required, the Decomposition processing can include filters, such as passive LC filters or discrete-time charge coupled devices (CCDs).

Time-Interleaving Approach is Very Sensitive to Mismatch Errors

For very high-speed conversion, manufacturers such as Hewlett-Packard and Tektronix have conventionally implemented Time-Interleaved ADCs which consist of an array of M moderate speed ADCs which are triggered successively at $1/M$ the effective sample rate of the system. The speed and resolution of the system is limited because the system is extremely sensitive to ADC mismatches and clock timing errors. Time-Interleaving ADCs provide up to 8 bits resolution at gigasample per second (GSa/s) speeds. With signal preconditioning and compensation for linearity and timing errors, Hewlett-Packard has built an 8 GSa/s, 8 bit, Time-Interleaved ADC with a signal bandwidth of nearly 2 GHz.[1] Effects of mismatches in converters in Time-Interleaved systems has been studied extensively.[2,3]

1. A. Montijo and K. Rush, "Accuracy in Interleaved ADC Systems," *Hewlett-Packard Journal*, pp. 36-42, October 1993.

2. A. Petraglia and S. K. Mitra, "Analysis of Mismatch Effects Among A/D Converters in a Time-Interleaved Waveform Digitizer," *IEEE Trans. on Inst. and Meas.* Vol. 40 No. 5, pp. 831-835, Oct. 1991.

3. R. Khoini-Poorfard, "Mismatch Effects in Time-Interleaved Oversampling Converters," *Proc. IEEE. Int. Symp. on Circ. and Syst.*, London, U.K., pp. 429-432, May 1994.

Switched-Capacitor Filter Bank ADCs Are Not Suitable for High-Speed Applications

Filter banks are used in a number of communications applications such as subband coders for speech signals[4], frequency domain speech scramblers[5], and image coding.[6] The theory for perfect-reconstruction digital filter banks has recently been established,[7,8,9,10]

Fully discrete-time Quadrature Mirror Filter (QMF) Banks have been applied to analog-to-digital conversion by using switched-capacitor Analysis Filters, downsamplers, an array of ADCs sampling at the subband rate, upsamplers, and digital Synthesis Filters.[11] However, the use of switched-capacitors limits the speed of the system, typically to the hundreds of kilohertz. Also, switched-capacitor filters introduce switching noise which can limit the signal-to-noise ratio (SNR) of the system.

AFB ADC Outperforms Time-Interleaving and Switched-Capacitor Filter Banks

The ***AFB ADC*** architecture overcomes the Time-Interleaved architecture's extreme sensitivity to converter mismatches and the switched-capacitor architecture's speed and noise limitations. The multirate filter bank signal processing used in the ***AFB ADC*** architecture isolate the converters in the array and attenuate the aliasing errors caused by gain and phase mismatches.[12,13,14,15,16]

Potential applications of the AFB include direct digital receivers for wireless communications; radar receivers; and test equipment such as oscilloscopes, spectrum analyzers, network analyzers, and signal and pattern generators.

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5. R. V. Cox, D. E. Boch, K. B. Bauer, J. D. Johnston, and J. H. Snyder, "The analog voice privacy system," *Proc. IEEE Int. Conf. ASSP*, pp. 341-344, April 1986.

6. J. Kovacevic, D. J. Le Gall and M. Vetterli, "Image coding with windowed modulated filter banks," *Proc. of IEEE Conf. ASSP*, pp. 1949-1952, May 1989.

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10. G. Strang and T. Q. Nguyen, *Wavelets and Filter Banks.* Wellesley-Cambridge Press: 1996.

11.A. Petraglia and S. K. Mitra, "High Speed A/D Conversion Using QMF Banks," *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 2797-2800, 1990.

12. S. R. Velazquez, "High-Performance Advanced Filter Bank Analog-to-Digital Converter for Universal RF Receivers," in *IEEE-SP Int. Symp. on Time-Frequency and Time-Scale Analysis*, October 1998.

13. S. R. Velazquez, "Hybrid Filter Banks for Analog/Digital Conversion" (Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, June 1997).

AFB ADC is Ideally-Suited for High-Performance Radar Systems and RF Communications

Achieving high-performance A/D conversion is currently the limiting factor in the cost, size, and power consumption of many electronic systems. For example, improving ADC performance in radar systems and radio frequency (RF) receivers can:

- Eliminate racks of analog electronics by performing more of the processing digitally
- Enable simultaneous support of multiple analog and digital signalling and protocols
- Seamlessly support next generation standards with software updates
- Reduce power, mass, volume and cost

A high-performance radar system employing the ***AFB ADC*** will significantly improve target tracking and discrimination in a compact, digitally-reconfigurable, easily updateable hardware solution.

Enables Software Radio

One particularly attractive application of the AFB ADC architecture and LinComp algorithm is the Software Radio, which can accommodate two or more RF modulation standards simultaneously by performing tuning and demodulation on the digital data in software.[17,18] The Software Radio can seamlessly integrate new standards as they arise. The Software Radio promises lower power, smaller size, and lower cost by processing 50 or more channels in software instead of dedicated hardware. For military applications, the Software Radio is capable of understanding many different signalling protocols with a compact, low-power transceiver. For cellular telephone applications, the Software Radio allows for universal coverage without necessitating worldwide agreement on a single standard (which, due to politics and competition, has proven to be impossible) since it can understand signals from many different types of cellular telephones.

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14. S. R. Velazquez, T.Q. Nguyen, S. R. Broadstone, "Design of Hybrid Filter Banks for Analog/Digital Conversion," in *IEEE Transactions on Signal Processing*, Volume 46, Issue 4, April 1998.

15. S. R. Velazquez, "A Hybrid Quadrature Mirror Filter Bank Approach to Analog-to-Digital Conversion," Massachusetts Institute of Technology Master's Thesis, May 1994.

16. S. R. Velazquez, T. Q. Nguyen, S. R. Broadstone, J. K. Roberge, "A Hybrid Filter Bank Approach to Analog-to-Digital Conversion," in *Proc. of IEEE-SP Int. Symp on Time-Frequency and Time-Scale Analysis*, October 1994, pp 116-119.

17. Mitola, J., 1995, "The Software Radio Architecture", *IEEE Communications Mag.*, May 1995, 26-38.

18. Lackey, R., and Upmal, D., 1995, "Speakeasy: The Military Software Radio", *IEEE Communications Mag.*, May 1995, 56-61.

3. Overview of *AFB ADC* System Design

3.1 Channel ADC Selection

Given the desired specifications for the ***AFB ADC*** to be built, the first task is to choose suitable channel ADCs for the parallel array. The channel ADCs must have the same number of bits resolution as the desired ***AFB ADC***, and to minimize the number of channels, the channel ADC sample rate should be as high as possible. The channel ADCs should be chosen such that their dynamic range and signal-to-noise ratio performance for the input frequencies used by the ***AFB ADC*** system is adequate to meet the overall system performance

3.2 Decomposition Splitter Design

The degree to which the Decomposition Splitters, $D_k(s)$, provide frequency-division multiplexing is determined by the gain and phase mismatches that still exist between the channel ADCs in the parallel array AFTER DIGITAL CALIBRATION. Careful circuit layout can yield gain and phase matching between the channels of approximately -50 dB. The powerful digital Recombination Filters, $R_k(z)$, correct for frequency-dependent gain and phase mismatch errors between the ADCs in the array. Special calibration routines are used to design the filters to accurately match the channels. The digital filters provide channel matching to reduce the mismatch errors to approximately -75 dB. If the remaining mismatch errors are limiting the dynamic range of the system, then the Decomposition Splitters may use frequency selectivity to attenuate the remaining errors. For example, if the stopband attenuation of the Decomposition splitters is 15-20 dB, the mismatch errors are attenuated to below -90 dB.

3.3 Calibration of Recombination Filters

Once the system has been built, the digital Recombination Filters are optimized such that the digital output is simply a delayed version of the analog input. Given measurements of the actual analog characteristics of the system (i.e., gain and phase of each of the channels with respect to input frequency), the digital Recombination Filters are designed to accurately combine the channel signals to form the digitized output. A computationally-efficient filter design algorithm based on the Inverse Fast Fourier Transform is used in an iterative optimization to design finite impulse response (FIR) digital Recombination filters with the shortest length possible that still provides accurate reconstruction (i.e., error signals do not limit the dynamic range of the system).

4. Channel ADC Selection

As mentioned above, the first task in the design of an ***AFB ADC*** is to choose suitable channel ADCs for the parallel array. For the example system described in this report, the desired ***AFB ADC*** specifications are 12-bit resolution and 260 MHz sample rate. Several commercially-available 12-bit ADCs with sample rates from 40 MHz to 65 MHz were evaluated. In general, the channel ADCs should be chosen such that their dynamic range and signal-to-noise ratio performance for the input frequencies used by the ***AFB ADC*** system is adequate to meet the overall system performance. The example system has a Nyquist sampling bandwidth of 130 MHz, so the dynamic range and signal-to-noise ratio performance of the channel ADCs were chosen to provide 12-bit performance for input frequencies up to 130 MHz.

4.1 Channel ADC Testing

Four commercial ADC chips were tested to evaluate their suitability for incorporation into a 4-channel ***AFB ADC*** architecture, which quadruples the sample rate without degrading the resolution. Three of the chips were rated for 40 MHz sample rate with 12 bits resolution and one chip was rated for 65 MHz sample rate with 12 bits resolution. The sampling bandwidth of the 4-channel ***AFB ADC*** architecture incorporating four 40 mega-samples per second (MSa/s) chips is 80 MHz; therefore, testing for these chips was performed with test signals up to 80 MHz to evaluate how well the chips will perform in the ***AFB ADC*** configuration. The sampling bandwidth of the 4-channel ***AFB ADC*** architecture incorporating four 65 MSa/s chips is 130 MHz; therefore, testing for this chip was performed with test signals up to 130 MHz.

The devices tested include:

National Semiconductor CLC952 (12-bit, 40 MHz sample rate)
Analog Devices AD9042 (12-bit, 40 MHz sample rate)
Burr Brown ADS800 (12-bit, 40 MHz sample rate)
Analog Devices AD6640 (12-bit, 65 MHz sample rate)

See Table 4-1 for a summary of the test results. The chips were tested for a wide range of test frequencies (up to 80 MHz for the parts sampling at 40 MHz and up to 130 MHz for the part sampling at 65 MHz).

Table 4-1. Summary of Test Results for Candidate Channel ADCs

Manufacturer	Part Number	Resolution [bits]	Sample Rate [MHz]	SFDR [dB]	SNR [dB]	Analog Bandwidth
National	CLC952	12	40	55-75	57-64	>80 MHz
Analog Devices	AD9042	12	40	65-82	60-67	>80 MHz
Burr-Brown	ADS800	12	40	58-70	55-61	>80 MHz
Analog Devices	AD6640	12	65	63-77	58-66	>130 MHz

Based on test results, the Analog Devices AD6640 (12-bit, 65 MHz sample rate) was selected for inclusion in the 12-bit, 260 MHz sample rate *AFB ADC* hardware.

The dynamic range and signal-to-noise ratio performance of the AD6640 equals or surpasses that of the other chips while providing much higher sample rate (65 MHz vs. 40 MHz). These results indicate that an ***AFB ADC*** architecture with four AD6640 chips will provide 12-bit resolution at 260 MHz sample rate (130 MHz Nyquist bandwidth).

4.2 Description of Tests

Maximum Spurious Distortion

The chips were tested with sinusoidal signals across a wide range of input frequencies. The maximum spurious distortion is the peak harmonic distortion spur, measured relative to the sinusoidal input signal [dBc]. This is a measure of the dynamic range of the chip (the Spurious Free Dynamic Range (SFDR) is the negative of the maximum spurious distortion relative to the input signal in decibels [dBc]). The distortion is expected to increase as the input test frequency increases due to accuracy of the sampling circuitry.

Residual Error

The chips were tested with sinusoidal signals across a wide range of input frequencies. Residual error quantifies the noise generated by the chip and is calculated by measuring the power in the error signal (the fundamental sinusoidal signal is subtracted from the device output, which yields the error signal). This is a measure of the noise of the chip (the Signal-to-Noise Ratio (SNR) is the negative of the residual error in decibels [dBFS]). Residual error is sometimes expressed as "effective number of bits" which can be calculated from the SNR with the $6n$-Rule:

$$SNR = 6.02n + 1.76 \quad [\text{dB}], \tag{4-1}$$

where n is the "effective number of bits". The residual error is expected to increase as the input test frequency increases due to sensitivity to phase noise or jitter in the clock source and sampling circuitry.

Gain

The chip were tested with sinusoidal signals across a wide range of input frequencies. The input signal level is constant and the output signal level is measured. This is a measure of the analog bandwidth of the device (analog bandwidth is typically defined as the frequency at which the gain is -3 dB).

Spectral Response

The Fourier output spectrum for single-tone sinusoidal input signals of varying frequencies were calculated. The spectrum reveals the dominant harmonic distortion signals and the complexity of the harmonic distortion profile. Note that simpler harmonic distortion profiles (those where only two or three harmonic components are dominant) can be digitally corrected more easily than complex harmonic distortion profiles by using separate linearity correction algorithms (such as the V Company ***LinComp*** algorithm), which were not considered in this project.

4.3 Test Results for Analog Devices AD6640 ADC (12 bits, 65 MHz sample rate)

Maximum Spurious Distortion

The SFDR is greater than approximately 63 dB up to 130 MHz input. The performance is better (approximately 70 dB) up to about 90 MHz input.

Residual Error

The SNR is greater than approximately 58 dB up to 130 MHz input. Performance steadily declines from 66 dB at low frequencies.

Gain

The analog bandwidth is greater than 130 MHz (gain is about 0.5 dB at 130 MHz input).

Spectral Response

The Fourier Spectrum showed a simple harmonic distortion profile for all input frequencies (only two or three harmonics dominated).

4.3.1 Performance Plots

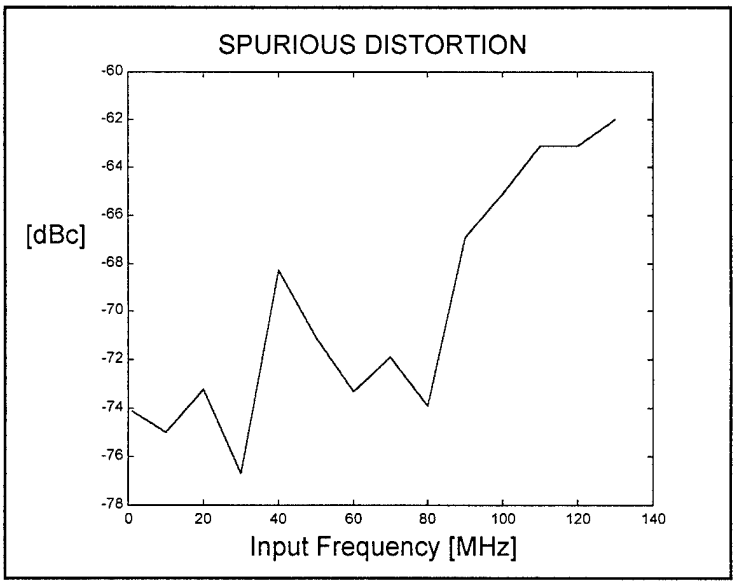

Figure 4-1. Maximum Spurious Distortion (i.e., negative of Spurious Free Dynamic Range (SFDR)) for AD6640 (12-bit, 65 MHz)

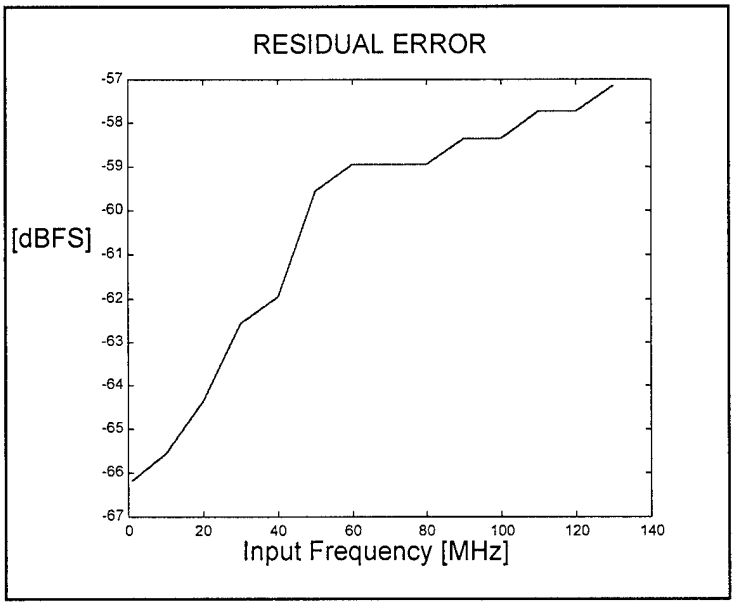

Figure 4-2. Residual Error (i.e, negative of Signal-to-Noise Ratio (SNR)) for AD6640 (12-bit, 65 MHz)

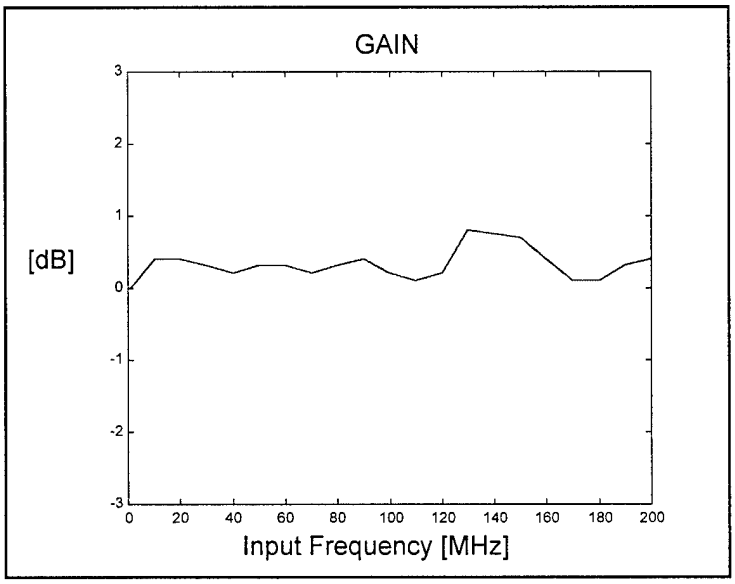

Figure 4-3. Gain (Analog Bandwidth) for AD6640 (12-bit, 65 MHz)

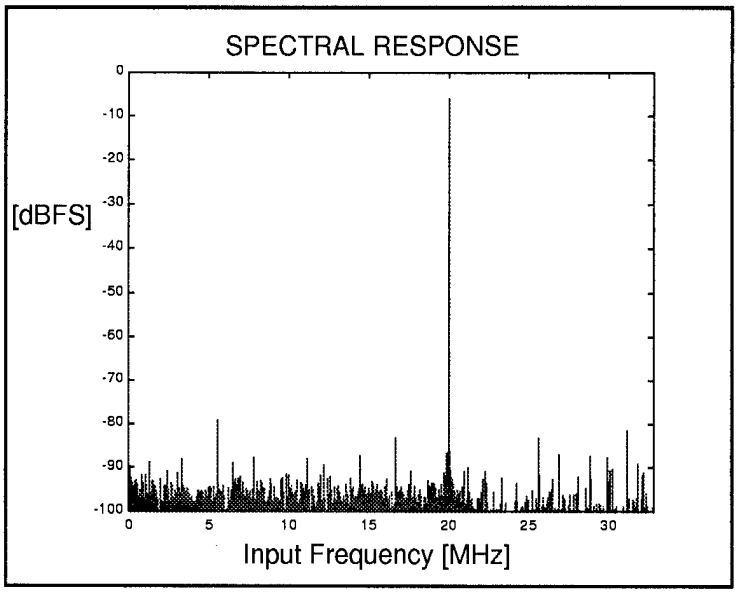

Figure 4-4. Spectral Response for 20 MHz input (first Nyquist zone) for AD96640 (12-bit, 65 MHz)

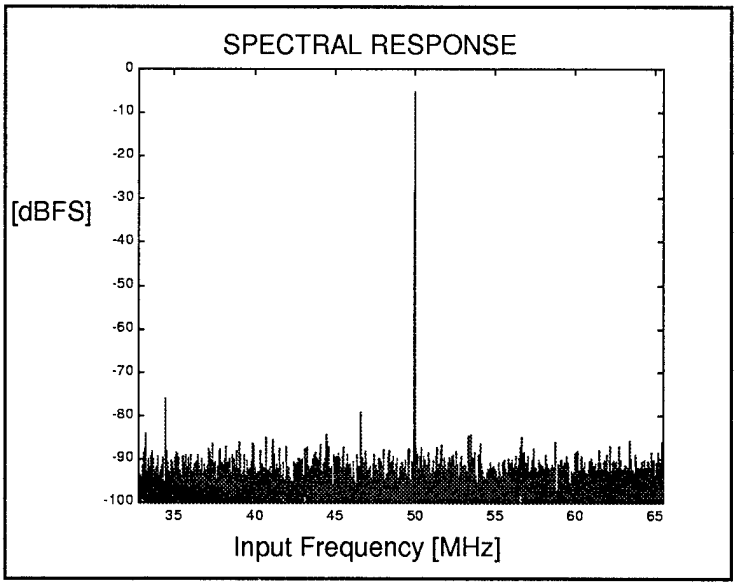

Figure 4-5. Spectral Response for 50 MHz input (second Nyquist zone) for AD6640 (12-bit, 65 MHz)

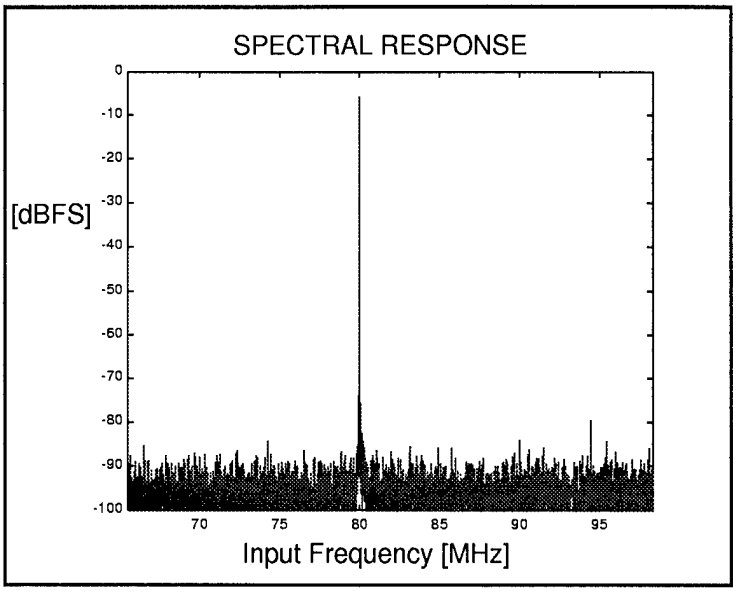

Figure 4-6. Spectral Response for 80 MHz input (third Nyquist zone) for AD6640 (12-bit, 65 MHz)

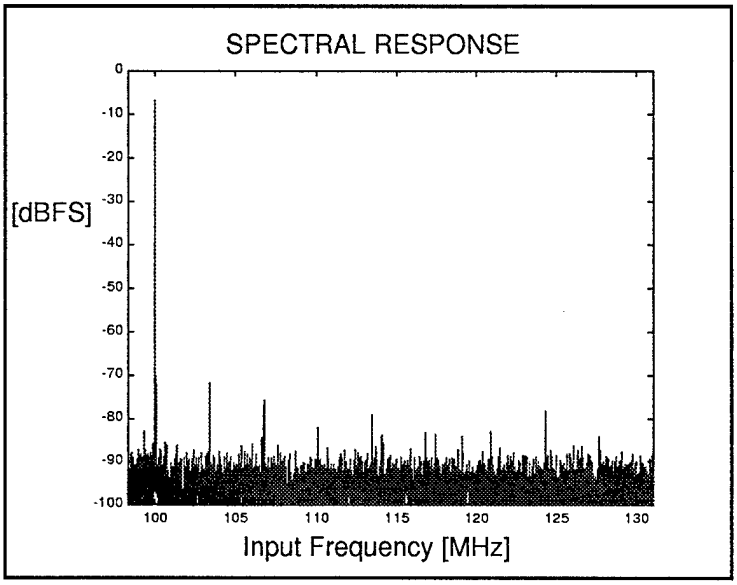

Figure 4-7. Spectral Response for 100 MHz input (fourth Nyquist zone) for AD6640 (12-bit, 65 MHz)

5. *AFB ADC* Pre-Prototype Hardware

To demonstrate the significant performance enhancements afforded by the ***AFB ADC***, a 12-bit system with 260 MHz sample rate using four 65 MSa/s, 12-bit channel ADCs was built. The configuration includes four ADC Boards (each includes a single channel ADC and FIFO memory) which are stacked vertically and mated to a Main Board (which includes the FPGA controller, Input Signal Splitter, and Clock Circuitry). The test apparatus is approximately 10 cm wide by 15 cm long by 5 cm high. This approach was chosen for this pre-prototype implementation to allow great flexibility in testing (capability to change clocking options, easy access to each channel ADC). As a future upgrade, the board layout design could easily be modified to accept the new Analog Devices AD6644 (14-bit, 80 MSa/S) ADC parts if they become available in late 1999 or early 2000 (these parts would provide ***AFB ADC*** performance with 14-bit resolution and 320 MHz sample rate).

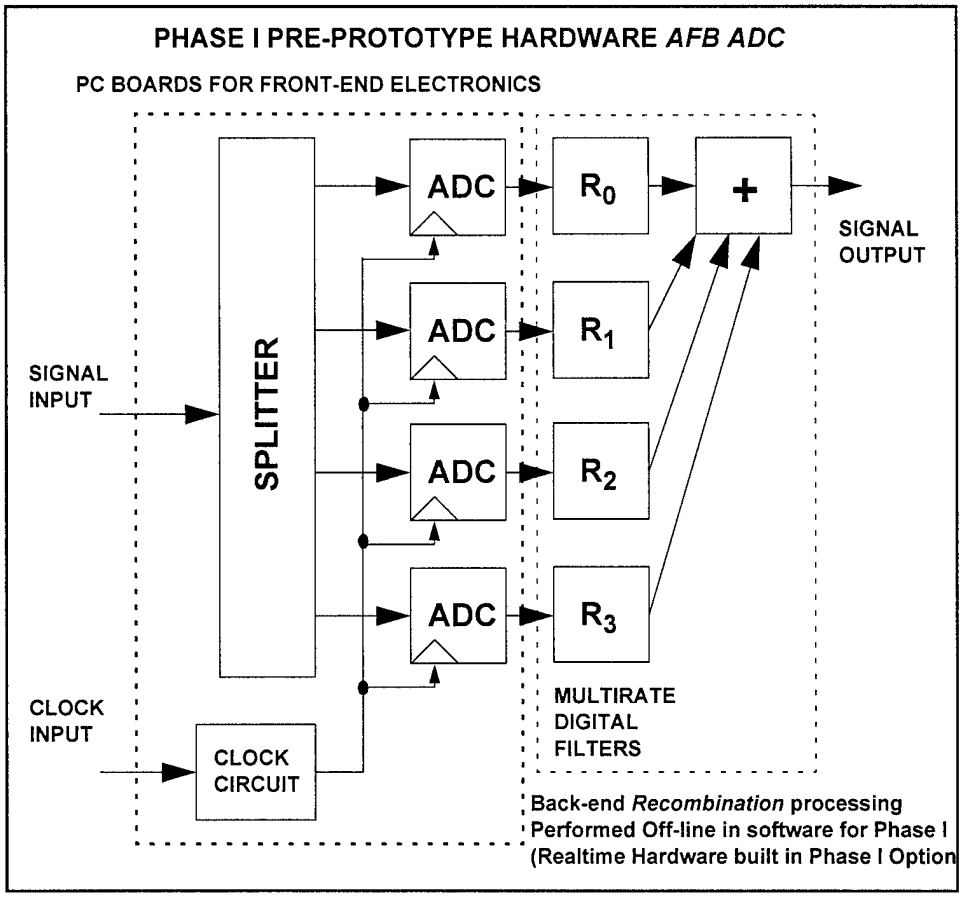

Figure 5-1. Pre-prototype hardware *AFB ADC* (12 bit, 260 MHz).

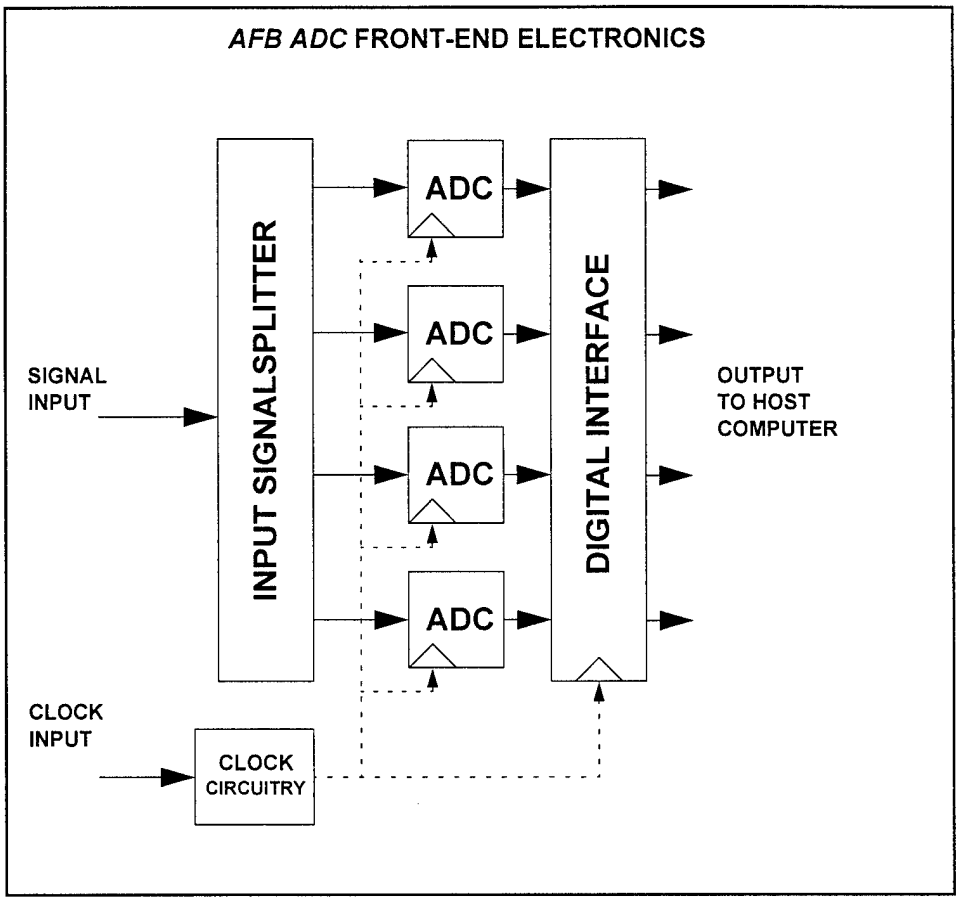

Figure 5-2. Front-End Electronics for 12-bit, 260 MHz *AFB ADC* System. System inputs include the analog input signal and the sample clock signal. Outputs include four 12-bit digital signals (total of 48 bits).

Decomposition Splitter Design

Ideally, the Decomposition Splitters, $D_k(s)$, and Recombination Filters, $R_k(z)$, are designed such that the system output, $Y(e^{j\omega})$, should simply be a scaled, delayed version of the input, $U(j\Omega)$,

$$Y(e^{j\omega}) = \sum_{m=0}^{M-1} U(j(\omega M - 2\pi m)/T)\, T_m(e^{j\omega}) = M e^{-j\omega D}\, U(j\omega M/T) \quad , \tag{5-1}$$

where D is the system delay, T is the channel ADC sample period, and the *distortion/aliasing* functions, $T_m(e^{j\omega})$, are

$$T_m(e^{j\omega}) = \sum_{k=0}^{M-1} R_k(e^{j\omega})\, D_k(j(\omega M - 2\pi m)/T) = \begin{cases} M e^{-j\omega d} & m = 0 \\ 0 & m = 1, 2, \ldots, M-1 \end{cases} . \tag{5-2}$$

$T_0(e^{j\omega})$ is the *distortion* function and corresponds to the gain and phase of the system, and

$T_m(e^{j\omega})$, $1 \le m \le M-1$, are the *aliasing* functions and correspond to the aliasing errors in the system. Equation 5-2 corresponds to the traditional "perfect reconstruction" (PR) conditions. The goal in the design of the ***AFB ADC*** system is to design the Decomposition Splitters to have the required frequency selectivity properties and to approximate the perfect reconstruction conditions as closely as possible. *Distortion* should be small (e.g., less than a tenth of a dB deviation from ideal 0 dB) and *aliasing* error should be minimized so that it does not limit the resolution of the system (e.g., -75 dB for a 12-bit system).

As mentioned earlier, the degree to which the Decomposition Splitters, $D_k(s)$, provide frequency-division multiplexing is determined by the gain and phase mismatches that still exist between the channel ADCs in the parallel array AFTER DIGITAL CALIBRATION. Since the splitters can be used to attenuate the effects of mismatches between the channel ADCs in the array, the *stopband* gain is related to the ADC mismatch errors. Mismatches cause *aliasing* errors which limit the *Spurious Free Dynamic Range* (*SFDR*). The relationship is derived in Velazquez[19] and the result for gain mismatches between the channel ADCs is

$$SFDR = \frac{1}{E\{\ a^2\ \}\ 2(stopband)^2}, \tag{5-3}$$

where $E\{\ a^2\ \}$ is the expected value of the gain mismatch error between ADCs in the array after digital calibration. For example, assuming a good 14-bit ADC has *SFDR* = 90 dB and that the channel ADCs have mismatch error $E\{\ a^2\ \}$= -75 dB (after digital calibration). Therefore, from Equation (5-3), the required *stopband* gain is -18 dB.

However, not all systems require Decomposition splitters that have frequency selectivity. For the 12-bit example system described in this report, the desired *SFDR* = 75 dB and the channel ADCs have mismatch error $E\{\ a^2\ \}$= -75 dB (after digital calibration). The required *stopband* gain is 0 dB, so the Decomposition splitters do not need to provide frequency selectivity.

For systems that require frequency selectivity, one option for the Decomposition Splitters is to simply use off-the-shelf filters that meet the required stopband specifications. This is the simplest solution, but as discussed in Velazquez[19] the characteristics of some standard filter types complicate the reconstruction demands of the digital Reconstruction Filters. For example, Chebyshev or Elliptic filters can have passband ripple and non-constant group delay which require Synthesis Filters to be very high order to provide accurate signal reconstruction; Butterworth filters, which have no passband ripple and nearly constant group delay, enable lower order Synthesis Filters to provide accurate signal reconstruction. An alternative is to constrain the number of poles and zeros in the Decomposition Splitters, and iteratively optimize the pole and zero locations to provide both adequate channelization and accurate signal reconstruction with low-order Recombination Filters. This method is discussed in Velazquez.[19]

19. S. R. Velazquez, "Hybrid Filter Banks for Analog/Digital Conversion" (Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, June 1997).

6. AFB ADC System Calibration

6.1 Recombination Filter Optimization

As described earlier, the Recombination Filters, $R_k(z)$, should be optimized such that the system output, $Y(e^{j\omega})$, is simply be a scaled, delayed version of the input, $U(j\Omega)$,

$$Y(e^{j\omega}) = \sum_{m=0}^{M-1} U(j(\omega M - 2\pi m)/T)\ T_m(e^{j\omega}) = Me^{-j\omega D}\ U(j\omega M/T), \qquad (6\text{-}1)$$

where D is the system delay, T is the channel ADC sample period, and the *distortion/aliasing* functions, $T_m(e^{j\omega})$, are

$$T_m(e^{j\omega}) = \sum_{k=0}^{M-1} R_k(e^{j\omega})\ D_k(j(\omega M - 2\pi m)/T) = \begin{cases} Me^{-j\omega d} & m = 0 \\ 0 & m = 1, 2, \ldots, M-1 \end{cases}. \qquad (6\text{-}2)$$

$T_0(e^{j\omega})$ is the *distortion* function and corresponds to the gain and phase of the system, and $T_m(e^{j\omega})$, $1 \le m \le M-1$, are the *aliasing* functions and correspond to the aliasing errors in the system. The goal in the calibration of the ***AFB ADC*** system is to optimize the Recombination Filters to approximate the perfect reconstruction conditions (Equation 6-2) as closely as possible. *Distortion* should be small (e.g., less than a tenth of a dB deviation from ideal 0 dB) and *aliasing* error should be minimized so that it does not limit the resolution of the system (e.g., -75 dB for a 12-bit system).

Given the system delay, D, and the Decomposition splitters, $D_k(s)$, the perfect reconstruction constraints in Equation (6-2) can be solved for the frequency response of the ideal Recombination filters, $R_k(z)$.

An efficient Recombination Filter design algorithm based upon the Fast Fourier Transform is used to design FIR digital filters that approximate the ideal frequency response as closely as possible.[20]

The design of the Recombination Filters also requires specification of the system delay, D, which can be optimized to further improve the reconstruction accuracy. The system delay, D, is iteratively adjusted, the Recombination Filters are re-calculated, and the process is repeated until the reconstruction is accuracy is sufficient. Standard minimization algorithms, such as Matlab's *fmin*, can be used. Note that the system delay is not necessarily an integer. This optimization is computationally efficient because it relies on iterated evaluations of the Inverse FFT, and it can calculate optimal Recombination Filters and system delay in a matter of seconds.

The Recombination Filter length, L, should be the smallest value that still yields the desired *distortion* and *aliasing* error. As mentioned earlier, the *distortion* should be small (e.g., less than a tenth of a dB deviation from ideal 0 dB) and the *aliasing* should be lower than the desired *SFDR* of the system.

20. S. R. Velazquez, "Hybrid Filter Banks for Analog/Digital Conversion" (Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, June 1997).

Recombination Filters Compensate for Channel Mismatch Errors

Gain and phase delay errors in the k^{th} channel ADC in the array are described as

$$A_k(e^{j\omega}) = (1 + a_k(\omega))\, e^{-j\omega d_k(\omega)}, \quad -\pi \le \omega \le \pi, \tag{6-5}$$

where $a_k(\omega)$ is the frequency-dependent gain error and $d_k(\omega)$ is the frequency-dependent phase delay error. With the ADC distortion modeled as in Equation 6-5, the AFB output, $Y(e^{j\omega})$, becomes

$$Y(e^{j\omega}) = \sum_{m=0}^{M-1} U(j(\omega M - 2\pi m)/T)\, \hat{T}_m(e^{j\omega}), \tag{6-6}$$

where the new *distortion/aliasing* functions, $\hat{T}_m(e^{j\omega})$, are

$$\hat{T}_m(e^{j\omega}) = \sum_{k=0}^{M-1} A_k(e^{j\omega M})\, R_k(e^{j\omega})\, D_k(j(\omega M - 2\pi m)/T). \tag{6-7}$$

Note that the channel ADCs do not need to have zero gain and phase error for *aliasing* errors to be canceled. If the gain and phase errors in the ADCs are equal but non-zero

$$A_k(e^{j\omega}) = A(e^{j\omega}) \neq 1, \tag{6-8}$$

(i.e., the converters are *matched* in gain and phase) then the term $A(e^{j\omega})$ can be factored outside the summation in the *distortion/aliasing* functions,

$$\hat{T}_m(e^{j\omega}) = A(e^{j\omega M})\, T_m(e^{j\omega}) = \begin{cases} A(e^{j\omega M})\, M e^{-j\omega D} & m = 0 \\ 0 & m = 1, 2, \ldots, M-1 \end{cases}, \tag{6-9}$$

so aliasing is cancelled. The converters need not be perfect to cancel aliasing (aliasing is often the dominant error source in the ***AFB ADC***), they need only be *matched* in gain and phase to each other, which greatly simplifies the optimization of the Recombination Filters. One of the main functions of the digital Recombination Filters in the ***AFB ADC*** is to improve the matching of the channel ADCs in the array by 20-30 dB.

Gain and phase mismatch errors degrade the resolution of the system by degrading the *distortion/aliasing* functions. Figures 6-1 and 6-2 depict the effects of gain mismatch errors, which are seen as undesired spectral components in the system output. Figure 6-2 shows how the Recombination Filter optimization reduces the effects of mismatch errors by approximately 20-30 dB.

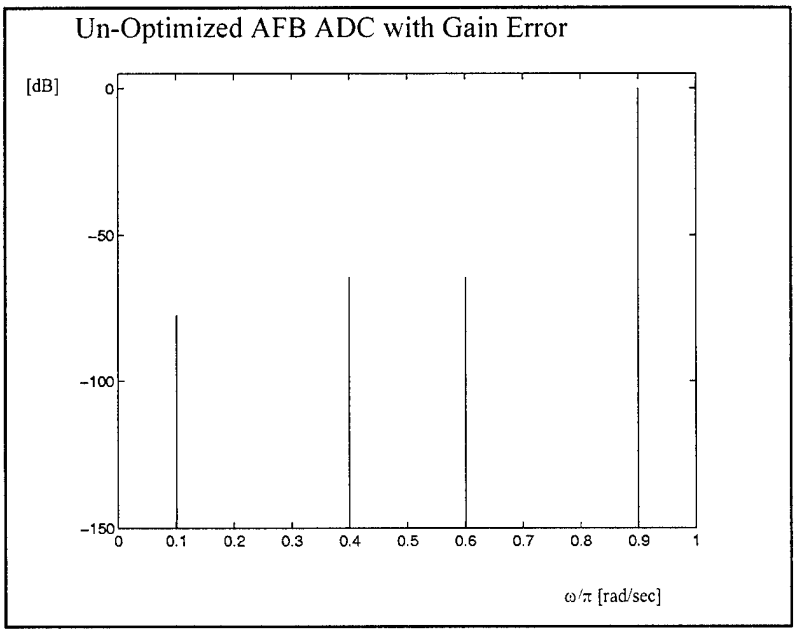

Figure 6-1. Output of *M*=4 *AFB ADC* system BEFORE RECOMBINATION FILTER OPTIMIZATION. Gain mismatch errors ($E\{ a^2 \} = 10^{-6}$, -60 dB) in frequency domain. Input is sinusoidal signal at $\omega \approx 0.9\pi$. Errors are seen as aliasing spurs. Compare to the performance of the optimized *AFB ADC* in Figure 6-2.

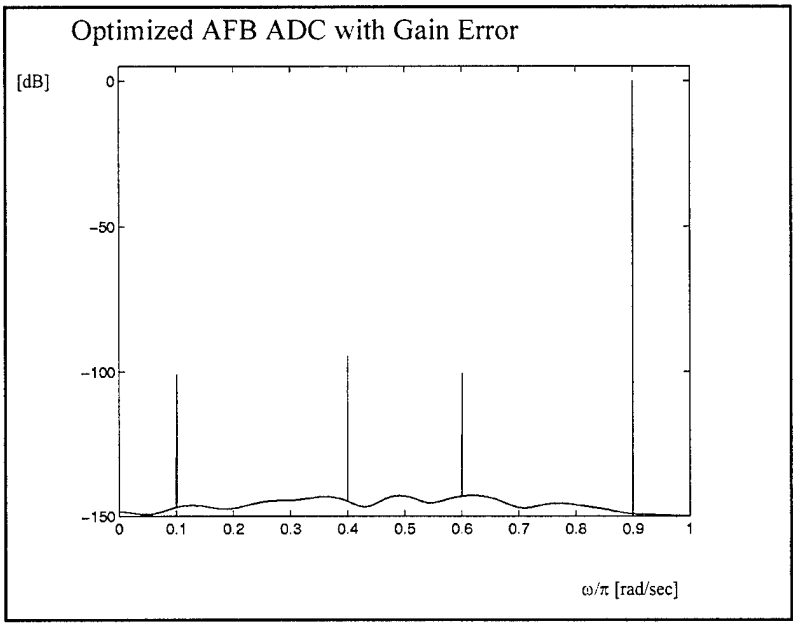

Figure 6-2. Output of *M*=4 *AFB ADC* AFTER RECOMBINATION FILTER OPTIMIZATION. Gain mismatch errors ($E\{ a^2 \} = 10^{-6}$, -60 dB). Input is sinusoidal signal at $\omega \approx 0.9\pi$. Errors are seen as aliasing spurs, which are compensated by the Recombination Filters. Compare to the performance of the Un-Optimized *AFB ADC* system in Figure 6-1.

7. 12-bit, 260 MHz *AFB ADC* Hardware Testing Results

The Recombination Filters were optimized as described above to yield four length 64 digital FIR filters with 12-bit coefficients. Buffers of data from the hardware were imported into Matlab software where the Recombination Filtering was performed.

The V Company high-performance ADC testbed was used for testing. Test equipment includes:

- Two Hewlett-Packard HP8656B high-performance synthesized signal generators (for single and multi-tone sinusoidal testing and clock source generation)
- Arbitrary waveform generator
- High-speed data acquisition system interfaced to a host computer with Matlab software
- Tektronix TDS3054 4-channel, 500 MHz digitizing oscilloscope
- Two Topward 4302 bench power supplies (low noise, low ripple linear supplies)

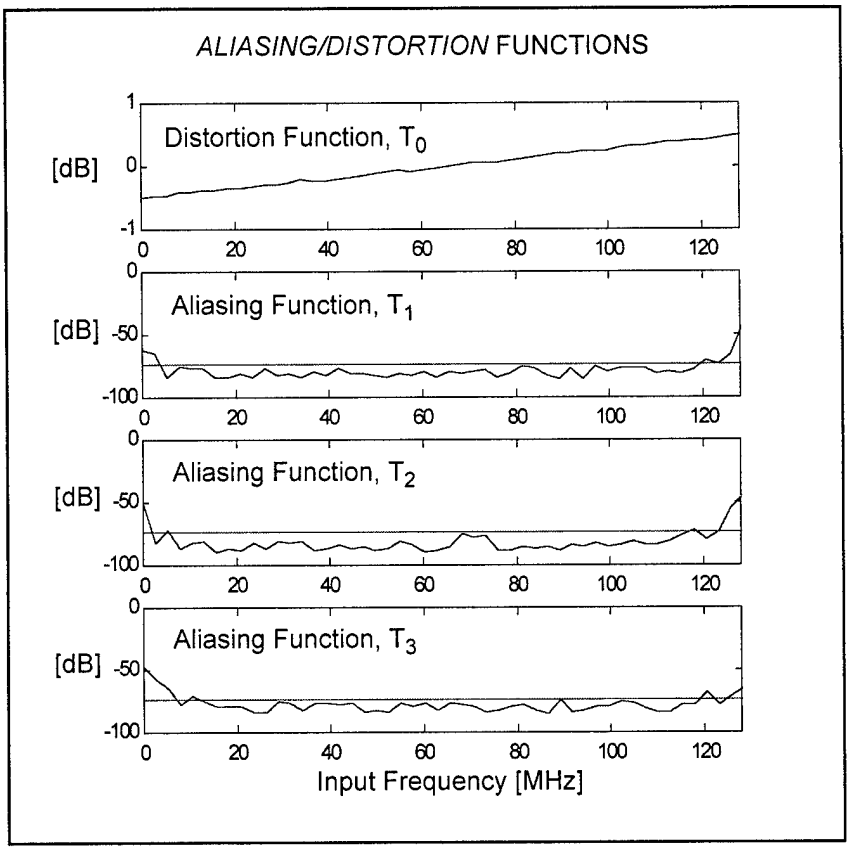

Figure 7-1. *Aliasing/Distortion* functions for 12-bit, 260 MSa/s *AFB ADC* hardware. The magnitude of the *distortion* function corresponds to the gain of the *AFB ADC* transfer function with respect to input frequency. The *aliasing* functions correspond to the aliasing errors in the *AFB ADC* output signal. The dashed lines indicate 12-bit resolution (-74 dBFS).

7.1 Aliasing/Distortion Functions

$T_0(e^{j\omega})$ is the *distortion* function and corresponds to the gain and phase of the system, and $T_m(e^{j\omega})$, $1 \le m \le 3$, are the *aliasing* functions and correspond to the aliasing errors in the system.

The goal in the calibration of the ***AFB ADC*** system is to optimize the Recombination Filters to approximate the perfect reconstruction conditions as closely as possible: *distortion* should be small (e.g., less than a tenth of a dB deviation from ideal 0 dB) and *aliasing* error should be minimized so that it does not limit the resolution of the system (e.g., -74 dB for a 12-bit system).

7.2 Maximum Spurious Distortion

The system was tested with sinusoidal signals across a wide range of input frequencies. The maximum spurious distortion is the peak harmonic distortion spur, measured relative to the sinusoidal input signal [dBc]. This is a measure of the dynamic range of the chip (the Spurious Free Dynamic Range (SFDR) is the negative of the maximum spurious distortion relative to the input signal in decibels [dBc]). Aliasing errors in the ***AFB ADC*** architecture can limit the SFDR of the system, so the digital Recombination filters are optimized to insure that the aliasing errors are accurately cancelled and do not limit the resolution.

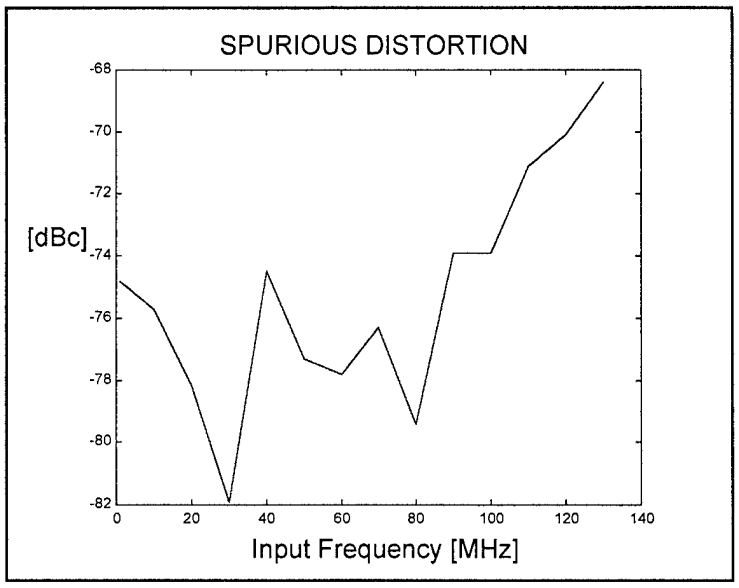

Figure 7-2. Maximum Spurious Distortion (i.e., negative of Spurious Free Dynamic Range (SFDR)) for *AFB ADC* hardware (12-bit, 260 MHz). Note that performance is approximately 3-6 dB better than that shown for the ADC component testing (Figure 4-1 on page 11) because the prototype hardware had circuitry improvements over the relatively inexpensive Analog Devices evaluation board used in the ADC component testing, leading to cleaner performance overall.

7.3 Residual Error

The system was tested with sinusoidal signals across a wide range of input frequencies. Residual error quantifies the noise generated by the chip and is calculated by measuring the power in the error signal (the fundamental sinusoidal signal is subtracted from the device output, which yields the error signal). This is a measure of the noise of the system (the Signal-to-Noise Ratio (SNR) is the negative of the residual error in decibels [dBFS]). Residual error is sometimes expressed as "effective number of bits" which can be calculated from the SNR with the $6n$-Rule:

$$SNR = 6.02n + 1.76 \quad [\text{dB}], \tag{7-1}$$

where n is the "effective number of bits". The residual error normally increases as the input test frequency increases due to sensitivity to phase noise or jitter in the clock source and sampling circuitry.

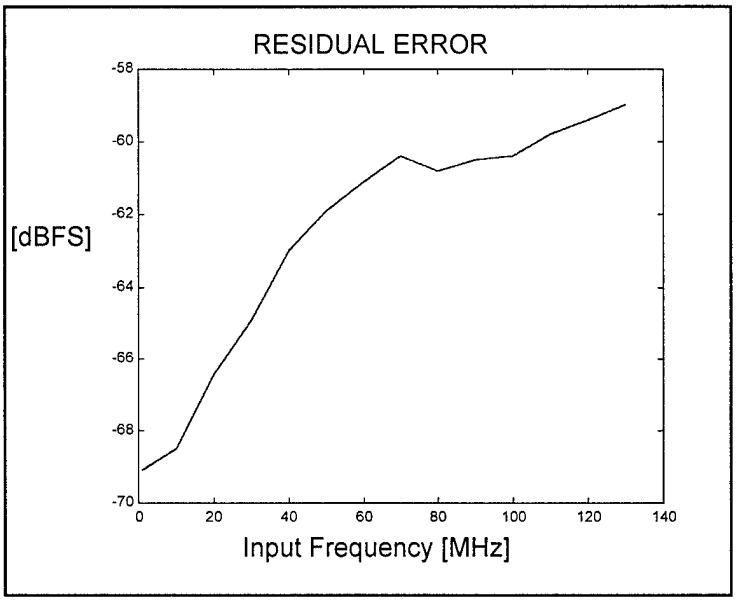

Figure 7-3. Residual Error (i.e, negative of Signal-to-Noise Ratio (SNR)) for *AFB ADC* hardware (12-bit, 260 MHz). Note that performance is approximately 2 dB better than that shown for the ADC component testing (Figure 4-2 on page 12) because the prototype hardware had circuitry improvements over the relatively inexpensive Analog Devices evaluation board used in the ADC component testing, leading to cleaner performance overall.

7.4 Spectral Response

The Fourier output spectrum for single-tone sinusoidal input signals and multi-tone input signals is shown. The single-tone spectra reveal the dominant harmonic distortion signals and the complexity of the harmonic distortion profile. Note that simpler harmonic distortion profiles (those where only two or three harmonic components are dominant) can be digitally corrected more easily than complex harmonic distortion profiles by using separate linearity correction algorithms (such as the V Company ***LinComp*** algorithm), which were not considered in this project. The single-tone spectra confirm that the aliasing error signals generated by the system are accurately cancelled in the system output so they do not limit the resolution of the system.

The multi-tone testing was designed to demonstrate the powerful aliasing error cancellation properties of the ***AFB ADC*** architecture. The test input signal consisted of two sinusoidal signals at 80 MHz and 90 MHz (from synthesized signal generator sources) and a pseudorandom noise signal spanning 0 - 15 MHz (from a precision digital-to-analog converter arbitrary waveform generator). The ***AFB ADC*** architecture introduces three aliasing error signals (in the case of a four-channel system), which must be accurately canceled in the output. These error signals are seen in the channel outputs as replicas of the input signal shifted in frequency. For this multi-tone testing, the aliasing errors actually overlap with the desired signals in the channel outputs (as shown in Figures 7-11 through 7-14 below). The powerful ***AFB ADC*** digital signal processing adjusts the amplitude and phase of the signals to cancel the error signals and retain the desired signal when the channel signals are summed to form the system output.

7.4.1 Single-Tone Sinusoidal Testing

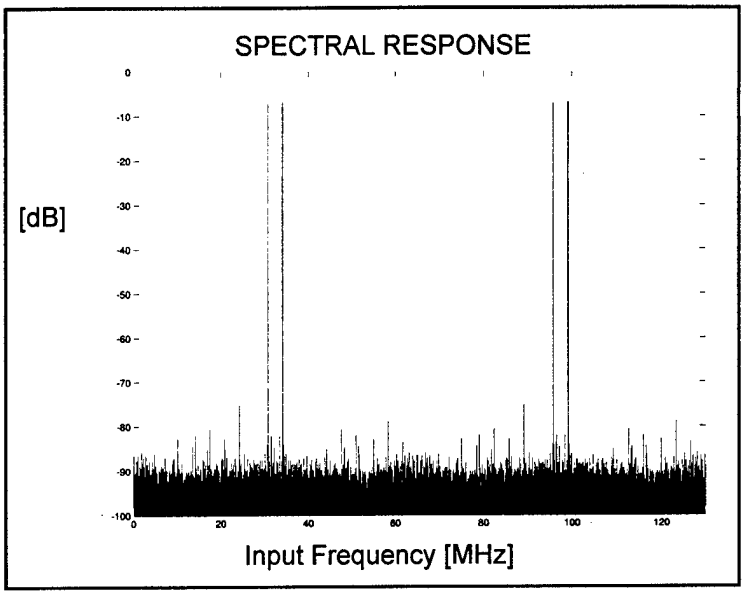

Figure 7-4. Channel 1 output Spectral Response with 100 MHz single-tone sinusoidal input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of 3 aliasing signals (at 30 MHz, 35 MHz, and 95 MHz) which must be cancelled in the *AFB ADC* system output.

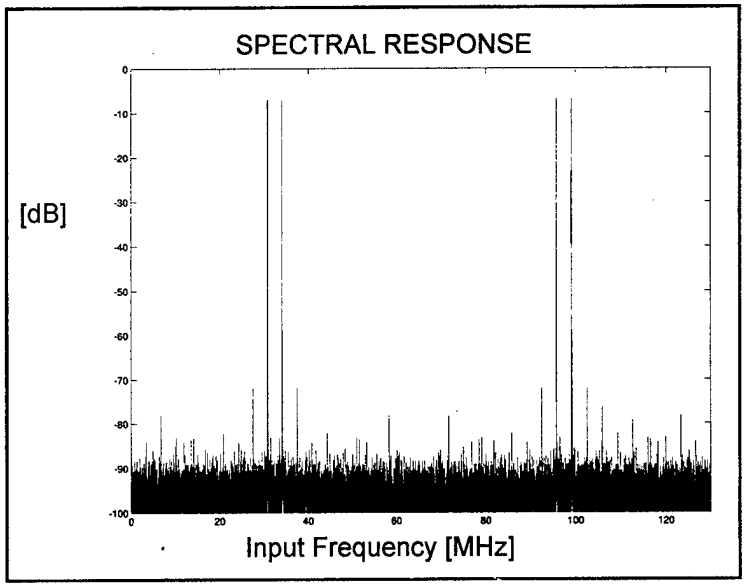

Figure 7-5. Channel 2 output Spectral Response with 100 MHz single-tone sinusoidal input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of 3 aliasing signals (at 30 MHz, 35 MHz, and 95 MHz) which must be cancelled in the *AFB ADC* system output.

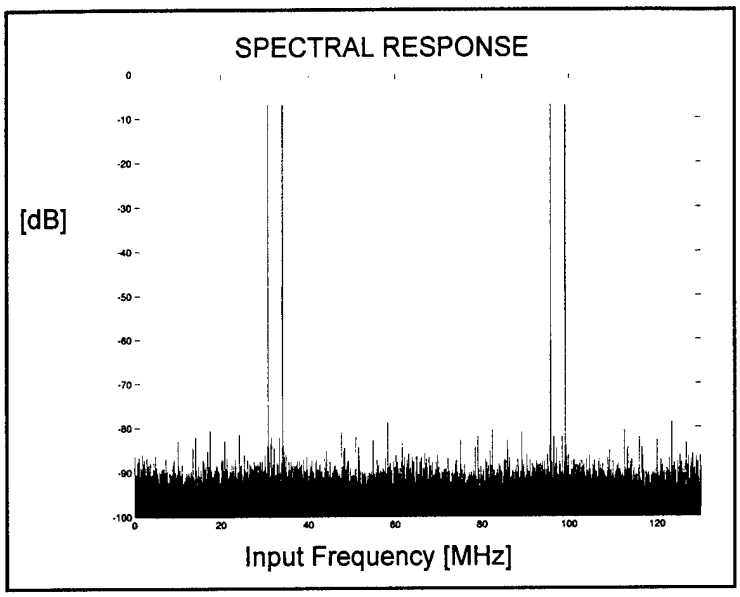

Figure 7-6. Channel 3 output Spectral Response with 100 MHz single-tone sinusoidal input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of 3 aliasing signals (at 30 MHz, 35 MHz, and 95 MHz) which must be cancelled in the *AFB ADC* system output.

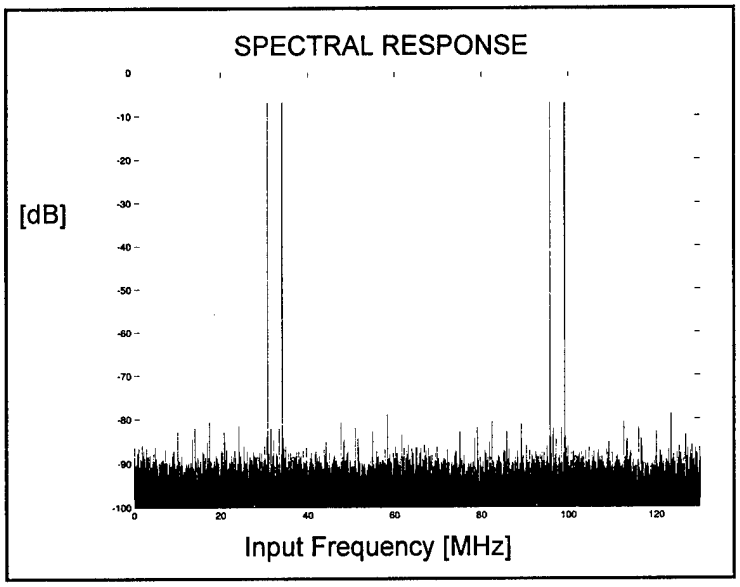

Figure 7-7. Channel 4 output Spectral Response with 100 MHz single-tone sinusoidal input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of 3 aliasing signals (at 30 MHz, 35 MHz, and 95 MHz) which must be cancelled in the *AFB ADC* system output.

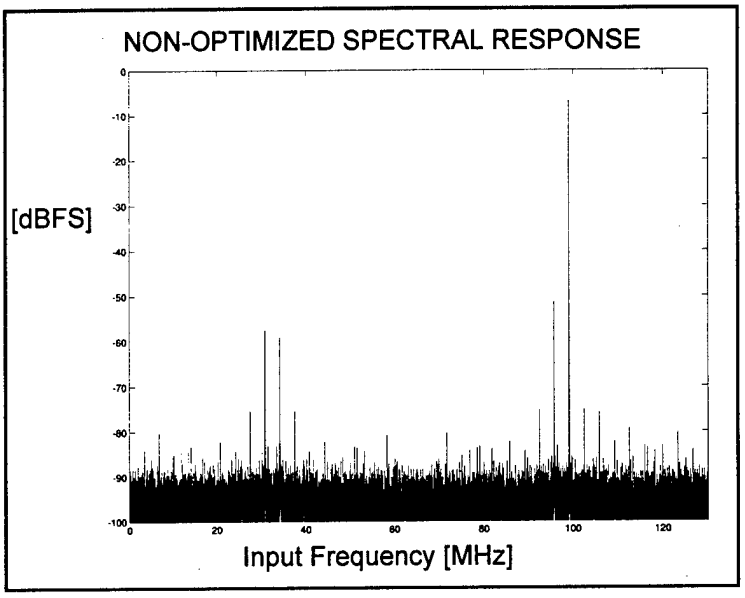

Figure 7-8. Output Spectral Response for 100 MHz single-tone sinusoidal input for *AFB ADC* hardware (12-bit, 260 MHz) with Non-Optimized digital Recombination Filters. Note that the 3 aliasing signals (at 30 MHz, 35 MHz, and 95 MHz) are not accurately cancelled and therefore limit the resolution of the system (SFDR is approximately 55 dB).

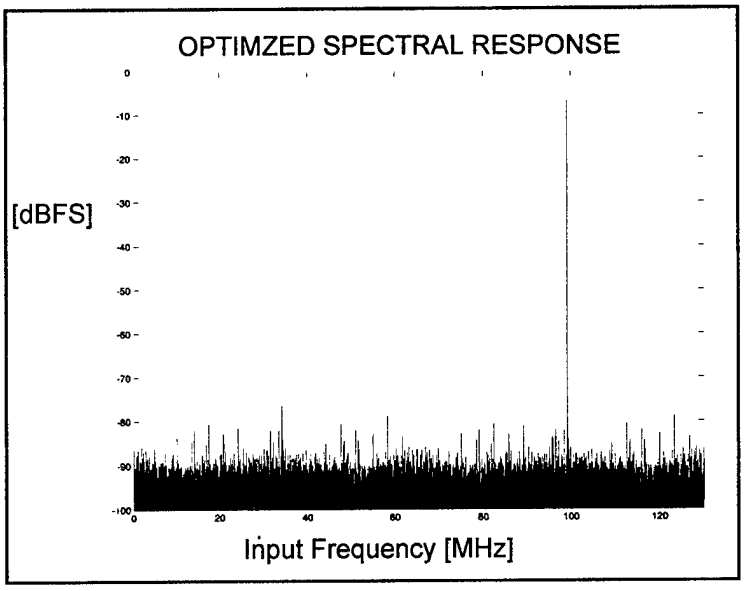

Figure 7-9. Output Spectral Response for 100 MHz single-tone sinusoidal input for *AFB ADC* hardware (12-bit, 260 MHz) with Optimized digital Recombination Filters. Note how the Recombination Filters compensate for the mismatch errors to cancel the aliasing error signals by an additional 20-30 dB so the remaining errors do not limit the resolution of the system.

7.4.2 Multi-Tone Testing

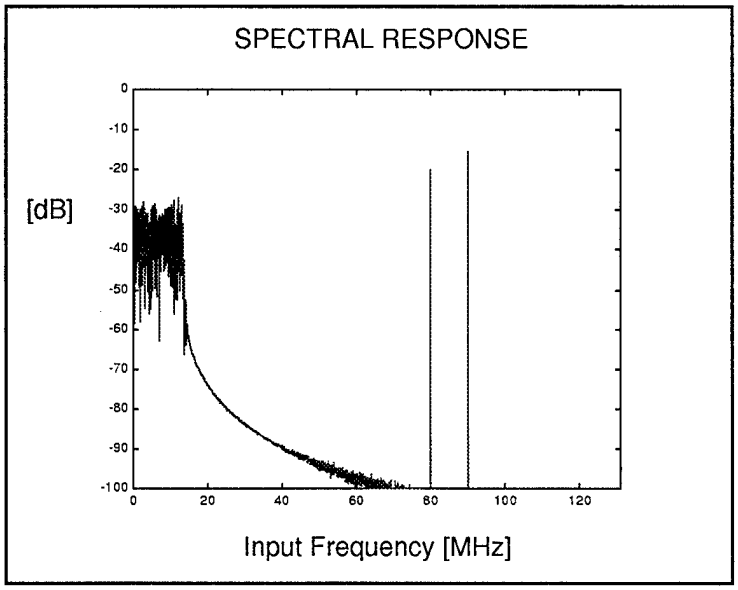

Figure 7-10. Spectral Response of multi-tone input signal for testing of *AFB ADC* hardware (12-bit, 260 MHz). The input signal consists of two sinusoidal signals at 80 MHz and 90 MHz (from synthesized signal generator sources) and a pseudorandom noise signal spanning 0 - 15 MHz (from a precision digital-to-analog converter).

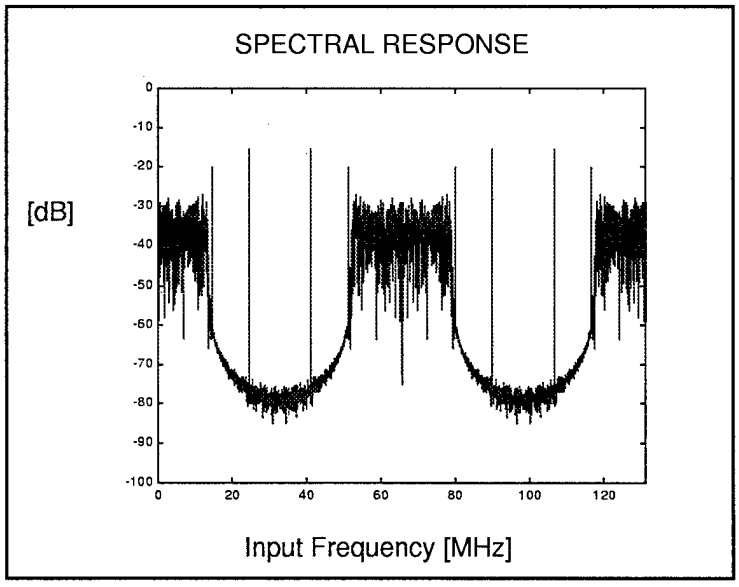

Figure 7-11. Channel 1 output Spectral Response with multi-tone input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of overlapping aliasing signals which must be cancelled in the *AFB ADC* system output.

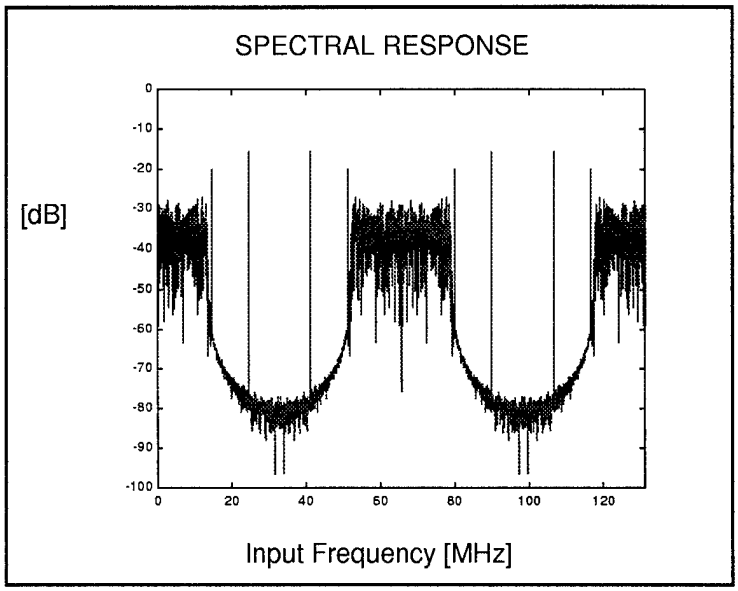

Figure 7-12. Channel 2 output Spectral Response with multi-tone input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of overlapping aliasing signals which must be cancelled in the *AFB ADC* system output.

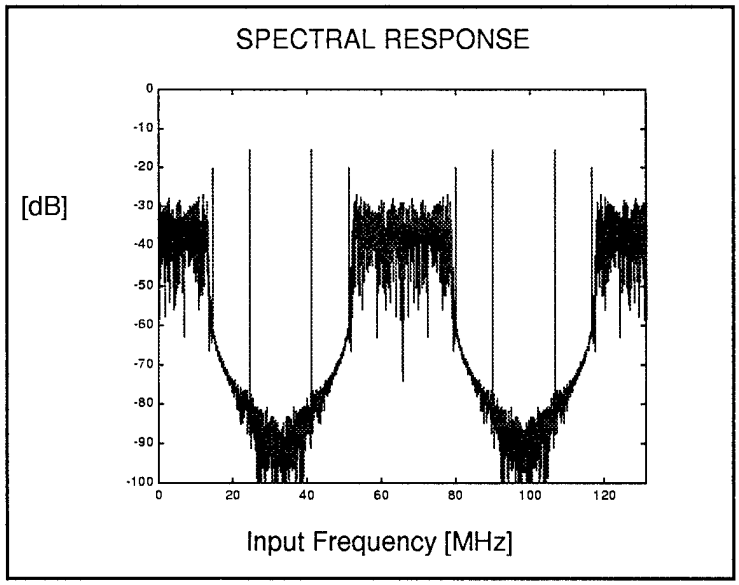

Figure 7-13. Channel 3 output Spectral Response with multi-tone input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of overlapping aliasing signals which must be cancelled in the *AFB ADC* system output.

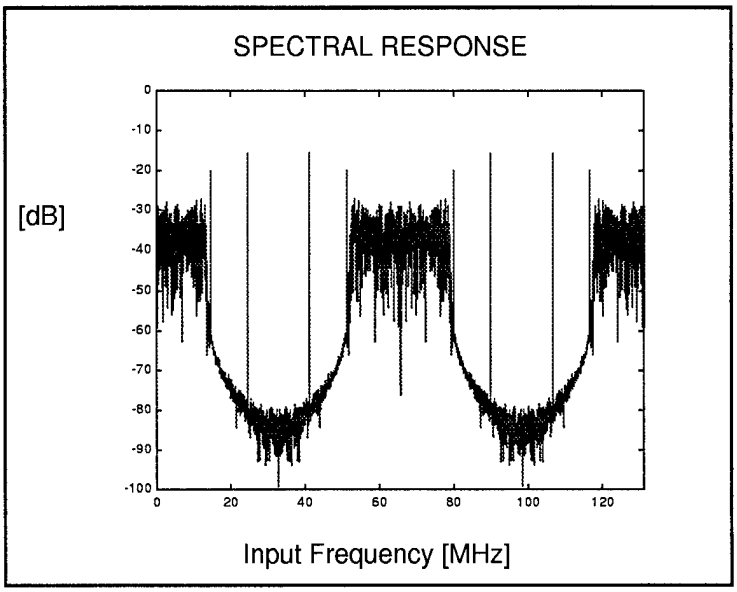

Figure 7-14. Channel 4 output Spectral Response with multi-tone input for *AFB ADC* hardware (12-bit, 260 MHz). Note the presence of overlapping aliasing signals which must be cancelled in the *AFB ADC* system output.

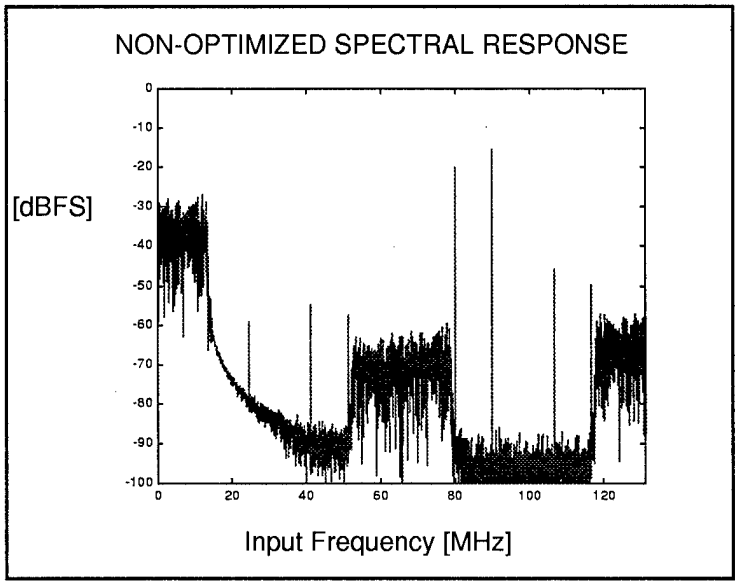

Figure 7-15. Output Spectral Response with multi-tone input for *AFB ADC* hardware (12-bit, 260 MHz) with Non-Optimized digital Recombination Filters. Note that the overlapping aliasing signals are not accurately canceled and therefore limit the resolution of the system.

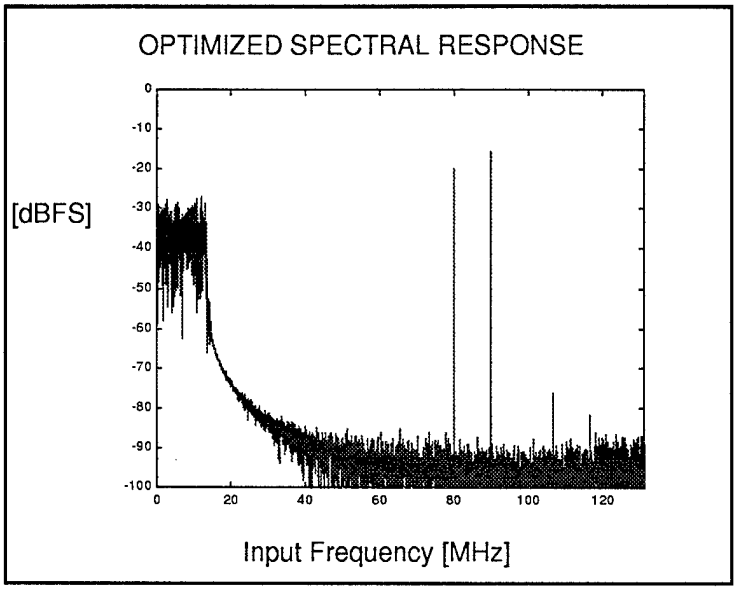

Figure 7-16. Output Spectral Response with multi-tone input for *AFB ADC* hardware (12-bit, 260 MHz) with Optimized digital Recombination Filters. Note how the Recombination Filters compensate for the mismatch errors to cancel the aliasing error signals by an additional 20-30 dB so the remaining errors do not limit the resolution of the system.

8. Conclusions

Discussion of Test Results

Table 8-1. Summary of Test Results for *AFB ADC* Hardware (12-bit, 260 MHz)

Resolution [bits]	Sample Rate [MHz]	SFDR [dB]	SNR [dB]	Analog Bandwidth
12	260	75	60	130 MHz

This project demonstrates that the ***AFB ADC*** system can be used to effectively widen the bandwidth of analog-to-digital conversion by using a parallel array of state-of-the-art converters. Test results confirm that the errors introduced by the parallel architecture can be accurately canceled in the system output so that they do not limit the resolution of the system (unlike conventional parallel approaches such as Time-Interleaving). The alias error cancellation was confirmed for single-tone test signals as well as more complex multi-tone and pseudorandom test signals.

In general, the ***AFB ADC*** architecture neither degrades nor improves the dynamic range and signal-to-noise ratio performance of the individual converters in the array. The ***AFB ADC*** architecture was used to quadruple the bandwidth without limiting the resolution. The marginal performance improvements seen in the prototype's SFDR and residual error testing can be attributed to circuitry improvements implemented in the prototype hardware compared to the relatively inexpensive Analog Devices evaluation board used to test the devices at the beginning of the project.

Even though the investigation of linearity correction techniques was not a part of this project, it is worth noting that the use of such approaches (such as the V Company ***LinComp*** algorithm) can improve the dynamic range of the system by compensating for harmonic and intermodulation distortion, especially for frequencies above 100 MHz where the SFDR of the individual ADCs in the array is degraded. Such linearity correction can insure full 12-bit dynamic range across the entire 130 MHz bandwidth of the system.

Phase I - Demonstrate high performance of *AFB ADC* via hardware breadboarding

The objective of the Phase I project was to verify the significant performance improvements afforded by the ***AFB ADC*** architecture by demonstrating a system design procedure and building and testing a pre-prototype breadboard implementation of the front-end electronics of a 12-bit ***AFB ADC*** system with 260 MHz sample rate (four times the speed of state-of-the-art, commercially-available 12-bit ADCs). This objective has been fulfilled.

Phase II - Test *AFB ADC* Architecture in Navy AMFRFS Testbed

The proposed Phase II effort will be dedicated to the development of ***AFB ADC*** hardware for integration in the Navy Advanced Multi-Function RF System (AMFRFS) testbed, which is being used to develop the AMFRFS system. V Company will be corresponding with the testbed engineers to develop a Phase II proposal for an ***AFB ADC*** design suitable for their testbed requirements.

Phase III - Customization and integration into radar systems and RF receivers

Phase III will involve the customization and integration of the ***AFB ADC*** in the next generation of high-performance radar systems and RF receivers via commercial and military contracts to build the requisite hardware. Eventually, V Company will leverage its base of very high-performance mixed analog and digital products to build systems (such as radar receivers, universal communications receivers, and specialized test equipment).