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13. ABSTRACT (Maximum 200 words) The purpose of this research was to determine the expected yields and bit error rates of HTS digital circuits operated at tens of gigahertz at various temperatures. This was done by using device parameters from TRW, Conductus, and Northrup Grumman for state-of-the-art devices. The circuits studied included two rapid-single-flux-quantum (RSFQ) T flip-flop circuits. One (with 14 Josephson junctions) included estimated undesirable parasitic inductances and other was assumed free of parasitics. We also analyzed a three-stage counter made of a cascade of the T flip-flops with parasitics with 38 junctions. We conducted Monte Carlo simulations and evaluated the bit-error rates (BER) at various temperatures. Yield calculations were made for operation at a number of multi-gigahertz frequencies. For higher frequency operation, the results improved strongly with higher assumed products of critical current and normal-state resistance (IcRn). For 50 GHz operation with IcRn = 0.5 mV, we compared the yield for a T flip-flop with that of the three-stage counter (70% vs. 34%). Bit-error-rate calculations suggest that operating temperature must be <20-30 K for a BER <10 ⁻⁶ .				
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ANALYSIS OF ULTRA-HIGH-SPEED, HIGH-TEMPERATURE SUPER-CONDUCTOR (HTS) DIGITAL CIRCUITS P.I.: T Van Duzer

The purpose of this research was to determine the expected yields and bit error rates of HTS single-flux-quantum digital circuits [1] operated at tens of gigahertz at various temperatures. The issues are: how large can a circuit be and how high an operating temperature can be used and still get adequate yield at a significant operating speed. This was done by using device parameters from TRW, Conductus, and Northrop Grumman.

Our study had several components: (1) introduction of subprograms into the very high speed simulation program WRspice [2] to provide the special features required for this project; (2) Monte Carlo noise-free simulations; (3) development of techniques for introduction of calibrated noise into all the resistive components in the circuit; (4) Simulations including the effect of noise in order to estimate the bit-error rates (BER) as a function of operating temperature; (5) preliminary calculations introducing noise effects into Monte Carlo calculations to evaluate bit-error rates.

It was agreed by the industry sources that we should assume zero global spread for some parameters because the chips will be selected to give the right device resistance (R_n) value and temperature will be adjusted to give the nominal critical current I_c . This obviously biases the yield data to be more favorable than the overall yield of a manufacturing process but was considered appropriate in view of the embryonic state of the technology. We did include chip-to-chip global inductance variations with standard deviation of 15%. The on-chip spreads (standard deviations) entered into the Monte Carlo program for the HTS circuit parameters are those shown in the table below. These are the values agreed to by our industrial information sources.

Local variations of circuit parameters

	J_c	$I_c R_n$	L	R
Standard deviation	10%	5%	15%	4%

Two rapid-single-flux-quantum (RSFQ) T flip-flop circuits were studied. One was designed and tested at TRW (at 40 K) and included estimated parasitic inductances that unavoidably appear in making the layout, and are undesirable [3]. It contained 14 Josephson junctions. We also analyzed a similar circuit designed at Conductus, Inc. which was taken to be free of parasitics. Comparison of these results permitted seeing the effect of the

parasitics on performance. In a qualitative way it is a *a priori* obvious that parasitic inductances, even when taken into account in the optimization, will worsen the performance. This is because they appear in series with the Josephson junctions, which are nonlinear inductances; the effect of the useful nonlinearity of the Josephson junction is weakened by the series linear inductance. As a quantitative example, the yield for the T flip-flop with $I_c R_n = 0.5$ mV without parasitics at 50 GHz is 83% but only 71% with parasitics. Without parasitics, the yield is nearly constant at least up to 50 GHz. (These calculations did not include noise effects.) [4]

We also studied a 3-stage counter including parasitics; the circuit is a coupled set of three T flip-flops and included 38 Josephson junctions. The yield results obtained from noise-free Monte Carlo calculations, assuming $I_c R_n = 0.5$ mV, and 50 GHz clock rate were 70% for the T-flip flop and 34% for the 3-stage counter. One consideration in calculating yields is to assure that the SFQ pulses at the circuit output have not been delayed or advanced by the random selection of parameters by so much that they fall in the wrong clock period. Taking this into account led to a reduction of yield by several percent in these circuits at the higher frequencies (where the periods are shorter).

In order to address the question of the highest usable operating temperature, we incorporated thermal noise into the WRspice Josephson SPICE simulator. To do this, random-current sources were introduced in parallel with resistors using a gaussian random number generator. A number of tests were made to confirm the accuracy of the algorithm. The noise rounding of Josephson junction I-V characteristics was calculated by means of simulations using the modified WRspice program and was verified by comparison with earlier theoretical and experimental studies [5]. We also simulated a basic RSFQ comparator consisting of two Josephson junctions in series, with the experimental parameters given by Phillipov et al. [6]. The calculated result was in excellent agreement with the experiment with no fitting parameters.

We introduced noise in WRspice to make estimates of bit-error rates. A rate of less than one error in 10^9 periods ($BER < 10^{-9}$) is required in most circuit applications. Unfortunately, a calculation of a circuit's operation for long enough to see an error if the $BER = 10^{-9}$ would require many days of computation. Our procedure, therefore, was to simulate a temperature high enough that the bit error rates were much larger, say $> 10^{-6}$ and then extrapolate the results to estimate the BER at temperatures of interest. We applied this approach to the T flip-flop with and without parasitic inductances. With $I_c R_n = 0.25$ mV and in the absence of parasitics, it appears that $BER < 10^{-6}$ with $T = 40$ K even with clocking frequencies as high as 100 GHz (there is little frequency dependence in the range < 100 GHz) for which the circuit is designed). However, the result is worsened by at least an order of magnitude if the parasitic inductances are taken into account. There is some improvement

with higher $I_c R_n$ products. One should combine Monte Carlo and noise calculations. But 50 or more runs are needed for Monte Carlo calculations and they must be long runs for noise analysis. The average BER calculated for the ideal T flip-flop without parasitic inductances at 50 GHz is approximately doubled when spreads are taken into account. Overall, we estimate that operating temperature may need to be as low as 20-30 K to get $BER < 10^{-6}$.

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[2] For more information on WRspice contact S. R. Whiteley, Email: stevew@srware.com, Phone: (408) 735-8973, FAX: (408) 245-4033.

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