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Standard Form 298 (Rev. 8-98)
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NexGenBus Simulations

Details a Modeling and Simulation
effort for the Next Generation
Instrumentation Bus (NexGenBus)
Program

Simulation Overall Objectives

- Simulate Fibre Channel Topologies
- Simulate Message Latency and Throughput
- Simulate effect of Upper Layer Protocols
- Simulate different Classes of Service
- Simulate Synchronization

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Simulation Method

- Generate Network Modeling and Simulation Plan
- Develop Baseline Model
- Build Lab Network
- Perform Verification on Baseline Model
- Document Initial Simulation Results

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Simulation Method (cont'd)

- Generate Expanded Model Capabilities and Assumptions Document
- Build Small, Medium (today's max) and Large (tomorrow's max) Simulations
- Document results of Small, Medium and Large Simulations

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Baseline Model

- Demonstrate the ability to produce model that matches the performance characteristics of a duplicate lab network

- FXLP protocol simulation in each transaction

- Fibre Channel data link uses vendor specifications

Lab Network

- Lab consists of two Pentium PC's
- NT 4.0
- Systran PCI card with FXLP drivers
- Twinax wires PC to PC
- Visual C++ program

Initial Model Results

- All file transfers performed 1000 times for statistical averages
- Simulation and Lab test throughput match within 5%
- Fibre Channel link not utilized over 50% during any of the file transfers
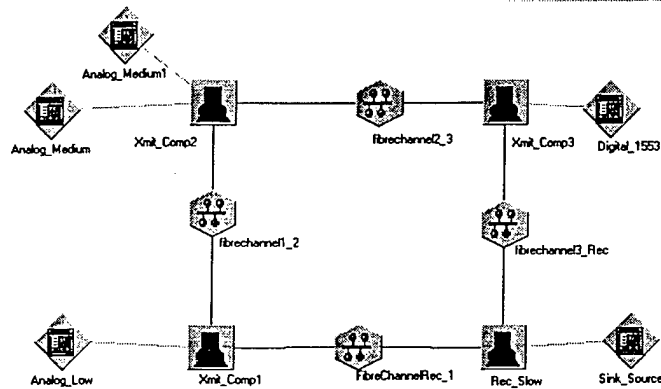- Simulation and Lab message latencies match up to the 200Kbytes file size

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Expanded Models

- Objective is to build on initial model to simulate small, medium and large NexGenBus Instrumentation system
- models consist of sources and sinks
- Models do not simulate at the physical or data encoding layer
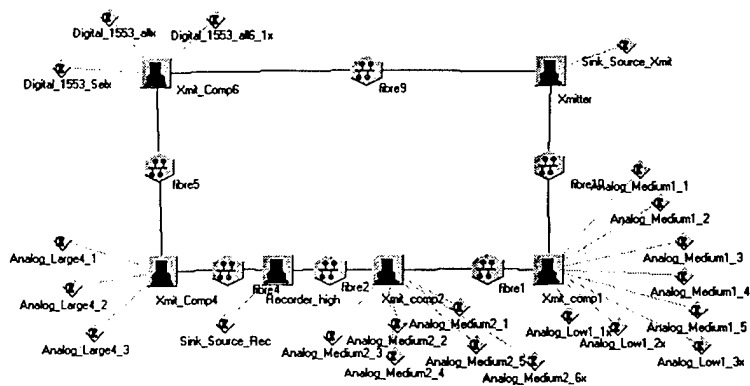- TCP/IP lab network tested

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Small Simulation

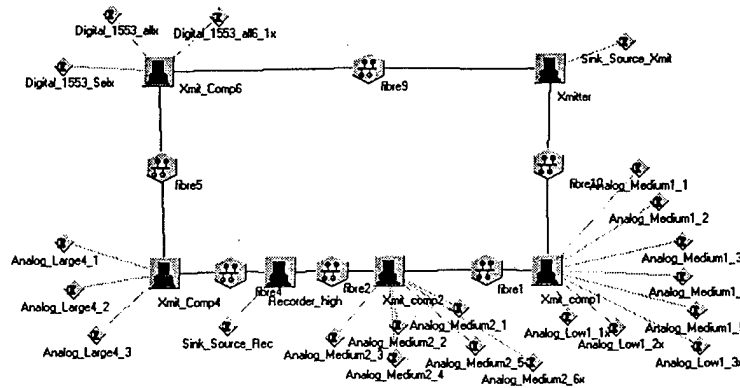Analog_Medium1
Analog_Medium
Xmit_Comp2
fibrechannel2_3
Xmit_Comp3
Digital_1553
fibrechannel1_2
fibrechannel3_Rec
Analog_Low
Xmit_Comp1
FibreChanneRec_1
Rec_Slow
Sink_Source

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Medium Simulations

Digital_1553_allx Digital_1553_all6_1x
Digital_1553_Sebr
Xmit_Comp6
fibre9
Sink_Source_Xmit
Xmitter
fibre5
fibreAAnalog_Medium1_1
Analog_Medium1_2
Analog_Large4_1
Analog_Medium1_3
Analog_Large4_2
Analog_Medium1_4
fibre4
fibre2
fibre1
Analog_Large4_3
Xmit_Comp4
Recorder_high
Xmit_comp2
Xmit_comp1
Analog_Medium1_5
Analog_Medium2_1
Sink_Source_Rec
Analog_Medium2_2
Analog_Low1_1x
Analog_Medium2_3
Analog_Low1_2x
Analog_Low1_3x
Analog_Medium2_4
Analog_Medium2_5
Analog_Medium2_6x

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Large Simulations

Expanded Model Results

- Talk about noticeable delay for small, medium and large models
- No topology changes on small, medium and large models
- class of service effects on small, medium and large models
- TCP/UDP/IP ULP discussions