SMC-TR-00-09

AEROSPACE REPORT NO.
TR-95(5925)-6

Correlation of Picosecond Laser-Induced Latchup and Energetic Particle-Induced Latchup in CMOS Test Structures

15 March 2000

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This report was submitted by The Aerospace Corporation, El Segundo, CA 90245-4691, under Contract No. F04701-93-C-0094 with the Space and Missile Systems Center, 2430 E. El Segundo Blvd., Los Angeles Air Force Base, CA 90245. It was reviewed and approved for The Aerospace Corporation by B. Jaduszliwer, Principal Director, Electronics and Photonics Laboratory; and A. B. Christensen, Principal Director, Space Science Applications Laboratory. Michael Zambrana was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

Michael Zambrana
SMC/AXE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 March 2000	

4. TITLE AND SUBTITLE
Correlation of Picosecond Laser-Induced Latchup and Energetic Particle-Induced Latchup in CMOS Test Structures

5. FUNDING NUMBERS
F04701-93-C-0094

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
The Aerospace Corporation
Laboratory Operations
El Segundo, CA 90245-4691

8. PERFORMING ORGANIZATION REPORT NUMBER
TR-95(5925)-6

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Space and Missile Systems Center
Air Force Materiel Command
2430 E. El Segundo Boulevard
Los Angeles Air Force Base, CA 90245

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
SMC-TR-00-09

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

We show that the thresholds for picosecond (psec) laser pulse-induced latchup and energetic particle-induced latchup are well correlated over a range of bulk CMOS test structures designed to be susceptible to latchup. The spatial length of the latchup-sensitive node of the test structures covers a range of values that commonly occur in bulk CMOS devices. The accuracy of this correlation implies that laser-induced latchup can be used for hardness assurance and, under the proper conditions, can be an accurate predictor of latchup threshold linear energy transfer (LET) for most bulk CMOS devices.

14. SUBJECT TERMS
Single event latchup, CMOS, Picosecond

15. NUMBER OF PAGES
18

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	

Contents

Figures

Tables

1. Introduction

Some microelectronic devices are sensitive to latchup, i.e., an anomalous current path produced between npn or pnp structures that will only disappear if all power is removed from the device.[1] Latchup can be induced in these devices by a variety of mechanisms, including the passage of ionizing radiation (such as that encountered in the space environment) through the device.[2,3] Once initiated, the currents produced can be much higher than those encountered in normal operation, causing catastrophic failure, performance reduction, or reliability reduction. Modern device design techniques can reduce the potential for latchup, but cannot eliminate the possibility for many device technologies. Consequently, many devices to be used in the space environment, including all bulk CMOS devices, must be tested for their susceptibility to radiation-induced latchup. These tests have traditionally been performed using energetic particles produced at accelerators such as the Lawrence Berkeley Laboratory 88-inch cyclotron, and latchup susceptibility has been characterized in terms of linear energy transfer (LET). Recently, however, picosecond (psec) laser pulses have been used to induce single-event phenomena (SEP) such as high-voltage transients, single-event latchup (SEL), or single-event upset (SEU) in microelectronic devices.[4–16]

Laser-based simulation of SEP has several advantages over particle-beam-based measurements. Using laser-based techniques, sensitive device nodes may be located on-chip with submicron precision. Laser-based tests can be repeated many times on-chip without concern over displacement damage or oxide total dose accumulation. Device test fixtures and circuitry can be changed easily in laser-based tests; whereas, in particle-beam tests performed under vacuum, only a limited number of configurations can be tested before the test chamber must be unsealed. Laser-based testing allows diagnostic equipment to be located very close to the device under test, facilitating evaluation of high-speed device response; whereas, during particle-beam testing, some equipment may have to be located many meters away.

However, objections to laser-based simulations of SEP have persisted because: (1) laser light cannot penetrate metallization as particle-beams can, (2) no correlation has been shown between particle-beam and laser-pulse thresholds for SEP scaled with device geometry, and (3) there are clear differences between the microscopic physical effects that occur during excitation of microelectronic devices with laser pulses or with energetic particles. These differences have been explored in some detail elsewhere[7,18] and will not be repeated here. Simulation of energetic particle-induced SEL with psec pulses of light has proven of benefit in several recent studies on commercially available components. Nonetheless, because of the differences in the microscopic physics associated with laser-beam-induced and particle-beam-induced phenomena, questions have recently arisen as to the practicality of using psec laser pulses to simulate particle-beam-induced SEP.[17] These focus upon the essential issue of whether or not laser-induced SEP can be shown to scale with or correlate with particle-beam-induced SEP. Although some of the studies referenced here have reported correlations between laser-induced and particle-beam-induced SEP, the measurements have usually been performed across variations in device fabrication technologies as well as variations in device dimensions.[6,12] Here, we describe results of laser-induced SEL and particle-beam SEL tests performed on

bulk CMOS test structures designed to be susceptible to SEL. We show that the laser pulse energy thresholds for laser-induced SEL correlate well with the LET thresholds for particle-beam SEL over a range of a single device design parameter that is sensitive to SEL.

2. CMOS Test Structures

A cross-sectional view of the CMOS latchup test structures is shown in Figure 1a, and a photograph from the top is shown in Figure 1b. The devices were fabricated using the commercial MOSIS (non-radiation hard) process. The devices consist of n-wells in p-type silicon containing a single n+ contact and a single p+ source/drain. This forms a vertical pnp transistor. A single n+ source/drain region is then placed near the n– well. The closeness of this placement tends to enhance the latchup sensitivity of the structure. There is also a p+ substrate contact adjacent to the n+ source/drain which serves as the base contact for the lateral npn parasitic transistor. The n– well and all the n+ and p+ implants are arranged as parallel stripes 65 μm in length. The separation between the edge of the n– well and the n+ source/drain region was 4, 5, 6, 7, and 9 μm. The CMOS design rule for this process specifies a minimum separation of 5 μm. Thus, the design rule was bracketed by larger and smaller spacings. The parasitic nature of these transistors is enhanced in close proximity, and they make an ideal latchup test structure. Laser beam testing, in contrast to particle beam testing, can identify the most vulnerable SEL pathway. The metallization pattern consists of four L-shaped lines, each connected to a 75 μm square contact pad.

The metallization is aluminum with 10 μm line widths. The long portion of the four L-shaped lines are parallel to each other. The separation between the metal lines connected to ground is 3 μm. The separation between the metal lines connected to V_{DD} is 3 μm. The p+ and n+ regions forming the contact points were rectangular with dimensions of 65 μm by 6 μm. The large n-well is rectangular with dimensions of 65x25 μm. The large n-well is 2 μm deep and phosphorus doped to a concentration of ~ 10^{17} cm^{-3}. The mask spacing between the edge of the large n-well and the n+ contact outside the n-well was 4, 5, 6, 7, or 9 μm. The actual spacing is somewhat less (≈ 1 μm) due to lateral diffusion of the n-well implant. This set of structures thus allows characterization of the spatial dependence of the lateral pnpn region that forms the parasitic latchup path in CMOS devices. The p+

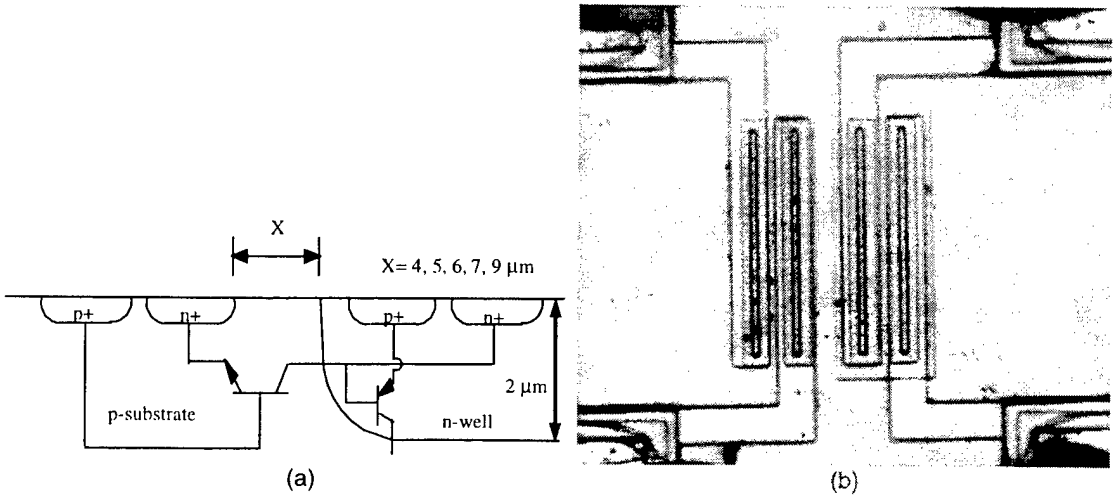


Figure 1. CMOS latchup test structures. (a) Cross-sectional view; (b) photograph of top view.

source/drain and p+ body tie contacts were boron doped to ~10^{20} cm^{-3} to a depth of 0.3 μm. The p– substrate dopant concentration was ~10^{16} cm^{-3}. The n+ source/drain and n+ well tie were arsenic doped to ~10^{21} cm^{-3} to a depth of 0.2 μm. The devices were susceptible to latchup if over-voltages were applied and, as described below, also latched up under the influence of psec pulse excitation or energetic particle excitation. The devices were also extremely susceptible to damage during latchup if not current-limited. These devices are structurally similar to a test structure with a 10-μm spacing between the edge of the n– well and the external n+ source/drain contact used previously to compare laser-induced and particle-beam-induced latchup.[5]

It was found that the test structures could be latched up readily using either heavy ions or laser pulses. If connected across a stiff power supply, the structures would be rapidly burned out since the currents rose to high values. To prevent this occurrence, we used a capacitor charged to the 5-V power supply voltage to provide the latchup current. The current was limited with a total series resistance of 1 kΩ, and the circuit discharge time constant was approximately 100 μs. The circuit shown in Figure 2a was used for the tests of the 5, 6, 7, and 9 μm devices to limit the current felt by each device during SEL and thus prevent permanent damage caused by the high latch currents. This test fixture essentially replaced the unlimited current from the power supply with current from the capacitors. The larger capacitor, C_2, supplied the charge, while the smaller capacitor, C_1,was a high-frequency bypass capacitor. When driven into latchup, the CMOS test structures would draw enough current to rapidly pull down the charge on the capacitors. After the discharge current of the capacitors fell below the holding current, the CMOS test structure fell out of latchup. The transient SEL waveforms were measured across R_5. The 4-μm devices were "punched through" at the nominal applied biases with the test structure shown in Figure 2a. A slightly different test circuit shown in Figure 2b was used for the punched through structure with n– well to n+ separation of 4 μm.

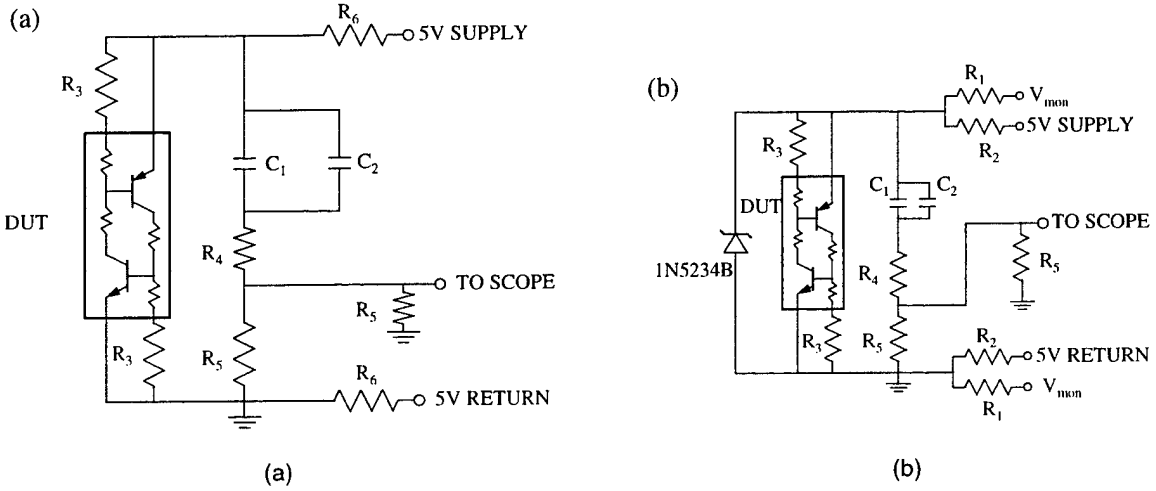


Figure 2. Test circuits for CMOS latchup test structures. (a) 5, 6, 7, and 9 μm devices; (b) 4 μm devices. R_1=10KΩ, R_2=2.5KΩ, R_3=10Ω, R_4=75Ω, R_5=50Ω, R_6=1.0KΩ, C_1=0.001μF, C_2=1.0μF.

Although the lateral npn transistor is punched through, it still exhibits bipolar transistor action if base current is supplied. Therefore, it was biased using a current source adjusted to provide a DUT operating voltage of 2.5 V, the largest voltage that could be maintained across it without inducing the latchup with avalanche breakdown. The current source was formed using a large-value charging resistor (20 kΩ total). The punch-through current in the DUT was approximately 4 mA at the DUT voltage of 2.5 V. The 1N4234B is a 6.2-V Zener diode to prevent an overvoltage condition in case of a fault, and is normally non-conducting. This circuit produces the same latchup waveforms as that of Figure 2a.

The sensitivity of all of these devices to SEL was tested using particle-beam excitation as well as laser-beam excitation, as described below. The same test fixtures were used for both the particle-beam and laser-induced SEL measurements. Prior to the laser-beam or particle-beam SEL measurements, all of these devices were characterized with a curve tracer to map out their current-voltage characteristics. All of the devices displayed current-voltage characteristics with the S-shaped characteristic typical of latchup.[1] The trigger voltages at the supplied lateral npn base currents are listed in Table 1. The measured values fall within the normal range for CMOS structures of this type. The vertical pnp transistors had a ""beta" of ~6.7 measured at a collector current of 300 μA and a collector voltage of 5 V. The lateral npn betas were measured under these same conditions and had the betas shown in Table 1. Also, the triggering was achieved by applying current to the lateral npn base. Note that the product of these two betas exceeds unity by a significant fraction; however, the beta measurements are made at very high currents compared to normal operation in CMOS circuits. There, the currents are nA or less, and the betas are very much smaller than 1. However, under the right excitation, the currents can be brought much higher into the realm where the beta product is greater than 1, and then latchup occurs.[1]

Table 1. Trigger voltage and base current for the CMOS latchup test structures.

Well Separation (μm)	V_{trig} (V)	I_{base} (mA)	Lateral npn β
4	1.00	4	∞ (punched through)
5	1.15	4	18.5
6	2.05	4	10.6
7	2.10	6	8.0
9	4.50	8	5.3

3. Laser Measurements

3.1 Laser Apparatus

The equipment used to perform the laser measurements is shown in Figure 3. A Rhodamine 6G dye laser operated in a cavity-dumping mode is synchronously pumped by the output of an actively mode-locked, frequency-doubled Nd:YAG laser. The dye laser output parameters were: (a) 600 nm wavelength, (b) 180 mW average power, (c)10 ps temporal optical pulse duration (FWHM of Intensity), and (d) 5 MHz pulse repetition rate out of the dye laser. An electro-optic shutter (EOS) was used to reduce the repetition rate of pulses incident upon the device. The measurements described in this report were performed with the EOS operated in the single-shot mode. In single-shot mode, the pulse train from the cavity-dumped dye laser is rejected from the shutter until a switch is thrown that allows a single optical pulse to pass. After the EOS, a small portion of the beam was directed by a beamsplitter in front of the periscope to a fast silicon PIN photodiode, PD. The transient electrical response of the PIN photodiode was monitored on a shot-to-shot basis using a digital storage oscilloscope. The photodiode was operated in a bias regime such that the amplitude of the electrical response was linearly proportional to the optical pulse energy. The dye laser beam was then attenuated and passed through a periscope incorporating a microscope so that the laser beam could be focused onto the sample. A 50x microscope objective with 13.5-mm working distance allowed the laser beam to be focused to a spot size of less than 2 μm on the device. A dye laser mirror was used in one portion of the periscope to allow incoherent light from a white light source to illuminate the sample colinearly with the laser beam. A second glass beamsplitter in the periscope allowed the image of the illuminated sample to be viewed through an eyepiece or imaged onto a CCD camera. Pictures of the illuminated portion of the device were obtained from the CCD output with the aid of a

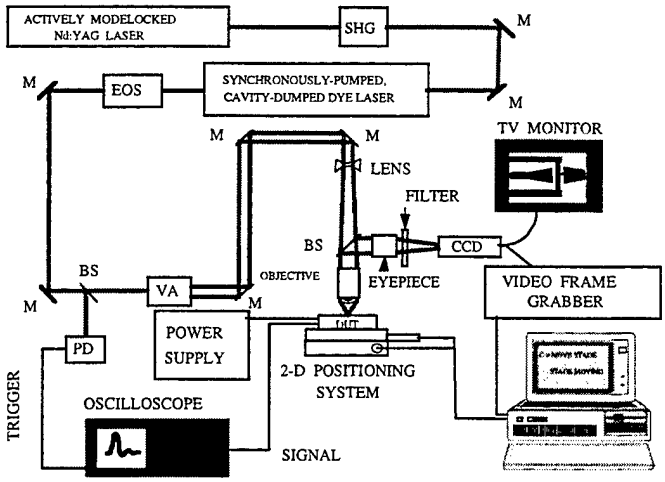


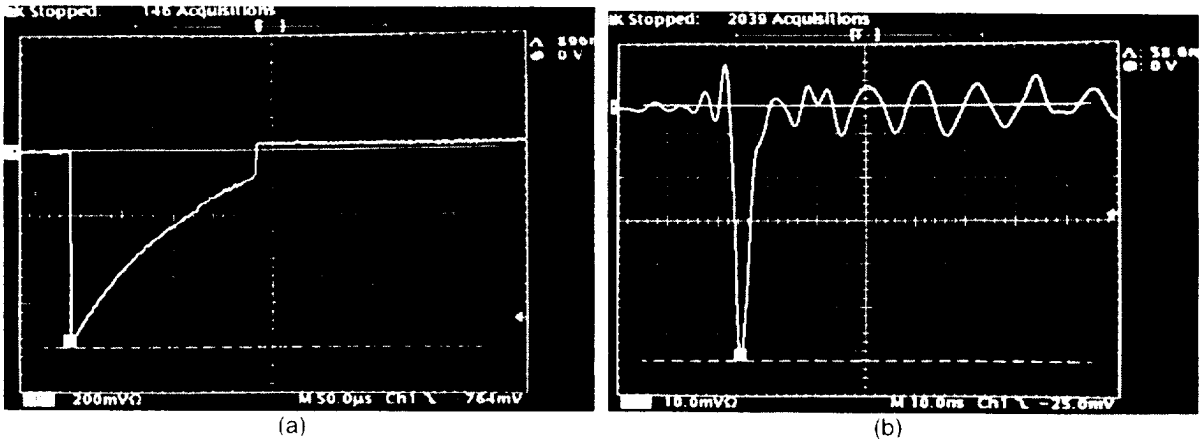
Figure 3. Laser system and apparatus for producing psec laser-induced latchup. BS - beamsplitter, EOS - electro-optic shutter, M - mirror, PD - photodetector, SHG - optical second harmonic generating crystal, VA - variable optical attenuator.

frame-grabber. The field of regard of the system was ~100 μm, limited by the region illuminated by the white light source. Control of the focusing of the image and the laser beam was accomplished independently with the aid of a lens located just prior to the periscope. The optical imaging system was held fixed and the device under test was moved laterally through the focused laser beam. The device was mounted on a positioning system consisting of two one-inch travel translation stages mounted together so that their motion was along orthogonal axes. The position of the device was controlled using a two-axis, computer-controlled, micro-positioning system with a repeatability of 0.1 μm.

Test structure reflectivity was measured by replacing the CCD with a photodetector and measuring the ratio of the signals on the photodetector that monitored the incident light with that monitoring the reflected light. Comparison of this ratio for the test structure with that of a 100% reflector yielded the test structure reflectivity. For these devices, little variation in reflectivity was observed from device-to-device or from site-to-site on a device.

3.2 Laser Results

The most sensitive region of the CMOS test structures to optical pulse-induced SEL was the center of the devices, between the two center metallization lines. A typical laser-induced SEL waveform is shown in Figure 4a for excitation of the 5-μm device with a 270-pJ laser pulse, i.e., well above the threshold for laser-induced SEL. The polarity is negative since current flows out of the capacitor during latchup. The falling edge of the SEL waveform was synchronous with the incident laser pulse. There is some structure on the falling edge of this waveform, not resolved on this time scale, that indicates very complex phenomena occur within a very short time of absorption of the psec laser pulse. We have not, as yet, performed a careful set of measurements of these early time transients. After the waveform reaches its minimum value, the current begins to decline as the charge held in the capacitors is drawn down. After 180–190 μs, determined by the test fixture RC time constant, the current falls below that needed to sustain latchup. When the DUT voltage drops below the holding voltage of the test structure, the output voltage abruptly reverses in polarity as the slow charging current from the 1-kΩ resistors replenishes the capacitor charge. This waveform, shown in Figure



(a) (b)

Figure 4. Transient laser-induced waveforms. (a) SEL - Scale: y-axis = 200 mV/div; x-axis = 50 μs/div ; (b) transient - Scale: y-axis = 10 ns/div, x-axis = 10 mV/div.

4a, is characteristic of latchup for these CMOS test structures in this test fixture. Any laser shot that produced this type of waveform was deemed to have driven the device into latchup. At lower pulse energies, transient waveforms such as that shown in Figure 4b for excitation of the 5-μm device with a 8-pJ laser pulse, i.e., just below the threshold for laser-induced SEL, indicated that the laser pulse energy was not sufficient to drive the device into latchup. The device response is initially of positive polarity, followed rapidly by a 2–3-ns-wide transient of negative polarity, and then by ringing at longer times. The results of laser excitation at the most sensitive region are shown in Figures 5a–d for the 5, 6, 7, and 9 μm devices, respectively. These graphs show, as a function of absorbed laser pulse energy, whether or not the device latched up on a given laser shot. As can be seen from these graphs, the devices do not latchup for energies below a value E_{NL}. However, at laser pulse energies above a value E_L, the devices latchup with every laser shot. At intermediate laser energies between E_{NL} and E_L, the devices go into latchup only some of the time. This uncertainty in latchup threshold can be partly tied to measurement limitations such as the uncertainty in referencing the fast photodetector to the optical power meter. We estimate that the uncertainty in our laser pulse energy measurements is ±5%. However, in general, the separation between E_{NL} and E_L is larger than the uncertainty in optical pulse energy. This may be due to an instability such as those found in other highly nonlinear optically induced feedback phenomena wherein the final state of the device is a critical function of the initial state. Relatively small fluctuations in applied bias or device temperature (i.e., fluctuations below the limits that can easily be controlled with state-of-the-art power supplies) may

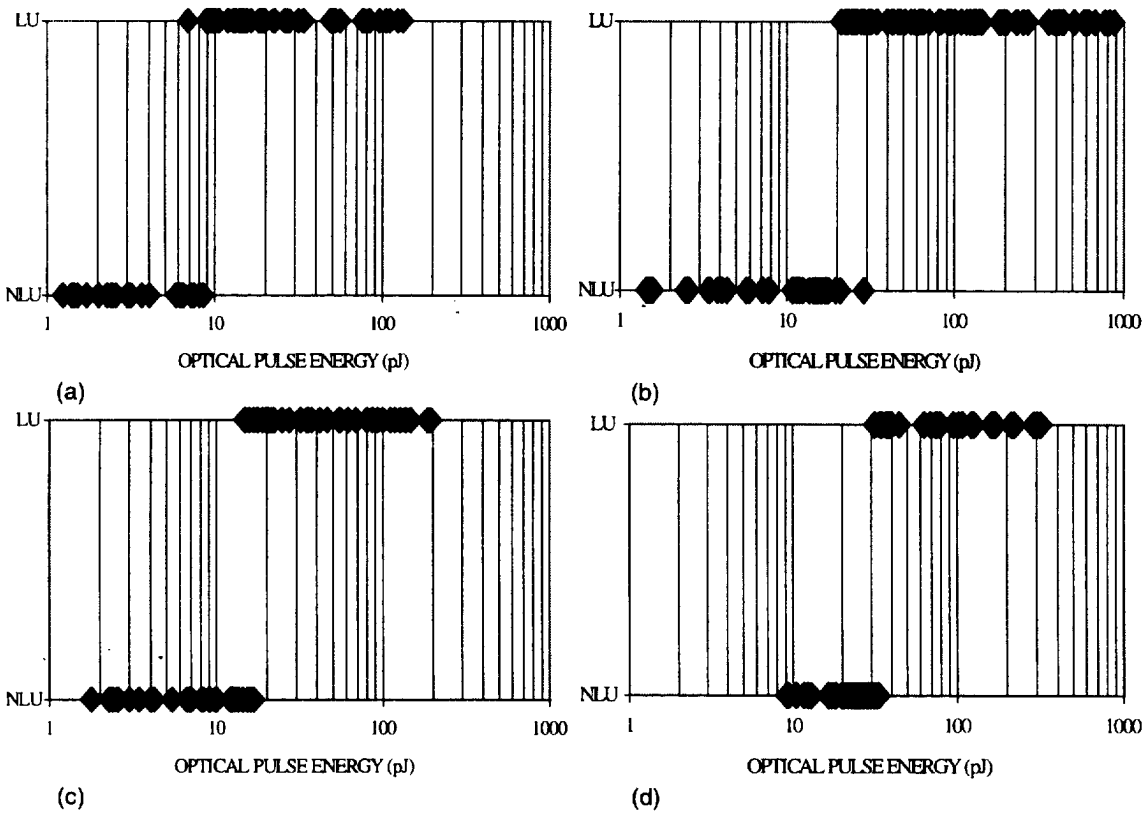


Figure 5. Laser-induced latchup threshold (the energy axis indicates deposited energy): (a) 5-μm device, (b) 6-μm device, (c) 7-μm device, and (d) 9-μm device. LU - device latched on excitation, NLU - device did not latch upon excitation.

produce these instabilities. We defined the latchup threshold as the median point between E_{NL} and E_L, i.e., as many shots above E_{TH} as below E_{TH} within the region between E_{NL} and E_L. Clearly, from Figures 5a–d, the latchup threshold increased with increasing separation.

The results of laser excitation at the most sensitive region of the 4 μm device are shown in Figure 6. The device was biased at 2.4 V for these measurements because it was punched through at the nominal 5 V bias used for the other devices. Also, as described above, the test fixture shown in Figure 2b was used for this device rather than the one shown in Figure 2a. The laser-induced latchup result for the 4 μm device shows that it requires the least optical energy to excite into latchup. This result is at least consistent with the set of measurements displayed in Figure 5a-d for the other devices in that the trend toward smaller laser thresholds with smaller well separation is maintained. However, because the 4 μm device was punched through at the 5 V applied bias and because of the differences in test fixtures, it may not be valid to correlate latchup thresholds throughout the entire group of devices. Finally, we note that repetitive excitation of these devices in excess of 1 kHz rates yielded latchup threshold values that differed from the single shot measurements. This could be due to heating phenomena due to the high currents generated by SEL and the short interpulse time or it could be due to an incomplete recovery of the current during the interpulse time. Caution should be exercised when performing SEL tests at even moderately high repetition rates to avoid errors due to incomplete recovery of the device, whether of thermal or of electronic origin.

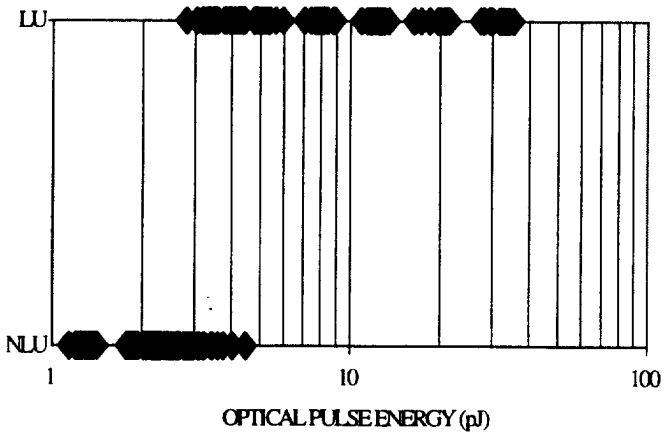


Figure 6. 4-μm device laser-induced latchup threshold.

4. Particle Beam Measurements

4.1 Apparatus

The SEL tests were carried out at the Lawrence Berkeley Laboratory 88-in. cyclotron using the ions listed in Table 2. The ion beam delivery, analysis, and exposure techniques are identical to those used for other SEU testing, and, therefore, can be found in previously published technical literature.[19,20] The beams of ions in Table 2 were chosen for their LET range and for the special property that when mixed together in, and simultaneously extracted from, the electron cyclotron resonance ion source, they can be brought individually on target by minor adjustments in the cyclotron frequency. In effect, any one of the several beams with different LET values can be selected by the push of a button.

Values of "effective" LET intermediate to those listed in Table 2 were obtained by orienting the sample such that the ions were incident upon the device at an angle. When the incident ion is very energetic and the sensitive region is a very thin, flat volume, the charge deposited by an ion varies with sec(θ) for a wide range of incident angles. This is a reasonable approximation for our devices for small enough θ. Effective LET is calculated by multiplying the LET of the incident ion by sec(θ), where θ is the angle between the incident beam and the chip normal surface. An individual device is irradiated with a known total fluence of particles, and the total number of SELs is recorded. The SEL probability or cross section (σ) is calculated from the expression $\sigma = (N/F)\sec(\theta)$, where N and F are the number of SELs and the beam fluence, respectively.

Since the occurrence of SEL is accompanied by a dramatic increase in the device bias current, local heating is inevitable. It is, therefore, mandatory that the SEL be detected and cleared before the device has a chance to heat up. We used a circuit that performed the functions of sensing (within ≈1 μs), clearing (within ≈1 ms), and recording SEL (in a few ms). For details of the circuit, the reader is referred to the description of the same circuit used to detect latchup.[20]

Table 2. Particle beam parameters.

Ion	Energy (MeV)	LET (MeV/mg/cm²)	Range (μm)
Bi	949	95	50
Xe	603	63	50
Kr	378	41	46
Cu	290	30	45
Ar	180	15	46
Ne	90	5.6	45
N	67	3.2	55

4.2 Particle Beam Results

In the discussion that follows, "effective LET" is defined as the product of the actual particle LET and the secant of the angle of incidence relative to the device surface normal. Unless otherwise indicated, it will be assumed in the remainder of the discussion that effective LET is the same as the actual LET of a normally incident particle. In the figures that follow, the errors in the data points are typically equal to or smaller than the size of the data points themselves. Plots of SEL cross section vs LET curves for the five devices are shown in Figures 7 and 8. All data were taken with a bias voltage of 5 V, except for the 4-μm device, for which data was taken at both 2.0 and 2.4 V. At 5-V bias, the 4-μm device conducted high current without the beam, as described above.

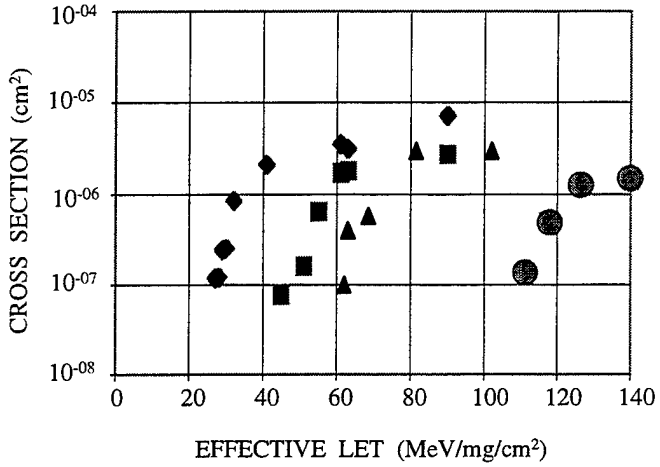


Figure 7. SEL cross section vs. effective LET for the 5 μm (diamonds), 6 μm (squares), 7 μm (triangles), and 9 μm (circles) CMOS test structures.

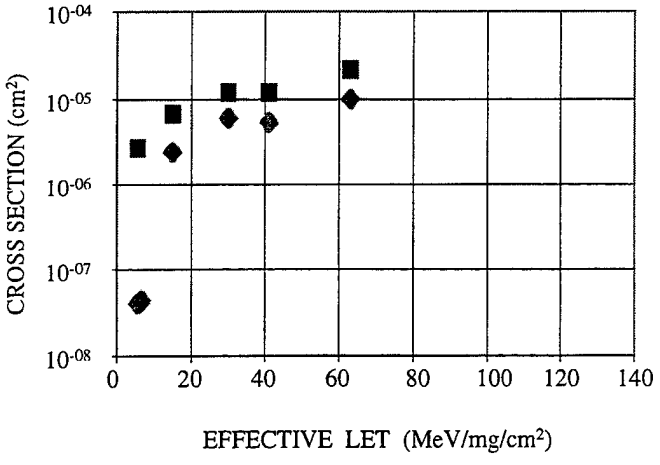


Figure 8. SEL cross section vs. effective LET for the 4 μm CMOS test structure at 2.4 V applied bias (squares) and at 2.0 V applied bias (diamonds).

5. Discussion and Conclusions

The laser pulse energy required to produce SEL in the CMOS test structures is plotted as a function of well spacing in Figure 9. On the same graph, we've plotted the SEL LET thresholds from the particle-beam measurements described above, with the relative scales adjusted to achieve the best fit. These results show that the laser pulse energy SEL threshold values scale to within an average deviation of 15% of the measured LET values. Furthermore, the total charge generated in the device by the laser pulse at the threshold for latchup also correlates with the total charge generated along the particle track at the threshold for particle-beam-induced latchup. At the laser wavelength used in these studies, the absorption of each quantum of light (of energy $E = h\nu$, where h is Planck's constant, and ν is the optical frequency) produces one electron-hole pair. The charge Q_L generated by the laser pulse is given by the absorbed optical energy E_P divided by the energy of each quantum, i.e., $Q_L = E_P/h\nu$. The total charge Q_P generated along the particle track is given by $Q_P = \text{LET} * \rho_{Si} * R/E_{Si}$ where ρ_{Si} is the density of silicon (=2330 mg/cm^3), R is the particle range (listed in Table 2.), and E_{si} is the energy required for an energetic particle to produce an electron-hole pair in silicon (E_{si} = 3.6 eV). Comparing the charge generated by absorption of the laser pulse to the amount of charge generated within the particle track, we calculate that the laser-generated charge corresponds to ≈ 33% (standard deviation ≈ ±6 %) of the charge in the particle track at threshold. The differences in charge generation necessary for latchup suggest that, at threshold, only about a third of the charge generated in the particle track is collected at the junction where latchup is initiated. We note also, as is obvious, that the psec laser light could not penetrate the metallization on the CMOS test structures, whereas the high-energy particles easily penetrate the metallization. Thus, it is possible that the most sensitive region for particle beam excitation of SEL is under the metallization and does not correspond to the position most sensitive to laser-induced SEL. Nonetheless, the strong correlation between laser-induced SEL threshold and particle-induced SEL threshold for these bulk CMOS test structures shows that the laser-induced SEL technique has substantial merit as a hardness assurance test. Furthermore, the strong correlation shows that under the proper measurement conditions, reasonably accurate prediction of absolute SEL threshold in terms of conventional figures of merit such as LET is valid for such bulk CMOS devices.

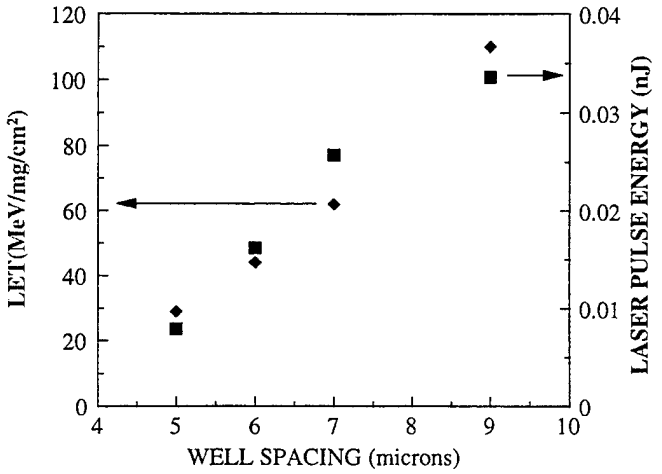


Figure 9. Correlation of laser-induced latchup (squares) and particle-induced latchup (diamonds) thresholds.

We note that latchup can be induced in these devices by excitation of either the vertical pnp parasitic transistor or the lateral npn parasitic transistor.[1] The absorption depth of the 600-nm light is ≈1.8 μm. Thus, the light can penetrate to a depth below the junction between the bottom of the n– well and the substrate. One might believe that the absorption of the light would seriously interfere with the ability to excite the vertical pnp transistor because the light intensity at the junction between the n– well and the substrate is reduced by a factor of exp(–αL), where α is the optical absorption coefficient (5445 cm^{-1} in silicon for 600-nm light), and L is the distance below the surface. For our bulk CMOS test structures, the distance L is 2 μm. For most modern bulk CMOS devices the distance L is in the range of 2–4 μm. At a depth of 2 μm, the light intensity is 34% of the intensity just below the surface, and at a depth of 4 μm, the light intensity is 11% of the intensity just below the surface. However, even though much of the charge is generated near the surface, excitation of the buried n–well/substrate junction can still occur as long as the charge generated in the n– well can drift or diffuse to the junction before significant recombination can occur. We note that the charge carrier lifetime in bulk silicon is hundreds of μs to ms,[21] while the time required to drift a distance of 2–4 μm is of the order of tens to hundreds of ps.[21] Charge carrier diffusion times over these distances are also short, on the order of a few ns. Furthermore, in our bulk CMOS test structures and also in most modern bulk CMOS devices, the distance from the surface to the buried junction is smaller than the distance between lateral n– wells. Thus, transport-initiated phenomena are often dominated by vertical transport. Consequently, excitation with the 600-nm light is capable of exciting directly the lateral npn parasitic transistor and indirectly the vertical pnp parasitic transistor. Other measurements on devices constructed on epi-CMOS have indicated that the vertical pnp transistor is the easiest to excite.[5,6] However, our laser-induced latchup measurements indicate that the region between the two central metal contacts is most sensitive to latchup, and that the laser-induced threshold is independent of excitation site within this region. This indicates that, in our devices, the lateral npn parasitic transistor is the easiest to excite. It is also consistent with our measurements of parasitic transistor gains, in which the gain of the lateral npn transistor is larger than the gain of the vertical pnp transistor for all but the 9-μm device (for which the two gain results are nearly the same). Furthermore, if the vertical pnp transistor were the easiest to excite, one would expect that the latchup threshold would be sensitive to the location of the laser beam within the central region. Finally, we note that excitation of the device within the n– well between the p+ source/drain contact and the n+ contact (represented as B in Figure 10.) also produces latchup, but at a higher threshold than excitation within the central region outside the n– well but near the p+ source/drain contact (represented as A in Figure 10.). This is inconsistent with the location of the sensitive node being under the p+ source/drain contact.

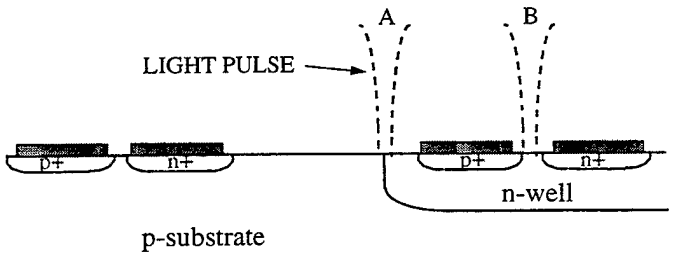


Figure 10. Laser-pulse excitation of different regions. Dashed lines - laser pulse, solid blocks - metalization.

The particle-beam cross section measurements indicate that the cross-sectional area sensitive to latchup is $\approx 1 \times 10^{-7}$ cm^2 at the latchup threshold, i.e., an area only about 3 times the area of the laser spot. However, the laser measurements indicate that the area at threshold most sensitive to laser-beam excitation is much larger. We note, in contrast to the discussion in the previous paragraph, that the difference in these cross sections may indicate that the most sensitive region of the device lies under the metallization where the laser beam cannot probe. However, the size of the region sensitive to latchup at the particle-beam threshold is so small that it may not correspond to any regular feature of the device, but to a high-field region near some hidden defect.

In conclusion, we have shown that laser-beam measurements of the SEL threshold of bulk CMOS latchup test structures correlate well with particle-beam SEL measurements. We note, however, that these measurements were only performed as a function of one design parameter, i.e., the spacing between the n– well and the n+ source/drain contact outside the n– well. Other features of CMOS devices (e.g., aspect ratio, dopant concentration, n– well depth) also affect the threshold for particle-induced latchup. Systematic studies of the correlation between laser-beam and particle-beam latchup thresholds as a function of these other design parameters will be the subject of future investigations.

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