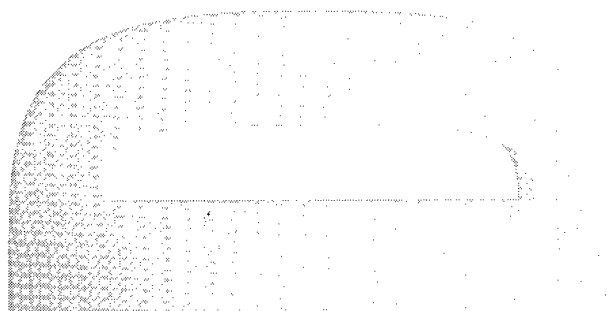
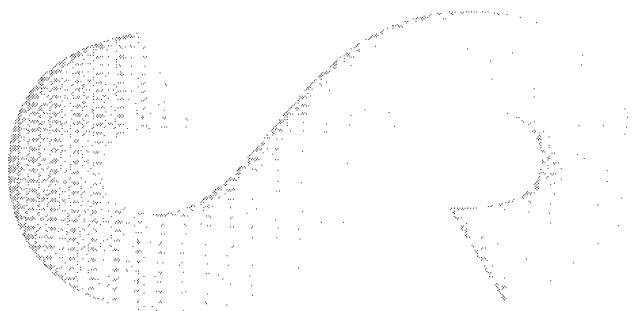
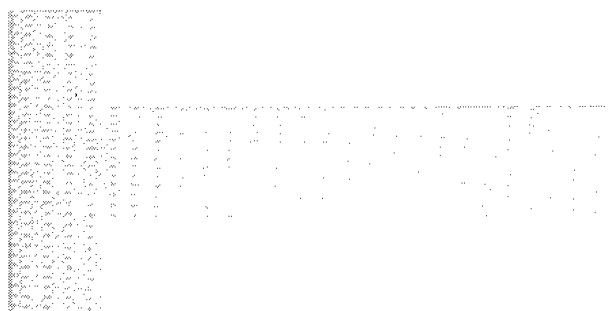
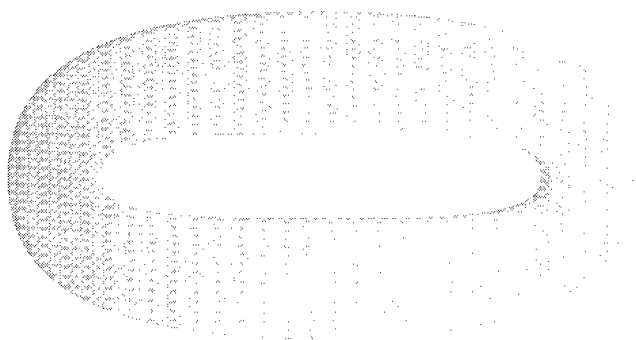




Lithium Niobate Reactive Ion Etching

Stephen Winnall and
Saul Winderbaum

DSTO-TN-0291

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Stephen Winnall and Saul Winderbaum

**Electronic Warfare Division
Electronics and Surveillance Research Laboratory**

DSTO-TN-0291

ABSTRACT

Reactive ion etching (RIE) of lithium niobate substrates has been performed using $\text{CF}_4:\text{O}_2$ chemistry. A maximum etch rate of $38 \text{ \AA}/\text{min}$ was obtained, and a deepest etch of $1.2 \text{ }\mu\text{m}$ was achieved.

The x-cut crystal orientation of the lithium niobate crystal etched more slowly than the z-cut orientation, at a ratio of 8:15.

Sidewall roughness was minimised at the expense of etch rate by increasing the oxygen flow rate for fixed CF_4 flow rate.

The achieved etch rate is suitable for low refractive index contrast devices such as integrated optical gratings or lenses. However the low etch rate is impractical for low drive voltage etched modulators.

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Lithium Niobate Reactive Ion Etching

EXECUTIVE SUMMARY

Lithium Niobate is a useful synthetic material for integrated optical devices such as wideband electro-optical modulators. Etching the Lithium Niobate can reduce the drive voltage and improve efficiency. This work was undertaken under task DST99/177.

Reactive ion etching (RIE) of lithium niobate substrates has been performed using CF_4/O_2 chemistry. A maximum etch rate of $38 \text{ \AA}/\text{min}$ was obtained, and a deepest etch of $1.2 \text{ }\mu\text{m}$ was achieved.

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1. Introduction

Lithium niobate is a useful material for many integrated optical applications. Device performance can be improved by etching the lithium niobate substrate.

Reactive ion etching (RIE) is a dry etching process in which a substrate is etched by a combination of chemical and physical interactions between the etching gas and the substrate. The etch rate and sidewall slope can be controlled by adjustment of the chemical and physical parameters in the etching unit.

We investigate in this report some of the factors which control the etch rate, sidewall slope and cross contamination of lithium and niobium when lithium niobate substrates are etched with a CF_4/O_2 chemistry.

Integrated optical devices generally have reduced scattering losses with smooth sidewalls. The sidewall slope is a parameter that is important in modelling device performance. Analysis of contaminants generated by this particular RIE process is important since contaminated RIE machines are considered unsuitable for general microelectronic processing.

Scanning electron microscope (SEM) inspection was the method used to determine etch rate and sidewall slope, and X-ray photoelectron spectroscopy (XPS) analysis was used to analyse the cross contamination levels generated by the different etch recipes.

2. Experimental Description

2.1 Preparation of Lithium Niobate Samples

The LiNbO_3 substrates were coated with a 3000 Å layer of NiCr using the RF sputter method. The coated substrates were then patterned using a photolithographic mask with AZP 4620 photoresist. The NiCr layer was sputter etched to create the NiCr RIE mask and the photoresist residual removed.

Sputter etch was the chosen technology to pattern the NiCr for two main reasons;

- An improved accuracy compared with wet etching with respect to linewidth and
- A reduced sensitivity to the NiCr layer uniformity.

2.2 The RIE Apparatus and Process

The RIE equipment used in these experiments was a Vacutec parallel plate system. The lower electrode was powered by a 13.56 MHz RF generator coupled through an automatic tuning network. A conceptual diagram is depicted in Figure 1.

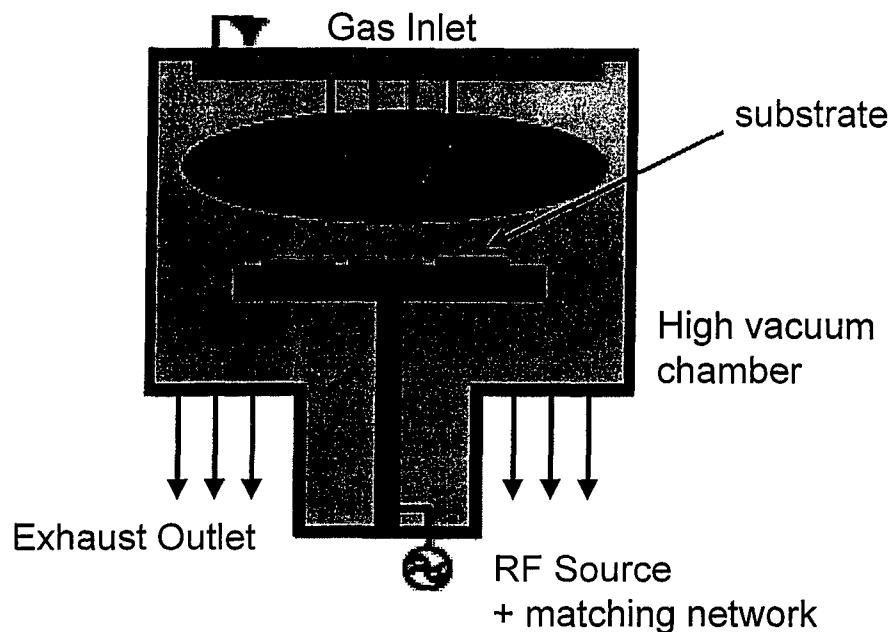


Figure 1 – RIE Conceptual Diagram

Each electrode is 200 mm in diameter and the distance between them is 23 mm. The RF electrodes are made of anodised aluminium. The chamber volume is 13 litres and the system is pumped by a 350 l/min turbomolecular pump backed by a mechanical rotary vane pump. The base pressure before each run was $< 5 \times 10^{-6}$ Torr.

The lithium niobate etch processes were performed with the test sample mounted on top of a 6 inch diameter, 1 mm thick silicon wafer. This was done in order to allow the back sputtered material to be analysed, and also protect the cathode chamber from contamination.

The angles of the sidewall and the etch rate were determined by cleaving the samples and inspecting the cross section of the etched surface with an SEM. The angle at which the substrate is measured is a source of error but it is estimated that this technique is reliable to approximately ± 3 degrees.

2.3 Experimental Matrix and Results

Table 1 shows the matrix of runs performed during this investigation.

The silicon substrates used in runs #4, #9 and #11 were subjected to XPS analysis. The results of these analyses are presented in Tables 2, 3 and 4 respectively.

Table I Experimental matrix

Run number	Lithium Niobate substrate name	Power (watt)	Pressure (mtorr)	CF ₄ flow (sccm)	O ₂ flow (sccm)	CF ₄ :O ₂	DC bias (Volt)	time (min)	etch rate (Å/min)	Etch depth (Å)
1	LN-1a	100	150	30	0	30:0	--225	30	<dl	<dl
2	LN-1b	100	150	30	15	2:1	--208	30	<dl	<dl
3	LN-1c	100	10	30	0	30:0	-312	30	<dl	<dl
4*	LN-1d	150	150	30	0	30:0	-288	30	<dl	<dl
5	LN-2a	60	10	30	0	30:0	-222	100	29	
6	LN-2b	60	10	30	10	3:1	-230	100	33	
7	LN-2c	60	10	30	20	3:2	-220	100	31	
8	LN-2d	60	10	30	30	1:1	-215	100	38	
9*	LN-3a	60	10	30	30	1:1	-208	240	Not checked	
10	LN-3b	60	10	30	30	1:1	-202	480	13.5--14.6	
11*	LN-3c	60	12-13.5	30	60	1:2	-205	380	19.2	7300
12	LN-3d	55	10	8.9	80	9:80	-205	480	13.9	6666
13	LN4a xcut	55	15	8.9	80	9:80	-189	1440	8.3	12000
14	LN4B xcut	55	15	8.9	80	9:80	-190	800	7.9	6300
15	LN5-1 z cut	55	15	8.9	80	9:80	-190	800	15.0	12000

Note:

* Runs subjected to XPS analysis

<dl denotes value less than detection level

Table 2 XPS analysis of silicon substrate from run # 4

	Sample LN 1-D					
	Atomic concentration (atomic %)					
	Under substrate	Adjacent substrate	1.8 cm from edge	1.6 cm from edge	1.0 cm from edge	0.5 cm from edge
C	15.6	22.9	18.7	21.7	18.8	17.4
O	41.4	27.7	32.0	34.8	31.1	31.4
Si	43.0	16.1	31.7	33.7	31.1	29.1
F	<dl	16.3	8.8	9.2	8.6	10.7
Al	<dl	<dl	<dl	0.6	1.7	3.6
Li	<dl	13.5	8.6	<dl	8.5	7.6
Nb	<dl	3.5	0.1	<0.06	0.1	0.05

Table 3 XPS analysis of silicon substrate from run #9

	Sample LN 3-A				
	Atomic concentration (atomic %)				
	Under substrate	Adjacent substrate	16 mm from sample	32 mm from sample	Edge of wafer
C	15.3	24.1	18.4	16.9	17.9
O	40.7	38.3	44.8	42.3	41.1
Si	43.4	31.1	33.0	37.2	36.5
F	0.6	1.2	2.8	3.4	3.8
Al	<dl	<dl	0.4	<dl.	0.6
Li	<dl	1.7	0.5	<dl	<dl
Nb	<dl	3.6	0.2	0.1	0.02

Table 4 XPS analysis of silicon substrate from run #11

	Sample LN -3C Atomic Concentration , (atomic %)					
	Under substrate	Adjacent substrate	1.8 cm from edge	1.6 cm from edge	1.0 cm from edge	0.5 cm from edge
C	16.0	22.1	18.1	19.5	19.7	19.7
O	41.2	32.6	35.2	34.0	33.2	32.8
Si	42.3	18.1	36.0	36.3	36.5	32.4
F	0.45	18.9	9.6	9.1	8.9	11.5
Al	<dl	0.6	0.2	0.5	1.6	3.5
Li	<dl*	3.5	0.5	0.5	<dl	<dl
Nb	<dl	4.1	0.1	0.1	<dl	<dl

3. Results and Discussion

As can be seen from Table I etch rates for lithium niobate were very slow, between 7.9 and 19.2 Å/min.

This magnitude of variation in the etch rate for the same process conditions and type of crystal is expected due to the time length of these runs and the method of measurement employed.

Samples from LN1 through to LN3 inclusive were not classified according to crystal orientation, and thus no information is available in these cases regarding the differences in the etching behaviour for various crystal cuts.

3.1 Sidewalls

All samples from LN2 exhibited a film on the etched sidewalls. This type of film formation is characteristic of RIE processing and one of the ways to minimise it is the increase of oxygen flow. The increased oxygen flow rate results in a higher percentage of volatile by-products from the etching reactions, which are not then redeposited on the wafer.

3.2 Lithium and Niobium Contamination

The data in Table 2 and 3 illustrates that run #4 has high detectable levels of lithium around the lithium niobate substrate as well as near the silicon wafer edge, while run #9 exhibits uniformly lower levels of lithium contaminants.

This difference is probably due to the reduction in DC bias voltage and hence in the reduction in the intensity of the physical bombardment process.

3.3 Aluminium Contamination

Aluminium contamination (originating in the bombardment of the cathode material) has been detected in all the samples measured and this is the reason DC bias was reduced from run #12 onwards.

3.4 Lithium Niobate Etch Rate

In samples LN4 and LN5, crystal orientation was specified and found that X-cut substrates had a much lower etch rate than Z-cut, at a ratio of approximately 8:15. Etch rate could have been higher if the DC bias and pressure were set at higher values. This approach however results in cross-contamination from the cathode onto the substrate itself for reasons outlined in Section 3.3.

3.5 Discussion of SEM Pictures

The SEM pictures are shown in Section 6 of this report. Figures 2 and 3 illustrate the minimal etch depths produced with conditions listed in Table 1 under the process parameters LN1-C. Figures 4 and 5 illustrate the deeper etch that was achieved for processes LN-2A and LN-2D. These figures show the smoother sidewalls resulting from an increase in the oxygen flow rate. The etch time was increased in process LN-3B which resulted in a deeper etch, but a rough film still remained. This film, which is clearly visible in Figure 6, was suspected to be due to a redeposition of material onto the substrate.

This redeposition was reduced significantly by increasing the O_2 / CF_4 flow ratio. Increasing this ratio should produce more volatile etch by-products, which do not redeposit on the wafer. This has the beneficial effect of smooth sidewalls, but also a reduced etch rate as listed in Table 1. This result is shown by the SEM pictures in Figures 7 and 8 for the x-cut and Figures 9 and 10 for the z-cut substrates.

Figure 7 also illustrates that the etching follows the shape of the mask and any variation in the device width produced by either the lithographic process or mask resolution limits will be transferred onto the final device by the RIE process. This will have limitations on the loss that can be achieved for optical devices and importantly

implies that accuracy in the lithographic process and high resolution masks are required for low-loss devices.

3.6 Conclusion

A maximum etch rate of 38 Angstroms/minute was obtained with the following process parameters:

RF power (W)	100	Pressure (mtorr)	10	CF4 flow (sccm)	30
Flow rate ratio CF4:O2	1:1	DC bias (V)	-215	Etch time (min)	100

The deepest etch was 1.2 microns. This etch rate was achieved at these process conditions:

RF power (W)	55	Pressure (mtorr)	15	CF4 flow (sccm)	8.9
Flow rate ratio CF4:O2	9:80	DC bias (V)	-190	Etch time (min)	800

X-cut lithium niobate tended to etch more slowly than z-cut crystal under the same processing conditions at a ratio of 8:15.

The etch rate achieved is suitable for low index contrast devices such as integrated optical gratings and lenses. For the large etch depths required for wideband low drive voltage modulators [1], however, the low etch rates obtained with the above detailed chemistries would be unsuitable.

Increasing the plasma frequency with apparatus such as an Electron Cyclotron Resonance (ECR) system would allow more control over the plasma and result in rates close to those described in [1].

4. References

- [1] K. Noguchi, O. Mitani, H. Miyazawa and S. Seki, "A Broadband Ti:LiNbO₃ Optical Modulator with Ridge Structure" J. Lightwave Technol, Vol 13 pp 1164-1168, June 1995

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6. Figures

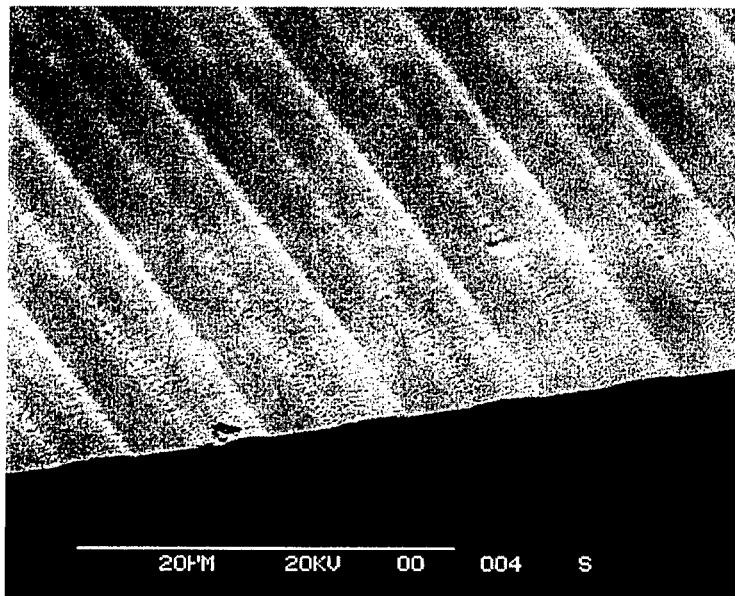


Figure 2 – Minimal etching - LN-1C-1

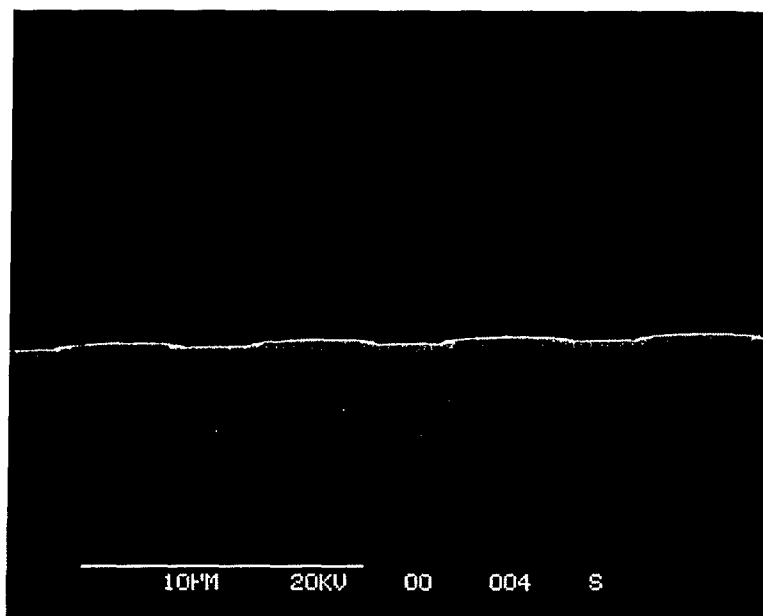


Figure 3 - Minimal etching - LN-1C-2

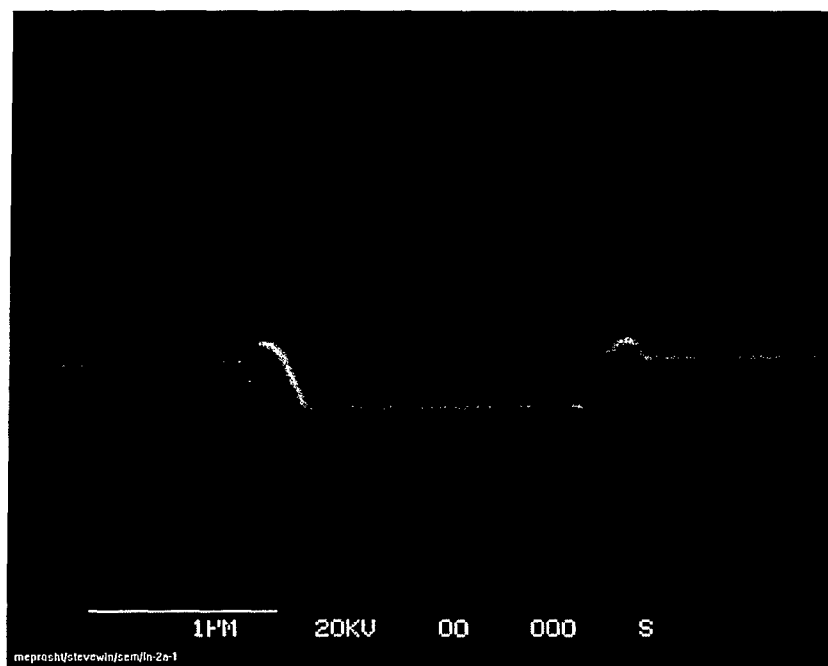


Figure 4 - Deeper etch - LN-2A

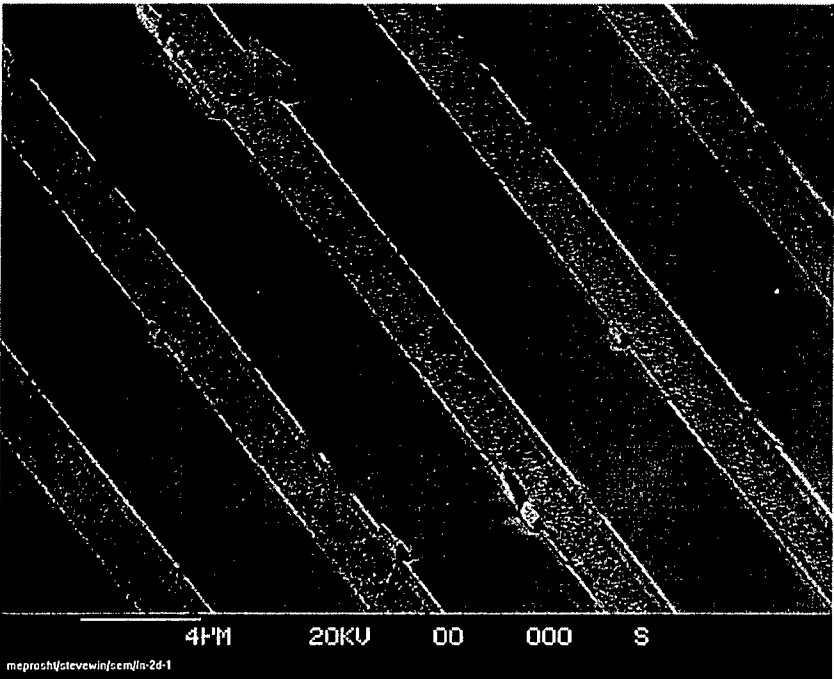


Figure 5 – Deeper etch - LN-2D-1

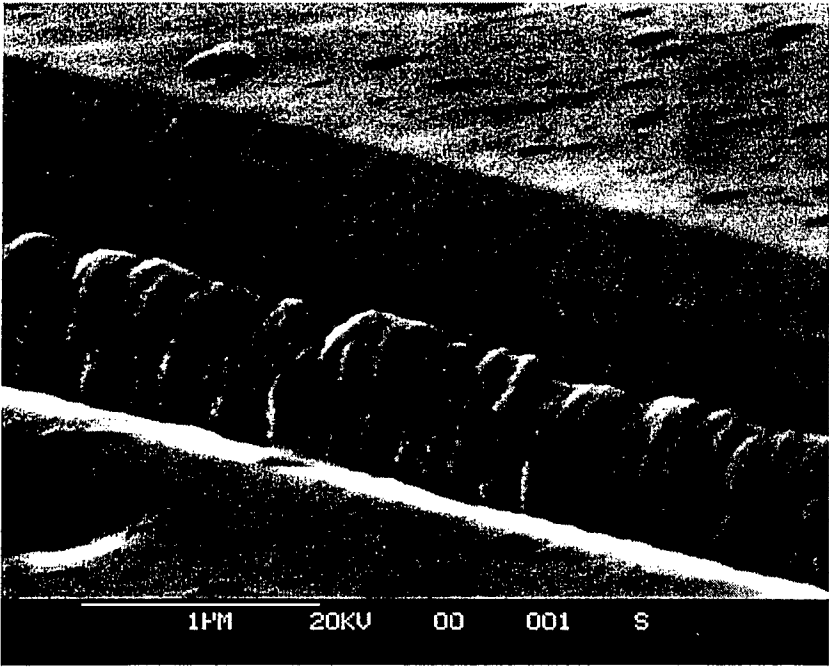


Figure 6 – Redeposition - LN-3B-4

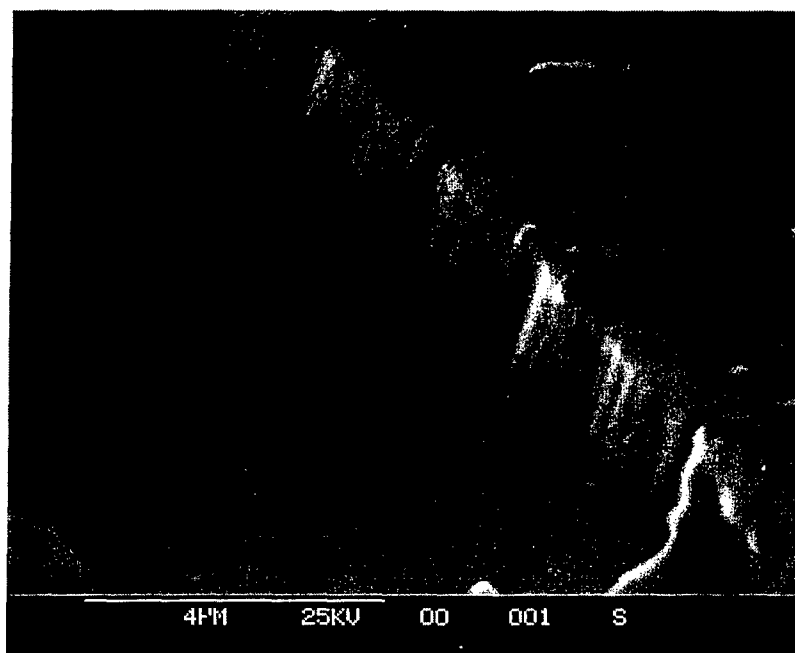


Figure 7 – Smooth sidewall etch x-cut - LN4-XCUT-1

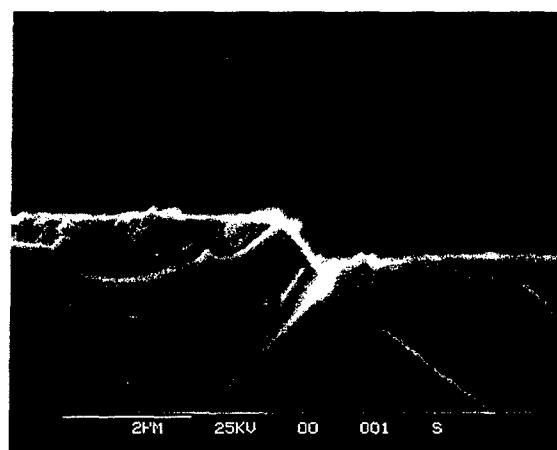


Figure 8 – Cross-section x-cut - LN4-XCUT-2

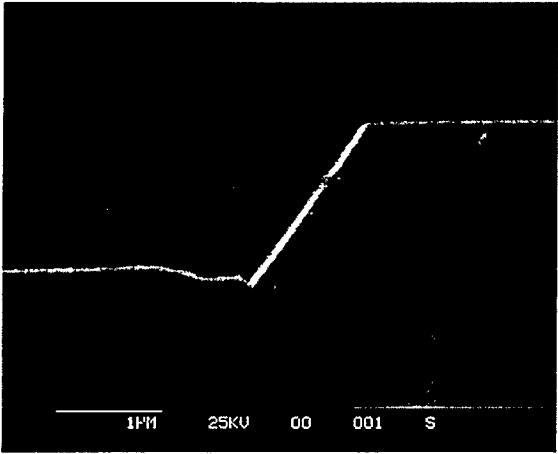


Figure 9 – Cross-section z-cut - LN5-ZCUT-1

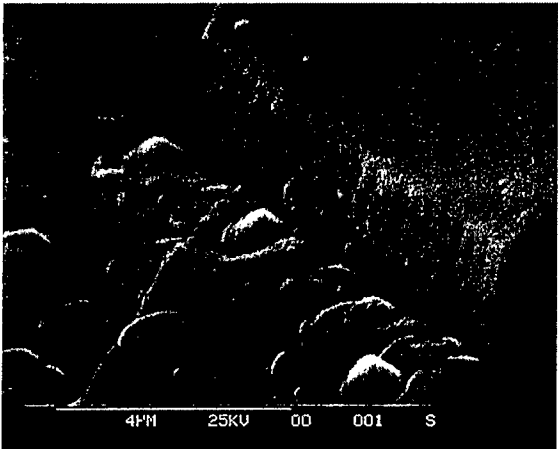


Figure 10 – Smooth sidewall etch z-cut - LN5-ZCUT-4

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