REPORT DOCUMENTATION PAGE

AFRL-SR-BL-TR-00-

0323

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY)	2. REPORT DATE	3. DATES COVERED (From - To)
	3/28/00	6/1/95 - 5/31/98

4. TITLE AND SUBTITLE

Fabrication of sub-5nm silicon nano-wires and nano devices

5a. CONTRACT NUMBER

F49620-95-0418 95-1-0418

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

6. AUTHOR(S)

J. Bokor

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of California, Berkeley
Electronics Research Laboratory
253 Cory Hall
Berkeley, CA 94720

8. PERFORMING ORGANIZATION REPORT NUMBER

442427-23108

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(E

U.S. Army Research Office
P.O. Box 12221
Research Triangle Park, NC 27709-2211

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT

Distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

A reproducible process for fabricating s licon nonowires down to 4nm in diameter has been developed. The process, as desc bed in previous reviews, relies on the stress limited oxidation of a thin silic n line. The initial line is fabricated by patterning an SOI wafer using electron b m lithography and a NiCr lift-off process. The post-oxidation wire was found to be ry sensitive to crystallographic orientation of the line, its height/widt aspect ration, and the presence of the supporting substrate.

15. SUBJECT TERMS

silicon nano-wire, nano devices

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPONE NUMBER (Include area code)

Fabrication of sub-5nm silico : nano-wires and nano devices

Final Tech l cal Report

Prof. Jeffrey Bokor EECS Department, Univ : sity of California, Berkeley, CA 94720

AASERT Grant #F49620-95-1-0418

Accomplishments/New Findings:

A reproducible process for fabricating silic n nanowires down to 4nm in diameter has been developed. The process, as describ . in previous reviews, relies on the stress limited oxidation of a thin silicon line. The itial line is fabricated by patterning an SOI wafer using electron beam lithography and NiCr lift-off process. The post-oxidation wire was found to be very sensitive to ystallographic orientation of the line, its height/width aspect ratio, and the presence c the supporting substrate.

The TEM analysis of a wide range of wir in <100> and <110> orientations revealed that the post oxidation aspect ratio is subst tially different from the initial line's aspect ratio. Figure 1 shows a 1:1 aspect ratio line hat resulted in a 4:1 aspect ratio wire. The single most important factor in determining he aspect ratio of the wire is the initial line orientation. Since (110) surfaces oxidize ster then (100) surfaces, lines in the <110> orientation fabricated on a (100) wafer o: dize faster laterally then from the top and bottom. Local stress distribution tends lower the oxidation rate of the shorter dimension, making the change in the aspec atio much larger then the 35% difference in the planar oxidation rates. The second fact that affected the geometry of the wire was the presence of the substrate oxide. When esent during the stress-limited oxidation the substrate oxide inhibited oxidation of the b om part of the wire producing a top/bottom asymmetry, as shown in figure 2.

In order to fabricate wires with a minimu diameter the initial <110> line has to be approximately 50% wider then it is tall, ar be mostly free of the oxide substrate. For <100> wires the minimum diameter aspec ratio condition is 1:1 as expected since all sides are (100). Stress limited oxidation c be used to fabricate structures other then a small silicon wire. A deviation from the p scribed aspect ratios produces a rectangular profile, that can be further oxidized to proc ce two separate wires. This occurs because the longer sides of the rectangle oxidiz faster in the middle due to lower stress distribution there.

An immediate problem with incorporat g the silicon nanowire into a device is preventing the source/drain area from oxidi ing away during the stress limited oxidation. A process that uses a thin silicon nitride lay to prevent oxidation of the source and drain regions during wire formation has been de loped. Source and drain mesas at the ends of the silicon line are formed with the same tch step as the line itself. Then a pad oxide and nitride stack is deposited using CVD. A second lithography level is used to pattern

the nitride, opening a window to the silicon l ne, but leaving the mesas protected. The substrate oxide is undercut with an wet etc : and the wire is formed by stress-limited oxidation. Then the nitride is removed and a polysilicon gate is deposited and patterned. SEM of the nanowire device is shown in fig e 3. The mesa regions are to the right and left of the central 200nm wide gate. This d vice functions as a transistor with an ultra thin body and is expected to show excellent t n-off characteristics.

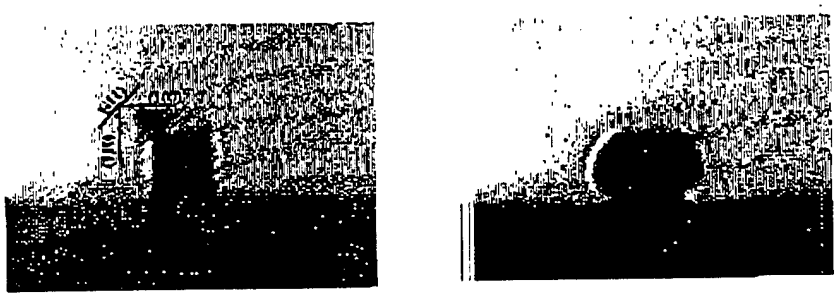


Figure 1) Left, TEM cross section of a 1 l aspect ratio line prior to oxidation. Right 1:4 aspect ratio wire af : the oxidation of a 1:1 aspect ratio line.

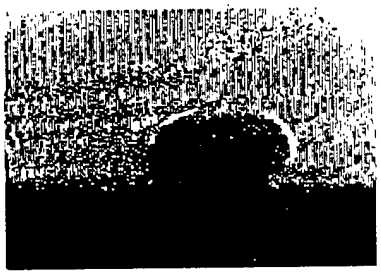


Figure 2) TEM profile of a post-oxidation profile with significant substrate oxide present. The profile shows significant top/bottom asymmetry.

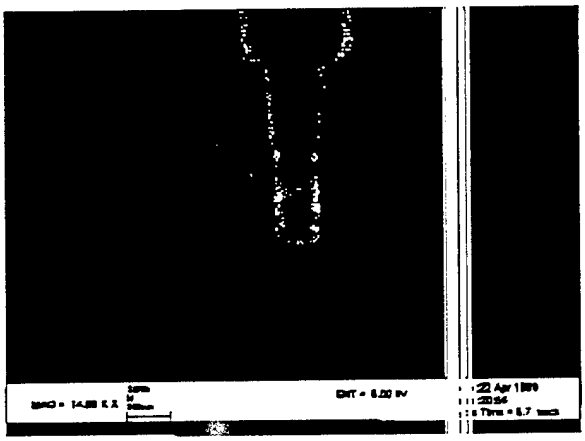


Figure 3) SEM of a nanowire device. Source/drain mesas are on the right/left. The central gate is 200nm wide. The initial silicon channel line is 50nm wide and drawn in the <110> direction. After oxidation the channel should consist of a wire only 5nm in diameter.

PERSONNEL SUPPORTED:

Graduate students: Jakub Kedzierski, Troy C[illegible]ar

PUBLICATIONS

J. Kedzierski, J. Bokor, and C. Kisielowski, . Vac. Sci. Technol. B 15, pp. 2825-2828 (1997).

NEW DISCOVERIES, INVENTIO[illegible]S OR PATENT DISCLOSURES:

None

HONORS/AWARDS

J. Bokor is a Fellow of the Optical Soci[illegible]y of America and the American Physical Society

ATTACHMENT

AUGMENTATION AWARDS FOR SCIENCE & ENGINEERING RESEARCH TRAINING (AASERT) REPORTING FORM

The Department of Defense (DoD) requires certain information to evaluate the effectiveness of the AASERT Program. By accepting this Grant which bestows the AASERT funds, the Grantee agrees to provide 1) a brief (not to exceed one page) narrative technical report of the research training activities of the AASERT-funded student(s) and 2) the information requested below. This information should be provided to the Government's technical point of contact by each annual anniversary of the AASERT award date.

1. Grantee identification data: (R&T and Grant numbers found on Page 1 of Grant)

   a. University of California, Berkeley
   University Name

   b. F49620-95-0418
   Grant Number

   c. _____
   R&T Number

   d. Professor Jeffrey Bokor
   P.I. Name

   e. From: 6/2/95 To: 5/31/98
   AASERT Reporting Period

NOTE: Grant to which AASERT award is attached is referred to hereafter as "Parent Agreement".

2. Total funding of the Parent Agreement and the number of full-time equivalent graduate students (FTEGS) supported by the Parent Agreement during the 12-month period prior to the AASERT award date.

   a. Funding: $ 200,000

   b. Number FTEGS: 2

3. Total funding of the Parent Agreement and the number of FTEGS supported by the Parent Agreement during the current 12-month reporting period.

   a. Funding: $ 2000,000

   b. Number FTEGS 3

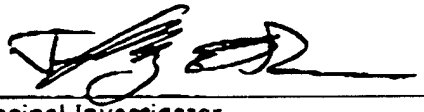
4. Total AASERT funding and the number of FTEGS and undergraduate students (UGS) supported by AASERT funds during the current 12-month reporting period.

   a. Funding: $ 50,000

   b. Number FTEGS: 1.5

   c. Number UGS: _____

VERIFICATION STATEMENT: I hereby verify that all students supported by the AASERT award are U.S. Citizens.



Principal Investigator

3/30/00
Date

University of California, Berkeley
F49620-94-1-0387