REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-01-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
06-08-1999	Presentation	

4. TITLE AND SUBTITLE
Silicon-on-Sapphire

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHORS
de la Houssaye, Paul
Lagnado, Isaac

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Space and Naval Warfare Systems Center
53560 Hull Street
San Diego, CA 92152-5001

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

In this presentation, the major issues, which confronted the formation of very thin layers of silicon (30-100 nm) on sapphire substrates for application to sub 100-nm device technology, will be reviewed. The focus of the investigation was, and still is, to achieve a structure in which the modern CMOS technology, the mainstay technology and workhorse of the electronic revolution, can be affordably implemented. In this context, one approach to the obtention of crystalline, device-quality thin film silicon-on-sapphire (TFSOS), namely the double Solid Phase Epitaxy (DSPE), has achieved truly outstanding results which are presently incorporated into high-performance products, such as phase-locked loop (PLL) ICs for wireless communication, and analog-to-digital converters for space application.

Presented at the Lateral Epitaxial Overgrowth Workshop, Juneau, Alaska, August 2-6, 1999.

15. SUBJECT TERMS
thin film silicon-on-sapphire (TFSOS)
chemical vapor deposition (CVD)

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			De la Houssaye, Paul R., D876
U	U	U	UU	35	19B. TELEPHONE NUMBER *(Include area code)* (619) 553-3912

Presented at the "Lateral Epitaxial Overgrowth Workshop", Juneau, Alaska, August 2-6, 1999.

Silicon-on-Sapphire

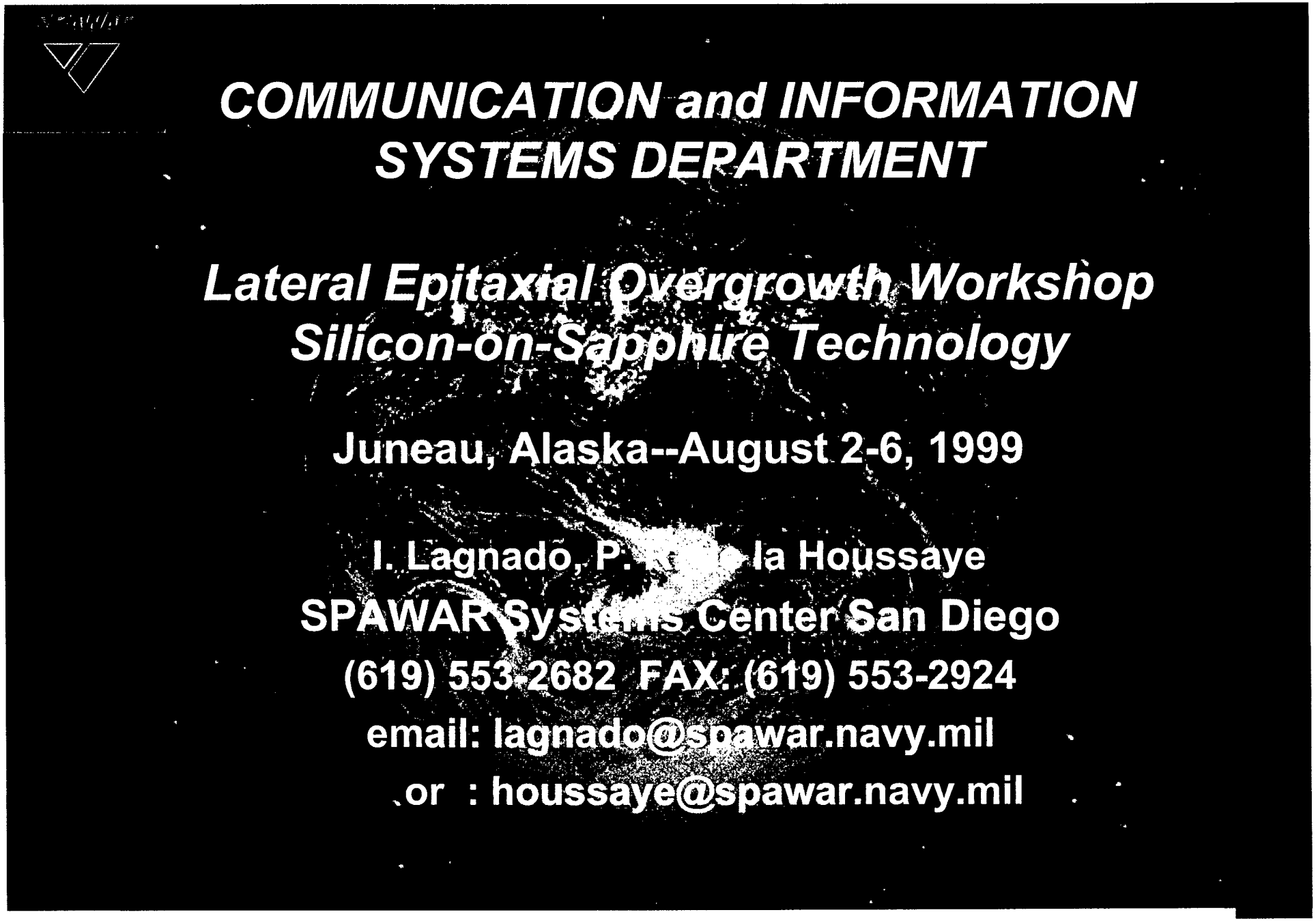
Abstract

The early sixties were at the beginning of the electronics revolution where silicon integrated circuits built their current dominance, fundamentally and pervasively on tailor-made materials, starting at the atomic level. Thin-film deposition techniques, particularly chemical vapor deposition (CVD) and molecular-beam epitaxy (MBE) were developed to provide control over material constituents "in atomic amounts", in order to form the active part of high-performance devices. Nonetheless, the CVD techniques failed to provide a crystalline silicon structure amenable to advanced devices on insulating substrates, particularly sapphire.

In this presentation, the major issues, which confronted the formation of very thin layers of silicon (30-100 nm) on sapphire substrates for application to sub 100-nm device technology, will be reviewed. The focus of the investigation was, and still is, to achieve a structure in which the modern CMOS technology, the mainstay technology and workhorse of the electronic revolution, can be affordably implemented. In this context, one approach to the obtention of crystalline, device-quality thin film silicon-on-sapphire (TFSOS), namely the double Solid Phase Epitaxy (DSPE), has achieved truly outstanding results which are presently incorporated into high-performance products, such as phase-locked loop (PLL) ICs for wireless communication, and analog-to-digital converters for space application.

Besides the materials properties, devices' performances (f_t >100GHz) and circuits' applications (analog and mixed signals), present investigations aimed at producing stressed layers of Si_{1-x} Ge_x (x>0.75) grown on TFSOS will also be described. Based on the present results, TFSOS could become entrenched, as CMOS, as new materials and devices appear – witness the recent success in developing highly-engineered structures with SiGe on TFSOS (hole mobility, through Hall measurements, is in excess of 800cm^2/V.sec) – using the established industrial infrastructure.

Isaac Lagnado
SPAWAR Systems Center San Diego
D805
San Diego, CA 92152



COMMUNICATION and INFORMATION SYSTEMS DEPARTMENT

Lateral Epitaxial Overgrowth Workshop Silicon-on-Sapphire Technology

Juneau, Alaska--August 2-6, 1999

I. Lagnado, P. [redacted] la Houssaye
SPAWAR Systems Center San Diego
(619) 553-2682 FAX: (619) 553-2924
email: lagnado@spawar.navy.mil
or : houssaye@spawar.navy.mil

SPAWAR
Systems Center
San Diego

TFSOS

- Introduction — A historical perspective
- The Vision: Thin Film Silicon on Sapphire
- Comparison with other SOI alternatives
- Recent results for SiGe –The march of Technology
- Prognosis-Trend
- Conclusion

SPAWAR
Systems Center
San Diego

Collaborators

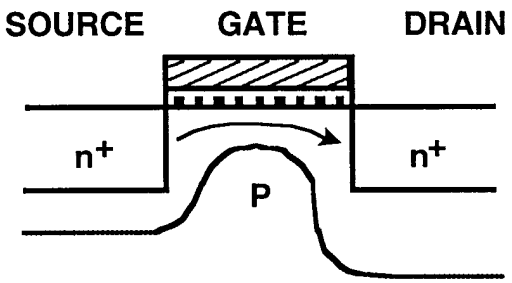
- Space and Naval Warfare Systems Center, San Diego
- University of California at San Diego (UCSD)
- International Business Machines (IBM)
- Auburn University
- Oklahoma State University
- Saphikon
- Lawrence Semiconductor
- Massachusetts Institute of Technology (MIT)
- Lincoln Laboratory
- University of Florida, Gainesville
- Peregrine Semiconductor Corporation
- Northup Grumman
- Rockwell International (Science Center)

SPAWAR
Systems Center
San Diego

Conventional Microelectronics

A Historical Perspective

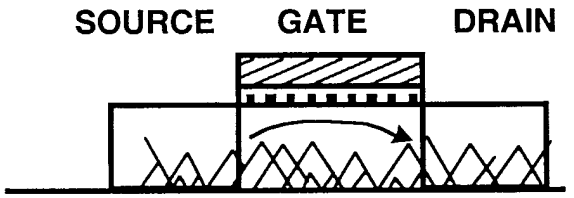
Bulk Silicon



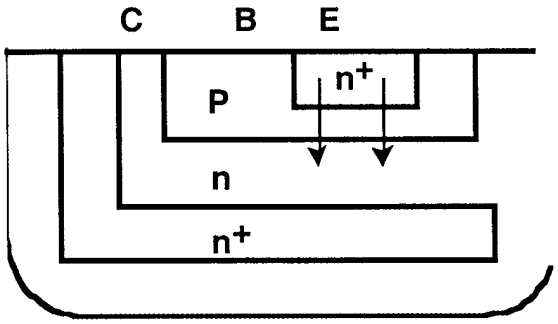
Parasitic Capacitor

← MOS →

Silicon on Sapphire (SOS)

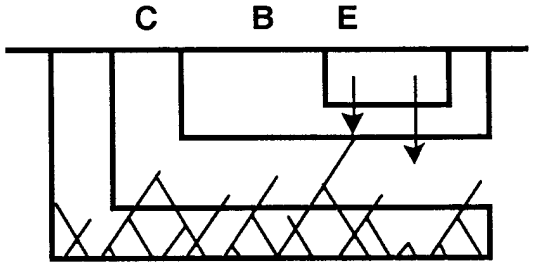


Sapphire



Parasitic Capacitor

← BIPOLAR →

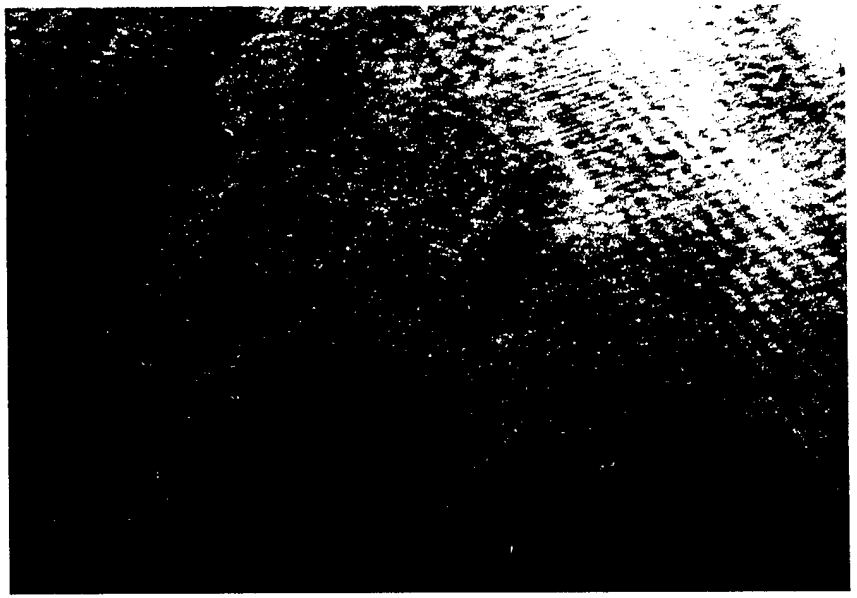


Sapphire

H.M. Manasevit & W.S. Simpton. JAP, **35**, pg 1349, 1964.

SPAWAR
Systems Center
San Diego

Thin Film Silicon on Sapphire TEM Images: Before & After Improvement Process



Before Improvement

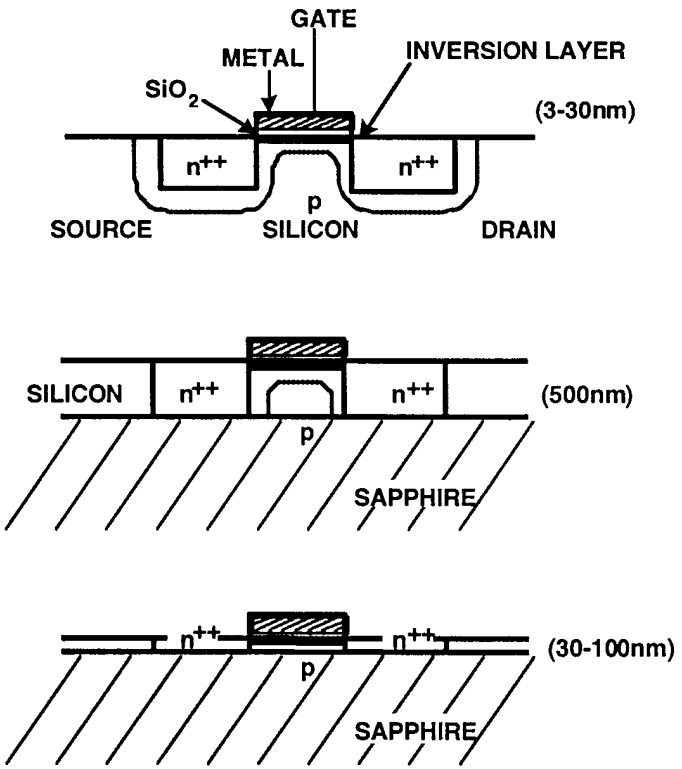
After Improvement

SPAWAR
Systems Center
San Diego

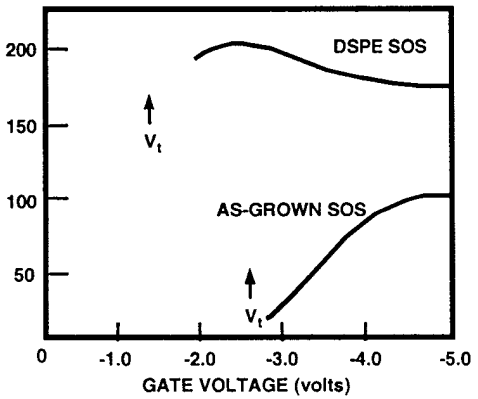
Thin Film Silicon on Sapphire

The Vision

Scaling Limits



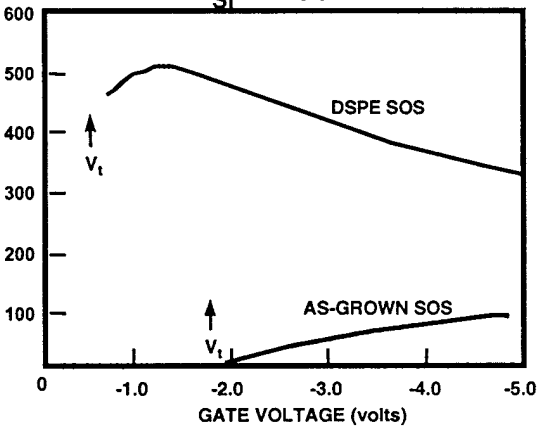
Low-Field Hole Mobility
t_{Si} = 100nm



G.A. Garcia, R.E. Reedy. *Elect. Let.*, **22**(10), p. 537-538, 8 May 1986.
G.A. Garcia, R.E. Reedy, M.L. Burgener. *EDL*, **9**(1), p. 32-34, Jan. 1988

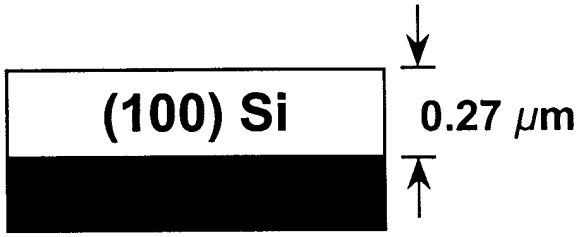
M. Roser, *et al.*. 50th Device Research Conference, June 22-24, 1992

Low-Field Electron Mobility
t_{Si} = 100nm

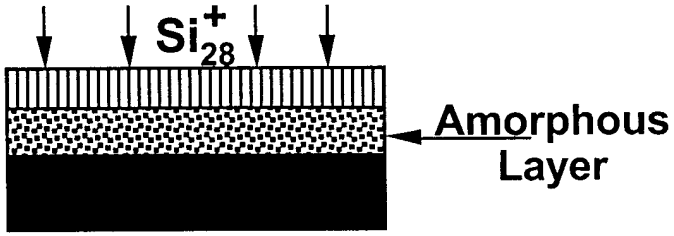


SPAWAR
Systems Center
San Diego

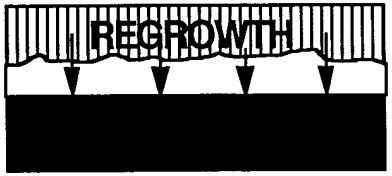
ULTRATHIN SOS
Improvement and Thinning Sequence



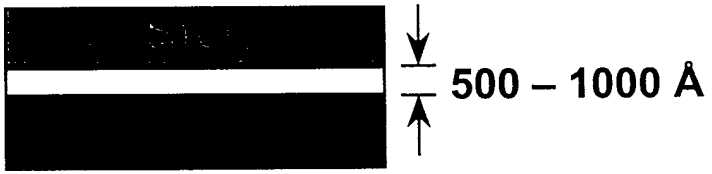
1) CVD Silicon as Grown



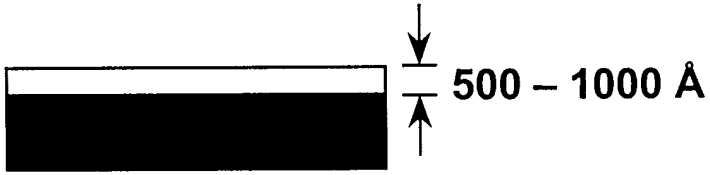
2) Si implant



3) Two–Step Anneal
   a) 550 °C SPE Regrowth
   b) 900 °C Defect Removal



4) Thermal Oxidation



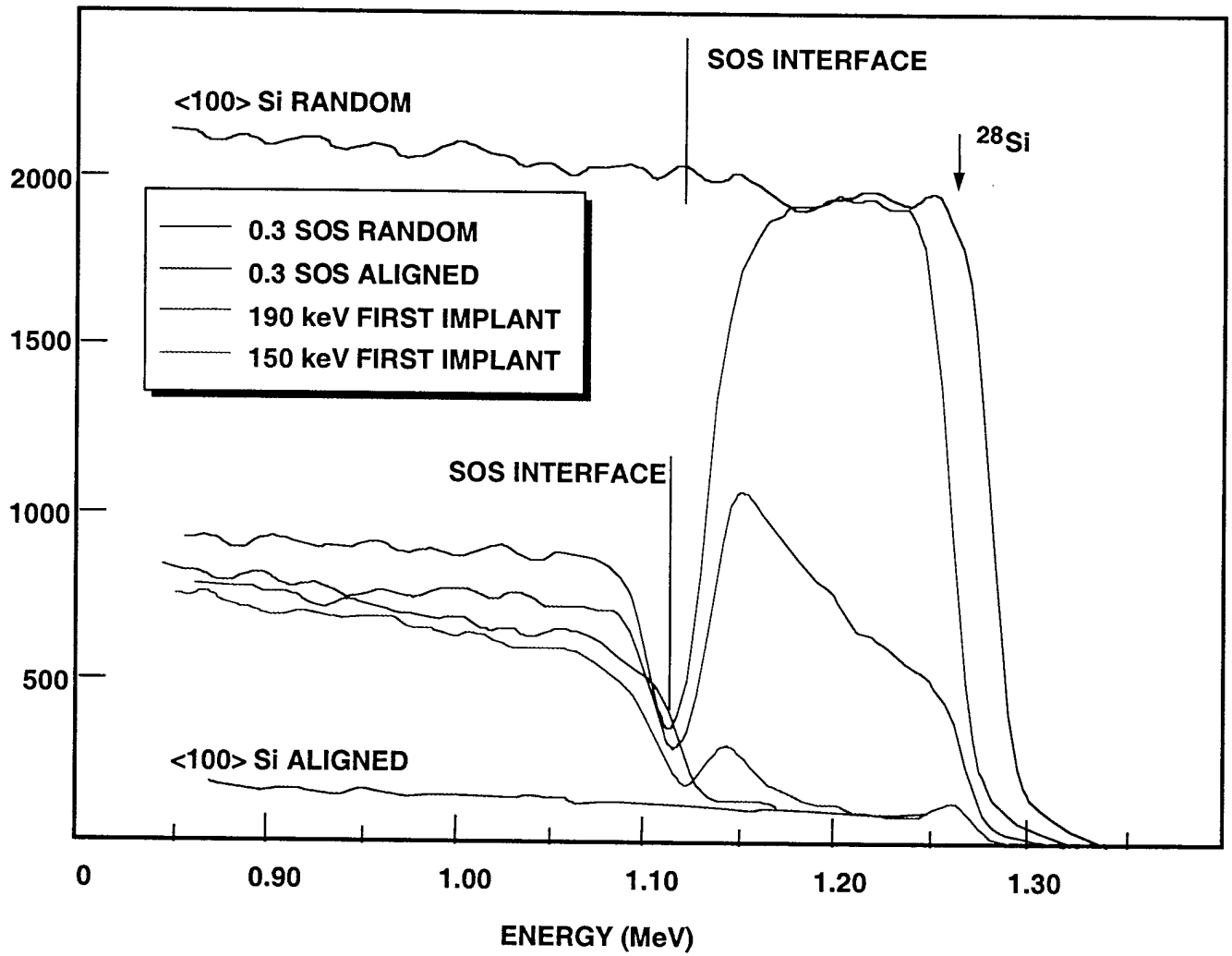
5) Strip Oxide (HF)

Final Product:
Device Quality Single Crystal Silicon Film Under Compressive Strain

S.S. Lau *et al.*, *APL*, **34**(1), p. 76-78, 1 Jan. 1979.
T. Yoshii *et al.*, *JJAP*, Part 1, **21**(suppl.21-1), p.175-179, 1982.

SPAWAR
Systems Center
San Diego

RBS Data, TFSOS

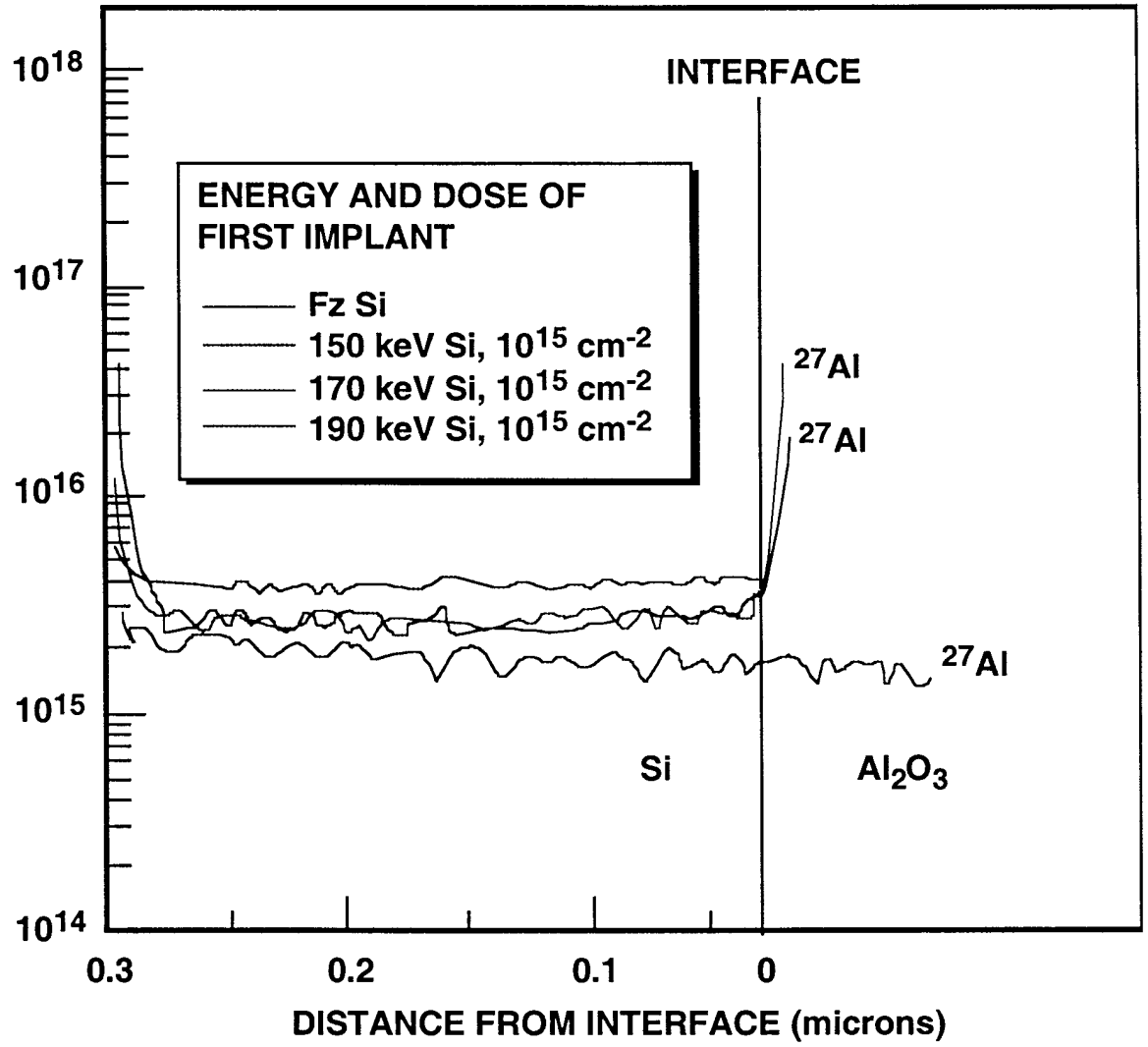


G.A. Garcia, R.E. Reedy. *Electronics Let.*, **22**(10), p. 537-538, 8 May 1986.

R.E. Reedy, G.A. Garcia. MRS Symposium Proc. **107**, p. 365-376, 1988.

SPAWAR
Systems Center
San Diego

Auger Analysis, TFSOS



R.E. Reedy, T.W. Sigmon, L.A. Christel, *APL*, **42**(8), p. 707-709, 15 April 1983.

SPAWAR
Systems Center
San Diego

Thin Film CMOS/SOS *vs.* Other Silicon Implementations

Relative to Bulk CMOS

- Reduced parasitic capacitances
  - less junction capacitances and higher speed)
- Reduced short channel effects
- Better device isolation
  - Latchup suppression
  - Lower body effect
  - Wider operating temperature
- Simple mesa fabrication
- Radiation hardness

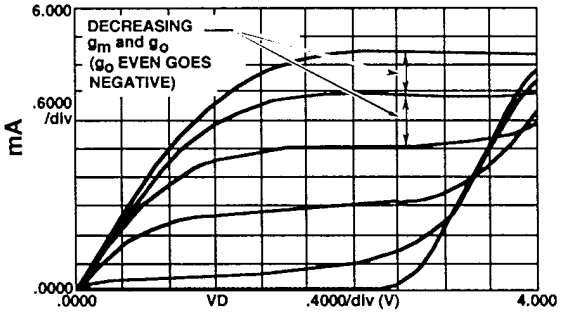
Relative to SIMOX/BESOI

- Lower loss dielectric substrate
  - Lower substrate capacitance
  - Higher Q passive elements
- Lower minority carrier lifetime
  - Parasitic bipolar suppressed
  - Higher S-D breakdown voltage
- Higher thermal conductivity than SiO_2
  - Reduced self-heating effects
- Enhanced hole transport properties
  - PMOS closer to NMOS in size, f_T, f_{Max}
  - Enhanced CMOS performance
- 6-in wafers available, 8-in also available
- Lower cost/Process Simplicity
- Much reduced Floating Body Effect
  - Low leakage Ioff (digital)
  - No Kink Effect in I-V (analog)
- No Transient Hysteresis (low frequencies)

SPAWAR
Systems Center
San Diego

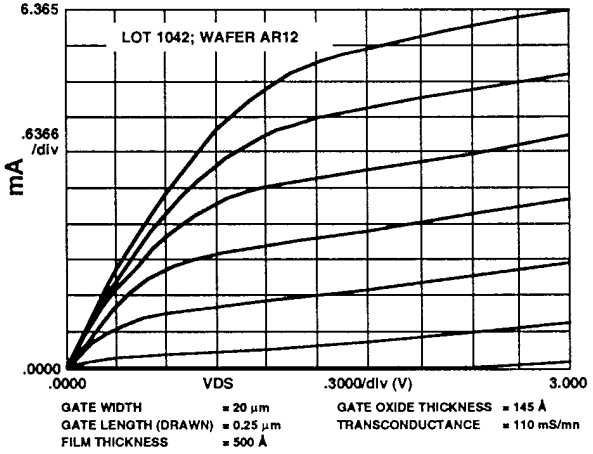
Thermal Effects
Thin Film Silicon on Sapphire *vs.* SIMOX

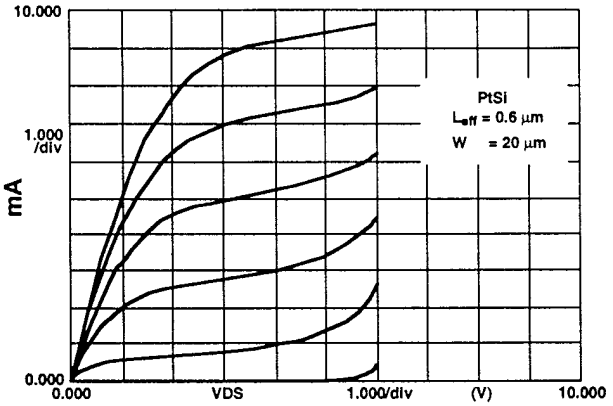
SIMOX

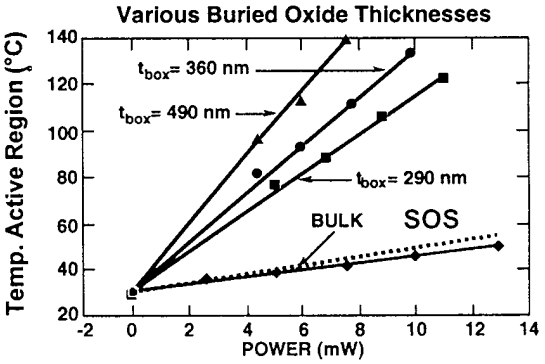


W_{eff} = 10 μm
L_{eff} = 0.3 μm
T_{st} = 70 nm
T_{ox} = 10 nm
T_{box} = 360 nm
N_{sub} = 3 x 10^{17} cm^{-3}

TFSOS





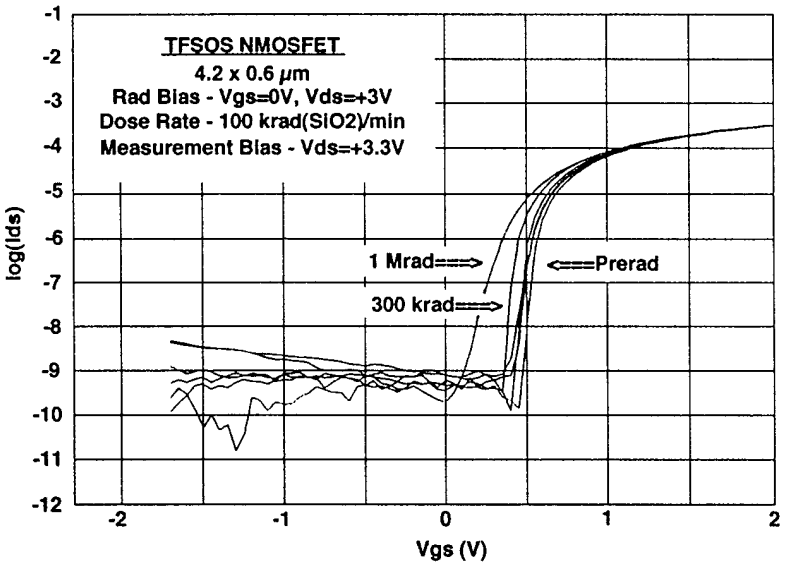


SOS Data:
M. Wetzel, UCSD Ph.D.
Thesis (to be published)

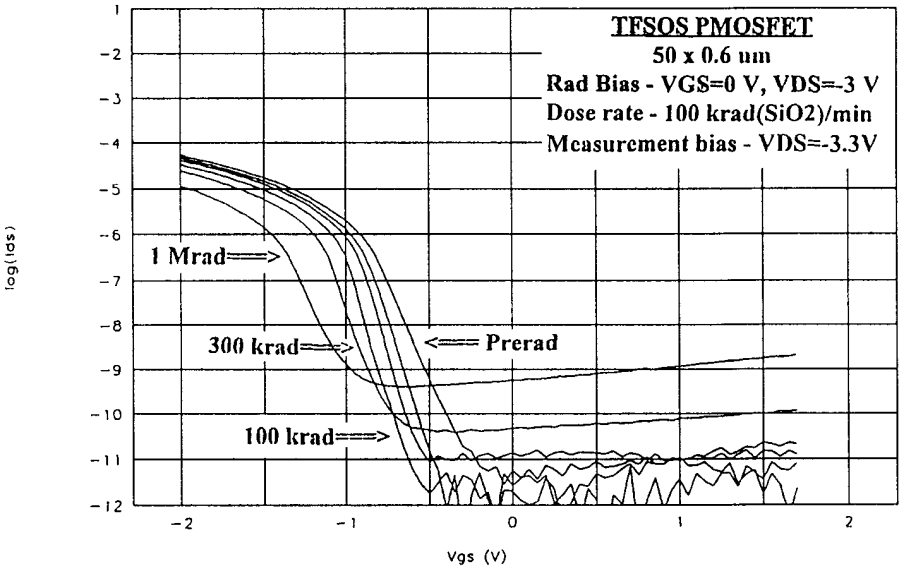
MIT data;
Courtesy Prof. D. Antoniadis

SPAWAR
Systems Center
San Diego

Radiation data for TFSOS MOSFETs



n-MOSFET



p-MOSFET

SPAWAR
Systems Center
San Diego

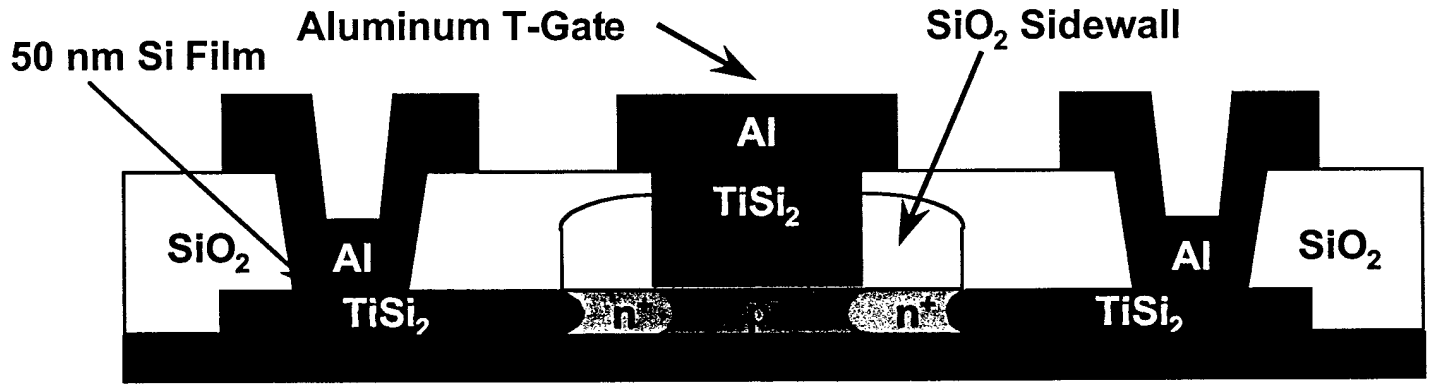
Thin Film Silicon on Sapphire

- T-Gate used to decrease R_g
- Record high f_t , f_{max} microwave transistor
- Record low noise microwave transistor

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + G_o\left[R_g + R_s\right]}}$$

$$F_{min} = 1 + kLf\sqrt{g_m\left[R_s + R_g\right]}$$

Device	$L_{g,drawn}$(μm)	f_t (GHz)	w/wo T-Gate f_{max} (GHz)	@ 2GHz F_{MIN} (dB)	G_a (dB)
NMOS	0.5	25	66/11	0.9	21
PMOS	0.5	14	41/7	0.9	13



R.Johnson *et al. TED*, **45**(5), May 1998.

SPAWAR
Systems Center
San Diego

NOISE COMPARISON

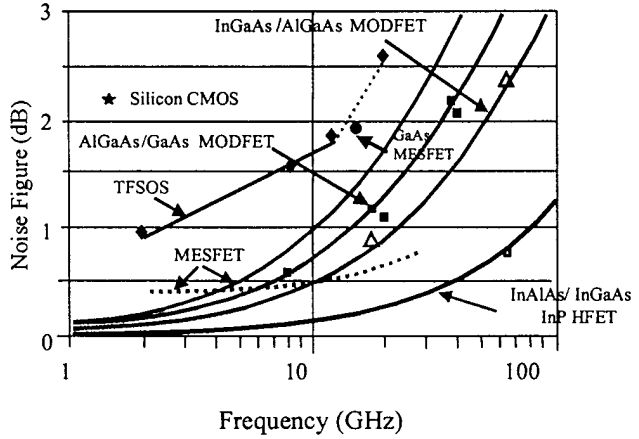
	2 GHz		8 GHz		12 GHz		$L_g(\mu m)$	Technology
	F_{min}	G_a	F_{min}	G_a	F_{min}	G_a		
TFSOS:								
NMOS[9]	0.9	21	1.4	11	1.8	8.5	0.5	TF SOS
PMOS[9]	0.9	13	1.3	4.7	-	-	0.5	TF SOS
Other Si:								
NMOS [1]	1.5	18	3.25	8.5	-	-	0.25	MICROX
PMOS [1]	2.7	15	-	-	-	-	0.25	MICROX
NMOS [2]	0.8	17	1.6	9.8	2.2	6.8	0.6	MICROX
NMOS [3]	5.0	6.4	-	-	-	-	1.0	BESOI
Other:								
HBT [4]	0.5	12	0.8	-	1.0	-	2 x .6 x 8	SiGe
HBT [5]	0.46	11.6	1.4	-	2.0	-	3.5 x 3.5	InP/InGaAs
PHEMT [6]	0.2	-	.33	-	0.41	13	0.15	GaP/InGaAs
JFET [7]	0.4	-	1.6	-	-	-	0.5	GaAs
MESFET [8]	0.4	23	0.5	15	0.5	13	0.11	GaAs

1. EDL, May 1993, pg. 219, Hanes *et al.*
2. MTT-S Workshop, May 1995, Agarwal *et al.*
3. EDL, Jan 1991, pg. 26, Caviglia, *et al.*
4. MTTS, 1994 pg 1167, H. Schumacher, *et al.*
5. EDL, Oct 1989, Y.K. Chen *et al.*
6. EDL, Aug 1983, pg. 406, M. Takikawa *et al.*
7. EDL, Sept. 1993, D. Scherrer *et al.*
8. TED, Feb 1999, pg. 310, Kimo *et al.*
9. TED, May 1998, pg. 1047-54, R.Johnson *et al.*

SPAWAR
Systems Center
San Diego

Noise Figure Results for Different Technologies: Transistors and LNAs

Noise figures of FET's based on GaAs and of Si CMOS transistors.
After L.M. Franca-Neto *et al.*, *IEDM*, pg. 305-307, 1997.



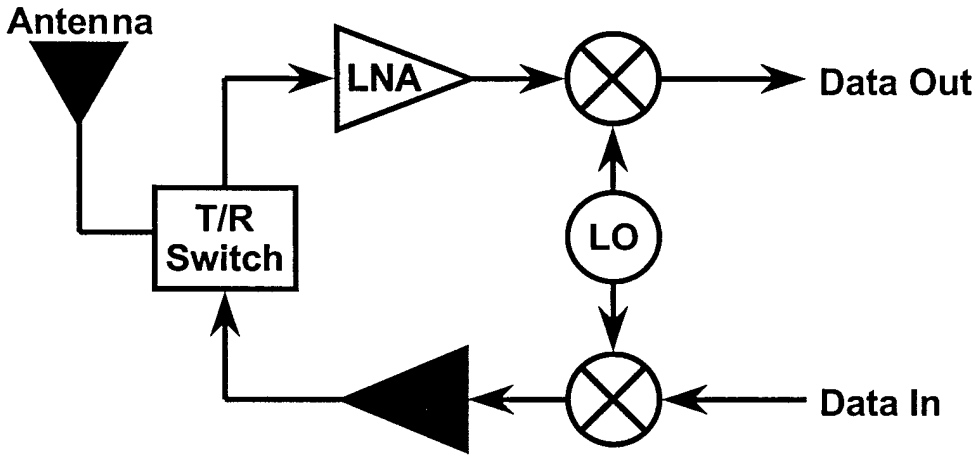
Recent Results on Low Noise Amplifier Designs
After L.M. Franca-Neto *et al* ., *IEDM*, pg. 305-307, 1997.

Technology	F (GHz)	NF (dB)	Author
1 micron GaAs FET	1	2.2	Cioffi, IMMMCS, 1992
1 micron GaAs FET	1.6	2.2	Cioffi, IMMMCS, 1992
0.3 micron GaAs FET	1.9	2.0	Nakatsugawa, GaAs-IC Symp, 1993
1 micron GaAs FET	1.9	1.5	Heaney, GaAs-IC Symp., 1993
0.3 micron GaAs FET	1.6	2.5	Imai, IEEE-Trans. MTT, 1991
0.5 micron CMOS	0.9	2.2	Karanicolas, ISSCC, 1996
1 micron CMOS	0.9	3.5	Rofougaran, IEEE-JSSC, 1996
0.6 micron CMOS	1.5	3.5	Shaeffer, IEEE-JSSC, 1997
0.5 micron CMOS/SOS	2.4	2.2	Johnson, R.A. *et al.*, IEEE-TED, 1998

SPAWAR
Systems Center San Diego

Thin Film Silicon on Sapphire Wireless Communications Applications

- **Demonstrate SOS technology application to L and S band Applications**
- **Test Vehicle: 2.4 GHz transceiver**
  - **Transmit / Receive Switch** R.A. Johnson et al., *IEE Elect. Lett.*, **33**(15), pg. 1324-1326, 17 July 1997.
  - **Mixer** R.Johnson et al., TED, **45**(5), pg. 1047-1054, May 1998.
  - **Low Noise Amplifier** R.A. Johnson et al, *IEEE Microwave & Guided Wave Letters*, **7**(10), pg. 350-352, Oct.1997.
  - **Power Amplifier** M. Wetzel *et al.*, 1st Annual UCSD Conference on Wireless Communications, March 8-10, 1998



SPAWAR
Systems Center
San Diego

Why CMOS/SOS at Microwave/RF Frequencies

- Low power, high noise immunity
- Cost
  - High integration level (VLSI) / Mature technology
    - ➡ Competitive manufacturing cost (7-10% higher than CMOS bulk Si)
    - ➡ Complexity => Low cost per functional unit
    - ➡ 6" wafers available with low defect density
  - Reduced processing steps (mesa isolation)
    - ➡ Much lower cost than bipolar, HBTs (Si or III-V's)
  - Inexpensive material (except vs. bulk silicon)
  - Leverage off Si manufacturing base
- Mixed analog / digital integration
  - Low loss dielectric substrate (isolation/ no latch up)
    - ➡ Low substrate capacitance
    - ➡ High Q passive elements
  - f_{max} = 66 GHz (L_{eff} ~ .3 μm), Noise Figure < 1 dB optically defined devices
  - f_t > 100 GHz (L_{eff} ~ .1 μm) (x-ray)
  - Very high linearity at low power (good IP3)
  - Excellent ESD protection with low parasitics
- SiGe/SOS, m_h > 800 $cm^2/V.sec$ (pMODFET, L_g = 0.1 μm, g_m = 420 mS/mm)
  --> much higher speed CMOS with lower power

SPAWAR
Systems Center
San Diego

Why CMOS/SOS at Microwave/RF Frequencies

- Low power, high noise immunity
- Cost
  - High integration level (VLSI) / Mature technology
    - ➡ Competitive manufacturing cost (7-10% higher than CMOS bulk Si)
    - ➡ Complexity => Low cost per functional unit
    - ➡ 6" wafers available with low defect density
  - Reduced processing steps (mesa isolation)
    - ➡ Much lower cost than bipolar, HBTs (Si or III-V's)
  - Inexpensive material (except vs. bulk silicon)
  - Leverage off Si manufacturing base
- Mixed analog / digital integration
  - Low loss dielectric substrate (isolation/ no latch up)
    - ➡ Low substrate capacitance
    - ➡ High Q passive elements
  - f_{max} = 66 GHz (L_{eff} ~ .3 μm), Noise Figure < 1 dB optically defined devices
  - f_t > 100 GHz (L_{eff} ~ .1 μm) (x-ray)
  - Very high linearity at low power (good IP3)
  - Excellent ESD protection with low parasitics
- SiGe/SOS, m_h > 800 $cm^2/V.sec$ (pMODFET, L_g = 0.1 μm, fabricated; to be published)
  --> much higher speed CMOS with lower power

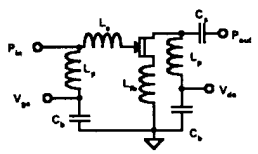
SPAWAR
Systems Center
San Diego

Circuit Level SOS rf Results

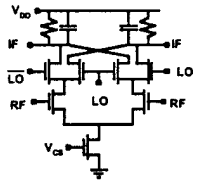
FY98 Circuits Test Results

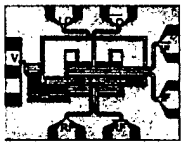
LNA, MIXER and T/R Switch Fabricated in TFSOS

MEASURED	Operating Freq	Gain	NF (50 Ω)	IP3 (output)	Power@vdd
LNA	2.4 GHz	11 dB	2.2 dB	14 dBm	13.2mW@1.5V
Mixer	Center=2.4 GHz IF=250 MHz	-5 dB		5 dBm	8.4mW@1.5V



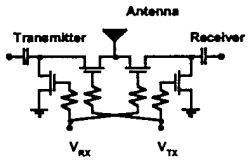
1.3 mm X 0.95 mm

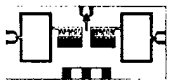




0.95 mm X 0.73 mm

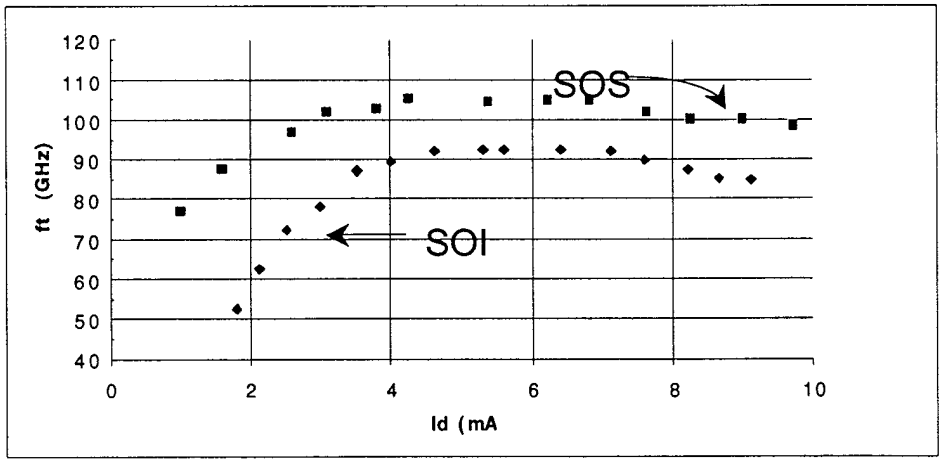
MEASURED	Operating Freq	Insertion Loss	Isolation	IP3
T/R Switch	1-5 GHz	1.7-2 dB 0.6-0.7 db	30 dB 20 dB	8 dBm





1.5 mm X 0.55 mm

- Record high f_t (> 105 GHz)
- CMOS inverter delay < 8 psec at RT; 6 psec @ 77K, close to JJ speed;
- Record low noise (0.9 dB NF @ 2GHz), resulting in low noise front end
  ==> MAKES HIGH SPEED, HIGH RESOLUTION A/DC possible
- Record BW (10 GHz) for distributed amplifier



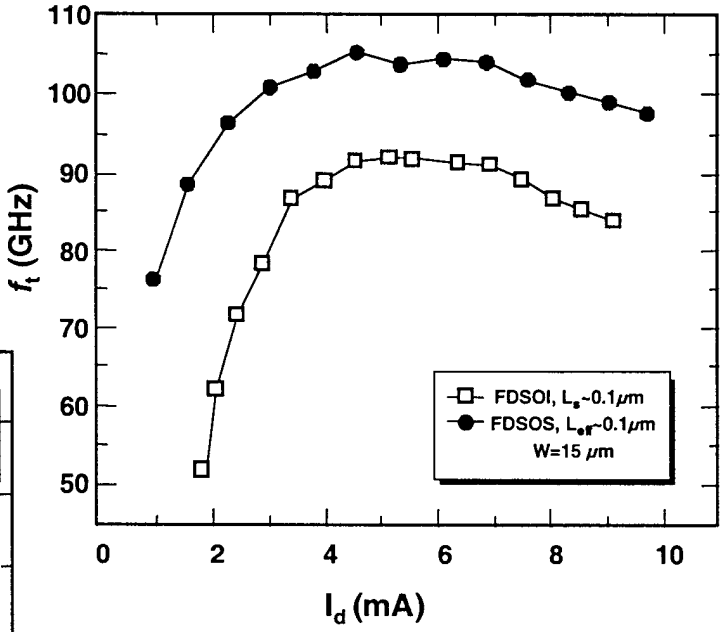
F_t *vs.* I_{ds}

SPAWAR
Systems Center
San Diego

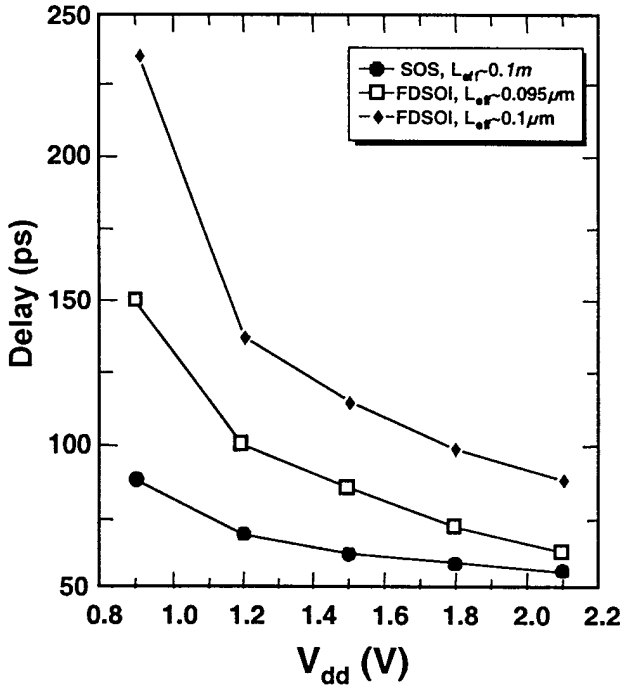
TFSOS *vs.* TFSOI RF Data

C. Wann *et al.* ISSCC, Feb. 1998
C. Wann *et al. EDL*, **18**(12), pg. 625-627, Dec. 1997

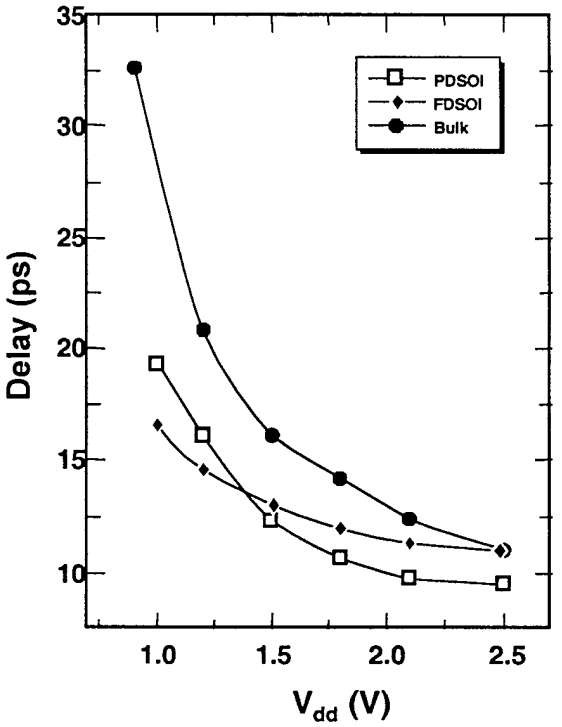
f_t *vs.* I_d



Unloaded 3-way NAND Delay *vs.* V_{dd}



Delay per Stage *vs.* V_{dd}



SPAWAR Systems Center San Diego

COMPARATIVE STUDY of CMOS on TFSOS *vs.* SIMOX *vs.* BULK SILICON

Accomplishment

Objective:

- **Determine the comparative CMOS-based alternatives (bulk Si, SIMOX, TFSOS) to implement low power, high frequency, cost-effective VLSIC technology at ≤ 100nm regime in an environment conducive to manufacturing.**

Accomplishment:

- **Test vehicle: 4-bit, 10 Gsps A/DC.**

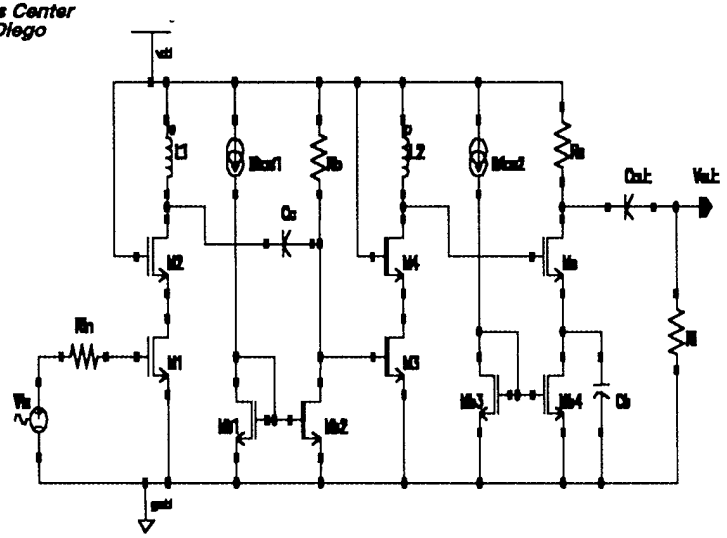
Comparator Bank **Bubble Detector** **Encoder Latch** **Output Buffer**

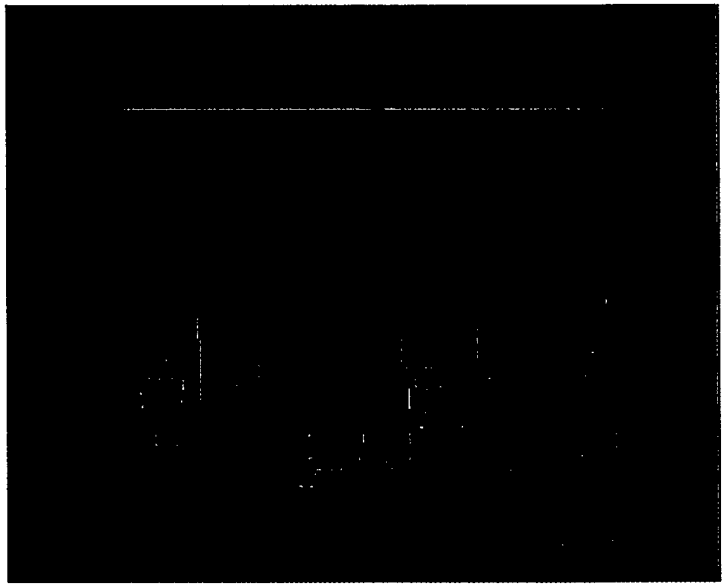
f_{max} = 10 GHz goal; f_{max} = 7.5-8 GHz experimental

	Comparator Bank Delay = t_d Ln 2^n (pS)	Bubble Detector Delay (pS)	Encoder Delay (pS)	Total Delay (pS)	Clock f_{max} (GHz)
CMOS/Si Bulk	108	47	76	231	4.1
CMOS/SIMOX	86	37	60	183	5.5
CMOS/TFSOS	56	29	46	131	7.5-8

SPAWAR
Systems Center
San Diego

13-GHz Tuned Amplifier





- **Demonstrated Functional Samples (Body-Tied and Floating Body) on Bulk, SOI, and SOS wafers.**
- **The Peak Gain is ~15dB for SOS Samples.**
- **Amplifiers with Floating Body have ~5dB Higher Gains.**
- **Bulk Samples Have Less than 0dB Gain**
- **SOS Samples Have Significantly Better Characteristics than SOI and Bulk Samples.**

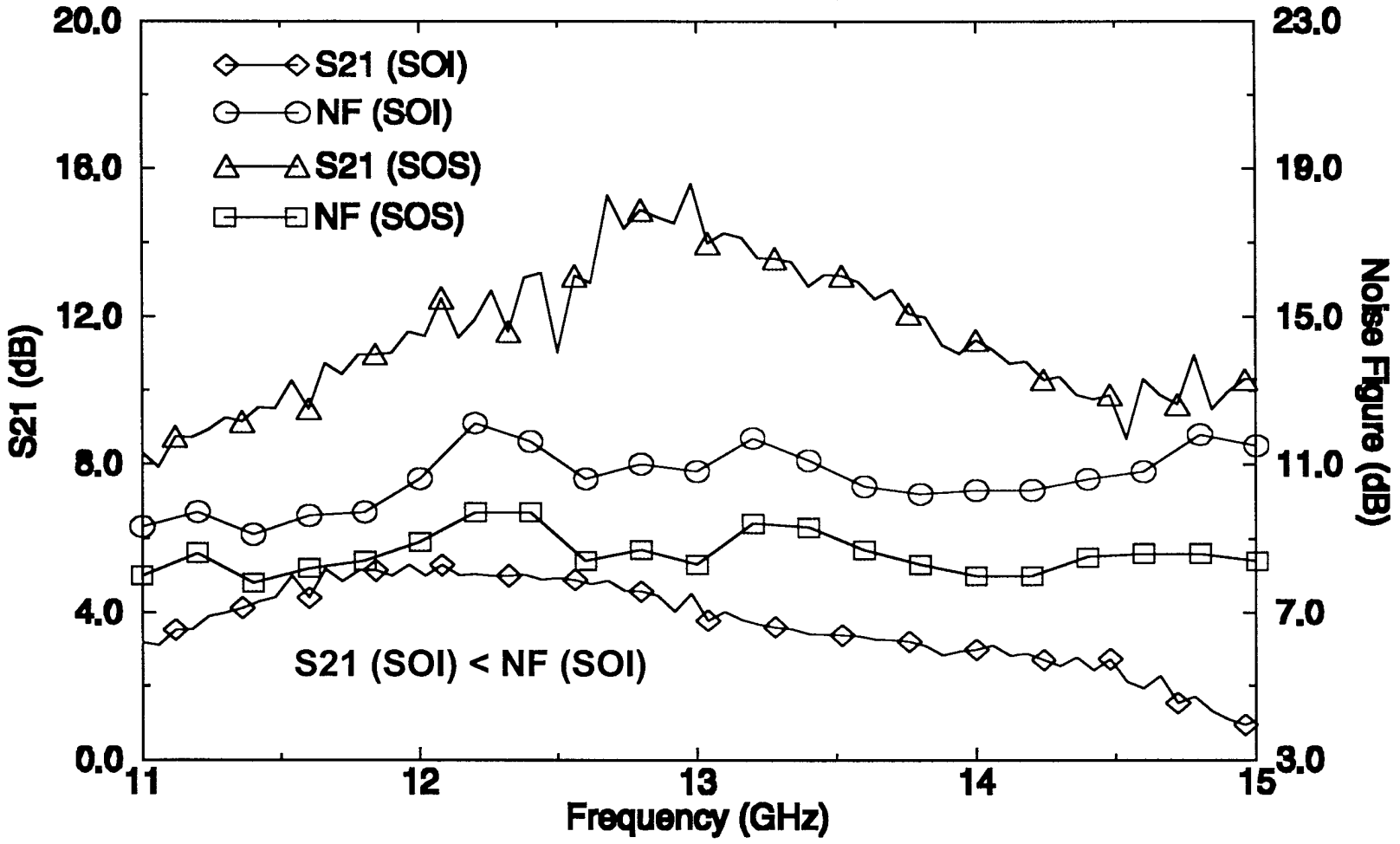
K.K. O *et al. GOMAC*, March 1998.
Yo-Chuol Ho, *et al.* Custom Integrated Circuits Conference, April 1998.
K.-H. Kim et al. ISSCC, Feb. 1998.

SPAWAR
Systems Center
San Diego

Transducer Power Gain & Noise Figure

PD Floating-Body SOS and SOI

13-GHz Tuned Amplifier

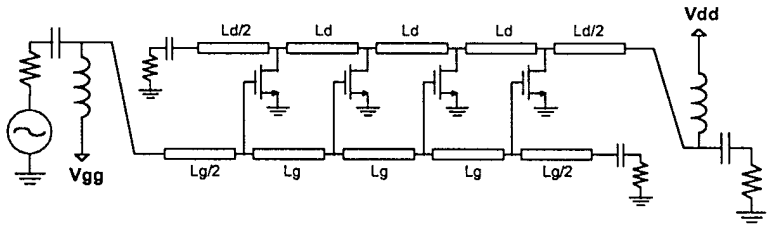


SPAWAR
Systems Center
San Diego

Distributed Amplifer

Broadest bandwidth ever reported for any Si-FET distributed amplifier

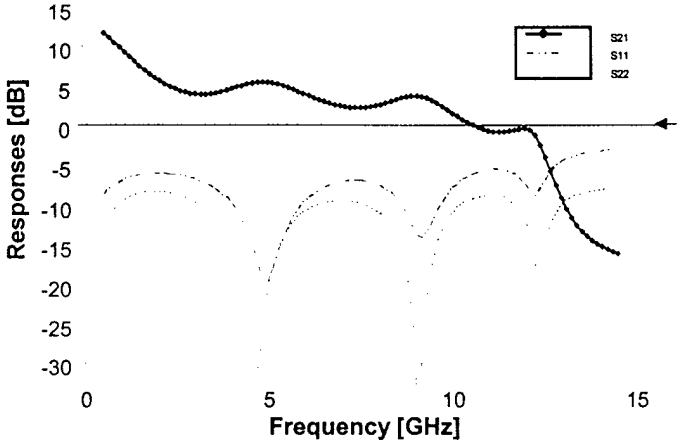
300 um gate width, 4 stages



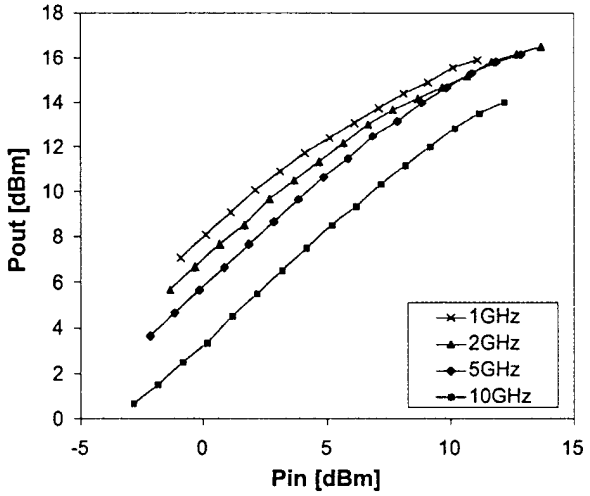
Schematic

Photograph of Amplifier

SOS Distributed Amplifier
300µm x 4 stages (External Matching)



Frequency response



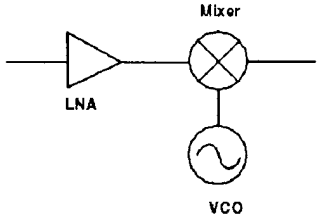
Power measurements at 1, 2, 5, & 10 GHz

SPAWAR
Systems Center
San Diego

NEAR FUTURE

Fabrication in Progress:

- LNAs, Mixers, VCOs for operation @18-40 GHz
- System-on-a-Chip @18 GHz
- Single-chip GPS receivers (~80-100 dB isolation)-SBIR '99
- SiGe p-FET (> 100 GHz) & Logic



SIMULATED	Operating Freq	Gain	NF (50 Ω)	IP3 (output)	Power@vdd
LNA	18 GHz	15 db	3 dB	5dBm	22mW@1.5V
LNA/Differential	18 GHz	22 dB	3.7	10 dBm	60mW@1.5
Mixer	Center=16-20GHz IF=0.5-4 GHz	7 db	10 dB	5dBm	40mW@1.5V

SPAWAR
Systems Center
San Diego

Thin-film Silicon-on-Sapphire Characteristics

- Lower capacitance --> higher speed at lower power
- Fully depleted operation --> improved low voltage performance (esp. w.r.t. bipolar)
- Lower minority carrier lifetime
  - Parasitic bipolar suppressed
  - Higher S-D breakdown voltage
- Enhanced PMOS --> higher hole mobility than bulk Si, due to compressive stress (valence band splitting); better design flexibility for low power CMOS over GaAs (no p-channel)
- Excellent rf performance
  - f_t > 100 GHz for 0.1 μm L_{eff} n-type transistors
  - f_{max} > 66/45 GHz for .4 μm n/p-channel
  - Extremely low-loss substrate at rf (loss tangent < .0001)
- No parasitic coupling to substrate for passive components
- Good thermal conductivity
  - Higher than SiO_2
  - Comparable to GaAs

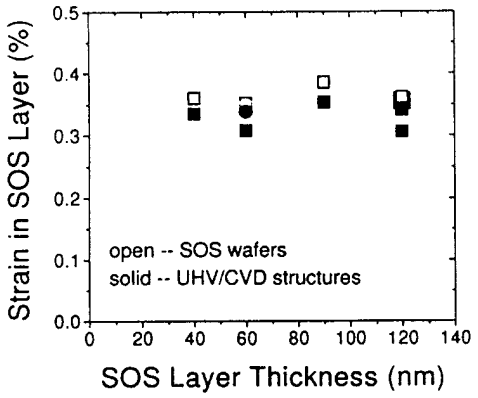
SPAWAR
Systems Center
San Diego

UHV/CVD Grown FET Structures

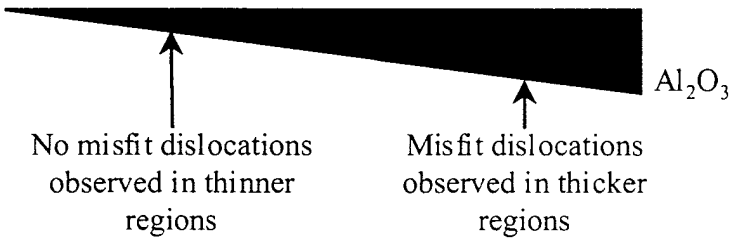
- SOS layer is compressively strained ~ 0.35%
- Remains ~ 0.30% strained after UHV/CVD growth
- Low density of misfit dislocation at the Si/Al_2O_3 interface

P. Mooney *et al.*, Appl. Phys. Lett. 73, pg. 924 , 1998.
——Mat. Res. Soc. Symp. Proc., **533**, pg. 55, 1998.
——*To be published in Applied Physics Letters.*

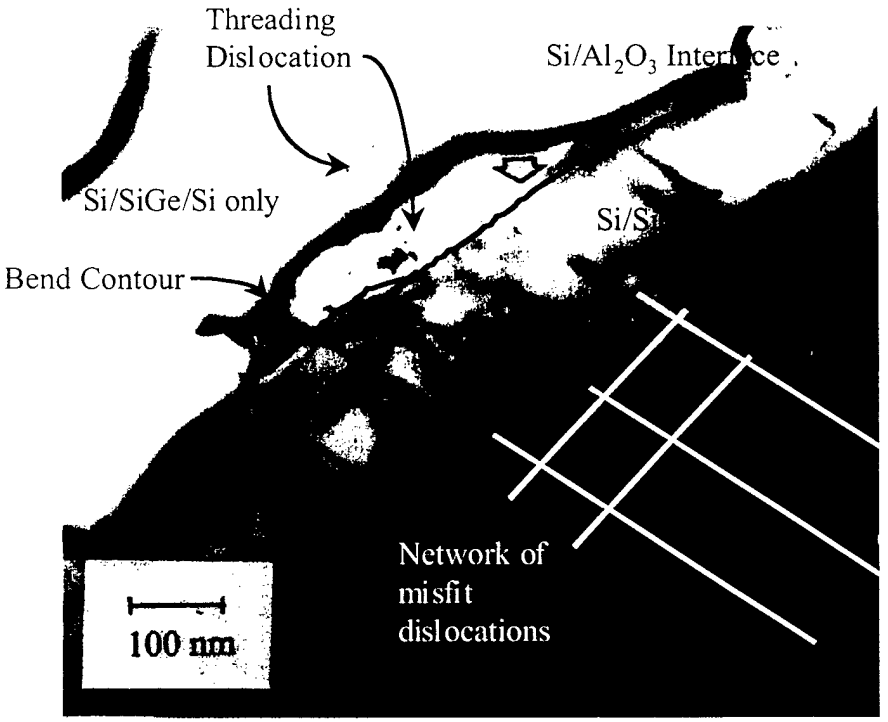
X-ray diffraction



Cross Section



Planar-view TEM



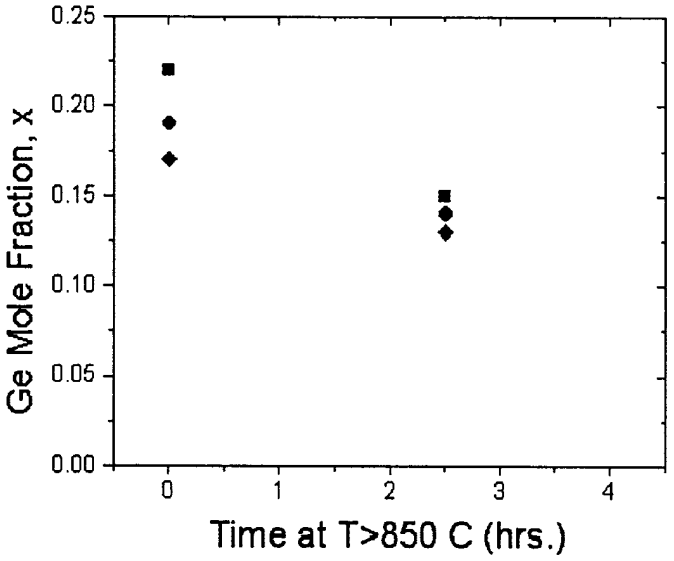
Arrows point to Si/Al_2O_3 interface where misfit dislocations end

SPAWAR
Systems Center
San Diego

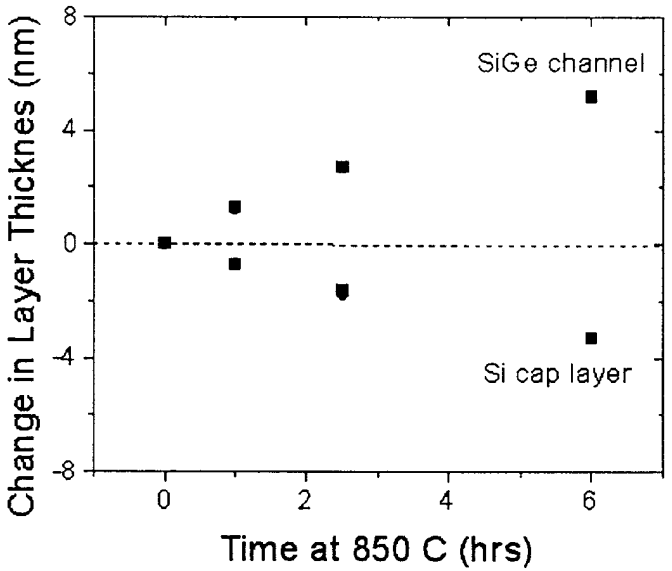
Triple-Axis X-Ray Diffraction Measurements

- **Measured thickness and strain of Si layer, thickness and alloy composition of SiGe layer, and thickness of Si cap layer**
- **Showed that interdiffusion of Si and Ge at Si/SiGe interfaces occurs during thermal annealing at 850°C**
- **Demonstrated that SiGe layer structures were degraded by device fabrication processes at T > 800°C**
  - → **Low temperature processing required**

Ge concentration in strained SiGe Layer over time at 850°C



SiGe strained layer thickness over time at 850°C



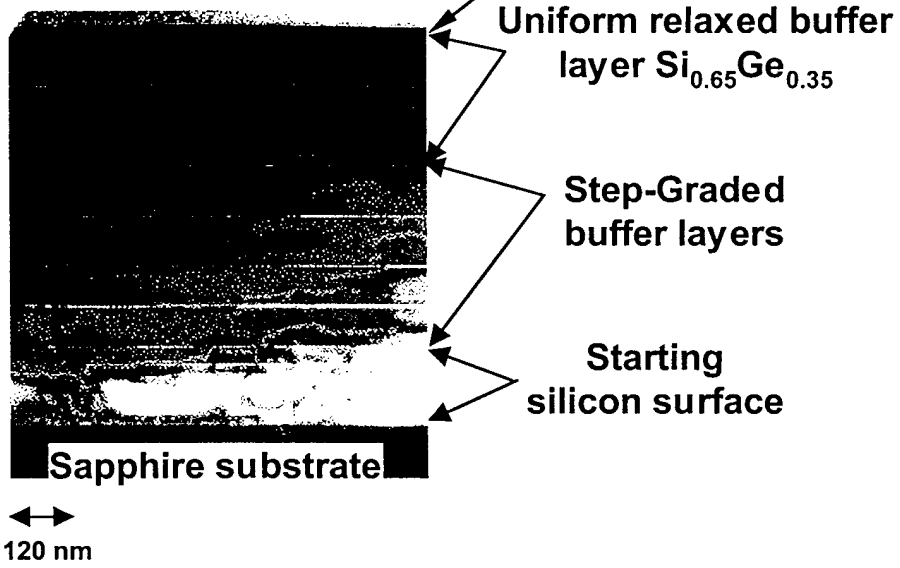
SPAWAR
Systems Center
San Diego

SiGe FETs on Silicon-on-Sapphire Substrates

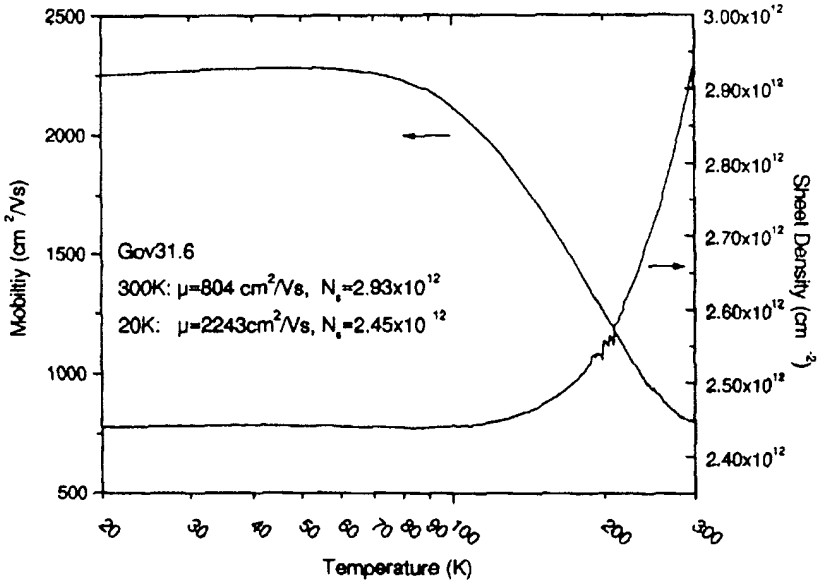
- **SiGe p-MOSFET Devices (Ge 20-30%)**
  - Hole mobilities 30 to 50% higher, up to 200 $cm^2/V\text{-}s$ (S.J. Mathew *et al.*, Tech. Dig. 1997 Device Research Conf. and Electron Device Letters 20, 173 (1999))
- **New Approach: p-MODFET Devices**
  - Room temperature hole mobilities up to 1050 cm^2/Vs in modulation doped structures on bulk Si (K. Ismail *et al.*, Appl./ Phys. Lett. 64, 3124 (1994))
  - f_t = 70 GHz for p-MODFETs on bulk Si (M. Arafa *et al.*, Electron Devices Lett. 17, 586 (1996))

SPAWAR
Systems Center San Diego

Modulation-doped p-FET layers on SOS



Mobility and Sheet Hole Density *vs.* T



Hole mobility (300K): 804 cm^2/V sec
Sheet hole density: 2.5 x 10^{12} cm^{-2}

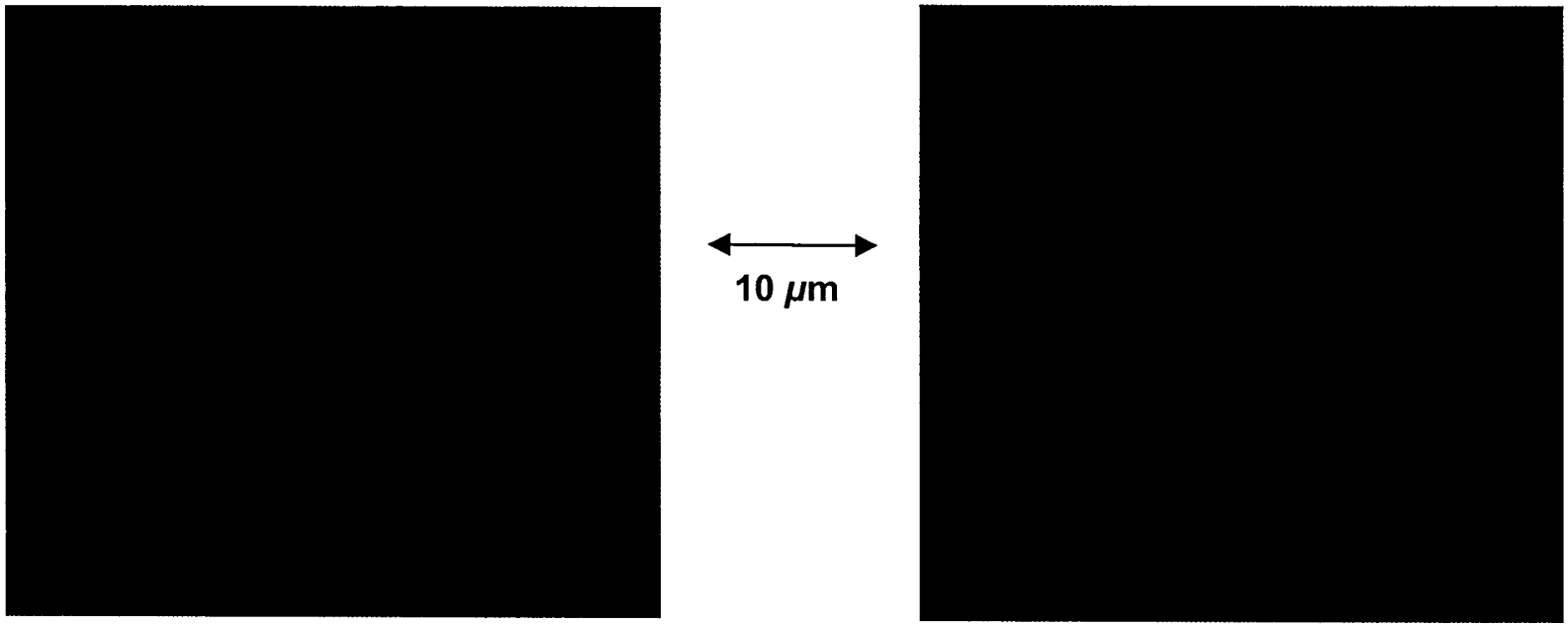
Active device layers are grown on top of a strain-relaxed SiGe buffer layer: total epi thickness approx. 1 micron

SPAWAR
Systems Center
San Diego

Nomarski image of p-MODFET wafer surface

Gov32.6: 4" Union Carbide SOS substrate

Gov32.8: 4" bulk silicon



- If not well-improved, large pits occur after SiGe growth at macro-twin defects in original SOS layer;
- Low defect density in SOS substrate required
- Wafer bonding methods have the potential to produce SOS substrates with
  - zero microtwin defects;
  - threading defect densities reduced by many orders of magnitude;
  - thin relaxed SiGe buffer layers on sapphire (required for fully depleted FETs)

SPAWAR
Systems Center
San Diego

Closing Thoughts

- TFSOS addresses present and long-term issues and needs in battery-operated wireless communication and S to K-band (~40 GHz) applications providing unique solutions for low power System-on-a-Single-Chip, integrating analog and digital functions
- Focus of present and near-term
  - Strained SiGe (>75% Ge) on SOS to achieve high μ_h
    - $1/f_{p\text{-SiGe/SOS}} < 1/f_{p\text{-SiGe/Si}}$
      $\Rightarrow$ Mixers with lower phase noise
    - f_t, f_{max} highest ever, for low power CMOS and high performance A/DCs
- SiGe p-FETs with greater or similar n-FET mobility will significantly reduce device size/chip area
  - higher CMOS performance products (f_t, f_{max} > 100-200 GHz), for reduced system cost, using industrial IC infrastructure
- QHD simulation predicts similar device transconductance for SiGe on SOS FETs and AlGaAs/GaAs HEMTs (Prof. David Ferry, ASU, Seminar UCSD, May 26, 1998)
- World highest hole mobility (804 $cm^2/V.sec$ @300 K) measured on modulation-doped p-FET structure on TFSOS substrate
- MOSIS accepts TFSOS designs

SPAWAR
Systems Center
San Diego

The Future

- Extend performance of silicon technology to K-band, benefiting from established industrial infrastructure resulting in lower cost

- TFSOS technology for digital and analog devices
  - —10 times lower power x delay product than conventional bulk technologies benefits in, e.g.,
    - —Real-time sensor information processing
    - —Radar image processing
    - —Digital communication
  - —Another factor of 5 reduction with low V_{dd}
    - —Deployable/Unattended situation awareness systems
    - —Extended operation of all battery-powered systems
  - —10x greater immunity to SEU which benefits
    - —All space based electronics

- TFSOS, a technology to implement advanced components, such as A/D converters, and single chip wireless communication systems

SPAWAR
Systems Center
San Diego

The Future

- Extend performance of silicon technology with SiGe/TFSOS CMOS to K-band, benefiting from established industrial infrastructure resulting in lower cost, advanced components, such as A/DCs and wireless communication functions

- TFSOS, implementing a low power, lower cost, high performance technology for application to:
  - Space based electronics
  - Image processing
  - Digital communication
  - Extended operation battery-powered systems
  - Other commercial/military systems

SPAWAR
Systems Center
San Diego

What all the wise promised
has not happened,
and what all the damned fools said
would happen has come to pass

William Lamb
Second Viscount Melbourne
(from Lord Melbourne, 1834)