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Attn: Gerald L. Witt.
AFOSR/NE
801 North Randolph Street, Room 732
Arlington, VA 22203-1977
Tel: (703)-696-8571
Fax: (703)-696-8481

DR. UMESH K. MISHRA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
UNIVERSITY OF CALIFORNIA
SANTA BARBARA, CA 93106-9560
Tel : (805)-893-3586

Signature: Umesh K. Mishra

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Dr. Umesh K. Mishra

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Research under the PRET program has covered a varied range of materials and device applications. Early work was directed mostly toward understanding and implementing low-temperature grown (LTG) GaAs into field-effect transistors (FETs) providing increased breakdown voltages and a reduced noise performance. In recent years the research has been redirected into the newly emerging area of oxides and oxide electronics.

Oxide produced from the steam oxidation of aluminum containing semiconductors has found widespread applications in the area of opto-electronics, specifically in vertical cavity lasers. In the research performed under the PRET program, additional applications in electronics, such as an insulating buffer in GaAs-On-Insulator (GOI) technology, as a lattice-engineered-substrate (LES), and most recently as a current aperture in high-speed heterojunction bipolar transistors (HBTs), have been implemented and studied. All of which have been shown, or potentially show, improved performances in devices, or introduced as yet unseen applications in material science.

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1. Overview

In the past year research efforts under the PRET program fall under 4 main categories.

1. Lattice engineered substrates using lateral oxidation of AlAs(Sb).
2. AlInAs/GaInAs Metamorphic HEMTs on GaAs substrates.
3. GaAs on Insulator pHEMTs.
4. LT GaAs Based Optoelectronic Devices – 1.55 μm Waveguide Photodetector and THz Photomixers

• Lattice engineered substrates using lateral oxidation of AlAs(Sb) to generate epitaxial substrates with lattice constants, which are between those of commercially available binary III-V substrates. Work on GaAs based lattice engineered substrates was mainly concentrated in two areas. The first was the process of strain relaxation during the process of lateral oxidation of AlAs. The second was the characterization of MBE growth of $Al_{1-x}Ga_xAs_{1-y}Sb_y$ materials on lattice-engineered substrates. The AlGaAsSb material system has many advantages for the fabrication of long-wavelength (1.3-1.55 μm) optoelectronic devices, when compared to the conventional AlGaInAs and InGaAsP materials. This work is discussed in section 2.

• Formation of Sb interlayer during the oxidation of AlAsSb lattice-matched to InP is a major issue which needs to be addressed for the development of lattice-engineered substrate technology on InP substrates. These efforts are summarized in section 3.

• Work on AlInAs/GaInAs Metamorphic substrates was done at HRL Laboratories, Malibu. AlInAs/GaInAs Metamorphic HEMTs on GaAs substrates with dc and rf characteristics that rival those grown on InP substrates have been demonstrated. This work is discussed in section 4.

• Work on Metamorphic Buffer layers was also started at UCSB. The main objective of this work is to develop a long wavelength photoreceiver on GaAs substrates and is discussed in section 5.

• In 1997-1998 work on the PRET program was mainly related to GaAs on Insulator (GOI) MESFETs. In the past year, the efforts in this area dealt with the development of a GOI pHEMT and are discussed in section 6.

• Low-temperature grown GaAs (LT-GaAs) can absorb long wavelength light (1~1.6 μm) by mid gap defect centers or As precipitates. A novel n-i-n (i-LT-GaAs) photodetector was used to study the carrier transport in LT-GaAs. Compared to a conventional p-i-n structure at the different

bias, a higher efficiency is obtained with high-speed performance. These results are discussed in Section 7.

- Terahertz radiation can be generated by optical heterodyne conversion in a LT GaAs MSM photodetector. The low thermal conductivity of LT GaAs is significantly low when compared to stochiometric GaAs and affects the heat flow in a photomixer. Thermal failure of LT GaAs photomixers was investigated. This work is discussed in Section 8.

2. GaAs Based Lattice Engineered Substrate Technology Using Lateral Oxidation of AlAs:

2.1 Introduction

Conventional III-V semiconductor devices are usually grown on the four main commercially available III-V substrates namely, GaAs, InP, GaP and GaSb. The performance of many optoelectronic devices has often been constrained because only alloy systems that are nearly lattice matched to these substrates can be used for device applications. In many cases the performance of the device can be improved by using a material system that is lattice matched to a substrate with a lattice constant between these commercially available substrates. This is particularly true for long wavelength lasers grown on InP substrates. Also the manufacturing costs can be reduced by growth on a large area cheaper substrate like GaAs when compared to InP or GaSb.

Many approaches have been investigated to overcome the limitations imposed by binary substrates. These include using graded buffer layers to transform the lattice constant from the binary substrate to the desired value. Recently the use of twist-bonded compliant substrates has also been investigated to solve this problem. Another solution is the use of InGaAs or InAsP ternary substrates of various compositions.

We demonstrate an approach that utilizes the process of relaxation of a coherent hypercritical thickness ($h > h_{critical}$) strained semiconductor over-layer (InGaAs) in direct contact with an oxidizing Al-containing semiconductor (e.g. AlAs or AlGaAs). The porous and reactive interface between the strained semiconductor overlayer and the oxide enables extensive plastic strain relaxation due to efficient dislocation motion without interaction and generation of new dislocations. This results in the formation of a relaxed InGaAs template *(Lattice Engineered Substrate)* that is epitaxially decoupled from the underlying GaAs substrate, while still mechanically supported by the substrate. Subsequent regrowth on this template (lattice engineered substrate) enables the fabrication of relaxed low threading dislocation density InGaAs buffers and device structures.

Work on lattice-engineered substrates was commenced on the PRET program in the year 1997-1998. Initial experiments led to the use of LT-GaAs buffer layers and AlAs defect diffusion barrier in the templates to enable the growth optical quality materials on lattice-engineered

substrates. The experiments were done on templates with $In_{0.2}Ga_{0.8}As$ epitaxial layers. In the past year the process of strain relaxation during lateral oxidation of $AlAs_{1-y}Sb_y$ was studied in detail by varying the initial strain in the $In_xGa_{1-x}As$ template and the nature of the oxide/$In_xGa_{1-x}As$ interface. Also growth of Sb based materials on lattice-engineered substrates was investigated for the fabrication of long-wavelength (1.3 μm) optoelectronic devices.

The process of strain-relaxation in lattice-engineered substrates is explained in the following section. This is followed by a discussion of various factors affecting the process of strain relaxation and the various techniques used employed to improve the strain relaxation efficiency in the $In_xGa_{1-x}As$ templates upon lateral oxidation of the underlying $AlAs_{1-y}Sb_y$ layers. This section ends with a discussion of growth and structural and optical characterization of Sb based optoelectronic materials on lattice-engineered substrates.

2.2 Strain Relaxation Mechanism in Lattice-Engineered Substrates

Figure 2.1 explains the difference in strain relaxation mechanisms in conventional substrates and lattice-engineered substrates. In conventional heteroepitaxy (for example, InGaAs growth on a GaAs substrate) formation of misfit dislocation segments by the movement of

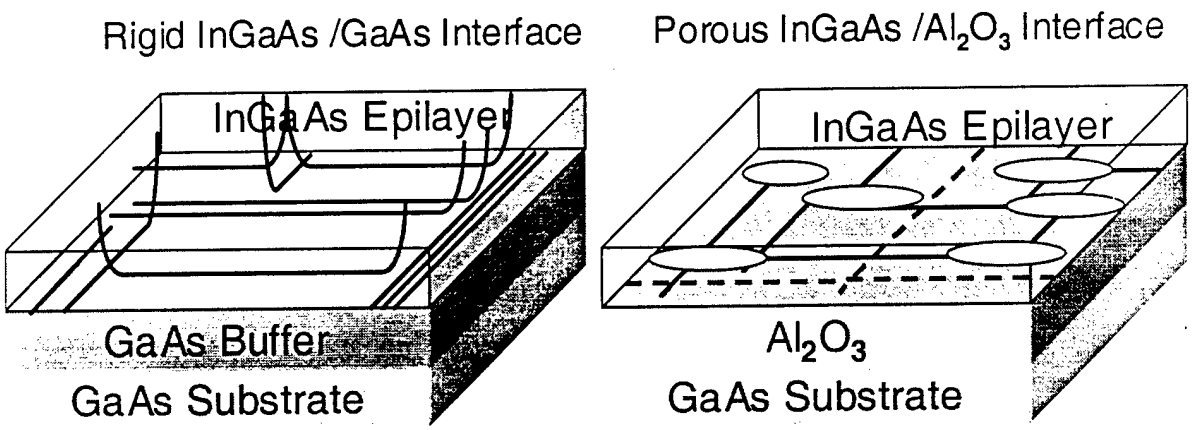


Figure 2.1: Strain relaxation mechanisms in conventional and lattice-engineered substrates

threading dislocation ends relieves strain in the lattice-mismatched epilayer. However existing clusters of other misfit dislocations may block this motion. Therefore the existing dislocations cannot relieve the mismatch strain building up in the growing epitaxial layer. Hence generation of additional dislocations is required to relieve the strain in the epilayer. Thus a large number of dislocations are generated to accommodate the lattice mismatch. Conventional approaches like

graded buffers reduce the threading/misfit dislocation interaction by vertically distributing the misfit dislocation segments over a large layer thickness. In a lattice-engineered substrate, enhanced threading dislocation movement at the template/oxide interface that is porous and has voids relieves the strain in the epitaxial template. Also core regions of existing misfit dislocations may be reactively removed during the process of lateral oxidation. As a result there are fewer barriers to increasing misfit dislocation length, which prevents the generation of additional threading dislocations.

Plan-view transmission electron microscopy (PVTEM) has been used to characterize the interface between oxidized AlAs and lattice-mismatched $In_{.2}Ga_{.8}As$. The sample growth structure shown in Fig. 2.2 was patterned and oxidized at 450°C for one hour to a distance of 90μm.

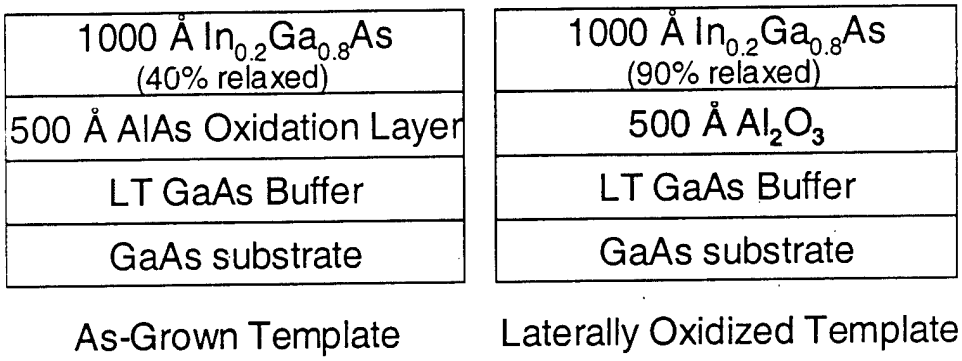


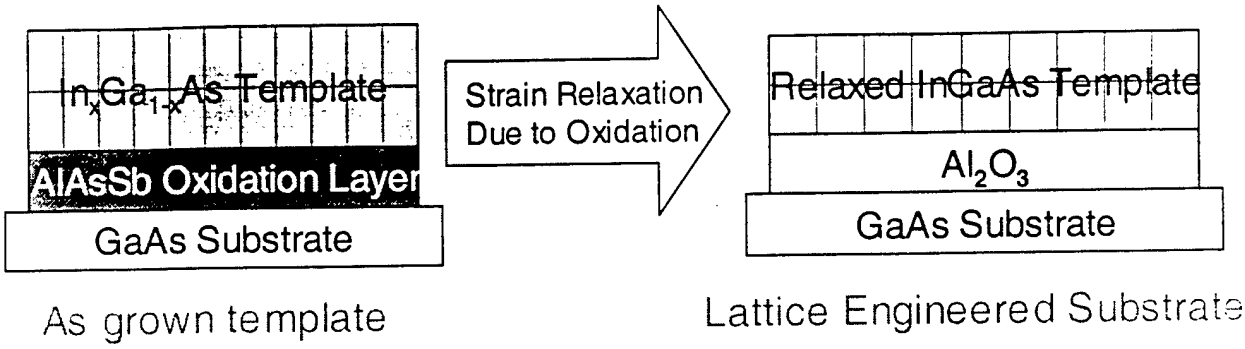
Figure 2.2: Growth structure of GaAs-based lattice engineered substrate under investigation by PV TEM.

Figure 2.3 shows a strong-beam **g**=220 image of an area including the oxidation front as viewed along the substrate normal. In the region not yet oxidized, there is a dense network of misfit dislocations oriented along the two orthogonal <110> directions in the (001) plane. The oxidation front is indicated by the transition between the high and low misfit dislocation density areas. The misfit dislocation density has been reduced from 1.67×10^5/cm in the unoxidized region to less than ~5×10^3/cm in the oxidized region. At the same time, this sample was previously measured to have reduced its residual misfit strain from 40% before oxidation to 90% after oxidation at 450°C. This indicates the reduction in strain in the InGaAs layer without the creation of dislocations. This has not been observed in other compliant substrate approaches. However, reliable measurements of the threading dislocation density have not been possible since the density is quite low. Measurements via other methods are ongoing.

*Figure 2.3: Plan-view, bright field **g**=220 TEM micrograph of GaAs-based, 20% InGaAs lattice-engineered substrate, showing oxidized and unoxidized areas of LES. The misfit dislocation density has been reduced from 1.67x10^5/cm in the unoxidized region to less than ~5x10^3/cm in the oxidized region.*

2.2 Factors affecting strain relaxation during lateral oxidation

The process of strain relaxation during lateral oxidation is studied by varying the strain in the as-grown $In_xGa_{1-x}As$ template and by varying the nature of the $In_xGa_{1-x}As$/oxide interface. Changing the Indium composition in the template varies the mismatch strain in the template and the initial misfit dislocation density, whereas varying the oxidation temperature controls the nature of the InGaAs/oxide interface. The goal is to minimize the relaxation of the as-grown InGaAs template and maximize the relaxation after the process of lateral oxidation as summarized in Fig. 2.4.



Strain relaxation affected by:

Built-in (initial) Strain in InGaAs
Oxidation Process

- Vary Indium composition
- Vary oxidation temperature
- Vary Sb content in $AlAs_{1-x}Sb_{1-x}$

Goal : Minimize relaxation of as-grown template
Maximize relaxation after oxidation

Figure 2.4: Factors affecting strain relaxation during lateral oxidation of AlAs

The epitaxial structures investigated consisted of strained $In_xGa_{1-x}As$ template layers grown on AlAs oxidation layer on a n-type GaAs substrate in a Varian Gen II molecular beam epitaxy system. After oxide desorption from the GaAs substrate, a high temperature GaAs buffer was grown at 580 °C. This was followed by a low-temperature (LT) GaAs buffer grown at 250 °C and a 500 Å AlAs oxidation layer grown at 650 °C. The LT GaAs buffer was grown beneath the AlAs layer to assist in oxidation. The strained $In_xGa_{1-x}As$ layers were grown directly on the AlAs oxidation layers. The thicknesses of the different $In_xGa_{1-x}As$ layers used were 1000 Å $In_{0.2}Ga_{0.8}As$ grown at 430 °C, 760 Å $In_{0.3}Ga_{0.7}As$ grown at 400 °C and 480 Å $In_{0.4}Ga_{0.6}As$ grown at 300 °C respectively. These thicknesses are roughly 20 times the Matthews-Blakslee critical thickness of $In_xGa_{1-x}As$ (x=0.2, 0.3, 0.4) on GaAs substrate. The $In_xGa_{1-x}As$ template layers were grown at low temperature to minimize the formation of threading dislocations and maintain a two-dimensional growth-front. Note that the growth temperature has to be progressively lowered with increasing lattice mismatch to suppress formation of threading dislocations and prevent islanding. Further lowering of growth temperature is undesirable as it results in a rough surface morphology due to the low mobility of atoms on the growing surface. The $In_xGa_{1-x}As$ layers were capped with a 30 Å AlAs etch stop layer and 200 Å GaAs cap layer to protect it during oxidation.

After growth the substrate was patterned using photolithography and reactive ion etching into 100 μm x 100 μm square mesas to enable lateral oxidation of the AlAs layers. Lateral oxidation was carried out in a furnace with steam generated by bubbling N_2 gas through water maintained at 90 °C. The oxidation temperatures of 410, 430 and 450 °C were used and the oxidation time was chosen so as to completely oxidize the mesas. To ascertain whether strain relaxation is caused by lateral oxidation only and not by thermal annealing, a set of the patterned samples were annealed under same conditions, but in a non-oxidizing environment. The degree of strain relaxation was determined by X-Ray diffraction of as-grown, oxidized and annealed templates.

Figure 2.5 shows the extent of strain relaxation of the as grown and oxidized/annealed $In_xGa_{1-x}As$ templates as a function of oxidation/annealing temperature. As the Indium composition is increased, the relaxation of the as-grown epitaxial layers increases due to higher lattice-mismatch. This implies that the misfit dislocation density at the $In_xGa_{1-x}As$/AlAs interface increases with the Indium composition. The strain in the $In_xGa_{1-x}As$ template is relaxed after oxidation with the degree of relaxation increasing with oxidation temperature.

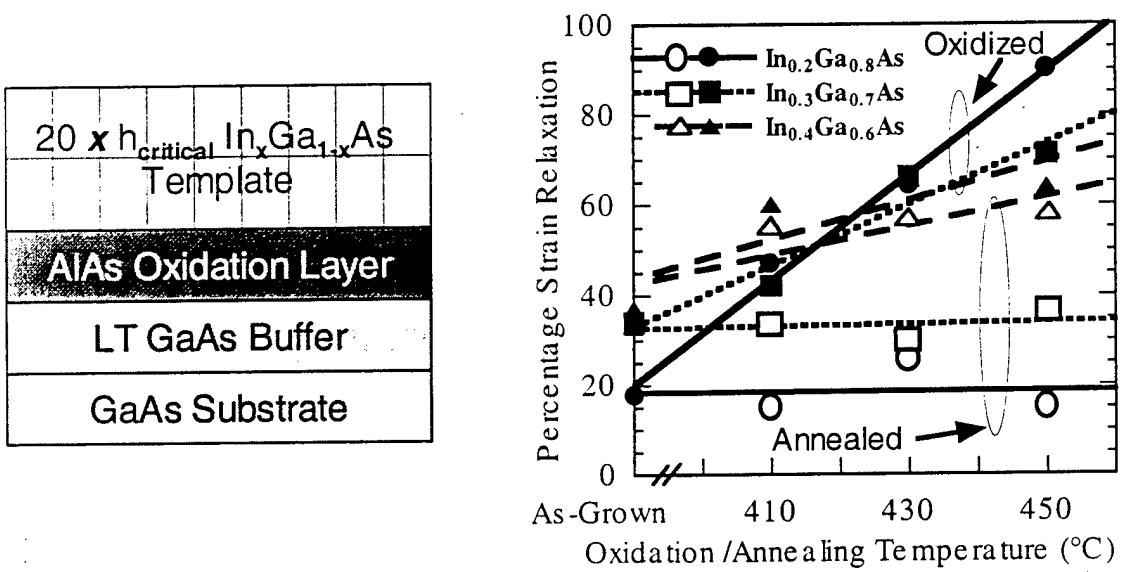


Figure 2.5: Strain Relaxation as a function of oxidation temperature for various $In_xGa_{1-x}As$ templates

During the process of AlAs oxidation, strain relaxation can occur in because of two different mechanisms. The first is the increased thermal energy available for threading

dislocation movement; the other is change in the nature of the $In_xGa_{1-x}As/Al_2O_3$ interface. Data from the published literature for low Indium composition $In_xGa_{1-x}As$ epilayers indicates that strain relaxation due to thermal annealing occurs only at temperatures exceeding 650-700 °C. Hence at oxidation temperatures of 410-450 °C, the thermal energy in the system appears to be insufficient to substantially enhance threading dislocation motion. This is corroborated by the fact that no strain relaxation is observed for the $In_{0.2}Ga_{0.8}As$ and $In_{0.3}Ga_{0.7}As$ structures annealed under the same conditions as seen in Fig. 2.5. However in the case of $In_{0.4}Ga_{0.6}As$ structures relaxation is observed. This is due to the combination of high excess stress due to 2.8 % lattice mismatch, oxidation/annealing temperatures that are 100-150 °C higher than growth temperatures. On the other hand for the $In_xGa_{1-x}As$ (x=0.2, 0.3) structures the oxidation and annealing temperatures are nearly the same as the growth temperature. It has been reported previously that conversion of AlAs to Al_2O_3 results in volume contraction. Since the dislocation glide velocity is directly proportional to the effective stress, it is proposed that the stress generated at the oxidation front during volume contraction increases the threading dislocation glide velocity. Also from Fig. 2.5, it is observed that strain relaxation can be greatly enhanced by increasing the oxidation temperature from 410 °C to 450 °C. Since the available thermal energy for threading dislocation glide does not increase appreciably for such a small change in temperature and effective stress due to volume contraction does not change appreciably, the only possible reason for the enhanced strain relaxation is the change in the nature of the InGaAs/oxide interface. Oxidation kinetics of AlAs change from a diffusion limited mechanism to a reaction-limited mechanism as the oxidation temperature is increased from 410 °C to 450 °C. It is therefore proposed that the increase in strain relaxation with oxidation temperature is due to the increased porosity of the InGaAs/oxide interface, which reduces the misfit dislocation interaction. Also reactive removal of misfit dislocation cores is enhanced at higher oxidation temperatures. This is verified by the TEM analysis of the $In_xGa_{1-x}As/Al_2O_3$ interface, which shows the absence of strain contrast associated with misfit dislocations. Prior to oxidation, we observe strain contrast associated with the misfit dislocations that give rise to partial relaxation.

The role initial dislocation density on the efficiency of relaxation is clear if the slope of the strain relaxation curve is examined. The barrier to threading dislocation movement is higher for higher Indium composition templates due to higher initial misfit dislocation density. Hence

strain relaxation after oxidation is less efficient for the $In_{0.4}Ga_{0.6}As$ structure. The trend also points towards pathways to increase the degree of strain relaxation for higher Indium composition templates. Reducing the misfit dislocation density at the as-grown InGaAs/AlAs interface can enhance strain relaxation. An alternate way is to change the nature of the oxide and the InGaAs/oxide interface itself. Besides increasing the oxidation temperature, this can be achieved by addition of Sb (upto 10 %) to AlAs. Addition of Sb to AlAs has demonstrated a significant change in the oxidation mechanism and the InGaAs/oxide interface.

2.3 Improving Strain Relaxation Efficiency in Lattice-Engineered Substrates

As discussed in the previous section, one of the ways to improve the strain relaxation efficiency is to reduce the misfit dislocation density at the $In_xGa_{1-x}As$/AlAs interface in the

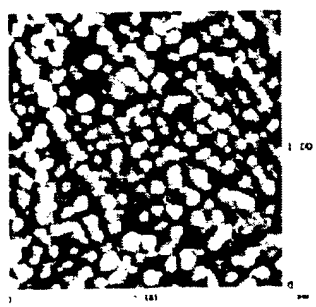
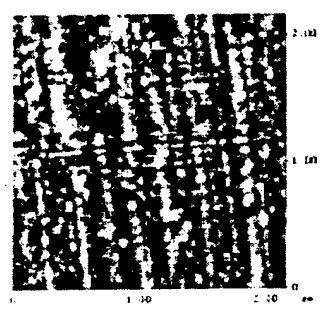
T_{growth}	Strain Relaxation (As-Grown)	AFM Scan	RMS Surface Roughness
430 °C	48 %		7 Å
400 °C	34 %		4 Å

Figure 2.6: Effect of growth temperature reduction on strain relaxation and surface morphology of as-grown $In_{0.3}Ga_{0.7}As$ templates.

template. This is achieved by reducing the $In_xGa_{1-x}As$ template growth temperature. Figure 2.6 illustrates the effect of reduction of growth temperature in the case of $In_{0.3}Ga_{0.7}As$ templates that are 20 times the critical thickness. Reduction in the growth temperature from 430 °C to 400 °C, reduces the strain relaxation of the as-grown sample, also the rms surface roughness reduces from 7 Å to 4 Å.

Figure 2.7 compares the strain relaxation as a function of oxidation temperature for these two templates. The higher efficiency of strain relaxation as seen in the sample grown at low temperature is a direct consequence of the lower misfit dislocation density in the template grown at lower growth temperature. Also the lower surface roughness is results in better regrowth of the desired epitaxial layers.

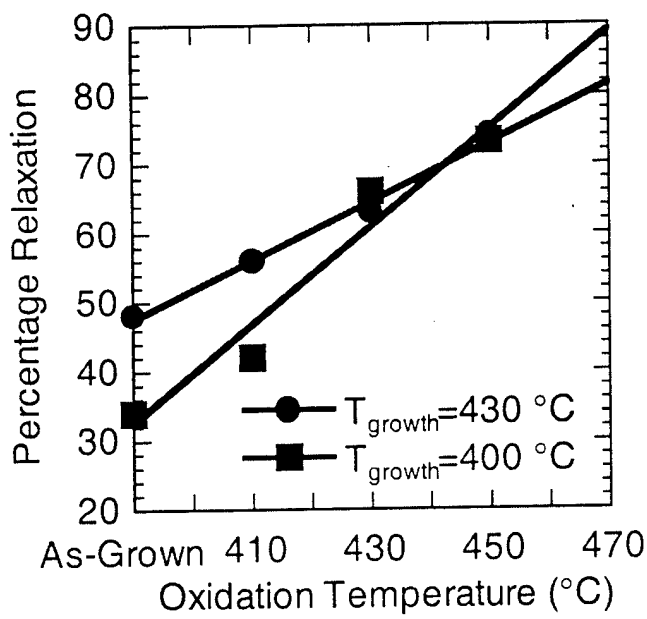


Figure 2.7: Comparison of strain relaxation as a function of $In_xGa_{1-x}As$ growth temperature

Another approach to increase the strain relaxation efficiency is to change the nature of the $In_xGa_{1-x}As$/oxide interface itself. This is achieved by addition of Sb (upto 10 %) to the AlAs oxidation layer. An important consequence of addition of Sb to AlAs is the segregation of Sb during lateral oxidation, which results in an increase in the porosity of the oxide. This changes

the oxidation kinetics from diffusion limited to reaction rate limited. Thus oxidation of larger size mesa is possible, as the oxidation reaction is no longer limited by the diffusion of the reactants through the oxide.

To investigate the effect of Sb addition on the strain relaxation process, $In_{0.2}Ga_{0.8}As$ template layers were grown on AlAsSb oxidation layers with Sb compositions of 0, 7 and 10%. Figure 2.8 shows the effect of Sb addition on the oxidation kinetics and the strain relaxation process during lateral oxidation.

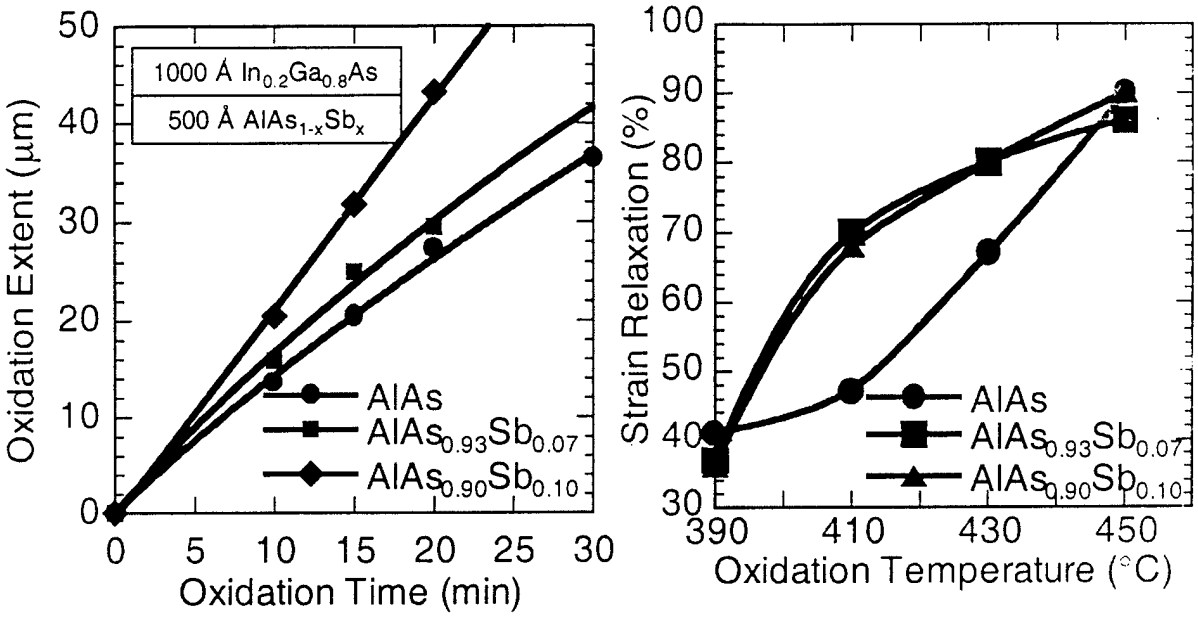


Figure 2.8: a) Lateral Oxidation extent as a function of time for $AlAs_{1-x}Sb_x$ layers with varying Sb composition. Oxidation Temperature = 410 °C
b) Strain relaxation as function of oxidation temperature for various $In_{0.2}Ga_{0.8}As$ templates with $AlAs_{1-x}Sb_x$ oxidation layers

As seen from Fig. 2.8, addition of Sb to AlAs improves the strain relaxation efficiency at a given oxidation temperature when compared to AlAs. This is as mentioned before is a consequence of increased porosity of the oxide.

To summarize the previous sections, we studied in detail the process of strain relaxation of InGaAs templates during lateral oxidation for various AlAsSb oxidation layers. For the above experiments it can be concluded that to maximize the strain relaxation in the InGaAs template after lateral oxidation of the underlying AlAs layer, it is necessary to minimize the strain

relaxation of the as-grown InGaAs template. This is achieved by lowering the InGaAs growth temperature. The strain relaxation efficiency can also be improved by changing the porosity of the oxide and the nature of the InGaAs/oxide interface. This can be achieved by the use of higher oxidation temperature and the addition of Sb to the AlAs oxidation layer. Since the process of strain relaxation is driven by excess stress present in the InGaAs template, it is not possible to achieve complete strain relaxation. This is because as the template relaxes the excess stress in the template that acts a driving force is reduced. In the following sections, the structural and optical characterization of Sb based materials grown on lattice-engineered substrates will be discussed.

2.4 Structural Characterization of Epitaxial Layers grown on Lattice Engineered Substrates

The GaAs based lattice-engineered substrate technology enable the growth of material systems with lattice constants between GaAs and InP. The various III-V material systems that can be grown are $Al_xGa_yIn_{1-x-y}As$, $Al_xGa_{1-x}As_{1-y}Sb_y$, $Al_xGa_yIn_{1-x-y}P$ and $In_xGa_{1-x}As_{1-y}P$. The material systems enable the growth of long-wavelength optoelectronic devices on GaAs based lattice-engineered substrates and have many advantages compared to long-wavelength optoelectronic materials grown on InP substrates. Prior to the recent installation of a valved phosphorus source at UCSB, it was possible to grow only $Al_xGa_yIn_{1-x-y}As$ and $Al_xGa_{1-x}As_{1-y}Sb_y$ based materials on lattice-engineered substrates.

Thick, high bandgap AlGaInAs and AlGaAsSb epitaxial layers are used as cladding layer in long wavelength optoelectronic devices. It is difficult to grow high quality AlGaInAs epitaxial layers by MBE due to the large difference in the mobility of Al and In atoms on the growing surface. On the other hand growth of AlGaAsSb is easier. This is due to comparable surface mobility of Al and Ga cations on the growing surface and the surfactant effect of the Sb. The use of valved As and Sb cells enables accurate composition control of the AsSb based epitaxial layers. We have investigated the growth of GaAsSb layers on lattice-engineered substrates as function of As/Sb fluxes and growth temperatures. Figure 2.9 illustrates the variation of Sb composition in $GaAs_{1-x}Sb_x$ epitaxial layers as a function of As, Sb fluxes and growth temperatures. As seen from the figure, at higher temperatures, the incorporation efficiency of Sb is reduced to Sb desorption from the growing surface.

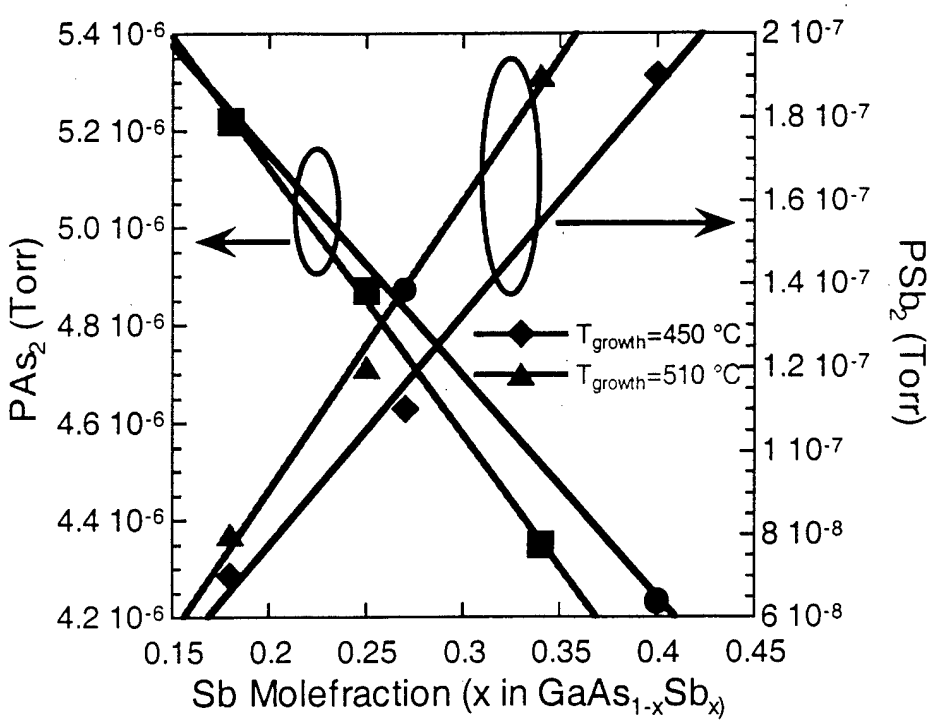


Figure 2.9: Variation of Sb mole fraction in $GaAs_{1-x}Sb_x$ layers grown on lattice-engineered substrates as function of As, Sb fluxes and growth temperature

The growth temperature also affects the surface morphology of the $GaAs_{1-x}Sb_x$ epitaxial layers grown on lattice-engineered substrates. As seen from Figure 2.10, at higher growth temperatures (510 °C), the RMS surface roughness of the layer increases with Sb composition. However at lower growth temperatures (450 °C), the RMS surface roughness is independent of the Sb composition. RMS surface roughness measurements on $Al_yGa_{1-y}As_{0.78}Sb_{0.22}$ epitaxial layers (not shown here) grown on lattice-engineered substrates showed that the surface roughness is low (<10 Å) and is independent of the Al composition. Thus the AlGaAsSb is a desirable material system for the implementation of long wavelength optoelectronic devices on GaAs based lattice-engineered substrates.

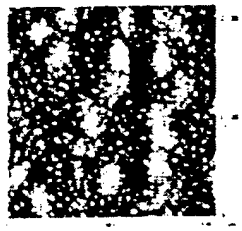
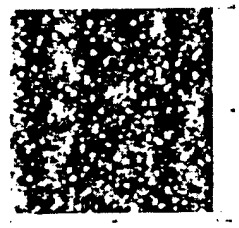
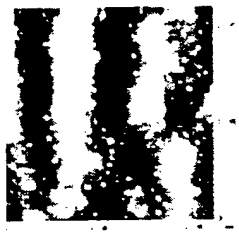
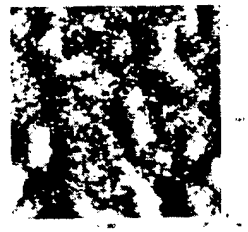
	T_{growth} =510 °C	T_{growth} =450 °C
$GaAs_{0.85}Sb_{0.15}$	 RMS Roughness = 8.7 Å	 RMS Roughness = 5.1 Å
$GaAs_{0.75}Sb_{0.25}$	 RMS Roughness = 20 Å	 RMS Roughness = 5.6 Å

Figure 2.10: Surface Morphology of $GaAs_{1-x}Sb_x$ layers grown on lattice-engineered substrates as a function of Sb composition and growth temperature.

2.5 Optical Characterization of 1.3 μm Quantum wells grown on Lattice Engineered Substrates

One of the major applications of GaAs based lattice engineered substrates is the fabrication of 1.3 μm lasers on GaAs substrates. Cost-effective high speed, short distance optical communication networks will be enabled by the fabrication of temperature-stable 1.3 μm lasers on large area GaAs substrates. At present these devices are grown on InP substrates using the InGaAsP/InP material systems. In addition to substrate size limitations, lasers based on the InGaAsP/InP material system are not temperature-stable due to the low band-offset. Recently high temperature (210 °C) operation of 1.3 μm InGaP/InGaAs lasers on InGaAs ternary substrates was demonstrated. However this approach is currently limited by the ternary InGaAs substrate size and composition control of the ternary substrate. GaAs based Lattice Engineered Substrates are a cost-effective viable alternative to InGaAs ternary substrates.

Current long-wavelength lasers are grown mainly on InP substrates. Due to the high lattice mismatch these devices cannot be grown on a GaAs substrate. Long-wavelength (1.3 μm) lasers with gain regions having deeper quantum wells can be implemented in material systems with a lattice constant of 5.75 Å. The lattice constant of 5.75 Å is between that of a GaAs substrate (5.653 Å) and InP substrate (5.8686 Å). It can be achieved by a using a GaAs based lattice-engineered substrate or an InGaAs ternary substrate. Figure 2.11 compares the band-offsets of various quantum wells that can be used for 1.3 μm emission. The barrier layers are lattice-matched to the corresponding substrate and the 80 Å thick well is compressively strained with a 1.4 % lattice mismatch.

On a lattice-engineered substrate with a lattice constant of 5.75 Å the possible active regions are $Al_{0.2}Ga_{0.8}As_{0.78}Sb_{0.22}/GaAs_{0.58}Sb_{0.42}$, $In_{0.25}Ga_{0.75}As/In_{0.42}Ga_{0.58}As$ and $In_{0.7}Ga_{0.3}As_{0.08}P_{0.92}/In_{0.46}Ga_{0.54}As$. On an InP substrates the possible active regions are $In_{0.87}Ga_{0.03}As_{0.29}P_{0.71}/In_{0.98}Ga_{0.02}As_{0.48}P_{0.52}$ and $Al_{0.32}Ga_{0.16}In_{0.52}As/Al_{0.16}Ga_{0.10}In_{0.74}As$.

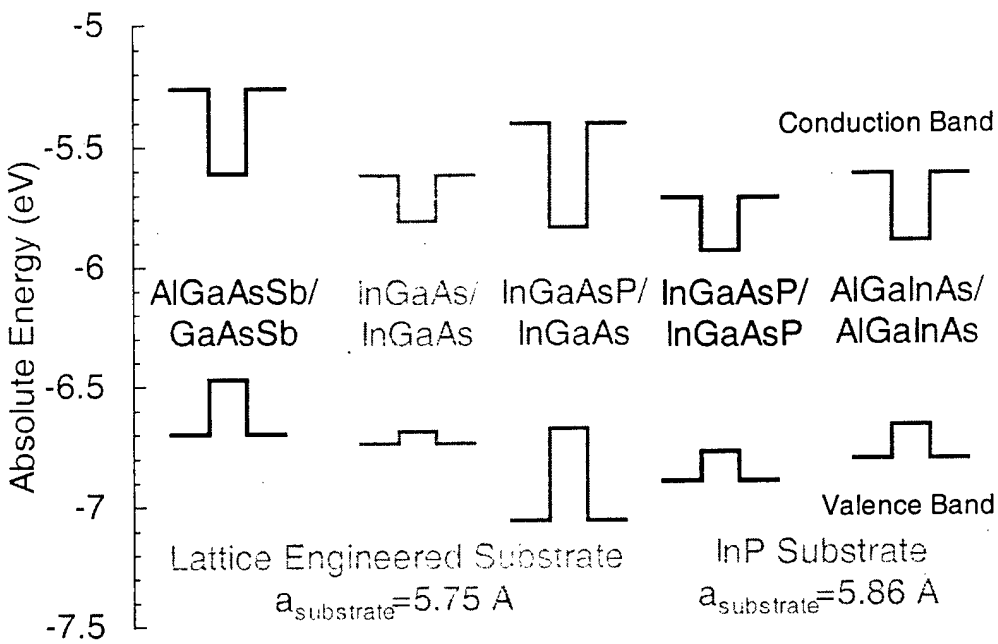


Figure 2.11: Conduction and Valence Band offsets of 1.3 μm quantum wells on Lattice Engineered Substrate and InP substrate

As seen from Fig. 2.11 higher band-offsets can be achieved in quantum wells grown on lattice-engineered substrates when compared to those grown on InP substrates. This has two-fold

advantages. The first is that deeper quantum wells have higher optical gain. The other is that electrons confinement is higher in a deep quantum well. Electron leakage from the active region into the SCH and cladding regions limits the operating temperature range of long-wavelength lasers. A quantum well with higher band-offsets will minimize electron leakage and hence enable high temperature operation. In addition a lattice-engineered substrate enables the growth of a high bandgap cladding layer like $Al_{0.8}G_{0.2}As_{0.78}Sb_{0.22}$ or InGaP. On the other hand the highest possible bandgap achievable on an InP substrates is 1.4 eV for AlInAs. Thus the GaAs based lattice-engineered substrate technology is attractive for the fabrication of high-performance uncooled long-wavelength lasers.

As a first step towards the fabrication of 1.3μm lasers on GaAs based lattice engineered substrate arsenide and arsenide-antimonide based quantum wells were grown. Figure 2.12 shows layer structure and room temperature PL spectrum of 1.3 μm MQW active region with $In_{0.25}Ga_{0.75}As$ barriers and $In_{0.42}Ga_{0.58}As$ quantum well.

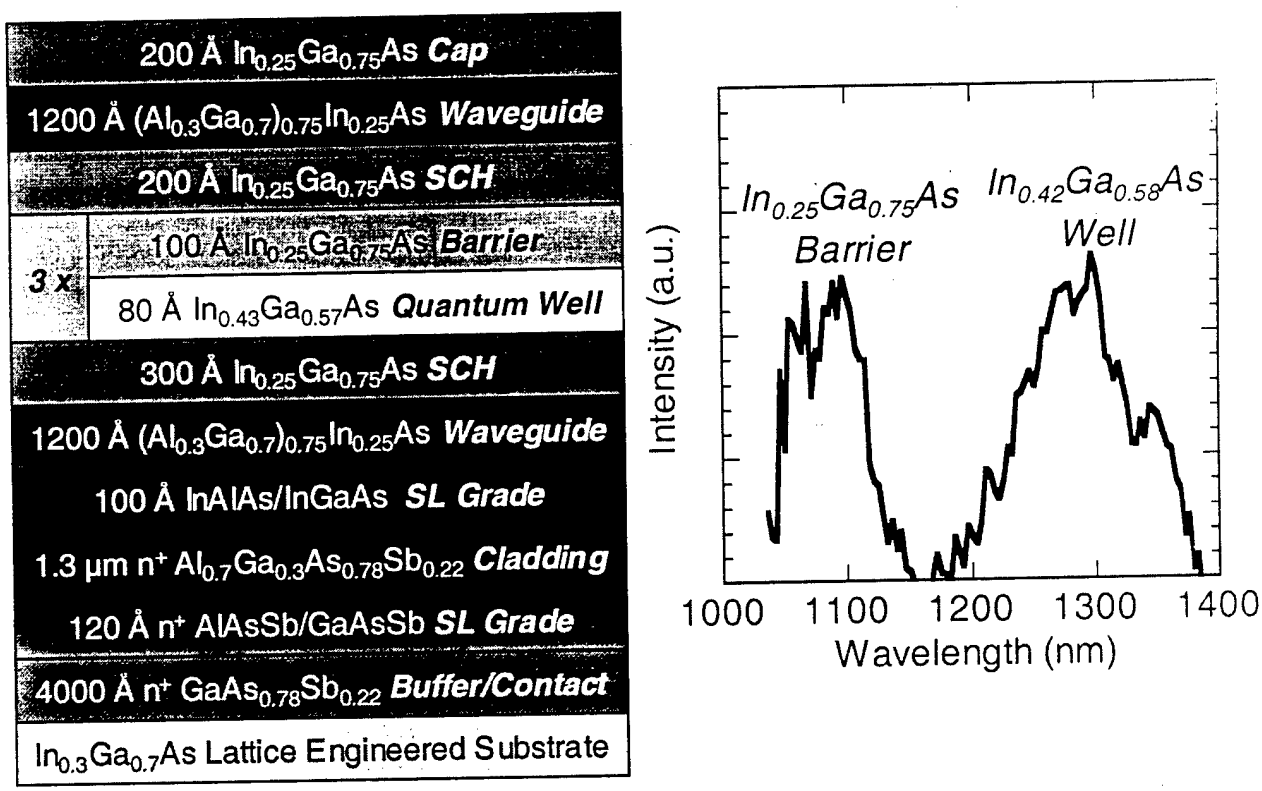


Figure 2.12: Layer structure and Room temperature PL spectrum of 1.3 μm arsenide based quantum well

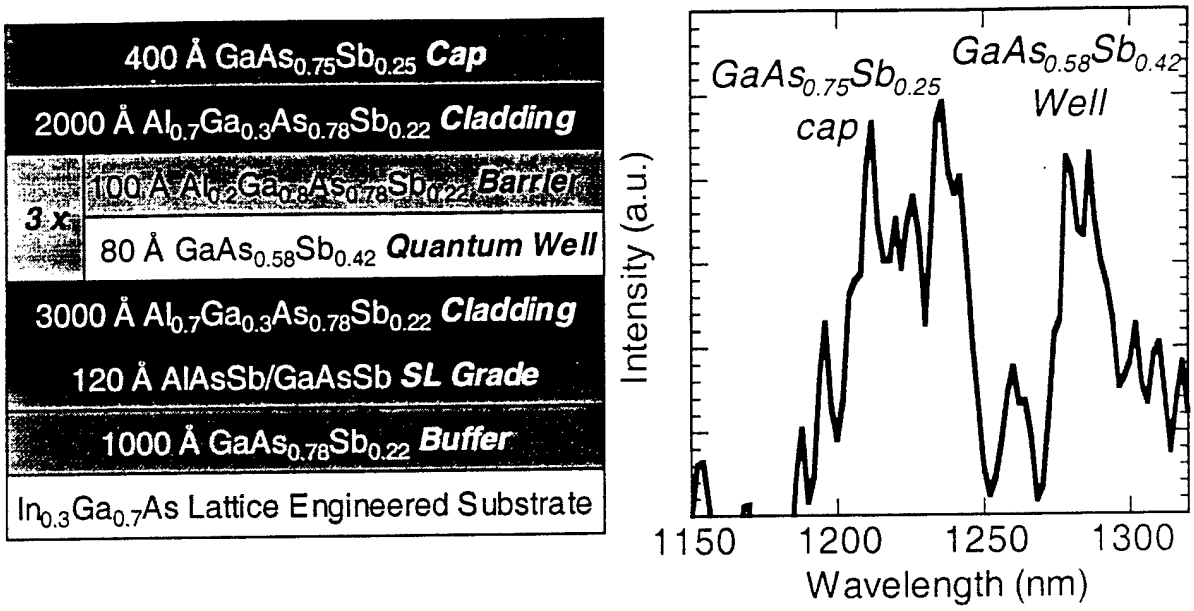


Figure 2.13: Layer structure and Room temperature PL spectrum of 1.3 μm arsenide-antimonide based quantum well

Figure 2.13 shows layer structure and room temperature PL spectrum of 1.3 μm MQW active region with $Al_{0.2}Ga_{0.8}As_{0.78}Sb_{0.22}$ barriers and $GaAs_{0.58}Sb_{0.42}$ quantum well. Fabrication of LEDs and lasers based on these active regions is in progress.

2.6 Conclusion

In conclusion we have demonstrated that lateral oxidation of AlAs in conjunction with strained layers can be used generate epitaxial substrates with new lattice constants. These results suggest that lattice engineering through lateral oxidation of Al-containing compounds is a promising technique to generate substrates with new lattice constants for low threading dislocation density growth of technologically important semiconductors which cannot be grown on conventional substrates.

3. InP-Based Lattice-Engineered Substrates

3.1 Introduction

In addition to implementation of a GaAs based lattice engineered substrate, implementation of an InP-based lattice engineered substrate has also been investigated as part of the PRET program. An InP based lattice-engineered substrate enables the generation of lattice constants between InP (5.86 Å) and InAs (6.05 Å). As in the case of the GaAs-based lattice-engineered substrate, a suitable material for lateral, wet oxidation is needed. Two ternary oxidation layers can be lattice-matched to InP: $AlAs_{0.56}Sb_{0.44}$ and $Al_{0.48}In_{0.52}As$. Since InP substrates are sensitive to the high temperatures necessary to oxidize AlInAs/InP (525°C in our laboratory), AlAsSb was chosen as the oxidation layer.

The AlAsSb composition is lattice-matched to InP using a group-V induced RHEED oscillation calibration[1]. This is done by lowering the group V flux below the point where the V/III ratio = 1. The RHEED oscillations become limited by the arrival of the group V species at the surface of the sample, resulting in a period dictated by the group V flux. This calibration is done monthly for arsenic and antimony, as there is only a very slow change in the flux with valve position for valved, cracked solid sources. Using the group V RHEED oscillations, the antimony flux is set to the proper growth rate under the assumption that all of the antimony will be incorporated at the growth temperature of 490°C. The arsenic is set to a slightly higher flux than the V/III stable condition to provide for a smoother growth surface. For example, if a growth rate of 1μm/hour is desired, the Sb_2 flux is set to 0.44μm/hour level, and the As_2 flux is set to >~0.65μm/hour level. This reproducibly provides for a simple way to calibrate the As/Sb ratio insitu.

In the lateral oxidation of AlAsSb, the resulting microstructure is as shown schematically in Fig. 3.1, with a non-uniform "float" layer of Sb metal at the interface between the oxide and the upper semiconductor layer. This is in contrast to the oxidation of AlAs and AlGaAs, where most of the arsenic escapes from the system. The roughness created by uneven Sb segregation at the interface results in a surface that is not usable for regrowth. The oxidation of an AlAs/AlSb

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[1] G. Almuneau, E. Hall, H. Kroemer, and L.A. Coldren, in press.

superlattice lattice-matched overall to InP was investigated as a possible method for controlling or altering this Sb segregation, since AlSb has been shown not to oxidize laterally. However, the Sb segregation and the oxidation kinetics remained the same between the AlAs/AlSb superlattice and the uniform alloy.

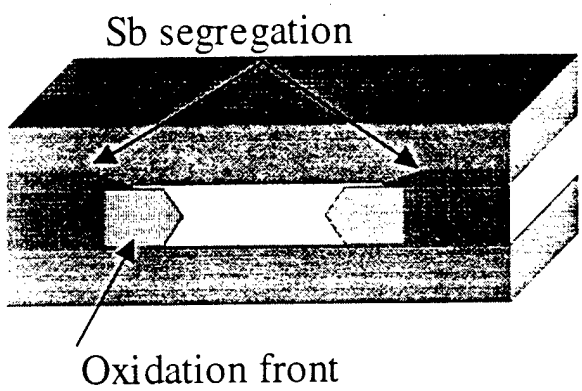

Figure 3.1: Schematic showing the oxidation of AlAsSb and the resulting microstructure. The arsenic escapes laterally as the oxidation front passes, while the antimony remains in the oxidation layer. After the front passes, it segregates to one or the other oxide/semiconductor interface. Most often, it segregates upward, probably due to the ease of deforming the top capping layers with no hard Al_2O_3 intervening.

3.2 Oxidation kinetics of AlAsSb and related materials

The lateral oxidation of AlAsSb is unique due to the presence of antimony. After the oxidation of AlAs and AlP, the oxide is nearly free of residual group V atoms. (AlSb does not oxidize laterally, a phenomenon that is not at present explained). AlAsSb, by contrast, retains nearly all of the antimony originally present in the AlAsSb layer. This Sb is in the form of a continuous, non-uniform metallic layer at the interface between the oxide and the upper semiconductor layer, as shown in an SEM micrograph in Fig. 3.2 and schematically in Fig. 3.1. It is believed that the antimony phase-separates to one or the other interface, eventually collecting at the top interface because it can more easily deform the top cap. The residual antimony thickness is ~25% of the thickness of the original AlAsSb layer, while the oxide itself is ~90% of the AlAsSb layer thickness. As a result, the structure swells overall by about 20% of the oxidation layer thickness. This swelling and the thickness of the antimony as a percentage of oxidation layer thickness are not affected by oxidation parameters such as oxidation temperature,

water temperature, layer thickness, oxidation time, or by the presence of a stiff, thick dielectric cap such as Si_3N_4.

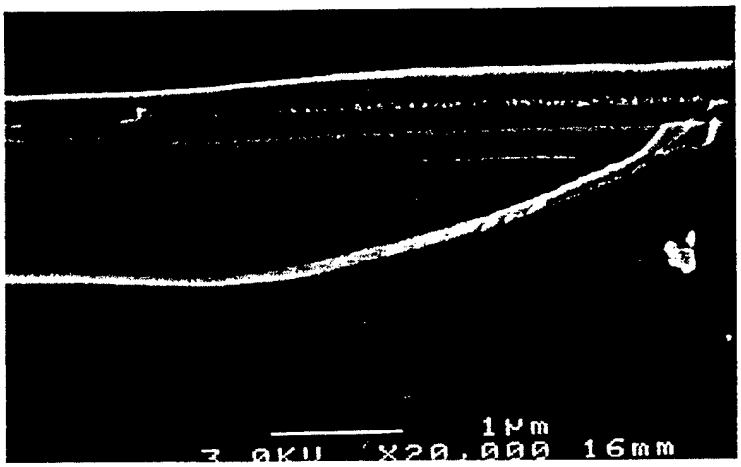

Figure 3.2: Cross-section SEM micrograph of the antimony segregation after AlAsSb oxidation. The micrograph shows that there is a "lag" in the oxidation of antimony behind the oxidation front. This distance is affected by the oxidation conditions (it can be adjusted from ~100nm to ~3μm), but there is no change in the total amount of antimony that segregates.

The oxidation kinetics of AlAsSb have been investigated. Figure 3 shows the oxidation distance as a function of time for temperatures ranging from 325-500°C. Over the range 325-400°C, an activation energy of 1.8eV is found. This contrasts with previously reported data, where activation energies of 1.2eV have been reported[2]. The activation energy is a measurement related to the rate-limiting step during oxidation. Generally, the rate-limiting step for oxidation can be either reaction at the oxidation front or diffusion of species to or from the oxidation front (including both reactants and products). Compared with the wet lateral oxidation of AlAs and AlGaAs, AlAsSb oxidation is more likely to be rate-limited by reaction at the oxidation front. This may be a result of the removal of Sb metal from the oxide, leaving a more porous Al_2O_3 layer, or it may be due to the lower oxidation temperatures considered in calculating the AlAsSb oxidation activation energy. (AlAs and AlGaAs are most commonly oxidized in the temperature range 400-450°C, which may allow the oxide to densify somewhat during oxidation).

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[2] P. Legay, P. Petit, G. Le Roux, A. Kohl, I.F.L. Dias, M. Juhel, and M. Quillec, *J. Appl. Phys.*, **81** (11), 7600 (1997).

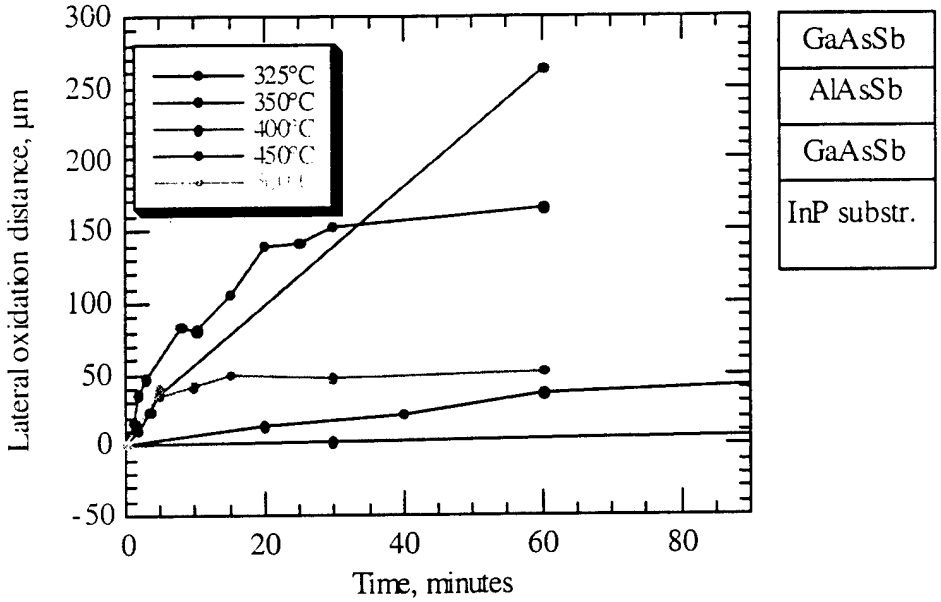

Figure 3.3: Oxidation distance as a function of time. Data are shown for a 500Å thick $AlAs_{56}Sb_{44}$ oxidation layer. Over the range 325°C-400°C, the oxidation remains reaction-limited, whereas above 400°C, self-stopping oxidation is observed.

The AlAsSb oxidation front is non-planar, in contrast to the case of AlAs lateral oxidation. Figure 3.4(i-iii) show optical and AFM images of AlAsSb oxidized at 450°C (in the structure 2000Å GaAsSb/500Å AlAsSb/2000Å GaAsSb/InP substrate), where fingers of oxide and Sb extend in front of the main front of the oxide. A slice through the AFM image shown in Fig. 3.4(iii) shows that the oxidation front at the edges of the "finger" have a much larger initial swelling (~60% of the oxidation layer thickness) which reduces to the equilibrium level as the front passes. This could be a pileup of antimony behind the oxidation front. It is enhanced at high oxidation temperature (450-500°C), where the oxidation reaction is fast relative to the mobility of antimony. This would be analogous to the solidification reaction of a molten metal alloy, where the solute is rejected at the solidification front, piling up and undergoing constitutional supercooling, making a cellular (finger-like) solidification front favorable.

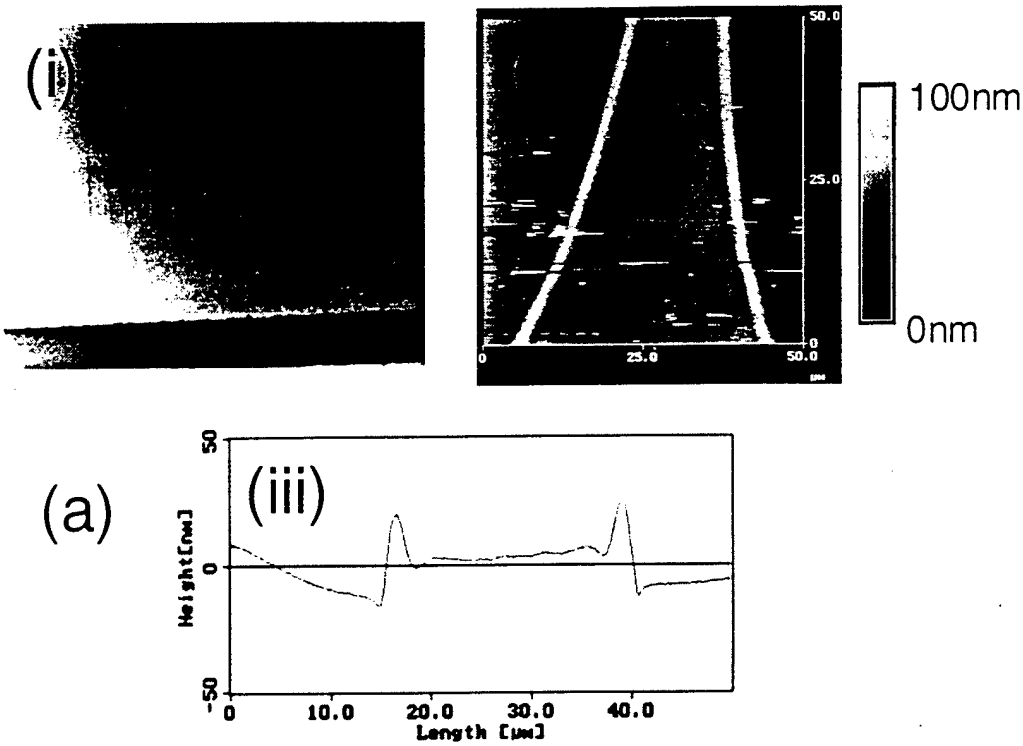

Figure3 4:Oxidation at 450°C of uncapped 500Å AlAsSb

(i) Optical micrograph showing the "fingered" oxidation front.

(ii) AFM image of a finger

(iii) Vertical cut through the AFM image of (ii), showing the depression, then elevation after the oxidation front passes. This appears to be due to a buildup of antimony behind the oxidation front immediately after it passes.

A second dramatic effect of high oxidation temperature is observed at or above 450°C: the oxidation distance saturates. This has not been previously observed as the typical AlAsSb/InP oxidation temperatures are kept below 400°C. This is also thought to be related to the antimony pileup behind the oxidation front at high temperatures, which could prevent the oxidants from reaching the reaction front and the oxidation products from leaving. The effect becomes more pronounced at higher temperature as the oxidation distance saturates faster, as shown in Fig. 3.3.

3.3 Antimony Segregation during AlAsSb oxidation

Several engineering solutions to the problem of uneven antimony segregation have been attempted. These have included varying the composition and structure of the oxidation layer itself, varying the layer thickness and oxidation temperature, and capping the entire structure with a thick dielectric cap. These attempts are recounted here, ending with the only viable solution yet found: a 500Å AlAsSb oxidation layer and a 5000Å thick Si_3N_4 cap on top of the entire structure.

The effect of changing the oxidation temperature on the surface morphology has been studied. This was done by oxidizing the structure shown in Fig. 3.5, the standard structure for each of these studies. Due to the relatively large thickness of the oxidation layer, the roughness

2000Å GaAsSb
Oxidation layer
2000Å GaAsSb
InP substrate

Figure 3.5: Standard oxidation structure used in the study of oxidation kinetics and antimony segregation. The oxidation layer was varied for the different samples, but the standard thickness investigated was 2000Å.

of the surface after oxidation was sufficient for easy observation using an optical microscope. At oxidation temperatures of less than ~375°C, and at oxidation temperatures of ~425°C or more, the surface was rough after oxidation. The surface was also rough at temperatures of ~400°C, but the surface undulations appeared to be correlated with either the <110> directions or with the oxidation fronts, which were aligned along <110>, as shown in Fig. 3.6. However, the antimony segregation was nonuniform in each case, so the effect of temperature appears not to be useful. Additionally, at sufficiently high temperature (500°C), the final oxidation distance is too short to use for oxidizing large mesas (100-500μm square, for example), and the upper layers in the structure are more likely to delaminate after oxidation at high temperatures.

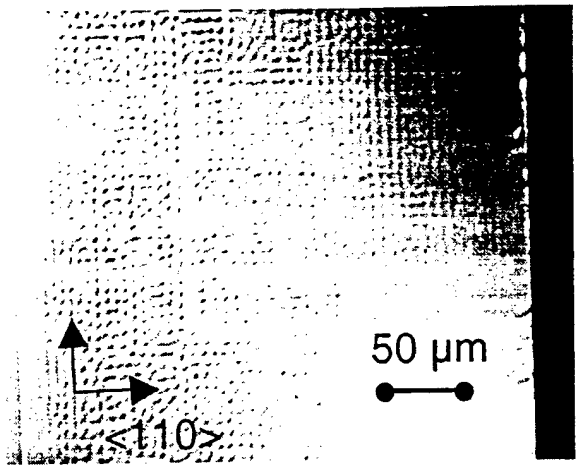

Figure 3.6: Optical micrograph showing the roughness correlated with the <110> directions after oxidation of 2000Å AlAsSb in the structure of Fig. 5.

The thickness of the antimony float layer is a nearly constant fraction of the overall thickness of the oxidation layer. Therefore, an oxidation layer with less antimony was investigated: (Al,In)(As,Sb). First, the growth conditions were determined for this quaternary alloy. Figure 3.7 shows the lattice-matched compositions to InP. By adding a larger group III atom (In), the fraction of antimony at the lattice-matched condition is lessened. The growth of these layers was

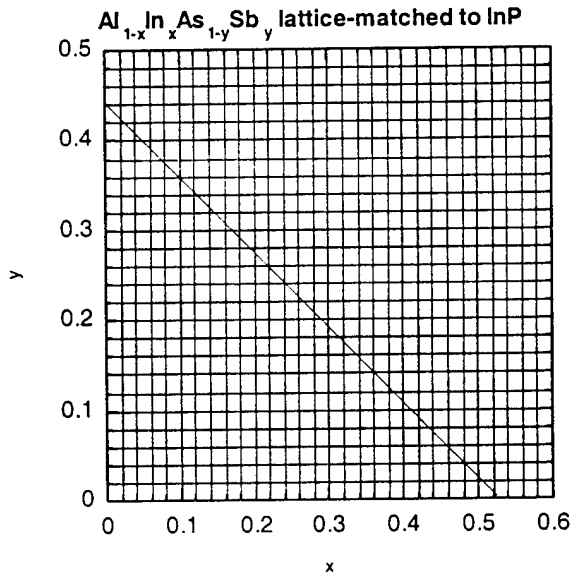

Figure 3.7: Calculated lattice-matched compositions of AlInAsSb to InP.

simplified by the use of group V induced RHEED oscillations to calibrate the Sb/As ratio. Three target compositions were grown in a structure similar to Fig. 3.5, but replacing AlAsSb with 2000Å $Al_{.76}In_{.24}As_{.76}Sb_{.24}$ or $Al_{.95}In_{.05}As_{.6}Sb_{.4}$. Since the layer was a quaternary material (and not a pseudobinary like InGaAs), the composition could not be uniquely determined by X-ray diffraction, but the peak splitting was less than 300 arcsec in each case. Samples were cleaved and inserted into the oxidation furnace held at 400°C and at 500°C for one hour. No lateral oxidation was measured in the higher In composition sample for either temperature. The oxidation rate in the low-In sample was about one-tenth of that in AlAsSb at 400°C, while at 500°C, the oxidation rate could not be measured due to apparent self-stopping oxidation. This can be explained in the following way: at low temperatures, any addition of indium slows the rate tremendously without reducing the antimony content significantly. At high temperatures, oxidation should proceed, except that the presence of antimony and its relatively low mobility in the wake of the oxidation front prevent further oxidation, effectively stopping oxidation before it starts. Therefore, the reduction in the amount of antimony through the introduction of indium is not useful since the oxidation reaction is slowed too far.

AlGaAsSb was also investigated as a possible oxidation layer. It has been suggested that by adding Ga to the oxidation layer, the oxidation temperature could be elevated, allowing Sb_2 and Sb_4 to escape through the oxide. This might reduce the residual antimony layer. To investigate this possibility, layers of digitally alloyed AlAsSb and GaAsSb were grown to 2000Å thick in the same structure as Fig. 3.5. Overall, these layers had 2, 5, and 10% Ga addition. Generally, the 2% Ga layers retained the same oxidation kinetics as the AlAsSb, while the 10% Ga layers were much slower. Interestingly, the addition of Ga prevented the onset of self-stopping oxidation at 450°C for both the 2 and 5% Ga layers, but at 500°C, self-stopping oxidation was observed for all compositions. The morphology of these layers remained similar to pure AlAsSb regardless of composition, as did the swelling, which remained constant at about 20% of the original layer thickness.

A third option for reducing the amount of residual antimony in the oxidized layer was studied: reducing the layer thickness of the AlAsSb. Using the structure of Fig. 3.5, oxidation layers of 100, 200, 300, and 500Å were grown. At all temperatures, the oxidation rates of the 500Å AlAsSb were the same as for the 2000Å AlAsSb layer. The 100Å layer was not observed

to oxidize, similar to the behavior of AlGaAs and AlAs. However, the thinner layers had lower oxidation rates and a different surface morphology. The oxidation fronts were not planar and the surface was more likely to develop "fingers" protruding out from the main front. These fingers persisted in the final oxidized layer, although far behind the oxidation front, the surface layer became smooth at 400° and 450°, as shown in Fig. 3.8. Thinning the oxidation layer may be

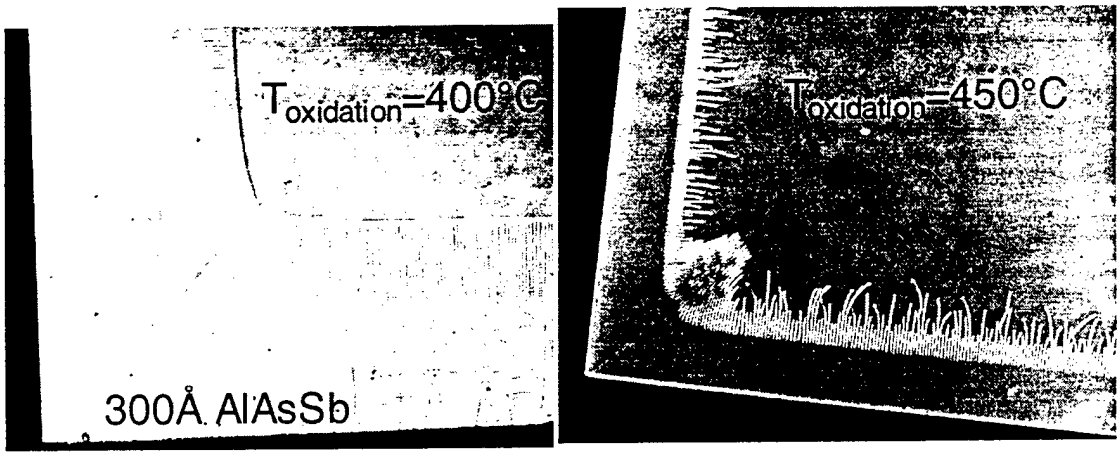

Figure 3.8: Thin oxidized layers of AlAsSb, showing the transition from a rough to a smooth morphology after the oxidation front passes.

used effectively for short distances provided the layer is over-oxidized to remove the fingered morphology, but for our purposes, over-oxidation is not desired. Therefore, the minimum thickness for a fast reaction rate was chosen to be 500Å AlAsSb.

Superlattices of AlAsSb/GaAsSb have been grown and oxidized. In contrast to the digital alloy method, where a superlattice of total period ≤ 20Å was used, much thicker sublayers of GaAsSb and AlAsSb were used. The reason for this was to decrease the mobility of antimony in the growth direction to prevent a continuous metallic layer from forming. In fact, the presence of antimony may allow for delamination from the oxidation layer. Since GaAsSb should not oxidize, the Sb should remain where it is generated. Two growth structures have been investigated, as shown in Fig. 3.9. The oxidation layers have the structure n•(200Å AlAsSb, 25Å GaAsSb) or n•(400Å AlAsSb, 50Å GaAsSb). This ensures that both oxidation layers had overall the same fraction of Ga and Al. Both structures have rough surfaces when first oxidized. Additionally, the swelling of the structure as measured by AFM shows that these superlattices

may have as much as 40% swelling immediately behind the oxidation front relative to the original oxidation layer. This could be due to delamination of the upper semiconductor from the

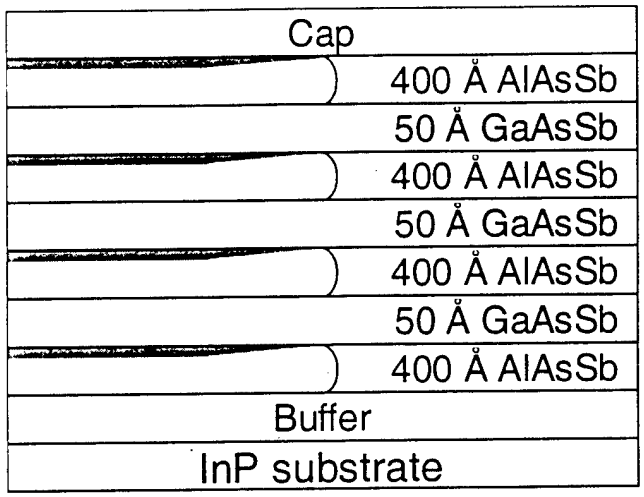

Figure 3.9: Layer structures of superlattice samples. The GaAsSb should not oxidize and may therefore prevent a diffusion barrier to the Sb metal. However, these structures roughen and swell more than the uniform AlAsSb oxidation layers, and are therefore not considered to be viable.

oxide. As a result, these structures have not proven to aid in controlling the antimony segregation. As might be expected, the oxidation of these layers is slower than that of the uniform alloy.

While the amount of residual antimony after AlAsSb oxidation is not alterable, the surface morphology is easily controlled. Recent results have shown that the use of a thick, stiff dielectric cap planarizes the oxidized structure. The same structure of Fig. 3.4 was capped with 0.5μm Si_3N_4 and oxidized at the same temperature (450°C), where fingers are most likely to form. This structure is shown in Fig. 3.10(i-iii), where Fig. 3.10(iii) shows a section taken of the AFM image of the still-capped structure in Fig. 3.10(ii). The resulting oxidation has a planar front, and the surface is smooth on the scale of the optical microscope as well as the AFM.

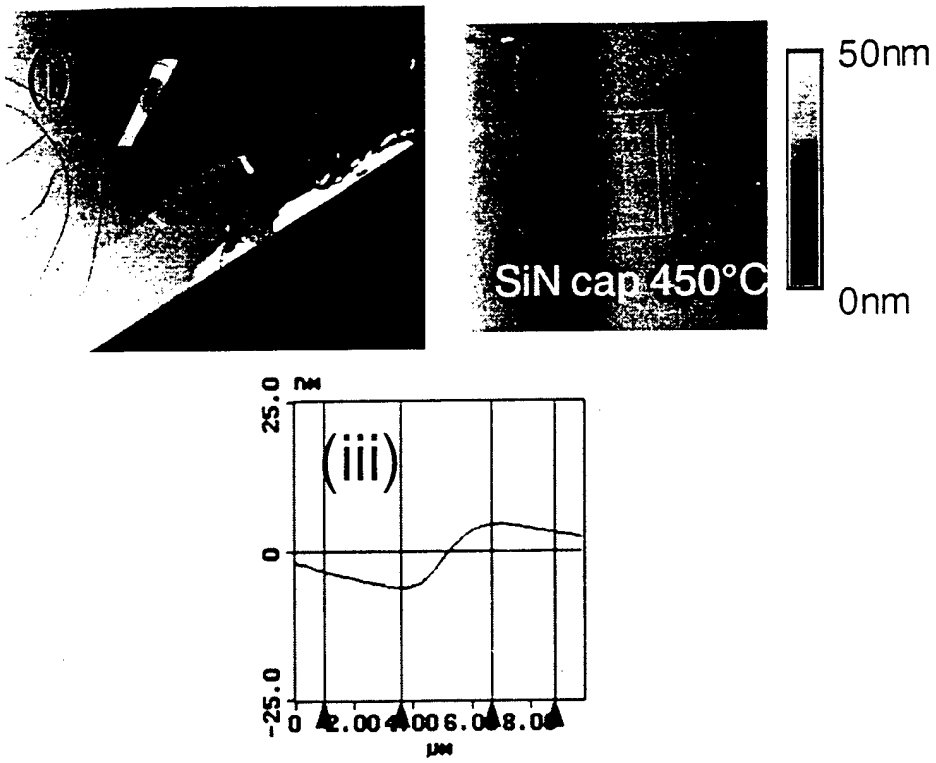

Figure 3.10: Oxidation at 450°C of 500Å AlAsSb capped with 0.5µm of Si_3N_4.

(i) Optical micrograph showing the "fingered" oxidation front

(ii) AFM image of a finger.

(iii) Vertical cut through the AFM image of (ii), showing the depression, then elevation after the oxidation front passes. This appears to be due to a buildup of antimony behind the oxidation front immediately after it passes.

The optical micrograph shows the cracking of Si_3N_4 at this temperature, which is due to a thermal expansion mismatch between the substrate and the dielectric cap.

4. High Performance Metamorphic HEMTs on GaAs substrates (Work done at HRL Laboratories, Malibu)

During this period of performance, HRL has focused on one practical application of metamorphic materials, i.e. high performance HEMT on low cost substrate. We were able to grow, fabricate, and demonstrate HEMTs on GaAs substrates with dc and rf characteristics that rival those grown on InP substrates. The performance of these metamorphic HEMTs is to our knowledge the best ever obtained for HEMTs grown on GaAs substrates.

4.1 Introduction

High electron mobility transistors (HEMT's) based on InP substrate have excellent high frequency and low noise performance[3]. Superior performance of these devices over that of GaAs based pseudomorphic HEMT's is a result of good transport properties of $In_{.53}Ga_{.47}As$ channel and large value of conduction band discontinuity between $In_{.53}Ga_{.47}As$ channel and $In_{.52}Al_{.48}As$ barrier layers. It is argued that the main obstacle for mass production and commercialization of these high performance devices is high cost and small size of InP substrates.

It has been demonstrated in the past that material structures that mimic those of InP based HEMT's can be grown on cheaper GaAs substrates using metamorphic buffer layers to accommodate lattice mismatch between GaAs substrate and InAlAs/InGaAs active layers[4]. Devices fabricated from structures grown on metamorphic buffer layers have similar electrical characteristics as devices grown on InP substrate and are not significantly affected by large concentration of threading dislocations in their active layer and by cross hatch surface morphology that is typical for thick, compressively strained epitaxial layers. Despite the large interest in metamorphic HEMT's on GaAs substrate[5], there are few reports of the power performance of these devices in V-band.

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[3] L. D. Nguyen, A. S. Brown, M. A. Thompson, L. Jelloian, IEEE Trans. El. Dev. **39**, 2007-2014 (1992).
[4] G. U. Wang, Y. K. Chen, W. J. Schaff, L. F. Eastman, IEEE Trans. Electron. Devices, **ED-35**, 818 (1988), J. C. Harmand, T. Matsuno, K. Inoue, Jpn. J. Appl. Phys. **28**, 1101 (1989).
[5] M. Zaknoune, B. Bonte, C. Gaquiere, Y. Cordier, Y. Druelle, D. Theron, Y. Crosnier, IEEE El. Dev. Let. **EDL 19**, 345 (1998).

In this work we report for the first time power performance measured at 57 GHz of metamorphic $In_{.6}Ga_{.4}As/In_{.52}Al_{.48}As$ HEMT's grown on GaAs substrate.

4.2 MATERIAL GROWTH AND DEVICE FABRICATION

Metamorphic InGaAs/InAlAs HEMT layers were grown on 3 inch (001) oriented GaAs substrates in Perkin-Elmer 430 solid source Molecular Beam Epitaxy (MBE) system. A series of test structures was initially grown to optimize the growth conditions. Table 4.1 shows test structure and growth conditions that were used in the study. The only parameters that were

Thickness [Å]	Material	Growth Temperature [°C]	Composition
70	$In_xGa_{1-x}As$ n = $1x10^{18}$ cm^{-3}	520	x=0.53
200	$In_xAl_{1-x}As$	520	x=0.52
3	$In_xAl_{1-x}As$ N_s = $3x10^{12}$ cm^{-2}	520	x=0.52
15	$In_xAl_{1-x}As$	520	x=0.52
400	$In_xGa_{1-x}As$	520	x=0.53
2500	$In_xAl_{1-x}As$	520	x=0.52
1000	$In_xAl_{1-x}As$	T_{buffer}	x=0.52
d	$(In_yGa_{1-y})_{.52}Al_{.48}As$	T_{buffer}	y -linearly graded from 0 to 1
500	$Ga_{.52}Al_{.48}As$	600	
	S.I. GaAs Substrate		
d = 0.25 μm, 0.5 μm, 1 μm grown at T_{buffer} = 430 °C			
T_{buffer} = 390 °C, 410 °C, 430 °C d = 1 μm			

Table 4.1: Device structure used for optimization of growth conditions

varied during optimization were thickness of linearly graded InAlGaAs metamorphic buffer layer, and substrate temperature used for its growth. We focused on these two parameters, because published results suggest that they have the strongest impact on the material quality. We decided to use linearly graded buffer layers in our structures, because it is the most documented approach to accommodate lattice mismatch between GaAs substrate and InGaAs active layers in films grown by MBE. Metamorphic buffer layers are grown at reduced substrate temperatures to prevent three dimensional growth mode that is common in strained layer epitaxy. Fluxes of metal atoms and the III/V pressure ratios were the same as we commonly use for the growth of

lattice matched InP based HEMT's. To examine effects of the buffer layer thickness three wafers were grown having graded layer thickness of 0.25 μm, 0.5 μm and 1 μm, respectively. The substrate temperature during the buffer layer growth of these wafers was kept at 430 °C. Electrical properties of these wafers were characterized by Hall effect. Figures 4.1 and 4.2 show the summary of Hall effect measurements. Results presented in Fig. 4.1 show that material quality,

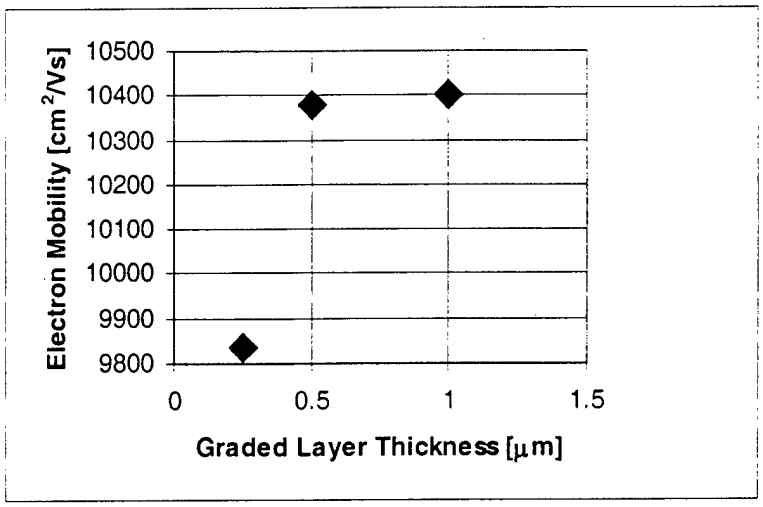


Figure 4.1: Measured relationship between electron mobility and graded buffer layer thickness of metamorphic HEMT structures. Graded layers were grown at a substrate temperature of 430 °C.

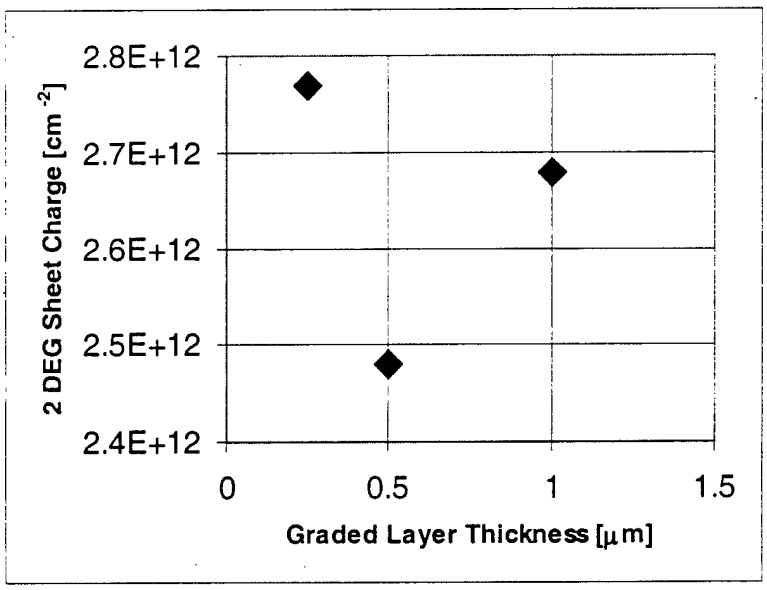


Figure 4.2: Measured relationship between sheet charge and graded buffer layer thickness of metamorphic HEMT structures. Graded layers were grown at a substrate temperature of 430 °C.

manifested as mobility of two-dimensional electron gas (2DEG), increases with thickness of linearly graded buffer layer. It is, however, important to note that increase of the buffer layer thickness from 0.5 μm to 1 μm yielded only a small improvement of electron mobility. Extrapolation of these results suggests that only marginal improvements of material quality can be obtained as buffer layer thickness is increased beyond 0.5 μm and that fairly thin linearly graded buffer layers are sufficient to accommodate lattice mismatch between GaAs and $In_{.48}Ga_{.52}As$. Based on these results we decided to fix buffer layer thickness of our metamorphic HEMT structures to 1 μm, to keep reasonably short growth times.

To examine the effect of buffer layer growth temperature on material quality of metamorphic HEMT's three wafers were grown at buffer layer temperatures of 390 °C, 410 °C and 430 °C, respectively. The thickness of linearly graded buffer layer of these wafers was 1 μm. Results of Hall measurements presented in Figs. 4.3 and 4.4 show that the highest electron mobility was obtained for buffer layer grown at 410 °C.

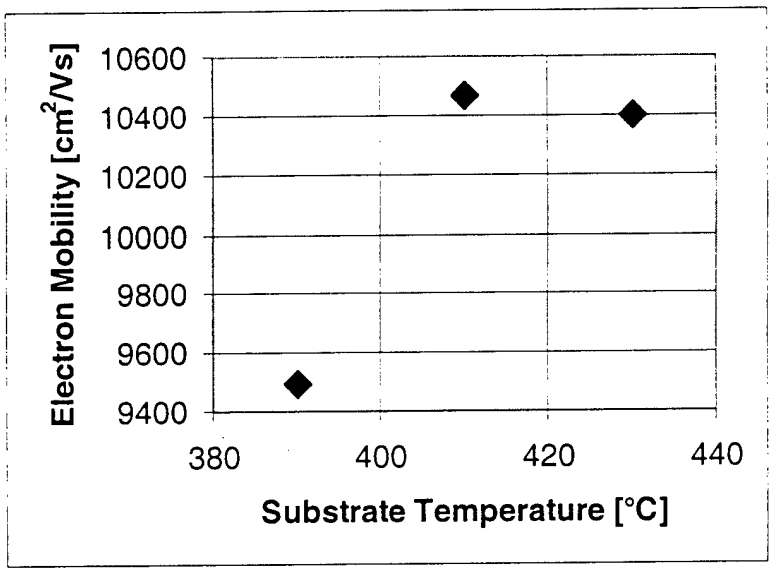


Figure 4.3: Measured relationship between electron mobility and growth temperature of the graded buffer layer. Graded buffer layer thickness was 1 μm.

The room temperature 2DEG electron mobility of 10430 cm^2/Vs of metamorphic HEMT grown under optimized conditions was slightly lower than mobility of 11000 cm^2/Vs that we typically obtain in similar InP based structures with same concentration of electrons in the channel. The electron mobility of metamorphic HEMT structure is probably lower due to high density of threading dislocations in channel layer of metamorphic HEMT's and due long range

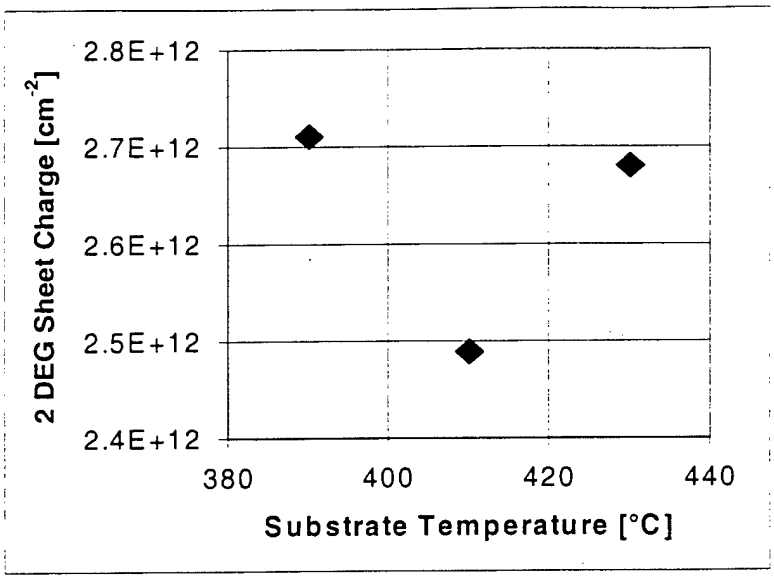


Figure 4.4: Measured relationship between Sheet charge and growth temperature of the graded buffer layer. Graded buffer layer thickness was 1 μm.

roughening of the channel/barrier layer interface, which is a result of cross-hatch surface morphology.

In Fig. 4.5 typical double crystal x-ray rocking curve of (004) reflection of metamorphic HEMT wafer is shown. The diffraction pattern consists of a sharp peak at 33.0248° that

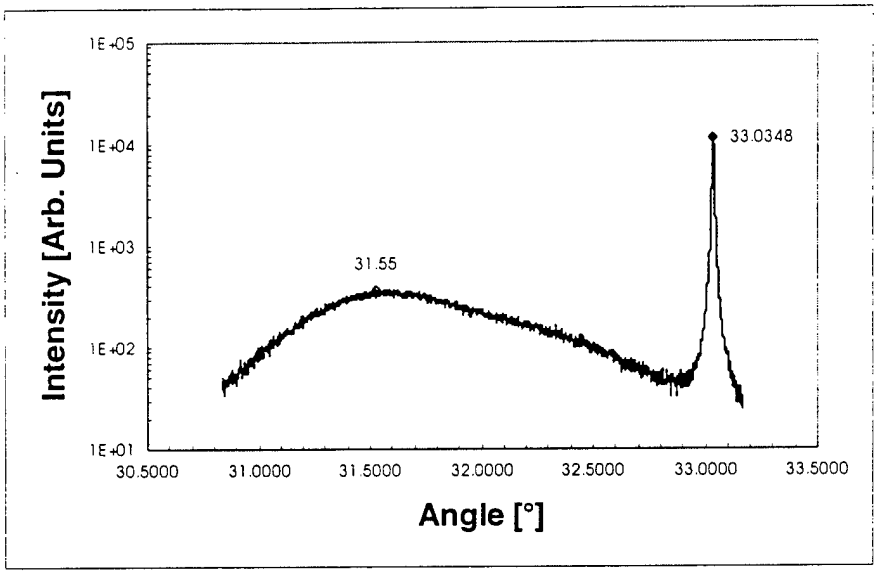


Figure 4.5: Typical Double crystal x-ray diffraction rocking curve of (0 0 4) reflection of Metamorphic HEMT wafer. Diffraction image was obtained with Cu Kα line x-rays. Peak at 33.0348° corresponds to GaAs substrate.

corresponds to GaAs substrate and broad peak with maximum at 31.55 ° that corresponds to metamorphic HEMT layer. The diffraction peak corresponding to InP would be located on the same figure at approximately 31.67°. The diffraction peak that corresponds to metamorphic HEMT layer is broad because it is merged with diffraction peak of thick linearly graded buffer layer, and because our metamorphic HEMT wafers have cross-hatch surface morphology. In Figure 4.6 image obtained by Nomarski microscopy of typical surface morphology of our metamorphic wafer is shown. The cross-hatch surface morphology promotes alloy clustering

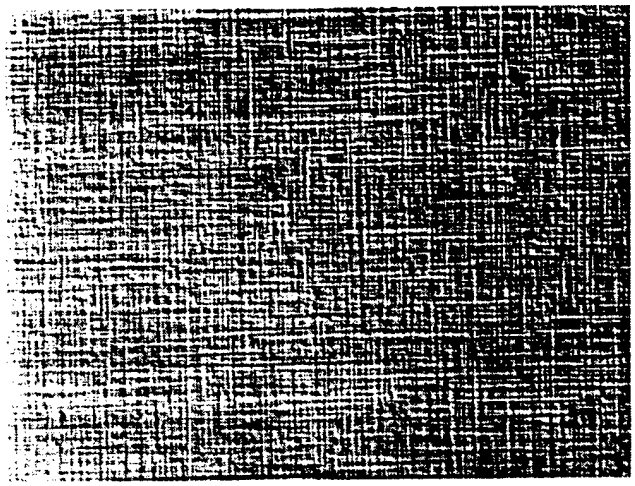


Figure 4.6: Typical image of surface morphology of metamorphic HEMT wafers. The image was obtained by Nomarski microscopy. Magnification factor is 320.

during the crystal growth, and hence diffraction peak broadening.

In Table 4.2 structure grown for fabrication of high power metamorphic HEMT's is shown. This structure is better suited for fabrication of short gate length HEMT's than structure shown in Table 1, because it has thinner channel layer to suppress short gate effects. The channel layer is In rich to improve electron confinement and transport properties. The structure was grown using optimized growth conditions. The room temperature electron mobility of 9500 cm^2/Vs and sheet charge of $4x10^{12}$ cm^{-2} were measured by Hall effect for this structure. For a comparison we typically obtain electron mobility of 10400 cm^2/Vs for similar lattice matched InP-based structure.

Device fabrication began with deposition of GeAu/Ni/Ti/Au ohmic contact metal. Contact metal was annealed at 360 °C and device isolation was obtained by ion implantation. Gate openings with nominal length of 0.12 μm were defined into bilayer resist by electron-beam lithography to obtain T – shaped gate profile.

Thickness [A]	Material	Growth Temperature [C]	Composition
70	$In_xGa_{1-x}As$ n = $1x10^{18}$ cm^{-3}	520	x=0.53
200	$In_xAl_{1-x}As$	520	x=0.52
3	$In_xAl_{1-x}As$ Ns = $3x10^{12}$ cm^{-2}	520	x=0.52
15	$In_xAl_{1-x}As$	520	x=0.52
200	$In_xGa_{1-x}As$	520	x=0.60
50	$In_xAl_{1-x}As$	520	x=0.52
3	$In_xAl_{1-x}As$ Ns = $1x10^{12}$ cm^{-2}	520	x=0.52
2500	$In_xAl_{1-x}As$	520	x=0.52
1000	$In_xAl_{1-x}As$	410	x=0.52
10000	$(In_yGa_{1-y})_{.52}Al_{.48}As$	410	y - linearly graded from 0 to 1
500	$Ga_{.52}Al_{.48}As$	600	
	S.I. GaAs Substrate		

Table 4.2: Device structure used for fabrication of metamorphic HEMT's

Wet chemical gate recess etching was used to expose Schottky barrier InAlAs layer. Gate metals consisting of Ti/Pt/Au were subsequently deposited into defined openings and e-beam resist was removed. Devices were than passivated with 50 nm thick plasma deposited SiN_x film. Wafers were thereafter thinned to 50 μm and backside via-holes were made by reactive ion etching to connect source contact metal to the backside ground plane. Backside metal was than deposited and the wafer was diced into individual discrete device chips. In Figure 4.7 a chip with 600 μm wide-gate power HEMT is shown. This device has a10 gate finger layout. In the same Figure backside of the same chip with metal filled via-holes is shown.

4.4 DEVICE CHARACTERISTICS

Typical I-V curve of fully fabricated metamorphic HEMT is shown in Fig. 4.8. The peak value of extrinsic transconductance g_m at a drain bias of 1 V was 1.1 S/mm for a typical device,

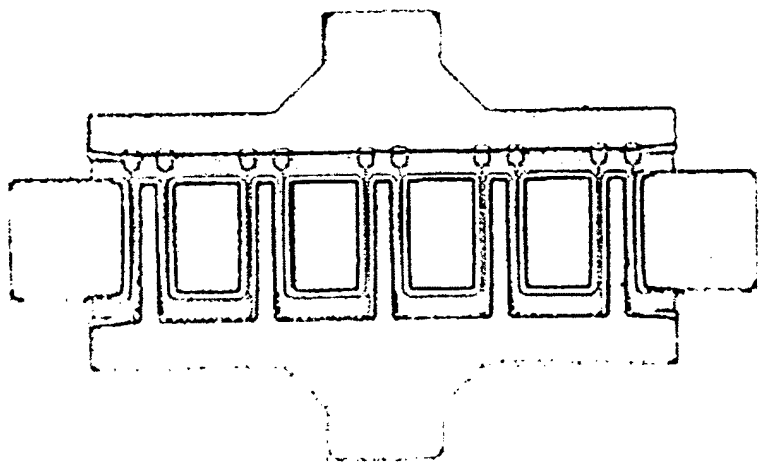
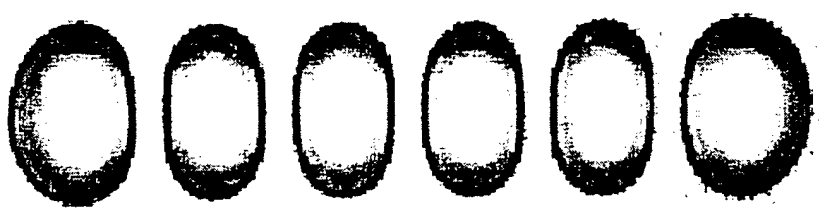


Figure 4.7: Microscope image of a chip with 10 gate finger metamorphic HEMT with total gate width of 600 μm. In bottom image backside of the chip with metal filled via-holes is shown.



while peak g_m values of 1.3 S/mm were obtained on some devices. This is to our knowledge the highest value of extrinsic transconductance ever reported for a metamorphic HEMT. The maximum value of drain current I_{ds} at the same drain bias was 600 mA/mm. These devices have forward bias gate turn on voltage of 0.4 V and reverse bias gate breakdown voltage of 4.0 V. Both parameters were measured at a gate current of 1 mA/mm. Devices with 0.12 μm x 120 μm gates have current gain cutoff frequency of 160 GHz and maximum frequency of oscillations of more than 200 GHz at V_{ds} of 1 V.

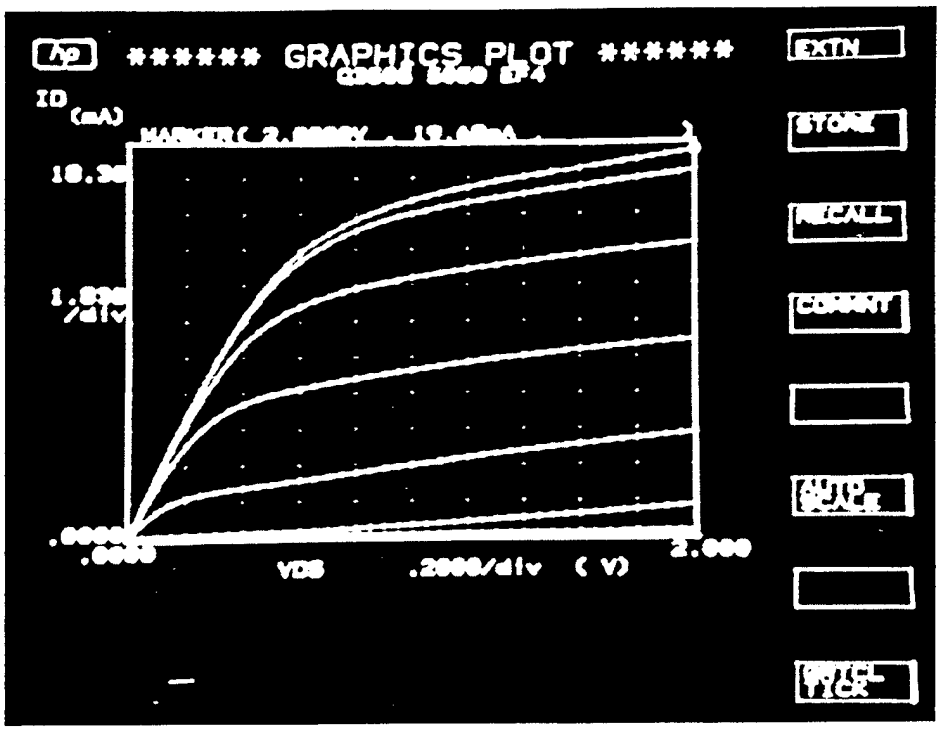


Figure 4.8: Current voltage characteristics of 0.12 μm x 25 μm gate metamorphic HEMT.

Preliminary measurements of the power performance of discrete devices with two and six gate-finger layout were done at 57 GHz. External tuning network was used to tune devices inserted into the test fixture for maximum output power. In Figures 4.9 and 4.10 measured plots of output power, power gain, and power added efficiency versus input power are shown for devices with 120 μm and 360 μm wide gates, respectively. The maximum output power and associated power density of 120-μm device was 18 mW and 153 mW/mm, respectively. These values were measured at drain bias of 2.0 V, gate voltage of 0 V, resulting in a drain current of 26.15 mA (218 mA/mm). The power added efficiency of 29% measured for this device is the highest ever reported for a metamorphic HEMT at this frequency. Devices with 360 μm wide gates had maximum output power of 66.1 mW (183.5 mW/mm) and power added efficiency of 27.3%. The biasing conditions were similar as for the smaller device (Vds = 2.0V, Vgs = 0 V and Id = 79 mA (219 mA/mm). Preliminary results of power measurements at 57 GHz of our metamorphic devices are encouraging because we believe that better power performance will be obtained with

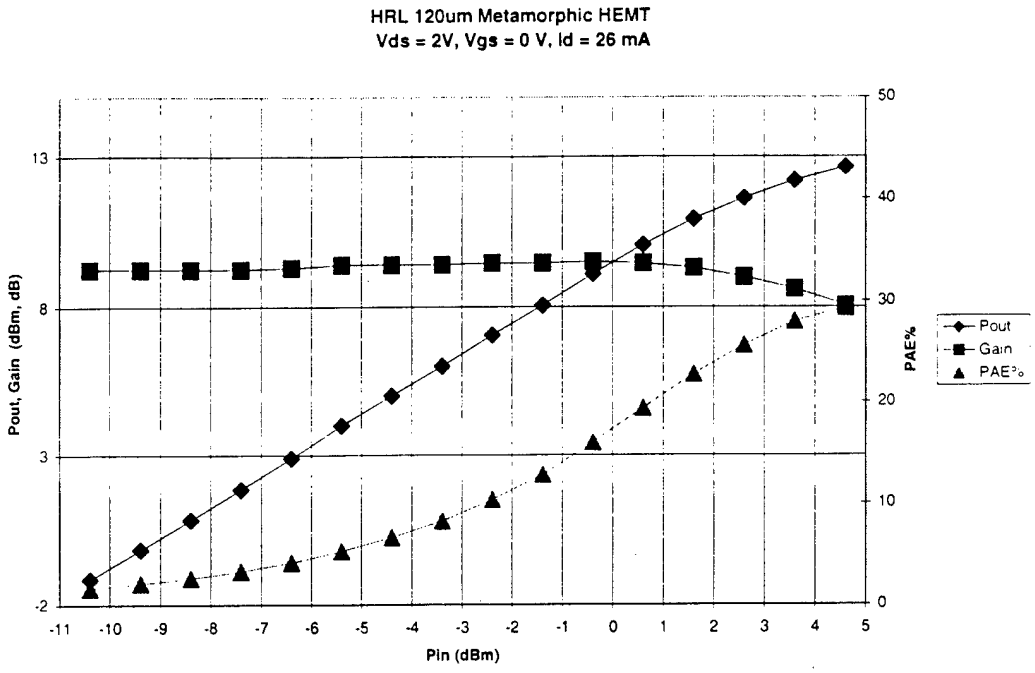


Figure 4.9: Output power, power gain and power added efficiency as a function of input power of 0.12 μm x 120 μm gate metamorphic HEMT.

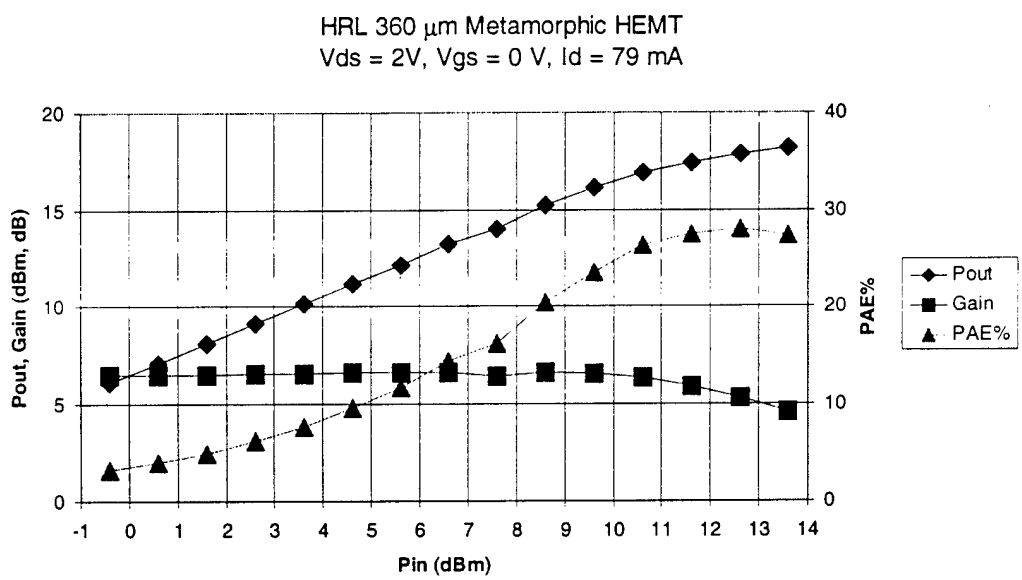


Fig 4.10 Output power, power gain and power added efficiency as a function of input power of 0.12 μm x 360 μm gate metamorphic HEMT.

optimization of biasing conditions. We are also planning to perform power measurements in W band.

4.5 Conclusions

We have optimized process for growth of InGaAs/InAlAs metamorphic HEMT structures on GaAs by Molecular Beam Epitaxy. Electrical properties of metamorphic HEMT structures grown under optimized conditions were only marginally inferior to properties of equivalent InP-based HEMT structures. We have fabricated 0.12 μm gate-length metamorphic HEMT's using our conventional process. These devices have demonstrated excellent DC performance. The peak gm of 1.3 S/mm at Vds = 1 V is the highest ever reported for a metamorphic HEMT. We performed preliminary measurements of power performance of metamorphic HEMT's at 57 GHz. The maximum output power of 66 mW and associated power density of 184 mW/mm were obtained for a device with 360 μm wide gate. These preliminary results are lower than the best values obtained on InP (324 mW/mm). We, however, believe that our results are encouraging and anticipate that higher output powers can be obtained on these devices with optimization of biasing conditions.

5. Long Wavelength Photoreceiver on GaAs Substrate

5.1 Introduction

For future long-haul optical fiber communications systems, the development of monolithically integrated, high speed (>10 Gbit/s), long wavelength photoreceiver is of considerable interest due to the potential advantages in size, reliability, and performance in comparison to hybrid receivers. Monolithically integrated photoreceivers for long wavelengths (1.3–1.55 μm) are usually realized on InP substrates. An alternative to InP based structures is to grow the absorbing InGaAs layer on GaAs substrates to take advantage of the well-established GaAs based electronic device technology.

InGaAs absorption layer with Indium content of 0.48 or more is required for the absorption of 1.3 and 1.55μm wavelength, which leads to higher than 3.3% lattice mismatch. Lattice mismatched growth of InGaAs on GaAs substrate was realized either by grading[6] or low temperature (120 - 300°C) growth of InGaAs on GaAs[7]. The dislocations in the InGaAs epilayer prevent the realization of high performance photoreceiver. Step graded MBE growth of InGaAs layer was chosen to accommodate the lattice mismatch between GaAs substrate and the InGaAs absorption layer since the step interface can effectively bend the dislocations into the interface.

Metal-semiconductor-metal photodetector (MSM) is a promising device for future ultra-high-speed photoreceiver systems. In contrast to the parallel-plate geometry of the vertical p-i-n photodiode, the MSM has both of its electrode on the device surface, in a series of alternating interdigitated fingers. This electrode geometry provides the MSM photodiode with a very low intrinsic capacitance, and thus the possibility of extremely high-speed devices. MSM photodiodes are especially attractive for integration with FETs and III-V integrated circuits because of their simple material structure and easy fabrication. On the transistor side the high cut-off frequency of HEMTs provide photoreceivers ultimately with a performance advantage.

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[6] Hurm, V.; Benz, W.; et al. ,"Long wavelength MSM-HEMT and PIN-HEMT photoreceivers grown on GaAs". GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 19th Annual Technical Digest 1997, IEEE, 1997. p.197-200.

[7] L. F. Lester, K. C. Hwang, et al., " Ultrafast Long – Wavelength Photodetectors Fabricated on Low-Temperature InGaAs on GaAs", IEEE Photonics Technology Letters, vol. 5, (no.5), 1993, p.511 - 14.

Additionally, the HEMT is the lowest-noise three-terminal device demonstrated to date. So HEMT is a natural fit with the high speed and low noise requirements for high performance photoreceivers. Further more, pseudomorphic HEMT (pHEMT) has superior power and efficiency performance due to the higher mobility of InGaAs channel compared with GaAs channel and increased conduction band offset of AlGaAs/InGaAs in contrast to that of AlGaAs/GaAs. Oxide was integrated into the photoreceiver as an insulator to suppress the substrate leakage current and thus give better charge control.

5.2 Lattice mismatched MBE growth of InGaAs on GaAs substrate

Seven step graded InGaAs (Fig. 5.1) was used to accommodate the lattice mismatch between GaAs and $In_{0.53}GaAs$. The thickness of the InGaAs graded layer is 0.6μm or less since thin epi-layer is desired for lower cost. $AlAsSb_{0.44}$ or $In_{0.52}AlAs$ layer was grown on top of the InGaAs graded layer to act as a spacer to electrically isolate the top device active region and the high defect density graded region. The $In_{0.53}GaAs/In_{0.52}AlAs$ HEMT structure was grown on step graded InGaAs layer to monitor the electrical property of the material.

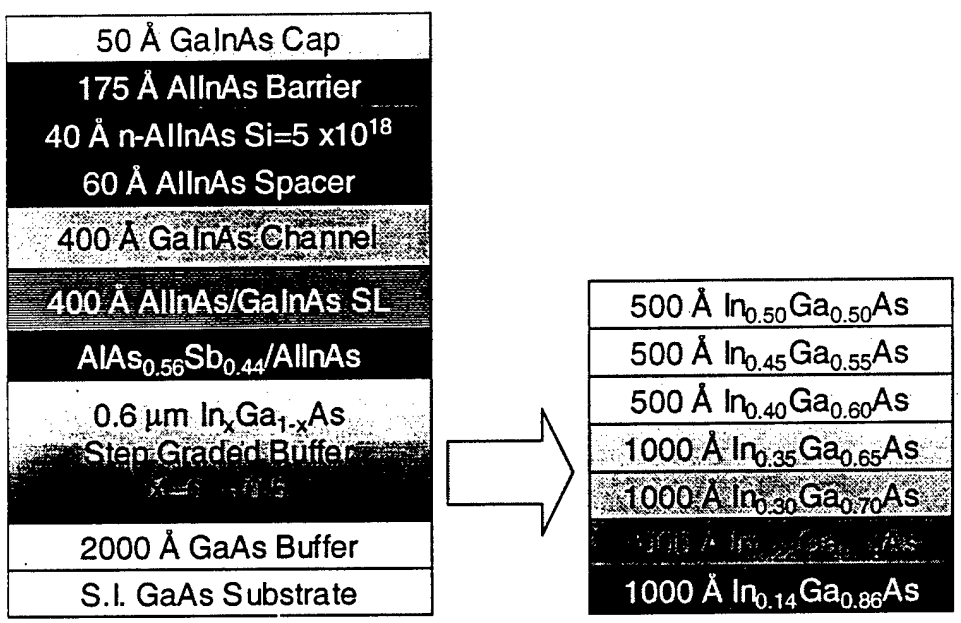
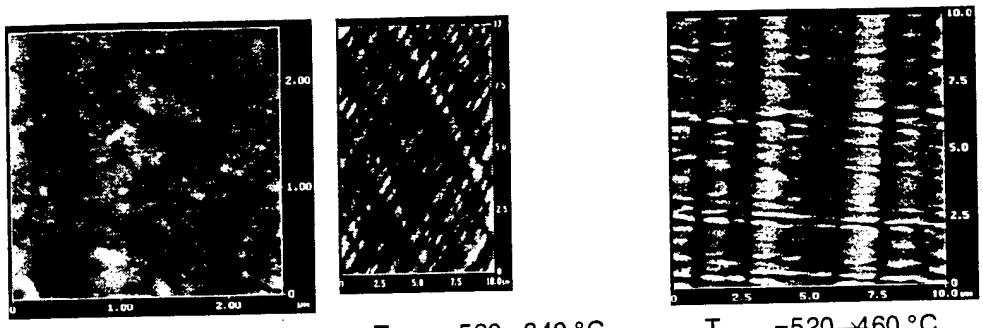


Figure 5.1: InGaAs/InAlAs HEMT structure on step graded InGaAs buffer.

As shown in Fig. 5.2, with the increase of the growth temperature of the InGaAs graded layer, the Hall mobility increases, although the AFM RMS surface roughness also increases.



T_{growth}=350 °C
μ= 3348cm^2/(v.sec)
RMS Roughness=10Å

T_{growth}=520→340 °C
μ= 5396cm^2/(v.sec)
RMS Roughness=20Å

T_{growth}=520→460 °C
μ= 7300cm^2/(v.sec)
RMS Roughness=55Å

Figure 5.2: AFM surface image of InGaAs graded layers grown at different temperature.

The low growth temperature of the InGaAs graded layer was believed to minimize the formation of dislocations and maintain a two-dimensional growth front. But more point defects were incorporated at lower growth temperature. While high growth temperature can enhance the strain relaxation of mismatched epilayers.

5.3 Conclusion

InGaAs step graded layer was used to accommodate the lattice mismatch between GaAs and $In_{0.5}GaAs$. Higher growth temperature of the graded layer gave higher mobility, although accompanied by higher surface roughness.

6. GaAs on Insulator pHEMTs

The oxide formed from the lateral oxidation of AlAs or $Al_{0.98}GaAs$[8] was demonstrated as an insulator for GaAs based devices. After the success of the application of the GaAs-On-Insulator (GOI) technology to the GaAs metal-semiconductor field-effect transistor (MESFET) work has been done to extend this technology to other devices, more specifically the GaAs psuedomorphic high-electron-mobility transistor (pHEMT).

Due to the elimination of substrate leakage current and excellent charge control, high efficient and linear devices could be realized based on this GOI technology. But the charge loss

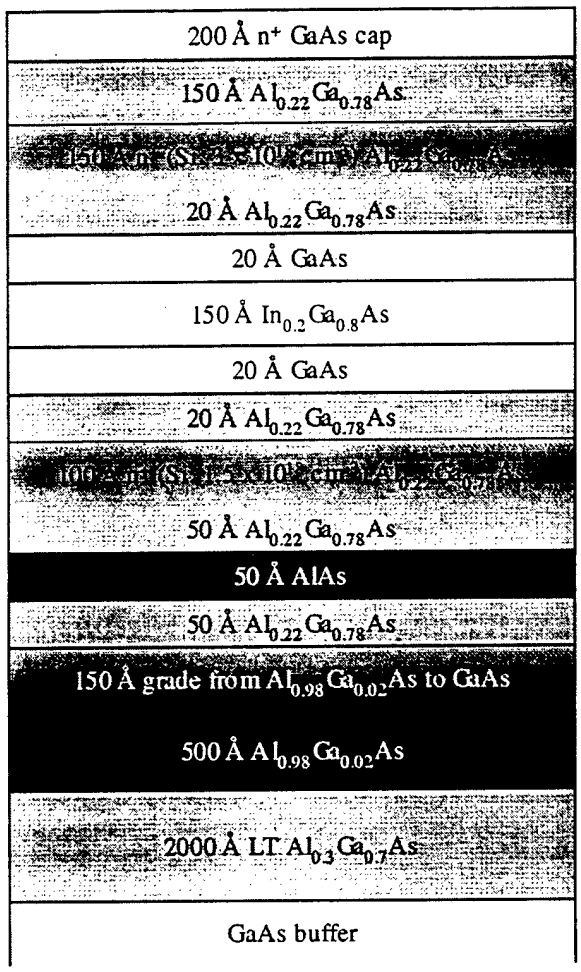


Fig 6.1: Layer structure of GaAs on Insulator pHEMT

[8] P. Parikh, "Oxide based Electronics in Gallium Arsenide", Ph.D. Thesis, ECE Technical Report # 98-16, University of California at Santa Barbara.

after the oxidation has been a serious problem for the application of GOI for FETs and HEMTs. The pHEMT structure is shown in Fig. 6.1. The growth conditions are presented in Table 6.1. The LT $Al_{0.3}GaAs$ buffer is grown underneath the $Al_{0.98}GaAs$ layer to assist the oxidation process. The active device layer is capped with an AlAs etch stop layer and GaAs cap layer to protect it during oxidation.

Nominal Growth Temperature (°C)	Channel Growth Temperature (°C)	Channel Growth Rate (μm/hour)	LT $Al_{0.3}Ga_{0.7}As$ Growth Temperature (°C)	LT $Al_{0.3}Ga_{0.7}As$ Anneal Temperature (°C)
530	480	1.25	270	550

Table 6.1: Growth conditions for GOI pHEMT

To determine the effect of oxidation on the pHEMT electrical characteristics Hall samples were prepared. Results of the Hall measurements for unoxidized and oxidized samples ($T_{oxidation}$ = 400,

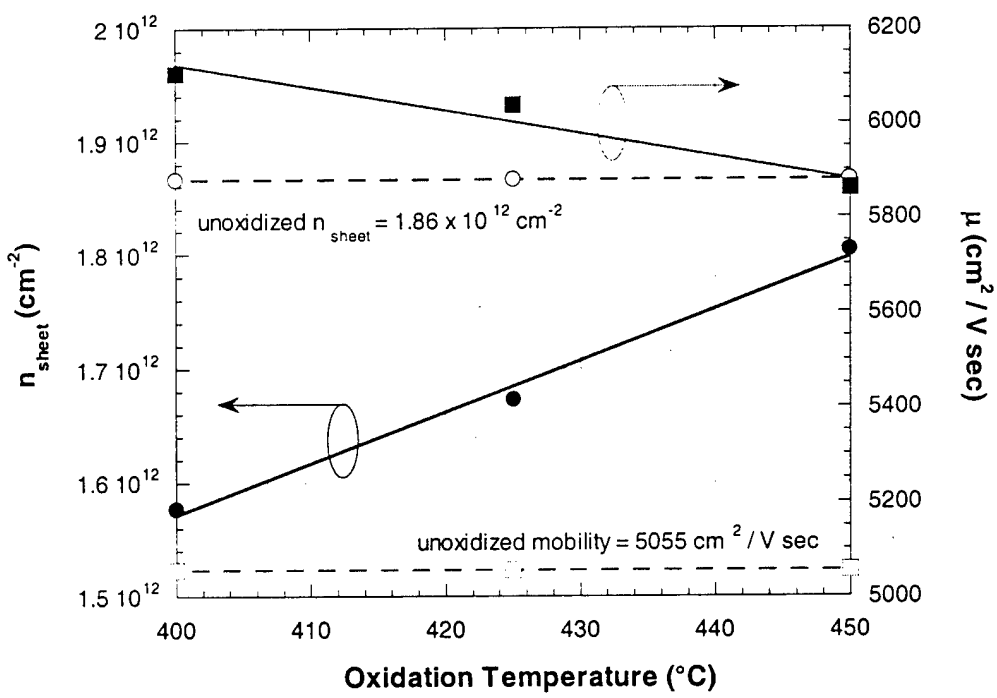


Figure 6.2: Plot of sheet concentration and mobility versus oxidation temperature

425, 450 °C) are presented in Fig. 6.2.

The results of the Hall measurements are very promising. The sheet concentration (n_{sh}) after oxidation decreases with comparison to the unoxidized sample. The exact reason as to why this occurs is still unknown, but it is believed that a compensating species is generated during the oxidation, which reduces n_{sh} but has no effect on the mobility (μ) of the sample. In this case there is approximately a 20 % increase in μ.

Though the results of the Hall experiment were promising as far as the effect of oxidation on the GaAs pHEMT is concerned, the original structure shows lower than expected n_{sh} and μ. The growth of the structure was reexamined and a series of new growth were preformed using the same structure but under different conditions, see Table 6.2.

Nominal Growth Temperature (°C)	**Channel Growth Temperature (°C)**	**Channel Growth Rate (μm/hour)**	LT $Al_{0.3}Ga_{0.7}As$ Growth Temperature (°C)	**LT $Al_{0.3}Ga_{0.7}As$ Anneal Temperature (°C)**
530	**490**	**0.625**	270	**600**

*Table 6.2. Growth conditions for the pHEMT (altered values in **bold** print)*

The results of Hall measurements on these samples are presented in Fig. 6.3.

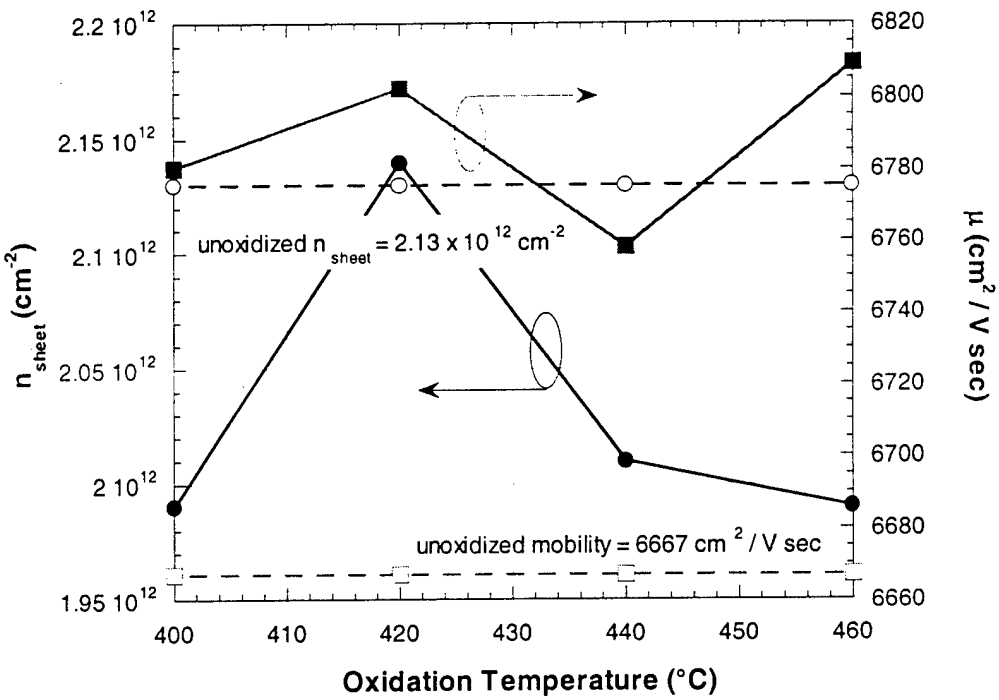


Figure 6.3: Plots of Hall measurements for new growth

In the new growths there is a maximum change of only 6.5 % in n_{sh} and an increase in μ of ~2 % over the entire oxidation range. In addition, the unoxidized values for n_{sh} (2.13 x 10^{12} cm^{-2}) and μ (6667 cm^2 / V sec) are at acceptable levels.

7. High-speed 1.55μm n-i-n photodetectors using LT-GaAs

It has been shown that low-temperature grown GaAs (LT-GaAs) can absorb long wavelength light (1~1.6 μm) by mid gap defect centers or As precipitates[9][10]. Previous results[11] have shown that the traveling wave photodetectors using LT-GaAs can have high frequency response in the long wavelength regime (1.55μm). We utilize a novel n-i-n (i-LT-GaAs) photodetector to study the carrier transport in LT-GaAs. Compared to a conventional p-i-n structure at the different bias, a higher efficiency is obtained with high-speed performance.

As shown in Figure 7.1, to improve the low absorption coefficient of LT-GaAs at long wavelengths, a waveguide structure of photodetectors were designed and fabricated. In contrast

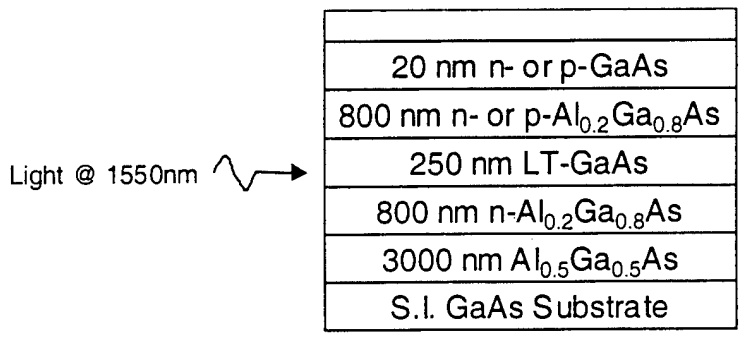


Figure 7.1: Layer structure of waveguide photodetector

to the top illuminated detectors, the waveguide length can be made long to have a large volume to complete the light absorption. The optical waveguide was formed by MBE-grown n-i-n and p-i-n heterostructure. A 250 nm thick LT-GaAs (i-layer) was deposited at 230°C and *in-situ* annealed at 600°C. N- and p- cladding layers were doped with Si and Be (above $3\times10^{18}\,cm^{-3}$). Standard self-aligned p-i-n photodetector processing was used[12]. A HP optical component network analyzer (8703A) was used to measure frequency response.

Two structures of photodetectors (n-i-n and p-i-n) were compared with the same design, material growth and fabrication except for the top p-cladding layer growth and p-contact metallization, where the waveguides are 3μm wide and 100μm long. Because the Fermi level is

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[9] A. Srinivasan et al. J. of Electronic Materials, 12, p.1457, 1993.
[10] A. C. Warren et al., IEEE Electron Device Lett. 10, p. 527, 1991.
[11] Y.J. Chiu, et al., Elec. Lett., 34, p1253,1998.
[12] Y.J. Chiu, et al., Elec. Lett., 34, p1253,1998.

pinned in the LT-GaAs[13], in a p-i-n structure, most of the applied voltage is dropped in the junction of p- and i-layers. To overcome the junction voltage, the n-i junction has an advantage over the p-i type since the electron barrier is only around half energy bandgap (0.7 eV in GaAs). Therefore, the efficiency can be enhanced by the applied voltage. Figure 7.2 shows the D.C. photocurrent and dark current of the n-i-n and p-i-n structures. The n-i-n structure has at least 4 times larger responsivity than the p-i-n structure. The responsivity is around 2 mA/W at 8V and

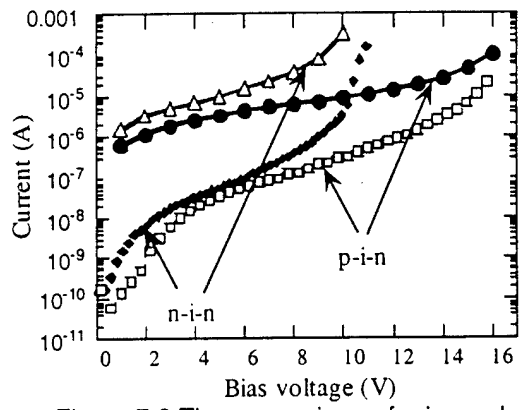

Figure 7.2 The comparison of n-i-n and p-i-n structures. The solid curves are photocurrent. The dashed curves are dark current.

0.06 A/W even at 9.5 V. The coupling efficiency is about 30%. The efficiency increases about one order of magnitude from 1 V to 8 V. By comparing different lengths of devices, as shown in Figure 7.3, it was found that the optical modal-absorption coefficient ($\Gamma\alpha$) is about 50 μm at the bias of interest (2~8 V), indicating that the amount of optical light absorbed in the waveguide is the same with the bias. Hence, The reason causing the monotonous increase in the

[13] Ibbetson, J.P et al; Appl. Phys. Lett, 68, p3781, 1996.

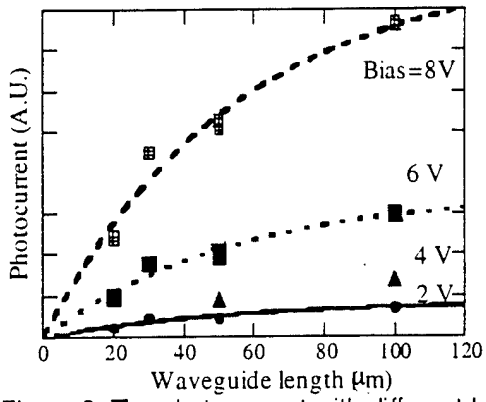

Figure 3. The photocurrent with different length devices. By fitting photocurrent with length, the modal absorption coefficient is about 50 μm at bias 2~8 V.

n-i-n photocurrent (2~8 V) is mainly due to the decreasing of carrier trapping time at the high electric field (carrier saturation field is around at bias 2.5V) [14]. As shown in Figure 7.4, the frequency response shows that the n-i-n structures have only 2 dB drop at 20GHz below 8V.

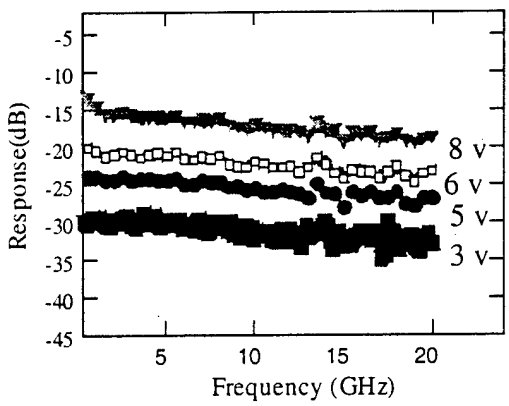

Figure 7.4: the frequency response of n-i-n structure.

The microwave loss extracted from s-parameter measurement is around 1dB at 20GHz for a 100 μm long detector. It ensures that the device speed is dominated by the microwave loss mechanism.

In summary, we have successfully fabricated a novel n-i-n photodetector operating at 1.55 μm on GaAs. The characteristics of the high-speed (above 20 GHz) and the considerable high efficiency at high bias show that this kind of photodetector has potential application in the fields

[14] Ibbetson, J.P et al; Appl. Phys. Lett, 68, p3781, 1996.

of long-wavelength-optical-fiber communication and for integration with GaAs integrated circuits.

8. LT GaAs Photomixers

Terahertz radiation can be generated by optical heterodyne conversion in a LT GaAs MSM photodetector. Two frequency-offset laser beams are used to illuminate voltage biased inter-digitated electrodes, resulting in an AC current at the difference frequency that drives a miniature planar antenna. There are several applications that could benefit from such a compact solid-state THz source including high-resolution molecular spectroscopy, remote sensing, and sub-mm wave astronomy.

Thermal failure of LT GaAs photomixers was investigated and a novel photomixer structure has been developed to provide increased THz power. It was found that thermal conductivity of LT GaAs is significantly reduced relative to stochiometric GaAs, which affects heat flow in the device. By reducing the thickness of LT GaAs layer and incorporating a transparent, high thermal conductivity AlAs layer, the thermal impedance of the photomixer can be greatly reduced. This structure also provides significantly enhanced optical and electrical power conversion efficiencies.

(Please see attached reprint and abstract for a detailed discussion)

9. Oxide Aperture Heterojunction Bipolar Transistors

9.1 Introduction

In addition to lattice-engineered substrates and GaAs-On-Insulator, the application of an oxide aperture to heterojunction bipolar transistors (HBTs) for high-speed application has been studied under the PRET program.

Heterojunction bipolar transistors (HBTs) have been extensively examined as a device for high-speed applications[15,16]. Additionally, double-heterojunction bipolar transistors (DHBTs) have been examined for microwave power applications[17].

The high-speed performance of these devices are represented through the two figures of merit: f_τ and f_{max}. For bipolar junction transistors (BJTs) and HBTs, these figures of merit are characterized by the following equations:

$$f_\tau = \frac{1}{2\pi}(\tau_E + \tau_B + \tau_C + \tau_{CC})^{-1}$$

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}}$$

In the equation for f_τ, τ_E is the emitter-charging time (associated with the charging of the device capacitances through the emitter-base junction), τ_B is the base transit time (associated with the diffusion of minority carriers across the base), τ_C is the collector transit time (associated with the transit of carriers across the collector space-charge region), and τ_{CC} is the collector-charging time (associated with the charging of the base-collector capacitor). In the equation for f_{max}, R_B is the base resistance and C_{BC} is the base-collector capacitance of the HBT.

However, the speed and microwave performance of these devices is commonly limited by parasitic components such as the extrinsic base resistance and the extrinsic base-collector capacitance. To reduce the effect of these parasitic components, techniques such as highly-

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[15] Kroemer, H.; Proceedings of the IEEE, 70, p13, 1982.
[16] Asbeck, P. M. et al; IEEE Transactions on Electron Devices, 36, p2032, 1989.
[17] Liu, W. et al; IEEE Electron Device Letters, 16, p309, 1995.

doped, regrown base contacts[18], ion implantation into the collector and sub-collector[19], undercut collectors[20], and transferred substrate[21] have been used.

The concept common among most of these approaches is the increase of f_{max} by means of reducing the base-collector capacitor. Our research is similarly concerned with increasing fmax by means of reducing C_{BC}. To this end we have examined two methods for the reduction of C_{BC}: the use of an oxide aperture in the collector in an emitter-up design to reduce the overall permittivity of the collector and thereby its capacitance and the use of an oxide aperture in the emitter of a collector-up design to act as a current aperture, maintaining a high gain (Figure 9.1).

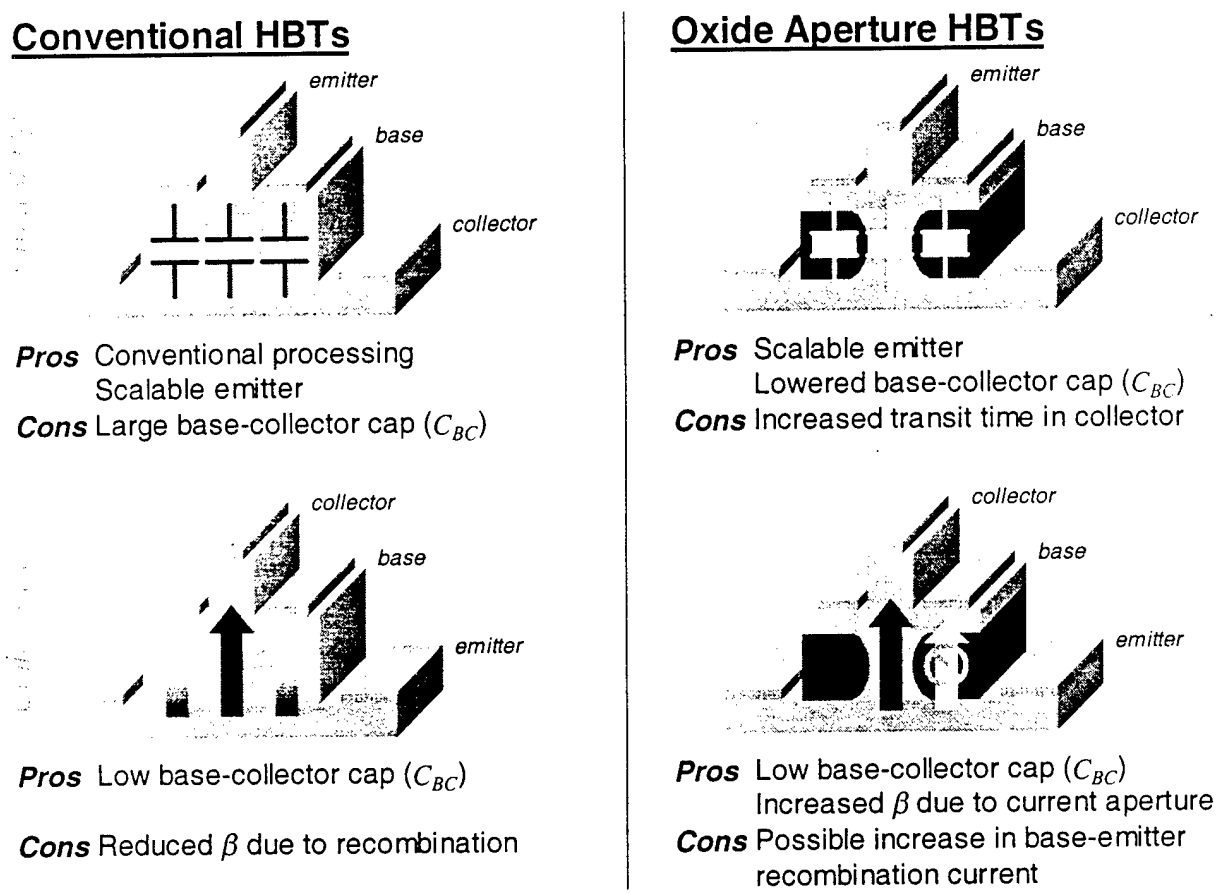

Figure 9.1: Comparison of conventional HBTs and oxide aperture HBTs

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[18] Shimawaki, H. et al; IEEE Transactions on Electron Devices, 42, p1735, 1995.
[19] Ho, M. C. et al; IEEE Electron Device Letters, 16, p512, 1995.
[20] Chau, H.-F. et al; IEEE Microwave and Guided Wave Letters, 7, p288, 1997.
[21] Lee, Q. et al; IEEE Electron Device Letters, 19, p77, 1998.

9.2 Emitter-Up Oxide Aperture HBTs

Presented here is an alternative method to reduce C_{BC} by reducing the base-collector capacitor's relative permittivity (ε_r). By introduction of an oxide aperture into the collector of a HBT, the ε_r of that portion of the collector can be reduced from 10.9 ($\varepsilon_{r,AlAs}$) to 5.8 ($\varepsilon_{r,GaAs}$), and thereby the overall capacitance of the junction is reduced. The subsequent removal of the oxide to form an air aperture ($\varepsilon_{r,air} = 1$) results in a further reduction of the junction's capacitance. Application of the oxide and air aperture to HBTs is discussed. Specifically, the resulting possible implications for f_τ and f_{max} are examined.

Two structures to examine the effect of the oxide and air aperture were grown by solid-source molecular beam epitaxy. Both structures were grown on semi-insulating GaAs substrates. Structure A consisted of a 6000 Å n^+ (Si: 4×10^{18} cm^{-3}) GaAs buffer/sub-collector layer, a 2500 Å n^- (Si: 3×10^{16} cm^{-3}) $Al_{0.92}Ga_{0.08}As$ layer to be converted to oxide and a 2500 Å n^- (Si: 3×10^{16} cm^{-3}) linear grade from $Al_{0.92}Ga_{0.08}As$ to GaAs collectively referred to as the collector. The grade from $Al_{0.92}Ga_{0.08}As$ to GaAs in the collector is required to remove the triangular "notch" in the conduction band that would normally be produced between the highly-doped, small bandgap, p-type GaAs base and the low-doped, large bandgap, n-type $Al_{0.92}Ga_{0.08}As$ collector. The removal of this "notch", from a transistor point of view, is critical because any parasitic charge storage would lead to additional delays in the device. Additionally, a "long" grade is required to remove the kink in the conduction band associated with the transition from the X-valley to the Γ-valley in $Al_xGa_{1-x}As$ at $x_{Al} = 0.43$, for the same reason. Following the collector a 500 Å p^+ (Be: 1×10^{19} cm^{-3}) GaAs base layer, capped with a 50 Å AlAs etch stop layer and a 200 Å undoped GaAs layer to protect the structure during oxidation were grown. Structure B is identical to Structure A except that the collector region is replaced by a 4600 Å n- (Si: 3×10^{16} cm^{-3}) $Al_{0.92}Ga_{0.08}As$ layer, a 300 Å n- linear grade from $Al_{0.92}Ga_{0.08}As$ to GaAs with a 100 Å highly doped (Te: 4×10^{18} cm^{-3}) region located 150 Å from the beginning of the grade, and a 100 Å n^- GaAs layer. The requirement for the long grade is removed in Structure B by highly doping the region around the transition point between the X-valley and the Γ-valley. Figure 9.2 shows the band diagrams for Structures A and B, indicating the collector region and the graded regions for both structures.

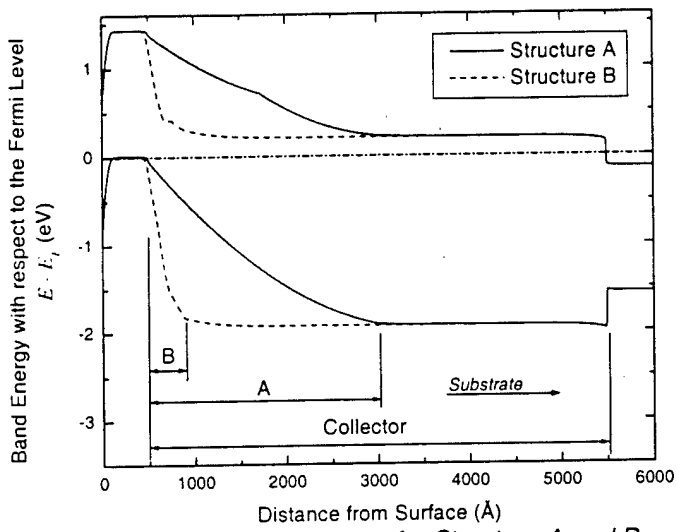

Figure 9.2: Bands diagrams for Structure A and B

Large-area mesa diodes (A_{cap} = 452.5 kμm^2) were fabricated using standard processing techniques. First, the mesa was defined using contact photolithography and a chlorine-based reactive-ion-etch (RIE). Following the mesa RIE, the samples were oxidized in a water-vapor atmosphere ($T_{oxidation}$ = 425 °C, T_{H_2O} = 90 °C). Next, the protective GaAs cap was removed by a citric acid-based etch, followed by a short phosphoric acid-based dip to remove the AlAs etch stop. Finally, using standard contact photolithography and e-beam evaporation, the Ti/Au contacts were defined on the p$^+$-base and n$^+$-sub-collector. This completed the fabrication of the oxide aperture diodes.

Capacitance-voltage (CV) measurements were performed on samples oxidized for 0, 10, 20, 30, 45, 60, and 120 minutes. Figure 9.3 shows a plot of a typical CV measurement for a sample oxidized for 60 minutes. The fraction of oxidized junction area is represented as:

$$\delta = \frac{A_{oxide}}{A_J}$$

where A_{oxide} is the area of the oxidized portion of the diode and A_J is the area of the total junction. The oxidized capacitance of the diode (C) with respect to the unoxidized capacitance of the diode ($C_0 = C(t = 0$ minutes)) for a fully depleted collector versus δ for both structures is plotted in

Figure 9.4. Reductions in capacitance of up to 20 % and 30 % were observed for the Structure A and B, respectively.

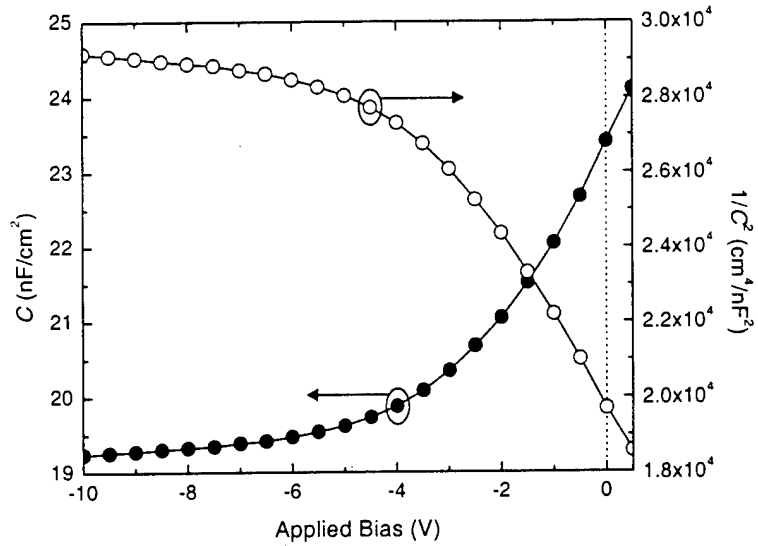

Figure 9.3: Typical CV measurement. $t_{oxidation}$ *= 60 minutes*

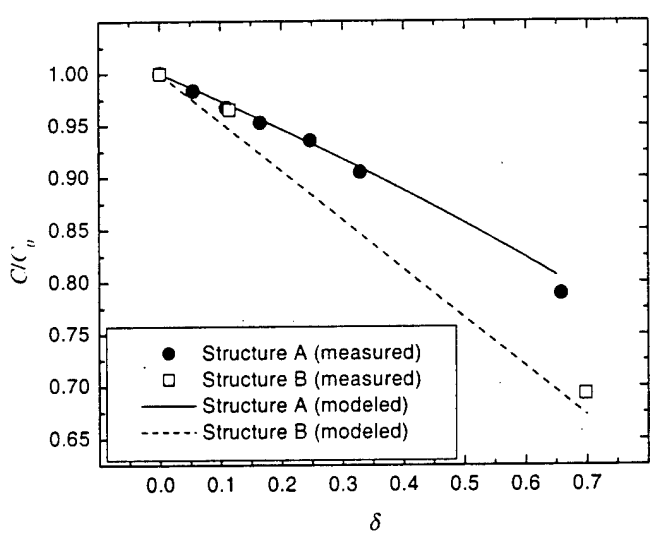

Figure 9.4: Relative capacitance versus fraction of oxidized collector

The total capacitance of the junction may be modeled as a network of simple parallel plate capacitors. Examining the diode structure, the capacitor network is as shown in Figure 9.5. From this capacitor network C/C_0 is easily calculated:

$$\frac{C}{C_o} = \frac{\varepsilon_{grade} d_{oxide} + \varepsilon_{unox} d_{grade}}{\varepsilon_{unox}} \frac{\varepsilon_{unox}(1-\delta) + \varepsilon_{oxide}\delta}{\varepsilon_{grade} d_{oxide} + \left[\varepsilon_{unox}(1-\delta) + \varepsilon_{oxide}\delta\right] d_{grade}}$$

Figure 9.4 shows the results of the model plotted against the measured results.

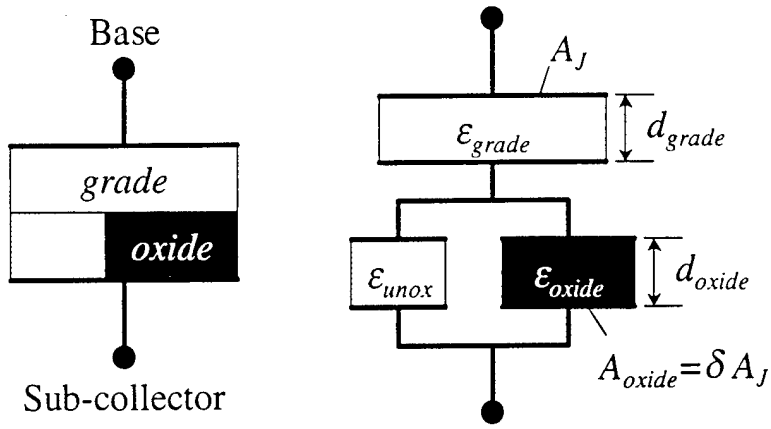

Figure 9.5: Capacitor network representation of BC junction

After testing was completed on the oxide aperture diodes, the samples were placed into a solution of KOH:H_2O (1:12 by vol.) to selectively remove the oxide aperture from the diode structure[22]. This resulted in air aperture diodes.

The CV measurements were repeated on the air aperture diodes. The results of these measurements versus δ for both Structure A and B are plotted in Fig. 5. Reductions in capacitance of up to 40 % and 60 % were observed for Structures A and B, respectively, with the air aperture. The same model for the capacitance of the junction used for the oxide aperture diode may be used here for the air aperture diode with the replacement of ε_{oxide} by ε_{air}. Figure 9.6 shows the results of the model plotted against the measured results.

[22] Naone, R. L. et al; IEEE Photonics Technology Letters, 11, p1339, 1999.

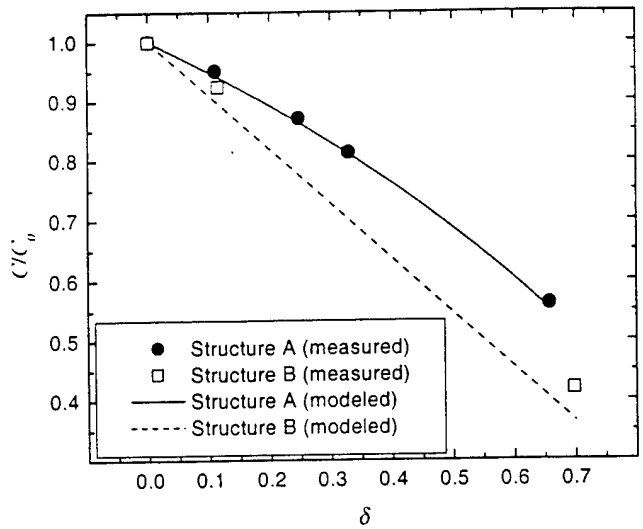

Figure 9.6: Relative capacitance versus fraction of air aperture collector

In examining the impact of the oxide aperture and the air aperture on the high-frequency figures of merit of a HBT, we first consider f_τ. This is due to the dependence of f_{max} upon f_τ, given by:

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}}$$

To simplify the analysis it is assumed that f_τ is dominated by the transit time across the collector space-charge region, τ_C. Therefore, f_τ reduces to:

$$f_\tau = \frac{1}{2\pi\tau_C}$$

For a homogenous collector, τ_C is of the well-known form:

$$\tau_C = \frac{W_C}{2v_{sat}} = \frac{d_C}{2v_{sat}}$$

where W_C is the depletion width in the collector, which is commonly equal to d_C, the thickness of the collector, and v_{sat} is the saturation velocity of the carriers in the collector. For the case of a

heterogeneous collector, in which v_{sat} varies as a function of distance from the base-collector junction this equation does not hold.

For cases where v_{sat} does vary as a function of distance into the collector it has been shown[23,24]:

$$\tau_C = \langle t \rangle_C = \frac{\int_0^{t_f} t v(t)\,dt}{\int_0^{t_f} v(t)\,dt}$$

where τ_C is the centroid in time of the velocity profile in the collector space-charge region. This equation reduces to the previous equation in the case of a homogeneous collector.

The proposed velocity profiles for the structures presented in this letter are shown in Figure 9.7. Taking $v_{sat,GaAs}$ and $v_{sat,AlAs}$ to be 2×10^7 cm/sec and 1×10^7 cm/sec, respectively, and the thickness of the oxide/air aperture and the collector from their respective layer structures, the calculated transit times for Structures A and B, for the oxide aperture and air aperture cases, are: $\tau_{CA} = \tau_{CA,oxide} = \tau_{CA,air} = 1.88$ psec, $\tau_{CB} = \tau_{CB,oxide} = \tau_{CB,air} = 2.35$ psec. For a homogeneous GaAs collector the calculated transit time is $\tau_{C,GaAs} = 1.25$ psec. Therefore, Structures A and B would suffer decreases in f_τ of $1/3$ and $1/2$, respectively.

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[23] Ishibashi, T.; IEEE Transactions on Electron Devices, 37, p2103, 1990.
[24] Bhattacharya, U.; Santa Barbara: University of California, p135, 1996.

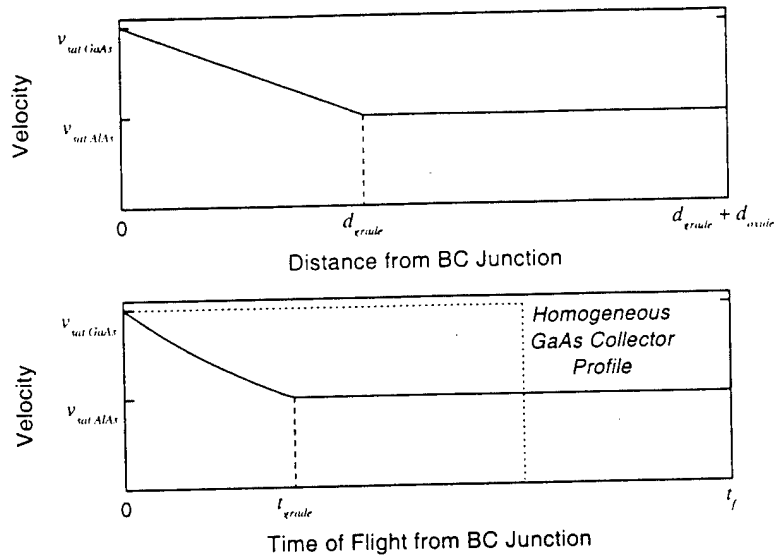

Figure 9.7: Velocity profiles versus distance and time

We now consider f_{max}. Solving for f_{max} of an oxide aperture or an air aperture collector device with respect to a homogeneous GaAs collector device results with the following equation:

$$\frac{f_{max}}{f_{max,GaAs}} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}} \Bigg/ \sqrt{\frac{f_{\tau,GaAs}}{8\pi R_B C_{BC,GaAs}}} = \sqrt{\frac{f_\tau}{f_{\tau,GaAs}} \Bigg/ \frac{C_{BC}}{C_{BC,GaAs}}} = \left(\frac{\tau_C}{\tau_{C,GaAs}} \frac{C_{BC}}{C_{BC,GaAs}} \right)^{-1/2}$$

where R_B is considered equal in both the oxide/air aperture and homogeneous GaAs devices; variables with the *GaAs* subscript correspond to the homogeneous GaAs collector device, variables without the *GaAs* subscript correspond to the oxide/air aperture collector device. It should be noted that the ratio of capacitances in this equation is not the same as that presented earlier but is given by:

$$\frac{C_{BC}}{C_{BC,GaAs}} = \left(d_{oxide} + d_{grade}\right) \frac{\varepsilon_{unox}(1-\delta) + \varepsilon_{oxide}\delta}{\varepsilon_{grade} d_{oxide} + \left[\varepsilon_{unox}(1-\delta) + \varepsilon_{oxide}\delta\right] d_{grade}}$$

The difference comes from comparing the capacitance of the oxide/air aperture junction (C) to its unoxidized counterpart (C_0) and comparing the capacitance of the oxide/air aperture device ($C_{BC} = C$) to the capacitance of a homogeneous GaAs device ($C_{BC,GaAs}$). Note, the above equation is specifically for the case of an oxide aperture collector device. For the case of an air aperture collector device ε_{oxide} must be replaced by ε_{air}. Figure 9.8 shows a plot of **Error! Reference source not found.** as a function of δ for Structures A and B with the oxide aperture. Figure 9.9 shows a similar plot for both structures with the air aperture.

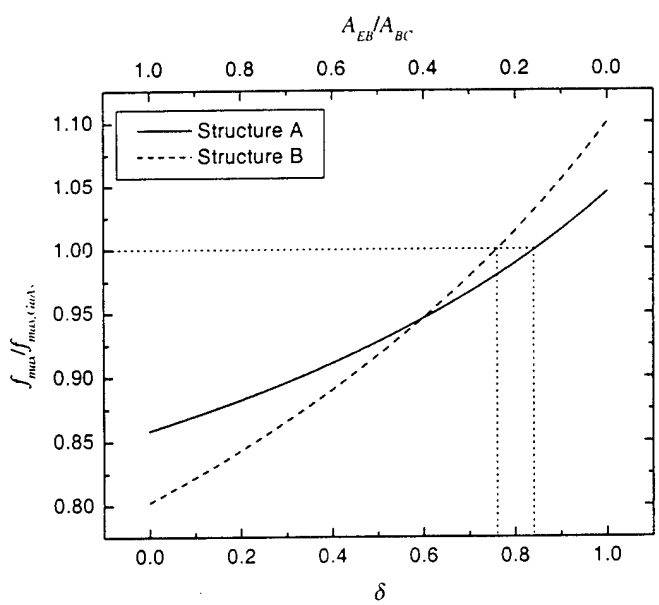

Figure 9.8: Plot of f_{max} versus δ

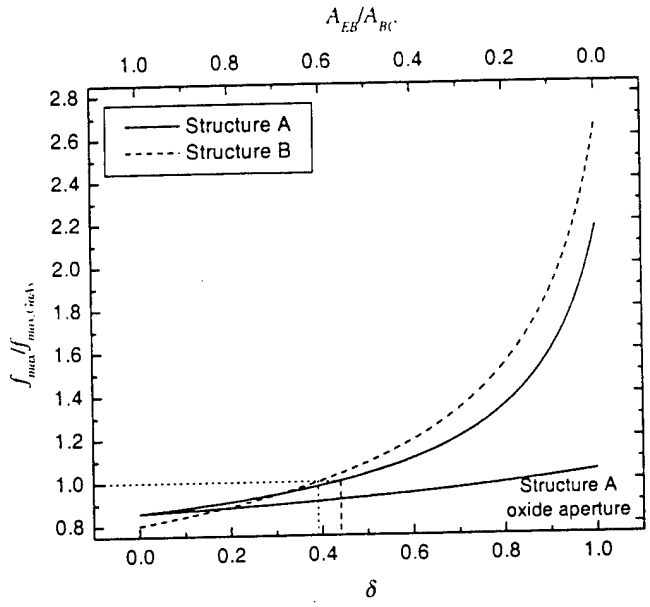

Figure 9.9: Plot of f_{max} versus δ

Recall that δ is defined as the ratio of the oxide area, A_{oxide}, to the total junction area, A_{BC}. In a HBT, for maximum impact on the transistor's f_{max}, it would be desirable to have all but the area directly under the emitter to be oxidized, see Figure 9.10.

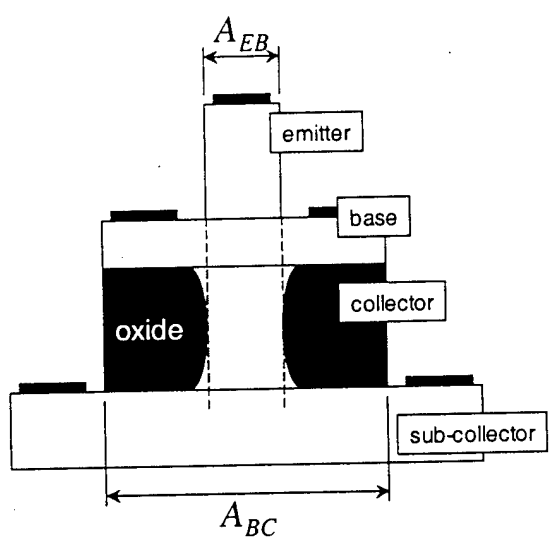

Figure 9.10: Graphic of emitter-up oxide aperture HBT

Rewriting δ in terms of device areas results in:

$$\delta = \frac{A_{oxide}}{A_J} = \frac{A_{BC} - A_{EB}}{A_{BC}} = 1 - \frac{A_{EB}}{A_{BC}}$$

where A_{EB} is the area of the emitter-base junction/emitter mesa and A_{BC} is the area of the base-collector junction/mesa. One can see immediately from Figure 9.8 and Figure 9.9 that the maximum attainable improvement in f_{max} for an oxide aperture collector as compared to a homogeneous GaAs collector device is approximately 10 %, but for an air aperture collector as compared to a homogeneous GaAs collector device this increases to approximately 160 %. However, HBTs are commonly fabricated with an emitter to collector ratio (A_{EB}/A_{BC}) on the order of 1/3. Therefore, from examining Figure 9.8 and Figure 9.9, one would expect essentially no advantage in the use of an oxide aperture, but an increase in f_{max} of approximately 50 % could still be obtained with the use of an air aperture design.

In the final examination it was found that the oxide aperture collector design, though providing a definite reduction in junction capacitance, would provide a minimally positive impact on f_{max}, associated with a reduction in f_T. The air aperture collector design, on the other hand, could offer a dramatic increase in f_{max}, though still accompanied by a reduction in f_T.

9.3 Collector-Up Oxide Aperture HBT

Initial research into the collector-up oxide aperture HBT design has just begun. It is believed that this design will show far better performance than the emitter-up design because the oxidized material does not reside in the collector, which would slow the device down, but instead reside in the emitter acting as a current aperture similar to those found in vertical cavity lasers. This combined with the application of InP lattice-matched materials such as $GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and $In_{0.53}Ga_{0.47}As$ should result in a high-gain, low-power, high-speed device.