International Semiconductor Device Research Symposium

FINAL REPORT

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June 29, 2000

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STATEMENT OF THE PROBLEM

The International Semiconductor Device Research Symposium (ISDRS) is held biannually in Charlottesville, Virginia. Since its inception in 1991, it has developed an international reputation as a convivial, collegial, and effective forum for the exchange of the latest results and ideas relating to semiconductor device research. Technical themes of the conference include new device concepts, device characterization, processing, new materials, simulation, and nanoelectronics. The conference has an international program committee of over thirty internationally renowned scientists from the United States, Canada, Europe, the former Soviet Union, and the Far East.

Recurring themes of this conference include an unusually international attendance and a very strong emphasis on student participation. The structure of the conference consists primarily of focussed topical sessions with no more than two sessions in parallel. In addition, there are poster and plenary sessions. There is also an active social program of receptions, mixers, and conference meals. The conference is entirely sited within one hotel (the Charlottesville Omni) which is at one end of a small pedestrian mall with a multitude of restaurants. The number of participants is usually around 150 to 200.

SUMMARY OF RESULTS

The 1999 International Semiconductor Device Research Symposium was held from December 1 to December 3 of 1999. There was an approximate total of 150 participants representing research groups from the United States, Canada, Europe, the former Soviet Union, Japan, and China. The conference addressed an number of topics with particular relevance to ARO research in electronics including nanoscale devices, optoelectronics, wide bandgap devices, infrared sensor arrays, advanced processing techniques, self-assembled nanostructures and millimeter/microwave circuits and devices. The funding provided though this Army Research Grant (DAAD19-99-1-0369, $2,500) was used to support student travel and participation in the conference. Specific student support included (1) reduced registration fees, (2) conference proceedings, (3) attendance at the conference awards banquet, and (4) lodging at the conference facility. It is estimated that approximately one-quarter of the attendees were student participants.

PUBLICATIONS AND TECHNICAL REPORTS

The primary publication resulting from this program is the Symposium Proceedings that contain all paper presented at the conference. Six copies of the Proceedings are included with this final report.

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13. ABSTRACT (Maximum 200 words)

The International Semiconductor Device Research Symposium (ISDRS) is held biannually in Charlottesville, Virginia. Since its inception in 1991, it has developed an international reputation as a convivial, collegial, and effective forum for the exchange of the latest results and ideas relating to semiconductor device research. Recurring themes of the conference include an unusually international attendence and a very strong emphasis on student participation. The range of topics addressed by the conference include many areas that directly impact research supported by the Army Research Office. These include nanoscale devices, optoelectronics, self-assembled systems, advanced fabrication technology, and microwave/millimeter-wave devices.

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Enclosure 1

PROCEEDINGS

1999 INTERNATIONAL SEMICONDUCTOR DEVICE RESEARCH SYMPOSIUM

December 1 - 3, 1999 • Omni Charlottesville Hotel



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VIRGINIA INSTITUTE
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University of Virginia

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ENGINEERING & APPLIED SCIENCE
Academic Outreach

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Semiconductor

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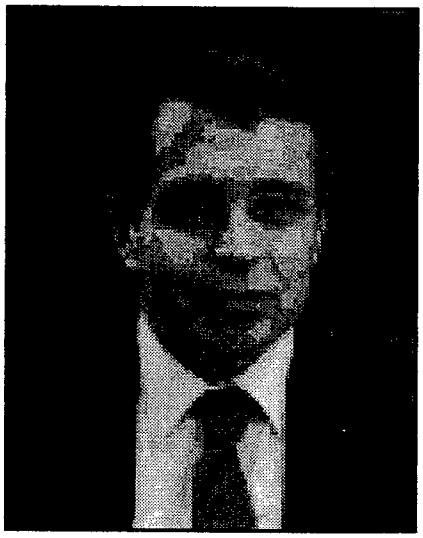


Professor Aldert van der Ziel

(December 12, 1910 - January 20, 1991)

The van der Ziel Award, sponsored by White Oak Semiconductor, was established in honor of Professor Aldert van der Ziel for his long, distinguished and illustrious career as an educator and a research scientist.

Past recipients of the Aldert van der Ziel Award include Arthur Milnes, Lester Eastman and Herbert Kroemer. The Aldert van der Ziel Award for 1999 will be presented to Professor Michael Shur of Rensselaer Polytechnic Institute.



MICHAEL SHUR

Michael Shur received his M.S.E.E. degree (with honors from St. Petersburg Electrotechnical Institute in 1965, Ph.D. in Physics from A.F. Ioffe Institute in 1967, Doctor of Science degree from A.F. Ioffe Institute in 1992. He has held research or faculty positions at A.F. Ioffe Institute, Wayne State University, Oakland University, Cornell University, IBM T.J. Watson Research Center, and the University of Minnesota. From 1989 to 1996, he was John Money Professor at the University of Virginia, where he served as Director of Applied ElectroPhysics laboratories in 1996. He is currently Patricia W. and Sheldon C. Roberts Professor of Solid State Electronics, Professor of Physics, Professor of Information Technology, and Associate Director of the Center for Integrated Electronics and Electronics Manufacturing at Rensselaer Polytechnic Institute. He has published many papers and books and holds many patents on solid-state devices. He is Fellow of IEEE, Fellow of the American Physical Society, a member of Eta Kappa Nu and Tau Beta Pi, a former Chair of the US Chapter of Commission D of the International Union of Radio Science, a member of the Electrochemical Society, Materials Research Society, and SPIE, Editor-in-Chief of the International Journal of High Speed Electronics and Systems, and a member of the Honorary Editorial Board of Solid State Electronics Magazine. In 1990-1993, he served as an Associate Editor of IEEE Transactions. He has also served as a Commitee Member, Chair, and Organizer at many conferences and as a member of the IEEE Awards Committee. He has given many invited, keynote, and plenary talks and lectures. In 1994, Saint Petersburg State Technical University awarded him an Honorary Doctorate. In 1996, he was a co-recipient of the A.F. Ioffe Institute Award for his work on plasma wave electronics. In 1998, he co-authored a paper that received Best Paper Award at GOMAC Conference. In 1999, he received a Commendation for Excellence in Technical Communications from the Editors of Laser Focus World magazine.

1999 INTERNATIONAL SEMICONDUCTOR DEVICE RESEARCH SYMPOSIUM

HISTORY OF SYMPOSIUM OFFICERS

YEAR	SYMPOSIUM CHAIR	PROGRAM CHAIR	LOCAL ARRANGEMENTS
1999	William Peatman Chris Mann	Agis Iliadis Holly Slade	Robert Weikle
1997	Robert Hull Sean McAlister	William Peatman	Robert Weikle
1995	Elias Towe Federico Capasso	Stephen Jones	William Peatman
1993	Michael Shur	Elias Towe	Stephen Jones
1991	Robert Mattauch	Michael Shur	Stephen Jones

YEAR	TREASURER	SECRETARY	PUBLICITY
1999	Robert Weikle	—	Greg Tait
1997	Robert Mattauch	Michael Hurt	—
1995	Robert Weikle	Holly Slade	Michael Spencer
1993	William Peatman	—	—
1991	—	—	—

ALDERT VAN DER ZIEL AWARDS

YEAR	RECIPIENT	AFFILIATION
1999	Michael Shur	Rensselaer Polytechnic Inst
1997	Herbert Kroemer	UC - Santa Barbara
1995	Lester F. Eastman	Cornell University
1993	Arthur G. Milnes	Carnegie Mellon University

BEST STUDENT PAPER AWARDS

YEAR	RECIPIENT	AFFILIATION
1997	Dennis Sylvester	UC - Berkeley
	Wen-Chin Lee	UC - Berkeley
1995	Erno Klaassen	Stanford University
1993	Edgar Martinez	Wright Laboratory
	Kaushik Bhaumik	Cornell University
1991	R. Mickevičius	Wayne State University

Introduction

This volume contains the Proceedings of the Fifth International Semiconductor Device Research Symposium (ISDRS-99, Charlottesville,Virginia, December 1-3, 1999).

The goal of this international meeting is to provide a congenial forum for the exchange of information and new ideas for researchers from university, industry and government laboratories in the field of semiconductor devices and device physics. To this end, we have an unusually short period between the submission of papers and the conference, a speedy publication of the proceedings, and a wide dissemination of the conference proceedings. This conference is endorsed by the IEEE MTT Society, IEEE EDS, and the United States National Committee of URSI.

The program committee received submissions from 25 countries, representing 4 continents. Of the received abstracts, 90 have been selected for oral presentations and about 50 for poster presentations. These papers cover a broad range of topics, including photonics and optoelectronics, new device fabrication technologies, novel semiconductor devices, nanoelectronics, SiGe circuits and devices, wide band gap materials and devices, microwave devices, characterization techniques, SOI device technology, and simulation and modeling. It is hoped that such a broad range of topics will foster a cross-fertilization of the different fields related to semiconductor materials and devices.

In addition to the regular sessions, we are very pleased to offer two Special Symposia this year. These are "Emerging Materials for Microelectronics" and "MEMS and Micromachining." The plenary session has three excellent talks by Professors Alivisatos of UC - Berkeley, Hadis Morkoç of Virginia Commonwealth University, and Jerry Woodall of Yale University. Furthermore, two panel discussions are planned: "Enabling Technologies for the New Millenium" and "THz Region: Battleground of the Photon and Electron."

The first ISDRS symposium in 1991 was dedicated to the memory of Professor Aldert van der Ziel who made seminal contribution to the theory of semiconductor devices, especially to the theory of noise, and who educated literally hundreds of graduate students. Past awardees include Arthur Milnes, Lester Eastman and Herbert Kroemer. We are pleased to announce that the 1999 award goes to Professor Michael Shur of Rensselaer Polytechnic Institute. Every year a Best Student Paper Award is chosen by the Organizing Committee at the close of the symposium from evaluations received from the participants. The 1997 Best Student Paper was awarded to two students of the University of California - Berkeley: Wen-Chin Lee for "Impact of Poly-$Si_{0.8}Ge_{0.2}$-Gate Technology on Device Performance and Reliability," and Dennis Sylvester for "Measurement-Based Interconnect Capacitance Characterization for Circuit Simulations."

ISDRS-99 was made possible by the generous support of the US Department of the Army, National Science Foundation, Virginia Commonwealth University, University of Virginia Institute for Microelectronics, and White Oak Semiconductor. We are also grateful to many individuals, including the Special Symposia chairs and the session chairs, and the international Symposium Co-Chairs, and others whose contributions have made the Symposium a success. Special thanks to L. Tawney for her dedication and superlative contributions to the program, registration and administrative functions. Finally we thank the authors for their technical abstracts.

We hope that you find the symposium stimulating and that you will look forward to ISDRS in 2001.

William Peatman, Symposium Co-Chair

Chris Mann, Symposium Co-Chair

Agis Iliadis, Symposium Program Co-Chair

Holly Slade, Symposium Program Co-Chair

Technical Sessions Schedule

	Time / Location	Room 1: Salon A	Room 2: Salon B	Room 3: Salon C
Tuesday November 30	4:00PM - 9:00PM	Conference Registration		
	7:00PM - 9:00PM	Conference Reception		
Wednesday, December 1	9:00AM–12:00AM	Plenary Session (in the Ballroom)		
	1:40PM–3:20PM	Photonics & Optoelectronics	New Device Fabrication Technologies	Poster Display
	3:50PM–5:30PM	Novel Semiconductor Devices	Nano-electronics	
	6:30PM 8-10PM	Poster Session/Recep Panel Discussions		
Thursday, December 2	8:30AM–10:10AM	SiGe (C) Devices	Wide Band Gap I	
	10:40AM–12:20PM	Micro Millimeter & Submillimeter Devices	Wide Band Gap II	
	1:40PM–3:20PM	Simulation & Modeling I	Advanced Concepts SOI - I	Poster Session Take Down
	3:50PM–5:30PM	Simulation & Modeling II	Advanced Concepts SOI - II	
	7:30PM–9:00PM	Symposium Awards Banquet		
Friday, December 3	8:30AM–10:10AM	Emerging Materials for Microelectronics	MEMS & Micromachining I	
	10:40PM–12:20PM	M&D Characterization Techniques - I	MEMS & Micromachining II	Late News Papers
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Semiconductor Nanocrystals as Building Blocks for New Electrical Devices

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ABSTRACT

In recent years there have been significant advances in the preparation of semiconductor quantum dots by colloidal chemistry routes. CdSe and InAs are examples of materials which can be made as nanocrystals of high quality. These nanocrystals provide an excellent proving grounds for examining size dependence scaling laws of physical properties, and a few examples will be described briefly. Colloidal nanocrystals may also be integrated into more complex structures, and three examples will be described. The first involves blends of nanocrystals semiconductor polymers to yield photovoltaics. A second example involves the integration of single nanocrystals into lithographically prepared transistors. Finally, efforts to use DNA to create complex spatial arrangements of nanocrystals will be described.

Nitride Semiconductors and Devices

by Hadis Morkoç

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Wide bandgap nitride semiconductors have been attracting a great level of attention owing to their direct bandgaps in the visible to ultraviolet regions of the spectrum as emitters and detectors. Emitters have advanced to the point where high efficiency blue and green LEDs and violet lasers are available. LEDs have found quick acceptance in display, lighting (now termed as solid state lighting), indicator light, advertisement, moving sign, and traffic sign/signal related applications. Lasers, as coherent sources, are expected to play a crucial role for high-density optical read and write technologies. Nitride based detectors are being developed for visible blind and solar blind regions of the spectrum for a variety of applications. On the electronics side, nitrides with favorable hetero-junctions and transport properties began to produce very respectable power and noise levels in microwave amplifiers. If and when the breakdown fields achieved experimentally approach the predicted values, this material system would also be very attractive for power switching devices also. More recently, quantum dots produced in GaN have become of special interest particularly in the light of lattice mismatch with available substrates. A number of scientific challenges remain including hetero-epitaxy related issues, extended and point defects, doping and a clear experimental investigation of polarization effects. In this paper, following a succinct review of the progress that has been made, spontaneous and piezoelectric

polarization effects and their impact on hetero-structures and recent developments in quantum dots will be discussed.

Technology Realization (at a University!) for Fun and Profit

Jerry M. Woodall,
C. Baldwin Sawyer Professor of Electrical Engineering
Yale University

Abstract:

For hundreds of years the main functions of universities were education, training and scholarship, including discoveries and breakthroughs in the sciences. About a decade ago, owing to severe global competition at the marketplace, major high tech corporations began scaling back and downsizing "blue sky" or "curiosity driven" research at their corporate R&D labs. As a result, breakthroughs and innovations in materials and devices were also added to the list of research university functions.

Very recently, large corporations have dramatically increased their reliance on outsourcing of product components. In addition, interest in adding a materials DESIGN science and engineering component to the overall functional design of products has been mounting. This has produced a "golden opportunity" for universities to participate in the rewards of technology realization, especially for niche market products, while still maintaining traditional academic purity.

Advanced Electronic and Optoelectronic Devices from Engineered type-II Sb-Based Superlattices

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Abstract:

III-V quantum wells and superlattices based on InAs/GaSb, AlSb, and related compounds have attracted many attentions due to their unique band alignments and physical properties. Recently, novel electronic and optoelectronic heterostructures have been proposed from this material system for hundred gigahertz logic circuits, terahertz transistors, RTDs, infrared lasers, and infrared detectors. In this paper we will describe the ongoing research at the Center for Quantum Devices to develop the theory, modeling, growth, characterization, and device fabrication techniques for this material system. We have demonstrated the first uncooled infrared detectors from type-II superlattices. The measured detectivity is more than $1x10^8 cmHz^{1/2}/W$ at 10.6μm at room temperature which is higher than the commercially available uncooled photon detectors at similar wavelength. The measured carrier lifetime is about 27nsec which is an order of magnitude longer than the bulk material due to the suppression of the Auger recombination. Optically pumped type-II lasers at 6.1μm operating at 160K as well as light e mitting diodes at 4.8μm operating at room temperature have also been demonstrated.
I this talk the latest results as well as the comparison with Type 1 interband and intersuband devices will be discussed.

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Precision Characterization of Infrared Hot-Electron Transistors at Low Temperatures

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In certain infrared applications, both the optical signal and background can be very small, in which a photodetector with extremely low dark current I_d is required. By reducing the operating temperature T of the quantum well infrared photodetectors (QWIPs), the thermal dark current can be suppressed and detectors with extremely low I_d can be achieved. In this work, we have performed precision measurements on I_d and the noise current i_n of a QWIP at T = 4.2 K with the associated 4.2 K radiation background. From these measurements, the actual detector performance in this operation regime can be assessed. In addition, we have also evaluated the utility of electron energy filtering technique realized in an infrared hot-electron transistor[1] (IHET) under these conditions.

The band structure of the QWIP and the corresponding IHET is shown in Fig. 1. The IHET has three contacts: the emitter, the base and the collector. The bias setup for detector operation is in the common base configuration, and the base is grounded. The QWIP structure is located between the emitter and the base, and a quantum barrier filter is located between the base and the collector. At 4.2 K, the thermal current is completely suppressed. The dominant dark currents in the QWIP are the direct tunneling (DT) current transported directly among the ground states of each wells and the impurity assisted tunneling (IAT) current transported via impurity sites within the QW barriers. In the presence of an infrared source, there is also a photocurrent I_p passing above the QW barriers. Under an emitter bias V_e, these three current components inject into the base at different energies E, with $E(I_p) >> E(DT) > E(IAT)$. The last inequality is true at low T because only energy emission tunneling processes are allowed, and hence only the impurity sites below the ground state energy can be accessed for IAT. The function of the filter is to block the DT and IAT current entering into the collector but allow I_p to pass through, thereby increasing the sensitivity of the detector.

Two QWIPs, labeled QWIPs A and B, and the associated IHETs A and B from the same material wafer have been measured. The detector structure consists of a 6000 Å GaAs emitter contact layer ($n = 1.2\times10^{18}$ cm^{-3}), a QWIP with 30.5 periods of 500 Å $Al_{0.25}Ga_{0.75}As$ barrier and 50 Å GaAs well (1.2×10^{18} cm^{-3}), a base with 300 Å $In_{0.15}Ga_{0.85}As$ and 200 Å GaAs (both doped to 1.0×10^{18} cm^{-3}), a 2000 Å $Al_{0.25}Ga_{0.75}As$ filter barrier, and a 1.1μm GaAs collector contact layer (1.2×10^{18} cm^{-3}). The emitter area A_e is 7.92×10^{-4} cm^2, and the collector area A_c is 2.25×10^{-4} cm^2.

The dark current and the noise current are measured with the detectors immersed in liquid helium at 4.2 K. The measurement system is composed of a cryogenic probe and a home-made low-noise electrometer. The entire measurement system has an input current noise floor of 0.80 fA/√Hz at the frequency f = 1 Hz (Fig 4). For current below 8 pA, the data are taken at femto-ampere level resolution using the electrometer with integration time of 1 second. All the current noise data are measured with the electrometer except for QWIP B, which has a much higher I_d level. QWIP B is measured with a current amplifier having a wider bandwidth and a higher noise floor of 4 fA/√Hz at 1 Hz. In this experiment, we also measured the "window current" I_w, which is the sum of the photocurrent and the dark current measured at T = 4~8K under a 300K background source with 36° field-of-view using 45° edge coupling.

The dc I-V characteristics of QWIP A and B were measured with the collector contact shorted to the ground. Fig. 2 shows that when $|V_e| < 3V$, $I_p >> I_d$, so that $I_w \approx I_p$. On the other hand, when $|V_e| > 3V$, the reverse is true, and $I_w \approx I_d$. The data also show that I_d of the two QWIPs can differ by two orders of magnitude despite the similar I_p. We attribute this difference to the difference in the IAT current in these detectors. The optimum bias for QWIP operation is about –2.5V, at which the QWIP spectral responsivity R_λ reaches a maximum, while I_d remains relatively low.

Fig. 3 shows the corresponding IHET characteristics with the collector voltage V_c = 0.1 V. We found that a small positive V_c substantially increases the collection of photocurrent in IHETs with a thick filter barrier. After current filtering, both the collector dark current and window current become much more

uniform as shown in Fig. 3, indicating that the IHET is able to block the IAT current that causes the detector nonuniformity at low temperature. The performance improved by an IHET is measured by the current transfer ratio $\alpha \equiv j_c / j_e$ where j_e and j_c are the emitter and collector current densities, respectively. For large improvement, the photocurrent transfer ratio α_p should be high, and the dark current transfer ratio α_d should be low. At $V_e = -2.5V$ and $V_c = 0.1V$, measurements show $\alpha_p = 0.79$ and $\alpha_d = 0.22$ for detector A, and $\alpha_p = 0.82$ and $\alpha_d = 0.0039$ for detector B. Therefore, an IHET structure is able to improve the QWIP performance in this temperature regime, especially when the dark current is dominated by impurities.

In order to determine the dark current limited detectivity D* at low background, we measured the dark current noise. Its spectra at $V_e = -2.5V$ are shown in Fig 4. After subtracting out the instrument noise, the current noise density i_{ne} of QWIP B clearly shows the 1/f behavior expected from a large IAT current. In the frequency range shown, $i_{ne} = 119.4f^{-0.63}$ fA/$\sqrt{Hz}$, where f is in Hz. Even for QWIP A, which has much lower dark current and a constant spectrum at the measured frequency range, i_{ne} is far from the expected shot noise i_s. If a QWIP could be considered as having N independent QW periods connected in series, i_s would be given by $(2eg_nI_e)^{1/2}$, where $g_n = 1/N$ from the circuit theory and I_e is the emitter tunneling dark current. Using the measured $I_e = 44.5$ pA and $i_{ne} = 7.5$ fA/$\sqrt{Hz}$ for QWIP A at –2.5 V, g_n is deduced to be 3.94, much larger than the expected $1/N = 0.033$. Therefore, the dark current noise of a QWIP is not shot noise in nature even if the transport is not dominated by IAT.

To further characterize the QWIP noise properties, we changed V_e to obtain different dark current levels for both QWIP A and B. The noise current i_{ne} at f=1Hz is plotted against I_e in Fig. 5 for both detectors. It turns out that if the dc current level is the same, both detectors will have the same noise level. This important result implies that the nature of the noise associated with DT and IAT is very similar. The QWIP noise power $(i_{ne})^2$ can be fitted to the sum of two components as shown in Fig. 4: (a) a constant noise which is independent of I_e or V_e, and (b) a 1/f noise which is proportional to $(I_e)^2$, similar to that of the mobility-fluctuation 1/f mechanism.[2] We did not find a linear I_e dependence for the noise power, indicating that the shot noise is negligible in these QWIPs, consistent with the estimated g_n above.

One can understand the frequency dependence of the DT current in the QWIPs with the following argument. Due to the large RC time constant τ (or equivalently the dielectric relaxation time) of the present QWIPs, the positive charges left behind in the electron direct tunneling process can take a long time to neutralize. The net charges change the entire QW potential profile so that different QWs are no longer independent from each other. The value of τ depends on the location of the QW from the cathode, which introduces a different characteristic frequency $f_c = (2\pi\tau)^{-1}$ to the charge fluctuation Δn in each QW. If the smallest f_c is less than the measuring frequency, 1/f noise will result.[2] For the present case, the smallest f_c is estimated to be 0.61 Hz at –2.5 V for QWIP A, which is just below the measurement range. Therefore, 1/f noise is observed. When I_e increases such that f_c is well beyond the measurement range, in which different QWs become independent, the noise is then determined by shot noise or g-r noise, as in high temperature or high background cases.

We can also explain the dc current dependence. For the usual generation-recombination noise, Δn is caused by the statistical fluctuation of n and is thus proportional to $\sqrt{n}$, which leads to $i_{ne} \propto \sqrt{I_e}$. In the present case, Δn is caused by the fluctuation in the tunneling process, which is directly proportional to the tunneling probability. Therefore, $i_{ne} \propto I_e$ as long as f_c is within the measurement range.[2]

Contrary to the 1/f component, the origin of the bias-independent noise component is not well understood at present. The measured value of 2fA/$\sqrt{Hz}$ is much higher than the expected Johnson noise of $(4kT/R)^{1/2} = 0.002$fA/$\sqrt{Hz}$ at 0 V. Furthermore, this noise component deviates from the typical value in a few cool-down runs, which can range from 0 to 6 fA/$\sqrt{Hz}$ for both detectors. Therefore, more studies are still needed to better understand this noise component.

The IHET structure is able to reduce the noise current passing into the collector as seen in Fig. 4. Since the emitter and the collector have different areas, quantitatively, we should examine the noise power transfer ratio γ^2 given by $\gamma^2 \equiv ((i_{nc})^2 / A_c) / ((i_{ne})^2 / A_e)$. We found that γ^2 equals 0.26 for detector A and 0.0088 for detector B. If the noise of the QWIPs were determined by shot noise, γ^2 would be equal to α_d quoted above.

With the actual noise measurements, we can then calculate D* according to $D^* = R_\lambda\sqrt{A}/i_n$. For the QWIPs, the bias-independent noise dominates at $|V_e| < 2$ V, and 1/f noise dominates at $|V_e| > 2.5V$. D_e^* turns out to be near maximum at the bias of –2.5V. At this bias and at the peak wavelength λ of 8.45 μm, R_λ is 0.62 A/W for the QWIP and 0.58 A/W for the IHET with $V_c = 0.1V$. As a result, at T = 4.2 K,

$D^*(QWIP\ A) = 2.3\times10^{12}cm\sqrt{Hz}/W$, $D^*(IHET\ A) = 4.2\times10^{12}cm\sqrt{Hz}/W$, $D^*(QWIP\ B) = 1.5\times10^{11}cm\sqrt{Hz}/W$ and $D^*(IHET\ B) = 1.5\times10^{12}cm\sqrt{Hz}/W$. The measured D^* of the IHETs is higher than the QWIPs, their ratio is approximately equal to α_p/γ from the dc photocurrent measurement. These values of D^* are significantly lower than the estimation based on the shot noise of the dark current as commonly assumed.

In conclusion, the QWIP dark current noise at low temperatures is the sum of a 1/f noise and possibly a bias-independent noise. The IHET reduces the dark current and the noise, and improves the detectivity and the uniformity. From these measurements, a QWIP with thinner QW barriers will be advantageous at low temperatures. It reduces the RC time constant and thus reduces the associated noise in the highly resistive detectors. It will also increase the speed of photoresponse under low background condition. The resulting higher dark current and higher shot noise in this QWIP can be blocked by the IHET structure, with which high sensitivity and high speed thermal imaging can be performed under these operating conditions.

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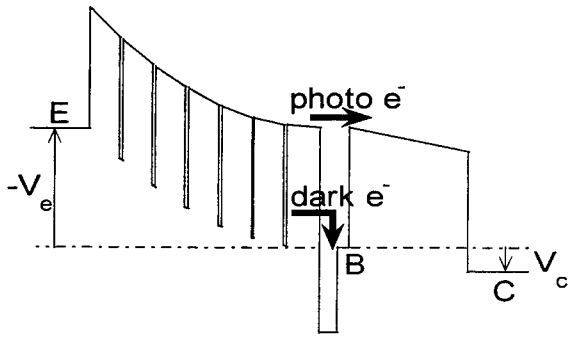


Figure 1: The IHET band structure.

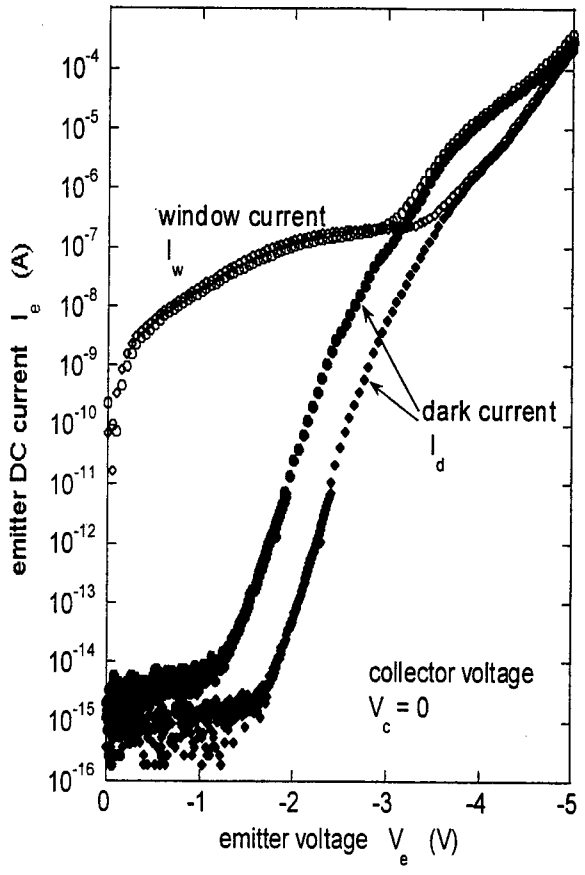


Figure 2: dc I_e-V_e characteristics of QWIP A (diamonds) and B (circles). Base and collector are both grounded.

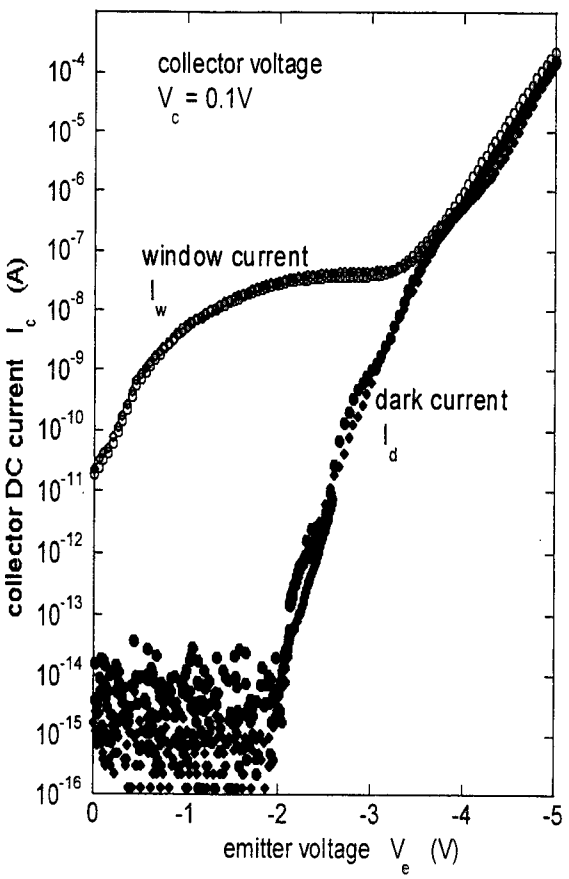


Figure 3: dc I_c-V_e of IHET A (diamonds) and B (circles) with V_c = 0.1V.

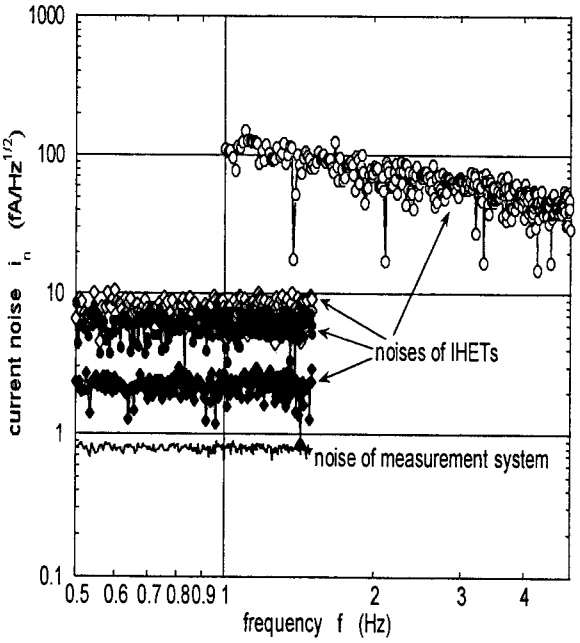


Figure 4: Dark current noise power spectrum at the collector (solid symbols) and the emitter (open symbols) for detector A (diamonds) and B (circles) with V_e = –2.5V and V_c = 0.1V. All data include the noise of the measurement system, which is 0.80 fA/√Hz (line) for all detectors except QWIP B.

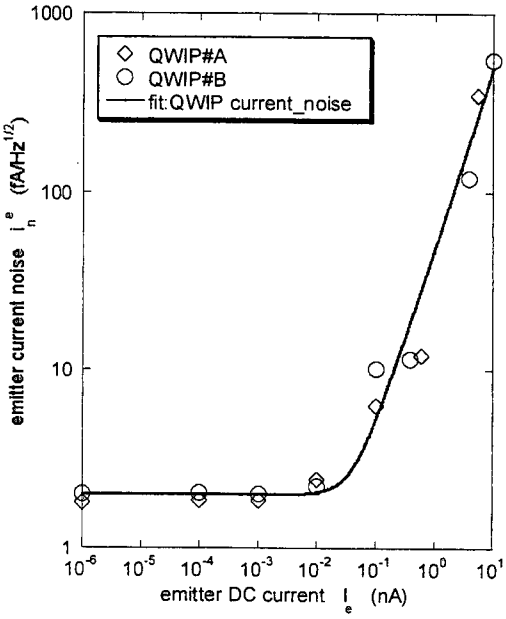


Figure 5: The dark noise current density versus the dc dark current for both QWIP A and B at f=1Hz. The QWIP current noise power spectral density i_n is fitted by $i_n = \sqrt{(2^2 + 50^2 \times I_e^2)}$, where the units for i_n and I_e are fA/√Hz and nA, respectively.

Passive-Active-Resonant Couplers (PARC): a New Platform Technology for Monolithic Integration

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1. INTRODUCTION

Several approaches for monolithically integrating devices have been reported. One of the methods is to use regrowth or selective area growth for creating a low-loss passive waveguide [1]. Besides being a complex technology, issues like non-satisfactory electrical properties at the interface between the active and passive regions and low-loss coupling etc. still have to be resolved. Another approach is to use spatially selective quantum well inter-diffusion to create sections with higher bandgap [2]. However, in this scheme, the bandgap and the waveguide properties cannot be arbitrarily varied in different sections of the device. Twin-waveguide structures using a single epitaxial growth have also been reported [3]. However, they suffer from an unacceptably large coupling loss (~5-6 dB) between the two waveguides.

At the University of Maryland, we have developed a platform technology called PARC (Passive Active Resonant Coupler) for integrating various active and passive devices [4]. PARC uses resonant coupling over a taper to transfer optical power between two vertically placed waveguides. The platform uses very short taper regions (~100 μm) with very low coupling loss (<0.2 dB). The two waveguides can be optimized separately for various functionalities required in an optical module; e.g. one waveguide can be a highly confined active waveguide (AW) optimized for high gain while the other is a well confined passive waveguide (PW) optimized for devices like splitter. The platform uses single epitaxial growth and conventional fabrication schemes. PARC also allows the possibility of placing multiple waveguides in the vertical direction. In this paper, we describe the design, fabrication and testing of some basic PARC circuits.

2. DEVICE DESIGN

The schematic of the device is shown in Fig. 1. The device consists of an AW optimized for maximum gain at 1.55 μm and a well-confined PW optimized for passive devices. The lateral confinement in the waveguides is done by etched waveguides. The device has three sections: (i) the gain section where the mode is well confined in the AW, (ii) the mode transformation section where the mode

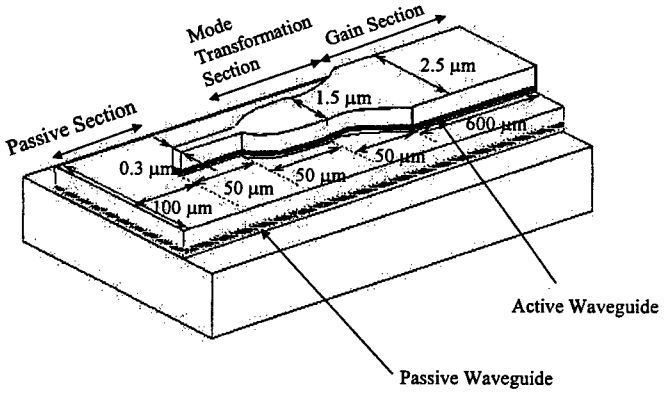


Fig. 1. Schematic of the device. Various dimensions are marked

is transformed from the AW to the PW, and (iii) the passive section. The AW consists of 4 compressively strained QWs in a separate confined heterostructure (SCH) optimized for maximum gain at 1.55 μm. The PW is a 20-layer stack of lattice-matched quaternary and InP with thickness of 0.4 μm and an effective index of 3.32. The advantage of using a stack is that any arbitrary index for the PW can be obtained by changing the relative thicknesses of the layers and is not limited by growth capabilities. A 0.8 μm thick InP cladding separates the two waveguides.

Commercial 3-D beam propagation software (BPM-CAD, Optiwave Corporation) was used to optimize the taper shape on the AW. The ridge defining the PW is 4.5 μm wide throughout the device. In the gain section of the device, the ridge on the AW is 2.5 μm wide. In this section, the AW is the dominant waveguide (propagation constant is larger in the AW than in the PW) and the light intensity is well confined in the AW. The resonant width of the AW where the propagation constant in the two waveguides is equal is 1.5 μm. The AW is tapered from the initial width of 2.5 μm to the resonant width of 1.5 μm using a 50 μm long exponential taper of third order. It is then tapered from the width of 1.5 μm to the final width of 0.3 μm using another 50 μm long inverse exponential taper of third order. The advantage of this hetero-taper shape is that it varies very slowly around the resonant width. Hence, the light gets the required coupling length to resonate into the PW. After that the taper varies quickly to lock the mode in the PW. We chose the final width of 0.3 μm because that is what we can reproducibly achieve in our fabrication process.

However, it is to be noted that the device would work efficiently even with taper tips as large as 0.6 μm. A 100 μm long passive section is added to the device. Here, the AW is completely etched off. The $1/e^2$ diameter of the active mode was 0.75 μm X 2.0 μm in the transverse and lateral directions respectively,

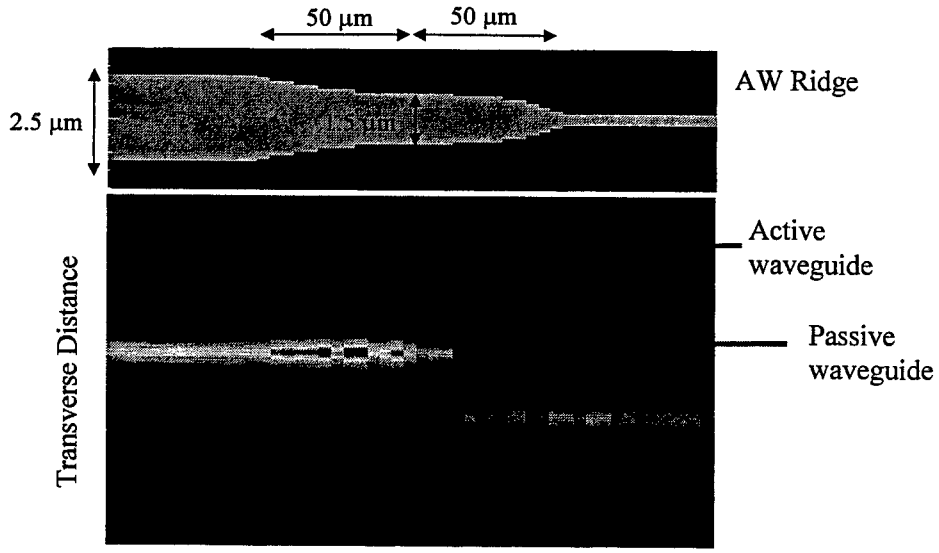


Fig. 2. Simulation of the mode transformation. The taper shape on the active waveguide is also shown.

whereas the passive mode was 1.3 μm X 3.5μm in diameter. The lateral confinement of the PW can be further increased by tapering the width of the ridge to the required value in the passive section. The taper shape and the simulation of the propagation are shown in Fig. 2. The mode conversion loss was less than 0.1 dB. We also did simulations to see the effect of growth and fabrication errors. It was found that the excess loss was less than 0.4 dB even for a very high index variation of 0.03 for the AW. The device was also found to be insensitive to the fabrication errors like etch depths etc. that we expected in our process.

3. DEVICE PROCESSING

The epitaxial layers were grown using solid source molecular beam epitaxy (MBE) on 3-inch InP substrate. The ridges were defined using a conventional photoresist (OCG-OIR 12 MK) and an optical 10x-projection aligner. By using a 10x projection aligner, the tolerances on the resolution of the masks are relaxed. The ridges on the AW were etched to 0.3 μm below the active region. This etch was done using $Ar:Ch_4:H_2$ chemistry in a parallel plate reactive ion etching (RIE) chamber. No metal or dielectric mask was used for the etching of sharp tapers. A 4.5 μm wide, 1 μm high mesa, was then dry etched using the same chemistry to create the confinement for the underlying waveguide. A spin-on-glass (SOG) process was used to create the dielectric isolation. This process is self-aligned and eliminates the critical alignment of the dielectric-opening window on top of the ridge. Thus, the whole taper region can be electrically pumped, resulting in better device performance. The samples were thinned to 100 μm, and p-side (TiPtAu) and n-side (AuNiGeNiAu) ohmic contacts deposited. The samples were then annealed at 400^0 C for 1 min. Using negative photoresist and a metal lift-off process; selective p-side metallization was carried out to obtain electrically isolated devices in an array. The devices were mounted p-side up on copper heat sinks and were tested without any coatings. 850 μm long control samples were also prepared with a uniform ridge width of 2.5 μm.

4. RESULTS AND DISCUSSION

The devices were tested at room temperature both in the pulsed and CW mode. Fig. 4 shows the typical light-current characteristics of the control sample and the mode transformed devices. The mean threshold current for the control samples was 29 mA with slope efficiency of 0.16 W/A. The mode transformed devices had a mean threshold current value of ~ 30 mA, with slope efficiency of 0.16W/A. Output power greater than 40 mW and 15 mW were obtained in pulsed and CW operation respectively. By mounting the devices p-side down, higher power can be obtained in CW operation. By comparing the L-I curves and accounting for the difference of the active gain volumes in the two samples, a round trip mode transformation loss of 0.3 dB was calculated. To observe if any residual reflections were taking place at the end of the taper, we anti-reflection (AR) coated the passive facet of the device. The L-I curve of the device with AR coated facet is also shown in Fig. 3. No lasing was observed even at a high current of 500 mA. This shows that the reflections in the taper are negligible.

The transverse and lateral far-fields were obtained from both the facets of the device using a rotating stage and a pinhole detector. The far-field plots from the passive facet are shown in Fig. 4. Theoretically calculated farfields are also plotted and show good agreement to the experimental results. This shows that the optical power is well coupled into the PW. The far-filed divergence angles (FWHM) of 47^0 X 26^0 were obtained in the transverse and lateral directions respectively.

5. PARC VARIATIONS

In the previous design, the underlying waveguide is of constant width 4.5 μm. The minimum width of the passive waveguide is determined by fabrication, as the underlying waveguide always has to be larger than the top waveguide. However, in many passive devices, the underlying waveguide may need to be narrower ~2μm. One solution is to add another section where the passive waveguide is tapered from 4.5 μm to the required width adiabatically. However, this would increase the mode transformation section length. The elegant solution is to put a taper on the passive waveguide in the resonant section itself. We have designed a device where the passive waveguide is tapered linearly from 4.5 μm to 3.5 μm over the first 50 μm and then from 3.5 μm to 2.0 μm over another 50 μm. The mode is resonantly coupled from the active waveguide to the final 2.0 μm passive waveguide with less than 0.1 dB loss. This example shows the versatility of the PARC platform in designing the active and passive waveguides.

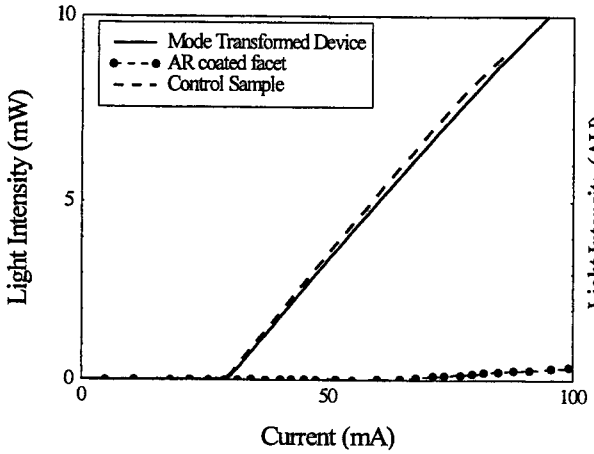


Fig. 3. L-I curve of the PARC device and the control sample

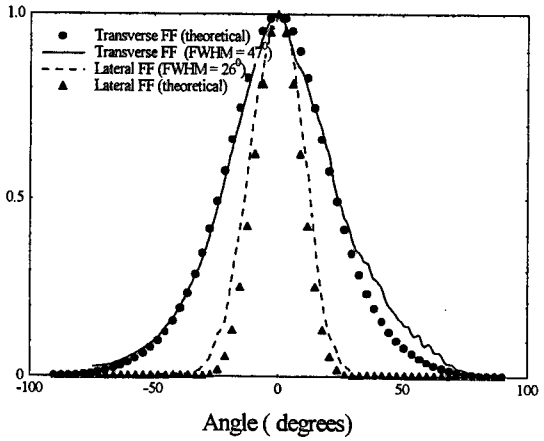


Fig. 4. Farfield profiles from the passive facet

6. CONCLUSION

In this paper, we have demonstrated an efficient platform technology called PARC for monolithic integration of optical devices. PARC allows choosing the waveguides arbitrarily and uses resonance in tapers to couple the mode over a very short region with low loss. Various active passive devices like loss-less splitters where the mode is first split in the passive waveguide and then coupled to the active waveguide for gain, can be built. NxN Optical cross connects and balanced Mach-Zehnder interferometers used for high speed optical signal processing like optical logic gates and wavelength conversion can be fabricated. As the PARC uses single epitaxial growth and conventional fabrication schemes, it appears to be a very promising technique for monolithic integration of active and passive devices.

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DEFECT-RELATED ABSORPTION OF a-SI:H FILMS FOR SOLAR CELLS

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Abstract. Optical characteristics for undoped a-Si:H films of different thicknesses and for a phosphorous doped n-type a-Si:H film have been determined using transmission and reflectance measurements over a wide range of wavelengths. Using an algorithm introduced earlier to extract the optical absorption spectrum $\alpha(E)$ over a wide energy (E) range, we have shown that it is possible to discern defect related absorption bands in the sub-gap band region. The value of sub-gap absorption is significantly higher than that estimated from indirect techniques such as photothermal deflection spectroscopy or photocurrent spectroscopy. The near-edge absorption appears to be quite different from the conventionally assumed exponential edge. With this defect related and near edge absorption subtracted, films of different thickness appear to have the same Tauc Gap of ~1.70 eV. However, the interband absorption is better described by the $(\alpha E)^{1/3}$ plot as a function of energy.

1. Introduction

Hydrogenated silicon devices are strongly affected by localized defect states in the energy gap. These states control the width of the space charge layers, the slope of thin film transistor (TFT) transfer characteristics in the subthreshold regimes, the leakage current and dynamic characteristics of TFTs, as well as the photoconductivity and the luminescence of optoelectronic devices. The efficiency of energy conversion in solar cells fabricated with a-Si:H and related materials and the stability of all hydrogenated silicon devices are also believed to be determined by the localized defect states in the energy gap. In this work we present some results from applications of the interference characterization technique [1-3] to study optical properties of a-Si:H films for solar cells, including subgap, defect related absorption.

The comparison of results obtained by different techniques is an important subject. The total subgap absorption coefficient obtained by the interference technique, which includes all transitions in the bulk and at the surface is of the order of 100-200cm $^{-1}$ in our undoped films and can be higher depending on doping and other conditions of film manufacturing. At the same time, two widely used methods give very low subgap absorption for a-Si:H. These are the Constant Photocurrent Method (CPM) [4] and Photothermal Deflection Spectroscopy (PDS) [5]. CPM can detect only a reduced number of electron transitions because of the low mobility of holes in the valence band as well as of electrons in the localized conduction bandtail- states [4]. PDS can not detect all optical transitions since it measures the thermal rise in the sample due to the recombination of photoexcited charge carriers. As a result, "PDS is sensitive to optical transitions where excited non-equilibrium carriers recombine non-radiatively, but it will not detect transitions in which the photoexcited carriers recombine radiatively" [6]. It has been demonstrated however [7] that the non-radiative quantum efficiency has a strong wavelength dependence for subgap illumination.

On the other hand, there are other methods which give much higher subgap absorption than CPM and PDS do. The total yield photoelectron spectroscopy measures only transitions from the valence band and from the filled localized states in the gap below the Fermi energy, and does not include transitions to the empty states above the Fermi level. In their review paper, K. Winer and L. Ley [8] compared total yield and PDS absorption spectra of simultaneously-prepared undoped a-Si:H. Using the usual adjusting procedure (for all methods which measure only relative spectra) around the energy 1.8 eV, one can obtain a high total yield subband absorption at the level 10^2 cm^{-1} for undoped film, although not all transitions are detected by this method. Taking all the above into account, the subgap absorption coefficient obtained by the interference technique seems reasonable.

2. Experiment

In comparison with other optical methods, interference spectroscopy has some important advantages including very high sensitivity to small variations of optical characteristics, because of

multiple reflections at the film boundaries. Both transmission, T, and reflection, R, spectra of our samples reveal deep interference fringes in the IR region. The transmission and reflection spectra are measured with a Cary 5E Spectrophotometer using a two-beam scheme with specular reflection attachments which ensure a near normal (~8 °) angle of incidence on the sample. The analysis of refractive index, $n(\lambda)$, and absorption coefficient, $\alpha(\lambda)$, spectra from the measured characteristics as a function of wave length, λ, is based on exact interference equations for the system of a film on a substrate [1]. This analysis requires precise knowledge of the film thickness and accounts not only for the interference in the a-Si:H film but also for the absorption inside the substrate and for the reflection from both substrate surfaces. At the same time, the product of refractive index and the film thickness nd can be obtained independently and very accurately from the position of R and T extrema, λ_{extr}: $nd = \frac{m\,\lambda_{extr}}{4}$, where m is an integer number starting from one and corresponding to the order of extremum, including maxima and minima. The order of extremum m is found from the wavelengths of two adjacent extrema in the spectral region where n does not change appreciably when m is increased by one.

The shift in interference pattern is used to control for the non-uniformity in thicknesses for different regions of the wafer. Normally, film thickness uniformity was sufficiently high for implementing the interference method. Similarly, positions of T and R extrema practically coincide in the range of small absorption with an accuracy of 0.1-0.5%, which is important for further analysis. Although the results of the analysis are extremely sensitive to the film uniformity, to the exact value of d, and to the consistency of both measured characteristics $T(\lambda)$ and $R(\lambda)$, the values of absorption coefficient at wavelengths corresponding to transmission maxima depend almost entirely on T and on the product nd, and as a result are determined with a very high accuracy. On the other side, experimental data at maxima of R are very sensitive to the absolute value of the film thickness and are used to obtain d with an accuracy of at least 0.5%. Small variations in d for two measurements (T and R) have to be included in the analysis to eliminate traces of the interference pattern from the absorption spectra.

Three samples of different thicknesses have been prepared at Solarex, using standard intrinsic a-Si:H conditions on a glass substrate, and one n-type sample with a doping level about 1% measured as the gas concentration of dopant in SiH_4. The rate of deposition was about 1.1 Å/s for all samples. The high quality of films is confirmed by very good thickness uniformity and by the position of the vibrational mode in the stretching region. The thickness variation for one sample has not exceeded 0.2%. The position of the vibrational mode has been determined by measurements of reflection derivative spectrum using a commercial Fourier Transform Spectrometer (Bruker IFS-66). A single absorption band is observed at 2000 cm^{-1} which is typical for standard a-Si:H films [9]. This technique has advantages in comparison with usual transmission measurements, since it can be utilized for films deposited on all substrates including those that are not transparent in the region under investigation.

3. Results and discussion

The review spectra of absorption coefficient are shown in Figure 1. Three different regions of absorption can be easily separated: 1) the subgap absorption, 2) the near edge absorption usually described as an Urbach tail, and 3) the interband absorption. Each of these regions is discussed below.

Subgap absorption

Two different types of defect related transitions are possible. Type I represents transitions from the states occupied by electrons below the Fermi energy into the conduction band or into the localized tail states, and type II - transitions from the valence band or from the localized tail states near the valence band into defect states above the Fermi energy, which are not occupied. Because of very large differences in the absolute values of subgap absorption obtained from the CPM method and from transmission measurements, we conclude that the probability of the type I transitions is very low and subgap absorption that we see is due to transitions of the second type. On the other hand, since the mobility of holes in a-Si:H is three orders less than the mobility of electrons, the

photocurrent from these transitions detected by the CPM method is very low in comparison with photocurrent from interband transitions.

The value of subgap absorption in our samples is significantly higher than that estimated from indirect techniques like PDS or CPM spectroscopy. It varies from 200 cm^{-1} to 500 cm^{-1} at the energy E =1.5 eV in undoped samples, and to 900 cm^{-1} in doped n-aSi:H (Figure 2). Fine structure in the form of small peaks and steps is also present and many fine features are reproducible. Subgap absorption starts at energies 0.85-0.9 eV in all three undoped samples. This correlates with the fact that the Fermi level in intrinsic layers is very deep - somewhat about 0.8 eV below the conduction band. The structure near this edge can be an indicator of a midgap defect band and correlates with the defect-related photoluminescence band which appears at 0.8-0.9 eV [10]. Other pronounced defect related bands peaked around 1.05-1.15 eV and 1.25 eV, which are close to energies obtained earlier in [2]. All these energies have been identified in defect related luminescence [10]. The band at 1.1 eV is believed to be related to the oxygen impurity. The transitions at 0.9 eV have been ascribed to the radiative recombination of electrons trapped in double occupied dangling bonds with holes in the valence band tail. Finally, transitions at 1.25 eV that are called band-edged, include the same valence-band tail states [10].

In n-aSi:H, absorption in the range 0.8-1 eV is reduced in comparison with intrinsic layers (Figure 2). This correlates with a possible shift in the Fermi level position upwards about 0.1-0.15 eV in the doped sample. There are several steps of subgap absorption with pronounced threshold energies at about 1.1 eV, 1.25 eV, and 1.5 eV. From these three components the last one is absent in intrinsic material and thus can be related to phosphorous induced defects. The two other steps have been observed in intrinsic layers too, although the level of absorption was much lower. It might be that more defects of this type are created in doped layers. These two defects situated in the upper half of the gap have to be filled by electrons at the doping, thus reducing the rate of the Fermi level shift and the donors' efficiency.

Near edge absorption.

Near edge absorption is usually described as an Urbach exponential tail and the width of this tail is used to evaluate the quality of material. However, for the quantitative analysis of near edge absorption, we have to take into account subgap transitions which are obviously intensive enough to effect results. As a first and a very rough estimate, we can approximate the subgap absorption for this analysis as a constant at the highest step, that most close to the near edge region. After subtracting the subgap absorption using this approach, the near edge absorption does not obey the exponential law typical for the Urbach edge, but rather follows a power law with a sharp edge and threshold energies between 1.5 eV and 1.6 eV. In a thinner sample, this absorption has the lowest threshold about 1.52 eV. It grows slowly with energy and gives significant contribution to the total absorption at high energies, above the gap. In other samples the near band absorption is much lower and does not effect significantly the results of interband absorption analysis.

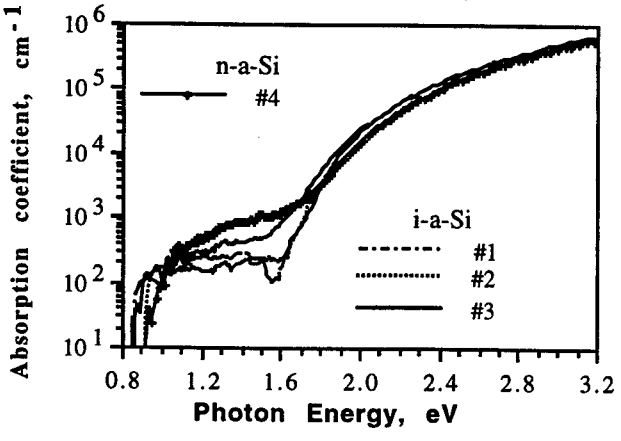


Figure 1. Absorption coefficient spectra for i-a-Si and n-a-Si.

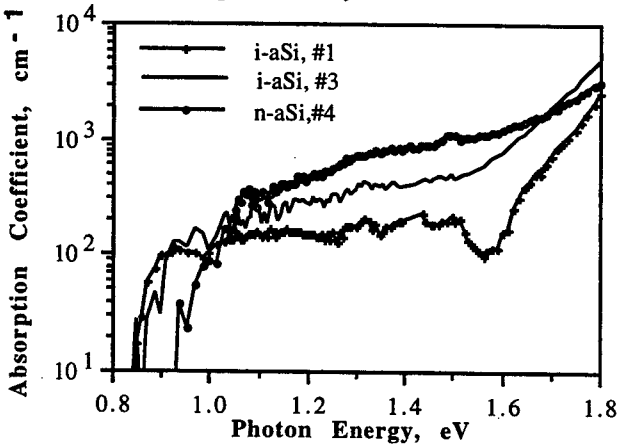


Figure 2. Subgap absorption in i-a-Si and n-a-Si.

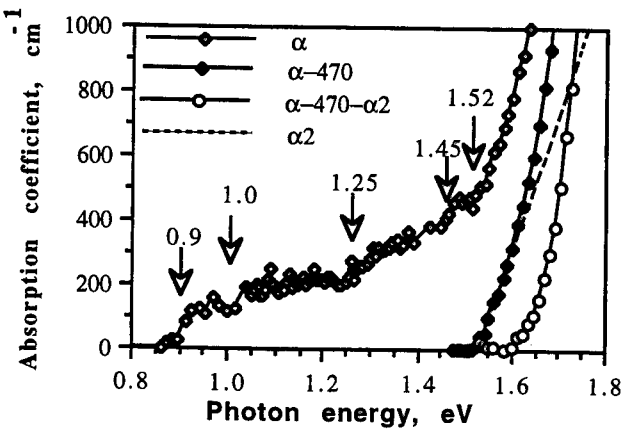


Figure 3. Sub-gap and near -edge absorption analysis in i-a-Si .#3; α2 - the near-edge absorption approximation

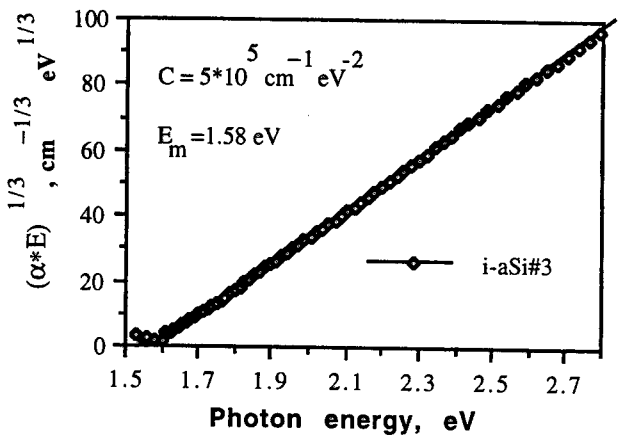


Figure 4. The $(\alpha E)^{1/3}$ plot of i-aSi after extraction of defect band and near-gap band absorption.

Interband absorption.

The Tauc dependance $\alpha(E)\,E = B\,(E-E_T)^2$ is most often used to determine the optical gap, E_T, in a-Si:H. This procedure, however, gives results which depend on the energy range since the linearity of dependence $(\alpha E)^{1/2}$ is very poor. In the energy region below 2 eV we obtained the optical gap E_T ~ 1.7 eV for all intrinsic films, and B~ 4.5×10^5 $cm^{-1}eV^{-1}$.

As was demonstrated in [11], the ambiguity of the optical gap can be reduced dramatically by using the $(\alpha E)^{1/3}$ plot as a function of E. Theoretical analysis [12] indicated that the expression in the form $\alpha(E)\,E = C\,(E-E_m)^3$, where C is a constant, can be derived if transitions involving localized states are also included with the same matrix elements as other interband transitions. The characteristic energy E_m determined from this dependence might be not the real gap in the density of states, but the mobility gap. Figure 4 shows that the $(\alpha E)^{1/3}$ plot as a function of E is almost ideally linear and gives E_m ~1.58 eV and C ~ 5×10^5 $cm^{-1}eV^{-2}$.

Acknowledgments

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EFFECT OF ENERGY TRANSPORT OF ELECTRONS THROUGH *LO* PHONON EMISSION ON SUPERLUMINESCENCE AND BLEACHING OF A THIN GaAs LAYER EXCITED BY A POWERFUL PICOSECOND LIGHT PULSE

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In certain high-speed powerful semiconductor optoelectronic devices the energy transport of charge carriers is going under somewhat peculiar conditions. It refers, in particularly, to devices being developed on the basis of GaAs where both ultrafast optical pumping and the high-intensity amplified spontaneous emission occur in picoseconds, such as a picosecond modulator of the optical transparency and photoconductivity, picosecond light wave converter, semiconductor laser with pumping by ultrashort light pulses, etc.. The above-mentioned peculiar conditions might be as follows: (1) the energy transport of electrons becomes very intensive due to intensive stimulated recombination of charge carriers; (2) the energy distribution of photogenerated electron-hole plasma (EHP) may be somewhat different from the quasi-equilibrium distribution due to this transport [1]; (3) average lifetime of photogenerated charge carriers till their recombination is within the picosecond range [2,3]. In the present work under similar conditions we have found a new effect of energy transport of photogenerated electrons on bleaching (i.e., an increase of transparency) and superluminescence (i.e., amplified spontaneous emission in a medium without an optical cavity) of a thin (~ 1 μm) GaAs layer, excited by a powerful 14 ps light pulse. This is true for the intensive energy transport that occurs during the exciting pulse and decays in ~10 ps after the pulse and which is being stimulated by superluminescence. As follows from the revealed effect, even when the EHP concentration is $>10^{18}$ cm^{-3}, this energy transport of electrons is caused in part by the electron-LO phonon interaction. On one hand, it is distinct from the case of continuos photogeneration where the electron transitions through LO phonon emission escape detection at EHP concentration $>10^{17}$ cm^{-3} due to the screening of electron-LO phonon interaction and to a high probability of the electron leaving the initial state as a result of interaction of the electron with EHP. On the other hand, both Raman light scattering with LO phonon emission [4] and phonon (LO) oscillations, induced by superluminescence, in energy distribution of electrons (and, consequently, in the spectrum of the reversible bleaching) [5,6], were also observed only in picoseconds (in picosecond time scale) at concentrations $>10^{18}$ cm^{-3} of EHP, photogenerated in GaAs by ultrashort pulse. So, experimental results obtained in the present work and in [4-6] allow us to suppose that the screening of electron-LO phonon interaction is attenuated during the energy electron transport, which occurs by generation of dense EHP in GaAs by the ultrashort light pulse and which is being stimulated by superluminescence recombination. The attenuation of the screening is probably connected with the above conditions (1) - (3). Presumably, as a result of the supposed attenuation of the screening, the LO phonon emission processes measurably contribute to the energy transport of electrons, even at the EHP concentration $>10^{18}$ cm^{-3}, causing changes of bleaching and superluminescence in picoseconds as described below.

The experiments were carried out at room temperature. Both the superluminescence and bleaching of GaAs layer arise by photogeneration of dense hot EHP by a 14 ps light pulse and decay with a characteristic time ~ 10 ps after pulse. The superluminescence and bleaching have been studied as functions of the pulse photon energy $\hbar\omega_{ex}$ with the fixed value of the pulse energy density averaged over the light beam cross section. An antireflection coating was deposited on the sample to exclude the exciting light interference. The time-integrated spectra of superluminescence (investigated, e.g., in [7])

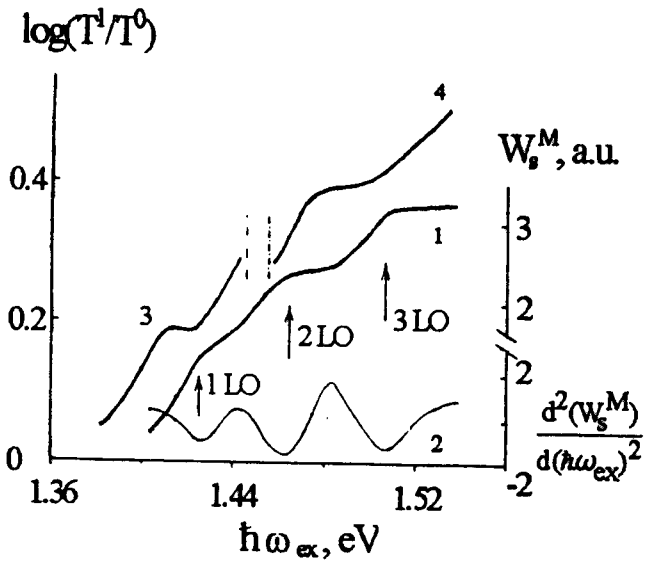


Fig.1. Curve 1: the energy W_s^M at the maximum of the superluminescence spectrum as a function of the exciting pulse photon energy $\hbar\omega_{ex}$ (the exciting beam diameter F = 0.5 mm). The positions of the maximum local enhancement of superluminescence are indicated by the arrows.

Curve 2: $d^2(W_s^M)/d(\hbar\omega_{ex})^2$ as a function of $\hbar\omega_{ex}$, used to determine the positions of the maximum local enhancement in curve 1.

Curves 3 and 4: optical bleaching of GaAs versus $\hbar\omega_{ex}$. Probe pulse photon energy $\hbar\omega_p$ = 1.557 eV. (3) – the probe pulse time delay relative to the exciting pulse τ_d = 6 ps, F = 0.56 mm; (4) - τ_d = 0, F = 0.5 mm.

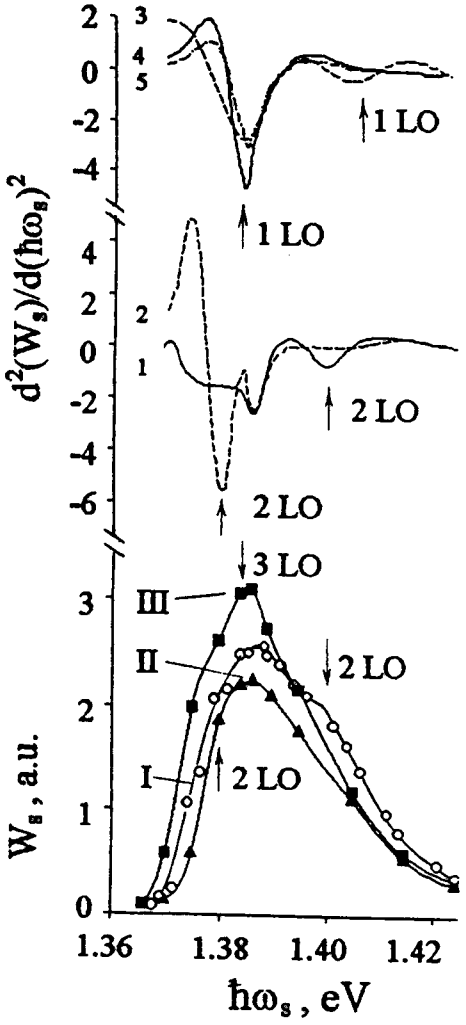


Fig.2. Superluminescence spectra of GaAs (curves I-III) measured for F = 0.5 mm: (I) $\hbar\omega_{ex}$=1.481 eV; (II) 1.46 eV; (III) 1.504 eV. Curves 1-5 are plots of $d^2(W_s)/d(\hbar\omega_s)^2 = f(\hbar\omega_s)$ obtained by differentiating the superluminescence spectra measured at: (1) $\hbar\omega_{ex}$ = 1.481 eV; (2) 1.46 eV; (3) 1.449 eV; (4) 1.423 eV; (5) 1.415 eV. The positions (indicated by arrows) of the predominant enhancement over the superluminescence spectrum, due to the transport of electrons through LO phonon emission, are determined from the positions of the minima of $d^2(W_s)/d(\hbar\omega_s)^2$ as a function of $\hbar\omega_s$. The number of LO phonons, emitted by this transport of one electron, is pointed adjacent to the arrows here and in the other Figures.

were measured in the same way as in [5]. The intensity of superluminescence emission was estimated to be as high as ~10^8 W/cm^2. The bleaching, measured by "excite-probe" method, was described by the ratio $\log(T^1/T^0)$, where T is the transparency, and the indices 1 and 0 denote the presence and absence of excitation, respectively. As $\hbar\omega_{ex}$ is increased, when the spacing between the individual energy levels (further called resonance levels) at which electrons are generated and the levels from which they undergo stimulated recombination is a multiple of the longitudinal optical (LO) phonon energy $\hbar\Omega$, the following phenomena are revealed.

Recombination superluminescence is enhanced so that stepwise local prominences were observed in $W_s^M(\hbar\omega_{ex})$ curve (Fig.1), here W_s^M is the energy at the maximum of the superluminescence spectrum. The enhancement is somewhat nonuniform over the spectrum of superluminescence (Fig.2), hence the dependence of the spectrum width

(FWHM) on $\hbar\omega_{ex}$ becomes modulated with the period of $\Delta = \hbar\Omega\,(1+m_e/m_h)$ (Fig.3), where m_e and m_h are the masses of the electron and the heavy hole, respectively. The shift of the superluminescence spectrum edge $\hbar\omega_s^e$ toward longer wavelengths is increased, when the electrons are generated on resonance levels, so that $\hbar\omega_s^e(\hbar\omega_{ex})$ curve also becomes period-Δ modulated (Fig.4). Local features also appear in the dependence of the bleaching on $\hbar\omega_{ex}$ (Fig.1). A comparison with $W_s^M(\hbar\omega_{ex})$ curve reveals that when the increase of superluminescence with increasing $\hbar\omega_{ex}$ slows down, the bleaching begins to increase faster; and when the superluminescence begins to increase faster, the bleaching increases slower.

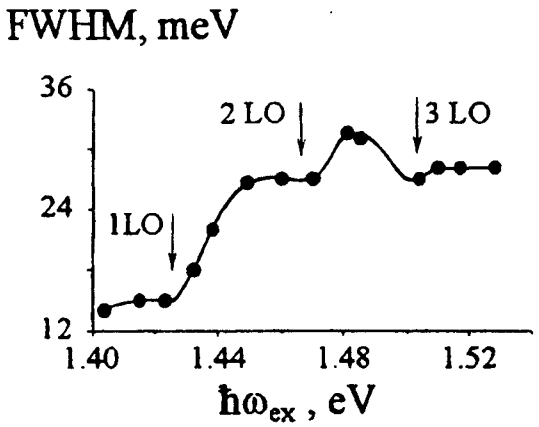


Fig.3. The superluminescence spectrum width (FWHM) versus $\hbar\omega_{ex}$ for F=0.5 mm.

All these phenomena are qualitatively explained as follows. The fraction of transitions, involving emission of LO phonons, in the energy transport of electrons toward the bottom of the conduction band increases, when electrons are generated at the resonance levels. The corresponding changes of the EHP heating and the density of nonequilibrium LO phonons appear due to enhancement of emission of LO phonons. Below we discuss this in more details.

Besides the above-supposed attenuation of the screening of electron-LO phonon interaction, the superluminescence stimulated transport of electrons by the emission of LO phonons has to increase due to the following reason. When the electron, photogenerated on a resonance level, emits a LO phonon, it transfers to energy levels with depleted carrier population, corresponding to a minimum of phonon oscillations in energy distribution of electrons [5,6]. Presumably, this process also leads to an increase in the density of nonequilibrium LO phonons. An increase in the LO phonon density has the effect of narrowing the band gap E_g by virtue of the electron-phonon interaction [8]. This assumption is consistent with the observed period-Δ stepwise shift of the long-wavelength edge of the superluminescence spectrum toward longer wavelengths with increasing $\hbar\omega_{ex}$ (Fig.4).

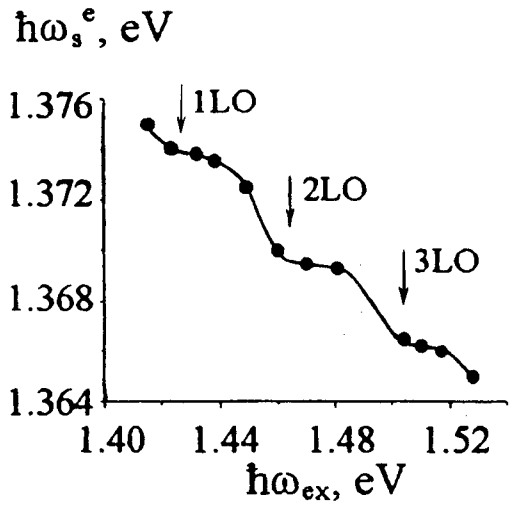


Fig.4. Position of the long-wavelength edge $\hbar\omega_s^e$ of the superluminescence spectrum versus $\hbar\omega_{ex}$ for F = 0.5 mm ($\hbar\omega_s^e$ is the photon energy at which the radiation energy at the long-wavelength edge of the superluminescence spectrum is equal to 0.12).

The enhancement of superluminescence by recombination of electrons transported to the bottom of the conduction band through the emission of LO phonons is manifested both in dependence $W_s^M(\hbar\omega_{ex})$ (Fig.1) and in the period-Δ oscillations of the width of the superluminescence spectrum (FWHM) as a function of $\hbar\omega_{ex}$ (Fig.3). The oscillations of FWHM can be attributed to the fact that if such a superluminescence enhancement (for a fixed $\hbar\omega_{ex}$) is distributed nonuniformly over its spectrum and is predominant, for example, on a side

slope of the spectrum (curve I in Fig.2), the result is a certain broadening of the spectrum relative to the case when the enhancement takes place predominantly in the vicinity of the spectrum peak (curve III in Fig.2). So, the observed features of the superluminescence spectrum (Fig. 2, 3) are consistent with the hypothesis that the enhancement of superluminescence is distributed nonuniformly over its spectrum, and that the region of predominant enhancement shifts along the superluminescence spectrum as $\hbar\omega_{ex}$ is varied.

The density ($n = p$) of the EHP increases or decreases according to whether the temperature T_c of the EHP increases or decreases because the density of EHP is controlled by recombination superluminescence and approximately satisfies (neglecting deviations from quasi-equilibrium energy distribution of EHP, *etc.*) the condition $\mu_e(n,T_c)$-$\mu_h(p,T_c) = E_g$ [2,9], where μ_e and μ_h are the Fermi quasi-levels of electrons and holes, respectively. In the presence of superluminescence, variations of the bleaching are more affected by variations of the EHP density than of EHP temperature [9]. The transfer of energy from the EHP to the lattice by the emission of LO phonons is intensified when electrons are generated at a resonance level. Accordingly, heating of the EHP with increasing $\hbar\omega_{ex}$ and the concomitant (heating-controlled) increase of both the EHP density and bleaching slow down. The corresponding variation of the bleaching with increasing $\hbar\omega_{ex}$ was observed during the exciting pulse at a fixed probe-beam photon energy $\hbar\omega_p > \hbar\omega_{ex}$ (see Fig.1).

On the whole, the experimental results obtained here and in [5,6] indicate that LO phonon emission processes can contribute significantly to the energy transport of electrons, photogenerated by ultrashort pulse in GaAs, even though the EHP concentration is $> 10^{18}$ cm^{-3}. This is true for the intensive transport which is stimulated by intensive superluminescence and which occurs during ~10 ps. According to the experimental results and their interpretation here and in [5,6,10], participation of the LO phonon emission processes in the energy transport can have a certain influence on the superluminescence, the bleaching, the heating of the dense EHP, the energy distribution of electrons, the density of nonequilibrium LO phonons, and on the variation of the width of the band gap. This influence increases when electrons are photogenerated at resonance levels defined above.

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SUB 0.1 MICRON E-BEAM LITHOGRAPHY FOR NANOSTRUCTURE DEVELOPMENT

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Current developmental trends in science and technology call for the resolution of features whose critical dimensions are below 0.1 micron. This is well below the most up-to-date SIA roadmap goals of 0.13 micron technology by 2001. Beam technologies (electron and ion beams, for example) have demonstrated ultra-high resolution. E-beam technology, for example, has produced practical resolution of arbitrary features as low as 0.01microns. As a volume manufacturing technique, in which each lithography tool must produce in excess of 60 completed 300mm silicon wafers per hour, serial beam technique are of limited utility.

For advanced scientific inquiry or for long range development, e-beam approaches have traditionally been used. Ion beams have the advantage of lack of forward scattering, and an ability to expose resists with low ion doses. Despite this, ion beam approaches have not been the major resource for advanced high-resolution development. They require higher voltages to steer beams and barrier layers to prevent ion penetration into active device regions. These issues make it impractical to execute physically large integrated structures and they lead to reliability issues both in the beam-tool and in the finished product.

However, electron beam scattering processes prevent precise localization of deposited energy. This leads to an apparent "blurring" of the beam-written image. This blurring is known as "proximity effect." To see this better, imagine the surface partitioned into squares known as "pixels." An electron beam is shot into each box for some amount of time. The center-to-center spacing of the boxes is called the 'address structure" of the lithography tool. Ideally, the beam should fill the box and no energy would spill out of the box. Unfortunately, the beam energy is dispersed over a distance as great as 10 microns (or more, depending on beam accelerating potential and substrate material). So the individual pixel exposures "interfere" with one another.

There are a number of ways to deal with this problem. There are physical techniques, in which low energy secondary electrons, released from the substrate as a result of interaction with the primary beam, are "filtered" by use of a low-atomic weight absorber.

There are "dose equalization" schemes, such as GHOST, in which the normally unexposed field of the surface is written with a low-dose, beam broadened background which makes the exposure doses in the field and in the exposed patterns "flat." This enhances contrast and minimizes feature size departures from target. Individual shapes can also be re-sized to account for under- or over-exposures as a result of proximity effect. The most "accurate" of all approaches is dose modulation. Here, the pixel-to-pixel dose is varied in such a way as to compensate for proximity effect. We focus on dose modulation in this paper.

In dose modulation, we recognize that the final dose in any pixel is given as a convolution integral:

$$\int d_I(\tau)M(x-\tau)d\tau = d_a(x) \qquad (1)$$

Where d_I is the incident dose at the pixel site, d_a is the actual total absorbed dose and M is an interaction term that specifies the strength of the coupling between pixels. This may in turn be expressed, numerically, as a matrix-vector product:

$$M \cdot \vec{d}_I = \vec{d}_a \qquad (2)$$

where M is a matrix representation of the convolution kernel.

It would seem that all one had to do was specify some desired absorbed dose pattern and invert eq. 2 to obtain the desired dose pattern. There are two problems with this. First, there may not be enough pixels to obtain the desired resolution (i.e., the matrix equation 2 is under-ranged). But more often, the problem is that eq. 2 requires negative doses to be satisfied. This is physically impossible.

Rather than solve eq. 2 directly, it is possible to re-cast the problem as one of calculus of variation. To do this, we bring d_a to the left, take a magnitude and minimize the by varying d_I. We express this mathematically as:

$$\delta\left\| M \cdot \vec{d}_I - \vec{d}_a \right\| = 0 \qquad (3)$$

Where the δ stands for variation and the vertical lines mean "take the norm of..." The expression whose magnitude we're taking is referred to in optimization theory as the cost function. As such, we are minimizing a "cost" of a given operation.

The resulting approach still has the problem of negative dose requests. We can remedy this by adding a term to the cost function which will become very large as any of the doses becomes negative. As the logarithm of any number approaches negative infinity as the number approaches negative values, we choose the following cost function:

$$\delta\left\|M\cdot\vec{d}_I-\vec{d}_a-\lambda S\left(\vec{d}_a\right)\right\|=0 \tag{4}$$

where:

$$S(d_a)=\sum_{\substack{all\\pixels}} d_a\ln(d_a) \tag{4a}$$

The problem is now a subset of the so-called simplex problem of optimization:

Minimize: $\vec{c}^{\,T}\cdot\vec{d}_a$

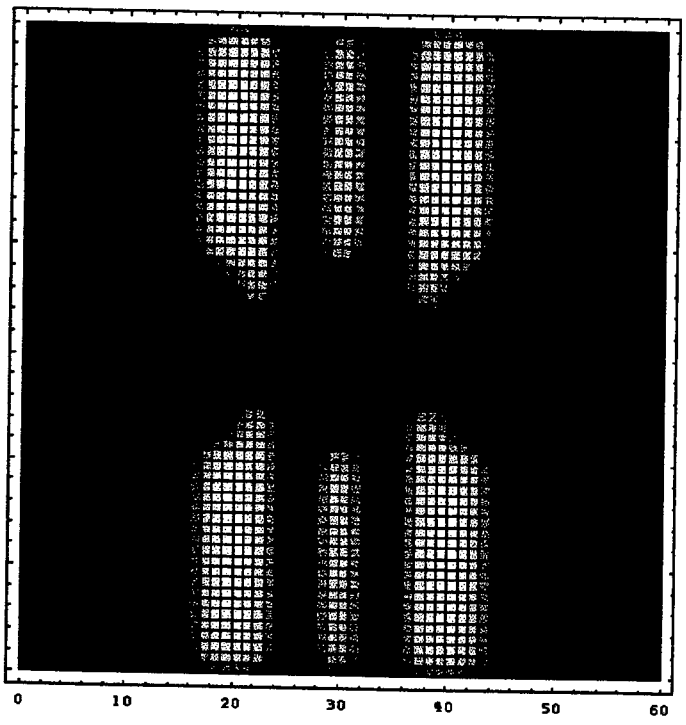
Subject to constraints: $M\cdot\vec{d}_I^{\,\prime}=\vec{d}_a$

$\vec{d}_I\geq 0$

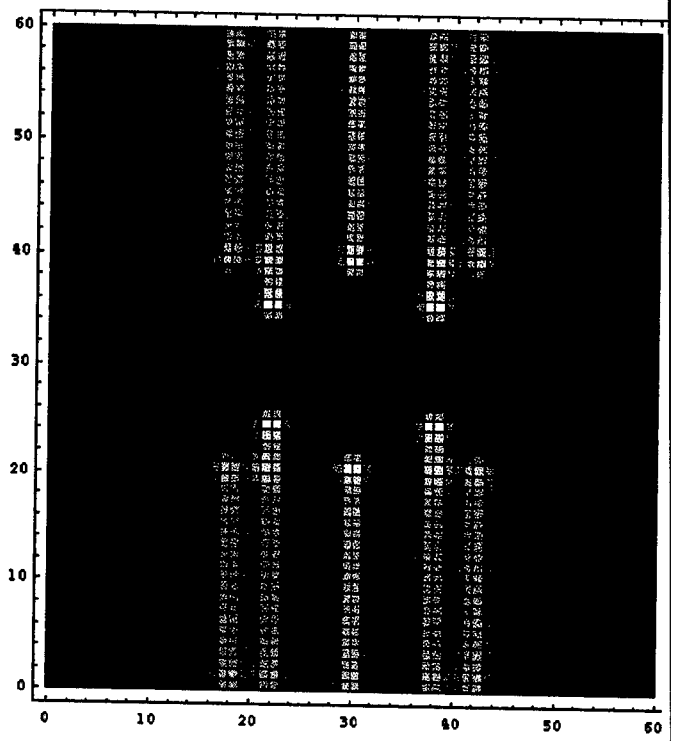
Much work has been done to solve this problem efficiently and a considerable body of literature has sprung up around it. The approach outlined here is one of the "barrier potential" approaches which have emerged over the last five years. One of the major advantages of this approach over other simplex approaches is that it can be solved by iteration. We can terminate the iteration when the cost function moves into acceptable bounds.

As the main parts of the computation are matrix-vector multiplication, and since experience has shown that two or three iterations make significant improvement in image quality, the complexity of the problem need not be much more than second order. We have studied the use of the barrier algorithm on a number of quantum effect mask features. It appears possible to accomplish 10nm features using a 6nm diameter (Gaussian) beam, such as one produced in a typical JBX-2d Jeol "nanowriter". An example of the output of the algorithm as a applied to a Coulomb blockade structure with 20nm gaps, compared to a similar structure fabricated using simple dose scaling is shown below:

Note the lack of feature edge rounding and the well defined spaces between lines thus obtained.



scaled



corrected and scaled

Nano-lithography by SPM-induced oxidation: role of space charge in the kinetics of oxide growth

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Introduction

Scanning Probe Microscopy (SPM) has recently demonstrated a strong potential in the field of nano-lithography. In particular, SPM-induced nano-oxidation has been successfully used for patterning tunnel junctions [1] and field-effect devices [2] on thin metallic or SOI films, respectively. The strong activity developed around this lithography technique takes advantage of the simplicity to reach nanometer range and to visualize the corresponding patterns with the same equipment. Several contributions have reported on the mechanism and kinetics of SPM-based oxidation in order to get a better control and more detailed insight of this patterning method. However, none of them gives a complete and satisfactory explanation for the wide range of experimental data proposed in the literature [3]-[6]. This paper proposes an enhanced oxidation model for SPM nano-lithography that reproduces the power-of-time law reported for tip-induced anodic oxidation [6]. It is based on a formulation similar to that proposed in [7] but adapted to the case of anodic oxidation. It is shown that the space-charge resulting from nonstoichiometric states strongly limits the oxidation rate. For the first time, the direct relationship between the oxide thickness and time is provided by integration of the oxide rate equation. Measurements on SPM-induced oxides generated on a titanium surface are compared to theory. The predominant role of the space charge is corroborated by electrical measurements on oxide barriers that exhibit current fluctuations due to Coulombic effects.

Experiments

A 80 nm thick oxide layer was first thermally grown on a silicon substrate and covered by a thin Ti film obtained by evaporation (4-10 nm). The oxide patterns are formed by exposing the Ti surface to a strong electric field generated by an electrically conductive AFM tip (anodic oxidation). Under normal ambient conditions (room temperature and 30-70% humidity), the oxidizing agents (typ. O^-, OH^-) drift across the existing oxide layer under the influence of the electric field developed between the surface and the biased SPM tip [8]. The most important parameters that influence the oxide growth are the anodization voltage, the tip velocity and the setpoint that controls the tip/surface interaction. In the present case, experiments have been conducted with an Atomic Force Microscope (AFM) in tapping mode (TM). TM-AFM holds the distinct advantage to decouple the exposure mechanism (electric field) from the tip/sample control when compared to another SPM tool such as Scanning Tunneling Microscopy (STM). Tapping mode is also preferred over contact mode (CM) AFM to avoid strong mechanical interactions (e.g. indentation, adhesion forces) between the tip and the surface to oxidize. Using this approach, 10 nm resolution can be routinely obtained with a satisfying reproducibility as shown in Fig. 1. Fig. 2 reports the sensivity of the height of oxide lines as a function of the anodisation voltage. The oxide height exhibits a quasi-linear dependence on the anodiation bias. It is worth noting that oxidation rate is very slow when the applied voltage is below a threshold that depends on the tip speed. This observation is consistent with the voltage-dependent threshold time τ_{th} necessary to form a detectable oxide bump [9]. A low tip velocity allows for a longer exposition to the electric field which in turn determines a shorter threshold time for oxidation. Fig.3 is a typical cross-section of the resulting topography after oxidation when the substrate voltage is varied. When the writing speed is increased, i.e. the exposure time is decreased, a fast decay of the oxide height is generally observed [8]. In order to explain this effect, experiments have been conducted by keeping the tip stationnary above the titanium surface while varying the duration of voltage pulses applied to the tip. Fig. 4 corresponds to a series of AFM images of oxide dots fabricated at a voltage of 10 V for different pulse length. Fig. 5 shows that the corresponding data follow a power-of-time law of the type $h \propto (t/t_0)^\gamma$ (here γ=1/5) as systematically observed in other reports [6][10].

Space-charge limited anodic oxidation

So far, SPM-based oxidation has been poorly described by a simple drift model [3] adapted from the Mott-Cabrera theory [11] or by empirical equations issued from thermal oxidation of thin Si films [12][13]. On the other hand, Ley et al. [6] have shown that a two-parameters empirical relation of the form $h \propto (t/t_0)^\gamma$ gave a remarkable fit to a wide spectrum of data including the experimental results of other groups. In order to explain this functional dependence, we have first to recognize that the low activation energy found for SPM anodisation (~0.4 eV [3]) is representative of plasma oxidation. Dagata et al. [4] also outlined the role of a rapid build-up of space-charge within the field-induced oxide during the initial stage of growth. For plasma oxidation, Beck et al. [14] attributes the presence of these charges to the initial high rate of oxidation that prevents a complete saturation of broken bonds at the bulk/oxide interface resulting in nonstoichiometic states. As outlined by Wolters and Zegers-van Duynhoven [7], the variation of this space charge in the oxide is governed

by a trapping-detrapping mechanism. For large charge densities (e.g. > 10^{12} cm^{-2}), Coulomb interactions between trapped charges and newly incorporated charges must be taken into account to calculate the trapping rate. On this basis, the integration of the trapping rate equation yields:

$$N = \frac{1}{s} \cdot \ln\left(1 + \frac{sN_0\sigma}{q} \cdot \int_0^t J \cdot dt\right) = \frac{1}{s} \cdot \ln\left(1 + \frac{Q}{Q_0}\right)$$

where s is the surface occupied by a trap. N is the areal density of traps and N_0 is the maximum areal density of trap sites, σ is the effective trap capture cross-section and $Q_0 = q/sN_0\sigma$. Q is the integrated areal density of charge obtained from the incoming flux of oxyanions. It corresponds to the charge brought by oxyanions that have crossed the oxyde layer at time t and can be simply calculated from C_{ox} the concentration of oxygen in the oxide, $Q = zqC_{ox}h$ where h is the oxide thickness, q the electronic charge and z the number of electronic charge per ion. Considering that the trapped charges density N is a consequence of the total oxyanion charge (e.g. OH^-) transported to the oxide/bulk interface, the space charge comes from nonstoichiometric states and is of opposite sign. This charge N induces a distortion of the electric field that significantly influences the transport of oxydizing agents in the oxide layer. The initial electric field between the bulk/oxide interface and the positive charge density N is decreased by the following amount:

$$\xi_{bias} \rightarrow \xi_{bias} - \frac{qN}{\varepsilon} \cdot \frac{h - h_0}{h} = \xi_{bias} - \frac{q}{s\varepsilon} \cdot \frac{h - h_0}{h} \cdot \ln\left(1 + \frac{zqC_{ox}h}{Q_0}\right)$$

where ε is the oxide dielectric constant and $\xi_{bias} = -(U_{tip} - U_{bulk})/h = U_{bias}/h$ is the external field imposed by the tip and substrate voltages. The potential and electric field distribution are depicted in Fig. 6. It is assumed hereafter that the flux of oxyanions through the oxide layer is totally controlled by the region where the electric field is decreased by the presence of the space charge. The ionic transport equation that describes oxide growth rate is given by:

$$\frac{dh}{dt} = u_0 \cdot \exp\left(-\frac{W}{kT}\right) \cdot \exp\left\{\frac{h_a}{h} - \delta \ln\left(1 + \frac{h}{h_b}\right)\right\}$$

where u_0 is a constant velocity, W is the energy barrier that an ion has to overcome to move to the next interstitial sites located at a distance 2a. δ is a dimensionless parameter equal to $q^2a/kTs\varepsilon$, $h_b = Q_0/zqC_{ox} = 1/sN_0\sigma zC_{ox}$ and $h_a = zqaU_{bias}/kT$. The series development and integration of the last equation leads to the desired functional form $h = h_b \cdot (t/t_0)^{1/(\delta+1)}$ where t_0 is a voltage-dependent time constant equal to:

$$t_0 = \frac{h_b \cdot \exp\left(-\frac{h_a}{h}\right)}{(\delta + 1) \cdot u_0 \exp\left(-\frac{w}{kT}\right)} = \frac{h_b \cdot \exp\left(-\frac{zqa}{kT} \cdot \frac{U_{bias}}{h}\right)}{(\delta + 1) \cdot u_0 \exp\left(-\frac{w}{kT}\right)}.$$

This last parameter t_0 explains a voltage-dependent threshold time τ_{th} necessary to observe oxide growth as experimentally observed in [9]. Double oxide barriers have been fabricated on a thin Ti film (Fig. 7). The corresponding electrical characterisation reveals large current fluctuations with time (Fig. 8), similar to those observed in random telegraph signal (RTS). The RTS, characterized by discrete change of current, is also governed by a trapping/detrapping process associated to individual defects. As outlined by Schulz [15], a trap center may be viewed as an extremely small capacitance that make possible the existence of large Coulomb barriers that induce charge quantization.

Conclusion

In summary, the incorporation of a space charge submitted to Coulomb repulsion leads to a power-of-time law for oxide grown by SPM anodization. The above derivation is consistent with experimental observations made on silicon [6][8] and titanium (this work). On the other hand, the electrical characterization of oxide barriers on Ti confirms the important role of the space charge due to individual nonstoichiometric defects submitted to strong Coulomb interactions.

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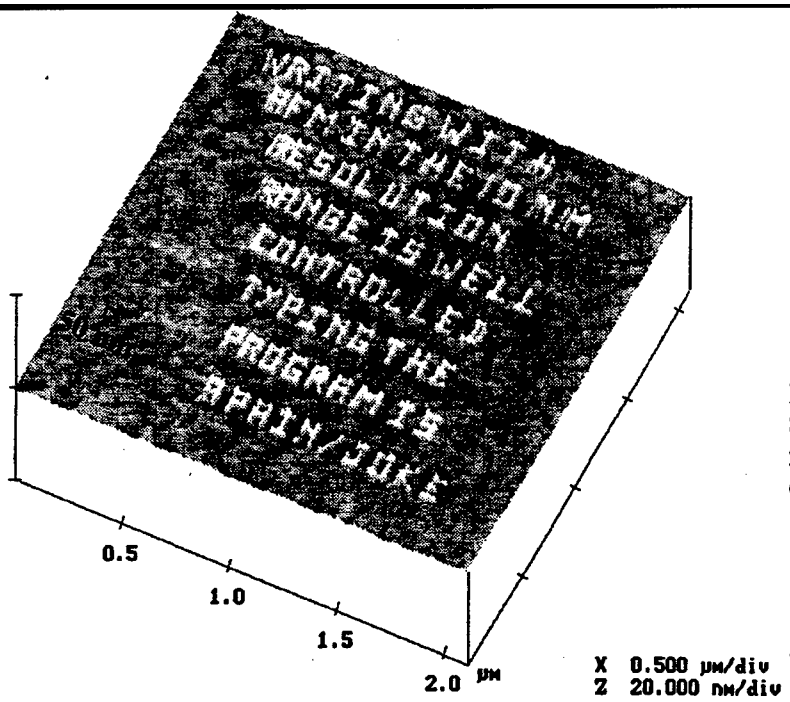


Fig 1:Typical patterns generated by AFM induced oxidation in tapping mode that exemplify reproducibility. The width of each letter is 50 nm while the resolution of each line is ~10 nm.
82 characters, ~50 µm line length and ~1200 elementary instructions

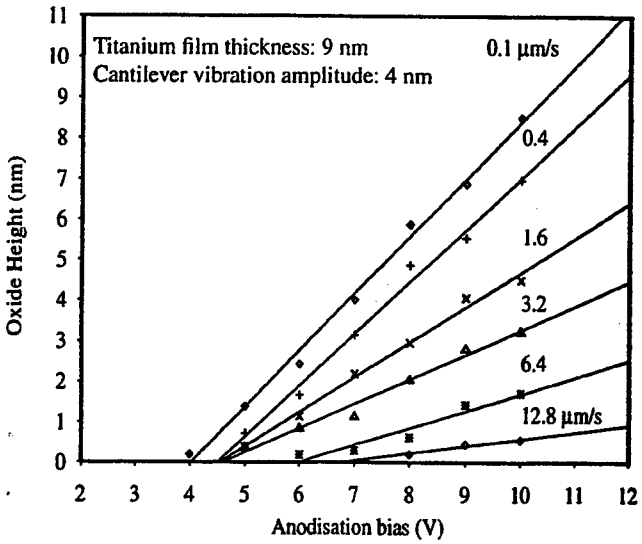


Fig. 2: Sensivity of the oxide height to the anodisation voltage for different tip speeds

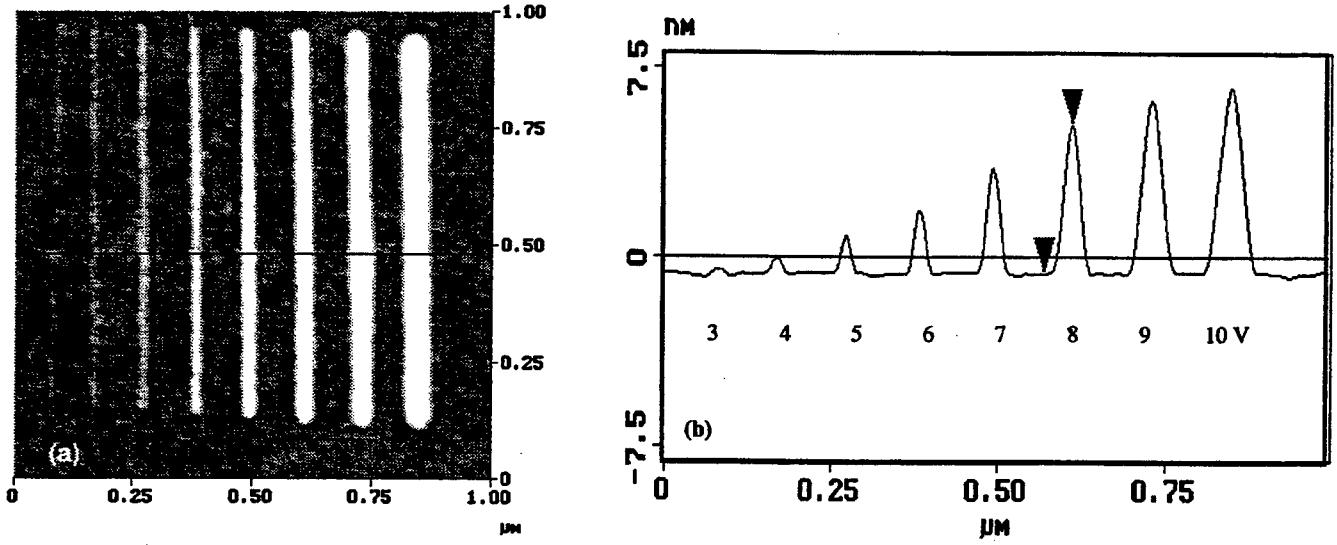
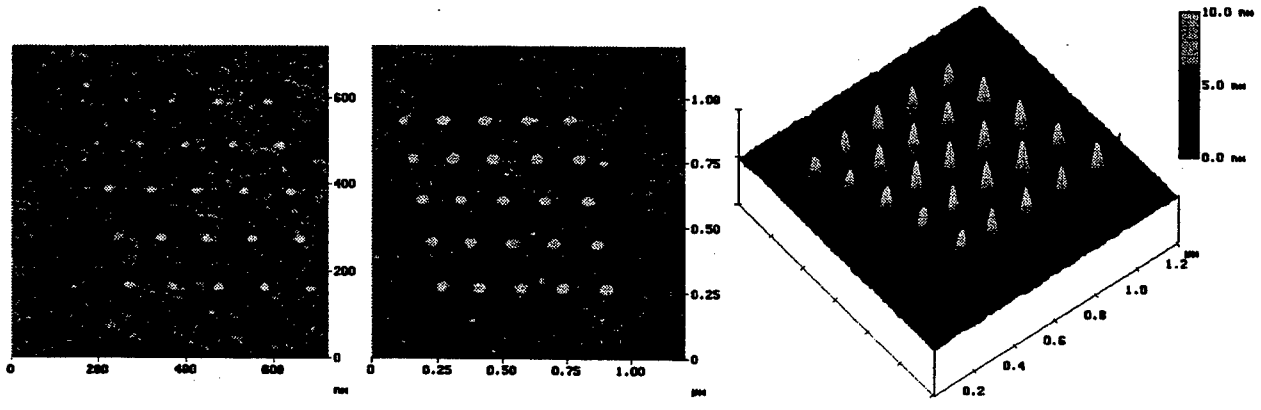


Fig. 3: Sensivity of the oxide height to the anodisation voltage
a) TM-AFM image b) anodic oxide profile along cross-section defined in a)
(tip velocity 0.1 µm/s, cantilever amplitude of vibration 4 nm)



t=0.01 s t=0.1 s t=10 s

Fig. 4: AFM images of arrays of oxide 25 dots obtained by anodization induced by the tip of an AFM in tapping mode.
The amplitude of the voltage pulse is 10 V and its duration varies from 10 ms to 10 s.
Oscillation amplitude of the cantilever is 8 nm at a frequency around 330 kHz.

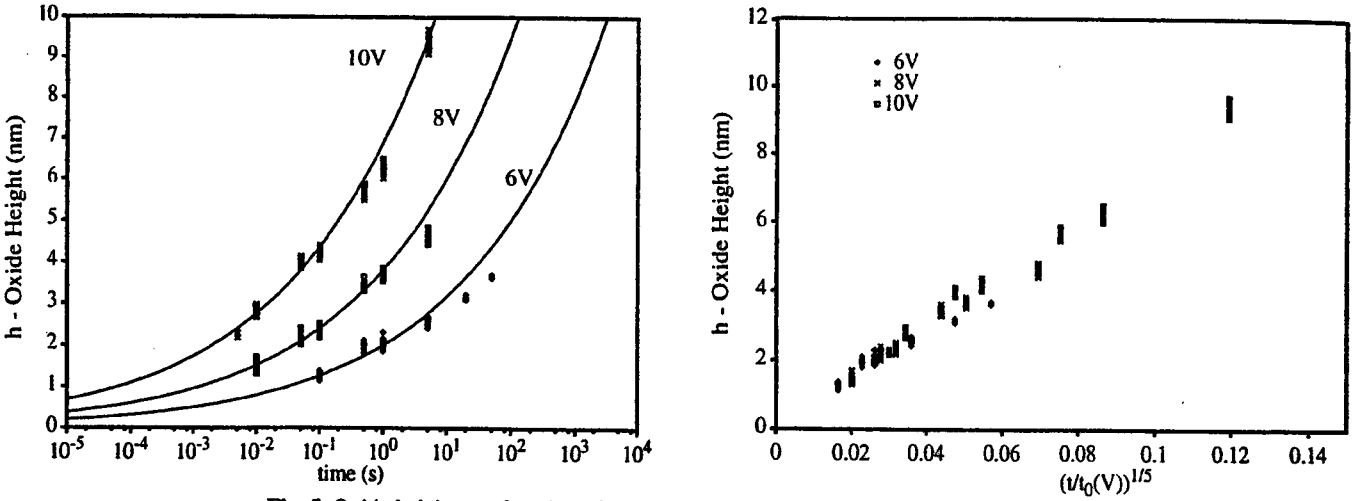


Fig. 5: Oxide height as a function of time for three different anodization voltages (6, 8, 10V).
(a) Measurements follow the power-of-time law of the type $h \propto (t/t_0)^{\gamma}$ with γ=1/5.
(b) Oxide height versus $(t/t_0(V))^{1/5}$ perfectly align for all anodisation voltages.

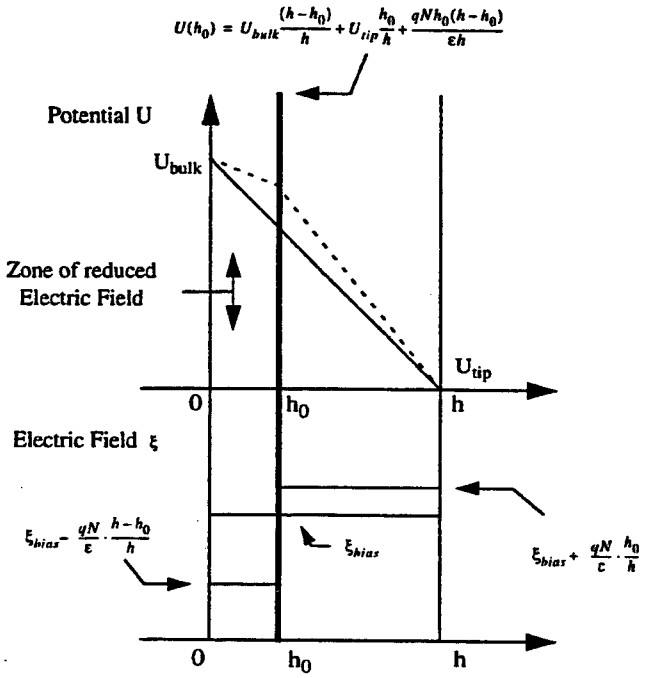


Fig. 6: Potential and electric field distorsion induced by the presence of an areal charge density located at h_0

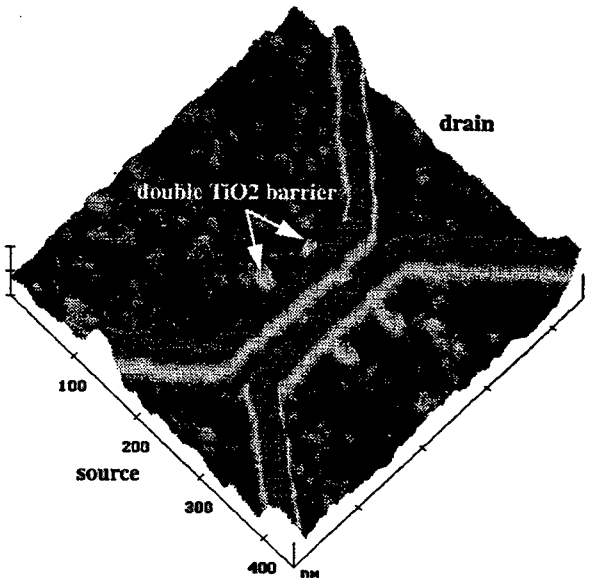


Fig. 7: Direct formation of a double oxide barrier on a thin Ti film (4 nm)

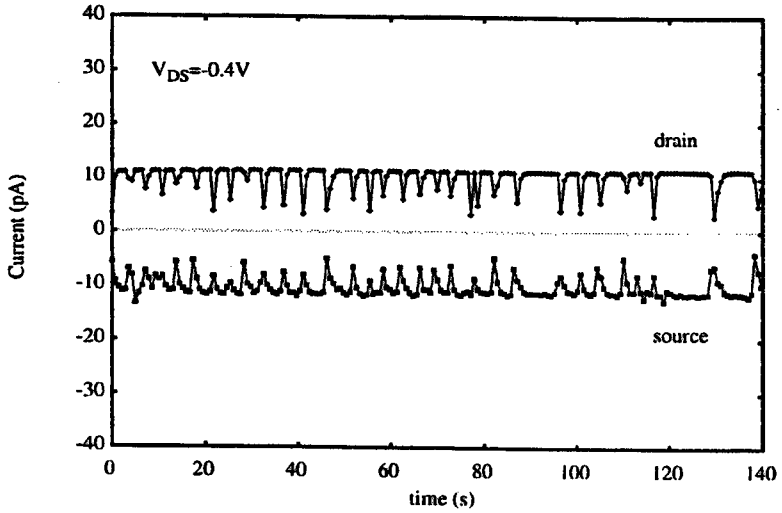


Fig. 8: Current fluctuations with time at a fixed source/drain voltage V_{DS}=-0.4V. Fluctuations are related to a trapping/detrapping mechanism via individual non-stoichiometric traps.

Microcontact Printing (μCP) of Electronic Materials Utilizing Focused Ion Beam Fabricated Printheads

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1. Introduction

The focused ion beam (FIB) is now an indispensable tool in both nanoscale characterization and fabrication of electronic materials and devices. Applications range from transmission electron microscope (TEM) sample preparation to the fabrication of diffusion cooled hot-electron bolometers.[1-2] Recently, we have used the FIB to generate "printheads" that are used to pattern Ag-coated substrates with deep sub-micron features (minimum feature sizes ~ 230 nm). Transfer of the patterns contained on the printheads is accomplished through microcontact printing (μCP).

Microcontact printing (μCP) has been developed by G. Whitesides' research group at Harvard University as a novel, non-photolithographic technique for printing micron-scale and sub-micron scale features and devices.[3-6] It utilizes self-assembling monolayers (SAMs) as an "ink," and polydimethylsiloxane (PDMS) as a "stamp." Patterns are cast as molds into PDMS from "masters" (such as traditional photolithography masks, e-beam masks, and now FIB patterned printheads). The PDMS replicas of the original patterns are then coated with SAMs (2 mM hexadecanethiol in ethanol for our experiments) and dried. The PDMS is brought into conformal contact with an Ag-coated single crystal Si substrate and the SAMs transfer from the PDMS to the Ag film. Then the Ag film is etched; it will etch only in regions not patterned by the SAMs. In essence, the SAMs act as an etch barrier. Thus, the patterns from the original master are reproduced on the target substrate. (Materials other than Ag have been patterned, such as Au, Cu, etc., but thus far, Ag is the most reliable.)

The main advantages of μCP as a "soft" lithographic technique are low cost, ease of reproducibility, and application to both planar and curved surfaces. Conventional lithographic techniques are limited generally to planar surfaces because of small depth of focus; we have been able to print deep sub-micron features both planar and curved substrates (radius of curvature 3-5 cm).

We have developed a new avenue in both μCP and FIB fields by fabricating "masters" for μCP in the FIB. A main advantage is the rapid prototyping of printhead "master" patterns in the FIB, enabling a much quicker turnaround time from concept to printing. In addition, use of the FIB allows for printhead fabrication on both planar and curved surfaces, which cannot be done by conventional lithography. This paper discusses our recent developments in FIB fabrication of masters and applications of μCP.

2. FIB Pattern Fabrication

Printheads are fabricated in the FIB (FEI Series 200, Ga^+ liquid metal ion source, minimum spot size ~10 nm) on single crystal Si (100) wafers in sections of approx. 1/8

mm^2 area. These areas are added together to produce larger overall patterned areas (currently up to ~2 mm^2 area). See Figure 1 for an example FIB printhead master. Patterns were milled into the Si at 2700pA and 1000pA beam currents (120 nm and 80 nm spot sizes, respectively), with times ranging from 20 min to 1.5 hours per pattern. Lateral feature sizes varied from micron scale to deep sub-micron scale (~80 nm minimum feature sizes). Vertical feature heights ranged from approximately 200 nm to greater than 1 μm. Atomic Force Microscope (AFM) data (Digital Instruments Nanoscope III) from the FIB-patterned surface shows an example of the pattern trench dimensions. (Figure 2.)

Features milled in the FIB exhibit a trapezoidal geometry, with the base of the feature smaller than the top, due to the Gaussian profile of the ion beam. This is an ideal situation for casting PDMS stamps, as the PDMS replicas will incorporate this geometry from the trench patterns in the FIB master. This serves to both reduce feature dimension on the PDMS stamps, and improve stability of the PDMS features when combined with careful control of aspect ratios. This is to prevent very thin or high aspect ratio PDMS features from crushing during μCP. (Figure 3.)

3. Microcontact Printing (μCP)

μCP is performed by coating the PDMS stamp with a 2 millimolar SAMs solution in ethanol. Conformal contact between the inked PDMS and the Ag film surface is allowed for approximately 5 seconds. Ag films used in this experiment were 150 nm thick. The SAMs-patterned Ag film is then etched for ~15-20 seconds during which an overall pattern area of approximately 1 mm^2 area will become visible to the eye. The sample is then removed from the etch solution, rinsed and dried. The patterned areas are those protected by the SAMs, and are evident in the Ag features left behind on the Si substrate. AFM measurements of the features have shown successful μCP of deep sub-micron line widths down to 230 nm. (Figure 4.)

4. Summary

μCP has been performed successfully on both planar and curved substrates utilizing patterns of lines and dots fabricated in the FIB. Printed feature line widths range from micron scale down to 230 nm. Pattern areas are additive up to at least a few mm^2. FIB fabrication of printhead masters is advantageous because it enables rapid prototyping of specimens for testing μCP. Initial concept patterns can be taken from fabrication through printing in less than a day. This offers promise as an alternative to traditional lithography for patterning planar and curved surfaces. A main advantage of utilizing the FIB in this manner is that it enables rapid prototyping of printhead patterns in the μCP process, with the ability to pattern and print deep sub-micron features. In addition, the large depth of focus of the FIB allows for printhead patterning on both planar and curved substrates.

Acknowledgements

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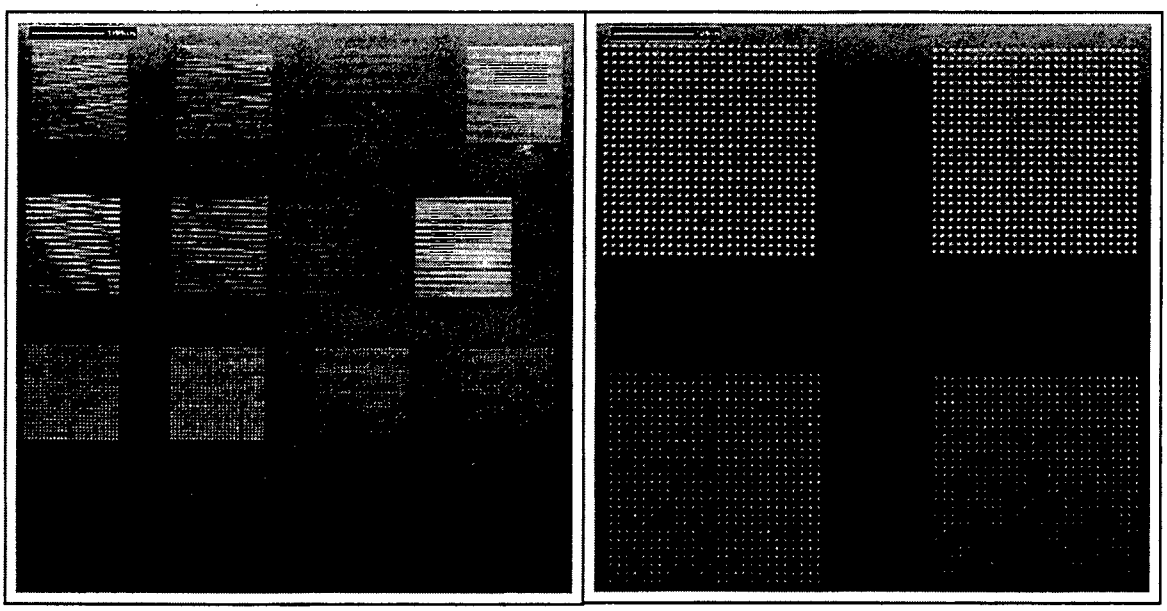
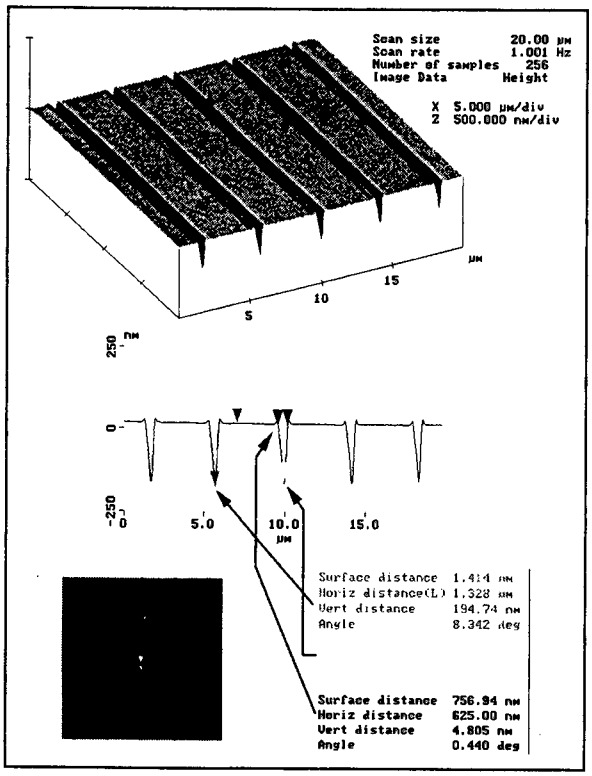
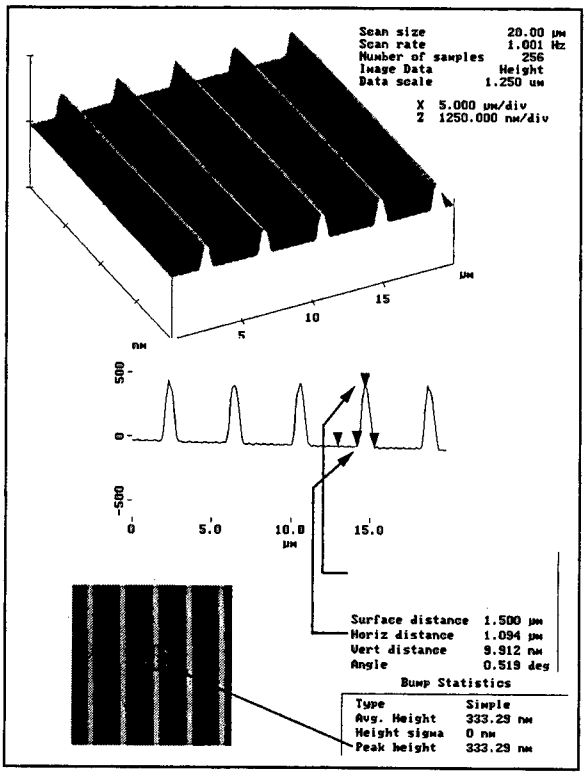


Figure 1a: FIB micrograph showing 15 patterns out of a 37 pattern printhead. Milled at 1000pA and 2700pA beam currents. Line patterns in top half, dot patterns in bottom half.

Figure 1b: FIB micrograph showing magnified view of lower left dot patterns in Fig. 1a. Each pattern is 26 x 26 dots.





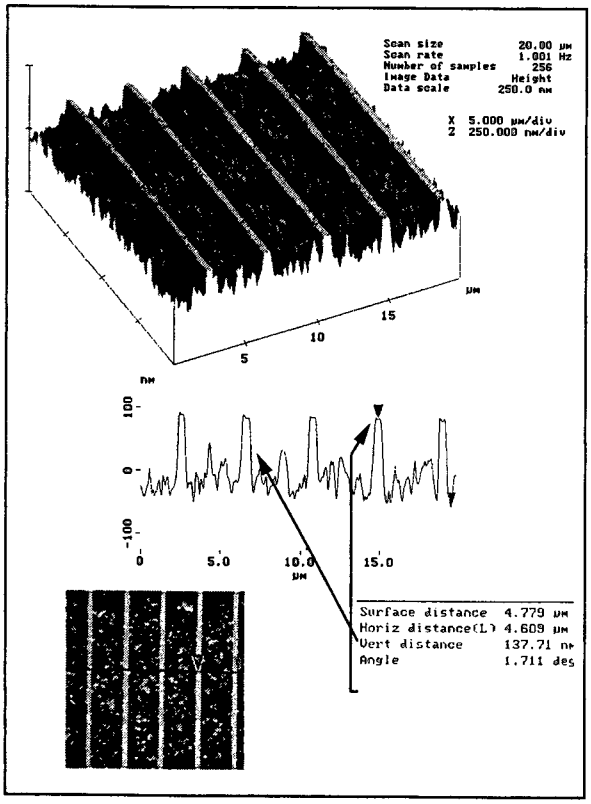


Figure 2: (upper left) AFM data showing 3D profile and feature dimensions for part of one pattern of the FIB-fabricated printhead surface (Si (100) wafer). Scan area 20 μm^2, line depth ~200 nm, width ~78 nm at the trench bottom.

Figure 3: (upper right) AFM data showing same for PDMS stamp cast from the pattern represented in Fig. 2. Scan area 20 μm^2, line height ~333 nm, width ~156 nm at apex. (Line height discrepancy with Fig. 2 trench depth is due to casting effects, as well as the difficulty in accurately measuring a sharp-featured elastomer in the AFM.)

Figure 4: (lower left) AFM data showing same for the µCP surface of Ag film on Si (100) wafer. This is the printed substrate from the PDMS stamp of Fig. 3. Scan area 20 μm^2, line width ~230 nm. Line height is ~138 nm, with an upper limit being the thickness of the Ag film (150 nm). Slightly longer etching times would remove the remaining ridges between lines.

Focused-Ion Beam (FIB) Fabrication of Diffusion-Cooled Hot-Electron Bolometers (HEBs)

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I. Introduction

Radio astronomy and atmospheric sensing missions planned for the near future will require highly sensitive heterodyne receivers in the submillimeter wavelengths. Superconducting hot-electron bolometers (HEBs), first introduced in 1990, have recently become the technology of choice for use in such receivers at frequencies near and above 1 THz. At the University of Virginia, we have recently developed a very flexible and highly robust method of HEB fabrication utilizing a focused-ion beam (FIB). This FIB technique is simpler than competing fabrication methods using electron-beam lithography, and should be well-suited to the fabrication of arrays of devices on silicon nitride membranes to which it will eventually be applied.

II. Background

A diffusion-cooled HEB consists of a thin (10 nm) bridge of superconducting niobium which contacts thicker pads of a normal metal at either end. Electrons within the device absorb incident power, share it with the electron gas, and diffuse out of the microbridge, as shown in Figure 1. The speed with which this outdiffusion occurs determines the useful bandwidth of the device.

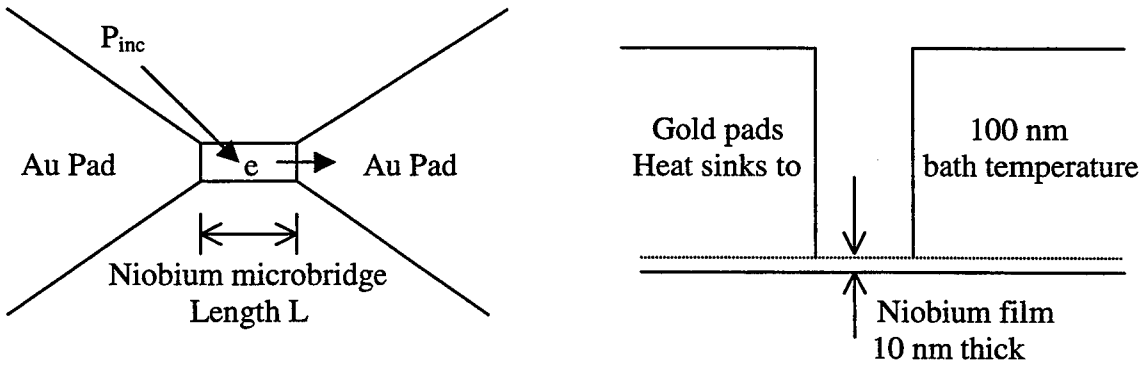


Figure 1. Schematic top and side views of a diffusion-cooled HEB. The top view illustrates the mechanism of heat diffusion which cools the device.

In order for diffusion cooling of hot electrons to dominate phonon cooling (which must occur in a wide-bandwidth niobium device), it is necessary that the length of the microbridge be 0.3 μm or less. Shorter lengths allow for faster cooling and increased bandwidth, so that intermediate frequency (IF) bandwidths as great as several GHz have been reported. [1] This is sufficient for the needs of current spectroscopic applications.

III. Fabrication

The HEB fabrication process which we have developed begins with a quartz substrate upon which are deposited layers of niobium and gold with another layer of niobium on top (Figure 2). The top layer serves as an etch mask for gold in a subsequent step. A unique feature of this process is that the metal films are all deposited under a single vacuum, producing the cleanest film interfaces possible. Conventional lithography and a one-step chlorine-based dry etch process are used on this three-layer film to pattern the filter circuits in which the bolometers will be embedded.

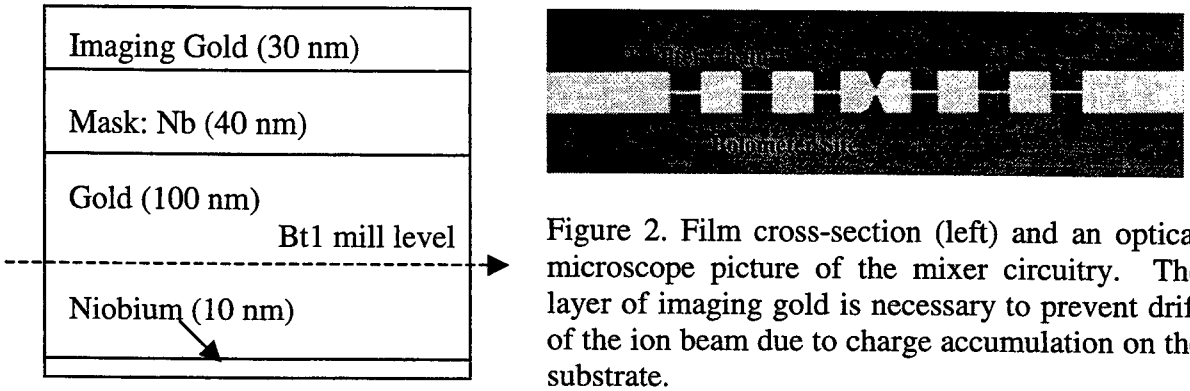


Figure 2. Film cross-section (left) and an optical microscope picture of the mixer circuitry. The layer of imaging gold is necessary to prevent drift of the ion beam due to charge accumulation on the substrate.

The bolometer microbridge is fabricated from the film already deposited on the quartz wafer using the focused-ion beam to cut away unwanted material. The FEI, Inc., Series 200 FIB Workstation [2] available to us at the University of Virginia operates much as a scanning electron microscope does, imaging secondary electrons ejected from a sample bombarded with gallium ions. These ions, however, are much more massive than electrons, so that the focused-ion beam sputters material from the sample at its point of contact. In this system, the ion beam is controlled by CAD software, allowing the ion flux to be used as a vertical mill with nanometer-scale resolution. The ability to create user-defined patterns and to control such parameters as dwell time, overlap, beam current and milling time make the FIB a versatile tool for submicron fabrication.

The FIB pattern used in this work looks like a bowtie, with the microbridge positioned at the knot of the tie (Figure 3a). In fact, two overlapping patterns (called bt1 and bt2) are used in sequence. The bt2 pattern mills all of the pixels in the bt1 pattern except for those covering the microbridge. The patterns are milled sequentially, with the net effect of milling the bowtie (excluding the knot) down to substrate while removing material from the microbridge down only to the "Bt1 mill level" noted in Figure 2. A subsequent low-power argon sputter etch removes the remaining gold from atop the 10 nm thick layer of microbridge niobium without harming this underlying layer. The masking layer of niobium protects the adjacent gold contacts and mixer circuitry during this etch. A completed diffusion-cooled HEB is pictured in Figure 3b.

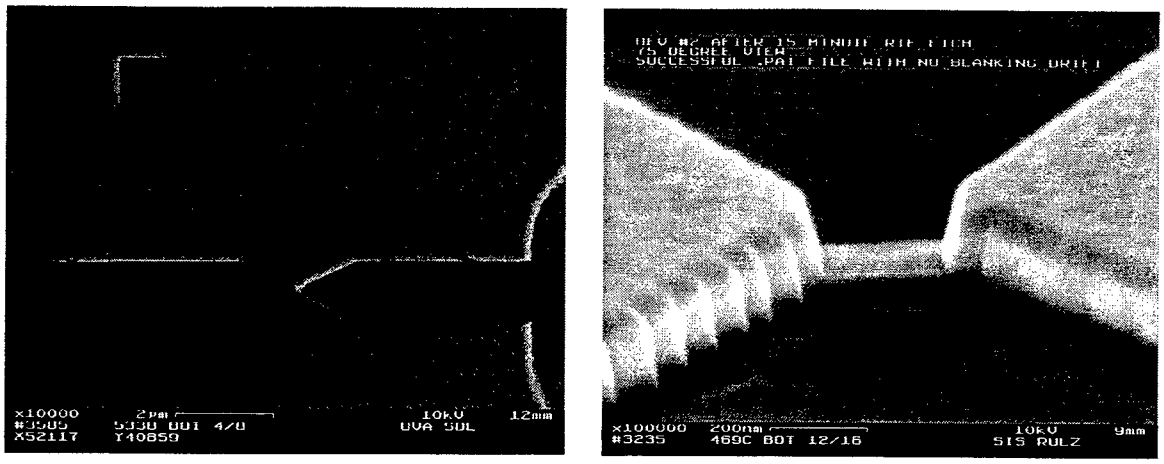


Figure 3. A bowtie milled by the FIB (a, left) and a photograph of a completed diffusion-cooled HEB (b, right).

IV. Results and Concerns

Four microbridges fabricated identically on the same wafer exhibited nearly identical room temperature sheet resistances of 23-25 Ω, in reasonable agreement with expectation. This is a promising result in view of the application of this technique to the fabrication of arrays of devices. Unfortunately, possibly due to a decline in the stability of the FIB ion source with age, this degree of uniformity has not been present in more recent work. We have recently adapted our process to deal with this problem.

Source instability causes the FIB beam current to drift substantially, which in turn causes the milling rate to vary during even a single FIB session. Since we initially milled all of our devices for set amounts of time (19 passes with the bt1 pattern followed by 12 passes with the bt2 pattern, for example), this fluctuation in milling rate adversely affected the uniformity of devices fabricated using this method.

It is therefore preferable to mill, not for a set amount of time, but until a certain endpoint is reached. This is accomplished using the secondary-ion mass spectroscopy (SIMS) equipment attached to the FIB workstation. A thin layer of chrome co-sputtered with the gold layer (Figure 4) can be detected with SIMS in real time and used as an end-point signal. Preliminary results using this new technique are promising.

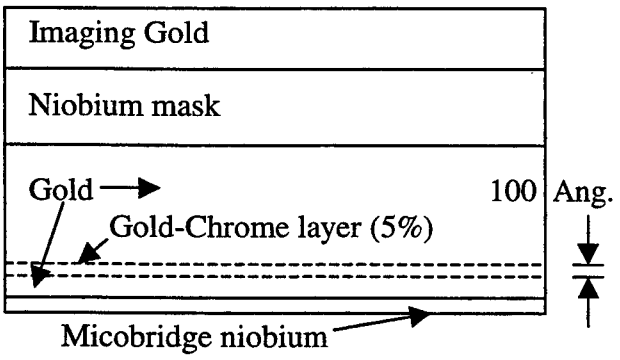


Figure 4. Film cross-section for the work involving a chrome marker layer for SIMS endpoint detection. The bt1 mill level can be brought down to the marker layer using a SIMS signature obtained in real time during the milling session without concern for the fluctuating mill rate.

It is also possible that the films we have deposited recently are not optimal for this work. Some evidence for this interpretation may be seen in Figure 5, where large voids are seen to form in the gold layer during FIB milling. Additionally, there is some concern that the thin microbridge niobium layer may be highly tensile, and that the microbridge therefore may not respond robustly to the argon sputter-etch. Investigation of these issues is ongoing.



Figure 5. SEM view of a bt1 bowtie pattern milled into the gold layer. The formation of voids such as those seen here is a concern for two reasons. Firstly, a void which develops on the microbridge site will destroy the device. Secondly, when a void exposes the underlying marker layer, the SIMS signal which results prompts the operator to cease the mill before the appropriate depth has been reached.

V. Conclusion

We have demonstrated a fast, easily variable method of HEB fabrication suitable for the creation of arrays of these devices. This technique is immediately applicable to the fabrication of aluminum-based diffusion-cooled HEBs (in which there is significant interest) and to the shrinking of niobium nitride phonon-cooled HEBs, which work we have recently undertaken at UVa. Beam current instability and film quality appear to be the two issues of pressing concern to us, but earlier results indicate that this can be a highly uniform, repeatable fabrication technique with high yield.

VI. References

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On the Optimization of HALOs for 0.1 μm MOSFETs and below

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Abstract

This paper investigates the relationship among halo parameters best suited to achieve SCE control in MOSFETs with channel lengths of $\simeq 0.1$ μm. New insights on the halo control upon threshold voltage are achieved through a simple analytical model. The analysis has been refined through extensive drift diffusion simulations based on a parametric representation of the halo profile.

Introduction

It is generally accepted that halo (p-pocket) or super-halo type devices represent good candidates for 0.1 μm MOSFETs and below [1, 2, 3], thanks to the reduced sensitivity to channel length variations and to a better control over short channel effects (SCE). Optimization of this MOSFET architecture, however, is still a difficult task because of: 1) the unclear understanding of what the optimum halo profile should be [4]; 2) the limited knowledge on the relationship between halo process parameters (dose, energy, implantation angle, etc...) and the resulting doping profile. In this framework, we exploit two different modeling approaches to gain a deeper insight in the effect of halos on threshold voltage and short channel effect control in deep sub-micron technologies.

Quasi two-dimensional model.

To gain a first understanding of halo design constraints and to restrict the range of suitable halo parameters we implemented a simple model based on the quasi-two dimensional approach proposed in [5] to integrate Poisson's equation in conventional MOSFETs. Following [6] the doping is approximated with a piece-wise constant profile (Fig. 1). The threshold voltage (V_T) is defined as the gate voltage such that $\phi_{s,min} = 2\Phi_{FC}$, where $\phi_{s,min}$ is the minimum surface potential and Φ_{FC} is the substrate Fermi potential. In each region (left pocket - LP, right pocket - RP, and channel - C) $\phi_s(x)$ is expressed as:

$$\phi_s(x) = (\phi_{R,i} - \phi_{s,i})\frac{\sinh((x - x_{L,i})/\lambda_i)}{\sinh(L_i/\lambda_i)} + (\phi_{L,i} - \phi_{s,i})\frac{\sinh((x_{R,i} - x)/\lambda_i)}{\sinh(L_i/\lambda_i)} + \phi_{s,i}$$

where $i = RP, LP$ or C, $x_{R,i}$ and $x_{L,i}$ are the coordinates of the region boundaries, $L_i = x_{R,i} - x_{L,i}$, $\phi_{R,i} = \phi_s(x_{R,i})$, $\phi_{L,i} = \phi_s(x_{L,i})$ ($\phi_{L,LP} = V_{bi}$, $\phi_{R,RP} = V_{bi} + V_{DS}$), and λ_i is a suitable decay length computed according to [5]. Figs. 2 and 3 compare ϕ_s and V_T calculated with the analytical model to those of a drift-diffusion simulator [7] and demonstrate satisfactory mutual agreement over a broad parameters' range. The upper plot in Fig. 4 reports the analytical linear threshold voltage of submicron MOSFETs as a function of the pocket penetration in the channel (L_P). As can be seen, a critical L_P exists ($L_{P,crit}$) that yields a V_T independent of channel length. Below $L_{P,crit}$ the threshold voltage of the longer devices is controlled by the channel doping and unaffected by the halo, whereas that of the short ones exhibits relevant SCE. Around $L_{P,crit}$, an optimum region exists where V_T is controlled by the halo, but still fairly independent of L_G. Well above $L_{P,crit}$, instead, relevant reverse short channel effects (RSCE) arise, eventually compromising the flatness of V_T versus L_G. Qualitatively similar results are observed at high V_{DS}, although the curves exhibit a larger spread than at small V_{DS}.

To explain this behavior, Fig. 5 reports $\phi_s(x)$ of devices with increasing L_P biased at $V_{GS} = V_T$ (i.e., having the same $\phi_{s,min}$). Clearly, $L_{P,crit}$ corresponds to the physical

condition in which two distinct minima appear in the surface potential. The model has been used extensively to derive first-order halo design guidelines for short MOSFETs and to restrict the range of suitable halo parameters. L_P values corresponding to a controlled V_T for a given L_G range and fixed N_P and N_C have been calculated, resulting in the contours of Fig. 6, where the limits of each shaded region correspond to $L_G = 0.5$ μm and $L_G = 0.09$ μm.

Full two-dimensional simulations.

To refine the first order choices above and verify halo control of SCE, a more realistic model of the halos has been adopted. In particular, halos have been described with gaussian profiles parametrized by the quantities defined in Fig. 7. The super steep retrograde channel profile, the source/drain and the MDD structure, instead, representative of a 0.13μm technology, were tentatively kept fixed to emphasize the role of halos on device performance.

Two different optimization strategies have been explored through extensive two dimensional drift diffusion simulations including Van Dort's quantum mechanical corrections [8]. Both assume $Y_{peak} = L_{vert} = X_j/2$ to limit the increase of junction capacitance due to boron spreading below the source and drain. The first strategy (denoted (a) in the following) assumes that the ratio between the vertical and lateral standard deviation of the gaussian halos ($\eta = L_{lat}/L_{vert} = 0.3$) is fixed by processing conditions. N_P is then optimized for each implantation angle (θ) to get the flattest V_T compatible with a RSCE lower than $\approx$ 30 mV. The second strategy (b) aims at the same goal with respect to V_T flatness, but changes the ratio $\rho = (X_{peak} + L_{lat})/(Y_{peak} + L_{vert})$ as a function of θ according to the data in [1]. These strategies are summarized by the ρ versus θ curves in Fig. 8, and emulate different processing conditions. Notice that strategy (a) corresponds to a steeper lateral halo profile than strategy (b).

Performance analysis.

Fig. 9 reports V_T as a function of L_G for different θ and optimization strategies. The corresponding optimum N_P is shown in Fig. 10. We observe that, for a given maximum RSCE, a small θ is beneficial to achieve a flat V_T over a large L_G range. Furthermore, strategy (a) provides better SCE control than strategy (b), thereby confirming that a steep halo profile is needed in the lateral direction. Such steep profiles, however, have a detrimental effect on the sensitivity to process variations and in particular to the spread on $\eta = L_{lat}/L_{vert}$. This is shown in Fig. 11, reporting V_T curves for different η values. Finally, Fig. 12 reports the off state current of the optimized devices, demonstrating less than 10^{-9} A/μm for progressively lower L_G as θ is decreased.

Conclusions.

In summary, a quasi two-dimensional model and drift diffusion simulations were exploited to derive halo design guidelines for a scaled MOS technology. Results indicate that the lateral halo steepness plays a crucial role in controlling SCE and I_{off} for a given source/drain structure. Simulations results, however, demonstrate that super steep profiles require tighter control on process conditions due to increased sensitivity to process variations.

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This work was partially supported by the UE in the framework of the ULIS project.

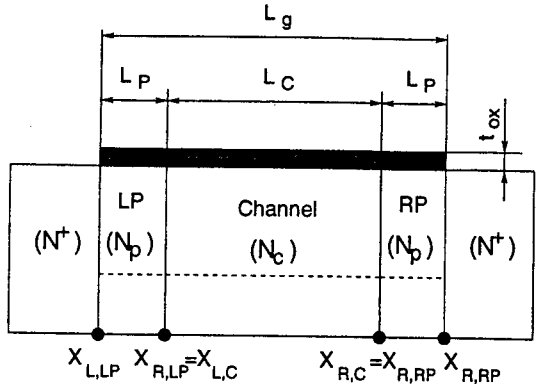


Figure 1: Schematic MOSFET cross section with the definition of the analytical model parameters.

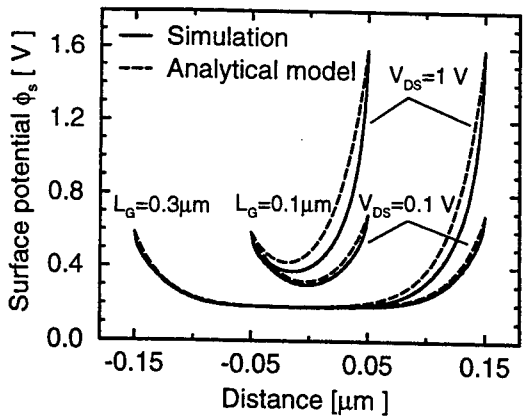


Figure 2: Comparison of the surface potential calculated by the analytical model with that of fully two-dimensional drift diffusion simulations. $V_{GS} = 0$ V, $t_{ox} = 40\AA$, $N_C = 5 \cdot 10^{17}$ cm^{-3}.

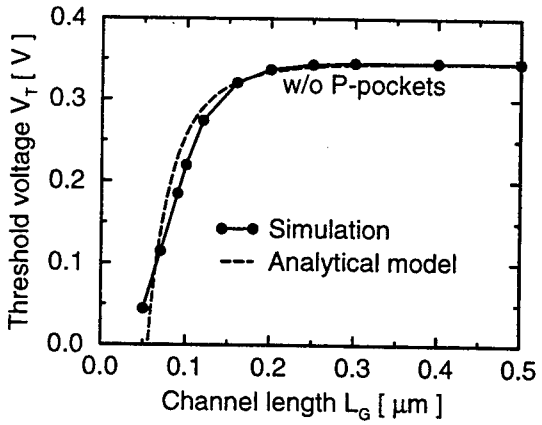


Figure 3: Threshold voltage calculated with the analytical model (dashed line) and with fully two-dimensional drift-diffusion simulation (solid line). $N_C = 5 \cdot 10^{17}$ cm^{-3}, $t_{ox} = 40\AA$, $V_{DS} = 1$ mV.

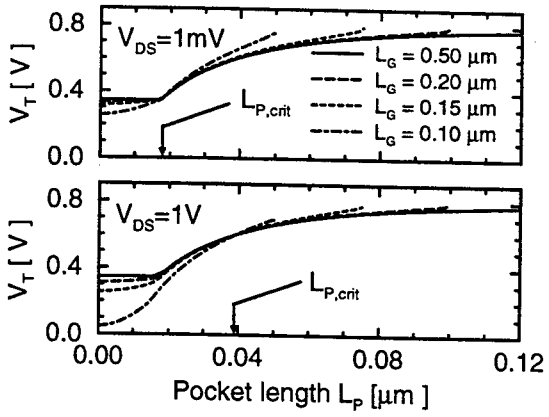


Figure 4: Threshold voltage V_T of halo devices at V_{DS}=1 mV (upper graph) and $V_{DS} = 1$ V (lower graph), as a function of pocket length L_P. $N_C = 5 \cdot 10^{17}$ cm^{-3}, $N_P = 2 \cdot 10^{18}$ cm^{-3}, $t_{ox} = 40\AA$.

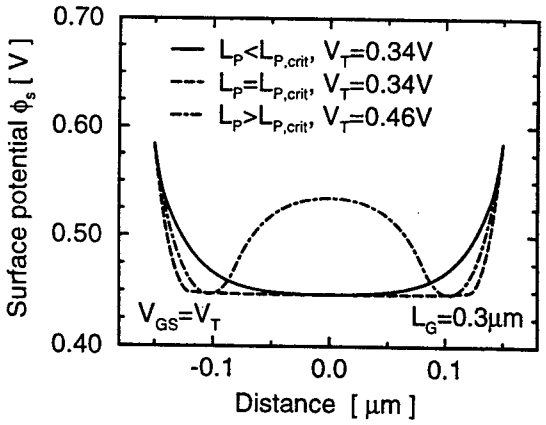


Figure 5: Surface potential of halo devices featuring $V_{GS} = V_T$ and different pocket length L_P but constant channel and pocket doping ($N_C = 5 \cdot 10^{17}$ cm^{-3} and $N_p = 10^{18}$ cm^{-3}, respectively). V_T is unchanged as long as the surface potential exhibits only one minimum.

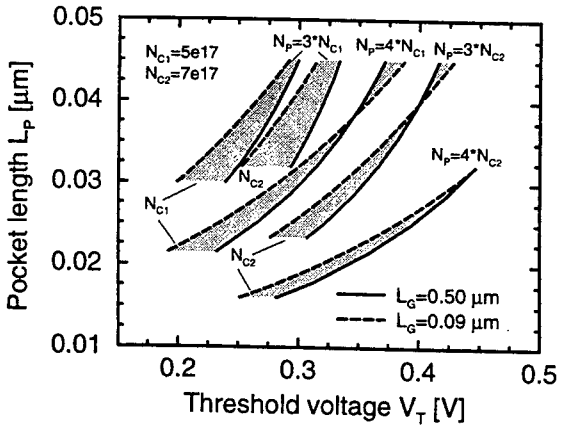


Figure 6: Halo extension L_P versus V_T for $L_G = 0.5$ µm (solid lines) and $L_G = 0.09$ µm (dashed lines) for different N_C and N_P combinations. $N_{C1} = 5 \cdot 10^{17}$ cm^{-3}, $N_{C2} = 7 \cdot 10^{17}$ cm^{-3}, $t_{ox} = 2.5$ nm. $V_{DS} = 1.2$ V.

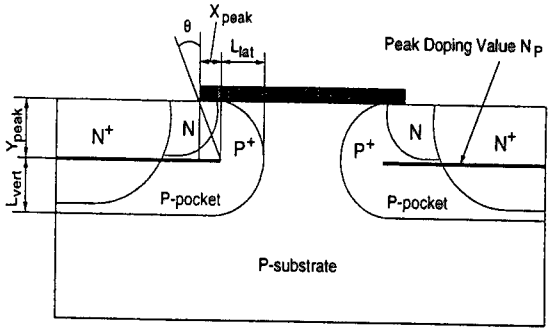


Figure 7: Schematic cross section of a MOSFET with the definition of the parameters of the gaussian doping profiles used to describe the halos. L_{lat} and L_{vert} represent the standard deviation of the gaussian profile in the lateral and vertical direction, respectively.

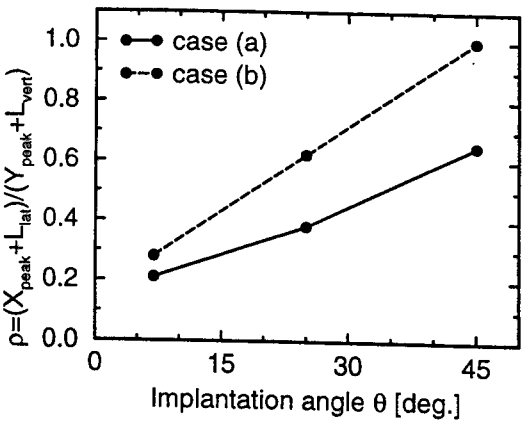


Figure 8: Relationship between the pocket implantation angle θ and $\rho = (X_{peak} + L_{lat})/(Y_{peak} + L_{vert})$ according to: a) assumptions of this work; b) data from [1].

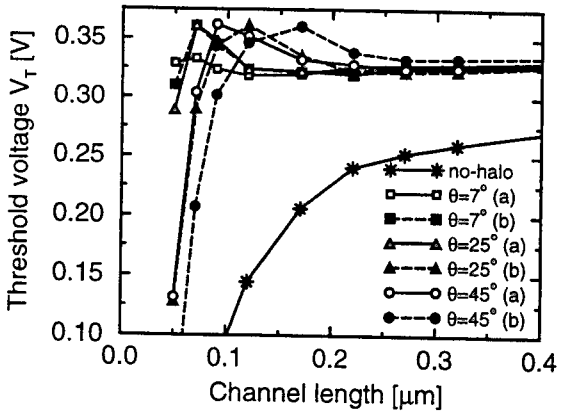


Figure 9: Threshold voltage of optimized structures according to strategy (a) (solid line with open symbols) and (b) (dashed line with filled symbols). $t_{ox} = 25\AA$, $V_{DS} = 1.2$ V. V_T is defined as the V_{GS} such that $I_D = 1\mu A/\mu m$ at $V_{DS} = 1.2$ V.

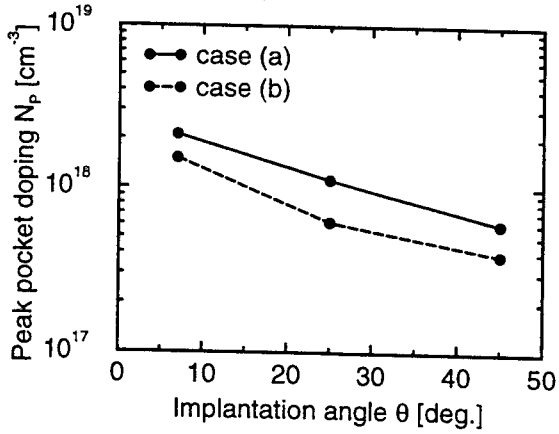


Figure 10: Optimum peak pocket doping as a function of implantation angle θ for the two strategies explored in this work. Symbols are the same as in Fig. 8.

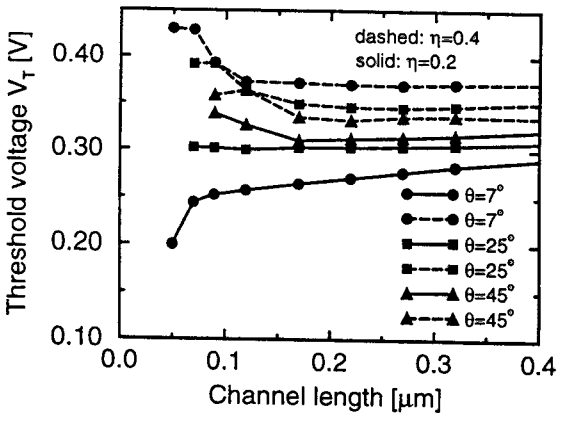


Figure 11: Threshold voltage versus channel length for different implantation angles according to strategy (a) and different values of $\eta = L_{lat}/L_{vert}$. Dashed line: $\eta = 0.4$; solid line: $\eta = 0.2$.

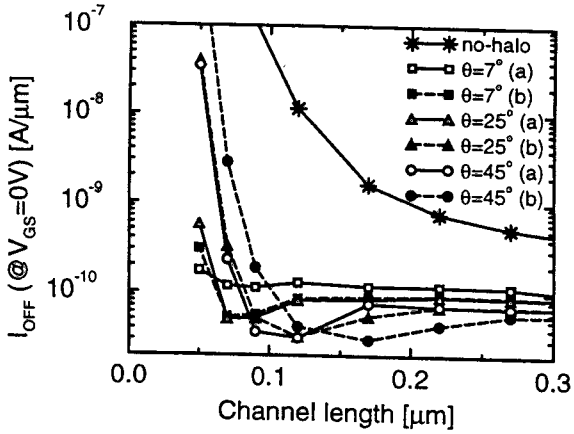


Figure 12: Off state current at $V_{GS} = 0$ V and $V_{DS} = 1.2$ V of the devices in Fig. 9. Solid line: strategy (a); dashed line: strategy (b).

High-Temperature Glass-Ceramic Substrates for Thin Film Electronics

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I. INTRODUCTION

The economical production of thin film polycrystalline silicon electronic devices, including solar cells and active matrix liquid crystal displays (AMLCDs), requires transparent substrates that can be processed at high (>700°C) temperatures. The most heat resistant commercial glass substrates soften at temperatures above 620 °C. Fused silica (often referred to as 'quartz') is transparent and meets the temperature requirements but is expensive and its thermal expansion coefficient is 1/5 of that of silicon, leaving a polysilicon layer deposited at high temperature under a tensile stress.

Glass-ceramics offer an alternative to glass to fabricate transparent, high-temperature substrates that can be matched to the thermal expansion of silicon. The strategy is to keep the grain size small (< 150 Å) to reduce scattering of the light and to control the valence state of Ti to avoid coloring of the substrate. The main concern in processing glass-ceramics is that the glass components can out-migrate from the substrate and contaminate the device.

II. GLASS-CERAMIC SUBSTRATES

After surveying glass-ceramic systems, the composition system SiO_2-Al_2O_3-ZnO-MgO-TiO_2-ZrO_2 was selected [1]. The final microstructure of the glass-ceramic consisted of 10-15 nm-sized spinel crystals, dispersed uniformly in a siliceous glass matrix. The transparency of 2 mm thick uncoated glass-ceramics was over 90 %.

Some glass components, such as alkali atoms, are mobile at elevated temperatures and can migrate out of the substrate during high temperature processing [2]. To prevent the out-migration of substrate components into the thin film electronics the glass-ceramic substrates need to be coated with a barrier layer.

After investigating various schemes, a barrier layer consisting of 1000 Å of SiN_x followed by 1000 Å of SiO_2, both deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD), was selected. To check the effectiveness of the barrier layer in stopping ion out-migration, coated substrates were annealed in N_2 at 900 °C for 8 hours. Secondary ion mass spectroscopy (SIMS) showed that the concentration of glass components dropped in the SiN_x layer and reached background levels in the following SiO_2 layer.

To demonstrate the suitability of these substrates for thin film electronics at high temperatures, both majority carrier devices (thin film transistors) and minority carrier devices (p-i-n junction diodes) were fabricated.

III. THIN FILM TRANSISTORS

Thin Film Transistors (TFTs) permit quantitatively measurement of the carrier mobility and density of mid–gap states in polysilicon. To competitively evaluate various substrates TFTs were fabricated on oxidized single crystal silicon (8600 Å thermally grown), barrier layer coated glass-ceramic and fused silica substrates. The 1000 Å thick channel polysilicon was deposited by LPCVD at 550 °C as amorphous and then recrystallized at 900 °C. The gate oxide was also deposited by LPCVD at 450 °C. A detailed process description can be found at [3,4]. The device characteristics were analyzed using a combination of classical MOSFET theory [5] and TFT theory [6].

Non-hydrogenated TFTs fabricated on all substrates had lower leakage currents and higher carrier mobility (Table 1) than devices fabricated previously on Corning 1737 glass substrates at 620 °C [4]. Figure 1 shows typical current-voltage ($I_d(V_g)$) curves for TFTs fabricated on various substrates. Figure 2 presents the corresponding densities of gap states (DOS) in polysilicon gap deduced by the temperature method [7]. It should be noted that the performance of TFTs on glass-ceramic and fused silica substrates exceeds those on oxidized silicon wafers. Possible reasons for different performance of TFTs fabricated on different substrates include different grain structure, different gettering ability of substrates, and the electric field distribution in TFT with and without a ground plane, all of which are being investigated

IV. P-I-N JUNCTION DIODES

To investigate if glass-ceramics would make suitable substrates for thin polysilicon film solar cells, we fabricated and tested p-i-n junction diodes on barrier layer coated glass-ceramics, fused silica substrates and oxidized silicon wafers. The device consisted of 500 Å n+, 6000 Å undoped (i-) and 1500 Å p+ polysilicon deposited at 550 °C and annealed for 4 hours at 900 °C. Grain size of the deposited polysilicon film ranged from 100 Å to 1000 Å. The structures were patterned by photolithography and etched to form isolated devices. Aluminum contacts were deposited on the top and annealed in H_2 at 400 °C for 0.5 hour.

The dark current-voltage characteristics (I-V) were measured and analyzed. P-i-n junctions on both glass-ceramic and oxidized silicon substrates had low reverse leakage currents and high breakdown fields, while on fused silica device performance was much poorer (Fig. 3). Oxidized silicon and glass-ceramic substrates have a coefficient of thermal expansion (CTE) matched to Si, whereas fused silica does not. During cooldown from the high temperature anneal the difference in CTE induces a tensile strain of 0.2% into the polysilicon film. The corresponding tensile stress can reach 60 000 psi exceeding breaking strength of polysilicon which is between 10 000 and 35 000 psi [8]. Visual inspection confirmed the formation of cracks in the polysilicon films that degrade the performance of large area devices fabricated on fused silica substrates.

The forward current-voltage characteristics of solar cells and p-i-n diodes followed an exponential law with ideality factor of ~ 2. This behavior is expected for semiconductor materials such as polycrystalline silicon containing near mid-gap recombination states [9].

V. SUMMARY

Novel transparent glass-ceramics having high strain point (over 920 °C) and CTE matched to Si, developed by Corning Incorporated, were shown to be suitable substrates for high temperature fabrication of thin film polycrystalline solar cells and thin film transistors. Out-diffusion of glass components from the substrate was effectively suppressed with a PECVD SiO_2/SiN_x barrier layer.

Thin film transistors fabricated at 900 °C on glass-ceramic substrates had leakage currents and electron mobilities comparable to devices on fused silica and oxidized silicon wafers.

The performance of p-i-n junction diodes, simulating solar cells, fabricated on the glass-ceramic substrates matched that of devices made on oxidized silicon. The difference in thermal expansion coefficient of silicon and fused silica was shown to be the reason for the poor performance of p-i-n diodes fabricated on fused silica substrates.

ACKNOWLEGMENTS

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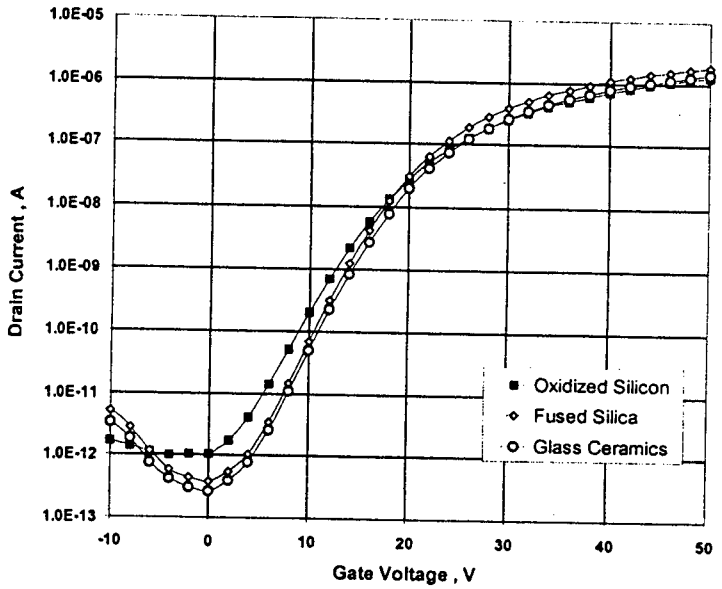


Figure 1. Current-voltage characteristics of thin film transistors fabricated on oxidized silicon, fused silica and glass-ceramic substrates. Channel size is 15 x 15 mkm^2. Source-drain voltage V_{sd} = 0.15V.

	V_{fb}, V	I_{min}, pA	mobility, $cm^2/V \cdot sec$	Q_t, $10^{12}cm^{-2}$	S, V/decade
Oxidized Silicon	-1.5	0.97	68.3	2.1	3.48
Fused Silica	0	0.38	220	2.1	3.00
Glass-Ceramic	-0.5	0.27	179	2.2	3.05

Table 1. Parameters of TFTs fabricated on glass-ceramic, fused silica and oxidized silicon wafers. The columns list, left to right, the flat band voltage, V_{fb}; the leakage current, I_{min}; the intrinsic electron mobility; the trap density Q_t; the subthreshold slope S.

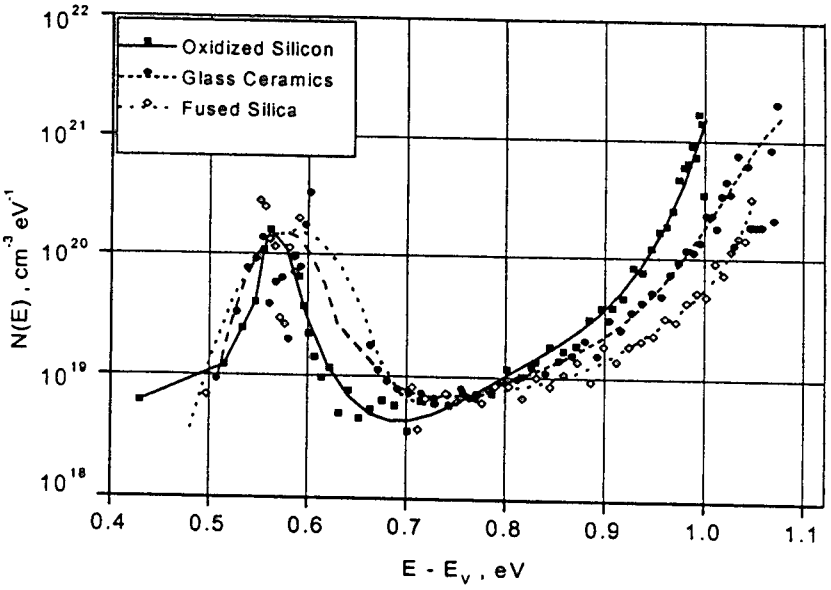


Figure 2. Densities of gap states in polysilicon films deposited on oxidized silicon, glass-ceramic and fused silica substrates. DOS were deduced by the temperature method [7] (dots). Lines are guides for the eye only.

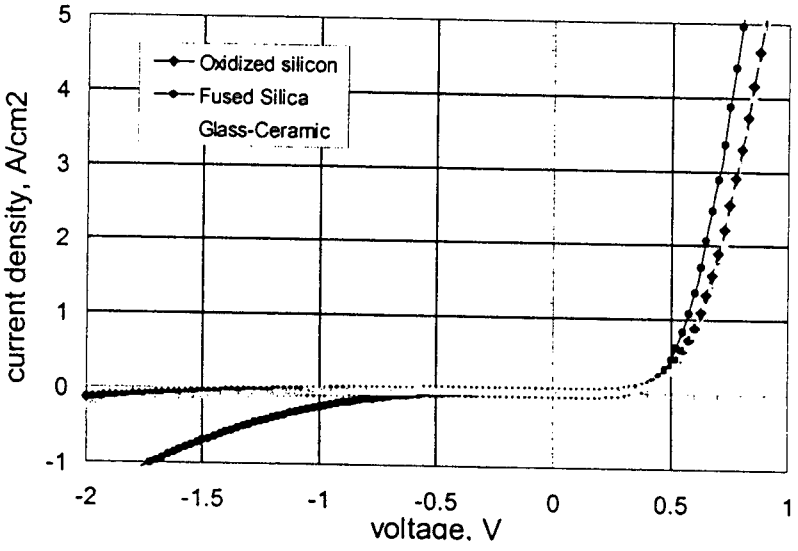


Figure 3. Dark current voltage characteristics (I-V) of p-i-n junction diodes fabricated on oxidized silicon, fused silica substrates and barrier layer coated glass-ceramic.

Aharonov-Bohm interference in semiconductors: Coherent transport of one-dimensional electrons in InAs quantum wires

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1. INTRODUCTION

Bloch electrons by definition have long-range phase coherence without scattering. But, realistically, due to random electron-phonon and electron-electron scattering, the coherence length of electrons in high-mobility GaAs/$Al_xGa_{1-x}As$ heterojunctions is found to be only several microns at 4.2K, [1] and in silicon MOSFETs, it is approximately 20 nm at room temperature. The device dimension should be much less than the coherence length in order to substantiate the quantum phase coherence in the device characteristics.

Limited by the surface Fermi level pinning voltage in GaAs-based system, almost all coherent transport experiments are done with a "split-gate" geometry, where Schottky gates at the surface deplete 2D electron gas below. [2] By defining multiple electrodes at the top surface, the electron gas is pushed to form wires and dots. One disadvantage of this approach is that the potential confining the electrons is so smooth that the size of the quasi-zero-dimensional quantum dot is typically one micron in diameter. Due to such a large dimension, size-quantization effect can only be observed at very low temperature.On the other hand, the Fermi level pinning position of InAs is unique: it is pinned at ~ 100 meV above the conduction band minimum. Thereby, it is still possible to make an n-type ohmic contact to InAs wires without surface depletion problem. We have developed a fabrication process realizing such a system. Aharonov-Bohm rings [3] and quantum ballistic transistors have been designed, fabricated and characterized.

2. EXPERIMENT

The sample is grown by MBE on S.I. GaAs substrates. Following a 2 micron AlSb/GaSb superlattice buffer, a 12 nm InAs quantum well is grown. A 12 nm AlSb barrier caps the InAs quantum well. Negative electron-beam resist is used as the etch mask, which in turn defines the nanometer-scale structures in an RIE process. Fig. 1 shows an SEM micrograph of a finished Aharonov-Bohm ring, after the e-beam resist is removed. The wire width for this specific ring is ≅ 50nm. Magnetotransport is used to demonstrate the effect of phase coherence. A nanoAmpere ac current of 16.7Hz is fed into the leads at opposite sides of the ring. Four-terminal longitudinal magnetoresistance measurement is taken at 1.5K. Data shown in Fig. 2 is the magnetoresistance of the ring as a function of a sweeping magnetic field perpendicular to the plane of the ring structure. As a result of interference, many oscillations are observed. Such oscillatory feature in theory is periodic in magnetic field. The Aharonov-Bohm theory predicts a period

of hS/e, where h is hyperfine constant, S is the area of the ring, and e the electron charge.

Figure 3 is the Fourier spectrum of the data shown in Fig. 2. The first peak comes from the AB interference, and the 2nd, 3rd and the 4th are higher order harmonics. These four peaks in the Fourier transform power spectrum are clearly equally spaced, with the period consistent with the area of the ring. Furthermore, the observed damping of the peaks can be used to estimate the coherence length, following theory developed for one-dimensional electron gas. More data and detailed analysis will be presented at the conference.

In addition, we have defined a Schottky gate on one arm of the AB-ring by electron-beam lithography, metal evaporation and lift-off. A gate with 30nm width can successfully control the potential in the quantum wire channel. Data of such electrostatic version of AB-rings will also be presented at the conference.

3. SUMMARY

An InAs-based Aharonov-Bohm interference ring is characterized. The coherence length is measured to be much longer than the diameter (300nm) of the ring. The sample system is a 12nm high-electron mobility InAs quantum well, patterned by electron-beam lithography and subsequent reactive ion-etching for isolation. The unique surface Fermi level pinning voltage at InAs surface allows for population of electrons in 30nm-scale wires/dots. Electrons in the quantum wire have demonstrated the following interesting characteristics. (1) One-dimensional density of states and ballistic transport (from the observed quantized conductance). (2) Long-range phase coherence (from magneto-oscillations of the conductance observed on AB-rings). (3) Strong size-quantization effect (only a few transverse modes are occupied) with large (10meV and higher) intersubband energy separation. (4) Quantum interference behavior dominates in both the transverse and longitudinal magnetoresistance of the InAs quantum wire, even under intense magnetic fields up to 9 tesla. In comparison with other available sample systems, this new quantum wire system offers more flexibility and a favorable coherence length versus device dimension ratio. The implications for device applications will be further discussed.

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Fig. 1
SEM micrograph of an InAs quantum wire, the wire width is ~ 50nm. The loop feature at the middle is for characterizing the Aharonov-Bohm interference, while the Hall bar at right is for transverse and longitudinal magnetoresistance measurements.

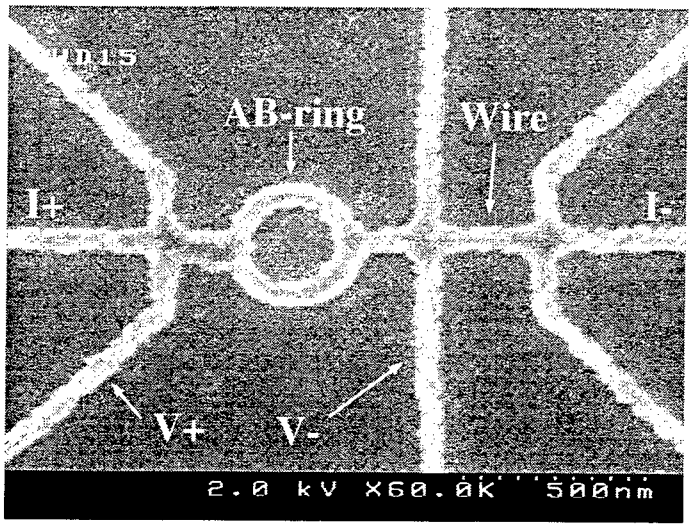


Fig. 2
Magneto-oscillations of the resistance of an Aharonov-Bohm ring structure. The resistance of the ring is plotted against a sweeping magnetic field. The oscillatory features persists up to 9 tesla without apparent changes in the characteristics.

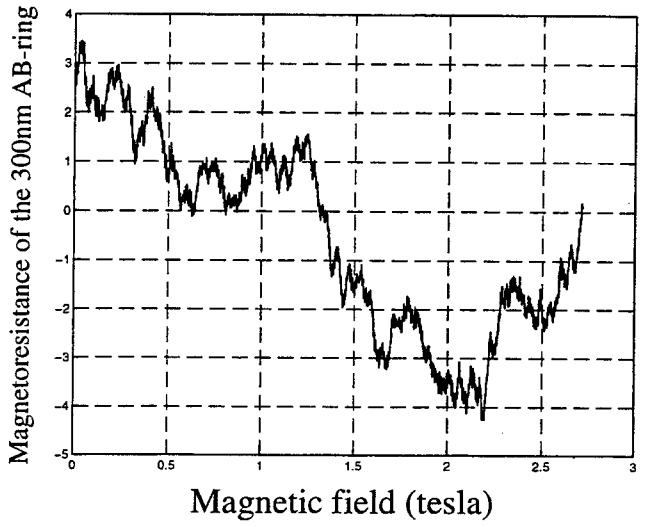
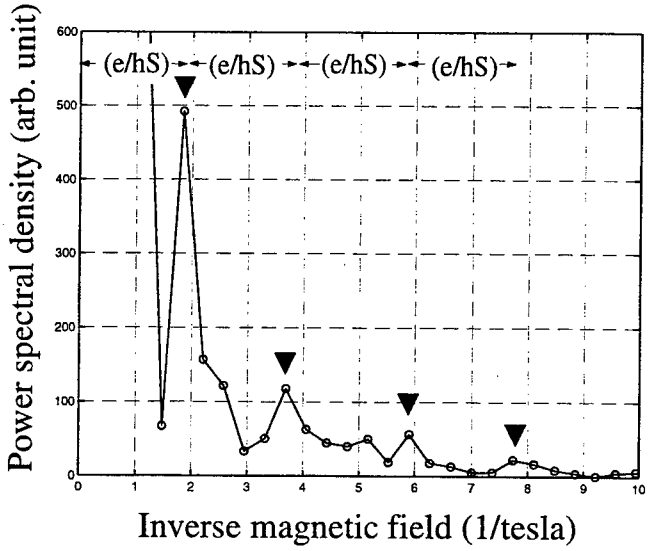


Fig. 3
Fourier spectrum of the data shown in Fig. 2. In addition to aperiodic oscillations, four apparently equally spaced peaks are observed. The spacing is determined by the loop's area S.



A NOVEL HEMT/FET ZEROBIAS DIODE

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Abstract- A zero bias diode based on enhancement FET or HEMT technology is described, realized and characterized for the first time. A diode with a tailored turn-on voltage can be realized by simply connecting the gate and drain of the device. The series resistance of the diode is determined by the sum of the on-resistance of the channel and the source and drain resistances. This diode can replace diodes based on the gate-Schottky diode often used in MMICs for applications such as mixers, frequency multipliers, and detectors.

I. INTRODUCTION

The FET/HEMT MMIC technology is today a mature and widely accepted technology for use in microwave and millimeter wave communication and radar systems. The FET/HEMT device can be used for many different circuit functions like amplifier, mixer, frequency multiplier, oscillator, digital circuits etc. In some circuits, designers would also like to have access to diodes. This is possible by using the gate as an anode and connecting the source and drain together to form the cathod. This diode has however some disadvantages like a high turn-on voltage, a high series resistance and a high dc-gate current which might be the result when the diode is used as rectifying element is normally not recommended due to possible problems with reliability. The exist some MMIC-processes based on high quality Schottky diodes with a cut-off frequency in the Thz-regime, however no active devices are then available for active circuits. In principle it would also be possible to combine high quality diodes with active devices by using selective epitaxy or ion-implantation processes. Some FET and HEMT -processes can provide both depletion and enhancement devices in the same process. For the users of these processes we believe that the suggested zero-bias diode can be an interesting alternative in order to realize diodes for certain circuits.

II. THE ZERO BIAS DIODE

The function of this diode can be understood by realizing that a FET/HEMT at low drain-source voltage can be regarded as a gate-voltage controlled resistor. This resistance can be varied from hundreds of MΩ to a minimum value determined by the source and drain resistances and the minimum channel resistance. Typical values are 1-2 Ω·mm. i e a device with 100 μm width will have a series resistance of 10-20 Ω. If we connect the gate with the drain of an enhancement device, we will have a two terminal device, a diode which is turned on at a positive voltage. This voltage is mainly determined by the barrier height of the Schottky diode, the doping concentration and the thickness of the gate-Schottky layer. For a n-type MESFET the threshold voltage is

$$V_{th} = V_{bi} - \frac{q \cdot N_d \cdot a^2}{2 \cdot \varepsilon}$$

V_{bi} is the built in voltage, N_d is the doping concentration, a is the thickness of the channel, q is the electron charge and ε is the permittivity of the semiconductor. For a HEMT with homogenous doping in the Schottky layer the the threshold voltage is

$$V_{th} = \Phi_b - \Delta E_c - \frac{q \cdot N_d \cdot d^2}{2 \cdot \varepsilon} + \Delta E_{F0}$$

Φb is the barrier height and d is the thickness of the high bandgap Schottky layer, ΔE_c is the conduction band discontinuity and ΔE_{F0} is a small constant, the energy difference between the conduction band edge and the first sub band in the quantum well. For the delta doped HEMT we have

$$V_{th} = \Phi_b - \Delta E_c - \frac{q \cdot N_{dss} \cdot d}{\varepsilon} + \Delta E_{F0}$$

N_{dss} is the surface charge density of the deltadoping. By designing the device so that Vth is positive, an enhancement type FET/HEMT can be fabricated.

III. SIMULATIONS AND EXPERIMENTAL RESULTS

A set of different diodes were fabricated and tested. Different layouts are shown in Fig.1. For the experimental demonstration of the device, a commercially available E/D HEMT foundry process was used (ED02AH from PML, Philips). The nominal gate length of the HEMT is 0.2 μm and ft is 63 GHz. The gate width is 100 μm and number of gate fingers is 4.

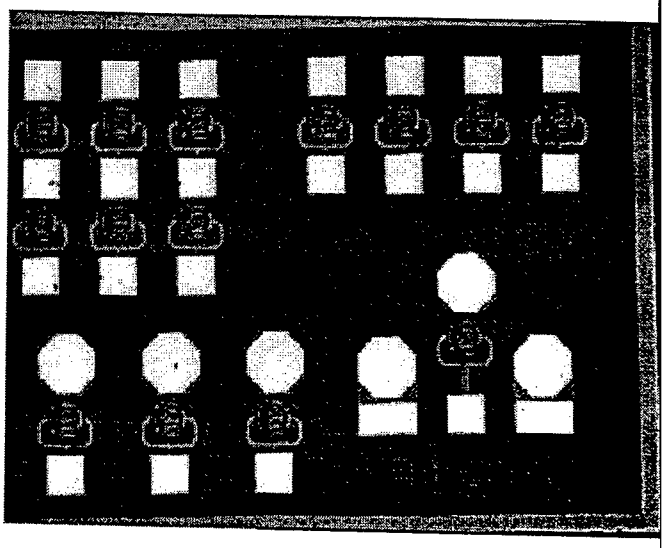


Fig 1 Different diode configurations

The layout contain diode-pairs, single diodes and a CPW-diode. The I-V characteristic of diodes were measured by using a hp 4145 parameter analyzer, the result is plotted in Fig.2. This figure is indeed the I-V characteristic of a diode.

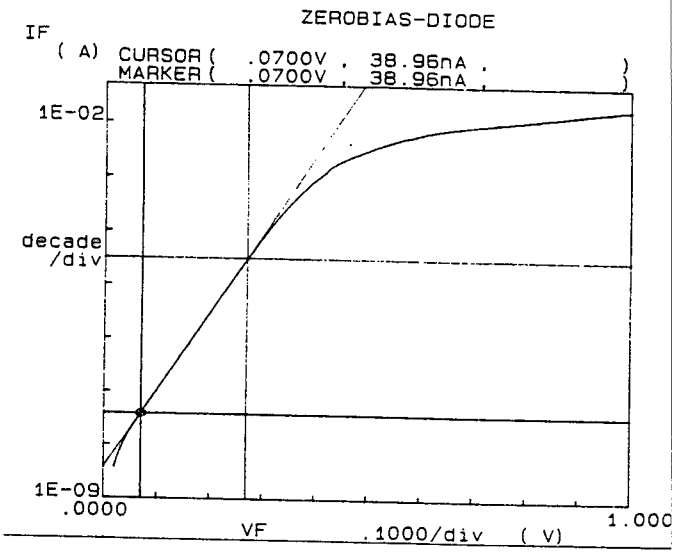


Fig 2 The measured I-V characteristic of the new zero-bias diode

Bias-dependent S-parameters were calculated and measured by using the CPW-layout shown in Fig.1. In the simulation, the diode was modeled by using a nonlinear

circuit model of the transistor and connecting the gate and the drain. The influence of the pad and connecting transmission line were not considered so the result is relevant for the intrinsic device. In Fig.3 the modeled S-parameters are shown for different currents 0.1, 0.2, 0.5, 1, 2, 5 and 10 mA. As can be seen from the Smith-diagram, the diode can be switched from a high impedance state at negative voltage to a low impedance state at a positive voltage. The resistance in the 'on' state is a combination of the source, drain, and the minimum channel resistance and is approximately 20 Ω for this device. In the off-state, the equivalent capacitance is 56 fF, therefore the cut-off frequency $f_c=1/2\pi C_{off} R_s$ is 148 GHz.

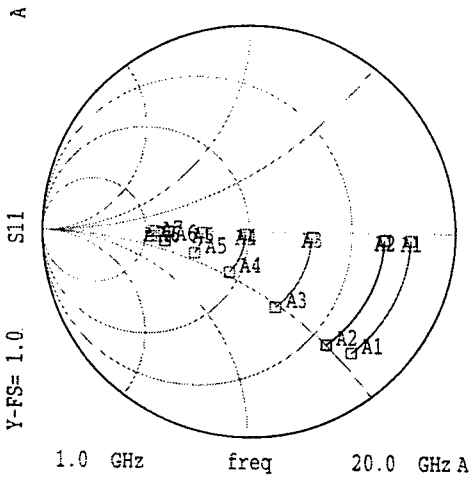


Fig 3 Modeled S-parameters of the diode at different bias currents (0.1, 0.2, 0.5, 1, 2, 5 and 10 mA). The frequency varies between 1-20 GHz

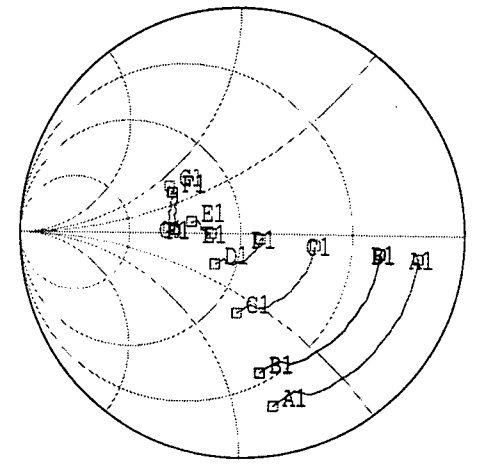


Fig 4 Measured S-parameters of the diode at different bias currents (0.1, 0.2, 0.5, 1, 2, 5 and 10 mA).The frequency varies between 2-21 GHz

The measured S-parameters for the device including the probe-pads and the connecting transmission lines are shown in Fig 4. Experimental and simulated characteristics are similar and we have to remember that the experimental data also include the characteristics of the probe pattern and connecting transmission lines.

VI. SUMMARY

A new device, a zero-bias diode is described for the first time. 'Proof of concept' for this diode was demonstrated by fabrication of devices and by measuring current-voltage characteristics, and bias dependent S-parameters. This type of diode can be used as a complement in E/D mode HEMT/MESFETs MMIC's whenever a Schottky diode is needed. Due to the small equivalent barrier height of this diode, dc-bias can be omitted which simplifies the design of mixers, detectors etc.

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A CMOS-Compatible Single-Poly Cell for Use as a Non-Volatile Memory

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Abstract: A low-voltage non-volatile memory device using a standard CMOS process without additional processing steps is investigated for embedded applications. The cell consists of a PMOS transistor in which no electrical contact is made to its gate electrode and a series NMOS access transistor. Experimental data show that sufficient read current and disturb lifetime can be achieved. Data retention characteristics are also examined.

Introduction: In ASIC circuits, it is often desirable to have available a low-cost, low-density non-volatile memory device. However, process complexity hinders the incorporation of traditional non-volatile memory devices into CMOS circuits. The need for multiple polysilicon layers, different gate oxide thicknesses, and modified junction doping profiles, for example, is responsible for added process complexity and cost. The proposed structure (NSC patents pending) circumvents this problem by creating low voltage non-volatile memory cells from standard CMOS transistors. Thus, no additional masking or processing steps are necessary. These advantages in cost and process compatibility make the device useful when small amounts of non-volatile memory are needed for embedded applications.

Cell Structure: Unlike other single-poly EPROM designs, this device does not make use of capacitive coupling between a floating poly gate and an implant situated in the wafer substrate [1,2,3]. Instead, it is merely a PMOS transistor without any electrical contact made to the polysilicon gate. To selectively program and read cells, an NMOS access transistor is placed in series with the floating gate structure. As seen in Figure 1, two transistors are required for each bit. Figure 2 depicts the memory array in which cells can share common word lines and bit lines. Bits can be set to 0 and 1 by controlling the number of electrons stored in the floating gate. An unprogrammed device conducts only a small leakage current. On the other hand, after injection of electrons into the floating gate, a programmed cell can conduct a large amount of current since the electrons induce inversion of the p-channel. To enhance programming, the device may be drawn below the nominal gate length in order to reduce the programming voltage.

Devices organized into a 5x13 bit memory array were fabricated using a 2.5V, 0.25μm CMOS technology. Features include a 50Å nitrided gate oxide, LDD and halo implants, polysilicon gates and $CoSi_2$ salicide. PMOS memory devices were drawn with channel lengths between 0.17μm and 0.24μm. NMOS access transistors were drawn at 0.30μm to guard against punchthrough in the off-state during programming.

Device Operation: Because the gate of the PMOS transistor is floating, it can be used as a charge storage device [4]. Charge injection into the floating gate is instigated by applying a minimum source-drain potential of ~4V. This bias causes a drain current of about 200μA to flow through the device due to a combination of capacitive coupling between the source and the floating gate, drain-induced barrier lowering, and punchthrough. This hole current generates electrons in the drain's high field region through impact ionization. Electrons are thus injected through the gate oxide and accumulated in the floating gate [5,6]. This negative gate charge induces a conductive inversion at the Si/SiO_2 interface, and the device effectively becomes a depletion-mode transistor.

The cell can be programmed by simultaneously applying a pulse of positive polarity to the bit line and the word line. With the NMOS device turned on, current can flow through the memory device. At a sufficient large programming voltage (V_{PP}), the PMOS storage device can be programmed. To read the memory cell, a reading voltage of only 1V is used at the bit line while V_{DD} is applied to the word line.

Since the present implementation of the memory device has no control gate, it could not be erased electrically. However, bulk erasure can be accomplished through UV exposure.

Programming, Disturb, and Retention Characteristics: Depending on the desired programming speed and read current, programming voltages as low as 4V may be used. Figure 4 shows I_{read} as a function of programming time, voltage, and device gate length. Because programming will likely be performed by a charge-pump circuit, a ~1kΩ resistor was placed in series with the memory device to simulate the effect of such a setup. Read current saturates with time because the injected gate current is reduced during programming as the vertical electric field decreases. Channel length dependence of programming characteristics is noticeable but not significant due to the strong effect of halo implants on the PMOS punch-through characteristics.

Because read and write operations differ only in the magnitude of the applied source-drain potential across the PMOS transistor, a cell may be inadvertently programmed during reading. In this case, read disturb lifetime is defined as the stress time necessary to program the device to a read current of 1μA/μm. DC stressing shows that at V_{READ}=1V, the read disturb lifetime exceeds ten years (Figure 5).

Program disturbs may occur in unselected cells when a programming pulse is applied to either a common bit line or word line. For example, when the bit line is pulsed with V_{PP}, the access transistor in an unselected cell is in the cutoff regime because the word line is low. When the word line is pulsed with V_{PP}, the access transistor is turned on, but because the bit line is low, there is no potential drop across the channel. In both cases, no current can flow and thus no inadvertent programming occurs even when stressed at large programming voltages for extended periods of time.

Retention studies were carried out on individual memory devices without an NMOS access transistor across a range of bake temperatures. Degradation characteristics are depicted in Figure 6. Reasonable retention, as reflected in I_{READ}, was observed. As shown in Figure 7, the activation energy of the charge loss mechanism has an activation energy of 1.1eV, which is within the range reported in published work [7].

Summary: A true CMOS-compatible non-volatile memory cell has been demonstrated. The structure can be integrated into a CMOS process without additional fabrication steps. Reasonable drive current levels can be achieved with low programming voltages and read disturb lifetime is excellent. Data retention characteristics have also been reported. The device is suitable for use in low-cost embedded applications which require low voltages. This cell presents a convenient and inexpensive way to introduce non-volatile memory into a CMOS process.

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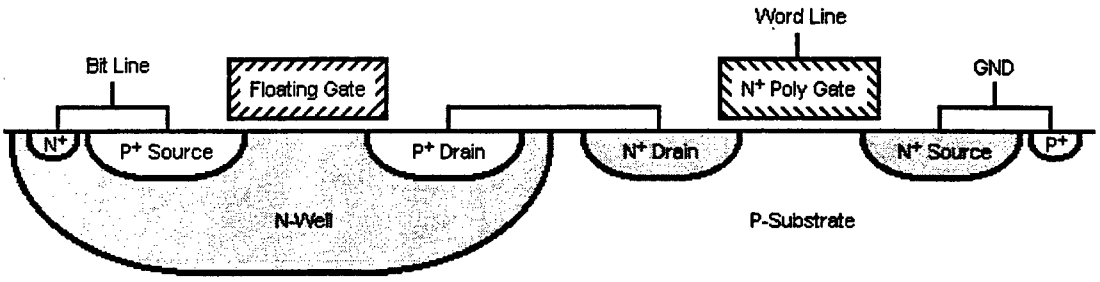


Figure 1: Cell structure consisting of a PMOS transistor with the gate left floating and a series NMOS access transistor

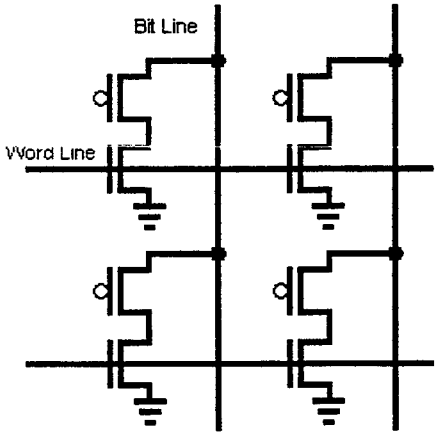


Figure 2: Memory array structure

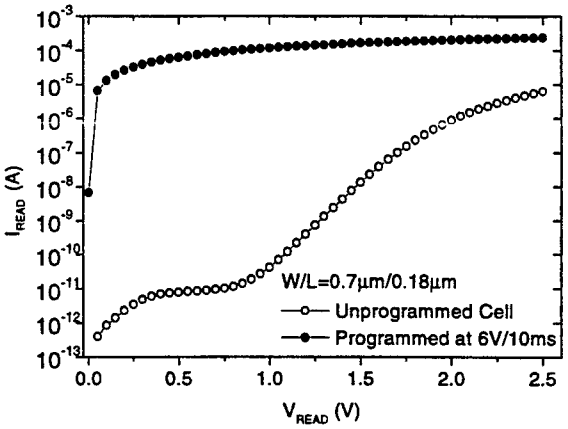


Figure 3: I-V characteristics for programmed and erased cells. Cells include a series 0.7μm/0.3μm access NMOS.

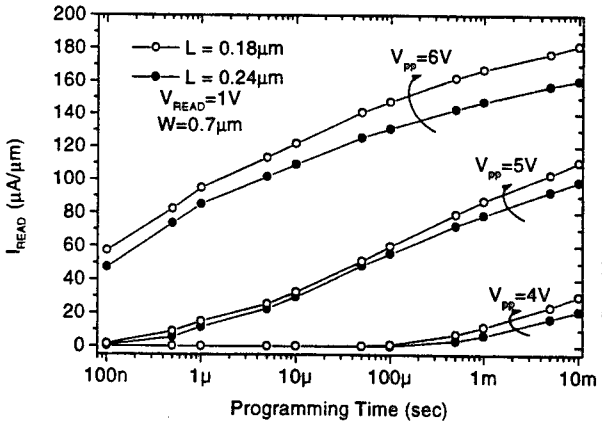


Figure 4: Programming characteristics of a memory device in series with a 0.7μm/0.3μm access NMOS

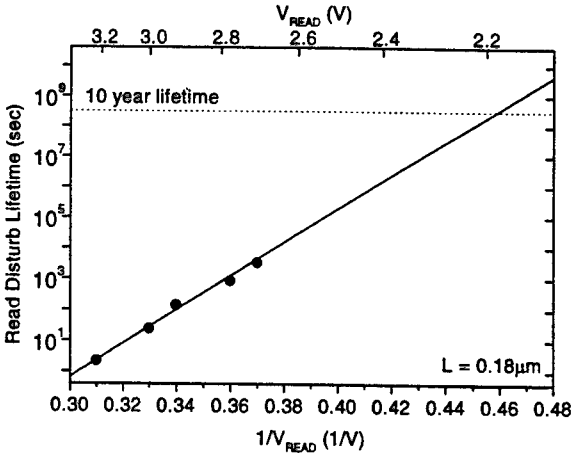


Figure 5: Read disturb lifetime at V_{READ}=1V

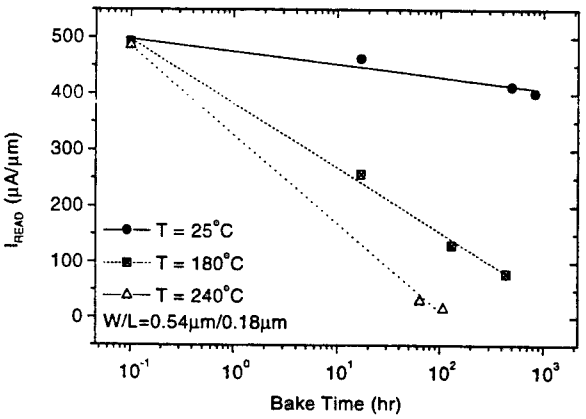


Figure 6: Data retention of an individual memory device (no series access NMOS). Devices were programmed at 6V/50ms. V_{READ}=1.25V

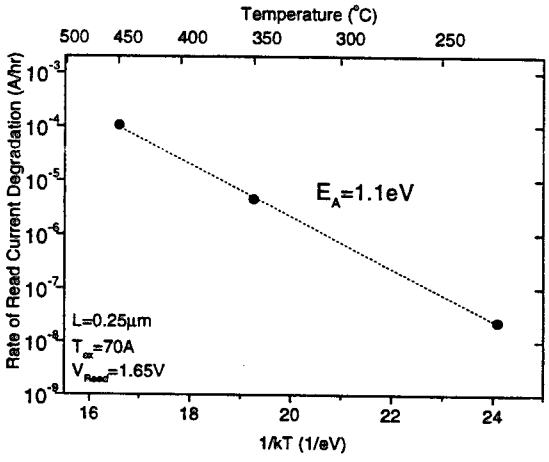


Figure 7: Data retention activation energy extraction

3-D FET: A New Heterodimensional Device for High-Speed Ultra-Low Power Applications

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Abstract

We propose a new device (3-D FET) based on heterodimensional technology and especially suitable for ultra-low power applications. We have analyzed the performance of the new device structures using three-dimensional simulations. Based on the simulation results, we discuss the most promising device design for high-speed ultra-low power applications.

I. Introduction

Heterodimensional technology has been proven to be very promising for future nanoscale high-speed integrated circuits [1]. Several devices based on junctions between electronics systems of different dimensions (in particular, on 2D-3D junctions) have already been fabricated and studied [1-4].

In the new device we propose, we also use lateral gates to control the channel width (similar to the devices in [1-4]), but, in addition, a top gate is used to control the channel charge. Instead of using a heterojunction to create a 2D channel, we propose to use a planar doped layer structure with a Schottky top gate and *p-n* lateral contacts (see Fig. 1). This structure is much easier to fabricate than a heterojunction device [1,5]. Our simulations show that this device should have a very high transconductance and gain, almost ideal subthreshold slope, and greatly reduced short-channel and narrow-channel effects. This eases the scaling down of this device down to the nanoscale range. Because of these advantages, the device is especially suited to high-speed low power applications.

II. Discussion

Fig. 1. shows the device structure in which the doped layer is thin enough to be considered a 2D channel. The two lateral 3D-2D *pn* junctions modulate the channel width. The Schottky top gate modulates the channel charge density. A *pn* junction can be used instead of a Schottky top gate. A low doped *p*-buffer below the channel is necessary in order to suppress parasitic current in the substrate. The top and the lateral gates might be connected, leading to a very high-speed device, since the charge and the width of the channel are simultaneously controlled. This concept is somewhat similar to an "all-around gate" Si-MOSFET [6], although no intention to control the channel width was shown for that device.

The 3-D FET takes advantage of the fact that the depletion depth of the 3D-2D *pn* junctions depends almost linearly on the gate bias in a wide range of gate voltages (instead of a square root behavior, as in three-dimensional junctions). This means that the width of the channel is linearly modulated by the lateral gates. In addition, the charge density of the 2D channel depends linearly on the voltage applied to the top gate.

III. Analytical Model

The lateral depletion depth is given by [7,8]:

$$d_{dep} = 2\varepsilon_s \frac{V_{bi} - V_{GS}}{qn_s}, \qquad (1)$$

where n_s is the sheet density in the 2D channel, V_{bi} is the built-in voltage of the junction, and V_{GS} is the voltage applied to the junction. Therefore, the mobile charge density (per unit length) is given by:

$$q_c = qn_s\left(W - 4\varepsilon_s\frac{V_{bi}-V_{GC}}{qn_s}\right), \tag{2}$$

where V_{GC} is the voltage between the gate and a given position in the channel (at the source end $V_{GC}=V_{GS}$ and at the drain end $V_{GC}=V_{GD}$), and W is the nominal channel width, i.e., the distance between the two gates (Fig. 1). The sheet density, n_s, also depends linearly on the gate voltage:

$$n_s = \frac{\varepsilon_s}{qd}\left(V_{GC}-V_{T0}\right), \tag{3}$$

where d is the distance between the top gate to the channel and V_{T0} is the threshold voltage of n_s, given by $V_{T0}=\phi_b-\frac{qn_Dd}{\varepsilon_s}$, n_D being the sheet concentration of donors in the doped plane.

The mobile charge per unit length can therefore be written as:

$$q_c = c_{eff}\left(V_{GC}-V_T\right), \tag{4}$$

where $c_{eff}=\varepsilon_s(4+W/d)$ is the capacitance per unit length and $V_T=\frac{\frac{W}{d}V_{T0}+4V_{bi}}{W/d+4\varepsilon_s}$ is the threshold voltage.

In addition, since the depletion region within the 2D channel extends in two dimensions, the effective gate length will depend on the gate voltage, decreasing as the gate voltage is increased above threshold, therefore increasing the transconductance. This effect will be very important in deep-submicron devices.

IV. Results of 3D simulation

Using DAVINCI, a three-dimensional drift-diffusion simulator, we explore the main electrostatic design issues of the 3-D FET and we compare its performance with that of conventional planar-doped JFET and 2-D JFET [5]. The material of the simulated device is GaAs. The doping of the p-lateral regions is $10^{19}\,cm^{-3}$. The doping of the p-buffer and of the p-layer between the top gate and the channel are $10^{17}\,cm^{-3}$. Figs. 2-9 show the simulation results.

We observe that: (a) the transconductance increases as d decreases (Fig 2); (b) the threshold voltage increases as W is decreased (Fig 3); (c) the threshold voltage decreases almost linearly as we increase the channel thickness (Fig 4) and d (Fig 5). These observations are in agreement with the theory (including equations) explained above. Besides, V_T decreases as L is decreased (Fig 6, 7), which is a short-channel effect. One of the solutions to make this roll-off smaller is to decrease the channel doping (Fig 6, 8). Although the device is not optimized, we observe in Fig 7 that the threshold voltage roll-off of a 3D JFET device is smaller than the roll-off of the equivalent 2-D JFET and planar-doped JFET. The subthreshold slope and the transconductance are also better. Fig. 9 shows the subthreshold ideality factor dependence on L for 3-D FET, 2D JFET and JFET. To counterbalance the increase of this factor as the channel length decreases, simulations also show that this factor can be decreased if we decrease W, the film thickness, the channel doping, or the distance between the top gate and the channel.

The 3-D FET can also be operated in a multi-gate mode, with two or three independent gate voltages. Although this reduces the speed of the device, it can be useful in some applications. If the top gate voltage is biased at an independent constant voltage, and the same voltage is applied to the two lateral gates, the device behaves as a 2-D JFET; therefore 3-D FET and 2-D JFET can easily be integrated in the same IC circuits.

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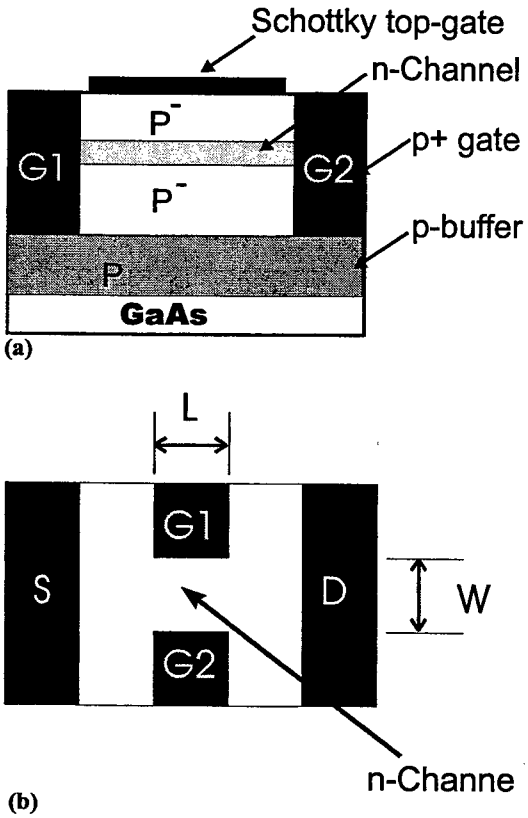


Fig 1. Cross section of a 3-D JFET (a) through the sidegates ; (b) view on the channel layer.

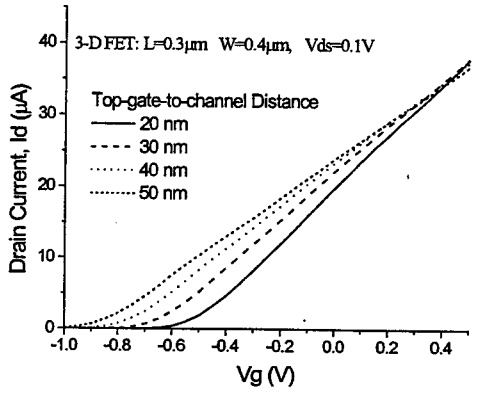


Fig. 2. *I-V* characteristics of a 3-D FET with channel doping $5 \cdot 10^{17}$ cm^{-3}, channel thickness 80 nm and distance gate-channel 30nm

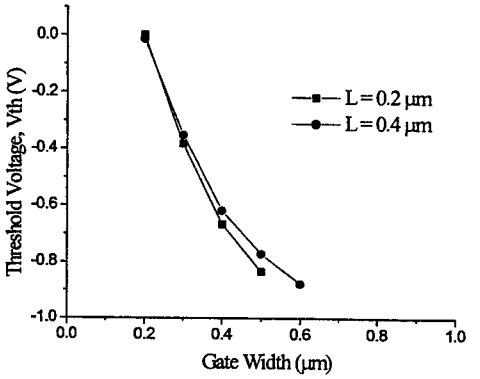


Fig. 3. Threshold voltage dependence on *W* for the 3-D FET as in Fig. 2.

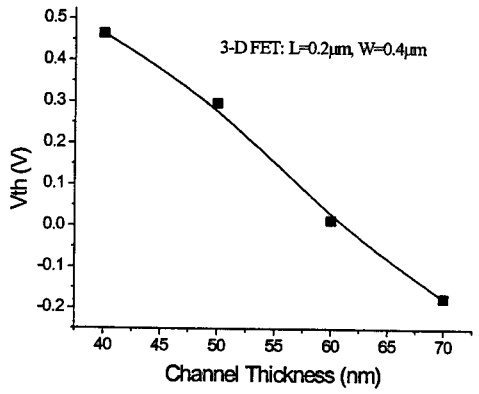


Fig. 4. Threshold voltage dependence on channel thickness for a 3-D FET with channel doping $5 \cdot 10^{17}$ cm^{-3}, distance gate-channel 30nm

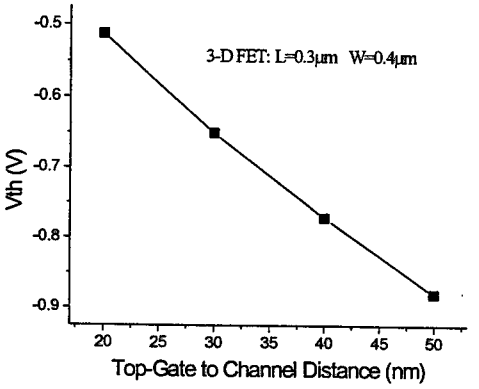


Fig. 5. Threshold voltage dependence on the distance between top gate and channel for a 3-D FET with channel doping $5 \cdot 10^{17}$ cm^{-3}, channel thickness 80nm

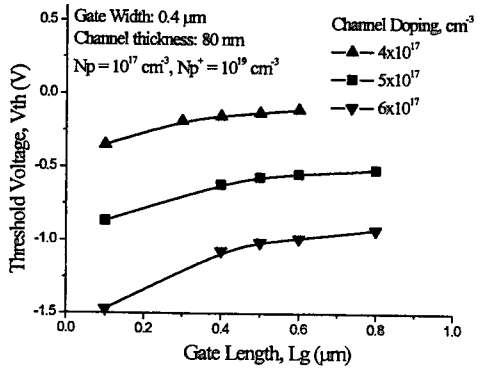


Fig. 6. Threshold voltage dependence on L for a 3-D FET with different channel doping, channel thickness 80 nm and distance gate-channel 30nm

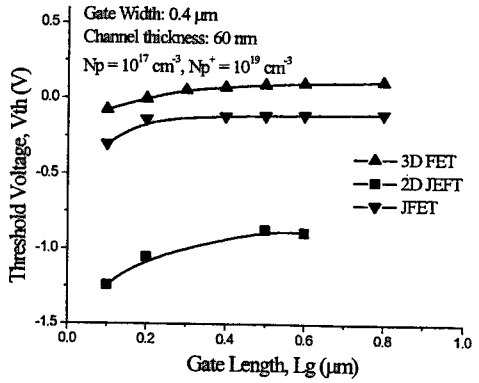


Fig. 7. Threshold voltage dependences on L for a 3-D FET,2D JFET and JFET.

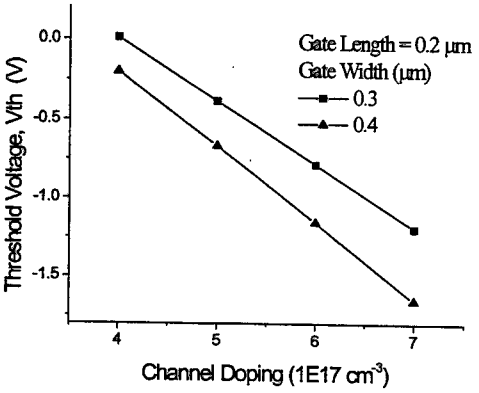


Fig. 8. Threshold voltage dependence on channel doping for 3-D FETs with channel thickness 80 nm and distance gate-channel 30nm

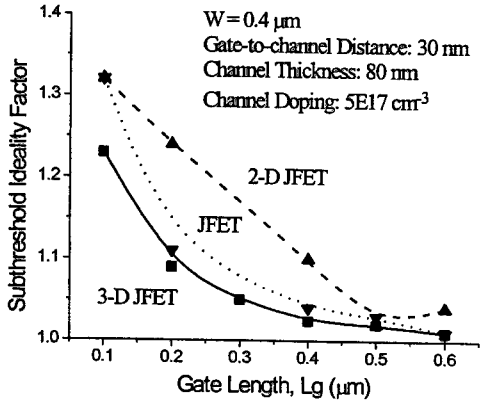


Fig. 9. Subthreshold ideality factor dependence on L for 3-D FET, 2D JFET and JFET.

MBE Growth and Device Applications of III-V Compound Semiconductor Nanowires

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1. Introduction

One of the important building blocks for future nanoelectronics seems to be the nanowire structure made out of semiconductors. Standard approaches for semiconductor wire formation include; (1) direct application of standard Si ULSI processing technologies, such as EB lithography, dry etching, oxidation to silicon or silicon-on-insulator(SOI) wafers, (2) wire formation on III-V multi-layer hetero-epitaxial wafers by EB lithography and etching, (3) selective depletion of 2DEG in III-V multi-layer heteroepitaxial wafers by Schottky split gate, (4) realization of III-V semiconductor wires by selective growth on specially patterned substrates, (5) realization of III-V semiconductor wire structures by area-selective growth using patterned insulator windows, and (6) direct fabrication of nanostructures by scanned probe-induced atom-manipulation or surface reaction.

In the present paper, formation, properties and device applications of two novel types of III-V compound semiconductor wires grown by MBE based techniques are presented and discussed[1]. One type of the wire is the gate controlled GaAs wires using the Schottky in-plane gate (IPG) and the Schottky wrap gate (WPG), formed on the trapezoidal etched wires produced by the above approach (2) on MBE grown AlGaAs/GaAs quantum well wafers. The basic structures of IPG and WPG nanowires are shown in Fig.1(a) and (b), respectively. The other type of the wire is a completely embedded InGaAs ridge nanowires of InGaAs/InAlAs heterostructure on an InP substrate, formed by selective MBE growth on InP patterned substrates using the above approach(4). The basic structure is shown in Fig.1(c). Device applications of these nanowire structures are also discussed.

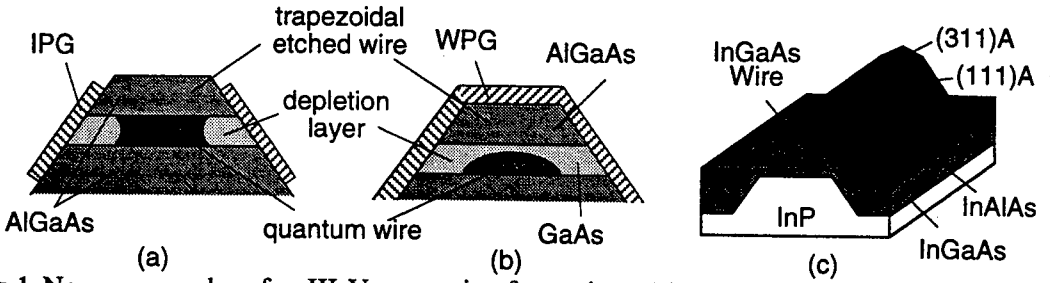


Fig.1 New approaches for III-V nanowire formation. (a) the cross-section of a novel Schottky in-plane gate (IPG) controlled GaAs wire, (b) the cross-section of a novel Schottky wrap gate (WPG) controlled GaAs wire and (c) a schematic view of an InGaAs nanowire embedded in InAlAs formed by selective molecular beam epitaxy (MBE) on an InP patterned substrate.

2. Gate Controlled GaAs Nanowires Using Novel Schottky Gates

To form Schottky IPG and WPG controlled wires[2-6] shown in Fig.1(a) and (b), basic trapezoidal wire structures having smooth side wall crystalline facets are formed by standard electron beam (EB) lithography and wet chemical etching on MBE grown AlGaAs/GaAs quantum well wafers. Then, Schottky gates are formed by EB lithography and metal deposition processes. It has been found that a novel in-situ pulsed electrochemical process[2] is particularly suitable to form damage-free Schottky IPGs with high Schottky barrier heights. Both IPG and WPG controlled nanowires have been characterized by plan view and cross-sectional SEM/AFM, electron beam induced currents (EBIC), conductance and magnetotransport measurements.

Both IPG and WPG gates provide excellent gate control with good pinch-off characteristics. Nanowires controlled by these gates have given marked non-linear Landau plots in SdH oscillation measurements, indicating that they act as high quality gate controlled one-dimensional electron waveguides with substantially increased subband spacing energy values of larger than 10 meV as compared with the traditional split gate III-V wires with subband spacings of a few meV or below. At low temperatures near pinch-off, both wires show clear quantization of conductance[2-4,6].

3. InGaAs Nanowires by Selective Molecular Beam Epitaxy

The completely embedded InGaAs ridge nanowires of InGaAs/InAlAs heterostructure shown in Fig.1(c) is formed by selective MBE growth on InP patterned substrates[7-11]. Such a selective epitaxy possesses the following advantages; sizes smaller than the lithography sizes can be realized by the self-organization mechanism in the crystal growth, sizes are independent of lithography size and its fluctuation, the interfaces are defect-free high quality heterointerfaces with steep and high potential barriers necessary for strong electron confinement, and the position of wires can be precisely controlled.

Arrays of nanowires oriented in the $<\bar{1}10>$[7-10] and <100>[11] directions, Y-branch couplers[12] and wire-dot coupled structures[13-15] have been successfully formed using the above technique. As an example, the growth sequence, and plan-view SEM and panchromatic CL images of high density InGaAs coupled wire-dot array are shown in Fig.2(a), (b) and (c), respectively. The dot size and the energy-distance profile of the potential barrier can be controlled by the initial pattern geometry and the growth conditions. So far, a minimum dot width of 30 nm, and a minimum lateral barrier width of 80 nm have been obtained. The present approach seems to be capable of realizing SET densities in the rage of 10^9-10^{10} cm^{-2} by further miniaturization of the pattern.

4. Device Applications

As shown in Fig.3, the nanowires reported here can serve as promising starting structures for various quantum devices such as quantum wire transistors (QWTrs) for logic and memory applications, coupled QWTrs for analog applications, and single electron transistors(SETs) for logic and memory applications.

IPG and WPG QWTrs have been fabricated and have shown excellent FET characteristics with good threshold voltage controllability[16]. Near pinch-off, they

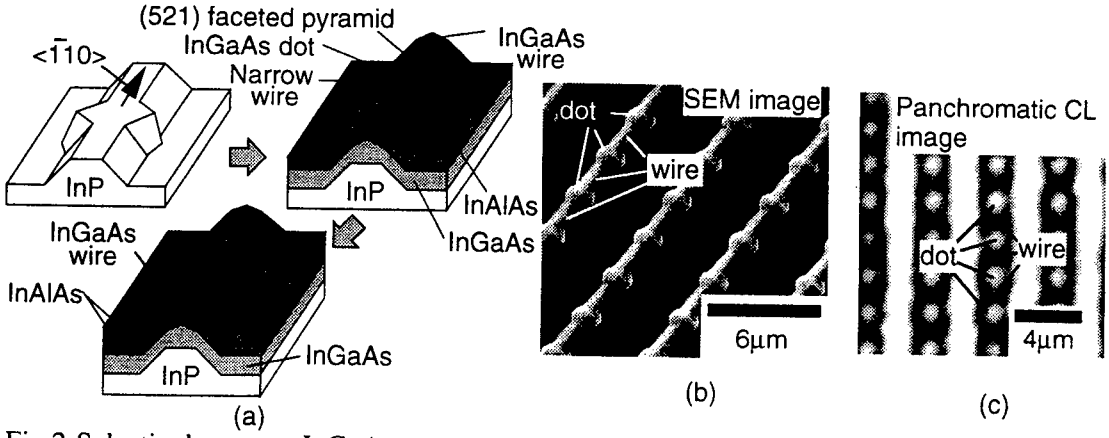


Fig.2 Selectively grown InGaAs quantum wire-dot coupled structure. (a) Selective growth sequence including initial substrate pattern, formation of a dot and wires with connecting narrower wires and coverage by top InAlAs layer, (b) plan-view SEM image and (c) CL image of the wire-dot coupled structure array.

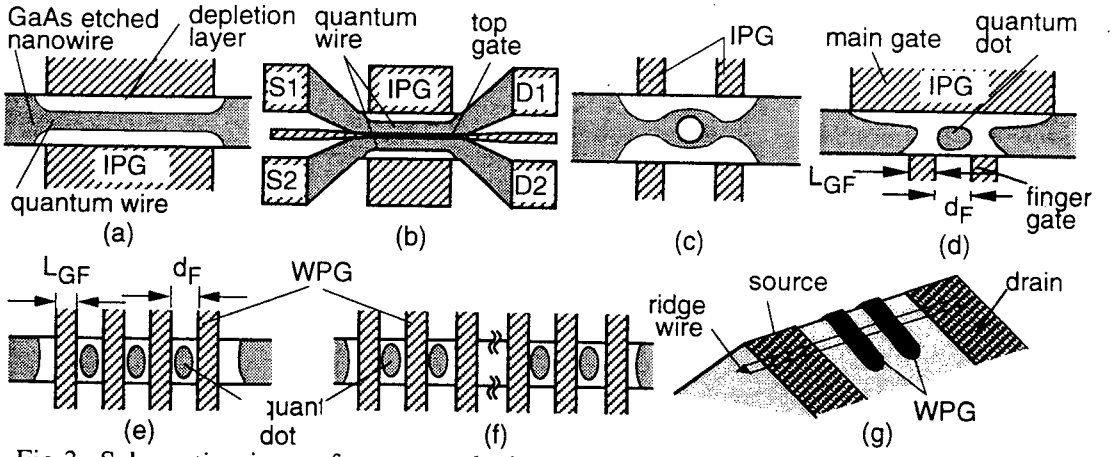


Fig.3 Schematic views of quantum devices realized by IPG and WPG nanowires. (a) quantum wire transistor(QWTr), (b) coupled QWTr, (c) Aharanov-Bohm effect device, (d) single-dot single electron transistor(SET), (e) triple-dot SET, (f) multiple-dot chain and (g) WPG SET using an embedded wire.

show conductance quantization. These devices can be operated near the quantum limit by switching between zeroth and first quantized conductance steps[16,17], making them attractive for low-power, high-speed logic and memory applications. The coupled IPG QWTrs have shown evidence for coupling of symmetric and anitsymmetric modes[6].

By using ultra-short and multiple Schottky IPG and WPG wires, SETs suitable for planar integration can be realized. IPG and WPG SETs have been fabricated and have shown clear conductance oscillation characteristics at low temperature up to 50K[18-23]. Conductance peaks have shown irregular voltage spacings and temperature-dependent peak heights, indicating presence of artificial atom-like quantum effects in the dot. Small voltage gains have been a problem in ULSI logic applications of SETs. In this connection, a novel three-WPG SET[20] shown in Fig.4(a) has recently realized a voltage gain above unity for the first time as the III-V SET. Combining a WPG SET with a WPG QWTr, a logic inverter has been successfully fabricated[24], as shown in Fig.4(b).

We believe that two different kinds of MBE-based III-V semiconductor nanowires and novel devices based on them, discussed in this paper, have excellent prospects for future quantum ULSIs in future nanoelectronics for logic and memory applications as well as sophisticated analog applications including quantum computation and information processing.

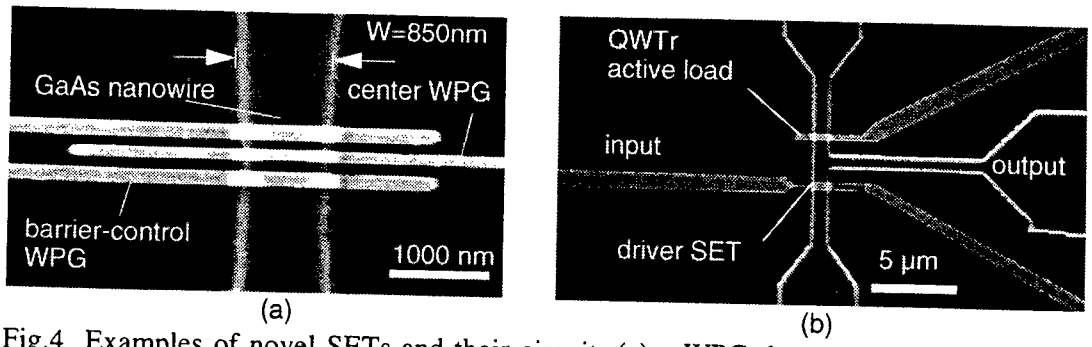


Fig.4 Examples of novel SETs and their circuits.(a) a WPG three-gate SET, (b) a logic inverter consisting of a WPG SET driver and a WPG QWTr active load.

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Silicon MOSFET Shrinking Limits: Quantitative Study

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Abstract—**We have performed numerical modeling of dual-gate two-dimensional ballistic *n*-MOSFETs with channel length of the order of 10 nm, including the effects of quantum tunneling along the channel and through the gate oxide. The results show that transistors with channel length as small as 8 nm (but larger than 6 nm) can exhibit either a transconductance up to 2,000 mS/mm or gate modulation of current by more than 8 orders of magnitude, depending on the gate oxide thickness. These characteristics make the devices satisfactory for logic and memory applications, respectively, though their gate threshold voltage is rather sensitive to nanometer-scale variations of the channel length.**

The prospects of silicon MOSFET scaling below 0.1 μm have received much attention in recent years - see, e.g., Ref. [1]. However, until recently the ultimate limits of scaling have not been well explored even theoretically. A simple analytical model for a dual-gate thin-channel field-effect transistor which allows such study has been proposed by our group [2]. The model used the fact that in MOSFETs with an undoped channel of 10-nm-scale length the electron-phonon scattering [3] and scattering due to Si/SiO_2 interface roughness are negligible, so that electron transport is essentially ballistic. Besides that assumption, the model used the well-known parabolic approximation [4,5] to reduce the system electrostatics to a 1D Poisson equation. The results obtained in this model have shown that ballistic MOSFETs with channel length down to 10 nm may retain almost all the performance of longer devices, while 5-nm devices show considerable degradation, but may still be useful for memory applications [2].

These results, however, have been questioned, since the parabolic approximation is only valid if the effective 1D screening length λ is much smaller than the screening scale λ_0 of free-standing 2D electron gas. However, concrete results discussed in Ref. [2] were calculated for such a set of parameters that λ and λ_0 were uncomfortably close (3.5 and 5 nm, respectively). In this work we have replaced the parabolic approximation with the numerical solution of the full (2D) Poisson equation which is valid for any λ/λ_0 ratio. In contrast to most works in this field, our Poisson solver (based on the conjugate gradient method [6]) treated the contacts and gate on an equal footing with the channel, thus taking full account of the electric field penetration into the source, drain, and gate electrodes. The mesh size necessary to describe this penetration accurately in our parameter range is about 0.1 nm; for 10-nm-scale devices, even such a dense mesh takes a low-end workstation CPU run time of only 3 seconds for a single iteration and below 1 minute for the full calculation for a single parameter set [7].

The analytical model used in Ref. [2] had another (apparently, more serious) problem. Following the tradition of earlier works on ballistic devices (see. e.g., Ref. [8]) it assumed "completely absorbing" boundary conditions on the channel-to-contact interfaces. In this assumption, the electrons arriving from the channel are absorbed in the source and drain, while those entering the channel are in thermal equilibrium with the corresponding contact. This is a good approximation, however, only if the number of electron states in the channel is much smaller than that in the source and drain, due to constraints in real and/or energy/momentum space [9]. There are no such constraints in the thin channel geometry considered in Ref. [2]. This is why in this work we have considered a slightly different model (Fig. 1) in which a thin undoped channel (of a thickness $t \ll L, \lambda$) is extended all the way between the bulk, n^+- doped electrodes. In this geometry, the electron energy quantization in the channel shifts up the conduction band edge. If this shift E_s is smaller than but close to the Fermi energy E_F of the degenerate electron gas in source and drain, the "completely absorbing" boundary conditions can be strictly justified [9]. (An additional suppression of the electron reflection back into the channel may be provided by small protrusions of the channel into the source and drain - see Fig. 1).

Finally, in contrast to Ref. [2], we have incorporated into our calculation scheme the quantum mechanical tunneling of electrons under the maximum of the electron potential profile in the channel (Fig. 2), within the framework of the usual quasiclassical (WKB) approximation with the parabolic dispersion law of tunneling electrons. (For silicon, the latter assumption is well justified even for electron energies of a few hundred meV below the conduction band edge, because of the large electron-to-hole mass ratio [10]). Gate oxide tunneling has been evaluated a posteriori, just as in Ref. [2].

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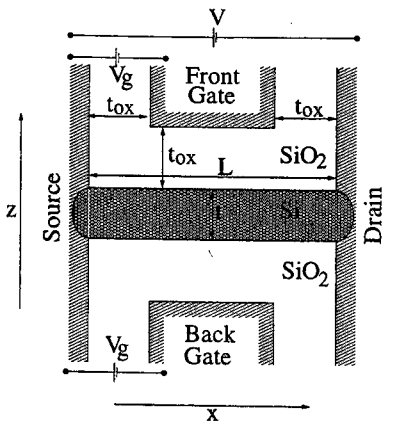


FIG. 1. The model of dual-gate MOSFET used here.

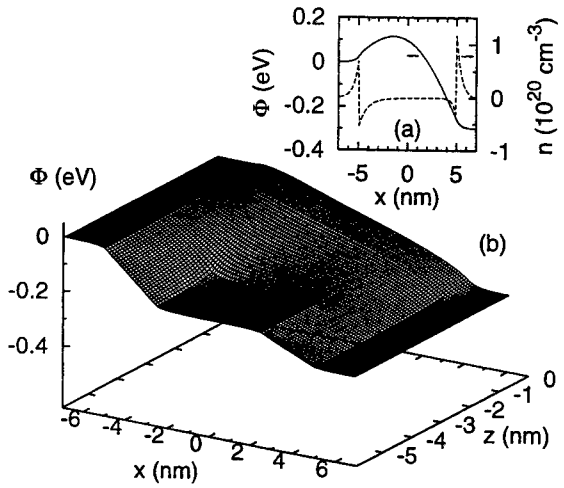


FIG. 2. (a) Electric potential and charge density distribution along the center of the channel for typical negative gate voltage ($V_g = -0.3$ V). (b) Electric potential distribution in lower half of the transistor for typical positive gate voltage ($V_g = 0.2$ V). In both panels $L = 10$ nm, $t_{ox} = 2.5$ nm, and $V = 0.3$ V.

In what follows we present results for silicon n-MOSFETs with a contact electron concentration N_D of 3×10^{20} cm^{-3} (the smallest concentration for which the statistical fluctuations of impurity positions have negligible effect on the device characteristics) and a channel thickness t of 2 nm. The latter parameter was chosen to be a little thicker than the typical width of silicon inversion layers (~ 1.5 nm), which exhibit high-field mobilities of the order of 200 cm^2/Vs, consistent with our assumption of negligible surface-roughness scattering. For these parameters, $E_s = 96$ meV, while $E_F = 150$ meV.

Figure 3 shows source-drain $I - V$ curves for devices with $t_{ox} = 1.5$ nm for two values of L. The curves show a well-expressed current saturation even at $L = 8$ nm. In these ultrasmall devices the saturation shows up only when the electron potential energy maximum in the channel is suppressed by positive gate voltage, and is due to the exhaustion of source electrons [11]. Current continues to grow slowly even in this saturated regime because of the finite voltage drop on the screening layer of the source.

Sub-threshold curves of transistors with $t_{ox} = 2.5$ nm are presented in Fig. 4. For the 12-nm device the curves have a nearly perfect log slope (indicated by the dashed line) and very small DIBL effect. However, the slope rapidly goes down and DIBL up as the length decreases below 10 nm. This loss is especially rapid at small currents (big negative gate voltages) due to electron tunneling under the narrower "bump" in the electric potential profile. Fig. 5 shows, on the same scale as Fig. 4, the thermal and tunneling currents separately, at V=0.3 V. As can be seen, the tunneling current dominates at small L and large negative gate voltage, and is responsible for the nonlinear shape of the semi-log plots shown in Fig. 4b.

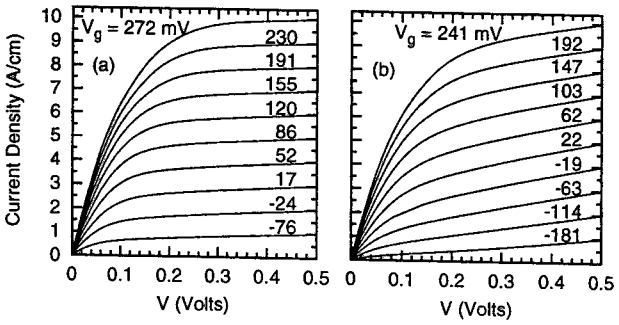


FIG. 3. Source-drain $I - V$ curves of transistors with (a) $L = 12$ nm and (b) $L = 8$ nm, for 10 values of gate voltage. Oxide thickness is $t_{ox} = 1.5$ nm.

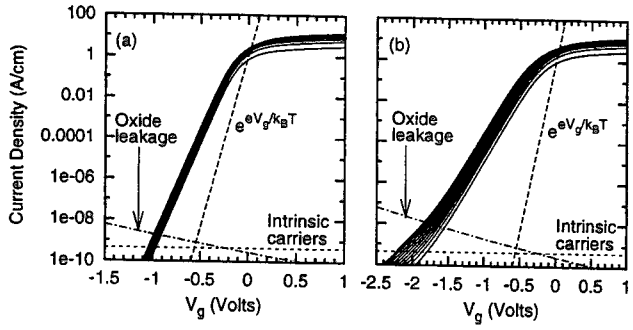


FIG. 4. Subthreshold curves for transistors with (a) $L = 12$ nm and (b) $L = 8$ nm for 10 values of source-drain voltage between $V = 0.03$ V and $V = 0.3$ V. Almost-vertical dashed lines denote the 60-mV-per-decade slope of an ideal transistor. Horizontal dashed lines represent the limit below which intrinsic carriers are not negligible. Dot-dashed lines show the current due to tunneling through the gate oxide.

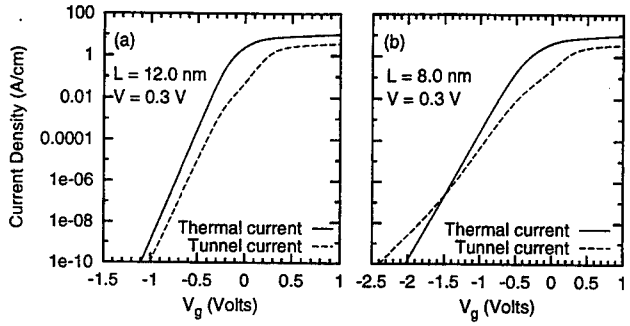


FIG. 5. Thermal and tunnel currents for the same parameters as in Fig. 4, at V=0.3 V.

The growth of DIBL with the channel length decrease may be characterized by the decrease of voltage gain $G_V = (dV/dV_g)_{I=\text{const}}$ shown in Fig. 6 as a function of V_g for devices with thinner gate oxide ($t_{ox} = 1.5$ nm) for several values of the channel lengths. In order to evaluate these results one should remember that the usual CMOS design tools imply $G_V \gg 1$, while devices with $G_V < 1$ cannot sustain logic circuits.

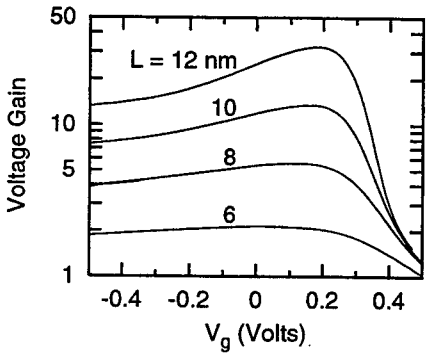


FIG. 6. Voltage gain as a function of gate voltage for various channel lengths. Here $t_{ox} = 1.5$ nm and $V = 0.3$ V.

The main conclusion which can be drawn from our results is that transistors with channels as short as 8 nm still seem quite suitable for digital applications, with proper choice of the gate oxide thickness. In fact, devices with a relatively thick oxide allow very high I_{on}/I_{off} ratio, above 8 orders of magnitude (Fig. 4b), making them suitable for memory applications including both DRAM and NOVORAM [12]. In contrast, transistors with thinner gate oxides (say, 1.5 nm) have a gate oxide tunneling too high for memory applications, but their transconductance and voltage gain (Figs. 3 and 6) are sufficient for logic circuits. Thus, the basic conclusions of our previous analysis [2] are generally confirmed, especially taking into account that the gate width of devices in our new model (Fig. 1) is by $2\times t_{ox}$ smaller than the channel length, making the 5-nm limit claimed in Ref. [2] crudely equivalent to our current 8-nm restriction. Our results are also compatible with those obtained in Ref. [13] for larger values of t.

The practical implementation of the remarkable MOSFET scaling opportunities requires several technological problems to be solved. First of all, the fabrication of dual-gate transistors requires rather advanced fabrication techniques - see, e.g. Ref. [14]. Second, the gate voltage threshold V_g of nanoscale transistors is rather sensitive to nanometer fluctuations of the channel length - see Fig. 7. Notice, however, that the *relative* sensitivity of V_g [which may be adequately characterized by the log-log plot slope $(L/V_g) \times dV_g/dL$] *decreases* at small L. This fact gives hope that with appropriate transistor geometry (for example, vertical structures where L is defined by layer thickness rather than by patterning - see, *e.g.*, Ref. [15]) the channel length fluctuations will eventually be made small enough for appreciable VLSI circuit yields.

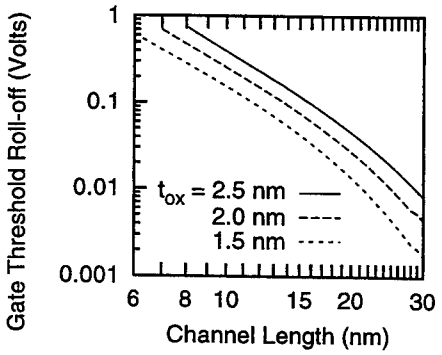


FIG. 7. Gate threshold roll-off (at current 10^{-4} A/cm) as a function of the channel length for three values of oxide thickness, for $V = 0.3$ V.

To summarize, we have performed numerical modeling of 10-nm-scale n-MOSFETs, taking into account both thermionic and tunneling currents. The results show that devices as short as 8 nm (but longer than 6 nm) can be optimized satisfactorily for both memory and logic applications.

Helpful discussions with D.J. Frank, S. Laux, M. Lundstrom, M. Fischetti, J. Palmer, Y. Taur, S. Tiwari, H.-S.P. Wong and especially P. M. Solomon are gratefully acknowledged. This work was supported in part by the AME program of DARPA via ONR.

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Characteristics of P-channel Si Nano-crystal Memory with Tunneling Oxide

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1. Introduction

The nano-crystal memory operates at low voltage compared to conventional Flash memory due to thinner tunneling dielectrics since the spacing between the Si dots suppresses the charge loss through lateral paths[1][2]. Recently, N-channel nano-crystal memory has been reported to have good characteristics compared to conventional EEPROM[1][2]. In this paper, the characteristics of the P-channel nano-crystal memory, which stores holes as the information, is presented.

2. Device Fabrication

The silicon nano-crystal memory has been fabricated at various dimensions by using 0.8μm-standard process. We used 4 nm thermal oxide as tunneling dielectrics for p-channel nano-crystal device. Fig.1 shows the schematic structure of the fabricated device. The silicon nano-crystals were formed through spontaneous decomposition and assembly during LPCVD. For oxide tunneling dielectrics, we could obtain a high dot density of about $5\times10^{11}/cm^2$ by using chemical treatment. After dot formation, 20nm control oxide was deposited. To implement p-channel device, the source and the drain were implanted with BF_2^+. N^+ polysilicon was used for the gate. Fig.2 shows the SEM image of cross section of nano-crystal memory. Si dots of about 4.5nm in diameter were obtained on tunneling oxide[1]. For comparison, devices without nano-crystal were also fabricated.

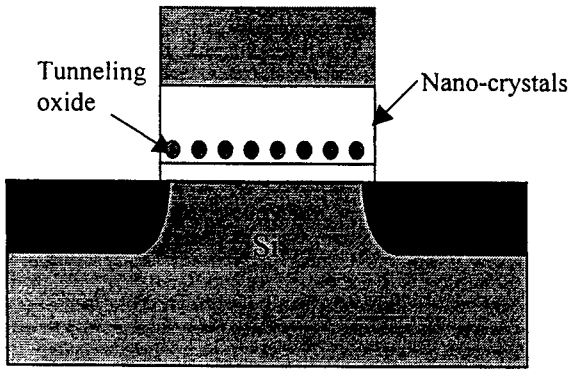


Fig.1. Schematic structure of nano crystal memory with tunneling oxide.

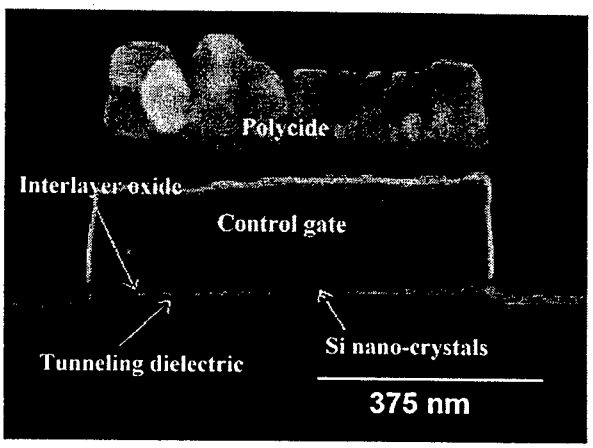


Fig. 2. SEM image of cross section of Si nano crystal memory.

And the programming and erasing was done through direct tunneling mechanism.

Fig.3 shows the energy band diagram when the gate

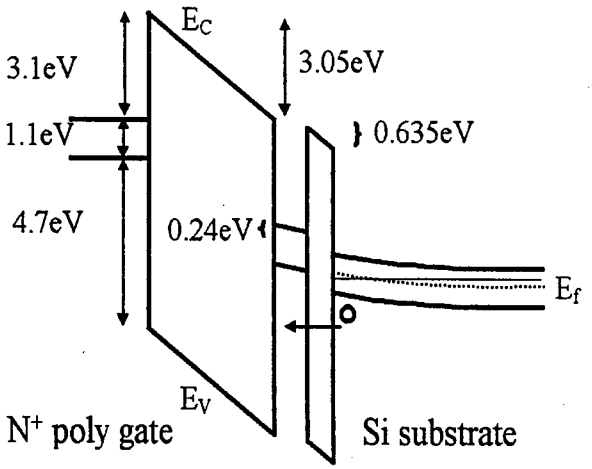


Fig. 3. Energy Band diagram during programming when the gate was biased to –5V. The substrate was doped with $N_A = 10^{17}/cm^3$ and the oxide charge was assumed to be equal to $1.6\times10^{-9}\,C/cm^2$

was biased to -5V. Since the nano-crystals are undoped, the number of free electrons in the conduction band of the nano-crystals is so small that the electron tunneling component is negligible. Only when the doping of the nano-crystals is larger than $3\times10^{18}/cm^3$, the electron tunneling component is significant. Therefore, the hole tunneling from the channel into the dots is the dominant mechanism for programming. The threshold voltage shift ΔV_T for one hole per Si dot is approximately given by the following equation [1][2]:

$$\Delta V_T = \frac{qn_{DOT}}{\varepsilon_{OX}}\left(t_{CG}+\frac{1}{2}\frac{\varepsilon_{OX}}{\varepsilon_{si}}t_{DOT}\right) \qquad (1)$$

,where t_{CG} is the control oxide thickness, n_{DOT} is the density of the Si dots, t_{DOT} is the dimension of a Si dot, ε's are permittivities, and q is the magnitude of electronic charge. From this equation, ΔV_T is calculated to be 0.48V when one hole tunnels into nano-crystal.

3. Electrical characteristics

Fig.4 shows the hysteresis characteristics of the memory devices with tunneling oxide. The fact that the drain current during the backward scan is smaller than that during forward scan indicates hole programming into Si dots. For maximum gate programming voltage of 8V in tunneling oxide, the threshold voltage shift was about 0.45V, which corresponds to nearly one hole per Si dots. Fig.4 also shows the feasibility of practical memory operation. The threshold voltage shift can be increased by larger programming voltage.

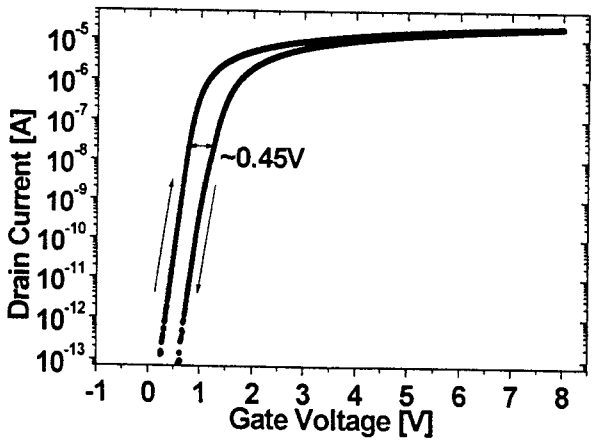


Fig. 4. Hysteresis characteristics of the memory. This figure shows holes tunnel into nano-crystals.

Fig.5 shows the threshold voltage shift versus program gate voltage. In the case of memory devices with nano-crystals, the threshold voltage shift increases with the program gate voltage. However, the threshold voltage shift was very small in the case of devices without dots as shown in Fig.5. This characteristic indicates that almost all the holes are programmed into the dots not into traps.

We also performed hot carrier programming to program

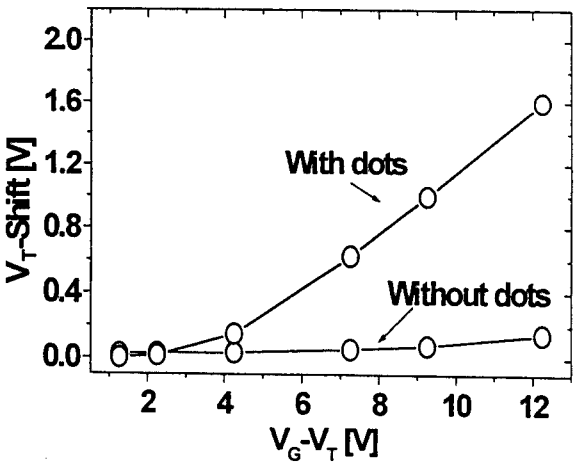


Fig. 5. Comparison of threshold voltage shift in device with dots and device without dots.

holes locally near the drain junction. Hot holes were injected near the drain junction during hot carrier

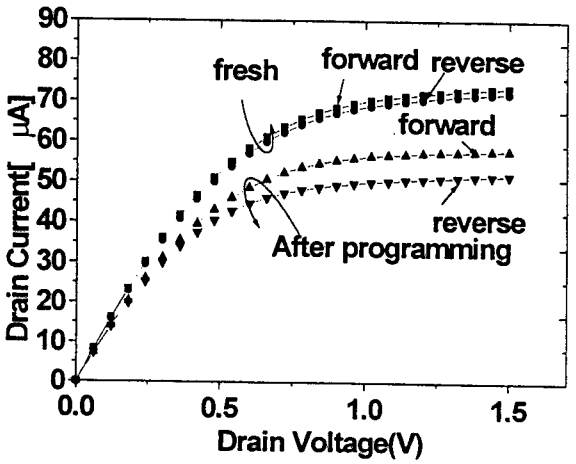
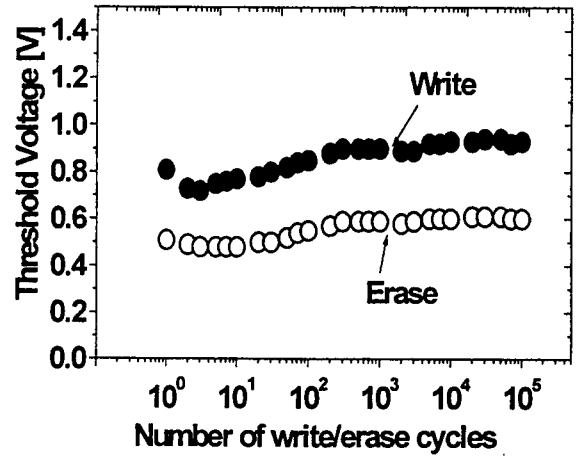


Fig. 6. Asymmetry of the I_D -V_D curve due to the localization of trapped hot carriers. The gate was biased to –3V and drain to –7V.

programming. Because of local programming of hot holes, the stressed IV curves measured after hot carrier programming have asymmetry as shown in Fig.6. The holes which trapped near drain junction did not spread into nano-crystal on the source junction side even after long time. Fig.7(a) shows the endurance characteristics of the devices. Pulse height of $\pm 5V$ and pulse duration of 10msec was used for writing and erasing. Until 10^5

write/erase cycles, write state and erase state still does not collapse. Fig.7(b) shows subthreshold slope does not change significantly until 10^5 write/erase cycles. From this, we can conclude significant interface trapping or



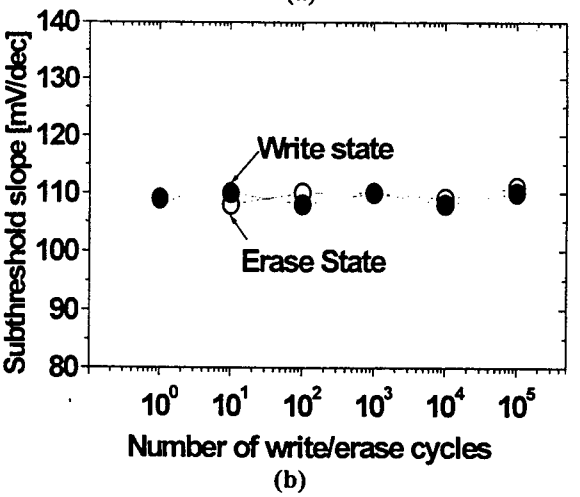


Fig. 7. (a) Endurance characteristics of the memory until 10^5 write/erase cycles. (b) subthreshold slope until 10^5 write/erase cycles.

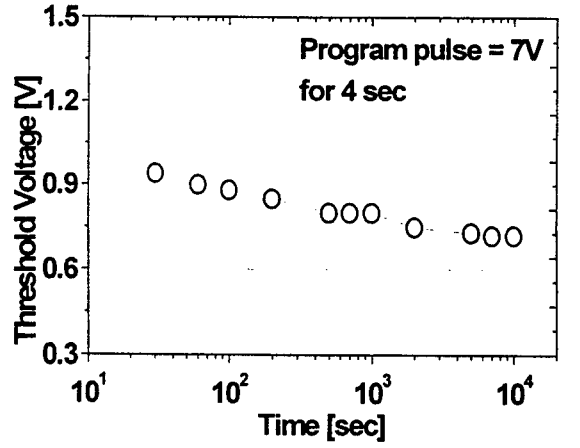


Fig. 8. Retention characteristics of the memory after gate 7 V programming up to 10^4sec

detrapping does not occurred under the endurance test. Fig.8 shows the measured retention characteristics for nano crystal memory. After holes were tunneled into nano-crystals by applying constant gate voltage of 7V for 4 second, the change of threshold voltage was measured up to 10^4s. To avoid additional programming during retention measurement, small gate readout voltage was applied. Although the tunneling dielectric is very thin, this good retention results from the spatial separation of nano-crystals.

4. Conclusion

In this work, we have shown that the holes in channel region tunnels into nano-crystals in p-channel nano-crystal memory, which increases threshold voltage. And we have shown that the p-channel nano crystal memory with tunneling oxide has the feasible practical characteristics in program, endurance, and retention characteristics.

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Two-Dimensional Quantum Simulation of Silicon MOSFETs

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Abstract

This paper presents fully two-dimensional (2D) quantum simulations of silicon MOSFETs. Starting from the 2D potential of the device, the 2D Schrödinger equation is solved in k-space and the 2D quantum electron concentration is computed. Comparisons with 1D Schrödinger solutions are shown for MOS capacitors and transistors, and 2D short-channel effects not evidenced by 1D solvers are presented.

Introduction

Deep sub-micron MOSFETs exhibit non negligible quantum effects [1, 2]. So far, these have been studied either through 1D models [3, 4] or (quasi-) 2D corrections [5, 6, 7], Fully 2D quantum calculations are thus necessary to validate these models and to perform more complete analysis. In this framework, we present a new code and numerical results regarding fully 2D quantum simulations of MOS structures.

Solution method

Simulations (see Fig. 1) start calculating the electrostatic potential $V(x,y)$ with a Drift-Diffusion code, and interpolating it on a uniform rectangular grid with dimensions L_x, L_y. The Schrödinger equation is discretized assuming that the solution is $\Phi_H = \sum_K A_K \phi_K = \sum_i^M \sum_j^N A_{ij}\phi_{ij}$, where $\phi_{ij}(x,y) = sin(k_i\ x)\ sin(k_j\ y)$ is the basis of the unperturbed Hilbert space, and $k_i = \pi\ i/L_x$, $k_j = \pi\ j/L_y$. The resulting system of equations is [8]:

$$\sum_{K=1}^{M\times N}\left[\left(V_{HK} + \frac{\hbar^2}{2m^*}\ (k_i^2 + k_j^2)\ \delta_{HK}\right) - \epsilon_H\ \delta_{HK}\right] A_K = 0 \qquad \forall H = 1,..(M\times N)$$

where A_K is the amplitude of the K^{th} component (ϕ_K) of the searched solution Φ_H relative to the H-th unknown eigenvalue ϵ_H, δ_{HK} is the Kronecker delta, $(M \times N)$ is the 2D discretization grid, and $V_{HK} = \langle\phi_H|V|\phi_K\rangle$ is the matrix element of the electrostatic potential in the k-space representation. The electron concentration is computed as:

$$n(x,y) = 2\sqrt{\frac{2kT}{\pi\hbar^2}}\sum_H m_H^* \mathcal{F}_{-1/2}\left(\frac{\epsilon_F(x,y) - \epsilon_H}{kT}\right)|\Phi_H(x,y)|^2$$

where $\epsilon_F(x,y)$ is the Fermi energy, m_H^* is the effective electron mass in the free direction for the H-th eigenvalue, and $\mathcal{F}_{-1/2}(\eta)$ is the Fermi integral of order -1/2. Representing $\Phi(x,y)$ in k-space allows us to reconstruct $n(x,y)$ on a finer mesh than that used to solve the Schrödinger equation, thus reducing memory requirements and avoiding inaccurate interpolations. $\mathcal{F}_{-1/2}(\eta)$ has been approximated as [9]:

$$\mathcal{F}_{-1/2}(\eta) = \left(e^{-\eta} + \sqrt{\frac{\pi}{2}}(\eta + b + (a + (|\eta - b|)^c)^{1/c})^{-1/2}\right)^{-1}$$

where $a = 6.68$, $b = 1.72$ and $c = 4.11$ were found with a best fit procedure yielding a residual error below 0.75 % (see Fig. 2).

Verifications.

The method was first checked by means of comparison with the analytical results for an electron inside a box. As show in Fig. 3, the values ϵ_H are apparently a function of the grid size. Actually, a coarser mesh leads to miss some eigenvalues, resulting in a distorted curve. In addition, the calculated eigenvalues fill rectangular contours in k-

space (see Fig. 4) that do not match the ellipsoidal equi-energy contours. Since the contribution of each eigenvalue to the total charge is a decreasing function of $\epsilon_H - \epsilon_F$, eigenvalues of small occupation probability can be accounted for at the expenses of others having a larger occupation probability. The resulting inaccuracy can be eliminated with a proper choice of the mesh size. As a second check we simulated a MOS capacitor. L_x and L_y were optimized to get a grid independent eigenvalue curve (see Fig. 5). The resulting node spacing is between 0.5 and 3 nm. The eigenvalues of the 2D solution are compared in Fig. 6 with those of an independent 1D solver. Eigenvalues are grouped into sub-bands and the bottom of each sub-band agrees well with the corresponding 1D eigenvalue. The 1D and 2D solution of this intrinsically 1D problem compare very well also in terms of electron density (Fig. 7) and charge vs. gate voltage characteristics (Fig. 8). These curves, however, are not suited for threshold voltage extraction since Schrödinger-Poisson self-consistency has not been implemented yet in our simulator. However, the non self-consistent 2D solution computed on the self-consistent 1D potential and the 1D self-consistent solution also coincide (compare $\diamond$ with $\times$ in Fig. 8).

MOSFET simulations

Fig. 9 shows the carrier concentration in the vertical direction across the source of a MOS transistor. As the grid size increases, a better approximation of the electron concentration is obtained, because a larger number of spectral components is available to reproduce the exponential behavior of each $\Phi_H(x,y)$ towards the bulk. As can be seen, the number of points adopted is large enough to correctly reproduce $n(x,y)$ over many orders of magnitude. Fig. 10 compares the 2D electron concentration with that of a 1D solver at the center of a 0.01 μm MOSFET similar to that of [10]. Due to relevant short-channel effects, the 1D and the 2D solutions differ even around the charge peak (see inset). Differences are observed also in the direction parallel to the interface, as shown in Fig. 11. In particular, due to wave-function penetration, the 2D solution shows a smoother transition between the source and the channel that raises the electron concentration inside the channel. Finally, we simulated a 0.04 μm MOSFET with ultra-shallow source/drain extensions, as those of [11]. Fig. 12 shows contours of $\Phi_H(x,y)$ corresponding to the two first degenerate eigenvalues giving the maximum contribution to $n(x,y)$ inside the extensions. The eigenvalues' energy is $\approx$ 20 meV above the bottom of the conduction band, thus suggesting the existence of non negligible quantization effects also inside the source/drain extensions, which may impact the access resistance of these devices.

Conclusions

In summary, a code for fully 2D quantum simulations of MOS devices has been developed. The k-space representation allows us to reconstruct the charge concentration on fine grids with reduced memory requirements with respect to real space solutions. The simulator was successfully checked against 1D solutions, and ultra-small geometry MOSFETs have been simulated, showing 2D quantum short-channel effects not evidenced by 1D simulations.

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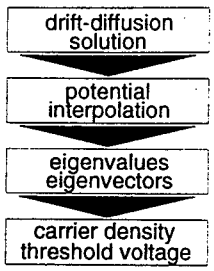


Figure 1: The flowchart of the simulation procedure.

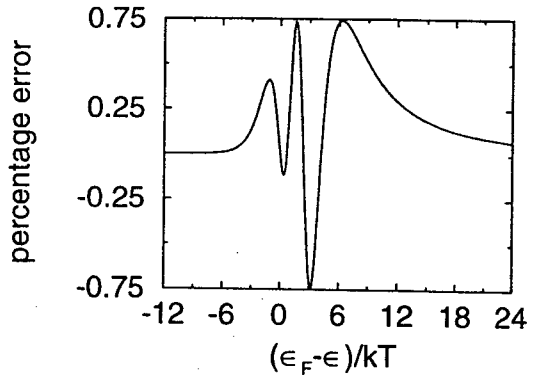


Figure 2: Percentage error of the approximated formula for the Fermi integral $\mathcal{F}_{-1/2}(\eta)$ with respect to an accurate numerical calculation.

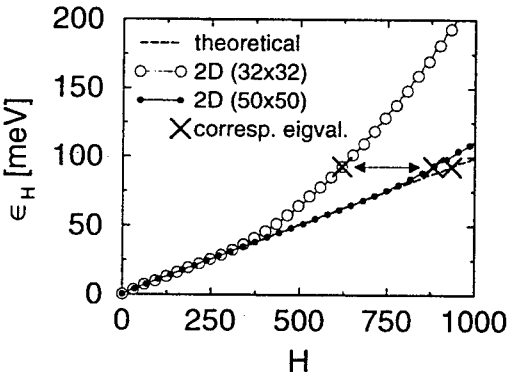


Figure 3: Eigenvalue energy as a function of eigenvalue index for a two-dimensional box. The eigenvalue energy is apparently a function of the k-space grid size (reported in the legend). Crosses mark eigenvalues that are quantitatively corresponding, but misplaced due to missing eigenvalues. L_x=0.12 μm, L_y=0.1 μm.

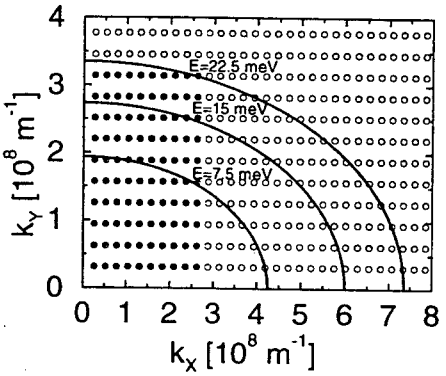


Figure 4: Open symbols: k-space representation of the theoretical eigenvalues of a 2D box featuring L_x=0.12 μm and L_y=0.1 μm. Filled symbols: typical distribution of the eigenvalues actually determined by the 2D algorithm. Solid lines: equi-energy contours of the ellipsoidal silicon energy band structure.

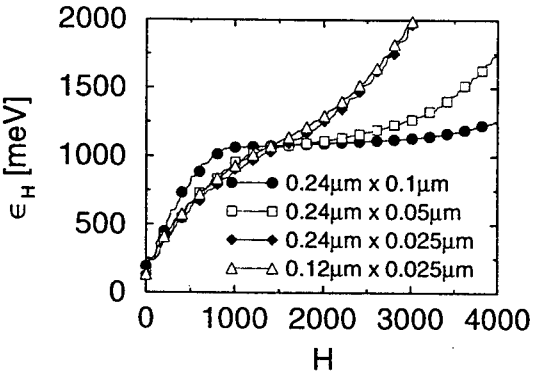


Figure 5: Eigenvalue energy as a function of eigenvalue index for different sizes ($L_x \times L_y$) of the 2D simulation domain of a MOS capacitor featuring V_G=1 V, t_{OX}=3 nm, N_{SUB}= 2x10^{18} cm^{-3}. The k-space grid size is 48x48.

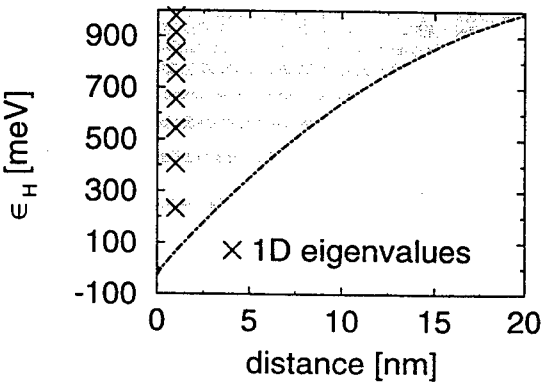


Figure 6: The sub-band of the 2D eigenvalues (solid lines) inside a MOS capacitor of length L_x=0.24 μm and those obtained solving the 1D Schrödinger equation on a section of the electrostatic potential profile (crosses). The large offset of the first sub-band is due to the light effective mass ($m^* = 0.19m_o$) in the vertical direction. Dot-dashed line: electrostatic potential. The finite width of each sub-band is determined by the finite number of grid points in the lateral dimension.

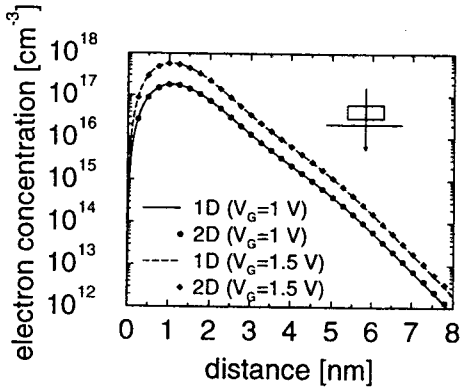


Figure 7: Comparison between 1D and 2D electron concentration computed at different V_G inside a MOS capacitor. L_x=0.12 μm, L_y=0.1 μm, t_{OX}=3 nm, N_{SUB}=2x10^{18} cm^{-3}. The k-space grid is 48x48. The concentration, instead, has been reconstructed in 200 points.

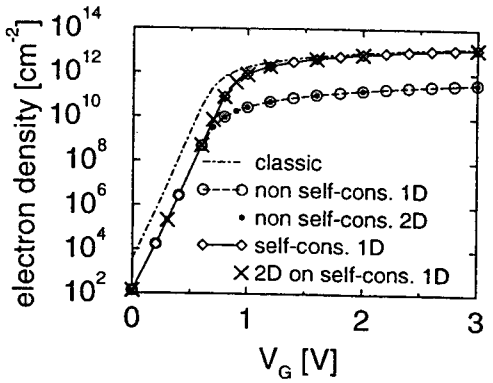


Figure 8: Charge sheet density as a function of gate voltage inside the MOS capacitor of Fig. 7. As expected, non self-consistent 1D (circles) and 2D (bullets) solutions coincide, but self-consistent 1D (diamonds) and non self-consistent 2D performed on the 1D self-consistent potential (crosses) also do.

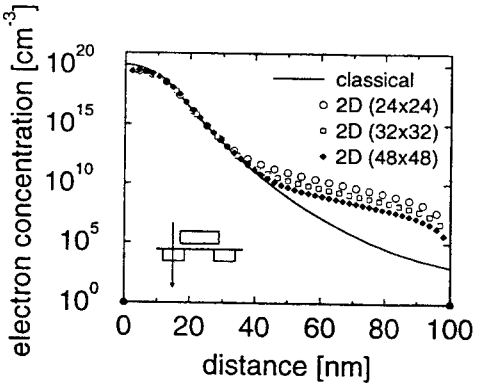


Figure 9: The classical electron concentration in a vertical section at the source of a MOSFET (solid line) is better approximated by the 2D quantum simulation as the number of discretization points is increased. The bias is $V_{GS} = 0V$, $V_{DS} = 0V$.

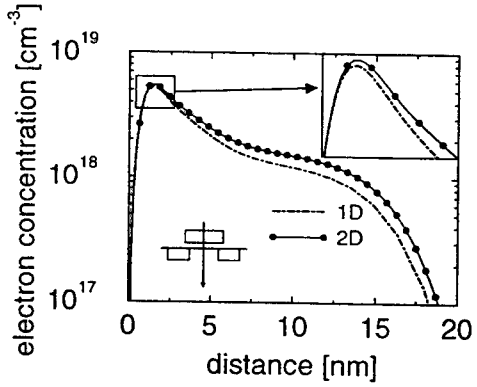


Figure 10: Electron concentration in the vertical direction of a 0.01 μm MOSFET. The section has been taken at the center of the channel. Dot-dashed line: 1D Schrödinger solution; symbols: 2D Schrödinger solution. The bias is $V_{GS} = 1.5V$, $V_{DS} = 0V$.

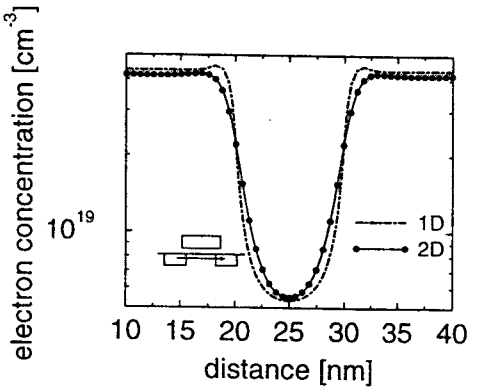


Figure 11: Electron concentration in the lateral direction of a 0.01 μm MOSFET. The depth of the section is 1.25 nm, namely that of the charge concentration peak. Dot-dashed line: 1D Schrödinger solution in the vertical direction; symbols: 2D Schrödinger solution. The bias is $V_{GS} = 1.5V$, $V_{DS} = 0V$.

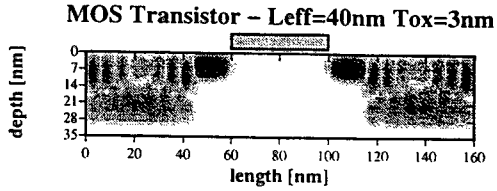


Figure 12: Contour plot of $|\Phi(x,y)|^2$ inside a MOSFET, similar to those of [11], with source and drain extensions. The depths of the deep and shallow portions of the source and drain regions are 30 and 10 nm, respectively.

Power Consumption in Single Electron Transistor Logic Circuits

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I. INTRODUCTION

Single-electron devices utilizing the Coulomb blockade of electron tunneling have attracted much attention in recent years. One of the most attractive applications of single-electron tunneling is for digital circuits with extremely high packing density and low power dissipation [1]. For the room temperature operation of a single electron transistor (SET) circuit is possible, Coulomb islands constituting the circuit should be made extremely small to provide large charging energy sufficient to overcome thermal agitation. As the dimension of a single-electron tunneling device is scaled down, both the current and voltage increase, thereby the power dissipated per device increases as a factor of square of device scaling factor [2]. Thus, in contrast to the MOS transistor, the power-delay product of single-electron device is proportional to the inverse of device feature size. This concludes that the power consumption of a SET circuit increases as the possible operation temperature increases.

In this paper, we present the results of a detailed analysis of the power consumption in SET logic circuits based on the behavior of a complementary capacitively coupled single-electron transistor (complementary C-SET) inverter. Possible means to reduce the power consumption are discussed.

II. POWER CONSUMPTION OF A COMPLEMENTARY C-SET INVERTER

Figure 1 shows the schematic of a complementary C-SET inverter circuit composed of an nMOS-like SET (nSET) and a pMOS-like SET (pSET) [3]. One SET unit is composed of two tunnel junctions with capacitances C_1 and C_2, tunnel resistances R_1 and R_2, gate capacitor C_g and control capacitor C_s. pSET and nSET are identical with the exception of the control voltages connected to the ground and V_{dd}, respectively. Also shown in Fig. 1 are the power consumption components in a SET inverter circuit. In general, there are three components that constitute the amount of power consumed in circuit operation: dynamic, short-circuit, and leakage power [4]. The dynamic power is consumed due to the charging and discharging of the output capacitance C_L when logic switching occurs. Dynamic power is inevitable in circuit operation. Short-circuit power occurs when both the nSET and pSET are simultaneously turned-on, conducting short-circuit current from supply to ground. An ideal complementary inverter does not dissipate power when the input does not change. However, in a complementary C-SET inverter leakage power is dissipated by the thermal enhancement of normal tunneling and cotunneling. At $T \neq 0$, thermally generated normal tunneling occurs even at the Coulomb blockade state and this results in leakage current during the absence of transients on the input. Cotunneling process is the simultaneous tunneling of multiple electrons across more than one tunnel junction and is a main factor contributing to leakage current at very low temperatures at which thermal fluctuation can be neglected. However, as the operation temperature is increased cotunneling rate is buried under thermally enhanced normal tunneling rate, thus almost all leakage current can be attributed to thermal agitation in this case [5].

The short-circuit power can be easily reduced in SET circuits. As mentioned earlier, the

short-circuit current occurred when both the nSET and pSET are simultaneously turned-on. Thus, if the transition regions of the two SETs can be made apart, the short-circuit current from supply to ground can be greatly reduced. Figure 2 shows the transfer curves of hysteretic / nonhysteretic inverters. With appropriate capacitance adjustment, the transient region of the transfer curves of pSET and nSET can be mismatched, thus, creating hysteretic characteristics without modifying the circuit configuration. This is possible in view of the fact that pSET and nSET are physically identical devices. Thus, if the capacitance adjustment makes the transition region of one SET shift to the left in the transfer curve of a SET inverter circuit, the transition region of the other SET shifts to the right. This can be easily understood from the fact that the "turn on" gate voltage of pSET and nSET are given by $[-e/2 + (C_g + C_s + C_1) V_{dd}] / C_g$ and $[e/2 - (C_s + C_1) V_{dd}] / C_g$, respectively. The use of a hysteretic inverter also helps the reduction of leakage current resulting from the thermal agitation, since the conductance minima of two SETs of the hysteretic inverter are more close to 0 for the nSET and V_{dd} for the pSET in the gate voltage axis than the nonhysteretic inverter. No short-circuit current at zero temperature, and reduced current is achieved by using the hysteretic inverter.

The power consumption in a SET inverter as described is analyzed using the Monte Carlo method. For the SETs used in the analysis, the capacitances are scaled with respect to the tunnel capacitance C_2 as: $C_1 = 2\ C_2$, $C_g = 7\ C_2$, $C_s = 6\ C_2$. All the tunnel resistances are set to a constant value $R = 1$ MΩ. The supply voltage V_{dd} is given as $V_{dd} = 1.33\ e / 2\ C_{tot}$, where C_{tot} is the total capacitance of a SET, i. e., $C_{tot} = C_1 + C_2 + C_g + C_s$. The output capacitance is set to a value $C_L = 360\ C_2$, and thus fifteen electrons are needed for full logic swing from the fact that $n\ e = C_L\ V_{dd}$, where n is the number of electrons participating the switching. With given capacitance values, the inverter under consideration operates as a hysteretic inverter, and the short-circuit power is neglected in the simulation.

Figure 3 shows the power consumption of a SET inverter versus clock frequency for different values of operation temperature. The dotted line shows the ideal power consumption, i. e., the dynamic power consumption $C_L V_{dd} V_s f_{clk}$, where f_{clk} is the clock frequency and V_s is the output voltage swing. The simulated power at zero temperature matches well in high clock frequency region, however, cotunneling induced dissipation appears as the increase of power in low frequency region. As the operation temperature rises, leakage current resulting from the thermally generated normal tunneling increases and the leakage power becomes significant. The declination of the slope above the clock frequency 1 GHz indicates that the circuit cannot catch up the clock speed, thereby the level of signal swing V_s is substantially lower than the supply voltage V_{dd}. The power-delay product is the energy dissipated in each switching event, i. e., P / f_{clk}. Figure 4 shows the power-delay product of C-SET inverter as the feature size of a SET varies. The lines with symbols show the total power-delay product while the dotted lines show the switching component. In case of ideal CMOS circuits where the leakage power is not significant, the power-delay product does not depend on clock frequency. However, in SET circuits, the leakage power consumption due to the thermally enhanced normal tunneling and cotunneling prevails and thus the power-delay product varies inversely as the clock frequency increases in the low clock frequency region. It can be easily seen in the figure that, as the dimensions of the devices are decreased by a factor of K, the power-delay product and the operation speed of a SET circuit increase by a factor of K.

III. TERNARY CIRCUITS

For the reduction of the relatively large power consumption in SET circuits, some novel circuit design methods should be utilized. Most of all, the number of transistors constituting the circuit should be minimized. For this purpose, multiple valued logic schemes are useful. The central region in the transfer curve of the hysteretic inverter (see Fig. 2) where both the pSET and nSET are turned off could be utilized in the design of ternary circuits. Figure 5 shows two CMOS-type dynamic unary gates, one operating as a positive ternary inverter (PTI) and the other as a negative ternary inverter (NTI) as defined in [6]. The logic levels are

defined as '2' = V_{dd}, '1' = V_{dd}/ 2, and '0' = *gnd*. The operation principles are identical to their CMOS counterparts, *i. e.*, when the clock ϕ is V_{dd}, the output is preset to V_{dd} for PTI and zero for NTI, and When ϕ is zero, logic operations, as indicated in the figure, are performed. For the realization of any ternary function, an additional unary gate known as a simple ternary inverter (STI) is required. The design of the STI is straightforward by using the pull-up circuit of the NTI, the pull-down circuit of the PTI, and a transmission gate connected to an output terminal and V_{dd}/2. Other ternary gates and circuits can be easily designed with the use of hysteretic inverter characteristics.

Figure 6 shows the switching characteristics of designed PTI and NTI. Inputs and outputs are normalized with V_{dd}. For the extension of the noise margin of logic level "1", the tunnel capacitance C_1 is reduced to $C_1 = C_2$. The supply voltage V_{dd} is given as $V_{dd} = 1.25\ e / 2\ C_{tot}$ and the output capacitance is set to a value of $C_L = 384\ C_2$, and thus sixteen electrons are needed for full logic swing. With given capacitance values, the "both-off" region lies in (0.5 ± 0.22) V_{dd} in the transfer curve. The switching characteristics shown in this figure clearly indicate that each of these circuits properly function as a PTI and NTI. However, large discrepancy between rising / falling times is observed. This problem is due to the serial connections of SETs and can be solved by means of multi-gate SET configurations, in which the serial connection is replaced by an additional input terminal [7]. Thus, in real circuit design multi-gate SET optimizations should be followed to further minimize circuits and to improve circuit performance.

IV. CONCLUSIONS

Numerical analysis on the power consumption of complementary C-SET logic has been performed based on the behavior of an inverter circuit. It has been shown that the leakage power due to the thermal enhancement of normal tunneling occupies considerable portion of total power consumption as the operation temperature grows up. A SET inverter circuit that has a hysteretic transfer characteristic has been presented for the reduction of short-circuit and leakage power. By utilizing hysteretic inverter characteristics, basic ternary logic gates have been designed and verified with the Monte Carlo method. These considerations prove some room for relaxing the power consumption problem of the SET circuits.

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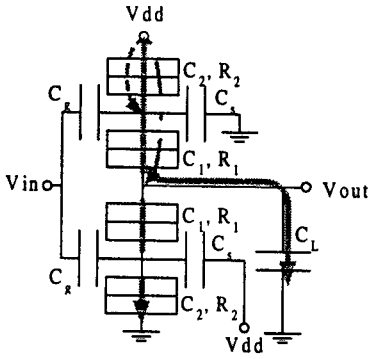


Fig. 1 Schematic of a complementary C-SET inverter and power consumption processes. ---: thermally enhanced normal tunneling, —·— : cotunneling, ——: dynamic current, and —— : short-circuit current.

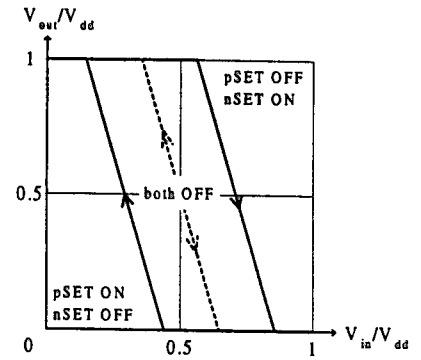


Fig. 2 Transfer curves of hysteretic (——) / nonhysteretic (·····) inverters.

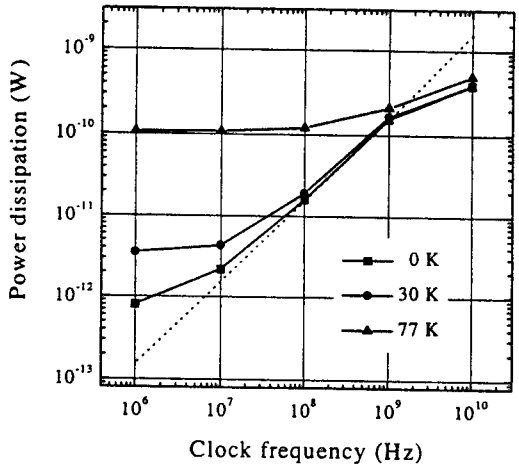


Fig. 3 Power consumption versus clock frequency of a SET inverter circuit. $C_2 = 0.1$ aF.

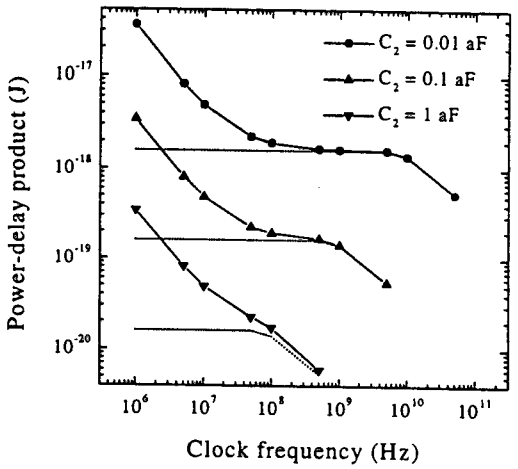


Fig. 4 Power-delay product of a C-SET inverter. The dotted curves show the switching component of the total power dissipation. $T = 300$, 30, and 3 K (from top to down).

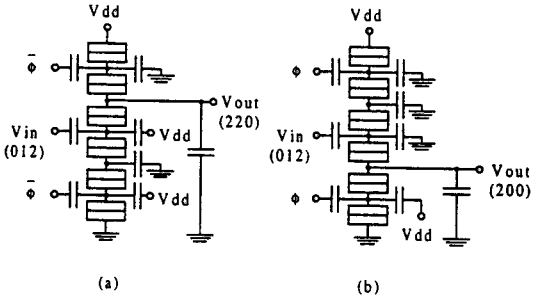


Fig. 5 Schematics of SET dynamic unary gates, (a) positive ternary inverter, (b) negative ternary inverter.

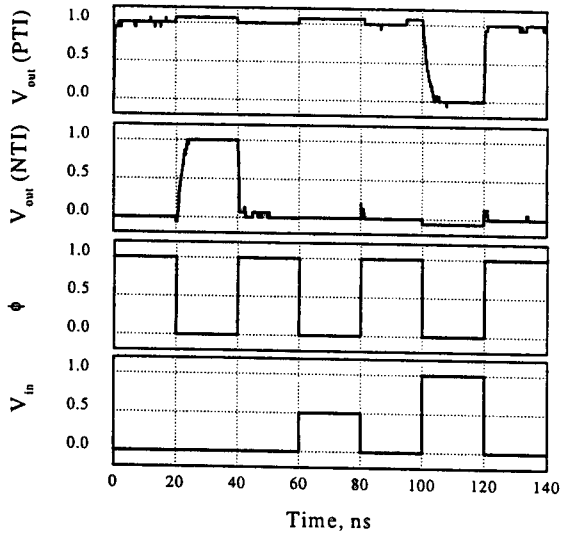


Fig. 6 Switching characteristics of NTI and PTI. $C_2 = 0.1$ aF, $T = 10$ K.

Channel Thermal Noise Extraction and Model Verification of MOSFETs

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ABSTRACT

An extraction method to obtain the channel thermal noise (i_d^2) of MOSFETs directly from the d.c., a.c. and RF noise measurements is presented. It shows that the induced gate noise and its correlation with the channel thermal noise are negligible for frequencies up to 18GHz and the equations $8kTg_m/3$, $8kTg_{do}/3$ and $8kT(g_m+g_{ds})/3$ for calculating i_d^2 are not valid for sub-micron MOSFETs biased in the saturation region. High-frequency noise performance of MOSFETs became an important issue after the high unity-gain frequency (f_T) had been achieved (fig. 1). Therefore, an accurate noise model for the channel thermal noise in MOSFETs is crucial for low-noise CMOS RF circuits.

INTRODUCTION

This paper presents an extraction method to obtain the channel thermal noise directly from the d.c., a.c. and RF noise measurements. Based on measured *s*-parameters, the simulation of noise parameters shows that the induced gate noise and its correlation with the channel thermal noise discussed in [1] are negligible in the noise modeling of MOSFETs for frequencies up to 18GHz. In addition, the equations $8kTg_m/3$, $8kTg_{do}/3$ and $8kT(g_m+g_{ds})/3$ for calculating the power spectral density of the channel thermal noise are not valid for the noise prediction of sub-micron MOSFETs, especially for the devices biased in the saturation region.

Currently, the measured minimum noise figure (NF_{min}) of devices is often used to confirm the noise model built from a suitable a.c. model of the transistor. However, the accuracy of the small-signal model and of values of the extracted model elements used in noise calculations are not easily obtained. In addition, there is still much on-going research on how to accurately calculate the channel thermal noise of MOSFETs. Therefore, obtaining the channel thermal noise of MOSFETs directly from RF noise measurements is crucial in noise modeling. The method presented in this paper can get rid of the influence of the inaccuracy of the small-signal model from the characterization of the channel thermal noise in MOSFETs.

THEORY OF EXTRACTION

A noisy two-port may be represented by a noise-free two-port and two current noise sources as shown in fig. 2 (a), and these two noise sources are usually correlated with each other. From the *y*-parameters of the two-port and the noise source information (i_1, i_2 and the their correlation term), we may evaluate the noise parameters of the two-port by transforming the noisy two-port to a noise-free two-port with a noise current and a noise voltage source at the input side of the two-port (fig. 2(b)). Fig. 3 shows the complete equivalent noise circuit model for an intrinsic MOSFET operated in the GigaHertz region. However, at low frequency, the equivalent noise circuit model can be simplified (shown in fig. 4) and the power spectral density of the noise current source i_2 defined in fig. 2 (a) can be obtained from

$$\frac{\overline{|i_2|^2}}{\Delta f} = \overline{|u|^2} \cdot |Y_{21}|^2 = 4kTR_n \cdot |Y_{21}|^2 = \frac{\overline{|i_{Gout}|^2}}{\Delta f} + \frac{\overline{|i_{Sout}|^2}}{\Delta f} + \frac{\overline{|i_{Dout}|^2}}{\Delta f} + \frac{\overline{|i_{dout}|^2}}{\Delta f} \quad (1)$$

where i_{Gout}, i_{Sout}, i_{Dout} and i_{dout} are the noise currents contributed at the output port by gate resistance (R_G), source and drain resistances (R_S and R_D), and the channel thermal noise (i_d), respectively. By calculating the noise contribution from each noise source analytically and substituting i_{Gout}, i_{Sout}, i_{Dout} and i_{dout} in eqn. (1), the power spectral density of the channel thermal noise in MOSFETs can be extracted from

$$\overline{|i_d|^2} = 4kT \cdot \left[(R_{no} - R_G - R_S) g_m^2 - \frac{2g_m R_S}{R_{DS}} - \frac{R_D + R_S}{R_{DS}^2} \right] \quad (2)$$

where R_{no} is the equivalent noise resistance extrapolated at DC or measured at low frequencies.

EXPERIMENTAL RESULTS

The device-under-test (DUT) is a 0.36μm n-type MOSFET with ten 12μm wide devices connected in parallel and fabricated in a 0.25μm CMOS technology by Conexant. By using the parameter extraction method described in [2], $R_G \sim 9.5\Omega$, $R_S = R_D \sim 1\Omega$, and $R_{db} \sim 11.5\Omega$. Figs. 5 to 7 show the selected parameter values as a function of bias condition and figs. 8 to 11 show the measured and simulated y-parameters for the DUT biased at I_{DS} = 3.1mA. By using these extracted values and eqn. (2), the calculated channel thermal noise i_d^2 is 3.2×10^{-22}Amp^2/Hz. Figs. 12 to 15 show the measured and simulated noise parameters as a function of frequency by using the measured y-parameters without including the induced gate noise (i_g^2 in fig. 3) and its correlation with the channel thermal noise (dash lines are based on eqn. $8kTg_m/3$ which underestimates NF_{min} and r_n, and solid lines are based on the extracted value of i_d^2 (3.2×10^{-22} Amp^2/Hz). Fig. 16 shows the extracted and calculated channel thermal noise vs. bias current characteristics. It shows that the calculated channel thermal noise based on the equation $8kTg_m/3$, $8kTg_{do}/3$ or $8kT(g_m + g_{ds})/3$ cannot model the channel thermal noise of MOSFETs biased in the saturation region.

CONCLUSIONS

In conclusion, a direct extraction method of the channel thermal noise in MOSFETs has been presented and verified. This technique removed the influence of inaccurate a.c. parameter fitting from characterizing the channel thermal noise of MOSFETs. The physics-based models can then be developed and compared to the experimental results in a direct way. Very good agreement between the simulated and measured noise data has been achieved without including the induced gate noise and its correlation with the channel thermal noise.

ACKNOWLEDGEMENT

It is a great pleasure to acknowledge C. Enz and M. Schroter of Conexant Systems Inc., Ca, and D. R. Pehlke of Rockwell Science Center, Ca, for their assistance and advice in this work.

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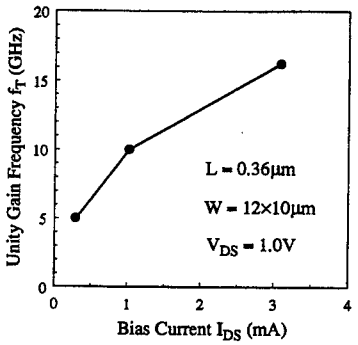


Fig. 1: Unity gain frequency vs. bias current characteristics.

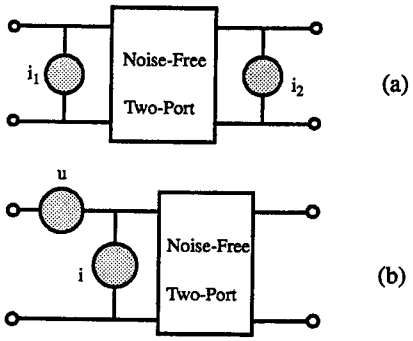


Fig. 2: Different representations of noisy two-port networks.

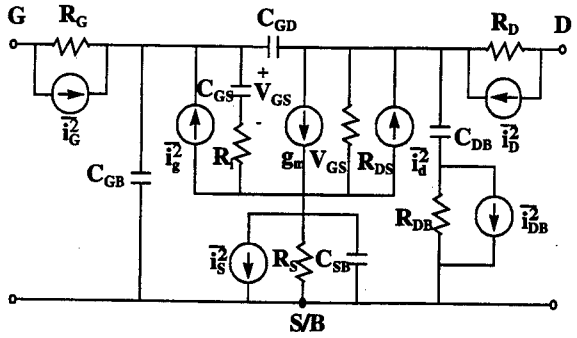


Fig. 3: Equivalent noise circuit model for an intrinsic MOSFET

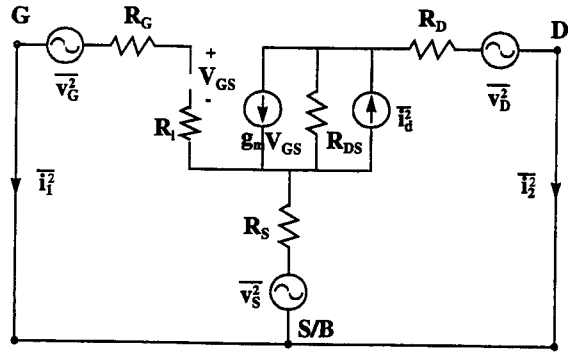


Fig. 4: Simplified equivalent noise model at DC or lower frequency.

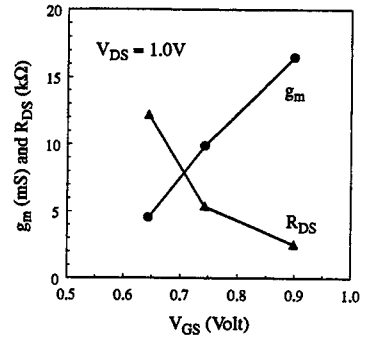


Fig. 5: Extracted g_m and R_{DS} vs. V_{GS} characteristics of a n-type MOSFET with L= 0.36μm, W = 12×10μm.

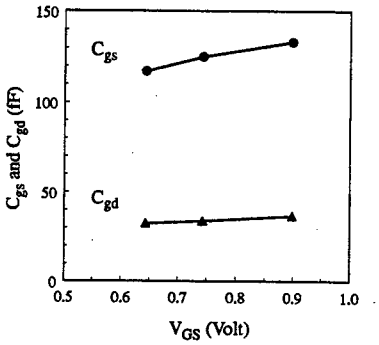


Fig. 6: Extracted C_{gs} and C_{gd} vs. V_{GS} characteristics of a n-type MOSFET with L= 0.36μm, W = 12×10μm.

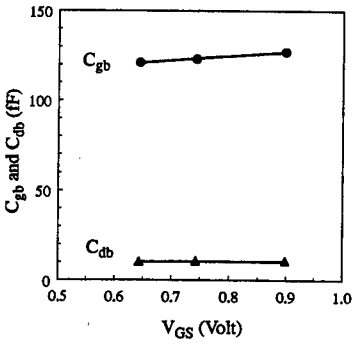


Fig. 7: Extracted C_{gb} and C_{db} vs. V_{GS} characteristics of a n-type MOSFET with L= 0.36μm, W = 12×10μm.

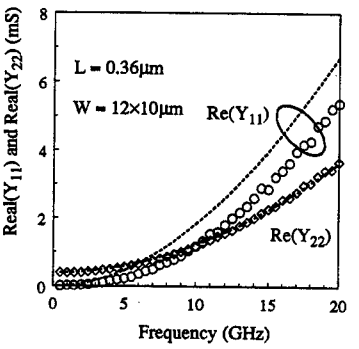


Fig. 8: Measured and simulated real part of Y_{11} and Y_{22} at V_{DS} = 1.0V, I_{DS} = 3.09mA.

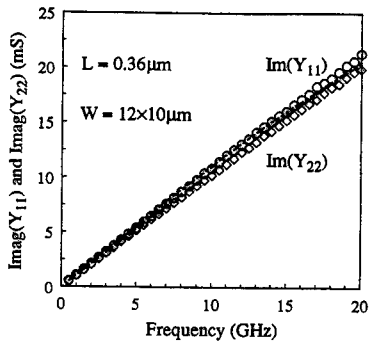


Fig. 1: Measured and simulated imaginary part of Y_{11} and Y_{22} at V_{DS} = 1.0V, I_{DS} = 3.09mA.

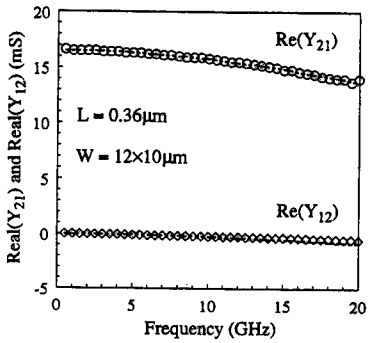


Fig. 2: Measured and simulated real part of Y_{21} and Y_{12} at V_{DS} = 1.0V, I_{DS} = 3.09mA.

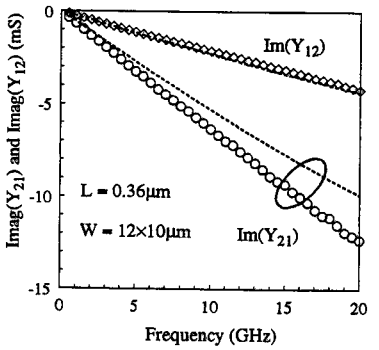


Fig. 3: Measured and simulated imaginary part of Y_{21} and Y_{12} at V_{DS} = 1.0V, I_{DS} = 3.09mA.

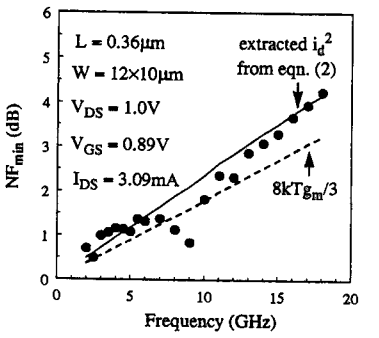


Fig. 4: Measured and simulated NF_{min} vs. frequency characteristics of a 0.36 μm n-type MOSFET.

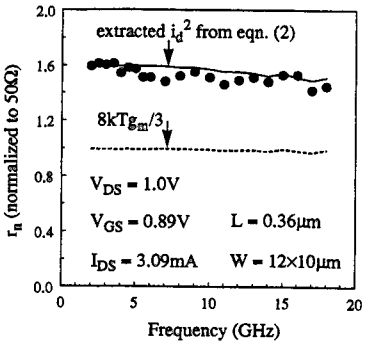


Fig. 5: Measured and simulated equivalent noise resistance vs. frequency characteristics of a n-type MOSFET.

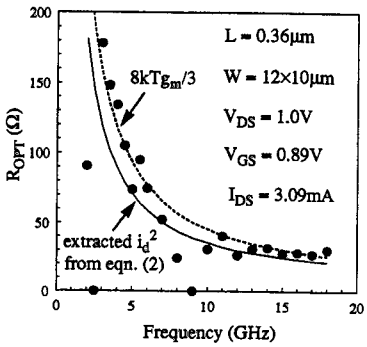


Fig. 6: Measured and simulated optimize source resistance vs. frequency characteristics of a n-type MOSFET.

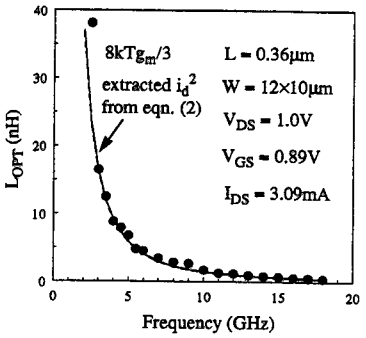


Fig. 7: Measured and simulated optimized source inductance vs. frequency characteristics.

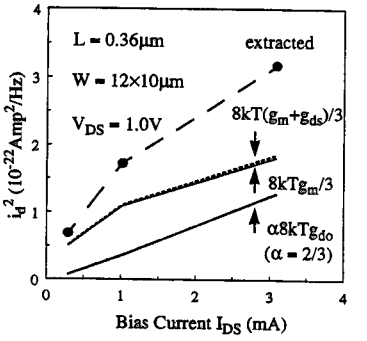


Fig. 8: Measured and calculated power spectral density of channel thermal noise vs. bias current.

The Effects of Radiation on Gate-Induced-Drain-Leakage (GIDL) For SOI and Bulk MOSFETs

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Abstract

The effect of ionizing radiation on Gate-Induced-Drain-Leakage (GIDL) current for radiation-hard SOI and non-radiation-hard bulk MOSFETs has been investigated. It is shown that GIDL current increases with radiation exposure for n-channel SOI and bulk MOSFETs. The radiation-induced increase in GIDL current for SOI devices is mainly due to charge trapping induced flat-band voltage shifts; whereas, for bulk devices it is due to both charge trapping induced flat-band voltage shifts as well as interface state assisted tunneling.

Introduction

The reduction, or minimization, of off-state currents in high-density and low-power CMOS technologies is an important issue in the scaling of VLSI technologies. One type of leakage current for thin gate oxides is GIDL current. Band-to-band tunneling in the gate-drain overlap region causes this leakage current. It has been shown that GIDL current changes after hot-carrier stressing on SOI structures [1], and that SOI floating body effects can amplify GIDL current [2]. In this work we demonstrate the effect 10-keV x-rays have on GIDL currents on radiation-hard SOI technology, and make comparisons to a radiation-soft bulk technology.

Experimental Details

Two types of radiation hard SOI technologies are evaluated in this investigation, a 0.5μm and a 0.35μm technology. Both were fabricated using a SIMOX thick buried oxide substrate, and device fabrication was on partially depleted silicon films. Both technologies were designed for V_{dd}=3.3V operation. The 0.5μm technology had a gate-oxide thickness of 15nm and the 0.35μm technology had a gate-oxide thickness of 10nm. For comparison a non-hardened bulk 0.65μm technology was also investigated. The bulk 0.65μm technology had a gate-oxide thickness of 14nm and operated with V_{dd}=5V. Both the SOI and bulk technologies used LDD designs.

Standard current vs. voltage (IV) techniques were used to obtain the SOI transistor threshold voltages (Vt) for the front- and back-gate transistor. The GIDL measurement was obtained by measuring the drain current (Id) vs. drain voltage (Vd) at a large negative gate voltage (Vg= -8V) for n-channel MOSFETs. The large negative gate

voltage, in addition to the applied drain voltage, is needed to activate the GIDL tunneling current. In this work, the GIDL current was obtained by an over-stressing condition, typically beyond the normal operating range. To avoid radiation induced transistor edge leakage currents, the source lead was disconnected, or floating, during the GIDL measurement while the body lead was grounded. In addition, long channel transistors were evaluated to avoid short channel effects such as drain-induced-barrier-lowering (DIBL) effects.

An ARACOR 10-keV x-ray radiation source was used for wafer level irradiations. All device irradiations and measurements were done via a probecard, and all activities were done at room temperature. The structures were irradiated with gate-high bias conditions, i.e. Vg=3.3V for SOI devices and Vg=5V for bulk devices, and all other leads grounded. All measurements were made immediately after the irradiations.

Discussion

The radiation induced voltage shift of the isolation-oxide for both the 0.35μm SOI and the 0.65μm bulk structures are shown in Fig. 1. The threshold voltage for the SOI back-channel transistor is above 8V for a x-ray dose of 6Mrad(SiO_2), and the front-gate transistor is still functional. This SOI back-gate response demonstrates the radiation-

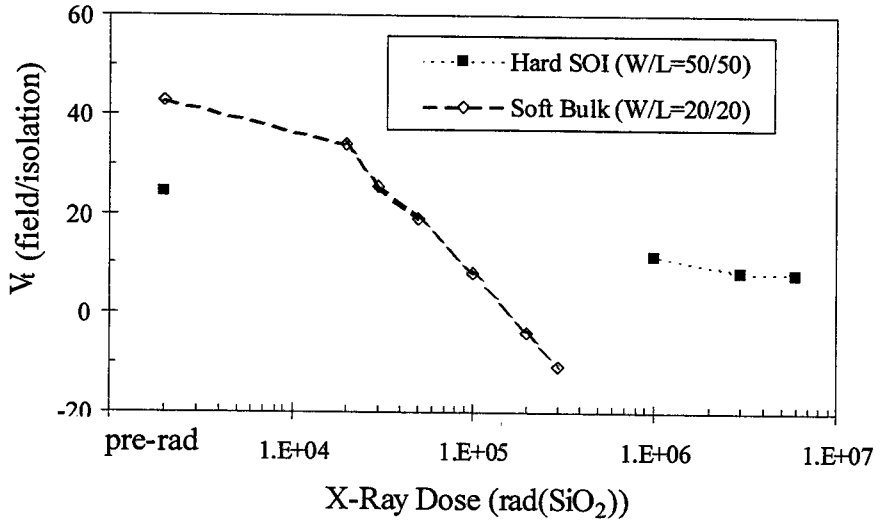


Figure 1. The radiation induced voltage shifts of the isolation-oxide for both the 0.35 μm SOI and the 0.65μm bulk structures are shown in Fig. 1. The radiation bias conditions were Vg= 3.3V for SOI and Vg= 5V for bulk, all other leads were grounded.

hard level of the 0.35μm SOI technology evaluated here. As for the bulk 0.65μm technology, the threshold voltage of the LOCOS field-oxide transistor passes through zero volts near 100krad(SiO_2), and device operation fails near 30krad(SiO_2). Figure 1 demonstrates the radiation response difference between the two technologies evaluated in this work.

Figure 2 shows GIDL results for the 0.35μm SOI W/L=50/50 transistor for pre- and post irradiation levels. With Vg= -8V and Vd=3V, i.e. Vgd=11V, GIDL tunneling current begins, and it increases upon exposure to radiation. From the shape of the curves it is concluded that this is a band-to-band tunneling current, and its increase with radiation is due to flat-band voltage shifts. The absence of any discernible peaks signifies that no significant number of interface states were generated by the radiation.

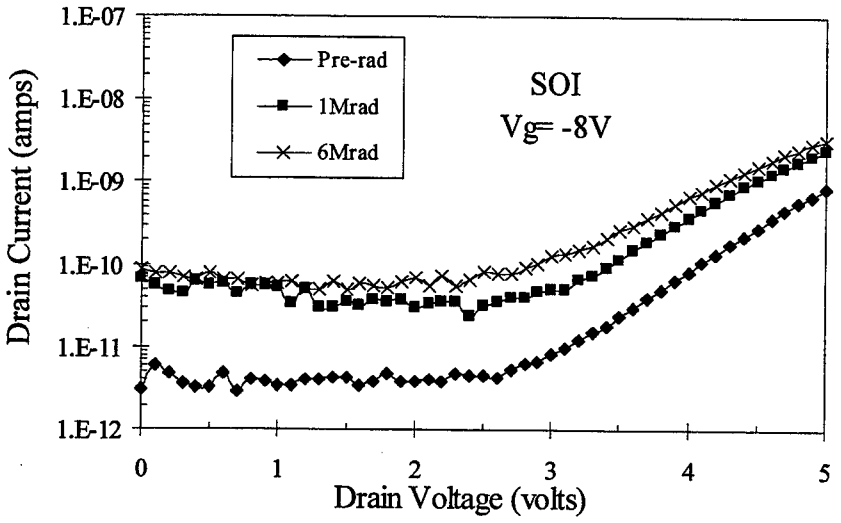


Figure 2. Shows GIDL results for the 0.35μm radiation-hard SOI W/L=50/50 transistor for pre- and post irradiation levels. The GIDL tunneling current begins at Vgd= 11V (or Vd= 3V on the graph), and the GIDL current increases upon exposure to radiation.

GIDL results for the 0.65μm bulk W/L=20/20 transistor are shown in Fig.3. The interesting feature is the presence of GIDL current peaks, known to be the result of interface state assisted tunneling. The inset to the right of Fig. 3, graphed with a linear y-axis, yields an clearer graphical view of the effect of interface state assisted tunneling on GIDL currents. The shift of the peaks towards larger drain voltage is due to the flat-band voltage increase with radiation; whereas, the increase in peak magnitude is due to the increasing interface state density with radiation.

GIDL current is known to impose scaling constraints on gate oxide thickness and power supply voltage [3]. In Ref. 3, Chan found that to limit GIDL current to 0.1pA per micron of channel width in a 10nm thick gate oxide technology, the power supply must be below 3.1V. As a direct band-to-band and/or interface-state assisted tunneling current

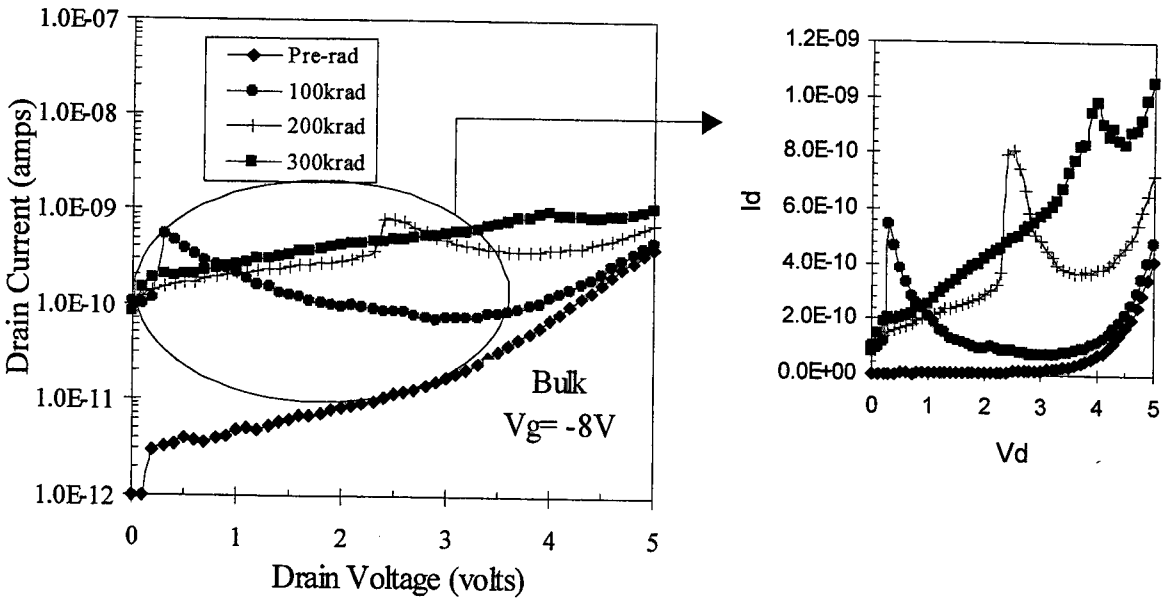


Figure 3. GIDL currents for the 0.65μm bulk W/L=20/20 transistor for pre- and post-radiation levels are shown. The presence of GIDL current peaks are observed in the radiation results. The graphical inset to the right of Fig. 3, graphed with a linear y-axis, shows the interface state assisted tunneling peaks observed on GIDL currents more clearly.

[4], the GIDL is strongly dependent on the surface electric field. The results in Fig.2 and 3 show that radiation-induced oxide charge trapping and radiation-induced interface state generation influence GIDL current. Namely, the GIDL current increases with exposure to radiation, and GIDL thresholds are lowered. Our radiation results indicate additional constraints on acceptable gate-oxide thickness and power supply voltage levels may be needed to combat GIDL effects when scaling technology.

Conclusions

This work demonstrations that ionizing radiation increases GIDL current for SOI and bulk MOSFETs. These leakage current results are important for device designers scaling VLSI technologies for high-density and low power CMOS technologies. It was found that total dose hardening can suppress interface state generation, but GIDL can still increase upon x-ray exposure due to increased band-to-band tunneling.

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Investigation of Dynamic Threshold-Voltage SOI MOSFET's with Low-Impurity-Density Channels

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I. INTRODUCTION

Reduction in supply voltage is in general the most effective way to achieve low power performance for MOSFET's. It however will seriously degrade device speed performance if the threshold voltage V_{TH} remains 3 to 5 times as high as the subthreshold swing S_w. On the other hand, use of a lower V_{th} to avoid speed degradation, while reducing supply voltage, will induce large off-state current I_{off}. Recently a novel dynamic threshold-voltage MOSFET (DTMOS) using the SOI technology, which ties the gate and the body of an SOI MOSFET together, has been proposed [1]. The DTMOS structure provides low V_{th} for high saturation driving current I_{dr} when the device is switched on, and high V_{th} for low I_{off} when the device is turned off. In order to maintain low static power dissipation, the DTMOS device needs to operate at a supply voltage near or below 0.6V to maintain a low forward-biased body current I_B [1]. This however limits the current driving capability to some extent.

The SOI DTMOS device proposed in the previous paper [1] was based on a uniform doping profile in the channel. This paper presents a simulation-based investigation on deep-submicrometer SOI DTMOS devices with a low-impurity density channel (LIDC) using a stepped-channel-doping (SCD) profile [2], which was used to achieve low-voltage high-performance operation at low temperature. The DTMOS structure with a SCD configuration, using a lightly doped surface channel and a heavily doped body, takes advantage of a higher body-source junction barrier. This device therefore provides considerably smaller body current I_B than the structure with a uniform-channel-doping (UCD) profile. In addition to the smaller body current and larger saturation driving current in the SCD DTMOS structure than in the UCD structure, study shows that SCD DTMOS structure can also effectively overcome the short channel effects.

II. DEVICE STRUCTURE AND SIMULATION DESCRIPTION

The SOI DTMOS devices used in the simulations included the SCD and the UCD configurations. Unless otherwise specified, the channel lengths for both devices

were chosen to be 0.18μm. The gate oxide thickness and the silicon film thickness were taken as 4 and 100nm, respectively. Fig. 1 shows the SCD profile for the DTMOS device. The step profile in the simulation is described by a Gaussian function with a standard deviation of $25\text{Å}/\sqrt{2}$. The surface channel thickness and doping density were t_{ch}=30nm and $N_{ch}=10^{17}\text{cm}^{-3}$, respectively. The doping density in the body was $N_B= 6\times10^{18}\text{cm}^{-3}$. As for the UCD device, N_{ch} was chosen such that it has the same threshold voltage as its SCD counterpart.

Numerical simulations were carried out using a 2D device simulator, MEDICI-4.0 [3], where the energy transport model is used for electrons and holes. Impact ionization and recombination models are incorporated into the energy transport equations, including concentration and electrical field dependent empirical mobility. The threshold voltage V_{th} is defined as the gate voltage V_{gs} at which the drain-source current I_{ds} reaches a value of 0.1μA/μm at the drain voltage V_{ds} = 0.1V. The off-state current I_{off} is evaluated at V_{gs} = 0 and V_{ds} = V_{dd}, and saturation driving current I_{dr} is obtained at V_{gs} = V_{ds} = V_{dd}. The subthreshold swing S_w is calculated at V_{ds} = V_{dd} and 0 ≤ V_{gs} < V_{th}. In order to realize the dynamic threshold operation mode, we set V_{gs} = V_{bs} for all simulated devices, where V_{bs} is the body-to-source voltage.

III. RESULTS AND DISCUSSIONS

Switching speed of a MOSFET is strongly dependent on the current driving capability. Fig. 2 compares the saturation driving current I_{dr} between the SOI DTMOS devices with SCD and UCD profiles at various supply voltages. Body currents in these structures are also included in Fig. 2. The SCD device provides a driving current that nearly doubles the current in the UCD device at the same V_{dd}. This is mainly caused by a larger lateral BJT current gain [1,4] in the SCD device than in the UCD device due to a higher emitter-to-base density ratio in the SCD device.

In addition, the body current I_B of the SCD device is considerably lower than that of the UCD device at the same V_{dd} because the heavily doped body in the SCD device induces a higher body-source junction barrier. This allows the SCD DTMOS device to operate at higher V_{dd} in order to improve the driving capability without degrading low static power performance. For example, as shown in Fig. 2, the body currents in the SCD device at 0.68V and in the UCD device at 0.6V are nearly the same. However, the SCD DTMOS device at 0.68V can provide a driving current 2.6 times as large as that in the UCD DTMOS device at 0.6V. It should be noted that V_{bs} below 0.6V was chosen in UCD DTMOS devices in Ref. [2] to keep I_B < 2nA/μm. Our simulation result indicates that in the SCD device I_B is near 1.7 nA/μm at V_{bs}=0.7V in Fig. 2 where V_{bs} = V_{gs} =V_{dd}.

Off-state leakage current I_{off} as a function of V_{dd} is illustrated in Fig. 3 for the SOI DTMOS devices using the SCD and UCD profiles. Partially due to the lightly doped channel in the SOI DTMOS devices using the SCD profile, a steeper

subthreshold swing is observed in the SCD structure than in the UCD device. Our calculations lead to $S_w \approx 60.5$ mV/Dec in the SCD device and $S_w \approx 65.5$ mV/Dec in the UCD device for supply voltage as large as 0.8Volt . As a result, a considerably lower off-state current I_{off} in the SCD device than in the UCD device is observed even though these two device structures have the same threshold voltage.

I_{off} in the SCD device shown in Fig. 3 is insensitive to V_{dd}. On the contrary, I_{off} in the UCD device increases evidently with V_{dd}. This implies that, due to the heavily doped body, the SCD profile can effectively overcome the short channel effects and substantially minimize the source-drain punch-through current. Figs. 4(a) and 4(b) show the variations in I_{off} and V_{th}, respectively, with channel lengths of SOI DTMOS devices with SCD and UCD profiles. Significant improvement in the punch-through current in the short-channel DTMOS devices, when using the SCD profile, is also clearly observed in Fig. 4(a). In addition, it is apparent in Fig. 4(b) that the SCD device exhibits a substantial improvement on the V_{th} roll-off characteristics over the UCD structure. This is also ascribed to the heavily doped body in the SCD device.

IV. CONCLUSIONS

Based on the 2D energy transport model using MEDICI, influences of the low-impurity-density channel (LIDC) using SCD profiles on performance of deep-submicrometer SOI DTMOS devices were studied systematically. It is found that the LIDC with the step-channel-doping (SCD) configuration incorporated into the SOI DTMOS device can not only effectively suppress the short-channel effects, but also provide much higher driving capability than the SOI DTMOS device with uniformly doped channels. In addition, the heavily doped body in the SCD device substantially reduces the forward-biased body current and source-drain punch-through current. Supply voltage for the SOI DTMOS device with the SCD profile can therefore be increased to improve the driving capability and switching performance without degrading low static power performance. SOI DTMOS devices with SCD profiles are therefore very suitable for low-power and high-speed VLSI applications.

Acknowledgement - This work was supported by SGI/Cray Research and ARO under Grant No. DAAG55-98-1-0525.

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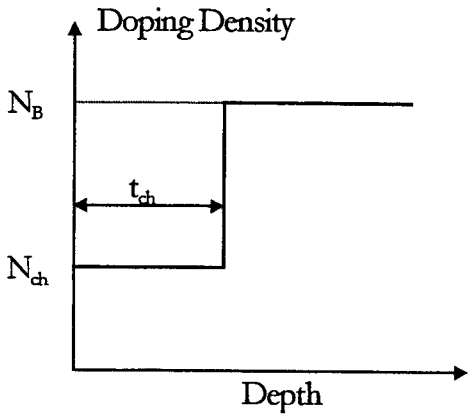
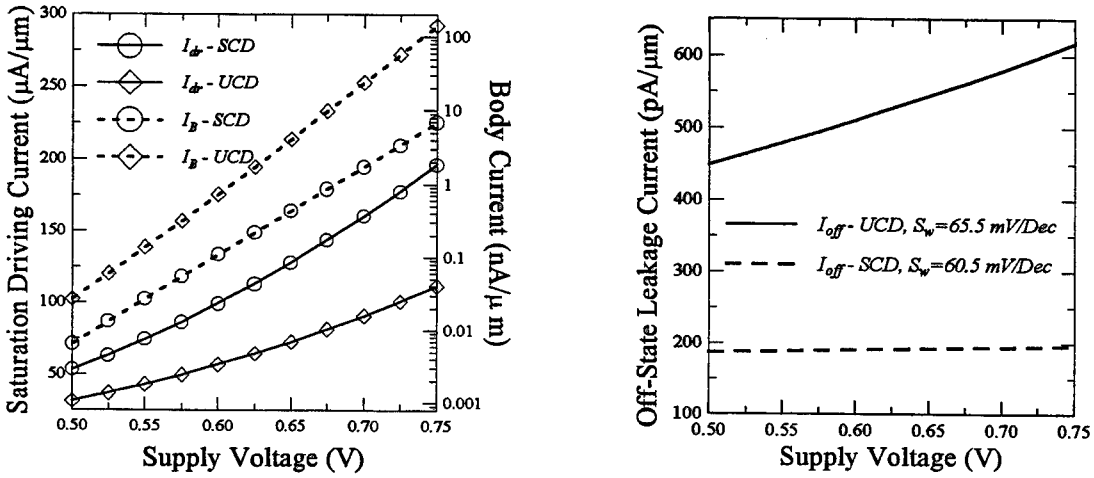


Fig. 1 Stepped channel doping profile for the DT SOI structure.



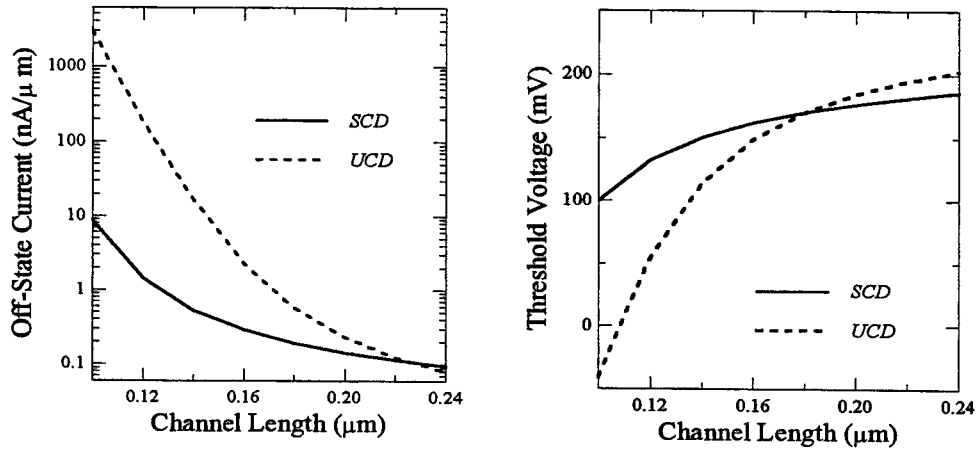


Fig. 4 (a) I_{off} and (b) V_{th} vs. channel length for devices with SCD and UCD profiles. V_{dd}= 0.7V is chosen for the calculations of I_{off}.

Nonlinearity Analysis of HBTs

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Intermodulation distortion in microwave and milli-meter wave common-emitter HBT amplifiers have been analyzed using a general Volterra series representation. The analysis takes into account interactions between the nonlinear parameters and generated spectral components by partitioning the total current density into tunneling and thermionic components. The output power as well as IP2 and IP3 are derived for third-order intermodulation distortion.

I. INTRODUCTION

Heterojunction bipolar transistors (HBTs) have been widely used for microwave and millimeter-wave power application, particularly for mobile radiotelephony or scanning radar application [1]. HBTs are known for their low-distortion characteristics in linear power applications. The good linearity of HBTs has been attributed to partial cancellation of the intermodulation current generated by the emitter-base dynamic resistance and emitter-base capacitance [2]. Nonlinearity creates intermodulation distortion and is one of the key issues in power application design. AlGaAs/GaAs HBTs have demonstrated a third-order intermodulation point (IP3) of 33 dBm with 150mW dc power as reported by Nelson *et al.* [3] and by Kim [4]. An internally matched linear power HBT with 20 W output power, 6.5 dB gain, and 40% power-added-efficiency (PAE) at 7.5 GHz was reported and a high-efficiency HBT monolithic-microwave integrated-circuit (MMIC) linear power amplifier for personal communication application has also been demonstrated, where the output power was 21 dBm and PAE was 35% [5].

The nonlinearity of HBT in base-emitter junction has been reported [6]. This work investigates distortion in HBT amplifiers using simple nonlinear device models that are analyzed by a systematic procedure based on the Volterra series. The analysis may readily be extended to more complex networks involving multistage amplifiers. Closed-form expression for third-order intermodulation distortion is derived. The analytical result of output power (Pout) is compared with the experimental data of a CE HBT operating at 7GHz.

II. THEORY

The nonlinear circuit representation of the HBT amplifier using a hybrid-π is shown in Fig. 1. Three dominant nonlinearities from the base-emitter capacitance, C_π, the base-emitter conductance, g_π, and the transconductance, g_m [6] are considered. The parameters in Fig. 1 are defined as [7]

$$g_\pi = \frac{dI_B}{dV_{BE}} = \frac{g_m}{\beta} \qquad g_m = \frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT}$$

$$C_\pi = \frac{dQ_{BE}}{dV_{BE}} = \tau g_m + C_{je}(V_{BE}) \qquad g_0 = \frac{dI_c}{dV_{BE}} = \frac{I_c}{|V_A|}$$

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where I_C and I_B are the collector and base currents, C_π, the base-emitter capacitance which includes junction capacitance as well as diffusion capacitances, τ is the forward carrier transport time, and β is the current gain. Base-collector conductance, g_{bc}, is negligible due to the insignificant basewidth modulation and is due to the high Early voltage, V_A ($g_{bc} = kT/qV_A \cdot g_m/\beta$ [6]).

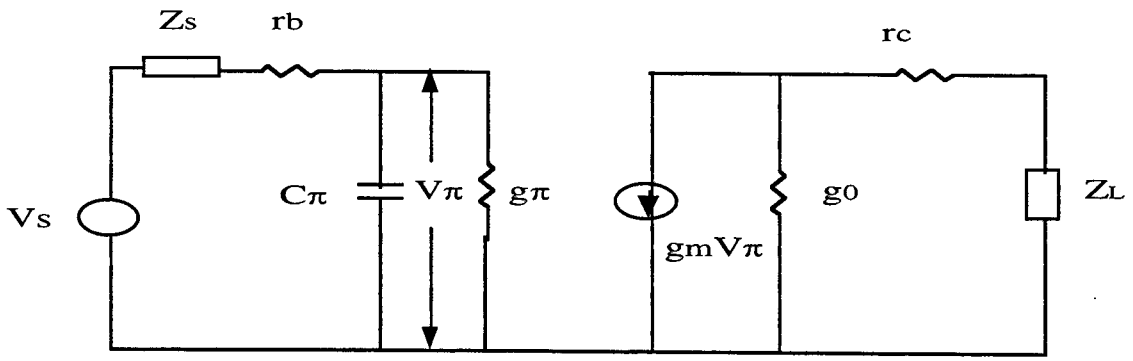


Fig 1. Simplified CE HBT small signal circuit

The voltage dependence of conductance, the base-emitter capacitance and transconductance can be expressed as a Taylor series in the vicinity of the bias point.

$$g_m = g_{m1} + g_{m2}v_{be} + g_{m3}v_{be}^2, \qquad C_\pi = C_{\pi 1} + C_{\pi 2}v_{be} + C_{\pi 3}v_{be}^2,$$

$$g_\pi = g_{\pi 1} + g_{\pi 2}v_{be} + g_{\pi 3}v_{be}^2$$

The results shown in Fig. 2 are based on the calculation where partitioning the total current density into tunneling and thermionic components[8] carrier velocities at emitter-base and base-collector junctions, the bandgap narrowing and quasi-Fermi level splitting are considered. The size dependence of diffusion constant and mobility due to non-stationary transport in narrow base HBTs is also incorporated [9]. The nonlinearities are represented as voltage-controlled current sources using a three-term Taylor series expansion of the characteristic about the operating point as: $i_{g\pi} = \sum_{n=1}^{3} g_{m\pi} v_\pi^n$, $i_{C\pi} = \frac{d}{dt}\sum_{n=1}^{3} C_{\pi n} v_\pi^n$, $i_{gm} = \sum_{n=1}^{3} g_{mn} v_\pi^n$ and $i_{g0} = \sum_{n=1}^{3} g_{0n} v_\pi^n$. The output power at the fundamental frequency, ω_1, and the third-order intermodulation, $2\omega_2 - \omega_1$, can be expressed as

$$P_{out_1} = \frac{1}{2} v_{01}^2 Y_L(\omega_1) = \frac{1}{2} \frac{Re[Z_L(\omega_1)] \left| V_s H_1(\omega_1) \right|^2}{\left| Z_L(\omega_1) \right|^2} \qquad (1)$$

$$P_{out_3} = \frac{1}{2} v_{03}^2 Y_L(2\omega_1 - \omega_2) = \frac{1}{2} \frac{Re[Z_L(2\omega_1 - \omega_2)] \left| V_s^3 H_3(\omega_1, \omega_1, -\omega_2) \right|^2}{\left| Z_L(2\omega_1 - \omega_2) \right|^2} \qquad (2)$$

where v_{01}, v_{03} is the first-order and third-order output voltage in the load, Z_L, and $H_1(\omega_1)$, $H_3(\omega_1, \omega_1, -\omega_2)$ is the first-order and third-order transfer function, respectively.

RESULTS AND DISCUSSION

The power HBTs with emitter area of $20\,\mu m^2$ are used in this work [10]. Typical bias dependence of the various equivalent circuit elements are shown in Fig.2. Fig.3 shows the simulated output power which compared well with the experimental data reported by Wang *et al.* [10] for HBT operating in class A under single and double tone excitation with signals at frequencies $f_1 = 7\,GHz$ and $f_2 = f_1 + \Delta f$, where $\Delta f = 5\,MHz$. The operating condition are V_{ce}=7.0V and I_c=70mA. The calculated 1 dB gain compression point of 24.5 dBm at an input power of 13.5 dBm compares well with the experimental value of 23.8 dBm. Intermodulation distortion is a strong function of g_m which in turn depends upon current gain and dynamic base resistance. A high Early voltage, due to heavy base doping, makes intermodulation distortion less sensitive on g_0.

In Fig. 4, the fundamental and third-order intermodulation output power is plotted as a function of frequency. At low frequencies the third order intermodulation output power is very small and hence not so important for power amplifiers. The second and third order intercept points (IP) obtained by extrapolating P_{out_1} and P_{out_3} are plotted in Fig. 5. A higher IP, at low P_{out}, implies good linearity which depends with increasing output power.

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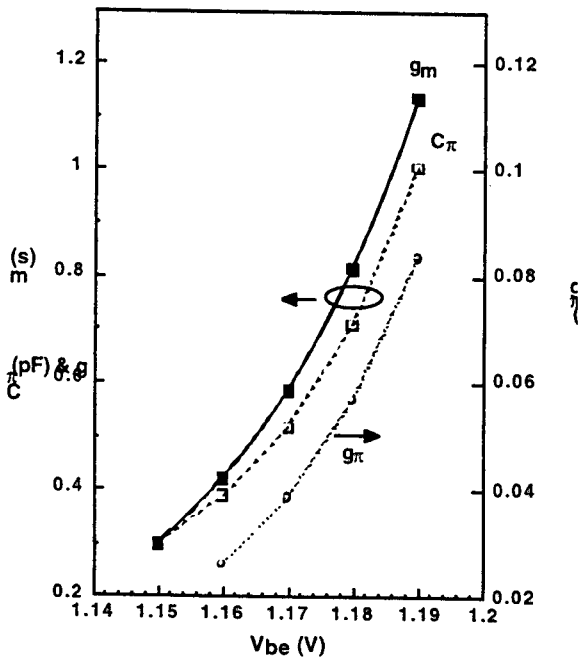


Fig. 2. g_m, C_π and g_π bias dependence of the HBT [19]

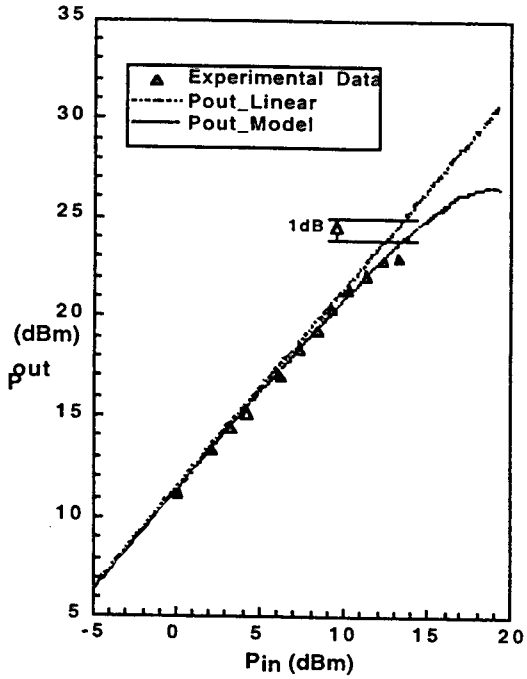


Fig. 3. Measured and calculated fundamental output and IM distortion for CE HBT in class A operation at 7 GHz biased at V_{cc}=7V and I_c=70mA.

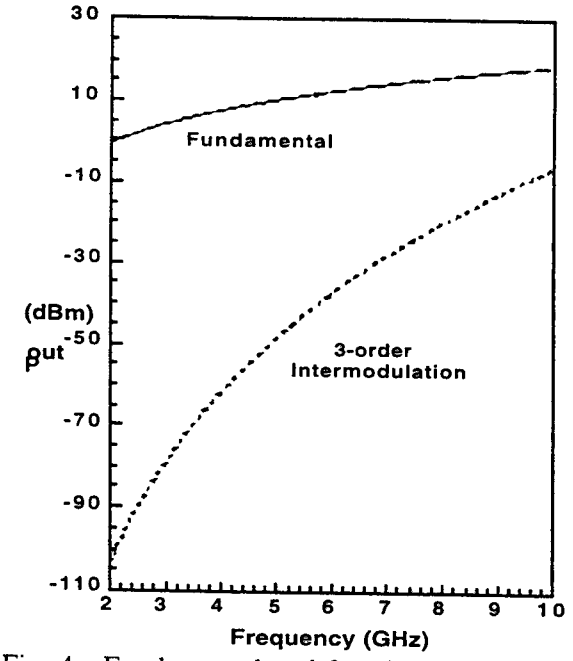


Fig. 4 . Fundamental and 3-order intermodulation output power as a function of frequency at 4dBm input power.

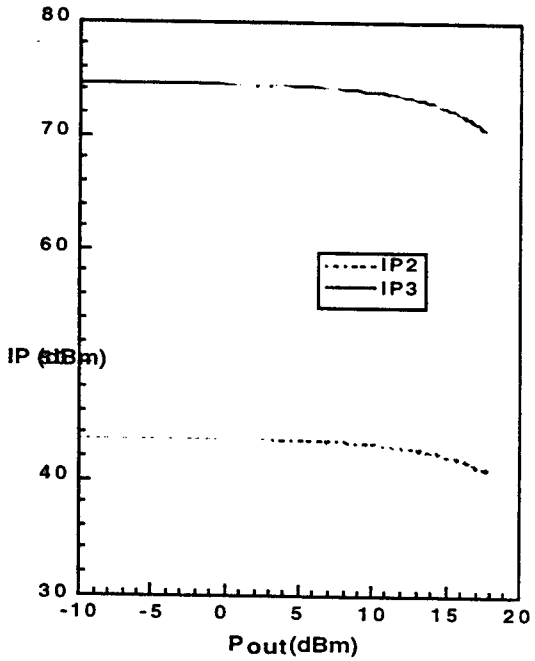


Fig. 5 Simulated IP2 and IP3 at 7 GHz .

BALLISTIC NEGATIVE-EFFECTIVE-MASS FIELD-EFFECT TRANSISTOR: SIMULATIONS

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We consider several designs of gated ballistic p^+pp^+- or n^+nn^+- planar diodes. Gate potential control of concentration in a base channel allows us to switch an oscillatory regime of a ballistic negative-effective-mass terahertz generator on and off, to vary amplitude of current oscillations, and to tune oscillation frequency in very wide ranges.

The basic subject of our consideration in this report is a ballistic field-effect transistor (FET), that is, a planar ballistic p^+pp^+- or n^+nn^+-diode, in which a middle region (a p-base or an n-base) is a gate-controlled current-conducting channel, sandwiched between p^+- or n^+- source S and drain D (Fig. 1).

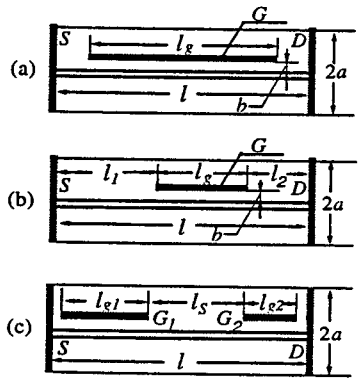


Fig.1 Designs of single-gate (a), (b), and double-gate (c) ballistic generator structures. We select for simulation the following sizes:
(a) $l = 0.2$ μm; $(l - l_g)/2 = 0.02$ μm; $b = 0.016$ μm, $2a = 0.16$ μm;
(b) $l_1 = l_2 = 0.083$ μm (1); $l_1 = 0.061$ μm, $l_2 = 0.105$ μm (2); $l_1 = 0.105$ μm, $l_2 = 0.061$ μm (3); $l = 0.2$ μm, $l_g = 0.033$ μm; $b = 0.016$ μm, $2a = 0.16$ μm;
(c) $l = 0.2$ μm; $l_{g1} = l_{g2} = 0.085$ μm; $b = 0.016$ μm, $2a = 0.16$ μm.

A single gate or two gates are placed over the base and cover some part of the base area. It is assumed that some specific dispersion relation $\varepsilon(p)$ (ε is energy, p is a momentum) containing a negative effective mass section (Fig. 2) is inherent in current carriers of the channel. Such dispersion relations take place for holes in square p-type quantum wells (p-QWs), for electrons in asymmetric double QWs etc [1-4]. Base length, l, is assumed to be short enough that carrier transport in the channel to be ballistic (collisionless). But this length is assumed to be long enough in order to accommodate some quasineutral region (QR) between source-adjacent and drain-adjacent spatial charge regions (S-SCR and D-SCR).

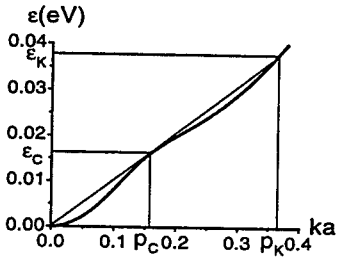


Fig.2 A dispersion relation of quantized holes in the ground subband of 8 nm square p-type GaAs/AlAs quantum well. This relation is used for our simulations.

In the absence of the NEM-section in a dispersion relation, a current in the conventional ballistic FET channel I rises with rising a drain-source voltage V_D (if $V_D < V_G + V_{G0}$) as

$$I \sim (V_G + V_{G0})V_D^{1/2}, \qquad (1)$$

where V_G is a gate potential relative to the source, and V_{G0} is defined by an initial channel doping (see [5]). This current is saturated to value $I = I_S \sim (V_G + V_{G0})^{3/2}$ at $V_D \approx V_G + V_{G0}$. According to [6] a saturated current is stable for all voltages but there is a current instability in a rising current

branch while formula (1) takes place. This instability is initiated by convective two-beam instability in the QR. Similar instabilities in bulk ballistic diode structures are considered in [7,8] (see also references in review [7]) and are demonstrated in ungated planar ballistic structures [9].

The presence of the NEM-section in a dispersion relation leads to current saturation in ungated channels. Therefore behavior of gated channels depends on correlation of two voltages: $V_G + V_{G0}$ and $V_C = \varepsilon_C / e$ (the latter is defined by positioning the NEM section – see Fig. 2). If $V_G + V_{G0} << V_C$, current saturation occurs much earlier than NEM-carriers can appear, and such a transistor has not to differ from the conventional ballistic FET. If $V_G + V_{G0} >> V_C$, a current increase in such a transistor is restricted by the NEM-section. A new section of quasisaturation appears (NEM saturation in planar structures is never absolute). As a result the stationary *IV*-characteristic becomes unstable, and a section of current oscillations is displayed in exchange. This unstable NEM quasisaturation section has to be extended by a new section of current increasing and next a new section of current saturation (beginning from $V_D \approx V_G + V_{G0}$). We test all these expectations by numerical simulations. We use for these simulations the dispersion relation for quantized holes in the ground subband of 8-nm square p-type GaAs/AlAs QW shown in Fig. 2. Oscillatory regimes in ungated p^+pp^+-structures with such a dispersion relation and with bases of different lengths are considered in great detail in Ref. [10].

First of all we consider characteristics of the maximally gate covered structure sketched in Fig. 1(a). Indeed (as in [10]) a periodic system of parallel channels confined between the plane source and the plane drain is considered. Spatial period $2a$ is selected large enough that each channel to be almost independent. This system can not radiate electromagnetic waves in the free space. Therefore, we solve only a selfconsistent problem with a 2D Poisson equation and 1D ballistic transport kinetic equation. This problem is described in detail in [3,10]. Results of calculations of source (I_S) and gate ($I_G = I_D - I_S$) currents in dependence on adiabatically raising with time drain voltage V_D at several values of V_G are presented in Fig. 3.

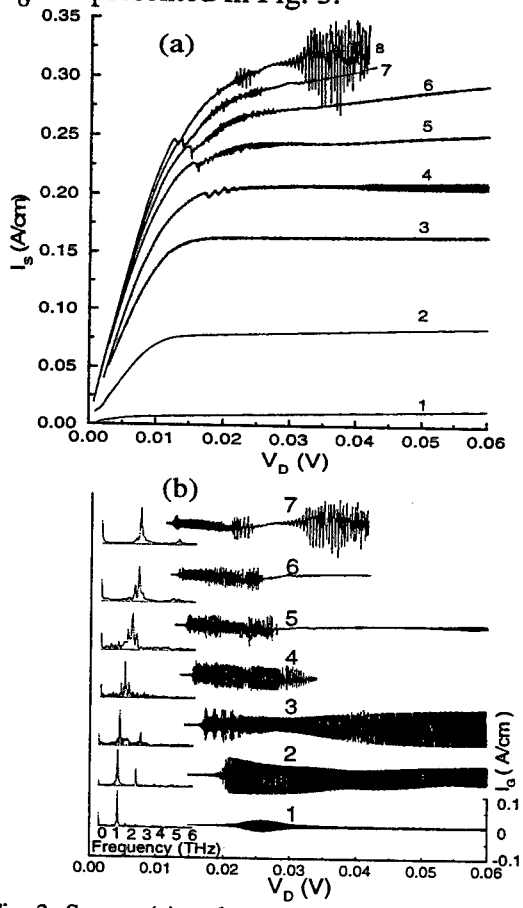


Fig. 3 Source (a) and gate (b) currents versus drain voltage V_D for different gate potentials V_G:
(a) V_G = 50 mV(1), 25 mV(2), 0 mV(3), -25 mV(4), -50 mV(5), -75 mV(6), -100 mV(7), -125 mV(8);
(b) V_G = -4 mV(1), -8 mV(2), -25 mV(3), -50 mV(4), -75 mV(5), -100 mV(6), -125 mV(7). Positive gate potentials are depleting and negative gate potentials are enhancing. Drain potential V_D is adiabatically increasing with time t with rate dV_D/dt = 0.2 mV/ps. Fourier analysis results of gate current oscillations (calculated in the intervals of the highest frequency) are presented on the right side of (b)

The gate current is the oscillating displacement current only because the barrier outside the channel is nonconducting at T=4.2 K. We see that the source current [Fig. 3(a)] is almost free of oscillations. Highly developed oscillations of this current take place only for large enhancing voltages V_G. Oscillations of the drain current and connected with them appearance of the oscillating gate current occur from $V_G \sim 0$ (that is, $V_G + V_{G0} \sim$ 50 mV). A drain voltage range of these oscillations is very narrow at the threshold of their beginning but it expands very quickly with increasing V_G. The right border of this range at $V_G =$ 8 mV is much greater than right border of the NEM instability $V_K = \varepsilon_K / e$ (see Fig. 2) is. For $V_G >$ 50 mV this range is narrowed again and goes into the prescribed interval $[V_C, V_K]$. But at large values of V_G(>75 mV) certain additional intervals of oscillations appear. These intervals are isolated from the initial NEM section. Such an additional interval becomes very expanded at V_G=125 mV and amplitudes of oscillations in this interval exceed significantly amplitudes in the NEM section. However, the oscillation frequency in the NEM section increases monotonically with increasing V_G (from 1.2 THz at $V_G =$ 4 mV to 2.8 THz at $V_G =$ 125 mV) while oscillation frequencies in additional intervals do not increase evidently with increasing V_G and stay in the level of 0.7-1.0 THz. These frequencies are close to oscillation frequencies in ballistic FETs without of the NEM –sections in dispersion relations of channel carriers. [We have considered such non-NEM FET side by side with the NEM FET. An effective mass of channel carriers in the non-NEM FET is selected to be equal to the heavy hole effective mass. The oscillations in the non-NEM FET are present only in the rising branches of *IV*-characteristics and are absent in the saturation sections in accordance with the predictions of [6]. Let us note that the additional intervals of oscillations in the NEM FET are just in a section of visible current saturation, as this is seen in Fig.3 (c)]. We can assume that an oscillation structure in the additional intervals is more complicated than in the case of development of the conventional two-beam instability.

Short-gated single- and double-gate structures [Fig.1 (b), (c)] are aimed for to produce such distribution of carrier concentration and electric field in the channel that a certain effective base (much shorter than drain-source distance l) could be formed.

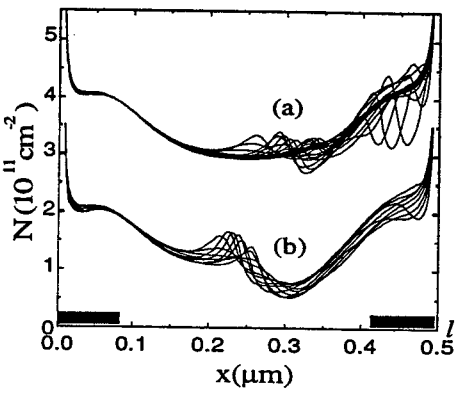


Fig.4 Snapshots of concentration distributions, $N(x)$, in the base of the double-gate device for two different stages of oscillation process: (a) – small drain voltages, V_D (50 – 65 mV). Sample parameters: l = 0.5 μm; $l_{g1} = l_{g2}$ = 0.085 μm; b = 0.064 μm, $N_A = 8 \cdot 10^{10}$ cm^{-2}, μ = 20 meV. Distributions (a) are $2 \cdot 10^{10}$ cm^{-2} shifted upward.

For example, for the double-gate structure [Fig. 1(c)] the effective base length could be smaller than intergate distance l_s. For the short single gate structure [Fig. 1(b)] results of such tries are successful only partially because all the base section from the right side of the gate is included in the oscillatory process. For the double-gate structure our

progress is more completed at increased drain voltages.

It is seen in Fig. 4 where snap-shots of oscillating concentration distributions in two drain voltage ranges are presented. Oscillatory activity for large drain voltages [Fig. 4(b)] is concentrated in the middle (ungated) section of the device. Results of simulations for the short-gated ballistic diodes are stated in more detailed form in [11].

The NSF grant and the GPL DFDR grant supported this work.

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Attenuation of Aluminium Air-Bridges in Coplanar Waveguides

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I. Introduction

Coplanar waveguides (CPW) are becoming more important in millimeter wave-technology because of their uniplanarity. This leads to an excellent incorporation with other active and passive surface devices without the need for etching via holes. Conversely CPW leads to parasitic (even) slot line modes. To suppress these multi modes the use of connections between the two ground metallizations is necessary. These bridges have to be placed at the corners, T-connections and other discontinuities. Our principle area of concern leans towards bridges on insulators which are more CMOS compatible. In the first instance we achieved Al air-bridges. This approach avoids the use of gold, which causes problems in CMOS technology because of electromigration. As shown in several publications [1], [2] air-bridges cause a change in reflection and a higher attenuation.

We investigated in the attenuation and reflection of aluminium air-bridges in CPW on high-resistivity silicon substrates. There are two main possibilities to realise air-bridges: in one version the ground plane is bridged over the center conductor (type A), and in the other the center conductor is bridged over the ground to ground connection (type B). Former simulations of both types showed smaller reflections for air-bridges of type B [3]. Because of these results we decided to process only air-bridges of type B.

II. Technology

The air-bridges were processed in six steps. The first layer was a thin 200nm thick oxide covering the whole wafer (step 1). After this the first aluminium layer was evaporated and patterned (step 2); the thickness of this layer was 250nm. The third step was a 200nm thick sputter oxide to isolate the first and the second aluminium layer. After this the contact holes were etched to enable electric contact between the first and the second metallic layer (step 4). This was done by a dry etching process. The fifth step was the spinning and structuring of the photoresist. The photoresist was used as sacrificial layer for the air bridges. We used a standard photoresist (Hoechst AZ 5214) with a thickness of 1.4µm. Together with the sputter oxide the distance between the first and the second aluminium layer was 1.6µm. Because of the high ε_r of our sputter oxide

(ε_r = 3.9) and the thin layer thickness the reduction in capacity resulting from this layer was negligible. After the sacrificial layer the second aluminium layer was evaporated on the photoresist with a thickness of 1.5µm (step 6). Finally the photoresist layer was removed in acetone. See also figure 1 for an SEM picture of a realised aluminium air-bridge.

III. Results

For the measurements we processed transmission lines with a centre conductor width (w) of 45µm and a slot width (s) of 25µm (ground to ground spacing d=95µm). This transmission line fits to the 50Ω environment of the HP 8510B network analyzer. We processed two different lengths, 500µm and 1000µm without air-bridges and the same lengths with air-bridges. While the shorter CPW contains two air bridges the longer contains six air-bridges. The distance between the air-bridges was always 150µm.

As it is known from simulations each air-bridge causes a certain amount of attenuation [4],[5], which is dependent on the frequency. The results of the measurements of S_{21} are displayed in figure 2 and 3. Figure 2 shows the results of the longer transmission lines without air-bridges and with six air-bridges. Figure 3 depicts the same measurements for the short CPW line with two air-bridges. In both cases the increase in attenuation corresponds with the increase in the number of air-bridges. The amount of the increase depending on frequency is shown in figure 4. Compared with [4] the measurements show the similar frequency dependence. It has to be taken into account that different dimensions and smaller distances between the metal layers create another attenuation level.

Figure 5a points out the increase of the magnitude of the reflection depending on the number of the air-bridges. Additionally the Smith chart in fig. 5b shows the phase of the reflection. Because of the small number of air-bridges in the 500µm CPW line the phase shift cannot be estimated exactly. For the 1000µm CPW line with six air-bridges the behaviour is inductive. This agrees with former results [3] predicting an inductive behaviour of air-bridges of type B and the measurements in [6].

IV. Conclusions

Standard process steps and materials were used to fabricate aluminium air-bridges on high resistivity substrates. To be as close as possible to standard process steps we reduced the distance between the two aluminium layers to 1,6µm. It is evident that this leads to a higher attenuation per air-bridge than a distance of approximately 3µm which is often used together with gold metallisation. Because of different dimensions of the transmission lines (a smaller transmission line leads to a higher attenuation) and a different distance between the aluminium layers, it is not possible to get an exact relationship between the results of the simulations and our measurements. Apart from the variations our measurements show good agreement with theory [4].

Acknowledgements
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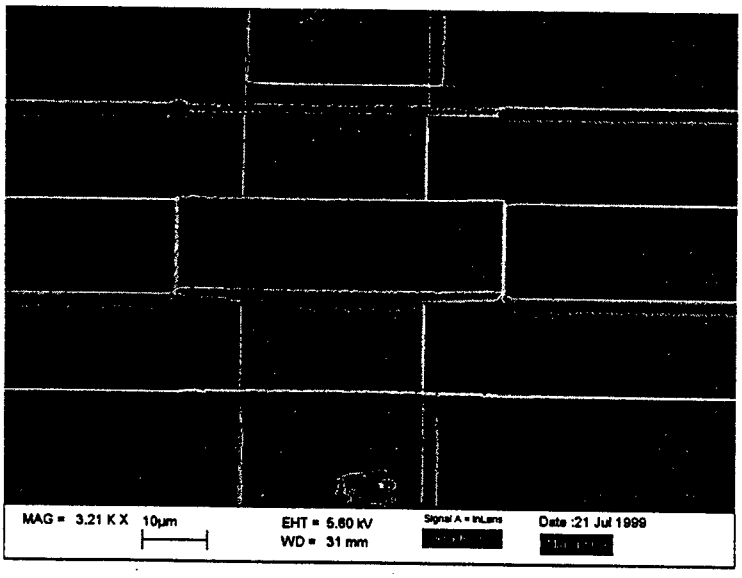


Fig. 1 : SEM picture of a realised aluminium air-bridge

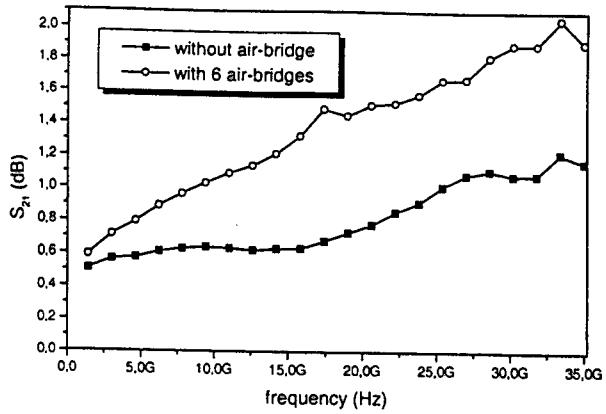


Fig. 2 : Attenuation of the 1000µm CPW line

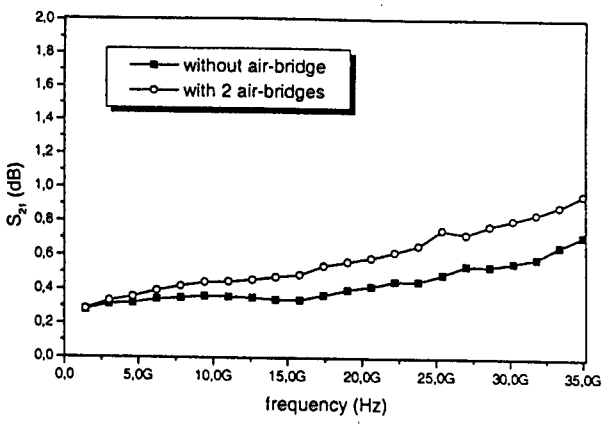


Fig. 3 : Attenuation of the 500µm CPW line

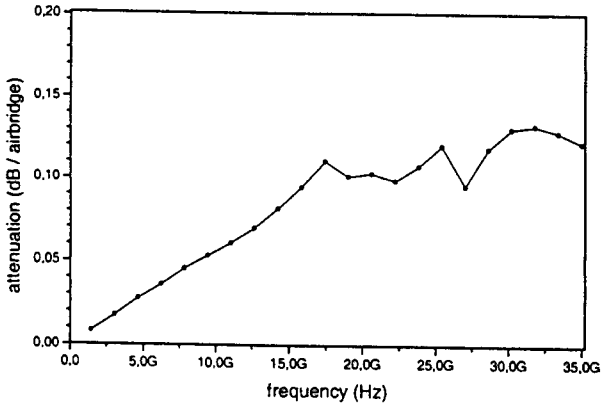


Fig. 4 : Attenuation per Air-Bridge vs. Frequency

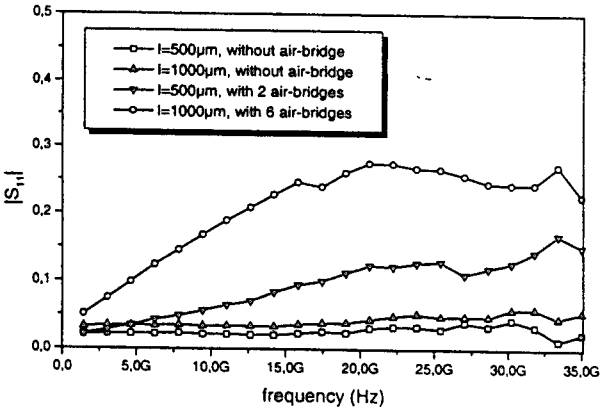


Fig. 5a : Magnitude of S_{11}

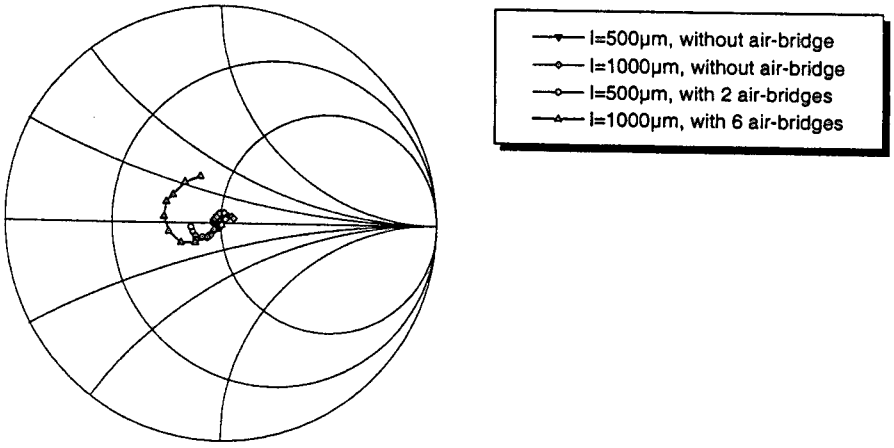


Fig. 5b : Smith chart of the CPW lines

Fabrication of nanometer-scale InAs quantum wires

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1. INTRODUCTION

Recently, there has been remarkable progress in the fabrication of quantum devices, whose dimensions are comparable to the Fermi electron wavelength λ_F, where $\lambda_F = 2\pi/k_F$ and $E_F = \hbar^2 k_F^2 / 2m^*$. In addition to quantum size effects, new device applications using coherent phenomena, e.g., electron wave diffraction [1] and Aharonov- Bohm interference [2] have been proposed. Most experimental effort has focused on the GaAs-based heterojunction system, in which high-mobility two-dimensional electron gas is confined at the hetero-interface. To further produce size quantization along the lateral directions, a "split-gate" approach is often adopted. Patterned Schottky gates with a negative bias can deplete electrons below. However, due to the Schottky barrier height and the material constants, the confining potential is smooth, resulting in disparity of the physical size and the dimension where electrons are located. For example, a quantum wire ~ 450-500 nm [3] in width is fully depleted of electrons. Such uncertainty leaves quantitative modeling of many interesting behavior of electrons unfinished.

To substantiate quantum wave phenomena in the device characteristics, the device dimension should be much less than the coherence length. Limited by electron-phonon and electron-electron scattering, the coherence length in high-electron mobility GaAs/$Al_xGa_{1-x}As$ heterojunctions is measured to be several microns at 4.2K. It is therefore challenging to engineer a system where several function quantum devices can fit into such a dimension.

Electrons in the InAs/$Al_xGa_{1-x}Sb$ system offer important properties that can be utilized in nanometer-scale quantum devices. First, the electron effective mass is 3 times smaller than that in GaAs. A small effective-mass will lead to high low-field mobility, long mean free path, and large inter-subband energy separation. Moreover, its larger conduction-band discontinuity leads to a stronger confinement of electrons in the quantum well. Another unique property is that the Fermi level pinning position of InAs is ~100 meV above the conduction band minimum. That is, any metal can make an n-type ohmic contact to InAs.

In order for InAs wires/dots to show lateral size quantization, the dimension of the device should be shorter than the Fermi electron wavelength. In InAs, λ_F is 250nm and 25 nm, for E_F = 1meV and 100 meV, respectively. Even at high electron concentration (large E_F), experimentally, 25 nm is a very attainable dimension. Developing reproducible techniques to fabricate a one- and zero-dimensional system would open up important new research areas.

2. EXPERIMENT

Because wet etching cannot offer the desired resolution and reproducibility, a reliable reactive ion etching (RIE) fabrication needs to be developed to facilitate research in nanoelectronics. Electron-beam lithography and RIE have been used successfully to make small devices for Si MOSFETs. However, RIE for GaAs and InP systems are largely developed for optical waveguides, and is not as well characterized as for silicon. Typical problems include tapered sidewalls, polymer deposition, mask erosion, damage to lattice, reduced electron mobility, surface states, Fermi level pinning, etc. We have successfully developed a fabrication process for defining InAs quantum wires/dots with 30 nm feature size. The process involves the following steps.

(1) *MBE growth* of InAs quantum well, sandwiched by AlSb. Typically, the sample consists of a S.I. GaAs substrate, a 2 μm AlSb/GaSb superlattice buffer, a 12 nm InAs quantum well, and a 12 nm AlSb gate insulator as the cap.

(2) *Electron-beam lithography* using "negative" electron-beam resist, where the region exposed will stay after development. The e-beam resist is later used as etch-mask in RIE.

(3) *Oxygen plasma ashing* to remove the traces of cross-linked resist at both sides of the patterns. Back-scattered electrons are responsible for exposing and linking a thin layer of resist undesirably. We found that this thin layer of resist, although too thin to be observed by SEM, does stop the RIE from etching into the quantum layers.

(4) *Plasma-enhanced RIE* (hydrogen, methane and argon [4]) to etch away the top AlSb barrier and the InAs quantum well and form the masked pattern into 30 nm-scale quantum devices. Dry etch damage is minimized by using low power and a low methane/hydrogen ratio. Polymer deposition during RIE is reduced by decreasing the concentration of methane and by lowering the power consumption in the plasma chamber. Damage due to RIE is extensively studied by fabricating hall-bar devices and magnetotransport measurements in the quantum Hall regime. Electron concentration increases after RIE, but it does not impede the device operation.

(5) *Oxygen plasma ashing* to remove the residue on top of the InAs quantum wire for characterization. Finally, external gold wires are soldered for electrical characterization.

We have also further developed an alignment scheme for defining a second electron-beam lithography pattern. The alignment resolution is ~10 nm, in principle only limited by the size of DRAM in our computer.

For a demonstration of this new technique, a quantum-wire-transistor is fabricated. Two SEM micrographs are shown in Fig. 1. The InAs channel is isolated by RIE, and the etching stops at the AlSb buffer. Next, a 60 nm thick Au is defined by a 2nd level electron-beam lithography with PMMA (positive resist), metal evaporation and lift-off. The gate extends across the channel, with 100 ohm measured between the two large (100 μm by 100 μm) bonding pads. The gate

length is 40 nm. The InAs quantum well channel is reduced to an 80 nm by 200 nm region at the middle of the transistor. The gate voltage V_g can successfully control the source-drain current flow for $-6V < V_g < 6V$, with negligible gate leakage current. At 4K, the source-drain conductance becomes quantized, a signature of one-dimensional density of states and ballistic transport. Fig. 2 shows the transverse relation of this transistor, where the source-drain conductance near zero bias is plotted against a sweeping gate voltage. Near zero gate voltage, in between -1 V and + 2 V, the conductance is a constant near 2.75×10^{-5} ohm^{-1}. This conductance is less than the theoretical quantized conductance of a single transverse mode, $2e^2/h$ (= 7.7×10^{-5} ohm^{-1}), since the resistance of the leads were not yet taken into account. Pseudo-four terminal devices will be characterized to verify the number of transverse modes along the channel.

In addition to three-terminal transistors, we have also fabricated a series of Hall bars with different channel width. A gradual transition from two-dimensional characteristics to one-dimensional-like is clearly observed. The coherence length of Fermi electrons has also been characterized in an Aharonov-Bohm ring-interferometer. More discussions, including fabrication recipes, further device analysis, gating effect, screening by surface charge, magneto-dependence, temperature-dependence and phase coherence effect, will be reported at the conference.

3. SUMMARY

We have developed a quantum wire system, useful for investigating nanometer-scale devices. In this regime, the quantum coherent length is much longer than the size of the devices. Since the coherence length is limited by (electron-phonon and electron-electron) scattering, thus an intrinsic material property, the coherent length is at best a few microns at low temperature. We took advantage of unique properties of the InAs-based heterojunctions and a new RIE techniques, and created a nanometer-scale device system. It is now feasible to put several quantum coherent devices together and build functional circuits based on the wave nature of electrons.

4. REFERENCES

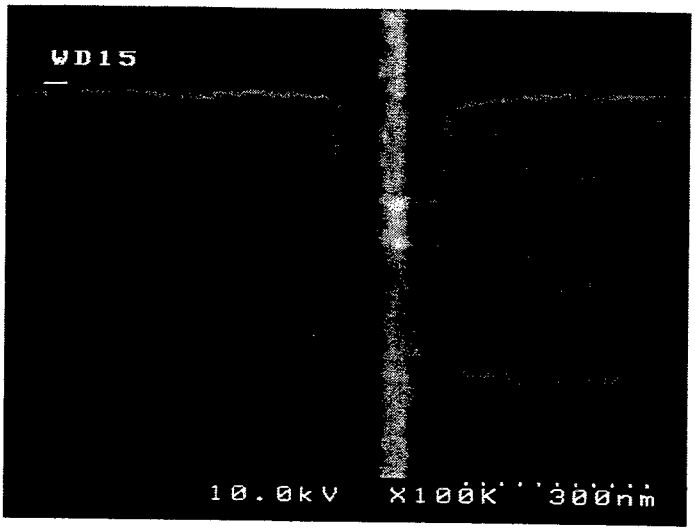
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Fig. 1
Top:
SEM micrograph of a completed quantum-wire field-effect transistor, where the channel length is ~ 200 nm, and the channel width ~ 80 nm. The metal gate is defined also by electron-beam lithography and it has two large bonding pads at the ends for connecting to gold wires. The etched field is AlSb buffer.



Bottom:
SEM micrograph of the same transistor tilted at 45 degrees relative to the scanning electron beam. The gated region as expected shows how the gate electrode goes over the 12 nm InAs quantum wire channel.

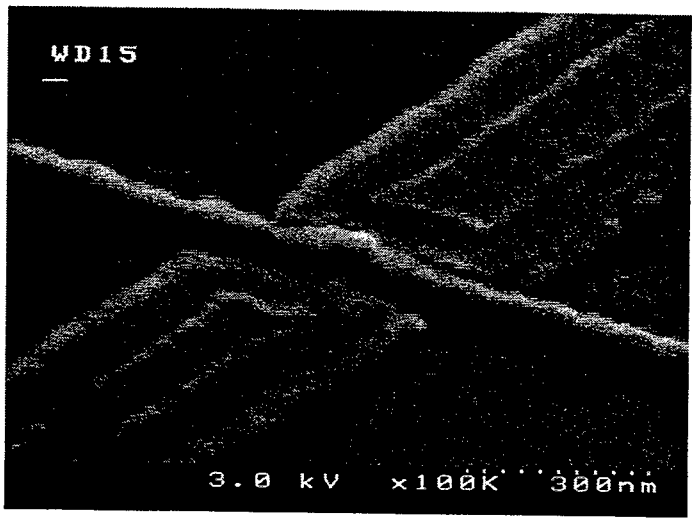
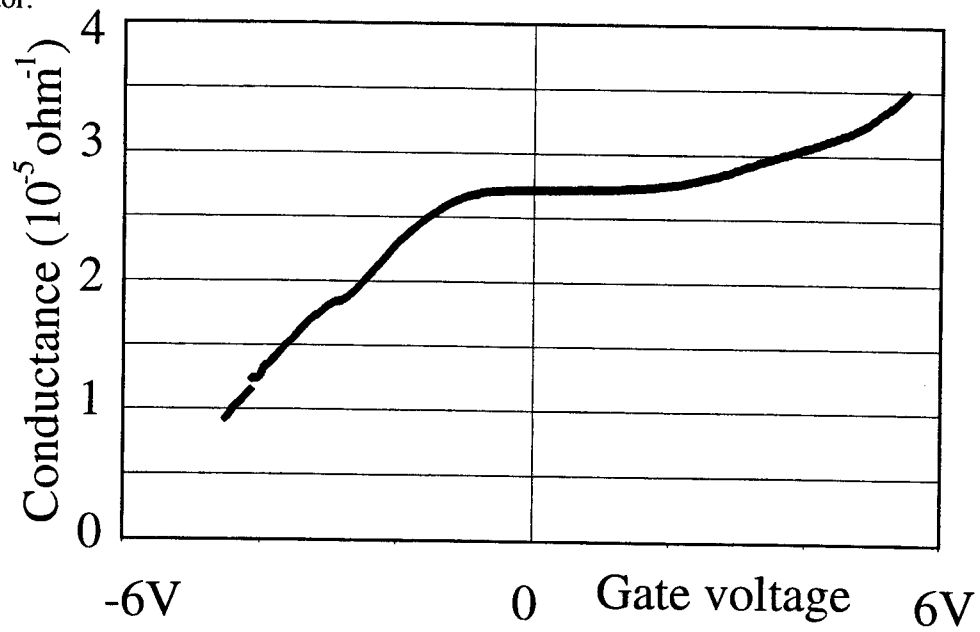


Fig. 2
Transfer relation of the same quantum-wire transistor.



Mesoscopic limits of metal-dielectric composite material conductivity

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The electrical properties of metal-dielectric composite materials containing nanometer-size metallic particles are the subject of extensive studies during the last 30 years since first works of Abeles and co-workers[1]. The one of the most challenging trends in this field is the fabrication and study of ultrasmall composite conductors which were proved to behave in a quite different way than bulk composites. The key feature of such small structures constitute so-called "incoherent mesoscopic effects" showing up in, for example, random variation of electrical properties from one sample to another. There is still high uncertainty about sample sizes separating such mesoscopic and bulk regimes of conductivity. The general possibility of using the mesoscopic behavior in nanoelectronics applications such as transistor or memory cell is also in question at present.

In this work we present the results of extensive numerical simulations of metal-dielectric composite material conductivity. In simulations, the composite sample was represented by a cube of a given size filled with randomly distributed metal balls having given diameter. The minimum allowed distance between balls was introduced as a parameter of this distribution. First of all, the capacitance matrix of this system was calculated. This matrix is needed for constructing the energy spectrum of elementary excitations of the system, namely single-electrons hops between metallic particles. The nontrivial point is that at high enough metal concentration the distances between metallic balls are comparable to their sizes, so as the Coulomb interaction between charged balls can not be considered as an interaction of point charges. We have developed the numerical procedure for capacitance matrix calculations in random systems with metal phase concentration up to 30 vol.% [2].

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When the capacitance matrix C_{ij} is obtained, the charging energy of each particle i can be calculated as $E_i^c = \frac{1}{2}Q^2 C_{ii}^{-1}$, where Q is the particle charge and C_{ii}^{-1} - the element of inverse capacitance matrix. If Q is the elementary charge e, the E_i^c is the energy needed to add or remove additional electron to the metallic ball. For the lone metallic ball having radius r in dielectric with dielectric constant ϵ the single-electron charging energy is $E_0^c = e^2/2\epsilon r$, but in the dense system of metallic particles this energy decreases due to the electrostatic polarization of particles surrounding given one. The results of numerical simulations of mean single-electron charging energies and their r.m.s. fluctuations are presented in Fig.1. The parameter Δ_{min} in this figure stands for the minimum allowed distance between balls, the dashed curve corresponds to the case when balls are placed in simple cubic lattice.

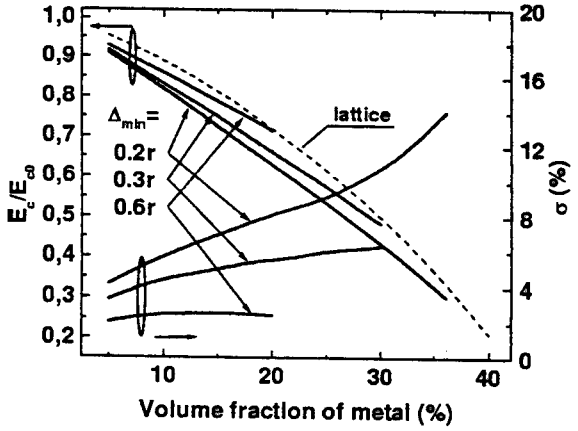


Fig.1. Mean charging energies and their r.m.s. fluctuations as a functions of metal phase concentration.

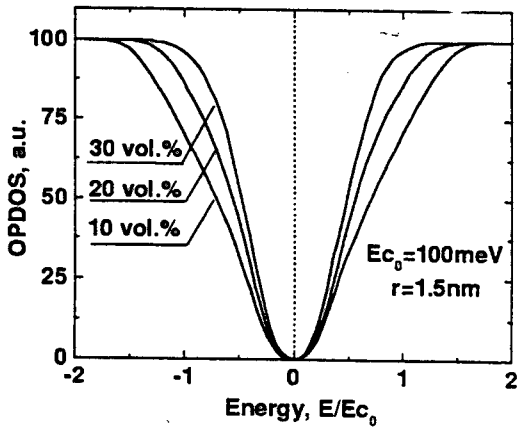


Fig.2. Simulated one particle density of states for different metal phase concentrations.

Let us write down the total Hamiltonian of the system as:

$$H = \frac{1}{2}\Sigma_{i,j=1}^{n} C_{ij}^{-1} Q_i Q_j + \Sigma_{i=1}^{n} Q_i \phi_i \,, \qquad (1)$$

where ϕ_i is so-called "random potential"[3] of particle i. This random potential was taken to be uniformly distributed in the range $-\bar{E}^c < \phi_i < \bar{E}^c$.

The procedure of calculating of the energy spectrum of single-particle excitations was as follows. First, the main state of the system was found, being the state with minimum energy (1) with respect to all possible single-electron hops. Then the energies needed to put the additional electron or hole to each particle were calculated. The results are summarized in Fig.2., where one-particle densi-

ties of states are depicted. It can be seen from this figure that well-pronounced Coulomb-gap occurred at the vicinity of the Fermi-level.

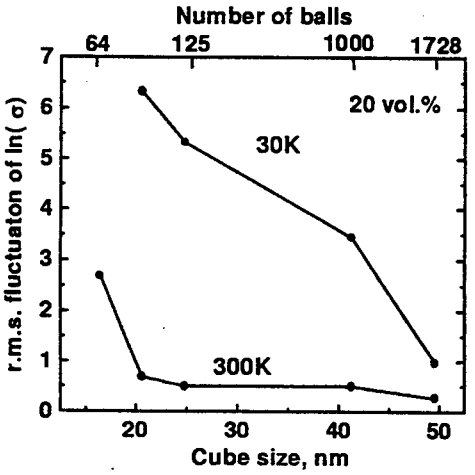


Fig.3. Simulated r.m.s. fluctuations of logarithm of composite sample conductivity vs. sample size.

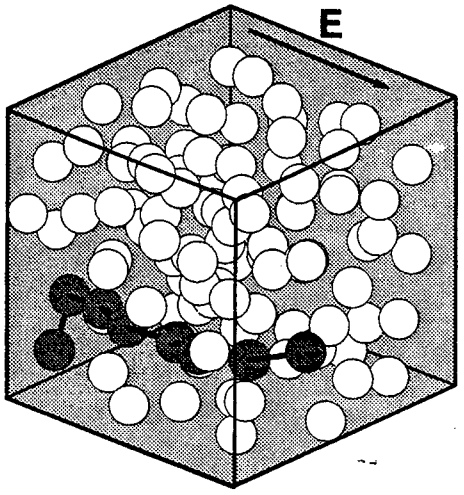


Fig.4. Simulated conducting path carrying 95% of total current. Sample consists of 125 balls, 30K.

We have performed series of calculations of temperature dependencies of low-field conductivity on the basis of obtained spectra of single-particle excitations. The calculations were carried out for sets of composite samples having different number of metallic balls. As it was expected, the conductivity varies noticeably from one random realization to another, even when the macroscopic sample characteristics are kept constant. This is so-called incoherent mesoscopic effect arising in systems having relatively small number of particles. The Fig.3 traces the dependencies of mesoscopic variation amplitude on number of particles comprising sample for temperatures 30K and 300K.

The Fig.4 illustrates the origin of such mesoscopic behavior. As it is seen from the figure, the current in the system actually concentrates along single chain of particles comprising optimal self-selected path. So, the macroscopic conductivity of the system is controlled by the conductivity of this chain constituted by several particles. Such a chain, in principle, could be shifted by external electric field. Such a switching of conducting path between different chains should result in significant change of sample conductivity, so as transistor-like structure could be implemented. Alternatively, the rearrangement of random potential of metallic particles could be achieved by charging or discharging some of them by means of, for example, carrier injection through tunnel contact. There are some evidences

that such quasi-stable charging states may have extremely long relaxation times[4]. The small rearrangement of random potential should switch conducting chains, thus resulting in drastic change of sample conductivity. This effect could be used in designing non-volatile memory cells.

To summarize, we have developed the numerical model capable of simulating low-field conductivity of metal-dielectric composite samples containing up to several thousands metallic particles. It was proved that mesoscopic deviations of conductivity of different composite samples with identical macroscopic parameters constitute several orders of magnitude at 30K for samples containing up to ~ 1000 particles and at room temperature for samples containing up to ~ 100 particles. Several suggestions were made concerning fabrication of nanoelectronic devices, such as transistor or memory cell, on the basis of mesoscopic-size composite conductors.

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Techniques for Submicron SIS Tunnel Junction Fabrication

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I. Introduction

The objective of our research is to develop fabrication techniques for the definition and insulation of submicron Nb/Al-AlO_x/Nb superconducting-insulating-superconducting (SIS) tunnel junctions. Fabrication of planar sub-half micron squared area SIS tunnel junctions has previously only been achieved using electron-beam lithography [1]. Our aim is to develop techniques for the fabrication of such junctions using technologies available here at the University of Virginia. These include a focused ion beam (FIB) fabrication tool, xerogel thin films and new metal-masking fabrication schemes.

The standard process used for fabrication of micron-scale SIS junctions involves a self-aligned resist structure [2]. A trilevel resist pattern is used to both define the junction counter-electrode and to form a via in the insulation field that separates the wiring layer from the base electrode. After the counter-electrode is defined using reactive ion etching (RIE), the wafer is covered with thermally evaporated SiO. The via through the SiO is then defined by lift-off, allowing a subsequent metal deposition to contact the junction counter-electrode. This is visually outlined in Figure 1. We have found this process to be reliable for fabricating junctions as small as 1.5μm^2. However, the trilevel resist process has shown to be much less repeatable for smaller junctions.

Several new issues appear when fabricating submicron SIS junctions. First, perimeter effects become far more prevalent in the performance of submicron junctions. In order to maintain excellent I-V characteristics, complete insulation of the junction perimeter is required. However, standard insulation techniques are unreliable for small junctions, either due to poorly define vias, inadequate perimeter coverage or both. Second, for a given insulator thickness, the aspect ratio of the vias (ratio of via height to diameter) increases as junction size decreases. Achieving a high current density contact of the wiring layer to the counter-electrodes becomes more difficult as junction sizes decrease; deposition of niobium along the sidewalls of the via can pinch-off the top of the via before it is completely filled. This leaves a void inside the via resulting in a poor contact between the counter-electrode and the wiring layer. Several fabrication techniques have been developed to eliminate these problems. Third, niobium stress effects are expected to be more pronounced for small junction areas. Our research on this topic will be published at a later date.

II. The Focused Ion Beam and Metal Masking

An FIB extracts and focuses positively charged gallium ions from a liquid metal ion source using a strong applied electric field. The gallium ions are focused onto a specimen surface using electrostatic lenses. Secondary electrons, produced as a result of the gallium ions striking the specimen surface, are collected and processed to form an image of the scanned area, similar to a scanning electron microscope (SEM). By varying the intensity of the beam and using the scan control mechanisms, the FIB can be used to physically mill

patterns into the specimen surface. These milling patterns are controlled by the user with computer-aided design (CAD) software[3].

The FIB process decouples the junction definition and insulation steps, allowing better insulation of the base electrode from the niobium wiring layer. Instead of using the trilevel resist structure to define the contact via, the resist is removed after the junction is defined, followed by the deposition of an insulating thin film that completely covers the junction. This ensures complete coverage of the junction perimeter. The FIB is then used to form a contact via through the insulation to the top of the junction counter-electrode.

Once the insulation layer is deposited, 50nm of germanium, 35nm of chrome and 5nm of gold are sputtered on to the wafer. These layers serve as a metal etch mask. Patterns are defined in the metal masking layers using the FIB and, based on these patterns, the structure of the underlying insulation layer is realized. The mill is complete when all of the metal has been removed from atop the insulating layer above the junction site. A pictorial outline is shown in Figure 2. The middle chrome layer is the actual etch mask of the structure; the ability of chrome to withstand chemical and physical attack during the reactive ion etching of the underlying insulation layer makes it well-suited for masking. The bottom germanium layer eliminates micro-masking, which occurs when small bits of metal remain atop the insulating material after the metal mask has been milled away using the FIB. Micro-masking impedes the RIE etch of the remaining insulation in the via, leaving unwanted material at the bottom of the vias. With germanium as the bottom layer, any metal that does happen to remain atop the insulator is likely to be germanium rather than chrome. This is desirable because germanium readily etches in any fluorine-based reactive ion etch chemistry. The etch rate of germanium in SF_6 is around 200Å/sec compared with 4Å/sec for SiO. Germanium, therefor, is quickly etched away during the RIE of the remaining insulating layer, leaving no unwanted material inside the via. The thin gold overlayer prevents oxidation of the chrome, which can change FIB etch conditions unpredictably.

To define the metal mask using the FIB, small holes are milled into the metal layers directly atop the junction sites, exposing the insulating material beneath. The via dimensions are determined by the FIB user and are realized using CAD software along with C++ generated data files. Figure 3 shows an SEM micrograph of a $0.16um^2$ via atop a $0.3um^2$ junction after the FIB milling process. After the metal mask has been defined using the FIB, the exposed insulating material is etched away using a fluorine-based reactive ion etch [4].

III. Xerogel Insulating Layers

Our research on the use of xerogel as an interlayer dielectric aims to replace the current insulation layer (SiO) with a material that can be just as effective electrically and yet can be deposited in much thinner layers. Such a dielectric would also need to have a high RIE etch rate and would require low processing temperatures.

Submicron junctions call for small diameter vias, through which the wiring layer contacts the junction counter-electrode. Because via depth is dictated by the required thickness of the insulating layer, smaller diameter vias have a higher aspect ratio (ratio of height to diameter) than do traditional vias for micron-range SIS junctions. During deposition of the wiring layer niobium, voids tend to form inside these high aspect ratio vias.

The voids form due to sidewall deposition of niobium inside the via. If the aspect ratio is too high, accumulation of sputtered material on the via sidewalls prevents lateral deposition of niobium. As a result, the vias are only partially filled. Voids can degrade and even destroy SIS I-V characteristics because they are unlikely to support supercurrents. Maintaining a low via aspect ratio avoids this problem.

In order to reduce the aspect ratio, we needed to find an alternative insulator with a dielectric constant less than that of SiO. A lower dielectric constant allows the insulation layer to be thinner than an SiO layer while maintaining the same electrical thickness within the circuit. Xerogel, being a porous matrix of silica with a dielectric constant less than 2, is a suitable alternative. Air trapped within the pores of the silica matrix allows for the low dielectric constant [5].

Xerogel thin films are derived from Silbond, which is a suspension of silica in an ethanol solution. The silica is brought out of solution with the aid of a silane-decoupling agent such as SHTES (sulfhydryltriethoxysilane). In addition, SHTES promotes good adhesion between xerogel and gold. Silica materials tend to not bond well with materials that do not support a native oxide, such as gold. Since the SIS junction counter-electrode is topped with gold, it is necessary to promote good adhesion between gold and any subsequent insulation layer. SHTES contains a mercapto (thiol) group attached to an alkoxysilicate group. Since thiols form covalent bonds with gold, good adhesion between xerogel and the junction counter-electrode may be achieved [5].

To form thin films of xerogel, Silbond and SHTES are combined in-situ at a resist spinning station; after a 10 minute exposure to SHTES vapor, Silbond is dropped onto a wafer using a syringe. Once the Silbond is mixed with the SHTES, the silica drops out of suspension. The wafer is then spun, expelling any excess Silbond. The remaining ethanol is then allowed to evaporate in a controlled environment over an eight hour period. During this time, the ethanol is replaced by the ambient air and the silica matrix partially collapses. What is left after curing is a thin film of xerogel. The entire process is conducted at ambient temperature and requires no special equipment or high temperature curing. Film thickness is simply controlled by diluting Silbond with ethanol; larger dilutions result in thinner films. For instance, a 1:2.5 dilution of Silbond with ethanol results in a film thickness of around 140nm for a spin rate of 6krpm. Using this method of control, fairly uniform films as thin as 100nm have been achieved repeatedly. Thinner layers may be achieved using RIE etch-back techniques. This thickness, along with the low dielectric constant and reasonable processing requirements, makes xerogel a suitable candidate for use as an interlayer dielectric in SIS circuitry. By reducing the aspect ratio of the vias, high quality contacts between submicron junction counter-electrodes and upper level wiring layers are realizable.

IV. Conclusion

We have discussed three new techniques that are currently being applied to the fabrication of submicron-size SIS tunnel junctions at the University of Virginia. By combining the advantages of the focused ion beam, xerogel thin films and new metal masking techniques, high quality junctions can be realized. Such devices have applications in high frequency radio astronomy applications as well as in circuits designed for the study of quantum coherence.

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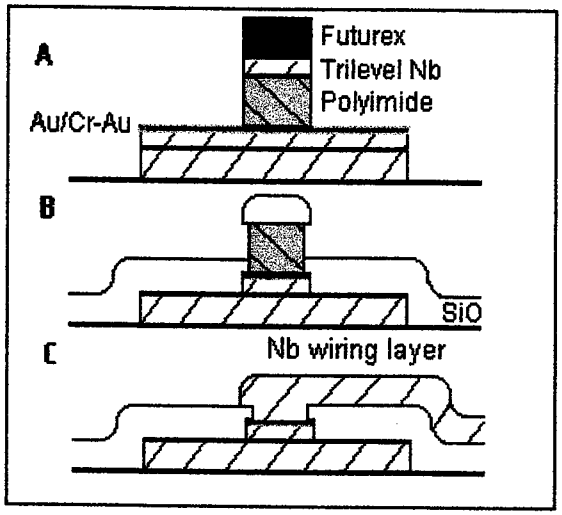


Figure 1. (A) Self-aligned trilevel (Futurrex/Nb/ Polyimide) sitting atop an unetched SIS junction. (B) SiO shown covering an etched SIS junction. (C)The SiO is then lifted-off from atop the junction, allowing the Nb wiring layer to contact the junction.

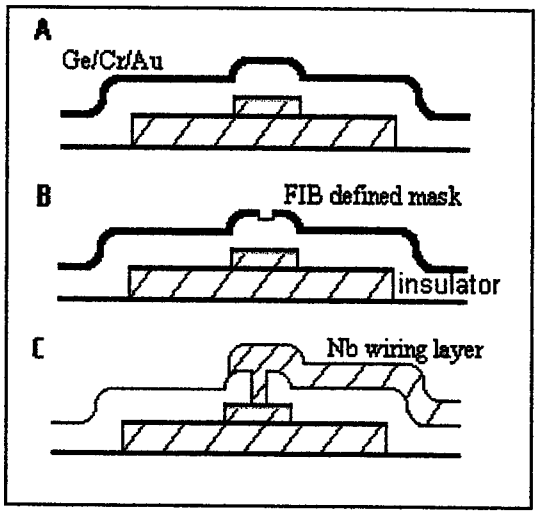


Figure 2. (A) An insulating material is layered directly on top of the junction followed by thin Ge, Cr and Au layers. (B) These metals are then patterned using the FIB. (C) A subsequent RIE of the insulation layer allows the Nb wiring layer to be contacted to the junction.

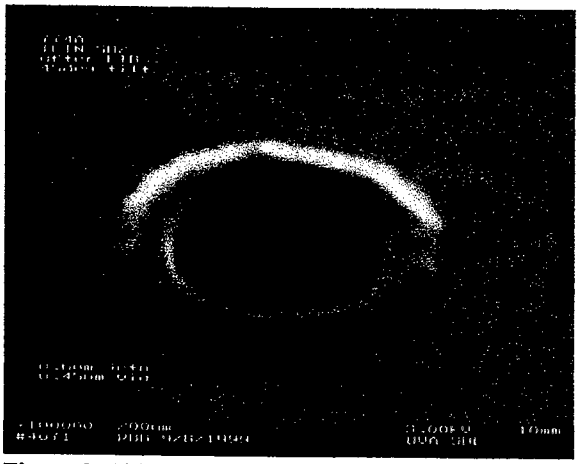


Figure 3. This is an SEM micrograph of a 0.16um^2 via milled through a Ge/Cr/Au metal mask above a 0.3um^2 junction. The exposed (dark) material is the insulating layer (SiO in this case).

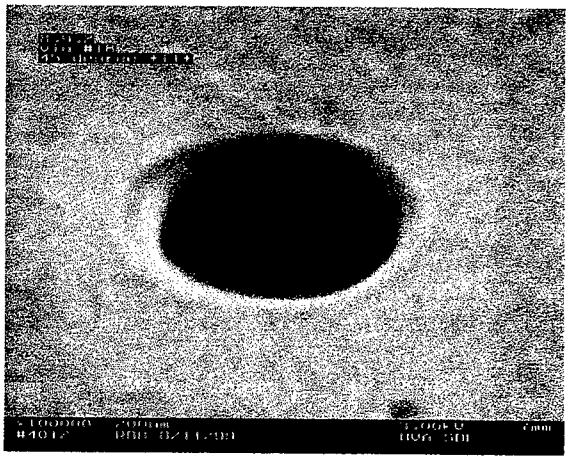


Figure 4. This is an SEM micrograph of a (test) via milled through a Ge/Cr/Au mask. Below the mask is 120nm of xerogel (dark material).

USING OF ALUMINIUMOXIDE FILMS FOR MILLIMETER WAVE AMPLIFIERS

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Abstract-In this report we presenting of results of the design and researching of millimetre-wave amplifiers which had been manufactured on aluminiumoxide substrates of new type. Design of the amplifier is run for the base of calculated parameters offered equivalent scheme and measured volt of ampere characteristics HEMT. Transition processes of determination of mode of amplification in HEMT amplifier have been simulated. Reached parameters of multistage amplifiers following: Gp=26 dB, NF=2.1 dB at f=28...31 GHz and Gp=24 dB, NF=2.4 dB at f=33.5...36 GHz.

I. INTRODUCTION

One of functional problems of modern radioelectronics is the creation of new devices with small level of own noise.

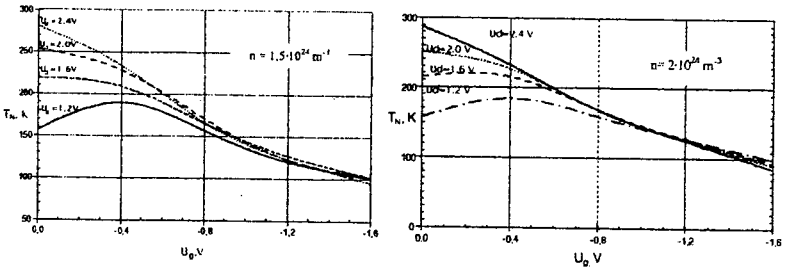
The minimisation of noise has both theoretical and practical importance. The theoretical importance consists in creation of the theory of noise on the basis of knowledge of mechanisms of its generation, and practical, is based on research of ways of noise reduction.

Using devices with small level of own noise the improvement of the power characteristics in telecommunication, radar tracking, navigating, photoreceiver and other systems is possible at the expense of improvement of ratio signal/noise in transmitting- receiving path.

In last, time alongside with field effect transistors with Shottky barrier (MESFET), the large attention is given to low noise field effect heterostructure transistors on the basis of such semiconductor materials as InGaAs. The first results of their application have shown improvement of noise parameters in comparison with the most widespread MESFET transistors on a basis GaAs.

Using three-element firm solutions InGaAs it is possible to increase frequency limit of gain and to create devices on the basis of new materials. Changing molar attitude In to Ga in the material is possible to receive the various characteristics.

The minimal equivalent noise temperature is 89K. Source-drain distance is 1.2 microns at gate length 0.25 microns. In the Fig. 1 the characteristic of the equivalence noise temperature versus a voltage on the drain and gate are submitted [2].



a) b)

Fig. 1. Equivalent noise temperature of the field effect transistor

The designed results coincide with experimental data [2], that testifies to the correctly chosen approach to the decision of the given task.

II. DESIGN OF THE MILLIMETERWAVE AMPLIFIER

After definition of noise temperature HEMT the important question is the low noise matching of the transistor in practical design of the millimetre wave amplifier. For the HEMT amplifier the low noise matching are close to the matching on maximum of amplification [1]. For decrease of parasitic parameters and real millimetre wave amplifier apply to increase of amplification and unpackage chips of transistors. In this case for calculations we used the equivalent circuit HEMT (fig.2).

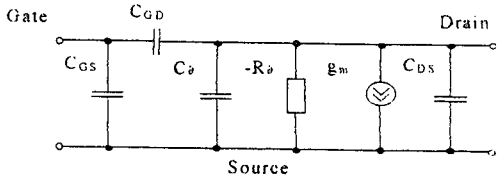


Fig. 2 The equivalent circuit HEMT

We have found, that maximal stage gain can achive more 29 dB.

Shown on fig.3 the stage are designed for the maximal stage gain. Input and output loading there were $Z_{in}=Z_{out}=50$ Ohm. However, practical realisation of the intensifying stage collides with gain more than 10 dB deal with problem of unsufficient stability.

Therefore, circuits stage amplification of the circuits have been limiting up to value 12 dB. Parameters of topology Z_1 = 142.5 Ohm, Z_2 = 50 Ohms, Z_3 = 50 Ohm, Z_4 = 15.5 Ohm, θ_1= 167.3°, θ_2=167.3°, θ_3= 167.3°,θ_4= 167.3° in this case were designed.

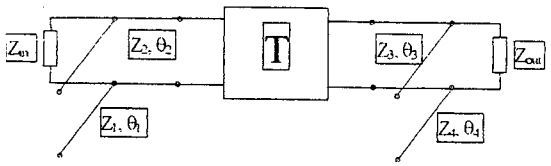


Fig. 3. The stage are designed for the maximal stage gain

Parameters of multistage amplifier also were calculated by analogical technique [2].

For few rustling transistor amplifiers of important parameter is the time of establishment of transients. In fig.4 the temporary dependencies of establishment of mode of amplification in HEMT are given.

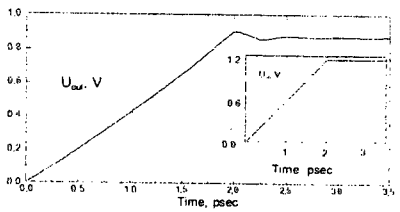


Fig. 4. Time of establishment of transients The modified field model HEMT into circuit with distributed parameters was used in investigations

So from the fig.4 it is visible, that the transients come to an end for one period equal 3 psec.

The model describing behaviour of electrons in transistors from their (carriers) by high mobility HEMT is necessary for account of microwave of devices. The complexity of physical processes does not allow in millimeter band of lengths of waves to apply analytical models, as they use the instant response of the drift characteristics on change of an electrical field. So, the account of inter valley carriage of carriers in InGaAs at least between two valleys is important. The most acceptable way of the analysis of microwave transistors with high electron mobility is using temperature model. The temperature model is based on the system of three equations: preservations of number of particles, balance of energy and balance of pulse.

Two valleys Γ- and L-type were taken into account in the modeling. Also it was accepted: length of structure is equal 1.2 microns, gate length is 0.25 microns, gate width is 200 microns, thickness of a layer InGaAs 35 microns, concentration doping impurity of layer InGaAs is 1.5 $10^{24}m^{-3}$.

In fig. 5 are shown calculated HEMT volt-ampere characteristics. It is visible, that the characteristics have failures of current, which size decreases with increasing gate voltage. The presence of failures is connected to redistribution of carriers between valleys with voltage on drain more than 0.5 V.

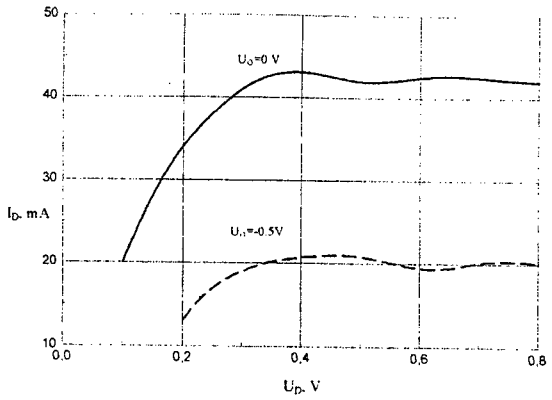


Fig. 5. Volt-ampere characteristic of HEMT

Temperatures distribution of Γ- and L-valley carriers along the channel (the point of beginning corresponds to middle of gate with maximum of current in the channel) have been modeled. The carriers are warmed up in under gate area, and temperature of carriers have changed no more than on 10 per cent in other part of the channel.

The important parameters describing own properties of the transistor is the steepness Gm and limit frequency of amplification F_{up}. Volt-ampere characteristic allow to expect steepness, which is equal to 50 mCm. However, at estimation F_{up} it is necessary to use dynamic meaning of steepness, which depends on meanings of parasitic resistance of source R_S and resistance of drain R_D.

$$G = Gm / (1 + Gm \cdot (R_S + R_D)) \tag{1}$$

For typical meanings R_S and R_D is equal to 3 Ohm, the dynamic steepness is equal to 40 mCm. The designed meanings there are not enough of alarm capacities gate-source C_{gs} and gate-drain C_{gd} are equal accordingly $6.56 \cdot 10^{-14}$ F and $4.5 \cdot 10^{-14}$ F. The calculated F_{up} is equal to 96 GHz. Negative differential resistance $R_д$ at frequency 36 GHz with zero bias on gate is equal to 222 Ohm. The negative differential resistance exists in the bands of frequencies: 26... 59, 92... 105, 188... 202 GHz. Last are caused by intervalley electron carriage in InGaAs. The modeling with negative resistance R_d of the equivalent circuit HEMT (fig.1) have shown more than double expanding of limit frequency of amplification of the transistor.

The results of the analysis of HEMT were used in parametrical synthesis of the single stage amplifier. The matching circuits of with input and output loads (Z_{in} = Z_{out}=50 Ohm) in represented stage have form of connections open of loop and piece of transmission line. The losses of the transmission lines (factor of attenuation) took into calculations of parameters is α= 0.11 dB/cm. On the fig.6 (curve 1) and fig. 7 (curve 2) the dependencies of gain G_p and input VSWR from frequency accordingly are shown at small signal. G_p is 29 dB at minimal VSWR=1.3.

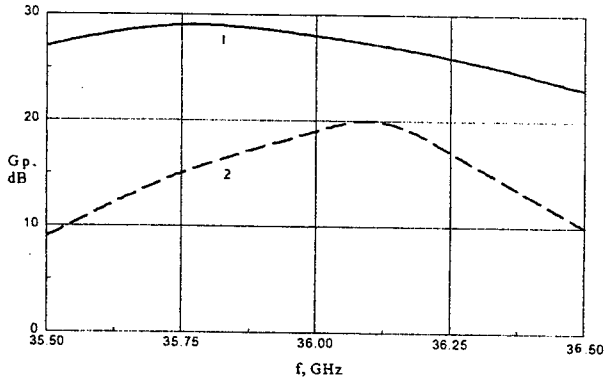


Fig. 6. Dependence of gain from frequency

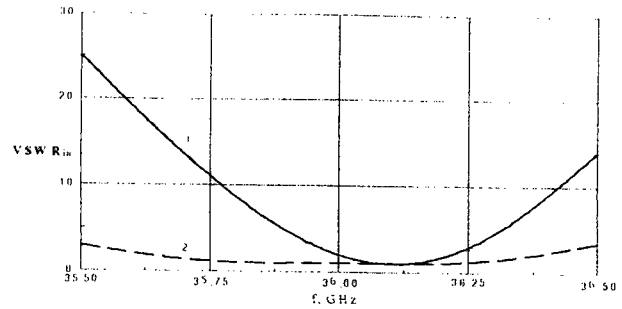


Fig. 7. Dependence of input VSWR from frequency

In a mode of a large signal with zero gate bias at 36 GHz with the help of the Fourie analysis are determined, that on the first harmonic the negative differential impedance can be presented as parallel connection of negative resistance and inductance, which have sizes 2127 Ohm and 0.38 nH ccordingly. In fig. 6 (curve 2) and fig. 7 (curve 1) the dependencies of gain G_p and input VSWR accordingly are shown at large signal.

The minimal VSWR is equal to1.08 at 36.1 GHz, and gain G_p achieves 20 dB. Value essentially differs from meanings calculated with amplification of small signals.

Thus, on the basis of temperature model is calculated volt-ampere characteristic of HEMT. Is shown, that the volt-ampere characteristic of HEMT has downfalls of current because of carry of carriers between valleys in InGaAs. The values of capacities C_{GS} and C_{GD} equal accordingly $6.56 \cdot 10^{-14}$ F and $4.5 \cdot 10^{-14}$ F, and steepness G are determined equal to 40 mCm. The limiting frequency of amplification equal 96 GHz is calculated. The negative differential resistance R_e at 36 GHz with zero gate bias is equal to 222 Ohm. The zones R_e are found out in the field of frequencies 26... 59, 92... 105, 188... 202 GHz, that more than double increase limit frequency of the HEMT. Is shown, that the representation of the static domain at large signal at the first harmonic as parallel connection of negative resistance and inductance equal accordingly 2127 Ohm and 0.38 nH, satisfactorily describes processes occurring in the transistor.

III. RESEARCH OF MILLIMETERWAVE AMPLIFIER

The increased requirements of reliability of millimeter wave devices lead to necessity of development and research of new types of dielectric substrates.

The devices based on free aluminumoxide films and strip transmission lines make a next amplifier.

In table 1 the parameters of multistage amplifiers on the basis of aluminumoxide substrates are given.

Table 1

The amplifier	Frequency band, GHz	Gain, dB	Noise factor, dB
1	28-31	26	2.1
2	33.5-36	24	2.4

The anodic oxidation electrochemical process of Al is the basis of the technology. This and photolithography able to produce all the important components of hybrid circuits.

The substrates with a high quality dielectric layer based on an anodic Al oxide with the following parameters: maximum dielectric layer thickness – from 5 to 2000 μm, dielectric constant - 4÷6, breakdown voltage is beyond 1000 V.

Interconnection multi-layer system based on Al and its anodic oxide with the following parameters: minimum track width and track spacing - 10 μm, Al track thickness - 3 μm, interlevel dielectric is Al anodic oxide, interconnection level number - up to 5.

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Characterization Techniques for Plasma Process Induced Electric Degradation in MOS Devices

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I. INTRIDUCTION

The plasma process induced damage to the gate oxide in metal-oxide-silicon (MOS) devices has become one of the major concerns for the ultralarge-scale integration (ULSI) processes [1-4]. This damage would degrade the yield and reliability of devices, which is generally attributed to the charging effects and is dependent on the area ratio of processed film to gate oxide (i.e., antenna area ratio) [1]. But some researchers studied the charging effects by using peripheral length intensive pattern of the etched film [2]. It is important to realize whether the area or peripheral length of antenna has dominant influence on the plasma charging effects. It is believed that the charging effect is mainly due to the local charge accumulation induced by the plasma non-uniformity [3]. Yet, a simple test structure for detecting this plasma uniformity is of lack. The device structure of MOS capacitor for characterizing the charging damage is generally the cover type, of which the gate oxide is wholly covered by the etched poly-Si films and the process is more simple. However, the actual structure in MOSFET is the uncover type, which means the gate oxide may be subjected to radiation exposure damage or photo-annealing [4].

In this work, we propose some promising techniques for characterizing the plasma poly-Si etching process induced electric degradation in MOS capacitors. By comparing the effects of area ratio and peripheral length of antenna, the plasma induced reliability degradation is dependent on the peripheral length of antenna but not on the area ratio of it. The plasma uniformity and charging current direction can be detected by the P/N or N/P bypassing diodes, which are connected between antenna and substrate. The plasma induced electric degradation in MOS capacitor with covered antenna type is more severe than that with uncovered one, indicating that the photo-annealing effect is more significant. The uncover type of MOS device should be used to characterize the plasma charging effects although it requires more complex processes.

II. EXPERIMENTAL

The MOS capacitors were fabricated on p(100) Si wafers with a diameter of 6 inches and resistivities of 15～25 Ω · cm by the conventional poly-Si gate process.

Oxide films with thickness of 26 Å were grown at 900℃ in dry O_2 by a furnace. The oxide thickness was measured using an ellipsometer (index=1.46) and were confirmed by the high-frequency capacitance-voltage (CV) method. Next, by the conventional low pressure chemical vapor deposition (LPCVD) method, poly-Si films 2500 Å thick were deposited at 620℃. Then, predeposition and drive-in of $POCl_3$ were performed on all samples at 875℃ for 22 min and 20 min, respectively. The sheet resistance of poly-Si was about 50Ω/□. The plasma etching of poly-Si was performed using a Electron Cyclotron Resonance (ECR) with the experimental conditions: Gas flow, Cl_2= 95 sccm, O_2= 2 sccm, HBr= 95 sccm; Gas pressure= 5 mtorr; Microwave power= 350 W, RF power= 35 W. Finally, after Al films 200 nm thick were evaporated onto the samples and patterned by lithography, the samples were annealed in N_2 at 400℃ for 20 min. The electric properties of MOS devices shown here are the time dependent dielectric breakdown (TDDB), which can reveal the latent damage induced by plasma process. Charge-to-breakdown (Qbd) and time-to-breakdown (t_{bd}) were measured at a constant current stress of -100 mA/cm^2. Over twenty capacitors were measured to show the Qbd and t_{bd} data.

III. RESULTS AND DISCUSSION

Figure 1 shows charge-to-breakdown (Qbd) of MOS capacitors with different antenna area ratios (AR) and identical peripheral length. There is no difference between these two samples. Some inconsistent results reported by other researchers before could be due to the different peripheral length accompanied with the various AR. It is therefore clear that the change of antenna area ratio can not be used to study the charging effects for the plasma poly-Si etching process.

On the other hand, inverse phenomena is observed in Figure 2, which shows Qbd of MOS capacitors with identical AR and different peripheral length. The Qbd values for the samples with long peripheral length are clearly reduced. So, the charging effects for the poly-Si etching process should be studied by using various peripheral length of antenna.

Figure 3 shows time-to-breakdown (t_{bd}) for MOS capacitors at various wafer location without or with P/N or N/P by-passing diodes under photoresist plasma ashing. It can be seen that lots of negative charges exist on the center of the wafer. Also many positive charges are accumulated on the edge of the wafer. The negative current stressing (gate injection) on the center of the wafer destroy severely the reliability of MOS devices. The charges and uniformity of plasma etching can be easily characterized by the P/N and N/P bypassing diodes.

Figure 4 shows t_{bd} for MOS capacitors with cover, uncover (with short peripheral length) and uncover (long peripheral length) poly-Si gate electrodes. The t_{bd} values for uncover types are clearly larger than those of the cover one. The charging effect induced

electric degradation in MOS capacitor with the cover type is severe, which is not the actual structure for MOSFET. Therefore, the plasma charging effect is overestimated by using the cover type. The uncover type of MOS device should be used to characterize the plasma charging effects although it requires more complex processes. The t_{bd} values for uncover type with long peripheral length are somewhat reduced, which might be due to the increased incorporation of detrimental species during subsequent device process.

IV. SUMMARY

Some promising techniques for characterizing the plasma etching induced electric degradation in MOS capacitors are proposed. As for poly-Si etching process, it is experimentally found that the plasma induced damage is dependent on the peripheral length of antenna but not on the area ratio of it. P/N or N/P diodes that are connected between antenna and substrate are fabricated to bypass the charging current during plasma process. From the simple parallel diode test structures, the plasma uniformity and charging current direction are easily detected. The plasma induced electric degradation in MOS capacitor with covered antenna type is more severe than that with uncovered one. This implies that the photo-annealing effect is more obvious for the ultra-violet (UV) light generated in this plasma etcher. It is noteworthy to use the uncovered antenna type for measuring the plasma damage, otherwise the plasma etching induced electric degradation may be over estimated.

ACKNOWLEDGEMENTS

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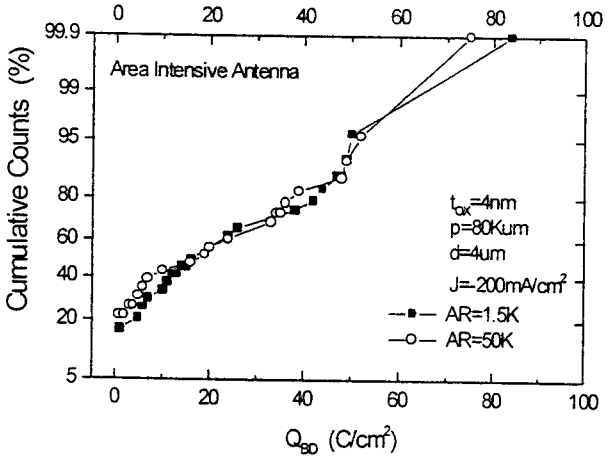


Fig.1 Charge-to-breakdown (Qbd) of MOS capacitors with different AR and identical peripheral length.

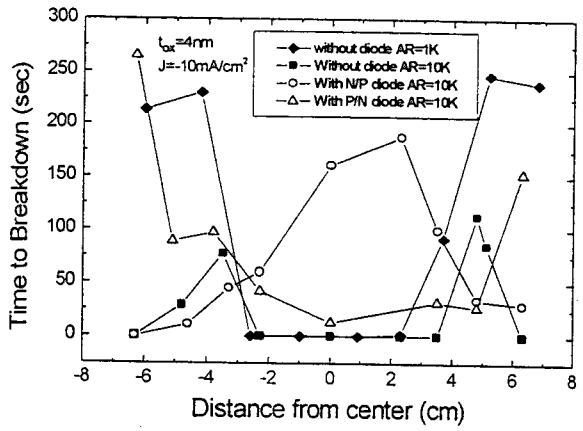


Fig.3 Time-to-breakdown (t_{bd}) in various wafer location for MOS capacitors without or with P/N or N/P by-passing diodes under photoresist plasma ashing.

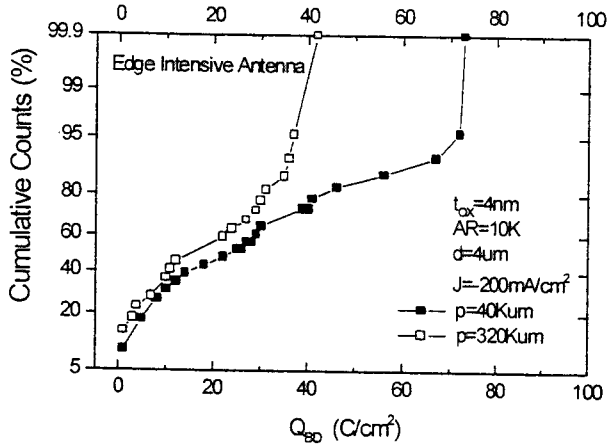


Fig.2 Qbd of MOS capacitors with identical AR and different peripheral length.

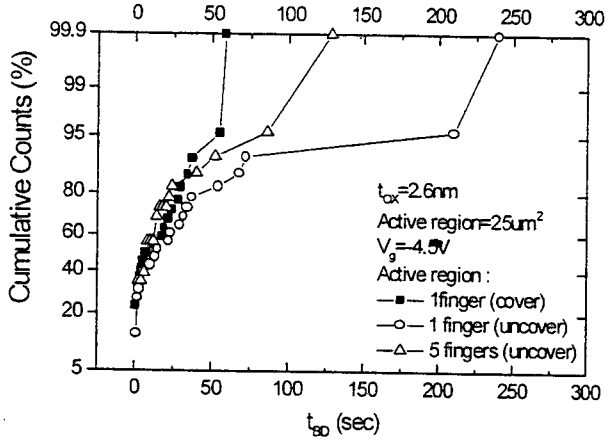


Fig.4 t_{bd} for MOS capacitors with cover and uncover poly-Si gate electrodes.

Current-voltage characteristics of heterostructures based on narrow-gap semiconductor ZnCdHgTe: experiment and numerical simulation.

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1.Introduction.

The numerical modeling is seemed to be interesting as a helpful tool good for prediction of different features of studied structures and processes. This abstract reports first results of computer experiment carried out for p-isotype heterostructure ZnCdHgTe/CdTe.

Semiconductor solid solution ZnCdHgTe (ZCMT) has been proposed as a new perspective material for different applications for optoelectronics devices working in wide temperature range (77-290 K) and wave-length region 4-12 μm. To avoid the sufficient mismatch of contacting materials lattice parameters ZCMT epilayers were manufactured on CdTe and ZnCdTe monocrystalline (111) substrates by the modified LPE technology [1-2]. However, performed structural studies have demonstrated the appearance of the as-grown epifilm and substrate lattice parameters mismatch in range of about 0.32÷1.29 % which in turn causes mismatch deformation generating the surface states band forming at the heterointerface plane (Fig.1). These states act as recombination centres and significantly change the band-gap diagram of the heterojunction and sufficiently effect on the current transfer processes. The I-V and C-V investigations performed for the monitoring of electrical properties have shown examined p-isotype heterostructures $Zn_xCd_yHg_{1-x-y}Te$/CdTe ($0<x\leq0.20$, $0.07\leq y\leq0.0.18$) have demonstrated the current-voltage and capacitance-voltage dependencies (Fig.2,a,b) similar to ones of abrupt heterojunctions with a sufficient effect of the surface electron states localized in the space-charge region.. In particular, the ideality factor n of both forward and reverse sections of current-voltage characteristic is more larger than 1 which indicates on the dominant trap-assisted tunneling process..

2.Experimental details.

Galvanomagnetic studies have shown the as-grown epifilms of 8-25 μm thickness were characterized by both p- and n-type of conductivity. Surface examinations have revealed the inhomogeneous microrelief of .the epilayer surface with an element size of about 0.1 μm . The electrical area of the examined samples was estimated to be 4-8 mm^2.. The measurements accomplished at 290 K have exhibited the two-section current-voltage dependence and a straight $C^{-2}=f(V)$ characteristic (Fig.2,a,b).

3. The energy-band diagram construction.

In order to clarify what represents the obtained heterostructure from the point of view of energy parameters the band diagram has been constructed according the theoretical model [3] developed for heterojunctions with close dielectrical constants of contacting materials (Table 1). The main equations for the energy-band diagram parameters calculation are: ,

$$\Delta E_c = \Delta E_v + kT\log(N_{cA}N_{vB}/N_{cB}N_{vA}) - (\Delta E_{ex} + \Delta E_{hxc}) - 2(\Delta E_{im} + \Delta E_b \quad (1) \qquad (1)$$

$$\Delta E_v + \Delta E_c = \Delta E_g. \qquad (2)$$

Here ΔE_m (m=c,v,g) are the conduction band discontinuity, valence band discontinuity and the difference between the band-gaps of the contacting materials, respectively, N_c, N_v stand for the effective state densities in c- and v-bands of both materials (A-index relates to CdTe, B-index relates to ZnCdHgTe) The third term in (1) accounts the effective electron-hole exchange-correlation energy:

$$E_{xc}\approx -2.5\cdot10^{-7}[1 + 0.7734y\log(1+y^{-1})N^{-1/3}\varepsilon^{-1}, \qquad (3)$$

$$y\approx 5.6\cdot10^{8}[m^*/\varepsilon)N^{-1/3}, \qquad (4)$$

where N and m^* denote the effective states density and effective mass of electrons or holes in both materials, the final term takes care of the image forces and heterointerface dipole bond energy due to interaction of dangling bonds:

$$E_{im}(A)=(\varepsilon_B-\varepsilon_A)e^2/\pi\varepsilon_0(\varepsilon_A + \varepsilon_B)\varepsilon_A d_B, \qquad (5a)$$

$$E_{im}(B)=(\varepsilon_B-\varepsilon_A)e^2/\pi\varepsilon_0(\varepsilon_B + \varepsilon_A)\varepsilon_B d_A \qquad (5b)$$

$$E_b(A) = e^2/4\pi\varepsilon_0\varepsilon_A d_B,\ E_b(B) = e^2/4\pi\varepsilon_0\varepsilon_B d_A, \quad (6)$$

where $d=(3)^{1/2}a$, a is a lattice parameter of the corresponding material. The energy spectrum of the surface electron states had been calculated according the method described in [4]. The following numerical simulation procedure had been performed with taking into account the values. of the calculated band-gap diagram.

4.The current transfer mechanisms.

As we have mentioned above the structural studies performed for as-grown ZnCdHgTe epifilm have exhibited quasi-3D symmetrical gaussian distribution of the surface inhomogeneities characterized by the typical elemental size of about 0.1 μm, in other words, this value is larger than Debye screening length (L_D consists of about 0.07μm) [5]. Accounting carriers generation in the space charge region and appearance of surface electron states band E_{ss}(see Fig.1) the expression for the total tunneling current can be written as follows:

$$j \sim \int \exp[-4(m^*)^{1/2}(Ess)^{3/2}/3e\hbar F] \exp[-(E-E_{ss})/\Delta^2]dE, \quad (7)$$

where m* stands for ZnCdHgTe hole effective mass , F is an electric field strain in the heterojunction region, Δ is a tunneling parameter caused by the surface relief of the epifilm, $\Delta << E_g$(here Eg denotes the forbidden gap of ZnCdHgTe).[5]. Thus, noting the experimental current as

$$j=eaN(\mu_h kT/\tau e)^{1/2} j_s \exp[-(4(m^*)^{1/2}(E_{ss})^{3/2}/3e\hbar F) + (m^* E_{ss}\Delta^2/e^2\hbar^2F^2)], \quad (8)$$

(here μ_h and τ are holes mobility and recombination life-time in ZnCdHgTe, j_s is a saturation current determined from the experimental data) we calculated the value of Δ: $\Delta \approx 52$ meV. On the other hand the current- voltage dependencies observed experimentally appear not only as the functions of the applied voltage but they are also determined by the value of band-gap or conductance band discontinuity and the energy level of the surface electron states at the heterointerface. So the principal expression for the experimental I-V characteristics numerical modeling can be written as follows:

$$J \sim f(\Delta E_v)f(E_{ss})f(M.P.)V^m, \quad (9)$$

where,M.P. stand for CdTe substrate parameters (see Table 1), m determines the change of current-voltage function, that is: $j \sim V^2$ at 0-2 V and $j \sim V^3$ at 2.1-5.0 V. Such a functional dependence gives a good description of experimental results obtained for abrupt p-p-heterostructures at applied voltage 0-5 V in case of prevailing tunneling currents and currents limited by the space charge region [6].

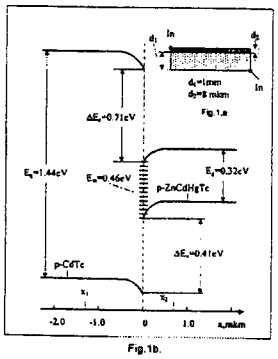


Fig.1b.

Fig.1,a. The examined sample geometry; fig.1,b plots the studied heterojunction one-dimensional energy-band diagram accounted only the contacting materials parameters.

Parameter	ZnCdHgTe	CdTe
Dielectric constant	16.3 ε_0	10.9 ε_0
Electron effective mass	0.01 m_0	0.11 m_0
Hole effective mass	0.55 m_0	0.35 m_0
Lattice parameter a, nm	0.6392	0.6478
Band-gap E_g, eV	0.32	1.44

Table 1. Some parameters of the investigated heterostructure compounds

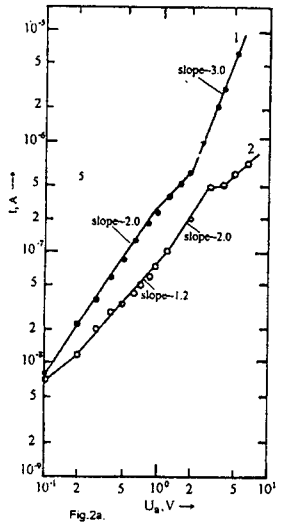
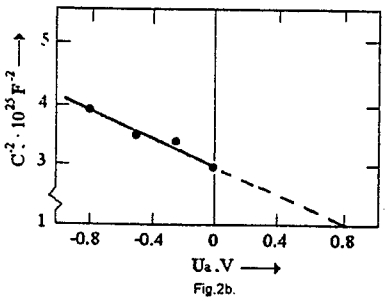


Fig.2, a. The experimental I-V characteristics: curve 1 is a forward section and curve 2 is the reverse one.T=290 K.

Fig.2,b. The experimental C-V dependence measured at 290 K; the test signal frequency f = 1 kHz.



5. Results of computer experiment.

Fig.3 plots the experimental and calculated current-voltage characteristics of the examined heterostructure. It is shown the theoretical curve reveals a good coincidence with the experimental data at applied voltage 0÷1.1 V in both forward and reverse directions; this section is fairly described by the expression given below:

$$I_1 = A \exp(-\Delta E_v/kT) e\tau\mu_n \mu_p N V^2 L^{-3} = BV^2, \quad (10)$$

where A is an electrical area of the sample, μ_n, μ_p are electron and hole mobilities of the epilayer, τ is a recombination life-time in ZnCdHgTe , N is a concentration of charge carriers localized in the space-charge region from the substrate side, L is a part of the space-charge region localized from the substrate side (both N and L values were calculated basing on capacitance-voltage measurements).

The observed discrepancies between experimental and calculated current values at 1.15÷2.0 V are believed to be caused by the influence of ZnCdHgTe epilayer surface microrelief [6].

The forward section of current-voltage characteristic at 2.1-5.0 V can be approximated as follows:

$$I_2 = AX \exp[-(\Delta + E_{ss})/kT] \varepsilon_0 \varepsilon_s \tau \mu_n \mu_p V^3 L^{-5} = DV^3, \quad (11)$$

where X is a tunneling transparency coefficient, Δ was determined in Secion 4.

The tunneling transparency coefficient value has been calculated in assumption that the potential barrier for the majority charge carriers can be described as an aggregate of microbarriers forming by the epifilm surface inhomogeneities. Thus, according [7] the triangle potential barrier approximation gives the following expression for X (the trap-asisted tunneling occurs in the surface states band E_{ss}):

$$X = \exp\{-[(4d/3\hbar)(2m^*)^{1/2} [(U-E_{ss})^{3/2}/U] + (E_{ss}/kT)]\}, \quad (12)$$

where d is a width of the barrier (is assumed to be equal approximately 0.09 μm), U is the barrier height (determined from the experimental measurements), m* stands for the hole effective mass of the solid solution ZnCdHgTe.

The differences observed in that case (see Fig.3, upper sections of the curves) are possible due to appearance of so-called exceeding tunneling currents as predicted by the theory [8].

6.Summary.

Numerical simulation of p-isotype heterostructure ZnCdHgTe/CdTe current-voltage characteristics performed at room temperature have been shown the quadratic ($j_1=BV^2$ at 0÷2 V) and cubic ($j_2=DV^3$ at 2÷5 V) I-V dependencies where coefficients B,D are strongly depended on the peculiarities of ZnCdHgTe epilayer surface and energy parameters of the examined heterostructure as an entity. The results of the computer experiment demonstrate the possibility of manufacturing active elements for charge-couple and tunneling devices.

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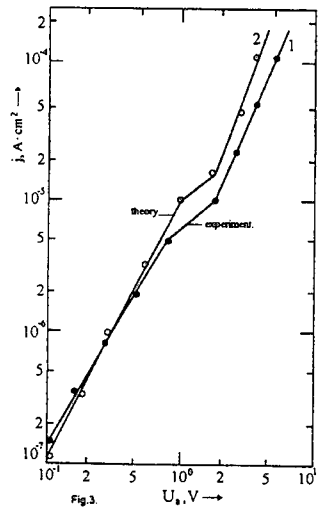


Fig.3. Experimental (curve 1) and calculated (curve 2) current-voltage characteristics of the p-isotype heterostructure CdTe/ZnCdHgTe, T=290 K. Above the applied voltage V>1.1 V the calculated current values are slightly larger than experimental ones due the epilayer potential relief influence.

Effect of Ni-silicide Boundary on the Leakage Current of Poly-Si TFT's Fabricated by Metal Induced Lateral Crystallization

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1.INTRODUCTION

Polycrystalline silicon TFT's with high mobility and low leakage current are needed for active matrix liquid crystal displays (LCDs) with integrated peripheral circuits and pixel transistors. In our previous report, a metal induced lateral crystallization (MILC) process was introduced. This process, which is attracting a lot of attention, allows amorphous silicon thin films to be crystallized at a temperature below 500℃ [1]. While the resulting TFT's have shown excellent device properties, they are less ideal in others such as high leakage current.

Since metal induced crystallization (MIC), instead of MILC, occurs in the source and drain regions of conventional MILC TFT's, continuous MIC/MILC interfaces [2],[3] are self-aligned to the edges of the gate electrode and a Ni-silicide ($NiSi_2$) boundary is also formed at the center of channel. The high leakage current of MILC poly-Si TFT's was drastically decreased by electrical stress in both n-channel and p-channel TFT's, fabricated by MILC [4]. The decrease of leakage current by electrical stress is due to the passivation of trap states in the drain junction region overlapping the MIC/MILC interface by injected carriers [5]. Symmetric Ni-offset deposition method, as shown in Fig. 1(a), could exclude MIC/MILC interfacial boundaries from the edges of the gate [2]. However, Ni-silicide boundary remained at the channel, therefore, asymmetric Ni-offset at either the source or the drain-side as shown in Fig. 1(b) was proposed to extract the nickel-silicide boundary [6][7].

In this work, considering symmetric and asymmetric Ni-offset MILC TFT's, the effect of electrical stress on the leakage current was investigated.

2.DEVICE FABRICATION

Self-aligned top gate n-channel TFT's were fabricated below 500℃. A 1000Å amorphous-Si film was deposited by plasma enhanced chemical vapor deposition at 300℃ on corning 1737 glass. After patterning the a-Si layer to form the active islands, a 1000Å layer of silicon oxide and a 3000Å thick Mo gate electrode was deposited by electron cyclotron resonance PECVD (ECR-PECVD) and RF sputtering. Photoresist (PR) mask for Ni-offset deposition was patterned symmetrically or asymmetrically after the gate patterning. A 20 Å-thick Ni thin film was deposited on the surface of the TFT's and then Ni film on the offset mask was removed by lift-off method. Details of the device fabrication process are presented elsewhere[2]. The transfer characteristics and the stress effects were measured with a HP 4140B pA meter/DC voltage source.

3.RESULT AND DISCUSSION

Fig. 2 shows typical transfer characteristics (Id-Vg) of symmetric Ni-offset MILC (SO_MILC) TFT's and asymmetric Ni-offset MILC (ASO_MILC) TFT's. At off-state region, anomalous leakage current increase is observed in SO_MILC TFT's. The high leakage current can be related to the Ni-silicide boundary in the channel, which generate localized trap states. Although the microscopic origin of such trap states is not clear, it could be speculated that they could arise by lattice distortion and impurities such as Ni-silicide and Ni ion.

In Fig. 3, variations of leakage current recorded during bias-stressing at the off-state region

(Vg=-10 and Vd=0~20V) are shown. Evidently, appreciable leakage current reduction of SO_MILC TFT's occurs at critical drain voltage. With constant gate bias (-10V), the leakage current of SO_MILC drastically increases as the drain bias increases and the current decreases over critical drain voltage (8V). This implies that the Ni-silicide boundary in the channel generates leakage current and trap states in the Ni-silicide boundary which could be passivated by electrical stress such as (Vg=-10 and Vd=8V).

In Fig. 4, variation of the leakage current measured during constant gate and drain biases (Vg=-10 and Vd=10V) are shown with stressing time. Clearly, as the stressing time is increased, the current of SO_MILC TFT's decreased and was finally saturated to the value of ASO_MILC TFT's. However, leakage current of ASO_MILC TFT's observed in Fig. 3 and Fig.4 does not change for electrical bias-stressing. Therefore, the defect-induced leakage current of SO_MILC TFT's decreases with specific bias conditions. However, as shown in Fig. 5, when the stressed TFT was post-annealed in the furnace, leakage current recovered as annealing temperature elevated. This phenomenon occurred after slight reduction around 100~150℃. It was found that the stress effect disappeared at 350℃. Fig. 6 shows that the leakage current of ASO_MILC TFT is lower than that of the unstressed SO_MILC TFT and it is not affected by electrical stress. This can be attributed to the fact that trap states introduced by the Ni-silicide boundary have been removed by the asymmetric Ni-offset method.

4.CONCLUSION

The defect-induced leakage current of SO_MILC TFT's can be effectively decreased after electrical bias-stressing (Vg<0, and Vd>0). With constant gate bias-stressing (Vg<0), stress effect appeared at specific drain voltage higher than critical value. However, when the stressed TFT was post-annealed in the furnace, the stress effect disappeared as annealing temperature elevated. Furthermore, asymmetric Ni-offset MILC method was proposed to improve the electrical properties of poly-Si TFT's. Since the Ni-silicide boundary defect was removed at channel, ASO_MILC TFT's showed the reduced leakage current.

ACKNOWLEGEMENT

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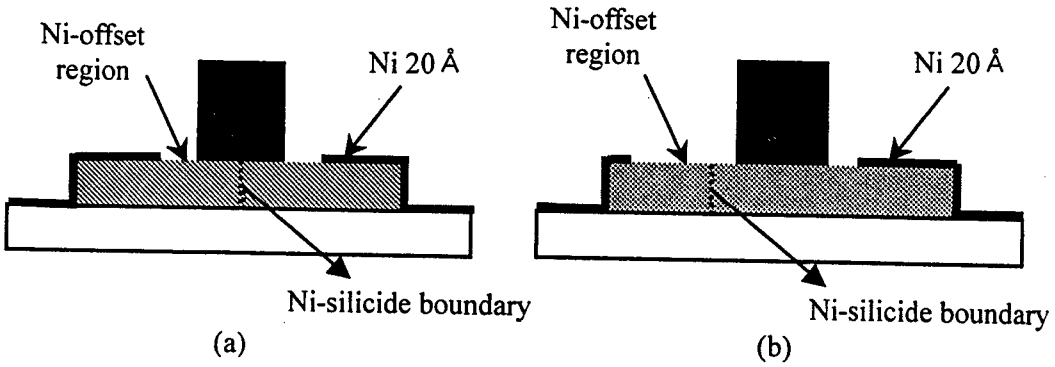


Fig. 1. Schematic diagram of symmetric Ni-offset TFT and asymmetric Ni-offset TFT.

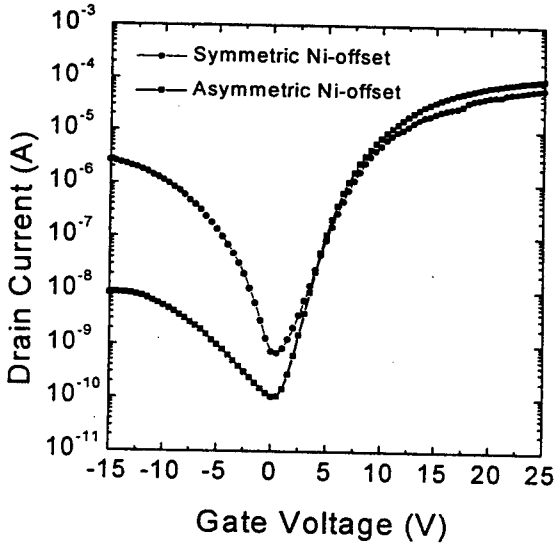


Fig. 2. Id-Vg characteristics of symmetric Ni-offset TFT and asymmetric Ni-offset TFT.

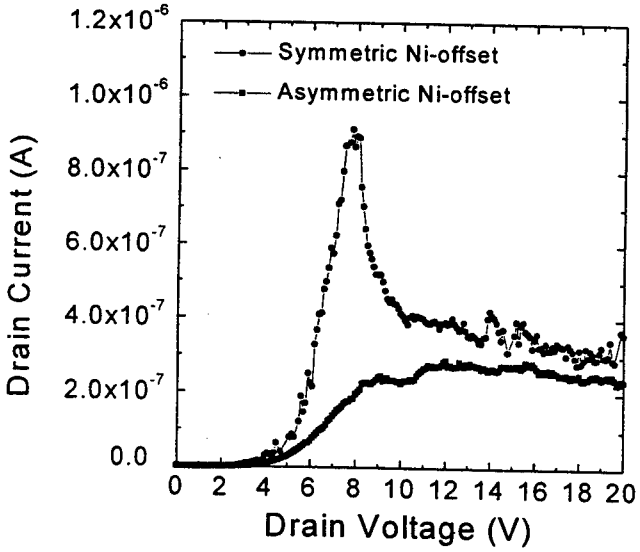


Fig. 3. Variation of leakage current during bias-stressing at off-state region (Vg= -10V and Vd= 0~20)

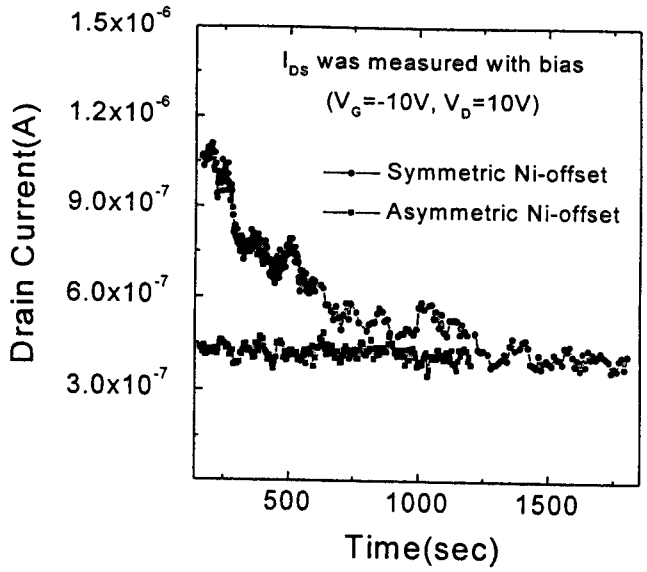


Fig. 4 Variation of leakage current during constant gate and drain voltage (Vg= -10V, Vd= 10V)

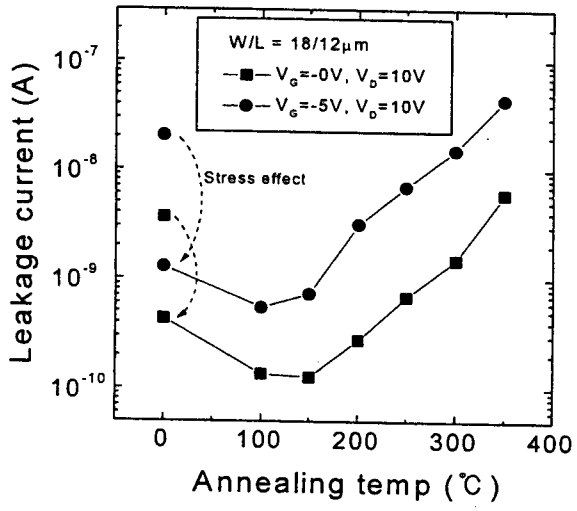


Fig. 5 The variation of leakage current with annealing temperature. (Annealing condition: H_2 ambient, 10minute at each temperature. Leakage current was measured at V_G=0, V_D=10V and V_G=5, V_D=10V.)

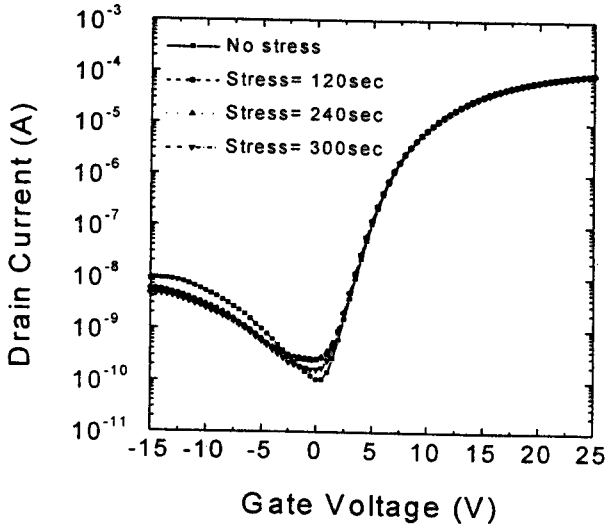


Fig. 6. I-V characteristics of asymmetric Ni-offset TFT. (W/L=20/8, Vd=5V)

Investigation of the ESD induced latch-up failure of RS- 232 data transceivers in telecommunication systems - A case study

by

V.Lakshminarayanan *,A.K.Manoj Kumar **,D.V.Raghava Rao***

Abstract

Electrostatic Discharge (ESD) is a major cause of failure of electronic devices which affects the reliability of electronic systems.With the increasing trend towards miniaturization in electronics, device size and thickness of layers have been reducing over the years,and this makes higher density devices more susceptible to ESD damage even at low values of ESD.

There are many sources of ESD - man-made,machines and natural sources such as lightning.Lightning causes charge propagation from atmosphere to terrestrial objects during a discharge.Telecommunications systems are the worst affected by such discharges and every year colossal losses are incurred by the telecom companies due to failure of equipment and down time losses.Overhead open wire telephone lines are easy targets for lightning discharges.

CMOS devices are especially susceptible to damage due to ESD.This is due to the build-up of charge in the parasitic capacitance in the device.Any defects in the oxide material at the atomic level will reduce the dielectric strength of the layer and make the device susceptible to failure due to electrostatic voltages.A few simple precautions taken in storage,handling ,assembling and appropriate design of circuits can minimise the effects of damage due to ESD.Devices can get damaged due to ESD due to electric field breakdown,thermal overstress due to electrical overstress,and latch-up in the internal structures leading to device damage.ESD can cause latch-up in ICs and CMOS devices are more susceptible to this type of failure due to the presence of pnpn structures in the device.Under latch-up conditions,the device becomes a short circuit across the power supply and ground,and this will cause flow of high currents,Electrical Overstress and damage to the device.A common ESD problem encountered in electronic systems is the failure of communication interface devices such as RS -232 drivers and receivers.ESD damage arises in such devices due to ESD pulses propagating through cable interconnections which are frequently handled by human operators and due to cables coming into contact with charged surfaces through unterminated connectors.The frequency of these ESD pulses goes into the GHz range and at these high frequencies,PCB traces and small pieces of cables act like antennas for receiving these interfering signals.

The case study presented in this paper presents an example of RS-232 device failure caused by CMOS latch-up.

Brief details of the analysis :

Failure of the data transceiver IC was occurring frequently especially during lightning discharges.Large-scale charring of the IC and the PCB underneath the device used to occur (see photograph 1). To identify the cause of the failure,monitoring of the power supply and input terminals of the RS 232 transceiver device,during the periods of heavy lightning was carried out using a recording instrument.The waveforms recorded showed short duration voltage transitions at the inputs of the transceiver device and supply pins during the occurrence of lightning discharges. Lightning discharges induce voltage disturbances on the power lines,and these propagate to the float rectifiers and to the device pins through the power supply ; very narrow voltage spikes cannot be filtered out or eliminated by conventional filtering techniques.

contd...

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In addition,lightning discharges induce voltage transients on open-wire telephone lines and these propagate to the line card circuits in the case of poorly protected line circuits.These voltage transients propagate through the line card - motherboard connections to the RS 232 data inputs of the device,i.e., into the gate of the parasitic thyristor,causing the thyristor to get latched into an ON state.Thus the above two mechanisms exist for latch-up conduction of the RS 232 device due to parasitic thyristor action,in this case. Once the thyristor is turned ON,the very low impedance of the device between the anode and cathode terminals under this condition presents a virtual dead short between the power supply and ground,causing a large current flow and high levels of Electrical Overstress (EOS) in the device. The higher temperatures caused by the heat dissipation initially causes increase in the carrier mobility and greater avalanche multiplication of carriers,aided by the higher electric field conditions (caused by the absolute difference of voltage between +12V and -12V used for the device). This EOS induces thermal overstress leading to intense heating with the following consequences - melting of metallizations in the device structures,heating of the device due to heat dissipation,melting of the plastic encapsulation and cracking of the package.Since a latched thyristor under conduction will continue to conduct until the power supply is removed,this process continues and ultimately leads to the charring of the device,and the PCB underneath the device also gets over-heated and charred.Thus the latch-up process ultimately leads to the destruction of the device by thermal overstress.Hot spots especially around the pins of the chip indicate the large scale heat transfer from the die to the leads. The enclosed photographs reveal the extent of damage observed.Since CMOS devices are prone to parasitic pnpn structures due their construction,and also sensitive to ESD,the failure observed in the case of the CMOS RS-232 transceiver has been found to be due to ESD induced latch-up of the device.

To gain an insight into the causative mechanisms which trigger charring of the device,the internal structure of failed devices was analysed.The techniques used for internal examination were IR microscopy after back- polishing in some cases and high magnification optical microscopy of some of the decapsulated failed devices.Examination revealed oxide layer breakdown in some failed samples and charring in some cases.The device is fabricated using CMOS technology.CMOS devices are prone to latch-up.The latch-up occurs due to parasitic pnpn structures occurring in the device due to the method of construction .Such parasitic structures do not interfere with the normal device operation as long as the the pnpn thyristor is in the OFF state.When latch-up occurs,the CMOS circuit behaves like a short circuit across the power supply.The exact mechanism of latch -up due to these voltage transients is the enabling of parasitic pnpn structures into conduction due to the voltage transients. Under normal conditions,the p-n junctions in the chip are all reverse-biased.Under some conditions such as voltage overshoot on an output terminal,ESD voltage appearing on an input lead,or application of signal to an input before application of power to the device,the junctions get forward biased.In other words,any voltage transient,caused for example by ESD,voltage surge,or a noise pulse,coupled into the device input or output can trigger the parasitic SCR into conduction by causing charge injection by triggering a regenerative process.Such an ESD voltage transient can be caused by lightning discharges and these voltage transients could propagate into the device through the device inputs or power supply pins.The triggering of the SCR structure causes a large current flow from V_{DD} to V_{SS} pins of the chip.Once the parasitic SCR is turned ON,it provides a low resistance path between the power supply and ground through the device.The current is quite large under these conditions and this leads to abnormal heat dissipation in the device due to thermal overstress.The excessive thermal overstress causes the plastic encapsulation to heat up and crack (see photograph 1).The heat transfer to the IC pins from the die causes temperature rise of the glass epoxy laminate of the PCB to the extent of charring.The examination of the failed devices,study of the instrument recordings and its correlation to the failure mode of the device confirms latch-up as the cause of failure.Photograph 2 shows the details of the damage observed at the die level on decapsulating the device.

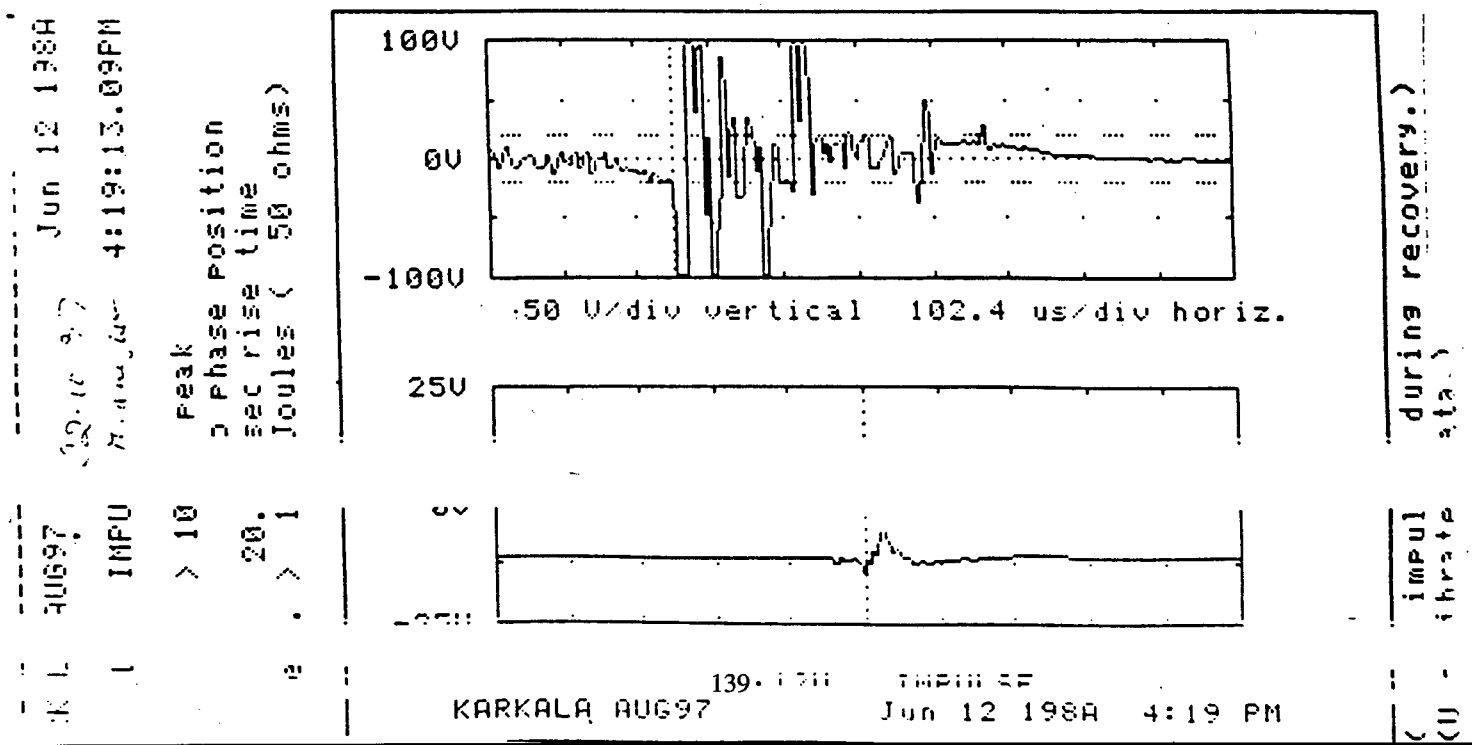
Conclusion :

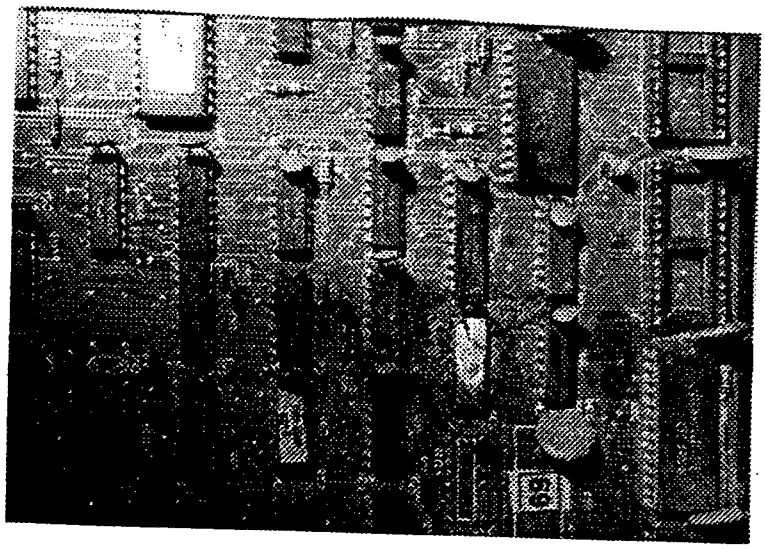
The device which was failing due to latch-up was being used in a number of cards in the system and it was not possible to redesign the product which was already under production for many years.Hence the problem was solved by replacing the RS 232 transceiver by a pin-compatible device based on a better technology and having built-in ESD protection features.The solution has been implemented and no failures have occurred after implementing the solution.

References (Key references are given below ; full list will be given in the final paper) :

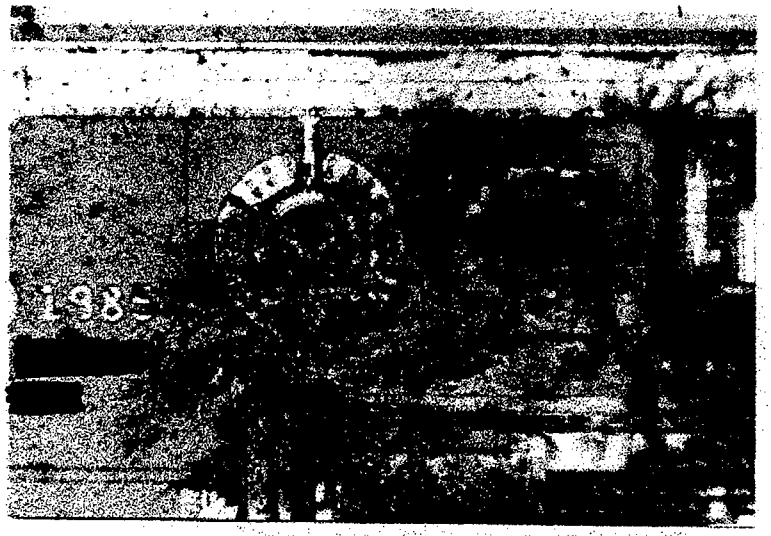
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(More details of the circuit level and device level analysis,mathematical modelling,etc. will be given in the final paper.)





Photograph 1 : Charring of the RS 232 transceiver observed in the card during occurrence of lightning discharges.



Photograph 2 : ESD induced latch-up has caused thermal overstress in the RS 232 device.Inside view of the chip.

DIELECTRIC RELIABILITY:

LIFETIME PROJECTION FROM TDDB DATA FOR THICK OXIDES

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ABSTRACT

This paper deals with the extensive characterization of dielectric films, ranging from 20 to 65 nm in order to study thick oxide reliability. It has been investigated with the time-dependent-dielectric-breakdown (TDDB). TDDB tests are conducted under constant current injection. We Assume that the logarithm of the median time-to-failure, ln(t_{50}), is described by linear electric field dependence. A generalized empirical law for the long-term reliability of the dielectric, taking into account the applied electric field and the dielectric thickness, is proposed.

1. INTRODUCTION

Today, power integrated circuits are developed and it's necessary to qualify the integrity and the reliability of thick dielectrics. These dielectrics have two essential functions in the device :

- accomplish a metal-insulator-semiconductor (MIS) function
- insulate the conductors from one to others.

Until today, thin SiO2 wearout and breakdown have been and continue to be the subject of many studies. As gate dielectrics are getting thinner (< 10 nm) with aggressive scaling down of the device geometries, the long-term reliability and integrity of the oxide layers are becoming a primary concern. However, because of needs for the functional integration of the power, that is a new concept, for the ASD™ (Application specific Discrete) products, industry must guarantee a certain lifetime without failure of the MIS (Metal Insulator Semiconductor) structures with oxide thickness from 20 to 1000 nm under normal condition.

Thus, our work goes against the current tendency of the scientific community, by studying the reliability of thick oxides. The aim of our work is to obtain a law, allowing to determine the lifetime of MOS devices, valid for a very wide range of oxide thickness.

The reliability of MOS devices results from the breakdown statistical studies after a strong charge injection in the dielectric. It is acquired that the thick oxides quality is worse than the one of thin oxides, under a significant field (> 8 MV/cm). But what does happen for a use under a nominal field, typically 4 MV/cm? That is the question we are going to answer in this paper.

Since the TDDB process of the gate oxide is believed to obey the thermodynamic model, stress field accelerated testing has been performed in order to determine and to verify the oxide reliability. This paper deals with the extensive characterisation of oxide thicknesses between 20 to 65 nm using multiple wafer fabrication lots

2. EXPERIMENTAL

All experiments were performed on n-type, Si/SiO_2/poly-cristalline-Si, MOS gate oxide test capacitors produced in an industrial process. Thermally grown oxides with areas of 1 to 5 mm² and thicknesses are 20, 35, 41, 55 and 65 nm were tested. The oxide test structures consisted of no LOCOS edges and had no poly-gate silicidation. The poly gates were degenerately doped and gate and substrate contacted via Aluminium pads on field oxide.

TDDB data were obtained by injecting a constant current density to the MOS structure. All measurements were performed in accumulation with a substrate injection (positive gate) at room temperature. So, the entire applied electric field appears across the oxide. The electric field is measured at time zero when the current density is injected at the Fowler-Nordheim regime. The time-to-breakdown is recorded when the voltage across the MOS capacitor drops suddenly, to a value of few volts. The measurement samples consisted of 82 capacitors for each statistical data, equally distributed across a 5-inch wafer that contains 328 capacitors. All measurements were performed with Keithley Parametric Test System and a half-automatic KarlSuss Wafer

Prober. A Hewlett-Packard workstation controls the measurement system, records the data, and performs statistical analysis. The control of instruments is realized from the LabVIEW software tool.

3. RELIABILITY PREDICTION

From the measurements, a statistical exploitation of the breakdown is undertaken. After having performed the measurements as presented in the foregoing paragraph, we obtained for each value of the injected current density, the initial electric field and the time-to-breakdown. Due the to the great number of samples tested, we can define the median time-to-breakdown (t_{50}), as being the cumulated probability so that 50% of the capacitors tested are broken. By performing that for each studied dielectric thickness, we obtain the results presented in figure 1.

The oxide wearout properties of the generated data show that the logarithm of the median-time-to-breakdown $\ln(t_{50})$ plotted against the electric field (E_{ox}) for all studied oxide thicknesses is linear (Fig.1).
Physically, this is attributed to the thermochemical breakdown based on the Eyring chemical reaction model. This model was observed by Crook [1], Berman [2], and later by McPherson and Baglee [3].

In a recent study, McPherson [4] has demonstrated and proved that the linear model, commonly referred as the «E-model», gives better results than the most popular model commonly referred to as the «1/E-model», described by [5-7].

McPherson collected data from a wide range of electric fields. In the same time, Kimura [8] has concluded that the linear field dependence yields a best fit compared with the hole-induced breakdown model. The difference between these 2 models appears at high temperature. The linear field model predict the most conservative oxide life estimates, whereas the reciprocal model will predict a more optimistic estimate.

The equation of the linear model is the following one :

$$\ln\left(t_{BD}\right) = \tau_0 - \gamma \cdot E_{OX} \qquad (1)$$

where the electric field acceleration factors, γ (slope of the curve) and τ_0 (intercept at zero electric field), are defined by :

$$\gamma = \frac{d(\ln(t_{BD}))}{dE_{OX}} \quad \text{and} \quad \tau_0 = t_{BD}\big|_{EOX=0}$$

There are many features that can be deduced from figure 1. For all oxide thicknesses, the data exhibit a good fit regarding to the linear electric field. Lifetime of devices with a thin oxide thickness is longer than that of the thick one at high electric fields. However, the most important feature to be noted is, that the difference in lifetime between thick and thin oxides diminishes with the electric field decreases, and we expect that this observation will be inverted when the electric field becomes very low, i.e. for example for 4 MV/cm, thick oxide has long lifetime than thin oxide.

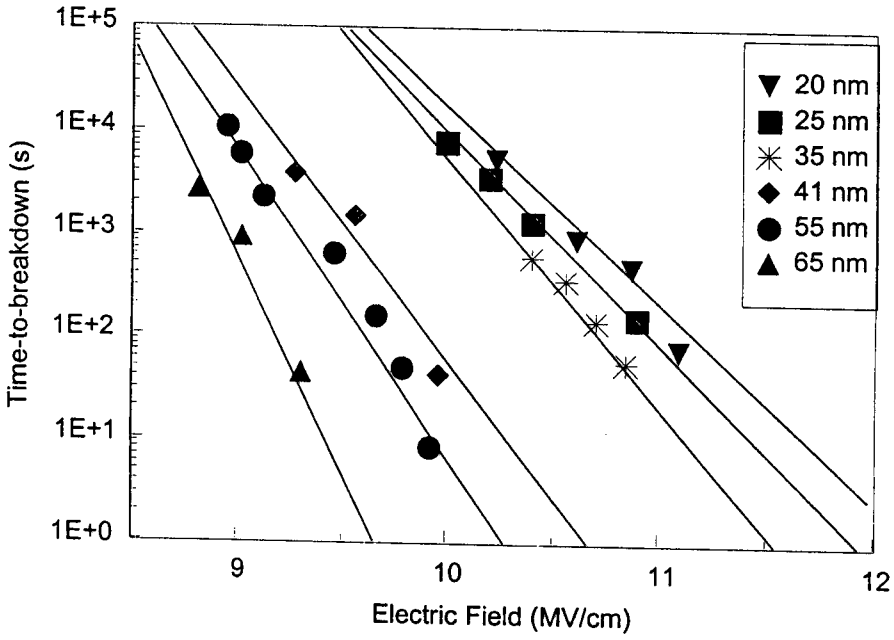


Fig. 1. The median time-to-breakdown (t_{50}) as function of electric field for different oxide thicknesses.

The electric field acceleration factor, γ, representing the slope of the curves, is lower when the oxide thickness decreases. This feature appears on Fig. 2, where γ is plotted as a function of the oxide thickness. The values of γ are in the range of 1 to 4 cm/MV for all thicknesses. The thickness dependence of the electric field acceleration factor of TDDB γ can be represented by the relation :

$$\gamma(cm/MV) = -5.8(\pm 1) + 3.15 \cdot \ln(T_{OX}) \qquad (2)$$

where T_{OX} is oxide thickness in nanometer.

This variation law is similar to the one presented in figure 8 by Yamabe and al. [9]. In their figure, the authors added other authors data to their data. So we accept the law presented by Yamabe with certain reservations, because the data presented are not obtained from the same process fabrication. We think that it is not correct to study the reliability of an oxide relative to a particular process and in the same time to mix data obtained from other process fabrication. Each one has its own reliability study. In our case, all the samples came from the same process fabrication named ASD™, and the goal is to develop both high reliable and competitive technology.

From figure 1 and for each thickness, we extrapolate the $\ln(t_{50})$-E_{OX} characteristic to an electric field equal to zero. Thus, we determine the value of $\ln(t_{50})$ at the origin, τ_0. Physically, τ_0 is function of ΔH, k and T, that are respectively, the enthalpy of activation for oxide breakdown, the Boltzmann's constant and the temperature. τ_0 is plotted versus oxide thickness (Fig. 3). This characteristic has never been taken into account or studied. However, we note that τ_0 has a same variation law as γ. τ_0 is described by the relation :

$$\tau_0 = -26.5(\pm 8) + 24.3 \cdot \ln(T_{OX}) \qquad (3)$$

With the relation (1), (2) and (3), we deduce a general empirical relation, giving ln(t50) according to the initial electric field and the dielectric thickness (higher than 10 nm). This relation is :

$$\ln(t_{50}) = -26.5 + 24.3 \cdot \ln(T_{OX}) - (5.8 + 3.15 \cdot \ln(T_{OX})) \cdot E_{OX} \qquad (4)$$

Relation (4) is a generalized reliability law that allows to predict lifetime of a dielectric (silica in this study) with any thickness higher than 10 nm and under any electric field.

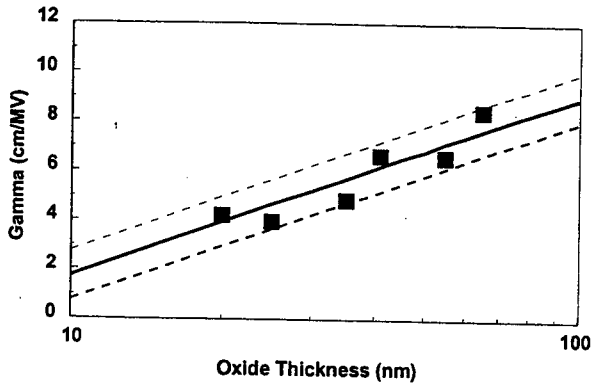


Fig. 2. The field acceleration parameter γ as function of oxide thickness.

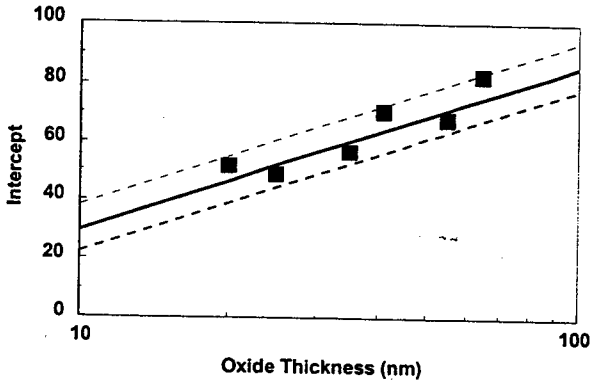


Fig. 3. The field acceleration parameter τ_0 as function of oxide thickness.

From the relation (4), we plotted the logarithm of the time-to-breakdown versus the electric field, for dielectric thicknesses of 10, 20, 50 and 100 nm (figure 4). As it has been predicted previously, the lifetime of devices with a thin oxide thickness is longer than the ones with a thick oxide at high electric fields, whereas when the electric field is lower, the results apparently are inverted. But the most important feature to be noted is the presence of a pivot field E_p, which is between 7 and 8 MV/cm.

The interpretation of this observation is : the breakdown occurs at a critical generated electron trap density (or hole density). A plausible breakdown mechanism is the conduction via these generated traps. Inside the oxide volume, electron traps are generated at random positions [10]. A sphere is defined around, which depicts the trap influence. If the sphere of two neighbouring traps overlap, the conduction between these traps becomes possible. The breakdown condition is reached when a conducting path is created from one interface to the other. The number of traps need to create a path, responsible of the breakdown for thick oxide, is more significant than for the thin one at high electric field.

Because, when an oxide is submitted to high electric field, greater than 8 MV/cm, the impact ionization phenomenon becomes the only major cause of the breakdown when the oxide thickness increases. Because the number of traps created in a thick oxide compared to a thin oxide is so much more significant, then the path through the oxide which brings to breakdown is created more quickly. But, when the field applied to the MOS structure is reduced, for a nominal use of 4 MV/cm, the path in thin oxide is created more quickly. Indeed, the probability to generate electron traps that are aligned is more significant when the oxide is thinner. This observation agrees with that suggested by Degreave [10].

From (4), we can also represent time-to-failure according to the dielectric thickness, by taking as parameter the electric field. That is what is shown in figure 5, for electric field of 6 MV/cm (straight line). Data of Kimura [8] and Degraeve [11] are added to this graph (symbols). In a recent study, Kimura [8] plotted the field acceleration factor, γ, as a function of oxide thickness. He showed that the values of $\gamma(T_{ox})$ decrease when the oxide thickness is reduced to 8 nm, reaching a plateau between 5 nm and 8 nm, and then increase for oxides thinner than 5 nm. This observation can give explanation to our results.

4. CONCLUSION

In this study, the reliability of oxide thicknesses greater than 20 nm was investigated. TDDB data are performed and the linear model is applied to study the reliability of industrial devices. The field acceleration factors of the model respectively γ and τ_0, of TDDB have a same law versus the oxide thickness. That permits to us to give a generalized law to predict lifetime for any electric field applied to any oxide thickness as long as the oxide thickness is greater than 10 nm. We note that when the electric field becomes lower, thicker oxide is more long-term reliability.

ACKNOWLEDGMENT

I wish to acknowledge Dr. Fabien Nebel for his encouragement and helpfull discussion..

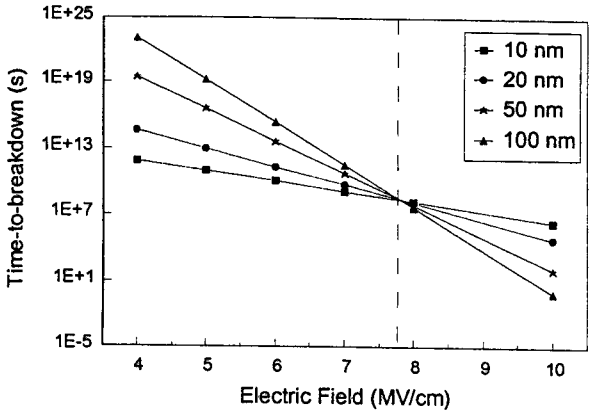


Fig. 4. Time-to-breakdown (t_{50}) versus electric field for different oxide thicknesses. We note the existence of a pivot between 7 and 8 MV/cm.

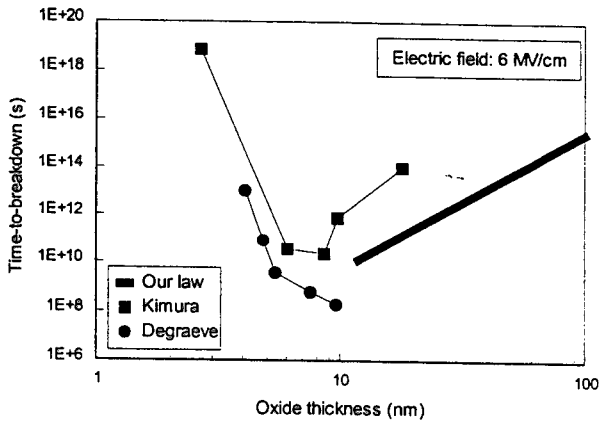


Fig. 5. Time-to-breakdown as function of oxide thickness for an electric field of 6 MV/cm. Straight line represent our reliability empirical law.

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RECOMBINATION LIFETIME MEASUREMENT BY THE CONDUCTIVITY MODULATION TECHNIQUE

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ABSTRACT

The conductivity modulation measurement method is described to determine the minority carrier recombination lifetime, τ, of a power p-i-n diodes. This method is based on the measurement of the basewidth conductivity modulation of diode, biased in the forward direction. The conductance-voltage characteristic allows us to extract τ. This method is fast, simple to use and adapted to the parametric test system, which is an industrial equipment. This measurement technique will be introduced in the parametric test system which the goal is to follow the parameter evolution of the ASD™ (Application Specific Discrete) process basic devices. To illustrate the method, it is compared to the reverse recovery methods.

1. INTRODUCTION

The lifetime of excess carriers in the base region of p-i-n diodes controls the electrical behavior of these devices. Both the forward voltage drop and the recovery time for diodes and the gain h_{FE} for bipolar transistors are greatly influenced by this parameter. Indeed, the knowledge of its magnitude and behavior is very important to control the design and fabrication of power devices. In an industrial environment, this parameter must be extracted after each fabrication process step. It allows to give information of any change occurred in the fabrication process. Thus, the fabrication process can be controlled more accurately.

In industry, the control of device elementary parameters of any technological fabrication process must be systematic, reproducible and fast. For that, a parametric test system (PTS), that is an industrial equipment, is solicited. The tester contains some fixed and compact instruments, able to extract and measure the major basic device parameters, like contact resistance, dielectric strength, sheet resistance, leakage current and so on. Sometimes, the instruments are incompatible with measurement techniques. In our case, the tester is incompatible with all the optical techniques, reverse recovery and open circuit voltage decay (OCVD) methods because there is no oscilloscope in the tester to record the transient current or voltage in real time.

Generally, instruments are adapted to the measurement techniques in the laboratories but in this study we must adapt the measurement technique to the PTS equipment. Taking into account this constraint, we applied correctly the conductivity modulation measurement technique because the PTS contains a capacimeter. In our knowledge, there are few papers that treat about this method experimentally. Generally, it's described more theoretically without taking into account the exact parameters of the diode, like the diode ideality factor [1], or it is used with a particular test structure[2], which is not adapted to the real device that will be marketed.

In this paper we demonstrate that the minority carrier lifetime of a p-i-n diode, can be extracted by using the conductivity modulation measurement technique. The method consists to bias the diode in the forward direction and plots the conductance-voltage characteristic. The exploitation of this characteristic allows to extract the minority carrier recombination lifetime.

To valid the method, we measured the lifetime with the reverse recovery technique.

2. THE METHOD DESCRIPTION

Before describing the lifetime measurement method, we would like to describe, both the PTS equipment and the ASD™ products.

◆ There is two parts in the PTS, a hard one and a soft one. The hard part is compound by a tester and an automatic prober. The soft part is compound by a workstation which controls all the instruments as the prober. It contains all the test libraries linked to each technology. Figure 1 shows the configuration of the parametric test system which the goal is to follow device basic parameters at each fabrication process step. The tester contains some source-measure units (SMU) with high/low-current/voltage, a pico-ampermeter, a voltmeter, a capacimeter with a fixed frequency and a matrix unit which switches between the instruments. PTS instru-

ments applies current or voltage to the devices. The devices are placed in a test vehicle or test die, in opposite to product die. This one contains test patterns relative both to the fabrication process like the Van Der Pauw test pattern to measure sheet resistance and to device patterns like diode to measure lifetime. The wafer, which contains all the dies, product and test dies, is placed in an automatic prober. A workstation controls all the instruments of the PTS and the prober by software.

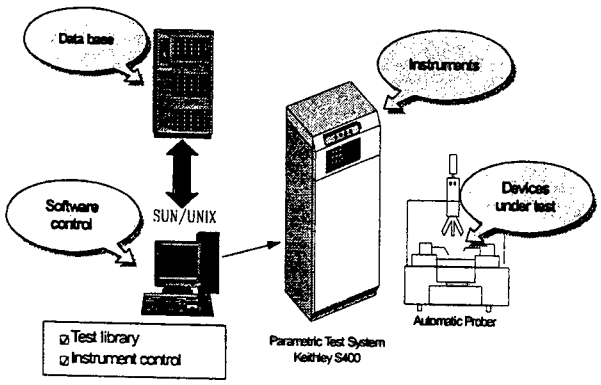


Fig. 1. Parametric test system (PTS) used in microelectronic industry environment to follow device and process parameters.

◆ Because our work is dealing with the device integration in power integrated circuits of the ASD2 process, we dwell on the power integration. Presently two approaches of power integration exist. The first approach is the "Smart Power" technology. In this technology, logic and/or analog control and diagnostic functions alongside the power architecture are integrated. The second approach, is developed by STMicroelectronics seven years ago, it's called ASD™ (Application Specific Discrete). The ASD products are based on a quite new approach called "functional integration". The principle is the following : on one single chip are integrated all the power elements (diode, transistors, SCRs,) required to achieve either the conversion of energy or the protection. The integration combines in the Si substrate various areas having specific features (such as doping, thickness,...), that are made to interact to perform a global power components individually mounted on a printed circuit.

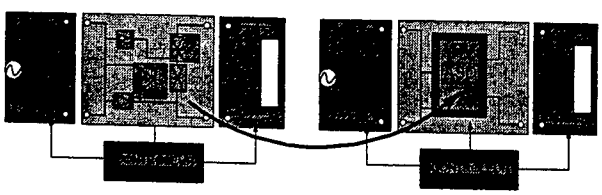


Fig. 2. ASD™ approach.

The measurement method needs only a capacimeter with a fixed frequency for biasing the diode in the forward direction. A small signal (sine wave) voltage is superimposed upon the dc voltage. The capacimeter measures the diode conductance and a voltmeter measures the forward voltage drop. The method is correctly adapted to the PTS equipment.

The ideal junction diode under forward bias conditions and perturbed by a small ac signal, is modeled by an admittance, that is just a capacitance in parallel with a conductance. The admittance is given by :

$$Y = \frac{di}{dt} = G_D + j\omega C_D \qquad (1)$$

With,

$$G_D = \frac{qI_0}{kT}\exp\left(\frac{qV}{kT}\right)\sqrt{\frac{1}{2}\left(\sqrt{1+(\omega\tau)^2}+1\right)} \qquad (2)$$

G_D is the conductance of the diode. q, k, T et I_0 are respectively, the elementary electric charge, the Boltzmann's constant, the temperature and the saturation current of the diode. τ is the minority carrier lifetime in the base of the diode and ω is the pulsation.

The relation (2) is given for an ideal diode. To take into account the real parameters of the diode, we make a correction on this equation, by replacing the voltage (V) by $(V-R_SI)$, with R_S, the serie resistance of the diode and we introduce the ideality factor n. I_0, R_S and n are extracted from the current-voltage characteristic. So, equation (2) becomes :

$$G_D = \frac{q}{nkT}I_0\exp\left(\frac{q(V-R_SI)}{nkT}\right)\sqrt{\frac{1}{2}\left(\sqrt{1+(\omega\tau)^2}+1\right)} \qquad (3)$$

When the frequency is fixed, the conductance depends only on the bias voltage. We verified that R_S has no influence on our results [1]. So, we can write :

$$G_D = G_{DF0}\exp\left(\frac{q}{nkT}V\right) \qquad (4)$$

with,

$$G_{DF0} = \frac{q}{nkT}I_0\sqrt{\frac{1}{2}\left(\sqrt{1+(\omega\tau)^2}+1\right)} \qquad (5)$$

G_{DF0} is the parameter extracted from the conductance-voltage characteristic. It is obtained by extrapolating the conductance curve until V=0. So, G_{DF0} depends only on τ. So, τ is given by the expression:

$$\tau = \frac{1}{\omega}\sqrt{\left(2\left(\frac{nkT}{qI_0}G_{DF0}\right)^2-1\right)^2-1} \qquad (6)$$

3. RESULTS AND DISCUSSION

Figure 3 shows the experimental conductance-voltage characteristic of a p-i-n diode. The theoretically characteristic is also plotted from (5), with a continuous line. It is clear that the theoretical characteristic well fits the experimental one, in the range of 0.2-0.5 V. We observe a large discrepancy when the voltage is under 2 V. Physically, the explanation of that is : when a low forward voltage is applied to the diode, few minority carriers are injected across the p-i-n junction boundaries since much of the electrons and holes recombine with each other in the space-charge layers and at the lightly doped layer before they have a chance to get across the potential barrier of the space-charge layers. In this case, the Sah-Noyce-Shockley (SNS) current dominates over the Shockley current [3]. Only at higher forward biases, the latter dominates and the minority carriers are effectively injected across the p-i-n junction boundaries. The voltage at which the injection becomes effective was estimated to 0.26 V, if we suppose that τ equal to 1µs [3]. This particular value of voltage was defined as the injection threshold voltage. From the conductance-voltage characteristic of figure 3, the lifetime is evaluated to 10 µs. The parameters of the diode are 1.05 and 1.28 10^{-12} A, respectively the diode ideality factor and the saturation current.

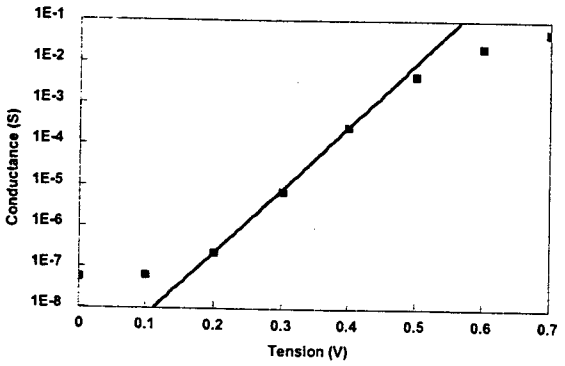


Fig. 3. Measured and calculated G_D versus forward bias voltage for an ASD™ lateral power diode

We have simulated the p-i-n diode structure with the ISE simulator. We enter the device parameters, like the dimensions, the doping and the junction depth. In figure 4, we show the measured and simulated results. The latter are given for 3 values of recombination lifetime. We see that there is a goode agrement between the experimental results and the simulated curves (1 and 10 µs) in the voltage range of 0.2 to 0.4 V.

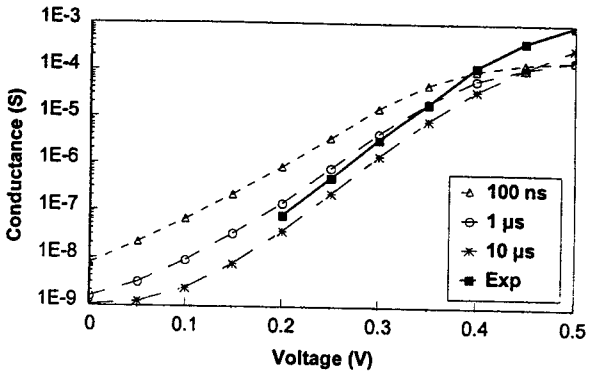


Fig. 4. Measured (solid squares) and simulated G_D for different value of lifetime versus forward-bias voltage.

To valid the method, we applied the reverse recovery technique in order to compare the results. The diode reverse recovery (RR) method was one of the first electrical lifetime characterization techniques.

There are two basic measurement schemes. In figure 5(a) the current is suddenly switched from forward to reverse current. This method is attributed to Moll [4] and Kuno [5]. In figure 5(b) the current is gradually changed and this method is attributed to Kao [6].

In all cases, the current through the device is inverted and the carrier lifetime is obtained from the measure of the time that takes the device takes to recover its reverse blocking capability. The charge control equation for the low doped region is:

$$\frac{dQ}{dt} = -\frac{Q}{\tau} + I(t) \tag{8}$$

Q is the electrical charge stored by the carriers in the low doped region. The initial condition is $Q_F = I_F \tau$, as in the forward steady state. In the above condition we have:

$$\frac{dQ}{dt} = 0 \quad \text{and} \quad I = I_F$$

1) Kuno and Moll's Methods: a constant reverse current I_R is imposed at t = 0 (Fig. 5(a)), after a forward steady state. The slope of $\ln(1+I_F/I_R)$ versus the storage time t_s, gives the value of τ (Kuno). This is valid for large base thickness [7]. If, as a supplementary hypothesis, we assume that at t_s the stored charge is zero (Moll), the solution of (8) becomes:

$$\frac{t_S}{\tau_P} = \ln\left(1 + \frac{I_F}{I_R}\right) \tag{9}$$

By assuming a tringular approximation of the excess hole concentration at $t = t_s$, Tyagui has found another relation between I_F, I_R and t_s [8]:

$$\frac{t_S}{\tau_P} = \ln\left(1+\frac{I_F}{I_R}\right) - \ln\left(1+\frac{I_F}{I_F+I_R}\right) \qquad (10)$$

2) Kao's Method: The circuit inductance which prevents an instantaneous current reversal is taken into account (Fig. 5(b)). The current goes from I_F to I_R with a finite rate dI/dt. If we accept that at t_2 the stored charge is zero, (8) leads to:

$$t_2 - t_1 = \tau.\left(1-\exp\left(-\frac{t_2}{\tau}\right)\right) \qquad (11)$$

As a particular case, if slope (dI/dt) is such that $I_F = -I_R$, $t_2 = 2t_1$, and $\tau = t_1/0.796$.

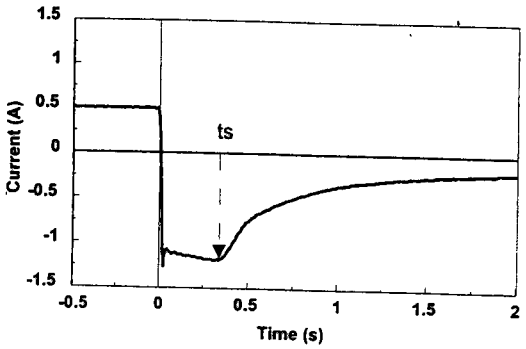
Finally we give in the table I, a summary of all the results obtained with the different methods. The G-V value is for the conductance-voltage measurement method. We note that all the results obtained with the different methods are in the same order

Methods	G-V	Kuno & Moll	Kao	Tyagui
τ (μs)	10	1.31	1.42	3.8

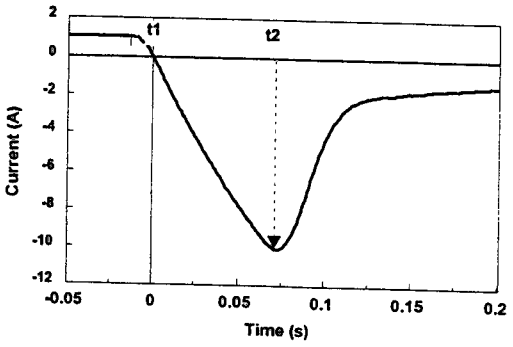
Table I. Experimental results obtained for carrier lifetime using the methods considered in the text.

4. CONCLUSION

In this work we demonstrate that the conductivity modulation technique is an alternative method to measure the power p-i-n diode minority carrier recombination lifetime in an industrial test parametric system. Only a capacimeter with a fixed frequency and an external voltmeter are required for this method. The diode is biased in the forward direction by the capacimeter which in the same time measures the conductance, when the voltmeter measures the voltage drop in the diode. The obtained results are in good agreement with the ones obtained from the reverse recovery time method. Nevertheless, a good accuracy from the method requires that ($\omega\tau$), be close to 1. In our case, the capacimeter has a fixed frequency, 100 kHz and the minority carrier lifetime is in the range of 1 μs.



(a)



(b)

Fig. 6. Current transients observed in the methods used for carrier lifetime measurement: a) Kuno and Moll; b) Kao.

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Analog IC's Using Space-Charge Waves in the Two-Valley Semiconductor Films for Microwave Signal Processing

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One of the urgent problems of advanced microelectronics is to develop monolithic devices, i.e. analog signal microprocessors, for processing complex and multichannel analog microwave signals in real time.

The use of space-charge waves (SCW) in GaAs thin films with hot electrons is a promising way for realization of analog signal microprocessors. Devices based on SCW use an attractive property of GaAs. Due to the electric field in excess of 3 kV/cm applied to GaAs sample the differential electron mobility in it reverses. In this case SCW's - the increasing perturbations of the electron density - can propagate with a drift velocity.

A travelling-wave amplifier developed in the USA at the beginning of the 1970'-s was the first integrated device based on SCW in GaAs [1]. It contains GaAs film on a semiinsulating substrate, source and drain ohmic contacts, input and output metal electrode strips forming Schottky barrier contact with a semiconductor layer. The advantage of this device over a MMIC amplifier based on a Schottky FET is extremely high gain of 30db or more with sufficient stability margin. The latter is due to the unidirectional propagation of the SCW and to the large input-output electrodes spacing.

We, in turn, realized a travelling-wave amplifier ICs at cm and mm ranges where SCW's are excited and/or received by the multielement electrode systems such as the interdigital type rather than a single electrode (Fig. 1).

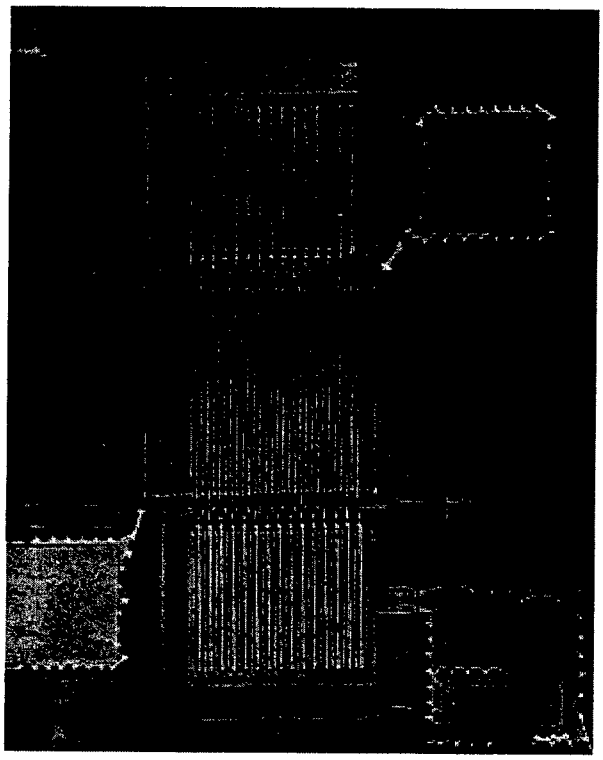


Fig. 1

These devices provide microwave signal gain and filtering capability directly at the input receiving channel. The simplest device of this type is a selective amplifier with electron tuning [2]. This amplifier includes equidistant interdigital system (IS) of the exiting electrodes. It can be seen that coherent SCW accumulation takes place only when interelectrode spacing equals one half the SCW length. The AFC of the device is Sin(x)/x, the main maximum width being close to 1/N, where N is the number of electrode pairs in the IS. To suppress AFC side maxima, apodization of the IS is used. Thus, Gaussian apodization allows realizing amplifiers in the X range with 15db gain and side maxima sup-

pression no less than 25db. The results obtained can be further improved.

Using non-equidistant IS at the device gives one great opportunities. Evidently, for each IS of any arbitrary topology there is such a signal that, being applied to the device input, will coherently excite SCW; the signal of a different waveform cannot drive the amplifier. In other words, the device operates as an active wideband optimal filter, having excellent weight and size characteristics with optimum filtering of complex microwave signals directly at the input of receiving channel. It should be noted that with slight modification of the construction - adding an input electrode between the source and IS - the device becomes a multifunctional one. Besides the above-mentioned functions this device can form a specific signal for which it is an optimal filter. We realized phase-shift signal formers providing duration-bandwidth product no less than 16 with N=32 in X range.

SCW can also be successfully used for various multichannel signal processing. Realization of the appropriate IC's is based on autodiaphragming phenomena of the SCW beams and their entrainment by the electron drift (our team found and studied these phenomena) [3].

The first phenomenon is that the beam of SCW formed by the bent input electrode is narrowed while propagating; its focus width can be a small fraction of the initial aperture size. By changing the direction of a static drift field one can scan it over the system of output electrodes (entrainment of the beam by the drift). Using this principle we developed three-five channeled switching amplifiers (Fig. 2).

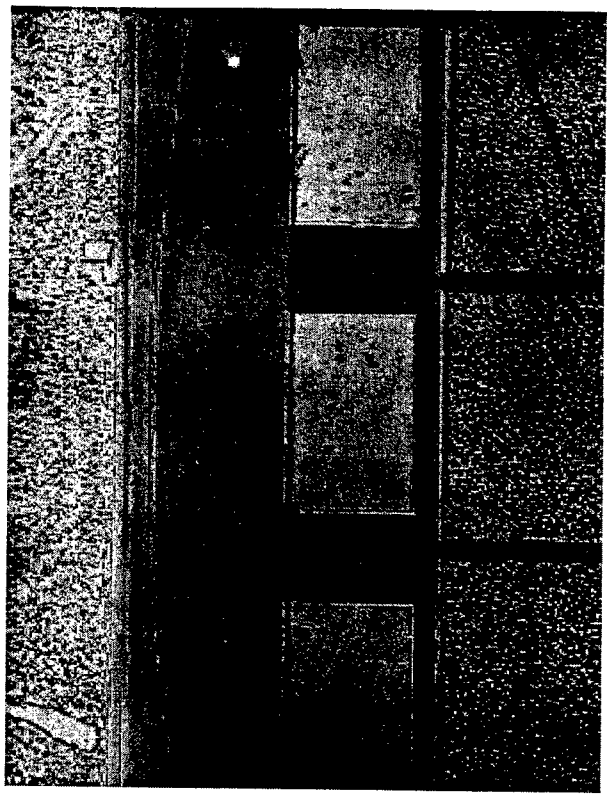


Fig. 2

Another application of the two-dimensional phenomena is an IC for processing signals from a phased array. Here, the wave beam forming is provided by a system of input electrodes (located along a parabolic arc) connected to the elements of the phased array. If we locate the system of output electrodes in the focal region of the device we'll provide an appropriate place of the main lobe of the pattern for each electrode.

The devices discussed do not limit the possible applications of SCW in microelectronics. Thus, using solid-state plasma nonlinearity in the devices of the two-port travelling-wave amplifier type allows us to realize the IC combining the functions of microwave amplifier, mixer, IF filter and IF pre-amplifier. We also propose the designs of monolithic phase-shifters, delay lines, analog memories for microwave signals, correlators etc. Analogues for all these devices are not found.

Such a variety of functional devices that can be realized using SCW's is due to the unique

combination of their properties. SCW's are slow (their velocity is 3.5 orders of magnitude less than that of the light) and therefore "electrically long" systems can be made extremely compact. They provide long lengths of coherence or significant gain; the magnitude and direction of SCW velocity can be easily controlled by changing the magnitude and direction of a static drift field. SCW's being surface in their nature, can easily interact with electrode systems on the semiconductor surface. The upper end of the frequency range where SCW's exhibit the above-mentioned properties is determined by the time of the intervalley electron transition in GaAs and can approach 50 - 80 GHz.

It is worth noting that SCW-based IC technology is quite compatible with the conventional processes of GaAs IC batch production, and it allows one to integrate not only various devices based on SCW but also traditional IC components on a single chip.

Thus, we have developed and studied prototypes of some functional devices, and derived the theory of SCW excitation, propagation, interaction and reception. So, a real background for rapid progress of this new class of IC's is created.

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Complementary Clock Feed-Through Reduction for Switched-Current Systems

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Abstract - **A novel method of clock feed through reduction in switched-current circuits is introduced here that outperforms previous methods. In principle, the output of identical circuits with complementary switches are added to cancel out switch based error without the requirement of separate DC and signal distortion cancellation in separate stages. Spice results are shown and compared with analysis and hardware layout. These circuits are useful for digital computation with analog hardware, and with respect to simulation, this circuit has yielded successful results when used in an ear-type network that requires a delay as part of its matrix.**

I. INTRODUCTION

For a good part of this decade, transistor-mode switched current systems have arisen as a cheap and simple form of analog to digital conversion [1], useful especially for current mode systems and biomedical applications with specific relevance to ear type systems [2]. The mechanism of this converter is that a switch controlling input to output amplification connection is periodically pulsated, giving an output that has the original signal alternated with a held, or discrete, value of the signal. A basic problem arising with the technique is the inaccuracy of the signal's held value on the output. Charge buildup on the switch and amplifier causes a differential transfer of the switch control voltage at the switch stage based on the basic capacitance properties of the materials [3]. These inaccuracies are problematic due to their high non-linearity and low-predictability. Previous techniques used for compensation at the receiver end vary from adjusting output widths to lower the significance of the voltage error difference [4,5], splitting the transition area into parts that have their own compensation switches [5], and multiple component optimization [6]. Our approach is to compensate feedthrough by adding the output of two filters that are identical except for the polarity of their inside switches. This technique ultimately reduces design factors and mismatch error due to its conceptual simplicity, although it does require as great a number of transistors as the techniques mentioned above.

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II. THEORETICAL AND PHYSICAL DESIGN ASPECTS

The circuit used here begins with the conceptual structure of [1]. Following through either the top or bottom part of Fig. 1(a), an input, *In(n)*, injected into the central node is added to the previous output, *-(B/A)Out(n-1)*, withheld due to capacitor storage at switch outputs and the non-overlapping nature of the complementary switching system. This is then modified by A to yield the final output, giving the following transfer function:

$$\frac{Out(n)}{In(n)} = \frac{-A}{1 - B \cdot \frac{Out(n-1)}{Out(n)}}. \quad (1)$$

The bias currents cancel out and are not necessary in the block model, but are required for the physical model in order to raise the input to the transistor saturation region: $V_{DS} \geq V_{GS} - V_{t2}$, where

$$V_{GS} = \sqrt{\frac{2I_{in}}{\mu \cdot C_{ox} (W/L)_1}} + V_{t1}. \quad (2)$$

μ denotes electron mobility, C_{ox} is the specific capacitance formed in the gate and channel junction, $(W/L)_1$ is the width over length of the input transistor, V_{t1} is the threshold voltage of the input transistor, V_{t2} of the output transistor, and V_{GS} the gate to drain voltage. The bias, *Idc*, in Fig. 1(a) is fed to the circuit through a buffering structure that prevents feedback distortion from its load [8]. Table I gives the comparison of the circuit's block diagram, Fig. 1(a), and its transistor implementation, Fig. 1(b), which is representative of its layout, Fig. 1(c).

TABLE I

Block	Transistors (Width:Length in microns per microns)			
Amp1	5(10:30)	6(10:10)	7(10:30)	
Amp2	8(25:30)	9(10:10)	10(9:30)	
Amp3	8(25:30)	9(10:10)	12(20:30)	
Amp4	14(10:30)		13(9:60)	
Amp5	14(10:30)		11(8:30)	
R1	1(10:10)	2(10:10)	3(10:10)	4(10:10)
R2	15(10:10)	16(10:10)	17(10:10)	18(10:10)
Amp6	25(10:30)	26(10:10)	27(10:30)	
Amp7	28(25:30)	29(10:10)	32(9:30)	
Amp8	28(25:30)	29(10:10)	30(20:30)	
Amp9	34(10:30)		33(9:60)	
Amp10	34(10:30)		31(8:30)	
R3	21(10:10)	22(10:10)	23(10:10)	24(10:10)
R4	35(10:10)	36(10:10)	37(10:10)	38(10:10)
J	19(10:30)	20(10:10)		

III. ANALYSIS

Error voltage, and in effect error current, occurs at the intermediary gate of any current mirror that contains a switch. This is due to the gate to drain or source junction capacitance expunging charge that it has withheld from a previous release stage. Rather than compensating with amplifier modification constants, the switches can be modified to give equal amount of error in order to cancel each other exactly and consistently. Error due to constant and signal components are canceled because of this, with only a necessary comparison of error due to P and N type switches. This can be obtained with simplified equations from [4]:

$$C_{total} = C_{OX}(WL)_{sw} \tag{3a}$$

$$Q_{total} = C_{total}(V_{Gsw} - V_{Tsw}) \tag{3b}$$

$$V_C = \frac{Q_{total}}{C_2} = \frac{C_{OX}(WL)_{sw}(V_{Gsw} - V_{Tsw})}{C_{OX}(WL)_2} = \frac{(WL)_{sw}}{(WL)_2}(V_{Gsw} - V_{Tsw}) \tag{3c}$$

Here C_{total} is the total gate capacitance of the switch transistor, C_2 is the capacitance of the output transistor.

So we see that the error voltage is a function of the threshold voltage, V_t and can be recompensed with $(WL)_2$, comparing terms of the N-switch, and P-switch, where V_{TN} and V_{TP} are the N and P switch threshold voltages respectively:

$$(WL)_{swN}(V_{Gsw} - V_{TN}) = (WL)_{swP}(V_{Gsw} - V_{TP}) \tag{4a}$$

$$W_{swP} = W_{swN}\left\lfloor \frac{V_{Gsw} - V_{TP}}{V_{Gsw} - V_{TN}} \right\rfloor \tag{4b}$$

Figure 1(c) shows the MOSIS 2 micron technology VLSI layout. Simulation was optimized for this technology: the N switches were set to have a *W/L* of *10/10*, and the P switches, *8/10* due to the relationship in (4b). The amplification, A, was taken as 0.45, and the delay modification, B, as 0.80. For non-biasing and non-switch transistors, the standard lengths used were 30 microns, and widths 10 or 25 microns for the NMOS or PMOS respectively. Figure 2 shows the output of the N-switch circuit (top curve) and the P-switch circuit (bottom curve) separated, along with the results of the complementary circuit (middle curve) and the input signal (smooth curve).

IV. SUMMARY AND CONCLUSIONS

We have demonstrated a circuit that cancels clock feed through with complementary addition that avoids signal rerouting. As well, the results of this sample and hold method are good, and have shown great improvement in comparison with previous methods.

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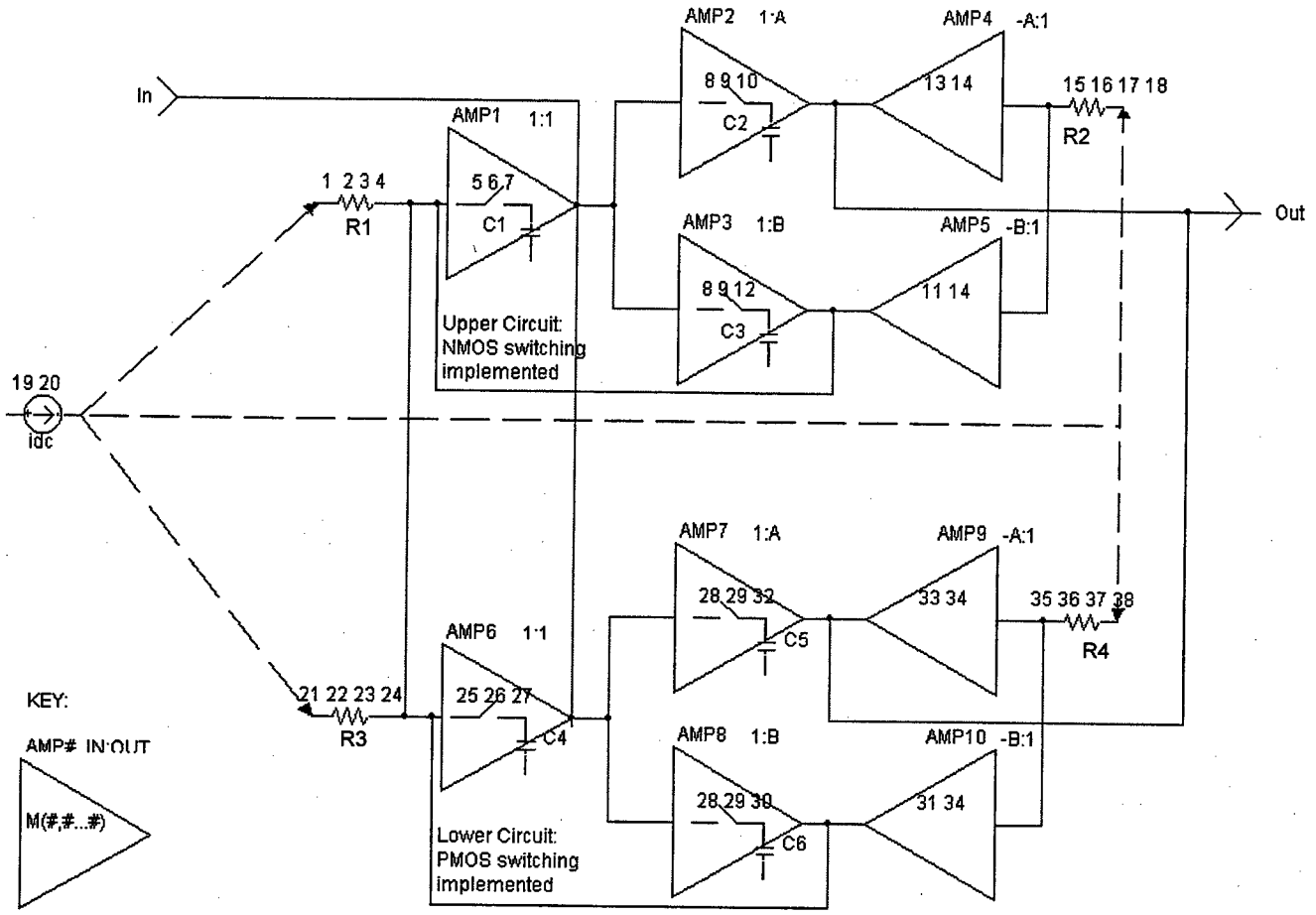


Figure 1(a). Block diagram of new circuit, the center-dashed-line that pulls the bias current also can be used to visualize the distinguishing of the N and P complements. The numbers inside or near the components indicate its counterpart in (b), also correlated to TableI.

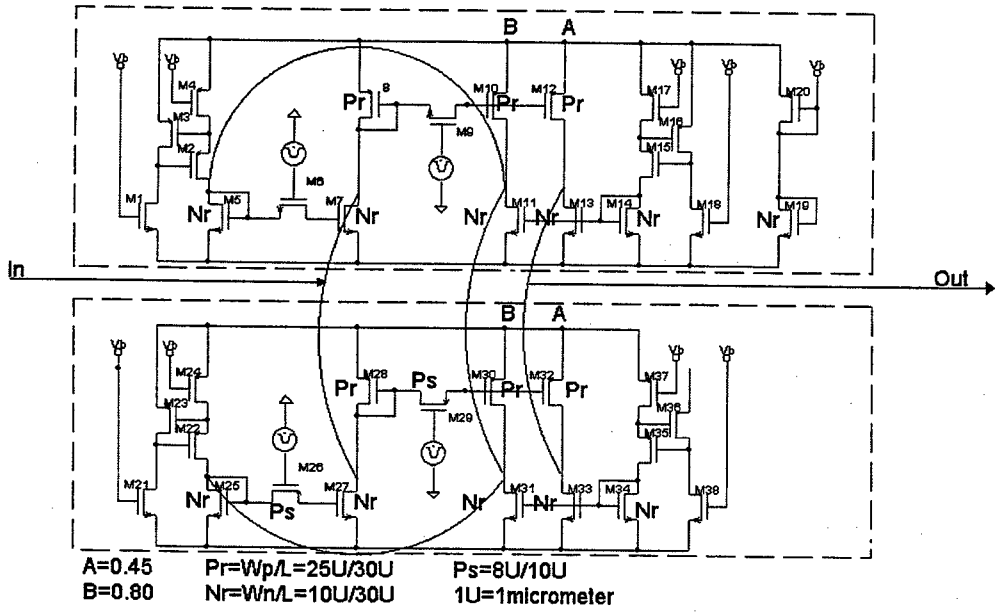


Figure 1(b). The transistor version of (a).

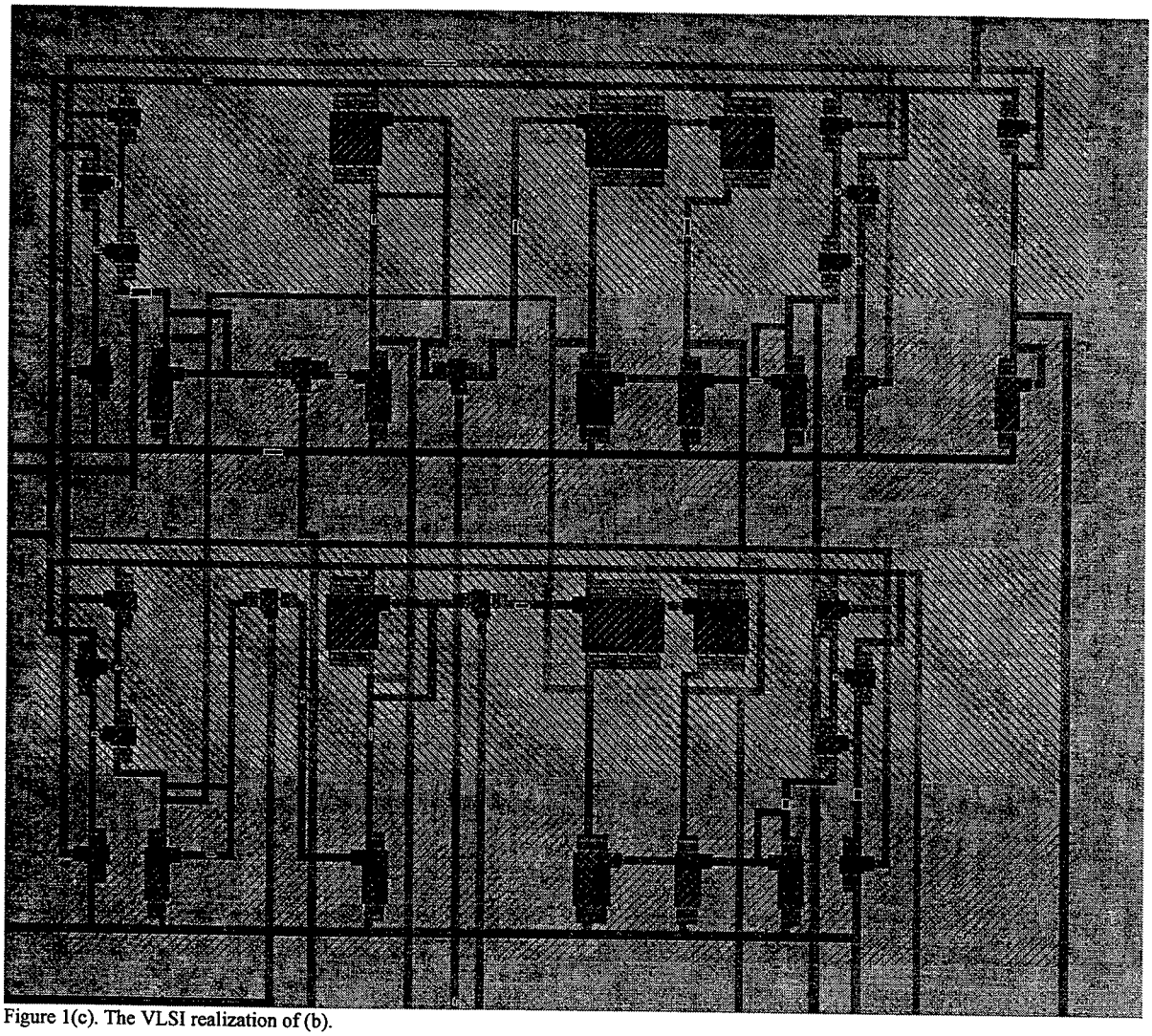


Figure 1(c). The VLSI realization of (b).

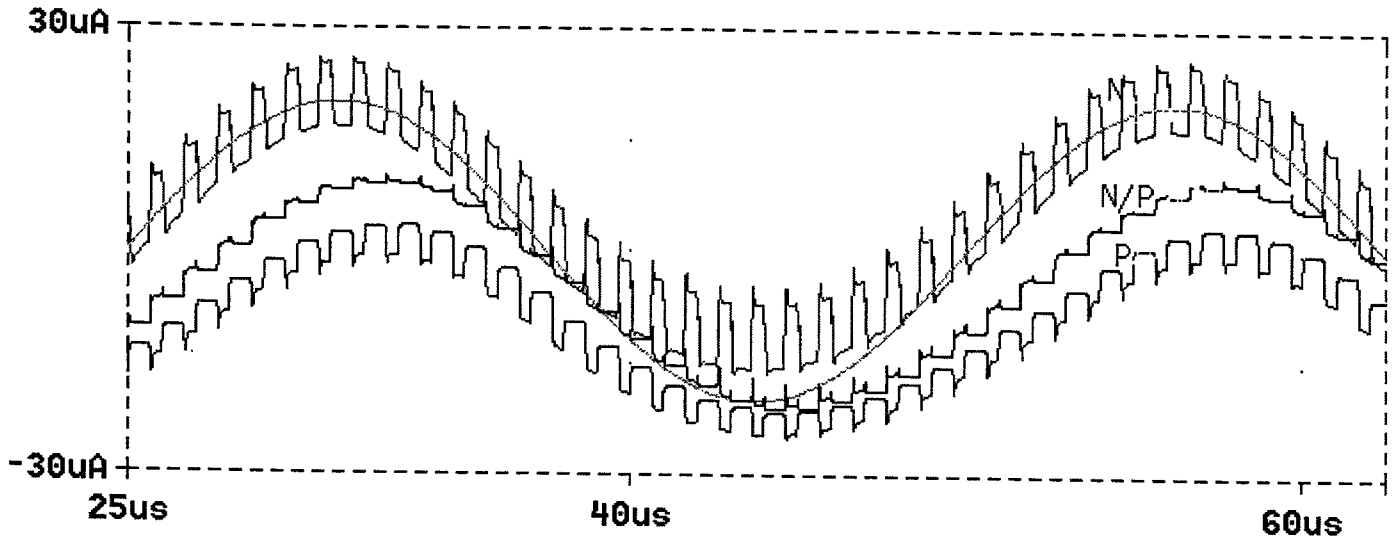


Figure 2. From top to bottom, N-switch, P-switch, and complementary circuit results. Smooth line is the input.

Kulikov O.N., Muravskiy B.S

Transistor structures with the distributed emitter and active contact to admixtures, which are leading in deep energy levels

As was established earlier, the transistor structures with distributed emitter p^+-n-junction and local collector contact (active contact) have electrophysical and photoelectric performances essentially distinguished from usual transistor structures, that has allowed to create a series of original semiconductor devices on their basis [1]. Earlier active contact (AC) was executed either as metal-tunnel-oxide-semiconductor or as n^+-p-diode. As further researches have shown AC providing beforehand given aspect of performances of structures and stable operation of gears on their basis, can be made and by means of implantation of admixture creating deep energy levels in a forbidden gap of a semiconductor into n-region of structure (basis). Schematic aspect of investigated structures and their energy diagrams are represented in a fig. 1.

For manufacture of transistor structures the silicon plates with a substrate p^+-type and specific resistance $\rho=10^{-2}$ Ohm•cm were used, on which by the method of a gas epitaxy was grown a layer of a n-type by width 10-20 microns (ρ=2,5 Ohm•cm). AC was made by a method of melting of a eutectic alloy to a n-region of a plate. For this purpose on a carefully stripped surface of n-region of a plate were located portions of a eutectic alloy of tin with lead and cadmium, with different percentage of components. Cd(87%) in some portions tin+lead in others. The plates with portions were heated in vacuum to temperature providing a superficial diffusion in to a surface layer of silicon, and were withstood at this temperature with consequent smoothly varying cooling up to a room temperature. Germanium samples represented plates of a n-type (ρ=10 Ohm•cm), on which by melting of indium p^+-n- junction was formed. AC were made by local introduction copper or

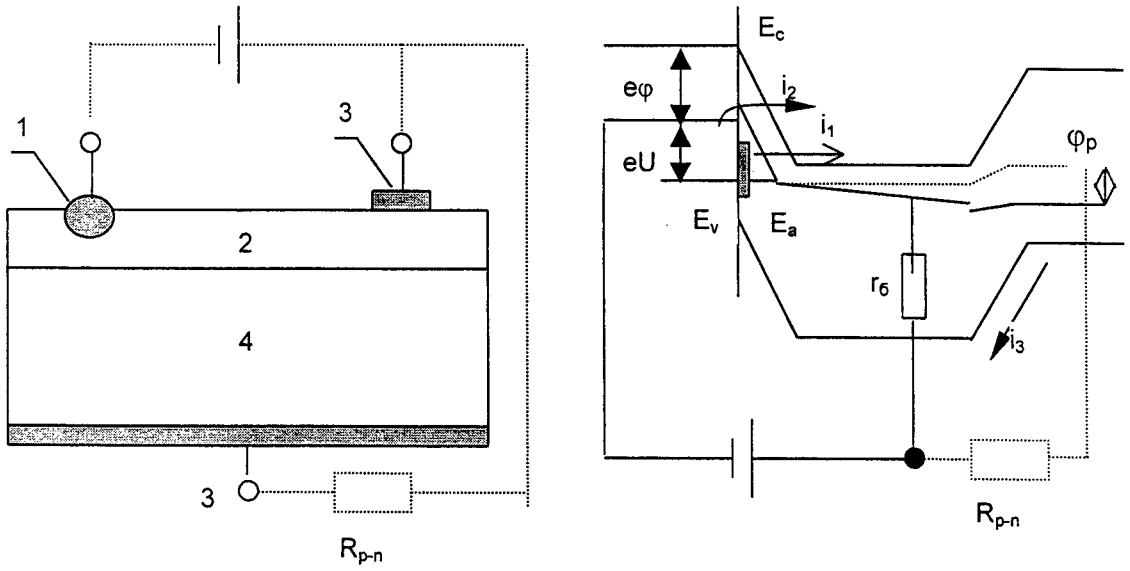


Fig. 1

a) schematic aspect of a sample

1 - active contact, 2 - n-region, 3 - ohmic contacts, 4 - p^+-region

b) the energy diagram of structure

E_a - energy levels entered by an admixture, e_a - height of a barrier of active contact, U_a - affixed voltage, φ_p - floating potential p^+-region, i_1 - current of electrons from deep levels, i_2 - current through a barrier, i_3 - current extraction of holes, E_c - edge of a conduction band, E_v - the edge of a valence band (Dotted lines is show the switching on of a voltage source and resistor R_{p-n} to structure).

argentum by means of light forming (by impulse voltage thin (10 microns) wires of the mentioned materials located on n-field of the plate.

Research of parameters of deep energy levels entered in AC by a method of their electrical recharging [2] has shown, that in silicon samples the depth of seam of levels makes 0,45 eV from a valence band (Cd), the section of an electron capture $Sn=10^{-14}$ cm^2 and 0,17 eV (Pb+Sn), $Sn=5\bullet10^{-13}\div10^{-14}cm^2$. In germanium samples the depth of seam of levels made 0,25-0,26 eV, and the section of an electron capture $Sn=10^{-15}\div5\bullet10^{-15}cm^2$.

The important feature of electrophysical processes in investigated structures defining difference them from known transistor structures, as was shown in [1], is the

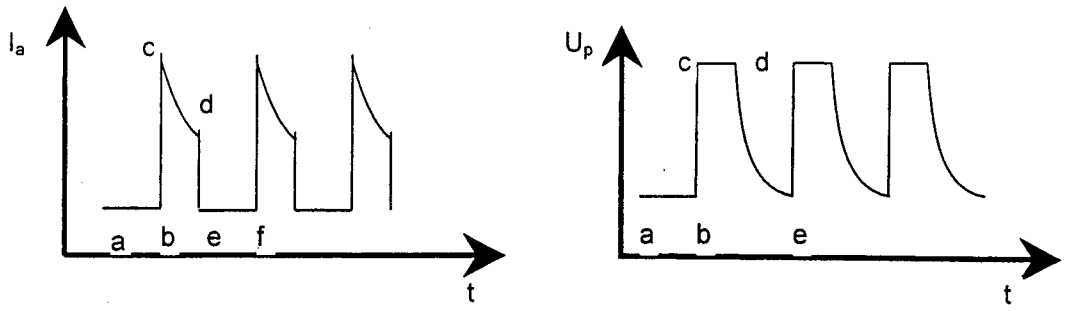


Fig. 2

accumulation of minority carriers in n-region (basis) and origin of instability of a current. The oscillograms of oscillations of a current through AC $I_к$ and voltage on p^+-region U_p are shown in a fig. 2

Let's consider physical processes causing dependences $I_к$ and U_p from time, on a site *ab* there is a reallocation of a charge in structure: the accumulation of minority carriers in basis and bound with it a contraction of region of a space charge AC and p^+-n-junction bound up with it on the site *bc* occurs a tunnel breakdown AC and emission of electrons in basis (fig. 1), and because of compensation of a charge of holes by electrons, going into from metal, the region of a space charge p^+-n-junction is dilated, its depletion-layer capacitance diminishes, and there is a sharp jump of potential on p^+-region. The site *cd* corresponds to the course of a current through a reduced barrier AC and its step-by-step diminution at the expense of a recombination of electron - hole pairs. The site *de* corresponds to restoring of a potential hill AC and restoring of an initial value of a current through AC. On a site *ef* the process of a recombination of carriers, accumulation in basis of vacant electron sites and step-by-step contraction of region of a space charge up to a critical value of its breadth corresponds to a breakdown is prolonged. Further processes iterate. The time relevant to a site *ef*, is defined by velocity of accumulation of holes in basis and is a period of oscillations, originating in structure. As researches have shown the velocity of accumulation of holes essentially depends on magnitude of the resistor $R_{p\text{-}n}$ switching on the parallel connection p^+-n-junction and from intensity of irradiating of basis by a light with a wavelength in the field of an own absorption of the semiconductor.

The surveyed features of electrophysical and photoelectric performances cause the following 3 modes of operations of the structure:

1) a "enclosed" state, when through structure the inappreciable back currents of p^+-n-junction (0,1-1 mkA and less) and AC (0,1 mA and less) flow past only, to this state there corresponds quasistationary allocation of carriers in AC and process of accumulation of holes in basis;
2) a condition of generation of oscillations thus the current through AC varies periodically from 10^{-6} up to 10^{-2} A, and voltage on p^+-region from 0,5 V up to voltage close to voltage of the power supply. To this condition there corresponds periodic accumulation and diffusions of holes in the basis;
3) a high-conductivity state, when through AC the direct current which magnitude is defined by resistance of a load R_n and distributed resistance of basis r_b flows past.

The translation of the structure from one state in another is carried out by the change of density and velocity of accumulation of holes, which is defined by change of parameters of an exterior electric circuit and exterior effects.

The detected features of electrophysical and photoelectric performances of investigated structures have allowed to create a series of is basic; in essence new gears: the generator of rectangular and sawtooth impulses, hierarchies photodetector conversing analogue change of power of radiation to a pulse repetition rate of a current, the time-pulsing optoelectronic transformer etc. The outlooking of gears is defined by presence of several channels of management, high responsivity on an input, major magnitude of an output signal, wide gamut and simplicity of reorganization of a pulse repetition rate of a current through AC and tooth voltage originating on p^+-region.

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High-Temperature Glass-Ceramic Substrates for Thin Film Electronics

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I. INTRODUCTION

The economical production of thin film polycrystalline silicon electronic devices, including solar cells and active matrix liquid crystal displays (AMLCDs), requires transparent substrates that can be processed at high (>700°C) temperatures. The most heat resistant commercial glass substrates soften at temperatures above 620 °C. Fused silica (often referred to as 'quartz') is transparent and meets the temperature requirements but is expensive and its thermal expansion coefficient is 1/5 of that of silicon, leaving a polysilicon layer deposited at high temperature under a tensile stress.

Glass-ceramics offer an alternative to glass to fabricate transparent, high-temperature substrates that can be matched to the thermal expansion of silicon. The strategy is to keep the grain size small (< 150 Å) to reduce scattering of the light and to control the valence state of Ti to avoid coloring of the substrate. The main concern in processing glass-ceramics is that the glass components can out-migrate from the substrate and contaminate the device.

II. GLASS-CERAMIC SUBSTRATES

After surveying glass-ceramic systems, the composition system SiO_2-Al_2O_3-ZnO-MgO-TiO_2-ZrO_2 was selected [1]. The final microstructure of the glass-ceramic consisted of 10-15 nm-sized spinel crystals, dispersed uniformly in a siliceous glass matrix. The transparency of 2 mm thick uncoated glass-ceramics was over 90 %.

Some glass components, such as alkali atoms, are mobile at elevated temperatures and can migrate out of the substrate during high temperature processing [2]. To prevent the out-migration of substrate components into the thin film electronics the glass-ceramic substrates need to be coated with a barrier layer.

After investigating various schemes, a barrier layer consisting of 1000 Å of SiN_x followed by 1000 Å of SiO_2, both deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD), was selected. To check the effectiveness of the barrier layer in stopping ion out-migration, coated substrates were annealed in N_2 at 900 °C for 8 hours. Secondary ion mass spectroscopy (SIMS) showed that the concentration of glass components dropped in the SiN_x layer and reached background levels in the following SiO_2 layer.

To demonstrate the suitability of these substrates for thin film electronics at high temperatures, both majority carrier devices (thin film transistors) and minority carrier devices (p-i-n junction diodes) were fabricated.

III. THIN FILM TRANSISTORS

Thin Film Transistors (TFTs) permit quantitatively measurement of the carrier mobility and density of mid–gap states in polysilicon. To competitively evaluate various substrates TFTs were fabricated on oxidized single crystal silicon (8600 Å thermally grown), barrier layer coated glass-ceramic and fused silica substrates. The 1000 Å thick channel polysilicon was deposited by LPCVD at 550 °C as amorphous and then recrystallized at 900 °C. The gate oxide was also deposited by LPCVD at 450 °C. A detailed process description can be found at [3,4]. The device characteristics were analyzed using a combination of classical MOSFET theory [5] and TFT theory [6].

Non-hydrogenated TFTs fabricated on all substrates had lower leakage currents and higher carrier mobility (Table 1) than devices fabricated previously on Corning 1737 glass substrates at 620 °C [4]. Figure 1 shows typical current-voltage ($I_d(V_g)$) curves for TFTs fabricated on various substrates. Figure 2 presents the corresponding densities of gap states (DOS) in polysilicon gap deduced by the temperature method [7]. It should be noted that the performance of TFTs on glass-ceramic and fused silica substrates exceeds those on oxidized silicon wafers. Possible reasons for different performance of TFTs fabricated on different substrates include different grain structure, different gettering ability of substrates, and the electric field distribution in TFT with and without a ground plane, all of which are being investigated

IV. P-I-N JUNCTION DIODES

To investigate if glass-ceramics would make suitable substrates for thin polysilicon film solar cells, we fabricated and tested p-i-n junction diodes on barrier layer coated glass-ceramics, fused silica substrates and oxidized silicon wafers. The device consisted of 500 Å n+, 6000 Å undoped (i-) and 1500 Å p+ polysilicon deposited at 550 °C and annealed for 4 hours at 900 °C. Grain size of the deposited polysilicon film ranged from 100 Å to 1000 Å. The structures were patterned by photolithography and etched to form isolated devices. Aluminum contacts were deposited on the top and annealed in H_2 at 400 °C for 0.5 hour.

The dark current-voltage characteristics (I-V) were measured and analyzed. P-i-n junctions on both glass-ceramic and oxidized silicon substrates had low reverse leakage currents and high breakdown fields, while on fused silica device performance was much poorer (Fig. 3). Oxidized silicon and glass-ceramic substrates have a coefficient of thermal expansion (CTE) matched to Si, whereas fused silica does not. During cooldown from the high temperature anneal the difference in CTE induces a tensile strain of 0.2% into the polysilicon film. The corresponding tensile stress can reach 60 000 psi exceeding breaking strength of polysilicon which is between 10 000 and 35 000 psi [8]. Visual inspection confirmed the formation of cracks in the polysilicon films that degrade the performance of large area devices fabricated on fused silica substrates.

The forward current-voltage characteristics of solar cells and p-i-n diodes followed an exponential law with ideality factor of ~ 2. This behavior is expected for semiconductor materials such as polycrystalline silicon containing near mid-gap recombination states [9].

V. SUMMARY

Novel transparent glass-ceramics having high strain point (over 920 °C) and CTE matched to Si, developed by Corning Incorporated, were shown to be suitable substrates for high temperature fabrication of thin film polycrystalline solar cells and thin film transistors. Out-diffusion of glass components from the substrate was effectively suppressed with a PECVD SiO_2/SiN_x barrier layer.

Thin film transistors fabricated at 900 °C on glass-ceramic substrates had leakage currents and electron mobilities comparable to devices on fused silica and oxidized silicon wafers.

The performance of p-i-n junction diodes, simulating solar cells, fabricated on the glass-ceramic substrates matched that of devices made on oxidized silicon. The difference in thermal expansion coefficient of silicon and fused silica was shown to be the reason for the poor performance of p-i-n diodes fabricated on fused silica substrates.

ACKNOWLEGMENTS

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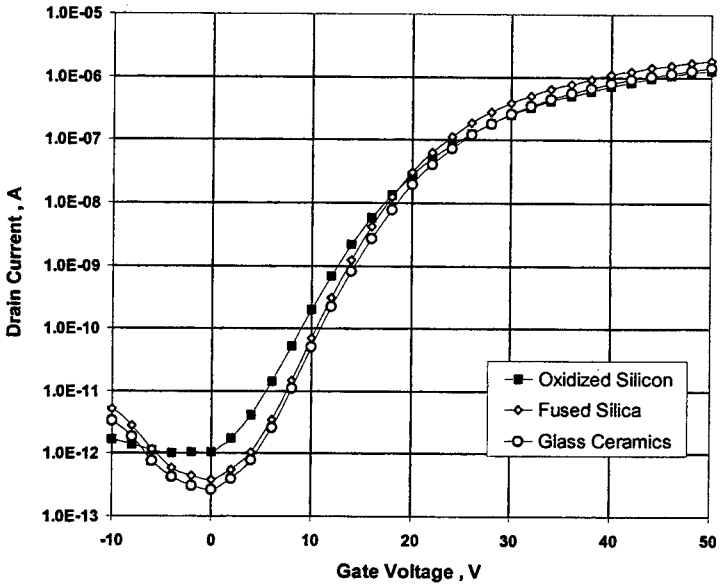


Figure 1. Current-voltage characteristics of thin film transistors fabricated on oxidized silicon, fused silica and glass-ceramic substrates. Channel size is 15 x 15 mkm^2. Source-drain voltage V_{sd} = 0.15V.

	V_{fb}, V	I_{min}, pA	mobility, cm^2/V·sec	Q_t, 10^{12}cm^{-2}	S, V/decade
Oxidized Silicon	-1.5	0.97	68.3	2.1	3.48
Fused Silica	0	0.38	220	2.1	3.00
Glass-Ceramic	-0.5	0.27	179	2.2	3.05

Table 1. Parameters of TFTs fabricated on glass-ceramic, fused silica and oxidized silicon wafers. The columns list, left to right, the flat band voltage, V_{fb}; the leakage current, I_{min}; the intrinsic electron mobility; the trap density Q_t; the subthreshold slope S.

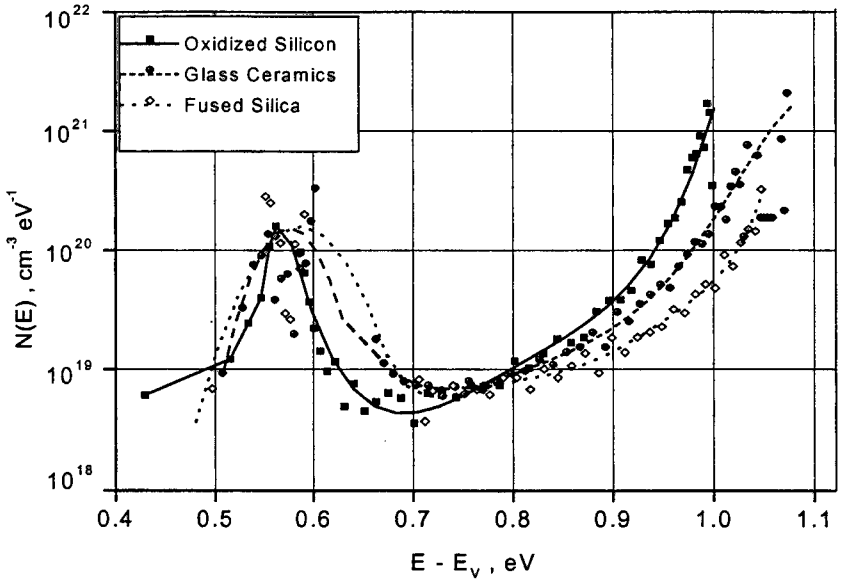


Figure 2. Densities of gap states in polysilicon films deposited on oxidized silicon, glass-ceramic and fused silica substrates. DOS were deduced by the temperature method [7] (dots). Lines are guides for the eye only.

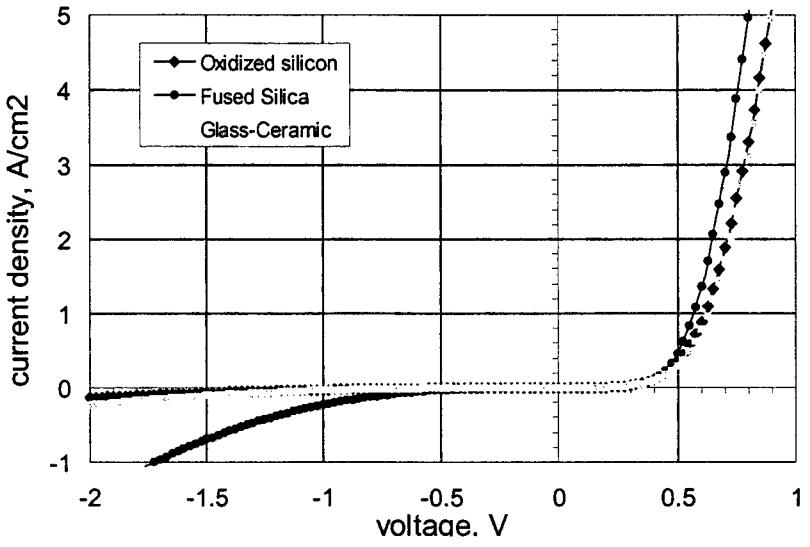


Figure 3. Dark current voltage characteristics (I-V) of p-i-n junction diodes fabricated on oxidized silicon, fused silica substrates and barrier layer coated glass-ceramic.

DECELERATION OF PICOSECOND RELAXATION OF GaAs BLEACHING AT INTENSIVE SUPERLUMINESCENCE

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At room temperature, we have investigated GaAs thin (~ 1 μm) layer bleaching, i.e., an increase of transparency, which arises as a result of photogeneration of dense hot electron-hole plasma (EHP) by a powerful 14 ps light pulse with the photon energy $\hbar\omega_{ex}$ slightly above the band gap width E_g. The picosecond relaxation of GaAs bleaching is experimentally found to decelerate with increasing light beam diameter F. The bleaching relaxation is caused by a carrier density decrease due to recombination superluminescence (i.e., amplified spontaneous emission) appearing in picoseconds in GaAs. As follows from the revealed bleaching deceleration, the superluminescence recombination rate slows down as the diameter F increases, despite the fact that the superluminescence radiation intensity must increase. We explain this apparent contradiction by the fact that the intensity of picosecond superluminescence is estimated to be very high ~10^8 W/cm^2, so the negative feedback appears between the temperature of dense EHP and the superluminescence intensity. The feedback occurs due to EHP heating caused by the recombination superluminescence. With approximately the same characteristic time τ_r ~10 ps, the feedback controls the picosecond relaxation of the bleaching, the concentration and temperature of EHP, and the superluminescence. The revealed experimental dependence of time τ_r on diameter F is satisfactorily described by relation (1), given below, which was obtained by Bronevoi *et al.* [1] using the theory of Kalafati *et al.* [2]. Practical application of the present study lies in the fact that the manifested feedback should control the decay of intensive ultra-short radiation pulses of semiconductor lasers and superluminescence diodes as well as the bleaching relaxation of GaAs picosecond modulators of the optical transparency.

Previous investigations [3-6] describe the relaxation process as follows. Under the experimental conditions, the GaAs bleaching mostly reflects the EHP concentration changes. Both nonequilibrium EHP concentration and the corresponding bleaching begin to decrease in a few picoseconds after the exciting light intensity have gone through the maximum, when EHP cooling begins. During the cooling, the occurring charge carrier transport from high to lower energy levels maintains the carrier population inversion. Recombination superluminescence that appears in picoseconds prevents the inversion band increase and lowers EHP concentration with the EHP cooling. The superluminescence recombination within the picoseconds' time interval provides EHP concentration relaxation down to a residual level, which at a fixed diameter F is independent of both photon energy $\hbar\omega_{ex}$ and the integral energy of the exciting pulse. When the residual level is reached, EHP temperature T_c becomes close to the room temperature, the superluminescence decays, and the energy distribution of EHP is approximately characterised by the conditions (1) $n = p$ and (2) $\mu_e - \mu_h \approx E_g$, where n and p stand for the concentrations of electrons and holes, and μ_e and μ_h are Fermi quasi-levels of electrons and holes, respectively. Note that the energy distribution of EHP during the cooling can also be characterised by these two conditions, if we neglect that small part of EHP concentration whose subtraction eliminates the population inversion.

As the diameter F of the photoexcited GaAs region increases, the superlumines-

cence intensity B_ω must increase [7], and one could expect that the superluminescence recombination rate $(dn/dt) \sim \int \alpha_\omega (n,T_c)\, B_\omega\, d\omega$ would also increase, where ω is the light frequency and α_ω is the light gain, and the integral is taken over the spectral band of the light amplification. Experimentally, as was mentioned above, we have found just the opposite effect: "picosecond" relaxation of bleaching and, correspondingly, EHP concentration down to the residual level decelerates with increasing diameter F. Hence, the decrease of (dn/dt) is caused by the decrease of α_ω, as is explained below.

The bleaching relaxation was studied with the excite-probe method. The superluminescence characteristics were investigated in [5,8]. The bleaching was described by the ratio $\log(T^1/T^0)$, where T is a transparency, the indices 1 and 0 denote the presence and absence of excitation, respectively. At the used probe photon energy $\hbar\omega_p$ = 1.568 eV the bleaching mostly reflects the EHP concentration changes, which is confirmed by the experimental and calculated bleaching spectra for different T_c and n [3,6]. The relaxation is found to be an approximately exponential function of time (See Fig. 1) and the characteristic relaxation time τ_r is found to increase with increasing diameter F (See Fig. 2), following relation (1) below. The level of the residual bleaching increased with decreasing diameter F, because the superluminescence decays at small diameters F, when certain population inversion is still preserved [1,2].

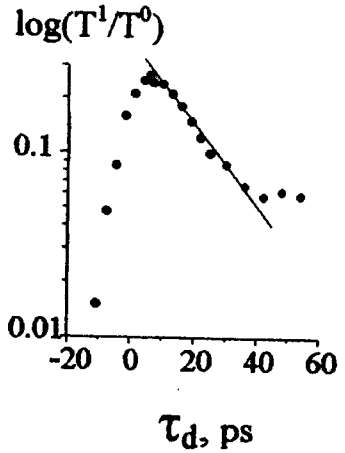


Fig. 1. GaAs bleaching as a function of the time τ_d of the delay between the probe (p) and exciting (ex) pulses. $\hbar\omega_{ex}$ = 1.485 eV, $\hbar\omega_p$ = 1.568 eV, F = 0.7 mm; the bleaching is shown in semi-log scale. As is determined from the plots, τ_r = 19 ps. Solid lines are depicted to be certain that the bleaching relaxation is approximately exponential function of time.

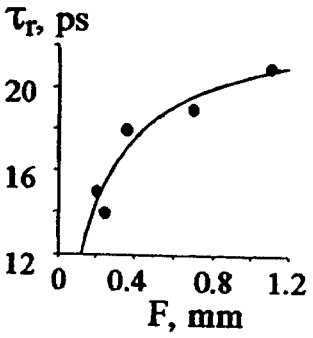


Fig. 2. The relaxation characteristic time τ_r as a function of the diameter F: • - experimental date, solid line - calculation.

We believe that the revealed deceleration of the bleaching and EHP concentration relaxation with increasing diameter F is caused, as was noted above, by a decrease of the light gain α_ω. The related carrier population inversion decrease is due to EHP heating by intraband superluminescence emission absorption, because the absorption probability increases with increasing F. Less population inversion must lead, in particular, to concentration of the superluminescence spectrum in a longer-wavelength region at a larger diameter F, which was observed in the experiment. According to the above explanation of the effect of relaxation deceleration, the dependence of τ_r on F is satisfactorily described by the relation [1,2]

$$\tau_r = 2/3(BT_c^{1/2}E_g/c(\gamma+F^{-1}) + A)\tau_h, \quad (1)$$

Here, the first term in the sum accounts for the relaxation deceleration due to EHP heating caused by the intraband absorption of the superluminescence. The second term corresponds to EHP heating caused by the fact that the energy of the charge carriers participating in the superluminescence is less than the average energy of the carriers in EHP. The parameters A and B were set at $A = 8.5$ and $B = 0.57$ in order to best fit the experimental data, and differ a little from the theoretical values of $A = 6.2$ and $B = 0.34$; c stands for the light speed in the medium and $\tau_h = 0.8$ ps is the EHP cooling time due to LO-phonon emission. The values of $T_c = 400$ K and $n = 2.8 \cdot 10^{18}$ cm^{-3}, average over the time of the bleaching relaxation to the residual level, were determined from the dependencies of the bleaching on T_c and n in works [3,6]. The intraband light absorption $\gamma = 54$ cm^{-1} was determined from concentration n according to [9]. The time variables in relation (1) were measured in picoseconds, T_c in K, and E_g in eV.

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Low-Frequency Electrical Noise of High-Speed, High-Performance 1.3-μm Strained MQW Gain-Coupled DFB Lasers

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Abstract

New results on the low frequency noise in high-speed, high-performance 1.3-μm strained MQW gain-coupled DFB lasers are presented. Above the lasing threshold current I_{th}, 1/f noise scales with the square of I_d and it is origin is the series resistance out of the active region due to mobility fluctuations. Below I_{th}, the 1/f noise arises from the active region and is due to fluctuations in the rate of spontaneous recombination from band-to-band and the rate of carriers' tunneling through the barriers between the multi-quantum-wells.

Introduction

Long haul and high bit-rate communications and the broadcast requirements of many channels are highly desirable in future communication systems. To meet such a demand, the only choice is to develop optical communication systems. Therefore, intensive efforts have been made to develop semiconductor lasers with high power, high-speed and low relative intensity noise. As a result, 1.3-μm gain-coupled distributed feedback (DFB) lasers with etched quantum wells to provide both gain and index coupling to achieve a high yield of single-mode operation were fabricated recently.

For optimizing performance of fiber-optic communication systems, it is necessary to understand both electrical noise and optical noise properties of photonic devices like semiconductor lasers, optical amplifiers, and wavelength converters. With respect to semiconductor lasers, the low-frequency electrical noise (LFN) is of a great interest because of its strong correlation to optical noise. To date, only few publications can be found about the LFN in semiconductor lasers. The LFN in diodes type devices has been investigated intensively. However, the achievement can not be applied to analyze the LFN of MQW laser diodes because the current conduction mechanism in MQW laser diodes is substantially different from that in conventional semiconductor diodes.

In this paper, new results of electrical noise measurements in high-speed, high-performance 1.3-μm strained multi-quantum-wells gain-coupled distributed-feed-back (DFB) lasers are presented. In particular the injected current dependence of LFN is investigated over a wide range of injection current (from 10^{-2} μA to 60 mA). The current dependence of the 1/f noise strongly correlates to the I-V characteristics. We discovered that noise from different mechanism dominates when the lasers operate in different ranges of injection currents.

Noise and Device Details

Low-frequency electrical noise of high-speed, high-performance 1.3-μm Strained MQW Gain-Coupled DFB lasers has been investigated over a wide range of injection currents. We have found that the noise is dominated by pure 1/f noise and different noise mechanisms were observed when the laser diodes operate at different injection current levels. Above the lasing threshold current, the 1/f noise scales with the square of the injection current. This 1/f noise stems from the series resistance out of the active region due to mobility fluctuations. Below the lasing threshold current, the 1/f noise arises from the active region. The origin of the 1/f noise is fluctuations in the rate of spontaneous recombination from band-to-band and the rate of carriers' tunneling through the barriers between the multi-quantum-wells.

Experimental Results

Fig. 1 shows the structure of devices that were fabricated by two-step metal organic chemical vapor deposition (MOCVD). The etching into the active region and the regrowth on the grating were carried out with good wafer to wafer reproducibility and with excellent morphology analyzed by a transmission electron micrograph. A nice feature of these etched quantum wells is that the carriers (holes in this case) can be transversely and laterally injected into the quantum wells along the longitudinal direction, thus reducing the carrier transport time, and as a results the device is expected to operate at a higher speed. Fig. 2 shows the I-V characteristics and dynamic conductance G_d versus bias voltage. Fig. 3 shows the light-current and efficiency-current characteristics. Fig. 4 shows the measurement system, fig. 5 a typical set of noise spectra, and fig.6 the S_I versus I_d. characteristics. The electrical noise was measured with bias-current varying from 30 nA up to 60 mA. Fig. 7 shows S_I versus I_d at 1 Hz and fig. 8 shows G_d versus V, for all samples. It is clear that the curve of current dependence of S_I and G_d is composed of several segments. This reveals different noise sources existing in the laser diodes when the laser diodes operate in different ranges of injection currents.

Conclusions

In conclusion, we found that above the lasing threshold current, the 1/f noise scales with the square of the injection currents. This 1/f noise stems from the series resistance out of the active region due to mobility fluctuations. Below the lasering threshold current, the 1/f noise arises from the active region. The origin of the 1/f noise is fluctuations in the rate of spontaneous recombination from band-to-band and the rate of carriers' tunneling through the barriers between the multi-quantum-wells. These results will help in designing better low-noise lasers.

Acknowledgements

The authors are grateful to Nortel Networks for providing the lasers used here. We are also grateful to Dr. R. Mallard for his advice and assistance, and to NSERC of Canada and Micronet for partial financial support of this project.

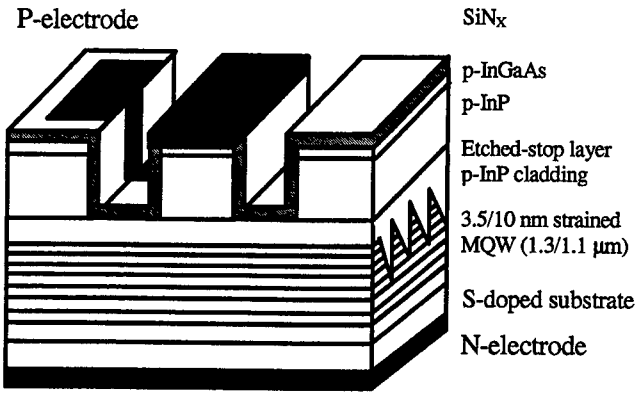


Fig. 1: Schematic cross-section of a 1.3 μm strained MQW gain-coupled DFB laser with the ridge waveguide structure.

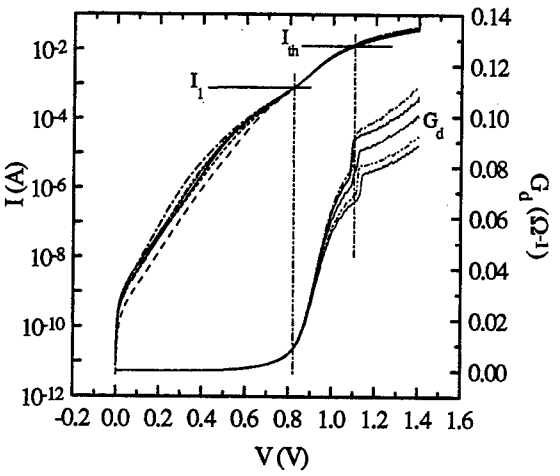


Fig. 2: Injection current I versus bias voltage V and dynamic conductance G_d versus bias voltage V. I_{th} and I_1 separate the curve into three parts.

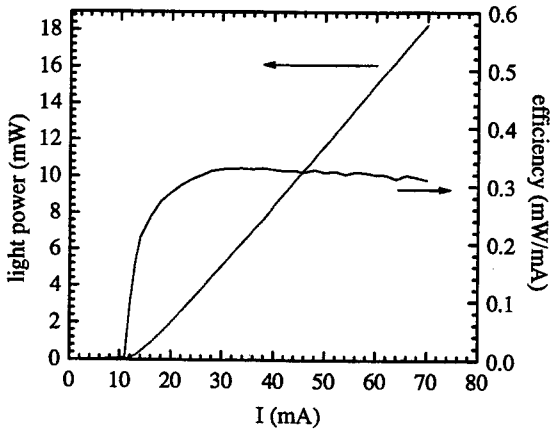


Fig. 3: Light power versus injection current and the efficiency versus injection current at 25°C. The lasing threshold current is equal to 13.4 mA for this sample.

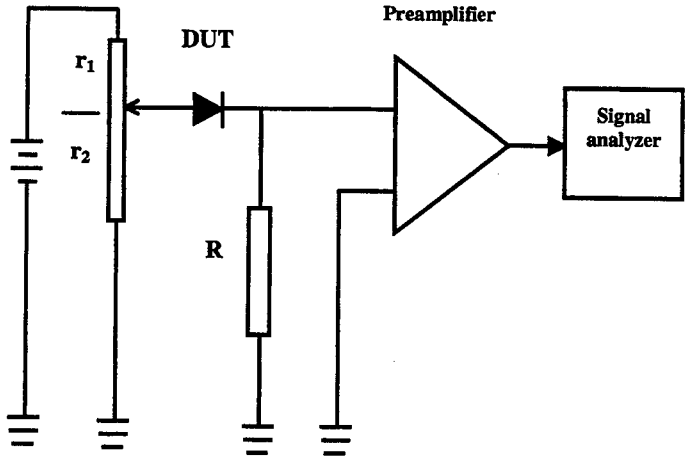


Fig. 4: The circuit configuration for noise measurements.

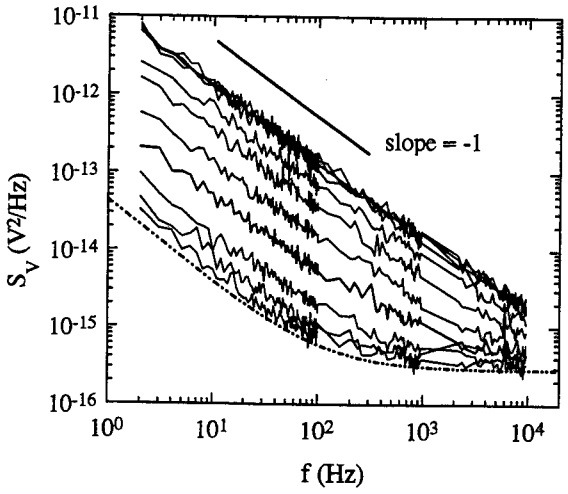


Fig. 5 S_V versus f, typical measured noise power spectral density. Dished line: the background noise. Solid lines are measured spectra at currents from $3x10^{-2}$ μA to 60 mA. The straight line for guide the eyes.

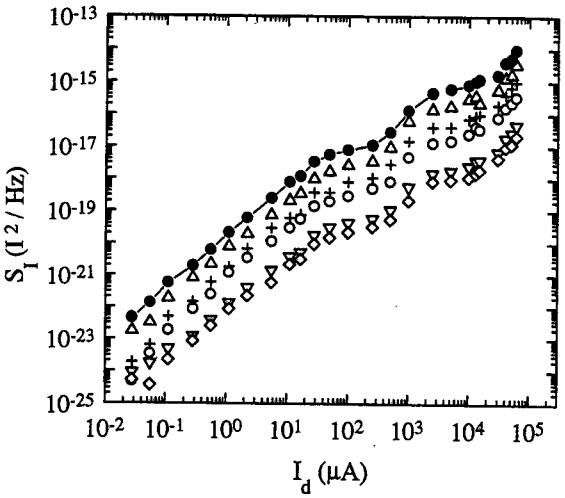


Fig. 6: S_I at different frequencies versus injection current in one of six samples. The frequencies, from top to bottom, are 1, 3, 11, 25, 250 and 400 Hz.

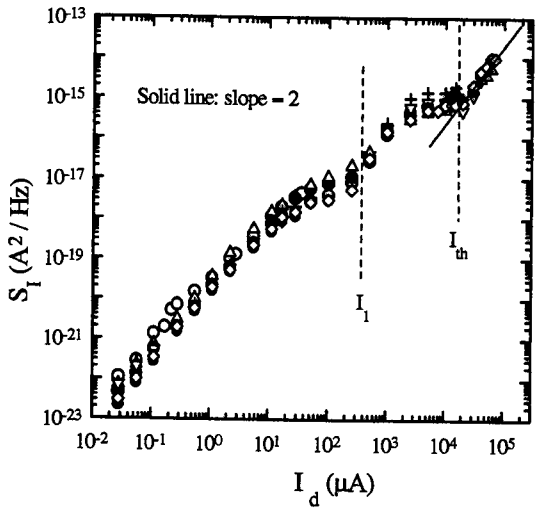


Fig. 7 S_I at 1Hz versus injection current I_d for all measured lasers. The different symbols are for different samples. I_{th} and I_1 separate the curve into three parts.

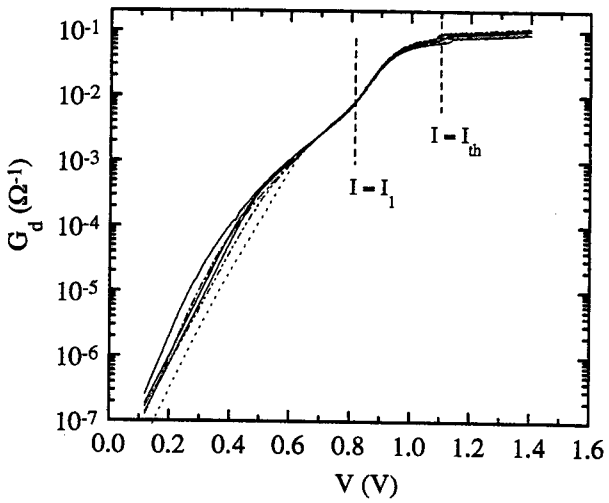


Fig. 8: Dynamic conductance G_d versus bias voltage V for all 6 smaples. I_{th} and I_1 separate the curve into three parts.

THICK PLZT SPATIAL PHASE MODULATOR DESIGN AND OPTIMIZATION

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I. INTRODUCTION

Lanthanum-modified lead zirconate titanate (PLZT) films have unique ferroelectric and optoelectronic properties that find their applications in ferroelectric memories (FRAMs), optical switches, displays, optical modulators and variety of other optical devices [1]. Many of the devices are build on ceramic bulk PLZT films and, thus, require high operating bias as compared to thin film epitaxial PLZT electro-optical devices operating at much lower voltages [2,3]. Thin PLZT films have been prepared by both physical deposition and sol-gel process.

By using thin epitaxial PLZT film, an efficient Spatial Phase Modulator has been designed that operates at low applied bias and has low power dissipation. This device is small in size and is totally monolithic so that it does not require wafer fusion. PLZT Spatial Phase Modulator is designed to produce random-access optical beam steering due to the applied programmable voltage bias steps. The deflection angle of the incoming beam can be changed by programming the applied voltages without changing the geometry of the electrodes. The speed of altering of the steering angle depends only on the switching time of the PLZT thin film.

II. DESIGN OF MODULATOR

Spatial Phase Modulator is based on the ferroelectric lanthanum-modified lead zirconate titanate, $Pb_{0.91}La_{0.09}Zr_{0.65}Ti_{0.35}O_3$ (PLZT 9/65/35) thin film which exhibits strong electro-optic effect. The PLZT films with this composition are very attractive for many optical applications since they have large quadratic electro-optic coefficients under an applied electric field, R_{11}=3.0 10^{-16} m^2/V^2 and R_{12}=2.42 10^{-16} m^2/V^2, and refractive index of 2.5 [4]. In addition, 9/65/35 PLZT is a material with a fast switching response, good thermal stability and broadband optical transmission range [4]. With no applied electric field, the PLZT film is optically isotropic. Under the applied electric field, PLZT undergoes a transition from an optically isotropic cubic phase to a rhombohedral or tetragonal ferroelectric phase with a quadratic optical anisotropy.

Spatial Phase Modulator consists of PLZT thin film which is grown on top of MgO buffer layer and GaAs semi-insulating substrate as seen in Figure 1, side view of the Modulator. Figure 2 presents top view of the device with 50 surface interdigitated ground and source transparent indium tin oxide (ITO) interconnects that are formed on 7μm thick PLZT film. When a polarized laser beam is passing through the Modulator as presented in Figure 1, it experiences a linear phase shift due to anisotropy of PLZT film under programmed bias, and thus the beam is deflected from its initial direction. The phase modulator has critical dimensions of 650μm by 506μm, where center-to-center spacing between electrodes is 10μm and each electrode is 6μm wide.

Simulations have been carried out by the authors that include calculations of the applied electric field distribution inside PLZT film, induced changes in the refractive index distributions as well as the total phase shift of the light that is travelling thought the device.

It has been demonstrated that the Modulator presented in Figures 1 and 2 would produce an optical beam steering of the HeNe laser beam (λ=0.633μm) with the deflection angle of 0.453° when a particular voltage sequence is applied to the ITO interconnects which is given in the Table 1. The corresponding induced phase shift distribution across the device aperture is linear as shown in Figure 3 under the applied bias.

Applied bias sequence	**Phase shift produced**
$V_1 = 28.4$ V	$\Delta\varphi = 1.57$
$V_2 = 40.0$ V	$\Delta\varphi = 3.14$
$V_3 = 49.2$ V	$\Delta\varphi = 4.71$

Table 1. Phase Modulator applied bias sequence with deflection angle of 0.453°.

III. SOL-GEL MATERIAL ISSUES

Sol-gel is one of the potential techniques used for the growth of thin PLZT films for the present modulator. It offers a number of advantages over conventional physical deposition methods, such as better stoichiometric control and homogeneity, processing at relatively low temperatures, lower cost and greater flexibility for composition modification [5].

The experiment has been carried out to fabricate PLZT 9/65/35 films from an air stable sol-gel solution which consisted of the following precursors [6], $Pb(CH_3CO_2)_2 3H_2O$, $Zr(n\text{-}OC_4H_9)_4$, $Ti(i\text{-}OC_3H_7)_4$, and $La(i\text{-}OC_3H_7)_3$ $1.5H_2O$, and a solvent, 2-methoxyethanol ($CH_3OCH_2CH_2OH$). The above described sol-gel solution contained 10% excess Pb. The PLZT films were spin coated on $La_{0.5}Sr_{0.5}CoO_3/LaAlO_3$ (LSCO/LAO) substrates. After the each spin coating deposition the gel films were dried at 400 C. The coating and heat treatment process were repeated several times as necessary to obtain films of the required thickness. The final film was annealed at 600 C which resulted in crystallization of the films. The films were characterized as epitaxial 9/65/35 PLZT films with (100) preferred orientation using standard X-ray and electron microscopy, microprobe techniques. Such films show excellent feasibility in attaining the required modulator performance.

IV. SUMMARY

An effective PLZT Spatial Phase Modulator has been design to produce a random-access laser beam deflection of 0.453° or smaller under the programmable applied bias steps. The highest applied voltage required to produce such deflection is only 49.2 V. The potential applications of the device include programmable optical interconnects, steering or switching devices, optical computing, displays and others similar applications.

ACKNOWLEDGMENTS

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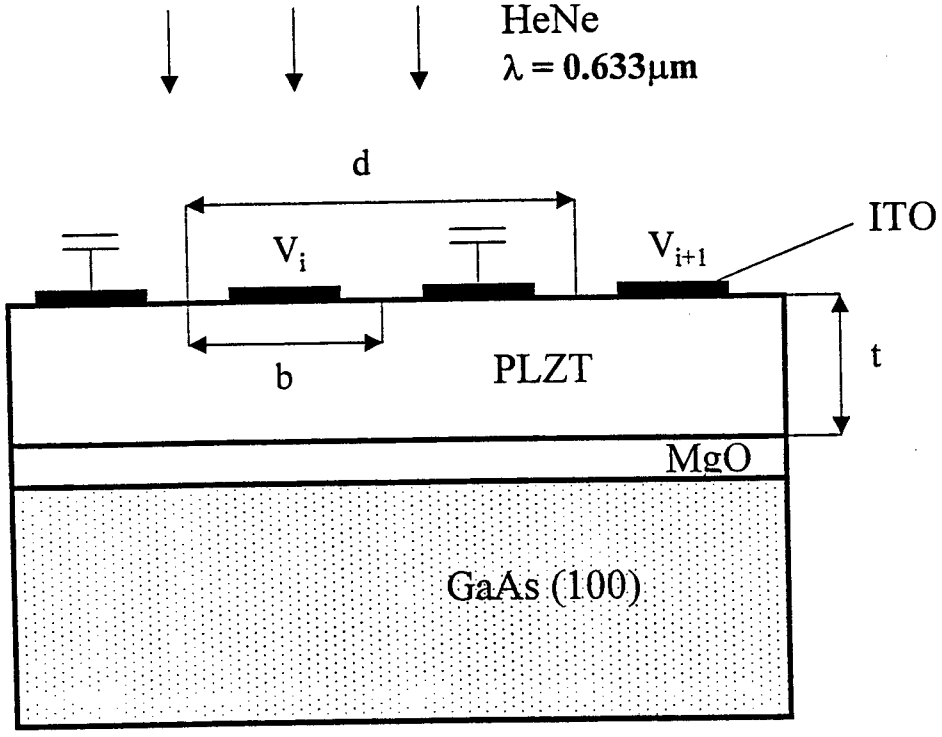


Fig. 1. Side-view representation of the PLZT Spatial Phase Modulator.

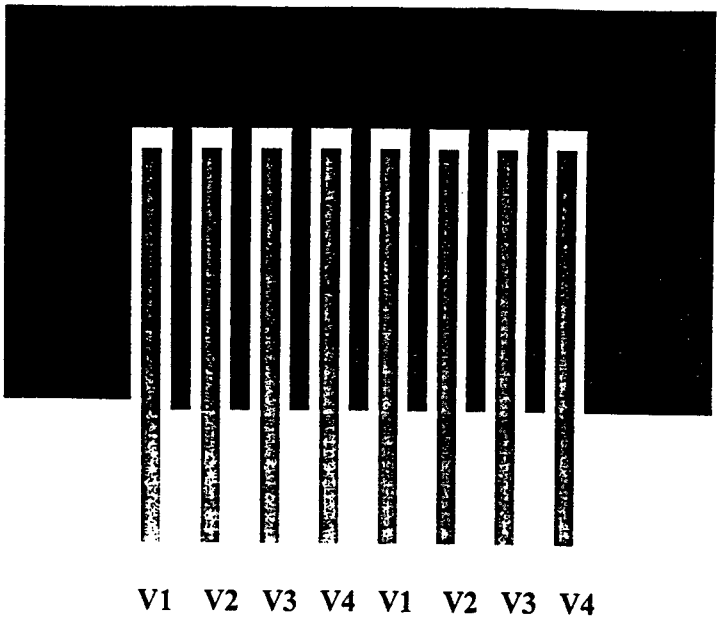


Fig. 2. Top view of the Spatial Phase Modulator.

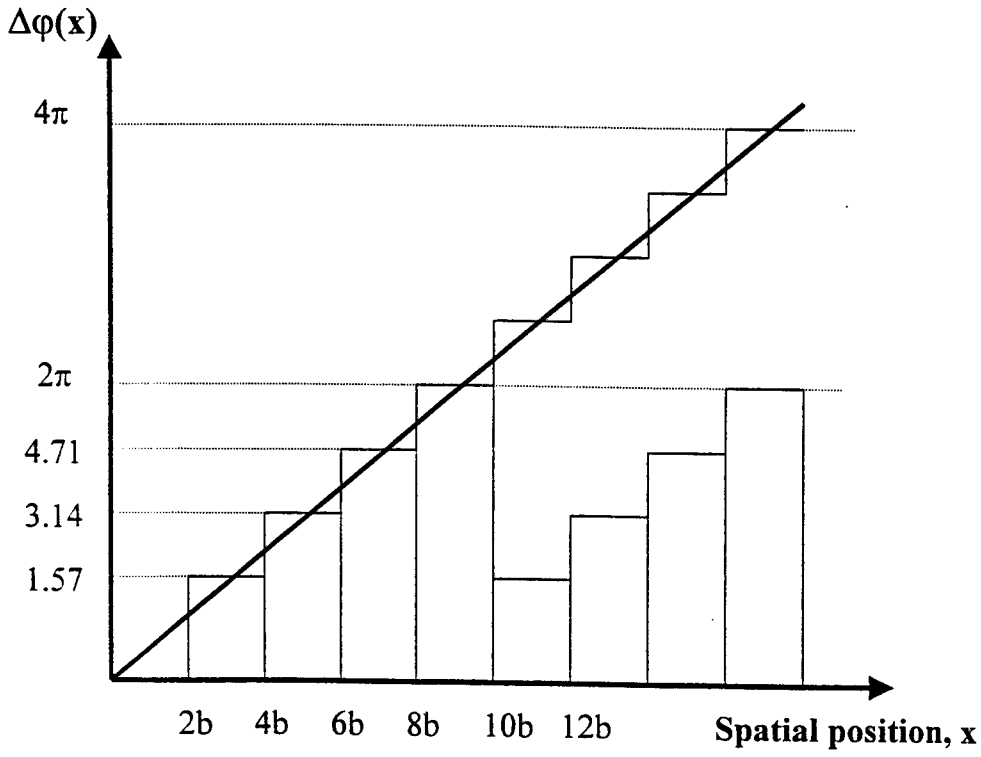


Fig. 3. Induced phase shift distribution across the Modulator aperture under the applied bias sequence.

An Analytical Opaque Gate Model for the GaAs OPFET

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ABSTRACT

Optically controlled field effect transistor (OPFET) are useful as optical devices for optical communication and as photo detector. The present work describes the realistic theoretical model for the I.V. characteristics of GaAs opaque gate OPFET. The model considers the non-uniform Gaussian doping for ion-implanted channel with schottky gate opaque to incident radiation. The radiation is absorbed in the device through the spacing between the source gate and drain gate. The importance of the present model is that there will be no photovoltage development across the schottky junction. The photovoltaic effect across the channel and the p-layer junction is highlighted. The Z/L ratio is also not very large. The following physical mechanisms are considered for the evaluation of the I-V characteristics of the device under illuminated condition.

1. Effect of surface recombination in GaAs MESFET, which takes place via deep traps either at or close to the surface.
2. The change in minority carrier life time in the illuminated condition.
3. The conductivity modulation of the channel by the incident radiation.
4. The semi-insulating nature of the substrate.

The continuity equations have been solved for excess carriers generated in the channel and low doped p-region. A comparison is made between the illuminated Gate and Opaque gate; significant increase in the device current is observed for opaque gate model. The characteristics of the device have been obtained in dark and various illuminated conditions. The theoretical works show good agreement with the empirical results and can serve as a tool for the optimal design of optically controlled MMIC and MIC.

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Quasi-Periodic Domain Structures in Quantum Well Infrared Photodetectors: Predictions from Monte Carlo Modeling

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The basic physics of QWIPs has been well understood [1]. However, the problem of the electric-field and space-charge distribution in QWIPs and their effect on QWIP characteristics still attracts considerable attention [2-6]. It is reasoned that the electric-field distribution in a QWIP with a large number of QWs consists of two parts: a narrow domain close to the emitter contact where the electric field is usually strong (charged domain) and a relatively wide region with nearly uniform electric field (quasi-neutral bulk region). In all cases the electric field in a QWIP was assumed to be a monotonic function of the coordinate directed perpendicular to the QW plane (in growth direction). The distributions of this type were calculated using drift- and drift-diffusion models of the electron transport in QWIPs and used for the experiment interpretations.

In this paper, we predict, using an ensemble Monte Carlo (MC) modeling, an instability of monotonic electric-field distributions with the excitation of the wave of QW recharging. We show that this instability in QWIPs can lead to the formation of stable large amplitude quasi-periodic electric-field distributions. Such electric-field distributions correspond to dipole distributions of the QW charges with opposite charges in neighboring QWs. The origin of the recharging instability and domain formation is associated with a nonlocal electric-field dependence of the capture of hot electrons into QWs. This instability is similar to that predicted for compensated semiconductors with the capture of electrons by the deep traps [7,8]. The inherent periodicity of the QW structure obviously can lead to interesting features of the instability and its consequences. This effect can significantly change the usual notion of physical phenomena in QWIPs.

We consider a QWIP comprising a GaAs/$Al_xGa_{1-x}As$ multiple QW structure ($x = 0.22$) sandwiched between doped contact layers. The QW structure consists of a series of N identical QWs of width L_w with a donor sheet concentration Σ_d separated by relatively thick barriers (their thickness $L_b \gg L_w$). The QW width is chosen in such a way that each QW has a single bound state while the bottom of the continuum states subband corresponds to the barrier top. The barrier thickness L_b is chosen to be large enough, hence, the inter-well tunneling is suppressed. It is assumed that the injection of electrons from the emitter contact layer into the QWIP active region is associated with the tunneling through the extreme (emitter) barrier.

We study transient processes in a QWIP at the temperature $T = 77$ initiated by a step-like pulse of incident infrared radiation resulting in the bound-to-continuum excitation of electrons. An ensemble MC particle method employed yields the transient self-consistent electric field, concentration of electrons in the continuum states;

and electron sheet concentrations in QWs. It is similar to the technique used previously [9,10]. The MC model takes into account the excitation of electrons from QWs and their capture into QWs, injection and extraction of electrons by the emitter and the collector, respectively, and transport of the excited and injected electrons in the continuum states across the QW structure under the influence of the self-consistent electric field. The capture of electrons into QWs is assumed to be primarily associated with the emission of polar optical phonons. The injected current density j_e is determined by the electric field E_e in the emitter barrier according to the following formula: $j_e = j_m \exp(-E_t/E_e)$. Here, j_m is the maximum current density from the emitter contact layer and E_t is the characteristic tunneling field. The value of j_m is determined by the doping level of the emitter contact layer, while E_t is determined mainly by the width of the emitter barrier and its height. The momentum distribution of the injected electrons corresponds to the tunneling nature of the injection from the emitter. For the MC calculations ensembles up to 50,000 particles (electrons) were used. The time-step of 10 fs was chosen.

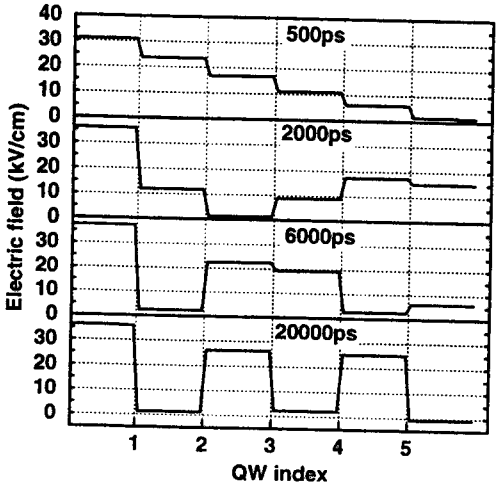


Fig. 1. Spatial distributions of electric-field in QWIP with five QWs at different moments.

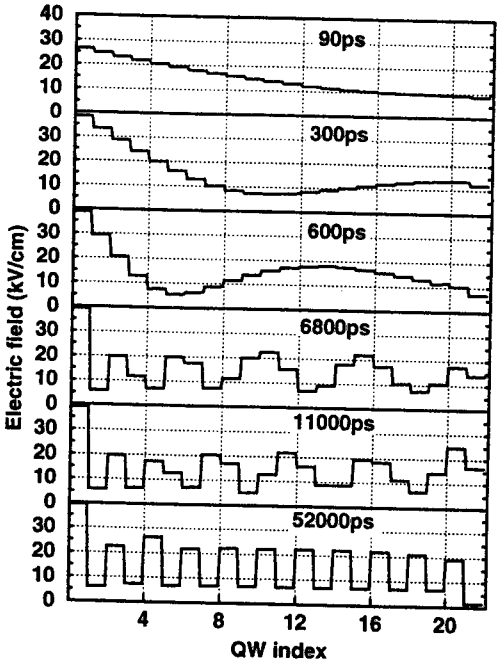


Fig. 2. Electric-field distributions in a QWIP with 21 QWs at different moments.

The QWIP parameters used in the calculations are as follows: the number of QW $N = 5$ - 50, the QWIP structure period $L = L_w + L_b = 52$ nm, the barrier donor concentration $N_d = 10^{15}$ cm^{-3}, the QW donor sheet concentration $\Sigma_d = 10^{12}$ cm^{-2}, and the characteristic emitter tunneling field $E_t = 340$ kV/cm. A QWIP with $\Sigma_d = 2\times10^{11}$ cm^{-2} was also studied for the comparison. The applied voltages V provide the average electric field in the QWIP structure $E = V/[NL_w + (N+1)L_b] = 15$ kV/cm. The initial energy of the photoexcited electrons was chosen to be $\Delta = 10$ meV. The above device parameters and average voltage are usual for the normal QWIP operation.

Figure 1 shows the transformation of the electric-field distribution in a QWIP with five QWs, under the influence of incident infrared radiation with the intensity of $I = 10^{23}$ cm^{-2}s^{-1}. It is seen from Fig. 1 that at the initial stage the electric-field distribution remains monotonic with a stepped decrease of the electric field in the

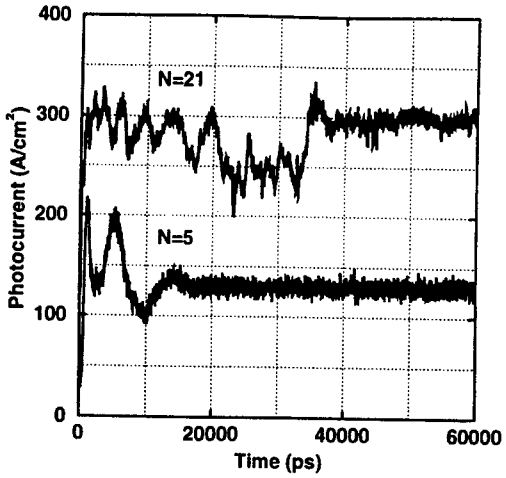


Fig. 3. Transient photocurrents for QWIP with $N = 5$ and $N = 21$.

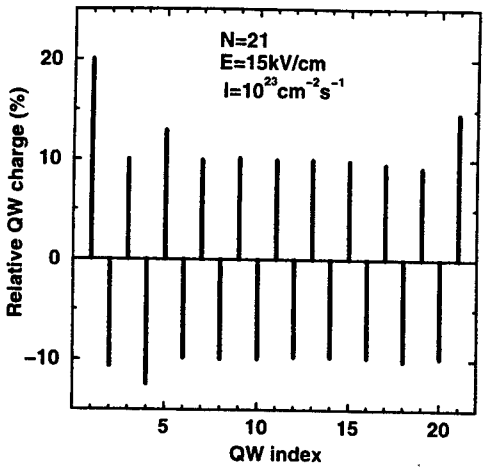


Fig. 4. Steady-state QW charges in QWIP with 21 QWs.

direction from the emitter to the collector. However, as seen from plots corresponding to the later moments, such a monotonic distribution is unstable with the excitation of a wave with alternative electric field and QW charges.

The excitation of the recharging wave in a QWIP with relatively large number of QWs ($N = 21$) for the same as above intensity of radiation is shown in Fig. 2. It is clearly seen from Fig. 2 that the wavelength gradually decreases.

At the latest stage, the electric-field distributions in QWIPs with different numbers of QWs in all cases studied become oscillatory. Figure 3 demonstrates temporal variations of the photocurrents in QWIPs with $N = 5$ and $N = 21$. One may conclude from Figs. 1, 2, and 3 that oscillatory electric-field domain structures and photocurrents in QWIPs with $N = 5$ and $N = 21$ stabilize at the times about of $t \simeq 20$ and 60 ns, respectively.

The calculations for lower intensities of radiation reveal a markedly slower development of the instability. This can be attributed to a decreasing dependence of the QW photoescape time τ with increasing intensity: $\tau = \sigma^{-1} I^{-1}$, where σ is the photoionization cross-section for the bound-to-continuum transitions. Assuming $\sigma = 2 \times 10^{-15}$ cm^{-2}, for $I = 10^{22} - 10^{23}$ cm^{-2}s^{-1} we obtain $\tau = 5 - 50$ ns. Apart from the photoescape time τ, the transient processes in the QWIP bulk are characterized by the capture time $\tau_c = L/p_c v_d$, where p_c is the macroscopic capture parameter (capture probability) and v_d is the electron drift velocity. Assuming $v_d = (5 - 10) \times 10^6$ cm/s, $p_c = 10^{-1} - 10^{-2}$, and $L = 50$ nm, we obtain $\tau_c = 0.005 - 0.1$ ns. Thus, $\tau_c \ll \tau$, and relatively slow recharging processes are primarily defined by the photoescape time. The operation of QWIPs is strongly affected by the injection from the emitter. The injection, in particular, is the origin of the QWIP photoelectric gain. The characteristic time of the injection is given by $\tau_e = E_e^2/p_c j_0 E_t$, where $j_0 \simeq e\Sigma_d \sigma I/p_c$ is the steady-state photocurrent density and e is the electron charge. Hence, one obtains $\tau_e \simeq \tau \cdot (æ E_e^2/2\pi e \Sigma_d E_t)$. The estimates show that for the parameters assumed for our simulations, $\tau_e \ll \tau$. The latter explains relatively fast establishment of the electric field near the emitter contact and the stability of its value during the recharging processes in the QWIP bulk.

An example of the distribution of the relative QW charge $(\Sigma_d - \Sigma_n)/\Sigma_d$ is shown in Fig. 4. Figure 4 indicates that the charges of QWs alter from positive (in QWs with odd indexes counted from the QW nearest to the emitter) to negative (in QWs with even indexes), creating a quasi-periodic dipole domain structure.

Steady-state and dynamic properties of QWIPs with quasi-periodic domain structure can differ from those of QWIPs with monotonic electric-field distributions and quasi-neutral bulk. This is due to significant differences in the electric fields in the barriers and the average electric field in the QW structure with a quasi-periodic electric-field distribution. As a result, the average electron drift velocity and energy in a QWIP with a quasi-periodic electric- field distribution and, hence, the fraction of electrons capable to be captured, should be different from those in the case of a monotonic distribution. Features of the electron transport in QWIPs under the conditions of the recharging instability can be responsible for the unusual behavior of the QWIP current-voltage characteristics. The formation of the domain structures in question can affect frequency- dependent characteristics of QWIPs at the frequencies comparable with τ^{-1}, τ_c^{-1}, and τ_e^{-1}. A difference in the electric fields in the barriers with odd and even indexes leads to different acceleration conditions for electrons over such barriers. This can be essential for the transit-time limited operation and ultra-high-frequency phenomena in QWIPs associated with the electron velocity overshoot effect.

In conclusion, we have studied transient effects in QWIPs stimulated by a step-like pulse of infrared radiation using a MC modeling. We have predicted that monotonic electric-field distributions in QWIPs can be unstable with the excitation of the recharging waves. The instability results in the formation of quasi-periodic steady-state electric-field and charge distributions The origin of the instability and the quasi-periodic domain formation is attributed to non-locality of the dependence of the hot electron capture rate on the electric field.

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Analysis of Dynamic Formation of Parasitic Conduction Band Barrier in SiGe HBTs

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I. INTRODUCTION

In recent years SiGe heterojunction bipolar transistors (HBTs) have been reported with impressive gain and high frequency performance [1,2]. These devices typically employ a compositionally graded base with a high Ge content at the collector end of the base, which creates a heterojunction with the silicon collector. To achieve high gain at high frequencies, the transistor must be operated at high collector current densities ($J_C \sim 1$ mA/μm^2) near the onset of base pushout. However, the presence of a valence band discontinuity (ΔE_V) at the base-collector junction modifies the physics of base pushout producing the dynamic formation of a parasitic barrier in the conduction band which degrades device performance and whose size is a function of ΔE_V and J_C [3-5]. Recently, Joseph et al. [6] have employed a numerical simulator to model the operation of SiGe HBTs at high current densities and showed that a parasitic barrier as large as 34 meV forms at current densities of ~ 4 mA/μm^2. Song and Yuan [7] and Mazhari and Morkoc [8] have presented simple models to describe the formation of this parasitic barrier. In this paper we investigate the formation of this barrier in greater detail because of its importance to device design and optimizing device performance at high current densities.

II. ANALYTICAL MODEL

A schematic profile of the electric field in the vicinity of the base-collector junction during formation of the parasitic barrier is shown in Figure 1. The field E_{pb} in the parasitic barrier region is positive inhibiting electron injection into the collector and is assumed constant. In the quasi-neutral base, there is a built-in field E_b due to the compositional Ge grading enhanced by the nonuniform base doping. Due to the high current induced base pushout, there is a small field E_{po} in the pushout region, which is negative and assumed constant for this analysis. In addition, the peak field has been pushed to the subcollector interface. This field profile is in qualitative agreement with that shown by Joseph et al. [6]. Shown in Figure 2 is the energy band diagram.

At the outset of this analysis, we note that the electron concentration n_s in the high field region in the base-collector space charge region (BC-SCR) near the subcollector is constant due to velocity saturation v_s in the base-collector space charge region (BC-SCR). It can be described by $n_s = J_C/qv_s$ where the term arises from the need for a finite electron concentration sufficient to carry the collector current. Substituting this in Poisson's equation, we can integrate to get the electric field in the vicinity of the subcollector junction, which varies linearly and peaks at the collector/subcollector junction as shown

in Figure 1. Setting the expression for the electric field on the collector side at the edge of the pushout region equal to E_{po}, we get an expression for the extent of base pushout W_{cib} given by

$$W_{cib} = W_C - \frac{\left[J_1 \frac{N_{c+}}{N_c} - J_C\right] W_{n+} + \varepsilon\, v_s E_{po}}{\left[J_C - J_1\right]} \tag{1}$$

where W_C is the collector epilayer width, N_C and N_{C+} are the collector and subcollector doping, respectively, $J_1 = qN_cv_s$ and W_{n+} is the width of the space charge region penetration in the subcollector. Integrating the field across the junction assuming E_{pb} and E_{po} are constant, we get an expression for W_{n+} that is a function of W_{cib} given by

$$W_{n+} = \sqrt{\frac{2\varepsilon}{q(N_{c+} - n_s)}}\sqrt{E_{pb}W_{pb} + E_{po}(W_C - W_{pb}) + (V_{bi} - V_{BC}) - \frac{q}{2\varepsilon}(n_s - N_c)(W_C - W_{cib})^2} \tag{2}$$

where V_{bi} is the builtin potential and V_{BC} is the applied bias, respectively, for the base-collector junction. Combining (1) and (2) and solving we get a final expression for the base pushout W_{cib} as a function of the current level J_C and V_{BC} given by

$$W_{cib} = W_C - \frac{\varepsilon}{q(N_{c+} - N_c)}\left\{E_{po} + \sqrt{\left[\frac{\frac{N_{C+}}{N_C}J_1 - J_C}{J_C - J_1}\right]\left[\frac{2q(N_{c+} - N_c)}{\varepsilon}(\phi_{po} + \phi_B + V_{bi} - V_{BC}) - E_{po}^2\right]}\right\} \tag{3}$$

where ϕ_{po} is the potential drop across the pushout region given by $E_{po}\{W_C - W_{pb}\}$ and ϕ_B is the barrier height and W_{pb} is the width, respectively, of the parasitic barrier in the conduction band. During base pushout E_{po} is negative and J_C is greater than J_1 so W_{cib} increases as J_C increases above J_1. To calculate W_{cib} using (3), we find the pushout field E_{po} as a function of J_C and V_{BC}. Setting $J_p = 0$ and $dp/dx = dn/dx$ in the pushout region and using the current density expression for J_n, we get

$$E_{po} = -\frac{v_s}{\mu_n}\frac{J_C}{\left[2J_C - J_1\right]} \tag{4}$$

where $V_T = kT/q$ and μ_n is the low field electron mobility in the collector. Finally, assuming the hole quasi-Fermi level is constant across the base-collector junction interface and using the thermionic emission theory, we get an expression for ϕ_B given by

$$\phi_B = \left(\frac{\Delta E_V}{q} - E_{po}W_{cib} + V_T \ln\left[\frac{J_C - J_1}{J_1}\right] + V_T \ln\left[\frac{N_C e^{\eta}}{N_{Bo}}\left(1 - \frac{E_b W_p}{V_T}\right)\right]\right) \Bigg/ \left(1 - \frac{E_{po}}{E_{pb}}\right) \tag{5}$$

where η is the exponential factor for the base doping profile and W_p is the width of space charge region penetration into the base.

In summary, for a given device structure and biasing (V_{BC} and J_C), we can calculate E_{po} from (4), W_{cib} from (3) (assuming ϕ_B and ϕ_{po} are negligibly small compared to the V_{bi} - V_{BC}), and then obtain ϕ_B from (5). In the following section, we calculate some numerical results as a function of the device's current level J_C and discuss their implications.

III. SIMULATION RESULTS

The above described device model was used to investigate the extent of the formation of the parasitic barrier ϕ_B and base pushout W_{cib} for the device structure of Joseph et al. [6]. Linear compositional grading from zero at the emitter to 10% Ge at the collector end of the base was assumed corresponding to ΔE_V = 75 meV at the collector junction. Assuming a base width of 90 nm with a peak doping of $5x10^{18}/cm^3$ decreasing exponentially to a collector doping of $1x10^{17}/cm^3$, a base builtin field was calculated as $E_b = -1.2x10^4$ V/cm, which yields a nearly constant value of 5 mV for the last term in (5). The current density constant J_1 was calculated to be 1.6 mA/μm^2. A builtin potential of 0.75 V and a junction reverse bias of 1 V were assumed. A W_C of 0.5 μm was used.

From (5) the size of ϕ_B is clearly a function of ΔE_V and J_C, as expected. Shown in Figure 3 is the parasitic barrier ϕ_B plotted as a function of the collector current density for V_{BC} = -1V. The onset of formation of the parasitic barrier ϕ_B occurs near a current density of 1.7 mA/μm^2, which is slightly larger than J_1 = 1.6 mA/μm^2. The parasitic barrier shows a sharp increase with increasing J_C, which is comparable to that described by Mazhari and Morkoc [8], but larger than that reported by Joseph et al. [6]. Seen in Figure 4 is the extent of base pushout W_{cib} calculated as a function of J_C using (3).

Since the formation of this parasitic barrier leads to excess electron buildup at the collector end of the quasi-neutral base, it produces a saturation effect in the collector current and an increase in the quasi-neutral base recombination, with a corresponding falloff in the current gain. In conjunction with this barrier formation, there is the onset of base pushout, which further degrades the current gain. The latter also degrades the base transit time and the cutoff frequency so that delay of the phenomena to higher current densities is desirable. Increasing the collector junction reverse bias and the collector doping help in this regard.

IV. CONCLUSIONS

In summary, we have developed an improved description of the physics associated with the dynamic formation of the parasitic barrier at the base-collector junction at high collector current densities. The model will provide a useful tool for device engineers in the design of the base-collector junction for optimizing the device's performance at high current densities near the onset of base pushout.

ACKNOWLEDGEMENTS

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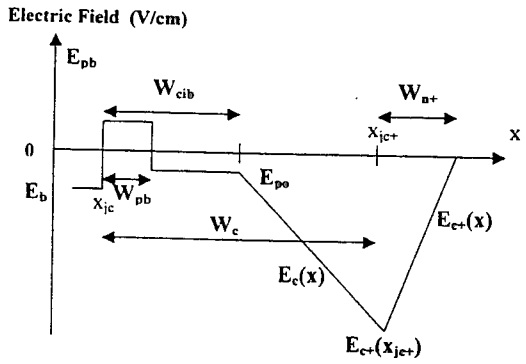


Figure 1 Electric field profile at B-C junction during parasitic barrier formation and base pushout.

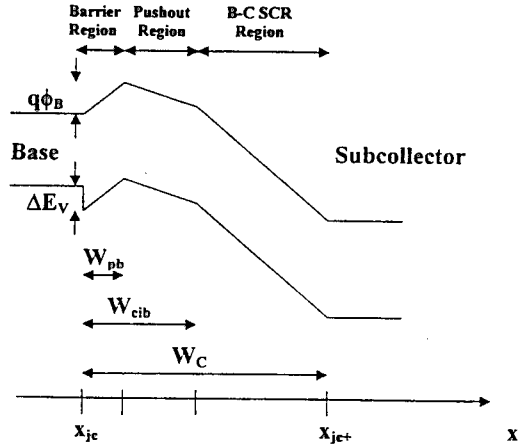


Figure 2 Energy band profile at B-C junction during parasitic barrier formation and base pushout.

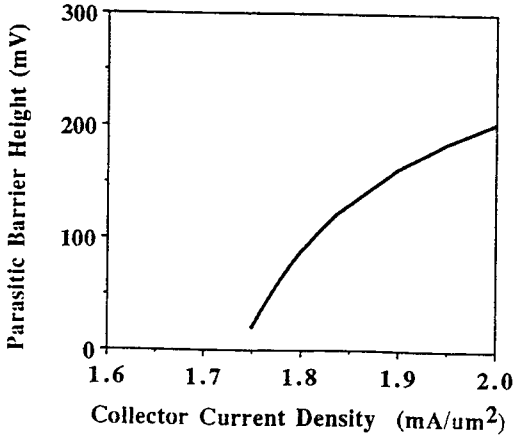


Figure 3 Parasitic barrier height ϕ_B as a function of the collector current density.

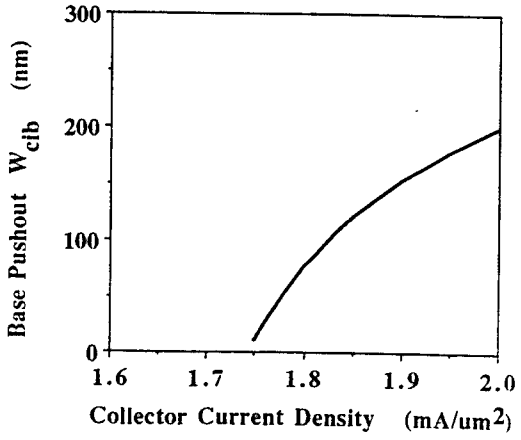


Figure 4 Base pushout W_{cib} as a function of the collector current density.

SIMULATION OF DISLOCATIONS FORMATION IN A PROFILED SILICON BY GAUGE FIELD THEORY

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Changes in temperature processes in different plastic flow regions influence upon structure formation of a growing crystal. Because of different conditions the growing structure is not homogeneous and that is why it's deformity has rotational and translation components which are described by gauge field theory. As it is known, there are different gauge field theory versions suggested by different authors [1-5]. In this work we deal with the thermal tension relaxations caused by the dislocations and polysynthetical twins structure in the silicon ribbons growth by EFG - method.

Thermal tensions in isotropic assumption for ribbon shaped non-dislocation crystal without polysynthetic twins are calculated in [6]. Thermal tensions maximum value is reached at the ribbon edges. Average tangent thermal tensions in polysynthetical twin's region don't reach critical values τ_c that cause dislocation formation if twin border distance in Si ribbon is no greater than $W_0 \sim 0{,}12$ cm [7]. Let's analyze the dislocations formation if twin border distance in Si ribbon is greater than W_0. In case of stationary growth regime and insignificant deformations the thermal tension equation of elastic continuum with defects was suggested in [4, 5]:

$$S_{bkpt}\Delta\sigma^{pt} + S^{i}_{ipt}(\nabla_b\nabla_k - \frac{1}{2}g_{bk}\Delta)\sigma^{pt} - S^{i}_{kpt}\nabla_i\nabla_b\sigma^{pt} - S^{i}_{bpt}\nabla_i\nabla_k\sigma^{pt} +$$
$$+\frac{1}{2}g_{bk}S^{rj}{}_{pt}\nabla_r\nabla_j\sigma^{pt} + \nabla_b\nabla_k\alpha T - \frac{1}{2s_2}(\sigma_{bk} - \frac{1}{2}g_{bk}\sigma^{i}{}_{i} - \frac{1}{2}g^{i(l)}\cdot \qquad (1)$$
$$\cdot(\nabla_b Z_{ki(l)} + \nabla_k Z_{bi(l)})) = 0,$$

where S_{bkpt} – crystal compliance coefficients, σ^{ij} – stress tensor components, Δ – Laplacian, ∇_i – operator that denotes the covariant derivative, $\alpha = 4{,}15\cdot10^{-6}$ K^{-1} – heat expansion coefficient, T – temperature, $g^{i(l)} = g^{il}$ – spatial components of metric tensor R_4, $Z_{ki(j)}$ are defined by structural defects. Equation (1) transforms into useal thermal tension equation under condition $s_2 \to \infty$. Stress tensor components satisfy equilibrium equation $\nabla_i\sigma^{ij}=0$.

We assume that ribbon crystallographic surface orientation is (110), direction of growth – $[1\,\bar{1}\,2]$ and is opposite to the temperature gradient. Twin borders Σ_3 have orientation $(\bar{1}\,1\,1)$ and are W_1 apart. Local coordinate system orientation in R_4 - space is $\vec{e}_1 = \frac{1}{\sqrt{2}}[110]$, $\vec{e}_2 = \frac{1}{\sqrt{3}}[\bar{1}\,1\,1]$, $\vec{e}_3 = \frac{1}{\sqrt{6}}[1\,\bar{1}\,2]$. The following boundary conditions are true for σ^{ij} [7]: on the ribbon surface $\sigma^{i1}=0$, on the cold edge $\sigma^{i3}(z\to\infty)\to0$, on the borders Σ_3 $\sigma^{23}=\sigma^{12}=\sigma^{13}=\sigma^{22}=0$.

The approximate solution of equation (1) for thin plane ribbon is:

$$\sigma^{33} \approx \frac{\hat{E}\alpha}{2}\frac{d^2T}{dz^2}\left(\frac{2}{\lambda^2} - \frac{W_1}{\lambda}\frac{ch\{\lambda y\}}{sh\{\lambda W_1/2\}}\right), \quad |y| \le W_1, \qquad (2)$$

$$\sigma^{23} = -\int_{-W_l/2}^{y} (\partial\sigma^{33}/\partial z)dy, \quad \sigma^{22} = -\int_{-W_l/2}^{y} (\partial\sigma^{23}/\partial z)dy, \tag{3}$$

$$\begin{aligned}\hat{E} = \{&S_{11} - \Delta_s[1 + 5(S_{11} - 2\Delta_s/3)(S_{11} + S_{12} - 2\Delta_s/3)^{-1}/6] + \\ &+\Delta_s{}^2 5(S_{11} - S_{12} - 10\Delta_s/9)[(S_{11} - S_{12} - 17\Delta_s/6)(S_{11} + S_{12} - 2\Delta_s/3)^{-1} + \\ &+(S_{11} + S_{12} - 3\Delta_s/2)(S_{11} - S_{12} - 2\Delta_s/3)^{-1}][2(S_{11} - S_{12} - 11\Delta_s/6)\cdot \\ &\cdot(S_{11} + S_{12} - 2\Delta_s/3) + \Delta_s(S_{11} - S_{12} - 10\Delta_s/9)(S_{11} - S_{12} - 17\Delta_s/6)\cdot \\ &\cdot(S_{11} - S_{12} - 2\Delta_s/3)^{-1} - \Delta_s{}^2 4(S_{11} + S_{12} - 2\Delta_s/3)\cdot \\ &\cdot(S_{11} - S_{12} - 2\Delta_s/3)^{-1}/9]^{-1}/12\}^{-1},\end{aligned} \tag{4}$$

$$\begin{aligned}\hat{D} = \{&1 + \Delta_s 5(S_{11} + S_{12} - 2\Delta_s/3)^{-1}/12 + \Delta_s{}^2 5(S_{11} - S_{12} - 10\Delta_s/9)\cdot \\ &\cdot(S_{12} + 13\Delta_s/12)(S_{11} - S_{12} - 2\Delta_s/3)^{-1}(S_{11} + S_{12} - 2\Delta_s/3)^{-1}\cdot \\ &\cdot[2(S_{11} - S_{12} - 11\Delta_s/6)(S_{11} + S_{12} - 2\Delta_s/3) + \Delta_s(S_{11} - S_{12} - 10\Delta_s/9)\cdot \\ &\cdot(S_{11} - S_{12} - 17\Delta_s/6)(S_{11} - S_{12} - 2\Delta_s/3)^{-1} - \\ &-\Delta_s{}^2 4(S_{11} + S_{12} - 2\Delta_s/3)(S_{11} - S_{12} - 2\Delta_s/3)^{-1}/9]^{-1}/6\},\end{aligned} \tag{5}$$

$$\Delta_s = \tfrac{1}{2}(S_{11} - S_{12}) - S_{44}, \quad \lambda^2 = \hat{E}\hat{D}/(2s_2). \tag{6}$$

S_{11}, S_{12}, S_{44} – are tabulated matrix of compliance coefficients [8]. $\hat{E}$, $\hat{D}$ coefficients depend on the crystallographic orientation of a crystal. $\hat{E} = 2{,}52\cdot10^7$ N·cm^{-2} – value is greater than Young's modulus $\hat{E} = S_{11}^{-1} = 1{,}3\cdot10^7$ N·cm^{-2}, $\hat{D} = 1{,}17$. Let's consider homogeneous dislocation density N_d spaced along the unit vector l^i with elementary Burgers vector $b^{(k)}$. In this case the potential energy density of dislocation creation under critical thermal tension influence is

$$W_{op} = s_2 N_d{}^2 b^2/2 = \pi R_0^2 \tau_c N_d{}^2 b^2/2, \tag{7}$$

where R_0 – dislocation's range. Therefore, it can be seen that $s_2 = \pi R_0^2 \tau_c \approx 0{,}15$ N, if $\tau_c \approx 75$ N·cm^{-2}, $R_0 \approx 0{,}025$ cm [9]. Then $\lambda \approx 10^4$ cm^{-1} and $\lambda W_l >> 1$.

From expressions (2, 3) we could get the following conditions:

$$\sigma^{33} \sim d^2T/dz^2 >> \sigma^{23} \sim d^3T/dz^3 >> \sigma^{22} \sim d^4T/dz^4.$$

Using equation of gauge theory [4, 5] and stress tensor components (2), we get the dislocation density tensor. It's maximum component is proportional to d^2T/dz^2:

$$P^{01(3)} \approx \frac{\alpha}{2\hat{D}}\frac{d^2T}{dz^2}\left(2y - W_l\frac{sh\{\lambda y\}}{sh\{\lambda W_l/2\}}\right), \quad |y| \le \frac{W_l}{2}. \tag{8}$$

The surface dislocation density is $N_d = |P^{01(3)}|/b$, $b = a/\sqrt{2}$.

Thermal tensions in non-dislocation Si ribbon with polysynthetic twins is [7]

$$\sigma^{33} = \frac{1}{24}\alpha\hat{E}W_l^2\left[1 - \frac{12y^2}{W_l^2}\right]T''(z), \tag{9}$$

$$\sigma^{23} = -\frac{1}{24}\alpha\hat{E}W_l^2 y\left[1 - \frac{4y^2}{W_l^2}\right]T'''(z), \tag{10}$$

$$\sigma^{22} = -\frac{1}{384}\alpha\hat{E}W_l^4\left[1 - \frac{4y^2}{W_l^2}\right]^2 T^{IV}(z), \tag{11}$$

where $|y| \le W_l/2$. Thermal tensions (9, 10, 11) depend from the twin-blocks width W_l. Thermal tensions [6] depend from the ribbons width W.

Figures 1 – 3 display the calculated dimensionless thermal tensions and surface dislocation density for $T'' \approx 10^3$ $K^{-1}cm^{-2}$. Dimensional coefficients are given in table.

Table.

Value	Coefficient
y, W_l	W_0=0,12 cm
λ	W_0^{-1}=8,33... cm^{-1}
σ^{33}	$\sigma_0=\tau_c/0,27$=278 $N \cdot cm^{-2}$
N_d	$N_{d0}=6\sigma_0/(\hat{E}\hat{D}\,bW_0)=1,2 \cdot 10^4$ cm^{-2}

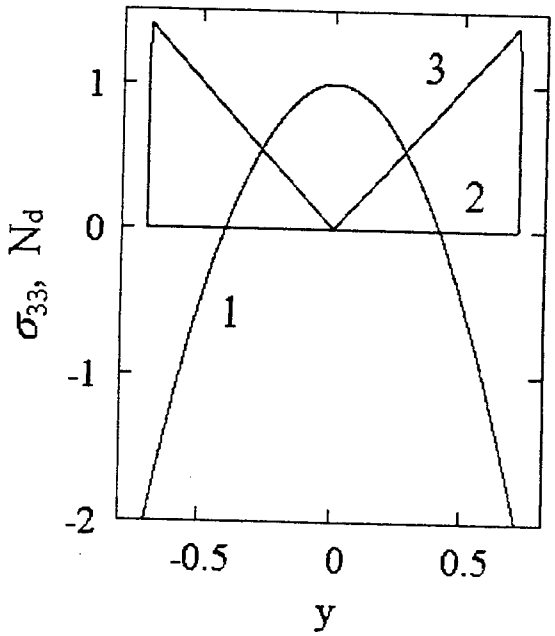


Fig. 1. Distributions of thermal tensions and surface dislocation density for $W_l=\sqrt{2}\,W_0$: 1 – σ^{33} in non-dislocation Si ribbon; 2 – σ^{33} in plastic region; 3 – N_d

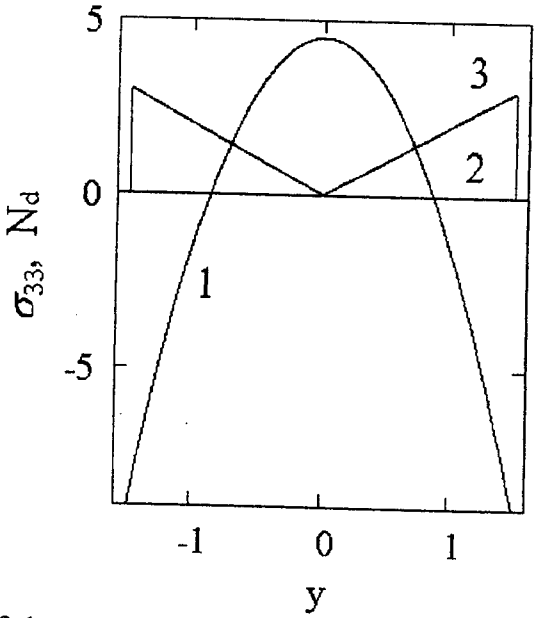


Fig. 2. Distributions of thermal tensions and surface dislocation density for $W_l=3W_0$: 1 – σ^{33} in non-dislocation Si ribbon; 2 – σ^{33} in plastic region; 3 – N_d

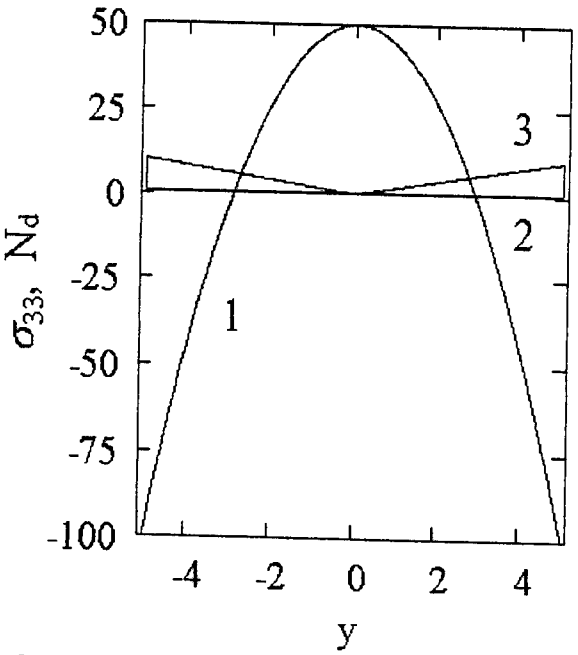


Fig. 3. Distributions of thermal tensions and surface dislocation density for $W_l=10W_0$: 1 – σ^{33} in non-dislocation Si ribbon; 2 – σ^{33} in plastic region; 3 – N_d

Thermal tensions maximum value σ^{33} in non-dislocation Si ribbon (9) is reached at the $|y|=W_l/2$. This value increases as W_l^2. However surface dislocation density maximum value $N_d|_{max}$ increases as W_l according to (8).

The dislocations formation, occuring in the plastic flow region during crystal growth, was explained by the means of gauge field theory of structural defects and thermal tensions. Dislocations develop under the thermal tensions influence in the region, where tangent thermal tensions τ exceed the critical value τ_c. The thermal tensions loosen in the plastic flow region because of dislocations formation. Thermal tensions loosen in the plastic flow region also because of twinning . Those two effects form regions containing dislocations in the neighborhood of twinning borders in silicon.

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SIMPLIFIED VERSION OF SYMMETRIC SURFACE-POTENTIAL-BASED MODEL

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As the power supply voltage approaches 1V, the moderate inversion region becomes fractionally larger fraction of the total voltage swing. Hence, the state of the art regional models, relying on a curve fitting over this region, are poorly suited for simulations of the low-V_{dd} circuits. A more physical approach can be based on short-channel adaptations of a charge-sheet model [1], but it suffers from the computional inefficiency, which is further exacerbated by the source-drain symmetry requirements.

Linearization of the inversion charge as a function of the surface potential ϕ_s is a common feature of both regional and short-channel charge-sheet MOSFET models. When the source is chosen as a reference point this leads to violation of the Gummel symmetry test and unphysical behavior of the transcapacitances for $V_{ds} = 0$ [2, 3]. This problem can be alleviated by linearization near the "midpoint" where the surface potential ϕ_m is an average of the source, ϕ_{ss}, and drain, ϕ_{sd}, surface potentials [3]. This, however, adds a third iterative procedure and further reduces the computational efficiency of the model. Here we present an outline of a symmetric surface-potential-based model which is free from this problem. This is essentially a symmetrized version of the model described in [4, 5].

In a usual manner, the drain current [2] with velocity-saturation

$$I_d = \beta (1+\phi / V_C)^{-1} C_{ox}^{-1} \left[\int_{\phi_{ss}}^{\phi_{sd}} Q_i d\phi_s + V_t (Q_{is} - Q_{id}) \right] \qquad (1)$$

where $\beta = \mu(W / L)\, C_{ox}$, $\phi = \phi_{sd} - \phi_{ss}$, Q_i is the inversion charge, Q_{is} and Q_{id} are its values at the source and drain respectively, $V_t = kT / q$, and velocity saturation parameter V_c includes the Grotjohh-Hofflinger factor [6]. This not only improves the quality of the I-V fit, but also removes the singularity at $V_{ds} = 0$ which is brought about by the conventional velocity-field model.

Midpoint linearization of the bulk charge yields

$$Q_i / C_{ox} = V_m - \alpha(\phi_s - \phi_m) \qquad (2)$$

where $V_m = (Q_i / C_{ox})\,|_{\phi_s = \phi_m}$ and α is obtained using Gummel linearization [2]. For the diffusion current, which is appreciable in subthreshold where ϕ is small, it is more appropriate to use first-order Taylor expansion. This yields $Q_{is} - Q_{id} \approx C_{ox}\, \alpha_m\, \phi$ and

$$I_d = \beta(1+\phi/V_c)(V_m + V_t\alpha_m)\phi \tag{3}$$

where

$$\alpha_m = 1 + 0.5\gamma f\,(f\phi_m - V_t)^{-1/2} \tag{4}$$

To escape the problem of negative drain conductance [3], we define ϕ_o by condition $(\partial I_d / \partial\phi)_{\phi=\phi_o} = 0$ and change ϕ into a suitably chosen "smoothing function" $\phi_x(\phi)$ with the unit slope at $\phi = 0$ and the property $\lim_{\phi\to\infty} \phi_x = \phi_o$. The equation for ϕ_o

$$\phi_o^2 + V_c\phi_O - (2/\alpha_m)V_m(\phi_O)V_C = 0 \tag{5}$$

cannot be solved in a closed form. This necessitates an iterative solution (in addition to that required to find the surface potential) and is detrimental to the model's computational efficiency. However, linearization $(V_1 = Q_{is}/C_{ox})$

$$V_m = V_1 - \alpha_m\phi_O/2 \tag{6}$$

which is slightly different from (2) leads to a simplified closed-form solution

$$\phi_O = (2V_1/\alpha_m)\left(1+\sqrt{1+2V_1/\alpha_m V_c}\right)^{-1} \tag{7}$$

As shown in Fig. 1, eq. (7) is quite accurate with the worst case error of about 4%. As far as the terminal device characteristics are concerned, the accuracy is even better (cf. Fig. 2). It is also important that as shown in Fig. 3, approximation (7) does not violate the Gummel symmetry test.

In conclusion, symmetrization of the short-channel surface-potential based model can be accomplished without increasing the model complexity or reducing its computational efficiency.

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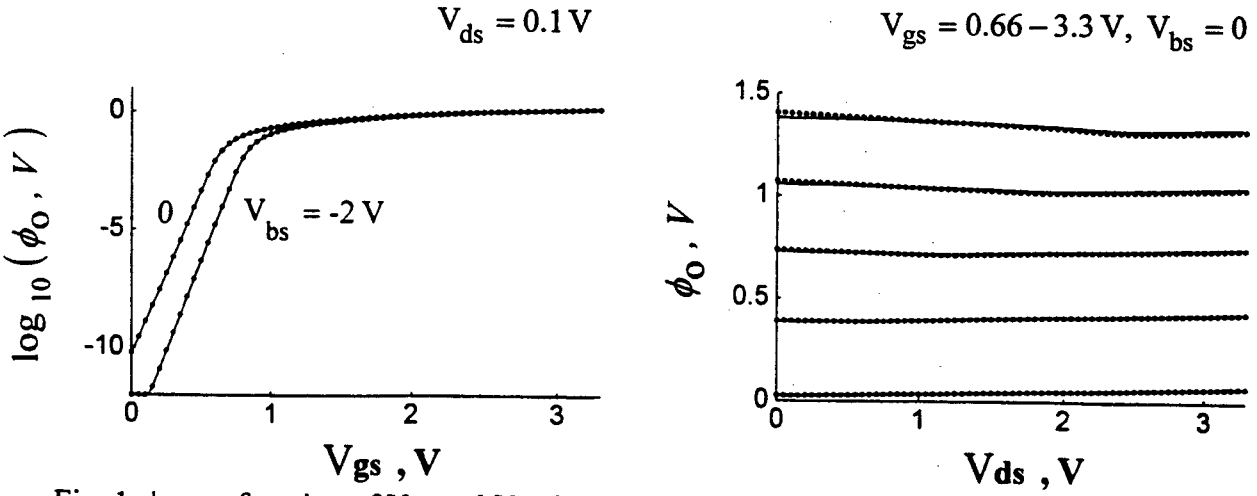


Fig. 1 ϕ_o as a function of V_{gs} and V_{ds} for a 0.6/0.25 μ MOSFET ;
Solid lines — eq (7), circles — iterative solution of eq.(5)

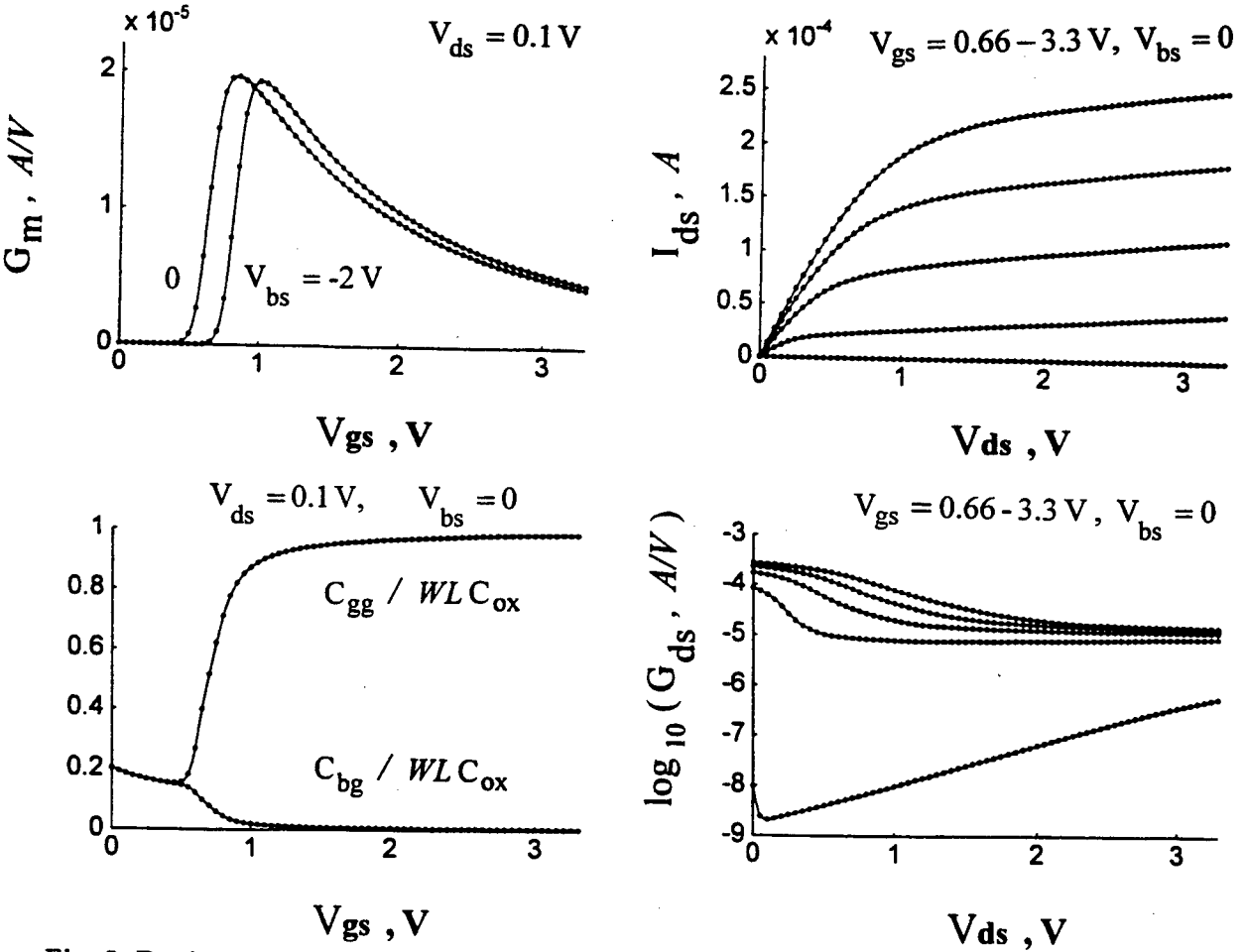


Fig. 2 Device characteristics computed using analytical approximation (7) — solid lines, and exact solution of eq. (5) — circles.

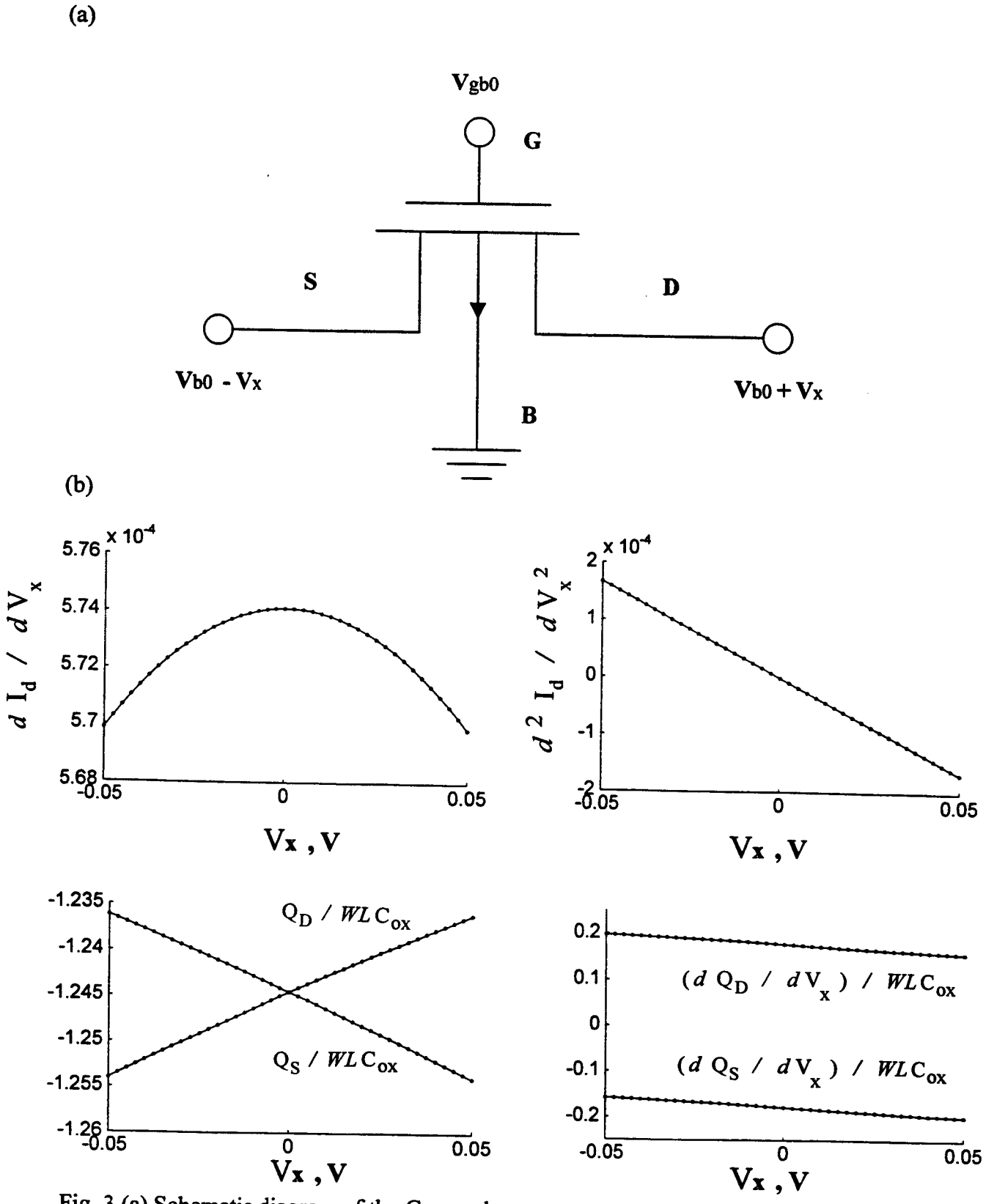


Fig. 3 (a) Schematic diagram of the Gummel symmetry test.
(b) Results of the Gummel symmetry test, V_{gb0}=3.3 V, Vbs = 0 V;
Solid lines — eq (7), circles — iterative solution of eq.(5)

A Circuit Simulation Model for Silicon-on-Insulator LDMOS Transistors, with Accurate High Side Behaviour

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Abstract

LDMOS transistors fabricated on SOI have significant advantages over their bulk equivalents, but when used in "High Side" power switching applications, special effects arise from high voltages appearing across the back oxide interface. This can lead to increasing on-resistance and changes in charge distribution. In this paper we present a practical circuit simulation model which can be easily implemented in most design flows. Several more conventional models are combined and modified to provide accurate prediction of behaviour, even with inversion along the back oxide. Parameter extraction is also shown to be feasible and measurements are shown to agree well with the model.

1. Introduction

SOI fabrication technology is attractive for smart power applications because of its intrinsic device isolation, allowing more flexible circuit topologies, and more significantly, because of greater packing density. Further, in high side applications, where an N channel device is used to pull up the voltage across the load, there is a significantly lower on-resistance[1,2]. This is illustrated in figure 1.

To take advantage of these benefits designers must be able to predict the behaviour of these devices at the circuit simulation stage. It is to meet the needs of the design community that this work has been addressed. Whilst the modelling of bulk LDMOS devices [3,4,5,6] has received much attention to date, there has been little attention to the particular problems of SOI devices. Unlike the existing bulk LDMOS subcircuit models, which use JFETs to model the drift region resistance [3,6], we are going to use a new depletion type SOI MOSFET.

2. The DC model

The model is constructed from the basis of several more established compact models, as shown in figure 2.

The MOSFET behaviour of the P-body under the gate is described by an established MOS model, in this case Philips' MM9 [7]. This advanced model handles channel length modulation, DIBL, impact ionisation and floating body effects.

When the transistor is on and the drain voltage is lower than the gate voltage, an accumulation layer is created in the drift region along the surface of the front oxide. The current flows from the MOSFET channel into the accumulation layer and then to the drain. However, when the drain voltage becomes higher than that of the gate, a depletion layer is created in the drift region at the top oxide interface. Hence, when the current leaves the small remaining accumulation layer still left near the p-n junction, it flows almost vertically . At a certain point this depletion layer touches the depletion layer of the p-n junction and the channel pinches, causing velocity saturation of the drift region [8]. This behaviour is modelled by a depletion bulk MOSFET model [9], and is illustrated

in figure 3. In the SOI-LDMOS the p-n junction is turned over 90 degrees compared to a normal depletion type MOSFET; hence some of the parameters must be calculated in a somewhat different way, taking this almost vertical current flow into account.

The second part of the drift region is represented by an SOI depletion MOSFET which has a front gate and a back gate instead of a substrate. Just as for the bulk depletion MOSFET, the model includes pinch-off mode and velocity saturation in the channel. The equations for depletion and accumulation at the surface and at the buried oxide are exactly the same as the ones used for the surface in the bulk depletion MOSFET, and don't include inversion. To stop the depletion layer growing any further when the surface along the buried oxide goes into inversion, we limit the substrate voltage to V_{SUB_l} given by

$$V_{SUB_l} = -V_{T0box} - k_{0box}\,(\sqrt{V_{DB} + \phi_B} - \sqrt{\phi_B})$$

This voltage is the drain dependent threshold voltage for the back gate. Note that the drain plays the role normally taken by the body in a normal MOSFET. V_{T0box} is the threshold voltage for inversion at the buried oxide at zero drain bias, k_{0box} is the body factor of the drain N^- body region at the back oxide and ϕ_B the surface potential again at the back oxide interface.

3. Self-Heating

Even more than in smaller geometry SOI devices, self-heating has a significant impact. This is due to the much higher thermal resistance of the buried oxide compared with that of normal silicon. To simplify the model, the device is assumed to have a uniform temperature distribution. Heat flow and temperature rise are modelled with a thermal "sub-circuit" [10] with a resistance term to represent the path of the heat to the substrate; to account for the dynamic as well as static effects a capacitor is used to represent the heat storage [11].

4. The charge modelling

MM9 describes the charge modelling for the MOSFET part of the LDMOS, with the difference that the gate-drain overlap capacitance has to be made zero, because it is included in the depletion type MOSFETs and varies with the drain and gate biases. The body to drain capacitance is included in the second depletion type MOSFET, and hence must also be made zero in the body-drain diode model.

Because inversion is not included in the depletion type MOSFET section of the model, an extra voltage dependent capacitance has been added to describe the additional substrate to body capacitance that is created when a hole layer is present in the drift region along the surface of the buried oxide. This additional capacitance can be described by the following equation :

$$Q(B,SUB) = C_{bo}\,W_{bbo}\,L_{bbo}\,V_{BSUB} +$$

$$C_{bo}\,W_{dbo}\,L_{dbo}\,\phi_T\,ln(1 + exp(\frac{V_{BSUB} + V_{SUB_l}}{\phi_T}))$$

with C_{bo} the back gate capacitance per unit area, W_{bbo} and L_{bbo} respectively the width and length of P-body at the buried oxide and W_{dbo} and L_{dbo} respectively the width and length of the N^- region at the buried oxide. The second part of the equation goes smoothly to zero when $V_{BSUB} \geq V_{SUB_l}$, i.e. when there is no longer any inversion layer.

5. Extraction strategy and verification of the model

No model is useful unless there is some way of obtaining a set of parameters from measured wafers. Here, a parameter optimisation strategy has been developed which divides the parameter set into groups. Separate optimisations are then performed starting from the

appropriate measured data. The parameters for the MOSFET (MM9) can be extracted in a similar way as for an ordinary NMOS [7] with the following differences: to obtain the threshold voltage and the gain factor β it is necessary to limit the linear characteristic to a couple of volts above the threshold voltage, this is before the drift region starts to play an important role. The output characteristics for the MM9 extraction procedure need to be measured only for low gate voltages, so that the main part of the applied drain voltage drops over the MOSFET channel.

To extract the depletion MOSFET parameters we added the measurement set-ups from the table below

Set-up	**M1**	**M2**
I_D-V_{GS}, V_{DS}=0.1V, V_{BS}=0,-1,-2V, high V_{GS}	R_{on}	-
I_D-V_{GS},high V_{GS}, V_{DS}=$V_{Gmax}/2$,V_{Gmax}	V_P,V_{Dsat}	V_{Dsat}
I_{DS}-V_{DS}, low V_{DS}, V_{GS}=V_{Gmax}-3V,..,V_{Gmax}	-	R_{on}

where M1 and M2 stand for respectively the bulk depletion MOSFET and the SOI depletion MOSFET. V_P is the pinch-off voltage for zero bias at gate and substrate, R_{on} the ohmic resistance at zero bias and V_{Dsat} the critical drain-source voltage for velocity saturation. The ideas behind the set-up choices are that for high V_{GS} and medium V_{DS}, the MOSFET channel has a very low resistance and isn't pinched. Therefore the current saturation behaviour originates in the drift region.

Clearly one must start with a realistic initial set of parameters in order that the optimisation converges to a sensible physical solution. The results are shown in figure 4 and 5, for the linear and output characteristic. The $I_D(V_G)$ plot is shown for different body biases (V_B). We notice the negative output conductance for high drain current and bias, due to self-heating. Figure 6 shows measured and simulated curves when the device is working under high side conditions: the current decreases as we make the handle wafer more negative, but once inversion is established the current stays constant.

6. Conclusions

A new comprehensive subcircuit model for the SOI LDMOS has been proposed. The model is based on a detailed study of the device physics and accounts for the unique high side behaviour of the SOI devices. An extraction strategy for the parameters is explained. Simulations and measured data support the accuracy of the model.

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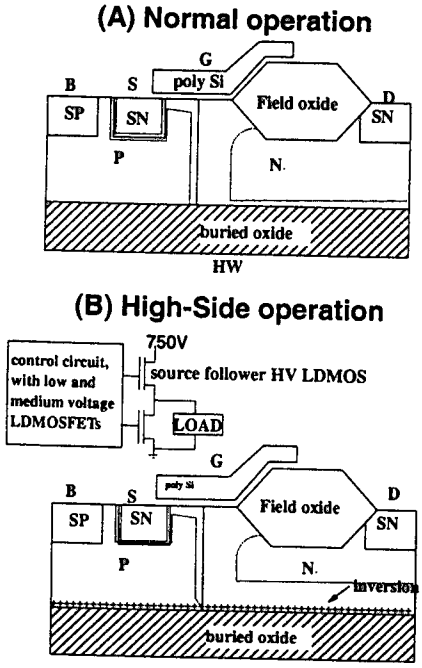


Figure 1: The depletion layers of an LDMOS working respectively in normal (a) and high side operation (b). Inset shows a typical half-bridge configuration, where some devices work under high side conditions.

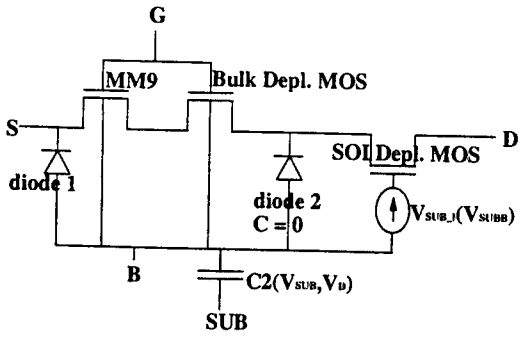


Figure 2: The subcircuit model for the LDMOS

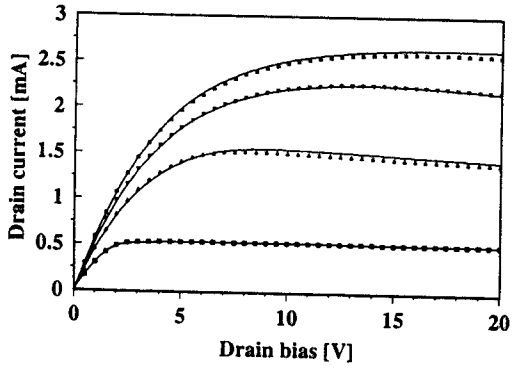


Figure 5: $I_D(V_D)$ [mA] for V_B=0V and V_G=5, 8, 11, 14V (markers: measured, full line: simulated) .

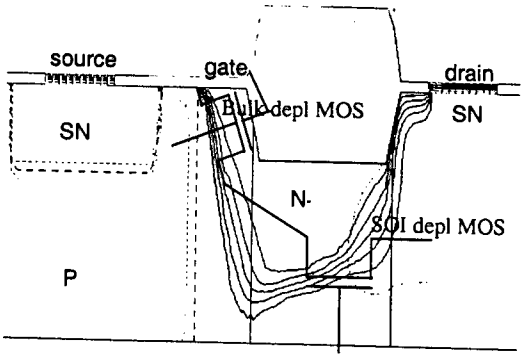


Figure 3: Current flow lines in the drift region and depletion layers to illustrate the use of the bulk and SOI depletion MOSFET

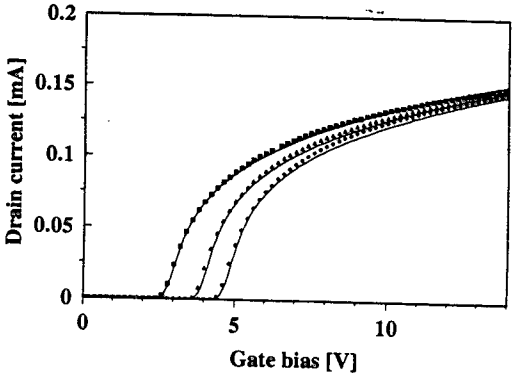


Figure 4: $I_D(V_G)$ [mA] for V_B=0, -1, -2V and V_D=0.25V (markers: measured, full line: simulated) .

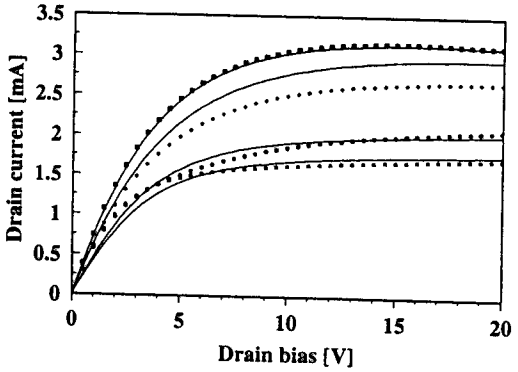


Figure 6: $I_D(V_D)$ [mA] for V_G=10V and V_{SUB}=0,-50,-100,-200V (markers: measured, full line: simulated) .

POLYSILICON DEPLETION EFFECT WITHIN A CONTEXT OF A SURFACE-POTENTIAL-BASED COMPACT MOSFET MODEL

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The reduction of the gate oxide thickness in scaled MOSFET's accentuates the polysilicon depletion effect responsible for the degradation of the transistors current driving capability. Hence it is desirable to incorporate the polysilicon depletion into the compact MOSFET models. A widely used modeling approach was developed within a context of the regional models and is based on the standard assumption that the active region surface potential ϕ_s is pinned at the $2\phi_f + V_{sb}$ level (V_{sb} denotes the back bias) [1,2]. This allows one to express the polysilicon surface potential ϕ_p as a function of the gate voltage V_{gs} and to develop suitable expressions for the "effective gate voltage" [3], or for the threshold voltage increment [1].

As the power supply voltage level continues to decrease, regional models are expected to become inadequate in view of their unphysical nature in a transitional region between the moderate and strong inversion regimes. This explains current interest in more accurate short-channel surface-potential-based models [4-6] which, however, were developed without taking into account the polysilicon depletion layer. Incorporation of the polysilicon depletion effect in these models presents certain difficulties. The original work [1,2] cannot be used directly, since it assumes $\phi_s = 2\phi_f + V_{sb}$, while the main feature of the surface-potential-based models is a faithful reproduction of the surface potential variation as a function of the gate voltage. Furthermore, this assumption leads to unphysical $\phi_p(V_{gs})$ dependence for low V_{gs} (Fig. 1). In a regional model this is not a problem since the polysilicon depletion factor can be excluded from the subthreshold region which is described separately from the rest of the model. But physically based charge-sheet models require a single expression for ϕ_p which is valid for all bias conditions and describes a gradual reduction of ϕ_p in subthreshold region. A brute-force approach – to modify the numerical procedure for the surface potential calculation – complicates the model and reduces its computational efficiency. Here, we present an analytical solution of the problem.

The surface potential ϕ_s at the source end of the channel is a solution of the equation

$$\left(w-\phi_s-\phi_p\right)^2=\gamma^2\left(f\phi_s-V_t+V_t\Delta\right) \tag{1}$$

where $w = V_{gs} + V_{sb} - V_{fb}$, V_{sb} denotes the back bias, V_{fb} is the flat-band voltage, γ is the body factor, f is a lateral gradient factor [4], V_t is the thermal voltage, and

$$\Delta = exp\left[\left(\phi_s-2\phi_f-V_{sb}\right)/V_t\right] \tag{2}$$

Neglecting the minority carriers effects in the heavily doped polysilicon gate yields ϕ_p as a function of gate drive and surface potential ϕ_s

$$\phi_p = k_p v^2 \left(1+\sqrt{1+k_p v}\right)^{-2} \tag{3}$$

where $k_p = C_{ox}^2/q\varepsilon_{Si}N_p$, C_{ox} denotes the oxide capacitance per unit area, and N_p is the polysilicon doping level, and $v = w - \phi_s$. As shown in Fig. 1, setting $\phi_s = 2\phi_f + V_{sb}$ produces unphysical behavior ($\partial\phi_p / \partial V_{gs} < 0$) in the weak inversion region. To alleviate this problem we incorporate (3) within a context of the surface-potential-based model. An equation similar to (1)

$$\left[w-\phi_s^{(0)}\right]^2 = \gamma^2\left[f^{(0)}\phi_s^{(0)} - V_t + V_t\Delta^{(0)}\right] \tag{4}$$

is valid for the surface potential $\phi_S^{(0)}$ in the absence of the polysilicon depletion effect. Here, $f^{(0)}$, $\Delta^{(0)}$ are the values of f and Δ for $\phi_p = 0$. The difference $\Delta\phi_s = \phi_s - \phi_s^{(0)}$ satisfies equation which follows from (1) and (4):

$$\begin{aligned}&\left[1-\gamma^2(\partial f/\partial\phi_s)\right](\Delta\phi_s)^2 + 2\Delta\phi_s\left\{\phi_p - w + \phi_s^{(0)} - 0.5\gamma^2\left[f^{(0)} + \phi_s^{(0)}(\partial f/\partial\phi_s)\right]\right\}\\ &+\phi_p\left[\phi_p - 2\left(w-\phi_s^{(0)}\right)\right] + \gamma^2 V_t\Delta^{(0)}\left[1-\exp(\Delta\phi_s/V_t)\right] = 0\end{aligned} \tag{5}$$

To obtain this result we noted that the lateral gradient is an almost linear function of ϕ_s, so the linearization $f = f^{(0)} + \Delta\phi_s(\partial f/\partial\phi_s)$ is appropriate. The advantage of eq. (5) is that it has an accurate approximate solution. Indeed, since typically $|\Delta\phi_s| < V_t$, one can use second order Taylor expansion for the exponent in (5). This yields quadratic equation with a solution

$$\Delta\phi_s = 2q\left(p+\sqrt{p^2-4uq}\right)^{-1} \tag{6}$$

where

$$q = 2\phi_p\left[\phi_p - 2\left(w-\phi_s^{(0)}\right)\right] \tag{7}$$

$$p = 2(w-\phi_p-\phi_s^{(0)}) + \gamma^2\left[f^{(0)} + \phi_s^{(0)}(\partial f/\partial\phi_s) + \Delta^{(0)}\right] \tag{8}$$

and

$$u = 1-\gamma^2\left(\partial f/\partial\phi_s + \Delta^{(0)}/2V_t\right) \tag{9}$$

The accuracy of (6) can be improved by linearization in terms of q. In this way, we obtain

$$\Delta\phi_s = q(2p - uq/p)^{-1} \tag{10}$$

The accuracy of the last result is better than 5% for all numerical values of process parameters (oxide thickness, impurity concentration, polysilicon doping level) of interest to CMOS circuit design (see Fig. 2). Furthermore, (10) provides an accurate approximation not only for $\phi_s = \phi_s^{(0)} + \Delta\phi_s$ but also for derivative $\partial\phi_s/\partial V_{gs}$ which enters the computations of transconductances and transcapacitances (see Fig. 3 and Fig. 4).

One of the problems associated with the surface-potential-based models is the computational inefficiency of the iterative computations of the surface potential at the source and drain ends of the channel. This problem was partially alleviated in [6]. Incorporation of the polysilicon depletion effect in a form presented here is compatible with the computational procedure developed in [6]. The resulting surface potential model provides a good global fit to experimental data. Some results are shown in Fig. 5.

In conclusion, we have developed an analytical approximation for the effect of polysilicon depletion layer on the surface potential in MOS inversion channel. The new approximation is accurate within a few percent and can be incorporated within a surface-potential-based compact MOSFET model with a minimal modification of the model structure.

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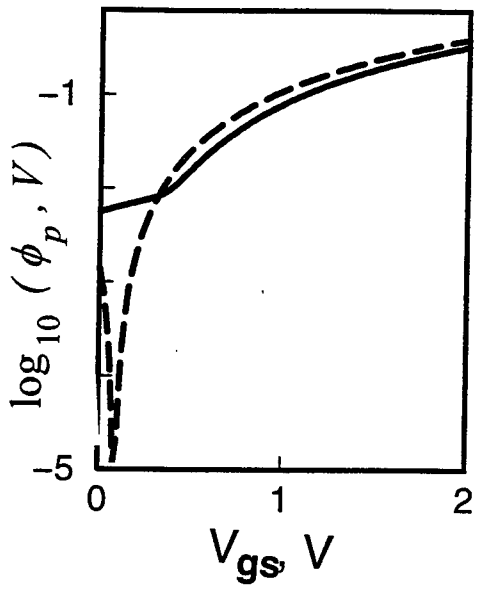


Fig. 1 Comparison of exact $\phi_p(V_{gs})$ dependence (solid line) with that obtained by setting $\phi_s = 2\phi_f + V_{sb}$ (broken line); $t_{ox} = 2$ nm, $N_{sub} = 5 \cdot 10^{17} cm^{-3}$, $V_{fb} = -0.784$ V, $V_{sb} = 0$ V, and $N_p = 5 \cdot 10^{19}$ cm^{-3}.

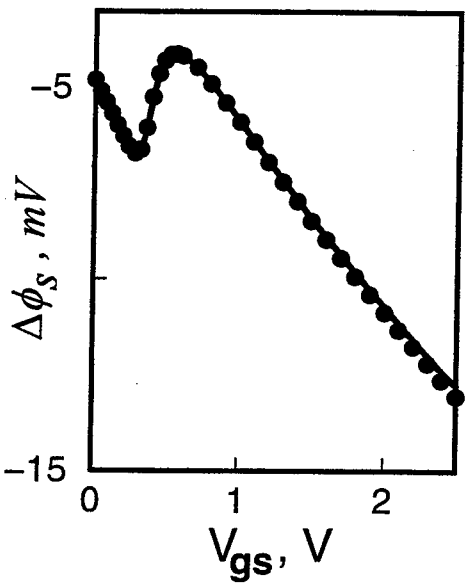


Fig. 2 Active region surface potential reduction by the formation of the polysilicon depletion region, $N_p = 5 \cdot 10^{19}$ cm^{-3}. $t_{ox} = 2$ nm, $N_{sub} = 5 \cdot 10^{17}$ cm^{-3}, $V_{sb} = 0$V. • • • • exact solution of *eq.* (1) —— analytical approximation (10)

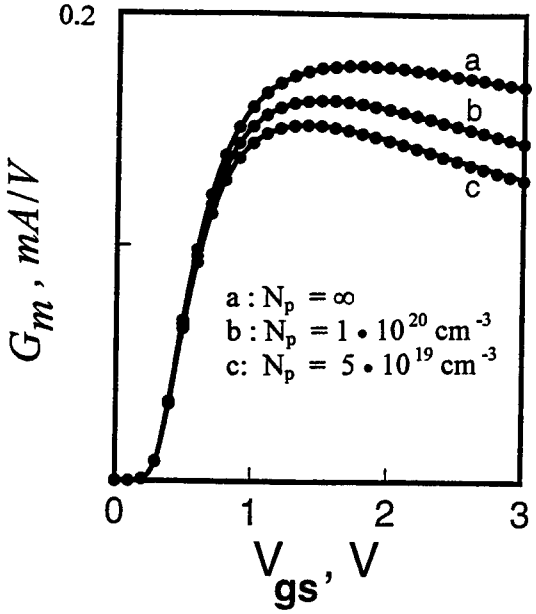


Fig. 3 Effect of polysilicon depletion region on the drain transconductance G_m;
t_{ox}= 3 nm, N_{sub}= $2 \cdot 10^{17}$ cm^{-3}
• • • • exact solution of *eq.* (1)
—— analytical approximation (10)

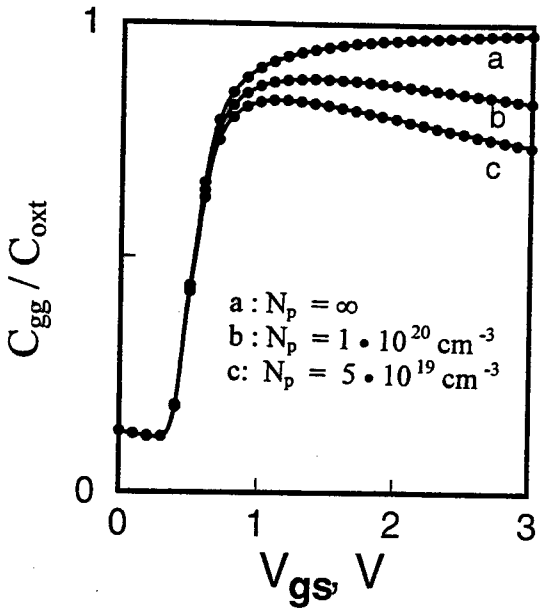


Fig. 4 Effect of polysilicon depletion region on the normalized gate capacitance,
$C_{oxt} = C_{ox} W L$, t_{ox} = 3 nm,
$N_{sub} = 2 \cdot 10^{17}$ cm^{-3}.
• • • • exact solution of *eq.* (1)
—— analytical approximation (10)

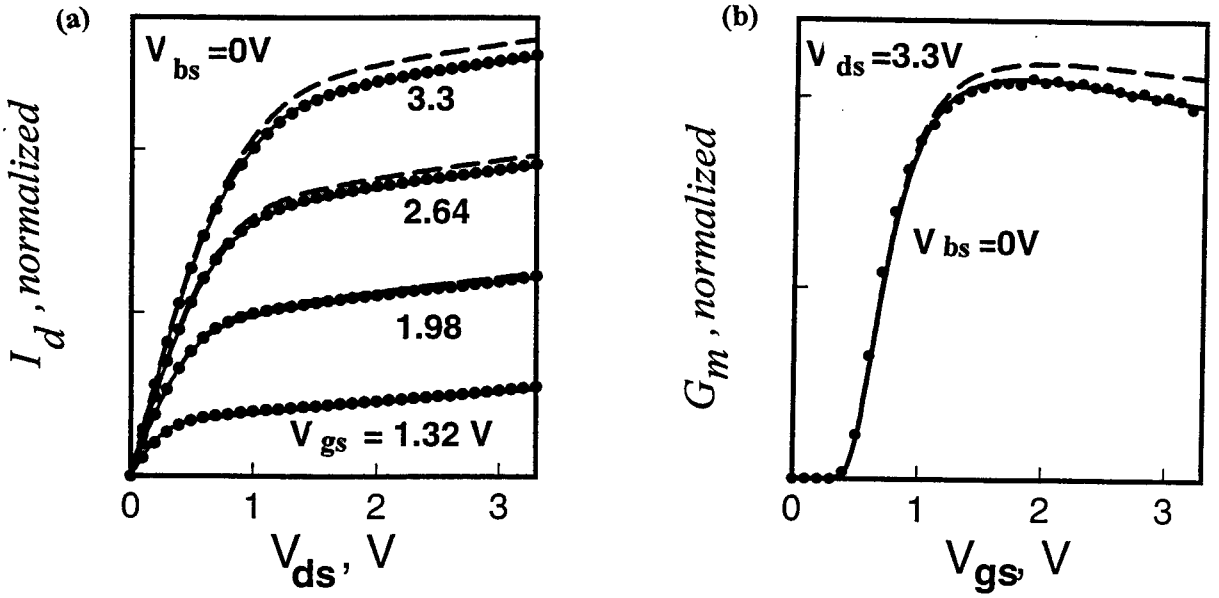


Fig. 5 I-V (a) and Gm (b) characteristics of 0.6/0.25 μ MOSFET, .
(• • • •) experimental data
(——) model based on *eq.* (10) with $N_p = 6 \cdot 10^{19}$ cm^{-3}
(- - - -) model without polysilicon depletion.
t_{ox} = 6.38 nm, $N_{sub} = 8.4 \cdot 10^{16}$ cm^{-3}

The Spherical Harmonics Wigner Equation for Quantum Transport in Semiconductor Devices

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1. Introduction

As device dimensions steadily decrease, simulation has become an integral component of the design and analysis process. Now that the critical dimensions in many semiconductor devices are on the nanometer scale, quantum effects are becoming increasingly noticeable. Researchers are introducing various methods to account for quantum effects in device simulation. These methods range from including quantum corrections to the moment equations used for modeling semiconductor devices to the solution of the Wigner-type equation[1-5]. These various approaches have their respective strengths. For example, the moment approaches can give quantum corrections to macroscopic quantities such as carrier concentration. However, they suffer from many of the same approximations as their semiclassical analogues. Furthermore, they do not provide a quantum distribution function. On the other hand, methods that employ the Wigner formalism can provide the quantum distribution function, but they usually rely on simplified phenomenological scattering terms to make their equations tractable for numerical solution. In general, the various approaches share a common challenge which is that inclusion of quantum effects in device simulation usually makes the modeling effort considerably more complicated.

In this paper, we introduce a new method for incorporating quantum effects in device modeling using the Wigner formalism. We start with the Wigner transport equation. To the Wigner equation we then add a semiclassical collision integral identical to the one used in the Boltzmann transport equation. This allows for the incorporation of elastic and inelastic scattering, including optical, acoustic phonon and ionized impurity scattering, which is critical to determining electron transport in semiconductors. This gives rise to a seven-dimensional high order integral-differential equation which is virtually impossible to solve directly. To help solve the equation we express the Wigner function as a spherical harmonic expansion. This reduces the dimensionality of the Wigner transport equation and allows for analytical evaluation of the collision integrals. As a result, the Wigner transport equation is reduced to a differential-difference equation that is tractable using numerical methods. We apply our method to solving the Wigner transport equation to a BJT. The results give the quantum corrected carrier density, current, as well as the quantum distribution function for the entire device. Since the Wigner transport equation reduces to the Boltzmann equation for slowly varying potentials, we also analyze the same structure using the semiclassical Boltzmann transport equation. We find that including quantum correction has the effects of reducing carrier concentration near potential barriers, and reducing high-energy electron density in certain regions of the quantum distribution function.

2. Theory and Realization

The Wigner function is defined as the Fourier transformation of the product of wave functions over nonlocal coordinates:

$$w(\vec{r},\vec{p},t)=\frac{1}{\pi^3}\int e^{2i\vec{r'}\cdot\vec{p}}\psi^*(\vec{r}+\vec{r'},t)\psi(\vec{r}-\vec{r'},t)d\vec{r'} \tag{1}$$

Where ψ is the wave equation which is the solution of Schrödinger equation at the point $\vec{r}-\vec{r'}$. By differentiating the Wigner function with respect to time, and employing the Schrödinger Equation, the following transport equation for the Wigner function can be derived[6]:

$$\frac{\partial w}{\partial t}+\frac{\vec{p}}{m}\cdot\nabla_{\vec{r}}w-e\sum_{n=0}^{\infty}\frac{(-1)^{2n}\hbar^{2n}}{4^n(2n+1)!}(\nabla_{\vec{p}}\cdot\nabla_{\vec{r}})^{2n+1}V(\vec{r})w=0 \tag{2}$$

It is important to keep in mind that $\nabla_{\vec{p}}$ only operates on w, and $\nabla_{\vec{r}}$ only operates on the potential $V(\vec{r})$. While the potential term should account for collisions, it is very difficult to incorporate this

explicitly. Instead, we separate the potential into a macroscopic one resulting from fields and barriers, and a microscopic one due to scattering. The time variation of w due to scattering is then given by the collision integral of the semiclassical Boltzmann equation for semiconductors. This gives rise to the following Wigner transport equation:

$$\frac{\partial w}{\partial t} + \frac{\vec{p}}{m} \cdot \nabla_{\vec{r}} w - e \sum_{n=0}^{\infty} \frac{(-1)^{2n} \hbar^{2n}}{4^n (2n+1)!} (\nabla_{\vec{p}} \cdot \nabla_{\vec{r}})^{2n+1} V(\vec{r}) w = \left(\frac{\partial w}{\partial t} \right)_{coll} \tag{3}$$

where

$$\left(\frac{\partial w}{\partial t} \right)_{coll} = \frac{1}{(2\hbar\pi)^3} \sum_j \int [w(\vec{r}, \vec{p}') S_j(\vec{p}', \vec{p}) - w(\vec{r}, \vec{p}) S_j(\vec{p}, \vec{p}')] \, d^3\vec{p}' \tag{4}$$

Where the functions $S_j(\vec{p}', \vec{p})$ refer to the matrix element for $j'th$ type of scattering obtained from Fermi's golden rule. We include optical, acoustic and ionized impurity scattering.

It is interesting to note that if we keep only the first order expansion of potential, the Wigner transport equation reduces to the Boltzmann transport equation(BTE) given by:

$$\frac{\partial w}{\partial t} + \frac{\vec{p}}{m} \cdot \nabla_{\vec{r}} w - e \nabla_{\vec{r}} V(\vec{r}) \cdot \nabla_{\vec{p}} w = \left(\frac{\partial w}{\partial t} \right)_{coll} \tag{5}$$

It can therefore be interpreted that the high order terms of the potential expansion give quantum correction to the BTE. In our work we retain the first the two terms of the potential, and the Wigner Equation becomes:

$$\frac{\partial w}{\partial t} + \frac{\vec{p}}{m} \cdot \nabla_{\vec{r}} w - e \sum_{n=0}^{1} \frac{(-1)^{2n} \hbar^{2n}}{4^n (2n+1)!} (\nabla_{\vec{p}} \cdot \nabla_{\vec{r}})^{2n+1} V(\vec{r}) w = \left(\frac{\partial w}{\partial t} \right)_{coll} \tag{6}$$

This truncation of the potential expansion is justified because higher terms contain $\hbar^{2n}$ which becomes negligible very quickly for $n > 2$.

To solve the Wigner transport equation we first employ the spherical expansion method originally used for the BTE[7,8]. The spherical harmonics expansion of the distribution function allows for analytical evaluation of the collision integral and reduction of dimensionality making the Wigner equation tractable for numerical solution.

$$w(\vec{r}, \vec{k}) = \sum_{l=0}^{\infty} \sum_{m=-l}^{l} w_l^m(\vec{r}, \varepsilon) Y_l^m(\theta_k, \phi_k) \tag{7}$$

After considerable mathematical manipulation employing the Spherical Harmonic method[7-8], we obtain the following tractable form for the Wigner transport equation.

$$\frac{v}{3\gamma} \left[\frac{\partial}{\partial x} (\gamma v \tau \frac{\partial w_0}{\partial x}) + \frac{\partial}{\partial y} (\gamma v \tau \frac{\partial w_0}{\partial y}) \right] + \left[\frac{\partial w_0}{\partial t} \right]_c + [w_0]_{QC} = 0 \tag{8}$$

where $[w_0]_{QC}$ is quantum correction which is:

$$\begin{aligned} [w_0]_{QC} = \; & -\tfrac{\alpha \tau v}{5\epsilon} (\nabla^2 \rho)(\hat{P}_1 w_0) \\ & -\tfrac{\alpha \tau v}{5\epsilon} (\hat{P}_1 + \hat{P}_0)(\nabla \rho \cdot \nabla w_0) \\ & -\tfrac{\alpha}{5\epsilon} (\nabla \rho \cdot \nabla w_0)(\hat{P}_0 \tau v) \\ & -\tfrac{q\alpha}{5\epsilon} [2\tau \hat{P} w_0 + (\hat{P}' \tau)(\hat{P}_1 w_0) + (\hat{P}_0 \tau)(\hat{P}'' w_0)] \end{aligned} \tag{9}$$

where $\alpha = 1/24$ and the 5 momentum operators are:

$$\hat{P}_0 = \frac{\partial^3}{\partial p^3} + \frac{2}{p} \frac{\partial^2}{\partial p^2} - \frac{2}{p^2} \frac{\partial}{\partial p} \tag{10}$$

$$\hat{P}_1 = \frac{\partial^3}{\partial p^3} + \frac{4}{p} \frac{\partial^2}{\partial p^2} \tag{11}$$

$$\hat{P}' = \frac{\partial}{\partial p} + \frac{2}{p} \tag{12}$$

$$\hat{P}'' = \frac{\partial}{\partial p} \tag{13}$$

$$\hat{P} = \frac{\partial^4}{\partial p^4} + \frac{4}{p}\frac{\partial^3}{\partial p^3} \tag{14}$$

3. Results and Conclusions

We have applied our method of investigating quantum transport to a NPN bipolar junction transistor (BJT). The doping structure of the BJT, which has a 50nm p-type base, is shown in Fig. 1. The emitter is at the left, base in center, and collector at right. Fig. 2 is the electrostatic potential inside the device with the applied bias $V_{BE} = 1.1V$ and $V_{CB} = 1.0V$. The potential was determined by self-consistent solution of the Poisson equation. It can be seen that the forward bias lowers the emitter-base barrier height, which has its maximum magnitude at $70nm$ into the device. It will be seen below that quantum mechanics influences the effects of this emitter-base barrier. Fig 3 is the quantum electron distribution function calculated by solution to the Wigner Equation along the device on a log scale. We see that in the emitter where the field is small, the quantum distribution function Maxwellian, whereas in the high field region in the collector the quantum distribution function departs from equilibrium behavior with more electrons occupying the high energy region. In Fig.4 we compare values for electron densities determined from classical and quantum calculations. The quantum electron concentration is obtained from the Wigner transport equation while the classical result is obtained from the BTE. It is clear to see that the electron densities calculated by two methods are very similar at two sides, while they show differences inside the device. The electron density by Wigner Equation is lower than that by BTE starting at $x = 0.06\mu m$. Then the difference reaches the peak at $x = 0.7\mu m$, where the emitter-base depletion region and the potential barrier peak are located. This phenomenon suggests that the quantum effect should be included where the potential is rapidly varying, especially near the base-emitter barrier. We interpret the lower carrier concentration for the quantum calculation at the barrier peak to be due to the QM result that the electron wave function will reach a minimum value at the barrier.

A detailed comparison of the quantum and classical electron distribution position by position is also instrumental for understanding quantum effects. The distribution functions are compared at $x = 0.09$ and $0.47\mu m$. No difference can be found at position $0.47\mu m$ between the classical and quantum distributions. This is because the field in these regions is relatively small and slowly varying, indicating little quantum confinement. As a result, semiclassical and quantum results coincide. However, at the point $x = 0.09$ which is near the barrier, the quantum distribution function predicts less electrons at high energy than does the classical result. In view of quantum mechanics, even electrons incident on the barrier with energy higher than the barrier peak may still be reflected back into the emitter, which can explain the lower high energy population of the quantum distribution function.

In summary we have developed a new method for investigating quantum effects in nanoscale devices. The method solves the Wigner transport equation using a spherical harmonic expansion and numerical methods. The results give the quantum distribution function throughout the devices. From the quantum distribution, most transport characteristics can be obtained.

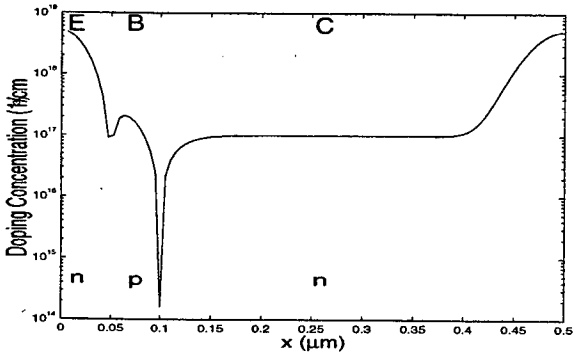


Fig.1 The doping profile of the NPN device.

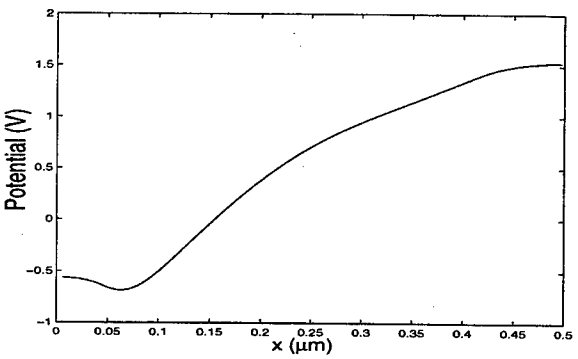


Fig.2 The potential of the NPN BJT device.

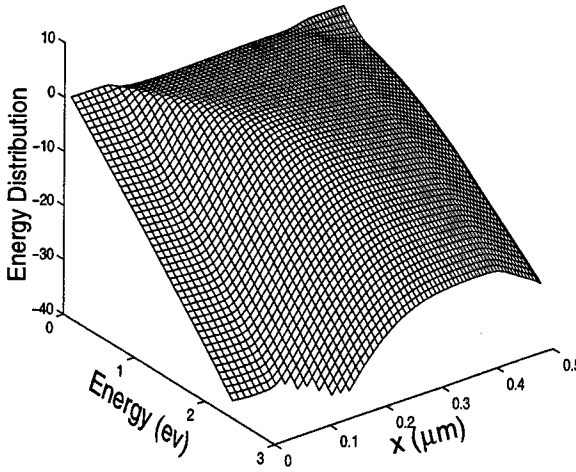


Fig.3 The 3D distribution function of the device by Wigner equation.

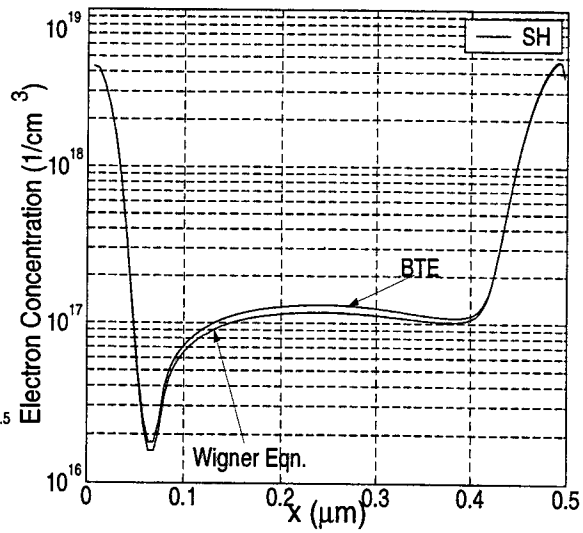


Fig.4 The comparison of the electron density between BTE and Wigner results.

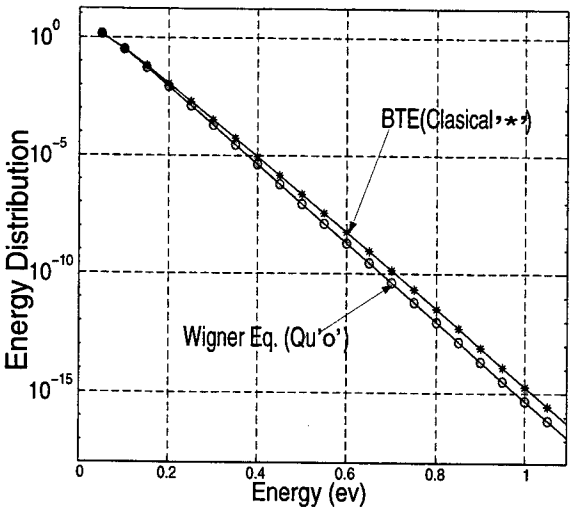


Fig.5 Distribution function comparison between BTE and Wigner at $x = 0.07\mu m$.

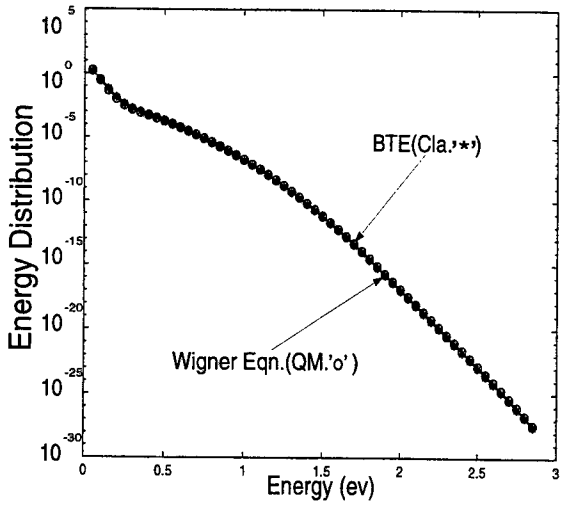


Fig.6 Distribution function comparison between BTE and Wigner at $x = 0.47\mu m$.

Acknowledgment

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Analysis of the Stresses Induced by Silicon Dioxide Growth in STI using a 3-Dimensional Calibrated Numerical Oxidation Modeling

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I. INTRODUCTION

Increased density in Si-based integrated circuits (IC) is obtained thanks to shallow trench isolation (STI) that are intrinsically three-dimensional structures. The major drawback of STI is the increase in the substrate dislocations generation [1] due to the combined influence of mechanical stresses and high temperature processing on implantation defects [2]. Thus, eliminating these trench dislocations partly requires to identify and to reduce the sources of stresses throughout the process. Although the measurements significantly contribute to the understanding of the stress induced problems [3], they suffer from a lack of resolution (around 0.5 μm for micro-Raman profiling technique) that does not allow to quantify local stress at trench edges. Recently, local stress fields associated with isolation trenches have been analyzed. However, due to the extremely complex nature of the problem, the investigations were limited to two dimensions [4], or simplified three-dimensional (3D) analysis [5-6]. This papers examines stress generation in STI using for the first time a 3D non-linear viscoelastic oxidation model. After having demonstrated the correct prediction of the silicon dioxide shape as well as of the stress level in the underlying silicon substrate in case of LOCOS structure, the effects of oxidation temperature and layout geometry are examined revealing the value of a real 3D analysis.

II. 3D OXIDATION MODEL

The initial strain condition induced by the net volume expansion of the oxidation reaction is defined by the Deal and Grove law. The resulting stress profile in the entire structure is computed assuming that silicon is an elastic material while silicon dioxide (SiO_2) and nitride (Si_3N_4) are non-linear (Eyring) viscoelastic bodies. Two different methods have been developed to solve the stresses in silicon, the boundary loading (BL) and fully-integrated (FI) methods, respectively [7] (Fig. 1). The second one, more accurate, is very computationally intensive and is only used for short time oxidations. Finally, the effects of stresses on the oxidation kinetics (diffusion coefficient and reaction rate) are also included.

The meshing task in our model can be described according to the following scheme. In an initial step, a tetrahedral mesh of the structure is generated using either MESH from ISE or TETMESH from SIMULOG. Then, a new SiO2 layer of infinitesimal thickness is generated on all interfaces between oxidizable and non-oxidizable materials preventing all discontinuous or singular displacements of mesh nodes. The changes in the geometry are described by the displacement field computed during the oxidation time step. In order to keep the same mesh resolution and quality during the simulation, nodes are either introduced or deleted from the initial mesh. Finally, when this procedure fails, a complete remeshing of the structure is performed preceded by an improvement of the surface discretization [8].

III. CALIBRATION

The capability to accurately predict the topography and stresses profiles depends on the calibration of the parameters of the model. This calibration has been performed in 2D [9] and is used for the 3D simulations. Fig. 2 compares SEM measurement of a LOCOS structure with its corresponding 2D and 3D simulations, and shows that this calibration is absolutely valid in 3D. To corroborate this result, following the approach proposed by Jones [10], the mechanical stresses, modeled (2D & 3D) and measured by micro-Raman technique, are compared. This comparison is performed: i) after nitride deposition (Fig. 3) including only intrinsic stress contribution and ii) after oxide growth (Fig. 4). The Raman spectrum is sensitive to mechanical strain in the crystal, which causes a small shift ($\Delta\omega$) in the position of the Raman peak from the reference peak (ω_0=520.25cm^{-1}) [10]: positive/negative shifts corresponding to compressive/tensile stress, respectively. A value of 1.4GPa (1.4x10^{10} dyn/cm^2) for the intrinsic nitride stress gives good agreement between models (2D & 3D) and measurements. By reaction, this induces compression in the substrate just under the film and tension elsewhere, as observed in

Fig. 6. The stress has several characteristics features seen in the Raman data and simulation (Fig. 7). In the silicon under the centre of the nitride, the compressive stress increases (i.e., the Raman shift reaches $+0.6cm^{-1}$), due to the non-vertical component of oxide growth at the edges of the field. At the edges of the nitride, we observe large stress peaks (two tensile and one compressive). In 2D, and even more in 3D simulations, the peaks are overestimated. This comes probably from the assumption of pure elasticity for silicon, whereas plastic phenomena might occur at such high stress levels. The larger values obtained for the 3D calculations can be explained by the non-infinite width of the nitride mask used to simulate the 3D LOCOS formation. However, these good results validated on 2D structures, allow now to study real 3D geometries. In particular, in LOCOS structures, the variation of the transition region (the so-called bird's beak - BB) between the active and isolation areas is a well known 3D effect [12]. In the hole structure (Fig. 5a), the BB is thinner in the corner of the active area compared to 2D structures, while in the island structure (Fig. 5b) it becomes thicker. The causes of these effects can be found both in the oxidant and stress profiles that are different in the angles of the patterns as revealed on Fig. 5c for the Raman shift of the island structure. The advantage of our 3D model over previous approaches [12] is to provide quantitative values of the stresses even at low temperature thanks to a non-linear viscoelastic modeling.

IV. STI ANALYSIS

In order to quantify the increase of the stress in island type active area compared to "long line" one, different STI processes have been simulated in 3D. The simulations include the patterning of pad oxide and nitride layer, the etching of silicon, the filling of the trench by oxide and the final oxidation (820 °C) dedicated to the rounding of the trench corner, in order to eliminate parasitic corner effects. Fig. 6 shows the 3D profiles of the hydrostatic pressure in two of these structures. Fig. 6a corresponds to a 0.2µm wide active area and Fig. 6b to a 0.2µmx0.2µm active area square, for which micro-Raman measurements can not be performed due to the extremely small geometrical sizes. One can see that the stress is larger for square than for line and that it reaches a maximum at the edges as revealed by the 2D cross section of the line structure given in Fig. 7a. Looking at the 1D stress profiles taken at the center of the active area along the vertical direction (Fig. 7b), one can see that in squares the stress is two times larger than in a line with the same dimensions. Moreover, we observed that the compressive stress reduces once reaching the top of the active area. This phenomenon is due to the reaction to the bending nitride film. If we increase the temperature of oxidation to 875°C (Fig. 8a) and 950°C (Fig. 8b), respectively, then one can see that the stress increases dramatically, in particular at the edges of the trench. The reason comes from the oxidation velocity that is greater at high temperature and that induces more silicon consumption. As a result, Fig. 9 shows that the stress at the center of the structure along the vertical direction increases up to 950°C, being two times larger at this highest temperature compared to the lowest one.

V. SUMMARY

In combination with Micro-Raman and SEM structural characterization, accurate calibration of a viscoelastic oxidation model has been obtained. The benefit of the extension to three dimensions to account for effect such as those at corners in Shallow-Trench Isolation structures has been demonstrated.

ACKNOWLEDGEMENTS

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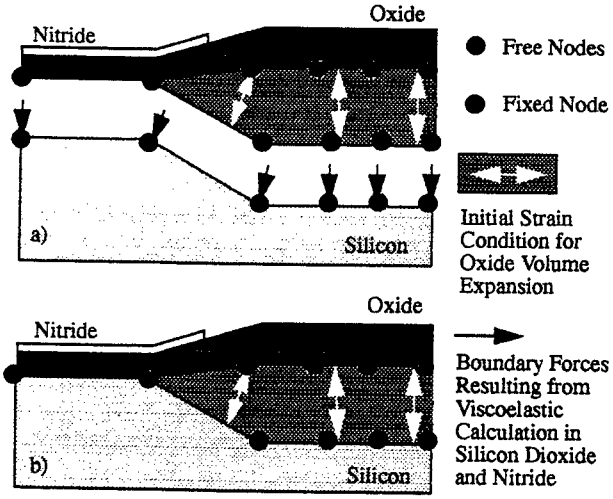


Figure 1: Schematic description of the a) boundary loaded and b) fully integrated method to calculate the stresses in silicon during an oxidation step.

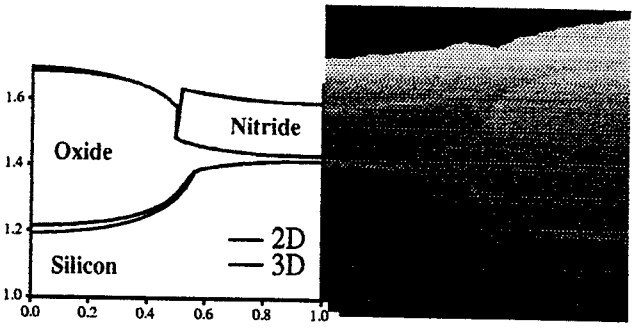


Figure 2: Comparison between SEM and simulations performed in 2D with IMPACT and in 3D with PROMPT for a LOCOS structure. Nitride thickness is 160 nm, pad oxide 15 nm, oxidation performed at 920 °C during 360 minutes.

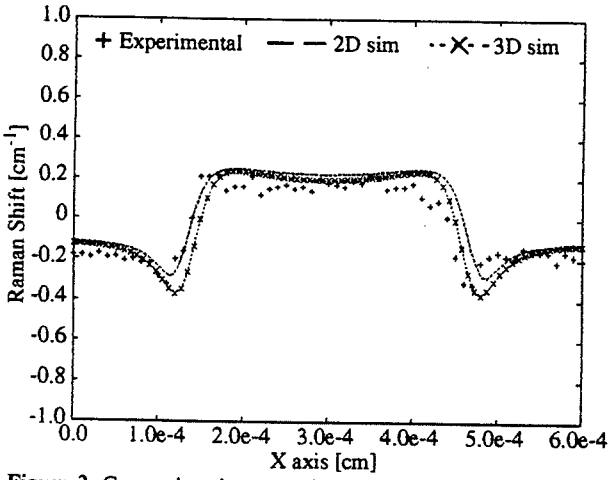


Figure 3: Comparison between simulated and measured Raman for nitride stripes of width 3.5 μm and thickness 130 nm with a pad oxide of 10 nm. The Raman shift was simulated from computed 2D & 3D stress data. Raman data were measured at 488 nm. This result includes only the intrinsic stress.

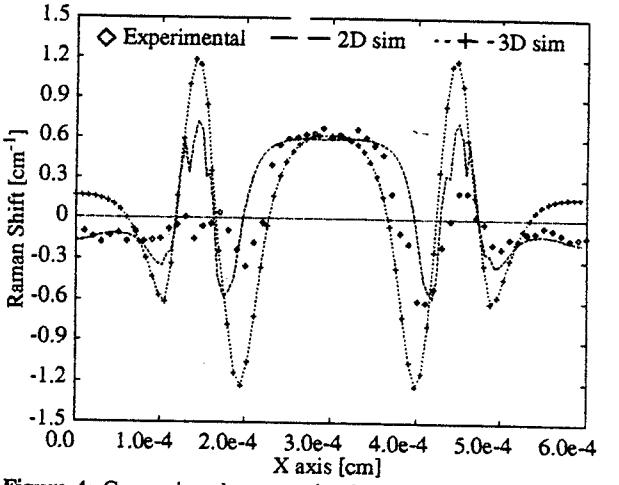


Figure 4: Comparison between simulated and measured Raman for a LOCOS structure grown at 875 °C (360 min) with a nitride stripe of width 3.5 μm and thickness 130 nm; pad oxide of 10 nm. Raman data were measured at 457.9 nm. This result includes the intrinsic stress and the oxide growth contributions.

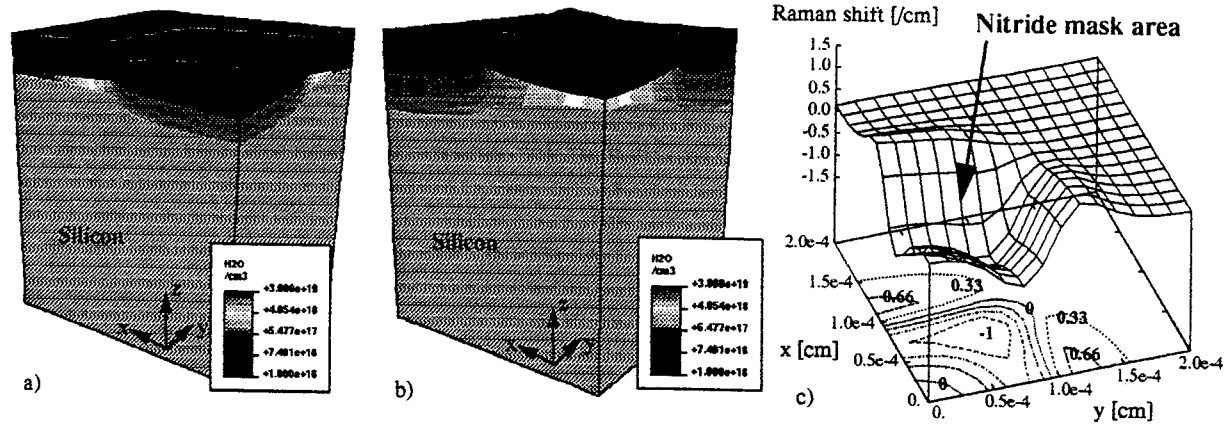


Figure 5: 3D simulations of LOCOS in case of a) hole structure and b) island structure. The oxidation was performed at 920 °C during 120 minutes. Pad oxide thickness is 20 nm, nitride thickness is 160 nm. The pattern geometry is 2x2 μm^2 with nitride mask 1x1 μm^2. The calculated Raman shift (c) for the island structure exhibits the well known 3D corner effect that is a high tensile peak corresponding to the large bending of the nitride layer.

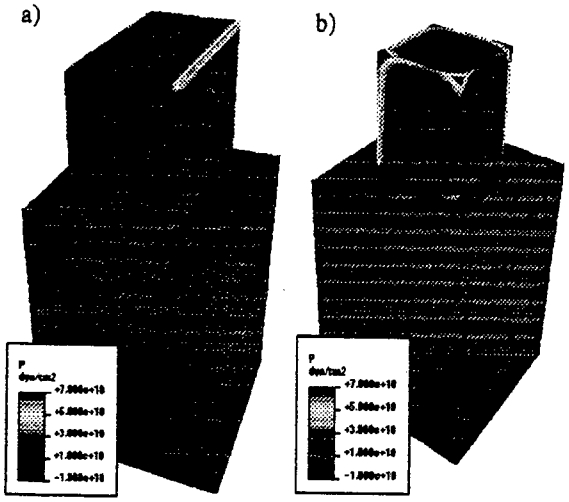


Figure 6 : Comparison between the simulated a) long and b) island active areas surrounded by a shallow trench isolation. The pressure distribution is induced by the oxide growth after filling of the trench. The active and isolation areas are 0.2 µm wide. The STI is 0.25 µm deep. The nitride and oxide layers have been removed for vizualisation.

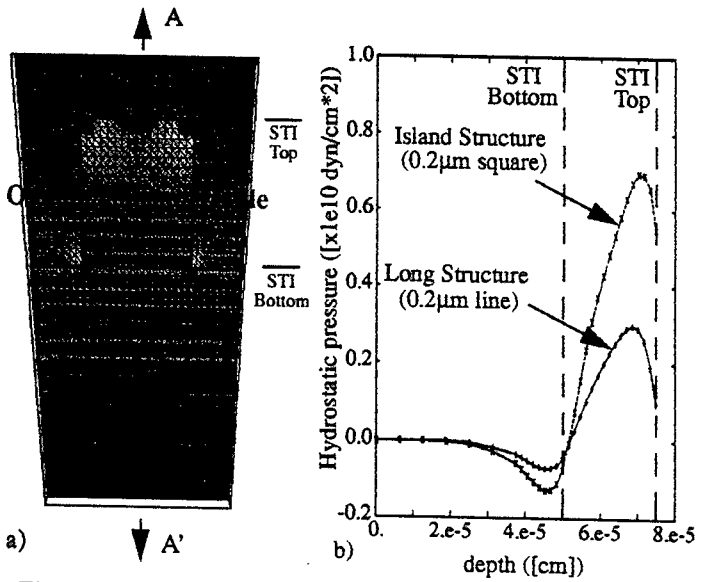


Figure 7 : Comparison of the hydrostatic pressure for the 2 active areas defined in Fig. 6. a) 2D cross-section of the line structure with its pressure profile, b) 1D profiles of the pressure along the depth AA'.

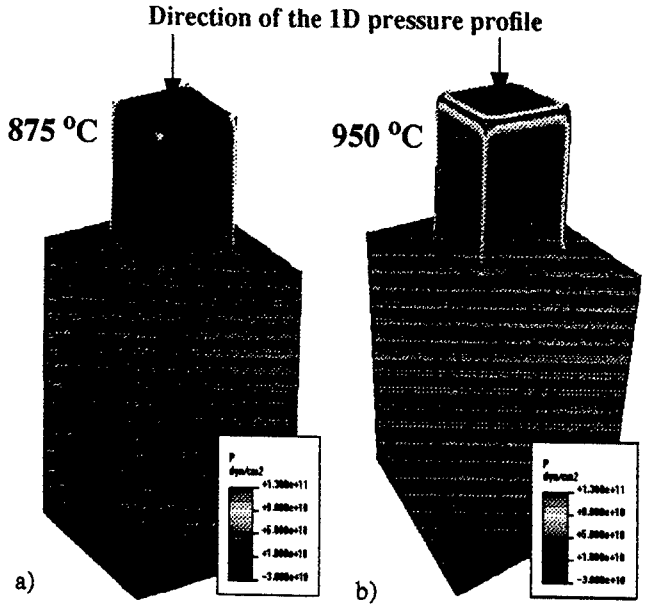


Figure 8 : Comparison between the simulated island active areas surrounded by a shallow trench oxidized in wet ambient at : a) 875°C and b) 950°C. The pressure distribution is given in both cases. The nitride and oxide layers have been removed for vizualisation.

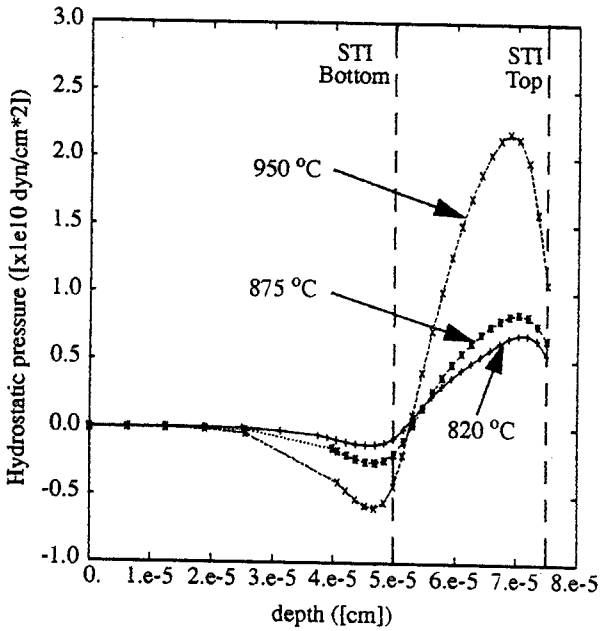


Figure 9: Comparison of the hydrostatic pressure for the 3 island type active areas defined in Figs. 6 & 8. The direction of the pressure profile is defined in Fig. 8.

Including the Pauli Exclusion Principle in Semiconductor Device Simulation

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1 Introduction

As devices approach the nanoscale regime, doping and mobile carrier densities are becoming increasingly larger and are often degenerate. To help accurately account for these high densities, we have developed a method for including the Pauli exclusion principle in semiconductor device modeling. To achieve this we build on the work of Lin et al, who calculated the distribution function for both degenerate and nondegenerate electron ensembles from solutions to a Boltzmann transport equation for homogenerous silicon. In this paper, we present a new technique to determine the energy distribution function of a degenerate electron gas in a very nonhomogeneous silicon device. This is achieved by incorporating the quantum-mechanical Pauli exclusion principle into the Boltzmann transport equation, and solving it for a deep submicron silicon device. The resulting Boltzmann equation takes on a non-linear form which is solved by means of a numerical iteration method. From our simulation results we find that for regions of high electron concentration the distribution function approaches the Fermi-Dirac form, while in regions of lower electron concentration Boltzmann type distributions are obtained.

2 Pauli Excluded Boltzmann Transport Equation(PEBTE)

We will refer to the Boltzmann transport equation, which includes the Pauli exclusion principle, as the Pauli-Excluded Boltzmann Transport Equation(PEBTE). The degenerate distribution function is obtained from the solution to the PEBTE. The well-known Boltzmann Transport Equation is:

$$\vec{v}(\vec{k})\nabla_r f(\vec{r},\vec{k},t) - \frac{q\vec{E}}{\hbar}\nabla_k f(\vec{r},\vec{k},t) + \frac{\partial f(\vec{r},\vec{k},t)}{\partial t} = \left.\frac{\partial f(\vec{r},\vec{k},t)}{\partial t}\right|_{coll} \tag{1}$$

where $\vec{v}(\vec{k})$ is the velocity, $\vec{k}$ is the electron wave vector, $f(\vec{r},\vec{k},t)$ is the momentum distribution function and $\vec{E}$ is the electric field. The collision term of Eq. (1) can be expressed as

$$\left[\frac{\partial f(\vec{r},t)}{\partial t}\right]_{coll} = \frac{1}{(2\pi)^3}\sum_j \int \left[f(\vec{r},\vec{k}')S_j(\vec{k}',\vec{k})(1-f(\vec{r},\vec{k})) - f(\vec{r},\vec{k})S_j(\vec{k},\vec{k}')(1-f(\vec{r},\vec{k}'))\right] d^3\vec{k}' \tag{2}$$

where $S_j(\vec{k}',\vec{k})$ is the transition probability of an electron scattering from $\vec{k}$ state to $\vec{k}'$ state by the j type of scattering. The effects of the Pauli exclusion principle are implied by the factors in the form of $(1-f)$ in the collision term. Inclusion of the Pauli factors gives rise to a nonlinear BTE. It is very difficult to solve this nonlinear equation. For nondegenerate conditions the Pauli exclusion principle can be neglected, and we will get a linear BTE. But, in the heavily doped $n^+(p^+)$ region

such approximations are no longer valid, and we can not ignore the $(1-f)$ term. To solve this equation, we adopt the Spherical Harmonic Boltzmann Transport Equation(SHBTE) approach [2]-[7]. We then modify the approach to account for the nonlinear Pauli factors in the collision integral. After considerable of mathematical manipulation[1, 4], the collision term can be expressed as

$$\begin{aligned}\left[\frac{\partial f(\vec{r},t)}{\partial t}\right]_{op} &= \Big\{C_{ab}\left[f_0^0(\vec{r},\varepsilon+\hbar\omega_{op})e^{\hbar\omega_{op}/KT} - f_0^0(\vec{r},\varepsilon) - f_0^0(\vec{r},\varepsilon+\hbar\omega_{op})f_0^0(\vec{r},\varepsilon)/N_{op}\right] \\ &+C_{em}\left[f_0^0(\vec{r},\varepsilon-\hbar\omega_{op}) - f_0^0(\vec{r},\varepsilon)e^{\hbar\omega_{op}/KT} + f_0^0(\vec{r},\varepsilon-\hbar\omega_{op})f_0^0(\vec{r},\varepsilon)/N_{op}\right]\Big\} Y_0^0 \\ &-\frac{(\varrho-1)\pi D_{op}^2}{\rho\omega_{op}}\sum_{l>0,m} N_{op}\left[g(\varepsilon+\hbar\omega)+g(\varepsilon-\hbar\omega)e^{\hbar\omega/KT}\right] f_l^m(\vec{r},\varepsilon,t)Y_l^m(\theta,\psi) \qquad (3)\end{aligned}$$

where ϱ is the number of equivalent valleys, D_{op} is the optical deformation potential; ω_{op} is the frequency of the optical intervalley phonon; ρ is the silicon density; g is the density of state and $N_{op} = 1/(e^{\hbar\omega/KT}-1)$; and

$$C_{ab} = (\varrho-1)\frac{\pi D_{op}^2}{\rho\omega_{op}}N_{op}g(\varepsilon+\hbar\omega); C_{em} = (\varrho-1)\frac{\pi D_{op}^2}{\rho\omega_{op}}N_{op}g(\varepsilon-\hbar\omega) \qquad (4)$$

After employing the spherical harmonic method for solving the Boltzmann equation to the left hand side of eqn.(1) as well, the final PEBTE can be expressed as

$$\begin{aligned}&-\frac{v}{3\gamma}\left[\frac{\partial}{\partial x}\left(\gamma\tau v\frac{\partial F_0^0}{\partial x}\right)+\frac{\partial}{\partial y}\left(\gamma\tau v\frac{\partial F_0^0}{\partial y}\right)\right] \\ &= \Big\{C_{ab}\left[F_0^0(\vec{r},H+\hbar\omega_{op})e^{\hbar\omega_{op}/KT} - F_0^0(\vec{r},H) - F_0^0(\vec{r},H+\hbar\omega_{op})F_0^0(\vec{r},H)/N_{op}\right] \\ &+C_{em}\left[F_0^0(\vec{r},H-\hbar\omega_{op}) - F_0^0(\vec{r},H)e^{\hbar\omega_{op}/KT} + F_0^0(\vec{r},H-\hbar\omega_{op})F_0^0(\vec{r},H)/N_{op}\right]\Big\} \\ &+\left[\frac{2F_0^0(\vec{r},2H+q\phi+\varepsilon)}{\tau_{ii}(2H+2q\phi+\Delta\varepsilon_{ii})} - \frac{F_0^0(\vec{r},H)}{\tau_{ii}(H+q\phi)}\right] + \frac{f_T}{\tau_{0,rec}^{out}}exp-(\frac{H_t-H}{KT}) - \frac{1-f_T}{\tau_{0,rec}^{out}}F_0^0(\vec{r},H) \qquad (5)\end{aligned}$$

where γ represents the dispersion relation; and

$$\frac{1}{\tau} = \frac{1}{\tau_{op}^{out,\mp}} + \frac{1}{\tau_{ii}} + \frac{1-f_T}{\tau_{0,rec}^{out}} + \frac{1}{\tau_{ac}} + \frac{1}{\tau_{imp}} \qquad (6)$$

The products of the form $F_0^0(\vec{r},H+\hbar\omega_{op})F_0^0(\vec{r},H)$ give the nonlinearities, so finding F_0^0 becomes especially difficult. By using a specially tailored numerical iteration method aimed at maximizing diagonal dominance we can overcome this nonlinear problem.

3 Results: Solutions of the PEBTE

We obtained solutions of the PEBTE for a $n^+ - n - n^+$ diode. The doping profile of this device is shown in Fig. 1. The doping concentration of the n^+ region is $1\times10^{21}cm^{-3}$, and $1\times10^{16}cm^{-3}$ is for the n region. From our simulation results we can get insight into the effect of the Pauli exclusion principle on the distribution function.

The distribution function of the nondegenerate n region($x = 0.5\mu m$) is shown in Fig. 2. As expected, the PEBTE and BTE results are approximately the same, and can be approximated by the Boltzmann function. Thus we can ignore the exclusion principle in this low carrier concentration region. Fig. 3 shows the distribution function in the n^+ region($x = 0.1\mu m$). The calculated distribution function has the form of the Fermi-Dirac function. The probability distribution attains values which are much greater than 1 when exclusion is ignored. So neglecting the exclusion principle under high concentration regions can result in considerable error.

The distribution function of the complete device is shown in Fig. 4 and Fig. 5 for PEBTE and BTE

respectively. The Fermi-Dirac type character resulting from the exclusion principle is especially evident in Fig. 4. The electron concentration of the $n^+ - n - n^+$ device is shown in Fig. 6. We calculate the electron concentration by the following equation.

$$n = \int_{\varepsilon} g(\varepsilon) F_0^0 d\varepsilon \tag{7}$$

We can see that the concentrations are almost the same for PEBTE and BTE in the n region. However, they are quite different in the n^+ region with the carrier concentration is significantly reduced due to exclusion effects.

4 Conclusion

In this paper, the quantum effect of the Pauli exclusion principle in a semiconductor device is addressed in detail. We formulated the Boltzmann transport equation, including the Pauli exclusion principle, as a nonlinear differential equation. By using a numerical iteration method we can overcome the difficulties in solving a nonlinear problem. For regions of high concentration, the solution tends toward the Fermi-Dirac function. On the other hand, Boltzmann-like behavior is observed at lower electron concentrations.

Acknowledgement

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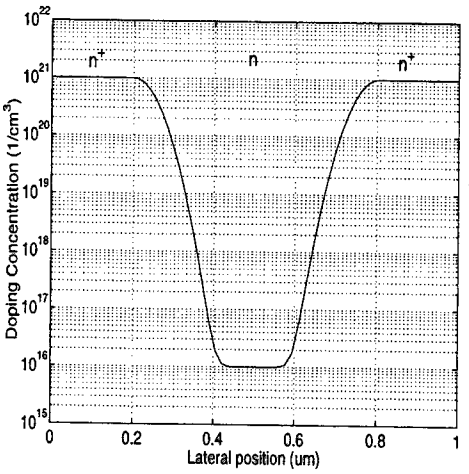


Fig. 1 Doping profile for the $n^+ - n - n^+$ device.

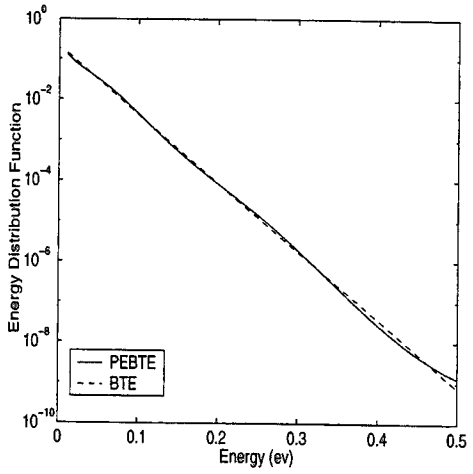


Fig. 2 The energy distribution function at x=0.5 μm.

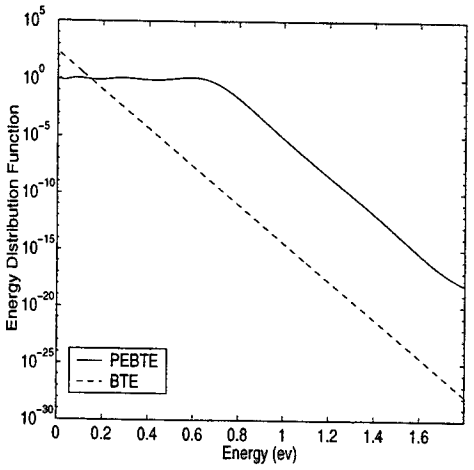


Fig. 3 The energy distribution function at x=0.1 μm.

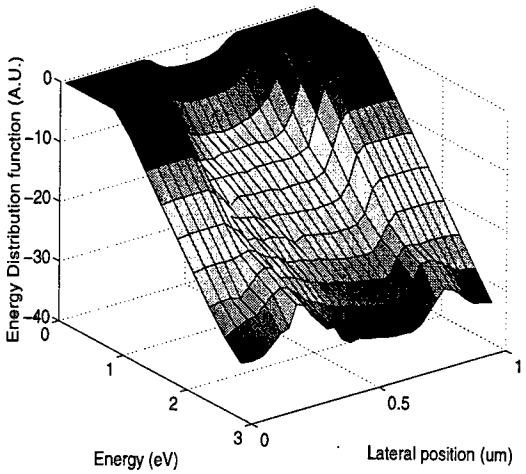


Fig. 4 The energy distribution function for whole device from PEBTE.

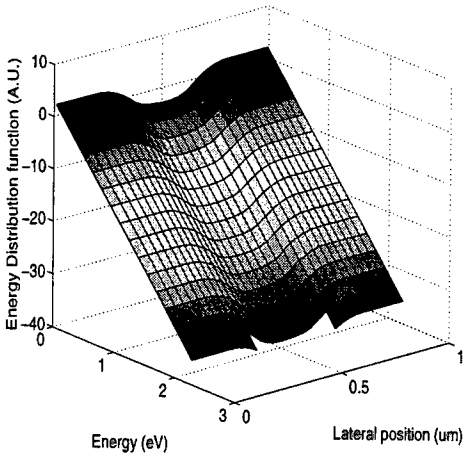


Fig. 5 The energy distribution function for whole device from BTE.

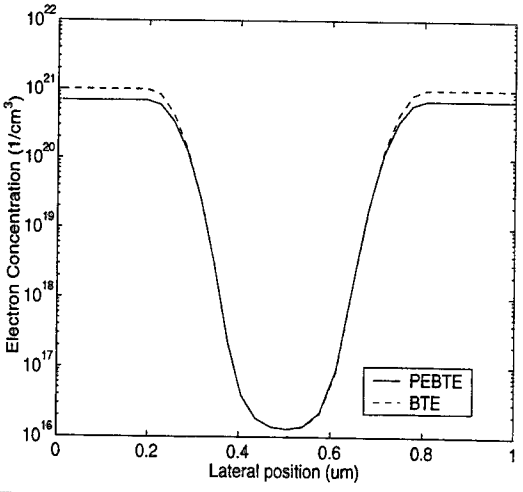


Fig. 6 The electron concentration of the device.

A General Approach for Calculation of Thermal Noise Currents in Semiconductor Devices and its Application to RF Noise Modeling of MOSFET's

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Abstract

A general approach, based on the characteristic potentials, is developed to calculate the short-circuit noise currents including thermal noise and excess noise (1/*f* noise and *g-r* noise) currents of multi-terminal semiconductor devices with arbitrary geometry under a given dc bias. We present the results obtained by applying this approach to thermal noise of nMOSFET's which include the frequency, channel length, and bias dependences of the drain and gate power and correlation noise spectra.

Introduction

Modeling of high frequency noise in MOSFET's is of primary importance for advanced submicron CMOS technologies used for analog and RF applications[1]. Recently, shot noise in multi-terminal diffusive mesoscopic conductors has been calculated using "the characteristic potentials"[2]. We have found that a similar technique can also be applied to calculate thermal noise and excess noise (1/*f* noise and *g-r* noise) of multi-terminal semiconductor devices. We show that this approach based on the characteristic potentials provides a direct and straightforward method to calculate the short-circuit thermal and excess noise currents of any semiconductor devices. In this paper, we present the results obtained by applying this approach to thermal noise of MOSFET's.

Formula for short-circuit thermal noise currents

We consider a multi-terminal semiconductor device of arbitrary 3-D shape with volume V, which is connected to N perfect metallic contacts of area A_n, n = 1, 2,..., N(see Fig. 1). A^* in Fig. 1 denotes the free surface. We introduce the characteristic potentials $\phi_n(\mathbf{r},\omega)$, n = 1, 2,..., N for the n-th contact under a given dc bias, which satisfy $\nabla \cdot [(\sigma_0(\mathbf{r})+j\omega\varepsilon(\mathbf{r}))\nabla\phi_n(\mathbf{r},\omega)] = 0$ inside the devices and $\mathbf{n}\cdot\nabla\phi_n(\mathbf{r},\omega)\,|_{A^*} = 0$ and $\phi_n(\mathbf{r},\omega)\,|_{Am} = \delta_{n,m}$, as boundary conditions, where $\sigma_0(\mathbf{r})$ is the dc conductivity under the given dc bias, $\varepsilon(\mathbf{r})$ is the electric permittivity, and $j = \sqrt{-1}$. Then, with these characteristic potentials and the accurate noise current density equation, given by $\Delta\mathbf{J}(\mathbf{r},t) = \sigma_0(\mathbf{r})\Delta\mathbf{E}(\mathbf{r},t) + \eta_{ex}(\mathbf{r},t) + \eta_{th}(\mathbf{r},t)$ with $\eta_{ex}(\mathbf{r},t) = \Delta\sigma(\mathbf{r},t)\,\mathbf{E}_0(\mathbf{r})$ being the excess noise source and with $\eta_{th}(\mathbf{r},t)$ being the diffusion noise source[3], we can show that the cross power spectral density, $S^{th}_{\Delta I_n,\Delta I_k}(\omega)$, between the short-circuit thermal noise currents for the n-th and k-th ohmic contacts, $\Delta I_n(t)$ and $\Delta I_k(t)$, under the given dc bias, becomes[4]

$$S^{th}_{\Delta I_n \Delta I_k}(\omega) = 4k_B \int_V d\mathbf{r}\,\nabla\phi_n(\mathbf{r},\omega)\cdot\left[T_n(\mathbf{r})\sigma_{no}(\mathbf{r}) + T_p(\mathbf{r})\sigma_{po}(\mathbf{r})\right]\nabla\phi_k^*(\mathbf{r},\omega) \tag{1}$$

where k_B is the Boltzmann constant, T_n and T_p the electron and hole carrier temperatures, σ_{no} and σ_{po} the dc electron and hole conductivities, ϕ_k^* the complex conjugate of ϕ_k, and we have used $S\eta_{th}(\mathbf{r},\mathbf{r}',\omega) = 4k_B(T_n\sigma_{no} + T_p\sigma_{po})\delta(\mathbf{r}-\mathbf{r}')$:I , with I being the unit tensor.

Results and Discussions

Figs. 2-9 show the simulated frequency dependence of the power spectral densities($S_{id}(\omega) \equiv S_{id,id}(\omega)$ and $S_{ig}(\omega) \equiv S_{ig,ig}(\omega)$) and the real and imaginary parts of the cross power spectral density($S_{ig,id}(\omega)$) of the short-circuit drain thermal noise current $i_d(t)$ and the gate thermal noise current $i_g(t)$ for nMOSFET's with gate oxide thickness(t_{ox}) of 200 Å and substrate doping of 1×10^{15} cm^{-3} and various channel

length(L) operating in the both linear and saturation regions. Figs. 10 and 11 show the channel length(L) dependence of S_{id} and S_{ig} in the linear and saturation regions. As we see in Figs. 2-9, $S_{id}(\omega)$ is independent of ω and $S_{ig}(\omega)$ is proportional to ω^2 as predicted by the classical theory by van der Ziel[5] and also by the steady-state Nyquist theorem[6][7]. Fig. 10 shows that $S_{id}(\omega)$ is proportional to $1/L$ in the linear region as predicted by the steady-state Nyquist theorem($S_{id} = 4k_BTI_D/V_D$)[6]. The result that $S_{ig}(\omega)$ is proportional to L^{α} with $\alpha > 2$ in both linear and saturation region(Fig. 11) can be explained by noting that S_{ig} is proportional to C_{gs}^2 according to the classical theory[5] and the steady-state Nyquist theorem[6].

In the classical theory[5], where the gate thermal noise is assumed to be due to the capacitive coupling between the channel and the gate, $S_{ig,id}(\omega)$ has only the imaginary part which is positive and proportional to ω, but both our results of this paper and the steady-state Nyquist theorem predict that $S_{ig,id}(\omega)$ has both real and imaginary parts which are negative, and also predict that the real part is proportional to ω^2 and the imaginary part is proportional to ω. The existence of the real part of $S_{ig,id}$ and the negative polarity of the imaginary part have been confirmed by other researchers[8][9]. Our theory shows that the gate thermal noise is not due to the capacitive coupling between the channel and the gate. The ω-dependence of S_{ig} can be explained by noting that the power spectral density of the equivalent thermal noise current of a circuit with a resistor R and a capacitor C connected in series is given by $S_{AI} \approx 4k_BT\omega^2C^2R$ for $(\omega CR)^2 << 1$.

Fig. 12 shows the V_D-dependence of the noise factor of drain noise current, γ ($\equiv S_{id}(\omega)/S_{id}(\omega)|_{V_D \to 0}$), calculated using Eq. (1), and compares the calculated results with the measured data[10]. For reference, the results from the steady-state Nyquist theorem($S_{id} = 4k_BTI_D/V_D$) is also shown in Fig. 12. In the linear region, the calculated values are well predicting the measurements, but in the saturation region the calculated ones are underestimating the measurements. We are now studying the origin of this discrepancy and preliminarily suspect that this comes from the shot noise in the drain depletion region arisen by possibly the carrier number fluctuation, which was not considered in the calculation.

Finally, we expect that this new approach can clarify and correct the mistakes in the assumptions made during derivation of the steady-state Nyquist theorem.

Conclusion

A general approach, based on the characteristic potentials, has been developed to calculate the short-circuit noise currents including thermal noise and excess noise currents of multi-terminal semiconductor devices with arbitrary geometry under a given dc bias. By applying this to nMOSFET's, we have obtained the noise characteristics of the devices as functions of frequency, bias, and channel length and have suggested that the origin of the gate thermal noise of the devices is not the capacitive coupling as the classical theory explained.

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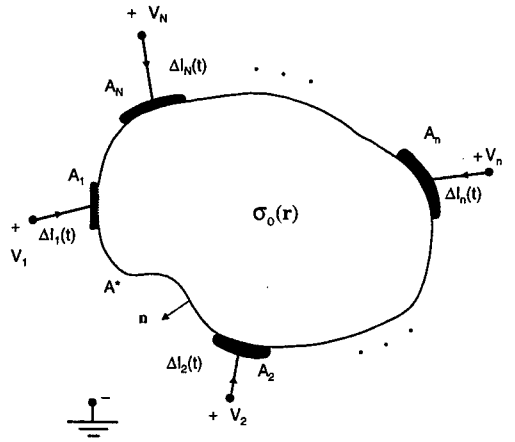


Fig. 1 The arbitrarily shaped N-terminal device. A_m is the m-th electrode, A^* is the free surface, $\mathbf{n}$ is the outward normal vector of the boundary surface.

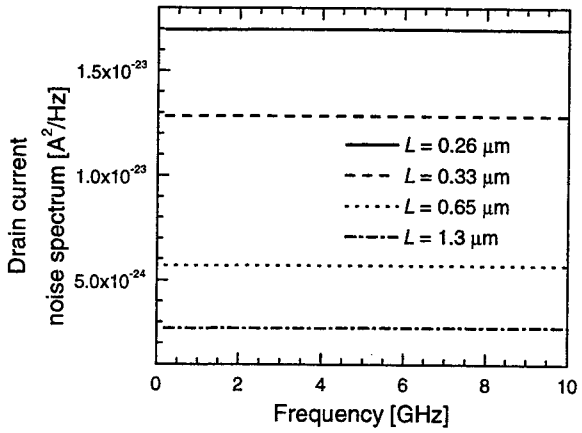


Fig. 2 Simulated drain noise current power spectral density(S_{id}) with various channel length(L) in the linear region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 0.1 V.

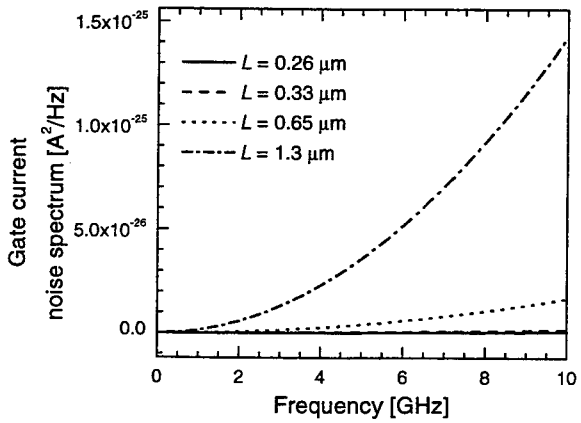


Fig. 3 Simulated gate noise current power spectral density (S_{ig}) with various channel length(L) in the linear region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 0.1 V.

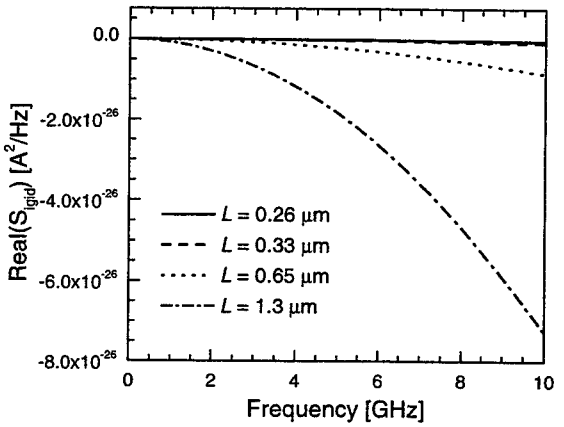


Fig. 4 Simulated real part of the cross power spectral densities of gate and drain noise currents($S_{ig,id}$) with various channel length(L) in the linear region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 0.1 V.

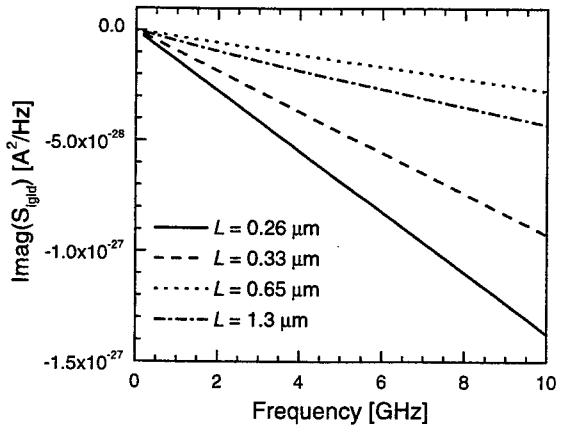


Fig. 5 Simulated imaginary part of the cross power spectral densities of gate and drain noise currents($S_{ig,id}$) with various channel length(L) in the linear region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 0.1 V.

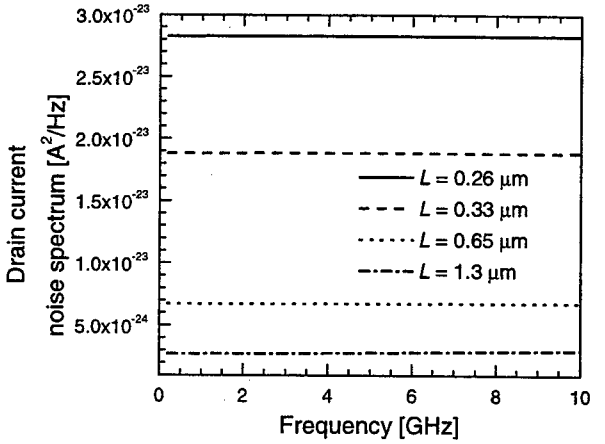


Fig. 6 Simulated drain noise current power spectral density (S_{id}) with various channel length(L) in the saturation region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 3 V.

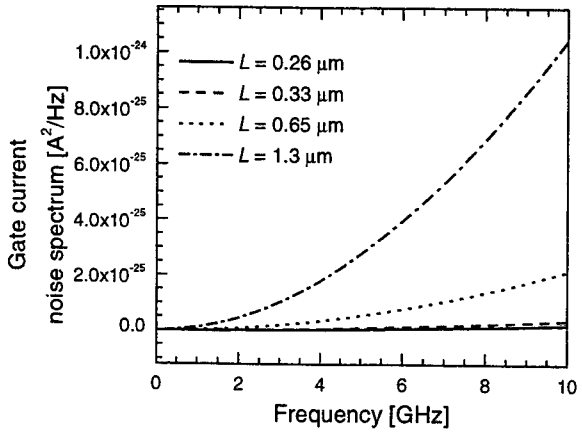


Fig. 7 Simulated gate noise current power spectral density (S_{ig}) with various channel length(L) in the saturation region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 3 V.

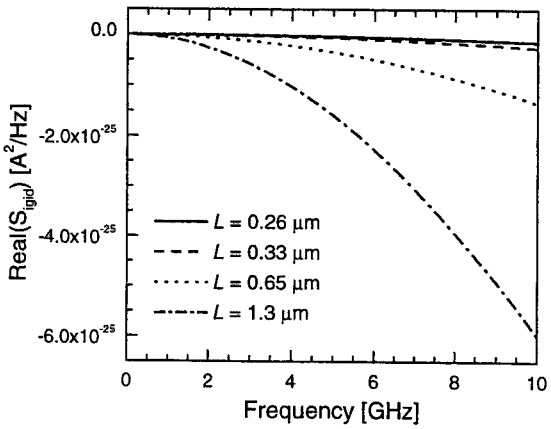


Fig. 8 Simulated real part of the cross power spectral densities of gate and drain noise currents($S_{ig,id}$) with various channel length(L) in the saturation region as a function of frequency. V_T = 0.35 V, V_{GS} = 3 V, V_{DS} = 3 V.

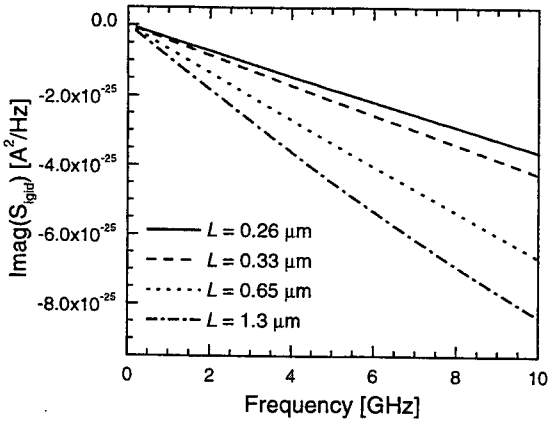


Fig. 9 Simulated imaginary part of the cross power spectral densities of gate and drain noise currents($S_{ig,id}$) with various channel length(L) in the saturation region as a function of frequency. V_T = 0.35 V,V_{GS} = 3 V, V_{DS} = 3 V.

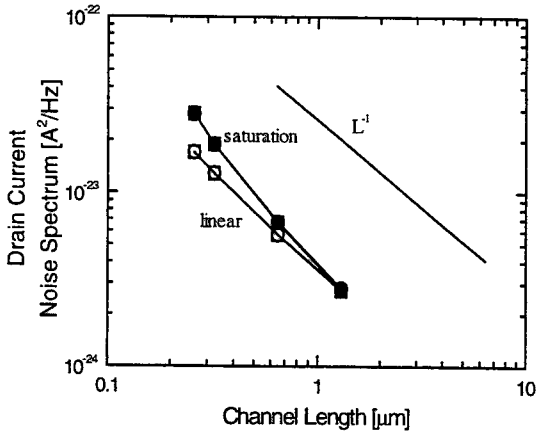


Fig. 10 Simulated drain noise current power spectral density(S_{id}) as a function of channel length(L) in both the linear(open) and saturation regions(solid) at 1 GHz and 5 GHz.

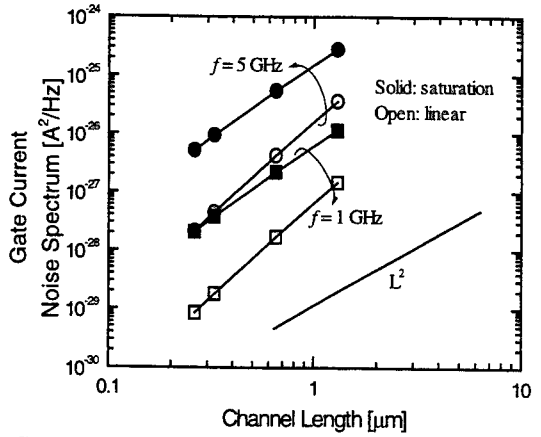


Fig. 11 Simulated gate noise current power spectral density (S_{ig}) as a function of channel length(L) in both the linear(open) and saturation regions(solid) at 1 GHz(square) and 5 GHz(circle).

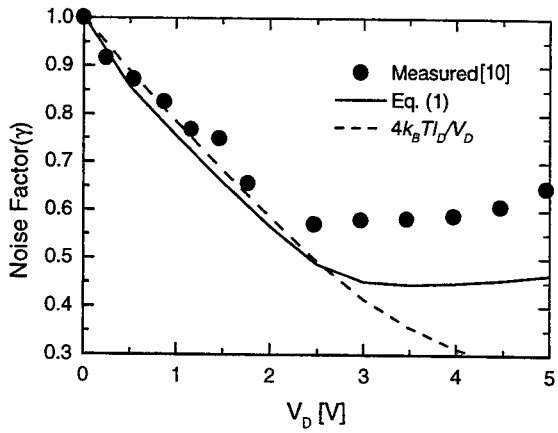


Fig. 12 Measured and simulated noise factor($\gamma \equiv S_{i_d}(\omega)/S_{i_d}(\omega)\big|_{V_D=0}$) of a long channel nMOSFET(L = 16 μm, W = 12 μm, V_T = 0.8V) vs. drain voltage when V_{GS} = 4 V.

Role of Shot Noise in Sub-micron MOSFET's

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1. Introduction

We report a significant shot noise component in sub-micron MOSFET's operating in strong inversion. Since it is very virtually impossible to distinguish shot and thermal noise experimentally, a quasi 3-D MOS device simulation was used. The accuracy of the 3-D noise simulator was first verified by comparing simulated noise parameters to measured noise parameters. For long channel devices thermal noise is shown to be the main source of noise, however for sub-micron devices with Leff less than 0.5μm, the shot noise becomes dominant. The shot noise component is primarily produced near the source of the device. The hot electron induced noise was determined to be less important then previously thought. It has been discussed in previous papers [1-3] and will not be re-addressed here.

2. Numerical Method

Fig. 1a depicts the procedure involved in calculating the noise powers and correlation factors at each terminal and between every terminal, respectively. A noise current is injected at each point within a 2D-device simulator and the terminal currents are recorded as a function of the position at which the noise current is injected. From these results, a scalar Green's function is constructed. By using this Green's function and the fact that each point within the device contributes diffusion noise, the total noise current at each terminal due to all the internal noises within the device is obtained by integrating over the device domain. More detail on the numerical method is available in [1-3] and [4] The microscopic noise sources injected at each node are diffusion noise - *note diffusion noise encompasses both shot and thermal components (see Fig. 1b).*

3. Comparison with Experiment

Fig. 2 compares computed noise parameters with measured results from a 0.5μm LDD nMOS device. The simulator was preliminary calibrated using comparison of simulated DC I-V characteristics of the device with measured IV curves. This was the only fitting made in the simulation. The results for small signal and noise parameters agree extremely well, thereby giving us confidence that the noise is modeled correctly.

4. Comparison of Long Channel and Short Channel MOSFETs

Fig. 3a and 4a show 3D plot of the drain local noise density for a 10.45μm and 0.45μm device, respectively. The local noise density for the 10.45μm looks as expected from classic long channel theory; i.e. it decreases as one moves away from the source region. However, the local noise density of the 0.45μm device is different in comparison to the long channel device. Furthermore, it looks very similar to the local noise density in the base region of a bipolar transistor (see [2]). Fig. 3b and 4b show the 2D local noise density profile nearest to the channel surface for the 10.45μm and 0.45μm devices, respectively. For the short channel device, the local noise density is a maximum near the center of the channel, but is skewed towards the source end. For the long

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channel device it is more or less evenly distributed along the channel with the maximum occurring near the source.

Shot noise occurs in the presence of a diffusion type current whereas thermal noise occurs in the presence of a drift (or electric field driven) current - see Fig. 5. If both diffusion and drift currents are present, both thermal and shot noises are present. One way to determine the amount of shot noise to thermal noise is to compare the amount of diffusion current to drift current. In Fig. 6 we have plotted the ratio of the diffusion current to drift current along the length of a long channel and short channel devices. For the long channel device the majority of current is drift current, as one would expect. Only near the source and drain is there some sign of diffusion current. For the short channel device there is a significant component of diffusion current near the source end. The diffusion component can be twice the drift current when the device is operating in strong inversion. Furthermore, the diffusion current takes up to 20% of the total channel length. From this one can conclude that there is a significant component of shot noise near the source region of the device.

Fig. 7 plots the drain current noise as a function of the bias current and the zero voltage drain-to-source conductance, g_{do} for a long channel device. The various curves are for various values of drain-source voltage. It is well known that for a long channel device the noise power is directly proportional to g_{do}. This is evident from Fig. 7a. Note that Fig. 6a and Fig. 7 are both consistent since they indicate that there is a small amount of shot noise.

Fig. 8 depicts the drain current noise as a function of the bias current and the zero voltage drain-source conductance for a short channel device. The various curves are for various values of drain-source voltage. The drain noise for modest bias follows the classical shot noise equation ($2qI_{ds}$). The best operating point for noise (see Fig. 2) occurs in the region where shot noise is predominant. For higher values of current both thermal and shot noise are present within the device. In Fig. 8b we can see that there is no obvious relationship between drain noise and g_{do}. However, there does exist various equations relating g_{do} to the drain current noise, but most of these relationships have many fitting parameters.

5. Conclusions

- Diffusion-drift based 2D noise simulation agrees well with experimental data for sub-micron MOSFETs
- Hot electron contribution to noise is not significant for 0.5 um MOSFETs
- High excess noise is caused by shot noise
- Strong temperature dependence of noise spectra indicates presence of shot noise in short-channel MOSFETs

6. References

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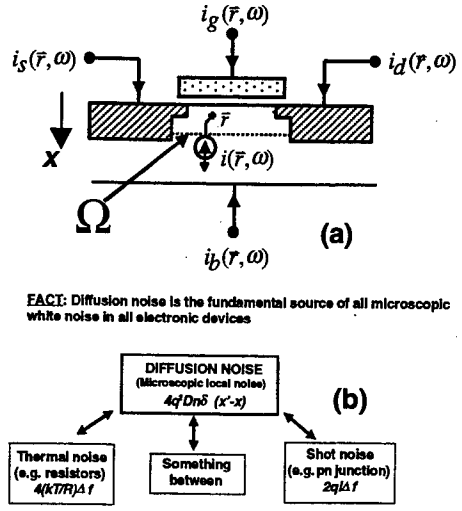


Fig. 1: (a) Illustration of device cross section and noise currents. (b) The noise source used is diffusion noise.

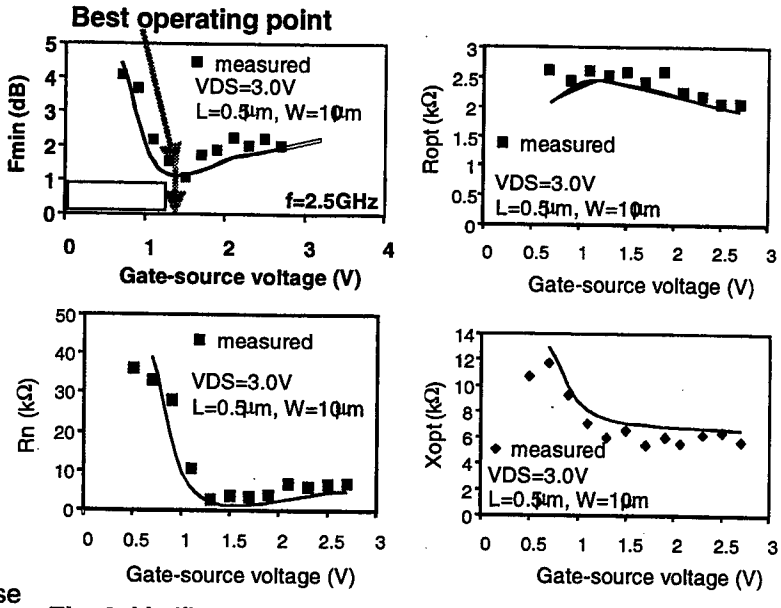


Fig. 2: Verification of the noise simulator. The gate resistance was taken into account as a distributed element. The solid line is simulated results.

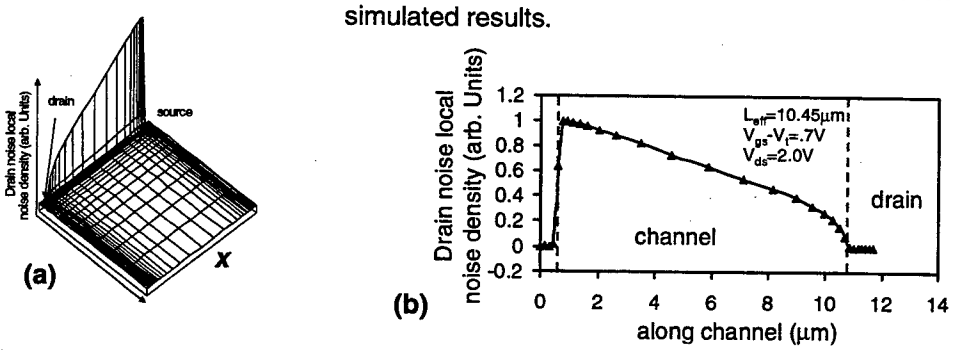


Fig. 3: (a) 3-D plot of the local noise density of a long channel device - local noise density describes how much noise is at a particular point. (b) 2-D cross section at the surface of the channel.

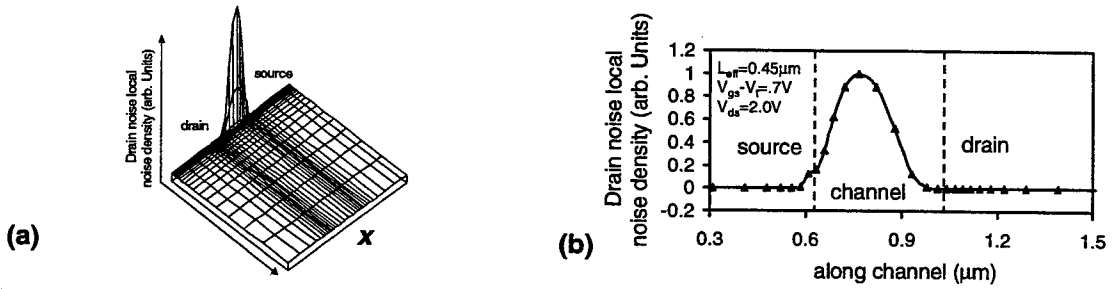


Fig. 4: (a) 3-D plot of the local noise density of a long channel device. (b) 2-D cross section at the surface of the channel. Note that a peak is located near the center, but is skewed to the source end. The local noise density is very different than that of a long channel device and looks very similar to the local noise density in the base of a BJT.

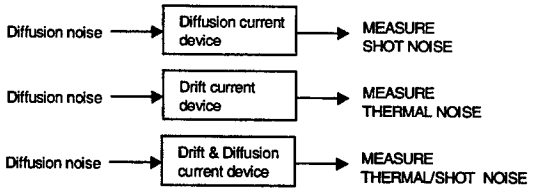


Fig. 5: This figure illustrates that different types of noises are generated depending on the current mechanism in the device.

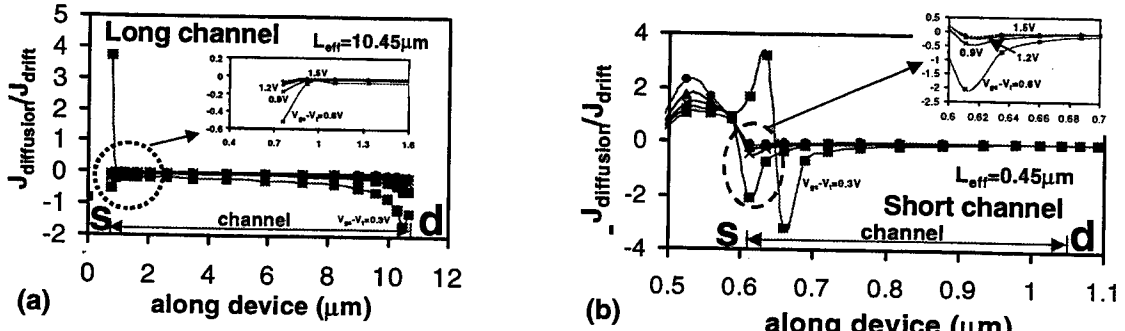


Fig. 6: The ratio of diffusion current to drift current for (a) long channel device and (b) a short channel device. For the long channel device the amount of diffusion current can be ignored since it is very small and only occurs in a small proportion of the channel. However, for a short channel device the diffusion current takes up approximately 20% of the channel length and is very important near the source end.

Long Channel in strong inversion

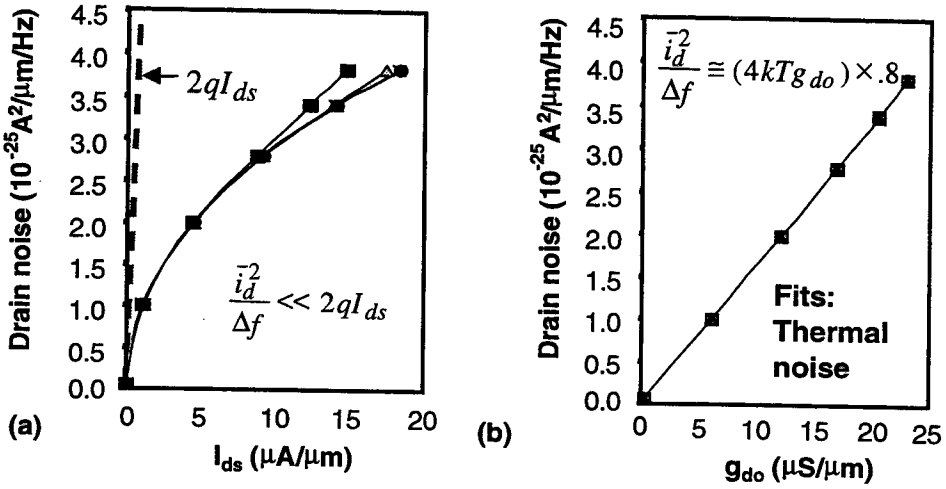


Fig. 7: (a) Drain noise for a long channel device as a function of drain source current (to the left) and the zero drain-source conductance, g_{do} (to the right) for various drain-source voltages ranging from 0.5V to 3.0V. The drain noise current shows the classically behavior of being proportional to g_{do}. The amount of shot noise is determined to be very small in comparison.

Short Channel in strong inversion

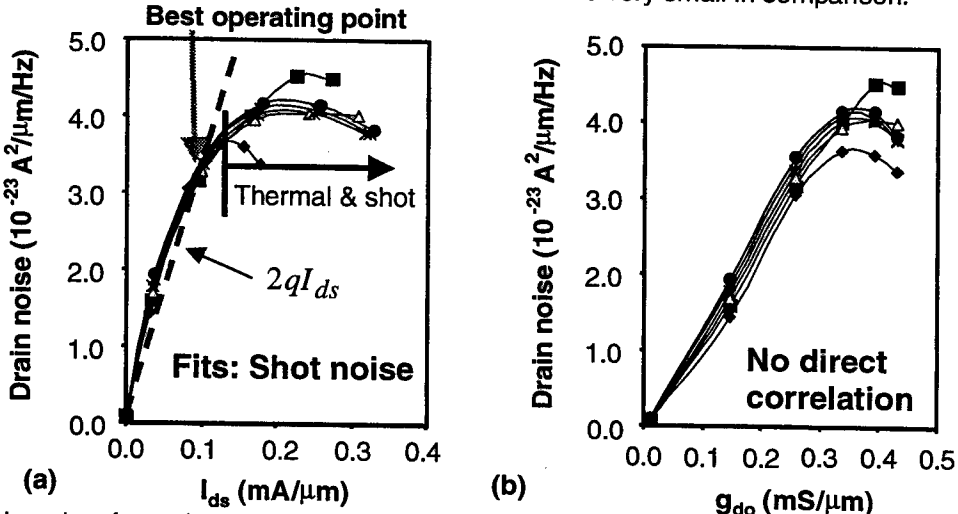


Fig. 8: (a) Drain noise for a short channel device as a function of drain source current (to the left) and the zero drain-source conductance, g_{do} (to the right) for various drain-source voltages ranging from 0.5V to 3.0V. The drain noise current shows a shot noise behavior, but does not show any direct correlation with g_{do}.

A general approach for calculation of thermal noise and excess noise in multi-terminal homogeneous semiconductor resistors

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ABSTRACT

A general approach, based on the characteristic potentials, is developed to calculate both the short-circuit noise currents including thermal noise and excess noise ($1/f$ noise and generation-recombination noise) currents and the open-circuit noise voltages of multi-terminal homogeneous semiconductor resistors with arbitrary geometry under dc bias. A direct experimental verification of the derived formulas has been done by measuring thermal and $1/f$ noise of 3- and 4-terminal homogeneous polycrystalline silicon resistors and carbon film resistors.

INTRODUCTION

Noise in semiconductor devices has been an area of extensive investigation, because it it of crucial importance for analog applications such as amplifiers, solid-state detectors, microwave oscillators, etc [1,2]. To minimize the system noise either by a proper choice of technology or by optimum design, an accurate and general method for noise modeling in semiconductor devices is required.

Recently, shot noise in multi-terminal diffusive mesoscopic conductors has been calculated using "the characteristic potentials" [3,4]. We have found that a similar technique can also be applied to calculate thermal noise and excess noise such as $1/f$ noise and generation-recombination (g-r) noise of multi-terminal homogeneous semiconductor resistors. We show that this approach based on the characteristic potentials provides a direct and straightforward method to calculate short-circuit noise currents and open-circuit noise voltages of multi-terminal homogeneous resistors. An experimental verification of the derived formulas is carried out by measuring thermal noise and $1/f$ noise of 3- and 4-terminal homogeneous polycrystalline silicon resistors and carbon film resistors under various bias conditions.

FORMULAS FOR SHORT-CIRCUIT NOISE CURRENTS

We consider a multi-terminal homogeneous semiconductor resistor of arbitrary 3-dimensional shape (see Fig. 1), which is connected to N perfect metallic contacts of area A_n, n=1,...,N with dc biases $V_1,\ldots,V_N$, applied to the N ohmic contacts. A* in Fig. 1 denotes the free surface. By a homogeneous resistor we mean a constant dc conductivity σ_o throughout the device.

As in Ref. [3], we introduce the characteristic potentials $\phi_n(\mathbf{r})$, n=1,...,N, which satisfy $\nabla\cdot[\sigma_o \nabla\phi_n(\mathbf{r})]=0$ inside the device, $\mathbf{n}\cdot\sigma_o\nabla\phi_n(\mathbf{r})=0$ on A*, and $\phi_n(\mathbf{r})|_{Am}=\delta_{n,m}$. Then with the characteristic potentials and the noise current density equation, given by $\Delta\mathbf{J}(\mathbf{r},t) =\sigma_o\Delta\mathbf{E}(\mathbf{r},t)+\eta_{ex}(\mathbf{r},t)+\eta_{th}(\mathbf{r},t)$ with $\eta_{ex}(\mathbf{r},t)=\Delta\sigma(\mathbf{r},t)\mathbf{E}(\mathbf{r})$ being the excess noise source and $\eta_{th}(\mathbf{r},t)$ being the diffusion noise source [5], we can show that the cross power spectral density $S_{\Delta In,\Delta Ik}(\omega)$ between the short-circuit noise currents $\Delta I_n(t)$ and $\Delta I_k(t)$ becomes

$$S_{\Delta I_n,\Delta I_k}(\omega)=S^{th}_{\Delta I_n,\Delta I_k}(\omega)+S^{1/f}_{\Delta I_n,\Delta I_k}(\omega) \tag{1}$$

$$S^{th}_{\Delta I_n,\Delta I_k}(\omega)=4k_BT\int_V d\mathbf{r}\nabla\phi_n(\mathbf{r})\cdot\sigma_o\nabla\phi_k(\mathbf{r}) \tag{2}$$

$$\begin{aligned}S^{1/f}_{\Delta I_n,\Delta I_k}(\omega)=&\int_V d\mathbf{r}\,\frac{\alpha_n(\mathbf{r})}{fn_o}[\nabla\phi_n\cdot\mathbf{J}_{no}(\mathbf{r})][\nabla\phi_k\cdot\mathbf{J}_{no}(\mathbf{r})]\\&+\int_V d\mathbf{r}\,\frac{\alpha_p(\mathbf{r})}{fp_o}[\nabla\phi_n\cdot\mathbf{J}_{po}(\mathbf{r})][\nabla\phi_k\cdot\mathbf{J}_{po}(\mathbf{r})]\end{aligned} \tag{3}$$

where the superscripts 'th' and '$1/f$' denote thermal noise and $1/f$ noise, respectively, we have used $S\eta_{th}(\mathbf{r},\mathbf{r}',\omega) = 4k_BT\sigma_o\delta(\mathbf{r}-\mathbf{r}')$:I with I being the unit tensor, and $S_{\Delta\sigma}(\mathbf{r},\mathbf{r}',\omega) = \sigma^2_{no}\alpha_n(\mathbf{r})\,\delta(\mathbf{r}-\mathbf{r}')/fn_o + \sigma^2_{po}\,\alpha_p(\mathbf{r})\,\delta(\mathbf{r}-\mathbf{r}')/fp_o$, with α_n and α_p being the Hooge parameters [6], and with n_o, p_o, σ_{no}, and σ_{po} being the dc electron and hole densities and the dc electron and hole conductivities, respectively, and $\mathbf{J}_{no}(\mathbf{r})$ and $\mathbf{J}_{po}(\mathbf{r})$ are the dc electron and hole current densities.

EXPERIMENTS AND DISCUSSION

3-terminal n-type poly-Si film resistors with geometry shown in Fig. 2 were fabricated. A large size poly-Si resistor has been chosen because it can be treated on a macroscopic scale as a homogeneous resistor, so that the derived formulas are applicable to this device. Fig. 3 shows the measured and simulated (with MEDICI) I-V characteristics of the device. During measurements, we confirmed that all noise spectra are of $1/f$ noise type near 10 Hz, and white at 3 kHz. Figs. 4 and 5 show excellent agreement between the measured and theoretical values of thermal noise of $S_{\Delta I1}{}^{th}(\equiv S_{\Delta I1,\,\Delta I1}{}^{th})$, $S_{\Delta I2}{}^{th}(\equiv S_{\Delta I2,\,\Delta I2}{}^{th})$, and $S_{\Delta I1,\,\Delta I2}{}^{th}$ as function of V_1 at V_2=1 V and V_3=0 V. We have also measured thermal noise of a 4-terminal poly-Si resistor, and have verified that the measured data are in good agreement with the theoretical results from Eq. (2).

For an n-type poly-Si with $\alpha_n \approx \alpha_p$, from Eq. (3) and $\mathbf{J}_{no}(\mathbf{r}) \cong \sigma_o \mathbf{E}(\mathbf{r}) = -\sigma_o[V_1 \nabla\phi_1(\mathbf{r}) + V_2 \nabla\phi_2(\mathbf{r})]$, we have the parabolic dependencies of $S_{\Delta I1}{}^{1/f}(\equiv S_{\Delta I1,\,\Delta I1}{}^{1/f})$, $S_{\Delta I2}{}^{1/f}(\equiv S_{\Delta I2,\,\Delta I2}{}^{1/f})$, and $S_{\Delta I1,\,\Delta I2}{}^{1/f}$:

$$S_{\Delta I_1}^{1/f}(\omega) = A_1 V_1^2 + A_2 V_1 V_2 + A_3 V_2^2, \quad (4)$$

$$S_{\Delta I_2}^{1/f}(\omega) = B_1 V_1^2 + B_2 V_1 V_2 + B_3 V_2^2, \quad (5)$$

$$S_{\Delta I_1,\Delta I_2}^{1/f}(\omega) = C_1 V_1^2 + C_2 V_1 V_2 + C_3 V_2^2 \quad (6)$$

where $A_1 = K \int d\mathbf{r}\ \alpha_n(\mathbf{r}) |\nabla\phi_1|^4$, $A_2 = 2C_1 = 2K \int d\mathbf{r}\ \alpha_n(\mathbf{r}) |\nabla\phi_1|^2 (\nabla\phi_1 \cdot \nabla\phi_2)$, $A_3 = B_1 = K \int d\mathbf{r}\ \alpha_n(\mathbf{r}) (\nabla\phi_1 \cdot \nabla\phi_2)^2$, $B_2 = 2C_3 = 2K \int d\mathbf{r}\ \alpha_n(\mathbf{r}) |\nabla\phi_2|^2 (\nabla\phi_1 \cdot \nabla\phi_2)$, $B_3 = K \int d\mathbf{r}\ \alpha_n(\mathbf{r}) |\nabla\phi_2|^4$, and $C_2 = K \int d\mathbf{r}\ \alpha_n(\mathbf{r}) \{|\nabla\phi_1|^2 |\nabla\phi_2|^2 + (\nabla\phi_1 \cdot \nabla\phi_2)^2\}$ with $K \equiv \sigma^2_{no}/fn_o$. Fig. 6 shows $S_{\Delta I1}{}^{1/f}$ vs. V_1 at V_2=0, 1 V. With a constant α_n=3.8 throughout the device, theoretical and experimental results for $1/f$ noise show excellent agreement. Figs. 7 and 8 show $S_{\Delta I2}{}^{1/f}$ vs. V_2 at V_1=0, 1 V, and $S_{\Delta I1,\,\Delta I2}{}^{1/f}$ vs. V_2 at V_1=1 V, respectively.

For further verification of the derived formulas, we have also fabricated a 3-terminal carbon composition resistor whose shape is similar to that of the 3-terminal poly-Si resistor but has non-uniform $\alpha_n(\mathbf{r})$. Figs. 9 and 10 show the experimental and best-fit parabolas of $S_{\Delta I1}{}^{1/f}$, $S_{\Delta I2}{}^{1/f}$ at V_2=0, 1 V, and $S_{\Delta I1,\,\Delta I2}{}^{1/f}$ at V_2=1 V, vs. V_1, respectively. And Figs. 11 and 12 show the measured and best-fit parabolas of $S_{\Delta I1}{}^{1/f}$, $S_{\Delta I2}{}^{1/f}$, at V_1=0, 1 V, and $S_{\Delta I1,\,\Delta I2}{}^{1/f}$ at V_1=1 V vs. V_2, respectively. The coefficients of the best-fit parabolas have shown excellent agreements with Eq. (4) at various bias conditions (Compare A's and B's in Figs. 9 and 11, and also check $A_2 \cong 2C_1$, $A_3 \cong B_1$, and $B_2 \cong 2C_3$.).

CONCLUSIONS

We have derived the general formulas of the short-circuit thermal noise and excess noise currents in multi-terminal homogeneous semiconductor resistors using the noise current density equation and the characteristic potentials. The derived formulas give the information on the locations of the thermal noise and excess noise sources, which affect most the terminal thermal noise and excess noise currents of the multi-terminal homogeneous semiconductor resistors. Experimental results on thermal noise and $1/f$ noise of 3- and 4-terminal homogeneous poly-Si resistors and 3-terminal carbon film resistors have proven the validity of the derived formulas. We expect that a similar approach based on the characteristic potentials can be developed for inhomogeneous semiconductor devices.

ACKNOWLEGMENTS

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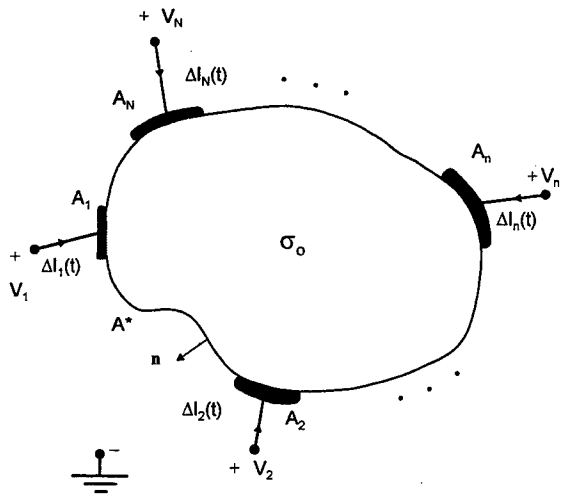


Fig. 1 The arbitrarily shaped homogeneous N-terminal device. A_m is the m-th electrode, A* is the free surface, **n** is the outward normal vector of the boundary surface, and σ_o is the homogeneous dc conductivity.

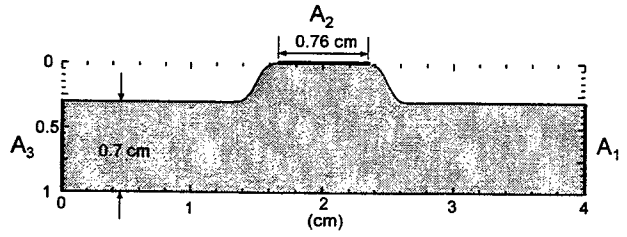


Fig. 2 The geometry of 3-terminal n-type polycrystalline silicon resistor under test: length is 4 cm, total width is 1 cm, thickness is 5100 Å, the width of electrodes 1 and 3 is 0.7 cm, and the width of electrode 2 is 0.76 cm.

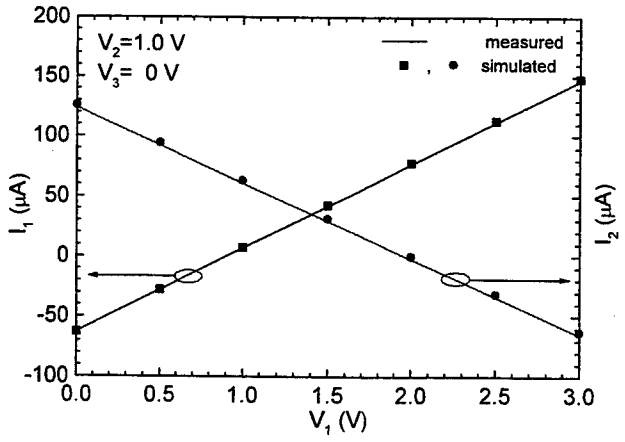


Fig. 3 The measured and simulated (with MEDICI) I-V characteristics for the 3-terminal poly-Si resistor with the Hall-measured μ_{no}=14.0 cm^2/Vs and n_o=1.8×10^{18} cm^{-3} at V_2 = 1 V, and V_3 = 0 V.

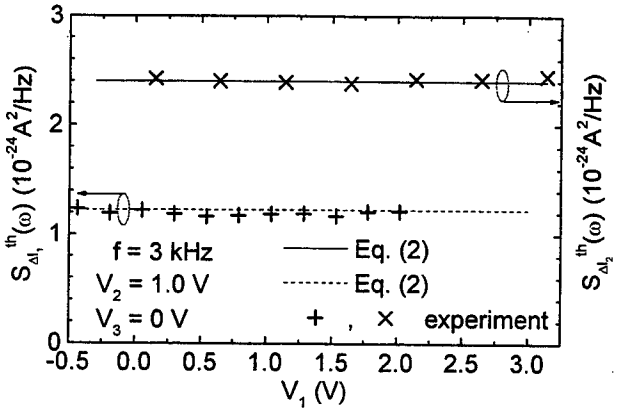


Fig. 4 The measured and theoretical values of thermal noise, $S_{\Delta I1}^{th}(\omega)$ and $S_{\Delta I2}^{th}(\omega)$, of the poly-Si resistor when V_2 = 1 V, and V_3 = 0 V at f = 3 kHz.

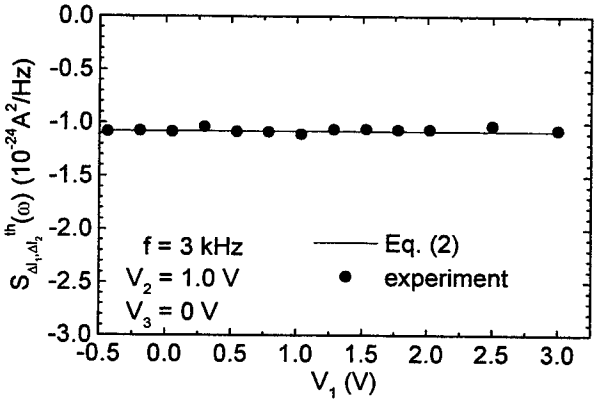


Fig. 5 The measured and theoretical values of thermal noise, $S_{\Delta I1,\,\Delta I2}^{th}(\omega)$, of the poly-Si resistor when V_2 = 1 V, and V_3 = 0 V at f = 3 kHz.

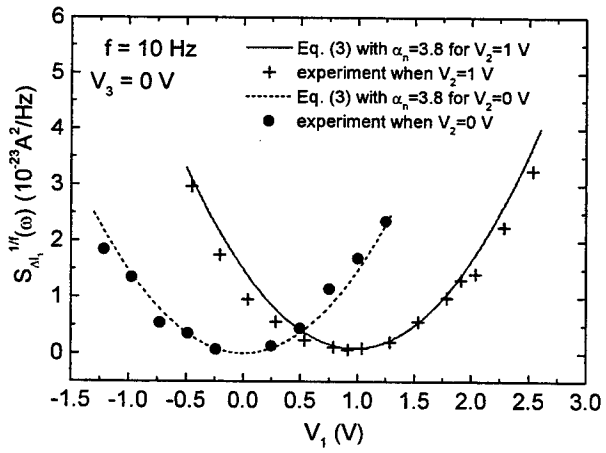


Fig. 6 The measured and theoretical values of 1/*f* noise, $S_{\Delta I1}^{1/f}(\omega)$, of the poly-Si resistor vs. V_1 when V_2 = 0 V, V_3 = 0 V, and V_2 = 1 V, V_3 = 0 V, respectively at f = 10 Hz .

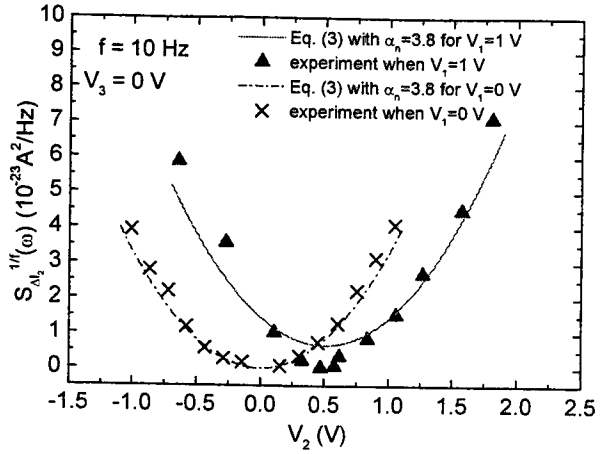


Fig. 7 The measured and theoretical values of $1/f$ noise, $S_{\Delta I2}^{1/f}(\omega)$, of the poly-Si resistor vs. V_2 when $V_1 = 0$ V, $V_3 = 0$ V, and $V_1 = 1$ V, $V_3 = 0$ V, respectively at f = 10 Hz.

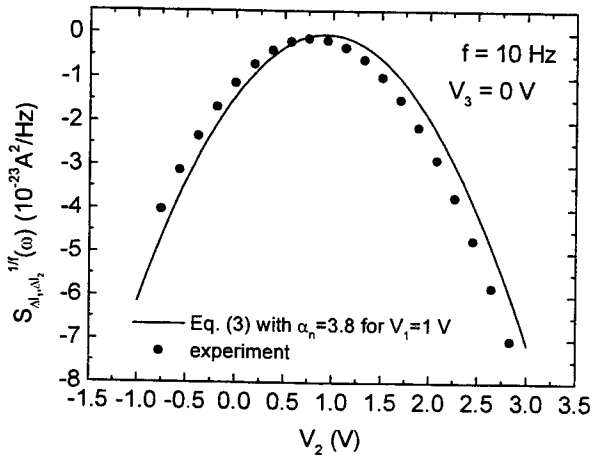


Fig. 8 The measured and theoretical values of $1/f$ noise, $S_{\Delta I1,\,\Delta I2}^{1/f}(\omega)$, of the poly-Si resistor vs. V_2 when $V_1 = 1$ V, $V_3 = 0$ V at f = 10 Hz.

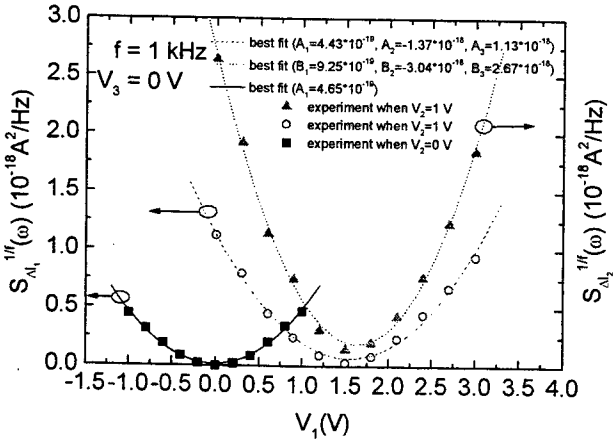


Fig. 9 The experiments and best-fit parabolas of $S_{\Delta I1}^{1/f}(\omega)$ and $S_{\Delta I2}^{1/f}(\omega)$ of the carbon composition resistor vs. V_1 when $V_2 = 0$ V, and 1 V with V_3 grounded at f = 1 kHz.

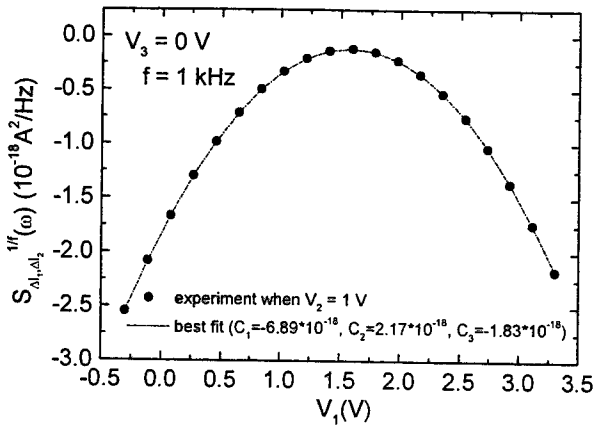


Fig. 10 The experiment and best-fit parabola of $S_{\Delta I1,\,\Delta I2}^{1/f}(\omega)$ of the carbon composition resistor vs. V_1 when $V_2 = 1$ V, $V_3 = 0$ V at f = 1 kHz.

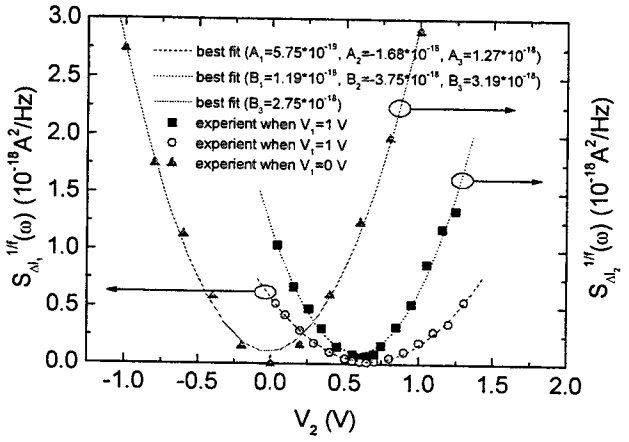


Fig. 11 The experiments and best-fit parabolas of $S_{\Delta I1}^{1/f}(\omega)$ and $S_{\Delta I2}^{1/f}(\omega)$ of the carbon resistor vs. V_2 when $V_1 = 0$ V, and 1 V, with V_3 grounded at f = 1 kHz.

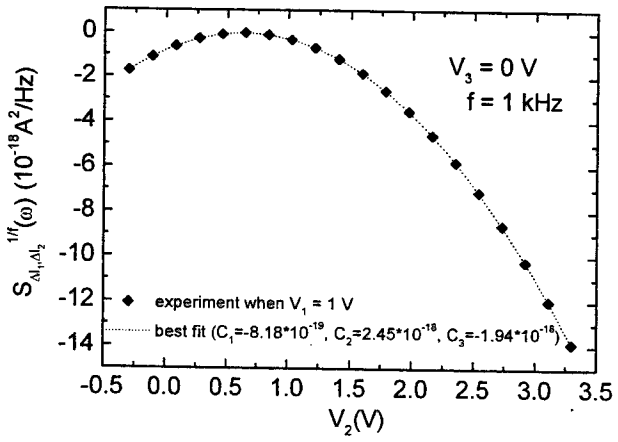


Fig. 12 The experiment and best-fit parabola of $S_{\Delta I1,\,\Delta I2}^{1/f}(\omega)$ of the carbon composition resistor vs. V_2 when $V_1 = 1$ V, $V_3 = 0$ V at f = 1 kHz.

Noise in the Drift-Diffusion Framework

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1 Introduction

The noise characteristics of semiconductor devices is a critical criterion in current circuit design. This is especially important in wireless applications where long battery life is placing an even greater demand on signal power. Increasingly, circuit engineers are being forced to design for lower signal levels and system noise which is inherent in all electronic devices. In this paper, a semiconductor device noise model in the framework of drift-diffusion is presented. The random evolution of electron and hole trajectories within a device is described by stochastic differential equations in which interband transitions are modeled by white noise perturbations while intraband transitions are modeled by Poisson type jump processes. As a result the model is able to account for the noise due to the generation and recombination of carriers, along with the noise associated with scattering inside of the bands.

Employing stochastic differential equation (SDE) theory, it is shown that the key computations for the resulting terminal current noise characteristics are reduced to the solution of the well-known drift-diffusion type equations with special initial and boundary conditions. As a result this approach broadens the scope of device analysis which can be performed with simulators based on the drift-diffusion model. The approach is general and can be applied to arbitrary semiconductor devices. It is demonstrated that real device calculations can be performed by simple modifications to classical drift-diffusion type device simulators.

2 Electron Motion Described be SDE's

In previous work [1] we showed that the current continuity equations utilized in the drift-diffusion model are identical in form to the forward Kolmogorov equation of SDE theory. As a result, it was demonstrated that in the drift-diffusion framework the electron position, $\vec{x}$, follows a trajectory governed by the following SDE:

$$d\vec{\mathbf{x}}(t) = -\mu_n \vec{E}(\vec{\mathbf{x}}(t))dt + D_n d\vec{\mathbf{W}}(t), \tag{1}$$

where μ_n and D_n are the electron mobility and diffusivity, respectively; $\vec{E}$ the electric field; and $\vec{\mathbf{W}}(t)$ is a zero mean Wiener process. This representation of the electron motion is quite informative at the physical level. According to this representation the electron follows a random trajectory whose average position drifts proportionally to the local value of the electric field. It turns out that such a process is Markov and is usually characterized by means of a transition density function, $\rho(\vec{x}, t|\vec{x}', t')$, which satisfies the following Kolmogorov equation:

$$\frac{\partial \rho}{\partial t}(\vec{x}, t|\vec{x}', t') = \nabla \cdot \Big(\mu_n \rho(\vec{x}, t|\vec{x}', t')\vec{E}(\vec{x}, t) + D_n \nabla \rho(\vec{x}, t|\vec{x}', t')\Big). \tag{2}$$

In the drift-diffusion model, electrons and holes not only drift within the conduction and valence bands, respectively, but also make interband transition. Such processes are generally characterized in terms of the Shockley-Read-Hall generation recombination model. As a result, in the drift-diffusion framework the state of an electron or hole is completely specified by its $\vec{x}$, and band index m. The value of the band index specifies whether an electron or hole is in the valence or conduction bands, or in a trap. Such a process can be characterized by two coupled SDE's which, in the case of electrons read as follows:

$$d\vec{\mathbf{x}}(t) = -\mu_n \vec{E}(\vec{\mathbf{x}}(t), \mathbf{m}(t))dt + D_n d\vec{\mathbf{W}}(t), \tag{3}$$

$$d\mathbf{m}(t) = \sum_i \Delta m_i \delta(t - t_i). \tag{4}$$

Here, $\mathbf{m}(t)$ corresponds to a process driven by the derivative of a Poisson type jump process, and Δm_i represents the intensity of the i^{th} interband transition. Again, these equations define a Markov process which is completely characterized by its transition probability density function, $\rho(\vec{x}, m, t|\vec{x}', m', t')$. According to SDE theory, such a transition probability satisfies the associated

Kolmogorov-Feller equations. For electrons in the conduction band and trap level, these equations read as follow:

$$\frac{\partial \rho}{\partial \tau}(\vec{x}, c, \tau | \vec{x}', \vec{m}') = \nabla \cdot \left(\mu_n \rho \vec{E}(\vec{x}) + D_n \nabla \rho \right) + \rho(\vec{x}, T, \tau | \vec{x}', \vec{m}') e_n - \rho(\vec{x}, c, \tau | \vec{x}', \vec{m}') c_n p_T(\vec{x}) \quad (5)$$

$$\frac{\partial \rho}{\partial \tau}(\vec{x}, T, \tau | \vec{x}', \vec{m}') = \rho(\vec{x}, c, \tau | \vec{x}', m') p_T(\vec{x}) c_n - \rho(\vec{x}, T, \tau | \vec{x}', \vec{m}')(e_n + c_p p(\vec{x})) \quad (6)$$

Here c and T have been used to designate the values of the band index, m, in the conduction band and trap, respectively. c_n, e_n and c_p are Shockley-Read-Hall generation recombination parameters. Also, $\tau = t - t'$ and since t' can be arbitrarily chosen for the stationary regime, it has not been included in the above equations. These two equations are precisely the electron current continuity and electron trap dynamic equations of the drift-diffusion model. This establishes that in the drift-diffusion framework the underlying microscopic motion of electrons is completely characterized by equations (3) and (4).

3 Terminal Current Spectral Density Computation

Ramo's theorem [2] allows to relate the induced current at the device terminals by the motion of an electron or hole inside of the device. By application of Green's theorem it is also possible to relate induced charge at a particular device terminal to the position of the electrons or holes within the device. Since the terminal current is the time derivative of the induced charge, once the noise properties of the induced charge are known, it is possible to asses the characteristics of the current fluctuations. More precisely, once the spectral density of the charge has been computed, the calculation of the current spectral density follows.

The autocovariance of any random process can be found from the transition probability density function of such a random process. Consequently, since the transition probability function of the process in question satisfies equations (5) and (6), all the information required to compute the induced charge autocovariance function is embedded in these two equations. Following an approach similar to the one described in [3], it is not difficult to show that the autocovariance function of the charge induced by the motion of the electrons inside a device is reduced to the solution of equations (5) and (6) with special initial conditions.

4 Summary

A new approach is presented to compute the spectral density of terminal current noise within the drift-diffusion framework. The random evolution of electron and hole trajectories within the device is described by stochastic differential equations in which the intraband scattering is modeled by white noise stocastic dynamics while interband transitions are modeled by Poisson type jump processes. As a result the model is able to account for the noise due the generation and recombination of carriers, along with the noise associated with their motion within the bands.

It also is shown how the key computations of the autocovariance function are reduced to a special initial value problem of the drift-diffusion equations. In this sense our research provides the means to broaden the scope of device analysis which can be performed with currently available device simulators. The distinct feature of this approach compared to other microscopic models is that the approach directly connects noise characteristics with the underlying stochastic dynamics without requiring the ad hoc addition of "Langevin sources" which are generally introduced into the drift-diffusion equations to account for random fluctuation.

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Simulation On the Influence of Structure on the Hot-Carrier-Effect Immunity for Deep-Sub-Micron Grooved gate MOSFET

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I. INTRODUCTION

To achieve higher speeds and packing densities in VLSI, the size of MOSFET has been continuously scaled down, the hot-carrier degradation becomes the stringent limitation to the reliability of deep-sub-micron devices and of VLSI packing densities [1]. The evaluation and modeling for hot-carrier effect in MOSFET has become one of the most important question which should be faced. Recent studies on new structure and fabrication process attempt to overcome the drawbacks faced by conventional planar MOSFET [2], such as short-channel-effect and hot-carrier-effects. Grooved gate MOSFET is proposed as a promising device for suppressing short channel effect and hot carrier effect in deep sub-micron and sub-0.1-micron regime, because structures with shallow junctions or even negative junctions can be fabricated without any increase in series resistance. There for, grooved gate MOSFET are good candidates for use in the sub-0.1-micron regime. However, there has been no discussion so far on how the dependence of hot-carrier-effect immunity of grooved gate MOSFET on its geometric structure can be in deep-sub-micron and sub-0.1-micron range.

In this paper, the influence of grooved gate MOSFET's structure on hot carrier effect is investigated using two-dimensional device simulator MEDICI [3], and their simulated performance is compared with that of conventional planar MOSFET's . MEDICI solves the hydro dynamics energy transport equations, which accurately predicts the electron heating and related phenomena such as velocity overshoot. The examined structure parameters include negative junction depth, grooved-gate corner and channel effective length. Simulation results prove that grooved-gate device can deeply suppress hot carrier effect even in deep-sub micron region. The studies also indicate that hot carrier effect is strongly influenced by the concave corner and channel length for grooved gate MOSFET.

II. DEVICE STRUCTURE AND SIMULATION TOOLS

The Simulated device structures are described by the schematic cross section in Fig.1. For both devices, the effective channel length L_{eff} corresponds here to the metallurgical channel length, taken along the gate oxide. In the simulated grooved gate MOSFET's, the source/drain junction depths are 0.02μm, 0.01μm and 0.01μm above the bottom of the groove (X_j=*-0.02μm, -0.01μm, 0.0μm*) respectively. The bottom concave corner are 30°、45°、60° respectively. The gate oxides are 4nm thick, which limits tunneling through the oxide. The effective channel lengths are 0.13μm, 0.18μm, 0.35μm

and 0.50μm respectively. In all simulated devices, the fixed interface state intensities are $10^{10}cm^{-2}$, the substrate doping concentrations are $5.0\times10^{16}cm^{-3}$, The maximum doping concentrations at the surface are $10^{20}cm^{-3}$ for the source/drain region and $10^{17}cm^{-3}$ for the channel, the groove depths are 0.1μm, the drain bias voltage are 2.0V.

In the simulation for deep-sub-micron devices, especially for the channel length is comparative to the carriers mean impact free path, the well-known drift-diffusion method is not adequate for it ignores the non-local transport of carriers and carriers heating, while the carriers are considered in non-equilibrium with semiconductor crystal and local electrical field in deep sub-micron devices. Now widely used tool for simulation high-bias and small size devices are hydrodynamics energy transport and Monte Carlo method. In our simulation, we adopted the hydrodynamic energy transport model, which includes the continuity equations, momentum transport equations, energy balance equations of carriers and Poisson equation, and can model the non-local transport phenomenon, is more accurate than drift-diffusion method. During the study on gate current, we adopted lucky electron gate current model [4].

III. RESULTS AND DISCUSSION

The hot carrier effect is sensitive to the electrical field in channel, gate current and substrate current in MOSFET. The substrate current can denote the number of generated hot carrier for it is directly related to impact ionization probability. So it is considered as a rule for hot carrier reliability during reality measurement.

1. The influence of Channel Length on hot carrier effect immunity

In this section, the simulated MOSFET's junction depth are 0.08μm, the grooved-gate corner are 45^0. Fig.2 and Fig.3 show the substrate currents versus gate voltage for grooved gate MOSFET and conventional planar MOSFET with different channel length respectively. It shows that the substrate current of grooved gate MOSFET's is far lower than that of conventional planar. So the hot carrier effect in grooved gate MOSFET is suppressed compared to planar MOSFET's. This is because the "corner effect" [5]: one potential barrier is formed at each groove corner in grooved gate MOSFET's, and carriers have to surmount them and change moving direction during their movement from source to drain.

It is also clearly observed that the substrate current is increased sharply with the reduction of channel length for both type devices. That demenstrates the hot carrier effect become intense as the channel length shorten, for the parallel electrical field along channel is strengthened. However, compare Fig.2 with Fig.3, it is obvious that the increase extent of the magnitude of hot carrier phenomenon in planar device is larger than that in grooved gate devices. So we can say that in short channel case, compared to planar MOSFET, grooved gate MOSFET have good performance to suppress hot carrier effect. It is also observed that the maximum number of generated hot carrier occurs at the same gate bias voltage (about equals to 1/2 drain voltage) in grooved gate MOSFET with different channel length. However, for planar device, this gate voltage is increase with the reduction of channel length (from 1/4 to 1/2 of drain voltage).

2. The influence of Concave Corner on hot carrier effect immunity

Fig.4 is the comparison of substrate current for grooved gate MODFET's with different concave corner respectively. The simulated device effective channel length are 0.13μm, junction depth are 0.08μm. The studies manifest that the substrate current is decreased along the increase of concave corner, so do the number of hot carrier generated by impact ionization. It is distinctly the concave corner can influence hot carrier effect remarkably. This also can be explained by "corner effect". The potential barrier at groove corner is elevated while the concave corner increases, carriers lose more energy when they surmount the potential barrier and their velocity are lower.

3. The influence of negative junction depth on hot carrier effect immunity

Fig.5 gives the comparison of substrate current (impact ionized current) as function of gate voltage for grooved gate and planar MOSFET with different junction depth. Fig.5(a), (b) and (c) are situations for deep negative (-0.02μm), shallow negative (-0.01μm) and even junction (zero negative junction) respectively. The effective channel length are 0.13μm, the concave corner are 45° for simulated devices. Compared the maximum substrate current of grooved gate MOSFET and of conventional planar MOSFET, it is the percent of 29.5% of planar device for grooved gate MOSFET with deep negative, 26.3% for shallow negative and 83.1% for zero negative junction. So it is apparent that the amount of hot carrier decreases with the negative junction deepen in grooved gate MOSFET. This is because the more the negative junction deep, the more the "corner effect" prominent. It also proves that with the groove depth increase, the hot carrier effect immunity becomes better.

IV. CONCLUSION

The influence of some structure parameters on hot-carrier-effect-free is investigated and compared with that of conventional planar device using 2-dimensional device simulator MEDICI. The examined parameters include effective channel length, negative junction depth and grooved-gate corner. The simulation results verify that compared to planar MOSFET, grooved gate MOSFET can suppress hot carrier effect deeply under short channel stations, and its capability of hot carrier effect immunity is enhanced as the concave corner and negative junction depth increase. All these phenomena result from the particular structure of grooved gate MOSFET, and can be explained by the "corner effect". So we can predict the good behavior and promising application future in deep sub-micron and sub-0.1μm for grooved gate MOSFET.

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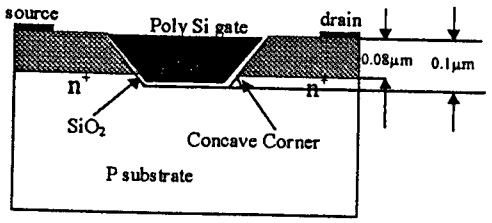
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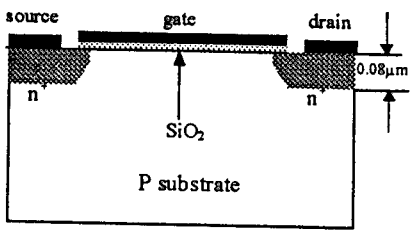
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(a) Schematic cross section of grooved gate NMOSFET (b) Schematic cross section of planar NMOSFET

Fig.1 Schematic cross section of grooved gate and planar NMOSFET

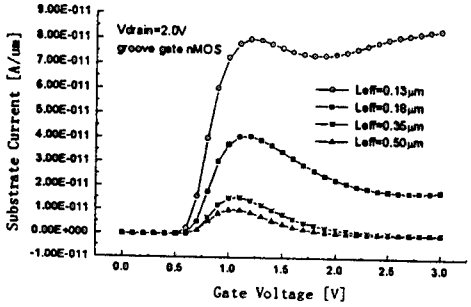


Fig.2 Substrate current for grooved gate MOSFET with different channel length

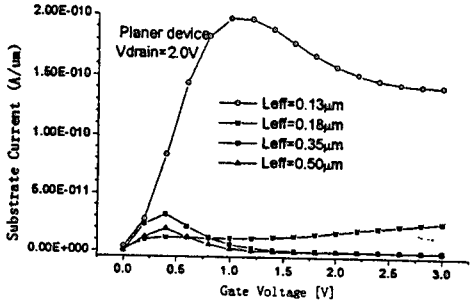


Fig.3 Substrate current for conventional planar MOSFET with different channel length

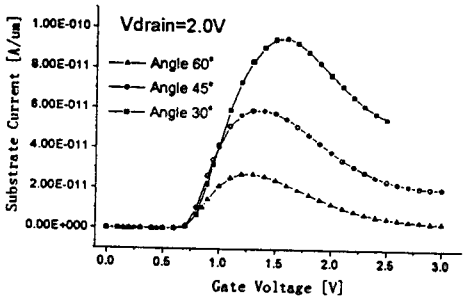


Fig.4 The substrate current for grooved gate MOSFET with different concave corner

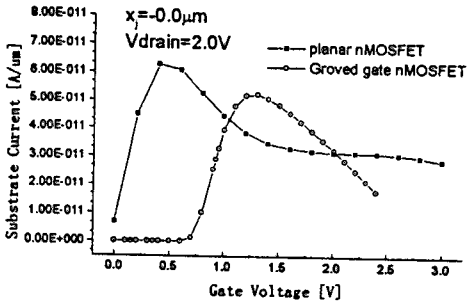
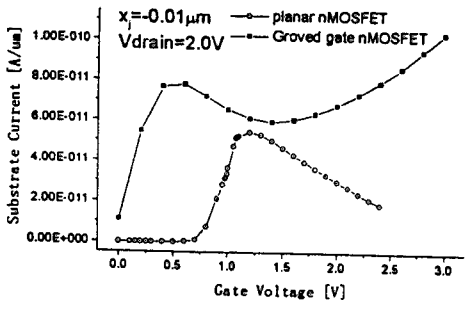
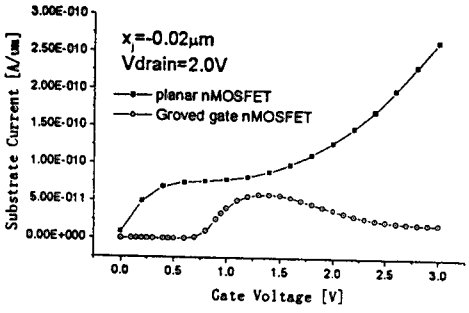


Fig.5 (a) Zero negative junction device





(b) Shallow negative junction device (c) Deep negative junction device

Fig.5 The substrate current for grooved gate and planar device with different negative junction depth

Exponentially Tapered Transmission Lines for High Speed Detection Circuits using Time-Domain Reflectometry

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Abstract

An approach is presented for modelling exponential transmission lines in high-speed digital interconnects with the use of time-domain reflectometry (TDR). The approach is far better in terms of accuracy since it shows that exact shape of line can be important if reflections are to be kept to a minimum. Exponential transmission lines with 50-ohms input impedance on one side and ~10-ohms on the other side, and has a large bandwidth and low reflection coefficient. Experimental results are presented to illustrate the validity of this approach.

Introduction

The transmission lines and their associated interconnections play an important role at virtually all aspects of today's communication technology involving applications of integrated circuits and printed circuit boards. In the world of high-speed digital design, clock rates are increasing at dramatic pace. With the design of fast devices having switching times in the picosecond range, transmitting data at gigabit per second are creating signal integrity problems for printed circuit board structures such as backplanes microstrip traces and interconnects. In recent years, modelling and simulation tools has become major focus interest into predicting structure performance, more test and measurements are needed to verify the actual response to fast edge speeds [4]. The time-domain reflectometry (TDR) is one of the tools used most frequently to detect discontinuities and relate physical interconnect structures to such parameters as characteristic impedance, reflection coefficient, propagation velocity and edge effects of signal lines including both RF and optics transmission paths. The intent of this paper is to show how to recognize and avoid some common problems associated with high-speed digital design.

Most of the conventional TDR applications thus far have been limited to the detection of discrete discontinuities of transmission lines. Conventional TDR techniques ignored the processes (such as reflection) of exponential transmission lines (ETL).

To extend the application of TDR technique to the construction of exponential transmission line we investigate a time domain simulation of pulse through a tapered line, where time domain approach is used to formulate the propagation equations on a loss-less line with non-linear behaviour at the termination.

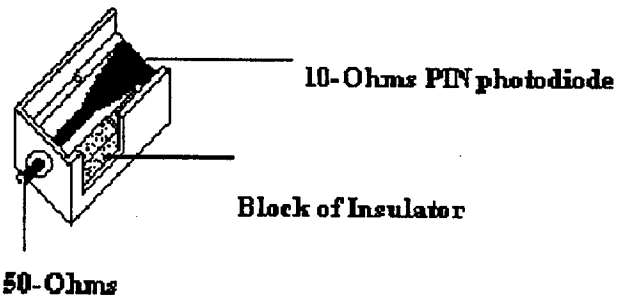


Figure 1.High speed device using ETL

This work involves the design and modelling of a high-speed signal detection circuit, based on loss-less tapered transmission lines. The detection circuit utilising tapered lines involves the use of components having low resistance typically in the range of 3 to 10 ohms. The most common type of semiconductor used for these devices consists of the III-IV compounds, i.e. GaAs and related compounds. Semiconductor lasers diodes and PIN photodiodes are useful in many circuit applications in microwave circuits because of their low cost, very small size, lightweight, high speed, time and space coherence. Laser diodes and high-speed photodiodes are normally coupled to 10-ohms circuit [1]. In this work exponential transmission line is used the input resistance of such components to 50 Ohms, allowing considerable improvement of the temporal response high speed photodiodes as compared with conventional coupling (see Figure 1.). The smoothness of the two set of ETL is investigated. Several experiments are carried out to verify the theoretical result concerning the construction of ETL; the result show that this technique produces better results than conventional methods widely employed.

Time Domain Analysis

The transient simulation of high-speed analog and digital integrated circuits require the analysis of frequency-dependent transmission lines. The frequency-dependent behaviours of transmission lines such as losses and dispersion are accurately represented in the frequency domain, while the determination of transmission line delays and noise require the time domain simulation. Linear and non-linear subsystems can be modelled using time-domain measurement data and the entire system consisting of the individual subsystems can then be very efficiently analysed [3]. The model of the subsystems use linear or non-linear time-domain transfer functions, not conventional equivalent circuits. This approach gives computational efficient non-linear models that can be identified from time-domain measurement, where the result is much reduced effort and volume of measured data compared to a frequency domain measurements. In the frequency domain large number of measurements have to be carried to determine the all four scattering parameters as a function of frequency and at number of power levels. In the time domain the response is real function and usually much fewer power levels and time points are required to model non-linear systems[6]. The analysis of ETL characterized by scattering parameters is done using the following incident and reflected voltage wave definitions:

$$A_i(j\omega) = \frac{1}{2}\left[\underline{V_i}(j\omega) + Z_{ref,1} I_i(j\omega)\right]$$
$$B_i(j\omega) = \frac{1}{2}\left[\underline{V_i}(j\omega) - Z_{ref,2} I_i(j\omega)\right] \qquad (1)$$

The impedance matrix Z_{ref} describes the reference impedance network shown in figure 1 and is used to describe the scattering parameters in the calculation or measurements of the S parameters. Exponential transmission line can be described as a set of scattering parameters that relate two reflected waves and two incident waves:

$$B_1(s) = S_{11}(s)A_1(s) + S_{12}(s)A_2(s)$$
$$B_2(s) = S_{21}(s)A_1(s) + S_{22}(s)A_2(s) \qquad (2)$$

Where $B_i(s)$ and $A_i(s)$ are the incident reflected waves for ports 1 and 2 and S_{ij} (i,j = 1,2)are the scattering parameters, and s represents the frequency.

To evaluate the S parameters we consider a lossless, ETL having characteristic impedance as follows:

$$Z(x) = Z_{ref,1}e^{\gamma x} \qquad (3)$$

Where:

$$\gamma = [\ln(Z_{ref,2}/Z_{ref,1})] / l$$

Where l is length of the line, x is a space variable, $Z_{ref,1}$ and $Z_{ref,2}$ are the characteristic impedance at the source and load of the ETL respectively, used as the reference impedance matching in determining the S parameters of ETL. The computation of the S parameters in the time-domain, which completely is described [3] and will not be discussed here. For clarification it should be noted that the method presented in [3] can handle complex normalizing impedance matrices, yielding generalized S parameters in terms of source and load impedance. In order to be able to analyze circuits with high speed, the frequency domain S parameters must be computed accurately over a very wide frequency band. The formulation used in [3] can accurately compute the S parameters over such a bandwidth because the frequency variation of the currents and voltages on the lines is a built into the solution approach.

Using the above equations and scattering functions signal flow graph to represent the interconnection of the subsystem, the whole system can be simulated in time domain explicitly and efficiently without

the need to use iteration to solve non-linear equation. Once computed, the S parameters are the inverse Fourier transformed to obtain the time domain s parameters. The time domain version of the Eq. (2) is the written as

$$b_1(t) = s_{11}(t)*a_1(t) + s_{12}(t)*a_2(t)$$
$$b_2(t) = s_{21}(t)*a_1(t) + s_{22}(t)*a_2(t) \quad (4)$$

Where t is the time, * denotes a convolution in the time domain, $a_1(t)$, $b_1(t)$, $a_2(t)$, $b_2(t)$ are incident and reflected waves for port 1 and port 2, s is time domain scattering matrices.

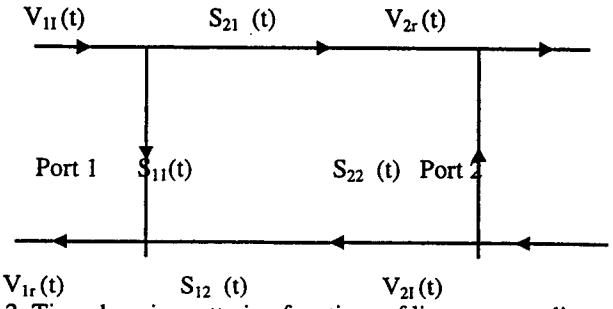


Figure 2: Time domain scattering functions of linear or non-linear two ports.

The voltages at ports 1 and 2 are the summation of the incident and reflected waves:

$$V_1(t)=a_1(t)+b_1(t) \quad (5)$$
$$V_2(t)=a_2(t)+b_2(t) \quad (6)$$

And the expressions for the currents are:

$$I_1=\frac{a_1}{Z_{ref}}-\frac{b_1}{Z_{ref}} \quad (7)$$

$$I_2=\frac{a_2}{Z_{ref}}-\frac{b_2}{Z_{ref}} \quad (8)$$

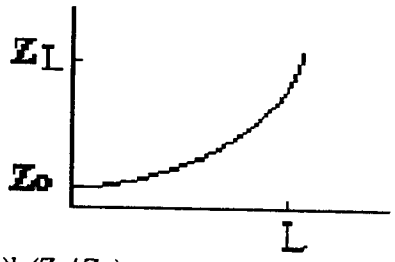
The time-domain reflected wave on a exponential line is the result of a progressive process in which a reflected wave is the summation of all signal components that suffer from internal multiple reflection-transmission processes and arrive at the input port at time t. The step response of a reflected wave of a exponential line is needed to complete the process. However, it also possible to obtain indirectly from the Fourier transformation of its corresponding frequency response of the signal line if sufficient bandwidth is included. Scattering parameters are employed for model formulation since they are measurable at high frequency, and because a scattering impulse response is typically shorter in duration than its admittance or impedance counterpart. This makes scattering parameters preferable as a tool for describing and working with a nearly lossless network in the time domain, since equivalent information is contained in fewer data points.

ETL Formulation

Exponential tapered lines represent a practical effective solution to impedance matching problems above 3GHz. They are about same length as stepped transform, but their upper frequency limit is as high as their upper frequency limit as high as the medium used for their construction. The reflections from the tapered line decrease rapidly with frequency, and are more manageable than those from stepped transforms. Discontinuities don't exist, since the impedance change is continuous. Let's consider synthesis of an exponential transmission line, going from 50-ohms to a 20-ohms in a stripline TEM medium. If design constrains are such that maximum reflection are such that maximum reflection coefficient is 0.1 with SWR= 1.22:1 and the lowest frequency of interest is 2.0GHz (as shown in Figure 3.), then length L can be calculated in the following manner. Since the reflection coefficient magnitude is at maximum at the lowest frequency of interest, all calculations will be done at 2GHz. Substituting 2 for Z_L in Equation where:

$$Z(x)=Z_0e^{\alpha x}, \text{for } 0<x<L \quad (9)$$

as indicated in fig.2. At x = 0, Z(0)= Z_0, as desired. At z = L , we wish to have Z(L) = $Z_L = Z_0 e^{\alpha L}$, The domain of Z(x) is from 0 to L where the units of L are arbitrary, as long as x is in the same units. Since at the point x, the end of the transform Z(L) must equal Z_L, which determines the constant α as :



$$\alpha = (1/L)\ln(Z_L / Z_0) \qquad (10)$$

Figure 3. Exponential transmission line continuously change impedance, thus avoiding line discontinuities

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_{eff}}}$$

Where Γ is the maximum reflection coefficient, Z_L is the normalised value of the load impedance to be matched, and λ_g is the guide wavelength at the lowest frequency of interest. The time domain S parameters of ETL section were computed with the use of the method [5] at frequency of interest 2GHz. Its length is calculated by substituting these values, Z_S =50 Ω, Z_L =20 Ω, maximum reflection coefficient of 0.1 at 2 GHz and effective dielectric constant of 9.8, in equation (11) and (12). Giving as, L=3.5cm. The significance of this simulated line length is that, it is the required length that will give ETL low lossless properties for the above conditions. For only a fractional increase in reflections, a $\lambda/4$ which would have a maximum SWR of 1.25 at 3GhzThis represents a 45 percent savings in space over the 2GHz model. The design and analysis for ETL is generated using a program on HP41C.

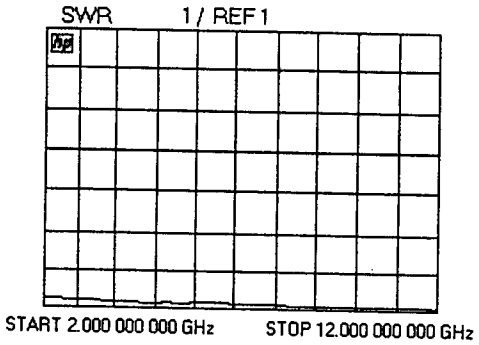


Figure 4. Standing wave ratio for exponential transmission line

Experimental Results

In very high-speed systems, the exact shape of a line can be important if reflections are to be kept at minimum (as shown in Figure 4). The arrangement shown in Figure 5 has been used to investigate the behaviour of two different line shapes. Notice that the changes from 50-ohms to 10-ohms in Fig.5a impedance changes are sharp, this causes the width of the line to be larger than elsewhere. For the other line Fig.5b, the impedance changes have been varied exponentially. These two microstrip lines are built on Ceramic substrate having thickness of 5mm and relative dielectric constant of 9.8. To determine the impedance at the ports and along the ETL, we use HP8510C network analyser to measure the S_{11} parameter of these two microstrip lines.

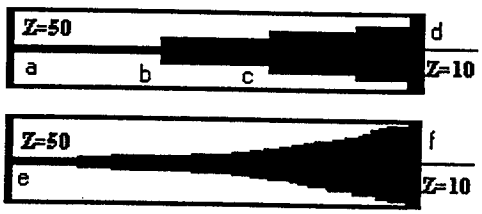
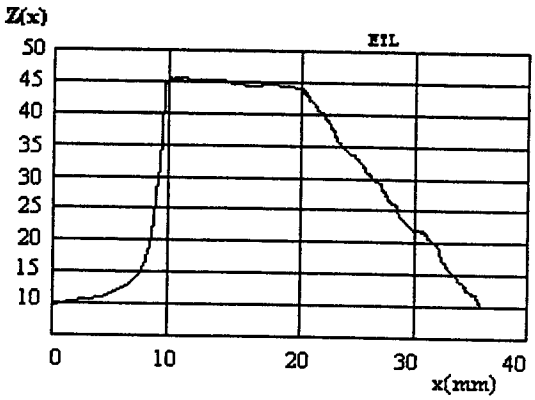


Figure 5. Physical layout of two microstrip lines

These data are added manually because of limitation oh network analyser for our method were these complex coefficient are converted into time-domain parameters via MATLAB software tool. It was found that with arrangement shown in Figure 6 the impedance dropped gradually from 50-ohms on one side to 10-ohms on the other side as shown in figure. It is seen that the reflection coefficient on the TDR trace varies close to linearly, the impedance varies exponentially along ETL. Also return loss was found that for frequencies above 9GHz to be less than –13dB where it should be noted that the reflections from the ETL decreases rapidly with frequency.

Figure 6. Time domain reflectometry trace showing how impedance is matched from 50-ohms to 10-ohms using ETL.



To compare the exponential transmission lines with those conventional microstrips in Fig 7a and 7b. we show the direct TDR measurment results of microstrip lines with the physical shape as shown in Figure 5. For one line, impedance changes sharp, these causes the width of line to be larger impedance changes than elsewhere. Figure 7a shows that –7.5% reflection occurs at point's b and c due to the lowered characteristic impedance at the changes. For the other line the impedance changes are exponential to produce constant line width which is shown on Figure 7b, it should be noted that an inductive reflection does occur at the end of the line due to the inductance of the resistors, (Resistor leads should be kept short to minimize termination inductance.

Conclusion

In the conclusion, a technique was described for analysing exponential lines for interconnects in high-speed digital circuits. First formulation for the transient analysis of high speed interconnects that uses time-domain scattering parameters for general N-port networks has been presented. Then we have shown how high speed digital circuits can be designed with a minimum reflection taking into consideration strong relationship between microstrip shape and the time domain reflectometry. The use of

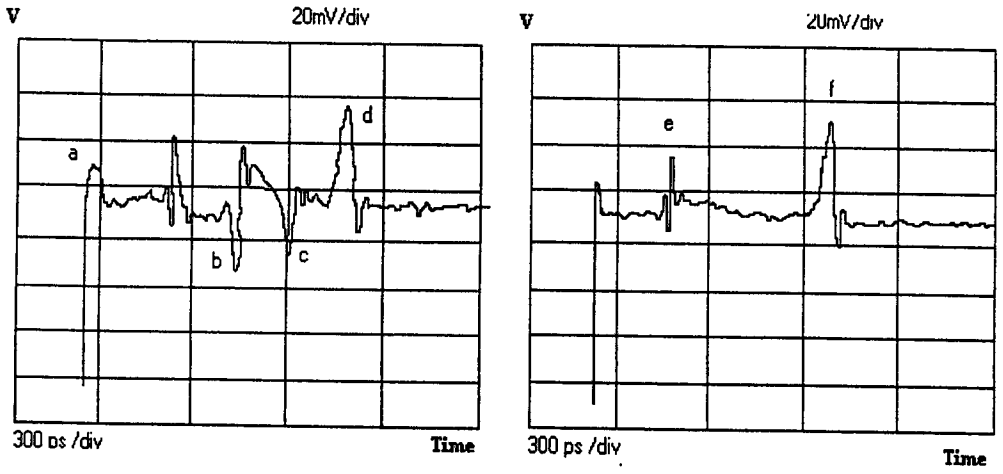


Figure 7. Reflection caused by transmission line shape (a) linear and (b) Exponential

exponential transmission lines, which acts as impedance matching is shown to bring improvements and enables unusually low impedance to be reached with large bandwidth which in principles shows the use of ETL in high speed PIN photodiode applications.

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Least-Square Finite Element Simulation of MESFET's Based on the Hydrodynamic Model

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I. INTRODUCTION

For years, the energy transport model has been used in commercial device simulators. The energy transport model is however not able to handle the situation when carrier velocity is comparable to random velocity. This may actually occur in very short-channel devices. In addition, the energy transport model ignores the convective term $\mathbf{v}\cdot\nabla\mathbf{v}$ that is partially responsible for high energy and velocity gradients in small devices. To properly account for the non-equilibrium behavior of carriers in short-channel devices, non-equilibrium physical transport models based on the hydrodynamic equations are desirable. Unfortunately, the hyperbolic nature of the hydrodynamic model enhances the difficulty in obtaining stable and the accurate numerical solution.

In the field of computational fluid dynamics, many numerical schemes have been developed to handle the hyperbolic conservation equations. The least square finite element method (LSFEM) is one of the successful examples. It was illustrated in [1,2] that this method is simple and stable for a large variety of flow and convection-diffusion problems. This study adapts the LSFEM to the one-carrier hydrodynamic transport equations, coupled with the Poisson's equation, for modeling of short-channel MESFET's. In addition to the detailed numerical results obtained from the developed least square hydrodynamic model, comparison of some electronic characteristics between the hydrodynamic and energy transport model is presented. ??

II. SEMICONDUCTOR HYDRODYNAMIC TRANSPORT MODEL

In the semiconductor hydrodynamic model, carrier transport is described by conservation equations of carrier density n, momentum $\mathbf{p}$ and energy w:

$$\frac{\partial n}{\partial t}+\nabla\cdot(n\mathbf{v})=0, \tag{1}$$

$$\frac{\partial n\mathbf{p}}{\partial t}+\nabla\cdot n\mathbf{p}\mathbf{v}+\nabla nk_BT_e=-en\mathbf{E}-\frac{n\mathbf{p}}{\tau_m}, \tag{2}$$

$$\frac{\partial nw}{\partial t}+\nabla\cdot n\mathbf{S}=-en\mathbf{E}\cdot\mathbf{v}-\frac{n(w-w_0)}{\tau_w}, \tag{3}$$

where $\mathbf{v}$ is the electron velocity, $\mathbf{p}=m^*\mathbf{v}$ (m^* is the electron mass), $\mathbf{E}$ is the electric filed, T_e is electron temperature, k_B is the Planck constant and e is the elementary charge. The energy flux $\mathbf{S}$ is defined as

$$\mathbf{S}=w\mathbf{v}+k_BT_e\mathbf{v}+\mathbf{q}. \tag{4}$$

$\mathbf{q}$ and κ are the heat flux and thermal conductivity, respectively, and are given as

$$\mathbf{q} = -\kappa \nabla T_e \quad \text{and} \quad \kappa = {5k_B^2 T_0 \tau_m}/{2m^*} \tag{5}$$

The carrier energy w is related to the carrier temperature and velocity by

$$w = \frac{3}{2}k_B T_e + \frac{1}{2}m^* |\mathbf{v}|^2 . \tag{6}$$

The thermal energy w_o is calculated from $w=1.5k_B T_o$, where T_o is the lattice temperature. The electric field E is obtained from the gradient of electric potential ψ

$$\mathbf{E} = -\nabla \psi , \tag{7}$$

and the potential is obtained by solving the Poisson's equation

$$\nabla^2 \psi = -\frac{e}{\varepsilon_s}(N_D - n), \tag{8}$$

where ε_s is the dielectric constant of the semiconductor, and N_D is the doping density.

III. LEAST-SQUARE FINITE ELEMENT FORMULATION

The hydrodynamic model can be rewritten as a unified matrix equation

$$[\mathbf{G}]\frac{\partial \mathbf{U}}{\partial t} + [\mathbf{A}_x]\frac{\partial \mathbf{U}}{\partial x} + [\mathbf{A}_y]\frac{\partial \mathbf{U}}{\partial y} + [\mathbf{A}_o]\mathbf{U} = \mathbf{Q}, \tag{9}$$

where the state variable vector is defined as

$$\mathbf{U} = [\rho \quad v_x \quad v_y \quad T_e \quad \psi \quad E_x \quad E_y \quad q_x \quad q_y]^T . \tag{10}$$

In Eq. (10), a new variable ρ is defined as $\rho = \ln n$. The implicit time-difference equation for Eq. (9) can be obtained using the backward difference in time with linearization of the coefficient matrices $[\mathbf{A}_x]$ and $[\mathbf{A}_y]$

$$[\mathbf{G}]\mathbf{U}^{k+1} - [\mathbf{G}]\mathbf{U}^k + \Delta t[\mathbf{A}_x]^k \frac{\partial \mathbf{U}^{k+1}}{\partial x} + \Delta t[\mathbf{A}_y]^k \frac{\partial \mathbf{U}^{k+1}}{\partial y} + \Delta t[\mathbf{A}_o]^k \mathbf{U}^{k+1} = \Delta t \mathbf{Q}^k , \tag{11}$$

where $\Delta t = t^{k+1} - t^k$. Based on Eq. (9), $\mathbf{U}^{k+1}$ is therefore determined from the vector $\mathbf{U}^k$ at the previous time step. The residual of the difference equation in Eq. (11) is defined as:

$$\Re = [\mathbf{G}]\mathbf{U}^{k+1} - [\mathbf{G}]\mathbf{U}^k + \Delta t[\mathbf{A}_x]^k \frac{\partial \mathbf{U}^{k+1}}{\partial x} + \Delta t[\mathbf{A}_y]^k \frac{\partial \mathbf{U}^{k+1}}{\partial y} + \Delta t[\mathbf{A}_o]^k \mathbf{U}^{k+1} - \Delta t \mathbf{Q}^k . \tag{12}$$

If the exact solution is found, the residual will be zero. A functional is introduced to minimize the deviation between the numerical and exact solutions in the 2D domain Ω,

$$\xi = \int_\Omega \Re^T \Re d\Omega . \tag{13}$$

When the optimum solution is obtained, the variation of the functional should be zero:

$$\delta\xi = 2\int_\Omega \delta\Re^T \Re \, d\Omega = 0 . \tag{14}$$

The finite element global matrix and load vector can be obtained from Eq.(14).

IV. SIMULATION RESULTS

The developed LSFEM for the hydrodynamic model is applied to simulation of Si MESFET's with deep submicron gates. The device structure is shown in Fig 1. The gate located at the center between source and drain contacts is 0.2μm long, and the drain/source metal contact is 0.1μm long. The device length and depth are 0.6 and 0.2

μm, respectively. The depth of the n^+ source/drain region is 0.05 μm. Four-node linear elements are used in the computation. The 2D device is divided uniformly into 96×32 elements.

Boundary discontinuities of electric field at the metal edges in the depletion-type MESFET structure given in Fig. 1 with a deep submicron gate length provide a challenging simulation problem. In addition, because of the depletion region under the gate due to the reverse-biased gate voltage, electron density near the gate contact is approximately 10 orders of magnitude smaller than the density in the n^+ region. This induces extremely large density and velocity gradients and enhances the challenge of avoiding the numerical instability, particularly in the hydrodynamic model that includes convective terms.

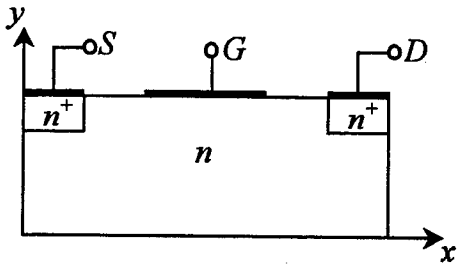


Fig. 1 The 2D MESFET structure used in the hydrodynamic simulation. In the n^+ source/drain regions, N_d= 3×10^{17} cm^{-3}, and N_d=10^{17} cm^{-3} in the n region.

Figs. 2 (a) and (b) displace the electron density and potential in the MESFET, respectively. Sudden changes in electron density at the n^+-n junction near the boundary are found. As shown in Fig. 2(b), strong electric field perpendicular to the gate near the Schottky barrier is shown due to the reverse-biased gate voltage. The strong filed deplete electrons near the gate. As a result, a depletion region is revealed under the gate between the source and drain n^+ regions, and a channel is formed on the bottom of the device away from the gate, as shown in Fig. 2(a).

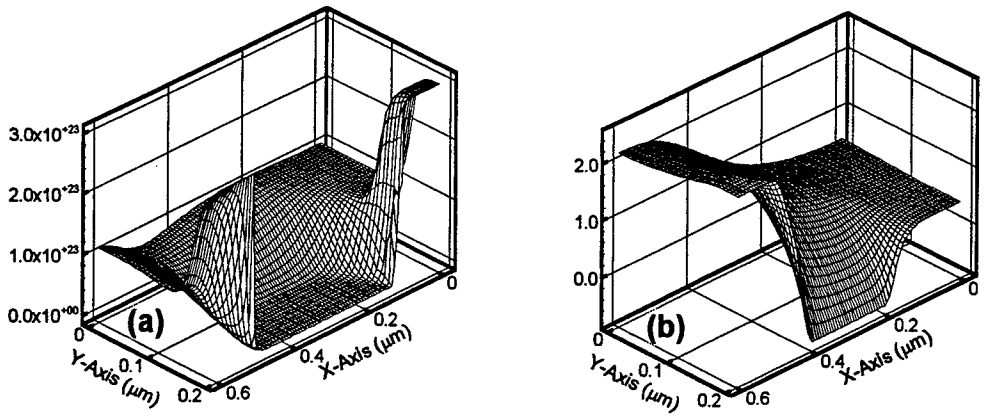


Fig. 2 (a) Electron density (m^{-3}) and (b) potential (V) in the MESFET at V_{ds}=2.0 Volt and V_{gs}= –0.6Volt.

The electron temperature distribution in the 2D MESFET is illustrated in Fig. 3. The electron temperature changes drastically near the edges of metal contacts due to the electrical field discontinuities and the equilibrium electron temperature on the metal contacts. An electron temperature as high as 4000K is reached near the gate contact between the drain and gate. However, in the channel the maximum electron temperature is near 2100K. In Fig. 4, drain current is shown as a function of V_{ds} at various gate-source voltages. As the negative V_{gs} increases, the depletion region extends toward the channel

that therefore becomes narrower. Consequently, drain current decreases with $|V_{gs}|$ at a given V_{ds}. The results from the hydrodynamic and energy transport models are compared in Fig. 4. As can been seen, the energy transport model overestimates the drain current at large drain voltage.

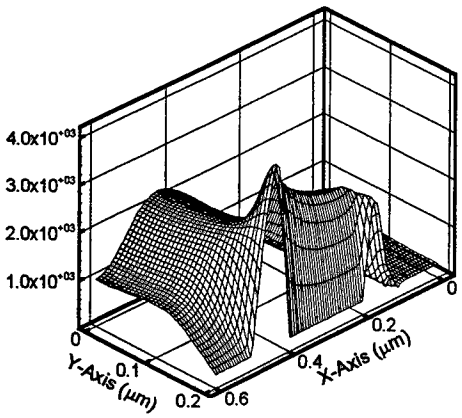


Fig. 3 Electron temperature (K) in the MESFET at V_{ds} =2.0 Volt and V_{gs}= −0.6Volt.

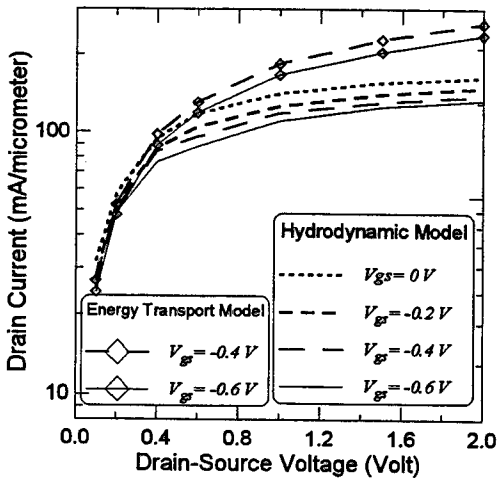


Fig. 4 I_{ds} of the MESFET as a function of V_{ds} at various gate voltage. Results from hydrodynamic and energy transport models are included.

IV. SUMMARY

A hydrodynamic LSFEM has been developed and applied to simulation of 2D MESFET's with deep-submicron gates. Unlike other finite element schemes developed for hydrodynamic modeling of semiconductor devices [3-5], no adjustable parameter or smooth operator is involved in the developed LSFEM to arrive at stable solution. In summary, the LSFEM has shown to be simple, stable and robust for hydrodynamic simulation of 2D semiconductor devices. In addition, the energy transport model has been found to overestimate the drain current of the MESFET's, as compared to the hydrodynamic model.

Acknowledgement – This work was supported in part by Superconductor Technologies and ARO under Grant No. DAAG55-98-1-0525.

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HYSTERESIS IN RESONANT TUNNELING DIODES WITH STAGGERED-BANDGAP HETEROSTRUCTURES

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In recent years, resonant tunneling diodes (RTDs) gained considerable attention as potential low-power sources of electromagnetic energy in submillimeter-wave region. Specifically, the extremely fast response associated with the negative differential resistance (NDR) of RTDs was seen as a viable gain mechanism for the generation of terahertz (THz) energy. Unfortunately, while double-barrier RTDs have been implemented as two-terminal oscillators up to 712 GHz [1] the power output levels have been restricted to microwatt levels primarily as a result of low-frequency design constraints (i.e., suppression of bias circuit oscillations). In fact, these fundamental limitations in the conventional implementation of RTDs as oscillation sources have motivated new study of "intrinsic" instabililty mechanisms [2]. This paper addresses a novel mesoscopic charge-feedback effect in staggered-bandgap structures as a potential new solution.

Indeed, a novel family of staggered-bandgap heterostructures may provide a new avenue for the development of very high frequency solid-state oscillators. Specifically, staggered bandgap heterostructures can admit significant interband tunneling currents. Furthermore, we expect these interband currents will lead to a nanoscale feedback between adjacent valence and conduction band wells. This novel use of nanotechnology seems extremely feasible, however, will require theoretical study and engineering to successfully demonstrate this electronic phenomenon.

The device is based on a type II resonant tunneling structure, i.e. a structure in which the quantum well and barrier semiconductors possess a type II band gap alignment to each other (Fig. 1). Here, the quantum well is formed by InAs sandwiched between two barrier regions (AlGaSb/InAs/AlGaSb double barrier structures). The left $Al_xGa_{1-x}Sb$ (x=0.4) barriers is adjacent to a highly doped InAs emitter while the right barrier is adjacent to the undoped InAs spacer which is grown on the highly doped InAs collector region. Note that the right barrier can also function as a quantum well for holes. However, the term quantum-well will be used here to denote conduction band confinement of electrons unless otherwise specified. As will be shown, this structure allows electrons to reside in the quantum-well layer and allows for hole trapping in the right quantum-barrier layer.

Under moderate levels of applied bias voltage, the staggered-bandgap allow for an alignment of quantum-barrier states with the empty states in the undoped collector spacer. Hence, significant interband tunneling currents result and leads to a buildup of holes in the valence band well via the staggered-bandgap channel. An electron-hole dipole is then formed and that may be subsequently discharged by properly specifying the charging process of the conduction-band well. An intrinsic bistability is observed in resonant tunneling diodes utilizing these structures due to the two different steady-state charge distribution that result for a single bias voltage [3].

The "qualitative" explanation of the observed bistability has been given by Buot and Rajagopal [4]. They underlined the importance of the Zener tunneling and trapped holes in these structures and have shown that a hysteresis can be realized in AlGaSb/InAs/AlGaSb double barrier structures. This paper presents results derived from a "quantitative" model for staggered-bandgap heterostructures This model includes: 1) interband Zener tunneling of valence-band electrons into the collector conduction and 2) hole resonant tunneling from the barrier through the well into emitter. A multiband description of electron and hole energy levels is incorporated into the quantitative model for an accurate study of interband resonant tunneling diodes.

In this analysis of the current-voltage (I-V) characteristic a sequential tunneling model has been utilized [5]. Here the potential has been approximated by a linear-coordinate dependence. Hence the electric field is piece-wise constant function of the coordinate with the discontinuity of the field occurring at the center of the well or the barrier (i.e., where the accumulated charges reside). Hence we have taken an electron-charge concentrated in the middle of the well while the hole-charge is concentrated in the middle of the right barrier. We define the field as F_{eb} at $0<z<b$, F_e at $b<z<b+w/2$, F_w at $b+w/2<z<b+w$, F_{wb} at $b+w<z<3b/2+w$, F_{rb} at $3b/2+w<z<w+2b$, and F_r at $w+2b<z<2b+w+c$ where w is the width of the well, b is the thickness of the barriers. Gauss's law gives the following relations between fields in neighboring regions

$$|F_{wb}| = |F_{rb}| + |Q_b|/\varepsilon_b \tag{1}$$

$$|F_w| = |F_e| + |Q_w|/\varepsilon_w \tag{2}$$

where Q_b is the hole charge in the right barrier, Q_e is the electron charge in the well, and ε_w and ε_b are dielectric permittivities of the well and barriers respectively. The balance equation for the electron distribution function f_e can be written as follows

$$\frac{\partial f_e}{\partial t} = \alpha_e(1-f_e) - \gamma_e f_e \tag{3}$$

where γ_e is the electron rate of decay through the right barrier into the collector and α_e is the influx from the emitter into the well. Similar balance equation can be derived for the hole distribution function f_h (i.e., $\partial f_h/\partial t = \alpha_h(1-f_h) - \gamma_h f$) where γ_h is the hole rate of decay through the well into the emitter and α_h is the rate of the Zener tunneling into the collector. It is possible to assume in the first approximation that rate coefficients γ_e and α_e do not depend on the in-plane wave vector k_{te} of the electron distribution function. It follows that f_e does not depend on k_{te} for

$$k_{te} < k_{tem} = \left(\frac{2m_n(E_F + e\,|\,F_e\,|\,(b+w/2) - E_{co})}{\hbar^2}\right)^{1/2} \tag{4}$$

where m_n is the electron effective mass, E_F is the electron Fermi energy in the emitter, E_{CO} is the energy of the lowest electron quasidisrete level with the middle of the well as a reference point and $f_e = 0$ at $k_{te} > k_{tem}$. The electron charge in the well can be found from (3) and (4) as

$$| Q_e | = \frac{ek_{tem}^2}{2\pi} f_e = \frac{ek_{tem}^2 \alpha_e}{2\pi(\alpha_e + \gamma_e)} \tag{5}$$

However, the Zener tunneling has a maximum at the hole in-plane wave vector $k_{th} = 0$. Hence equation (3) with $f_e \rightarrow f_h$ has to be solved for all k_{th} and Q_b must be found from a summation over all non-zero values of f_h. The system (1)-(5) is solved together with the Schrodinger equation for electron and hole wave functions. The wave functions are taken in WKB approximation. The positions of quasi-discrete electron and hole levels are found by neglecting tunneling currents through the barriers for electrons and through the well and across the forbidden gap for holes. The light hole components of the hole wave function is calculated from the Kane six-band model. The rate of the Zener tunneling is then derived via a dominate-decay resonant tunneling approximation. The thickness of barriers is taken as 20 A and the quantum-well thickness is 75 A. The spacer length is taken as 250 A and the doping donor concentration in the emitter and collector is taken 10^{18} cm $^{-3}$.

Our first goal was to find the existence of multiple stationary states in the I-V characteristic of the interband resonant tunneling diode (IRTD). This preliminary analysis was made by neglecting the temperature dependence of the distribution functions for electrons and holes in the well and the barrier, respectively. This simplified approach for solving equations (1)-(5) yields the I-V characteristic that is given in Fig. 2. As shown, the hole-charge strongly influences the spatial distribution of the potential and as result modifies the overall electron current. At threshold voltage $V_{th} = 0.56$ volts, where the position of the quantum-well resonant level becomes lower than the bottom of the conduction band in the emitter, a drastic drop in the electron current occurs. This is a familiar result as no electrons are available for the well-state resonant level. At higher voltages, a state with zero electron current can be realized due exclusively to interband hole tunneling (i.e., see dashed line). This second state persists down to 0.5 volts and creates a hysteresis in the I-V results. The extent of this duality in the I-V characteristics of the IRTD strongly depends on the spacer length and verifies the important influence of the interband tunneling mechanism. This initial work will be utilized in the future to consider the temporal nature of IRTD operation and the feasibility of charge-feedback instability.

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HYSTERESIS IN RESONANT TUNNELING DIODES WITH STAGGERED-BANDGAP HETEROSTRUCTURES

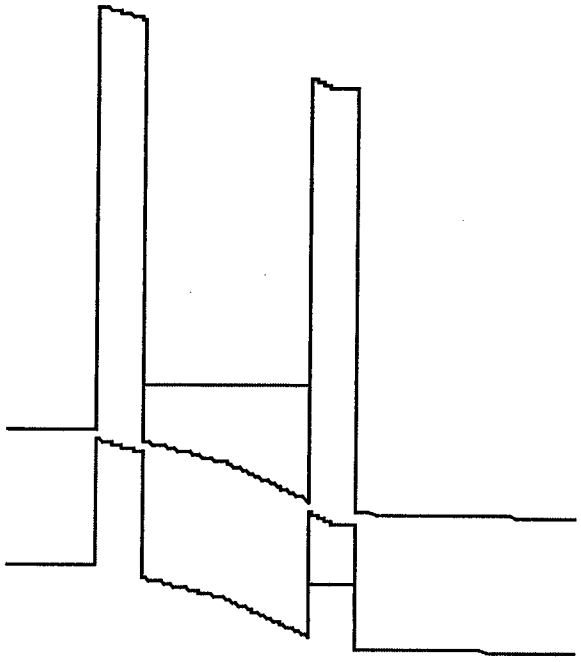


Fig.1. The band diagram for a type II resonant tunneling structure

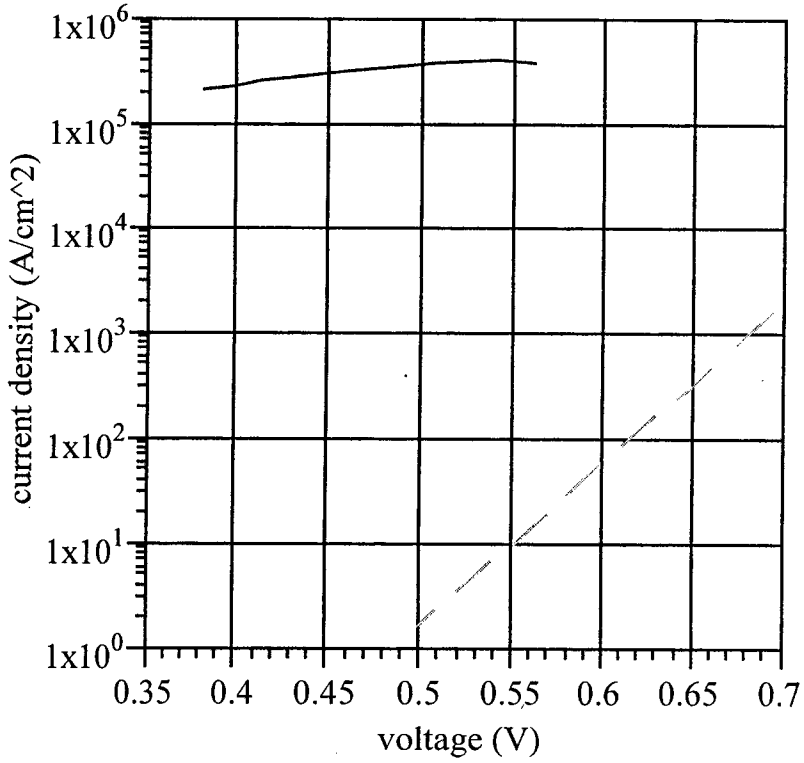


Fig.2. I-V characteristic of IRTD.

Numerical Simulation of G-V, C-V, and L-V Characteristics of a Resonant Tunneling Diode

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The remarkably fast-acting NDR of RTD's make them excellent devices for very high-frequency electronic applications. Generally, for the RTDs without plateau-like structure in their I-V characteristics, the operating frequency may reach 712GHz. Recent researches show that for RTD with plateau-like structure in I-V characteristics, intrinsic high frequency current oscillations exists at a fixed bias voltage over the RTDs. [1] The frequency of the oscillation can be as high as a few THz. Thus, RTDs can be used as a good THz source. The mechanism that the high frequency current oscillation exists at a fixed bias voltage is contributed to the wave-corpuscle duality of microscopic particles, the creation of an emitter quantum well (EQW), and the interaction between the energy level in the EQW and that in the main quantum well (MQW). Equivalent circuit model (ECM) is very important for understanding the performance limit of RTD and the design of devices integrated with radiating structures. The parallel-inductance model of RTDs is believed to be the suitable ECM. Conductance, capacitance, and inductance are the components of the ECM. Since RTDs are highly nonlinear devices and the carriers are in the state highly away from equilibrium, to understand the conductance-bias-voltage (G-V), capacitance-bias voltage (C-V), and inductance-bias-voltage (L-V) relationships of the RTDs with the plateau-like structure in the I-V characteristics is very important for designing RTDs and their integrated circuits. In this paper we will study the above stated relationships.

In order to get the above stated relationships, we numerically solved the coupled Wigner function-Poisson equations. The numerical method for solving the coupled equations and the detailed methods to extract the equivalent circuit parameters from simulation results can be found in our other paper. [2] Here, we report the G-V, C-V, and L-V characteristics for the resonant tunneling structure (RTS) extensively studied in literatures, [1] except the barrier width 27A is used here. Fig.1 shows the I-V characteristics of our simulation result. The detailed explanation of this curve has been given in our other paper.

Fig.2 shows the G-V characteristics of the RTS. That there are two negative conductance valleys in the curve is the basic feature of the G-V characteristics of the RTS with a plateau-like structure in its I-V characteristics. The double negative valley feature is the result of the interference between the injected and the reflected electron-waves and the coupling between the energy level in the EQW and that in the MQW. The first negative conductance valley is responding to the dramatic drop of current after the current passes its maximum value

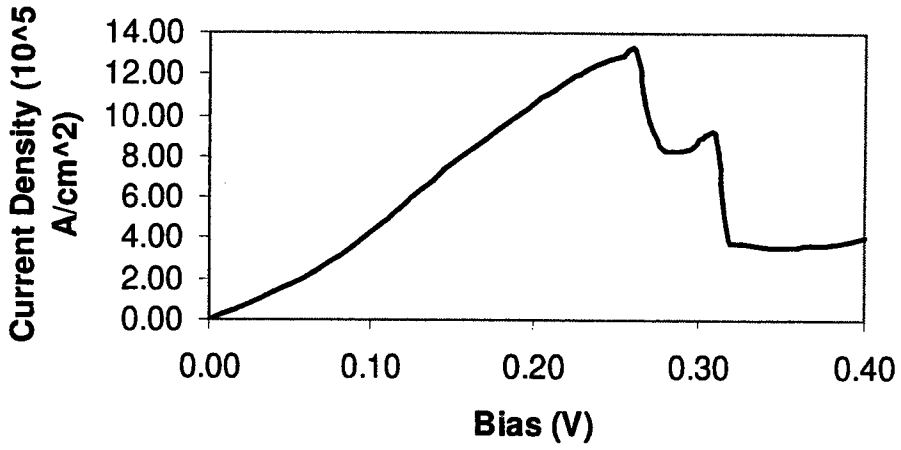


Fig.1 Current density via bias.

when the energy level in the MQW aligns the Fermi energy in the emitter. Then, the coupling between the energy in the EQW and that in the MQW lifts the energy level in the MQW. This process resists the further drop of the current and makes the conductance positive. Once the effect of this interaction is equal to or greater than that of the applied bias, the plateau-like structure of the I-V curve is created, the value of the conductance becomes small, and the variation of the

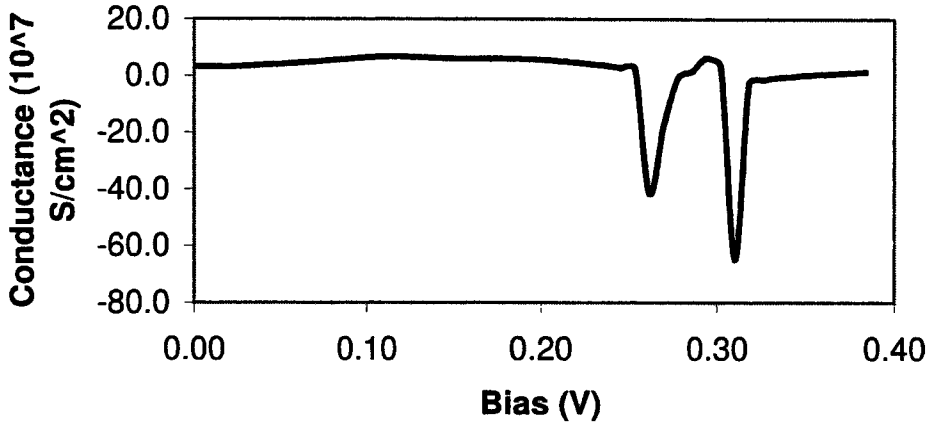


Fig.2 Conductance via bias. There are two negative differential conduction regions which show the basic features for the G-V characteristics of the RTDs with the plateau-like structure in the I-V characteristics.

conduction becomes flat. Further increasing the bias voltage may lead to the upside down of the positions of the energy level in the EQW and that in the MQW thereby the collapse of the EQW. With the collapse of the EQW, the distance between the energy level in the MQW and the Fermi energy in the emitter increases dramatically. This process leads to the

sharp drop of the current again thereby the negative conductance valley at a higher bias voltage. With the approach of the higher energy level in the MQW to the Fermi energy level in the emitter, more and more electrons can tunnel through the double barrier system. This process leads to the increase of the current again thereby the positive value of the conductance of the device again.

Fig.3 shows C-V characteristics of the RTD. The capacitance increases linearly with the bias until the bias enters the negative differential conductance and plateau-like structure region (NDCPLSR). After passing the NDCPLSR, the capacitance increase linearly again. From the definition of capacitance, we know that the capacitance is proportion to the net charge in the emitter and the collector of devices. With the increase of bias, more and more electrons are accumulated in front of the emitter barrier. Meanwhile, more and more electrons in the collector are extracted, resulting in a surplus of positive charge in back of the collector barrier. Because of the barriers, the net charge increases, so does the capacitance. When the bias enters the

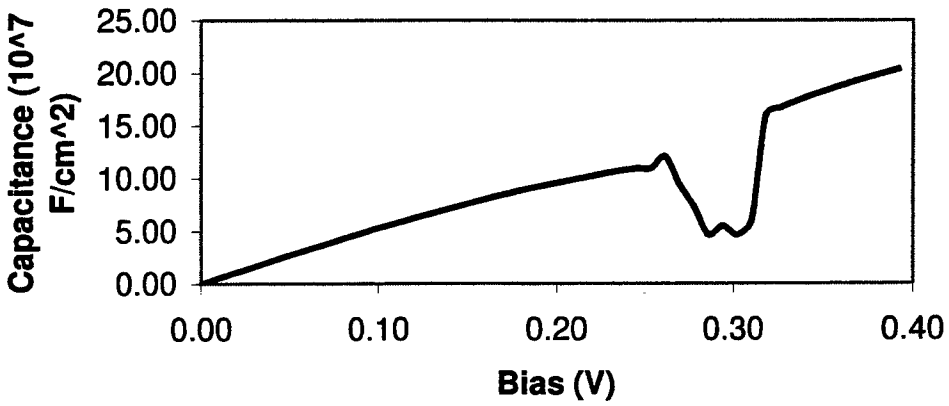


Fig.3 Capacitance via bias voltage. The capacitance drop in the C-V curve is caused by the depletion of electrons in front of the emitter barrier.

NDCPLSR, the interference between the injected and the reflected electron wave leads to the depletion of negative charges in front of the emitter and the formation of the EQW. Compared with the change of electron density in the emitter, the electron density in the collector does not change too much. Thus, the depletion of negative charge causes the reduction of the net charge in the emitter and collector thereby leading to the decrease of the capacitance. Once the bias passed NDCPLSR, the EQW collapses. Then the followed increase of the charge density in front of the emitter barrier leads to the increase of the capacitance again.

Fig.4 shows the inductance-voltage characteristic of the RTS's. The basic features of these curves show that outside of the NDCPLSR, the inductance of the RTS varies slowly. In the NDCPLSR, there are several valleys and a peak in the curves. The inductance of the devices is proportion to the time needed for the carriers passing the devices and and reversibly to the conductance of the devices. The negative sign of the inductance is passed on directly from the conductance of the

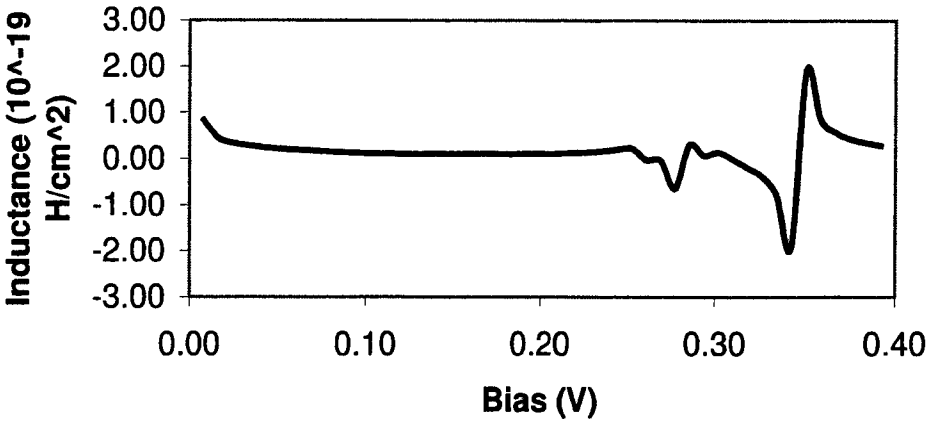


Fig.4 Inductance via bias voltage. Negative differential inductance means negative conductance. Since the inductance is proportion to the time that electrons pass the double barrier system, big inductance value means that the velocity of electrons is very slow.

devices. Thus, the sign of the inductance have the same meaning as that of the conductance. Physically, the velocity of the electrons when bias is in the plateau-like structure region is very low since the conduction state in the system comes from the coupling between the state in the EQW and that in the main QW, both being localized states. Thus, a valley of conductance in this region results. This is the reason for the creation of the valleys at lower bias. At higher bias voltages outside NDCPLSR, the electrons pass the RTD mainly by theormionic motion. Thus, the time passing the RTD is long. Considering that the conductance is negative in this voltage region, the second inductance valley is formed. Further increasing bias leads to the positive values of conductance after bias >0.35V. The sign change of the conductance causes the peak in L-V curve at 0.36V. With the approaching of the second energy level in the MQW to the Fermi energy level in the emitter, the time for electrons passing the structure reduces. This process leads to the decrease of the inductance.

It is important to note that there are two valleys in the curves' corresponding precisely to the two peaks in the I-V curve. This feature may be useful in making voltage-switched dual-frequency oscillators. This is corresponding to the number of the piece of the curves with NDC in the NDCPLSR in the current-voltage characteristic of RTS. According to this feature, maximum frequency changeable RTD concept may be provided.

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Temperature Dependent DC and Microwave Performance of 4H-SiC MESFET

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Abstract. Temperature dependent DC and small-signal performance of 4H-SiC is studied by 2D numerical Drift-Diffusion model. Simulation results of DC and small-signal characteristics are similar to the experimental results. Both DC and microwave performances degrade as temperature increases. This is mainly due to the degradation of mobilities. Simulation results show that 4H-SiC MESFET is capable to operate above $10GHz$ and $500K$.

I INTRODUCTION

Silicon carbide MESFET is a very promising compound semiconductor device for high temperature and high power microwave applications [1] such as high frequency power supplies and solid-state UHF broadcast systems. This is mainly due to the combination of its superior physical properties: wide energy band gap, high saturated electron velocity, high breakdown field and high thermal conductivity. Many experiments have successfully demonstrated the high temperature and high power microwave operations of 4H-SiC MESFET [2–4]. However, only a few papers have been published on the modeling of microwave performance of 4H-SiC MESFET [5–8]. Detail and accurate device modeling is indispensable in predicting the operation limits of the device and understanding the experimental results. In this paper we report a simulation study on the temperature dependent DC and the small-signal frequency responses of 4H-SiC MESFETs by using 2D temperature dependent numerical Drift-Diffusion model.

II TEMPERATURE DEPENDENT DC AND SMALL-SIGNAL MODELING

Due to its high thermal conductivity [3], isothermal drift-diffusion equations are used to describe the temperature dependent silicon carbide device operation. In this work the following temperature dependent physical parameters are included: intrinsic energy band gap [9], incomplete ionization of shallow donors and acceptors [9,10], low field mobility [11], electron saturation velocity [12,13], and impact ionization rate [14].

For small-signal analysis, dielectric permittivity is considered as frequency independent, which is reasonable for the frequency range we are interested. Mobilities are also considered frequency independent according to Monte Carlo simulation [15]. After high accuracy DC steady state solution is achieved, the small-signal characteristics can be obtained in frequency domain [16,17]. A set of appropriate boundary conditions are used: Ohmic contact boundary condition, Schottky contact boundary condition and artificial boundary condition. Both the ideal Schottky boundary condition [18] and the non-ideal Schottky boundary condition are used. The following non ideal Schottky boundary condition is used to take into account of the transition layer between metal and semiconductor [19]:

$$\psi \mid_{x=0} = V_G + \phi_{bi} + \frac{\varepsilon_{SiC}}{C_{int}} \cdot \frac{\partial \psi}{\partial x} \mid_{x=0+}, \tag{1}$$

where $\phi_{bi} = \frac{E_g}{2} + \frac{V_T}{2} \ln\left(\frac{N_v}{N_c}\right) - \phi_B$, $C_{int} = \varepsilon_{int}/\delta$ is the interfacial transition layer capacitance and δ is the thickness of the interfacial layer.

III SIMULATION RESULTS AND DISCUSSION

The structure of the simulated 4H-SiC MESFET [2]is shown in Figure 1. The N^+ contact doping is larger than $2 \times 10^{19} cm^{-3}$. The n-type channel doping is $1.7 \times 10^{17} cm^{-3}$. The p-type buffer doping is $1.4 \times 10^{15} cm^{-3}$.

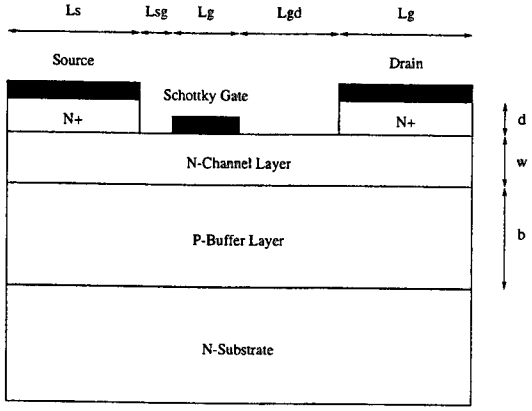


Figure 1. Structure of the simulated 4H-SiC MESFET. $L_s = 1.0\mu m$, $L_{sg} = 0.3\mu m$, $L_g = 0.7\mu m$, $L_{gd} = 0.8\mu m$, $L_d = 1.0\mu m$, $d = 0.15\mu m$, $w = 0.26\mu m$ and $b = 6.0\mu m$.

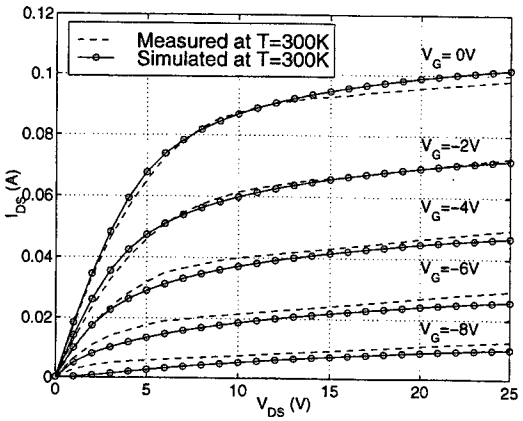


Figure 2. Simulated and measured steady state I-V characteristics at $300K$ for non-ideal case Schottky boundary condition with a thin interfacial transition layer.

After including the incomplete ionization effect, it is impossible to fit the experimental data with reasonable Schottky barrier height by using ideal Schottky boundary condition. But with non ideal Schottky boundary condition of a 5 Å interfacial layer. Excellent fitting with the experimental data [2] is achieved as shown in Figure 2.

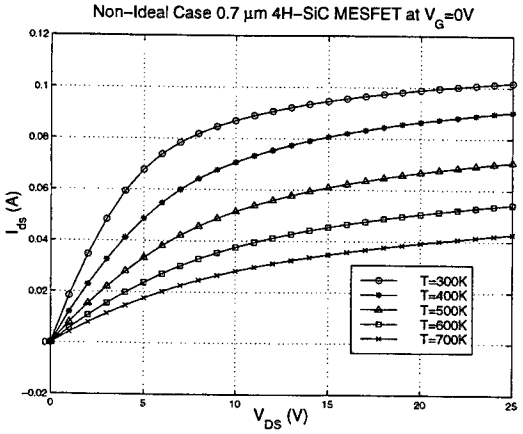


Figure 3. Non-ideal case drain current versus drain-to-source voltage at $V_G = 0V$ for the temperature range from $300K$ to $700K$.

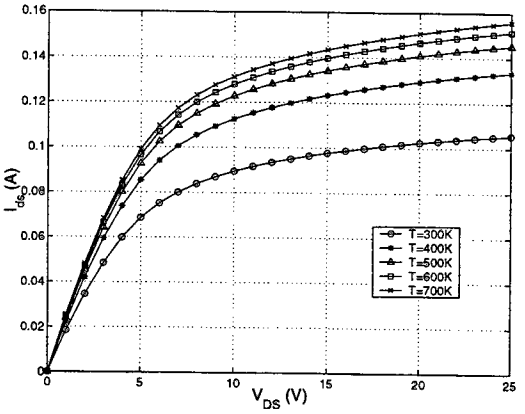


Figure 4. Temperature dependent IV characteristics assuming temperature independent mobilities and saturated velocities from $300K$ to $700K$.

The same set of physical parameters are used in the simulation of high temperature performance of the device. Figure 3. shows the drain current at the gate voltage $V_G = 0V$ for the temperature from $300K$ to $700K$. As temperature increases, the current level decreases monotonically. This behavior was observed for a similar device from $25°C$ to $285°C$ [3]. The temperature dependent characteristics can be explained as following. As temperature increases, the channel impurity ionization level increases, the depletion width decreases and the effective channel thickness increases. Thus the total

number of mobile carriers increases. At the same time, the carrier mobility decreases as temperature increases. But the decrease of the mobility is dominant over the increases of the ionization levels and the effective thickness. This effect is clear from Figure 4. where the same set of parameters is used except the mobilities and saturation velocities are kept temperature independent and taken the values as in the case of $T = 300K$. The increase of the ionization rate of the channel donors leads to the increase of the drain current as temperature increases. This proves that in the real device the mobility degradation is the dominant factor in the temperature dependent performance of 4H-SiC MESFET.

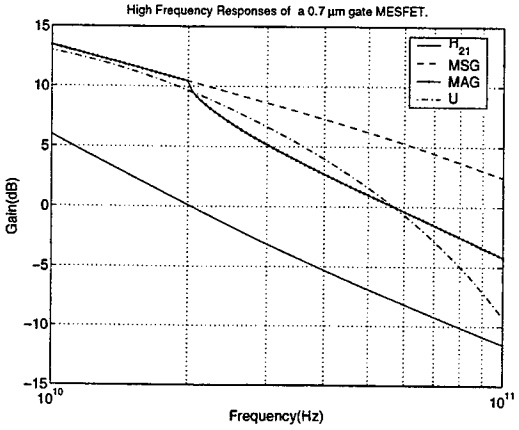


Figure 5. High frequency small-signal responses H_{21}, MSG, MAG and U of a $0.7\mu m$ gate length MESFET.

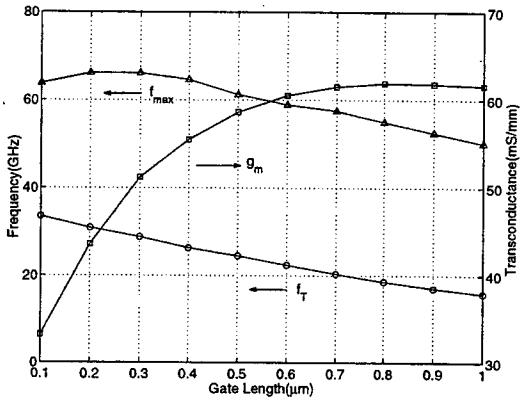


Figure 6. Cut-off frequency f_T, maximum oscillation frequency f_{max} and transconductance g_m of 4H-SiC as a function of gate length.

The small-signal frequency responses of current gain H_{21}, MSG(Maximum Stable Gain), MAG(Maximum Available Gain) and U(Unilateral Gain) of the same device are shown in Figure 5. The bias conditions are $V_{GS} = 0V$ and $V_{DS} = 30V$. The physical parameters are taken from literatures and ideal Schottky boundary conditions are used. The cut-off frequency f_T is $20GHz$ and the maximum oscillation frequency f_{max} is $57GHz$. The simulation results of f_T and f_{max} are much higher than the reported experimental results of $6.7GHz$ and $12.9GHz$ [2]. This means that the experimental 4H-SiC MESFET has not been optimized yet. The 4H-SiC MESFET with similar geometry should be capable of operating at $15GHz$.

The cut-off frequency f_T, maximum oscillation frequency f_{max} and transconductance g_m of 4H-SiC MESFET are shown in Figure 6. as a function of gate length. As the gate length decreases, f_T increases monotonically up to $33GHz$ with $0.1\mu m$ gate, while g_m decreases monotonically. This suggests that that C_{GS} and C_{GD} decrease much fast than g_m. f_{max} increases as the gate length decreases and reaches a maximum near $0.3\mu m$. With a $0.3\mu m$ gate length, f_T is around $28GHz$ and f_{max} is about $65GHz$.

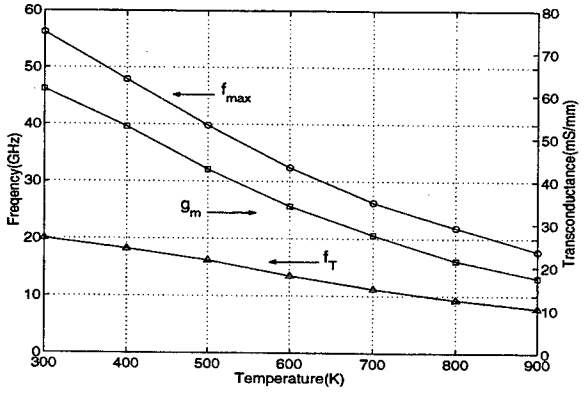


Figure 7. Temperature dependent f_T, f_{max} and g_m of simulated 4H-SiC MESFET.

The temperature dependent cut-off frequency f_T, maximum oscillation frequency f_{max} and transconductance g_m are shown in Figure 7. from $300K$ to $900K$ for a $0.7\mu m$ gate device. As temperature increases, f_T, f_{max} and g_m decreases. The same characteristics are observed experimentally [4]. But the simulation results are higher than experimental data. The degradations of f_T, f_{max} and g_m are due to the degradation of mobility and saturated velocity.

IV CONCLUSIONS

The temperature dependent DC and small-signal frequency responses are studied by 2D Drift-Diffusion model. The performance of 4H-SiC MESFET degrades as temperature increases: DC saturation current, small-signal cut-off frequency, maximum oscillation frequency, and transconductance decrease monotonically. This is mainly due to the degradations of mobilities and saturation velocities. The increase of channel dopants ionization can only slow down the degradation of the performance of the device. As the size of the gate decreases, the cut-off frequency and the maximum oscillation frequency increase. 4H-SiC MESFET should be capable of operating above $10GHz$.

ACKNOWLEDGMENTS

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Role of the Schottky Gate Structure in the Temperature Dependence of Breakdown Characteristics of 4H-SiC MESFET

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†U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, MD 20783

Abstract. Silicon carbide device is desired to work under high temperature and high power condition. The temperature dependent breakdown characteristic is crucial. This paper reports a simulation study of the influence of the structure of Schottky gate on the temperature dependent breakdown behavior of a 4H-SiC MESFET. The early breakdown is due to the existence of a thin interfacial transition layer. The existence of the interfacial layer may also destroy the positive temperature coefficient of breakdown voltage.

I INTRODUCTION

Silicon carbide is a very attractive semiconductor material for high temperature, high power and high frequency applications [1] due to a combination of its superior physical properties: wide energy band gap, high saturated electron velocity, high breakdown field and high thermal conductivity. Among hundreds of silicon carbide polytypes, 4H-SiC has received most attention because of its large band gap [2], high electron mobility [3] and negative temperature dependence of impact ionization rate [4]. The decreasing of impact ionization coefficients with increasing temperature may lead to positive temperature coefficient of breakdown voltage, which is a very preferable characteristics for a device operating under high power condition to maintain stability and reliability. Many experiments have successfully demonstrated the high voltage and high temperature operations of 4H-SiC MESFET [5–7]. However, there is a rather large discrepancy in the breakdown voltage between the experimental data and the theoretical predictions [5,8]. In this paper we report the physical mechanism possibly leading to the early breakdown of 4H-SiC MESFET and the negative temperature dependence of breakdown characteristics.

II TEMPERATURE DEPENDENT DRIFT-DIFFUSION MODELING

Like Si and GaAs, the thermal conductivity of silicon carbide decreases as temperature increases. But the high temperature thermal conductivity of silicon carbide is still much higher than the thermal conductivity of silicon at low temperature [6]. Due to its high thermal conductivity, the lattice temperature of the silicon carbide device can be considered as uniform even at relatively high temperature. Thus, it is possible to use isothermal drift-diffusion equations to describe the temperature dependent silicon carbide device operations. To obtain a correct picture of the temperature dependent operation of the device, the isothermal drift-diffusion model should include all available temperature dependent physical parameters. In this work the following temperature dependent physical parameters are included into the model: intrinsic energy band gap [9], incomplete ionization of shallow donors and acceptors [9,10], low field mobility [3], electron saturation velocity [11,12], and impact ionization rate [4].

In order to complete the description of the device, a set of appropriate boundary conditions are needed: Ohmic contact boundary condition, Schottky contact boundary condition and artificial boundary condition. Generally speaking it is very difficult to obtain sharp, clean and intimate metal-semiconductor contact as described by the ideal Schottky boundary condition [13]. Most of

times there always exists a transition layer between metal and semiconductor [14]. Depending on the experimental technique, the interfacial transition layer can be thin or thick, flat or rough, and with low density interfacial states or high density interfacial states. The experimental results of SiC Schottky diodes show that it is impossible to explain the I-V and C-V measurements with ideal intimate Schottky contact theory [14]. A thin interfacial transition layer is necessary to explain the experimental characteristics. The following non-ideal Schottky boundary condition for Poisson's equation can be derived by assuming charge neutrality [15].

$$\psi \mid_{x=0} = V_G + \phi_{bi} + \frac{\varepsilon_{SiC}}{C_{int}} \cdot \frac{\partial \psi}{\partial x} \mid_{x=0^+}, \tag{1}$$

where $\phi_{bi} = \frac{E_g}{2} + \frac{V_T}{2} \ln\left(\frac{N_v}{N_c}\right) - \phi_B$, $C_{int} = \varepsilon_{int}/\delta$ is the interfacial transition layer capacitance and δ is the thickness of the interfacial layer. The details of the analytical results will be published elsewhere.

Comparing to the ideal Schottky boundary condition, the only difference is the last term. If we absorb the last term in the expression of ϕ_{bi}, it can be considered that the effective Schottky barrier height becomes

$$\phi_B^{eff} = \phi_B - \frac{\varepsilon_{SiC}}{C_{int}} \frac{\partial \psi}{\partial x} \mid_{x=0^+} . \tag{2}$$

It is clear that the effective Schottky barrier height becomes temperature and voltage dependent instead of a fixed value. Equivalently the last term can be combined with the gate voltage to create an effective gate voltage

$$V_G^{eff} = V_G + \frac{\varepsilon_{SiC}}{C_{int}} \frac{\partial \psi}{\partial x} \mid_{x=0^+} . \tag{3}$$

MESFET works in the depletion regime, thus the electrical field at the interface $\frac{\partial \psi}{\partial x} \mid_{x=0^+} > 0$. Therefore the existence of a thin transition layer between metal and semiconductor leads to the increase of the effective gate voltage or equivalently the decrease of the effective Schottky barrier height. The thicker the transition layer, the stronger the deviation from the ideal Schottky boundary condition. However, the thickness of the transition layer should be small enough to allow most of the thermionic emission current tunnel through the transition layer without reflection, and allow the effective Schottky barrier height remain positive to create a depletion region under the gate. The analysis of the experimental data [14] shows that the transition layer thickness is between 3 Å and 6 Å if one assumes the dielectric permittivity of the transition layer is the same as that of SiO_2, which corresponds to one or two atomic layers of transition crystal structure that are different from the crystal structure of either semiconductor or metal. Such a thin transition layer allows us to assume that the tunneling probability of thermionic emission current is close to one. In fact the exact thickness may be different from the above values due to the uncertainty of the dielectric permittivity of the transition layer.

III SIMULATION RESULTS AND DISCUSSION

The structure of the simulated 4H-SiC MESFET [5]is shown in Figure 1. The N^+ contact doping is larger than $2 \times 10^{19} cm^{-3}$. The n-type channel doping is $1.7 \times 10^{17} cm^{-3}$. The p-type buffer doping is $1.4 \times 10^{15} cm^{-3}$. The gate width is $332 \mu m$.

First the temperature dependent breakdown characteristics are simulated under ideal Schottky boundary condition and shown in Figure 2. It is clear to see that the device has positive temperature coefficient of breakdown voltage. This is solely due to the negative temperature dependence of impact ionization rate of 4H-SiC. The room temperature breakdown voltage is around 180V while the experimental breakdown voltage is much less [5].

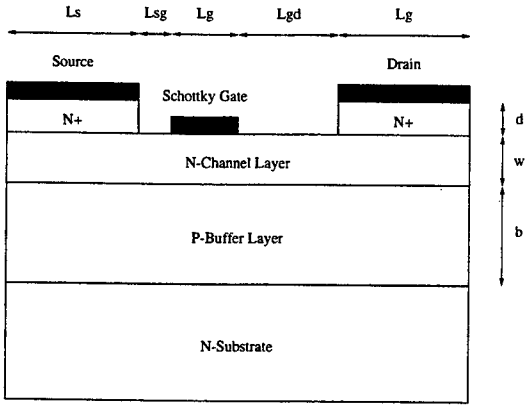


Figure 1. Structure of the simulated 4H-SiC MESFET. $L_s = 1.0\mu m$, $L_{sg} = 0.3\mu m$, $L_g = 0.7\mu m$, $L_{gd} = 0.8\mu m$, $L_d = 1.0\mu m$, $d = 0.15\mu m$, $w = 0.26\mu m$ and $b = 6.0\mu m$.

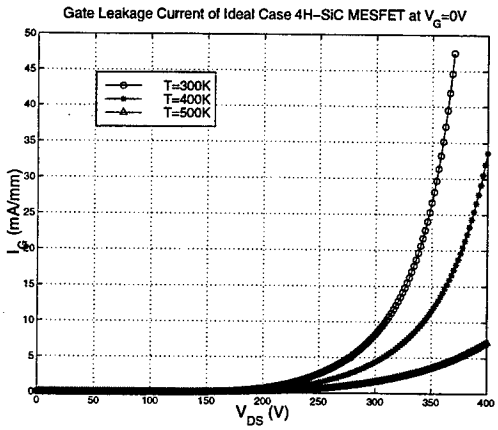


Figure 2. Temperature dependent gate leakage current at $V_G = 0V$ of ideal Schottky contact case.

Next the non-ideal Schottky boundary condition is used to simulate the breakdown behavior of the device while all the other physical parameters are kept the same. The gate leakage current is shown in Figure 3. for three different thickness of the interfacial layer at room temperature. As the thickness of the interfacial layer increases, the breakdown voltage decreases. This fact suggests that the existence of a thin transitional interfacial layer between gate metal and silicon carbide may be the possible reason that causes the early breakdown of the device and makes the ideal theory fail.

The temperature dependent breakdown behavior of the MESFET under non-ideal Schottky boundary condition with interfacial layer thickness of 5 Å is shown in Figure 4. In contrast to the case with ideal Schottky boundary condition, the temperature coefficient of breakdown voltage is negative.

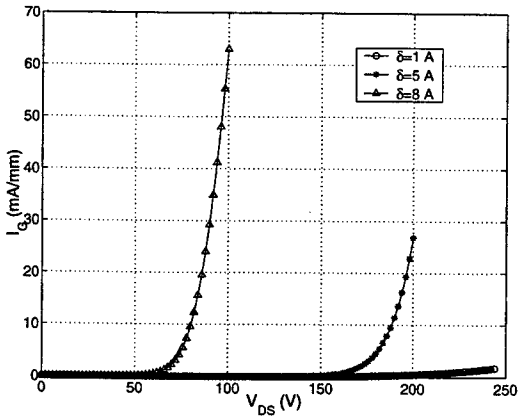


Figure 3. Gate leakage current at $V_G = 0V$ and $T = 300K$ of non-ideal Schottky contact with interfacial thickness of 1 Å, 5 Å and 8 Å.

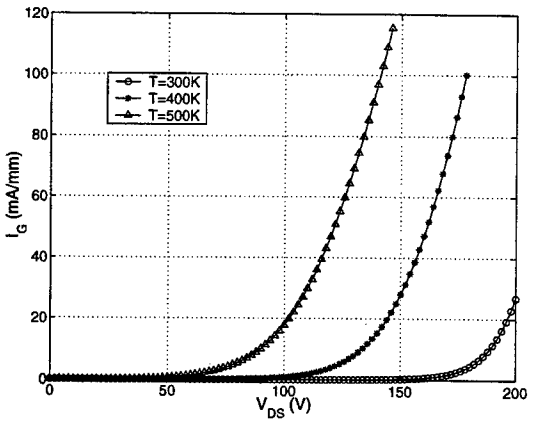


Figure 4. Temperature dependent gate leakage current at $V_G = 0V$ of non-ideal Schottky contact with a interfacial transition layer thickness of 5 Å.

The early breakdown and negative temperature coefficient of breakdown voltage are due to the existence of interfacial transition layer. The interfacial layer results in the effective Schottky barrier height lowering and consequently diffusion potential lowering. Analytical results show that the diffusion potential depends on the thickness of the transition layer as well as the temperature. As the thickness of the interfacial layer increases, as long as it is thin enough to allow most electron tunnel through, the diffusion potential decreases almost linearly. As temperature increases, the diffusion potential decreases almost linearly too. Since the gate leakage current depends on the diffusion potential exponentially, the diffusion potential lowering results in an exponential increases of the gate leakage current. Thus as the thickness of the interfacial layer increases, the breakdown voltage

decreases as shown in Figure 3. ; as temperature increases, the increase of the leakage current due to the diffusion potential lowering overwhelms the effect of the linear negative temperature coefficient of impact ionization rate. This is the reason that the gate leakage current increases as temperature increases. The existence of a thin transition layer completely destroys the nice property of the positive temperature coefficient of breakdown voltage of 4H-SiC MESFET.

IV CONCLUSIONS

The quality of Schottky gate contact plays a very important role in the high voltage and high temperature operation of 4H-SiC MESFET. The existence of a thin interfacial layer leads to early breakdown of the device and may destroy the nice characteristics of positive temperature coefficient of breakdown voltage promised by the negative temperature dependent impact ionization rate. A sharp and intimate Schottky contact is a necessary condition for a 4H-SiC MESFET working in high temperature and high voltage regime.

ACKNOWLEDGMENTS

The authors would like to thank U.S. Army Research Laboratory for financial support of this research.

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Ohmic Contacts to ZnO and Related II-VI Compound Semiconductors Using Ga Focused Ion Beams

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The piezoelectric, gas sensing and optoelectronic properties of ZnO provide for many applications in transducers, sensors and UV light emitting elements. This II-VI wide band gap semiconductor can be grown in n-type form, and research efforts are focusing on improving material quality, controlling resistivity and other properties by doping [1, 2], and developing devices usually in combination with other wide band-gap semiconductors like GaN [3]. Although in its heavily doped form ZnO can in itself be used as an ohmic contact for transparent electrodes, undoped and lightly doped ZnO, appropriate for transducer and other device work, may present significant problems in the development of reliable low contact resistance ohmic electrodes, especially when combined with its alloys with Mg. In view of the potential of this semiconductor in transducer and light emitting technology where the reliability and robustness of the ohmic contacts are critical for low loss long term operation, a reliable contact formation process for device fabrication needs to be addressed and developed.

In this work we report the development of ohmic contacts on ZnO and MgZnO epitaxial layers, using focused ion beam (Ga) surface-modification and direct-write Pt metal deposition. This technique has been developed for SiC [4], and it is now transferred to develop metallization technology in ZnO and its alloys.

The epitaxial ZnO layers were grown on sapphire substrates by pulsed laser deposition (PLD), at a substrate growth temperature of 750 °C in a vacuum chamber with base pressure of $1x10^{-7}$ torr and partial oxygen pressure of $1x10^{-4}$ torr. The focused ion beam (FIB) system uses Ga ions with energies of 20 and 30 keV. The surface-modification step is done prior to metal deposition, using Ga beam doses ranging between $1x10^{16}$ and $8x10^{17}$ cm^{-2}. Beam energies for this work were set at 30 keV. The direct-write metal

deposition step follows the surface-modification step in situ the FIB chamber by introducing dimethyl-methyl-cyclopentadienyl-Pt precursor gas in the Ga beam, and writing the TLM pattern [5] for the contact resistance measurements. Two different TLM patterns were formed, one with 25x10 μm and one with 60x40 μm metal pads for comparison (Fig. 1).

Fig. 2, shows the TLM contact resistance measurements for the direct-write Pt contacts on unmodified, and Fig. 3 shows the TLM measurements of the direct-write and surface-modified epitaxial ZnO. Figure 4 shows the contact resistance values with surface-modification dose. The unmodified surface produced a contact resistance $r_C = 4.1x10^{-3}$ Ω cm^2, while the direct-write and surface-modified samples produced contact resistance values of $r_C = 3.1x10^{-4}$ Ω cm^2, $r_C = 3.3x10^{-4}$ Ω cm^2, and $r_C = 3.7x10^{-4}$ Ω cm^2, for ion beam doses of $D_1 = 1x10^{17}$ cm^{-2}, $D_2 = 3x10^{17}$ cm^{-2}, and $D_3 = 3x10^{16}$ cm^{-2} respectively. The larger contact pads also gave contact resistance values of $r_C = 4.0x10^{-3}$ Ω cm^2 for the unmodified surface, and $r_C = 3.0x10^{-4}$ Ω cm^2 for the modified surface, in good agreement with the smaller size contacts. Clearly the effect of the surface-modification step is to substantially reduce the contact resistance by over one order of magnitude. An optimum surface-modification dose exists at $D_1 = 1x10^{17}$ cm^{-2}, whereby higher doses appear to degrade the contact resistance, as seen in our previous work [4].

SIMS analysis shows a significant distribution of Ga atoms incorporated within the top 25 nm of the ZnO surface. Ga has been examined in the past as a doping agent in ZnO [1], and the resistivity was found to be strongly influenced by Ga content (up to 6% Ga), and the substrate temperature. Carrier concentrations as high as $1x10^{20}$ cm^{-3} and resistivities as low as $4.9x10^{-2}$ Ω cm, were reported. ZnO ohmic contacts are usually In based [6], which lacks the necessary temperature and structural robustness required for thermal cycling and light emitting operation. Pt based ohmic metallizations have the potential for providing stability and reliability under thermal cycling in cases of sensor applications, but early work on understanding metal semiconductor barriers in ZnO [7] has established barrier heights in the range of 0.6 to 0.7 eV for Pd, Au and Pt [8], which, for ohmic contact formation, need to be significantly reduced. Our technique seems to reduce the barrier significantly by introducing disorder and a surface layer of Ga, that provides a low resistance robust ohmic contact for this system.

Acknowledgments: The assistance of Drs. J. H. Orloff and K. Edinger with the focused ion beam processing is gratefully acknowledged. This work was supported by NSF grant ECS9813819 supervised by R. Khosla, and by ARL agreement DAAL01-95-2-3530.

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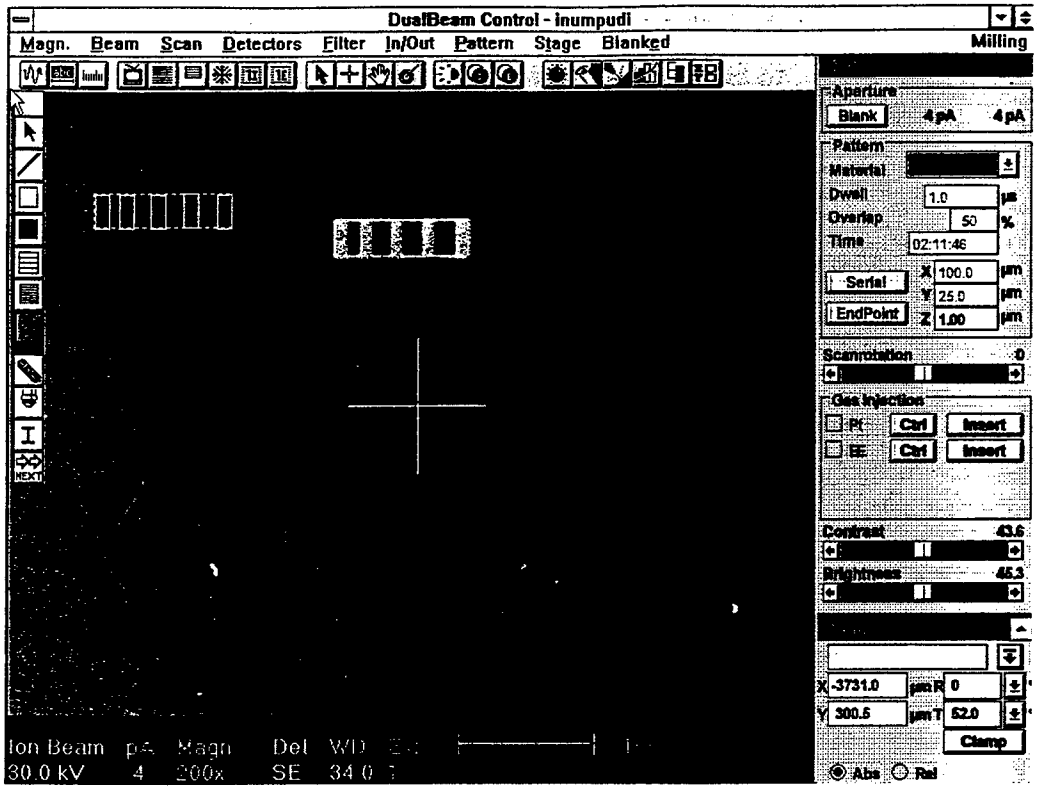


Fig. 1. Focused ion beam direct-write TLM pattern of Pt on PLD grown epitaxial ZnO on Sapphire for contact resistance measurement.

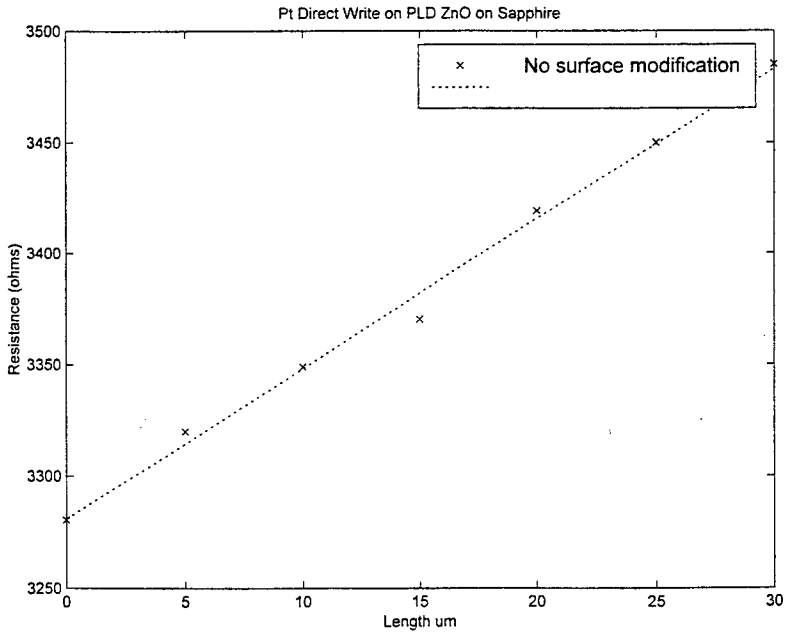


Fig. 2. TLM contact resistance measurement of unmodified direct-write Pt on ZnO.

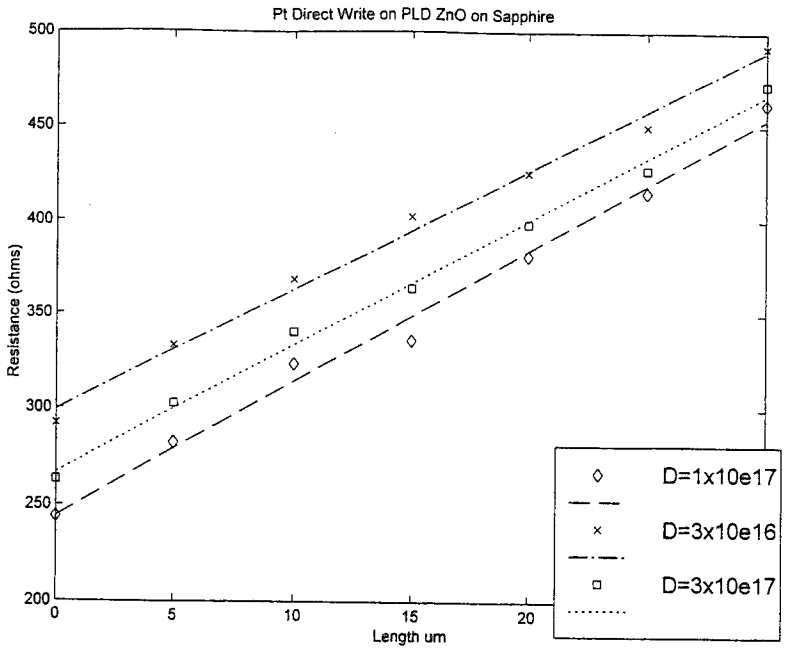


Fig. 3. TLM contact resistance measurement of surface-modified and direct-write Pt contacts on ZnO on Sapphire.

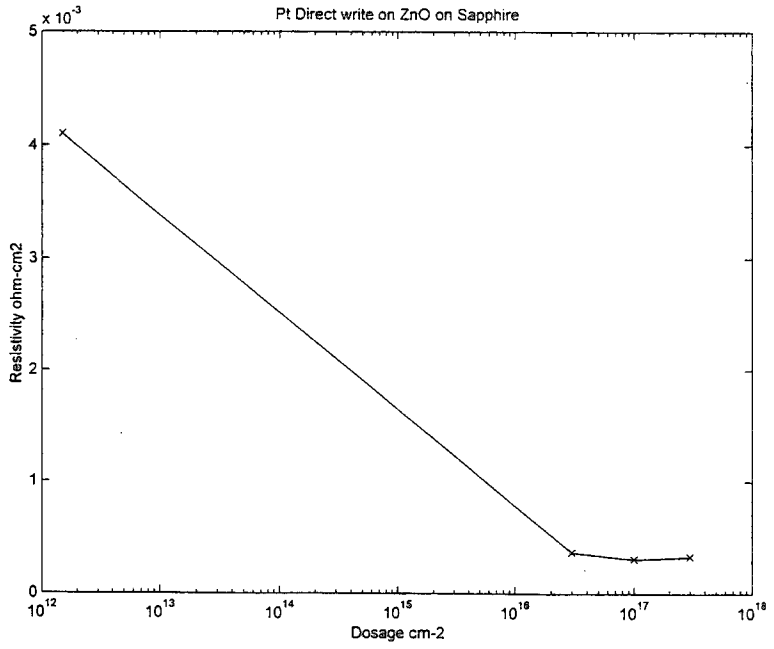


Fig. 4. Contact resistance versus surface-modification dose. Over one order of magnitude lower contact resistance is observed for the surface-modified Pt contacts.

Silicon-Germanium Substrates

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Introduction

In this paper we describe the bulk crystal growth of high germanium concentration Si-Ge single crystal substrates at least 50 mm in diameter using a standard silicon Czochralski (CZ) furnace. Although there are many publications regarding the preparation of thin film SiGe on silicon substrates, there has also been some progress reported on the preparation of various compositions of this alloy in bulk form using the (CZ) or other methods[1-6]. Si-Ge alloys are of interest because they have higher carrier mobility than silicon, and can be produced with bandgaps between those of silicon and germanium. Uses for large diameter substrates include epitaxy research, photodetectors, solar cells, x-ray detectors and analyzers, high performance heterostructure transistors and diodes, thermoelectric devices, and ultimately, high performance integrated circuits.

Experimental Procedure

An RF-heated CZ furnace was used to grow the Si-Ge single crystals. A silica crucible 18 cm in diameter was filled with either silicon and germanium pieces or previously solidified Si-Ge alloy to provide a total charge of 1500 gms. Helium was introduced into the furnace chamber and maintained at a pressure of one atmosphere. After heating for about one hour to form a Si-Ge liquid solution and removing surface contamination, the temperature was stabilized above the liquidus for the corresponding charge composition.

A silicon seed was used that was large enough to insure that the diameter of a Si-Ge single crystal would be no more than 15 mm smaller than the maximum diameter of the seed. As will be discussed later, this excess seed diameter was needed to allow for a slight diameter reduction at the start of growth and the removal of up to 5 mm of polycrystalline material which may have grown at the periphery of a boule.

The silicon seed was rotated at a constant rate between 5 rpm and 14 rpm; the crucible was rotated at a constant rate in a clockwise or counterclockwise direction between 4 rpm and 20 rpm. The seed was lowered to a position just above the surface of the alloy liquid for at least 15 minutes for preheating and then immersed to a position where the liquid surface coincided with the maximum diameter of the seed. After a meniscus formed, the temperature was adjusted and pulling began at no more than 2 mm per hour. The crucible was not lifted and, as pulling continued, the growing alloy body diameter became slightly smaller than the maximum seed diameter. Thereafter, the body diameter could be controlled by slowly lowering the temperature.

After growth, the boule was raised slightly above the liquid surface and furnace cooled. There were times when multiple boules were grown in a single batch crystal growing process by utilizing more than one seed. In

those cases, shorter boules were produced and only the last grown was furnace cooled. The others were raised slowly from the hot zone and kept for one hour inside the bellows before being cooled to room temperature outside the furnace.

Wafers cut from the Si-Ge boules were edge rounded, etched in KOH to remove saw damage and to delineate polycrystallinity, and polished either on one or on both sides for evaluation. The back-reflection Laue method was used to determine crystallographic orientation and the surface smoothness of polished wafers was evaluated by Atomic Force Microscopy (AFM). Polished wafers were etched for 10 minutes in a modified Schimmel etch (ASTM F47-87) to reveal resistivity striations and to determine defect density and distribution by optical microscopy. Chemical composition was determined either by calculating density, by energy dispersive X-ray (EDX) spectroscopy, or by Vis-UV absorption. Conductivity type was determined by the hot-probe method (ASTM F42-87), and electrical resistivity was measured using the four-point probe method (ASTM F84-84a).

Results

High quality SiGe substrates have been produced in diameters up to 50 mm, and with compositions ranging from 3%-17% Ge (at%). Most of the Si-Ge single crystals were grown with a (100) crystallographic orientation, but (111), (110) and (211) crystals were also produced. Both single-side and double-side polished wafers were successfully produced.

A 50 mm diameter Si-Ge single crystal was the largest grown. Crystals were either n-type (7-59 ohm cm) or p-type (22-67 ohm cm) as a result of the relative distribution coefficients of impurities coming primarily from the crucible, the germanium, and the silicon. Vis-UV measurement indicated the same bandgap at different positions across a 50 mm wafer and large area AFM scans revealed no features greater than 2 nm high on a polished surface.

Since the Si-Ge system exhibits a large liquidus-solidus gap, low pulling rates, usually well below 2 mm per hour, are needed to prevent the onset of dendritic growth. Standard pulling rates to grow elemental silicon from its melt are on the order of 2-10 cm per hour. Thus, when using a conventional CZ method for growing a Si-Ge single crystal, it can take forty times longer than it does for silicon to grow a cap to the same diameter. Since the total process time for CZ growth is limited by dissolution of the silica crucible and build up of oxide at various locations within the growth chamber, it is advantageous to reduce the time for cap growth as much as possible.

Although it was possible to pull slowly enough to avoid dendritic growth using a standard CZ technique without necking, it was found difficult to significantly increase the Si-Ge single crystal diameter because of the formation of polycrystallinity at the cap circumference. Since CZ growth of a Si-Ge alloy can be viewed as solidification of the alloy from solution in germanium, and high quality single crystal material can be grown over large areas from molten metal solution[7], it was conjectured that a single crystal silicon seed having a diameter equal to the intended diameter of the Si-Ge single crystal could be used as a template to initiate growth. Diameter control would then be obtained by proper adjustment of growth parameters. The silicon seeds that were used were obtained by growing single crystals in a separate process or by using caps cut from single crystals which had been grown for other purposes.

Although use of a large diameter seed eliminated problems associated with cap growth, a problem that was introduced was

fracture on cooling caused by the thermal expansion difference between the silicon seed and the Si-Ge alloy. For higher germanium content crystals, use of a Si-Ge single crystal seed having a composition slightly richer in silicon that of the alloy to be grown would prevent such fracture. For the alloy compositions that were grown, fracture did not occur until boule diameters exceeded 25 mm. For larger diameters, fracture could be eliminated by more carefully controlling the cooling rate, for example, by furnace cooling.

The polished and etched wafers were Schimmel etched to exhibit resistivity striations and defect density distributions. These features are related to the interface shape and mixing within the liquid resulting from the imposed seed and crucible rotations. Concentric resistivity striations occurred when the seed and crucible were counter-rotated. When iso-rotated, non-concentric resistivity striations were produced. It was observed, however, that the pattern of defects did not necessarily follow striation patterns. An average defect density of 5×10^4 per cm^2 was measured. Defects having the appearance of stacking faults as well as isolated areas of cellular structure were observed on wafers cut from boules that had not been furnace cooled. This was an indication that strain produced by radial thermal gradients during cooling had not been fully relaxed. Post-growth annealing of these boules would be useful in preventing fracture that would otherwise occur upon grinding and cutting.

Both EDX and Vis-UV Absorption analysis showed less than 2% composition variation across the 50mm (2") diameter. Similar variations were observed along the growth direction over approximately 1" of crystal (about 15-20 wafers).

Conclusion

Czochralski crystal growing technique was used to produce large diameter Si-Ge bulk single crystals with concentrations of up to 17 at% germanium. The use of a pregrown large diameter seed as a single crystal template for alloy solidification was found to save time and insure single crystallinity at the desired crystal diameter. The growth of even greater than 50 mm diameter Si-Ge single crystals with compositions covering the entire range from pure germanium to pure silicon should be possible using the technique described here, and are under investigation. The Authors R.H.D. and T.G.D. have 1 US Patent Pending on the CZ technology described here for growing SiGe.

Acknowledgements

The authors thank R. Bromme, M. Shelton, L. Holder and K. Heath for crystal growing assistance.

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Electrical characterization of silicon nanocrystals grown from thermal annealing of LPCVD SiOx

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Introduction:

The use of silicon nano-crystals embedded in SiO_2 is a possible way to reach the requirements for low power and low consumption memory cells. Theoretical calculations have shown that silicon quantum dots with nanometer size (≈2nm) could act as floating gates able to trap only one electric charge, thanks to the Coulomb blockade phenomenon. Therefore, an important work is actually devoted to the fabrication of such quantum dots with the aim of obtaining both small sizes and high densities. Si dots nucleation can be obtained directly during a chemical vapour deposition process using only SiH_4 [1,2]. The alternative techniques consist in making silicon precipitates with post deposition annealing steps. These techniques need the formation of a Si-rich oxide, which can be obtained by ion implantation of SiO_2 [3]or by direct deposition by CVD of SiO_x layers with $x<2$ [4]. The present work is focused on the electrical properties of Si-dots obtained by this last technique which allows a well-controlled bulk distribution. Using current-voltage and capacitance-voltage measurements, performed at low (90K) as at room temperature, we have studied the conduction mechanisms in oxide matrices containing silicon nano-crystals. Furthermore, in this work, the charge retention capability of the quantum dots are investigated at room temperature.

Experimental details:

In the past, SiO_x films have been used as a passivation layer for silicon devices The LPCVD growth mechanism of such layers was extensively studied by Hitchman et al., which were obtained by a chemical reaction of SiH_4 and N_2O at a surface substrate [5]. More recently, it has been demonstrated that the annealing of SiO_x ($x<2$) layers lead to the formation of silicon nano-crystallites, which could exhibit interesting optical and electrical properties [6]. The samples studied in this work consist in p-type 8'' silicon wafers which have been thermally oxidised in order to obtain a 24 nm-thick SiO_2 layer. This first thermal oxidation is required for all the samples in order to have a good Si/SiO_2 interface. After this first oxidation step, a 55nm-thick SiO_x layers (named hereafter **sample #A**), with $x=1.3$, is deposited by CVD at 650°C. Then, a thermal annealing at 1000° C for 30 min is used in order to form the Si nano-crystals by precipitation. A reference sample (named hereafter **sample #B**) without annealing has been made for comparison. A second reference consisting only in a 90nm thermal oxide on Si (named hereafter **sample #C**) has been also processed for the study of the SiO_2/Si system. Figure 1 shows a high-resolution TEM view of the obtained nano-crystals for sample #A, which have an averaged diameter between 4 and 6 nm. The interfacial composition between the nano-crystals and the oxide matrix remains an important point that surely requires further characterisations. In our samples, aluminium gates have been added by evaporation in order to obtain MOS capacitors suited for electrical characterisation. A schematic view of samples #A and #B is shown in Figure 2.

Current-voltage characterisation:

Figure 3 shows the current densities as a function of the electric field measured at 90 K and 300 K for sample #A as well as for the reference sample #B. Several observations can be made from this figure:

- A more important leakage current is obtained for the reference sample #B as compared with the annealed sample #A with Si-dots. This is explained by the poor dielectric properties of the not-annealed SiO_x layer which contains a high density of states introduced by the Si atoms.
- In the case of the reference sample #B, the conduction mechanism is strongly thermally activated. The threshold electric field increases at low temperature for the reference sample while it remains quite constant for the sample with precipitated quantum dots. This result indicates that the conduction phenomena are different for the two structures.

We suggest that the conduction process in the not-annealed SiOx layer (sample #B) can be explained by a Poole-Frenkel mechanism. In fact, a Poole-Frenkel current can be expressed by the following equation:

$$J_{PF} = A \cdot F_g \cdot \exp\left[\frac{\sqrt{\frac{q F_g}{\alpha \varepsilon \pi}}}{kT}\right] \quad \text{(eq. 1)};$$

were F_g is the electric field, q is the electric charge of the electron, ε is the dielectric constant, A is a proportionality constant, and α is a constant which depends on the distance between traps [7]. The fit between experimental data and theory obtained at 300K for sample #B is shown in Figure 4, which illustrates the plot of the current density divided by the electric field, in a logarithmic scale, as a function of the field square root. The slope of the curve obtained from this fitting has been used to extract the parameter α. The plot obtained at 90K is also linear and it gives exactly the same value for α. Finally, we can conclude that the current in a not-annealed SiO_x layer is controlled by a thermo-ionic emission from trap to trap with an average distance of 1.7 nm between traps (as extracted in our samples from the α value).

Data obtained for the annealed sample (sample #A) cannot be fitted by a Poole-Frenkel model, confirming that the conduction process has been modified after the annealing. In order to explain the conduction in such a sample, we have used the hopping model which involves direct tunnelling from trap to trap. In this model, the current density is given by:

$$J_H = A \cdot F_g \cdot \exp\left[\frac{\frac{d}{2} \cdot F_g}{kT}\right] \quad \text{(eq. 2)};$$

were d is the distance between traps. In this case, the slope of the curve $\ln(J_H/F_g)$ versus F_g allows to extract the parameter d. Figure 5 shows the fit obtained at 300 K using this model. An average distance of 2 nm between «traps» has been deduced from this graph.

Capacitance-voltage characterisation:

C-V measurements have been performed in order to study the charge trapping properties of the silicon dots. To put in evidence the effect of the nano-crystals we have compared the measurements obtained on samples #A and #B. The characterisations have been realised at two different temperatures, 90K and 300K, in order to study the influence of temperature. The verse and amplitude of the voltage sweep has been varied ($\pm 3V \rightarrow \mp 3V$ or $\pm 10V \rightarrow \mp 10V$) and repeated sweeps have been performed for the study of the flat band (V_{FB}) variations. Figure 6 shows the comparison of C-V curves obtained while varying the polarisation from a positive bias (inversion) to a negative bias (accumulation) for both samples at 90K and 300K.

Relative dielectric constant of the SiO_x layer: The value at 300K of the accumulation capacitance C_{Acc} for sample #B has been used to extract the relative dielectric constant of the $SiO_{1.3}$ layer, which is found to be $\varepsilon r_{SiO1.3} = 7$. This has been done by considering the equivalent total thickness of the dielectric which is made by a first thermal SiO_2 layer followed by the $SiO_{1.3}$ layer, as extracted by TEM measurements.

Effect of temperature: No variation of V_{FB} with temperature is observed for the reference sample #B and a small variation is measured for sample #A. The decrease of C_{ACC} at low temperature could be explained by a series resistance effect.

Repeated sweeps: A variation of V_{FB} of 0.84V is observed for the reference sample #B when the measurement from +3V to –3V is done just after a scan from +10V to –10V. This suggests that the SiO_2/Si interfacial states and/or SiO_x states may play an important role. Measurements performed on the reference sample #C, which is a pure SiO_2/Si MOS capacitor, have shown that no flat band variations are obtained either by changing the polarisation scanning or the temperature, so that the substrate interfacial states can be excluded from our interpretations. These kind of measurements have also shown that the ΔV_{FB} is more important (1.62 V) on sample #A than in the reference sample #B. This indicates an influence either of the initial traps of SiO_x which are not suppressed by thermal annealing or of the Si-dots themselves. Indeed, it is probable that we observe a combination of both phenomena.

Comparison between Si-dot sample and reference: A ΔV_{FB} difference value of 1.63V is obtained between samples #A and #B, as shown in Figure 6. These measurements have been done from inversion to accumulation conditions without any stress. The value of ΔV_{FB}=1.63 V is comparable to the one obtained for sample #A when the influence of successive scans was analysed. The total bulk charge of the Si-dot oxide can be relied either to the dots themselves or to other electronic states between the dots. The comparison of sample #A and #B shows a clear contribution of the Si-dots. A simple calculation of the charge density gives a value of 9.10^{16} #e^-/cm^3 which is consistent with the dots density estimated by TEM observations.

Conclusions:

I-V and C-V measurements performed on MOS capacitors containing silicon quantum dots, at low (90K) as at room temperature, have shown interesting electronic properties of Si nano-crystals embedded in a dielectric matrix. The possibility of charge retention at 300K in the Si-dots is observed, indeed proving the *potentiality of such materials for memory applications.*

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Figures:

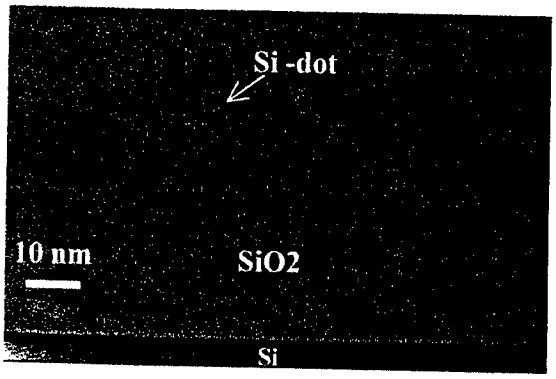


Figure 1: TEM view of the SiOx/SiO2/Si structure annealed at 1000°C – 30 min. Si-dots with average diameters of 5 nm are formed.

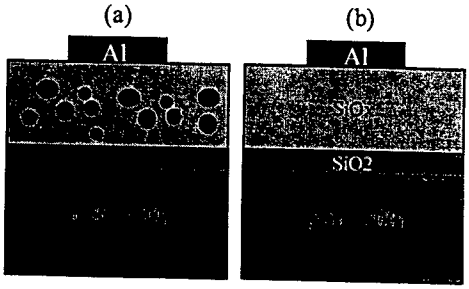


Figure 2 : Schematic view of MOS capacitors formed on sample #A (a) and the reference sample #B (b).

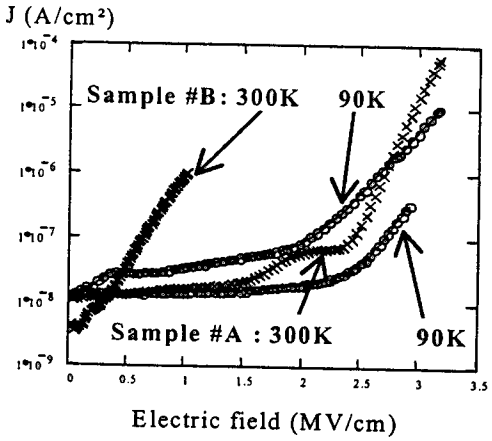


Figure 3: Current density vs electric field for samples #A and #B at 90K and 300K.

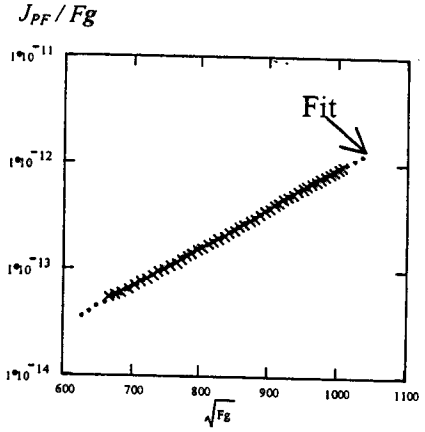


Figure 4: Current density J_{PF} divided by electric field F_g vs the square root of the electric field for sample #B at 300K.

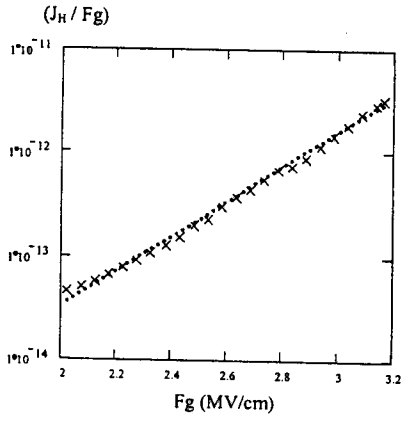


Figure 5: Current density J_H divided by electric field F_g vs electric field for sample #A at 300K.

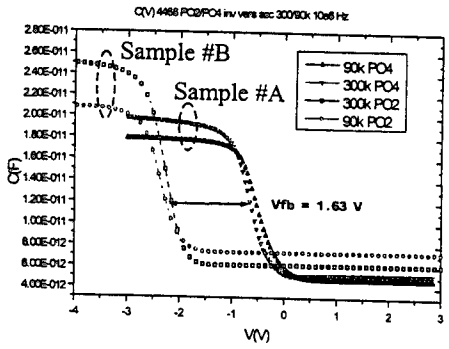


Figure 6: C-V curves recorded at 1 MHz for samples #A and #B at 90K and 300K.

Carrier emission and capture mechanism study of germanium nanostructures embedded in silicon

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Introduction:

The use of quantum dots (QDs) is a possible way to improve the quantum efficiency of the optoelectronic devices thanks to the three-dimensional confinement effects. This is specially interesting in the case of silicon-compatible materials such as silicon-germanium alloys were the quantum dots effects are expected to improve the performances of optical devices. In fact, for indirect band gap materials such as SiGe alloys, it is possible to improve the optical properties when a spatial localization of carriers can be achieved. For instance, radiative transitions without phonons are observed in SiGe layers thanks to the spatial localization of excitons due to local potential fluctuations. Nevertheless, this property of SiGe is not sufficient for reaching the requirements of an optoelectronic device. Several attempts, including two-dimensionnal confinements in quantum-well devices or the use of Si/Ge superlattices have been realized for the improvement of the quantum efficiency of Si-based devices. After a number of experiments with quantum-wells or superlattices, it seems obviously not a well suited approach for a drastic improvement of the optical properties. One of the major problems in this system is the limited values of band offsets wich are determined by the Ge concentration. Indeed, it is not possible to increase the band offsets by increasing the Ge content because of critical thickness considerations. Thus, the total volume of the active layer as well as its average Ge content is limited and this explains why the devices have good characteristics only at very low temperatures. In this context, a special attention has been devoted to the possibilities offered by the growth of quantum dots in the SiGe system. Several studies have shown that SiGe dots [1,2] and even pure Ge dots [3,4] embedded in silicon could be formed by self organized techniques. The use of such materials could be an alternative way of making high efficiency devices, because high Ge contents could be obtained without plastic relaxation in the dots. Interesting optical properties have been obtained for such materials up to room temperature, however, a good control of very small quantum dots with high densities is still required for a possible use in Si-based optoelectronics.

In this work, we focuss on the electrical study of pure Ge dots in silicon grown by UHV-CVD. The aim of the study is to get more information about the electronic properties of such nanocrystals and to evaluate the effects of size distribution. For that purpose, capacitance-voltage measurements have been performed in the 77-300 K temperature range as well as deep level transient spectroscopy which is used in order to study the carrier emission process from the Ge nanocrystals.

Experimental techniques:

The growth of the samples is carried out in UHV-CVD conditions. Pure SiH_4 and hydrogen-diluted (10%) GeH_4 were used as gas-souces for Si and Ge layers respectively, while p-type boron doping is obtained using diborane (B_2H_6). The base pressure of the chamber is better than 1×10^{-10} Torr, the pressure during growth is around 5×10^{-3} Torr. More details concerning the growth are given elsewhere [4]. Figure 1 shows the structure of the samples. The growth temperatures are 550°C and 600°C for Ge and Si layers respectively. First, a

highly boron-doped 10 nm-thick Si buffer layer is grown on p-type (001) silicon wafers, then a 100 nm-thick silicon layer with a boron doping level of 5 x 10^{16} cm^{-3} is realized before the deposition of the dot's layer. The Ge dot's layer is undoped as well as its two adjacent 10 nm-thick spacer layers. For a deposition time of 240 s at 550°C, an average dot size of 100 nm is expected with a density of about 1 x 10^{10} cm^{-2} [4]. After the undoped dot region, a 200 nm-thick boron-doped cap layer is grown with a doping level of 5 x 10^{16} cm^{-3}. Finally, a undoped silicon cap layer is necessary in order to form a good aluminum Schottky contact for space charge characterization techniques.

Capacitance-voltage measurements:

Figure 2 shows C-V curves recorded at 1 MHz for various temperatures ranging from 80 K to 290 K. The hole concentration profile deduced from the C-V measurement at room temperature is given in figure 3. This carrier profile shows a peak around 190 nm. The doping level and the thickness of the cap layer extracted from this curve are to 4 x 10^{16} cm^{-3} and 190 nm respectively. These values are in very good agreement with the target values. So the observed peak is attributed to the accumulation of holes in the dot's region. The peak observed in the carrier profile is shown as a shoulder between 0.5 V and 1.2 V in the C-V curve. For reverse biases above 1.2 V, the dots are emptied. Nevertheless, as the emission process of holes from the dots is thermally activated, the dots should be filled of carriers for very long durations at low temperatures. Indeed, at these temperatures, the emission process is very slow and the hole concentration within the dots can not follow the 1 MHz modulation signal.

Since the capacitance-meter DLTS setup operates at 1 MHz, it is easy to deduce the experimental conditions for the reverse bias and the filling pulse height directly from the C-V curves.

Deep Level Transient Spectroscopy:

In order to study the thermal emission of holes from the Ge dots, it has been necessary to establish the possible influence of deep levels in our samples. Therefore, we have first compared the DLTS spectra obtained when the total thickness of the epilayer is probed with the spectra obtained when the emission of holes from the cap layer or from the dot's region has been favored.

- Influence of the cap layer: A reverse bias of Vr = - 1V is used with a filling pulse of Vp = 0V as indicated on figure 4. Two main peaks around 120 K and 200 K are well observed and a shoulder above 220 K can be distinguished for the emission rate window of 465.1 s^{-1}. For these experimental conditions the dots partly influate the spectra because the reverse bias of - 1V is not sufficient for a good depletion of the dot's layer. For this reason, the two main peaks of figure 4 are rather linked to bulk silicon deep levels or to Al / Si interfacial states introduced during the Schottky process.

- Influence of the dot's layer: A reverse bias of Vr = - 1.5V is used with a filling pulse of Vp = - 1V. In that case illustrated by figure 5, only one peak around 220 K is obtained. As the cap layer is nearly not probed in these conditions, we attribute this signal to the dot's layer. When experimental conditions are choosen in order to probe both the dot's and the cap layers, we do not observe simultaneously the deep levels of the cap layer and the dot's signal. This is shown in figure 6 which is recorded with Vr = - 1.5 V and Vp = 0V. In fact, the DLTS signal shows a high temperature region identical to the dot's signal with a very large broadening on the low temperature side. The whole signal is probably only du to the dot's layer in such conditions, indicating that the trapping kinetics is faster for the Ge dots than for the silicon deep levels. This is confirmed by measurement performed with a filling pulse Vp = - 0.5 V as shown in Figure 7. The broadening on the low temperature side is less pronounced and the spectra have

a square shape. Once again the peak related to the cap layer at T = 120 K is not observed. The square signal is then only associated to the dot's layer. Such a DLTS shape as been already oberved in SiGe dots samples [5] and can be explained if one consider an energy distribution of the confined levels. In this model, the high temperature part of the spectrum is linked with the deeper states obtained for thicker wells, while the low temperature side is attributed to the thinner wells. The thicker wells in our case are obained in the Ge dots which have an average thickness of about 15 nm and an average base diameter around 100 nm. The thinner wells are located in the regions between the dots. In these parts of the Ge layer, the confinement energy is very important, and thus, the activation energy coresponding to the difference between the confined state and the silicon valence band is very weak. It is also possible to consider that smal dots have an influence at low temperature, nevertheless, the small size variations of the dots (5%) could not explain such an extention of the spectra.

- Influence of the filling pulse duration: The model of a DLTS signal arising from Ge dots and from the 2D Ge-layer can be more supported if the signal does not show the same behaviour at high and low temperatures when the pulse duration is changed. The result presented in figure 8 is a comparison of the spectra obtained for filling pulse durations of 10 µs and 100 µs. For short filling durations, the broadening at low temperatures is very important, while for longer durations, only the high temperature part of the spectra remain. This point is especially obseved for important emission rate values (4651.16 s^{-1}) which give a DLTS peak at high temperatures. These measurements indicate that the trapping kinetics are not the same in the whole range of temperature. The observations are in favour of a trapping mechanism in all the Ge layer (2D and dots). The emission of holes can be observed from the 2D Ge layers which have a large thickness distribution only for short filling pulse duration. For long filling durations, the holes trapped in the 2D layer have enough time to diffuse towards the Ge dots before being emitted.

- Confined level of the 100nm-Ge dots: The best conditions for studying the Ge dots have been deduced (those of fig. 5) and and activation energy of 0.53 eV as been obtained. This value corresponds to the hole ground state within the Ge dots and is in the same order of that obtained by Zhang et al. [6] (0.41 eV) for 25 nm Ge dots. In our samples 100nm-Ge dots should have a lower confinement energy and this explains the higher activation energy. No Coulomb charging effect is expected in our dots while in the case of 13 and 25 nm-Ge dots, these effects are observed [6]. Simples calculations from our C-V measurements have shown that a few tens of holes are trapped by each Ge dot.

Conclusion:

The trapping and detrapping mechanism of holes in 100-nm Ge dots as been studied carrefully by C-V and DLTS. It is shown that Ge dots are efficient hole traps. A thermal activation of 0.53 eV is measured for the DLTS peak which appears above T = 220 K. Further investigations are required on n-type samples in order to give accurately the band alignment between Si and Ge dots, nevertheless, these firts results show the interest of pure Ge dots for the room temperature operations which is required for Si-optoelectronics.

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[2] Schittenhelm et al., Thin Solid Films 294 (1997) p.291
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[4] Le Thanh et al., Phys. Rev. B 58 (1998) p. 13115
[5] Chrétien et al., J. Appl. Phys. 78 (1995) p. 5439
[6] Zhang et al., Phys. Rev. Lett. 80 (1998) p. 3340

Figures:

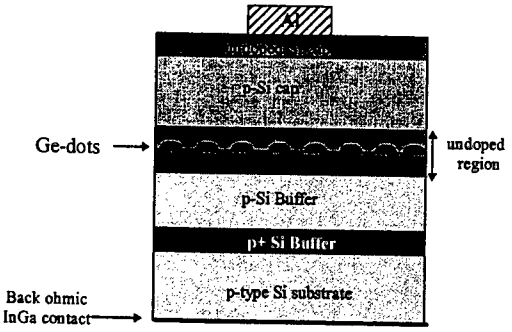


Figure I : Structure of the samples

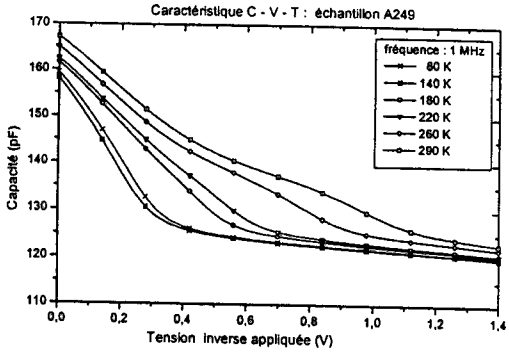


Figure 2: C-V curves (F=1MHz) at different temperatures.

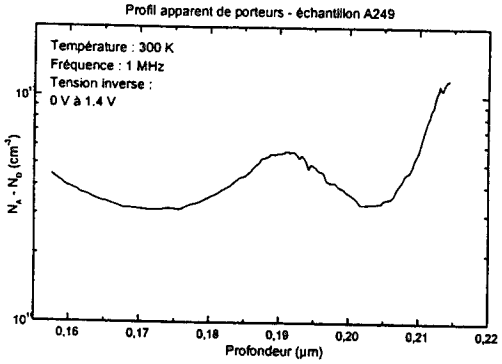


Figure 3 : Carrier profile obtained from room temperature C-V measurements.

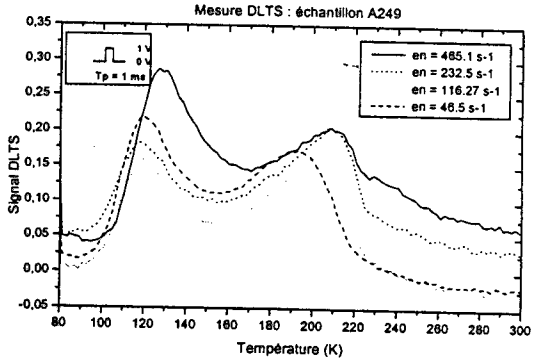


Figure 4 : DLTS spectra of the cap layer

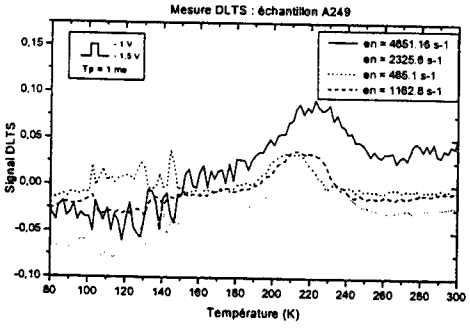


Figure 5: DLTS spectra of the Ge dots

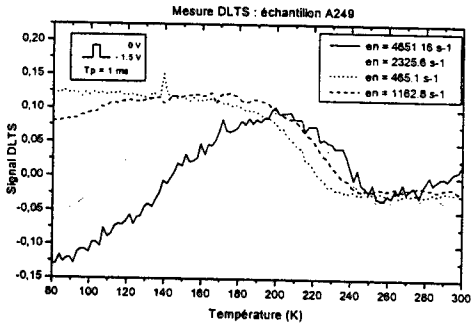
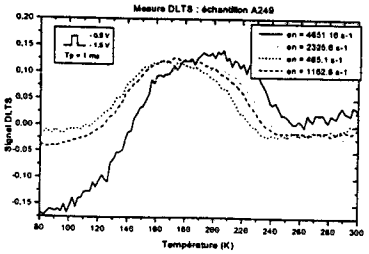
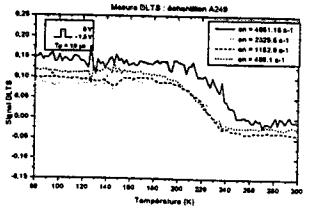
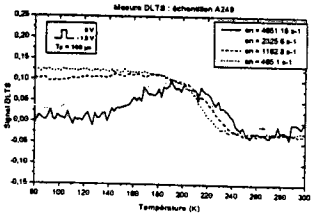


Figure 6: DLTS spectra of dot's and cap layers







Optical Thickness Mapping of Micromachined Silicon Substrates

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Introduction

Bulk Micromachining of silicon using wet-chemical etching or dry-reactive-ion etching is the critical processing step required in the fabrication of pressure sensors, accelerometers, gyroscopes, millimeter-wave waveguide structures, and other microelectromechanical devices. In many applications the absolute thickness of a silicon membrane determines the ultimate performance of the device. As an example, the thickness of micromachined membranes used in pressure sensing devices controls the pressure range and measurement resolution of the device.

Often, deep etching and micromachining of silicon substrates to depths of 5-400 um is required. Therefore, a nondestructive and rapid analysis tool for mapping and monitoring the thickness of etched membranes is needed. Rapid thickness mapping over broad sensor areas up to several millimeters is of interest in many applications. Also, sub-micron thickness resolution is needed since most applications require the membranes to be uniformly etched to within fractions of a micron.

In this paper, we describe an optical instrument (Optical Micrometer for Micromachined Substrates) capable of mapping membrane thickness over a 5mm x 5mm area with 0.2 um thickness resolution.

Instrument Design and Theory of Operation

The technique used to calculate silicon thickness is based on the absorption of light passing through the etched membrane. It is well know that the intensity of an optical signal monotonically decays as it transmits through silicon provided the photon energy is greater than the optical bandgap (about 1.1 eV) [1]. Therefore, the strength of the transmitted signal decreases as the silicon thickness increases. By carefully controlling the intensity of the input optical signal it is possible to calibrate the detected intensity of the transmitted signal to the thickness of the silicon. By using an input laser beam passing through the silicon, and a CCD array detector to monitor the transmitted beam one can actually map the transmitted beam intensity and subsequent map the silicon thickness.

The system described here uses a semiconductor IR laser with beam expanding and conditioning optics as the input analyzing-beam. At the exit side of the silicon wafer is a high performance CCD array digital video camera. The input laser power is automatically adjusted and controlled using virtual software instrumentation provided by LabView [2]. Similarly, the detected image from the camera is

captured and digital-signal-processed using LabView hardware and software. By controlling the laser power, and using a series of digital signal processing algorithms to reduce noise and variance in the detected image, one can calibrate the pixel intensity to the thickness of the silicon. Therefore, as the beam passes through the etched silicon membrane, the pixel-by-pixel signal intensity of the exiting beam received by the camera can be directly transformed into a thickness map for the silicon membrane.

Since the thickness is correlated to bulk absorption, the silicon must be mirror smooth on both surfaces to avoid strong surface absorption. Therefore, the system described here is only intended for structures etched into double-side-polished silicon.

Given that the system maps the absolute thickness of the silicon structure, both thickness and step-height can be analyzed; also, both the front-side and backside etch step-heights can be determined from the thickness map.

Results

Using a 480 x 640 pixel 10-bit camera, image integration, and a series of 7 x 7 pixel spatial filters we have been able to reproducibly and reliably map silicon membrane thickness; the field of view for the camera is about 5mm x 5mm wide allowing for large area thickness maps; the x-y resolution over the 5mm x 5mm map is about 50 um. Higher resolution can be achieved using a larger CCD array, and a smaller field of view. Thickness resolution for this technique is approximately 0.2 um with excellent reproducibility over time. The thickness measurement range is 5 – 500 um. Thickness maps are easily displayed to a computer monitor using LabView.

Conclusion

Mapping Si-membrane absolute thickness for micromachined structures has been demonstrated. The technique is based upon optical absorption within the silicon proportional to the silicon thickness. Reliable and reproducible measurements of silicon thickness with 0.2 um resolution have been demonstrated. The authors thank Thomas Digges, Jr. for many helpful discussions, and Virginia Semiconductor, Inc. for support of this project. The Authors S.H. Jones and R. Ross hold two US Patents and 1 US Patent Pending on this Optical Micrometer Technology.

References

[1] T. Globus; S.H. Jones, T. Digges, Jr., *Analysis of Refractive Index and Absorption Coefficient of Silicon Membraness*, Proceedings of the 1997 International Semiconductor Device Research Symposium, Charlottesville, Virginia (December 1997).

[2] LabView is a software program for creating virtual instrumentation, virtual circuits, and complex signal processing algorithms using the high level programming language, G. LabView is a commercial product sold by National Instruments.

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ABSTRACT

Since the dawn of civilization man has endeavored to analyze and understand the nature of the universe and his environment. In the last 100 years (based on a multitude of discoveries and inventions over the centuries) there has been a tremendous increase in the understanding of the basic sciences such as physics, mathematics, chemistry, biology and materials. Based on this understanding we have developed tools and technologies which have made a significant impact on our daily lives.

The invention of the transistors, quickly followed within a decade by integrated circuits, created the world of microelectronics and ushered in a second industrial revolution based on an intense exploitation of knowledge and information.

Moor's Law has stood the test of time for over two decades. The Semiconductor Industry Association (SIA) roadmap projects that by the year 2012 devices with feature sizes on the order of 50 nm will be routinely manufactured, allowing integration of more than 20 million logic gates on a single chip. To date, most advances have focussed upon top-down approaches, "making large things small". However, beyond the year 2012, this approach becomes less viable as a result of lithography and other fabrication tool limitations. Continuing progress in the reduction of gate feature-size is unlikely without radical changes in approach to miniaturization. Such an approach might capitalize upon the increasing confluence of the biological and nanoelectronic research communities. The scientists and engineers are starting to learn how to harness the self-assembly features of biological molecules, to enable the self-assembly of molecular-scale devices. In addition to the overlap between micro/nanotechnology and biology, there is also confluence and overlap with the information technology. The three technologies provide a wealth of opportunities for research and development for the science and engineering communities for the new millennium.

We will be presenting some of the interdisciplinary programs initiated by National Science Foundation in support of crossing of these technological streams. These include programs such as nanotechnology, engineering microsystems, and biosystems at the nanoscale level.

Panel I: Enabling Technologies for the New Millenium

Jim Prendergast
Vice President and Director
Physical Sciences Research Laboratories
Motorola Labs

CMOS processing, as we currently know it will come to an end within the next 20 years but CMOS will remain alive and well. Optical lithography at 157nm will happen, although 126nm is very questionable and other lithography solutions such as EUV or multi-ebeam will likely assume the baton. Solutions are already in sight to replace silicon dioxide gate dielectrics with very high permittivity dielectrics and the polysilicon gates with metal gates. Bulk silicon substrates will be replaced by thin-film SOI substrates. In addition, numerous engineering challenges such as source-drain tailoring, and circuit challenges with multi-threshold and dynamic threshold devices will be overcome. Exotic packaging solutions will become more common such as die-on-die solutions and free space optical interconnects. Nevertheless, CMOS processing can still be regarded as following a traditional "top-down" approach. That is, small structures are made on large wafers through lithography & etch. An alternative approach is emerging in which individual molecules are used to fabricate device and circuit components. Molecules are inherently nanoscale in size and uniform in nature. Furthermore, organic and inorganic molecules can be synthesized with unique chemical, physical and biological properties that could be used to promote self-assembly to one another and to specific surfaces resulting in logic and memory functions. Molecular electronics is a "bottom-up" approach of building what you need rather than eliminating what you don't. It has the potential of reaching sub-10-nm dimensions, and may impact mainstream products beyond the 20-year horizon.

Abstract

HIGH QUALITY, LOW NOISE III-N PHOTODIODES

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ABSTRACT

Low noise, highly efficient ultraviolet photodetectors are critical components in applications such as UV astronomy, flame sensors, pollution monitoring, and early missile warning systems. The development of the devices is best realized in a continuous feedback process involving alternate advancements in the material technology and the subsequent device design. We present the growth and characterization of very high quality GaN p-i-n photodiodes, grown by low-pressure metal-organic chemical vapor deposition. The room temperature spectral response shows a high responsivity of 0.20A/W up to 362 nm, above which the response decreases by five orders of magnitude. The analysis of the current voltage characteristics and the capacitance behavior with frequency and voltage provide feedback about the GaN material. An analytical model is used to compare the theoretical spectral responsivity to the experimental results for a fit of material constants such as the minority carrier diffusion length. The noise of the detector is below the noise level measurable by standard measurement systems. Therefore, high voltage noise measurements are used to extrapolate the noise conditions at zero bias. Certain characteristics, such as leakage current, noise and speed performance, are thought to be limited partly by the quality of the material, more specifically the presence of defect-related states in the depletion region. Therefore, additional AlGaN p-i-n devices grown on LEO and double LEO material are also investigated to provide a comparison to AlGaN p-i-n devices grown on normal template layers. The material characterization, fabrication techniques and device performance are presented, including spectral response, current-voltage characteristics, and capacitance analysis.

ABSTRACT

The Enabling Aspects of the Precise Control of Time

Max N. Yoder

Incremental True-Time-Delay-Steered (TTDS) apertures have significant system advantages over conventional Phase-Shift-Steered apertures, parabolic dish antennas and horn antennas. If implemented with conventional E/M delay lines, there are problems with size, dispersion and attenuation as a function of delay. Photonic delay lines overcome the attenuation problems, but introduce additional problems of dynamic range, intermodulation products, and the span of delay required (e.g., sub-picosecond to many nanoseconds). Size and cost are also significant problems with photonics. Only Direct Digital Synthesis (DDS) technology appears to provide all of the advantages of TTDS apertures with no systematic disadvantages. Precise control of time (in short duration) and phase, however, is required and this requirement leads to very stable master oscillators at 100 GHz with phase noise no greater than 30 femtoseconds. It also demands that amplifiers and any other componentry in the transmit and receive chains also exhibits exceptionally low phase noise and low 1/f noise.

While short duration time control is essential for beam steering, one must also control time over an extended period if multistatic radar is to become viable. With precise knowledge of time and position, any target moving in a volume illuminated by properly encoded E/M signals can be detected by any passive platform possessing the proper encryption codes. The corollary of this is that every platform in a given area instantly, intrinsically, and inherently possesses the common tactical picture without the need of establishing dedicated communication channels to relay such information. To implement this concept, miniature atomic clocks with exceptional accuracy and low power consumption have been and are continuing to be developed.

Finally, our ability to conduct surveillance in the presence of clutter or jamming as well as our ability to communicate in the presence of jamming is dependent on our ability to exploit broad instantaneous bandwidths in an orthogonal, non-interfering manner and to correlate signals in these broad bandwidth signals at speeds commensurate with high data rates. To do this requires exceptional control of time and phase stability.

THz Photomixing Sources: Principles and Progress*

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Abstract

Several ultrafast photoconductive materials (e.g., low-temperature-grown GaAs) offer sub-picosecond photocarrier lifetime, high breakdown electric field (> $5x10^5$ V/cm), and can be grown in epitaxial films having excellent quality for submicron lithography. After fabricating in a THz antenna-coupled integrated circuit, such materials can be pumped by two frequency-offset diode- or solid-state laser beams to generate cw highly-tunable THz radiation. This presentation summarizes the operational principles and performance characteristics of such "photomixer" devices in contrast to a competing electronic devices such as harmonic multipliers and solid-state power amplifiers (SSPAs). An emphasis is placed on new photomixer structures (e.g., vertical- cavity and traveling-wave structures) that could increase the THz output power well above the present μW levels by increasing the external quantum efficiency and improving the thermal management.

* This research is being supported by the Defense Advanced Research Projects Agency (Dr. Edgar Martinez) through a Grant administered by the U.S. Air Force Research Lab (Dr. John Loehr).

The Beginnings of a Practical Terahertz Technology

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Research Professor
Director, Semiconductor Device Laboratory
Department of Electrical Engineering
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Charlottesville, Virginia

As we approach the end of the 20th Century, terahertz technology remains the domain of scientific researchers. However, new, broader programs such as NRAO's Atacamba Large Millimeter Array and ESA's Far-Infrared and Submillimeter Telescope require a new generation of technology. Sources and receivers must be broad-band, electronically tunable and highly robust. Also, repeatability must be improved and costs must be minimized. If these goals can be achieved, other applications, military, medical, industrial and commercial, can become viable. Integration is the key. Already several groups are developing quasi-integrated receivers and sources and micromachining promises to make waveguide components cheaper and more broadly available. If resources can be focussed on practical technologies that have at least some chance of success, in five to ten years we can create a technology base that will allow the terahertz frequency band to become as useful as the microwave and IR bands are today.

Ultra-Broadband Receivers for the Terahertz Region

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Chalmers University of Technology, SE-412 96 Gothenburg, Sweden

There have been recent breakthroughs in ultra-broadband mixer technology using phonon cooled (NbN) or diffusion cooled (Nb) hot electron bolometers. Using a broad band spiral antenna and a NbN hot-electron bolometer typically one mixer can cover frequencies from about 700 GHz to 2.5 THz. The SYSTEM noise temperature that has been achieved is about 600 K at the low frequency end and about 1500 K at the high frequency range. Low local oscillator power can be as low as 10 nW for Nb devices. Ultimately this work may lead to imaging systems for other applications within astronomy and aeronomy, where cooling does not preclude their use. Also when combined with swept sources they could be used for fast accurate spectroscopy.

When combined with cheap simple sources such radiometer systems will form the basis for instrumentation for the analysis of gases in all kinds of environments: chemical industries, chimneys in steel manufacturing facilities, laboratory work, urban monitoring equipment etc.

Varactor Multipliers for Generation of Submillimetre Waves

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Recent progress in planar Heterostructue Barrier Varactor (HBV) technology has finally shown that they are likely replacements for the Schottky varactor diode. Their main advantage compared to the Schottky diode is that several barriers can be epitaxially stacked. Hence, a HBV diode can be tailored for a certain application in terms of both frequency and power handling capability. Moreover, the HBV operates unbiased and is a symmetric device thus generating only odd harmonics. This greatly simplifies the design of high order and broad band multipliers.

Today, state of the art Schottky balanced doublers can deliver 55 mW at 174 GHz (Rizzi *et al.* 1993) and state of the art four-barrier HBV triplers deliver about 9 mW at 248 GHz (Mélique *et al.* 1999).

Recently, whisker type HBVs have been fabricated on a copper substrate to improve their heat sinking capability (Dillner *et al.* 1999). Such devices are designed to be able to handle at least one Watt of input power and yet maintain the device temperature to below 100°C. For a single twelve-barrier HBV, a realistic conversion efficiency of 10% is expected, thereby providing output power in the region of 100 mW at 250 GHz, This in turn could then be used to drive a HBV quintupler to provide milliwatt levels of power at terahertz frequencies.

Advantages Shown in the DC Characteristics of SiGe HBTs by using a Graded Ge base Profile

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I. Introduction

Bandgap engineering is now being used in the context of silicon technology [1-4], following extensive research on SiGe growth [5,6]. As a result the high frequency performance of SiGe devices rivals that of GaAs, but leveraging the established knowledge and advantages of silicon. Other than the improvements in device speed, adding SiGe to a modern Si bipolar technology improves many of the dc characteristics.

In this paper we show results on the temperature dependence of some of those dc properties, confirming the advantages of SiGe. We focus on the gain and its temperature dependence, as well as the Early and breakdown voltages.

II. Device Design and Experimental Details

The devices were fabricated in a BiCMOS process, where a boron-doped epitaxial SiGe base layer was deposited by UHV-CVD as an additional part of the process flow. Existing process modules were adapted and used to accommodate the introduction of the SiGe layer. A schematic cross-section of a device is shown in Fig. 1, showing a standard poly-Si emitter deposited on a SiO_2 window onto the epitaxial SiGe layer. The SiGe base had a triangular Ge profile, ramping the Ge content from the emitter to the collector. Devices with a variety of dimensions were laid out although for this study only large-area dc devices (25 x 25 μm^2) were used.

The dc characteristics were measured using an HP4155, probing devices on a chip which was mounted with vacuum grease on a cold finger in a vacuum chamber. The sample temperature was measured with a calibrated Si diode thermometer mounted under the chip. At each temperature common-base, common-emitter and Gummel plots were measured.

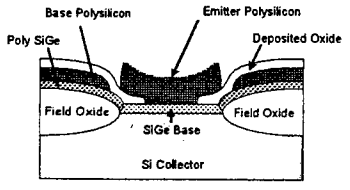


FIGURE 1. Schematic diagram of the structure of the SiGe HBTs.

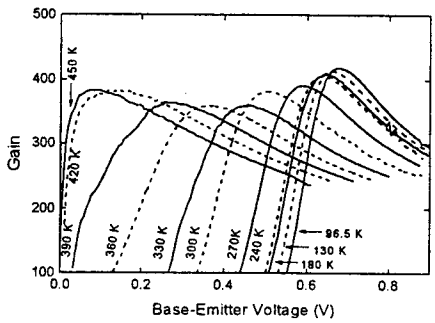


FIGURE 2. Variation of the dc gain versus V_{BE} as derived from Gummel plots.

III. Background

The currents in a bipolar transistors can be written as a combination of diffusion, J_D , recombination, J_R , and tunneling , J_T , currents. The diffusion current is thermally activated and shows the normal voltage and temperature dependence

$$J_D = J_{D0} \exp(qV_{BE} / k_B T).$$

Although the recombination current may have contributions from the bulk, surface, space-charge or other geometric regions most simple treatments predict $\exp(qV_{BE}/2k_B T)$ for its dependence [7]. The recombination term normally appears in the base current and leads to the collector and base currents crossing in a Gummel plot. By ascribing ideality factors, n_C , n_B, to the currents an $\exp(qV_{BE}/nk_B T)$ dependence is assumed to hold. For the collector current at room temperature and moderate voltages, where the current normally is diffusion current,

$$J_C = J_0(T) \exp(qV_{BE}/n_C k_B T) ,$$

with the ideality factor $n = n_C = 1$, reflecting the fact that the current mimics that of an ideal diode. $J_0(T)$ absorbs all the other temperature dependent factors ranging from the bandgap, to the carrier density and the mobilities [8].

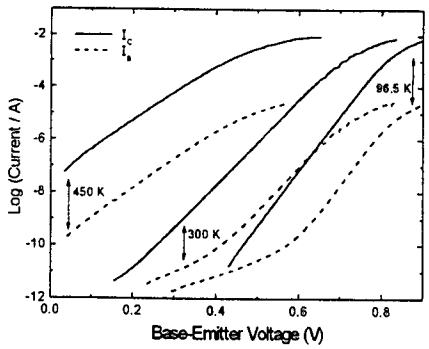


FIGURE 3. Typical Gummel plots from which the data in Fig. 1 was derived. V_{BC} was zero.

IV. Experimental Results and Discussion

In Fig. 2 we show the dc gain, as derived from Gummel plots, for a series of temperatures ranging from below 100K to 450K. Typical Gummel plots are shown in Fig. 3. The peak gain occurs at V_{BE} values which decrease with increasing temperature. At fixed V_{BE}, the gain can be seen to increase and then decrease with increasing temperature. Another aspect of these results is to examine the temperature dependence of V_{BE} at different fixed base currents. This is shown in Fig. 4. Above 250K, for the base currents chosen, the slopes are around 2 mV/K which is comparable with silicon-only devices. Allowance for these parameters is important in SPICE models and needs consideration when device or circuit specifications are given over extended operating ranges above and below room temperature. For example, at 10 μA base current, $\partial V_{BE} / \partial T$ is -1.71 ± .04 mV/K. Thus in a specification that applies over the +/- 40 °C range, V_{BE} will vary by more than 135 mV, which is significant and has to be accounted for in the design process.

In Fig. 5 we show the dc gain dependence on collector current. For currents less than $\sim 10^{-7}$ A the gain increases with increasing current but above

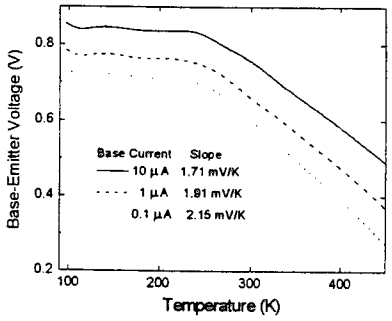


FIGURE 4. Variation of the base-emitter voltage V_{BE} with temperature, for different base currents.

that current the opposite is true. Similar comments apply to the temperature dependence of the gain seen in Fig. 5 - it decreases with temperature at the higher currents but does the opposite for currents < 10^{-7} A. Such small currents, however, may be of little practical importance but the characteristic is notable. At temperatures above ~220 K the region of increasing gain at low currents is less evident. The dc gain obtained from the Gummel plots is shown again in Fig. 6, confirming the negative dependence on increasing temperature.

The results in Figs. 5 and 6 are significant. For example, in power transistors to get the required output current a design may use many narrow emitter fingers. The assumption is that the current will be equally partitioned between all these parallel emitter fingers, ensuring that the current density is more or less even. The layout and device design is critical to ensure that this the case and ballast resistors may be needed. If the current density is not equal in each emitter finger effectively there are parallel devices operating

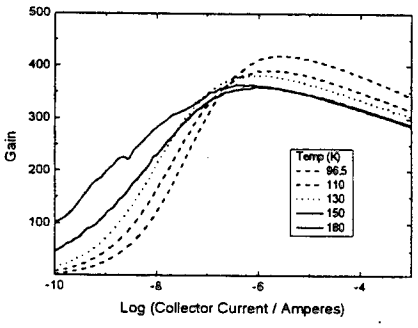


FIGURE 5. Variation of the dc gain with collector current for data below 200 K.

at a slightly different biases. Each dc or rf characteristic would then be some average from these 'parallel devices'. More importantly, if the gain of the device increases with increasing current, and also with increasing temperature, then thermal runaway can occur. An emitter finger with a disproportionate share of the current will experience an increase of temperature which will increase the gain and the current and so on. Burnout of an emitter finger is then possible. However, our data shows that the SiGe devices, if designed with multi-fingers, will not show this feature. If the temperature or current increases in one finger, the gain reduces producing a self-regulating effect [9]. This is not the case with Si devices, and is also not shown by devices with a 'box' Ge profile.

Although the dc gain is of vital importance in designing analog circuits the devices should also have a large output resistance. This is measured

from the common-emitter characteristics as the Early voltage, $V_A = I_C (\partial I_C / \partial V_{CE})$. Values for V_A > 30 V are desirable. The Early effect arises from the widening of the base-collection depletion region at high bias. This causes the effective base width to be reduced which increases and gain and collector current. To improve V_A the base doping can be increased which reduces the base width modulation, but reduces the gain in a homojunction bipolar transistor. One well-known useful advantage of incorporating a SiGe base layer into a bipolar device is to free the device designer from the

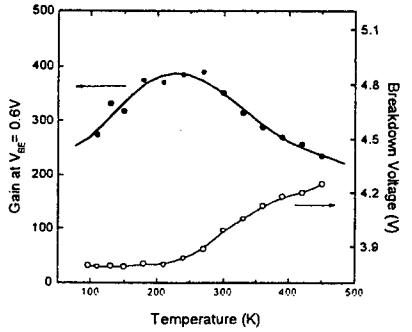


FIGURE 6. Temperature variation of the dc gain derived, from Gummel plots at $V_{BE} = 0.6$ V, and the breakdown voltage, from common-base measurements (see text).

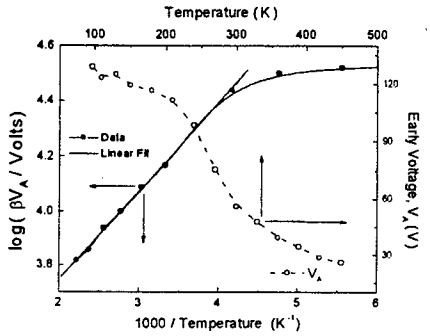


FIGURE 7. Temperature dependence of the Early voltage, V_A, and the gain-Early voltage product, βV_A.

contradictory influence of the base doping on β and V_A [10] The product βV_A , an important figure of merit for a circuit designer, displays higher values for SiGe devices than their Si counterparts. We have derived β and V_A from our common-emitter characteristics at a base current of 30 μA and measured V_A from the slope at V_{BE} = 1V and β at that voltage as well. In Fig. 7 we show the variation of both V_A and βV_A. Although V_A decreases with temperature above ambient, its value remains > 25 at 450 K. The $log(\beta V_A)$ vs. $1/T$ plot in Fig. 7 is close to linear above 270 K. These results are similar to those of Joseph et al [11], obtained for T < 300K.

In Fig.6 we also showed data for the breakdown voltage. Specifically we measured the voltage, in a common-base plot at I_E = 5 mA, at which $I_E = I_C$. Hence at this voltage $I_B = 0$, so we need to add V_{BE} to get an proper estimate for BV_{CE0} - this is the voltage we plot in Fig. 6. This voltage increases with increasing temperature which is a useful characteristic to help inhibit damage as the temperature is increased. This feature supports the advantage of having a negative temperature coefficient for the gain.

From the linear regions in the Gummel plot curves, such as those in Fig. 3, we have extracted the collector and base ideality factors which are plotted in Fig. 8. Over the whole temperature range n_C and n_B are approximately equal and both n_C, n_B ~1 above 250K. The values below 200K increase with decreasing temperature. Normally recombination effects produce ideality factors close to 2 often in the base [7] but not the collector current.

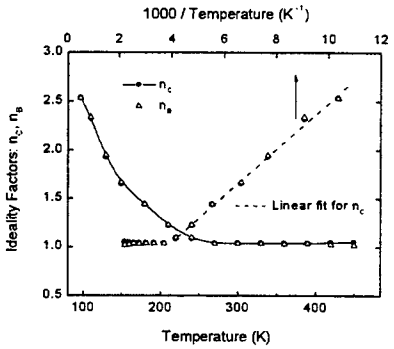


FIGURE 8. Variation of the collector (n_C) and base (n_B) current ideality factors with temperature. Top axis plots the variation as the reciprocal of the temperature.

It is unusual to get non-unity ideality factors for both the base and collector currents. This suggests we cannot simply ascribe the observation to a simple case of recombination, although we are aware that the inclusion of poly-Si and poly-SiGe in the extrinsic base could be a complicating feature, especially at low temperatures and bias. The curve in Fig. 8 which seems to indicate that that both n_C and n_B are proportional to $1/T$ is somewhat misleading. Actually the slopes of Gummel plots for both I_C and I_B are relatively insensitive to temperature below 250K. By extracting an ideality factor, using the normal thermally activated temperature dependence qV_{BE}/nk_BT, we are forcing a dependence which might be inappropriate. If the slopes have a weak

dependence on temperature n_C and n_B will have to be proportional to 1/T to be consistent.

To explain the non-ideal behavior of the base current in Si bipolar devices, Woo et al [7] have produced a model to show that recombination involving midgap traps in the space charge region can produce n values >2. In the space charge region of the base-emitter junction there is a high electric field which, through the Poole-Frenkel effect, can modify the energy barriers associated with the traps. Their model can lead to values of $n_B > 2$. Thus states (traps) in the emitter-base depletion region may be involved but we do not have a good model to explain the data.

Below ~250K in the lower V_{BE} region of the base current, for example the lowest temperature data in Fig. 3, there is a second region linear in V_{BE}. The values of n_B in this region are between 3.5 and 4 times higher than those values of n_B (Fig 8) over the low temperature range. We found this part of the I_B curves is almost independent of temperature. This suggests that the mechanism responsible is not thermally activated and most probably involves tunneling. There are at least 2 regions where tunneling may occur between the emitter and the base: in the space charge region defined by the emitter area (i.e. the normal base-emitter junction area) and the perimeter of the emitter between it and the p-doped extrinsic base. The extrinsic base, around the emitter, is typically pure Si which is highly p doped by the boron out-diffusion during thermal processes subsequent to the formation of the epi-base. Under the emitter window this boron is compensated by the n^+ diffusion from the poly-Si emitter. At the emitter periphery the depletion region is very narrow and the electric field higher there than at the intrinsic base. This region of self-aligned Si transistors has been implicated in the high n_B values observed in the base current of such devices before [12]. We suspect that this applies to our devices but we have not yet studied the perimeter/area dependence.

In Fig. 9 we show the variation of $log(J_0)$ vs. $1/T$, having derived the J_0 values from Gummel plots of I_C , such as those in Fig. 3. The plot is linear for T > 250 K, indicating that J_0 has an $exp(-T_0/T)$ dependence in this temperature range. The slope of this plot gives an equivalent energy of 1.19 eV. One of the temperature dependent terms in J_0 [8] involves $exp\ (-(E_G-\Delta E_G)/k_B T)$ where ΔE_G is the total bandgap narrowing. The bandgap narrowing caused by the Ge is zero because at the base-emitter junction $x_{Ge} = 0$. The narrowing due to the high base doping is ~ .045 eV, and is temperature independent. If the bandgap is written $E_G = E_{G0} - AT$ then the exponential term involves $-(E_{G0}-\Delta E_G)/k_B T$ and a constant. If we assume the bandgap over the 250-450 K temperature range is approximately linear in T then E_{G0} is ~1.18 eV, and the slope should give ~ 1.13 eV. Although this is lower than the observed value, the agreement is good since terms such as the mobility have not been included.

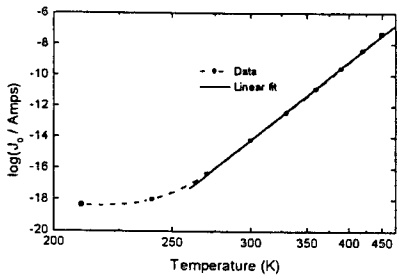


FIGURE 9. Temperature variation of J_0 ,the collector current at $V_{BE} = 0\ V$. (This is the intercept of the linear part of a Gummel plot with the y-axis.)

V. Conclusions

The temperature dependence of the *dc* characteristics of a SiGe bipolar transistor show that devices with a graded Ge base offer significant advantages. These include: negative dependence of the gain on increasing temperature and current; an increase in the breakdown voltages with temperature and high Early voltage values. This suggests that these SiGe devices could operate at higher power and temperature than Si-only devices

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Analytical Modeling of Low Frequency Noise and Static Characteristics of Si/Ge Channel pMOSFETs

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I. INTRODUCTION

The current confinement in buried, undoped quantum wells is known to increase the carrier mobility, μ, by suppression of some of the possible scattering modes. This principle was successfully applied to $Si_{1-m}Ge_m$ channel pMOSFETs (m being the Ge content in the alloy) and devices with μ values up to 4 times higher than the bulk hole mobility were obtained, for $m \approx 0.25$. The μ enhancement results here from a diminution of the scattering on charged traps near the SiO_2/Si interface and a reduction of the hole effective mass. By virtue of the same argument devices with higher μ were expected to have lower 1/f noise [1-3]. At the 1997 ISRDS we reported [4] that the low frequency noise, LFN, is not reduced at all in high-μ pMOSFETs. In the discussion that followed, questions as to the origin of the LFN in the buried channel devices were also posed. Namely, it was not evident how the current fluctuations in the channel, which, by construction, is separated by several nm of undoped Si (cap) from the SiO_2/Si interface, can be generated by capture/release phenomena involving the interface traps. Somewhat later, results of other groups came to our attention and some of them showed a reduction in the LFN noise in SiGe pMOSFETs [5,6], while some other have not. This rather confusing situation called for a more extensive analysis and this paper presents some of our results on this issue, resolving, in a good measure, the problems accumulated.

The departure point for this work was the observation that the charge fluctuations near the interface can create valence band edge displacements extending beyond the cap thickness, thus providing a mechanism for a density fluctuations in the SiGe channel holes. This had to be verified, though, by a numerical calculation. Our approach to the latter was inspired by the work of Chretien et al [3], who assumed two-dimensional, 2D, density of states, DOS, at the interfaces (under the oxide and under the cap) and demonstrated that a calculation, thus simplified, accounted adequately for the static characteristic of the pMOSFETs with buried SiGe channels. We have gone one step further and, combining McWhorter's (number fluctuations) [7] and Hooge's (mobility fluctuations) [8] treatments, calculated LFN properties of the SiGe channel devices, using a set of parameters accounting also for the static characteristics of the devices.

II. STATIC CHARACTERISTICS AND LOW FREQUENCY NOISE SIMULATION

II. 1. Static characteristics

The analytical model developed here involves solving the Poisson equation in the semiconductor for a given configuration, separately for each layer in the structure. It is based on the following assumptions,

(i). Denoting by m^*_{hh} a heavy hole effective mass, a single subband 2D-DOS is [3],

$$A_{2D} = m^*_{hh} / \pi \hbar^2, \tag{1}$$

Using the Fermi-Dirac statistics the inversion charges Q_{icap} and Q_{isige}, in the surface and SiGe channels, are obtained,

$$Q_{icap}(\Psi_{cap}) = qA_{2D}kT \times \ln\left[1+\exp\left(\frac{\Psi_{cap}-\Psi_0}{kT}\right)\right] \quad \text{and} \quad Q_{isige}(\Psi_{sige}) = qA_{2D}kT \times \ln\left[1+\exp\left(\frac{\Psi_{sige}-\Psi_0+\Delta E}{kT}\right)\right], \tag{2}$$

where Ψ_{si} and Ψ_{sige} are, respectively, the potentials at the Si/SiO_2 interface and $Si/Si_{1-m}Ge_m$ interfaces and Ψ_0 is the offset potential (depending on the substrate doping level). ΔE is the Si/SiGe valence band offset, approximated by $\Delta E = 0.84 \times m$ (eV). Other symbols have their usual meaning.

(ii). The Gauss's law and potential continuity are used to relate the potentials and inversion sheet charges as,

$$\Psi_{cap} = \Psi_{sige} + \frac{Q_{isige} + Q_d}{\varepsilon} . t_{cap}, \qquad \text{and} \qquad \Psi_{sige} = \Psi_d + \frac{Q_d}{\varepsilon} . (t_{sige} + t_{buf}), \tag{3}$$

where ψ_d is the buffer/substrate interface potential, t_{sige}, t_{cap} and t_{buf} are the cap layer, SiGe layer, and buffer region thickness values, ε is the Si permittivity, and Q_d is the depletion charge in the substrate, $Q_d = \sqrt{2q\,\varepsilon\,N_d\,\psi_d}$.

(iii). The gate charge conservation equation is then used to relate all the potentials and charges, with C_{ox}, the gate oxide capacitance,

$$V_g = V_{fb} + \psi_{cap} - \frac{Q_{icap} + Q_{isige} + Q_d}{C_{ox}}, \quad (4)$$

(iv). The total drain current is a sum of the cap layer current, I_{dcap}, and the SiGe channel current I_{dsige}, thus $I_d=Id_{cap}+Id_{sige}$. In the linear region ($V_d \to 0$) the drain current in the cap and the SiGe layers are given, respectively, by,

$$I_{dcap} = \frac{W}{L}\mu_{effcap} Q_{icap} V_d, \qquad \text{and} \qquad I_{dsige} = \frac{W}{L}\mu_{effsige} Q_{isige} V_d, \quad (5)$$

where μ_{effcap} and $\mu_{effsige}$ are the effective mobilities in the cap and SiGe layers, defined below.

(v). For the mobility in the cap layer and in the SiGe channel we use an empirical law which accounts for the mobility attenuation by the surface roughness scattering at strong inversion:

$$\mu_{effcap} = \frac{\mu_{cap0}}{(1 + Fcap/Fc)^2} \qquad \text{and} \qquad \mu_{effsige} = \frac{\mu_{sige}}{(1 + Qisige/Qc)}, \quad (6)$$

where μ_{cap0} is the low field mobility, μ_{sige} is the low field mobility in the SiGe alloy, F_{cap} the electric field at the cap/oxide interface, Fc a critical field (around 10^6V/cm) and Qc is a critical charge (around $6x10^{12}$q/cm^2).

The zero field mobility in SiGe is calculated using an empirical formula, which reproduces the Monte-Carlo simulation mobility results obtained by Fischetti and Laux for strained SiGe layers [9],

$$\mu_{sige}(m) = \mu_{sige0} + \left[(\mu_{si} - \mu_{sige0}) \frac{\sinh(m/m0) + \sinh[(1-m)/m0]}{\sinh(1/m0)} + (\mu_{ge} - \mu_{si}) \frac{\sinh(m/m0)}{\sinh(1/m0)} \right] + (\mu_{ge} - \mu_{si}) \frac{m^\alpha}{K}, \quad (7)$$

where μ_{si} (=500cm^2/Vs) and μ_{ge} (=20000cm^2/Vs) are the bulk Si and Ge hole mobilities, respectively, and μ_{sige0}, m0, α and K are fitting parameters.

II. 2 Low frequency noise model

(1) Carrier number fluctuations noise

We adopt here the known McWhorter's approach [7], assuming that the flat band fluctuations, $\delta V_{fb}=-\delta Q_{ox}/C_{ox}$, resulting from the capture/release of holes at slow states located near the SiO_2/cap Si interface, induce, by a capacitive coupling, fluctuations in both 2D carrier sheets, that of the cap and that of the SiGe channel. The δV_{fb} fluctuations create, therefore, correlated fluctuations in the number of carriers in each hole sheet. As the currents associated with each of them flow in parallel, the total current fluctuation δI_d is therefore a sum of the two components,

$$\delta I_d = \delta I_{dcap} + \delta Id_{sige} = -(g_{mcap} + g_{msige})\delta Q_{ox}/C_{ox}, \quad (8)$$

where g_{msi} and g_{msige} are the cap and the SiGe layer transconductances.

The cap and SiGe channel contributions to the spectral density of the carrier number fluctuation noise are analogous to the expressions derived [10] for conventional MOSFETs,

$$S_{Idcap} = S_{Vfb} \cdot g_{mcap}^2 \times \left(1 + \alpha_c C_{ox}\, \mu_{effcap} \frac{I_{dcap}}{g_{mcap}} \right)^2, \quad (9a)$$

and

$$S_{Idsige} = S_{Vfb} \cdot g_{msige}^2 \times \left(1 + R.\alpha_c C_{ox}\, \mu_{effsige} \frac{I_{dcap}}{g_{msige}} \right)^2. \quad (9b)$$

The total drain current noise, $S_{Id}=S_{Idcap}+S_{Idsige}$, is given by the sum of right-hand sides of Eqs (9); they comprise the effective mobilities, defined in Eqs. (6-7). S_{Vfb} is the spectral density at the frequency f, of the flat band voltage fluctuations, as in McWhorter's tunneling model [7],

$$S_{Vfb} = q^2 N_t kT/(WLC_{ox}^2 f), \quad (10)$$

where N_t is the density of slow oxide trap states and λ is the tunnel attenuation distance ($\lambda \approx 0.1$nm).

The expression in the parentheses of Eq. (9) accounts for the noise resulting from the correlated mobility fluctuations induced by the extra Coulomb scattering by the excess trapped oxide charges at high I_d values [10]. Its measure is provided by coefficient α_c (usually $\approx 10^5$). In Eq. (9b), for the SiGe channel, the correlation term is reduced by a factor R (≈ 0.1), because the Coulomb interactions between the SiGe channel holes and charged oxide states should be weaker than for the cap carriers, as the former are more distant.

(2) Hooge mobility fluctuations noise

The second contribution to the LFN arises from the Hooge mobility fluctuations [8] which are inversely proportional to the carrier number in a conductor. In the case of two channels we have two independent μ fluctuation sources, thus

$$S_{IdH} = \frac{q\alpha_{Hcap}}{WL\,Q_{icap}\,f}\cdot\frac{I_{dcap}^2}{I_d^2} + \frac{q\alpha_{Hsige}}{WL\,Q_{isige}\,f}\cdot\frac{I_{dsige}^2}{I_d^2}, \qquad (11)$$

where α_{Hcap} and α_{Hsige} are the Hooge parameters for the cap and SiGe channels, respectively.

Finally, we derive an expression for the total normalized drain current noise,

$$S_{IdTN} = (S_{Id} + I_d^2 \times S_{IdH})/I_d^2, \qquad (12)$$

for a direct comparison with the data.

III. RESULTS AND DISCUSSION

III. 1. Static characteristics

First we computed transconductance characteristics, $g_m(Vg)=\delta I_d/\delta V_g$, using Eq. (1-7) adjusting device parameters to fit our data [4] and those reported by the Ecole Polytechnique Federale de Lausanne, EPFL, team [6]. As shown in Figs 1 and 2, the calculation accounts satisfactorily for the experiment, indicating that our simple static analytical model can be successfully used for the SiGe pMOSFETs. The set of adjustable parameters obtained from the static data simulation has been subsequently used for LFN calculation, below.

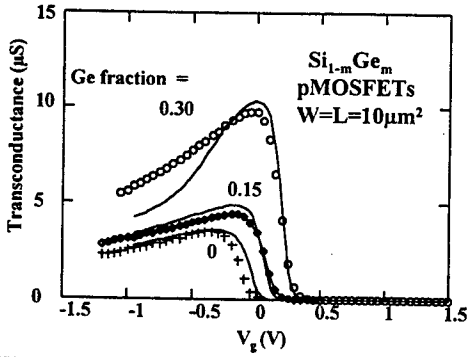


Fig. 1. Data (points) and calculated (lines) transconductance characteristics $g_m(V_g)$ for two SiGe channel and a Si control devices. This work [4].

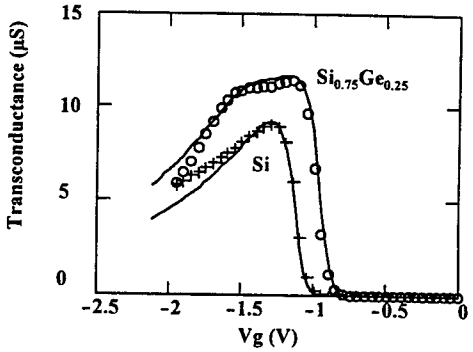


Fig. 2. Data (EPFL [6], points) and calculated (lines) transconductance characteristics $g_m(V_g)$ for SiGe and Si channel (control) 10x5μm² pMOFETs. Cap and channel conduction gives a double peak feature in SiGe devices.

III.2. LF noise results

The normalized power spectral density, PSD, of I_d fluctuations was calculated using Eqs (8-12), with the parameters obtained from the static data fitting. Figures 3 and 4 show the comparison between the model and the experiment for our devices and those from ref. [6]. For our data, the LFN fitting parameters computed for m=0 and 0.15 SiGe channels were found to be very close, (in particular, $\alpha_{hcap}\approx\alpha_{hsige}\approx10^{-6}$ and $N_t\approx10^{16}$ cm²) but for the m=0.3 device, $N_t=6\times10^{16}$cm², in agreement with [4], where this effect was attributed to the defect formation, expected at high Ge alloy fractions (stress relaxation). For the EPFL data, the LFN fitting parameters were found to be in good agreement with our data for low Ge content.

In order to understand why the LFN in the m=0.15 device and the control Si device are close, in spite of a significantly higher mobility in the former, we calculated S_{IdTN} as a function of m at a constant I_d at f=10Hz. The results in Fig. 5 show that the normalized LFN is, for weaker currents, a non monotonic function of m, and indeed takes, for m=0 and 0.15, the same values at lower I_d (here 0.5 μA). However, S_{IdTN} decreases monotonically with the Ge content for higher I_d values; the consequences of that are also seen in Fig. 3.

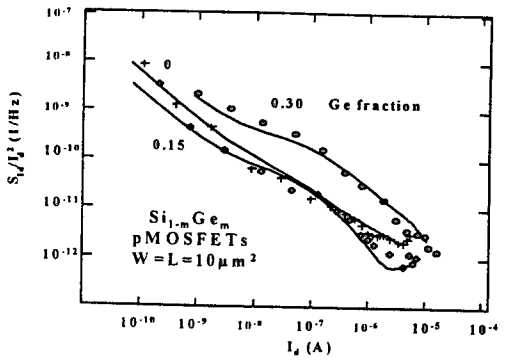


Fig. 3. Normalized PSD of I_d fluctuations at f=10Hz. Experimental data (points) [4] are well accounted for by the calculation (lines). I_d in abscissa.

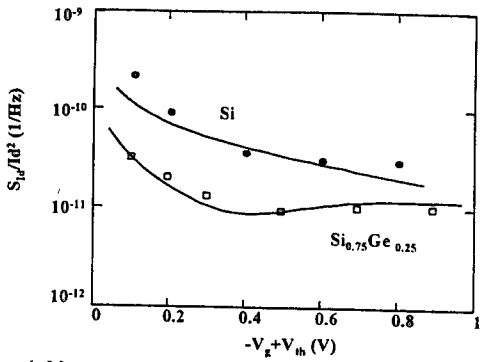


Fig. 4. Normalized PSD of I_d for SiGe and Si channel devices of EPFL devices [6] (points) and simulation (line) at f=1Hz. Gate voltage overdrive in abscissa.

Similarly the effect of cap layer thickness on S_{IdTN} at a constant current was calculated at f=10Hz. The results (Fig. 6) show that S_{IdTN} is non monotonic in t_{cap}, with a minimum depending on the operating current. Results presented in Figs 5 and 6 can serve for optimizing the noise properties of the devices.

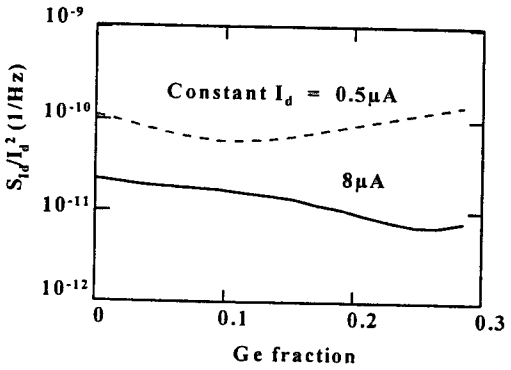


Fig.5. Normalized PSD of I_d fluctuations is a non monotonic function of Ge fraction at lower I_d; at higher values (here 8μA) the minimum vanishes.

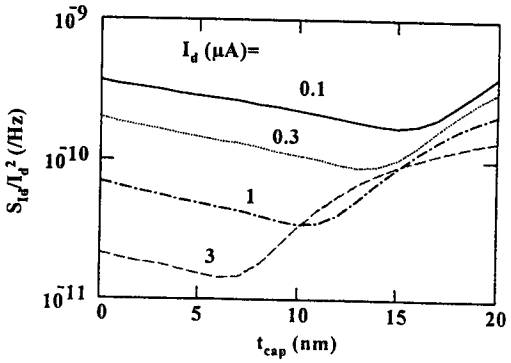


Fig. 6. Normalized PSD of I_d fluctuations is a non monotonic function of the cap layer thickness, with a minimum moving towards lower t_{cap} as I_d is increased.

IV. CONCLUSIONS

We have presented a novel analytical model for calculating self-consistently static and noise characteristics of $Si_{1-m}Ge_m$ channel pMOSFETs, and have shown that it accounts for the static and LFN data of ref. [4] and [6]. The model was further used for predicting LFN behavior for generic devices having an arbitrary Ge content and cap layer thickness. We have thus demonstrated the model capability for optimizing LFN properties of the devices. This procedure should be correlated with the optimization of device static properties, in order to generate an ideal pMOSFET, having low noise and optimal current carrying capacity. To our knowledge this is the first successful attempt to simulate and predict noise properties of microelectronics devices.

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Nanoscale SiGe-Channel Ultra-Thin-Body Silicon-on-Insulator P-MOSFETs

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I. INTRODUCTION

Device scaling has been successfully applied over many CMOS technology generations, resulting in consistent improvement in both device density and performance. However, new challenges are encountered in scaling conventional MOSFET structures much below 100 nm. The high channel doping concentration required to provide adequate short-channel effect (SCE) suppression results in degraded mobility and enhanced junction leakage. The ultra-thin-body silicon-on-insulator (SOI) MOSFET is a promising structure that suppresses SCE without using a heavily doped channel [1],[2]. With an undoped or lightly-doped channel, it also avoids the random fluctuation of threshold voltage due to random fluctuations of the position and number of dopant atoms in the channel region of nanoscale devices [3]. Another attractive approach to improving CMOS performance exploits the strain- or band-structure- induced mobility enhancement to increase the drive current while maintaining the same threshold and supply voltages. One of the most notable effects is the enhanced hole mobility in SiGe under biaxial compressive strain [4],[5] as this could be introduced into a P-MOSFET using a SiGe/Si heterostructure. Thus, a device that combines the advantages of the SiGe/Si heterostructure and an ultra-thin-body could be the device structure of choice in the nanoscale regime.

In this paper, we report the concept and the demonstration of nanoscale strained-SiGe-channel ultra-thin-body SOI P-MOSFETs, and demonstrate enhancement in the drive current due to the incorporation of SiGe in the channel. This paper is organized as follows. Section II describes the process flow for device fabrication. The results of device characterization are discussed in Section III, and the conclusions are summarized in Section IV.

II. DEVICE FABRICATION

The ultra-thin-body SOI MOSFET has a body thickness that is less than two or even one hundred angstroms. Etch-back or oxidation-thinning processes are incapable of producing a uniform body thickness since uniformity is limited by the thickness uniformity of the starting thick SOI layer. To provide adequate thickness uniformity, a deposited channel film is more desirable. A solid-phase-epitaxy-based ultra-thin-body SOI MOSFET fabrication technology was developed by Subramanian *et al.* [2]. A process flow similar to that reported in Ref. 2 is employed for the fabrication of the SiGe-channel ultra-thin-body SOI P-MOSFET, as illustrated in Fig. 1.

Devices were fabricated on mesa-isolated SmartCut™ wafers which had a 50 nm thick SOI layer and a 400 nm buried oxide. The SOI layer was etched away completely except for the source and drain islands (Fig. 1(a)). The trench between the source and drain islands was filled with SiO_2 using low-pressure chemical-vapor-deposition (LPCVD) and planarized to give the structure shown in Fig. 1(b). 150 Å of undoped amorphous $Si_{1-x}Ge_x$ (graded from $x = 0$ to $x = 0.3$ from bottom to top) and 50 Å of undoped amorphous-Si (α-Si) were deposited at 425°C using LPCVD to form a heterogeneous amorphous film connecting the source and drain islands. On the control wafers, 200 Å of undoped α-Si was deposited instead of the SiGe/Si stack to obtain a pure-Si channel. This was followed by a

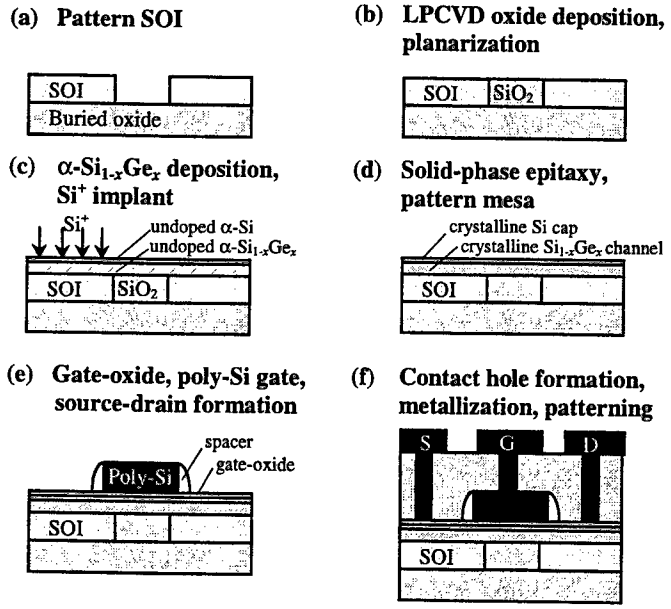


Fig. 1. Process flow for fabrication of the SiGe-channel ultra-thin body Solid-Phase Epitaxy MOSFET (SPEFET). Diagrams are not drawn to scale.

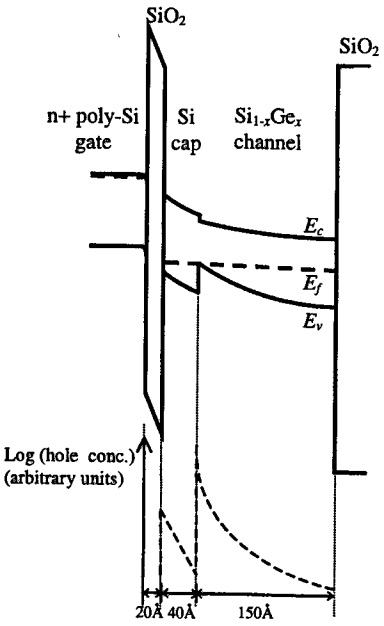


Fig. 2. Energy band diagram of the poly-Si–SiO_2–Si–$Si_{1-x}Ge_x$ structure at $|V_{GS}| > |V_{TH}|$.

masked or unmasked Si implant to break up the interfacial oxide over the source island or over both the source and drain islands, respectively (Fig. 1(c)). This implant facilitates the crystallization of the amorphous film with the SOI island(s) as the seed. The crystallization step, performed at 550°C for 24 hr, results in solid-phase epitaxial growth of the crystalline channel (Fig. 1(d)). The device islands were then patterned. After 20 Å gate oxide growth, and *in-situ* n+ poly-silicon gate deposition, the gate was patterned, and the source and drain regions implanted (Fig. 1(e)). Finally, contact-hole etch, metallization, and metal patterning were done to complete the device as shown in Fig. 1(f). This device structure is called the solid-phase epitaxy MOSFET (SPEFET) [2]. In Fig. 2, the energy-band diagram of the SiGe-channel SPEFET is shown. The top Si cap layer has a thickness of 40 Å after gate oxide growth. It serves to provide a good interface Si/SiO_2 quality since it is known that oxidation of SiGe yields a high density of trap states at the dielectric interface. The fact that nearly all of the band-gap difference between $Si_{0.7}Ge_{0.3}$ and Si appears at the valence band should be noted. As a result, the majority of the holes in P-SPEFETs are confined in the SiGe-channel (see hole concentration plot in Fig. 2) for typical gate biases, and their mobility is expected to be greatly enhanced [7].

III. CHARACTERIZATION AND DISCUSSION OF RESULTS

The results of device characterization are discussed in this Section. First, the characteristics of devices that received interfacial oxide break-up implant on both the source and drain islands and only on the source island are examined. With an implant on both source and drain, the solid-phase epitaxial growth proceeds from both ends and meets near the middle of the channel to form a grain boundary. Perfect coalescence of the two crystallization fronts is not usually possible even though the source and drain seeds were from the same crystal. With implant on only the source island, crystallization advances from only one side, thus eliminating the grain boundary in the channel at the cost of an additional lithography step. In Fig. 3, the effects of one- and two-sided crystallization on the I_{DS}-V_{DS} characteristics of the SiGe-channel SPEFETs are shown. The elimination of the grain boundary gives about 80% improvement in the drive current at V_{DS} = -1.5 V, V_{GS} - V_{TH} = -1.2 V. The I_{DS}-V_{GS} characteristics are plotted in Fig. 4 to show the excellent turn-off behavior of the devices that used one-sided crystallization. Fig. 5 illustrates the excellent short-channel effect of the ultra-thin-body devices. It also shows that the grain boundary not only increases the threshold voltage probably due to

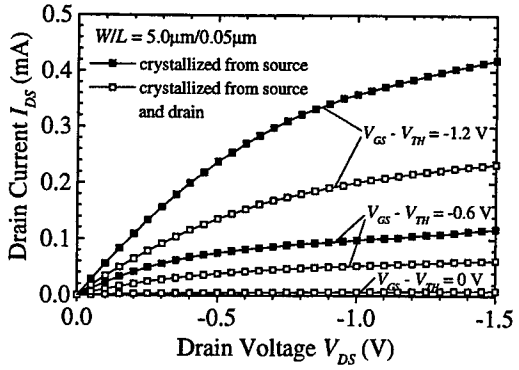


Fig. 3. I_{DS}-V_{DS} characteristics for SiGe-channel P-SPEFETs crystallized from the source and from both the source and drain.

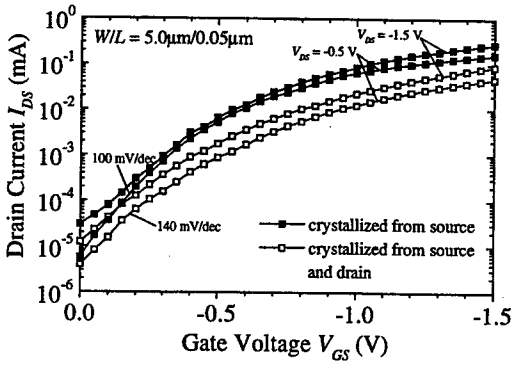


Fig. 4. I_{DS}-V_{GS} characteristics for SiGe-channel P-SPEFETs crystallized from the source and from both the source and drain.

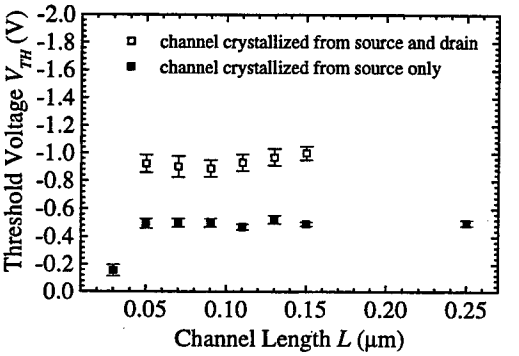


Fig. 5. Ultra-thin-body SiGe SPEFETs show little V_{TH} roll-off down to L = 0.05 μm.

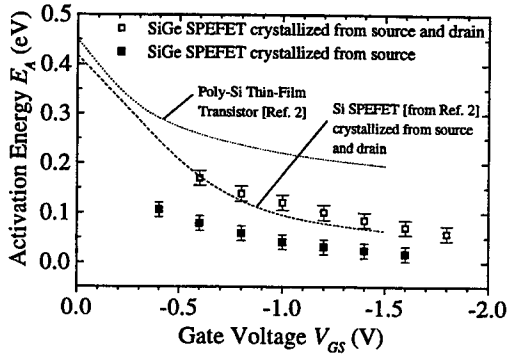


Fig. 6. Drain current activation energy is low for SPEFETs crystallized from the source, indicating low or no grain-boundary barrier.

the high interface state density at the grain boundary, but also causes a wider distribution of the V_{TH} values. Further evidence of the elimination of the grain boundary by the masked Si implant is shown in Fig. 6, where for all V_{GS}, the drain current activation energy [2],[6] is lower for the channel that is crystallized from one side. This indicates that the grain boundary is either eliminated or its barrier height much reduced.

In Fig. 7, we compare the drain current of the SiGe-channel and the Si-channel SPEFETs of W/L = 5.0μm/0.05μm at various V_{GS} - V_{TH} from 0 V to -1.2 V. The channel film of these devices are crystallized from the source side. An enhancement of 70% in the current drive is observed at V_{DS} = -1.5 V, V_{GS} - V_{TH} = -1.2 V in the SiGe SPEFETs. We observed comparable drive currents for the SiGe-channel and Si-channel N-SPEFETs as expected since the electrons are not confined to the SiGe layer due to the small conduction band offset between Si and SiGe. In both cases, I_{DS} is low probably due to a large series resistance and further process optimization is needed. In Fig. 8, the threshold voltage is plotted as a function of the channel length. We do not observe significant V_{TH} roll-off until L = 0.05 μm for either channel material, demonstrating good immunity to short-channel effects. Channel lengths are limited to below 0.25 μm because the limited extent of the lateral epitaxy. The difference in the threshold voltage of about 0.2 V between the two types of devices is consistent with the valence band offset between Si and $Si_{0.7}Ge_{0.3}$.

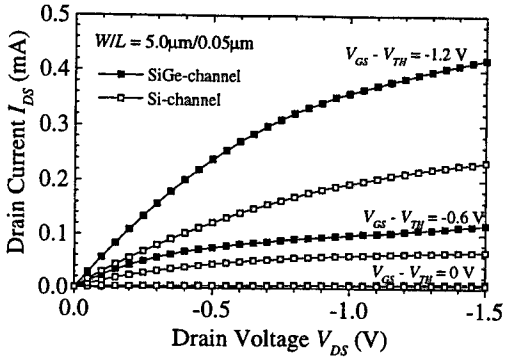


Fig. 7. SiGe P-SPEFETs have larger I_{DS} than Si SPEFET. The SiGe and Si N-SPEFET characteristics are similar to each other.

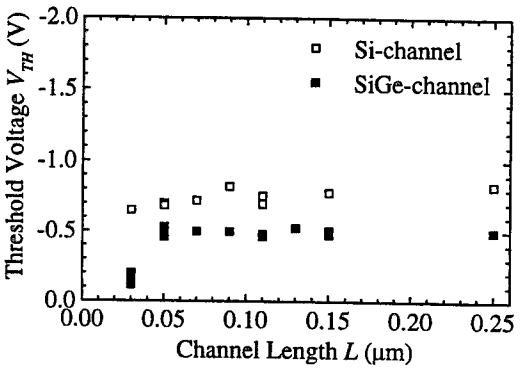


Fig. 8. Both Si and SiGe P-SPEFETs show excellent short-channel behavior.

IV. CONCLUSIONS

In conclusion, we have demonstrated the shortest channel-length strained-SiGe-channel heterostructure P-MOSFET reported to date. The device has a novel structure that employs an undoped ultra-thin body on SOI substrates to suppress the short-channel effects. The device is fabricated by lateral solid-phase epitaxy and is termed the SPEFET. We have observed excellent short-channel immunity and an enhancement of 70% in the drive current due to the introduction of $Si_{0.7}Ge_{0.3}$ in the channel. A masked interfacial oxide break-up implant is shown to facilitate unilateral crystallization to eliminate the grain boundary from the channel. Band-structure and strain engineering using SiGe/Si heterostructures combined with the advantages of the ultra-thin-body structure appears to be an attractive option for the sub-50 nm MOS transistors.

ACKNOWLEDGMENTS

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A Fully Certified SiGe-BiCMOS Process for ASICS and Multiproduct Wafers

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Only recently the first devices and integrated circuits based on the Silicon Germanium hetero bipolar transistor (HBT)[1] became available commercially.[2] The largely improved high frequency properties as compared to Si devices, and the compatibility with standard Si technologies make these ICs ideal candidates for high frequency analog applications in the booming telecommunication market. Still, the available number of components and the production capacities are limited, and mainly available to selected customers. Here we report on a fully certified SiGe BiCMOS process that is offered as a foundry service for ASICs and multiproduct wafers.[3]

Austria Microsystems (AMS), a leading European ASIC manufacturer, has introduced a BiCMOS platform for high frequency ASIC applications in 1993. It comprises 1.2, 0.8, and 0.6µm processes with fully established design environment. In order to go beyond its 18 GHz limit, a SiGe BiCMOS process was developed in cooperation with SiGE MICROSYSTEMS Inc. The main features of the new SiGe process include n and p buried layers with Si and SiGe:B epilayers, deep sinker, three types of poly-resistors (20, 70 and 1200 Ohm), high capacitance poly-poly (up to 1.75 fF/µm²) and poly to sinker capacitors, lateral PNP transistors, and full CMOS integration with up to 2800 gates/mm².

The newly developed quasi-self-aligned HBT module was integrated into the existing 0.8µ BiCMOS-process with just two additional mask levels. The HBT architecture is depicted in Fig. 1 as an energy-filtering transmission electron microscopy[4] picture.

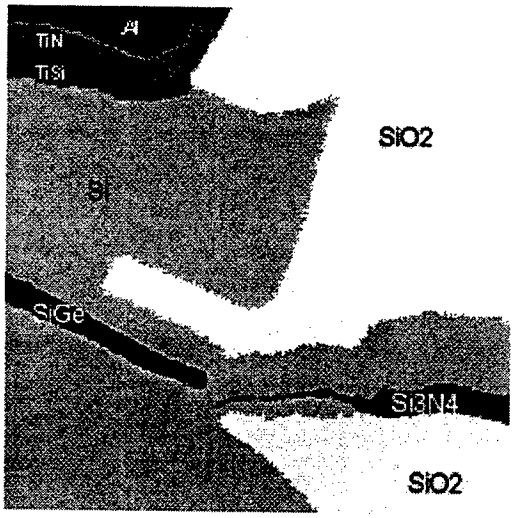


Fig.1 Energy filtered TEM micrograph displaying the HBT architecture

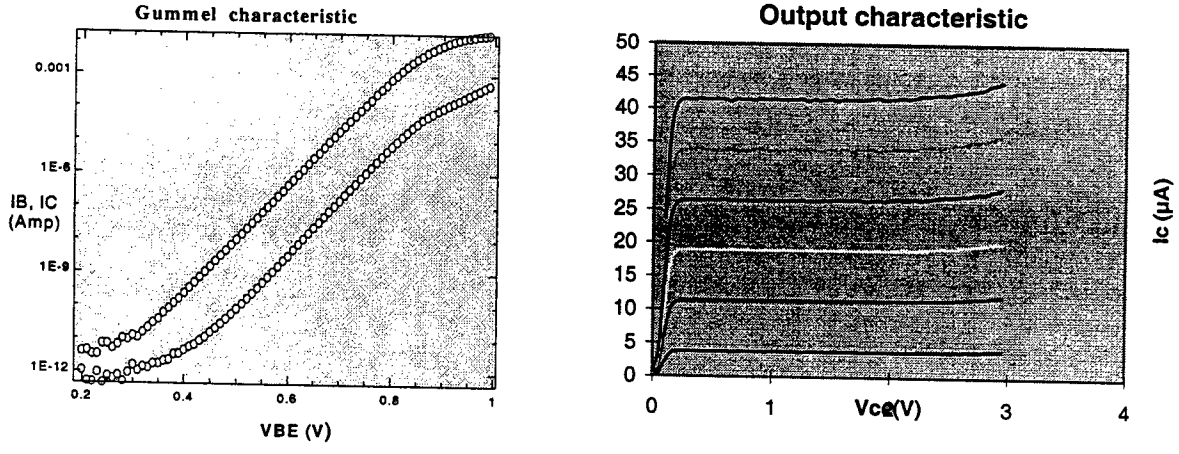
In order to meet the requirements of high frequency analog designs a drift transistor with a triangular Ge-Profile in the base was implemented. This concept mainly results in a reduced base transit time, which is the dominating contribution to the transistor delay time.[5] The graded Ge profile chosen here shows an improved Early voltage as compared to HBTs with a Ge box profiles, whereas the latter show superior current gain. The $\beta \cdot V_A$-product, which is crucial for analog processes, is thus optimized with a graded Ge-profile.

Typical performance date, especially the drastically enhanced high frequency behavior of the HBT-BiCMOS process, are listed in Table 1 in comparison with the original BiCMOS data set. The conflicting parameters BVceo, base-collector transit time and base-collector capacitance, which is a key-parameter for f_{max},[6] are optimized by a selective collector implant (SIC-implant).

PARAMETER	UNIT	0.8 µ - BJT	0.8 µ - HBT
f_t	GHz	12	> 35
f_{max}	GHz	8	> 35
BETA	-	100	100
Early Voltage	V	30	> 60
BVCEO	V	>6	> 3
Rbb*	OHM	350	200
RE*	OHM	12	12
RC*	OHM	110	110
Cje*	fF	12	24
Cjc*	fF	22	12
Cjs*	fF	50	32

*) measured at 3µ CBEB structure (double base)

Table 1 Comparison of 0.8µ Si-BiCMOS and 0.8µ SiGe-BiCMOS



I_B: 0.1 µA to 1.1µA in 0.2µA steps

Fig. 2 Gummel characteristics and output characteristics

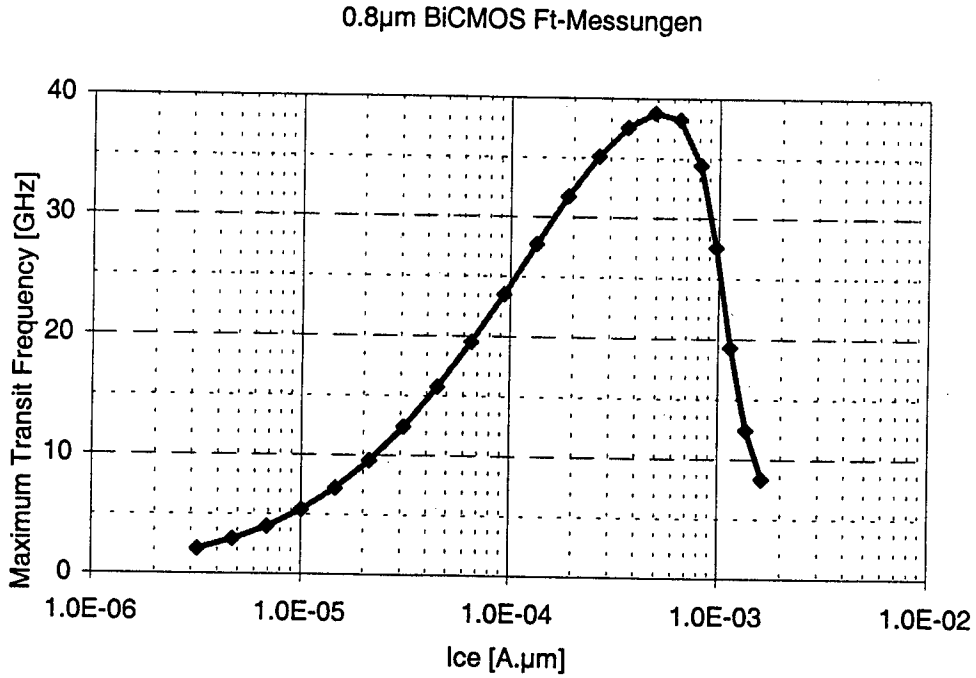


Fig. 3 f_t -curve of a typical double base 0.8x3µm² HBT

To achieve the demonstrated device parameters in Table 1 and Figs 2, 3, the vertical alignment of the boron and the germanium profile in the base is a crucial design issue. Transient enhanced boron outdiffusion (TED) into the Ge-free emitter and collector regions causes the formation of parasitic energy barriers in the conduction band[6]. This results in degraded device performance with lowered Early voltages, strong current gain variations and low f_t and f_{max} values. For routine process monitoring reverse Gummel characteristics are measured and ideality factors for the collector current are extracted as a function of V_{BE}. If the parasitic barriers come to lie within the depletion zone of the base collector junction their deteriorating effect on the collector current is diminished. Consequently one can probe the junction area by varying V_{BE} and thus the depletion width.
Such measurements allowed the optimization of the doping profile in the SiGe epi-base such that the detrimental effects are minimized for the thermal budget of a given process. However, this always requires compromises and reduces the effective base doping level. For further enhancement of the high frequency behavior it is therefore highly desirable to effectively suppress TED of the base doping. This is possible by replacing the binary $Si_{1-x}Ge_x$:B base by a ternary $Si_{1-x-y}Ge_xC_y$:B epi layer. Already small carbon concentrations of <0.5 at.% almost completely suppress TED, as can be seen in the reference experiment in Fig.4. This allows a high degree of freedom concerning the doping profile as well as the thermal budget of the BiCMOS process. We are presently developing a production compatible SiGeC process for the next generation of high-performance SiGe-BiCMOS ASICs.

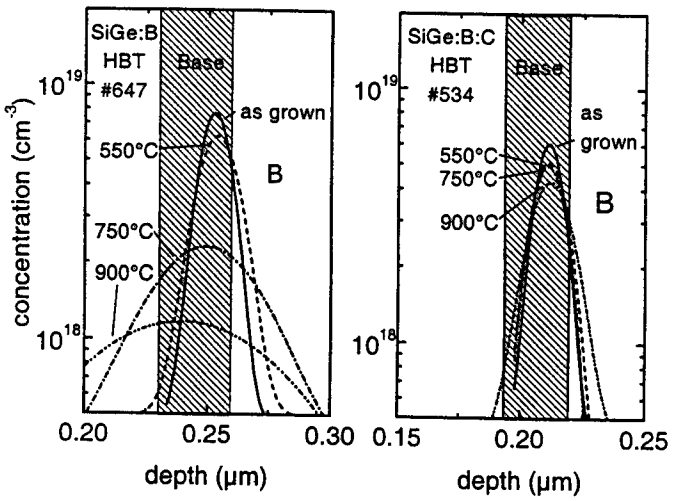


Fig. 4 Transient enhanced boron diffusion in the base of a SiGe HBT in comparison to a SiGeC:B base with 0.5 at.% carbon grown under otherwise identical conditions.

For analog applications the use of BiCMOS technology allows the merging of the advantages of CMOS, such as high integration density at low power consumption, with the favorable bipolar aspects: high transconductance, low noise and high speed. We demonstrated that by adding a SiGe epilayer and as few as two mask layers the performance of a given BiCMOS platform can be improved drastically. Since the enhanced f_t and f_{max} values are achieved at considerably lower Ic-values compared to conventional Si- technology the power consumption is further reduced, which is important for battery operated devices.

A main advantage of the SiGe approach chosen here is its full compatibility with standard Si technologies, which require little adjustment of an existing process. Introducing SiGe into an existing BiCMOS process can therefore be a cost effective alternative to the development of a new process with reduced critical dimensions, especially as standard CVD epi-reactors with SiGe capability are now becoming commercially available.

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A New Static Model for $Si/Si_{1-x}Ge_x$-MODFETs for Use in SPICE-Based Simulators

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I. Introduction

In today's design paradigm it is necessary to characterize the static, small-signal and large-signal behaviour of the various devices available in a given process, then choose a suitable model from the list of models installed in a simulator database and extract the model parameters. The problem of modeling the behaviour of the $Si/Si_{1-x}Ge_x$-MODFET [1] is complicated by the fact that existing circuit simulation tools such as SPICE, do not provide a $Si/Si_{1-x}Ge_x$-MODFET model "per se".

Without satisfying the DC functionality, optimisation of the circuit for e.g. maximum operating speed has little significance. As such, the present paper deals with the development of a suitable static model which could be installed in an existing simulator (e.g. Star-Hspice) as a set of equations which are built into the netlist. The development of a corresponding small-signal and large-signal model is ongoing and a first approach [2] is based on the static model presented in this paper.

II. Drain Current Model

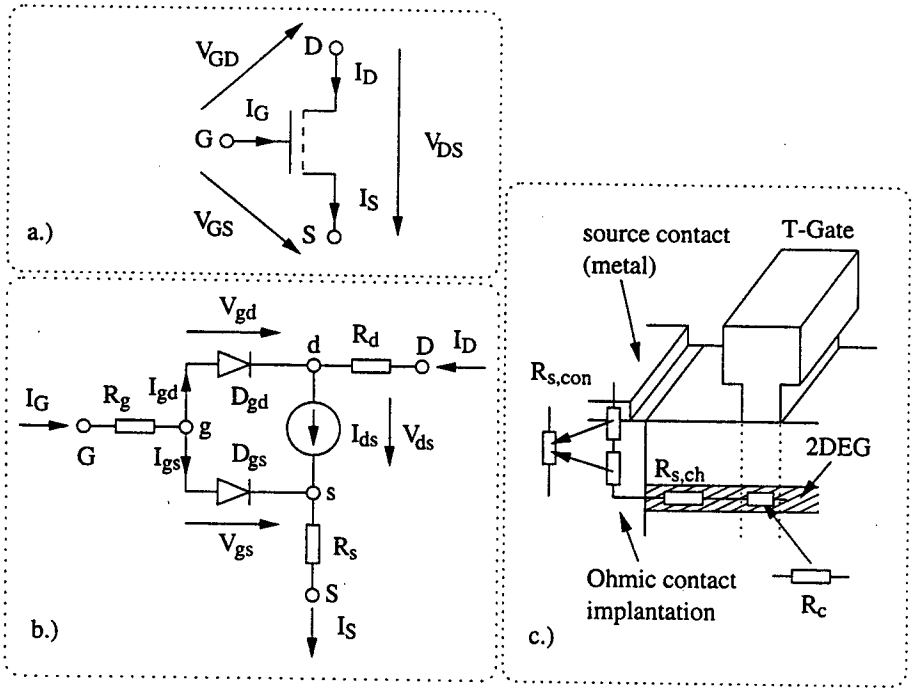


Fig. 1: Commonly used equivalent circuit for static MESFET models in SPICE

The commonly used equivalent circuit for static MESFET models in SPICE (fig. 1) has some disadvantages to describe the static behaviour of the $Si/Si_{1-x}Ge_x$-MODFET. The source and

drain resistances of the MODFET $R_s = R_{s,con} + R_{s,ch}$ and $R_d = R_{d,con} + R_{d,ch}$ are strongly bias dependent, especially in short channel devices due to the influence of the gate on the ungated part of the channel (source-gate and drain-gate distance), indicated as $R_{s,ch}$ in fig. 1.c for the source contact area. A second problem is encountered for the area of the gate-source and gate-drain diodes. Most models use a 50%/50% approach, but this is questionable especially for devices with asymmetric positioned gates.

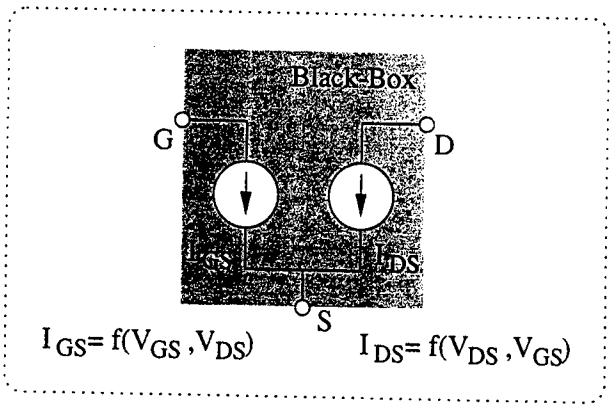


Fig. 2: "black box" equivalent circuit

For MESFET and MODFET devices with semi-isolated substrates (including the $Si/Si_{1-x}Ge_x$-heterostructure, where the substrat resistance is high enough [1]) the static behaviour is completely described with the two equations $I_{DS} = f_D(V_{DS}, V_{GS})$ and $I_{GS} = f_G(V_{GS}, V_{DS})$, where I_{DS} and I_{GS} are defined in fig. 2 and V_{DS} and V_{GS} in fig. 1.a (G,D,S are the contacts of the extrinsic device).

The equivalent circuit for our new static model is therefore a "black box" with two current sources (fig. 2). The drain current equation is based on an approach of the velocity-field characteristics model from Yeager et.al. [3], which was modified to account for the fact that onset of velocity saturation occurs at lower field levels in a strained silicon lattice than in (unstrained) bulk silicon [4,5], see fig. 3.

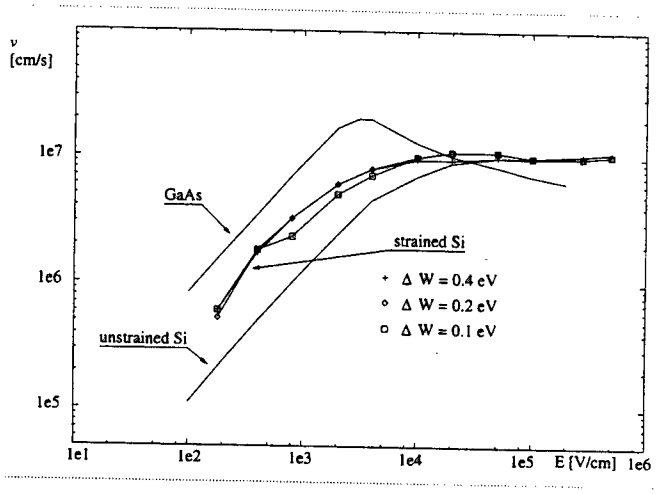


Fig. 3: Velocity-field characteristics of unstrained and strained Si (depending on the energy ΔW due to the split of the six-fold degenerate Δ valleys in two lowered and four raised valleys in strained Si) and GaAs [4,5].

The formulation of the drain current I_{DS} of the new static model is:

$$I_{DS} = (\Gamma_1 + \Gamma_2 \cdot V_{DS}) \cdot \tanh\left[\Gamma_3 \cdot V_{DS} + \Gamma_4\right]$$

with the four gate voltage dependent functions $\Gamma_{1...4} = f\,(V_{GS})$:

$$\begin{aligned}
\Gamma_1 &= \Theta_{1,1} \cdot \exp\left(\Theta_{1,2} \cdot V_{GS}\right) - \Theta_{1,3} \cdot \exp\left(-\Theta_{1,4} \cdot V_{GS}\right) + \Theta_{1,5} \cdot V_{GS}^3 + \Theta_{1,6} \cdot V_{GS} + \Theta_{1,7} \\
\Gamma_2 &= \Theta_{2,1} \cdot (\Theta_{2,2} + \Theta_{2,3} \cdot V_{GS}) \cdot \tanh(\Theta_{2,4} \cdot V_{GS}^2) + \Theta_{2,5} \cdot V_{GS} + \Theta_{2,6} \\
\Gamma_3 &= \Theta_{3,1} \cdot \tanh(\Theta_{3,2} \cdot V_{GS}) \cdot \exp\left(-\Theta_{3,3} \cdot V_{GS}\right) + \Theta_{3,4} \cdot V_{GS}^3 + \Theta_{3,5} \cdot V_{GS} + \Theta_{3,6} \\
\Gamma_4 &= \Theta_{4,1} \cdot \tanh(\Theta_{4,2} \cdot V_{GS}) \cdot \exp\left(-\Theta_{4,3} \cdot V_{GS}\right) + \Theta_{4,4} \cdot \tanh(\Theta_{4,5} \cdot V_{GS}^2) + \Theta_{4,6} \cdot V_{GS}^3 \\
&\quad + \Theta_{4,7} \cdot V_{GS} + \Theta_{4,8}
\end{aligned}$$

III. Results

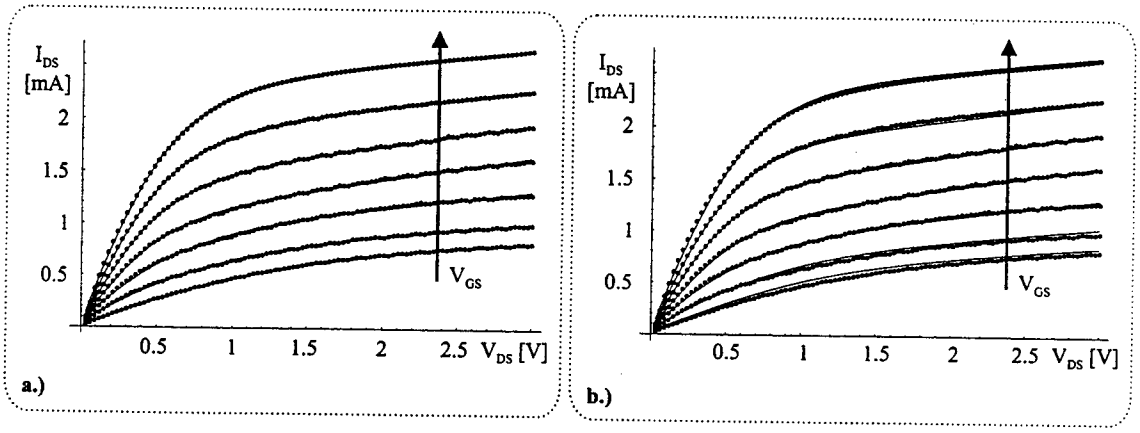


Fig. 4: measured (dotted) and simulated (solid) drain current ($V_{DS} = 0 \ldots 3V$, $V_{GS} = -0.5V \ldots 0.7V$) with a.) $\Gamma_{1...4}$ separately extracted for each V_{GS} value and b.) using the functions $\Gamma_{1...4} = f\,(V_{GS})$.

Fig. 4 and 5 show the good fitting between measured and simulated data for an n-type depletion mode $Si/Si_{1-x}Ge_x$-MODFET with gate length $L = 150nm$ and gate width $W = 10\mu m$ for a drain voltage range of $0 \ldots 3V$ and a gate voltage range of $-2 \ldots 0.7V$. In fig. 4.a the four $\Gamma_{1...4}$ parameters are extracted separately for each V_{GS} value, while in fig. 4.b and fig. 5 the functions $\Gamma_{1...4} = f\,(V_{GS})$ given in section II were used.

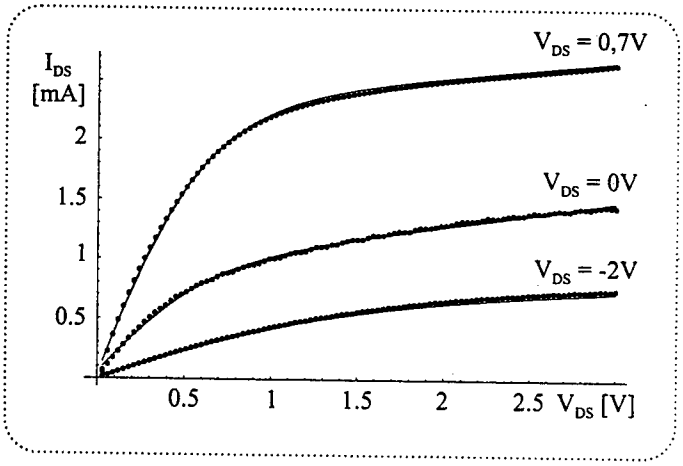


Fig. 5: measured (dotted) and simulated (solid) drain current ($V_{DS} = 0 \ldots 3V$, $V_{GS} = -2V, 0V, 0.7V$) using $\Gamma_{1...4} = f\,(V_{GS})$

A comparison of measured and simulated data for gate width $W = 5\mu m$ and $W = 50\mu m$ is shown in fig. 6. There are two possibilities to consider the gate width dependence of the drain current, the use of different extracted parameter sets or the use of an additional function $f_W\,(W, V_{DS}, V_{GS})$ for the drain current $I_{DS} = f_W \cdot f_n\,(V_{DS}, V_{GS})$, where f_n is the drain current $I_{DS,n} = (\Gamma_{1,n} + \Gamma_{2,n} \cdot V_{DS}) \cdot \tanh\left[\Gamma_{3,n} \cdot V_{DS} + \Gamma_{4,n}\right]$ for a chosen gate width W_n.

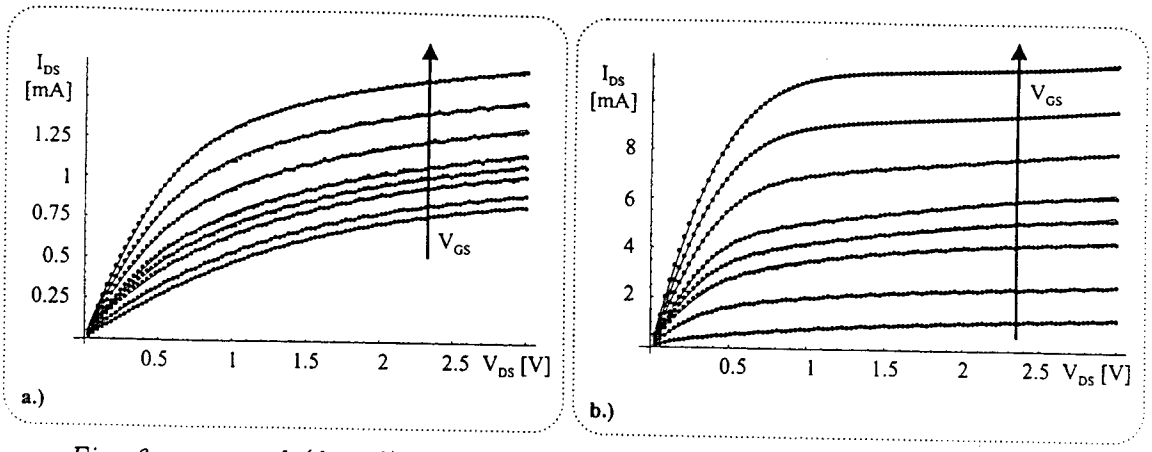


Fig. 6: measured (dotted) and simulated (solid) drain current ($V_{DS} = 0 \ldots 3V$, $V_{GS} = -0.5V \ldots 0.7V$) a.) gate width $W = 5\mu m$, b.) gate width $W = 50\mu m$

IV. Gate Current Model

For the gate current I_G the model uses the exponential approach

$$I_{GS} = \xi_1 \cdot \{\exp[\xi_2 \cdot V_{GS} + \xi_3] - \xi_4\}$$

with $\xi_1 = \eta_{1,1} \cdot (V_{DS} - \eta_{1,2})^2 + \eta_{1,3}$ and $\xi_2 = \eta_{2,1} - \eta_{2,2} \cdot V_{DS}$. The comparison between measured and simulated data is shown in fig. 7 for a $Si/Si_{1-x}Ge_x$-MODFET with gate length $L = 150nm$ and gate width $W = 10\mu m$.

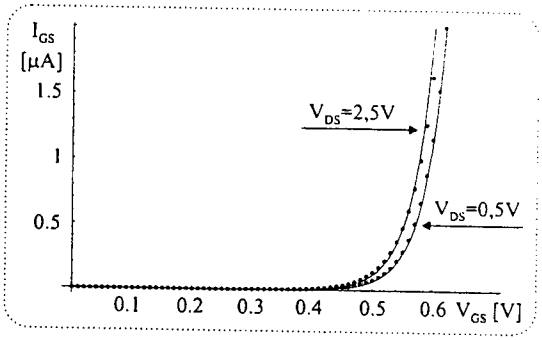


Fig. 7: measured (dotted) and simulated (solid) gate current using the functions $\Gamma_{1\ldots4} = f(V_{GS})$

V. Summary

We presented a new static model suitable for the $Si/Si_{1-x}Ge_x$-MODFET, which is based on a "black box" equivalent circuit. The model accounts for the velocity-field characteristics of strained Si and shows a good fitting between simulated and measured data for the drain and the gate current. For the use in SPICE-based simulators like Star-Hspice or PSPICE the model could be included in the netlist. To account for circuits, where the drain and source contacts of the MODFET are changing during operation, two different extracted parameter sets ($\Theta_{1,1} \ldots \Theta_{4,8}$) of the static model are used, which are selected in the netlist with an "if" or "sgn" (Star-Hspice) statement, depending on the sign of V_{DS}.

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Two Dimension Electron Gas Enhancement in AlGaN/GaN/InGaN/GaN Quantum Well Structures

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I. INTRODUCTION

The pyroelectric and piezoelectric effects play an important role in AlGaN/GaN/InGaN based heterostructures [1-3]. Very high values of the two-dimensional (2D) electron sheet density (up to $3x10^{13}$ cm^{-2}) have been both predicted theoretically and demonstrated experimentally in AlGaN/GaN Heterostructure Field Effect Transistors. Recently, it was suggested that piezoelectric effects could induce a 2D-hole gas [4].

In practical AlGaN/GaN heterostructures, at sheet concentrations close to and exceeding ~10^{13} cm^{-2}, the carriers are shared between 2D and 3D [5]. In order to confine all the electrons in the 2D gas, we propose a structure, combining the AlGaN/GaN heterostructure and InGaN/GaN multiple quantum wells (MQWs).

In this paper, we present our experimental and theoretical studies of $Al_{0.15}Ga_{0.85}N/GaN/[In_{0.14}Ga_{0.86}N/GaN]_n$ multiple quantum well structures. We demonstrate that the introduction of an InGaN Quantum Well (QW) might enhance the sheet carrier density.

II. EXPERIMENTAL RESULTS

For this study, we fabricated a series of $Al_{0.15}Ga_{0.85}N/GaN/[In_{0.14}Ga_{0.86}N/GaN]_n$ MQWs with n ranging from 0 to 4 by low pressure MOCVD (see Fig. 1). The top $Al_{0.15}Ga_{0.85}N$ layer was 20-nm thick; the GaN channel was 10 nm thick. In MQWs, $In_{0.14}Ga_{0.86}N$ layers were 2.5 – 3 nm, separated by 5 nm – 6 nm thick GaN. All structures were grown on 1 μm GaN buffer layer. The measured electron sheet density was from 0.8 $x10^{13}$ to $1.8x10^{13}$ cm^{-2} depending on the number of quantum wells. The measured mobility varied from 550 cm^2/V-s to 1,350 cm^2/V-s. The dependence of electron sheet density and mobility on the number of QWs is not monotonous (see Fig. 2). Lowest mobility and highest n_s were observed for n = 1. The results obtained for different runs were very consistent.

III. MODEL DESCRIPTION

Our calculations used the solution of Poisson's equation with 3D Fermi-Dirac distribution function for electrons. The boundary conditions for the $Al_xGa_{1-x}N/GaN$ and InGaN/GaN interfaces accounted for the piezoelectric effect and spontaneous polarization:

$$\varepsilon_1 F_1 + P_1 + P_{s1} = \varepsilon_2 F_2 + P_2 + P_{s2}. \quad (1)$$

Here ε_1 and ε_2 are the dielectric permittivities, F_1, F_2 are the interface electric fields, and P_1, P_{s1}, P_2, P_{s2} are the piezoelectric and spontaneous polarizations in AlGaN and GaN, or GaN and InGaN, respectively. For the (0001) growth direction, the piezoelectric polarizations are:

$$P_1 = \pm 2(e_{31} - e_{33}c_{31}/c_{33})u_{xx} \quad (2)$$

Here c_{31}, c_{33} and e_{31}, e_{33} are the $Al_xGa_{1-x}N$ or InGaN elastic constants and piezoelectric constants, respectively, and u_{xx} is $Al_xGa_{1-x}N$ or InGaN strain component in the interface plane. The piezoelectric constants of GaN were extracted from GaN electromechanical coupling coefficients (see Ref. [6]). Spontaneous polarization values were taken from Ref. [7]. According to the surface polarity definition given in Reference [7], the electron concentration enhancement corresponds to a gallium-terminated top surface.

In Fig. 3, we plotted the calculated band diagrams for $Al_{0.15}Ga_{0.85}N/GaN/In_{0.14}Ga_{0.86}N/GaN$ heterostructures with different In concentrations and doping levels in InGaN/GaN. Fig. 3 shows that a second quantum well in the same GaN channel should exist at the GaN/InGaN heterointerface. The calculated sheet electron density for this structure is plotted in Fig. 4 for different In concentrations and doping levels in InGaN/GaN. The results for In=0% are for $Al_{0.15}Ga_{0.85}N/GaN$ heterostructures. For AlGaN/GaN, the contributions to n_s are almost evenly divided between the piezoelectric- and spontaneous polarization. For InGaN/GaN layers, the main contribution to n_s is from strain, since spontaneous polarizations of GaN and InN are nearly equal [7]. As can be seen from the figure, n_s increases with an increase in the In concentration and doping level in InGaN/GaN layers.

Since our heterostructures were grown on a thick GaN buffer layer, we assumed that all GaN layers are strain-free and AlGaN and InGaN are strained to fit GaN. In real heterostructures, due to growth conditions, the strain distribution might differ from the ideal one, especially in the structures with several quantum wells. This might be the reason for a non-monotonous dependence of n_s on the number of the QWs. More theoretical and experimental studies are needed in order to understand this dependence.

IV. SUMMARY

We proposed and fabricated a series of $Al_{0.15}Ga_{0.85}N/GaN/[In_{0.14}Ga_{0.86}N/GaN]_n$ MQWs with n ranging from 0 to 4. The measured electron sheet density varied between 0.8 $x10^{13}$ and 1.8 $x10^{13}$ cm^{-2} depending on the number of the QWs. The measured mobility varied from 550 $cm^2/V\text{-}s$ to 1,350 $cm^2/V\text{-}s$. Our experimental data and calculations show that the electron sheet density can be enhanced in AlGaN/GaN/InGaN/GaN structures with a thin GaN layer.

ACKNOWLEDGMENTS

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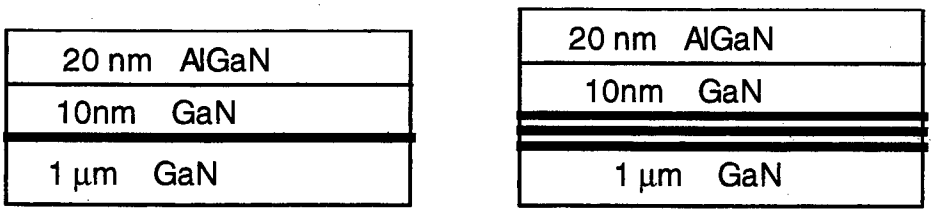


Fig. 1. Schematics of grown AlGaN-GaN-InGaN MQW structures. Structures with 1 QW and 3 QWs are shown. InGaN thickness is 3nm; QW separation is 5-6 nm.

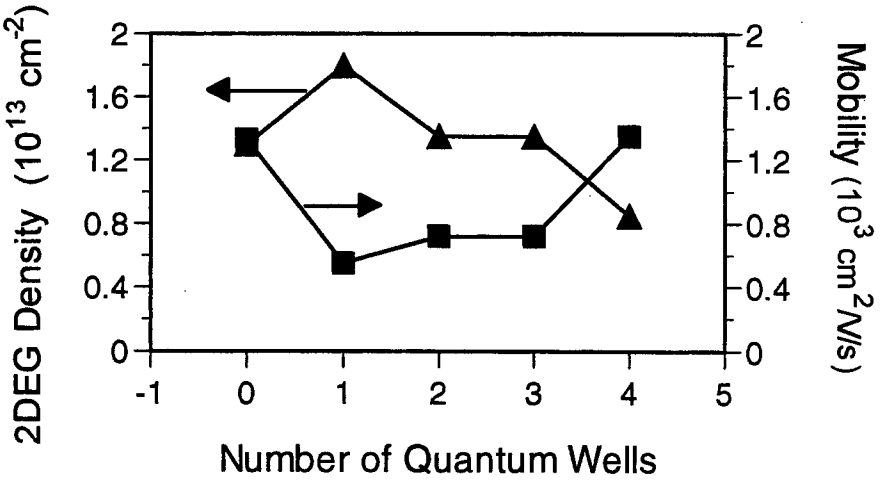


Fig. 2. Measured 2DEG density and mobility for grown structures with different number of quantum wells.

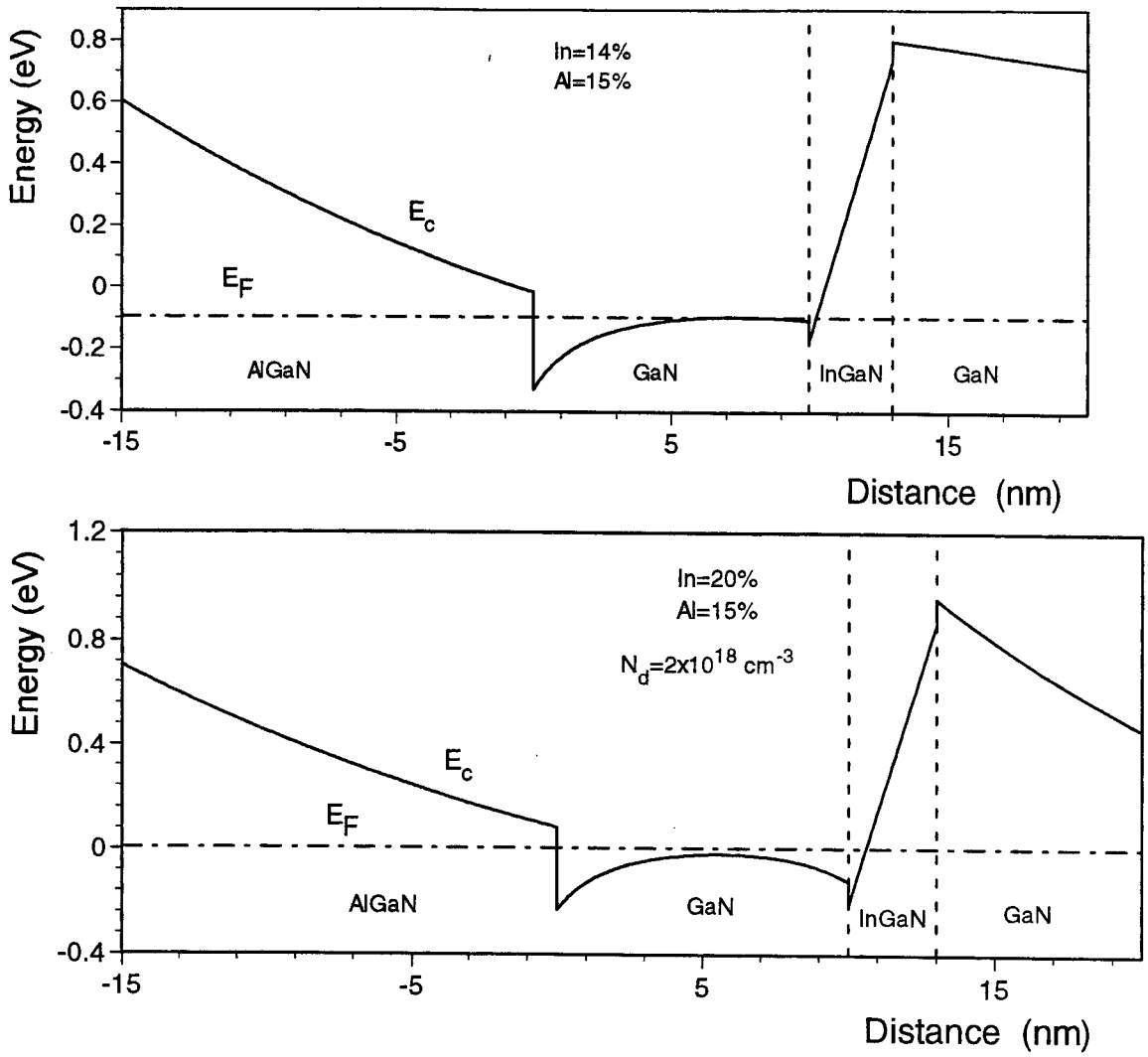


Fig. 3. Calculated band diagrams for AlGaN/GaN/InGaN/GaN structure for different In concentrations and donor concentrations in GaN and InGaN. Donor concentration in AlGaN is 10^{18} cm^{-3}.

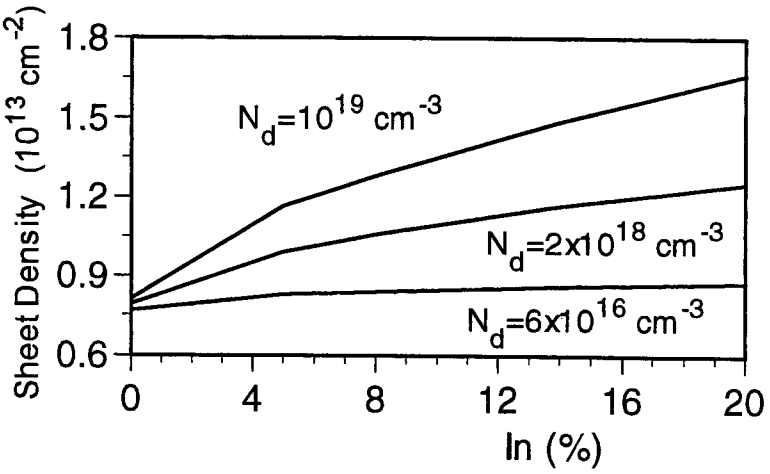


Fig. 4. Calculated 2DEG density in $Al_{0.15}Ga_{0.85}N/GaN/In_yGa_{1-y}N/GaN$ structure for different donor concentrations and In concentrations.

Designing high-performance SiC GTO thyristors using observations made with simulations and measurements

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Introduction

Semiconductor switches that can handle very high power are in increasing demand for power-conditioning circuits. Although silicon insulated-gate bipolar transistors are the devices of choice for switching moderate to high power, and silicon gate turn-off (GTO) thyristors are used for switching very high power, silicon carbide may redefine the operational range of these devices. SiC has the advantage of faster switching, not only because its electron saturation velocity is higher than that in silicon, but also because its larger breakdown voltage allows the use of thinner regions to support the high off-state voltages. Other advantages of this wide-bandgap material include lower leakage currents at higher temperatures and the ability to avoid catastrophic destruction at temperatures higher than that which silicon devices can withstand.

At the moment, the high-power SiC device being most actively investigated is the GTO thyristor, because it is most amenable to current fabrication processes and can block very high voltages, has a low on-state voltage drop, and can switch on and off quickly. Recent reports mention structures that exhibit less than 100-ns switching speeds [1], 1000-V blocking, switching of 5000 A/cm^2 [2], and switching of 10 A when paralleled [3].

We performed two-dimensional drift-diffusion model simulations and measurements on a number of SiC GTO thyristor structures and learned a great deal. We present our findings on how to optimize the performance of SiC GTO thyristors by optimizing the various regions concentrations and thickness. We also discuss different methods of connecting the gate drive circuit to the SiC GTO thyristor and how the controllable power can be increased by taking advantage of the portion of this device that presents just two back-to-back *p-n* junctions to the load current.

Simulation and Measurement Procedures

Unless otherwise indicated, the device structure we describe below consists of a substrate with epilayers deposited and denoted from top to bottom as the anode (*p*-type region), *n*-type base, drift region, *p*-type buffer region, and substrate (*n*-type). Mixed-mode simulations were performed with Silvaco's Atlas/Blaze software. We used models with SiC material parameters to account for incomplete ionization of impurities, concentration-dependent mobility, Shockley-Read-Hall and Auger recombination, and impact ionization. We provide details about these models elsewhere [4]. The devices used to verify some of the simulation results were fabricated as described by Geil et al [5]. To increase the load current that can be switched by the thyristor, we introduce an electrical contact that is physically touching one of the inner base regions and call it the "subbase" contact. It is through this contact that some of the load current is controlled by the thyristor.

Results

The simulation results in the off state and at low current densities compare well with steady-state I-V measurements from room temperature up to 400 °C. However, as the current increases, there is some difference, which may be due to the lack of a good model for bandgap narrowing or Auger recombination.

Obtaining an on state with a low voltage drop and an acceptable holding current is an important issue in designing SiC GTO thyristors. For a typical structure that blocks 2000 V as demonstrated in figure 1, we observed that the n-type base should be doped less than 1×10^{18} cm^{-3} for good hole injection from the anode. Also, the on-state properties are SRH carrier lifetime dependent. This same thyristor structure demonstrated a holding current of 6000 A/cm^2 with lifetimes of 100:50 ns, and this holding current decreased to 1 A/cm^2 as the lifetimes increased to 400:200 ns. Furthermore, the acceptor ionization energy also plays an important role in the on-state characteristics, because simulation results indicate that the holding current changed five orders of magnitude as the ionization energy changed from 161 meV to 251 meV.

The blocking voltage of the typical structure mentioned above increased 400 V for each 3-μm increase in drift region thickness. For one particular case, increasing the surface charge was observed to reduce the maximum voltage blocked from 1000 to 150 V [4]. This is due to the enhanced impact ionization that takes place at the charged surface, and suggests that surface effects may also be very important in determining off-state characteristics.

Transient operation issues

If the *n*-type buffer region concentration is too high the SiC thyristor can still turn on but not latch on. On the other hand, one can increase the *p*-type buffer region's concentration to improve the turn-off gain. Simulations indicate that the curve of turn-off gain vs. *p*-type buffer region concentration exhibits a minimum. Furthermore increasing the thickness of this layer was seen to increase both the maximum voltages blocked and the turn-off gain. The region that is between both of these buffer layers supports the voltage blocked in the off state, and simulations indicate that it can be either *n*-type or *p*-type without affecting the gate turn-off process regardless of whether the gates are on either an *n*-type or a *p*-type region.

Besides structural issues, other factors come into play in determining the turn-off characteristics of the SiC GTO thyristor. As temperature increases, the turn-off time increases, due to the larger number of carriers that have to be removed from the drift region. However, in some cases at very high temperatures, the mobility reduction is enough to cause the turn-off time to decrease, giving the following turn-off time vs. temperature set: 317 ns (20 °C), 494 ns (200 °C), and 182 ns (400 °C). At 400 °C the on-state voltage drop was over 5 V, rather than below 3 V, as seen at the lower temperature simulations. Furthermore, for several devices investigated, the turn-off gain was observed to increase as the load current increased.

External circuit design

The turn-off gain is always higher when the gate is connected to a *p*-type base region rather than an *n*-type base region. This is because the larger mobility of electrons leads to fewer electrons being removed for a particular gate current, compared to the effect the same gate current would have on a *p*-type base. Where the other end of the gate drive circuit is connected also affects device performance. For one particular structure the following were observed. If the other end of the gate drive circuit is connected to the closest emitter region through the external gate drive circuit, the turn-off characteristics are better. However, when the gate drive is on the *n*-type base, the SiC GTO thyristor will still turn off if the gate is connected to the emitter region furthest from the *n*-type base (the substrate), although in this case the load current momentarily increased 40 percent during the turn off process.

We have also demonstrated that the SiC GTO thyristor can operate in a mode where a portion of the load current is injected at the gate, and the rest is injected at the anode while still latching on and being turned off by a gate signal. For the unoptimized device investigated here, the ratio of the load current entering the gate to that entering the anode (after the GTO thyristor is switched

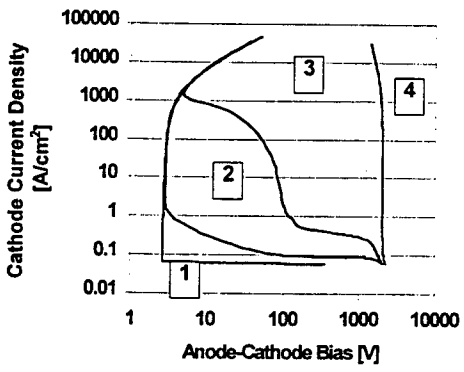
on and before the turn-off gate pulse is applied) is 38 percent at an on-state anode-cathode voltage drop (V_{AK}) of 4.75 V, dropping to 22 percent at V_{AK} = 5.45 V. Measurements indicate that at higher temperatures, the ratio of current injected at the gate to that injected at the anode increases for the same external circuit. In some cases, the gate-to-cathode voltage drop was measured to be less than 0.1 V. The current exiting at the cathode contact was measured to be the sum of the currents entering at the anode and gate contacts.

Simulation results for the structures shown in figure 2 are presented in figure 3. When the subbase and the gate are on the same layer, such as in case 2(b), the gate current does not go to zero until the gate drive circuit's current is turned off (around 8 μs in fig. 3(b)). This is because after the load current has switched off (but before the gate drive has switched off), there will be current flow in the circuit formed by V_G, R_G, R_A, R_B, and the p-base region that the gate is connected to. However, when the gate drive is connected to one region and the subbase contact is on another region, as in case 2(a), the gate drive current will turn off as soon as the load current is switched off. In all cases where the gate drive (V_G and R_G) is connected directly to the p-type buffer layer, the turn-off gain is higher than when the gate drive is connected to the n-type gated base. Moving the gate or subbase contacts laterally away from the main p-n-p-n region slightly increases the switching time.

Summary

We have discussed observations made recently to improve the design of SiC GTO thyristors for optimum on-state and turn-off and blocking characteristics. Ideal on-state characteristics are obtained by good carrier injection and conductivity modulation. High-voltage blocking in the off state occurs if the drift region is thick and the surface charge is not too strong. The transient characteristics can be optimized by proper choice of the p-type buffer region's concentration and thickness. Finally, to improve the power handling capability, a portion of the load current should be injected so that is encounters just two back-to-back p-n junctions in the SiC GTO thyristor.

The authors gratefully acknowledge the technical support of John Conrad and Brett Piekarski of ARL.



	Device 1	Device 2	Device 3	Device 4
N_A	1×10^{20}	1×10^{20}	1×10^{19}	1×10^{20}
N_D	1×10^{16}	5×10^{17}	5×10^{17}	1×10^{18}
N_A	1×10^{15}	1×10^{15}	1×10^{15}	1×10^{15}
N_A	1×10^{17}	1×10^{18}	1×10^{18}	1×10^{19}
N_D	1×10^{19}	1×10^{18}	1×10^{18}	1×10^{19}
N_D	5×10^{18}	5×10^{18}	5×10^{18}	5×10^{18}

Figure 1, Demonstration of degraded on state current-voltage characteristics as hole injection from the anode worsens. The table at the right lists the dopant concentrations in cm^{-3} for the layers from top to bottom of a SiC GTO thyristors with a 12 μm drift region. The electron and hole lifetimes are 400 and 200 ns respectively.

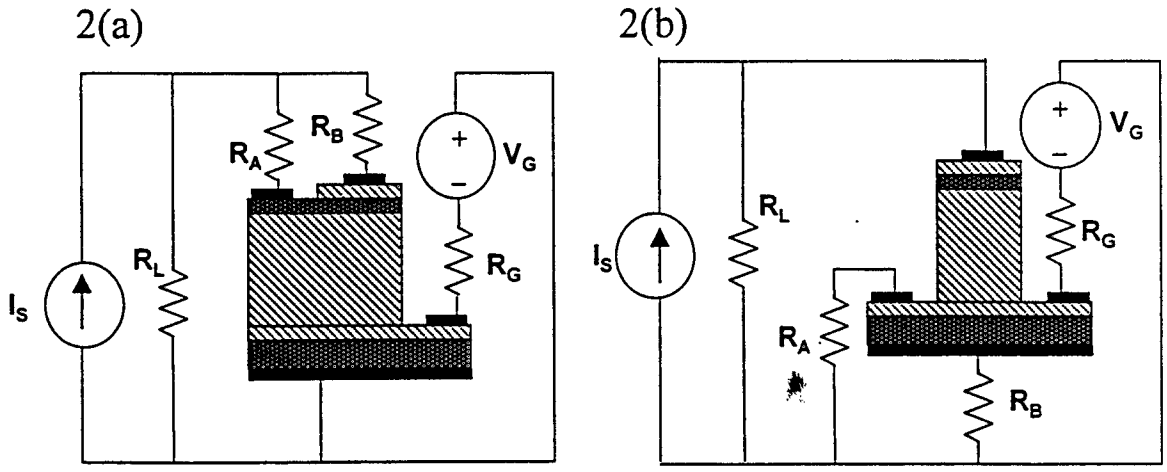


Figure 2. Circuit diagram indicating how the load current should be injected into both the anode contact in series with resistor R_B, and the subbase contact in series with resistor R_A. Dark shaded regions are donor doped, and light shaded regions are acceptor doped. R_L is the load resistor and R_G is the gate drive resistor. From top to bottom of this structure the regions are 1) anode, 2) *n*-type base, 3) drift region, 4) *p*-type buffer layer, and 5) cathode region.

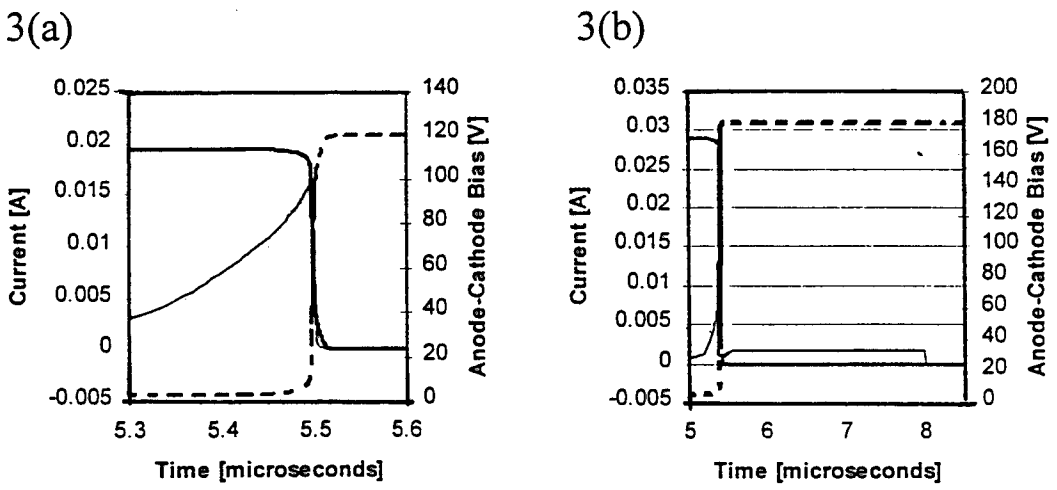


Figure 3. Simulation results for the structures with corresponding letters in figure 2. The thick solid line is the total current being switched by the SiC GTO thyristor, and the thin line is the gate drive current. The dashed line is the anode-cathode voltage drop.

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Frequency Dependent Output Resistance and Transconductance in AlGaN/GaN MODFETs

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I. Introduction

Wide bandgap III-V nitride semiconductors are excellent candidates for high power applications and superior power performance of AlGaN/GaN MODFETs has been reported recently [1]. Circuits designed for power applications such as power amplifiers, oscillators and mixers, operate under large-signal conditions and their performance can deviate significantly from small-signal predicted characteristics in case of frequency dependent device properties. It is consequently very important to understand and if possible control and suppress such dispersion effects. The low frequency output resistance (R_{DS}) and transconductance (g_m) dispersion characteristics of GaAs MESFETs [2]-[3] and GaAs as well as InP-based MODFETs [4]-[5] have been addressed by various groups. However, the dispersion characteristics of AlGaN/GaN MODFETs are not well understood at this point and significant interest exists in this area in order to explain dispersion between DC predicted and high–frequency measured power characteristics. This paper addresses such issues by presenting experimentally evaluated frequency dependent properties of R_{DS} and g_m in AlGaN/GaN MODFETs.

II. Characterization System used for Frequency Dependent Properties of GaN-based MODFETs

Measurements of the frequency dispersion of the output resistance (R_{DS}) and transconductance (g_m) in this study were made by direct evaluation of the AC current and voltage components to determine these parameters [2]. Coaxial transmission lines were employed for signal and bias paths to avoid device oscillation problems and reduce interference. A sense resistor was used to extract the small-signal drain current without influencing the intrinsic device output characteristics. A function generator was employed at the output or input for exciting the device and measuring the output resistance or, transconductance repetitively. The signal across the sense resistor was monitored using a high-resolution oscilloscope and tests were performed in the frequency range of 50 Hz to 100 kHz under small-signal conditions (amplitude ~ 120 to 150 mV). The measurement system was calibrated using different resistive elements at various small signal levels. Measurement verification was also possible by comparing the R_{DS} and g_m values at 50 Hz with DC values obtained from the HP4145B semiconductor analyzer. These tests showed good agreement between measured data presenting further confidence regarding the testing methodology.

III. Measured Frequency Dependent Characteristics of AlGaN/GaN MODFETs

The AlGaN/GaN power MODFETs evaluated in this study were grown using RF-assisted MBE on sapphire substrates. The device structures consist starting from the substrate of an undoped GaN buffer, an NID $Al_{0.22}Ga_{0.78}N$ spacer, n-$Al_{0.22}Ga_{0.78}N$ donor layer and an NID $Al_{0.28}Ga_{0.78}N$ cap layer. The gate length for all devices was 0.25 μm and the gate finger width was 0.1 mm. The devices demonstrated excellent scalability in terms of large-signal power performance and a maximum output density of 1.3 W/mm was obtained at 10 GHz [6]. The frequency-dependent R_{DS} and g_m measurements were performed under a wide range of V_{DS} and V_{GS} bias conditions.

Fig. 1 shows the V_{DS} bias dependence of output resistance dispersion under the same V_{GS} bias condition of the 2-finger (0.25μm × 0.2 mm) device. As can be seen, the dispersion is insignificant in the ohmic region but as V_{DS} increases, the output resistance dispersion increases dramatically. The trend observed resembles that reported for GaAs MESFETs [2]. Under low drain-source bias levels, the current variation

resulting for given V_{DS} change is dominated by the induced variation of carrier velocity and the impact of interface states at the undoped GaN buffer and 2DEG channel interface is insignificant. However, as the device enters the saturation regime, charge redistribution occurs in the channel and is affected by the occupation of the states. As a result, the frequency dependence of output resistance becomes more pronounced.

When the channel was modulated vertically with the help of V_{GS}, the dispersion increased as V_{GS} became more negative (see Fig. 2). This result can be explained by the fact that the channel is beyond thermal equilibrium condition as the gate voltage becomes more negative and free carrier injection into trapping states is enhanced. The injected charge results in an electrical field which modulates the shape of the channel leading therefore to more pronounced frequency dependence.

The measurement results for the frequency dependence of transconductance are shown in Fig. 3 and 4. The frequency dispersion of g_m appears to be much smaller than that of the output resistance over the same range of bias conditions. A similar observation has been previously reported by the authors for InP-based HFETs [4]. These results suggest that the influence of surface conditions which are often responsible for g_m dispersion is small in the AlGaN/GaN MODFETs reported here. The lateral (access) resistance does not consequently vary with frequency and the dispersion is therefore very small.

Consideration of the frequency dependent characteristics of R_{DS} and g_m shows that R_{DS} is reduced by ~ 6% to ~ 44% over the range of bias used for these studies while the g_m reduction ranges from ~ 4% to ~ 10%. It appears therefore that the key parameter effecting device performance when operation is considered from DC to high frequencies is R_{DS}.

Study of the large-signal output power characteristics of the devices showed that the measured RF output power was very close to values predicted from DC characteristics [6]. This good agreement was possible provided that the DC drain current used in the derivations was evaluated under large-signal conditions, as obtained during RF power measurements. Consideration of the good agreement between DC and RF power characteristics, as well as, the pronounced dispersion of R_{DS} but not g_m suggests the following mechanism of operation. As the frequency of operation increases from DC, the evaluated AlGaN/GaN MODFETs maintain their DC value of g_m but present lower output resistance R_{DS}. A suitable value of load impedance needs therefore to be employed in order to allow optimum large-signal operation, as for example occurring in case of load-pull power characterization of the AlGaN/GaN MODFETs. The DC drain current evaluated under high-frequency large-signal matching conditions accounts for the dispersion in R_{DS} characteristics leading to good agreement between DC and RF measured performance.

Overall, the frequency dependent characteristics of the output resistance (R_{DS}) and transconductance (g_m) of AlGaN/GaN MODFETs have been investigated experimentally. The results indicate that the frequency dispersion of transconductance dispersion is much smaller than that of the output resistance. These characteristics provide a better insight of device operation and DC versus HF small-signal and large-signal performances.

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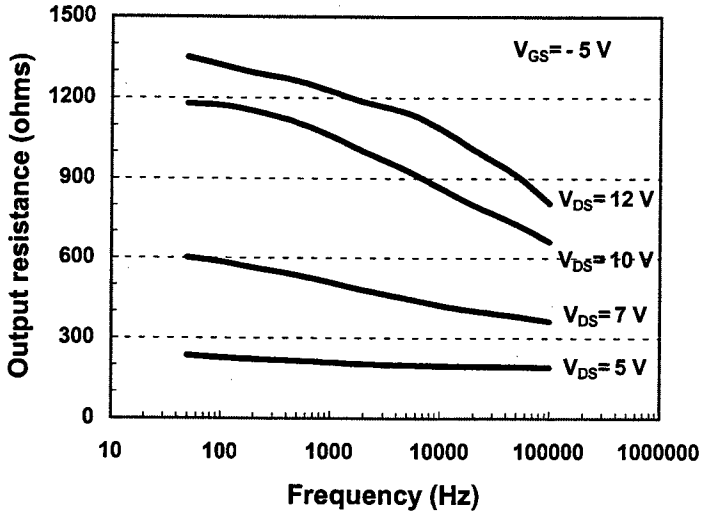


Fig. 1. Measured output resistance as a function of frequency for the 0.25 μm × 0.2 mm device under constant gate-source bias.

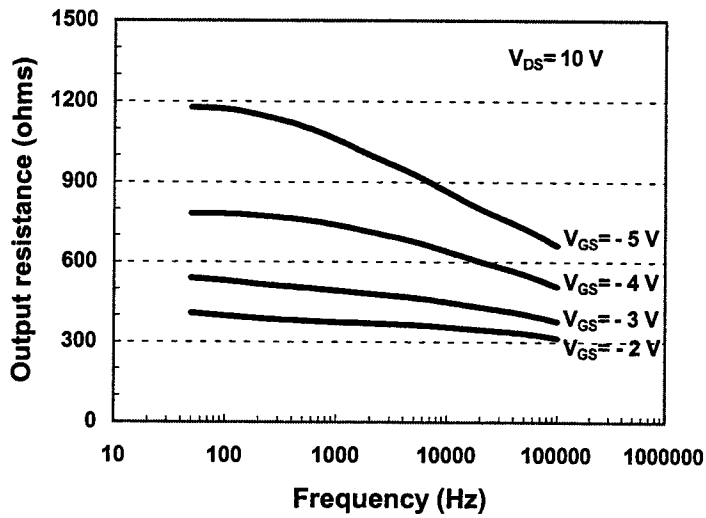


Fig. 2. Measured output resistance as a function of frequency for the 0.25 μm × 0.2 mm device under constant drain-source bias.

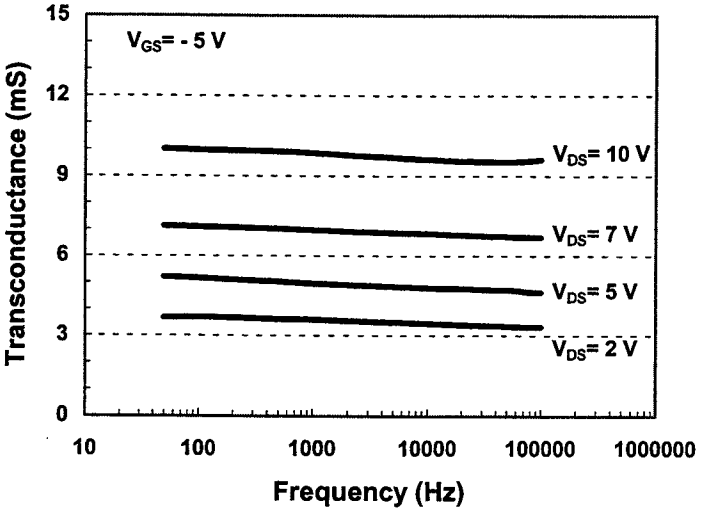


Fig. 3. Measured transconductance as a function of frequency for the 0.25 μm × 0.2 mm device under constant gate-source bias.

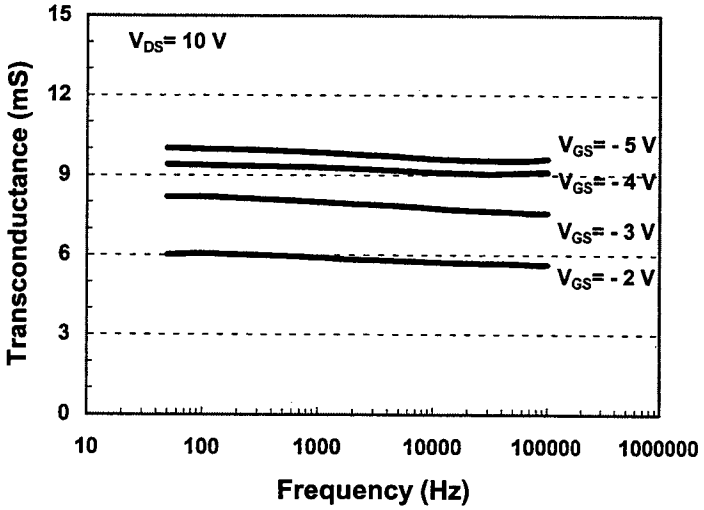


Fig. 4. Measured transconductance as a function of frequency for the 0.25 μm × 0.2 mm device under constant drain-source bias.

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Unipolar Light Emitting Device on the Base of III-Nitride Semiconductor Superlattices

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I. INTRODUCTION

A significant progress has been achieved recently in the field of visible light emitting diodes on the base of wide-band-gap gallium, aluminum and indium nitride semiconductors [1]. However, there is a problem to get a good p-type conductivity for these materials which blocks further development of the high power lasers and light emitting diodes for visible spectral range. To overcome these difficulties we suggest to use for light generation the III-Nitride semiconductors of n-type solely.

The main idea of unipolar light emitting device (ULED) is to create an analogy of n-p junction between two superlattices with a shallow and a deep subbands, Fig.1. The superlattice with shallow subband acts as an effective n-type semiconductor, whereas the superlattice with shallow subband plays role of an effective p-type semiconductor. In the ULED the radiation arises not due to recombination of the electrons and holes as it takes place in usual light emitting diodes but due to the electron transitions from shallow subband superlattice into the deep sub-band superlattice accompanying by the electron energy relaxation via emission of photons. The device works like usual LED at the forward bias, but has a great advantage that it is possible to tune resonantly the sub-band energy position to any optically active two-level quantum structures like quantum wells, impurities or quantum dots at the interface between the superlattices. That allows direct electrical pumping of the optical transitions in the band gap through the superlattices. It is possible to obtain visible light emission using the wide gap nitride superlattices. Connection in a series of three the "n-p junctions" tuned to three basic colors allows get an effective white light source.

II. THEORY OF ULED OPERATION

The physical mechanism of the ULED operation is illustrated in Fig.1. One of the superlattice has a shallow subband, but the another has a deep subband. Under the n-type doping the chemical potential in the superlattice with the shallow subband is higher then in the superlattice with the deep one. When the superlattices are in contact their chemical potentials becomes equal and it results in a built-in electric field at their interface. The resulting electric potential $U(x)$ can be found from the Poison equation accounting the two-dimensional character of the electron state density into the superlattice with one subband:

$$\varepsilon \frac{\partial^2 U}{\partial x^2} = \frac{em^*}{\pi \hbar^2 a_{SL}} (\mu - E_i + eU)\theta(\mu - E_i + eU) - eN_D \qquad (1)$$

where ε is the dielectric constant, e and m^* are charge and the effective mass of electron, a_{SL} is the lattice constant of the superlattice, μ is the chemical potential, E_i is the energy position of the sub-band minimum, index i =1,2 numerates the superlattices, i = 1 at $x < 0$, i = 2 at $x > 0$, N_D is donor concentration. Eq.(1) is valid for heavily doped single subband superlattices with degenerated carriers.

When difference in the chemical potentials μ_1 and μ_2 is smaller than $2(\mu_1 - E_1)exp(a_{SL}/2l)$ the effective p-n junction is symmetrical, where E_1 is the energy position of the subband

minimum for the superlattice, $l = e\sqrt{\pi\varepsilon a_{SL}/m^*\hbar^2}$. The corresponding dependence of the electric potential on the distance from the interface for unbiased effective p-n junction found from the equation (1) is:

$$U(x) = sign(x)(\mu_2 - \mu_1)(1 - e^{-|x|/l})/2e \tag{2}$$

where $sign(x) = +1$ at $x > 0$, $sign(x) = -1$ at $x < 0$.

For a difference in the chemical potentials larger than $2(\mu_1 - E_1)exp(a_{SL}/2l)$ the effective p-n junction is asymmetrical and the solution of the equation (1) for unbiased p-n junction is

$$U(x) = \begin{cases} U_1 = (U_2)^2/2U_0, x < -x_0 \\ -\dfrac{eN_D}{2\varepsilon}x^2 - \dfrac{U_2}{l}x, -x_0 < x < 0 \\ U_2\left[\exp\left(-\dfrac{x}{l}\right) - 1\right], 0 < x \end{cases} \tag{3}$$

where

$$U_0 = \frac{\pi\hbar^2 a_{SL} N_D}{m^* e},\ U_2 = U_0\left(\sqrt{\frac{2(\mu_1 - \mu_2)}{U_0} + 1} - 1\right) \tag{4}$$

In this case, a depletion region with empty quantum wells is formed in the superlattice with the shallow subband, Fig.1.

Under direct bias these empty quantum wells become gradually populated and the depletion region gradually disappears. The quantum well closest to the interface becomes populated under the bias V equal to $\mu_1 - \mu_2 - 2(\mu_1 - E_1)exp(a_{SL}/2l)$. Under this bias, a depletion region becomes symmetrical, the effective p-n junction opens and electrical current start to flow through the device. Corresponding equations for the electrical potential and the electrical density j are

$$U(x) = sign(x)(\mu_2 - \mu_1 - eV)\{1 - \exp(-|x|/l)\}/2e \tag{5}$$

$$j = en\theta(n)/\tau \tag{6}$$

$$n = \mu_1 - E_1 + (eV + \mu_2 - \mu_1)\exp(-a_{SL}/l)/2 \tag{7}$$

where τ is the characteristic time of the electron transition from the superlattice with the shallow subband to the superlattice with the deep subband via tunnelling and subsequent emission of photons and phonons. Above we assumed that the following inequalities are satisfied $\mu_1 - \mu_2 >> kT$, $\mu_1 - E_1 >> kT$ и $\mu_2 - E_2 >> kT$.

III. QUANTUM EFFICIENCY OF ULED

The internal quantum efficiency η of the device is determined by the ratio of the photon and phonon emission times τ_{photon}, τ_{phonon}

$$\eta = \tau_{phonon}/(\tau_{phonon} + \tau_{photon}) \tag{8}$$

Calculation of τ_{phonon} and τ_{photon} for the simplest case of the active layer made of single square quantum well with two 2d-subbands, one of which is deep with the minimum energy position

$-E_1$ and another is shallow with the minimum energy position $-E_2$ with respect to the conduction band edge, gives

$$1/\tau_{\text{phonon}} = \frac{512e^2am^*\omega_{phonon}}{81\pi^3\hbar^2\bar{\varepsilon}}\left(1-\frac{1}{x}[\arctan\{x\}]\right), \text{ where } x=\frac{\pi\hbar}{a\sqrt{2m^*(E_1-E_3)}} \quad (9)$$

and

$$1/\tau_{photon} = 128e^2\hbar n\omega_{photon}/27m^{*2}c^3a^2 \quad (10)$$

where ω_{LO} is the longitudinal phonon frequency, $\bar{\varepsilon}^{-1}=\varepsilon_\infty^{-1}-\varepsilon_0^{-1}$, ε_∞ and ε_0 is the optical and static dielectric constants respectively, $\hbar\omega_{photon}$ is the energy of the emitting photon quanta, a and U_0 are quantum well width and depths and m^* is the effective electron mass.

As can be seen from Eqs (8-10), the internal quantum efficiency increases with the increase of the light frequency. Qualitatively, it results from $\sim 1/q^2$ decay of the matrix element for electron-polar optical phonon interaction with increase of phonon momentum **q**. In the optical spectral region for the active layer made of single III-nitride quantum well Eqs. (9-10) give $\tau_{phonon} = 1.3\ 10^{-12}$ s , $\tau_{photon} = 5.3\ 10^{-10}$ s and $\eta \sim 0.2\%$. This value is rather small for practical applications.

A significant increase in the efficiency can be achieved with use of the active layer with the optical transitions from the quantum well subband to the impurity band related to a deep acceptor. For this active layer the single phonon emission is forbidden by the energy conservation law and τ_{phonon} in Eq.(8) is determined by multiple phonon emission processes which are orders of magnitude slower (by factor $\sim \exp\{\omega_{\text{photon}}/\omega_{\text{phonon}}\}$ at low temperature).

In GaInN/AlN superlattices the thransition metals Fe and Ni are good candidates for the deep acceptors. The corresponding acceptor energy levels are ~ 3 eV above the edge of the valence band and the optical transition from quantum well subband to the acceptor level can be tuned to any position in the visible spectral range. The photon emission time in this case can be estimated as $\tau_{photon} \sim 10/BN_a = 10^{-10}$ s for $N_a = 10^{21}$ cm^{-3}, where $B = 10^{-10}$ cm^3/s is van Roosbroek and Shockley radiative constant [2], N_a is the acceptor concentration in the active layer and factor 10 arises from 0.1 admixture of the nitrogen p-orbitals to the transition ion d-orbitals estimated with the empirical tight-binding parameters [3]. Thus, high efficiencies of ULED can be achieved using the active layers with the optical transitions from quantum well subband to the transition metal impurity band.

IV. SUMMARY

We have suggested unipolar light emitting device based on III-nitride superlattices for generation of visible light. This device allows to overcome problems related to low conductivity of p-type III-nitride semiconductors.

The efficiency of the device is limited by the non-radiative channel related to the phonon emission and is rather low for the active layer with the optical transitions between quantum well subbands. A suppression of the phonon non-radiative recombination channel and significant increase in the efficiency can be achieved using the active layers with the optical transitions from quantum well subband to transition metal impurity band.

A serial connection of unipolar light emitting devices allows to increase the output power and obtain any spectra in visible region, including white light via combination of different pairs of the superlattices.

With a resonator adjusted the structure made of the same pairs of the superlattices allows, in principal, to obtain a laser for visible spectra region similar to the infrared cascade laser suggested by Kasarinov and Suris [4] and realized recently by Faist et al [5].

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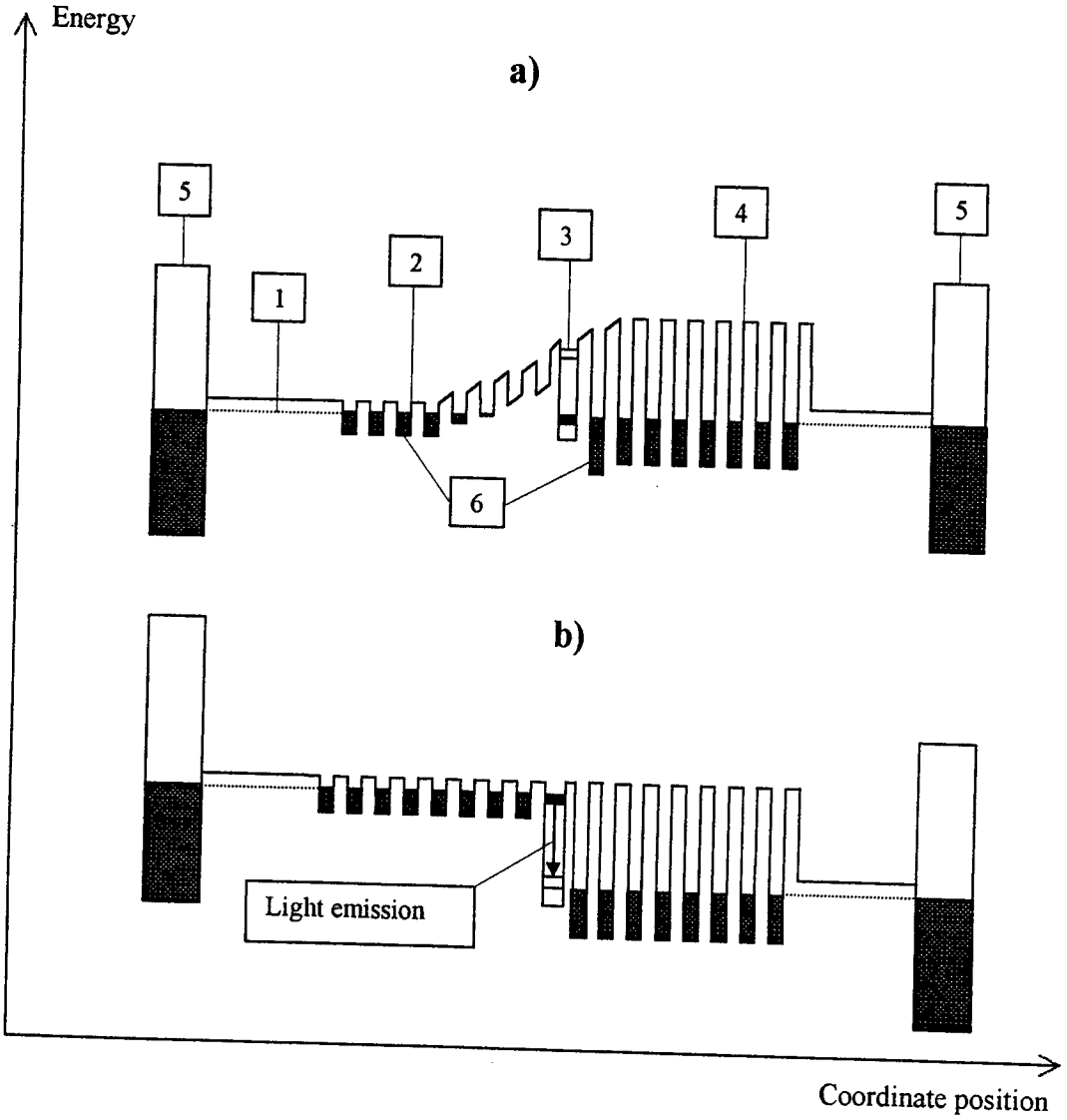


Fig.1. Schematic energy band diagram for the unbiased (a) and biased (b) ULED structures.

1 - chemical potential position; 2 - shallow subband superlattice; 3 - active layer; 4 - deep subband superlattice; 5 – contacts; 6 - electrons

The control of GaN microstructure and its impact on device performance

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I. Introduction

The III-N materials system is attractive for high-power microwave applications due to the large breakdown voltage of the wide bandgap materials, as well as to their ability to realize high sheet carrier densities in the two-dimensional electron gas (2DEG) region at the AlGaN/GaN interface. A large $n_{sheet}\mu$ product is required for power applications, which mandates high electron mobility as well. Defects and trapping centers, located either at interfaces or within the bulk of GaN and AlGaN thin films, have been observed and have been associated with reduced mobility, persistent photoconductivity, and current collapse which degrade device performance. We have observed that use of high Mg dopant flows has resulted in microstructural defects that may limit the activation efficiency of p-type GaN.

It is well known that heteroepitaxial growth of GaN thin films on sapphire initiates as an assemblage of crystallites, or grains, that coalesce into a two-dimensional film [1]. Despite the smooth surface, the GaN films have typical dislocation densities of 10^8 to 10^{10} cm^{-2}. These dislocations are due in part to the size and relative orientation of the grains, which are determined by the crystal growth process parameters. Recently, we have observed [2] that growth pressure strongly influences the grain size of GaN films. In this presentation, we will discuss how to increase the grain size of GaN films and suggest how the increased grain size improves high electron mobility transistor (HEMT) device performance by reducing scattering, trapping or compensating defects in the GaN films. We also present evidence of grain boundary inversion caused by high Mg dopant flows, and discuss the potential implications of film microstructure on p-type activation in GaN.

II. HEMT and GaN:Si structure and transport properties

$Al_{0.26}Ga_{0.74}N$:Si/GaN heterostructures have been grown under conditions in which the highly resistive GaN film has large grain size, as illustrated in Figure 1. The $Al_{0.26}Ga_{0.74}N$ film thickness was approximately 250 Å, of which the top 200 Å was silicon doped. The underlying HR-GaN film thickness was approximately 2.5 microns, with a measured resistivity of 10^5 Ω-cm and grain size on the order of 5 μm. A 300K Hall mobility of 1500 cm^2/Vs was measured for $n_{sheet} = 1.2 \times 10^{13}$ cm^{-2}, and at 77K, $\mu = 4000$ cm^2/Vs and $n_{sheet} = 1.3 \times 10^{13}$ cm^{-2}. Pulsed microwave power measurements of devices fabricated on this material yielded 5.9 W/mm with 37% power added efficiency and 12 dB gain at 3.8 GHz. These devices also exhibited minimal current collapse, and drain lag was eliminated. The electrical properties of the large grain GaN HEMT structure are considerably better than in similar HEMT structures in which the underlying HR-GaN was grown under conditions that yielded smaller GaN grain size.

The relationship between GaN microstructure and electron transport was studied by the growth of a controlled set of Si-doped GaN films at process pressures ranging

from 39 to 200 torr. All other process parameters were held constant, including SiH_4 dopant flow. The details of growth are reported elsewhere [3]. The growth time for each GaN film was adjusted to yield a film thickness of approximately 1 μm, since the GaN growth rate decreases with increasing pressure due to enhanced GaN decomposition [4]. The measured electron concentration, shown in Figure 2, varied by a factor of six over the pressure range studied, while the growth rate varied by a factor of two. This suggests increased electron compensation at lower pressures rather than just a simple reduction in Si due to volume incorporation. For increasing growth pressure, the electron mobility increases from 10 cm^2/Vs at 39 torr to 445 cm^2/Vs at 130 torr, even though the electron concentration increased. This anomaly has been modeled as the contribution of dislocation scattering [5], but the present work suggests that dislocations may actually group to form grain boundaries. In Fig. 3, TEM cross sections of the films show an increase in grain size with increasing growth pressure, from 0.2 μm at 39 torr to 2-5 μm at 130 and 200 torr. Dislocation density varied only by a factor of two in these films, at a level of approximately 10^9 cm^{-2}. X-ray analysis confirmed a reduction of edge-type threading dislocations, believed to form the grain boundaries [6], in the higher pressure films. Photoluminescence (PL) analysis revealed a 3.0 eV emission peak in the 39 torr film that is not seen in the films grown at higher pressures. The 3.0 eV band is commonly observed in the PL spectra of highly resistive GaN films. Analysis of the films based on a single donor/single acceptor conduction model indicated near total compensation in the 39 torr film, a 0.9 compensation level in the 65 torr film, and a compensation level of 0.6 for the 130 and 200 torr films.

We have observed that the resistivity of GaN films, both unintentionally-doped and silicon-doped, decreases with increased growth pressure. A highly resistive GaN buffer layer is required for pinchoff and high frequency performance of HEMT-type devices. This would suggest that GaN growth at low pressure is optimal for HEMT devices. However, our results indicate that the low pressure growth conditions which lead to the compensating centers in highly resistive GaN also limit the electronic transport properties in the HEMT films. It appears that the best highly resistive GaN layers should be grown under conditions that yield an adequate deep acceptor concentration to just compensate the background donors.

III. GaN:Mg structure and transport properties

GaN growth for electronic device applications is optimized to yield smooth, large grained films, which have a Ga-terminated polarity. Growth of GaN directly on sapphire without an intermediate nucleation layer results in hexagonal faceted N-terminated films that typically exhibit n-type conduction. Recent experiments in our laboratory on the growth of p-type GaN by Mg-doping have demonstrated that very high Mg precursor flows result in GaN:Mg fims having a rough surface with faceted hexagonal morphology. Dark field TEM imaging and convergent beam electron diffraction techniques have shown these films to be N-terminated. Evidence of polarity reversal for films grown with high Mg precursor flows may be associated with the introduction of microstructural disorder, and would be consistent with a reduction of hole concentration as the Mg concentration increases above approximately 1 x 10^{19} cm^{-3} [7].

IV. Summary

In summary, the growth pressure has been found to strongly influence the microstructure of heteroepitaxial GaN films. Transport properties in Si-doped GaN and unintentionally doped GaN films also vary dramatically with growth pressure, resulting in reduced compensation levels at higher growth pressures. The present study suggests that a correlation may exist between grain size and compensation in GaN films. Pressure may influence additional compensating centers such as point defects (Ga- or N-vacancies), or impurities such as carbon or oxygen. The identification and control of compensation centers in the GaN films is expected have a profound impact on p-type doping efficiency and trapping effects, and are the subject of continued investigation.

Acknowledgements

This work is supported by the Office of Naval Research.

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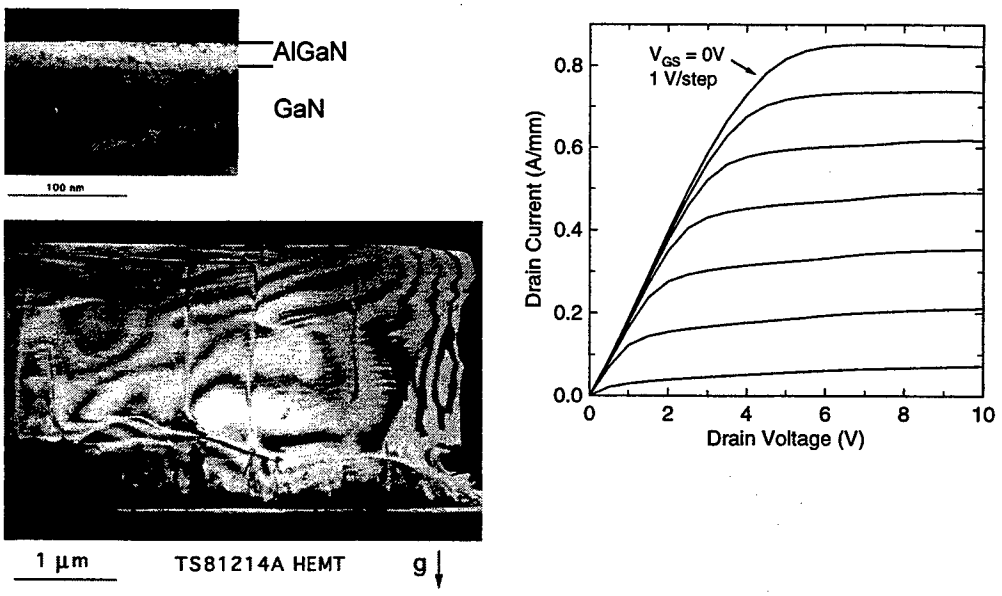


Figure 1. a) XTEM image of AlGaN/GaN HEMT device structure, in which an average grain size of 5 µm is observed in the HR-GaN film. Inset shows the AlGaN/GaN interface, exhibiting roughness on the order of 5-10 Å (100 nm marker); b) I/V characteristics of device.

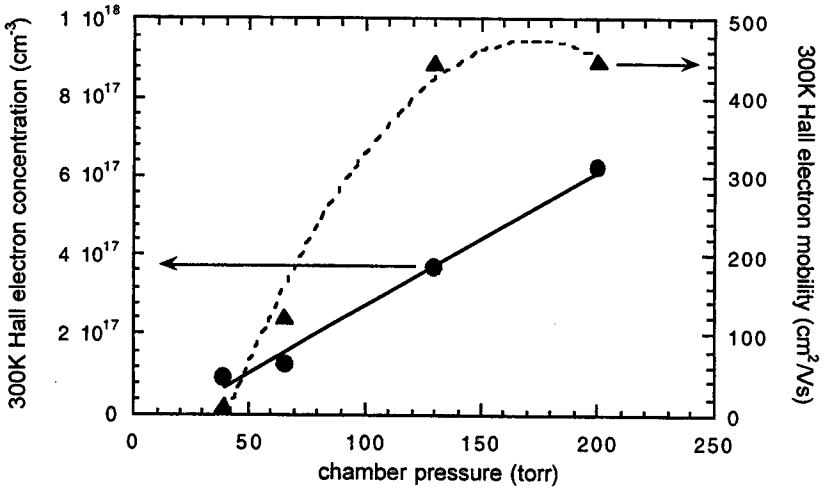


Figure 2. 300K Hall electron electron concentration and mobility of silicon doped GaN films grown at varying pressures.

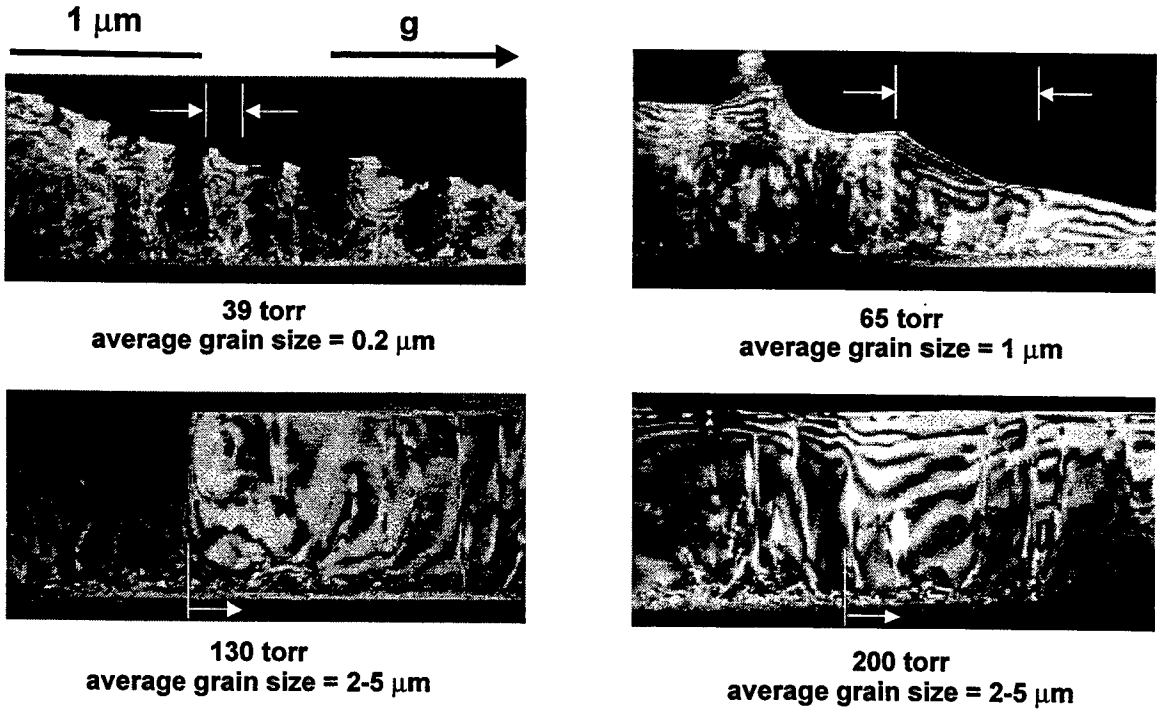


Figure 3. XTEM images illustrating the influence of growth pressure on grain size in controlled growth of GaN:Si films. The average grain sizes and growth pressures for the films are as indicated beneath each image.

An Intelligent TCAD System for Design of High Voltage IGBTs

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Abstract

This paper describes an intelligent TCAD system which can be used in design of high voltage IGBTs. The system, comprising process and device simulators and the RSM optimiser, has been applied to fabrication of a third generation trench gate IGBTs in the 1.4 kV class. The use of this new TCAD system has contributed largely to realizing devices with characteristics far superior to the previous DMOS generation of IGBTs. Full experimental results on 1.4kV Trench IGBTs which are in excellent agreement with the TCAD predictions are reported. The experimental results show exceptional on-state/short-circuit/switching performance with at least 30 % improvement compared to state-of-the art IGBTs.

1 Introduction

In the last few years, the area of high voltage semiconductor devices has expanded rapidly, either through inventions of new device concepts or optimization of existing devices [1-11]. In both cases, high performance can only be achieved by careful device design and optimization.

Extensive research carried out on high voltage devices using trench technology resulted in major improvements compared to the standard DMOS technology such as enhanced latch-up protection, lower on-state voltage drop, higher packing density and more flexible design. In this class, the Trench Insulated Gate Bipolar Transistor (TIGBT) is the most promising structure for the next generation of power semiconductor devices with wide applications ranging from motor control (1.4 kV) to HVDC (6.5 kV). Increased device complexity introduced by using the trench design highlited the importance of the optimisation procedure in the process of fabricating the device which will fulfil the requirements of a particular application.

We have reported previously [8] the process development of high voltage Trench IGBTs and discussed key issues such as oxide breakdown voltage and tunnelling current, channel mobility, surface roughness and edge terminations. In this paper we concentrate on advanced modelling and optimisation of the forward characteristics of Trench IGBTs with experimentally verified models for maximum controllability and short-circuit protection with no compromise in the on-state performance. For this purpose we created a fully integrated TCAD system based on TMA-Avant software [12] which includes the 2D process simulator TSuprem4, device simulator Medici and the RSM module of the TMA Workbench and employed it for the design of 1.4kV TIGBTs. It should be noted that this TCAD system can be applied to different problems of device optimisation and can be particulary helpful for better understanding of new or modified existing power devices.

2 Optimisation

The TCAD system used for optimisation of 1.4kV TIGBTs is given in figure 1 and the cross-section of a typical Trench IGBT half cell is shown in figure 2. The aim was to realize an optimum trade-off between the on-state performance, device controllability and wide safe operating area (SOA). An optimum 1.4 kV device must have a breakdown voltage (Vbr) of at least 1.5kV, a reduced on-state voltage drop (Va) at the operating current density (e.g. 100 A/cm^2) to minimise the on-state power losses and very importantly a low saturation current (Isat) to widen the Safe Operating Area (SOA) and to increase the endurance time in short-circuit conditions. Hence, the design goal is to select the critical process parameters and determine their optimum values so that the fabricated device fulfils these requirements.

We have previously reported [3] that a large accumulation layer length (given by the effective depth and the width of the trench) results in higher electron current injection and therefore enhanced modulation at the cathode

side, hence lower n-base resistance. Moreover, a large accumulation layer length significantly decreases the saturation current since more of the holes recombine with the electrons in the vicinity of the accumulation layer, thereby increasing the proportion of the electron current through the channel and facilitating current saturation in the Trench IGBT due to MOSFET pinch-off. Five process and geometrical parameters were selected as the most important for obtaining the desired Trench IGBT: the p base implantation dose, the p base drive-in time, the trench depth (d), the trench width (w) and the spacing between two trenches (s). The expected values of optimum process parameters and the range of their fluctuations (given in table 1) are used to build a full factorial design matrix [13]. An example of the full factorial design matrix for two parameters is given in Fig. 3. Each of the points in this figure represents an experiment (i.e. a different TIGBT simulation) with the corresponding input values X1 and X2 selected as shown in the graph, taking into account that:

$X_i(0) = X_c, \quad i = 1, 2$, (central value)

$X_i(\pm 1) = X_c \pm dX_i, \quad i = 1, 2$

$X_i(\pm t) = X_c \pm dX_i \cdot t, \; t = 1, \; 1.5 \; or \; 2$ (min and max values),

and dX_i is a step value selected for each parameter. Therefore, for 2 input parameters, there are 9 structures defined with different combinations of X1 and X2 and for n input parameters, there will be $n^2 + 2n + 1$ necessary simulations. By importing all combinations of process parameter values given by the design matrix into the corresponding process steps, 43 different devices were simulated using the process simulator Tsuprem4. These structures were further incorporated into the device simulator Medici in order to obtain the values of Vbr, Isat and Va for each of the devices. The created pairs of (process-parameters, device-characteristics) for the 43 simulated devices were subsequently imported into the RSM optimiser. An appropriate analysis of the correlations between process parameters and device characteristics was carried out in order to select the best fitting polynomial models. After achieving an acceptable accuracy (typically 1%) of the optimisation algorithm, the desired values for Vbr, Isat and Vsat were imported into the input of the RSM model and the optimum values of process parameters were prompted at the output.

To assess the accuracy of the obtained result, these optimum values of the process parameters were fed back into the process/device simulators. The values of Va, Isat and Vbr obtained after simulating the TIGBT using the optimum process parameters' values given by the RSM model are compared with the desired values of responses (table 2) showing high accuracy of the RSM model.

3 Device Fabrication

Prototype devices with a chip area of 36cm$^-$4 and full devices with a chip size of 0.25 cm^2 using both hexagonal and stripe lay-out have been fabricated. The hexagonal lay-out (figure 5) offers a higher cell density and allows easier pad contacts and hence was our preferred option. The trench was carefully controlled (figure 6) to eliminate high electric fields which would otherwise lower the breakdown capability. The gate oxide electric field strength supported by experimental devices was in excess of $6{\cdot}10^6$ V/cm. Unlike in other trench processes reported in the literature we did not encounter difficulties with bird's beak at the top corner of the trench which may increase significantly the series on-resistance. The trench surface was very smooth and the channel mobility was estimated to 600 cm^2/Vs using measured I-V characteristcs of lateral trench MOSFETs and numerical extraction procedures [8].

The contact of the n+ cathode/p base was realized using a second silicon etch. This contact gives a satisfactory gate yield, a low series resistance and a high channel density. In addition, if the trench contact penetrates through the n+ cathode layer, the latch-up immunity is further increased even during inductive switching or short-circuit conditions.

4 Results and Discussion

The measured breakdown was in excess of 1.4kV. The on-state voltage drop for non-irradiated Trench IGBTs was 1.1V which to the authors' knowledge represents the best reported result in the literature for the 1.4kV IGBT class. The saturation current at $V_G - V_T = 12V$ was 650 A/cm^2. This resulted in an endurance time of over 20μs in short-circuit conditions at 600V (figure 5). The switching time for non-irradiated devices was high, as expected, but fell to 0.5 μs

when the devices were irradiated with a dose of 16MRad. In this case the on-state voltage drop raised to 2.1 V. In addition, NPT Trench IGBTs were fabricated using the same process parameters [11] which further advanced the switching performance and enhanced device controllability. These devices are currently available on a sample basis. Figure 6 shows the I-V characteristics of both manufactured and prior to manufacturing simulated non-irradiated TIGBTs. The simulated characteristics are graphycally superimposed on the actual photograph of measured I-V curves for comparison purposes proving high accuracy of the created TCAD system.

5 Conclusion

We have constructed a TCAD system for optimising the high voltage trench IGBTs and employed it in the design of Trench IGBTs in the 1.4KV class. We have used our TCAD system to predict accurately the performance of these devices in all operation modes and to optimise geometrical and process parameters to give optimum trade-off between on-state and SOA. The results are in excellent agreement with the experimental data. One can also use this sytem to optimise the switching/on-state trade-off in an IGBT and in a more general context to design other semiconductor devices such as MOSFETs, bipolar transistors or bipolar-MOS devices.

Acknowledgement

The authors are grateful to Mitel Semiconductor trench devices team for fabricating the 1.4kV TIGBTs. T. Trajkovic acknowledges the award of COT and Kings College scholarships. F. Udrea acknowledges the award of an advanced research fellowship from the UK Engineering and Physical Sciences Research Council (EPSRC). The authors thank Avant and Silvaco for providing the simulation tools used in this paper.

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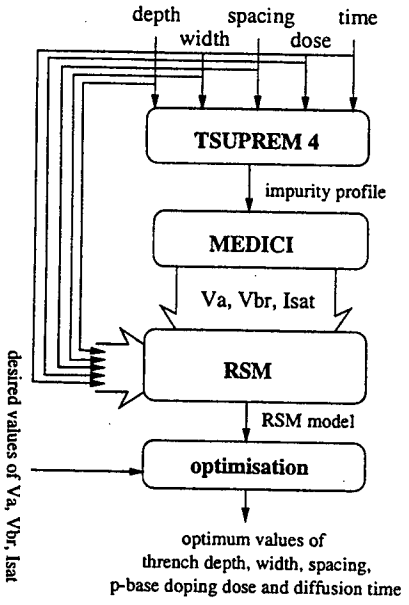


Figure 1: TCAD system created for 1.4kV TIGBT optimisation.

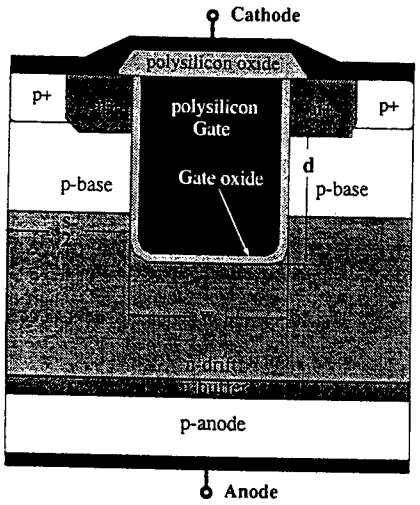


Figure 2: 1.4kV punch-through TIGBT cell.

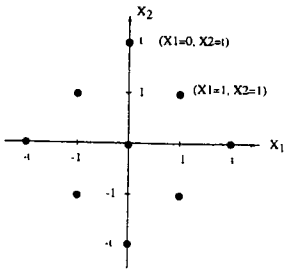


Figure 3: Graphical representation of the design matrix for two input parameters.

Process parameter	Unit	min value	central value	max value
depth (d)	μm	4	6	8
width (w)	μm	2	4	6
spacing (s)	μm	4	6	8
dose	cm^-2	1e14	2e14	3e14
time	min	100	200	300

Table 1: The central, minimum and maximum values of process parameters used for creating the full factorial design matrix.

Response	Desired	Optimum
Va [A]	1.1	1.1
Isat [A/cm^2]	650	670
Vbr [V]	1500	1600

Table 2: Desired values of the output parameters in comparison with the output parameter values of the optimum device (lifetime considered was 28μs).

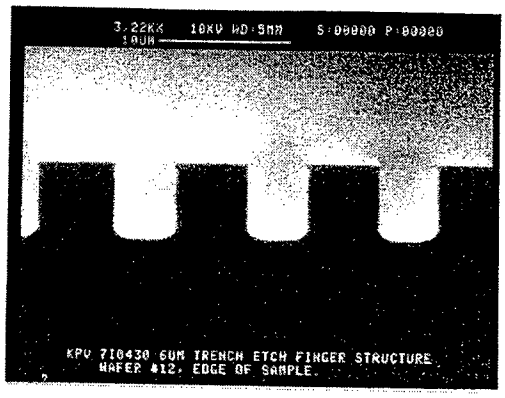


Figure 4: The hexagonal trench geometry

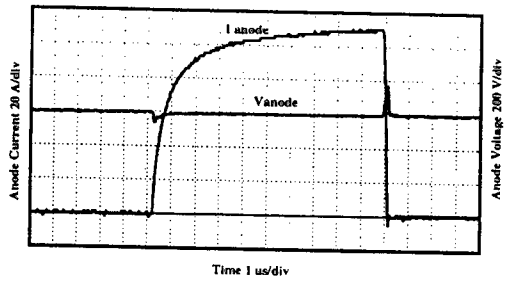


Figure 5: Short-circuit capability of 1.4kV TIGBT

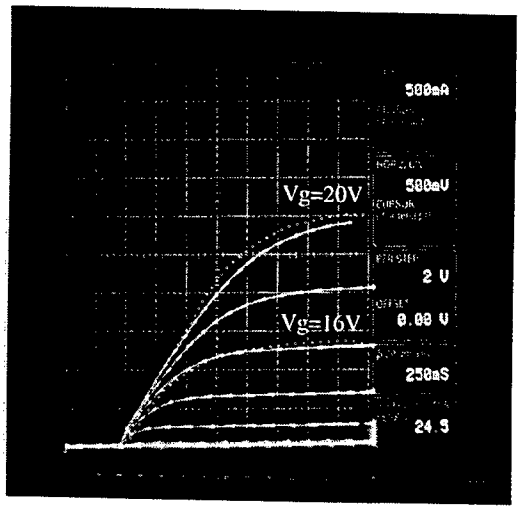


Figure 6: Comparison of the IV characteristics for the simulated and manufactured optimum prototype device with an active area of 36cm$^-4$.

10V, 3.5 GHz PHEMT Power Amplifiers

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Introduction

Base station power amplifiers operating above 2GHz are based primarily on GaAs transistor technologies such as the GaAs MESFET and InGaAs PHEMT. These technologies offer excellent performance at relatively low cost. Whereas handset PAs operate on 3-5V batteries and must be very efficient for long talk time, base station PAs operate on 10V (or higher) supplies and are designed for highly linear power and gain performance. In this paper, we discuss the device fabrication and rf performance of PHEMT PAs operating at 10V and 3.5GHz.

Device Fabrication

The FETs described here were fabricated in Motorola's CS1 fab using a standard PHEMT process flow and epitaxy. The epitaxial structure is a double delta-doped InGaAs/AlGaAs structure grown by MBE having nominal sheet charge and mobility of $2x10^{12}$ cm^{-2} and 6300 cm^2/Vs at room temperature. A cross section of the FET is shown in Fig. 1. The fabrication consists of a mesa etch (removing the n+ GaAs cap in the active region between the ohmic layers), formation of the Ni/Ge/Au ohmic contacts, dielectric passivation using SiN and CVD SiO2, gate etch and TiWN seed metal deposition followed by Au interconnect plating. The source via process involved thinning the wafer to 2-3 mil thickness, backside patterning, etching, and metallization of the via holes. A photo of the finished die is shown in Fig. 2. Nominal gate length is 0.6 um and a final passivation of 800 nm thick SiN ensures long term device integrity.

DC and RF Performance

The current-voltage characteristics of a 2.1mm FET were measured on a HP4156 semiconductor parameter analyzer. In Fig. 3, the drain current versus drain-source voltage (Id-Vds) is shown for gate voltages varying from –0.9V to 0.6V (0.3V steps). The peak current was 370mA/mm, the threshold voltage was –1.0V and the on resistance (Ron) was 2.4Ω–mm. The drain current and transconductance versus gate-source voltage (Id,Gm-Vgs are shown in Fig. 4. The peak transconductance was 270 mS/mm at Vgs=0V. Using the SPA's pulse capability to minimize heating and instability effects, the Id-Vds breakdown characteristics of a 200um width FET were measured, as shown in Fig. 5. The Vgs=-2.0V sweep reaches Vds = 30V at –0.2mA/mm gate current. This measurement illustrates the part should be quite suitable for 10V operation.

The rf performance of 2.1mm and 15.3mm FETs was measured using a Maury load pull station. Source and load pulls were performed to optimize the match to the part. The parts were biased at 10V and (nominally) 10% Idss. In Fig. 6, the output power, input return loss (IRL), transducer gain and power added efficiency (PAE) of a 2.1mm FET is plotted versus input power. At 1dB compression, the output power and gain were 14.7dB and 31.8dBm (1.5W) and the peak PAE was 65%. Similar measurements of a 15.3mm device, shown in Fig.7, resulted in a 9.8 dB gain, Pmax = 40dBm and maximum PAE of 57.7%. Finally, a swept load pull of the 15mm part is shown in Fig. 8. Here, the gain, output power and PAE contours are plotted at a linearity condition of –45dBc IM3. A linear gain of 9.7 dB and Pout of 25.4dBm with 11.4% PAE is achieved simultaneously (Γ_L).

Summary

This paper has summarized the fabrication and characteristics of PHEMT power amplifiers designed for operating at 10V and 3.5 GHz. The fabrication includes Ni/Ge/Au ohmic and refractor TiWN gate contacts as well as plated source vias to reduce source inductance. At 3.5GHz and 10V bias, transducer gains and power density of the 2.1mm device were 14.7dB and 0.72W/mm, respectively. The 15.3mm device achieved 9.8 dB gain and 10W peak Pout (1dB compression). At –45dBc IM3, the power, gain and PAE were 25.4dBm, 9.7dB, and 11.4%, respectively. These results represent state-of-the-art power amplifier performance designed for highly linear base station applications at 3.5 GHz.

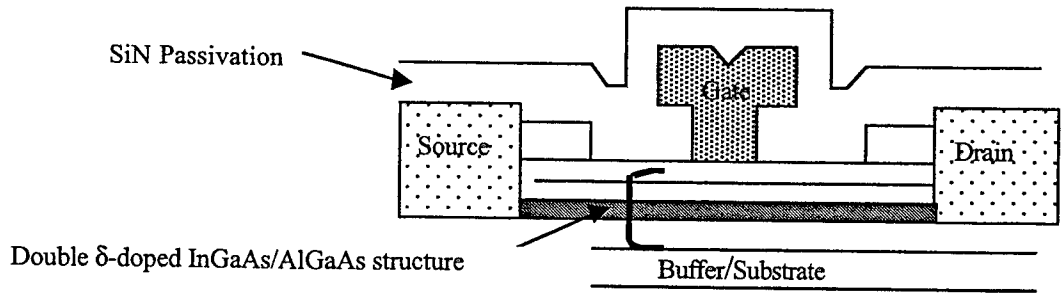


Figure 1. Cross-sectional sketch of an InGaAs/AlGaAs pseudomorphic HEMT.

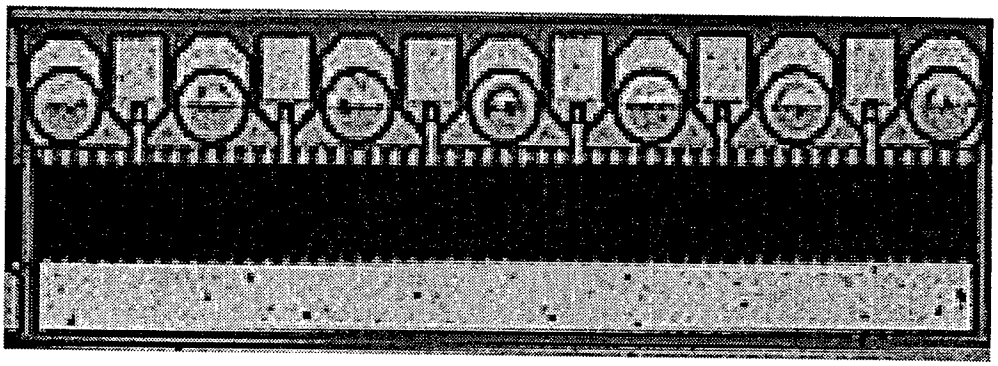


Figure 2. Photo of 15.3mm PHEMT. Gate and source pads (with circles) on top.

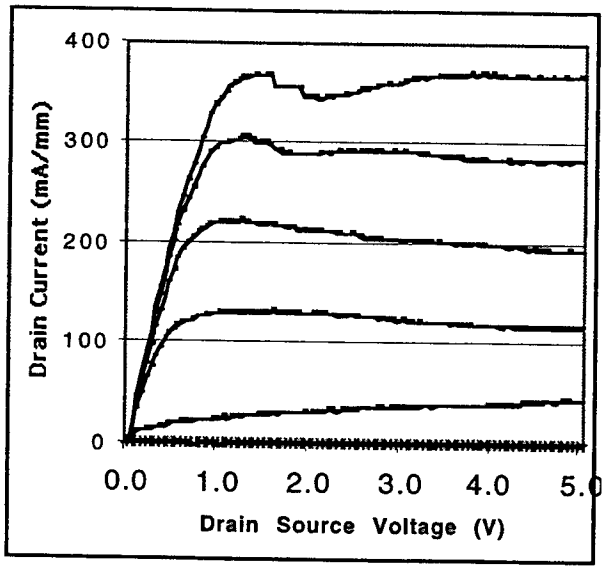


Figure 3. Drain-current vs drain-source voltage of 2.1 mm device. Gate voltage range is –0.9V< Vgs<0.6V (0.3V steps).

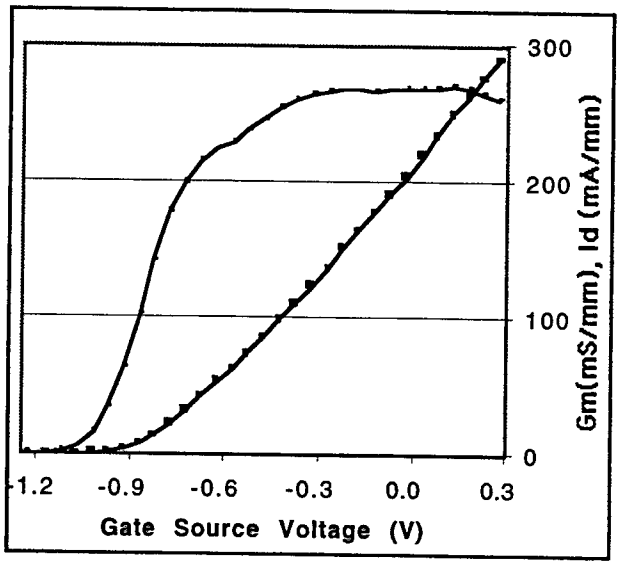


Figure 4. Transconcuctance and drain current vs gate-source voltage of a 2.1 mm device (Vds=2.5V)_.

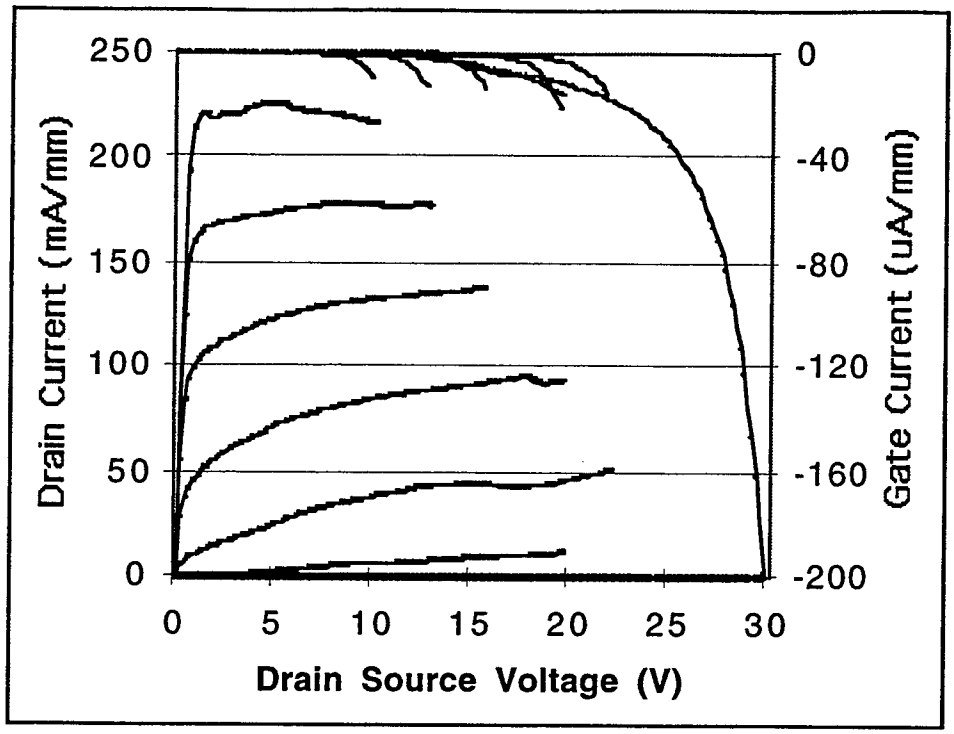


Figure 5. Three-terminal characteristics of a 200um device (Vgs = 0, -0.2, -0.4, -0.6, -0.8, -1.0, -2.0V). Corresponding gate currents are also shown. Note the Vgs=-2.0 V sweep reaches –0.2mA/mm gate current at Vds=30V.

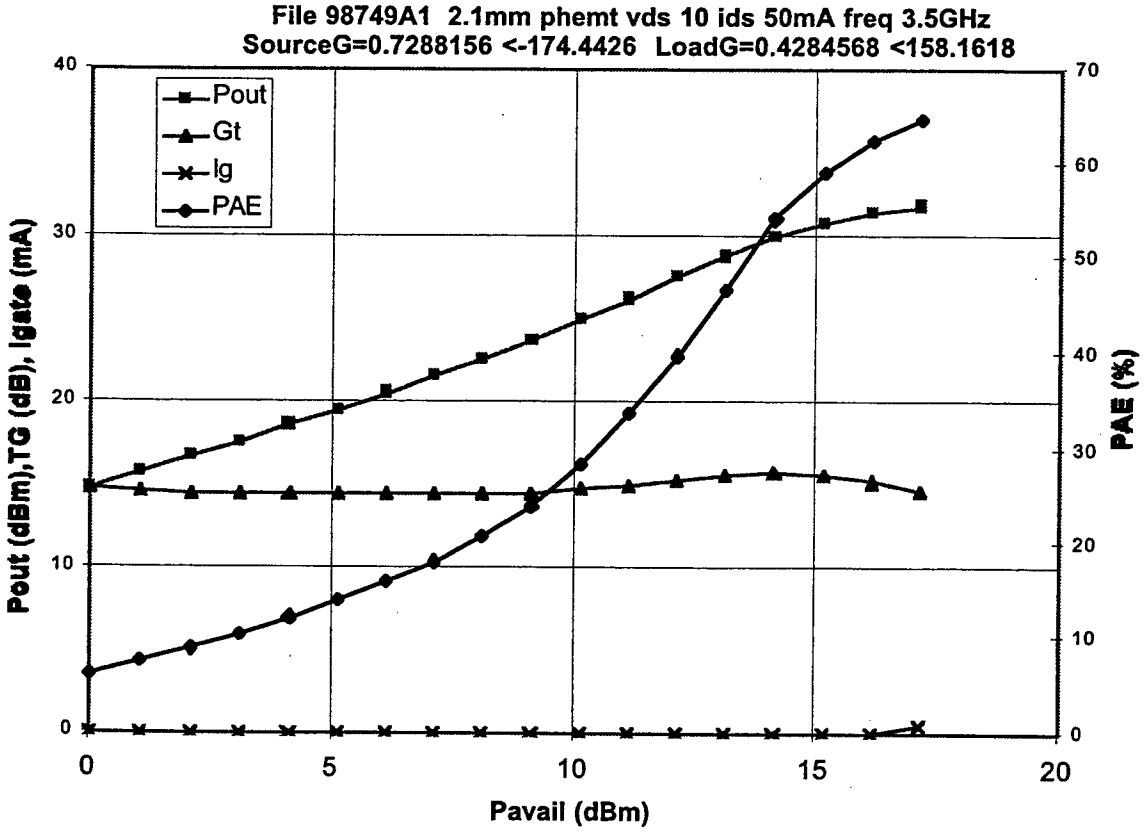


Figure 6. Output power, PAE, and gain vs. input power of 2.1 mm FET at 3.5 GHz with 10V and 10% Idss bias.

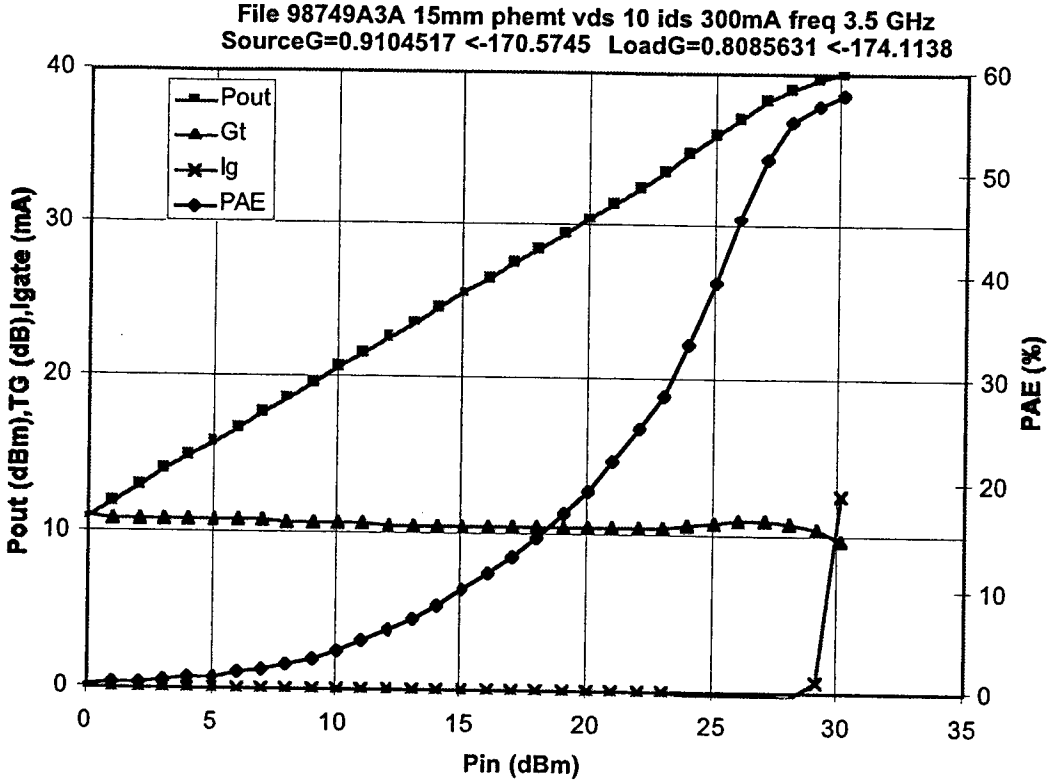


Figure 7. Output power, PAE, and gain vs. input power of 15.3 mm device (150um fingers) at 3.5 GHz with 10V and 10% Idss bias.

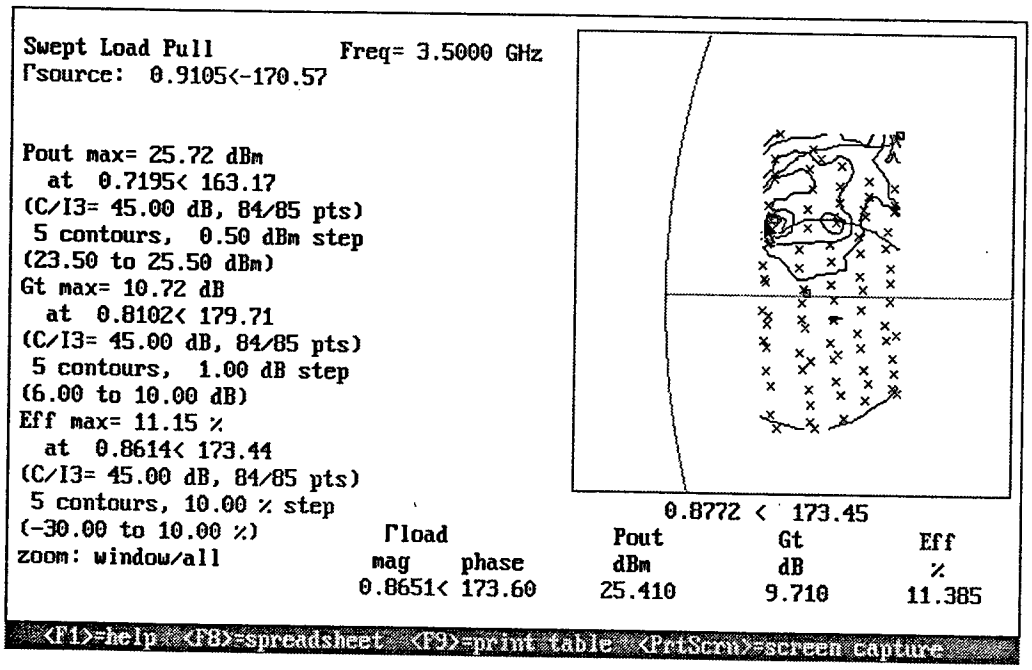


Figure 8. Swept load pull gain, power and PAE contours at –45dBc IM3 of the 15.3mm device biased at 10V and 10% Idss bias (3.5 GHz).

Novel Air-Bridged Diodes for Terahertz Frequencies

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I. Introduction

Applications such as satellite remote sensing, high resolution radar, plasma diagnostics and molecular line spectroscopy have resulted in considerable interest in the development of terahertz circuits and systems. In order for these systems to operate at terahertz frequencies the dimensions of the active devices must be reduced to a minimum and the parasitic elements associated with both the device and its embedding circuit need to be as low as possible. The effect of device dependent parasitics can be minimised mainly by controlling the device area and the epitaxial doping and layer profile; careful design of the device packaging is needed to reduce circuit parasitics.

Schottky diodes are often chosen for the applications mentioned above, as their behaviour as non-linear mixers and multipliers is well understood and they can be operated at room temperature. Good performance at millimetre wavelengths has been achieved with planar air-bridged Schottky diodes [1]. Performance is improved by reducing the parasitic capacitance of the structure by removing high permittivity GaAs from around the contact pads. Air-bridged diodes have shown good performance up to around 600 GHz [2]. For operation above this frequency it is still the case that the best performance is achieved using whisker contacted devices. Whisker-contacted devices offer the attraction of small diode area, reducing device capacitance, but have poor repeatability, poor resistance to thermal and vibrational stress and are difficult to integrate with the mixer circuitry.

The work reported here concerns the development of two air-bridged diode structures: conventional, planar, air bridged diodes and a novel, micromachined, sub-micron diameter device which combines the convenience of the planar diode with the low parasitics of a whisker contacted device.

II. Planar Air-Bridged Diodes

A processing scheme has been developed to allow fabrication of planar, air-bridged Schottky diodes for use at submillimetre wavelengths. Devices have been made on GaAs wafers with 0.1 micron thick epilayers having $n \sim 5 \times 10^{17}$ cm^{-3}. Anodes are defined by via holes etched through a 0.25 micron thick layer of SiO_2. The anodes are formed from platinum using a pulsed electroplating technique. Gold contact fingers, of thickness ~ 1.5 microns, are deposited by a combination of evaporation and sputtering and patterned by wet etching. The gold finger and contact pad are electrically isolated from the GaAs by the SiO_2. The GaAs is etched away from underneath the anode contact

finger, the resulting trench isolating the anode contact pad from the ohmic contact. The diodes are fabricated on 1 cm x 1 cm GaAs substrates, each substrate carrying ~ 700 devices. An anti-parallel pair of completed Schottky diodes is shown in Figure 1. The diodes are diced into individual chips; the thickness of the GaAs substrate is reduced to ~ 30 microns by a combination of lapping and wet etching. Diodes have been reproducibly fabricated having anode diameters of 1.5 micron, such devices typically having ideality η ~ 1.17, series resistance R_S ~ 9 Ω and junction capacitance C_0 ~ 2–3 fF. Experiments to determine the performance of these diodes as millimetre-wave mixers are now underway. We aim to further optimise the anode formation process and to reduce the anode diameter to 0.5 microns, using a combination of RIE and wet etching to form the anode vias.

III. The Cantilever Diode

Figure 2 is a schematic diagram showing the structure of the new device which we have termed a cantilever diode. It consists of an electroplated platinum whisker forming a point contact onto a Schottky barrier junction on epitaxial GaAs. The top of the electroplated pin is contacted by a metal cantilever arm. Away from the pin this cantilever is shaped to form an anode contact pad on the top surface of a SiO_2 layer sputtered onto the surface of the GaAs. The cathode is formed by an alloyed ohmic contact adjacent to the anode.

Devices have been fabricated on MBE grown epitaxial layers with semi-insulating GaAs substrates. These epitaxial layers consists of: GaAs(semi-insulating substrate)-AlGaAs undoped (1μm)-GaAs n^{++}doped 2×10^{18} (5μm) followed by the Schottky layer of GaAs n^{+}doped 2×10^{17} (0.12μm). At the start of the process a 0.2 micron thick layer of SiO_2 is sputtered onto the GaAs. A window is opened to accommodate the anode and ohmic contact. The ohmic contact is then formed by a standard evaporation and alloying process. The fabrication of the anode and cantilever contact is divided into two separate stages. The first stage forms the anode and the whisker structure and the second forms the cantilever arm.

Electron beam lithography can be used to define sub-micron holes in photoresist such that Schottky anodes may be platinum plated to form a rectifying junction. However as discussed previously the contact to these devices is often made via a whisker which provides small area contact and low parasitic capacitance. In our technique [3] the whisker is formed by electroplating platinum through a small hole, pre-formed in a thick layer of photoresist by a novel method (patent applied for). The photoresist is typically of thickness 10 - 20 micron. The platinum is electroplated using current pulses with an equal mark-to-space ratio at a current density of 10^{-10} A/μm^2.

Following the successful fabrication of the pin, the sample is baked in a conventional oven at a temperature of 90°C for 20 minutes. Using an appropriate mask a step is formed by UV exposing and developing part of the photoresist near to the whisker head as shown in Figure 2.

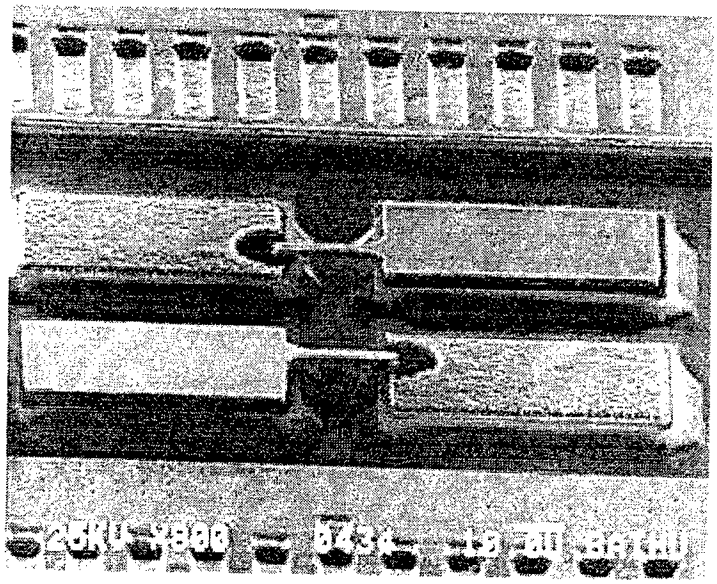


Figure 1 Anti-parallel pair of air-bridged Schottky diodes

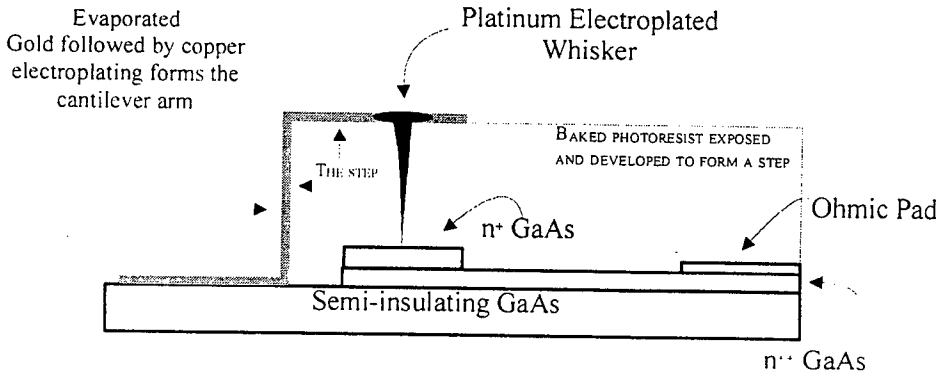


Figure 2 Schematic diagram of the cantilever diode

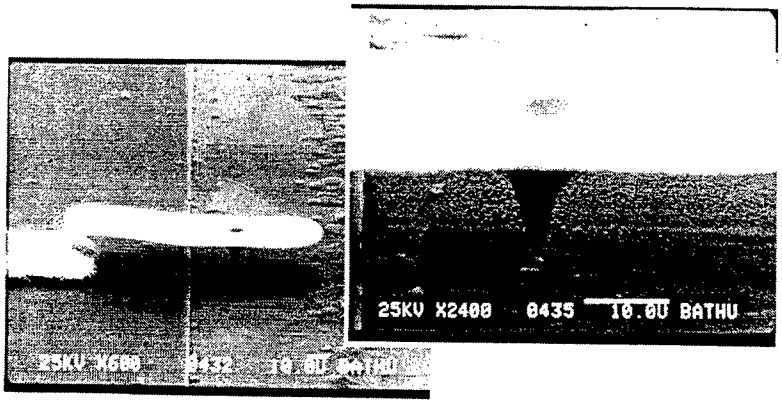


Figure 3 The Cantilever Diode

A shadow mask is then used to evaporate a gold cantilever arm seed layer, starting from the substrate over the photoresist step and to the top of the pin structure. The arm is then copper plated using an acid based copper solution for extra strength and support. The proximity of the whisker head to the edge of the step can be controlled lithograhically thereby optimising the length of the cantilever arm. The photoresist is removed leaving the cantilever arm supporting the pin structure. Figure 3 shows a device fabricated using the above procedure with a whisker pin having sub micron diameter at the base. The arm was placed on an SiO_2 insulating layer which was sputtered previously and etched away to leave an exposed open window of GaAs for the diode. The whisker was contacted directly to the layer and platinum plated, defining both the Schottky diode at the interface and also the whisker structure. Devices have been made with idealities of ~ 1.3; this will improve with better GaAs surface preparation immediately prior to anode formation. The junction capacitance of the cantilever diode has yet to be measured, but is expected to be < 1fF.

The cantilever diode has (a) a sub-micron anode, (b) contact finger entirely in air, not dielectric and (c) a large gap between finger and substrate, minimising capacitance. These are the effects the air-bridge seeks to achieve, but can never do so as effectively as the cantilever diode.

IV. Conclusions

High-quality, air-bridged Schottky diodes with 1.5 micron anode diameters can be routinely fabricated with good repeatability and yield. Work is under way to improve the anode quality still further and to reduce the anode diameter to 0.5 micron.

A novel method of electroplating a whisker pin has been used to provide a whisker contacted sub-micron Schottky diode. This was made possible by employing micromachining techniques to build up a vertical structure in a shape of the pin hence reducing the parasitic capacitance to an absolute minimum. The structure was then supported by an electroplated arm connecting the top of the whisker pin to a contact on the substrate. The authors believe that the cantilever diode potentially equals the conventional whisker contacted devices in terms of parasitics while retaining the advantages of a chip air-bridge device.

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Process Oriented Optimization of Single Quantum Well HFETs with Single in-channel Delta Doped Layer

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ABSTRACT:- We report on a HFET design approach which features the power capabilities of double delta doped devices and the low noise performance of the standard HFETs. Three different devices with single quantum well and a single δ doped layer located at three different positions inside the channel have been fabricated and tested. On wafer noise measurements have revealed that the position of the delta doped layer can be optimized to minimize the noise figure without any relevant degradation of neither the noise resistance nor the maximum transconductance. The device with the delta doped layer closer to the bottom heterointerface was found to exhibit the best performance in terms of maximum cutoff frequency, maximum oscillation frequency and minimum noise figure.

1. INTRODUCTION

Heterojunction Field Effect Transistors (HFETs) based on AlGaAs/InGaAs/GaAs or AlInAs/InGaAs/InP material system are known to have excellent microwave and millimeter wave performance, and thus they have extensively been studied [1-4]. The standard HFET with a single top delta doping layer generally gives rise to high electron mobility and low noise, while double delta doped is preferred to achieve larger carrier concentration and therefore higher drain current capabilities and larger output powers. On the other hand, double delta doped channel transistors usually exhibit lower electron mobilities.

The aim of this work is to present the first results obtained in the investigation of a new design approach which combines the advantages of double delta doped devices with those of the standard HFETs. Different single quantum well devices with single delta doping layer inside the channel have been fabricated and tested. The influence of delta doping position on the DC and RF performance of HFET has been investigated.

2. DESCRIPTION OF THE SAMPLES

The HFET layer structure (see figure 1) was grown by solid source MBE. The delta doping ($3 \cdot 10^{12}$ cm^{-2}) position was located at 40 Å (#31), 100 Å (#35) and 160 Å (#36) from the top heterointerface inside the 200 Å thickness $In_{0.15}Ga_{0.85}As$ channel. The devices were processed by combined conventional optical lithography and electron beam lithography techniques. The mesa processing was made by using wet chemical etching, and the source-drain ohmic contacts were defined by optical lithography. These contacts were based on Ni/Ge/Au/Ni/Au (150/510/820/175/1000 Å) and were annealed by RTP at 420 °C for 2.5 min. A contact resistance of 0.18-0.20 Ω-mm was obtained from TLM measurements. The gates were defined by a new trilayer resist system (PMMA/PMGI/PMMA) based on electron beam lithography [3].

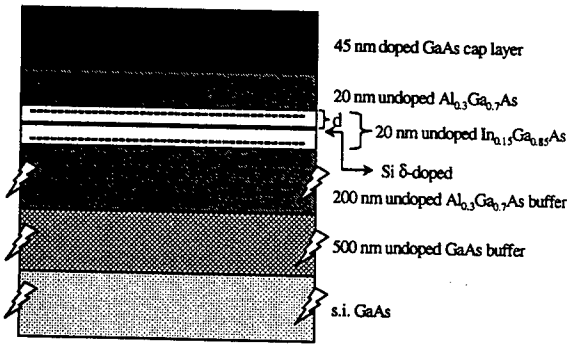


Fig. 1 Layer structure of delta doped channel HFET

The cap layer was removed by wet chemical etching with citric acid:H_2O_2:H_2O (25:1:75) solution at room temperature. The gate metals consisting of Ti/Pt/Au (200/100/3200Å) were deposited by electron beam evaporation. All gate lengths were 0.14 μm, and all the transistors were fabricated under the same process run and identical conditions.

After the removal of the cap layer, the Hall measurements gave electron channel mobilities of 1770, 1850, and 2360 $cm^2/V.s$ at room temperature for #31, #35 and #36 sample, respectively. A sheet carrier density of $2.6 \cdot 10^{12}$ cm^{-2} was obtained for all structures from Hall and PL measurements at 300K. In addition, XRD (x-ray diffraction along 002 and 004) measurements were performed to characterize different layer physical parameters such as thickness, aluminum and indium contents etc. From the X-ray rocking curves of all samples, the indium content in the channel was found to be 12.5%. The measured mobilities are therefore close to the expected ones for this indium content [1, 5].

3. RESULTS AND DISCUSSION

Figure 2 presents the I-V and transfer characteristics of 0.14 x 100 μm^2 delta doped channel devices. Smooth, and kink free I-V curves were obtained. All the transistors exhibited complete pinch off. The on-state R_{ds} was 2-3 Ω-mm, a value which may further be improved by optimizing the annealing temperature and annealing time and by increasing the doping (4-5 x 10^{18} cm^{-3}) in the cap layer. The drain-source saturation current was over 400 mA/mm at 0.7 V gate bias. The gate-drain breakdown voltage defined at a gate current of 1mA/mm was around 10 V for all devices. The two peaks in the transconductance curves indicate the coexistence of two sub-channels. At lower gate biases the electrons are first confined into the bottom channel, where they exhibit a poor mobility. The transconductance of sample #36 in this channel is slightly lower than in the other two samples due to the influence of ionized impurity scattering. However, the first peak of the transconductance have the same magnitude in samples #35 and #31, and therefore electron scattering with ionized impurities is already negligible in sample #35, with a 10 nm distance between the δ doped layer and the channel. The total distance from the gate to this channel is large (around 40 nm) and hence the transconductance is low in the first peak. As the gate bias increases the electrons start to accumulate at the top interface, where the distance from the gate to the channel is lower (around 20 nm). Therefore, the contribution of the top channel to the total transconductance in the second peak is higher than that of the bottom channel. A maximum extrinsic peak transconductance of > 350 mS/mm was obtained at 1.5 V drain bias.

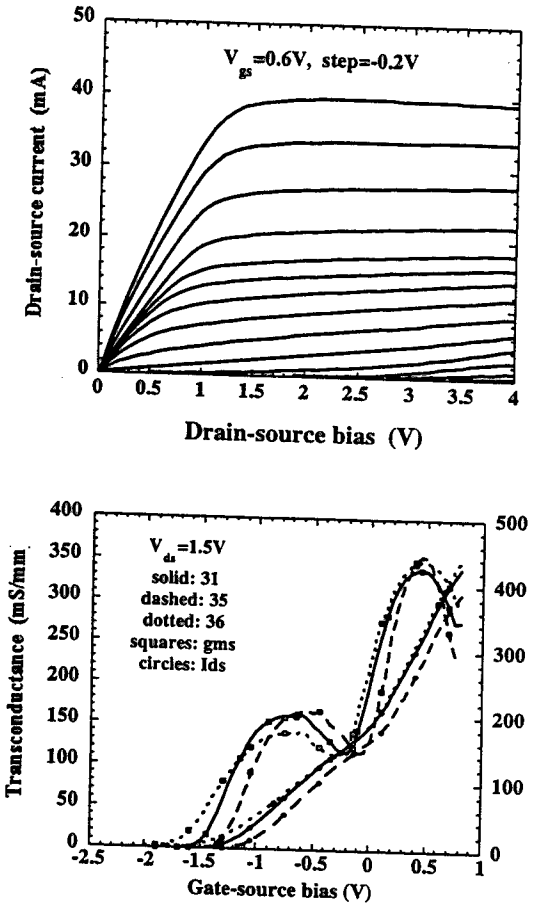


Fig. 2 I-V (top for #36) and transfer characteristics (bottom) of 0.14 x 100 μm^2 delta doped channel HFETs

Microwave noise and S parameter measurements were performed in the range 2-26 GHz by using an on wafer probe station with a network analyzer (HP8510) and an automated noise measurement system. The devices were biased at the two transconductance peaks for both S and noise parameter measurements.

The small signal equivalent circuit of the devices was extracted by using MILOU program [6], [7]. A total gate capacitance C_g (C_g=C_{gs}+C_{gd}) of 135, 130 and 100 ff was obtained for samples #31, #35 and

#36, respectively, at maximum transconductance biasing.

Figure 3 shows the cutoff frequency and the maximum oscillation frequency of all devices. The extrapolation of the current gain (h_{21}) gave a cutoff frequency f_T of 54, 60 and 75 GHz for #31, #35 and #36 sample, respectively, whereas the extrapolation of the unilateral gain (U_{21}) gave a maximum oscillation frequency f_{max} of 82, 85 and 120 GHz.

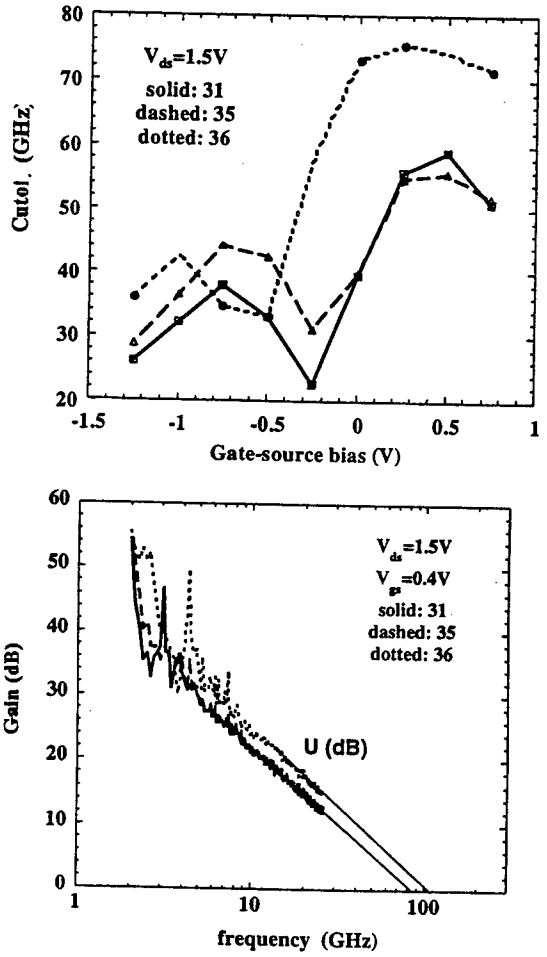


Fig. 3 Cutoff frequency (top) and maximum oscillation frequency (bottom) of the HFETs.

The measured minimum noise figure NF_{min} and normalized noise resistances of all devices are given in figure 4. Although the structures were designed for high power applications, the measured NF_{min} is still comparable to that of other standard PHEMTs/HFETs [7,8]. Sample #36 exhibited the highest f_T and f_{max} and the lowest NF_{min}. The minimum noise figure of this sample was approximately 1.0 dB at 20 GHz for the first peak and 1.5 dB for the second one, a 30% lower value than any of the other two samples. The higher electron mobility and lower total gate capacitance C_g of sample #36 played, therefore, a key role in the final noise performance.

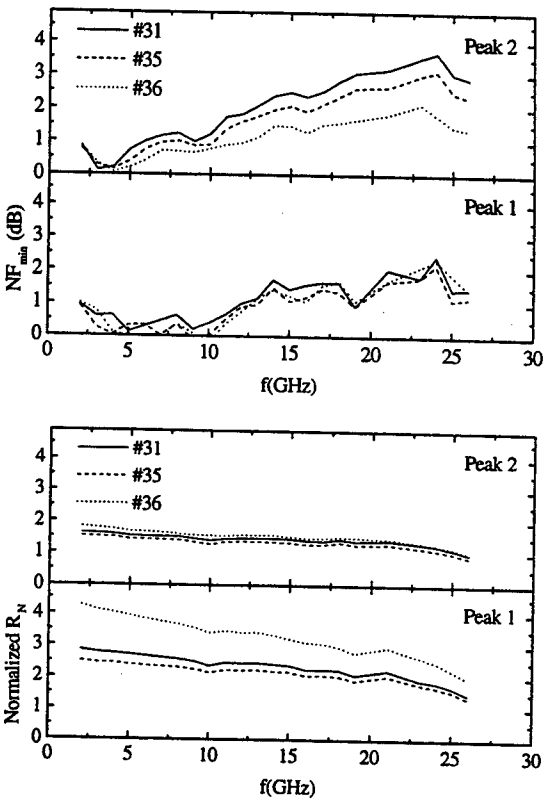


Fig. 4 Measured minimum noise figure (top) and noise resistance normalized to 50 Ohm (bottom) of the HFETs at 300K.

Despite the lower minimum noise figure of sample #36 at the second peak, the noise resistance is not noticeably higher than that of the other two samples. At the first peak, however, the differences between the noise resistance of #36 and the other two samples are more apparent, a fact which is attributed to the lower transconductance of this sample at low bias currents.

The Pospieszalski model was used to simulate the noise performance of the devices [9]. Figure 5 presents the calculated drain temperatures biased at the two transconductance peak positions. Since sample #35 exhibited a gate to source capacitance lower than that of sample #31, the minimum noise figure is less in #35 than in #31, despite its higher drain temperature. The drain temperature is approximately 2000-2400 K at the first transconductance peak, which is comparable to that of other devices biased for low noise operation [8], and 3500-4000 K at higher drain current (peak 2)

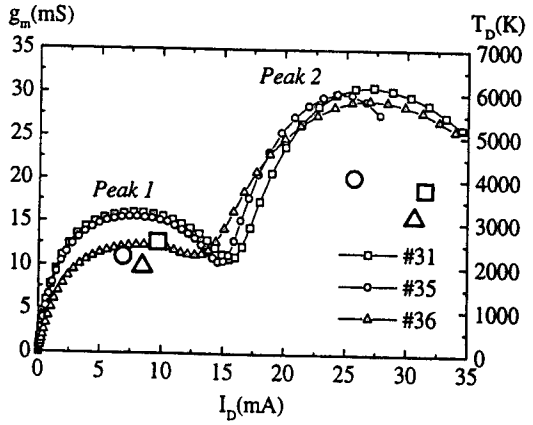


Fig. 5 Measured drain temperature at 300K of the HFETs.

4. CONCLUSIONS

The investigation of the electrical performance of single quantum well HFETs with single in-cannel doping plane has shown that the delta doping positioning inside the channel plays a relevant role in the final noise performance of the device at microwave frequencies. However, no noticeable influence of the layer location on neither the noise resistance nor the transconductance was found for optimum bias currents. The structure with the doping layer closer to the bottom heterojunction exhibited higher f_t and f_{max} and lower NF_{min} in comparison to other devices with delta plane either in the middle or closer to the top heterojunction. This new design structure is well suited for both low noise and high power applications. We expect to further improve the microwave performance by optimizing the material growth and using a thinner channel (120/150 Å).

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Accurate Parameter Extraction of Non-Quasi-Static Small-Signal Model for RF Si MOSFETs

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I. INTRODUCTION

A small-signal equivalent circuit modeling of silicon MOSFET becomes very important for designing RF/microwave ICs and characterizing processes and devices. In most papers, a simple quasi-static small-signal equivalent circuit in Fig. 1 has been widely used for the MOSFET modeling and parameter extraction [1], [2]. However, it was recently pointed out that the connection of drain-bulk junction capacitance C_{ds} to the internal source is not physically acceptable and produces severe errors in extracting model parameters at high frequencies [3]. In order to eliminate this problem, an improved model in Fig. 2 has been proposed and its physical accuracy has been verified [3]. Since these models are originated from quasi-static assumptions, the accuracy of these models are considerably limited to lower frequencies below the cutoff frequency (f_T) [4], [5]. Therefore, non-quasi-static effects existing in RC distributed bulk and channel should be incorporated to extend the frequency limit of model validity up to f_T.

Therefore, in this paper, we propose an accurate non-quasi-static small-signal model for Si MOSFET, and develop a semi-analytical parameter extraction technique combining analytical and optimization approach for enhancing the extraction accuracy.

II. A NON-QUASI-STATIC MODEL AND PARAMETER EXTRACTION

In this work, a non-quasi-static small-signal model shown in Fig. 3 for a Si MOSFET is constructed by incorporating RC distributed bulk and channel effects in Fig. 2. In this model, RC distributed channel effects are included by connecting effective channel resistances (R_{gsi} and R_{gdi}) in series with channel capacitances (C_{gsi} and C_{gdi}), respectively [4], [5]. In addition, distributed bulk effects are modeled by inserting series bulk resistance (R_{bk}) to C_{ds} [6], [7]. For the purpose of enhancing the model accuracy, overlap and fringing components (C_{gso} and C_{gdo}) are separated from channel ones.

The model parameters in conventional quasi-static models are usually determined from measured S-parameters using several direct methods [1]-[3], but these methods are not applicable to extract the non-quasi-static model due to the larger number of unknowns

as well as different circuit topology. In order to remove this drawback, a global optimization technique is traditionally be used, but this optimization may suffer uncertainties in finding unique solution due to the large number of unknowns. Therefore, in this paper, the following semi-analytical procedure combining analytical and optimization technique has been developed as an efficient way to reduce unknowns.

Since the non-quasi-static model in Fig. 3 can be approximated to be a quasi-static model in Fig. 2 in the low-frequency region well below f_T, all quasi-static parameters can be determined using a direct extraction method. Then, non-quasi-static parameters are extracted using numerical optimization while keeping all quasi-static parameters constant

S-parameters are measured on N-MOSFETs of 0.8 μm gate length and 10x10 μm gate width with grounded bulk fabricated using a standard twin-well CMOS process, and the de-embedding using "open" pad pattern was accurately carried out [2]. Then, a direct technique based on the quasi-static model is applied to extract R_d of 27 Ω and L_d of 112 pH by fitting the following equations vs. frequency [2], [3] as shown in Figs. 4 and 5.

$$\mathrm{Re}\,(Z_{22} - Z_{12}) = R_d + \frac{A_d}{\omega^2 + B} \quad (1), \qquad \frac{1}{\omega}\,\mathrm{Im}\,(Z_{22} - Z_{12}) = L_d - \frac{E_d}{\omega^2 + B} \quad (2)$$

, where B, A_d, and E_d are functions of intrinsic parameters and independent of frequency.

Because resistances and inductances in Fig. 2 can be omitted at lower frequencies, C_{ds} is extracted to be 35 fF using Y-parameter equation [1]: $C_{ds} = (1/\omega)\,\mathrm{Im}\,(Y_{22} + Y_{12})$. Then, extracted values of R_d, L_d, and C_{ds} were sequentially subtracted to obtain corrected Z-parameters from measured Z-parameters. Using corrected Z-parameters, R_g = 16 Ω, L_s = 50 pH, and L_g = 86 pH are extracted by finding constant terms through a simple curve fitting of the following equations vs. frequency [2], [3] in Figs. 4 and 5, respectively.

$$\mathrm{Re}\,(Z_{11} - Z_{12}) = R_g + \frac{A_g}{\omega^2 + B} \quad (3), \qquad \frac{1}{\omega}\,\mathrm{Im}\,(Z_{12}) = L_s - \frac{E_s}{\omega^2 + B} \quad (4)$$

$$\frac{1}{\omega}\,\mathrm{Im}\,(Z_{11} - Z_{12}) = L_g - \frac{E_g}{\omega^2 + B} - \frac{F_g}{\omega^2(\omega^2 + B)} \quad (5)$$

, where A_g, E_s, E_g, and F_g are independent of frequency. In Fig. 5, L_g is extracted from high-frequency data where $F_g/[\omega^2(\omega^2+B)]$ is neglected compared to $E_g/(\omega^2+B)$.

In order to measure R_s, the above Z-parameter technique has been performed for a test MOSFET where source and drain are interchanged. The value of R_s = 27 Ω is extracted by fitting the frequency response of Re $(Z_{22} - Z_{12})$ in the test device.

After R_s, L_s, R_g, and L_g are sequentially subtracted from the corrected Z-parameters, intrinsic parameters were extracted using Y–parameter equations [1]. Thus, it is found that C_{gs} = 130 fF, C_{gd} = 22 fF, R_{ds} = 710 Ω, g_{mo} = 13 mS, and τ = 3.6 ps. In addition, using $(1/\omega)\,\mathrm{Im}(Y_{11} + Y_{12})$, C_{gso} of 45 fF is obtained with greater accuracy from measured S-parameters at the zero gate voltage due to the absence of channel capacitance [7]. Thus, C_{gsi} is extracted by $C_{gsi} = C_{gs} - C_{gso}$ = 85 fF. Since C_{gdi} disappears in the

saturation region (V_{GS} = 2V, V_{DS} = 3V), $C_{gdo} = C_{gd}$ = 22 fF. However, when a device operates in the linear region, C_{gdi} should be determined by $C_{gdi} = C_{gd} - C_{gdo}$.

While all quasi-static model parameters are fixed to previously extracted values, non-quasi-static model parameters in Fig. 3 are optimized to fit measured S-parameters as closely as possible. From this optimization, it was obtained that R_{gsi} = 22 Ω and R_{bk} = 17 Ω. In Fig. 8, good agreement is observed between measured and modeled S-parameters up to 39.5 GHz, demonstrating the accuracy of the model and extraction method.

III. CONCLUSIONS

An accurate small-signal model accounting for non-quasi-static effects has been proposed for high-frequency circuit simulation. In order to identify model parameter values, all quasi-static parameters are directly extracted from derived formulations and non-quasi-static ones are next obtained using optimization. This new semi-analytical approach becomes an efficient way to prevent the optimization from trapping into a local minimum. The validity of this model and extraction method is verified up to 39.5 GHz.

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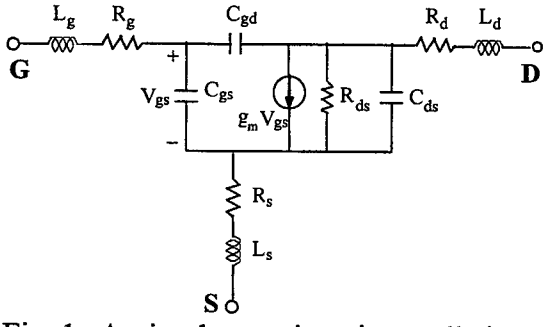


Fig. 1. A simple quasi-static small-signal equivalent circuit model for a Si MOSFET. $g_m = g_{mo} \exp(-j\omega\tau)$

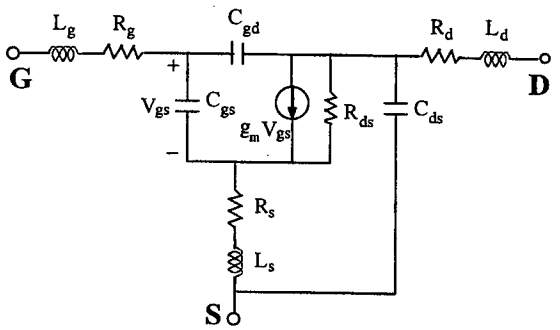


Fig. 2. A physically acceptable quasi-static small-signal equivalent circuit model for a Si MOSFET.

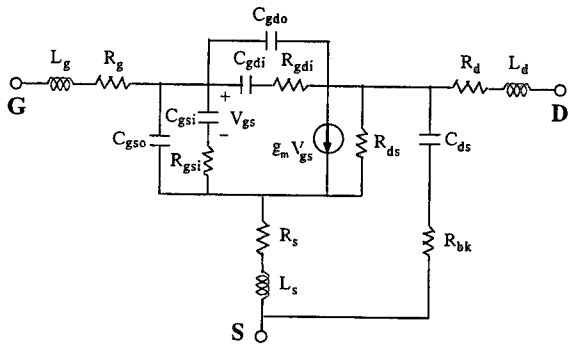
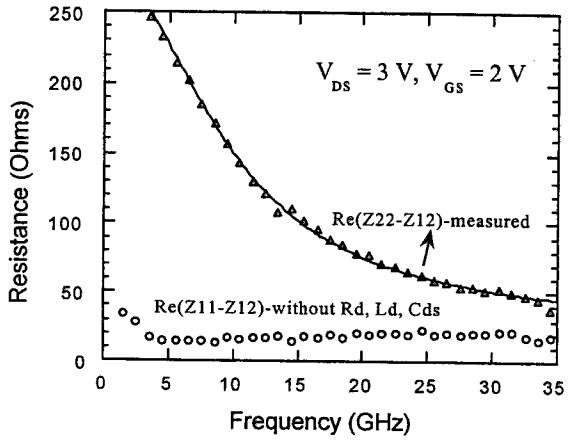
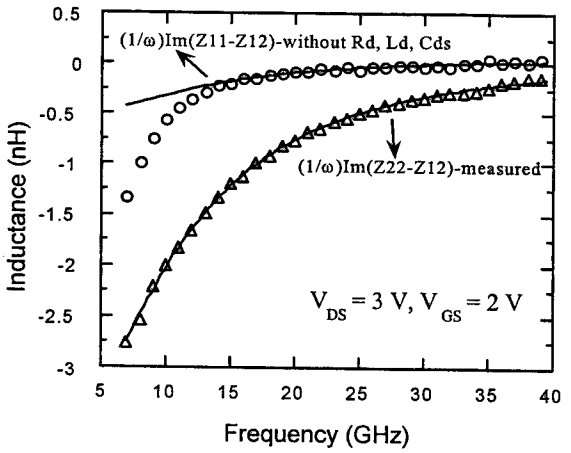


Fig. 3. A proposed non-quasi-static small-signal equivalent circuit model.



<Solid line: curve-fit>

Fig. 4. The frequency response of (1) before ("measured"), and (3) after subtracting R_d, L_d, and C_{ds}.



<Solid line: curve-fit>

Fig. 5. The frequency response of (2) before ("measured"), and (5) after subtracting R_d, L_d, and C_{ds}.

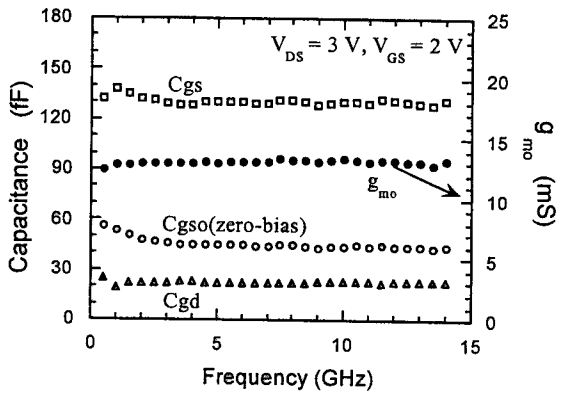


Fig. 6. The frequency response curves of C_{gs}, C_{gso}, C_{gd}, and g_{mo}.

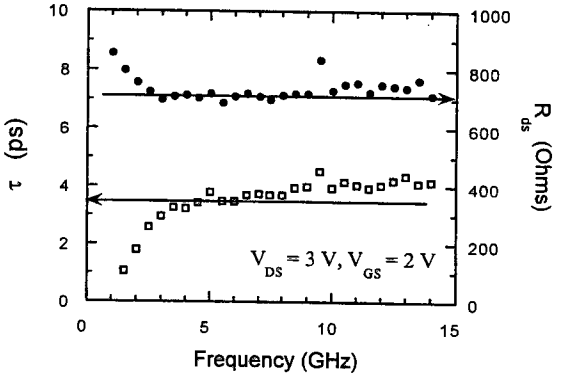


Fig. 7. The τ and R_{ds} versus frequency

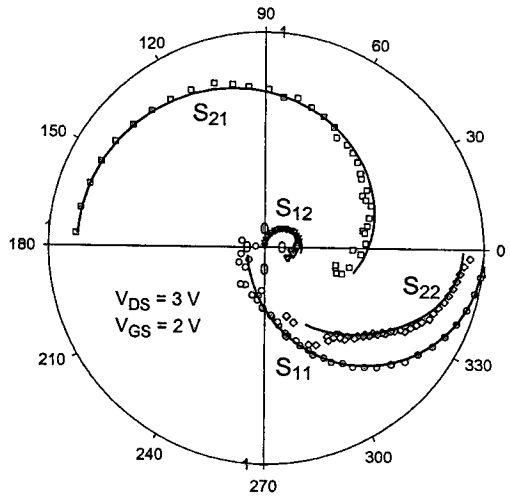


Fig. 8. The polar chart of measured (symbols) and modeled (lines) S-parameters from 0.5 to 39.5 GHz.

Studying Pd-based ohmic contacts to GaN

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I. INTRODUCTION

As GaN device technology advances, the demands on the low resistance, reproducibility, uniformity, long term stability, and high temperature operation of ohmic contacts to GaN devices will be more stringent. (Pd, Ti, Au) contacts, namely Ti/Pd/Au and Pd/Ti/Pd/Au, on p- and n-doped $In_{0.53}Ga_{0.47}As$ have demonstrated good ohmic behavior with low specific contact resistance (ρ_C=2.54×10^{-7}Ω-cm^2 for n=1×10^{19}cm^{-3} and ρ_C=1.68×10^{-6}Ω-cm^2 for p=1×10^{19} cm^{-3})[1] owing to the small band gap of $In_{0.53}Ga_{0.47}As$ (E_g=0.74eV). For GaAs with a larger band gap (E_g=1.43eV), Ti/Pd/Au and Pd/Ti/Pd/Au contacts do not show linear current-voltage (I-V) characteristics for n-doped GaAs, either as-deposited or after rapid thermal annealing (RTA)[2]. On the other hand, they achieve good ohmic behavior with low specific contact resistance on p-doped GaAs, especially Pd/Ti/Pd/Au contact which show the optimum result using a 100Å Pd interfacial layer (ρ_C=2.01×10^{-7}Ω-cm^2 for p= 4×10^{19} cm^{-3})[2]. It is our aim to extend the work on the (Pd, Ti, Au) contacts to n- or p-doped GaN (E_g=3.39eV).

Jang *et al*[3] has shown that Pt(200Å)/Ni(300Å)/Au(800Å) contact on p-GaN can achieve ρ_C=5.1×10^{-4}Ω-cm^2 for p=3×10^{17}cm^{-3}. Pd has been shown to be a good substitute for Pt in Ti/Pt/Au and Pt/Ti/Pt/Au contacts[1,2], owing to its lower melting point (1552°C for Pd; 1769°C for Pt) and higher vapor pressure (26 μmHg for Pd; 0.14 μmHg for Pt). Hence, investigations have been carried out to determine if Pd can also replace Pt in Pt/Ni/Au contact on p-GaN and yields comparable ohmic behavior.

II. EXPERIMENT AND RESULTS

The specific contact resistance, ρ_C, of the metal systems was evaluated by means of the linear transmission line model (LTLM) structure and the I-V characteristics of contacts were measured between metal pads with an interspacing of 50μm.

The surface cleaning of GaN was performed immediately before metal deposition. Various acid cleanings, including boiling aqua-regia, (1)HNO_3:(3)HCl, for 10min and soaking in (1)HCl:(1)H_2O for 1 to 10min, have been examined for their effectiveness in removing the native oxide. Although it has been reported that HCl:H_2O can reduce the oxide on GaN significantly[4], we have found that the adhesion between GaN and metal, such as Pd, Ti and Ni; is less than satisfactory. The metal layer either peels off after the liftoff process or forms bubbles after RTA, as shown in Figs.1(a), (b) and (c). We would like to highlight that these phenomena are also observed in the most common metal system, Ti/Al, for n-GaN, as seen in Fig.1(b). For the Ti/Al/Pd/Au contact shown in Fig.1(c), ohmic behavior was obtained despite metal peel off and rough surface. However, ρ_C was unstable and spanned the range of 1.02×10^{-5}~1.38×10^{-4}Ω-cm^2. In contrast, Ti/Pd/Au contact on aqua-regia treated n-GaN shows good morphology and good adhesion as-deposited and this is shown in Fig.1(d). In addition, such contact exhibits superior electrical characteristic to that treated by HCl:H_2O. As shown in Fig.2(a), as-deposited Ti(400Å)/ Pd(400Å)/Au(2000Å) contact on HCl:H_2O treated n-GaN is highly resistive and non-ohmic, while the same contact with aqua-regia treatment shows good ohmic characteristic. In subsequent discussion, GaN surface is aqua-regia treated unless otherwise stated.

(i) Ti/Pd/Au contact to n-GaN and p-GaN

The *I-V* characteristics of Ti(400Å)/Pd(400Å)/Au(2000Å) contact on n- and p-GaN treated by (1)HCl:(1)H_2O or aqua-regia, as-deposited and after RTA at various temperatures for 60s are shown in Fig.2. All RTAs were conducted in N_2 ambient. As shown in Fig.2(a), Ti(400Å)/Pd(400Å)/Au(2000Å) contact to n-GaN ($1\times10^{19}cm^{-3}$) shows ohmic behavior as-deposited and achieves $\rho_C=6.39\times10^{-4}\Omega$-$cm^2$. After RTA at 700°C for 60s, ρ_C became slightly lower of $5.65\times10^{-4}\Omega$-cm^2. However, consistent ρ_C measurement was difficult to obtain as the contact surface was very rough, as shown in Fig.1(e). The situation worsened after RTA at 800°C for 60s and the contact behaved almost like an open circuit, as shown in Fig.2(a). For Ti(400Å)/Pd(400Å)/Au(2000Å) contact to p-GaN ($9\times10^{17}cm^{-3}$), no ohmic behavior was observed, either as-deposited or after RTA, as shown in Fig.2(b), probably owing to the lower doping concentration.

(ii) Pd/Ti/Pd/Au contacts to p-GaN

Fig.3 shows the *I-V* curves of Pd(t)/Ti(400Å)/Pd(400Å)/Au(2000Å) contacts to p-GaN ($9\times10^{17}cm^{-3}$). These results are very different from those for $In_{0,53}Ga_{0.47}As$[1] and GaAs[2]. Most of the Pd(t)/Ti(400Å)/ Pd(400Å)/Au(2000Å) contacts, where t = 100Å, 200Å and 400Å, to p-GaN treated by aqua-regia show non-ohmic behavior, both as-deposited and after RTA from 500°C to 800°C. The only exception is as-deposited Pd(400Å)/Ti(400Å)/ Pd(400Å)/Au(2000Å) contact which exhibits a near linear *I-V* characteristic with $\rho_C=8.2\times10^{-4}\Omega$-$cm^2$, as shown in Fig.3(c). This is comparable to that obtained by Pd/Au on p-GaN[5] with $\rho_C=4.3\times10^{-4}\Omega$-$cm^2$.

(iii) Pd/Ni/Au contact to p-GaN

Fig.4 shows the variation in ρ_C as a function of the RTA duration for various temperatures for the new Pd(200Å)/Ni(300Å)Au(2000Å) tri-layer metallization scheme on p-GaN ($9\times10^{17}cm^{-3}$). The minimum ρ_C of $5.03\times10^{-4}\Omega$-cm^2 was obtained after RTA at 450°C for 2 min and the contact surface remained smooth and mirror like, as shown in Fig.1(f). Comparing this result with $\rho_C=5.1\times10^{-4}\Omega$-$cm^2$ obtained by the Pt/Ni/Au contact on p-GaN ($3\times10^{17}\ cm^{-3}$)[3], it can be seen that Pd/Ni/Au is a promising contact to p-GaN. Fig.5 shows the *I-V* characteristics of Pd(200Å)/ Ni(300Å)/Au(2000Å) contact on p-GaN ($9\times10^{17}cm^{-3}$) at various annealing temperatures for 60s. It is observed that 450°C is an optimum anneal temperature which yields ohmic behavior. The relatively low specific contact resistance obtained by Pd(200Å)/Ni(300Å)Au(2000Å) in the present work could possibly be related to the low barrier height occurred between the mutil-layer contacts with p-GaN after RTA.

III. SUMMARY

Pd/Ni/Au contact on aqua-regia treated p-GaN ($9\times10^{17}cm^{-3}$) has been investigated and has demonstrated good ohmic behavior contact with $\rho_C=5.03\times10^{-4}\Omega$-$cm^2$, obtained after an anneal at 450°C for 2min. As-deposited Ti/Pd/Au contact on aqua-regia treated n-GaN ($1\times10^{19}cm^{-3}$) has also shown good ohmic characteristic with $\rho_C=6.39\times10^{-4}\Omega$-$cm^2$. Unfortunately, Pd/Ti/Pd/Au contacts do not demonstrate as good ohmic behavior to p-GaN as to GaAs or $In_{0,53}Ga_{0.47}As$, probably caused by the lower doping concentration and higher band gap of GaN samples.

ACKNOWLEDGEMENTS

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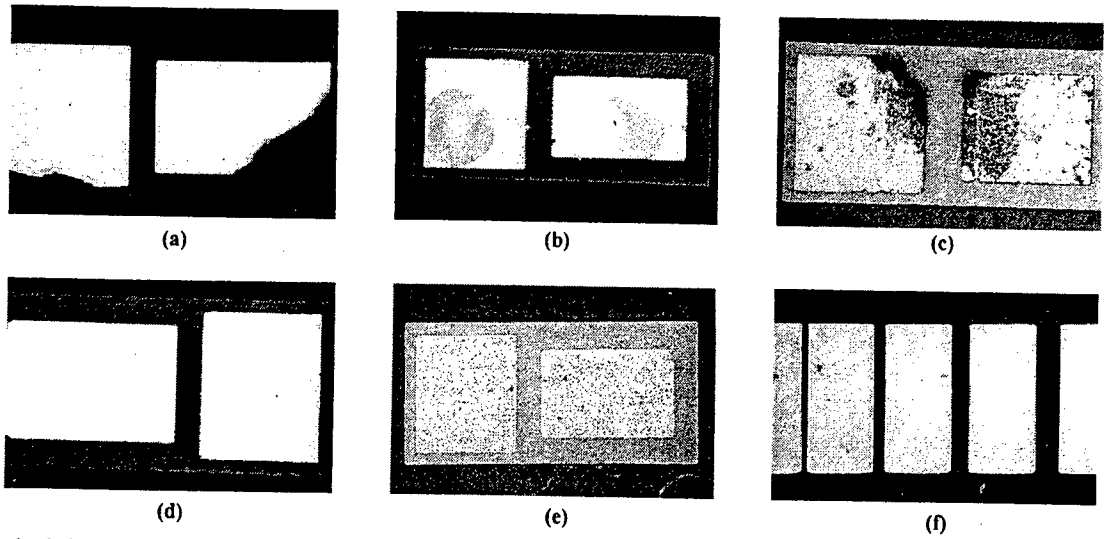


Fig.1 Micro-photographs showing the surface of as-deposited and after RTA contacts on n-GaN treated by different surface cleanings :

(a) As-deposited Ti(400Å)/Pd(400Å)/Au(2000Å) on (1)HCl:(1)H_2O treated sample. Contact peels-off and the *I-V* behavior is non-ohmic.

(b) 400°C-20s RTA Ti(350Å)/Al(2000Å) contact on (1)HCl:(1)H_2O treated sample. Bubbles are formed in contact.

(c) 600°C-4min RTA Ti(400Å)/Al(2200Å)/Pd(400Å)/Au(1000Å) contact on (1)HCl:(1)H_2O treated sample. Contact peels-off after anneal, the linear *I-V* behavior is unstable and ρ_c obtained is in the range of 1.02×10^{-5}~1.38×10^{-4} Ω-cm^2.

(d) As-deposited Ti(400Å)/Pd(400Å)/Au(2000Å) contact on aqua-regia treated sample. Contact surface is mirror like and shows good ohmic behavior with $\rho_c=6.39\times10^{-4}$Ω-cm^2.

(e) 700°C-60s RTA Ti(400Å)/Pd(400Å)/Au(2000Å) contact on aqua-regia treated sample. Contact surface becomes rough with an unstable ρ_c around 5.65×10^{-4}Ω-cm^2 after anneal.

(f) 450°C-2min RTA Pd(200Å)/Ni(300Å)/Au(2000Å) contact on aqua-regia treated sample. Contact surface is mirror like and shows good ohmic behavior with $\rho_c=5.03\times10^{-4}$Ω-cm^2.

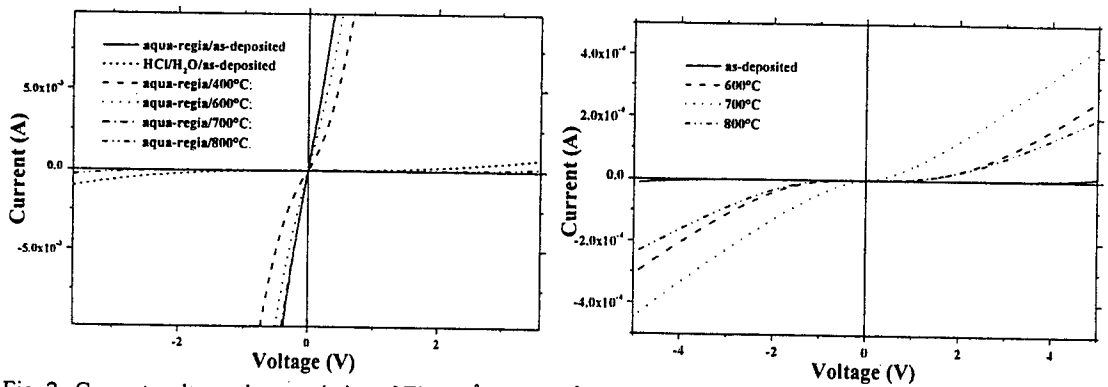
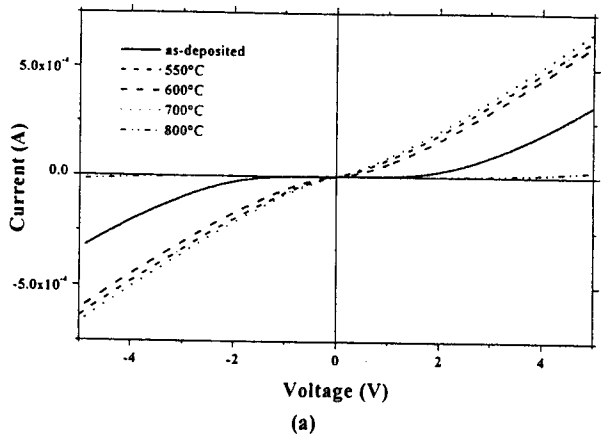
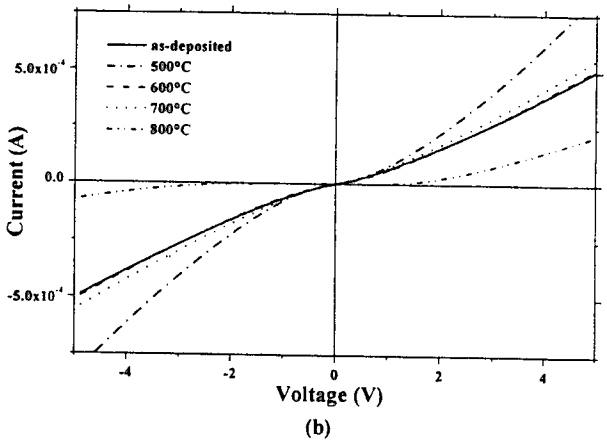


Fig. 2 Current-voltage characteristics of Ti(400Å)/Pd(400Å)Au(2000Å) contacts on n- and p-type GaN measured at various RTA temperatures for 60s under N_2 ambient: (a) n-GaN with surface treated by aqua-regia or (1)HCl:(1)H_2O and (b) p-GaN with surface treated by aqua-regia. The measured contact pads have an interspacing of 50μm.





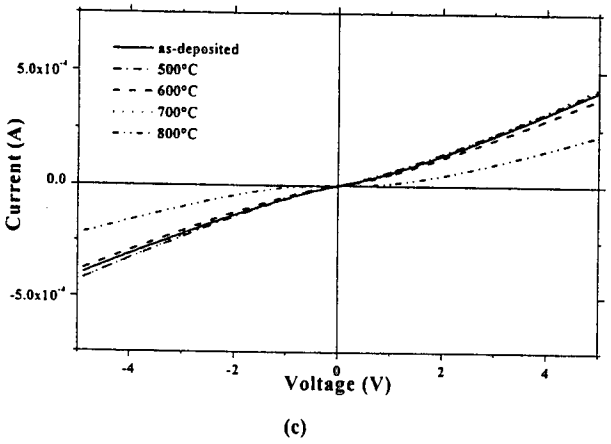
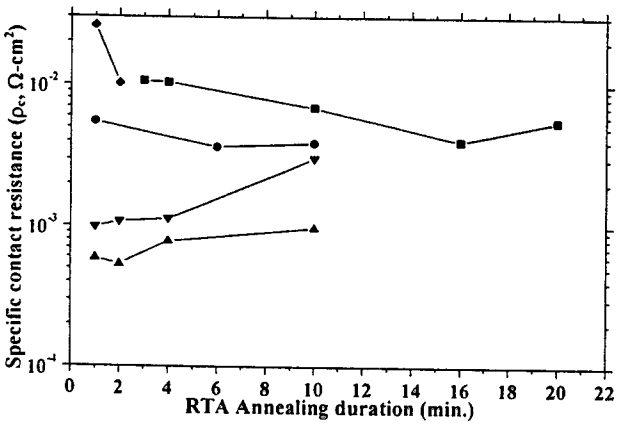


Fig.3 Current - voltage characteristics of Pd(tÅ)/ Ti(400Å)/Pd(400Å)/Au(2000Å) contacts on aqua-regia treated p-GaN samples measured at various RTA temperatures for 60s under N_2 ambient. The measured contact pads have an interspacing of 50μm.
(a) Pd(100Å)/Ti(400Å)/Pd(400Å)Au(2000Å);
(b) Pd(200Å)/Ti(400Å)/Pd(400Å)Au(2000Å);
(c) Pd(400Å)/Ti(400Å)/Pd(400Å)Au(2000Å), which has a near ohmic behavior with $\rho_c \cong 8.2\times10^{-4}\Omega\text{-cm}^2$.



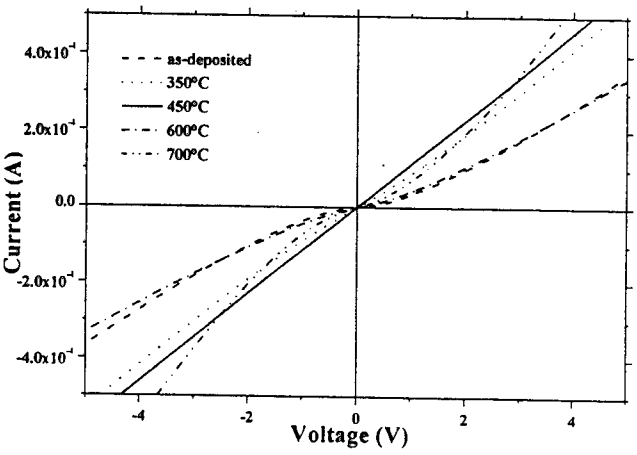


Fig.4 The variation in ρ_c of Pd(200Å)/Ni(300Å)/Au(2000Å) contact on aqua-regia treated p-GaN samples as a function of RTA duration for various temperatures :
(a) –■– 350°C
(b) –●– 400°C
(c) –▲– 450°C, minimum $\rho_c = 5.03\times10^{-4}\Omega\text{-cm}^2$ was obtained after 2 min.
(d) –▼– 500°C
(e) –◆– 600°C

Fig. 5 Current - voltage characteristics of Pd(200Å)/ Ni(300Å)/Au(2000Å) contact on aqua-regia treated p-GaN sample at various RTA temperatures for 60s under N_2 ambient. The contact pads have an interspacing of 50μm.

Monte Carlo simulation in submicron GaN n^+nn^+ diodes

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Abstract

We present a detailed Monte Carlo simulation for GaN n^+nn^+ diode at different bias voltages and lengths of the active region. The electron transport properties, such as distributions of electron energies, electron velocities, the profiles of the electron density, electric field, potential, and average electron velocity, are computed by coupling self-consistently a one-dimensional Poisson solver with ensemble Monte Carlo simulator.

Introduction

Non-equilibrium electron transport has been considered early in 1960's for possible high-frequency and high-speed applications[1,2]. Since in very small devices the local electric field may reach quite large values, the determination of the onset of hot-carrier phenomena is important for device design. In this paper, electron transport properties in wide band gap GaN sub-micron diode is reported.

Poisson's and time dependent Boltzmann equations are solved self consistently for a n^+nn^+ GaN diode. The steady state distribution of electron velocity and free-carrier density are shown. Quasi-ballistic transport is not observed clear for diodes with active layers greater than 0.2 μm. However in structures with shorter active layer the nature of quasi-ballistic transport is clearly evident.

Model and theory

We consider a sub-micron GaN n^+nn^+ diode at room temperature. An active n-layer that is doped to $2x10^{16}$ cm^{-3} is sandwiched between cathode and anode n^+-layers that are doped to $2x10^{17}$ cm^{-3}. The total length of diode is 0.55μm, and the length of active region varies from 0.05μm to 0.35μm. Acoustic phonons, polar optical phonons, intervalley, and ionized impurity scattering are included in the simulation[3]. The size of the spatial mesh and the time step used to solve the Poisson's equation are 0.005 μm and 1.5 fs, respectively[4]. Initially each mesh is taken to be electrically neutral. The number of super-particles is 30,000. Neuman boundary condition is imposed at both ends of the structure and the exiting super- particles are re-injected at the other end with a k-vector taken randomly from an equilibrium thermal distribution.

Within this model, the total number of carriers inside the device, N, is constant in time (and therefore of charge neutral). The total current j(t) through a cross-sectional area of the device, consisting of conduction and displacement currents, is given by:

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$$j(t) = j_{cont}(t) - \frac{\varepsilon_0 \varepsilon_r}{L_T} \frac{d}{dt} U_d(t)$$

where ε_0 is the vacuum permittivity, ε_r is the relative static dielectric constant of the material and $U_d(t)$ is the voltage drop between the diode terminals which is keep constant in this simulation. Therefore, the total current is only dependent on the conduction current that can be calculated following Ramo-Shockley theory [5,6] as:

$$j(t) = \frac{q'}{L_T} \sum_{i=1}^{N} v_i$$

where q' is the absolute value of the super-particle charge, L_T is the total length of the device and v_i is the instantaneous velocity along the direction of the field for the ith particle. I-V characteristics are determined by averaging j(t) up to 10ps, and by omitting the first 2ps current values to make sure that the effect of switching transient is not included.

Results and discussion

Fig.1 shows the distribution of electron velocities of a diode with an active-layer length equal to 0.25μm and biased at 3.0V. The near-ballistic nature of electron transport is shown. A weak ionized impurity scattering is the dominant scattering mechanism in the active layer. Optical phonon scattering is very weak due to the higher optical phonon energy in GaN. Due to very large electron effective mass, some electrons can only reach a velocity of $3x10^7$ cm/sec that is slightly higher than the peak velocity in GaN.

Fig.2 shows current density as a function of the applied voltage in n^+nn^+ structures for different length of the n- active region. The total length of the device is taken to be constant, and with increasing length of active layer the electric field across the n region decreases. Thus, the current corresponding to the same applied voltage is lower with wider active layer. At high bias voltages, by increasing the n region length, current density saturates and is explained as following. For a wider n region, the voltage drop tends to be localized at the two homojunctions and the local electric field in the active region near the anode is extremely high that results in electron velocity saturation that in turn leads to the saturation in current.

Fig.3, shows the effect of variation of length of the active layer on the profile of the free carrier density at U=3.0 V (for symmetry reason, the n region is centered at the center of the diode). It is noticed that by shortening the active layer of the device, the carrier density becomes closer to that of the homogeneous sample. Moreover, a travelling electron-accumulation region near the anode n^+-layer is clearly evident for an active region length equal of 0.35μm

In Fig.4, the average velocity is plotted as a function of position for varying length of active layer at U=3.0 V. With more "heavy" electron and higher phonon energy, GaN diode shows different velocity behavior as compared to similar GaAs device[7]. The dominant scattering mechanisms for GaN in our simulation are polar-optical phonon, acoustic phonon and ionized impurity scattering. Due to short transient times, electrons

can not gain enough energy to "jump over" the big valley separation of GaN, so the intervalley and equivalent phonon scattering are not important. The local electric field and the electron effective mass in the Γ valley mainly determine the electron average velocity in the GaN device. For devices with active layers greater than 0.2μm, electron move at saturation velocity through the whole structure. However, for active layers up to 0.2μm the signature of ballistic to near-ballistic transport is clearly evident.

Conclusion

One-dimensional Monte Carlo simulation coupled with a Poisson solver is used to investigate the electron transport in sub-micron GaN diode. The electron velocity overshoot is observed between the cathode and the anode, specially in short active layer diodes. The quasi-ballistic transport of the electron in the active region is also reflected in the I-V characteristic calculation of the sub-micron devices.

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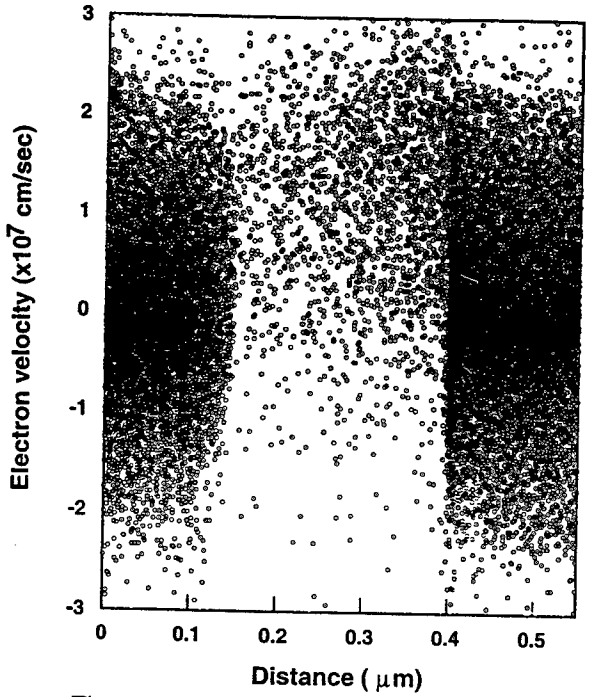


Fig.1 Distribution of electron velocity
T=300K, L=0.25μm,U=3.0 V, t=5.0ps

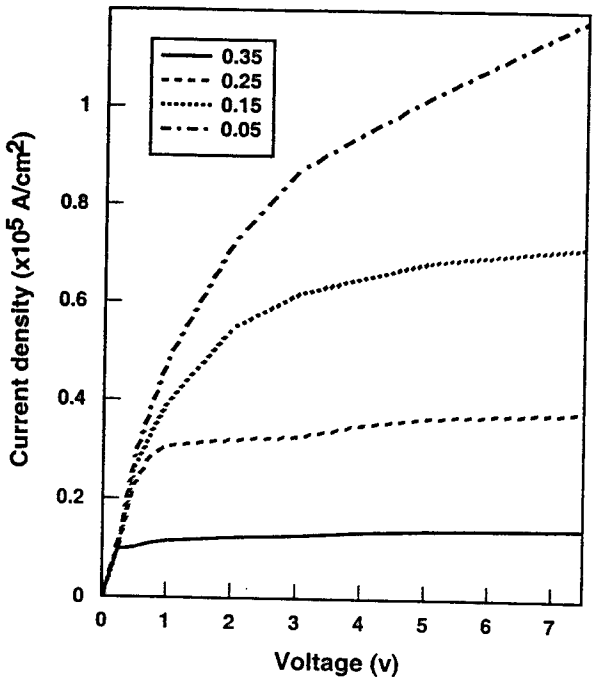


Fig.2 I-V characteristic for GaN n^+in^+ diode
T=300K

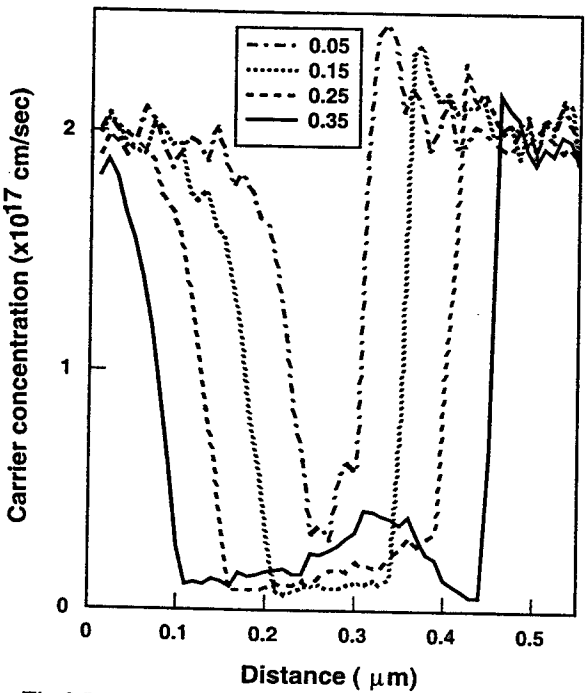


Fig.3 Free carrier concentration for GaN diode
T=300K, U=3.0 V, t=5.0ps

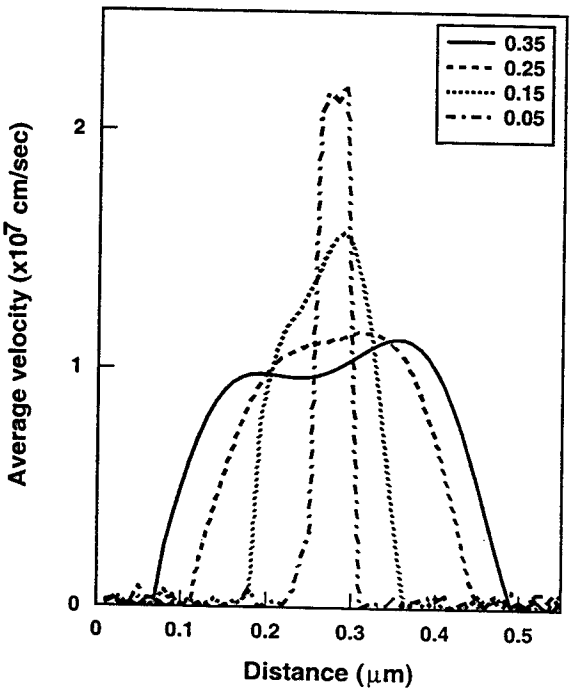


Fig.4 Average velocity for GaN diode
T=300K, U=3.0 V, t=5.0ps

Nonlocal-empirical pseudopotential calculation of 4H-SiC bandstructure for use in electron transport investigations

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I. Introduction

Due to recent progress in crystal growth[1], there has been a growing interest in the use of Silicon Carbide semiconductor devices in high frequency and temperature applications. The hexagonal 4H polytype is particularly advantagous since it has the largest bandgap of the more common polytypes. In order to understand the transport properties of this material under extreme operating conditions, the full bandstructure is needed. This will help determine properties such as the density of states, deformation potentials, electron velocities, and effective masses for use in device simulations and characterization.

We have calculated the bandstructure of 4H-SiC using a parameterized nonlocal pseudopotential that is fit to experimental band energies. This method is advantagous since it gives an accurate bandstructure with relative computational efficiency.

II. Empirical Pseudopotential Theory

The empirical pseudopotential method, developed in the 1960's[2], has long been noted for its remarkable insight into the electronic structure of crystalline solids through the use of a simple parameterized potential expanded in a small number of plane waves. The fundamental concept involved in a pseudopotential calculation is the overestimation of screening by electrons within the ion core. The pseudopotential is smoother than the real potential, giving plane wave pseudowavefunctions that are better for convergence while retaining the eigenvalues of the real potential. In our work, we were able to achieve convergence with just 500 plane waves.

The pseudopotential of a lattice site is given by the truncated expansion

$$V_p(\vec{r}) = \sum_{|\vec{G}|<|\vec{G_{max}}|,\alpha} (V_L^{\alpha}(\vec{G}) + V_{NL}^{C}(\vec{G},\vec{k}))S(\vec{G},\alpha)e^{i\vec{G}\cdot\vec{r}} \tag{1}$$

Where α represents each basis atom, and is summed over the basis. S is the structure factor and $\vec{G}$ represents the symmetry lattice vectors. The expansion is only up to $|\vec{G_{max}}|$, this leads to rapid convergence in a plane wave basis. $|\vec{G_{max}}|$ is typically no more than 4 in wave vector units[2]. The terms V_L^{α} and V_{NL}^{C} represent the local and nonlocal parts of the pseudopotential in k-space. Each basis atom contributes a local term, but only the deep $l = 1$ nonlocal well of carbon is used. This nonlocal potential depends on the conduction electron's energy and is therefore k dependent. A two parameter Heine model potential, fit to the optical spectra of carbon ions, is used for V_{NL}^{C}[3]. The local part at each lattice point can be seperated into effective symmetric and antisymmetric parts

$$\sum_{\alpha} V_L^{\alpha}(\vec{G})S(\vec{G},\alpha) = F(\vec{G})(V^S(\vec{G})cos(\vec{G}\cdot\vec{t}) + V^A(\vec{G})sin(\vec{G}\cdot\vec{t})) \tag{2}$$

The form factors V^S and V^A are treated as parameters and fit to band energies. F and $\vec{t}$ are factors which allow the form factors to be symmetrized for comparison with those of 3C-SiC.

III. Determination of Pseudopotential Parameters

There are 31 form factors in the local pseudopotential and only one reliable measured band energy, the experimental bandgap of 3.3eV. In contrast, the form factors of 3C-SiC have been obtained[4] by fitting to the bandstructure since more data is available and less form factors are needed. It has been shown that the form factors for 2H compounds may be approximated by scaling the 2H brillioun zone and interpolating the 3C values[5]. Since 4H-SiC is even more similar to 3C-SiC than 2H-SiC, we use this technique to obtain approximate form factors. The form factors were then all fit to the one experimental band energy by varying both the interpolation of the 3C-SiC form factors and the strength of the nonlocal ionic well of carbon. The final form factors were obtained by interpolating between the 3C-SiC form factors and the first approximate symmetric 4H form factor. The latter was varied up to 10% to fit the interpolation. The nonlocal well strength was varied by up to 15%, representing both the change in the well in going from a carbon atom to a 4H-SiC lattice and any error in the atomic values. A good fit was obtained by lowering the first form factor by 7.2%, deepening the local well, and raising the nonlocal well strength by 15%. The form factor interpolation used is shown in *Fig.1-2.* Plots of the band energies in the brillioun zone are shown in *Fig 3-5.*

III. Conclusion

The band structure along the brillioun zone symmetry directions in *Fig. 3* compares well with that obtained by density functional theory[7] and other approaches[6] while being much less computationally intensive. Our calculation does produce a much lower valence band energy at $k = 0$ though. Since our interpolations of the 3C-SiC form factors without using the nonlocal potential failed to raise the bandgap to more than 90% of the experimental value, the nonlocal term appears to be very important. The result could be further improved by using the nonlocal l=0 well of Si also, but the correction should be small since this well has only a fourth of the depth of the carbon nonlocal well used here. The nonlocal term is also very important in determining the curvature of the bands, especially the valence bands, and could be fit to experimental effective masses.

This method of calculating electronic structure is both accurate and fast enough to be used for the simulation of electron transport in 4H-SiC. The knowledge gained can then be used as a physical basis of the transport properties of this material.

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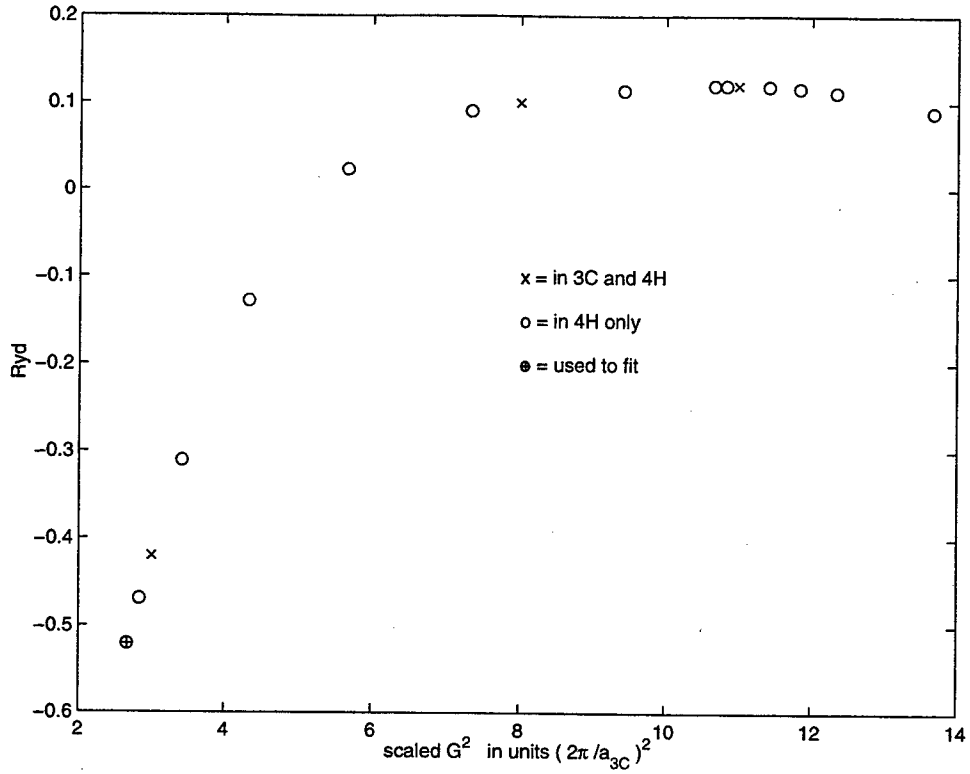


Fig. 1 Interpolated 4H-SiC symmetric form factors

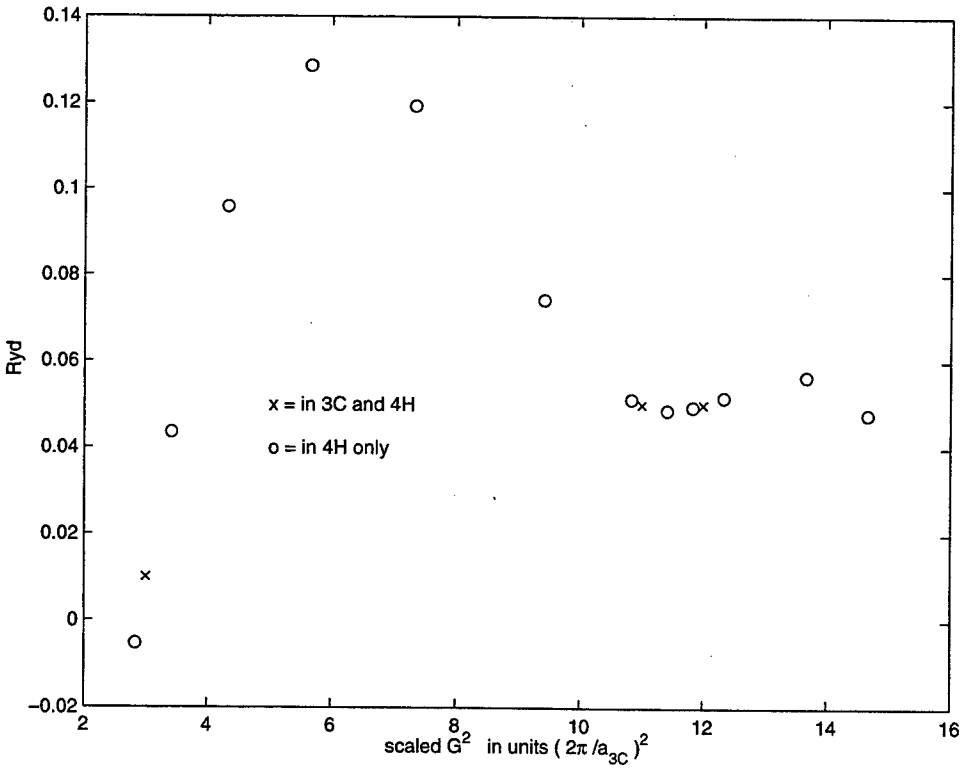


Fig. 2 Interpolated 4H-SiC antisymmetric form factors

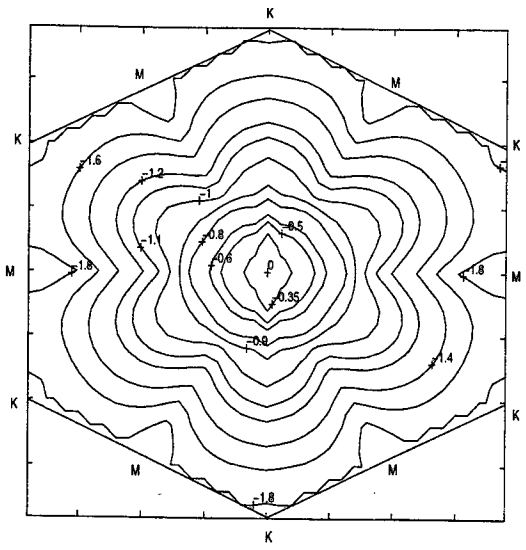


Fig. 4 (a) Contour plot of the top valence band at k_z=0.

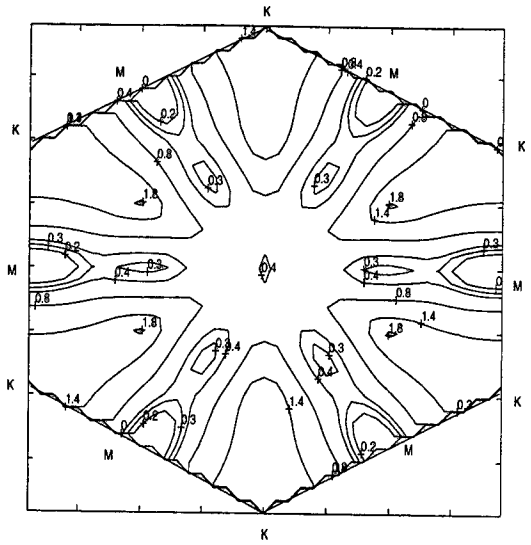


Fig. 4 (b) Contour plot of the lowest conduction band at k_z=0.

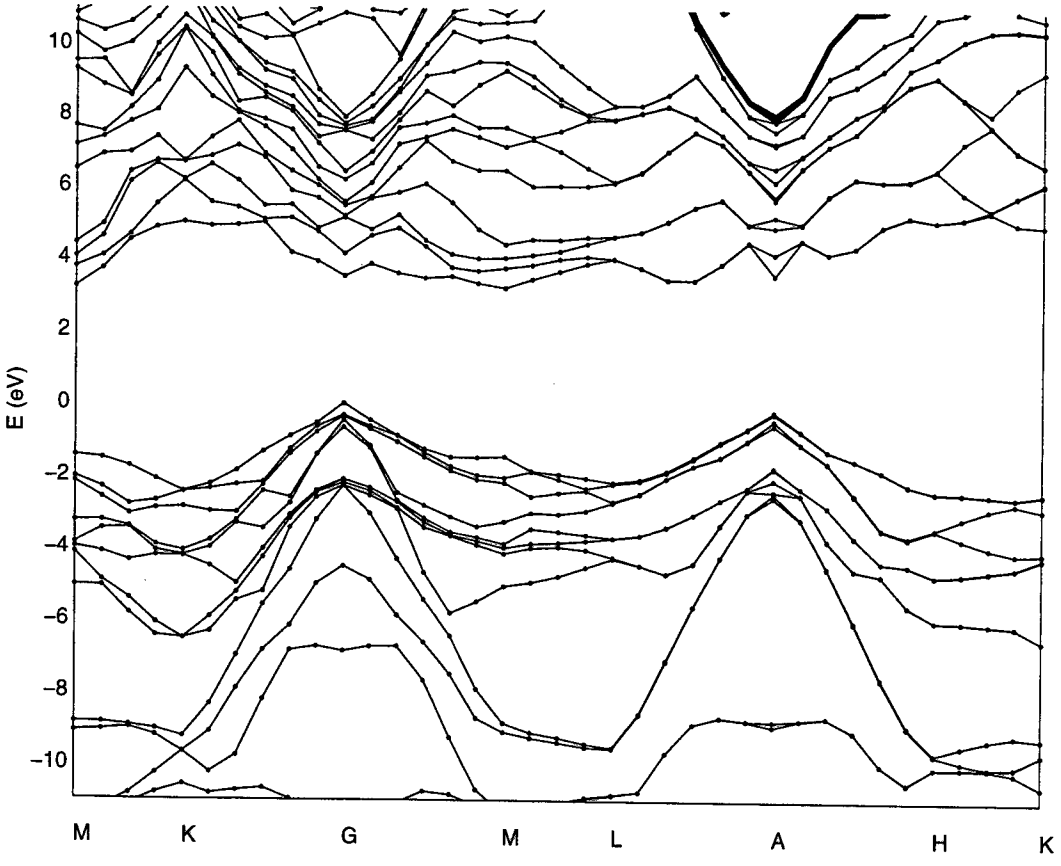


Fig. 3 4H-SiC bandstructure along symmetry lines.

ON SILICON CARBIDE HETEROSTRUCTURE BARITT DIODES

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1. Background As well known [1], the negative resistance effects can be increased in BARITT structures if the phase lag of the density modulation component of the current which is in anti phase with the local electric field is increased. In some cases this can be achieved by the use of a low-mobility material in order to reduce space charge carriers velocities in the source region. Then, after the transit through the central and drain regions, phase lag and generated power are increased. On the other hand, large attention is given to silicon carbide SiC as a wide-bandgap semiconductor, as such material well is operated well at higher temperature, voltage, power, and frequency [2-8].

Rather small lattice *SiC* mismatches with *AlN, GaN, Si*, as well as the abundance of poly-types in *SiC*, make *SiC* a material with an immense potential for manufacture of different hetero-junction electronic devices using differing bandgaps, charge carrier mobility, etc. Additionally, such heterojunction devices as heterojunction field-effect transistor (HFET) and heterojunction bipolar transistor (HBT) have been proposed and fabricated [2]. Examples included *3C-SiC/Si, 6H-SiC/3C-SiC,* and *GaN/6H-SiC* HBT [2,6]. Possibilities of the use of *SiC* in microwave technology are especially attractive, in particular for the manufacture of IMPATT and BARITT diodes [8].

The aim of present paper is to show how to use different heterostructures *6H-SiC/Si, 6H-SiC/3C-SiC, 3C-SiC/Si* for the manufacture of BARITT diodes using its difference in mobility and velocity. This difference can lead to higher efficiency and power performance and which could be possible to their fabrication with present-day technology. The use of *SiC* is promising owing to the fact that the mobility values of charge carriers in individual *SiC* polytypes are rather small. It should lead to an increased phase delay between the current and alternating electric field in the HF region and, hence, to an increase in the absolute magnitude of the negative dynamic resistance (NDR).

2.Small signal characteristics We have examined physical processes in p^+n *(6H-SiC)*/*n*-p^+ *(Si)*, p^+n *(6H-SiC)*/*n* p^+ *(3C-SiC)* BARITT devices which are consists of uniform doped two *n*-*(6H-SiC/Si)* or *n*-*(6H-SiC/3C-SiC)* heterojunctions drift regions L_1 and L_2 (Fig.1). Under the assumptions are:

a) Negligible space charge effects of the mobile carriers;

b) Expressions for the reach-through voltage are obtained by the solving the Poisson's equation in two distinct regions $0 \le X \le L_1$, $L_1 \le X \le L_2$, with the continuity conditions of the fields and potentials at the boundaries $x=0$, $x=L_1$, $x=L_2$. Then, using the method for the calculation of the impedance characteristics of BARITT diodes described in Refs. [1], for the small signal injection approximation we obtain an expression for the real part of the impedance corresponding to the barrier limited regime.

Numerical calculations were performed for the $p^+ n$ *6H-SiC*/n-p^+*Si* heterostructures with the following parameters: $N_{d1}=N_d=1.25\cdot10^{15}$ cm^{-3}, device area $S=10^{-4}$ cm^2,

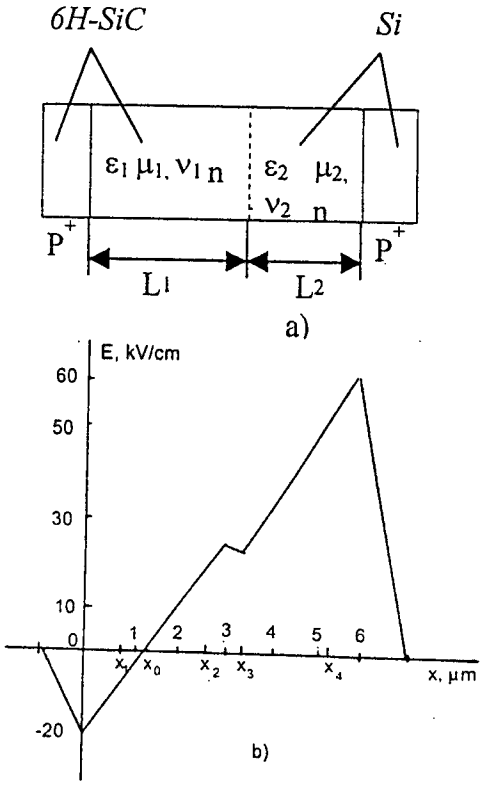


Fig.1 Schematic diagrams of p^+-n-n-p^+ heterojunction (a) BARITT and electric field distribution (b).

I_0=10A/cm^2, 50A/cm^2, 100A/cm^2 $L_1=L_2$=3μm, dielectric constants ε_1=9.7, ε_2=11.8.

Values for the hole mobilities μ_1=100cm^2/Vs, μ_2=470cm^2/Vs for the *6H-SiC* and *Si* are chosen respectively [1,8]. Due to low mobility μ_1 in the low field region, an increase in the phase delay between the current and alternating field and hence leads to increase in the absolute magnitude of NDR. This effect is illustrated in Fig.2 where analogous calculations of the resistance R for the Si homostructures [1, 9, 11] and *Ga$_x$Al$_{1-x}$As-Ga As* heterostructures [13] are shown for the comparison. As seen from Fig. 2, NDR in heterostructures in one or more orders of the magnitude higher, in absolute value, than in the *Si* or *Ga$_x$Al$_{1-x}$As/GaAs* cases, all other factors being equal. The analysis of the expression of active part of impedance and numerical calculations show that the maximum negative values of R can be realize if $\theta=\theta_3=\pi$. It means that for optimum transit angle ($\theta_0=\pi$) and frequency of the operation, there are some optimum values of NDR for which the device will generate maximum power. For example if we estimate the efficiency [see, for example, Refs. [9, 10], we obtain for examined heterostructures the following expression:

$$\eta \approx \frac{\cos^2(\pi\beta)}{\pi},$$

where β=0.96, and $\eta = 31\%$.

Note, that for p^+-n-p^+ *Si* BARITT diodes $\eta = 15.9\%$ [9,11,12], and for the $Ga_XAl_{1-X}As$-*GaAs* heterostructure diodes [13] under large–signal conditions $\eta = 18\%$.

Note also that the operating frequency is determined usually by the time of flight of charge carriers across the drift region. In first order approximation $T \sim L/v$. As $v_{SSiC} > v_{SSi}$, and $E_{mSi} < E_{mSiC}$, we can reduce the drift region length L_1 and therefore increase the operating frequency ($f \sim 1/T$).

As follows from Refs. [9,10] the optimum bias current density for homojunction BARITT's is equal to

$$I_0 = 3\varepsilon f E_m/2,$$

where E_m is the avalanche breakdown field, f is the operating frequency. In the other hand the width of the drift region is determined by the required operating frequency from the condition that the transit angle be equal to its optimum value.

For the *6H-SiC/Si*, $\theta_0 = \pi$, $\theta_{30} = \pi$. Let the carrier velocity in L_1 region is equal to $v_1 \sim 5 \cdot 10^6$ cm/s and $v_2 = v_{Ssi} = 10^7$ cm/s in the L_2 region. Then one obtains $f_0 \approx 8.3$GHz for the widths of the drift regions L_1, L_2 and for the optimum frequency f_0, $L_1 \approx 0.5L_2$, $L_1 \sim 3\mu$m, $L_2 \sim 6\mu$m.

It is known that for the BARITTs an average field of between E_m and $E_m/2$ in the drift region an punch through gives the highest microwave power. If the admissible field variation is somewhat arbitrarily limited to 30 percent of the average field in the drift region, the limits on the width and doping concentration (N_d) of the drift region are

$$L_1 N_{d1} < \frac{\varepsilon_1}{q} 0.3 \cdot \frac{3}{4} E_{mSiC} \qquad L_2 N_{d2} < \frac{\varepsilon_2}{q} 0.3 \cdot \frac{3}{4} E_{mSi}.$$

For the N_{d1} and N_{d2} we obtain $N_{d1} < 24/L_1 \cdot 10^{11}$ (cm^{-2}), $N_{d2} < 30/L_2 \cdot 10^{10}$ (cm^{-2}).

For larger output, at high frequencies, the length of first drift zone can be in two times lower than that of the second drift zone. As the $E_{mSiC} > E_{mSi}$ for the optimum transit angle $\theta = \theta_3 = \pi$, the corresponding optimum frequency is given by the following expression:

$$f_0 = v_1 v_2/(L_1 v_2 + L_2 v_1).$$

If the $L_1 = L_2/2$, $v_1 = v_2/2$, $f_0 = v_2/2L_2$, and $L_2 = 3\mu$m, $v_1 \sim 10^7$ cm/s, $f_0 = 33$GHz.

4. Conclusion Possibilities and advantages of the use of silicon carbide/silicon and silicon carbide heterojunctions for the manufacture of BARITT diodes have been discussed. It is shown that due to the low mobility's of holes in *6H-SiC* and different ratios of the mobility's and dielectric permitivity in two drift zones around the heterojunction, NDR in absolute value is increased one and more order in the magnitude and a conversion efficiency as high as 30 percent is possible to obtain. So, the performance of the double–velocity heterojunction BARITT's are better in comparison with the single velocity homojunction BARITT's, all other factors being equal.

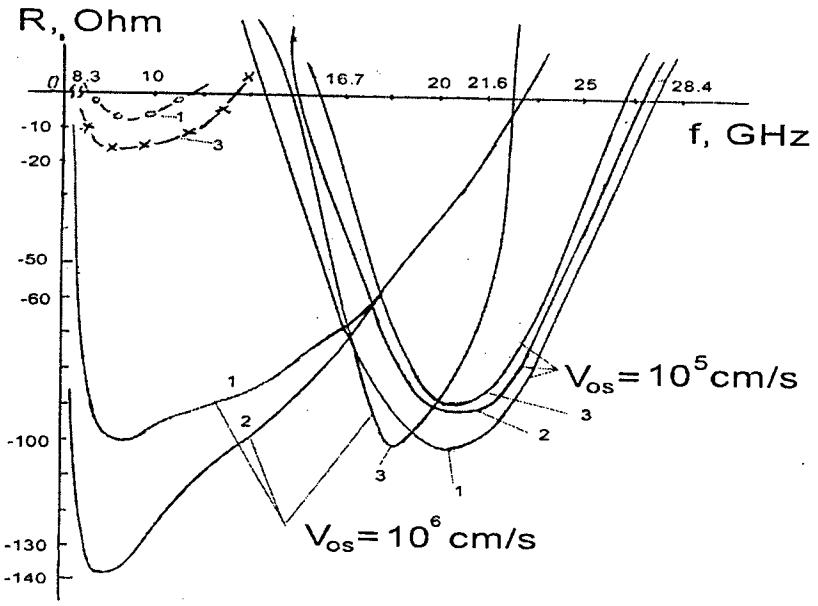


Fig. 2. Variation of small-signal negative resistance with frequency for *Si* p^+-*n*-p^+ homojunction (o-o-o) [1,9,11], $Ga_xAl_{1-x}As/GaAs$ heterojunction (x-x-x) [13] and p^+-*n*-*n*-p^+ *6H-SiC/3C-SiC* heterojunction (—, L_1=1.5μm, L_2=3μm) BARITT diodes. 1 - J_0=10A/cm^2, 2 - 50A/cm^2, 3 - 100 A/cm^2.

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Flicker Noise Characterization of Plasma-Induced Damage to Gallium Nitride

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GaN and its alloys have gained popularity as materials for optoelectronic, high power and high temperature device fabrication in recent years. However low frequency noise originating from the materials places limitations on the performance of the devices. Low noise levels are particularly pertinent in devices used for microwave applications. Despite significant advancements in GaN technology in the past few years, the level of structural perfection, as well as methods of surface processing and fabrication of contacts are in need of substantial improvement. Low levels of structural quality leads to high levels of low-frequency noise, as a result of high dislocation densities.

Plasma etching has become an important process in device fabrication. In fact it is the most satisfactory way of etching for GaN, with good etch rates of 0.2μm/min and good surface morphology. Nevertheless it involves the bombardment of energetic ions onto the semiconductor surface, making damage to the surface inevitable, giving rise to changes in electrical characteristics and other side effects.

In this presentation we report low-frequency (LF) noise measurements of n-doped GaN samples that have undergone Inductively-Coupled Plasma (ICP) etching treatments. Si-doped GaN layers ($n \approx 1 \times 10^{17}$ cm^{-3}) grown on sapphire substrates by metal organic chemical vapour deposition (MOCVD) were used for the experiments. Hallbar structures were patterned onto the samples by photolithography and ICP etching. Ti/Al ohmic contacts were deposited by electron-beam evaporation on the surface of the contact pads. Damage to the surface was induced by ICP etching in an BCl_3 and Cl_2 ambience at ICP power of 400W for 30s. Current noise spectral density was measured using the standard 4-point probe method with an HP35670A dynamic signal analyser after amplification with an SR570 low-noise current amplifier.

The spectral density of the current noise S_I/I^2 was measured as a function of biasing current I. Invariance of S_I/I^2 with respect to I [1] at currents beyond 1mA indicates that the contact noise does not contribute to the total noise significantly at these current levels. Subsequent noise measurements were performed at 2mA so that the contribution of contact noise could be ignored. To account for changes to the noise performance as a result of plasma damage, the McWhorter type of model for 1/f noise will be most appropriate. In brief, the McWhorter or number fluctuation theory assumes that the fundamental origin of 1/f noise is the trapping and detrapping of charge carriers by defect centres. In our case these defects are located in the vicinity of the GaN - native

oxide interface. As the traps are distributed in energy and distance from the surface, the capture-release time (lifetime) are distributed over a wide interval. The summation of the independent Lorentzian spectrum of each individual trap centre leads to a 1/f type of spectrum. An increase in interface or oxide trap density would be accompanied by a higher LF noise.
Plasma damage may exist as recombination centres, vacancy complexes, dislocations and implanted ions[2]. Our SEM microphotographs in Figure 2 reveal that the plasma etching treatment did leave behind dislocations, removed by subsequent rapid thermal annealing treatment (RTP). However the density of dislocations is extremely low. It would be logical to assume that any form of damage would lead to a higher LF noise level. P. Gottwald et al[3] investigated the effect of reactive ion etching (RIE) to indium phosphide (InP) and they found that 1/f noise component was indeed enhanced as a result of plasma-induced damage.

The spectra in figure 1 illustrate the effect of plasma damage and subsequent annealing treatment on the noise levels of our GaN samples. A half-an-order of magnitude reduction in LF noise was observed in the sample that received ICP etching treatment. This is different from what we predicted. To confirm our results the other plasma-damaged sample was subjected to rapid thermal annealing (RTP) at 900°C for 3 min in order to repair the damage. The measured noise was of a level identical to the untreated sample, indicating the return of crystalline order to the semiconductor surface, also revealed through the SEM microphotograph.

The native oxide plays a role of passivating the surface states of the material. Native oxide on GaN has been determined to be predominantly in the form of Ga_2O_3[4], which could attach to dangling bonds at the surface of GaN. The ICP etch leaves the surface roughened and the surface area is enhanced. Subsequently a new layer of native oxide is formed, which covers a larger surface area. A greater proportion of dangling bonds are passivated, giving rise to a substantial reduction in the density of traps near the interface.

Comparing our results with that of InP, we believe there are two possible explanations. Firstly ICP etching is a much milder etching technique than RIE etching. Also it has well known that GaN is highly damage resistant. The extent of the damage goes only as far as creating microscopic undulations on the surface of the material to expose more dangling bonds. Hence, instead of enhancing the noise level, the opposite is achieved as there is a nett reduction in density of interface traps.

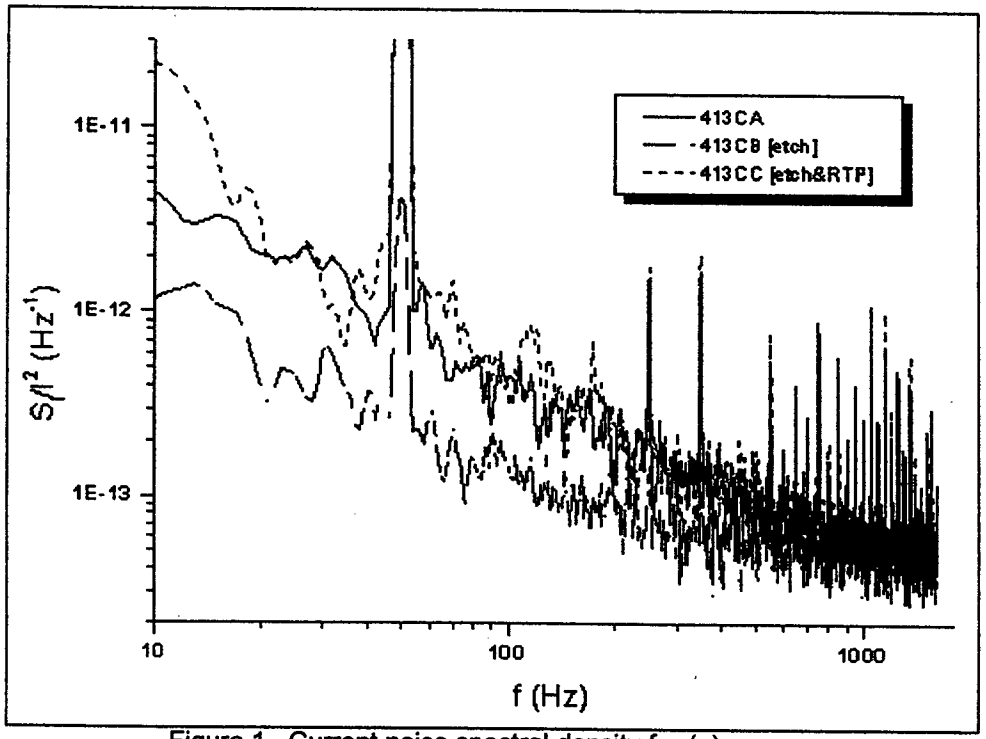


Figure 1. Current noise spectral density for (a)as-grown (b)etched and, (c)etched & RTP GaN samples

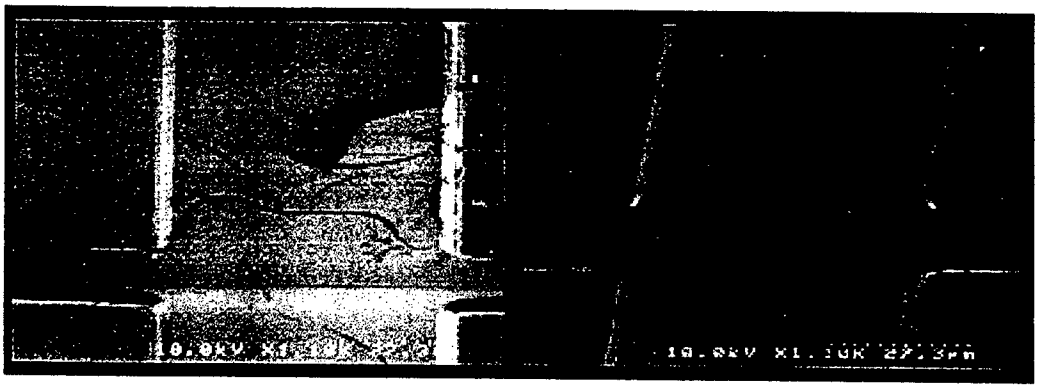


Figure 2. SEM microphotograph of (a)etched and (b)etched & RTP GaN sample.

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Terahertz Schottky Diode Dynamics near the Polar-Optical-Phonon Frequency

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The dynamical behavior of GaAs-based Schottky-diode interfaces near the polar-optical-phonon (POP) resonance frequency is addressed. The manifestation of a novel *terahertz-regime* coupling mechanism between the temporal evolution of the diode barrier and POPs is revealed. Specifically, POPs are shown to perturb the spatial dependence of the displacement field within the depletion-region and strongly enhance the nonlinearity associated with diode current. This resonance coupling emerges in the unscreened barrier region and leads to dramatic nonlinear effects on both the resistive (i.e., emission particle transport) and the reactive (displacement transport) physics.

1.Introduction.

The Schottky barrier diode, while simple in basic structural definition, remains an important device due to the fundamental advantages it offers to very-high-speed electronic applications. GaAs Schottky diodes are the primary nonlinear device used in millimeter- (mm) and submillimeter-wave (sub-mm) detectors and receivers. As these devices are extended farther into the THz regime, the electron physics will, for the first time, be impacted by polar optical phonon (POP) resonance that typically lies above 1 THz. It is well know that POPs are a dominant factor in determining the mobility of heteropolar crystals (e.g., GaAs) even at low frequencies where they contribute to electron scattering. Also at much higher frequencies, a frequency dependent permittivity dramatically affects the reflection and the absorption in bulk media [1]. The particular focus of this paper is the influence of POPs on the diode operation near the resonant frequency. Here, POP's are shown to introduce a novel effect on the nonlinear current-voltage (I-V) characteristics within Schottky diodes. In fact, both particle and displacement I-V components are strongly modified.

2. Analysis of POP-diode equations.

The first step in the analysis of Schottky diode operation with degenerate electron gas far from the barrier is to establish the exact spatial variation of the potential barrier as a function of depletion-region bias. Two regions can be identified. First, the depletion region (DR) adjacent to metal interface is situated between $0<z< w_s$ where w_s is the width of the depletion region. The second electron –screened region is spreading at $z> w_s$. The electron potential must align with the Femi energy , E_{FO}, of bulk electrons at the boundary point $z= w_s$. In the depletion region the displacement field, **D** , is a linear function of the one-dimensional (1-D) z-coordinate space

$$D(z) = eN_d(z-w); \qquad 0 < z < w_s \tag{1}$$

where N_d is the donor density, ewN_d is the total depleted charge. The total electric field , $\mathbf{F}= \mathrm{grad}(E_c)/e$ where E_c is the conduction band energy , and the lattice separation ,**u**, have to be found from equations [1]

$$\mathbf{D} = \alpha\mathbf{u} + \varepsilon_\infty \nabla E_c / e \tag{2}$$

$$\rho_m(\ddot{\mathbf{u}} + 2\gamma\dot{\mathbf{u}} + \omega_{to}^2\mathbf{u}) = \alpha\nabla E_c / e \tag{3}$$

where ε_o and ε_∞ are the zero-frequency and high-frequency electric permittivities respectively , ω_{to} and ω_{lo} are the transverse and longitudinal polar-optical frequencies respectively , and 2γ is the phonon damping-factor for the lattice, ρ_m is the mass density of the lattice

$$\alpha^2 = \rho_m\omega_{to}^2(\varepsilon_o - \varepsilon_\infty) = \rho_m\varepsilon_\infty(\omega_{lo}^2 - \omega_{to}^2) \tag{4}$$

In the external voltage oscillating with the frequency f the solution will converge after an initial transient period to periodic function with period 1/f

$$E_c(z,t) = \frac{e^2N_d}{2\varepsilon_o}\{(z - w(t))^2 + 2\frac{\varepsilon_o - \varepsilon_\infty}{\varepsilon_\infty}(z - w(t))(B(t) - w(t))\} \tag{5}$$

where the boundary condition for the conduction band energy have been used $E_C(z = w, t) = 0$,

$$\mathrm{B(t)} = \omega_{lo}\int_0^t dt_1 \mathrm{w(t - t_1)sin(t_1\sqrt{\omega_{lo}^2 - \gamma^2})exp(-\gamma t_1)}. \tag{6}$$

At z> $\mathrm{w_s}$ the Thomas-Fermi screened (TFS) approximation is applied

$$D(z) = -\sqrt{2eN_d\varepsilon_o}\{E_c(z) - E_{c\infty} + \frac{2}{5}E_{FO}[(1 + \frac{E_{c\infty} - E_c(z)}{E_{FO}})^{5/2} - 1]\}^{1/2} \tag{7}$$

where

$$E_{c\infty} = E_c(w_s) - E_{FO} = E_c(0) - eV_{bi} + eV_D \tag{8}$$

is the conduction band energy in the neutral region, $\mathrm{V_{bi}}$ is the built-in voltage, V_D is the electric potential applied across the active region (i.e., ignoring any bulk or spreading resistance) of the diode. Here, we assume that the epi-layer thickness, L_{epi}, is much greater than the entire depletion region. The displacement field must be continuous at the boundary of the DR and TFS regions. Hence applying Eqs. (1) and (7) the relation between w and $\mathrm{w_s}$ can be obtained

$$eN_d(w - w_s) = (\frac{6\varepsilon_o N_d E_{FO}}{5})^{1/2} \tag{9}$$

Equations (5) ,(8) and (9) may now be solved to obtain values for w and $\mathrm{w_s}$.
The current density through the electron-depleted and electron-screened regions consists of three components [2]. Specifically, there will be a thermionic emission current, J_{TE}, a field emission

$$\rho_m(\ddot{\mathbf{u}} + 2\gamma\dot{\mathbf{u}} + \omega_{to}^2\mathbf{u}) = \alpha\nabla E_c / e \tag{3}$$

where ε_o and ε_∞ are the zero-frequency and high-frequency electric permittivities respectively , ω_{to} and ω_{lo} are the transverse and longitudinal polar-optical frequencies respectively , and 2γ is the phonon damping-factor for the lattice, ρ_m is the mass density of the lattice

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$$eN_d(w_s - w) = (\frac{6\varepsilon_o N_d E_{FO}}{5})^{1/2} \tag{9}$$

Equations (5) ,(8) and (9) may now be solved to obtain values for w and $\mathrm{w_s}$.
The current density through the electron-depleted and electron-screened regions consists of three components [2]. Specifically, there will be a thermionic emission current, J_{TE}, a field emission

current due to tunneling, J_{FE}, and a displacement current, $J_C = -eN_d \frac{\partial w}{\partial t}$,due to the capacitance of the depletion region itself. The particle current is calculated in quasi-classical approximation [2].

3. Numerical simulation.

The previous model is used to analyze the time-dependent behavior of diode current density for an applied bias consisting of a dc component, V_O, and one harmonic of amplitude, $\hat{V}_1$, given by

$$V_D(t) = V_O + V_1(t) \quad ; \quad V_1(t) = \hat{V}_1 \sin(2\pi f \cdot t) \tag{10}$$

The model is solved for a degenerately-doped GaAs Schottky diode with a donar concentration in the epitaxial layer equal to $1\times10^{18} cm^{-3}$. The phonon damping-factor for GaAs is $2\gamma = 7.0\times10^{-3} \cdot \omega_{to}$ [3,4]. Numerical simulations were performed using the diode biasing defined in Eq. (10) with $V_O = 0.7\ volts$ and $\hat{V}_1 \cong 0.15\ volts$. Figure 1 plots the resulting *maximum* in the amplitude of the *particle* current density, J_P, that occurs over the large-signal steady-state cycle, versus source frequency, f. Here a *very* sharp peak is observed in the maximum particle-current-density, J_P^{max}, near the transverse polar-optical resonance frequency $f_{to} = 7.78$ THz. This 18 times increase in J_P^{max}, over the low-frequency result, is a direct indication of the strong coupling of the displacement-field to polar-optical phonons within the barrier depletion-region. The role of POP's is clearly revealed by a study the complex admittance per unit area as a function of frequency. Consider the result given in Fig. 2 for the fundamental-frequency (F-F) admittance defined as $Y_1 = \hat{I}_1 / \hat{V}_1$ where $\hat{J}_1$ is the amplitude of the current-density harmonic at frequency. The real and imaginary parts of the F-F admittance exhibit characteristics that are qualitative in nature with the complex permittivity . This is just a representation of the capacitive/inductive nature of the pre/post-resonance dielectric constant.

4.Conclusion.

This study shows that POPs have a dramatic effect on the nonlinear current-voltage (I-V) characteristics of Schottky diodes. Specifically, the POPs present within the electron-depleted region directly modify the potential barrier and in turn alter the time-dependent evolution of both the displacement and emission currents. The POPs reduce the potential barrier to particle current at the resonant frequency and lead to a very frequency-sharp (e.g. < *0.1* THz bandwidth @ *7.78* THz in GaAs) increase in particle current density. In addition, POP's perturb the spatial variation of the displacement field, and thus affect its time-dependent response to excitation. This work demonstrates a very *new and important* nonlinear phenomenon that will influence the future development of heterojunction based components. Finally, there exists the possibility that phonon tayloring, via material system engineering, may allow for the resonance to be shifted to lower frequencies.

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Terahertz Schottky Diode Dynamics near the Polar-Optical-Phonon Frequency

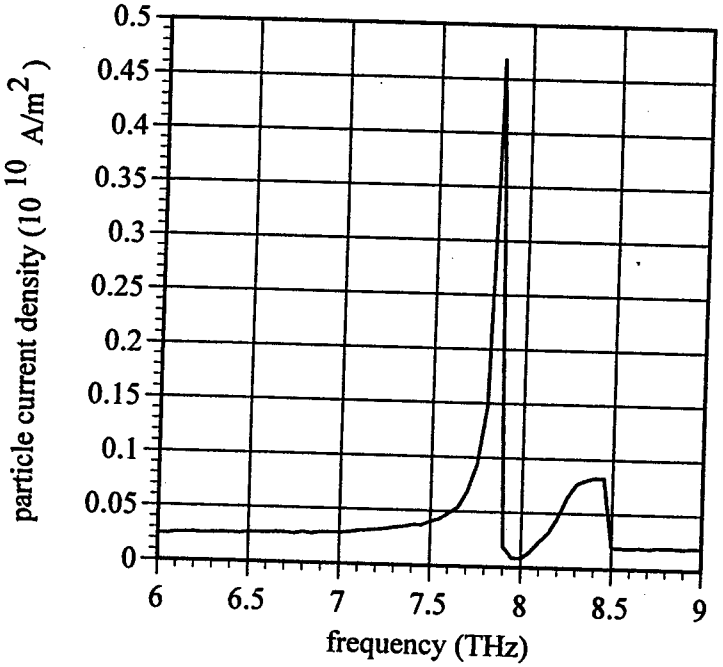


Fig. 1. Diode peak-particle-current density versus frequency.

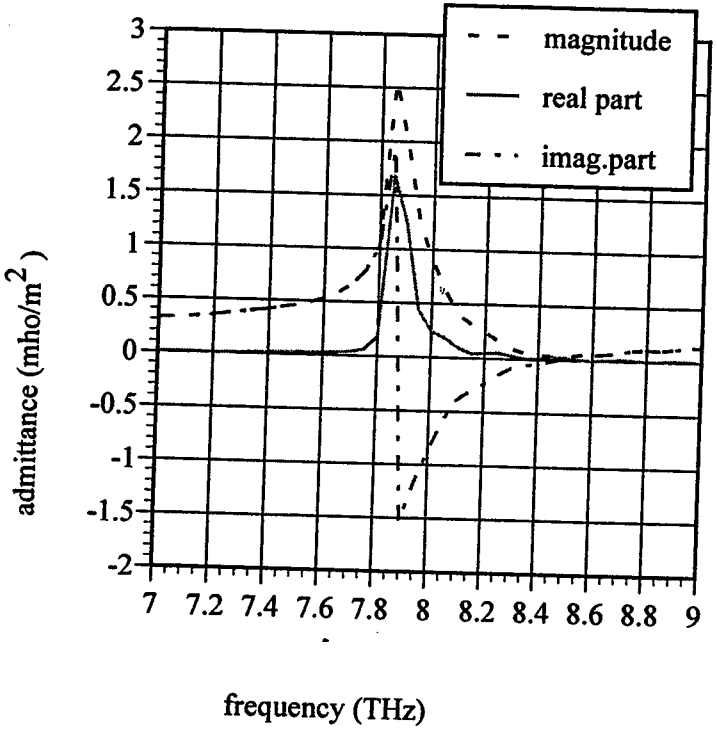


Fig. 2. The fundamental-frequency admittance versus frequency.

Organic Thin Film Transistor Models

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I. INTRODUCTION

Organic-based field effect transistors, see for example [1, 2], are emerging as viable contenders to amorphous Si technology. Organic five-stage ring oscillators with propagation delay 73 μsec have been demonstrated [2]. Complementary organic [3] and organic/inorganic circuits [4] have also been demonstrated. The best reported field-effect mobility and on/off ratio values for organic Thin Film Transistors (TFTs) have achieved values comparable to or exceeding those of amorphous Si TFTs. Field-effect mobility as high as 2.1 cm^2/V-s and on/off ratio as high as 10^8 have been measured for pentacene-based TFTs [5]. In this paper, we present organic TFT device models suitable for the device characterization and for the implementation in circuit simulators.

II. PENTACENE TFT DESIGN

In this work we simulate DC electrical characteristics of top contact pentacene TFTs (Figure 1). A heavily doped Si substrate served as a common gate for all TFTs on the chip. The thickness of a thermally grown SiO_2 gate dielectric layer was 300 nm. A pentacene active layer of 50 nm thickness was deposited by evaporation in vacuum from pre-purified commercially available pentacene powder. Details of the fabrication techniques can be found elsewhere [6]. Gold source and drain contacts were deposited by vacuum evaporation through a shadow mask. The TFT had the gate length L and the gate width W of 20 μm and 220 μm, respectively. An HP 4156B Precision Semiconductor Parameter Analyzer measured DC electrical characteristics of the pentacene TFT at room temperature. The measured characteristics varied depending on the measurement regime, humidity and, in certain cases, on the measurement history. A detailed analysis of these effects and the description of the measurement regimes will be published elsewhere [7].

III. PENTACENE TFT MODELING

We developed two semi-empirical models that allowed us to simulate pentacene TFT DC characteristics. Our first model (Model 1) is based on the crystalline silicon MOSFET Unified Charge Control Model [8]. In using this model we neglect the effects of velocity saturation, which are not observed in the pentacene TFTs. This model allows us to reproduce both below and above threshold regimes and provide continuity of the simulated device characteristics that is required for reliable circuit simulation. The model also accounts for contact resistances and is suitable for parameter extraction.

Figure 2 shows results of pentacene TFT modeling by Model 1. Figure 3 compares the measured data and the Model 1 calculations of the drain-source saturation current

versus gate-source voltage. The model accurately describes the saturation region. However, Model 1 deviates in the sub-threshold regime of the TFT operation (Figure 4) and in the linear above-threshold regime, see Figure 2.

Our second model, (Model 2) accounts for the fact that pentacene TFTs are accumulation mode devices (unlike Si MOSFETs). To model below and above threshold regimes of the pentacene TFT operation, we used an approach similar to that previously used for amorphous Si TFT modeling [9]. In amorphous Si TFTs operating above threshold, most of the induced charge is trapped in the localized tail states, leaving only a fraction of the total charge free to conduct the current [9]. Shur and Hack [10] proposed to include the effect of charge trapping into an empirical field effect mobility as

$$\mu_{FET} = \mu_0 \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma}$$

where γ and V_{AA} are empirical parameters that can be extracted from the $I_{DS}(V_{GS})$ characteristics and μ_n is a constant. The equations describing the above threshold current dependence on gate and drain voltages are almost the same as those for Model 1 (see ref. [8]) except that carrier mobility μ is substituted for μ_{FET}. Equation describing sub-threshold sheet density of the induced carriers n_{ind} can be found in [11] The results of the simulation of pentacene TFT input and output DC characteristics by Model 2 are illustrated in Figure 5 and Figure 6. The introduction of the gate-dependent mobility allowed us to simulate both sub-threshold and above-threshold regions of pentacene TFT operation.

The following parameter values were extracted by fitting the measured current dependencies:

$$\mu_o = 1 cm^2/V\text{-}s,\ \gamma = 0.41,\ V_{AA} = 7500V,\ V_T = 3V$$

Figure 7 shows dependence of the Model 2 field-effect mobility on gate-source bias together with the Model 1 field-effect mobility value. Gate-dependent mobility tends to reach the Model 1 mobility at high gate bias since more traps are filled at high gate bias and a larger fraction of carriers is induced into the conducting channel.

IV. SUMMARY

In summary, Model 1 for pentacene TFTs, based on the crystalline Si MOSFET Unified Charge Control model, is adequate for the simulation of the saturation current I_{sat} dependence on the gate-source voltage V_{GS}, while it deviates in linear above-threshold and in the sub-threshold regimes of the pentacene TFT operation.

The introduction of a gate-dependent mobility allowed us to simulate both sub-threshold and above threshold regimes of the pentacene TFT operation. The gate-dependent Model 2 field-effect mobility tends to reach the Model 1 mobility value at high gate bias. Both models can be used for parameter extraction and circuit simulation.

ACKNOWLEDGEMENT

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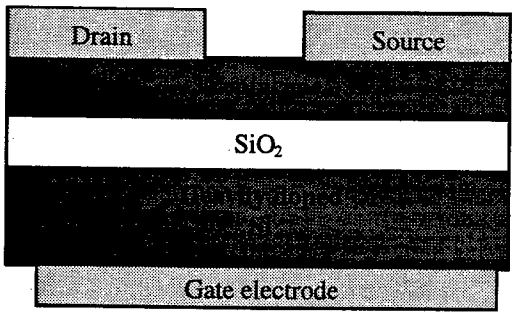


Figure 1. Top contact pentacene TFT structure. Heavily doped Si substrates serves as a common gate for all devices on a chip. W=220μm, L=20μm.

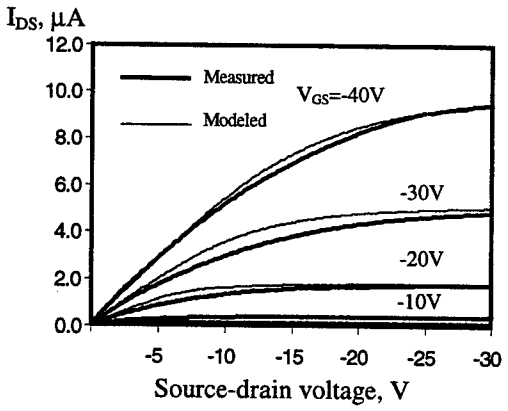


Figure 2. Drain current versus drain-source voltage. Comparison of Model 1 calculations with measured data.

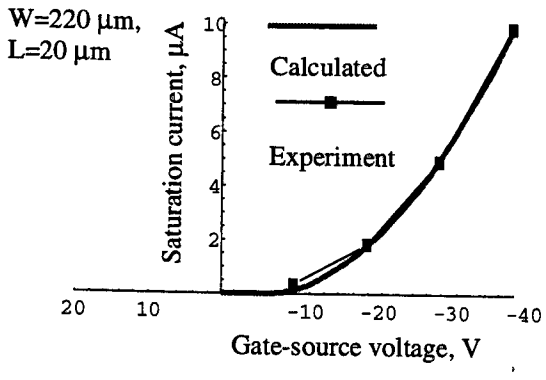


Figure 3. Saturation current at V_{DS}=-60V versus gate-source voltage. Comparison of Model 1 calculations with the measured data. Extracted Model 1 parameter values:

threshold voltage, V_t=-3V; leakage current, $I_{leak}=5\times10^{-12}$; transition width parameter, $\Delta=5$; field effect mobility, $\mu=0.1cm^2/V\text{-}s$; series resistance R_{sm}, $R_{dm}=0.3\Omega mm$; sub- threshold ideality factor, $\eta=60$; knee shape parameter $m_{sat}=3$

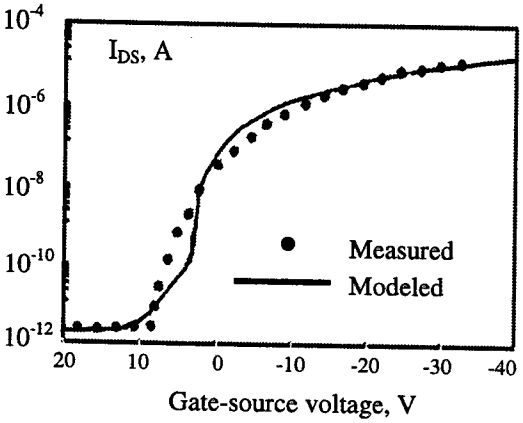


Figure 4. Drain current versus gate-source voltage. Comparison of measured data with Model 1 calculations (V_{DS}=-30V)

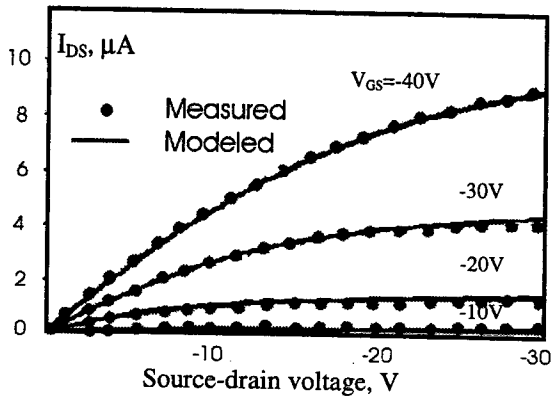


Figure 5. Comparison of measured and calculated by Model 2 drain-source current versus drain-source voltage.

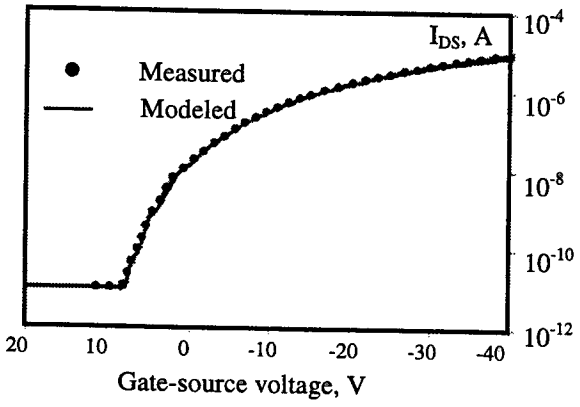


Figure 6. Comparison of measured and calculated by Model 2 drain current versus gate-source voltage at V_{DS}=-30V.

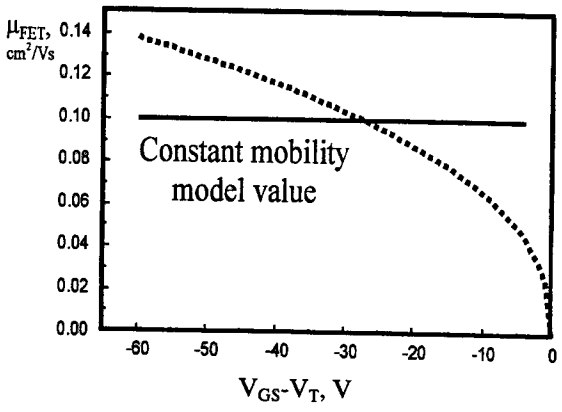


Figure 7. Dependence of the field-effect Model 2 mobility on V_{GT} and comparison with Universal Constant Mobility Model 1 value.

Investigating and Comparing the Effects of Lattice Heating in 4H-SiC and Si Devices

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I. Introduction

Because of its large band gap, large thermal conductivity, and large high-field drift velocity, SiC is a promising electric material for use in semiconductor devices operating at high temperature and power.[1] In order to determine the extent to which 4H-SiC based devices will be applicable for high power applications investigations are required. Central to these investigations is the ability to theoretically predict the thermal characteristics of 4H-SiC devices before considerable investment is made for their fabrication.

In this work we report on the development of a simulation tool and the results of applying this tool for calculating the effect of the lattice temperature characteristics in 4H-SiC devices. We find that for high power applications, including the effect of local lattice heating is very important for simulation of current-voltage characteristics. We also compare the lattice temperatures resulting from Joule heating in 4H-SiC with that of Si. We find that the temperature of Si becomes significantly higher since 4H-SiC has much higher thermal conductivity.

To understand the details of device operation, including the effects of lattice heating, we numerically solve the drift-diffusion (DD) semiconductor equations coupled to the lattice heat flow equation.

These equations are shown below.

Drift-Diffusion Equations

$$\nabla^2\phi = \frac{q}{\epsilon}(p + n - N_d^+ + N_a^-)$$

$$0 = \nabla \cdot (\mu_n n \nabla\phi - \mu_n \frac{k_B}{q} T_L \nabla n) - G_n + R_n$$

$$0 = \nabla \cdot (\mu_p p \nabla\phi - \mu_p \frac{k_B}{q} T_L \nabla p) + G_p - R_p$$

Heat Flow Equations

$$0 = \kappa \nabla^2 T_L + H$$

$$\mathrm{H} = \mathbf{J} \cdot \mathbf{E}$$

We achieve this by dividing our simulations into two basic parts: the drift diffusion and the heat flow blocks. First, we solve the drift diffusion equations under isothermal conditions, with the lattice temperature $T_L = 300\mathrm{K}$ everywhere in the device. The solution is obtained by first employing finite differences and exponential fitting to discretize the drft-diffusion equations. We then solve our discretized equations numerically using a fixed point iterative method[2]. When the iterative begins to linearly converge, we switch our solution method to a Newton approach. This allows for quadratic

convergence and lower error[3].

Once the drift diffusion equations block is converged, we solve the heat flow equation independently. The heat flow is solved by first using a linear discretization method which yields a system of algebraic equations. The resulting equations are then solved using Gaussian elimination for a banded matrix. Values for the variables **J** and **E** are obtained from the drift diffusion block and input into the heat flow block. The resulting values for position-dependent lattice temperature are then input back into the drift-diffusion block, which is then solved again. This procedure continues iteratively until the two blocks converge. The solution gives the carrier concentrations, electrostatic potential, current density, and lattice temperature throughout the device.

II. Simulation Results

At this time we will present the simulation results from the both 4H-SiC and Si devices. Data taken from the isothermal DD simulation is represented with a line while the drift diffusion-heat flow (DD-HF) simulation results are given by x's. At the boundaries semiconductor lattice temperature, T_L, is fixed at $T_o = 300$ K.

NPN BJT

Figures 1a and 1b show the simulation results for both 4H-SiC and Si NPN BJT's. The BJT's have $0.1\mu m$ P-type bases sandwiched between emitter and collector N-type regions. For this particular data set, the emitter voltage, V_E, is equal to -0.73 Volts, the base voltage is 0V, and the collector voltage is equal to 15V. The figure shows that calculations predict that lattice heating in the Si BJT is three times higher than of the 4H-SiC BJT. The peak lattice temperature increases from 300K in the isothermal approximation to 310K in the Si, and 303K in the 4HSiC. The figure also shows that including the effect of lattice heating causes a small variation in current. We see that the simulations show that lattice heating results in a 8% decrease in current for the Si BJT, and a 2% decrease in the case of 4H-SiC results. The decreased current is due to reduced mobility with temperature.

N^+NN^+ Diode

The N^+NN^+ Diode consists of a $0.3\mu m$ wide $N = 2 \times 10^{17}/cm^3$ region, sandwiched between two regions of $N^+ = 2 \times 10^{19}/cm^3$. The structure is often used to mimic the inversion layer of an NMOSFET. For the N^+NN^+ Diode, the left side voltage is equal to 0.0 Volts, and the right side voltage is equal to 10 Volts. For this device, there is considerable discrepancy between the iso-DD and DD-HF simulation results. The variation between the iso-DD and DD-HF results can be observed through lattice temperature and current density calculations. As bias voltage, V_{RL}, increases, the DD-HF model is needed in order to produce more accurate I-V curves. This is demonstrated in the in Figures 2a and 2b. The figures show that the lattice temperature increases from the isothermal approximation of 300K, to approximately 325K in Si, and 310K in 4H-SiC. Clearly the 4H-SiC dissipates heat more efficiently. Furthermore, the current density in the Si deceases by almost 20% due to lattice heating, while lattice heating in the 4H-SiC device causes only a 7% decrease in current.

III. Summary

These simulation results can be summarized as follows. Our DD-HF method verified our initial assumption that, because the thermal conductivity of 4H-SiC is three times higher than the thermal conductivity of Si, Si devices increase in temperature by about times more than the 4H-SiC devices during high voltage operation. We also observed that the current density, calculated using the DD-HF method is lower than J calculated using isothermal DD. This shows the effect that carrier mobility, $\mu_{n,p}$ decreases as temperature increases due to Joule heating in the device. This is significant because the corrected I-V curves, when compared to experimental data, can help improve device parameter calculations.

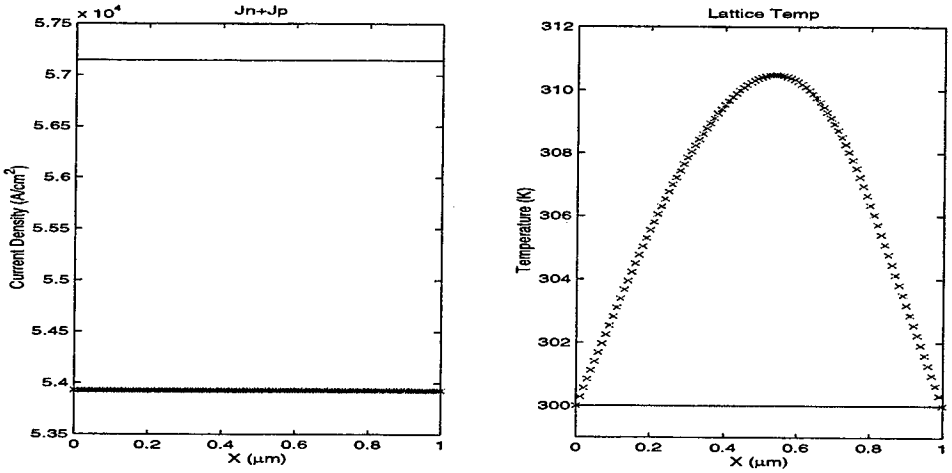


Figure 1(a) **Si NPN BJT** – V_{emit} = -0.73 V, V_{coll} = 15 V, V_{base} = 0 V
, line - iso-DD x - DD-HF

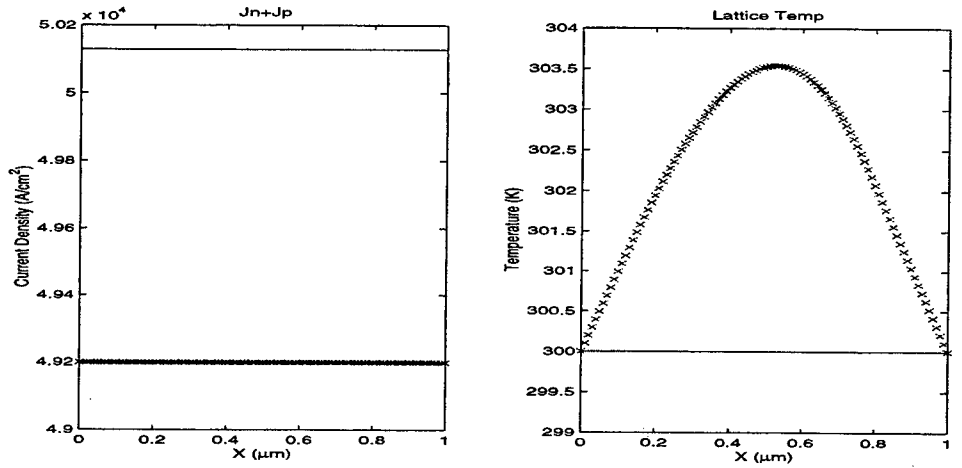


Figure 1(b) **4H-SiC NPN BJT** – V_{emit} = -0.73 V, V_{coll} = 15 V, V_{base} = 0 V
line - iso-DD x - DD-HF

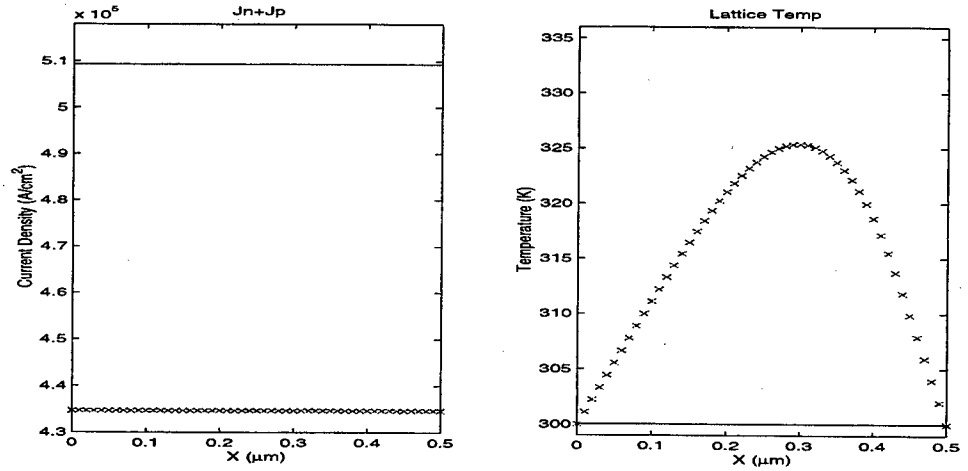


Figure 2(a) **Si N^+NN^+ Diode** – V_L = 0.0V, V_R = 10 V
line - iso-DD x - DD-HF

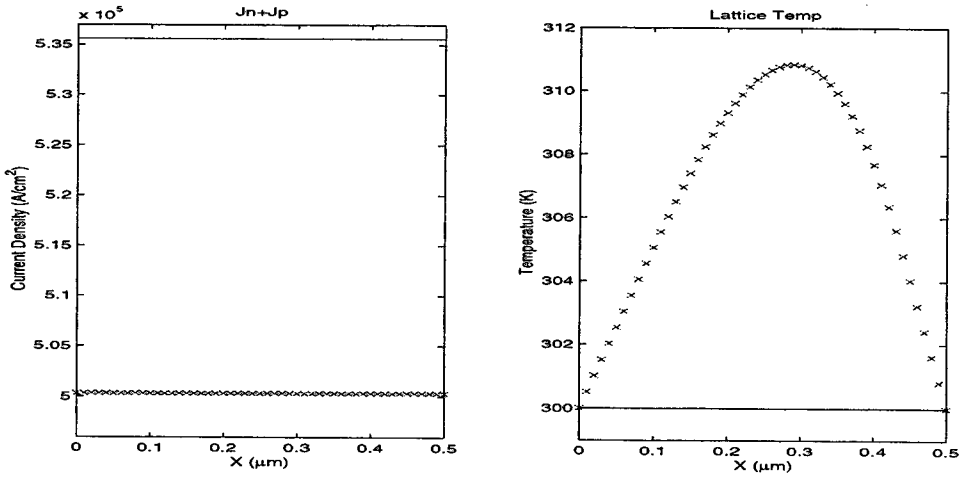


Figure 2(b) **4H-SiC N^+NN^+ Diode** – $V_L = 0.0$ V, $V_R = 10$ V
line - iso-DD x - DD-HF

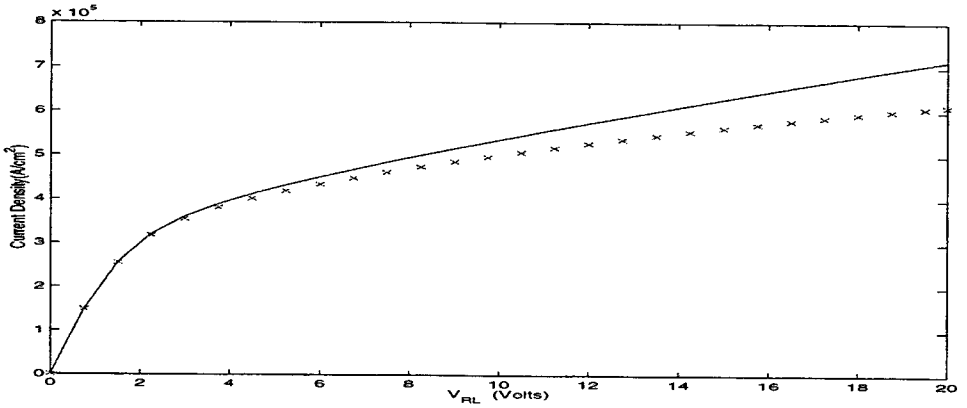


Figure 3 **4H-SiC N^+NN^+ Diode** — I-V Curve
line - iso-DD x - DD-HF

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The Electrical Property of Doped Semiconductor Due to Ionized Impurity Scattering

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I. INTRODUCTION

As it is known that substitution of a small fraction of the atoms of a semiconductor by appropriate foreign atoms (impurities) can change dramatically the electrical conductivity of the material. When doped atom is replaced in the crystal, attraction is reduced considerably by the polarization of the electronic cloud of the crystal between the electron and ion. Generally a Coulomb type potential is used to describe the interaction between an iterative electron and an ionized impurity. Conwell and Weisskopf [1] used such potential to treat the scattering effect of ionized impurity to carrier. In 1950's, Brooks and Herring [2] utilized Yugawa type screening potential to consider the scattering effect between the ionized impurity and electron in doped system and obtained an analytical mobility expression in nondegenerate situation. Since then, Brooks-Herring's treatment on carrier mobility has been met wide applications in concerning conductive processes in doped material. However, recently Poklonski *et al.*, pointed out [3] that the Brooks-Herring mobility overestimates carrier mobility in both nondegenerate semiconductors and degenerate semiconductors, and proposed new expressions of carrier mobility based on treating the scattering potential with a step function to cut off long distance effect of the Coulomb type potential. We think that such kind of long distance interaction cutoff treatment is slightly arbitrary, furthermore, an unphysical sudden change of the interaction potential is introduced unnaturally. Based on model potential presumption and the Boltzmann transport equation in relaxation time approximation form, new mobility expressions are proposed in this paper.

II. DEDUCTION OF THE MOBILITY

In order to overcome the mentioned shortcomings of other's mobility expressions, a new kind of ionized impurity-electron interaction potential is used and which can be expressed as below.

$$U(r) = \frac{Ze^2}{4\pi\epsilon r}\{[1-\exp(-\alpha r)]^2 - 1\} \tag{1}$$

where Ze is the electrical charge of the ionized impurity, $\epsilon = \epsilon_0\epsilon_r$ the static permittivity of an undoped system, α the screening parameter. In Figure 1, three kinds of interaction potentials are compared with each other. In this figure, the interaction potential proposed here is denoted as $V_3(r)$ which, obviously has good short distance feature that makes it fit the Coulomb potential in that region much better, and the fine long distance characteristic which approaches to zero much faster than that of Coulomb one and slower than that of Yugawa or Thomas-Fermi one. Therefore, it is expected that it can conquer the problems mentioned above.

In our deduction, the relaxation time approximation form [4] of Boltzmann transport equation is used. Under the condition of steady state problem within the restriction of homogeneousness, the relaxation time τ can be expressed as

$$\frac{1}{\tau} = \frac{\Omega}{(2\pi)^3}\int P(\mathbf{k}',\mathbf{k})(1-\cos\theta)d^3\mathbf{k}'. \tag{2}$$

Where θ is the angle between the wave vector $\mathbf{k}$ of a initial state and $\mathbf{k}'$ of a final state.

Considering electron-lattice interaction and using time-dependent perturbation method [5], the transition probability for a parabolic band is

$$P(\mathbf{k}', \mathbf{k}) = \frac{2\pi}{\hbar} N\Omega |U(q)|^2 \delta(E' - E). \tag{3}$$

Here the ionized impurity with concentration N is randomly distributed and independent to each other, Ω the volume of the system, $\mathbf{q} = \mathbf{k}' - \mathbf{k}$ taken to be much smaller than a reciprocal lattice vector, and $U(q)$ the Fourier transform of the impurity potential $U(r)$. For the sake of simplicity and acquiring analytical mobility expressions, only elastic scattering between localized ionized impurity centers and carrier electron is considered in this paper.

The component of the interaction potential in momentum space is

$$U(q) = \frac{Ze}{\epsilon\Omega}\left[\frac{1}{q^2 + (2\alpha)^2} - \frac{2}{q^2 + \alpha^2}\right] \tag{4}$$

The acquired relaxation time τ^{-1} is given as

$$\frac{1}{\tau} = \frac{NZ^2 e^4 E^{-3/2}}{16\sqrt{2}\epsilon^2\sqrt{m^*}} M(b)$$

where E is the energy of a scattered electron, m^* the effective mass of the electron, and function $M(b)$ is

$$M(b) = \frac{16}{3}\ln(1+b) - \frac{13}{3}\ln(1+\frac{b}{4}) - (\frac{4b}{1+b} + \frac{b}{4+b}) \tag{5}$$

with

$$b = \frac{8m^* E}{\hbar^2 \alpha^2}. \tag{6}$$

According to the viewpoint of statistical physics [6], the mobility μ can be calculated by

$$\mu = \frac{e}{m^*}\langle \tau \rangle = \frac{e}{m^*} \frac{\int_0^\infty \tau E^{3/2}\left(-\frac{\partial f}{\partial E}\right) dE}{\int_0^\infty E^{3/2}\left(-\frac{\partial f}{\partial E}\right) dE} \tag{7}$$

where f is Fermi-Dirac distribution function. Next, let us consder nondegenerate and degenerate situation separately.

II.1 NONDEGENERATE SITUATION

In this case, Fermi-Dirac distribution function reduces to Maxwell-Boltzmann distribution. The final analytical mobility expression is as follow

$$\mu^{\mathrm{nd}} = \frac{128\sqrt{2\pi}\epsilon^2 (k_B T)^{\frac{3}{2}}}{NZ^2 e^3 \sqrt{m^*} M(b_0)}. \tag{8}$$

For comparing the acquired analytical mobility expression with Brooks-Herring's, the screening parameter α^{-1} is chosen as Debye length $l_D = \sqrt{\frac{\epsilon k_B T}{e^2 n}}$ [7], where n is the carrier concentration.

The difference is the function $M(b_0)$ in this research and the function $f_{BH}(\beta)$ in Brooks-Herring's expression which are schematically plotted in Figure 2. It is clear that the overestimation on carrier mobility by Brooks-Herring expression can be at least partly overcome by the mobility proposed here. The direct comparison between the calculated mobility of this research and the Brooks-Herring mobility at the absolute temperature $300K$ with the same parameters are plotted in Figure 3.

II.2 DEGENERATE SITUATION

In this situation, the deduced degenerate mobility is of the following form

$$\mu^{\mathrm{deg}} = \frac{3\pi}{2}\left(\frac{\hbar}{e}\right)^3 \left(\frac{4\pi\epsilon}{m^*}\right)^2 \frac{n}{N_I M(E_F)} \tag{9}$$

where $M(E_F)$ is nothing but the expression of the Eq.(5) as $E = E_F$ with $b = \frac{8m^* E_F}{\hbar^2 \alpha^2}$.

In order to keep the validity of Born approximation, it is needed to make phase shift analysis on the scattering process according to the quantum mechanics point of view [9]. Using Friedel sum rule [10] which was pointed by Krieger *et al.* [11], one can get the screening parameter α under the condition of $\frac{E_F}{k_B T} \gg 1$, and finally the b expression as below

$$b = \frac{1}{1.75}\left(\frac{\hbar}{e}\right)^2 \left(\frac{4\pi\epsilon}{m^*}\right)(3\pi^5 n)^{1/3} \tag{10}$$

At the last, the degenerate mobility can be represented as

$$\mu^{\deg} = \frac{3\pi}{2}\left(\frac{\hbar}{e}\right)^3 \left(\frac{4\pi\epsilon}{m^*}\right)^2 \frac{n}{N_I M(b)} \tag{11}$$

where b is expressed in Eq.(10), function $M(b)$ is in Eq. (5) and $n = (1-K)N$.

For the degenerate case of ZnO:Al at room temperature, the calculated mobility (Cf. Eq.(11)) is compared with that of Brooks-Herring which is shown in Figure 4. It is clear that the overestimation on carrier mobility by the Brooks-Herring formula in such case also can be at least partly subdued by the expression proposed here.

III. COMPARING WITH AVAILABLE EXPERIMENTAL DATA

For comparing the calculated results with available experimental data for the case of ZnO doped with Al, besides considering the above discussed ionized impurity scattering, lattice and piezoelectric scattering mechanism are also included. The mobility expression μ_l [12] because of lattice acoustic phonon scattering is used. Since ZnO is a piezoelectric material, the mobility μ_{pz} due to the carrier scattered by longitudinal acoustic phonon because of piezoelectric scattering [13, 14]is also used.

The total mobility can be obtained by $\frac{1}{\mu_T} = \frac{1}{\mu_{ion}} + \frac{1}{\mu_l} + \frac{1}{\mu_{pz}}$. The related calculated results of mobilities, conductivities, resistivities and available experimental data are listed in Table 1 for comparison. One can see that the agreement with experimental data is fairly excellent and much better than those of Brooks-Herring's.

IV. SUMMARY

The deduced analytical mobility expressions due to ionized impurity scattering for both nondegenerate and degenerate cases can at least partly subdue the overestimation on the mobility in the same case by the Brooks-Herring expressions. The fact that the calculated carrier mobility based on the above derived expressions agrees with the related experimental data (both the magnitude order and approximately the value) indicates that the model potential postulation and the proposed analytical expressions for mobilities due to the ionized impurity scattering are physically reasonable and practically feasible.

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Table 1: In this table the theoretical calculation values using the proposed analytical expression of this research (labeled as TR), those of utilizing Brooks-Herring expression (labeled as BH) and available experimental data (represented as ED) are listed. Here n represents the carrier concentration, ion stands for considering the ionized impurity scattering only. Pp represents the physical properties and total indicates the situation where the lattice scattering, piezoelectric scattering and the ionized impurity scattering are taken into account together.

$n(cm^{-3})$	Pp	E D	TR(total)	TR(ion)	BH(total)	BH(ion)
$\sim 5 \times 10^{20a}$	$\mu(cm^2/Vs)$	20-30[a]	23.7	24.8	36	38.7
	$\sigma(\Omega^{-1}cm^{-1})$	$> 10^{3a}$	1.90×10^3	1.98×10^3	2.88×10^3	3.10×10^3
$\sim 7.5 \times 10^{20b}$	$\mu(cm^2/Vs)$		21.7	22.7	33.1	35.4
	$\sigma\ (\Omega^{-1}cm^{-1})$		2.6×10^3	2.72×10^3	3.97×10^3	4.25×10^3
	$\rho(\Omega cm)$	$\sim 4.7 \times 10^{-4b}$	3.8×10^{-4} $\sim 4 \times 10^{-4}$	3.7×10^{-4} $\sim 4 \times 10^{-4}$	2.5×10^{-4}	2.4×10^{-4}

[a]Ref [15]
[b]Ref [16]

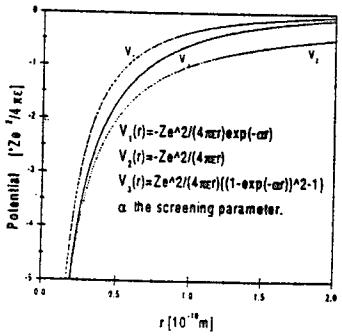


Figure 1: Three different model potentials.

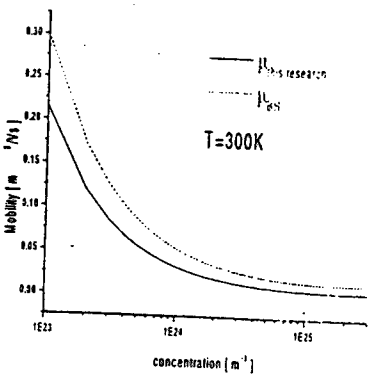


Figure 3: Calculated results using the mobility expression of this paper and compared with the results of Brooks-Herring mobility expression with the same parameters in nondegenerate case.

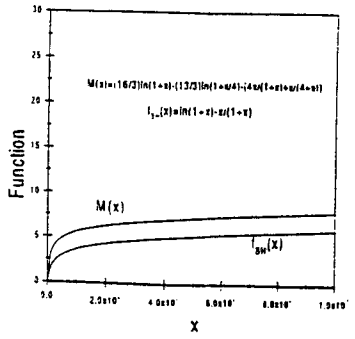


Figure 2: The schematic drawing for comparing the function $M(x)$ and $f_{BH}(b)$.

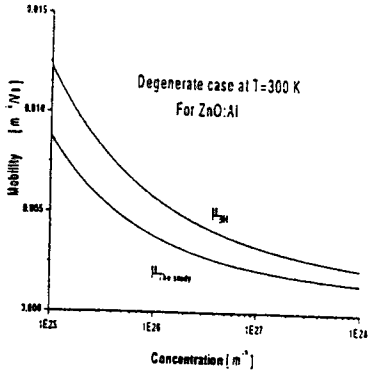


Figure 4: Calculated results of mobility expression of this study and compared with the results of Brooks-Herring mobility expression with the same parameters in degenerate case.

The Response Times and the Impedance of the Resonant-Tunneling Diodes

Michael Feiginov

Abstract— **We have shown that due to the Coulomb interaction of the electrons in the quantum well with emitter and collector the response times of the resonant-tunneling structures (τ_{resp}) can be much smaller as well as much larger than the quasibound-state lifetime. A simple analytical expression for the impedance of the resonant-tunneling diode has been derived that takes into account the Coulomb interaction and the quasibound-state lifetime. A simple equation relating τ_{resp} to the static differential conductance has been obtained also that allows one to get τ_{resp} in the static measurements of the I-V curve.**

Keywords— **Resonant tunneling diode, response time, impedance.**

I. Introduction

The resonant tunneling diodes (RTD) on the basis of the double-barrier heterostructures [1] are one of the fastest operating devises nowadays [2]. To optimize the RTD it is necessary to understand what are the mechanisms that are determining its high frequency operation. The 2D electron gas is present in the quantum well (QW) of RTD when the resonant tunneling current is nonzero and, until now, no consideration has been given to the effect of the Coulomb interaction of the 2D electrons with emitter and collector on the response time (τ_{resp}) of the RTD. So far it was believed [1] that τ_{resp} can not be less than the electron dwell times in the QW due to the tunneling to the emitter (τ_e) and collector (τ_c). In the present work we show that it is not true and that τ_{resp} can be much less than τ_e and τ_c. The Coulomb interaction should lead to the similar effect in other resonant tunneling structures, e.g., the quantum cascade laser [3], [4], also it should be essential for the domain speed in the superlattices [5], [6].

The problem of the equivalent circuit of the RTD is closely related to that of the response times. Many equivalent circuits have been proposed. Among them the simplest RC-circuit, RLC-circuit [7], the circuit from [8] are in most common use. Nevertheless, there are no a simple and comprehensive, in the same time, way to describe the impedance of the RTD. We solve the problem in the present work. An attempt to solve the problem has been made in [8], but the basic Eqs. used there are incorrect (see below), and in [9]-[11], but the results are so cumbersome that it seems to be possible to use them just for the numerical calculations and they leave unveiled the underlying physics.

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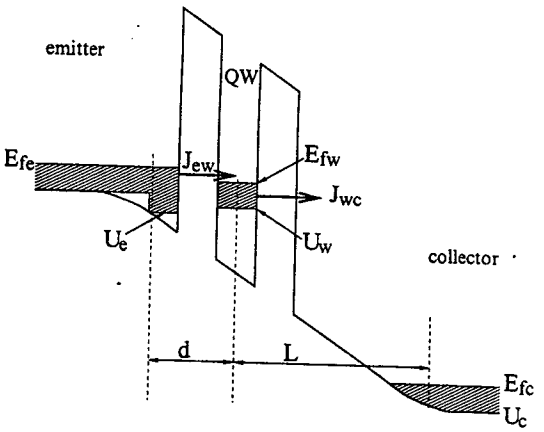


Fig. 1. The band diagram of the RTD in resonant tunneling regime. 2D electrons in the QW are formed by the balance of the resonant emitter-well current (J_{ew}) and the nonresonant well-collector one (J_{wc}).

II. Basic equations

We consider the RTD (Fig.1) in the sequential tunneling model [12] and suppose that the transit time of electron through the depletion region on the collector side of RTD is not essential. The current distribution is assumed to be homogeneous in the plane of the barriers. The set of Eqs. consists of Eq.(1) describing the Coulomb interaction of the electrons in the QW with emitter and collector, the Eqs. for emitter-well (J_{ew}) (2) and well-collector (J_{wc}) (3) currents, continuity Eqs. (4) and (5), electroneutrality Eq.(6) and Eq.(7) for emitter-collector Fermi level difference.

$$V - V_0 = N_{2D}\frac{e^2}{C} - (E_{fe} - E_{fc})\frac{d}{L+d}, \quad (1)$$

$$J_{ew} = -\left[E_{fe} - E_{fw}\right]\rho_{2D}\tilde{\theta}(V)\frac{e}{\tau_e}, \quad (2)$$

$$J_{wc} = -N_{2D}\frac{e}{\tau_c}, \quad (3)$$

$$-e\frac{\partial}{\partial t}N_{2D} = J_{ew} - J_{wc}, \quad (4)$$

$$\frac{\partial}{\partial t}Q_c = J_{wc} - J_{RTD}, \qquad (5)$$

$$Q_c + Q_e - eN_{2D} = 0, \qquad (6)$$

$$E_{fc} - E_{fe} = (Q_e d - Q_c L)\frac{4\pi e}{\epsilon}, \qquad (7)$$

where J_{RTD} is the density of the current through RTD, $N_{2D} = [E_{fw} - U_w]\rho_{2D}$ is the 2D electron concentration in the QW, ρ_{2D} is the 2D density of states in the QW, E_{fi} and U_i are the Fermi levels and the band bottom energies in the emitter close to the barrier ($i = e$), QW ($i = w$) and collector ($i = c$); $V = U_w - U_e$. Q_e and Q_c are 2D charge densities in the emitter and collector, respectively. We suppose for simplicity that $U_w > E_{fe}$ when the external bias is zero, $V = V_0$ in the case. Further, we shall be interested in such external biases only, when there is the resonant tunneling current ($U_w < E_{fe}$). τ_e and τ_c are supposed to be independent of V. The effective emitter-well distance (d) is more than the emitter-barrier thickness by the Thomas-Fermi screening length and the half width of the QW; L is the similar well-collector distance, that includes also the thickness of the depletion region. $C = \epsilon(L + d)/4\pi Ld$ is the capacitance of the QW per unit area. The form-factor $\tilde{\theta}(V)$ describes the broadening of the resonant levels for the emitter-well transitions, Fig.2. It should be pointed out that in the case of 3D emitter $\tilde{\theta}(V)$ is the step-function $\theta(V)$, if the broadening of the resonant level is negligibly small. An another Eq. has been used in [8] instead of (2) and the dependence of the well-emitter current on V was neglected there. We represent the solution of the set (1-7) as the sum of the static solution (the superscript "0") and a small fluctuation: $V = V^0 + \delta V(t)$, $N_{2D} = N^0_{2D} + \delta N_{2D}(t)$, $E_{fi} = E^0_{fi} + \delta E_{fi}(t)$, etc.

III. Static I-V curve

Eq. for $N^0_{2D}(V^0)$ follows from (1-4):

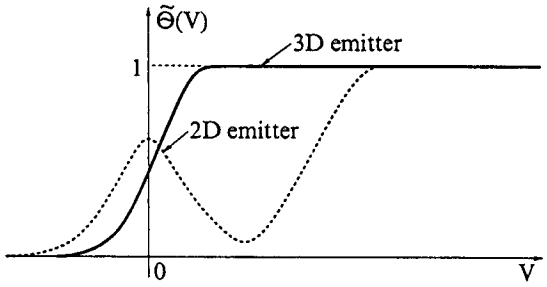


Fig. 2. The form-factor of the emitter-well resonant tunneling transitions. The solid line is for the transitions from 3D emitter, and the dashed line describes an additional contribution of the 2D emitter (i.e. from the accumulation region in Fig.1).

$$N^0_{2D} = \rho_{2D}\frac{\left[E^0_{fe} - U^0_e - V^0\right]\tilde{\theta}(V^0)}{\tau_e/\tau_c + \tilde{\theta}(V^0)}, \qquad (8)$$

This Eq., combined with (1) and (3), gives the static I-V curve $J^0_{RTD}(E^0_{fe} - E^0_{fc})$ as an implicit function of V^0, $J^0_{RTD} = J^0_{wc} = J^0_{ew}$. The I-V curve can have Z-type region, if the broadening of the resonant levels is sufficiently small [13]-[18].

IV. Response time

The Eq.(9) for the linear response of the RTD on the bias variation ($\delta E_{fc}(t)$) follows from (1-4) also. We suppose, without loss of generality, that $E_{fe}(t) = E^0_{fe}$ and $U_e(t) = U^0_e$.

$$\left[\frac{\partial}{\partial t} + \frac{1}{\tau_{resp}}\right]\delta N_{2D}(t) \propto \delta E_{fc}(t), \qquad (9)$$

$$\frac{1}{\tau_{resp}} = \frac{1}{\tau_c} + \frac{\tilde{\theta}(V^0)}{\tau_e} + \frac{e^2\rho_{2D}}{C}\left[\frac{\tilde{\theta}(V^0)}{\tau_e} - \frac{E^0_{fe} - U^0_e - V^0}{1 + \tilde{\theta}(V^0)\tau_c/\tau_e}\frac{\tilde{\theta}'(V^0)}{\tau_e}\right]. \qquad (10)$$

τ_{resp} has the sense of the tunnel relaxation time of the charge fluctuations in the QW. The first and the second terms in (10) describe relaxation due to the electron tunneling to collector and emitter, respectively, and they give the electron dwell time in the QW: $1/\tau_{dwell} \equiv 1/\tau_c + \tilde{\theta}(V^0)/\tau_e$. As E_{fw} changes, the energy of the bottom of the 2D subband in the QW also shifts due to the Coulomb interaction of the electrons in the QW with emitter and collector. As a result, firstly, an additional contribution in J_{ew} appears due to the change of the number of the free states in the QW available for tunneling (third term). Secondly, the current changes owing to the form-factor $\tilde{\theta}(V)$, that is described by the fourth term in (10). The factor before the square brackets in (10) equals to $\delta U_w/\delta E_{fw}$ and its typical value is $5 \div 10$. It should be noted that due to the factor the third term in (10) is always much larger than the second one. The last term in (10) can increase as well as diminish τ_{resp}. The factor before $\tilde{\theta}'(V^0)/\tau_e$ is the emitter-well Fermi-level difference, $\tilde{\theta}'$ is the derivative of the form-factor. If the Coulomb effects are omitted (the limit of $C \to \infty$), then $\tau_{resp} = \tau_{dwell}$. The Coulomb interaction significantly changes τ_{resp}.

Eq.(11) relating the static differential conductance (G^0_{RTD}) to τ_{resp} follows from (1-4) also:

$$G^0_{RTD} = \left[1 - \frac{\tau_{resp}}{\tau_{dwell}}\right]\frac{C_{wc}}{\tau_c}, \qquad (11)$$

where $C_{wc} = \epsilon/4\pi L$ is the well-collector capacitance. C_{wc} is determined by the structure geometry, the doping profile and external bias, and its value is known with good accuracy as a rule. One can get τ_c from (3) by measuring N^0_{2D} in QW (see, e.g., [19]). If the collector barrier is thinner or the same as the emitter one, then $\tau_{dwell} \approx \tau_c$. In the case, Eq.(11) gives possibility to get easily τ_{resp} in the static measurements of G^0_{RTD}.

V. RTD IMPEDANCE

An expression for linear impedance ($Z_{RTD} \equiv \delta E_{fc}/e\delta J_{RTD}$) follows from the set (1-7):

$$\frac{1}{Z_{RTD}(\omega)} =$$

$$i\omega C_{ec} + G^0_{RTD}\frac{1 + i\omega\tau_c d/(L+d)}{1 + i\omega\tau_{resp}}. \quad (12)$$

$C_{ec} = \epsilon/4\pi(L+d)$ is the emitter-collector capacitance. If the contact resistance is the significant one, it should be connected in series with Z_{RTD} (12).

VI. DISCUSSION

As it follows from (12), the RTD could be considered as RC-circuit in the low frequency limit only, when $\omega\tau_c d/(L+d) \ll 1$ and $\omega\tau_{resp} \ll 1$:

$$\frac{1}{Z_{RTD}} \approx i\omega\tilde{C} + G^0_{RTD}, \quad (13)$$

$$\tilde{C} = C_{ec} + G^0_{RTD}\left[\tau_c\frac{d}{L+d} - \tau_{resp}\right]. \quad (14)$$

The analysis of (14) and (11) shows that $\tilde{C} > 0$, although it can be essentially less than C_{ec}. It is worth noting that the RTD impedance (12) has formally the form coinciding with RLC-circuit [7], when $\omega\tau_{resp} \gtrsim 1$ and $\omega\tau_c d/(L+d) \ll 1$:

$$\frac{1}{Z_{RTD}(\omega)} \approx i\omega C_{ec} + \frac{G^0_{RTD}}{1 + i\omega\tau_{resp}}. \quad (15)$$

The "inductance" describes the delay of the current with respect to voltage [7] and the delay is τ_{resp} ("inductance" $l = \tau_{resp}/G^0_{RTD}$) rather than τ_{dwell} ($l = \tau_{dwell}/G^0_{RTD}$, [7]). The second term in the numerator of (12) appears due to the currents recharging Q_e and Q_c, the currents were omitted in [7]. In the general case one should use Eq.(12).

The I-V curve of the RTD could be broken down into two regions. Firstly, *the region where the resonant-tunneling current grows up.* $G^0_{RTD} > 0$ here and, as it follows from (11), $0 < \tau_{resp} < \tau_{dwell}$. In the case of the RTD with 3D emitter just the first three terms are left in (10) ($\bar{\theta}(V^0) \approx 1$ in the region) and $\tau_{dwell}/\tau_{resp} \approx 5 \div 10$ due to the third one, if $\tau_e \lesssim \tau_c$. It is in accordance with the unexplained result of [20], where $\tau_{dwell}/\tau_{resp} \approx 7$ was measured. τ_{resp} can drastically drop down owing to the last term in (10) in the case of 2D emitter and small broadening of the resonant levels, since $\bar{\theta}'(V^0) < 0$. For example, if $\tau_e \approx \tau_c \approx 100\ ps$, $e^2\rho_{2D}/C \approx 10$, $E^0_{fe} - U^0_e \approx 20\ meV$, $|\bar{\theta}'(V^0)| \approx \tau_s^2/\hbar\tau_{dwell}$, where τ_s is the the phonon scattering time and $\tau_s \approx 10\ ps$ (that corresponds to the mobility of $250 \times 10^3\ cm^2/Vs$), then $\tau_{resp} \approx 0.3\ ps$. That is, τ_{resp} can be by the orders of magnitude less than τ_{dwell} in the case.

The low-frequency capacitance of RTD (14) can have a peak in that region of the I-V curve, if $\tau_c d/(L+d) > \tau_{resp}$ (i.e. L or τ_e are sufficiently small) and this is in accordance with experiment [19]. Also, $\tilde{C}$ can have a valley, if the reverse inequality is fulfilled and it was observed in [21]. The dependence of $\tilde{C}$ on L qualitatively correlates with the numerical calculations [22] in spite of the fact that the approach used there inaccurately describes the redistribution of charges in RTD with external voltage.

Secondly, *the region of exit from resonance,* J^0_{RTD} drops down here, this is the region of the negative differential conductance (NDC) and the central arm of Z-type I-V curve. $\tau_{resp} > \tau_{dwell}$ in the region of NDC, as it follows from (11), with τ_{resp} the more, the more NDC is and $\tau_{resp} \to \infty$ when $G^0_{RTD} \to -\infty$. E.i. "good" RTDs with large NDC are principally slow. One have to choose "bad" RTDs for high-frequency applications. As follows from the analysis of the static I-V curve (1,3,8) and (10), $\tau_{resp} < 0$ in the region of the central arm of Z-type I-V curve, that corresponds to the instability of the region.

Our model easily explains the capacitance peak in the NDC region [9], [19], [21]-[23], to name a few Refs. It follows from (11) and (14) that $\tilde{C} \to \infty$ when $G^0_{RTD} \to -\infty$, but, generally speaking, the peak does not coincide with that neither in NDC nor in current.

Although all the results of the present work are obtained in the sequential tunneling approximation [12], the Coulomb interaction should lead to the similar effect in the coherent tunneling model. The assumption of the homogeneous current distribution ceases to be true at high frequencies in the RTDs with large diameters. In the case, the skin-effect can lead to the excitation of the junction polaritons [24]. Also, the assumption is not valid in the region of the central arm of Z-type I-V curve in the structures with large diameters or very thin

barriers [25].

VII. Conclusions

We have demonstrated that:

• The response time of RTD is smaller and much smaller than the electron dwell time in the quantum well in the positive differential conductance region (except the central arm of Z-type I-V curve). In the high-quality structures with 2D→2D tunneling τ_{resp} can be by the orders of magnitude less than τ_{dwell}.

• RTD is principally slow device in the negative differential conductance region, i.e. $\tau_{resp} > \tau_{dwell}$ and $\tau_{resp} \to \infty$ when $G^0_{RTD} \to -\infty$.

A simple analytical expression has been derived that relates τ_{resp} to the static differential conductance (11). Also, a simple and comprehensive analytical expression has been derived for the RTD impedance (12). In the low-frequency limit it describes the special features in the RTD capacitance.

Acknowledgments

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SOI MOSFET Scaling and Innovative Solutions

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Silicon On Insulator (SOI) technology was originally developed for the niche of radiation-hard circuits. Three decades of continuous improvement in material quality, device physics, and technology allowed SOI to enter the microelectronics roadmap. The attractiveness of SOI circuits, on the commercial market, comes from their superior capabilities in terms of performance (higher speed, lower power/voltage) and scalability.

The aim of this talk is to provide a synthetic view of the present status and the future developments of SOI technologies and devices. The family of SOI devices includes state-of-the-art circuits for mainstream applications, low-power/low-voltage and high-frequency (RF) components, high-temperature CMOS, high-voltage devices, and various sensors. In this context, SOI has many assets but also peculiar constrains which will be discussed.

The operation of partially-depleted SOI MOSFETs reveals special SOI mechanisms: floating body, parasitic bipolar action, drain current transients, and self-heating. On the other hand, fully-depleted SOI transistors (Fig. 1a) are governed by interface coupling effects. The main transistor parameters (threshold voltage, transconductance, subthreshold swing and leakage current) show considerable variations with both the back gate biasing and the quality of the interface between film and buried oxide.

On the prospective side, it is admitted that SOI is capable to expand the limits of bulk-silicon technology. It is even speculated that SOI transistors will be the unique survivors of the CMOS world. Indeed, SOI is more versatile than bulk Si because there are additional parameters (film thickness, nature and thickness of the buried oxide, doping in the underlying substrate, back gate biasing, etc) to use for optimized scaling.

As for the 'evolutionary' trend, we will discuss the typical SOI rules for MOSFET shrinking as well as the design windows for further generations of fully- and partially-depleted SOI circuits. The film doping and thickness are the main ingredients for the scalability of conventional single-gate SOI MOSFET. The thinning of the buried oxide allows relaxing the design constraints. Even more flexibility is achieved by using mid-gap metal gates and topological variants such as elevated source and drain terminals. Critical aspects, including the large series resistance in ultra-thin films, the control of the film thickness, the fringing fields in the gate oxide, buried oxide, and underlying silicon substrate, have still to be examined.

There are also 'revolutionary' aspects. SOI offers new exciting solutions for sub–0.1 μm fully-depleted transistors:

Ground-plane SOI MOSFET. Numerical simulations indicate that a ground plane can drastically attenuate the supplementary drain-induced barrier lowering (DIBL) caused by the fringing fields within and underneath the buried oxide. A ground-plane may be located at the bottom interface of the film (Fig. 1b) or just below the buried oxide (Figs. 1c,e). Several possibilities are examined: thin (Fig. 1c) or thick (Fig. 1e) buried oxides with a ground plane consisting of a degenerated Si layer or a metal layer, replacement of the buried oxide by air, etc.

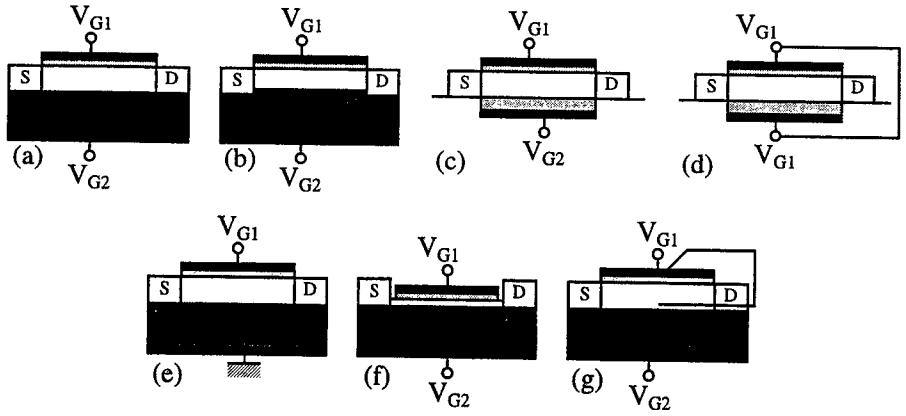


Figure 1: *Possible architectures for ultimate SOI MOSFETs: (a) fully depleted, (b) pulsed doping, (c) field plate, (d) double (surround) gate, (e) ground plane, (f) ultra thin, (g) dynamic threshold transistors.*

Extremely thin SOI MOSFET. Although the normal device thickness is considered to be in the range 20–50 nm, the current technology is already capable of producing much thinner (1–5 nm) transistors, where the MOS gene is maintained by just a few (1-4) monolayers of silicon (Fig. 1f). Thickness-related effects on the carrier mobility, threshold voltage, and subthreshold swing are discussed based on experimental data. The coupling of Poisson and Schrödinger equations indicates that the carrier confinement is dominated by quantum effects. Preliminary experiments in a fascinating 1 nm thick transistor show that the $I_D(V_G)$ characteristics are still MOS–like and well behaved.

Double-gate SOI MOSFET. These transistors have either two gates biased simultaneously or one surrounded gate (Fig. 1d). They take advantage of the concept of *volume inversion* which offers additional current, enhanced transconductance, and attenuated short-channel effects. Based on quantum considerations, we will discuss the features and advantages resulting from volume inversion as compared to single-gate transistors. The key aspect is that most electrons flow in the middle of the film, where the electric field is low and the electron scattering on the surface roughness is less frequent. The practical manufacturability of this structure is also examined.

Dynamic-threshold SOI MOSFET. This device has the transistor body internally connected to the gate or to the drain (Fig. 1g). A nearly ideal coupling develops between the gate voltage and the channel for the benefit of fast, low-voltage integrated circuits. A simple compact model allows anticipating the performance and parameters of DT–MOSFETs.

The discussion of the above structures is documented by simulation results, physics-based models, and measurements.

However, before achieving such challenging, extreme SOI devices, serious problems subsist in several domains (technology, device physics, modeling, and circuit design) and require a substantial amount of technical effort. Even more important, for SOI to become a major player in the commercial arena, is the strategic support needed to overcome the bulk-Si despotism.

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Characterization of Floating Body Thin Film Silicon-on-Insulator MOSFETs for Analog and RF Circuit Applications

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Abstract

Over the past decade, CMOS built on Silicon-On-Insulator technology has been matured not only due to the achievement of better quality starting SOI substrates with a lower production cost, but also to the improvement of SOI integration processes. With the inherent advantages in SOI CMOS technology, minimizing DC and switching floating body effects have enabled IBM to implement high speed digital frameworks, such as the low voltage 650MHz 64b PowerPC microprocessor with more than a 25% improvement over bulk silicon CMOS design. Currently, there is a need for a more comprehensive understanding of AC characteristics on SOI CMOS technology for coming mixed-mode baseband and RF (radio frequency) applications. The objective of this paper is to present a study of unique AC floating body effects and the resultant low-frequency noise overshoot phenomenon in SOI CMOS technology. Further study of their impact on the RF arena will also be discussed.

AC Floating Body Effects

In the case of analog circuits, the requirements of transistor characteristics are different from those of digital-only applications. Low noise, high g_m, low parasitic capacitances, and high output resistance are important. These are some of the potential advantages that thin film SOI CMOS can offer. The major difference between bulk MOSFETs and SOI devices is the floating body effect. In DC or steady state, the body voltage can be expressed as,

$$I_R \cdot (e^{V_{SB} \Leftrightarrow nV_T} - 1) = I_G + I_{ii} \tag{1}$$

In case of AC, the frequency dependence of small-signal body voltage can be expressed as [1]

$$v_{SB}^{\div}(AC) = \frac{r_{SB}}{1 + j(2\pi f \cdot r_{SB}C_{BB})} \leftrightarrow I_{SB}^{\div} \quad \text{And} \quad r_{SB} = \frac{nV_T}{I_{SB} + I_R} \cong \frac{nV_T}{I_{ii}} \tag{2}$$

Alternatively, the output conductance is therefore given by

$$G_{DS}(f) = G_{DS}(bulk) + \frac{G_{DS}(kink)}{[\sqrt{1 + (f \Leftrightarrow f_{kink})^2}]^{1+\eta}} + G_{DS}(bipolar) \tag{3}$$

Fig. 1 shows the drain voltage dependence of the output conductance. In order to suppress the AC kink effects, either FD depleted SOI MOSFETs or PD MOSFETs with body tie can be used. However, as Fig. 2 shows, FD MOSFETs still show mild AC kink. In the case of body-tie devices, the 3-D body discharge network is complicated. A non-ideal body tie device can have problematic AC behavior as shown in Fig. 3. The mechanism behind it has been contributing to the frequency dependence of small-signal body voltage, which is linked to body discharge network, including longitudinal source/body junction, lateral resistive body contact, and the extra edge components. In the floating body configuration, even though the source/ body junction is only discharge path, an

increase of junction leakage current (I_R), by using proper source/body junction engineer or shifting towards more fully-depleted mode, can significantly affect the device AC characteristics.

One major consequence of the AC kink effects is the linearity of SOI circuits. Fig. 4 shows the total harmonic distortion (*THD*) of a good body-tied (BT) SOI amplifier, a PD SOI amplifier and a bulk 0.5μm amplifier with small output swing. The output resistance (r_0) decreases as drain bias reduces (inset of Fig. 4) and increases the distortion at the low drain biases, which is a major concern for low-voltage applications [2]. Not only does a good body-tied SOI device provide similar linearity to bulk devices for small signal behavior, but they also demonstrate comparable large signal distortion behavior for low or high voltage applications.

Low Frequency Noise Characteristics

Low frequency noise is important for many RF and analog circuits such as PLL. Fig. 5 shows the 1/f noise of a good body-tie device. Although good body-tied SOI nMOS can provide a comparable flicker noise property with that of bulk silicon MOSFETs, it also comes with a larger device size (especially for the actual gate area) and increased parasitic capacitance. In the case of PD floating body SOI nMOSFETs, a kink-related Lorentzian-like noise overshoot is observed as shown in Fig. 6 [3]. This noise spectrum consists of a Lorentzian-like noise (characterized by a flat plateau followed by a $1/f^2$ roll-off at the corner frequency f_0) and a 1/f noise and can be expressed as,

$$S_{VG} = \frac{K_F}{C_{ox}^2 WL \cdot f} + K_2(V_{DS}) \cdot \frac{1}{1+(f/f_0(V_{DS}))^2} \tag{4}$$

Fig . 7 Shows that the noise overshoot is closely related to the AC kink effects. the mechanism behind post-kink Lorentzian-like noise overshoot can be explain using small-signal frequency dependence of body effect as follows.

$$f_{I_D} = \frac{f_{I_D}}{f_{V_{TH}}} \cdot \frac{f_{V_{TH}}}{f_{V_{BS}}} \cdot \frac{f_{V_{BS}}}{f_{I_{SB}}} \cdot f_{I_{SB}} = g_m \cdot \beta \cdot \frac{r_{SB}}{1+j(f/f_0)} \cdot f_{I_{SB}} \tag{5}$$

Therefore, the excess carriers in the body, generated by impact ionization current, discharge through the S/B junction resulting in a shot noise $2qI_{SB}$ where $I_{SB}= I_{ii}$. In addition, impact ionization current also induces the shot noise with a magnitude of $2qI_{ii}$ due to the fact that only the carriers with enough energy can generate electron-hole pairs. More importantly, they are uncorrelated shot noises. Therefore, these current fluctuations perturb the body voltage through the square of the body impedance with Lorentzian-like shape as follows [4].

$$S_{V,body} = S_{I,body} \cdot |Z_{Body}|^2 = 4qI_{ii} \cdot \frac{1}{1+(f/f_0)^2} \cdot \frac{(nV_T)^2}{I_{ii}^2} \tag{6}$$

The magnitude of shot noises themselves is negligible compared with the existing noise. But, the high impedance of S/B junction significantly amplifies their magnitude. Finally, they affect front channel conducting carriers by introducing Lorentzian-like excess noise as follows,

$$S_{ID,excess} = 4q(nV_T)^2 \frac{1}{1+(f/f_0)^2} \cdot \frac{1}{I_{ii}} \cdot g_m^2 \cdot \beta^2 \tag{7}$$

where $I_{SB}= I_{ii}$ and $f_0 = f_{kink} = 1/(2\pi r_{SB} C_{BB})$

In the case of FD MOSFETs, similar noise overshoot is observed (Fig. 8). In this case, the body-source junction has a smaller diffusion barrier, and the effective reversed saturation current of the junction I_R needs to be considered. As the operation mode shifts from PD towards more fully-depleted operation, the reduced S/B junction barrier exponentially increases resulting in a significant decrease of S/B junction impedance. Therefore, this factor has to be included in the excess noise model with a modification of

$$r'_{SB} = \frac{nV_T}{I_{SB} + I_R} \quad \text{As}$$

$$S_{ID,\,excess} = 4qI_{ii} \cdot \frac{1}{1 + \left(\frac{f}{f_0} \cdot \frac{I_{ii}}{I_R + I_{ii}}\right)^2} \cdot \frac{(nV_T)^2}{(I_R + I_{ii})^2} \cdot g_m^2 \cdot \beta^2 = 4q(nV_T)^2 \frac{1}{1 + (f/f_0)^2} \cdot \frac{I_{ii}}{(I_R + I_{ii})^2} \cdot g_m^2 \cdot \beta^2 \quad (8)$$

where $f'_0 = 1/(2\pi r'_{SB} C_{BB}) \propto I_{ii} + I_R$

Summary

In summary, the AC characteristics (especially, output conductance) in SOI MOSFETs have been presented. Floating body effects not only introduce a kink on G_{DS} but also result in a unique frequency-dependent feature — the AC kink effect. While fully-depleted operation and the body contact technique have been suggested to suppress DC floating body effects, there still exists a residual AC kink phenomenon at larger drain bias. Floating body induced kink or deviation on G_{DS} significantly degrades the circuit performance. More importantly, the sensitivity of 3rd order harmonic distortion on G_{DS} limits the use of FD device or body-tied devices with finite body resistance for large dynamic range applications.

With a good body contact, CMOS built on SOI substrates demonstrate a pure noise below 100kHz regardless of body contact technology. More importantly, it is comparable with the flicker noise level in current bulk CMOS technologies. In the floating body configuration, there exists Lorentzian-like excess noise spectrum as the devices are biased in the post-DC kink region. As floating body effect is suppressed (from PD to FD modes), the excess noise is also suppressed in the lower frequency range. However, the similar excess noise phenomena still exists at higher frequencies. In addition, the corner frequency of the excess noise is correlated to the AC kink effect regardless of device parameters and floating body effects, suggesting that the physics behind the excess noise is related to the AC characteristics of the source/body junction. Thus, the key device parameters are S/B junction saturation currentand the impact ionization current which determine the excess noise characteristics as the device is biased near DC kink onset voltage. In RF applications, the upconversion of Lorentzian-like excess noise degrades the phase noise characteristics in PD floating body SOI oscillators. It is necessary to suppress the low-frequency noise in SOI MOSFET technologies for future mixed-mode/RF analog applications.

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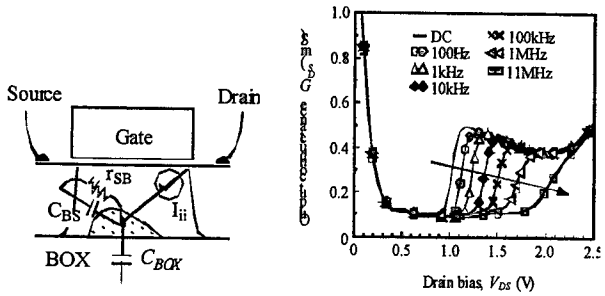


Fig. 1 (a) Schematic diagram of key elements inside SOI floating body and the relevant small-signal equations. (b) Output conductance versus drain bias of a PD floating body SOI nMOSFET biased at V_{GT} = 0.2 V with L = 0.45 μm for different frequencies.

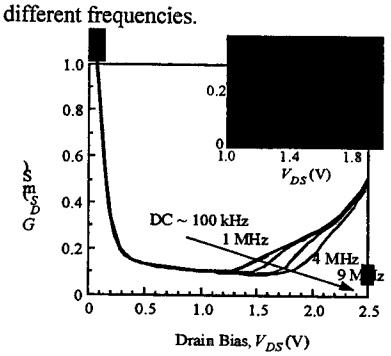


Fig. 2 Output conductance versus drain bias of a FD floating body SOI nMOSFET biased at V_{GT} = 0.2 V with L = 0.45 μm for different frequencies. The inset shows the zoom-in AC G_{DS}.

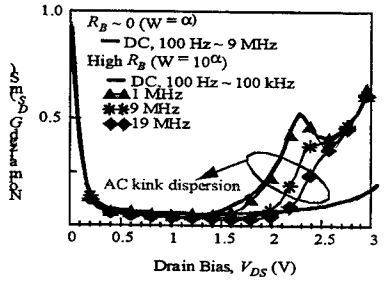


Fig.3 Output conductance versus drain bias of two H-gate body-grounded SOI MOSFETs biased at V_{GT} = 0.2 V with L = 0.45 μm with negligible and high body resistance.

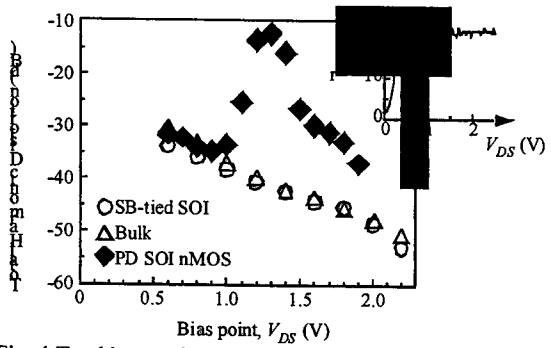


Fig. 4 Total harmonic distortion of a bulk, a SB-tied, and a PD floating body SOI nMOS amplifiers as a function of V_{DS} with 0.4 V output swing with 1kHz test signal. The inset shows the V_{DS} dependence of output resistance of SB-tied SOI nMOS.

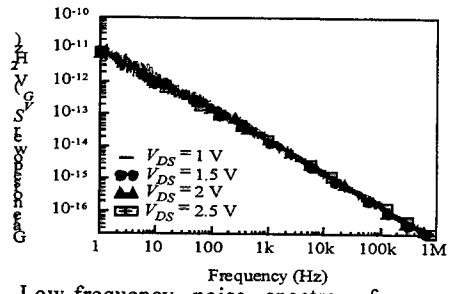


Fig. 5 Low-frequency noise spectra of a good source/body-tied SOI nMOS (w/ 10 fingers) for different drain biases biased at V_{GT} = 0.2 V with L = 0.45 μm.

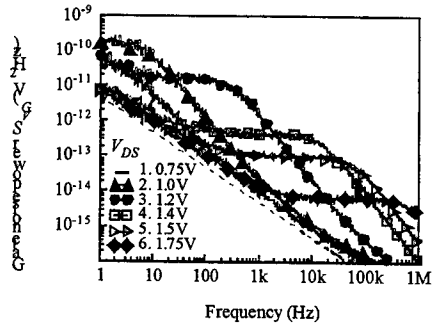


Fig. 6 Equivalent input-referred gate noise power spectrum versus frequency for a PD floating body SOI nMOSFET biased at V_{GT} = 0.2 V with L = 0.45 μm.

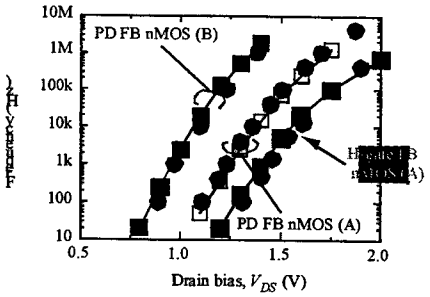


Fig. 7 Empirical correlation of the noise overshoot (corner frequency, f_0) and AC kink effect (f_{kink}) of floating body SOI MOSFETs

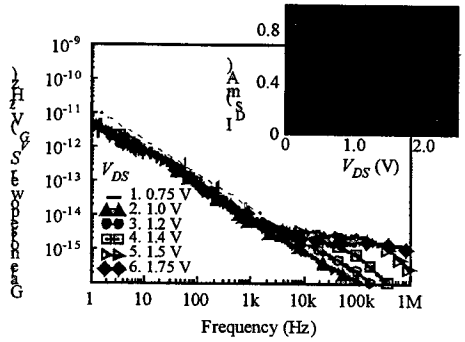


Fig. 8 Equivalent input-referred gate noise power spectrum versus frequency for a FD floating body SOI nMOSFET biased at V_{GT} = 0.2 V with L = 0.45 μm: arrows indicate the location of the corner frequency f_0.

EXTENDED CHARGES MODELING FOR DEEP SUBMICRON CMOS

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Abstract - **The simulation of deep submicron CMOS circuits operating at high-frequency requires adequate models representing the dynamic behavior of the transistors. Charges in the device are affected by carrier quantization and polydepletion in the gate. Velocity saturation is one of the short-channel effects that further affect the charges. An analytical MOS transistor (MOST) model for circuit simulation which includes the above effects is described. The charges/transcapacitances expressions show good qualitative behavior at all inversion levels from weak to moderate and strong inversion and have correct asymptotic behavior. The model agrees well with characteristics obtained from 2D device simulation and measured on deep submicron CMOS technology.**

1. Introduction

Modeling of charges and transcapacitances for deep submicron CMOS technologies is an increasingly challenging task. The use of thin gate oxides, high levels of channel dopant concentration, and polysilicon gates leads to increased influence of quantum effects (QM) (e.g. [1][2]) and polysilicon gate depletion (PD) (e.g. [3]). All device characteristics are affected, in particular the charges/transcapacitances. Short-channel devices are further affected by the two-dimensional nature of fields, leading to velocity saturation among other short-channel effects. Currently available analytical MOST models have some difficulty to represent such effects in a qualitatively correct way. An alternative approach using numerical MOST models may offer increased accuracy but has to deal with the difficulty of numerical iteration.

The modeling approach proposed here is based on an accurate evaluation of charges present in the MOS structure at all inversion levels, following the 'EKV' approach [4]-[6] extended to a charge-based model [7]-[11]. The charges model is extended to account for velocity saturation and channel length modulation. First-order models are proposed to account for QM and PD effects. The compact MOST model obtained satisfies the most important criteria for MOST models, among which are correct asymptotic behavior, smooth conductances and transcapacitances in all operating regions. The model further uses a small number of parameters closely related to the underlying physics.

The increasingly important influence of parasitic elements such as fringing and overlap capacitances and junction space charge regions (e.g. [13]) will be addressed elsewhere.

2. Charge-based modeling

The basic charge-sheet model for the drain current and the charges in the MOST will be established as simple functions of physical parameters and terminal voltages. The drain current of the MOST can be expressed according to [4]-[6],

$$I_D = I_S \cdot (i_f - i_r) \qquad I_S \cong 2nU_T^2 \mu C'_{ox} \frac{W}{L}$$

$$i_{f(r)} = F\left(\frac{V_P - V_{S(D)}}{U_T}\right) \tag{1}$$

$$V_P \cong \frac{V_G - V_{TO}}{n} \qquad n \cong 1 + \frac{\gamma}{2\sqrt{\Psi_0 + V_P}}$$

where I_S is the *specific current*, used as a normalization factor for the drain current, depending on the *slope factor* n, the mobility μ, and the effective device dimensions W and L. The slope factor n is in turn expressed as a function of the *pinch-off voltage* V_P depending on the gate voltage V_G. The *forward (reverse) normalized currents* $i_{f(r)}$ are the fundamental variables in this modeling approach [4]. They are symmetric in terms of source(drain) voltages $V_P - V_{S(D)}$. Note that all voltages are referred to the substrate; U_T is used to normalize voltages. The function F links the normalized variables i and υ; its asymptotes are $F(\upsilon) = (\upsilon/2)^2$ in strong inversion and $F(\upsilon) = \exp(\upsilon)$ in weak inversion [4]. Parameters in (1) are defined as,

$$V_{TO} = V_{FB} + \Psi_0 + \gamma\sqrt{\Psi_0} \qquad \Psi_0 \cong 2U_T \ln\left(\frac{N_{sub}}{n_i}\right)$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C'_{ox}} \qquad C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad U_T = \frac{kT}{q} \tag{2}$$

where undefined symbols have conventional meaning.

The current transport equation $I = \mu W \cdot [-Q_i' \cdot d\Psi_s/dx + U_T \cdot dQ_i'/dx]$ includes drift and diffusion in terms of inversion charge density Q_i' and surface potential Ψ_s at each coordinate x along the channel. Introducing the normalized channel current $i = I/I_S$, the channel potential $\upsilon = V/U_T$, and linearizing the inversion charge $dQ_i' \approx n \cdot C'_{ox} \cdot d\Psi_s$ [7], Q_i' can be expressed as a function of i [8][10],

$$Q_i' = -2nU_T C'_{ox}\left(\sqrt{\frac{1}{4} + i} - \frac{1}{2}\right) \tag{3}$$

Using the relationship between channel conductance and inversion charge, $dI/dV = \mu Q_i' W/L$ [4], a differential equation is obtained, linking the normalized quantities i and υ,

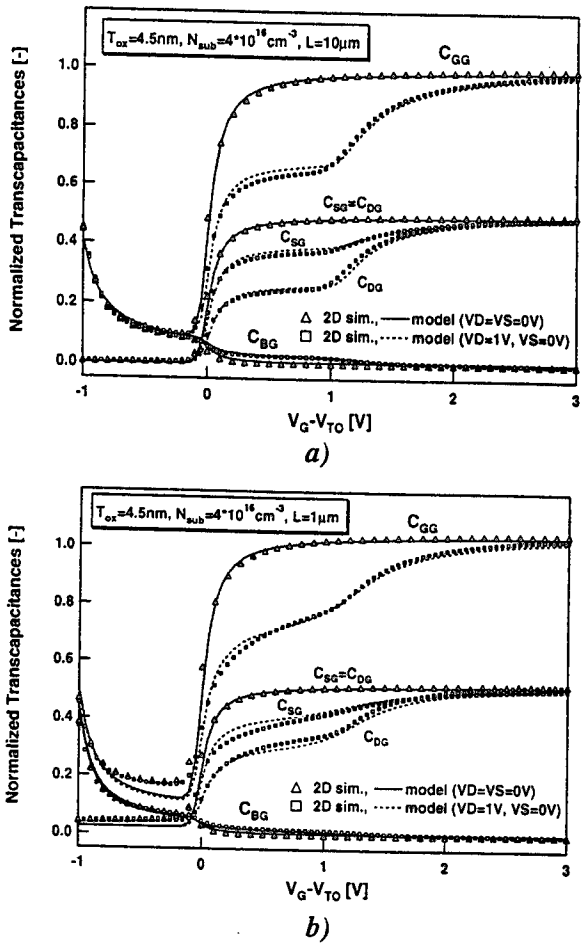


Fig. 1: *Transcapacitances, normalized to WLC'_{ox}, versus $V_G - V_{TO}$, at low and high drain voltage, for an n-channel device, a) long-channel, b) intermediate channel length. 2D device simulation (markers); model (dashed, lines).*

$$\frac{di}{d\upsilon} = \frac{1}{2} - \sqrt{\frac{1}{4}+i} = i \cdot G(i). \tag{4}$$

In (4), $G(i)$ is the normalized transconductance-to-current ratio [4][10], corresponding to $G(i_f) = g_{ms}U_T/I_D$ in saturation [4], where $g_{ms} \equiv -\partial I_D/\partial V_S$. The function $G(i_f)$ shows an excellent agreement with a numerical solution of the Poisson and Gauss equations as well as with measurements at all inversion levels over several technologies [10][11]. Integrating (4) and determining the integration constant from strong inversion conditions yields the relationship $\upsilon_P - \upsilon = F^{-1}(i)$ [8][10],

$$\upsilon_P - \upsilon = 2\left(\sqrt{\frac{1}{4}+i} - \frac{1}{2}\right) + \ln\left(\sqrt{\frac{1}{4}+i} - \frac{1}{2}\right) \tag{5}$$

An approximate analytical expression can be used to invert (5) without deteriorating the accuracy of the model [9].

The drain current (1) can now be expressed in terms of the terminal voltages, at all inversion levels from weak to strong inversion and from non-saturation to saturation. It is further adapted to include field-dependent mobility μ [10]. A velocity saturated region forms near the drain when carriers reach their saturated velocity [12]. The channel is divided in two parts, a first one of length $L - \Delta L$, where the gradual channel approximation (GCA) used so far does hold, and the velocity saturated part of length ΔL. At the transition point, an effective drain voltage V_{Dsat} is reached, replacing V_D in (1) resulting in the corresponding reverse current i_r' [9].

The total charges in the device can be obtained by integrating the charge densities along the channel, leading to the charges model [7]-[11]. The effect of velocity saturation on the charges will also be considered here by integrating the charges according to the two regions, assuming a constant inversion charge density in the velocity-saturated part (e.g. [14]). The inversion charge is integrated, using $dx = -(L-\Delta L)\cdot di/(i_f - i_r')$,

$$Q_I = \frac{1}{LC'_{ox}} \cdot \left[\int_0^{L-\Delta L} Q_i' dx + Q_i'|_{(x=L-\Delta L)} \cdot \int_{L-\Delta L}^{L} dx \right]$$

$$= -2nU_T \cdot \left[\frac{L-\Delta L}{L} \cdot \left(\frac{2}{3} \cdot \frac{\chi_f^2 + \chi_f\chi_r' + \chi_r'^2}{\chi_f + \chi_r'} - \frac{1}{2} \right) + \frac{\Delta L}{L} \cdot \left(\chi_r' - \frac{1}{2} \right) \right] \tag{6}$$

where $\chi_{f(r')} = \sqrt{1/4 + i_{f(r')}}$ is an auxiliary variable.

To obtain the drain and source charges, the inversion charge is partitioned linearly [15] among source and drain when integrating the inversion charge density;

$$Q_D = \frac{1}{LC'_{ox}} \cdot \left[\int_0^{L-\Delta L} \frac{x}{L} Q_i' dx + Q_i'|_{(x=L-\Delta L)} \cdot \int_{L-\Delta L}^{L} \frac{x}{L} dx \right]$$

$$= -nU_T \left[\frac{L-\Delta L}{L} \left(\frac{3\chi_r'^3 + 6\chi_r'^2\chi_f + 4\chi_r'\chi_f^2 + 2\chi_f^3}{(\chi_f + \chi_r')^2} - \frac{1}{2} \right) + \frac{\Delta L}{L} \cdot \left(2 - \frac{\Delta L}{L} \right) \cdot \left(\chi_r' - \frac{1}{2} \right) \right] \tag{7}$$

$$Q_S = Q_I - Q_D \tag{8}$$

The depletion charge expression is obtained through its linearization around $Q_i' = 0$ [4],

$$Q_B \cong -\gamma\sqrt{\Psi_0 + V_P} - \frac{n-1}{n} Q_I, \tag{9}$$

and the gate charge balances all other charges,

$$Q_G = -Q_B - Q_I - Q_{ox}, \tag{10}$$

where Q_{ox} is a fixed oxide charge per unit area. Note that all charges have been normalized to WLC'_{ox}.

All node charges have now been obtained through integration along the channel. Their derivatives yield the (trans-)capacitances $C_{XY} \equiv \delta(\partial Q_X/\partial V_Y)$, where $\delta = 1$ if $X = Y$ and $\delta = -1$ otherwise. In Fig. 1 some of the model's transcapacitances are compared to 2D device simulation, both for a long-channel device and a device with intermediate channel length. Correct

asymptotic behavior and good quantitative agreement in all operating regions can be observed.

The model expressions have been used as stated above, combined with charge-sharing for short-channel [9]; a slightly corrected expression for the slope factor for improved asymptotic behavior of the transcapacitances has been used. A single parameter set is used for all simulated characteristics, and the model parameters match closely those underlying the 2D simulation. Note that the model at this point requires only the five long-channel parameters μ, C'_{ox}, V_{TO}, γ and Ψ_0 (or equivalently t_{ox}, V_{FB}, and N_{sub}), and three short-channel parameters related to velocity saturation/channel length modulation and charge-sharing, to calculate the drain current, charges and transcapacitances in all operating regions and from long-channel to short-channel.

The shorter-channel device shows velocity saturation effects in strong inversion; only bias-independent fringing capacitances have been accounted for in the model. In depletion, the influence of the bias-dependent overlap and space-charge capacitances (not included in the model) can already clearly be seen. These capacitances terms become increasingly important with shorter channel lengths and will be addressed elsewhere.

3. Quantum effects and polysilicon depletion

In the following, first-order expressions for QM and PD effects will be introduced into the basic charge-sheet model. A field-dependent expression for the band-gap widening due to quantization of electron energy levels is obtained in [1] and used e.g. in [2] in the context of a surface-potential based model,

$$\Delta E_g = \frac{13}{9} \cdot \kappa \cdot \left[\frac{\varepsilon_{si}}{4kT}\right]^{1/3} \cdot E_\perp^{2/3} \qquad (11)$$

where the effective vertical field is defined as $E_\perp = |Q'_B + \eta Q'_i|/\varepsilon_{si}$ [16]; and $\kappa = 4.1 \cdot 10^{-10}\ eVm$. ΔE_g corresponds to the energy shift (with respect to the Si conduction band minima) of the lower 2D state of the quantum well near the SiO_2/Si interface. This effect is considered here as an energy shift of the conduction band minima with respect to the bulk Fermi level, and the MOST will still be treated within the charge-sheet approach. Under this assumption, ΔE_g leads to a modified intrinsic carrier concentration [1], $n_i^{qm} = n_i \cdot \exp(-\Delta E_g/2kT)$, which can be considered as a shift in the conduction band bending corresponding no longer to Ψ_0 but to $\Psi_0^{qm} = \Psi_0 + \Delta\Psi_0$, where $\Delta\Psi_0 = \Delta E_g/q$. In terms of threshold voltage change, the following expression is obtained,

$$\Delta V_{TO}^{qm} = \Delta\Psi_0 + \gamma \cdot (\sqrt{\Psi_0^{qm}} - \sqrt{\Psi_0}) \approx \sigma_{qm} \cdot \Delta\Psi_0 \cdot n_0 \qquad (12)$$

where $n_0 = 1 + \gamma/(2\sqrt{\Psi_0})$ results from a first-order development of the term $\sqrt{\Psi_0^{qm}}$, and $0 \le \sigma_{qm} \le 1$ is a model parameter allowing to adjust the QM effect. The

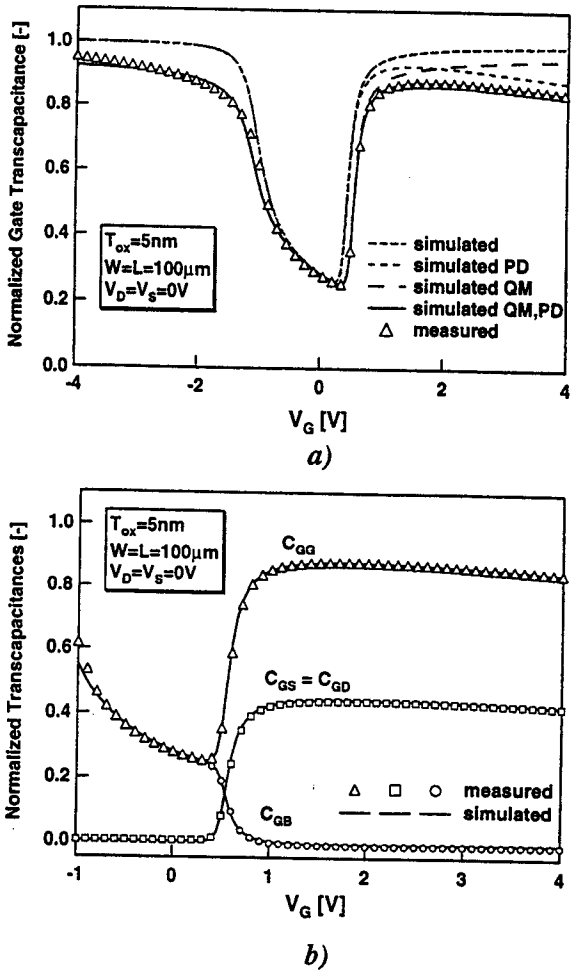


Fig. 2: *Transcapacitances normalized to WLC'_{ox}, measured (markers) from a large-area n-channel device of a 0.25µm CMOS technology, versus V_G at $V_D = V_S = 0V$. a) model corresponding to the basic charge model, without contribution of QM and PD effects individually (dashed) and cumulated (line). b) model (lines) with both QM and PD effects.*

charge-sheet model will now use the corrected threshold voltage $V_{TO}^{qm} = V_{FB} + \Psi_0 + \gamma\sqrt{\Psi_0} + \Delta V_{TO}^{qm}$. The model is first calculated using the bias-independent equivalent of $\Delta\Psi_0$ evaluated at $E_\perp^0 = \gamma C'_{ox}\sqrt{\Psi_0}/\varepsilon_{si}$, leading to

$$\Delta V_{TO}^{qm,0} \approx \sigma_{qm} \cdot n_0 \cdot \frac{13}{9} \cdot \kappa \cdot \left[\frac{\varepsilon_{si}}{4kT}\right]^{1/3} \cdot [E_\perp^0]^{2/3}. \qquad (13)$$

Following the first evaluation, the model is recalculated using the bias-dependent ΔV_{TO}^{qm}.

Successive approximations have been made until here, however justified considering that the slope factor n remains a slowly varying function of the gate voltage. As will be seen, the accuracy of the approximations is acceptable. Expression (13) may serve to evaluate the scaling trend in threshold voltage in terms of oxide thickness t_{ox} and substrate doping concentration N_{sub}.

The QM effect leads to a change in threshold volt-

age as discussed. Mobility is reduced in strong inversion, and the weak inversion slope of drain current is degraded. Further the total gate capacitance is severely reduced, both in inversion and accumulation.

In dual polysilicon gate technologies, the gates are implanted simultaneously with the source/drain regions (n-channel with n^+ poly, p-channel with p^+ poly). Insufficient active doping concentration in the poly gate leads to the formation of depletion layer causing a voltage drop in the gate, when the device is in inversion. Degradation of device characteristics becomes more severe when using thinner oxides.

The polydepletion effect will be modeled supposing uniform doping concentration in the gate and complete depletion [3]. The voltage drop in the gate can be readily expressed in terms of the gate charge,

$$\Delta V_G = \frac{q \cdot N_{poly}}{2\varepsilon_{si}} x_d^2 = \frac{q \cdot N_{poly}}{2\varepsilon_{si}} \left[\frac{C'_{ox} \cdot Q_G}{q \cdot N_{poly}} \right]^2 = \frac{Q_G^2}{\gamma_{poly}^2} \quad (14)$$

where x_d is the depletion layer width depending on the gate charge, and $\gamma_{poly} = \sqrt{2q\varepsilon_{si}N_{poly}}/C'_{ox}$ is the 'gate factor' depending on the polysilicon doping concentration N_{poly}. The effective gate voltage is then expressed as $V_{Geff} = V_G - \Delta V_G$. The gate charge Q_G (10) is first evaluated using the initial estimate $\Delta V_G^0 = (\gamma^2/\gamma_{poly}^2)\Psi_0$. The term ΔV_G^0 corresponds to the threshold voltage shift due to the PD effect (showing that PD is essentially dependent on the ratio of substrate to poly doping concentrations). Then the full model accounting for the bias-dependency of ΔV_G is calculated. To account for the approximation made when evaluating the gate charge, γ_{poly} (or equivalently N_{poly}) is considered as a fitting parameter.

The total gate capacitance of an n-channel device of a standard $0.25\mu m$ CMOS technology from accumulation to strong inversion is shown in Fig. 2 a). The simulated curves correspond to the charge sheet model, including QM and PD effects individually, and the final result including both contributions. The value of the gate capacitance corresponds to the physical oxide thickness. In accumulation, the slight discrepancies observed stem from the use of a rather simple charge expression, which does not compromise the validity of the present approach. In Fig. 2 b), other transcapacitances for the same device show excellent agreement between measurement and simulation from depletion to strong inversion.

The model developed is consistently based on the evaluation of charges within the channel and the gate of the MOS structure. The simple models for both PD and QM effects are approximate, and are therefore of limited validity. Nevertheless they allow to model the bias-dependency of the effects quite well, and make use of the correct physical device parameters. The full model can be used at all inversion levels with present deep submicron CMOS technology.

4. Conclusions

Polydepletion and quantization effects have an increasingly strong impact on all device characteristics of deep submicron CMOS devices with thin gate oxides and high substrate doping. An analytical compact MOST model, based on a charge-sheet modeling approach, including velocity saturation, polydepletion and quantum effects, has been presented. The model is valid at all inversion levels from weak through moderate and to strong inversion, and shows correct asymptotic behavior and smooth and qualitatively correct transition regions. Good agreement with 2D device simulation as well as with measured characteristics from deep submicron CMOS technology has been shown. The model is efficient in terms of computation and uses a small set of physical parameters, making it adequate for deep submicron CMOS circuit simulation. Model extensions, in particular for fringing capacitances, are the object of further work.

Acknowledgment

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Source Side P^+ Channel Implant Significantly Improves NMOSFET Performance

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I. Introduction

Short channel effects have become dominant as device dimensions shrink into the nanoscale region. To compensate these effects some researchers have proposed asymmetric MOSFET structures[2]-[7]. In this work we demonstrate that many detrimental short channel effects can be significantly improved by placing a narrow p^+ implant in the source side of an n-channel MOSFET. Previous work has shown that such an implant can improve channel length modulation effects as well as stabilize the threshold voltage. By applying precise device modeling we have found that an asymmetrical implant near the source end of the channel can improve drain-induced barrier lowering (DIBL), improve noise margins, reduce substrate current and increase the breakdown voltage. After first finding that such channel engineering can indeed improve the performance of deep submicron devices, we used detailed device modeling to help ascertain the optimal location of such an implant.

II. Device Design and Results

We performed our study on a $0.25\mu m$ device developed in industry. The structure and doping profile of the implanted device are shown in Fig. 1(a) and (b). To study the device performance, we simulated the device with a state-of-the-art two-dimensional(2-D) device simulator that goes beyond conventional modeling by solving the Boltzmann transport equation. This approach is especially useful for calculating short channel effects, including velocity overshoot and low breakdown voltage[8]. Where applicable, we also used more conventional simulators based on the drift-diffusion method. We study five different device structures. One conventional NMOSFET with no channel implant, and four with implants at different strategic implant locations (SIL). The SIL is the distance from the left side of the implant to the edge of the source.

We define the following five devices: a-no implant, b-SIL=0.0 μm(adjacent to source side), c-SIL=0.05 μm, d-SIL=0.10 μm and e-SIL=0.15μm(adjacent to drain side).

A. Noise Margins and Early Voltage($1/\lambda$)

By implanting the device in the correct location, the device characteristics can improve by giving rise to a larger Early voltage magnitude and improved current source characteristics. These characteristics yield larger gain in analog applications and improved noise margins for digital circuits. The I-V characteristics resulting from implanting the five different devices are given in Fig. 2, with device b (implant adjacent to source: $SIL = 0$) showing best Early voltage characteristics. The slope in the saturation region of device b is the smallest. Therefore, its Early voltage magnitude(26.05V) is the largest among those five devices. The Early voltage magnitude of the conventional NMOSFET is only 11.84V. In Fig. 3 we show how the larger Early voltage improves fundamental switching characteristics of a CMOS inverter. The CMOS inverter containing device b, and one using the conventional devices are compared. It is clear that the inverter characteristics for the implanted device are much closer to ideal than the one containing conventional devices. We also find that the noise margins (NM) for the implanted device b (NM_L=1.1V and NM_H=1.2V) are significantly improved over that for the inverter composed of the conventional MOSFETs (NM_L=1.0V and NM_H=1.0V).

B. Drain Induced Barrier Lowering(DIBL)

We find that device b, with implant near the source provides most protection against DIBL. The p^+ implant region provides an additional barrier for electrons to travel from source to drain. We help to verify this by simulating the threshold voltage at low and high values for V_{ds}. These values are extracted from the simulated curves of Fig. 4. The Id vs. Vg at Vds=0.05 V and Vds=3.0 V are given in Fig. 4(a) and (b). For Vds=0.05 V, the threshold voltages are 0.6 V, 0.8 V, 0.9 V, 0.9 V and 0.8 V for devices a-e respectively. For Vds=3.0 V, the threshold voltages change to 0.5 V, 0.75 V, 0.84 V, 0.8 V and 0.65 V for devices a-e respectively. The threshold voltage changes(ΔV_T) for devices a-e are 0.1 V, 0.05 V, 0.06 V, 0.08 V and 0.15 V. Thus, implanted structures b-d privide improved DIBL as compared to the conventional device. Furthermore, the closer the p^+ implant to the source, the better DIBL.

C. Substrate Current

Substrate current I_{sub} is a key factor for determining the reliability of submicron devices. Substrate current is usually proportional to the lateral electric field near the drain end of the device where hot electrons are generated. The lateral electrical field in the channel is lower for most of the implanted devices, as shown in Fig. 5. The I_{sub} vs. Vg of five devices is shown in Fig. 6. We know that the lateral electrical field of device b is the smallest. Therefore, the substrate current of device b is likely to be the smallest. This result is verified in Fig. 6.

D. Breakdown Voltage

In virtually all CMOS applications, it is best to have maximized the breakdown voltage. Our Boltzmann based simulations indicate that the implanted devices have improved breakdown voltage over the conventional structure. This is shown in Fig. 7 where the I-V characteristics for high drain bias of the five devices are given. The breakdown voltages are 5.5 V, 7.5 V, 8 V, 7.5 V and 6.5 V for devices a-e respectively. We see that while the device with implant near the source has improved breakdown over the conventional device, the device with implant in the middle of the channel has the best breakdown voltage characteristics. Therefore, if you want to design your device for maximum breakdown voltage, the implant should be in the channel center.

We also investigated the peak concentration and penetration depth of the p^+ implant. The higher the peak concentration, the larger the Early voltage. But the threshold voltage increases with peak concentration too. We can not increase the peak concentration without limit since the device will be impractical to use. The electron transport mainly occurrs in the inversion layer, which is approximately one hundred Å wide. The penetration depth of p^+ implant is usually much larger than this number. Therefore, varying the penetration depth of p^+ implant has no effect on device performance.

III. Conclusion

In this paper, the effect of placing an asymmetric p^+ implant in NMOSFET is investigated in datail. We find that for most applications, the p^+ implant should be put as close to the source side as possible. It has largest Early voltage, smallest lateral electrical field along the device surface, smallest DIBL, lowest substrate current and large breakdown voltage. Its I-V characteristics yield almost perfect current source behavior. The device with the implant near the source also shows larger noise margins than those of conventional devices.

Acknowledgement

This work is supported by Microelectronics Research Lab.

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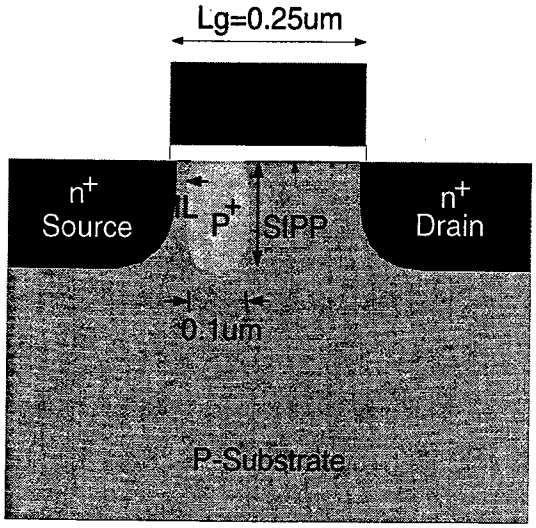


Fig. 1 (a) Asymmetric p^+ implant device structure.

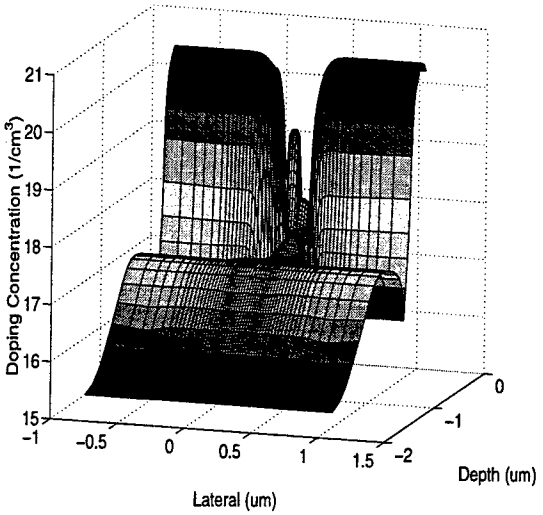


Fig. 1 (b) The doping profile of the device.

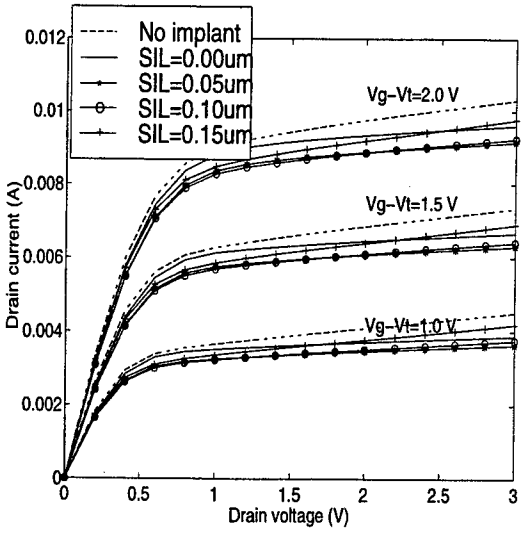


Fig. 2 The I-V characteristics of different devices.

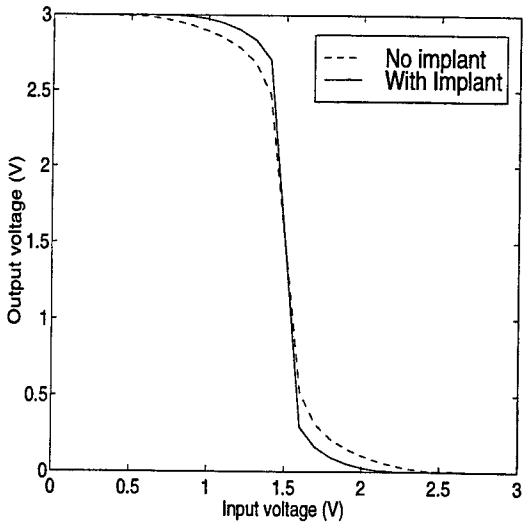


Fig. 3 The transfer curve of CMOS inverter.

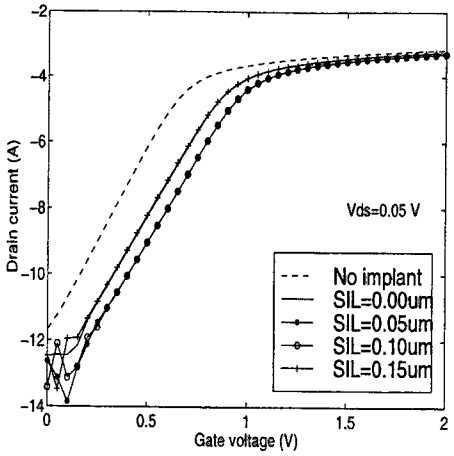


Fig. 4 (a) Subthreshold characteristics for Vd=0.05 V.

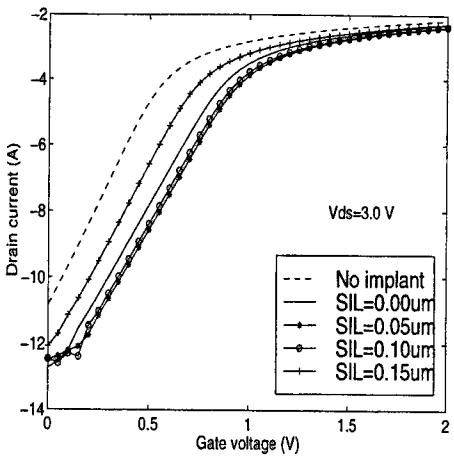


Fig. 4 (b) Subthreshold characteristics for Vd=3.0 V.

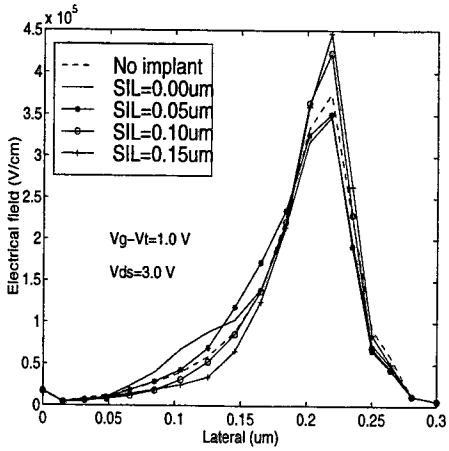


Fig. 5 The lateral electrical field along the surface of different devices.

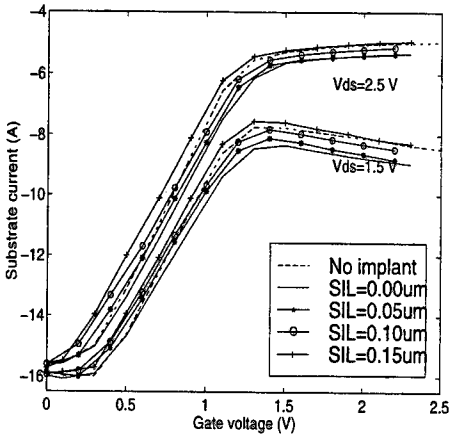


Fig. 6 The substrate current of different devices.

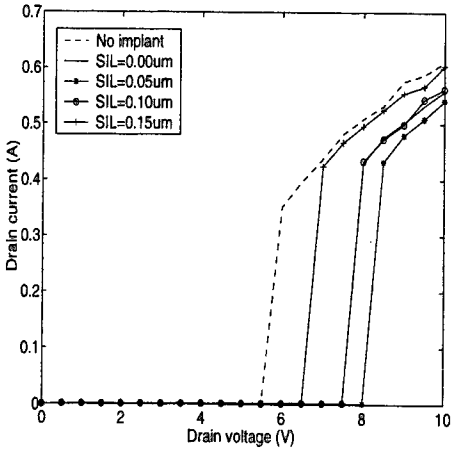


Fig. 7 The breakdown voltage of different devices.

The Enhanced Short Channel Performance of Narrow-width SOI MOSFET's with MESA Isolation

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I. INTRODUCTION

The continuous volume growth portable systems with their increasing demand for better performance makes Silicon-On-Insulator (SOI) technology one of the most competitive candidate for large volume IC production dedicated to low voltage, low power and high speed systems. Meanwhile, the ongoing device geometry scaling has pushed SOI MOSFETs to enter the regime of both short channel (for higher speed, lower supply voltage) and narrow-width (for higher density and lower power consumption) [1]. However, studies on narrow-width effects of SOI MOSFETs [2,3] are very limited compared with the extensive researches done on short channel effects [4].

In this paper, the behaviors of narrow-width SOI MOSFET's with MESA isolation have been investigated experimentally. Theoretical analysis has also been carried out to understand the mechanisms leading to the observations so that a strategy for optimization can be developed. We will present results on the influence of substrate biases on I-V characteristics in narrow-width fully-depleted (FD) SOI MOSFETs. The effect of substrate bias is suppressed in narrow width devices, which can be attributed to the influence of the 2-D field pattern on the potential distribution in the silicon film and demonstrated by 3-D device simulations. We will also present evidence for the improved immunity to short-channel effects in the narrow-width SOI MOSFETs. The observations are attributed to enhancement of gate control on channel potential in narrow-width devices.

II. DEVICE FABRICATION

The SOI MOSFET's used in this study were fabricated on p-type (100) SIMOX wafer with 380nm buried oxide. The devices being studied in this paper have n+ polysilicon gate for the n-channel MOSFET. Recessed-channel (RC) technology [5] has been chosen to reduce the source/drain series resistance, especially for MOSFETs with ultra-thin silicon film thickness (T_{si}). Different silicon film thickness at channel region was fabricated on the same wafer for comparison. The thickness of silicon film is measured by optical method after the RC process and other oxidation process. Gate oxide thickness is 101Å. The channel doping implant doses is 4×10^{12} cm^{-2}. The SEM micrograph of device cross section was shown in Fig.1.

III. SUPPRESION OF SUBSTRATE BIAS EFFECT IN NARROW-WIDTH FD SOI MOSFETs

The threshold voltages in FD SOI MOSFETs can be strongly influenced by substrate bias as shown in Fig.2. When we compare the results between Fig. 2 and Fig.3, we observe that the impact of substrate biases on threshold voltage is weakened dramatically in narrow-width devices. The threshold voltages as a function of substrate bias for SOI nMOSFET's with different channel width are shown in Fig. 4. When the channel width reaches 0.3μm, the threshold voltage becomes almost independent on substrate bias. To understand this phenomenon, we examined the special features unique to the structure of MESA-isolated SOI MOSFET's. As shown in Fig. 1, the gate bias can control the channel potential through the front gate, the sidewall gate, and the buried oxide. Fig. 5 shows the simulated equipotential contours and field vectors obtained from 3-dimensional simulator DAVINCI. The electric field originated from the front gate poly enters the silicon film through both the sidewall and the buried oxide, which enhances the control of the front gate on the channel potential. In actual process, the polysilicon under the silicon island(shown in Fig.1) enhances the control of the front gate on channel region and decreases the impact of substrate bias. Fig.6 shows the simulated back and front interface potential with and without the cavity structure considered. In narrow-width devices, this effect becomes more prominent and the back interface potential is being controlled by the front gate rather than the substrate bias.

IV. SHORT CHANNEL EFFECT IN NARROW-WIDTH SOI MOSFETs

As the channel length is reduced, the gate control on the channel potential becomes less effective and various short-channel effects appear. These short-channel effects set the limit of device scaling. Fig. 7 illustrates the subthreshold current characteristics of FD SOI nMOSFETs. The drawn channel length of the device is 0.2μm. As shown in the figure, serious punchthrough can be observed in devices with channel width equal to 1.5 μm. However, punchthrough is suppressed in the device with channel width equal to 0.3μm.. This is because the gate has better control of the channel potential in narrow-width devices which enable the channel length to scale down further. The better scalability of narrow width SOI MOSFETs can also be understood by examining the similarity of the structure in comparison with double-gate SOI MOSFETs (see Fig. 1). As double gate structure can improve short channel performance [6], similar effects can be observed in narrow-width SOI MOSFETs with MESA isolation. Fig.8 shows subthreshold swings of devices with different channel width under channel length scaling. As the channel width decreases, the subthreshold swing maintains its long channel value better even for very short-channel devices. Therefore, the scaling property of narrow-width MESA isolated SOI MOSFETs is much better than wide devices.

V. CONCLUSION

The behavior of narrow-width SOI MOSFETs with MESA isolation has been studied systematically. Through measurements and simulations, we have shown that the effects of substrate bias and punchthrough have been suppressed in narrow-width SOI MOSFETs due to the enhancement of gate control on channel potential through the sidewall and buried oxide. Narrow-width SOI MOSFETs exhibit a better channel length scaling ability as compared to wide devices. These enhanced performances may further promote the use of narrow width SOI MOSFET's in low voltage and low power electronics.

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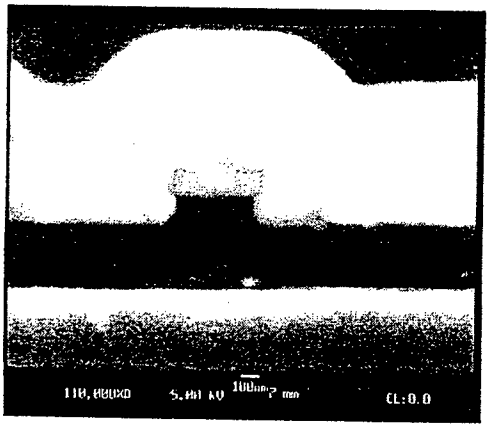


Fig.1. SEM micrograph showing the section of a SOI MOSFET with edge structure along the width direction.

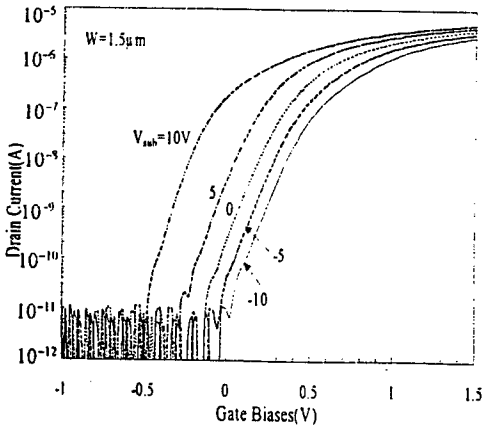


Fig.2. The subthreshold characteristics cross at different substrate biases. W=1.5μm t_{ox}=101Å, T_{Si}=791Å.

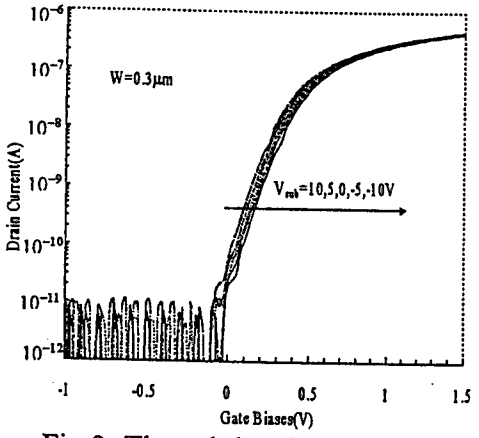


Fig.3. The subthreshold characteristics at different substrate biases. W=0.3μm.

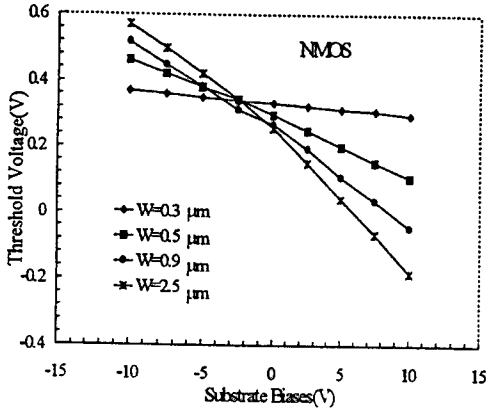


Fig.4. Threshold voltage vs. substrate bias for SOI nMOSFETs with different channel width.

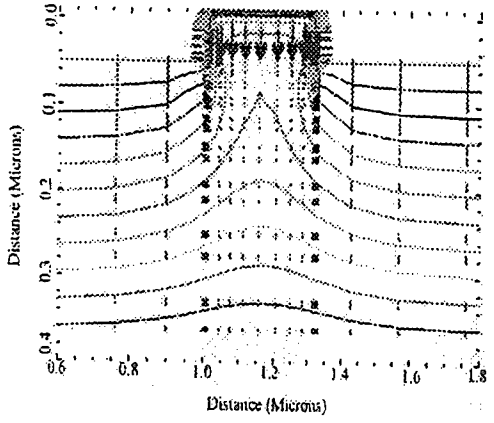


Fig.5. Davinci-simulated equipotential contours and field vectors for a 0.3μm width FD SOI nMOSFET biased at V_g=0.2V.

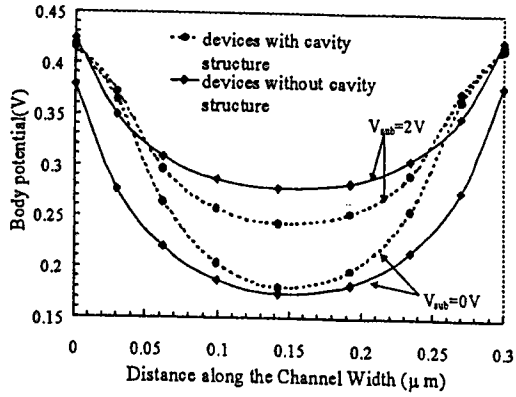


Fig.6. The simulated back interface potential profiles in the silicon film along the width direction for devices with and without including the cavity structure.

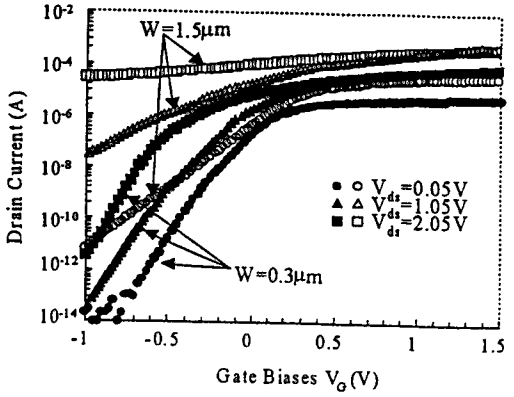


Fig.7. The subthreshold characteristics of short channel (L_g=0.2μm) SOI nMOSFETs at different drain voltages. Device parameters are T_{Si}=779Å, t_{of}=101 Å and the channel doping implantation dose = $4\times10^{12}cm^{-2}$.

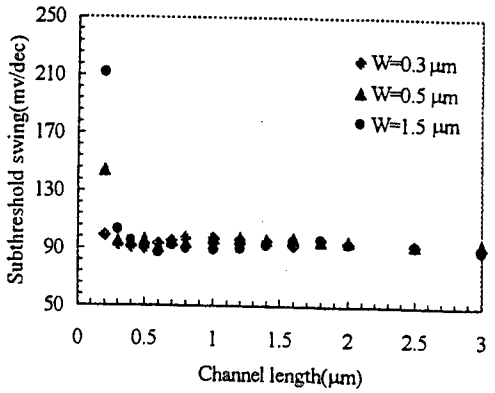


Fig.8. Subthreshold slope variation with channel length scaling at different channel width.

The Generalized Drift-Diffusion Model

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1. INTRODUCTION

The quasi-Fermi level approximation has provided a foundation for more than half a century of device theory and device simulation. Unfortunately, this approximation is very poor, even within the general class of "drift-diffusion" transport models. The most serious limitation is a systematic underestimation of diffusion. Another limitation is the potential for spurious mobility reduction due to built-in electric fields. These limitations have not been well publicized, and they are not widely appreciated.

The limitations of the quasi-Fermi level approximation cause significant discrepancies between theory and measurement. One example of the consequences is the pervasive need to perform empirical, structure-dependent 'mobility tuning' in order to achieve reasonable agreement between theoretical and measured results. The limitations of the quasi-Fermi level approximation also limit the predictive capabilities of numerical device simulators, and thus reduce the value of technology CAD. The fact that device theory and device simulation have suffered from these problems for half a century, without the source of the problems being recognized, will be referred to as "the quasi-Fermi level catastrophe.[1] "

The nature of the quasi-Fermi level catastrophe is explained in this paper, and a solution to the problem is proposed. The organization of this paper is as follows. The limitations of the quasi-Fermi level approximation are reviewed in the next section. The generalized drift-diffusion model, which avoids the major limitations of the quasi-Fermi level approximation, is described in section 3. Discussion and conclusions are presented in section 4.

2. THE QUASI-FERMI LEVEL APPROXIMATION

The current densities in semiconductor devices are often modeled using a low-order drift-diffusion approximation in which the electron current density has the form [1, p.50]:

$$\mathbf{J}_n = -nq\mu_n \nabla\varphi + qD_n \nabla n \qquad (1)$$

where $\mathbf{J}_n$ is the electron current density, n is the electron density, q is the magnitude of electronic charge, μ_n is the electron mobility, φ is the electrostatic potential and D_n is the electron diffusion coefficient. The transport parameters μ_n and D_n are treated as functions of the magnitude of the local electric field $\mathbf{E}$ (= $-\nabla\varphi$). For non-degenerate semiconductors it is assumed that μ_n and D_n are related through the Einstein relationship:

$$D_n = \frac{\mu_n k T_L}{q} \qquad (2)$$

[1]The term catastrophe only applies within the fields of device theory and device simulation. Developers of microelectronics products use experiments and empirical design techniques to compensate for the shortcomings of theory and simulation.

where k is Boltzmann's constant and T_L is the lattice temperature in Kelvins. Using (2) to eliminate the diffusion coefficient from (1) yields a compact expression for the electron current density:

$$\mathbf{J}_n = -nq\mu_n \nabla \phi_n \qquad (3)$$

where ϕ_n is the quasi Fermi level for electrons, given by

$$\phi_n = \varphi - \frac{kT_L}{q} \ln \frac{n}{n_i} \qquad (4)$$

and n_i is the intrinsic carrier concentration[2]. Similar equations are used for holes. This model will be referred to as the conventional drift-diffusion model.

This formulation of charge transport was introduced more than half a century ago [2], and many improved models have been developed subsequently. One hierarchy of models is obtained by starting from the Boltzmann Transport Equation and then introducing additional approximations. A popular approach within this hierarchy is to assume a parametric form for the carrier distribution as a function of energy and wave-vector [3-5]. This yields models that provide a description of 'non-local' effects such as velocity overshoot. Further approximations lead to 'local' drift-diffusion models, which do not provide a description of non-local effects.

Limitations of the conventional drift-diffusion model are readily apparent when higher-order transport models (see, e.g. [3]-[8]) are used as a reference standard. Two significant limitations of the conventional drift-diffusion model are that the lattice temperature T_L in equation (2) should be the electron temperature T_e, and the diffusion coefficient should be inside the second gradient term in equation (1). A third limitation is that built-in fields, which are present even at equilibrium, can cause an unphysical reduction in mobility. (In extreme cases they can also cause unphysical impact ionization.)

Compared to higher-order transport models, the conventional drift-diffusion model underestimates particle diffusion by a factor of T_e/T_L. The maximum values of T_e that occur in device operation have been investigated using Monte Carlo simulation and are as high as several thousand Kelvins. The conventional drift-diffusion model can thus underestimate diffusion effects by more than one order of magnitude.

3. THE GENERALIZED DRIFT-DIFFUSION MODEL

The generalized drift-diffusion model avoids the three previously identified limitations of the quasi-Fermi level approximation. The generalized drift-diffusion approximation is obtained as a local limit of a non-local energy balance model. The transition to a local model is made by assuming that all transport parameters, including the electron temperature, are functions of a local effective driving field. The form of the effective driving field is deduced from the requirement that the driving field vanishes at equilibrium. The transport parameters are determined from the requirement of correct behavior in the homogenous steady-state limit.

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[2] The consistency of equations (1) through (3) requires that $\phi_n = \varphi - \frac{kT_L}{q} \ln n + c$ where c is an arbitrary constant that determines the absolute level of ϕ_n. The choice $c = \frac{kT_L}{q} \ln n_i$ sets the quasi-Fermi level at equilibrium equal to the Fermi level.

When D_n is placed inside the second gradient term in equation (1), and T_e replaces T_L in equation (2), the electron current density has the form:

$$\mathbf{J}_n = -nq\mu_n \nabla\varphi + k\nabla(\mu_n n T_e) \qquad (5)$$

This can be written as

$$\mathbf{J}_n = nq\mu_n \mathbf{G} \qquad (6)$$

where **G** is an effective driving field given by

$$\mathbf{G} = -\nabla\varphi + \frac{k\nabla(\mu_n n T_e)}{nq\mu_n} \qquad (7)$$

The condition $T_e(\mathbf{G}=0) = T_L$ leads to correct behavior in the equilibrium limit. The dependencies of μ_n and T_e on $|\mathbf{G}|$ are determined by requiring correct behavior in the homogenous steady-state limit. For a uniform electric field $\mathbf{E}_0$ and spatially uniform values of n, μ_n and T_e, **G** is equal to $\mathbf{E}_0$. A characterization of μ_n and T_e as functions of $|\mathbf{E}_0|$ therefore provides the dependence of these quantities on $|\mathbf{G}|$. Characterizations as functions of $\mathbf{E}_0$ can be obtained from experiment, from analytic theory, or from Monte Carlo simulation.

Different but mathematically equivalent forms of equations (5) and (7) provide additional physical insight, and may be more suitable for numerical implementation. Expanding the gradient term in equation (7) yields the result that:

$$\mathbf{G} = -\nabla\varphi + \nabla V_T + V_T \nabla \ln n + V_T \nabla \ln \mu_n \qquad (8)$$

where $V_T = kT_e/q$ is the thermal voltage associated with the electron distribution. The first three terms are readily identifiable as the drift term, the thermal diffusion term, and the particle diffusion term. The fourth term arises from spatial variations in the mobility. A similar term is obtained in some higher-order transport models.

G is defined implicitly since μ_n and T_e on the right hand sides of (7) and (8) are themselves functions of $|\mathbf{G}|$. This is a significant impediment to the development of analytic theories of device operation. The implicit definition introduces some additional complexity for device simulation, but does not present any fundamental problems.

4. DISCUSSION AND CONCLUSIONS

The generalized drift-diffusion model described here is different from other transport models that are referred to as 'enhanced', 'generalized', or 'augmented' drift-diffusion models. These other models fall into two main classes. One is concerned with extending the conventional drift-diffusion model to account for degeneracy and for spatial variations in the electron affinity, band gap and density of states (see, e.g. [9]). The other class of model seeks to supplement the conventional drift-diffusion model with terms that account for velocity overshoot (see, e.g. [10]-[12]). The new model described in this paper eliminates several major deficiencies of conventional drift-diffusion, and provides a consistent local limit of the

non-local energy balance approach. It does not provide a description of non-local effects such as velocity overshoot.[3]

Results obtained using the conventional drift-diffusion model are often compared to results obtained using higher-order non-local transport models. The observed differences are normally attributed to the presence of non-local effects. This work shows that such attribution can be incorrect or misleading, since a significant component of the differences may be associated with errors in the way that the conventional drift-diffusion model accounts for diffusion.

In conclusion, three deficiencies of the conventional drift-diffusion model were identified. The most significant deficiency is the systematic underestimation of diffusion, which leads to the "quasi-Fermi level catastrophe." A generalized drift-diffusion model that corrects all three deficiencies was proposed. This new model should significantly improve the accuracy and range of applicability of drift-diffusion based simulators.

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[3] A first-order description of velocity overshoot can be obtained using the approach taken in [16], with ∇G replacing ∇E in the overshoot term.

A Flux Vector Splitting Scheme for Hydrodynamic Simulation of MESFET's

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I. INTRODUCTION

In recent years, physical transport models for simulation of semiconductor devices have been upgraded from the quasi-equilibrium drift-diffusion model to non-equilibrium energy transport model due to the reduction in device dimensions to submicron size. The transport model in the exiting commercial device simulators is usually based on the energy transport model that is however a simplified version of the hydrodynamic model. To more completely take into consideration the non-equilibrium behavior of charge carriers, the hydrodynamic model [1-3] has been employed in many recent studies of small devices. As the physical models become more sophisticated, challenge of developing a stable, efficient, and accurate numerical scheme has significantly increased.

Due to some similarity between the hydrodynamic semiconductor equations and the fluid dynamic Euler or Navier-Stokes equations, many numerical techniques including finite difference and finite element schemes applied to modeling semiconductor devices are based on those used in fluid dynamics. Among the finite difference schemes in fluid dynamic problems, the flux vector splitting (FVS) method [4-6] is one of the simplest and most efficient methods. Although it has been widely used in fluid dynamics, and it has been shown to be able to handle high gradient problems [5,6], the FVSM is rather new to the semiconductor device community.

In this study, a two-dimensional mixed FVS method based on the Steger-Warming splitting [4] is developed for hydrodynamic modeling of MESFET's. This method combines the upwind and central differences to achieve accuracy and stability. The upwind difference in the FVS method splits the hydrodynamic equations into two parts associated with the forward and backward running fluxes. The formulation is described in Sec. II, and numerical results are presented in Sec. III.

II. FLUX VECTOR SPLITTING FORMULATION FOR THE HYDRODYNAMIC EQUATIONS

Descriptions of the semiconductor hydrodynamic model, including carrier density (n), momentum ($\mathbf{p}$), and energy (w) conservation and Poisson's equations, can be found elsewhere [1-3]. Only the FSV formulation is presented in this paper. To construct the 2D FVS hydrodynamic formulation, the state-variable vector is defined as

$$\mathbf{U}^T = [n \quad v_x \quad v_y \quad w]. \tag{1}$$

where v_x and v_y are velocities in x and y direction, respectively. The 2D hydrodynamic equations can be expressed in the matrix form

$$\frac{\partial \mathbf{U}}{\partial t}+[A]\frac{\partial \mathbf{U}}{\partial x}+[B]\frac{\partial \mathbf{U}}{\partial y}=\mathbf{H}. \tag{2}$$

where $[A]$ and $[B]$ are the Jacobian matrices, and the source vector $\mathbf{H}$ includes the influences of electric field and collisions. The similarity transformations exist if the equation system is hyperbolic in both x and y directions. That is,

$$[A]=[L_A][\Lambda_A][L_A]^{-1} \text{ and } [B]=[L_B][\Lambda_B][L_B]^{-1}, \tag{3}$$

where $[\Lambda_A]$ and $[\Lambda_B]$ are diagonal matrixes for eigenvalues of $[A]$ and $[B]$, respectively, $[L_A]$ and $[L_B]$ are the matrixes whose rows are composed of corresponding eigenvectors. Then, the eigenvalues can be split into positive and negative parts, and consequently

$$[A]=[L_A][\Lambda_A]^{+}[L_A]^{-1}+[L_A][\Lambda_A]^{-}[L_A]^{-1}=[A]^{+}+[A]^{-} \tag{4}$$

$$[B]=[L_B][\Lambda_B]^{+}[L_B]^{-1}+[L_B][\Lambda_B]^{-}[L_B]^{-1}=[B]^{+}+[B]^{-} \tag{5}$$

A mixed scheme combining central and upwind differences is used to optimize the numerical stability as well as the accuracy. The time division Δt is split into 2 parts, $\beta\Delta t$ and $(1-\beta)\Delta t$, where $0<\beta<1$. Finite differencing is performed explicitly with two steps; that is, each time step is divided into 2 parts. The upwind scheme is used in the first part of the time step, and the central difference method in the second part. The upwind and central difference equations for Eq. (2) is given in Eq. (6) and (7), respectively.

$$\frac{\mathbf{U}_{i,j}^{n+\frac{1}{2}}-\mathbf{U}_{i,j}^{n}}{\beta\Delta t}+[A]^{+}\left[\frac{\mathbf{U}_{i,j}^{n}-\mathbf{U}_{i-1,j}^{n}}{\Delta x}\right]+[A]^{-}\left[\frac{\mathbf{U}_{i+1,j}^{n}-\mathbf{U}_{i,j}^{n}}{\Delta x}\right]+ [B]^{+}\left[\frac{\mathbf{U}_{i,j}^{n}-\mathbf{U}_{i,j-1}^{n}}{\Delta y}\right]+[B]^{-}\left[\frac{\mathbf{U}_{i,j+1}^{n}-\mathbf{U}_{i,j}^{n}}{\Delta y}\right]=\mathbf{H}_{i,j}^{n}. \tag{6}$$

$$\frac{\mathbf{U}_{i,j}^{n+1}-\mathbf{U}_{i,j}^{n+\frac{1}{2}}}{(1-\beta)\Delta t}+[A]\left[\frac{\mathbf{U}_{i+1,j}^{n+\frac{1}{2}}-\mathbf{U}_{i-1,j}^{n+\frac{1}{2}}}{2\Delta x}\right]+[B]\left[\frac{\mathbf{U}_{i,j+1}^{n+\frac{1}{2}}-\mathbf{U}_{i,j-1}^{n+\frac{1}{2}}}{2\Delta y}\right]=\mathbf{H}_{i,j}^{n+\frac{1}{2}}. \tag{7}$$

Selection of the β value will depend on the nature of the problems. To minimize the instability in a hyperbolic problem due to the convective term, a large value for β should be used, which reduces the effect of the central difference. On the other hand, if more distortion is observed, β needs to decrease to reduce the upwind contribution.

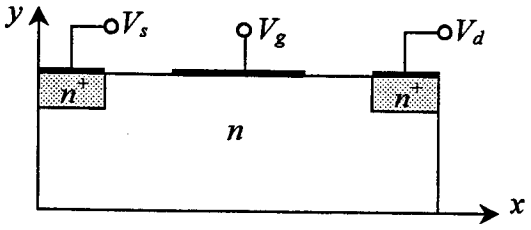


Fig. 1 The MESFET structure. N_d=3×10^{17} cm^{-3} in the n^+ regions, and N_d=10^{17} cm^{-3} in the n region.

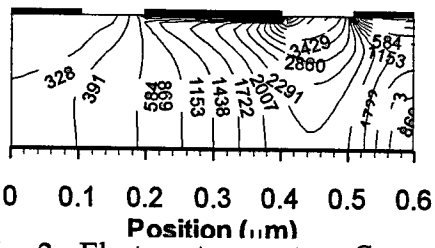


Fig. 2 Electron temperature Contour lines in the MESFET at V_{ds} =2V and V_{gs}= –0.8V.

III. SIMULATION RESULTS

3.1 Device structure

To examine the capability of the hydrodynamic FVS method presented in Sec. II, the developed numerical scheme is applied to a 2D *Si* MESFET structure shown in Fig. 1. The gate length equals 0.2 μm, and the drain/source metal contact is 0.1 μm long. The device length and depth are 0.6 and 0.2 μm, respectively. The depth of the n^+ source/drain region is 0.05 μm. In the simulation, the 2D device is divided uniformly into 120×40 elements.

3.2 Numerical results

The electron temperature contour curves in the 2D MESFET are shown in Fig. 2. The maximum electron temperature is found to appear near the gate metal edge between the gate and drain. The electron density and electric potential are displaced in Figs. 3(a) and 3(b), respectively. A depletion region under the gate is observed, where the electron density is extremely small due to the strong electric field perpendicular to the gate contact caused by the reverse-biased Schottky barrier. The *x*- and *y*-component electric fields are shown in Figs. 4(a) and 4(b), respectively.

The 2D MESFET structure with a deep submicron gate length given in Fig. 1 provides a challenging numerical problem. The source/drain and gate metal contacts impose discontinuities on the boundary conditions at the metal edges. The boundary discontinuities of electric fields are clearly revealed in Figs. 4(a) and 4(b). In addition, due to the negative applied voltage, electron density at the gate contact is approximately 10 orders of magnitude smaller than the electron density in the n^+ region. This induces a drastic change in electron density in the short-channel MESFET, as shown in Fig. 3(a), at the source/drain-channel junctions near the boundary along the source-gate-drain surface. Regardless the field discontinuities and the drastic changes in electron density that enhance the difficulty in getting stable numerical solution, the developed method provides very stable and smooth numerical results as illustrated in Figs. 3 and 4.

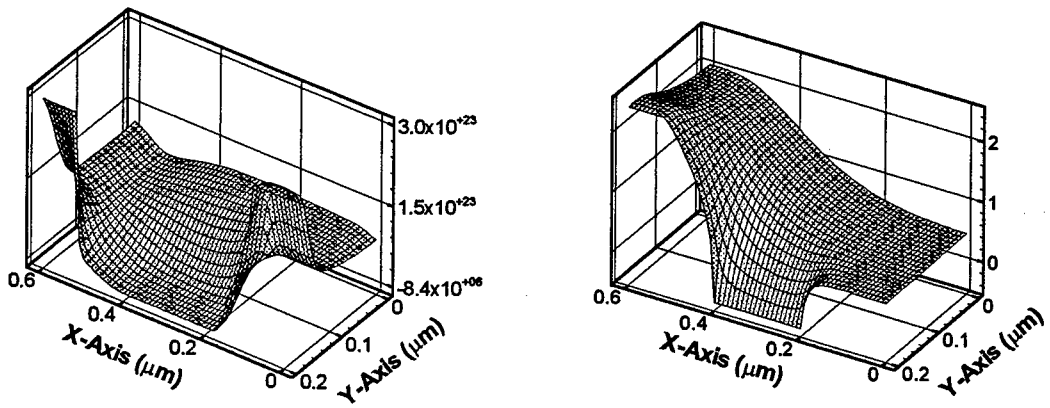


Fig. 3 (a) Electron density (m^{-3}) and (b) potential in the MESFET at V_{ds}=2.0 Volt and V_{gs}= −0.8Volt.

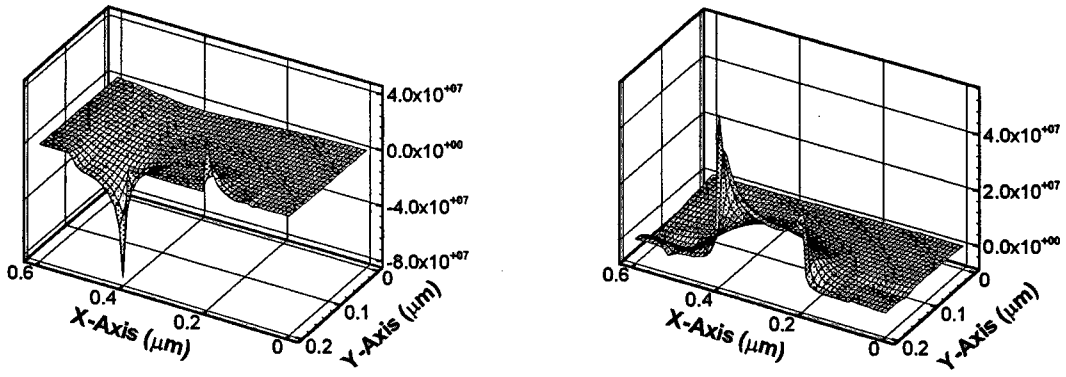


Fig. 3 (a) x-component and (b) y-component electric fields (V/m) in the MESFET at V_{ds} =2.0 Volt and V_{gs}= –0.8Volt.

Numerical results shown in Figs. 2-4 for the 2D MESFET indicate that the developed mixed FVS method based on the hydrodynamic model is capable of handling the discontinuities of the boundary conditions at the edges of metal contacts as well as the extremely large density gradient.

IV. CONCLUSION

A FVS finite-difference method for one-carrier hydrodynamic simulation of semiconductor devices has been developed. The developed method was applied to a 2D MESFET with a gate length of 0.2 μm. Unlike most of finite difference schemes developed for hydrodynamic modeling of semiconductor devices, the developed FVS method contains neither adjustable parameter nor smooth operator to arrive at stable solution. It has been demonstrated that the hydrodynamic FVS method is simple and robust for simulation of 2D semiconductor devices.

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Steady-State Time-Domain Analysis Including Frequency-Dependent Components

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***Abstract*-A method for steady-state time-domain analysis including components defined in the frequency domain is presented. The circuit is divided into time and frequency dependent parts where the time-domain representation of the frequency-dependent part is created with the aid of a convolution integral. Examples are given to demonstrate that the novel method is efficient and sufficiently fast to be used in circuit design. The simulation results show good agreement with those obtained by harmonic balance and transient analysis.**

I. Introduction

Several steady-state analysis methods for nonlinear circuits have been reported. The method evaluates the linear part of the circuit in the frequency domain and the nonlinear in the time-domain. The currents and voltages from the linear to nonlinear part and from the nonlinear to the linear part are given by Fourier and inverse Fourier transforms, respectively. Harmonic balance is applicable primarily to strongly nonlinear circuits and it is quite slow, especially in the case of two excitation signals.

The steady-state solution can also be calculated in the time-domain. It is a straightforward matter to use conventional circuit theory to write time-domain differential equations that describe a nonlinear circuit. The resulting differential equations can then be solved numerically. Differential equation algorithms may require large amounts of computing time, since the transient response may be significant for a hundred cycles or more. This gives rise to expensive and perhaps inaccurate results. Another problem is due to frequency-dependent components that can not be described in the time-domain. Ref. [4] solves that problem but the analysis is quite slow. Transient analysis is the simplest time-domain steady-state method. The main goal of time-domain steady-state methods is to find a steady-state solution with less computational cost than the transient analysis method requires. The steady-state methods find a portion of the transient response, which is used to predict the optimisation [2], and extrapolation [3]. Skelboe [3] presents three extrapolation methods: the scalar and vector ε -algorithms and the minimum polynomial extrapolation algorithm.

An ultimate steady-state method has not been presented. This work presents one more steady-state method. A steady state time-domain analysis method is introduced in [1], [7]. The method treats the nonlinear components in the time-domain while not allowing any linear frequency-dependent components to be included. However, in microwave circuit design, e.g., dispersive microstrip elements play a central role in the circuit. More than half of the components available in microwave circuit design tools are only known in the frequency domain. In this paper, the method presented in [1] has been extended to include frequency-dependent components using the convolution integral.

First, basic steady-state time-domain analysis is introduced, and then the extension for calculating frequency-dependent components is presented.

II. Description of the method

The steady-state time-domain analysis is carried out using fixed step integration by dividing period T into N_{ss} steps each being equal to

$$h = \frac{T}{N_{ss}}. \tag{1}$$

The steady-state condition requires that all voltages (currents) are equal at $t = t_n$ and $t = t_n + T$, i.e.,

$$\boldsymbol{u}_n = \boldsymbol{u}_n + N_{ss}, \tag{2}$$

where $\boldsymbol{u}_n$ denotes $u(t_n) = u(n \cdot h)$ and boldface is used to indicate vectors (matrices). Computationally, the steady-state can be found by writing a large matrix [1] including the voltage (current) equations for each time step as well as the simple steady-state condition (2). For linear circuits one matrix inversion directly gives the desired steady-state waveforms, whereas nonlinear circuits normally require iterations to be performed.

If the circuit includes frequency-dependent linear components it has to be divided into time- and frequency parts. The time-dependent part includes all nonlinear components whereas the frequency-dependent part includes all linear components having a frequency-domain representation. Calculation of the time-dependent part has already been shown. This section shows how to find the time-domain representation for the frequency-dependent part [4].

Let us assume, for the linear part, that all y-parameters have a finite value at the following discrete frequencies

$$f = 0, \cdots, \frac{N_f}{2t_{tran}}, \tag{3}$$

where t_{tran} is the time at which $y_{k,l}(t)$ has reached zero, $y_{k,l}(t)$ is the inverse Fourier transform of $Y_{k,l}(j\omega)$, and N_f is number of diescrete samples of $y_{k,l}(t)$. The current of port k caused by port voltage U_l is

$$i_{k,l}(j\omega) = Y_{k,l}(j\omega) U_l(j\omega), \tag{4}$$

which in the time domain yields

$$i_{k,l}(t) = y_{k,l}(t) * u_l(t) = \int_0^\infty y_{k,l}(\tau) u_l(t-\tau) d\tau. \tag{5}$$

Remembering that t_{tran} is the time at which $y_{k,l}(t)$ has reached zero, the convolution integral (5) can be rewritten [4]

$$\begin{aligned} i_{k,l}(t) &= \int_0^{t_{tran}} y_{k,l}(\tau) u_l(t-\tau) d\tau \\ &= \begin{cases} \int_0^t y_{k,l}(\tau) u_l(t-\tau) d\tau + U_{l,DC} \int_t^{t_{tran}} y_{k,l}(\tau) d\tau, & t < t_{tran} \\ \int_0^{t_{tran}} y_{k,l}(\tau) u_l(t-\tau) d\tau, & t \geq t_{tran}. \end{cases} \end{aligned} \tag{6}$$

In the method proposed only the time points $t \geq t_{tran}$ are of interest, because the steady-state solution of the circuit is to be found. Rewriting the last part ($t \geq t_{tran}$) of (6) using the Trapezoidal rule, which can be now used because the matrix is completely filled, and remembering $y(t_{tran}) = 0$, we get

$$i_{k,l}(t_n) = h\left[\frac{1}{2} y_{k,l}(0) u_l(t_n) + \sum_{p=1}^{N_f - 1} y_{k,l}(t_p) u_l(t_{n-p})\right], t_n \geq t_{tran}. \tag{7}$$

The first term of (7) is a conductance and the others are voltage-controlled current sources. Fig. 1 shows the equivalent circuit of (7).

When the steady-state is reached, (2) is true. Remember that N_f equals the number of discrete samples of $y(t)$ and N_{ss} is the number of time points in one period. We will be dealing with discrete values of currents

and voltages. Using the short-hand notation $u(t_n) = u(n)$ we can rewrite (7) (without port indices)

$$i(n) = \frac{1}{N_u}\left\{\frac{1}{2}y(0)u(n) + \sum_{p=1}^{N_f-1} y(p)u\left(n - p + \left(floor\left[\frac{n}{N_u}\right] - floor\left[\frac{n-p}{N_u}\right]\right)\cdot N_u\right)\right\}, \quad (8)$$

where floor $[x]$ is the largest integer that is less than or equal to x. Equation (8) may look complicated. However, it only says that the controlling voltage is always taken from the same steady-stae period of the circuit. Impulse response $y(n)$ goes from $n = 0....N_f$. That is also shown in Fig. 1.

III. Comparison with other methods

Steady-state time-domain analysis can be compared with harmonic balance and transient analysis. Normal transient analysis cannot take frequency-domain characteristics into account. However, a method that makes transient analysis for frequency-domain components possible (8) is implemented in APLAC circuit simulator program. The method is based on the same convolution integral as shown in this work. In this work the method is called the convolution method. A comparison with that method is also presented.

Comparison with harmonic balance, transient analysis and convolution method

Harmonic balance calculates the steady-state solution of a nonlinear circuit. All waveforms are represented in terms of Fourier series coefficients. In the stead-state time-domain method, only the period of the circuit has to be known. However, if the period of the circuit is very long or if the currents and voltages of the circuit change very rapidly, many time points in the steady-state time-domain analysis are needed.

Transient analysis is a well studied and general method to calculate the steady-state solution. Conventional analysis cannot take frequency-domain characteristics into account. The convolution method presented in reference [4] does make it possible. Disadvantages of transient analysis using convolution integral and steady-state time-domain analysis with convolution integral are that the user has to define the number of discrete samples N_f of the impulse response $y_{k,l}(t)$ and the time t_{tran} at which $y_{k,l}(t)$ has reached zero.

IV. Examples

This section presents two examples to demonstrate the method proposed as implemented in the circuit simulator APLAC [5]. In the first example, steady-state time-domain analysis is used without frequency-domain components. The last example shows how a convolution integral can be used to simulate dispersive transmission lines. Computer calculations were made on an HP9000/720.

A. *Voltage multiplier*

The voltage multiplier is shown in Fig. 2. The component values are $R = 1.0\Omega, R_L = 10\,k\Omega, C = 1.0\mu F$, and $e(t) = \hat{e}\sin(2\pi f_0 t)$, where $\hat{e} = \sqrt{2.220}$ V and $f_0 = 50$ Hz. The saturation current of the diodes is $I_s = 10$ fA.

The simulation is also compared with the harmonic balance method and transient analysis. Harmonic balance is done using $N_{hb} = 8$ harmonics. Table 1 shows the simulation times and memory requirements. The matrix of the steady-state time-domain analysis is solved using a sparse matrix algorithm. In Table 1 and Fig. 3 and 4 HB, TRAN, CONVOL, and SS-TD denote harmonic balance, conventional transient analysis, transient analysis using convolution (not applicable in this example), and steady-state time domain analysis, respectively.

B. *Transmission line*

The dispersive transmission line model includes the skin effect and frequency-dependent dielectric losses.

Conventional transient analysis can be used for the transmission line model presented in [6].

The component values of the circuit are $R = 50\ \Omega$, $C = 5$pF, and $j(t) = \hat{j} \sin(2\pi f_0 t)$, where $\hat{j} = 0.3$ A. The parameters of the dispersive transmission line are: length of line l = 1.0 m, inner diameter 2a = 0.4 mm, outer diameter 2b = 2.58 mm, relative dielectric constant $\varepsilon_r = 5.0$, conductivity of the dielectric material $\sigma_e = 0.1n\ {}^{S}/_{m}$, conductivity of the metal wire $\sigma = 57.0M\ {}^{S}/_{m}$, loss tangent of the dielectric material $\tan\delta = 0.1$, and frequency at which the loss tangent is given f_t = 1.0 MHz. The parameters which affect the time-domain model used in conventional transient analysis are : number of RC sections in the dielectric loss ladder N_c = 6, number of RL sections in the skin effect ladder N_L = 5, number of the transmission line sections N_s = 30.

The simulations were performed with N_{ss} = 64 time points and discrete samples of impulse response was N_f = 2048. The time-domain model of the transmission line is used only in the conventional transient analysis. Harmonic balance was performed using N_{hb} = 32 harmonics. Table 2 shows simulation times and memory requirements. In Table 2 and Figs. 6 and 7 HB, TRAN, CONVOL, and SS_TD denote harmonic balance, conventional transient analysis, transient analysis using convolution and steady-state time-domain analysis, respectively.

V. Conclusions

A method for steady-state time-domain analysis has been presented in which a circuit containing frequency-dependent components is divided into two parts, time- and frequency-dependent. The time-dependent part contains all nonlinear components and it may contain any components that are defined in the time domain. The frequency-dependent part is treated as an *n*-port for which the complex short-circuit admittance parameters (*y*-parameters) are calculated. The impulse response of the frequency-dependent part is obtained using the fast Fourier transform. The currents of the *n*-port can be calculated using a convolution integral for the impulse response and port voltages. It has been demonstrated that the method proposed is competitive with the widely used harmonic balance method. However, the present method does not have the restriction of the HB method, that is, the maximum number of independent excitations is not limited to three.

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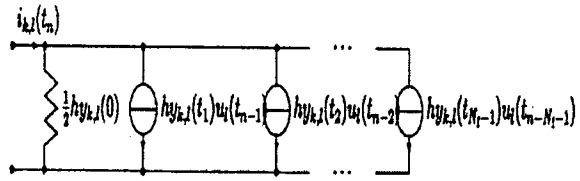


Figure 1 Equivalent circuit of (7).

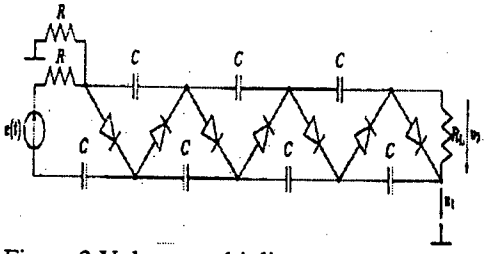


Figure 2 Voltage multiplier.

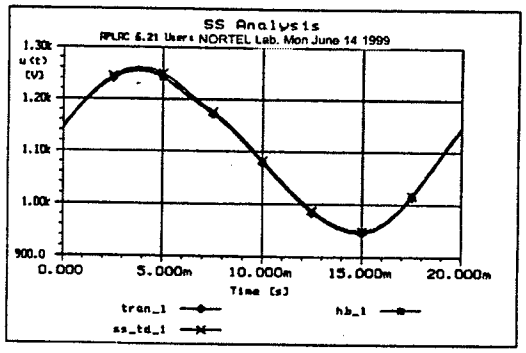


Figure 3 Steady-state waveforms of circuit in Fig. 2.

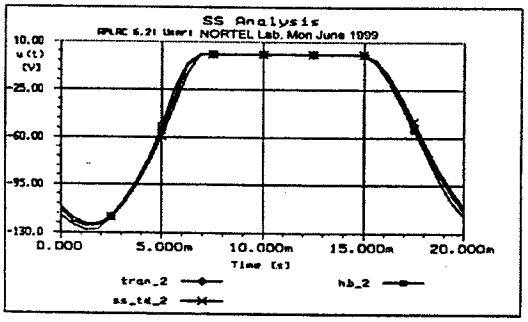


Figure 4 Steady-state waveforms of circuit in Fig. 2.

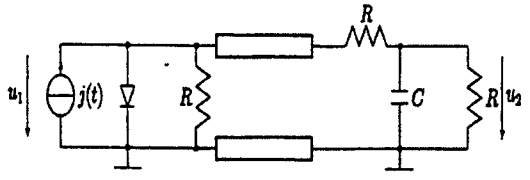


Figure 5 Transmission line.

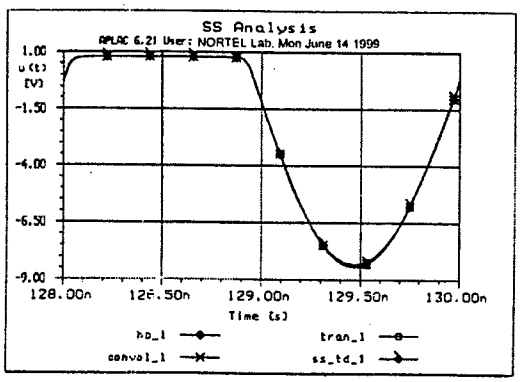


Figure 6 Steady state waveforms of circuit in Fig. 5.

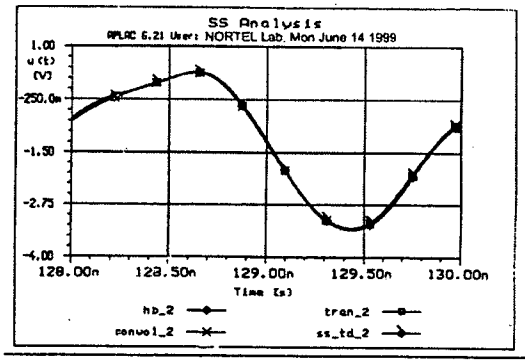


Figure 7 Steady state waveforms of circuit in Fig. 5.

	HB	TRAN	CONVOL	SS_TD
CPU time	13.1 s	8.9 s	-	1.6 s
Memory requirement	3.8 Mbytes	3.4 Mbytes	-	4.0 Mbytes

Table 1 CPU times and memory requirements of Circuit in Fig. 2.

	HB	TRAN	CONVOL	SS_TD
CPU time	8.0 s	94 s	7.0 s	16.6 s
Memory requirement	7.2 Mbytes	3.6 Mbytes	3.9 Mbytes	8.2 Mbytes

Table 2 CPU times and memory requirements of circuit in Fig. 5.

A Compact MOSFET I_{ds} Model for Channel-Length Modulation Including Velocity Overshoot

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Abstract—A compact model for MOSFET channel-length modulation based on velocity overshoot is presented, which has a simple familiar form with one fitting parameter embedded in the length- and bias-dependent effective Early voltage. The model physically describes the internal field distributions in the velocity-saturation region and interprets them in terms of the effective potential drop and average velocity in the intrinsic channel, and yet, it is easy to characterize from measured terminal current.

I. INTRODUCTION

MOSFET Channel-length modulation (CLM) has been conventionally modeled by the "pinch-off" model [1] where the effective channel length (L_{eff}) is reduced by Δl in saturation, which can be modeled by the Early voltage (V_A):

$$I_{ds} = \frac{L_{eff}}{L_{eff} - \Delta l} I_{ds0} = \left(1 + \frac{\Delta l}{L_{eff} - \Delta l}\right) I_{ds0} = \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right) I_{ds0}. \quad (1)$$

However, this picture leads to an infinite field at $y = L_{eff} - \Delta l$ due to zero mobile-charge requirement at that location [2]. The quasi-2D approach [3] has demonstrated success in physically modeling carrier transport in the velocity-saturation region (VSR). One major task is to empirically relate the characteristic length (l) to the gate oxide thickness (t_{ox}) and LDD junction depth (x_j) [2] so as to match the measured terminal current, which can be difficult for a wide range of devices and bias conditions.

In this paper, we propose a simple compact I_{ds} model for CLM based on the quasi-2D formulation but retaining the simple form of the "pinch-off" model. A bias- and length-dependent effective Early voltage (V_{Aeff}) is defined, which requires only one empirical parameter extraction.

II. MODEL FORMULATION

Our unified I_{ds} model is based on the two-region piecewise velocity–field formulation [3]:

$$I_{ds0} = C_{ox} \frac{W}{L_{eff}} \frac{\mu_{eff0}}{1 + V_{deff}/(E_{sat} L_{eff})} \left[(V_{gs} - V_t) V_{deff} - \frac{A_b}{2} V_{deff}^2 \right] \quad (2)$$

$$A_b = 1 + \zeta \frac{\gamma}{2\sqrt{\phi_s - V_{bs}}}, \quad \gamma = \frac{1}{C_{ox}} \sqrt{2q\varepsilon_{si} N_{eff}} \quad (2a)$$

where ζ in the bulk-charge factor (A_b) is a fitting parameter. N_{eff} is an effective channel doping modeled through the threshold voltage (V_t) [4], [5]. μ_{eff0} is the mobility due to vertical field [6]. V_{deff} is an effective saturation voltage (with a smoothing function used in BSIM3) [7]:

$$V_{deff} = V_{dsat} - \frac{1}{2}\left[V_{dsat} - V_{ds} - \delta_s + \sqrt{(V_{dsat} - V_{ds} - \delta_s)^2 + 4\delta_s V_{dsat}} \right]. \quad (2b)$$

The quasi-2D solution reveals that the electric field in the VSR (of length Δl) increases exponentially as $E_{sat}\cosh(y/l)$, as shown in Fig. 1 for three gate lengths (extracted from actual data), in which the VSR length (Δl), characteristic length (l), maximum field (E_m), and saturation field (E_{sat}) are well defined by

$$\Delta l = l \ln \frac{(V_{ds} - V_{deff})/l + E_m}{E_{sat}}, \quad l = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} x_j}, \quad E_m = \left[\frac{(V_{ds} - V_{deff})^2}{l^2} + E_{sat}^2 \right], \quad E_{sat} = \frac{2v_{sat}}{\mu_{eff0}}. \quad (3)$$

To retain the compact I_{ds} form, we assume that the saturation field E_{sat} in (2) (without CLM) is replaced by an "effective average field," defined as

$$E_{av} \equiv \frac{1}{L_{eff}}\left[\int_0^{L_{eff}-\Delta l} E_{sat}\,dy + \int_{L_{eff}-\Delta l}^{L_{eff}} E_{sat}\cosh(y/l)dy\right] = \frac{1}{L_{eff}}\left[E_{sat}\left(L_{eff}-\Delta l\right)+lE_{sat}\sinh(\Delta l/l)\right]. \quad (4)$$

Since $lE_{sat}\sinh(\Delta l/l) = V_{ds} - V_{deff}$ [3], we have

$$E_{av} = \frac{1}{L_{eff}}\left[E_{sat}\left(L_{eff}-\Delta l\right)+V_{ds}-V_{deff}\right]. \quad (5)$$

Replacing E_{sat} in (2) by (5), it can be shown that (2) becomes

$$I_{dseff} = \left(1+\frac{V_{ds}-V_{deff}-E_{sat}\Delta l}{V_{Aeff}}\right)I_{ds0} \approx \left(1+\frac{V_{ds}-V_{deff}}{V_{Aeff}}\right)I_{ds0} \quad (6)$$

where I_{ds0} is the original one in (2), and

$$V_{Aeff} = \frac{E_{sat}L_{eff}\left[E_{sat}\left(L_{eff}-\Delta l\right)+V_{ds}\right]}{\xi V_{deff}} \approx \frac{E_{sat}L_{eff}\left(E_{sat}L_{eff}+V_{ds}\right)}{\xi V_{deff}} \quad (7)$$

is an *effective Early voltage*, with an added scaling parameter ξ to be obtained by nonlinear regression on the measured $I_{dsat} - L_{drawn}$ data. The elegant part of this formulation is that, although Δl can be a significant portion of L_{eff} for short-channel devices, ignoring Δl in (6) has almost no loss of accuracy in I_{ds} since $E_{sat}\Delta l$ appears as part of the ratio in I_{dseff}, which is confirmed in Fig. 2. This allows the CLM model, which is derived from velocity-overshoot formulation, to have a simple and familiar compact form without the need for "expensive" Δl calculations. The final short-channel I_{ds} model including the effect of S/D series resistance (R_{sd}) is given by

$$I_{ds} = \frac{I_{dseff}}{1+\left(R_{sd}I_{dseff}\right)/V_{deff}}, \quad R_{sd} = R_{ext}+\frac{\upsilon}{V_{gs}-V_t}. \quad (8)$$

where R_{sd} has been derived physically and modeled semi-empirically [8].

III. Results and Discussion

The proposed model has been verified with measured data from a 0.25-μm technology wafer with drawn gate length (L_{drawn}) ranging from 10 μm down to 0.2 μm (W = 20 μm). After extracting the parameters for V_t [4], [5], μ_{eff0} [6], and R_{sd} [8], the CLM parameter (ξ) is extracted by fitting the I_{ds} model [(6)–(8)] to the measured I_{dsat} vs. L_{drawn} data, as shown in Fig. 2, together with V_{Aeff} (with or without Δl). The predicted $I_{ds} - V_{ds}$ curves for three gate lengths are shown in Fig. 3, and compared with the ones without CLM ($\xi = 0$).

This approach of modeling the effective field is somewhat equivalent to "effectively" modeling velocity overshoot [9]. In our model, electron saturation velocity has been kept constant ($v_{sat} = 8\times10^6$ cm/s). In reality, for deep-submicron MOSFET's, electrons in the VSR may experience spatial overshoot (larger than v_{sat}), which is difficult to measure (unless some special structure is designed [10]). Since $v_{sat} = \mu_{eff0}E_{sat}/2$, by modeling an effective E_{av} for E_{sat}, an "averaged" velocity overshoot effect ($\langle v\rangle$) is supposedly modeled by relating to the measured terminal current. With this interpretation, i.e., $\langle v\rangle = \mu_{eff0}E_{av}/2$, a length-dependent velocity overshoot is modeled. As shown in Fig. 4., average velocity can reach ~2×10^7 cm/s for L_{drawn} = 0.2 μm.

The bias- and length-dependent effective Early voltage, together with E_{av} and E_{sat}, are plotted in Fig. 5. Since they are physically derived, the V_{gs}-dependent CLM effect can be modeled, although the parameter ξ is extracted at V_{gs} = 2.5 V. This is shown in Fig. 6 for the L_{drawn} = 0.2-μm device. The extracted ξ = 0.05354 value is a best fit for *all* gate lengths, and due to process/device variations, it may not be optimum for *every* device. As shown, for the 0.2-μm device, a larger ξ (3x) fits better.

Although Δl has been ignored in our simplified V_{Aeff} model, it is fully characterized by (3) for any given device (L_{drawn}, t_{ox}, x_j) and bias conditions (V_{gs}, V_{ds}), which provides physical insights into the device operation, as shown in Fig. 7. The calculated channel field (E_y) for the 0.24-μm device at two V_{gs} values in saturation (V_{ds} = 2.5 V) is shown in Fig. 8. At lower V_{gs}, due to reduced inversion charge, channel electrons saturate ("pinch off") at lower V_{dsat}, giving rise to a larger VSR (Δl), as shown in the inset of Fig. 8. The effective average field (E_{av}), which is the integral of E_y under the intrinsic channel (L_{eff}), increases with decreasing V_{gs}. The physical interpretation of $E_{av}L_{eff}$ is some "effective potential drop" across the intrinsic channel, which is the sum of the voltage drop across the VSR (V_{VSR} =

$V_{ds} - V_{deff}$) and that across the "linear" channel (V_{ch0}). With the extracted R_{sd} and I_{ds} models (8), the voltage drop across the S/D series resistance can be quantified: $V_{Rsd} = I_{ds}R_{sd}$. So, V_{ch0} can be calculated: $V_{ch0} = V_{ds} - V_{VSR} - V_{Rsd} = V_{deff} - I_{ds}R_{sd}$. This is shown in Fig. 9 for all gate lengths at four V_{gs} values in saturation (V_{ds} = 2.5 V). For the 0.24-μm device at $V_{ds} = V_{gs}$ = 2.5 V, $V_{VSR} \approx$ 1.42 V and $V_{ch0} \approx$ 0.67 V, and $V_{Rsd} \approx$ 0.41 V. And from Fig. 4, the ensemble of electrons under the channel travels at an average velocity of ~1.7×10^7 cm/s. The same effective potential drops in linear region (V_{ds} = 0.1 V) is plotted in Fig. 10, which illustrates the physics that has built into the compact model. It can be seen that V_{VSR} is insignificant due to negligible Δl at low V_{ds} (Fig. 7), and V_{Rsd} has a larger contribution at shorter channel length. This is believed to be the first MOSFET compact model that includes such physics-based description of device internal operations with a one-region semi-empirical formulation.

IV. Conclusion

In conclusion, a unified I_{ds} compact model including the effect of velocity overshoot has been developed and verified, which has only one parameter for extraction. CLM in deep-submicron MOSFET's should, in principle, be modeled *microscopically* by "local" velocity overshoot (using, e.g., Monte Carlo), which has been modeled *macroscopically* by the quasi-2D solution of the electric field in VSR, and further *effectively* reduced to an equivalent potential in our simplified model. The bias- and length-dependent behavior has been included in an effective Early voltage. The proposed model has significant application in deep-submicron MOSFET device and circuit modeling.

Acknowledgment

Chartered Semiconductor Manufacturing Ltd. for providing the experimental data for this work is gratefully acknowledged.

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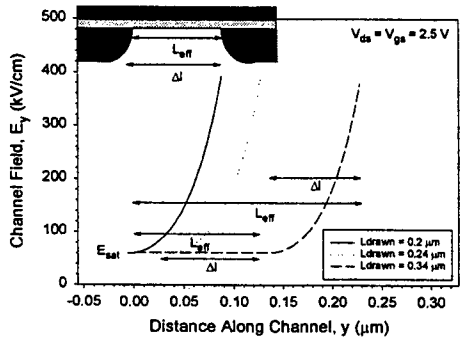


Fig. 1 Channel field from quasi-2D solution for three gate lengths at $V_{ds} = V_{gs}$ = 2.5 V. VSR lengths (Δl) are all calculated based on the extracted model of the actual devices.

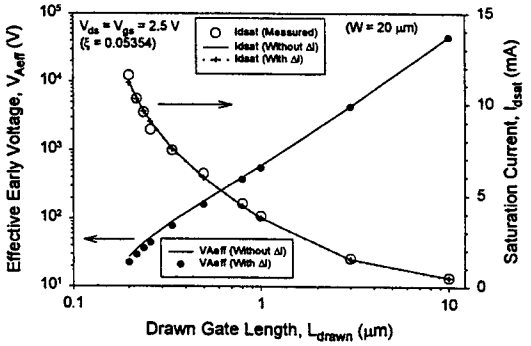


Fig. 2 CLM model with or without Δl fitted to the measured $I_{dsat} - L_{drawn}$ data (*right axis*) using the effective Early voltage (*left axis*). The extracted ξ = 0.05354 (without Δl) is a best fit for all L_{drawn} devices.

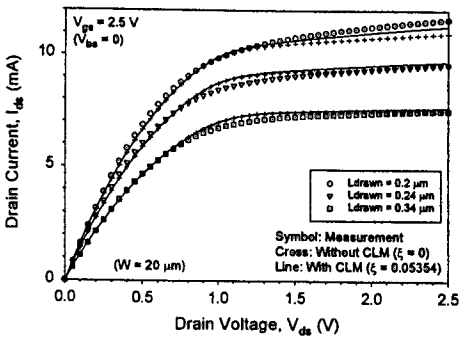


Fig. 3 Measured (*symbol*) and modeled $I_{ds} - V_{ds}$ curves with (*line*) and without (*cross*) CLM for the three devices indicated.

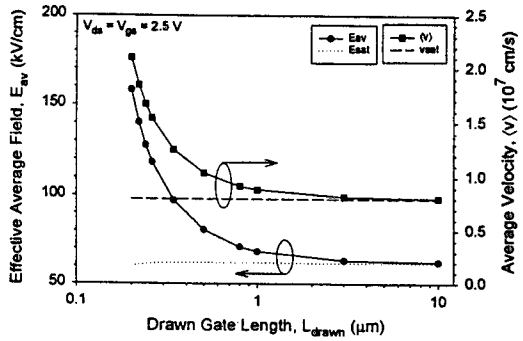


Fig. 4 Modeled average field E_{av} (*left axis*) and average velocity [based on $\langle v \rangle = \mu_{eff0} E_{av}/2$] (*right axis*) against gate length.

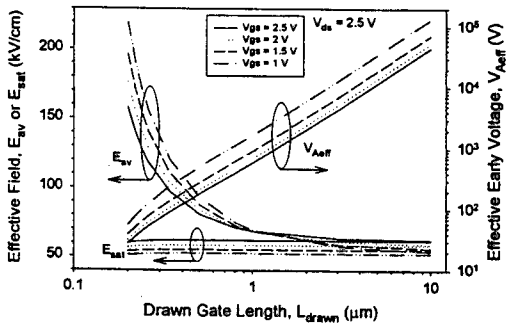


Fig. 5 Length-dependent average field, saturation field (*left axis*), and effective Early voltage (*right axis*) at four V_{gs} values.

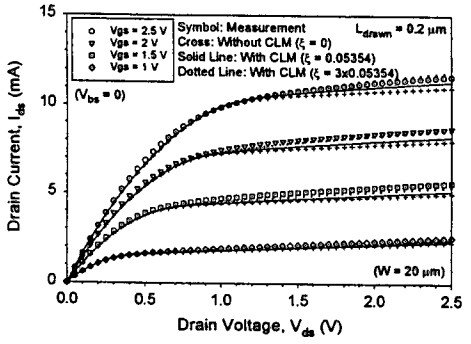


Fig. 6 $I_{ds} - V_{ds}$ characteristics for the 0.2-μm device. *Symbol*: measured; *Solid line*: model (with CLM); *Cross*: model (without CLM); *Dotted line*: model (with ξ increased by three times).

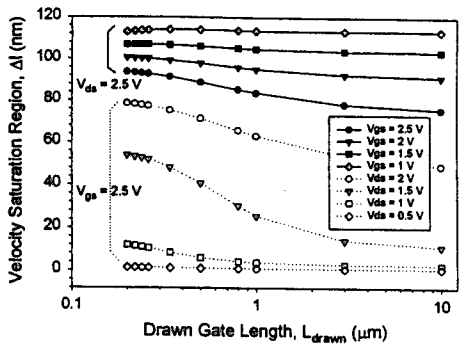


Fig. 7 Calculated VSR length Δl for all gate lengths and biases (V_{ds}, V_{gs}) as indicated.

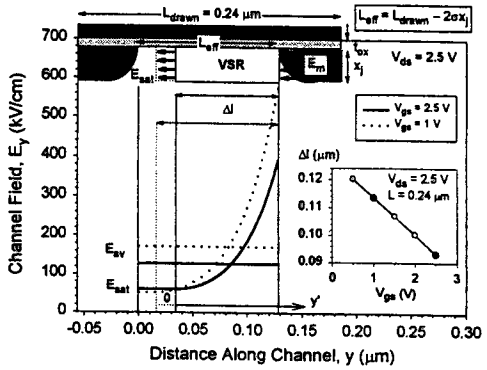


Fig. 8 Calculated channel field and modeled average field for the 0.24-μm device at $V_{gs} = 2.5$ (*solid line*) and 1 V (*dotted line*). The bias-dependent VSR length Δl is shown in the inset.

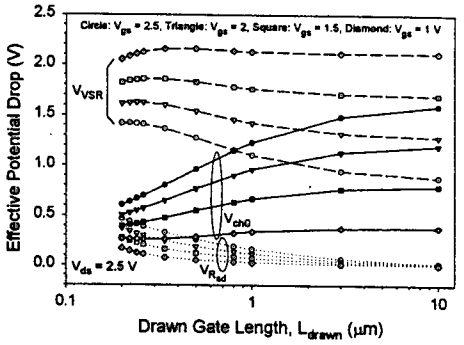


Fig. 9 Length- and bias-dependent effective potential drops across R_{sd} (*open/dotted*), VSR (*open/dashed*), and linear channel (*solid symbol/line*) in saturation.

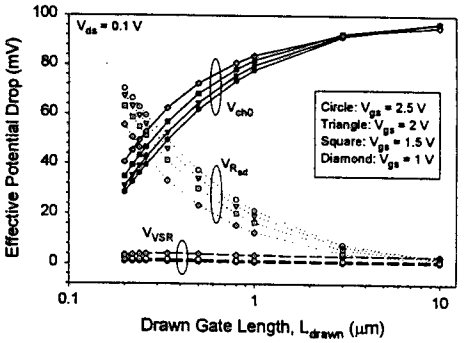


Fig. 10 Length- and bias-dependent effective potential drops across R_{sd} (*open/dotted*), VSR (*open/dashed*), and linear channel (*solid symbol/line*) in linear region.

Full Band Monte Carlo Simulation of Excess Noise Factor in Submicron GaAs p^+-i-n^+ Diodes

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I. INTRODUCTION

Avalanche photodetectors (APDs) is one of the key components on long-haul high-bit-rate optical communication systems because of the internal gain provided by the carrier multiplication through impact ionization. However, the amplification of signal current by impact ionization in an APD also yields addition noise due to the stochastic nature of the avalanche process. This excess noise has been well formulated by McIntyre [1] for long devices, where the electron and hole ionization probabilities can be assumed dependent only on the local electric field, E. According to this theory, low excess noise factors, F are achievable when the electron (α) and hole (β) ionization coefficients are be very different and with the carrier initiating ionization has the larger coefficient. Unfortunately, in most III-V semiconductor materials which are useful for modern optical communication systems display similar α and β at high electric fields. Thus, higher F is expected as the device shrinks in length. However, recently Hu *et al.*[2] have shown experimentally a decrease in F as the multiplication region in GaAs APDs decreases from 0.8μm to 0.1μm, under conditions of pure electron injection. Li *et al.*[3] have performed avalanche noise measurements on a range of GaAs homojunction p^+-i-n^+ and n^+-i-p^+ diodes with 'i' region widths, w ranging from 2.6μm to 0.05μm. These results clearly demonstrate that for $w \leq 1\mu m$, F does not follow the conventional McIntyre's theory which does not depends on the multiplication length. Instead, a continuously decreasing F is observed, for constant mean multiplication, $< M >$ as w is reduced. Moreover, this reduction in F occurs for both electron and hole initiated multiplication in the thinner structures, even though the ionization coefficient ratio is close to unity at the electric fields involved.

It is apparent that the conventional noise model [1], which assumes that impact ionization is a continuous local process and depends only on the local electric field, is not applicable in thin structures. This is because the nonlocal effects such as dead space and drift velocity overshoot become significant in these devices. A newly generated carrier must travel some distance (the dead space) in order to gain sufficient energy from the electric field to enable it to initiate an ionization event. If the dead space distance becomes comparable to the length of multiplication region, the impact ionization probability of a carrier is no longer independent of its history. Thus it is important to use physical device models based on realistic carrier transport physics, such as Monte Carlo models to investigate the avalanche multiplication and noise in thin APDs. In the previous study [4], we used an analytical-band Monte Carlo (AMC) model to perform fast and qualitative studies of the dependence of F on w in thin GaAs APDs. The simulation results are consistent with the experimental measurements [3,4], where F decreases with w (from 1.0μm to 0.05μm) for both the electron and hole initiated multiplication. This low noise behaviour is attributed to the higher operating electric field needed in thin devices, which causes the probability distribution function (PDF) for both electron and hole ionization path

lengths to change from the conventionally assumed exponential shape and to exhibit a strong dead space effect.

II. THE SIMULATION MODEL AND RESULTS

In this work, we used a more advanced MC model which employs a realistic pseudopotential band structure and is therefore able to model high field carrier transport more accurately, compared to the previous AMC model. This full band Monte Carlo (FMC) model is an extension from previous work [5]. In this earlier full band model the Keldysh formula [6] is used to represent the ionization rate above threshold. Since this formula is only strictly applicable for parabolic bands, it does not provide an accurate description of the hardness of the threshold. Thus, in the present version of this model the impact ionization rates for both electrons and holes in the first and second conduction and valence bands are obtained by performing empirical, isotropic power law fits to the first principles calculation of ionization rates of ref. [7] and [8]. The acoustic and non-polar optical deformation potentials are obtained from fits to experimental velocity-field characteristic [9] and data on the ionization coefficient [10]. In the simulation, carriers are injected 'cool' into the high field region and after an ionising collision the excess energy is distributed randomly among the two newly generated carriers and the impacting carrier. The momenta of these carriers are chosen randomly according to the density of state in the first conduction or valence band. This FMC model is very computationally intensive and so simulation is only carried out in a limited number of cases. In these MC simulations $< M >$ and F is estimated in the similar way as described in ref. [4].

The FMC model simulated electron initiated multiplication results are shown as a function of applied bias in Fig.1, for w equal to 0.1μm and 0.2μm and cladding doping density, $p^+ = n^+ = 1x10^{18}cm^{-3}$. The experimental results of Li *et al.*[3] and Hu *et al.*[2] for electron initiated ionization are also shown in the figure for comparison. The discrepancies from the measured results are due to different doping density in the cladding layers ($1\text{-}5x10^{18}$ cm^{-3}) of these devices. For the 0.1μm device, the FMC model result is in good agreement with Hu *et al.* at $< M >$ larger than 3 but predicts a slightly higher value near the onset of the multiplication. This close agreement is because in the 0.1μm device of Hu *et al.* the doping density in the cladding layers is similar to that used in the simulation. However, the model requires a larger applied bias in order to obtain the same $< M >$ value in the 0.2μm device as the results of Hu *et al*, when a different doping density is found in their device ($p^+ = 1x10^{18}$ cm^{-3} and $n^+ = 5x10^{18}$ cm^{-3}). The overall higher doping density in both p^+ and n^+ regions of Li *et al.*[3] measured devices ($\geq 2x10^{18}$ cm^{-3}) reduces the applied bias required for multiplication, although its characteristic is similar to that measured by Hu *et al.*[2]. The excess noise factor, F for each device is given in Fig.2 as a function of mean electron multiplication. Also shown in this figure are the measured results of Li *et al.*[3] and Hu *et al.*[2]. The FMC model successfully predicts the F of the electron initiated multiplication in 0.1μm and 0.2μm devices within the range of measured results. Over the whole range of $< M >$, F decreases as w reduces from 0.2μm to 0.1μm. Although the simulated multiplication characteristics for both devices are close to the results of Hu *et al.*, the predicted excess noise factors are in better agreement with the measurements of Li *et al.* However, the relative reductions in F as w decreases from 0.2μm to 0.1μm in both experimental works and the simulation results are consistent.

III. IONIZATION PATH LENGTH PDF

In order to explain this low noise behaviour in thin devices we use the FMC model to calculate the PDF for electron and hole impact ionization path lengths. These PDFs were calculated by making a histogram of the distance travelled by a single carrier between successive

ionization events and are shown in Fig.3 for electric fields of E = 600kV/cm and 900kV/cm. In general the shapes of these PDFs are similar to that generate from the AMC model [4], the curves start to rise from zero after a certain dead space distance and reach a peak value before they begin to decay almost exponentially to zero. It is evident that the length scales of the ionization path length PDFs for both electron and hole contract at higher fields, corresponding to a more deterministic impact ionization process in thin devices. The spread of the ionization path length distribution narrows because the number of phonon scattering events per average ionization path length decreases at higher fields.

Moreover, at high electric fields the electron and hole ionization path length distributions exhibit a strong dead space effect. In order to investigate the strength of this effect an effective dead space, d^* is defined as the point where the probability reaches half of its peak value. The electron effective dead space is found to be equal to 0.061μm and 0.0368μm for electric fields, E = 600kV/cm and 900kV/cm, respectively. Although d^* is longer at lower field, the ratio of d^* to the corresponding mean ionization path length $<\ell>$ is smaller at 600kV/cm that is 0.48, as compared with 0.60 at 900kV/cm. This shows that the dead space represents a larger portion of the multiplication length in thinner devices. Thus, in thin devices the subsequently generated carriers need to travel a larger fraction of the remaining device length in order to cause an impact ionization. As a result, the subsequently generated carriers are more likely to leave the multiplication region without inducing further impact ionization due to the dead space. Consequently, the length of multiplication chains in thin devices is limited and this therefore narrows the multiplication probability distribution, which results in a lower multiplication noise. Hence, in short devices a lower F is possible for electron initiated multiplication despite the higher feedback from hole ionization, because the fluctuations introduced by higher order ionization process are reduced by the dead space effect.

IV. SUMMARY

In conclusion, the multiplication noise in GaAs p^+-i-n^+ diodes has been investigated using a full band MC model. The model successfully predicts F of the electron initiated multiplication in 0.1μm and 0.2μm devices within the range of measured results. We also used this model to generate the ionization path length PDFs for both electron and hole. It is found that these PDFs become narrower and with relatively larger dead space influence at high electric fields which are the reasons for low noise behaviour in thin devices. Thus these simulations confirmed the previous findings using a relatively simple analytical-band MC model. Hence, a low noise and high speed APD structure is achievable, even with materials having similar electron and hole ionization coefficients, by utilising a submicron multiplication region to enhance nonlocal ionization behaviour.

ACKNOWLEDGEMENTS

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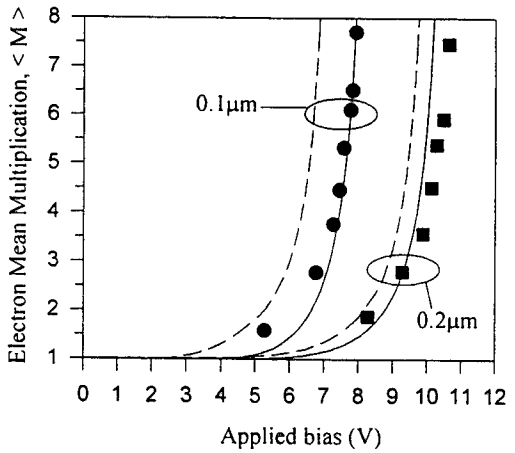


Figure 1: Mean electron multiplication as a function of applied bias. The symbols represent the FMC simulated results and the lines are measurements of Hu *et al.* [2] (solid lines) and Li *et al.* [3] (dashed lines). The discrepancies in the experimental results are mainly due to different doping densities in the cladding layers.

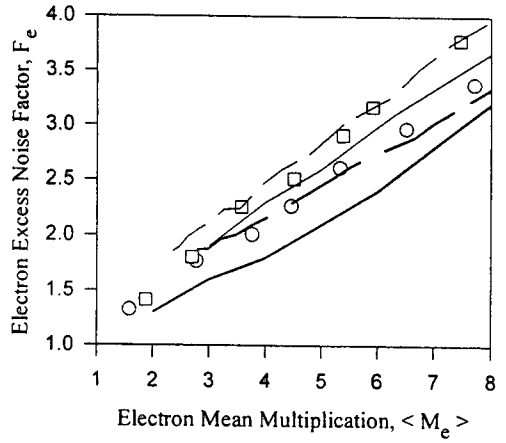


Figure 2: The excess electron noise factor as a function of mean multiplication. Symbols are the FMC simulated results and the lines are experimental measurement of Hu *et al.* [2] (solid lines) and Li *et al.* [3] (dashed lines). The bold and normal lines represent the 0.1μm and 0.2μm devices, respectively.

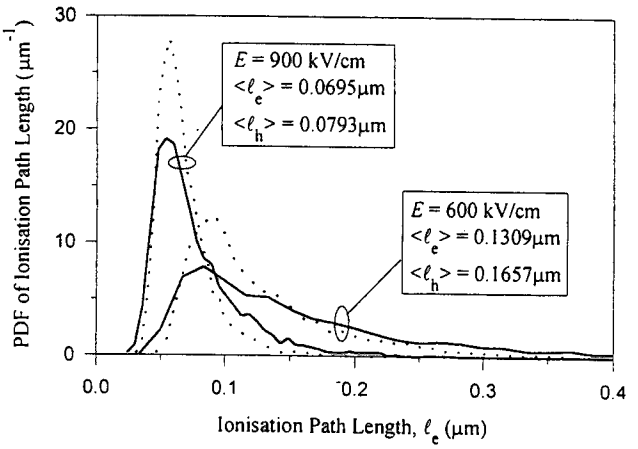


Figure 3: The FMC simulated electron (dotted lines) and hole (solid lines) ionization path length PDFs. The corresponding electron and hole mean ionization path lengths are represented by $< \ell_e >$ and $< \ell_h >$, respectively.

Narrow Channel Effect on Current-Leakage and Hot Carrier Reliability of SOI MOSFET's *

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In view of the increased interest of SOI technology for low power applications, the study and control of leakage current (DIBL, GIDL, etc) is of particular interest. As a result, several authors have studied the underlying leakage current mechanisms, as they relate to various isolation technologies. In addition, it has been found that hot carrier stress and floating body effects can affect the leakage current. With the advent of shallow trench isolation (STI) technologies it has become possible to reduce the channel width down to submicron ranges, and there has been an increased interest lately to understand the implications on device reliability and performance. In this talk we will examine the width dependence of the hot carrier degradation and of the off-state (leakage) current in SOI MOSFET's bearing in mind that the floating body effects (FBE) are expected to be less [1] and the GIDL leakage current more [2] important in PMOSFET's than NMOSFET's.

A SOI CMOS process [3] with implanted N and P wells was used to fabricate partially depleted (PD) N^+-polysilicon gate surface NMOS and buried channel (BC) PMOS transistors with LDD structures. The gate oxide, silicon film, and buried oxide thickness were equal to 10nm, 0.23μm, and 0.38μm, respectively and the channel doping $3x10^{17}cm^{-3}$. Planarized STI self-aligned the body-ties surrounding the active areas. The gate polysilicon and source/drain areas were silicided using titanium salicide processing. The DIBL and GIDL currents were measured as a function of channel width in the range 0.8-10μm and channel length down to 0.35μm. Care was taken to separate DIBL and GIDL on the basis of their channel length (Fig.1) and voltage dependence. Unless otherwise stated, the results shown below refer to PMOSFET's. Fig.2 shows the width dependence of DIBL and GIDL, as measured by their corresponding λ parameters (defined in the figure). It is seen from this figure that both DIBL and GIDL are reduced significantly with the channel width. The situation is different in Fig.3, where it is seen that the single transistor latch-up voltage V_{DLU} increases with decreasing channel width. Finally, the hot carrier degradation performed under maximum gate current stress at V_D=-7V (i.e., under weak impact ionization) is seen from Fig.3 to be more severe for narrower devices. For comparison, Fig.4 also shows the hot carrier degradation of a similar NMOSFET, stressed with its gate voltage near threshold and V_D=5V. There are important similarities as well as differences between the above results and similar measurements on NMOSFETs [4][5].

To explain the results, as well as the similarities and differences, it is important to consider that FBE are more prominent in NMOSFETs than in PMOSFETs [1] as well as the technological differences between the two devices [3]. The device design and process step sequence is such [3] that Boron out-diffusion/redistribution takes place near the S/D edges. This results in what might be considered a sort of "pseudo body-ties": narrow sections of the S/D to body junctions, adjacent and parallel to the channel edges along the gate of reduced built-in potential barriers. The effect is not unlike the lightly doped source (LDS) concept described in [1] for FBE control. This both "dampens" the FBE and reduces the band bending in the G/D overlap (and thus GIDL) for the narrower devices [Fig.2]. This idea can also explain Fig.4, where the reduced FBE significance in the narrower devices is reflected by the increasing V_{DLU} values. The DIBL (Fig.2) measurement was taken below the voltage level for which FBE are important, but it can be explained by considering that the edges of the drain are LDD-like, leading to increased DIBL currents in the narrower devices. With regard to hot carrier degradation (Fig.4), under the PMOSFET stress conditions FBE are not very important, and narrow channel devices degrade more than wide channel devices, just as the bulk case [6]. The situation is different for the NMOSFET's, where under the stress conditions at hand FBE are important, leading to decreased degradation for the narrow-channel devices. This had been previously observed and explained through 2D simulation results according to which there is more impact ionization at the edges of the wider-channel device [4][5]. It can now also be explained by the reduced relative significance of the FBE in the narrow-channel devices brought about by the "pseudo-body-ties", a result of thew Boron out-diffusion. This agrees with 3D simulations, to be presented at the conference.

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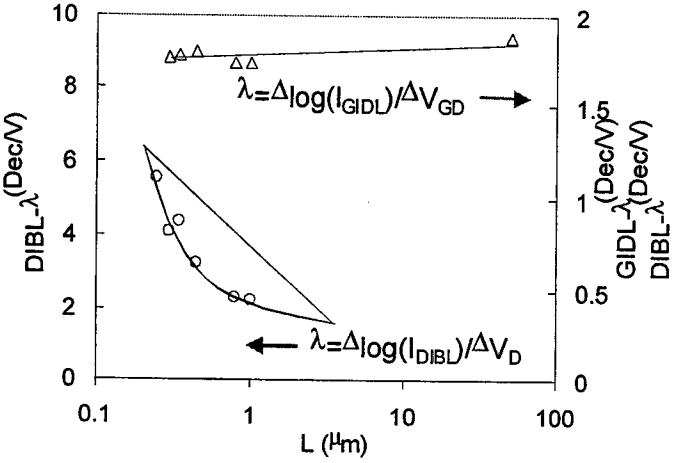


Fig. 1: DIBL-λ and GIDL-λ change with length. DIBL measured at V_{G1}=Vs= 0V; GIDL measured at V_{G1}= 4V, Vs floating. Both with body floating and V_{G2}=0V. W=10μm.

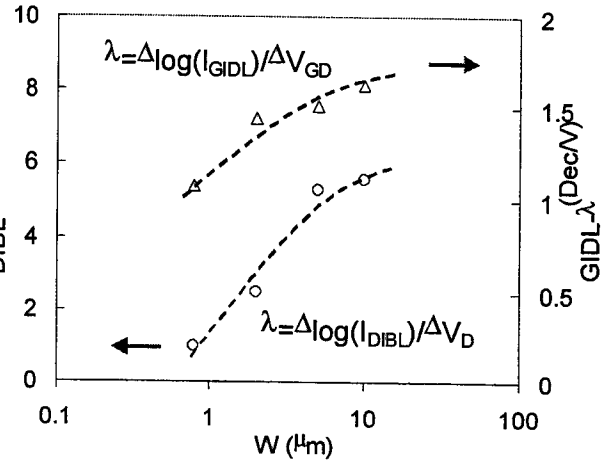


Fig. 2: DIBL-λ and GIDL-λ decrease with width. DIBL measured at V_{G1}=Vs= 0V; GIDL measured at V_{G1}= 4V, Vs floating. Both with body floating and V_{G2}=0V. L=0.35μm.

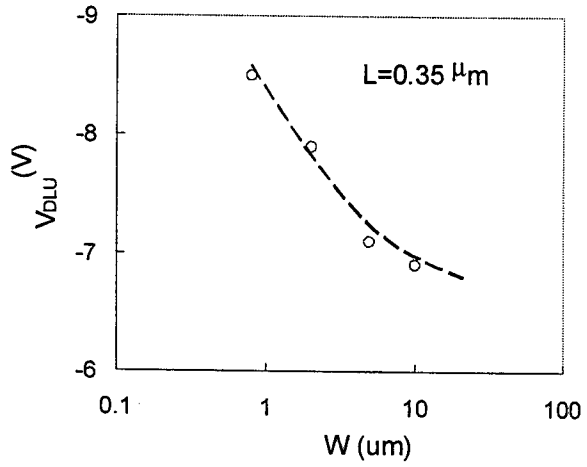


Fig. 3: The single transistor latch-up voltage V_{DLU} increases with decreasing width, indicating a "dampening" of FBE in narrower devices.

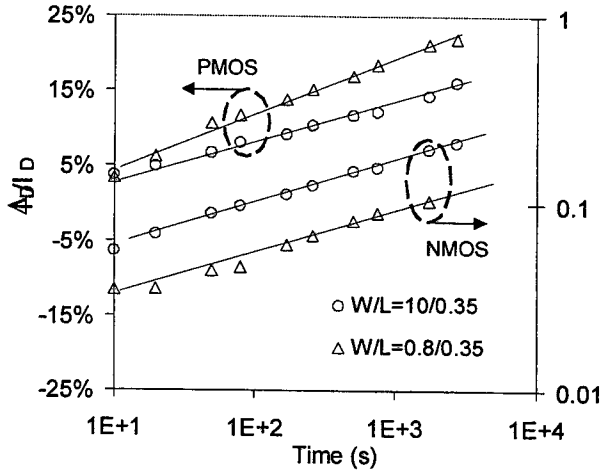


Fig. 4: Linear drain current degradation against stress time. Stress Conditions: PMOS, V_D= -7V, V_{G1} at maximum I_{G1}; NMOS, V_D= 5V, V_{G1} at V_{T1}. Both with body floating.

SOI Technology Applied to an Advanced Smart Power Structure

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Abstract

A localized SOI (Silicon On Insulator) structure for electric insulation between High Voltage Integrated Circuits and their control devices, using LEGO (Lateral Epitaxial Growth over Oxide) Technology is presented in this paper. This structure is composed of both a vertical and a lateral junction insulation. A modeling of the insulation performance of the structure is first given. Then, a method of making the vertical localized insulation and the corresponding experimental results including crystallographic analysis, are presented.

Introduction

An important issue of the integration of High Voltage (> 400 V) Integrated Circuits (HVIC) is the coexistence of the high voltage part with the low voltage circuits on the same chip. Dielectric insulation solves this integration problem. However, the above application requires substrates with both localized and thick SOI layers (see Fig.1). The existing techniques for making such structures are expensive while yield has still to be improved.
We present in this paper a method for the formation of this localized buried oxide at low cost. This method can be part of a standard process. It is based on the recrystallization of a thick polysilicon layer by Lateral Epitaxial Growth over Oxide (LEGO). The LEGO technique has been previously developed by Celler et al [1], but was not appropriate at that time for the VLSI requirements. Recently, LEGO was used for solar cell processing by Eyer et al [2].

Modeling of the electric insulation of SOI structures

The proposed insulation scheme is presented in Fig.1: the power transistor takes place in the bulk N^- substrate and the control circuitry is embedded in the SOI layer which is N^- doped. The control circuit area has both a vertical dielectric insulation and a lateral junction insulation provided by the buried oxide and by the deep heavily P^+ doped diffusions respectively.
Two-dimensional device simulations using ATLAS software have first been performed to demonstrate and assess the static electrical behaviour of the vertical (SOI) and lateral insulation structures, and then to identify the critical parameters of the process, such as the influence of geometrical parameters on the recrystallization phase.
At that stage, two different junction insulations structures are conceivable: a non overlapping well, i.e. a well diffused only above the oxide (Fig.2a) and an overlapping well, i.e. a well diffused around the buried oxide layer edges (Fig.2b).
However, the structure depicted in Fig.2a leads to a parasitic upside down nMOS transistor made up of the bulk substrate (gate/drain), the buried oxide (gate oxide) and the bottom of the P^+ insulation well (substrate) [3]. When the N^- substrate (gate of the MOST) voltage is increased (both P^+ insulation well and N^- SOI region are grounded) a leakage current flows

(the parasitic MOST is turned-on) between SOI region (source) and substrate (drain) (see Fig.3). This parasitic effect is completely avoided by the overlapping junction (Fig.2b) as shown by the results of Fig.3. It is worth mentioning that because of the doping distribution in the P^+ well of the non overlapping junction (Fig.2a) which is abruptly stoped by the buried oxide, the P^+/N^- junction avalanche breakdown voltage is lower than the one of the overlapping junction, giving an additional benefit to the structure depicted on Fig.2b. The simulation results also show (Nolhier et al [4]) that, due to the presence of the reverse biased P^+/N^- junction (see Fig.4a) in parallel with the MOS capacitor formed by the buried oxide, a deep-depletion mode is always achieved. This phenomenon is called self-shielding. When a high voltage bias is applied to the substrate, the major voltage drop is located in the bulk silicon under the N^- insulated region (see Fig.4b). In that way the buried oxide is protected from high electric field, its thickness is not a critical parameter and its reliability is improved.

Experimental setup for SOI structures

The technique chosen to form the localized SOI islands is the recrystallization of a deposited polysilicon layer over the oxide, from crystal seeds which will become the power transistor areas. The recrystallization is carried out using a specifically designed Rapid Thermal Processor RTP (Fig.5) which allows to melt the SOI layer only, and then to recrystallize it from the adjacent crystal seed. The RTP (Fig.5) is made of a single row of 15 tungsten halogen lamps ① cooled by forced convection and suspended below a water-cooled reflector ⑥, on one side. A black water-cooled base on the other side acts as a radiative heat sink ④. A quartz support prolongated by an axis ⑤ holds the wafer ③ and allows a rotating movement to uniformize the wafer temperature. Quartz windows ② allow to control the processing atmosphere.
The radiative heat sink, coupled to the halogen lamp row, provides a temperature gradient between the back and the front surfaces of the wafer of about 5K. The heat sink absorbs the radiations emitted by the non illuminated surface (backside) of the wafer. This gradient is an important parameter to the LEGO process, and is sufficient to keep solid the bulk silicon while the polysilicon surface is molten. The power supplied to the lamps can reach a maximum of 90kW. The power vs. time cycle is microprocessor controlled and monitored.
The starting materials are 4" Si (100) 500 µm thick wafers. A thermal oxidation provides 1 µm thick oxide layer. A photolithography permits to pattern the oxide into square and rectangle islands with different sizes. The islands are separated by a wide enough crystal seed area, which will become the substrate of the power transistor (see Fig.1). Dimensions of the seed area vs. dimensions of the oxide islands were determined previously by thermal simulations. A deposition of a thin polysilicon by LPCVD, followed by an epitaxial growth at high temperature and atmospheric pressure results in a polysilicon layer of 10 to 50 µm thick to be grown over the oxide layer (Fig.6). The wafers are finally encapsulated by an oxide layer to prevent the molten silicon from evaporating during the annealing.
A typical thermal cycle was previously presented by Dilhac et al [3]. An annealing cycle is composed of 3 parts: a lamp power ramp up to a sufficient value for starting the melting of the polysilicon layer over the oxide, then a power plateau which provides the extension of the molten silicon in depth and wideness, finally a lamp power ramp down to zero which permits the recrystallization of the SOI from the seed to the center of the pattern.

Experimental results for the SOI structures

A cross-section of a SOI structure is shown in Fig.7. Schimmel solution [5] was used to reveal crystal grains. Fig.7 is to be compared with the as deposited cross-section of Fig.6 showing numerous small size grains. RTP provides a single crystal zone on the order of 50 to 100 µm from the seed area for 10 µm thick polysilicon films. Further away from the

seed there are still grains of an average 30 μm width. A crystallographic analysis has been made on these two recrystallized regions. This analysis technique consists in a silicon etching through a circle, that gives a square shape if the substrate is (100) oriented, and a triangle shape if the substrate is (111) oriented. The etching results showed squares in single crystalline recrystallized region all oriented in the same direction as in the seed area, and squares misoriented one from each other in large grains area: the large grains are in the (100) orientation but all in different directions from the seed one.
As a result, narrower SOI structures were designed, with the objective of forming single crystal. Fig.8 shows two oxide lines of 100 μm wide: Fig.8a shows the SOI structure as deposited, Fig.8b represents the structure after annealing. There is obviously no more grain in the SOI regions.
An electrical test by spreading resistance analysis was also made: neither the silicon under the buried oxide layer nor the silicon in the seed area and the recrystallized silicon were contaminated by the oxide layer (clusters of oxygen atoms) during RTA. The achieved recrystallization of 10 μm thick polysilicon over 100 μm wide oxide patterns is therefore suitable for device processing.

Conclusion

The simulation results have shown the good insulation performance of our SOI high voltage structure. On the other hand, experimental results have shown that the recrystallized area may have similar physical characteristics to the bulk substrate ones and should be able to receive performing devices. More precisely, single crystal has been obtained with 100 μm wide SOI layers.
Consequently, our future objectives will be first to determine the maximum width of the oxide patterns vs. the polysilicon (SOI) and oxide thicknesses, and then to experimentally assess the voltage handling capability of our structures.

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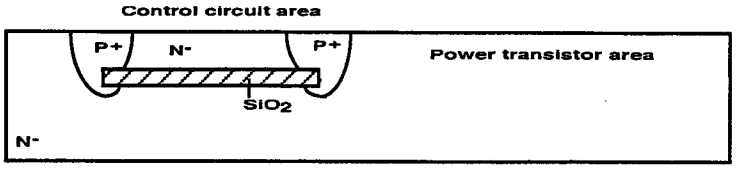


Figure 1: Proposed HVIC structure.

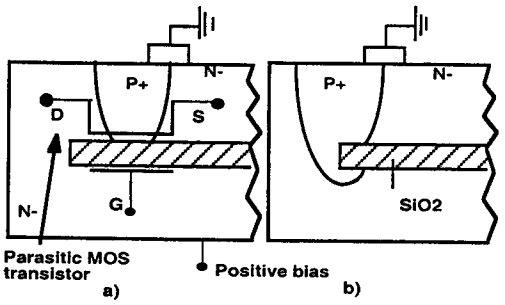


Figure 2: Two different insulation junctions: a) non overlapping well showing parasitic MOS ; b) overlapping well.

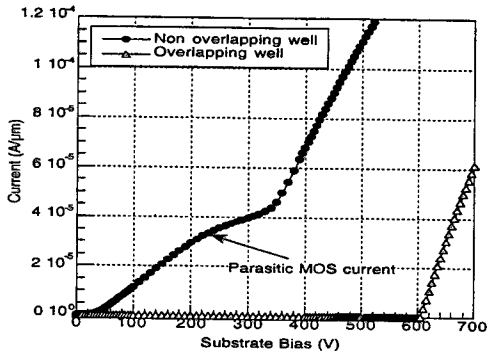
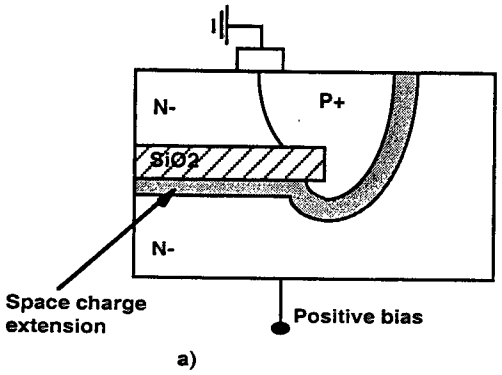


Figure 3: Substrate current vs. substrate bias for overlapping and non overlapping wells.



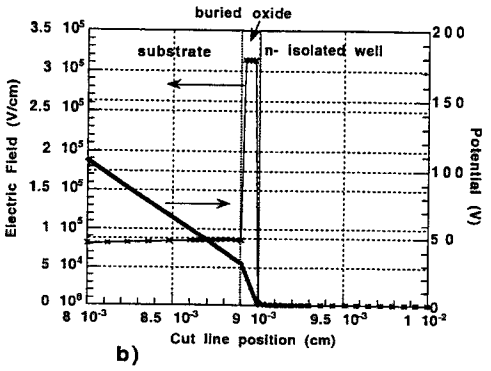


Figure 4: Self shielding phenomenon:
a) principle ; b) example of potential and electric field distributions.

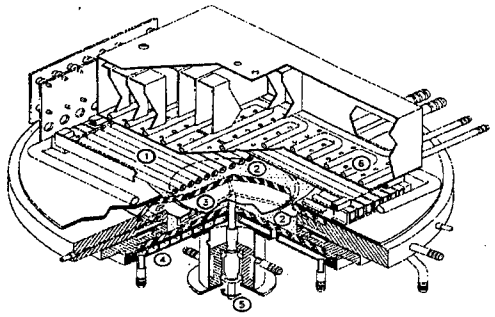


Figure 5: Rapid Thermal Processor (see text for details).

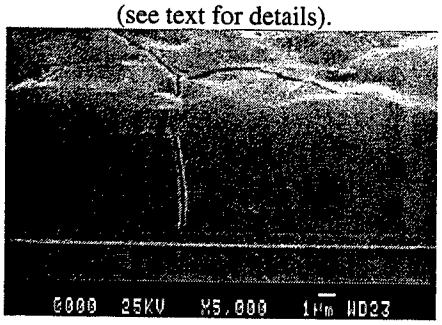


Figure 7: Cross section of the SOI structure afer the RTA
(SEM photograph after Schimmel etch).

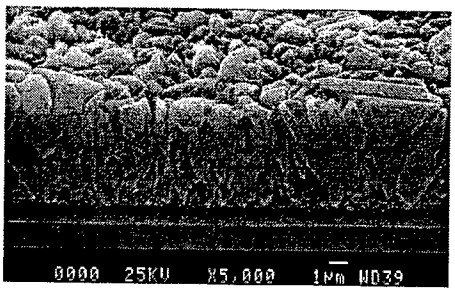


Figure 6: Cross section of the SOI structure as deposited
(SEM photograph after Schimmel etch).

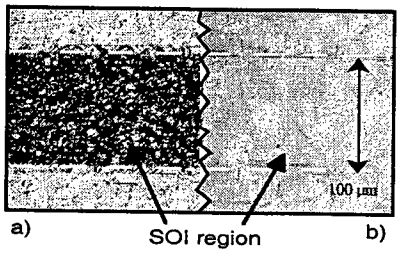


Figure 8: Comparison between
a) SOI structure as deposited and
b) SOI structure after annealing
(top views after Schimmel etch)
The white dotted line has been added to identify the SOI area.

A Novel FDSOI Device Design for Ultra Low Voltage Applications *

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1 Introduction

The Fully Depleted Silicon-On-Insulator (FDSOI) technology has been recognized for its ideal subthreshold slope, small parasitic capacitance and complete isolation. It has been regarded as the ideal candidate for low power, high speed, applications. Moreover, conventional FDSOI devices can be designed with the same concept used in a bulk Silicon technology, such as the dual poly (n+/p+ polysilicon for n/p channel MOSFETs) gate design with high channel doping. The potential of FDSOI scalability to the submicron region has been demonstrated by scaling the SOI film thickness [1], t_{si}, and buried oxide thickness [2], t_{box}. However, the use of conventional FDSOI becomes questionable when an ultra thin (10nm) SOI film is desired in short channel devices because the threshold voltage V_{th}, for the conventional FDSOI design, is very sensitive to t_{si} and the channel doping density, N_{ch}. This work reports on a novel design concept for FDSOI CMOS devices, where the V_{th} of these devices displays very little dependence on N_{ch} and very low sensitivity to t_{si}, when compared to the conventional design.

2 Design Principles

The threshold voltage of a thin-film long channel Fully Depleted (FD) enhancement-mode n-channel SOI device can be derived by solving Poisson's equation, using the depletion approximation. The relationship between the front gate voltage and surface potentials at both interfaces is given by [3]:

$$V_{G1} = \phi_{GS1} - \frac{Q_{ox1}}{C_{ox1}} + (1 + \frac{C_{si}}{C_{ox1}})\phi_{s1} - \frac{C_{si}}{C_{ox1}}\phi_{s2} - \frac{\frac{1}{2}Q_{depl} + Q_{inv1}}{C_{ox1}} \quad (1)$$

where ϕ_{GS1} is the workfunction difference between gate and semiconductor, $C_{si} = K_{si}\varepsilon_o/t_{si}$ and Q_{depl} is the total depletion charge in the silicon film, which is equal to $-qN_At_{si}$.

In the case of volume inversion [4], $\phi_{s1} \simeq \phi_{s2} \simeq 2\phi_F$, the threshold voltage V_{th1} becomes

$$V_{th1} = \phi_{GS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (2)$$

for $Q_{inv1} = 0$.

(a) Conventional Design

As shown in Figure 1a, the conventional FDSOI design has a heavily doped dual-poly gate device, with a very thin gate oxide and a highly doped channel. We may assume $\phi_{GS1} \simeq -2\phi_F$, $Q_{depl} = -qN_At_{si}$, $Q_{ox1} = 0$, to simplify V_{th1} as

$$V_{th1} \simeq \frac{qN_At_{si}}{2C_{ox1}} \quad (3)$$

*Supported by DARPA, Northrop Grumman Science and Technology Center, and the Sherman Fairchild Foundation

We can see clearly the dependence of threshold voltage on the Si film thickness, t_{si} for FD dual-poly gate SOI devices, which makes it extremely difficult to have good threshold voltage uniformity with film thickness fluctuations. Thus, even with so many distinctive advantages, FD SOI devices have lost their attractiveness to industry [5]. In order to fully utilize the unique advantages of the FD SOI devices, a solution must be found to reduce the dependence of threshold voltage on the Si film thickness.

(b).Midgap Gate Design

As shown in Fig. 1b, midgap metal gate and intrinsic epitaxy channel doping are used for both NMOSFET and PMOSFET devices. The gate to semiconductor workfunction difference $\phi_{GS1} \simeq -\phi_F$, and the threshold voltage now can be simplified as

$$V_{th1} = \phi_F + \frac{qN_A t_{si}}{2C_{ox1}} \simeq \phi_F = \frac{kT}{q} ln(\frac{N_A}{n_i}) \tag{4}$$

We can now reduce the channel doping $N_{ch} = N_A$, to set the threshold to a convenient value. For a 30 nm Si film, 3 nm gate oxide, and $N_A = 10^{15}/cm^3$, the second term only gives 0.2 mV, which is much smaller than $\phi_F(0.3V)$. This means the threshold voltage can be symmetrically set by the Fermi potential ϕ_F for both NMOSFET and PMOSFET devices with the channel doping as low as $10^{15}/cm^3$. Thus, the dependence of the threshold voltage on film thickness and the channel doping is reduced significantly as compared with the dual-poly case. Besides, the reduction on channel doping may increase the channel mobility due to the reduced surface electric field.

3 Results and Comparison

In order to remove the influence of the short channel effect, the channel length is selected to be $1\mu m$. The design target of V_{th} is set at 0.3V with 5 decades of I_{on}/I_{off} for low voltage application. With the midgap gate design, the V_{th} is automatically set around 0.3V with channel doping 1 x $10^{15}/cm^3$. While for the poly gate design, the channel must be heavily doped up to 3 x $10^{18}/cm^3$. All the devices have a fixed 3nm gate oxides and either a fixed channel doping (for thickness sensitivity) or a fixed film thickness (10nm, for doping sensitivity). Simulation results of the subthreshold chracteristics of both the conventional FDSOI devices and midgap gate FDSOI with thickness variation and channel doping variation are shown in Figs. 2a and 2b, respectively. The workfunction of midgap gate is set at 4.67eV. Fig. 3 shows the extracted threshold voltage V_{th} using linear-extrapolation method at low drain voltage (50mV). The sensitivity of V_{th} for midgap gate design is extremely small, 1% compared to the 33% for the conventional design for 25% thickness variation. V_{th} sensitivity to the variations of the channel doping density, N_{ch}, is shown in Fig. 3b. Again, the midgap gate design shows very little dependence on N_{ch}, 1% compared to 66% for the conventional design. Fig. 4 shows the sensitivity of midgap gate design with 125nm channel length. It can be seen that the sensitivities to both t_{si} and N_{ch} are as small as that in the long channel case in spite of the short channel effect, which can be limited by halo implantation. Drain Induced Barrier Lowering (DIBL) is shown to be about 0.1V/V for 125nm channel length devices. All the simulations have been performed with Silivaco Atlas without quantum considerations. However, the huge difference in terms of V_{th} sensitivity demonstrates the new design is superior to the conventional design for low power, high speed applications.

4 Conclusion

In conclusion, we have proposed a novel FDSOI CMOS device design concept based on a midgap workfunction gate, which demonstrates excellent immunity to variations of SOI film thickness and channel doping density. This approach is preferred over the conventional design with highly-doped poly gates and highly-doped channels, when devices are considered for ultra low voltage, low power, high speed, SOI circuits applications.

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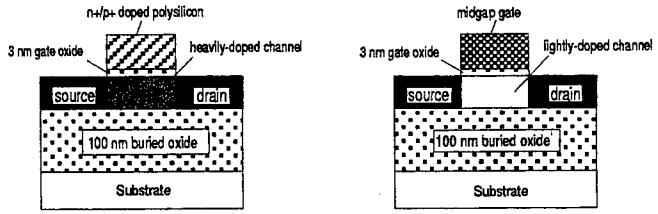
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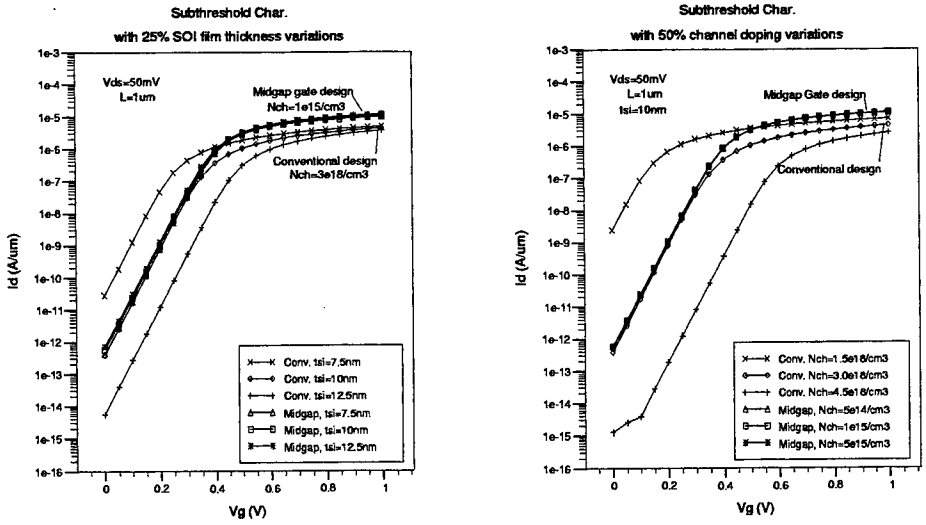
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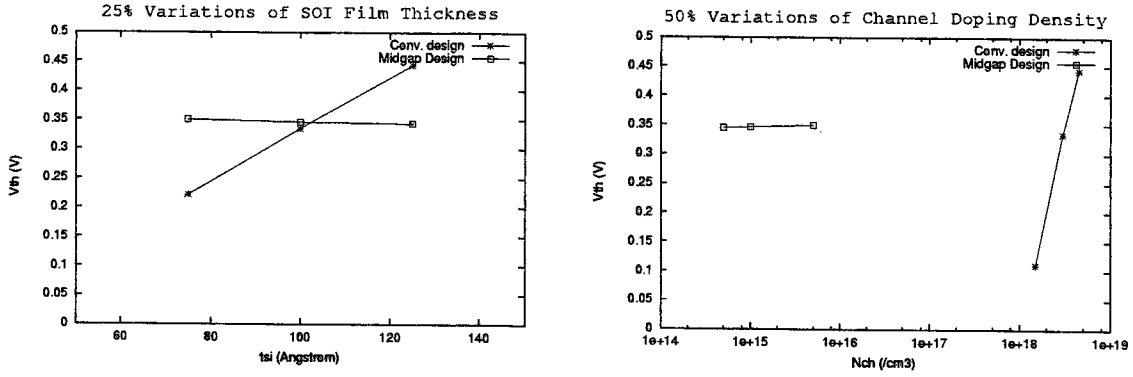
(a) Conventional design (b) Midgap gate design

Figure 1: Conventional FDSOI Design vs. Midgap Gate Design



(a) Sensitivity to tsi (b) Sensitivity to Nch

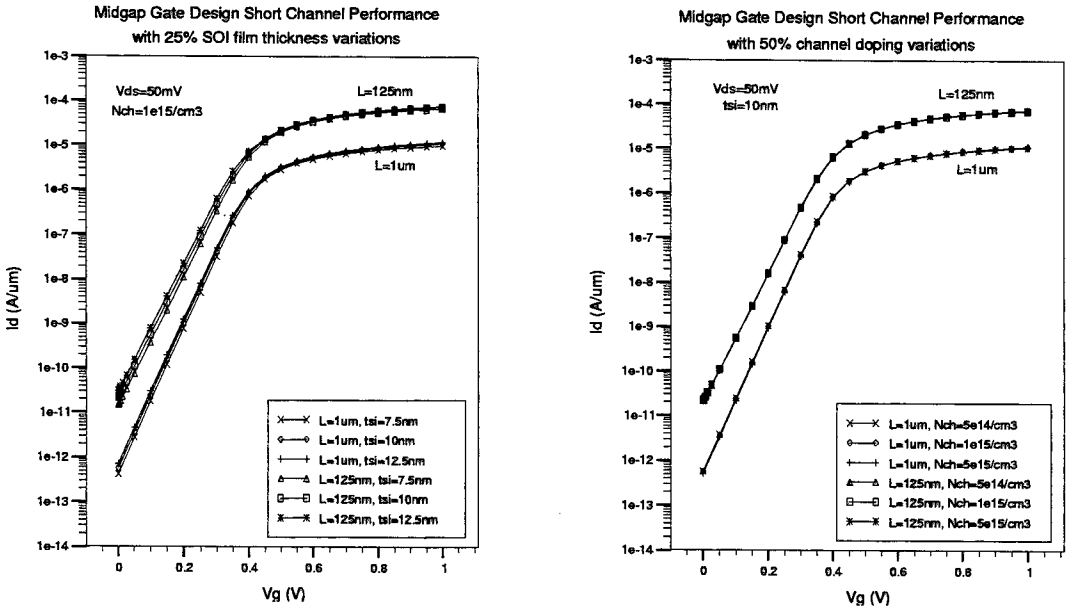
Figure 2: Sensitivity Comparision of Midgap Gate Design to Conventional Design



(a) Sensitivity to t_{si}

(b) Sensitivity to N_{ch}

Figure 3: Variations of Threshold Voltage Determined by Linear-extrapolation of I-V Characteristics



(a) Sensitivity to tsi

(b) Sensitivity to Nch

Figure 4: Sensitivity of Midgap Gate Design with Short Channel Length

Deep-Submicron DC to RF SOI MOSFET Characterization and Modeling

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Abstract-We present a submicron RF SOI MOSFET model based on a complete extrinsic small-signal equivalent circuit and an improved CAD model for the intrinsic device. The delay propagation effects in the channel are modeled by splitting the intrinsic transistor into a series of shorter transistors, for each of which a quasi-static device model can be used. The model has been validated for frequencies up to 25 GHz and effective channel lengths down to 0.16 μm.

Introduction

Thin-film short-channel SOI MOS technology appears to be a good candidate for low-power microwave circuits because of its excellent performance in terms of gain, speed and cutoff frequency [1,2]. Therefore, there is a need for an accurate submicron RF SOI MOSFET model with adequate non quasi-static extensions. The present standard MOSFET models for circuit simulation, such as BSIM3v3, are not accurate enough in high-frequency operation [3], because they do not properly include nor the extrinsic elements and neither the intrinsic non quasi-static effects (which arise because of the channel propagation delay), and because of their poor fitting and scaling of the intrinsic device transconductance and output conductance, which critically affect the gain and the S-parameters. As a result, these standard models can be used for frequencies up to a few GHz [3,4] only, and with the restriction of a small range of channel lengths and bias conditions.

Model Description

Our new model is based on the equivalent circuit shown in Fig. 1-3. This equivalent circuit is an enhancement of our previous one [2], in order to combine accurate extrinsic and intrinsic circuit models to deal both with the complex SOI substrate behaviour and with narrow channel device effects. In our analysis we have used the three-terminal small-signal equivalent circuit shown in Fig. 2 (a common-source configuration). This equivalent circuit is especially valid in the microwave frequency range, where the SOI MOSFET behaves as a three-terminal device, and the back gate potential is capacitively controlled by the source and drain diffusions [2]. This approach modifies the physical meaning of several equivalent circuit elements, but in a small proportion. In this small-signal equivalent circuit (Fig. 2) the channel propagation delay, is taken into account using the intrinsic gate resistances, R_{GSI} and R_{GDI}, in series with the intrinsic capacitors, C_{GSI} and C_{GDI}, respectively, and a delay τ in the transconductance term. The exact distributed nature of the gate resistance is accounted for by performing a careful small-signal analysis. We found that the small-signal propagation effects along the gate width can be accurately modeled by inserting an effective resistor, R_{GE}, in series with the gate terminal, and an effective capacitor, C_{GE}, in parallel with R_{GE}. The values of both elements significantly depend on the gate width. The value of R_{GE} is found to be $R_{GE} \approx R_{tot}/3$ [2] (where R_{tot} is the total gate resistance), and the value of C_{GE} is determined as $C_{GE} \approx C_g/5$ (where C_g is the total gate capacitance) [5].

Our large-signal intrinsic SOI MOSFET model for the circuit simulators has to reproduce the equivalent circuit of Fig. 2 in small-signal RF conditions. In order to account for the channel propagation delay effects, the channel of the transistor is split into several smaller sections along the channel length where quasi-static conditions are fulfilled and a quasi-static model can be applied. This approach is also valid for large signal simulation. Regarding delay effects, the accuracy of the model becomes better by increasing the number of these smaller transistors, but the computation time also increases. Furthermore, the DC equations must remain valid for the smallest subsections which may be hard to achieve for section lengths below 0.05 μm. A tradeoff between accuracy and computation time is thus necessary. We have found that the splitting of the channel into three sections is a good choice.

In each transistor we use the expressions of the quasi-static drain current and charges given by a new submicron fully-depleted SOI MOSFET model we have developed. This model is an extension of our previous model [6] to the deep-submicron regime, and it has been validated for channel lengths down to 0.16 μm. The model looks very adequate for the RF equivalent circuit, because it has the advantages of being physics-based,

scalable, charge conserving and infinitely continuous through all operation regimes, and accurately predicts the values of the intrinsic DC and small-signal parameters. The drain current and charge equations are written in terms of continuous expressions of the inversion charge densities at the source and drain ends of the channel; therefore, the same parameters can be used in all the equations. The most important short-channel effects are included using continuous equations: velocity saturation, channel length modulation, charge sharing and DIBL. We also account for relevant effects in deep-submicron technologies, neglected in standard models: quantum effect on the effective gate oxide thickness, short-channel effects in the charges, impact ionization at high lateral fields and adequate scaling. This is of great importance to allow channel splitting into sections of lengths smaller than 0.1μm. This model has been implemented in the ELDO circuit simulator and tested by simulating some benchmark circuits.

Extraction Procedure

The parameters of the model used for the intrinsic transistors are extracted in DC conditions by combining direct algorithms with global optimization [6]. In Fig. 4-6 we show comparison of the measured and modeled DC characteristics (drain current and output conductance) of deep-submicron transistors of two film thicknesses. These transistors come from a 0.25μm process developed in LETI. The front and back gate oxide are, respectively, $t_{of} = 4.5$ nm and $t_{ob} = 400$ nm. Impact ionization effects are not negligible for a film thickness of $t_b = 40$ nm, causing an increase of the DC output conductance as the drain voltage is increased in the moderate saturation regime (Fig. 6), but they are practically suppressed for $t_b = 30$ nm, since the depletion of the film is much better (Fig. 5).

The extrinsic elements are extracted from measurements of the S-parameters using a new parameter extraction scheme. To obtain the values of the parameters taking into account the distributed nature of the gate resistance, the transistor is split along the width into seven narrower transistors in the extraction procedure. The geometry dependences of the extrinsic parameters are also determined.

Discussion

In Fig. 7-10 we compare the measured magnitude and phase of the S-parameters with the ELDO simulations using our RF equivalent circuit with the new submicron SOI MOSFET model for the intrinsic device. The measured transistors come from the 0.25μm LETI process mentioned above, with $t_b = 30$ nm, and they consist of 16 fingers of 6.6 μm-width each. As we can see, the splitting of the channel length into three sections improves the accuracy, because the propagation delays are taken into account, which are not negligible even in channel lengths as short as 0.16 μm. The agreement is in general good in the whole frequency range and the relative error is smaller than in standard models [3] (although the measurements of S_{12} are very imprecise at low frequencies). In particular, the calculated values for the cutoff frequencies of the magnitude S_{21} are very close to the measured values. Furthermore, the accuracy of the calculated phase of the S parameters is much better than in standard models.

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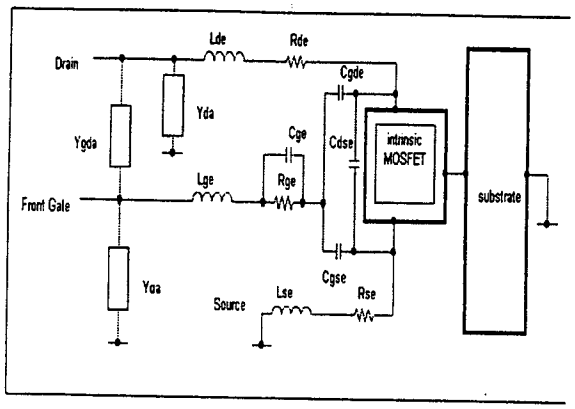


Figure 1. Complete equivalent circuit topology for a SOI MOSFET CAD model.

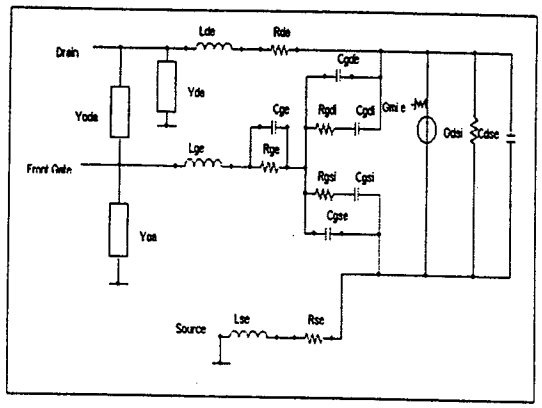


Figure 2. Three-terminal small-signal equivalent circuit for a SOI MOSFET.

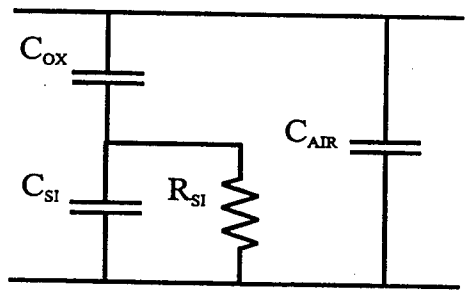


Figure 3 : Equivalent circuit model for the adjacent admittances Y_{DA} and Y_{GA} in Fig. 2.

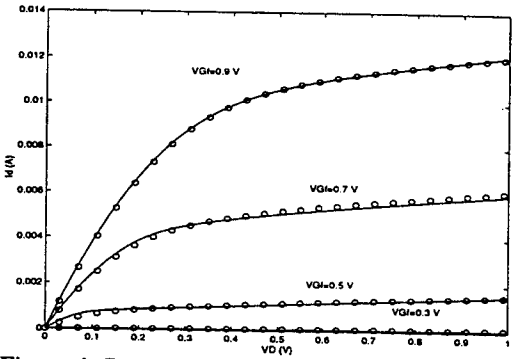


Figure 4. Comparison of measured (symbols) and modeled $I-V_D$ characteristics of a SOI nMOS with $L_{eff} = 0.16\ \mu m$, $W = 6.6\ \mu m$ (16 fingers) and $t_b = 30$ nm.

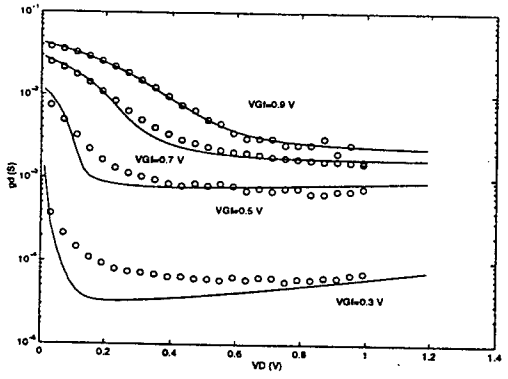


Figure 5. Comparison of measured (symbols) and modeled output conductance of a SOI nMOS with $L_{eff} = 0.16\ \mu m$, $W = 6.6\ \mu m$ (16 fingers) and $t_b = 30$ nm.

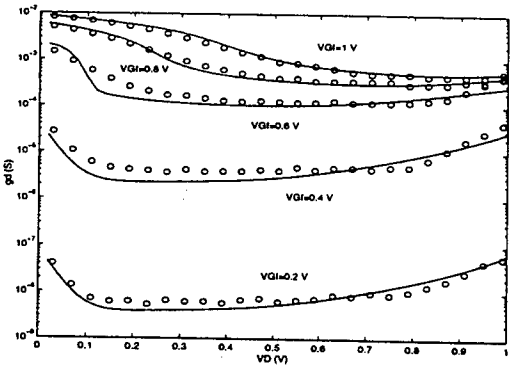


Figure 6. Comparison of measured (symbols) and modeled output conductance of a SOI nMOS with $L_{eff} = 0.16\ \mu m$, $W = 25\ \mu m$ and $t_b = 40$ nm.

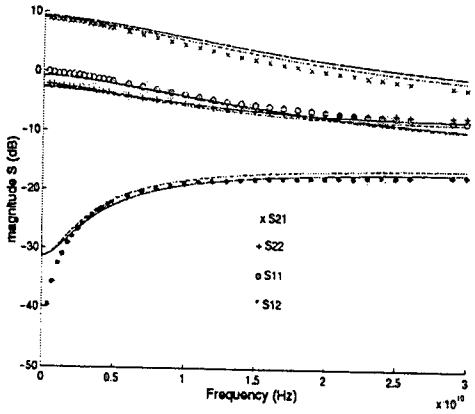


Figure 7. Comparison of measured (symbols) and simulated S magnitudes using the intrinsic model in ELDO for the single transistor (solid line) and with the channel split into three portions (dashed line). $W = 6.6\,\mu\text{m}$ (16 fingers). $L_{eff} = 0.16\,\mu\text{m}$. $V_D = V_{Gf} = 0.9\,\text{V}$.

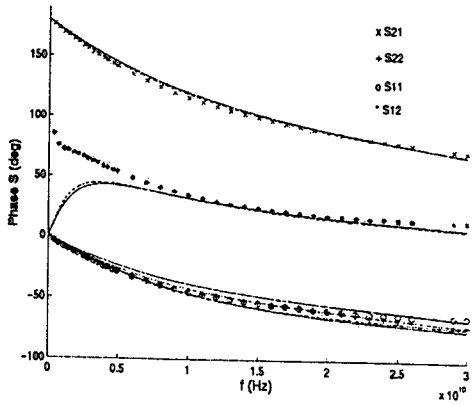


Figure 8. Comparison of measured (symbols) and simulated S phases using the intrinsic model in ELDO for the single transistor (solid line) and with the channel split into three portions (dashed line). $W = 6.6\,\mu\text{m}$ (16 fingers). $L_{eff} = 0.16\,\mu\text{m}$. $V_D = V_{Gf} = 0.9\,\text{V}$.

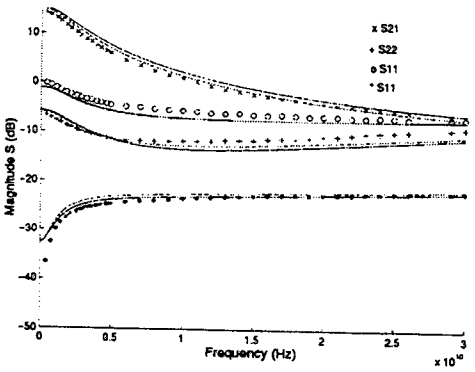


Figure 9. Comparison of measured (symbols) and simulated S magnitudes using the intrinsic model in ELDO for the single transistor (solid line) and with the channel split into three portions (dashed line). $W = 15\,\mu\text{m}$ (16 fingers). $L_{eff} = 0.16\,\mu\text{m}$. $V_D = V_{Gf} = 0.9\,\text{V}$.

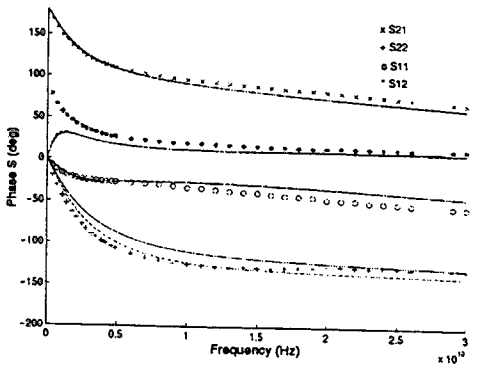


Figure 10. Comparison of measured (symbols) and simulated S phases using the intrinsic model in ELDO for the single transistor (solid line) and with the channel split into three portions (dashed line). $W = 15\,\mu\text{m}$ (16 fingers). $L_{eff} = 0.16\,\mu\text{m}$. $V_D = V_{Gf} = 0.9\,\text{V}$.

Effects of Forward-Biasing the Substrate on the D.C. Characteristics of Deep Submicron n-MOSFETs at Temperatures Between 5 K and 300 K

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Abstract

The effects of forward-biasing the substrate on the output and transfer characteristics of a 0.1 μm-long n-MOSFET are investigated for the 5 K to 300 K temperature range. The threshold voltage, maximum transconductance and subthreshold swing are extracted and evaluated. A low-temperature-enhanced degradation of transconductance was observed under a forward-biased substrate.

Introduction

The performance of CMOS ICs improves significantly with the lowering of the temperature [1]; circuits with higher speed at lower voltage supply are possible since a higher transconductance and steeper subthreshold characteristics are obtained under cryogenic conditions. The MOSFET's threshold voltage, however, increases with the lowering of temperature. The reduction of this parameter by forward-biasing the substrate has been proposed as an alternative for low temperature CMOS [2] and for developing room-temperature dynamic threshold CMOS logic gates [3],[4],[5]. In dynamic threshold CMOS, the substrate bias follows the gate bias, leading to a small threshold voltage in the on-state and to a high threshold voltage in the off-state.

The threshold voltage of long channel n-MOSFETs (2.0 μm) with a forward-biased substrate has been characterized over a wide temperature range [6]. The low temperature D.C. characteristics of submicron (0.8 μm) n-MOSFETs have also been reported for a forward-biased substrate [7]. In this letter, the main D.C. characteristics of a deep submicron (0.1 μm) n-MOSFET with a forward-biased substrate are presented for the 5 K to 300 K temperature range.

Experimental

A 0.1 μm-long and 4 μm-wide n-MOSFET was mounted in the cold-head of a closed cycle refrigerator and the temperature was varied in the 5 K to 300 K temperature range. To obtain the n-MOS transfer characteristics, the drain voltage was kept constant at 50

mV, while the gate voltage was swept from 0 to 1.5 V in 10 mV steps. This procedure was carried out for several forward and reverse substrate biases, and the source was used as the reference terminal. The output characteristics were similarly measured for gate and drain voltages in the 0-1.5 V range. The D.C. characteristics were measured with an HP 4145B Semiconductor Parameter Analyzer.

Results and Discussion

The measured output characteristics are presented in Fig. 1. Regardless of the temperature and gate voltage, the current driving capability improves with the forward biasing of the substrate. The increasing slope of the saturation current, which is present for all the temperatures, may be due to either overshoot or the drain induced barrier lowering effect. The forward biasing of the substrate and the lowering of temperature should promote a kink-like effect. However, this effect is negligible since a similar slope is observed in the saturation region at zero substrate bias and 300 K. A sharp increase of the drain current can be observed for the higher drain and the lower gate voltages at 5 K.

Fig. 2 presents the measured transfer characteristics. The forward-biasing of the substrate produces only a leftward shift of the subthreshold characteristics under deep cryogenic conditions. On the other hand, the forward-biasing of the substrate degrades the subthreshold current at 300 K because a substrate-bias-induced parasitic current is added to the drain current. The parasitic current becomes negligible at low temperatures.

The threshold voltage was obtained from the transfer characteristics by using the linear extrapolation method. The results, including those for a long channel device from the same technology (see [6] for more details), are shown in Fig. 3. Forward-biasing the substrate might not be a suitable approach for applications of the 0.1 μm n-MOSFET at 300 K since the threshold voltage decreases to impractical values. Under deep cryogenic conditions, however, a forward-biased substrate leads to reasonable values of the threshold voltage. The sensitivity of this parameter to the substrate bias is weaker for the short channel device as a result of short channel effects.

The measured maximum transconductance, for the long and short devices, is shown in Fig. 4. The enhancement of transconductance with the lowering of temperature is clearly seen. The transconductance of the long device increases with the forward-biasing of the substrate; this is expected because of the reduction in the transverse electric field in the channel. The transconductance of the short channel device behaves anomalously; it decreases when the substrate is forward biased. This effect is enhanced at low temperatures and agrees with the transconductance enhancement for a reverse biasing of the substrate reported for submicron MOSFETs at 300 K [8]. Due to the weaker control of the channel by the transverse field, the transconductance is less sensitive to the substrate bias in the short device. The subthreshold swing for the short device is also shown in Fig. 4. At 300 K, this parameter is degraded with the forward biasing of the substrate. This behaviour is directly correlated with the degradation of the transfer characteristics observed in Fig. 2. At lower temperatures, the subthreshold swing improves significantly and becomes insensitive to the substrate bias.

Conclusions

The main D.C. characteristics of a 0.1 μm n-MOSFET were measured in the 5 K to 300 K temperature range. The effects of forward biasing the substrate on these characteristics were discussed. Deep submicron MOSFETs are suitable for dynamic threshold voltage applications only at low temperatures. This is because the threshold voltage decreases to impractical values and the subthreshold characteristics degrades significantly at 300 K. The transconductance is improved with the lowering of temperature in spite of its enhanced degradation observed with a forward biased substrate.

Acknowledgements

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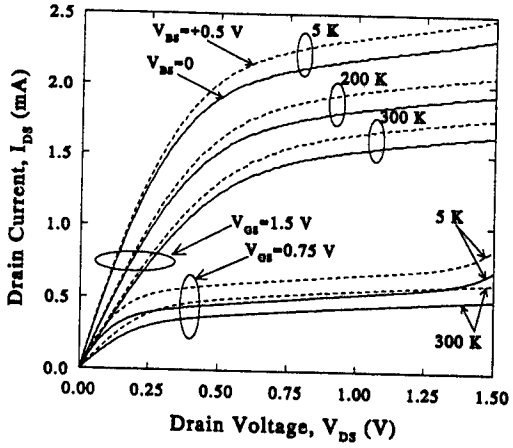


Figure 1: Measured output characteristics at different temperatures of the 0.1 μm-long n-MOSFET for V_{BS}=0 (continuous line) and V_{BS}=+0.5 V (dashed line). The results are shown for two different gate voltages.

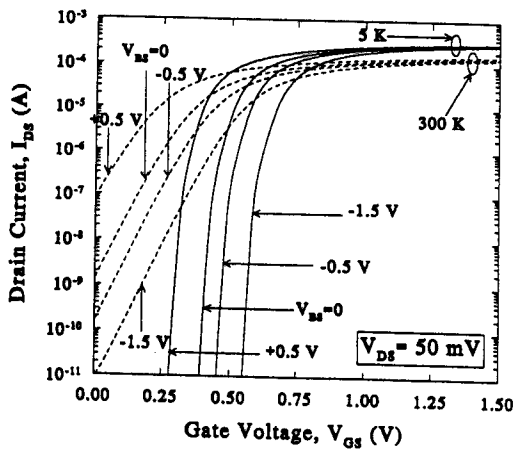


Figure 2: Measured transfer characteristics at 5 K (continuous line) and room temperature (dashed line) of the 0.1 μm-long n-MOSFET for several substrate biases.

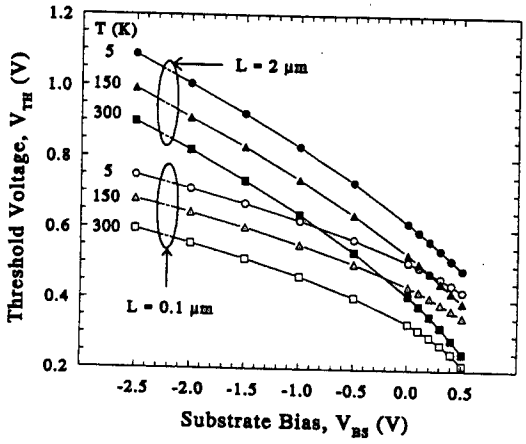


Figure 3: Measured threshold voltage as a function of the substrate bias at several temperatures. The results are presented for the long channel (filled symbols) and the deep submicron (hollow symbols) devices.

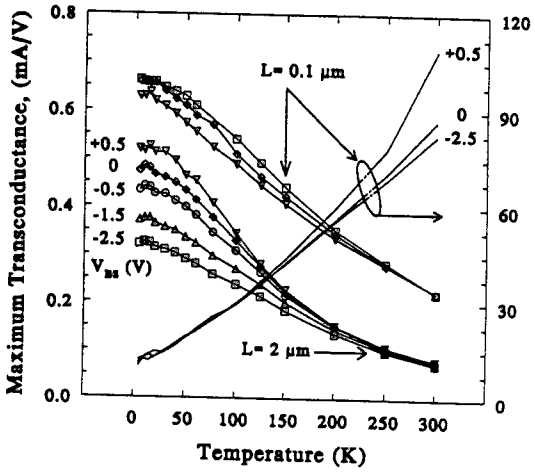


Figure 4: Temperature dependence of the maximum transconductance for several reverse and forward substrate biases for a long channel and a deep submicron n-MOSFETs. The subthreshold swing at different substrate biases is also included for the 0.1μm channel device.

Application of Silicon-Based Heterostructures in Microelectronics

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Finally, after years of intense basic and applied research, and after several premature announcements, silicon-germanium (SiGe) devices and integrated circuits became commercially available.[1] In 1998 the former Daimler-Benz subsidiary TEMIC (now with ATMEL), and subsequently IBM introduced products for high frequency analog and digital applications that incorporate SiGe HBTs (heterobipolar transistors). Both companies were among the pioneers regarding the epitaxial growth of SiGe, but meanwhile almost every manufacturer in the USA, Japan and Europe has implemented its own SiGe HBT process and has already entered the market, or is about to do so. Latest European examples are Infineon (the semiconductor device branch of Siemens), who offer SiGe HBTs for high frequency applications, and AMS of Austria who, in cooperation with SiGe Microsystems of Canada, provide a SiGe-BiCMOS process that is virtually open to everyone through their special multi-product wafer service.[2]

The Si/SiGe heterosystem is fully compatible with standard silicon technology, which is a distinctive advantage compared to the more common III-V heterosystems. Therefore, SiGe offers the benefits of band structure engineering without sacrificing the main advantage of Si technology, namely device integration on an ultra large scale.

In its simplest version the SiGe HBT requires just one additional pseudomorphic epilayer for the narrow gap SiGe base, and minor adjustment to the standard process parameters. Because Ge has a 4% larger lattice constant than Si the critical layer thickness for the generation of misfit dislocations is a concern. Therefore many manufacturers have adapted a drift transistor concept to keep the effective Ge concentration low.[3] In this version of the HBT the drift field in a compositionally graded $Si_{1-x}Ge_x$ base layer is exploited rather than the band offset, which traditional („true") HBTs[4] utilize. Daimler-Benz/TEMIC demonstrated with their approach that with a modified emitter design and reduced thermal budget a true SiGe HBT is feasible and suited for production.[5] On the long run the true HBT has distinctive advantages concerning the base sheet resistance, the maximum oscillator frequency and quite general the design freedom. It is therefore not surprising that the highest published cut-off and oscillator frequencies of about 160 GHz were achieved with true HBTs.[6,7] The most recent developments aim toward a ternary $Si_{1-x-y}Ge_xC_y$ base layer. It has been demonstrated that carbon concentrations as low as 0.1% can drastically reduce transient enhanced diffusion of the boron doping in the base, and thus allow even thinner base layers for improved cut-off frequencies.[8]

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The main applications of the SiGe HBT will be within the rapidly expanding field of high frequency telecommunications. On the other hand, more than 80% of the overall microelectronic market consist of low-power digital ICs, which are an exclusive domain of the silicon CMOSFET (complementary metal oxide semiconductor field effect transistor) technology. With the successful implementation of the SiGe HBT it is therefore an obvious step to extend the benefits of a heterosystem to the CMOS process in order to improve its moderate high frequency performance.

Proper exploitation of band offsets in a heterostructure can result in enhanced carrier mobilities concomitant with carrier confinement. This concept has led to the well-known HEMT (high electron mobility transistor) in several III-V material combinations, and has shown superior properties in high frequency behavior as well as in noise figures. HEMTs and their p-type complement can also be realized in the Si/SiGe heterosystem. However, in contrast to the rather simple pseudomorphic SiGe HBT, the peculiarities of the conduction band alignment at the strained Si/SiGe interface require additional strain-relaxed heterolayers for strain control. The reliability problems induced by these layers has so far only been solved on a laboratory level.[9] Nevertheless, the potential advantages of a hetero-CMOS process are obvious: Maximum oscillator frequencies of 120GHz for n-type[10] and of 85 GHz for p-type[11] hetero-FETs have been demonstrated even with rather conservative gate widths of 0.25μm. The results of the p-FETs, which incorporated a Ge channel for the 2D hole gas, are especially remarkable, given the inferior performance of p-devices in basically all other material systems. Thus combining a Si channel n-FET with a Ge channel p-FET will for the first time offer a complementary building block with almost perfectly matched properties. This makes the SiGe hetero-FETs especially attractive for high-speed digital applications, but also for high-end analog circuits. The main emphasis has now to be on the implementation of a strain-adjusting layer that is suited for the production environment of large scale integration. It is important to have a hetero-CMOS technology ready when - in the next 5 or 6 years - the cost for further down scaling of critical lengths become too prohibitive to remain an alternative to the introduction of the SiGe heterosystem.

Optical applications are commonly associated with III-V materials with direct band gaps. Nevertheless, it is again Si that has the largest market share, albeit restricted to detectors such as charge coupled device arrays (CCD) and solar cells. Still, the band gap of Si is too large to allow optical detectors for fiber communication networks, and the indirect band gap rules out competitive light emitters. The first deficit can be overcome by $Si_{1-x}Ge_x$ or $Si_{1-x-y}Ge_xC_y$ alloys and superlattices, which allow the tuning of the band gap absorption into the 1.3 to 1.55 μm range where fiber transmission works best. But even light emission is not entirely out of question with a proper exploitation of quantum mechanical principles. Si/Ge superlattices with periods of just a few atomic layers,[12] or self-assembled quantum dots of pure Ge in a Si matrix[13] could become the ingredients for future Si-based light emitters.

Such advanced concepts are presently in a stage of basic research, but they may one day allow the monolithic integration of fast and highly complex digital and analog functions with the light emitters and detectors required for long distant signal transmission. All this

could become possible with a single technology entirely based on group IV heterostructures.

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GaN-Based Materials for Microelectronics

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The AlGaInN materials system offers many potential advantages for use in high temperature, high power electronics, including high breakdown voltage, large bandgaps and good transport properties. To date, most of the attention has focussed on fabrication of AlGaN/GaN HFETs for power microwave applications. There is also strong interest in developing GaN/AlGaN HBTs for military systems in which device linearity is critical and ultra high power rectifiers and thyristors for switching in utility applications. In this paper we will discuss the performance of GaN Schottky rectifiers and GaN/AlGaN HBTs and identify areas for future work.

(a) Schottky Rectifiers

The GaN samples were grown by MOCVD on c-plane sapphire in two different systems using ammonia (NH_3) and trimethylgallium (TMG) as the precursors. In one case 3-11μm thick undoped GaN layers were grown on top of a 1μm thick n^+ GaN region, while in the other case 3μm of high resistivity GaN was grown on a 300Å thick novel buffer layer. The 4-12μm thick structures were used for fabrication of vertically-depleting diodes, while the 3μm thick structure was found to deplete laterally. In the former devices, a mesa down to the n^+ region was formed by Cl_2/Ar Inductively Coupled Plasma etching under low-damage conditions [13], while in the latter devices selective-area n^+ ohmic contact regions were formed by Si^+ implantation followed by annealing at 1125°C [13]. Ohmic contacts were formed by lift-off of Pt/Au. The ohmic contacts were annealed at 750°C for 20 secs prior to deposition of the Pt/Au. Schematics of the mesa and planar structures are shown in Figure 1.

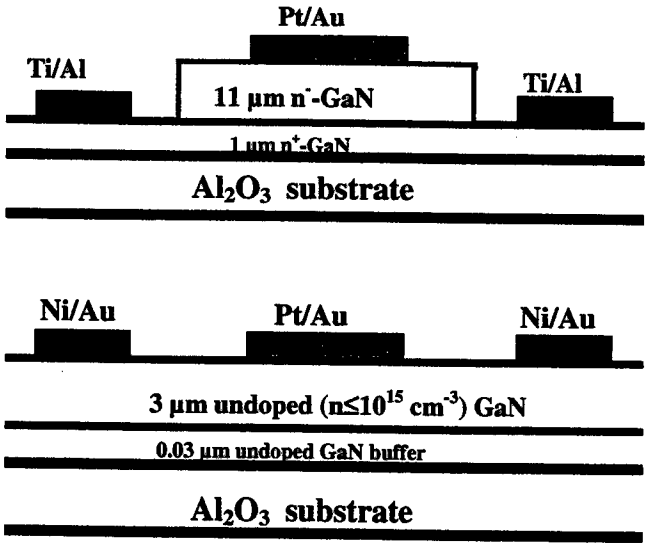


Figure 1. Schematic of mesa and planar GaN diodes.

We obtained V_{RB} values of ~550 V and >2 kV for the 11m thick active layer vertical diodes and 3μm thick lateral devices, respectively, at 25°C. Figure 2 shows a compilation of reverse density data for recently reported SiC and GaN diodes, as a function of reverse bias. Once again it is clear that some SiC devices are relatively close to optimal performance, at least for biases less than ~100 V. At higher biases, both GaN and SiC diodes show relatively high reverse current densities. We have generally found in our diodes that at low reverse biases (<50 V) the reverse current is dominated by surface leakage, whereas at higher biases the main contribution is from bulk leakage current. It is likely this latter current results from the problems discussed earlier, i.e. dislocations and impurities.

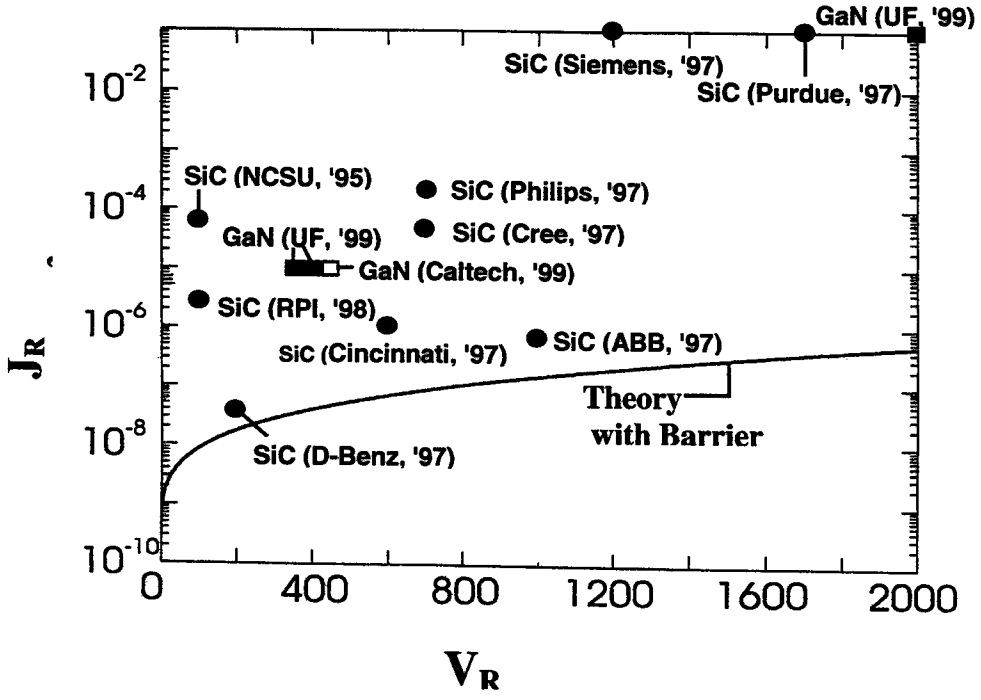


Figure 2. Reverse current density in GaN and SiC diodes as a function of reverse bias voltage. The solid line is the theoretical value for 4H-SiC.

Figure 3 shows corresponding data for V_F versus V_{RB} for GaN and SiC diodes, along with theoretical values for SiC based on different Schottky barrier heights. For our Pt/Au contacts, the barrier height is ~1eV. Once again the GaN devices are well above the theoretical values, indicating there is more work to be done on both the ohmic and rectifying contacts for this material.

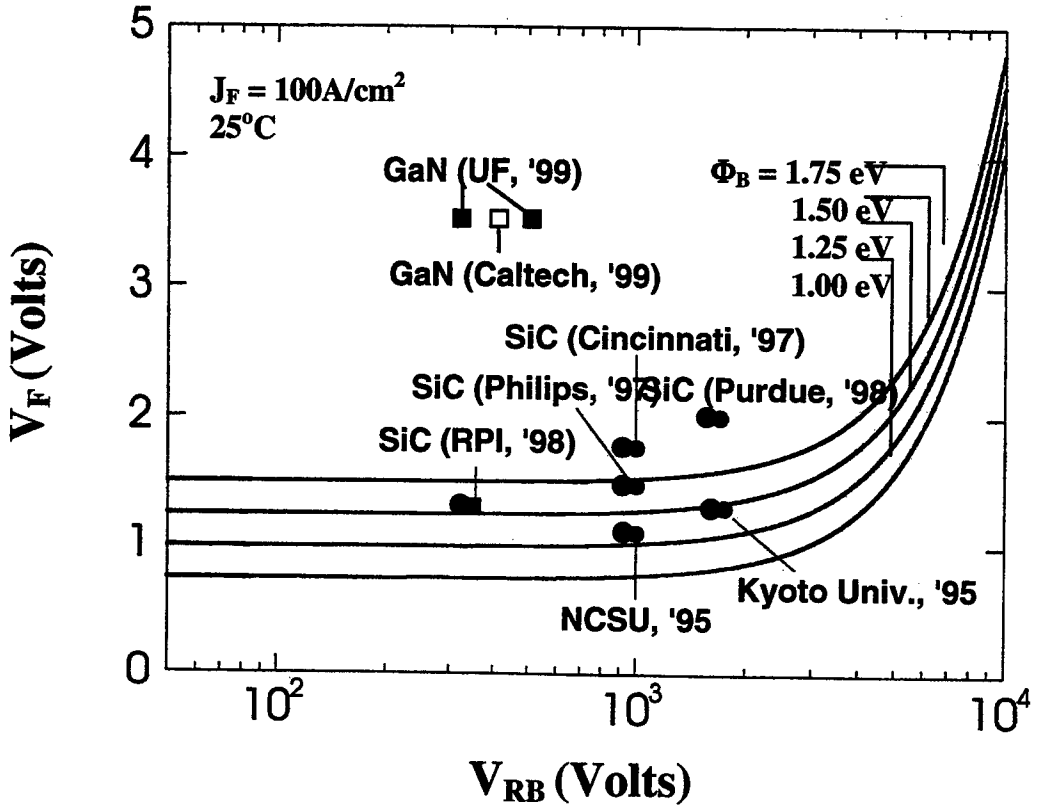


Figure 3. Forward voltage drop as a function of reverse breakdown voltage for GaN and SiC diodes. The solid lines are theoretical values for 4H-SiC, assuming different barrier heights.

(b) **HBTs**

The process flow for device fabrication is shown schematically in Figure 4. First the emitter metal (Ti/Al/Pt/Au) is patterned by lift-off and used as an etch mask for the fabrication of the emitter mesa. The dry etching was performed in a Plasma Therm 770 Inductively Coupled Plasma (ICP) system using Cl_2/Ar discharges. The process pressure was 5 mTorr, and the source was excited with 300 W of 2 MHz power. This power controlled the ion flux and neutral density, while the incident ion energy was controlled by application of 40 W of 13.56 MHz power to the sample chuck. Base metallization of Ni/Pt/Au was patterned by lift-off, and then the mesa formed by dry etching. The etch rate of GaN under our conditions was ~1100 Å-min^{-1}, and was terminated at the sub-collector where Ti/Al/Pt/Au metallization was deposited. The contacts were alloyed at 700-800 °C.

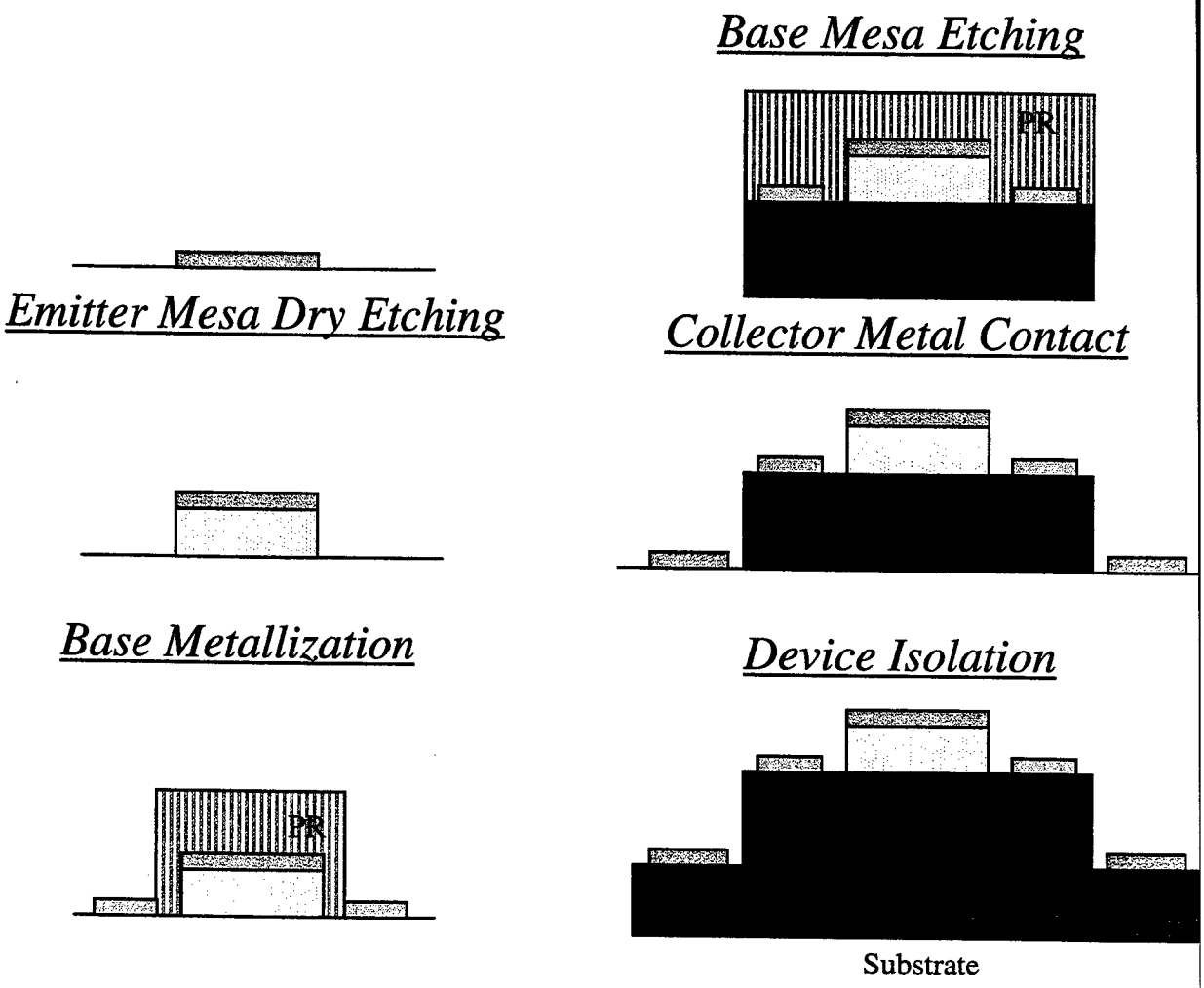


Figure 4. HBT fabrication sequence.

The device performance of both the MBE and MOCVD grown devices was similar, namely a common-emitter current gain of ≤3 at 25 °C. In both devices the performance was still limited by the base resistance, and methods to increase the base doping and lower the extrinsic resistance in this region will be critical for future efforts in this area. The common base current gain, ∝, was in the range 0.75 (25°C) to 0.9 (300°C), indicating that the base transport factor is close to unity and that I_B is dominated by re-injection to the emitter.

Material Issues in a-Si:H and poly-Si Thin-Film Transistors for Microelectronics and Optoelectronics Applications

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I. APPLICATIONS OF a-Si:H and Poly-Si THIN-FILM TRANSISTORS

Thin-film transistor (TFT) technology has been one of the fastest-growing semiconductor technology of the 1990s. It has emerged from obscurity in 1980s to a market value of over $20 billion today [1]. The market is expected to grow steadily well into the twenty-first century. Currently, TFTs are mainly used in high-performance liquid crystal displays (LCDs). However, TFT technology has expanded to products ranging from portable computers to desktop displays, TVs, industry, transportation, entertainment, avionics, hospitals, and military. Table 1 lists TFT products that have been prototyped or in production [2,3]. For most of these applications, the substrate material or size is not the limiting factor. At the present time, TFTs are exclusively used as the driving or readout devices that access local information at each pixel. Therefore, TFT is a general-purpose technology that is complimentary to, instead of competing with, VLSI technology.

II. TFT STRUCTURES, MATERIALS, PROCESSES, & DEVICES RELATIONSHIP

TFT has a structure similar to that of a MOS transistor, i.e., containing source, drain, and gate electrodes. All dielectric, semiconductor, conductor films in a TFT are deposited on the substrate. The thickness of each layer is in the range of 500Å to 4000Å. Varieties of TFT structures have been published and used in production [4]. Among them, the inverted and normally staggered structures are popular for a-Si:H TFT; the coplanar structure is popular for poly-Si TFT. Figure 1 shows a generalized chart of the relationship among the structure, material, process, and device characteristics of a TFT. It also includes major factors in each category. It is possible to prepare high performance TFTs using various types of structures and different process conditions. Therefore, the relationship among them is more complicated that that of a MOS. In spite of many researches in the TFT area, there are limited publications that delineate the relationship among these parameters. For example, the gate nitride and the threshold voltage of an a-Si:H TFT has been found [5]. The a-Si:H/gate nitride interface roughness affects the field effect mobility [6]. Material properties of individual films and process conditions are indispensable factors for the high performance TFT.

III. a-Si:H TFT MATERIALS

The a-Si:H TFT is composed of conductors, semiconductor, and dielectric films. The conductor films, i.e., for gate lines, date lines, and pixels, are typically prepared by the sputtering method. The semiconductor and dielectrics are prepared by the plasma enhanced chemical vapor deposition (PECVD) method at a low temperature, e.g., less than 350°C.

For gate and data lines, the film's conductivity is a major concern. Refractory metals, such as tantalum, molybdenum, tungsten, and their alloys, are commonly used. As the resolution and the size of the product are increased, aluminum and copper become popular. The suppression of the hillocks formation phenomenon is the major issue in preparing the aluminum gate line in the

inverted, staggered TFT. The adhesion, passivation, corrosion prevention, and critical dimension control are main issues in preparing the copper gate line. The high conductivity, light transmittance, homogeneous layer structure, and low etch residue are primary concerns of the pixel conductor, i.e., indium tin oxide (ITO).

For the a-Si:H film, both the bulk and the interface characteristics need to be considered. The bulk film properties include the hydrogenation concentration, the SiH/SiH_2 ratio, the defect density, conductivity, and photosensitivity. The interface properties include the interface states, roughness, and band gap variation. The gate dielectric requirements include low dangling bond concentration, high hydrogen concentration, proper Si/N ratio, SiH and NH bonds, low interface states, high resistance to hydrogen and chemical attacks. The passivation dielectric material issues are similar to those of the gate dielectric material. For large area applications, a redundant structure, i.e., one layer optimized for the interface are and another layer tailored for the bulk properties, is often used. The n^+ ohmic contact layer should have a high conductivity, e.g., using a microcrystalline film [7]. At the same time, the deposition process should be able to remove the native oxide on the a-Si:H surface.

The long-term stability of the thin film materials is critical to the reliability of the TFT. For example, in order to passivate dangling bonds in a-Si:H and dielectric SiN_x films, a large amount of hydrogen is included in them. Hydrogen exists in the TFT structure in two forms: weakly and strongly bonded. The former accounts for only a small portion of the total hydrogen content. However, it has a drastic influence on the TFT performance. Figure 2 shows that the 350°C prepared a-Si:H TFT can deteriorate dramatically at 250°C by losing the loosely bonded hydrogen [8]. The gate SiN_x structure also affects the TFT reliability. For example, when the gate dieleltric is composed of two different types of PECVD SiN_x films, the threshold voltage shift after the bias-stress test is a function of the interface layer thickness [9].

IV. Poly-Si TFT MATERIALS

The major material issue in polycrystalline silicon (poly-Si) TFT is how to form the low defect silicon film at a low temperature, e.g., less than 600°C, over a large area and at a high throughput.

Poly-Si can be directly deposited on glass by a CVD or sputtering method. It can also be transformed from the amorphous form into the crystalline form. The transformation process involves an energy source, such as heat, light, or plasma. In general, poly-Si with large grains and low inter- and intra-grain defects gives the best TFT characteristics, such as the high mobility and low threshold voltage. Under the proper process condition, e.g., power density, pulse duration, frequency, and substrate temperature, the excimer laser crystallized poly-Si has the best film quality. A field effect mobility high than 100 cm^2/Vs is routinely achieved with this kind of poly-Si. Most poly-Si TFTs have a high off-current due to the defective grain boundaries. Grain boundary defects, such as dangling bonds, can be removed with a hydrogenation step. The laser crystallization process cannot satisfy the large area, high throughput production requirement.

Other alternative crystallization methods have been actively pursued by researchers. For example, annealing in low temperature furnace, by rapid thermal processing, using metal-induced structure, exposing to plasma, or ion implantation have been tested. Poly-Si formed by these methods has smaller grains and a higher defect density than that formed by the excimer crystallization method. Most of the low temperature processes require a long crystallization period, such as several hours. Recently, a pulsed rapid thermal annealing method including the patterned metal seed layer has been successfully used to form poly-Si [10]. A high crystallization rate, i.e., greater than 10 micrometers/pulse of 1 sec. in the channel area, has been obtained. Figure 3 shows the poly-Si

structure formed by this method. This method is easily integrated into the existing TFT structure. This is an example of preparing poly-Si TFTs using novel crystallization methods that are applicable to large-area, low temperature substrates with a high throughput.

V. SUMMARY

Material issues in a-Si:H and poly-Si TFTs have been reviewed and discussed. For the a-Si:H TFT, the critical item is how to maintain the long-term stability of the films that are responsible for the transistor's high performance. For the poly-Si TFT, the most urgent issue is how to form the high quality polycrystalline silicon thin film on a low temperature glass at a high throughput. In addition to LCDs, many new and advanced microelectronics and optoelectronics can be fabricated with TFTs.

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Table 1. Applications of TFTs in Microelectronics and Optoelectronics [2,3]

TFT Functions	Applications	Silicon Materials
Driving devices	Liquid crystal displays	a-Si:H for direct-view poly-Si for projection
	Printers/facsimile	a-Si:H
	Organic light emitting diodes	a-Si:H
Readout devices	Medical imagers	a-Si:H
	Chemical sensors	a-Si:H
	Radiation detectors	a-Si:H or poly-Si
VLSI/ULSI	SRAM loading cells	Poly-Si
	E^2 PROM	Poly-Si or a-Si:H
	High voltage MOS	Poly-Si
Others	Artificial retina	a-Si:H
	Photo imagers	a-Si:H

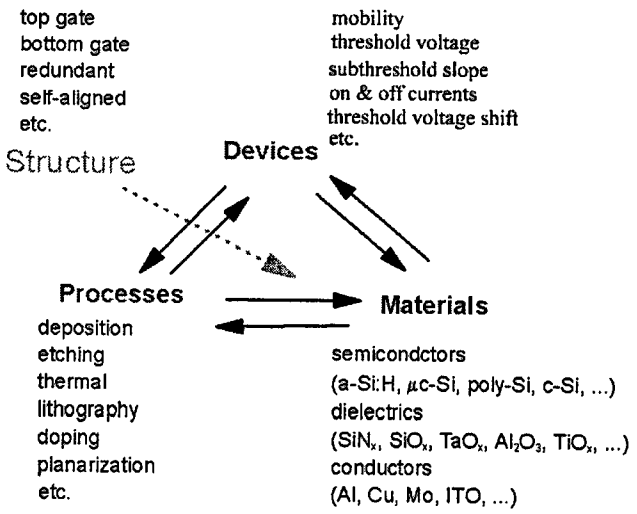


Figure 1 TFT Structures, Materials, Processes, and Devices Relationship

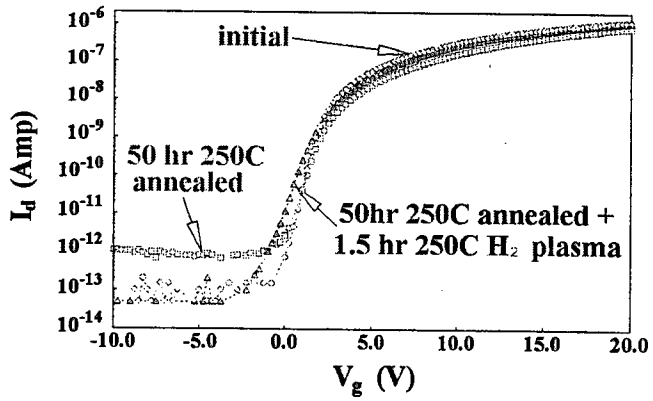


Figure 2 a-Si:H TFT Deterioration Due to Loose of Weakly Bonded Hydrogen [8]

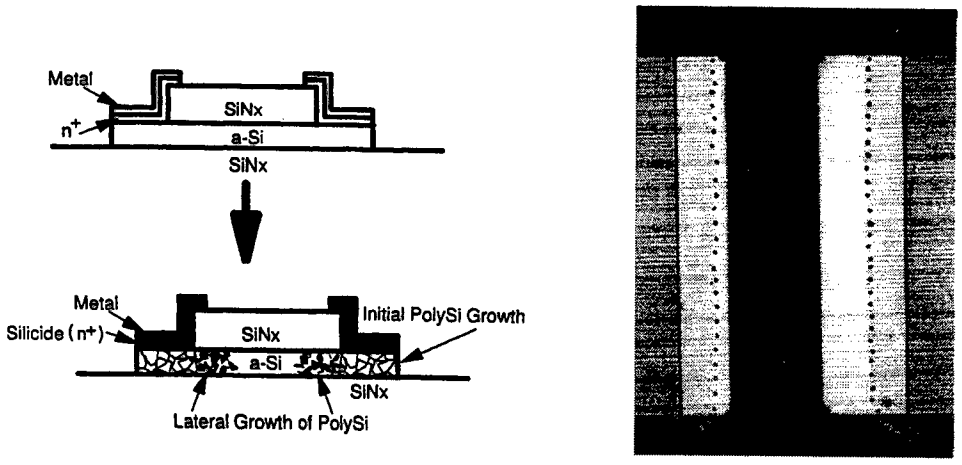


Figure 3 Poly-Si Formed by Pulsed Rapid Thermal Annealing [10]

Silicon Carbide Potential for Applications in Electronics and Microelectronics

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Abstract
This paper reviews status and first-to-solve problems in silicon carbide (SiC) technology.

I. INTRODUCTION

The outstanding properties of SiC as a material for high power and high temperature electronics are spoken of about 40 years [1]. Since that time the great progress has been achieved in improvement of the material quality and development of SiC based devices[2]. However, it is still remain a lot of unsolved and even not well-understood problems. In present paper we list the main steps in SiC material and device improvement (Fig. 1) and also outline the actual problems and limitations on the way of SiC-based electronics. We must emphasize that SiC technology is extremely dynamic field and some "record" results, which are described here, probably would be beaten before this paper is published.

II. BULK TECHNOLOGY

The first commercial valuable technology to produce electronic grade SiC crystals was the sublimation method developed by Lely in the 50th [3]. The method provided high quality SiC crystals of various SiC polytypes (mainly 6H and 4H) up to 1 inch in size. A lot of Lely crystals has been fabricated in the USSR on a commercial basis and, despite the fact that the production was stopped more than 10 years ago, these crystals are still on the market. Non-controllable nucleation of SiC crystals in the Lely method resulted in both good features of the crystals (high crystal quality, micropipe absence, low dislocation density) and technology limitations (small size, irregular shape). Today, these crystals are used as (1) seeds for bulk growth, (2) substrates for high quality experimental epi structures, and (3) for basic research.

Commercial technology for bulk crystal SiC growth has been developed based on original Lely idea using a seeded process [2]. Currently, more than 7 companies around the world are manufacturing SiC wafers using this technological approach. World leader in this area, Cree Research, recently has announced sale of 3 inch SiC wafers and demonstrated first 4 inch SiC material. We may expect 4 inch SiC wafers on the market in two years. Two polytypes of silicon carbide, 4H and 6H, are on the market. Recent results on MOSFET fabrication [4] initiated interest in 15R polytype which propabaly would result in the production of 15R-SiC crystals.

Despite a remarkable progress in bulk SiC growth, the main problem in SiC bulk technology is the high defect density. In commercial SiC wafers, micropipe and dislocation densities exceed 10 cm^{-2} and 10000 cm^{-2}, respectively. These crystals also

suffer from macro defects such as voids, foreign polytype blocks, and misoriented blocks. This defect density can be tolerated for some applications, but is unacceptable for high-power applications. SiC substrate materials with "zero" micropipe density, which are required for high-power devices, can be made by the Lely method and/or by SiC bulk growth from liquid phase [5]. Unfortunately, these methods are currently enable to produce large size SiC boules. Another approach is to use SiC epitaxial wafers with reduced defect density [6]. High-power devices require SiC wafers combining high electrical conductivity and low defect density. Effect of high doping level on defect formation in bulk SiC must be investigated. A new tendency is the development of chemical vapor deposition [7] and liquid phase growth [5] for bulk SiC fabrication.

III. EPIRAXIAL TECHNOLOGY

The most remarkable results in SiC epitaxial technology have been achieved by chemical vapor deposition (CVD) [8]. Growth rate can be controlled in a wide range from 1 to 20 μm/hr. High-quality thick SiC layers lead to high-voltage (up to 8.9 kV) devices [9]. Doping concentration in SiC epitaxial, for both p- and n-type, is controlled in the range from 10^{15} to 10^{20} cm^{-3}. Doping and thickness variations for 2 inch SiC epitaxial layers grown in multi-wafer production type machines do not exceed 10%. Material quality improvement resulted in significant increase in SiC device area (up to 7x7 mm^2 for pn diodes and 8x8 mm^2 Schottky diodes). As a result, the switching power has been increased from a few kilowatts a few years ago to 36 kW devices reported at the 1999 SiC conference [10].

Important results have been obtained on diffusion length of minority carriers in SiC pn structures showing that at a high injection level (high forward current) the diffusion length increases from 2 μm up to 10 μm [11]. Despite this remarkable fact, investigation of deep levels, controlling the diffusion length value, must be continued to develop SiC devices with blocking voltage exceeding 10 kV.

IV. RECENT DEVICE RESULTS

Recent progress in silicon carbide high-power switching electronics, which has been reached in last three years, is demonstrated in Fig. 2._H. Lendenmann and co-workers [12] reported on the fabrication of 2500 V 150 A Si-IGBT/SiC diode module. SiC pn diodes incorporated in the module were made using Al-B ion implantation. Maximum diode size was 7x7 mm^2. The diodes were fabricated in the areas of SiC samples without visible defects. For these diodes, leakage current density at 2500 V was $< 10^{-5}$ A/cm^2.

4H-SiC Schottky diode with reverse voltage of 3.85 kV has reported by Q. Wahab and co-workers [13]. Dahlquist and co-authors [14] demonstrated a 2.8 kV Junction Barrier Schottky (JBS) diodes. These diodes combine advantages of pn diodes and Schottky barriers resulting in relatively low leakage current and small forward voltage drop. The reported JBT diodes exhibited a forward voltage drop of 2.0 V at a current density of 100 A/cm^2 (8 $m\Omega\ cm^2$).

A Vertical Junction Field Effect Transistors (VJFET) with blocking voltage up to 1700 V were demonstrated [15]. The devices consist of 1452 connected cells resulting in the active area of 2.3 mm^2.

An asymmetrical gate turn off (GTO) 4H-SiC thyristor with a blocking voltage of 2600 V was fabricated [16]. The thyristor showed a forward current of 12 A at a voltage drop of 6.5 V.

In power microwave device field, SiC MESFETs operating at power density of 4.6 W/mm at 3.5 GHz and a power added efficiency of 60% with 3 W/mm power density at 800 MHz have been reported [17]. 4H-SiC microwave power transistors [18] exhibited f_{max} of 39 GHz and extrinsic transit frequency, f_T, of 8.1 GHz. Saturation drain current was 300 mA/mm for 12.8 mm gate periphery device.

V. SUMMARY

We may expect that in 5 years 4 inch SiC substrates will be widely used for device fabrication and 6 inch SiC wafers would be demonstrated. High-frequency devices for a frequency range of 2 – 10 GHz and power range from 100 – 200 W will be on the market. In 10 years, we may expect that 50 kV/1000 A switching devices will be realized making megawatt solid-state electronics real.

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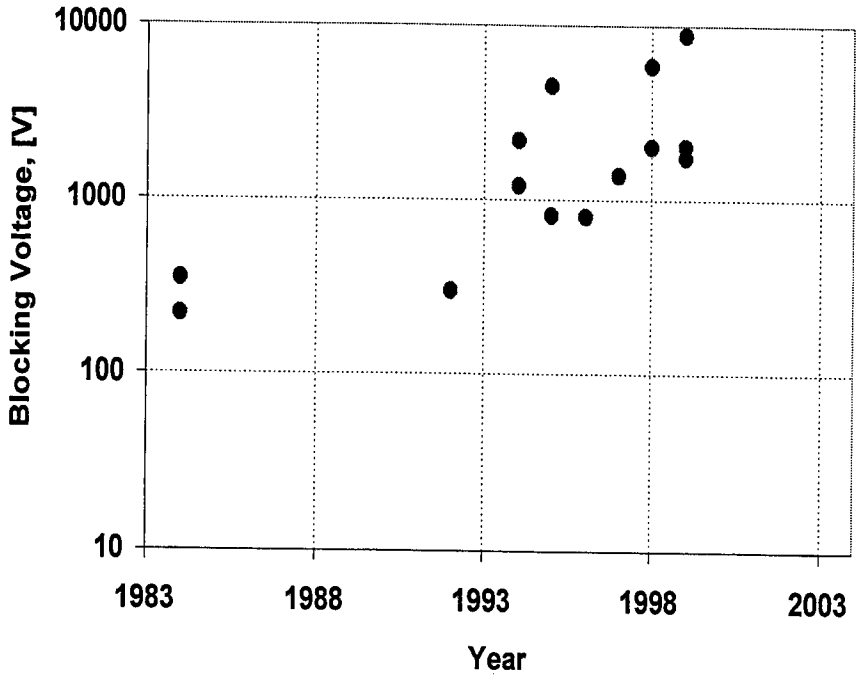


Figure 1. Progress in blocking voltage of SiC-based p-n-junctions.

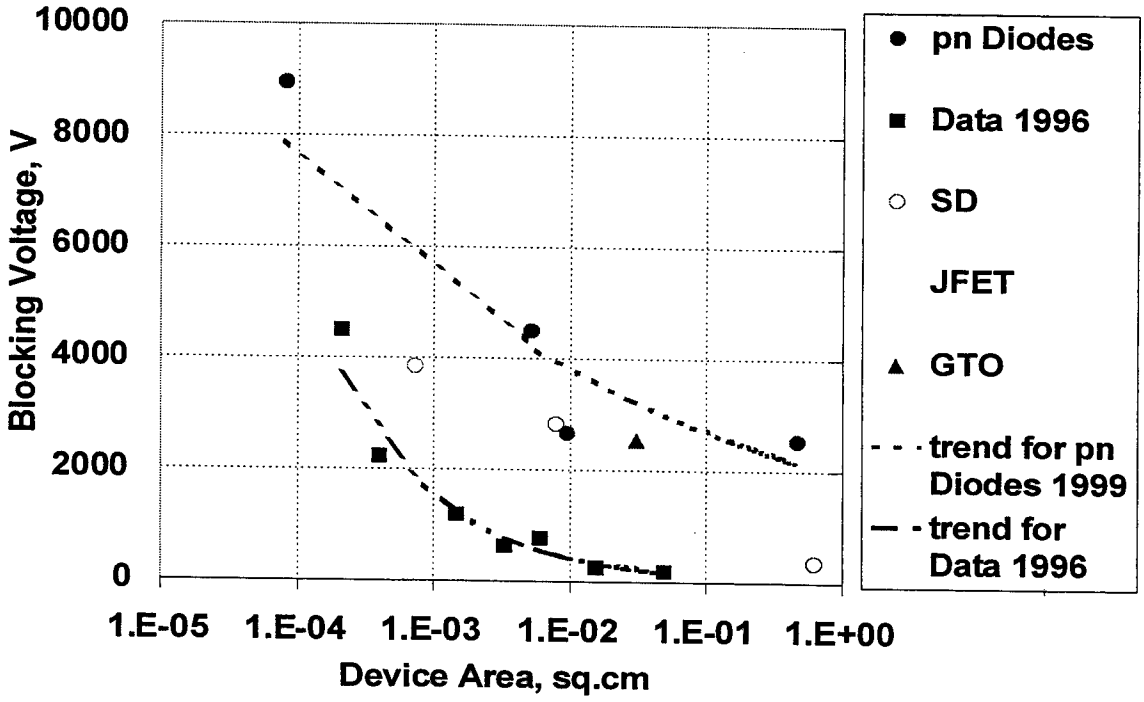


Figure 2. Blocking voltage of SiC devices vs. device area.

Carbon Nanotube Arrays and Y-Junctions
&
Non-lithographic Nanofabrication for Future Electronics

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The celebrated microelectronics technology has known a one-dimensional path: Miniaturization. It has now come to a crossroads. Looking down the road to nanoelectronics, one sees exponentially increasing cost and diminishing return with billion dollar IC fab costs doubling every generation. The high cost is on the one hand squeezing out all but the largest players, and on the other slowing down innovation from within. Troubles at the physical foundation of the technology are as concerning, if not more so. The wiring challenge and the power dissipation crisis are only going to get worse with each further step of miniaturization. These problems are rooted in the much hyped Digital (i.e. von Neumann's binary and serial computing) paradigm which has remained unchanged for decades.

The time has come to look for alternative paths; a view shared by many. Alternatives do exist, both on the fabrication front, as attested by the recent successes of "natural" approaches in nanofabrication, and on the architecture front, as advocated by von Neumann himself in his later years and many others.

In this talk, I will use our recent success in fabricating highly ordered arrays of carbon nanotubes with the best uniformity yet reported as an example of the capabilities enabled a non-lithographic nanofabrication technique we are developing. And, I will highlight additional examples of our efforts on two fronts "in search of alternative paths" to future evolution of microelectronics:

(1) Non-lithographic fabrication of highly-ordered arrays of nanotubes, nanowires and nanodots; their fundamental properties and device applications;

(2) The prospects of extracting computational functions from the collective behavior of large and highly ordered arrays of simple nanoelements.

Topics in Anisotropic Etching of Silicon

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1. CRYSTAL FEATURES

Anisotropic etching of silicon is potentially a very powerful microsystems process technique. While it is currently most often used for obtaining {111}-defined cavities with {100} floors in {100} silicon wafers, there are many other types of geometrical features available. More complex (and still accurate) shaping of silicon might be practical if we understood it better. Fully mature use of crystal-anisotropy-based etching of silicon will depend both on thorough experimental investigation, and on a better theoretical understanding of the involved chemical and atomic interactions.

This paper outlines an approach driven by features observed on etched and underetched surfaces, and by their direct geometrical relation to the underlying crystal structure. The variations in etch data can be highly complex, and an organized reporting of the experimental observations is a pre-requisite for more advanced theoretical understanding.

Some typical experimentally-observed phenomena in the use of a particular anisotropic etchant are: {100}:{110}:{111} plane anisotropy, temperature dependence of etch rates, fastest-etching plane (e.g. {411}, or {313} etc), and corresponding etch rate, hillock characteristics or absence on {100} surfaces, etch rate of certain masking materials such as SiO_2, SiN_x, etch rate of certain important materials like Al.

Less commonly reported, but potentially highly useful from a theoretical perspective, are graphs of under-etch-rate vs. mask-edge deviation angle, from experiments on {100} silicon. These are often seen in polar coordinates [1], and readily show the maxima and minima in under-etch rates. The collection of such under-etch data is not difficult, the main requirement being a wagon-wheel-type [1] mask, whereby a full set of data can be collected at once. Under etch data may be a good experimental compromise, given the more involved nature of observing full 3-D etch anisotropy (by etching a silicon sphere [2]).

In such underetch experiments, the inclination angles of the underetched planes also vary in a very interesting, systematic manner. Observations in this laboratory [3-5], showed that the plane inclination angles, on etched {100} silicon, vary in one of two modes, outlined in Fig.1. While both modes P and K must clearly converge at the {111} plane (54.7°-inclined from the horizontal, and 35.3°-inclined from the vertical), the two modes diverge substantially at other mask-edge deviation angles. When the mask-edge is 45°-deviated from the <110>-directed wafer flat, Mode P exposes 45°-inclined {110} planes (e.g. used in the formation of optical fiber holders [6]), while mode K exposes vertical {100} planes (e.g. to shape silicon beams with rectangular-cross-section [7,8]). Mode P can be characterized as "pbc-defined", since the

underetched inclined surfaces are (roughly) defined by <110>-directed periodic bond chains [3] (pbc's). Mode K can be characterized as 'kink-defined".

Fig. 2 illustrates a schematic view of the silicon crystal structure viewed from a <110> direction. This view looks directly down the channels defined by {111} planes. The labelled planes are all perpendicular to the page in this view. At the left and right of the structure are {100} planes, made up of kinks, as shown. At the top and bottom of the structure are {110} planes, made up of pbc's. The pbc's extend in a direction perpendicular to the page (see refs [3,9] for better views of these features.) In Fig. 2, Mode P corresponds to the bottom-left portion of the figure, while Mode K corresponds to the top-right portion of the figure. The two modes meet at the {111} plane which runs diagonally from top-left to bottom-right.

While the slowest-etching planes are always the {111} family of planes, there are widely-differing reports of the fastest-etching planes. For example, {313}, {212} and {411} families of planes have been reported. As seen in Fig. 2, the {411} is ~19.5° deviated from the indicated {100}, while {331} and {212} are ~18.4° and ~26.4°, respectively, deviated from the indicated {110}. More generally, when the etch is pbc-defined, the fastest-under-etch plane index is of the form {hkh}, where h>k. Conversely, when etch rate is more kink-defined, the fastest-under-etch plane has h<k.

The formation of hillocks during etching on {100} surfaces is another phenomenon of interest in the study of wet anisotropic etching. This research has found that hillocks generally occur when the under-etched inclined planes are pbc-defined, not when they are kink-defined. This distinction may be related to the relative probabilities of attack of kinks and pbc's. This type of relation could be very useful in furthering the theoretical understanding of the chemical and atomic processes involved.

2. FABRICATION OF SQUARE-CROSS-SECTION SILICON BEAM

One implementation of an angular rotation rate sensor (gyro) involves the use of a vibrating beam with matched natural frequencies in two directions of vibration. An x-directed beam is actuated to resonance in one direction (say y), and Coriolis acceleration is detected by monitoring perpendicular (z) sense vibrations. For good sensitivity, the resonant frequencies in the y and z directions must be quite closely matched. If such a device is implemented using a single-crystal silicon beam (to take advantage of the high Q and long-term material stability), a square-cross-section beam must be fabricated with well-enough-matched clamping in the vertical and horizontal directions.

If it is desired further to implement this in {100} silicon by wet anisotropic etching, the task involves several difficulties. Since {111} planes are not vertical in a (100) coordinate system, one must resort to using relatively faster-etching (010) planes for the beam sidewalls. This can be accomplished by orienting the beam mask at 45° to the wafer flat. However, at the corners of the beam, there will appear {111} flanges, quite large because one must etch through the full thickness of the wafer. These flanges will render unsymmetric the clamping in the vertical and horizontal directions, significantly impacting the performance of the sensor.

In order to resolve this problem, a concave corner compensation technique was devised [8,10], in which the {111} planes are etched away at a controlled rate. By carefully designing and arranging a pattern of rectangles in the corner of the mask opening (see Fig.3), the etch front is guided into each corner at the appropriate rate to keep pace with the advancement of the main etch front on the sides of the beam [8,10]. The use of this technique was shown to dramatically reduce {111} flange width, and reduce mismatch of natural frequencies, such that sensor operation was viable.

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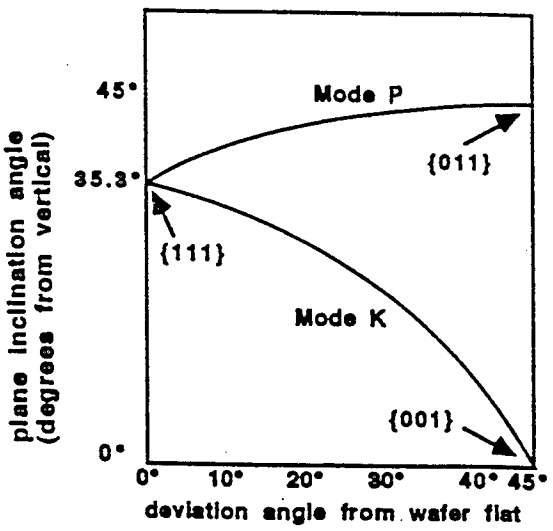


Fig. 1

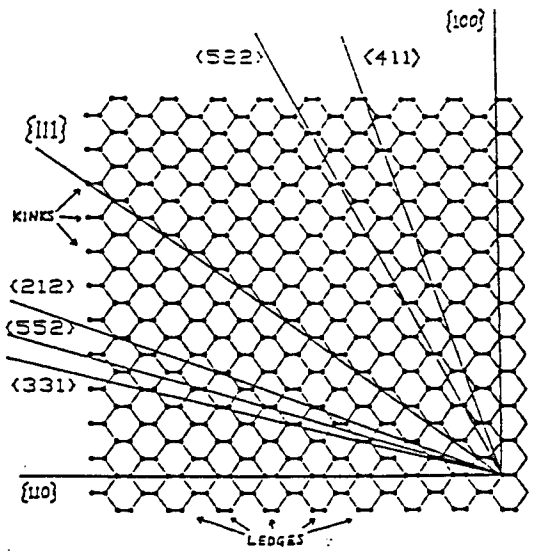


Fig. 2: Schematic view of Si structure from <110> direction.

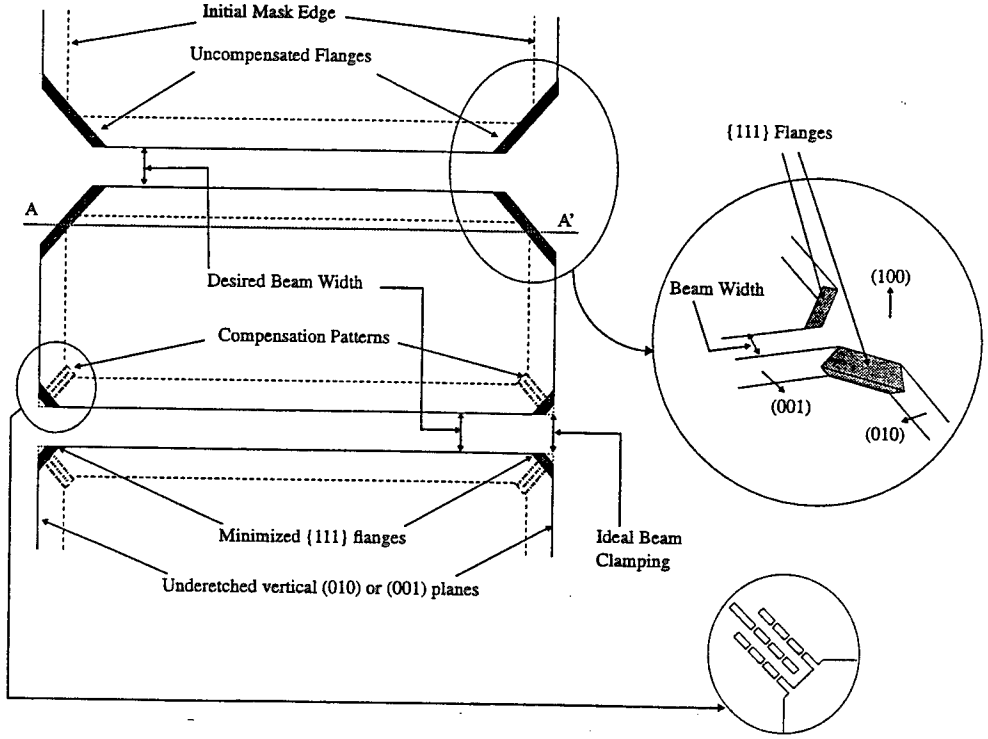


Fig. 3: Top left: structures resulting without compensation patterns. Top right: plan view of {111} "flanges". Bottom left: structures using concave corner compensation patterns, showing reduced flanges. Beam is aligned 45° to wafer flat.

MINIATURIZED DEVICES FOR BIO/CHEMICAL SAMPLE PREPARATION

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ABSTRACT

Micro scale biochemical sample preparation technologies are relevant to many application areas ranging from environmental monitoring systems to miniaturized biomedical analysis systems. In this paper, selected micro fluidic systems are discussed for use as approaches to micro scale sample preparation for biomedical applications. The three systems include a) micro electrical field flow fractionation; b) micro needle technology, and c) micromachined pipette technology. Micro electrical field flow fractionation provides a tool for separation (and fractionation) of particles based on size and zeta potential for particles in a size range of approximately 1 nanometer to 1 micrometer. The micro needle technology is an enabling technology base for the development of needles with micro scale cross sectional dimensions and added functionality. The micro needles are used for conventional drug delivery and sample extraction applications as well as for integration with other miniaturized biochemical analysis systems. The micromachined pipettes are enabling for the manipulation of pL–μL volumes of samples as well as for parallel distribution of samples or reagents on a close (<500 μm) center-to-center spacing.

INTRODUCTION

The miniaturization of biochemical analysis systems has been a topic of growing interest over the past decade. During this time, a large majority of the technical effort has been invested in the development of the primary separation (or amplification) component of the various analysis systems such as the micro columns used in the miniaturized chromatographic systems (e.g. electrophoresis, gas chromatography, liquid chromatography) or the chambers used for miniaturized polymerase chain reaction (PCR) systems. Less efforts have been directed toward the development of technologies for micro scale sample preparation (with the exception of PCR). Sample preparation technologies include methods for purifying, manipulating, interfacing, amplifying, and chemically modifying sub-micro liter volumes of samples for analysis in a miniaturized format. While each of these technologies is available in a macro scale format, most have not been available on the micro scale until recently. During the past two to three years, there has been a significant increase in the worldwide efforts to improve the technology base for integrated miniaturized sample preparation. These efforts have resulted in integrated systems for purifying and sorting samples, manipulating samples, interfacing samples and modular analysis system components, and sample amplification [1].

In this paper, we will focus on the use of micro systems fabrication technologies for the development of three different micro systems for sample preparation. The three systems include: a) micro electrical field flow fractionation; b) micro needle technology, and c) micromachined pipette technology

MICROMACHINED NEEDLE ARRAYS

Micro instrumentation is a rapidly growing area of interest for a broad spectrum of engineering applications. One application of interest to the biomedical industry is the development of microneedles. Some of the smallest hollow needles that are available today have inner diameters of over 200μm. A demand exists for a hollow needle device that can withstand typical handling and subcutaneously deliver medication without the usual discomfort associated with current needles. A schematic representation of such a device, a fluid coupled hollow metallic micromachined needle array, is presented in Figure 1.

Each array is composed of hollow metallic microneedles fabricated on top of a silicon substrate using surface micromachining fabrication techniques [2]. Every microneedle of the array consists of input shafts and cantilevered output shafts. A novel cross-flow design (needle coupling channels) is incorporated to equalize pressure

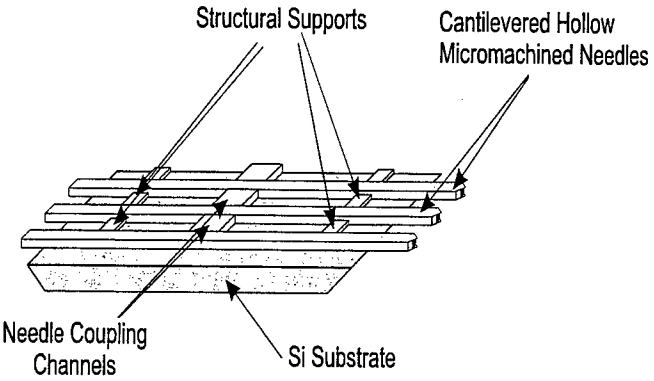


Figure 1. Schematic representation of the fluid coupled micromachined needle array.

distribution and minimize the effects of clogged passages within the needles. The optimum design for the needle coupling channels has been investigated using an ANSYS finite element numerical model [1]. The process used to fabricate the fluid coupled micromachined needle array includes p^+ etch-stop membrane technology, anisotropic etching of silicon in potassium hydroxide, sacrificial thick photoresist micromolding technology, and micro-electrodeposition technology. The fabrication process is low temperature and is compatible with integrated circuit (IC) technology as a post process. The microneedles are fabricated on top of 3-inch silicon wafers using microelectroformed palladium and are subsequently released from the substrate before packaging.

A scanning electron micrograph of a fabricated micromachined needle array released from silicon substrate is shown in Figure 2. The needle coupling channels are positioned at the center of each needle and are 100 μm wide. Two sets of 60×100 μm^2 structural supports are 250 μm from each needle end. The needle wall thickness is approximately 20 μm of electroformed palladium. Each needle channel is 2 mm long, while the total width of the 25-needle array is 5.2 mm. The center-to-center spacing of individual needles is 200 μm.

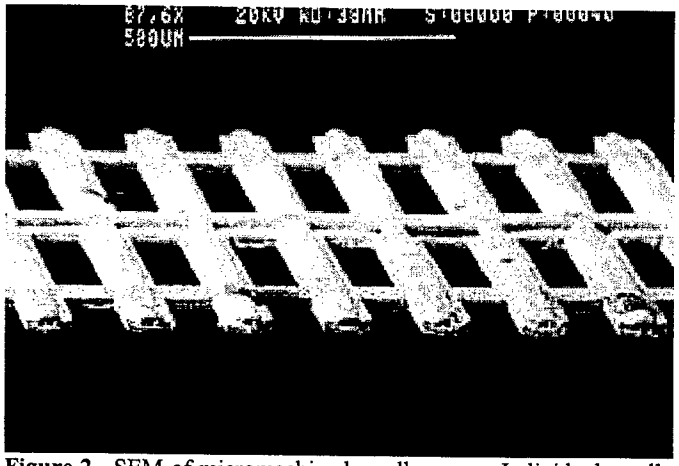


Figure 2. SEM of micromachined needle array. Individual needle channels are 2 mm long and have center-to-center spacing of 200 μm. The inner dimensions are approximately 20×40 μm^2. The total needle array width is 5.2 mm. Needle coupling channels are centered along the length of each needle and are 100 μm wide.

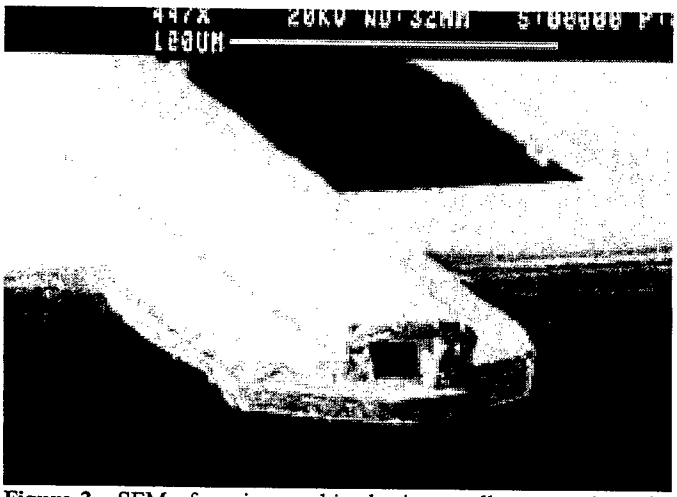


Figure 3. SEM of a micromachined microneedle output tip. The inner dimensions are approximately 30×20 μm^2, while the outer dimensions are approximately 80×60 μm^2.

It is especially important to note the quality of the fabrication of the tip of each needle, since this is the part that will be inserted through skin for drug delivery. Figure 3 is a SEM showing a close-up of one of the needle tips. The inner dimensions are approximately 30×20 μm^2, while the outer dimensions are approximately 80×60 μm^2. The distance from the needle tip to the structural supports is 250 μm. The needle tip is formed by a 45° angle for ease of penetration.

Packaging of the micromachined needle arrays is accomplished using machined acrylic that serves as an interface between a standard syringe and the array. The input end of the interface has a tapered luer fitting that allows connection to a standard syringe. The midsection of the interface contains a region that serves as a fluid reservoir that allows development of flow into individual microneedles and ensures an equal pressure distribution between microneedle inputs. The output end of the interface contains a machined slot in which the micromachined needle array is inserted and permanently mounted using a biocompatible polymeric adhesive.

MICROMACHINED PIPETTE ARRAYS

One of the challenges of future miniaturized biological/chemical analysis laboratories is to manipulate small (sub-μL) samples on a macro-scale in a parallel fashion. Today's commercially available sample handling systems for biochemical analysis are limited to wide center-to-center spacing (3.0 mm) and cannot handle sample volumes less than approximately 0.5 μL. In addition, these systems are able to dispense in the range of 6 to 12 pipettes at one time. With the current trends of miniaturizing biochemical analysis techniques (e.g., electrophoresis, chromatography, PCR) and the drive toward the development of a μ-TAS, techniques must be developed to allow precise macro-scale manipulation of pL to nL range sample volumes in a highly parallel manner.

Therefore, it is important to develop a method for highly parallel macroscale sample loading of pL to μL volumes that would allow precise handling of samples in the pL to μL range and still be compatible with the size dimensions (center-to-center spacing) of the micromachined biochemical analysis systems. One technique that addresses these problems uses micromachined pipette arrays for sample loading of miniaturized biochemical analysis systems.

The micromachined pipette arrays are fabricated using extensions of previously reported surface micromachining fabrication technologies in a manner similar to the process described for the microneedles [3,4].

Each array typically consists of 5 or 7 pipettes. While each pipette had an individual input port, the acrylic interface provides a single pressure source through a manifold. The volume of the manifold is many times greater than the volume of each pipette, allowing a uniform pressure distribution across input ports of the entire array. Thus, the flow through each pipette is assumed to be equal.

Individual pipettes are access through ports that are fabricated by etching through the substrate for backside access. The use of bottom input ports allowed the macroscale interface between microchannels and macro-tubing to be moved from the front of the device to the back, resulting in a more robust interconnect. The interface can also be modified to provide downstream ports for static pressure measurement in addition to the inputs for fluid flow.

An example of a micromachined pipette array fabricated on top of a silicon substrate is shown in 4. These pipettes are 7 mm in length with 2 mm extending from the substrate, while 3 mm separates the pressure ports from the pipette ends. The inner width of individual pipettes is 600 μm while the inner height (the thick photoresist thickness) is 30 μm. The electroplated nickel walls are 20 μm thick.

Interfaces machined from acrylic are used to connect the fabricated micromachined pipette arrays with 397 μm inner diameter Teflon tubing. The acrylic interfaces are attached to the micromachiend pipette arrays using an ultra-violet (UV) curable adhesive. Teflon tubing connects the acrylic interfaces to either a pressure source or a pressure transducer. Photographs of interfaced single-input and double-input micromachined pipette arrays are shown in Figure 5.

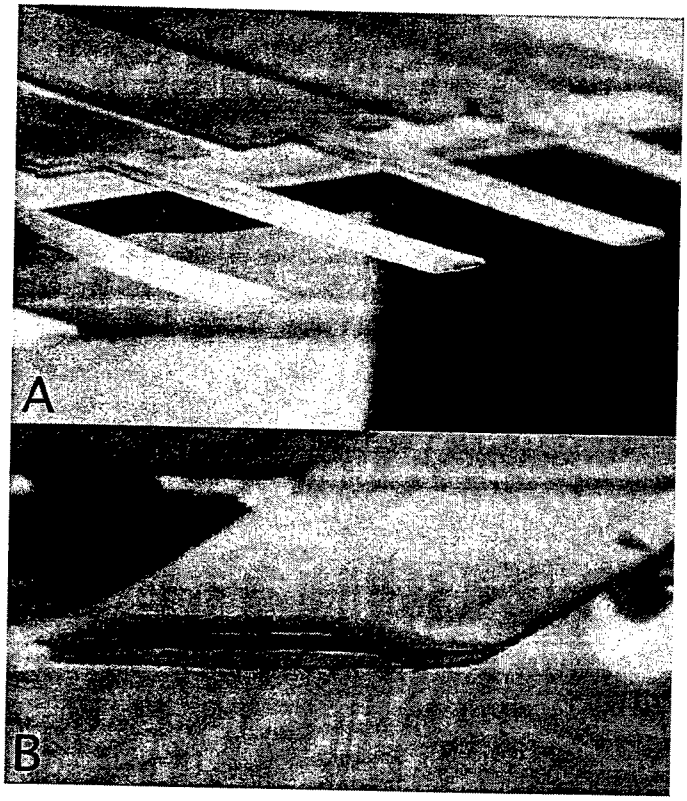


Figure 4. **A**. SEM micrograph of an array of pipettes extending from the silicon substrate. The wide sections are 12750×1500×30 μm^3 (L×W×H). Pipettes extend 1.5 mm from the substrate and are 500 μm wide. The structural material is electroformed nickel with wall thickness of 15 μm. **B**. Close-up of the end of a pipette. The inner cross-sectional area is 500×30 μm^2.

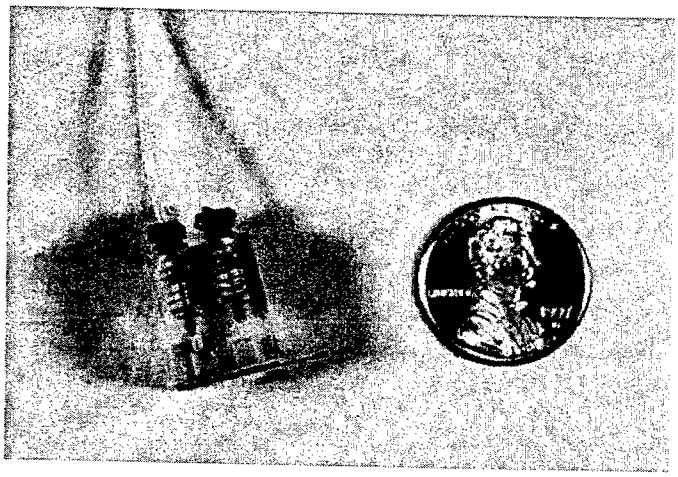


Figure 5. Photograph of a double-input micromachined pipette array interfaced from the backside. Teflon tubing with a 397 μm inner diameter connects the acrylic interface to an external pressure source. A penny is provided for size comparison.

Micromachined Electrical Field- Flow Fractionation System

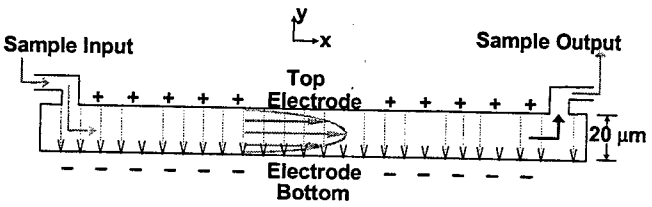


Figure 6. Schematic diagram of the operation of an EFFF system.

Another system that has some unique packaging requirements with which we have been working is the micromachined electrical field- flow fractionation system (μ-EFFF). Electrical Field-Flow Fractionation is a particle separation technique that relies on an electric field perpendicular to the direction of flow and separation as shown in Figure 6. The separations are performed in a low-viscosity liquid (typically an aqueous buffer solution) which is pumped through the separation channel. EFFF controls the relative velocity of particles by forcing particles towards the wall of the channel. Particles with high charge density pack closer to the wall and move more slowly compared to particles of lower charge density that form a more diffuse cloud and move more quickly through the channel. The channels for the miniaturized EFFF system are fabricated by bonding a silicon substrate and a glass substrate together around a photolithographically defined polyimide

spacer. Both substrates have metal thin films on their surface, which are patterned to define the electrodes for the channel and an electrical impedance detector. The input and output ports are fabricated in the silicon substrate using KOH etching and are 200 μm square on the interior of the channel and about 1 mm square on the external face of the silicon substrate. The channel dimensions are typically about 6 cm long, 1-6 mm wide, and 10-50 μm in height. Fabrication and other information about the system has been reported previously [5]. The system also has an integrated electrical impedance detector that has been incorporated at the exit end of the channel. The μ-EFFF system, therefore, requires both electrical and liquid connections. The electrical connections are rather straightforward with the only complication being that connections must be made to two parallel substrates separated by a very small distance and covered by polyimide. The fluid flow connections are much more demanding and include a need for sample injection into the system. The electrical and fluid connections will be covered separately. The electrical connections for the prototype μ-EFFF system were made by bonding small diameter wire to the metal bond pads using an electrically conducting adhesive. The resistance of the connection was typically 2-3 Ω with very good strength and flexibility. The requirements for the fluid flow connections in the μ-EFFF were much more demanding and included the following, a) ability to withstand up to 20 psi (140 kPa), b) flow area match with channel, c) accurate positioning of connections, c) flexible connections to allow component changes, and d) biocompatibility and no leaching components. In addition to these requirements, the two ends of the channel do not have identical requirements. At the entrance of the channel there is a requirement for sample injection while the exit of the channel connects only to a drain or fraction collector. The ideal though, we be to have the same basic configuration that can be modified for either purpose. The connection is made by bonding a polypropylene ferrule for 1/16" tubing from Upchurch Scientific over the port using a biocompatible UV cured adhesive (Loctite 3301). Just a small amount of adhesive can be used to position the ferrule since further bonding will be performed later. This step is critical in that the position of the ferrule determines the position of the tubing later on. To facilitate accurate placement of the ferrule (which can usually be done visually), some large bore tubing can be placed in the ferrule with either some wire or a needle through the center of the tubing. The wire or needle can then be placed into the port to insure that the tubing is centered over the port. Once the ferrule has been adequately positioned, tubing can be placed into the ferrule and seated against the silicon substrate. At low pressures the friction fit is sufficient to prevent leakage, but for most applications additional adhesive can be applied to prevent leakage even at high pressures. The tubing of choice for this application is Tefzel tubing from Upchurch Scientific. Tefzel can be securely bonded using most adhesives while Teflon tubing is nearly impossible to bond with any strength. Steel and titanium tubing have also been used in this application, but they tend to transmit torque and bending moments very well which can cause loss of adhesion or outright fracture of the adhesive or the silicon (due to the small diameter and long moment arms, the torques can be very high even at low applied forces). This setup meets all of the requirements specified earlier and can be assembled in about five minutes due to the fast curing of the UV-cured adhesive. An external sample injection system is used since the flow into which the injection is made is pressurized and the addition of valves would greatly increase the complexity, cost, and losses in the system. Additionally, the external system eliminates losses in analyte and still functions adequately, though and on-chip injection system would likely improve the resolution of the separation system. A schematic of the injection system is shown in Figure 7. This configuration has several advantages including ease of setup and reconfiguration for other attachments, sample injection in or very near the entrance of the channel (which improves resolution in the system and eliminates the time required for sample transport to the channel), there is no flow blockage during injection which eliminates pressure buildup, and the connections are very robust with high resistance to applied forces.

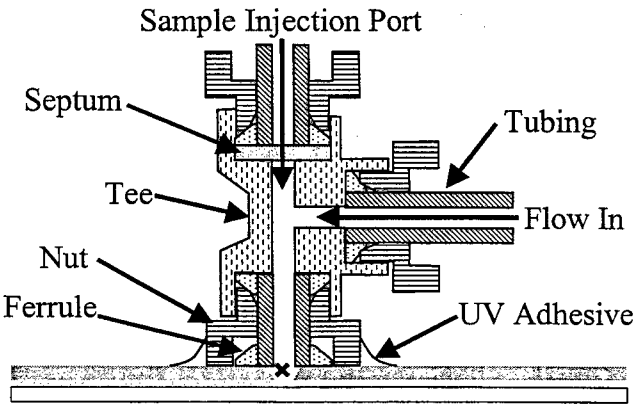


Figure 7. Cross section of the sample injection system showing the inverted nut bonded to the silicon substrate, the injection tee, and the configuration of the attached components. The X marks the point of sample injection.

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Recent Advances In Micromachined Millimetre and Submillimetre Waveguide Components

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The implementation of micromachining techniques for the fabrication of millimetre and submillimetre waveguide circuits promises a cheap and flexible means to realise high performance components. This talk will describe a particularly versatile fabrication approach presently being developed at RAL. The technique uses a combination of anisotropic Silicon etching and high aspect ratio, multilevel UV lithography in both positive and negative tone resist. As such it leads itself ideally to the realisation of harmonic waveguide circuits as well as the integration of active devices into waveguide packaging.

Process Technology for Manufacturing High Reliability Capacitive Pressure Sensors

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1. INTRODUCTION

Silicon- based pressure sensors for control of industrial processes are manufactured using a blend of materials and processes which have been utilized for years in the semiconductor industry and those which have evolved specifically for MEMS (micro electromechanical systems) devices. These sensors exploit both the mechanical and electrical properties of silicon. Capacitive sensors, including the Moore Mycrosensor™, use pressure-sensitive capacitors to measure changes in pressure, flow, and level. are designed for high reliability operation, stability over time and temperature, and high manufacturing yield.

Capacitors are ideally suited for measuring pressure because they provide a significantly higher gage factor (10 to 100 times) than strain gauges[1]. The term "gage factor" refers to the ratio of the change in applied force to the change in the sensor output. A high gage factor indicates a more sensitive sensor that needs less amplification, has greater stability, and has a higher turndown than other sensors. In conjunction with an oscillator circuit, a capacitor's response to pressure produces frequency outputs which indicate applied pressure.

II. SENSOR DESIGN

Fig 1 shows the structure of the dual capacitor pressure sensor. Glass and silicon substrates are separately metallized, etched, and cleaned, and are then anodically bonded together to create a permanent, reliable structure which is able to withstand applied pressures of up to 500 psi. Each sensor has two capacitors, a sense capacitor (Cs) and a reference capacitor (Cr). Each capacitor includes a metallized top glass plate, which is stationary, a silicon diaphragm plate, and silicon fill fluid, which serves as the dielectric. The silicon plate of the sense capacitor deforms with applied pressure, and the resulting movement of the plate changes the distance between the plates, thus changing the capacitance of the sense capacitor. The silicon plate of the reference capacitor is subject to equal pressures on both sides of the silicon plate, and thus provides a constant capacitance from which the incremental capacitance change of the sense capacitor can be compared.

The sensor's capacitors are measured by using the sensor in a frequency determining circuit using an enhanced mode oscillator (EMO). This IC provides an output frequency whose period is proportional to the capacitors which make up the sensor. The output frequency of the circuit is determined by the following equation:

$$f = 1/RC$$

where f is the output frequency of the circuit
R is the fixed resistance of the circuit
C is the varying capacitance of the circuit

The equation shows that a change in the value of the capacitor is inversely proportional to the output frequency of the circuit. Figure 2 shows a schematic drawing of the sensor circuit.

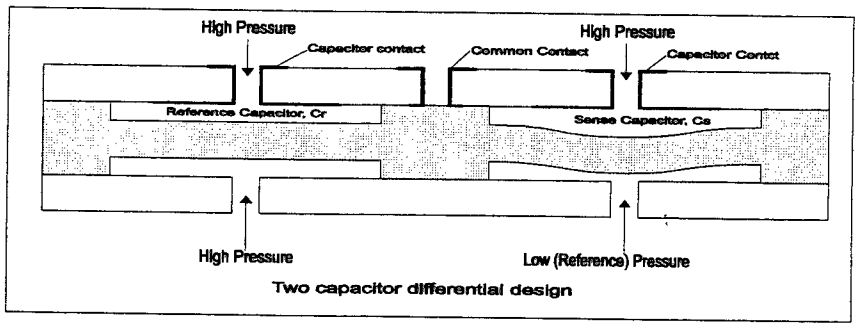


Figure 1 Cross-Section of Sensor

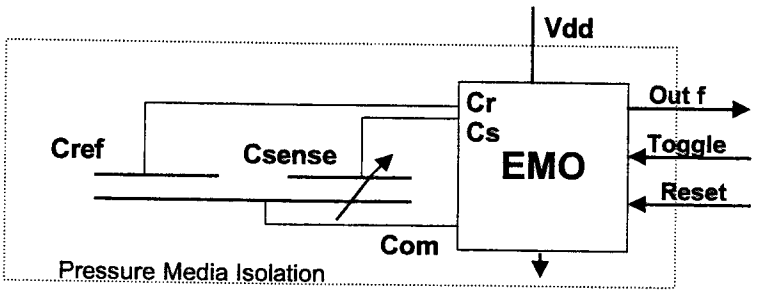


Figure 2 Sensor Functionality Schematic

III. SENSOR MANUFACTURING

Pressure sensor manufacturing must be carefully controlled to ensure consistent performance of the finished device. Variations in material properties of glass and silicon, as well as variations in anodic bonding parameters, can all introduce instabilities in the assembled sensor.

a. Top Glass:

Pyrex 7740 borosilicate glass is chosen for its close match of its coefficient of thermal expansion to that of silicon in the temperature range commonly used for anodic bonding.[2] The glass must be polished to provide a TTV of 20 microns or less to facilitate anodic bonding. The cleanliness of the glass substrates from the supplier must also be closely controlled.
Holes are drilled through the glass to provide for pressure inlets to the silicon diaphragm. These holes can be laser , ultrasonically, or etched, depending on the shape of the hole and the taper of the hole sidewall, if any is required. Laser drilled holes add considerable thermal stress to the glass, but provide flexibility of sidewall angle. Ultrasonic drilling is less stressful, but provides only nearly vertical sidewalls. Etching is very slow, but allows freedom of hole size and shape. The Mycrosensor top glass uses tapered holes and sputtered aluminum, chrome, and tungsten to make wire-bond connections on the top side of the sensor that connect with thin film capacitor plates deposited on the underside of the top glass.

b. Diaphragm Silicon:

The starting material of the diaphragm silicon is double-sided polished <100> P-type silicon, 50-400 microns thick, depending on the pressure range of the device. Diaphragm areas are created using standard photolithographic techniques, using silicon dioxide as an etch mask. The silicon is etched on both sides to thin the wafer by 3-10 microns using KOH (22% KOH,

78% H_2O by volume) at 70°C. The etch rate is highly dependent on temperature; therefore, the etch bath must be well-controlled to within 1°C. This silicon etch creates the gap of the capacitors. After the initial etch, the front of the wafer is protected and additional silicon is removed as required from the backside of the wafer to adjust the thickness of the diaphragm. Etch depths are controlled by strict etch bath parameter control and are monitored by surface profilometry. After the etch depths are within requirements, the silicon dioxide is removed using a buffered HF etch.

c. Bottom Silicon/ Glass Assembly:

A rugged bottom assembly is fabricated to provide structural robustness to the sensor at operating pressures. This assembly is composed of a thick <100> P-type silicon wafer, 1275 microns thick, with a thin glass substrate to facilitate anodic bonding of the bottom silicon to the diaphragm silicon. The bottom silicon is metallized with aluminum which will be wirebonded to surrounding circuitry to minimize electrical noise. The silicon wafer and glass substrate are processed separately, then anodically bonded together to form the bottom assembly.

As mentioned previously, the individual glass substrates and silicon wafers are chemically and plasma cleaned, then aligned and anodically bonded together to form the sensors. Bond conditions are 400-450°C at an applied voltage of 500-1000 volts. The cleanliness of each substrate is critical to a successful anodic bond. Particles and residues will cause voids and poorly bonded areas, resulting in inconsistent behavior at high pressures. Choosing the proper anodic bond parameters can minimize thermal stresses and the resultant bow in the bonded pair.[3]

IV. UNIQUE MANUFACTURING ISSUES

Sensor manufacturing often involves creating cavities and other non-planar structures which present unique processing challenges.

Wet etching and cleaning processes, which would be straightforward with planar devices, become difficult or impossible once cavities are introduced. Spin processes can not always be used. Liquid photoresists often must be applied by spray methods, or dry film photoresist can be used to tent over through holes and cavities, though with a loss of pattern resolution.

Dicing the completed glass/ silicon assembly into individual sensors is also more difficult with cavities, as dicing requires copious amounts of water for cooling. Dicing tape is successfully used in the Mycrosensor™ processing to protect the top side of the sensors. Several dicing tapes have recently been introduced and are useful:

1. UV release tapes, which exhibit high tack until they are exposed to approximately 1000mJ of ultraviolet light, when they become very low in tack and can easily be removed.
2. Heat release tapes, which are high tack, but release when heated to 90-150°C.

V. MARKET FORCES IN SENSOR MANUFACTURING

As the sensor market continues to mature, and MEMS applications expand, demands for higher performance and lower cost will remain the primary drivers for the following:

1. Process innovations and standardization
2. Integration of mechanical and electronic components
3. Chip size reduction
4. Higher quality substrate materials
5. Process equipment specifically designed for MEMS

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MEMS DEVICES BASED ON THE USE OF SURFACE TENSION

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1. INTRODUCTION

Surface tension, a line force, is a unique type of force, which scales directly to length. When the dimension of interest shrinks down to sub-millimeter range, the size range typical for MEMS devices, surface-tension force becomes dominant over most other forces, such as those based on pressure (surface force) or mass (body force), e.g., see [1,2]. This dominance of surface tension has most typically been the source for a serious hindrance against successful fabrication and operation of microdevices, calling for elaborate analyses and fabrication techniques in MEMS [3-6].

A completely different approach would be to design microdevices which *use* surface tension. Unfortunately, however, there has been little knowledge on how to make a machine run by this unfamiliar force. This presentation reports our on-going effort to establish surface tension as a useful force for microdevices and eventually a main driving force for micromachines. We explain several examples of using surface tension for microdevices, including an exploration to implement continuous electrowetting (CEW) phenomenon for MEMS devices in order to control surface tension and drive microdevices.

2. MECHANICS IN MICROSCALE

Manifestation of the scale effect is abundant in nature, as we see ants not collapsing from the loads they carry but helplessly trapped in a water droplet, small creatures climbing up the wall, or a water strider running on water surface. It is interesting that biologists reported by empirical observation of nature that surface force becomes more important than body or muscle force in the world below 1 mm scale [1], the domain we did not experience building mechanical systems in until the advent of MEMS. By the way, be reminded that typical MEMS devices are even smaller than ants by orders of magnitude.

If human beings were creatures of sub-millimeter in size, the main force of interest to us would have been surface tension. If a thousand times smaller, we would fear being stuck to many liquid surfaces around us but never worry about getting hurt falling. In this scale, it is interesting to suspect that we might have invented many machine that are driven by surface tension.

Indeed there have been a few attempts in MEMS to utilize surface tension, some passively using surface tension to block unwanted movements and some actively controlling it to induce movements. Let us start with passive examples.

3. PASSIVE USE OF SURFACE TENSION

Many examples can be found that use surface tension to stabilize small objects, such as picking up a contact lens with a finger tip. Those with an engineering flavor include such examples as keeping ink from leaking through the micro-nozzles in the popular inkjet printers. This stabilizing effect can be used much more elaborately for the microdevices made by MEMS technologies.

Figure 1 shows a novel droplet ejection mechanism that uses the flow-blocking effect of bubbles in microchannels. Due to the large surface tension in microscale, the bubble in microchannel functions as a check valve, which can be created thermally by a patterned resistor and elminated by conductive heat dissipation. With a bubble in place (i.e., virtual check valve closed), a droplet can be ejected with high pressure without the problem of chamber-to-chamber cross talk. With the bubble collpased (i.e., valve open), ink refills the microchamber quickly without much restriction in the flow path. The result is a high

frequency droplet ejection without any microvalve fabricated. The device demonstrated an ejection frequency several folds higher than commercial inkjet printers (e.g., from 5 kHz to 35 kHz), not to mention the complete elimination of the so-called satellite droplet, with no added fabrication complexity [7,8].

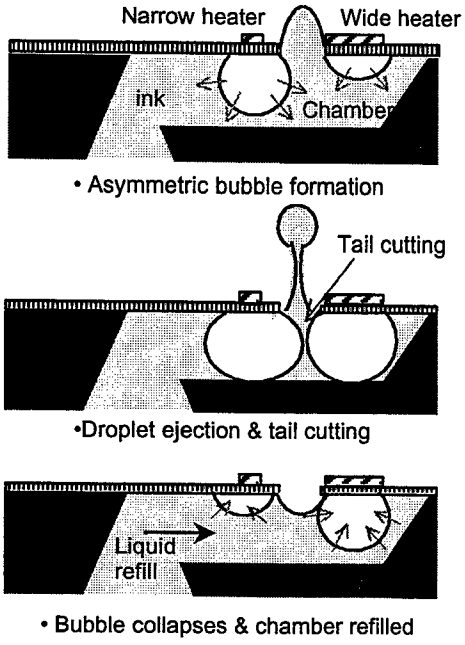


Fig. 1. Principle of bubble valve for micro injector [7,8]

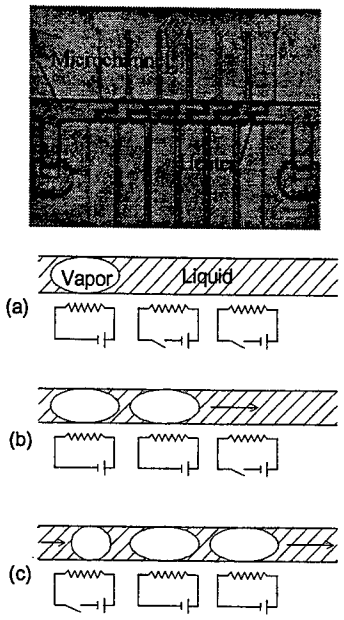


Fig. 2. Valveless micropump using bubbles [9]

It has been shown that sequential generation of thermal bubbles can pump the liquid in microchannel [9]. In Fig. 2, the bubble on the left side functions as a check valve while a new bubble is formed and expands on the right side. The effect is a non-symmetric expansion of the new bubble and flow of liquid to the right. This valveless pumping mechanism, demonstrated with 2 μm high, 10 μm wide microchannels made of SiO_2, has produced about 200 μm/s of flow velocity and pressure head of 800 Pa.

Taking advantage of the strong physical stability of droplets in microscale, even a droplet-based microswitch shown in Fig. 3 can be made. A droplet of liquid metal (e.g., mercury), 5-20 μm in diameter, closes the circuit between the reference line and one of the two electrodes. The bistable droplet can be moved to switch by electrostatic attraction. Yet, it is stable against physical disturbances even at thousands of G's, thanks to the high surface tension and negligible inertia effect in microscale. Since the switch contact is between metal and liquid metal, many of the typical contact problems in solid-solid contact switches can be eliminated. The droplet being the only moving part, as opposed to the long beams found in typical microswitches, an array of microswitch as densely populated as LSI circuits can be envisioned.

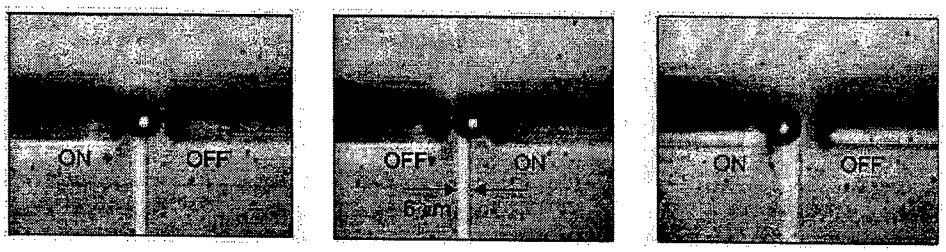


Fig. 3. Microswitch with a droplet of liquid metal (switching at 70 V)

4. ACTIVE USE OF SURFACE TENSION

More ambitious goal is the active usage of surface tension, such as driving liquids directly by surface tension. Surface-tension-induced motion is possible by creating surface tension difference in fluid-fluid or fluid-solid interface. There are several ways to control the surface tension, such as chemical (i.e., use of surfactant), thermal (e.g., Marangoni force), and electrical methods (i.e., electrocapillary, [10,11]). Among them, use of electrocapillary appears most promising due to the energy efficiency (vs. thermal) and potentially simple and long-lasting operation (vs. chemical), as well as the simplicity in realizing by microfabrication.

Continuous electrowetting (CEW) principle

While the electrocapillary, in general, refers to a relationship between surface tension change of liquid metal due to applied voltage, continuous electrowetting (CEW) refers to a principle of *moving* a lump of liquid metal using electric potential [10]. In brief, a drop of liquid metal (typically mercury) travels along an electrolyte-filled channel or tube when electric potential is applied across the length of the channel. The movement of a mercury slug in electrolyte is due to the local change of surface tension.

Figure 4 shows a state of electric charge distribution at the mercury-electrolyte interface, which is responsible for surface tension gradient according to Lippman's equation [10], and the motion induced by it. The electric potential across the electrical double layer becomes higher as x-coordinate increases. The surface tension decreases as the electric potential increases and the motion occurs to the right where the surface tension is lower. Movement of the mercury to the lower surface-tension area can be interpreted as the tendency to minimize the energy by wetting low surface tension region more than the higher one.

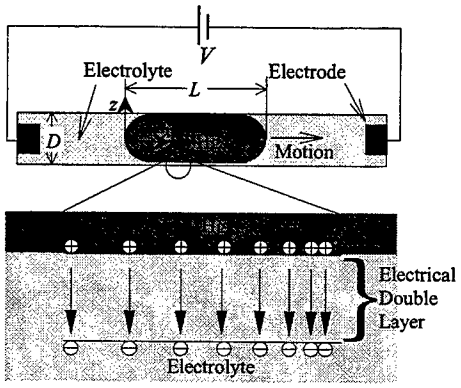


Fig. 4. Continuous electrowetting (CEW) effect

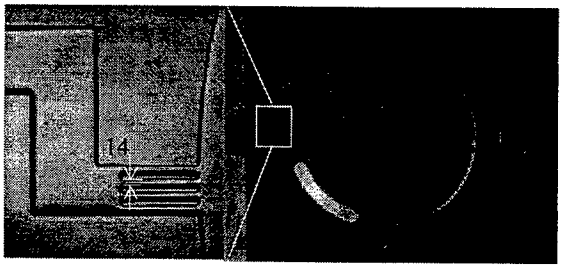


Fig. 5. Liquid micromotor under testing [15]
Diameter of the channel loop is 2 mm.

Liquid micromotor

Using the enabling technologies developed to make microscale mercury droplets on lithographically defined spots and to encapsulate electrolyte in lithographically defined region [12,13], CEW effect has been realized with MEMS [14,15]. Although the moving distance of the liquid metal is found limited for microscale devices due to the severe polarization effect caused by the unusually small size of the electrode, a long-range movement can still be obtained by alternating the polarity to the overlapping electrodes. The application of long-distance travel strategy to a loop of channel results in indefinite circular motion of a liquid metal droplet, which we call a *liquid micromotor*.

Figure 5 is the liquid micromotor under testing. The loop diameter is 2 mm, channel width is 200 μm, and the deep-RIE depth is 20 μm. This liquid micromotor demonstrated successful operation with maximum speed of 420 rpm at only 2.8 V and an average current around only 10 μA. This is in contrast to electrostatic actuation, which consumes little current but typically requires high voltage, and electromagnetic or thermal actuation, which uses low voltage but consumes high current. Being a liquid

motion, the movement of the liquid-metal slug by CEW is very smooth and free from dry friction and wear from which many microactuation mechanisms are suffering. We thus anticipate a long operating life cycle and reliability with this type of devices. Numerous devices in different application areas are expected, such as micro inertia sensors and motors (e.g., momentum wheel), micro switches, and micro optical switches.

5. SUMMARY

Surface tension dominates almost all other forces in microscale, but there is little knowledge on how to make use of it in designing mechanical devices. Summarized was our on-going effort to establish surface tension as a useful force for microdevices and eventually a main driving force for micromachines. Several examples of using surface tension for microdevices, some passive and some active usage, have been described. Most noticeable is the exploration of continuous electrowetting (CEW) phenomenon in order to electrically control surface tension and drive microdevices. The efficiency of this microactuation method is unprecedented: low voltage (2-3 V), low power consumption (~10 μW), and no dry friction between solid elements. Initial testing shows successful operation of a liquid micromotor.

ACKNOWLEDGEMENTS

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FTIR-Spectroscopic Characterization of DNA Macromolecules

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1.Introduction

The development of new techniques for the detection and identification of biological materials is a very important and challenging scientific problem at this time. Previous studies have indicated that spectroscopic characterization of ribonucleic acid (RNA) and deoxyribonucleic acid (DNA) polymer chains in submillimeter-wave range (3-300 cm^{-1}) reflects low-frequency molecular internal motions. For example, twisting, bending and stretching of the double helix, sugar pseudorotational vibrations and fluctuations of hydrogen bonds can all give information regarding the three-dimensional structure and flexibility of DNA double helix. Theoretical results have indicated that low-frequency deformations in DNA are extremely sensitive to its nucleotide composition and three-dimensional structure, and have an impact on the main processes related to transferring of genetical information, such as replication, transcription and viral infection [1]. This indicates that the long-wavelength phonon spectra should reflect features specific to the DNA sequence. Hence, phonon modes that arise in the very far-infrared region can serve as a signature of specific DNA-molecules.

This paper will present experimental results on DNA spectroscopy with emphasis on the submillimeter range. Semi-dry films made from randomly oriented DNA fibers and other biological materials such as Bacillus subtillis (BG) have been studied. The goal of this spectroscopic investigation is to confirm the fundamental character of the resonant spectra in submillimeter wave range and to demonstrate the feasibility of long-wavelength vibration spectroscopy as an approach for identification of DNA signatures.

2. Experimental technique

The study was performed using Fourier-Transform Infrared (FTIR) spectroscopy over the spectral range from 300 GHz to 100 THz. The DNA films were prepared by dissolving herring and salmon DNA sodium salts from Sigma Chemical Co. in glass-distilled water with a concentration ratio between 1: 5 and 1:10. The material formed a gel that was brought to the desired thickness by placing the gel inside an arbor shim between two Teflon sheets. The assembly was left to dry at room temperature for several days. The samples were then completely separated from the mold. All the far IR results were obtained from freestanding films. Films of various thickness were studied to confirm that the observed resonances were directly attributable to the absorption characteristics of the biological material. In most cases, interference effects were not observed experimentally due to variations in the optical thickness across the sample. In these cases, the absorption coefficient spectra were calculated from results of transmission measurements of two samples with different thickness. At the same time, our preliminary study of all available experimental data, including data from existing publications, indicated that the effects of multiple reflections in the system and at both sample surfaces could cause significant errors in the interpretation of experimental data in the very far IR. Indeed, this is one of the most important reasons for poor reproducibility of result. Thus, the consideration of interference effects has been included in the analysis of all the data in this work [2].

To provide adequate signal-to-noise ratio all the measurements are performed using a bolometer cooled to 1.7 K by liquid helium under vacuum. All the measurements are made in vacuum so that water absorption does not affect the spectra. To improve the reproducibility of the results, over 200 measured interferrograms were averaged to form each spectrum. Here, each sample was measured several times in the same position, and the procedure was repeated for

several different sample positions. Finally, samples of different thickness were measured and the results averaged to provide reliable absorption coefficient spectra.

3. Background

A general view of an absorption coefficient spectrum over an extended frequency range is presented in Figure 1. Above about 10 THz (300 cm^{-1}) the absorption spectra consist of numerous sharp, well defined resonances (regions I and II). They represent different covalent short-range, high-energy interactions that have been relatively well studied primarily by Raman spectroscopy. These features tend to be independent of the base-pair sequence. For this study we are interested in region III. Here, in the very far infrared, specific spectral features of different DNA molecules are expected to be found that can be used as a mechanism for understanding the functions of DNA in biological processes and, potentially, for identification of DNA signatures. The absorption coefficient is low in this range and eventually drops to zero at wavelengths of about 3-5 cm^{-1}. This frequency range has not been widely investigated because of the many challenges for both experimental and theoretical researchers. Experimental difficulties arise from the low energy of sources in this spectral range, between the upper end of the microwave spectra (~100 GHz) and the lower end of the extreme far IR at 1000 GHz. The low absorption of material in this region necessitates samples with large areas and thickness which are difficult to achieve. High absorption by water masks absorption by biological material in solutions. As a result, several sharp bands that were earlier observed in the very far IR have not subsequently confirmed. Also, the interpretation of observed features is not straightforward. Hence, previous investigations have not definitively established the existence of DNA phonon modes at submillimeter-wave frequencies. For these reasons, we focus our efforts on measuring highly resolved and reproducible spectra in the very far IR.

4. Results

Figure 2 shows the absorption spectrum of Herring DNA in a range between 2000 cm^{-1} and 400 cm^{-1} (1800-1500 cm^{-1} - in plane double-bond vibration of the bases; 1500-750 cm^{-1} - backbone sugar vibration modes [3]). The difference between our results in this range and those given earlier is that we receive not simply the transmission of samples, but quantitative characteristic of the material (i.e. absorption coefficient spectrum). The position of peaks here is well reproducible and practically the same for both salmon and herring DNAs. Bacillus subtillis has additional absorption bands since it is a more complicated specimen. Around 200-500 cm^{-1}, a dip in the absorption coefficient spectrum is observed at about 300 cm^{-1} (Figure 3). This is the short wavelength edge of absorption related to low energy vibrations (weak bonds and non-bonded interactions in DNAs). This edge was previously predicted by a theoretical analysis [4]. In

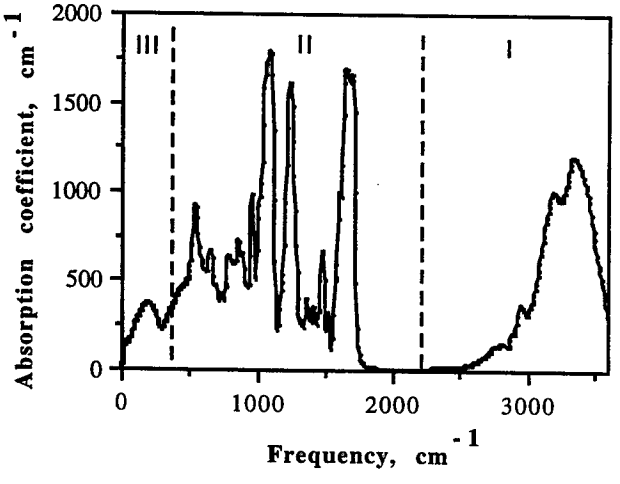


Figure 1. Absorption spectrum of Herring DNA in the extended energy range.

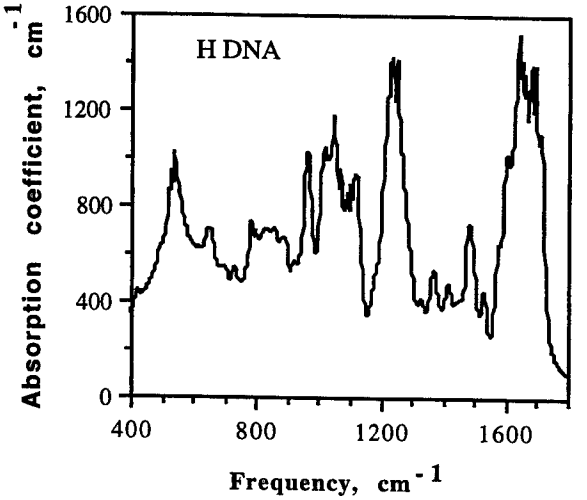


Figure 2. Absorption spectrum of herring DNA film in the IR.

this spectral range we also see weak features, basically shoulders, that are more easily detected in the derivative spectra. The position of the peaks in the derivative spectra are the same for herring and salmon DNAs, but the presence of these features and the magnitude of peaks are very sensitive to water content in the gel used for film preparation. Earlier, spectral features observed in the spectra of nucleic acids in the region 300-500 cm^{-1} were assigned to the ribose ring vibrations [5]. Many difficulties were encountered in the spectral range below 100 cm^{-1} (3 THz). Spectra in this region are strongly influenced by the water and salt contents in the sample. The results confirm increasing absorption in samples with higher water content. Some of these results were reported earlier [6,7]. Figure 4 demonstrates the transmission for samples of different thickness, d. Clearly, the position of the transmission maximum depends on d, which indicates the important contribution from multiple reflection at two film surfaces. The results are consistent with an interference pattern, and calculated values of absorption coefficient are shown in the Figure 3 at the low frequency end.

The basic findings and most important aspects of this research are now presented. A broad series of measurements carried out in this frequency region with a higher resolution of 0.2 cm^{-1} revealed fine features in the spectra which can be more or less pronounced depending on the sample. The transmission spectra demonstrating this fine structure are given in Figure 5 for both salmon and herring DNAs. This fine structure was found to be independent of sample-preparation water content. Peaks appear with a density of approximately one per cm^{-1} in the interval between 10 and 200 cm^{-1}. This general density of frequencies in this regime has been predicted earlier by others [8]. The intensity of absorption lines gradually drops toward the upper end of the band. Here, the aperture of spectrometer determined the lower-frequency limit. **As far as we know, this is the first demonstration of submillimeter-wave spectroscopic features that can serve as DNA signatures.** However, it is extremely difficult in this spectral range to separate real peaks from the noise and other artifacts. The sample from Figure 6 was measured multiple times over a period of several weeks and reproducible results were achieved. However, each measurement was made with significant averaging of results (3x 128 interferrograms), and some variation in results was observed. In general, a process of raw data generalization is required to extract regularities and eliminate false structures resulting from system noise, contaminated samples and interference effects.

5. Discussion

It was pointed out in [9] that since DNA polymers are of low symmetry, and none of the spectral line are truly forbidden, this low frequency region should reveal many features related to biopolymer structure. A theoretical study of a double helical DNA fragment (Poly dAdT)$_6$(Poly

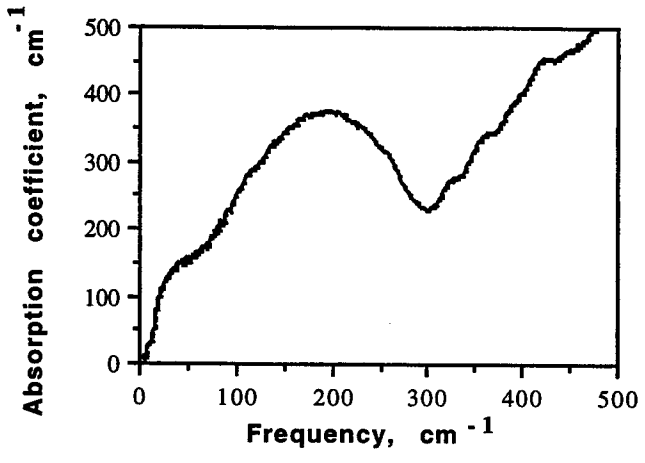


Figure 3. Absorption spectrum of herring DNA in the range 10- 500 cm^{-1}.

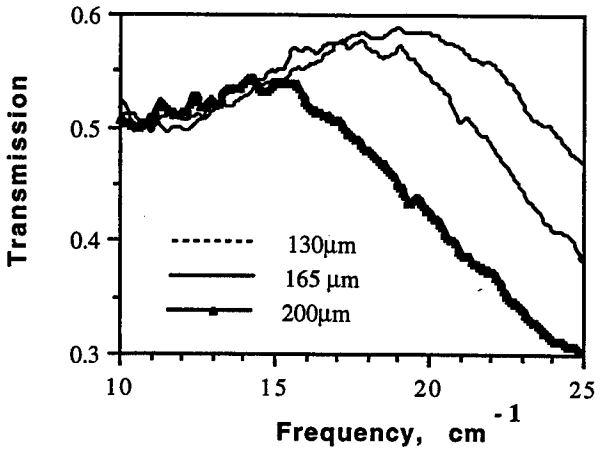


Figure 4. Change of transmission spectra of herring DNA in the range 10-25 cm^{-1} depending on sample thickness.

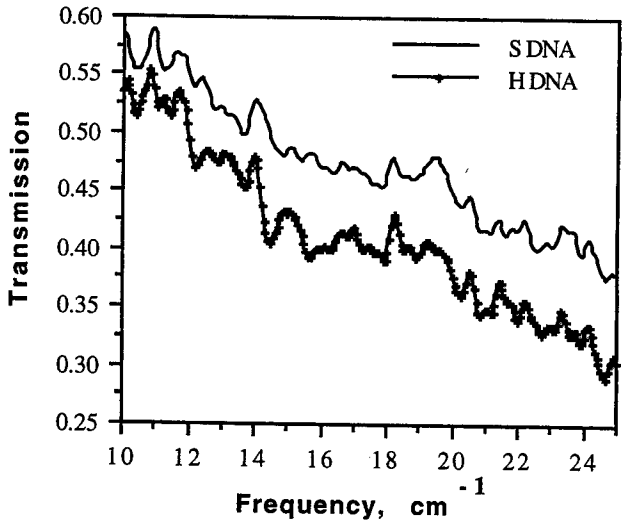


Figure 5. Fine structure in transmission spectra of Herring (H) DNA and Salmon (S) DNAs in the range 10-25 cm^{-1}.

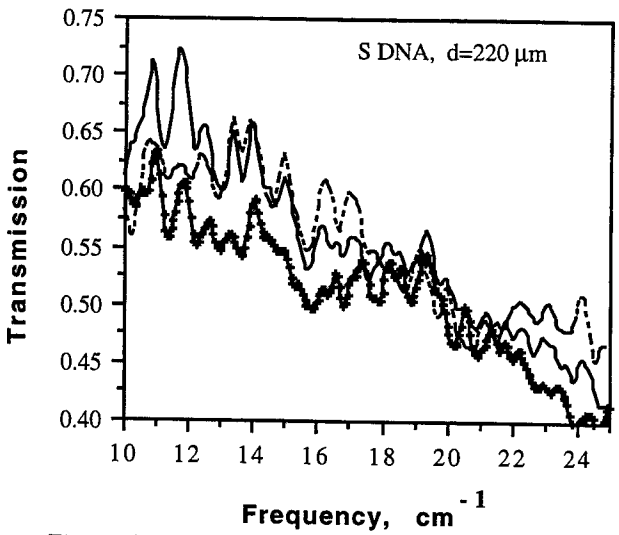


Figure 6. Fine structure in transmission spectra of Salmon DNA in the range 10-25 cm^{-1}. Three independent measurements.

$dTdA)_6$ carried out by our group has applied a first-principles normal mode analysis to predict over 360 normal modes [10]. Most of these modes are below 220 cm^{-1}, with the density higher than one mode per cm^{-1}, which is approximately what was observed experimentally. As predicted by the theoretical research, the observed modes are determined primarily by long-distance interactions, and do not overlap with those produced by vibrations of covalent bonds (above 500-1000 cm^{-1}). Therefore, one can reasonably expect variations in order, over moderate to short range, within the macromolecules to impact modal frequencies, and absorption intensity. Thus, these experimental results have demonstrated the possibility of exploiting long-wavelength (i.e., down to 10 cm^{-1}) FTIR spectroscopy to characterize films of DNA polymers. While these results are positive and lay an initial foundation for the method, extensive research will be required to completely demonstrate the feasibility of long-wavelength phonon spectroscopy and enable a revolutionary new bio-sensing technology.

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Comparison of 14Å $T_{OX,EQ}$ JVD and RTCVD Silicon Nitride Gate Dielectrics for Sub-100 nm MOSFETs

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I. INTRODUCTION

It is well known that tunneling leakage current will likely limit the scaling of SiO_2 gate dielectric thickness to 15 Å [1]. In addition, defect-related reliability concerns may set the limit at 22 Å [2]. The limiting electrical thickness will be larger by 4 Å due to the quantum-mechanical inversion charge layer thickness [3] and several angstroms more due to poly-Si gate depletion. In order to meet the projected future needs for sub-20 Å gate dielectric [4], some high–k dielectrics will be required. Although recent literature on the demonstration of high-k gate dielectrics in MOSFETs has focused on materials such as Ta_2O_5 and TiO_2, silicon nitride has the obvious advantage of simpler process integration into existing CMOS technology, and may be the first practical post-SiO_2 gate dielectric material.

In general, conventional chemical-vapor-deposited (CVD) nitride has been considered to be inferior in quality, so that oxynitride comprised mostly of oxide has been widely studied, but it is not sufficient for use in sub-20 Å thickness range. Recently, two process technologies have been shown to be attractive candidates for forming sub-20 Å nitride gate dielectric stacks. Jet-vapor-deposited (JVD) nitride has been studied as a candidate gate dielectric in the 30-60 Å range for many years. 1 μm Al-gate NMOSFETs with 15 Å $t_{OX,EQ}$ (equivalent SiO_2 thickness) JVD nitride have been demonstrated [5]. A more recent entry is RTCVD nitride with an oxynitride buffer layer at the Si interface [6]. Sub-micron n- and p-channel MOSFETs with ultrathin (18.5 Å) rapid thermal CVD (RTCVD) nitride have recently been demonstrated. In this work, the suitability of JVD and RTCVD nitride gate-dielectric films with 14 Å $t_{OX,EQ}$ applied to sub-100 nm channel length MOSFETs is studied.

II. DEVICE FABRICATION

A LOCOS CMOS technology was used to evaluate the nitride films. JVD nitride films were deposited at Yale University. In the JVD process, the kinetic energy in the supersonic vapor jet provides the energy for chemical decomposition. Therefore, high temperature is not needed. After deposition, the films were annealed at 800°C in N_2 ambient for 5 minutes. The RTCVD nitride films were deposited at UT-Austin. In the RTCVD process, a SiON interfacial layer was grown in NO at 800°C. The Si_3N_4 film was then deposited using SiH_4 and NH_3 at 800 °C, followed by rapid thermal annealing (RTA) in NH_3 and NO_2 at different temperatures. Undoped poly-Si gate was deposited by low temperature CVD. Gate patterning was done with I-line lithography followed by photoresist ashing in O_2 plasma to obtain sub-100nm gate length. Fig. 1 is a Scanning-Electron-Microscope (SEM) picture of an 80 nm gate. Gate etching was performed with HBr:He:O_2 chemistry, which provided good selectivity against silicon nitride. A "reverse-LDD" process [7] was employed to achieve shallow junction depths and minimal source and drain (S/D) extension underlap with the gate. Following gate etch, silicon nitride spacer was formed, and the source and

drain regions were implanted with phosphorus for N-MOSFETs and boron for P-MOSFETs, respectively. Then the spacer was removed, and the source and drain extension regions were implanted. Rapid thermal annealing in N_2 was used for dopant activation. Unfortunately, NMOSFET devices displayed low drive current, possibly because the S/D extensions regions did not underlap the gate. Only PMOSFETs data are presented in this paper.

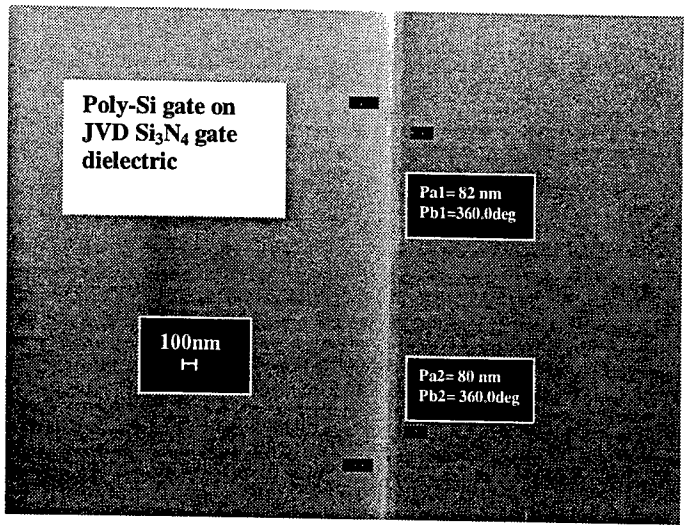
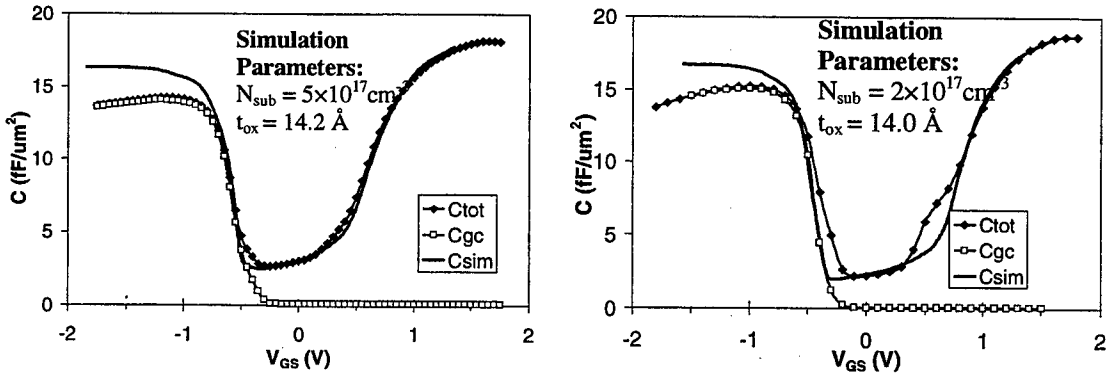


Figure 1. Scanning electron microcope picture of the poly-Si gate on JVD Si_3N_4. The gate length is 80 nm.

III. CHARACTERIZATION AND DISCUSSION OF RESULTS

Fig. 2 shows the C-V characteristics for the JVD and RTCVD nitride films. C_{gc} is the inversion-channel-to-gate capacitance, which should be zero in accumulation region, as shown in the figure. C_{gc} measurement provides an excellent way to zero out the parasitic capacitance introduced by the measurement system, such as the probes and pads. C_{tot} is the commonly measured capacitance between substrate and gate. Also shown with the measured data are simulated C-V curves using a quantum simulator [8]. Simulation results indicate an oxide equivalent thickness of 14.2 Å for the JVD and 14.0 Å for RTCVD nitride films, respectively. As the poly-gate is not *in situ* doped, poly-depletion is obvious on the measured data. The RTCVD films in this study showed more interface traps than the JVD films, while these interface traps do not seem to degrade the subthreshold swing nor I_{DS}, as will be shown later. Fig. 3 shows the gate tunneling current density with both the substrate and the poly-Si gate in accumulation. In the very low voltage range, the higher leakage of RTCVD film could be correlated to the higher trap states density as shown in Fig. 1, and at higher gate voltage, the two films have comparable tunneling current. Both 14 Å JVD and RTCVD nitride films exhibit significantly lower leakage than an equivalent 14 Å of SiO_2 by about 2 orders of magnitude [1]. For example, at V_{GS}=2V, nitride films have a current density of roughly 1A/cm^2, while SiO_2 is expected to have 10^2 A/cm^2. This suggests that silicon nitride is an attractive gate dielectric material for scaling below 15 Å. Fig. 4 shows the subthreshold characteristics of 80 nm gate-length PMOSFETs. Definition V_T as the V_{GS} at which I_{DS}=50nA/μm for V_{DS}= 0.05V, both JVD and RTCVD devices showed V_T=-0.45V. This value is higher than desirable, and can be optimized by V_T adjust implant. The subthreshold swing of long-channel devices is 86 mV/dec for both the JVD and RTCVD films, respectively. The steep subthreshold swing is indicative of acceptable Si-gate dielectric interface quality. The leakage current at V_{DS} = -1.5V and V_{GS} = 0V is due to punchthrough, and can be suppressed with



(a) JVD Si_3N_4 gate dielectric **(b) RTCVD Si_3N_4 gate dielectric**

Figure 2. High-frequency capacitance-voltage characteristics of (a) JVD and (b) RTCVD Si_3N_4.

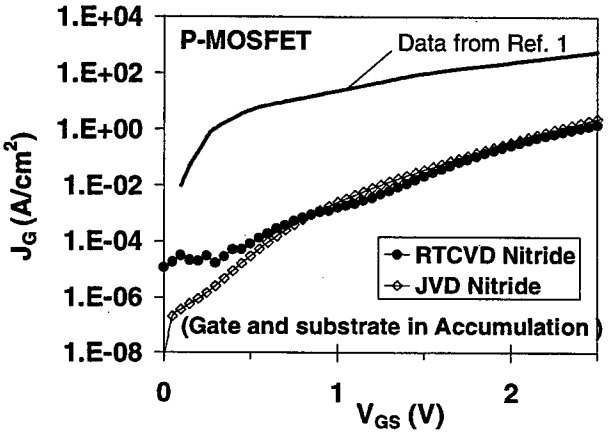
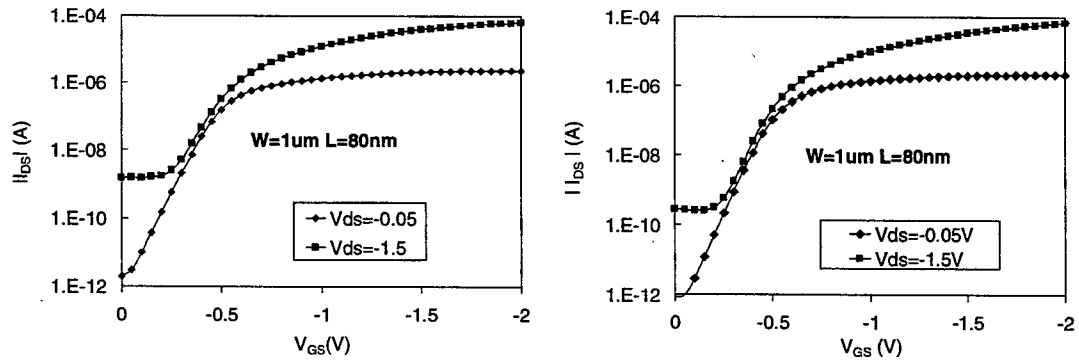
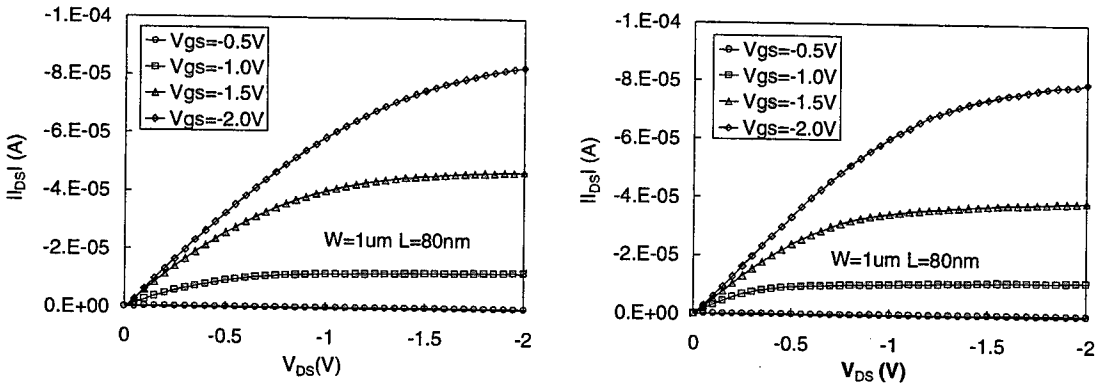


Figure 3. Gate leakage current of JVD Si_3N_4 and RTCVD Si_3N_4 is about 100 times lower than SiO_2, with the same $t_{OX,\,EQ}$=14Å



(a) JVD Si_3N_4 gate dielectric **(b) RTCVD Si_3N_4 gate dielectric**

Figure 4. I_{DS}-V_{GS} characteristics of (a) JVD Si_3N_4 and (b) RTCVD Si_3N_4 MOSFETs.



(a) JVD Si_3N_4 gate dielectric **(b) RTCVD Si_3N_4 gate dielectric**

Figure 5. I_{DS}-V_{DS} characteristics of (a) JVD Si_3N_4 and (b) RTCVD Si_3N_4 MOSFETs.

an optimized well doping profile. The JVD device may have slightly shorter channel length, which gives higher leakage. Fig. 5 shows the I_{DS}-V_{DS} characteristics of the PMOSFETs. Both the JVD and the RTCVD devices have a gate length of 80 nm. Since they have the same V_T, they provide similar drive current, suggesting nearly identical carrier mobility.

IV. CONCLUSIONS

JVD and RTCVD silicon nitride films have been evaluated as gate dielectric material in a side by side experiment using the same CMOS process technology. Both have been found to be suitable as the MOSFET gate dielectric down to at least 14 Å $t_{OX,EQ}$, with gate length scaled to sub-100nm range. Given its compatibility with conventional CMOS processing technology, silicon nitride is a very attractive material as the first post-SiO_2 gate dielectric. The similarity in leakage current, swing and mobility between the two kinds of nitride film is striking. This suggests that nitride stacks of comparable good quality can be fabricated by both technologies, and perhaps by other deposition techniques as well.

ACKNOWLEDGMENTS

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Suggested Area: Simulation and Modeling

Student Paper

New Trap-Assisted Band-to-Band Tunneling(TAB) Induced Gate Current Model for PMOSFET's with Sub-3nm Oxides

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Abstract- A new trap-assisted band-to-band tunneling(**TAB**) gate current model is proposed to describe the new observed BBT induced gate current characteristics of ultra-thin gate oxide PMOSFET's. Based on this new TAB model, the off-state gate currents of PMOSFET's with various sub-3nm gate oxides can be well characterized while the conventional BBT current model is no longer applicable in this regime.

I. Introduction

As CMOS technology scales into deep sub-micron regime for higher density and speed, thinner gate oxide is required to provide sufficient current drive under low supply voltages. However, the large gate leakage current resulting from the scaling of gate oxides significantly affects the device performance. In the past years, mechanisms and models of ultra-thin gate-oxide leakage currents for MOS capacitors, such as TAT, have been comprehensively discussed [1].In this paper, a new leakage current in PMOSFET's with 2.2nm gate oxide is observed, and a new tunneling current model is established.

II. Experiments and Calculations

The PMOSFET's used in this paper are fabricated symmetrically in structure with 0.18μm technology, and the gate oxide thickness is well controlled at around 2.2nm by TEM inspection. With source terminal floating, the off-state gate current illustrated in Fig. 1 can be divided into two regions: V_D-dependent and V_D-independent. Within the V_D-dependent region, the band-to-band tunneling induced gate current dominants. As gate voltage increases, the gate-to-substrate tunneling current raises and finally dominates the gate current under large gate biases. To verify these two mechanisms illustrated in Fig. 2, the gate currents of two PMOSFET's with different channel lengths are compared in Fig. 3. The two gate current curves coincide in the V_D-dependent region, while the gate-to-substrate overlap area varies.

To analyze the band-to-band tunneling (BBT) induced gate currents in the V_D-dependent region, the conventional BBT gate current model is used for theoretical calculation. Although being successful in describing the gate currents for thick-oxide devices, the conventional BBT gate current model fails to describe the off-state gate currents of 2.2nm-thick gate oxide PMOSFET's as illustrated in Fig. 4. Not only the slope of calculated BBT induced gate current does not agree with measured data, the magnitude of experimental data also differs significantly from the theoretical predictions. To accurately describe the BBT induced gate current of ultra-thin gate oxide PMOSFET's, we propose a new trap-assisted BBT gate current model.

III. Trap-Assisted BBT(TAB) Gate Current Model

The band diagrams of the new trap-assisted BBT (TAB) and the conventional BBT gate current models are illustrated in Fig. 5 and Fig. 6. Without gaining enough energy to surmount the 3.1eV-oxide barrier, the BBT induced electrons on the drain side may still tunnel through the gate oxide via oxide traps. Based on the concept of trap-assisted tunneling, the BBT induced gate current of ultra-thin gate oxide PMOSFET's can be modeled with the new TAB gate current model expressed by the followed equation:

$$I_G = I_D \cdot P(V_{OX}, N_T)$$

where I_D is the theoretical drain current calculated by the conventional BBT model, and $P(V_{OX},N_T)$ is the trap-assisted direct tunneling probability of the conduction band electrons on the drain side. Since $P(V_{OX},N_T)$ is proportional to the "visible" oxide trap density for the BBT induced conduction band electrons under various oxide drop voltages, the trap-assisted direct tunneling probability can be rewritten as:

$$P(V_{OX},N_T) = C \cdot N_{T,MAX} \cdot D(V_{OX}) \cdot \exp\left(\frac{-K(\varphi^{1.5} - (\varphi - V_{OX})^{1.5}) \cdot T_{OX}}{2 \cdot V_{OX}}\right)$$

where C is a fitting parameter determined by probability normalization and device geometry, $N_{T,MAX}$ is the maximum "visible" oxide trap density; $D(V_{OX})$ is the normalized V_{OX}-dependent trap distribution function, and the exponential term is a characteristic function of trap-assisted direct tunneling. To calculate the trap-assisted BBT induced gate current of the 2.2nm gate oxide furnace-PMOSFET, I_D is calculated by the conventional BBT model, $N_{T,MAX}$ of $2\times10^{12}/cm^2$ is extracted from the N-well MOSC I-V curve measured under accumulation. φ is 3.1eV-oxide barrier for BBT induced electrons on the drain side, and the oxide voltage drop is obtained by solving the Poisson's equation under different bias conditions. To obtain the normalized trap distribution function $D(V_{OX})$, the fitting parameter C is set to be 9×10^{-5} to match the experimental data when $D(V_{OX})$ is set to be 1, as illustrated in Fig. 7. After dividing the measured gate currents with calculated data, the normalized trap distribution functions are obtained and compared in Fig. 8.The V_{OX}-dependent-only $D(V_{OX})$ can be expressed as:

$$D(V_{OX}) \sim 10^{(15-50 \cdot Vox + 30 \cdot Vox^2)}$$

Reassemble all parameters in the TAB gate current model, the BBT induced gate currents of furnace-fabricated 2.2nm gate oxide PMOSFET's can be well modeled, as shown in Fig. 9. Without modifying any parameter except the extracted $N_{T,MAX}$ value, the TAB model agrees very well with measured data of RTO(rapid thermal oxidation)- and ISSG(In-situ steam gas)-PMOSFET's shown in Fig. 10 and Fig. 11, respectively. By combining the theoretical TAB gate current calculation with the non-BBT experimental data, the complete gate current curves under various drain biases are perfectly demonstrated in Fig. 12. These figures demonstrate agreement between the model and experimental data; they also show the improved accuracy of this new TAB gate current model for 2.2nm gate oxide PMOSFET's fabricated with various process techniques.

IV. Conclusion

A new TAB gate current model is proposed to characterize the BBT induced gate currents in sub-3nm PMOSFET's. With this simple and practical model, the off-state gate current characteristics can be accurately described.

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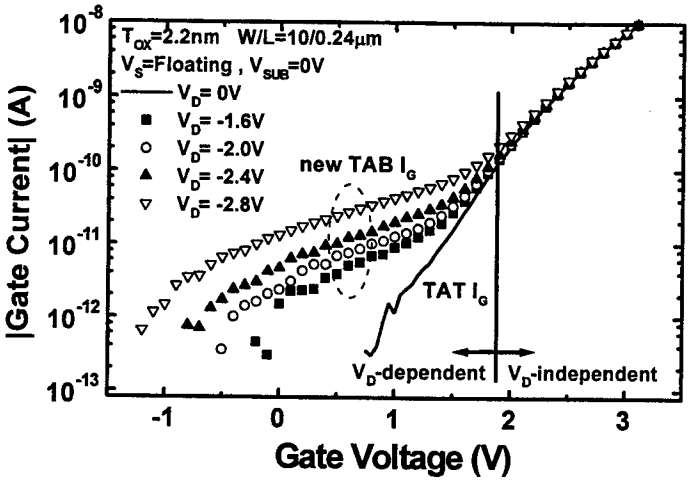


Fig. 1 The off-state gate current of 2.2nm gate oxide PMOSFET can be divided into two regions: V_D-dependent and V_D-independent.

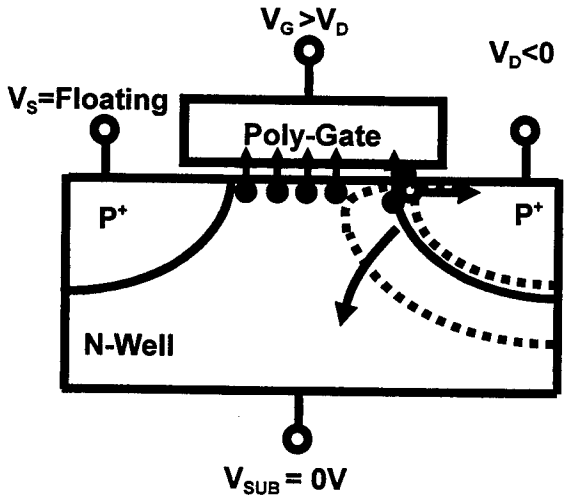


Fig. 2 The off-state gate current consists of BBT induced gate current and gate-to-substrate tunneling current.

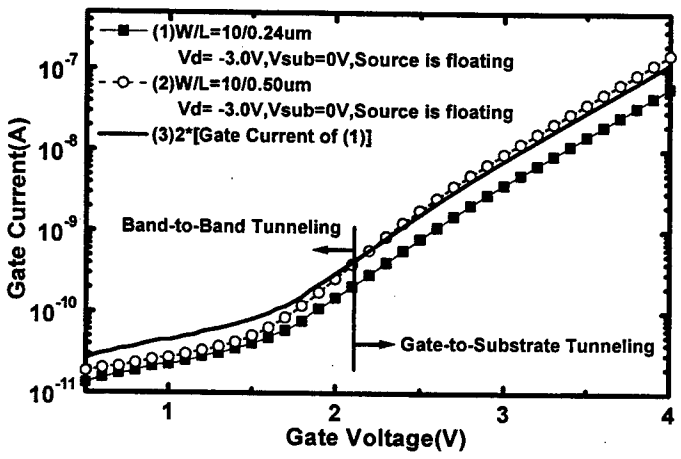


Fig. 3 The gate current curves of two different PMOSFET's merge in the BBT-induced-gate-current-dominant region, while the gate-to-substrate overlap area varies.

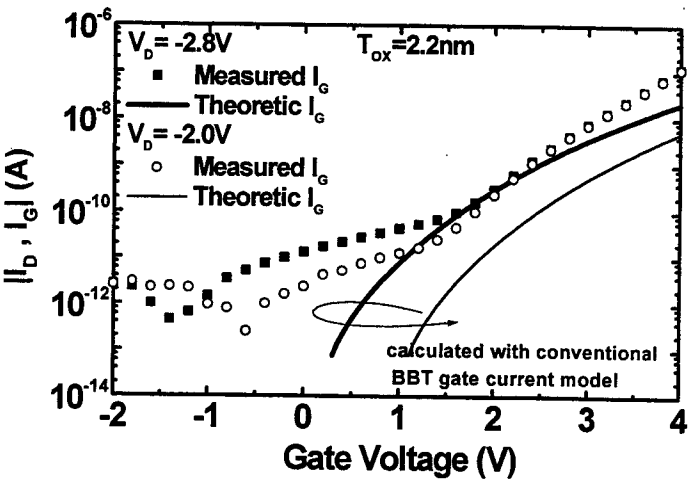


Fig. 4 The conventional BBT gate current model fails to accurately predict the slope and magnitude of BBT induced gate current in 2.2nm oxide PMOSFET.

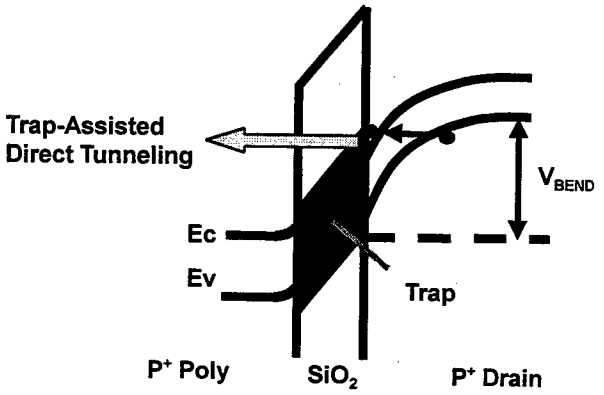


Fig. 5 In the TAB gate current model, electrons may tunnel through the gate oxide via traps without gaining enough energy to surmount the oxide barrier.

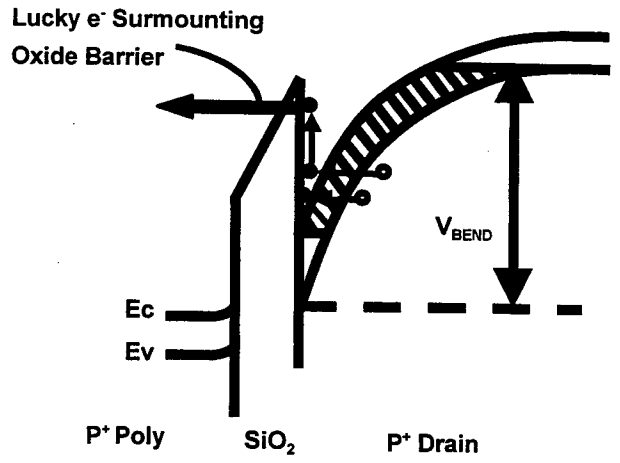


Fig. 6 In the conventional BBT gate current model, only the electrons with enough energy to surmount the 3.1eV oxide barrier can be injected into the gate terminal.

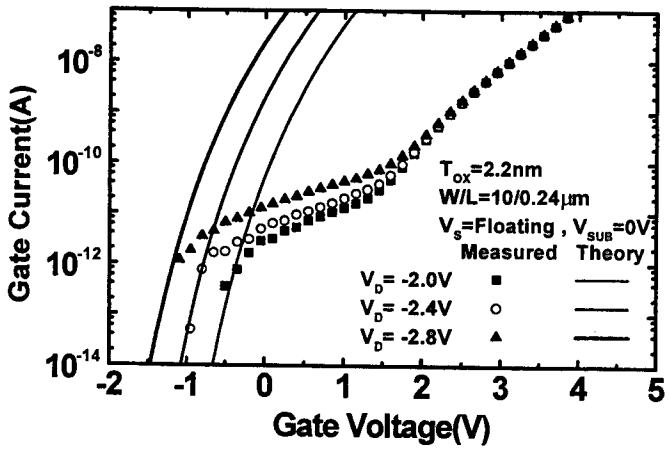


Fig. 7 In order to obtain the normalized trap distribution $D(V_{OX})$, the theoretical data are fitted with minimal experimental data where $D(V_{OX})$ at these intersections is set to be 1.

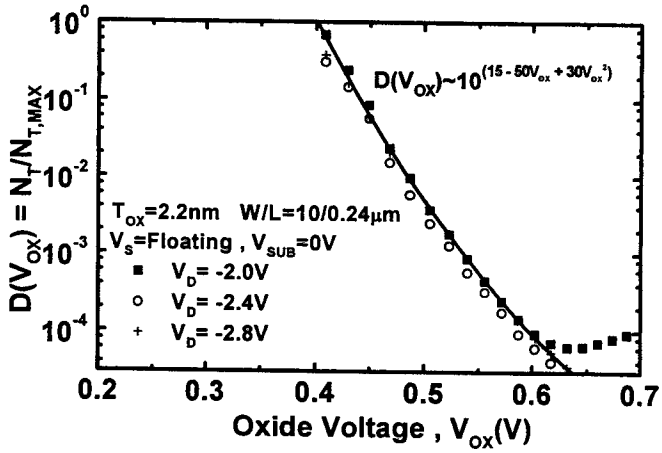


Fig. 8 After dividing the measured gate currents with calculated data illustrated in Fig. 7, the normalized trap distribution function is obtained.

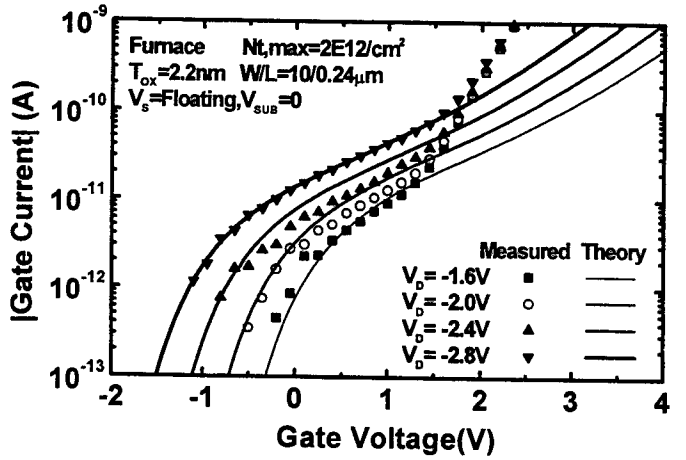


Fig. 9 Reassemble all parameters in the TAB gate current model, the BBT induced gate currents of furnace-fabricated 2.2nm gate oxide PMOSFET's can be well described.

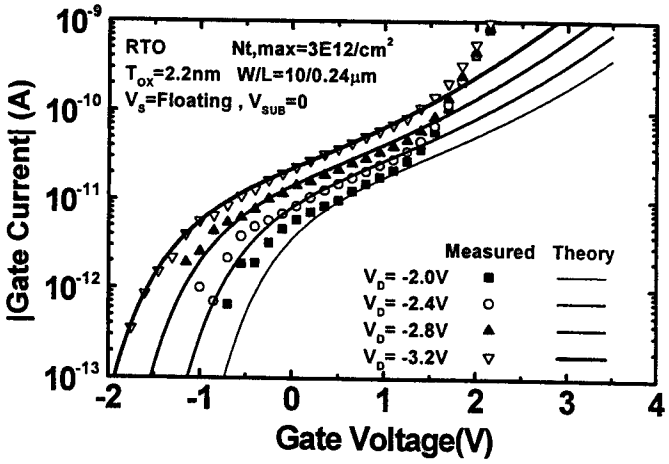


Fig. 10 The BBT induced gate currents of RTO-PMOSFET are accurately characterized by using the $N_{T,MAX}$ extracted from the RTO-PMOSC I-V curve measured under accumulation.

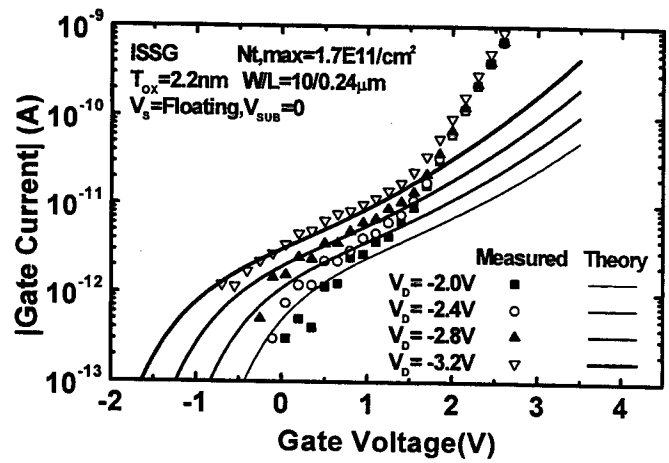


Fig. 11 Using the $N_{T,MAX}$ extracted from ISSG-PMOSC I-V curves, the BBT induced gate currents of ISSG-PMOSFET's are accurately explained with the new TAB gate current model.

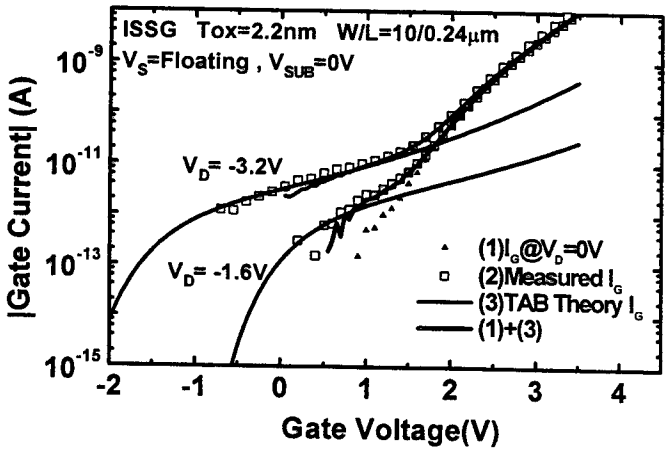


Fig. 12 After combining the gate current calculation with non-BBT experimental data, the complete gate current curves are established.

De-Embedding Procedure for RF Equivalent Circuits of MOSFETs

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ABSTRACT

An improved de-embedding procedure for extraction of parasitic elements of metal oxide semiconductor field effect transistors (MOSFETs) is proposed. This extraction enables to determine the intrinsic elements of the small-signal equivalent circuit. As a result a new method to calculate the oxide capacitance is presented. This de-embedding procedure is based on an analytic solution of the equations and facilitates the determination of the elements at any specific frequency.

I. INTRODUCTION

Decreasing channel length and consequently increasing transit frequency allows for the use of MOSFETs in mobile communication products. For circuit development precise small-signal equivalent circuits of the devices are needed. Especially the resistive substrate losses of RF MOSFETs require to distinguish between interconnection network and device. Therefore de-embedding procedures are necessary to separate intrinsic transistor elements and parasitic elements to obtain a valid transistor model for circuit simulation.

II. COLD MODELING

Figure 1 shows the small-signal equivalent circuit of the MOSFET used for the de-embedding procedure [1]. The intrinsic transistor is embedded by series resistors R_g, R_d and R_s and series inductors L_g, L_d and L_s representing the interconnection lines. In addition, the parasitics of the pad due to substrate losses are modeled by the capacitances C_{pg} and C_{pd} in series with the resistors R_{pg} and R_{pd}. The objective of our method is to separate these elements from the intrinsic device.

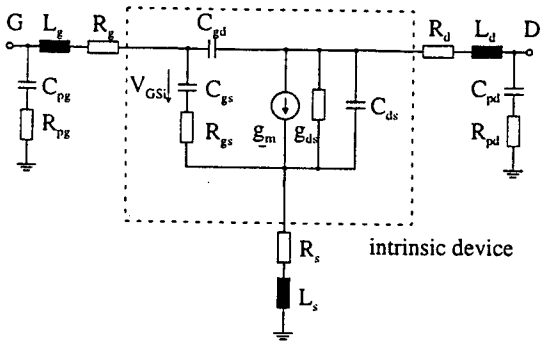


Fig. 1. Small-signal equivalent circuit of a MOSFET.

First of all, the four elements, which are characterizing the pads (C_{pg}, C_{pd}, R_{pg} and R_{pd}), are derived from a measurement of a test structure with the same metalization as the real structure but without connected transistor (open-structure) [2]. In the following, the gate- and drain-pad are represented by $\underline{Y}_{pg}$ and $\underline{Y}_{pd}$. Figure 2 shows the equivalent circuit, which is valid for a gate voltage above pinch-off and at zero drain voltage. The intrinsic device is modeled through a distributed channel resistance R_c' and a distributed oxide capacitance C_{ox}'.

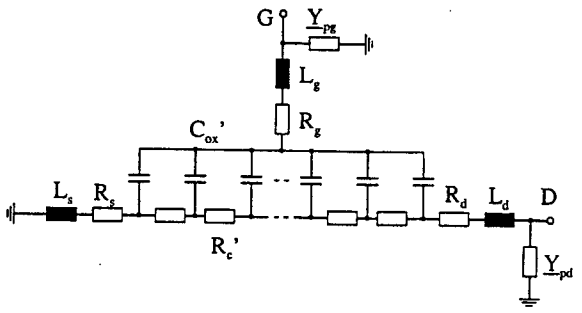


Fig. 2. Equivalent circuit of the MOSFET device for zero drain voltage and gate voltage above pinch-off.

The device is measured at different gate voltages with zero drain voltage. This allows to determine the channel resistance R_c from the real part of the $\underline{Z}_{22}$-parameter by extrapolating the sum of R_d and R_s at large gate voltages according to the following equation [3].

$$\mathrm{Re}\{\underline{Z}_{22}\} = R_d + R_s + R_c = R_d + R_s + \frac{1}{\beta\,(V_{GS} - V_{TH})} \qquad (1)$$

For the derivation of the still missing elements knowledge of the oxide capacitance C_{ox} is necessary. Figure 3 shows the valid small-signal equivalent circuit for a gate voltage below pinch-off and at zero drain voltage. In this case the transistor can be modeled by capacitances only. The circuit consists of the pads with $\underline{Y}_{pg}$ and $\underline{Y}_{pd}$, a divided oxide capacitance between source and drain, an overlap capacitance between gate and drain (which can be neglected depending on the technology used) and a channel capacitance between source and drain.

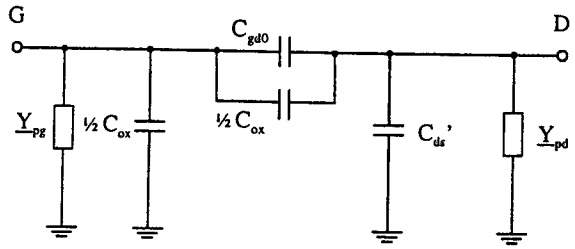


Fig. 3. Equivalent circuit of the MOSFET device for zero drain voltage and gate voltage below pinch-off.

The oxide capacitance can be derived from the $\underline{Y}$-parameters of the small-signal equivalent circuit of Figure 3.

$$C_{ox} = \frac{2\left(\mathrm{Im}\{\underline{Y}_{11coldC}\} + \mathrm{Im}\{\underline{Y}_{12coldC}\} - \mathrm{Im}\{\underline{Y}_{pg}\}\right)}{\omega} \quad (2)$$

With the knowledge of the oxide capacitance, of the channel resistance and the complete set of $\underline{Z}$-parameters for the equivalent circuit of Figure 2 the remaining parasitic elements R_g, R_s, R_d, L_g, L_s and L_d can be derived.

$$\underline{Z}_{11} = R_g + R_s + \frac{R_c}{3} + j\left[\omega(L_g + L_s) - \frac{1}{\omega C_{ox}}\right] \quad (3)$$

$$\underline{Z}_{12} = \underline{Z}_{21} = R_s + \frac{R_c}{2} + j\omega L_s \quad (4)$$

$$\underline{Z}_{22} = R_d + R_s + R_c + j\omega[L_d + L_s] \quad (5)$$

The de-embedding matrix for the series elements used in Figure 1 is formulated in the following equation [4].

$$[\underline{Z}_s] = \begin{bmatrix} \underline{Z}_{11} - \frac{R_c}{3} + j\frac{1}{\omega C_{ox}} & \underline{Z}_{12} - \frac{R_c}{2} \\ \underline{Z}_{21} - \frac{Rc}{2} & \underline{Z}_{22} - R_c \end{bmatrix} \quad (6)$$

$\underline{Y}_i$ represent the $\underline{Y}$-parameters of the intrinsic device, which are calculated via matrix operation, where $\underline{Y}_a$ are the $\underline{Y}$-parameters of the measured device at the reference plane.

$$[\underline{Y}_i] = \left[\left([\underline{Y}_a] - [\underline{Y}_{pad}]\right)^{-1} - [\underline{Z}_s]\right]^{-1} \quad (7)$$

III. HOT MODELING

Figure 4 shows the small-signal equivalent circuit of the intrinsic device with all parasitic elements subtracted.

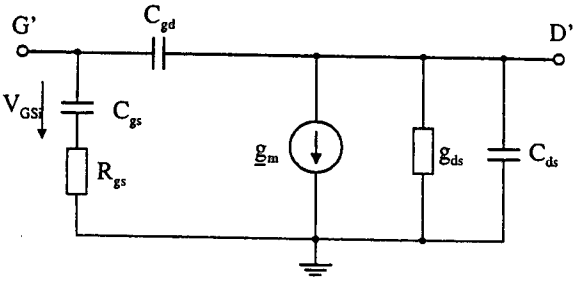


Fig. 4. High-frequency equivalent circuit of the intrinsic device.

The so called "hot-modeling" allows the calculation of the elements by the $\underline{Y}$-parameters of the equivalent circuit.

$$\underline{Y}_{11} = \frac{R_{gs}C_{gs}^2\omega^2}{1+\omega^2C_{gs}^2R_{gs}^2} + j\omega\left[\frac{C_{gs}}{1+\omega^2C_{gs}^2R_{gs}^2} + C_{gd}\right] \quad (8)$$

$$\underline{Y}_{12} = -j\omega C_{gd} \quad (9)$$

$$\underline{Y}_{21} = \frac{g_m e^{-j\omega\tau}}{1+j\omega R_{gs}C_{gs}} - j\omega C_{gd} \quad (10)$$

$$\underline{Y}_{22} = g_{ds} + j\omega(C_{ds} + C_{gd}) \quad (11)$$

IV. MEASUREMENT RESULTS

For the verification of the presented de-embedding procedure measurements were performed with a standard 0.35 µm CMOS process from the JESSI project. The measurements were investigated with a microwave probing system in the frequency range of 50 MHz to 20 GHz. The method requires measurement results of an open-structure and of an active device at different operating points for hot and cold modeling. Figure 5 shows the comparison between measurement and simulation of the input and output reflection ($\underline{S}_{11}$ and $\underline{S}_{22}$) of the open-structure (measurement: crossed, simulation: circled). The simulation was performed with the extracted elements C_{pg}, C_{pd}, R_{pg} and R_{pd}. The good agreement validates the equivalent circuit chosen for the pads in Figure 1. The root-mean-square deviation is 0.9 % for $\underline{S}_{11}$ and 0.8 % for $\underline{S}_{22}$.

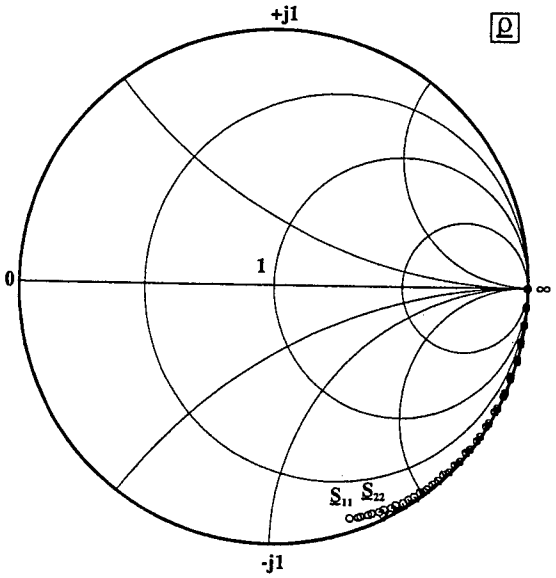


Fig. 5. Comparison between measurement and simulation of the open-structure (measurement: crossed, simulation: circled).

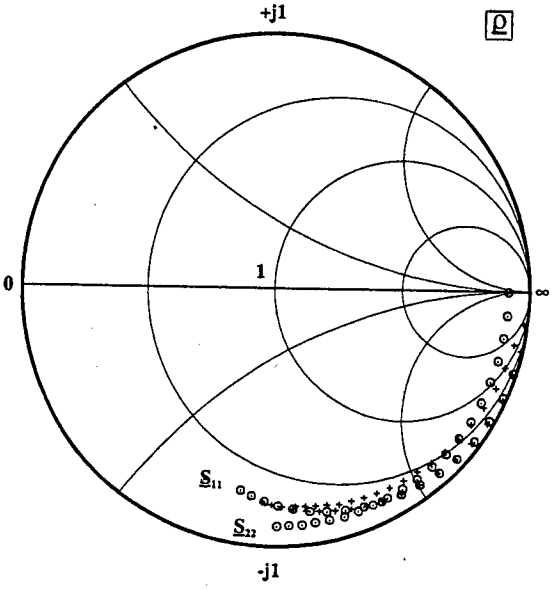


Fig. 7. Input and output reflection factors $\underline{S}_{11}$ and $\underline{S}_{22}$ of the intrinsic device (measurement: crossed, simulation: circled).

The next figure shows the determination of the channel resistor. According to equation (1) the channel resistor can be derived from the real part of the $\underline{Z}_{22}$-parameter from Figure 2. The points in Figure 6 are the measured values at different gate voltages and the line is the extrapolation, which allows the determination of the sum of R_d and R_s and thereby the calculation of the channel resistor R_c.

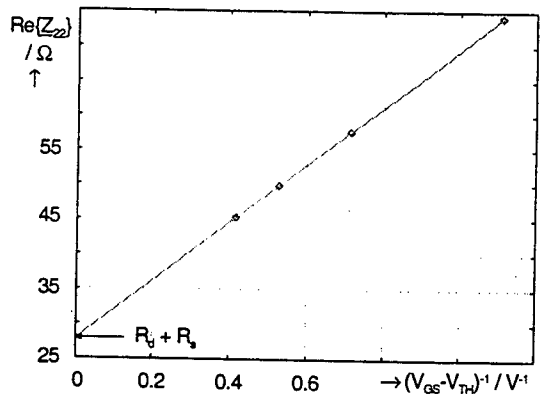


Fig. 6. Determination of the channel resistor R_c.

The good agreement of measurement and interpolation justifies the equivalent circuit for zero drain voltage and gate voltage above pinch-off (Figure 2). Figure 7 shows input and output reflection ($\underline{S}_{11}$ and $\underline{S}_{22}$) of the intrinsic, de-embedded device at saturation. Measured values are depicted as crosses and simulation results as circles.

$\underline{S}_{11}$ and $\underline{S}_{22}$ show good agreement with small deviations for high frequencies. In this case the root-mean-square deviation is 3.2 % for $\underline{S}_{11}$ and 5.2 % for $\underline{S}_{22}$. Figure 8 shows the transmission factors (forward and reverse) $\underline{S}_{21}$ and $\underline{S}_{12}$ of the intrinsic transistor in a polar plot.

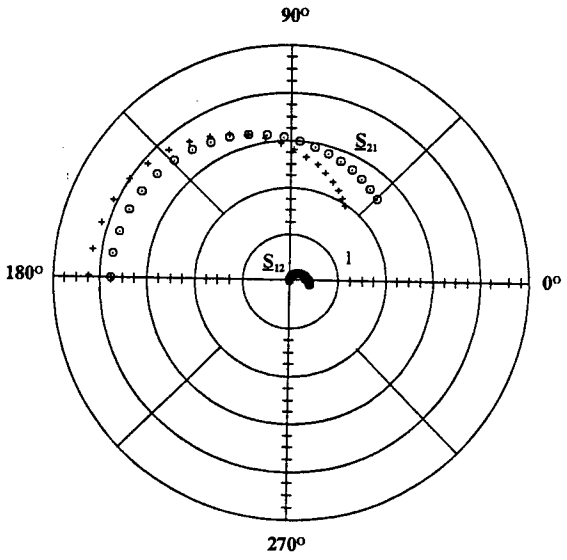


Fig. 8. Forward and reverse transmission factors $\underline{S}_{21}$ and $\underline{S}_{12}$ of the intrinsic device in saturation (measurement: crossed, simulation: circled).

Small deviations occur for $\underline{S}_{21}$ and $\underline{S}_{12}$ with a root-mean-square deviation of 11.3 % for $\underline{S}_{21}$ and 11.0 % for $\underline{S}_{12}$. To verify the validity of the equivalent circuits used at every step of the de-embedding procedure the frequency dependence of the elements has to be checked [5]. If there is a strong frequency dependence in a special frequency range, the equivalent circuit is not valid. As the de-embedding procedure is frequency-independent, the element values can be calculated at every frequency point. To illustrate this, the next two plots show the frequency dependence of three elements of the intrinsic device. Figure 9 shows the dependence from the norm of the transconductance $|g_m|$ in the frequency range of 0–20 GHz.

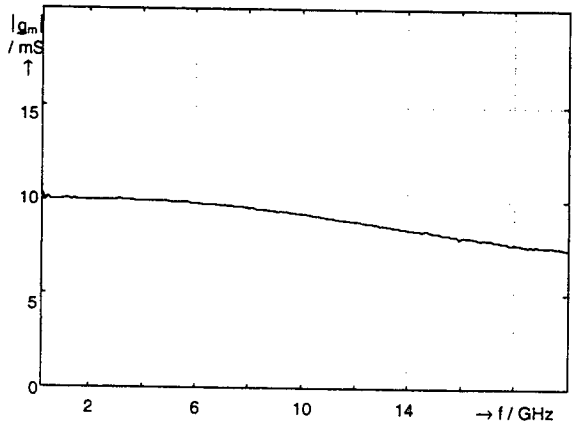


Fig. 9. Norm of the transconductance $|g_m|$ versus the frequency.

As an example figure 10 shows two capacitances C_{gs} and C_{gd} in the same frequency range.

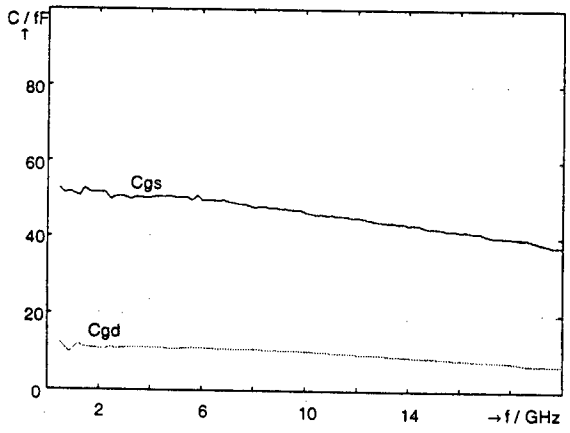


Fig. 10. Intrinsic capacitances C_{gs} and C_{gd} versus the frequency.

The extracted values of the intrinsic elements Cgd, Cgs (Figure 9) and $|g_m|$ (Figure 10) show nearly no frequency dependence up to 10 GHz. A slight decrease of the element values appears for higher frequencies.

V. CONCLUSION

A new de-embedding procedure for the derivation of RF equivalent circuits was described. As a result a new method for the calculation of the oxide capacitance was presented. With the use of an open test structure and measurements at different bias conditions an analytic derivation of all parasitic elements is possible. The analytic solution allows the determination of the element values at any specific frequency. The validity of the small-signal equivalent circuits used for the procedure can be checked by examining the frequency-dependence of the derived elements. This method allows quick derivation of the intrinsic small-signal equivalent circuit for circuit development.

ACKNOWLEDGEMENT

The author would like to thank Mr. Gerhardt and Mr. Sailer from the ALCATEL company who provided us with a test wafer from the JESSI project.

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Device Characterization of Body Bias Effect on Analog Characteristics with sub-0.2 μm PD-SOI for Analog and RF Applications

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ABSTRACT

In this paper, interaction of the body bias effect, device size and the analog characteristics such as DC gain, matching effect, and speed (f_T) of sub-0.2 μm PD-SOI technology is reported. From these results, the optimized device size and the body bias for the analog and RF application can be determined according to the their specific demand.

INTRODUCTION

Especially, design engineer of SOI circuit have more elaborate than that of bulk silicon, the following reason; SOI has the structural disadvantage such as floating body effect and kink effect etc.. Although, much work has been done on both analog [1] and digital [2], [3] performance of SOI, the effects of body bias and matching, I_{on}/I_{off} ratio, and ac characteristics on the analog performance of PD-SOI has not been extensively in the literature. In this paper, interaction of the body bias effect, device size and the analog characteristics such as DC gain, matching effect, and speed (f_T) of sub-0.2 μm PD-SOI technology is reported. Some consequences of the effect on the characterization of the device size for the mixed mode circuit and RF applications will be discussed.

DEVICE FABRICATION

The starting 8" SIMOX wafer has the silicon film thickness of 100 nm and buried oxide thickness of 100 nm. Device are integrated into sub-0.2 μm dual poly (n+/p+) gate PD-SOI process with 3.8 nm-gate oxide, shallow trench isolation (STI) process for isolation among devices, boron and arsenic implantation for LDD and source/drain (S/D), with a 1000 °C, 25 sec rapid thermal anneal (RTA) to be used for both NMOSFET's and PMOSFET's, and salicide process for reducing gate and S/D sheet resistance. The threshold voltage adjust ion implant dose were such that they resulted in V_{TH} = 0.35 V for NMOSFET's and – 0.4 V for PMOSFET's. Brief process steps for SOI device fabrication is shown in Table-1.

DEVICE CHARACTERISTICS

In this section, some important device characteristics related with body bias and device size will be presented.

A. DC Characteristics

In Fig. 1, the slopes of $\Delta V_{TH}/\Delta L_g$ vs. channel length are compared for various V_B conditions (– 0.5-, 0-, + 0.25-, + 0.5-V and floating body). Because of decreased charge sharing effect due to narrowed depletion region, short channel effect is improved with increasing V_B. For example, L_g with V_B of + 0.5 V has a margin of about 0.05 μm over that with V_B of – 0.25 V. Fig. 2 and Fig. 3 show output resistance (R_{OUT}) and gain vs. V_{GS}–V_{TH} for various V_B's, where better characteristics can be found as V_B increases to positive bias, which concords with the result of Babcock et al. [1]. R_{OUT} and gain increase slightly as V_{GS}–V_{TH} increases due to increase of the Early voltage [1]. The above experimental results can be summarized in Fig. 4 for use in determining the device size and V_B condition, where a gain variation due to V_B variation vs. V_{TH} slope indicating the short channel effect is plotted for various values of L_g's at fixed V_{GS}–V_{TH}. To be noticed is a contour of fixed V_B for different L_g. It can be seen that gain saturates for L_g longer than 0.7 μm, then decreases slightly from L_g of 5 μm. The gain decrease for $L_g > 5$ μm is due to the fact that the effect of g_m decrease is larger than that of R_{OUT} increase. From the above results, it is recommended to bias V_B positively to make high-density circuits with smaller L_g.

B. Matching Effect

The matching effects [2], [3], [4], [5], which is an important design parameter in precision analog circuits applications such as data converter and switched-

capacitor filter is investigated. Fig. 5 shows the relation of standard deviation with the inverse square root of the channel area (W x L) for variations of V_{TH} values (– 0.25-, 0-, + 0.25- and + 0.5-V). σ_{VTH} decreases as the body potential increases from negative to positive bias due to the depletion layer width reduction (Table-2 (1), (2)). Hence, the positive V_B of the NMOSFET's would lead to the observed lower value for matching coefficient A_{VT} (Fig. 5(b)). The calculated SD (in this work) does not consider the effective area (W_{eff} x L_{eff}) due to higher channel doping concentration (narrow depletion width) and STI process to be adopted (to skip V_{TH} I/I for parasitic MOSFET's) but the calculated SD of V_{TH} (lines) shows good agreement with the measurement SD of V_{TH} (symbols). In order to see the change of site variation of V_{TH} according to V_B condition, the correlation of V_{TH} at V_B = 0 V vs. V_B = – 0.25 and + 0.25 V with various L_g (0.2-, 0.25- and 0.7-μm) are shown in Fig. 6 (a), (b) and (c). V_{TH} has smaller site variation (smaller slope) in the case of positive V_B due to improvement of the short channel effect as the depletion width decreases in positive V_B [7]. It is shown, for the first time, that the matching effect and V_{TH} site variation effect are improved for positive V_B than those under other V_B conditions (0 V, and negative bias condition).

C. Speed Characteristics

Degradation of analog performance due to the floating body effect is one of the disadvantages of SOI. In order to investigate this effect, the body of SOI MOSFET was considered a JFET structure (Fig. 10, Table-2 (3), (4)). The relation of the width of MOSFET's and the frequency characteristics of JFET are obtained as shown (Fig. 8). While constraint of the gate sheet resistance determines the width of finger (W_{finger}) in the case of bulk RF MOSFET's, the body stability does in case of SOI MOSFET's. RF applications with bulk MOSFET's operate with almost no problem if the width is less than 5 μm (0.25 μm technology) [11], [12] but SOI has the stable body potential up to 25 GHz only if the W_{finger} less than 0.7 μm (in this work). The f_T increases as the number of finger decreases (Fig. 7 and Fig. 9) as explained above.

D. I_{on}/I_{off} Ratio

MOSFET's operate in the saturation region in analog circuits so that I_{off} leakage constraint is not severe as the case in the digital circuits. However, I_{off} should be analyzed for use in mixed mode circuits and system-on-a-chip (SOC) applications. Fig. 11(a) shows the I_{on}/I_{off} ratio [8], [9] as a function of L_g. From – 0.25 V to + 0.25 V for V_B, the ratio is larger than 10,000 [10] regardless of L_g, which is a required number to guarantee the limit of standby power. It increases with the decrease in L_g but saturates after 0.7 μm as shown in Fig. 4. I_{on}/I_{off} ratio is re-plotted as a function of V_B as a design guideline to determine the device size and the body bias in Fig. 11(b).

CHARACTERIZATION PROCEDURE

Determination of a window for device sizes and body bias condition can be made with the previous device characterization if the specific application is given. In this work, three sets have been considered; device characteristics related with DC analog characteristics, matching effect and speed characteristics. Once the data base are prepared, the SOI device size and body bias are readily found. The sequence to establish the window is presented in Table-3. For example, the device window for the accurate analog circuit such as data converter can be determined from the matching characteristics (Fig. 5 and Fig. 6). Fig. 1 to Fig. 4 can be used for the circuits of large gain such as the current source.

CONCLUSIONS

A method for the determining the channel length and body bias of SOI MOSFET's according to the their specific demand such as precision, large gain, and RF application is proposed. It has been shown from various measurements that the positively biased body voltage could improve the circuit performance. Especially, the method to design the analog and RF application with the consideration of body bias effect has been proposed.

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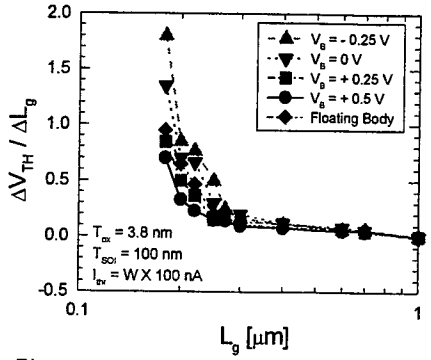


Fig. 1. V_{TH} slope ($\Delta V_{TH} / \Delta L_g$) vs.$L_g$ characteristics at various body bias.

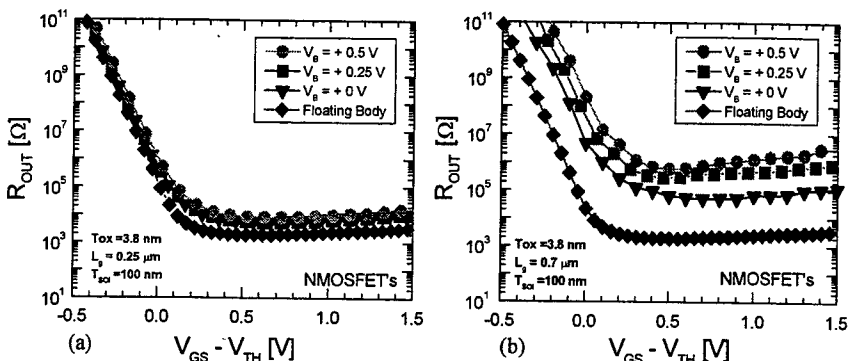


Fig. 2. Comparison of output resistance for (a) 0.25 μm of L_g and (b) 0.7 μm of L_g at various body bias such as floating body, 0 V and positive bias (+ 0.25, + 0.5 V).

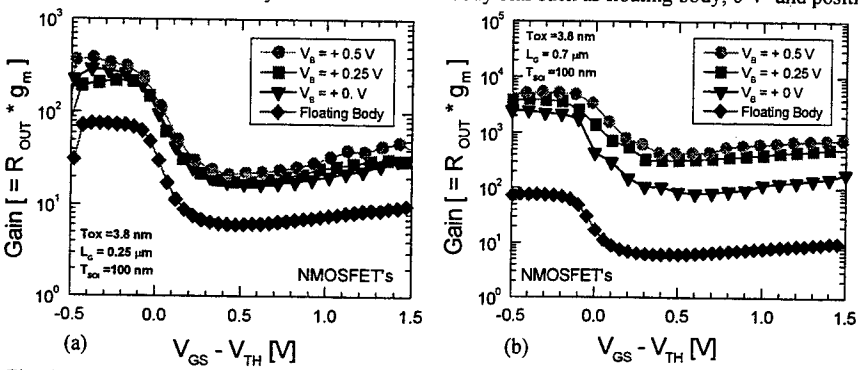


Fig. 3. Comparison of DC gain for (a) 0.25 μm of L_g and (b) 0.7 μm of L_g at various body bias such as floating body, 0 V and positive bias (+ 0.25, +0.5 V).

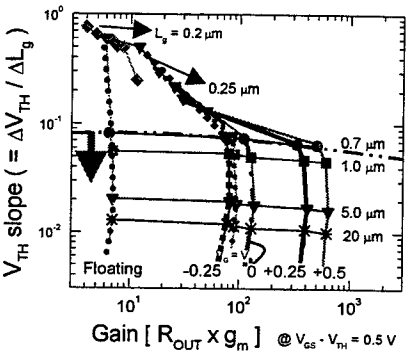
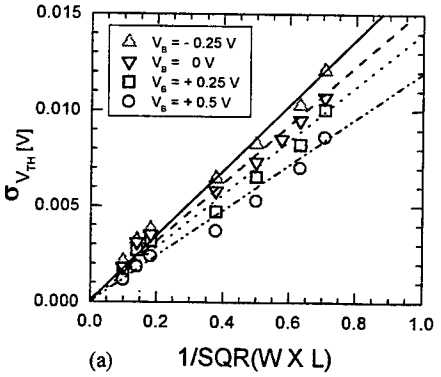
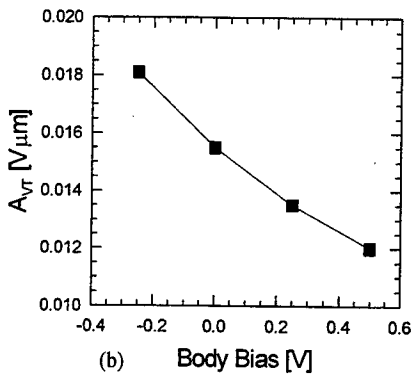


Fig. 4. DC gain (at a fixed gate voltage) vs. V_{TH} slope





1/√WL	W/L
0.1	10/10
0.141	10/5
0.183	10/3
0.37796	10/0.7
0.5	10/0.4
0.63246	10/0.25
0.70711	10/0.2
0.745	10/0.18
4.714	0.25/0.18
4	0.25/0.25
2	1.0/0.25
1.414	1.0/0.5
0.577	1.0/3.0
1.054	5/0.18

(c)

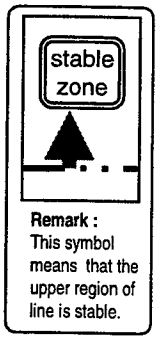


Fig. 5. (a) $\sigma_{V_{TH}}$ of NMOSFET's vs. the inverse square root of the area, for sub-0.2 μm (T_{OX} = 3.8 nm) technology. (b) Matching coefficient A_{VT} for PD-SOI NMOSFET's in various body bias. The coefficient are calculated from Table-2 (1), (2) [2], [5]. (c) Table of the measured NMOSFET's

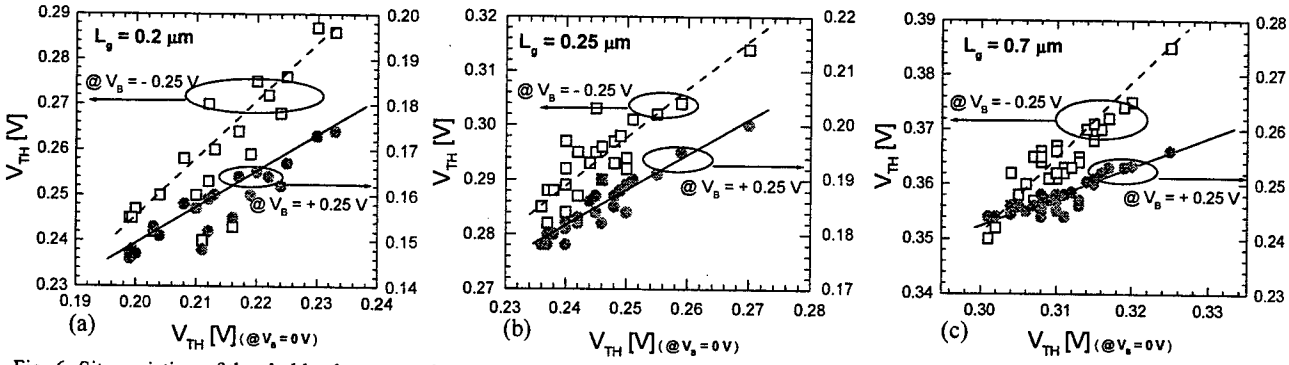


Fig. 6. Site variation of threshold voltage at various channel length and body bias (V_B = - 0.25 V, + 0.25 V) where (a) L_g = 0.2 μm, (b) L_g = 0.25 μm, and (c) L_g= 0.7 μm. Correlation of threshold voltage increases as gate length and body bias(+) increase.

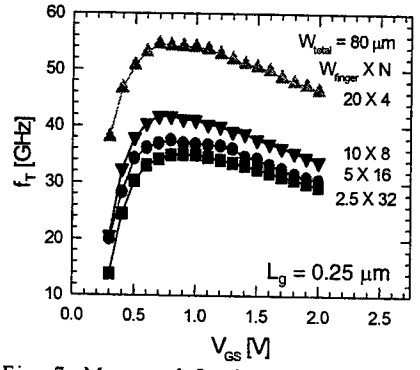


Fig. 7. Measured f_T characteristics of NMOSFET's vs. Gate voltage.

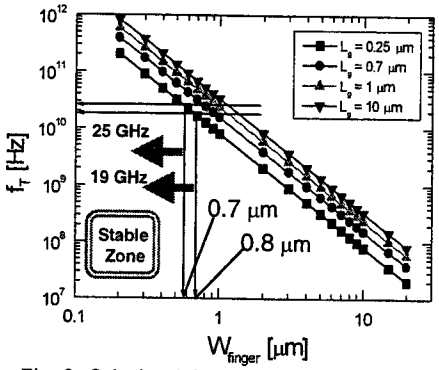


Fig. 8. Calculated f_T characteristics of JFET in SOI vs. W_{finger} (using (3&4) in Table-2).

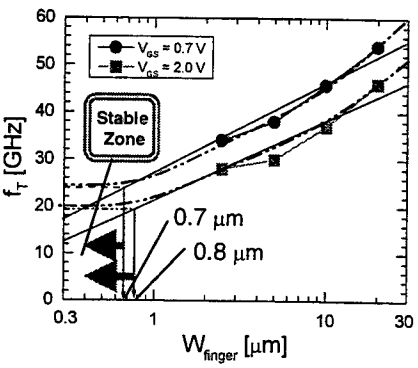


Fig. 9. Measured f_T characteristics of NMOSFET's vs. W_{finger} (from Fig. 7).

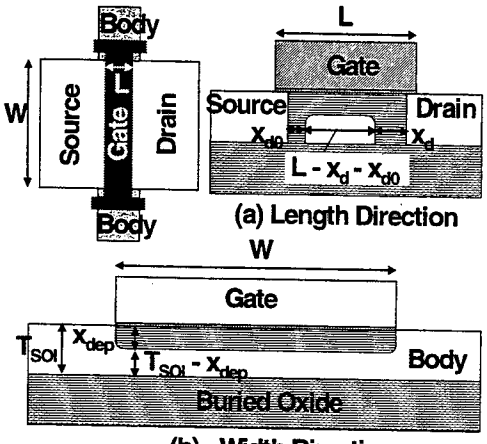


Fig. 10. Body to be considered a JFET structure in PD-SOI structure

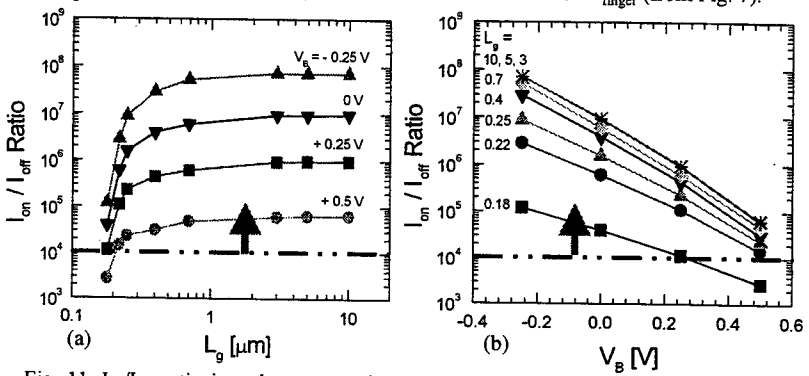


Fig. 11. I_{on}/I_{off} ratio in order to guess the power dissipation in the circuits (a) variation of the ratio by channel length and (b) body bias [10].

TABLE-1. BRIEF PROCESS FOR PD-SOI DEVICE

- P (100) SIMOX 8 inch Wafer T_{SOI} = 100 nm T_{BOX} = 100 nm
- Shallow Trench Isolation
- V_{TH} adjust channel I/I (V_{THN} = 0.35 V, V_{THP} = - 0.35 V
- Gate Oxidation (T_{OX} = 3.8 nm)
- Poly Si Deposition N+/P+ I/I on dual Poly Si Gate for Surface Channel MOSFET's
- Gate Reoxidation
- LDD I/I
- Oxide S/W Formation
- S/D I/I
- RTA 1000 °C, 30 sec
- Salicidation
- ILD + CMP
- Metalization

TABLE-2. COLLECTION OF EQUATIONS FOR CALULATION AND MODELING

Matching Effect

$$\sigma_{V_{TH}} = \frac{A_{VT}}{(W \times L)^2} \quad (1)$$

$$A_{VT} \propto \sqrt{2N_a x_{dep}}$$

$$\sigma^2_{VTH} = \sigma^2_{Q_B}/C^2 + q^2 \sigma^2_{D_i}/C^2 \quad (2)$$

$\sigma^2_{D_i} = D_i/(W * L)$

$\sigma^2_{Q_B} = Q_B^2/(4(L-x_{d0}-x_d)*x_{dep}*N_a)$

D_i : channel doping implant dose

Q_B : depletion charge density

This description is based on the assumptions that mismatch is caused by independent random disturbance of physical properties and that the correlation distance of the statistical disturbance is small compared to the active area [3],[4],[5].

Derived equation of body current from JFET in SOI MOSFET

$$I_B = q\mu_p N_a (T_{SOI} - x_{dep}) \frac{L - x_d - x_{d0}}{W} \quad (3)$$

$$* \left[V_B - \frac{3}{2} \left\{ \frac{2\varepsilon_{si}}{qN_a (T_{SOI} - x_{dep})^2} \right\}^{1/2} \{(\phi_i - V_D - V_B)^{2/3} - (\phi_i - V_D)^{2/3}\} \right]$$

V_B : body potential, V_D : drain bias, ϕ_i :built in potential

Cut-off frequency of JFET in SOI MOSFET

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gb} + C_{db} + C_{sb}} \quad (4)$$

C_{gb} : cap, of inversion layer to body

C_{db} : cap, of drain to body

C_{sb} : cap, of source to body

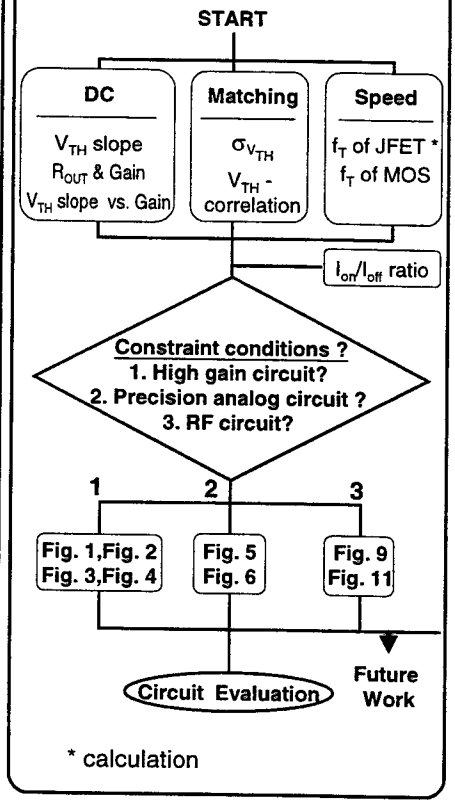
N_a : doping concentration

x_d : depletion width of drain to body

x_{d0} : depletion width of source to body

x_{dep} : depletion width of inversion layer

TABLE-3. SEQUENCE FOR CHARACTERIZATION PROCEDURE



Refurbishing Solid State and Materials Science Research using MEMS

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It is an accepted fact that fundamental discoveries in science lead to technological marvels. It is also equally true that technological developments can enable new discoveries. Thus measurements that were too difficult in yesteryears or signals that were buried in noise can come to life with new technological aids. We will attempt in the following to construct a blue-print for the exploitation of MEMS and related technologies to enhance and richen basic solid state and materials science research. The emphasis will be more on a discussion of the 'possibilities' rather than on a presentation of work done. However, as one example of the application of MEMS we will present recent results in our effort to develop sensitive force and torque detection methods for use in magnetic and scanning probe microscopies.

Innovative Microfluidics and BioMEMS Systems Using Magnetic MEMS Technologies

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MEMS technology is currently enjoying a moment of formidable expansion in synergy with the health and environmental sciences, giving rise to the notion of MEMS for biomedical and biochemical applications, or BioMEMS. Interests in laboratory medicine, diagnostic biosensing technology, miniaturized biochemical analytical instrumentation, and environmental monitoring systems have strongly influenced the early development of BioMEMS. The establishment of microfabricated chemical analysis systems has brought into the immediate horizon the notions of point-of-care detection and analysis, to be achieved by extremely fast, hand-held, and portable 'lab-on-a-chips'. Thus, microfludics and BioMEMS technologies are now having a revolutionary impact over the analytical biochemical industries working on on-chip biochemical micro total analysis systems.

Recently, using an innovative UV-LIGA (UV Lithography-based Galvanoforming) technique developed at the University of Cincinnati, the author has realized several novel magnetic MEMS and microfluidic devices such as microvalves, micropumps and biofilters. With these magnetic MEMS devices, the author has successfully developed several microfluidic devices and BioMEMS devices for a portable bio/chemical detection system or 'lab-on-a-chip'.

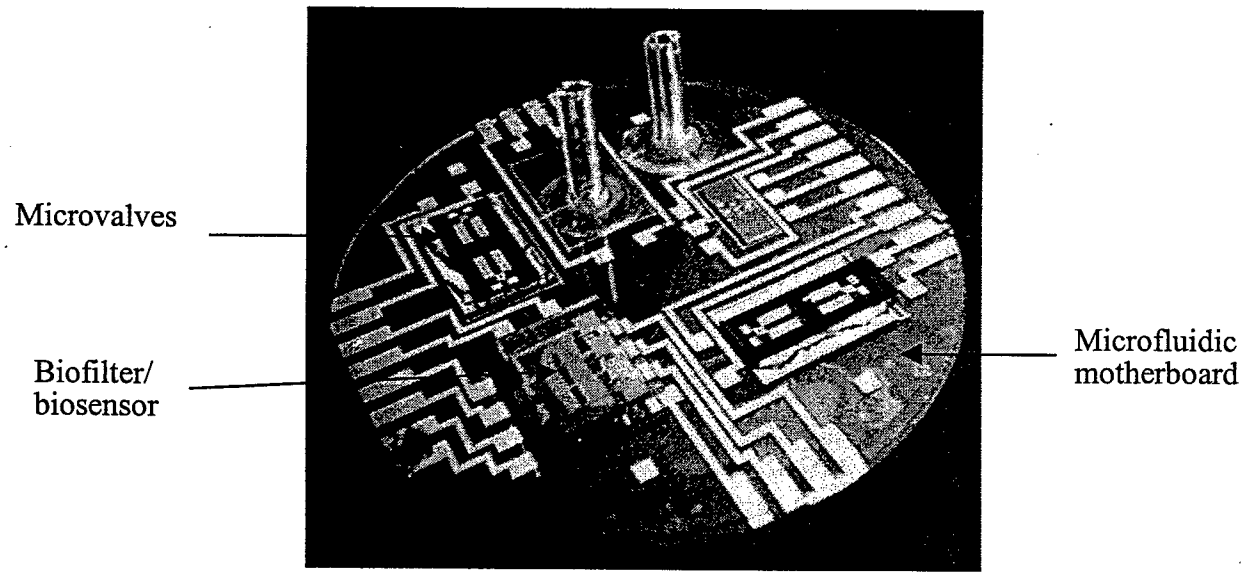


Figure 1. Microfluidic system with microvalves and flow sensors.

In this paper, magnetic MEMS and BioMEMS research activities in the Center for Microelectronic Sensors and MEMS (CMSM) at the University of Cincinnati (UC) will be

described, which includes the development and characterization of microsensors, microactuators, remote bio/chemical detection systems, microfluidic systems, and immunosensors [1-6]. The author and his colleagues at UC are now performing numerous magnetic MEMS and BioMEMS projects to explore various magnetic MEMS-based microfluidic devices and biochemical sensors toward the realization of remotely accessible bio/chemical detection system. An overview of the magnetic MEMS-based microfluidic components and systems (Figure 1) and BioMEMS-based biocells will be presented first, including magnetically driven microvalves (Figure 2), micropumps, flow sensors, magnetic bead separators, biofilters, and immunosensors. Then, microfluidic motherboards and potable biochemical detection systems will be described. The analytical concept is based on an immunoassay with electrochemical detection.

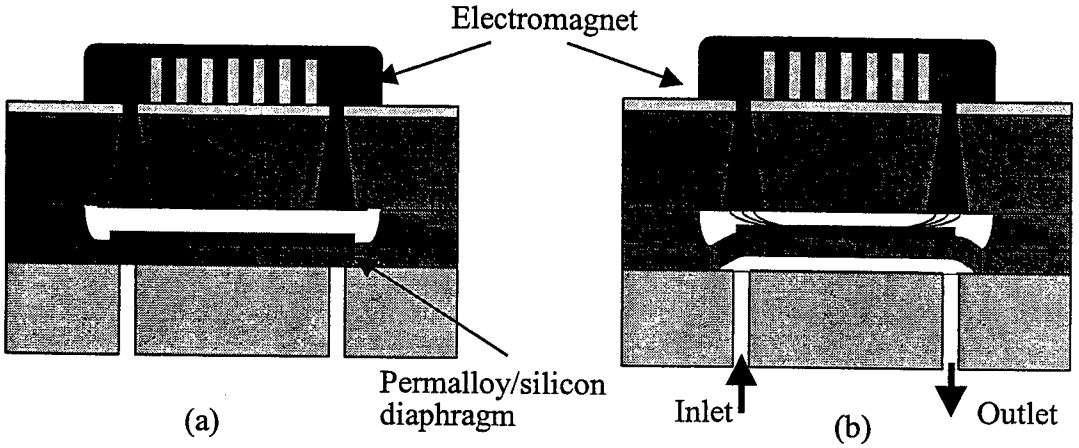


Figure 2. Schematic diagram of magnetically driven microvalve: (a) close and (b) open mode.

Furthermore, an overview of the speaker's recent research achievements at the University of Cincinnati will be presented, discussing the relevant issues to the design, fabrication, and characterization of the magnetic MEMS and BioMEMS devices and systems.

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An Integrated MEMs Approach to Submillimetre Wave Frequency Multiplier Design

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I. Introduction

Systems operating at > 100 GHz tend to be based upon individually fabricated components, such as waveguide blocks, which are difficult and expensive to make. This has tended to limit the range of submm applications to highly specialised ones such as astronomy and remote sensing. Other applications, such as plasma diagnostics, radar and telecommunications, are waiting for appropriate and cost effective technology to become available. A proof-of-concept project to fabricate a fully integrated, micromachined frequency multiplier, tripling from 270–810 GHz, is described here. Other applications for these methods include mm and submm-wave detectors, mixers and oscillators.

The processing scheme involves both planar and three-dimensional lithography, using conventional optical resist and epoxy-based EPON SU-8 [1]. Conventional split-block technology [2] has been replaced with a design featuring a GaAs substrate, on which is formed a varactor diode with an integral, low-capacitance, electroplated contact whisker, integrated with a stripline filter and probe. Trenches patterned in SU-8 on a separate silicon substrate form the input and output waveguide cavities. Accurate registration of the top and bottom substrates is achieved through lithographically defined alignment pins. For the work described here, an in-line configuration of input and output waveguides was used.

II. Fabrication scheme

The processing scheme is outlined in Figure 1. Initially, ohmic regions are formed on the 5x10mm GaAs substrate to provide bias contact and to minimise the varactor substrate resistance. Silicon dioxide is sputtered onto the substrate and a conventionally spun layer of S1813 resist is exposed and developed to form via-hole arrays. These arrays are translated into the silicon dioxide layer by wet etching in buffered hydrofluoric acid (Fig. 1(a)). The exposed GaAs anode regions undergo surface oxide removal in 1:1 HCl:H_2O and platinum plating is performed using Engelhard or Platanex plating solutions. Evaporated anodes are an option at this stage and titanium/palladium diodes have also been fabricated. Typical idealities for the Engelhard and Platanex plated diodes were in the range 1.2-1.3 with reverse breakdown voltages between 8.5-9.5V. Evaporated diodes had idealities 1.2-1.3 with reverse breakdown occurring at 6.5-7.0V.

A 3μm thick layer of SU-8 is spun over the substrate in order to form a further isolation layer. This is exposed and developed to form a continuous layer with an opening over a single selected diode array (Fig. 1(b), Fig. 2). A gold ground plane is evaporated and a further SU-8 layer is spun, exposed and developed to form a dielectric support strip for the filter (Fig. 1(c), Fig. 3). The diode contact whisker is formed by electroplating platinum through a window defined in thick photoresist using a novel method (patent applied for). The electroplating method was described in [3] and has been modified to allow accurate alignment of the whisker above pre-formed anode arrays. At this point an IV measurement can be used to assess the quality of the contacted diode.

Contact to the varactor and electroplated post is achieved using a gold strip, patterned to provide third harmonic rejection and act as a probe within the input waveguide. The strip is formed using evaporated gold followed by another SU-8 layer, which is patterned with the desired stripline shape. A simple gold etch completes the contacting filter and input probe and the AZ4562 layer is dissolved in acetone to leave the anode contacting post supported by the SU-8/gold filter (Fig. 1(d), Fig. 4).

The waveguides and stripline cavity are formed as an in-line arrangement on the second substrate. An SU-8 layer (the thickness of which defines the waveguide height) is processed in order to produce waveguide trenches, which are finally coated in gold. Completed structures have recently been fabricated and preliminary measurements are now underway. Further refinements are planned for the input and output waveguide circuits. Greyscale [4] and stepped resist techniques have been used successfully to produce multi-height structures and can be readily incorporated into the multiplier scheme to allow varied waveguide heights. These methods have already been used to form tapered feedhorn and waveguide transformer sections. Similarly, sacrificial layer techniques have been used to produce sliding waveguide stubs and these will be added to form input and output tuning circuits.

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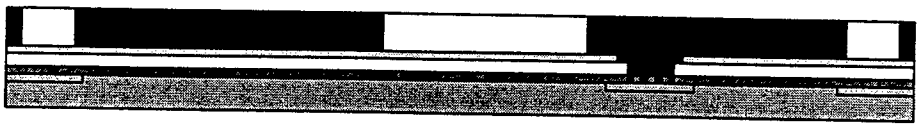
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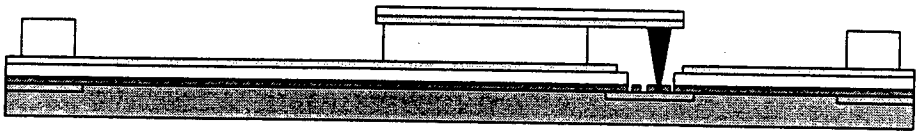
(a) Via etched silicon dioxide layer on GaAs with ohmic contacts.



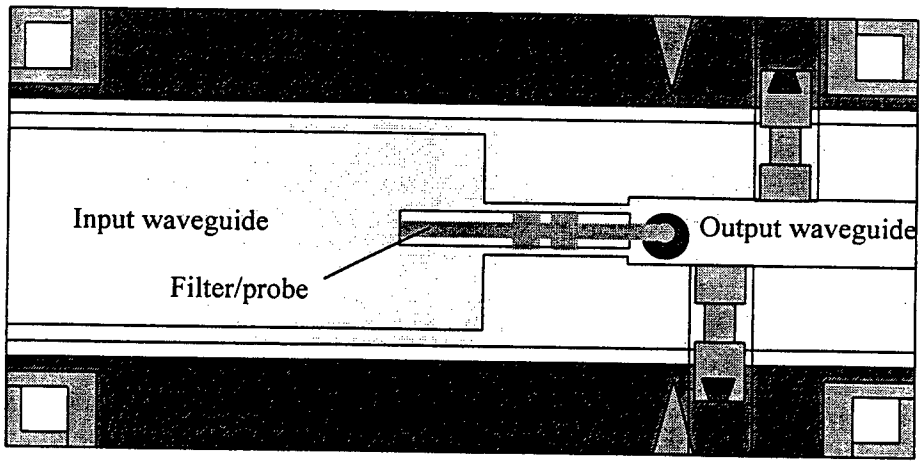
(b) SU-8 isolation layer and gold ground plane.



(c) SU-8 filter support and location blocks and conventional photoresist.



(d) Platinum plated post and contacting gold filter/SU-8 layer.



(e) Aerial view of completed structure, showing location of waveguides, tuning elements and stripline cavity.

Figure 1. Processing scheme for integrated multiplier

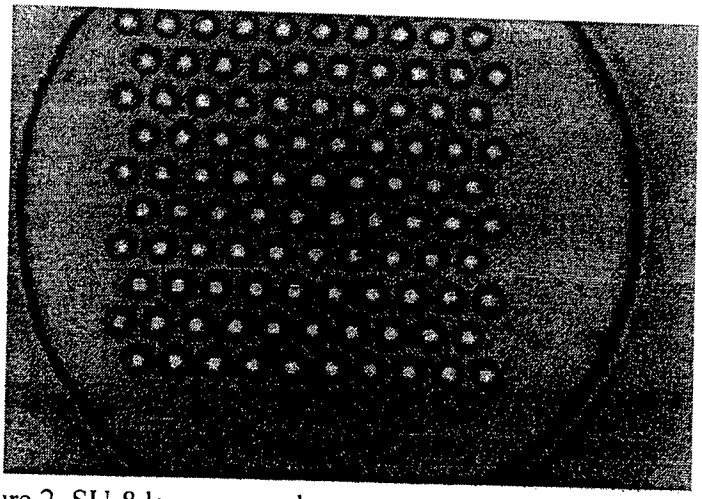


Figure 2. SU-8 layer opened onto array of 3μm diameter anodes.

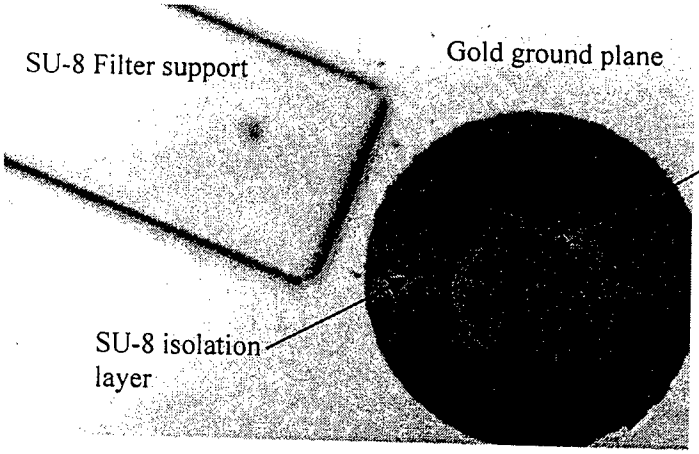


Figure 3. Anode array, SU-8 isolation layer, gold ground plane and SU-8 filter support.

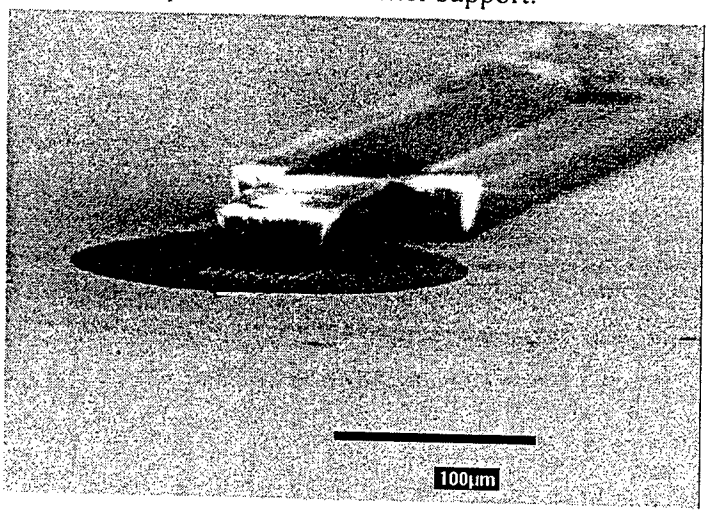


Figure 4. Stripline filter to electroplated platinum post on diode array.

A Bulk Micromachined Monolithic 3-Axis Accelerometer Fabricated With Wafer Bonding And Deep Trench Etching

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I. INTRODUCTION

Micromachined accelerometer is very attractive for space navigation and automobile application, such as airbag, automatic guidance, and security, because of its size, weight, cost, and power advantages [1-8]. In some applications, such as navigation and guidance, 3-axis accelerometers are needed to sense acceleration in different directions. To meet the demand, the conventional way is that three orthogonal accelerometers are mounted on a stage. The disadvantages are that it takes more spaces, and it is difficult to align three accelerometers precisely. In the second way, a single device is used to sense all accelerations along three directions[6-8]. Unfortunately, such a device is difficult to be fabricated, and it is difficult to decouple accelerations along different directions. As an alternative method, three devices, which are fabricated in one chip, are used to sense accelerations along three directions, respectively. Using this method, three accelerometers are aligned precisely, and, indeed, any one of them sensing a directional acceleration along one axis can be designed to have minimum cross sensitivity to accelerations along other two axes. Though it takes more spaces than the second one, it is still enough compact, since all of them are fabricated in one chip. Some resistive 3-axis accelerometers have been developed [6]. Nevertheless, capacitive one is more attractive, because of its high sensitivity and low thermal coefficient. Some surface micromachining capacitive accelerometers have been reported, but its small mass and capacitance limit its sensitivity [7, 8].

In this study, we have developed a bulk micromachined monolithic 3-axis accelerometer fabricated with wafer bonding and deep trench etching, which have high sensitivity along all three directions.

II. STRUCTURES

Two orthogonal lateral accelerometers (shown in Fig. 1) are used to sense x-axis and y-axis acceleration, respectively. In our prototype, we use the simple mass-beam structures. To optimize the performance of the accelerometers, we design some different structures. These efforts include changing shape of proof mass and /or spring, comb fingers as capacitor in order to increase capacitance, compress high mode response, increase linearity, increase shock resistance, and so on. One of them is shown in Fig. 2, in which double fold springs and comb finger capacitors are used to increase the initial capacitance and improve linearity. Using ANSYS, a finite element analysis (FEA) software, we simulated the mechanical performance of the accelerometer with a typical size. The first two modes are shown in Fig.3. The resonant frequency at the first mode is 2.5kHz, while on at the second mode is 9.3kHz.

To sense z-axis acceleration, we design an unbalance teeter- totter -like toritinal structure shown in Fig. 4 (see Ref. [2, 4]). The beam locates at 1/5 of the mass, and it is

bonded to the substrate. A z-axis acceleration will cause the proof mass torque about beam because of unbalanced inertial force. Consequently, the capacitance between proof mass and electrode on glass wafer will change differently. The first two modes simulated with ANSYS are shown in Fig. 5. The resonant frequency at the first mode is 13.7kHz, while on at the second mode is 70.9kHz.

III. FABRECATIONS

This processing combines wafer bonding and ICP deep etching technologies (shown in Fig.6). Samples are (100), medium doped 4" wafers. After shallow trench (about 4um) were etched by either RIE or chemically etching, surface doping was done to get ohmic contact with interconnects fabricated on glass wafers later (if a heavy doped wafers are used, surface doping is not necessary). A Ti/Pt/Au layer with thickness of about 2000A was sputtered on Pyrex glass wafer, and patterned by lift-off to form interconnects, followed by Si and glass wafers anotically bonding at 400C, for 60min. Silicon wafers were thinned to about 100 micron by either mechanically grinning/polishing or chemically etching with KOH. Finally, structures were formed by ICP deep etching. Using this processing, the structure can be very thick (dependent on capability of deep etching, ~100μm in our experiments), so a large mass and capacitance can be formed. Besides, ICP etching can precisely control lateral size, so that symmetry and precision are guaranteed. Consequently, the accelerometer will have high sensitivity.

IV. RESULTS AND DISCUSSION

We have fabricated a prototype of monolithic 3-axis accelerometer. The highest aspect ratio of etching is above 20 (3μm wide and 70μm deep). We have measured and reported mechanical performance of a lateral accelerometer (as shown in Fig. 1). In the device, the cantilever is 559μm long, 13μm wide and 70μm thick, while the area of mass is about $1000*500\mu m^2$. The measured output voltage as the function as input acceleration from -1g to +1g is shown as dots in Fig 7, and the linearly regressed curve is shown in the same figure as solid line. Calculation shows that the sensitivity is 1.85V/g, and the linearity is 99.9954%. The calculated mechanical noise floor is estimated to be about $1.7\mu g/Hz^{1/2}$. The open-loop frequency response and shock resistance were also measured. The mechanical performance of other devices and mechanical performances such as cross sensitivity are in study.

V. CONCLUSION

We have developed a bulk micromachined monolithic 3-axis accelerometer fabricated with wafer bonding and deep trench etching, which are predicted to have high sensitivity along all three directions. In the chip three individual devices used to sense accelerations along three directions, respectively. Using this method, three accelerometers are aligned precisely, and, indeed, any one of them sensing a directional acceleration along one axis can be designed to have minimum cross sensitivity to accelerations along other two axes.

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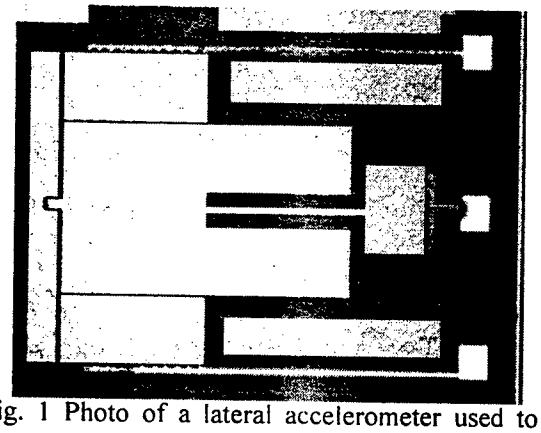


Fig. 1 Photo of a lateral accelerometer used to sense x-axis or y-axis acceleration.

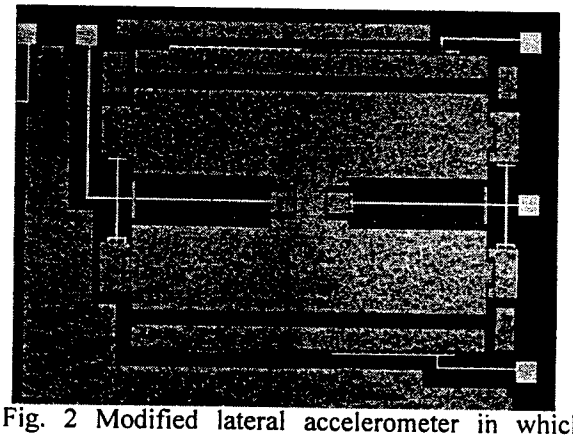
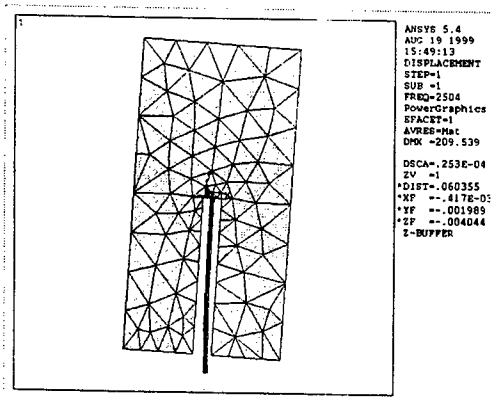


Fig. 2 Modified lateral accelerometer in which double fold springs and comb finger capacitors are used



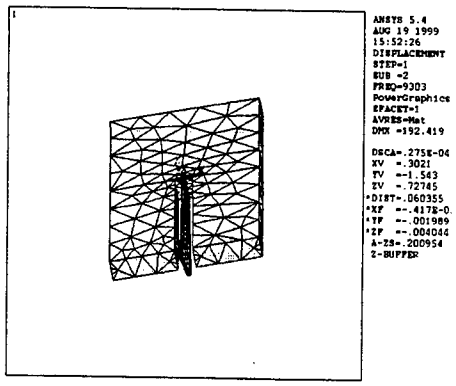


Fig. 3 With ANSYS, simulated the modal shapes of the first two modes of the lateral accelerometer.

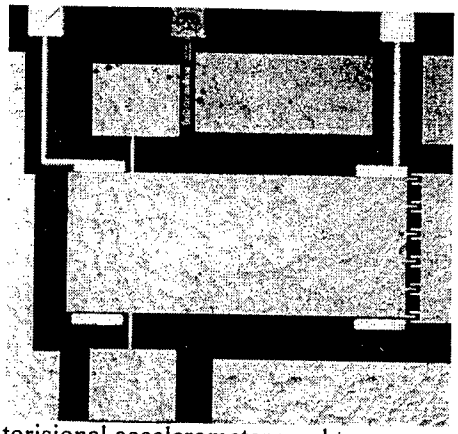


Fig. 4 Photo of a torisional accelerometer used to sense z-axis acceleration.

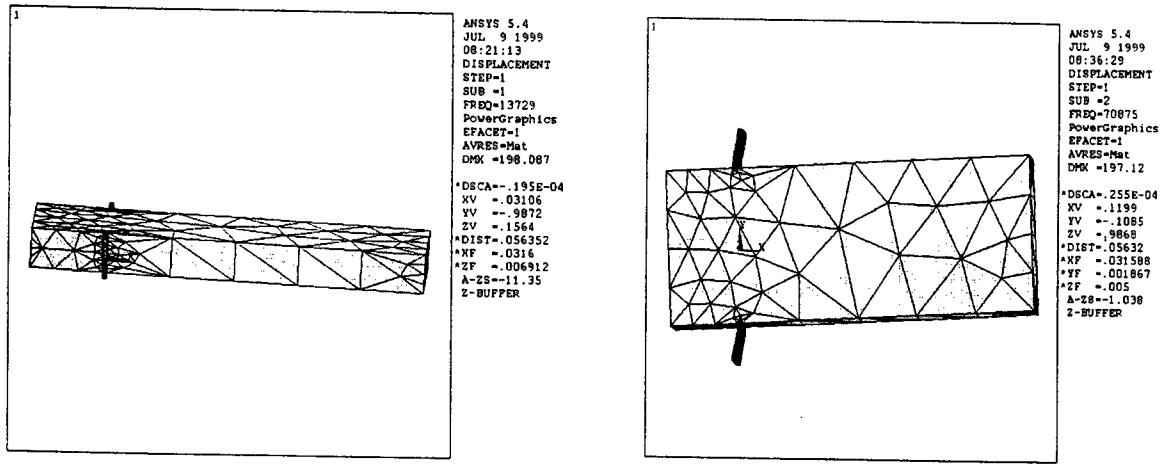


Fig. 5 With ANSYS, simulated the modal shapes of the first two modes of the torisional accelerometer.

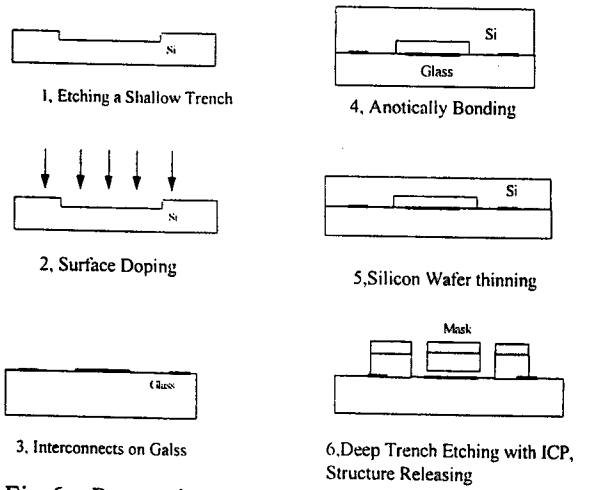


Fig.6 Processing for a bulk micromachined monolithic 3-axis accelerometer fabricated with wafer bonding and deep trench etching.

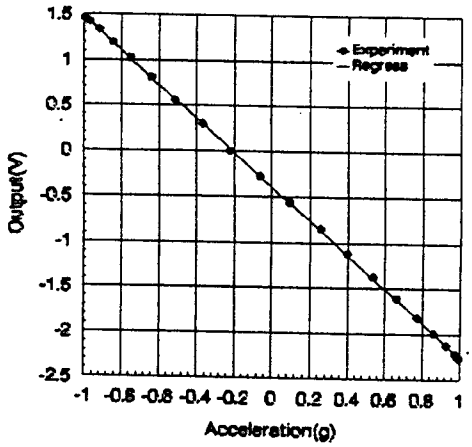


Fig. 7 For the lateral accelerometer shown in Fig. 1, the measured output voltage as the function as input acceleration from -1g to +1g

A Bulk Micromachined Gas Sensor Based on Silicon Beam Resonator with Pt Heater and Temperature Detector

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I. INTRODUCTION

Micro sensors with silicon beam resonator (SBR), in which the measurand is available as the resonance frequency of the silicon beam, offer advantages such as high sensitivity, high accuracy, high resolution, and high stability. The semi-digital character of the output frequency signal is less prone to noise and interference, and is highly compatible with digital circuitry. In addition, compared to conventional sensors such as the quartz crystal microbalance (QCM), the realization process of the micro sensor structure is based on IC technology, which makes it possible to reduce transducer dimensions and add on-chip circuitry. There is an increasing interest in the use of SBR for many sensor applications such as force detection [1], pressure detection [2], mass flow detection [3] and acceleration detection [4]. Recently, the development of micro gas sensors based on silicon nitride [5] or silicon [6] beam is gaining importance.

In this paper, we developed a micro gas sensor based on SBR, on which piezoelectric exciter and detector using ZnO film, and heater and temperature detector using metal Pt film are integrated. By optimizing the design, we fabricated the complete structure only using four masks. The experimental results, compared with QCM, demonstrated that this gas sensor have good performances and suitability for different gas-sensitive films under different operational temperatures.

II. DESIGN

The structure of our micro gas sensor based on SBR is illustrated in Fig.1. The gas sensor detects a certain gas through measuring a change of resonance frequency of the beam caused by gas absorption in the gas-sensitive film on the beam. The silicon beams, which are composed of four structural layers, are 2100μm long, 200μm wide and 10μm thick. The first layer is a high boron doped (p++) silicon sheet, as the main part of the silicon beam, whose thickness can be controlled accurately by selective etching in KOH. This layer is also as the bottom electrode of the ZnO film. The second layer is a ZnO piezoelectric film, which acts as the element to excite and detect vibration of the SBR. The third layer is a metal Pt layer, which has three functions. Firstly, the Pt layer on the middle part of the beam serves as the heater and temperature detector. Secondly, the Pt layer on the both ends of the beam serves as the top electrodes of the ZnO film. Thirdly, the Pt layer on the rest serves as the lead wires and pads. The fourth layer is a gas-sensitive film, in which the measured gas molecules can be absorbed.

The temperature distribution on the silicon beam is important for normal operation of gas-sensitive film. We used ANSYS Release 5.4, a finite element analysis (FEA) software, to simulate the temperature distribution. The simulating result (showed in Fig.2)

shows the temperature distribution is uniform when the heater is situated on the middle part of the silicon beam and its length is less than half of the silicon beam. Therefore, we designed the length of heater to be half of the silicon beam in order to optimize the performance. We also used ANSYS to simulate the mode of vibration of the silicon beam. The result shows that, at the first mode, the interface of tension stress and compressive stress in the surface of the beam is located at the place which is 0.225 times the length of the beam apart from the fixed end of the beam. According to the simulating results, we put heater and temperature detector at the middle part of the beam, and vibration exciter and detector at two fixed ends.

III. FABRICATION

The fabrication process is shown in Fig.3. The starting material is a 4" n-type (100), 5~10 Ωcm, 400μm in thickness, double-sided polished silicon wafer. The fabrication began with the 5000Å thermal SiO_2 and the 2000Å LPCVD Si_3N_4, used as mask material for high boron doping. High boron doping with 10μm depth was performed in the front side at 1140℃ for 13 hour, after the removal of SiO_2 and Si_3N_4 on the front side. Mask 1# was used to pattern KOH-etching windows on the reverse side. A ZnO film (4000Å) was sputtered by dc magnetron reactive sputtering. A annealing step was then performed in oxygen at 500℃ for 4 hours in order to reduce the highly compressive residual stress of the ZnO film, and, especially, to improve the c-axis orientation of the film. Fig.4 shows the x-ray rocking curves at the ZnO (002) diffraction before and after the annealing. Fig.5 shows the change of reflection electron diffraction patterns (RHEED) before and after the annealing. The improvement is distinct after the annealing. Fig.6 is the SEM micrograph of the ZnO film. The ZnO film was patterned by Mask 2#, and etched in buffered hydrofluoric acid (BHF). A Pt layer (5000 Å) was sputtered on the ZnO film, and patterned by lift-off employing Mask 3# to form the top electrodes, heaters, temperature detectors, lead wires, and pads. With the front side of the wafer protected by using a Teflon holder, the anisotropic etching of the reverse side was performed in KOH solution at 80℃, until the etching stop by high boron doped silicon. Mask 4# was used to pattern the beams, followed by inductive coupled plasma reactive ion etching (ICP RIE). The next step in the process was depositing of the gas-sensitive film. We employed two types of gas-sensitive films. One is triethanolamine operating in room temperature, deposited by spray coating, and another is SnO_2 operating in high temperature, deposited by sputtering. Finally, the wafer was diced and packaged in 18 pins ceramics package. Fig.7 is the optical photograph of the complete micro gas sensor with eight silicon beams.

IV. RESULT AND DISCUSSION

The silicon beam is operated in a self-oscillation mode at its resonance frequency using an external feedback loop. The output of the vibration detector on the beam is connected to an external amplifier and a frequency counter. After the signal is amplified, the output of the external amplifier is applied to the vibration exciter on the beam to close the feedback loop. When the total amplification in the feedback loop is sufficient, self-oscillation occurs at the resonance frequency of the silicon beam. The resonance frequency is measured with the frequency counter. A QCM gas sensor, coated with a same gas-sensitive film, is integrated in a measurement chamber with the micro gas sensor in order to compare their characteristic.

The two gas sensors were exposed to different concentrations of NO_2. The frequency shift as a function of NO_2 concentrations was measured and shown in Fig.8. The frequency shifts of the two gas sensors coated with triethanolamine are linear in measuring NO_2 whose concentration varied from 0 to 100 ppm. The sensitivities of gas sensors based on SBR and based on QCM are 0.9Hz/ppm and 1.3Hz/ppm, respectively. They are on the same order of magnitude. The detectable limits of the two gas sensors to NO_2 are both 1 ppm.

In addition, the micro gas sensor based on silicon beam coated with SnO_2 film was characterized in ethanol at 210℃ and in methanol at 320℃. The results are similar to Fig.8. The detail will be presented in other paper.

V. CONCLUSION

In this communication, we have fabricated a micro gas sensor based on silicon beam resonator. The resonance frequency of the sensor is reduced due to additional mass loading by absorbed gas molecules. The sensitivity of the sensor is on the same order of magnitude as for conventional QCM sensor while the total area is reduced by two orders of magnitude. The sensor is suitable for different gas-sensitive films under different operational temperature, due to the integrating with the heater and temperature detector.

ACKNOWLEDGMENT

The authors would like to thank Prof. Dacheng Zhang and Li Ting for useful discussion, and Dayu Tian, Wang Ying, Li Jin and Luo Kui for their help in wafer fabrication.

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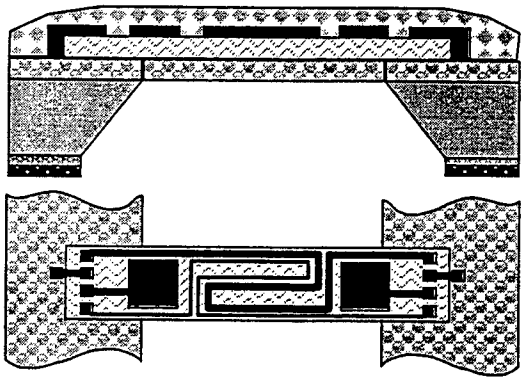


Fig. 1 Schematic drawing of the SBR gas sensor

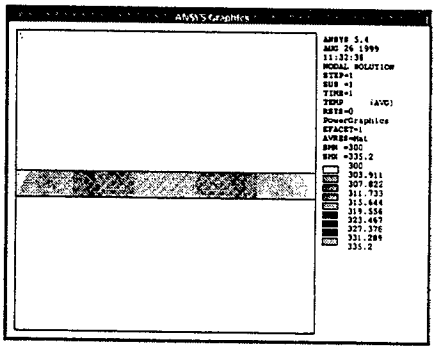


Fig.2 Temperature distribution on the beam

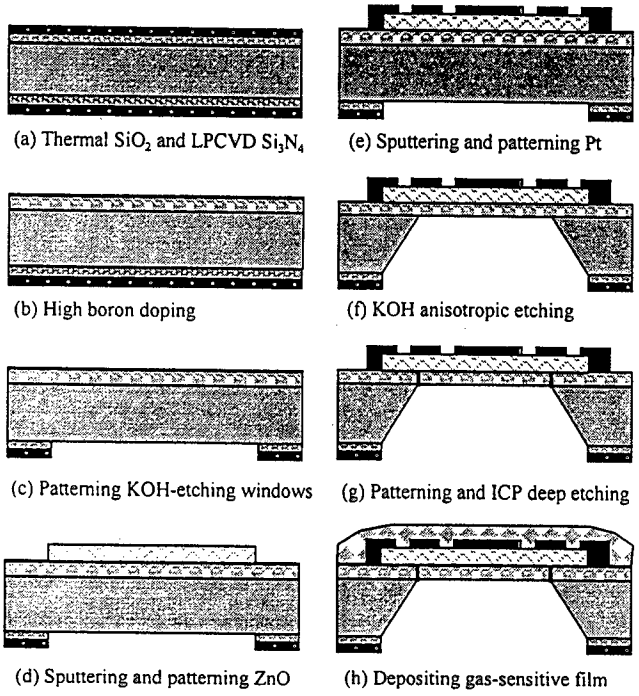


Fig.3 Fabrication process of the SBR gas sensor

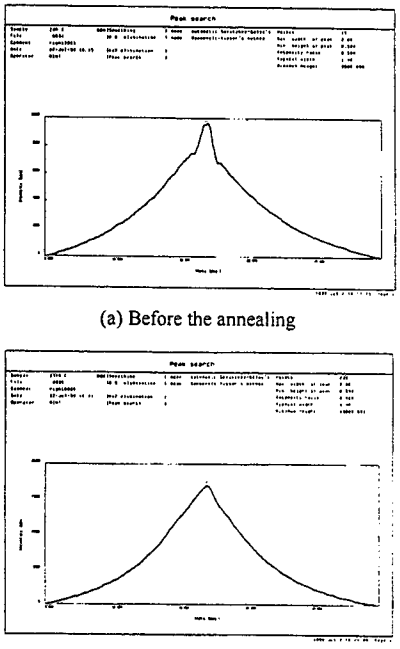


Fig.4 X-ray rocking curves of ZnO (002) diffraction

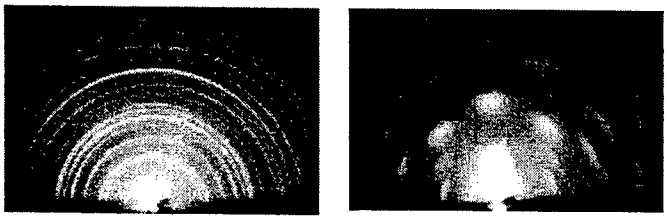


Fig.5 RHEED patterns of the ZnO film

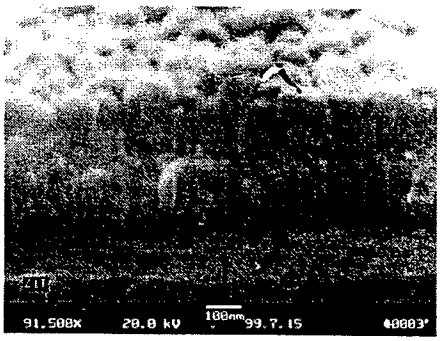


Fig.6 SEM micrograph of the ZnO film

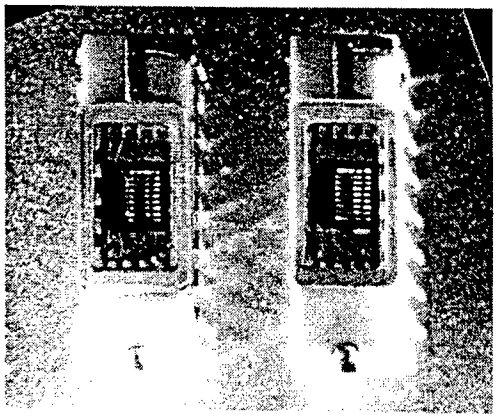


Fig.7 Optical photograph of the SBR gas sensor with eight beams

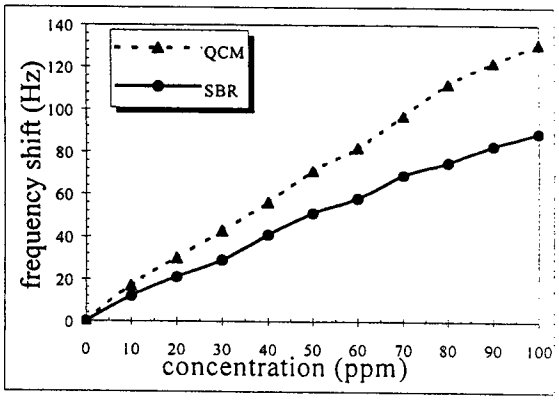


Fig.8 Frequency shift as a function of NO_2 concentration

Characterization of Heterostructure Bipolar Transistors by the Spectral Photocurrent Technique

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Abstract *– Spectral photocurrent studies are performed on emitter/base and collector/base junctions of HBTs. The transistors possess a window in the emitter metal to allow front side illumination. We report results obtained on GaAs based HBTs with AlGaAs and InGaP emitter and collector structures. These results provide new and valuable information on the energy configuration of these junctions for device optimization.*

1. Introduction

Heterojunction Bipolar Transistors (HBTs) often employ emitter and collector layers with varying material composition and doping concentrations to optimize device performance. A detailed understanding of these variations is important for device design and provides important feedback to the material grower. New characterization techniques are needed to analyze these junctions (particularly what happens close to the heavily doped base). We have previously used photoelectric techniques [1] to analyze fully fabricated InP based HBTs, using backside illumination. In this paper, we apply this method to specially fabricated InGaP(AlGaAs)/GaAs single and compound collector HBTs using front side illumination.

In these measurements, the photocurrent of the emitter/base and the collector/base junctions are studied. Figure 1 presents the energy diagram of a typical collector/base junction without applied bias voltage. Optical absorption generates electron hole pairs both in the base and the collector areas. All carriers, photogenerated in the depleted collector area (Process B) contribute to the photocurrent due to the electric field. The holes and the electrons move towards the base and collector, respectively. Electrons and holes, photogenerated in the undepleted areas also can contribute to the photocurrent. The thickness of the base is much smaller than the electron diffusion length. Hence, electrons photogenerated in the base (Process A), escape either to the emitter or collector. Similarly, holes, generated in the undepleted part of the collector (Process C) have a 50% probability to reach the base, contributing to the photocurrent. The other 50% of holes move towards the heavily doped collector part. Due to the heterobarrier, these holes remain in the collector and do not contribute to the photocurrent. Also, carriers generated in the GaAs layer of the collector (Process D) are not able to escape towards the base

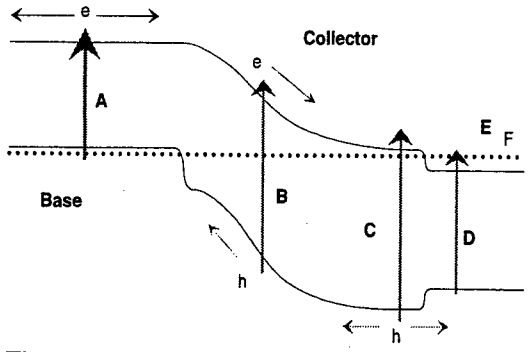


Figure 1. Energy diagram of collector/base junction, indicating optical excitation in different parts of the structure.

due to the heterobarriers. The electron and hole barriers play a key role in the flow of the photogenerated carriers.

The energy configuration of the junctions depends strongly on the applied voltage. This voltage determines the width of the depletion layer, impacting the photocurrent. Also, the height of barriers depends on the electric field in the junctions. Especially, grading layers have a significant impact on the effectiveness of the barriers. These grading layers present electric fields to the electrons and holes, either accelerating or retarding them. These fields are modified by

applied voltages and their direction may be reversed, eliminating or generating barriers. Hence, the magnitude and the spectral characteristics of the photocurrent depend on the applied bias voltage and the understanding this dependence provides invaluable information on the energy configuration of the heterojunctions. The change in spectral characteristic with the change in applied junction voltage provides energy and material information at the depletion boundary.

The purpose of this paper is to demonstrate the spectral photocurrent technique, using examples of collector/base and emitter/base spectra and their dependence on applied bias voltage. These data are correlated with electrical characteristics.

2. Experimental Technique

The HBTs, tested have windows in the emitter metal to allow illumination of the active transistor area. The dimensions of the emitter and window are 100x120 and 90x60 μm^2, respectively. The measurements are performed on-wafer at room temperature. Light from a halogen tungsten source passes through a mechanical chopper and a monochromator and is piped via an optical fiber to the microscope of the probe station. The light is focused through the microscope onto the transistor, resulting in a light spot with a diameter of 70 µm. The electrical part of the measurement system has been described previously [1].

3. Transistor Structures

In this study, four wafers with different emitter and collector structures are investigated. All transistors utilize a 120 nm thick base, p- doped to a concentration of $4x10^{19}$ cm^{-3}. Table 1 provides the emitter and collector combinations of the four wafers, identified by their wafer numbers. Table 2 presents the emitter and collector layer structures of the devices discussed in this abstract. Grading layers are used with all AlGaAs layers to avoid charge storage at the collector and to ease charge injection at the emitter. No grading layers are utilized in InGaP structures. A thin, highly doped GaAs layer is employed with the InGaP collector to minimize charge storage effects.

Table 1. Wafer Material Characteristics

		Emitter	
		InGaP	AlGaAs
Collector	InGaP	5505	5504
	AlGaAs		5503
	GaAs		5502

Table 2. Emitter and Collector Structures

Description	Doping Concentration [cm^{-3}]	Thickness [nm]
InGaP Emitter		
InGaAs Cap		
N GaAs	$8x10^{18}$	120
N InGaP (0.5)	$3x10^{17}$	35
AlGaAs Collector		
N AlGaAs Grading	$3x10^{16}$	100
N AlGaAs (0.25)	$3x10^{16}$	120
N AlGaAs Grading	$3x10^{16}$	80
N GaAs	$3x10^{16}$	400
N GaAs	$5x10^{18}$	1000

4. Photoelectric Analysis of the Collector/Base Junction

Figure 2 presents the spectral characteristics of the AlGaAs collector/base junction for three junction voltages: Vcb = +1, 0, and –0.6 V. The curves are plotted both in logarithmic and linear format. The +1 and 0 V curves have GaAs like character with very steep fall-off at the bandedge (30 meV/decade). This indicates that the photocarriers are generated in a very pure, low doped material. The only layer within the collector with this characteristics is the 400 nm, $3x10^{16}$ doped GaAs layer. Photogenerated holes in this layer travel through the AlGaAs to the base. These observations prove that the lower AlGaAs grading layer was successfully fabricated. At Vcb = -0.6 V, the fall-off at the GaAs band edge is 115 meV/decade, a much larger value than observed at

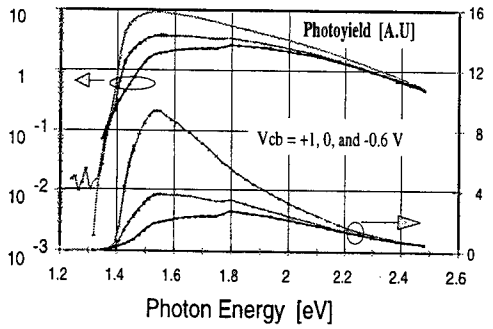


Figure 2. Spectral photoyield of AlGaAs collector junction for three applied voltages

0 and +1 V. Also the signal magnitude depends on the applied junction voltage. These findings suggest that at Vcb = -0.6 V, the depletion boundary is within the AlGaAs layer and that the holes generated in the GaAs do not have sufficient energy to travel into the AlGaAs layer. The GaAs signal in the –0.6 V curve probably stem from

electron injection from the base. The 0 and –0.6 V curves show a small, but clearly identifiable signal at hν = 1.75 eV due to photogeneration in the AlGaAs layer. The AlGaAs signal is expected to be smaller than the GaAs signal due to differences in layer thickness and absorption coefficient. This signal is not observable at Vcb = 1 V since the strong GaAs signal rapidly decays with increasing energy in this range.

Figure 3 provides spectral response characteristics under forward bias, -0.4, -0.6, and -0.8 V. The curves, obtained at -0.4 and -0.6 V are

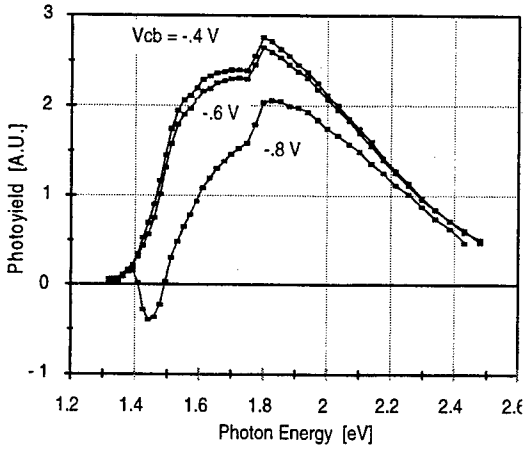


Figure 3. Spectral Photoyield of AlGaAs collector for three forward bias voltages

very similar to each other, while the –0.8 curve differs vastly. Especially, the signal changes polarity at approximately 1.45 eV. Subtracting the –0.8 V from the -0.6 V curves yields the GaAs spectrum with steep fall-off at the band edge. This finding suggests that charge storage takes place at the interface between the low doped GaAs and AlGaAs collector layers, which affects the forward junction current. The agreement between the -.4 and -.6 V curves suggests that the base is the source for the GaAs like photocurrent.

In Figure 4, the dependence of the photocurrent on the collector base voltage at two photon energies, 1.5 and 1.8 eV is shown. The 1.5 eV signal stems from photogeneration in GaAs layers while the 1.8 eV signal also includes AlGaAs contributions. Both curves in Figure 4 show strong change between Vcb = -0.2 and +0.5 V. From the spectral characteristics we know that at the negative voltages this signal stems from photoexcitation in the base while at positive voltages the low doped collector layer is the dominant source for the photocurrent. Hence, if the depletion boundary lies in the AlGaAs layer, a hole barrier of 330 meV (difference between the

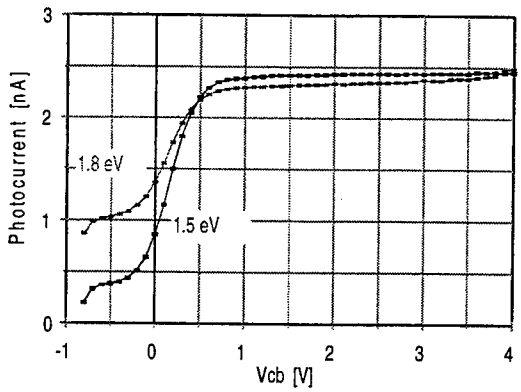


Figure 4. Dependence of the photocurrents of the AlGaAs collector on junction voltage

AlGaAs and GaAs bandgaps) exists which effectively blocks the flow of holes, generated in the low doped GaAs layer, towards the base. If the depletion boundary is within the GaAs layer, this barrier is minimized or eliminated, depending on the location of the boundary and the holes can freely flow towards the base. These studies provide a novel profiling technique for heterostructure devices, complementing electrical analysis data such as capacitance voltage and current voltage results.

These data do not fully agree with results from capacitance voltage (C-V) measurements, shown in Figure 5. This figure indicates that the AlGaAs layer is fully depleted at -0.5 V while the lower grading layer is depleted at 2 V. At 0.5 V, there should exist a hole barrier approximately five times the thermal energy, which would block the flow of holes, generated in the GaAs layer. The photomeasurements predict that the depletion boundary lays in the GaAs layer at Vcb = 0.5 V, in contradiction to the C-V results.

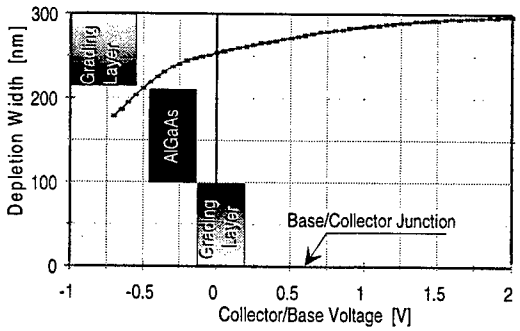


Figure 5. Depletion width vs. collector junction voltage, obtained from capacitance voltage measurements

5. Photoelectric Analysis of the Emitter/Base Junction

The spectral photoyield for the InGaP emitter is shown in Figure 6 for the indicated emitter/base junction voltages. The threshold energy for all

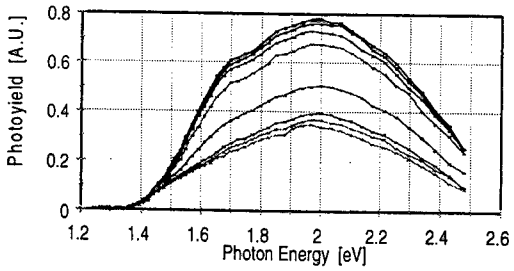


Figure 6. Spectral photoyield of InGaP emitter. From top to bottom, Veb =1.5 to 0 V in 0.25 V steps. Lowest curve: -0.8 V

curves is approximately 1.4 eV, the GaAs bandgap. The bandedge fall-off in logarithmic format is 90 meV/decade, indicating emission from highly doped or impure material. We observe that below 1.5 eV the photoyield is independent of the junction voltage. Hence, the signal in this energy range stems from the emission of photogenerated electrons from the base into the emitter. Emission of holes, photogenerated in the GaAs layer of the emitter is ruled out as an explanation for the signal below 1.5 eV since this current would depend strongly on the bias voltage. The curves indicate a faint second transition at approximately 1.8 eV due to photogeneration in the InGaP layer. This signal is expected to be very small since the layer thickness is only 35 nm.

Figure 7 presents the dependence of the photocurrent, obtained at 1.5 and 1.9 eV, on the

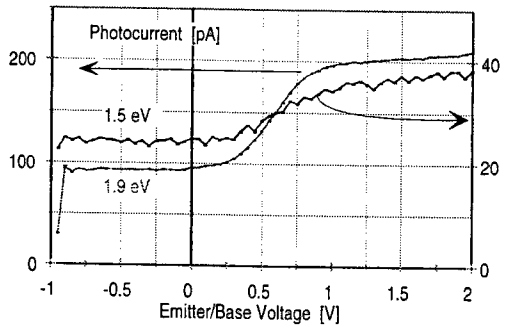


Figure 7. Photocurrent of InGaP emitter junction obtained at the indicated photoenergies

emitter to base junction voltage. Both curves indicate that the photocurrent is independent of emitter base voltage in a bias range below 0.25 V and marginally depends on this voltage above 1 V. Between these two ranges, one observes a strong change in photocurrent with bias voltage, especially for the 1.9 eV curve. In agreement with the spectral response, the data suggest that for Veb < 0.25 V only the photogeneration in the base contributes to the photocurrent and this current does not depend on the junction voltage. Photogeneration in the emitter contributes to the photocurrent for more positive voltages. Hence, subtracting the 0 V spectrum from spectra obtained at more positive junction voltages provides the spectral characteristics of the emitter contribution. We observe that all curves have identical threshold energies of approximately 1.45 eV, suggesting photogeneration in the $8x10^{18}$ cm^{-3} doped GaAs layer. The InGaP layer provides a barrier to the generated holes at Veb < 0.25 V but this barrier does not exist at Veb > 1 V. These findings suggest that the depletion boundary lays in the InGaP layer at Veb < 0.25 eV and in the GaAs layer at larger voltages.

Summary and Conclusions

We performed spectral photocurrent studies on GaAs based HBTs with InGaP and GaAlAs emitters and with AlGaAs, InGaP, and GaAs collectors. In this abstract, results on the AlGaAs collector and InGaP emitter are presented. These measurements provide a novel profiling technique for heterojunctions in fully fabricated transistors. We observed that both grading layers in the AlGaAs/GaAs compound collector were successfully implemented. Electron emission from the base was not impeded by the heterobarrier even under forward bias. Also, the lower heterobarrier allowed the flow of holes under reverse bias condition. The agreement between capacitance voltage and spectral photocurrent profiling was marginal and more work is required to resolve the differences.

Studies on the InGaP emitter indicate that the emitter/base heterobarrier is small and does not impede the emission of photogenerated electrons from the base into the emitter, even under forward bias. Further results suggest that the InGaP/GaAs interface in the emitter is not abrupt.

These heterobarriers are able to stop the flow of holes under low field condition or for abrupt junctions. This finding can be utilized in the design of high power transistors, where holes, generated by impact ionization impede the performance of HBTs.

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A New Accurate model for Drain-Gate Avalanche Current Source of GaAs MESFET

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Abstract – A new drain-gate avalanche current source model which is controlled by V_{ds} and V_{gs} is proposed. A Fujitsu MESFET, FLC-103WG, is adopted for measurement and the model is extracted. Compared with several conventional models, the proposed model is found to be more accurate than the Curtice and Fujii model.

1. Introduction

The design of power GaAs MESFET amplifiers, mixers, and oscillators can be made more accurately if the large-signal characteristics of the MESFET are modeled more accurately. Generally, three nonlinear current sources should be included in the nonlinear models. The main $I_{ds}(V_{ds}\ V_{gs})$ current source represents the large-signal form of the transconductance. The I_{gs} voltage-controlled current source represents the forward biased input diode. The I_{dg} current source is an avalanche current source between drain and gate. A lot of empirical models suitable for the simulation of GaAs MESFET in nonlinear circuit have been developed. Most of those models can be used to predict gain, intermodulation distortion, generation of harmonics, and others. But most of these models focus only on the main current source I_{ds}. The avalanche current source is usually ignored. The modeling of the avalanche breakdown current source is generally grouped under two methods. The first method includes using the piecewise functions [1] to describe the current before and after breakdown. The second method involves using the exponential function [2] to model the current source. Both of these methods have their weakness. For piecewise function fitting, its first derivative is discontinuous. As such, it is difficult to implement in CAD software, where intermodulation distortion prediction is needed. For the normal exponential function, it can accurately describe the current source before and near the breakdown voltage, but not after the breakdown. The avalanche current looks more like a linear function rather than a exponential function, and the exponential function increases much faster than the measurement results.

In this paper, a new accurate avalanche breakdown current model for GaAs MESFET is proposed. The model can describe the avalanche current both before and after breakdown voltage, and because it is a continuous function, it can be easily programmed into a commercial CAD software such as HP MDS. A commercial high power MESFET (Fujitus FLC103WG) is adopted for verification and the model is extracted. The simulation and measurement results agreed excellently.

2. The model functions

The current model proposed by Curtice [1] for breakdown phenomenon is a piecewise function:

$$I_{dg} = \begin{cases} \dfrac{V_{dg}(t) - V_B}{R_1} & V_{dg} > V_B \\ 0 & V_{dg} < V_B \end{cases} \quad \text{where } V_B = V_{B0} + R_2 \cdot I_{ds}$$

This equation can describe the I_{dg} when V_d is much less or greater than V_B, but it cannot describe the breakdown phenomenon around the breakdown voltage. Since it is a piecewise function, it is difficult to implement into a CAD software.

Recently, Fujii *et al.* [2] has proposed an exponential function, which is given below, to describe this phenomenon.

$I_{dg} = I_{g0}[\exp(\alpha_g \cdot (V_{dg} - V_{BR}(V_{gs}))) - 1]$, where $V_{BR}(V_{gs})$ is represented as follows:

$V_{BR}(V_{gs}) = V_{BRcnt}(1 + \psi)$ and V_{BRcnt} is selected at the center of the linear potion of a measured V_{BR} versus V_{gs} slope. The ψ is a power series function centered at V_{GScnt} with V_{gs}, and is expressed as:

$\psi = P_1(V_{gs} - V_{GScnt}) + P_2(V_{gs} - V_{GScnt})^2 + P_3(V_{gs} - V_{GScnt})^3 + \cdots$,

where the variables P_I, I=1,2,3..., are the fitting parameters.

This exponential equation can describe the avalanche phenomenon accurately when the V_d is less or around the breakdown voltage. But when the V_d is much greater the breakdown voltage, the simulation result increases much faster than measurement result, which approximates more like a linear function.

3.The Improved model for avalanche current source

An Improved model for avalanche current source is proposed. It can describe the current source both below and above the breakdown voltage. When the V_d is less than or around the breakdown voltage, the model equation is approximately an exponential equation. While the V_d is much greater than breakdown voltage, the model equation approximates as a linear equation. The proposed avalanche current source model equation is given as:

$$I_{dg} = I_{g0}[\exp(\alpha \cdot V_{dg}) - 1] \quad \ldots(1)$$

where $$\alpha = \frac{-\operatorname{arcsin} h(V_{ds} - F)}{C} \quad \ldots(2)$$

$C = P_0 + P_1 \cdot V_{gs} + P_2 \cdot V_{gs}^2 + \ldots$ and $F = A \cdot V_{gs} + B$,

the variables P_i, i=0,1,2,... and A,B, I_{g0} are the fitting parameters. In our extraction procedure, we found that for the power series C, the first three components is enough for fitting.

4.Result

To verify the new model, a commercial packaged MESFET, Fujitsu FLC-103WG is measured and the breakdown model is extracted. Fig. 1 is the topology of the large signal model. For comparison purpose, the Curtice model and the Fujii model also are extracted. Fig. 2 shows the simulation and measurement results. The model is measured at V_{gs} from –3v to –0.5v and V_{ds} from 0v to 20v. From the diagram, we notice that the new model is more accurate than the Curtice and Fujii model at all the bias points.

Following is the parameters of the new model. P_0, P_1, P_2, A and B are dimensionless quantities.

P_0	P_1	P_2	A	B	I_{g0} (A)
30.9	15.8	2.4	8	54	6.59×10^{-8}

5.Conclusion

In conclusion, a novel avalanche current source equation, which can accurately describe the measurement result, is proposed. Compared with the available conventional model, the proposed model is noticed to be more accurate. The simulation and measurement results of our proposed model agree excellently.

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6.Figures

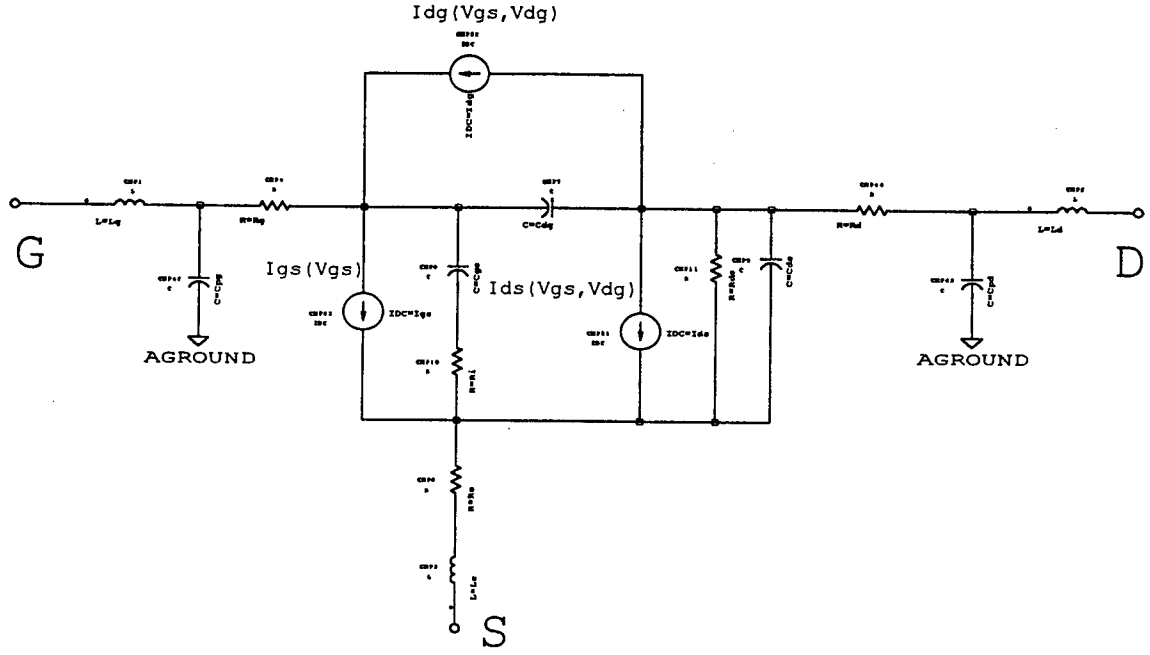


Fig. 1 The Large Signal Model of the MESFET

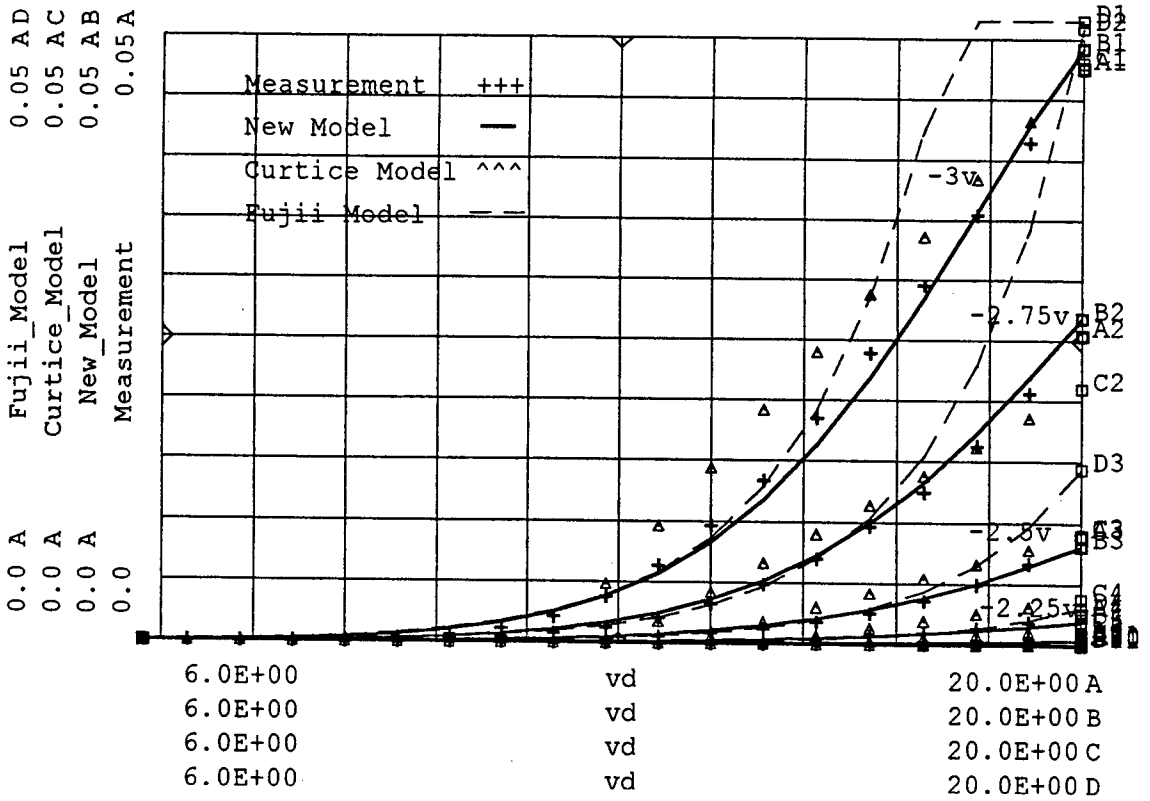


Fig. 2 Measured and Modeled Drain Breakdown Current of the MESFET, FLC-103WG.

Design and Interpretation of Laser Absorption Measurements for Power Devices

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I. INTRODUCTION

For optimizing the performance of modern power devices, the recently developed internal laser probing techniques (e.g. [1], [2]) have shown to be a useful supplement to the electrical measurement of the terminal behavior. Those characterization methods exploit the dependence of the refractive index on the free carrier concentration and the lattice temperature and, thereby, enable the experimental determination of carrier concentration and temperature profiles in the interior of semiconductor devices. However, if the evaluation of the measurement signals is merely based on geometrical optics, diffraction phenomena and the finite extension of the probing beam cannot be properly taken into account. For that reason, a physically rigorous model of the entire measurement process has been developed ([3]). In this work, it is used for investigating the beam propagation in laser absorption measurements. As a result, various design parameters of the optical setup, as e.g., the numerical beam aperture, can be optimized.

II. MEASUREMENT SETUP

The experimental setup for internal laser absorption and deflection measurements is shown in Fig. 1. During transient switching conditions, carrier injection decreases the transmitted intensity. In addition, gradients of carrier concentration and lattice temperature cause a deflection of the focused laser beam, which is transformed into a parallel shift by a long distance objective. A four-quadrant photodiode detects both the transmitted intensity (sum of the photo-currents) and the parallel shift (difference of the photo-currents of opposite segments). From these signals the local carrier concentration and temperature gradients can be extracted. For example, the excess carrier concentration Δn is obtained from the absorption law

$$I_{on} = I_{off} \exp\left(-L\frac{\partial \alpha}{\partial C}\Delta n\right) \tag{1}$$

where I_{on} and I_{off} are the transmitted intensities during on-state and off-state of the device, respectively, L is the interaction length, and $\frac{\partial \alpha}{\partial C} = \frac{\partial \alpha}{\partial n} + \frac{\partial \alpha}{\partial p}$ is the dependence of the absorption coefficient on the carrier concentration under high injection conditions. Vertical profiles of the carrier density and temperature distribution are obtained by shifting the device along its vertical axis.

III. NUMERICAL SIMULATIONS

The power dissipated by the probing laser beam does not affect the device operation and can be neglected. Therefore, the simulation of the entire measurement process can be based

on the scheme sketched in Fig. 2 [3].

First, a self–consistent electrothermal device simulation [4] of the specific operating conditions delivers the transient carrier concentration and temperature distributions during measurement. From these quantities the modulation of the complex refractive index (real part and absorption coefficient) is calculated. Finally, simulating the beam propagation through the device under test, the lenses, and the aperture holes for a properly chosen sequence of time steps yields the field distribution on the detector, from which the time–dependent measurement signal is constructed.

IV. OPTICAL FIELD DISTRIBUTION

Figure 5 shows the field distribution at the rear surface of the device. The beam profile is nearly Gaussian, when the laser beam traverses the device at a position in the middle of its vertical extension. However, considerable distortions including several additional maxima are observed for beam positions near the top and the bottom boundaries.

These effects can be explained by the field distribution in the interior of the device. The spot diameter in the focus is $25\,\mu$m (numerical aperture 0.04) and increases up to $39\,\mu$m at the edges ($L = 2.5\,$mm), cf. Fig. 3. Due to diffraction and reflections at the anode metallization layers (cf. Fig. 4), the beam profile exhibits several minima and maxima.

V. OPTIMIZING THE OPTICAL PARAMETERS

In order to investigate the error introduced by the above–described effects, we simulate the whole probing process in all details (cf. section III.) and extract the carrier concentration according to eq. (1). This value is then compared to the carrier concentration as obtained from the electrothermal device simulation (cf. Fig. 7).

Because of the finite lateral extension of the laser beam, only an average carrier concentration in a region around the vertical position of the laser beam is detected. Diffraction and reflection at the metallization layers make the problem even worse, since the beam traverses regions with different carrier concentrations.

Another error is introduced by the geometry of the detector. The beam deflection shifts the maximum of the field distribution from the gap between the individual segments of the four–quadrant photodiode towards one of the segments, since the detector position is adjusted such that the deflection signal in the off-state vanishes. Therefore, the absorption signal seems to increase, even if the transmitted intensity stays the same. Replacing the four–quadrant detector (cf. Fig. 7) by a pin diode (cf. Fig. 8) diminishes the deviation and enables measurements closer to the upper and lower device surfaces.

Fig. 6 compares the average deviation for different spot diameters of the incident Gaussian beams and different sample sizes. For small numerical apertures, there is a large error due to the large spot diameter. Using larger apertures decreases the minimum spot diameter, but increases the beam spreading and, therefore, the spot diameter at the device surfaces. In this case, the averaging near the surfaces introduces the dominant error. For that reason, there is an optimum numerical aperture which produces the minimum deviation. Since the spot diameter at the surfaces scales linearly with the device length, the optimum aperture increases and the minimum error decreases with shrinking device extensions.

VI. DISCUSSION AND CONCLUSION

One should note that, however, the reduction of the device length is limited by the following practical constraints: First, the sample preparation is only manageable for devices longer than 0.5 mm. With view to an acceptable signal-to-noise ratio, this minimum length is also necessary for detecting carrier densities down to $10^{15}\,\mathrm{cm}^{-3}$. Finally, to prevent an additional error introduced by surface recombination the device length should exceed 10 to 20 ambipolar diffusion lengths. The typical ambipolar carrier lifetime in power devices subjected to heavy metal diffusion is about $1\,\mu\mathrm{s}$. The resulting diffusion length is approx. $40\,\mu\mathrm{m}$ so that a device length of 0.8 mm is required.

As a result of our investigations it is now possible to predetermine an optimum combination of device length and numerical aperture for precision measurements of the carrier profile in power devices.

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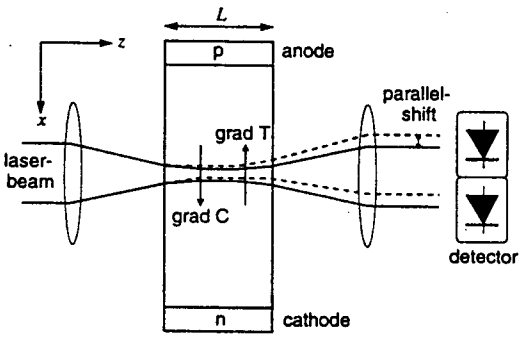


Figure 1: Measurement setup for laser absorption and deflection measurements

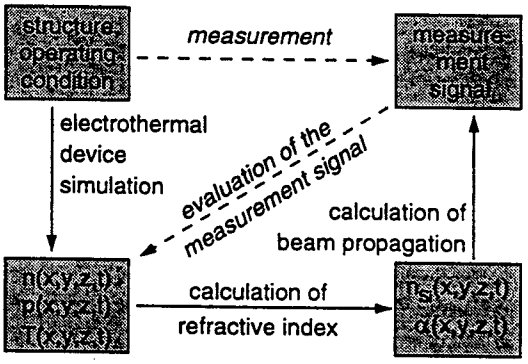


Figure 2: Simulation strategy for the simulation of the whole measurement process

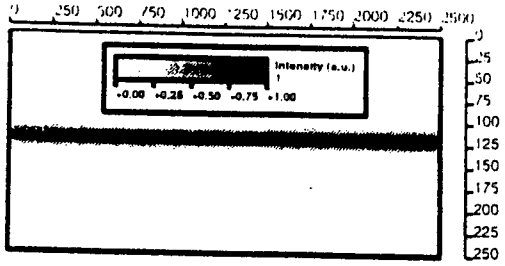


Figure 3: Intensity distribution in the interior of the device under test. The laser beam incides at $x = 120\,\mu$m.

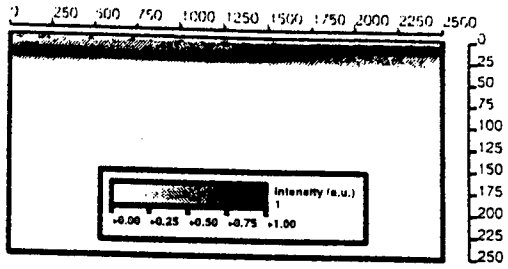


Figure 4: Intensity distribution in the interior of the device under test. The laser beam incides at $x = 20\,\mu$m.

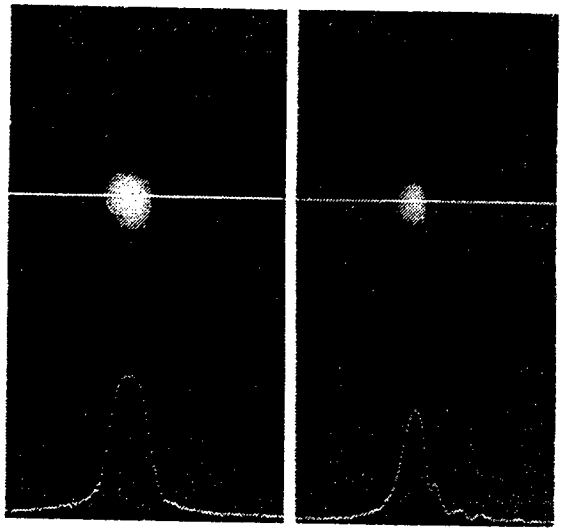


Figure 5: Intensity distribution at the rear surface of the device (image from IR camera) for beam position in the middle (left) and at the anode side (right) of the device.

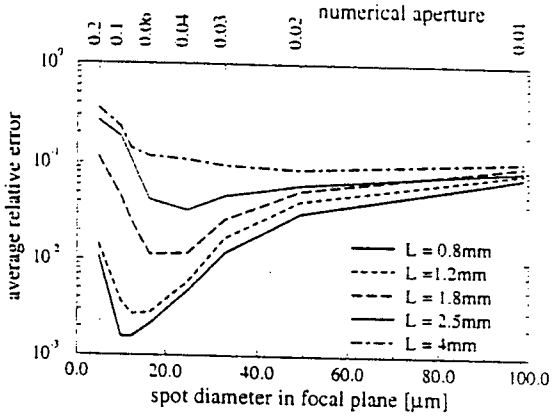


Figure 6: Deviation of the extracted carrier concentration (pin diode detector) from the carrier concentration obtained by device simulation

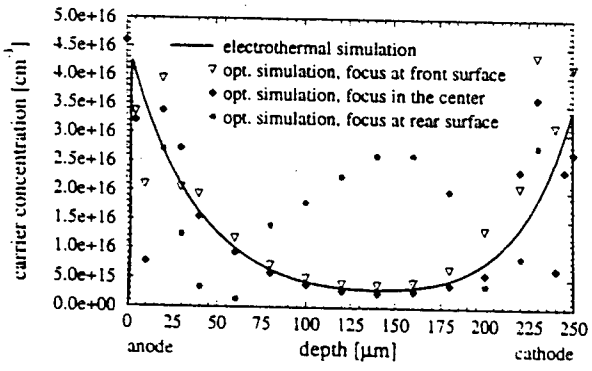


Figure 7: Carrier concentration extracted according to equation 1 (four-quadrant detector) in comparison with the carrier density obtained from device simulation

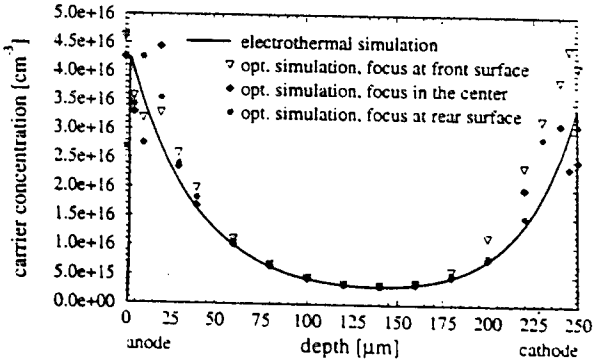


Figure 8: Carrier concentration extracted according to equation 1 (pin diode detector) in comparison with the carrier density obtained from device simulation

Student Paper

Nanoscale Characterization of Stresses in Semiconductor Devices

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By using transmission electron microscopy (TEM) and focused ion beam (FIB) technology in conjunction with an ensemble of computer programs which include finite element modeling, electron diffraction strain contrast simulation, and image manipulation we have been able to quantitatively measure stresses in semiconductor devices with a spatial resolution on the order of nanometers and a sensitivity on the order of tens of Mega Pascals. By utilizing this technique upon silicon germanium (SiGe) heterojunction bipolar transistors (HBTs), stress information on an extraordinarily high level of resolution and sensitivity can be deduced for structural components of the device. Examples provided in this presentation will include isolation trenches and collector contacts. This technique thus allows high sensitivity measurement of stresses in real devices.

The stress measurement process consists of first obtaining a sample through the HBT by FIB sputtering, which results in a thin cross sectional membrane of precisely known geometry. This geometrical information is critical for subsequent quantitative application of electron diffraction equations to the device stress field. An experimental image obtained via TEM is then used to build a finite element structure with ANSYS software (Figure 1). The finite element method (FEM) is then used to obtain a theoretical stress field throughout the HBT of the actual thin membrane structure (Figure 2: A), where the intrinsic stresses of polycrystalline and amorphous materials contained within the device structure were determined by wafer curvature measurements of uniform thin films. A program which simulates electron diffraction contrast (SIMCON[1]) from FEM stress field data by the application of the Howie-Whelan equations for dynamic electron diffraction is then used to create a simulated TEM image (Figure 2: B). The two images, experimental and simulated, are then normalized to each other such that their intensities and gray levels fall along the same dynamic range. Subtraction of one image from the other on a pixel by pixel basis can then be performed, which creates a difference map of changes in grayscale (Figure 3). The change in stress corresponding to a unit change in gray level can be determined by mapping the known stresses and gray levels of the simulated image onto the known gray levels of the experimental image in a region of close correlation as evidenced by the difference map. The theoretical stress field in the finite element model is then varied to determine the stress field which best fits the experimental data as determined by the difference map technique. The validity of the quantitative procedure is verified by examination of nodal stress values within the region of interest (Figure 4). Areas of higher stress within the device structure have been identified. These include single crystalline regions in close proximity to tungsten (W)

vias (due to the large intrinsic stress present in W—on the order of 1.2 GPa), material immediately adjacent to thin thermal SiO_2 layers, the strained SiGe epitaxial base, and oxide trenches. The stresses under several different collector contact geometries have been studied and application to the SiGe base structure is currently being explored.

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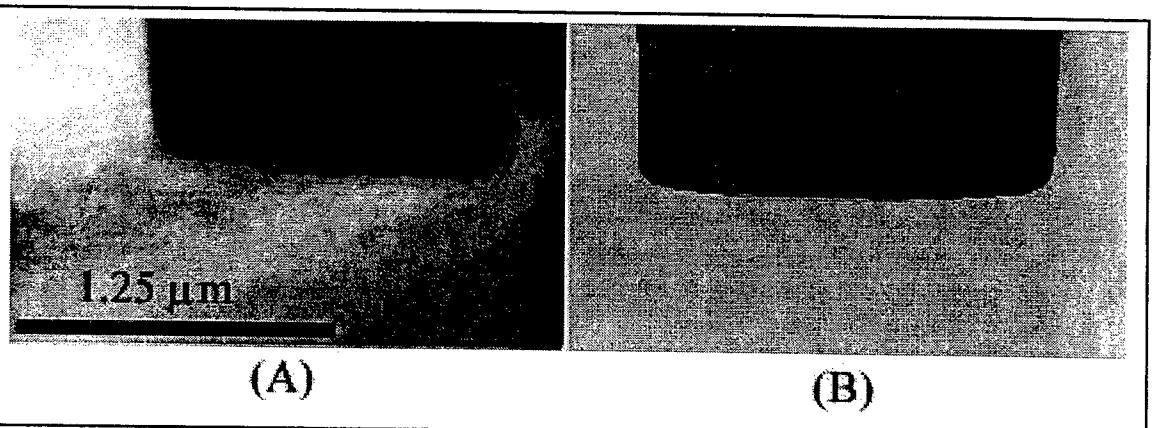


Figure 1: TEM Image (recorded with a g = (400) diffraction vector) (A) and simplified FEM Model (B) ***Note: Images not at exactly the same scale***

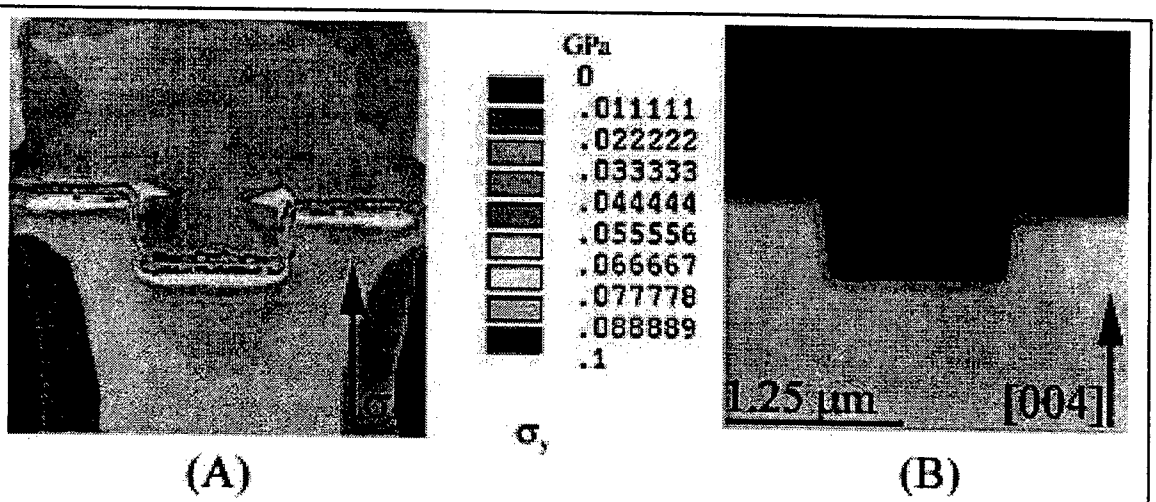


Figure 2: FEM Stress Plot (A) and g = (400) SIMCON Simulated Image (B) *Note: Images not exactly at the same scale*

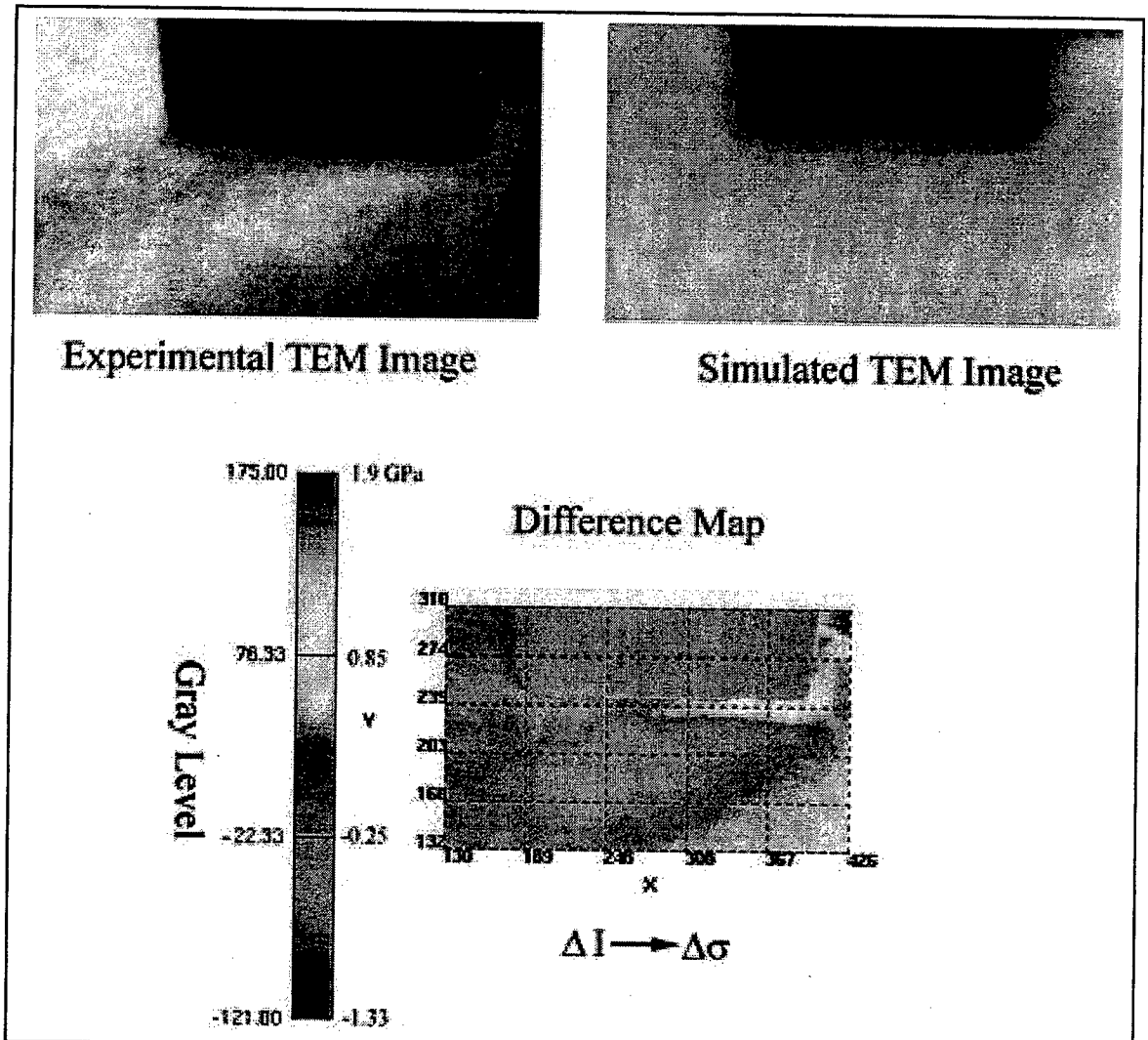


Figure 3: TEM, SIMCON (both with g = 400), and Difference Map Images

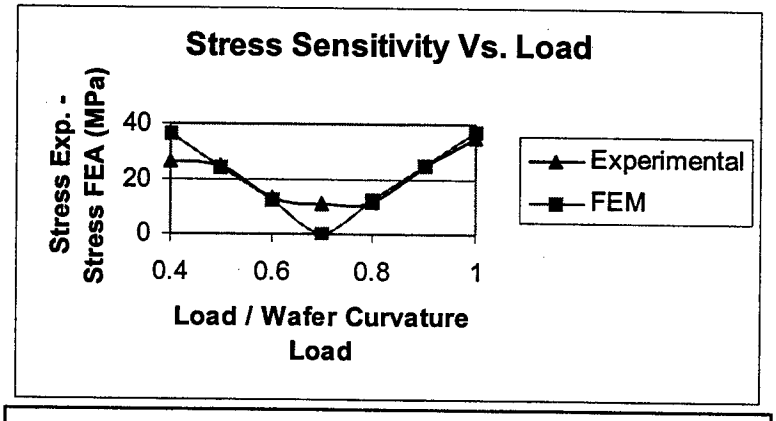


Figure 4: Variation of FEM Stress Field

Temperature dependence of carrier recombination lifetimes in n-type silicon

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I. INTRODUCTION

The carrier lifetime is one of the most important parameters determining the electrical characteristics of semiconductor devices. Furthermore, lifetime mapping of the starting material and test wafers provides a powerful tool for controlling the defect and impurity concentration during wafer processing. Therefore, diverse techniques for lifetime measurements have been developed in the past (for an overview see, e.g. [1]). At present, irradiation by electrons or ions or the diffusion of metal impurities such as Pt or Au are the most commonly used methods to control the carrier lifetime and much effort has been spent on characterizing the corresponding defect and impurity levels. However, in many applications semiconductor devices are operated under extremely different conditions: so, current densities in power devices range from 10^{-5} A/cm^2 in the blocking mode up to 400 A/cm^2 under surge current conditions. Moreover, the devices are operated at temperatures ranging from –30 °C to 180 °C. With a view to meeting the requirements of automobile industry, power electronics should work even at temperatures as high as 200 °C. On the other hand, there is also a strong interest in applications operating at low temperatures down to about –200 °C, as, for example, in the realization of superconducting magnetic energy storages. Therefore, an understanding of the dependence of the carrier lifetime on both the injection level and the temperature is very important. Although some work on the temperature and injection dependence of carrier lifetime on as-grown silicon wafers [2], on wafers doped with metal impurities (e.g. [3-7]) and on irradiated silicon (e.g. [8-10]) has been done, the characterization and understanding of the lifetime dependence is still incomplete. Therefore, in this work we present injection and temperature dependent microwave photoconductivity decay (μPCD) measurements on Pt, Au and Fe-doped n-type silicon wafers. While the doping with Pt and Au is important for controlled lifetime adjustment, Fe-doped samples have been analyzed, because Fe is one of the most undesired contamination elements.

II. EXPERIMENTAL DETAILS

The investigated samples are FZ grown silicon wafers. They are doped with metal impurities during crystal growth. The specific resistivity and geometrical data of the samples are listed in Table 1.

For the μPCD measurements a 200 ns light pulse from a laser diode with a wavelength λ = 904 nm was used. The penetration depth at room temperature is about 30 μm. The focussed spot diameter on the sample surface is about 1 mm^2 and the laser power was adjusted to a level, that the injected carrier density is of the order of 5×10^{15} cm^{-3} for

the temperature-dependent measurements. Since the impurity concentrations in all samples are relatively large, small carrier lifetimes are expected. Therefore, no special surface passivation has been performed. Details of the measurement set-up can be found in [11].

III. RESULTS AND DISCUSSION

The measured lifetime dependence on the injection level at 300 K is qualitatively similar for the Pt, Au and Fe doped samples: For excess carrier concentrations in the interval of 10^{13} to 5×10^{15} cm^{-3} we observe a monotonous increase of the lifetime with increasing injection level in all three samples. As an example, the lifetime dependence for the Pt-doped sample is shown in Fig. 1. In addition, calculated Shockley-Read-Hall (SRH) lifetimes based on three independent recombination centers are shown. The trap parameters of the investigated centers are listed in Table 2. Equal donor and acceptor concentration have been assumed, while the concentration ratio of acceptor to mid-gap centers was assumed to be 6:1 [7]. From the calculated curves, it is obvious that the lifetime is mostly determined by the acceptor-like center. Since the specific resistance of the Pt-sample is 7.8 Ωcm, the Fermi level E_F is close to the acceptor level $E_A=E_C$-0.24 eV at 300 K. For this reason, the calculated slope of the lifetime-curve for the acceptor level depends sensitively on the capture cross-sections of the acceptor-like center. Furthermore, it is obvious from Fig. 1, that the donor-like center and the mid-gap center are of minor importance for the total lifetime in the injection interval under consideration.

The temperature dependence of the lifetime for an excess carrier concentration of about 5×10^{15} cm^{-3} is displayed in Fig. 2. At temperatures between 50 K and 240 K the lifetime is almost constant, whereas in the temperature interval between 240 K and 470 K a monotonous increase of the lifetime with temperature is measured. This is in accordance with earlier measurements by Miller et al. [12], although these were performed under low injection conditions. Miller et al explained this dependence by taking into account one temperature-dependent hole capture cross-section, namely the Pt acceptor level in n-doped material. Analyzing the contributions of the three recombination centers we find that, indeed, the lifetime in the lower temperature range is actually determined by the acceptor level. However, at temperatures above 350 K, it is increasingly affected by the other two centers resulting in a weaker increase of the total lifetime at higher temperatures.

The measured and calculated lifetimes for the Au-doped n-type silicon wafer are plotted in Fig. 3 as a function of temperature. It is commonly accepted, that the Au-doped samples are characterized by a mid-gap acceptor-like center with an energy level at E_C-0.55 eV and a donor-like recombination center at E_V+0.35 eV. From the calculated SRH-lifetimes, we recognize that the lifetime in the low-temperature range is dominated by the donor, whereas at temperatures above 400 K the acceptor level is dominant.

In contrast to this, the total lifetime in the Fe-doped sample decreases with increasing temperature, as shown in Fig. 4. The strong lifetime decrease with temperature can be reproduced by the simple SRH-model, when a temperature dependence of the hole capture cross section $\sigma_p \sim \exp(-0.048\text{eV}/kT)$ is assumed for the interstitial donor-like Fe-center at E_V+0.38 eV. Such a dependence has been determined in Fe-doped p-type silicon [13]. The low temperature behavior can be described, when we assume the existence of a mid-gap center with an energy level at about E_C-0.48 eV. This is in

agreement with other measurements [e.g. 14] and the fact, that iron acts as effective generation center. However, it is worth to mention, that there is experimental evidence that the concentration of this mid-gap level decreases strongly, when Fe-doped n-type samples are annealed at temperatures of about 500 K [14]. Therefore, additional studies are in progress to confirm these preliminary results.

IV. SUMMARY

We investigated the injection and temperature dependence of the carrier recombination lifetime for Pt-, Au-, and Fe-doped n-type silicon wafers by microwave reflectance photoconductance decay in a temperature interval from 50 to 475 K. All samples show a characteristic lifetime variation in a certain temperature range. In particular, in the temperature interval between 250 and 450 K the lifetime increases monotonously in the Pt- and Au-doped samples, while it decreases in the Fe-doped sample. By comparing the experimental results with Shockley-Read-Hall lifetime calculations for independent recombination levels, it could be decided which are most relevant recombination centers in the individual temperature ranges. Finally, we point out that the μPCD provides a powerful tool for non-contact characterization of the injection and temperature dependence of carrier lifetime.

ACKNOWLEDGEMENT

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type	resistivity [Ωcm]	impurity material	width [μm]
FZ, n	7.8	Pt	900
FZ, n	12.7	Au	1000
FZ, n	18.1	Fe	1000

Table 1: Sample parameters

impurity		energy level	electron capture cross section σ_n [cm^{-2}]	hole capture cross section σ_p [cm^{-2}]
Pt	acceptor	$E_C - 0.24$ eV	4×10^{-15}	$4 \times 10^{-14}\ (T/300)^{-1.5}$
	donor	$E_V + 0.36$ eV	1×10^{-14}	1.1×10^{-16}
	mid-gap	$E_C - 0.52$ eV	3.2×10^{-15}	6.5×10^{-15}
Au	acceptor	$E_C - 0.55$ eV	1×10^{-16}	$1 \times 10^{-14}\ (T/300)^{-1.3}$
	donor	$E_V + 0.35$ eV	$3.05 \times 10^{-16}\ (T/300)^{-1}$	4×10^{-15}
Fe	mid-gap	$E_C - 0.48$ eV	5×10^{-15}	$1 \times 10^{-15}\ (T/300)^{-1}$
	donor	$E_V + 0.38$ eV	2.6×10^{-14}	$5.6 \times 10^{-16}\ \exp(-0.048\text{eV}/kT)$

Table 2: Trap parameters used for SRH-calculations

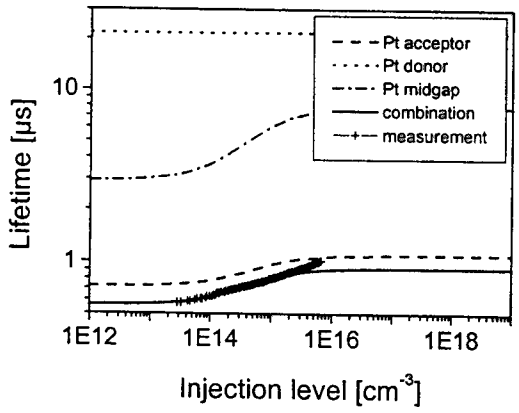


Fig.1: Lifetime vs. injection level for the Pt-doped n-type sample

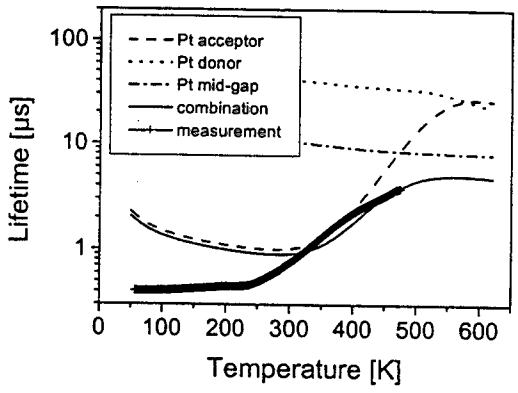


Fig.2: Lifetime vs. temperature for the Pt-doped n-type sample

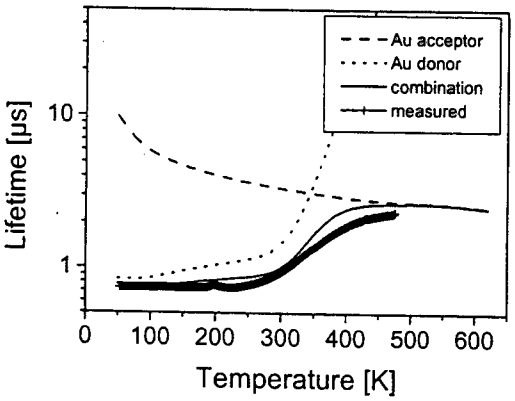


Fig.3: Lifetime vs. temperature for the Au-doped n-type sample

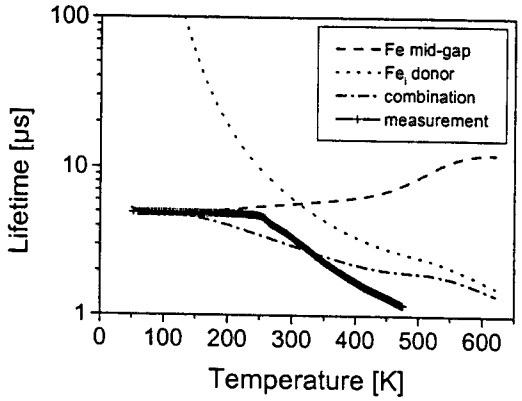


Fig.4: Lifetime vs. temperature for the Fe-doped n-type sample

The Growth of Giant Magnetoresistance Films on Silicon Substrates: Opportunities, Challenges, and Impediments

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One of the most promising opportunities in the rapidly emerging field of "Spintronics" is the integration of ultrathin magnetic films on Si substrates for the direct injection of spin-polarized electrons into Si.[1,2] One of the most interesting combinations would involve so-called giant magnetoresistance (GMR) spin valves. GMR spin valves have the property of changing their resistivity in response to the presence of a magnetic field, and are termed spin valves since their magnetic state acts as a valve controlling electron flow.[2] This property makes them suitable as magnetic field sensors,[3,4] and they are presently of great technological importance as the read-head in hard-disk drives. Another important application of GMR spin valves is as the memory element in magnetoresistive random access memory chips (MRAM).[3] MRAM chips hold great potential as non-volatile memory since a spin valve can be designed to have stable states of high and low resistivity.

Present applications of GMR spin valves utilize an electrical circuit to measure the resistivity of the film. However, it would be of great interest if the GMR spin valve could be integrated into the Si at the gate of a transistor, greatly shrinking the device size and increasing the operating speed. Attempts have been made to produce such a "spin-valve transistor."[5,6] These devices utilize a Schottky barriers and hot (1 eV) electrons to achieve modest values of gain. However, in such devices only a tiny fraction ($\sim 10^{-4}$) of the injected electrons actually get into the Si. The rest are lost to inelastic scattering in the magnetic metal. It is difficult to envision practical spintronic devices that suffer such high losses.

A possible alternative would be to inject electrons from the Fermi level (E_f) of a GMR spin valve directly into the conduction band of Si. In the present work, we have begun to investigate this alternative and to identify the impediments that will constitute the challenges in making this alternative a successful technology.

In principle, it should be possible to achieve very large injected currents that change with the magnetic state of the GMR spin valve. The key is to make the Schottky barrier negligibly small. It appears from our work that "negligibly small" will be something significantly smaller than what is commonly referred to as an ohmic contact to Si. We have found that so-called ohmic contacts in fact have small but non-negligible Schottky barriers. At room temperature, thermally excited electrons can yield an I-V

curve that appears quite linear, yet conceal a Schottky barrier on the order of 0.2 eV (measured at 77 K).

We have found that even a barrier of 0.2 eV appears to cause a complete loss of sensitivity to the magnetic state of the GMR spin valve. Apparently, the process of thermal excitation of an electron to allow it to overcome the Schottky barrier involves many electron-phonon inelastic scattering events and causes the electron spin state to be randomized. Consequently, the current actually injected into the Si has no dependence on the magnetic state of the GMR spin valve.

It is well-known from so-called "current perpendicular-to-the-plane" or CPP-GMR measurements that the current flowing at E_f in a GMR spin valve is strongly dependent on its magnetic state[7] even if, as it seems, the current 0.2 eV above the E_f is not. Thus, a major challenge for this field will be to reduce the Schottky barrier to the order of the Fermi-Dirac distribution function, or ~0.025 eV.

In principle, fine tuning of a Schottky barrier height is merely a matter of fine tuning the interface electrostatic dipole, and with the wide variety of metals and alloys available and the many processing methods that can be employed, such small Schottky barriers should certainly be possible. However, a major caveat is in order here. It is not an easy matter to find suitable substrates for GMR spin valves. Many of the approaches that will yield suitably small Schottky barriers will probably turn out to be very poor substrates for GMR spin valves.

In our work, we have found that Si is not a substrate that readily yields high-quality GMR spin valves. The problem appears to be the interdiffusion of Si and Co or NiFe, which typically constitute the first layer of a spin valve. Seed layers such as 1 nm of Pt or Ta tend to suppress the interdiffusion between the Si and the spin-valve layers and yield spin valves of moderate quality. However, Pt and Ta seed layers produce unacceptably large Schottky barriers. Future research should concentrate on finding an interfacial layer between the spin valve and the Si that yields a very small Schottky barrier and which is very thin. Layers thicker than a few nm are unlikely to have high transmission probability for Fermi level electrons.

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CURRENT MODULATION IN SUPERCONDUCTING/MAGNETIC NANOSTRUCTURED MATERIALS

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1.INTRODUCTION.

Superconductors allow the fabrication of devices with exceedingly low losses and with unsurpassed speed. Up to now the development of active superconducting devices has been based almost entirely on Josephson junction technology. In the approach utilized here simpler and cheaper processing steps were implemented for fabrication of a new generation of superconducting materials. Our goal was fabrication and evaluation of prototype thin film superconductors containing square arrays of artificial centers (submicron holes or submicron magnetic dots) as basis for new generation of active superconducting devices.

The value of the critical current in superconductors is determined by the balance of Lorentz forces and pinning forces acting on the flux lines in the superconductor. Lorentz forces proportional to the current flow tend to drive the flux lines into motion, which dissipates energy and destroys the zero resistance state. Pinning forces created by isolated defects in the microstructure oppose flux line motion and increase the critical current. Many kinds of artificial pinning centers have been proposed and developed to increase critical current performance, ranging from dispersal of small non-superconducting second phases to creation of defects by proton, neutron or heavy ion irradiation. In all of these methods, the pinning centers are randomly distributed over the superconducting material, causing them to operate well below their maximum efficiency. We have overcome this drawback by creating pinning centers in a periodic lattice [1-3]. Up to now, only electron beam lithography (EBL) has been employed to perform this task. The main drawback to EBL is that it is too slow and expensive to pattern areas large enough necessary for useful sample fabrication. An efficient novel fabrication technique for the production of superconducting thin films containing a periodic array of pinning sites in the form of sub-micron holes and magnetic dots was developed and successfully implemented. This technique was based on laser interferometric lithography [4-6]. It allows for the fast production of large area samples without the need of joining individually written blocks as is necessary in electron beam lithography. We applied this technique for the fabrication of vanadium and niobium thin films containing a periodic lattices of artificial pinning centers (APC) with period of 1 – 2 μm and diameter of 0.1 - 0.4 μm. Tailoring the type (magnetic dots or antidots/holes), size of the pin sites, the period and symmetry of the pinning lattice enables new control of the critical current for fabrication of a series of prototype of active thin film superconducting devices containing square arrays of APC.

2. SAMPLE FABRICATION.

A process for device fabrication requiring 3 different masks and 3 layers of deposition-(Nb, Al and Au) was developed. An extra layer (Fe or Ni) is required if arrays of submicron dots are used as APC. Using e-beam evaporation or magnetron sputtering a superconducting (vanadium or niobium) film is deposited onto the array of photoresist pillars, in this case a 1μm x 1μm square array with 0.3μm pillar diameter. A film containing the square array of holes was obtained after lift-off. This film was patterned

into a bridge using standard optical lithography and wet chemical or reactive ion (SF_6) etching. An insulating 20Å AlO layer was deposited by e-beam evaporation and patterned using optical lithography. Photoresist was patterned and after deposition and lift-off an Au control line was deposited on the top. Au wires were attached using silver epoxy and postbaking. DC and AC transport characteristics as well as the magnetization were measured on devices such as shown in Fig1.

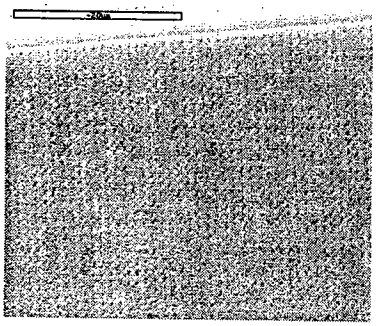


Fig.1a. 50μm wide 1000Å thick Nb-bridge with square ($1x1\mu m^2$) lattice of sub-micron holes

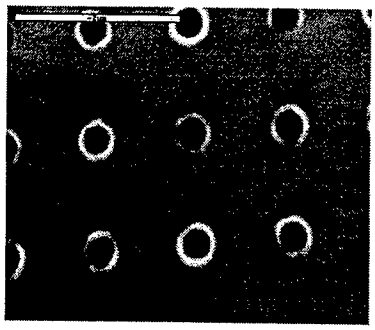


Fig.1b. Hole diameter d = 0.35μm

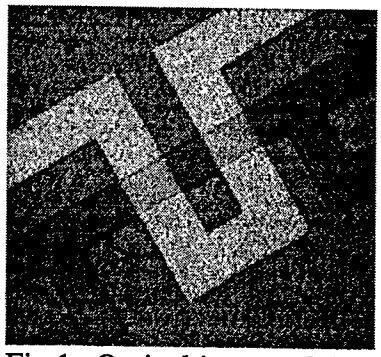
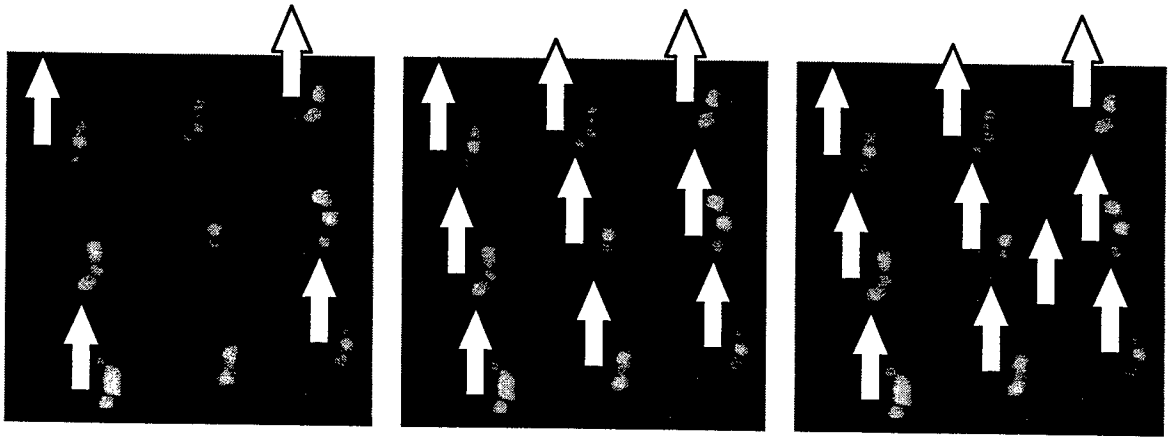


Fig.1c.Optical image of the active area of device. Au-control line on the top of Nb bridge is separated by underlying 20Å AlO insulating layer.



(a) (b) (c)

Fig.2. AFM image of 1500Å V film with square lattice of holes. Arrows schematically indicates vortices pinned by holes. (a) For $H < H_1$ the number of vortices is less than the number of holes; (b) For $H = H_1$ the number of vortices is equal to the number of holes; (c) For $H > H_1$ an extra interstitial vortex is shown in the interstitial region between the pinning sites.

3.EXPERIMENTAL RESULTS

The unique properties of nanostructured superconducting films are based on a commensurability effect between the pinning centers and the flux lines themselves (Fig. 2). The distance between flux lines $a_v \propto (\Phi_0/H)^{1/2}$ is a function of external magnetic field. The higher the magnetic field, the smaller the distance between vortices. At a well defined matching field $H_m = \Phi_0/d^2$, where a_v=d is the distance between pins (Fig. 2b), every vortex is strongly pinned in a pinning site, giving rise to high values of the critical

current (Fig.3). For H< H_m (Fig. 2a) the number of the vortices is smaller than the number of the pinning sites and the vortices can jump from one site to another, thus leading to the dissipation and suppression of the critical current; c) For H> H_m (Fig. 2c) all pinning sites are filled and any additional field will create weakly pinned vortices which reside in the interstitial region between the pinning sites. These interstitial vortices move easily in response to an electric current causing a precipitous drop in critical current (Fig.3). The very steep slope of the I_c-H curve is ideally suited for the construction of a new generation of amplifiers as indicated schematically in Fig.3 and of switches and logic circuits with a performance comparable to that of conventional flux flow transistors.

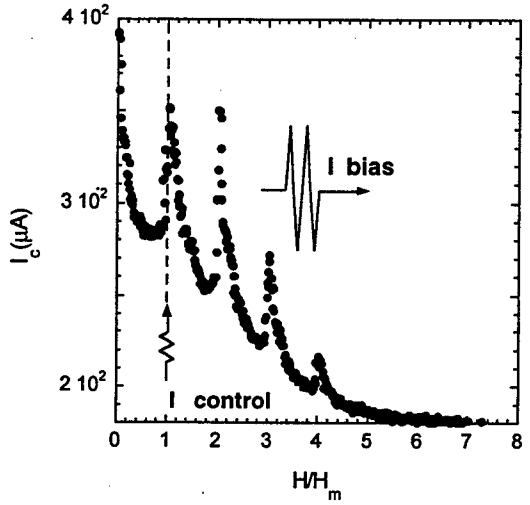


Fig. 3a. Field dependence of the critical current (threshold level 0.2μm) in Nb-superconducting device shown in Fig.1. The mechanism of current amplification is shown schematically

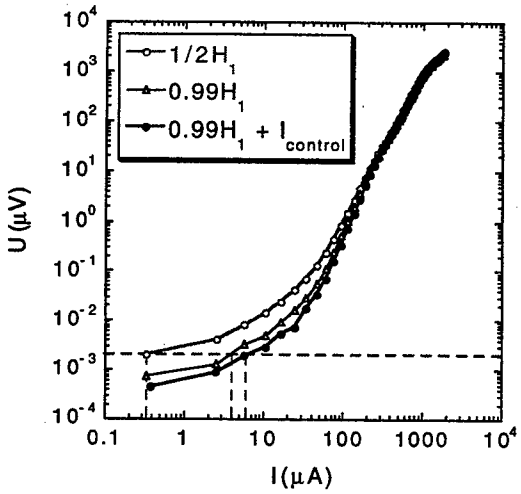


Fig.3b. IV characteristics of Nb-device shown in Fig.1. For working point H= $0.99H_1$ on I_c(H) curve (Fig.3a) the shift of IV to higher critical current values by $I_{control}$ =1mA for low voltages (< 0.1μm) is clearly observed.

By creating the lattice of holes in superconducting film we obtained the critical current amplification *more than 20 times* in comparison with unpatterned film and current modulation $j_c(H_1)/j_c(1/2H_1)$ more than an order of magnitude for low voltages in Nb-film with APC, however, to get essential current gain ($I_{bias}/I_{control}$ >>1) the optimization of the device geometry (width and thickness of superconducting film, shape of the control line), material choice (Nb/Al or MoGe/Ge multilayers) and better coupling of magnetic field of control line with underlying superconducting film with APC are necessary.

Current research focuses on fabrication, testing and optimization of the nanoscale periodic structures in hybrid magnetic (Fe, Ni, permalloy, with in plane magnetization (see Fig.4) and [Co4/Pt10]5 with out of plane magnetization) and superconducting (V, Nb) materials which enable new methods for the control of the critical current of superconductors and possible implementation of the laser interferometric lithography for magnetic storage applications.

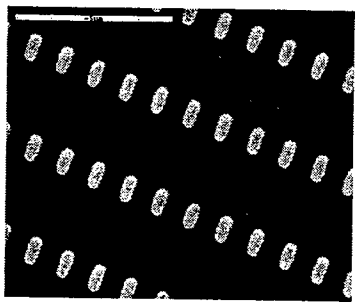


Fig. 4a Rectangular array of independent Ni dots.

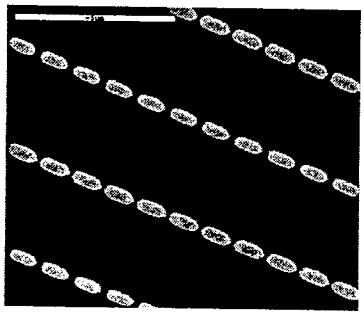


Fig. 4b Chains of strongly interacting Ni dots. The dot size and period are the same as in (a), but the dots are rotated 90°.

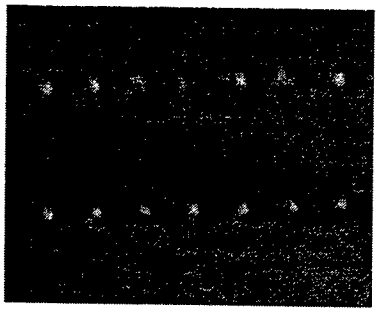


Fig 4c MFM image of chains shown in (b). The single domain state is stabilized by collective interaction among dots.

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Modeling the Electrical Behavior of Ferroelectric $SrBi_2(Ta_{(1-x)}Nb_x)_2O_9$ Capacitors Using the Distribution Function Integral Method (DFIM)

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I. INTRODUCTION

In recent years there have been numerous publications that propose memory cell architectures using ferroelectric devices. The reason for this is that such devices are best suited for non volatile data storage since they combine fast access time and virtually unlimited read/write cycles. Circuit designers therefore have a strong demand for compact models of ferroelectric devices, which can be used in circuit simulators and which give an accurate prediction of the electrical behavior of the devices. Another important requirement on compact models, however, is that they can be adapted to a wide range of devices with different electrical properties by varying a limited number of model parameters. In this work we demonstrate a ferroelectric capacitor model based on the DFIM approach [1]. Different types of $SrBi_2(Ta_{(1-x)}Nb_x)_2O_9$ capacitors with different electrical properties have been simulated and the results have been compared with measurements to show the suitability of the method for circuit simulation. To complete the work a method for extracting model parameters from measured hysteresis curves is described.

II. MODELING THE HYSTERESIS

The ferroelectric effect is based on the phenomenon that a Perovscite type crystal can be polarized by applying a voltage and that this polarization remains after the voltage is removed as shown in fig.1. According to the physical based Preisach model [2], a macroscopic system with a large number of dipoles can be mathematically described by a number of rectangular hysteresis loops whose coercive voltages u_+ and u_- are distributed statistically. Assuming a distribution function $d(u_+ , u_-)$ of the coercive voltages as shown in fig. 2, the total polarization of a ferroelectric material is then given by [1]

$$P(t) = -P_{sat} + P_{lin} + 2P_{sat}\iint_{g(t)} d(u_+,u_-)\,du_+\,du_- \quad , \qquad (1)$$

where the time dependent boundary $g(t)$ of the integral in equation (1) is determined by the values of the so far applied voltage $V(t)$. P_{lin} is the linear contribution to the polarization and P_{sat} is the saturated value of the polarization as shown in fig 3. The correct description of the polarization $P(t)$ for arbitrary input voltages $V(t)$ is the main difficulty towards modeling ferroelectric devices. So far published models either use simple mathematical functions to approximate the shape of the hysteresis curve [3,4] or they use subcircuit models to describe the complex relation between charge and voltage [5,6]. Both methods however are not sufficient to model the hysteresis curve over a great range of operation particularly for small voltages. On the other hand numerical approaches can be found, which yield accurate results but which are not useful for circuit simulation due to long simulation time.

A. The DFIM model

To overcome these problems, the DFIM approach has been developed which can be derived in three steps. First, we need to recognize that the area, in which the distribution function $d(u_+ , u_-)$ has to be integrated, can always be assembled by a number of rectangles as shown in fig. 4. This

is valid for arbitrary input voltages $V(t)$. Second, we define a function $A(u'_+, u'_-)$ for each coordinate in the u_+ - u_- plane

$$A(u'_+,u'_-)=\int_{-\infty}^{u'_-}\int_{-\infty}^{u'_+} d(u_+,u_-)\,du_+du_- \ , \tag{2}$$

which represents the integral of the distribution function within the boundaries $-1<u_+<u'_+$ and $-1<u_-<u'_-$, indicated by the dark gray area in fig. 4. Third, we approximate this integral by a two dimensional function

$$A(u_+, u_-) = \{\arctan[\sigma_1 (u_+ - u_1)] + \pi/2\}\ \{\arctan[\sigma_2 (u_- - u_2)] + \pi/2\} / \pi^2 \ , \tag{3}$$

as shown in fig. 5 in order to avoid time consuming numerical integration. Evaluating the integral in equation (1) can then be performed by evaluating equation (3) at coordinates determined by the values of the so far applied voltage $V(t)$.

B. Determination of the model parameters

The used model has six parameters as listed in table 1. The dielectric constant ε_r can be derived from the slope of the *P-V* curve in saturation. P_{sat} denotes the saturated value of the polarization which is deducted from the saturated part of the hysteresis curve by subtracting the linear contribution $P_{lin}(t) = \varepsilon_0\varepsilon_r V(t)/d_{Fe}$. The coercive voltages $u_{1,(2)}$ are determined by $P(u_{1,(2)}) = 0$ and $\sigma_{1,(2)}$ can be calculated by analyzing a saturated loop which is equivalent to setting one of the arctan functions to $\pi/2$. Solving the resulting equation for $\sigma_{1,(2)}$ yields

$$\sigma_{1,(2)} = \frac{1}{u_{1,(2)}} \tan\left(\frac{\pi}{2}\frac{P_{rem}}{P_{sat}}\right). \tag{4}$$

III. MEASUREMENTS AND RESULTS

In this paper we have applied the DFIM approach to different types of ferroelectric capacitors. We used $SrBi_2Ta_2O_9$ (SBT) as well as $SrBi_2(Ta_{(1-x)}Nb_x)_2O_9$ with $x = 0.28$ (SBTN) and a thickness of the ferroelectric layer of d_{Fe} = 192nm and d_{Fe} = 180nm, respectively. Due to different physical properties of the materials the hysteresis curves of undoped SBT differs from that of niobium doped SBT (SBTN). In particular, SBTN has a larger value of the remnant polarization which results in larger output signals in memory applications. SBT, on the other hand, has lower coercive voltages, which makes it suitable for low voltage designs. To set up the simulation we have extracted the model parameters for the two capacitors from measured curves as described above.

The measurements have been performed using a Sawyer Tower circuit and a Radiant test system, respectively. The first set of measurements (figs. 6-8) shows *P-V* curves with saturated and sub loops of the SBT capacitor for different input voltages. Figures 9 to 11 show measured and simulated curves of the SBTN capacitor for different amplitudes of the applied voltage $V(t)$. In both cases the simulated curves are in good agreement with the measured curves for saturated as well as sub loops and for different amplitudes of the input signal.

IV. SUMMARY

The distribution function integral method has been used to simulate different types of ferroelectric capacitors (SBT and SBTN). The simulation results are in good agreement with the measured curves for both saturated and sub loops and different types of ferroelectric material over a wide range of operation. Due to the simple algorithm of the approach, the model is best suited for use in circuit simulators. There are only a few model parameters that can easily be determined by extracting values from measured hysteresis loops. The model has been implemented in the Saber circuit simulator. The results show the flexibility and accuracy of the DFIM approach and its usefulness not only for circuit design but also for device optimization.

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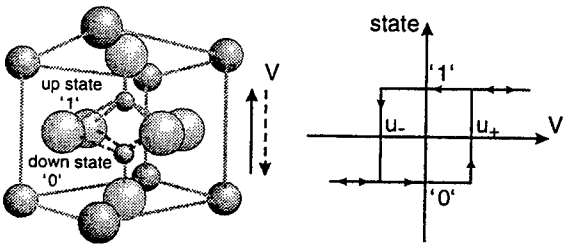


Fig. 1 Depending on the applied voltage, a Perovscite type crystal can take on two stable states *'1'* (-) and *'0'* (- -) that remain after the voltage is removed.

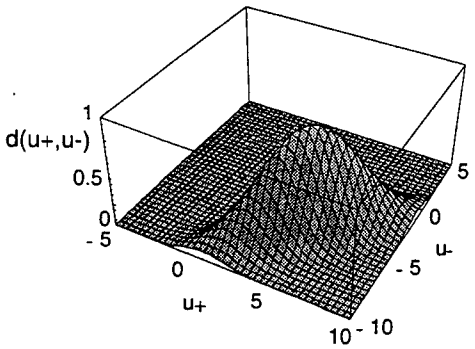


Fig. 2 Typical distribution function $d(u_+, u_-)$ of the coercive voltages u_+ and u_- of a ferroelectric material.

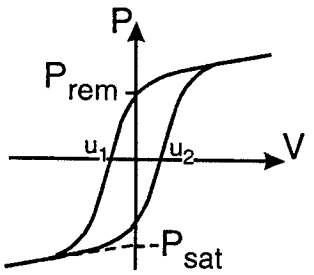


Fig. 3 Hysteresis loop of a ferroelectric capacitor. u_1, u_2: coercive voltages, P_{rem}: remnant polarization, P_{sat}: saturated polarization.

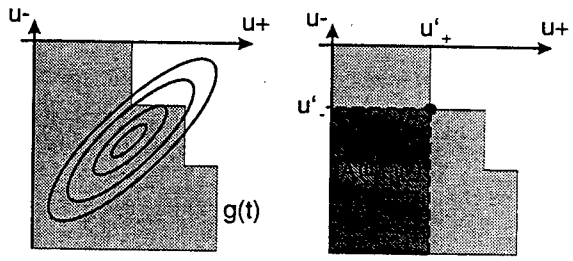


Fig. 4 Contour plot of the distribution function $d(u_+, u_-)$. The function $g(t)$ forms the boundary of the integration area (left figure). $A(u'_+, u'_-)$ is the integral of $d(u_+, u_-)$ within a rectangle (dark gray in right figure).

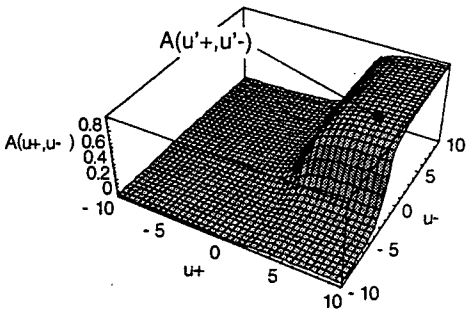


Fig. 5 Two dimensional plot of $A(u_+, u_-)$ given by equation (3). The value at the coordinates (u'_+, u'_-) approximates the integral of the distribution function within the dark gray rectangle in fig. 4.

Table 1 Model parameters used for the simulation

Parameter	SBT	SBTN
ε_r	250	225
P_{sat}	10.68 µC/cm²	14.56 µC/cm²
P_{rem}	8.0 µC/cm²	12.9 µC/cm²
u_1	0.56 V	1.07 V
u_2	-0.67 V	-1.07 V
d_{Fe}	192 nm	180 nm

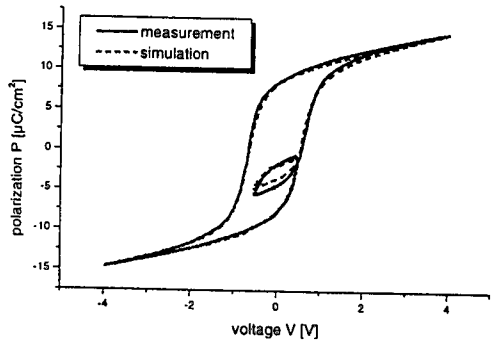


Fig. 6 Measured (-) and simulated (- -) hysteresis curves $P(V)$ of a ferroelectric capacitor (SBT) including a sub loop at the ascending branch.

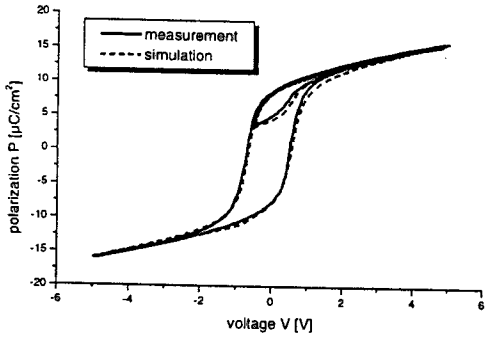


Fig. 7 Measured (-) and simulated (- -) hysteresis curves $P(V)$ of a ferroelectric capacitor (SBT) including a sub loop at the descending branch.

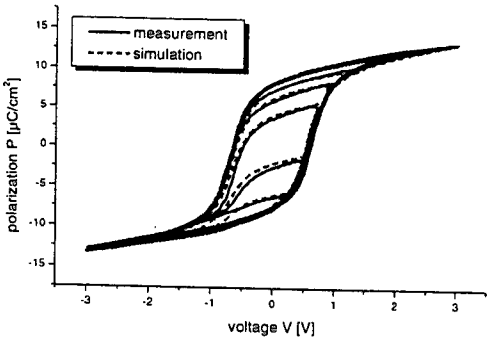


Fig. 8 Measured (-) and simulated (- -) hysteresis curves $P(V)$ of a ferroelectric capacitor (SBT) including several sub loops.

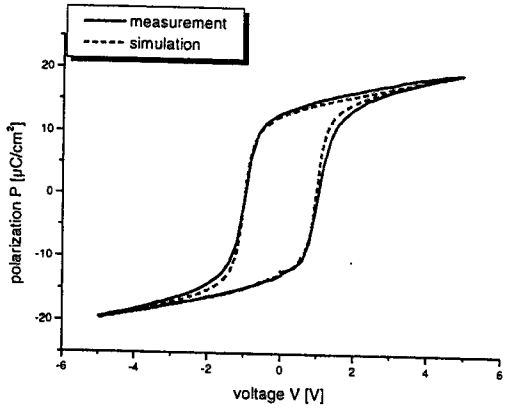


Fig. 9 Measured (-) and simulated (- -) hystereseis curve, SBTN, $|V_{max}| = 5V$.

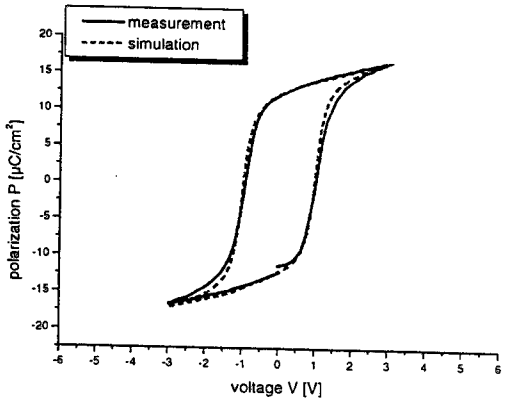


Fig. 10 Measured (-) and simulated (- -) hystereseis curve, SBTN, $|V_{max}| = 3V$.

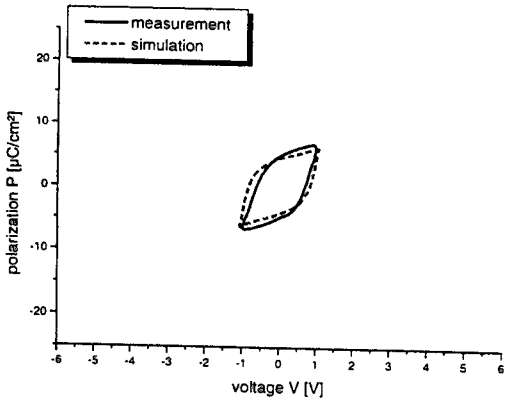


Fig. 11 Measured (-) and simulated (- -) hystereseis curve, SBTN, $|V_{max}| = 1V$.

Simulated Spectral Response of NSN Single Electron Transistor (SET)

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I. INTRODUCTION

The present-day goals of astronomy require detectors capable of a variety of spectral resolutions and highest possible sensitivity. In the visible/IR range one can use the natural energy level structure of semiconductors to produce sensitive photoconductive detectors. However, the smallest energy level splittings which can be used in semiconductors determine a maximum wavelength for semiconductor photon detectors of about 300 μm. At millimeter wave frequencies, the most sensitive broadband (low spectral resolution) detectors are of the bulk type, i.e. bolometers. It is of interest to investigate if photon type detectors are feasible in this wavelength range as well. The SIS detector is such a device and has demonstrated heterodyne (high spectral resolution) noise temperature characteristics very close to the quantum noise limit (hf/2k). A two-junction quantum tunneling system, the Single Electron Transistor (SET), has been studied in the last few years [1][2][3]. FIG.1 illustrates the SET configuration. Photons can interact with the energy levels of the SET system through Photon-Assisted Tunneling (PAT) and therefore SETs have potential applications as both intermediate spectral resolution and broadband detectors. The SET energy level separations correspond to millimeter wavelengths and the quantum-mechanical effect of Coulomb Blockade minimizes the dark current and thus the noise level of the SET as a detector. A limited number of investigations of PAT in SETs have been reported [4][5]. This paper presents results of simulated response of the NSN (Normal-Superconductor(Al)-Normal) SET to monochromatic radiation.

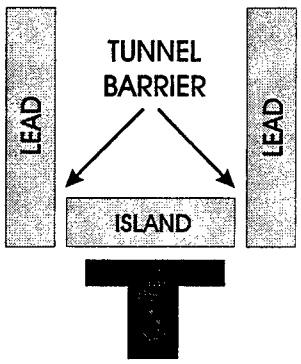


FIG. 1. SET device configuration.

II. SIMULATION THEORY

A kinetic simulator for a two junction NSN SET was developed. It is an extension of a previously developed simulator [6] which models the island charge state transition rates (ignoring co-tunneling and other second order processes) and solving a master equation for the island charge state occupation probabilities. These probabilities, along with the calculated transition rates, are then used to compute the current, which consists of single electron tunneling and Andreev Reflection, through the device.

In the presence of photons, the rate for single electron tunneling in the NSN system can be written as a convolution of the rate for tunneling in a dark device $\Gamma_0(\Delta E)$ with a function P(E'), the probability that the electromagnetic environment will contribute an energy E' to a tunneling process [7], as follows:

$$\Gamma_{PAT}(\Delta E) = \int_{-\infty}^{\infty} \Gamma_o(\Delta E - E')P(E')dE' \qquad (1)$$

Here P(E') is related to the spectrum of voltage fluctuations $S_v(\omega)$ induced by the environment and is given by,

$$P(E') = \frac{1}{h}\int_{-\infty}^{\infty} \exp\left(\frac{2\pi i}{h}E't\right.$$

$$\left. + \frac{(2\pi)^2}{hR_K}\int_0^{\infty} \frac{S_V(\omega)}{\omega^2}(\cos(\omega t) - 1)d\omega\right) dt \qquad (2)$$

In previous analyses, the spectrum $S_v(\omega)$ has been given by a Planck-Nyquist distribution [6]. For monochromatic radiation $S_v(\omega) = R_K P_c \delta(\omega - \omega_o)$, where P_c is defined as the total power coupled to the device and available for absorption. For low values of P_c, the exponential of the integral over ω in Eq.(2) can be expanded in powers of $P_c/h\nu_o^2$ and P(E') to first order can be written as,

$$P(E') \cong (1-(\tfrac{P_c}{h\nu_o^2}))\delta(E') + \tfrac{1}{2}(\tfrac{P_c}{h\nu_o^2})(\delta(E'-h\nu_o) + \delta(E'+h\nu_o)) \quad (3)$$

From Eq.(1), the functional form of the photon assisted tunneling rate becomes,

$$\Gamma_{pat}(\Delta E) \cong (1-(\tfrac{P_c}{h\nu_o^2}))\Gamma_o(\Delta E) + \tfrac{1}{2}(\tfrac{P_c}{h\nu_o^2})[\Gamma_o(\Delta E - h\nu_o) + \Gamma_o(\Delta E + h\nu_o)] \quad (4)$$

The three terms present here represent a rate for tunneling without photon interaction, a rate for photon-assisted tunneling, and a rate for tunneling accompanied by photon emission. Henceforth processes represented by Eq.(4) will be referred to as PAT. Since Eq.(4) is expressed in terms of the tunneling rate Γ_o in the absence of photons, a modified version of the "dark" (no PAT) simulator of [6] can be utilized to simulate device kinetics in the presence of monochromatic radiation.

The rate for single electron tunneling in the absence of PAT as calculated by the UMass simulator on the MATLAB platform agrees well with the results from the simulator (written in C) and corresponding measurements described in [6].

III. Simulation Results

Spectral responses of NSN SETs were simulated for different cases of device configuration and power illumination. The spectral response at two ambient temperatures of 25 mK and 250 mK are presented in this paper. The low temperature results show features corresponding to mechanisms of charge transport in the presence of a strong Coulomb blockade. The high temperature simulation probes device photo-response at temperatures attainable with a simplified cryogenic system. A symmetric SET device configuration with junction resistance of 50 kΩ and a total capacitance of 800 aF was chosen.

"Sweeps" Through Photon Energy at T=25 mK

Source-drain currents versus photon energy for SET devices with gate charges (Q_g) of 0e and 1.0e were simulated for a device at ambient temperature of 25 mK. Three values of photon energy set the scale of features found in the plots: the charging energy $E_c = e^2/2C_\Sigma$ (=100 μeV corresponding to 24 GHz) where C_Σ is the total capacitance of the SET device, Δ, the superconducting gap energy (=2.45E_c), and W, the absolute value of the bias work done in moving charge through either junction (=0.63E_c). FIG. 2 shows the current as a function of photon energy for various P_c and Q_g= 0e. At a photon energy corresponding to Δ+E_c-W (≅ 282 μeV), there is a sharp rise in the current through the device as photons excite the island to the n=±1 degeneracy point, resulting in Andreev and PAT currents. For the higher power levels, the Andreev current remains at about the same level while the single charge current due to PAT processes determines the total current. As a consequence, the current drops sharply for the higher powers at photon energy $h\nu_o$=Δ+E_c+W (≅ 408 μeV) where it becomes probable for PAT processes to pass charge through the island *against* the bias voltage, re-

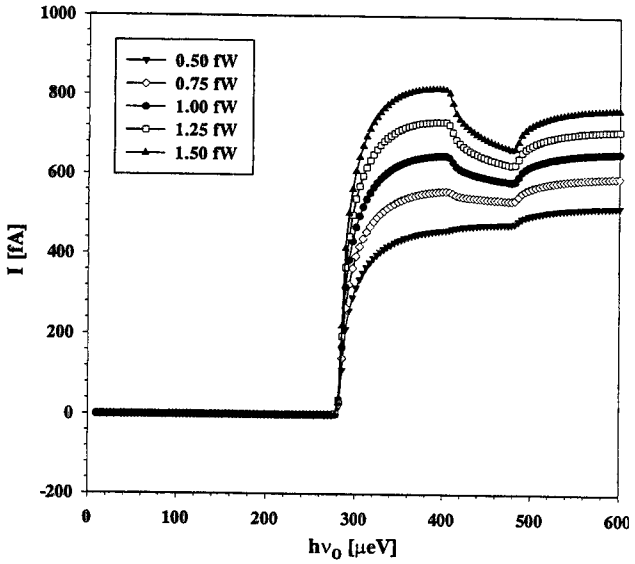


FIG. 2. Source-drain current vs. photon energy for various P_c with a gate charge of 0*e* and at an ambient temperature of 25 mK.

ducing the net PAT contribution to the current. When $h\nu_o \geq \Delta + 3E_c - W$ ($\cong 482$ μeV), transition cycles $n=1 \rightarrow n=2 \rightarrow n=1$ result in a current which is sensitive to the photon power.

FIG. 3 shows current as a function of photon energy for $Q_g = 1e$. For $h\nu_o < \Delta - E_c - W$ ($\cong$ 82 μeV), the current is about 800 fA while the island is energetically stable at the n=0/n=2 degeneracy point, where Andreev current transports charge through the system at high rates [6]. For $h\nu_o \geq \Delta - E_c - W$ ($\cong 82$ μeV), photon assisted "trapping" of quasiparticles takes place removing the island from the n=0/n=2 degeneracy point which blocks the Andreev cycle. This "trapping" mechanism is more effective for higher power levels. For $h\nu_o \geq \Delta - E_c + W$ ($\cong$ 208 μeV), the "trapping" process occurs both along and against the direction of the bias, reducing the net current. At $h\nu_o \geq \Delta + E_c - W$ ($\cong$ 282 μeV), the addition of quasiparticles returns the island to the n=0/n=2 degeneracy point and results in a sharp increase in current. This current is mostly Andreev reflection in the low power case and about equal parts Andreev reflection and PAT current for higher power. For $P_c = 0.5$ fW, the next feature is at $h\nu_o = \Delta + 3E_c - W$ ($\cong$ 482 μeV), where the channel $n=2 \rightarrow n=3$ opens and current due to cycles of $n=2 \rightarrow n=3 \rightarrow n=2$ in the direction of the bias increases. The simulations with P_c greater than 0.5 fW display a drop in net current relative to the levels just below $h\nu_o = \Delta + E_c + W$ ($\cong$ 408 μeV) since PAT against the bias becomes possible at this energy.

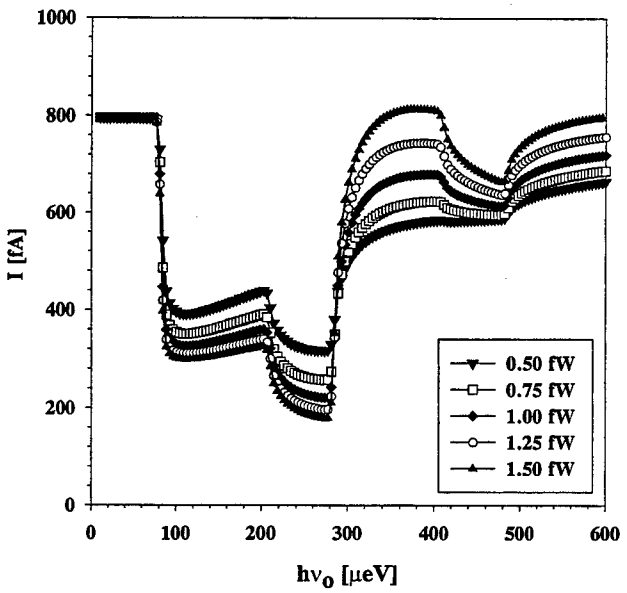


FIG. 3. Source-drain current vs. photon energy for various P_c with a gate charge of e and at an ambient temperature of 25 mK.

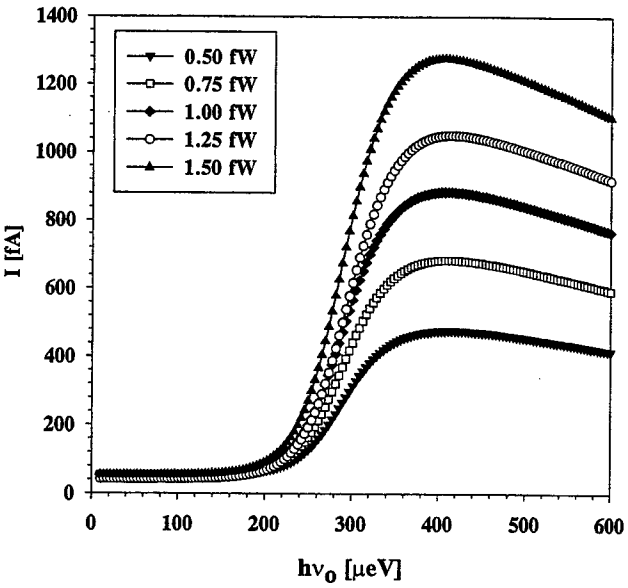


FIG. 4. Source-drain current vs. photon energy for various P_c with a gate charge of 0e and at an ambient temperature of 250 mK.

"Sweeps" Through Photon Energy at T=250 mK

FIG. 4 shows current as a function of photon energy for various values of P_c and $Q_g = 0e$, this time at ambient temperature of 250 mK. For $h\nu_o < \Delta + E_c - W$ ($\cong 282$ μeV), there is a small (~ 50 fA) "leakage" current. This small current is a result of the fact that the temperature is a significant fraction (about 0.22) of E_c/k, allowing thermal transport of charge onto and through the island. At 282 μeV, PAT currents in the direction of the bias rise sharply to produce peak total current levels. The values of the peak levels display a strong dependence on P_c.

FIG. 5 shows current as a function of photon energy for different values of P_c and $Q_g = 1e$ at an ambient temperature of 250 mK. The processes responsible for charge transport in this case are similar to those at $Q_g = 0e$. Note that more thermal current is present here due to the fact that quasiparticle addition to the island is energetically less costly at 1e than at 0e. The asymmetry with gate charge is a result of par-

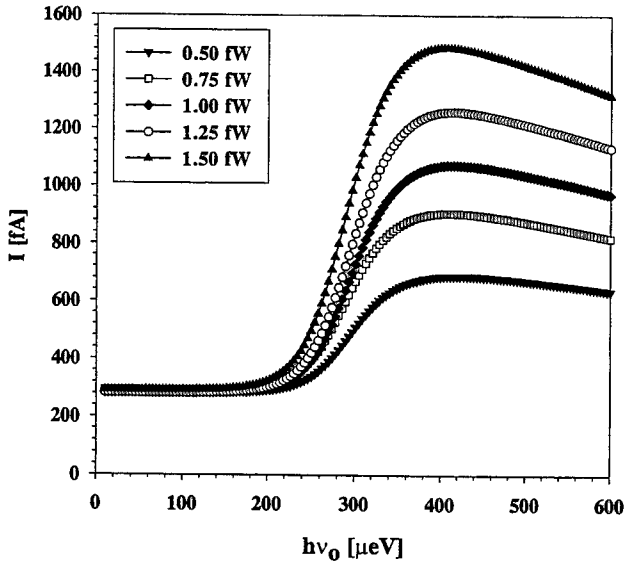


FIG. 5. Source-drain current vs. photon energy for various P_c with a gate charge of e and at an ambient temperature of 250 mK.

ity effects which persist up to temperatures of about 290 mK [6].

IV. Discussion

The spectral response simulations reported here are a useful design tool for device characterization and optimization. Various charge transport mechanisms are evident as sharp features in simulations of source-drain current versus photon energy at T=25 mK. Observation of these features allow exploration of charge transport processes according to the accepted models of PAT in the NSN SET. At T=250 mK, the high responsivity of the device to photon power ($\approx$ 800 A/W maximum for Q_g=0e) combined with current shot noise yield an estimate of Noise Equivalent Power (NEP) of 4×10^{-19} W/Hz$^{1/2}$. This NEP is roughly equal to the estimated photon shot noise at frequencies of about 100 GHz. Measured leakage current (less than 50 fA at 225 mK with zero gate charge [6]) in the SET device agrees with the simulated response and is significantly smaller than the leakage current measured in a single junction system (about 1 nA at 500 mK [8]).

SSS SET devices have been shown to have significantly better photoresponse to incoming radiation. Experimental data published in [6] has demonstrated this improved response as well. Spectral response of the SSS SET is under investigation using techniques similar to those described here.

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Improved Noise Temperature and Bandwidth of Phonon-Cooled NbN Hot Electron Bolometric Mixers

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I. INTRODUCTION

The development of low-noise receivers in the THz frequency region (here defined as 1 THz to 6 THz) is presently motivated by the need for new and improved receivers for the next generation of space-based, airborne, and space-based astronomical and remote sensing instruments (FIRST, SOFIA, EOS-MLS, etc.). Such receivers should also see significant use in ground-based telescopes in a few atmospheric windows above 1 THz followed by balloon-based investigations. Double Sideband (DSB) receiver Noise Temperature (NT) of the present state of the art THz receivers of different technologies is compared in FIG. 1. Recent measured results for NbN Hot Electron Bolometric (HEB) mixer receivers approach 10×hf/2k, where hf/2k is the quantum noise limit for DSB receivers (24 K at 1 THz). The values plotted for Phonon cooled receivers are the total receiver NTs including the beam splitter used for LO injection. The estimated *intrinsic* mixer noise temperature is significantly smaller (~ 5×hf/2k).

There are two types of superconducting HEB devices, the Phonon-Cooled (PC) version [1] and the Diffusion-Cooled (DC) version [2]. This paper will only describe the PC type except for a few brief comparative comments. At present, the lowest recorded receiver noise temperatures have been obtained with the PC type HEB. Furthermore, as this paper shows, a large number of NbN devices have been measured and demonstrated noise temperatures in the same very low range. Superconducting HEB mixers also require much less LO power compared with SB diodes (100 nW to 1 μW for NbN HEBs versus mWs for SB diodes; NbN HEBs will be designed for slightly smaller LO power in future versions). All HEB mixers operate basically as radiation absorbers and have very low parasitic reactance. They are therefore expected to work well at least up to the Near IR.

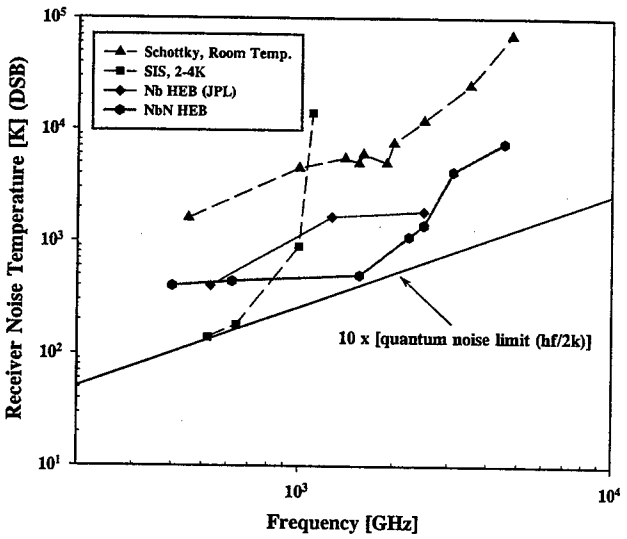


FIG. 1. Noise temperatures as a function of frequency for receivers in the terahertz regime.

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II. Characteristics of HEB Mixers

Receiver Noise Temperature

HEB mixers operate by a bulk hot electron effect, i.e. the THz radiation heats the electron medium to a temperature (the "electron temperature", θ) above the temperature of the substrate and the phonons in the device. Their important characteristics such as conversion gain and output noise can be calculated using what has become the "standard" model for HEB devices [3],[4]. The main assumption inherent in this model is that equal amounts of DC and RF (LO) power produce identical changes in the electron temperature. The entire device is taken to be at the same electron temperature. Improved models have discarded the latter assumption by realizing that the heating develops a "hotspot" in the device [5]. These models agree better with experimental data. The output noise from the device has two main components: (1) thermal fluctuation noise (T_{FL}), which arises from the fact that there are fundamental temperature fluctuations in a small thermal system such as a bolometer, and (2) Johnson noise (T_J) at the transition temperature (T_c) which is about 10 K for our NbN films. The DSB receiver noise temperature can be found from the standard expression as follows,

$$T_{RX,DSB} = \frac{L_c}{2}\left(T_{FL} + T_J + T_{IF}\right) \qquad (1)$$

where T_{IF} is the noise temperature of the IF amplifier chain (typically 5 K), and L_c is the Single SideBand (SSB) conversion loss.

IF Bandwidth

The IF bandwidth for the conversion gain is determined by the thermal time-constant (τ_m) of the HEB device, as

$$B_G = \frac{1}{2\pi\tau_m} \qquad (2)$$

The bandwidth is modified by electro-thermal feedback as expressed by Eq. 10 in [3]. The HEB dissipates the power it absorbs through a two-stage process: the heated electrons first collide inelastically with phonons, which are then transmitted through the film/substrate interface into the substrate. Since the interface reflects some phonons, one must also take into account that phonons feed some of their energy back to the electrons. To minimize this effect, the film should be as thin as possible while still having good superconducting properties. A well known feature of HEB mixers, which is confirmed in [6][7], is that the receiver noise temperature bandwidth (B_{NT}) is wider than the conversion gain bandwidth (B_G). In typical recent devices with film thickness of 3.5 to 4 nm on silicon substrates we have measured B_G = 3 to 4 GHz. We estimate that B_{NT} = 6.5 to 8 GHz [6],[7]. The bandwidth of NbN/Si devices is presently limited by the difficulty of sputtering even thinner films. We present in this paper new measurements which use MgO substrates with much lower boundary resistance between the film and the substrate. NbN devices were fabricated at Chalmers University from films sputtered on MgO at Moscow State Pedagogical University as well as at the Communications Research Laboratory, Kobe, Japan. These devices can have greater thickness and still show the same bandwidth as the thinner NbN/Si devices. For example, we measured a B_G = 3.7 GHz for a device with film thickness of 5 nm. A 15 nm film thickness device had a bandwidth of 1.3 GHz. The NbN/MgO devices presently have a somewhat lower T_c than NbN/Si (8 K vs. 10 K). Future optimization of NbN/MgO film growth is expected to solve this problem and achieve even wider bandwidths if devices with thinner NbN can be made on MgO with higher T_c. For comparison, the widest bandwidth measured for the DC type of HEB is about 10 GHz. These bandwidths are sufficient for most astronomy and remote sensing receivers.

III. Device Design and Fabrication

Device Fabrication and LO Power

A typical HEB device is made from a thin film of NbN deposited on a substrate of silicon, quartz, sapphire, or MgO by DC magnetron sputtering. Much effort has been spent on improving the quality of the NbN films especially critical for the thinnest films. The critical current for a device is a few hundred μA. Since the device acts as a bolometer, the absorbed LO power is measured by the device itself and can be computed from its I-V curve. An accurate method for calculating the LO power has been presented in [8]. As a rule of thumb, the LO power required is three to

five times the DC power. Devices fabricated at UMass/Amherst utilize UV photolithography and have a typical size of length L = 0.6 μm and width W = 5 μm. These devices require an LO power from 0.5 μW to 1 μW ([9], see TABLE I). Devices fabricated at Chalmers University (CUT) utilize an e-beam process which can produce much smaller devices, with dimensions as low as L = 0.1 μm and W = 1 μm. A device with dimensions 0.2×2 μm requires an LO power of 100 nW [6]. Smaller devices should have lower LO power, in proportion to the device volume (maintaining the smallest thickness for maximum IF bandwidth). Precautions must be taken so that as devices are made even smaller, the device does not saturate on the thermal radiation it picks up over the wide RF bandwidth of the antenna. Ultra-low LO power devices will therefore need to use an input filter to lessen this effect. These HEBs could be used with the new generation of solid-state THz sources now under development.

Quasi-Optical Coupling

Quasi-optical coupling is very convenient at the very high THz frequencies. Although quasi-optical antennas have been well developed in the millimeter wave range, these same techniques have only rarely been demonstrated at THz frequencies. We couple our devices through an extended hemispherical lens or an elliptical lens made from high-purity silicon. Lens diameters from 1.3 mm to 13 mm have been used so far. Smaller lenses are used at the higher frequencies. In order to facilitate testing over a wide range of frequencies, we use either a log periodic self-complementary toothed antenna or a logarithmic spiral antenna. Both appear to be about equivalent in terms of receiver NT but more systematic studies need to be performed to compare the efficiencies of different antennas. The antenna types in TABLE I have letter designations from A through C; the development (from A to C) involves scaling the entire antenna to smaller size in order to increase the upper frequency of the antenna band [6],[9]. At the moment, we use no reflection matching for the silicon lens (ε_r = 11.8) for frequencies above 1 THz. Optical losses (and the NT) should decrease by about 2 dB once a suitable material for such coatings in the THz range becomes available. Thermal radiation filtering employs a 0.2 mm thick sheet of material. Liquid helium-cooled HEMT amplifiers are used for IF pre-amplification with a typical bandwidth of 1.2 to 1.8 GHz.

Laser LO Source

CO_2-laser pumped FIR gas lasers which utilize different active media such as difluoromethane and methanol are used for pumping the HEB mixers. Good amplitude stability is required for accurate NT measurements. The amplitude stability of one excellent 1.56 THz laser source at UMass/Lowell, measured over a period of minutes, with a relatively fast (0.1 s) integration time, was 0.3% [9]. A dielectric lens is used to focus the laser LO. The LO power is injected via a 6 μm thick beam splitter, which reflects a few percent of the laser power, while transmitting more than 90% of the power from the hot/cold source.

IV. Experimental Results

A detailed summary of the data for only a portion of the measured devices is presented in TABLE I. Specific frequencies were chosen depending on availability of laser lines; measurements at 0.62 THz were done with a BWO LO source.

It is clear that the NbN HEB technology is maturing in the sense that the receiver noise temperature only varies by about 20% within a group of devices fabricated with similar technology. Devices with different sizes also yield similar noise temperatures. Analysis shows that the *intrinsic* receiver NT is as low as 5 times the quantum noise limit. One may ask how close to the quantum noise limit the NT of HEBs can get? The answer to this question partly depends on unresolved theoretical arguments regarding the correct model for HEB devices [4,5]. Meanwhile, further work on improving NbN HEBs is ongoing in several areas.

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TABLE I: SUMMARY OF EXPERIMENTAL RESULTS FOR SEVEN NbN HEB DEVICES

Device Name	V24	V47	M2_8	J2_1	UM1/A	UM5/B	UM6/C
t [nm]	3.5-4	3.5-4	5	5	3.5	4	3.5
L [μm]	0.15	≤0.1	0.25	0.2	0.6	0.6	0.7
W [μm]	2	1	2	2	10	5	4
I_c [μA] @ 4.2K	180,215,285	145	230	240	425	325	580
T_c [K]	10	10	8	8	10	10	10
R_{20K} [W]	320	430	120	100	140	260	330
P_{LO} [nW]	100	—	—	—	500	850	450
Substrate	Si	Si	MgO	MgO	Si	Si	Si
Fabricated @	CUT	CUT	CUT	CUT	UMass	UMass	UMass
Bandwidth [GHz]	3.2	3.2	3.7***	1.6	3.0	—	—
Antenna Type	Spiral B	Spiral C	Spiral B	Spiral B	Log-Per A	Log-Per B	Log-Per C
NT_{DSB} [K] @ 0.62 THz	—	—	480***	530***	440**	—	—
NT_{DSB} [K] @ 0.7 THz	800	1,900	750	650**	—	—	—
NT_{DSB} [K] @ 1.4 THz	1,100	1,700	—	—	—	—	—
NT_{DSB} [K] @ 1.56 THz	1,100	1,700	—	—	—	1,000	500
NT_{DSB} [K] @ 2.24 THz	—	—	—	—	—	2,200	1,100
NT_{DSB} [K] @ 2.52 THz	2,100	2,000*	1,400**	1,500**	—	—	—
NT_{DSB} [K] @ 3.1 THz	—	4,200	—	—	—	—	—

*Measured at an ambient temperature of 3 K; **Measured at 2.2 K; ***Devices from the same batch measured at 2.2 K; noise temperatures given are for the entire receiver, including the beam splitter.

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Student Paper

First Demonstration of High-Speed Uncooled Type-II Superlattices for Long Wavelength Infrared Detection

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I- INTRODUCTION

Uncooled infrared (IR) detectors are required for low-cost, lightweight sensor systems that have both military and commercial applications. Commercially available uncooled IR sensors use ferroelectric or microbolometer detectors. These sensors are inherently slow and cannot detect rapid signal changes needed for many applications. Some of the applications which require a fast detector response time ($\tau < 30$ msec) are: free-space communication, proximity fuzes, active infrared countermeasure systems, non-invasive medical monitoring, and LIDARs. Although photon detectors have frequency responses in the megahertz range, their high temperature detectivity is severely degraded due to physical limitations. The existing infrared photon detectors can be categorized as interband, which are mostly HgCdTe and InAsSb, or intersubband quantum well infrared detectors (QWIP). Unfortunately, fast Auger recombination rate in the interband detectors and high thermal generation rate in the intersubband detectors decrease their performance for room temperature operation drastically.

In order to realize Auger suppression at room temperature, we have developed a new type-II superlattice detector design[1]. The experimental results show nearly one order of magnitude lower Auger recombination rate at room temperature in such detectors compared to typical intrinsic (HgCdTe) detectors with similar bandgap . Preliminary single-element detectors[2] shows a detectivity of 1.3×10^8 cmHz$^{1/2}$/W at 11&m at room temperature which is comparable to microbolometers. However, the measured response time of the detector is less than 68 nsec which is more than six orders of magnitude faster than microbolometers.

II- MODELING

For the simulation of energy bands and the electrons and holes wavefunctions in the superlattices, we used an 8-band **k.p** approach. Finite Element Method (FEM) was used to generate the system of differential equations. The band structure of type-II superlattices was engineered for lower Auger recombination rate, since Auger is the primary recombination mechanism at high temperatures in narrow gap IR detectors and lasers. Figure 1 shows the result of such simulation for the band structure of two superlattice structures in the k-space. Numerical calculation shows that the Auger resonance between the conduction, heavy-hole, and light-hole bands (Auger 7) is much less in the left structure since the light-hole band is out of the resonance for low values of $k_\perp$.

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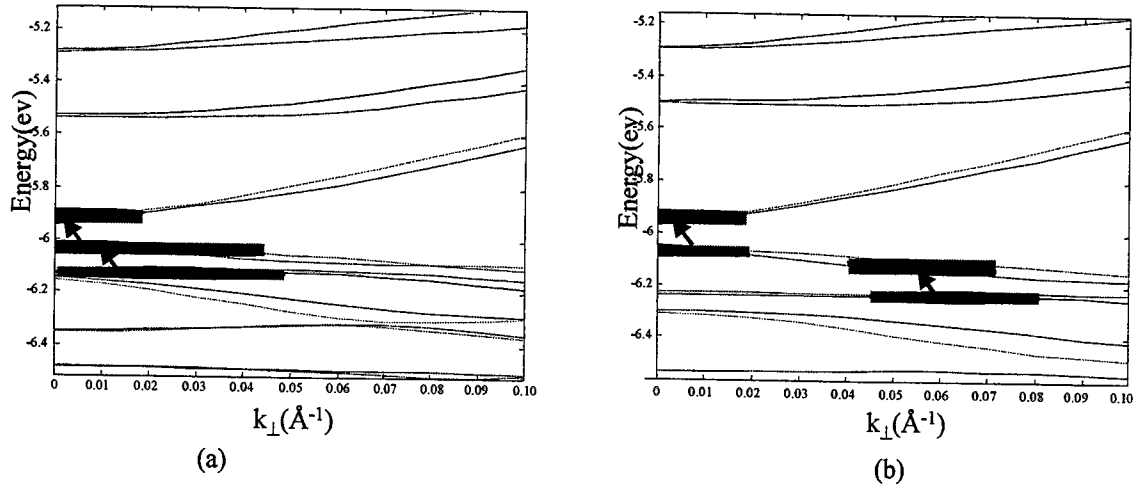


Figure 1. (a) Energy band structure of InAs/InSb/GaSb/InSb 48O/3O/48O/3O and (b) InAs/InSb/GaSb/InSb 48O/3O/30O/3O superlattices calculated with the eight-band **k.p** simulation.

III- GROWTH AND CHARACTERIZATION

The optimized structures were grown in a Varian Modular Gen-II solid source molecular beam epitaxy (MBE) system. The reactor is designed to grow Sb-based material with high uniformity on 3 inch wafers. The growth temperature, III/V flux ratio, and the growth rate of the material were optimized for minimum compositional and thickness variation over large areas. Theoretical calculation shows that as the cut-off wavelength of the superlattice increases, its sensitivity to the composition and to the thickness superlattices increases. On the other hand, it has been shown that the interface layer in type-II superlattices can considerably affect the optical and electrical properties of this material system. In order to control the interface accurately, migration-enhanced epitaxy was used to control the intermixing at the interfaces. MBE shutter sequence was designed to increase the surface diffusion length of the adatoms. In the first step of the sequence, group III shutter was opened to provide the designed surface coverage. In the next step, all the shutters were closed so the adatoms could diffuse over the surface. Then group V shutter was opened. Our experimental results show that atomically flat surfaces over large areas can be grown at low temperatures with this technique. The low growth temperature will also ensure low diffusion of arsenic atoms through the interfaces which leads to lower background carrier concentration.

In order to fulfill the tight material quality requirement (composition and interface control), epitaxial layers were systematically characterized using a combination of structural, optical, and electrical techniques. For structural characterization, high resolution five-crystal x-ray diffraction system, scanning electron microscopy (SEM), and atomic force microscopy (AFM) were used. The average lattice constant and the period of the superlattices were accurately measured with a high-resolution x-ray diffraction system. The cross section of the samples was studied with SEM. The surface roughness of the samples was measured with AFM system, since SEM cannot provide comparable resolution and contrast. For optical characterization we used photoluminescence (PL), and Fourier Transform Infrared (FTIR) techniques in the 77K and 300K range. PL measurement provided information about the material quality, and in particular on the generation-recombination mechanism. FTIR system was used for absorption coefficient measurements. This information were used to estimate the internal quantum efficiency and the effective bandgap of the superlattices. For electrical inspection we used Hall measurement system, parameter and spectrum analyzers. Magnetic-dependent Hall measurement of the superlattices provided some information about the electron and hole concentration as well as their mobilities. The minority carrier lifetime was extracted from the measured quantum efficiency, carrier mobility, carrier concentration, and optical responsivity of the photoconductors.

IV- DEVICE PROCESSING AND MEASUREMENT

Photoconductor devices were fabricated by standard lithography and subsequent etching with H_3PO_4:H_2O_2:H_2O (1:1:10) solution. For ohmic contacts, Ti/Au (500Å/2000Å) was deposited and then the contacts were defined by lift-off technique. No anti-reflection coating or surface passivation was employed.

Spectral photoresponse of the device was measured using a Galaxy 3000 FTIR spectrometer system. The samples were illuminated through the front side at normal incidence. The absolute response of the photodetectors was calculated using a blackbody test set, which is composed of a blackbody source (Mikron 305), preamplifier (EG&G PA-100), lock-in amplifier (EG&G 5209), and chopper system (Stanford Research System SR540). Figure 2 (a) shows the spectral response of the device in the 2-17μm wavelength range at 78K and 300K. To asses the temperature dependence, the current responsivity of the device was measured at 10.6μm wavelength from 78K to room temperature at constant electrical field. Figure 2 (b) shows the responsivity of the detector at 10.6 μm versus the detector temperature. An Allometric fitting with a general form of $A.T^B$ where T is the temperature and A and B are the fitting variables, shows that the responsivity of the detector is nearly proportional to T^{-2}. This is an unusual behavior since responsivity of the narrow gap material is usually an exponential function of temperature at higher temperatures where Auger recombination is the dominant recombination mechanism.

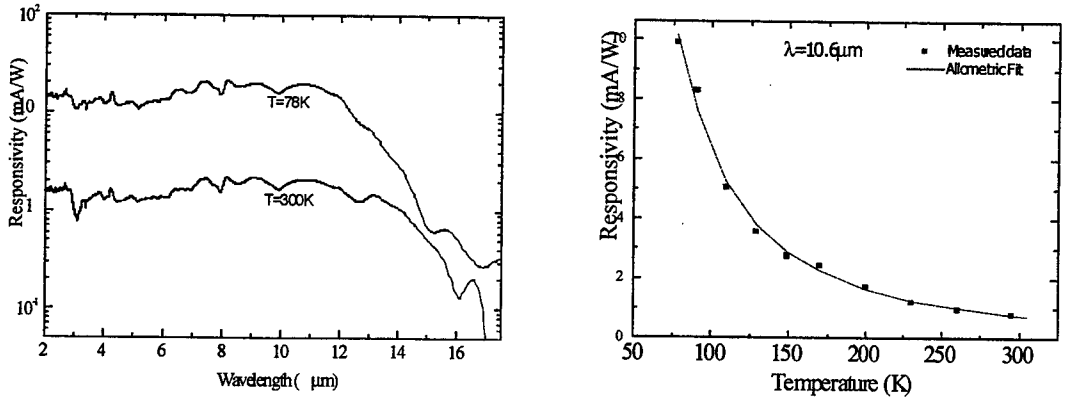
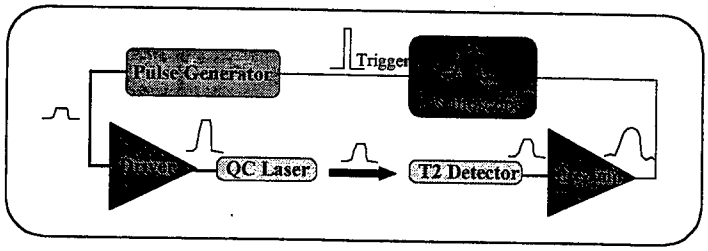


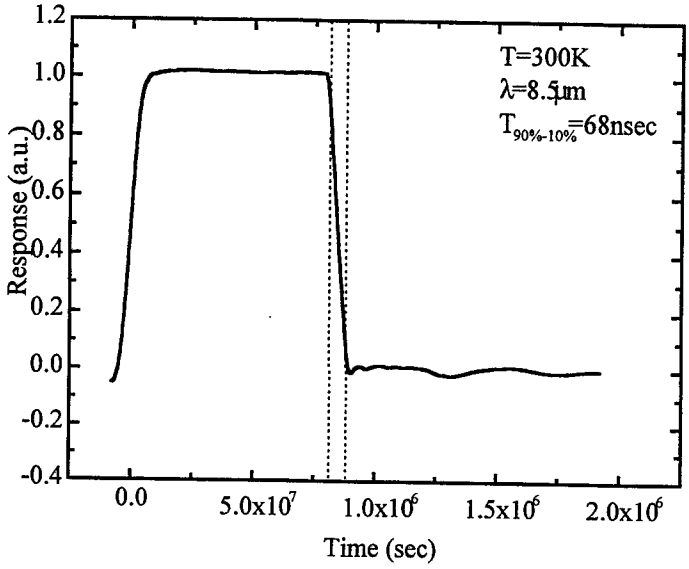
Figure 2. (a) The responsivity spectra of the device at 78K and 300K with an in-plane electrical field of 5V/cm and (b) current responsivity of the device versus temperature at λ=10.6μm.

Also, a field-depended Hall measurement was used to extract the mobility and concentration of electrons and holes in the superlattice at different temperatures. The carriers lifetime was extracted from the optical responsivity of the detectors and the carrier concentrations and mobilities. The extracted carrier lifetime is about 27nsec which is about one order of magnitude longer than the best bulk semiconductors with similar bandgap (HgCdTe) at room temperature. The results of this study shows that the Auger recombination is suppressed[3] in this material system. Based on the responsivity and noise measurements, the detectivity of the device was calculated as $1.3x10^8$ cm $Hz^{1/2}$/W at 11μm at room temperature[2]. This value is several times higher than the detectivity of commercially available high-speed HgCdTe detectors.

In order to study the speed of the detector, the time response of the detector to the infrared pulses generated by a quantum cascade laser was measured. The schematic diagram of the setup is shown in figure 3 (a). The pulse generator and laser driver were inside an Avtech AVR-4A-PW which is capable of generating high power electrical pulses with fall time of about 5 nsec. The quantum cascade laser was uncooled and operated at λ=8.5μm with a negligible time delay. An EG&G PA-100 low-noise pre-amp was used to amplify the detector signal. Unfortunately, the pre-amp is not very fast and has a fall time of more than 40 nsec. The output signal of the pre-amp was measured with a Tektronix TDS 520B digital oscilloscope. It shows a fall time of about 68 nsec, as shown in figure 3(b), for the whole setup and hence the detector has a fall time of less than this value.



(a)



(b)

Figure 3. (a) The schematic diagram of the time response measurement setup. (b) The overall time response of the setup.

V- CONCLUSION

Using the bandgap engineering and optimization of the growth, we demonstrated the first long wavelength uncooled infrared detector from type-II superlattices. The measured detectivity is 1.3×10^8 $cmHz^{1/2}/W$ at 11μm at room temperature which is comparable to microbolometers. However, our preliminary results shows that the response time of the detector is less than 68 nsec which is about six orders of magnitude shorter than microbolometers.

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Student Paper

Lateral Epitaxial Overgrowth of GaN: Materials and Devices

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I. INTRODUCTION

Over the past decade, wide bandgap GaN based semiconductors have become the most coveted material system thanks to their exceptional physical properties and immense potential for use in numerous devices. Not only are they ideally suited for short wavelength optoelectronic devices such as ultraviolet photodetectors and blue lasers, but they are becoming strong candidates for high temperature and high power electronics as well. In spite of all the recent successes, the lack of a suitable native GaN-based substrate remains the core problem of this promising technology. The resulting unavoidable use of heteroepitaxy on a foreign substrate, e.g. widely used sapphire, has plagued these materials with a high density of defects and preventing these from reaching a device has been a challenge ever since. An encouraging approach which has recently received increasing attention is lateral epitaxial overgrowth (LEO), which has the potential to achieve low defect GaN films on wide range of substrates.[1] This paper reports the LEO growth and characterization of low defective GaN films on sapphire (Al_2O_3) and silicon (Si) substrates, along with the first demonstration of high performance GaN-based solar blind ultraviolet photodetectors.

II. MATERIAL GROWTH

The GaN films were grown by low pressure metalorganic chemical vapor deposition. The Al_2O_3 and Si substrates were chemically cleaned prior to loading into the reactor. 1-2 μm and 0.2 μm thick GaN *template* epilayers (i.e. non-LEO) were first grown on Al_2O_3 and Si substrates, respectively, under typical growth conditions as reported earlier.[2] A thin (500-2000 Å) SiO_2 film was subsequently deposited onto these template layers and a 15 μm period stripe pattern was defined, with dielectric stripe widths between 7-11 μm and oriented along the <10.0> direction of the underlying GaN crystal. The samples were then loaded back into the reactor for regrowth.

III. CHARACTERIZATION OF LEO GaN FILMS

The resulting LEO films were characterized through scanning and transmission electron microscopy (SEM, TEM), atomic force microscopy (AFM), x-ray diffraction

(XRD), photoluminescence (PL). Capacitance-voltage (CV) and deep level transient spectroscopy (DLTS) were also conducted after fabrication of Schottky diodes on the wafers using Ti/Au (ohmic) and Pt/Au (Schottky) metal contacts.

Fully coalesced single and double LEO GaN films were achieved on sapphire substrates, as shown in the cross-section SEM micrographs in Figure 1. Similarly, high quality fully coalesced single LEO GaN films were achieved on silicon substrates, as shown in Figure 2. AFM imaging of the sample surfaces on both substrates showed a clear morphology disparity between the regions grown over the open windows ("vertically" grown GaN) and those over the dielectric mask ("laterally" grown GaN). The vertically grown regions showed an irregular structure and numerous pits which corresponded to the termination of threading dislocations, whereas the laterally grown regions exhibited a much more regular structure without pit. The LEO grown GaN on Si had a much smoother surface (rms=0.639 nm) than the template layer used (rms=2.723 nm). Cross-section and plan view TEM microanalysis demonstrated at least a three order of magnitude reduction in the threading dislocation density in the laterally overgrown areas over the dielectric mask.

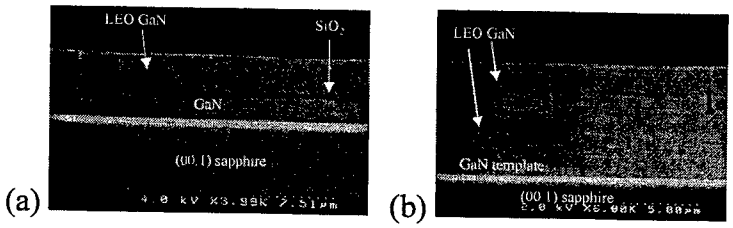


Figure 1. SEM micrographs of a coalesced (a) single, (b) double LEO GaN on sapphire.

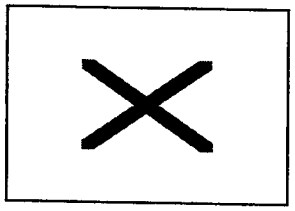


Figure 2. SEM micrograph of a coalesced single LEO GaN on silicon.

Symmetric XRD measurements were found to be sensitive to the relative direction of the incident x-ray diffraction beam with respect to the LEO stripes. It was shown that when the x-ray beam is in a plane parallel to the stripes, a single diffraction peak is observed, whereas when the beam is in a plane perpendicular to the stripes, multiple peaks could sometimes be observed. This phenomenon was interpreted by the existence of a misalignment between the crystal planes in different laterally overgrown regions. The magnitude of this misalignment was on the order of a degree.

The optical properties of LEO GaN were assessed through PL. The luminescence spectra for 300, 77 and 16 K are shown in Figure 3 for a double LEO GaN/sapphire, a single LEO GaN/silicon and were compared a state-of-the-art non-LEO GaN/sapphire. The same intensity scale has been used for all three measurements. These showed that

the most intense luminescence originated from the double LEO GaN/sapphire, followed by the LEO GaN/Si and the non-LEO GaN/sapphire. This indicates the LEO GaN on either substrate exhibits an improved optical quality over non-LEO material (by up to one order of magnitude in PL intensity), which is most likely due to the reduction of defects in the laterally overgrown material.

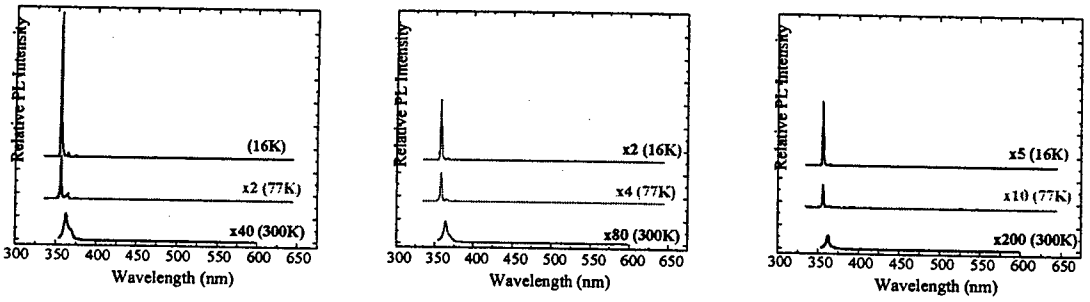


Figure 3. PL spectra at various temperatures for double LEO GaN on sapphire (left), single LEO GaN on silicon (middle) and non-LEO GaN on sapphire (right). The magnifications in the PL spectra are noted accordingly.

The electrical characterization of LEO grown films cannot be performed as simply as on non-LEO films because the LEO samples are non isotropic over the surface and non uniform over the thickness of the sample. However, CV and DLTS measurements have been successfully conducted to determine for the first time the electrical properties of single LEO GaN on both sapphire and silicon substrates, after defining ohmic and Schottky metal contacts.

Linearly fitting the $1/C^2$ vs. reverse bias plots shown in Figure 4 allowed to determine the doping concentration N_D to be $1.13x10^{16}$ cm^{-3} and $6.4x10^{15}$ cm^{-3} for the LEO GaN on sapphire and silicon, respectively. The depletion widths could then be estimated from these doping concentrations and were found to be range, for a reverse bias of 0-5 V, from 0.325 to 0.753 μm and from 0.42 to 1 μm for the films on sapphire and Si, respectively. The good linearity of the C-V data points shown in Figure 4 indicates a good uniformity in doping for the material over the thickness of the depletion width. Moreover, the low values obtained for the doping concentrations, as low as the lowest unintentionally doped non-LEO samples reported, confirm that there is minimal contamination from the dielectric mask in the growth conditions used.

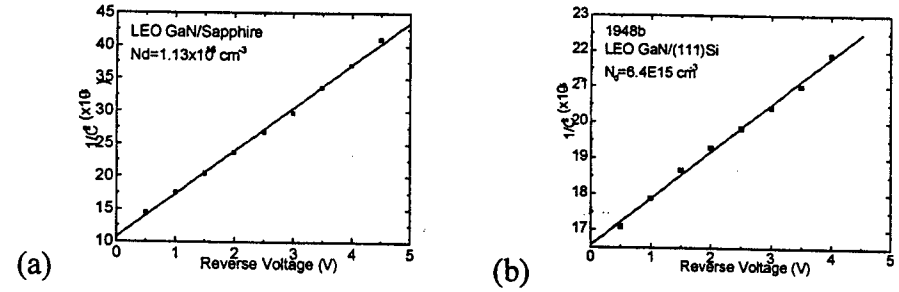


Figure 4. $1/C^2$ vs. reverse voltage for a Schottky diode on LEO GaN on (a) sapphire and (b) silicon.

Three levels were found in LEO GaN on sapphire from DLTS measurements and were located at 0.19, 0.30 and 0.454 eV below the conduction band, with activation energies of 4.88×10^{-18}, 7.83×10^{-17} and 1.50×10^{-15} cm^2, respectively. The LEO GaN on silicon exhibited two deep levels at 0.45 and 0.60 eV below the conduction band, with capture cross sections of 2.59×10^{-14} and 1.35×10^{-15} cm^2, respectively.

IV. ULTRAVIOLET PHOTODETECTORS ON LEO GaN

$Al_xGa_{1-x}N$ p-i-n photovoltaic detector structures with high Al concentrations (70%), as shown in Figure 5(a), were grown on LEO GaN wafers on sapphire substrates for the first time. Square mesas were subsequently etched through ECR-RF dry etching, Ti/Au and Ni/Au were deposited to form ohmic metal contacts to the n-type and p-type AlGaN, respectively. The spectral response of these detectors is show in Figure 5(b) and exhibits a peak responsivity of 0.052 A/W without bias at 232 nm, and a visible rejection ratio of five orders of magnitude. The internal quantum efficiency was estimated at 50%. For comparison, the same device structure grown on non-LEO GaN on sapphire yielded a lower efficiency (40%) and a slightly lower visible rejection ratio.

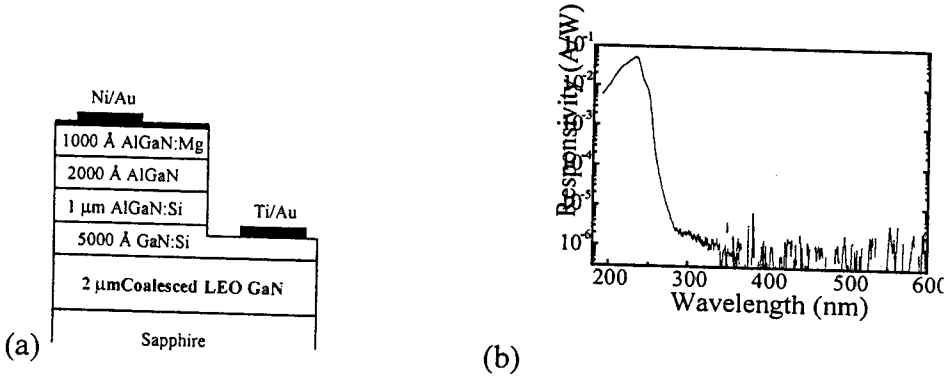


Figure 5. (a) structure and (b) room temperature, unbiased spectral response from a AlGaN p-i-n photodiode on LEO GaN wafer.

V. CONCLUSIONS

Low defect density GaN films have been demonstrated using lateral epitaxial overgrowth on sapphire and silicon substrates. The epilayers exhibited superior structural and optical properties than non-LEO GaN grown on the same respective substrates. Enhanced performance short wavelength $Al_xGa_{1-x}N$ p-i-n ultraviolet photodetectors have been demonstrated on LEO GaN wafers, with a quantum efficiency of 50% at 232 nm.

VI. ACKNOWLEDGMENTS

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AlGaInAs/InP AND GaInSbAs/InP HIGHLY REFLECTIVE MIRRORS FOR VCSEL APPLICATIONS OPERATING AT 1.55μm

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I. INTRODUCTION

Vertical cavity surface emitting lasers (VCSELs) are promising for the telecommunication range of applications (1.3μm – 1.5μm) because of their ultra low threshold currents, and small optical beam divergence [1]. Long wavelength VCSELs are promising as light sources for long-distance optical communication systems [2], optical scanning, displays, data links [3], and two-dimensional light sources for optical parallel processing and high capacity optical fiber communications [4].

The development of VCSELs for applications at 1.3 –1.5μm wavelength has been centered on the investigation of structures and materials grown lattice matched to InP substrates [5], and in particular high quality epitaxial Bragg mirrors. The most commonly used material systems are InGaAsP/InP [4,6], InGaAlAs/InAlAs [7], AlAsSb/GaAsSb [8], and AlGaAsSb/AlAsSb [9,10]. The above DBR structures produce the optical index step of about 0.25 to 0.5 [1] at the incident wavelength of 1.55μm, thus implying the need for very thick structures (from 40 to 20 DBR pairs) to obtain highly reflective Bragg mirrors (99%). The large refractive index contrast is required to reduce the number of DBR pairs to achieve a given peak reflectance[11], to have shorter processing times, and to minimize the diffraction losses.

In order to find the optimum material system for high index contrast DBR, fifteen various quaternary alloys were investigated, and their refractive indices were calculated at the wavelength of 1.55μm. As a result, a DBR structure has been designed which incorporates 15 pairs of alternating AlGaInAs/InP (101.9nm and 122.5nm thick respectively) or 15 pairs of GaInSbAs/InP (100.6nm and 122.5nm thick respectively) which produces 99% reflective mirrors.

II. DESIGN AND OPTIMIZATION OF THE BRAGG MIRRORS

Theoretical optimization of the refractive indices of the III-V quaternary alloys in the form $A_xB_{1-x}C_yD_{1-y}$, $A_xB_yC_{1-x-y}D$, and $AB_xC_yD_{1-x-y}$ was based on the model presented by Adachi [12]. The quaternary alloy band gap energies required for the refractive index calculations were obtained from the corresponding binary alloy energy band gaps and ternary bowing parameters as described by Glisson *et al.*[13] and Adachi [12]. In all calculations only direct energy band gaps larger than 0.8eV have been taken into account in order to avoid strong absorption in the material.

The investigation and comparison of the refractive indices of fifteen III-V quaternary alloys lattice matched to InP calculated as a function of the incident wavelength and the alloy composition, x and y, reveals that the biggest optical index contrast can be achieved for two systems: $Ga_{0.78}In_{0.22}Sb_{0.29}As_{0.71}$/InP and $Al_{0.05}Ga_{0.42}In_{0.53}As$/InP. The lattice matching conditions for these alloys are:

$Al_xGa_yIn_{1-x-y}As$ to InP:

$$y = 0.47 - 0.98x \quad (1)$$

$Ga_xIn_{1-x}Sb_yAs_{1-y}$ to InP:

$$y = (0.41x - 0.19)/(0.02x + 0.42) \quad (2)$$

Figures 1 and 2 present the dependence of the refractive indices of GaInSbAs and AlGaInAs on the alloy composition at the incident wavelength of 1.55μm. The optical index difference,Δn, of 0.66 is obtained by $Ga_{0.78}In_{0.22}Sb_{0.29}As_{0.71}$ ($n_1 = 3.83$) and InP ($n_2 = 3.17$), and $\Delta n = 0.63$ by $Al_{0.05}Ga_{0.42}In_{0.53}As$ ($n_1 = 3.8$) and InP ($n_2 = 3.17$). Further reflectivity calculations for the two alloy pairs show that reflectivity of 99% can be obtained over 15 alternating pairs of $Ga_{0.78}In_{0.22}Sb_{0.29}As_{0.71}$/InP or $Al_{0.05}Ga_{0.42}In_{0.53}As$/InP assuming that InP substrate is used and $Ga_{0.37}In_{0.63}As_{0.8}P_{0.2}$ is taken as an active layer with the index of refraction of 3.79. Theoretical thicknesses of the alternating layers in the DBR stack satisfy Bragg quarter wavelength condition: $\lambda/4 = n_1d_1 = n_2d_2$, where d_1(GaInSbAs) = 100.63nm, d_1(AlGaInAs) = 101.25nm, and d_2(InP) = 122.5nm.

III. SUMMARY

In conclusion. we report two material systems consisting of the quaternary and binary semiconductor alloys. $Ga_{0.78}In_{0.22}Sb_{0.29}As_{0.71}$/InP and $Al_{0.05}Ga_{0.42}In_{0.53}As$/InP, which may be used as DBRs due to the large optical index difference they demonstrate between alternating layers. This result was obtained by modeling the refractive index and energy band gap for fifteen quaternary alloys lattice matched to InP and at the incident wavelength of 1.55μm.

ACKNOWLEDGEMENTS

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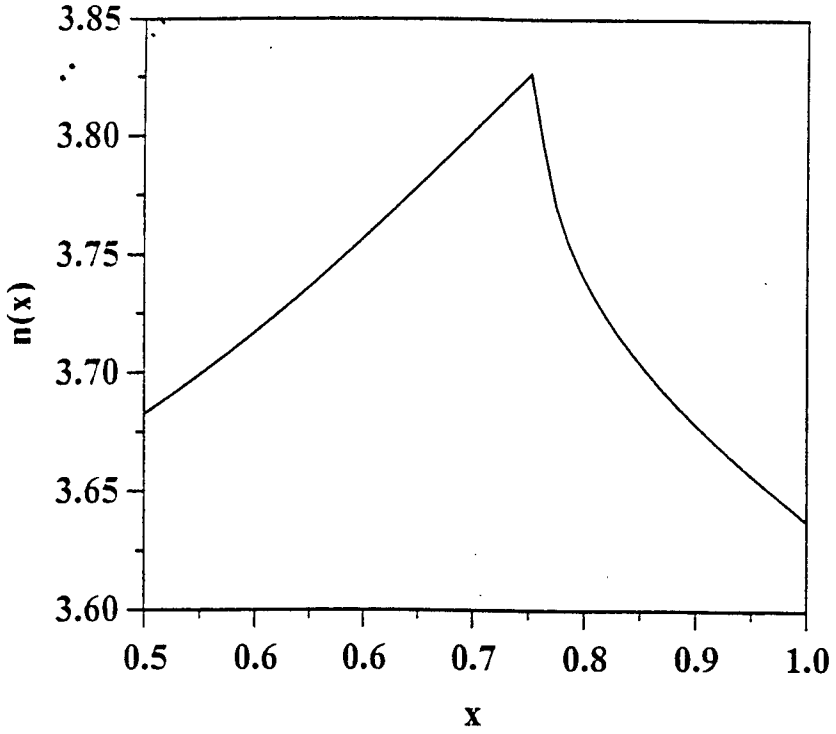


Fig.1. Dependence of the refractive index of $Ga_xIn_{1-x}Sb_yAs_{1-y}$ alloy lattice matched to InP as a function of its composition, x, in the direct energy band gap region.

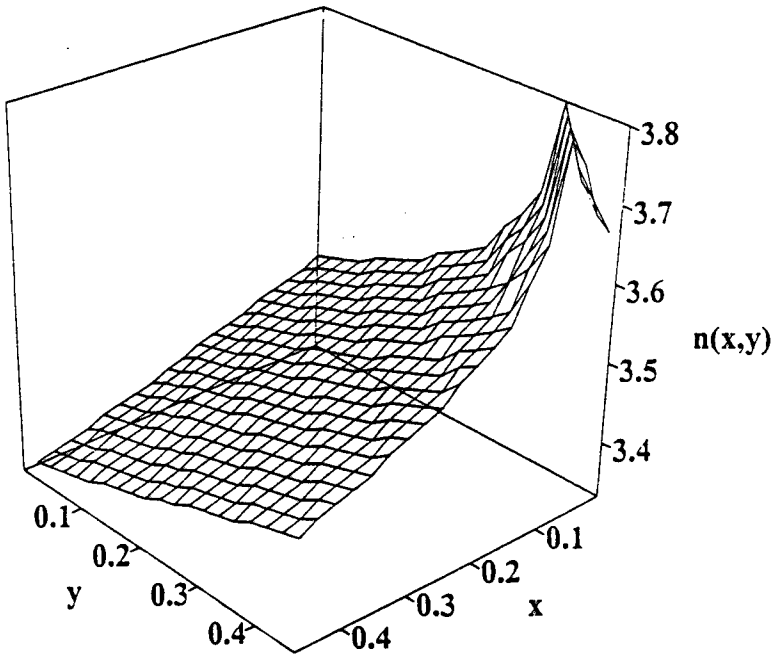


Fig.2. Dependence of the refractive index of $Al_xGa_yIn_{1-x-y}As$ alloy as a function of its composition, x and y.

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