SECOND ANNUAL REPORT
ON
PACKAGING OF POWER ELECTRONICS BUILDING BLOCKS

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SUBMITTED TO
Dr. Albert J. Tucker
Office of Naval Research (ONR 334)
Ship Structures and Systems S&T Division
800 N. Quincy Street
Arlington, VA 22217-5660

PREPARED BY
Professors: J.D. van Wyk, G-Q. Lu, D. Boroyevich and F.C. Lee
Staff: Dan Huff, Zhenxian Liang
Students: S. Wen, V. Liu, L. Zhao, Z. Chen, J. Xiukuan
Center for Power Electronics Systems (CPES)
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061-0179

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I. EXECUTIVE SUMMARY

Our primary objective remains to explore innovative three-dimensional electronics packaging approaches with the elimination of wirebonds as device interconnection for packaging PEBB's. Our accomplishments, on-going research, and proposed future work are summarized below:

1.1 Accomplishments

Many significant accomplishments have been made on the PEBB project to date. We have selected the zero-voltage-zero-current-transition (ZVZCT) soft-switching technique developed by CPES because of the successful experimental results obtained with this technique on other ONR projects (SMES and PEBB Systems Integration).

We have focused our packaging efforts on two basic interconnect approaches in our effort to eliminate wirebonds. One is a direct solder approach where devices with a solderable pad metalization are obtained and interconnection is achieved by soldering directly to the pads. We have been successful in obtaining solderable power devices, which has permitted us to construct a functioning prototype MPIPPS module. The other approach is through a sputtered thin-film metalization deposited directly onto the device pads and a surrounding dielectric layer, then thickened by electroplating and patterned by photo etching to achieve the required circuit pattern. Power switching stages using two different sputtered metal approaches, Power Overlay-"POL" and Embedded Power, have been under development, with one Embedded Power module completed up to a functioning prototype. Test results of the functioning solder-approach module, test results of the modules by sputtered approach, and a description of the design and manufacturing steps of all packaging approaches are presented in this report.

We have recognized a need for the ability to perform comparison testing on modules constructed using the different packaging approaches. For this we have designed and assembled a universal tester, which permits the measurement of the module's switching characteristics under full current and voltage conditions.

We have continued the upgrade of the packaging lab facility. Equipment has been added and modified so that manufacturing processes can be performed in a manner approaching that used in industry. The packaging researchers have developed the capability to perform the processes and have established sources for the required materials from vendors common to the electronics industry.

1.2 On-going Research

The strongest emphasis of our on-going research is in the production of functioning PEBB modules using each of the packaging approaches. We have developed the capability to perform all of the unit steps required for each type of module we are considering and we are now working to optimize each of these processes. In conjunction with the process development, phase leg modules are being constructed to aid in the evaluation of the process's effect on performance.

Much emphasis is also being placed on the integration of passive devices. We are investigating an alternative approach to inductor and capacitor integration using a planar structure based on planar ferrites, flat conductors, and high permittivity ceramic dielectrics. Software has been developed at CPES to aid in the electromagnetic and thermal design.

Thermal and thermo-mechanical models are being developed to analyze the heat and stress characteristics of the different packaging approaches. We are also exploring methods of temperature measurement to validate the modeling. This analysis, along with a recently formed alliance with University of Maryland's CALCE Lab will permit us to evaluate the reliability of the different packaging approaches while the results can still influence the design.

1.3 Proposed Future Effort

In the coming year process development for constructing prototype modules along each of the packaging approaches will be completed. Several samples representing each of the approaches will be produced. Using these, comparison performance testing and reliability analysis will be performed to determine the best packaging approach to adopt. We also propose to incorporate gate drive control circuitry and passive devices in the construction of PEBB-spec modules.

II. INTRODUCTION

2.1 Review of Objectives and Approaches

The major objective of the PEBB research at CPES remains to support ONR's program to develop a new generation of electric ships based on the building block concept utilizing high voltage dc distribution. From the system point of view, the integrated power system (IPS) must be reliable and provide uninterrupted power supply to critical loads. The IPS should be based on the PEBB concept and should be reconfigurable and programmable via a high-level communication and control bus. This requires the development of programmable converters with high levels of intelligence and control autonomy, wide control bandwidths, and fail-safe capability. At present, high frequency power conversion technology has reached the point where further advances in semiconductor technology have limited benefit due to physical limitations of the current packaging methods. Package inductance, thermal handling, wire insulation, active and passive components, packaging materials, interconnect structures, thermal management, EMC and EMI, circuits and system integration, as well as manufacturing technologies are all important considerations for developing the correct packaging approach. At CPES we would adopt an integrated systems approach to standardize power electronics components and packaging techniques in the form of highly integrated Power Electronics Building Block modules. This approach makes possible an increased level of integration in the components that comprise a power electronics system: devices, circuits, controls, sensors, and actuators. These components are integrated into standardized manufacturable subassemblies and modules, which in turn, are customized for particular applications. By developing the PEBB based power electronics converters using an integrated systems approach, we will improve the quality, reliability, and cost-effectiveness of power electronics systems and reduce both the time and effort associated with design cycles for system application. Power electronics and related power processing technologies constitute an "enabling infrastructure technology" with significant potential impact on the U.S. Navy, other U.S. government agencies and industries.

The technical approach remains to construct the first generation PEBB as an integrated phase-leg module, fabricated based on the packaging techniques developed in the previous program effort. Power handling capability and the feasibility of a high bus voltage will be estimated for the approaches developed. The PEBB module will incorporate integrated gate in a three-dimensional package. Active components are bare dice and are attached with various attachment techniques. The module could communicate to higher-level controller via fiber optics. Packaging techniques and improved electrical design will be targeted to minimize both conducted and radiated EMI. Appropriate soft-switching techniques will be implemented in the module to improve electrical performance.

Finally, the different packaging technologies developed will be assessed on a comparative basis, using the electrical test results, thermal and thermo-mechanical modeling and the results of thermal cycling in the packaging lab test facilities.

2.2 Facilities Upgrade

Accomplishments in the past year have proven that the CPES power electronics packaging lab has the capability to provide the equipment and resources that will allow the researchers the capability to perform all of the necessary assembly processes for each of the packaging approaches in a consistent manner. CPES has added a senior packaging engineer with over fifteen years of experience in electronics packaging and microelectronics process engineering, to supervise the lab and maintain an industry level of standards to its processing work. Equipment added in the past year includes a plasma cleaning system, a microscopic digital imaging system, and modular workstations. Modifications to existing equipment has been performed, such as designing and incorporating a rotating stage for the thin-film sputtering system which

permits the use of multiple sputtering targets without opening the chamber. Work in progress includes expanding cleanroom processing space, establishing nitrogen atmosphere dry storage cabinets and upgrading the darkroom facilities. These efforts have been undertaken in the effort to eliminate processing variables in module performance.

The following is an outline of the current processing capabilities in the CPES packaging lab.

Circuit Boards:

CAD layout of circuit artwork from schematics

Gerber file generation

Photolithography

Chemical and electro-chemical etching of copper on DBC, IMS, flex, and FR4

Copper thru-hole plating

Electrolytic copper, nickel, and chromium plating

Electro-less nickel and tin plating

Immersion gold plating

Laser machining of ceramic, metals, and ferrites

Hybrid Thick Film Processing:

CAD layout of circuit artwork for paste printing screens

Gerber file generation

Screen printing and controlled atmosphere firing of thick film pastes on Al_2O_3, AlN, and BeO substrates

High-temperature pressure lamination

Thin Film Processing:

Plasma cleaning

Thin film sputter deposition of Cu, Ni, Au, Ti, Cr, Ag, and dielectric on ceramic and kapton

Design and laser cutting of sputter masks

Module Assembly:

Design of artwork for solder paste stencils

Pick and place assembly of surface mount components

Die and device solder attach by hand soldering and controlled-atmosphere reflow ovens

Wire bonding, 1 to 4 mil gold and 10 to 20 mil aluminum

Epoxy attach of components and substrates using conductive and non-conductive epoxies

Component removal by hot gas rework station

Module encapsulation

Electrical Characterization:

Cascade probe station

Low and high power curve tracers

Standard lab electrical testing equipment

Reliability:

Computer modeling of thermal and mechanical stresses

Temperature distribution and hot-spot analysis using real-time thermal imaging camera

In-process electrical testing of components and sub-assemblies

Thermal cycling, -68°C to 177°C

Humidity testing, 20 to 95% RH

III. GENERIC WORK

3.1 Selected Design

A zero-voltage-zero-current-transition (ZVZCT) soft-switching technique developed by CPES has been selected as a test bed, based on the theoretical evaluations during the first year of the project and on the successful experimental results obtained with this technique on other ONR projects (*SMES* and *PEBB Systems Integration*). This topology is shown in Figure 3.1.1 Evaluation of all the packaging concepts developed is done against the background of constructing modules that can be used successfully in this PEBB-1 converter concept.

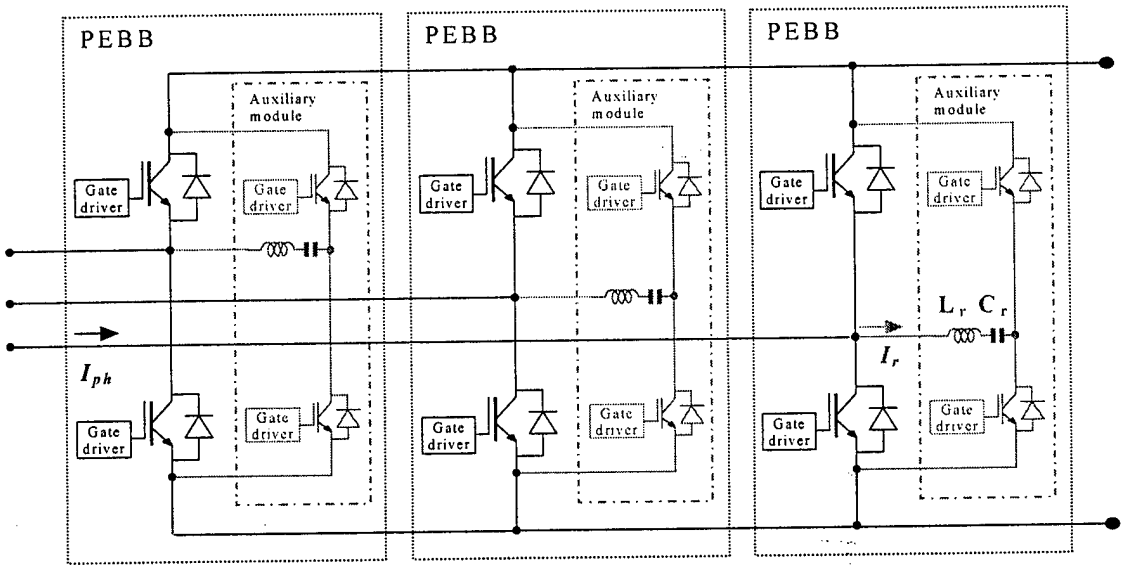


Figure 3.1.1. Schematic of a 100 kW three-phase ZVZCT rectifier/inverter based on PEBB modules.

3.2 Comparison Testing

The universal tester of device switching characteristics, that is used at CPES, allows characterization of the devices under full current and voltage conditions, such as pulse testing and four quadrant high power testing. The principal circuit diagram of the tester is shown in Fig.3.2.1. In addition to the module under test (S1, D1, S2 and D2) it consists of a low power, variable-voltage, dc power supply, load inductor L, reset resistor R, gate drivers, and control signals with programmable waveforms.

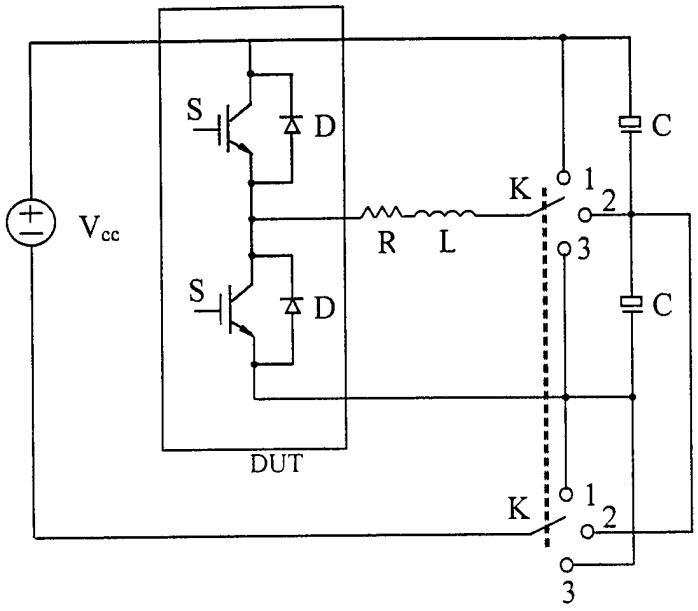


Fig. 3.2.1 A universal testing setup

The device under test (DUT) is located on an aluminum heat sink. In order to reduce parasitic inductance in the testing circuit, laminated bus plates are used to connect the power supply and the DUT. By the connection combinations shown in Fig.3.2.2 and Fig.3.2.3, S_1&D_2 and S_2&D_1 can each be tested under pulsed test conditions separately. Due to the duty cycle of less than 1%, the total power dissipation in the DUT is so low that its temperature could be assumed to be equal to the temperature of the heat sink(cooled by a fan) . For high temperature testing, the heat sink is placed on a hot plate to reach the preset temperature. A thermal probe is used to monitor the temperature of the heat sink during the whole testing.

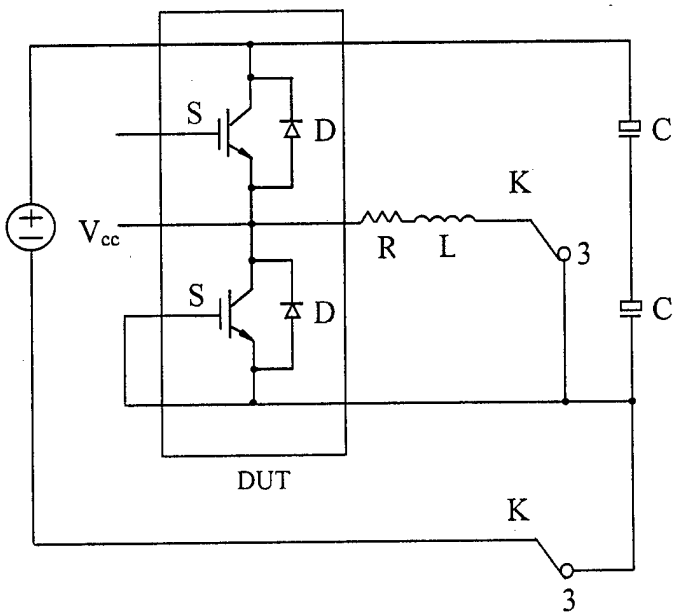


Fig. 3.2.2 Testing setup for S_1 and D_2

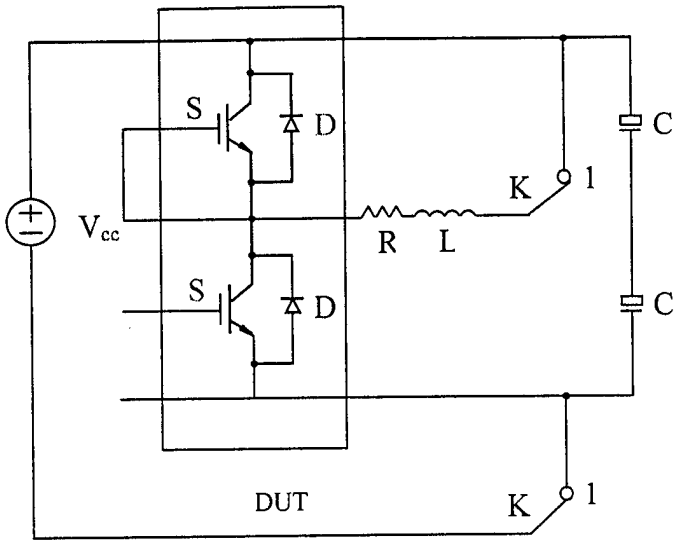


Fig. 3.2.3 Testing setup for S_2 and D_1

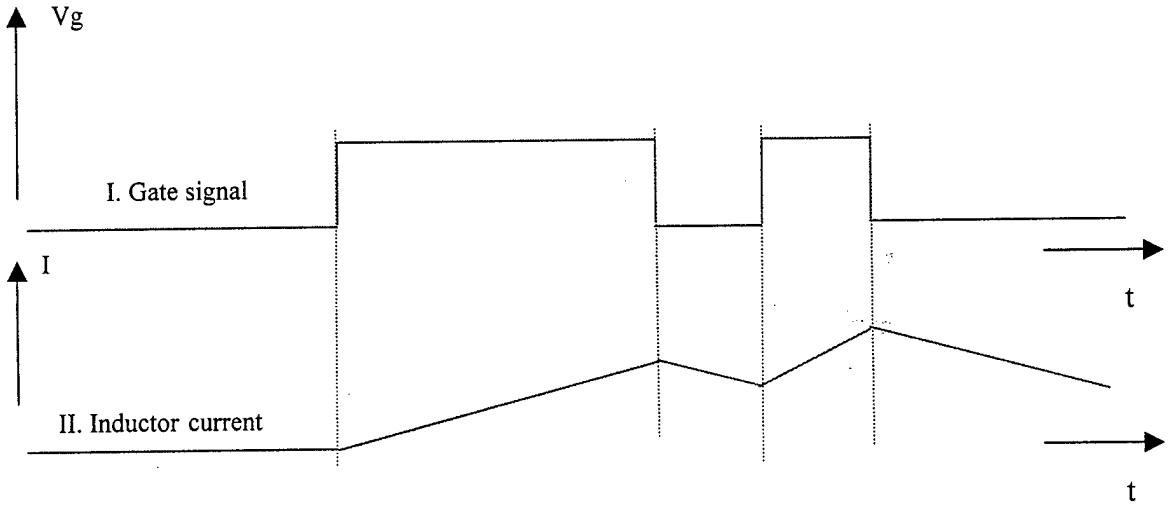


Fig. 3.2.4 Key testing waveforms

In Fig. 3.2.4, the key waveforms for measuring turn-on and turn-off losses under hard-switched conditions are shown. At T_1 DUT switch is turned on, and the load inductor current is built up from zero until T_2. At T_2 DUT is turned off, and the turn-off loss is measured at T_2. At T_3 DUT is turned on again; the current in the diode is shifted to the switch, which causes the reverse recovery of the freewheeling diode. Turn-on loss is measured at this moment. In the design of the signal generating circuit, T_2-T_1 must be long enough to let the inductor increase its current to an expected value; T_3-T_2 should be long enough so that before the turn on of switch at T_3, the switch is totally off, which means, T_3-$T_2 > T_{off}$.

Fig. 3.2.5 is the setup for device high power testing. Instead of high voltage power supply for the testing, a lower voltage one is used. For instance, 800V bus voltage is required for 1200V CPES -IGBT module testing, here only a 400V power supply is needed due to the voltage boosting converter setup.

Generation of control signals for pulse testing and high power testing are shown in Fig.3.2.6. A variable frequency clock signal is created first, then this signal is sent to the control signal generator as the input clock as shown in Fig.3.2.7. The signal generator produces the necessary signals for the gate drivers.

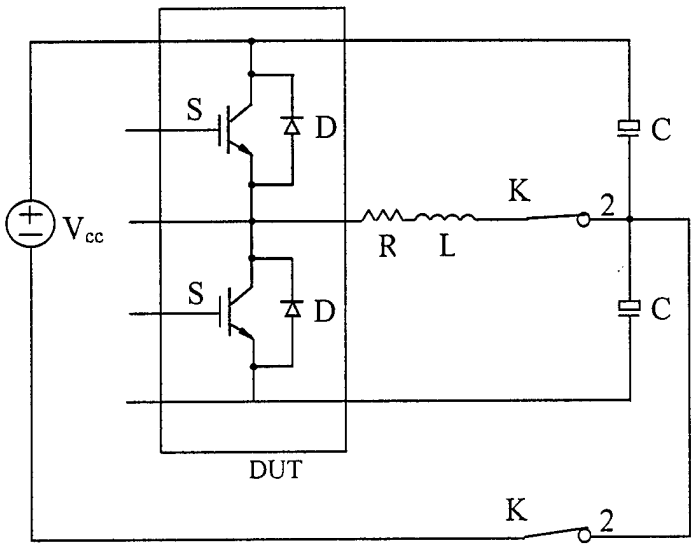


Fig. 3.2.5 Setup for high power testing

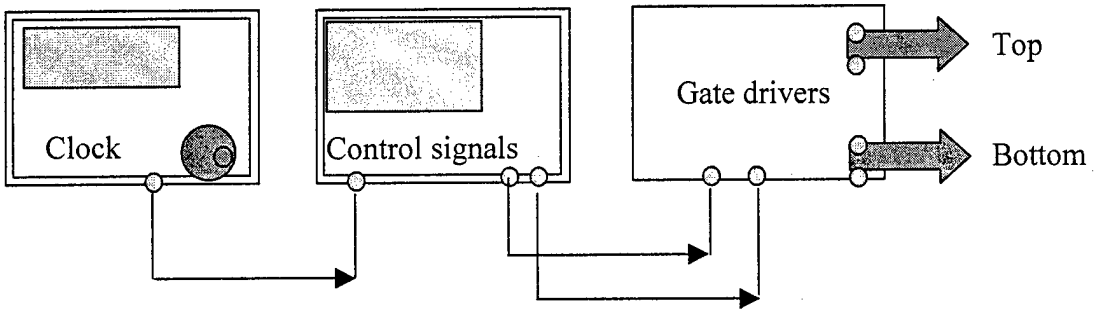


Fig. 3.2.6 Control signal generation

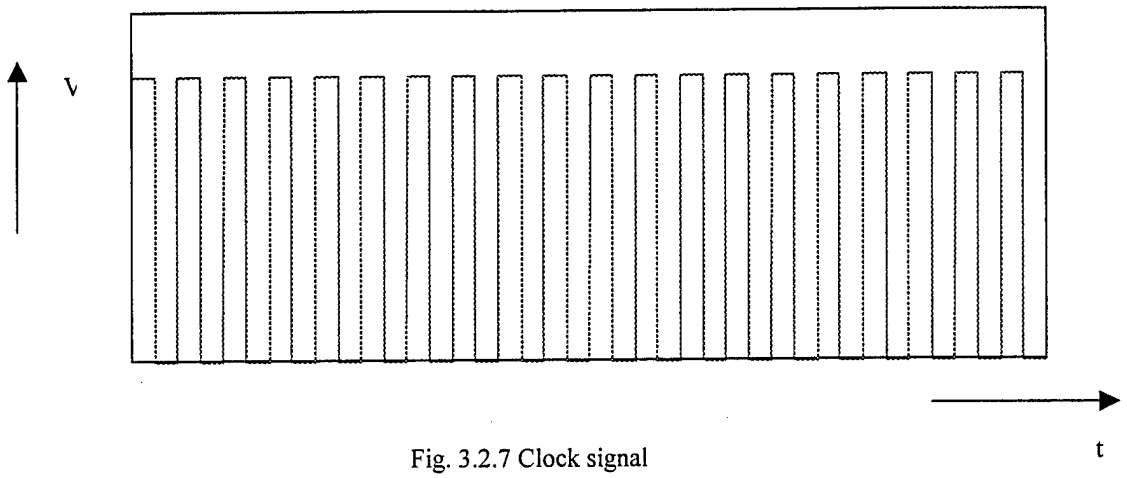


Fig. 3.2.7 Clock signal

In the control signal generator, two signals for the top and bottom switches are generated as given in Fig.3.2.8 and Fig.3.2.9 according to the embedded program. An HP8175A is used as the digital signal generator. In order to have a sinusoidal current in the load inductor, the control signal x(t) is a sine wave and the pulse widths are sinusoidally modulated

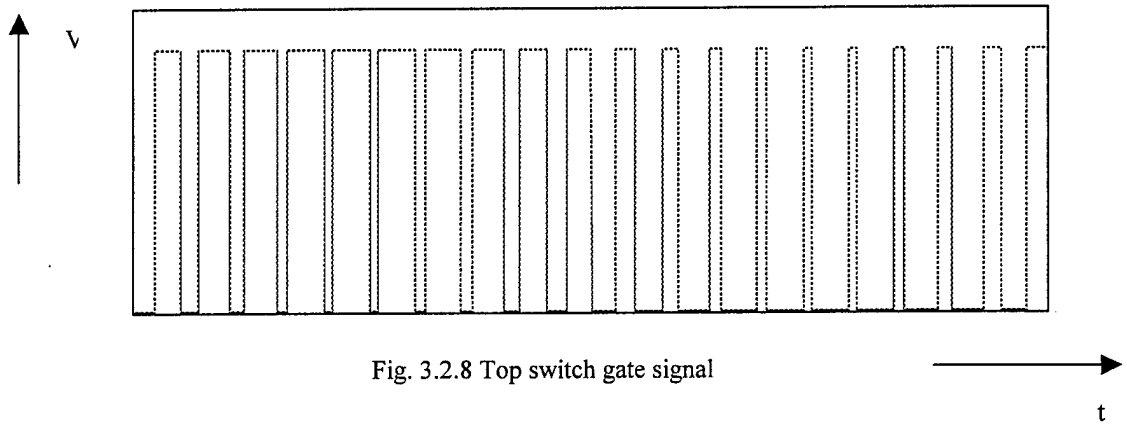


Fig. 3.2.8 Top switch gate signal

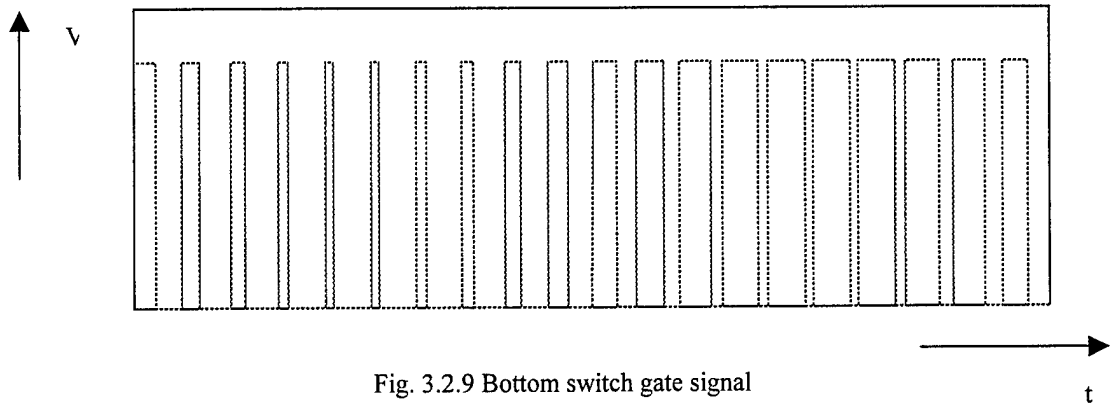


Fig. 3.2.9 Bottom switch gate signal

3.3. Generic Design Software for Integrated Resonant Modules

3.3.1 Introduction

As explained subsequently the design of an integrated LC module is generally time-consuming due to the many possible designs, dependent on the selection of magnetic core, dielectric material, current density, etc.. An interactive user-friendly software with comprehensive material libraries have been developed and serves as powerful support for LC design.

The software, based on MATLAB, has been developed to output a range of designs with the material characteristics, the technology constraints and the required electromagnetic characteristics as input. With these inputs, the software package can output a range of designs with variable form factors, each having different losses. Fig. 3.3.1 shows the design procedures and the final results output. The software also has a design optimization toolbox, which plots the design volume and estimated power loss etc. with structural parameters for each design. An example of this type of output is given in Fig. 3.3.2.

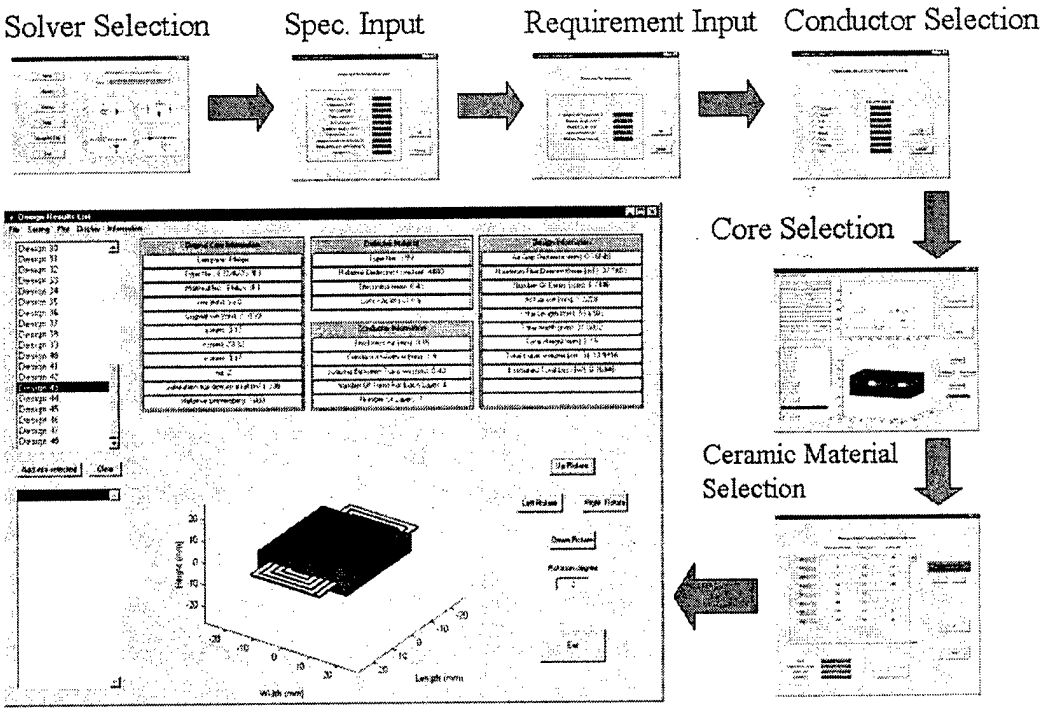
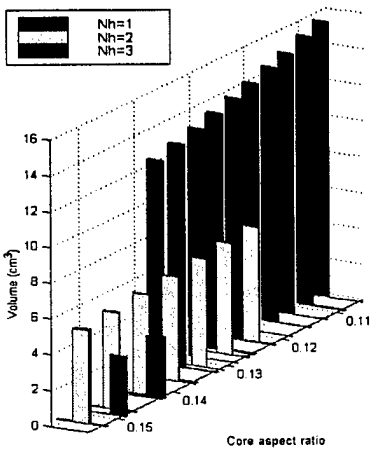
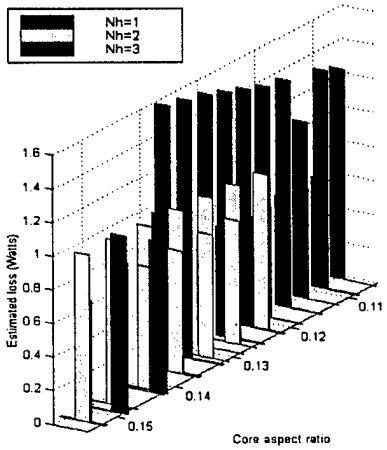


Fig. 3.3.1. LC design procedures and final results output



(a). Volume vs core aspect ratio with various number of layers (Nh)

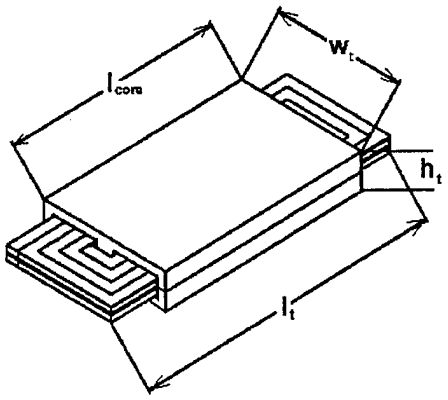


(b). Estimated power loss vs core aspect ratio with various number of layers (Nh)

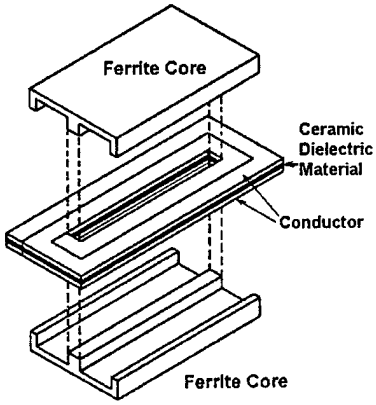
Fig. 3.3.2 Typical design optimization toolbox results.

3.3.2 The design problem for integrated resonant circuits

The integration of LC series resonant circuit in resonant and soft-switching power electronic converters has been reported previously [1]-[4]. As an alternative to a discrete inductor and capacitor LC resonant circuit, a planar integrated LC resonant module has demonstrated promising merits for power electronic applications [2]. An integrated series resonant module (ISRM) is based on planar ferrites, flat conductors and high permittivity ceramic type dielectrics, as shown in Fig. 3.3.3. Though only one layer is shown in this figure, a multi-layer structure is widely used in ISRM technology.



(a) Overview



(b) Exploded view

Fig. 3.3.3 Structure of a planar integrated LC resonant module.

Taking into account of the skin effect, the conductor thickness h_c is generally set to 1-2 times the skin depth at resonant frequency. Normally, an h_c of less than 150 μm is preferred. Therefore, h_c is selected as about 1 time of skin depth.

With the current density J fixed, the conductor width

$$w = \frac{I_{rms}}{h_c J} \tag{1}$$

From given I_{pk}, L and $B_{\max}$, the core middle leg cross-section area

$$A_{core} = \frac{I_{pk} L}{B_{\max} N_t} = l_{core} w_{core} \tag{2}$$

in which l_{core} is the length of the core middle leg, w_{core} is the width of the core middle leg.

The air gap distance

$$l_g = \frac{\frac{\mu_0 \mu_r N_T^2 A_{core}}{L} - l_e}{\mu_r - 1} \tag{3}$$

The current density J is normally 2-10 A/mm^2 in LC resonant module design. One has to make sure that $B_{\max}$ is within the core saturation flux density as well. The selection of J and $B_{\max}$ is a trade-off between both volume and power loss. Fig. 3.3.4 and Fig. 3.3.5 illustrate the impact of various $B_{\max}$ and J on total volume and quality factor. From Fig. 3.3.4, it is apparent that the volume can be reduced by selecting a higher current density J and a higher $B_{\max}$ in most cases. On the other hand, a higher J may lead to a lower Q at low $B_{\max}$ but a higher Q at high $B_{\max}$. Taking into account the actual core size, current density J is chosen as 9.3 A/mm^2 and $B_{\max}$ 300mT as an example for a design. From (1), based on the selected J and h_c, a conductor width 32mm can be obtained.

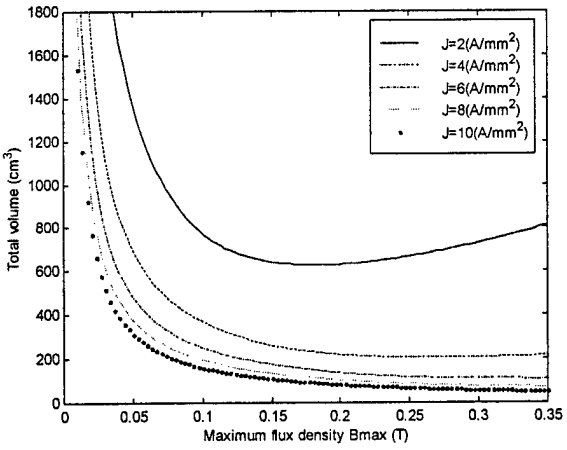


Fig. 3.3.4 Total volume versus $B_{\max}$ characteristics with various current densities.

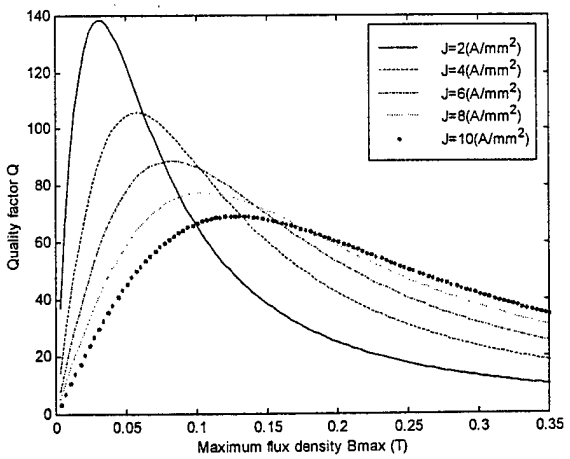


Fig. 3.3.5 Quality factor versus $B_{\max}$ characteristics with various current densities.

The cross sectional view of a planar integrated resonant module and the definitions of the variables as used in the software are shown in Fig. 3.3.6.

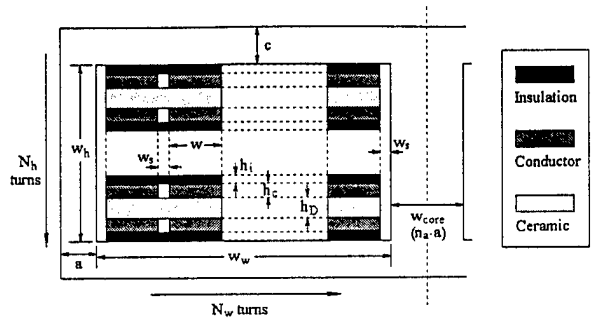


Fig. 3.3.6. Cross sectional view of a planar integrated resonant module.

The total length of conductor

$$l = N_t\left(2(w_{core} + l_{core}) + 4N_w(w + w_s) + \frac{(4N_w - 1)w_s}{N_w}\right) \tag{4}$$

To form the capacitor C, the total conductor area

$$A_D = l \cdot w = \frac{C \cdot h_D}{\varepsilon_0 \varepsilon_{rD}} \tag{5}$$

The flow diagram for the software is given in figure 3.3.7.

3.3.3 Application

The software has been applied to the design of several modules, one of which is being reported subsequently. Although the software at present calculates a temperature profile for a cross section of the module, it is being upgraded with more advanced heat generation models.

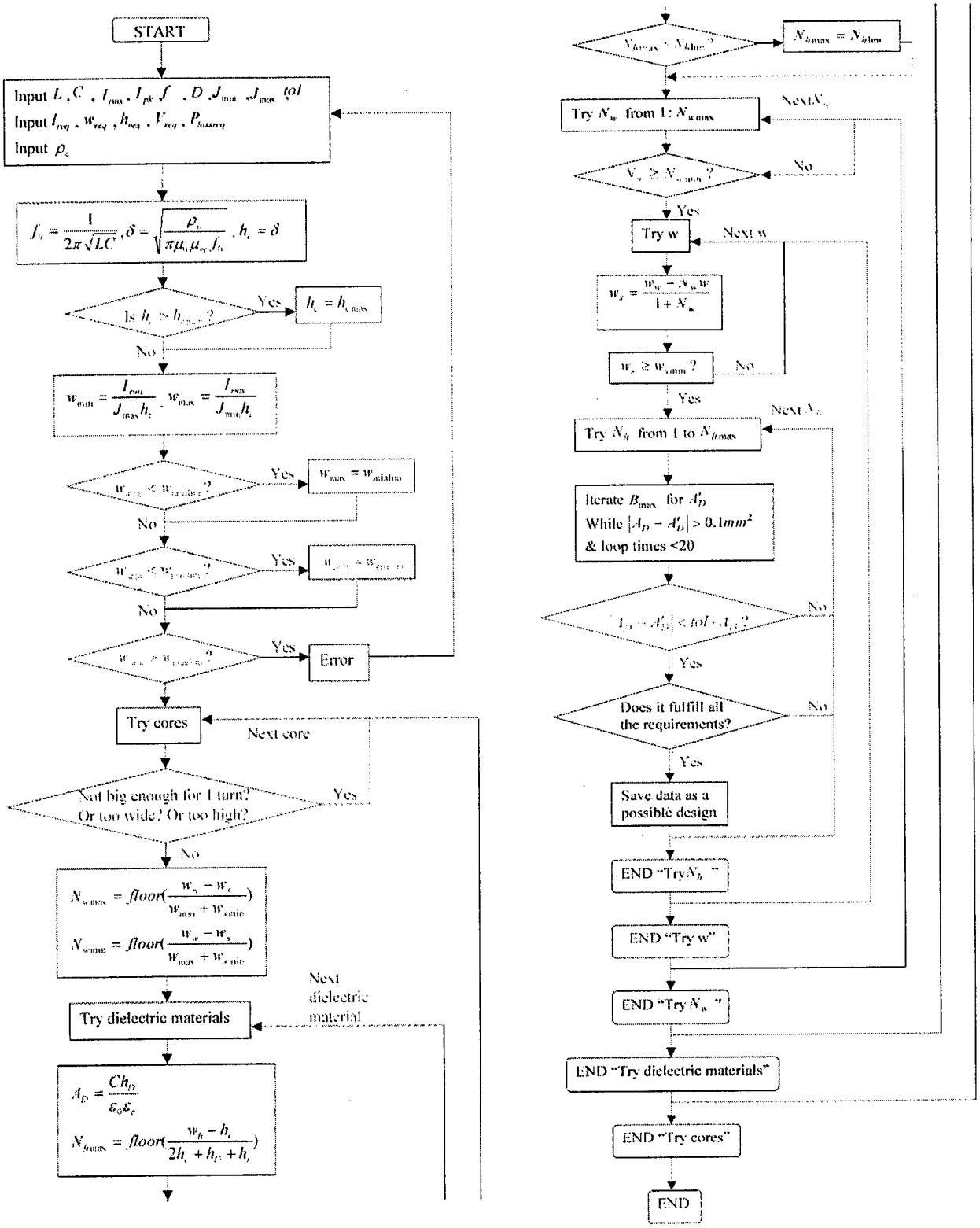


Fig. 3.3.7. Flow diagram of the software.

IV. REPORT ON DELIVERABLES FOR YEAR II

4.1 Packaging Approaches

The CPES research team believes that the highest potential for significant improvements in the performance and efficiency of power electronics modules lies in the development of alternative approaches to module packaging. The research team continues to explore several alternatives, including the previously reported MPIPPS and MLIT (now Embedded Power), as well as the Power Overlay technology, which is being investigated in a cooperative arrangement with GE CR&D. GE CR&D has already committed to transfering the Power Overlay technology as a part of the joint work in the NSF Center for Power Electronics Systems (CPES).

This section focuses on the packaging technology development and evaluation of these approaches, including physical layout and design, fabrication and process development, and package evaluation and testing. It concentrates on the issues associated with interconnecting the high-current busses, power devices and gate drive control circuitry and integrating them into a package to minimize parasitic losses and maximize both thermal conductivity and device density.

4.1.1 Thrust 1: MPIPPS Packaging

Our original design, called Metal-Post-Interconnect-Parallel-Plate-Structure (MPIPPS), shown in Figure 4.1.1.1, is a low-cost approach for packaging high-performance modules of power electronics building blocks (PEBBs). The design concept is based on the direct-bonding of copper posts, not wire-bonding of fine aluminum wires, to interconnect power devices.

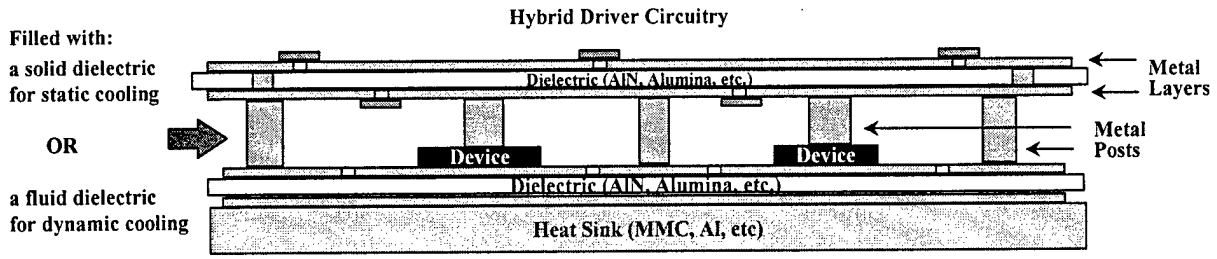


Figure 4.1.1.1 MPIPPS cross-section structure.

In last year's report we expressed our disappointment in not being able to create a solderable metal bond pad surface on purchased die in spite of much development work on the process. This year we were able to obtain solderable devices from IXYS which has allowed us to resume this approach. Figure 4.1.1.2 shows the first prototype MPIPPS module built with these devices and figure 4.1.1.3 shows the performance characteristics.

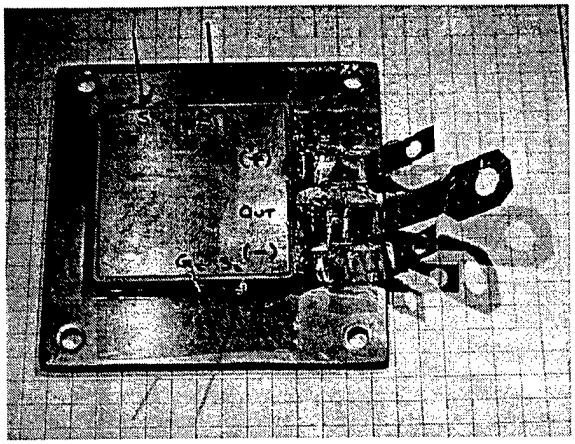
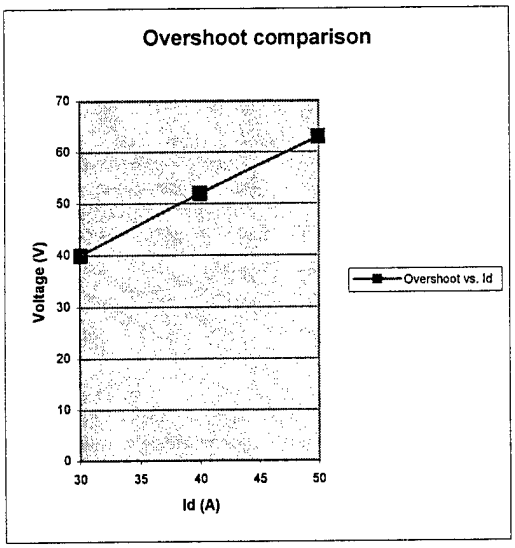
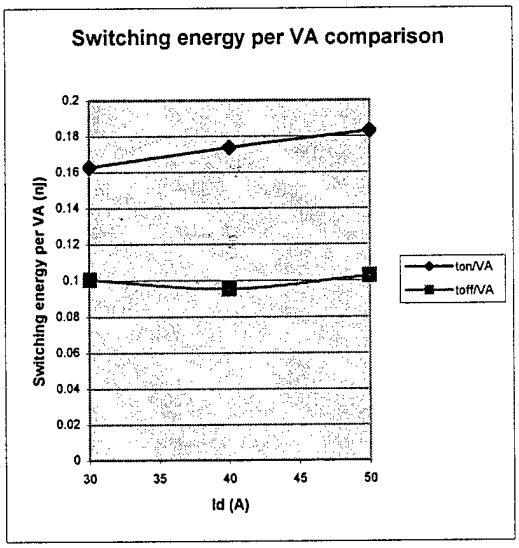


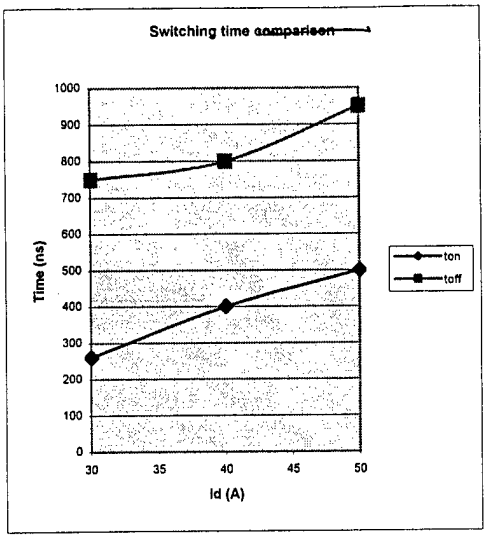
Figure 4.1.1.2 Prototype MPIPPS module

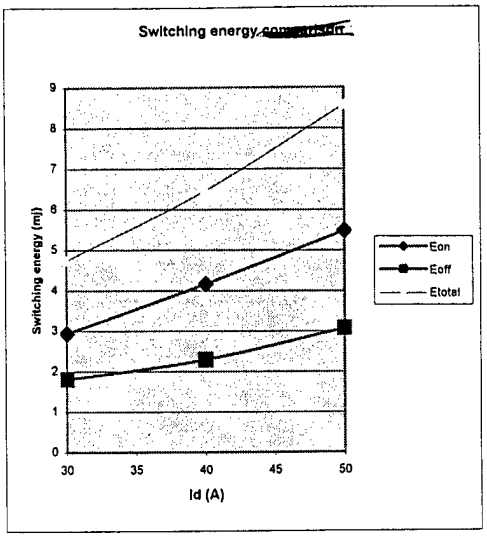


a. Switching time



b. Switching energy





c. Turn-off voltage overshoot

d. Switching energy per VA

Fig. 4.1.1.3 Testing results for the MPIPPS module

Solderable Device Characterization

After we received the solderable devices from IXYS, we did careful characterization. We first used a low power curve tracer to screen all the devices. We then put protective coating on the devices since we found that the breakdown of the IGBT device tended to be lowered after the solder reflow process if there is no protective coating. The polymer protective coating was applied with conventional screen-printing. Photolithography allowed definition of openings in the protective coating for the device pads. Fig. 4.1.1.4 shows the as received solderable IGBT device and one after applying a protective coating. In order to fully test the devices at high power and get ready for the next assembling process, we either attached metal posts on the device pads or formed solder bumps on the device pads by a reflow process. Fig. 4.1.1.5 shows the metal posts on the IGBT pads. The device has six source pads and one gate pad on the topside and the drain on the bottom. Fig. 4.1.1.5(a) shows seven individual metal posts (1 mm x 1mm x 2mm) that were soldered onto the source and gate pads, while Fig. 4.1.1.5(b) shows a single seven-post assembly soldered onto the device. Fig. 4.1.1.6 shows the solder bumps on the device pads. The solder bumps are achieved by reflowing solder paste and solder balls onto the device pads. The as-packaged devices, which are essentially chip-scale packages, can be readily tested on a high-power curve tracer for static performance. This possibility establishes a route to obtain known good die. Our experiments showed that the blocking voltage of the IGBT devices remain the same as those before processing.

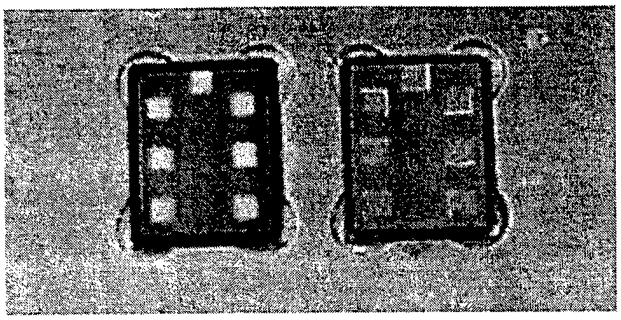
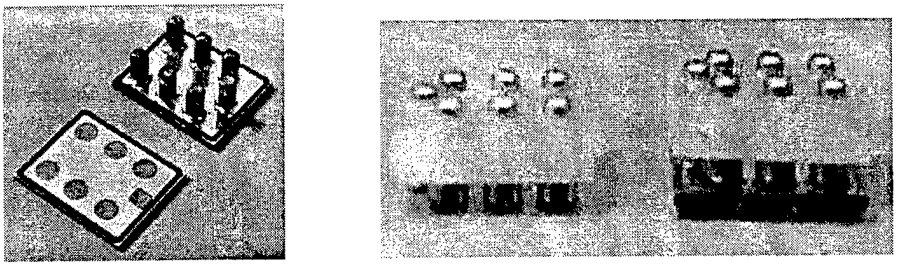


Fig. 4.1.1.4 As received solderable IGBT device (the right one) and one IGBT after putting protective coating (the left one).



(a) (b)

Fig. 4.1.1.5 Soldered metal–post interconnection of IGBT with (a) seven individual metal posts and (b) a single seven-post assembly.

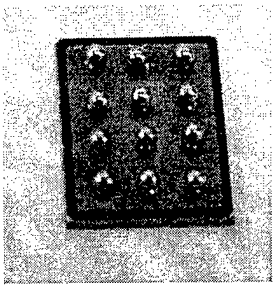


Fig. 4.1.1.6 Solder-bump interconnection of power device.

The ability to have known-good-die (KGD) before packaging them into a multi-chip module is highly desired for MCM packaging. Supply of KGD helps lower the cost for manufacturing MCMs by cutting down the intermediate testing and rework time during module fabrication. However, cost-effective burn-in and test technologies leading to KGD are still under development. This is especially true in power electronics, where testing bare dies (such as MOSFETs, IGBTs) at levels of several hundred to thousand volts and hundreds of amps is currently impossible. The chip-scale packaging of the power devices as shown in Figs. 4.1.1.5 and 4.1.1.6 offers a potential solution for known-good power devices since the packaged devices can be readily handled and tested at full power ratings on a pulsed basis. It also makes it possible for the power-processing elements of a power module to be in the form of low-profile surface-mount packages.

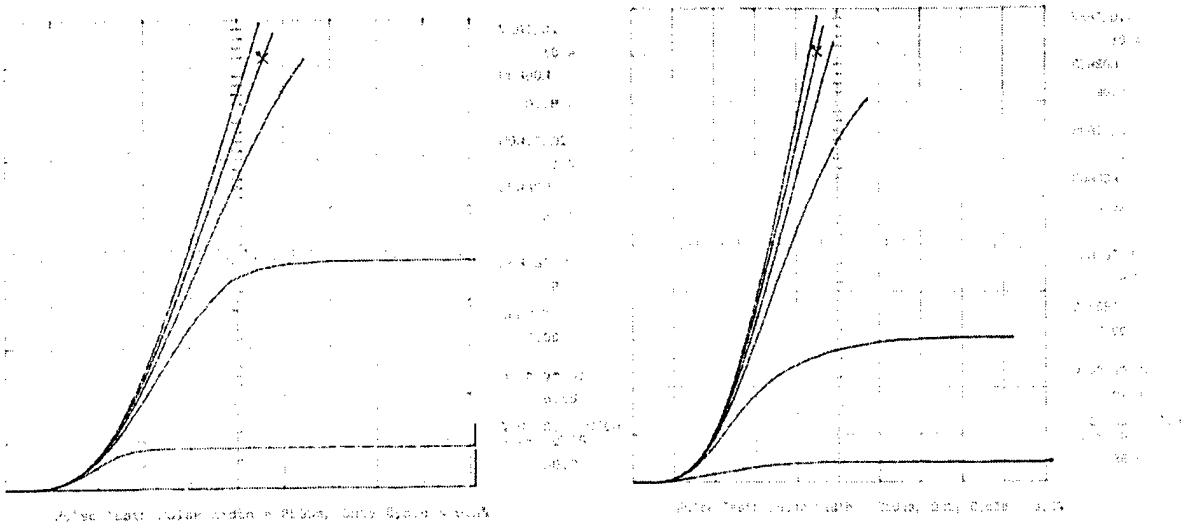
Static test

Chip-scale packaged (CSP) IGBT and commercially packaged IGBT from vendors in the form of TO-247 packages were evaluated using static testing. For the above mentioned packages, the same IGBT die are used which we bought from the same vendor. SONY Tektronix 371 programmable high power curve tracer was used to conduct the static tests. The test condition was: pulse width of 250 μs, duty cycle lower than 0.5%. Five samples of each kind of packages (commercially packaged IGBT, chip-scale packaged IGBT) were tested. The results are consistent with the tolerance under 5%. The IGBT die we used is a high speed IGBT. Its I_C versus V_{CE} curve is almost linear in the active region, thus we can define the amount of change in V_{CE} by the amount of change in the collector current I_C as on-state resistance R_{on}. Table 4.1.1.7 is typical test data for CSP IGBT and commercially packaged IGBT and figure 4.1.1.8 shows the typical saturation characteristics curves of CSP IGBT and commercial packaged IGBT. We can see that CSP IGBT has the lower voltage drop and on-state resistance (even lower than what data sheet claims). Compared with the commercially packaged IGBT, the $V_{CE(sat)}$ and R_{on} of CSP IGBT are improved by about 17-20% and 30%, respectively.

Both posted and solder bumped power device chip-scale packages have lower conduction resistance because of the elimination of the wirebonds and other external interconnections such as the leadframe. Conduction resistance is a critical parameter as it determines on-state power dissipation. A lower voltage drop means lower losses and higher efficiency.

Table 4.1.1.7 Typical static test data of various power devices and modules

	$V_{CE\ (sat)}$ (V) ($I_C \approx 35$ A) ($V_{GE}=15$ V)	$V_{CE\ (sat)}$ (V) ($I_C \approx 90$ A) ($V_{GE}=15$ V)	Ron (mΩ) ($I_C \approx 90$ A) ($V_{GE}=15$ V)	$I_{C(on)}$ (A) ($V_{GE}=15$) ($V_{CE} \approx 10$ V)
IGBT chip (Data sheet)	3.1	X	X	X
Commercial packaged IGBT	3.5	5.6	37	158
CSP IGBT	2.9	4.5	26	211



(a) (b)

Figures 4.1.1.8 Typical saturation characteristic curves of (a) Commercial packaged IGBT and (b) CSP IGBT.

Year II task summary for Thrust 1 work plan

Task 2.1.1 Fabrication of a phase-leg MPIPPS module has been completed.

Task 2.1.2 Comparative analysis of thermo-mechanical modeling with thermal cycling study has not yet been completed.

Task 2.1.3 Electromagnetic and electrical characterization has been completed.

Task 2.1.4 Final evaluation of upscaling has not been completed.

4.1.2 Thrust 2: Embedded Power

Introduction: From MLIT to Embedded Power

Last year we reported that we have developed a Multilayer Integrated Technology (MLIT) for packaging Power Electronics Building Blocks (PEBBs). After one year technical modifying and optimizing we developed an upgraded version of this technology – Embedded Power, which is a hybrid MCM-based integrated packaging approach to assembly bare power die and components into a blocks without wire-bonds. Fig. 4.1.2.1 shows the conceptual structures in the Embedded Power packaged module. It consists of three parts – embedded power stage, electronics circuitry and substrate, which are soldered together to build a module. The electronics circuitry includes gate driver, controller and protection components. The

base substrate provides electrical interconnection and thermal path of power chips. The core element in this structure is the embedded power stage that comprises of ceramic frame, power chips, isolation dielectrics and metallization circuit. This element supports a high-density interconnection of PEBBs.

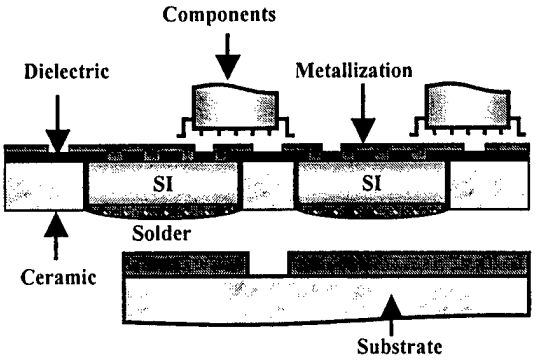


Fig. 4.1.2.1 Schematic structure of Embedded Power PEBB

When all three parts are assembled together we can see an identical multilayer structure to the one in MLIT as reported last year. Through this modification, the feasibility of this technology and reliability has been largely improved.

As integration objective we focused on assembling PEBB modules with bare chips of semiconductor power devices. The power device chips such as IGBTs and MOSFETs commercially supplied offer a vertical semiconductor structure in which the electrode pads are arranged on two sides. Fig.4.1.2.2 shows the cross-section of a typical IGBT chip. Usually, the gate, source or emitter pads (mostly metal Al for wire-bond, non-solderable) are on the top surface, and Ag or Au solderable drain or collector pads are fabricated on the

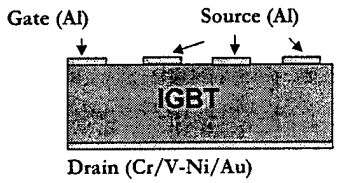


Fig. 4.1.2.2 Cross-section schematic of IGBT

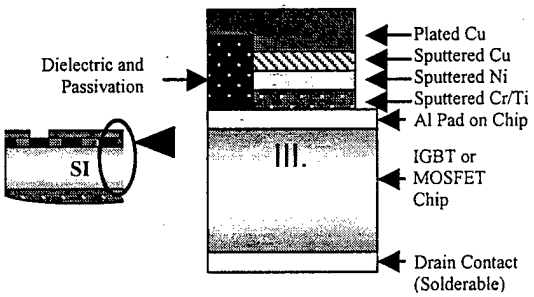


Fig. 4.1.2.3 The contact scheme in Embedded Power module

bottom of the chip. This structural feature can be employed to build a sandwich type module. Furthermore, a novel 3-D MCM interconnection structure can be realized with stacked isolation and conductive layers, as shown in Fig 4.1.2.1. Fig. 4.1.2.3 shows the details of the pad contact and isolation scheme.

The main features of this technology are the use of ceramic plate with openings as a chip carrier, in which the bare power dice are buried and encapsulated with a screen-printed dielectric. This screen-printable polymer with via holes is used for electrical isolation of multiple circuit planes in the 3-D module construction. The designed metallization layout is deposited to build high-density interconnects between power devices and electronic circuitry. The benefit of using ceramic plates in the structure is the potential for incorporating passive components, generally in the planar form, into the modules, as well as high-density hybrid circuitry. Because the height of deposited-film interconnects can be made very small, and

sandwich power bus layout can be easily realized, much lower parasitic inductance is expected along with improved heat dissipation through the joints.

Technology Development

The implementation of the proposed Embedded Power concept necessitates an understanding of the electrical and thermal characteristics for the multilayer structure. Simulation tools have been used for analysis and optimization. Materials used in the structure must offer good comprehensive performance including mechanical, electrical and thermal, as well as processing properties. Experimental investigation methods were mainly employed to tailor and apply these advanced materials.

The multilayer structure of the Embedded Power module was shown in Fig.4.1.2.1. The main issues we have addressed include high current and high voltage capabilities of the interconnect system, high thermal dissipation and structural integrity. Electrical simulation for high performance and thermal-mechanical analysis for high reliability have been done. The final material combination and contact scheme in the structure are as follows:

The power chips are embedded in a ceramic carrier by filling the gap. A selected dielectric layer is coated on the chip surface with openings on pads. This interlayer provides encapsulation for electrical insulation of power devices and other circuitry. A deposited metal (Cu) circuit (pattern) is designed to connect the open Al pads (after dielectric coating) of the power chips to external driver/control and protection circuitry. The die pad metallization schemes used widely in IC packaging are employed in our approach to accomplish this metallurgical interconnect. Die pad metallization schemes such as Ti-Ni-Cu or Cr-Ni-Cu layers provide low film stress with good adhesion and electrical/thermal conduction. For high current requirements, an electro-plated Cu layer is added to the thin sputtered Cu layer of the UBM scheme as shown in Fig.4.1.2.3.

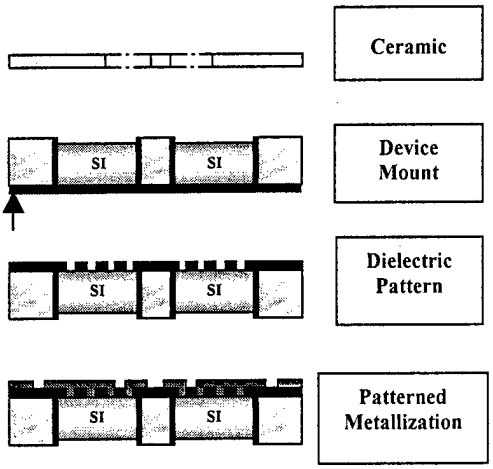


Fig. 4.1.2.4 Process flow chart of Embedded Power

Step Description	Issues & Solution
1:Ceramic frame	Openings in flat AlO or AlN plate by laser cutting
2:Die mount	Dispense dielectric
3:Dielectric pattern	Void-free precision dielectric pattern, Good adhesion & CTE match by screen printing or/and photolithography
4:UBM contact/ Metallization	Adhesion, barrier, low stress, Low resistance by sputtering of Ti/Cr-(Ni)-Cu thin film
	Thicker(>5mil), low stress, Low resistance, solderable, Precision pattern by Electroplating of Cu+Electroless plating of Ni, Etching

Table I Processing scheme of Embedded Power

The key to accomplish the Embedded Power concept is the application of selected materials into the designed structure. The packaging technologies for power electronics have not kept pace with those of low power electronics, like the packaging of microelectronics. But existing thin- and thick-film process methods can be modified and optimized to apply in power packaging. These efforts can also result in cost-effective technology for large production volumes. Fig.4.1.2.4 illustrates the process flow chart of Embedded Power technology. Table I lists the designed fabrication steps of Embedded Power stage including issues and specific processing solutions. We have experimentally investigated and compared different alternatives for each processing. Finally an all-low temperature (<250°C) hybrid technology to fabricate the Embedded Power stage has been used. It consists simply of ceramic cutting, device mount, dielectric printing and multilayer metallization.

Experimental Investigation and Application of Embedded Power

Two power electronics modules were chosen as prototypes to demonstrate the feasibility of this technology and address potential technical issues.

IGBT-based PEBB module

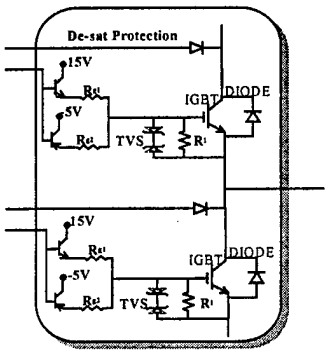


Fig. 4.1.2.5 Circuit diagram of Embedded Power packaged PEBB

Fig.4.1.2.5 shows the schematic of the packaged circuit for PEBB module. It is a one-phrase DC/AC converter consisting of two IGBTs and two diodes with a few driver components. The performance goals are 800V DC bus, 20KW power and 20kHz frequency. The IGBT and diode is IXYD35N120A (1200V/70A) and C-DWEP69-12S (1200V/70A), respectively, both from IXYS. The size of all chips is 7.9X9.1 mm^2. There are six-emitter Al pads (1.1×1.1 mm^2) and one-gate Al pad ($1.1\times1.1mm^2$) on the upper side of each IGBT. A larger Ag pad on the upper side of the diode is $7\times8.5mm^2$. The backsides of all device chips are gold metallization as drain or cathode, which is solderable and can be directly soldered to the substrate. The driver components are surface mountable. To assemble all these components in one module using Embedded Power technology, a 2"X2" Al_2O_3 ceramic plate was chosen as chip-carrier and a 2"X2" Al_2O_3 DBC was used as the base substrate.

The one characteristic of Embedded Power is its mask-based processing. The base substrate and metallization circuit are etched by photolithography technique. Dielectric polymer is applied with a screen-printing method and the chip-carrier is fabricated by computer controlled laser cutting. So a set of masks incorporating the designed layout is needed first. Fig.4.1.2.6 shows the designed layout and patterns for every single step of the process.

Ceramic plate with a thickness of 25 mils has been machined to have four middle openings for mounting power chips and three edge windows for fixing three power terminals. After mounting the chips by dispensing dielectric paste in the gaps, the whole surface was coated with screen-printed dielectric polymer. The designed screen is 80-mesh, and emulsion thickness is 2 mils. The screen pattern ensures that all pads on the IGBTs are open. Six via holes were made on each diode to obtain balanced distribution of current between the IGBT and the diode. Then the top metallization was fabricated. A Ti or Cr (500Å) adhesive layer, a Ni (500Å) barrier layer and a seed layer of Cu (1000Å) were sputtered on the whole surface after plasma cleaning of the Al pads. The thickness of this die pad metallization is not enough for the designed

current rate. Therefore, an electroplated Cu layer was added up to 5 mil thickness. In the experiment, photolithography was used to pattern all connect paths. The Cu is plated just on the effective area. After stripping off the photoresist, the UBM metallization in the non-plated area is etched by using another step of photolithography. Fig.4.1.2.7 shows the pictures of all four processing steps. Fig.4.1.2.8 shows the fabricated power stage and final module encapsulated and attached to the heat sink. Figure 4.1.2.9 gives the variation of switching parameters versus current. This illustrates that good electrical performance has been achieved with Embedded Power modules.

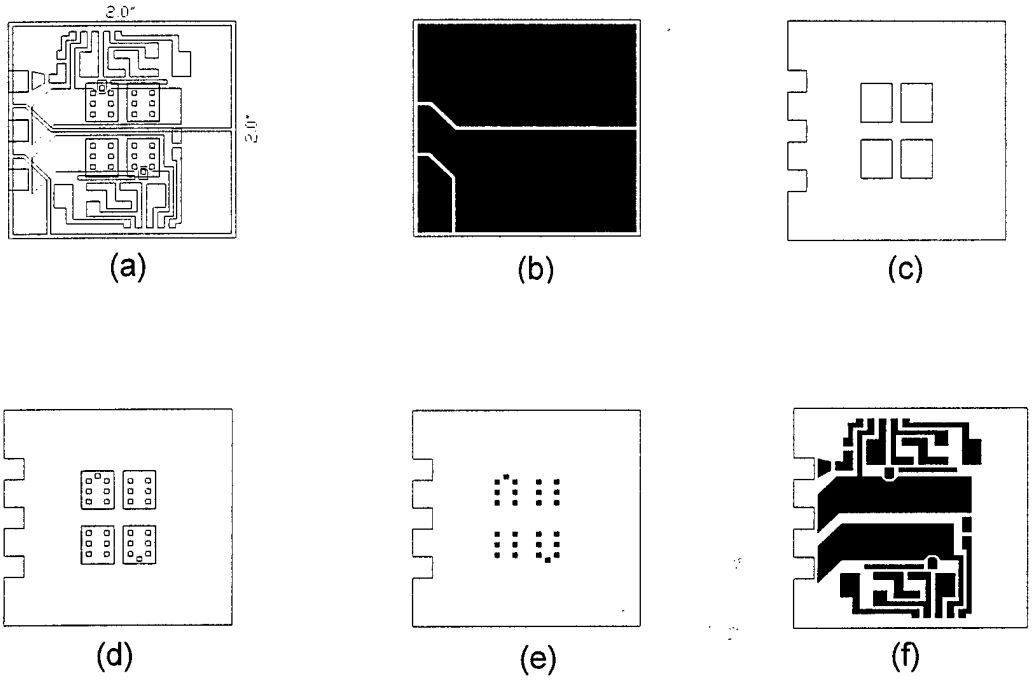


Fig. 4.1.2.6 (a) Layouts for multilayer in Embedded Power, (b) substrate pattern, (c) ceramic frame, (d) ceramic with chips, (e) dielectric pattern and (f) metallization pattern (circuit)

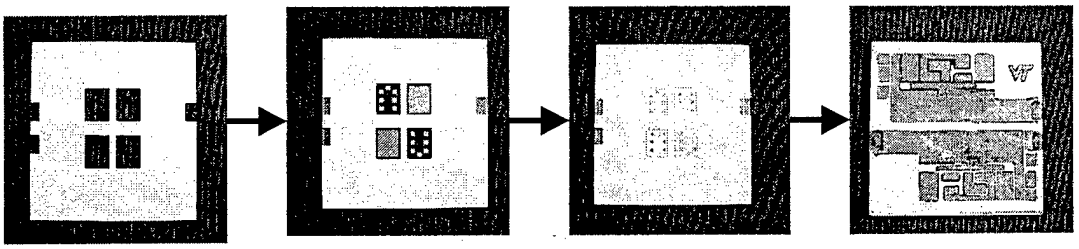


Fig. 4.1.2.7 Processing steps for fabricating Embedded power stage

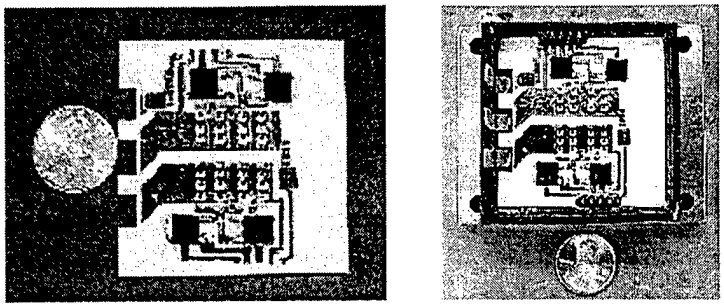


Fig.4.1.2.8 Embedded Power stage and surface mounted components and fabricated demonstration module

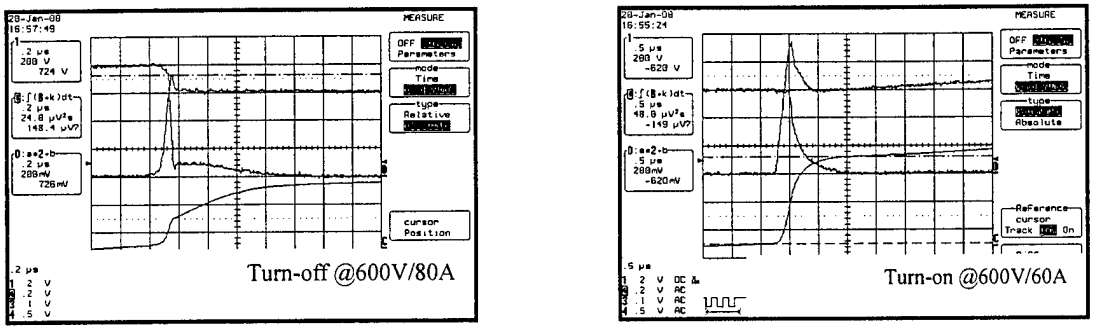


Fig. 4.1.2.9 Power switching characteristics of demonstration module

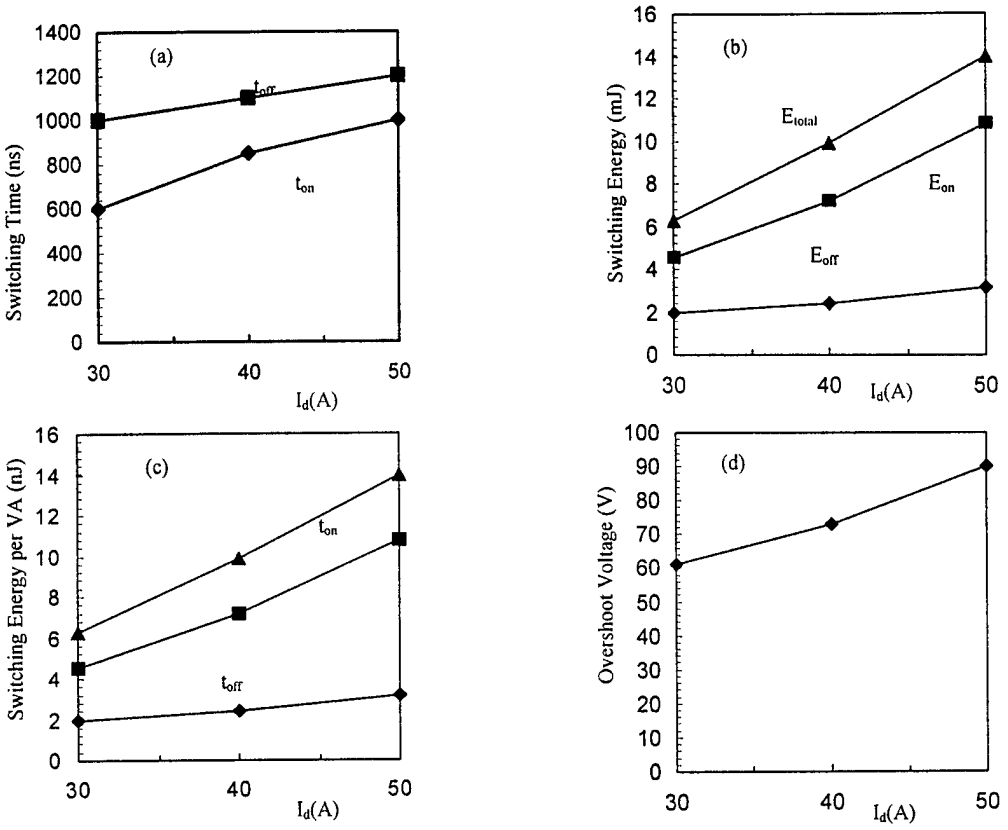


Fig.4.1.2.10 The variation of switching parameters Vs current

Year II task summary for the Thrust 2 work plan

Task 2.2.1	Fabrication of a phase-leg Embedded Power module has been completed.
Task 2.2.2	Comparative analysis of thermo-mechanical modeling with thermal cycling has not yet been completed awaiting receipt of thermal cycling equipment.
Task 2.2.3	Electrical characterization has been started but the electromagnetic characterization will be conducted in year III.
Task 2.2.4	Evaluation of Embedded Power as a PEBB technology, including up-scaling, has not been completed.

4.1.3 Thrust 3: Power Overlay (POL) Packaging

The Power Overlay (POL) Technology developed by the General Electric Company eliminated wire bonding through the use of metallized Cu vias/polyimide to realize power and control interconnection. Figure 4.1.3.1 shows a cross section of a Power Overlay module structure for power electronics application.

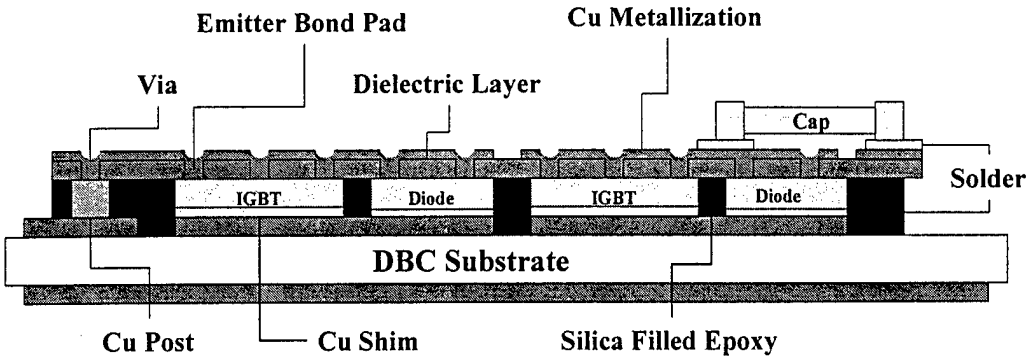


Figure 4.1.3.1 Cross-section view of GE Power Overlay module structure

GE Power Overlay has the potential of integrating power devices and some driver and control components with a low profile, high-density configuration. Its solderless interconnect makes it a possible candidate for high-temperature application. The evaluation of GE's Power Overlay Technology in the aspects of processing as well as its electrical, thermal and mechanical performance, and the exploration of GE POL technology on its low cost track with processing robustness and high reliability will extend our scope in developing advanced power packaging capability. Therefore, the high-density, low-profile package coupled with better electrical and thermal performances [7] makes POL itself a promising candidate for the application in PEBB technology.

Technical Approach

The processing steps for POL are shown in figure 4.1.3.2. Currently, processing steps performed at CPES include from via-punching to dielectric filling. Power semiconductor devices (IGBT, MOSFET, diode) are mounted to the backside of polyimide tape using adhesive. The polyimide tape has pre-formed vias with specific pitch and size. These vias serve as electrical path for circuit functioning. Topside of polyimide is then metallized through thin film deposition of Ti/Cu in sputtering machine. Subsequent electro-plating is performed to build a Cu layer of 2 to 4 mil on top of the sputtered seed metal. Circuit patterns are achieved by the application of photoresist and chemical etching process. DBC substrates are attached on the backside of devices through soldering.

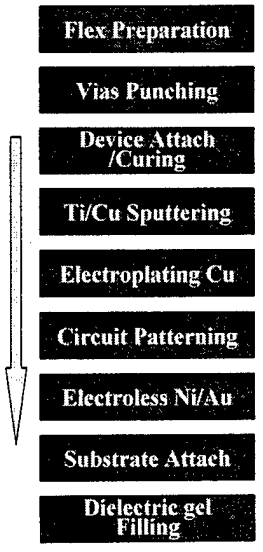


Figure 4.1.3.2 POL Processing

Via formation

We have set up pick-and-place equipment to achieve a device-to-polyimide attaching process. After the via formation on polyimide film, the devices need to be accurately positioned according to via location and glued to the polyimide. These vias will serve as power and control path in POL module.

Thin film deposition

This step forms a thin layer of metal on top of polyimide and the device pads. A Ti/Cu configuration is selected, according to GE's recommendation, to deposit first about 1000~2000 Å of Titanium, and subsequently deposit 2000~3000 Å of copper. We have configured and expanded our thin film deposition system with rotational sample holder that enables non-stop sputtering of up to 3 different target metals. We were able to achieve uniform deposition over the polyimide/via frame with low electric resistance.

Electroplating and patterning

In this step, metallization of up to 5 mil copper on the seed metal layer deposited on polyimide frame was achieved. A current density of 30A/ft^2 is used during plating. Bright, smooth plating was accomplished on our experimental samples. Photoresist definition and a spray etching method is used to pattern the plated copper layer with desired circuitry. The backside of the polyimide frame (with devices attached to it) is protected from the attack of etchant media.

Thermo-mechanical Modeling

In parallel with processing capability evaluation, the thermo-mechanical stresses on POL interconnects are

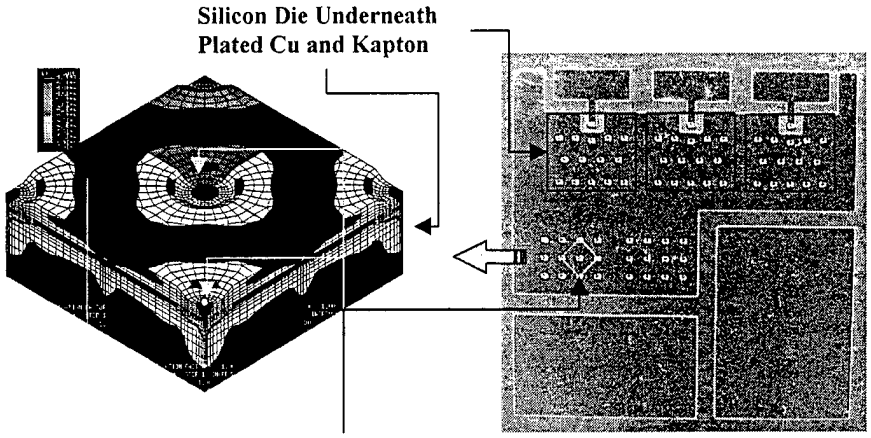


Figure 4.1.3.3 Stress distribution of POL

being evaluated using the numerical analysis programs PATRAN and ABAQUS. . Figure 4.1.3.3 shows a plot of stresses in POL interconnects with 50 mil via pitch, 20 mil via size and 2 mil polyimide thickness. Key parameters affecting the reliability of POL have been identified, including via pitch, via size, electro-plated copper thickness, polyimide thickness and material selection. Currently, all the models are studied under the condition of a thermal shock of 0~100°C.

Using linear elastic material properties for copper, kapton, solder, and aluminum nitride, initial results of thermo-mechanical stresses were obtained. All results show that high stress concentration most likely occurs at the peripheral of the vias. Examples of typical high stress patterns are shown in figure 4.1.3.4.

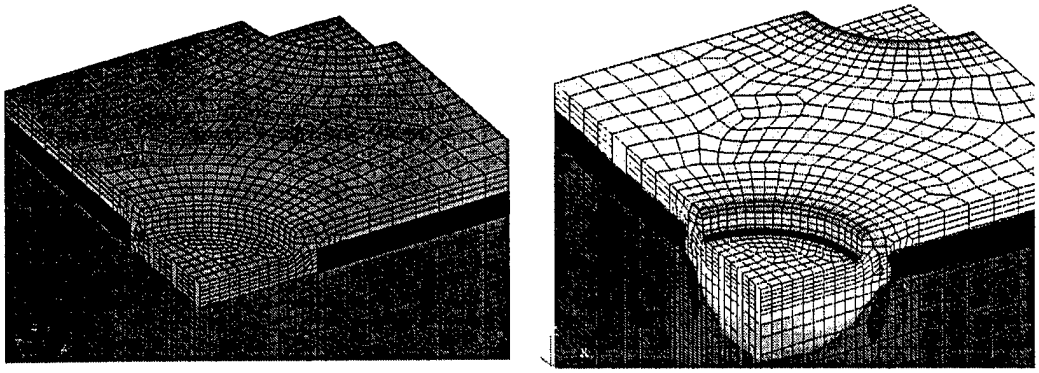


Figure 4.1.3.4 Material interface (left) and typical high stress pattern (right)

Table 4.1.3.5 lists some of the linear static results of the maximum Von Mises stress in POL models:

Table 4.1.3.5 Maximum stresses in POL models

FEM #	Cu Thickness (Inch)	Via Diameter (Inch)	Via Spacing (Inch)	Max. Von Mises Stress (ksi)
1	0.002"	0.020"	0.040"	**33.9**
2	0.002"	0.020"	0.050"	**34.7**
3	0.002"	0.040"	0.080"	**45.6**
4	0.002"	0.040"	0.100"	**46.8**
5	0.004"	0.020"	0.040"	**38.9**
6	0.004"	0.020"	0.050"	**39.4**
7	0.004"	0.040"	0.080"	**40.7**
8	0.004"	0.040"	0.100"	**41.2**

Future work will be to develop an analysis process simulating thermal cycling conditions for Power Overlay interconnect and include the consideration of visco-plastic properties of solder materials.

Year II task summary for the Thrust 3 work plan

Task 2.3.1 Fabrication of a phase-leg POL module has been completed.

Task 2.3.2 Comparative analysis of thermo-mechanical modeling with thermal cycling has not yet been completed awaiting receipt of thermal cycling equipment.

Task 2.3.3 Electrical characterization has been started but the electromagnetic characterization will be conducted in year III.

Task 2.3.4 Evaluation of POL as a PEBB technology, including upscaling, has not been completed.

4.1.4 Thrust 4: Passives Integration

This report presents exploratory work on the design of an ISRM for the auxiliary soft-switching circuit in a 100kVA 20kHz 3-phase ZCT inverter. One phase arm of this inverter is shown in Fig. 4.1.4.1. The specifications are shown in Table 4.1.4.2.

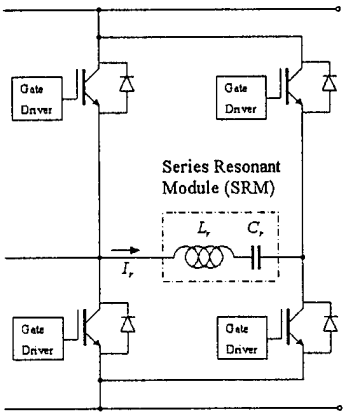


Fig. 4.1.4.1. One phase leg of the 3-phase ZCT inverter

TABLE 4.1.4.2
DESIGN SPECIFICATIONS

L	Inductance	$2\mu H$
C	Capacitance	$0.25\ \mu F$
I_{rms}	RMS current	$40\ A$
I_{pk}	Peak current	$240\ A$
D	Conduction duty cycle	0.12
f_0	Resonant frequency	$110kHz$
f	Operating frequency	$20kHz$

The design of this module was done with the software presented earlier in this report. Since a large number of designs result, the design chosen for assembly is indicated in figure 4.1.4.2

One example ISRM has been constructed with the design parameters shown in Table 4.1.4.7. The photo of the ISRM prototype is shown in Fig. 4.1.4.8 with dimensions indicated. The impedance analyzer testing result is shown in Fig. 4.1.4.9, from which it can be seen that the series resonance occurs at around 222kHz and the first parallel resonant frequency is at around 100 times the frequency. The curve below 3MHz can be well predicted by the model based on transmission line theory [3]. To test the dynamic response and quality factor of this module, a test circuit that adds up to 800 volts step voltage to the ISRM has been built. To clearly show the oscillation frequency and duration, the current response from a 100V step voltage input is shown in Fig. 4.1.4.10. Testing at higher voltages has also been done. It can be seen that the ISRM works very well as a high frequency resonator with an acceptable quality factor.

Table 4.1.4.7. Module parameters

w	Conductor width	$32mm$
h_c	Conductor thickness	$140\mu m$
w_s	Spacing between adjacent turns	$1.4mm$
N_h	Total number of layers	2
N_w	Total number of turns per layer	1
	Core type No.	Philips E43/10/28-3F3 (with center leg removed) Philips PLT43/28/4-3F3
n_b	Number of cores used	7.2
l_g	Estimated air gap distance	$1mm$
B_{max}	Maximum magnetic flux density	$297mT$
	Ceramic dielectric material type No.	N1250
ε_{rD}	Relative dielectric constant of ceramic material	186
h_D	Thickness of ceramic dielectric material	$0.15mm$
$\tan\delta$	Loss factor of ceramic dielectric material	0.05%
k_{core}	Core aspect ratio	0.082
V_t	Total volume	$121\ cm^3$
l_t	Total length	$167mm$
w_t	Total width	$86mm$
h_t	Total height	$12mm$

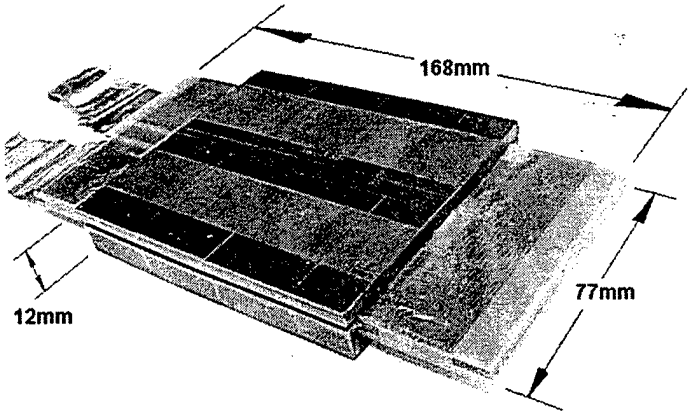


Fig. 4.1.4.8. Outline and dimensions of the ISRM prototype.

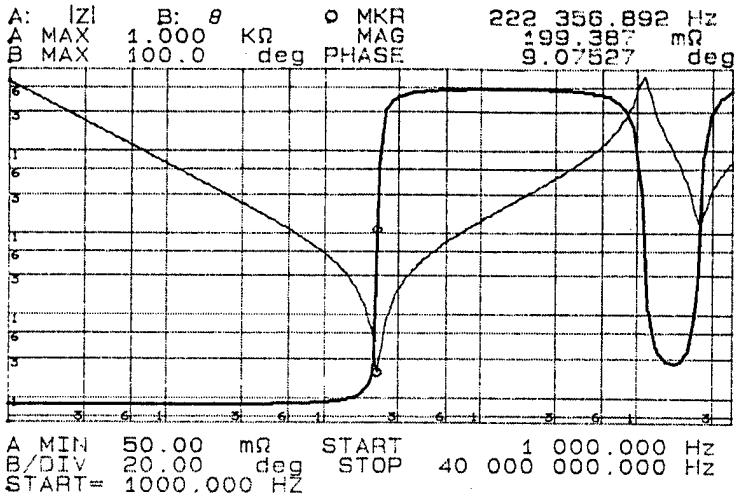


Fig. 4.1.4.9. Impedance analyzer testing results of the ISRM.

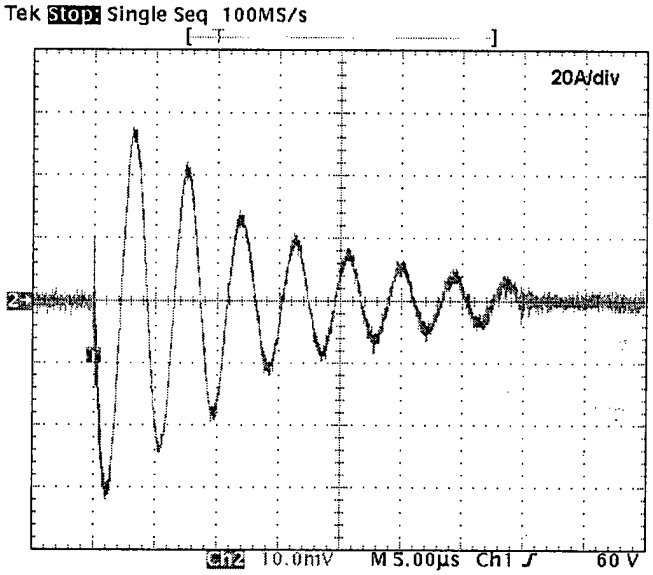


Fig. 4.1.4.10. Dynamic current waveform response from a 100V step input voltage.

Due to the relatively large area of a high power ISRM and the fragility of the thin dielectric material, the mechanical stress caused by different thermal expansion coefficients of the conductor and dielectric material at high current can not be neglected. Therefore, four small tiles are connected together with a small gap between each other to form one layer instead of making one big tile as one layer. A clamping technique is used to connect the tiles with each other with a certain degree of freedom for them to expand a little bit inside. Fig. 4.1.4.11 shows the configuration of the clamped tiles.

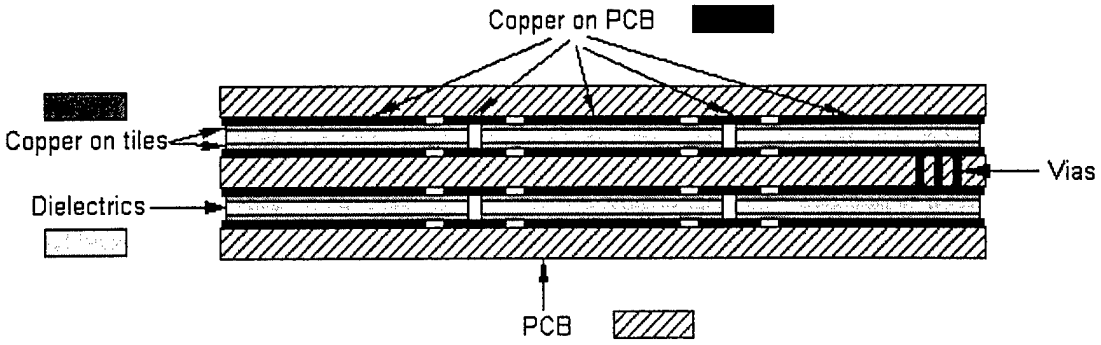
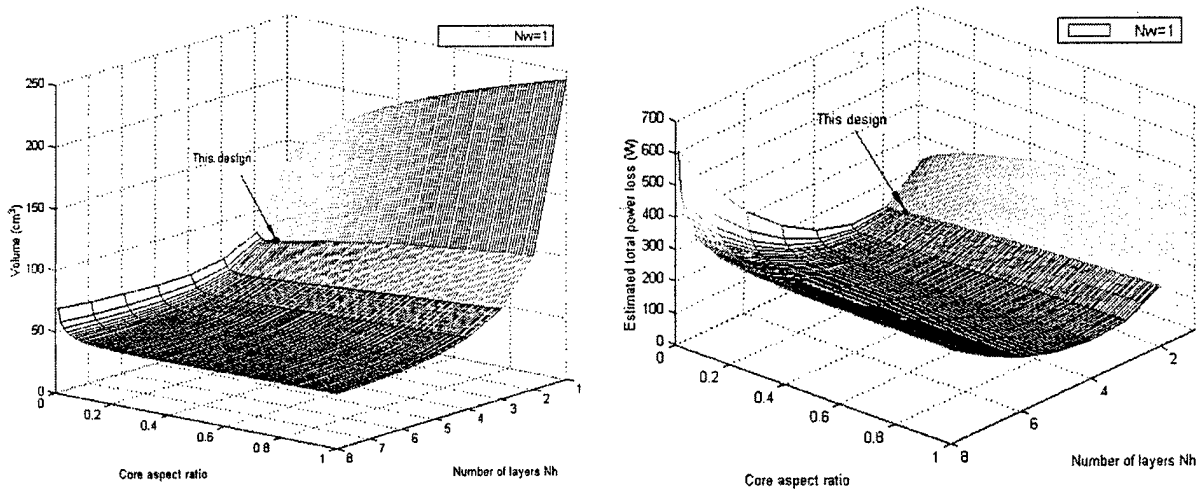


Fig. 4.1.4.11. PCB clamping interconnection of copper-plated dielectric tiles.

With $N_w = 1$, $J = 9.3A/mm^2$, $B_{\max} = 300mT$, assuming the dielectric material with any dielectric constant and magnetic core with any dimensions are available, the changing trend of the total volume and estimated power loss with various numbers of layers N_h and core aspect ratio k_{core} is shown in Fig. 4.1.4.12. The location of this design is highlighted in Fig. 4.1.4.12. This design is based on the dielectric materials and magnetic cores currently available in our lab or vendors. From Fig. 4.1.4.12, the volume could be reduced using 1-2 more layers without much compromising the quality factor. However, the cooling may be more difficult for more layers besides the air gap of the magnetic core has to be larger. The availability of the appropriate dielectric materials and complexity of the fabrication for more layers are issues to be further investigated. If J and $B_{\max}$ can be increased without bringing down the thermal performance, the module size can be further reduced. Obviously, this possibility may be more dependent on the cooling technique.



(a) Volume

(b) Estimated power loss

Fig. 4.1.4.12. Changing trend of the total volume and estimated power loss with various numbers of layers N_h and k_{core}.

Year II Task Summary for the Thrust 4 Work Plan

Task 2.4.1 Materials evaluation study for resonant auxiliary circuits – The study was conducted using equipment developed in related projects and led to the selection of the material to be used in the module that was designed and built as indicated.

Task 2.4.2 Development of design rules for electromagnetic integration of passives in auxiliary module – The design rules developed was incorporated into the generic software development and successfully used for designing the module, taking all material characteristics into account.

Task 2.4.3 Construction of module – The construction of the module was completed.

Task 2.4.4 Thermal cycling – No thermal cycling has been done yet but equipment has been ordered to do this.

Task 2.4.5 Thermal and mechanical modeling and comparison – As part of the thermal modeling the generation of realistic temperature profiles in the complicated module schedule has been completed. The rest of thermal and mechanical modeling will be completed in year III.

Task 2.4.6 Construction of a full auxiliary phase leg, including power devices, incorporating either MPIPPS, Embedded Power, or POL – The full construction has yet to be completed.

Task 2.4.7 Final evaluation of the integrated auxiliary module – The final evaluation can only be done after the commissioning of the auxiliary phase arm with the integrated resonant module. This will be undertaken in year III.

V. PROPOSED FUTURE EFFORT

The remaining work in the area of packaging is to complete the fabrication of functioning prototype modules and evaluate the effect of the packaging approach on the performance. The approaches that provide the best performance will be analyzed for reliability and manufacturability, and the integration of gate drive control circuitry and passive devices will be investigated.

Future efforts in the integration of passive devices will focus on completing the assembly of an Integrated Series Resonant Module (ISRM). Upon successful completion of thermal and performance testing, the effort will be placed on size reduction and module integration.

Upon the selection of the optimum packaging approach, thermal and thermo-mechanical modeling will be used to refine the design. Working in conjunction with University of Maryland's CALCE lab the design will be further refined to meet reliability requirements. At that point we propose to build a number of PEBB modules for a more rigorous performance and reliability testing.

VI. SUMMARY AND CONCLUSIONS

In order to facilitate the progressive development of PEBB packaging, we have paid special attention to materials engineering and testing. Major issues related to thermal management, noise reduction, integration of passive components, mechanical resistance to thermal cycling and stress, limit the current PEBB performance. We have pursued advances in these issues through materials selection and design for a high performance and compatible material system, interface engineering to improve thermal, electrical and mechanical properties, development of innovative processes for increased integration, and materials testing and characterization. We have developed advanced substrate materials/interface designs capable of removing heat from embedded power devices and power interconnects, with significantly improved heat-transfer efficiency compared to the current available power modules.

In this year the work resulted in building functioning hybrid integrated power switching modules in a range of technologies such as metal post, Power Overlay and Embedded Power, while design software and technology for building a resonant integrated passive module was also developed. The work has now progressed for the evaluation stage for all these technologies.

In order to achieve substantial advancements in PEBB packaging, we originally recognized a major technical challenge facing the packaging research is the lack of 3-dimensional packaging technologies that can offer high-level of integration of power devices, passive components, driver circuitry, controls, sensors and communication connections. Integration in power electronics is a rather complex process due to the incompatibility of materials and processing methods used in fabrication, and due to the high energy levels these components must handle. As a result of these high power levels, the required physical volume is usually large, especially for passive energy transfer and storage components, and monolithic integration is impractical in most applications. Our research in PEBB packaging addresses these existing barriers in the current state-of-the-art packaging approach. To achieve needed size reductions, we would increase the level of integration in hybrid assemblies by interconnecting power devices and control devices on a common substrate. Inside the state of the art power modules, interconnection of power devices is accomplished with wire-bonds, which are prone to noise, parasitic oscillations, fatigue and eventual failure. Our current packaging approach of direct bonding process for the interconnecting devices makes possible the development of three-dimensional packaging technologies by getting rid of the use of wire-bonds for device interconnection, which would offer even lower interconnection parasitics, reduced package size and low cost. We realize that increased integration and three dimensional structure would result in barriers such as increasing thermal density and cross talk, which we would overcome via thermal, electrical and thermo-mechanical modeling and improved materials/interface engineering of the proposed structures. By developing the PEBB based power electronics processes using our proposed integrated systems approach, we will improve the quality, reliability, and cost-effectiveness of power electronics systems and reduce both the time and effort associated with design cycles for system application. Packaging of power electronics building blocks is a critical part of the Navy's strategic approach to power electronic systems. Our accomplishments would significantly advance the current PEBB concept and establish a solid foundation for the development and implementation of future PEBB generations.

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11. Zhenxian Liang, Fred C. Lee, and Guo-Quan Lu, "Embedded Power, an Integrated Packaging Technology for IPEMs," Proceedings of the 33rd International Symposium on Microelectronics (IMAPS 2000), pp. 123-127, Boston, Massachusetts, September 20 - 22, 2000. (Best Paper of Session)

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Abstract

In the past year we have continued our objective to explore innovative three-dimensional power electronics packaging approaches, with the goal of eliminating wirebonds as device interconnections, for use in the construction of PEBB modules.

Our research has focused on two basic interconnection approaches, a direct solder approach where interconnection is achieved by soldering directly to the pads of the power devices, and a sputtered metal approach where interconnection is achieved by depositing a thin film of metal directly onto the device pads and a surrounding dielectric layer. In both approaches we have developed the capability to perform the unit processing steps and are close to having completed power switching stage modules representing two different sputtered metal packaging approaches.

We have also made significant accomplishments in the integration of passive devices. Our investigation into an alternative approach to inductor and capacitor integration using a low profile planar structure has led to the development of generic design software and the construction of a prototype integrated series resonant module (ISRM).

There has been considerable effort to quantify the effect of the packaging approaches on the performance of the modules. A universal tester has been designed and built which permits the measurement of the module's switching characteristics under full current and voltage conditions. Thermal and thermo-mechanical modeling techniques as well as alternative temperature measurement methods are being developed to investigate the thermal characteristics of the module. The packaging lab is increasing its environmental testing capability and an alliance with University of Maryland's CALCE lab will permit us to evaluate the reliability of the modules.

Our goal for the coming year is to construct functioning prototype modules using each of the packaging approaches and further investigate the incorporation of passive components and gate drive control circuitry. We expect that this effort will lead to the construction of fully integrated PEBB modules providing significantly improved efficiency and performance.