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# A Process for 94-GHz Schottky-Diode-Based Phase-Shifter MMICs

Warren Berk

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# Army Research Laboratory

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## A Process for 94-GHz Schottky-Diode-Based Phase-Shifter MMICs

Warren Berk

Sensors and Electron Devices Directorate

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## Abstract

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This report describes the first working monolithic microwave integrated circuit (MMIC) process produced at the Army Research Laboratory and the University of Maryland's Laboratory for Physical Sciences. This report describes a process that was used to produce 94-GHz phase shifters with  $357^\circ$  phase shift and a loss of  $-7.7$  dB at 10 V.

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## 1. Introduction

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A working process has been developed to produce Schottky-diode-based monolithic microwave integrated circuits (MMICs). The work was done in support of an Army Research Laboratory (ARL) Federation Laboratory (FedLab) project to produce an E-scan phased-array radar demonstration in 2001. The phase-shifter chips (along with PALNAs—power amplifier/low-noise amplifiers—made at Sanders) will go into an eight-channel transmitter/receiver module called an octopack. The phase-shifter circuits are designed to produce channel phase shifting of more than 360°. The full MMIC fabrication process presented here is based on passivated diodes with resistors, capacitors, and thinned wafers with via holes.

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## 2. Material

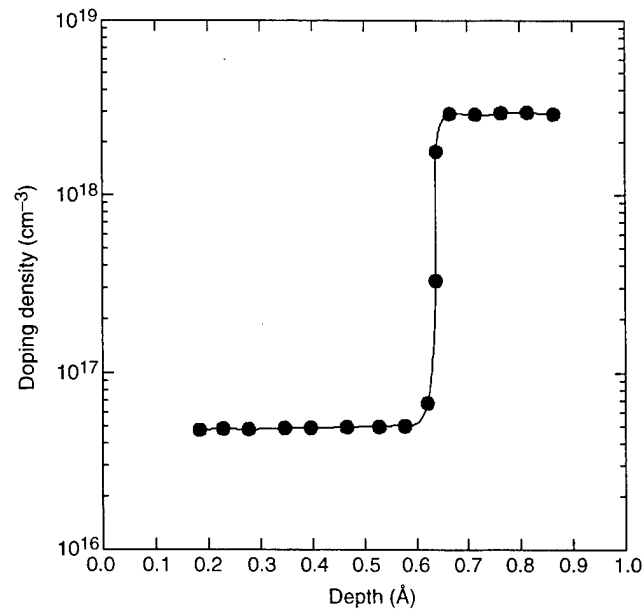
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Semi-insulating 3-in. substrates were bought from AXT, and the diode profile used for this project came from Sanders (fig. 1). Epitaxial films were grown on semi-insulating wafers with the ARL Varian GEN II molecular beam epitaxy (MBE) system. The wafers were characterized with a Polaron C-V (capacitance/voltage) profiling machine (fig. 2).

Figure 1. Doping profile used for this device.

7000 Å	$6 \times 10^{16}$	$n^-$ GaAs
2.5 μm	$4 \times 10^{18}$	$n^+$ GaAs
5000 Å	buffer	GaAs
GaAs substrate semi-insulating		

Figure 2. Polaron data of doping profile on PSIF3 5-2.



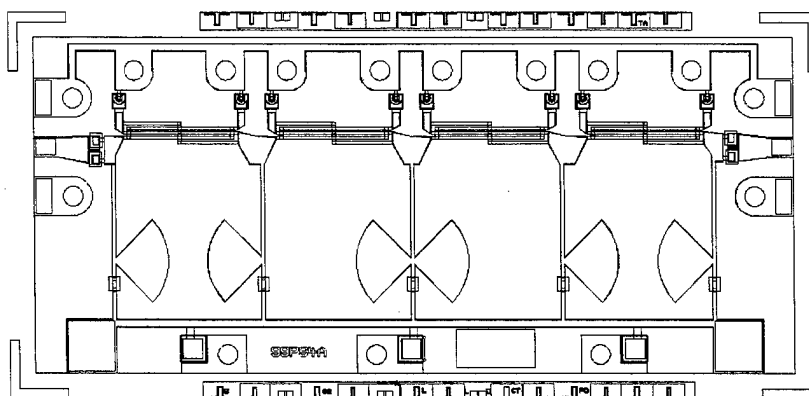
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### 3. Design and Layout

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Sanders had 94-GHz phase-shifter chips left over from the old Martin Marietta Laboratories and used those chips to build the first modules. They quickly realized that the new modules had no rf blocking capacitors between chips, so they had no way to independently control the diodes. The original design had to be changed so that rf blocking capacitors could be placed on the input side of the chip. (The original design already had blocking capacitors on the output side.) After consulting with the chip designer, Sandy Weinreb of the Jet Propulsion Laboratory, I changed the layout and sent the layout files to Sanders for mask fabrication. Figure 3 shows the final design of the chip.

Figure 3. Chip design used for FedLab project.



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## 4. Processing

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The process given here is an 11-mask-level process with wafer thinning to 100  $\mu\text{m}$ . This process is done at two locations: the Laboratory for Physical Sciences at the University of Maryland and the ARL compound in Adelphi, MD. Presented below is each process level and what was done. The process was developed with five lots of wafers of two or three wafers each, all going through the process at one time. Each lot consisted of at least one dummy (test) wafer for etch calibration and photoresist profile evaluations. Negative resists used for liftoffs were Futurrex NR8-1500 and NR7-3000.

Two steps were constantly being done for all the levels: plasma descum and oxide etching. Plasma descum is done to remove any photoresist residue left after photoresist development. Plasma descum either occurred in a parallel-plate machine or was done with a reactive ion etcher (RIE). Oxide etching was done to etch away any oxide generated during plasma descumming or removal of the native oxide.

### 4.1 Ohmic Contact

The ohmic contact process involves etching the wafers to make an ohmic contact to the  $n^+$ -GaAs layer. First, the wafers are coated with 1.5- $\mu\text{m}$ -thick negative photoresist to create the selected areas where I would like to produce the ohmic contacts. The wafers are etched in an inductively coupled plasma (ICP) system to a depth of about 6500  $\text{\AA}$ . Next, the samples are chemically etched for 1 min in 3 : 1 : 50  $\text{H}_3\text{PO}_4$  :  $\text{H}_2\text{O}_2$  : DI (deionized)  $\text{H}_2\text{O}$ ; this etch removes any surface damage created during the dry etching. The final etch depth needed is 7000  $\text{\AA}$ . After the samples are oxide etched in 1 : 1  $\text{HCl}$  : DI  $\text{H}_2\text{O}$ , they are placed in an  $e$ -beam evaporator for ohmic metal deposition. The metalization scheme used for this work is 800- $\text{\AA}$  Au : 400- $\text{\AA}$  Ge : 350- $\text{\AA}$  Ni : 500- $\text{\AA}$  Au. The excess metal is lifted off, and the wafers are annealed in a rapid thermal annealer (RTA) at 420  $^\circ\text{C}$  for 20 s.

### 4.2 Anode Contact Formation

To form an anode contact, I make a Schottky contact to the  $n^-$ -GaAs layer. The wafers are again coated with negative photoresist and aligned so that the anode pad is within the opening of the ohmic pad. After plasma descums, the wafers are oxide etched again and placed in the  $e$ -beam evaporator. The anode contact metalization scheme is 500- $\text{\AA}$  Ti : 250- $\text{\AA}$  Pt : 1000- $\text{\AA}$  Au. The metal and resist are lifted off before the wafers are cleaned. The contacts are measured so that I can ensure desired breakdown and resistance values.

### 4.3 Mesa Isolation

For mesa isolation, a pattern of photoresist is first applied to protect the area around the diode structures. A 3- $\mu\text{m}$ -thick positive photoresist is used for this purpose. After plasma descum, the wafers are etched in the ICP to a depth of 3.5  $\mu\text{m}$ . The dummy wafer is etched first so that the GaAs etch rate value can be determined, and then the etch time is adjusted so that the etch achieves 3.5  $\mu\text{m}$ . The wafers are then chemically etched in 3 : 1 : 50  $\text{H}_3\text{PO}_4$  :  $\text{H}_2\text{O}_2$  : DI  $\text{H}_2\text{O}$  until a depth of 3.9 to 4.0  $\mu\text{m}$  is reached.

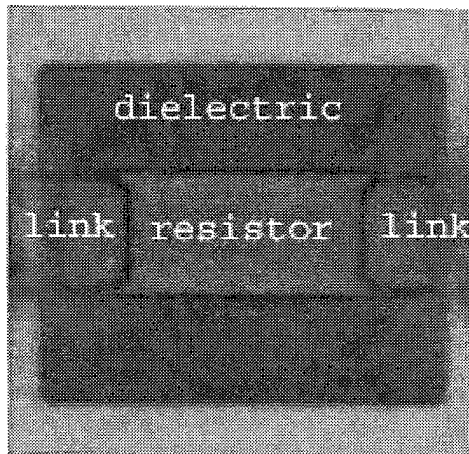
### 4.4 Resistors

Patterns for resistors are done with a 3- $\mu\text{m}$  negative resist. A layer of this thickness is needed to give mesas adequate protection during this step. The resistor material used for this process is TaN, which is reactively sputtered onto the wafers. The system used is the CVC 610 dc sputtering machine, with a tantalum target and nitrogen added into the argon plasma to create TaN films. Sheet resistivities are measured and calibrated with a cross bridge test structure. Flow rates and power are adjusted to yield sheet resistances of 50  $\Omega$  per square. Figure 4 shows a passivated resistor.

### 4.5 Circuit Metal

Circuit metal (also called link) is used (1) to connect resistors, (2) to be the bottom plates for the capacitors that come in the next step, and (3) to create the Lange couplers. The same 3- $\mu\text{m}$  negative resist is used for this liftoff process. Linewidth control is important at this step. The Lange couplers are designed for 94 GHz, so if the linewidths are off, the circuits will have more loss than expected. Samples are plasma descummed and then oxide etched before being placed in the *e*-beam evaporator. The metalization scheme used for this step is 1000- $\text{\AA}$  Ti : 250- $\text{\AA}$  Pt : 3000- $\text{\AA}$  Au : 500- $\text{\AA}$  Ti. The metalization is thicker so that the line resistances are kept low. Metal and resist are lifted off.

Figure 4. Passivated resistor on PSIF3 4-3 wafer.



## 4.6 Dielectric

PECVD (plasma-enhanced chemical vapor deposition) grown silicon nitride is used as the dielectric material. The wafers are cleaned and placed in the PECVD system. The film is deposited to a thickness of 2000 Å. Silicon nitride is deposited on additional test samples so that etch rates can be calculated later in this step. Photoresist is spun on after the dielectric deposition runs. The samples are then patterned to leave photoresist in the spots that need to be protected: diode mesas, resistors, and capacitors. Wafers are etched in an RIE with  $\text{CF}_4$ . Care is taken not to etch too long, since  $\text{CF}_4$  will attack the underlying titanium layer.

## 4.7 Air Bridge Formation

Air bridge formation requires five steps: post photoresist application, electroplating base, span photoresist application, electroplating, and photoresist/base stripping. First, AZ4620 positive photoresist is used to achieve 6.5 to 7.0  $\mu\text{m}$  of post photoresist. This photoresist is used to define the opening on top of the diode and form the bottom of the air bridges. The wafers are descummed and hard baked at 115 °C for 20 min. The wafers are oxide etched before being placed in the CVC sputtering machine. Second, plating base layers are deposited with the metalization scheme of 500-Å Ti : 1000-Å Au : 250-Å Ti. Third, the span photoresist, AZ4620, is spun on the wafers right after the wafers come out of the sputtering machine. The top titanium layer is etched away with 10% buffered hydrofluoric acid (BHF) solution. Fourth, the wafers are plated up to 4  $\mu\text{m}$  in a Technics TG-25 plating solution. Last, the photoresist and metals are etched with solvents, developers, and RIE.

## 4.8 Wafer Thinning

The wafers are then cleaved down to a 2-in. by 1-in. area to fit into the ICP system. Wafers are coated with FSC-M photoresist and hotplate baked at 140 °C for 10 min. The resist layer is used to prevent the air bridges from collapsing during mounting to the sapphire carriers. Samples are hand mounted to the sapphire (frontside down) with Z-71 wax. The samples are lapped to 110  $\mu\text{m}$  on a glass plate with 9- $\mu\text{m}$  calcined alumina and water. The wafers are polished down to 100  $\mu\text{m}$  on a polishing cloth with bleach and 0.3- $\mu\text{m}$  alumina.

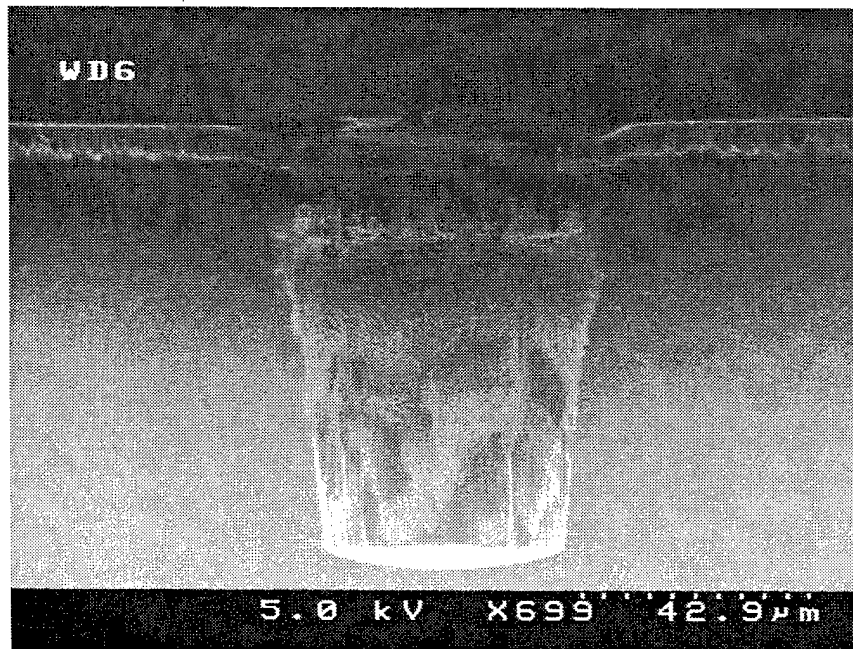
## 4.9 Transfer Etch

The first step to affect the wafer back is the transfer of alignment marks from the front to the back of the wafer. The wafers are coated with positive photoresist (AZ4330), and the patterns are aligned by an aligner with IR imaging. Alignment marks on the mask are aligned to the alignment marks on the front of the wafer. The resist is removed where the alignment marks need to be located, and the wafers are then etched in 3 : 1 : 50  $\text{H}_3\text{PO}_4$  :  $\text{H}_2\text{O}_2$  : DI  $\text{H}_2\text{O}$  for 5 min.

#### 4.10 Via-Hole Etching

Three layers of AZ4620 are used to pattern the wafers for dry etching of via holes. A total thickness of 21  $\mu\text{m}$  of resist is needed to etch through 100  $\mu\text{m}$  of GaAs. The ICP system is used again for this step. Maximum chlorine and  $\text{BCL}_3$  flow rates (20 sccm each) are used with etching pressures of 15 mT. Average etching rates of 2  $\mu\text{m}/\text{min}$  are achieved at room temperature. Figure 5 is a side view of an etched via-hole profile. I periodically check the wafers under the microscope to see if the vias are etched to the gold layer on the front of the wafer. The bottom contact diameter of the via is kept under 60  $\mu\text{s}$ .

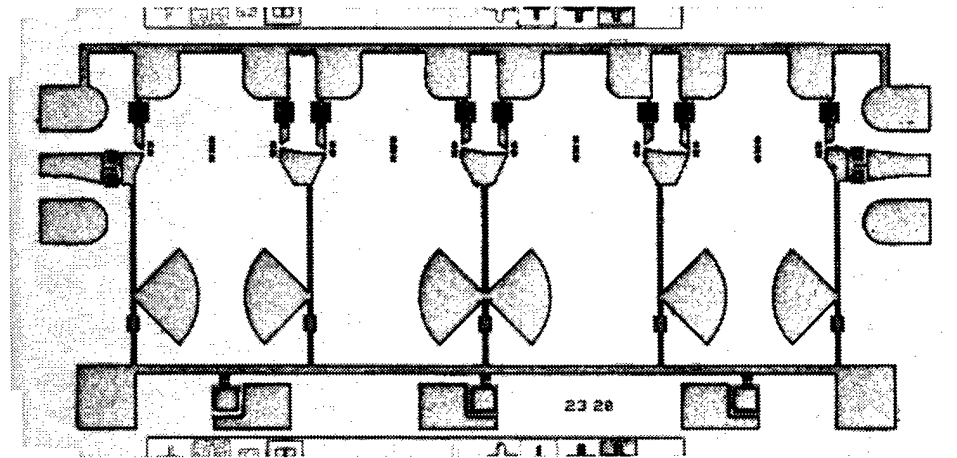
Figure 5. Side view of an etched via hole created by ICP.



#### 4.11 Linkback Plating

The wafers are cleaned with solvents and plasma descummed in an RIE. Samples are oxide etched in 1 : 9  $\text{NH}_4\text{OH}$  : DI  $\text{H}_2\text{O}$  for 1 min. Wafers are placed in the CVC sputtering machine for electroplating base deposition. The metalization scheme is 1000-Å Ti : 3000-Å Au : 500-Å Ti. Waycoat SC negative resist is spun on the wafers after the deposition runs. This resist when exposed is very resilient to its developer. This property is needed so that the vias can be developed out while the pattern on the back of the wafer stays in place. The top titanium layer is etched in 10% BHF. The wafers are plated with 4  $\mu\text{m}$  of gold with the Technics TG-25 plating solution. After plating, the wafers are  $\text{O}_2$  plasma etched in an RIE to remove the SC negative resist. The electroplating base is chemically removed. The wafers are flipped and cleaned for discrete diode dc and rf testing. Figure 6 is the front of a finished chip.

Figure 6. A finished chip from wafer PSIF3 4-3.



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## 5. Summary

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Described in the previous section is a working diode phase circuit process used to deliver chips to Sanders for the E-scan array radar project. Out of the six epitaxial wafers going through the process, only two failed. Dc testing was done on discrete devices (fig. 7), which consisted of via continuity testing,  $I$ - $V$  testing, and four-point testing for calculating series resistances. Dc test results showed a series resistance average of  $3 \Omega$ , ideality factors of 1.1, breakdown voltages of 13.5 to 15.5 V, and over 90-percent continuity yield on via holes. Sanders has just started to test the chips on wafers at 94 GHz. The first results show a phase shift of  $357^\circ$  with a loss of 7.7 dB at a bias of 10 V (fig. 8). A copy of an actual "traveler" (a blueprint of the process) is provided in the appendix.

Figure 7. Discrete diodes used for dc testing.

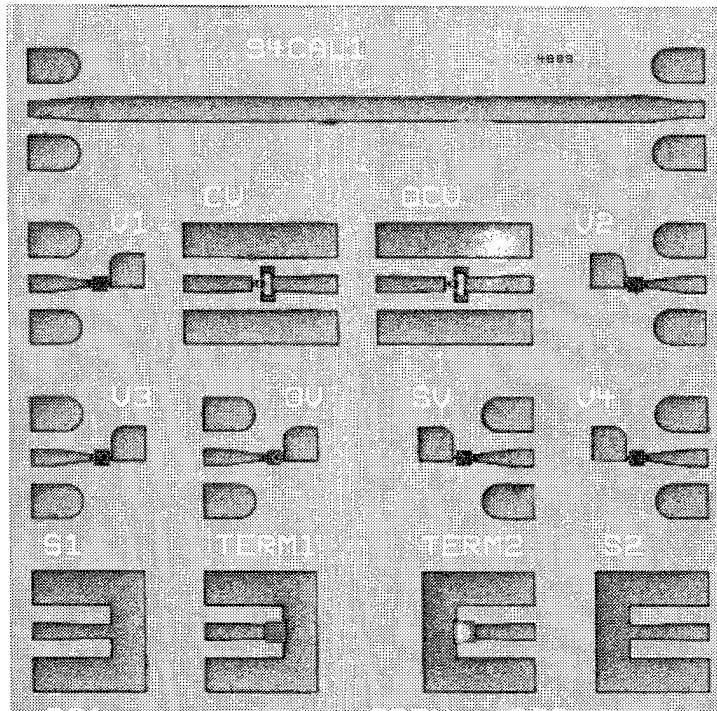
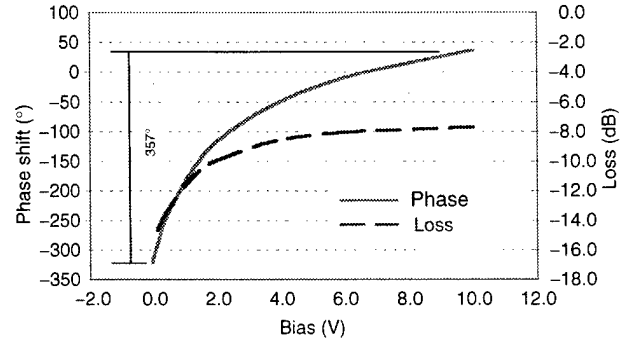


Figure 8. First 94-GHz test results from Sanders (chip 2812).



Bias (V)	Loss (dB)	Phase shift (°)
10.0	-7.7	36
6.1	-8.0	-10
3.9	-8.6	-54
2.5	-9.6	-98
1.5	-10.6	-148
0.5	-13.3	-238
-0.1	-15.5	-321

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## Acknowledgments

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Thanks go to Stefan Svensson for the growth of the epitaxial material and for reviewing this report. I also wish to thank Steve Brown (ARL), Allen Lepore (ARL), Kevin Larson (Northrup Grumman), and Doug Burrows (Sanders) for mask fabrication.



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## Appendix. Process Traveler

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The process traveler presented in this appendix was the general blueprint used to fabricate the circuits described in this report. Individual steps were optimized independently and then put together to form this process. Every lot had a traveler accompanying it as it went through the process. Actual times and conditions were written down as the lots went through each step. Each lot had at least one mechanical wafer to verify process times and machine conditioning.

**1.00 Ohmic Metal**

- 1.01 Clean**  
ACE soak:10 min, IPA soak: 10 min, blow dry
- 1.02 Hard Bake**  
Convection oven, 120 °C, 30 min
- 1.03 Coat Photoresist**  
Spinner: HMDS, 4 krpm, 20 s  
Futurrex NR8-1500, 4 krpm, 20 s
- 1.04 Soft Bake**  
Hot plate, 120 °C, 60 s
- 1.05 Expose**  
Mask: ohmic  
Tool: Karl Suss contact aligner,  
Exposure: 11 mW/cm<sup>2</sup>, 15 s
- 1.06 Develop**  
RD2: 110 s, DI rinse 1 min, blow dry
- 1.07 Inspect**  
Resist overhang, adhesion  
Critical dimension
- 1.08 Descum**  
Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1 min
- 1.09 Inspect**  
Photoresist adhesion
- 1.10 Ohmic Etch**  
*RIE etch*

Wafer	Flow (sccm)		Pressure (mTorr)	Power (W) RF1/RF2	Time (min)
	BCl <sub>3</sub>	Cl <sub>2</sub>			
Test	12.5	2.5	5	70/500	1.5
Wafer 1	12.5	2.5	5	70/500	_____
Wafer 2	12.5	2.5	5	70/500	_____

*Chem etch*

3 : 01 : 50 H<sub>3</sub>PO<sub>4</sub> : H<sub>2</sub>O<sub>2</sub> : H<sub>2</sub>O

Photoresist thickness (Å): \_\_\_\_\_

Etch depth (Å): \_\_\_\_\_

Etch time (s): \_\_\_\_\_

Total thickness (sum of photo thickness & etch depth) (Å): \_\_\_\_\_

Desired etch depth: 1500-2000 Å

**1.11 Oxide Etch**

50% HCl, 60 s, DI rinse 20 s, blow dry

**1.12 Deposit Thin Film**

Tool: \_\_\_\_\_

	Design thickness (Å)	Rate (Å/s)	Thickness (Å)
Metal			
Au	800	_____	_____
Ge	400	_____	_____
Ni	350	_____	_____
Au	500	_____	_____

**1.13 Liftoff**

Beaker/air brush, ACE: \_\_\_\_\_ min

**1.14 Inspect**

Critical dimension

**1.15 Measure Metal Thickness**

Thickness (Å): \_\_\_\_\_

**1.16 Clean**

ACE soak: 10 min, IPA soak: 10 min; blow dry

**1.17 Bake**

Convection oven, 125 °C, 25 min

**1.18 RTA**

AG610, Recipe: GaAs

Temp: 420 °C

Time: 20 s

Degree of overshoot per wafer run (°C): 1 \_\_\_\_\_ 2 \_\_\_\_\_ 3 \_\_\_\_\_

**1.19 Inspect**

## 2.00 Anode Metal

### 2.01 Clean

ACE soak: 10 min; IPA soak: 10 min, blow dry

### 2.02 Hard Bake

Convection oven, 120 °C, 30 min

### 2.03 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
Futurrex NR8-1500, 4 krpm, 20 s

### 2.04 Soft Bake

Hot plate, 120 °C, 60 s

### 2.05 Expose

Mask: anode  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 11 s

### 2.06 Develop

RD2: 110 s, DI rinse 1 min, blow dry

### 2.07 Inspect

Resist overhang, adhesion  
Critical dimension

### 2.08 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1 min

### 2.09 Oxide Etch

50% HCl, 60 s, DI rinse 20 s, blow dry

### 2.10 Inspect

Photoresist adhesion

### 2.11 Deposit Thin Film

Tool: \_\_\_\_\_

	Design thickness	Rate	Thickness
Metal	(Å)	(Å/s)	(Å)
Ti	500	—	—
Pt	250	—	—
Au	1500	—	—

**2.12 Liftoff**

Beaker/air brush, ACE: \_\_\_\_\_ min  
ACE soak: 10 min, IPA soak: 10 min, blow dry

**2.13 Inspect**

Critical dimension  
Metal edge acuity

**2.14 Measure Metal Thickness**

Thickness (Å): \_\_\_\_\_

### 3.00 Mesa

#### 3.01 Clean

ACE soak: 10 min; IPA soak: 10 min, blow dry

#### 3.02 Hard Bake

Convection oven, 120 °C, 30 min

#### 3.03 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
AZP 4330, 4 krpm, 20 s

#### 3.04 Soft Bake

Convection oven, 100 °C, 25 min

#### 3.05 Expose

Mask: mesa  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 10 s

#### 3.06 Develop

Beakers with solution: AZ400K : DI = 1 : 4  
Time: 50 s  
Rinse in DI: 1 min, blow dry

#### 3.07 Inspect

#### 3.08 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1.5 min

#### 3.09 Mesa Etch

*RIE etch*

ICP or MIE

Wafer	Pressure (mTorr)	Flow (sccm)		Power (W) RF1/RF2	Time (min)	Etch depth (Å)
		BCl <sub>3</sub>	Cl <sub>2</sub>			
Test	5	12.5	2.5	70/500	20	_____
Wafer 1	5	12.5	2.5	70/500	_____	_____
Wafer 2	5	12.5	2.5	70/500	_____	_____

*Chem etch*

3 : 01 : 50 H<sub>3</sub>PO<sub>4</sub> : H<sub>2</sub>O<sub>2</sub> : H<sub>2</sub>O

Etch rate (Å/s)	Time (s)	Etch depth (Å)	Height measurement (Å)
_____	_____	_____	_____
_____	_____	_____	_____
_____	_____	_____	_____

**3.10 Strip Resist**

Beaker, ACE soak, IPA soak, blow dry

**3.11 Inspect**

**3.12 Measure Mesa Height**

Height (Å): \_\_\_\_\_

## 4.00 Resistor

### 4.01 Clean

ACE soak: 10 min; IPA soak: 10 min, blow dry

### 4.02 Hard Bake

Convection oven, 120 °C, 30 min

### 4.03 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
Futurrex NR7-3000, 4 krpm, 20 s

### 4.04 Soft Bake

Hot plate, 120 °C, 60 s

### 4.05 Expose

Mask: circuit metal  
Tool: Karl Suss contact aligner  
Esposure: 11 mW/cm<sup>2</sup>, 27 s

### 4.06 Postbake

Hot plate, 120 °C, 60 s

### 4.07 Develop

RD6: 30 s, DI rinse 1 min, blow dry

### 4.08 Inspect

Resist overhang, adhesion  
Critical dimension

### 4.09 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1.5 min

### 4.10 Oxide Etch

50% HCl, 60 s, DI rinse 20 s, blow dry

### 4.11 Inspect

Photoresist adhesion

### 4.12 Deposit Thin Film

Tool: CVC

	Target	Flow	Pressure	Power	Time	Dep.	Design
Wafer	metal	(sccm)	(mTorr)	(W)	(min)	rate	(Å)
Test	Ta	N <sub>2</sub> /Ar				(Å/s)	
	Ta	3/30	10	700	6	_____	400-440
1	Ta	3/30	_____	_____	_____	_____	400-440
2	Ta	3/30	_____	_____	_____	_____	400-440

**4.13 Liftoff**

RR2 Remover soak and rinse, 100 °C, 10 min

Beaker/air brush, ACE: \_\_\_\_\_ min

ACE soak: 10 min, IPA soak: 10 min, blow dry

**4.14 Inspect**

Critical dimension

Metal edge acuity

**4.15 Measure Metal Thickness**

Thickness (Å): \_\_\_\_\_

## 5.00 Circuit Metal

### 5.01 Clean

ACE soak: 10 min, IPA soak: 10 min, blow dry

### 5.02 Hard Bake

Convection oven, 120 °C, 30 min

### 5.03 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
Futurrex NR7-3000, 4 krpm, 20 s

### 5.04 Soft Bake

Hot plate, 120 °C, 60 s

### 5.05 Expose

Mask: circuit metal  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 20 s

### 5.06 Postbake

Hot plate, 120 °C, 60 s

### 5.07 Develop

RD6: 30 s, DI rinse 1 min, blow dry

### 5.08 Inspect

Resist overhang, adhesion  
Critical dimension

### 5.09 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1 min

### 5.10 Oxide Etch

50% HCl, 60 s, DI rinse 20 s, blow dry

### 5.11 Inspect

Photoresist adhesion

**5.12 Deposit Thin Film**

Tool: \_\_\_\_\_

	Design thickness	Rate	Thickness
Metal	(Å)	(Å/s)	(Å)
Ti	500	_____	_____
Pt	250	_____	_____
Au	3000	_____	_____
Ti	500	_____	_____

**5.13 Liftoff**

RR2 Remover soak and rinse, 100 °C, 10 min

Beaker/air brush, ACE: \_\_\_\_\_ min

ACE soak: 10 min, IPA soak: 10 min, blow dry

**5.14 Inspect**

Critical dimension

Metal edge acuity

**5.15 Measure Metal Thickness**

Thickness (Å): \_\_\_\_\_

## 6.00 Passivation

### 6.01 Clean

ACE soak: 15 min, IPA soak: 15 min, blow dry

### 6.02 Hard Bake

Convection oven, 120 °C, 30 min

### 6.03 Deposit Thin Film

Tool: LPS Plasmalab Temp: 300 °C

Wafer	Pressure (mTorr)	Flow (sccm)		Power (W)	Dep. time (min)	Thickness (Å)
		NH <sub>3</sub>	SiH <sub>4</sub> /N <sub>2</sub>			
Test	350	5	200	20	21	—
1	—	—	—	—	—	—
2	—	—	—	—	—	—

### 6.04 Inspect

### 6.05 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
AZP 4330, 4 krpm, 20 s

### 6.06 Softbake

Convection oven, 105 °C, 25 min

### 6.07 Expose

Mask: passivation  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>

### 6.08 Develop

Beaker switch solutions: AZ400K : DI = 1 : 4  
Time: 50 s  
Rinse in DI: 1 min, blow dry

### 6.09 Inspect

### 6.10 Etch

Tool: PlasmaLab RIE Gas: CF<sub>4</sub>

Wafer	Pressure (mTorr)	Flow (%)	Power (W)	Etch time (min)
1	—	—	—	—
2	—	—	—	—

**6.11 Strip Resist**

ACE soak, IPA soak, blow dry

**6.12 Inspect**

**6.13 Measure Nitride/Oxide Height**

Height (Å): \_\_\_\_\_

## 7.00 Electroplate

### 7.01 Clean

ACE soak: 10 min, IPA soak: 10 min, blow dry

### 7.02 Hard Bake

Convection oven, 120 °C, 30 min

### 7.03 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
AZP4620, 4 krpm, 20 s

### 7.04 Soft Bake

Convection oven, 105 °C, 25 min

### 7.05 Expose

Mask: post  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 18 s

### 7.06 Develop

Beaker switch solution: AZ400K : DI = 1 : 4 , 60 s  
Rinse in DI: 1 min, blow dry

### 7.07 Inspect

### 7.08 Measure Postresist Thickness

Thickness (Å): \_\_\_\_\_

### 7.09 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, flow rate: 66 sccm, 100 W, 1 min

### 7.10 Postbake

Convection oven, 115 °C, 15 min

### 7.11 Oxide Etch

Etchant: 10% NH<sub>4</sub>OH, 30 s, blow dry 1 min

### 7.12 Plating Base Deposition

Tool: CVC sputtering machine

	Desired layer thickness (Å)	Pressure (mTorr)	Power (W)	Flow (sccm)	Time (s)
Metal					
Ti	500	10	700	30	7.8
Au	1000	10	300	30	15.0
Ti	250	10	700	30	3.9

**7.13 Coat Photoresist**

Spinner  
AZP4620, 4 krpm, 20 s

**7.14 Soft Bake**

Convection oven, 100 °C, 25 min

**7.15 Expose**

Mask: span  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 30 s

**7.16 Develop**

Solution: AZ400K : DI = 1 : 4, 70 s  
Rinse in DI: 1 min, blow dry

**7.17 Inspect**

**7.18 Descum**

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W/2 min

**7.19 Measure Resist Thickness**

**7.20 Ti Etch**

Beaker, 10% BHF, 50 s

**7.21 Electroplate**

Solution: Technicgold 25, 120 °F    Design: 4 μm  
Pulse power supply: 10% duty cycle, 90 min at 8 mA  
DI rinse 1 min, blow dry  
Thickness measurement (μm): \_\_\_\_\_

**7.22 Strip Span Resist**

Mask: none  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 2 min  
Developer: AZ400K : DI = 1 : 4, 2 min  
DI rinse 1 min, blow dry

**7.23 Inspect**

**7.24 Strip Plating Base**

Ti    Gas: CF<sub>4</sub>

	Pressure	Flow	Power	Etch time
Wafer	(mTorr)	(sccm)	(W)	(s)
Test	_____	_____	_____	_____
Wafer 1	_____	_____	_____	_____
Wafer 2	_____	_____	_____	_____

Au 50% Technistrip, 45–60 s, rinse, blow dry  
Ti 10% BHF, 20 s, rinse, blow dry

**7.25 Strip Post Photoresist**

Tool: PlasmaLab RIE Gas: O<sub>2</sub>

Wafer	Pressure (mTorr)	Flow (sccm)	Power (W)	Etch time (s)
Test	_____	_____	_____	_____
Wafer 1	_____	_____	_____	_____
Wafer 2	_____	_____	_____	_____

ACE spin, IPA spin: 10 min, spin dry

**7.26 Inspect**

**7.27 Measure Plating Thickness**

Thickness (μm): \_\_\_\_\_

**8.00 Lapping (Target: 100  $\mu\text{m}$ )**

**8.01 Mount Wafer Face Down**

Wax: \_\_\_\_\_

Uniformity ( $\mu\text{m}$ ):  $\pm$  \_\_\_\_\_

**8.02 Lap Wafer**

Grit used: \_\_\_\_\_

Starting thickness ( $\mu\text{m}$ ): \_\_\_\_\_

Midpoint thickness ( $\mu\text{m}$ ): \_\_\_\_\_

**8.03 Polish Wafer**

Chemical used: \_\_\_\_\_

Time (s): \_\_\_\_\_

Final thickness ( $\mu\text{m}$ ): \_\_\_\_\_

## 9.00 Alignment Mark Transfer

### 9.01 Clean

ACE spin, IPA spin: 10 min, spin dry

### 9.02 Hard Bake (optional)

Convection oven, 120 °C, 30 min

### 9.03 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
AZP4330, 4 krpm, 20 s

### 9.04 Soft Bake

Convection oven, 105 °C, 30 min

### 9.05 Expose

Mask: anode

Tool: Karl Suss contact aligner

Exposure: 11 mW/cm<sup>2</sup>, 10 s

### 9.06 Develop

Beakers with solution: 1 : 4 400KAZ : DI, 45 s, DI rinse 10 s, blow dry

### 9.07 Descum

Plasma asher: Metrix

100% O<sub>2</sub>, 66 sccm, 100 W, 1 min

### 9.08 Inspect

### 9.09 Transfer Etch

*Chem etch*

3 : 01 : 50 H<sub>3</sub>PO<sub>4</sub> : H<sub>2</sub>O<sub>2</sub> : H<sub>2</sub>O

Wafer	Etch rate (Å/s)	Time (s)	Etch depth (Å)
Test	_____	_____	_____
1	_____	_____	_____
2	_____	_____	_____

### 9.10 Measure Depth

Depth (Å): \_\_\_\_\_

## 10.00 Via Hole

### 10.01 Clean

ACE spin, IPA spin, spin dry

### 10.02 Hard Bake (optional)

Convection oven, 120 °C, 30 min

### 10.03 Coat Photoresist

Spinner

AZ4620, 3 krpm, 20 s, 3 coats

### 10.04 Soft Bake

Convection oven, 110 °C/60 min, 100 °C/45 min, 90 °C/30 min

### 10.05 Expose

Mask: via

Tool: Karl Suss contact aligner

Exposures: 11 mW/cm<sup>2</sup>, 90 s

### 10.06 Develop

Beakers with solution: AZ400K : DI = 1 : 4, 90 s

Rinse in DI 1 min, blow dry

### 10.07 Inspect

### 10.08 Measure Via Resist Thickness

Thickness (µm): \_\_\_\_\_

### 10.09 Descum

Plasma asher: Metrix

100% O<sub>2</sub>, 66 sccm, 100 W/1 min

### 10.10 Postbake (optional)

Convection oven, 120 °C, 15 min

### 10.11 Via Etch

DC bias (V): \_\_\_\_\_

Wafer	Pressure (mTorr)	Flow (sccm)		Power (W)	Time (min)
		BCl <sub>3</sub>	Cl <sub>2</sub>	RF1/RF2	
Test	_____	_____	_____	_____	_____
1	_____	_____	_____	_____	_____
2	_____	_____	_____	_____	_____

### 10.12 Strip Photoresist

## 11.00 Backside Electroplating Base

### 11.01 Clean

### 11.02 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1 min

### 11.03 Oxide Etch

Etchant: 10% NH<sub>4</sub>OH, 30 s, blow dry 1 min

### 11.04 Deposit Plating Base

Tool: CVC sputtering machine

	Desired layer Metal thickness (Å)	Pressure (mTorr)	Power (W)	Flow (sccm)	Time (min)
Ti	1000	10	700	30	15.6
Au	3000	10	300	30	45.0
Ti	250	10	700	30	3.9

## 12.00 Backside Electroplating Photowork

### 12.01 Clean Wafer

### 12.02 Coat Photoresist

Spinner: HMDS, 4 krpm, 20 s  
Waycoat, 4 krpm, 20 s

### 12.03 Soft Bake

Convection oven, 90 °C, 30 min

### 12.04 Expose

Mask: back link  
Tool: Karl Suss contact aligner  
Exposure: 11 mW/cm<sup>2</sup>, 30 s

### 12.05 Develop

PF develop for about 5 min, then rinse in N-butyl acetate

### 12.06 Inspect

Critical dimension

### 12.07 Descum

Plasma asher: Metrix  
100% O<sub>2</sub>, 66 sccm, 100 W, 1 min

## 13.00 Backside Electroplating

### 13.01 Ti Etch

Beaker with solution, 10% BHF, 50 s

### 13.02 Electroplate

Solution: Technicgold 25, 120 °F    Design: 4  $\mu$ m  
Pulse power supply: 10% duty cycle, 60 min at 10 mA  
DI rinse 1 min, blow dry  
Thickness measured ( $\mu$ m): \_\_\_\_\_

### 13.03 Strip Resist

Tool: RIE

Pressure (mTorr)	Flow	Power (W)	Time (min)
300	40% O <sub>2</sub>	75	35

### 13.04 Inspect

### 13.05 Strip Plating Base

Ti    10% BHF, 60 s, rinse, blow dry  
Au    50% Technistrip, 45–60 s, rinse, blow dry  
Ti    10% BHF, 20 s, rinse, blow dry

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