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13. ABSTRACT (Maximum 200 words)

This grant supported additional graduate students to work on a parent DARPA Research Grant at Lehigh University entitled "Polysilicon TFT's in Advanced Display Technologies".

I had many good results throughout the work done under this DARPA grant. This section is divided into three major subsections. The first section describes my results regarding advances in polysilicon material. We set out to investigate a new crystallization technique to be used to crystallize the amorphous silicon. The second section describes work regarding the integration of polysilicon TFTs for active matrix organic light emitting diode displays. The third section summarizes work done on polysilicon display driver circuits.

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Mark Stewart

Final Fellowship Report

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Subordinate to DARPA Grant 19949444 C

"Polysilicon TFTs in Advanced Display Technologies"

March 2000

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Goals of the Fellowship

This fellowship was awarded to support a DARPA grant entitled "Low Temperature Polysilicon Devices in Advanced Display Technologies". The advanced display technology that was considered through this work was that of active matrix organic light emitting diode displays (AM-OLEDs). The goal of this fellowship was to provide support to a student to perform research to help achieve the goals of the above stated DARPA grant.

The specific goals of this student were as follows: (1) To investigate a new crystallization process (RTP) for thin film transistors fabricated at glass compatible temperatures: (2) To develop a process to fabricated AM-OLED displays: (3) To design and layout AM-OLED displays and polysilicon driver circuits: (4) To fabricate AM-OLED displays.

Summary of Important Results

I had many good results throughout the work done under this DARPA grant. This section is divided into 3 major subsections. The first section describes my results regarding advances in polysilicon material. We set out to investigate a new crystallization technique to be used to crystallize the amorphous silicon. The second section describes work regarding the integration of polysilicon TFTs for active matrix organic light emitting diode displays. The third section summarizes work done on polysilicon display driver circuits.

Section 1. Work on Polysilicon Material

The primary goal of this work was to investigate the use of Rapid Thermal Processing for the crystallization of amorphous silicon films. In the process of conducting this research, other related topics were also covered such as the effect of polysilicon grain size on the carrier mobility. I will first discuss my accomplishments regarding the investigation of RTP and then I will discuss some of the advances made in polysilicon technology not directly related to RTP.

1.1.0. Results on RTP Processing for Polysilicon Crystallization

1.1.1 EXPERIMENTAL

First, this section details the statistical experiments that were conducted to optimize the polysilicon films. Then, the results of the experiments are presented followed by a discussion of how the most important factors effect the crystallization temperature and the device performance.

In order to meet the goals of this work, a series of statistically designed experiments were designed and conducted. Statistical models were then derived from the experimental results that quantitatively define the effects of the most important process parameters on the polysilicon crystallization temperature and device performance. These models are then used to understand how to co-optimize both the RTP crystallization temperature and the device performance.

The research was conducted in three experimental phases with each phase corresponding to a different method for the deposition of the amorphous silicon. The first phase investigated the RTP crystallization of amorphous silicon deposited by low pressure chemical vapor deposition (LPCVD) using silane as the source gas. The second phase investigated amorphous silicon deposited by LPCVD using disilane as the source gas. The third phase investigated the deposition of amorphous silicon by plasma enhanced chemical vapor deposition (PECVD). For each phase, 'screening' experiments were conducted to determine and compare the linear effects of a variety of deposition and annealing conditions. For the PECVD experimental phase, a 'response surface' experiment was also conducted after the screening experiment was complete. The goal of the response surface experiment was to investigate fewer parameters (4) in more detail.

Two 8 run screening experiments were designed to determine the importance of LPCVD deposition and RTP annealing conditions to optimize device performance and crystallization temperature. One experiment was conducted using silane as the source gas and the other was conducted using disilane as the source gas. The experimental set-up for both experiments is shown in table 1.1. A more detailed explanation of this experimental approach is found in reference [1.1].

In order to investigate amorphous silicon deposited using PECVD, a third screening experiment was designed. Due to the complicated nature of the PECVD deposition process, many more variables needed to be investigated. To accommodate the increased number of variables, a 16 run screening experiment was designed. The experimental set-up for the PECVD deposited material is shown in table 1.2. After completion of the 16 Run screening experiment, the four most important parameters were chosen for more detailed investigation. A response surface experiment was conducted using 27 Runs and investigating three different levels for each variable [1.2]. Table 1.3 shows the response surface experimental set-up.

		de-	df-	ab-	ae-	ad-	ag-	af-
		fg-	eg-	dg-	bf-	bg-	bd-	be-
		cb-	ac-	ef-	cg-	cf-	ce-	cd-
	run #	A	B	C	D	E	F	G
silane	+	200 mT	580 C		100 nm	15 mm/s	LTO	Yes
experiment	-	100 mT	550 C		500 nm	5 mm/s	PECVD	No
		deposition pressure	deposition temp	dummy	film thickness	RTP speed	oxide type	preclean
disilane	+	160 mT	500 C		100 nm	15 mm/s	5 nm	
experiment	-	80 mT	470 C		50 nm	5 mm/s	0	
		deposition pressure	deposition temp	dummy	film thickness	RTP speed	seed thickness	dummy
	1	-1	-1	-1	-1	-1	-1	-1
	2	-1	-1	-1	1	1	1	1
	3	-1	1	1	1	1	-1	-1
	4	-1	1	1	-1	-1	1	1
	5	1	1	-1	-1	1	1	-1
	6	1	1	-1	1	-1	-1	1
	7	1	-1	1	1	-1	1	-1
	8	1	-1	1	-1	1	-1	1

Table 1.1. LPCVD screening experimental set-up. The investigated input parameters for the experiments using silane as the source gas and disilance as the source gas as shown.

					AD										
					BG	BD									
Alias	NO	HJ	IJ	HL	HM	HN	HO			BH	BI		BO	BL	
Structure	LM	LN	LO	IM	IL	IO	IN	BJ	DM	DN	DO	BM	DI	DJ	BM
	HI	MO	MN	JN	JO	JL	JM	DL	GN	GM	GL	DH	GJ	GI	GH
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
+		1 T		300 W			350 C	disilane	Ar	1500 sccm		yes	yes	yes	15 mm/s
-		0.5 T		200 W			200 C	silane	H2	700 sccm		no	no	no	5 mm/s
		deposition		power			deposition	deposition	dilutant	dilutant		argon	RTP	hydrogen	RTP scan
		pressure					temp	gas	gas	flow		clean	dehydrog.	clean	speed
Run #															
1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
2	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
3	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1
4	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
5	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1
6	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1
7	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1
8	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
9	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1
10	1	1	-1	-1	1	1	-1	1	-1	-1	1	1	-1	-1	1
11	1	1	-1	1	-1	-1	1	1	-1	-1	1	-1	1	1	-1
12	1	1	-1	1	-1	-1	1	-1	1	1	-1	1	-1	-1	1
13	1	-1	1	1	-1	1	-1	-1	1	-1	1	1	-1	1	-1
14	1	-1	1	1	-1	1	-1	1	-1	1	-1	-1	1	-1	1
15	1	-1	1	-1	1	-1	1	1	-1	1	-1	1	-1	1	-1
16	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1

Table 1.2. Experimental set-up for the PECVD screening experiment.

	Deposition Temperature (degrees C)	Deposition Pressure (Torr)	Deposition Power (Watts)	RTP Scan Speed (mm/s)
high value (+)	300	1.5	300	7
center value (0)	350	1	200	5
low value (-)	400	0.5	100	3

Table 1.3. Response Surface experimental set-up.

In order to determine the effect of the deposition and annealing conditions on the device performance, TFTs were fabricated for all the experimental runs corresponding to a wide variety of polysilicon microstructures and crystallization temperatures.

The devices were characterized in the linear region for four device parameters; the effective mobility, threshold voltage, sub-threshold slope, and the leakage current. Throughout the discussion in this chapter the emphasis will be placed on the carrier mobility. The other parameters are indicated in the tables. Unlike other device parameters, the carrier mobility is dependent mainly on the polysilicon properties. Other TFT parameters, such as the sub-threshold slope, threshold voltage, and leakage current, are all strong functions of the film thickness, [1.3] which varied up to 20% from its target value. The mobility was chosen as the device parameter that measures the polysilicon material quality most independent of process variability and therefore is the best parameter in evalutating the quality of the different RTP crystallized polysilicon films.

The grain size of the polysilicon films was measured using transmission electron microscopy (TEM). The grain size was determined as the square root of the length of the long axis multiplied by the short axis. The effective mobility was calculated from the maximum trans-conductance in the linear mode with V_{DS} = 1V for n-channel TFTs and V_{DS} = -1V for p-channel TFTs. The threshold voltage was determined as the voltage-intercept of the extrapolation of the linear part of the $I_D(V_{DS})$ characteristic. The sub-threshold slope was measured as the maximum slope of the [log(I_{DS}) vs. V_{GS}] plot. The leakage current was taken as the minimum drain current at V_{DS} = 5V for n-channel TFTs and V_{DS} = -5V for p-channel TFTs.

1.1.2. DISCUSSION OF EXPERIMENTAL RESULTS.

A carrier mobility as high as 36 cm^2/V-s section and crystallization temperatures as low as 600°C were achieved. These results indicate that the high throughput crystallization method of RTP can be used for polysilicon crystallization on glass substrates and for achieving adequate device performance.

Since there were 23 input variables investigated in the experiments, a large number of interesting observations and conclusions were made regarding the effect of these variables on the crystallization temperature, the polysilicon microstructure, and the resulting TFT performance. Only the most important or most interesting of these effects are discussed in this section. The following discussion focuses on the effects of three of

the most important parameters; (a) the effect of deposition method, LPCVD or PECVD, (b) the effect of source gas, and (c) the effect of using a seed layer.

1.1.2.1. EFFECT OF DEPOSITION METHOD - LPCVD OR PECVD

The deposition method was determined to be important in determining device performance and crystallization temperature, but neither method could be concluded as universally superior. Each of these two deposition methods had some advantages over the other. The LPCVD deposited amorphous silicon resulted in a greater range in device performance, but the PECVD deposited material resulted in a greater range in crystallization temperature. Figure 1.1 plots the mobility as a function of the crystallization temperature for both the PECVD and LPCVD deposited polysilicon. The LPCVD devices had a range in mobility from 0.4 cm^2/V-s to 36 cm^2/V-s while the PECVD material had a range from 7.2 cm^2/V-s to 15.4 cm^2/V-s. The LPCVD devices had a range in crystallization temperature from 698 °C to 788 °C while the PECVD material had a range of 595°C to 870°C. It is worth noting that the PECVD experiments explored scan speeds bewteen 3 mm/s and 15 mm/s while the LPCVD experiments explored only between 5 mm/s and 15 mm/s. However, even at 5 mm/s, the PECVD experiments achieved crystallization temperatures as low as 642 °C.

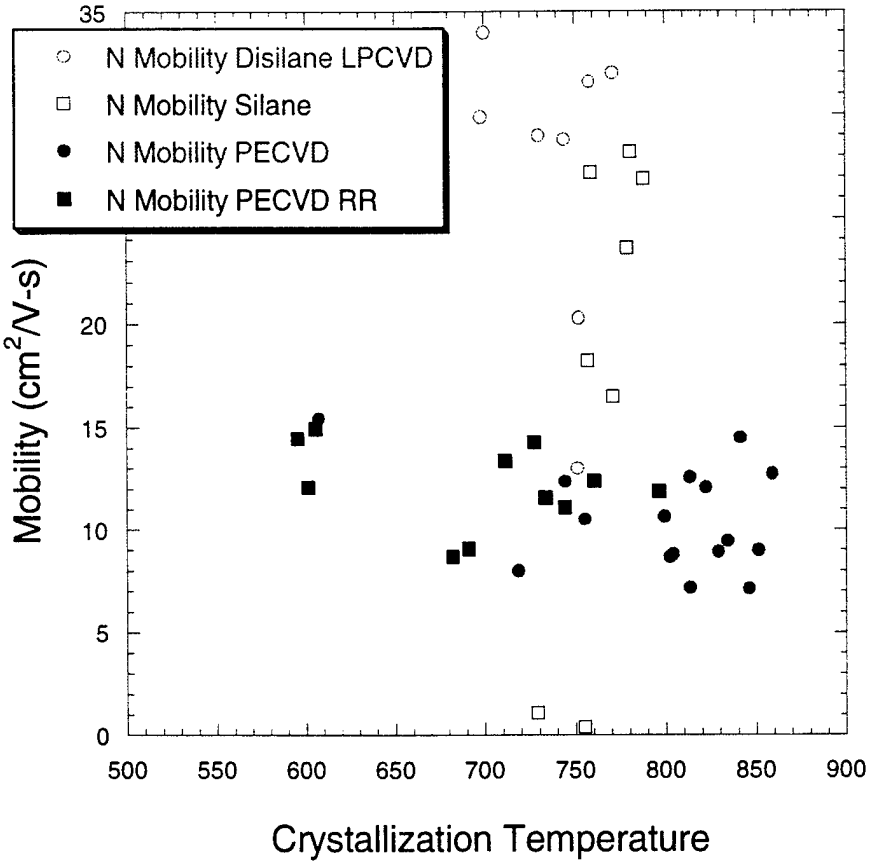

Figure 1.1. The mobility is plotted as a function of the crystallization temperature of the polysilicon material. A trend of higher mobility at lower crystallization temperatures can be seen, particularly for the LPCVD depostied material.

1.1.2.2. EFFECT OF SOURCE GAS

The choice of source gas also had a major impact on TFT performance and crystallization temperature. Using disilane as the source gas produced polysilicon with lower crystallization temperatures and TFTs with better device performance compared with using silane as the source gas. This result agrees with previous work that used furnace annealing to crystallize the films [1.4].

1.1.2.3. USE OF A SEED LAYER FOR LPCVD DEPOSITED FILMS

Lower crystallization temperatures are achieved by increasing the number of crystallites. However, this approach is not desirable because increasing the number of crystallites reduces the resulting grain size of the polysilicon film. During the LPCVD disilane experiment, one of the variables investigated was the use of a seed layer. A seed layer is a thin layer of amorphous silicon deposited prior to the actual film deposition. This seed film is optimized to have many crystallites and, as a result, have a low crystallization temperature. The film layer is engineered to have few crystallites and, on its own, a high crystallization temperature. However, when the two films are stacked together, the seed layer can induce crystallization of the film layer and result in a polysilicon layer that has a low crystallization temperature and a large grain size. Since larger grain sizes generally lead to improved polysilicon mobility, the use of a seed layer produces polysilicon films with high mobility and low crystallization temperature.

Figure 1.2. plots the TFT mobility as a function of the crystallization temperature for only those films deposited by LPCVD. This plot is a subset of the information contained in figure 1.1. It can be seen that without the use of a seed layer, lower crystallization temperatures lead to smaller grain size and lower mobility. However, the devices with a seed layer can have high mobility and low crystallization temperature.

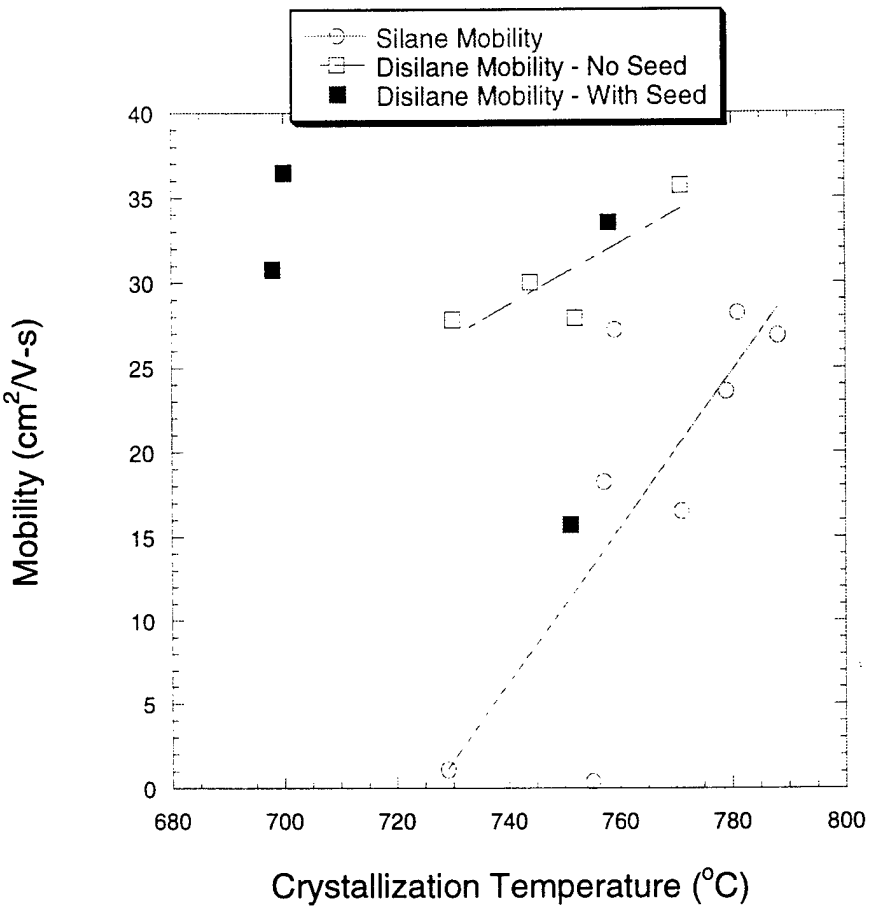

Figure 1.2. The mobility is plotted vs. the crystallization temperature for the LPCVD deposited TFTs. It can be seen that without the use of a seed layer, lower crystallization temperatures coincide with lower mobilities. However, when a seed layer is present, this trend can be avoided and high mobility was achieved at low crystallization temperatures.

1.2.0. Results on the Effect of Polysilicon Grain Size on Carrier Mobility

1.2.1. CORRELATION BETWEEN GRAIN SIZE AND MOBILITY

In order to improve device performance by altering the deposition and annealing conditions of the polysilicon film, it is best to understand the mechanism for that improvement. One property of the film that theoretically impacts the device performance is the polysilicon grain size. Previous work has indicated that the mobility is a function of the polysilicon grain size. A formulation for the mobility as a function of the grain size is

given in equation (1), where it is assumed that the grains are partially depleted and l_G represents the grain size and v_c is defined as $(kT/2\pi m_e)^{(1/2)}$ [1.5]. E_B is the barrier height caused by trapped carriers at the grain boundaries and is a function of the grain boundary defect density. An expression for E_B for a grain boundary in a polysilicon film is given in equation (2), where N_T represents the surface density of defects at a grain boundary (cm^{-2}), t_{ch} is the polysilicon channel thickness, and V_{TH} is the threshold voltage of the TFT [1.6]. Equation (1) indicates that an increase in grain size should lead to an increase in the carrier mobility.

$$\mu_{GB} = \frac{qv_c}{kT} l_G e^{\frac{-E_B}{kT}} \tag{1}$$

$$E_B = \frac{q^3 N_T^{\ 2} t_{ch}}{8\varepsilon_s C_{ox}(V_{GS} - V_{TH})} \tag{2}$$

Figure 1.3 plots the measured mobility as a function of the grain size for all of the deposition and annealing conditions considered in this work. It can be seen that, as a general trend, larger grain sizes lead to higher mobility as predicted by equation (1), but that the improvement of mobility with increasing grain size tends to saturate at large grain sizes. This saturation can be explained as being a result of intra-grain defects that exist in the polysilicon film. Due to the solid phase crystallization process that occurs during the RTP process, many defects within a grain may exist. These defects within a grain can trap charges and behave as coulombic scattering centers. When the contribution of the intra-grain defects is considered, the total mobility can be written according to equation (3) as a sum of the grain boundary limited mobility as well as the intra-grain mobility that is limited by coulombic scattering. An expression for the intra-grain mobility is given in equation (4) where N_I is the density of coulombic scattering centers [1.7].

$$\frac{1}{\mu_{Total}} = \frac{1}{\mu_{GB}} + \frac{1}{\mu_{IG}} \tag{3}$$

$$\mu_{IG} = \frac{113\varepsilon_s^{\ 2}(2kT)^{\frac{3}{2}}}{N_I q^3 m^{*\frac{1}{2}}} \left\{ \ln(1 + (\frac{12\pi\varepsilon_s kT}{q^2 N_I^{\frac{1}{3}}})^2 \right\}^{-1} \tag{4}$$

From the data in figure 3.5, the coefficient of grain boundary limited mobility can be extracted from the region of small grain size. Knowing this value, the intra-grain mobility can be extracted by a using a best fit of equation 3 with the data. The intra-grain mobility for this solid phase crystallization process was extracted to be 58 $cm^2/V\text{-}s$. Using this value and using equation (4) and assuming that each defect in the film results in a coulombic scattering center, the average level of intra-grain defects in these polysilicon films is extracted to be $3x10^{19}$ cm^{-3}.

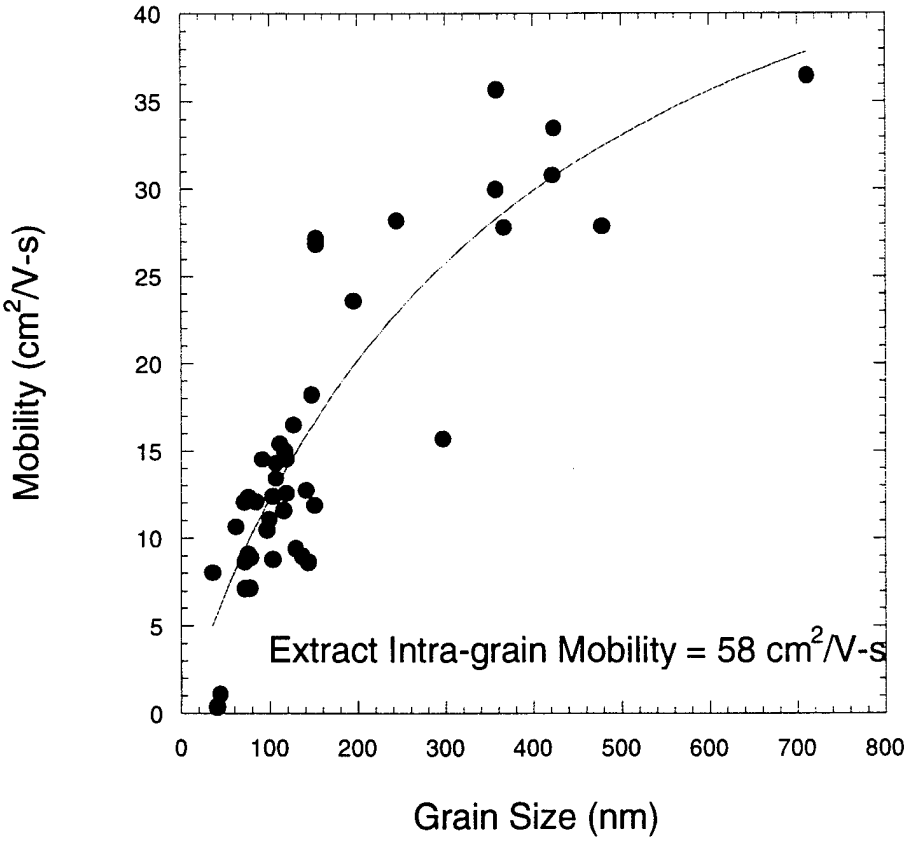

Figure 1.3. The mobility is plotted as a function of grain size.

Section 2. Polysilicon Display Driver Circuits

Throughout this DARPA grant, much work was done on polysilicon display driver circuits. We have demonstrated polysilicon display driver circuits using the low cost, high throughput RTP crystallization process. Among the circuits that have been demonstrated are shift registers, ring oscillators, buffers, operational amplifiers and DACs. We have fabricated some shift register designs operating at clock frequencies as high as 20 MHz. We have demonstrated a trade-off between the mobility of the polysilicon and the gain of operational amplifiers. We have developed our own shift register design improvements.

This work done for this fellowship included the design, simulation, layout, fabrication and testing of all the above mentioned circuits.

2.1.0. Results on Low Temperature Display Driver Circuit Performance

This section describes my results concerning the functionality of the necessary components of integrated drivers in RTP crystallized polysilicon. These components include buffers, shift registers, operational amplifiers and DACs. These circuits were fabricated using the silicon wafers that were processed for the PECVD screening and response surface experiments discussed in the previous section. The n channel transistors had an average mobility in the range of ~15.0 $cm^2/V\text{-}s$ while the p channel transistors had an average mobility of ~11.0 $cm^2/V\text{-}s$.

2.1.1. LOW TEMPERATURE DRIVER CIRCUIT DESIGN

In this section, the design buffers, shift registers, operational amplifiers and digital to analog converters is discussed.

2.1.1.1. DIAGNOSTIC CIRCUITS - RING OSCILLATORS

Diagnostic circuits can be used to determine the maximum possible speed of a logic gate fabricated with RTP crystallized polysilicon TFTs. The ring oscillators used in this study contained 19 CMOS gates. Each inverter consists of a NAND gate with its two inputs connected together. This W/L ratio of the n channel TFTs and the p channel TFTs was 20μm /4μm. A schematic of the ring oscillator is shown below in figure 2.1.

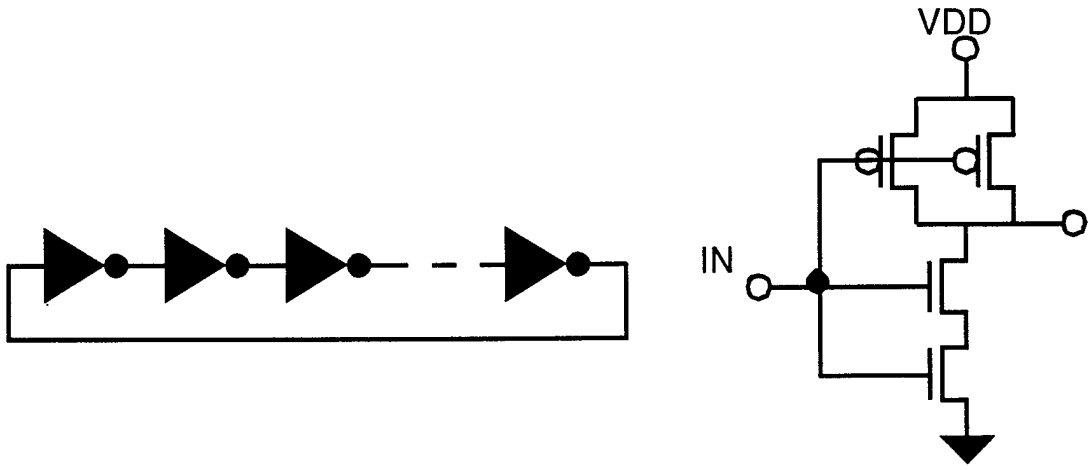

Figure 2.1. This figure shows the ring oscillator structure on the left and the internal inverter structure on the right.

2.1.1.2. BUFFERS

A buffer is useful in reducing the output impedance of a digital circuit as well as in isolating that circuit from its load. In the case of display drivers, the buffer is used to isolate the shift register and the address lines. In this work, both NMOS and CMOS buffers have been characterized to determine their rise times for a 30 pF load. Each buffer contains 4 stages with the NMOS stages having W/L ratios of 20, 45, 90 and 180 and the CMOS stages having W/L ratios of 10, 25, 50, and 100. For the NMOS buffers, the saturation load TFT has a W/L ratio of 1/10 that of the drive TFT. The channel length was 8 microns for all buffer TFTs.

2.1.1.3. SHIFT REGISTERS

Twelve different shift register architectures were investigated to determine which designs are most compatible with the properties of the RTP crystallized polysilicon transistors. Table 2.1 summarizes some of the of the important features of the designs that were investigated in the most detail.

Figures 2.2 and 2.3 show the design schematics of the dynamic, pseudo-static, and static approaches. The dynamic approach has the lowest transistor count (5 per stage) which can lead to higher yield. The static design, an NMOS design based on clocked D Flip Flops (DFFs), requires 8 transistors per stage but does not require low

leakage current transistors. The pseudo-static designs require 6 TFTs per stage. The static and CMOS dynamic designs were not buffered and could be tested only up to speeds such that they could drive the input capacitance to the probe. The other designs were buffered and the W/L ratio of the final stage is also given in Table 5.1.

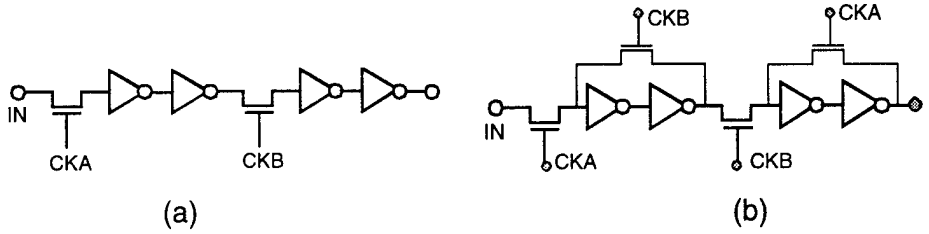

Figure 2.2. Circuit schematics of the (a) dynamic design and (b) the pseudo-static design.

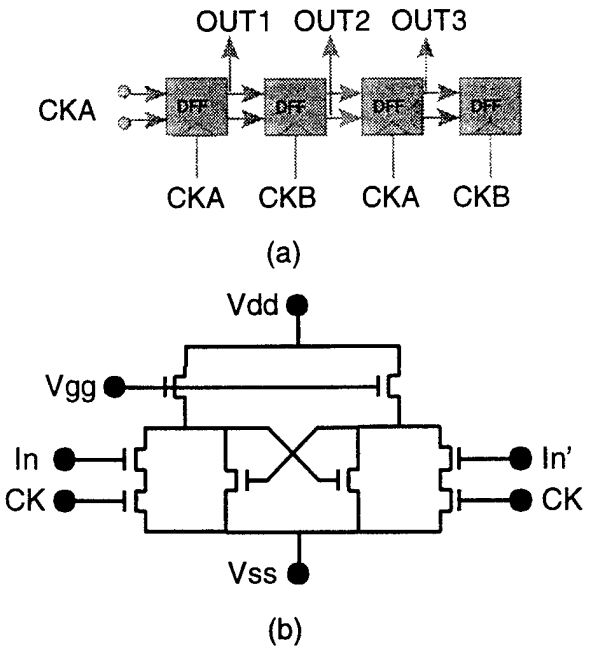

Figure 2.3. Schematics of the static shift register design showing (a) the block diagram and (b) the D-Flip Flop internal circuit schematic.

Table 2.1. Overview of shift register designs to be investigated.

Design		Technology	TFTs per Stage	Cell Pitch	Pass TFT W/L (um)	Buffer W/L
Static	D Flip-Flop	NMOS	8 T	70 um	x	x
Dynamic	Inverter Chain	CMOS	5 T	48 um	(80 / 8)	x
		NMOS	5 T	48 um	(12 / 4)	180,18
		NMOS	5 T	48 um	(12 / 4 (offset))	180,18
Pseudo-static	Inverter Chain	CMOS	6 T	36 um	(20 / 4)	50,50
		NMOS	6 T	48 um	(12 / 4)	30,3

2.1.1.4. OPERATIONAL AMPLIFIER DESIGN

An operational amplifier design was desired with maximum gain and minimum complexity to demonstrate the feasibility of op-amp design with RTP crystallized polysilicon TFTs. The design chosen was a CMOS uncompensated design containing 9 TFTs. Figure 2.4 shows a circuit schematic of the op-amp [2.1]. The 10 μm channel length was chosen to provide better saturation TFT behavior. The width to length ratio of the output stage is 50.

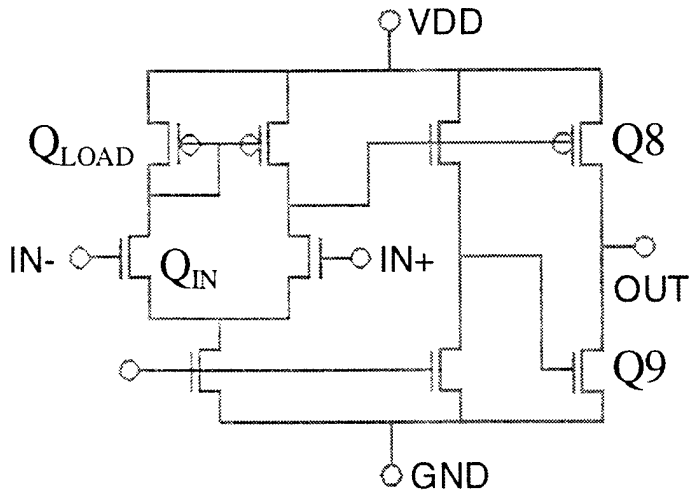

Figure 2.4. Uncompensated operation amplifier schematic [2.1].

2.1.1.5. DIGITAL TO ANALOG CONVERTER DESIGN

Our goal in the design of the DAC was to achieve proper digital to analog conversion with the simplest design. For these reasons a current based DAC architecture was used. Low transistor count is critical in large area electronics where yield is an important issue. This design, shown in figure 2.5, requires 4 transistors for 3-bit conversion and would require one additional TFT for each additional bit of resolution.

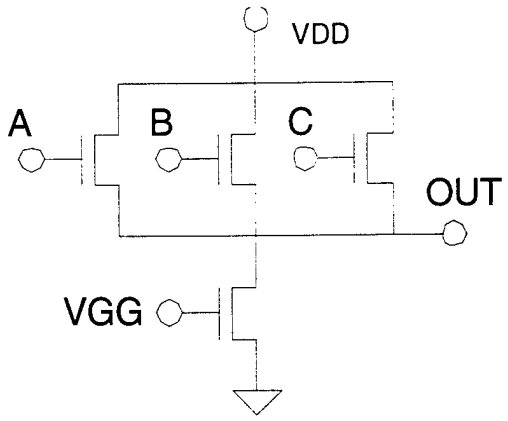

Figure 2.5. Current based 3 bit DAC design.

2.1.2.0. LOW TEMPERATURE CIRCUIT PERFORMANCE

2.1.2.1. DIAGNOSTIC CIRCUITS – RING OSCILLATORS

The oscillation period of the ring oscillators were characterized as a function of the power supply voltage. Figure 2.6 plots the delay per gate as a function of the supply voltage. At a supply voltage of 26 Volts, a gate delay as low as 5 ns was achieved. This indicates a maximum circuit frequency of 100 MHz. This speed is above what is required for integrated display drivers for VGA sized displays. Figure 2.6 also illustrates the difference between using silicided devices and low resistance silicided gate interconnects compared with using a standard highly doped polysilicon gate process. It can be seen that the silicidation process improves the circuit speed by approximately 10%.

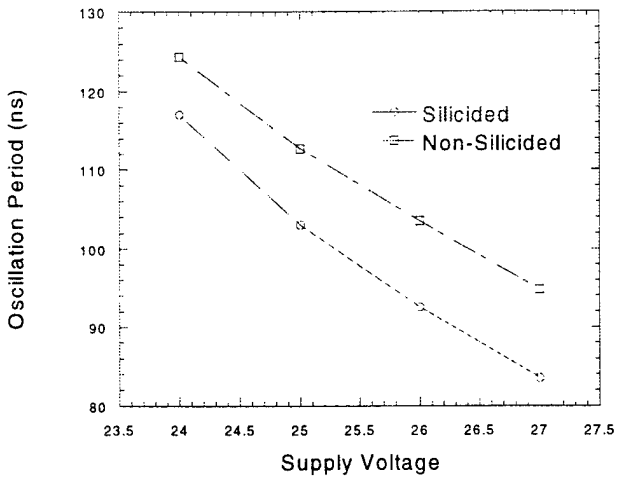

Figure 2.6. Oscillation period of a 19 stage ring oscillator as a function of the power supply voltage. The data is shown for both silicided and non-silicided ring oscillators.

2.1.2.2. BUFFER CHARACTERIZATION

Both the NMOS and CMOS buffers were tested to determine their rise and fall times. A 30pF load was used. Figure 2.7 plots the rise and fall times of the two buffer technologies as a function of the supply voltage. The expected trade-off between operating speed and supply voltage is evident. Also as expected, the NMOS technology consumed far more power than the CMOS technology for the same rise time (2 mW/stage compared to 0.001 mW/stage for V_{DD}=20V). However, the CMOS technology required higher operating voltages to achieve microsecond rise and fall times (30V compared to 22V). This is due to a higher p-channel TFT threshold voltage compared with the n-channel TFT threshold voltage for the low temperature RTP crystallized material.

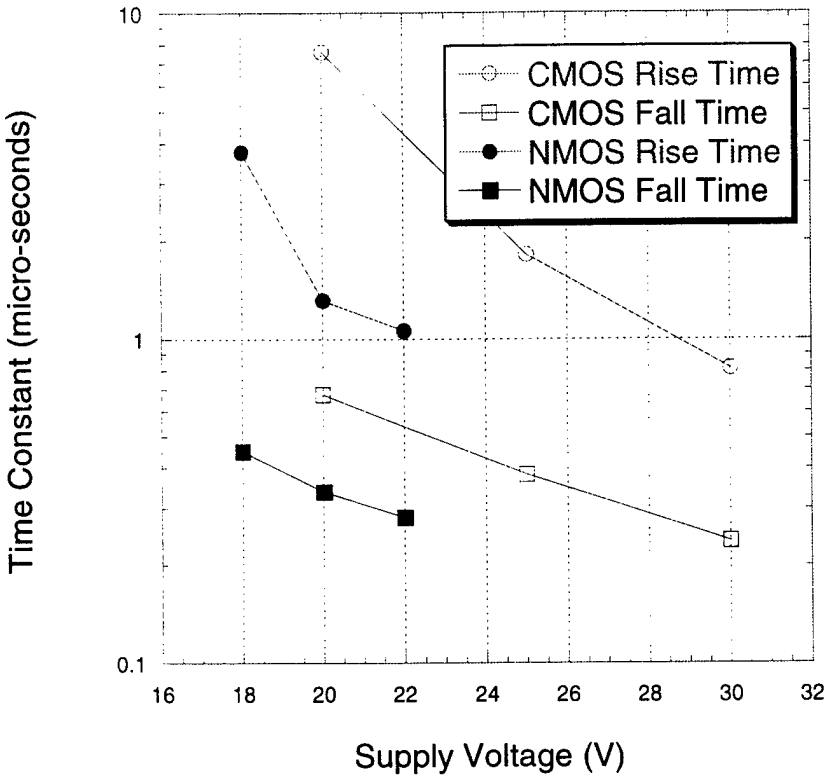

Figure 2.7. Rise and fall times of NMOS and CMOS buffers. C_{LOAD} = 30 pF.

2.1.2.3. SHIFT REGISTER CHARACTERIZATION

The designs listed in Table 2.1 were fabricated and characterized and their performance is summarized in Table 2.2. The first column lists the supply voltage for which the register was tested and the second column lists the DC power consumed through the supply terminal. The minimum operating frequency is the minimum speed that the register was driven where it still functioned. This parameter provides insight into the leakage current of the pass transistors. The lower the TFT leakage current, the lower the minimum operating frequency. It can be seen from Table 2.2 that the NMOS dynamic design using offset devices (TFTs optimized for lower leakage current) has a lower minimum operating frequency than the same design using the standard self-

aligned TFT structure. All designs were tested using a clock high voltage of 15 V and a clock low voltage of 0 V.

It can be seen from Table 2.2 that all of the designs except for the static design are able to operate in the MegaHertz frequency range. Figure 2.8 shows the timing diagram for the dynamic NMOS register (48 μm pitch) operating at a clock frequency of 30 kHz. This is the required speed for a shift register as an integrated scan driver for a VGA sized display operating at 60 frames per second. The non-overlapping clocks are shown as well as the input and the outputs of the 2nd, 4th, 6th and 8th stages with relation to the input signal. It can be seen that the subsequent stages are each properly shifted by one clock cycle.

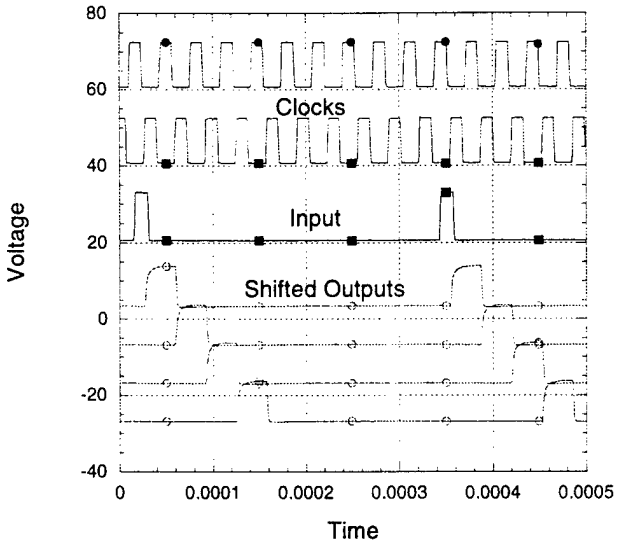

Figure 2.8. Timing diagram showing the shifted outputs of a dynamic NMOS register operating at 30kHz. The 2 clocks, outputs and the input are shown.

Table 2.2. Summary of shift register performance.

Design		Technology	Supply Voltage	Minimum Speed	Maximum Speed - A	Maximum Speed - B	DC Power / Stage
Static	D Flip-Flop	NMOS	20	x	50 kHz	62.5 kHz	1.3 mW (unbuffered)
Dynamic	Inverter Chain	CMOS	20	18 kHz	> 2.5 MHz	17 MHz	0.019 mW (unbuffered)
		NMOS	20	230 kHz	1.4 MHz	1.7 Mhz	16 mW
		NMOS(offset)	20	100 kHz	2 MHz	1.4 MHz	16 mW
Pseudo-static	Inverter Chain	CMOS	20	250 kHz	> 2.5 Mhz	20 MHz	0.13 mW
		NMOS	20	180 kHz	> 2.5 MHz	12.5 MHz	1.8 mW

2.1.2.4. OPERATIONAL AMPLIFIER CHARACTERIZATION

The CMOS operational amplifier design was fabricated and characterized for both ac and dc performance. The unity gain point for the design is greater than 200 kHz for a supply voltage of 15 V and increases with increasing supply voltage. The op amps had a maximum DC gain of 500 (54 dB) depending upon the polysilicon material properties

2.1.2.5. DIGITAL TO ANALOG CONVERTER CHARACTERIZATION

The DAC design was fabricated and tested for functionality at low frequencies. Figure 2.9 plots the output voltage of the DAC as a function of time. The 3 input bits were varied with time to raster from the case of the digital inputs being all high to the case of the digital inputs being all low. The bits were changed at a frequency of 1.2 kHz. This sequence was then repeated in time at a frequency of 150 Hz. The output voltage range of the DAC was between 0 and 0.5 Volts. This smaller range can be amplified to the desired range using analog amplification methods, such as an op-amp.

It can be seen from figure 2.9 that the output is not completely linear with the input bit sequence. This is because the resistance of the amount of current flowing through the input transistors is a function of their gate to source voltages. The source voltage depends directly upon the output voltage of the DAC. If the output voltage changes are small, the linearity can be improved. This can be accomplished by reducing the resistance of the load TFT by increasing the voltage on its gate (Vgg). The linearity of the design also may be improved by using p-channel TFTs as the input transistors. If operating in saturation, this eliminates the dependence of the input TFT current on the output of the DAC.

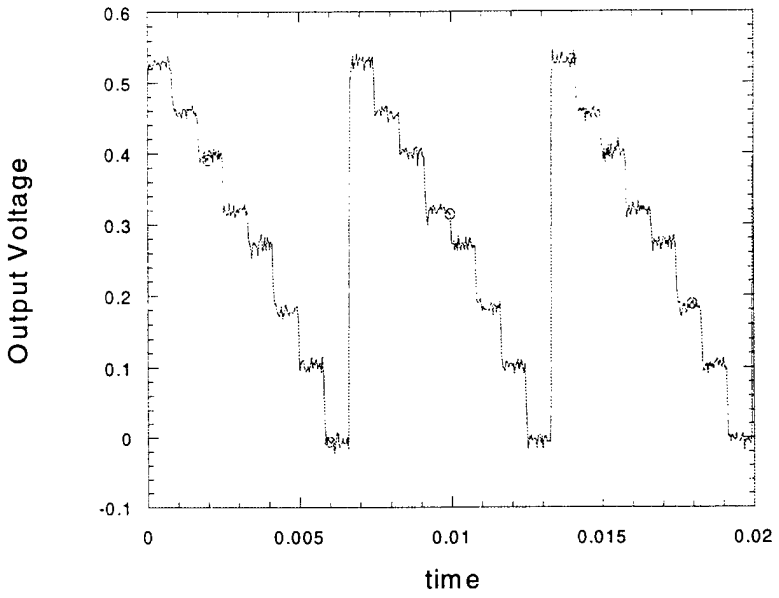

Figure 2.9. Plot of DAC output voltage as a function of time. The input bits are changed at a rate of 1.2 kHz.

2.1.3. CONCLUSIONS

This work shows that RTP polysilicon is a viable material for integrating driver circuitry onto the display panel. Both digital and analog circuits, suitable for AMLCDs and AM-OLED displays, have been demonstrated for the first time in RTP crystallized polysilicon material. Ring Oscillators indicate a maximum logic gate operation speed of 100 MHz at Vdd = 28V. NMOS and CMOS buffers have been fabricated and tested to have rise and fall times less than 1 μs for a 30 pF load. Multiple shift register designs have been characterized, and operating speeds greater than 20 MHz were achieved. Functional DACs and operational amplifiers have also been demonstrated and an open loop gain as high as 500 V/V was achieved.

2.2.1.0. Improved Dynamic Shift Register Design.

2.2.1.1. IMPROVED SHIFT REGISTER DESIGN

The shift register is an important circuit component for integrated drivers and it is desirable to have a shift register design that can function over as broad a frequency

range as possible. This work discussed in this section discusses the implementation of a double gate pass TFT structure to improve the operating frequency range compared with either the self-aligned or LDD TFT structures. The structure consists of a modified LDD pass TFT structure, but with the addition of a second control gate that is used to modulate the conductivity of the lightly doped regions of the LDD device. When a positive bias is applied to the control gate, the concentration of carriers in the LDD regions is increased. This extra terminal can provide an increase in the ON current of the device without sacrificing the low leakage current behavior of the LDD structure. This operation of this device is similar to other device structures aimed at increasing the concentration of carriers in the LDD region [2.2,2.3]. A cross section of this device structure is shown in figure 2.10.

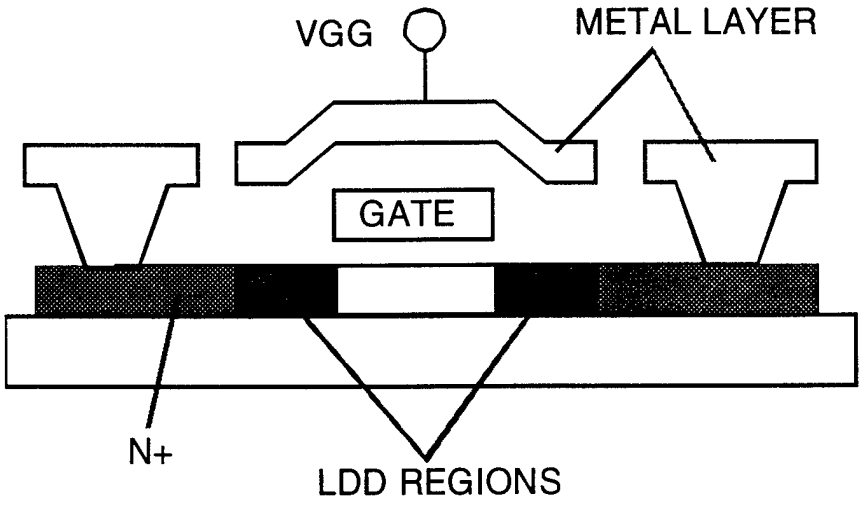

Figure 2.10. Cross section of modified pass gate TFT structure.

2.2.2. IMPROVED SHIFT REGISTER PERFORMANCE

Figure 2.11 plots the transfer characteristics of the standard LDD (V_{GG}=0V) and the double gated pass TFT structure. The characteristic of a self-aligned TFT is shown for comparison. It can be seen that the gated LDD device has a greater ON-OFF ratio compared to the standard LDD device and therefore is expected to lead to a greater range of operating frequency when applied to the dynamic register design.

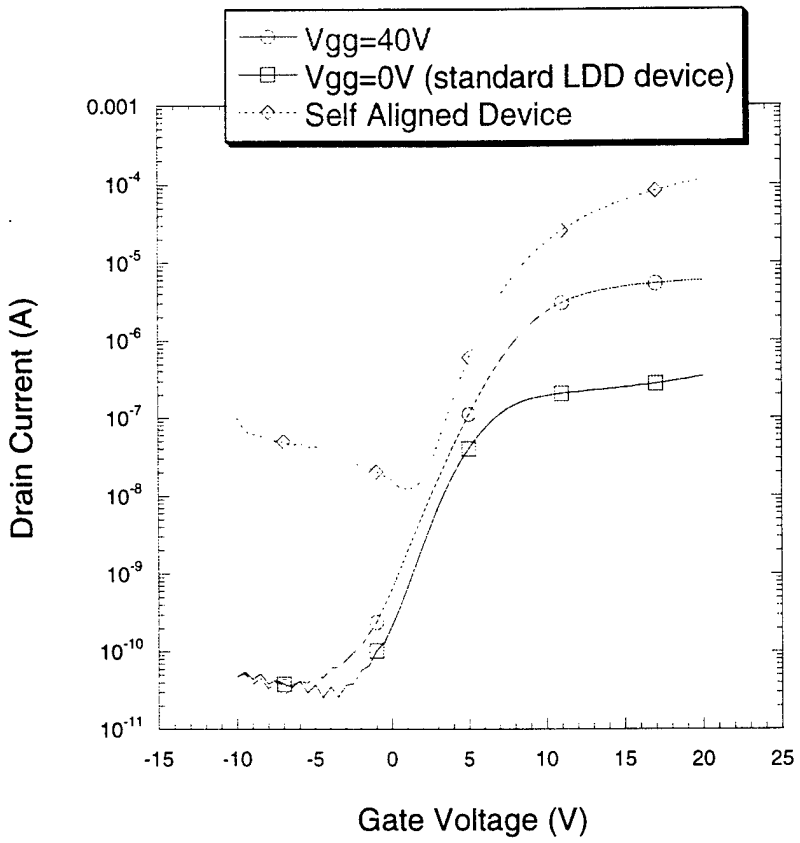

Figure 2.11. Transfer characteristics of the standard LDD structure (V_{GG}=0V), gated LDD structure, and self-aligned TFT structure.

The dynamic registers with the different pass TFT structures behaved as expected with respect to their minimum and maximum operating frequencies. Figure 2.12 plots the minimum and maximum frequency of the dynamic shift register design as a function of the gate voltage over the LDD (V_{GG}) regions. All registers were tested for V_{DD}=17V. The standard LDD structure is equivalent to the case where V_{GG} = 0V. According to figure 2.12, the standard LDD device achieved the lowest minimum operating speed of 500 Hz, but the increase of the minimum speed with increasing V_{GG} was minor. Even for V_{GG} = 40 V, the minimum operating frequency has only increased to 730 Hz. However, the increase in maximum frequency with increasing V_{GG} was far more significant. The maximum operating frequency of the register using the standard LDD structure (V_{GG} = 0 V) was 49 kHz while the maximum operating frequency for the case of V_{GG} = 40 V was 333 kHz.

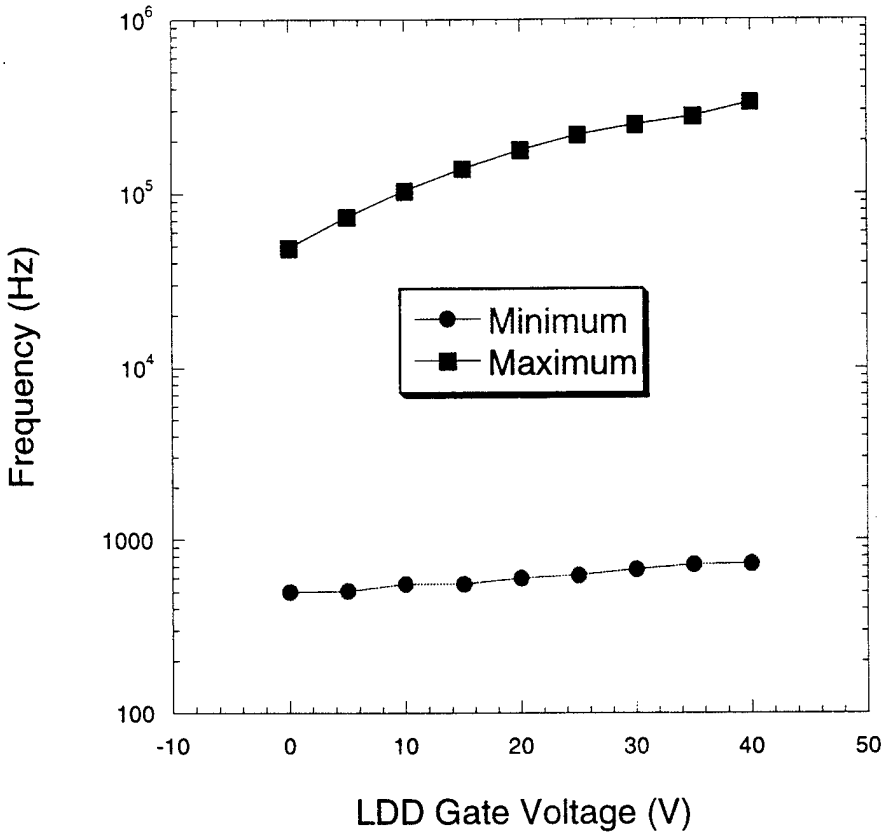

Figure 2.12. Plot of the minimum and maximum frequency for the dynamic as a function of V_{GG}. The register with V_{GG} = 40 V has the greatest range of operating frequency.

2.2.3. CONCLUSIONS.

A design improvement for dynamic shift registers fabricated with low temperature polysilicon TFTs has been described. A greater range of operating frequency was achieved using a gated LDD device structure for the pass gate of the dynamic register (f_{MAX}/f_{MIN} = 450). This was more than four times greater than that achieved using a standard LDD pass gate structure (f_{MAX}/f_{MIN} = 100). This improvement in operating frequency range is explained by an increase in the ON current of the pass gate without a significant increase in the leakage current. This increase in operating frequency range is important to low temperature integrated display driver circuit design. The greater range

of operating frequency provides more tolerance to limitations in device performance and indicates an improvement in register design.

2.3.0. Results Regarding the Trade-Off Between Mobility and Op-Amp Gain

2.3.1. TRADE-OFF BETWEEN MOBILITY AND GRAIN SIZE

This section describes a trade-off between the carrier mobility and the gain of an operational amplifier. In general, we wish to fabricate TFTs with high mobility and amplifiers with high gain. However, in this section we describe some of our results that indicate that these two goals are in conflict.

The theoretical gain of the op-amp that was investigated in this work is given by equation (1) [2.1]. It can be seen from equation (1) that the op-amp gain can be increased by increasing either the TFT trans-conductance or by reducing the TFT saturation conductance.

$$A = \left(\frac{-g_{mi}}{g_{dl} + g_{di}} \right) \left(\frac{g_{m8} + g_{m9}}{g_{d8} + g_{d9}} \right) \qquad (1)$$

The CMOS operational amplifier design was fabricated and characterized for AC and DC performance. The AC performance was already presented earlier in this section. The op amps had a large variance in DC gain ranging from less than 100 to over 500 depending upon the polysilicon material properties. In general, the goal is to achieve as large gains as possible. In order to maximize the operational amplifier gain it is necessary to understand how the TFT performance impacts the DC op-amp gain. Equation 8 indicates that larger g_m and smaller g_d lead to increased DC op-amp gain. Polysilicon TFTs fabricated in larger grain size polysilicon are known to have higher mobility. Increasing the mobility increases the g_m and hence should increase the op-amp gain. However, we found that smaller grain sizes have a reduced g_d by reducing the channel length modulation effect and thereby also increase the op-amp gain. To investigate the effect of polysilicon microstructure on op-amp DC performance, operational amplifiers were measured for a variety of low temperature polysilicon materials having a variety of mobility values

Figure 2.13 plots the DC open loop gain as a function of the carrier mobility at a supply voltage of 20V. From this plot, it is clear that larger op-amp gain is achieved using polysilicon material with smaller mobility. Apparently, even though these materials

have smaller g_m, they also have smaller g_d which leads to an increase in the open loop gain. This observation and understanding is important in optimizing the polysilicon material not only for device performance but also for circuit and system performance.

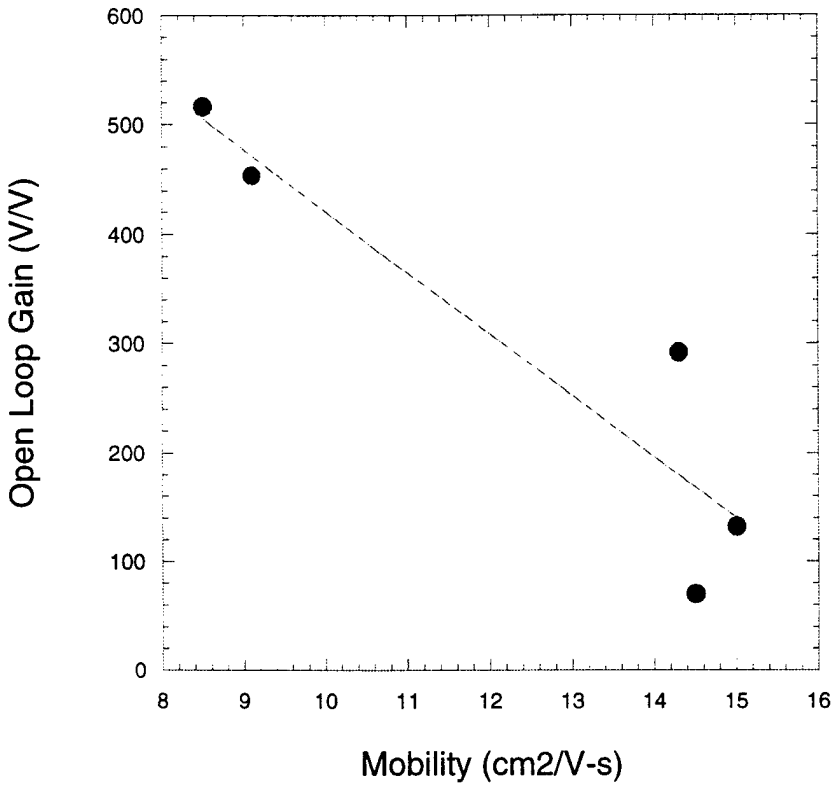

Figure 2.13. The DC open loop op-amp gain is plotted as a function of the polysilicon carrier mobility. Smaller mobility leads to larger open loop gains.

Section 3. Results on AM-OLED Displays

3.1. OLED DISPLAY DESIGN APPROACH.

Both the one and two transistor per pixel designs were considered in this work. Figure 3.1 shows a schematic of these architectures. Other architectures have also been proposed to improve brightness uniformity by correcting for variations in the transistor threshold voltage (≥ 4 transistors per pixel) [3.1]. Our approach attempts to reduce brightness variations across the substrate through processing improvements rather than circuit design corrections.

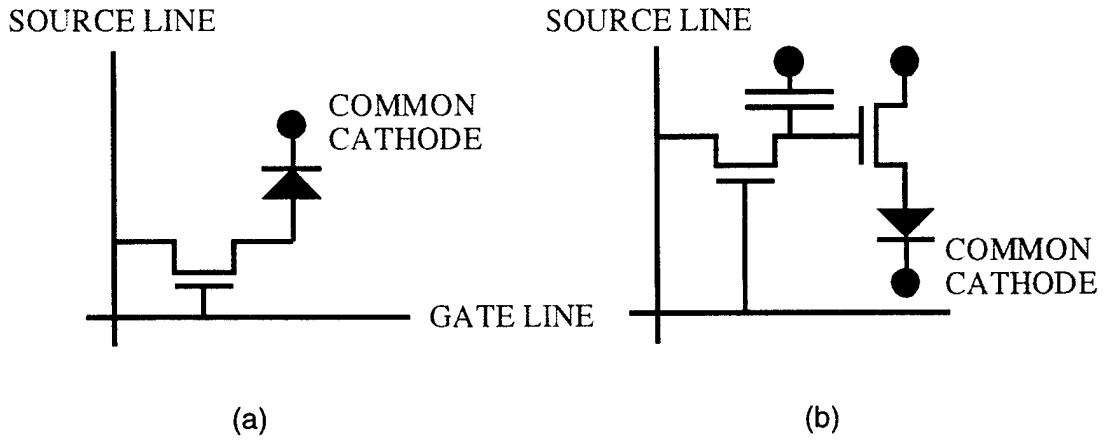

Figure 3.1. Pixel design schematics showing (a) the single TFT per pixel design, and (b) the two TFT per pixel design.

3.2. DISPLAY PROCESSING.

This section describes a fabrication process used to realize both pixel designs. In both architectures (1 transistor per pixel and 2 transistors per pixel), the current passes out of a transistor and into the organic light emitting diode structure. Since the transistor controls the current through the OLED material, the uniformity of the transistor threshold voltage, carrier mobility, and series resistance is crucial to the final performance of the display array. This is because, to first order, the saturation TFT current can be written as shown in equation (2) where R_s represents a sum of both the series and contact resistance, μ_p represents the hole mobility, and V_{TH} represents the threshold voltage. To reach this equation (2) it has been assumed that the mobility degradation due to surface scattering is not significant.

$$I_{DS} = \frac{\frac{W}{2L}\mu_p C_{ox}(V_{GS} - V_{TH})^2}{1 + \frac{W}{L}\mu_p C_{ox} R_s (V_{GS} - V_{TH})} \quad (2)$$

It is evident from equation (2) that variations in the threshold voltage, carrier mobility, or series resistance will directly impact the uniformity of the TFT current and consequently, the brightness of the display. In this work, a variety of steps were implemented to reduce the series resistance and improve the uniformity of the pixel electrical characteristics. The carrier mobility and threshold voltage variations were reduced through the use of rapid thermal processing (RTP) for polysilicon crystallization to achieve uniform polysilicon microstructure. A silicidation process was developed to eliminate TFT series resistance and a low resistance contact scheme was developed to connect the ITO to the drain of the TFT. Finally, a planarization scheme based on spin on glasses (SOGs) was used in order to provide a smooth and uniform surface prior to OLED material deposition. A cross section of the process indicating four areas were a large amount of research was done is shown in figure 3.2.

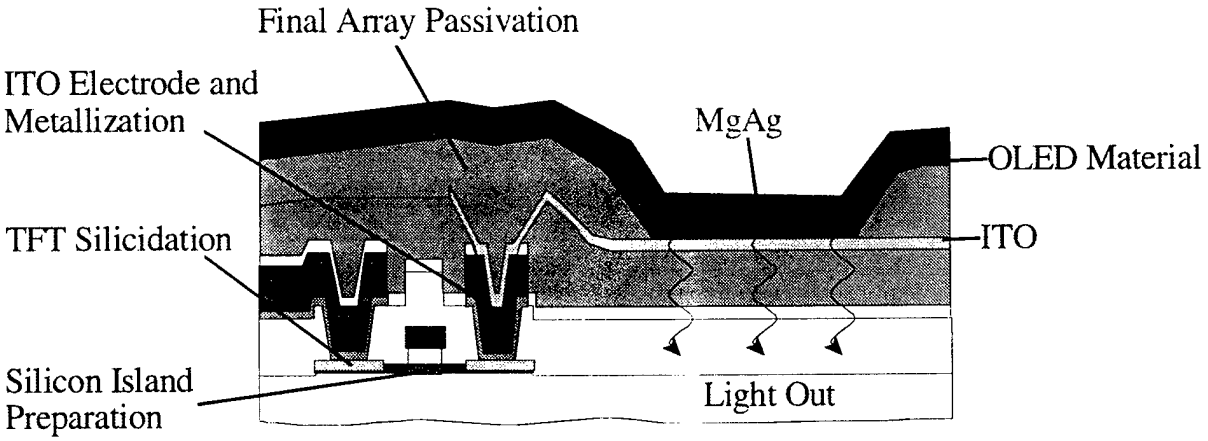

Figure 3.2. AM-OLED array process overview.

3.3. ARRAY PERFORMANCE.

There were four major process improvements that were particularly important to the final array performance. The RTP process achieved uniform polysilicon characteristics. The silicidation and ITO contact step reduced parasitic series resistance

and therefore further improved uniformity. The metallization was hillock free and prevented shorts to the OLED common cathode. Finally, the passivation and planarization produced a viable, smooth ITO surface prior to OLED material deposition.

To determine the uniformity of polysilicon TFTs crystallized using the RTP process, data was collected from wafers processed by RTP. The local uniformity was determined by measuring the standard deviation of threshold voltage over the area of one die (0.25 cm^2). The global wafer uniformity was determined by evaluating the data over an area of 10 cm^2. The local variation was 65mV for n-channel TFTs and 140mV for p-channel TFTs. The global variation was 100mV for n-channel TFTs and 150mV for p-channel TFTs. This data confirms that the RTP crystallization process leads to highly uniform polysilicon TFTs.

The silicidation process also was found to improve the uniformity of the TFTs. Figure 3.3 shows a cumulative probability plot comparing TFTs fabricated with silicides to TFTs fabricated without silicides. For a large group of silicided or non-silicided devices, the value of V_{GS} was determined that achieved a median current level of 20 μA, at V_{DS} = 1V. Then, the individual devices were measured to determine the exact drain current of each TFT at this fixed V_{GS} value. The percent deviation from the median current (the target current) was then measured for each TFT. This graph plots the deviation in the targeted current as a function of the percentage of devices. This method takes into account both mobility and threshold voltage non-uniformity and therefore best imitates the non-uniformity in TFT pixel current.

For the graph, it is clear that the silicided devices are more uniform. For example, 80% of the silicided devices have currents that vary within 2% of each other, whereas the non-silicided devices have currents with variation greater than 5%. This increase in uniformity is attributed to a reduction in the variable series resistance.

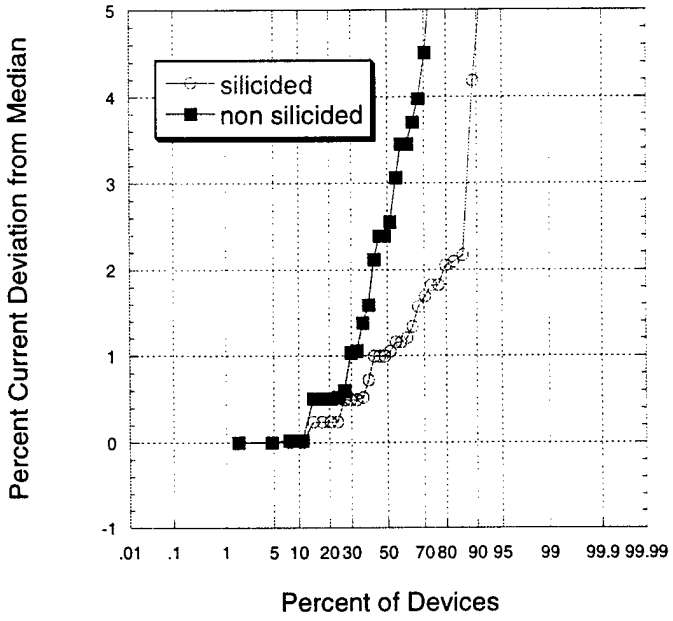

Figure 3.3. This figure shows a cumulative probability plot of TFT drain currents falling within a percentage of the median current. It can be seen that the silicided devices are more uniform.

In addition to TFT silicidation, it was also found that the method of contacting the ITO to the silicon island was critical in determining the parasitic resistance of the pixel. The series resistance resulting from connecting the ITO directly to the silicided island was intolerably high and significantly deteriorated the pixel drive current. The contact resistance using the ITO-metal-silicide contact scheme was 480 $\mu\Omega$-cm^2 at a bias of 1Volt. In contrast, the contact resistance of the ITO-silicide scheme was 33 mΩ-cm^2, even at a bias of 10V

VGA size arrays with a 4-cm diagonal were fabricated using the process described above. Figure 3.4 shows a photograph of a completed wafer prior to organic material deposition and figure 3.5 shows a microscope photograph of a completed pixel having the single TFT per pixel design. The pixel size is 50 μm by 50 μm. Figure 3.6 shows a transmission mode photograph of a pixel having the two TFT per pixel design; its pixel size is 100 μm by 100 μm.

The pixel functionality was tested by probing the ITO pad and applying test voltages to the periphery of the array. Pixel TFT characteristics were measured for n

channel and p channel wafers and for wafers with both types of ITO to island contacts. Figure 3.7 shows the transfer characteristics at V_{DS} = -1V of a p channel TFT in the single TFT pixel structure. The p channel pixel TFT has a mobility of 21 cm^2/V-s and the n channel pixel TFT has a mobility of 46 cm^2/V-s. These characteristics were measured for the case where the ITO contacts the NiSi via a metal plug. After the completion of the arrays, the OLED material was deposited and the displays were tested. An average brightness of 101 cd/m^2 was obtained at a frame rate of 60 Hz [3.2]. The operating AM-OLED display testifies to the success of the active matrix array panel and the fabrication approach discussed in this paper.

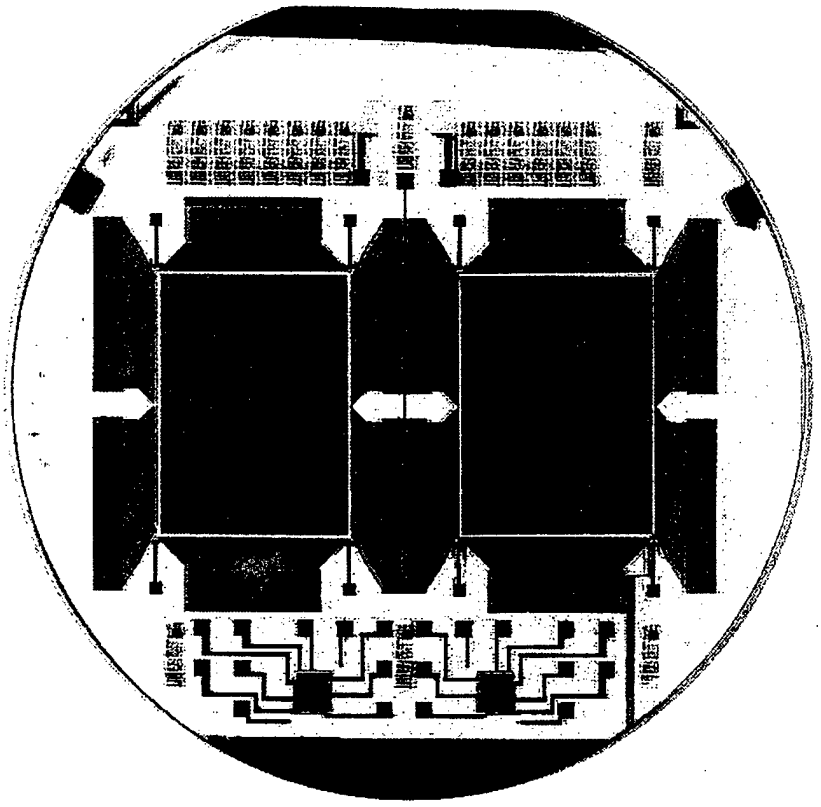

Figure 3.4. Photograph of the completed AM-OLED array.

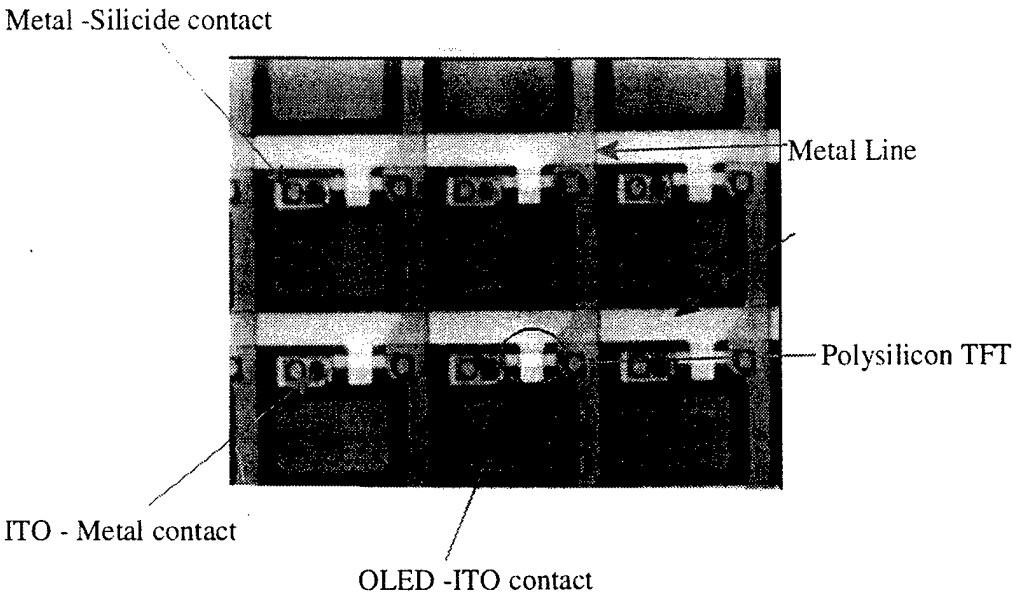

Figure 3.5. Photograph of a completed 50 μm square single TFT pixel (top view).

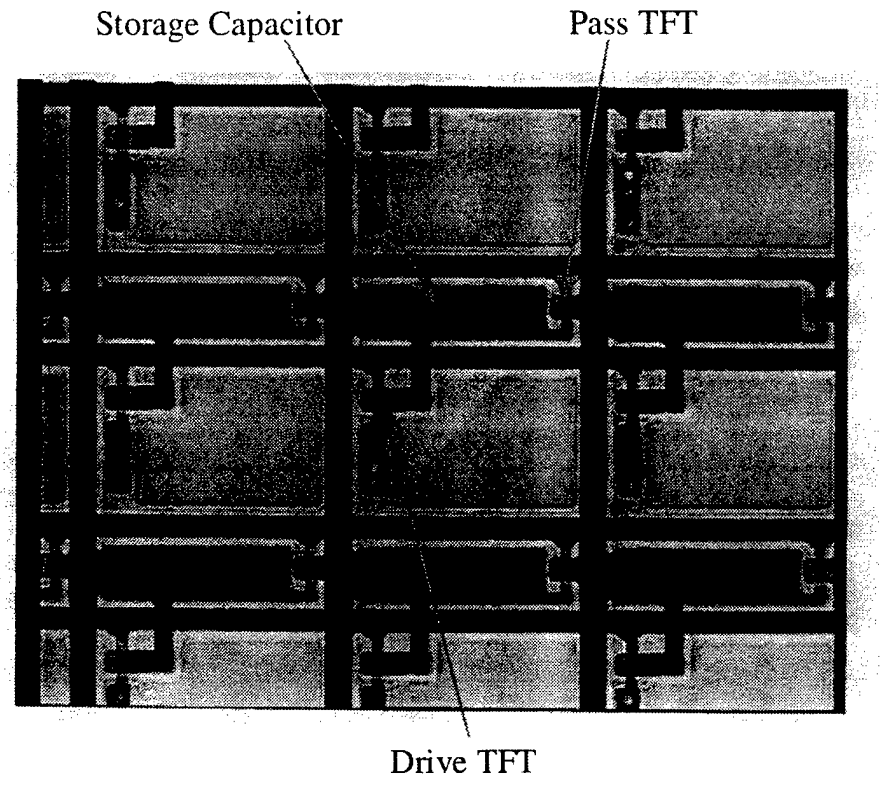

Figure 3.6. Photograph of completed 100 μm square pixel having the 2-TFT design. The pass TFT, storage capacitor and drive TFT are indicated.

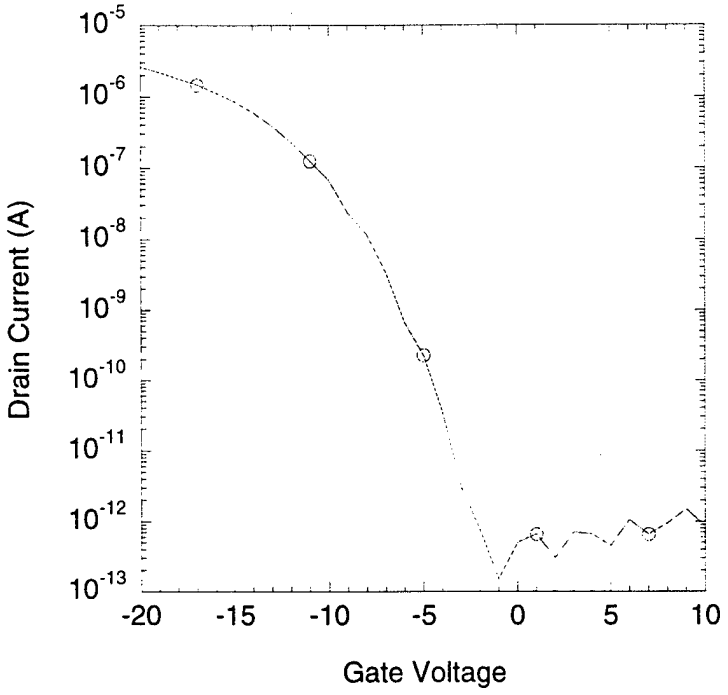

Figure 3.7. P-channel pixel TFT transfer characteristics. W/L= 4μm/8μm, V_{DS} = -1V.

A unique driving method was implemented to operate the single TFT displays that were fabricated. Normally the address line turns on the gates of all the transistors in a line at once while maintaining the rest of the gates off. The data for this line is then written to the drains of these pixel transistors. In our approach, we connect the address line to the drains of all the pixel transistors, which is the data line in the other approach. The data is then written to the gates of the transistors. Figure 3.8 shows a photograph taken from a 4 cm VGA AM-OLED display driven with this scheme.

The 2 TFT pixel design was tested for functionality. The testing was performed by illuminating alternating address lines. This method was chosen because illuminating alternate data lines does not demonstrate the sample and hold capability of the design. Good contrast was achieved indicating that this design also has promise for active matrix OLED displays using the polysilicon technology described in this paper.

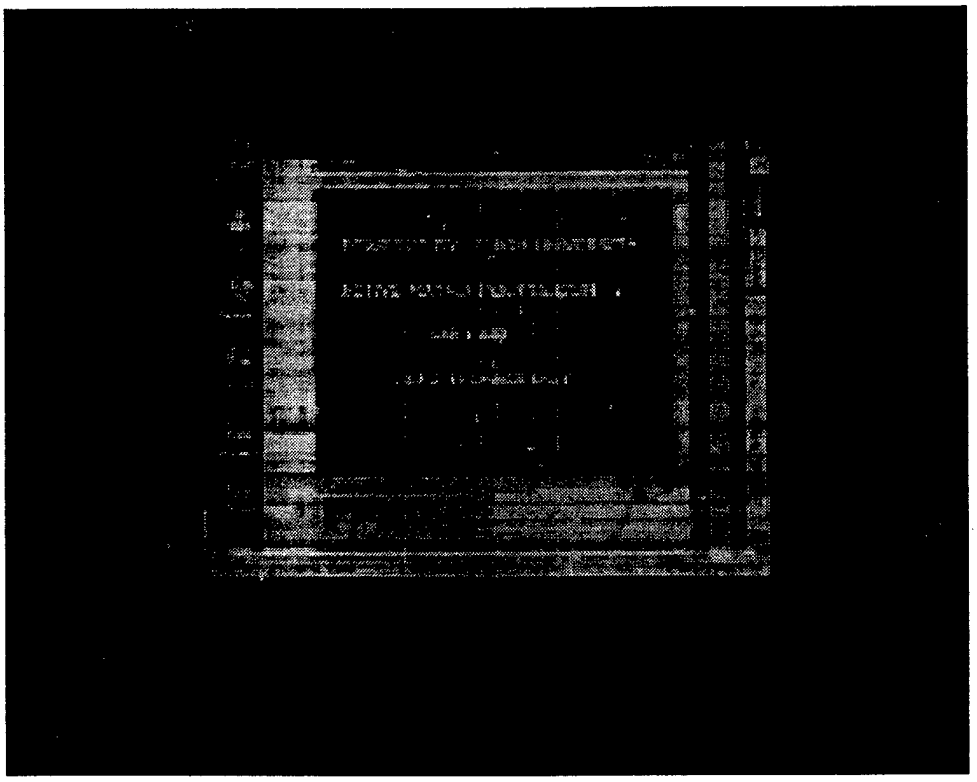

Figure 3.8. A 4 cm VGA polysilicon TFT based OLED display.

2.5. CONCLUSIONS.

A process to fabricate polysilicon TFT active matrix OLED display arrays has been described. In order to create a display with uniform brightness, a variety of steps have been introduced to reduce non-uniformity that may arise through processing. To achieve uniform transistor threshold voltage and carrier mobility, a solid phase polysilicon crystallization by rapid thermal processing (RTP) was used. TFT threshold voltage variation less than 200 mV was achieved using the RTP crystallization process. To reduce the TFT series resistance, silicides were incorporated onto the source and drain regions of the TFT and the silicides were found to significantly improve TFT current uniformity. To reduce the series resistance of the pixel, a Ti-Al-Ni metallization scheme was developed to interface the ITO and the TFT island, resulting in a good ohmic contact to the ITO. The Ti-Al-Ni metallization scheme also eliminated hillocks, which could otherwise cause catastrophic shorts in the display. Finally, spin on glasses were integrated to provide a well-planarized surface for the OLED material. The final array

pixel TFTs had effective mobilities of 46 cm^2/V-s for n channel TFTs, and 21 cm^2/V-s for the p channel TFTs. These arrays resulted in functional VGA AM-OLED displays with brightness of 101 cd/m^2.

Report of Inventions

1. A single address line used to drive two rows of pixels. This invention was a design invention that made use of a single address line addressing two rows of pixels. This was done by using both n-type and p-type transistors in the array. When the gate pulsed high, it addressed the n-type pixels, when the gate pulsed low it addressed the p-type transistors.

2. Use of a p+ polysilicon electrode as the hole injecting material for AM-OLED displays. This invention enables process simplification. A silicon electrode can be used to replace the ITO electrode for AMLCDs or for AM-OLEDs. P-type silicon can be used for AM-OLEDs as the hole-injection layer. It has the advantage of being a smooth layer and elimnates the troublesome contact between the ITO and the silicon.

3. A robust static shift register design. A robust static shift register design was designed, fabricated and tested. The register operation is not a significant function of the TFT leakage current. This is of particular use in high throughput polysilicon technology where the TFT performance is not very good.

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