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14. ABSTRACT

Using the Flow Modulation Epitaxial Technique in an Organometallic Vapor Phase Epitaxial (OMVPE) reactor, we have discovered a simple process which produces epitaxial lateral overgrowth (ELO) of GaN-based materials directly on SiC sapphire and silicon substrates patterned with silicon nitride. The key feature of this process is the use of a high temperature AlGaN nucleation layer which wets the exposed substrate surface and grows smoothly in mask windows without significant nucleation on the silicon nitride mask. Subsequent deposition of GaN results in relatively defect free materials grown laterally over the mask. For growth on silicon the high temperature AlGaN nucleation layer is replaced by AlN where, under proper growth conditions, high mobility 2DEG have been realized for the first time.

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Innovative Approach to AlGaInN Homoepitaxial Thin Films

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Using the Flow Modulation Epitaxial Technique in an Organometallic Vapor Phase Epitaxial (OMVPE) reactor, we have discovered a simple process which produces epitaxial lateral overgrowth (ELO) of GaN-based materials directly on SiC. sapphire and silicon substrates patterned with silicon nitride. The key feature of this process is the use of a high temperature AlGaN nucleation layer which wets the exposed substrate surface and grows smoothly in mask windows without significant nucleation on the silicon nitride mask. Subsequent deposition of GaN results in relatively defect free materials grown laterally over the mask. For growth on silicon the high temperature AlGaN nucleation layer is replaced by AlN where, under proper growth conditions, high mobility 2DEG have been realized for the first time. This final report covers research performed on the growth of AlGaN materials on silicon and the single step lateral overgrowth process.

Epitaxial Lateral Overgowth

Since the report of improved performance and reliability of GaN-based laser diodes grown on epitaxial lateral overgrown (ELO) GaN on sapphire[1], there has been a considerable interest in the deposition process and the characterization of nitride materials grown in this fashion. It was only recently established that dislocation free materials (at least within the observation limits of TEM) were obtained in severely mismatched systems, GaN on 6H-SiC substrates in this case, in regions where lateral overgrowth occurs[2]. In both of these studies, SiO_2 masks are patterned on planar heteroepitaxial GaN growth surfaces formed by the deposition of relatively standard nucleation layers followed by the growth of a GaN buffer layer. A multiple growth temperature Organometallic Vapor Phase Epitaxial (OMVPE) process was used regardless of the choice of substrate. Once the planar GaN surface is realized, the SiO_2 mask is deposited and patterned, and the ELO substrate is returned to the OMVPE reactor for a second regrowth step.

In this program a single deposition temperature, single step process is used to obtain similar quality ELO GaN materials. The regrowth step is avoided by initiating the process directly on both sapphire, 6H-SiC and silicon substrates masked with Si_3N_4. The Si_3N_4 mask material is required by this process as the $Al_{0.1}Ga_{0.9}N$ used in the nucleation step does not grow on the masked surface unlike the more commonly used SiO_2 mask.[3] The materials grown by this method exhibit similar growth features and materials quality as those grown with the conventional method requiring regrowth.

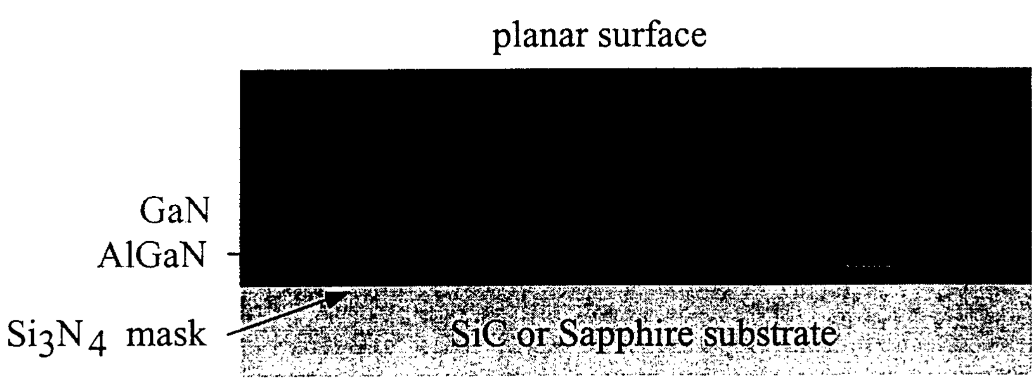


Figure 1. Schematic illustration of the single step epitaxial lateral overgrowth process.

Substrates are prepared for this process by depositing a Si_3N_4 mask, followed by patterning with RIE etching. Using arrays of stripe windows (either 2 or 4 microns wide on a 12 micron pitch) aligned parallel to the <1$\underline{1}$00> crystal direction, the entire growth surface completely planarized (parallel to the substrate surface) after roughly 5 microns of growth (normal to the substrate surface). Atomic Force Mircographs indicate atomically smooth surfaces and reveal features which correlate to threading dislocations which terminate at the crystal surface. The defect densities obtained from these images on SiC indicate a reduction from mid 10^8 to 10^3 cm^{-2} in regions over the window and over the mask, respectively. This process represents a significant simplification over currently used regrowth methods for obtaining low defect density ELO GaN materials.

The ELO growth process was carried out at a fixed susceptor temperature of 1040 °C with hydrogen and ammonia mixtures as the carrier gas in a reaction cell maintained at 76 torr. The substrates, sapphire(0001) and 6H-SiC(0001), had slightly different surface temperatures due to their substantial difference in thermal conductivity (the SiC surface was 30 °C cooler). The substrates were coated with a 700 Å thick Si_3N_4 film using plasma enhanced chemical vapor deposition (PECVD). This masking layer was patterned using standard photolithographic techniques in separate arrays of stripes consisting of 2 and 4 micron openings, each on a 10 micron pitch. The $Al_{0.06}Ga_{0.94}N$ nucleation layer was first deposited to a thickness of roughly 2000 Å. This layer is necessary for smooth growth in the mask openings. The $Al_{0.06}Ga_{0.94}N$ was not observed to nucleate on the Si_3N_4 mask in contrast to experiments carried out simultaneously on substrates with using a PECVD SiO_2 mask. The V/III ratio was increased to 1800 during the subsequent GaN growth as the lateral growth rate is reported to increase with ammonia flow.[4] The group III flux (triethylgallium and trimethylaluminum in this case) is modulated in roughly a 25 % duty cycle with a period of 10 seconds throughout the entire growth process. A schematic of the structures produced with this process is presented in Figure 1.

If GaN deposition is allowed to proceed, eventually planarization of the surface occurs resulting in very smooth morphology. Figure 2 gives SEM and AFM micrographs of a GaN laterally overgrown millimeter size mesa on an $Al_{0.06}Ga_{0.94}N$ nucleation layer. The mask consisted of 2 μm wide windows with 10 μm center to center spacing, as depicted in the Figure 2. Planarization occurs after roughly 4 microns of growth and the surface roughness is less than +/- 25 Å, where very slight depressions appear above the centers of the masked regions (indicated on image).

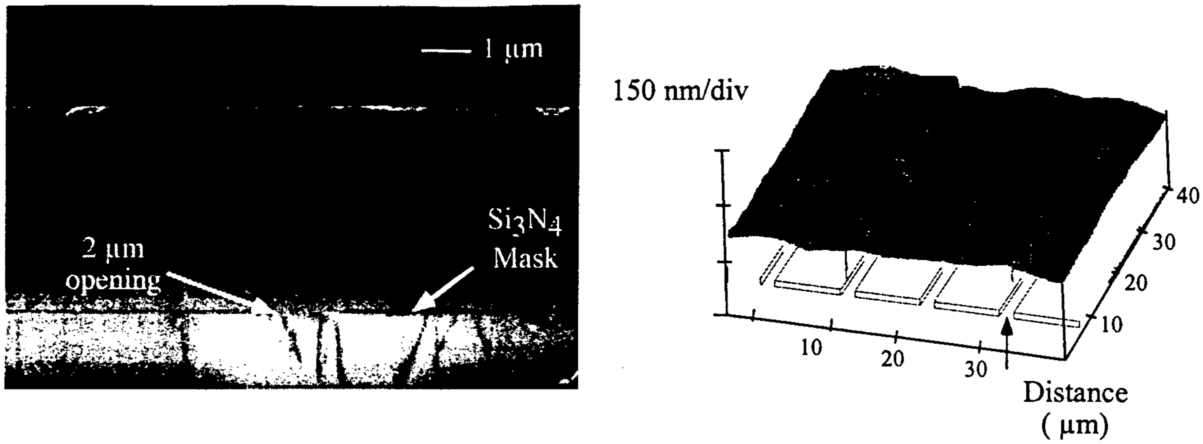
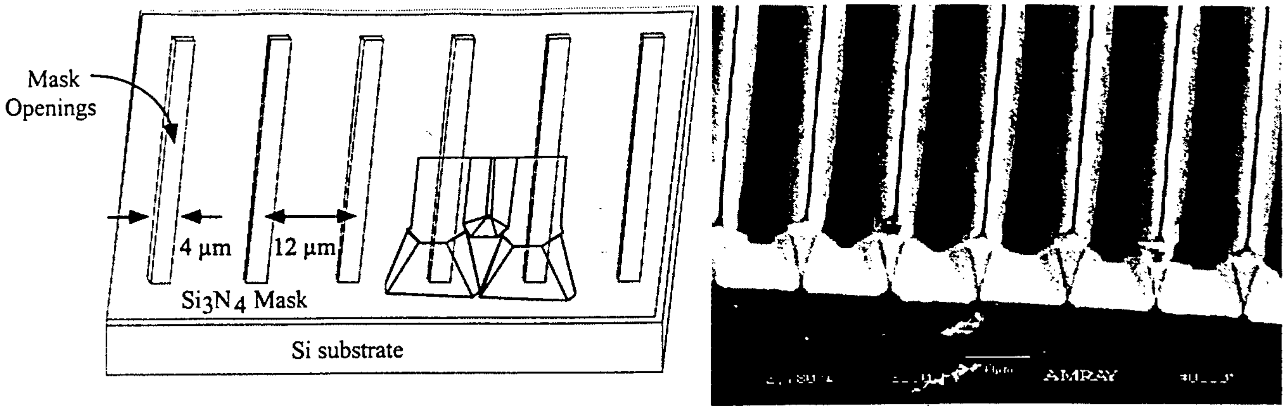


Figure 2. SEM micrograph (left) and AFM surface profile (right) of a planarized 4.5 μm thick GaN mesa grown over the AlGaN nucleation structure. The mask geometry is shown schematically under the AFM data - the windows were 2 μm wide on 10 μm centers.

We have successfully demonstrated that Flow Modulation Epitaxy results in high quality laterally overgrown GaN films on both SiC and sapphire masked surfaces. Hexagonal pyramids with heights as large as 30 μm are produced without evidence of strain induced cracking. Either triangular or trapezoidal growth features, prior to coalescence, were seen in dependence on stripe orientation. Photoluminescence measurements indicate that planarized laterally grown films are partially relaxed. Defect densities of GaN films were characterized by AFM, STEM, and SEM using chemical assisted ion beam etching. Defect densities were significantly reduced in the overgrown regions to less than 10^5 cm^{-2}. Finally, coalesced planar layers 4 μm thick were achieved on both SiC and sapphire substrates.

This technique also is applicable to growth on silicon as shown in Figure 3. In this case, the growth was stopped prior to complete planarization. The defect reduction is also observed on silicon, but film cracking did occur on samples with fully planarized surfaces.



Wire Frame of Regrown GaN
Mesa Prior to Coalescence

Figure 3. Lateral overgrowth of GaN on silicon masked with silicon nitride.

Epitaxial Growth of AlGaN Structures on Silicon (111)

There has been a considerable interest in the synthesis of GaN on (111) silicon substrates by a variety of methods including MOMBE[5], MBE with an ECR nitrogen source[6,7], HVPE[8] and OMVPE or MOCVD[7,9,10]. In addition, growth of GaN on SOI "compliant" substrates has been reported[11]. From this prior art, one can conclude that the silicon-based materials are generally not of the same quality as sapphire or SiC-based materials. Electron mobilities (300K) as high as several hundred are typical[11] for MOCVD while somewhat lower values (< 100 cm^2/volt·sec) are reported for MBE grown films on Si[7]. It is clear that the substrate orientation producing the best nitride quality is the (111) growth surface where both cubic and hexagonal crystal structures are observed depending on growth conditions and the technique itself.

In our synthesis approach we use a single flow, single temperature OMVPE process to realize very high quality HEMT structures on both SiC, sapphire and Si. The materials produced with the Cornell growth technique have established several bench marks including for the lowest channel sheet resistance, the best PAE (78 % measured at 4 GHz by Lockheed Martin), and the lowest noise figure (1.5 dB at 10 GHz by HRL), on short channel devices sapphire-based devices. In addition, our SiC-based devices have set the records for the highest f_Ts (75 GHz on a 0.15 µm gate length) and static power dissipation (> 30 Watts/mm). On silicon, we are currently the only group to produce working HEMTs. A key aspect to the growth on silicon is the large thermal mismatch between the Si and GaN which places the GaN film in tension upon cooling from the growth. This mismatch is over twice as large as for the SiC/GaN case where layer cracking can be observed at thickness exceeding several microns. For growth on Si with our process and nucleation layer, we are limited to structures of 1 μm in thickness or less. Figure 4 illustrates the layer cracking which is seen in Nomarski micrographs (left image) when the nucleation layer is not optimized. After optimization of the nucleation layer, the surface quality is nearly featureless as shown in Figure 4 (right image). This surface quality is considerably better than the GaN grown on sapphire or SiC. If the growth was allowed to proceed another 2000 Å to a total thickness of 1.2 μm, all structures grown to date show the cracks over the entire substrate surface.

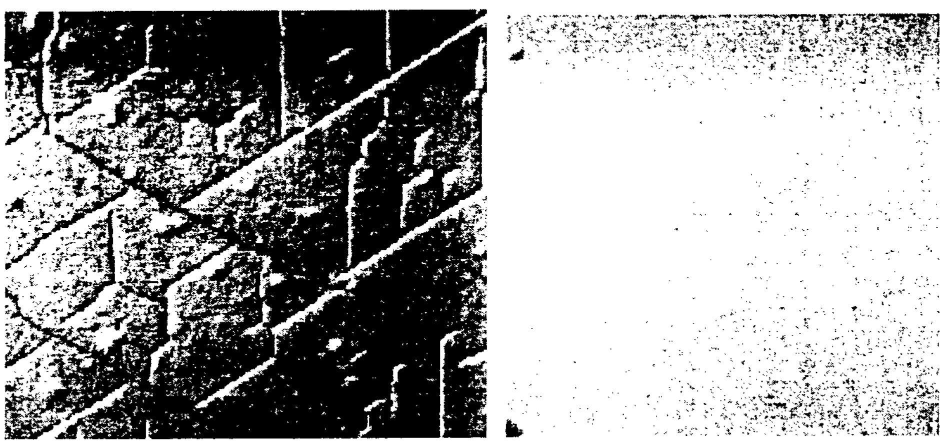


Figure 4. Nomarski phase contrast images (magnification 950) of 1 μm thick GaN films grown on (111) Si. The left image showing cracks was on an un-optimized nucleation layer.

For development of HEMT structures, we fix the total GaN buffer thickness to roughly 6000 Å prior to the growth of the undoped $Al_{0.35}Ga_{0.65}N$ barrier and supply layer. Examination of these structures with X-Ray diffraction indicates the presence of both cubic and hexagonal phases. We also observe only the hexagonal phase using low temperature (2 K) PL. As a result, we believe our process produces cubic GaN initially on the nucleation layer, and during the growth of the GaN buffer, the crystal phase changes to wurtzite (Ga face) prior to the deposition of the 300 Å thick AlGaN top layer. With a three layer model, we can explain the Hall data presented in Figure 5. At low sample currents we observe a mobility of 1500 cm^2/volt·sec and a sheet electron density consistent with our best materials on sapphire and SiC where the GaN is hexagonal. At modest sample currents the mobility increases to values exceeding 2500 cm^2/volt·sec which is believed to represent dominant conduction in underlying cubic GaN. Finally, as we continue to increase the Hall sample current, we observe a sharp decrease in Hall mobility and a corresponding increase in sheet electron density which represents some additional conduction in the 1 ohm-cm p-type Si substrate.

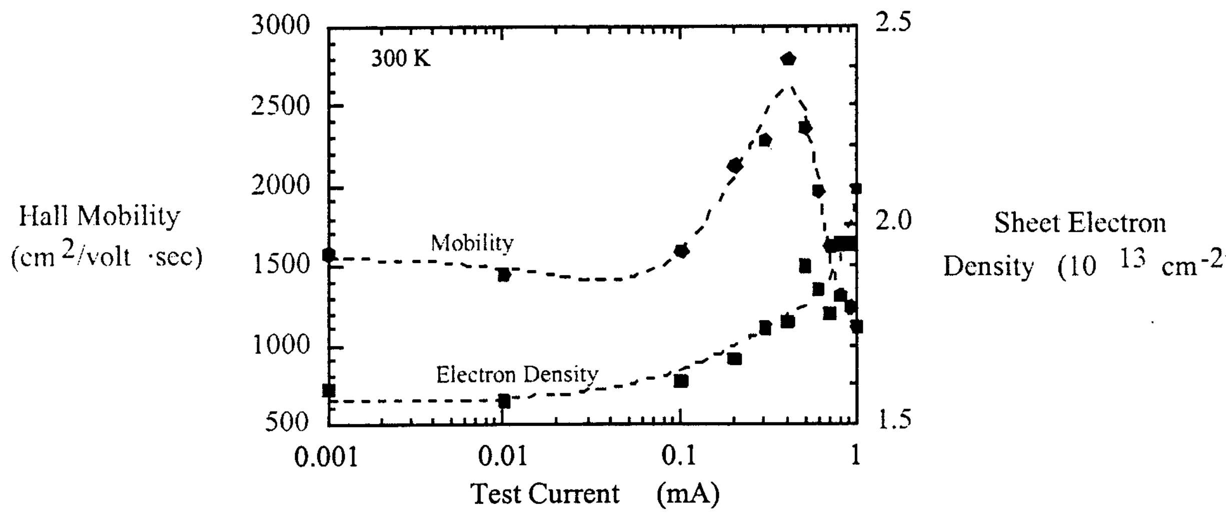


Figure 5. Room temperature Hall mobility plotted versus the Hall sample current for an AlGaN/GaN HEMT on (111) Si.

At first glance, these mobility data appear to be the highest numbers ever reported on GaN at 300 K. The data evaluated at test currents exceeding 0.1 mA were dominated by the underlying pn junction with the silicon substrate – these mobiltity numbers are not representative of the 2DEG in the GaN structure. Although these data were taken off our best Hall sample, we have "wafer mapped" with the Hall technique several other wafers and we consistently observe numbers exceeding 1200 cm^2/volt·sec for our structures on Si. Finally, its worth mentioning that 300 K PL linewidths of the GaN are less than 40 meV, far better than what appears in the literature.

With device quality structures on Si available, we proceeded to use a standard E-beam lithographic process to fabricate small periphery devices with sub-micron gate lengths. The process includes a 1000 Å etch to remove the top AlGaN for "mesa" isolation. Next, the ohmic metallization is defined, followed by a roughly 700 °C anneal, and finally, the mushroom gate metallization step. These devices have a cascade co-planar waveguide probe geometry to facilitate static and RF testing. As seen from the static IV testing presented in Figure 6, our nucleation layer is indeed insulating, which results good isolation between devices and the observed low output conductance. While there are a few reports on UV photo diodes fabricated on GaN on Si[12,13], these devices represent the first nitride transistor devices fabricated on silicon.

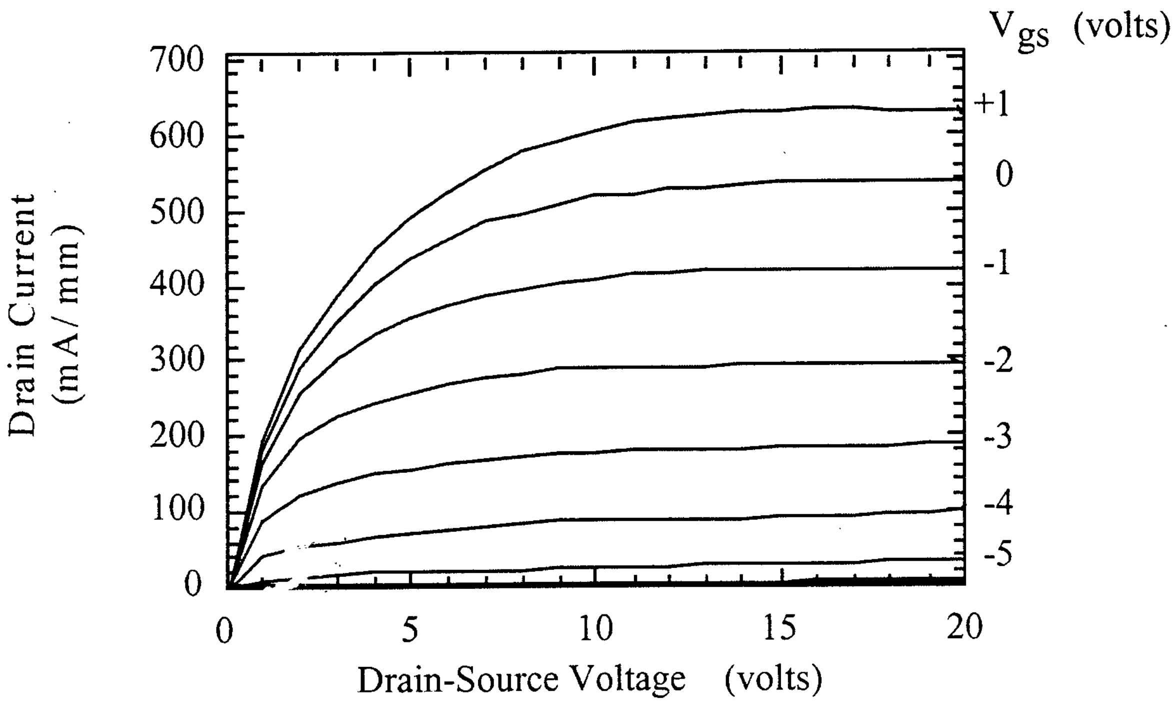


Figure 6. Static output characteristics of a 150 μm periphery, 0.3 μm gate length device on 1 ohm-cm p-type Si.

As is evident from this data, the full channel current is somewhat less than expected resulting in a peak transconductance of 130 mS/mm for this device. Also, the thermal droop of the output curves is negligible, in spite of the some 12 Watts/mm of thermal dissipation, providing direct evidence of the considerable thermal heat sinking through the Si substrate.

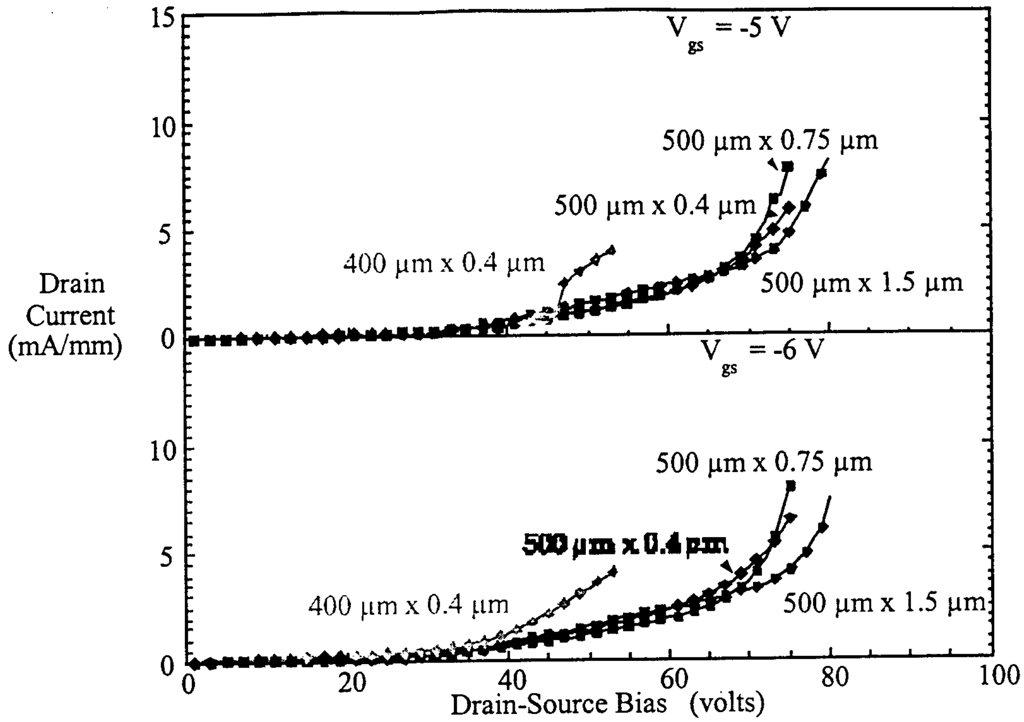


Figure 7. Pinch off characteristics of the GaN PI-HEMTs on Si of the indicated dimensions.

The pinch off characteristics up to 80 volts are shown in Figure 7. There is little evidence of conduction in the Si substrate until the drain-source bias exceeds 40 volts. In fact, these devices require drain-source biases voltages of up to 80 volts to produce significant substrate conduction (less than 10 mA/mm). This problem would clearly be lessened using high resistivity Si substrates (proposed work).

For all RF performance evaluations, a co-planar waveguide geometry, large enough to accommodate the cascaded probes of 150 µm pitch, was incorporated in all transistor designs. A significant RF parasitic is introduced when conduction occurs in the substrate. Although our nucleation layer provides static isolation, partially due to its small thickness, a capacitively coupled RF shunt is introduced by the underlying silicon. Measurements on the probe pads alone yield normalized capacitance values increased by more than twenty fold on 1 ohm-cm p-type Si compared to identical structures on sapphire. Accordingly, even with intrinsic performance advantages, the Si-based devices suffer as demonstrated by the small signal performance summary given in Figure 8.

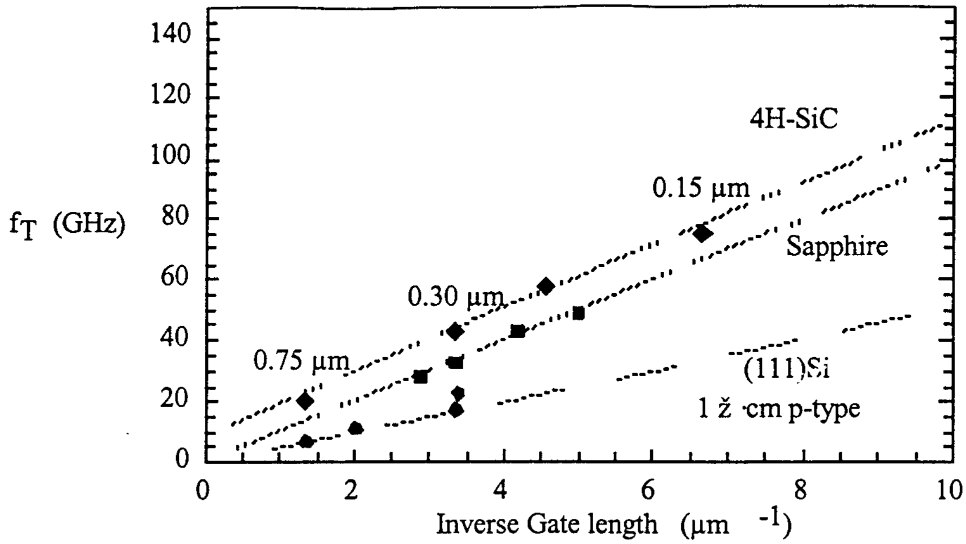


Figure 8. Unity current gain cut off frequency versus inverse gate length of GaN-based HEMTs on sapphire, SiC, and Si.

Here the current gain cut off frequency (f_T) is plotted versus inverse gate length for the substrates investigated: 1 ohm-cm p-type (111) Si, semi-insulating 4H-SiC (courtesy CREE), and sapphire. The SiC substrate produced the best combination of device/insulating substrate performance in these small signal tests. For 0.3 μm gate length devices, the f_T values on SiC are 45 GHz while the f_Ts on Si are 25 GHz. As for the large signal RF performance, several power sweeps at 4 GHz are shown in Figure 9 (courtesy Lockheed Martin) for the Si-based devices.

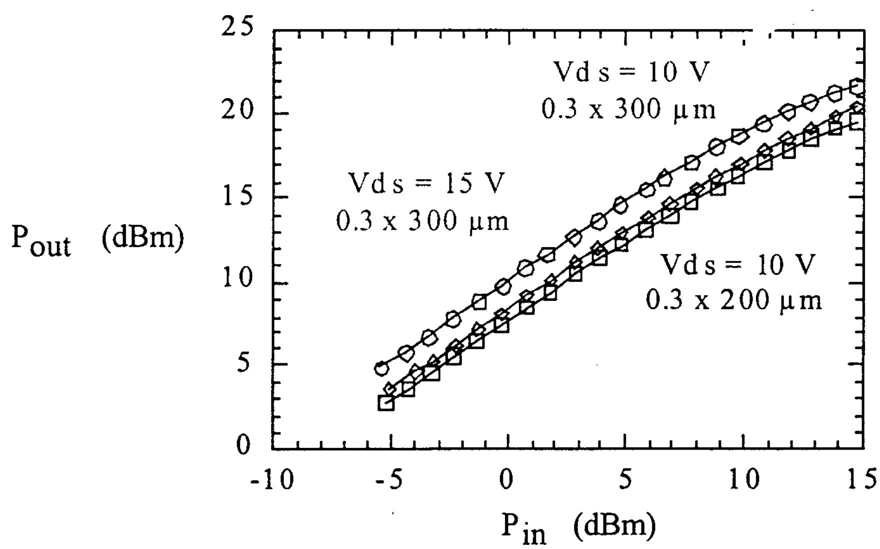


Figure 9. Large Signal RF performance of the GaN HEMT on 1 Ω-cm p-type Si.

. As shown, increasing the drain-source bias voltage does not increase the maximum RF power over the range of drive used. The best normalized power densities at 4 GHz were 0.5 Watts/mm at 10 % PAE. Good linearity is observed until a premature saturation is introduced by the RF shunt in the Si. In summary, the materials on Si clearly can produce identical or better intrinsic device performance, compared to sapphire and SiC, given their surface quality and high mobility. Both the small signal and large signal performance are limited by capacitively coupled substrate conduction. Overcoming this limitation is the focus of our future work in this application of GaN materials on silicon.

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