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**GEORGIA TECH GT-VNUC**  
**VLSI DESIGN VERIFICATION DOCUMENT**

VLSI DEVELOPMENT REPORT  
REPORT NO. VDR-0142-90-011  
JULY 5, 1991

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**GUIDANCE, NAVIGATION AND CONTROL**  
**DIGITAL EMULATION TECHNOLOGY LABORATORY**

Contract No. DASG60-89-C-0142  
Sponsored By  
The United States Army Strategic Defense Command

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**COMPUTER ENGINEERING RESEARCH LABORATORY**

Georgia Institute of Technology  
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# **GEORGIA TECH GT-VNUC VLSI DESIGN VERIFICATION DOCUMENT**

## **INTRODUCTION**

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems / Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech non-uniformity compensation chip, GT-VNUC.

**Table 1. Georgia Tech Chip Set for AHAT**

Design	DV Passed	Tape Delivered	Fabricated	Tested
GT-VFPU/1A	01/17/89	08/03/90	05/19/89	04/04/90
GT-VSNI	01/17/89	05/23/90	04/14/89	04/04/90
GT-VSM8	01/17/89	06/08/90	05/06/89	04/04/90
GT-VCTR	02/08/90	07/12/90	07/13/90	07/27/90
GT-VCLS	01/26/90	07/12/90	07/13/90	07/27/90
GT-VSF	09/12/89	07/19/90	07/13/90	07/27/90
GT-VTHR	12/11/90	02/15/91	03/01/91	03/08/91
GT-VDAG	02/22/91	02/25/91	05/01/91	
GT-VIAG	03/08/91	03/11/91	05/07/91	
GT-VTF				
GT-VNUC		07/05/91		

**Table 2. Georgia Tech Documents Sent for AHAT**

Document Item	Date Sent
Georgia Tech GT-VFPU VLSI Design Verification Document	05/15/90
Georgia Tech GT-VSNI VLSI Design Verification Document	05/23/90
Georgia Tech GT-VSM8 VLSI Design Verification Document	06/08/90
Georgia Tech GT-VCTR VLSI Design Verification Document	07/12/90
Georgia Tech GT-VCLS VLSI Design Verification Document	07/12/90
Georgia Tech GT-VSF VLSI Design Verification Document	07/19/90
Data Address Generation GT-VDAG Programming Model Document (v.2)	01/03/91
Instruction Address Generation GT-VIAG Programming Model Document (v.1)	01/03/91
GT-EP I/O Interface Specification Note	01/17/91
EP, SNI, SM8 Interconnection Note	01/28/91
Georgia Tech GT-VTHR VLSI Design Verification Document	02/15/91
Georgia Tech GT-VDAG VLSI Design Verification Document	02/25/91
Georgia Tech GT-VIAG VLSI Design Verification Document	03/11/91
GT-FPU: Operating Speed Test Document	04/16/91
Staggered Row Focal Plane Array Analysis Document	05/01/91
GT-EP Pascal Compiler Note, Source Code, and Program Examples	05/06/91
Instruction Address Generation GT-VIAG Programming Model Document (v.2)	06/07/91
Georgia Tech GT-VNUC VLSI Design Verification Document	07/05/91

<b>1. Design Verification Checklist .....</b>	<b>1</b>
<b>2. Functional Description .....</b>	<b>1</b>
2.1. Module state_mach .....	1
2.1. 1. Sub-module clock_sync .....	1
2.1. 2. Sub-module control .....	1
2.1. 3. Sub-module cal_out_gen .....	1
2.1. 4. Sub-module bad_pixel .....	2
2.1. 5. Sub-module subtract .....	2
2.1. 6. Sub-module glue .....	2
2.2. Module pre_div .....	2
2.2. 1. Sub-module reg_file .....	2
2.2. 2. Sub-module pix_cal_sub .....	2
2.2. 3. Sub-module int_sub .....	2
2.2. 4. Sub-module cal_out_sub .....	2
2.2. 5. Sub-module mult .....	3
2.3. Module divider .....	3
2.3. 1. Module divider1 .....	3
2.3. 2. Module divider2 .....	3
2.3. 3. Module overflow .....	3
2.4. Module pipe .....	3
2.4. 1. Sub-module buf_tree .....	3
2.4. 2. Sub-module shifter .....	3
2.4. 3. Sub-module cal_int_n .....	4
2.5. Module pixel_out .....	4
2.6. Module pix_counter .....	4
2.7. Module frame_sync .....	4
2.8. Module mem_host_if .....	4
2.8. 1. Sub-module mem_ctrl .....	4
2.8. 2. Sub-module mem_addr .....	4
2.8. 3. Sub-module mem_data .....	4
2.8. 4. Sub-module host_ctrl .....	5
2.8. 5. Sub-module host_data .....	5
2.8. 6. Sub-module strob .....	5
<b>3. Signal Descriptions .....</b>	<b>5</b>
<b>4. Final Notes .....</b>	<b>6</b>
<b>5. Block Diagrams and Schematics .....</b>	<b>6</b>
<b>6. Pin Description .....</b>	<b>6</b>
<b>7. Key Parameters .....</b>	<b>10</b>
<b>8. PADRING.033 .....</b>	<b>11</b>
<b>9. Power Dissipation .....</b>	<b>15</b>
<b>10. Timing Setup Files .....</b>	<b>18</b>
10.1. reg_room.040 .....	18

10.2. reg_worst.040 .....	18
<b>11. Timing Reports .....</b>	<b>19</b>
11.1. <Clk_in>, GUARANTEED, Max T, Min V .....	19
11.2. <Clk_in>, GUARANTEED, Room T, 5.0 V .....	27
11.3. <Clk_in>, TYPICAL, Max T, Min V .....	35
<b>Appendix A DV Checklist .....</b>	<b>43</b>
<b>Appendix B Block Diagrams And Schematics .....</b>	<b>59</b>

# GT-VNUC : Non-Uniformity Compensation

## 1. Design Verification Checklist

The DV checklist is attached in Appendix A.

## 2. Functional Description

The GT-VNUC (call NUC) compensates non-linear responses of a FPA by up to 4 linear segments. First the FPA is exposed to known intensity values (calibration intensities) and the responses from every pixel (calibration responses) are stored in external memories. After the calibration, the NUC reads responses of FPA pixels in scan order and performs the compensation by the following equation,

$$Pixel\_out = \frac{(fpa\_pixel - O_{cn})(I_{n+1} - I_n)}{O_{cn+1} - O_{cn}} + I_n \quad [1]$$

where *fpa\_pixel* is the FPA response,  $O_{cn}$  and  $O_{cn+1}$  are the calibration response of the current pixel which the *fpa\_pixel* falls between ( $O_{cn} < O_{cn+1}$ ).  $I_n$  and  $I_{n+1}$  are the calibration intensities corresponding to  $O_{cn}$  and  $O_{cn+1}$  respectively.

The following sections describe briefly the function of each module.

### 2.1. Module *state\_mach*

This module performs basically four functions: synchronizes the chip with respect to the pixel clock, performs a binary search to determine which linear segment the current pixel response lies on (ie. find  $O_{cn}$  and  $O_{cn+1}$ ), detects an invalid response during calibration and generates control signals for the rest of the chip to synchronize their operations with respect to the pixel clock.

#### 2.1.1. Sub-module *clock\_sync*

This module synchronizes the pixel clock to the 4X chip clock.

#### 2.1.2. Sub-module *control*

This PLA directs the binary search. For more information about how the binary search works, see the GT-VNUC Design Document.

#### 2.1.3. Sub-module *cal\_out\_gen*

This module contains various latches to hold pixel data and memory data. The flow of the data is controlled by the signals coming out from the sub-module *control*.

#### 2.1. 4. Sub-module *bad\_pixel*

While the chip is in the calibration mode, this module examines the incoming pixel data and checks if it is monotonically increasing as the calibration intensity increases. If not, the pixel is marked as 'bad pixel' by forcing the response of the highest calibration intensity to zero and storing zero to the corresponding memory location in the external RAMs. For information about a *bad\_pixel* detection algorithm, see the GT-VNUC Design Document or GT-VNUC User Guide.

#### 2.1. 5. Sub-module *subtract*

A comparator to check if the pixel data is larger than memory data. The result *gte* is one of the signals passed to the *control* to decide the direction of the binary search.

#### 2.1. 6. Sub-module *glue*

Some outputs from the *control* are delayed one or half cycle here and fed back to the *control*. Then this sub-module together with the *control* forms a state-machine. The output of the counter in the *clock\_sync* is decoded to generate *cycle0*, *cycle1*, *cycle2* and *cycle3*. They go all over the chip so that every module is synchronized to the pixel clock. A 3-bit up-counter is used to generate *bank[2:0]* during the calibration. The *bank[2:0]* is generated in the *control* during the compensation. This sub-module also collects various internal signals of the *state\_mach* and put them onto the external bus *stm\_out[15:0]* through a multiplexer to increase the observability of the *state\_mach*.

### 2.2. Module *pre\_div*

This module calculates a numerator and a denominator and gives them to the divider.

$$\text{numerator} = (\text{fpa\_pixel} - O_{cn}) * (I_{n+1} - I_n) \quad [2]$$

$$\text{denominator} = O_{cn+1} - O_{cn} \quad [3]$$

#### 2.2. 1. Sub-module *reg\_file*

This module consists of the five 16-bit registers and the control circuitry for this register file. The register file holds the calibration intensities and is accessed at *cycle2* by *int\_sub* to calculate *delta\_int* and at *cycle0* by a module *pipe* to perform the final addition in *pixel\_out*.

#### 2.2. 2. Sub-module *pix\_cal\_sub*

Calculate *pixel\_diff* = *fpa\_pixel* - *O<sub>cn</sub>*

#### 2.2. 3. Sub-module *int\_sub*

Calculate *delta\_int* = *I<sub>n+1</sub>* - *I<sub>n</sub>*

#### 2.2. 4. Sub-module *cal\_out\_sub*

Calculate *denominator* = *O<sub>cn+1</sub>* - *O<sub>cn</sub>*

### 2.2. 5. Sub-module *mult*

Calculate  $numerator = pix\_diff * delta\_int$

### 2.3. Module *divider*

The divider consists of three module: *divider1*, *divider2* and *overflow*. The divider performs the division of

$$q = \frac{numerator}{denominator} = \frac{(fpa\_pixel - O_{cn})(O_{cn+1} - O_{cn})}{(I_{cn+1} - I_{cn})} \quad [4]$$

The functionalities of each modules are described below.

#### 2.3. 1. Module *divider1*

This is the first half of the divider pipeline. The reason for the divider being spread into two is that the whole divider was too big to be logic compiled. But the size of the divider is crucial to the size of the whole chip and without logic compiling it, we could not achieve the acceptable chip size. If we spread the divider into two, then each of them could be logic compiled separately and the chip size became acceptable.

A random logic block *probe* consists of two 4-to-1 muxes which collect various internal signals of *divider1* and put them onto the external buses *divider1\_out* and *divider1\_out2*. These buses can be read by host at anytime through *mem\_host\_if*, hence increase the observability of *divider1*.

#### 2.3. 2. Module *divider2*

This is the second half of the divider pipeline.

#### 2.3. 3. Module *overflow*

This module detects an overflow of the division. Upon the occurrence of the overflow, it generates the signal, *div\_ovf*, to the module *pixel\_out* and the *pixel\_out* sets its output to the maximum intensity value, 0xffff.

### 2.4. Module *pipe*

This module delays *cal\_int\_n* until the result of the division is available. The output is sent to the *pixel\_out* to form the final result.

#### 2.4. 1. Sub-module *buf\_tree*

This module generates load signals for a sub-module *shifter*.

#### 2.4. 2. Sub-module *shifter*

This module consists of shift registers with the width of 3 and the length of 16. The index to the register file is stored here and shifted every pixel clock cycle. The output from the *shifter* is used to access the register file in *pre\_div/reg\_file* and the output of the register file is send to *cal\_int\_n*.

### 2.4.3. Sub-module *cal\_int\_n*

This datapath latches *cal\_int\_n[15:0]* from *pre\_div/reg\_file* at *cycle0* and output it at *cycle2* to synchronize with the *q[15:0]*.

### 2.5. Module *pixel\_out*

This module performs the final addition in [5] to form the compensated output of the FPA response.

$$Pixel\_out = q + I_n = \frac{(fpa\_pixel - O_{cn})(I_{n+1} - I_n)}{O_{cn+1} - O_{cn}} + I_n \quad [5]$$

In case of an overflow in the divider, the result is set to 0xffff. In case of a bad pixel response, the result is set to the previous value of the same row or zero if the pixel is the first element of the row.

### 2.6. Module *pix\_counter*

The chip sees the FPA as an one-dimensional linear array and this module keeps track of which pixel is currently supplying the input by using 20-bit up-counter. This module also flags data between *End\_row\_in* and *Begin\_row\_in* as dead pixel data.

### 2.7. Module *frame\_sync*

This module delays frame sync signals (*Beg\_frame\_in*, *Beg\_row\_in*, *End\_frame\_in* and *End\_row\_in*) until the compensated result (*Pixel\_out*) is available so that the NUC outputs *Pixel\_out* together with proper frame sync signals (*Beg\_frame\_out*, *Beg\_row\_out*, *End\_frame\_out* and *End\_row\_out*) to the next SP chip.

### 2.8. Module *mem\_host\_if*

This module handles interfaces to the external RAMs and to the host.

#### 2.8.1. Sub-module *mem\_ctrl*

This sub module generates an output enable signal for the external RAMs. During the calibration mode, the chip writes to the external RAMs at *cycle2*. Thus the output is disabled during the cycle. During the compensation mode, the outputs from the external RAMs are always enabled.

#### 2.8.2. Sub-module *mem\_addr*

This sub module generates a memory address (*Mem\_addr*) and chip select signals (*Cs32k* and *Cs16k*) for the external RAMs. It contains various decoding circuitries to generate those signals.

#### 2.8.3. Sub-module *mem\_data*

This sub module supplies the data to the external RAMs during calibration. Normally the data is coming out from the bad pixel detection circuitry (*state\_mach/bad\_pixel*), but the host can also write data

directly to the RAMs. When *host\_mem\_wr\_en* in *control\_word* is set to 1, the host has the direct control of *Mem\_data[15:0]*.

#### 2.8. 4. Sub-module *host\_ctrl*

This sub module handles a handshaking between the chip and the host. When a device select signal from the host (*Dev\_sel[3:0]*) matches with *Chip\_id[3:0]* which are hard wired, the NUC pull the *Dr* low to tell the host that the NUC is ready for accepting a request from the host. Now the host can write/read to the internal registers of the chip. This module also contains the *control\_word* register which have to be configured by the host prior to the regular operations.

#### 2.8. 5. Sub-module *host\_data*

All the data from/to the host go through this sub module. Data from the host is latched here at phase A and data to the host is muxed here. *Host\_addr[4:0]* selects which data to be read by the host or which register to be written by the host.

#### 2.8. 6. Sub-module *strob*

This module generates a write pulse to the external RAMs.

### 3. Signal Descriptions

Table 3.1 Pin Summary Table

Pin Name	Function	Active State	Type	Timing
<i>Clk_in</i>	Chip Clock		Input	Clk
<i>Pixel_clk_in</i>	SP clock, 4X		Input	Prop
<i>Fpa_pixel[15:0]</i>	Input from FPA	Data	Input	$V_B$
<i>Beg_frame_in</i>	Precede start of input frame	High	Input	$V_B$
<i>Beg_row_in</i>	Precede start of input row	High	Input	$V_B$
<i>End_row_in</i>	Precede end of input row	High	Input	$V_B$
<i>End_frame_in</i>	Precede end of input frame	High	Input	$V_B$
<i>N_reset</i>	Chip reset	Low	Input	$V_B$
<i>Chip_id[3:0]</i>	Chip identification bits	Data	Input	$V_A$
<i>Dev_sel[3:0]</i>	Device select	Data	Input	$V_A, V_B$
<i>Ode</i>	Output data enable	Low	Input	$V_A, V_B$
<i>Host_addr[4:0]</i>	Host address	Data	Input	$V_A, V_B$
<i>Host_data[15:0]</i>	Host data	Data	Input-Output	$V_A, V_B$
<i>Dr</i>	Device ready	High	Output	$V_A, V_B$
<i>Mem_data[15:0]</i>	Memory data	Data	Input-Output	$V_B$
<i>Mem_addr[22:0]</i>	Memory address	Data	Output	$S_A$
<i>N_mem_we</i>	Memory write enable	Low	Output	$V_B$
<i>N_mem_oe</i>	Memory output enable	Low	Output	$V_B$

<i>Pixel_out</i> [15:0]	Compensated <i>Fpa_pixel</i>	Data	Output	S <sub>B</sub>
<i>Beg_frame_out</i>	Precede start of output frame	High	Output	S <sub>B</sub>
<i>Beg_row_out</i>	Precede start of output row	High	Output	S <sub>B</sub>
<i>End_row_out</i>	Precede end of output row	High	Output	S <sub>B</sub>
<i>End_frame_out</i>	Precede end of output frame	High	Output	S <sub>B</sub>
<i>Pixel_clk_out</i>	Synchronized <i>Pixel_clk_in</i>		Output	S <sub>B</sub>
<i>Cs32k</i> [2:0]	Chip select for external rams	Low	Output	S <sub>A</sub>
<i>Cs16k</i> [4:0]	Chip select for external rams	Low	Output	S <sub>A</sub>

## 4. Final Notes

The compile build all in DV preparation was done in 2 passes. First 'COMPILE FORCE BUILD\_ALL' was issued but the command failed at 'COMPILE LAYOUT: /divider1' due to some internal faults of genesis. Then 'COMPILE BUILD\_ALL' was issued to pick up the rest of the commands including the 'COMPILE LAYOUT: /divider1'. This time all the commands were executed successfully.

To restore the database of the GT\_VNUC from the DV tape, first read the compressed database by  
 tar xvf /dev/rst8

This creates a file called 'nuc.tar.Z'. Then uncompress it by  
 zcat nuc.tar.Z | tar xvpBf -

## 5. Block Diagrams and Schematics

All the diagrams and schematics are attached in Appendix B.

## 6. Pin Description

Pin#	Loc.	Signal Name	Abbrev. Name	Pad Type	Strength	Timing
1	B1					
2	C1	corner_vss	cmr_vss	VSS CORNER		
3	D1	Host_data[1]	Hdata_1	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
4	E1	Host_data[2]	Hdata_2	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
5	F1	Host_data[3]	Hdata_3	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
6	G1	Host_data[4]	Hdata_4	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
7	H1	Host_data[5]	Hdata_5	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
8	C2	Host_data[6]	Hdata_6	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
9	D2	Host_data[7]	Hdata_7	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
10	E2	Host_data[8]	Hdata_8	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
11	F2	Host_data[9]	Hdata_9	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
12	G2	Host_data[10]	Hdata_10	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
13	H2	Host_data[11]	Hdata_11	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
14	D3	Ring_vss[0]	Rvss_0	RING VSS		
15	E3	Ring_vdd[0]	Rvdd_0	RING VDD		
16	F3	Host_data[12]	Hdata_12	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>

18	H3	Host_data[14]	Hdata_14	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
19	E4	Host_data[15]	Hdata_15	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A,B</sub>
20	F4	Beg_frame_in	Beg_f_in	DATA IN	NORMAL	V <sub>B</sub>
21	G4	Beg_row_in	Beg_r_in	DATA IN	NORMAL	V <sub>B</sub>
22	H4	End_row_in	End_r_in	DATA IN	NORMAL	V <sub>B</sub>
23	H5	End_frame_in	End_f_in	DATA IN	NORMAL	V <sub>B</sub>
24	J4	Pixel_clk_in	Pclk_in	DATA IN	NORMAL	PROP
25	K4	core_vdd	core_vdd	CORE VDD		
26	L4	Fpa_pixel[0]	Fpain_0	DATA IN	NORMAL	V <sub>B</sub>
27	M4	Fpa_pixel[1]	Fpain_1	DATA IN	NORMAL	V <sub>B</sub>
28	J3	Fpa_pixel[2]	Fpain_2	DATA IN	NORMAL	V <sub>B</sub>
29	K3	Fpa_pixel[3]	Fpain_3	DATA IN	NORMAL	V <sub>B</sub>
30	L3	Fpa_pixel[4]	Fpain_4	DATA IN	NORMAL	V <sub>B</sub>
31	M3	Fpa_pixel[5]	Fpain_5	DATA IN	NORMAL	V <sub>B</sub>
32	N3	Fpa_pixel[6]	Fpain_6	DATA IN	NORMAL	V <sub>B</sub>
33	J2	Fpa_pixel[8]	Fpain_8	DATA IN	NORMAL	V <sub>B</sub>
34	K2	Fpa_pixel[7]	Fpain_7	DATA IN	NORMAL	V <sub>B</sub>
35	L2	Ring_vdd[1]	Rvdd_1	RING VDD		
36	M2	Ring_vss[1]	Rvss_1	RING VSS		
37	N2	Fpa_pixel[10]	Fpain_10	DATA IN	NORMAL	V <sub>B</sub>
38	P2	Fpa_pixel[9]	Fpain_9	DATA IN	NORMAL	V <sub>B</sub>
39	J1					
40	K1	Fpa_pixel[11]	Fpain_11	DATA IN	NORMAL	V <sub>B</sub>
41	L1					
42	M1					
43	N1					
44	P1					
45	Q1					
46	M5					
47	M6					
48	M7	corner_vdd[0]	cmr_vdd	CORNER VDD		
49	Q2					
50	Q3	Fpa_pixel[12]	Fpain_12	DATA IN	NORMAL	V <sub>B</sub>
51	Q4	Fpa_pixel[13]	Fpain_13	DATA IN	NORMAL	V <sub>B</sub>
52	Q5	Fpa_pixel[14]	Fpain_14	DATA IN	NORMAL	V <sub>B</sub>
53	Q6	Fpa_pixel[15]	Fpain_15	DATA IN	NORMAL	V <sub>B</sub>
54	Q7	Mem_data[0]	Mdata_0	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
55	P3	Mem_data[1]	Mdata_1	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
56	P4	Mem_data[2]	Mdata_2	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
57	P5	Mem_data[3]	Mdata_3	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
58	P6	Mem_data[4]	Mdata_4	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
59	P7	Mem_data[5]	Mdata_5	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
60	N4	Mem_data[6]	Mdata_6	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
61	N5	Mem_data[7]	Mdata_7	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
62	N6	Mem_data[8]	Mdata_8	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
63	N7	Mem_data[9]	Mdata_9	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
64	M8	Mem_data[10]	Mdata_10	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
65	M9	Mem_data[11]	Mdata_11	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>
66	M10	Ring_vss[2]	Rvss_2	RING VSS		
67	M11	Ring_vdd[2]	Rvdd_2	RING VSS		
68	L8	Mem_data[12]	Mdata_12	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>

69	M12						
70	N8	Mem_data[13]	Mdata_13	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>	
71	N9	Mem_data[14]	Mdata_14	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>	
72	N10	Mem_data[15]	Mdata_15	DATA IO	NORM/DRV2	V <sub>B</sub> /S <sub>A</sub>	
73	N11	N_we	N_we	DATA OUT	DRVSPEED2	V <sub>B</sub>	
74	N12	N_oe	N_oe	DATA OUT	DRVSPEED2	S <sub>A</sub>	
75	N13	Mem_addr[0]	Maddr_0	DATA OUT	DRVSPEED3	S <sub>A</sub>	
76	P8	Mem_addr[1]	Maddr_1	DATA OUT	DRVSPEED3	S <sub>A</sub>	
77	P9	Ring_vss[3]	Rvss_3	RING VSS			
78	P10	Mem_addr[2]	Maddr_2	DATA OUT	DRVSPEED3	S <sub>A</sub>	
79	P11	Mem_addr[3]	Maddr_3	DATA OUT	DRVSPEED3	S <sub>A</sub>	
80	P12	Ring_vdd[3]	Rvdd_3	RING VDD			
81	P13	Mem_addr[5]	Maddr_5	DATA OUT	DRVSPEED3	S <sub>A</sub>	
82	P14	Mem_addr[4]	Maddr_4	DATA OUT	DRVSPEED3	S <sub>A</sub>	
83	Q8	Mem_addr[7]	Maddr_7	DATA OUT	DRVSPEED3	S <sub>A</sub>	
84	Q9	Mem_addr[6]	Maddr_6	DATA OUT	DRVSPEED3	S <sub>A</sub>	
85	Q10	Ring_vss[4]	Rvss_4	RING VSS			
86	Q11	Mem_addr[8]	Maddr_8	DATA OUT	DRVSPEED3	S <sub>A</sub>	
87	Q12						
88	Q13	Ring_vdd[4]	Rvdd_4	RING VSS			
89	Q14						
90	Q15						
91	P15						
92	N15						
93	M15						
94	L15	Mem_addr[10]	Maddr_10	DATA OUT	DRVSPEED3	S <sub>A</sub>	
95	K15	Mem_addr[9]	Maddr_9	DATA OUT	DRVSPEED3	S <sub>A</sub>	
96	J15	Mem_addr[12]	Maddr_12	DATA OUT	DRVSPEED3	S <sub>A</sub>	
97	H15	Mem_addr[11]	Maddr_11	DATA OUT	DRVSPEED3	S <sub>A</sub>	
98	N14	Mem_addr[14]	Maddr_14	DATA OUT	DRVSPEED3	S <sub>A</sub>	
99	M14	Mem_addr[13]	Maddr_13	DATA OUT	DRVSPEED3	S <sub>A</sub>	
100	L14	Ring_vdd[5]	Rvdd_5	RING VDD			
101	K14	Ring_vss[5]	Rvss_5	RING VSS			
102	J14	Mem_addr[16]	Maddr_16	DATA OUT	DRVSPEED3	S <sub>A</sub>	
103	H14	Mem_addr[15]	Maddr_15	DATA OUT	DRVSPEED3	S <sub>A</sub>	
104	M13	Mem_addr[18]	Maddr_18	DATA OUT	DRVSPEED3	S <sub>A</sub>	
105	L13	Mem_addr[17]	Maddr_17	DATA OUT	DRVSPEED3	S <sub>A</sub>	
106	K13	Mem_addr[19]	Maddr_19	DATA OUT	DRVSPEED3	S <sub>A</sub>	
107	J13	Mem_addr[20]	Maddr_20	DATA OUT	DRVSPEED3	S <sub>A</sub>	
108	H13	Ring_vss[6]	Rvss_6	RING VSS			
109	L12	Ring_vdd[6]	Rvdd_6	RING VDD			
110	K12	Mem_addr[21]	Maddr_21	DATA OUT	DRVSPEED3	S <sub>A</sub>	
111	J12	Mem_addr[22]	Maddr_22	DATA OUT	DRVSPEED3	S <sub>A</sub>	
112	H12	core_vss	core_vss	CORE VSS			
113	H11	Cs16k[0]	Cs16k_0	DATA OUT	DRVSPEED3	S <sub>A</sub>	
114	G12	Cs16k[1]	Cs16k_1	DATA OUT	DRVSPEED3	S <sub>A</sub>	
115	F12	Cs16k[2]	Cs16k_2	DATA OUT	DRVSPEED3	S <sub>A</sub>	
116	E12	Cs16k[3]	Cs16k_3	DATA OUT	DRVSPEED3	S <sub>A</sub>	
117	D12	Ring_vss[7]	Rvss_7	RING VSS			
118	G13	Ring_vdd[7]	Rvdd_7	RING VDD			
119	F13	Cs16k[4]	Cs16k_4	DATA OUT	DRVSPEED3	S <sub>A</sub>	

120	E13	Cs32k[0]	Cs32k_0	DATA OUT	DRVSPEED3	S <sub>A</sub>
121	D13	Cs32k[1]	Cs32k_1	DATA OUT	DRVSPEED3	S <sub>A</sub>
122	C13	Cs32k[2]	Cs32k_2	DATA OUT	DRVSPEED3	S <sub>A</sub>
123	G14	N_reset	N_reset	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
124	F14	Pixel_out[0]	Pout_0	DATA OUT	DRVSPEED2	S <sub>B</sub>
125	E14	Ring_vdd[10]	Rvdd_10	RING VDD		
126	D14	Ring_vss[10]	Rvss_10	RING VSS		
127	C14	Chip_id[0]	Chip_id0	DATA IN	NORMAL	V <sub>A</sub>
128	B14	Chip_id[1]	Chip_id1	DATA IN	NORMAL	V <sub>A</sub>
129	G15	Chip_id[2]	Chip_id2	DATA IN	NORMAL	V <sub>A</sub>
130	F15	Chip_id[3]	Chip_id3	DATA IN	NORMAL	V <sub>A</sub>
131	E15					
132	D15					
133	C15					
134	B15					
135	A15					
136	D11	corner_vdd[1]	cmr_vdd	CORNER VDD		
137	D10					
138	D9	Pixel_out[1]	Pout_1	DATA OUT	DRVSPEED2	S <sub>B</sub>
139	A14					
140	A13	Pixel_out[3]	Pout_3	DATA OUT	DRVSPEED2	S <sub>B</sub>
141	A12	Pixel_out[2]	Pout_2	DATA OUT	DRVSPEED2	S <sub>B</sub>
142	A11	Pixel_out[5]	Pout_5	DATA OUT	DRVSPEED2	S <sub>B</sub>
143	A10	Pixel_out[4]	Pout_4	DATA OUT	DRVSPEED2	S <sub>B</sub>
144	A9	Pixel_out[6]	Pout_6	DATA OUT	DRVSPEED2	S <sub>B</sub>
145	B13	Pixel_out[7]	Pout_7	DATA OUT	DRVSPEED2	S <sub>B</sub>
146	B12	Pixel_out[8]	Pout_8	DATA OUT	DRVSPEED2	S <sub>B</sub>
147	B11	Pixel_out[9]	Pout_9	DATA OUT	DRVSPEED2	S <sub>B</sub>
148	B10	Pixel_out[10]	Pout_10	DATA OUT	DRVSPEED2	S <sub>B</sub>
149	B9	Ring_vss[9]	Rvss_9	RING VSS		
150	C12	Ring_vdd[9]	Rvdd_9	RING VDD		
151	C11	Pixel_out[11]	Pout_11	DATA OUT	DRVSPEED2	S <sub>B</sub>
152	C10	Pixel_out[12]	Pout_12	DATA OUT	DRVSPEED2	S <sub>B</sub>
153	C9	Pixel_out[13]	Pout_13	DATA OUT	DRVSPEED2	S <sub>B</sub>
154	D8	Pixel_out[14]	Pout_14	DATA OUT	DRVSPEED2	S <sub>B</sub>
155	D7	Pixel_out[15]	Pout_15	DATA OUT	DRVSPEED2	S <sub>B</sub>
156	D6	clk_pad_vcc	clk_vdd	CLK VDD		
157	D5	clk_pad_vss	clk_vss	CLK VSS		
158	E8	clk_pad_clk	clk	CLK		
159	D4					
160	C8	Pixel_clk_out	Pclk_out	DATA OUT	DRVSPEED2	S <sub>B</sub>
161	C7	Beg_frame_out	B_f_out	DATA OUT	DRVSPEED2	S <sub>B</sub>
162	C6	Beg_row_out	B_r_out	DATA OUT	DRVSPEED2	S <sub>B</sub>
163	C5	End_row_out	E_r_out	DATA OUT	DRVSPEED2	S <sub>B</sub>
164	C4	End_frame_out	E_f_out	DATA OUT	DRVSPEED2	S <sub>B</sub>
165	C3	Dev_sel[0]	Dev_sel0	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
166	B8	Dev_sel[1]	Dev_sel1	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
167	B7	Dev_sel[2]	Dev_sel2	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
168	B6	Dev_sel[3]	Dev_sel3	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
169	B5	Host_addr[4]	Haddr_4	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
170	B4	Host_addr[3]	Haddr_3	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>

171	B3	Host_addr[2]	Haddr_2	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
172	B2	Host_addr[1]	Haddr_1	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
173	A8	Ring_vss[8]	Rvss_8	RING VSS		
174	A7	Ring_vdd[8]	Rvdd_8	RING VDD		
175	A6	Host_addr[0]	Haddr_0	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
176	A5	Dr	Dr	DATA IN	DRVSPEED2	S <sub>A</sub> ,S <sub>B</sub>
177	A4	Ode	Ode	DATA IN	NORMAL	V <sub>A</sub> ,V <sub>B</sub>
178	A3	Host_data[0]	Hdata_0	DATA IO	NORM/DRV2	V <sub>A</sub> /S <sub>A</sub> ,B
179	A2					
180	A1					

## 7. Key Parameters

```

)
) Key Parameters for Chip /mntb/nuc/nuc/gt_nuc/nuc
) =====
)
) TIME = Thu May 30 14:51:39 1991
)
) ROUTE_VERSION = 8.00
) HEIGHT = 399.2 MILS
)   ( = 10139.6 u )
) WIDTH = 403.2 MILS
)   ( = 10241.2 u )
) ROUTED = 1 (0=NO,1=YES)
) TOTAL_WIRE_LENGTH = 1324581 MILS
)   ( = 33644357. u )
) CORE_AREA = 125560.2 SQUARE_MILS
)   ( = 81006422.1 u2 )
) PADRING_AREA = 35382.1 SQUARE_MILS
)   ( = 22827117. u2 )
) PAD_AREA = 27829.2 SQUARE_MILS
)   ( = 17954286. u2 )
) ROUTE_AREA = 62035.6 SQUARE_MILS
)   ( = 40022889. u2 )
) PERCENT_ROUTING_OF_CORE = 49 %
) PERCENT_ROUTING_OF_CHIP = 38 %
) PERCENT_CORE_OF_CHIP = 78 %
) PERCENT_PADRING_OF_CHIP = 21 %
) PERCENT_PAD_OF_PADRING = 78 %
)
) NETLIST_VERSION = 2.0
) NETLIST_EXISTS = 1 (0=NO,1=YES)
)
) PHASE_A_TIME = 35.4 NANoseconds
) PHASE_B_TIME = 36.2 NANoseconds
) SYMMETRIC_TIME = 74.2 NANoseconds
)
)
) ROUTE_ESTIMATE_LVL = 0
) FLAT_ROUTE = 0 (0=NO,1=YES)
) TECHNOLOGY_NAME = CMOS-1
) PACKAGE_SPECIFIED = 1 (0=NO,1=YES)
) PACKAGE_NAME = CPGA180f
) FABLINE_NAME = HP2_CN10B
) COMPILER_TYPE = GCX
)
) FLOORPLAN_VERSION = 8.0

```

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) BOND_PAD_CNT = 153
) HEIGHT_ESTIMATE = 433.52 MILS
)   ( = 11011.40 u )
) WIDTH_ESTIMATE = 440.53 MILS
)   ( = 11189.46 u )
) FUSED = 1 (0=NO,1=YES)
) FUSION_REQUIRED = 1 (0=NO,1=YES)
) PINOUT = 1 (0=NO,1=YES)
) PINOUT_REQUIRED = 1 (0=NO,1=YES)
) PLACED = 1 (0=NO,1=YES)
) PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
)
)
) DOWN_BONDS_ALLOWED = 1 (0=NO,1=YES)
) PKG_PIN_COUNT = 180
) PKG_WELL_HEIGHT = 472.00 MILS
)   ( = 11988.80 u )
) PKG_WELL_WIDTH = 472.00 MILS
)   ( = 11988.80 u )
) AREA = 160957.4 SQUARE_MILS
)   ( = 103843282. u2 )
) OBJECT_TYPE = Chip
) PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
) CHECKPOINTS_EXIST = 0 (0=NO,1=YES)
) CAN_SET_FABLINE = 1 (0=NO,1=YES)
)
) Key Parameter Listing Complete

```

## 8. PADRING.033

### OUTPUT RINGS REPORT Version 1

Noise contribution:(ma/nh) Speed0: 2.50 Speed1: 5.00 Speed2: 8.33 Speed3: 16.66  
Limits: Maximum noise level: 100. Unacceptable level: 150

Combined power pads do not supply clean power to the core.  
Their use is discouraged

Ring under analysis: VDD

PAD NAME	EDGE	SPEED	DRIVE	PAD	COMMENT
			TYPE	SUPPLY	
Pixel_out[15]	SOUTH	2	CMOS	1	OK
Pixel_out[14]	SOUTH	2	CMOS	1	OK
Pixel_out[13]	SOUTH	2	CMOS	1	OK
Pixel_out[12]	SOUTH	2	CMOS	1	OK
Pixel_out[11]	SOUTH	2	CMOS	1	OK
Ring_vdd[9]	SOUTH		POWER		
Pixel_out[10]	SOUTH	2	CMOS	1	OK
Pixel_out[9]	SOUTH	2	CMOS	1	OK
Pixel_out[8]	SOUTH	2	CMOS	1	OK
Pixel_out[7]	SOUTH	2	CMOS	1	OK
Pixel_out[6]	SOUTH	2	CMOS	1	OK
Pixel_out[5]	SOUTH	2	CMOS	3	OK
Pixel_out[4]	SOUTH	2	CMOS	3	OK
Pixel_out[3]	SOUTH	2	CMOS	2	OK
Pixel_out[2]	SOUTH	2	CMOS	2	OK
Pixel_out[1]	SOUTH	2	CMOS	2	OK
corner_vdd[1]	SOUTH		POWER		

Ring_vdd[10]	WEST		POWER		
Pixel_out[0]	WEST	2	CMOS	2	OK
Cs32k[2]	WEST	3	CMOS	2	OK
Cs32k[1]	WEST	3	CMOS	3	OK
Cs32k[0]	WEST	3	CMOS	3	OK
Cs16k[4]	WEST	3	CMOS	1	OK
Ring_vdd[7]	WEST		POWER		
Cs16k[3]	WEST	3	CMOS	1	OK
Cs16k[2]	WEST	3	CMOS	1	OK
Cs16k[1]	WEST	3	CMOS	1	OK
Cs16k[0]	WEST	3	CMOS	1	OK
Mem_addr[22]	WEST	3	CMOS	1	OK
Mem_addr[21]	WEST	3	CMOS	1	OK
Ring_vdd[6]	WEST		POWER		
Mem_addr[20]	WEST	3	CMOS	1	OK
Mem_addr[19]	WEST	3	CMOS	1	OK
Mem_addr[18]	WEST	3	CMOS	1	OK
Mem_addr[17]	WEST	3	CMOS	1	OK
Mem_addr[16]	WEST	3	CMOS	1	OK
Mem_addr[15]	WEST	3	CMOS	1	OK
Ring_vdd[5]	WEST		POWER		
Mem_addr[14]	WEST	3	CMOS	1	OK
Mem_addr[13]	WEST	3	CMOS	1	OK
Mem_addr[12]	WEST	3	CMOS	1	OK
Mem_addr[11]	WEST	3	CMOS	1	OK
Mem_addr[10]	WEST	3	CMOS	1	OK
Mem_addr[9]	WEST	3	CMOS	1	OK
Ring_vdd[4]	NORTH		POWER		
Mem_addr[8]	NORTH	3	CMOS	1	OK
Mem_addr[7]	NORTH	3	CMOS	1	OK
Mem_addr[6]	NORTH	3	CMOS	1	OK
Mem_addr[5]	NORTH	3	CMOS	1	OK
Mem_addr[4]	NORTH	3	CMOS	1	OK
Mem_addr[3]	NORTH	3	CMOS	1	OK
Ring_vdd[3]	NORTH		POWER		
Mem_addr[2]	NORTH	3	CMOS	1	OK
Mem_addr[1]	NORTH	3	CMOS	1	OK
Mem_addr[0]	NORTH	3	CMOS	1	OK
N_oe	NORTH	2	CMOS	1	OK
N_we	NORTH	2	CMOS	1	OK
Mem_data[15]	NORTH	2	CMOS	1	OK
Mem_data[14]	NORTH	2	CMOS	1	OK
Mem_data[13]	NORTH	2	CMOS	1	OK
Mem_data[12]	NORTH	2	CMOS	1	OK
Ring_vdd[2]	NORTH		POWER		
Mem_data[11]	NORTH	2	CMOS	1	OK
Mem_data[10]	NORTH	2	CMOS	1	OK
Mem_data[9]	NORTH	2	CMOS	1	OK
Mem_data[8]	NORTH	2	CMOS	1	OK
Mem_data[7]	NORTH	2	CMOS	1	OK
Mem_data[6]	NORTH	2	CMOS	1	OK
Mem_data[5]	NORTH	2	CMOS	2	OK
Mem_data[4]	NORTH	2	CMOS	2	OK
Mem_data[3]	NORTH	2	CMOS	2	OK
Mem_data[2]	NORTH	2	CMOS	2	OK
Mem_data[1]	NORTH	2	CMOS	3	OK
Mem_data[0]	NORTH	2	CMOS	3	OK
corner_vdd[0]	NORTH		POWER		
Ring_vdd[1]	EAST		POWER		
Host_data[15]	EAST	2	CMOS	3	OK

Host_data[14]	EAST	2	CMOS	3	OK
Host_data[13]	EAST	2	CMOS	3	OK
Host_data[12]	EAST	2	CMOS	3	OK
Ring_vdd[0]	EAST		POWER		
Host_data[11]	EAST	2	CMOS	3	OK
Host_data[10]	EAST	2	CMOS	3	OK
Host_data[9]	EAST	2	CMOS	1	OK
Host_data[8]	EAST	2	CMOS	1	OK
Host_data[7]	EAST	2	CMOS	1	OK
Host_data[6]	EAST	2	CMOS	1	OK
Host_data[5]	EAST	2	CMOS	1	OK
Host_data[4]	EAST	2	CMOS	1	OK
Host_data[3]	EAST	2	CMOS	1	OK
Host_data[2]	EAST	2	CMOS	1	OK
Host_data[1]	EAST	2	CMOS	1	OK
Host_data[0]	SOUTH	2	CMOS	1	OK
Dr	SOUTH	2	CMOS	1	OK
Ring_vdd[8]	SOUTH		POWER		
End_frame_out	SOUTH	2	CMOS	1	OK
End_row_out	SOUTH	2	CMOS	1	OK
Beg_row_out	SOUTH	2	CMOS	1	OK
Beg_frame_out	SOUTH	2	CMOS	1	OK
Pixel_clk_out	SOUTH	2	CMOS	1	OK

This ring has 3 more VDD pads than it needs  
 Ring under analysis: VSS

PAD NAME	EDGE	SPEED	DRIVE	PAD TYPE	PAD SUPPLY	COMMENT
Pixel_out[15]	SOUTH	2	CMOS	1	OK	
Pixel_out[14]	SOUTH	2	CMOS	1	OK	
Pixel_out[13]	SOUTH	2	CMOS	1	OK	
Pixel_out[12]	SOUTH	2	CMOS	1	OK	
Pixel_out[11]	SOUTH	2	CMOS	1	OK	
Ring_vss[9]	SOUTH		POWER			
Pixel_out[10]	SOUTH	2	CMOS	1	OK	
Pixel_out[9]	SOUTH	2	CMOS	1	OK	
Pixel_out[8]	SOUTH	2	CMOS	1	OK	
Pixel_out[7]	SOUTH	2	CMOS	1	OK	
Pixel_out[6]	SOUTH	2	CMOS	1	OK	
Pixel_out[5]	SOUTH	2	CMOS	2	OK	
Pixel_out[4]	SOUTH	2	CMOS	2	OK	
Pixel_out[3]	SOUTH	2	CMOS	1	OK	
Pixel_out[2]	SOUTH	2	CMOS	1	OK	
Pixel_out[1]	SOUTH	2	CMOS	1	OK	
Ring_vss[10]	WEST		POWER			
Pixel_out[0]	WEST	2	CMOS	1	OK	
Cs32k[2]	WEST	3	CMOS	1	OK	
Cs32k[1]	WEST	3	CMOS	2	OK	
Cs32k[0]	WEST	3	CMOS	2	OK	
Cs16k[4]	WEST	3	CMOS	1	OK	
Ring_vss[7]	WEST		POWER			
Cs16k[3]	WEST	3	CMOS	1	OK	
Cs16k[2]	WEST	3	CMOS	1	OK	
Cs16k[1]	WEST	3	CMOS	1	OK	
Cs16k[0]	WEST	3	CMOS	1	OK	
Mem_addr[22]	WEST	3	CMOS	1	OK	
Mem_addr[21]	WEST	3	CMOS	1	OK	
Ring_vss[6]	WEST		POWER			

Mem_addr[20]	WEST	3	CMOS	1	OK
Mem_addr[19]	WEST	3	CMOS	1	OK
Mem_addr[18]	WEST	3	CMOS	1	OK
Mem_addr[17]	WEST	3	CMOS	1	OK
Mem_addr[16]	WEST	3	CMOS	1	OK
Mem_addr[15]	WEST	3	CMOS	1	OK
Ring_vss[5]	WEST		POWER		
Mem_addr[14]	WEST	3	CMOS	1	OK
Mem_addr[13]	WEST	3	CMOS	1	OK
Mem_addr[12]	WEST	3	CMOS	1	OK
Mem_addr[11]	WEST	3	CMOS	1	OK
Mem_addr[10]	WEST	3	CMOS	1	OK
Mem_addr[9]	WEST	3	CMOS	1	OK

Ring_vss[4]	NORTH		POWER		
Mem_addr[8]	NORTH	3	CMOS	1	OK
Mem_addr[7]	NORTH	3	CMOS	1	OK
Mem_addr[6]	NORTH	3	CMOS	1	OK
Mem_addr[5]	NORTH	3	CMOS	1	OK
Mem_addr[4]	NORTH	3	CMOS	1	OK
Mem_addr[3]	NORTH	3	CMOS	1	OK
Ring_vss[3]	NORTH		POWER		
Mem_addr[2]	NORTH	3	CMOS	1	OK
Mem_addr[1]	NORTH	3	CMOS	1	OK
Mem_addr[0]	NORTH	3	CMOS	1	OK
N_oe	NORTH	2	CMOS	1	OK
N_we	NORTH	2	CMOS	1	OK
Mem_data[15]	NORTH	2	CMOS	1	OK
Mem_data[14]	NORTH	2	CMOS	1	OK
Mem_data[13]	NORTH	2	CMOS	1	OK
Mem_data[12]	NORTH	2	CMOS	1	OK
Ring_vss[2]	NORTH		POWER		
Mem_data[11]	NORTH	2	CMOS	1	OK
Mem_data[10]	NORTH	2	CMOS	1	OK
Mem_data[9]	NORTH	2	CMOS	1	OK
Mem_data[8]	NORTH	2	CMOS	1	OK
Mem_data[7]	NORTH	2	CMOS	1	OK
Mem_data[6]	NORTH	2	CMOS	1	OK
Mem_data[5]	NORTH	2	CMOS	1	OK
Mem_data[4]	NORTH	2	CMOS	1	OK
Mem_data[3]	NORTH	2	CMOS	1	OK
Mem_data[2]	NORTH	2	CMOS	1	OK
Mem_data[1]	NORTH	2	CMOS	2	OK
Mem_data[0]	NORTH	2	CMOS	2	OK

Ring_vss[1]	EAST		POWER		
Host_data[15]	EAST	2	CMOS	2	OK
Host_data[14]	EAST	2	CMOS	2	OK
Host_data[13]	EAST	2	CMOS	2	OK
Host_data[12]	EAST	2	CMOS	2	OK
Ring_vss[0]	EAST		POWER		
Host_data[11]	EAST	2	CMOS	2	OK
Host_data[10]	EAST	2	CMOS	2	OK
Host_data[9]	EAST	2	CMOS	1	OK
Host_data[8]	EAST	2	CMOS	1	OK
Host_data[7]	EAST	2	CMOS	1	OK
Host_data[6]	EAST	2	CMOS	2	OK
Host_data[5]	EAST	2	CMOS	2	OK
Host_data[4]	EAST	2	CMOS	2	OK
Host_data[3]	EAST	2	CMOS	2	OK
Host_data[2]	EAST	2	CMOS	2	OK

Host_data[1]	EAST	2	CMOS	2	OK
corner_vss	EAST		POWER		
Host_data[0]	SOUTH	2	CMOS	2	OK
Dr	SOUTH	2	CMOS	2	OK
Ring_vss[8]	SOUTH		POWER		
End_frame_out	SOUTH	2	CMOS	2	OK
End_row_out	SOUTH	2	CMOS	2	OK
Beg_row_out	SOUTH	2	CMOS	2	OK
Beg_frame_out	SOUTH	2	CMOS	2	OK
Pixel_clk_out	SOUTH	2	CMOS	1	OK

This ring has 2 more VSS pads than it needs

## 9. Power Dissipation

```

) Clock Clk_in [clock=-9999]
) Reading Routing Data . . .
) INFO: longest net delay: 17.0ns
) Nets with delay longer than 10.0ns are recorded in ancillary file LONG_NET STD
) INFO: Nets loading, driving information can be found in ancillary file TA_NET STD
) Back-annotating route capacitance for block power calculation. . .
) Power for block math/strob: 0.00mW(DC) 0.89mW(AC)
) Power for block math/state_mach/subtract: 0.00mW(DC) 3.40mW(AC)
) Power for block math/state_mach/glue: 0.00mW(DC) 22.85mW(AC)
) W: Node math/state_mach/control/n[2] is not routed
) Power for block math/state_mach/control: 0.00mW(DC) 2.07mW(AC)
) Power for block math/state_mach/clock_sync: 0.00mW(DC) 1.50mW(AC)
) Power for block math/state_mach/cal_out_gen: 0.00mW(DC) 31.08mW(AC)
) W: Node math/state_mach/bad_pixel/sel_pixelin/ADDSUB1_COUT is not routed
) W: Node math/state_mach/bad_pixel/sel_pixelin/PORT7_EXT1[16] is not routed
) Power for block math/state_mach/bad_pixel/sel_pixelin: 0.00mW(DC) 2.42mW(AC)
) Power for block math/state_mach/bad_pixel/control: 4.50mW(DC) 0.58mW(AC)
) Power for block math/pre_div/reg_file/reg_sel: 0.00mW(DC) 1.86mW(AC)
) Power for block math/pre_div/reg_file/reg: 0.00mW(DC) 4.45mW(AC)
) Power for block math/pre_div/pix_cal_sub: 0.00mW(DC) 6.77mW(AC)
) Power for block math/pre_div/mult/mult_out: 0.00mW(DC) 21.84mW(AC)
) Power for block math/pre_div/mult/mult_block/mult1: 0.00mW(DC) 14.58mW(AC)
) Power for block math/pre_div/mult/mult_block/mult0: 0.00mW(DC) 15.13mW(AC)
) Power for block math/pre_div/mult/mult_block/ms_add1: 0.00mW(DC) 3.68mW(AC)
) Power for block math/pre_div/mult/mult_block/ms_add0: 0.00mW(DC) 3.62mW(AC)
) Power for block math/pre_div/mult/mult_block/gate_m1: 0.00mW(DC) 3.44mW(AC)
) Power for block math/pre_div/mult/mult_block/gate_m0: 0.00mW(DC) 3.41mW(AC)
) Power for block math/pre_div/mult/mult_block/final_add: 0.00mW(DC) 6.38mW(AC)
) Power for block math/pre_div/int_sub: 0.00mW(DC) 4.34mW(AC)
) Power for block math/pre_div/cal_out_sub: 0.00mW(DC) 5.45mW(AC)
) Power for block math/pixel_out/datapath: 0.00mW(DC) 3.67mW(AC)
) Power for block math/pixel_out/control: 0.00mW(DC) 0.14mW(AC)
) Power for block math/pix_counter: 0.00mW(DC) 16.34mW(AC)
) Power for block math/pipe/shifter: 0.00mW(DC) 6.02mW(AC)
) Power for block math/pipe/cal_int_n: 0.00mW(DC) 4.51mW(AC)
) Power for block math/pipe/buf_tree: 0.00mW(DC) 0.56mW(AC)
) Power for block math/overflow: 0.00mW(DC) 8.31mW(AC)
) Power for block math/mem_host_if: 0.00mW(DC) 58.97mW(AC)
) Power for block math/frame_sync: 0.00mW(DC) 38.82mW(AC)
) Power for block math/divider2: 0.00mW(DC) 153.65mW(AC)
) Power for block math/divider1: 0.00mW(DC) 190.09mW(AC)
) Power for block corner_vss: 0.00mW(DC) 0.00mW(AC)
) Power for block corner_vdd: 0.00mW(DC) 0.00mW(AC)
) Power for block corner_test: 0.00mW(DC) 0.12mW(AC)

```

) Power for block core\_vss: 0.00mW(DC) 0.00mW(AC)  
) Power for block core\_vdd: 0.00mW(DC) 0.00mW(AC)  
) Power for block clk\_pad: 0.00mW(DC) 33.88mW(AC)  
) Power for block Ring\_vss: 0.00mW(DC) 0.00mW(AC)  
) Power for block Ring\_vdd: 0.00mW(DC) 0.00mW(AC)  
) Power for block Pixel\_out[9]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[8]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[7]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[6]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[5]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[4]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[3]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[2]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[1]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[15]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[14]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[13]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[12]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[11]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[10]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_out[0]: 0.00mW(DC) 4.26mW(AC)  
) Power for block Pixel\_clk\_out: 0.00mW(DC) 4.50mW(AC)  
) Power for block Pixel\_clk\_in: 0.00mW(DC) 0.22mW(AC)  
) Power for block Ode: 0.00mW(DC) 0.54mW(AC)  
) Power for block N\_we: 0.00mW(DC) 4.26mW(AC)  
) Power for block N\_reset: 0.00mW(DC) 0.91mW(AC)  
) Power for block N\_oe: 0.00mW(DC) 4.26mW(AC)  
) Power for block Mem\_data[9]: 0.00mW(DC) 4.56mW(AC)  
) Power for block Mem\_data[8]: 0.00mW(DC) 4.63mW(AC)  
) Power for block Mem\_data[7]: 0.00mW(DC) 4.58mW(AC)  
) Power for block Mem\_data[6]: 0.00mW(DC) 4.63mW(AC)  
) Power for block Mem\_data[5]: 0.00mW(DC) 4.60mW(AC)  
) Power for block Mem\_data[4]: 0.00mW(DC) 4.64mW(AC)  
) Power for block Mem\_data[3]: 0.00mW(DC) 4.68mW(AC)  
) Power for block Mem\_data[2]: 0.00mW(DC) 4.67mW(AC)  
) Power for block Mem\_data[1]: 0.00mW(DC) 4.70mW(AC)  
) Power for block Mem\_data[15]: 0.00mW(DC) 4.62mW(AC)  
) Power for block Mem\_data[14]: 0.00mW(DC) 4.58mW(AC)  
) Power for block Mem\_data[13]: 0.00mW(DC) 4.58mW(AC)  
) Power for block Mem\_data[12]: 0.00mW(DC) 4.59mW(AC)  
) Power for block Mem\_data[11]: 0.00mW(DC) 4.57mW(AC)  
) Power for block Mem\_data[10]: 0.00mW(DC) 4.57mW(AC)  
) Power for block Mem\_data[0]: 0.00mW(DC) 4.69mW(AC)  
) Power for block Mem\_addr[9]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[8]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[7]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[6]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[5]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[4]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[3]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[2]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[22]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[21]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[20]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[1]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[19]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[18]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[17]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[16]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[15]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[14]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[13]: 0.00mW(DC) 4.50mW(AC)

) Power for block Mem\_addr[12]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[11]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[10]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Mem\_addr[0]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Host\_data[9]: 0.00mW(DC) 4.80mW(AC)  
) Power for block Host\_data[8]: 0.00mW(DC) 4.79mW(AC)  
) Power for block Host\_data[7]: 0.00mW(DC) 4.81mW(AC)  
) Power for block Host\_data[6]: 0.00mW(DC) 4.79mW(AC)  
) Power for block Host\_data[5]: 0.00mW(DC) 4.81mW(AC)  
) Power for block Host\_data[4]: 0.00mW(DC) 4.81mW(AC)  
) Power for block Host\_data[3]: 0.00mW(DC) 4.84mW(AC)  
) Power for block Host\_data[2]: 0.00mW(DC) 4.84mW(AC)  
) Power for block Host\_data[1]: 0.00mW(DC) 4.86mW(AC)  
) Power for block Host\_data[15]: 0.00mW(DC) 4.75mW(AC)  
) Power for block Host\_data[14]: 0.00mW(DC) 4.77mW(AC)  
) Power for block Host\_data[13]: 0.00mW(DC) 4.75mW(AC)  
) Power for block Host\_data[12]: 0.00mW(DC) 4.79mW(AC)  
) Power for block Host\_data[11]: 0.00mW(DC) 4.78mW(AC)  
) Power for block Host\_data[10]: 0.00mW(DC) 4.79mW(AC)  
) Power for block Host\_data[0]: 0.00mW(DC) 4.88mW(AC)  
) Power for block Host\_addr[4]: 0.00mW(DC) 0.51mW(AC)  
) Power for block Host\_addr[3]: 0.00mW(DC) 0.51mW(AC)  
) Power for block Host\_addr[2]: 0.00mW(DC) 0.52mW(AC)  
) Power for block Host\_addr[1]: 0.00mW(DC) 0.52mW(AC)  
) Power for block Host\_addr[0]: 0.00mW(DC) 0.56mW(AC)  
) Power for block Fpa\_pixel[9]: 0.00mW(DC) 0.26mW(AC)  
) Power for block Fpa\_pixel[8]: 0.00mW(DC) 0.26mW(AC)  
) Power for block Fpa\_pixel[7]: 0.00mW(DC) 0.25mW(AC)  
) Power for block Fpa\_pixel[6]: 0.00mW(DC) 0.25mW(AC)  
) Power for block Fpa\_pixel[5]: 0.00mW(DC) 0.23mW(AC)  
) Power for block Fpa\_pixel[4]: 0.00mW(DC) 0.23mW(AC)  
) Power for block Fpa\_pixel[3]: 0.00mW(DC) 0.23mW(AC)  
) Power for block Fpa\_pixel[2]: 0.00mW(DC) 0.23mW(AC)  
) Power for block Fpa\_pixel[1]: 0.00mW(DC) 0.22mW(AC)  
) Power for block Fpa\_pixel[15]: 0.00mW(DC) 0.31mW(AC)  
) Power for block Fpa\_pixel[14]: 0.00mW(DC) 0.32mW(AC)  
) Power for block Fpa\_pixel[13]: 0.00mW(DC) 0.33mW(AC)  
) Power for block Fpa\_pixel[12]: 0.00mW(DC) 0.34mW(AC)  
) Power for block Fpa\_pixel[11]: 0.00mW(DC) 0.29mW(AC)  
) Power for block Fpa\_pixel[10]: 0.00mW(DC) 0.29mW(AC)  
) Power for block Fpa\_pixel[0]: 0.00mW(DC) 0.24mW(AC)  
) Power for block End\_row\_out: 0.00mW(DC) 4.26mW(AC)  
) Power for block End\_row\_in: 0.00mW(DC) 0.35mW(AC)  
) Power for block End\_frame\_out: 0.00mW(DC) 4.26mW(AC)  
) Power for block End\_frame\_in: 0.00mW(DC) 0.20mW(AC)  
) Power for block Dr: 0.00mW(DC) 4.20mW(AC)  
) Power for block Dev\_sel[3]: 0.00mW(DC) 0.52mW(AC)  
) Power for block Dev\_sel[2]: 0.00mW(DC) 0.51mW(AC)  
) Power for block Dev\_sel[1]: 0.00mW(DC) 0.51mW(AC)  
) Power for block Dev\_sel[0]: 0.00mW(DC) 0.51mW(AC)  
) Power for block Cs32k[2]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs32k[1]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs32k[0]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs16k[4]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs16k[3]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs16k[2]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs16k[1]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Cs16k[0]: 0.00mW(DC) 4.50mW(AC)  
) Power for block Chip\_id[3]: 0.00mW(DC) 0.35mW(AC)  
) Power for block Chip\_id[2]: 0.00mW(DC) 0.34mW(AC)  
) Power for block Chip\_id[1]: 0.00mW(DC) 0.33mW(AC)  
) Power for block Chip\_id[0]: 0.00mW(DC) 0.33mW(AC)

```

) Power for block Beg_row_out: 0.00mW(DC) 4.26mW(AC)
) Power for block Beg_row_in: 0.00mW(DC) 0.36mW(AC)
) Power for block Beg_frame_out: 0.00mW(DC) 4.26mW(AC)
) Power for block Beg_frame_in: 0.00mW(DC) 0.47mW(AC)
) Total power consumption (5.5V, 0 DegC 50pf/out_pad):
)   DC:          4.50mW [4.50(core)+0.00(ring)]
)   AC@10MHz:   1080.85mW [654.19(core)+426.66(ring)]

```

## 10. Timing Setup Files

### 10.1. reg\_room.040

```

LABEL Jn temp 63.0, 5.0V Power=1.07
TEMP_VOLT 63 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk_in
BIND math/mem_host_if/calibrate 0 1
BIND N_reset/N_reset 1 1
IGNORE_PATH math/mem_host_if/order[0] math/state_mach/control/order[0]
IGNORE_PATH math/mem_host_if/order[1] math/state_mach/control/order[1]
IGNORE_PATH math/mem_host_if/order[2] math/state_mach/control/order[2]
IGNORE_PATH math/mem_host_if/test_int_sub math/pre_div/int_sub/test_int_sub
IGNORE_PATH math/mem_host_if/test math/pre_div/mult/mult_out/test
IGNORE_PATH math/mem_host_if/host_pix_sel math/state_mach/cal_out_gen/host_pix_sel
IGNORE_PATH math/mem_host_if/calibrate math/state_mach/bad_pixel/sel_pixelin/calibrate
IGNORE_PATH math/mem_host_if/calibrate math/state_mach/glue/calibrate

```

### 10.2. reg\_worst.040

```

LABEL Jn temp 113, 4.5V Power=1.07W
TEMP_VOLT 113 4.50
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk_in
BIND N_reset/N_reset 1 1
IGNORE_PATH math/mem_host_if/order[0] math/state_mach/control/order[0]
IGNORE_PATH math/mem_host_if/order[1] math/state_mach/control/order[1]
IGNORE_PATH math/mem_host_if/order[2] math/state_mach/control/order[2]
IGNORE_PATH math/mem_host_if/test_int_sub math/pre_div/int_sub/test_int_sub
IGNORE_PATH math/mem_host_if/test math/pre_div/mult/mult_out/test
IGNORE_PATH math/mem_host_if/host_pix_sel math/state_mach/cal_out_gen/host_pix_sel
IGNORE_PATH math/mem_host_if/calibrate math/state_mach/bad_pixel/sel_pixelin/calibrate
IGNORE_PATH math/mem_host_if/calibrate math/state_mach/glue/calibrate

```

# 11. Timing Reports

## 11.1. <Clk\_in>, GUARANTEED, Max T, Min V

```

*****
                Genesil Version v8.0.3 -- Thu May 30 14:16:54 1991
Chip: /mntb/nuc/nuc/gt_nuc/nuc
                Timing Analyzer
*****
CLOCK REPORT MODE
-----
Fabline: HP2_CN10B-----Corner: GUARANTEED
Junction Temperature:113 deg C      Voltage:4.50v
External Clock: Clk_in
Included setup files:
#0 reg_worst          (Jn temp 113, 4.5V Power=1.07W)
-----
                                CLOCK TIMES (minimum)
Phase 1 High:    55.1 ns          Phase 2 High:    57.2 ns
-----
Cycle (from Ph1): 115.8 ns      Cycle (from Ph2): 90.5 ns
-----
Minimum Cycle Time: 115.8 ns    Symmetric Cycle Time: 115.8 ns
-----
                                CLOCK WORST CASE PATHS
Minimum Phase 1 high time is 55.1 ns set by:
-----
** Clock delay: 4.4ns (59.5-55.1)
Node                Cumulative Delay      Transition
math/divider1/(internal)    59.5          fall
math/divider1/n[28]         58.2          rise
<v/mult/mult_out/numerator[28]    58.0          rise
</mult/mult_out/numerator[28]'    56.6          rise
<th/pre_div/mult/mult_out/_N23    56.2          fall
<h/pre_div/mult/mult_out/n[28]    54.8          rise
<block/final_add/final_sum[20]    54.8          rise
<lock/final_add/final_sum[20]'    51.6          rise
</mult_block/final_add/sum0[8]    39.2          rise
<lt/mult_block/ms_add0/sum0[8]    39.2          rise
<t/mult_block/ms_add0/sum0[8]'    38.3          rise
<t/mult_block/ms_add0/m0_ms[0]    25.9          fall
</mult_block/gate_m0/and_ms[0]    25.8          fall
<mult_block/gate_m0/and_ms[0]'    25.3          fall
<mult_block/gate_m0/disable_ms    20.4          rise
math/mem_host_if/disable_ms       19.9          rise
math/mem_host_if/disable_ms'      17.4          rise
math/mem_host_if/_N389            17.1          fall
<f/host_ctrl.ctrlword.out_x[9]    16.2          rise
math/mem_host_if/PHASE_A          11.2          rise
clk_pad/PHASE_A                   10.4          rise
Clk_in                             0.0          rise

Minimum Phase 2 high time is 57.2 ns set by:
-----
** Clock delay: 5.3ns (62.5-57.2)
Node                Cumulative Delay      Transition
<_div/mult/mult_out/(internal)    62.5          fall
<e_div/mult/mult_out/ld_num_hi    61.3          rise
<h/mem_host_if/ld_numerator_hi    61.0          rise
</mem_host_if/ld_numerator_hi'    59.3          rise

```

math/mem_host_if/_N385	59.0	fall
math/mem_host_if/_N455	57.7	rise
<host_if/host_data.mux1.SEL_1_	55.4	fall
math/mem_host_if/_N250	41.1	rise
math/mem_host_if/host_addr[1]	9.9	fall
Host_addr[1]/host_addr	8.3	fall
Host_addr[1]/host_addr'	4.2	fall
Host_addr[1]	0.0	fall

Minimum cycle time (from Ph1) is 115.8 ns set by:

-----  
 \*\* Clock delay: 10.8ns (126.7-115.8)

Node	Cumulative Delay	Transition
</Row15.fft15.SHIFT2.mout_y[3]	126.7	rise
</Row16.row16.csx_3.NAND10.OUT	125.0	rise
math/divider1/_N1584	123.6	fall
math/divider1/_N206	123.0	rise
math/divider1/_N205	122.0	fall
math/divider1/_N70	121.3	rise
math/divider1/_N1692	106.0	fall
</Row16.row16.csx_14.NAND4.OUT	105.4	rise
math/divider1/_N81	104.1	fall
math/divider1/_N80	103.5	rise
math/divider1/_N1677	102.9	fall
math/divider1/_N1339	101.3	rise
math/divider1/_N493	100.5	fall
</Row16.row16.csx_12.NAND4.OUT	99.8	rise
math/divider1/_N35	98.5	fall
math/divider1/_N34	97.9	rise
math/divider1/_N1647	97.2	fall
math/divider1/_N404	96.0	rise
math/divider1/_N1632	94.9	fall
math/divider1/_N372	93.7	rise
math/divider1/_N374	92.9	fall
<1/Row16.row16.csx_9.NAND4.OUT	92.1	rise
math/divider1/_N125	88.9	fall
<1/Row16.row16.csx_8.NAND4.OUT	88.1	rise
math/divider1/_N96	87.0	fall
math/divider1/_N95	86.4	rise
math/divider1/_N1585	85.6	fall
math/divider1/_N339	84.4	rise
math/divider1/_N1570	83.2	fall
<1/Row16.row16.csx_5.NAND4.OUT	81.7	rise
math/divider1/_N1555	80.1	fall
<1/Row16.row16.csx_4.NAND4.OUT	78.9	rise
math/divider1/_N1540	77.0	fall
math/divider1/_N1448	76.0	rise
math/divider1/_N1525	74.5	fall
<1/Row16.row16.csx_2.NAND4.OUT	72.7	rise
math/divider1/_N1510	71.0	fall
math/divider1/_N927	70.2	rise
math/divider1/_N1495	68.3	fall
<1/Row16.row16.csx_1.NAND4.OUT	67.4	rise
math/divider1/_N110	64.5	fall
math/divider1/_N1483	64.0	rise
math/divider1/n16[16]	61.9	fall
math/divider1/n16[16]'	57.0	fall
*<6.INTER0.std2.latch_data[16]	53.2	fall
math/divider1/n[16]	50.3	fall
<v/mult/mult_out/numerator[16]	50.1	fall
</mult/mult_out/numerator[16]'	49.6	fall
<th/pre_div/mult/mult_out/_N49	49.2	rise

<h/pre_div/mult/mult_out/n[16]	46.6	fall
<_block/final_add/final_sum[8]	46.6	fall
<block/final_add/final_sum[8]'	45.7	fall
</mult_block/final_add/sum0[1]	33.8	fall
<lt/mult_block/ms_add0/sum0[1]	33.8	fall
<t/mult_block/ms_add0/sum0[1]'	33.4	fall
<t/mult_block/ms_add0/m0_ms[0]	25.9	fall
</mult_block/gate_m0/and_ms[0]	25.8	fall
<mult_block/gate_m0/and_ms[0]'	25.3	fall
<mult_block/gate_m0/disable_ms	20.4	rise
math/mem_host_if/disable_ms	19.9	rise
math/mem_host_if/disable_ms'	17.4	rise
math/mem_host_if/_N389	17.1	fall
<f/host_ctrl.ctrlword.out_x[9]	16.2	rise
math/mem_host_if/PHASE_A	11.2	rise
clk_pad/PHASE_A	10.4	rise
Clk_in	0.0	rise

Minimum cycle time (from Ph2) is 90.5 ns set by:

\*\* Clock delay: 12.3ns (102.8-90.5)

Node	Cumulative Delay	Transition
math/pre_div/pix_cal_sub/28	102.8	fall
*<e_div/pix_cal_sub/(internal)	101.0	rise
math/pre_div/pix_cal_sub/n_ovf	97.0	fall
<th/pre_div/pix_cal_sub/n_ovf'	96.8	fall
<v/pix_cal_sub/invert_2_IV2[0]	74.9	fall
</pre_div/pix_cal_sub/BUS_B[0]	73.9	rise
<mach/cal_out_gen/cal_out_n[0]	73.3	rise
<ach/cal_out_gen/cal_out_n[0]'	70.6	rise
<h/state_mach/cal_out_gen/_N95	70.1	fall
<h/state_mach/cal_out_gen/_N64	68.7	rise
<state_mach/cal_out_gen/swapBC	56.4	fall
math/state_mach/glue/swapBC	55.7	fall
math/state_mach/glue/swapBC'	54.1	fall
math/state_mach/glue/_N139	53.7	rise
<th/state_mach/glue/swapBC_out	52.1	fall
math/state_mach/control/swapBC	52.0	fall
<th/state_mach/control/swapBC'	51.6	fall
math/state_mach/control/_N36	51.2	rise
math/state_mach/control/_N21	50.5	fall
math/state_mach/control/_N69	49.1	rise
math/state_mach/control/_N33	45.7	fall
math/state_mach/control/_N39	45.0	rise
math/state_mach/control/_N66	44.6	fall
math/state_mach/control/_N32	43.8	rise
math/state_mach/control/gte	43.0	fall
<th/state_mach/subtract/borrow	42.9	fall
<h/state_mach/subtract/borrow'	41.5	fall
</state_mach/subtract/BUS_A[0]	19.3	fall
<h/state_mach/cal_out_gen/a[0]	19.0	fall
</state_mach/cal_out_gen/a[0]'	18.0	fall
</state_mach/cal_out_gen/_N191	17.6	rise
</cal_out_gen/LATCH_A.out_x[0]	16.1	fall
<h/cal_out_gen/LATCH_A.clock_x	13.3	rise
<tate_mach/cal_out_gen/PHASE_B	10.5	rise
clk_pad/PHASE_B	9.7	rise
Clk_in	0.0	fall

\*\*\*\*\*

Genesil Version v8.0.3 -- Thu May 30 14:16:56 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

OUTPUT DELAY MODE

Fabline: HP2\_CN10B-----Corner: GUARANTEED

Junction Temperature:113 deg C Voltage:4.50v

External Clock: Clk\_in

Included setup files:

#0 reg\_worst (Jn temp 113, 4.5V Power=1.07W)

Output	OUTPUT DELAYS (ns)					
	Ph1(r) Delay		Ph2(r) Delay		Loading(pf)	
	Min	Max	Min	Max		
Beg_frame_out	24.5	26.6	---	---	50.00	PATH
Beg_row_out	24.6	26.7	---	---	50.00	PATH
Cs16k[0]	---	---	18.7	22.8	50.00	PATH
Cs16k[1]	---	---	18.7	22.7	50.00	PATH
Cs16k[2]	---	---	18.7	22.7	50.00	PATH
Cs16k[3]	---	---	18.7	22.7	50.00	PATH
Cs16k[4]	---	---	18.6	22.7	50.00	PATH
Cs32k[0]	---	---	18.6	22.7	50.00	PATH
Cs32k[1]	---	---	18.6	22.7	50.00	PATH
Cs32k[2]	---	---	18.6	22.7	50.00	PATH
Dr	23.4	28.5	23.4	28.5	50.00	PATH
End_frame_out	24.2	26.4	---	---	50.00	PATH
End_row_out	24.3	26.5	---	---	50.00	PATH
Host_data[0]	24.1	121.3	24.1	111.9	50.00	PATH
Host_data[10]	24.0	120.3	24.0	113.8	50.00	PATH
Host_data[11]	24.0	121.1	24.0	115.5	50.00	PATH
Host_data[12]	24.0	120.2	24.0	112.0	50.00	PATH
Host_data[13]	23.9	119.9	23.9	116.9	50.00	PATH
Host_data[14]	23.9	122.3	23.9	116.8	50.00	PATH
Host_data[15]	23.9	121.5	23.9	113.3	50.00	PATH
Host_data[1]	24.1	120.3	24.1	113.1	50.00	PATH
Host_data[2]	24.1	120.7	24.1	113.8	50.00	PATH
Host_data[3]	24.1	120.2	24.1	112.4	50.00	PATH
Host_data[4]	24.1	122.0	24.1	113.9	50.00	PATH
Host_data[5]	24.1	122.6	24.1	113.1	50.00	PATH
Host_data[6]	24.1	121.4	24.1	113.3	50.00	PATH
Host_data[7]	24.1	123.7	24.1	115.6	50.00	PATH
Host_data[8]	24.1	122.2	24.1	114.0	50.00	PATH
Host_data[9]	24.1	122.1	24.1	112.7	50.00	PATH
Mem_addr[0]	---	---	19.0	23.0	50.00	PATH
Mem_addr[10]	---	---	18.9	23.0	50.00	PATH
Mem_addr[11]	---	---	18.9	23.0	50.00	PATH
Mem_addr[12]	---	---	18.9	23.0	50.00	PATH
Mem_addr[13]	---	---	18.9	23.0	50.00	PATH
Mem_addr[14]	---	---	18.9	23.0	50.00	PATH
Mem_addr[15]	---	---	18.9	22.9	50.00	PATH
Mem_addr[16]	---	---	18.9	22.9	50.00	PATH
Mem_addr[17]	---	---	18.8	22.9	50.00	PATH
Mem_addr[18]	---	---	18.8	22.9	50.00	PATH
Mem_addr[19]	---	---	18.8	22.9	50.00	PATH
Mem_addr[1]	---	---	19.0	23.0	50.00	PATH
Mem_addr[20]	---	---	18.8	22.9	50.00	PATH
Mem_addr[21]	---	---	18.8	22.8	50.00	PATH
Mem_addr[22]	---	---	18.7	22.8	50.00	PATH
Mem_addr[2]	---	---	19.0	23.0	50.00	PATH
Mem_addr[3]	---	---	19.0	23.0	50.00	PATH

Mem_addr[4]	---	---	19.0	23.0	50.00	PATH
Mem_addr[5]	---	---	19.0	23.0	50.00	PATH
Mem_addr[6]	---	---	19.0	23.0	50.00	PATH
Mem_addr[7]	---	---	19.0	23.0	50.00	PATH
Mem_addr[8]	---	---	19.0	23.0	50.00	PATH
Mem_addr[9]	---	---	18.9	23.0	50.00	PATH
Mem_data[0]	---	---	25.4	27.9	50.00	PATH
Mem_data[10]	---	---	24.2	27.3	50.00	PATH
Mem_data[11]	---	---	24.6	27.9	50.00	PATH
Mem_data[12]	---	---	24.3	27.5	50.00	PATH
Mem_data[13]	---	---	24.2	27.2	50.00	PATH
Mem_data[14]	---	---	24.1	27.2	50.00	PATH
Mem_data[15]	---	---	24.4	27.7	50.00	PATH
Mem_data[1]	---	---	24.5	27.4	50.00	PATH
Mem_data[2]	---	---	24.7	27.5	50.00	PATH
Mem_data[3]	---	---	24.5	27.4	50.00	PATH
Mem_data[4]	---	---	25.1	27.8	50.00	PATH
Mem_data[5]	---	---	24.8	27.6	50.00	PATH
Mem_data[6]	---	---	24.8	27.6	50.00	PATH
Mem_data[7]	---	---	24.6	27.5	50.00	PATH
Mem_data[8]	---	---	24.5	27.4	50.00	PATH
Mem_data[9]	---	---	24.3	27.3	50.00	PATH
N_mem_oe	---	---	22.5	24.7	50.00	PATH
N_mem_we	28.2	28.2	36.1	40.2	50.00	PATH
Pixel_clk_out	19.3	23.4	---	---	50.00	PATH
Pixel_out[0]	34.3	68.5	41.1	66.8	50.00	PATH
Pixel_out[10]	33.6	68.0	40.5	66.3	50.00	PATH
Pixel_out[11]	33.2	67.6	40.1	66.0	50.00	PATH
Pixel_out[12]	33.3	67.7	40.1	66.0	50.00	PATH
Pixel_out[13]	33.1	67.5	40.0	65.9	50.00	PATH
Pixel_out[14]	32.8	67.3	39.6	65.6	50.00	PATH
Pixel_out[15]	34.0	68.2	40.9	66.5	50.00	PATH
Pixel_out[1]	35.8	69.9	42.7	68.2	50.00	PATH
Pixel_out[2]	36.6	70.3	43.5	68.7	50.00	PATH
Pixel_out[3]	36.3	70.2	43.2	68.6	50.00	PATH
Pixel_out[4]	36.4	70.3	43.3	68.7	50.00	PATH
Pixel_out[5]	35.4	69.3	42.3	67.7	50.00	PATH
Pixel_out[6]	35.4	69.4	42.3	67.7	50.00	PATH
Pixel_out[7]	34.6	68.7	41.5	67.1	50.00	PATH
Pixel_out[8]	37.1	70.9	44.0	69.2	50.00	PATH
Pixel_out[9]	34.0	68.3	40.9	66.6	50.00	PATH

\*\*\*\*\*

Genesil Version v8.0.3 -- Thu May 30 14:19:37 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

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SETUP AND HOLD MODE

-----  
 Fabline: HP2\_CN10B-----Corner: GUARANTEED

Junction Temperature:113 deg C Voltage:4.50v

External Clock: Clk\_in

Included setup files:

#0 reg\_worst (Jn temp 113, 4.5V Power=1.07W)

-----INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
Beg_frame_in	---	6.6	---	-2.2	PATH
Beg_row_in	---	3.7	---	-0.7	PATH
Chip_id[0]	48.8	---	-4.5	---	PATH
Chip_id[1]	48.9	---	-3.8	---	PATH
Chip_id[2]	48.1	---	-3.5	---	PATH
Chip_id[3]	49.5	---	-5.1	---	PATH
Dev_sel[0]	51.9	---	-8.0	---	PATH
Dev_sel[1]	52.6	---	-7.1	---	PATH
Dev_sel[2]	51.5	---	-7.1	---	PATH
Dev_sel[3]	52.5	---	-8.4	---	PATH
End_frame_in	---	1.3	---	1.7	PATH
End_row_in	---	3.6	---	-0.6	PATH
Fpa_pixel[0]	---	0.8	---	2.1	PATH
Fpa_pixel[10]	---	0.8	---	2.1	PATH
Fpa_pixel[11]	---	0.9	---	2.1	PATH
Fpa_pixel[12]	---	2.6	---	0.5	PATH
Fpa_pixel[13]	---	2.8	---	0.4	PATH
Fpa_pixel[14]	---	2.8	---	0.4	PATH
Fpa_pixel[15]	---	2.4	---	0.7	PATH
Fpa_pixel[1]	---	0.6	---	2.4	PATH
Fpa_pixel[2]	---	0.7	---	2.2	PATH
Fpa_pixel[3]	---	1.1	---	1.8	PATH
Fpa_pixel[4]	---	1.3	---	1.7	PATH
Fpa_pixel[5]	---	1.1	---	1.8	PATH
Fpa_pixel[6]	---	1.5	---	1.5	PATH
Fpa_pixel[7]	---	1.5	---	1.5	PATH
Fpa_pixel[8]	---	1.8	---	1.3	PATH
Fpa_pixel[9]	---	1.7	---	1.3	PATH
Host_addr[0]	23.4	---	-5.5	---	PATH
Host_addr[1]	47.6	58.4	-4.6	-20.8	PATH
Host_addr[2]	42.9	45.6	-4.7	-19.2	PATH
Host_addr[3]	33.7	29.1	-4.5	-10.9	PATH
Host_addr[4]	27.6	23.0	-4.6	-8.1	PATH
Host_data[0]	31.9	---	-8.5	---	PATH
Host_data[10]	17.1	---	-6.3	---	PATH
Host_data[11]	16.7	---	-5.9	---	PATH
Host_data[12]	16.4	---	-6.1	---	PATH
Host_data[13]	16.1	---	-5.2	---	PATH
Host_data[14]	16.5	---	-5.7	---	PATH
Host_data[15]	16.0	---	-5.2	---	PATH
Host_data[1]	31.4	---	-7.8	---	PATH
Host_data[2]	22.5	---	-7.4	---	PATH
Host_data[3]	18.4	---	-7.5	---	PATH
Host_data[4]	17.7	---	-6.6	---	PATH
Host_data[5]	17.7	---	-6.8	---	PATH
Host_data[6]	17.5	---	-6.2	---	PATH

Host_data[7]	17.5	---	-6.6	---	PATH
Host_data[8]	17.4	---	-6.3	---	PATH
Host_data[9]	17.1	---	-6.4	---	PATH
Mem_data[0]	---	5.6	---	-0.2	PATH
Mem_data[10]	---	3.4	---	2.1	PATH
Mem_data[11]	---	3.5	---	2.0	PATH
Mem_data[12]	---	4.0	---	1.5	PATH
Mem_data[13]	---	3.8	---	1.7	PATH
Mem_data[14]	---	3.8	---	1.7	PATH
Mem_data[15]	---	4.4	---	1.1	PATH
Mem_data[1]	---	5.8	---	-0.4	PATH
Mem_data[2]	---	5.4	---	0.1	PATH
Mem_data[3]	---	5.6	---	-0.1	PATH
Mem_data[4]	---	4.9	---	0.6	PATH
Mem_data[5]	---	4.2	---	1.3	PATH
Mem_data[6]	---	4.6	---	0.8	PATH
Mem_data[7]	---	3.6	---	1.9	PATH
Mem_data[8]	---	4.6	---	0.9	PATH
Mem_data[9]	---	3.4	---	2.1	PATH
N_reset	14.6	17.8	-9.6	-11.1	PATH
Ode	45.2	---	-1.6	---	PATH
Pixel_clk_in	---	-5.6	---	7.8	PATH

\*\*\*\*\*

Genesil Version v8.0.3 -- Thu May 30 14:19:41 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

VIOLATION MODE

-----  
Fabline: HP2\_CN10B-----Corner: GUARANTEED

Junction Temperature:113 deg C Voltage:4.50v

External Clock: Clk\_in

Included setup files:

#0 reg\_worst (Jn temp 113, 4.5V Power=1.07W)

-----

NO VIOLATIONS

Hold time check margin: 2.0ns

\*\*\*\*\*

### 11.2. <Clk\_in>, GUARANTEED, Room T, 5.0 V

Genesis Version v8.0.3 -- Thu May 30 14:20:05 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

CLOCK REPORT MODE

Fabline: HP2\_CN10B-----Corner: GUARANTEED

Junction Temperature:63 deg C Voltage:5.00v

External Clock: Clk\_in

Included setup files:

#0 reg\_room (Jn temp 63.0, 5.0V Power=1.07)

```

-----
CLOCK TIMES (minimum)
Phase 1 High:    44.6 ns          Phase 2 High:    46.1 ns
-----
Cycle (from Ph1): 93.5 ns          Cycle (from Ph2): 73.1 ns
-----
Minimum Cycle Time: 93.5 ns          Symmetric Cycle Time: 93.5 ns
-----

```

----- CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 44.6 ns set by:

\*\* Clock delay: 3.5ns (48.1-44.6)

Node	Cumulative Delay	Transition
math/divider1/(internal)	48.1	fall
math/divider1/n[28]	47.1	rise
<v/mult/mult_out/numerator[28]	46.9	rise
</mult/mult_out/numerator[28]'	45.8	rise
<th/pre_div/mult/mult_out/_N23	45.5	fall
<h/pre_div/mult/mult_out/n[28]	44.4	rise
<block/final_add/final_sum[20]	44.3	rise
<lock/final_add/final_sum[20]'	41.8	rise
</mult_block/final_add/sum0[8]	31.7	rise
<lt/mult_block/ms_add0/sum0[8]	31.7	rise
<t/mult_block/ms_add0/sum0[8]'	31.0	rise
<t/mult_block/ms_add0/m0_ms[0]	20.9	fall
</mult_block/gate_m0/and_ms[0]	20.8	fall
<mult_block/gate_m0/and_ms[0]'	20.4	fall
<mult_block/gate_m0/disable_ms	16.4	rise
math/mem_host_if/disable_ms	16.0	rise
math/mem_host_if/disable_ms'	14.0	rise
math/mem_host_if/_N389	13.8	fall
<f/host_ctrl.ctrlword.out_x[9]	13.0	rise
math/mem_host_if/PHASE_A	8.9	rise
clk_pad/PHASE_A	8.3	rise
Clk_in	0.0	rise

Minimum Phase 2 high time is 46.1 ns set by:

\*\* Clock delay: 4.3ns (50.4-46.1)

Node	Cumulative Delay	Transition
<_div/mult/mult_out/(internal)	50.4	fall
<e_div/mult/mult_out/ld_num_hi	49.4	rise
<h/mem_host_if/ld_numerator_hi	49.2	rise
</mem_host_if/ld_numerator_hi'	47.8	rise
math/mem_host_if/_N385	47.5	fall
math/mem_host_if/_N455	46.4	rise
<host_if/host_data.mux1.SEL_1	44.6	fall
math/mem_host_if/_N250	32.7	rise

math/mem_host_if/host_addr[1]	7.9	fall
Host_addr[1]/host_addr	6.6	fall
Host_addr[1]/host_addr'	3.3	fall
Host_addr[1]	0.0	fall

Minimum cycle time (from Ph1) is 93.5 ns set by:

\*\* Clock delay: 8.7ns (102.2-93.5)

Node	Cumulative Delay	Transition
</Row15.fft15.SHIFT2.mout_y[3]	102.2	rise
</Row16.row16.csx_3.NAND10.OUT	100.8	rise
math/divider1/_N1584	99.7	fall
math/divider1/_N206	99.2	rise
math/divider1/_N205	98.4	fall
math/divider1/_N70	97.9	rise
math/divider1/_N1692	85.6	fall
</Row16.row16.csx_14.NAND4.OUT	85.2	rise
math/divider1/_N81	84.2	fall
math/divider1/_N80	83.7	rise
math/divider1/_N1677	83.2	fall
math/divider1/_N1339	81.8	rise
math/divider1/_N493	81.2	fall
</Row16.row16.csx_12.NAND4.OUT	80.6	rise
math/divider1/_N35	79.6	fall
math/divider1/_N34	79.1	rise
math/divider1/_N1647	78.5	fall
math/divider1/_N404	77.5	rise
math/divider1/_N1632	76.7	fall
math/divider1/_N372	75.6	rise
math/divider1/_N374	75.0	fall
<1/Row16.row16.csx_9.NAND4.OUT	74.4	rise
math/divider1/_N125	71.8	fall
<1/Row16.row16.csx_8.NAND4.OUT	71.2	rise
math/divider1/_N96	70.2	fall
math/divider1/_N95	69.7	rise
math/divider1/_N1585	69.1	fall
math/divider1/_N339	68.1	rise
math/divider1/_N1570	67.2	fall
<1/Row16.row16.csx_5.NAND4.OUT	66.0	rise
math/divider1/_N1555	64.7	fall
<1/Row16.row16.csx_4.NAND4.OUT	63.7	rise
math/divider1/_N1540	62.2	fall
math/divider1/_N1448	61.3	rise
math/divider1/_N1525	60.1	fall
<1/Row16.row16.csx_2.NAND4.OUT	58.6	rise
math/divider1/_N1510	57.3	fall
math/divider1/_N927	56.6	rise
math/divider1/_N1495	55.1	fall
<1/Row16.row16.csx_1.NAND4.OUT	54.4	rise
math/divider1/_N110	52.1	fall
math/divider1/_N1483	51.6	rise
math/divider1/n16[16]	50.0	fall
math/divider1/n16[16]'	46.0	fall
*<6.INTER0.std2.latch_data[16]	43.0	fall
math/divider1/n[16]	40.7	fall
<v/mult/mult_out/numerator[16]	40.5	fall
</mult/mult_out/numerator[16]'	40.1	fall
<th/pre_div/mult/mult_out/_N49	39.8	rise
<h/pre_div/mult/mult_out/n[16]	37.7	fall
<_block/final_add/final_sum[8]	37.7	fall
<block/final_add/final_sum[8]'	37.0	fall
</mult_block/final_add/sum0[1]	27.3	fall

<lt/mult_block/ms_add0/sum0[1]	27.2	fall
<t/mult_block/ms_add0/sum0[1]'	27.0	fall
<t/mult_block/ms_add0/m0_ms[0]	20.9	fall
</mult_block/gate_m0/and_ms[0]	20.8	fall
<mult_block/gate_m0/and_ms[0]'	20.4	fall
<mult_block/gate_m0/disable_ms	16.4	rise
math/mem_host_if/disable_ms	16.0	rise
math/mem_host_if/disable_ms'	14.0	rise
math/mem_host_if/_N389	13.8	fall
</host_ctrl.ctrlword.out_x[9]	13.0	rise
math/mem_host_if/PHASE_A	8.9	rise
clk_pad/PHASE_A	8.3	rise
Clk_in	0.0	rise

Minimum cycle time (from Ph2) is 73.1 ns set by:

-----  
 \*\* Clock delay: 9.8ns (82.9-73.1)

Node	Cumulative Delay	Transition
.math/pre_div/pix_cal_sub/28	82.9	fall
*<e_div/pix_cal_sub/(internal)	81.5	rise
math/pre_div/pix_cal_sub/n_ovf	78.3	fall
<th/pre_div/pix_cal_sub/n_ovf'	78.1	fall
<v/pix_cal_sub/invert_2_IV2[0]	60.3	fall
</pre_div/pix_cal_sub/BUS_B[0]	59.5	rise
<mach/cal_out_gen/cal_out_n[0]	59.0	rise
<ach/cal_out_gen/cal_out_n[0]'	56.8	rise
<h/state_mach/cal_out_gen/_N95	56.5	fall
<h/state_mach/cal_out_gen/_N64	55.3	rise
<state_mach/cal_out_gen/swapBC	45.5	fall
math/state_mach/glue/swapBC	44.9	fall
math/state_mach/glue/swapBC'	43.7	fall
math/state_mach/glue/_N139	43.3	rise
<th/state_mach/glue/swapBC_out	42.1	fall
math/state_mach/control/swapBC	42.0	fall
<th/state_mach/control/swapBC'	41.6	fall
math/state_mach/control/_N36	41.3	rise
math/state_mach/control/_N21	40.8	fall
math/state_mach/control/_N69	39.6	rise
math/state_mach/control/_N33	36.9	fall
math/state_mach/control/_N39	36.3	rise
math/state_mach/control/_N66	36.0	fall
math/state_mach/control/_N32	35.3	rise
math/state_mach/control/gte	34.7	fall
<th/state_mach/subtract/borrow	34.6	fall
<h/state_mach/subtract/borrow'	33.5	fall
</state_mach/subtract/BUS_A[0]	15.5	fall
<h/state_mach/cal_out_gen/a[0]	15.3	fall
</state_mach/cal_out_gen/a[0]'	14.5	fall
</state_mach/cal_out_gen/_N191	14.1	rise
</cal_out_gen/LATCH_A.out_x[0]	12.9	fall
<h/cal_out_gen/LATCH_A.clock_x	10.7	rise
<tate_mach/cal_out_gen/PHASE_B	8.4	rise
clk_pad/PHASE_B	7.8	rise
Clk_in	0.0	fall

-----

\*\*\*\*\*

Genesil Version v8.0.3 -- Thu May 30 14:20:07 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

OUTPUT DELAY MODE

-----  
 Fabline: HP2\_CN10B-----Corner: GUARANTEED

Junction Temperature:63 deg C Voltage:5.00v

External Clock: Clk\_in

Included setup files:

#0 reg\_room (Jn temp 63.0, 5.0V Power=1.07)

-----

Output	OUTPUT DELAYS (ns)					
	Ph1(r) Delay		Ph2(r) Delay		Loading(pf)	
	Min	Max	Min	Max		
Beg_frame_out	19.6	21.4	---	---	50.00	PATH
Beg_row_out	19.7	21.4	---	---	50.00	PATH
Cs16k[0]	---	---	15.0	18.3	50.00	PATH
Cs16k[1]	---	---	15.0	18.3	50.00	PATH
Cs16k[2]	---	---	15.0	18.3	50.00	PATH
Cs16k[3]	---	---	14.9	18.3	50.00	PATH
Cs16k[4]	---	---	14.9	18.2	50.00	PATH
Cs32k[0]	---	---	14.9	18.2	50.00	PATH
Cs32k[1]	---	---	14.9	18.2	50.00	PATH
Cs32k[2]	---	---	14.9	18.2	50.00	PATH
Dr	18.7	22.8	18.7	22.8	50.00	PATH
End_frame_out	19.4	21.2	---	---	50.00	PATH
End_row_out	19.5	21.3	---	---	50.00	PATH
Host_data[0]	19.3	97.7	19.3	90.1	50.00	PATH
Host_data[10]	19.2	96.9	19.2	91.3	50.00	PATH
Host_data[11]	19.2	97.5	19.2	92.7	50.00	PATH
Host_data[12]	19.1	96.8	19.1	90.1	50.00	PATH
Host_data[13]	19.1	96.6	19.1	93.8	50.00	PATH
Host_data[14]	19.1	98.5	19.1	93.8	50.00	PATH
Host_data[15]	19.1	97.8	19.1	91.2	50.00	PATH
Host_data[1]	19.3	96.9	19.3	90.9	50.00	PATH
Host_data[2]	19.3	97.2	19.3	91.3	50.00	PATH
Host_data[3]	19.3	96.8	19.3	90.2	50.00	PATH
Host_data[4]	19.3	98.3	19.3	91.6	50.00	PATH
Host_data[5]	19.3	98.7	19.3	91.1	50.00	PATH
Host_data[6]	19.2	97.8	19.2	91.1	50.00	PATH
Host_data[7]	19.2	99.6	19.2	93.0	50.00	PATH
Host_data[8]	19.2	98.4	19.2	91.7	50.00	PATH
Host_data[9]	19.2	98.4	19.2	90.8	50.00	PATH
Mem_addr[0]	---	---	15.2	18.5	50.00	PATH
Mem_addr[10]	---	---	15.2	18.5	50.00	PATH
Mem_addr[11]	---	---	15.2	18.5	50.00	PATH
Mem_addr[12]	---	---	15.2	18.5	50.00	PATH
Mem_addr[13]	---	---	15.1	18.5	50.00	PATH
Mem_addr[14]	---	---	15.1	18.5	50.00	PATH
Mem_addr[15]	---	---	15.1	18.4	50.00	PATH
Mem_addr[16]	---	---	15.1	18.4	50.00	PATH
Mem_addr[17]	---	---	15.1	18.4	50.00	PATH
Mem_addr[18]	---	---	15.1	18.4	50.00	PATH
Mem_addr[19]	---	---	15.1	18.4	50.00	PATH
Mem_addr[1]	---	---	15.2	18.5	50.00	PATH
Mem_addr[20]	---	---	15.1	18.4	50.00	PATH
Mem_addr[21]	---	---	15.0	18.3	50.00	PATH
Mem_addr[22]	---	---	15.0	18.3	50.00	PATH
Mem_addr[2]	---	---	15.2	18.5	50.00	PATH
Mem_addr[3]	---	---	15.2	18.5	50.00	PATH

-----

Mem_addr[4]	---	---	15.2	18.5	50.00	PATH
Mem_addr[5]	---	---	15.2	18.5	50.00	PATH
Mem_addr[6]	---	---	15.2	18.5	50.00	PATH
Mem_addr[7]	---	---	15.2	18.5	50.00	PATH
Mem_addr[8]	---	---	15.2	18.5	50.00	PATH
Mem_addr[9]	---	---	15.2	18.5	50.00	PATH
Mem_data[0]	---	---	20.4	22.4	50.00	PATH
Mem_data[10]	---	---	19.4	21.9	50.00	PATH
Mem_data[11]	---	---	19.8	22.3	50.00	PATH
Mem_data[12]	---	---	19.5	22.0	50.00	PATH
Mem_data[13]	---	---	19.5	21.8	50.00	PATH
Mem_data[14]	---	---	19.4	21.8	50.00	PATH
Mem_data[15]	---	---	19.6	22.2	50.00	PATH
Mem_data[1]	---	---	19.7	22.0	50.00	PATH
Mem_data[2]	---	---	19.9	22.1	50.00	PATH
Mem_data[3]	---	---	19.7	22.0	50.00	PATH
Mem_data[4]	---	---	20.2	22.2	50.00	PATH
Mem_data[5]	---	---	19.9	22.1	50.00	PATH
Mem_data[6]	---	---	19.9	22.1	50.00	PATH
Mem_data[7]	---	---	19.8	22.1	50.00	PATH
Mem_data[8]	---	---	19.6	21.9	50.00	PATH
Mem_data[9]	---	---	19.5	21.9	50.00	PATH
N_mem_oe	---	---	18.0	19.8	50.00	PATH
N_mem_we	22.7	22.7	29.0	32.3	50.00	PATH
Pixel_clk_out	15.5	18.8	---	---	50.00	PATH
Pixel_out[0]	27.5	55.1	33.0	53.8	50.00	PATH
Pixel_out[10]	27.0	54.7	32.5	53.4	50.00	PATH
Pixel_out[11]	26.7	54.5	32.2	53.2	50.00	PATH
Pixel_out[12]	26.7	54.5	32.2	53.2	50.00	PATH
Pixel_out[13]	26.6	54.4	32.1	53.1	50.00	PATH
Pixel_out[14]	26.3	54.2	31.8	52.9	50.00	PATH
Pixel_out[15]	27.3	54.9	32.8	53.6	50.00	PATH
Pixel_out[1]	28.8	56.3	34.3	55.0	50.00	PATH
Pixel_out[2]	29.4	56.6	34.9	55.3	50.00	PATH
Pixel_out[3]	29.1	56.5	34.6	55.2	50.00	PATH
Pixel_out[4]	29.2	56.6	34.7	55.3	50.00	PATH
Pixel_out[5]	28.4	55.8	33.9	54.5	50.00	PATH
Pixel_out[6]	28.4	55.8	34.0	54.5	50.00	PATH
Pixel_out[7]	27.8	55.3	33.3	54.0	50.00	PATH
Pixel_out[8]	29.8	57.1	35.3	55.8	50.00	PATH
Pixel_out[9]	27.3	55.0	32.8	53.7	50.00	PATH

\*\*\*\*\*

Genesil Version v8.0.3 -- Thu May 30 14:22:27 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

SETUP AND HOLD MODE

-----  
 Fabline: HP2\_CN10B-----Corner: GUARANTEED

Junction Temperature:63 deg C Voltage:5.00v

External Clock: Clk\_in

Included setup files:

#0 reg\_room (Jn temp 63.0, 5.0V Power=1.07)

-----INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time		Hold Time		PATH
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
Beg_frame_in	---	5.4	---	-1.8	PATH
Beg_row_in	---	3.0	---	-0.6	PATH
Chip_id[0]	39.1	---	-3.7	---	PATH
Chip_id[1]	39.3	---	-3.1	---	PATH
Chip_id[2]	38.6	---	-2.9	---	PATH
Chip_id[3]	39.7	---	-4.2	---	PATH
Dev_sel[0]	41.6	---	-6.4	---	PATH
Dev_sel[1]	42.2	---	-5.7	---	PATH
Dev_sel[2]	41.3	---	-5.8	---	PATH
Dev_sel[3]	42.1	---	-6.8	---	PATH
End_frame_in	---	1.1	---	1.3	PATH
End_row_in	---	3.0	---	-0.6	PATH
Fpa_pixel[0]	---	0.7	---	1.7	PATH
Fpa_pixel[10]	---	0.7	---	1.7	PATH
Fpa_pixel[11]	---	0.8	---	1.6	PATH
Fpa_pixel[12]	---	2.1	---	0.4	PATH
Fpa_pixel[13]	---	2.3	---	0.3	PATH
Fpa_pixel[14]	---	2.3	---	0.3	PATH
Fpa_pixel[15]	---	2.0	---	0.6	PATH
Fpa_pixel[1]	---	0.5	---	1.9	PATH
Fpa_pixel[2]	---	0.6	---	1.7	PATH
Fpa_pixel[3]	---	1.0	---	1.4	PATH
Fpa_pixel[4]	---	1.1	---	1.3	PATH
Fpa_pixel[5]	---	1.0	---	1.4	PATH
Fpa_pixel[6]	---	1.2	---	1.2	PATH
Fpa_pixel[7]	---	1.2	---	1.2	PATH
Fpa_pixel[8]	---	1.5	---	1.0	PATH
Fpa_pixel[9]	---	1.4	---	1.0	PATH
Host_addr[0]	18.8	---	-4.4	---	PATH
Host_addr[1]	38.1	47.0	-3.7	-17.1	PATH
Host_addr[2]	34.3	36.6	-3.8	-15.8	PATH
Host_addr[3]	26.9	23.3	-3.6	-8.9	PATH
Host_addr[4]	22.0	18.4	-3.7	-6.6	PATH
Host_data[0]	25.5	---	-6.8	---	PATH
Host_data[10]	13.7	---	-5.0	---	PATH
Host_data[11]	13.5	---	-4.8	---	PATH
Host_data[12]	13.2	---	-4.9	---	PATH
Host_data[13]	12.9	---	-4.2	---	PATH
Host_data[14]	13.3	---	-4.6	---	PATH
Host_data[15]	12.8	---	-4.2	---	PATH
Host_data[1]	25.2	---	-6.3	---	PATH
Host_data[2]	18.1	---	-5.9	---	PATH
Host_data[3]	14.8	---	-6.0	---	PATH
Host_data[4]	14.2	---	-5.3	---	PATH
Host_data[5]	14.2	---	-5.4	---	PATH
Host_data[6]	14.1	---	-5.0	---	PATH

Host_data[7]	14.0	---	-5.3	---	PATH
Host_data[8]	14.0	---	-5.0	---	PATH
Host_data[9]	13.7	---	-5.1	---	PATH
Mem_data[0]	---	4.6	---	-0.2	PATH
Mem_data[10]	---	2.8	---	1.6	PATH
Mem_data[11]	---	2.8	---	1.6	PATH
Mem_data[12]	---	3.2	---	1.2	PATH
Mem_data[13]	---	3.1	---	1.3	PATH
Mem_data[14]	---	3.1	---	1.3	PATH
Mem_data[15]	---	3.6	---	0.8	PATH
Mem_data[1]	---	4.7	---	-0.3	PATH
Mem_data[2]	---	4.3	---	0.1	PATH
Mem_data[3]	---	4.5	---	-0.1	PATH
Mem_data[4]	---	3.9	---	0.4	PATH
Mem_data[5]	---	3.4	---	1.0	PATH
Mem_data[6]	---	3.8	---	0.6	PATH
Mem_data[7]	---	3.0	---	1.4	PATH
Mem_data[8]	---	3.7	---	0.7	PATH
Mem_data[9]	---	2.8	---	1.7	PATH
N_reset	11.7	14.3	-7.7	-8.9	PATH
Ode	36.3	---	-1.4	---	PATH
Pixel_clk_in	---	-4.4	---	6.2	PATH

```
*****
          Genesil Version v8.0.3 -- Thu May 30 14:22:30 1991
Chip: /mntb/nuc/nuc/gt_nuc/nuc
          Timing Analyzer
*****
VIOLATION MODE
-----
Fabline: HP2_CN10B-----Corner: GUARANTEED
Junction Temperature:63 deg C      Voltage:5.00v
External Clock: Clk_in
Included setup files:
#0 reg_room      (Jn temp 63.0, 5.0V Power=1.07)
-----
NO VIOLATIONS
-----
Hold time check margin: 2.0ns
*****
```

### 11.3. <Clk\_in>, TYPICAL, Max T, Min V

Genesis Version v8.0.3 -- Thu May 30 14:23:58 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

CLOCK REPORT MODE

-----  
 Fabline: HP2\_CN10B-----Corner: TYPICAL

Junction Temperature:113 deg C Voltage:4.50v

External Clock: Clk\_in

Included setup files:

#0 reg\_worst (Jn temp 113, 4.5V Power=1.07W)

-----  
 CLOCK TIMES (minimum)  
 Phase 1 High: 35.4 ns Phase 2 High: 36.2 ns  
 -----  
 Cycle (from Ph1): 74.2 ns Cycle (from Ph2): 57.2 ns  
 -----  
 Minimum Cycle Time: 74.2 ns Symmetric Cycle Time: 74.2 ns  
 -----

-----  
 CLOCK WORST CASE PATHS  
 Minimum Phase 1 high time is 35.4 ns set by:

\*\* Clock delay: 2.5ns (37.9-35.4)

Node	Cumulative Delay	Transition
math/divider1/(internal)	37.9	rise
math/divider1/n[28]	36.3	fall
<v/mult/mult_out/numerator[28]	36.3	fall
</mult/mult_out/numerator[28]'	35.9	fall
<th/pre_div/mult/mult_out/_N23	35.7	rise
<h/pre_div/mult/mult_out/n[28]	33.9	fall
<block/final_add/final_sum[20]	33.9	fall
<lock/final_add/final_sum[20]'	33.2	fall
</mult_block/final_add/sum0[8]	24.8	rise
<lt/mult_block/ms_add0/sum0[8]	24.8	rise
<t/mult_block/ms_add0/sum0[8]'	24.2	rise
<t/mult_block/ms_add0/m0_ms[0]	15.9	fall
</mult_block/gate_m0/and_ms[0]	15.9	fall
<mult_block/gate_m0/and_ms[0]'	15.5	fall
<mult_block/gate_m0/disable_ms	12.3	rise
math/mem_host_if/disable_ms	12.3	rise
math/mem_host_if/disable_ms'	10.9	rise
math/mem_host_if/_N389	10.7	fall
<f/host_ctrl.ctrlword.out_x[9]	10.1	rise
math/mem_host_if/PHASE_A	6.7	rise
clk_pad/PHASE_A	6.7	rise
Clk_in	0.0	rise

Minimum Phase 2 high time is 36.2 ns set by:

\*\* Clock delay: 3.0ns (39.2-36.2)

Node	Cumulative Delay	Transition
math/pix_counter/(internal)	39.2	rise
<h/pix_counter/wr_pix_count_hi	37.6	fall
<h/mem_host_if/wr_pix_count_hi	37.6	fall
</mem_host_if/wr_pix_count_hi'	37.2	fall
math/mem_host_if/_N270	36.9	rise
math/mem_host_if/_N455	35.8	fall
<host_if/host_data.mux1.SEL_1_	35.1	rise
math/mem_host_if/_N250	13.9	fall

math/mem_host_if/host_addr[1]	5.3	rise
Host_addr[1]/host_addr	5.3	rise
Host_addr[1]/host_addr'	2.4	rise
Host_addr[1]	0.0	rise

Minimum cycle time (from Ph1) is 74.2 ns set by:

\*\*\*\*\*  
 \*\* Clock delay: 6.7ns (80.9-74.2)

Node	Cumulative Delay	Transition
</Row15.fft15.SHIFT2.mout_y[3]	80.9	rise
</Row16.row16.csx_3.NAND10.OUT	79.9	rise
math/divider1/_N1584	78.9	fall
math/divider1/_N206	78.6	rise
math/divider1/_N205	77.9	fall
math/divider1/_N70	77.5	rise
math/divider1/_N1692	67.9	fall
</Row16.row16.csx_14.NAND4.OUT	67.5	rise
math/divider1/_N81	66.7	fall
math/divider1/_N80	66.3	rise
math/divider1/_N1677	65.9	fall
math/divider1/_N1339	64.8	rise
math/divider1/_N493	64.4	fall
</Row16.row16.csx_12.NAND4.OUT	63.9	rise
math/divider1/_N35	63.0	fall
math/divider1/_N34	62.7	rise
math/divider1/_N1647	62.2	fall
math/divider1/_N404	61.4	rise
math/divider1/_N1632	60.7	fall
math/divider1/_N372	59.9	rise
math/divider1/_N374	59.4	fall
<1/Row16.row16.csx_9.NAND4.OUT	58.9	rise
math/divider1/_N125	56.8	fall
<1/Row16.row16.csx_8.NAND4.OUT	56.3	rise
math/divider1/_N96	55.6	fall
math/divider1/_N95	55.2	rise
math/divider1/_N1585	54.7	fall
math/divider1/_N339	53.9	rise
math/divider1/_N1570	53.1	fall
<1/Row16.row16.csx_5.NAND4.OUT	52.2	rise
math/divider1/_N1555	51.1	fall
<1/Row16.row16.csx_4.NAND4.OUT	50.3	rise
math/divider1/_N1540	49.1	fall
math/divider1/_N1448	48.5	rise
math/divider1/_N1525	47.4	fall
<1/Row16.row16.csx_2.NAND4.OUT	46.3	rise
math/divider1/_N1510	45.2	fall
math/divider1/_N927	44.7	rise
math/divider1/_N1495	43.4	fall
<1/Row16.row16.csx_1.NAND4.OUT	42.8	rise
math/divider1/_N110	41.0	fall
math/divider1/_N1483	40.6	rise
math/divider1/n16[16]	39.3	fall
math/divider1/n16[16]'	36.3	fall
*<6.INTER0.std2.latch_data[16]	33.8	fall
math/divider1/n[16]	31.9	fall
</mult/mult_out/numerator[16]	31.9	fall
</mult/mult_out/numerator[16]'	31.6	fall
<th/pre_div/mult/mult_out/_N49	31.3	rise
<h/pre_div/mult/mult_out/n[16]	29.6	fall
<_block/final_add/final_sum[8]	29.6	fall
<block/final_add/final_sum[8]'	29.1	fall
</mult_block/final_add/sum0[1]	21.0	fall

<t/mult_block/ms_add0/sum0[1]	21.0	fall
<t/mult_block/ms_add0/sum0[1]'	20.8	fall
<t/mult_block/ms_add0/m0_ms[0]	15.9	fall
</mult_block/gate_m0/and_ms[0]	15.9	fall
<mult_block/gate_m0/and_ms[0]'	15.5	fall
<mult_block/gate_m0/disable_ms	12.3	rise
math/mem_host_if/disable_ms	12.3	rise
math/mem_host_if/disable_ms'	10.9	rise
math/mem_host_if/_N389	10.7	fall
<f/host_ctrl.ctrlword.out_x[9]	10.1	rise
math/mem_host_if/PHASE_A	6.7	rise
clk_pad/PHASE_A	6.7	rise
Clk_in	0.0	rise

Minimum cycle time (from Ph2) is 57.2 ns set by:

\*\* Clock delay: 7.5ns (64.7-57.2)

Node	Cumulative Delay	Transition
math/pre_div/pix_cal_sub/28	64.7	fall
*<e_div/pix_cal_sub/(internal)	63.5	rise
math/pre_div/pix_cal_sub/n_ovf	61.0	fall
<th/pre_div/pix_cal_sub/n_ovf'	60.8	fall
<v/pix_cal_sub/invert_2_IV2[0]	46.7	fall
</pre_div/pix_cal_sub/BUS_B[0]	46.1	rise
<mach/cal_out_gen/cal_out_n[0]	46.1	rise
<ach/cal_out_gen/cal_out_n[0]'	44.5	rise
<h/state_mach/cal_out_gen/_N95	44.2	fall
<h/state_mach/cal_out_gen/_N64	43.2	rise
<state_mach/cal_out_gen/swapBC	35.2	fall
math/state_mach/glue/swapBC	35.2	fall
math/state_mach/glue/swapBC'	34.2	fall
math/state_mach/glue/_N139	33.9	rise
<th/state_mach/glue/swapBC_out	32.9	fall
math/state_mach/control/swapBC	32.9	fall
<th/state_mach/control/swapBC'	32.6	fall
math/state_mach/control/_N36	32.4	rise
math/state_mach/control/_N21	31.9	fall
math/state_mach/control/_N69	31.0	rise
math/state_mach/control/_N33	28.9	fall
math/state_mach/control/_N39	28.4	rise
math/state_mach/control/_N66	28.2	fall
math/state_mach/control/_N32	27.6	rise
math/state_mach/control/gte	27.1	fall
<th/state_mach/subtract/borrow	27.1	fall
<h/state_mach/subtract/borrow'	26.2	fall
</state_mach/subtract/BUS_A[0]	11.9	fall
<h/state_mach/cal_out_gen/a[0]	11.9	fall
</state_mach/cal_out_gen/a[0]'	11.3	fall
</state_mach/cal_out_gen/_N191	11.0	rise
</cal_out_gen/LATCH_A.out_x[0]	10.0	fall
<h/cal_out_gen/LATCH_A.clock_x	8.1	rise
<tate_mach/cal_out_gen/PHASE_B	6.3	rise
clk_pad/PHASE_B	6.3	rise
Clk_in	0.0	fall

\*\*\*\*\*

Genesil Version v8.0.3 -- Thu May 30 14:24:00 1991

Chip: /mntb/nuc/nuc/gt\_nuc/nuc

Timing Analyzer

\*\*\*\*\*

OUTPUT DELAY MODE

Fabline: HP2\_CN10B-----Corner: TYPICAL

Junction Temperature:113 deg C Voltage:4.50v

External Clock: Clk\_in

Included setup files:

#0 reg\_worst (Jn temp 113, 4.5V Power=1.07W)

Output	OUTPUT DELAYS (ns)					
	Ph1(r) Delay		Ph2(r) Delay		Loading(pf)	
	Min	Max	Min	Max		
Beg_frame_out	16.8	18.8	---	---	50.00	PATH
Beg_row_out	16.9	18.8	---	---	50.00	PATH
Cs16k[0]	---	---	13.4	16.6	50.00	PATH
Cs16k[1]	---	---	13.4	16.6	50.00	PATH
Cs16k[2]	---	---	13.4	16.6	50.00	PATH
Cs16k[3]	---	---	13.4	16.6	50.00	PATH
Cs16k[4]	---	---	13.4	16.6	50.00	PATH
Cs32k[0]	---	---	13.4	16.6	50.00	PATH
Cs32k[1]	---	---	13.4	16.6	50.00	PATH
Cs32k[2]	---	---	13.4	16.6	50.00	PATH
Dr	15.9	18.4	15.9	18.4	50.00	PATH
End_frame_out	16.6	18.7	---	---	50.00	PATH
End_row_out	16.7	18.8	---	---	50.00	PATH
Host_data[0]	13.7	77.8	13.7	71.9	50.00	PATH
Host_data[10]	13.7	77.7	13.7	72.7	50.00	PATH
Host_data[11]	13.7	78.2	13.7	73.6	50.00	PATH
Host_data[12]	13.7	77.8	13.7	72.2	50.00	PATH
Host_data[13]	13.7	77.2	13.7	74.4	50.00	PATH
Host_data[14]	13.7	79.2	13.7	74.5	50.00	PATH
Host_data[15]	13.7	78.6	13.7	73.0	50.00	PATH
Host_data[1]	13.7	77.4	13.7	72.3	50.00	PATH
Host_data[2]	13.7	77.7	13.7	72.4	50.00	PATH
Host_data[3]	13.7	77.2	13.7	71.8	50.00	PATH
Host_data[4]	13.7	78.6	13.7	73.0	50.00	PATH
Host_data[5]	13.7	78.4	13.7	72.2	50.00	PATH
Host_data[6]	13.7	78.3	13.7	72.7	50.00	PATH
Host_data[7]	13.7	79.8	13.7	74.2	50.00	PATH
Host_data[8]	13.7	78.8	13.7	73.2	50.00	PATH
Host_data[9]	13.7	78.3	13.7	72.1	50.00	PATH
Mem_addr[0]	---	---	13.4	16.6	50.00	PATH
Mem_addr[10]	---	---	13.4	16.6	50.00	PATH
Mem_addr[11]	---	---	13.4	16.6	50.00	PATH
Mem_addr[12]	---	---	13.4	16.6	50.00	PATH
Mem_addr[13]	---	---	13.4	16.6	50.00	PATH
Mem_addr[14]	---	---	13.4	16.6	50.00	PATH
Mem_addr[15]	---	---	13.4	16.6	50.00	PATH
Mem_addr[16]	---	---	13.4	16.6	50.00	PATH
Mem_addr[17]	---	---	13.4	16.6	50.00	PATH
Mem_addr[18]	---	---	13.4	16.6	50.00	PATH
Mem_addr[19]	---	---	13.4	16.6	50.00	PATH
Mem_addr[1]	---	---	13.4	16.6	50.00	PATH
Mem_addr[20]	---	---	13.4	16.6	50.00	PATH
Mem_addr[21]	---	---	13.4	16.6	50.00	PATH
Mem_addr[22]	---	---	13.4	16.6	50.00	PATH
Mem_addr[2]	---	---	13.4	16.6	50.00	PATH
Mem_addr[3]	---	---	13.4	16.6	50.00	PATH

Mem_addr[4]	---	---	13.4	16.6	50.00	PATH
Mem_addr[5]	---	---	13.4	16.6	50.00	PATH
Mem_addr[6]	---	---	13.4	16.6	50.00	PATH
Mem_addr[7]	---	---	13.4	16.6	50.00	PATH
Mem_addr[8]	---	---	13.4	16.6	50.00	PATH
Mem_addr[9]	---	---	13.4	16.6	50.00	PATH
Mem_data[0]	---	---	17.1	19.4	50.00	PATH
Mem_data[10]	---	---	16.6	19.2	50.00	PATH
Mem_data[11]	---	---	16.8	19.5	50.00	PATH
Mem_data[12]	---	---	16.7	19.3	50.00	PATH
Mem_data[13]	---	---	16.6	19.2	50.00	PATH
Mem_data[14]	---	---	16.6	19.1	50.00	PATH
Mem_data[15]	---	---	16.7	19.4	50.00	PATH
Mem_data[1]	---	---	16.8	19.2	50.00	PATH
Mem_data[2]	---	---	16.8	19.3	50.00	PATH
Mem_data[3]	---	---	16.8	19.3	50.00	PATH
Mem_data[4]	---	---	17.0	19.4	50.00	PATH
Mem_data[5]	---	---	16.9	19.3	50.00	PATH
Mem_data[6]	---	---	16.9	19.3	50.00	PATH
Mem_data[7]	---	---	16.8	19.3	50.00	PATH
Mem_data[8]	---	---	16.7	19.2	50.00	PATH
Mem_data[9]	---	---	16.6	19.2	50.00	PATH
N_mem_oe	---	---	15.5	17.6	50.00	PATH
N_mem_we	19.0	19.0	24.8	27.5	50.00	PATH
Pixel_clk_out	13.9	17.0	---	---	50.00	PATH
Pixel_out[0]	22.2	44.4	24.0	43.8	50.00	PATH
Pixel_out[10]	21.9	44.2	23.7	43.6	50.00	PATH
Pixel_out[11]	21.7	44.1	23.5	43.5	50.00	PATH
Pixel_out[12]	21.8	44.1	23.6	43.5	50.00	PATH
Pixel_out[13]	21.7	44.1	23.5	43.5	50.00	PATH
Pixel_out[14]	21.5	43.9	23.3	43.3	50.00	PATH
Pixel_out[15]	22.2	44.5	24.0	43.9	50.00	PATH
Pixel_out[1]	22.7	44.8	24.5	44.2	50.00	PATH
Pixel_out[2]	23.3	45.2	25.1	44.6	50.00	PATH
Pixel_out[3]	22.9	45.0	24.7	44.4	50.00	PATH
Pixel_out[4]	22.9	45.0	24.7	44.4	50.00	PATH
Pixel_out[5]	22.8	44.9	24.6	44.3	50.00	PATH
Pixel_out[6]	22.8	44.9	24.6	44.3	50.00	PATH
Pixel_out[7]	22.4	44.6	24.2	44.0	50.00	PATH
Pixel_out[8]	23.3	45.2	25.1	44.7	50.00	PATH
Pixel_out[9]	22.1	44.4	23.9	43.8	50.00	PATH

\*\*\*\*\*  
 Genesil Version v8.0.3 -- Thu May 30 14:26:19 1991  
 Chip: /mntb/nuc/nuc/gt\_nuc/nuc  
 Timing Analyzer  
 \*\*\*\*\*

SETUP AND HOLD MODE

-----  
 Fabline: HP2\_CN10B-----Corner: TYPICAL  
 Junction Temperature:113 deg C      Voltage:4.50v  
 External Clock: Clk\_in  
 Included setup files:  
 #0 reg\_worst                      (Jn temp 113, 4.5V Power=1.07W)  
 -----

-----INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time		Hold Time		PATH
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
Beg_frame_in	---	4.5	---	-1.7	PATH
Beg_row_in	---	2.7	---	-0.7	PATH
Chip_id[0]	30.2	---	-3.1	---	PATH
Chip_id[1]	30.1	---	-2.6	---	PATH
Chip_id[2]	29.7	---	-2.4	---	PATH
Chip_id[3]	30.6	---	-3.4	---	PATH
Dev_sel[0]	31.4	---	-4.7	---	PATH
Dev_sel[1]	31.9	---	-4.0	---	PATH
Dev_sel[2]	31.2	---	-4.0	---	PATH
Dev_sel[3]	31.7	---	-4.9	---	PATH
End_frame_in	---	1.3	---	0.7	PATH
End_row_in	---	2.6	---	-0.7	PATH
Fpa_pixel[0]	---	1.0	---	1.0	PATH
Fpa_pixel[10]	---	0.9	---	1.0	PATH
Fpa_pixel[11]	---	1.0	---	1.0	PATH
Fpa_pixel[12]	---	1.9	---	0.1	PATH
Fpa_pixel[13]	---	2.0	---	-0.0	PATH
Fpa_pixel[14]	---	2.0	---	-0.0	PATH
Fpa_pixel[15]	---	1.8	---	0.2	PATH
Fpa_pixel[1]	---	0.9	---	1.1	PATH
Fpa_pixel[2]	---	0.9	---	1.0	PATH
Fpa_pixel[3]	---	1.2	---	0.8	PATH
Fpa_pixel[4]	---	1.3	---	0.7	PATH
Fpa_pixel[5]	---	1.2	---	0.8	PATH
Fpa_pixel[6]	---	1.4	---	0.6	PATH
Fpa_pixel[7]	---	1.4	---	0.6	PATH
Fpa_pixel[8]	---	1.6	---	0.4	PATH
Fpa_pixel[9]	---	1.5	---	0.5	PATH
Host_addr[0]	13.3	---	-2.7	---	PATH
Host_addr[1]	28.7	36.8	-2.4	-12.7	PATH
Host_addr[2]	25.6	28.3	-2.4	-11.5	PATH
Host_addr[3]	19.8	18.0	-2.4	-6.4	PATH
Host_addr[4]	16.0	13.0	-2.4	-4.6	PATH
Host_data[0]	15.2	---	-3.9	---	PATH
Host_data[10]	9.8	---	-3.1	---	PATH
Host_data[11]	9.7	---	-3.0	---	PATH
Host_data[12]	9.5	---	-3.0	---	PATH
Host_data[13]	9.4	---	-2.7	---	PATH
Host_data[14]	9.6	---	-2.9	---	PATH
Host_data[15]	9.3	---	-2.7	---	PATH
Host_data[1]	14.7	---	-3.7	---	PATH
Host_data[2]	12.8	---	-3.5	---	PATH
Host_data[3]	10.3	---	-3.6	---	PATH
Host_data[4]	10.1	---	-3.2	---	PATH
Host_data[5]	10.0	---	-3.3	---	PATH
Host_data[6]	10.1	---	-3.1	---	PATH

Host_data[7]	10.0	---	-3.2	---	PATH
Host_data[8]	10.0	---	-3.1	---	PATH
Host_data[9]	9.8	---	-3.1	---	PATH
Mem_data[0]	---	3.7	---	-0.1	PATH
Mem_data[10]	---	2.6	---	1.1	PATH
Mem_data[11]	---	2.6	---	1.1	PATH
Mem_data[12]	---	2.8	---	0.8	PATH
Mem_data[13]	---	2.7	---	0.9	PATH
Mem_data[14]	---	2.7	---	1.0	PATH
Mem_data[15]	---	3.1	---	0.6	PATH
Mem_data[1]	---	3.8	---	-0.2	PATH
Mem_data[2]	---	3.6	---	0.1	PATH
Mem_data[3]	---	3.7	---	-0.0	PATH
Mem_data[4]	---	3.3	---	0.3	PATH
Mem_data[5]	---	2.9	---	0.7	PATH
Mem_data[6]	---	3.2	---	0.4	PATH
Mem_data[7]	---	2.7	---	1.0	PATH
Mem_data[8]	---	3.2	---	0.4	PATH
Mem_data[9]	---	2.5	---	1.1	PATH
N_reset	6.9	8.9	-5.0	-4.4	PATH
Ode	27.0	---	-0.5	---	PATH
Pixel_clk_in	---	-3.2	---	4.7	PATH

```
*****  
          3  Genesil Version v8.0.3 -- Thu May 30 14:26:23 1991  
Chip: /mntb/nuc/nuc/gt_nuc/nuc  
          Timing Analyzer  
*****  
VIOLATION MODE  
-----  
Fabline: HP2_CN10B-----Corner: TYPICAL  
Junction Temperature:113 deg C      Voltage:4.50v  
External Clock: Clk_in  
Included setup files:  
#0  reg_worst      (Jn temp 113, 4.5V Power=1.07W)  
-----  
----- NO VIOLATIONS  
Hold time check margin: 2.0ns
```

## Appendix A DV Checklist

# DV CHECKLIST

1. DV CONTROL NUMBER : \_\_\_\_\_

## 2. CUSTOMER INFORMATION

Customer Name : Georgia Tech / CERL Chip Name : GT-VNUC

Address : 400 Tenth Street FAX : (404) 894-3120

CRB Room 377

Atlanta, GA 30332-0540

Project Manager : Dr. C. O. Alford Phone : (404) 894-2505

Design Engineer : Toshiro Kubota Phone : (404) 894-2506

\_\_\_\_\_ Phone : \_\_\_\_\_

Test Engineer : Joseph I. Chamdani Phone : (404) 894-2527

## 3. SERVICES INFORMATION

Design Verification Service only. PO # \_\_\_\_\_

\_\_\_\_\_ Prototype Service and Design Verification. PO # \_\_\_\_\_

\_\_\_\_\_ 1.8% Maintenance

\_\_\_\_\_ SCS Test \_\_\_\_\_ Foundry Test \_\_\_\_\_ Customer Test

When DV is complete, send verified physical database tape to

Customer  N Silicon Vendor  N

4. DV CONTACT : Wallace Wai Phone : (408) 371-2900

## 5. REGRESSION

- 5.1. GENESIL Version : 8.0.3  
5.2. Name of Session Log from recompile : rebuild.LOG  
5.3. Include DV regression.CMD : DV regression.001 (simulation and timing)  
5.4. Size of database (MB) : 242 Guess     Density : 6250     1600     TK50      
Tar xx wbak     Apollo Cartridge      
(compressed) Sun Cartridge xx

## 6. FUNCTIONAL INFORMATION (check when included)

- 6.1. Number of Transistors :      
6.2. Key Parameters : xx Testing      
6.3. DV pin description : xx Testing      
6.4. Block Diagram : xx Testing      
6.5. Functional Description : xx Testing      
6.6. Timing Diagrams at Pins :     Testing      
6.7. Annotated Views : xx Testing     Annotated Schematics : xx Testing      
6.8. Chip Text Specification on tape : xx Density: 6250     1600     TK50      
(nuc.012) Apollo Cartridge      
Sun Cartridge xx

## 7. PHYSICAL INFORMATION

- 7.1. Fabline Name : HP2 CN10B  
Customer-Specific : Y N Fabline GENECAL Directory on tape : Y N  
Fabline GENESIL Directory on tape : Y N  
Fabline Calibration Status : Production : xx Beta :     Alpha :      
NOTE: If not a production fabline, then approval from SCS is required.
- 7.2. Plots: (check when included or indicate filename)  
Chip Route (D size) : xx Bonding Diagram (B size) : xx  
Route Filename : route d.031 Bonding Filename : bond b.031
- 7.3. Die Size : Reported Die Size : 403.2 x 399.2 square-mils  
Maximum Acceptable Die Size (+/- 2%) : 432 x 432 square-mils  
Minimum Acceptable Die Size (+/- 2%) : 272 x 272 square-mils
- 7.4. GENESIL Package Name : CPGA180f Spec included? Y N  
Cavity/Well Size : 472 mils by 472 mils  
Non-GENESIL Supplied Package? Y N Text Spec included on tape? Y N  
Vendor Name/Part # : KYOCERA KD-84143A Foundry Approval? Y N
- 7.5. External Block: none
- 7.6. LRAM: Y N LROM: Y N LPLA: Y N LogicCompiler Blocks: Y N
- 7.7. Test Pad (PM Pad) is included? Y N (Required for PS)

7.8. Power Pad : VCC: Core 1 VSS: Core 1  
Ring 11 Ring 11

NP protection for nwell pad? Y N

TTL output pads or N Protection for inputs? Y N  
If yes, have you received silicon vendor approval? Y N

Error in PADRING.033 (PADRING.DRC)? Y N Hardcopy attached? Y N

ESD requirements \_\_\_\_\_ Approved by SCS? Y N

### 8. ELECTRICAL INFORMATION

- 8.1. Chip Frequency Specified in netlist : 10 MHz Target frequency : 6.67MHz  
8.2. Power Dissipation: GENESIL = 1.07 W at 10 MHz Spec = \_\_\_\_\_ W at \_\_\_\_\_ MHz  
8.3. Operating Voltage: from 4.5 Volts to 5.5 Volts

### 9. SIMULATION

9.1. Number of Clocking Regimes : 1

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	<u>clk pad</u>	<u>NO DIV</u>	<u>Clk in</u>	<u>PHASE A / PHASE B</u>
2.	_____	_____	_____	_____
3.	_____	_____	_____	_____
4.	_____	_____	_____	_____
5.	_____	_____	_____	_____

9.2. Simulation Setup Files:

Name : none / default Listings attached : \_\_\_\_\_

Description : \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
Affected Tests : \_\_\_\_\_

9.3. Test Vector Set:

Total No. of Vectors : 37667

NOTE : Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz. Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name : cal int n tr083 No of vectors : 575

Description : tests register files in pre\_div

Portions of Chip Tested : pre\_div/reg\_file

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

2. Name : cal out tr.083 No of vectors : 102  
 Description : tests an adder in pre\_div/cal\_out\_sub  
 Portions of Chip Tested : pre\_div/cal\_out\_sub  
 -  
 Pass with GFL model? yes  
 Pass with GSL model? yes Use for PS testing? Y N  
 Pass Fight Test? yes
3. Name : cal out2 tr.083 No of vectors : 102  
 Description : tests an adder in pre\_div/cal\_out\_sub  
 Portions of Chip Tested : pre\_div/cal\_out\_sub  
 Pass with GFL model? yes  
 Pass with GSL model? yes Use for PS testing? Y N  
 Pass Fight Test? yes
4. Name : calibration tr.083 No of vectors : 504  
 Description : tests the calibration mode with a short address format  
 Portions of Chip Tested : all  
 Pass with GFL model? yes  
 Pass with GSL model? yes Use for PS testing? Y N  
 Pass Fight Test? yes
5. Name : calibration2 tr.083 No of vectors : 504  
 Description : tests the calibration mode with a long address format  
 Portions of Chip Tested : all  
 Pass with GFL model? yes  
 Pass with GSL model? yes Use for PS testing? Y N  
 Pass Fight Test? yes
6. Name : div tr.083 No of vectors : 892  
 Description : tests the divider  
 Portions of Chip Tested : divider  
 Pass with GFL model? yes  
 Pass with GSL model? yes Use for PS testing? Y N  
 Pass Fight Test? yes
7. Name : div2 tr.083 No of vectors : 732  
 Description : tests the divider using its scan out feature  
 Portions of Chip Tested : divider

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

8. Name : div3.083 No of vectors : 2820

Description : tests the divider using its scan out feature

Portions of Chip Tested : divider

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

9. Name : div4.083 No of vectors : 2820

Description : tests the divider using its scan out feature

Portions of Chip Tested : divider

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

10. Name : div5.083 No of vectors : 2820

Description : tests the divider using its scan out feature

Portions of Chip Tested : divider

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

11. Name : div6.083 No of vectors : 2820

Description : tests the divider using its scan out feature

Portions of Chip Tested : divider

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

12. Name : ext add tr.083 No of vectors : 206

Description : tests the adder following the multiplier in pre\_div/mult

Portions of Chip Tested : pre\_div/mult

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

13. Name : ext add cin tr.083 No of vectors : 206

Description : tests the adder following the multiplier in pre\_div/mult

Portions of Chip Tested : pre div/mult

Pass with GFL model? yes  
Pass with GSL model? yes      Use for PS testing? Y N  
Pass Fight Test? yes

14.Name : extern\_ram1 tr.083      No of vectors : 746  
Description : tests the overall functionality (calibration and compensation) of the first order linear approximation in conjunction with external RAMs

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes      Use for PS testing? Y N  
Pass Fight Test? yes

15.Name : extern\_ram2 tr.083      No of vectors : 874  
Description : tests the overall functionality (calibration and compensation) of the second order linear approximation in conjunction with external RAMs

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes      Use for PS testing? Y N  
Pass Fight Test? yes

16.Name : extern\_ram3 tr.083      No of vectors : 1010  
Description : tests the overall functionality (calibration and compensation) of the third order linear approximation in conjunction with external RAMs

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes      Use for PS testing? Y N  
Pass Fight Test? yes

17.Name : extern\_ram4 tr.083      No of vectors : 1130  
Description : tests the overall functionality (calibration and compensation) of the fourth order linear approximation in conjunction with external RAMs.

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes      Use for PS testing? Y N  
Pass Fight Test? yes

18.Name : extern\_ram1b tr.083      No of vectors : 834  
Description : tests the overall functionality (calibration and compensation) of the first order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

19.Name : extern\_ram2b\_tr.083 No of vectors : 994

Description : tests the overall functionality (calibration and compensation) of the second order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

20.Name : extern\_ram3b\_tr.083 No of vectors : 1154

Description : tests the overall functionality (calibration and compensation) of the third order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

21.Name : extern\_ram4b\_tr.083 No of vectors : 1314

Description : tests the overall functionality (calibration and compensation) of the forth order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

22.Name : extern\_ram1c\_tr.083 No of vectors : 994

Description : tests the overall functionality (calibration and compensation) of the first order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

23.Name : extern\_ram2c\_tr.083 No of vectors : 1154

Description : tests the overall functionality (calibration and compensation) of the second order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

24.Name : extern ram3c tr.083 No of vectors : 1314

Description : tests the overall functionality (calibration and compensation) of the third order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

25.Name : extern ram4c tr.083 No of vectors : 1474

Description : tests the overall functionality (calibration and compensation) of the forth order linear approximation in conjunction with external RAMs. Bad pixels and dead pixels are included.

Portions of Chip Tested : all

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

26.Name : fadd tr.083 No of vectors : 310

Description : tests the final adder in the *pre\_div/mult*

Portions of Chip Tested : *pre\_div/mult*

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

27.Name : frame shift tr.083 No of vectors : 740

Description : tests the *frame\_sync*

Portions of Chip Tested : *frame\_sync*

Pass with GFL model? yes

Pass with GSL model? yes

Pass Fight Test? yes

Use for PS testing? Y N

28.Name : host mem wr tr.083 No of vectors : 184

Description : tests the capability of the host to write/read data to/from the external RAM.

Portions of Chip Tested : memory-to-host interface

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

29.Name : host mem wr2 tr.083 No of vectors : 184  
Description : tests the capability of the host to write/read data to/from the external RAM.  
Portions of Chip Tested : memory-to-host interface

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

30.Name : int\_sub tr.083 No of vectors : 102  
Description : tests the adder in pre\_div/int\_sub  
Portions of Chip Tested : pre\_div/int\_sub

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

31.Name : mult tr.083 No of vectors : 2438  
Description : tests the multiplier in pre\_div/mult  
Portions of Chip Tested : pre\_div/mult

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

32.Name : mathnew tr.083 No of vectors : 332  
Description : tests the functionality of the forth order compensation with bad pixels and dead pixels  
Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

33.Name : new tr.083 No of vectors : 360  
Description : tests the functionality of the forth order compensation with bad pixels and dead pixels  
Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

34.Name : new clk tr.083 No of vectors : 360  
Description : tests the functionality of the forth order compensation with bad pixels and dead pixels  
Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

35.Name : nuc tr.083 No of vectors : 330  
Description : tests the functionality of the forth order compensation with bad pixels and dead pixels

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

36.Name : order1 tr.083 No of vectors : 358  
Description : tests the functionality of the 1st order compensation with bad pixels and dead pixels

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

37.Name : order2 tr.083 No of vectors : 358  
Description : tests the functionality of the 2nd order compensation with bad pixels and dead pixels

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

38.Name : order3 tr.083 No of vectors : 358  
Description : tests the functionality of the 3rd order compensation with bad pixels and dead pixels

Portions of Chip Tested : all

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

39.Name : overflow tr.083 No of vectors : 406  
Description : tests the overflow detection module and check if the final result (Pixel\_out) is set to the maximum intensity value.

Portions of Chip Tested : overflow and pixel\_out

Pass with GFL model? yes  
Pass with GSL model? yes Use for PS testing? Y N  
Pass Fight Test? yes

40.Name : pix cal tr.083 No of vectors : 114  
Description : tests the adder in pre\_div/pix\_cal\_sub

Portions of Chip Tested : pre\_div/pix\_cal\_sub

Pass with GFL model? yes  
 Pass with GSL model? yes      Use for PS testing? Y N  
 Pass Fight Test? yes

41. Name : pix\_counter tr.083      No of vectors : 464  
 Description : tests the 16bit and 4bit up counter in pix\_counter.

Portions of Chip Tested : pix\_counter

Pass with GFL model? yes  
 Pass with GSL model? yes      Use for PS testing? Y N  
 Pass Fight Test? yes

42. Name : trans1 tr.083      No of vectors : 968  
 Description : tests the compensation mode with data from the transputer model.

Portions of Chip Tested : all

Pass with GFL model? yes  
 Pass with GSL model? yes      Use for PS testing? Y N  
 Pass Fight Test? yes

43. Name : trans2 tr.083      No of vectors : 968  
 Description : tests the compensation mode with data from the transputer model.

Portions of Chip Tested : all

Pass with GFL model? yes  
 Pass with GSL model? yes      Use for PS testing? Y N  
 Pass Fight Test? yes

44. Name : underflow tr.083      No of vectors : 238  
 Description : tests the underflow detection and check if the final result (Pixel\_out) is set to the least calibration sample intensity.

Portions of Chip Tested : all

Pass with GFL model? yes  
 Pass with GSL model? yes      Use for PS testing? Y N  
 Pass Fight Test? yes

9.4. IMS Grouping within limitation? Y N (Required for PS only)

9.5. Tester clock frequency = 6.67 MHz

9.6. Signals that must be glitch free: Y N

Signal Name	Ran GSL with glitch detection feature on?
1. <u>N mem we</u>	<u>Y</u> N
2. _____	Y N
3. _____	Y N
4. _____	Y N
5. _____	Y N

## 10. TIMING ANALYSIS

### 10.1. System Environment

Temperature Coefficient: 35 Degrees C / Watt (theta JA)  
 Operating Temp : from 0<sup>0</sup> C (min) to 70<sup>0</sup> C (max)  
 Operating Voltage : from 4.5 V (min) to 5.5 V (max)  
 room junction temp = 25 + (theta JA \* Power) = 63 degrees C  
 maximum junction temp = maximum ambient temp + (theta JA \* Power) = 113 degrees C

### 10.2. Reports (Include the following reports)

(required for PS)* guaranteed corner 5.0V room junc temp	(required for PS)* guaranteed corner min operating V max junction temp	typical corner min operating V max junction temp
Cycle : <u>xx</u>	Cycle : <u>xx</u>	Cycle : <u>xx</u>
Setup/Hold : <u>xx</u>	Setup/Hold : <u>xx</u>	Setup/Hold : <u>xx</u>
Output Delay : <u>xx</u>	Output Delay : <u>xx</u>	Output Delay : <u>xx</u>
Violation : <u>xx</u>	Violation : <u>xx</u>	Violation : <u>xx</u>

### 10.3. Timing Setup Files:

Name : reg\_worst.040 Listings attached : yes  
 Temperature : 113 degrees C Voltage : 4.50 V  
 Description : worst case condition, maximum junction temperature, minimum operating voltage

Name : reg\_room.040 Listings attached : yes  
 Temperature : 63 degrees C Voltage : 5.00 V  
 Description : nominal condition, room junction temperature, 5.0 V operating voltage

### 10.4. Critical Boundary Conditions:

List critical paths here or annotate the timing report.  
 Attach additional pages if needed.

Clock Name : Clk\_in

	report	limit (+/-5%)	report	limit (+/-5%)
1. Phase 1 High	<u>55.1 ns</u>	<u>75.0 ns</u>	<u>          </u>	<u>          </u>
2. Phase 2 High	<u>57.2 ns</u>	<u>75.0 ns</u>	<u>          </u>	<u>          </u>
3. Symmetric Cycle	<u>115.8 ns</u>	<u>150.0 ns</u>	<u>          </u>	<u>          </u>
4. Minimum Cycle	<u>115.8 ns</u>	<u>150.0 ns</u>	<u>          </u>	<u>          </u>

#### Outputs

	Signal Name	load (pF)	delay	limit
1.	<u>Mem_addr[22:0]</u>	<u>50.00</u>	<u>23.0 ns</u>	<u>27 ns</u>
2.	<u>Cs16k[4:0]</u>	<u>50.00</u>	<u>22.8 ns</u>	<u>27 ns</u>
3.	<u>Cs32k[2:0]</u>	<u>50.00</u>	<u>22.7 ns</u>	<u>27 ns</u>

4.	_____	_____	_____	_____
5.	_____	_____	_____	_____
6.	_____	_____	_____	_____
7.	_____	_____	_____	_____

Inputs

	Signal Name	setup report / limit	hold report / limit
1.	Mem_data[15:0]	5.8nsec/8.0nsec	/
2.	_____	/	/
3.	_____	/	/
4.	_____	/	/
5.	_____	/	/
6.	_____	/	/
7.	_____	/	/
8.	_____	/	/
9.	_____	/	/

10.5. Hold Time Violations : none (At 2.0 nsec.)

## 11. DC CHARACTERISTICS

PARAMETERS	DESCRIPTION	CONDITIONS 0 to 70	CONDITIONS -55 to +125	MIN	MAX
<b>DATA PAD INPUT ONLY</b>					
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IIL	Input Leakage	VSS < Vin < VDD	VSS < Vin < VDD	-10uA	10uA
CIN	Input Capacitance				6.0pf
<b>DATA PAD OUTPUT ONLY</b>					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
IOZ	Output Leakage current(high Z)	VSS < Vout < VDD	VSS < Vout < VDD	-10uA	10uA
COUT	Output Capacitance				7.0pf
<b>DATA PAD INPUT/OUTPUT</b>					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IOZ	Output leakage current (high Z)	VSS < Vout < VDD	VSS < Vout < VDD	-10uA	10uA
CIO	Input/Output Capacitance				7.0pf
<b>CLOCK PAD</b>					
VIH	Input High Voltage			3.9V	
VIL	Input Low Voltage				0.6V
IIL	Input Leakage	VSS < Vin < VDD	VSS < Vin < VDD	-10uA	10uA
CIN	Input Capacitance				15pf

NOTE: All parameters at a supply voltage of VDD = 5V (+/- 10%).

**12. CUSTOMER COMMENTS**

**Pre-Verification Comments**

COMPILE FORCE BUILD ALL always fails at compile-layout of some logic-compiled blocks or some ndp adders. We believe it is due to some internal faults of genesil since the remaining commands including the one just failed can be done successfully by COMPILE BUILD ALL following immediately after the COMPILE FORCE BUILD ALL has failed. The session log from recompile (rebuild.LOG) contains this two step processes. In the first COMPILE BUILD ALL, COMPILE:LAYOUT at divider1 failed, but in the second COMPILE BUILD ALL, the remaining commands including COMPILE:LAYOUT at divider1 ran successfully.

**13. CUSTOMER APPROVAL**

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : \_\_\_\_\_ Date 5 / 31 / 91

Title : Research Assistant

**14. SCS APPROVAL**

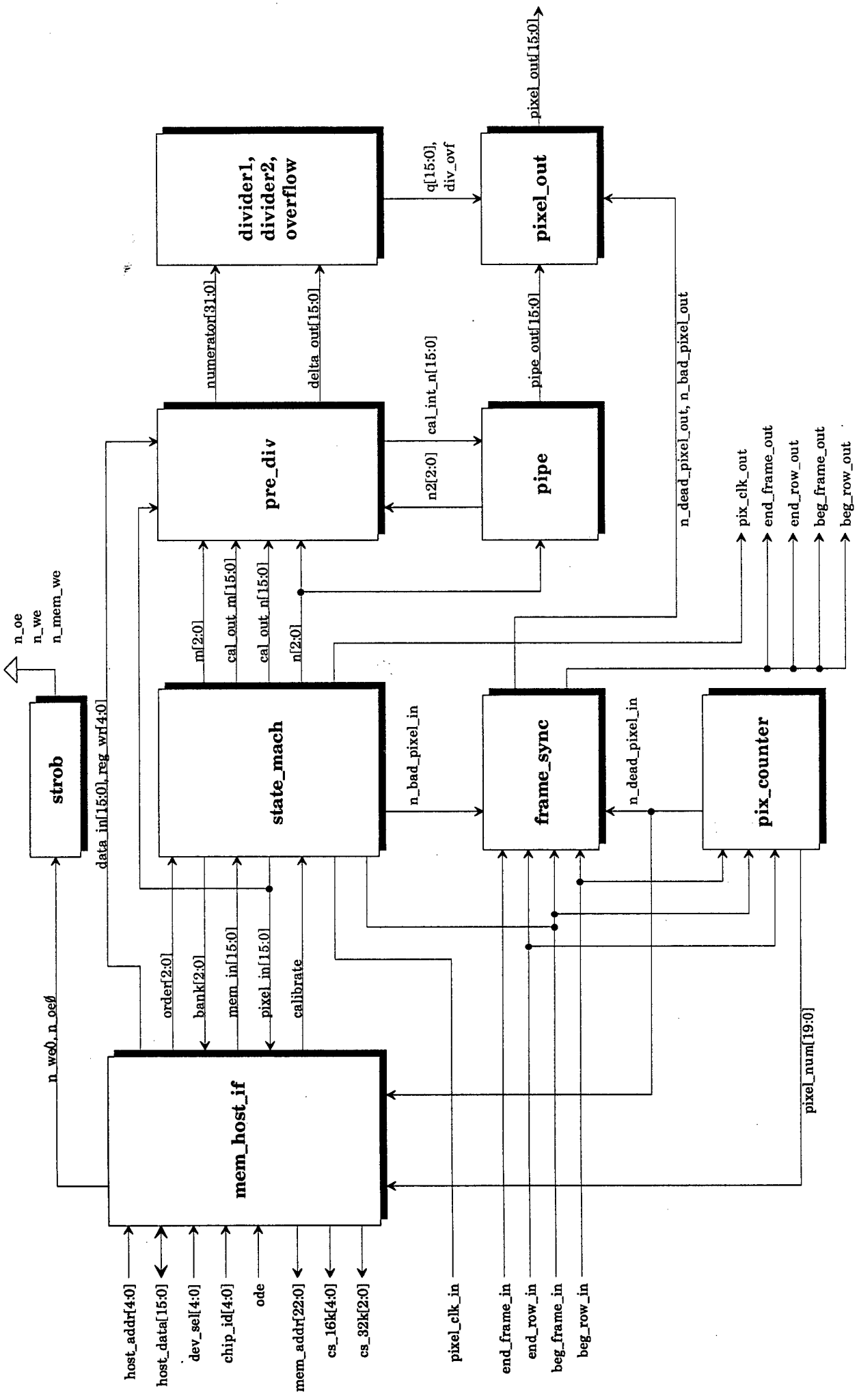
**Pre-Verification Comments**

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

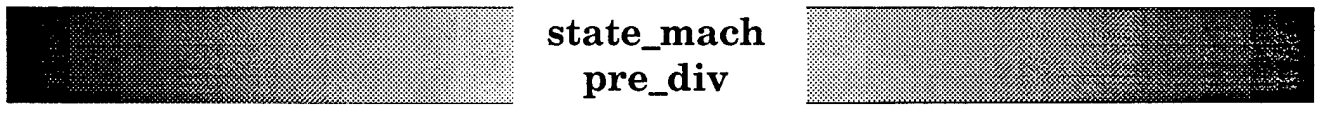
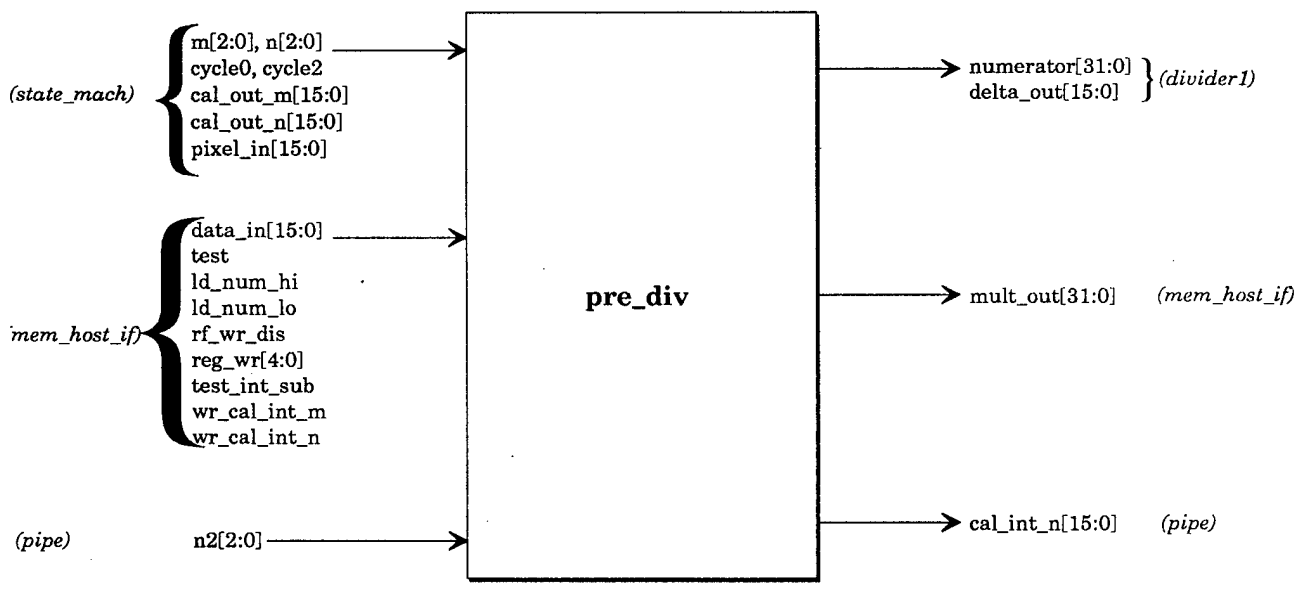
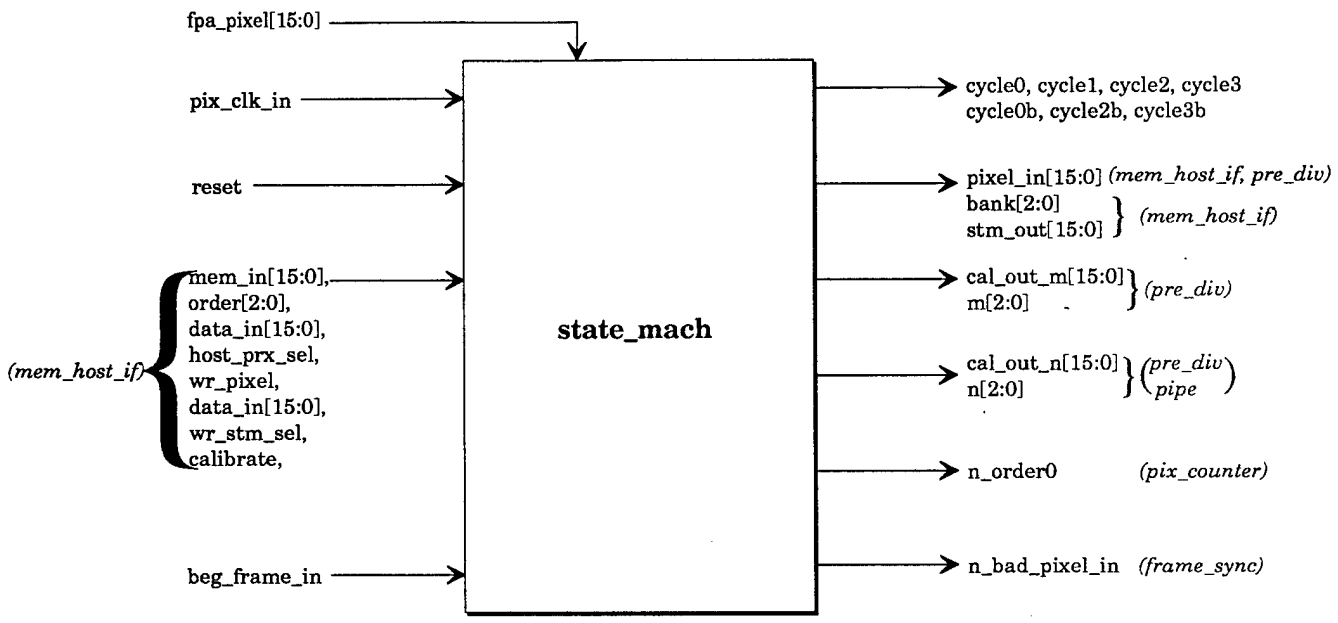
SCS Approval : \_\_\_\_\_ Date \_\_\_\_/\_\_\_\_/\_\_\_\_  
Regional Field Application Consultant

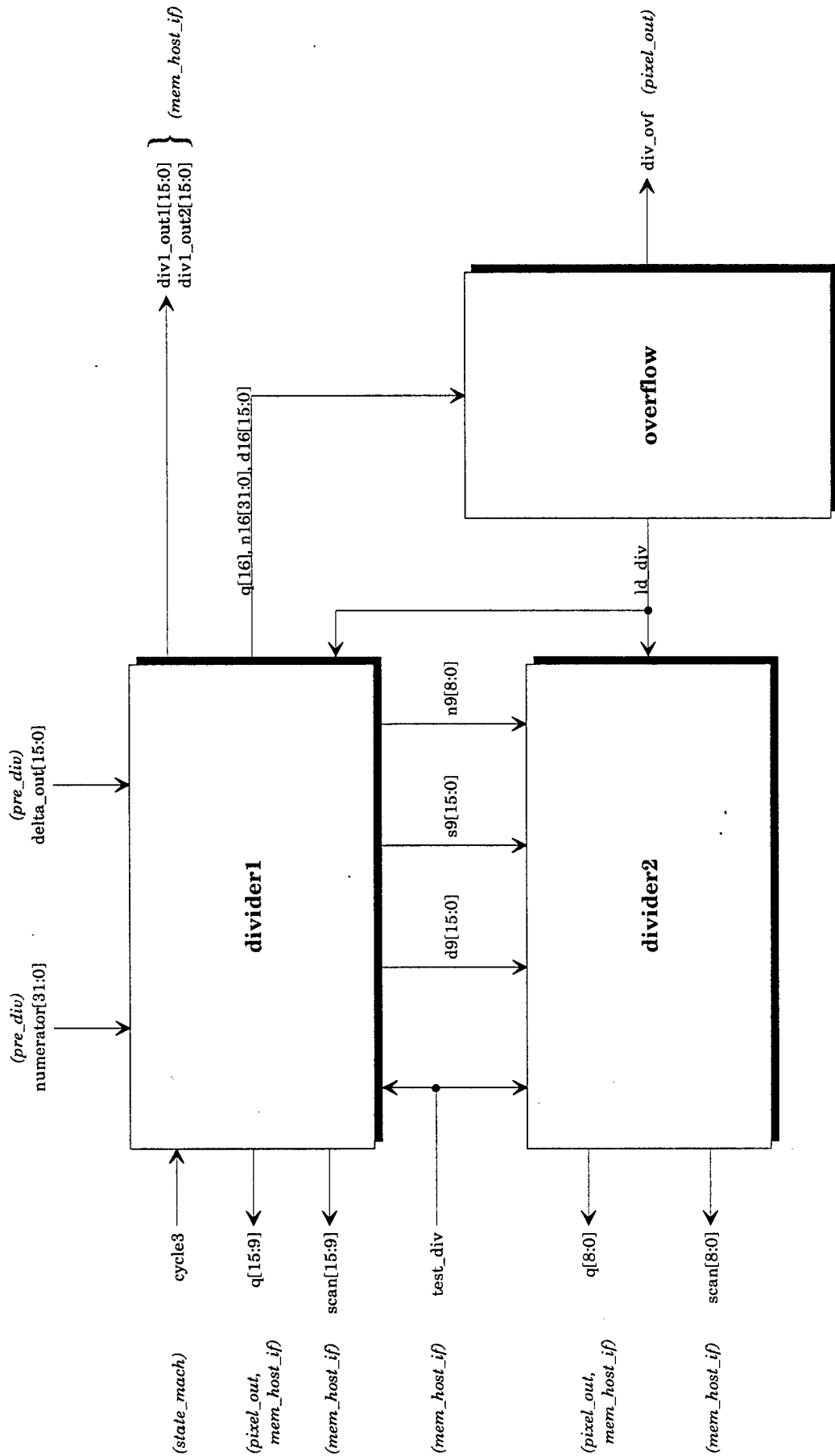
SCS Approval : \_\_\_\_\_ Date \_\_\_\_/\_\_\_\_/\_\_\_\_  
Technical Support Team Leader

## **Appendix B Block Diagrams And Schematics**

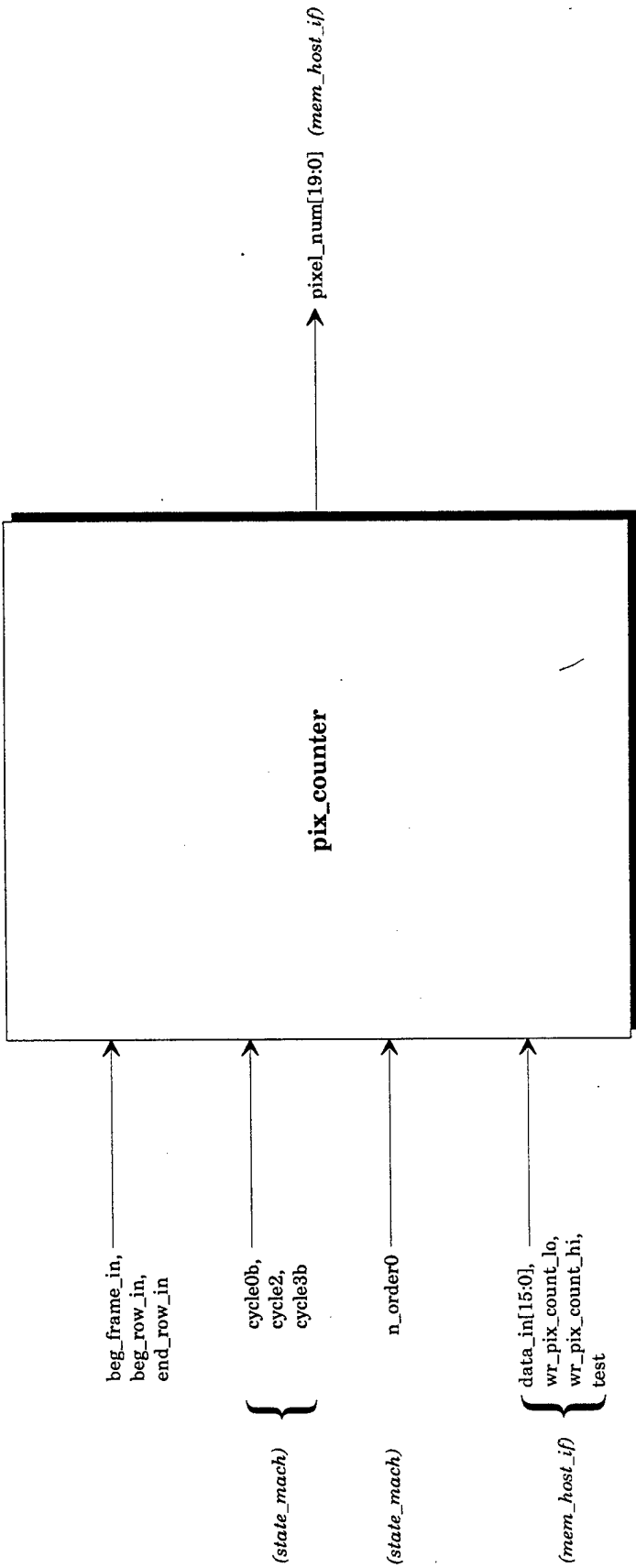


**nuc/math (simplified dataflow)**



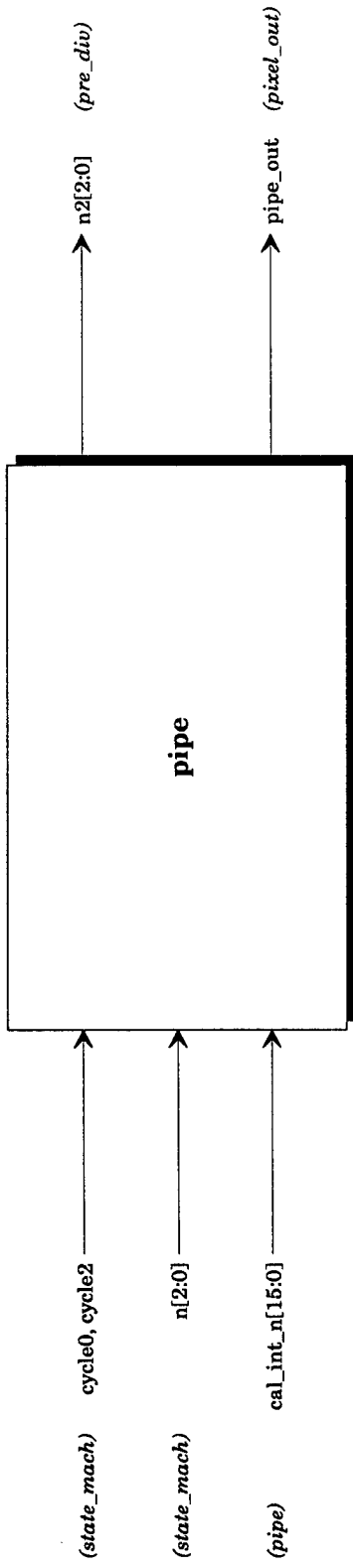


math/divider1  
 math/divider2  
 math/overflow

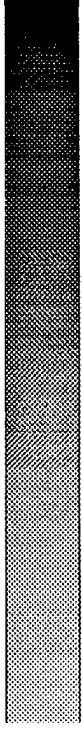
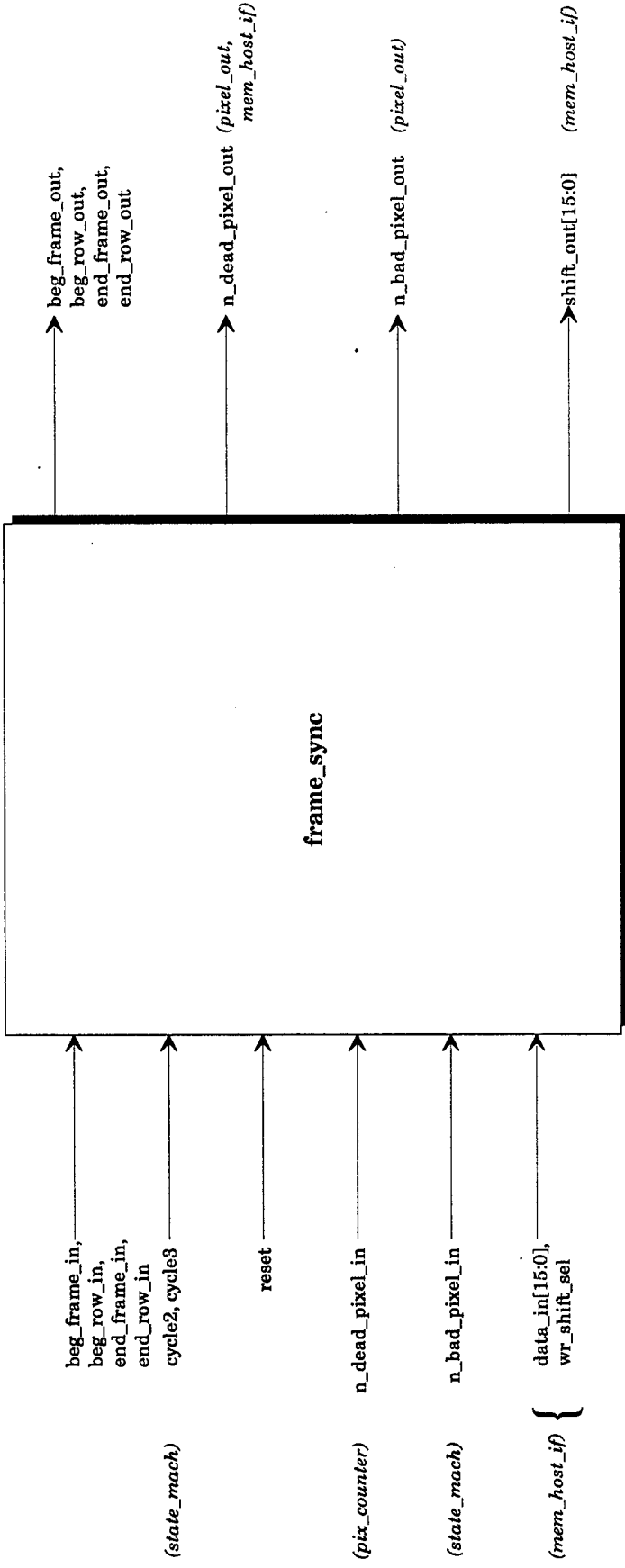


**math/pix\_counter**





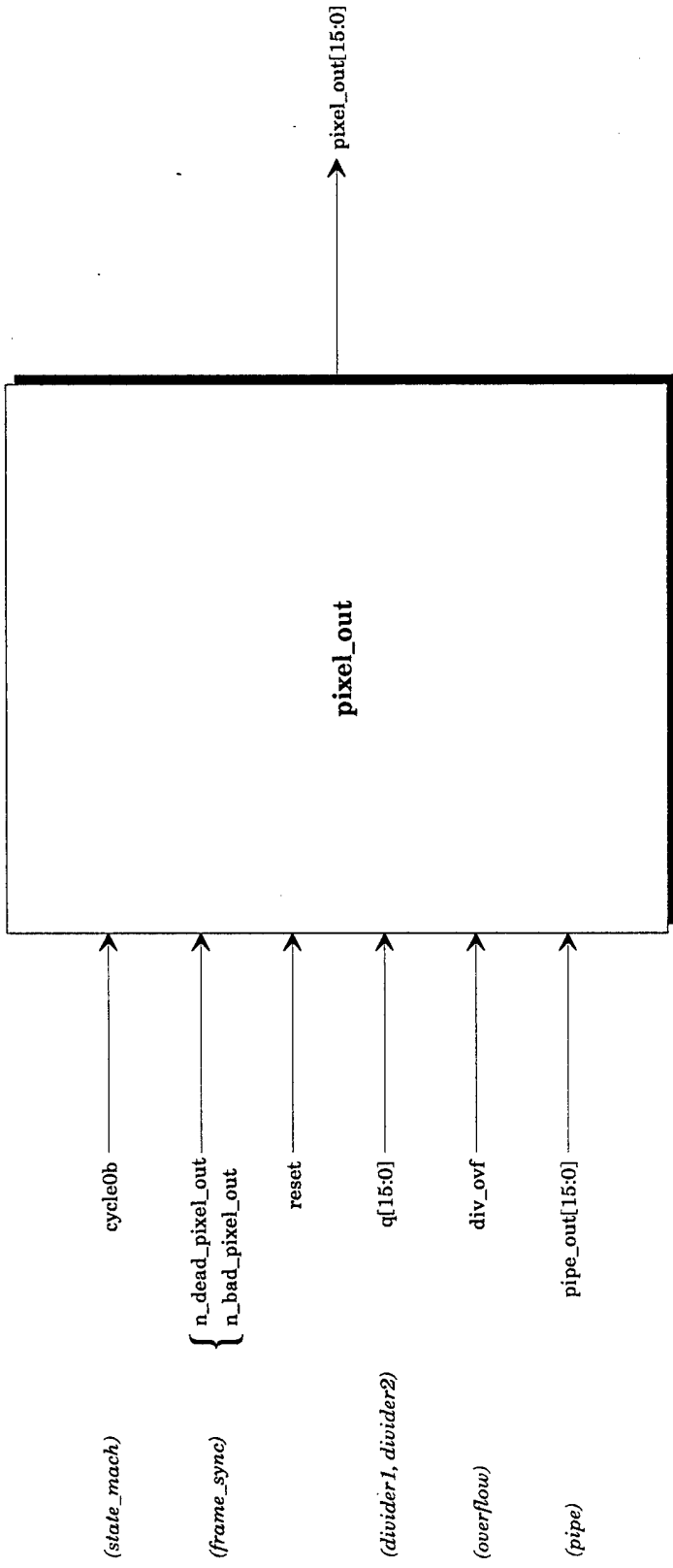
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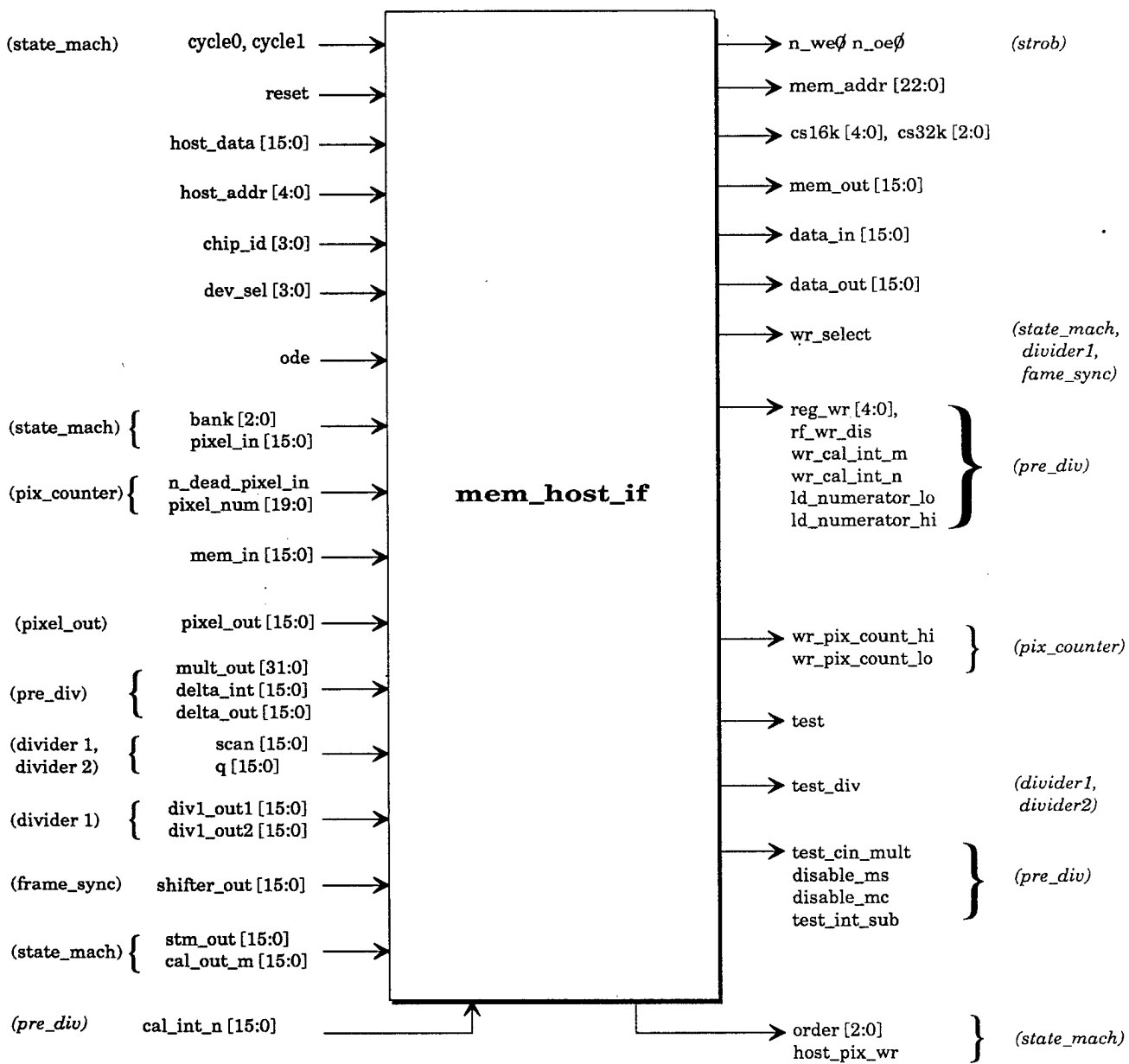
math/frame\_sync



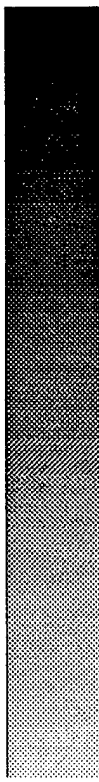
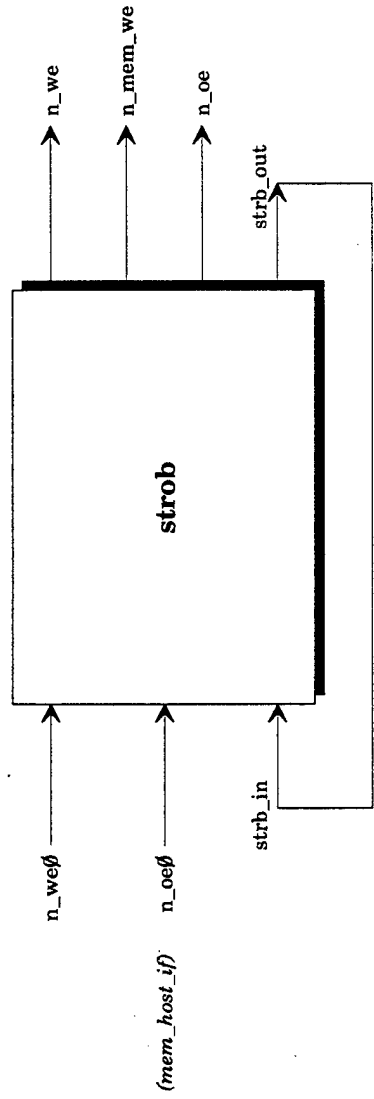
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 Path:   
 Gen: schip



**math/pixel\_out**

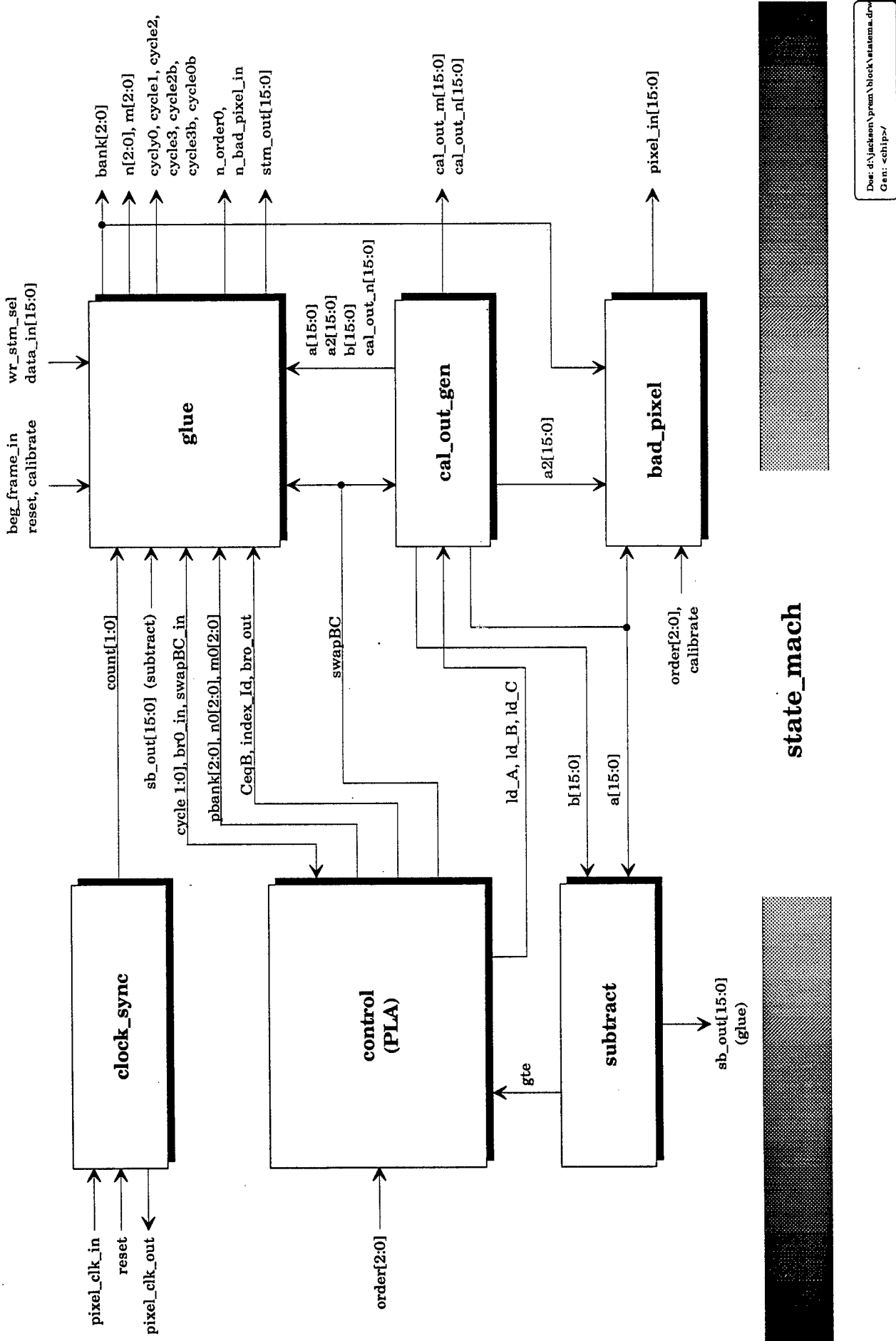


**math/mem\_host\_if**

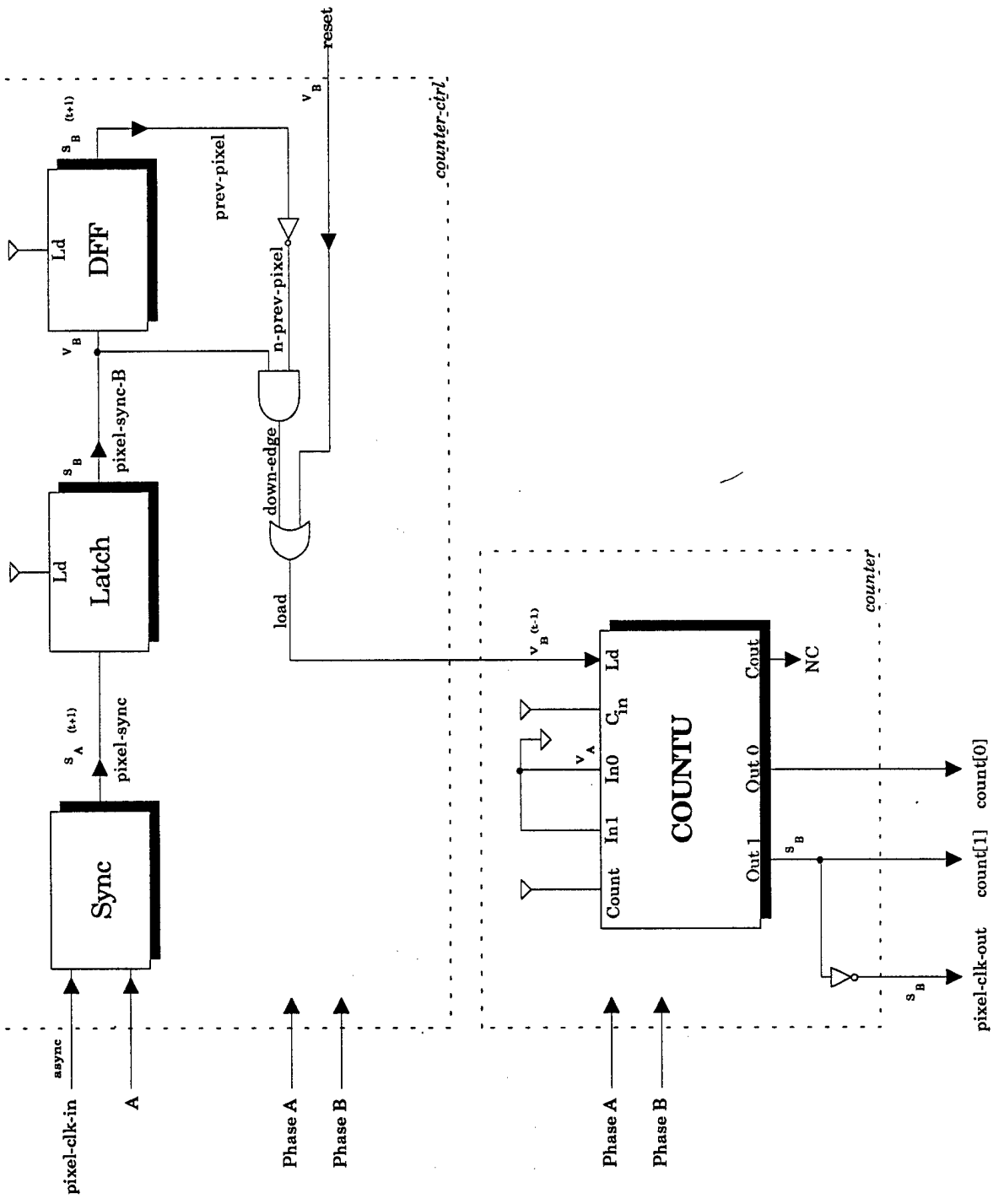


math/strob

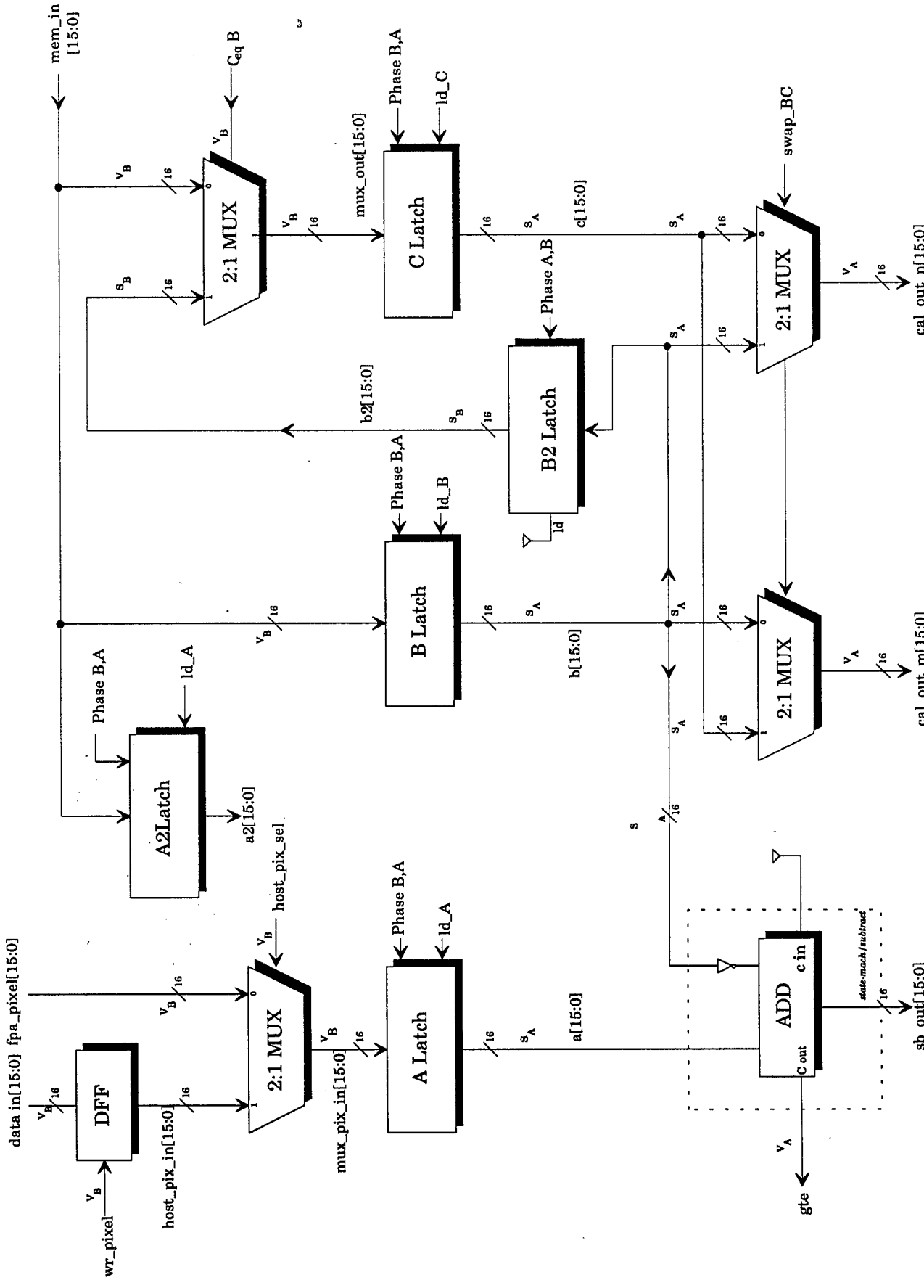




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 Gen: <chip>/

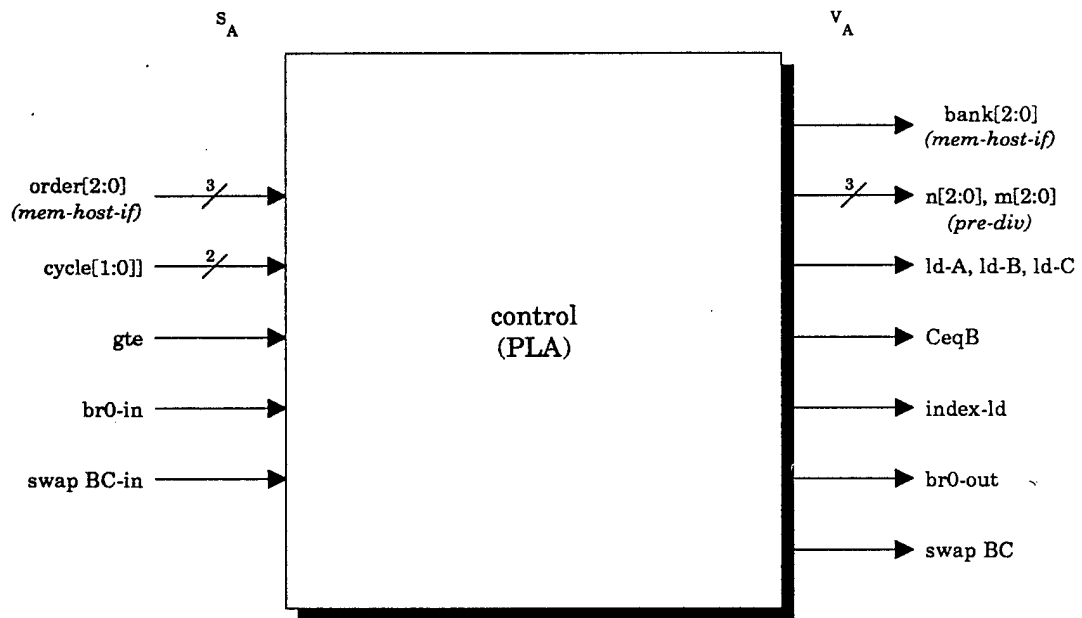


**state-mach/clock-sync**



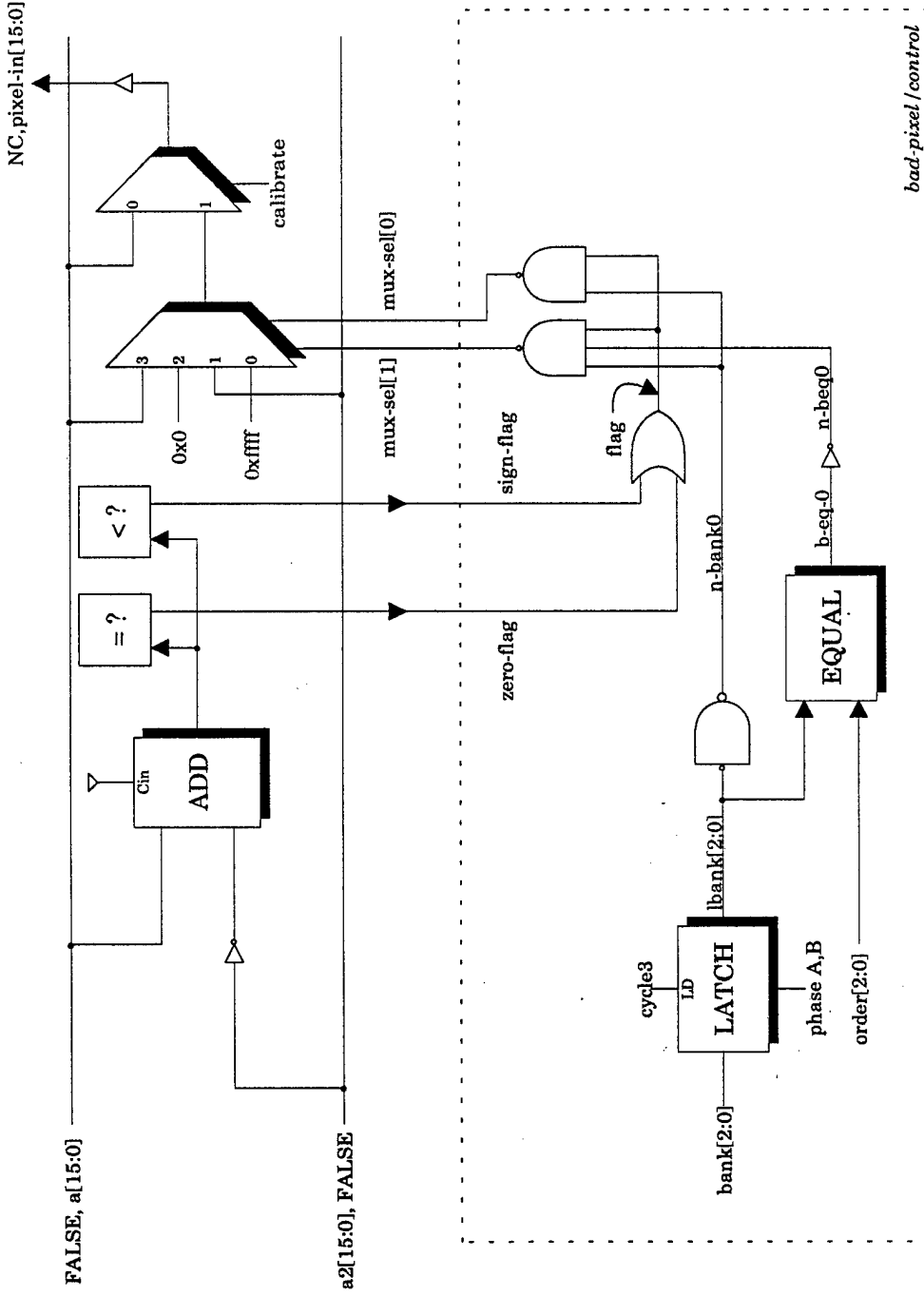
**state-mach/cal\_out\_gen**  
**state-mach/substract**

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math/state-mach/control

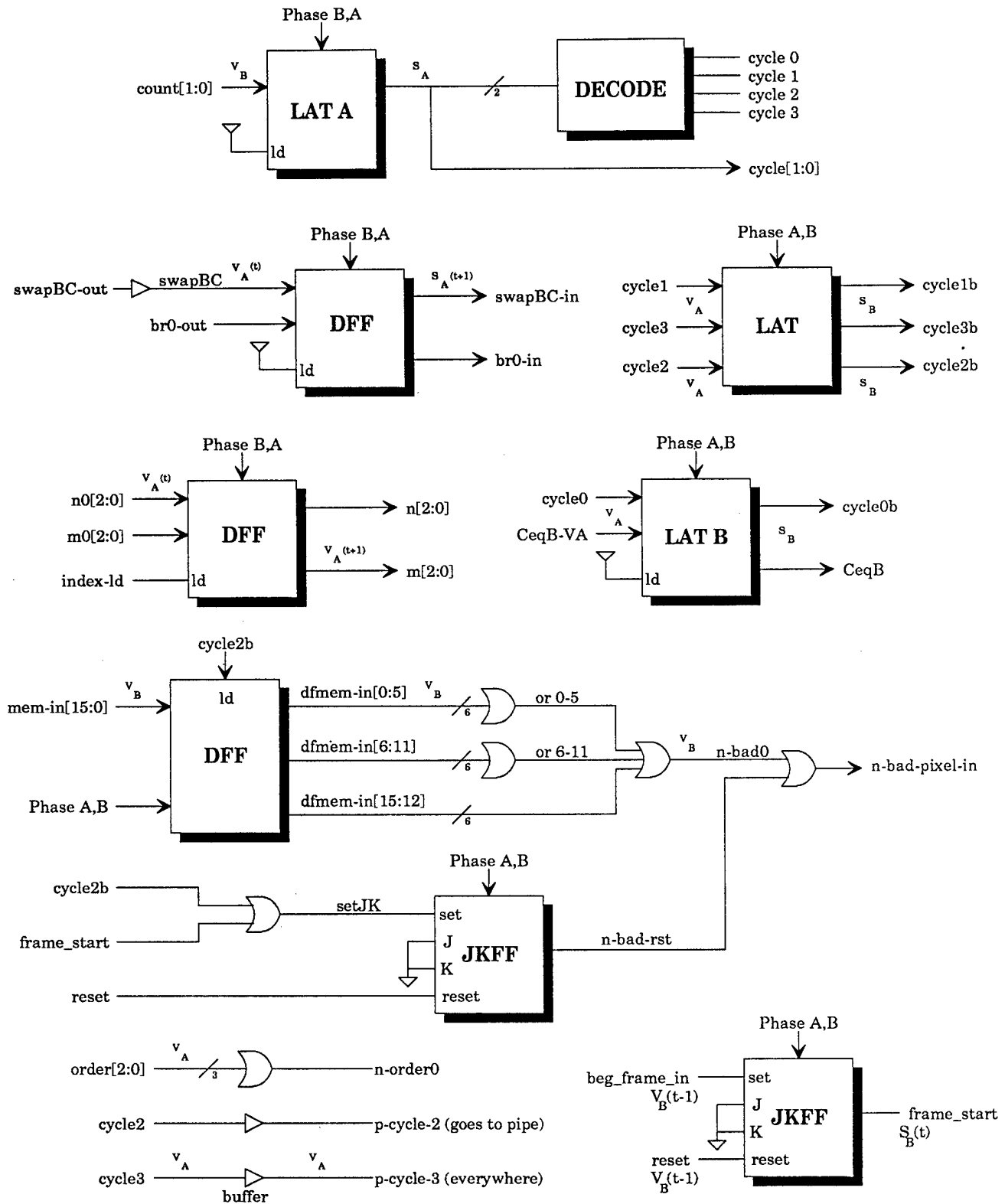
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*bad-pixel/control*

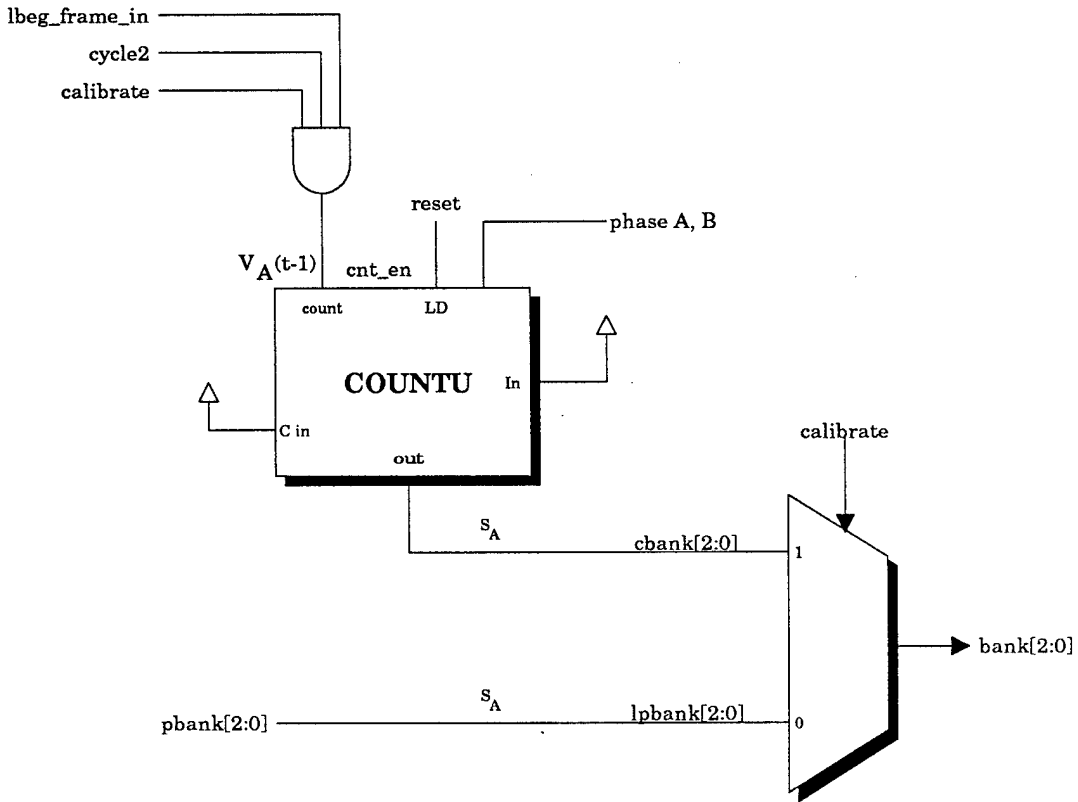
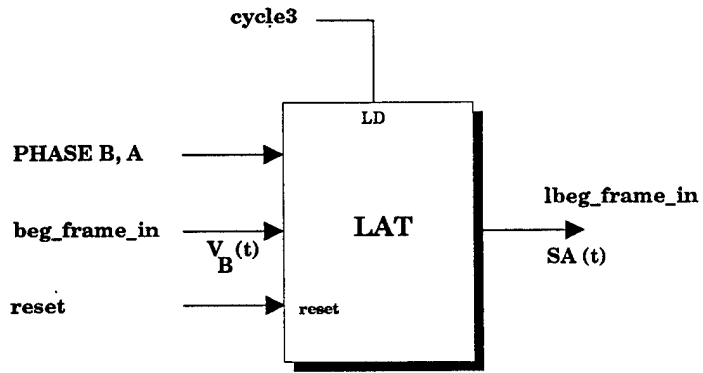
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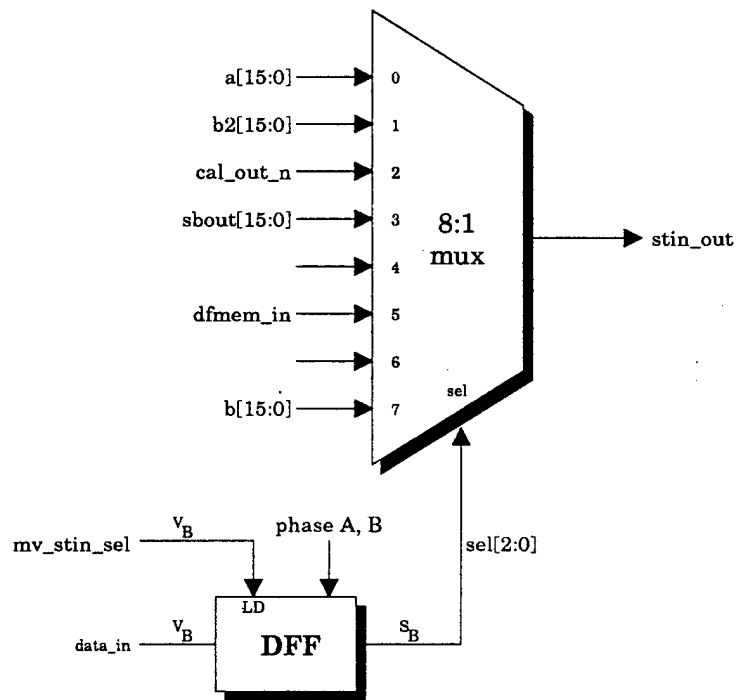


**math/state-mach/glue**

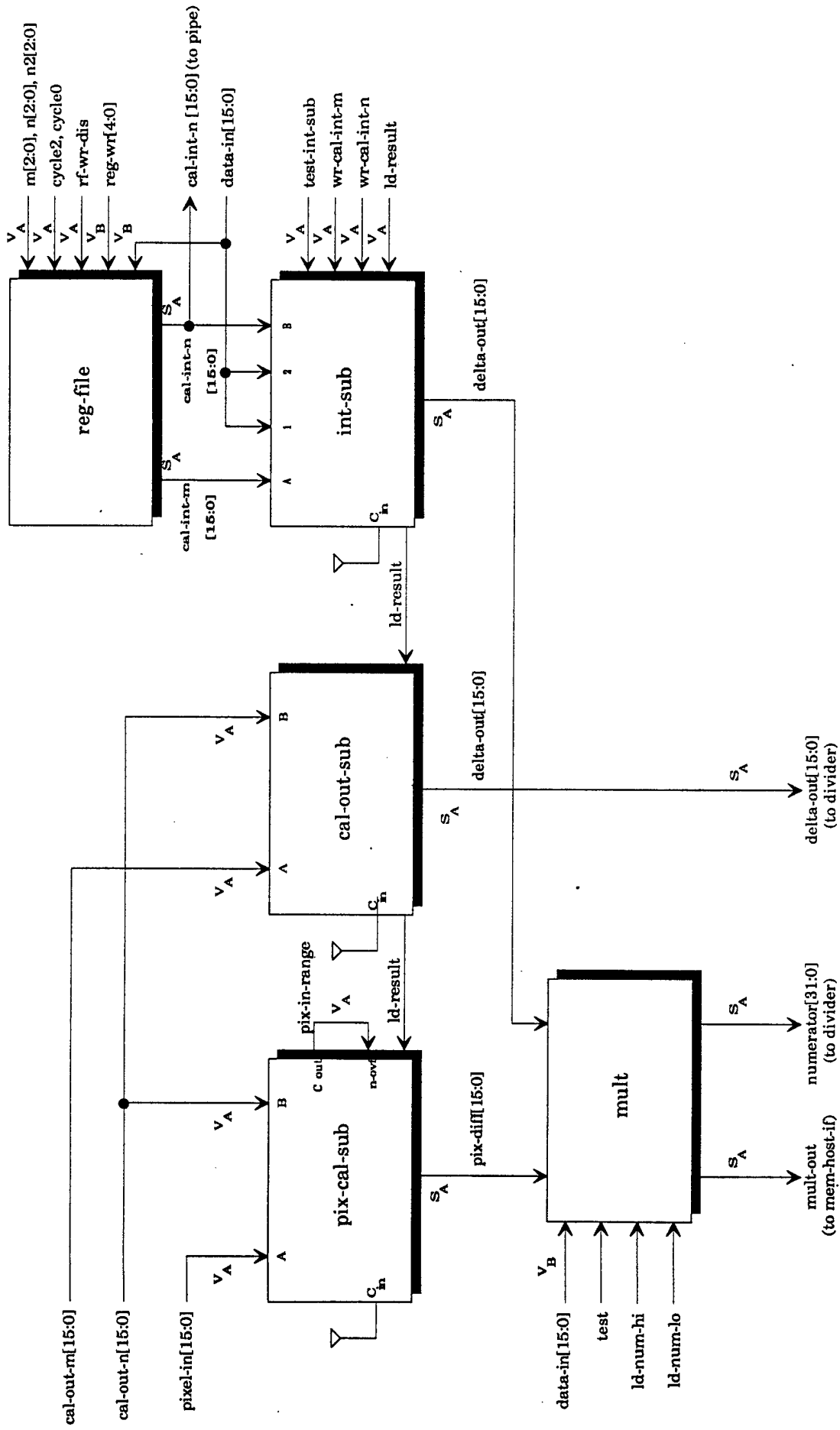
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 <chip>math/state-mach/glue



state\_mach/glue

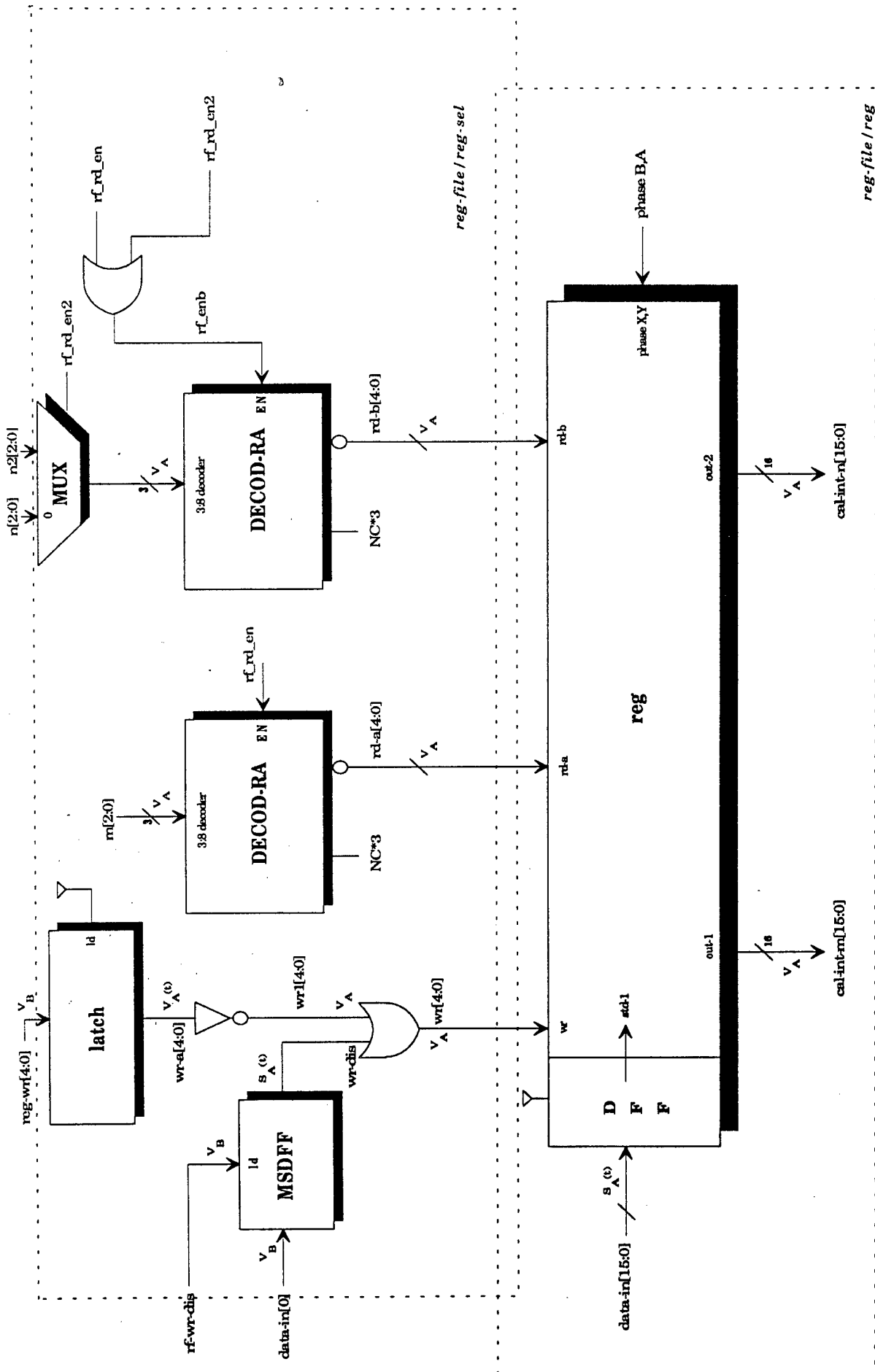


state\_mach/glue



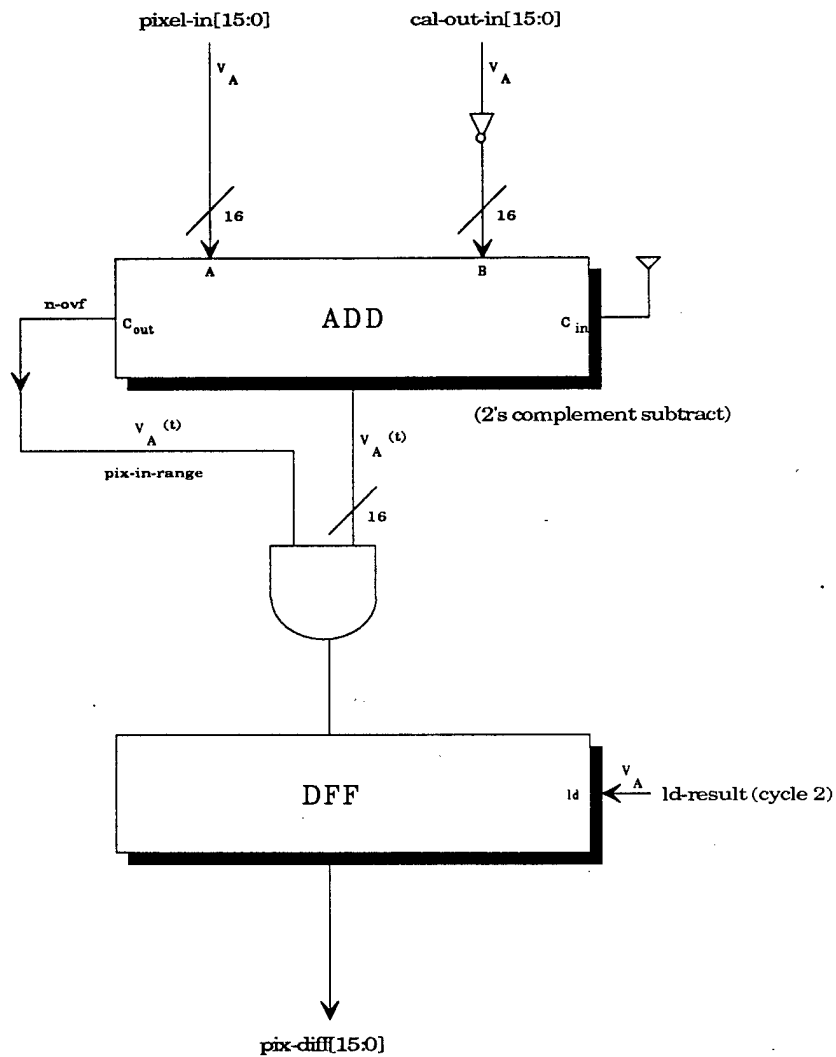
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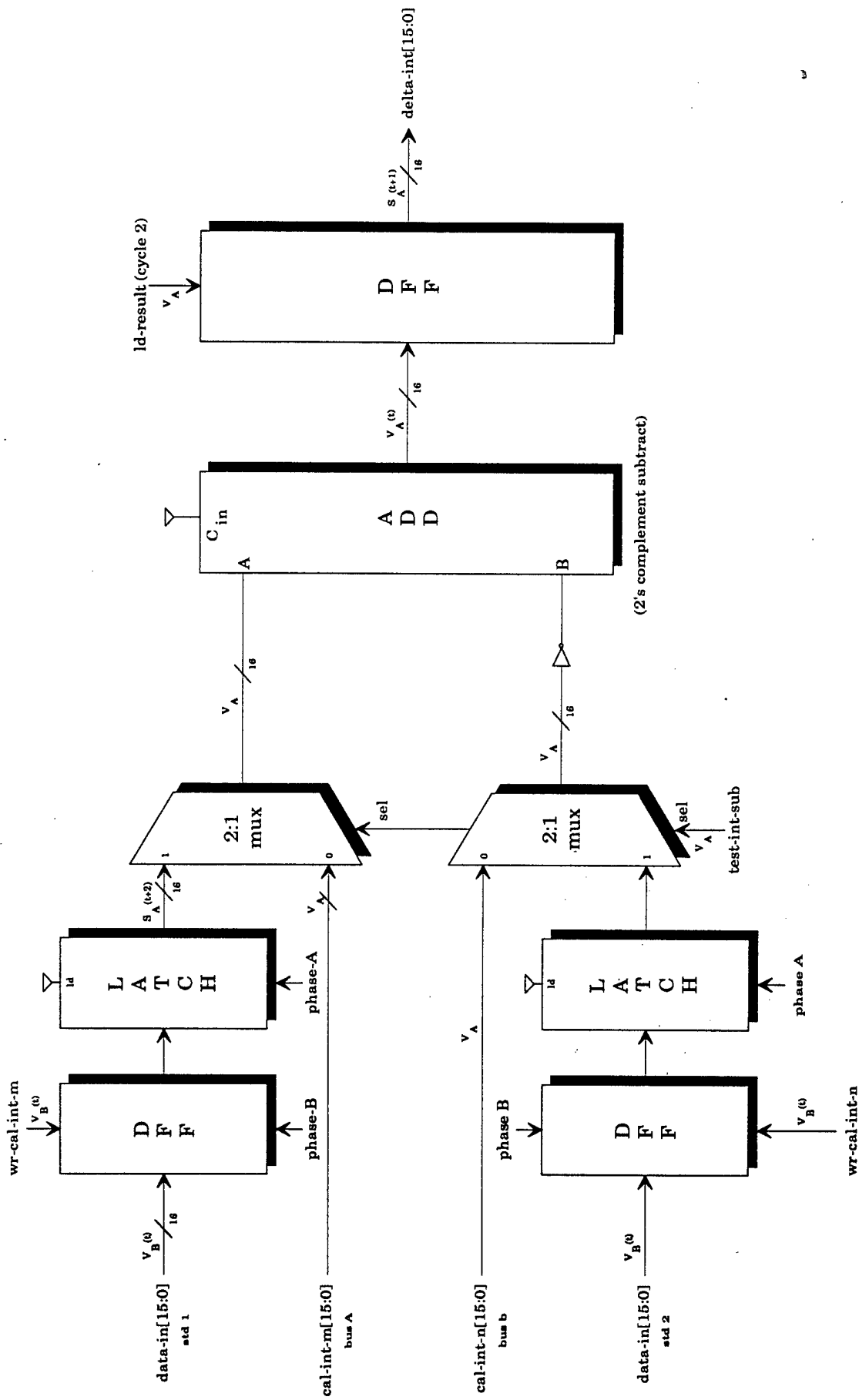
**pre-div/reg-file**

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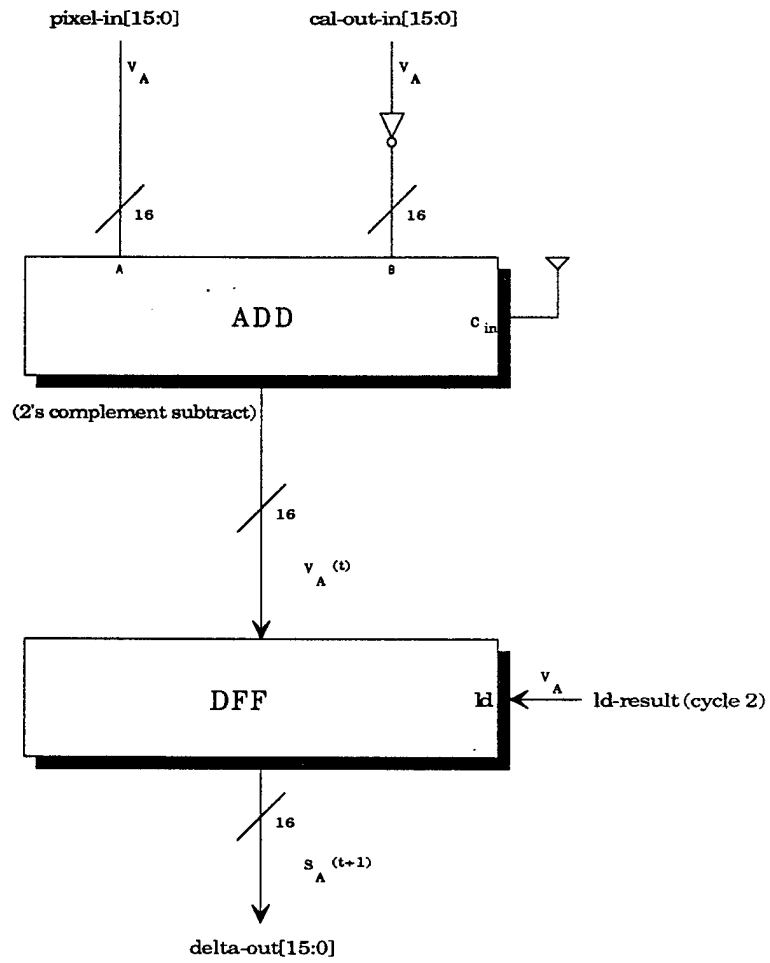
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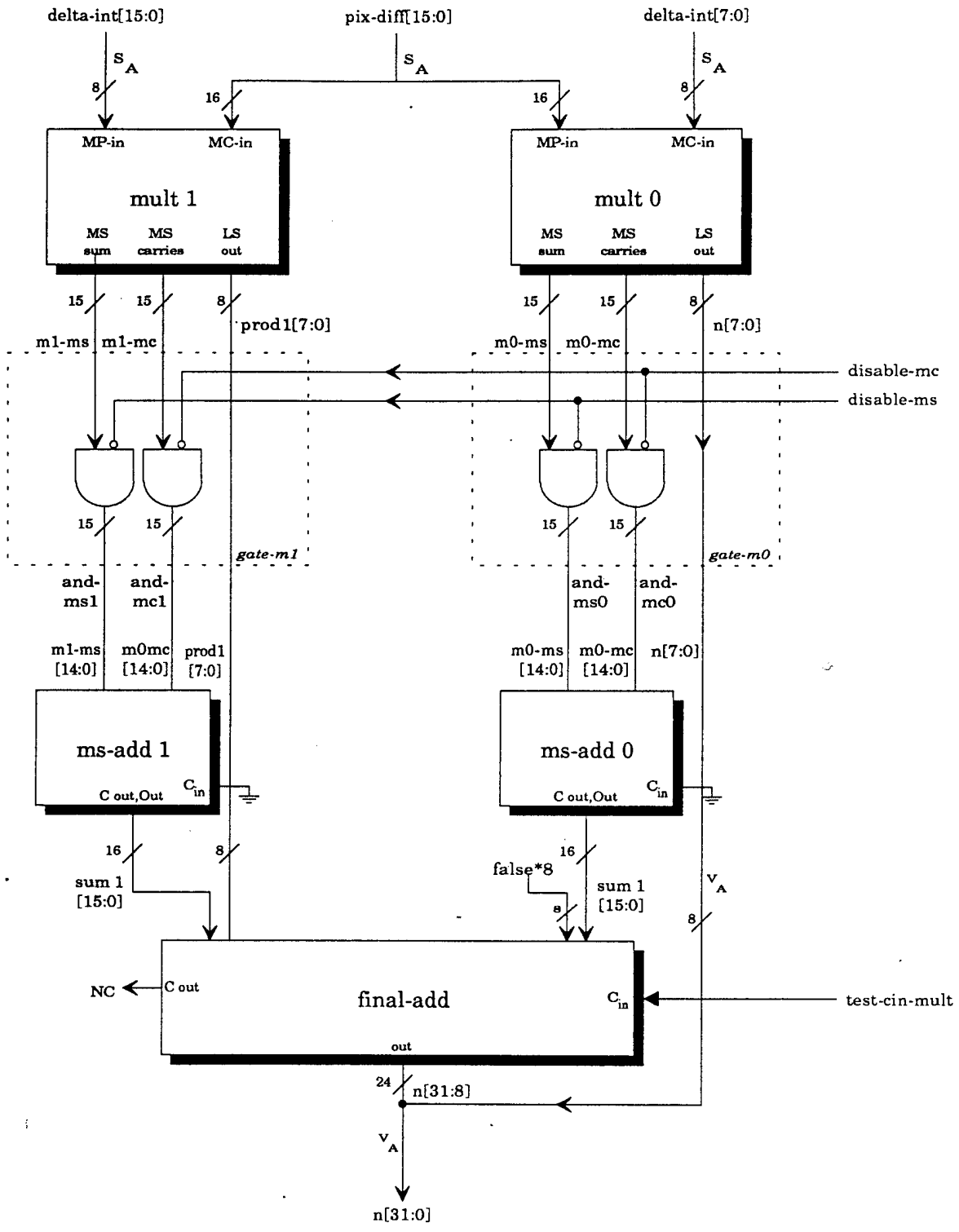
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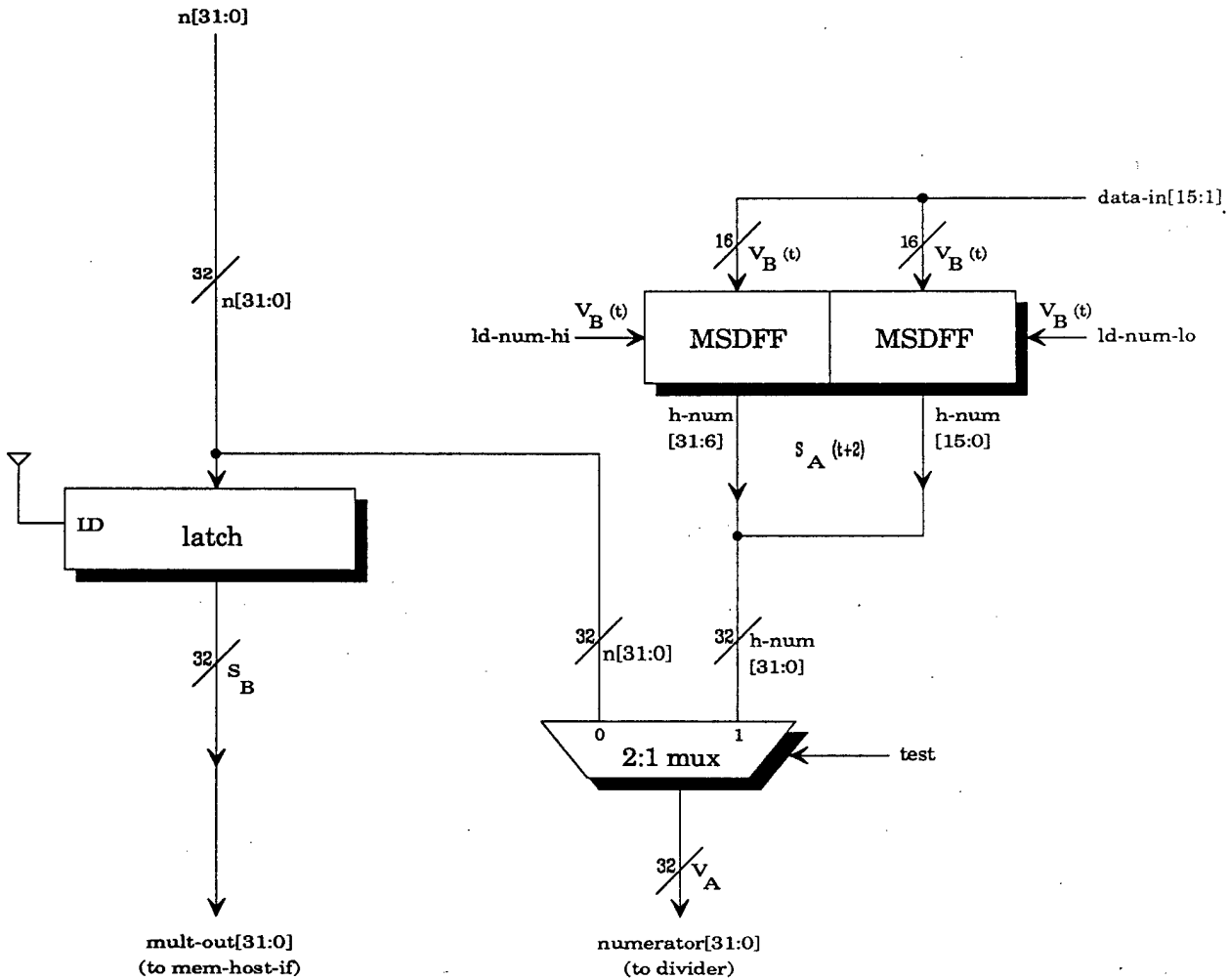


pre-div/cal-out-sub

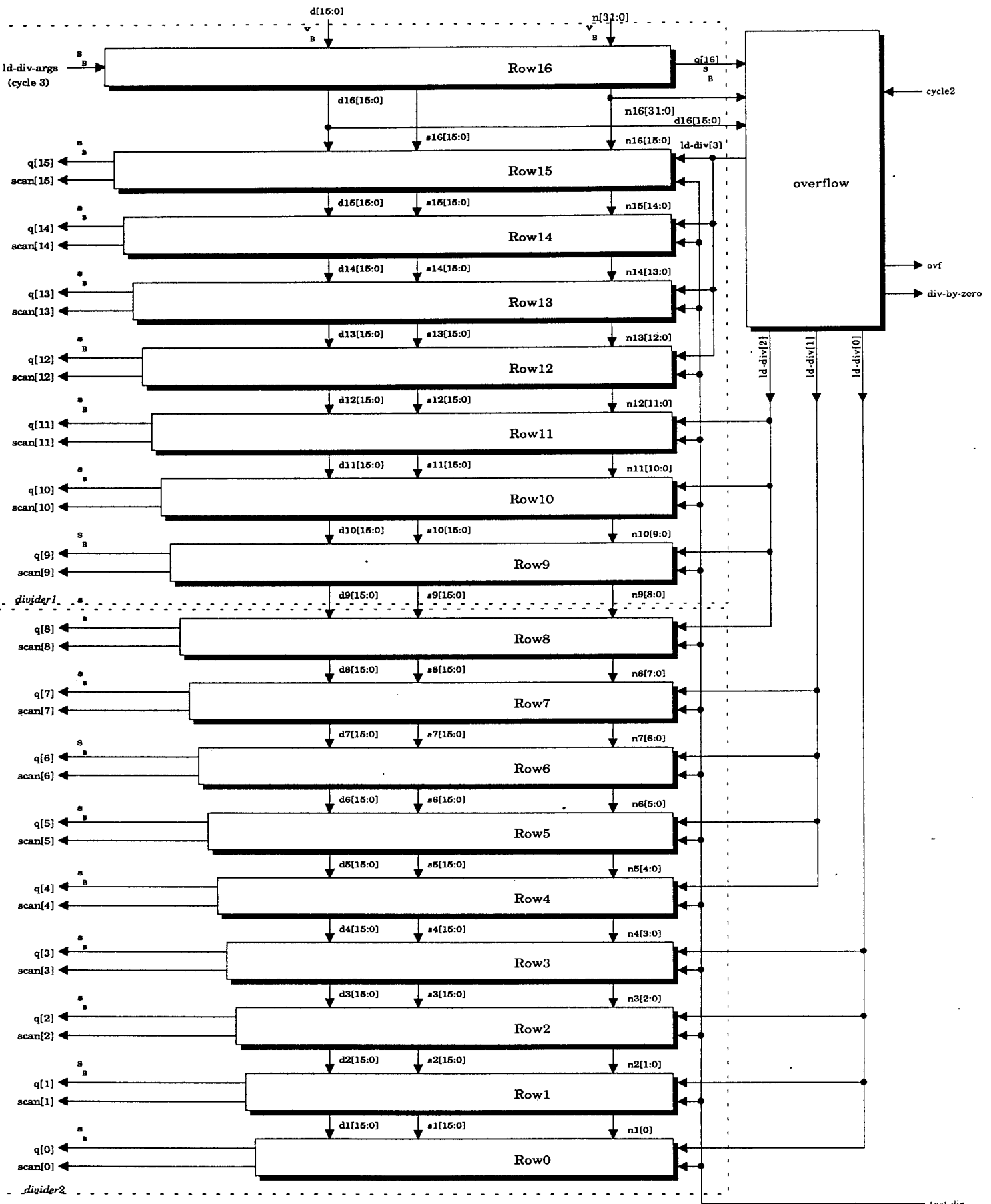
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 Gen: <chip>/math/pre-div  
 <chip>/math/pre-div/cal-out-sub



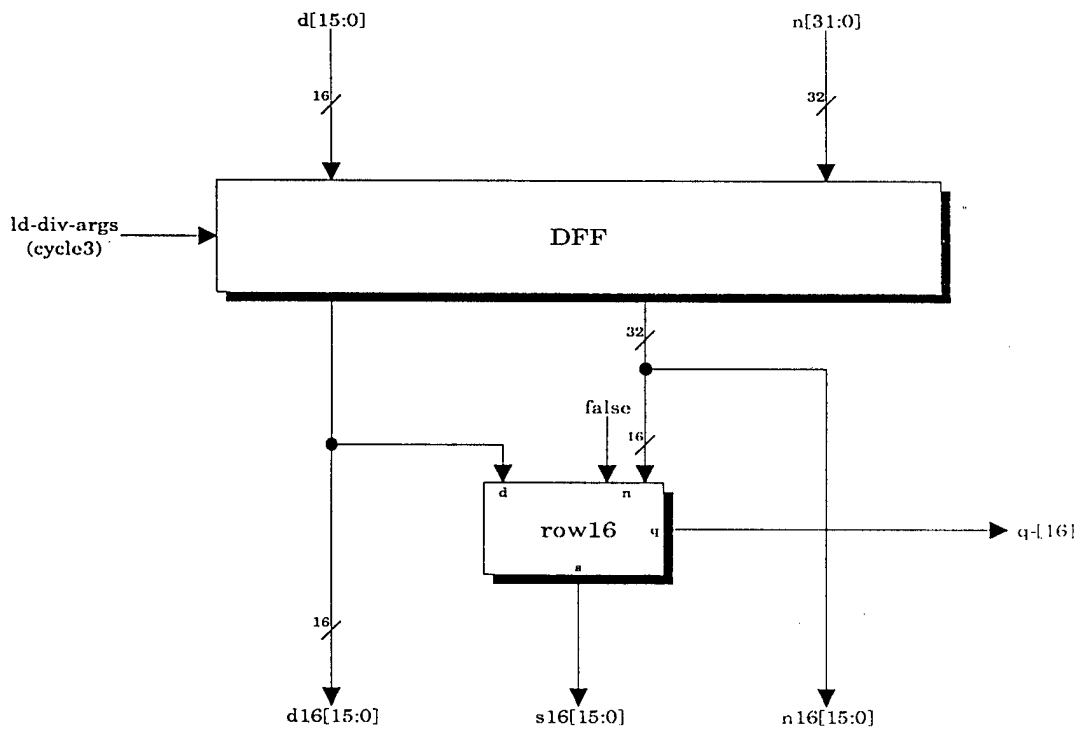
pre-div/mult/mult-block



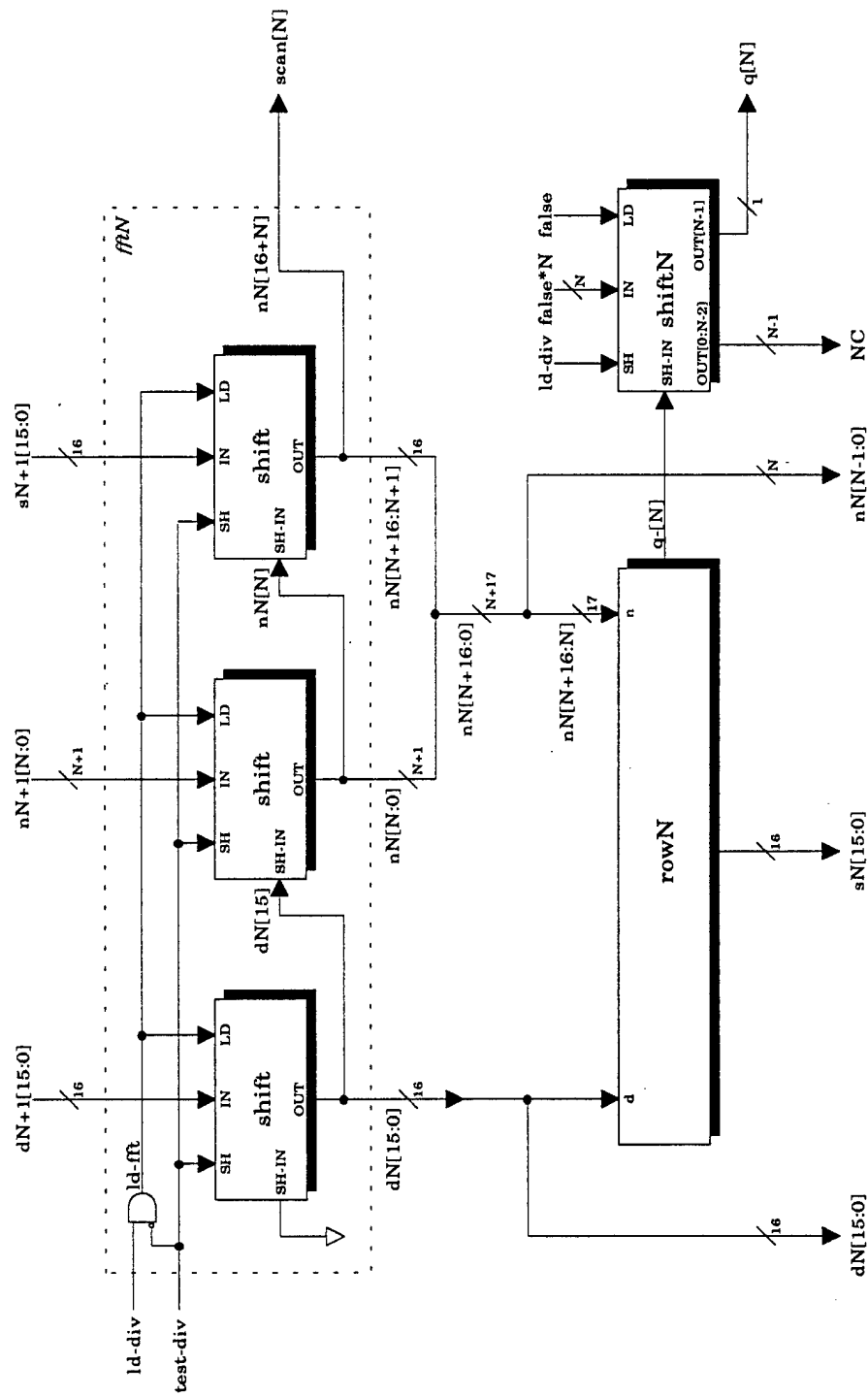
pre-div/mult/mult-out



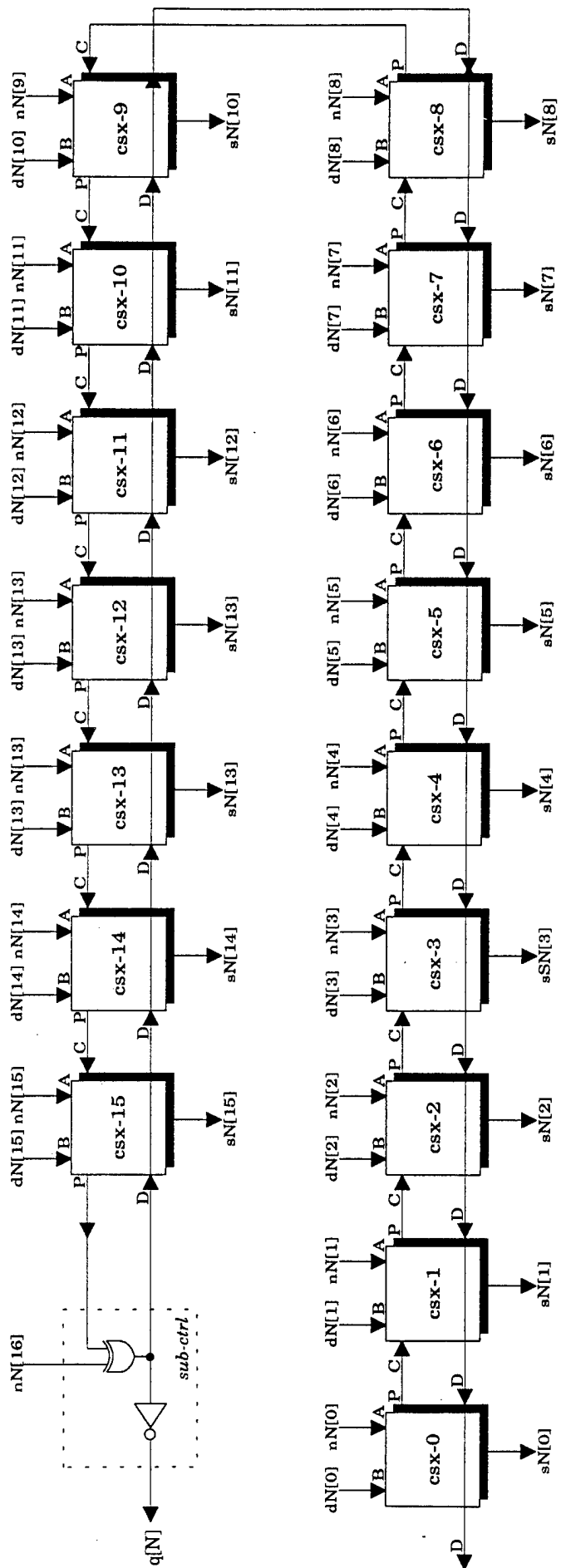
divider pipeline



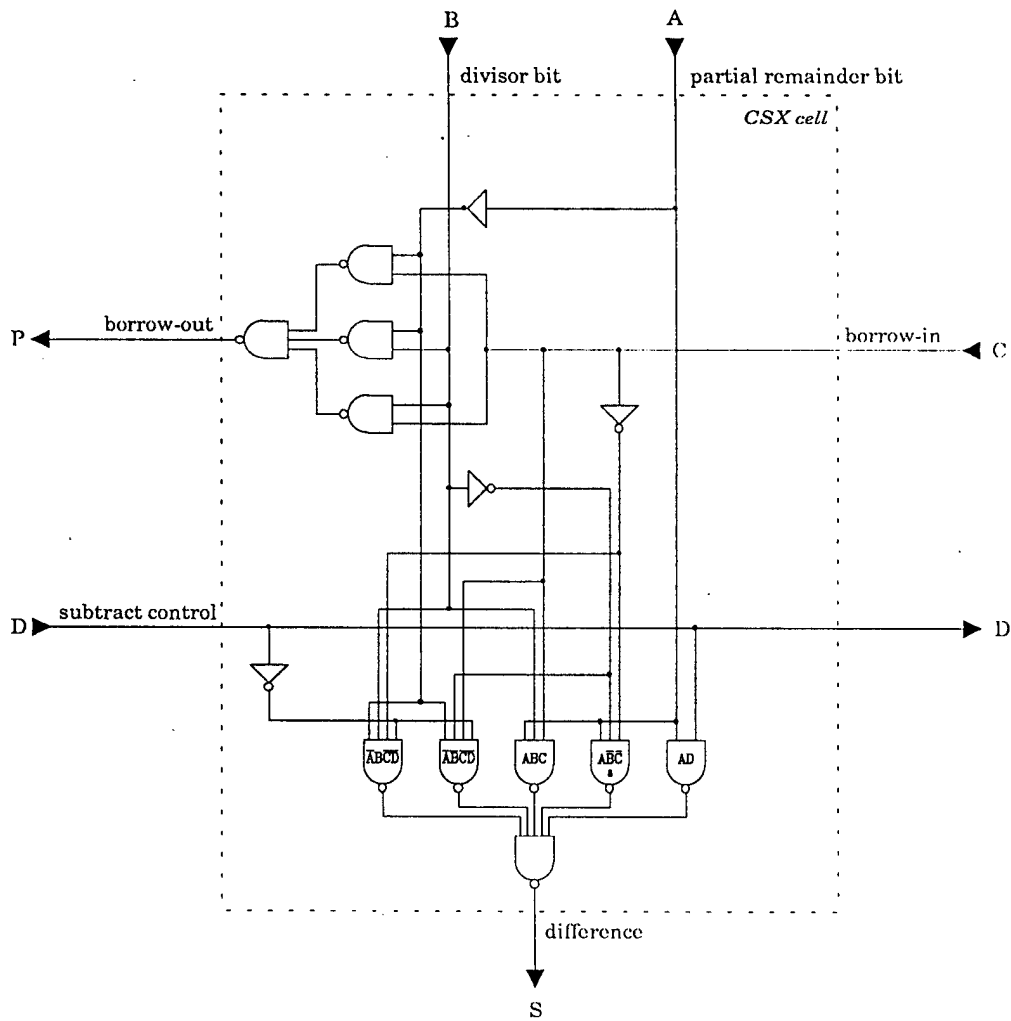
math/divider1/  
divider2/row16



**math/divider1/RowN**  
**divider2/**  
 (N = 0..15)

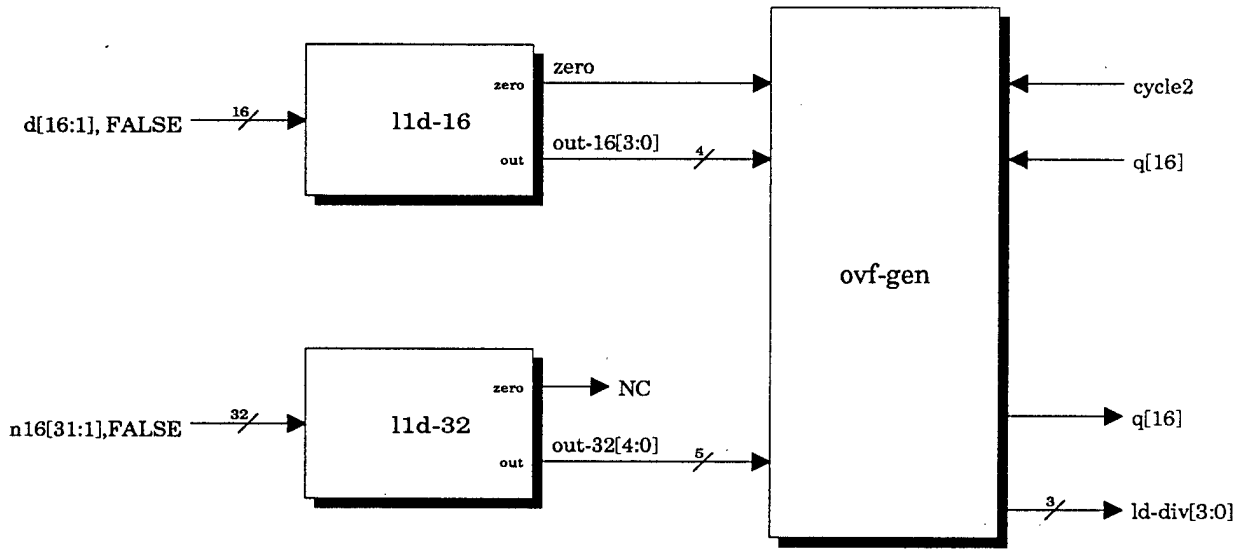


divider1 / RowN/rowN  
divider2 /



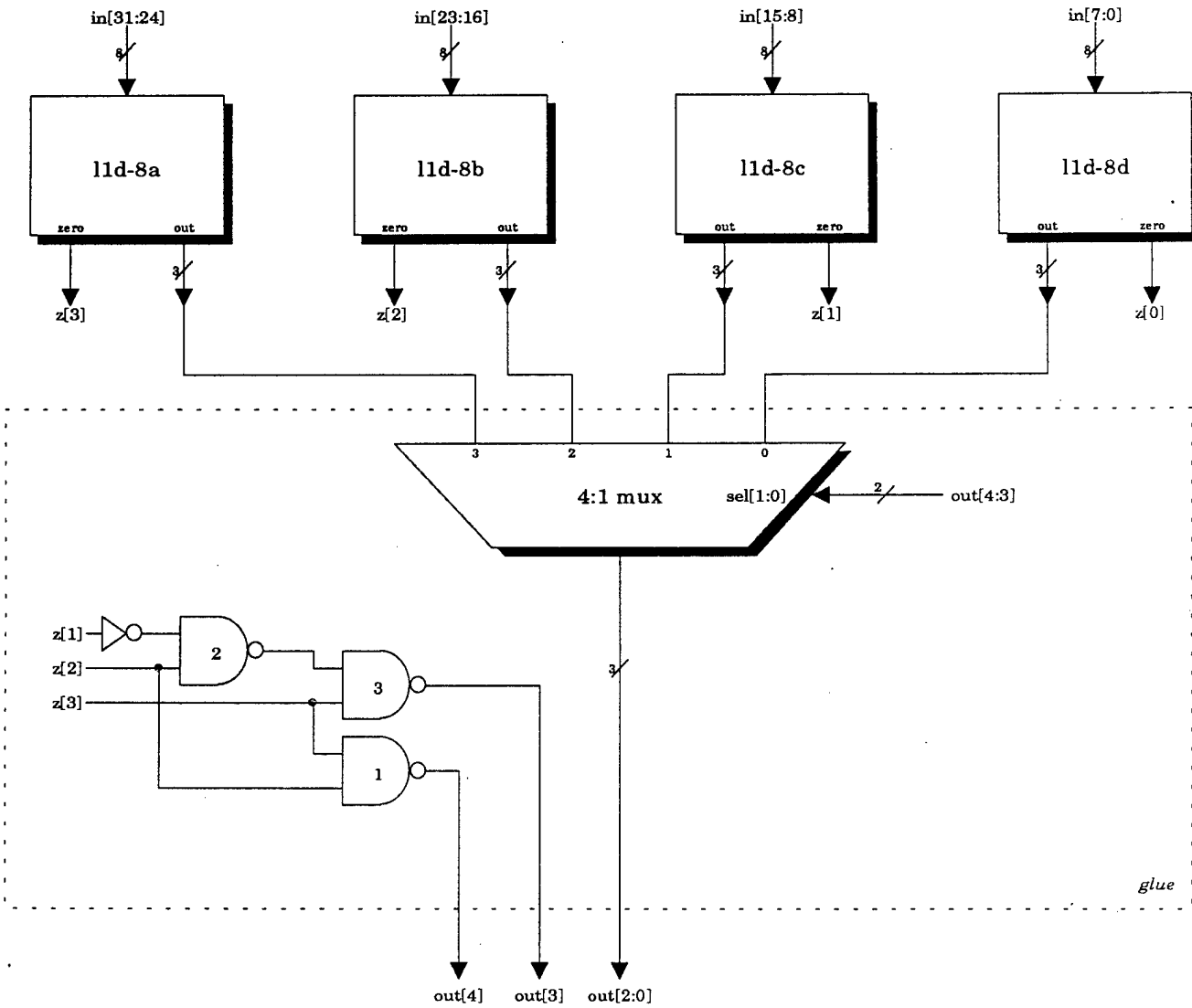
divider1 / RowN/rowN/csx-M  
 divider2 /  
 ( N=0..16, M=0..15)

Doc: d:\jackson\prem\csx.drw  
 Gen: <chip>/math/divider/Row[16..0]/row[16..0]/csx-[15..0]

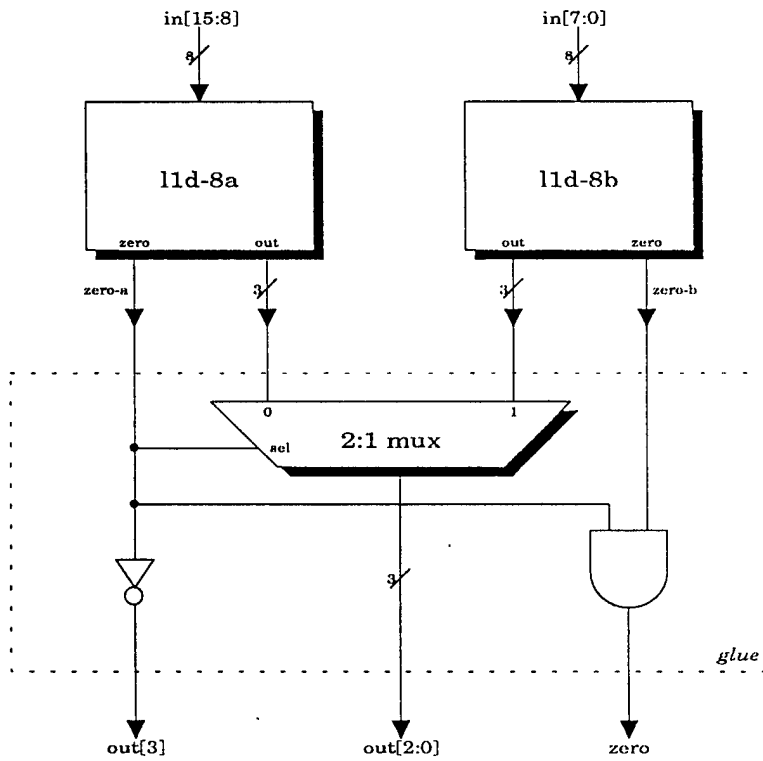


**math/overflow**

Doc: d:\jackson\premi\overflow.drw  
 Gen: <chip>\math\divider\overflow

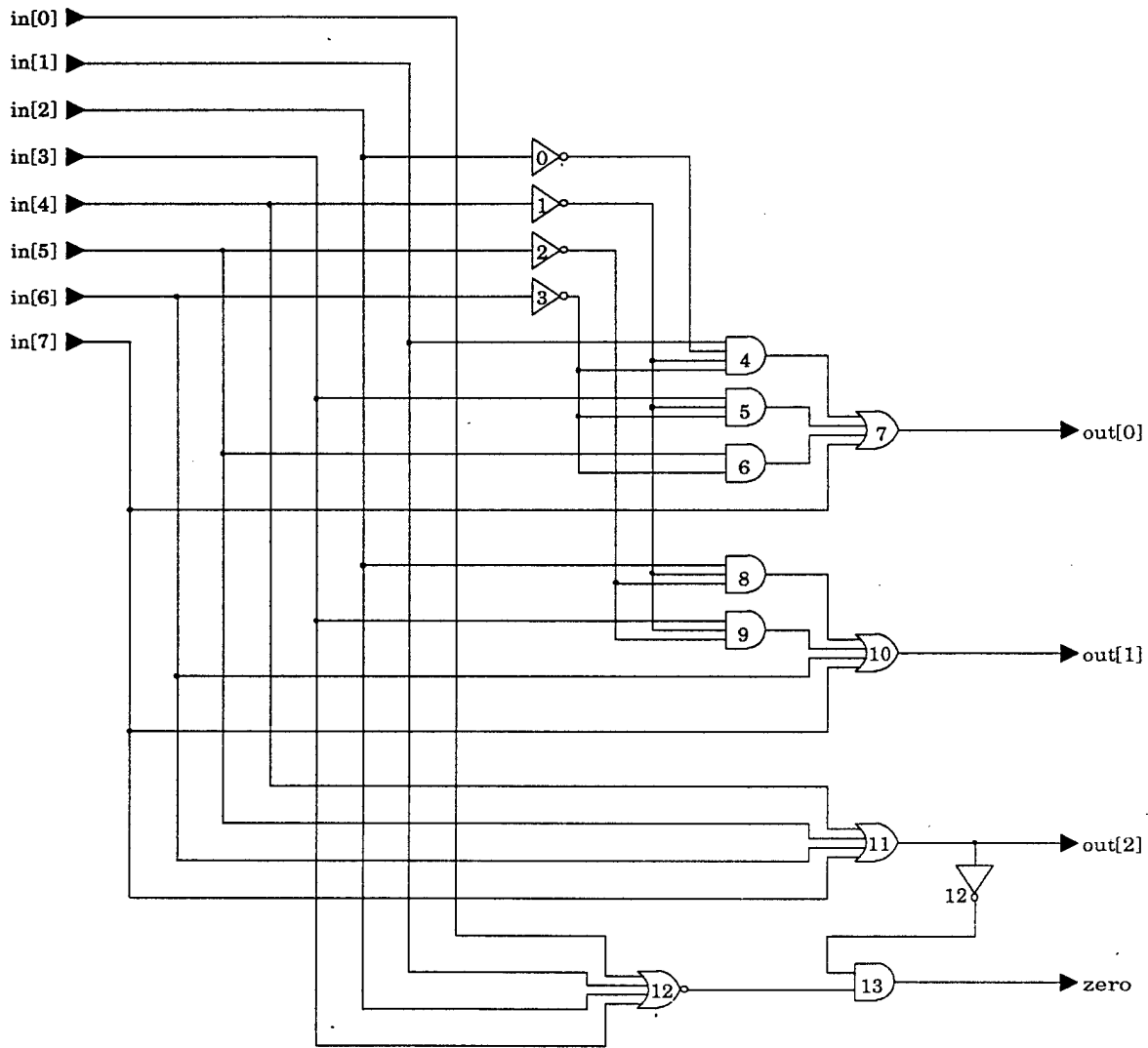


**overflow/11d-32**



overflow/11d-16

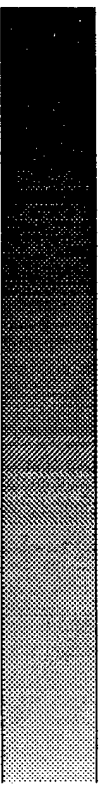
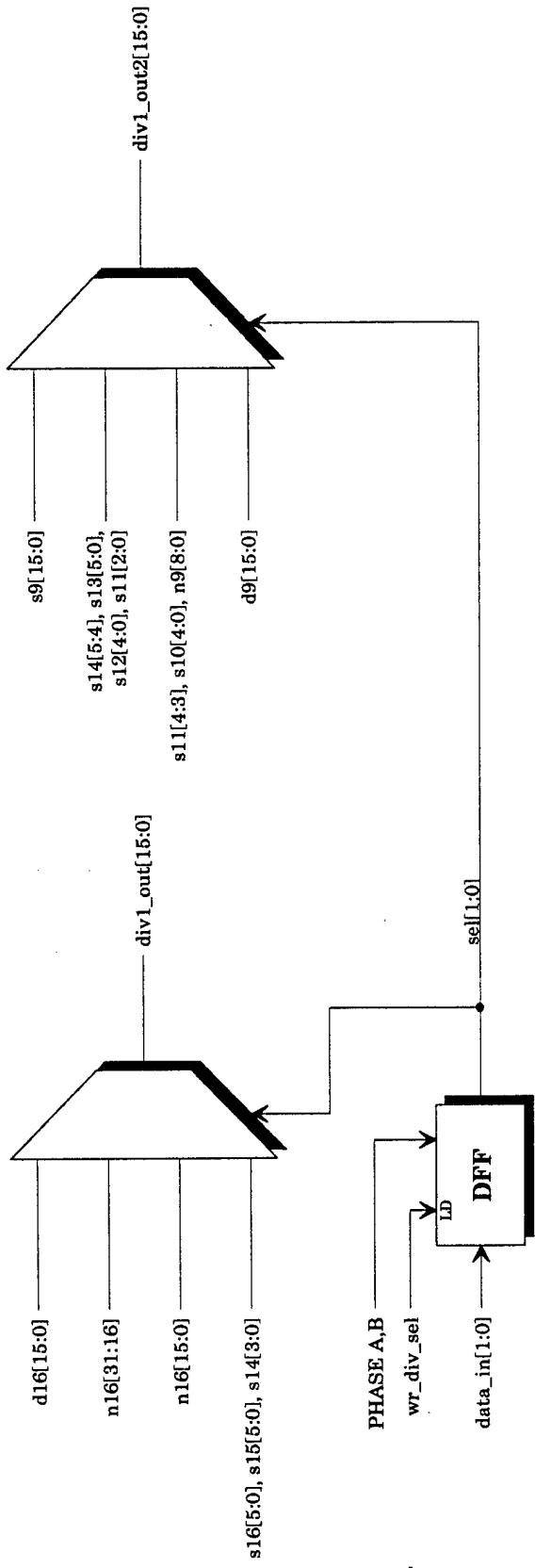
Doc: d:\jackson\prom\11d16.drw  
Gen: cchip>divider/overflow/11d-16



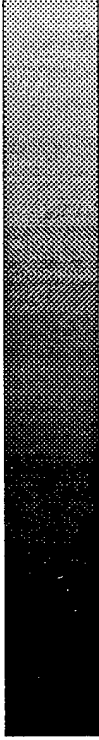
**l1d-32/l1d-8x, l1d-16/l1d-8x**  
 (8-bit leading one detector)

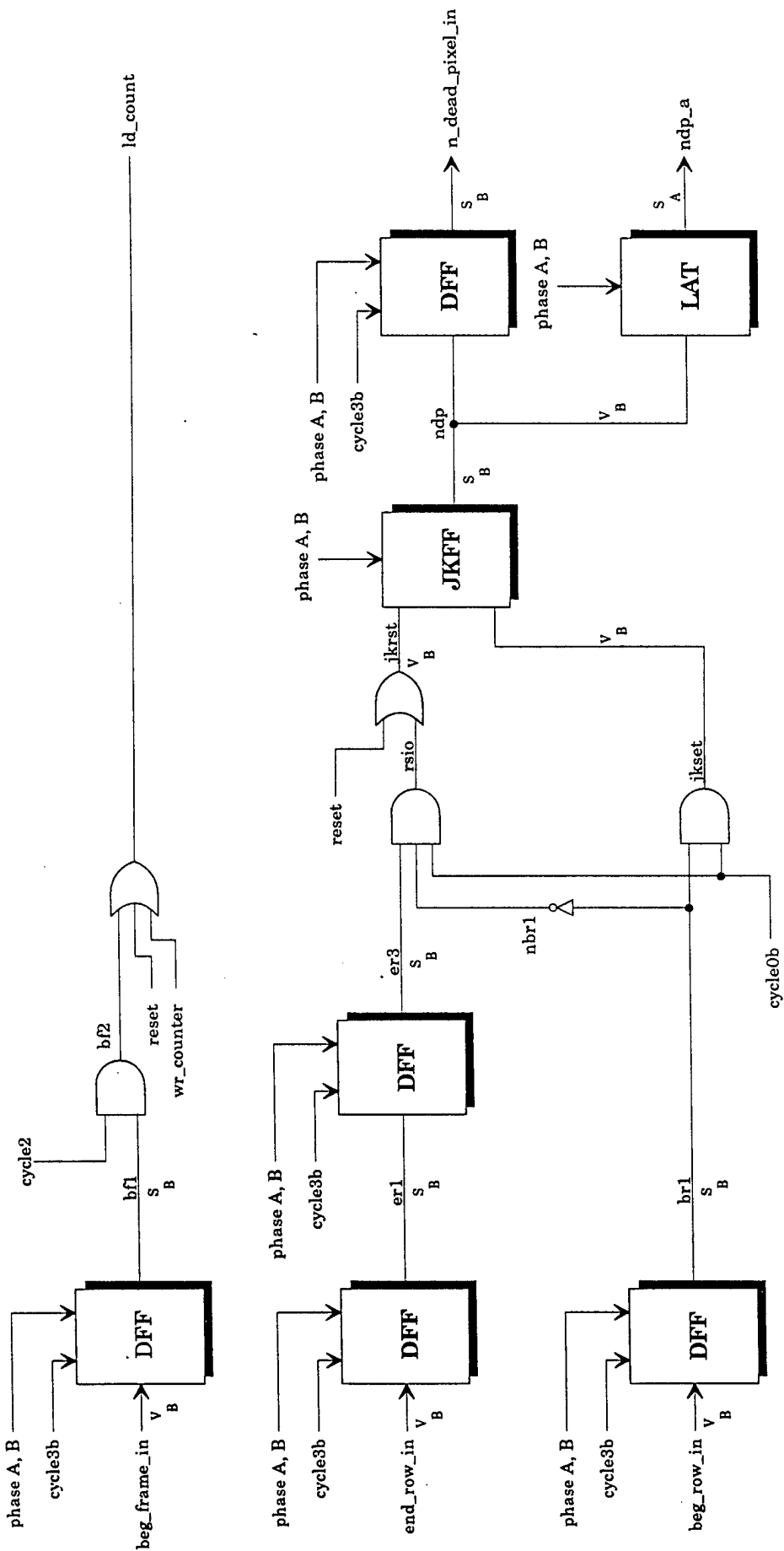
Doc: d:\yachon\yachon\l1d\l1d.drw  
 Date: 04/19/2000 09:41:14  
 Author: yachon





**divider1/probe**

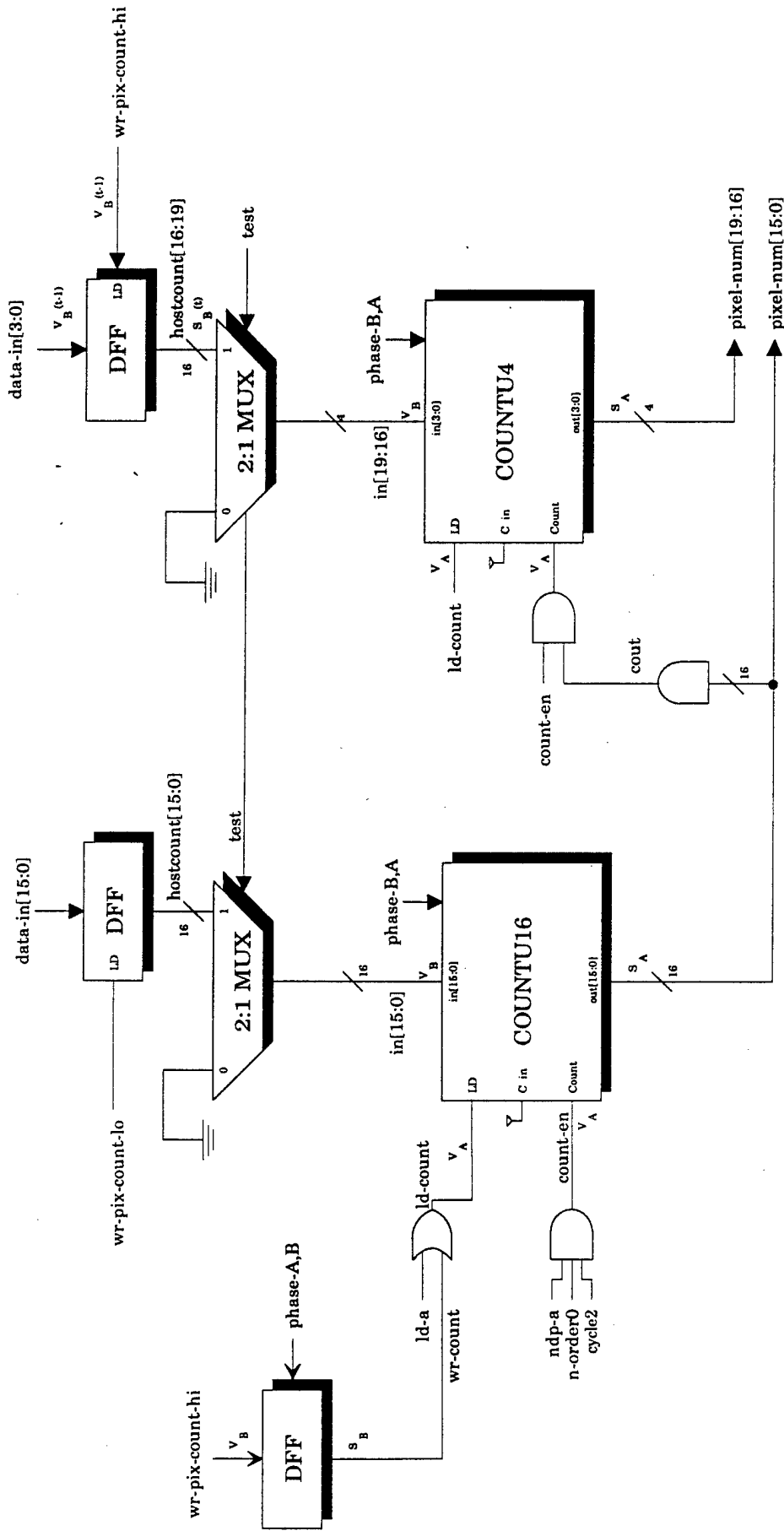


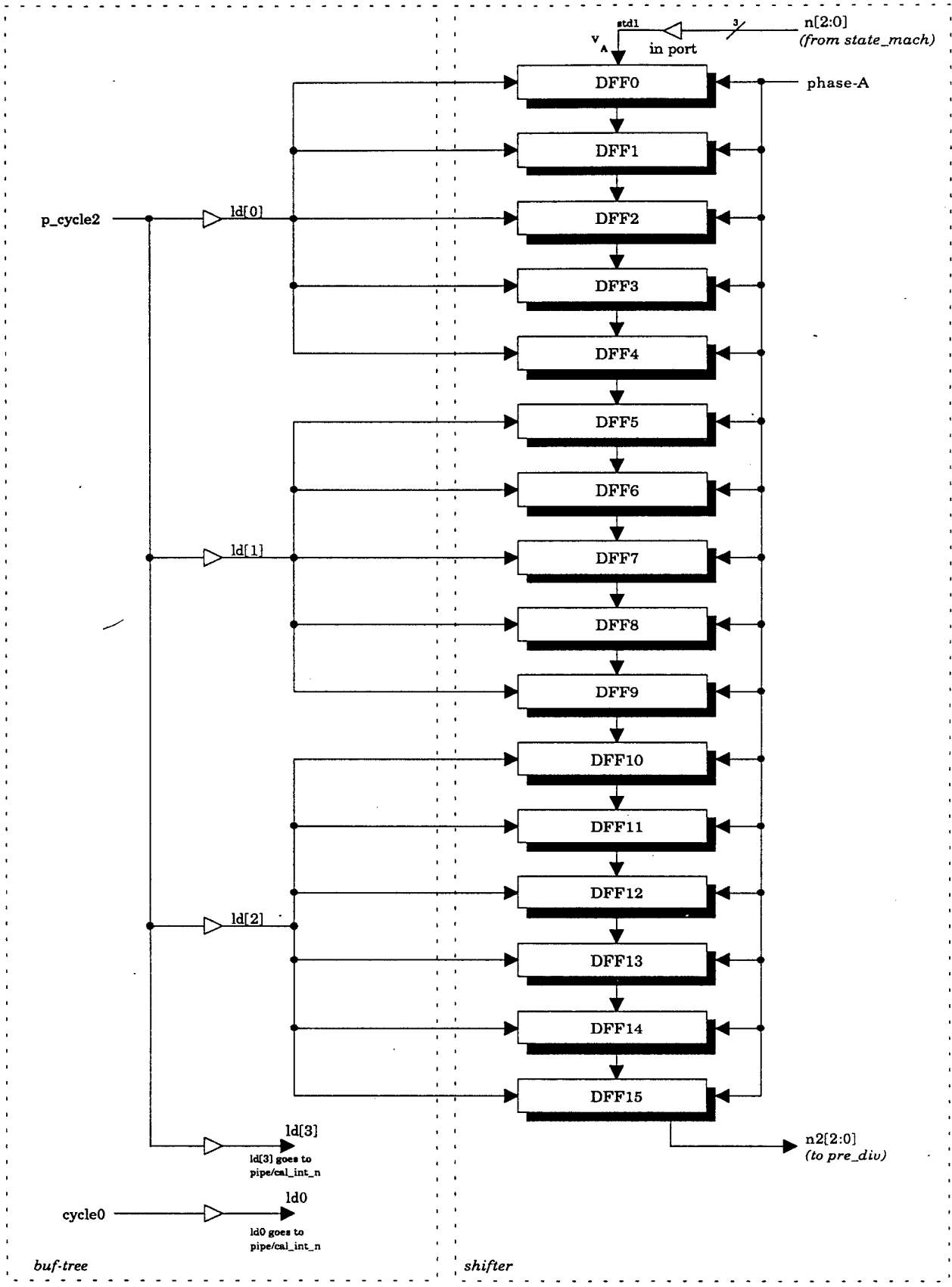


# nuc/math/pix\_counter

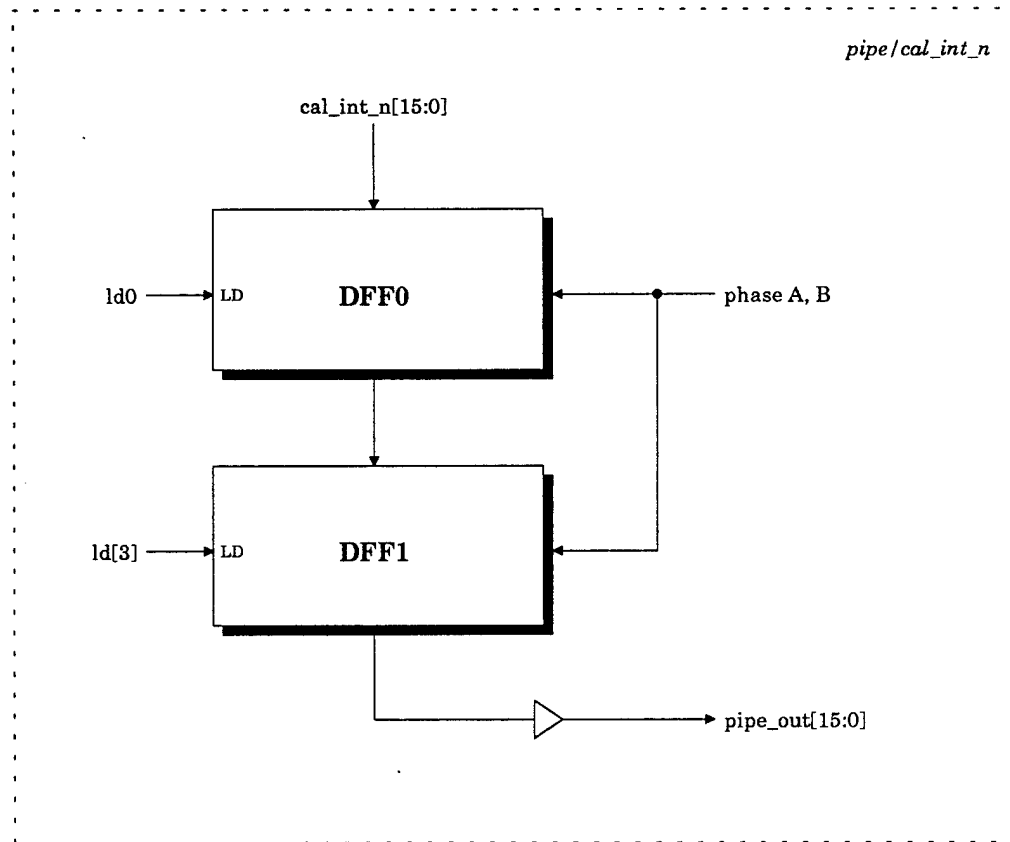
(page 1 of 2)

D:\gtnuc\pix2.drw  
Gen: chip>pix\_counter



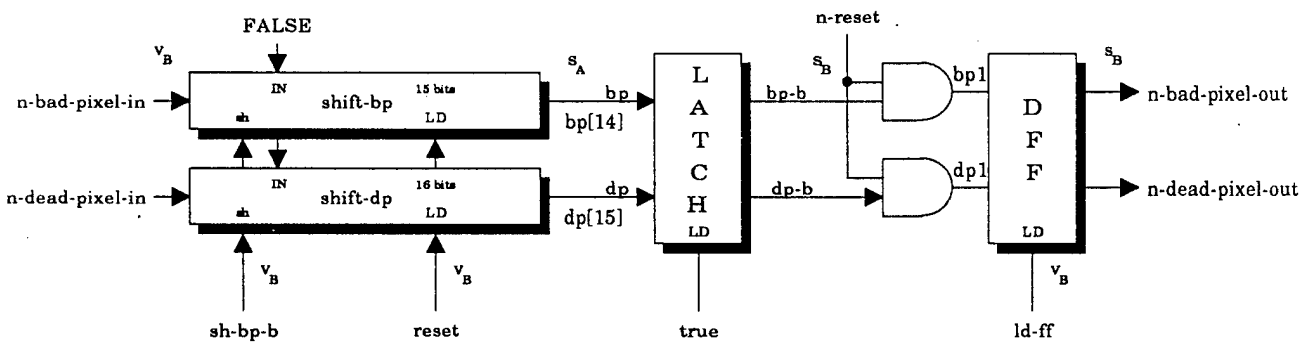
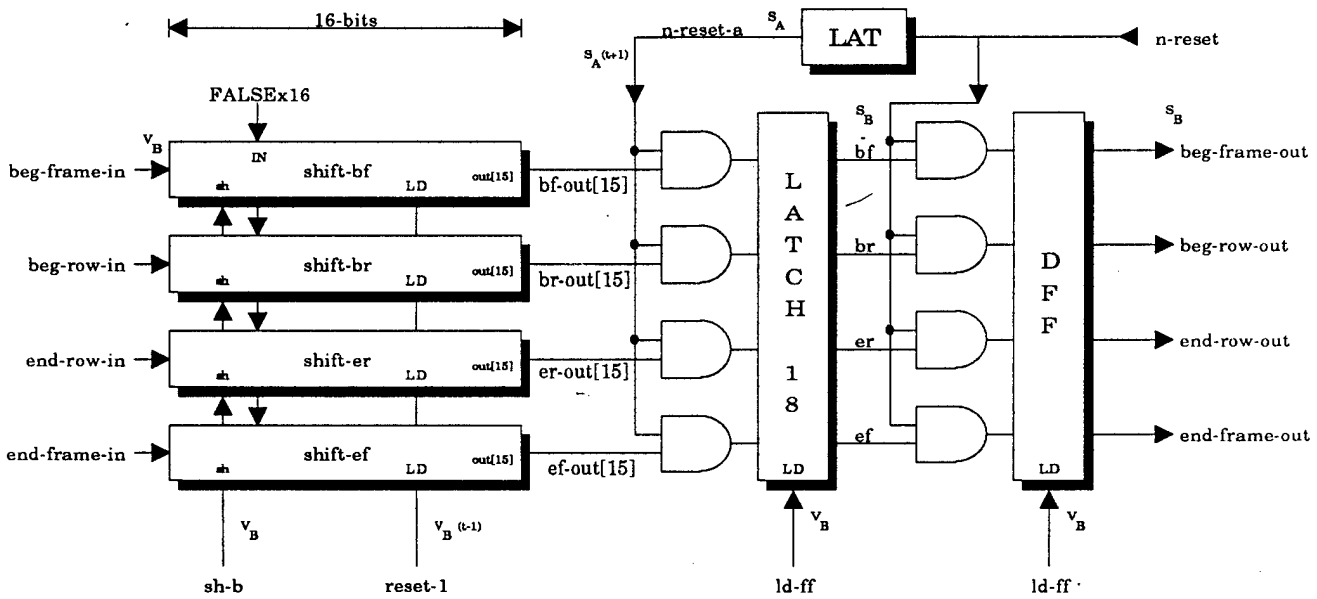
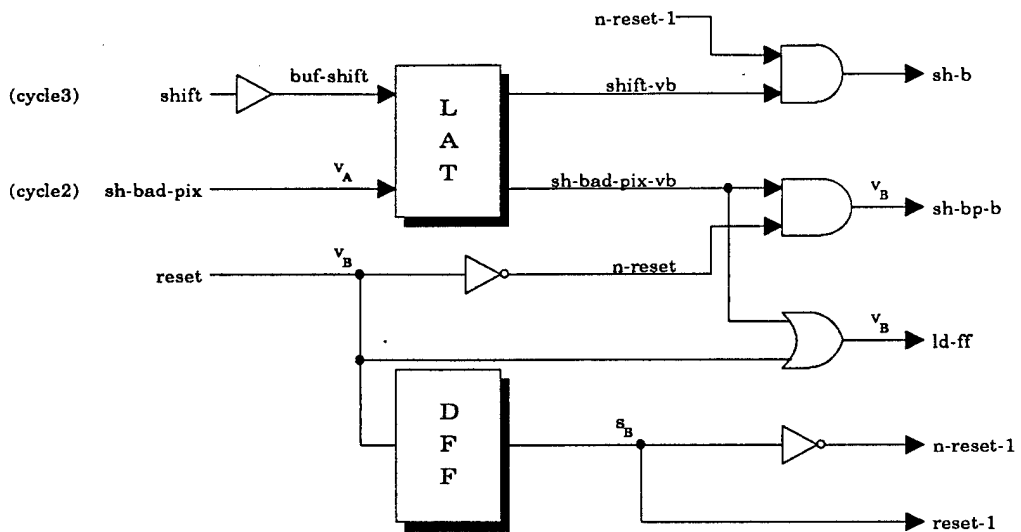


nuc/math/pipe



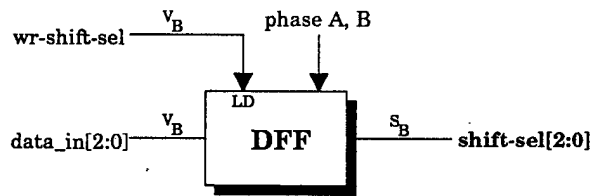
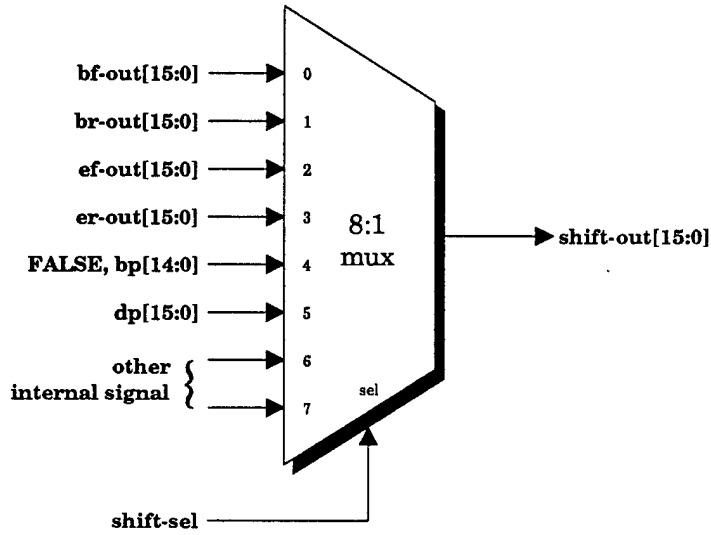
**pipe/cal\_int\_n**

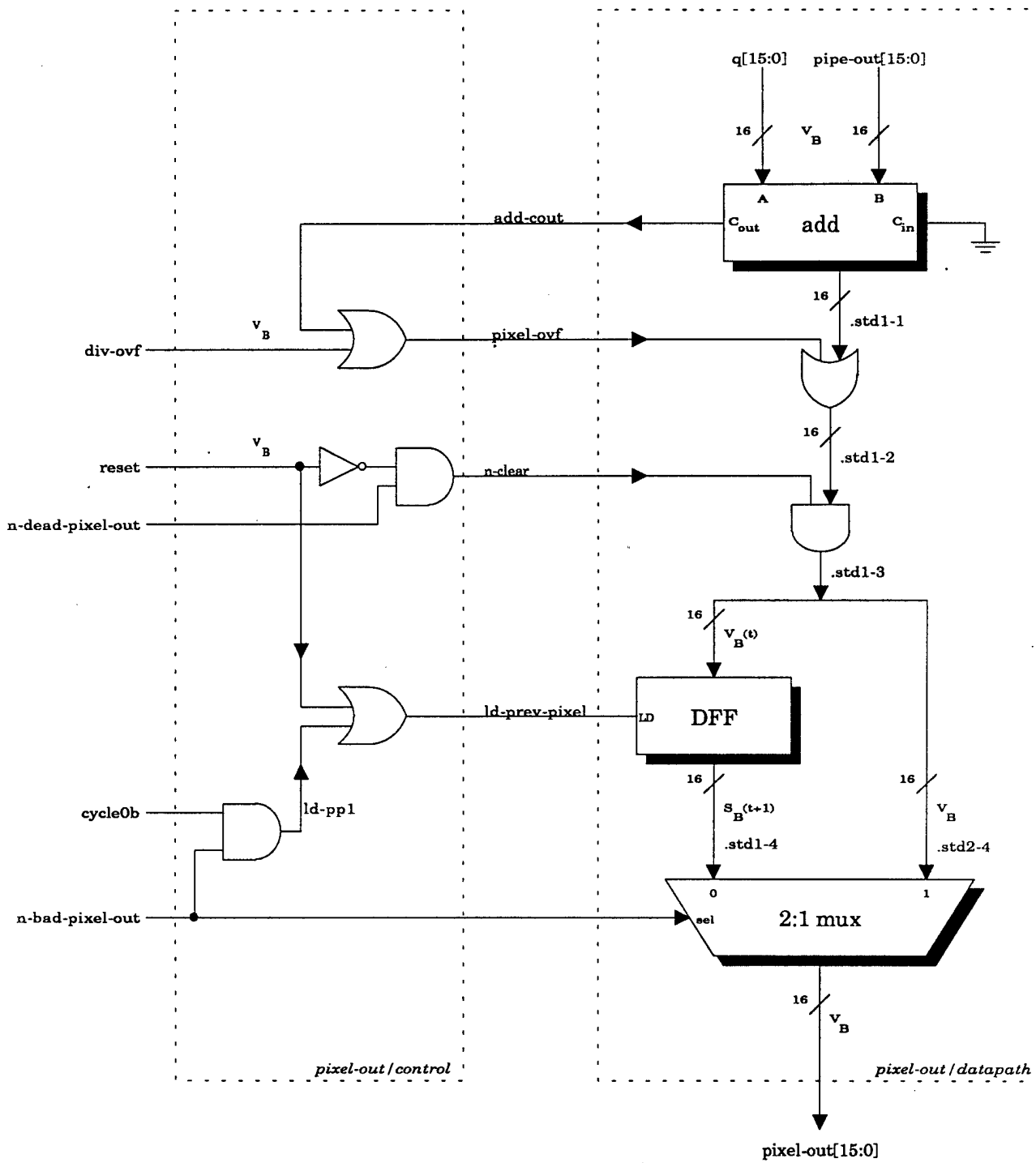
Dos: d:\jackson\prem\cal\_int.drw  
Gen: <chip>/pipe/cal\_int\_n



**math/frame-sync**

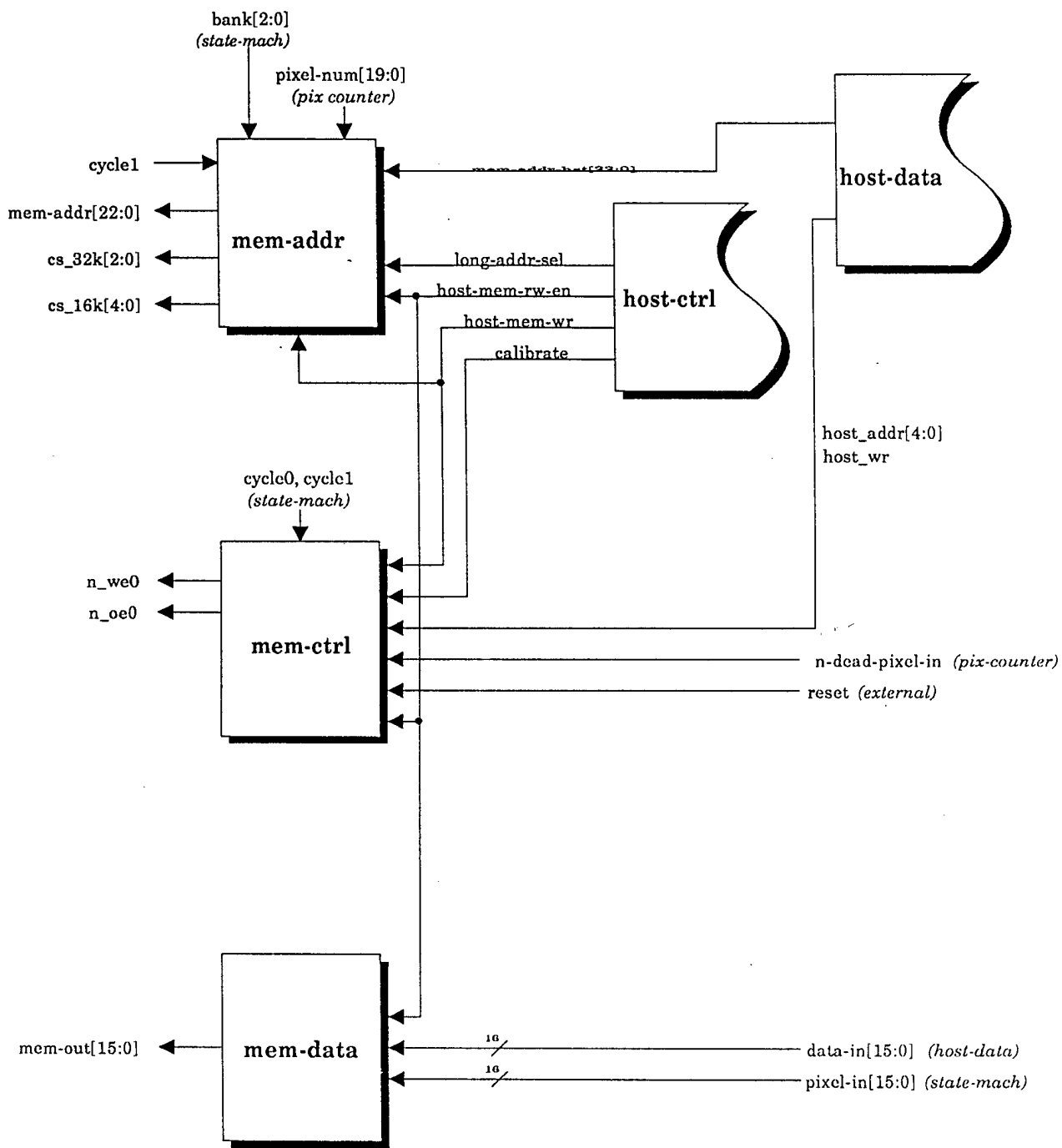
(page 1 of 2)

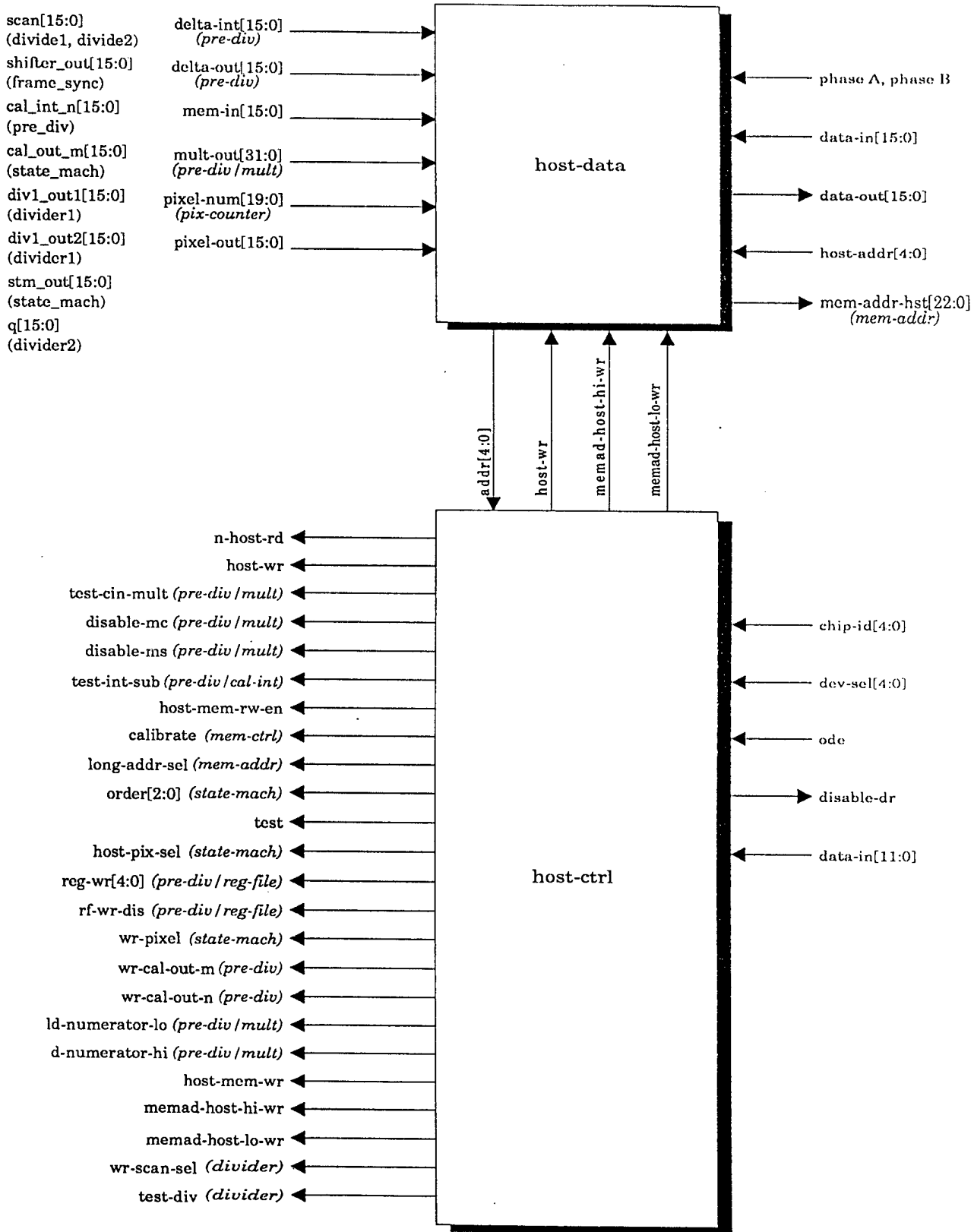




nuc/math/pixel-out

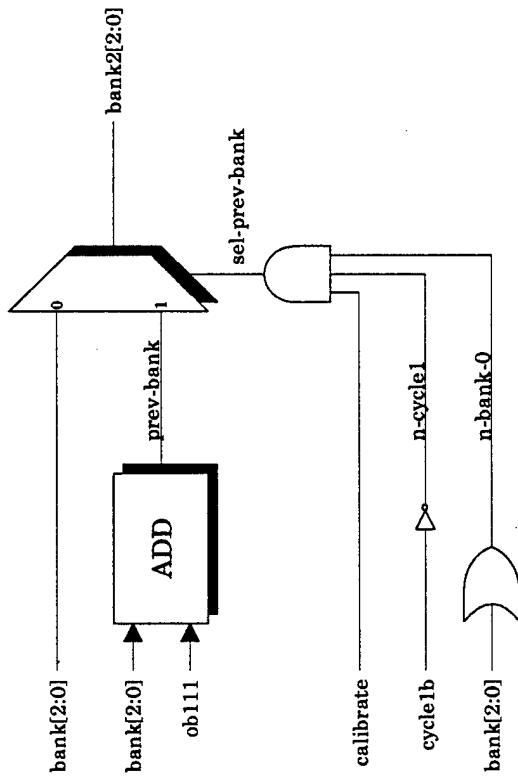
Doc: d:\jackson\prem\pixelout.drw  
Gen: <chip>math/pixel-out





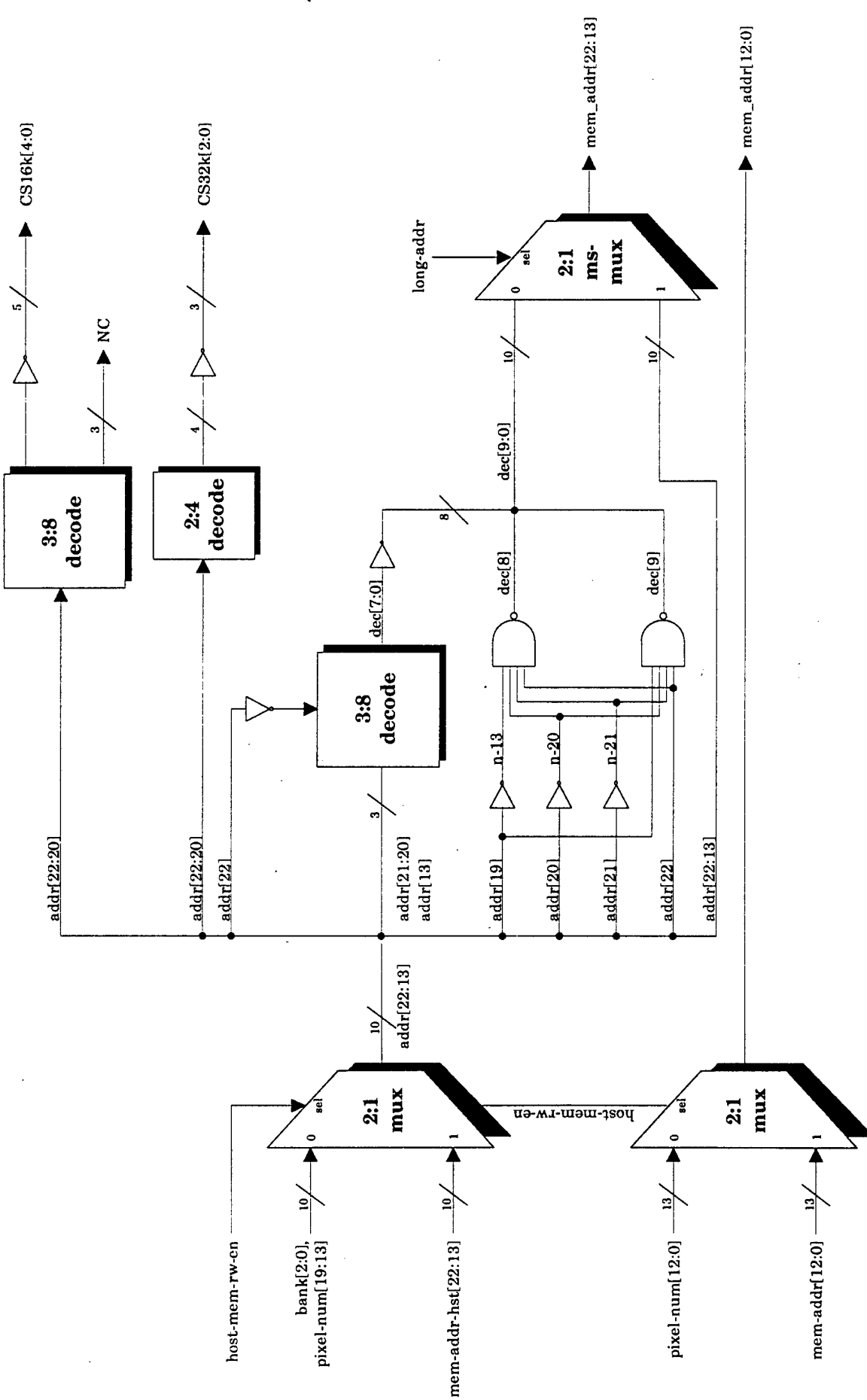
**math/mem-host-if**

(page 2 of 2)



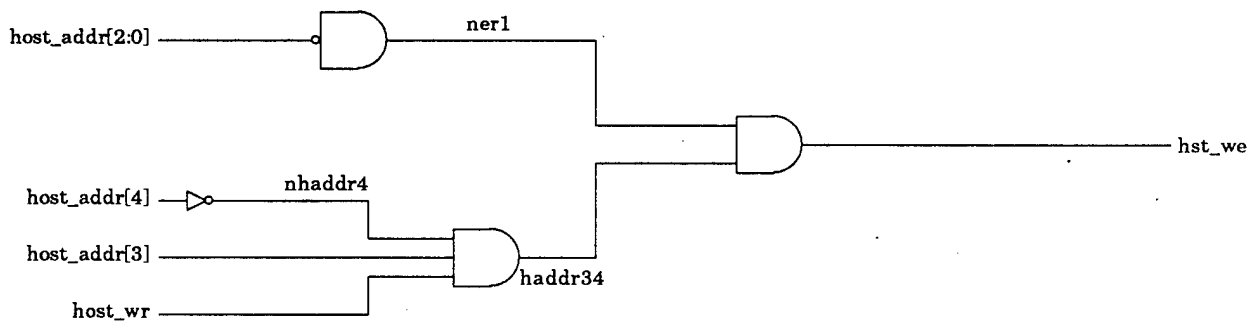
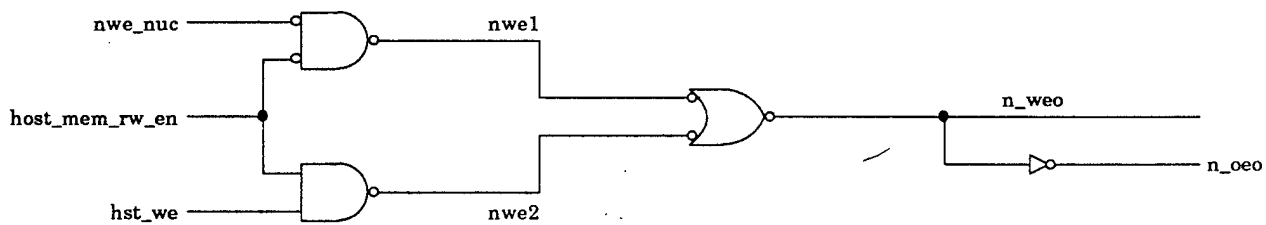
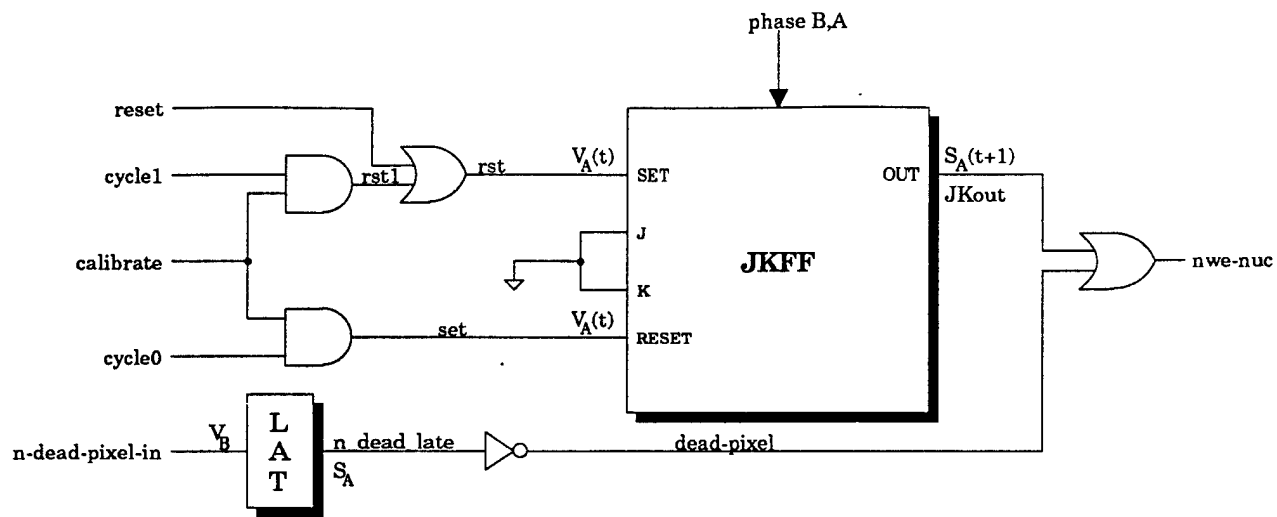
math/mem-host-if/mem-addr

Doc: d:\jackson\prem\lbpdetest.drw  
 Gen: <chip>math/state-mach/bad-pixel-detection



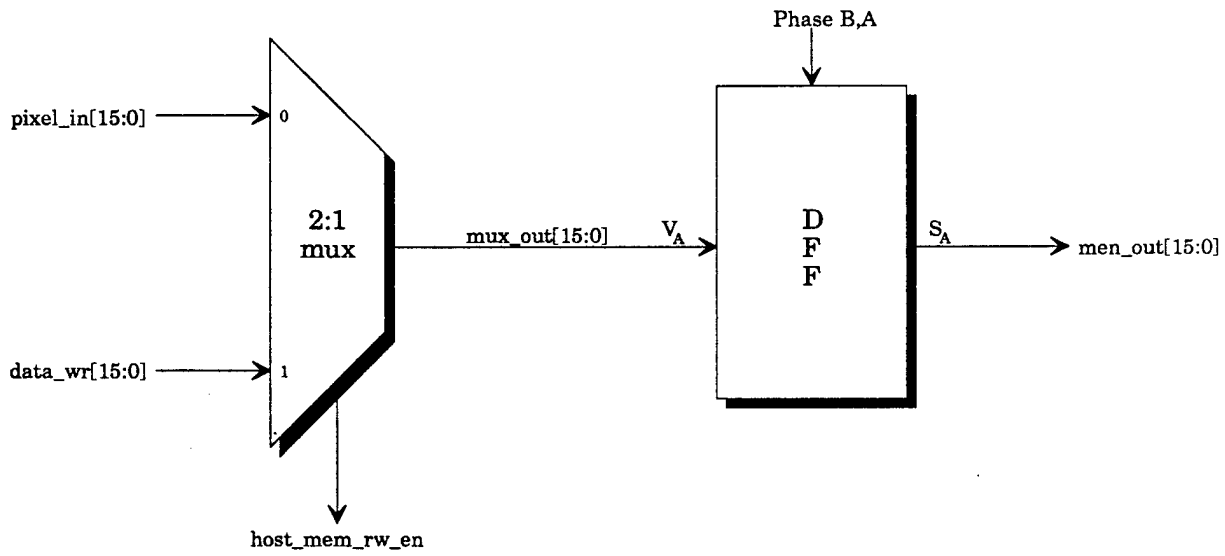
math/mem-host-if/mem-addr

Do not touch  
Gen-chip/math/mem-host-if/mem-addr



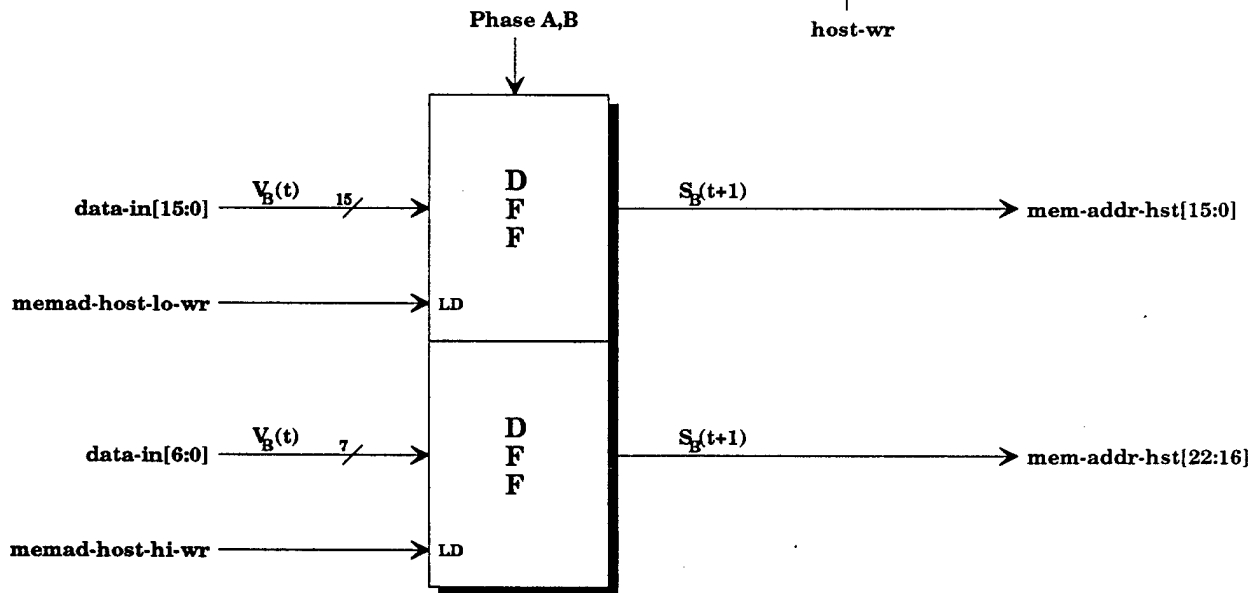
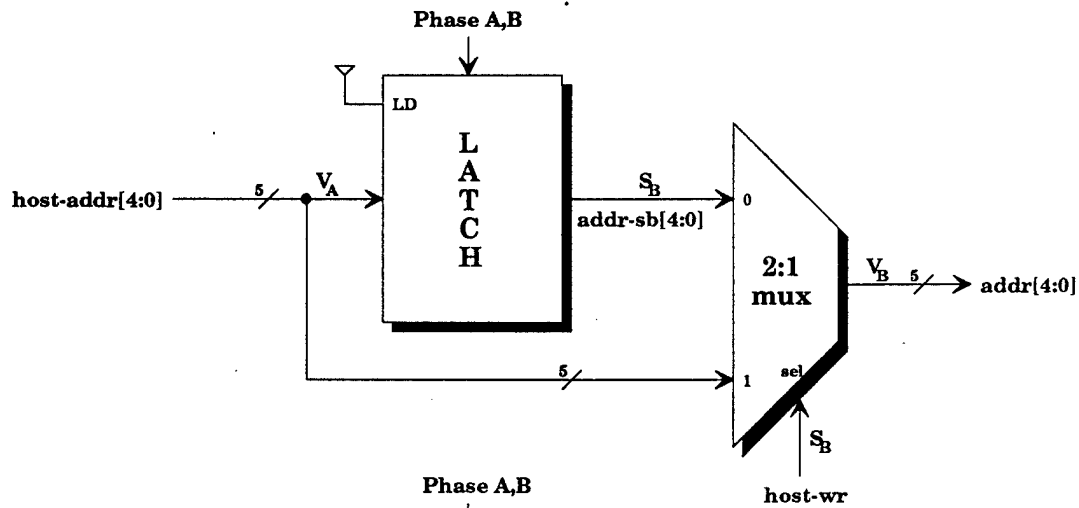
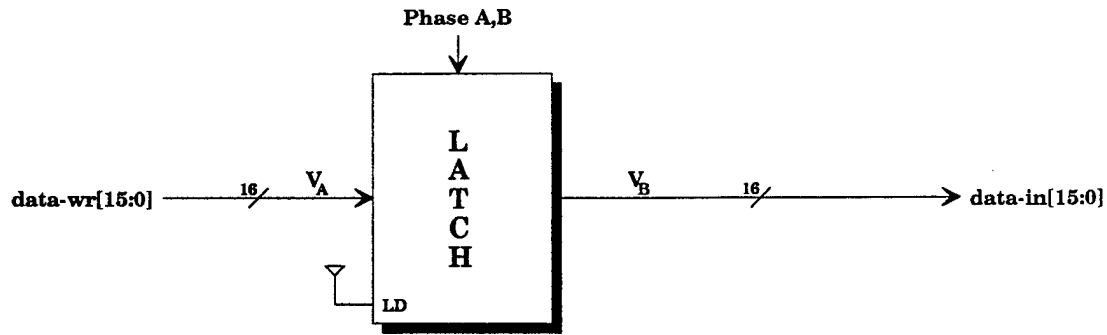
math/mem-host-if-/mem-ctrl

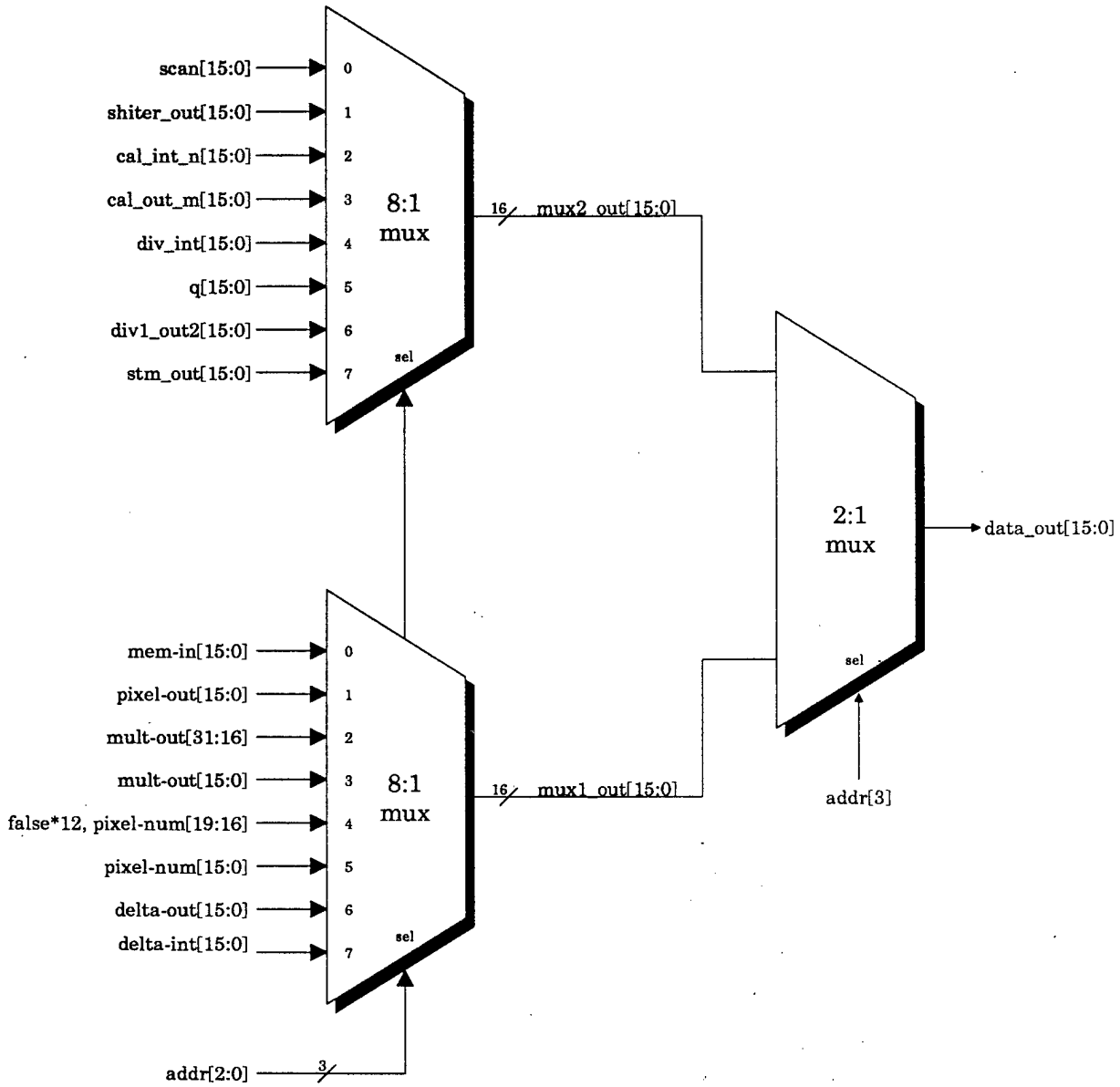
Doc: d:\jackson\premem\memctrl.drw  
 Gen: <chip>/math/mem-host-if/mem-ctrl

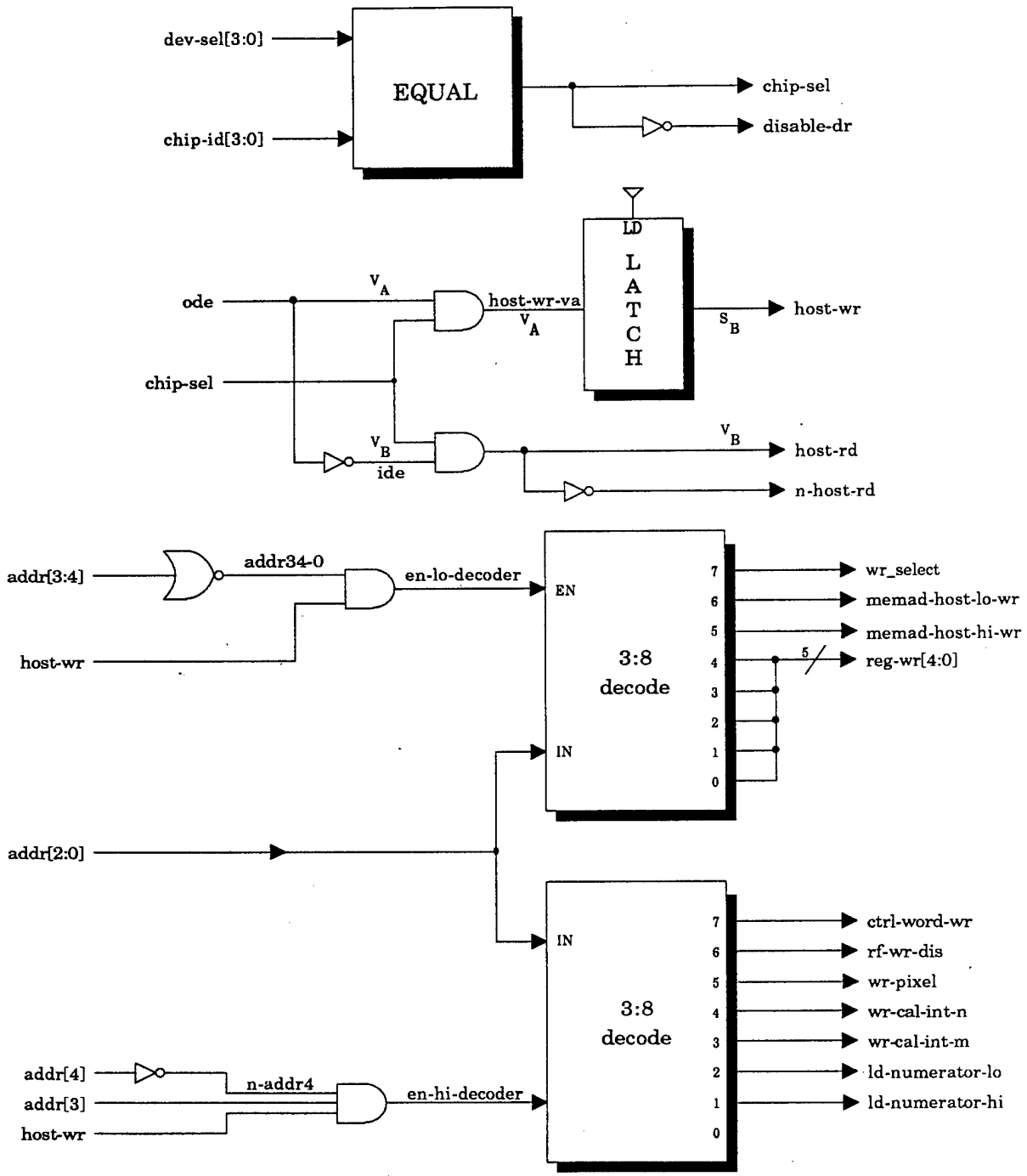


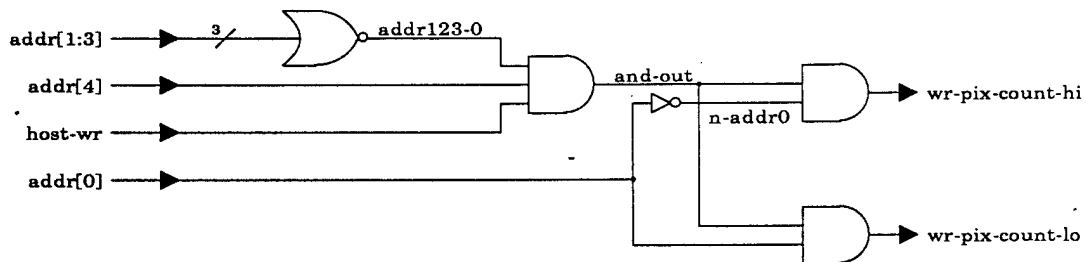
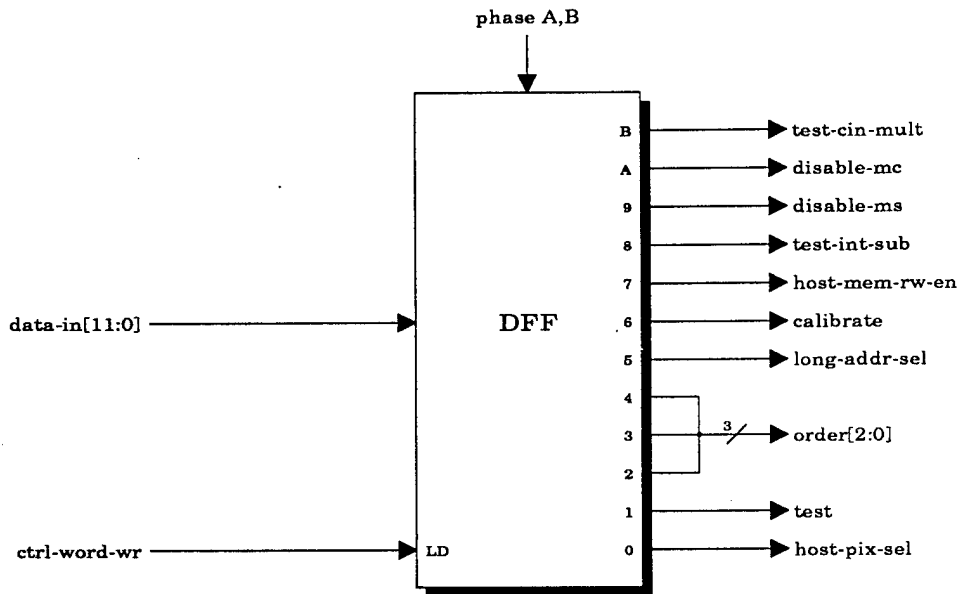
**math/mem-host-if/mem-data**

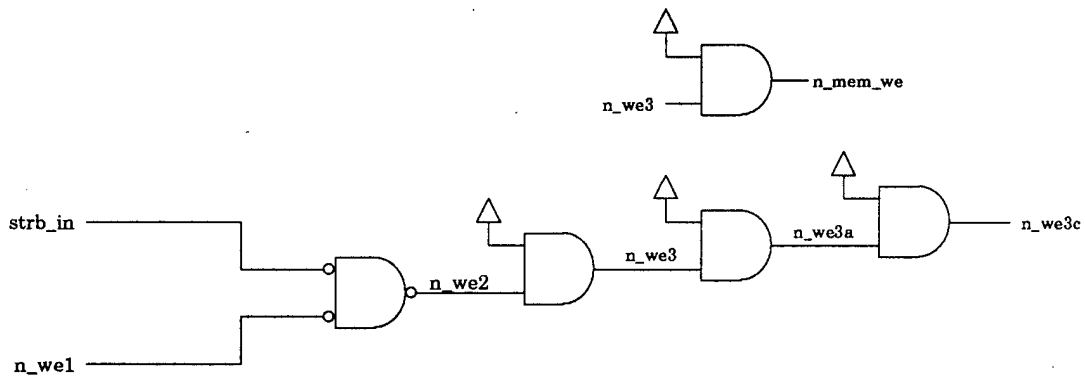
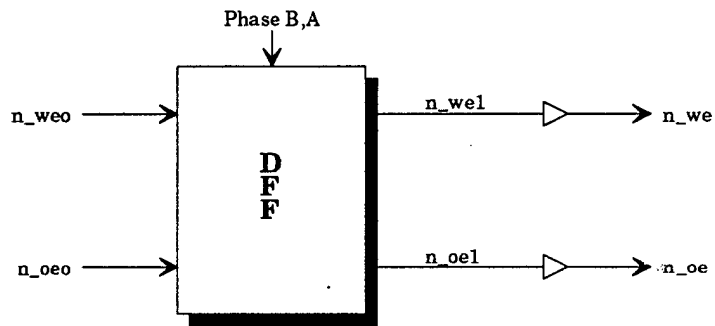
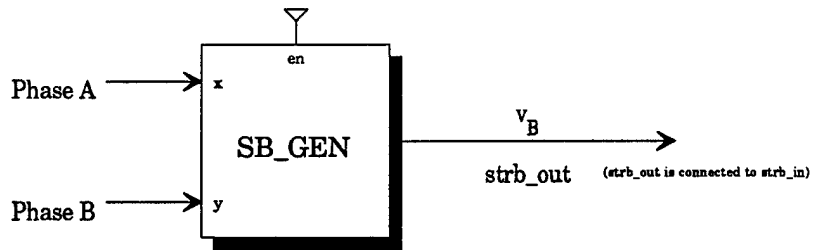
Doc: d:\jackson\prem\memdata.drw  
Gen: <chip>math/mem-host-if/mem-data



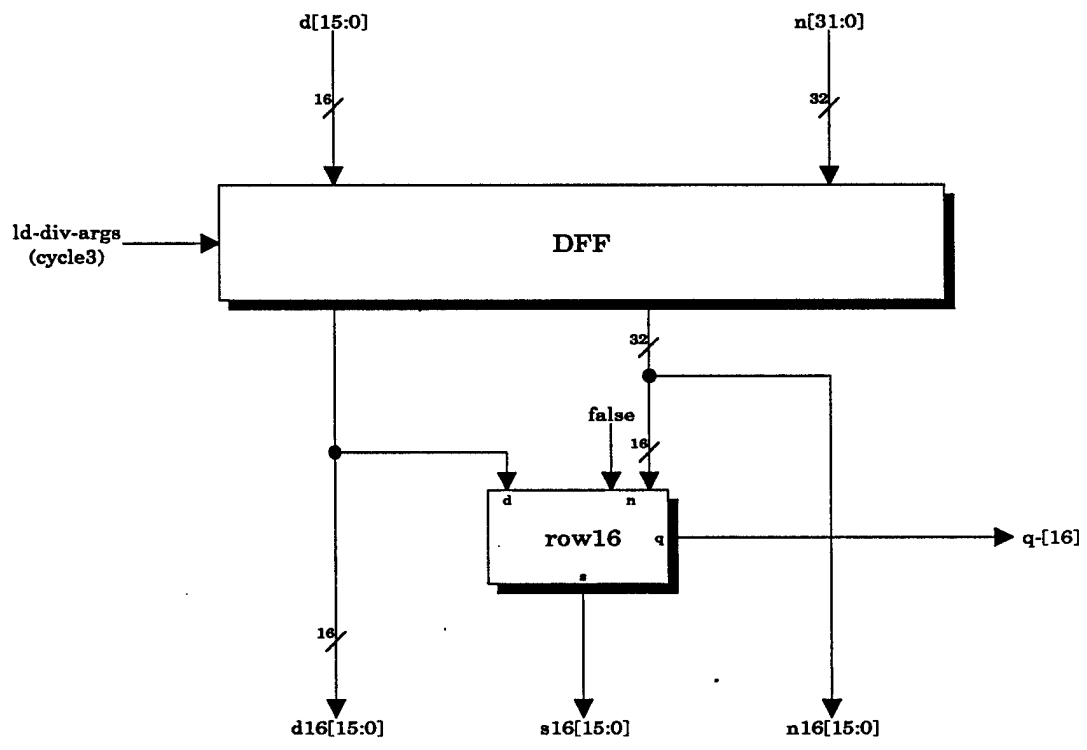






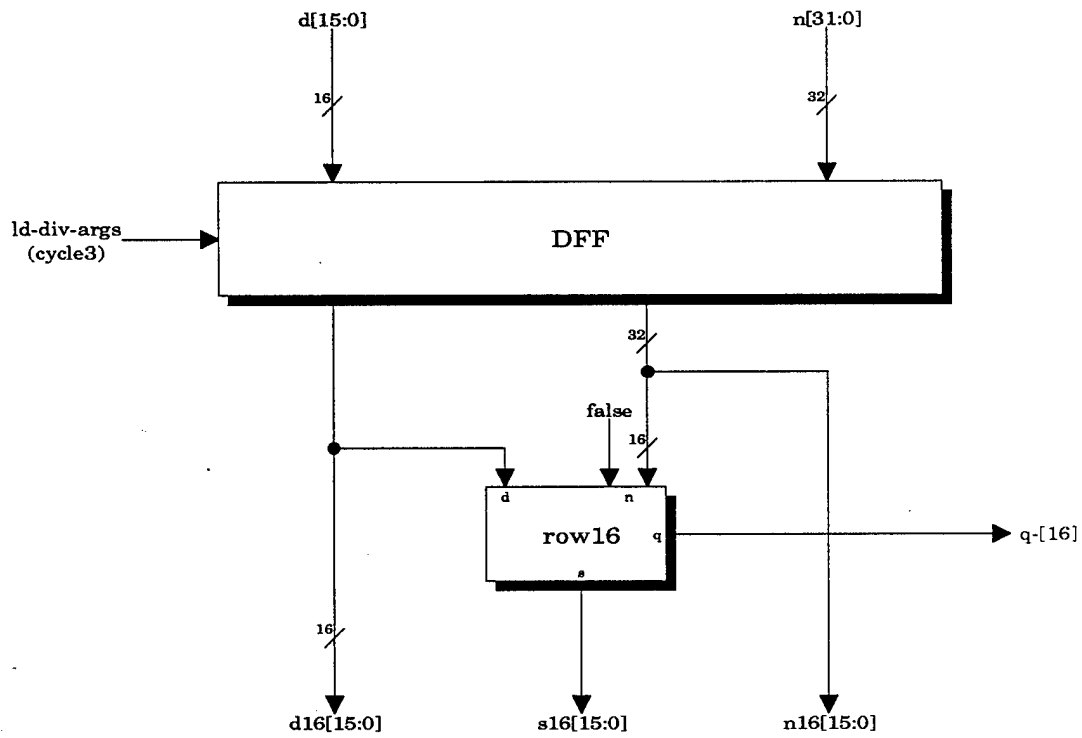


math/strob



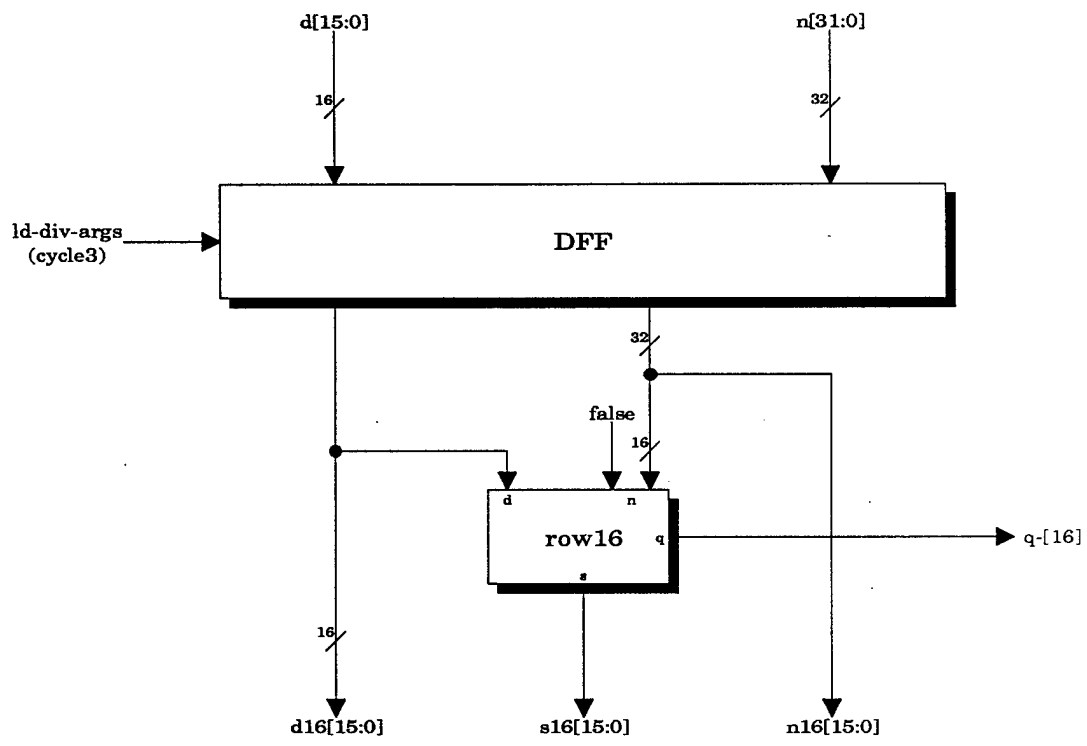
math/divider/Row16

Des: d:\jackson\pnm\row16.drw  
Gen: cchip\math\dividerrow16



math/divider/Row16

Dos: d:\jackson\prem\row16.drw  
Gen: <chip>math/divider/row16



**math/divider/Row16**

Doc: d:\jackson\pre\row16.drw  
Gen: <chip>math/divider/row16