GEORGIA TECH GT-VSM8

VLSI DESIGN VERIFICATION DOCUMENT

VLSI DEVELOPMENT REPORT

REPORT NO. VDR-0142-90-003

JUNE 8, 1990

GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY

Contract No. DASG60-89-C-0142

Sponsored By

The United States Army Strategic Defense Command

COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology

Atlanta, Georgia 30332 - 0540

Contract Data Requirements List Item A006

Period Covered: Not Applicable

Type Report: As Required

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Wei Siong Tan

COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology

Atlanta, Georgia 30332 - 0540

Eugene L. Sanders	Cecil O. Alford
USASDC	Georgia Tech
Contract Monitor	Project Director

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VLSI DESIGN VERIFICATION DOCUMENT

1.0 INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems/Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech eight point crossbar switch chip, GT-VSM8.

TABLE 1. GEORGIA TECH CHIP SET FOR AHAT

Design	DV PASSED	TAPE DELIV.	FABRICATED	TESTED
GT-VFPU	1/17/89	5/10/90	5/19/89	4/4/90
GT-VNUC				
GT-VTF				
GT-VTHR				
GT-VCLS	1/26/90			
GT-VCTR	2/8/90			
GT-VIAG				
GT-VDAG				
GT-VSNI	1/17/89	5/23/89	4/14/89	4/4/90
GT-VSM8	1/17/89	6/8/90	5/6/89	4/4/90
GT-VSF	9/12/89			

1. Scheduled March 31, 1991
2. Scheduled December 31, 1990

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DESIGN VERIFICATION CHECKLIST

1. DV CONTROL NUMBER : _____ (Assigned by SCS)

2. CUSTOMER INFORMATION

Customer Name: Georgia Tech Chip Name: transfer(GT-VSM8/1)

Project Manager: Cecil O. Alford Phone: 894-2505

Design Engineer: Amar Ghori Phone: 894-7472

_____ Phone: _____

Test Engineer : Amar Ghori Phone: 894-7472

3. SCS CONTACT: Girish Kumar

4. REGRESSION

4.1 GENESIL Version: 7.0
4.2 Name of Session Log from recompile: DV-Session.Log
4.3 Include DV_regression.001?: _____ (simulation and timing)
4.4 Size of database: 45M Density: 6250___ 1600___ TK50 x

5. FUNCTIONAL INFORMATION (check when included)

5.1 Key Parameters : x
5.2 DV_pin_description : x
5.3 Block Diagram : x
5.4 Functional Description : x
5.4 Timing Diagrams at Pins : _____
5.6 Annotated Views : x Annotated Schematics: x

6. PHYSICAL INFORMATION

6.1 Fabline : NSC-CN12A

6.2 Plots: (check when included or indicate filename)
Chip Route (D size): x Bonding Diagram (B size) : x
Route Bonding
Filename: xferplt_1.031 Filename: xferbond_1.031

6.3 Die Size: Reported Die Size: 337.9 x 325.7
Maximum Acceptable Die Size: 337.9 x 325.7
Minimum Acceptable Die Size: _____

6.4 GENESIL Package Name : CPGA100C Spec included?: yes
Cavity/Well Size : 433 mils by 433 mils

6.5 External Block: None

7. ELECTRICAL INFORMATION

7.1 Chip Frequency
Specified in netlist: 10(default) Target frequency: 60.9ns

7.2 Power Dissipation: GENESIL= 0.8 W at 10 MHz Spec=____ W at ____ MHz

7.3 Operating Voltage: from 4.5 Volts to 5.5 Volts

8. SIMULATION

8.1 Number of Clocking Regimes : single

	Clock Pad Name	DIV/NO_DIV	Ext Clock Name	Int PHASE_A/PHASE_B Name
1.	Clock pad	NO	Net_clk	Phase-A/Phase-B
2.				
3.				
4.				
5.				

8.2 Simulation Setup Files:

Name: _____ Listings attached: _____

Description: _____

Affected Tests: _____

Name: _____ Listings attached: _____

Description: _____

Affected Tests: _____

Name: _____ Listings attached: _____

Description: _____

Affected Tests: _____

8.3 Test Vector Set:

NOTE: Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz.
Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name: runvecs_obj.001 No of vectors: _____
Generated using MASM: x traceobj: x other: command file
Timing Resolution: phase _____ cycle _____ other: _____
Description: This file runs all trace obj test vector files. To run, enter simulation environment and execute $source runvecs_obj.

Portions of Chip Tested: All

Use for switch level simulation? Y N
Use for tester? Y N

2. Name: runvecs-n.001 No of vectors: _____
Generated using MASM: x traceobj: x other: command file
Timing Resolution: phase _____ cycle _____ other: _____
Description: This file runs all test vectors in the normal mode. Execute $source runvecs_n

Portions of Chip Tested: all

Use for switch level simulation? Y N
Use for tester? Y N

3. Name: _____ No of vectors: _____
Generated using MASM: _____ traceobj: _____ other: _____
Timing Resolution: phase _____ cycle _____ other: _____
Description: _____

Portions of Chip Tested: _____

Use for switch level simulation? Y N
Use for tester? Y N

4. Name: _____ No of vectors: _____
Generated using MASH: _____ traceobj: _____ other: _____
Timing Resolution: phase _____ cycle _____ other: _____
Description: _____
_____
_____

Portions of Chip Tested: _____
_____

Use for switch level simulation? Y N
Use for tester? Y N

5. Name: _____ No of vectors: _____
Generated using MASH: _____ traceobj: _____ other: _____
Timing Resolution: phase _____ cycle _____ other: _____
Description: _____
_____

Portions of Chip Tested: _____
_____

Use for switch level simulation? Y N
Use for tester? Y N

6. Name: _____ No of vectors: _____
Generated using MASH: _____ traceobj: _____ other: _____
Timing Resolution: phase _____ cycle _____ other: _____
Description: _____
Description: _____
_____
_____

Portions of Chip Tested: _____
_____

Use for switch level simulation? Y N
Use for tester? Y N

7. Name: _____ No of vectors: _____
Generated using MASH: _____ traceobj: _____ other: _____
Timing Resolution: phase _____ cycle _____ other: _____
Description: _____
_____
_____

Portions of Chip Tested: _____
_____

Use for switch level simulation? Y N
Use for tester? Y N

9. TIMING ANALYSIS

9.1 Environment

Temperature Coefficient: 35 Degree C / Watt (theta_JA)
Operating Temp : from 0 C (min) to 70 C (max)
Operating Voltage : from 4.5 V (min) to 5.5 V (max)

room junction temp = 25 + (theta_JA * Power) = 53 degrees C
maximum junction temp =
maximum ambient temp + (theta_JA * Power) = 98 degrees C

9.2 Include the following reports:

guaranteed model 5.0V room temp (53°c)	guaranteed model min operating V max junction temp (98°c)	target model min operating V max junction temp
Cycle:	Cycle:	Cycle:
Setup/Hold:	Setup/Hold:	Setup/Hold:
Output Delay:	Output Delay:	Output Delay:
Path Delay:	Path Delay:	Path Delay:

9.3 Setup Files:

Name:
Description :

Name:
Description :

Name:
Description :

Name:
Description :

9.4 Critical Boundary Conditions:

List critical paths here or annotate the timing report.
Attach additional pages if needed.

Clocks

	report	limit
1. Phase 1 High		
2. Phase 2 High		
3. Symmetric Cycle		
4. Minimum Cycle		

Outputs

	Signal Name	load (pF)	delay	limit
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				

Inputs

	Signal Name	setup	hold	limit
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				

9.5 Hold Time Violations: _____

10. DC CHARACTERISTICS - CMOS

PARAMETERS	DESCRIPTION	CONDITIONS 0 to 70	CONDITIONS -55 to +125	MIN	MAX
DATA PAD INPUT ONLY					
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	-100uA	100uA
CIN	Input Capacitance				6.0pf
DATA PAD OUTPUT ONLY					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
IOZ	Output Leakage current(high Z)	VSS<Vout<VDD	VSS<Vout<VDD	-100uA	100uA
COUT	Output Capacitance				7.0pf
DATA PAD INPUT/OUTPUT					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IOZ	Output leakage current (high Z)	VSS<Vout<VDD	VSS<Vout<VDD	-100uA	100uA
CIO	Input/Output Capacitance				7.0pf
CLOCK PAD					
VIH	Input High Voltage			3.9V	
VIL	Input Low Voltage				0.6V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	-100uA	100uA
CIN	Input Capacitance				15pf

NOTE: All parameters are measured at a supply voltage of VDD = 5V +/- 10% and a junction temperature of 125 C.

11. TAPEOUT AND TESTING SPECIFICATION

Prototype Brokerage Service Purchased? _____yes _____no
If yes: PO #_____

12. CUSTOMER CHECKLIST COMMENTS

Pre-Verification Comments

_____

_____

_____

_____

_____

13. CUSTOMER CHECKLIST APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Brokerage Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : _____ Date ___/___/___

Title : _____

14. SCS CHECKLIST APPROVAL

Pre-Verification Comments

_____

_____

_____

_____

_____

SCS Approval : Matthew S. Buehring Date 6/8/88

Title : FAE. Southeast

```
) Key Parameters for Chip ~transfer/transfer/transfer
) ----------------------------------------
)
) ROUTE_VERSION = 87.20
) HEIGHT = 325.7 MILS
)    ( = 8272.78 u )
) WIDTH = 337.9 MILS
)    ( = 8582.65 u )
) ROUTED = 1 (0=NO,1=YES)
) TOTAL_WIRE_LENGTH = 431493 MILS
)    ( = 10959922. u )
) CORE_AREA = 85185.4 SQUARE_MILS
)    ( = 54958212. u2 )
) PADRING_AREA = 24849.8 SQUARE_MILS
)    ( = 16032097. u2 )
) PAD_AREA = 20422.4 SQUARE_MILS
)    ( = 13175716. u2 )
) ROUTE_AREA = 35470.3 SQUARE_MILS
)    ( = 22884019. u2 )
) PERCENT_ROUTING_OF_CORE = 41 %
) PERCENT_ROUTING_OF_CHIP = 32 %
) PERCENT_CORE_OF_CHIP = 77 %
) PERCENT_PADRING_OF_CHIP = 22 %
) PERCENT_PAD_OF_PADRING = 82 %
)
) NETLIST_VERSION = 1.0
) NETLIST_EXISTS = 1 (0=NO,1=YES)
)
) PHASE_A_TIME = 16.3 NANOSECONDS
) PHASE_B_TIME = 20.1 NANOSECONDS
) SYMMETRIC_TIME = 60.9 NANOSECONDS
) NUMBER_OF_TRANSISTORS = 49967
) **** ctrl-Z ****
) ** foreground **
) POWER_DISSIPATION = 805.87 MILLIWATTS_@5V_10MHZ
)
)
) ROUTE_ESTIMATE_LVL = 0
) FLAT_ROUTE = 1 (0=NO,1=YES)
) TECHNOLOGY_NAME = CMOS-1
) PACKAGE_SPECIFIED = 1 (0=NO,1=YES)
) PACKAGE_NAME = CPGA100e
) FABLINE_NAME = NSC_CN12A
) COMPILER_TYPE = GCX
)
) FLOORPLAN_VERSION = 7.0
) BOND_PAD_CNT = 99
) HEIGHT_ESTIMATE = 162.69 MILS
)    ( = 4132.326 u )
) WIDTH_ESTIMATE = 168.71 MILS
)    ( = 4285.234 u )
) FUSED = 1 (0=NO,1=YES)
) FUSION_REQUIRED = 1 (0=NO,1=YES)
) PINOUT = 1 (0=NO,1=YES)
) PINOUT_REQUIRED = 1 (0=NO,1=YES)
```

```
) PLACED = 1 (0=NO,1=YES)
) PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
)
)
) DOWN_BONDS_ALLOWED = 1 (0=NO,1=YES)
) PKG_PIN_COUNT = 100
) PKG_WELL_HEIGHT = 434.00 MILS
)    ( = 11023.60 u )
) PKG_WELL_WIDTH = 434.00 MILS
)    ( = 11023.60 u )
) AREA = 110054.0 SQUARE_MILS
)    ( = 71002439.9 u2 )
) OBJECT_TYPE = Chip
) AREA_PER_TRANSISTOR = 2.202534 SQUARE_MILS
)    ( = 1420.98683 u2 )
) PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
) CHECKPOINTS_EXIST = 1 (0=NO,1=YES)
) Genesil internal fault:  Please file a bug report, if needed.
) c_spawn_sub: oops -3:
) program 'UTIL' was aborted by Unix
) )Program EXEC
) **** ctrl-Z ****
) ** foreground **
EXIT_GENESIL
c
K EP_LOG
) End of GENESIL session '7_Jun_2'
```

```
**********************************************************************************
Chip: ~transfer/transfer/transfer                                    Timing Analyzer
- ------------------------Genesil Version v7.0_Beta---------------------------
CLOCK REPORT MODE
--------------------------------------------------------------------------------
Pipeline: NSC_CN12A                      Corner: GUARANTEED
  Junction Temperature:75 degree C       Voltage:5.00v
  External Clock: Net_clk
 Included setup files: default setup file
- --------------------------------------------------------------------------------
                              CLOCK TIMES (minimum)
Phase 1 High:    16.3   ns              Phase 2 High:    20.1   ns
              ----------                              ----------
Cycle (from Ph1):    49.9   ns         Cycle (from Ph2):    60.9   ns
              ----------                              ----------
Minimum Cycle Time:    60.9   ns       Symmetric Cycle Time:          ns
                    ----------                              ----------
--------------------------------------------------------------------------------
                              CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    16.3   ns set by:
                              ----------
  ** Clock delay: 5.2ns (21.5-16.3)
   Node                              Cumulative Delay      Transition
   host_output/(internal)                 21.5                rise
   host_output/dataout[0]                 19.7                fall
   host_output/dataout[0]'                19.5                fall
   host_output/address_sync[0]            11.9                fall
   host_interface/address_sync[0]         10.6                fall
   <st_interface/address_sync[0]'          8.1                fall
   host_interface/PHASE_A                  5.2                rise
   clock_pad/PHASE_A                       1.2                rise
   Net_clk                                 0.0                rise

Minimum Phase 2 high time is    20.1   ns set by:
                              ----------
  ** Clock delay: 5.2ns (25.3-20.1)
   Node                              Cumulative Delay      Transition
   host_interface/(internal)              25.3                rise
--------------------------------------------------------------------------------
 INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
- --------------------------------------------------------------------------------
BACK            PHASE1_HIGH     CYCLE_PH1       DUMP_LATCH_THRESHOLD
                PHASE2_HIGH     CYCLE_PH2       DUMP_LATCH


--------------------------------------------------------------------------------


>TIMING>CLOCKS>
```

```
**********************************************************************************
Chip: ~transfer/transfer/transfer                                    Timing Analyzer
- ------------------------Genesil Version v7.0_Beta----------------------------
   host_interface/(internal)          25.3                rise
   host_interface/data_in[0]          23.8                fall
   data_pad[0]/data_in                23.7                fall
   data_pad[0]/data_in'               23.3                fall
   Data[0]                            19.6                fall
   data_pad[0]/read_disable           11.3                fall
   host_interface/read_disable        11.2                fall
   host_interface/read_disable'        6.6                fall
   host_interface/chip_select          6.1                rise
   host_interface/chip_select'         5.1                rise
   host_interface/n_chip_select        4.2                fall
   n_chip_select/n_chip_select         4.1                fall
   n_chip_select/n_chip_select'        3.6                fall
   N_chip_select                       0.0                fall

Minimum cycle time (from Ph1) is   49.9    ns set by:
                                   ----------

  ** Clock delay: 5.1ns (55.0-49.9)
   Node                          Cumulative Delay      Transition
   switch4/switch_mux/latch/1          55.0                fall
   *</switch_mux/latch/(internal)      53.0                rise
   <witch_mux/latch/internal_xfer      52.5                fall
   switch4/control/internal_xfer       52.4                fall
   switch4/control/internal_xfer'      51.7                fall
   switch4/control/int_xfer            49.7                fall
   switch4/control/int_xfer'           49.6                fall
   switch4/control/state_detect        48.3                fall
   state_machine/state_detect          45.0                fall
   state_machine/state_detect'         13.5                fall
   state_machine/not_run               11.6                fall
   run_control/not_run                 11.4                fall
   run_control/not_run'                10.3                fall
   run_control/run                      9.9                rise
   run_control/run'                     9.6                rise
   run_control/PHASE_A                  5.3                rise
--------------------------------------------------------------------------------
  INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
  ------------------------------------------------------------------------------
BACK            PHASE1_HIGH     CYCLE_PH1       DUMP_LATCH_THRESHOLD
                PHASE2_HIGH     CYCLE_PH2       DUMP_LATCH


--------------------------------------------------------------------------------


>TIMING>CLOCKS>
```

```
**********************************************************************
Chip: ~transfer/transfer/transfer                          Timing Ana
----------------------------Genesil Version v7.0_Beta----------+----------
 serial in[5]    Serial in          15.9     15.9              BLOCK NA
   serial out[3]    Serial out          15.9     15.9  PATH*CURRENT*
 serial in[5]    Serial in          19.1     19.3              address_pac
   serial out[4]    Serial out          19.1     19.3  PATHaddress_pac
 serial in[5]    Serial in          18.0     18.2              address_pac
   serial out[5]    Serial out          18.0     18.2  PATHaddress_pac
 serial in[5]    Serial in          17.3     17.4              address_pac
   serial out[6]    Serial out          17.3     17.4  PATHaddress_pac
 serial in[5]    Serial in          16.5     16.6              chip_contr
   serial out[7]    Serial out          16.5     16.6  PATHclock_pad
 serial in[6]    Serial in           ---      ---              data_pad[0
   *CURRENT*        Address[0]           ---      ---  PATHdata_pad[1
 serial in[6]    Serial in          16.8     17.0              data_pad[2
   serial out[0]    Serial out          16.8     17.0  PATHdata_pad[3
 serial in[6]    Serial in          16.1     16.2              data_pad[4
   serial out[1]    Serial out          16.1     16.2  PATHdata_pad[5
 serial in[6]    Serial in          15.6     15.7              data_pad[6
   serial out[2]    Serial out          15.6     15.7  PATHdata_pad[7
 serial in[6]    Serial in          15.5     15.6              dav_mux
   serial out[3]    Serial out          15.5     15.6  PATHdav_pad[0]
 serial in[6]    Serial in          18.7     19.0              dav_pad[1]
   serial out[4]    Serial out          18.7     19.0  PATHdav_pad[2]
 serial in[6]    Serial in          17.7     17.9              dav_pad[3]
   serial out[5]    Serial out          17.7     17.9  PATHdav_pad[4]
 serial in[6]    Serial in          16.9     17.1              dav_pad[5]
   serial out[6]    Serial out          16.9     17.1  PATHdav_pad[6]
 serial in[6]    Serial in          16.2     16.3              dav_pad[7]
   serial out[7]    Serial out          16.2     16.3  PATHhost_inter
 serial in[7]    Serial in          16.8     16.9              host_outpu
   serial out[0]    Serial out          16.8     16.9  PATHn_chip_sel
 serial in[7]    Serial in          16.1     16.2              n_mem_read
   serial out[1]    Serial out          16.1     16.2  PATHn_mem_writ
 serial in[7]    Serial in          15.6     15.6              n_xack_pad
   serial out[2]    Serial out          15.6     15.6  PATHnet_sync_p
 serial in[7]    Serial in          15.5     15.5               * MORE *
----------------------------------------------------------+----------
 INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      U
----------------------------------------------------------------------
BACK            PATH_DELETE_TOGGLE



----------------------------------------------------------------------

Enter [string]:
>TIMING>PATH DELAY>
```

```
**********************************************************************
Chip: ~transfer/transfer/transfer                          Timing Analyzer
----------------------Genesil Version v7.0_Beta----------------------
OUTPUT DELAY MODE
----------------------------------------------------------------------
Fabline: NSC_CN12A                    Corner: GUARANTEED
Function Temperature:75 degree C      Voltage:5.00v
External Clock: Net_clk
Included setup files: default setup file
----------------------------------------------------------------------
```

OUTPUT DELAYS (ns)

Output	Ph1(r) Delay Min	Ph1(r) Delay Max	Ph2(r) Delay Min	Ph2(r) Delay Max	Loading(pf)	
Data[0]	0.0		0.0		50.00	PATH
Data[1]	0.0	32.2	0.0	19.6	50.00	PATH
Data[2]	0.0	32.0	0.0	19.6	50.00	PATH
Data[3]	0.0	31.8	0.0	19.6	50.00	PATH
Data[4]	0.0	31.6	0.0	19.6	50.00	PATH
Data[5]	0.0	31.5	0.0	19.6	50.00	PATH
Data[6]	0.0	31.4	0.0	19.6	50.00	PATH
Data[7]	0.0	31.3	0.0	19.6	50.00	PATH
N_xack	14.8		14.8		50.00	PATH
N_t_run	15.1		---	---	50.00	PATH
N_t_sync	16.9		---	---	50.00	PATH
Node_error[0]	12.9		---	---	50.00	PATH
Node_error[1]	12.9	15.7	---	---	50.00	PATH
Node_error[2]	12.9	15.7	---	---	50.00	PATH
Node_error[3]	12.9	15.7	---	---	50.00	PATH
Node_error[4]	12.9	15.7	---	---	50.00	PATH
Node_error[5]	12.9	15.7	---	---	50.00	PATH
Node_error[6]	12.9	15.6	---	---	50.00	PATH
Node_error[7]	12.8	15.6	---	---	50.00	PATH
Serial_out[0]	16.8	36.1	16.8	18.3	50.00	PATH
Serial_out[1]	16.1	35.2	16.1	17.9	50.00	PATH
Serial_out[2]	15.6	34.1	15.6	17.4	50.00	PATH
Serial_out[3]	15.5	33.4	15.5	17.4	50.00	PATH
Serial_out[4]	18.7	38.0	18.7	20.8	50.00	PATH
Serial_out[5]	17.6	37.0	17.6	19.8	50.00	PATH

```
----------------------------------------------------------------------
  INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
----------------------------------------------------------------------
BACK


----------------------------------------------------------------------


>TIMING>OUTPUT DELAY>
```

```
**********************************************************************************
Chip: ~transfer/transfer/transfer                                  Timing Analyzer
-------------------------Genesil Version v7.0_Beta--------------------------
Node_error[5]                12.9     15.7      ---      ---       50.00   PATH
Node_error[6]                12.9     15.6      ---      ---       50.00   PATH
Node_error[7]                12.8     15.6      ---      ---       50.00   PATH
Serial_out[0]                16.8     36.1     16.8     18.3       50.00   PATH
Serial_out[1]                16.1     35.2     16.1     17.9       50.00   PATH
Serial_out[2]                15.6     34.1     15.6     17.4       50.00   PATH
Serial_out[3]                15.5     33.4     15.5     17.4       50.00   PATH
Serial_out[4]                18.7     [redacted]  18.7  [redacted]  50.00   PATH
Serial_out[5]                17.6     37.0     17.6     19.8       50.00   PATH
Serial_out[6]                16.9     32.9     16.9     19.1       50.00   PATH
Serial_out[7]                16.1     31.5     16.1     18.6       50.00   PATH
Switch_error[0]              12.8     [redacted]  ---      ---     50.00   PATH
Switch_error[1]              12.8     15.6      ---      ---       50.00   PATH
Switch_error[2]              12.8     15.6      ---      ---       50.00   PATH
Switch_error[3]              12.8     15.6      ---      ---       50.00   PATH
Switch_error[4]              12.9     15.7      ---      ---       50.00   PATH
Switch_error[5]              12.9     15.7      ---      ---       50.00   PATH
Switch_error[6]              12.8     15.6      ---      ---       50.00   PATH
Switch_error[7]              12.8     15.6      ---      ---       50.00   PATH
Transfer_in[0]                9.9     14.0      ---      ---       50.00   PATH
Transfer_in[1]                9.8     13.9      ---      ---       50.00   PATH
Transfer_in[2]                9.6     13.7      ---      ---       50.00   PATH
Transfer_in[3]                9.5     13.6      ---      ---       50.00   PATH
Transfer_in[4]                9.8     13.9      ---      ---       50.00   PATH
Transfer_in[5]                9.9     14.1      ---      ---       50.00   PATH
Transfer_in[6]               10.1     14.2      ---      ---       50.00   PATH
Transfer_in[7]               10.2               ---      ---       50.00   PATH
Transfer_out[0]              11.0               ---      ---       50.00   PATH
Transfer_out[1]              10.7     14.8      ---      ---       50.00   PATH
Transfer_out[2]              10.6     14.7      ---      ---       50.00   PATH
Transfer_out[3]              10.5     14.6      ---      ---       50.00   PATH
Transfer_out[4]              10.4     14.5      ---      ---       50.00   PATH
Transfer_out[5]              10.2     14.3      ---      ---       50.00   PATH
Transfer_out[6]              10.1     14.2      ---      ---       50.00   PATH
Transfer_out[7]              10.0     14.1      ---      ---       50.00   PATH
--------------------------------------------------------------------------------
 INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
--------------------------------------------------------------------------------
BACK


--------------------------------------------------------------------------------


>TIMING>OUTPUT DELAY>
```

```
**********************************************************************************
Chip: ~transfer/transfer/transfer                                    Timing Analyzer
-------------------------Genesil Version v7.0_Beta--------------------------
SETUP AND HOLD MODE
--------------------------------------------------------------------------------
I bline: NSC_CN12A                        Corner: GUARANTEED
  Junction Temperature:75 degree C        Voltage:5.00v
  External Clock: Net_clk
 Included setup files: default setup file
--------------------------------------------------------------------------------
                        INPUT SETUP AND HOLD TIMES (ns)
Input                     Setup Time          Hold Time
                        Ph1(f)   Ph2(f)     Ph1(f)   Ph2(f)
Address[0]                ---      4.8        ---      -1.3      PATH
Address[1]                ---      4.6        ---      -1.1      PATH
 ldress[2]                ---      4.5        ---      -1.0      PATH
 ldress[3]                ---      [redacted] ---      -1.6      PATH
Address[4]                ---      5.0        ---      -1.5      PATH
 ldress[5]                ---      4.9        ---      -1.4      PATH
 ata[0]                   ---      [redacted] ---       2.0      PATH
Data[1]                   ---      1.4        ---       2.0      PATH
Data[2]                   ---      1.4        ---       2.1      PATH
 ata[3]                   ---      1.3        ---       2.2      PATH
 ata[4]                   ---      1.2        ---       [redacted] PATH
Data[5]                   ---      1.2        ---       2.3      PATH
 ata[6]                   ---      1.2        ---       2.3      PATH
 ata[7]                   ---      1.3        ---       2.2      PATH
Dav[0]                    ---      1.4        ---       [redacted] PATH
Dav[1]                    ---      1.4        ---       0.3      PATH
 av[2]                    ---      1.4        ---       0.2      PATH
Dav[3]                    ---      1.5        ---       0.2      PATH
Dav[4]                    ---      1.8        ---      -0.1      PATH
 av[5]                    ---      1.9        ---      -0.2      PATH
 av[6]                    ---      1.9        ---      -0.2      PATH
Dav[7]                    ---                 ---      -0.3      PATH
 _chip_select             ---                 ---      -0.0      PATH
 _mem_read                ---                 ---       1.6      PATH
N_mem_write               ---                 ---       1.4      PATH
--------------------------------------------------------------------------------
 INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
--------------------------------------------------------------------------------
BACK

--------------------------------------------------------------------------------


>TIMING>SETUP HOLD>
```

```
**********************************************************************************
Chip: ~transfer/transfer/transfer                                    Timing Analyzer
- ------------------------Genesil Version v7.0_Beta----------------------------
Data[0]                    ---      1.5        ---       2.0        PATH
Data[1]                    ---      1.4        ---       2.0        PATH
D ta[2]                    ---      1.4        ---       2.1        PATH
D ta[3]                    ---      1.3        ---       2.2        PATH
Data[4]                    ---      1.2        ---       2.3        PATH
D-ta[5]                    ---      1.2        ---       2.3        PATH
D ta[6]                    ---      1.2        ---       2.3        PATH
Data[7]                    ---      1.3        ---       2.2        PATH
Dav[0]                     ---      1.4        ---       0.3        PATH
D v[1]                     ---      1.4        ---       0.3        PATH
D_v[2]                     ---      1.4        ---       0.2        PATH
Dav[3]                     ---      1.5        ---       0.2        PATH
D v[4]                     ---      1.8        ---      -0.1        PATH
D v[5]                     ---      1.9        ---      -0.2        PATH
Dav[6]                     ---      1.9        ---      -0.2        PATH
Dav[7]                     ---      2.0        ---      -0.3        PATH
N chip_select              ---     20.1        ---      -0.0        PATH
N_mem_read                 ---     19.3        ---       1.6        PATH
N_mem_write                ---     18.6        ---       1.4        PATH
F i[0]                     ---      [redacted] ---      -0.8        PATH
F i[1]                     ---      2.5        ---      -0.8        PATH
Rfi[2]                     ---      2.5        ---      -0.7        PATH
F i[3]                     ---      2.4        ---      -0.7        PATH
F i[4]                     ---      2.4        ---      -0.7        PATH
Rfi[5]                     ---      2.4        ---      -0.6        PATH
Rfi[6]                     ---      2.3        ---      -0.6        PATH
F i[7]                     ---      2.3        ---      -0.6        PATH
Serial_in[0]               ---      0.7        ---      [redacted]  PATH
Serial_in[1]               ---      1.3        ---       1.6        PATH
S rial_in[2]               ---      [redacted] ---       1.1        PATH
S rial_in[3]               ---      ---        ---       ---        PATH
Serial_in[4]               ---      ---        ---       ---        PATH
Serial_in[5]               ---      ---        ---       ---        PATH
S rial_in[6]               ---      ---        ---       ---        PATH
Serial_in[7]               ---      ---        ---       ---        PATH
----------------------------------------------------------------------------------
  NSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD       UTILITY
 ---------------------------------------------------------------------------------
BACK


---------------------------------------------------------------------------------


>TIMING>SETUP HOLD>
```

```
**********************************************************************
Chip: ~transfer/transfer/transfer                          Timing Analyzer
- ----------------------Genesil Version v7.0_Beta----------+---------------
PATH DELAY MODE                                            BLOCK NAME
-----------------------------------------------------------*CURRENT*
Pipeline: NSC_CN12A                Corner: GUARANTEED      address_pad[0]
  Junction Temperature:75 degree C Voltage:5.00v           address_pad[1]
  External Clock: Net_clk                                  address_pad[2]
 Included setup files: default setup file                  address_pad[3]
- ----------------------------------------------------------address_pad[4]
                                PATH DELAY (ns)            address_pad[5]
Source Object     Connector          (Ph1) Min     Max     chip_control
   Dest. Object      Connector       (Ph2)   Min     Max   clock_pad
 Serial in[0]     Serial in                 11.6    12.2   data_pad[0]
   serial out[0]    serial out                 11.6    12.2 PATHdata_pad[1]
 Serial in[0]     Serial in                 17.3    17.4   data_pad[2]
   serial out[0]    Serial out                 17.3    17.4 PATHdata_pad[3]
serial in[0]      Serial in                 16.7    16.8   data_pad[4]
   serial out[1]    Serial out                 16.7    16.8 PATHdata_pad[5]
 Serial in[0]     Serial in                 16.3    16.3   data_pad[6]
   serial out[2]    Serial out                 16.3    16.3 PATHdata_pad[7]
serial in[0]      Serial in                 16.2    16.3   dav_mux
   serial out[3]    Serial out                 16.2    16.3 PATHdav_pad[0]
 Serial in[0]     Serial in                  ---     ---   dav_pad[1]
   *CURRENT*        Address[0]                 ---     --- PATHdav_pad[2]
 Serial in[0]     Serial in                 19.5    19.8   dav_pad[3]
   serial out[4]    Serial out                 19.5    19.8 PATHdav_pad[4]
*CURRENT*         Address[0]                  0.0     0.0   dav_pad[5]
   *CURRENT*        Address[0]                  0.0     0.0 PATHdav_pad[6]
 Serial in[0]     Serial in                 18.5    18.7   dav_pad[7]
   serial out[5]    Serial out                 18.5    18.7 PATHhost_interface
serial in[0]      Serial in                 17.8    17.9   host_output
   serial out[6]    Serial out                 17.8    17.9 PATHn_chip_select
 Serial in[0]     Serial in                 17.3    17.4   n_mem_read
   serial out[7]    Serial out                 17.3    17.4 PATHn_mem_write
 Serial in[1]     Serial in                 17.7    17.8   n_xack_pad
   serial out[0]    Serial out                 17.7    17.8 PATHnet_sync_pad
 Serial in[1]     Serial in                 17.2    17.3     * MORE *
-----------------------------------------------------------+---------------
 INSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
- ----------------------------------------------------------------------------
BACK            PATH_DELETE_TOGGLE


----------------------------------------------------------------------------

Enter [string]:
>TIMING>PATH DELAY>
```

```
**************************************************************************
Chip: ~transfer/transfer/transfer                          Timing Analyzer
-----------------------Genesil Version v7.0_Beta----------+---------------
 serial in[1]   Serial in                  17.2    17.3          BLOCK NAME
   serial out[1]   Serial out                  17.2    17.3  PATH*CURRENT*
 erial in[1]   Serial in                   16.8    16.8          address_pad[0]
   serial out[2]   Serial out                  16.8    16.8  PATHaddress_pad[1]
 serial in[1]   Serial in                  16.8    16.8          address_pad[2]
   serial out[3]   Serial out                  16.8    16.8  PATHaddress_pad[3]
 erial in[1]   Serial in                   20.1    20.3          address_pad[4]
   serial out[4]   Serial out                  20.1    20.3  PATHaddress_pad[5]
 erial in[1]   Serial in                   19.1    19.3          chip_control
   serial out[5]   Serial out                  19.1    19.3  PATHclock_pad
 erial in[1]   Serial in                   18.4    18.5          data_pad[0]
   serial out[6]   Serial out                  18.4    18.5  PATHdata_pad[1]
 erial in[1]   Serial in                   18.0    18.1          data_pad[2]
   serial out[7]   Serial out                  18.0    18.1  PATHdata_pad[3]
 serial in[2]   Serial in                  18.2    18.3          data_pad[4]
   serial out[0]   Serial out                  18.2    18.3  PATHdata_pad[5]
 erial in[2]   Serial in                   17.8    17.9          data_pad[6]
   serial out[1]   Serial out                  17.8    17.9  PATHdata_pad[7]
 serial in[2]   Serial in                  17.4    17.4          dav_mux
   serial out[2]   Serial out                  17.4    17.4  PATHdav_pad[0]
 erial in[2]   Serial in                   17.3    17.4          dav_pad[1]
   serial out[3]   Serial out                  17.3    17.4  PATHdav_pad[2]
 erial in[2]   Serial in                   20.5    20.8          dav_pad[3]
   serial out[4]   Serial out                  20.5          PATHdav_pad[4]
 serial in[2]   Serial in                  19.6    19.8          dav_pad[5]
   serial out[5]   Serial out                  19.6    19.8  PATHdav_pad[6]
 erial in[2]   Serial in                   19.0    19.1          dav_pad[7]
   serial out[6]   Serial out                  19.0    19.1  PATHhost_interface
 serial in[2]   Serial in                  18.5    18.6          host_output
   serial out[7]   Serial out                  18.5    18.6  PATHn_chip_select
 erial in[3]   Serial in                   17.8    18.0          n_mem_read
   serial out[0]   Serial out                  17.8    18.0  PATHn_mem_write
 erial in[3]   Serial in                   17.1    17.2          n_xack_pad
   serial out[1]   Serial out                  17.1    17.2  PATHnet_sync_pad
 serial in[3]   Serial in                  16.6    16.7           * MORE *
-----------------------------------------------------------------+---------
  NSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
--------------------------------------------------------------------------
BACK            PATH_DELETE_TOGGLE


--------------------------------------------------------------------------

Enter [string]:
>TIMING>PATH DELAY>
```

```
**********************************************************************************
Chip: ~transfer/transfer/transfer                                    Timing Analyzer
----------------------Genesil Version v7.0_Beta----------+---------------
serial in[3]   Serial in                    16.6    16.7          BLOCK NAME
  serial out[2]  Serial out                   16.6    16.7  PATH*CURRENT*
serial in[3]   Serial in                    16.5    16.6       address_pad[0]
  serial out[3]  Serial out                   16.5    16.6  PATHaddress_pad[1]
serial in[3]   Serial in                    19.7    20.0       address_pad[2]
  serial out[4]  Serial out                   19.7    20.0  PATHaddress_pad[3]
serial in[3]   Serial in                    18.7    18.9       address_pad[4]
  serial out[5]  Serial out                   18.7    18.9  PATHaddress_pad[5]
serial in[3]   Serial in                    17.9    18.1       chip_control
  serial out[6]  Serial out                   17.9    18.1  PATHclock_pad
serial in[3]   Serial in                    17.2    17.3       data_pad[0]
  serial out[7]  Serial out                   17.2    17.3  PATHdata_pad[1]
serial in[4]   Serial in                    17.4    17.6       data_pad[2]
  serial out[0]  Serial out                   17.4    17.6  PATHdata_pad[3]
serial in[4]   Serial in                    16.7    16.8       data_pad[4]
  serial out[1]  Serial out                   16.7    16.8  PATHdata_pad[5]
serial in[4]   Serial in                    16.2    16.3       data_pad[6]
  serial out[2]  Serial out                   16.2    16.3  PATHdata_pad[7]
serial in[4]   Serial in                    16.1    16.2       dav_mux
  serial out[3]  Serial out                   16.1    16.2  PATHdav_pad[0]
serial in[4]   Serial in                    19.3    19.6       dav_pad[1]
  serial out[4]  Serial out                   19.3    19.6  PATHdav_pad[2]
serial in[4]   Serial in                    18.3    18.5       dav_pad[3]
  serial out[5]  Serial out                   18.3    18.5  PATHdav_pad[4]
serial in[4]   Serial in                    17.5    17.7       dav_pad[5]
  serial out[6]  Serial out                   17.5    17.7  PATHdav_pad[6]
serial in[4]   Serial in                    16.8    16.9       dav_pad[7]
  serial out[7]  Serial out                   16.8    16.9  PATHhost_interface
serial in[5]   Serial in                    17.2    17.3       host_output
  serial out[0]  Serial out                   17.2    17.3  PATHn_chip_select
serial in[5]   Serial in                    16.4    16.5       n_mem_read
  serial out[1]  Serial out                   16.4    16.5  PATHn_mem_write
serial in[5]   Serial in                    15.9    16.0       n_xack_pad
  serial out[2]  Serial out                   15.9    16.0  PATHnet_sync_pad
serial in[5]   Serial in                    15.9    15.9        * MORE *
----------------------------------------------------------+---------------
 NSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
---------------------------------------------------------------------------
BACK            PATH_DELETE_TOGGLE


---------------------------------------------------------------------------

Enter [string]:
>TIMING>PATH DELAY>
```

```
**********************************************************************************
C: ip: ~transfer/transfer/transfer                                  Timing Analyzer
- ------------------------Genesil Version v7.0_Beta----------+----------------
 serial in[5]   Serial in          15.9     15.9          BLOCK NAME
   serial out[3]   Serial out          15.9     15.9  PATH*CURRENT*
  erial in[5]   Serial in          19.1     19.3          address_pad[0]
   serial out[4]   Serial out          19.1     19.3  PATHaddress_pad[1]
 serial in[5]   Serial in          18.0     18.2          address_pad[2]
   serial out[5]   Serial out          18.0     18.2  PATHaddress_pad[3]
  erial in[5]   Serial in          17.3     17.4          address_pad[4]
   serial out[6]   Serial out          17.3     17.4  PATHaddress_pad[5]
 erial in[5]   Serial in          16.5     16.6          chip_control
   serial out[7]   Serial out          16.5     16.6  PATHclock_pad
 serial in[6]   Serial in           ---      ---          data_pad[0]
   *CURRENT*   Address[0]            ---      ---  PATHdata_pad[1]
  erial in[6]   Serial in          16.8     17.0          data_pad[2]
   serial out[0]   Serial out          16.8     17.0  PATHdata_pad[3]
 serial in[6]   Serial in          16.1     16.2          data_pad[4]
   serial out[1]   Serial out          16.1     16.2  PATHdata_pad[5]
  erial in[6]   Serial in          15.6     15.7          data_pad[6]
   serial out[2]   Serial out          15.6     15.7  PATHdata_pad[7]
 erial in[6]   Serial in          15.5     15.6          dav_mux
   serial out[3]   Serial out          15.5     15.6  PATHdav_pad[0]
 erial in[6]   Serial in          18.7     19.0          dav_pad[1]
   serial out[4]   Serial out          18.7     19.0  PATHdav_pad[2]
  erial in[6]   Serial in          17.7     17.9          dav_pad[3]
   serial out[5]   Serial out          17.7     17.9  PATHdav_pad[4]
 serial in[6]   Serial in          16.9     17.1          dav_pad[5]
   serial out[6]   Serial out          16.9     17.1  PATHdav_pad[6]
  erial in[6]   Serial in          16.2     16.3          dav_pad[7]
   serial out[7]   Serial out          16.2     16.3  PATHhost_interface
 serial in[7]   Serial in          16.8     16.9          host_output
   serial out[0]   Serial out          16.8     16.9  PATHn_chip_select
 erial in[7]   Serial in          16.1     16.2          n_mem_read
   serial out[1]   Serial out          16.1     16.2  PATHn_mem_write
  erial in[7]   Serial in          15.6     15.6          n_xack_pad
   serial out[2]   Serial out          15.6     15.6  PATHnet_sync_pad
 serial in[7]   Serial in          15.5     15.5           * MORE *
----------------------------------------------------------+----------------
  NSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
----------------------------------------------------------------------------
BACK            PATH_DELETE_TOGGLE


- ----------------------------------------------------------------------------

Enter [string]:
>TIMING>PATH DELAY>
```

```
Chip: ~transfer/transfer/transfer                                  Timing Analyzer
- ----------------------Genesil Version v7.0_Beta----------+---------------
   serial out[1]   Serial out                    16.1    16.2  PATH   BLOCK NAME
serial in[6]   Serial in                    15.6    15.7        *CURRENT*
   serial out[2]   Serial out                    15.6    15.7  PATHaddress_pad[0]
 erial in[6]   Serial in                    15.5    15.6        address_pad[1]
   serial out[3]   Serial out                    15.5    15.6  PATHaddress_pad[2]
serial in[6]   Serial in                    18.7    19.0        address_pad[3]
   serial out[4]   Serial out                    18.7    19.0  PATHaddress_pad[4]
erial in[6]   Serial in                    17.7    17.9        address_pad[5]
   serial out[5]   Serial out                    17.7    17.9  PATHchip_control
 erial in[6]   Serial in                    16.9    17.1        clock_pad
   serial out[6]   Serial out                    16.9    17.1  PATHdata_pad[0]
serial in[6]   Serial in                    16.2    16.3        data_pad[1]
   serial out[7]   Serial out                    16.2    16.3  PATHdata_pad[2]
 erial in[7]   Serial in                    16.8    16.9        data_pad[3]
   serial out[0]   Serial out                    16.8    16.9  PATHdata_pad[4]
serial in[7]   Serial in                    16.1    16.2        data_pad[5]
   serial out[1]   Serial out                    16.1    16.2  PATHdata_pad[6]
erial in[7]   Serial in                    15.6    15.6        data_pad[7]
   serial out[2]   Serial out                    15.6    15.6  PATHdav_mux
 erial in[7]   Serial in                    15.5    15.5        dav_pad[0]
   serial out[3]   Serial out                    15.5    15.5  PATHdav_pad[1]
serial out[7]   Serial out                     ---     ---        dav_pad[2]
   serial out[4]   Serial out                      ---     ---  PATHdav_pad[3]
 erial in[7]   Serial in                    18.7    18.9        dav_pad[4]
   serial out[4]   Serial out                    18.7    18.9  PATHdav_pad[5]
serial in[7]   Serial in                    17.6    17.8        dav_pad[6]
   serial out[5]   Serial out                    17.6    17.8  PATHdav_pad[7]
 erial in[7]   Serial in                    17.6    17.8        host_interface
   serial out[5]   Serial out                    17.6    17.8  PATHhost_output
erial in[7]   Serial in                    16.9    17.0        n_chip_select
   serial out[6]   Serial out                    16.9    17.0  PATHn_mem_read
serial in[7]   Serial in                    16.1    16.2        n_mem_write
   serial out[7]   Serial out                    16.1    16.2  PATHn_xack_pad
>                                                              net_sync_pad
                                                                * MORE *
-------------------------------------------------------------+---------------
  NSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
- ------------------------------------------------------------------------------
BACK            PATH_DELETE_TOGGLE


------------------------------------------------------------------------------

Enter [string]:
>TIMING>PATH DELAY>
```

```
/*     pad        wire          pin  padx  pady  pinx piny length angle */
BOND Address[0]/Address Address[0] -1 0 0 0 0 0 0
BOND Address[1]/Address Address[1] -1 0 0 0 0 0 0
BOND Address[2]/Address Address[2] -1 0 0 0 0 0 0
BOND Rb[0]/R R[8] -1 0 0 0 0 0 0
BOND Rb[1]/R R[9] -1 0 0 0 0 0 0
BOND Rb[2]/R R[10] -1 0 0 0 0 0 0
BOND Rb[3]/R R[11] -1 0 0 0 0 0 0
BOND Rb[4]/R R[12] -1 0 0 0 0 0 0
BOND Rb[5]/R R[13] -1 0 0 0 0 0 0
BOND Rb[6]/R R[14] -1 0 0 0 0 0 0
BOND Rb[7]/R R[15] -1 0 0 0 0 0 0
BOND N_xack/N_xack N_xack -1 0 0 0 0 0 0
BOND Net_dav/Net_dav Net_dav -1 0 0 0 0 0 0
BOND N_mem_write/N_mem_write N_mem_write -1 0 0 0 0 0 0
BOND Proc_run/Proc_run Proc_run -1 0 0 0 0 0 0
BOND N_chip_select/N_chip_select N_chip_select -1 0 0 0 0 0 0
BOND Transfer_in/Transfer_in Transfer_in -1 0 0 0 0 0 0
BOND Ra[0]/R R[0] -1 0 0 0 0 0 0
BOND Ra[1]/R R[1] -1 0 0 0 0 0 0
BOND Ra[2]/R R[2] -1 0 0 0 0 0 0
BOND Ra[3]/R R[3] -1 0 0 0 0 0 0
BOND Ra[4]/R R[4] -1 0 0 0 0 0 0
BOND Ra[5]/R R[5] -1 0 0 0 0 0 0
BOND Ra[6]/R R[6] -1 0 0 0 0 0 0
BOND Ra[7]/R R[7] -1 0 0 0 0 0 0
BOND Net_rfi/Net_rfi Net_rfi -1 0 0 0 0 0 0
BOND Rfi/Rfi Rfi -1 0 0 0 0 0 0
BOND Net_sync/Net_sync Net_sync -1 0 0 0 0 0 0
BOND Serial_in/Serial_in Serial_in -1 0 0 0 0 0 0
BOND Host_rfi/Host_rfi Host_rfi -1 0 0 0 0 0 0
BOND Host_dav/Host_dav Host_dav -1 0 0 0 0 0 0
BOND Serial_out/Serial_out Serial_out -1 0 0 0 0 0 0
BOND Core_vss/VSS FALSE -1 0 0 0 0 0 0
BOND Ring_vss[0]/VSS FALSE -1 0 0 0 0 0 0
BOND Ring_vss[1]/VSS FALSE -1 0 0 0 0 0 0
BOND Ring_vss[2]/VSS FALSE -1 0 0 0 0 0 0
BOND Ring_vss[3]/VSS FALSE -1 0 0 0 0 0 0
BOND Corner_vdd[0]/VDD TRUE -1 0 0 0 0 0 0
BOND Corner_vdd[1]/VDD TRUE -1 0 0 0 0 0 0
BOND Core_vdd/VDD TRUE -1 0 0 0 0 0 0
BOND Corner_vss[0]/VSS FALSE -1 0 0 0 0 0 0
BOND Corner_vss[1]/VSS FALSE -1 0 0 0 0 0 0
BOND Ring_vdd[0]/VDD TRUE -1 0 0 0 0 0 0
BOND Ring_vdd[1]/VDD TRUE -1 0 0 0 0 0 0
BOND Ring_vdd[2]/VDD TRUE -1 0 0 0 0 0 0
BOND Ring_vdd[3]/VDD TRUE -1 0 0 0 0 0 0
BOND Ring_vdd[4]/VDD TRUE -1 0 0 0 0 0 0
BOND Data[0]/Data Data[0] -1 0 0 0 0 0 0
BOND Data[1]/Data Data[1] -1 0 0 0 0 0 0
BOND Data[2]/Data Data[2] -1 0 0 0 0 0 0
BOND Data[3]/Data Data[3] -1 0 0 0 0 0 0
BOND Data[4]/Data Data[4] -1 0 0 0 0 0 0
BOND Data[5]/Data Data[5] -1 0 0 0 0 0 0
BOND Data[6]/Data Data[6] -1 0 0 0 0 0 0
BOND Data[7]/Data Data[7] -1 0 0 0 0 0 0
BOND Rc[0]/R R[16] -1 0 0 0 0 0 0
BOND Rc[1]/R R[17] -1 0 0 0 0 0 0
BOND Rc[2]/R R[18] -1 0 0 0 0 0 0
BOND Rc[3]/R R[19] -1 0 0 0 0 0 0
BOND Rc[4]/R R[20] -1 0 0 0 0 0 0
BOND Rc[5]/R R[21] -1 0 0 0 0 0 0
BOND Rc[6]/R R[22] -1 0 0 0 0 0 0
BOND Rc[7]/R R[23] -1 0 0 0 0 0 0
```

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BOND Net_run/Net_run Net_run -1 0 0 0 0 0 0
BOND Net_error/Net_error Net_error -1 0 0 0 0 0 0
BOND Net_clk/VDD TRUE -1 0 0 0 0 0 0
BOND Net_clk/VSS FALSE -1 0 0 0 0 0 0
BOND Net_clk/Net_clk Net_clk -1 0 0 0 0 0 0
BOND Proc_clk/VDD TRUE -1 0 0 0 0 0 0
BOND Proc_clk/VSS FALSE -1 0 0 0 0 0 0
BOND Proc_clk/Proc_clk Proc_clk -1 0 0 0 0 0 0
BOND N_mem_read/N_mem_read N_mem_read -1 0 0 0 0 0 0
BOND R_bus_en[0]/R_bus_en R_bus_en[0] -1 0 0 0 0 0 0
BOND R_bus_en[1]/R_bus_en R_bus_en[1] -1 0 0 0 0 0 0
BOND R_eq_f_2/R_eq_f_2 R_eq_f_2 -1 0 0 0 0 0 0
BOND IO_opcode[0]/IO_opcode IO_opcode[0] -1 0 0 0 0 0 0
BOND IO_opcode[1]/IO_opcode IO_opcode[1] -1 0 0 0 0 0 0
BOND IO_opcode[2]/IO_opcode IO_opcode[2] -1 0 0 0 0 0 0
BOND Dav/Dav Dav -1 0 0 0 0 0 0
BOND Rd[0]/R R[24] -1 0 0 0 0 0 0
BOND Rd[1]/R R[25] -1 0 0 0 0 0 0
BOND Rd[2]/R R[26] -1 0 0 0 0 0 0
BOND Rd[3]/R R[27] -1 0 0 0 0 0 0
BOND Rd[4]/R R[28] -1 0 0 0 0 0 0
BOND Rd[5]/R R[29] -1 0 0 0 0 0 0
BOND Rd[6]/R R[30] -1 0 0 0 0 0 0
BOND Rd[7]/R R[31] -1 0 0 0 0 0 0
BOND Transfer_out/Transfer_out Transfer_out -1 0 0 0 0 0 0
BOND F[0]/F F[0] -1 0 0 0 0 0 0
BOND F[1]/F F[1] -1 0 0 0 0 0 0
BOND F[2]/F F[2] -1 0 0 0 0 0 0
BOND F[3]/F F[3] -1 0 0 0 0 0 0
BOND F[4]/F F[4] -1 0 0 0 0 0 0
BOND F[5]/F F[5] -1 0 0 0 0 0 0
BOND F[6]/F F[6] -1 0 0 0 0 0 0
BOND F[7]/F F[7] -1 0 0 0 0 0 0
BOND F[8]/F F[8] -1 0 0 0 0 0 0
BOND F[9]/F F[9] -1 0 0 0 0 0 0
BOND F[10]/F F[10] -1 0 0 0 0 0 0
BOND F[11]/F F[11] -1 0 0 0 0 0 0
BOND F[12]/F F[12] -1 0 0 0 0 0 0
BOND F[13]/F F[13] -1 0 0 0 0 0 0
BOND F[14]/F F[14] -1 0 0 0 0 0 0
BOND F[15]/F F[15] -1 0 0 0 0 0 0
BOND F[16]/F F[16] -1 0 0 0 0 0 0
BOND F[17]/F F[17] -1 0 0 0 0 0 0
BOND F[18]/F F[18] -1 0 0 0 0 0 0
BOND F[19]/F F[19] -1 0 0 0 0 0 0
BOND F[20]/F F[20] -1 0 0 0 0 0 0
BOND F[21]/F F[21] -1 0 0 0 0 0 0
BOND F[22]/F F[22] -1 0 0 0 0 0 0
BOND F[23]/F F[23] -1 0 0 0 0 0 0
BOND F[24]/F F[24] -1 0 0 0 0 0 0
BOND F[25]/F F[25] -1 0 0 0 0 0 0
BOND F[26]/F F[26] -1 0 0 0 0 0 0
BOND F[27]/F F[27] -1 0 0 0 0 0 0
BOND F[28]/F F[28] -1 0 0 0 0 0 0
BOND F[29]/F F[29] -1 0 0 0 0 0 0
BOND F[30]/F F[30] -1 0 0 0 0 0 0
BOND F[31]/F F[31] -1 0 0 0 0 0 0
```