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GEORGIA TECH GT-VSNI
VLSI DESIGN VERIFICATION DOCUMENT

VLSI DEVELOPMENT REPORT
REPORT NO. VDR-0142-90-002
MAY 23, 1990

**GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY**

Contract No. DASG60-89-C-0142
Sponsored By
The United States Army Strategic Defense Command

COMPUTER ENGINEERING RESEARCH LABORATORY
Georgia Institute of Technology
Atlanta, Georgia 30332 - 0540

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**GEORGIA TECH GT-VSNI
VLSI DESIGN VERIFICATION DOCUMENT**

May 23, 1990

Wei Siong Tan

COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology
Atlanta, Georgia 30332 - 0540

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Georgia Tech Research Corporation
Centennial Research Building
Atlanta, Georgia 30332

GEORGIA TECH GT-VSNI

VLSI DESIGN VERIFICATION DOCUMENT

1.0 INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems/Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech serial network interface chip, GT-VSNI.

TABLE 1. GEORGIA TECH CHIP SET FOR AHAT

Design	DV PASSED	TAPE DELIV.	FABRICATED	TESTED
GT-VFPU	1/17/89	5/10/90	5/19/89	4/6/90
GT-VNUC				
GT-VTF				
GT-VTHR				
GT-VCLS	1/26/90			
GT-VCTR	2/8/90			
GT-VIAG				
GT-VDAG				
GT-VSNI	1/17/89	5/23/89	4/14/89	
GT-VSM8	1/17/89		5/6/89	4/18/89
GT-VSF	9/12/89			

1. Scheduled March 31, 1991
2. Scheduled December 31, 1990

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APPENDIX A DESIGN VERIFICATION CHECKLIST

1. DV CONTROL NUMBER : _____ (Assigned by SCI)

2. CUSTOMER INFORMATION

Customer Name: Georgia Tech Chip Name: xserial (GT-VSNI/1)

Project Manager: Dr. C. O. Alford Phone: (404) 894-2533

Design Engineer: Wei Siong Tan Phone: (404) 894-2508

Phone: _____

Test Engineer : Wei Siong Tan Phone: (404) 894-2508

3. SCI CONTACT: Girish Kumar

4. REGRESSION

4.1 Name of Session Log from recompile: build_all.session

4.2 Name of Simulation ~~and Timing~~ Command File: run all vectors.001

5. FUNCTIONAL INFORMATION (check when included)

5.1 Block Diagram : OK

5.2 Functional Description : OK

5.3 Timing Diagrams at Pins : OK

5.4 Annotated Views : OK Annotated Schematics: OK

5.5 Key Parameters : OK

5.6 Pin Description : OK Attach the _001.216 file.

6. PHYSICAL INFORMATION

6.1 Fabline : NSC-CN12A

6.2 Plots:

Chip Route (D size): OK Bonding Diagram (A size) : OK

6.3 Die Size: Reported Die Size: 300.91x272.17

Maximum Acceptable Die Size: 325x325

Minimum Acceptable Die Size: none

6.4 Genesil Package Name : CPGA120E

If nonstandard, package spec is included _____

6.5 Cavity/Well Size : 434 mils by 434 mils

6.6 Size of database: 40 Meg

Tape density: 6250 1600 TK50 XXX

7. ELECTRICAL INFORMATION**7.1 Chip Frequency**

Specified in netlist: 10 Meg. Target frequency: Net clk - 22.1 Meg. Proc_clk - 14.2 Meg.

7.2 Power Dissipation : Genesil 0.616 Watts Spec 0.616 Watts

7.3 Operating Voltage : from 4.5 Volts to 5.5 Volts

8. SIMULATION

8.1 Number of Clocking Regimes : 2

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	Net_clk	no_div	Net_clk	PHASE_C/PHASE_D
2.	Proc_clk	no_div	Proc_clk	PHASE_A/PHASE_B
3.				
4.				
5.				

8.2 Simulation Setup file (Attach Listings):

Name: design_init.080

Description: Execute "design_init" prior to the execution of vector0.089, ...
vector10.089. Execute "async setup" prior to the execution of vector11.089

Affected Tests: _____

Name: _____

Description: _____

Affected Tests: _____

Name: _____

Description: _____

Affected Tests: _____

Name: _____

8.3 Test Vector Set:

NOTE: Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz.

Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

- ```

1. Name: run_all_vectors.001 No of vectors: 25,181
Generated using MASH: xxx traceobj: other:
Timing Resolution: phase xx cycle xx other:
Description: vector0.089, ... vector10.089 have timing resolution of
cycles. vector11.089 has timing resolution of phases.

```

**Portions of Chip Tested:** all (refer to chip document page 15 to 17)

```
Use for switch level simulation? Y N yes
Use for tester? Y N yes
```

2. Name: \_\_\_\_\_ No of vectors: \_\_\_\_\_  
Generated using MASM: \_\_\_\_\_ traceobj: \_\_\_\_\_ other: \_\_\_\_\_  
Timing Resolution: phase \_\_\_\_\_ cycle \_\_\_\_\_ other: \_\_\_\_\_  
Description: \_\_\_\_\_

Portions of Chip Tested: \_\_\_\_\_

```
Use for switch level simulation? Y N
Use for tester? Y N
```

3. Name: \_\_\_\_\_ No of vectors: \_\_\_\_\_  
Generated using MASM: \_\_\_\_\_ traceobj: \_\_\_\_\_ other: \_\_\_\_\_  
Timing Resolution: phase \_\_\_\_\_ cycle \_\_\_\_\_ other: \_\_\_\_\_  
Description: \_\_\_\_\_

Portions of Chip Tested: \_\_\_\_\_

```
Use for switch level simulation? Y N
Use for tester? Y N
```

4. Name: \_\_\_\_\_ No of vectors: \_\_\_\_\_  
Generated using MASM: \_\_\_\_\_ traceobj: \_\_\_\_\_ other: \_\_\_\_\_  
Timing Resolution: phase \_\_\_\_\_ cycle \_\_\_\_\_ other: \_\_\_\_\_  
Description: \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

Portions of Chip Tested: \_\_\_\_\_  
\_\_\_\_\_

Use for switch level simulation? Y N  
Use for tester? Y N

5. Name: \_\_\_\_\_ No of vectors: \_\_\_\_\_  
Generated using MASM: \_\_\_\_\_ traceobj: \_\_\_\_\_ other: \_\_\_\_\_  
Timing Resolution: phase \_\_\_\_\_ cycle \_\_\_\_\_ other: \_\_\_\_\_  
Description: \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

Portions of Chip Tested: \_\_\_\_\_  
\_\_\_\_\_

Use for switch level simulation? Y N  
Use for tester? Y N

6. Name: \_\_\_\_\_ No of vectors: \_\_\_\_\_  
Generated using MASM: \_\_\_\_\_ traceobj: \_\_\_\_\_ other: \_\_\_\_\_  
Timing Resolution: phase \_\_\_\_\_ cycle \_\_\_\_\_ other: \_\_\_\_\_  
Description: \_\_\_\_\_  
Description: \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

Portions of Chip Tested: \_\_\_\_\_  
\_\_\_\_\_

Use for switch level simulation? Y N  
Use for tester? Y N

7. Name: \_\_\_\_\_ No of vectors: \_\_\_\_\_  
Generated using MASM: \_\_\_\_\_ traceobj: \_\_\_\_\_ other: \_\_\_\_\_  
Timing Resolution: phase \_\_\_\_\_ cycle \_\_\_\_\_ other: \_\_\_\_\_  
Description: \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

Portions of Chip Tested: \_\_\_\_\_  
\_\_\_\_\_

Use for switch level simulation? Y N  
Use for tester? Y N

## 9. TIMING ANALYSIS

## 9.1 Environment

Temperature Coefficient: 35 Degree C / Watt (theta\_JA)  
 Operating Temp : from 0 C (min) to 70 C (max)  
 Operating Voltage : from 4.5 V (min) to 5.5 V (max)

room junction temp =  $25 + (\text{theta\_JA} * \text{Power}) = 46.56$  degrees C  
 maximum junction temp =

maximum ambient temp +  $(\text{theta\_JA} * \text{Power}) = 91.56$  degrees C

## 9.2 Include the following reports:

guaranteed model  
 5.0V (@47 C)  
 room temp

-----  
 Cycle: OK  
 Setup/Hold: OK  
 Output Delay: OK  
 Path Delay: OK

guaranteed model  
 min operating V (@ 4.5V)  
 max junction temp (@ 92C)

-----  
 Cycle: OK  
 Setup/Hold: OK  
 Output Delay: OK  
 Path Delay: OK

target model  
 min operating V  
 max junction temp

-----  
 Cycle:       
 Setup/Hold:       
 Output Delay:       
 Path Delay:     

## 9.3 Setup Files:

Name: \_\_\_\_\_  
 Description : \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_

Name: \_\_\_\_\_  
 Description : \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_

Name: \_\_\_\_\_  
 Description : \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_

Name: \_\_\_\_\_  
 Description : \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_  
 \_\_\_\_\_

## 9.4 Critical Boundary Conditions:

List critical paths here or annotate the timing report.  
Attach additional pages if needed.

## Clocks

|                    | Net clk<br><del>report</del> | Proc clk<br><del>limit</del> |
|--------------------|------------------------------|------------------------------|
| 1. Phase 1 High    | <u>20.7</u>                  | <u>24.2</u>                  |
| 2. Phase 2 High    | <u>22.1</u>                  | <u>41.7</u>                  |
| 3. Symmetric Cycle | <u>44.1</u>                  | <u>70.2</u>                  |
| 4. Minimum Cycle   | <u>44.1</u>                  | <u>70.2</u>                  |

## Outputs

|     | Signal Name                         | load (pF) | delay | limit |
|-----|-------------------------------------|-----------|-------|-------|
| 1.  | all of the signals use default load |           |       |       |
| 2.  | ( see the attached timing report )  |           |       |       |
| 3.  |                                     |           |       |       |
| 4.  |                                     |           |       |       |
| 5.  |                                     |           |       |       |
| 6.  |                                     |           |       |       |
| 7.  |                                     |           |       |       |
| 8.  |                                     |           |       |       |
| 9.  |                                     |           |       |       |
| 10. |                                     |           |       |       |

## Inputs

|     | Signal Name                        | setup | hold | limit |
|-----|------------------------------------|-------|------|-------|
| 1.  | ( see the attached timing report ) |       |      |       |
| 2.  |                                    |       |      |       |
| 3.  |                                    |       |      |       |
| 4.  |                                    |       |      |       |
| 5.  |                                    |       |      |       |
| 6.  |                                    |       |      |       |
| 7.  |                                    |       |      |       |
| 8.  |                                    |       |      |       |
| 9.  |                                    |       |      |       |
| 10. |                                    |       |      |       |

9.5 Hold Time Violations: none

## 10. DC CHARACTERISTICS - CMOS

| PARAMETERS            | DESCRIPTION                        | CONDITIONS<br>0 to 70 | CONDITIONS<br>-55 to +125 | MIN    | MAX   |
|-----------------------|------------------------------------|-----------------------|---------------------------|--------|-------|
| DATA PAD INPUT ONLY   |                                    |                       |                           |        |       |
| VIH                   | Input High Voltage                 |                       |                           | 2.0V   |       |
| VIL                   | Input Low Voltage                  |                       |                           |        | 0.8V  |
| IIL                   | Input Leakage                      | VSS<Vin<VDD           | VSS<Vin<VDD               | -100uA | 100uA |
| CIN                   | Input Capacitance                  |                       |                           |        | 6.0pf |
| DATA PAD OUTPUT ONLY  |                                    |                       |                           |        |       |
| VOH                   | Output High Voltage                | VDD= 4.5V<br>IOH=-2.2 | VDD= 4.5V<br>IOH=-2mA     | 2.4V   |       |
| VOL                   | Output Low Voltage                 | VDD= 4.5V<br>IOL= 6mA | VDD= 4.5V<br>IOL= 5mA     |        | 0.4V  |
| IOZ                   | Output Leakage<br>current(high Z)  | VSS<Vout<VDD          | VSS<Vout<VDD              | -100uA | 100uA |
| COUT                  | Output Capacitance                 |                       |                           |        | 7.0pf |
| DATA PAD INPUT/OUTPUT |                                    |                       |                           |        |       |
| VOH                   | Output High Voltage                | VDD= 4.5V<br>IOH=-2.2 | VDD= 4.5V<br>IOH=-2mA     | 2.4V   |       |
| VOL                   | Output Low Voltage                 | VDD= 4.5V<br>IOL= 6mA | VDD= 4.5V<br>IOL= 5mA     |        | 0.4V  |
| VIH                   | Input High Voltage                 |                       |                           | 2.0V   |       |
| VIL                   | Input Low Voltage                  |                       |                           |        | 0.8V  |
| IOZ                   | Output leakage<br>current (high Z) | VSS<Vout<VDD          | VSS<Vout<VDD              | -100uA | 100uA |
| CIO                   | Input/Output Capacitance           |                       |                           |        | 7.0pf |
| CLOCK PAD             |                                    |                       |                           |        |       |
| VIH                   | Input High Voltage                 |                       |                           | 3.9V   |       |
| VIL                   | Input Low Voltage                  |                       |                           |        | 0.6V  |
| IIL                   | Input Leakage                      | VSS<Vin<VDD           | VSS<Vin<VDD               | -100uA | 100uA |
| CIN                   | Input Capacitance                  |                       |                           |        | 15pf  |

NOTE: All parameters are measured at a supply voltage of VDD = 5V +/- 10% and a junction temperature of 125 C.

**11. TAPEOUT AND TESTING SPECIFICATION**

Prototype Brokerage Service Purchased? xxx yes        no  
If yes: PO # will be provided at later date

**12. CUSTOMER CHECKLIST COMMENTS****Pre-Verification Comments**

We request that SCS inform us of the fault coverage of the test vectors we provided.

If the test coverage is low, we will provide additional test vectors.

The die size as it stands now causes design errors on the packaging.

This is not corrected because to do that would require trial and error (ad hoc)

expansion of the chip size. The die size already exceeds the minimum die size

**13. CUSTOMER CHECKLIST APPROVAL** requirement for the PGA120E package.

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compilers as agreed to in either the Design Verification Terms & Conditions or the Prototype Brokerage Services Terms & Conditions.

Customer Approval : Martin Buching Date 6/8/88  
Title : FAC - Southeast Area

**14. SCI CHECKLIST APPROVAL****Pre-Verification Comments**

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

SCI Approval : \_\_\_\_\_ Date \_\_\_\_/\_\_\_\_/\_\_\_\_

Title : \_\_\_\_\_

## 11.2.1.3 CPGA100e

TYPE: 100 Lead Ceramic Pin-Grid Array

## DIMENSIONS:

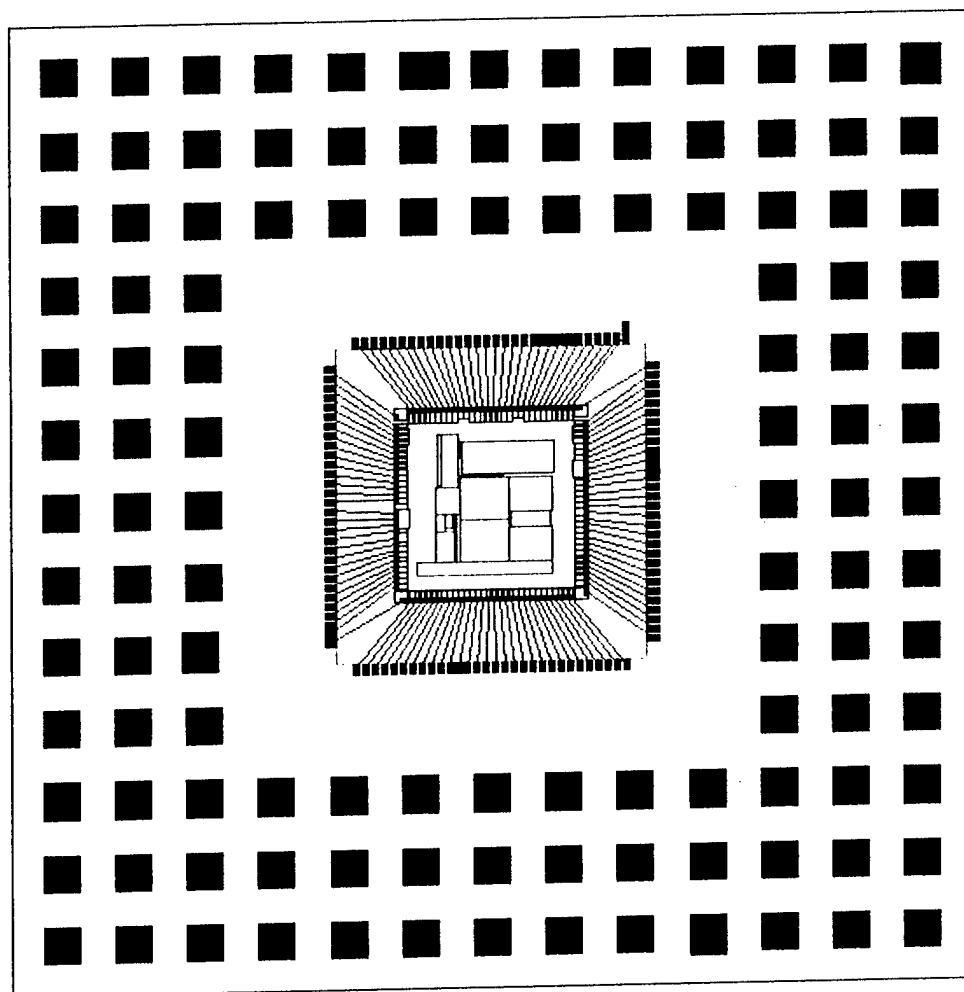
|                          |                                                      |
|--------------------------|------------------------------------------------------|
| PACKAGE                  | w = 1.332 inch.<br>l = 1.332 inch.<br>h = .134 inch. |
| CAVITY                   | w = .433 inch.<br>l = .433 inch.                     |
| LEAD SPACING:            | .100 inch.                                           |
| MAXIMUM DIE SIZE:        | .393 x .393 inch./side*                              |
| MINIMUM DIE SIZE:        | .193 x .193 inch./side*                              |
| MAXIMUM BOND LENGTH:     | .120 inch.*                                          |
| MAXIMUM BOND ANGLE:      | 45 deg.*                                             |
| TEMPERATURE COEFFICIENT: | 35 deg. C/Watt                                       |

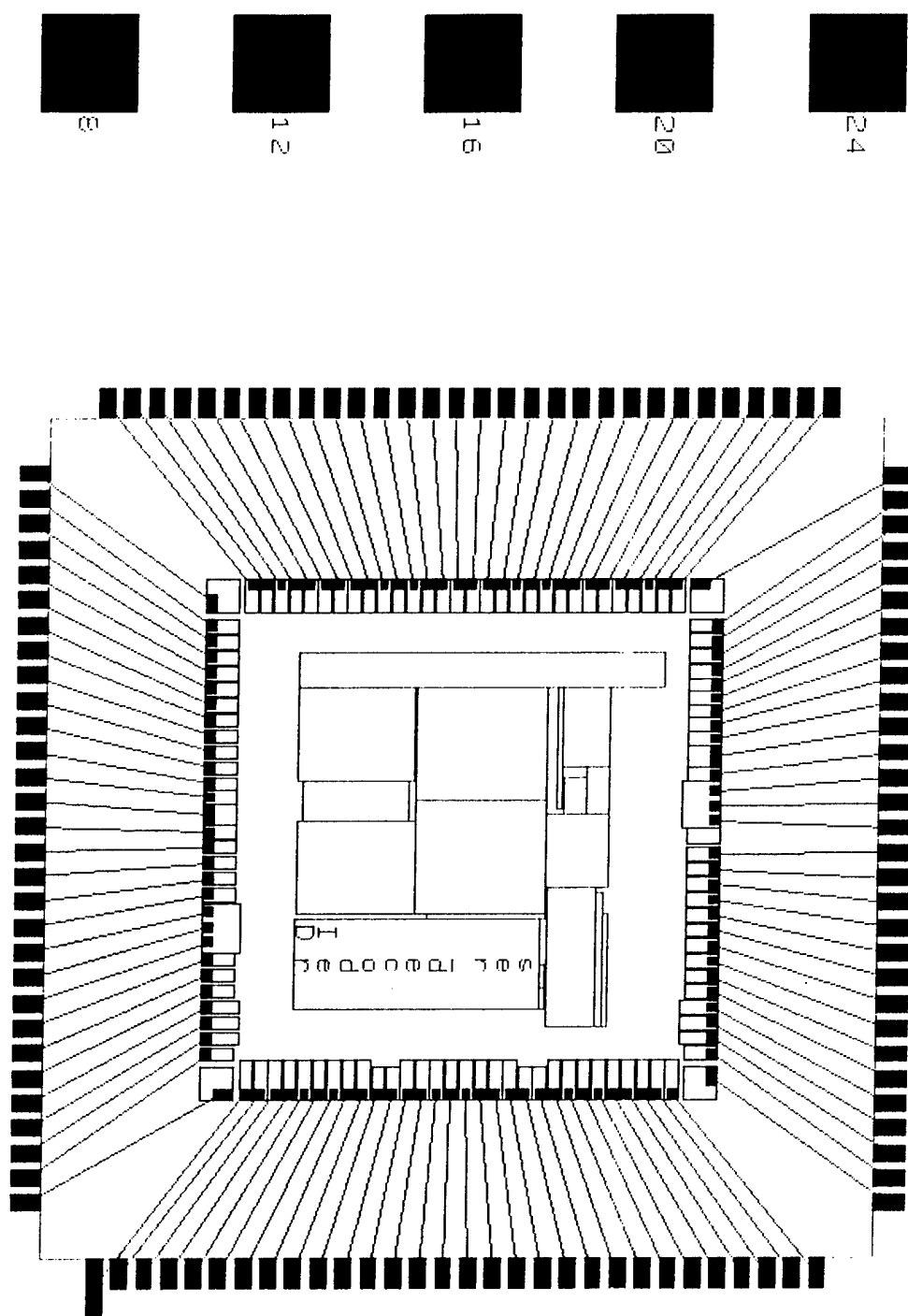
## 11.2.1.4 CPGA120e

TYPE: 120 Lead Ceramic Pin-Grid Array

## DIMENSIONS:

|                          |                                                      |
|--------------------------|------------------------------------------------------|
| PACKAGE                  | w = 1.332 inch.<br>l = 1.332 inch.<br>h = .134 inch. |
| CAVITY                   | w = .433 inch.<br>l = .433 inch.                     |
| LEAD SPACING:            | .100 inch.                                           |
| MAXIMUM DIE SIZE:        | .393 x .393 inch./side*                              |
| MINIMUM DIE SIZE:        | .193 x .193 inch./side*                              |
| MAXIMUM BOND LENGTH:     | .120 inch.*                                          |
| MAXIMUM BOND ANGLE:      | 45 deg.*                                             |
| TEMPERATURE COEFFICIENT: | 35 deg. C/Watt                                       |





6



12



16



20



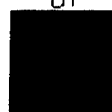
24



64



80



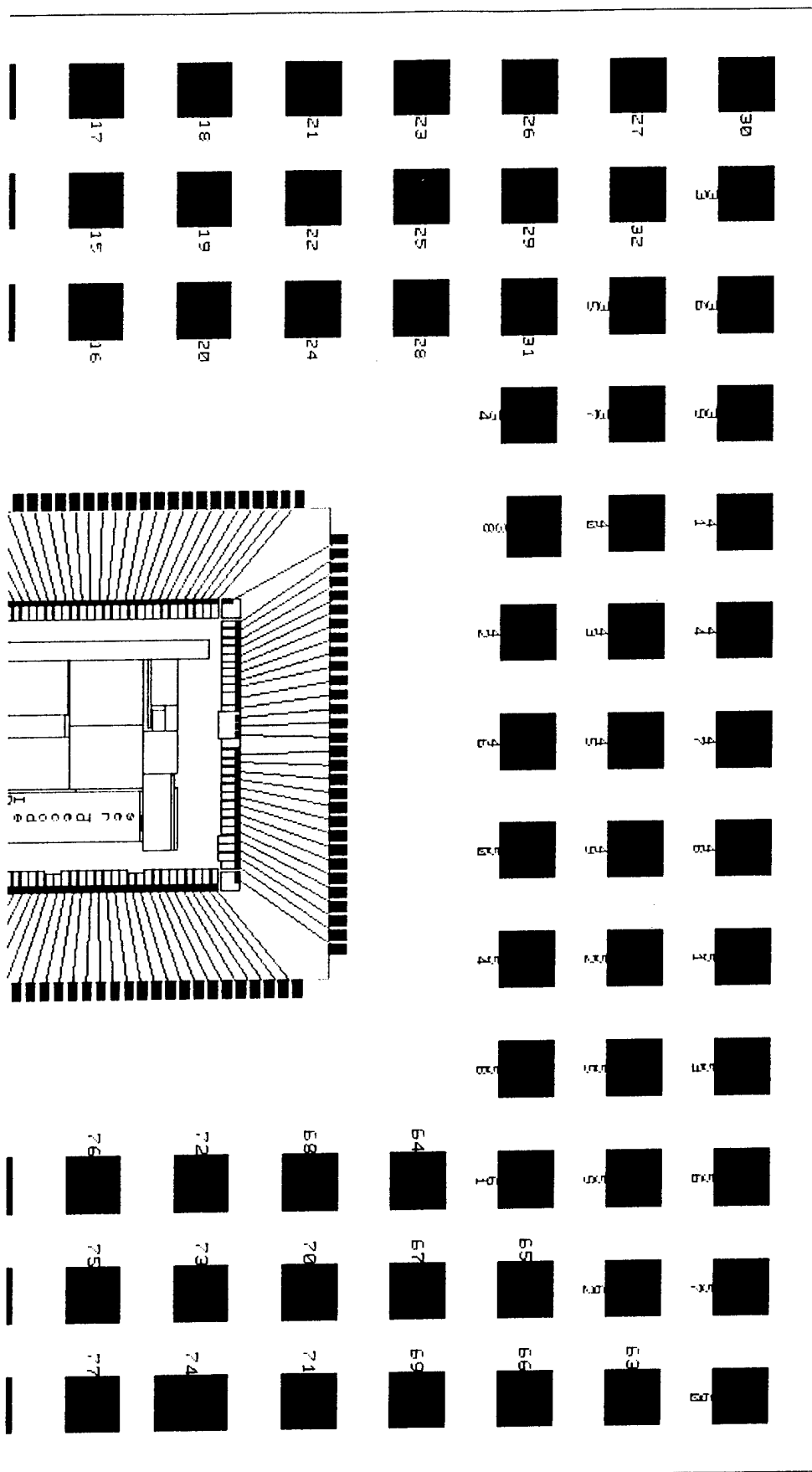
96

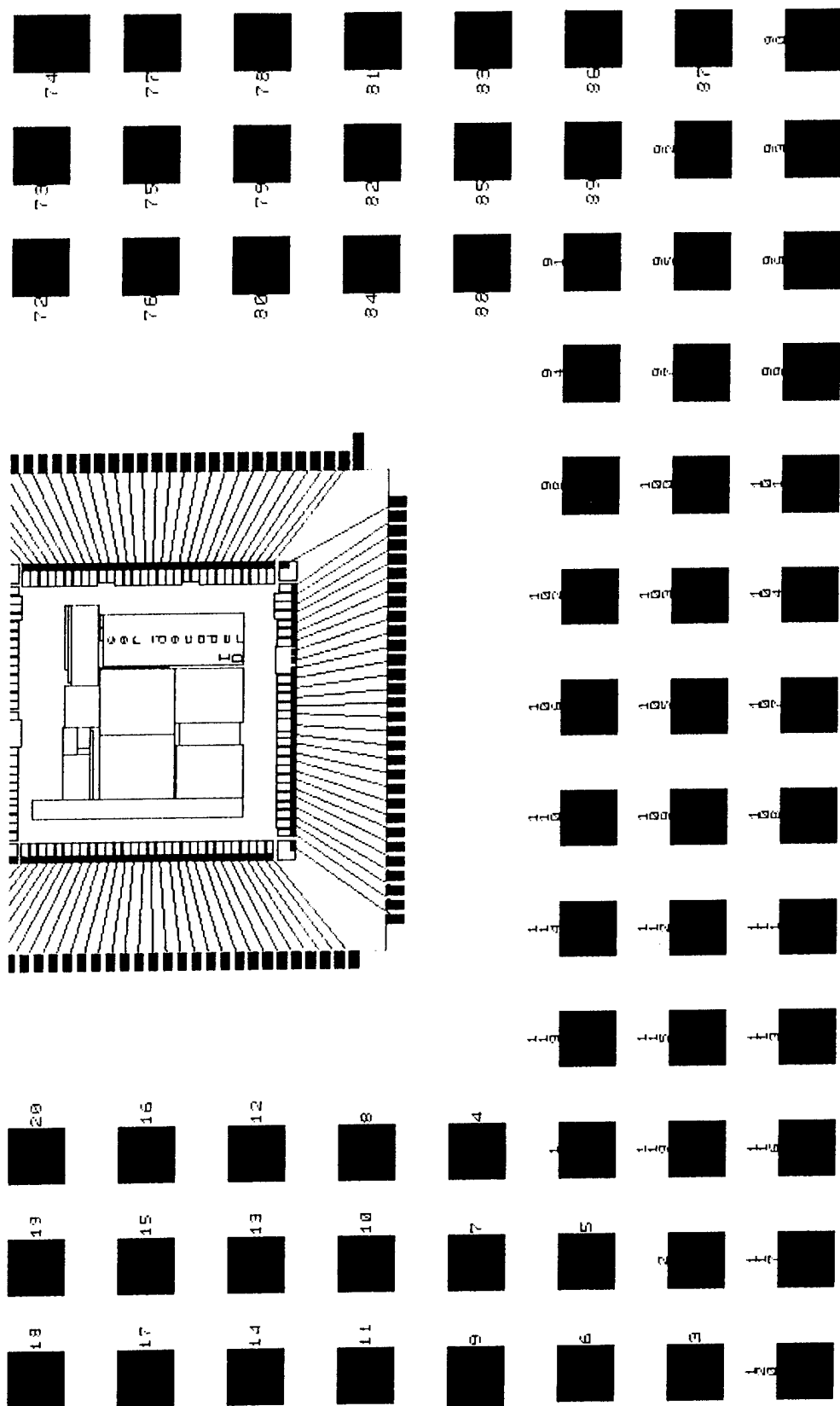


112



128





```
east {
 "Ra[3]" = 1
 "Ra[4]" = 2
 "Ra[5]" = 3
 "Ra[6]" = 4
 "Ra[7]" = 5
 "Rb[0]" = 6
 "Rb[1]" = 7
 "Rb[2]" = 8
 "Rb[3]" = 9
 "Ring_vss[1]" = 10
 "Ring_vdd[1]" = 11
 "Rb[4]" = 12
 "Rb[5]" = 13
 "Rb[6]" = 14
 "Rb[7]" = 15
 "Rc[0]" = 16
 "Rc[1]" = 17
 "Rc[2]" = 18
 "Rc[3]" = 19
 "Ring_vss[2]" = 20
 "Ring_vdd[2]" = 21
 "Rc[4]" = 22
 "Rc[5]" = 23
 "Rc[6]" = 24
 "Rc[7]" = 25
 "Rd[0]" = 26
 "Rd[1]" = 27
 "Rd[2]" = 28
 "Rd[3]" = 29
 "Rd[4]" = 30
}
north
{
 "Ring_vss[0]" = 32
 "Rd[5]" = 33
 "Rd[6]" = 34
 "Rd[7]" = 35
 "Data[0]" = 36
 "Data[1]" = 37
 "Data[2]" = 38
 "Data[3]" = 39
 "Ring_vss[3]" = 40
 "Ring_vdd[3]" = 41
 "Data[4]" = 42
 "Data[5]" = 43
 "Data[6]" = 44
 "Data[7]" = 45
 "Label" = 0
 "Proc_clk" = 46,47,48
 "N_xack" = 49
 "Core_vss" = 50
 "N_mem_write" = 51
 "N_mem_read" = 52
 "N_chip_select" = 53
 "Address[0]" = 54
}
```

```
"Address[1]" = 55
"Address[2]" = 56
"Req_f_2" = 57
"F[0]" = 58
"F[1]" = 59
```

```
}
west
```

```
{
"F[2]" = 61
"F[3]" = 62
"F[4]" = 63
"F[5]" = 64
"F[6]" = 65
"F[7]" = 66
"F[8]" = 67
"F[9]" = 68
"F[10]" = 69
"F[11]" = 70
"F[12]" = 71
"F[13]" = 72
"F[14]" = 73
"F[15]" = 74
"F[16]" = 75
"F[17]" = 76
"F[18]" = 77
"F[19]" = 78
"F[20]" = 79
"F[21]" = 80
"F[22]" = 81
"F[23]" = 82
"F[24]" = 83
"F[25]" = 84
"F[26]" = 85
"F[27]" = 86
"F[28]" = 87
"F[29]" = 88
"F[30]" = 89
"F[31]" = 90
}
```

```
south
```

```
{
"Ring_vdd[4]" = 92
"Host_dav" = 93
"Host_rfi" = 94
"Net_dav" = 95
"Net_rfi" = 96
"Net_error" = 97
"IO_opcode[2]" = 98
"IO_opcode[1]" = 99
"IO_opcode[0]" = 100
"R_Bus_en[0]" = 101
"R_bus_en[1]" = 102
"Proc_run" = 103
"Core_vdd" = 104
"Net_run" = 105
"Net_sync" = 106
}
```

```
"Transfer_out" = 107
"Transfer_in" = 108
"Serial_in" = 109
"Net_clk" = 110,111,112
"Dav" = 113
"Rfi" = 114
"Serial_out" = 115
"Ra[0]" = 116
"Ra[1]" = 117
"Ra[2]" = 118
"Ring_vdd[0]" = 119
}
```

```
pinout:
```

```
pad = "Corner_vss[0]" :
```

```
{
 location = (47201,-2726);
 orientation = R90;
 pinout = 120;
}
```

```
pad = "Ra[3]" :
```

```
{
 location = (47201,-1560);
 orientation = R90;
 pinout = 1;
}
```

```
pad = "Ra[4]" :
```

```
{
 location = (47201,-6);
 orientation = R90;
 pinout = 2;
}
```

```
pad = "Ra[5]" :
```

```
{
 location = (47201,1548);
 orientation = R90;
 pinout = 3;
}
```

```
pad = "Ra[6]" :
```

```
{
 location = (47201,3102);
 orientation = R90;
 pinout = 4;
}
```

```
pad = "Ra[7]" :
```

```
{
 location = (47201,4656);
 orientation = R90;
 pinout = 5;
}
```

```
pad = "Rb[0]" :
```

```
{
 location = (47201,6210);
 orientation = R90;
 pinout = 6;
}
```

```
pad = "Rb[1]" :
```

```
{
 location = (47201,7764);
 orientation = R90;
 pinout = 7;
}
```

```
pad = "Rb[2]" :
```

```
{
 location = (47201,9319);
 orientation = R90;
 pinout = 8;
}
```

```
pad = "Rb[3]" :
```

```
{
 location = (47201,10873);
 orientation = R90;
 pinout = 9;
}
```

```
pad = "Ring_vss[1]" :
```

```
{
 location = (47201,12427);
 orientation = R90;
 pinout = 10;
}
```

```
pad = "Ring_vdd[1]" :
```

```
{
 location = (47201,13981);
 orientation = R90;
 pinout = 11;
}
```

```
pad = "Rb[4]" :
```

```
{
 location = (47201,15535);
 orientation = R90;
 pinout = 12;
}
```

```
pad = "Rb[5]" :
```

```
{
 location = (47201,17089);
 orientation = R90;
 pinout = 13;
}
```

```
pad = "Rb[6]" :
```

```
{
 location = (47201,18643);
 orientation = R90;
 pinout = 14;
}
```

```
pad = "Rb[7]" :
```

```
{
 location = (47201,20197);
 orientation = R90;
 pinout = 15;
}
```

```
pad = "Rc[0]" :
```

```
{
 location = (47201,21752);
 orientation = R90;
 pinout = 16;
}
```

```
pad = "Rc[1]" :
```

```
{
 location = (47201,23306);
 orientation = R90;
 pinout = 17;
}
```

```
pad = "Rc[2]" :
```

```
{
 location = (47201,24860);
}
```

```
orientation = R90;
pinout = 18;
```

```
}
pad = "Rc[3]" :
```

```
{
location = (47201,26414);
orientation = R90;
pinout = 19;
```

```
}
pad = "Ring_vss[2]" :
```

```
{
location = (47201,27968);
orientation = R90;
pinout = 20;
```

```
}
pad = "Ring_vdd[2]" :
```

```
{
location = (47201,29522);
orientation = R90;
pinout = 21;
```

```
}
pad = "Rc[4]" :
```

```
{
location = (47201,31076);
orientation = R90;
pinout = 22;
```

```
}
pad = "Rc[5]" :
```

```
{
location = (47201,32630);
orientation = R90;
pinout = 23;
```

```
}
pad = "Rc[6]" :
```

```
{
location = (47201,34185);
orientation = R90;
pinout = 24;
```

```
}
pad = "Rc[7]" :
```

```
{
location = (47201,35739);
orientation = R90;
pinout = 25;
```

```
}
pad = "Rd[0]" :
```

```
{
location = (47201,37293);
orientation = R90;
pinout = 26;
```

```
}
pad = "Rd[1]" :
```

```
{
location = (47201,38847);
orientation = R90;
pinout = 27;
```

```
}
pad = "Rd[2]" :
{
 location = (47201,40401);
 orientation = R90;
 pinout = 28;
}
pad = "Rd[3]" :
{
 location = (47201,41955);
 orientation = R90;
 pinout = 29;
}
pad = "Rd[4]" :
{
 location = (47201,43509);
 orientation = R90;
 pinout = 30;
}
pad = "Corner_vdd[0]" :
{
 location = (47201,45452);
 orientation = R180;
 pinout = 31;
}
pad = "Ring_vss[0]" :
{
 location = (45997,45452);
 orientation = R180;
 pinout = 32;
}
pad = "Rd[5]" :
{
 location = (44391,45452);
 orientation = R180;
 pinout = 33;
}
pad = "Rd[6]" :
{
 location = (42785,45452);
 orientation = R180;
 pinout = 34;
}
pad = "Rd[7]" :
{
 location = (41179,45452);
 orientation = R180;
 pinout = 35;
}
pad = "Data[0]" :
{
 location = (39573,45452);
 orientation = R180;
 pinout = 36;
}
pad = "Data[1]" :
```

```
{
 location = (37967,45452);
 orientation = R180;
 pinout = 37;
}
```

```
pad = "Data[2]" :
```

```
{
 location = (36361,45452);
 orientation = R180;
 pinout = 38;
}
```

```
pad = "Data[3]" :
```

```
{
 location = (34755,45452);
 orientation = R180;
 pinout = 39;
}
```

```
pad = "Ring_vss[3]" :
```

```
{
 location = (33149,45452);
 orientation = R180;
 pinout = 40;
}
```

```
pad = "Ring_vdd[3]" :
```

```
{
 location = (31543,45452);
 orientation = R180;
 pinout = 41;
}
```

```
pad = "Data[4]" :
```

```
{
 location = (29937,45452);
 orientation = R180;
 pinout = 42;
}
```

```
pad = "Data[5]" :
```

```
{
 location = (28331,45452);
 orientation = R180;
 pinout = 43;
}
```

```
pad = "Data[6]" :
```

```
{
 location = (26725,45452);
 orientation = R180;
 pinout = 44;
}
```

```
pad = "Data[7]" :
```

```
{
 location = (25119,45452);
 orientation = R180;
 pinout = 45;
}
```

```
pad = "Label" :
```

```
{
 location = (23513,45452);
}
```

```
orientation = R180;
pinout = NC;
```

```
}
pad = "Proc_clk" :
```

```
{
location = (21908,45452);
orientation = R180;
pinout = 46,47,48;
}
```

```
pad = "N_xack" :
```

```
{
location = (17090,45452);
orientation = R180;
pinout = 49;
}
```

```
pad = "Core_vss" :
```

```
{
location = (15484,45452);
orientation = R180;
pinout = 50;
}
```

```
pad = "N_mem_write" :
```

```
{
location = (13878,45452);
orientation = R180;
pinout = 51;
}
```

```
pad = "N_mem_read" :
```

```
{
location = (12272,45452);
orientation = R180;
pinout = 52;
}
```

```
pad = "N_chip_select" :
```

```
{
location = (10666,45452);
orientation = R180;
pinout = 53;
}
```

```
pad = "Address[0]" :
```

```
{
location = (9060,45452);
orientation = R180;
pinout = 54;
}
```

```
pad = "Address[1]" :
```

```
{
location = (7454,45452);
orientation = R180;
pinout = 55;
}
```

```
pad = "Address[2]" :
```

```
{
location = (5848,45452);
orientation = R180;
pinout = 56;
}
```

```
}
pad = "R_eq_f_2" :
{
 location = (4242,45452);
 orientation = R180;
 pinout = 57;
}
pad = "F[0]" :
{
 location = (2636,45452);
 orientation = R180;
 pinout = 58;
}
pad = "F[1]" :
{
 location = (1030,45452);
 orientation = R180;
 pinout = 59;
}
pad = "Corner_vdd[1]" :
{
 location = (-977,45452);
 orientation = R270;
 pinout = 60;
}
pad = "F[2]" :
{
 location = (-977,44286);
 orientation = R270;
 pinout = 61;
}
pad = "F[3]" :
{
 location = (-977,42732);
 orientation = R270;
 pinout = 62;
}
pad = "F[4]" :
{
 location = (-977,41178);
 orientation = R270;
 pinout = 63;
}
pad = "F[5]" :
{
 location = (-977,39624);
 orientation = R270;
 pinout = 64;
}
pad = "F[6]" :
{
 location = (-977,38070);
 orientation = R270;
 pinout = 65;
}
pad = "F[7]" :
```

```
{
 location = (-977,36516);
 orientation = R270;
 pinout = 66;
}
```

```
pad = "F[8]" :
```

```
{
 location = (-977,34962);
 orientation = R270;
 pinout = 67;
}
```

```
pad = "F[9]" :
```

```
{
 location = (-977,33408);
 orientation = R270;
 pinout = 68;
}
```

```
pad = "F[10]" :
```

```
{
 location = (-977,31853);
 orientation = R270;
 pinout = 69;
}
```

```
pad = "F[11]" :
```

```
{
 location = (-977,30299);
 orientation = R270;
 pinout = 70;
}
```

```
pad = "F[12]" :
```

```
{
 location = (-977,28745);
 orientation = R270;
 pinout = 71;
}
```

```
pad = "F[13]" :
```

```
{
 location = (-977,27191);
 orientation = R270;
 pinout = 72;
}
```

```
pad = "F[14]" :
```

```
{
 location = (-977,25637);
 orientation = R270;
 pinout = 73;
}
```

```
pad = "F[15]" :
```

```
{
 location = (-977,24083);
 orientation = R270;
 pinout = 74;
}
```

```
pad = "F[16]" :
```

```
{
 location = (-977,22529);
}
```

```
orientation = R270;
pinout = 75;
```

```
}
pad = "F[17]" :
```

```
{
location = (-977,20974);
orientation = R270;
pinout = 76;
```

```
}
pad = "F[18]" :
```

```
{
location = (-977,19420);
orientation = R270;
pinout = 77;
```

```
}
pad = "F[19]" :
```

```
{
location = (-977,17866);
orientation = R270;
pinout = 78;
```

```
}
pad = "F[20]" :
```

```
{
location = (-977,16312);
orientation = R270;
pinout = 79;
```

```
}
pad = "F[21]" :
```

```
{
location = (-977,14758);
orientation = R270;
pinout = 80;
```

```
}
pad = "F[22]" :
```

```
{
location = (-977,13204);
orientation = R270;
pinout = 81;
```

```
}
pad = "F[23]" :
```

```
{
location = (-977,11650);
orientation = R270;
pinout = 82;
```

```
}
pad = "F[24]" :
```

```
{
location = (-977,10096);
orientation = R270;
pinout = 83;
```

```
}
pad = "F[25]" :
```

```
{
location = (-977,8541);
orientation = R270;
pinout = 84;
```

```
}
pad = "F[26]" :
{
 location = (-977,6987);
 orientation = R270;
 pinout = 85;
}
pad = "F[27]" :
{
 location = (-977,5433);
 orientation = R270;
 pinout = 86;
}
pad = "F[28]" :
{
 location = (-977,3879);
 orientation = R270;
 pinout = 87;
}
pad = "F[29]" :
{
 location = (-977,2325);
 orientation = R270;
 pinout = 88;
}
pad = "F[30]" :
{
 location = (-977,771);
 orientation = R270;
 pinout = 89;
}
pad = "F[31]" :
{
 location = (-977,-783);
 orientation = R270;
 pinout = 90;
}
pad = "Corner_vss[1]" :
{
 location = (-977,-2726);
 orientation = ID;
 pinout = 91;
}
pad = "Ring_vdd[4]" :
{
 location = (269,-2726);
 orientation = ID;
 pinout = 92;
}
pad = "Host_dav" :
{
 location = (1930,-2726);
 orientation = ID;
 pinout = 93;
}
pad = "Host_rfi" :
```

```
{
 location = (3592,-2726);
 orientation = ID;
 pinout = 94;
}
```

```
pad = "Net_dav" :
```

```
{
 location = (5253,-2726);
 orientation = ID;
 pinout = 95;
}
```

```
pad = "Net_rfi" :
```

```
{
 location = (6914,-2726);
 orientation = ID;
 pinout = 96;
}
```

```
pad = "Net_error" :
```

```
{
 location = (8576,-2726);
 orientation = ID;
 pinout = 97;
}
```

```
pad = "IO_opcode[2]" :
```

```
{
 location = (10237,-2726);
 orientation = ID;
 pinout = 98;
}
```

```
pad = "IO_opcode[1]" :
```

```
{
 location = (11898,-2726);
 orientation = ID;
 pinout = 99;
}
```

```
pad = "IO_opcode[0]" :
```

```
{
 location = (13559,-2726);
 orientation = ID;
 pinout = 100;
}
```

```
pad = "R_bus_en[0]" :
```

```
{
 location = (15221,-2726);
 orientation = ID;
 pinout = 101;
}
```

```
pad = "R_bus_en[1]" :
```

```
{
 location = (16882,-2726);
 orientation = ID;
 pinout = 102;
}
```

```
pad = "Proc_run" :
```

```
{
 location = (18543,-2726);
}
```

```
orientation = ID;
pinout = 103;
```

```
}
pad = "Core_vdd" :
```

```
{
location = (20205,-2726);
orientation = ID;
pinout = 104;
```

```
}
pad = "Net_run" :
```

```
{
location = (21866,-2726);
orientation = ID;
pinout = 105;
```

```
}
pad = "Net_sync" :
```

```
{
location = (23527,-2726);
orientation = ID;
pinout = 106;
```

```
}
pad = "Transfer_out" :
```

```
{
location = (25189,-2726);
orientation = ID;
pinout = 107;
```

```
}
pad = "Transfer_in" :
```

```
{
location = (26850,-2726);
orientation = ID;
pinout = 108;
```

```
}
pad = "Serial_in" :
```

```
{
location = (28511,-2726);
orientation = ID;
pinout = 109;
```

```
}
pad = "Net_clk" :
```

```
{
location = (30173,-2726);
orientation = ID;
pinout = 110,111,112;
```

```
}
pad = "Dav" :
```

```
{
location = (35156,-2726);
orientation = ID;
pinout = 113;
```

```
}
pad = "Rfi" :
```

```
{
location = (36818,-2726);
orientation = ID;
pinout = 114;
```

```
}
pad = "Serial_out" :
{
 location = (38479,-2726);
 orientation = ID;
 pinout = 115;
}
pad = "Ra[0]" :
{
 location = (40140,-2726);
 orientation = ID;
 pinout = 116;
}
pad = "Ra[1]" :
{
 location = (41802,-2726);
 orientation = ID;
 pinout = 117;
}
pad = "Ra[2]" :
{
 location = (43463,-2726);
 orientation = ID;
 pinout = 118;
}
pad = "Ring_vdd[0]" :
{
 location = (45124,-2726);
 orientation = ID;
 pinout = 119;
}
end_pinout;
```

\*\*\*\*\*  
Genesil Screen Dump -- Wed Jun 8 17:10:29 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## SETUP AND HOLD MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Proc\_clk

Included setup files:

#0 nom\_phase\_a

(nominal op. cond. for Proc\_clk)

-----  
INPUT SETUP AND HOLD TIMES (ns)

| Input      | Setup Time |        | Hold Time |        |      |
|------------|------------|--------|-----------|--------|------|
|            | Ph1(f)     | Ph2(f) | Ph1(f)    | Ph2(f) |      |
| Address[0] | ---        | 8.8    | ---       | -5.4   | PATH |
| Address[1] | ---        | 9.0    | ---       | -5.6   | PATH |
| Address[2] | ---        | 8.8    | ---       | -5.5   | PATH |
| Data[0]    | ---        | 6.0    | ---       | -2.5   | PATH |
| Data[1]    | ---        | 6.1    | ---       | -2.6   | PATH |
| Data[2]    | ---        | 5.9    | ---       | -2.5   | PATH |
| Data[3]    | ---        | 5.9    | ---       | -2.5   | PATH |
| Data[4]    | ---        | 7.2    | ---       | -3.8   | PATH |
| Data[5]    | ---        | 7.1    | ---       | -3.7   | PATH |
| Data[6]    | ---        | 7.0    | ---       | -3.6   | PATH |
| Data[7]    | ---        | 6.8    | ---       | -3.5   | PATH |
| F[0]       | ---        | 0.4    | ---       | 1.0    | PATH |
| F[10]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[11]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[12]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[13]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[14]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[15]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[16]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[17]      | ---        | 0.3    | ---       | 1.1    | PATH |
| F[18]      | ---        | 0.3    | ---       | 1.2    | PATH |
| F[19]      | ---        | 0.3    | ---       | 1.2    | PATH |
| F[1]       | ---        | 0.4    | ---       | 1.0    | PATH |
| F[20]      | ---        | 0.3    | ---       | 1.2    | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK-----  
>TIMING>SETUP HOLD>

\*\*\*\*\*  
Genesil Screen Dump -- Wed Jun 8 17:10:40 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|                |     |      |     |      |      |
|----------------|-----|------|-----|------|------|
| F[20]          | --- | 0.3  | --- | 1.2  | PATH |
| F[21]          | --- | 0.3  | --- | 1.2  | PATH |
| F[22]          | --- | 0.3  | --- | 1.2  | PATH |
| F[23]          | --- | 0.2  | --- | 1.2  | PATH |
| F[24]          | --- | 0.2  | --- | 1.2  | PATH |
| F[25]          | --- | 0.2  | --- | 1.2  | PATH |
| F[26]          | --- | 0.2  | --- | 1.2  | PATH |
| F[27]          | --- | 0.2  | --- | 1.2  | PATH |
| F[28]          | --- | 0.2  | --- | 1.2  | PATH |
| F[29]          | --- | 0.2  | --- | 1.2  | PATH |
| F[2]           | --- | 0.4  | --- | 1.1  | PATH |
| F[30]          | --- | 0.2  | --- | 1.2  | PATH |
| F[31]          | --- | 0.2  | --- | 1.2  | PATH |
| F[3]           | --- | 0.4  | --- | 1.1  | PATH |
| F[4]           | --- | 0.3  | --- | 1.1  | PATH |
| F[5]           | --- | 0.3  | --- | 1.1  | PATH |
| F[6]           | --- | 0.3  | --- | 1.1  | PATH |
| F[7]           | --- | 0.3  | --- | 1.1  | PATH |
| F[8]           | --- | 0.3  | --- | 1.1  | PATH |
| F[9]           | --- | 0.3  | --- | 1.1  | PATH |
| IO_opcode[0]   | --- | 24.0 | --- | -7.3 | PATH |
| IO_opcode[1]   | --- | 22.7 | --- | -7.4 | PATH |
| IO_opcode[2]   | --- | 24.2 | --- | -8.3 | PATH |
| IO_chip_select | --- | 8.2  | --- | -4.9 | PATH |
| N_mem_read     | --- | 5.6  | --- | -2.2 | PATH |
| N_mem_write    | --- | 7.0  | --- | -3.6 | PATH |
| set_run        | --- | 4.5  | --- | -1.2 | PATH |
| set_sync       | --- | ---  | --- | ---  | PATH |
| R[0]           | --- | 0.3  | --- | 1.3  | PATH |
| R[10]          | --- | 0.4  | --- | 1.3  | PATH |
| R[11]          | --- | 0.4  | --- | 1.3  | PATH |
| R[12]          | --- | 0.4  | --- | 1.2  | PATH |
| R[13]          | --- | 0.4  | --- | 1.2  | PATH |
| R[14]          | --- | 0.4  | --- | 1.2  | PATH |
| R[15]          | --- | 0.4  | --- | 1.2  | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY-----  
BACK-----  
>TIMING>SETUP HOLD>

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\*\*\*\*\*  
 Genesil Screen Dump -- Wed Jun 8 17:10:50 1988  
 \*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0 Beta-----

|              |     |      |     |       |      |
|--------------|-----|------|-----|-------|------|
| R[12]        | --- | 0.4  | --- | 1.2   | PATH |
| R[13]        | --- | 0.4  | --- | 1.2   | PATH |
| R[14]        | --- | 0.4  | --- | 1.2   | PATH |
| R[15]        | --- | 0.4  | --- | 1.2   | PATH |
| R[16]        | --- | 0.4  | --- | 1.2   | PATH |
| R[17]        | --- | 0.5  | --- | 1.2   | PATH |
| R[18]        | --- | 0.5  | --- | 1.2   | PATH |
| R[19]        | --- | 0.5  | --- | 1.2   | PATH |
| R[1]         | --- | 0.3  | --- | 1.3   | PATH |
| R[20]        | --- | 0.5  | --- | 1.1   | PATH |
| R[21]        | --- | 0.6  | --- | 1.1   | PATH |
| R[22]        | --- | 0.6  | --- | 1.0   | PATH |
| R[23]        | --- | 0.6  | --- | 1.0   | PATH |
| R[24]        | --- | 0.7  | --- | 1.0   | PATH |
| R[25]        | --- | 0.7  | --- | 1.0   | PATH |
| R[26]        | --- | 0.7  | --- | 1.0   | PATH |
| R[27]        | --- | 0.7  | --- | 0.9   | PATH |
| R[28]        | --- | 0.7  | --- | 0.9   | PATH |
| R[29]        | --- | 0.7  | --- | 0.9   | PATH |
| R[2]         | --- | 0.3  | --- | 1.3   | PATH |
| R[30]        | --- | 0.8  | --- | 0.9   | PATH |
| R[31]        | --- | 0.8  | --- | 0.9   | PATH |
| R[3]         | --- | 0.3  | --- | 1.3   | PATH |
| R[4]         | --- | 0.4  | --- | 1.3   | PATH |
| R[5]         | --- | 0.4  | --- | 1.3   | PATH |
| R[6]         | --- | 0.4  | --- | 1.3   | PATH |
| R[7]         | --- | 0.4  | --- | 1.3   | PATH |
| R[8]         | --- | 0.4  | --- | 1.3   | PATH |
| R[9]         | --- | 0.4  | --- | 1.3   | PATH |
| R_bus_en[0]  | --- | 16.8 | --- | -13.4 | PATH |
| R_bus_en[1]  | --- | 17.4 | --- | -14.1 | PATH |
| R_eq_f_2     | --- | 0.4  | --- | 1.0   | PATH |
| Serial_in    | --- | ---  | --- | ---   | PATH |
| Transfer_in  | --- | ---  | --- | ---   | PATH |
| Transfer_out | --- | ---  | --- | ---   | PATH |

-----  
 INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY  
-----BACK

&gt;TIMING&gt;SETUP HOLD&gt;

\*\*\*\*\*  
Genesil Screen Dump -- Wed Jun 8 17:11:08 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## CLOCK REPORT MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Proc\_clk

Included setup files:

#0 nom\_phase\_a

(nominal op. cond. for Proc\_clk)

## CLOCK TIMES (minimum)

Phase 1 High: 20.8 ns

Phase 2 High: 24.2 ns

Cycle (from Ph1): 41.7 ns

Cycle (from Ph2): 70.2 ns

Minimum Cycle Time: 70.2 ns

Symmetric Cycle Time: 70.2 ns

## CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 20.8 ns set by:

\*\* Clock delay: 1.8ns (22.6-20.8)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| host_data_latch/(internal)     | 22.6             | rise       |
| host_data_latch/wr[1]          | 21.0             | fall       |
| host_data_latch/wr[1]'         | 20.8             | fall       |
| host_data_latch/dec_en         | 19.6             | fall       |
| host_data_latch/host_proc_mwtc | 18.0             | fall       |
| <oc_sync/stage2/host_proc_mwtc | 16.6             | fall       |
| <c_sync/stage2/host_proc_mwtc' | 7.1              | fall       |
| <st_proc_sync/stage2/n_cs_sync | 6.2              | rise       |
| host_proc_sync/stage2/cs_sync  | 5.4              | fall       |
| host_proc_sync/stage1/cs_sync  | 5.3              | fall       |
| host_proc_sync/stage1/cs_sync' | 5.0              | fall       |
| host_proc_sync/stage1/PHASE_A  | 2.2              | rise       |
| Proc_clk/PHASE_A               | 1.2              | rise       |
| Proc_clk                       | 0.0              | rise       |

| INSERT | MESSAGES | GRAPHICS | FORM | OVERLAY | RECORD | UTILITY |
|--------|----------|----------|------|---------|--------|---------|
|--------|----------|----------|------|---------|--------|---------|

BACK

PHASE1\_HIGH

CYCLE\_PH1

DUMP\_LATCH\_THRESHOLD

PHASE2\_HIGH

CYCLE\_PH2

DUMP\_LATCH

&gt;TIMING&gt;CLOCKS&gt;

\*\*\*\*\*  
Genesil Screen Dump -- Wed Jun 8 17:11:16 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

Proc\_clk

0.0

rise

Minimum Phase 2 high time is 24.2 ns set by:

\*\* Clock delay: 3.8ns (28.0-24.2)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| Rd[5]/(internal)               | 28.0             | rise       |
| R[29]                          | 23.7             | fall       |
| Rd[5]/r                        | 17.4             | fall       |
| proc_out_mux/r[29]             | 16.4             | fall       |
| proc_out_mux/r[29]'            | 12.2             | fall       |
| proc_out_mux/net_read          | 9.7              | rise       |
| opcode_decoder/net_read        | 9.3              | rise       |
| opcode_decoder/net_read'       | 8.6              | rise       |
| opcode_decoder/n_io_opcode[2]  | 7.6              | rise       |
| opcode_decoder/n_io_opcode[2]' | 7.5              | rise       |
| opcode_decoder/io_opcode[2]    | 6.2              | fall       |
| IO_opcode[2]/io_opcode         | 4.6              | fall       |
| IO_opcode[2]/io_opcode'        | 3.5              | fall       |
| IO_opcode[2]                   | 0.0              | fall       |

Minimum cycle time (from Ph1) is 41.7 ns set by:

\*\* Clock delay: 2.1ns (43.8-41.7)

| Node                      | Cumulative Delay | Transition |
|---------------------------|------------------|------------|
| proc_host_fifo/(internal) | 43.8             | fall       |
| proc_host_fifo/r[29]      | 43.5             | rise       |
| proc_in_mux/proc_din[29]  | 42.9             | rise       |
| proc_in_mux/proc_din[29]' | 39.5             | rise       |
| proc_in_mux/r_in[29]      | 38.2             | rise       |
| Rd[5]/r_in                | 37.7             | rise       |
| Rd[5]/r_in'               | 37.6             | rise       |
| *Rd[5]/(internal)         | 36.1             | fall       |
| R[29]                     | 33.4             | rise       |
| Rd[5]/r                   | 27.8             | rise       |

| INSERT | MESSAGES    | GRAPHICS  | FORM                 | OVERLAY | RECORD | UTILITY |
|--------|-------------|-----------|----------------------|---------|--------|---------|
| BACK   | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |         |        |         |
|        | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |         |        |         |

&gt;TIMING&gt;CLOCKS&gt;

\*\*\*\*\*  
Genesil Screen Dump -- Wed Jun 8 17:11:25 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|                                |      |      |
|--------------------------------|------|------|
| Rd[5]/r                        | 27.8 | rise |
| proc_out_mux/r[29]             | 26.8 | rise |
| proc_out_mux/r[29]'            | 23.4 | rise |
| proc_out_mux/net_proc_do[29]   | 22.1 | rise |
| net_proc_fifo/net_proc_do[29]  | 21.8 | rise |
| net_proc_fifo/net_proc_do[29]' | 21.8 | rise |
| net_proc_fifo/PHASE_A          | 2.2  | rise |
| Proc_clk/PHASE_A               | 1.2  | rise |
| Proc_clk                       | 0.0  | rise |

Minimum cycle time (from Ph2) is 70.2 ns set by:

\*\* Clock delay: 2.1ns (37.2-35.1) cycle sharing disabled

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| Data[2]                        | 59.3             | fall       |
| Data[2]/host dout              | 53.6             | fall       |
| <ceiver/8to1_mux/host dout[2]  | 53.3             | fall       |
| <ceiver/8to1_mux/host dout[2]' | 51.1             | fall       |
| <ver/8to1_mux/proc_host_do[10] | 46.8             | fall       |
| <ceiver/latch/ph_do latch[10]  | 46.8             | fall       |
| <ceiver/latch/ph_do latch[10]' | 46.6             | fall       |
| <ceiver/latch/proc_host_do[10] | 43.1             | fall       |
| <oc host_fifo/proc_host_do[10] | 42.8             | fall       |
| <c host_fifo/proc_host_do[10]' | 42.0             | fall       |
| *proc_host_fifo/(Internal)     | 35.9             | rise       |
| proc_host_fifo/r[10]           | 35.5             | fall       |
| proc_in_mux/proc_din[10]       | 35.3             | fall       |
| proc_in_mux/proc_din[10]'      | 31.9             | fall       |
| proc_in_mux/r_in[10]           | 30.4             | fall       |
| Rb[2]/r_in                     | 29.2             | fall       |
| Rb[2]/r_in'                    | 28.3             | fall       |
| R[10]                          | 23.7             | fall       |
| Rb[2]/r                        | 17.4             | fall       |
| proc_out_mux/r[10]             | 16.4             | fall       |
| proc_out_mux/r[10]'            | 12.2             | fall       |

| INSERT | MESSAGES    | GRAPHICS  | FORM                 | OVERLAY | RECORD | UTILITY |
|--------|-------------|-----------|----------------------|---------|--------|---------|
| BACK   | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |         |        |         |
|        | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |         |        |         |

&gt;TIMING&gt;CLOCKS&gt;

\*\*\*\*\*  
 Genesil Screen Dump -- Wed Jun 8 17:11:30 1988  
 \*\*\*\*\*

\*\*\*\*\*  
 hip: ~sni/sni/xserial Timing Analyzer  
 \*\*\*\*\*

-----Genesil Version v7.0 Beta-----  
 Minimum cycle time (from Ph2) is 70.2 ns set by:

\*\*\*\*\*  
 \*\* Clock delay: 2.1ns (37.2-35.1) cycle sharing disabled  
 \*\*\*\*\*

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| Data[2]                        | 59.3             | fall       |
| Data[2]/host dout              | 53.6             | fall       |
| <ceiver/8to1_mux/host_dout[2]  | 53.3             | fall       |
| <ceiver/8to1_mux/host_dout[2]' | 51.1             | fall       |
| <ver/8to1_mux/proc_host_do[10] | 46.8             | fall       |
| <ceiver/latch/ph_do latch[10]  | 46.8             | fall       |
| <ceiver/latch/ph_do latch[10]' | 46.6             | fall       |
| <ceiver/latch/proc_host_do[10] | 43.1             | fall       |
| <oc host fifo/proc_host_do[10] | 42.8             | fall       |
| <c host fifo/proc_host_do[10]' | 42.0             | fall       |
| *proc host fifo/(Internal)     | 35.9             | rise       |
| proc_host_fifo/r[10]           | 35.5             | fall       |
| proc_in_mux/proc_din[10]       | 35.3             | fall       |
| proc_in_mux/proc_din[10]'      | 31.9             | fall       |
| proc_in_mux/r_in[10]           | 30.4             | fall       |
| Rb[2]/r_in                     | 29.2             | fall       |
| Rb[2]/r_in'                    | 28.3             | fall       |
| R[10]                          | 23.7             | fall       |
| Rb[2]/r                        | 17.4             | fall       |
| proc_out_mux/r[10]             | 16.4             | fall       |
| proc_out_mux/r[10]'            | 12.2             | fall       |
| proc_out_mux/net_read          | 9.7              | rise       |
| opcode_decoder/net_read        | 9.3              | rise       |
| opcode_decoder/net_read'       | 8.6              | rise       |
| opcode_decoder/n_io_opcode[2]  | 7.6              | rise       |
| opcode_decoder/n_io_opcode[2]' | 7.5              | rise       |
| opcode_decoder/io_opcode[2]    | 6.2              | fall       |
| IO_opcode[2]/io_opcode         | 4.6              | fall       |
| IO_opcode[2]/io_opcode'        | 3.5              | fall       |
| IO_opcode[2]                   | 0.0              | fall       |

-----  
 INSERT    MESSAGES    GRAPHICS    FORM                    OVERLAY                    RECORD                    UTILITY  
 -----  
 BACK                    PHASE1\_HIGH            CYCLE\_PH1                DUMP\_LATCH\_THRESHOLD  
                          PHASE2\_HIGH            CYCLE\_PH2                DUMP\_LATCH  
 -----

>TIMING>CLOCKS>

\*\*\*\*\*  
Genesil Screen Dump -- Wed Jun 8 17:11:50 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## OUTPUT DELAY MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Proc\_clk

Included setup files:

#0 nom\_phase\_a

(nominal op. cond. for Proc\_clk)

-----  
OUTPUT DELAYS (ns)

| Output    | Ph1(r) Delay | Ph2(r) Delay | Loading(pf) |
|-----------|--------------|--------------|-------------|
|           | Min Max      | Min Max      |             |
| Data[0]   | 0.0 25.8     | 0.0 24.2     | 50.00 PATH  |
| Data[1]   | 0.0 25.8     | 0.0 24.2     | 50.00 PATH  |
| Data[2]   | 0.0 25.8     | 0.0 24.2     | 50.00 PATH  |
| Data[3]   | 0.0 25.9     | 0.0 24.2     | 50.00 PATH  |
| Data[4]   | 0.0 25.9     | 0.0 24.1     | 50.00 PATH  |
| Data[5]   | 0.0 25.8     | 0.0 24.0     | 50.00 PATH  |
| Data[6]   | 0.0 26.1     | 0.0 24.3     | 50.00 PATH  |
| Data[7]   | 0.0 26.3     | 0.0 24.7     | 50.00 PATH  |
| av        | ---          | ---          | 50.00 PATH  |
| Host_dav  | 12.6 13.8    | ---          | 50.00 PATH  |
| Host_rfi  | 16.1 18.8    | ---          | 50.00 PATH  |
| xaack     | 12.9 18.2    | 15.0 18.2    | 50.00 PATH  |
| et_dav    | 12.7 13.9    | ---          | 50.00 PATH  |
| Net_error | 13.5 28.1    | ---          | 50.00 PATH  |
| Net_rfi   | 14.8 28.0    | ---          | 50.00 PATH  |
| roc_run   | 11.9 14.3    | ---          | 50.00 PATH  |
| R[0]      | 0.0 30.4     | 0.0 21.6     | 50.00 PATH  |
| R[10]     | 0.0 33.2     | 0.0 23.7     | 50.00 PATH  |
| [11]      | 0.0 32.0     | 0.0 22.3     | 50.00 PATH  |
| [12]      | 0.0 31.6     | 0.0 21.8     | 50.00 PATH  |
| R[13]     | 0.0 31.5     | 0.0 21.7     | 50.00 PATH  |
| R[14]     | 0.0 31.4     | 0.0 21.5     | 50.00 PATH  |
| [15]      | 0.0 31.3     | 0.0 21.4     | 50.00 PATH  |
| R[16]     | 0.0 30.2     | 0.0 21.2     | 50.00 PATH  |

-----  
INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY

BACK

-----  
>TIMING>OUTPUT DELAY>

\*\*\*\*\*  
 Genesil Screen Dump -- Wed Jun 8 17:11:59 1988  
 \*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0 Beta-----

|            |      |      |     |      |       |      |
|------------|------|------|-----|------|-------|------|
| Proc_run   | 11.9 | 14.3 | --- | ---  | 50.00 | PATH |
| R[0]       | 0.0  | 30.4 | 0.0 | 21.6 | 50.00 | PATH |
| R[10]      | 0.0  | 33.2 | 0.0 | 23.7 | 50.00 | PATH |
| R[11]      | 0.0  | 32.0 | 0.0 | 22.3 | 50.00 | PATH |
| R[12]      | 0.0  | 31.6 | 0.0 | 21.8 | 50.00 | PATH |
| R[13]      | 0.0  | 31.5 | 0.0 | 21.7 | 50.00 | PATH |
| R[14]      | 0.0  | 31.4 | 0.0 | 21.5 | 50.00 | PATH |
| R[15]      | 0.0  | 31.3 | 0.0 | 21.4 | 50.00 | PATH |
| R[16]      | 0.0  | 30.2 | 0.0 | 21.2 | 50.00 | PATH |
| R[17]      | 0.0  | 30.1 | 0.0 | 21.1 | 50.00 | PATH |
| R[18]      | 0.0  | 30.0 | 0.0 | 20.9 | 50.00 | PATH |
| R[19]      | 0.0  | 29.9 | 0.0 | 20.8 | 50.00 | PATH |
| R[1]       | 0.0  | 30.6 | 0.0 | 21.8 | 50.00 | PATH |
| R[20]      | 0.0  | 30.0 | 0.0 | 20.9 | 50.00 | PATH |
| R[21]      | 0.0  | 30.2 | 0.0 | 21.1 | 50.00 | PATH |
| R[22]      | 0.0  | 30.3 | 0.0 | 21.2 | 50.00 | PATH |
| R[23]      | 0.0  | 30.3 | 0.0 | 21.2 | 50.00 | PATH |
| R[24]      | 0.0  | 30.4 | 0.0 | 21.3 | 50.00 | PATH |
| R[25]      | 0.0  | 30.5 | 0.0 | 21.4 | 50.00 | PATH |
| R[26]      | 0.0  | 30.6 | 0.0 | 21.6 | 50.00 | PATH |
| R[27]      | 0.0  | 31.7 | 0.0 | 21.7 | 50.00 | PATH |
| R[28]      | 0.0  | 31.8 | 0.0 | 21.9 | 50.00 | PATH |
| R[29]      | 0.0  | 33.4 | 0.0 | 23.7 | 50.00 | PATH |
| R[2]       | 0.0  | 30.8 | 0.0 | 22.0 | 50.00 | PATH |
| R[30]      | 0.0  | 32.8 | 0.0 | 23.1 | 50.00 | PATH |
| R[31]      | 0.0  | 32.6 | 0.0 | 22.8 | 50.00 | PATH |
| R[3]       | 0.0  | 31.2 | 0.0 | 22.4 | 50.00 | PATH |
| R[4]       | 0.0  | 31.3 | 0.0 | 22.6 | 50.00 | PATH |
| R[5]       | 0.0  | 32.4 | 0.0 | 22.7 | 50.00 | PATH |
| R[6]       | 0.0  | 32.5 | 0.0 | 22.9 | 50.00 | PATH |
| R[7]       | 0.0  | 32.7 | 0.0 | 23.1 | 50.00 | PATH |
| R[8]       | 0.0  | 32.8 | 0.0 | 23.3 | 50.00 | PATH |
| R[9]       | 0.0  | 33.1 | 0.0 | 23.5 | 50.00 | PATH |
| fi         | ---  | ---  | --- | ---  | 50.00 | PATH |
| Serial_out | ---  | ---  | --- | ---  | 50.00 | PATH |

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|        |          |          |      |         |        |         |
|--------|----------|----------|------|---------|--------|---------|
| INSERT | MESSAGES | GRAPHICS | FORM | OVERLAY | RECORD | UTILITY |
|--------|----------|----------|------|---------|--------|---------|

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BACK

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>TIMING>OUTPUT DELAY>

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 07:52:49 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

SETUP AND HOLD MODE

Tabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature:47 deg C

Voltage:5.00v

External Clock: Net\_clk

Included setup files:

#0 nom\_phase\_c

(nominal op. cond. for Net\_clk)

INPUT SETUP AND HOLD TIMES (ns)

| Input      | Setup Time |        | Hold Time |        |      |
|------------|------------|--------|-----------|--------|------|
|            | Ph1(f)     | Ph2(f) | Ph1(f)    | Ph2(f) |      |
| Address[0] | ---        | 7.4    | ---       | -4.1   | PATH |
| Address[1] | ---        | 7.5    | ---       | -4.2   | PATH |
| Address[2] | ---        | 7.5    | ---       | -4.1   | PATH |
| Data[0]    | ---        | 5.0    | ---       | -3.2   | PATH |
| Data[1]    | ---        | 5.1    | ---       | -3.2   | PATH |
| Data[2]    | ---        | 5.0    | ---       | -3.2   | PATH |
| Data[3]    | ---        | 5.1    | ---       | -3.2   | PATH |
| Data[4]    | ---        | 5.7    | ---       | -4.0   | PATH |
| Data[5]    | ---        | 5.7    | ---       | -4.0   | PATH |
| Data[6]    | ---        | 5.7    | ---       | -4.0   | PATH |
| Data[7]    | ---        | 5.7    | ---       | -4.0   | PATH |
| [0]        | ---        | ---    | ---       | ---    | PATH |
| [10]       | ---        | ---    | ---       | ---    | PATH |
| F[11]      | ---        | ---    | ---       | ---    | PATH |
| [12]       | ---        | ---    | ---       | ---    | PATH |
| [13]       | ---        | ---    | ---       | ---    | PATH |
| F[14]      | ---        | ---    | ---       | ---    | PATH |
| F[15]      | ---        | ---    | ---       | ---    | PATH |
| [16]       | ---        | ---    | ---       | ---    | PATH |
| [17]       | ---        | ---    | ---       | ---    | PATH |
| F[18]      | ---        | ---    | ---       | ---    | PATH |
| [19]       | ---        | ---    | ---       | ---    | PATH |
| [1]        | ---        | ---    | ---       | ---    | PATH |
| F[20]      | ---        | ---    | ---       | ---    | PATH |

INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

BACK

>TIMING>SETUP HOLD>

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 07:53:01 1988  
 \*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|               |     |      |     |      |      |
|---------------|-----|------|-----|------|------|
| F[20]         | --- | ---  | --- | ---  | PATH |
| F[21]         | --- | ---  | --- | ---  | PATH |
| F[22]         | --- | ---  | --- | ---  | PATH |
| F[23]         | --- | ---  | --- | ---  | PATH |
| F[24]         | --- | ---  | --- | ---  | PATH |
| F[25]         | --- | ---  | --- | ---  | PATH |
| F[26]         | --- | ---  | --- | ---  | PATH |
| F[27]         | --- | ---  | --- | ---  | PATH |
| F[28]         | --- | ---  | --- | ---  | PATH |
| F[29]         | --- | ---  | --- | ---  | PATH |
| F[2]          | --- | ---  | --- | ---  | PATH |
| F[30]         | --- | ---  | --- | ---  | PATH |
| F[31]         | --- | ---  | --- | ---  | PATH |
| F[3]          | --- | ---  | --- | ---  | PATH |
| F[4]          | --- | ---  | --- | ---  | PATH |
| F[5]          | --- | ---  | --- | ---  | PATH |
| F[6]          | --- | ---  | --- | ---  | PATH |
| F[7]          | --- | ---  | --- | ---  | PATH |
| F[8]          | --- | ---  | --- | ---  | PATH |
| F[9]          | --- | ---  | --- | ---  | PATH |
| IO_opcode[0]  | --- | ---  | --- | ---  | PATH |
| IO_opcode[1]  | --- | ---  | --- | ---  | PATH |
| IO_opcode[2]  | --- | ---  | --- | ---  | PATH |
| N_chip_select | --- | 5.7  | --- | -2.4 | PATH |
| N_mem_read    | --- | ---  | --- | ---  | PATH |
| N_mem_write   | --- | 5.8  | --- | -2.5 | PATH |
| Net_run       | --- | 21.1 | --- | -4.1 | PATH |
| Net_sync      | --- | 5.3  | --- | -2.6 | PATH |
| R[0]          | --- | ---  | --- | ---  | PATH |
| R[10]         | --- | ---  | --- | ---  | PATH |
| R[11]         | --- | ---  | --- | ---  | PATH |
| R[12]         | --- | ---  | --- | ---  | PATH |
| R[13]         | --- | ---  | --- | ---  | PATH |
| R[14]         | --- | ---  | --- | ---  | PATH |
| R[15]         | --- | ---  | --- | ---  | PATH |

-----INSERT MESSAGES GRAPHICS FORM-----

OVERLAY

RECORD

UTILITY

-----  
 BACK-----  
 >TIMING>SETUP HOLD>

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 07:53:11 1988  
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Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|              |     |      |     |      |      |
|--------------|-----|------|-----|------|------|
| R[12]        | --- | ---  | --- | ---  | PATH |
| R[13]        | --- | ---  | --- | ---  | PATH |
| R[14]        | --- | ---  | --- | ---  | PATH |
| R[15]        | --- | ---  | --- | ---  | PATH |
| R[16]        | --- | ---  | --- | ---  | PATH |
| R[17]        | --- | ---  | --- | ---  | PATH |
| R[18]        | --- | ---  | --- | ---  | PATH |
| R[19]        | --- | ---  | --- | ---  | PATH |
| R[1]         | --- | ---  | --- | ---  | PATH |
| R[20]        | --- | ---  | --- | ---  | PATH |
| R[21]        | --- | ---  | --- | ---  | PATH |
| R[22]        | --- | ---  | --- | ---  | PATH |
| R[23]        | --- | ---  | --- | ---  | PATH |
| R[24]        | --- | ---  | --- | ---  | PATH |
| R[25]        | --- | ---  | --- | ---  | PATH |
| R[26]        | --- | ---  | --- | ---  | PATH |
| R[27]        | --- | ---  | --- | ---  | PATH |
| R[28]        | --- | ---  | --- | ---  | PATH |
| R[29]        | --- | ---  | --- | ---  | PATH |
| R[2]         | --- | ---  | --- | ---  | PATH |
| R[30]        | --- | ---  | --- | ---  | PATH |
| R[31]        | --- | ---  | --- | ---  | PATH |
| R[3]         | --- | ---  | --- | ---  | PATH |
| R[4]         | --- | ---  | --- | ---  | PATH |
| R[5]         | --- | ---  | --- | ---  | PATH |
| R[6]         | --- | ---  | --- | ---  | PATH |
| R[7]         | --- | ---  | --- | ---  | PATH |
| R[8]         | --- | ---  | --- | ---  | PATH |
| R[9]         | --- | ---  | --- | ---  | PATH |
| R_bus_en[0]  | --- | ---  | --- | ---  | PATH |
| R_bus_en[1]  | --- | ---  | --- | ---  | PATH |
| R_eq_f_2     | --- | ---  | --- | ---  | PATH |
| Serial_in    | --- | 5.4  | --- | -2.5 | PATH |
| Transfer_in  | --- | 4.8  | --- | -3.3 | PATH |
| Transfer_out | --- | 13.9 | --- | -4.9 | PATH |

-----  
 INSERT    MESSAGES    GRAPHICS    FORM                    OVERLAY                    RECORD                    UTILITY  
 -----

BACK

-----  
 >TIMING>SETUP HOLD>

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 07:54:09 1988

\*\*\*\*\*  
 Chip: ~sni/sni/xserial

\*\*\*\*\*  
 Timing Analyzer

-----Genesil Version v7.0\_Beta-----

CLOCK REPORT MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Net\_clk

Included setup files:

#0 nom\_phase\_c (nominal op. cond. for Net\_clk)

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 CLOCK TIMES (minimum)  
 Phase 1 High: 19.9 ns Phase 2 High: 21.1 ns  
 Cycle (from Ph1): 34.6 ns Cycle (from Ph2): 29.5 ns  
 Minimum Cycle Time: 41.0 ns Symmetric Cycle Time: 42.2 ns  
 -----

CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 19.9 ns set by:

\*\* Clock delay: 4.0ns (23.9-19.9)

| Node                     | Cumulative Delay | Transition |
|--------------------------|------------------|------------|
| proc_net_fifo/(internal) | 23.9             | fall       |
| proc_net_fifo/PHASE_C    | 2.1              | rise       |
| Net_clk/PHASE_C          | 1.2              | rise       |
| Net_clk                  | 0.0              | rise       |

Minimum Phase 2 high time is 21.1 ns set by:

\*\* Clock delay: 2.3ns (23.4-21.1)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| <c_net_con/prefetch/(internal) | 23.4             | fall       |
| proc_net_con/prefetch/dav_ld   | 21.2             | fall       |
| <et_con/prefetch/proc_net_read | 19.5             | fall       |
| <t_con/prefetch/proc_net_read' | 18.7             | fall       |
| proc_net_con/prefetch/n_dav_rd | 17.8             | fall       |

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 INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY

BACK PHASE1\_HIGH CYCLE\_PH1 DUMP\_LATCH\_THRESHOLD  
 PHASE2\_HIGH CYCLE\_PH2 DUMP\_LATCH

-----  
 >TIMING>CLOCKS>

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 07:54:18 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|                                |      |      |
|--------------------------------|------|------|
| proc_net_con/prefetch/n_dav_rd | 17.8 | fall |
| <oc_net_con/prefetch/fifo_read | 16.3 | fall |
| <_net_con/rd_control/fifo_read | 16.3 | fall |
| <net_con/rd_control/fifo_read' | 15.3 | fall |
| <c_net_con/rd_control/xfer_out | 14.1 | fall |
| <_net_con/rd_control/xfer_out' | 12.8 | fall |
| proc_net_con/rd_control/n_run  | 11.1 | fall |
| host_proc_sync/sync_run/n_run  | 7.4  | fall |
| host_proc_sync/sync_run/n_run' | 4.4  | fall |
| host_proc_sync/sync_run/run    | 4.1  | rise |
| host_proc_sync/sync_run/run'   | 3.1  | rise |
| <st_proc_sync/sync_run/net_run | 2.0  | rise |
| Net_run/net_run                | 2.0  | rise |
| Net_run/net_run'               | 1.9  | rise |
| Net_run                        | 0.0  | rise |

Minimum cycle time (from Ph1) is 34.6 ns set by:

\*\* Clock delay: 2.4ns (37.0-34.6)

| Node                            | Cumulative Delay | Transition |
|---------------------------------|------------------|------------|
| ser_encoder/data_register/280   | 37.0             | fall       |
| *<der/data_register/(internal)  | 35.1             | fall       |
| <r_encoder/data_register/cb[0]  | 34.8             | rise       |
| <n_coder/parity_gen/xor16_0/out | 34.6             | rise       |
| <coder/parity_gen/xor16_0/out'  | 34.2             | rise       |
| <coder/parity_gen/xor16_0/m[0]  | 32.7             | fall       |
| <oder/parity_gen/xor16_0/m[0]'  | 32.7             | fall       |
| <coder/parity_gen/xor16_0/k[0]  | 30.4             | rise       |
| <oder/parity_gen/xor16_0/k[0]'  | 30.3             | rise       |
| <coder/parity_gen/xor16_0/j[1]  | 28.0             | fall       |
| <oder/parity_gen/xor16_0/j[1]'  | 27.9             | fall       |
| <oder/parity_gen/xor16_0/in[3]  | 25.8             | rise       |
| proc_net_fifo/proc_net_do[7]    | 23.5             | rise       |
| proc_net_fifo/proc_net_do[7]'   | 21.7             | rise       |
| proc_net_fifo/PHASE_C           | 2.1              | rise       |

| INSERT | MESSAGES    | GRAPHICS  | FORM                 | OVERLAY | RECORD | UTILITY |
|--------|-------------|-----------|----------------------|---------|--------|---------|
| BACK   | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |         |        |         |
|        | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |         |        |         |

&gt;TIMING&gt;CLOCKS&gt;

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 07:54:26 1988  
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\*\*\*\*\*  
 Chip: ~sni/sni/xserial  
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\*\*\*\*\*  
 Timing Analyzer  
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-----Genesil Version v7.0\_Beta-----

|                                |      |      |
|--------------------------------|------|------|
| <coder/parity_gen/xor16_0/m[0] | 32.7 | fall |
| <oder/parity_gen/xor16_0/m[0]' | 32.7 | fall |
| <coder/parity_gen/xor16_0/k[0] | 30.4 | rise |
| <oder/parity_gen/xor16_0/k[0]' | 30.3 | rise |
| <coder/parity_gen/xor16_0/j[1] | 28.0 | fall |
| <oder/parity_gen/xor16_0/j[1]' | 27.9 | fall |
| <oder/parity_gen/xor16_0/in[3] | 25.8 | rise |
| proc_net_fifo/proc_net_do[7]   | 23.5 | rise |
| proc_net_fifo/proc_net_do[7]'  | 21.7 | rise |
| proc_net_fifo/PHASE_C          | 2.1  | rise |
| Net_clk/PHASE_C                | 1.2  | rise |
| Net_clk                        | 0.0  | rise |

Minimum cycle time (from Ph2) is 29.5 ns set by:

\*\* Clock delay: 4.1ns (18.8-14.8) cycle sharing disabled

| Node                            | Cumulative Delay | Transition |
|---------------------------------|------------------|------------|
| <oder/data_register/(internal)  | 35.1             | rise       |
| <r_encoder/data_register/cb[5]  | 34.6             | fall       |
| <n_coder/parity_gen/xor16_5/out | 34.6             | fall       |
| <coder/parity_gen/xor16_5/out'  | 34.5             | fall       |
| <oder/parity_gen/xor16_5/m[0]   | 33.0             | rise       |
| <oder/parity_gen/xor16_5/m[0]'  | 33.0             | rise       |
| <oder/parity_gen/xor16_5/k[1]   | 30.6             | fall       |
| <oder/parity_gen/xor16_5/k[1]'  | 30.5             | fall       |
| <oder/parity_gen/xor16_5/j[3]   | 28.4             | rise       |
| <oder/parity_gen/xor16_5/j[3]'  | 28.3             | rise       |
| <oder/parity_gen/xor16_5/in[7]  | 26.0             | fall       |
| proc_net_fifo/proc_net_do[15]   | 24.0             | fall       |
| proc_net_fifo/proc_net_do[15]'  | 22.3             | fall       |
| *proc_net_fifo/(internal)       | 18.0             | fall       |
| proc_net_fifo/PHASE_C           | 1.9              | fall       |
| Net_clk/PHASE_C                 | 0.9              | fall       |
| Net_clk                         | 0.0              | fall       |

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 INSERT    MESSAGES    GRAPHICS    FORM    OVERLAY    RECORD    UTILITY  
 -----

|             |             |           |                      |
|-------------|-------------|-----------|----------------------|
| <u>BACK</u> | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |
|             | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |

-----  
 >TIMING>CLOCKS>

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 07:54:49 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## OUTPUT DELAY MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Net\_clk

Included setup files:

#0 nom\_phase\_c

(nominal op. cond. for Net\_clk)

\*\*\*\*\*  
OUTPUT DELAYS (ns)

| Output    | Ph1(r) Delay<br>Min Max | Ph2(r) Delay<br>Min Max | Loading(pf) |
|-----------|-------------------------|-------------------------|-------------|
| Data[0]   | 0.0 24.2                | 0.0 24.2                | 50.00 PATH  |
| Data[1]   | 0.0 24.2                | 0.0 24.2                | 50.00 PATH  |
| Data[2]   | 0.0 24.2                | 0.0 24.2                | 50.00 PATH  |
| Data[3]   | 0.0 24.2                | 0.0 24.2                | 50.00 PATH  |
| Data[4]   | 0.0 24.1                | 0.0 24.1                | 50.00 PATH  |
| Data[5]   | 0.0 24.0                | 0.0 24.0                | 50.00 PATH  |
| Data[6]   | 0.0 24.3                | 0.0 24.3                | 50.00 PATH  |
| Data[7]   | 0.0 24.7                | 0.0 24.7                | 50.00 PATH  |
| Dav       | 14.7 16.1               | ---                     | 50.00 PATH  |
| Host_dav  | ---                     | ---                     | 50.00 PATH  |
| Host_rfi  | ---                     | ---                     | 50.00 PATH  |
| N_xack    | 15.0 18.2               | 15.0 18.2               | 50.00 PATH  |
| Net_dav   | ---                     | ---                     | 50.00 PATH  |
| Net_error | ---                     | ---                     | 50.00 PATH  |
| Net_rfi   | ---                     | ---                     | 50.00 PATH  |
| Proc_run  | ---                     | ---                     | 50.00 PATH  |
| R[0]      | 0.0 21.6                | 0.0 21.6                | 50.00 PATH  |
| R[10]     | 0.0 23.7                | 0.0 23.7                | 50.00 PATH  |
| R[11]     | 0.0 22.3                | 0.0 22.3                | 50.00 PATH  |
| R[12]     | 0.0 21.8                | 0.0 21.8                | 50.00 PATH  |
| R[13]     | 0.0 21.7                | 0.0 21.7                | 50.00 PATH  |
| R[14]     | 0.0 21.5                | 0.0 21.5                | 50.00 PATH  |
| R[15]     | 0.0 21.4                | 0.0 21.4                | 50.00 PATH  |
| R[16]     | 0.0 21.2                | 0.0 21.2                | 50.00 PATH  |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY  
-----BACK

&gt;TIMING&gt;OUTPUT DELAY&gt;

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 07:54:59 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial\*\*\*\*\*  
Timing Analyzer

-----Genesil Version v7.0 Beta-----

|            |      |      |     |      |       |      |
|------------|------|------|-----|------|-------|------|
| Proc_run   | ---  | ---  | --- | ---  | 50.00 | PATH |
| R[0]       | 0.0  | 21.6 | 0.0 | 21.6 | 50.00 | PATH |
| R[10]      | 0.0  | 23.7 | 0.0 | 23.7 | 50.00 | PATH |
| R[11]      | 0.0  | 22.3 | 0.0 | 22.3 | 50.00 | PATH |
| R[12]      | 0.0  | 21.8 | 0.0 | 21.8 | 50.00 | PATH |
| R[13]      | 0.0  | 21.7 | 0.0 | 21.7 | 50.00 | PATH |
| R[14]      | 0.0  | 21.5 | 0.0 | 21.5 | 50.00 | PATH |
| R[15]      | 0.0  | 21.4 | 0.0 | 21.4 | 50.00 | PATH |
| R[16]      | 0.0  | 21.2 | 0.0 | 21.2 | 50.00 | PATH |
| R[17]      | 0.0  | 21.1 | 0.0 | 21.1 | 50.00 | PATH |
| R[18]      | 0.0  | 20.9 | 0.0 | 20.9 | 50.00 | PATH |
| R[19]      | 0.0  | 20.8 | 0.0 | 20.8 | 50.00 | PATH |
| R[1]       | 0.0  | 21.8 | 0.0 | 21.8 | 50.00 | PATH |
| R[20]      | 0.0  | 20.9 | 0.0 | 20.9 | 50.00 | PATH |
| R[21]      | 0.0  | 21.1 | 0.0 | 21.1 | 50.00 | PATH |
| R[22]      | 0.0  | 21.2 | 0.0 | 21.2 | 50.00 | PATH |
| R[23]      | 0.0  | 21.2 | 0.0 | 21.2 | 50.00 | PATH |
| R[24]      | 0.0  | 21.3 | 0.0 | 21.3 | 50.00 | PATH |
| R[25]      | 0.0  | 21.4 | 0.0 | 21.4 | 50.00 | PATH |
| R[26]      | 0.0  | 21.6 | 0.0 | 21.6 | 50.00 | PATH |
| R[27]      | 0.0  | 21.7 | 0.0 | 21.7 | 50.00 | PATH |
| R[28]      | 0.0  | 21.9 | 0.0 | 21.9 | 50.00 | PATH |
| R[29]      | 0.0  | 23.7 | 0.0 | 23.7 | 50.00 | PATH |
| R[2]       | 0.0  | 22.0 | 0.0 | 22.0 | 50.00 | PATH |
| R[30]      | 0.0  | 23.1 | 0.0 | 23.1 | 50.00 | PATH |
| R[31]      | 0.0  | 22.8 | 0.0 | 22.8 | 50.00 | PATH |
| R[3]       | 0.0  | 22.4 | 0.0 | 22.4 | 50.00 | PATH |
| R[4]       | 0.0  | 22.6 | 0.0 | 22.6 | 50.00 | PATH |
| R[5]       | 0.0  | 22.7 | 0.0 | 22.7 | 50.00 | PATH |
| R[6]       | 0.0  | 22.9 | 0.0 | 22.9 | 50.00 | PATH |
| R[7]       | 0.0  | 23.1 | 0.0 | 23.1 | 50.00 | PATH |
| R[8]       | 0.0  | 23.3 | 0.0 | 23.3 | 50.00 | PATH |
| R[9]       | 0.0  | 23.5 | 0.0 | 23.5 | 50.00 | PATH |
| afi        | 13.1 | 14.3 | --- | ---  | 50.00 | PATH |
| Serial_out | 12.0 | 13.0 | --- | ---  | 50.00 | PATH |

-----  
INSERT    MESSAGES    GRAPHICS    FORM                    OVERLAY                    RECORD                    UTILITY-----  
BACK-----  
>TIMING>OUTPUT DELAY>

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 14:27:34 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## PATH DELAY MODE

## BLOCK NAME

Labline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Net\_clk

Included setup files:

#0 nom\_phase\_c

(nominal op. cond. for Net\_clk)

|               |           | PATH DELAY (ns) |      |     |  |  | BLOCK NAME |
|---------------|-----------|-----------------|------|-----|--|--|------------|
| Source Object | Connector | (Ph1) Min       | Max  |     |  |  |            |
| Dest. Object  | Connector | (Ph2) Min       | Max  |     |  |  |            |
| R bus en[0]   | R bus en  | 14.8            | 16.1 |     |  |  | *CURRENT*  |
| Rd[7]         | R         | 14.8            | 16.1 | PAT |  |  | Address[0] |
| R bus en[0]   | R bus en  | 14.1            | 15.4 |     |  |  | Address[1] |
| Rc[7]         | R         | 14.1            | 15.4 | PAT |  |  | Address[2] |
| R bus en[0]   | R bus en  | 14.4            | 15.7 |     |  |  | Data[0]    |
| Rb[7]         | R         | 14.4            | 15.7 | PAT |  |  | Data[1]    |
| R bus en[0]   | R bus en  | 15.2            | 16.5 |     |  |  | Data[2]    |
| Ra[7]         | R         | 15.2            | 16.5 | PAT |  |  | Data[3]    |
| R bus en[0]   | R bus en  | 15.4            | 16.7 |     |  |  | Data[4]    |
| Ra[0]         | R         | 15.4            | 16.7 | PAT |  |  | Data[5]    |
| R bus en[1]   | R bus en  | 15.5            | 16.7 |     |  |  | Data[6]    |
| Rd[7]         | R         | 15.5            | 16.7 | PAT |  |  | Data[7]    |
| R bus en[1]   | R bus en  | 14.8            | 16.0 |     |  |  | Dav        |
| Rc[7]         | R         | 14.8            | 16.0 | PAT |  |  | F[0]       |
| R bus en[1]   | R bus en  | 15.1            | 16.3 |     |  |  | F[10]      |
| Rb[7]         | R         | 15.1            | 16.3 | PAT |  |  | F[11]      |
| R bus en[1]   | R bus en  | 15.9            | 17.1 |     |  |  | F[12]      |
| Ra[7]         | R         | 15.9            | 17.1 | PAT |  |  | F[13]      |
| R bus en[1]   | R bus en  | 16.1            | 17.4 |     |  |  | F[14]      |
| Ra[0]         | R         | 16.1            | 17.4 | PAT |  |  | F[15]      |
| IO opcode[0]  | IO opcode | 20.6            | 22.6 |     |  |  | F[16]      |
| Rd[7]         | R         | 20.6            | 22.6 | PAT |  |  | F[17]      |
| IO opcode[0]  | IO opcode | 19.2            | 21.0 |     |  |  | F[18]      |
| Rc[7]         | R         | 19.2            | 21.0 | PAT |  |  | F[19]      |
|               |           |                 |      |     |  |  | F[20]      |
|               |           |                 |      |     |  |  | F[21]      |
|               |           |                 |      |     |  |  | F[22]      |
|               |           |                 |      |     |  |  | F[23]      |
|               |           |                 |      |     |  |  | F[24]      |
|               |           |                 |      |     |  |  | F[25]      |
|               |           |                 |      |     |  |  | F[26]      |
|               |           |                 |      |     |  |  | F[27]      |
|               |           |                 |      |     |  |  | * MORE *   |

INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

BACK

PATH\_DELETE\_TOGGLE

Enter [string]:

&gt;TIMING&gt;PATH DELAY&gt;

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 14:27:47 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0 Beta-----+-----

| Rc[7]        | R         | 19.2 | 21.0 | PATH           | BLOCK NAME |
|--------------|-----------|------|------|----------------|------------|
| IO opcode[0] | IO opcode | 19.4 | 21.2 |                | *CURRENT*  |
| Rb[7]        | R         | 19.4 | 21.2 | PATHAddress[0] |            |
| IO opcode[0] | IO opcode | 20.8 | 22.9 |                | Address[1] |
| Ra[7]        | R         | 20.8 | 22.9 | PATHAddress[2] |            |
| IO opcode[0] | IO opcode | 19.5 | 21.4 |                | Data[0]    |
| Ra[0]        | R         | 19.5 | 21.4 | PATHData[1]    |            |
| IO opcode[1] | IO opcode | 19.9 | 21.3 |                | Data[2]    |
| Rd[7]        | R         | 19.9 | 21.3 | PATHData[3]    |            |
| IO opcode[1] | IO opcode | 18.5 | 19.7 |                | Data[4]    |
| Rc[7]        | R         | 18.5 | 19.7 | PATHData[5]    |            |
| IO opcode[1] | IO opcode | 18.7 | 19.9 |                | Data[6]    |
| Rb[7]        | R         | 18.7 | 19.9 | PATHData[7]    |            |
| IO opcode[1] | IO opcode | 20.1 | 21.6 |                | Dav        |
| Ra[7]        | R         | 20.1 | 21.6 | PATHF[0]       |            |
| IO opcode[1] | IO opcode | 18.8 | 20.0 |                | F[10]      |
| Ra[0]        | R         | 18.8 | 20.0 | PATHF[11]      |            |
| IO opcode[2] | IO opcode | 21.2 | 22.8 |                | F[12]      |
| Rd[7]        | R         | 21.2 | 22.8 | PATHF[13]      |            |
| IO opcode[2] | IO opcode | 19.8 | 21.2 |                | F[14]      |
| Rc[7]        | R         | 19.8 | 21.2 | PATHF[15]      |            |
| IO opcode[2] | IO opcode | 20.0 | 21.4 |                | F[16]      |
| Rb[7]        | R         | 20.0 | 21.4 | PATHF[17]      |            |
| IO opcode[2] | IO opcode | 21.4 | 23.1 |                | F[18]      |
| Ra[7]        | R         | 21.4 | 23.1 | PATHF[19]      |            |
| IO opcode[2] | IO opcode | 20.1 | 21.6 |                | F[1]       |
| Ra[0]        | R         | 20.1 | 21.6 | PATHF[20]      |            |
| Address[0]   | Address   | 21.4 | 24.7 |                | F[21]      |
| Data[7]      | Data      | 21.4 | 24.7 | PATHF[22]      |            |
| Address[0]   | Address   | 21.0 | 24.2 |                | F[23]      |
| Data[3]      | Data      | 21.0 | 24.2 | PATHF[24]      |            |
| Address[0]   | Address   | 21.0 | 24.2 |                | F[25]      |
| Data[0]      | Data      | 21.0 | 24.2 | PATHF[26]      |            |
| Address[1]   | Address   | 19.1 | 21.6 |                | F[27]      |
| Data[7]      | Data      | 19.1 | 21.6 | PATH           | * MORE *   |

| INSERT | MESSAGES           | GRAPHICS | FORM | OVERLAY | RECORD | UTILITY |
|--------|--------------------|----------|------|---------|--------|---------|
| BACK   | PATH_DELETE_TOGGLE |          |      |         |        |         |

Enter [string]:  
>TIMING>PATH DELAY>

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 14:28:01 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0 Beta-----+-----

| Data[3]       | Data          | 21.0 | 24.2 | PATH | BLOCK NAME |
|---------------|---------------|------|------|------|------------|
| Address[0]    | Address       | 21.0 | 24.2 |      | *CURRENT*  |
| Data[0]       | Data          | 21.0 | 24.2 | PATH | Address[0] |
| Address[1]    | Address       | 19.1 | 21.6 |      | Address[1] |
| Data[7]       | Data          | 19.1 | 21.6 | PATH | Address[2] |
| Address[1]    | Address       | 18.7 | 21.1 |      | Data[0]    |
| Data[3]       | Data          | 18.7 | 21.1 | PATH | Data[1]    |
| Address[1]    | Address       | 18.7 | 21.1 |      | Data[2]    |
| Data[0]       | Data          | 18.7 | 21.1 | PATH | Data[3]    |
| Address[2]    | Address       | 17.7 | 19.7 |      | Data[4]    |
| Data[7]       | Data          | 17.7 | 19.7 | PATH | Data[5]    |
| Address[2]    | Address       | 17.3 | 19.2 |      | Data[6]    |
| Data[3]       | Data          | 17.3 | 19.2 | PATH | Data[7]    |
| Address[2]    | Address       | 17.3 | 19.2 |      | Dav        |
| Data[0]       | Data          | 17.3 | 19.2 | PATH | F[0]       |
| N mem read    | N mem read    | 16.7 | 18.1 |      | F[10]      |
| Data[7]       | Data          | 16.7 | 18.1 | PATH | F[11]      |
| N mem read    | N mem read    | 16.9 | 18.3 |      | F[12]      |
| Data[3]       | Data          | 16.9 | 18.3 | PATH | F[13]      |
| N mem read    | N mem read    | 16.9 | 18.3 |      | F[14]      |
| Data[0]       | Data          | 16.9 | 18.3 | PATH | F[15]      |
| N chip select | N chip select | 18.3 | 19.7 |      | F[16]      |
| Data[7]       | Data          | 18.3 | 19.7 | PATH | F[17]      |
| N chip select | N chip select | 18.5 | 19.9 |      | F[18]      |
| Data[3]       | Data          | 18.5 | 19.9 | PATH | F[19]      |
| N chip select | N chip select | 18.5 | 19.9 |      | F[1]       |
| Data[0]       | Data          | 18.5 | 19.9 | PATH | F[20]      |
| N mem read    | N mem read    | 15.0 | 16.4 |      | F[21]      |
| N xack        | N xack        | 15.0 | 16.4 | PATH | F[22]      |
| N mem write   | N mem write   | 16.8 | 18.2 |      | F[23]      |
| N xack        | N xack        | 16.8 | 18.2 | PATH | F[24]      |
| N chip select | N chip select | 16.6 | 18.2 |      | F[25]      |
| N xack        | N xack        | 16.6 | 18.2 | PATH | F[26]      |
|               |               |      |      |      | F[27]      |

\* MORE \*

-----+-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

BACK

PATH\_DELETE\_TOGGLE

Enter [string]:  
>TIMING>PATH DELAY>

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 16:20:10 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## SETUP AND HOLD MODE

Fabline: NSC CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Net\_clk

Included setup files:

#0 max\_phase\_c

(max. temp. min v. for Net\_clk)

-----  
INPUT SETUP AND HOLD TIMES (ns)

| Input      | Setup Time |        | Hold Time |        | PATH |
|------------|------------|--------|-----------|--------|------|
|            | Ph1(f)     | Ph2(f) | Ph1(f)    | Ph2(f) |      |
| Address[0] | ---        | 8.4    | ---       | -4.7   | PATH |
| Address[1] | ---        | 8.5    | ---       | -4.8   | PATH |
| Address[2] | ---        | 8.5    | ---       | -4.7   | PATH |
| Data[0]    | ---        | 5.7    | ---       | -3.6   | PATH |
| Data[1]    | ---        | 5.8    | ---       | -3.7   | PATH |
| Data[2]    | ---        | 5.8    | ---       | -3.7   | PATH |
| Data[3]    | ---        | 5.8    | ---       | -3.7   | PATH |
| Data[4]    | ---        | 6.5    | ---       | -4.6   | PATH |
| Data[5]    | ---        | 6.5    | ---       | -4.6   | PATH |
| Data[6]    | ---        | 6.5    | ---       | -4.6   | PATH |
| Data[7]    | ---        | 6.5    | ---       | -4.5   | PATH |
| [0]        | ---        | ---    | ---       | ---    | PATH |
| [10]       | ---        | ---    | ---       | ---    | PATH |
| F[11]      | ---        | ---    | ---       | ---    | PATH |
| F[12]      | ---        | ---    | ---       | ---    | PATH |
| [13]       | ---        | ---    | ---       | ---    | PATH |
| [14]       | ---        | ---    | ---       | ---    | PATH |
| F[15]      | ---        | ---    | ---       | ---    | PATH |
| [16]       | ---        | ---    | ---       | ---    | PATH |
| [17]       | ---        | ---    | ---       | ---    | PATH |
| F[18]      | ---        | ---    | ---       | ---    | PATH |
| F[19]      | ---        | ---    | ---       | ---    | PATH |
| [1]        | ---        | ---    | ---       | ---    | PATH |
| [20]       | ---        | ---    | ---       | ---    | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK-----  
>TIMING>SETUP HOLD>

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 16:20:21 1988  
 \*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|               |     |      |     |      |      |
|---------------|-----|------|-----|------|------|
| F[20]         | --- | ---  | --- | ---  | PATH |
| F[21]         | --- | ---  | --- | ---  | PATH |
| F[22]         | --- | ---  | --- | ---  | PATH |
| F[23]         | --- | ---  | --- | ---  | PATH |
| F[24]         | --- | ---  | --- | ---  | PATH |
| F[25]         | --- | ---  | --- | ---  | PATH |
| F[26]         | --- | ---  | --- | ---  | PATH |
| F[27]         | --- | ---  | --- | ---  | PATH |
| F[28]         | --- | ---  | --- | ---  | PATH |
| F[29]         | --- | ---  | --- | ---  | PATH |
| F[2]          | --- | ---  | --- | ---  | PATH |
| F[30]         | --- | ---  | --- | ---  | PATH |
| F[31]         | --- | ---  | --- | ---  | PATH |
| F[3]          | --- | ---  | --- | ---  | PATH |
| F[4]          | --- | ---  | --- | ---  | PATH |
| F[5]          | --- | ---  | --- | ---  | PATH |
| F[6]          | --- | ---  | --- | ---  | PATH |
| F[7]          | --- | ---  | --- | ---  | PATH |
| F[8]          | --- | ---  | --- | ---  | PATH |
| F[9]          | --- | ---  | --- | ---  | PATH |
| IO_opcode[0]  | --- | ---  | --- | ---  | PATH |
| IO_opcode[1]  | --- | ---  | --- | ---  | PATH |
| IO_opcode[2]  | --- | ---  | --- | ---  | PATH |
| N_chip_select | --- | 6.5  | --- | -2.8 | PATH |
| N_mem_read    | --- | ---  | --- | ---  | PATH |
| N_mem_write   | --- | 6.6  | --- | -2.9 | PATH |
| Net_run       | --- | 23.6 | --- | -4.7 | PATH |
| Net_sync      | --- | 6.0  | --- | -3.1 | PATH |
| R[0]          | --- | ---  | --- | ---  | PATH |
| R[10]         | --- | ---  | --- | ---  | PATH |
| R[11]         | --- | ---  | --- | ---  | PATH |
| R[12]         | --- | ---  | --- | ---  | PATH |
| R[13]         | --- | ---  | --- | ---  | PATH |
| R[14]         | --- | ---  | --- | ---  | PATH |
| R[15]         | --- | ---  | --- | ---  | PATH |

-----  
 INSERT    MESSAGES    GRAPHICS    FORM

OVERLAY

RECORD

UTILITY  
 -----BACK
 -----  
 >TIMING>SETUP HOLD>

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 16:20:49 1988  
 \*\*\*\*\*

\*\*\*\*\*  
 Chip: ~sni/sni/xserial  
 \*\*\*\*\*

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## CLOCK REPORT MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Net\_clk

Included setup files:

#0 max\_phase\_c (max. temp. min v. for Net\_clk)

## CLOCK TIMES (minimum)

Phase 1 High: 22.1 ns

Phase 2 High: 23.6 ns

Cycle (from Ph1): 38.6 ns

Cycle (from Ph2): 32.8 ns

Minimum Cycle Time: 45.7 ns

Symmetric Cycle Time: 47.1 ns

## CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 22.1 ns set by:

\*\* Clock delay: 4.4ns (26.5-22.1)

| Node                     | Cumulative Delay | Transition |
|--------------------------|------------------|------------|
| proc_net_fifo/(internal) | 26.5             | fall       |
| proc_net_fifo/PHASE_C    | 2.2              | rise       |
| Net_clk/PHASE_C          | 1.2              | rise       |
| Net_clk                  | 0.0              | rise       |

Minimum Phase 2 high time is 23.6 ns set by:

\*\* Clock delay: 2.4ns (26.0-23.6)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| <c_net_con/prefetch/(internal) | 26.0             | fall       |
| proc_net_con/prefetch/dav_ld   | 23.6             | fall       |
| <et_con/prefetch/proc_net_read | 21.6             | fall       |
| <t_con/prefetch/proc_net_read' | 20.7             | fall       |
| proc_net_con/prefetch/n_dav_rd | 19.7             | fall       |

INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

BACKPHASE1\_HIGH  
PHASE2\_HIGHCYCLE\_PH1  
CYCLE\_PH2DUMP\_LATCH\_THRESHOLD  
DUMP\_LATCH

&gt;TIMING&gt;CLOCKS&gt;

\*\*\*\*\*  
 Genesil Screen Dump -- Thu Jun 9 16:21:16 1988

\*\*\*\*\*  
 Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|                                |      |      |
|--------------------------------|------|------|
| proc_net_con/prefetch/n_dav_rd | 19.7 | fall |
| <oc_net_con/prefetch/fifo_read | 18.1 | fall |
| <_net_con/rd_control/fifo_read | 18.1 | fall |
| <net_con/rd_control/fifo_read' | 17.0 | fall |
| <c_net_con/rd_control/xfer_out | 15.7 | fall |
| <_net_con/rd_control/xfer_out' | 14.2 | fall |
| proc_net_con/rd_control/n_run  | 12.3 | fall |
| host_proc_sync/sync_run/n_run  | 8.2  | fall |
| host_proc_sync/sync_run/n_run' | 4.9  | fall |
| host_proc_sync/sync_run/run    | 4.6  | rise |
| host_proc_sync/sync_run/run'   | 3.4  | rise |
| <st_proc_sync/sync_run/net_run | 2.3  | rise |
| Net_run/net_run                | 2.2  | rise |
| Net_run/net_run'               | 2.1  | rise |
| Net_run                        | 0.0  | rise |

Minimum cycle time (from Ph1) is 38.6 ns set by:

\*\* Clock delay: 2.5ns (41.1-38.6)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| ser_encoder/data_register/280  | 41.1             | fall       |
| *<der/data_register/(internal) | 39.0             | fall       |
| <r_encoder/data_register/cb[0] | 38.7             | rise       |
| <ncoder/parity_gen/xor16_0/out | 38.4             | rise       |
| <coder/parity_gen/xor16_0/out' | 38.1             | rise       |
| <coder/parity_gen/xor16_0/m[0] | 36.3             | fall       |
| <oder/parity_gen/xor16_0/m[0]' | 36.3             | fall       |
| <coder/parity_gen/xor16_0/k[0] | 33.8             | rise       |
| <oder/parity_gen/xor16_0/k[0]' | 33.7             | rise       |
| <coder/parity_gen/xor16_0/j[1] | 31.2             | fall       |
| <oder/parity_gen/xor16_0/j[1]' | 31.1             | fall       |
| <oder/parity_gen/xor16_0/in[3] | 28.7             | rise       |
| proc_net_fifo/proc_net_do[7]   | 26.1             | rise       |
| proc_net_fifo/proc_net_do[7]'  | 24.2             | rise       |
| proc_net_fifo/PHASE_C          | 2.2              | rise       |

-----

| INSERT | MESSAGES | GRAPHICS | FORM | OVERLAY | RECORD | UTILITY |
|--------|----------|----------|------|---------|--------|---------|
|--------|----------|----------|------|---------|--------|---------|

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|             |             |           |                      |
|-------------|-------------|-----------|----------------------|
| <u>BACK</u> | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |
|             | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |

-----

>TIMING>CLOCKS>

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\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 16:21:23 1988 .

\*\*\*\*\*  
Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|                                |      |      |
|--------------------------------|------|------|
| <oder/parity_gen/xor16_0/m[0]  | 36.3 | fall |
| <oder/parity_gen/xor16_0/m[0]' | 36.3 | fall |
| <oder/parity_gen/xor16_0/k[0]  | 33.8 | rise |
| <oder/parity_gen/xor16_0/k[0]' | 33.7 | rise |
| <oder/parity_gen/xor16_0/j[1]  | 31.2 | fall |
| <oder/parity_gen/xor16_0/j[1]' | 31.1 | fall |
| <oder/parity_gen/xor16_0/in[3] | 28.7 | rise |
| proc_net_fifo/proc_net_do[7]   | 26.1 | rise |
| proc_net_fifo/proc_net_do[7]'  | 24.2 | rise |
| proc_net_fifo/PHASE_C          | 2.2  | rise |
| Net_clk/PHASE_C                | 1.2  | rise |
| Net_clk                        | 0.0  | rise |

Minimum cycle time (from Ph2) is 32.8 ns set by:

\*\* Clock delay: 4.4ns (20.8-16.4) cycle sharing disabled

| Node                            | Cumulative Delay | Transition |
|---------------------------------|------------------|------------|
| <oder/data_register/(internal)  | 38.9             | rise       |
| <r_encoder/data_register/cb[5]  | 38.3             | fall       |
| <n_coder/parity_gen/xor16_5/out | 38.3             | fall       |
| <oder/parity_gen/xor16_5/out'   | 38.2             | fall       |
| <oder/parity_gen/xor16_5/m[0]   | 36.6             | rise       |
| <oder/parity_gen/xor16_5/m[0]'  | 36.5             | rise       |
| <oder/parity_gen/xor16_5/k[1]   | 33.8             | fall       |
| <oder/parity_gen/xor16_5/k[1]'  | 33.8             | fall       |
| <oder/parity_gen/xor16_5/j[3]   | 31.4             | rise       |
| <oder/parity_gen/xor16_5/j[3]'  | 31.3             | rise       |
| <oder/parity_gen/xor16_5/in[7]  | 28.8             | fall       |
| proc_net_fifo/proc_net_do[15]   | 26.5             | fall       |
| proc_net_fifo/proc_net_do[15]'  | 24.7             | fall       |
| *proc_net_fifo/(internal)       | 19.9             | fall       |
| proc_net_fifo/PHASE_C           | 2.0              | fall       |
| Net_clk/PHASE_C                 | 0.9              | fall       |
| Net_clk                         | 0.0              | fall       |

-----  
INSERT    MESSAGES    GRAPHICS    FORM    OVERLAY    RECORD    UTILITY

|             |             |           |                      |
|-------------|-------------|-----------|----------------------|
| <u>BACK</u> | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |
|             | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |

-----  
>TIMING>CLOCKS>

Jun 10 08:57 1988 timing\_at\_92C\_4.5V Page 8

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 16:21:47 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## OUTPUT DELAY MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Net\_clk

Included setup files:

#0 max\_phase\_c

(max. temp. min v. for Net\_clk)

-----  
OUTPUT DELAYS (ns)

| Output    | Ph1(r) Delay | Ph2(r) Delay | Loading(pf) |      |
|-----------|--------------|--------------|-------------|------|
|           | Min Max      | Min Max      |             |      |
| Data[0]   | 0.0 26.8     | 0.0 26.8     | 50.00       | PATH |
| Data[1]   | 0.0 26.8     | 0.0 26.8     | 50.00       | PATH |
| Data[2]   | 0.0 26.8     | 0.0 26.8     | 50.00       | PATH |
| Data[3]   | 0.0 26.8     | 0.0 26.8     | 50.00       | PATH |
| Data[4]   | 0.0 26.8     | 0.0 26.8     | 50.00       | PATH |
| Data[5]   | 0.0 26.6     | 0.0 26.6     | 50.00       | PATH |
| Data[6]   | 0.0 26.9     | 0.0 26.9     | 50.00       | PATH |
| Data[7]   | 0.0 27.4     | 0.0 27.4     | 50.00       | PATH |
| av        | 16.3 17.7    | ---          | 50.00       | PATH |
| Host_dav  | ---          | ---          | 50.00       | PATH |
| Host_rfi  | ---          | ---          | 50.00       | PATH |
| _xack     | 16.7 20.2    | 16.7 20.2    | 50.00       | PATH |
| et_dav    | ---          | ---          | 50.00       | PATH |
| Net_error | ---          | ---          | 50.00       | PATH |
| Net_rfi   | ---          | ---          | 50.00       | PATH |
| roc_run   | ---          | ---          | 50.00       | PATH |
| R[0]      | 0.0 23.9     | 0.0 23.9     | 50.00       | PATH |
| R[10]     | 0.0 26.3     | 0.0 26.3     | 50.00       | PATH |
| [11]      | 0.0 24.7     | 0.0 24.7     | 50.00       | PATH |
| [12]      | 0.0 24.2     | 0.0 24.2     | 50.00       | PATH |
| R[13]     | 0.0 24.1     | 0.0 24.1     | 50.00       | PATH |
| R[14]     | 0.0 23.9     | 0.0 23.9     | 50.00       | PATH |
| [15]      | 0.0 23.7     | 0.0 23.7     | 50.00       | PATH |
| R[16]     | 0.0 23.5     | 0.0 23.5     | 50.00       | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK

&gt;TIMING&gt;OUTPUT DELAY&gt;

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\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 16:21:56 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0 Beta-----

| Proc_run   | ---  | ---  | --- | ---  | 50.00 | PATH |
|------------|------|------|-----|------|-------|------|
| R[0]       | 0.0  | 23.9 | 0.0 | 23.9 | 50.00 | PATH |
| R[10]      | 0.0  | 26.3 | 0.0 | 26.3 | 50.00 | PATH |
| R[11]      | 0.0  | 24.7 | 0.0 | 24.7 | 50.00 | PATH |
| R[12]      | 0.0  | 24.2 | 0.0 | 24.2 | 50.00 | PATH |
| R[13]      | 0.0  | 24.1 | 0.0 | 24.1 | 50.00 | PATH |
| R[14]      | 0.0  | 23.9 | 0.0 | 23.9 | 50.00 | PATH |
| R[15]      | 0.0  | 23.7 | 0.0 | 23.7 | 50.00 | PATH |
| R[16]      | 0.0  | 23.5 | 0.0 | 23.5 | 50.00 | PATH |
| R[17]      | 0.0  | 23.4 | 0.0 | 23.4 | 50.00 | PATH |
| R[18]      | 0.0  | 23.2 | 0.0 | 23.2 | 50.00 | PATH |
| R[19]      | 0.0  | 23.1 | 0.0 | 23.1 | 50.00 | PATH |
| R[1]       | 0.0  | 24.2 | 0.0 | 24.2 | 50.00 | PATH |
| R[20]      | 0.0  | 23.2 | 0.0 | 23.2 | 50.00 | PATH |
| R[21]      | 0.0  | 23.4 | 0.0 | 23.4 | 50.00 | PATH |
| R[22]      | 0.0  | 23.6 | 0.0 | 23.6 | 50.00 | PATH |
| R[23]      | 0.0  | 23.5 | 0.0 | 23.5 | 50.00 | PATH |
| R[24]      | 0.0  | 23.7 | 0.0 | 23.7 | 50.00 | PATH |
| R[25]      | 0.0  | 23.8 | 0.0 | 23.8 | 50.00 | PATH |
| R[26]      | 0.0  | 24.0 | 0.0 | 24.0 | 50.00 | PATH |
| R[27]      | 0.0  | 24.2 | 0.0 | 24.2 | 50.00 | PATH |
| R[28]      | 0.0  | 24.3 | 0.0 | 24.3 | 50.00 | PATH |
| R[29]      | 0.0  | 26.3 | 0.0 | 26.3 | 50.00 | PATH |
| R[2]       | 0.0  | 24.4 | 0.0 | 24.4 | 50.00 | PATH |
| R[30]      | 0.0  | 25.6 | 0.0 | 25.6 | 50.00 | PATH |
| R[31]      | 0.0  | 25.3 | 0.0 | 25.3 | 50.00 | PATH |
| R[3]       | 0.0  | 24.9 | 0.0 | 24.9 | 50.00 | PATH |
| R[4]       | 0.0  | 25.1 | 0.0 | 25.1 | 50.00 | PATH |
| R[5]       | 0.0  | 25.3 | 0.0 | 25.3 | 50.00 | PATH |
| R[6]       | 0.0  | 25.4 | 0.0 | 25.4 | 50.00 | PATH |
| R[7]       | 0.0  | 25.6 | 0.0 | 25.6 | 50.00 | PATH |
| R[8]       | 0.0  | 25.8 | 0.0 | 25.8 | 50.00 | PATH |
| R[9]       | 0.0  | 26.1 | 0.0 | 26.1 | 50.00 | PATH |
| Rfi        | 14.5 | 15.7 | --- | ---  | 50.00 | PATH |
| Serial_out | 13.1 | 14.4 | --- | ---  | 50.00 | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY  
-----BACK-----  
>TIMING>OUTPUT DELAY>

Jun 10 08:57 1988 timing\_at\_92C\_4.5V Page 10

\*\*\*\*\*  
Genesil Screen Dump -- Thu Jun 9 16:22:27 1988

\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

VIOLATION MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Net\_clk

Included setup files:

#0 max\_phase\_c

(max. temp. min v. for Net\_clk)

-----  
NO VIOLATIONS

Hold time check margin: 0.0ns

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

BACK

-----  
>TIMING>VIOLATIONS>

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\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:57:09 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## SETUP AND HOLD MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Proc\_clk

Included setup files:

#0 max\_phase\_a

(max. temp. min v. for Proc\_clk)

-----  
INPUT SETUP AND HOLD TIMES (ns)

| Input      | Setup Time |        | Hold Time |        |      |
|------------|------------|--------|-----------|--------|------|
|            | Ph1(f)     | Ph2(f) | Ph1(f)    | Ph2(f) |      |
| Address[0] | ---        | 9.9    | ---       | -6.2   | PATH |
| Address[1] | ---        | 10.1   | ---       | -6.4   | PATH |
| Address[2] | ---        | 10.0   | ---       | -6.2   | PATH |
| Data[0]    | ---        | 6.8    | ---       | -2.9   | PATH |
| Data[1]    | ---        | 6.9    | ---       | -3.0   | PATH |
| Data[2]    | ---        | 6.8    | ---       | -2.9   | PATH |
| Data[3]    | ---        | 6.7    | ---       | -2.9   | PATH |
| Data[4]    | ---        | 8.1    | ---       | -4.3   | PATH |
| Data[5]    | ---        | 8.1    | ---       | -4.3   | PATH |
| Data[6]    | ---        | 7.9    | ---       | -4.2   | PATH |
| Data[7]    | ---        | 7.7    | ---       | -4.0   | PATH |
| F[0]       | ---        | 0.6    | ---       | 1.0    | PATH |
| F[10]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[11]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[12]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[13]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[14]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[15]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[16]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[17]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[18]      | ---        | 0.5    | ---       | 1.1    | PATH |
| F[19]      | ---        | 0.4    | ---       | 1.1    | PATH |
| F[1]       | ---        | 0.6    | ---       | 1.0    | PATH |
| F[20]      | ---        | 0.4    | ---       | 1.1    | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK-----  
>TIMING>SETUP HOLD>

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\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:57:22 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|               |     |      |     |      |      |
|---------------|-----|------|-----|------|------|
| F[20]         | --- | 0.4  | --- | 1.1  | PATH |
| F[21]         | --- | 0.4  | --- | 1.1  | PATH |
| F[22]         | --- | 0.4  | --- | 1.2  | PATH |
| F[23]         | --- | 0.4  | --- | 1.2  | PATH |
| F[24]         | --- | 0.4  | --- | 1.2  | PATH |
| F[25]         | --- | 0.4  | --- | 1.2  | PATH |
| F[26]         | --- | 0.4  | --- | 1.2  | PATH |
| F[27]         | --- | 0.4  | --- | 1.2  | PATH |
| F[28]         | --- | 0.4  | --- | 1.2  | PATH |
| F[29]         | --- | 0.4  | --- | 1.2  | PATH |
| F[2]          | --- | 0.6  | --- | 1.0  | PATH |
| F[30]         | --- | 0.4  | --- | 1.2  | PATH |
| F[31]         | --- | 0.4  | --- | 1.2  | PATH |
| F[3]          | --- | 0.5  | --- | 1.0  | PATH |
| F[4]          | --- | 0.5  | --- | 1.0  | PATH |
| F[5]          | --- | 0.5  | --- | 1.1  | PATH |
| F[6]          | --- | 0.5  | --- | 1.1  | PATH |
| F[7]          | --- | 0.5  | --- | 1.1  | PATH |
| F[8]          | --- | 0.5  | --- | 1.1  | PATH |
| F[9]          | --- | 0.5  | --- | 1.1  | PATH |
| IO_opcode[0]  | --- | 26.8 | --- | -8.2 | PATH |
| IO_opcode[1]  | --- | 25.4 | --- | -8.4 | PATH |
| IO_opcode[2]  | --- | 27.0 | --- | -9.4 | PATH |
| N_chip_select | --- | 9.3  | --- | -5.5 | PATH |
| N_mem_read    | --- | 6.3  | --- | -2.6 | PATH |
| N_mem_write   | --- | 7.9  | --- | -4.2 | PATH |
| Net_run       | --- | 5.2  | --- | -1.4 | PATH |
| Net_sync      | --- | ---  | --- | ---  | PATH |
| R[0]          | --- | 0.5  | --- | 1.3  | PATH |
| R[10]         | --- | 0.6  | --- | 1.3  | PATH |
| R[11]         | --- | 0.6  | --- | 1.3  | PATH |
| R[12]         | --- | 0.6  | --- | 1.2  | PATH |
| R[13]         | --- | 0.6  | --- | 1.2  | PATH |
| R[14]         | --- | 0.6  | --- | 1.2  | PATH |
| R[15]         | --- | 0.6  | --- | 1.2  | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY  
-----BACK>TIMING>SETUP HOLD>

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\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:57:33 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|              |     |      |     |       |      |
|--------------|-----|------|-----|-------|------|
| R[12]        | --- | 0.6  | --- | 1.2   | PATH |
| R[13]        | --- | 0.6  | --- | 1.2   | PATH |
| R[14]        | --- | 0.6  | --- | 1.2   | PATH |
| R[15]        | --- | 0.6  | --- | 1.2   | PATH |
| R[16]        | --- | 0.6  | --- | 1.2   | PATH |
| R[17]        | --- | 0.7  | --- | 1.2   | PATH |
| R[18]        | --- | 0.7  | --- | 1.2   | PATH |
| R[19]        | --- | 0.7  | --- | 1.2   | PATH |
| R[1]         | --- | 0.5  | --- | 1.3   | PATH |
| R[20]        | --- | 0.8  | --- | 1.1   | PATH |
| R[21]        | --- | 0.8  | --- | 1.0   | PATH |
| R[22]        | --- | 0.8  | --- | 1.0   | PATH |
| R[23]        | --- | 0.9  | --- | 1.0   | PATH |
| R[24]        | --- | 0.9  | --- | 1.0   | PATH |
| R[25]        | --- | 0.9  | --- | 0.9   | PATH |
| R[26]        | --- | 0.9  | --- | 0.9   | PATH |
| R[27]        | --- | 0.9  | --- | 0.9   | PATH |
| R[28]        | --- | 0.9  | --- | 0.9   | PATH |
| R[29]        | --- | 1.0  | --- | 0.9   | PATH |
| R[2]         | --- | 0.5  | --- | 1.3   | PATH |
| R[30]        | --- | 1.0  | --- | 0.8   | PATH |
| R[31]        | --- | 1.0  | --- | 0.8   | PATH |
| R[3]         | --- | 0.5  | --- | 1.3   | PATH |
| R[4]         | --- | 0.5  | --- | 1.3   | PATH |
| R[5]         | --- | 0.5  | --- | 1.3   | PATH |
| R[6]         | --- | 0.6  | --- | 1.3   | PATH |
| R[7]         | --- | 0.6  | --- | 1.3   | PATH |
| R[8]         | --- | 0.6  | --- | 1.3   | PATH |
| R[9]         | --- | 0.6  | --- | 1.3   | PATH |
| R_bus_en[0]  | --- | 18.7 | --- | -15.0 | PATH |
| R_bus_en[1]  | --- | 19.4 | --- | -15.8 | PATH |
| R_eq_f_2     | --- | 0.6  | --- | 0.9   | PATH |
| Serial_in    | --- | ---  | --- | ---   | PATH |
| Transfer_in  | --- | ---  | --- | ---   | PATH |
| Transfer_out | --- | ---  | --- | ---   | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY  
-----BACK

&gt;TIMING&gt;SETUP HOLD&gt;

Jun 10 08:57 1988 timing\_at\_92C\_4.5V Page 14

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:58:04 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## CLOCK REPORT MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Proc\_clk

Included setup files:

#0 max\_phase\_a (max. temp. min v. for Proc\_clk)

## CLOCK TIMES (minimum)

Phase 1 High: 23.1 ns

Phase 2 High: 27.0 ns

Cycle (from Ph1): 46.4 ns

Cycle (from Ph2): 78.2 ns

Minimum Cycle Time: 78.2 ns

Symmetric Cycle Time: 78.2 ns

## CLOCK WORST CASE PATHS

Minimum Phase 1 high time is 23.1 ns set by:

\*\* Clock delay: 1.9ns (25.0-23.1)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| host_data_latch/(internal)     | 25.0             | rise       |
| host_data_latch/wr[1]          | 23.2             | fall       |
| host_data_latch/wr[1]'         | 23.0             | fall       |
| host_data_latch/dec_en         | 21.7             | fall       |
| host_data_latch/host_proc_mwtc | 19.8             | fall       |
| <oc_sync/stage2/host_proc_mwtc | 18.3             | fall       |
| <c_sync/stage2/host_proc_mwtc' | 7.7              | fall       |
| <st_proc_sync/stage2/n_cs_sync | 6.7              | rise       |
| host_proc_sync/stage2/cs_sync  | 5.8              | fall       |
| host_proc_sync/stage1/cs_sync  | 5.8              | fall       |
| host_proc_sync/stage1/cs_sync' | 5.4              | fall       |
| host_proc_sync/stage1/PHASE_A  | 2.3              | rise       |
| Proc_clk/PHASE_A               | 1.2              | rise       |
| Proc_clk                       | 0.0              | rise       |

| INSERT | MESSAGES | GRAPHICS | FORM | OVERLAY | RECORD | UTILITY |
|--------|----------|----------|------|---------|--------|---------|
|--------|----------|----------|------|---------|--------|---------|

BACK

PHASE1\_HIGH

CYCLE\_PH1

DUMP\_LATCH\_THRESHOLD

PHASE2\_HIGH

CYCLE\_PH2

DUMP\_LATCH

&gt;TIMING&gt;CLOCKS&gt;

\*\*\*\*\*  
 Genesil Screen Dump -- Fri Jun 10 06:58:13 1988  
 \*\*\*\*\*

\*\*\*\*\*  
 Chip: ~sni/sni/xserial  
 \*\*\*\*\*

\*\*\*\*\*  
 Timing Analyzer  
 \*\*\*\*\*

-----Genesil Version v7.0\_Beta-----

Proc\_clk 0.0 rise

Minimum Phase 2 high time is 27.0 ns set by:

-----  
 \*\* Clock delay: 4.1ns (31.1-27.0)

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| Rd[5]/(internal)               | 31.1             | rise       |
| R[29]                          | 26.3             | fall       |
| Rd[5]/r                        | 19.4             | fall       |
| proc_out_mux/r[29]             | 18.2             | fall       |
| proc_out_mux/r[29]'            | 13.6             | fall       |
| proc_out_mux/net_read          | 10.7             | rise       |
| opcode_decoder/net_read        | 10.4             | rise       |
| opcode_decoder/net_read'       | 9.6              | rise       |
| opcode_decoder/n_io_opcode[2]  | 8.4              | rise       |
| opcode_decoder/n_io_opcode[2]' | 8.3              | rise       |
| opcode_decoder/io_opcode[2]    | 6.9              | fall       |
| IO_opcode[2]/io_opcode         | 5.1              | fall       |
| IO_opcode[2]/io_opcode'        | 3.8              | fall       |
| IO_opcode[2]                   | 0.0              | fall       |

Minimum cycle time (from Ph1) is 46.4 ns set by:

-----  
 \*\* Clock delay: 2.2ns (48.7-46.4)

| Node                      | Cumulative Delay | Transition |
|---------------------------|------------------|------------|
| proc_host_fifo/(internal) | 48.7             | fall       |
| proc_host_fifo/r[29]      | 48.3             | rise       |
| proc_in_mux/proc_din[29]  | 47.6             | rise       |
| proc_in_mux/proc_din[29]' | 43.9             | rise       |
| proc_in_mux/r_in[29]      | 42.4             | rise       |
| Rd[5]/r_in                | 41.9             | rise       |
| Rd[5]/r_in'               | 41.7             | rise       |
| *Rd[5]/(internal)         | 40.1             | fall       |
| R[29]                     | 37.1             | rise       |
| Rd[5]/r                   | 30.8             | rise       |

-----  
 INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY  
 -----

|             |             |           |                      |
|-------------|-------------|-----------|----------------------|
| <u>BACK</u> | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |
|             | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |

-----  
 >TIMING>CLOCKS>  
 -----

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:58:22 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

|                                |      |      |
|--------------------------------|------|------|
| Rd[5]/r                        | 30.8 | rise |
| proc_out_mux/r[29]             | 29.8 | rise |
| proc_out_mux/r[29]'            | 26.0 | rise |
| proc_out_mux/net_proc_do[29]   | 24.5 | rise |
| net_proc_fifo/net_proc_do[29]  | 24.3 | rise |
| net_proc_fifo/net_proc_do[29]' | 24.2 | rise |
| net_proc_fifo/PHASE_A          | 2.3  | rise |
| Proc_clk/PHASE_A               | 1.2  | rise |
| Proc_clk                       | 0.0  | rise |

Minimum cycle time (from Ph2) is 78.2 ns set by:

\*\* Clock delay: 2.2ns (41.3-39.1) cycle sharing disabled

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| Data[2]                        | 65.9             | fall       |
| Data[2]/host dout              | 59.5             | fall       |
| <ceiver/8to1_mux/host dout[2]  | 59.2             | fall       |
| <ceiver/8to1_mux/host dout[2]' | 56.7             | fall       |
| <ver/8to1_mux/proc host do[10] | 52.0             | fall       |
| <ceiver/latch/ph do latch[10]  | 51.9             | fall       |
| <ceiver/latch/ph do latch[10]' | 51.8             | fall       |
| <ceiver/latch/proc host do[10] | 47.9             | fall       |
| <oc host fifo/proc host do[10] | 47.6             | fall       |
| <c host fifo/proc host do[10]' | 46.6             | fall       |
| *proc host fifo/(Internal)     | 39.9             | rise       |
| proc host fifo/r[10]           | 39.4             | fall       |
| proc_in_mux/proc din[10]       | 39.1             | fall       |
| proc_in_mux/proc din[10]'      | 35.5             | fall       |
| proc_in_mux/r_in[10]           | 33.7             | fall       |
| Rb[2]/r_in                     | 32.4             | fall       |
| Rb[2]/r_in'                    | 31.4             | fall       |
| R[10]                          | 26.3             | fall       |
| Rb[2]/r                        | 19.4             | fall       |
| proc_out_mux/r[10]             | 18.2             | fall       |
| proc_out_mux/r[10]'            | 13.6             | fall       |

-----  
INSERT    MESSAGES    GRAPHICS    FORM    OVERLAY    RECORD    UTILITY

|      |             |           |                      |
|------|-------------|-----------|----------------------|
| BACK | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |
|      | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |

-----  
>TIMING>CLOCKS>

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\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:58:28 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0 Beta-----

Minimum cycle time (from Ph2) is 78.2 ns set by:

\*\* Clock delay: 2.2ns (41.3-39.1) cycle sharing disabled

| Node                           | Cumulative Delay | Transition |
|--------------------------------|------------------|------------|
| Data[2]                        | 65.9             | fall       |
| Data[2]/host dout              | 59.5             | fall       |
| <ceiver/8to1_mux/host_dout[2]  | 59.2             | fall       |
| <ceiver/8to1_mux/host_dout[2]' | 56.7             | fall       |
| <ver/8to1_mux/proc_host_do[10] | 52.0             | fall       |
| <ceiver/latch/ph_do_latch[10]  | 51.9             | fall       |
| <ceiver/latch/ph_do_latch[10]' | 51.8             | fall       |
| <ceiver/latch/proc_host_do[10] | 47.9             | fall       |
| <oc_host_fifo/proc_host_do[10] | 47.6             | fall       |
| <c_host_fifo/proc_host_do[10]' | 46.6             | fall       |
| *proc_host_fifo/(internal)     | 39.9             | rise       |
| proc_host_fifo/r[10]           | 39.4             | fall       |
| proc_in_mux/proc_din[10]       | 39.1             | fall       |
| proc_in_mux/proc_din[10]'      | 35.5             | fall       |
| proc_in_mux/r_in[10]           | 33.7             | fall       |
| Rb[2]/r_in                     | 32.4             | fall       |
| Rb[2]/r_in'                    | 31.4             | fall       |
| R[10]                          | 26.3             | fall       |
| Rb[2]/r                        | 19.4             | fall       |
| proc_out_mux/r[10]             | 18.2             | fall       |
| proc_out_mux/r[10]'            | 13.6             | fall       |
| proc_out_mux/net_read          | 10.7             | rise       |
| opcode_decoder/net_read        | 10.4             | rise       |
| opcode_decoder/net_read'       | 9.6              | rise       |
| opcode_decoder/n_io_opcode[2]  | 8.4              | rise       |
| opcode_decoder/n_io_opcode[2]' | 8.3              | rise       |
| opcode_decoder/io_opcode[2]    | 6.9              | fall       |
| IO_opcode[2]/io_opcode         | 5.1              | fall       |
| IO_opcode[2]/io_opcode'        | 3.8              | fall       |
| IO_opcode[2]                   | 0.0              | fall       |

-----  
INSERT    MESSAGES    GRAPHICS    FORM    OVERLAY    RECORD    UTILITY

|      |             |           |                      |
|------|-------------|-----------|----------------------|
| BACK | PHASE1_HIGH | CYCLE_PH1 | DUMP_LATCH_THRESHOLD |
|      | PHASE2_HIGH | CYCLE_PH2 | DUMP_LATCH           |

-----  
>TIMING>CLOCKS>

Jun 10 08:57 1988 timing\_at\_92C\_4.5V Page 18

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 06:58:55 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## OUTPUT DELAY MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Proc\_clk

Included setup files:

#0 max\_phase\_a

(max. temp. min v. for Proc\_clk)

-----  
OUTPUT DELAYS (ns)

| Output    | Ph1(r) Delay | Ph2(r) Delay | Loading(pf) |      |
|-----------|--------------|--------------|-------------|------|
|           | Min Max      | Min Max      |             |      |
| Data[0]   | 0.0 28.6     | 0.0 26.8     | 50.00       | PATH |
| Data[1]   | 0.0 28.6     | 0.0 26.8     | 50.00       | PATH |
| Data[2]   | 0.0 28.6     | 0.0 26.8     | 50.00       | PATH |
| Data[3]   | 0.0 28.7     | 0.0 26.8     | 50.00       | PATH |
| Data[4]   | 0.0 28.7     | 0.0 26.8     | 50.00       | PATH |
| Data[5]   | 0.0 28.5     | 0.0 26.6     | 50.00       | PATH |
| Data[6]   | 0.0 28.9     | 0.0 26.9     | 50.00       | PATH |
| Data[7]   | 0.0 29.1     | 0.0 27.4     | 50.00       | PATH |
| dav       | ---          | ---          | 50.00       | PATH |
| Host_dav  | 13.9 15.1    | ---          | 50.00       | PATH |
| Host_rfi  | 17.7 20.7    | ---          | 50.00       | PATH |
| _xack     | 14.2 20.2    | 16.7 20.2    | 50.00       | PATH |
| et_dav    | 14.0 15.2    | ---          | 50.00       | PATH |
| Net_error | 15.0 31.2    | ---          | 50.00       | PATH |
| Net_rfi   | 16.3 31.1    | ---          | 50.00       | PATH |
| roc_run   | 13.0 15.7    | ---          | 50.00       | PATH |
| R[0]      | 0.0 33.8     | 0.0 23.9     | 50.00       | PATH |
| R[10]     | 0.0 36.9     | 0.0 26.3     | 50.00       | PATH |
| [11]      | 0.0 35.5     | 0.0 24.7     | 50.00       | PATH |
| [12]      | 0.0 35.1     | 0.0 24.2     | 50.00       | PATH |
| R[13]     | 0.0 35.0     | 0.0 24.1     | 50.00       | PATH |
| R[14]     | 0.0 34.9     | 0.0 23.9     | 50.00       | PATH |
| [15]      | 0.0 34.7     | 0.0 23.7     | 50.00       | PATH |
| R[16]     | 0.0 33.6     | 0.0 23.5     | 50.00       | PATH |

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK-----  
>TIMING>OUTPUT DELAY>

\*\*\*\*\*  
 Genesil Screen Dump -- Fri Jun 10 06:59:07 1988  
 \*\*\*\*\*

\*\*\*\*\*  
 Chip: ~sni/sni/xserial  
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\*\*\*\*\*  
 Timing Analyzer  
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-----Genesil Version v7.0 Beta-----

|            |      |      |     |      |       |      |
|------------|------|------|-----|------|-------|------|
| Proc_run   | 13.0 | 15.7 | --- | ---  | 50.00 | PATH |
| R[0]       | 0.0  | 33.8 | 0.0 | 23.9 | 50.00 | PATH |
| R[10]      | 0.0  | 36.9 | 0.0 | 26.3 | 50.00 | PATH |
| R[11]      | 0.0  | 35.5 | 0.0 | 24.7 | 50.00 | PATH |
| R[12]      | 0.0  | 35.1 | 0.0 | 24.2 | 50.00 | PATH |
| R[13]      | 0.0  | 35.0 | 0.0 | 24.1 | 50.00 | PATH |
| R[14]      | 0.0  | 34.9 | 0.0 | 23.9 | 50.00 | PATH |
| R[15]      | 0.0  | 34.7 | 0.0 | 23.7 | 50.00 | PATH |
| R[16]      | 0.0  | 33.6 | 0.0 | 23.5 | 50.00 | PATH |
| R[17]      | 0.0  | 33.4 | 0.0 | 23.4 | 50.00 | PATH |
| R[18]      | 0.0  | 33.3 | 0.0 | 23.2 | 50.00 | PATH |
| R[19]      | 0.0  | 33.2 | 0.0 | 23.1 | 50.00 | PATH |
| R[1]       | 0.0  | 34.0 | 0.0 | 24.2 | 50.00 | PATH |
| R[20]      | 0.0  | 33.3 | 0.0 | 23.2 | 50.00 | PATH |
| R[21]      | 0.0  | 33.5 | 0.0 | 23.4 | 50.00 | PATH |
| R[22]      | 0.0  | 33.6 | 0.0 | 23.6 | 50.00 | PATH |
| R[23]      | 0.0  | 33.6 | 0.0 | 23.5 | 50.00 | PATH |
| R[24]      | 0.0  | 33.8 | 0.0 | 23.7 | 50.00 | PATH |
| R[25]      | 0.0  | 33.9 | 0.0 | 23.8 | 50.00 | PATH |
| R[26]      | 0.0  | 34.0 | 0.0 | 24.0 | 50.00 | PATH |
| R[27]      | 0.0  | 35.2 | 0.0 | 24.2 | 50.00 | PATH |
| R[28]      | 0.0  | 35.3 | 0.0 | 24.3 | 50.00 | PATH |
| R[29]      | 0.0  | 37.1 | 0.0 | 26.3 | 50.00 | PATH |
| R[2]       | 0.0  | 34.2 | 0.0 | 24.4 | 50.00 | PATH |
| R[30]      | 0.0  | 36.5 | 0.0 | 25.6 | 50.00 | PATH |
| R[31]      | 0.0  | 36.2 | 0.0 | 25.3 | 50.00 | PATH |
| R[3]       | 0.0  | 34.6 | 0.0 | 24.9 | 50.00 | PATH |
| R[4]       | 0.0  | 34.8 | 0.0 | 25.1 | 50.00 | PATH |
| R[5]       | 0.0  | 36.0 | 0.0 | 25.3 | 50.00 | PATH |
| R[6]       | 0.0  | 36.1 | 0.0 | 25.4 | 50.00 | PATH |
| R[7]       | 0.0  | 36.3 | 0.0 | 25.6 | 50.00 | PATH |
| R[8]       | 0.0  | 36.5 | 0.0 | 25.8 | 50.00 | PATH |
| R[9]       | 0.0  | 36.7 | 0.0 | 26.1 | 50.00 | PATH |
| fi         | ---  | ---  | --- | ---  | 50.00 | PATH |
| Serial_out | ---  | ---  | --- | ---  | 50.00 | PATH |

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|        |          |          |             |         |        |         |
|--------|----------|----------|-------------|---------|--------|---------|
| INSERT | MESSAGES | GRAPHICS | <u>FORM</u> | OVERLAY | RECORD | UTILITY |
|--------|----------|----------|-------------|---------|--------|---------|

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BACK

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>TIMING>OUTPUT DELAY>

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\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 07:01:08 1988

\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

VIOLATION MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Proc\_clk

Included setup files:

#0 max\_phase\_a

(max. temp. min v. for Proc\_clk)

-----  
NO VIOLATIONS

Hold time check margin: 0.0ns

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK

-----  
>TIMING>VIOLATIONS>

Jun 10 08:57 1988 timing\_at\_92C\_4.5V Page 21

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 08:03:31 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

## PATH DELAY MODE

## BLOCK NAME

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 92 deg C

Voltage: 4.50v

External Clock: Proc\_clk

Included setup files:

#0 max\_phase\_a

(max. temp. min v. for Proc\_clk)

|               |           | PATH DELAY (ns) |      |     |          |
|---------------|-----------|-----------------|------|-----|----------|
| Source Object | Connector | (Ph1) Min       | Max  |     |          |
| Dest. Object  | Connector | (Ph2) Min       | Max  |     |          |
| R bus en[0]   | R bus en  | 16.4            | 17.8 |     |          |
| Rd[7]         | R         | 16.4            | 17.8 | PAT | Data[0]  |
| R bus en[0]   | R bus en  | 15.7            | 17.1 |     | Data[1]  |
| Rc[7]         | R         | 15.7            | 17.1 | PAT | Data[2]  |
| R bus en[0]   | R bus en  | 16.0            | 17.4 |     | Data[3]  |
| Rb[7]         | R         | 16.0            | 17.4 | PAT | Data[4]  |
| R bus en[0]   | R bus en  | 16.9            | 18.3 |     | Data[5]  |
| Ra[7]         | R         | 16.9            | 18.3 | PAT | Data[6]  |
| R bus en[0]   | R bus en  | 17.2            | 18.5 |     | Data[7]  |
| Ra[0]         | R         | 17.2            | 18.5 | PAT | Dav      |
| R bus en[1]   | R bus en  | 17.1            | 18.5 |     | F[0]     |
| Rd[7]         | R         | 17.1            | 18.5 | PAT | F[10]    |
| R bus en[1]   | R bus en  | 16.4            | 17.8 |     | F[11]    |
| Rc[7]         | R         | 16.4            | 17.8 | PAT | F[12]    |
| R bus en[1]   | R bus en  | 16.7            | 18.1 |     | F[13]    |
| Rb[7]         | R         | 16.7            | 18.1 | PAT | F[14]    |
| R bus en[1]   | R bus en  | 17.6            | 19.0 |     | F[15]    |
| Ra[7]         | R         | 17.6            | 19.0 | PAT | F[16]    |
| R bus en[1]   | R bus en  | 17.9            | 19.2 |     | F[17]    |
| Ra[0]         | R         | 17.9            | 19.2 | PAT | F[18]    |
| IO opcode[0]  | IO opcode | 22.9            | 25.1 |     | F[19]    |
| Rd[7]         | R         | 22.9            | 25.1 | PAT | F[1]     |
| IO opcode[0]  | IO opcode | 21.3            | 23.3 |     | F[20]    |
| Rc[7]         | R         | 21.3            | 23.3 | PAT | F[21]    |
|               |           |                 |      |     | F[22]    |
|               |           |                 |      |     | F[23]    |
|               |           |                 |      |     | F[24]    |
|               |           |                 |      |     | F[25]    |
|               |           |                 |      |     | F[26]    |
|               |           |                 |      |     | F[27]    |
|               |           |                 |      |     | * MORE * |

INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

BACK

PATH\_DELETE\_TOGGLE

Enter [string]:

&gt;TIMING&gt;PATH DELAY&gt;

Jun 10 08:57 1988 timing\_at\_92C\_4.5V Page 22

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 08:03:42 1988  
\*\*\*\*\*

Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0 Beta-----+-----

|              | Rc[7]     | R | 21.3 | 23.3 | PATH | BLOCK      | NAME      |
|--------------|-----------|---|------|------|------|------------|-----------|
| IO opcode[0] | IO opcode |   | 21.5 | 23.5 |      |            | *CURRENT* |
| Rb[7]        | R         |   | 21.5 | 23.5 | PATH | Address[0] |           |
| IO opcode[0] | IO opcode |   | 23.1 | 25.4 |      | Address[1] |           |
| Ra[7]        | R         |   | 23.1 | 25.4 | PATH | Address[2] |           |
| IO opcode[0] | IO opcode |   | 21.7 | 23.7 |      | Data[0]    |           |
| Ra[0]        | R         |   | 21.7 | 23.7 | PATH | Data[1]    |           |
| IO opcode[1] | IO opcode |   | 22.0 | 23.7 |      | Data[2]    |           |
| Rd[7]        | R         |   | 22.0 | 23.7 | PATH | Data[3]    |           |
| IO opcode[1] | IO opcode |   | 20.5 | 21.9 |      | Data[4]    |           |
| Rc[7]        | R         |   | 20.5 | 21.9 | PATH | Data[5]    |           |
| IO opcode[1] | IO opcode |   | 20.7 | 22.1 |      | Data[6]    |           |
| Rb[7]        | R         |   | 20.7 | 22.1 | PATH | Data[7]    |           |
| IO opcode[1] | IO opcode |   | 22.3 | 24.0 |      | Dav        |           |
| Ra[7]        | R         |   | 22.3 | 24.0 | PATH | F[0]       |           |
| IO opcode[1] | IO opcode |   | 20.9 | 22.3 |      | F[10]      |           |
| Ra[0]        | R         |   | 20.9 | 22.3 | PATH | F[11]      |           |
| IO opcode[2] | IO opcode |   | 23.5 | 25.3 |      | F[12]      |           |
| Rd[7]        | R         |   | 23.5 | 25.3 | PATH | F[13]      |           |
| IO opcode[2] | IO opcode |   | 22.0 | 23.5 |      | F[14]      |           |
| Rc[7]        | R         |   | 22.0 | 23.5 | PATH | F[15]      |           |
| IO opcode[2] | IO opcode |   | 22.2 | 23.7 |      | F[16]      |           |
| Rb[7]        | R         |   | 22.2 | 23.7 | PATH | F[17]      |           |
| IO opcode[2] | IO opcode |   | 23.8 | 25.6 |      | F[18]      |           |
| Ra[7]        | R         |   | 23.8 | 25.6 | PATH | F[19]      |           |
| IO opcode[2] | IO opcode |   | 22.3 | 23.9 |      | F[1]       |           |
| Ra[0]        | R         |   | 22.3 | 23.9 | PATH | F[20]      |           |
| Address[0]   | Address   |   | 23.7 | 27.4 |      | F[21]      |           |
| Data[7]      | Data      |   | 23.7 | 27.4 | PATH | F[22]      |           |
| Address[0]   | Address   |   | 23.3 | 26.8 |      | F[23]      |           |
| Data[3]      | Data      |   | 23.3 | 26.8 | PATH | F[24]      |           |
| Address[0]   | Address   |   | 23.3 | 26.8 |      | F[25]      |           |
| Data[0]      | Data      |   | 23.3 | 26.8 | PATH | F[26]      |           |
| Address[1]   | Address   |   | 21.2 | 24.0 |      | F[27]      |           |
| Data[7]      | Data      |   | 21.2 | 24.0 | PATH | * MORE *   |           |

-----+-----  
INSERT    MESSAGES    GRAPHICS    FORM                    OVERLAY                    RECORD                    UTILITY-----  
BACK                    PATH\_DELETE\_TOGGLE

Enter [string]:  
>TIMING>PATH DELAY>

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 10 08:03:52 1988\*\*\*\*\*  
Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0 Beta-----+-----

| Data[3]       | Data          | 23.3 | 26.8 | PATH  | BLOCK NAME |
|---------------|---------------|------|------|-------|------------|
| Address[0]    | Address       | 23.3 | 26.8 |       | *CURRENT*  |
| Data[0]       | Data          | 23.3 | 26.8 | PATH  | Address[0] |
| Address[1]    | Address       | 21.2 | 24.0 |       | Address[1] |
| Data[7]       | Data          | 21.2 | 24.0 | PATH  | Address[2] |
| Address[1]    | Address       | 20.8 | 23.4 |       | Data[0]    |
| Data[3]       | Data          | 20.8 | 23.4 | PATH  | Data[1]    |
| Address[1]    | Address       | 20.8 | 23.4 |       | Data[2]    |
| Data[0]       | Data          | 20.8 | 23.4 | PATH  | Data[3]    |
| Address[2]    | Address       | 19.6 | 21.8 |       | Data[4]    |
| Data[7]       | Data          | 19.6 | 21.8 | PATH  | Data[5]    |
| Address[2]    | Address       | 19.2 | 21.3 |       | Data[6]    |
| Data[3]       | Data          | 19.2 | 21.3 | PATH  | Data[7]    |
| Address[2]    | Address       | 19.2 | 21.3 |       | Dav        |
| Data[0]       | Data          | 19.2 | 21.3 | PATHF | [0]        |
| N mem read    | N mem read    | 18.5 | 20.0 |       | F[10]      |
| Data[7]       | Data          | 18.5 | 20.0 | PATHF | [11]       |
| N mem read    | N mem read    | 18.7 | 20.2 |       | F[12]      |
| Data[3]       | Data          | 18.7 | 20.2 | PATHF | [13]       |
| N mem read    | N mem read    | 18.8 | 20.3 |       | F[14]      |
| Data[0]       | Data          | 18.8 | 20.3 | PATHF | [15]       |
| N chip select | N chip select | 20.3 | 21.8 |       | F[16]      |
| Data[7]       | Data          | 20.3 | 21.8 | PATHF | [17]       |
| N chip select | N chip select | 20.5 | 22.0 |       | F[18]      |
| Data[3]       | Data          | 20.5 | 22.0 | PATHF | [19]       |
| N chip select | N chip select | 20.6 | 22.1 |       | F[1]       |
| Data[0]       | Data          | 20.6 | 22.1 | PATHF | [20]       |
| N mem read    | N mem read    | 16.7 | 18.2 |       | F[21]      |
| N xack        | N xack        | 16.7 | 18.2 | PATHF | [22]       |
| N mem write   | N mem write   | 18.7 | 20.2 |       | F[23]      |
| N xack        | N xack        | 18.7 | 20.2 | PATHF | [24]       |
| N chip select | N chip select | 18.4 | 20.2 |       | F[25]      |
| N xack        | N xack        | 18.4 | 20.2 | PATHF | [26]       |
|               |               |      |      |       | F[27]      |

\* MORE \*

| INSERT | MESSAGES | GRAPHICS | FORM | OVERLAY | RECORD | UTILITY |
|--------|----------|----------|------|---------|--------|---------|
| BACK   |          |          |      |         |        |         |
|        |          |          |      |         |        |         |

PATH\_DELETE\_TOGGLE

Enter [string]:

&gt;TIMING&gt;PATH DELAY&gt;

\*\*\*\*\*  
 Genesil Screen Dump -- Fri Jun 10 12:24:12 1988

\*\*\*\*\*  
 Chip: ~sni/sni/xserial

\*\*\*\*\*  
 Executive

-----Genesil Version v7.0\_Beta-----

) Checking file currency . . .  
 ) \*\*\*\* ctrl-C -- ABORT ACTIVITY \*\*\*\*  
 ) UTILITY;  
 ) KEY\_PARAMETERS

) Key Parameters for Chip ~sni/sni/xserial  
 ) -----

) ROUTE VERSION = 87.20  
 ) HEIGHT = 272.2 MILS  
 ) ( = 6913.88 u )  
 ) WIDTH = 300.9 MILS  
 ) ( = 7642.85 u )  
 ) ROUTED = 1 (0=NO,1=YES)  
 ) TOTAL WIRE LENGTH = 676194 MILS  
 ) ( = 17175327. u )  
 ) CORE\_AREA = 60427.7 SQUARE\_MILS  
 ) ( = 38985535. u2 )  
 ) PADRING AREA = 21468.3 SQUARE\_MILS  
 ) ( = 13850489. u2 )  
 ) PAD\_AREA = 18413.7 SQUARE\_MILS  
 ) ( = 11879782. u2 )  
 ) ROUTE\_AREA = 32301.5 SQUARE\_MILS  
 ) ( = 20839636. u2 )  
 ) PERCENT\_ROUTING\_OF\_CORE = 53 %  
 ) PERCENT\_ROUTING\_OF\_CHIP = 39 %  
 ) PERCENT\_CORE\_OF\_CHIP = 73 %  
 ) PERCENT\_PADRING\_OF\_CHIP = 26 %  
 ) PERCENT\_PAD\_OF\_PADRING = 85 %  
 )  
 ) NETLIST\_VERSION = 1.0  
 ) NETLIST\_EXISTS = 1 (0=NO,1=YES)  
 )  
 ) PHASE\_A\_TIME = 23.1 NANOSECONDS  
 ) PHASE\_B\_TIME = 27.0 NANOSECONDS

| INSERT       | MESSAGES      | GRAPHICS                   | OVERLAY                                | RECORD                       | UTILITY |
|--------------|---------------|----------------------------|----------------------------------------|------------------------------|---------|
| EXIT_GENESIL | SELECT_OBJECT | DEFINITION<br>PACKAGE_EDIT | COMPILE<br>SIMULATION<br>TIMING<br>ATG | TOOLING<br>PLOT<br>TRANSLATE |         |

\*\*\*\*\*  
 Genesil Screen Dump -- Fri Jun 10 12:24:30 1988  
 \*\*\*\*\*

\*\*\*\*\*  
 Chip: ~sni/sni/xserial  
 \*\*\*\*\*

Executive

-----Genesil Version v7.0\_Beta-----

) PHASE\_B TIME = 27.0 NANOSECONDS  
 ) SYMMETRIC TIME = 78.2 NANOSECONDS  
 ) NUMBER\_OF\_TRANSISTORS = 60356  
 ) POWER\_DISSIPATION = 616.49 MILLIWATTS\_@5V\_10MHZ  
 )

) ROUTE\_ESTIMATE\_LVL = 0  
 ) FLAT\_ROUTE = 1 (0=NO,1=YES)  
 ) TECHNOLOGY\_NAME = CMOS-1  
 ) PACKAGE\_SPECIFIED = 0 (0=NO,1=YES)  
 ) FABLINE\_NAME = NSC\_CN12A  
 ) COMPILER\_TYPE = GCX  
 )

) FLOORPLAN\_VERSION = 7.0  
 ) BOND\_PAD\_CNT = 120  
 ) HEIGHT\_ESTIMATE = 134.63 MILS  
 ) ( = 3419.602 u )  
 ) WIDTH\_ESTIMATE = 134.15 MILS  
 ) ( = 3407.409 u )  
 ) FUSED = 1 (0=NO,1=YES)  
 ) FUSION\_REQUIRED = 1 (0=NO,1=YES)  
 ) PINOUT = 1 (0=NO,1=YES)  
 ) PINOUT\_REQUIRED = 1 (0=NO,1=YES)  
 ) PLACED = 1 (0=NO,1=YES)  
 ) PLACEMENT\_REQUIRED = 1 (0=NO,1=YES)  
 )

) AREA = 81905.0 SQUARE MILS  
 ) ( = 52841830. u2 )  
 ) OBJECT\_TYPE = Chip  
 ) AREA\_PER\_TRANSISTOR = 1.357032 SQUARE MILS  
 ) ( = 875.502744 u2 )  
 ) PHYSICAL\_IMPLEMENTATIONS\_EXIST = 0 (0=NO,1=YES)  
 ) CHECKPOINTS\_EXIST = 1 (0=NO,1=YES)  
 ) Genesil internal fault: Please file a bug report, if needed.

-----  
 INSERT MESSAGES GRAPHICS

OVERLAY

RECORD

UTILITY

EXIT GENESIL

SELECT\_OBJECT

DEFINITION  
 PACKAGE\_EDIT

COMPILE  
 SIMULATION  
 TIMING  
 ATG

TOOLING  
 PLOT  
 TRANSLATE

-----

Jun 10 12:25 1988 designinit.080 Page 1

```
func designinit {
 toggle Proc_clk 0 '(0 5 10)
 toggle Net_clk 0 '(0 5 10)
 tag Proc_clk cycle rising
 tag Proc_clk step rising
 tag Net_clk step falling
 tag Net_clk cycle none
 showtoggles

 func async_setup{
 toggle Proc_clk 0 '(3 13 23 33 43)
 toggle Net_clk 0 '(8 18 28 38 48)
 tag Proc_clk cycle rising
 tag Net_clk cycle rising
 tag Proc_clk step falling rising
 tag Net_clk step falling rising
 showtoggles
 }
}
```

Jun 10 12:37 1988 nom\_phase\_a.040 Page 1

LABEL nominal op. cond. for Proc\_clk

TEMP VOLT 47 5.00

HOLDTIME MARGIN 0.00

SELECT EXT CLOCK Proc\_clk

IGNORE\_PATH Data[0]/host\_dout Data[0]/host\_din

IGNORE\_PATH Data[1]/host\_dout Data[1]/host\_din

IGNORE\_PATH Data[2]/host\_dout Data[2]/host\_din

IGNORE\_PATH Data[3]/host\_dout Data[3]/host\_din

IGNORE\_PATH Data[4]/host\_dout Data[4]/host\_din

IGNORE\_PATH Data[5]/host\_dout Data[5]/host\_din

IGNORE\_PATH Data[6]/host\_dout Data[6]/host\_din

IGNORE\_PATH Data[7]/host\_dout Data[7]/host\_din

IGNORE\_PATH Data[0]/read\_disable Data[0]/host\_din

IGNORE\_PATH Data[1]/read\_disable Data[1]/host\_din

IGNORE\_PATH Data[2]/read\_disable Data[2]/host\_din

IGNORE\_PATH Data[3]/read\_disable Data[3]/host\_din

IGNORE\_PATH Data[4]/read\_disable Data[4]/host\_din

IGNORE\_PATH Data[5]/read\_disable Data[5]/host\_din

IGNORE\_PATH Data[6]/read\_disable Data[6]/host\_din

IGNORE\_PATH Data[7]/read\_disable Data[7]/host\_din

Jun 10 12:37 1988 nom\_phase\_c.040 Page 1

LABEL nominal op. cond. for Net\_clk

TEMP VOLT 47 5.00

HOLDTIME MARGIN 0.00

SELECT EXT CLOCK Net\_clk

IGNORE\_PATH Data[0]/host\_dout Data[0]/host\_din

IGNORE\_PATH Data[1]/host\_dout Data[1]/host\_din

IGNORE\_PATH Data[2]/host\_dout Data[2]/host\_din

IGNORE\_PATH Data[3]/host\_dout Data[3]/host\_din

IGNORE\_PATH Data[4]/host\_dout Data[4]/host\_din

IGNORE\_PATH Data[5]/host\_dout Data[5]/host\_din

IGNORE\_PATH Data[6]/host\_dout Data[6]/host\_din

IGNORE\_PATH Data[7]/host\_dout Data[7]/host\_din

IGNORE\_PATH Data[0]/read\_disable Data[0]/host\_din

IGNORE\_PATH Data[1]/read\_disable Data[1]/host\_din

IGNORE\_PATH Data[2]/read\_disable Data[2]/host\_din

IGNORE\_PATH Data[3]/read\_disable Data[3]/host\_din

IGNORE\_PATH Data[4]/read\_disable Data[4]/host\_din

IGNORE\_PATH Data[5]/read\_disable Data[5]/host\_din

IGNORE\_PATH Data[6]/read\_disable Data[6]/host\_din

IGNORE\_PATH Data[7]/read\_disable Data[7]/host\_din

LABEL max. temp. min v. for Proc\_clk

TEMP VOLT 92 4.50

HOLDTIME MARGIN 0.00

SELECT EXT CLOCK Proc\_clk

IGNORE\_PATH Data[0]/host\_dout Data[0]/host\_din

IGNORE\_PATH Data[1]/host\_dout Data[1]/host\_din

IGNORE\_PATH Data[2]/host\_dout Data[2]/host\_din

IGNORE\_PATH Data[3]/host\_dout Data[3]/host\_din

IGNORE\_PATH Data[4]/host\_dout Data[4]/host\_din

IGNORE\_PATH Data[5]/host\_dout Data[5]/host\_din

IGNORE\_PATH Data[6]/host\_dout Data[6]/host\_din

IGNORE\_PATH Data[7]/host\_dout Data[7]/host\_din

IGNORE\_PATH Data[0]/read\_disable Data[0]/host\_din

IGNORE\_PATH Data[1]/read\_disable Data[1]/host\_din

IGNORE\_PATH Data[2]/read\_disable Data[2]/host\_din

IGNORE\_PATH Data[3]/read\_disable Data[3]/host\_din

IGNORE\_PATH Data[4]/read\_disable Data[4]/host\_din

IGNORE\_PATH Data[5]/read\_disable Data[5]/host\_din

IGNORE\_PATH Data[6]/read\_disable Data[6]/host\_din

IGNORE\_PATH Data[7]/read\_disable Data[7]/host\_din

LABEL max. temp. min v. for Net\_clk

TEMP VOLT 92 4.50

HOLDTIME MARGIN 0.00

SELECT EXT CLOCK Net\_clk

IGNORE\_PATH Data[0]/host\_dout Data[0]/host\_din

IGNORE\_PATH Data[1]/host\_dout Data[1]/host\_din

IGNORE\_PATH Data[2]/host\_dout Data[2]/host\_din

IGNORE\_PATH Data[3]/host\_dout Data[3]/host\_din

IGNORE\_PATH Data[4]/host\_dout Data[4]/host\_din

IGNORE\_PATH Data[5]/host\_dout Data[5]/host\_din

IGNORE\_PATH Data[6]/host\_dout Data[6]/host\_din

IGNORE\_PATH Data[7]/host\_dout Data[7]/host\_din

IGNORE\_PATH Data[0]/read\_disable Data[0]/host\_din

IGNORE\_PATH Data[1]/read\_disable Data[1]/host\_din

IGNORE\_PATH Data[2]/read\_disable Data[2]/host\_din

IGNORE\_PATH Data[3]/read\_disable Data[3]/host\_din

IGNORE\_PATH Data[4]/read\_disable Data[4]/host\_din

IGNORE\_PATH Data[5]/read\_disable Data[5]/host\_din

IGNORE\_PATH Data[6]/read\_disable Data[6]/host\_din

IGNORE\_PATH Data[7]/read\_disable Data[7]/host\_din

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 24 07:41:46 1988

\*\*\*\*\*  
Chip: ~sni/sni/xserial

Timing Analyzer

-----Genesil Version v7.0\_Beta-----

VIOLATION MODE

Fabline: NSC\_CN12A

Corner: GUARANTEED

Junction Temperature: 47 deg C

Voltage: 5.00v

External Clock: Net\_clk

Included setup files:

#0 nom\_phase\_c

(nominal op. cond. for Net\_clk)

-----  
NO VIOLATIONS

Hold time check margin: 2.0ns

-----  
INSERT MESSAGES GRAPHICS FORM

OVERLAY

RECORD

UTILITY

-----  
BACK

-----  
>TIMING>VIOLATIONS>

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 24 13:08:03 1988

\*\*\*\*\*  
Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0\_Beta-----

VIOLATION MODE

-----  
Fabline: NSC\_CN12A Corner: GUARANTEED  
Junction Temperature: 47 deg C Voltage: 5.00v  
External Clock: Proc\_clk  
Included setup files:  
#0 nom\_phase\_a (nominal op. cond. for Proc\_clk)

-----  
NO VIOLATIONS

Hold time check margin: 2.0ns

-----  
INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY

-----  
BACK

-----  
>TIMING>VIOLATIONS>

\*\*\*\*\*  
Genesil Screen Dump -- Fri Jun 24 15:43:49 1988

\*\*\*\*\*  
Chip: ~sni/sni/xserial Timing Analyzer  
-----Genesil Version v7.0\_Beta-----

VIOLATION MODE

-----  
Fabline: NSC\_CN12A Corner: GUARANTEED  
Junction Temperature: 92 deg C Voltage: 4.50v  
External Clock: Net\_clk  
Included setup files:  
#0 max\_phase\_c (max. temp. min v. for Net\_clk)  
-----

NO VIOLATIONS

Hold time check margin: 2.0ns

-----  
INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY  
-----

BACK

>TIMING>VIOLATIONS>

Jun 26 09:24 1988 screen.106 Page 5

\*\*\*\*\*  
 Genesil Screen Dump -- Sun Jun 26 09:12:39 1988

\*\*\*\*\*  
 Chip: ~sni/sni/xserial Timing Analyzer

-----Genesil Version v7.0\_Beta-----

VIOLATION MODE

-----  
 Fabline: NSC\_CN12A Corner: GUARANTEED  
 Junction Temperature: 92 deg C Voltage: 4.50v  
 External Clock: Proc\_clk  
 Included setup files:  
 #0 max\_phase\_a (max. temp. min v. for Proc\_clk)  
 -----

NO VIOLATIONS

Hold time check margin: 2.0ns

-----  
 INSERT MESSAGES GRAPHICS FORM OVERLAY RECORD UTILITY  
 -----

BACK

-----  
 >TIMING>VIOLATIONS>