

**GEORGIA TECH GT-VSF
VLSI DESIGN VERIFICATION DOCUMENT**

VLSI DEVELOPMENT REPORT
REPORT NO. VDR-0142-90-006
JULY 19, 1990

**GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY**

Contract No. DASG60-89-C-0142
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COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology
Atlanta, Georgia 30332-0540

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JULY 19, 1990

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INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems / Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech spatial filter chip, GT-VSF.

Table 1. Georgia Tech Chip Set for AHAT

| Design | DV Passed | Tape Delivered | Fabricated | Tested |
|---------------|------------------|-----------------------|-------------------|---------------|
| GT-VFPU | 1/17/89 | 5/10/90 | 5/19/89 | 4/4/90 |
| GT-VNUC | | | | |
| GT-VTF | | | | |
| GT-VTHR | | | | |
| GT-VCLS | 1/26/90 | 7/12/90 | 7/13/90 | |
| GT-VCTR | 2/8/90 | 7/12/90 | 7/13/90 | |
| GT-VIAG | | | | |
| GT-VDAG | | | | |
| GT-VSNI | 1/17/89 | 5/23/90 | 4/14/89 | 4/4/90 |
| GT-VSM8 | 1/17/89 | 6/8/90 | 5/6/89 | 4/4/90 |
| GT-VSF | 9/12/89 | 7/19/90 | 7/13/90 | |

DV CHECKLIST

1. DV CONTROL NUMBER : _____

2. CUSTOMER INFORMATION

Customer Name: Georgia Tech Chip Name: GT-VSF (Sfilter)

Address : 400 10th Street FAX : (404) 894-3120
CRB Room 377

Atlanta, GA 30332

Project Manager: Dr. C.O. Alford Phone: (404) 894-2505

Design Engineer: Amar Ghori Phone: (404) 894-2527

_____ Phone: _____

Test Engineer : Joseph Chamdani Phone: (404) 894-2527

3. SERVICES INFORMATION

Design Verification Service only. PO # _____

_____ Prototype Service and Design Verification. PO # _____

_____ 1.8% Maintenance

_____ SCS Test _____ Foundry Test _____ Customer Test

When DV is complete, send verified physical database tape to

Customer N Silicon Vendor N

4. DV CONTACT: _____ Phone: _____

A-4 DV CHECKLIST

5. REGRESSION

5.1 GENESIL Version: 7.1
5.2 Name of Session Log from recompile: DV_session.LOG
5.3 Include DV_regression.CMD: DV_regression_001 (simulation and timing)
5.4 Size of database (MB): 80 Density: 6250 1600 TK50
Tar XX wbak _____ Apollo Cartridge _____
(compressed) Sun Cartridge XX

6. FUNCTIONAL INFORMATION (check when included)

6.1 Key Parameters : _____
6.2 DV_pin_description : XX
6.3 Block Diagram : XX
6.4 Functional Description : XX
6.5 Timing Diagrams at Pins : _____
6.6 Annotated Views : XX Annotated Schematics: XX
6.7 Chip Text Specification on tape : _____ Density: 6250 1600 TK50
Apollo Cartridge _____
Sun Cartridge XX

7. PHYSICAL INFORMATION

7.1 Fabline Name : HPL-CIOA
Customer-Specific: Y Fabline GENECAL Directory on tape: Y
Fabline GENESIL Directory on tape : Y
Fabline Calibration Status: Production: XX Beta: _____ Alpha: _____

NOTE: If not a production fabline, then approval from SCS is required.

7.2 Plots: (check when included or indicate filename)
Chip Route (D size): XX Bonding Diagram (B size) : XX
Route _____ Bonding _____
Filename: route_1.031 Filename: bond_1.031

7.3 Die Size: Reported Die Size: 335x311 square-mils
Maximum Acceptable Die Size ($\pm 2\%$): 394x394 square-mils
Minimum Acceptable Die Size ($\pm 2\%$): 234x234 square-mils

7.4 GENESIL Package Name : CPGA100e Spec included? Y
Cavity/Well Size : 434 mils by 434 mils
Non-GENESIL Supplied Package? Y Text Spec included on tape? Y
Vendor Name/Part # : KYOCERA KD-82258B Foundry Approval? N

7.5 External Block: None

7.6 LRAM: Y LROM: Y LPLA: Y LogicCompiler Blocks: N

7.7 Test Pad (PM Pad) is included? N (Required for PS)

7.8 Power Pad : 2 pair of Core Power 5 pair of Ring Power Pad
 +1 ring VDD Pad

NP protection for nwell pad? Y N

Error in PADRING.033 (PADRING.DRC)? Y N Hardcopy attached? Y N

ESD requirements Normal Approved by SCS? Y N

8. ELECTRICAL INFORMATION

8.1 Chip Frequency

Specified in netlist: 10 MHz Target frequency: 3 MHz

8.2 Power Dissipation: GENESIL=0.8 W at 10 MHz Spec= W at MHz

8.3 Operating Voltage: from 4.5 Volts to 5.5 Volts

9. SIMULATION

9.1 Number of Clocking Regimes : 1

| | Clock Pad Name | DIV/NO_DIV | Ext Clock Name | Int PHASE_A/PHASE_B Name |
|----|----------------|------------|----------------|--------------------------|
| 1. | pixelclk | No_DIV | Pixel_clk | PHASE_A/PHASE_B |
| 2. | _____ | _____ | _____ | _____ |
| 3. | _____ | _____ | _____ | _____ |
| 4. | _____ | _____ | _____ | _____ |
| 5. | _____ | _____ | _____ | _____ |

9.2 Simulation Setup Files:

Name: _____ Listings attached: _____

Description: _____

Affected Tests: _____

Name: _____ Listings attached: _____

Description: _____

Affected Tests: _____

A-6 DV CHECKLIST

Name: _____ Listings attached: _____

Description: _____

Affected Tests: _____

9.3 Test Vector Set:

Total No. of Vectors: 22,602

NOTE: Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz.
Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name: add test_trace No of vectors: 164
Description: manufacturing test for address

Portions of Chip Tested: adders

Pass with GFL model? XX
Pass with GSL model? XX Use for PS testing? Y N
Pass Fight Test? _____

2. Name: coefftest_trace No of vectors: 671
Description: coefficient testing

Portions of Chip Tested: _____

Pass with GFL model? x
Pass with GSL model? x Use for PS testing? Y N
Pass Fight Test? _____

3. Name: dead pix_trace No of vectors: 194
Description: dead pixel condition testing

Portions of Chip Tested: _____

Pass with GFL model? XX
Pass with GSL model? XX Use for PS testing? Y N
Pass Fight Test? _____

4. Name: frame 10x10 trace No of vectors: 150
 Description: _____

 Portions of Chip Tested: _____

 Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

5. Name: frame10x128 trace No of vectors: 680
 Description: _____

 Portions of Chip Tested: _____

 Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

6. Name: frame128x128 trace No of vectors: 16552
 Description: _____
 Description: _____

 Portions of Chip Tested: _____

 Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

7. Name: frame13x15 trace No of vectors: 250
 Description: _____

 Portions of Chip Tested: _____

 Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

8. Name: frame19x17x2_trace No of vectors: 706
Description: _____

Portions of Chip Tested: _____

Pass with GFL model? XX
Pass with GSL model? XX Use for PS testing? Y N
Pass Fight Test? _____

9. Name: frame5x5_trace No of vectors: 71
Description: _____

Portions of Chip Tested: _____

Pass with GFL model? XX
Pass with GSL model? XX Use for PS testing? Y N
Pass Fight Test? _____

10. Name: interface_trace No of vectors: 500
Description: _____
Description: host interface testing

Portions of Chip Tested: _____

Pass with GFL model? XX
Pass with GSL model? XX Use for PS testing? Y N
Pass Fight Test? _____

11. Name: multa_trace No of vectors: 433
Description: _____
Description: multiplier A testing

Portions of Chip Tested: _____

Pass with GFL model? XX
Pass with GSL model? XX Use for PS testing? Y N
Pass Fight Test? _____

12. Name: multb trace No of vectors: 400
 Description: _____
mult B testing

Portions of Chip Tested: _____

Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

13. Name: multc trace No of vectors: 293
 Description: _____
mult C testing

Portions of Chip Tested: _____

Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

14. Name: multd trace No of vectors: 267
 Description: _____
 Description: mult D testing

Portions of Chip Tested: _____

Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

15. Name: out trace No of vectors: 197
 Description: _____
output testing

Portions of Chip Tested: _____

Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

16. Name: pipetest_trace No of vectors: 1074
 Description: Pipe testing

 Portions of Chip Tested: _____

 Pass with GFL model? XX
 Pass with GSL model? XX Use for PS testing? Y N
 Pass Fight Test? _____

17. Name: _____ No of vectors: _____
 Description: _____

 Portions of Chip Tested: _____

 Pass with GFL model? _____
 Pass with GSL model? _____ Use for PS testing? Y N
 Pass Fight Test? _____

18. Name: _____ No of vectors: _____
 Description: _____
 Description: _____

 Portions of Chip Tested: _____

 Pass with GFL model? _____
 Pass with GSL model? _____ Use for PS testing? Y N
 Pass Fight Test? _____

9.4 IMS Grouping within limitation? Y N (Required for PS only)

9.5 Tester clock frequency = 3 MHz

9.6 Signals that must be glitch free: Y N

| Signal Name | Ran GSL with glitch detection feature on? |
|-------------|---|
| ----- | ----- |
| 1. _____ | Y N |
| 2. _____ | Y N |
| 3. _____ | Y N |
| 4. _____ | Y N |
| 5. _____ | Y N |

Name: _____ Listings attached: _____
 Temperature: _____ Voltage: _____
 Description : _____

10.4 Critical Boundary Conditions:

List critical paths here or annotate the timing report.
 Attach additional pages if needed.

Clock Name: Pixel_clk

| | report | limit ($\pm 5\%$) | report | limit ($\pm 5\%$) |
|--------------------|-----------------|---------------------|--------|---------------------|
| 1. Phase 1 High | <u>104.7ns</u> | <u>165 ns</u> | _____ | _____ |
| 2. Phase 2 High | <u>162.7 ns</u> | <u>165 ns</u> | _____ | _____ |
| 3. Symmetric Cycle | <u>325.5 ns</u> | <u>330 ns</u> | _____ | _____ |
| 4. Minimum Cycle | <u>267.4 ns</u> | <u>330 ns</u> | _____ | _____ |

Outputs

| | Signal Name | load (pF) | delay | limit |
|-----|-------------|-----------|-------|-------|
| 1. | _____ | _____ | _____ | _____ |
| 2. | _____ | _____ | _____ | _____ |
| 3. | _____ | _____ | _____ | _____ |
| 4. | _____ | _____ | _____ | _____ |
| 5. | _____ | _____ | _____ | _____ |
| 6. | _____ | _____ | _____ | _____ |
| 7. | _____ | _____ | _____ | _____ |
| 8. | _____ | _____ | _____ | _____ |
| 9. | _____ | _____ | _____ | _____ |
| 10. | _____ | _____ | _____ | _____ |

Inputs

| | Signal Name | setup report/limit | hold report/limit |
|-----|-------------|-----------------------|----------------------|
| 1. | _____ | _____/____ | _____/____ |
| 2. | _____ | _____/____ | _____/____ |
| 3. | _____ | _____/____ | _____/____ |
| 4. | _____ | _____/____ | _____/____ |
| 5. | _____ | _____/____ | _____/____ |
| 6. | _____ | _____/____ | _____/____ |
| 7. | _____ | _____/____ | _____/____ |
| 8. | _____ | _____/____ | _____/____ |
| 9. | _____ | _____/____ | _____/____ |
| 10. | _____ | _____/____ | _____/____ |

10.5 Hold Time Violations: none (At 1.7 nsec.)

A-10 DV CHECKLIST

11. DC CHARACTERISTICS

| PARAMETERS | DESCRIPTION | CONDITIONS 0 to 70 | CONDITIONS -55 to +125 | MIN | MAX |
|------------------------------|------------------------------------|-----------------------|---------------------------|-------|-------|
| DATA PAD INPUT ONLY | | | | | |
| VIH | Input High Voltage | | | 2.0V | |
| VIL | Input Low Voltage | | | | 0.8V |
| IIL | Input Leakage | VSS<Vin<VDD | VSS<Vin<VDD | -10uA | 10uA |
| CIN | Input Capacitance | | | | 8.0pf |
| DATA PAD OUTPUT ONLY | | | | | |
| VOH | Output High Voltage | VDD= 4.5V IOH=-2.2 | VDD= 4.5V IOH=-2mA | 2.4V | |
| VOL | Output Low Voltage | VDD= 4.5V IOL= 8mA | VDD= 4.5V IOL= 5mA | | 0.4V |
| IOZ | Output Leakage current (high Z) | VSS<Vout<VDD | VSS<Vout<VDD | -10uA | 10uA |
| COU | Output Capacitance | | | | 7.0pf |
| DATA PAD INPUT/OUTPUT | | | | | |
| VOH | Output High Voltage | VDD= 4.5V IOH=-2.2 | VDD= 4.5V IOH=-2mA | 2.4V | |
| VOL | Output Low Voltage | VDD= 4.5V IOL= 8mA | VDD= 4.5V IOL= 5mA | | 0.4V |
| VIH | Input High Voltage | | | 2.0V | |
| VIL | Input Low Voltage | | | | 0.8V |
| IOZ | Output leakage current (high Z) | VSS<Vout<VDD | VSS<Vout<VDD | -10uA | 10uA |
| CIO | Input/Output Capacitance | | | | 7.0pf |
| CLOCK PAD | | | | | |
| VIH | Input High Voltage | | | 3.9V | |
| VIL | Input Low Voltage | | | | 0.6V |
| IIL | Input Leakage | VSS<Vin<VDD | VSS<Vin<VDD | -10uA | 10uA |
| CIN | Input Capacitance | | | | 15pf |

NOTE: All parameters at a supply voltage of VDD = 5V ± 10%.

12. CUSTOMER COMMENTS

Pre-Verification Comments

Three sets of vector files are provided as explained below
'name'.083 = normal vector file created from .089 file
'name'_trace.083 = trace object file
'name trace.call.083 = collapsed trace file using
"collapse" program.

13. CUSTOMER APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : *Amphai* Date 8/30/89
 Title : Research Engineer - I

14. SCS APPROVAL

Pre-Verification Comments

SCS Approval: _____ Date ____/____/____
 Regional Field Application Consultant

SCS Approval: _____ Date ____/____/____
 Technical Support Team Leader

GT-VSF: SPATIAL FILTER

INTRODUCTION

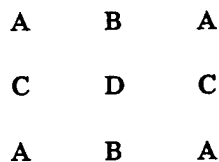
The Spatial Filter chip implements a 9-point bi-symmetric filter. The purpose of this chip is to eliminate or suppress noise in the image frame through spatial filtering. The chip is designed to handle arbitrary frame sizes from 5x5 pixels upto 128x128 pixels. Frame size is determined automatically by the chip based on incoming signals and the chip is appropriately configured. The chip is also designed to handle dead pixels between consecutive rows as well as dead pixels between consecutive frames. The chip accepts a 16-bit unsigned pixel intensity as input and provides a 17-bit filtered output in sign magnitude format. Filter coefficients are loaded into the chip through the host. The host may also read back these coefficients at any time. Due to the nature of the algorithm, the chip introduces a latency of 130 clock cycles

FUNCTIONALITY

The filtered intensity of each pixel is computed as a weighted sum of the intensities of its nearest neighbors as well as itself. These weights are pre-loaded by the host when the chip is in the "load" state. The weights are in 16 bit sign magnitude format with 1-bit integer and 14-bit fraction resolution. Thus the range of the weights is -1.999999 to +1.999999 with a resolution of 2^{-13} .

The exact I/O relation for this chip are as follows.

Let the filter coefficients be labelled as shown below and let Q be the output function of the chip.



Then,

$$Q(P_k) = A(P_{k-129} + P_{k-127} + P_{k+127} + P_{k+129}) + B(P_{k-128} + P_{k+128}) + C(P_{k-1} + P_{k+1}) + DP_k \quad \text{--- (1)}$$

where,

P_n = The intensity of pixel n
 $Q(P_k)$ = The output intensity for pixel k

A causal form of equation (1) is :

$$Q(P_{k-129}) = A(P_{k-258} + P_{k-256} + P_{k-2} + P_k) + B(P_{k-257} + P_{k-1}) + C(P_{k-130} + P_{k-127}) + DP_{k-129} \quad \text{--- (2)}$$

The primary function of the Spatial filter chip is to implement equation (2). Secondary requirements are listed below.

- (1). Filter coefficients must be loadable at all times.
- (2). Pixel intensities should be output every cycle after the initial latency.
- (3). The end of a frame should be signalled by the chip.
- (4). For the purpose of computation, frame edges behave as pixels with null intensity.

INPUT/OUTPUT

INPUTS

| <u>Signal</u> | <u>Timing</u> | <u>Description</u> |
|-----------------|---------------|--|
| Pixel_in[15:0] | VB(t) | Data signal denoting intensity of current pixel. |
| Begin_Frame_in | VB(t) | Active high. When active, it signals the beginning of current frame. |
| End_Frame_in | VB(t) | Active high. When active, it signals the end of current frame. |
| Begin_Row_in | VB(t) | Active high. When active, it signals the start of current row. |
| End_Row_in | VB(t) | Active high. When active, it signals the end of current row. |
| Reset | VB(t) | Active high. When active, it resets the chip. |
| Pixel_clk | N/A | Clock signal. |
| Addr[7:0] | VB(t) | Host address bus. |
| Ios | VB(t) | Host control signal for read/write interface. |
| Chip_Id[3:0] | VB(t) | 4-bit Chip Id. Used to select chip. |
| Dev_select[3:0] | VB(t) | Host signal. Selects the chip if it matches chip-id |
| Ode | VB(t) | Output device enable. Host control signal. |

OUTPUTS

| <u>Signal</u> | <u>Timing</u> | <u>Description</u> |
|---------------|---------------|--------------------|
|---------------|---------------|--------------------|

| | | |
|-----------------|-------|--|
| Pixel_out[15:0] | PROP | Data signal denoting intensity of pixel after filtering. |
| Begin_Frame_out | SB(t) | Active high. When active, it signals the beginning of current frame. |
| End_Frame_out | SB(t) | Active high. When active, it signals the end of current frame. |
| Begin_Row_out | SB(t) | Active high. When active, it signals the start of current row. |
| End_Row_out | SB(t) | Active high. When active, it signals the end of current row. |

BI-DIRECTIONAL

| | | |
|------------|-------------|--|
| Data[15:0] | SB(t)/VB(t) | Host data bus. Used to read and write to chip. |
|------------|-------------|--|

CHIP DESIGN

The chip is composed of the following major components

Pipe: This is a 129 stage memory structure that stores incoming pixel intensities and makes them available to the computational element of the chip at the appropriate time. The pipe also contains control circuitry to determine the size of the incoming image frame and configures itself appropriately. This frame size is held constant till the chip is reset.

sumA: A simple computational module that adds the intensities that are to be multiplied by weight A.

$$\text{sumA} := P_k + P_{k-2} + P_{k-256} + P_{k-258}$$

sumB: This module adds the intensities that are to be multiplied by weight B.

$$\text{sumB} := P_{k-1} + P_{k-257}$$

sumC: This module adds the intensities that are to be multiplied by weight C.

$$\text{sumC} := P_{k-129} + P_{k-127}$$

multA: This module multiplies the output of sumA by coefficient A.

multB: This module multiplies the output of sumB by coefficient B.

multC: This module multiplies the output of sumC by coefficient C.

multD: This module multiplies P_{k-128} by coefficient D.

Output: This module adds the outputs from multA, multB, multC and multD, converts the result to sign magnitude form and sets the output to maximum intensity if overflow occurs.

Host Interface: This module provides the circuitry required to interface with a fast host. The interface is designed to handle a host whose clock speed is an integer multiple of the chip clock speed.

Control: This module provides address decoding, sequencing and other related features. Control signals to all of the above blocks are generated by this module.

LAYOUT , TIMING & POWER DISSIPATION

The design is implemented in NCR 1.0 micron VLSI process. The die size for this chip is 335x311 sq. mils. Preliminary timing figures show a cycle time of 275ns. Power dissipation is 0.8 Watts.

FUNCTIONAL TEST

The design was successfully tested with various image frames. The frames used are listed below.

| <u>Frame size</u> | <u>Type</u> |
|-------------------|---|
| 5x5 | Normal pixel intensities. |
| 10x10 | Very high pixel intensities. |
| 10x10 | Negative pixel intensities. |
| 128x10 | Normal pixel intensities. |
| 128x128 | Normal pixel intensities. |
| Scene 19x17x2 | Dead pixels between frames. Second frame with very high pixel values. |
| 10x10 | Dead pixels between rows. |

PACKAGING

The chip uses a 100 pin Ceramic Pin Grid Array.

```

/*****
/*      Pin Description of Spatial Filter Chip (GT-VSF)      */
/*****

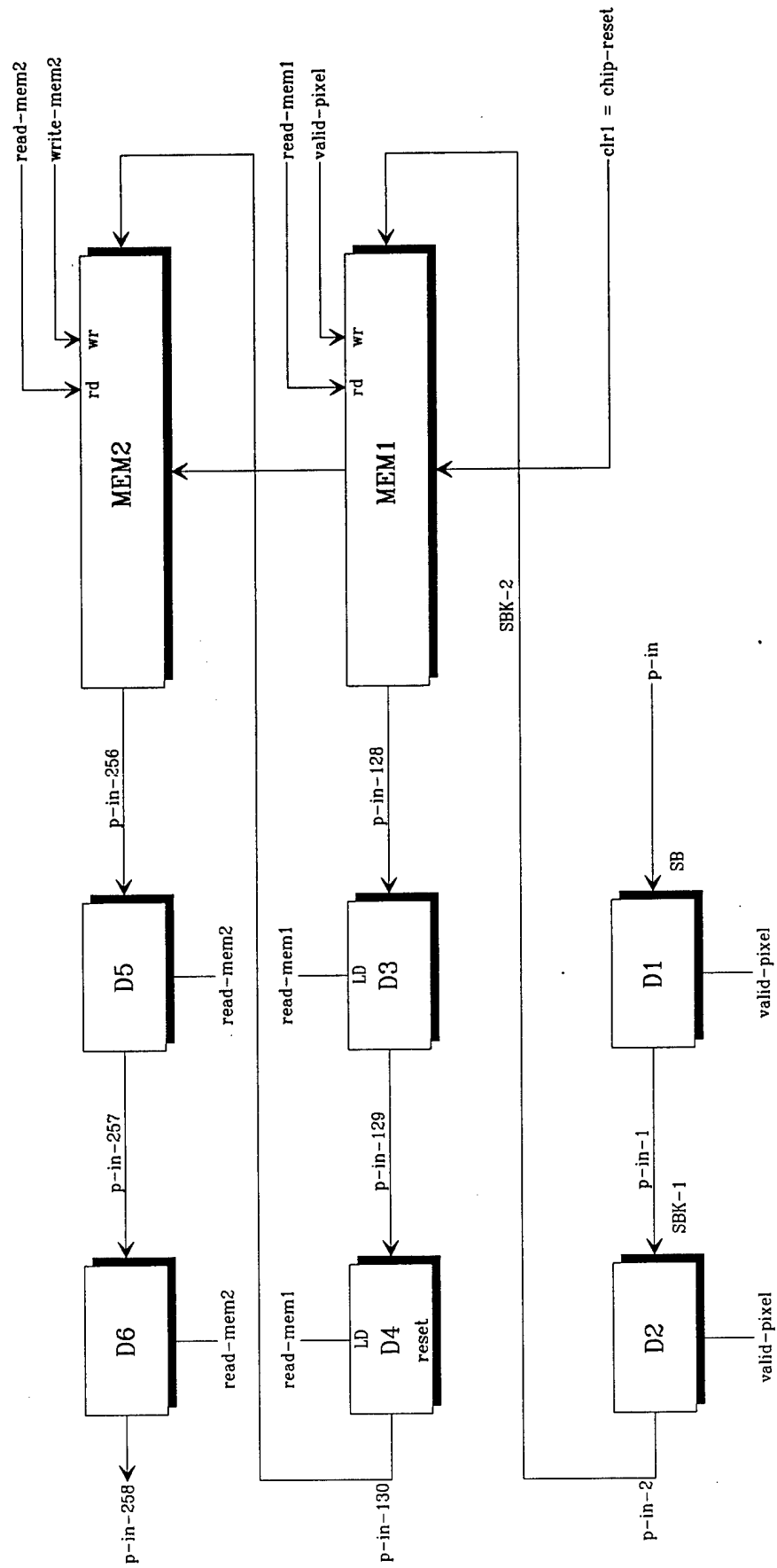
```

| PIN_# | ABBREVIATED NAME | SIGNAL_NAME | PAD_TYPE | TIMING |
|-------|------------------|-----------------|------------|--------|
| 1 | VDD | VDD | VDD CORNER | |
| 2 | Data[5] | Data[5] | DATA IO | SB/VB |
| 3 | Data[6] | Data[6] | DATA IO | SB/VB |
| 4 | Data[7] | Data[7] | DATA IO | SB/VB |
| 5 | Data[8] | Data[8] | DATA IO | SB/VB |
| 6 | Data[9] | Data[9] | DATA IO | SB/VB |
| 7 | Data[10] | Data[10] | DATA IO | SB/VB |
| 8 | Data[11] | Data[11] | DATA IO | SB/VB |
| 9 | Data[12] | Data[12] | DATA IO | SB/VB |
| 10 | Data[13] | Data[13] | DATA IO | SB/VB |
| 11 | Data[14] | Data[14] | DATA IO | SB/VB |
| 12 | Data[15] | Data[15] | DATA IO | SB/VB |
| 13 | Pxl_in[0] | Pixel_in[0] | DATA IN | VB |
| 14 | Pxl_in[1] | Pixel_in[1] | DATA IN | VB |
| 15 | Pxl_in[2] | Pixel_in[2] | DATA IN | VB |
| 16 | Pxl_in[3] | Pixel_in[3] | DATA IN | VB |
| 17 | Pxl_in[4] | Pixel_in[4] | DATA IN | VB |
| 18 | Pxl_in[5] | Pixel_in[5] | DATA IN | VB |
| 19 | Pxl_in[6] | Pixel_in[6] | DATA IN | VB |
| 20 | Pxl_in[7] | Pixel_in[7] | DATA IN | VB |
| 21 | VSS | VSS | VSS RING | |
| 22 | Pxl_in[8] | Pixel_in[8] | DATA IN | VB |
| 23 | Pxl_in[9] | Pixel_in[9] | DATA IN | VB |
| 24 | Pxl_in[10] | Pixel_in[10] | DATA IN | VB |
| 25 | VSS | VSS | VSS CORE | |
| 26 | VSS | VSS | VSS CORNER | |
| 27 | Pxl_in[11] | Pixel_in[11] | DATA IN | VB |
| 28 | Pxl_in[12] | Pixel_in[12] | DATA IN | VB |
| 29 | Pxl_in[13] | Pixel_in[13] | DATA IN | VB |
| 30 | Pxl_in[14] | Pixel_in[14] | DATA IN | VB |
| 31 | Pxl_in[15] | Pixel_in[15] | DATA IN | VB |
| 32 | Multtest | Multtest | DATA IN | VB |
| 33 | VDD | VDD | VDD RING | |
| 34 | Addtest | Addertest | DATA IN | VB |
| 35 | VDD | VDD | VDD CLOCK | |
| 36 | VSS | VSS | VSS CLOCK | |
| 37 | Pxl_Clk | Pixel_clk | CLOCK | |
| 38 | VDD | VDD | VDD CORE | |
| 39 | N_reset | N_reset | DATA IN | WA |
| 40 | Erow_in | End_row_in | DATA IN | VB |
| 41 | Brow_in | Begin_row_in | DATA IN | VB |
| 42 | VSS | VSS | VSS RING | |
| 43 | Bfrm_in | Begin_frame_in | DATA IN | VB |
| 44 | Efrm_in | End_frame_in | DATA IN | VB |
| 45 | Bfrm_out | Begin_frame_out | DATA OUT | SB |
| 46 | Efrm_out | End_frame_out | DATA OUT | SB |
| 47 | Brow_out | Begin_row_out | DATA OUT | SB |
| 48 | Ode | Ode | DATA IN | VB |
| 49 | - | | | |
| 50 | - | | | |
| 51 | VDD | VDD | VDD CORNER | |
| 52 | Ios | Ios | DATA IN | VB |
| 53 | DR_n_aDR | DR_n_aDR | DATA OUT | SB |
| 54 | Erow_out | End_row_out | DATA OUT | SB |
| 55 | Host_addr[4] | Host_addr[4] | DATA IN | VB |
| 56 | Host_addr[3] | Host_addr[3] | DATA IN | VB |
| 57 | Host_addr[2] | Host_addr[2] | DATA IN | VB |
| 58 | Host_addr[1] | Host_addr[1] | DATA IN | VB |

| | | | | |
|-----|-------------|---------------|------------|-------|
| 59 | Host_adr[0] | Host_addr[0] | DATA IN | VB |
| 60 | Dev_sel[0] | Dev_select[0] | DATA IN | VB |
| 61 | Dev_sel[1] | Dev_select[1] | DATA IN | VB |
| 62 | Dev_sel[2] | Dev_select[2] | DATA IN | VB |
| 63 | Dev_sel[3] | Dev_select[3] | DATA IN | VB |
| 64 | Pix_lsb[2] | Pix_lsb[2] | DATA OUT | SB |
| 65 | Pix_lsb[1] | Pix_lsb[1] | DATA OUT | SB |
| 66 | Pix_lsb[0] | Pix_lsb[0] | DATA OUT | SB |
| 67 | VDD | VDD | VDD RING | |
| 68 | Pix_msb[2] | Pix_msb[2] | DATA OUT | SB |
| 69 | Pix_msb[1] | Pix_msb[1] | DATA OUT | SB |
| 70 | Pix_msb[0] | Pix_msb[0] | DATA OUT | SB |
| 71 | Chip_id[3] | Chip_id[3] | DATA IN | VB |
| 72 | Chip_id[2] | Chip_id[2] | DATA IN | VB |
| 73 | Chip_id[1] | Chip_id[1] | DATA IN | VB |
| 74 | Chip_id[0] | Chip_id[0] | DATA IN | VB |
| 75 | Sign | Sign | DATA OUT | SB |
| 76 | VSS | VSS | VSS CORNER | |
| 77 | VDD | VDD | VDD CORNER | |
| 78 | Pxl_out[0] | Pixel_out[0] | DATA OUT | SB |
| 79 | Pxl_out[1] | Pixel_out[1] | DATA OUT | SB |
| 80 | Pxl_out[2] | Pixel_out[2] | DATA OUT | SB |
| 81 | Pxl_out[3] | Pixel_out[3] | DATA OUT | SB |
| 82 | Pxl_out[4] | Pixel_out[4] | DATA OUT | SB |
| 83 | Pxl_out[5] | Pixel_out[5] | DATA OUT | SB |
| 84 | Pxl_out[6] | Pixel_out[6] | DATA OUT | SB |
| 85 | Pxl_out[7] | Pixel_out[7] | DATA OUT | SB |
| 86 | VDD | VDD | VDD RING | |
| 87 | Pxl_out[8] | Pixel_out[8] | DATA OUT | SB |
| 88 | Pxl_out[9] | Pixel_out[9] | DATA OUT | SB |
| 89 | Pxl_out[10] | Pixel_out[10] | DATA OUT | SB |
| 90 | Pxl_out[11] | Pixel_out[11] | DATA OUT | SB |
| 91 | Pxl_out[12] | Pixel_out[12] | DATA OUT | SB |
| 92 | Pxl_out[13] | Pixel_out[13] | DATA OUT | SB |
| 93 | VSS | VSS | VSS RING | |
| 94 | Pxl_out[14] | Pixel_out[14] | DATA OUT | SB |
| 95 | Pxl_out[15] | Pixel_out[15] | DATA OUT | SB |
| 96 | Data[0] | Data[0] | DATA IO | SB/VB |
| 97 | Data[1] | Data[1] | DATA IO | SB/VB |
| 98 | Data[2] | Data[2] | DATA IO | SB/VB |
| 99 | Data[3] | Data[3] | DATA IO | SB/VB |
| 100 | Data[5] | Data[4] | DATA IO | SB/VB |

Note:

-
- (1) TIMING = SB/VB means the bidirectional pad has SB output timing and VB input timing.
 - (2) TIMING = WA means valid at both clock phases, VA and VB.



Schematic of data-flow pipe

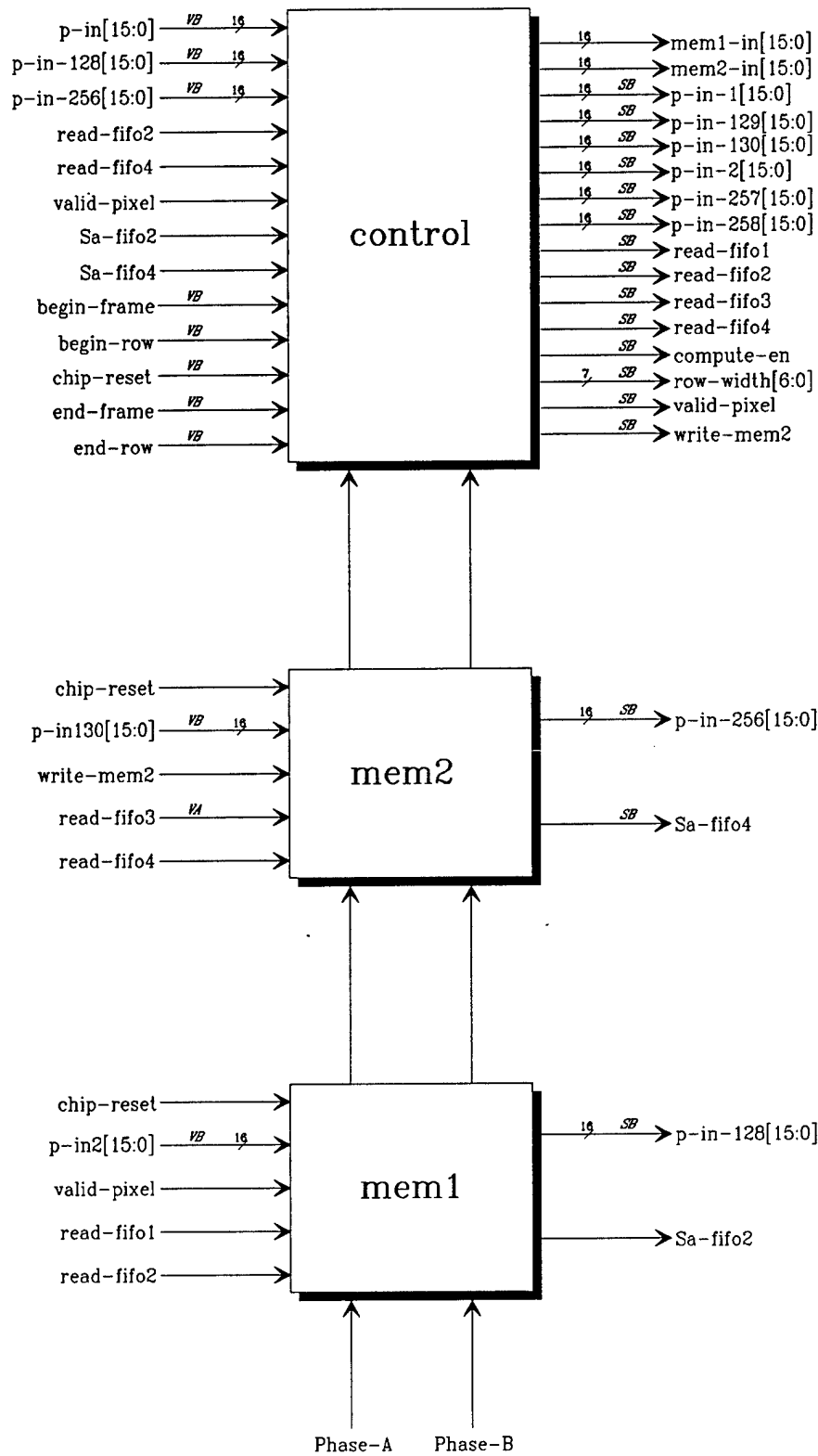
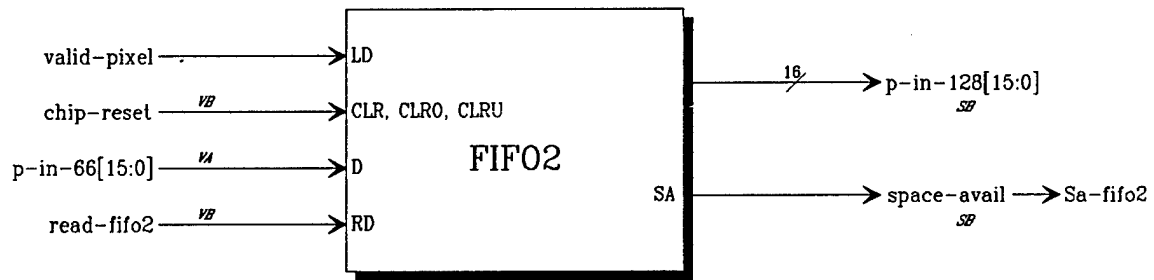
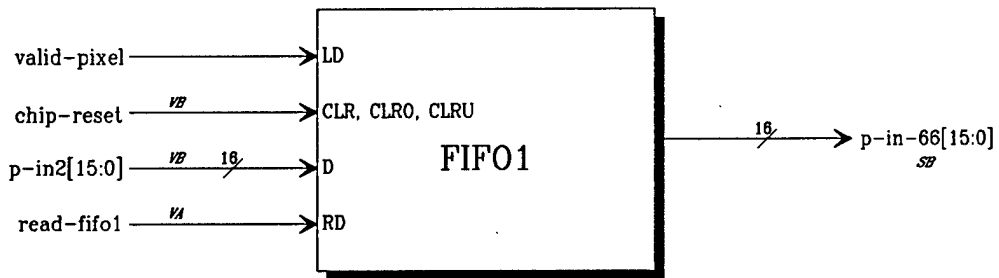
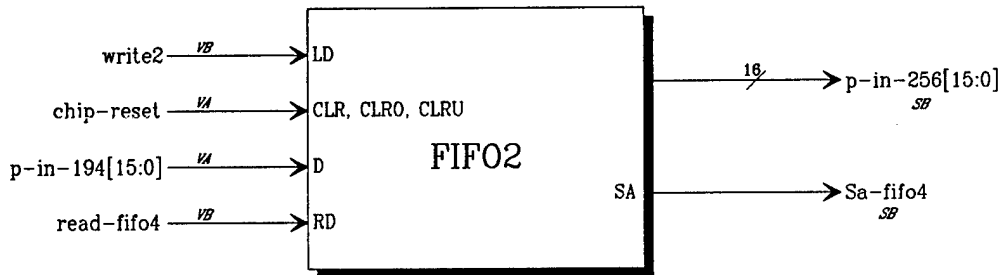
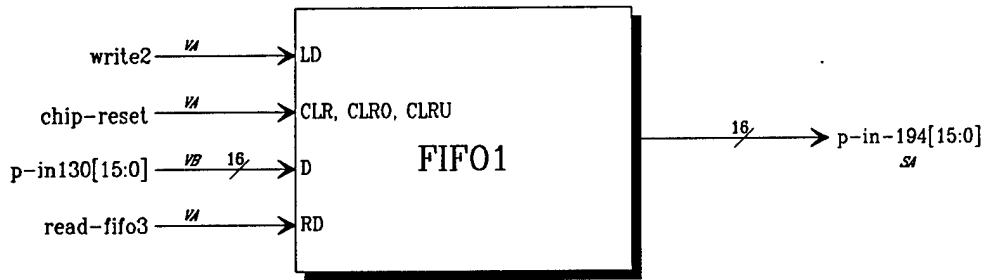


Fig. 1 /SFILTER/PIPE

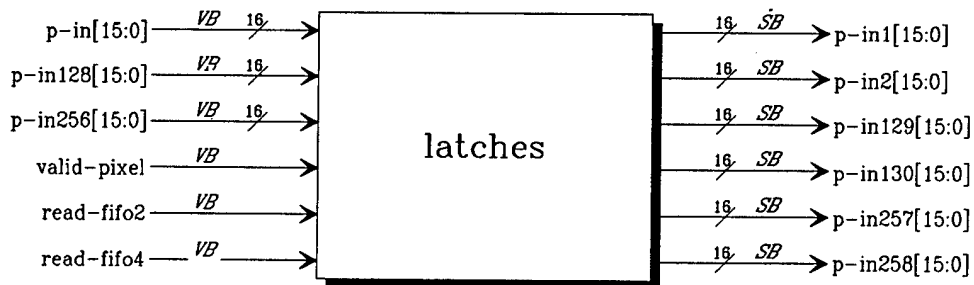
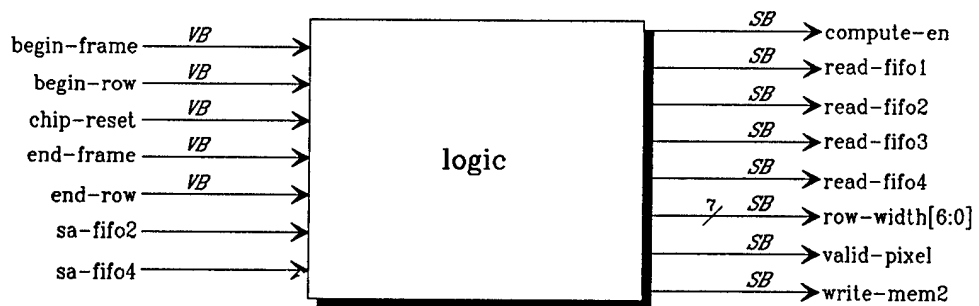
June 14, 1989



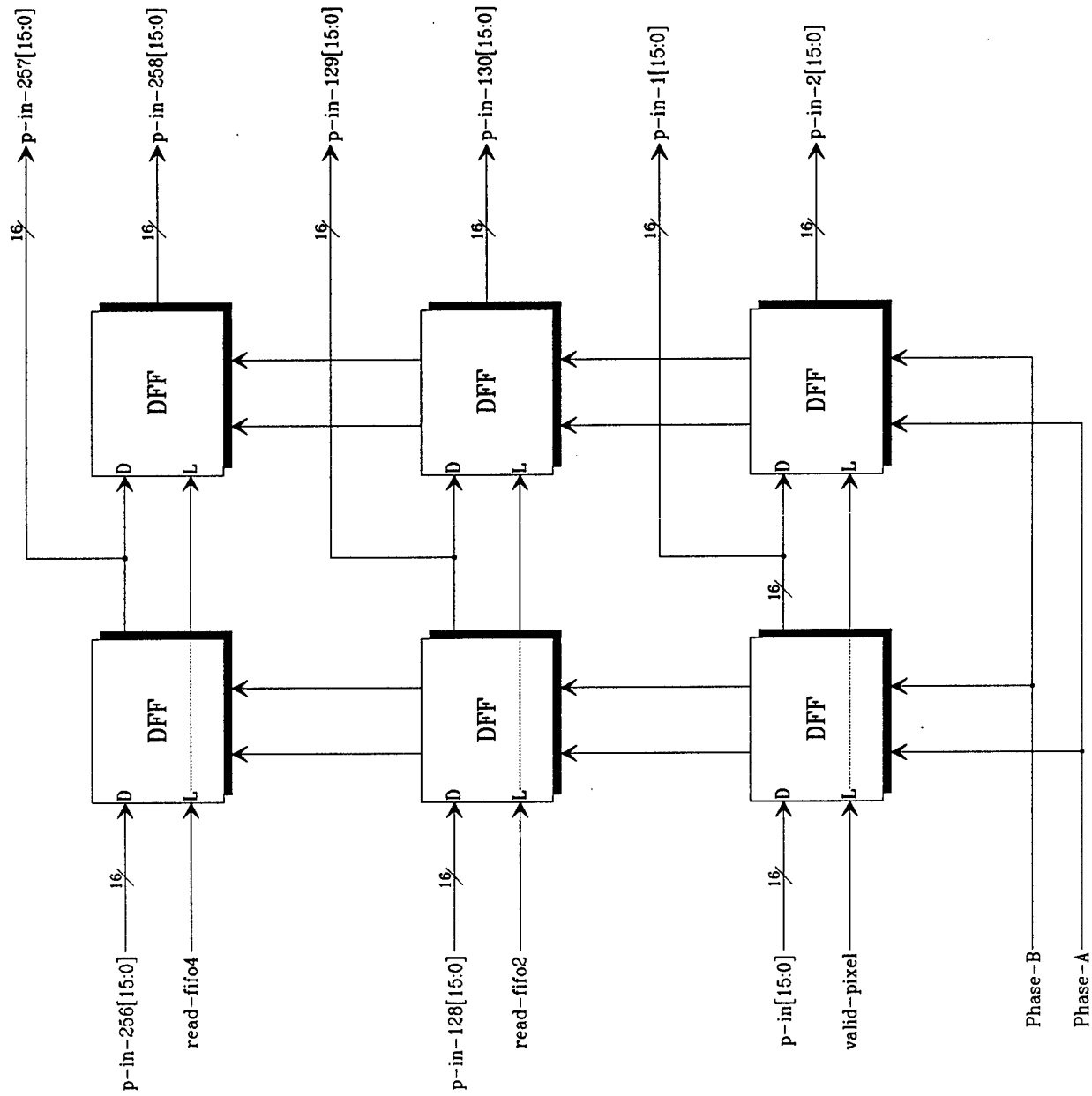
/SFILTER/PIPE/MEM1



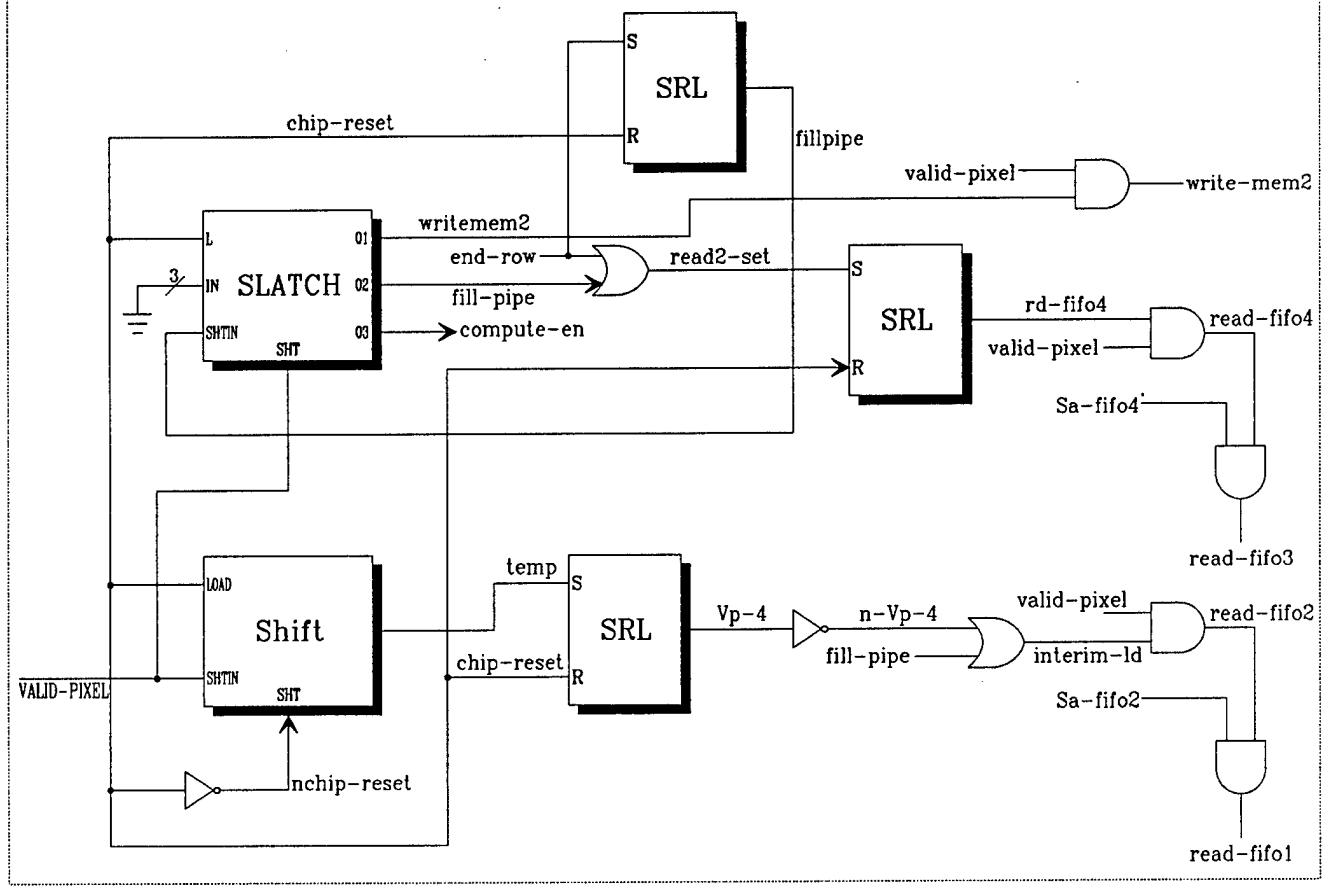
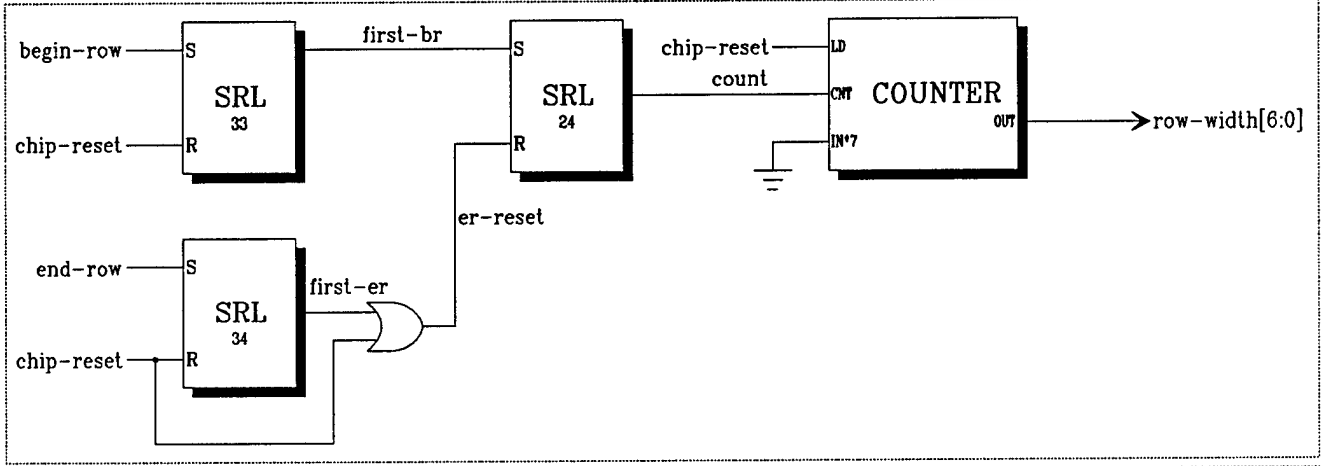
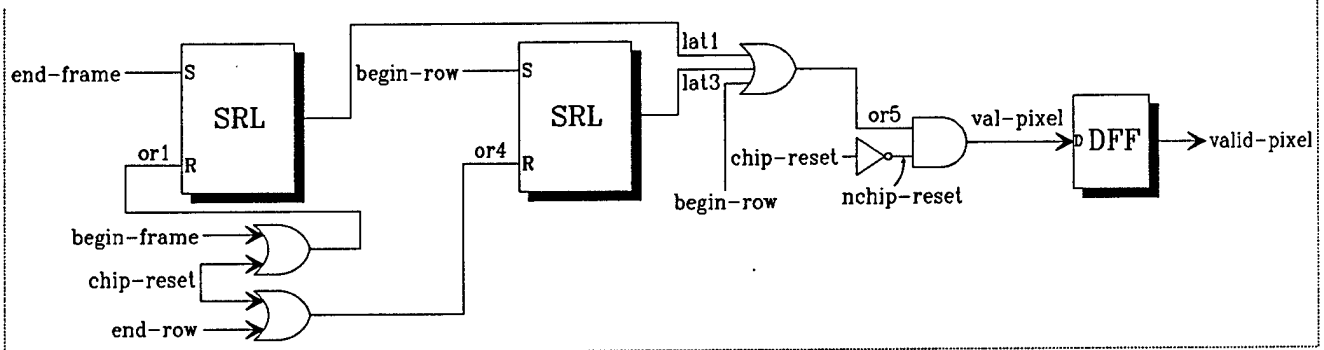
/SFILTER/PIPE/MEM2

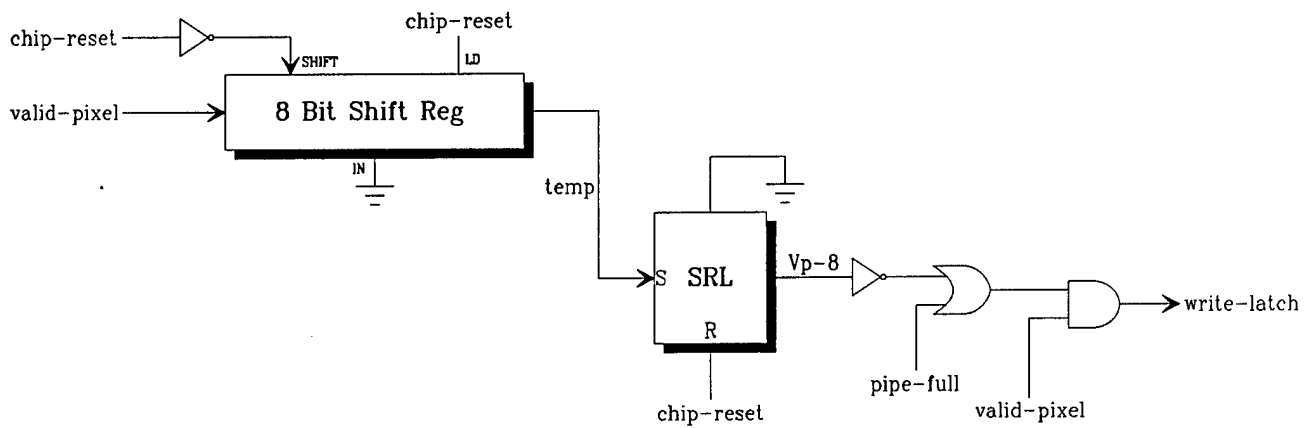
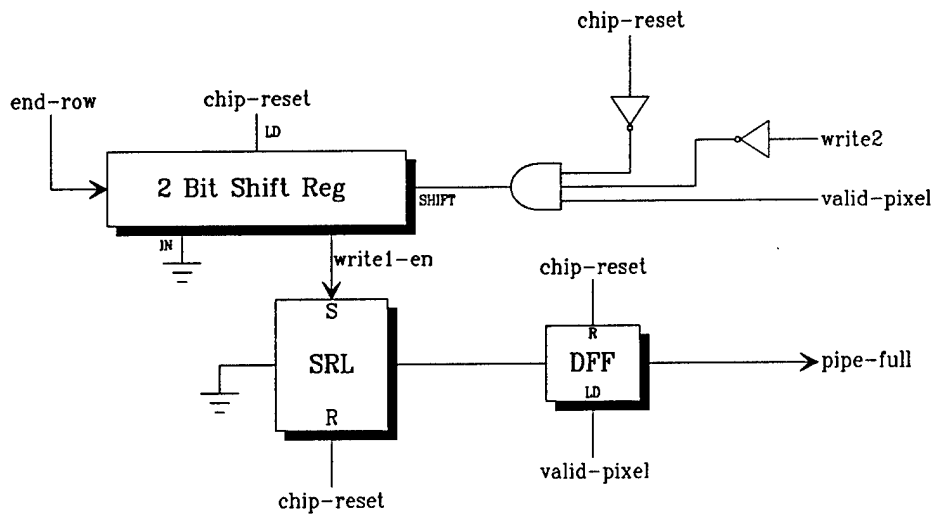


/SFILTER/PIPE/CONTROL

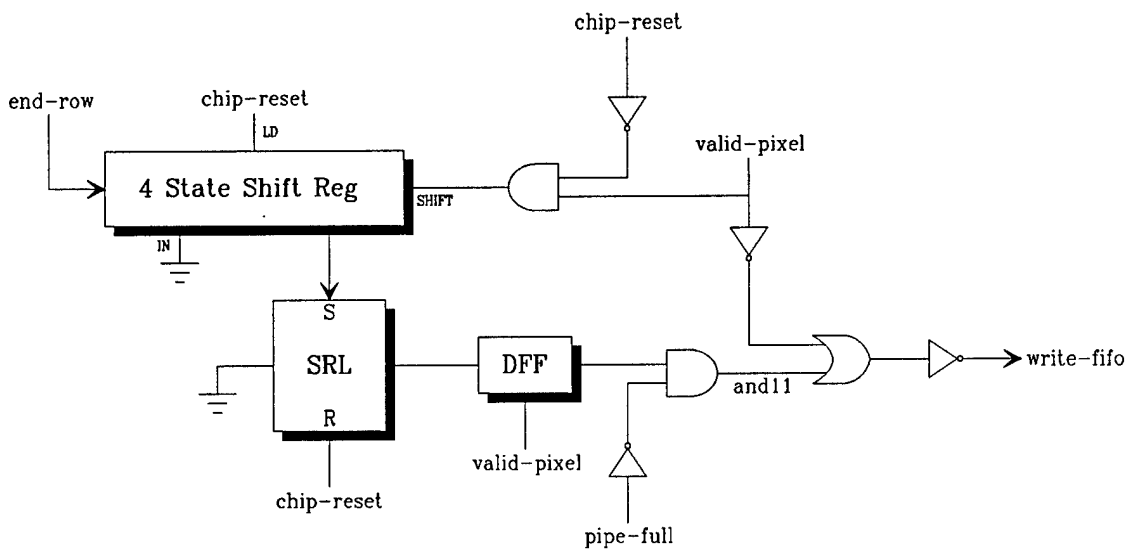
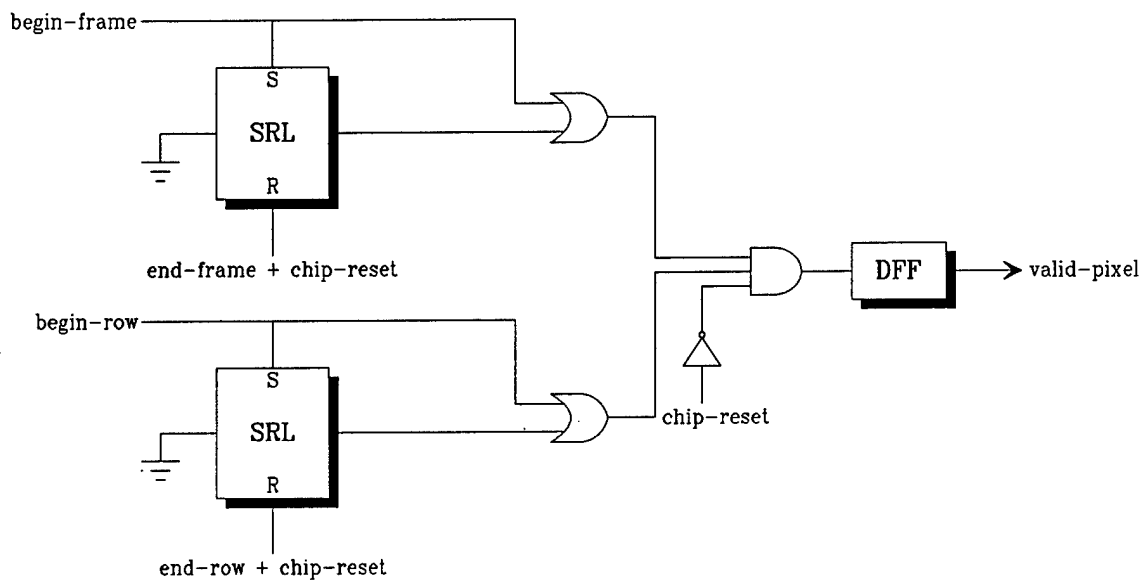


/SFILTER/PIPE/CONTROL/LATCHES





Schematic of pipe/control (page 2/2)



Schematic of pipe/control (page 1/2)

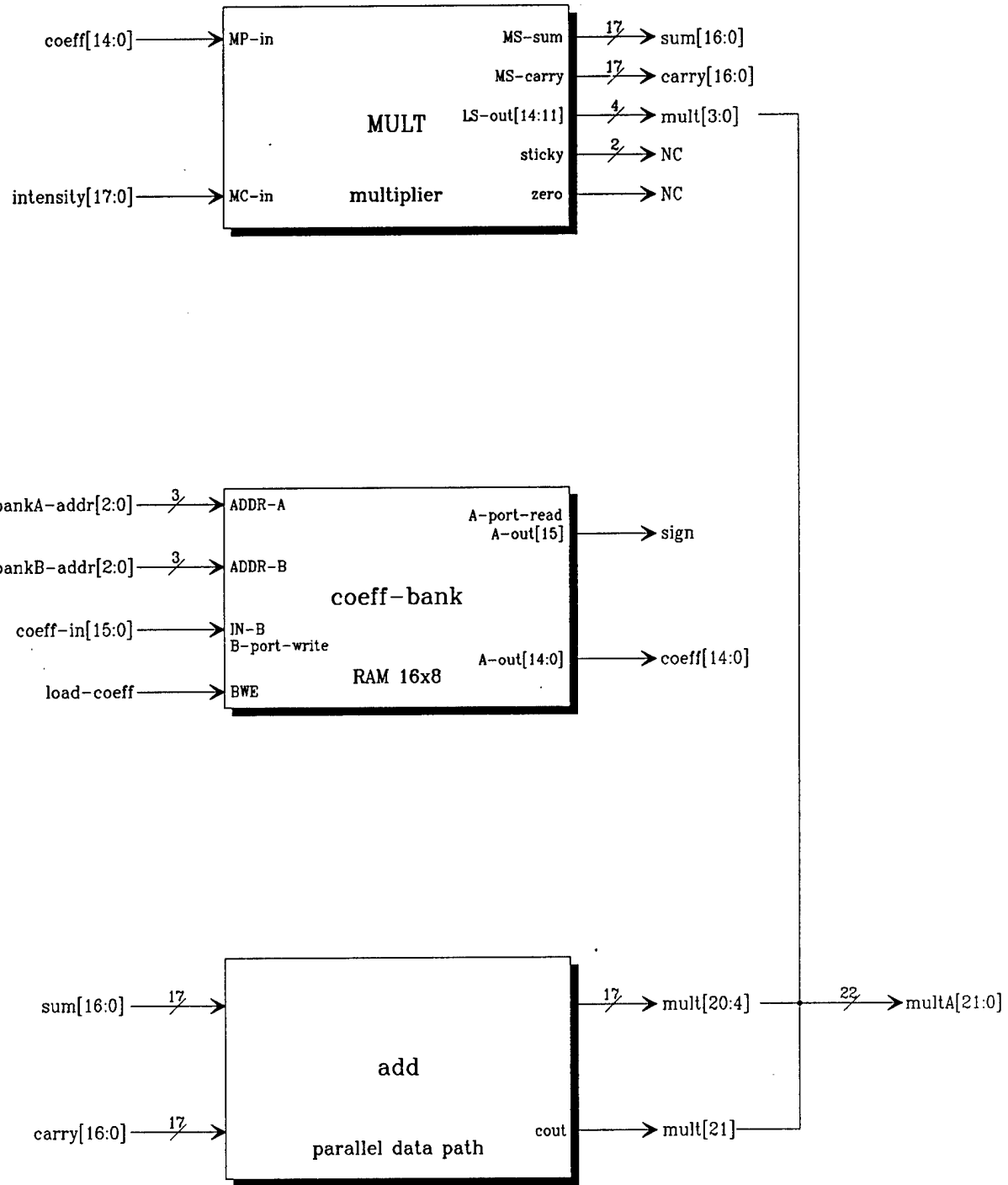


Fig. 3 /SFILTER/MULTA

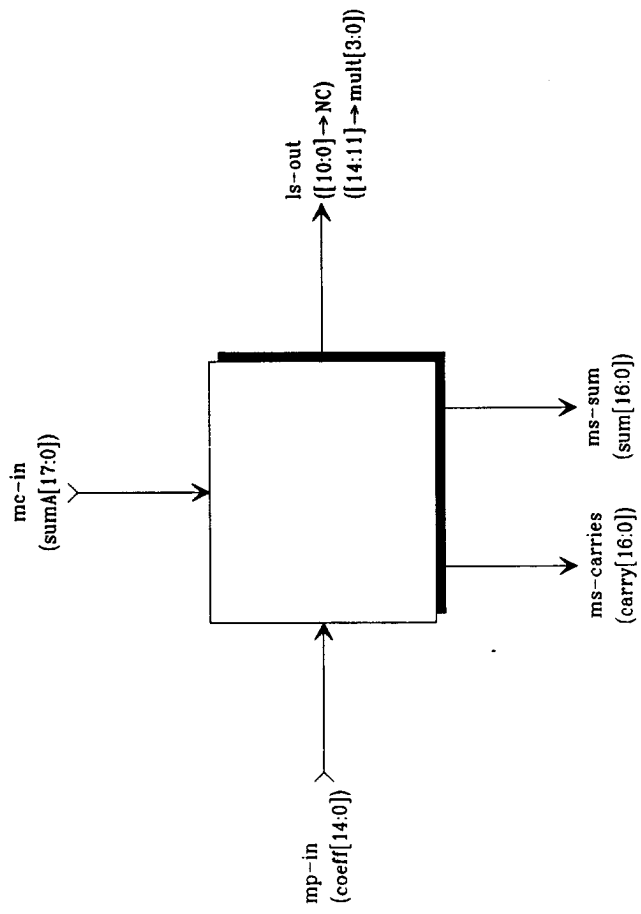


Fig 3A sfilter/multiA/mult

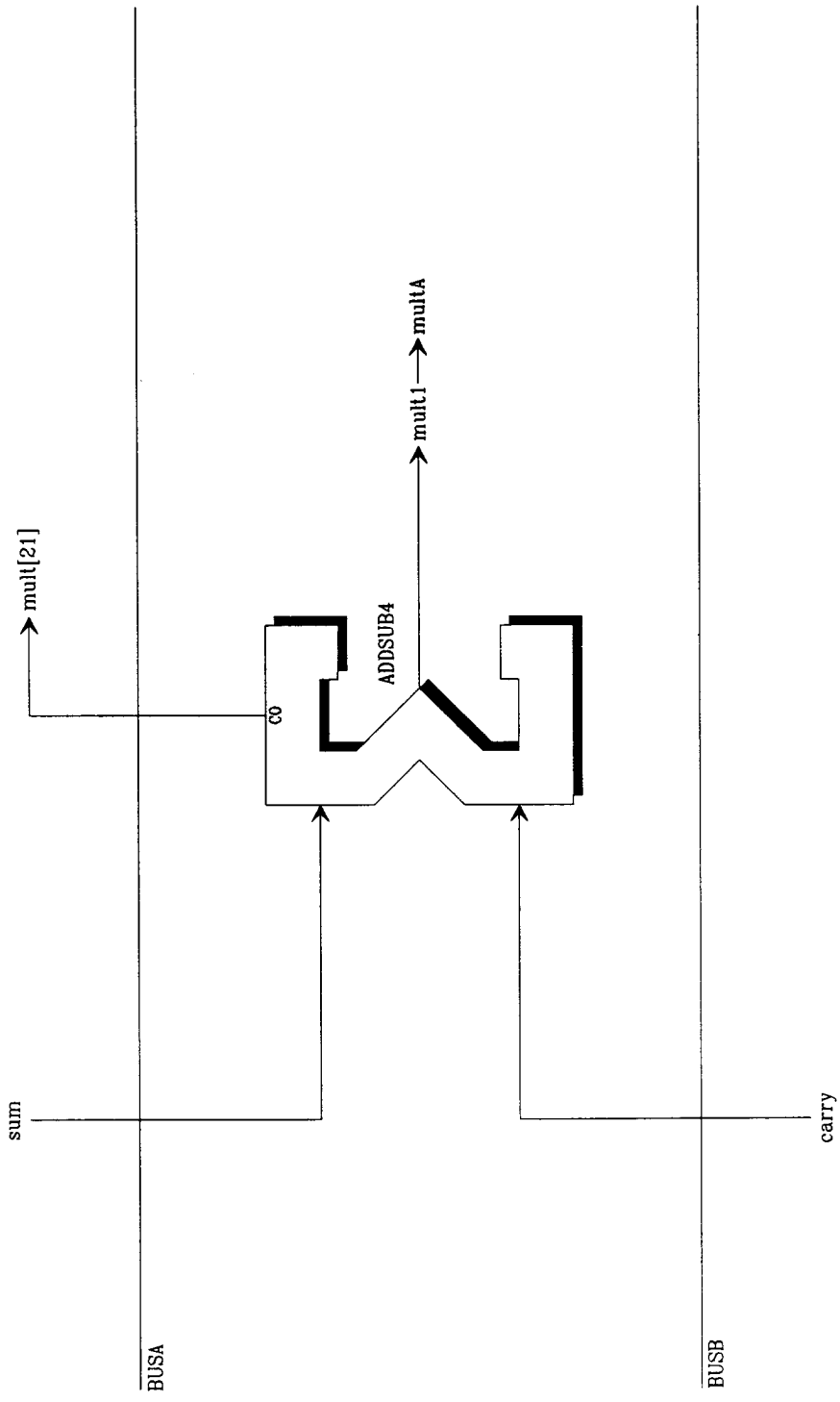


Fig. 26 /SFILTER/multA/add

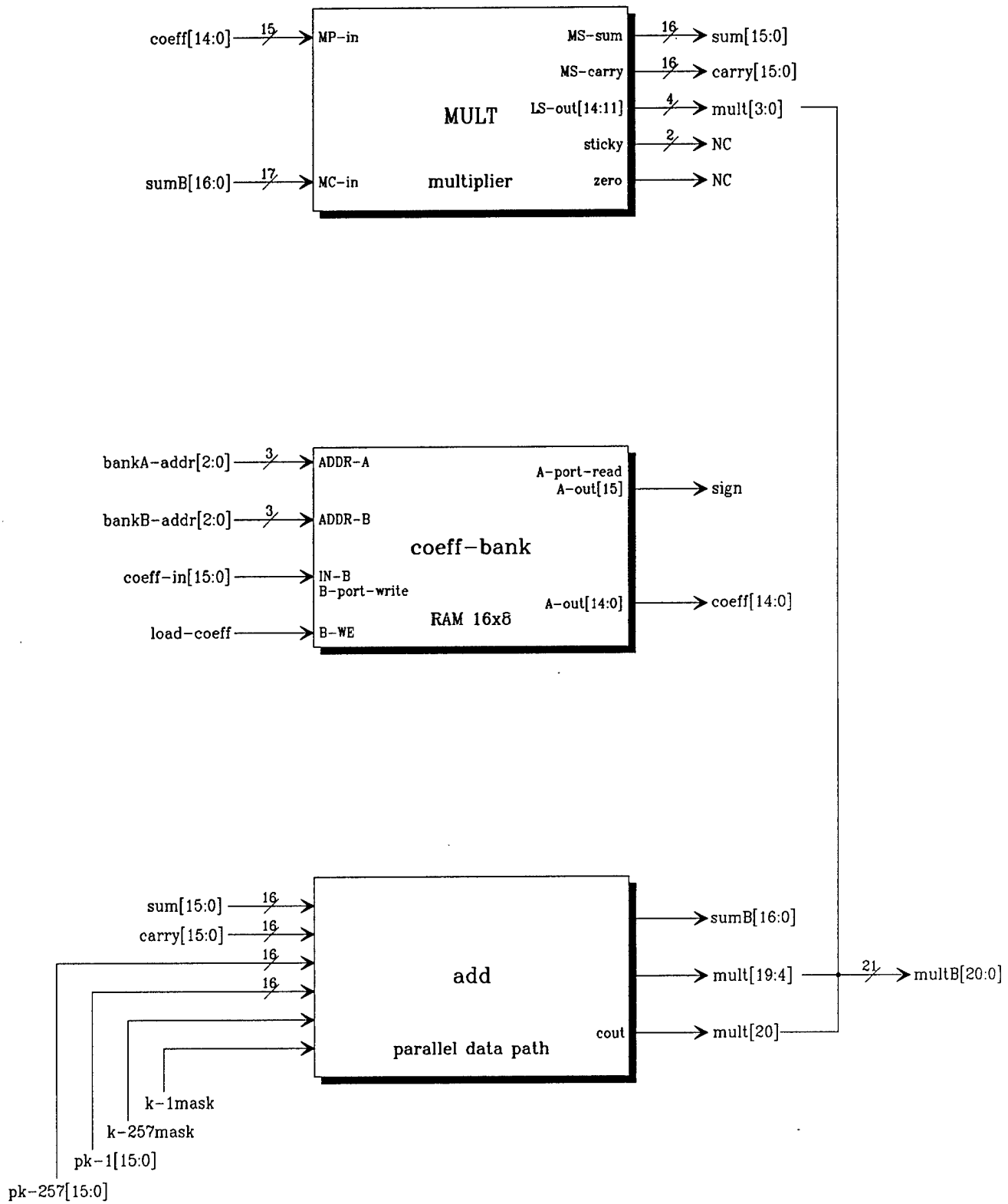


Fig. 4 /SFILTER/MULTB

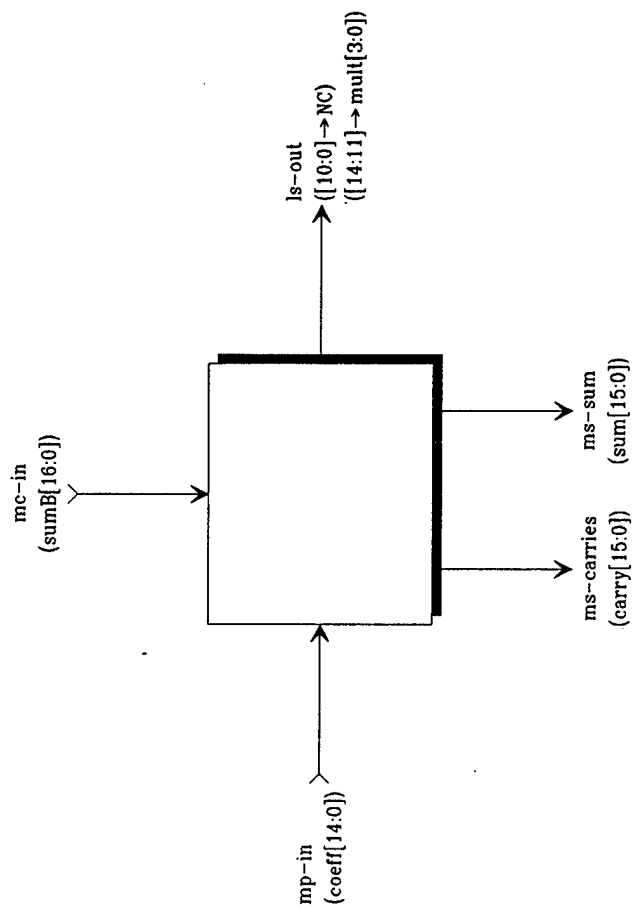


Fig 41A filter/multB/mult

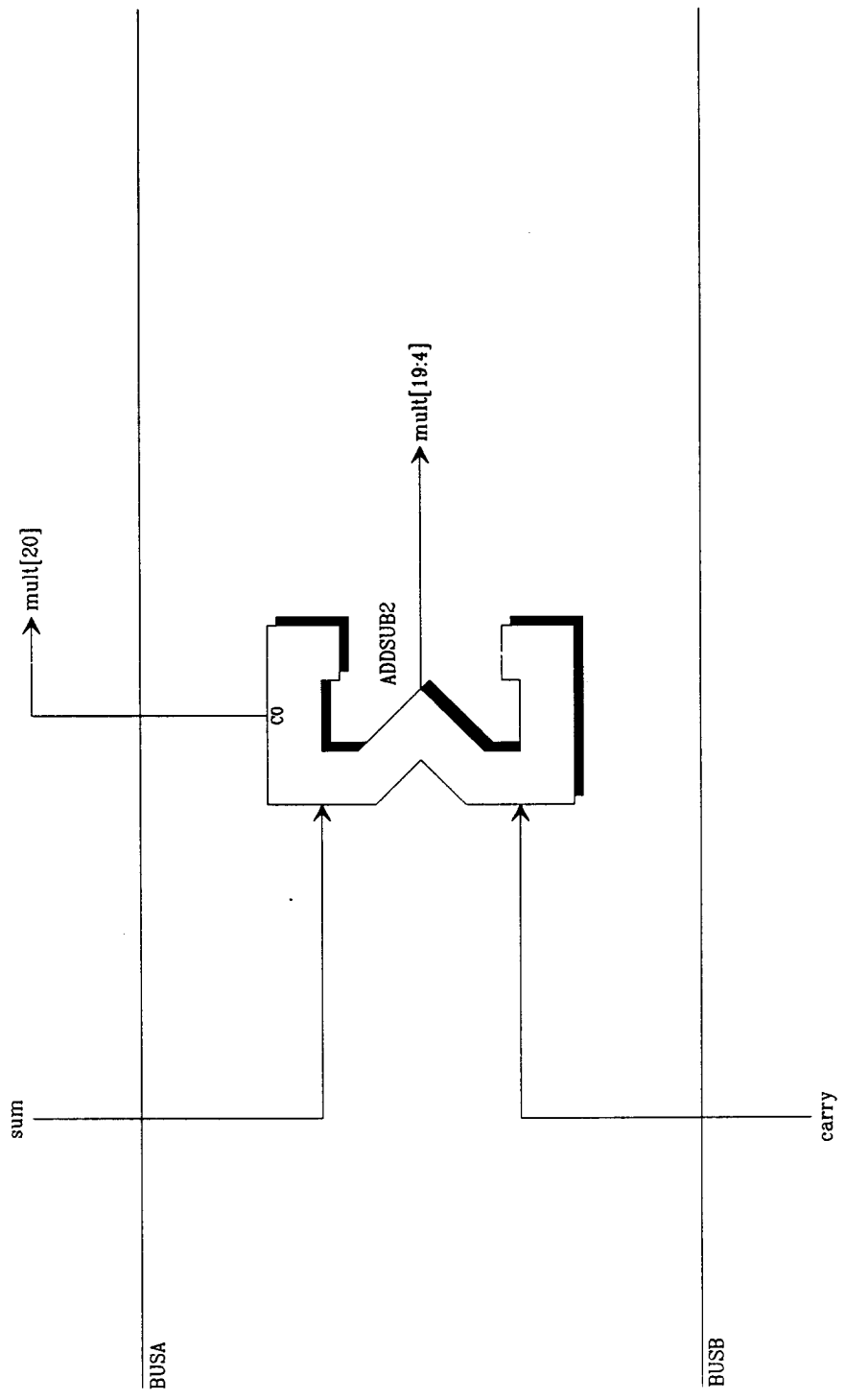


Fig 4B /SFILTER/multB/add

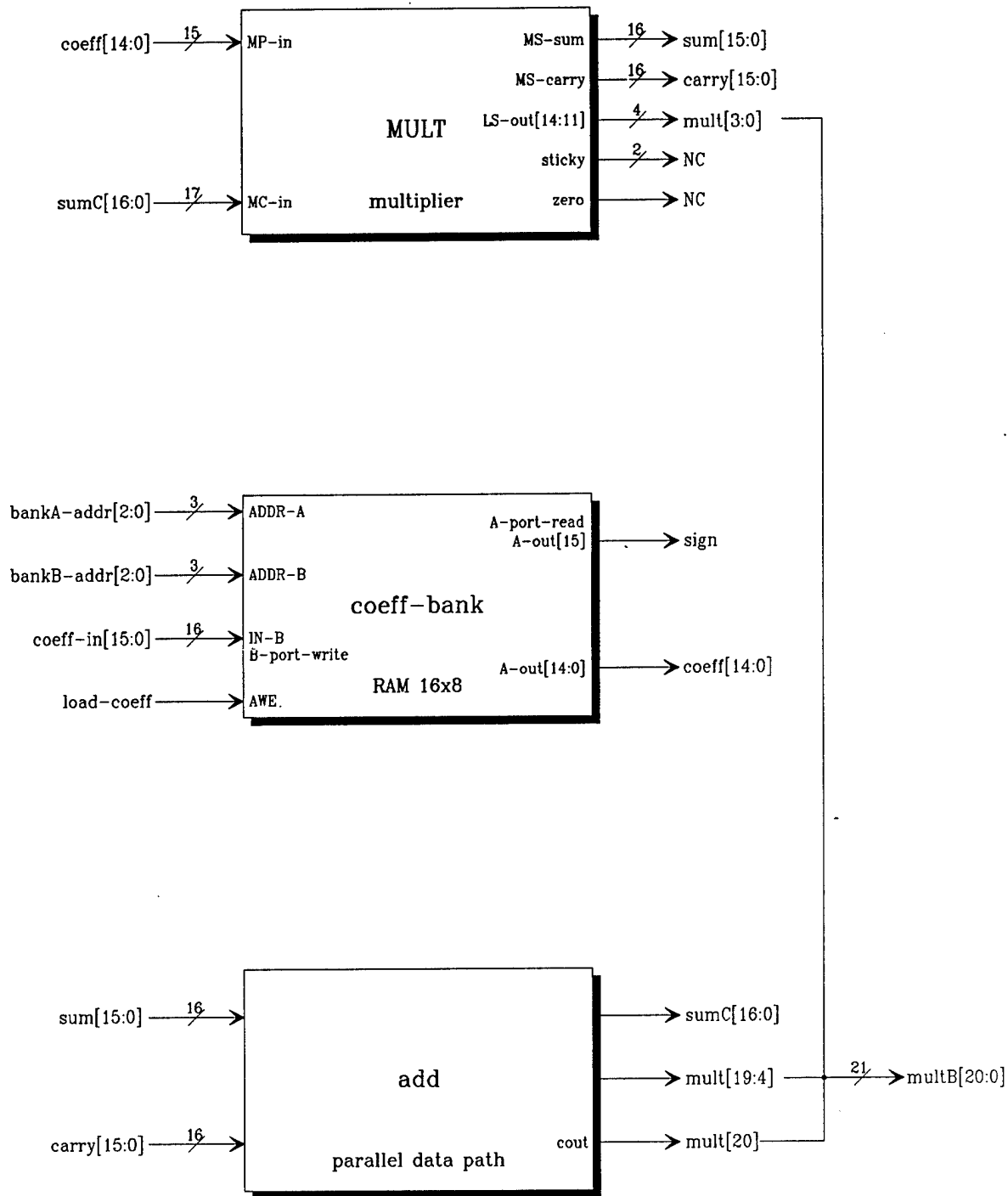


Fig. 5 /SFILTER/MULTC

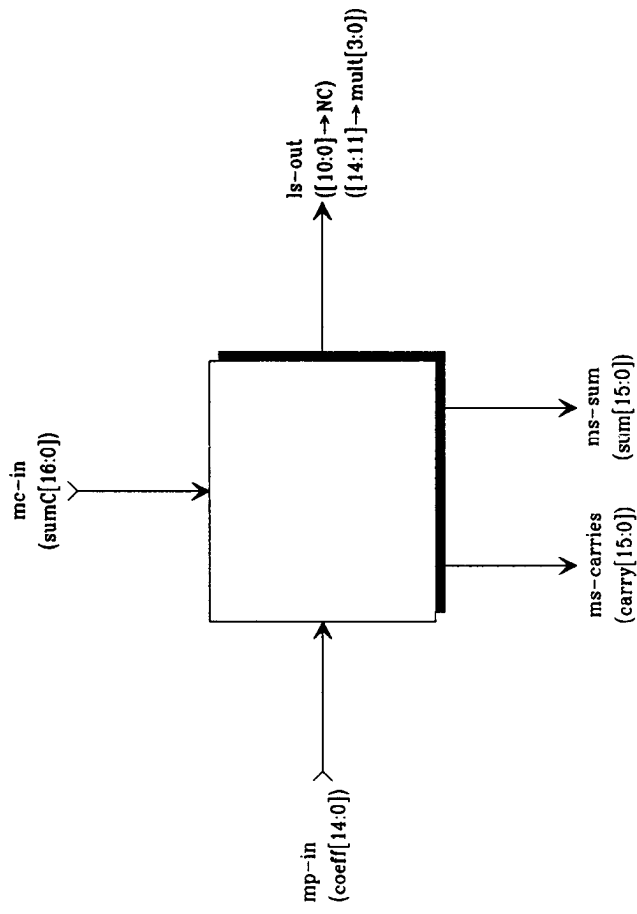


Fig 5A sfilter/multC/mult

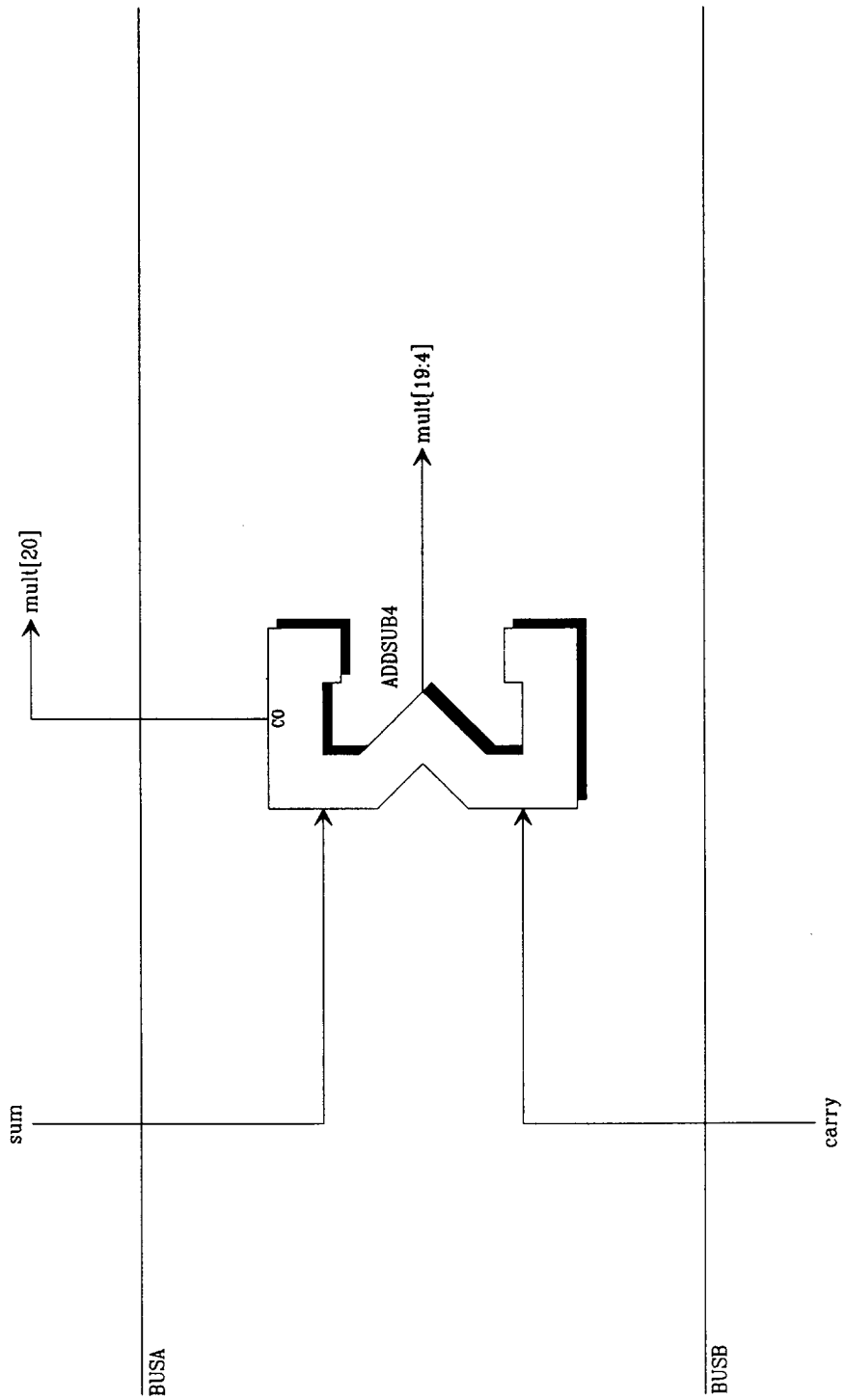


Fig 58 /SFILTER/multC/add

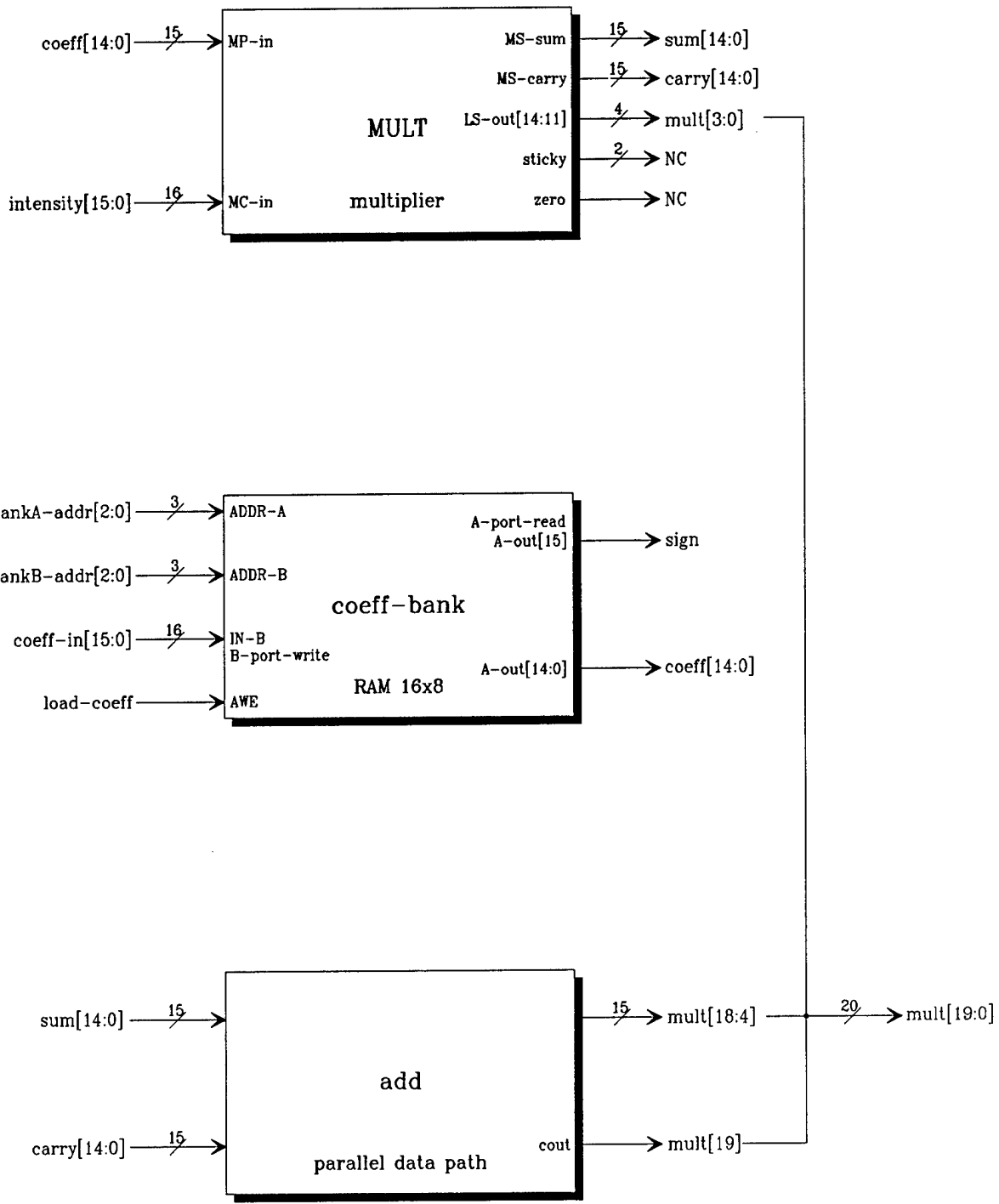


Fig. 6 /SFILTER/MULTD

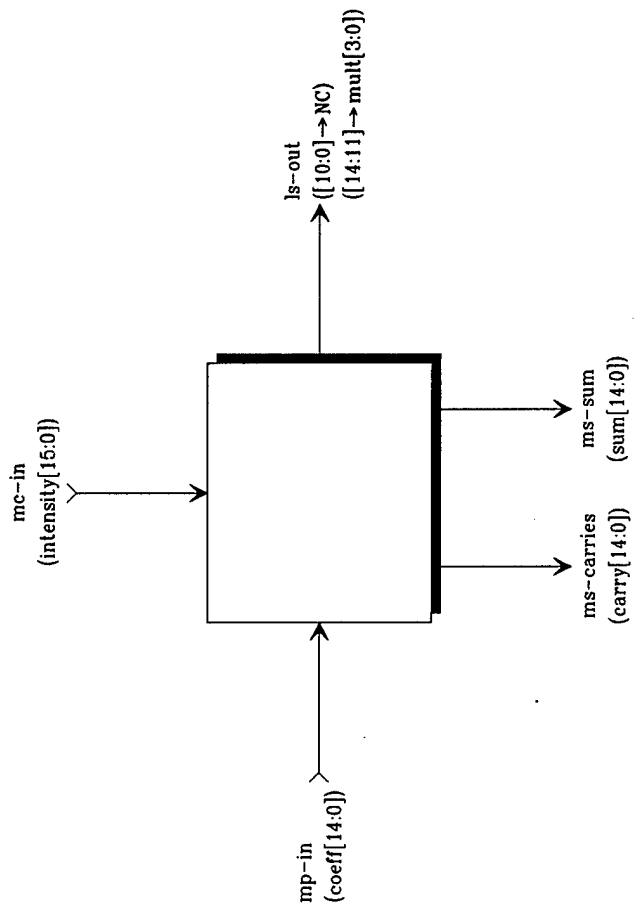


Fig 6A sfilter/multD/mult

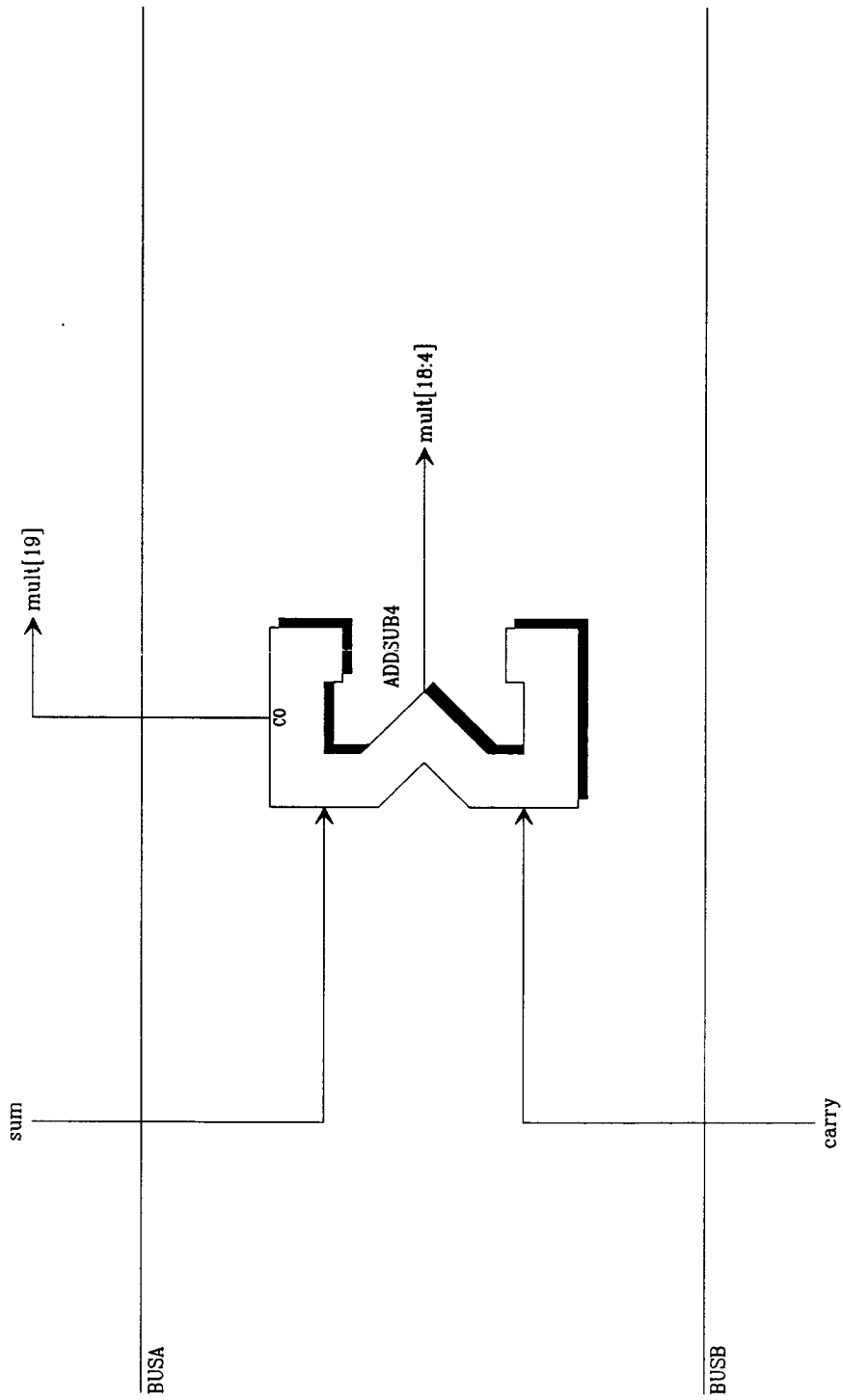


Fig 6B /SFILTER/multD/add

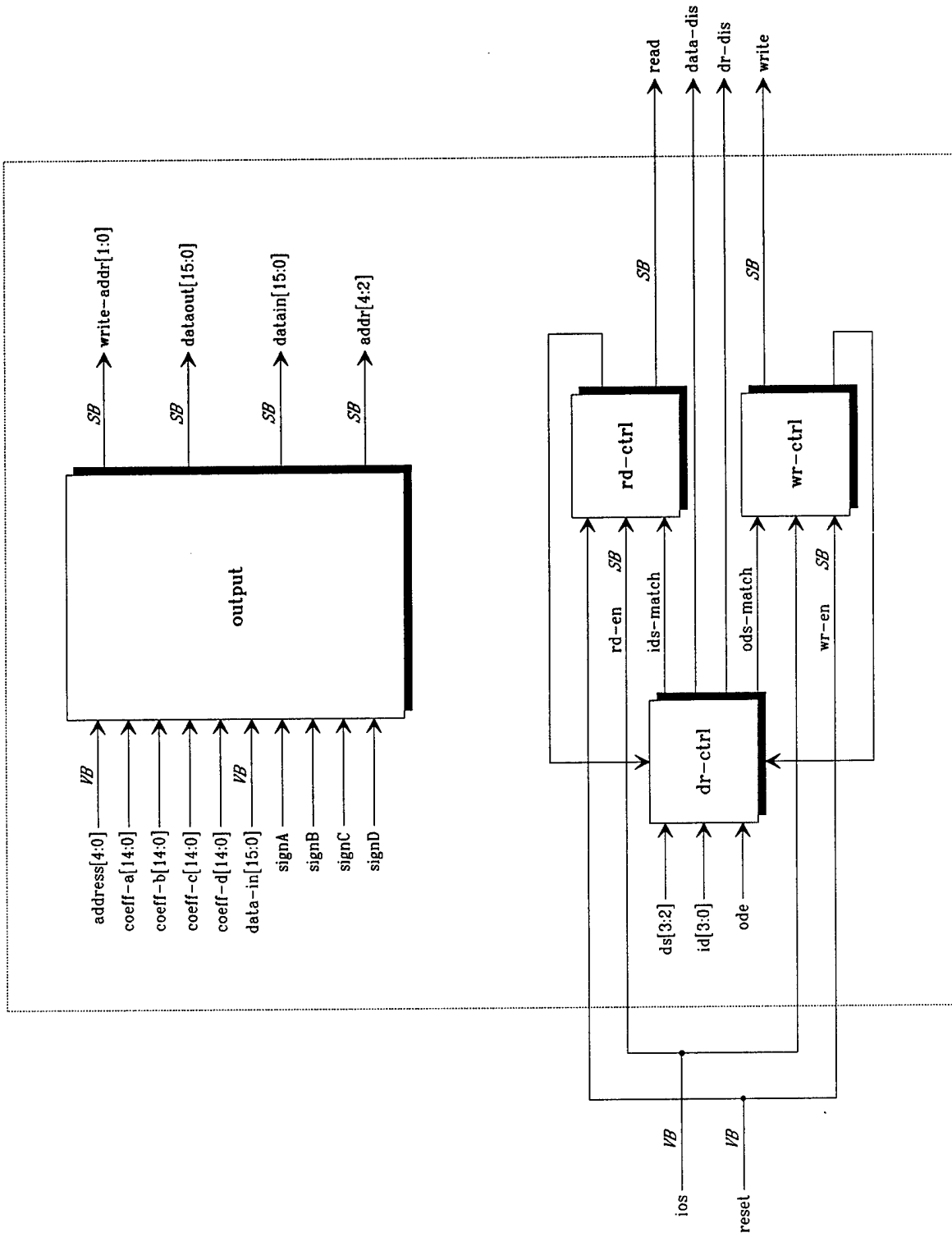


Fig. 8 /SFILTER/HOST-INTERFACE

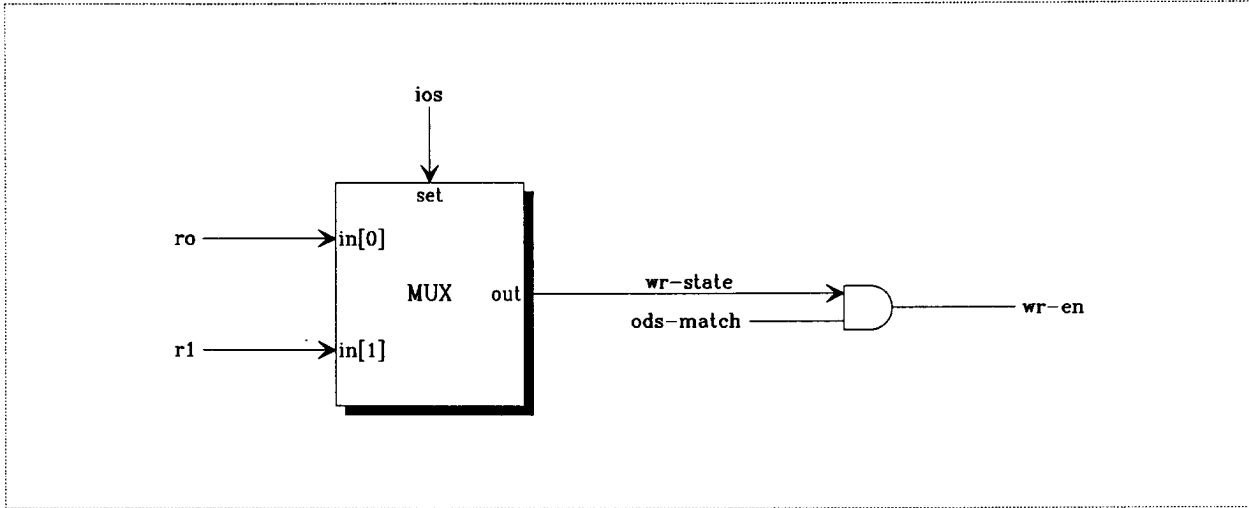
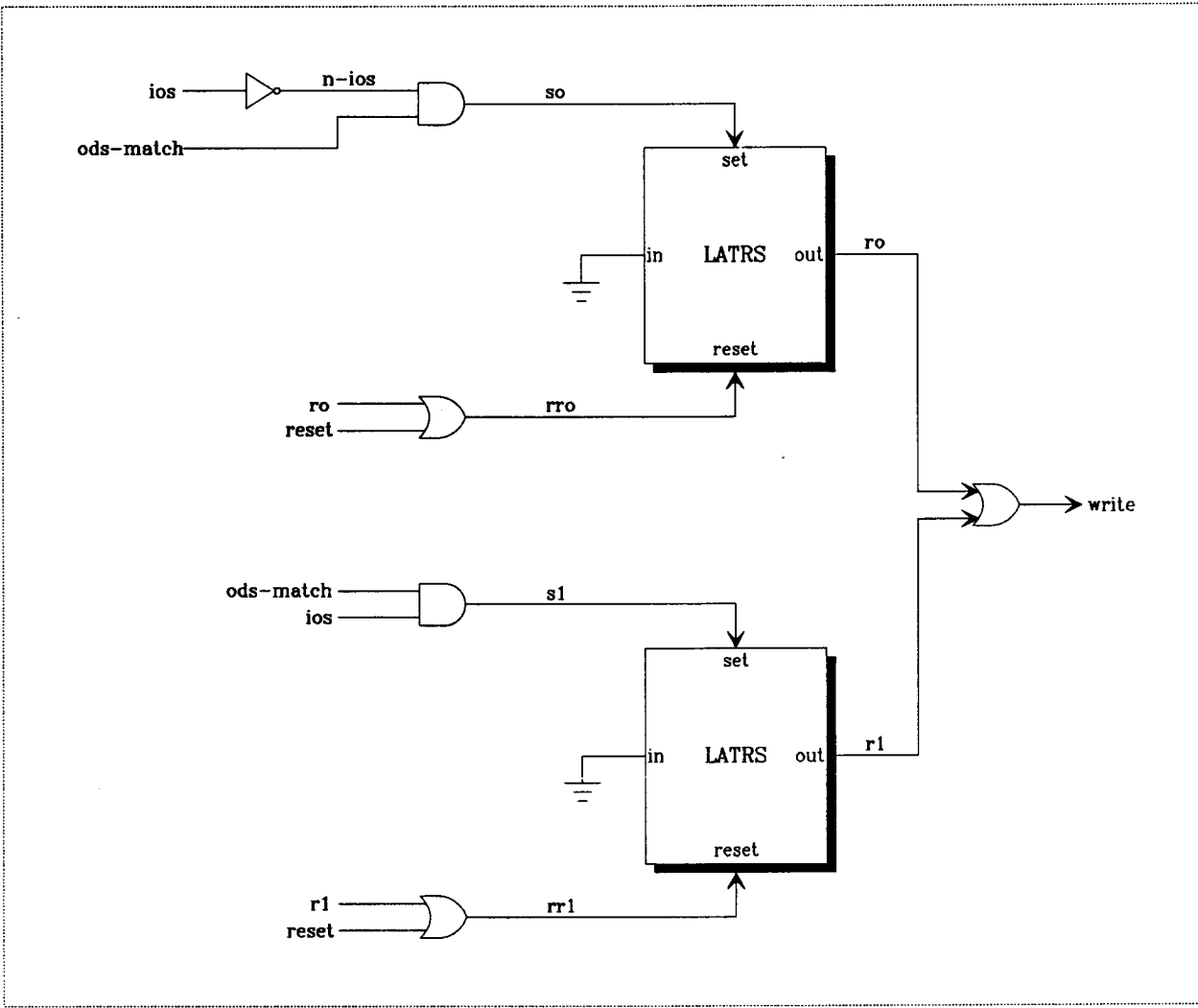


Fig 8A sfilter/host-interface/wr-ctrl

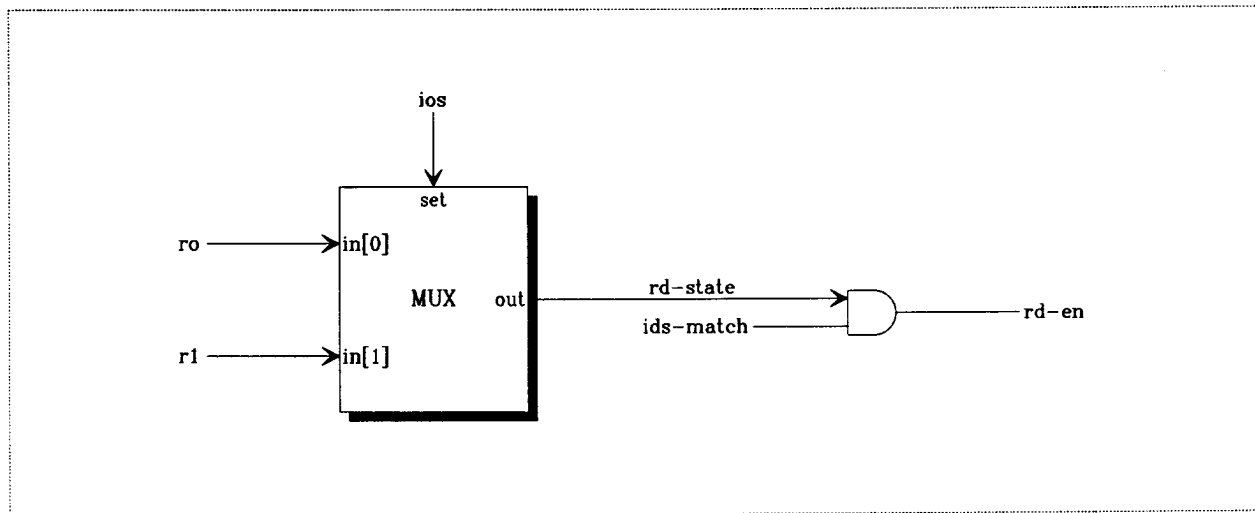
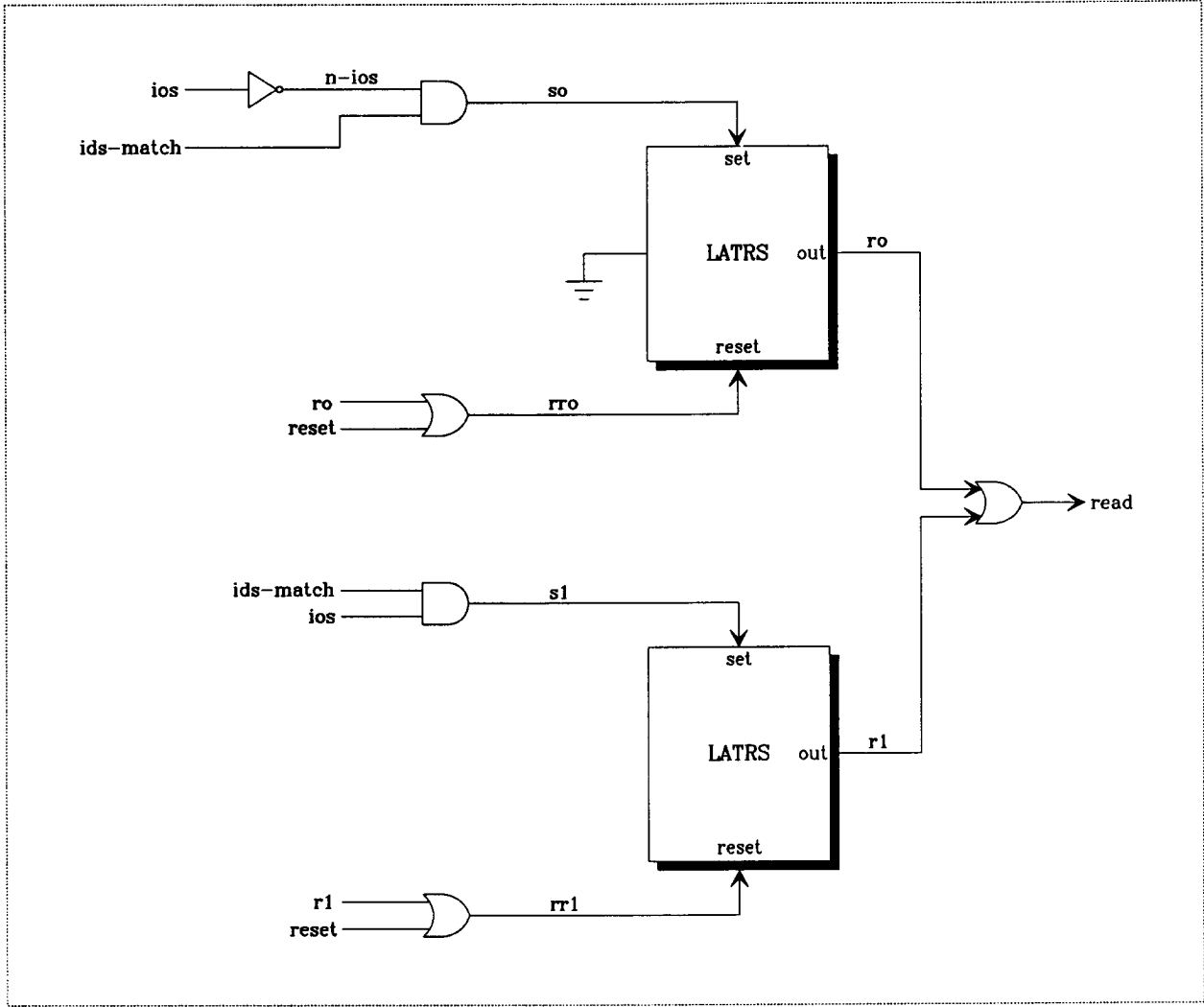


Fig 8B sfilter/host-interface/rd-ctrl

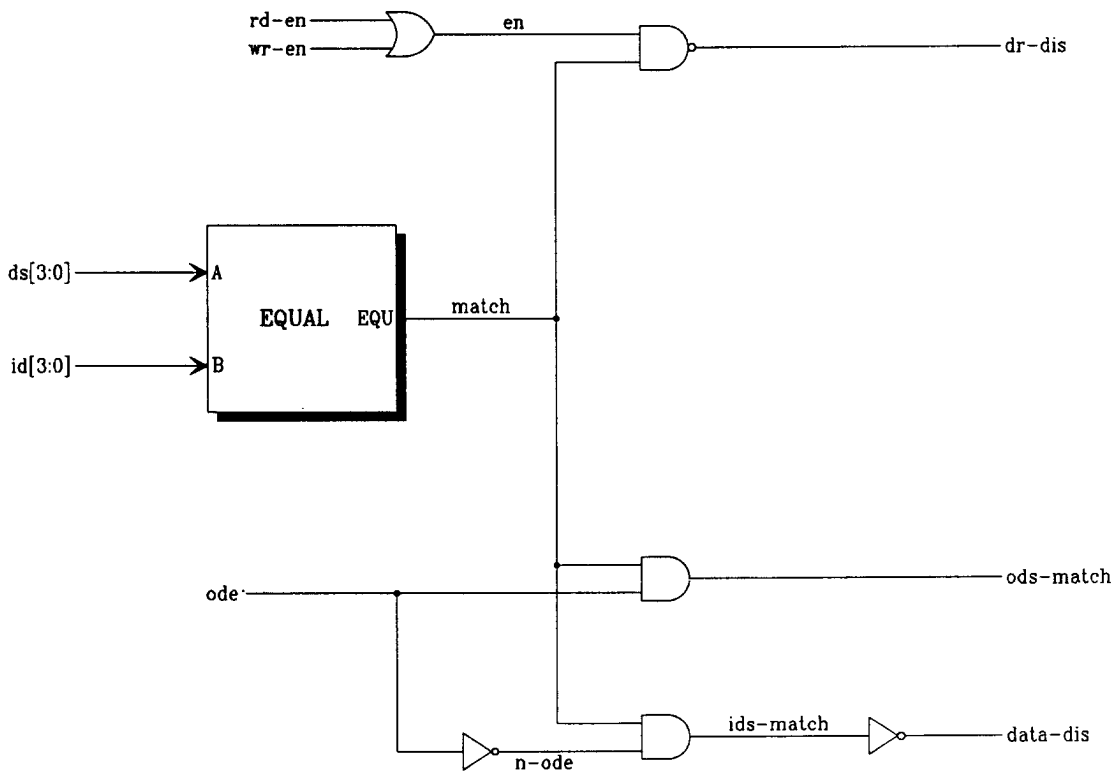


Fig 8C sfilter/host-interface/dr-ctrl

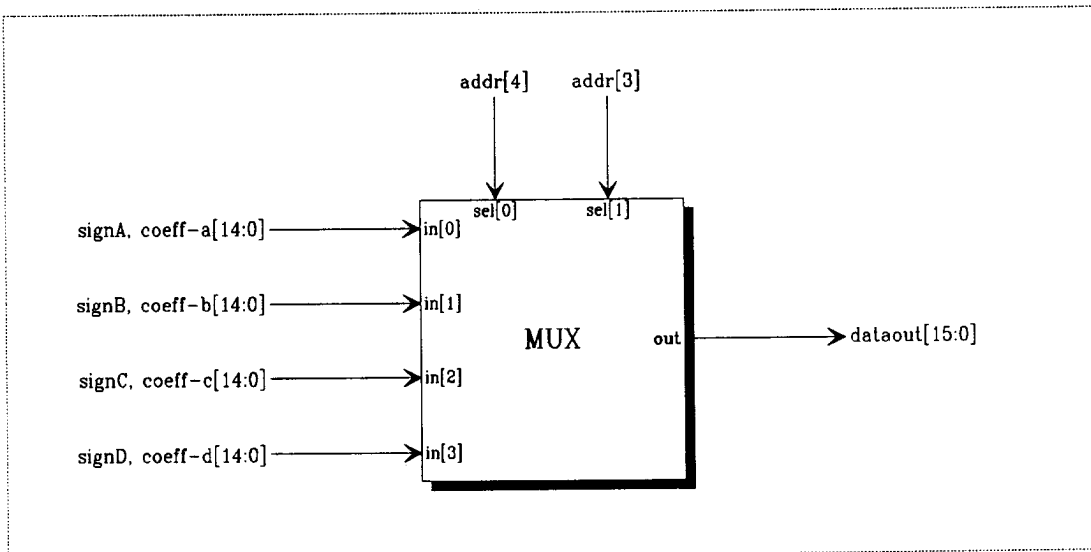
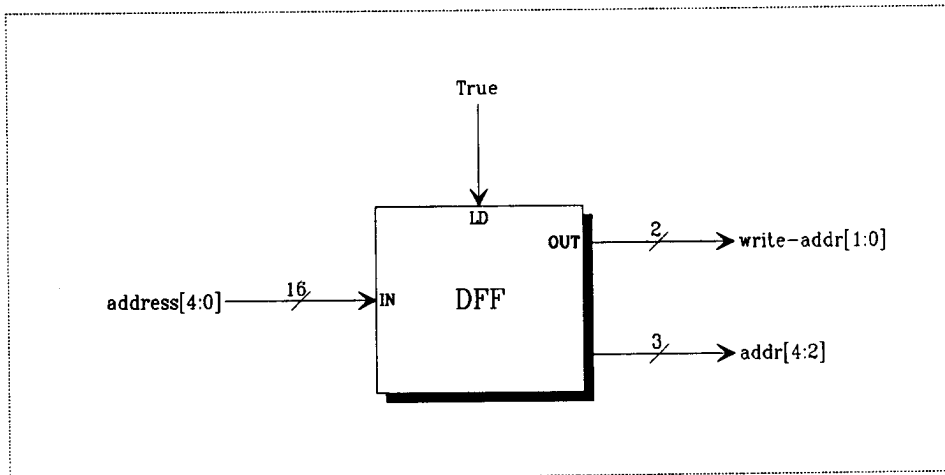
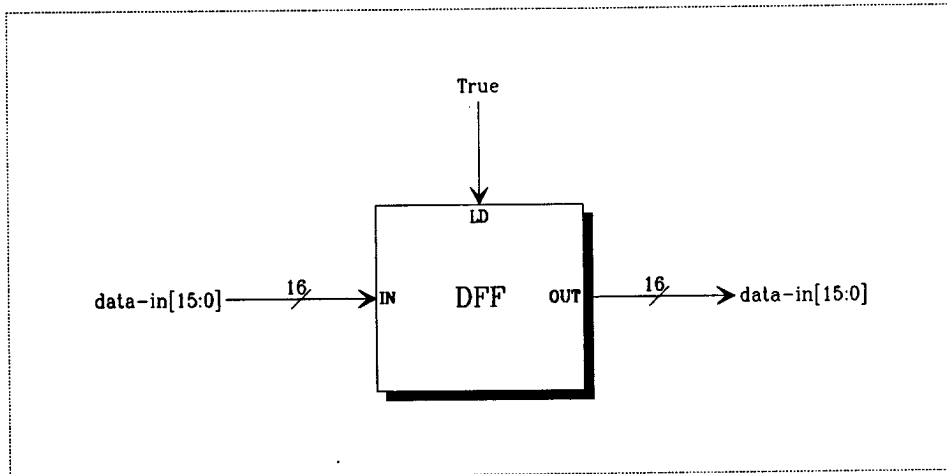


Fig 8D sfilter/host-interface/output

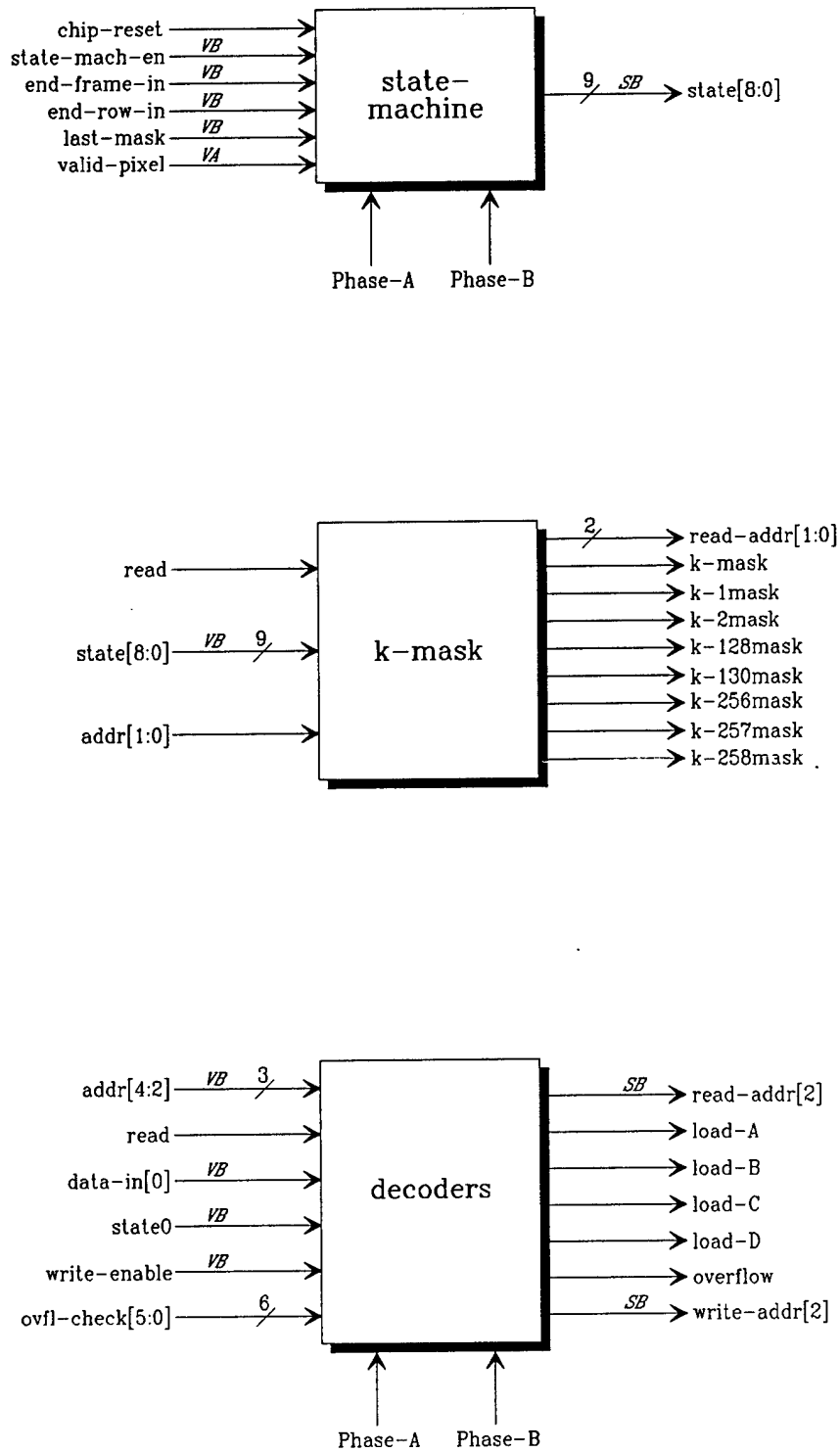
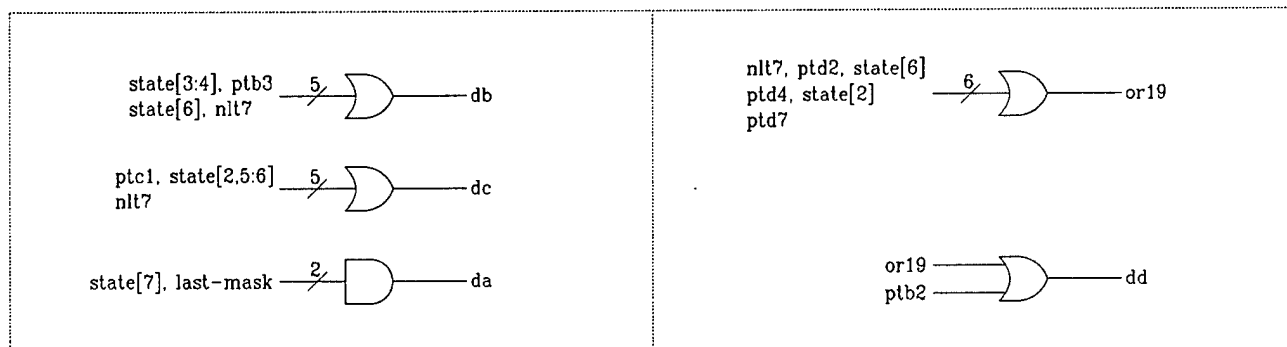
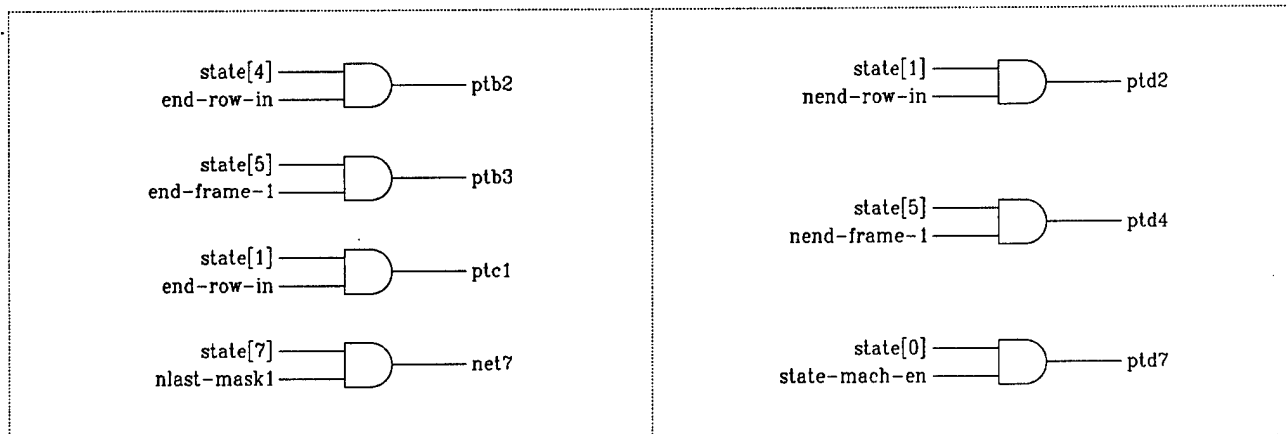
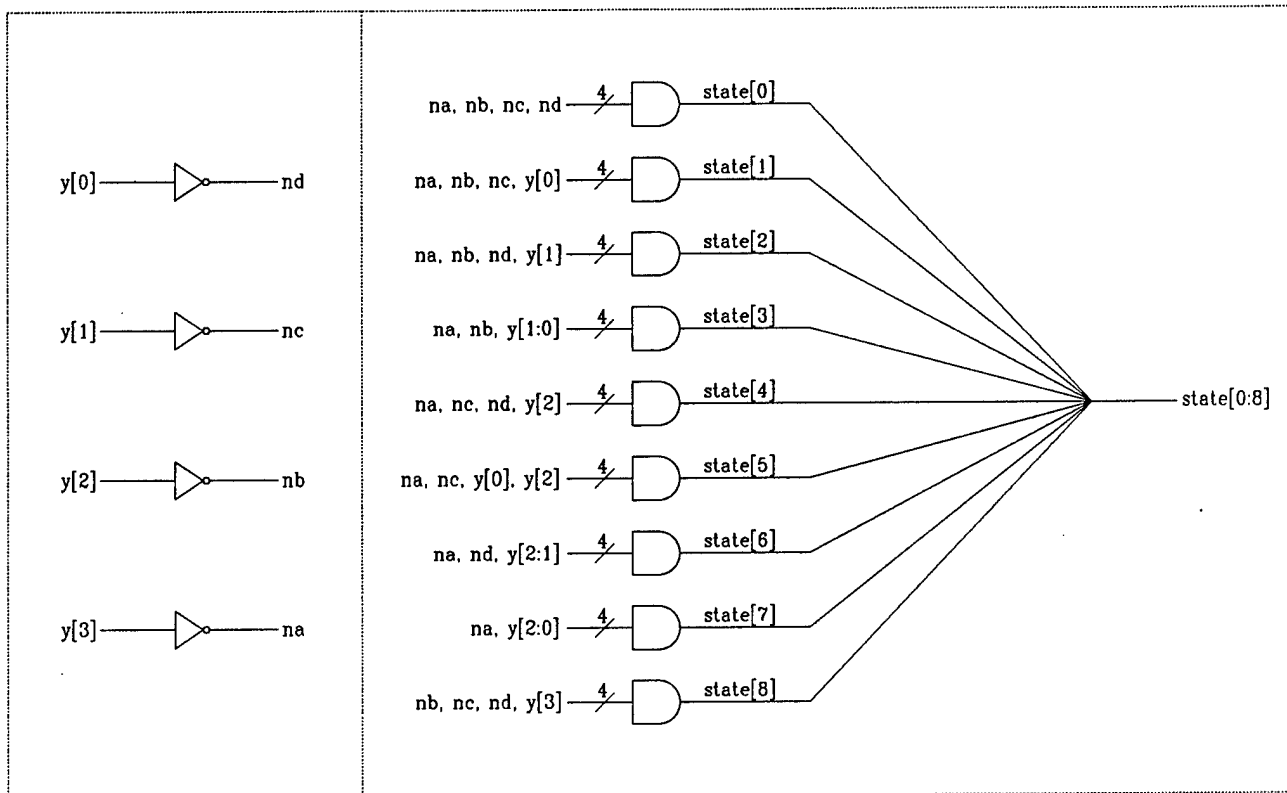
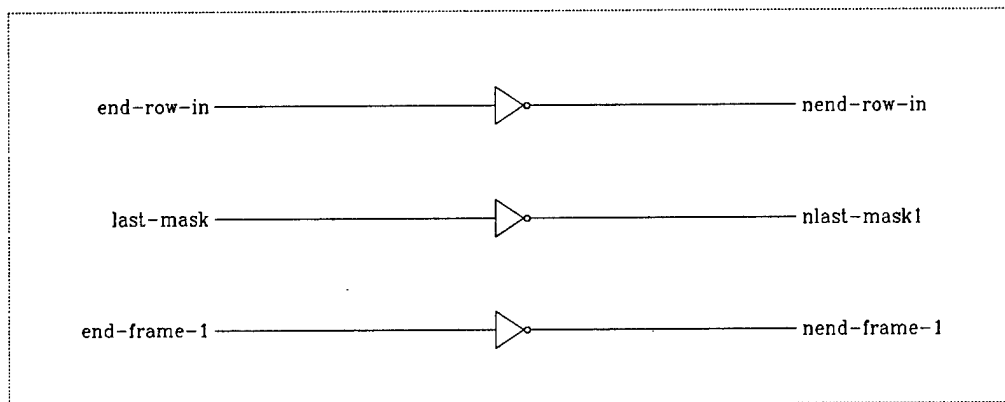
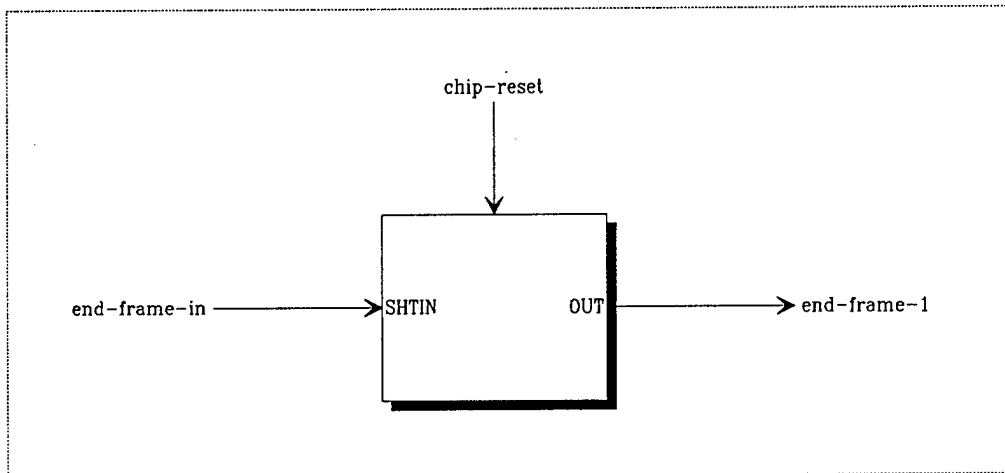
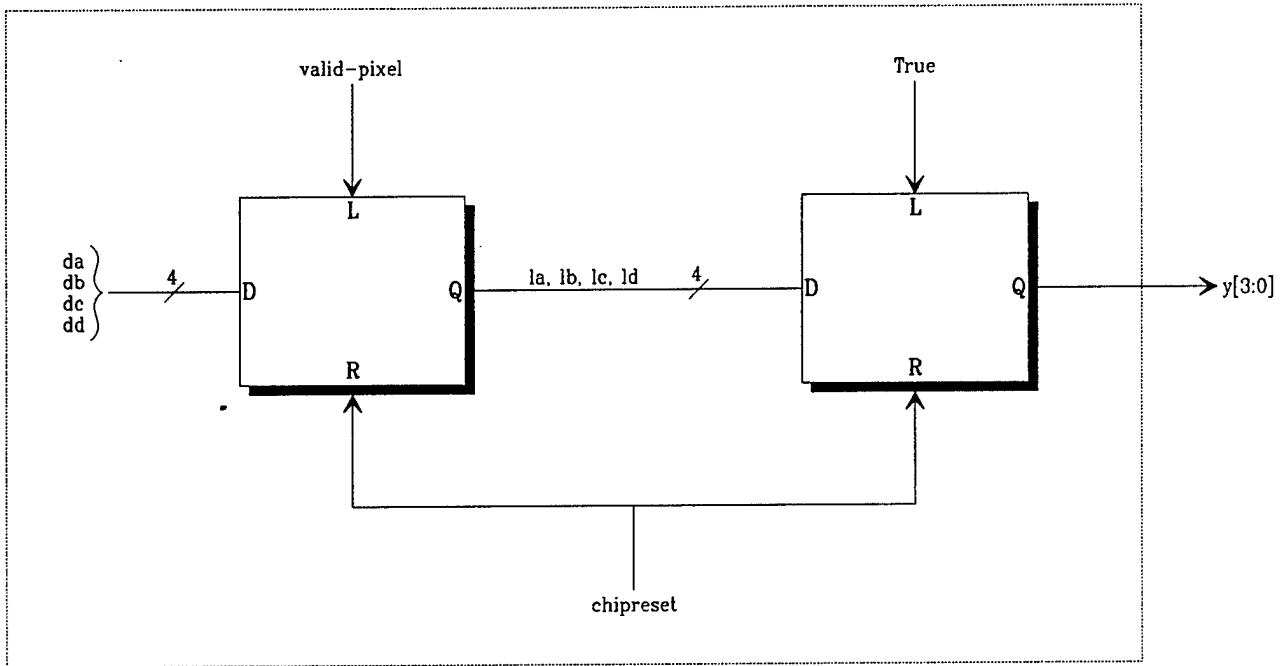
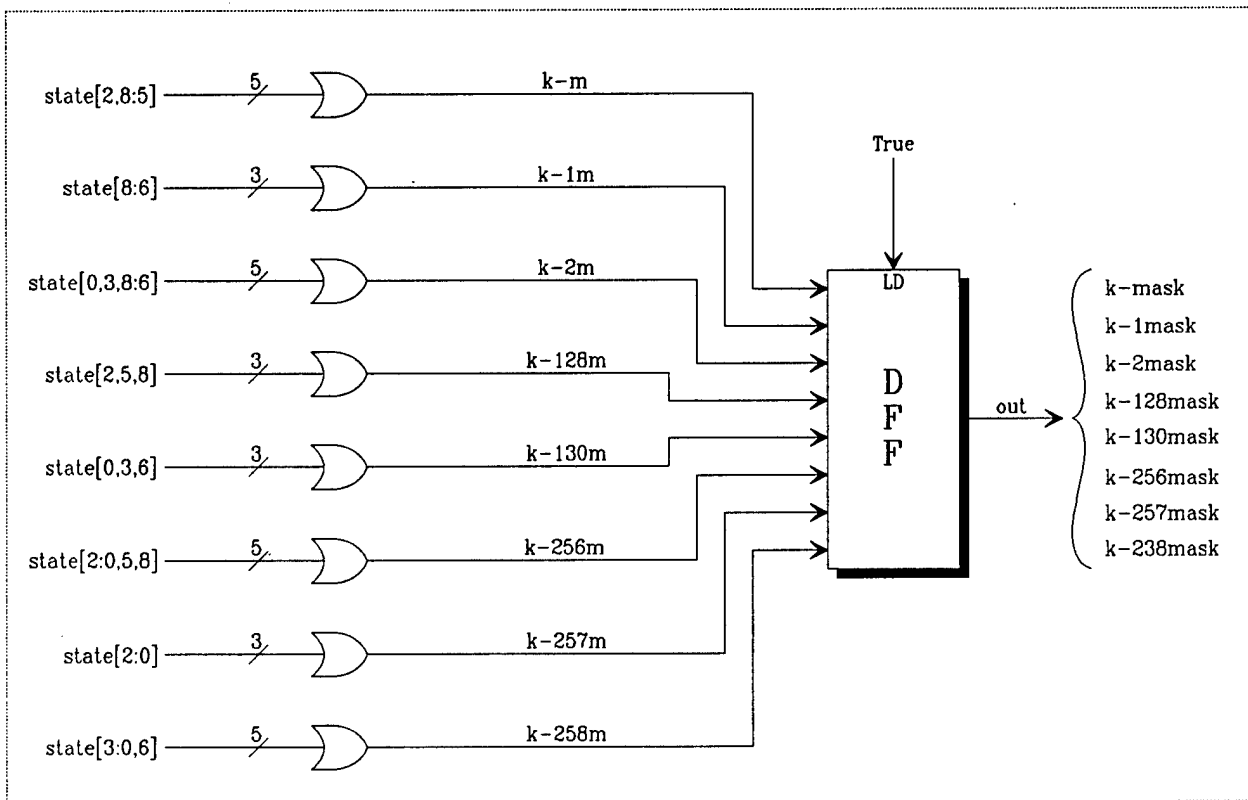
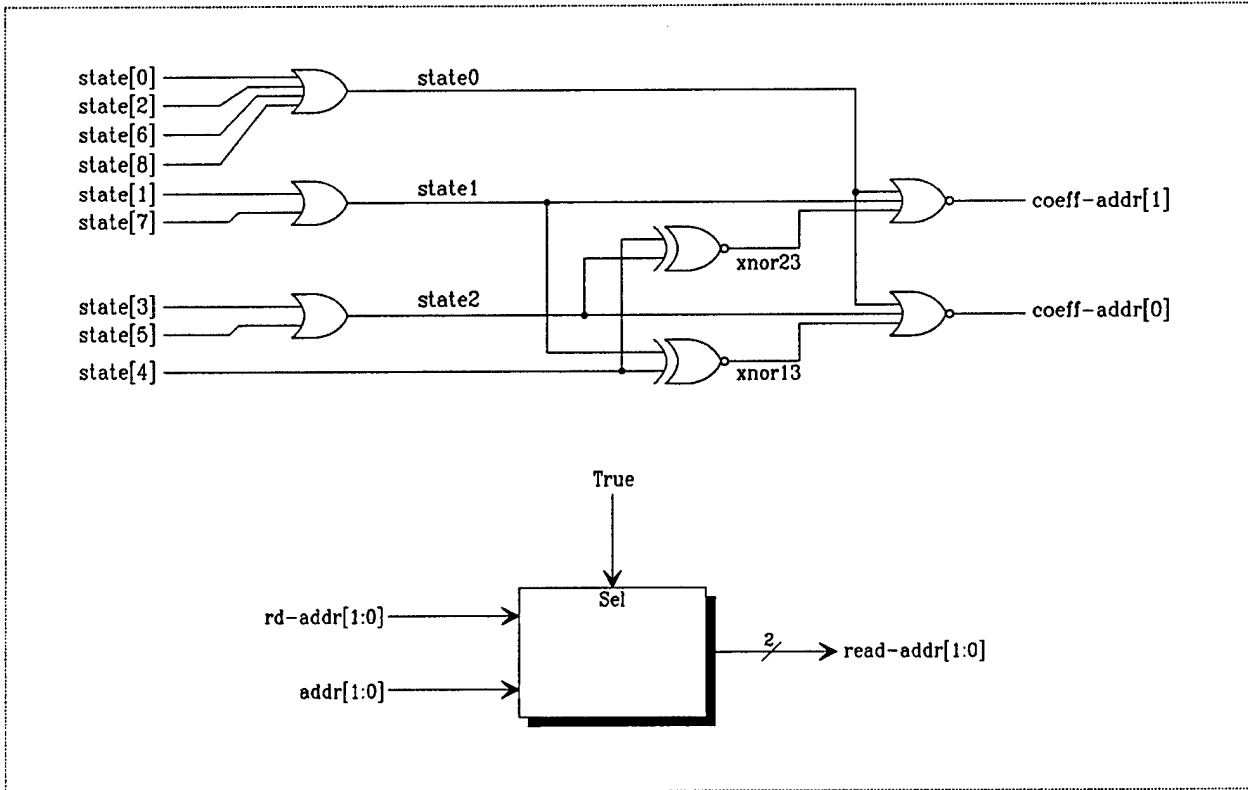


Fig. 9 /SFILTER/CONTROL



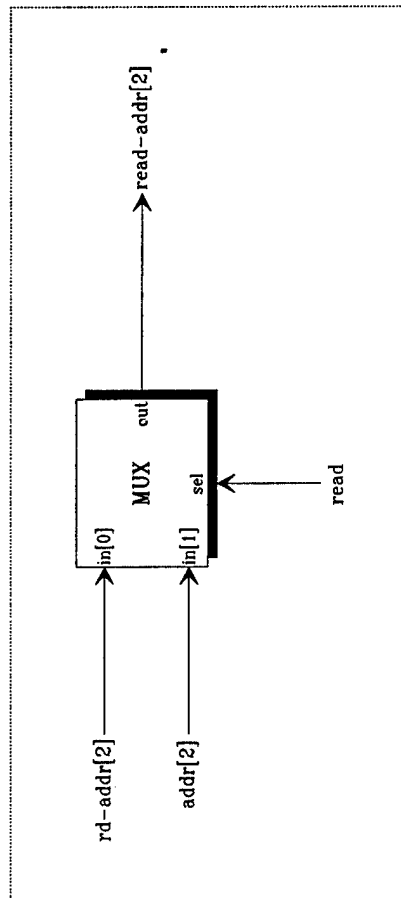
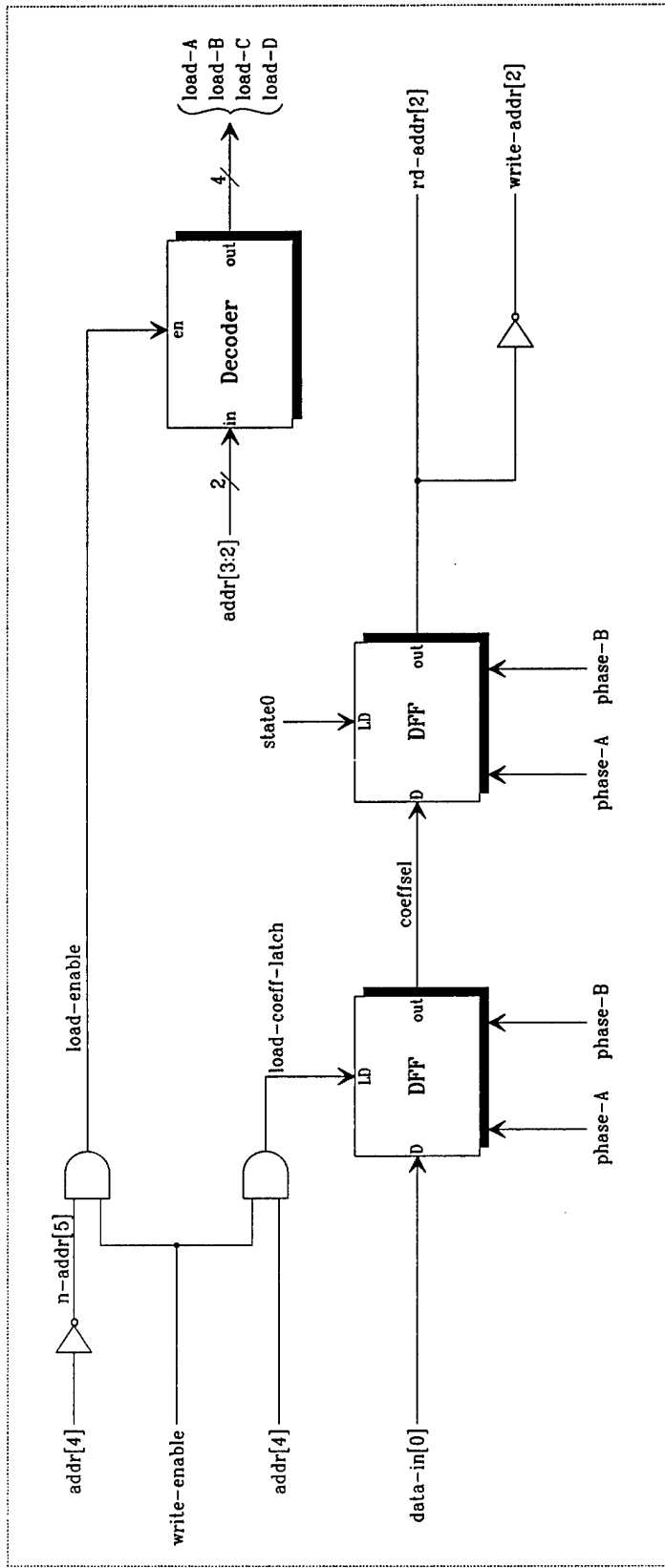


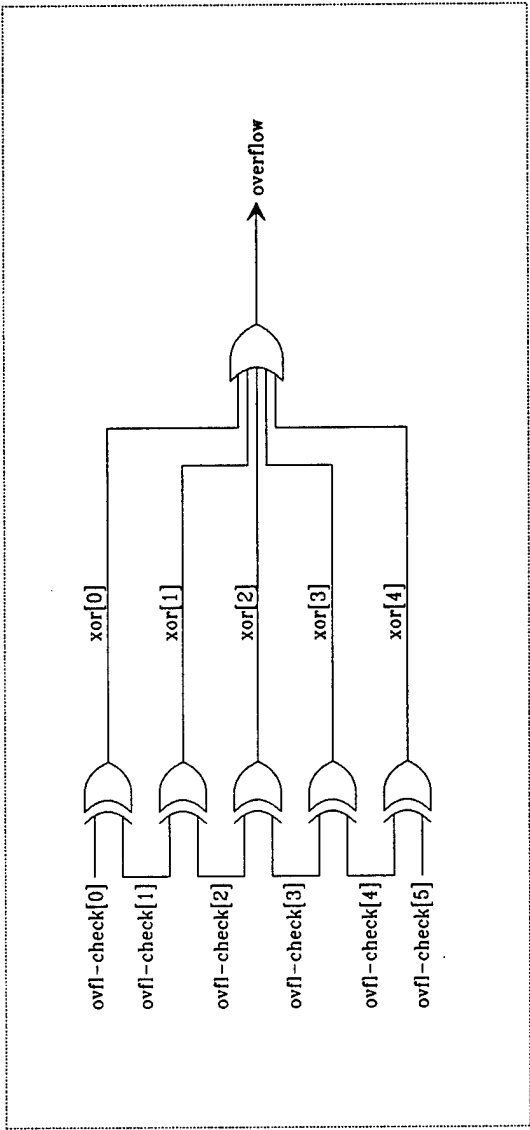
sfilter/control/state-machine



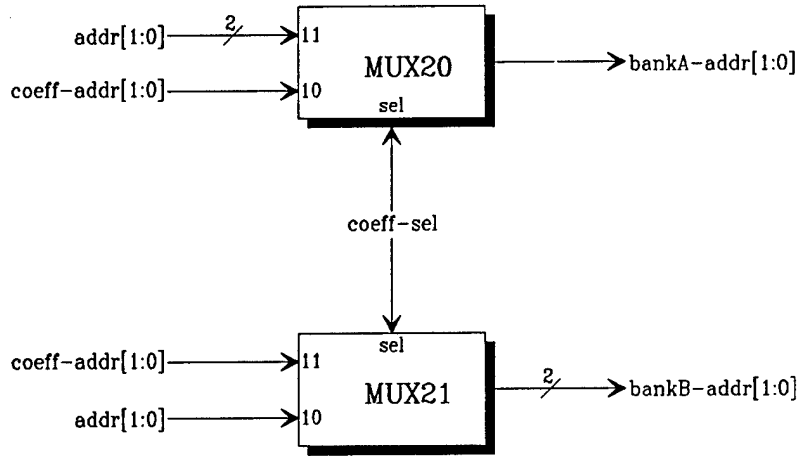
sfilter/control/k-mask

April 28, 1989

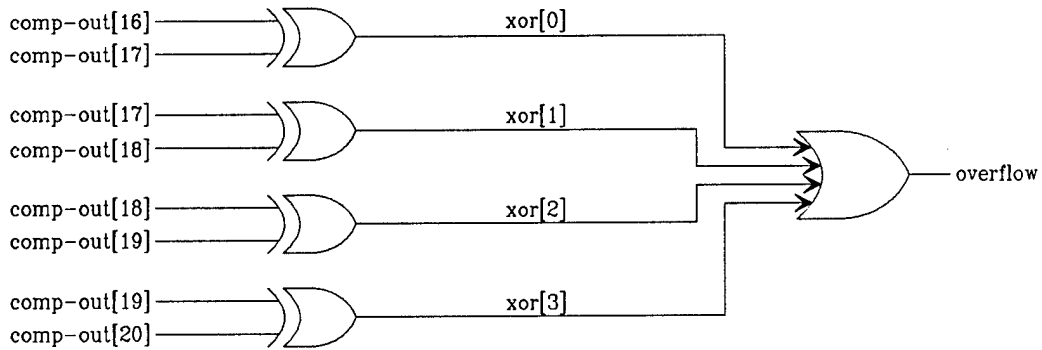
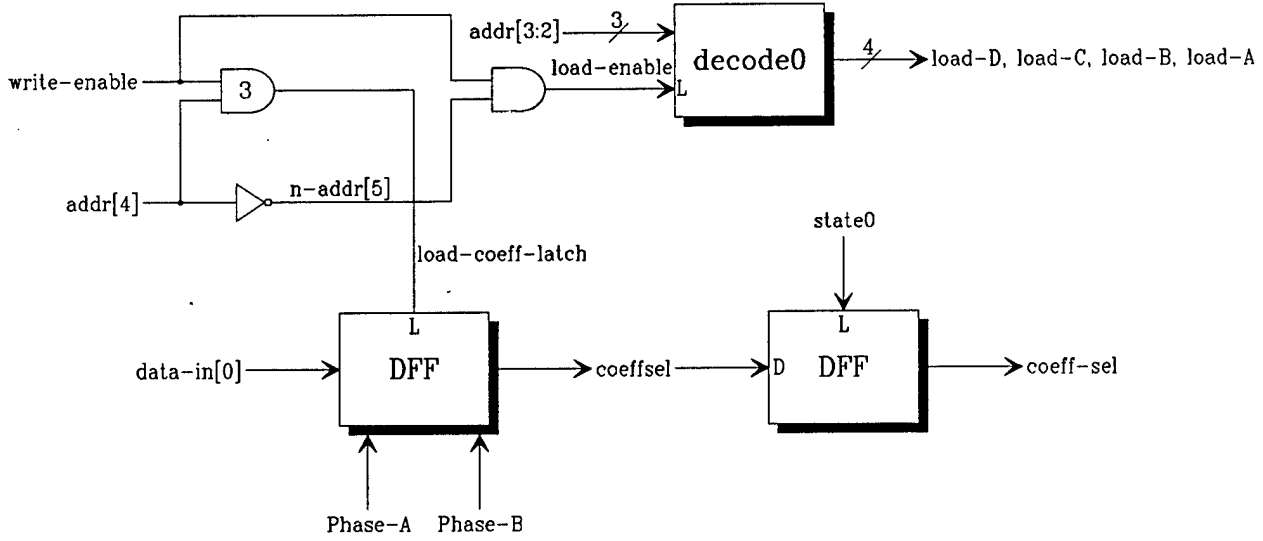


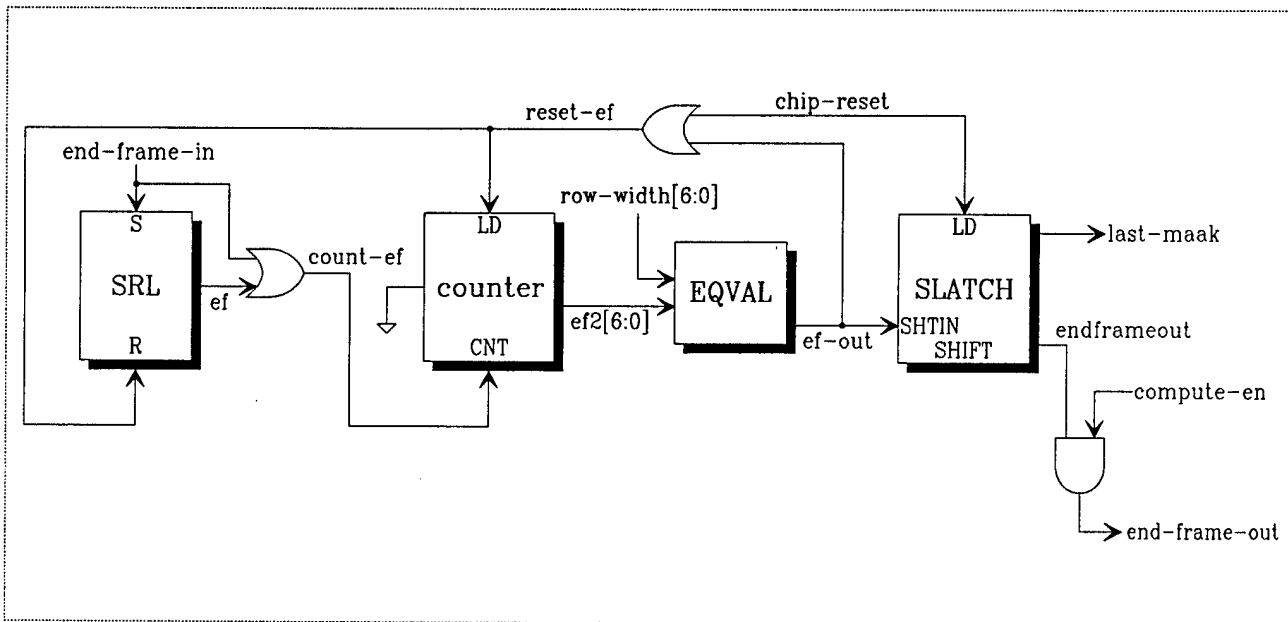
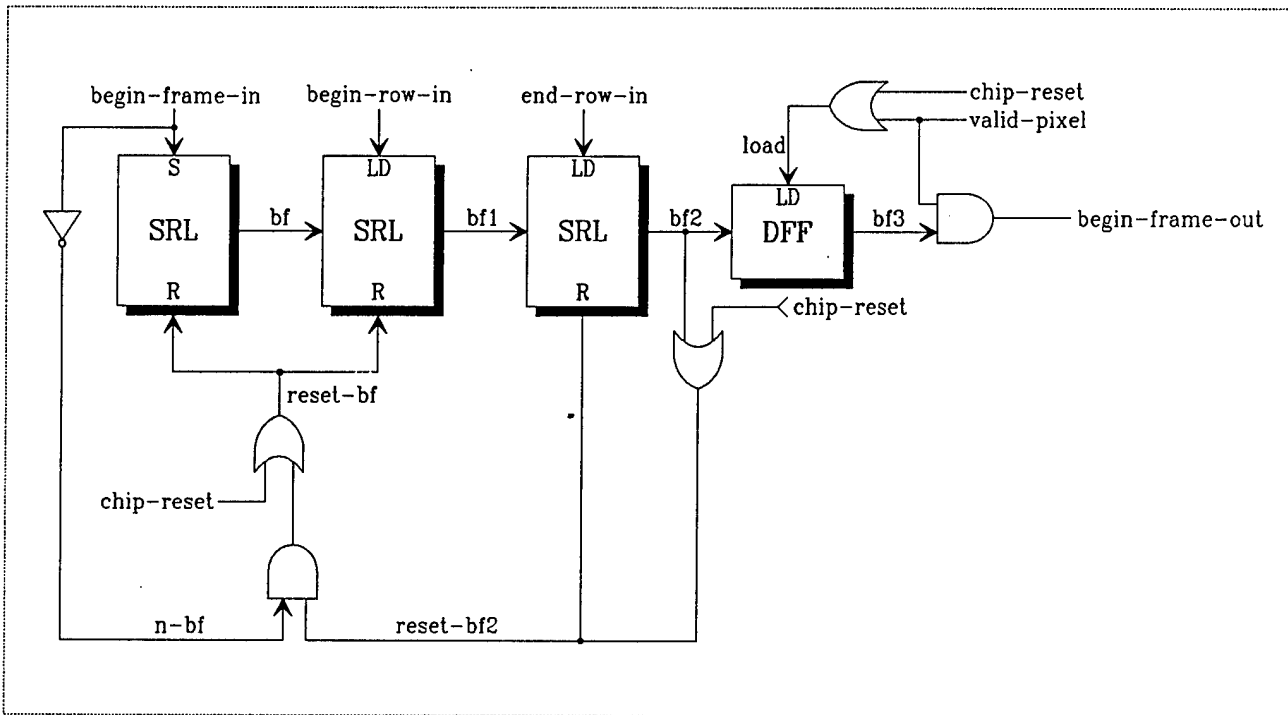


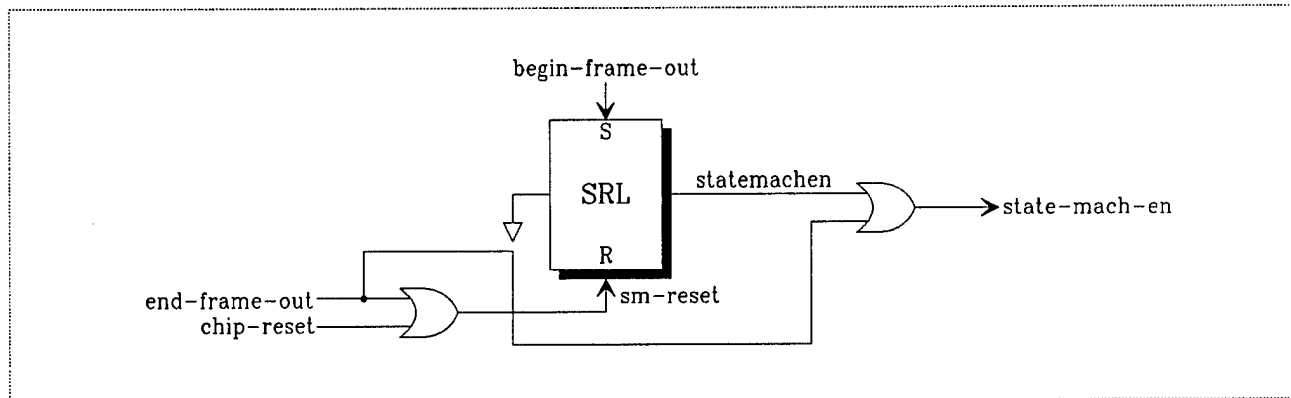
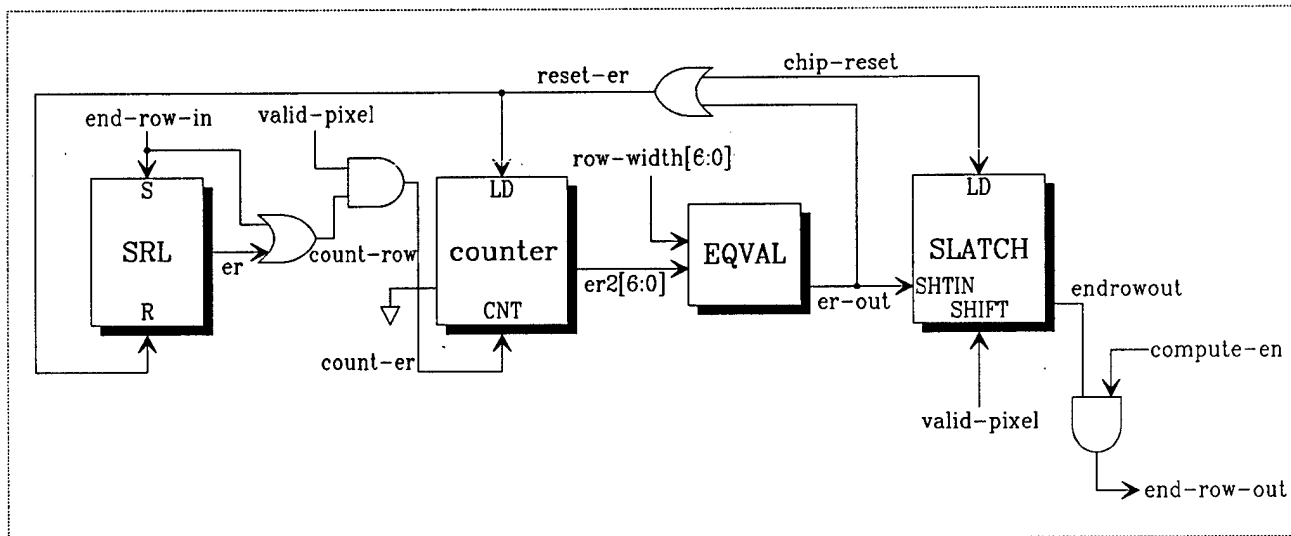
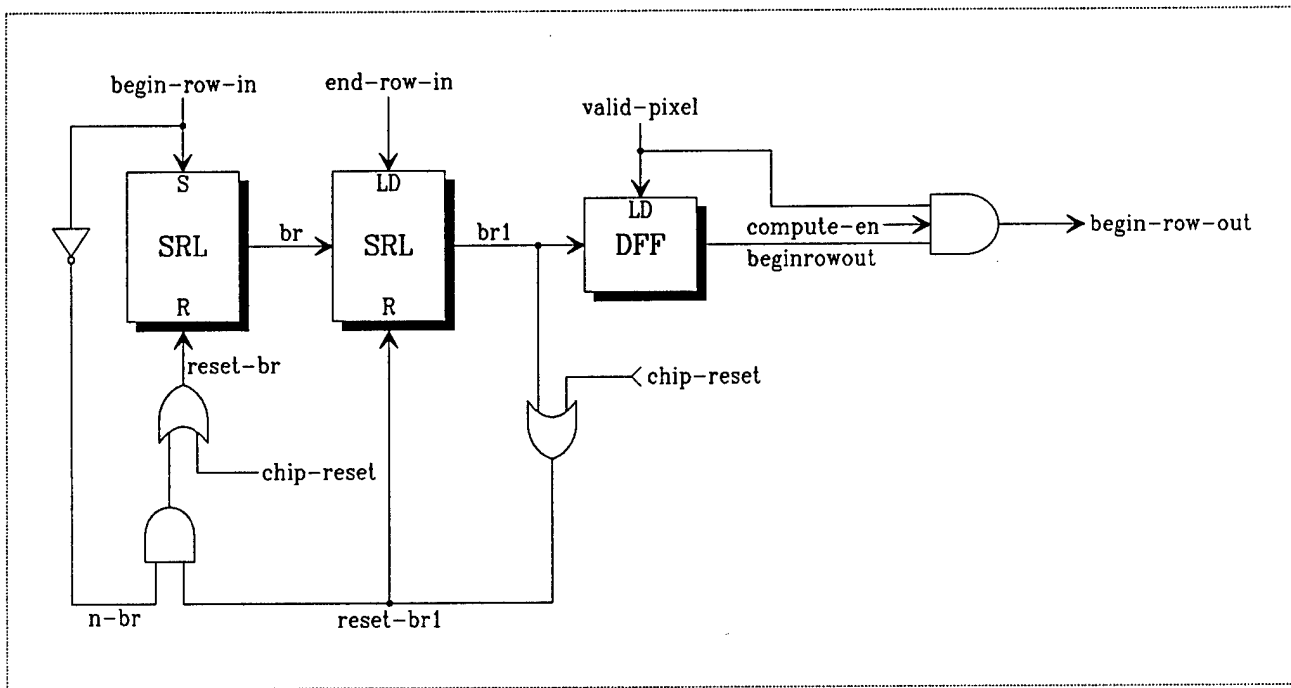
Address-select



Decoders





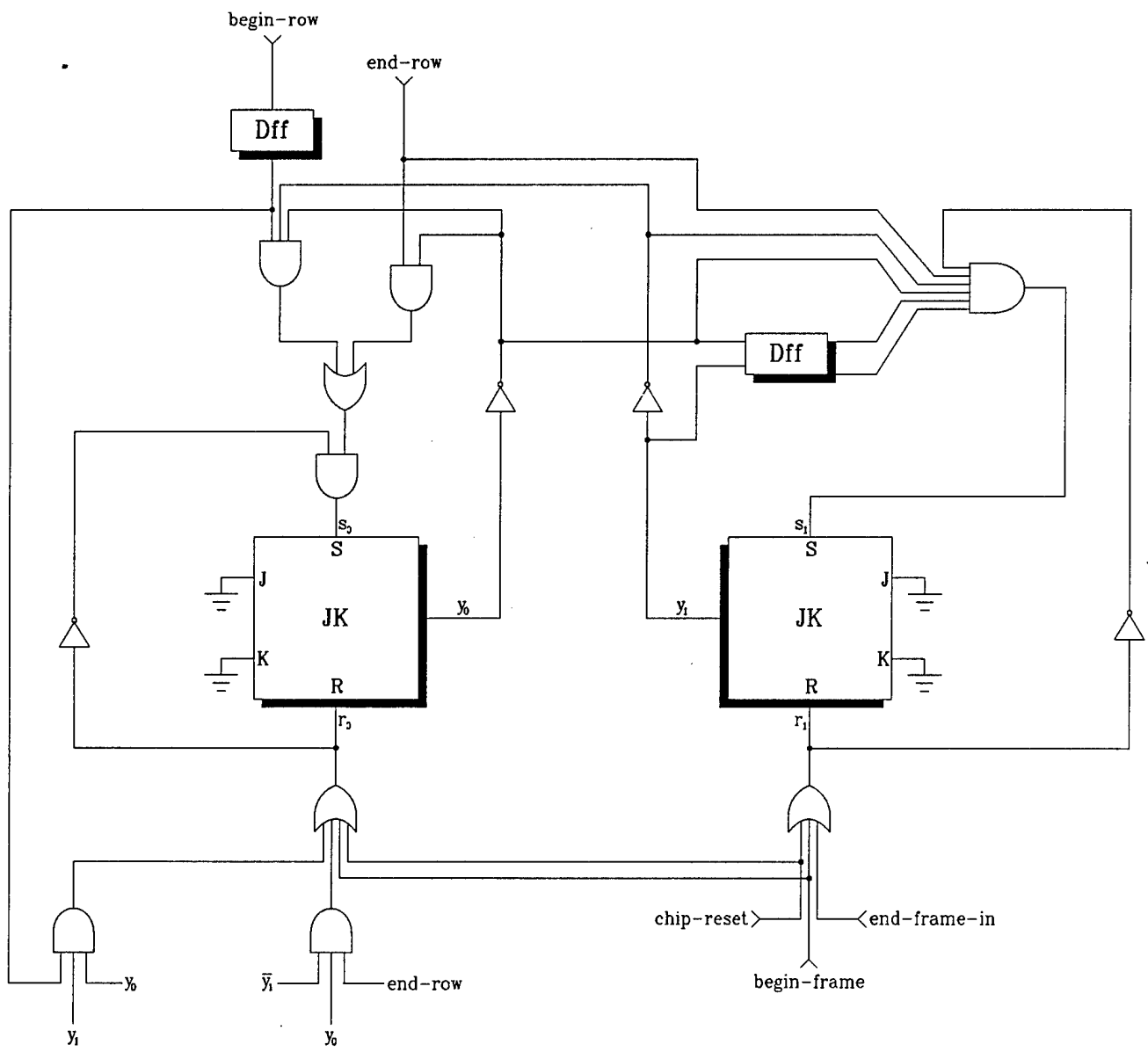


$$s_0 = (\bar{y}_1 \bar{y}_0 b_{r_{n-1}} + \bar{y}_0 e) \text{ reset}$$

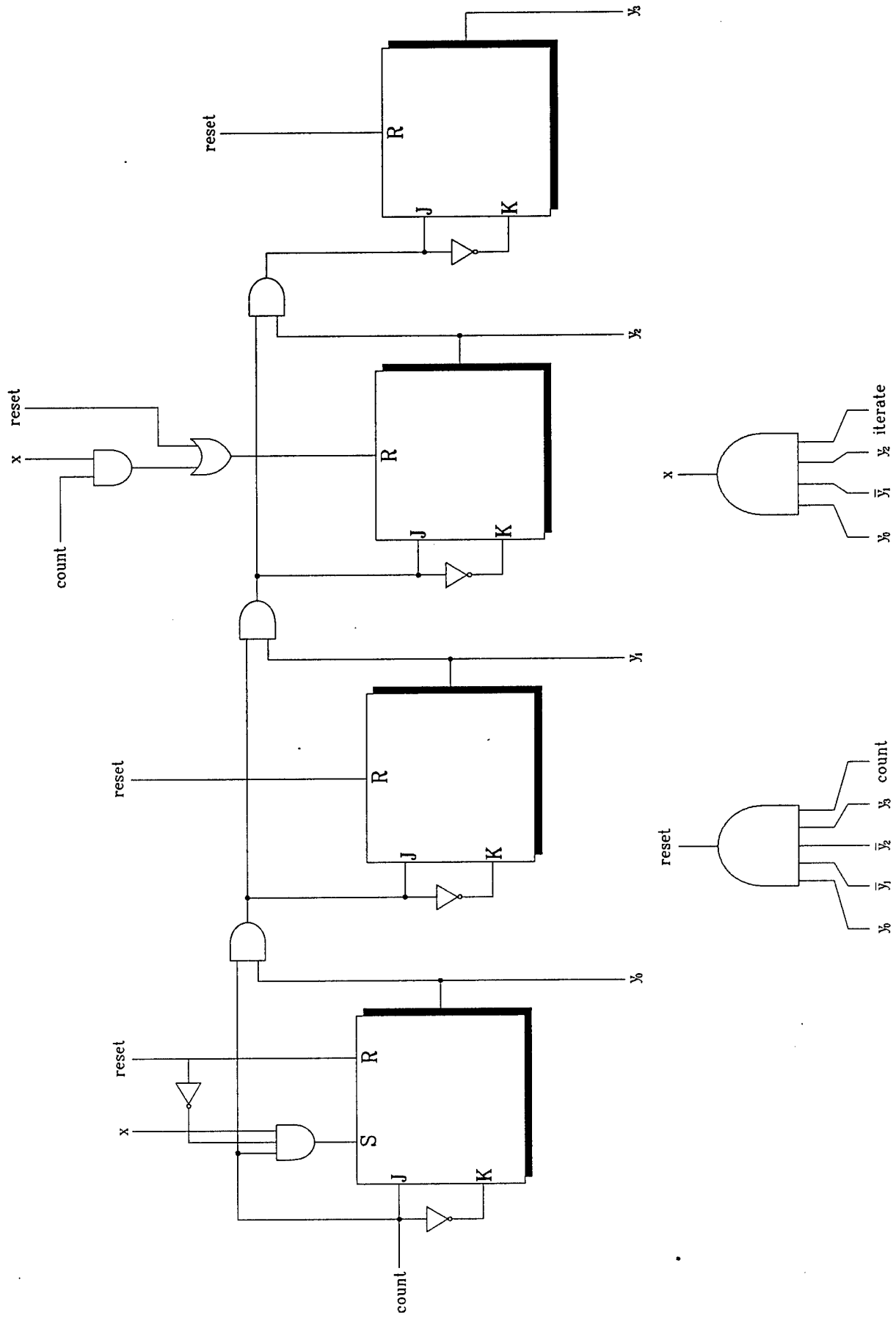
$$r_0 = \text{reset} + b_r + y_1 y_0 b_{r_{n-1}} + \bar{y}_1 y_0 e_r$$

$$s_1 = r_1 \cdot \{(y_1 \bar{y}_0)_{k-1} (\bar{y}_1 \bar{y}_0)_k e_r\}$$

$$r = \text{reset} + b + \text{end-frame-in (last-row)}$$



Schematic of state-mach block



Schematic of state-mach

INFO:Selecting last corner used - 'GUARANTEED'
Operating condition changed: 60 deg C and 5.00v

CLOCKS

Phase 1 High = 75.8ns Phase 2 High = 117.5 ns
Cycle (Ph1) = 114.7ns Cycle (Ph2) = 142.6ns
Minimum Cycle Time = 193.3ns Symmetric Cycle Time = 234.9ns

** Minimum Phase 1 High Time = 75.8 ns (clockdelay:9.1ns (84.9-75.8))

| | | |
|--------------------------------|------|------|
| pipe/mem1/fifo1/(internal) | fall | 84.9 |
| pipe/mem1/fifo1/read_fifo1 | rise | 74.6 |
| pipe/control/logic/read_fifo1 | rise | 74.5 |
| pipe/control/logic/read_fifo1' | rise | 63.5 |
| pipe/control/logic/GB.LP.I_220 | fall | 62.9 |
| pipe/control/logic/read_fifo2 | rise | 61.8 |
| pipe/control/logic/read_fifo2' | rise | 33.6 |
| pipe/control/logic/GB.LP.I_265 | fall | 31.7 |
| pipe/control/logic/valid_pixel | rise | 31.1 |
| <pe/control/logic/valid_pixel' | rise | 14.3 |
| pipe/control/logic/GB.LP.I_139 | rise | 11.6 |
| pipe/control/logic/GB.LP.I_165 | fall | 11.2 |
| pipe/control/logic/PHASE_A | rise | 9.6 |
| pixelclk/PHASE_A | rise | 8.0 |
| pixel_clk | rise | 0.0 |

** Minimum Phase 2 High Time = 117.5 ns (clockdelay:4.6ns (122.1-117.5))

| | | |
|-----------------------------|------|-------|
| multD/coeff_bank/(internal) | fall | 122.1 |
| multD/coeff_bank/A_ADDR[1] | rise | 120.7 |
| control/read_addr[1] | rise | 120.5 |
| control/read_addr[1]' | rise | 56.4 |
| control/GB.LP.I_248 | fall | 50.0 |
| control/read | rise | 49.0 |
| host_interface/read | rise | 48.4 |
| host_interface/read' | rise | 15.3 |
| host_interface/GB.LP.I_298 | fall | 14.3 |
| host_interface/GB.LP.I_152 | rise | 12.8 |
| host_interface/GB.LP.I_161 | fall | 10.4 |
| host_interface/GB.LP.I_290 | rise | 9.8 |
| host_interface/GB.LP.I_155 | fall | 7.8 |
| host_interface/id[2] | fall | 5.4 |
| chip_id[2]/chip_id | fall | 5.1 |
| chip_id[2]/chip_id' | fall | 3.6 |
| Chip_id[2] | fall | 0.0 |

** Minimum Cycle (Ph1) Time = 114.7 ns (clockdelay:9.4ns (124.0-114.7))

| | | |
|------------------------------|------|-------|
| multB/coeff_bank/225 | fall | 124.0 |
| *multB/coeff_bank/(internal) | fall | 122.1 |
| multB/coeff_bank/A_ADDR[1] | rise | 121.7 |
| control/read_addr[1] | rise | 121.4 |
| control/read_addr[1]' | rise | 57.3 |
| control/GB.LP.I_248 | fall | 51.0 |
| control/read | rise | 50.0 |
| host_interface/read | rise | 49.4 |
| host_interface/read' | rise | 16.2 |
| host_interface/GB.LP.I_298 | fall | 15.2 |
| host_interface/GB.LP.I_61 | rise | 13.4 |
| host_interface/GB.LP.I_262 | rise | 10.7 |
| host_interface/PHASE_A | rise | 8.8 |

```

pixelclk/PHASE_A  rise      8.0
pixel_clk        rise      0.0

```

** Minimum Cycle (Ph2) Time = 142.6 ns (clockdelay:8.3ns (151.0-142.6))

```

multD/coeff_bank/(internal)  fall      151.0
multD/coeff_bank/A_ADDR[1]   rise      150.5
control/read_addr[1]         rise      150.3
control/read_addr[1]'        rise      86.1
control/GB.LP.I_248          fall      79.8
control/read                  rise      78.8
host_interface/read           rise      78.2
host_interface/read'          rise      45.1
host_interface/GB.LP.I_298    fall      44.0
host_interface/GB.LP.I_61     rise      42.3
*host_interface/(internal)   fall      39.8
host_interface/GB.LP.I_54     rise      39.6
host_interface/GB.LP.I_71     fall      37.4
host_interface/GB.LP.I_68     fall      35.0
host_interface/GB.LP.I_274    rise      34.4
host_interface/GB.LP.I_159    fall      33.1
host_interface/GB.LP.I_276    rise      32.2
host_interface/data_dis       fall      31.0
host_interface/data_dis'      fall      16.8
host_interface/GB.LP.I_149    rise      15.7
host_interface/GB.LP.I_294    fall      13.8
host_interface/GB.LP.I_152    rise      12.8
host_interface/GB.LP.I_161    fall      10.4
host_interface/GB.LP.I_290    rise       9.8
host_interface/GB.LP.I_155    fall       7.8
host_interface/id[2]          fall       5.4
chip_id[2]/chip_id           fall       5.1
chip_id[2]/chip_id'          fall       3.6
Chip_id[2]                   fall       0.0

```

tv_clkrpt() DONE

CLOCK_PERIOD VIOLATIONS: 0

tv_verify_clk() DONE

BACK

SETUP_HOLD

| Input name | Phase_1 | | Phase_2 | |
|----------------|---------|--------|----------|---------|
| | (setup) | (hold) | (setup) | (hold) |
| Addertest | (---) | (---) | (7.1) | (-1.3) |
| Begin_frame_in | (---) | (---) | (4.7) | (1.2) |
| Begin_row_in | (---) | (---) | (5.7) | (1.2) |
| Chip_id[0] | (---) | (---) | (116.0) | (-6.5) |
| Chip_id[1] | (---) | (---) | (116.4) | (-6.9) |
| Chip_id[2] | (---) | (---) | (117.5) | (-8.0) |
| Chip_id[3] | (---) | (---) | (114.5) | (-5.1) |
| Data[0] | (---) | (---) | (-1.0) | (3.3) |
| Data[10] | (---) | (---) | (-0.2) | (2.1) |
| Data[11] | (---) | (---) | (-0.1) | (1.9) |
| Data[12] | (---) | (---) | (-0.2) | (2.1) |
| Data[13] | (---) | (---) | (-0.8) | (2.9) |
| Data[14] | (---) | (---) | (-0.3) | (2.3) |

```

Data[15] ( ---- ----) ( -0.4 2.3)
Data[1] ( ---- ----) ( -0.6 2.8)
Data[2] ( ---- ----) ( -0.7 2.9)
Data[3] ( ---- ----) ( -0.6 2.8)
Data[4] ( ---- ----) ( -0.6 2.8)
Data[5] ( ---- ----) ( -0.2 2.2)
Data[6] ( ---- ----) ( -0.2 2.2)
Data[7] ( ---- ----) ( -0.5 2.5)
Data[8] ( ---- ----) ( -0.4 2.4)
Data[9] ( ---- ----) ( -0.3 2.2)
Dev_select[0] ( ---- ----) ( 115.6 -6.5)
Dev_select[1] ( ---- ----) ( 116.1 -7.0)
Dev_select[2] ( ---- ----) ( 116.3 -7.1)
Dev_select[3] ( ---- ----) ( 113.5 -4.4)
End_frame_in ( ---- ----) ( 6.7 -1.8)
End_row_in ( ---- ----) ( 15.0 0.2)
Host_addr[0] ( ---- ----) ( -0.3 3.5)
Host_addr[1] ( ---- ----) ( -0.2 3.5)
Host_addr[2] ( ---- ----) ( -0.3 3.5)
Host_addr[3] ( ---- ----) ( -0.5 3.8)
Host_addr[4] ( ---- ----) ( 0.1 3.2)
Ios ( ---- ----) ( 1.9 1.9)
Multtest ( ---- ----) ( 47.1 -6.6)
N_reset ( 21.2 -16.1) ( 20.8 -10.5)
Ode ( ---- ----) ( 107.8 0.3)
Pixel_in[0] ( ---- ----) ( -1.2 4.9)
Pixel_in[10] ( ---- ----) ( -0.9 4.6)
Pixel_in[11] ( ---- ----) ( -0.8 4.5)
Pixel_in[12] ( ---- ----) ( -0.4 4.1)
Pixel_in[13] ( ---- ----) ( -0.1 3.8)
Pixel_in[14] ( ---- ----) ( -0.6 4.2)
Pixel_in[15] ( ---- ----) ( -0.4 4.0)
Pixel_in[1] ( ---- ----) ( -1.6 5.3)
Pixel_in[2] ( ---- ----) ( -1.2 4.9)
Pixel_in[3] ( ---- ----) ( -1.3 5.0)
Pixel_in[4] ( ---- ----) ( -1.5 5.3)
Pixel_in[5] ( ---- ----) ( -1.3 5.1)
Pixel_in[6] ( ---- ----) ( -1.1 4.9)
Pixel_in[7] ( ---- ----) ( -1.2 4.9)
Pixel_in[8] ( ---- ----) ( -1.1 4.8)
Pixel_in[9] ( ---- ----) ( -1.0 4.7)

```

tv_input() DONE

BACK

OUTPUT_DELAY

```

Begin_frame_out (min1= 25.8 max1= 44.6) (min2= --- max2= ---) (loa
Begin_row_out (min1= 31.3 max1= 50.1) (min2= --- max2= ---) (loa
DR_n_aDR (min1= 19.6 max1= 31.7) (min2= 19.6 max2= 26.3) (loa
Data[0] (min1= 0.0 max1= 43.2) (min2= 0.0 max2= 43.2) (loa
Data[10] (min1= 0.0 max1= 43.0) (min2= 0.0 max2= 43.0) (loa
Data[11] (min1= 0.0 max1= 43.0) (min2= 0.0 max2= 43.0) (loa
Data[12] (min1= 0.0 max1= 43.0) (min2= 0.0 max2= 43.0) (loa
Data[13] (min1= 0.0 max1= 42.9) (min2= 0.0 max2= 42.9) (loa
Data[14] (min1= 0.0 max1= 42.9) (min2= 0.0 max2= 42.9) (loa
Data[15] (min1= 0.0 max1= 42.9) (min2= 0.0 max2= 42.9) (loa
Data[1] (min1= 0.0 max1= 43.2) (min2= 0.0 max2= 43.2) (loa
Data[2] (min1= 0.0 max1= 43.2) (min2= 0.0 max2= 43.2) (loa

```

| | | | | | | | | | |
|---------------|--------|------|-------|--------|--------|------|-------|--------|------|
| Data[3] | (min1= | 0.0 | max1= | 43.2) | (min2= | 0.0 | max2= | 43.2) | (loa |
| Data[4] | (min1= | 0.0 | max1= | 43.2) | (min2= | 0.0 | max2= | 43.2) | (loa |
| Data[5] | (min1= | 0.0 | max1= | 43.1) | (min2= | 0.0 | max2= | 43.1) | (loa |
| Data[6] | (min1= | 0.0 | max1= | 43.1) | (min2= | 0.0 | max2= | 43.1) | (loa |
| Data[7] | (min1= | 0.0 | max1= | 43.1) | (min2= | 0.0 | max2= | 43.1) | (loa |
| Data[8] | (min1= | 0.0 | max1= | 43.1) | (min2= | 0.0 | max2= | 43.1) | (loa |
| Data[9] | (min1= | 0.0 | max1= | 43.0) | (min2= | 0.0 | max2= | 43.0) | (loa |
| End_row_out | (min1= | 26.2 | max1= | 32.8) | (min2= | --- | max2= | --- | (loa |
| End_row_out | (min1= | 28.8 | max1= | 35.8) | (min2= | --- | max2= | --- | (loa |
| Pix_lsb[0] | (min1= | 30.9 | max1= | 188.5) | (min2= | 30.9 | max2= | 168.3) | (loa |
| Pix_lsb[1] | (min1= | 31.0 | max1= | 188.6) | (min2= | 31.0 | max2= | 168.4) | (loa |
| Pix_lsb[2] | (min1= | 31.1 | max1= | 188.7) | (min2= | 31.1 | max2= | 168.6) | (loa |
| Pix_msb[0] | (min1= | 30.3 | max1= | 189.1) | (min2= | 30.3 | max2= | 168.9) | (loa |
| Pix_msb[1] | (min1= | 30.3 | max1= | 190.2) | (min2= | 30.3 | max2= | 170.1) | (loa |
| Pix_msb[2] | (min1= | 30.4 | max1= | 191.1) | (min2= | 30.4 | max2= | 170.9) | (loa |
| Pixel_out[0] | (min1= | 29.6 | max1= | 186.9) | (min2= | 29.6 | max2= | 166.8) | (loa |
| Pixel_out[10] | (min1= | 29.3 | max1= | 186.6) | (min2= | 29.3 | max2= | 166.4) | (loa |
| Pixel_out[11] | (min1= | 28.9 | max1= | 186.1) | (min2= | 28.9 | max2= | 166.0) | (loa |
| Pixel_out[12] | (min1= | 28.5 | max1= | 185.6) | (min2= | 28.5 | max2= | 165.4) | (loa |
| Pixel_out[13] | (min1= | 28.4 | max1= | 185.5) | (min2= | 28.4 | max2= | 165.3) | (loa |
| Pixel_out[14] | (min1= | 28.3 | max1= | 185.3) | (min2= | 28.3 | max2= | 165.1) | (loa |
| Pixel_out[15] | (min1= | 28.2 | max1= | 186.3) | (min2= | 28.2 | max2= | 166.1) | (loa |
| Pixel_out[1] | (min1= | 29.5 | max1= | 186.9) | (min2= | 29.5 | max2= | 166.7) | (loa |
| Pixel_out[2] | (min1= | 30.4 | max1= | 187.9) | (min2= | 30.4 | max2= | 167.8) | (loa |
| Pixel_out[3] | (min1= | 30.0 | max1= | 187.5) | (min2= | 30.0 | max2= | 167.4) | (loa |
| Pixel_out[4] | (min1= | 29.9 | max1= | 187.4) | (min2= | 29.9 | max2= | 167.2) | (loa |
| Pixel_out[5] | (min1= | 29.8 | max1= | 187.2) | (min2= | 29.8 | max2= | 167.1) | (loa |
| Pixel_out[6] | (min1= | 29.7 | max1= | 187.1) | (min2= | 29.7 | max2= | 166.9) | (loa |
| Pixel_out[7] | (min1= | 29.6 | max1= | 187.0) | (min2= | 29.6 | max2= | 166.8) | (loa |
| Pixel_out[8] | (min1= | 29.5 | max1= | 186.8) | (min2= | 29.5 | max2= | 166.7) | (loa |
| Pixel_out[9] | (min1= | 29.4 | max1= | 186.7) | (min2= | 29.4 | max2= | 166.5) | (loa |
| Sign | (min1= | 51.9 | max1= | 154.7) | (min2= | 51.9 | max2= | 134.6) | (loa |

tv_output() DONE
) BACK
) VIOLATIONS

INPUT VIOLATIONS: 0
 tv_verify_input() DONE

OUTPUT VIOLATIONS: 0
 tv_verify_output() DONE

Internal hold time check (Margin=1.7ns)
 INFO: 4814 Phase_1 latches checked; 0 violations detected
 INFO: 4966 Phase_2 latches checked; 0 violations detected
 INFO: No internal hold time violations detected.
 Internal hold time check done.
 NO VIOLATIONS.

INFO:Selecting last corner used - 'GUARANTEED'
 Operating condition changed: 150 deg C and 4.50v

CLOCKS

Key Parameters (set 122) Modified
 Phase 1 High = 104.7ns Phase 2 High = 162.7 ns
 Cycle (Ph1) = 158.8ns Cycle (Ph2) = 197.3ns
 Minimum Cycle Time = 267.4ns Symmetric Cycle Time = 325.5ns

```

** Minimum Phase 1 High Time = 104.7 ns (clockdelay:12.5ns (117.2-104.7))
pipe/mem1/fifo1/(internal) fall 117.2
pipe/mem1/fifo1/read_fifo1 rise 103.2
pipe/control/logic/read_fifo1 rise 103.0
pipe/control/logic/read_fifo1' rise 87.7
pipe/control/logic/GB.LP.I_220 fall 87.0
pipe/control/logic/read_fifo2 rise 85.5
pipe/control/logic/read_fifo2' rise 46.3
pipe/control/logic/GB.LP.I_265 fall 43.6
pipe/control/logic/valid_pixel rise 42.8
<pe/control/logic/valid_pixel' rise 19.6
pipe/control/logic/GB.LP.I_139 rise 15.9
pipe/control/logic/GB.LP.I_165 fall 15.3
pipe/control/logic/PHASE_A rise 13.2
    pixelclk/PHASE_A rise 11.0
        pixel_clk rise 0.0

```

```

** Minimum Phase 2 High Time = 162.7 ns (clockdelay:6.3ns (169.1-162.7))
multD/coeff_bank/(internal) fall 169.1
multD/coeff_bank/A_ADDR[1] rise 167.3
control/read_addr[1] rise 166.9
control/read_addr[1]' rise 77.9
    control/GB.LP.I_248 fall 69.2
        control/read rise 67.8
    host_interface/read rise 67.0
    host_interface/read' rise 21.0
host_interface/GB.LP.I_298 fall 19.6
host_interface/GB.LP.I_152 rise 17.6
host_interface/GB.LP.I_161 fall 14.3
host_interface/GB.LP.I_290 rise 13.5
host_interface/GB.LP.I_155 fall 10.7
host_interface/id[2] fall 7.4
    chip_id[2]/chip_id fall 7.0
    chip_id[2]/chip_id' fall 4.9
        Chip_id[2] fall 0.0

```

```

** Minimum Cycle (Ph1) Time = 158.8 ns (clockdelay:12.9ns (171.7-158.8))
multB/coeff_bank/225 fall 171.7
*multB/coeff_bank/(internal) fall 169.1
multB/coeff_bank/A_ADDR[1] rise 168.5
control/read_addr[1] rise 168.2
control/read_addr[1]' rise 79.2
    control/GB.LP.I_248 fall 70.4
        control/read rise 69.0
    host_interface/read rise 68.2
    host_interface/read' rise 22.2
host_interface/GB.LP.I_298 fall 20.8
host_interface/GB.LP.I_61 rise 18.4
host_interface/GB.LP.I_262 rise 14.7
host_interface/PHASE_A rise 12.2
    pixelclk/PHASE_A rise 11.0
        pixel_clk rise 0.0

```

```

** Minimum Cycle (Ph2) Time = 197.3 ns (clockdelay:11.5ns (208.8-197.3))
multD/coeff_bank/(internal) fall 208.8
multD/coeff_bank/A_ADDR[1] rise 208.2
control/read_addr[1] rise 207.9
control/read_addr[1]' rise 118.9
    control/GB.LP.I_248 fall 110.1

```

```

control/read rise 108.7
host_interface/read rise 107.9
host_interface/read' rise 61.9
host_interface/GB.LP.I_298 fall 60.5
host_interface/GB.LP.I_61 rise 58.1
*host_interface/(internal) fall 54.7
host_interface/GB.LP.I_54 rise 54.4
host_interface/GB.LP.I_71 fall 51.4
host_interface/GB.LP.I_68 fall 48.2
host_interface/GB.LP.I_274 rise 47.4
host_interface/GB.LP.I_159 fall 45.7
host_interface/GB.LP.I_276 rise 44.5
host_interface/data_dis fall 42.7
host_interface/data_dis' fall 23.0
host_interface/GB.LP.I_149 rise 21.6
host_interface/GB.LP.I_294 fall 19.0
host_interface/GB.LP.I_152 rise 17.6
host_interface/GB.LP.I_161 fall 14.3
host_interface/GB.LP.I_290 rise 13.5
host_interface/GB.LP.I_155 fall 10.7
host_interface/id[2] fall 7.4
chip_id[2]/chip_id fall 7.0
chip_id[2]/chip_id' fall 4.9
Chip_id[2] fall 0.0
tv_clkrrpt() DONE

```

```

CLOCK_PERIOD VIOLATIONS: 0
tv_verify_clk() DONE

```

) SETUP_HOLD

| Input name | Phase_1 | | Phase_2 | |
|----------------|---------|---------|-----------|-----------|
| | (setup) | (hold) | (setup) | (hold) |
| Addertest | (---) | (---) | (9.4) | (-1.8) |
| Begin_frame_in | (---) | (---) | (6.2) | (1.6) |
| Begin_row_in | (---) | (---) | (7.9) | (1.6) |
| Chip_id[0] | (---) | (---) | (160.7) | (-8.8) |
| Chip_id[1] | (---) | (---) | (161.2) | (-9.4) |
| Chip_id[2] | (---) | (---) | (162.7) | (-10.9) |
| Chip_id[3] | (---) | (---) | (158.7) | (-7.0) |
| Data[0] | (---) | (---) | (-1.4) | (4.5) |
| Data[10] | (---) | (---) | (-0.3) | (2.9) |
| Data[11] | (---) | (---) | (-0.2) | (2.6) |
| Data[12] | (---) | (---) | (-0.3) | (2.9) |
| Data[13] | (---) | (---) | (-1.1) | (3.9) |
| Data[14] | (---) | (---) | (-0.5) | (3.1) |
| Data[15] | (---) | (---) | (-0.6) | (3.2) |
| Data[1] | (---) | (---) | (-0.8) | (3.8) |
| Data[2] | (---) | (---) | (-0.9) | (4.0) |
| Data[3] | (---) | (---) | (-0.8) | (3.8) |
| Data[4] | (---) | (---) | (-0.8) | (3.8) |
| Data[5] | (---) | (---) | (-0.4) | (2.9) |
| Data[6] | (---) | (---) | (-0.4) | (2.9) |
| Data[7] | (---) | (---) | (-0.7) | (3.4) |
| Data[8] | (---) | (---) | (-0.6) | (3.3) |
| Data[9] | (---) | (---) | (-0.4) | (3.0) |
| Dev_select[0] | (---) | (---) | (160.2) | (-8.8) |
| Dev_select[1] | (---) | (---) | (160.8) | (-9.5) |
| Dev_select[2] | (---) | (---) | (161.1) | (-9.5) |

```

Dev_select[3] ( ---- ----) ( 157.3 -6.0)
End_frame_in ( ---- ----) ( 9.3 -2.5)
End_row_in ( ---- ----) ( 20.4 0.2)
Host_addr[0] ( ---- ----) ( -0.4 4.8)
Host_addr[1] ( ---- ----) ( -0.4 4.8)
Host_addr[2] ( ---- ----) ( -0.4 4.9)
Host_addr[3] ( ---- ----) ( -0.8 5.2)
Host_addr[4] ( ---- ----) ( 0.1 4.3)
Ios ( ---- ----) ( 2.5 2.6)
Multtest ( ---- ----) ( 65.2 -9.0)
N_reset ( 29.3 -22.5) ( 28.8 -14.7)
Ode ( ---- ----) ( 149.5 0.3)
Pixel_in[0] ( ---- ----) ( -1.7 6.6)
Pixel_in[10] ( ---- ----) ( -1.3 6.2)
Pixel_in[11] ( ---- ----) ( -1.1 6.0)
Pixel_in[12] ( ---- ----) ( -0.7 5.6)
Pixel_in[13] ( ---- ----) ( -0.2 5.0)
Pixel_in[14] ( ---- ----) ( -0.9 5.7)
Pixel_in[15] ( ---- ----) ( -0.6 5.4)
Pixel_in[1] ( ---- ----) ( -2.3 7.3)
Pixel_in[2] ( ---- ----) ( -1.7 6.6)
Pixel_in[3] ( ---- ----) ( -1.8 6.8)
Pixel_in[4] ( ---- ----) ( -2.2 7.2)
Pixel_in[5] ( ---- ----) ( -1.9 6.9)
Pixel_in[6] ( ---- ----) ( -1.6 6.6)
Pixel_in[7] ( ---- ----) ( -1.7 6.6)
Pixel_in[8] ( ---- ----) ( -1.6 6.5)
Pixel_in[9] ( ---- ----) ( -1.5 6.4)

```

```

tv_input() DONE
) BACK

```

```

tanA tanB tanB tanB

```

) OUTPUT_DELAY

tanB

```

Begin_frame_out (min1= 35.4 max1= 61.5) (min2= --- max2= ---) (loa
Begin_row_out (min1= 43.0 max1= 69.1) (min2= --- max2= ---) (loa
DR_n_aDR (min1= 26.8 max1= 43.4) (min2= 26.8 max2= 36.2) (loa
Data[0] (min1= 0.0 max1= 59.7) (min2= 0.0 max2= 59.7) (loa
Data[10] (min1= 0.0 max1= 59.4) (min2= 0.0 max2= 59.4) (loa
Data[11] (min1= 0.0 max1= 59.3) (min2= 0.0 max2= 59.3) (loa
Data[12] (min1= 0.0 max1= 59.3) (min2= 0.0 max2= 59.3) (loa
Data[13] (min1= 0.0 max1= 59.3) (min2= 0.0 max2= 59.3) (loa
Data[14] (min1= 0.0 max1= 59.2) (min2= 0.0 max2= 59.2) (loa
Data[15] (min1= 0.0 max1= 59.2) (min2= 0.0 max2= 59.2) (loa
Data[1] (min1= 0.0 max1= 59.7) (min2= 0.0 max2= 59.7) (loa
Data[2] (min1= 0.0 max1= 59.7) (min2= 0.0 max2= 59.7) (loa
Data[3] (min1= 0.0 max1= 59.7) (min2= 0.0 max2= 59.7) (loa
Data[4] (min1= 0.0 max1= 59.6) (min2= 0.0 max2= 59.6) (loa
Data[5] (min1= 0.0 max1= 59.5) (min2= 0.0 max2= 59.5) (loa
Data[6] (min1= 0.0 max1= 59.5) (min2= 0.0 max2= 59.5) (loa
Data[7] (min1= 0.0 max1= 59.5) (min2= 0.0 max2= 59.5) (loa
Data[8] (min1= 0.0 max1= 59.4) (min2= 0.0 max2= 59.4) (loa
Data[9] (min1= 0.0 max1= 59.4) (min2= 0.0 max2= 59.4) (loa
End_frame_out (min1= 36.0 max1= 45.2) (min2= --- max2= ---) (loa
End_row_out (min1= 39.6 max1= 49.4) (min2= --- max2= ---) (loa
Pix_lsb[0] (min1= 42.5 max1= 258.2) (min2= 42.5 max2= 230.7) (loa
Pix_lsb[1] (min1= 42.6 max1= 258.3) (min2= 42.6 max2= 230.9) (loa
Pix_lsb[2] (min1= 42.8 max1= 258.5) (min2= 42.8 max2= 231.1) (loa
Pix_msb[0] (min1= 41.7 max1= 258.5) (min2= 41.7 max2= 231.1) (loa

```

| | | | | | | | | | |
|---------------|--------|------|-------|--------|--------|------|-------|--------|------|
| Pix_msb[1] | (min1= | 41.7 | max1= | 260.1) | (min2= | 41.7 | max2= | 232.6) | (loa |
| Pix_msb[2] | (min1= | 41.8 | max1= | 261.2) | (min2= | 41.8 | max2= | 233.8) | (loa |
| Pixel_out[0] | (min1= | 40.7 | max1= | 256.0) | (min2= | 40.7 | max2= | 228.6) | (loa |
| Pixel_out[10] | (min1= | 40.4 | max1= | 255.6) | (min2= | 40.4 | max2= | 228.2) | (loa |
| Pixel_out[11] | (min1= | 39.9 | max1= | 254.9) | (min2= | 39.9 | max2= | 227.5) | (loa |
| Pixel_out[12] | (min1= | 39.2 | max1= | 254.1) | (min2= | 39.2 | max2= | 226.7) | (loa |
| Pixel_out[13] | (min1= | 39.1 | max1= | 254.0) | (min2= | 39.1 | max2= | 226.6) | (loa |
| Pixel_out[14] | (min1= | 38.9 | max1= | 253.8) | (min2= | 38.9 | max2= | 226.3) | (loa |
| Pixel_out[15] | (min1= | 38.8 | max1= | 254.6) | (min2= | 38.8 | max2= | 227.2) | (loa |
| Pixel_out[1] | (min1= | 40.6 | max1= | 255.9) | (min2= | 40.6 | max2= | 228.5) | (loa |
| Pixel_out[2] | (min1= | 41.8 | max1= | 257.4) | (min2= | 41.8 | max2= | 230.0) | (loa |
| Pixel_out[3] | (min1= | 41.4 | max1= | 256.8) | (min2= | 41.4 | max2= | 229.4) | (loa |
| Pixel_out[4] | (min1= | 41.2 | max1= | 256.6) | (min2= | 41.2 | max2= | 229.2) | (loa |
| Pixel_out[5] | (min1= | 41.0 | max1= | 256.4) | (min2= | 41.0 | max2= | 229.0) | (loa |
| Pixel_out[6] | (min1= | 40.9 | max1= | 256.2) | (min2= | 40.9 | max2= | 228.8) | (loa |
| Pixel_out[7] | (min1= | 40.8 | max1= | 256.1) | (min2= | 40.8 | max2= | 228.7) | (loa |
| Pixel_out[8] | (min1= | 40.6 | max1= | 255.9) | (min2= | 40.6 | max2= | 228.4) | (loa |
| Pixel_out[9] | (min1= | 40.5 | max1= | 255.7) | (min2= | 40.5 | max2= | 228.3) | (loa |
| Sign | (min1= | 71.0 | max1= | 211.8) | (min2= | 71.0 | max2= | 184.3) | (loa |

tv_output() DONE

) BACK

) VIOLATIONS

INPUT VIOLATIONS: 0

tv_verify_input() DONE

OUTPUT VIOLATIONS: 0

tv_verify_output() DONE

Internal hold time check (Margin=2.0ns)

INFO: 4814 Phase_1 latches checked; 0 violations detected

INFO: 4966 Phase_2 latches checked; 0 violations detected

INFO: No internal hold time violations detected.

Internal hold time check done.

NO VIOLATIONS.

) BACK

**** END Command File 'timing'

ACK

CONFIRM

EXIT_GENESIL

o ke

 ^^^^^^^ GENESIL Client session log is above ^^^^^^^

vvvvvvvvv GENESIL Server session log is below vvvvvvvvv

End of GENESIL session '30_Jan_1'