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THESIS

THE DESIGN, SIMULATION, AND FABRICATION OF A BICMOS VLSI DIGITALLY PROGRAMMABLE GIC FILTER

by

Paul R. Milne

September 2001

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This thesis used a previously-designed programmable GIC filter as a basis in which to incorporate a BiCMOS operational amplifier. An NPN bipolar transistor layout was designed and incorporated into an opamp layout, which was a modified version of a CMOS-only design. The BiCMOS opamp was simulated using Silvaco SmartSpice and showed considerable improvement over its CMOS equivalent. Additional improvements were made to the GIC filter to include a passgate with reduced resistance, and a correction was made to the capacitor layout. Simulations were also performed on a switched-capacitor bilinear resistor and a switched-capacitor variable bilinear resistor. Results from the bilinear resistor simulations require further study and testing. Finally, a VLSI layout of the filter was accomplished using LASI and has been submitted to MOSIS for fabrication.

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THE DESIGN, SIMULATION, AND FABRICATION OF A BICMOS VLSI DIGITALLY PROGRAMMABLE GIC FILTER

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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

This thesis used a previously designed programmable GIC filter as a basis in which to incorporate a BiCMOS operational amplifier. An NPN bipolar transistor layout was designed and incorporated into an opamp layout, which was a modified version of a CMOS-only design. The BiCMOS opamp was simulated using Silvaco SmartSpice and showed considerable improvement over its CMOS equivalent. Additional improvements were made to the GIC filter to include a passgate with reduced resistance, and a correction was made to the capacitor layout. Simulations were also performed on a switched-capacitor bilinear resistor and a switched-capacitor variable bilinear resistor. Results from the bilinear resistor simulations require further study and testing. Finally, a VLSI layout of the filter was accomplished using LASI and has been submitted to MOSIS for fabrication.

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EXECUTIVE SUMMARY

Analog filtering is a necessity to electronic systems even in many digital applications. The BiCMOS programmable General Immittance Converter (GIC) filter VLSI design offers a robust set of characteristics that makes it ideal for implementation in any system-on-a-chip type design. The GIC filter design, which has been studied in great detail at NPS, was upgraded to contain a BiCMOS amplifier. The BiCMOS amplifier outperforms its CMOS counterpart by improving the gain bandwidth product and thus extending the operating range of frequencies.

Other improvements were made as well. The power consumption was reduced by approximately 1/5 by reducing the input power supply from ± 5.0 Volts to ± 3.3 Volts. The voltage-dependant VLSI capacitor design was replaced with a capacitor that varies very little with voltage. The switches used for switched capacitors and digital logic were examined in detail and optimized for size and resistance. The bilinear resistor and variable bilinear resistor accomplished with switched capacitors were also studied in detail. Numerous simulations suggested that further work must be accomplished in the area of simulating and designing switched capacitor resistors.

Because this is the first design and fabrication of a BiCMOS chip at NPS, the research performed in this thesis and the design submitted for fabrication will aid future analog designers. Studies into how well simulations match the actual test results from the fabrication of the BiCMOS opamp and studies into bilinear resistors will allow designers to develop extremely robust designs for a multitude of applications.

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I. INTRODUCTION

A. BACKGROUND

Digital Signal Processing (DSP) has made its indelible mark on the world of electronics. It appears that every form of electronics from computer and communications systems to music and children's toys have become laden with digital technology. "Digital" has become a word associated with quality, the state-of-the-art, and has turned into somewhat of a fashionable craze. However, the great incubus of the digital giant has been the analog world in which we live and with which it must interface.

A great multitude of digital systems require the ability to interface to the analog world. Analog signals are a necessity to communications systems in order to transmit and receive. Entertainment systems require an analog interface such that we can physically interpret audio and visual output. Internal to digital systems, analog-to-digital and digital-to-analog converters require analog filtering to reduce aliasing and minimize the negative effects of sampling. In short, the need for analog filtering has not been diminished by the move of electronics systems to digital implementations.

The General Immittance Converter (GIC) filter presented in this thesis is an analog filter that can be used to aid in the interface between the digital and analog worlds. The ability to place digital and analog components on the same integrated circuits (IC) has made this particularly attainable. The GIC filter has proven itself to be a robust design that is highly insensitive to component variation and well suited to VLSI implementation. Current technology also allows for the integration of bipolar – transistors-well suited for analog applications – and CMOS transistors – well suited for digital applications – on the same IC. This leads to applications with both superior analog and digital components, e.g. the best of both worlds.

B. OBJECTIVE

Research at the Naval Postgraduate School has been prolific in the area of the GIC filter. However, research into analog VLSI implementation of the filter has not had the same share of assiduity as the filter itself. Although many layouts have been designed

only a few have been fabricated. This thesis is an attempt to add to the analog VLSI body of knowledge at NPS by fabricating a BiCMOS version of the GIC filter. Because BiCMOS technology has never been incorporated in a VLSI design at NPS, it is the primary focus of this thesis. This will allow future analog VLSI researchers to tests and improve the BiCMOS design process. In addition to the BiCMOS design itself, researchers will be able to study the results from another VLSI layout in order to offer improvement techniques for future designers. Although the BiCMOS opamp improvement is the primary focus of this thesis, the secondary goal is to make other improvements to the VLSI design where possible.

C. RELATED WORK

Several previous theses have focused on the design and implementation of the GIC filter. The latest design was developed by LCDR Ralph Lee and fabricated by MOSIS in 2001. LCDR Lee's design is the basis for the improvements made in this thesis.

D. THESIS ORGANIZATION

Chapter II discusses all the necessary equations and background of the GIC Filter, including filters, opamps, and switched capacitors. Chapter III focuses on the BiCMOS opamp, the improvement made to the opamp, and a design problem found with the capacitors in LCDR Lee's design. Chapter IV then turns to discuss the implementation of switched capacitors in the bilinear resistor, to include a performance improvement made on the switches (passgates.) The programmable logic is detailed in Chapter V, while the final filter design and chip layout are covered in Chapter VI. Finally, Chapter VII focuses on recommendations and conclusions.

II. THE SWITCHED CAPACITOR GIC FILTER

The programmable switched-capacitor GIC filter can be decomposed into several sub components. The purpose of this chapter is to give an overview of the major subcomponents and to provide a cursory review of the necessary theory.

A. FILTER

The GIC Filter is composed of two major components, each of which is comprised of several elements or subcomponents. The first major component of the filter is the operational amplifier and the second is the bilinear resistor. This section will begin with an overview of filter basics. Next, the operational amplifier is covered and finally, the overall circuit design is discussed.

1. Filter Basics

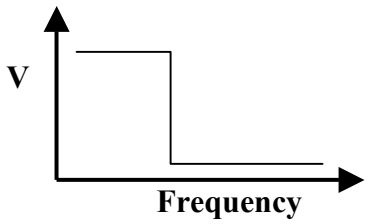
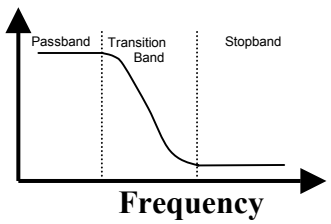
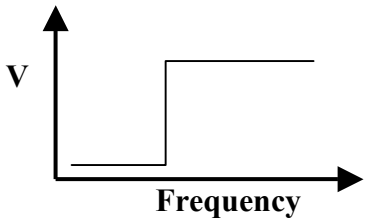
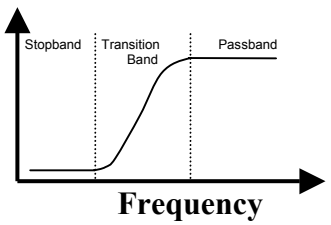
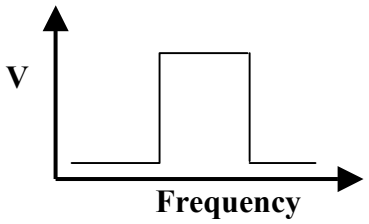
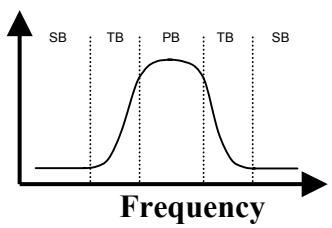
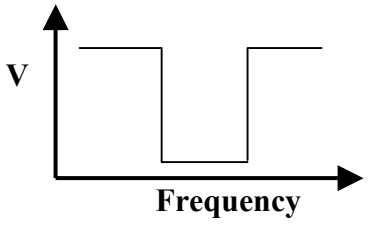
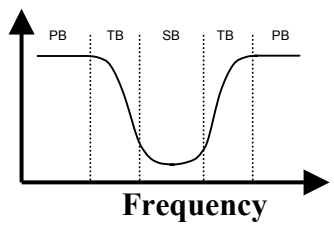
Electronic filters are used to select or reject certain frequency content from an electric signal. This is accomplished by using circuits that take advantage of the frequency responses of its components. Frequency selection is accomplished by adjusting the signal level such that the magnitude of the desired frequencies of the signal are much greater than that of the undesired frequencies. This can be achieved by amplifying the desired portion, attenuating the undesired portion, or a combination of both.

Table 2.1 contains a summary of the basic filter types. The figures in the table depict the ideal and non-ideal response characteristics of the four basic filter types. Desirable frequencies are resident in the passband while undesirable frequencies are located in the stop band. Ideal filters have a perfect transition between the passband and the stopband. Although, ideal filters cannot be realized, their concepts aid in filter analysis. Non-Ideal filters, unlike their ideal counterparts, do not transition perfectly but have a transition band from the passband to the stopband.

Non-ideal filters are represented mathematically by an s-domain transfer function, also shown in the table. A transfer function can be analyzed to determine the

characteristics of the filter. The general form of the equation can narrow the filter type into one of the four basic types in the table. In addition, the transition frequencies (cut-off frequencies) can be determined by ω_p. The quality factor, Q_p (a number that determines the sharpness of the filter at the transition band,) can also be determined from the general equation.

Table 2.1. Filter Response Summary (after Lee, 2000).

Ideal Frequency Response	Non-Ideal Frequency Response	Non-Ideal Transfer Function
Low Pass		
		$T(s)=\frac{a_0}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
High Pass		
		$T(s)=\frac{a_2 s^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Band Pass		
		$T(s)=\frac{a_1 s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Notch		
		$T(s)=\frac{s^2+\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$

The frequency response of a bandpass filter is used in Figure 2.1 to demonstrate how the quality factor determines the sharpness of the filter. For the bandpass filter, a larger quality factor produces a sharper, narrower filter.

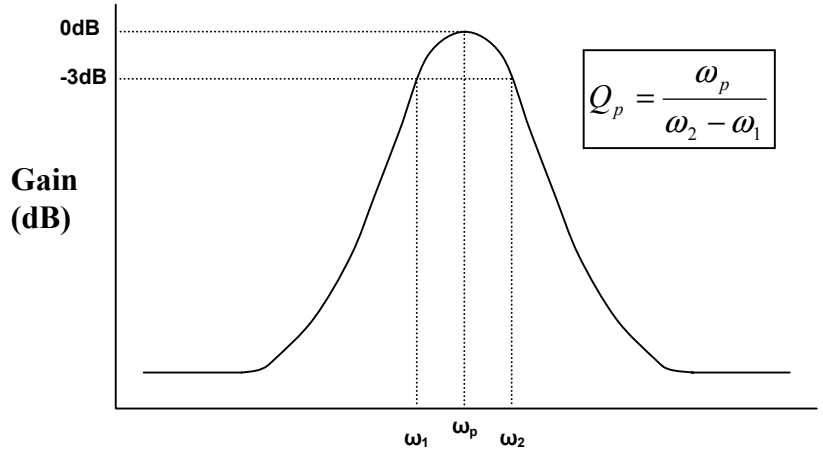


Figure 2.1. Quality Factor for a Bandpass Filter (after Lee, 2000).

2. Operational Amplifier

The simplest of filters are realized using passive components such as resistors, capacitors and inductors. More sophisticated filters use active components such as operational amplifiers in addition to the passive components. The GIC Filter is realized using a combination of operational amplifiers, capacitors, and resistors.

Operational amplifiers have several characteristics that are used to measure their performance with other amplifiers. The most distinguishing opamp characteristics are gain, bandwidth, slew rate, and offset voltage. In order to determine how well the opamp performs, it is typically compared with the ideal opamp. The most common opamp symbol is depicted in Figure 2.2.

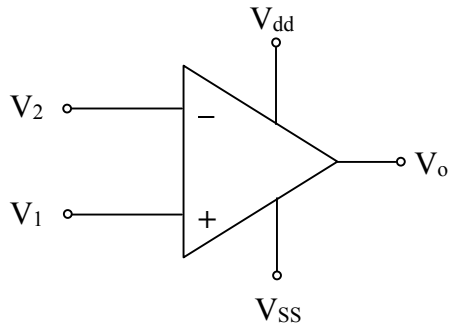


Figure 2.2. Opamp Circuit Symbol (after Lee, 2000).

The gain and the bandwidth are the most limiting factors of the opamp frequency response characteristics. The open loop gain for an opamp is defined by the following equation (Sedra, 1998)

$$A = \frac{V_o}{(V_1 - V_2)} \qquad \text{(Eq. 2.1)}$$

The ideal opamp has an infinite open loop gain, which can be seen from Equation 2.1 when V1 = V2.

The bandwidth determines the operating range of frequencies in which the opamp functions. The ideal opamp has a constant gain over all frequencies; the non-ideal opamp does not. Figure 2.3 depicts the frequency response of a typical non-ideal opamp. The gain begins at 100 dB and begins to drop off around 10 Hz where it has lowered by 3 dB. The 3 dB points in a frequency response are commonly used to determine the cut-off frequencies of filters. Past the 3 dB point, the response declines at a rate of 20 dB per decade. The intercept point on the frequency axis determines the bandwidth of the amplifier. The bandwidth of the figure is near 1 MHz. The gain and bandwidth are typically multiplied together to form the gain bandwidth product (GBWP), a figure of merit that defines the performance of any amplifier. Opamps with a higher GBWP typically perform better in most applications; therefore, they are more desirable.

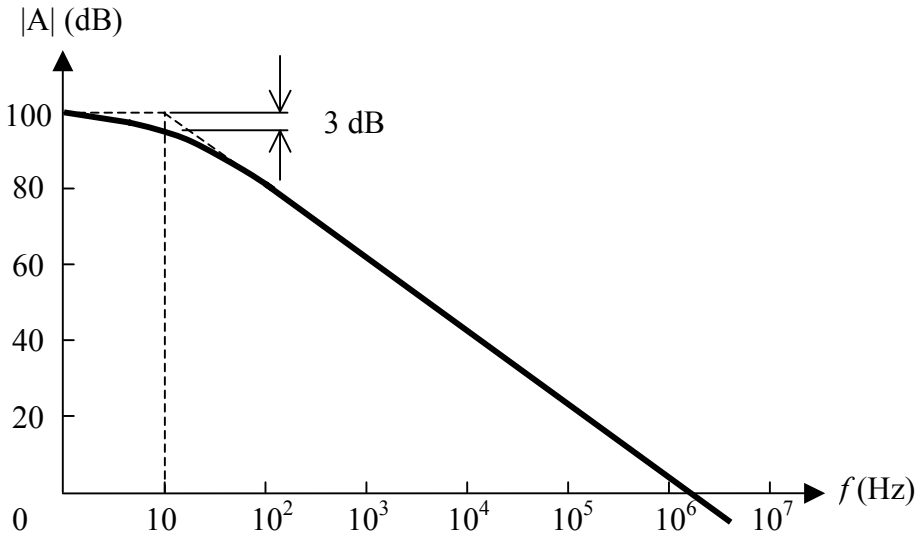


Figure 2.3. Non-Ideal Opamp Frequency Response (from Lee, 2000).

The slew rate is another limitation of the non-ideal opamp. If an opamp is configured for unity gain, the input should ideally follow the output. However, this is not the case with a non-ideal opamp. Figure 2.4 depicts the distortion that can result from a non-ideal opamp due to its slew rate limitation.

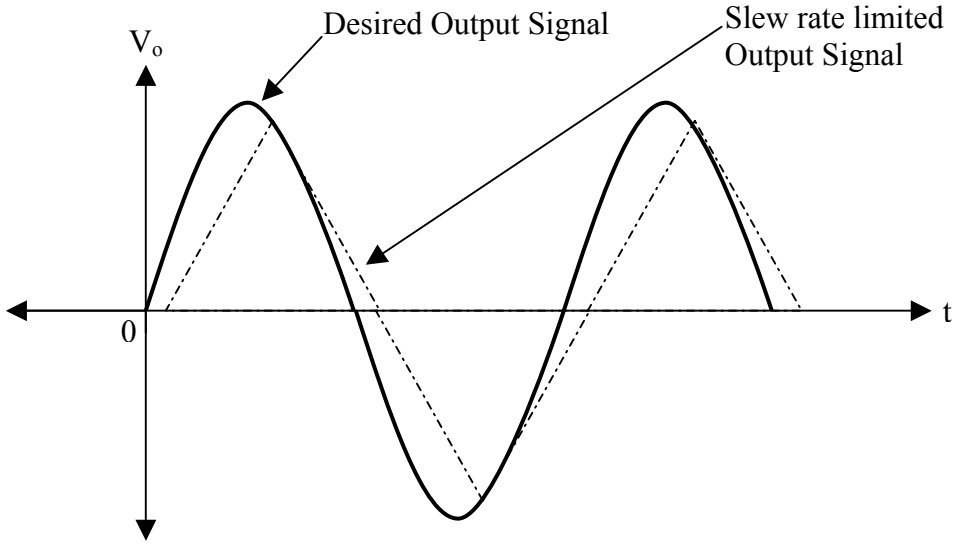


Figure 2.3. Non-Ideal Opamp Frequency Response (from Lee, 2000).

The slew rate is defined by the following equation (Sedra, 1998)

$$SR = \left.\frac{dV_o}{dt}\right|_{\max} \qquad \text{(Eq. 2.2)}$$

The slew rate limitation typically causes distortion at a frequency higher than a certain value. The following equation is a measure of the frequency at which slew rate distortion causes severe non-linearity (Figure 2.3 depicts this distortion.)

$$f_M = \frac{SR}{2\pi \hat{V}_{O\max}} \qquad \text{(Eq. 2.3)}$$

Another limitation of non-ideal opamps is offset voltage. Offset voltage is simply a DC error voltage added to the output signal.

3. Switched Capacitors and the Floating Bilinear Resistor

Fabricating accurate resistors on silicon has proven to be a difficult task for IC designers. Standard IC resistors are made by using the resistance properties of long zigzagged lengths of semiconductors or other material. However, the resistance of the same design can vary considerably for each fabrication. Although a circuit is designed to be identical for each fabrication, this variation can lead to circuits with a wide degree of possible frequency responses. The switched capacitor is one method developed to solve this problem (Sedra, 1998.)

Switched capacitor circuits rely on the properties of certain configurations of switches and capacitors. If a capacitor is switched between two circuit nodes at a high enough frequency it acts like a resistor. The accuracy of capacitors is considerably better than that of resistors in IC processing. However, this smaller resistance can still lead to frequency deviation if the design is sensitive to resistor values. Although, if the circuit to be realized is arranged in such a manner that its frequency responses are dependent on a ratio of resistors, then considerable improvements to the circuit can be made. This is because standard IC processes can control capacitor ratio variation to 0.1% (Sedra, 1998.) The GIC filter makes use of this property by using a transfer function that is dependant on a ratio of capacitors and resistors.

A floating bilinear resistor is constructed by using the resistive properties of switches and a capacitor in a certain circuit arrangement. This arrangement is especially useful because it does not have to be grounded and can be directly substituted for a standard resistor. Figure 2.4 depicts a bilinear resistor. The subscripts after the Greek letter phi in the figure indicate the switch timing. The subscript "e" denotes even, and the "o" denotes odd. The even and odd clock pulses control the switch position, are out-of-phase, and non-overlapping (the odd and even controlled switches are never closed at the same time.)

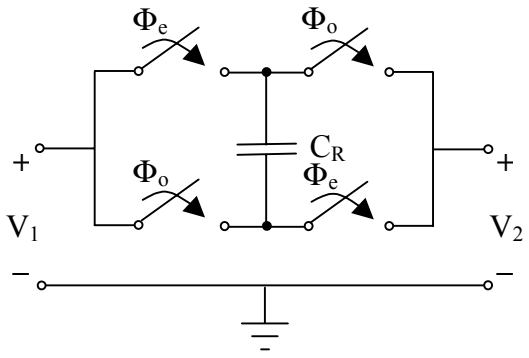


Figure 2.4. Floating Bilinear Resistor (from Lee, 2000).

In order to analyze the bilinear resistor, the bilinear transformation and the admittance of each circuit element is required. Because the bilinear resistor is a sampled system, it is necessary to analyze its admittance in the z-domain. The bilinear transformation is given by (Kubicki, 1999)

$$s = \frac{2}{T}\frac{z-1}{z+1} \qquad \text{(Eq. 2.3)}$$

where $s=j\omega$, $z= e^{s\tau}$, and τ is the clock period. The equivalent admittance for the bilinear resistor in the figure is (Kubicki, 1999)

$$y_R = C\left(1+\hat{z}^{-1}\right) \qquad \text{(Eq. 2.4)}$$

where $\hat{z} = e^{\frac{s\tau}{2}}$.

Table 2.2. Laplace and Z Domain Equivalent Admittances (from Lee, 2000).

	Circuit Element		
	Capacitor	**Resistor**	**Inductor**
Laplace Domain Admittance	sC	G	1/sL
Z-Domain Admittance after Bilinear Transform	$C\left(1-z^{-1}\right)$	$\frac{G\tau}{2}\left(1+z^{-1}\right)$	$\frac{\tau^2}{4L}\frac{\left(1+z^{-1}\right)^2}{1-z^{-1}}$

Setting the admittance for a resistor in the table above equal to the admittance for the bilinear resistor in Equation 2.4 gives (Lee, 2000)

$$C\left(1+z^{-1}\right)=\frac{G\tau\left(1+z^{-1}\right)}{2} \qquad \text{(Eq. 2.5)}$$

for a half clock cycle. Solving for the resistor admittance gives (Lee, 2000)

$$G=\frac{2C}{\tau} \qquad \text{(Eq. 2.6)}$$

For the full clock cycle, the equivalent admittance of the bilinear resistor becomes

$$G=\frac{4C}{\tau} \qquad \text{(Eq. 2.7)}$$

4. GIC Filter

Previous research has demonstrated that the GIC filter is an excellent filter. It is easily converted between topologies with the addition of minimal switches and it is relatively insensitive to component variation (Lee, 2000.) Figure 2.5 depicts the basic GIC filter. The Y's in the figure denote the admittance of the elements represented by each of the eight rectangular boxes. By carefully choosing the appropriate element for each box, filter topology can be easily selected.

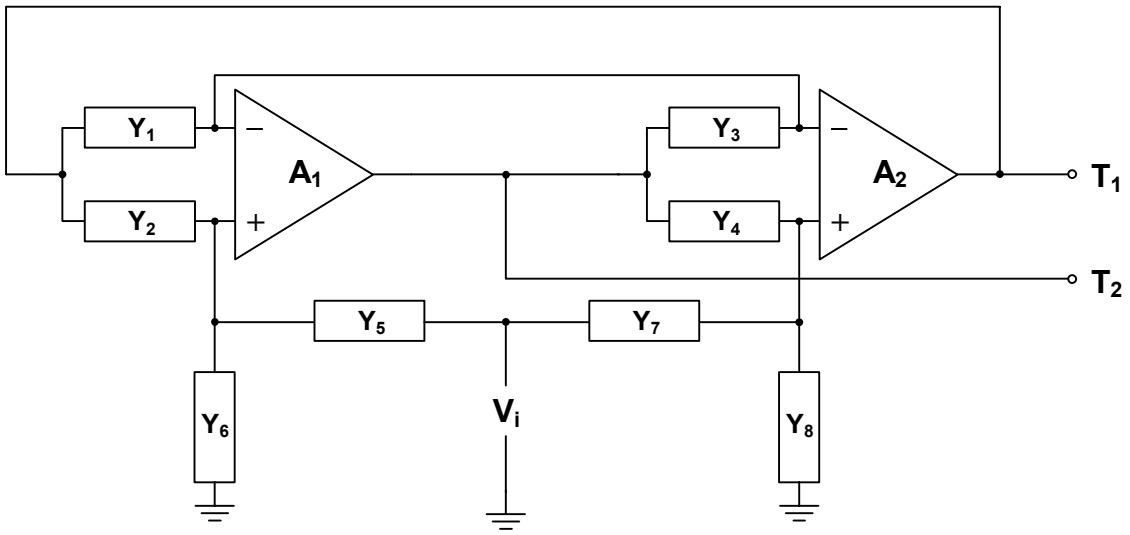


Figure 2.5. Basic GIC Filter (from Lee, 2000).

The transfer functions for the GIC filter are as follows (Lee, 2000)

$$T_1 = \frac{V_1}{V_i} = \frac{Y_1Y_4Y_5 + Y_3Y_7(Y_2 + Y_6) - Y_3Y_5Y_8}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)} \qquad \text{(Eq. 2.8)}$$

$$T_2 = \frac{V_2}{V_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)} \qquad \text{(Eq. 2.9)}$$

Choosing appropriate elements and substituting the proper admittance for each element into the transfer functions in Equations 2.8 and 2.9 yields transfer functions representing the four filter types. Table 2.3 depicts the transfer functions and admittance selection for each of the eight elements.

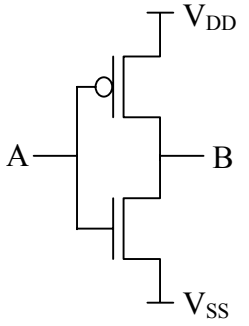
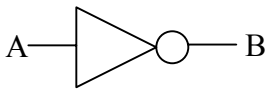
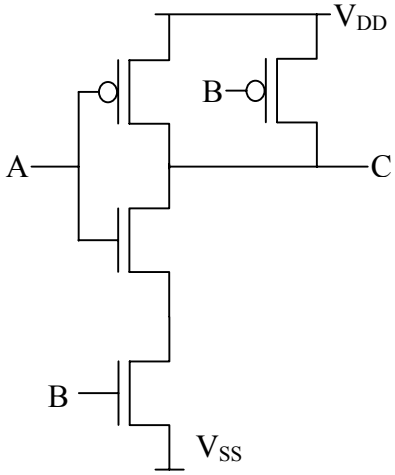
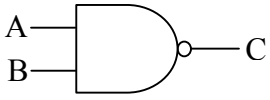
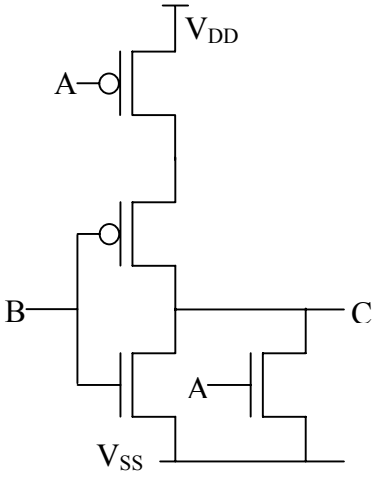
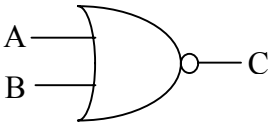
Table 2.3. Admittance Selection and Transfer Functions (from Lee, 2000).

Filter Type	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Transfer Function
Low-Pass	G	sC	$sC+\frac{G}{Q_p}$	G	G	0	0	G	$T_2=\frac{2\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
High-Pass	G	G	sC	G	0	G	C	$\frac{G}{Q_p}$	$T_1=\frac{2s^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Band-Pass	G	G	sC	G	0	G	$\frac{G}{Q_p}$	C	$T_1=\frac{2\frac{\omega_p}{Q_p}s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Notch	G	G	sC	G	G	0	C	$\frac{G}{Q_p}$	$T_2=\frac{s^2+\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$

B. PROGRAMMABLE LOGIC

Digital logic can be used to control filter topology, quality factor, and center frequency. By controlling switches with logic gates, the filter can be programmed to the desired frequency response. Input controls are used to drive inverters, NAND gates, and NOR gates, which in turn open or close switches. Thus, with careful switch placement, circuit components can be connected in different configurations. Table 2.4 depicts the circuit diagrams and truth tables for the basic logic gates used in this thesis.

Table 2.4. Digital Logic Summary.

	Transistors	Circuit Symbol	Truth Table
Inverter			A | B 0 | 1 1 | 0
NAND			A | B | C 0 | 0 | 1 0 | 1 | 1 1 | 0 | 1 1 | 1 | 0
NOR			A | B | C 0 | 0 | 1 0 | 1 | 0 1 | 0 | 0 1 | 1 | 0

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III. BICMOS OPERATIONAL AMPLIFIER

The central component of the GIC Filter is the operational amplifier (opamp.) The opamp design is therefore the most meaningful place to start if one wishes to improve the response characteristics of the GIC Filter. Although there are many avenues by which one may improve amplifier designs, BiCMOS technology was chosen to improve the GIC filter performance in this research.

BiCMOS technology can make opamp improvements possible by adding the capabilities of bipolar transistors to standard CMOS designs. Because bipolar transistors have a larger transconductance than their CMOS equivalents, they can produce opamps with a larger Gain Bandwidth Product (GBWP) – arguably the most important opamp characteristic. Bipolar transistors are limited in that they do not have a high input impedance like their CMOS equivalents. In addition to this, BiCMOS technology requires more advanced process techniques leading to additional steps in the fabrication process (Sedra, 1998.)

Previous GIC filter designs at the Naval Postgraduate School have always been based on CMOS technology. Therefore, this is the first attempt to design and fabricate a filter composed of BiCMOS amplifiers. The focus of this design lies in two areas: first, improving the characteristics of past designs and second, making the design simple and easy to implement such that proof of concept can be achieved.

Considering these criteria, two basic opamp designs were analyzed for operating characteristics such that the best one could be chosen for the GIC filter design. This chapter begins by analyzing both designs. Next, the design criteria are used to narrow the selection. Then, the best design is selected and the VLSI layout of the selected amplifier is discussed. Finally, the best design is summarized.

A. CIRCUIT CONFIGURATIONS

1. Sone and Yotsuyanagi Configurations

The first BiCMOS operational amplifier design was derived from "Design Techniques for Analog BiCMOS Circuits" by Kazuya Sone and Michio Yotsuyanagi.

Figure 3.1 shows the original configuration with all CMOS transistors. One CMOS differential pair at a time is replaced with one BJT pair to form the circuits in Figures 3.2 through 3.4. Although the bottom rail in all configurations was presented in the paper as "ground," all simulations used a bottom rail voltage such that $V_{SS} = - V_{DD}$. The current source in all the simulations was set to 50 mA, all resistors were set to 400 Ω, and V_{DD} was set to 5 V.

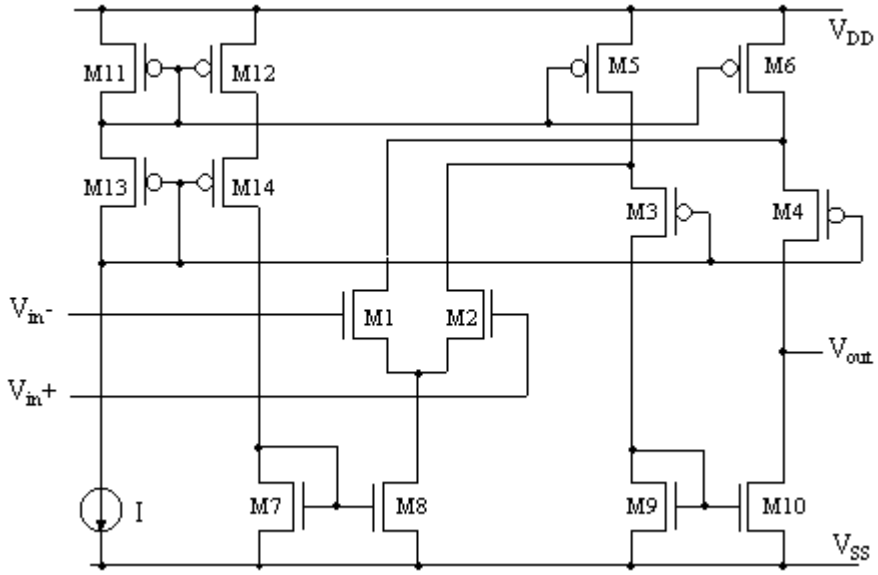

Figure 3.1. Sone and Yotsuyanagi Configuration A.

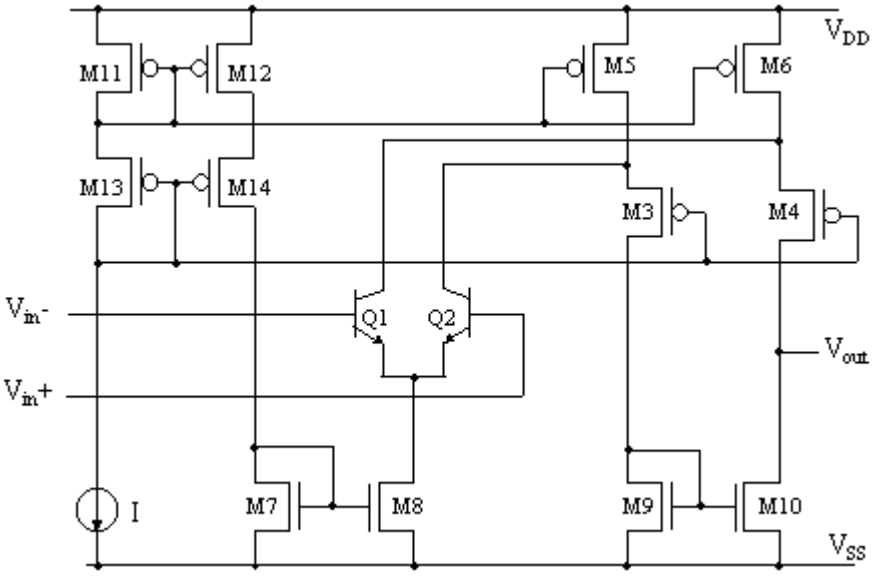

Figure 3.2. Sone and Yotsuyanagi Configuration B.

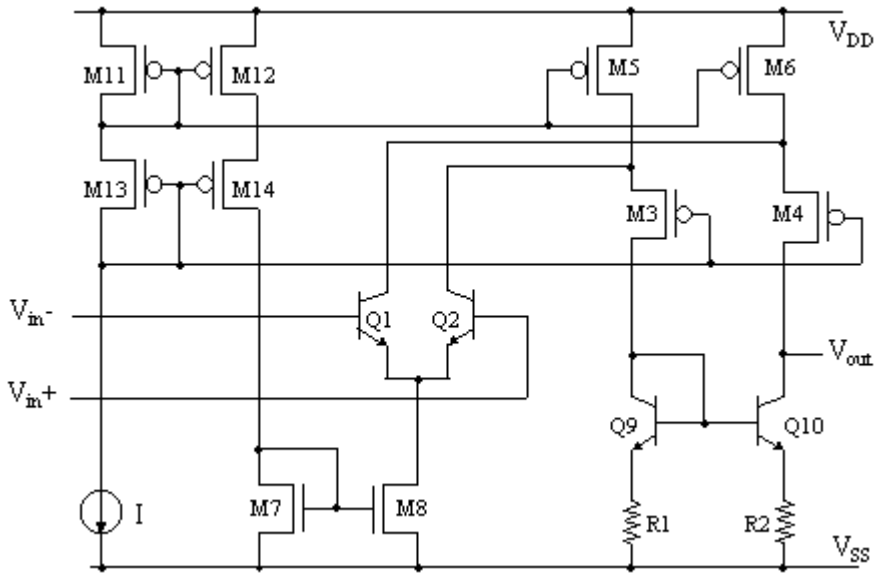

Figure 3.3. Sone and Yotsuyanagi Configuration C.

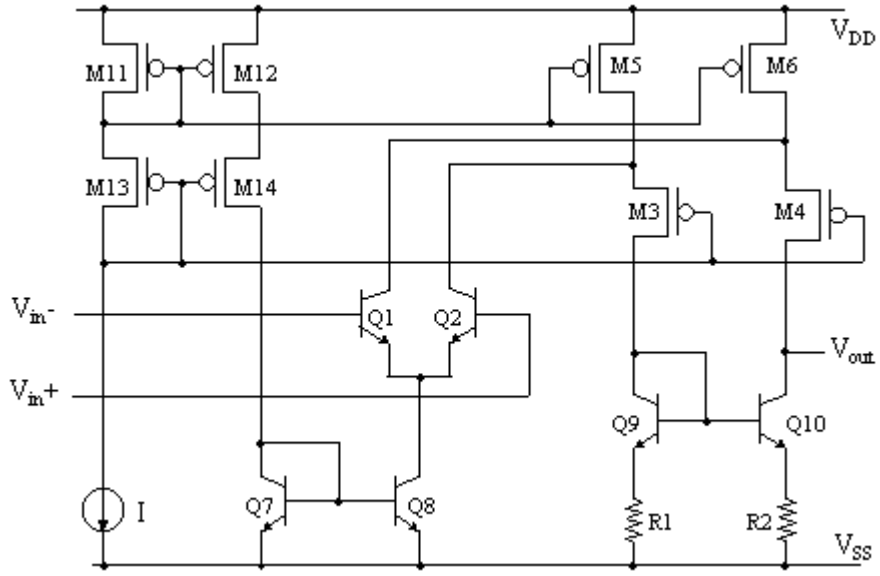

Figure 3.4. Sone and Yotsuyanagi Configuration D.

2. Lee Configurations

The second operational amplifier design was derived from Lee's programmable GIC filter (Lee, 2000.) Figure 3.5 is the circuit layout for the original CMOS design in Lee's filter. Figures 3.6 and 3.7 are the modified BiCMOS versions of the circuit.

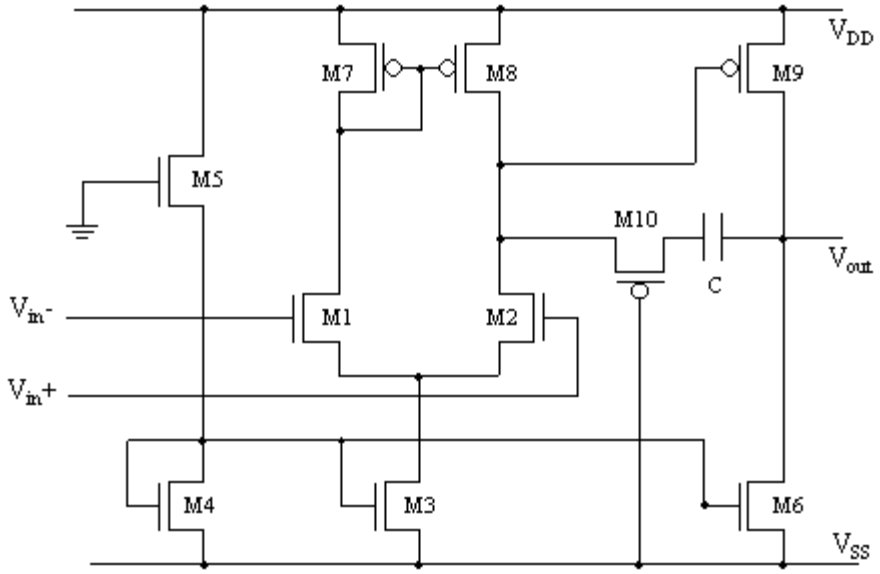

Figure 3.5. Lee Configuration A.

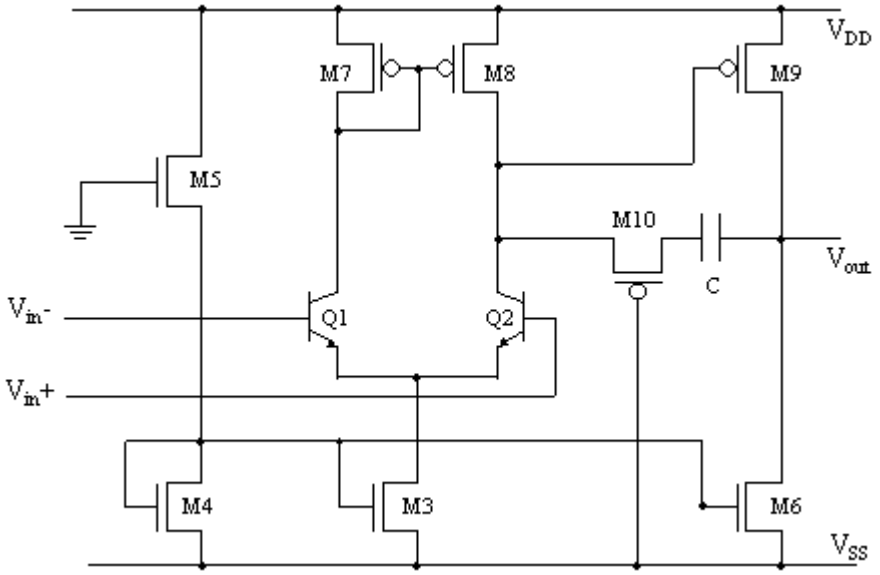

Figure 3.6. Lee Configuration B.

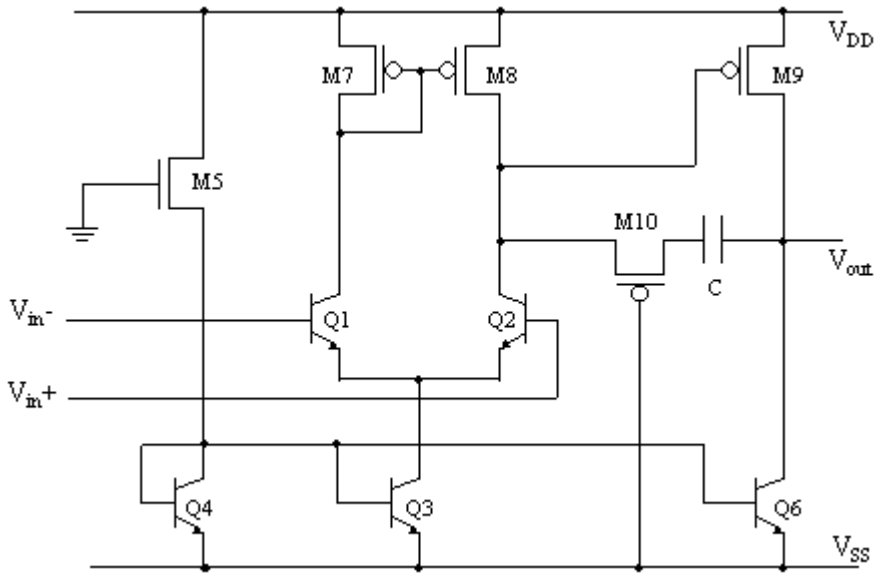

Figure 3.7. Lee Configuration C.

B. TRANSISTOR SIZES

Tables 3.1 and 3.2 contain a summary of all the changes made to both original circuit configurations. In addition to the changes, the tables also contain all the transistor sizes used in simulation. All NPN bipolar transistors are sized as default Spice transistors.

Table 3.1. Sone & Yotsuyanagi Transistor Sizes.

Original Configuration			Changes to Original Configuration		
	W	L	B	C	D
M1	100	2	Q1	Q1	Q1
M2	100	2	Q2	Q2	Q2
M3	240	2			
M4	240	2			
M5	480	2			
M6	480	2			
M7	50	2			Q7
M8	200	2			Q8
M9	100	2		Q9	Q9
M10	100	2		Q10	Q10
M11	120	2			
M12	120	2			
M13	120	2			
M14	120	2			

Table 3.2. Lee Transistor Sizes.

Original Configuration			Changes to Original	
	W	L	B	C
M1	33	5	Q1	Q1
M2	33	5	Q2	Q2
M3	27	5		Q3
M4	13	5		Q4
M5	5	33		
M6	67	5		Q6
M7	30	5		
M8	30	5		
M9	150	5		
M10	5	5		

C. OPEN LOOP GAIN

Figures 3.8 and 3.9 above show the frequency response of the Sone configurations A and B. It can be seen from the figures that the replacement of the input pair of transistors (M1 and M2) has increased the DC gain but decreased the 3dB point, though their product still increases the Gain Bandwidth Product.

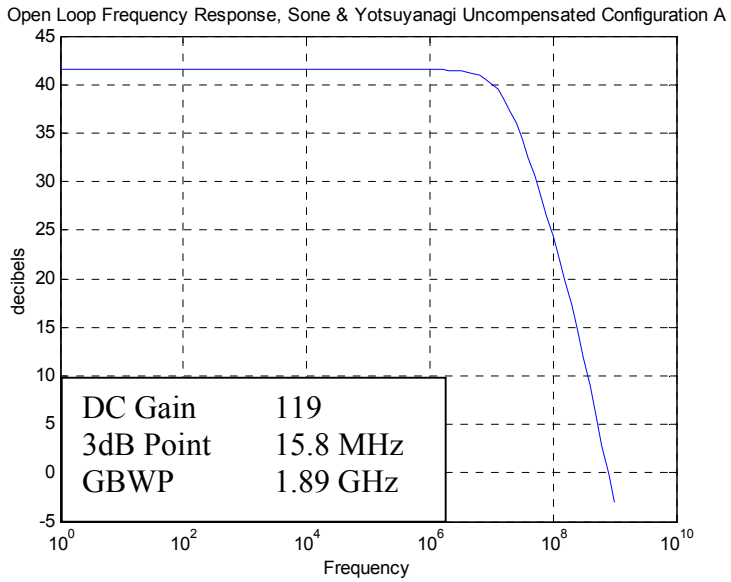

Figure 3.8. Frequency Response, Sone Configuration A.

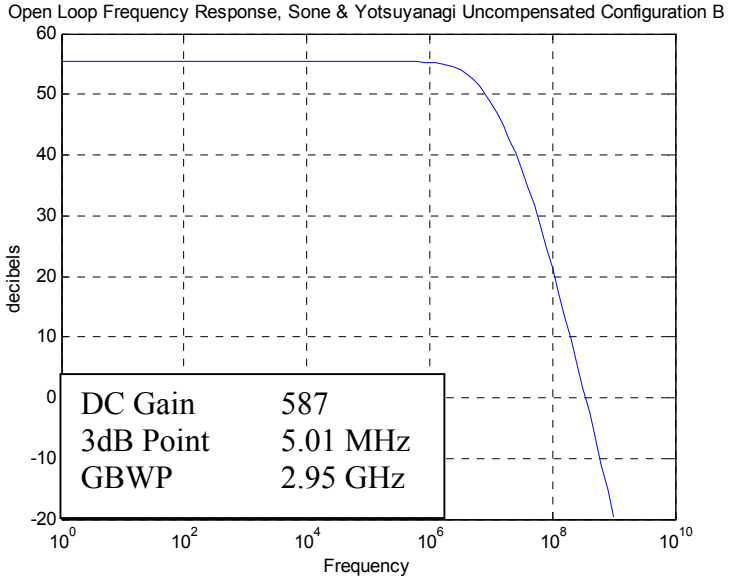

Figure 3.9. Frequency Response, Sone Configuration B.

Figures 3.10 and 3.11 show the frequency response of the Sone configurations C and D. It can be seen from the figures that the replacement of the second pair of transistors (M9 and M10) has increased the DC gain, increased the 3dB Point, and increased the GBWP. The replacement of the third pair (M7 and M8) further increases the 3dB Point but the DC gain and the GBWP drop back down nearer to the CMOS configuration (configuration A.)

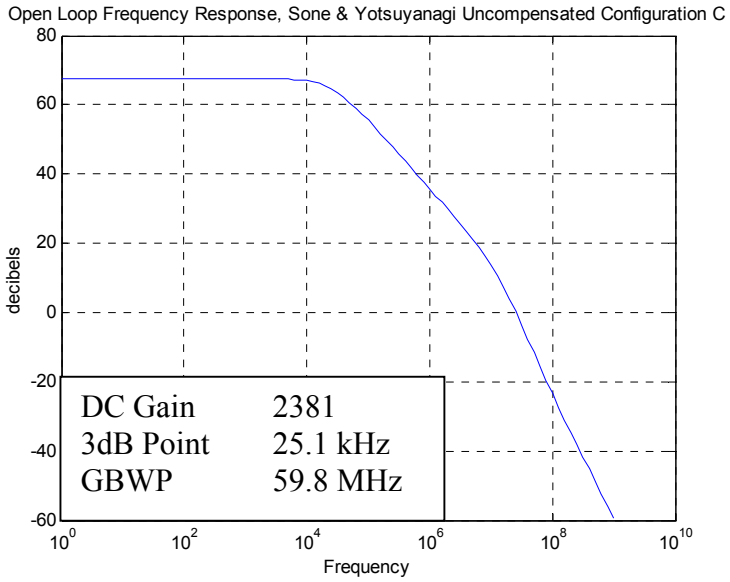

Figure 3.10. Frequency Response, Sone Configuration C.

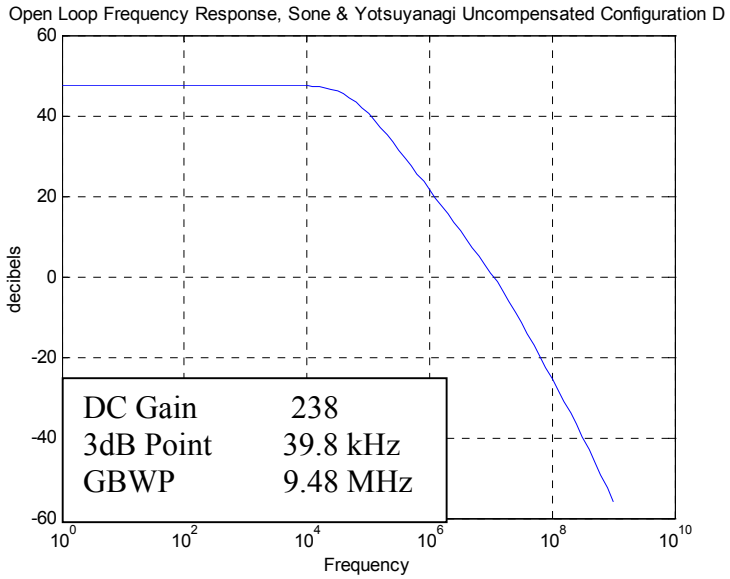

Figure 3.11. Frequency Response, Sone Configuration A.

Figures 3.12 and 3.13 show the frequency response of the Lee configurations A and B. The replacement of the input pair of transistors (M1 and M2) from configuration A has increased all three of the performance indicators. The replacement of the additional transistors (Configuration C, not shown here) reduces the GBWP to less than that of the original configuration (configuration A,) due to changes in the bias points.

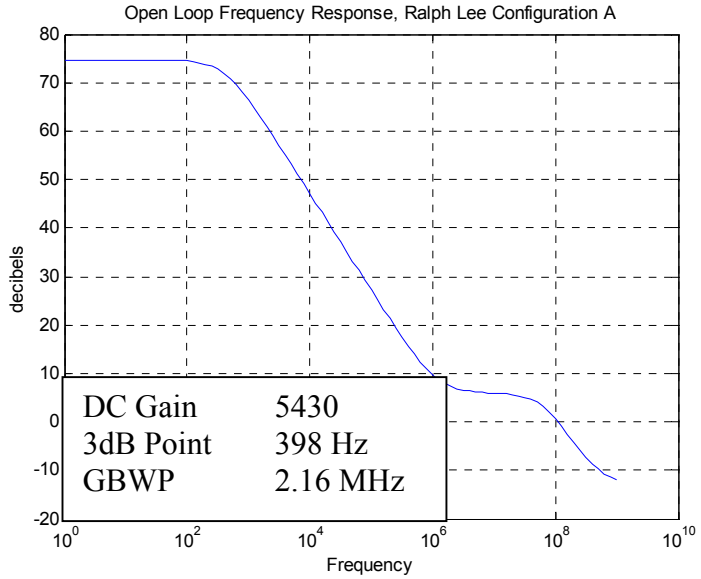

Figure 3.12. Frequency Response, Lee Configuration A.

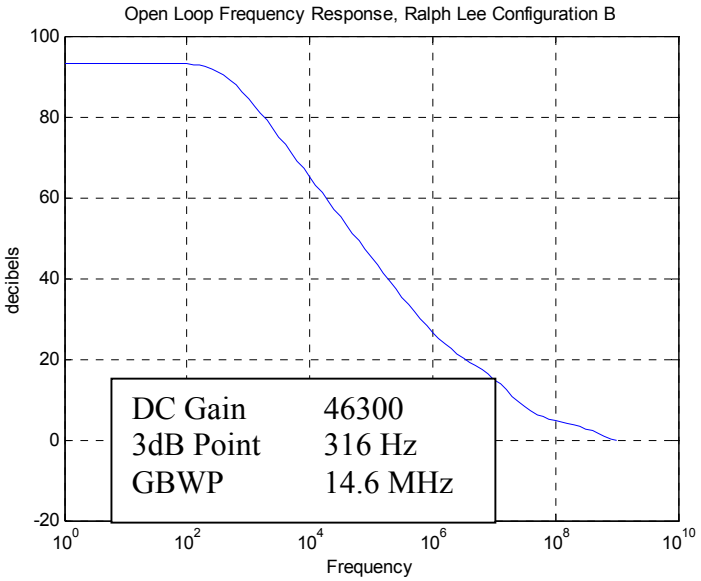

Figure 3.13. Frequency Response, Lee Configuration B.

Replacing the input pair on both the Sone and Lee original designs greatly enhances the performance of the respective operational amplifiers. In the Sone opamp, the replacement of the second pair (configuration C) also increases the performance. In both the Sone and Lee amplifiers the addition of the final NPN transistors increases the 3dB point but greatly reduces the DC gain. Figure 3.14, Figure 3.15 and Table 3.3 summarize these results.

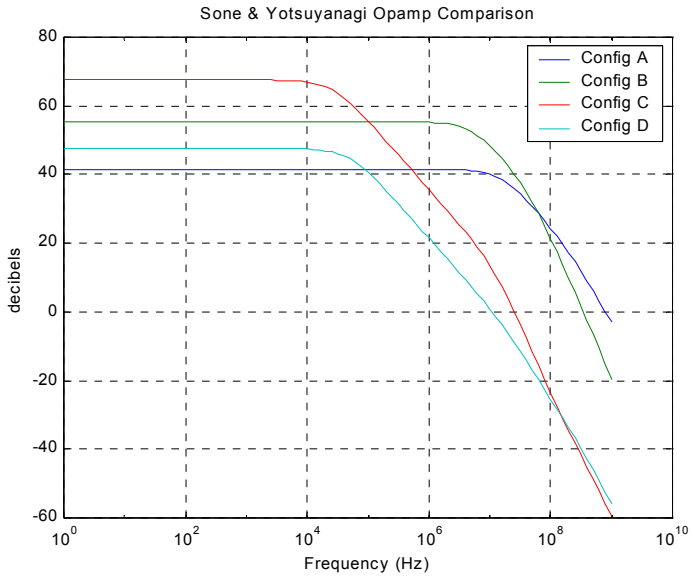

Figure 3.14. Operational Amplifier Comparison.

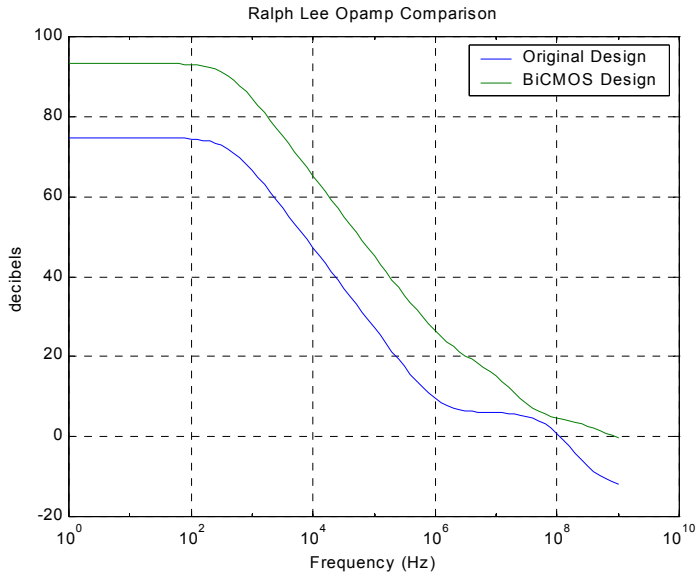

Figure 3.15. Operational Amplifier Comparison.

Table 3.3. Summary of Performance Indicators.

	DC Gain	3 dB Point	GBWP
Sone & Yotsuyanagi Config A	119	15.8 kHz	1.89 GHz
Sone & Yotsuyanagi Config B	588	5.01 MHz	2.95 GHz
Sone & Yotsuyanagi Config C	2,380	25.1 kHz	59.8 MHz
Sone & Yotsuyanagi Config D	238	39.8 kHz	9.49 MHz
Lee Configuration A	5,430	398 Hz	2.16 MHz
Lee Configuration B	46,300	316 Hz	14.6 MHz
Lee Configuration C	278	6.3 kHz	1.75 MHz

In consideration of the performance parameters, the best opamp from both design was chosen for further testing. From this point on, only the Sone & Yotsuyanagi configuration C will be used and referred to as the Sone configuration and only the Lee configuration B will be used and will be referred to as the Lee configuration.

D. CLOSED LOOP GAIN

Both operational amplifiers were arranged in the configuration shown in Figure 3.16 to analyze the closed loop gain.

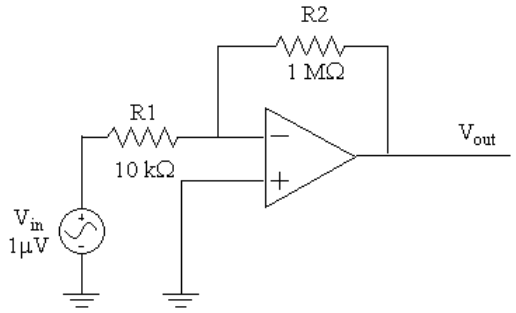

Figure 3.16. Closed Loop Gain Configuration.

Figure 3.17 compares the frequency response of the Lee configuration and the Sone configuration. The gain of the circuit in Figure 3.16 is 100, or 40 dB. The Lee response attains a 40 dB gain and has a GBWP of 12.5 MHz -- still fairly close to the open loop GBWP as expected. The Sone configuration, on the other hand, has some problems. First, the GBWP has increased to 20 GHz or 10 times the open loop GBWP. In addition to this, it does not attain the 40 dB benchmark (it only reaches 39 dB.) There is also an undesirable dip in the amplitude responses between 1MHz and 10MHz.

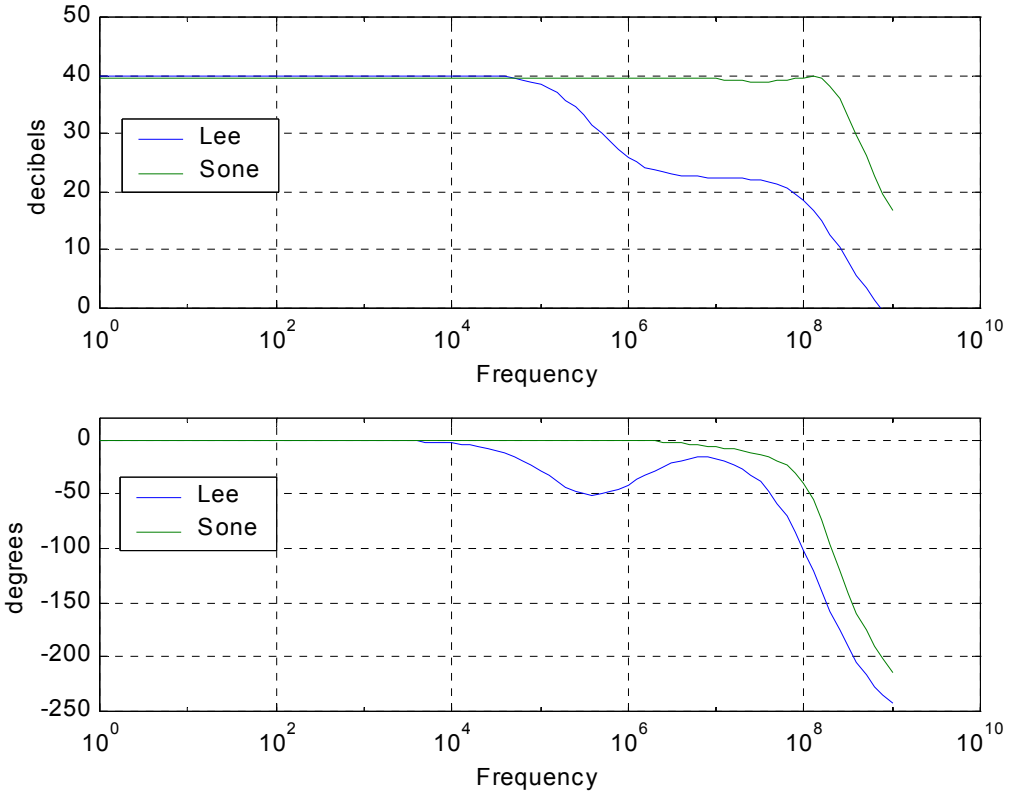

Figure 3.17. Bode Plot of Closed Loop System with Gain = 100.

From Figure 3.17, it is clear that the Sone configuration has erratic GBWP behavior, it does not reach the expected gain, and there is an undesirable perturbation between one and ten megahertz; therefore, it will not be analyzed further. Compensating the Sone model with a capacitor may help to stabilize the response, but would also reduce the GBWP. A study into compensating the amplifier may be of future value. Considering these factors, the Lee model has the best response characteristics and has been selected for use in the GIC Filter.

E. CAPACITOR SIZE

The compensating capacitor in the Lee model was varied in size from 1 aF to 1 nF to investigate the effect on the frequency response. The open loop configuration discussed in Section C of this chapter was used to analyze the response. Figures 3.18 and 3.19 show the frequency response for each capacitance value and a comparison of

capacitance and GBWP. Note that if the capacitor is large the GBWP is reduced. If the capacitor is small the GBWP approaches a limit that coincides with an uncompensated opamp. Although this range of capacitance is not necessarily plausible for VLSI design, it is a good "big picture" illustration of how the frequency response is affected relative to capacitance. Figure 3.18 focuses on the range of frequencies to be analyzed for the VLSI design.

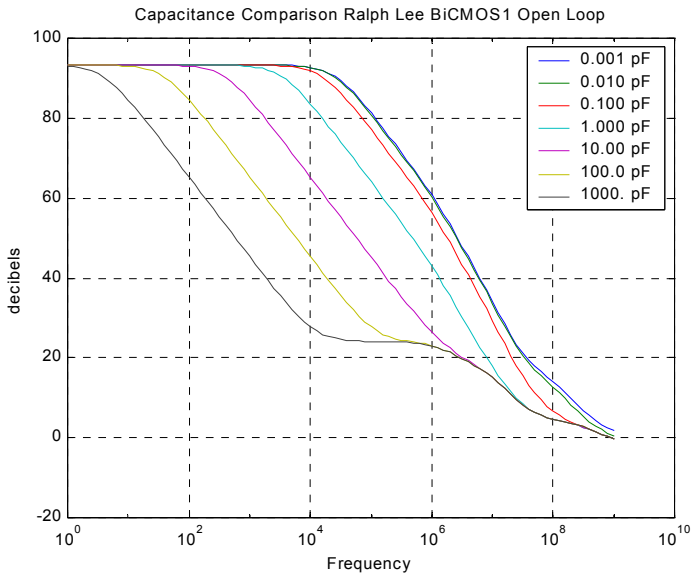

Figure 3.18. Response with Various Compensating Capacitors.

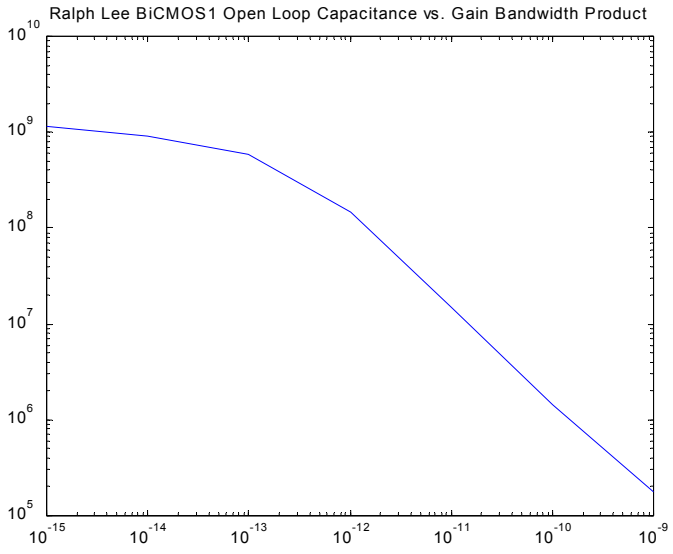

Figure 3.19. Capacitance vs. Gain Bandwidth Product.

As illustrated in Figure 3.20, the smaller the capacitor the better the response. The approach taken will be to select the smallest capacitor possible that still allows the amplifier to meet performance specifications during transient analysis. It should be noted that the "spike" in the phase plot, Figure 3.21, is due to the arctan function, which wraps around from –90º to +90º. Therefore, the spike is only a continuation of the downward slope of the phase response above 10 MHz.

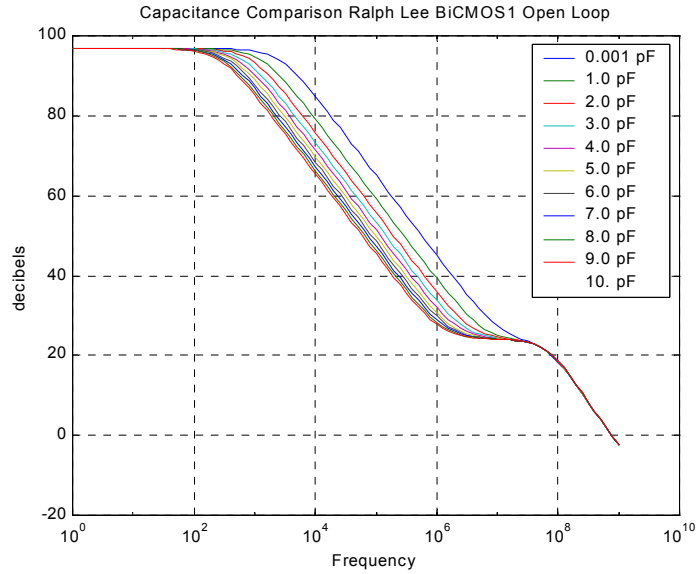

Figure 3.20. Frequency Response for 1pF to 10pF Capacitor.

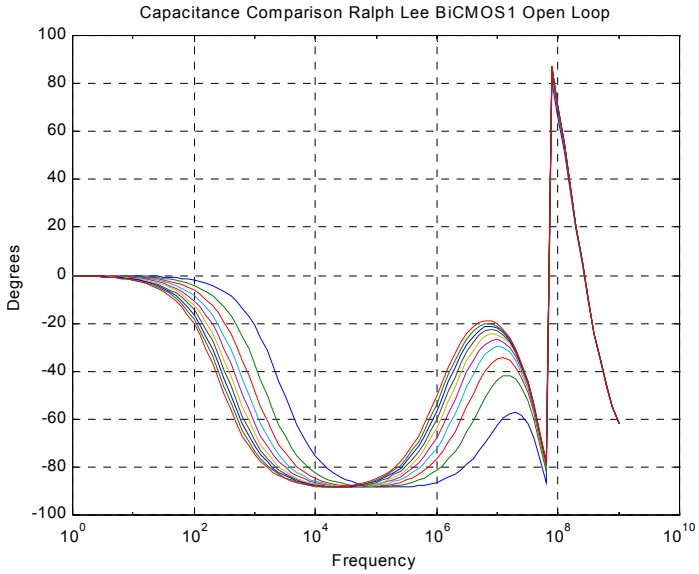

Figure 3.21. Phase Response for 1pF to 10pF Capacitor.

F. TRANSIENT ANALYSIS

Figure 3.22 is the standard slew rate configuration in which a large input square wave is used in a unity feedback loop to determine how much distortion is present in the output. The closed loop gain configuration used in Section D (Figure 3.16) was used for linearity testing.

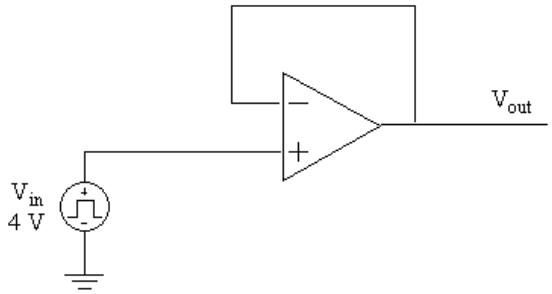

Figure 3.22. Slew Rate Configuration.

1. Slew Rate

An input square wave was generated at 250 kHz, 500 kHz, and 1 MHz. The output waveform is expected to be a square wave with the same frequency. The distortion between the input and output waveforms is the basis for the slew rate calculation. The slew rate is defined as the voltage deviation divided by the time period for that deviation. Figures 3.23, 3.24, and 3.25 demonstrate the output characteristics from the three input waveforms. Note that the 1 pF capacitor results in unstable circuit operation for all three frequencies. A larger capacitor results in a less distorted waveform, while a smaller capacitor produces a larger slew rate. Table 3.4 summarizes these results.

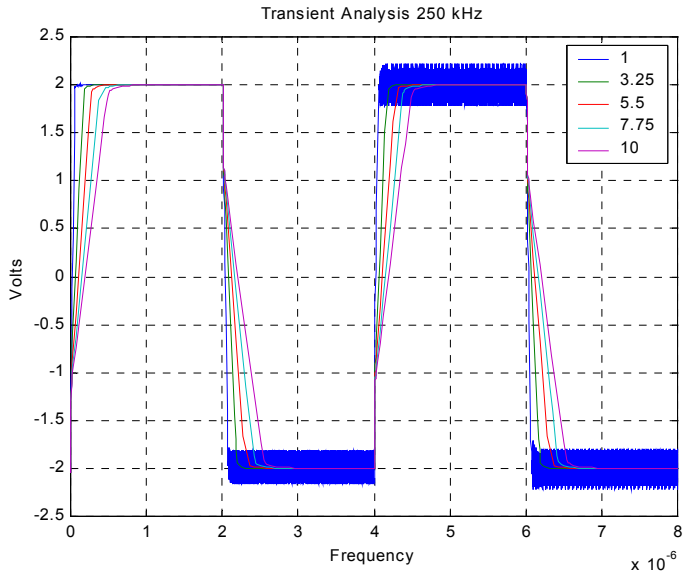

Figure 3.23. Slew Rate Analysis for Varying Capacitors.

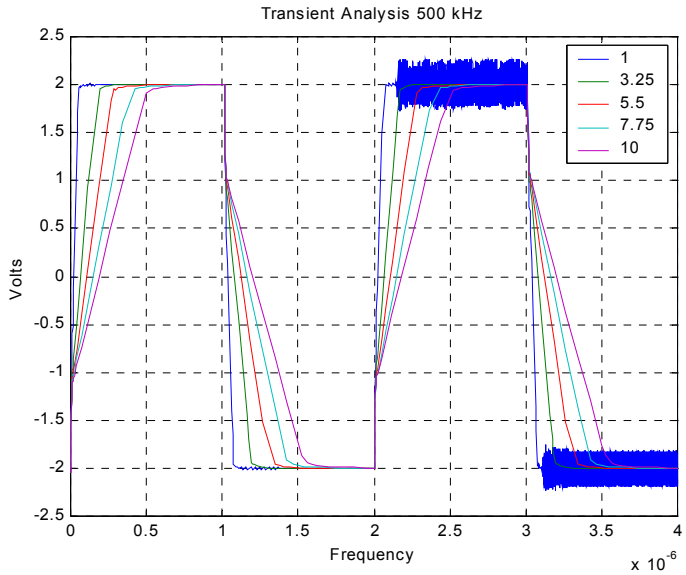

Figure 3.24. Slew Rate Analysis for Varying Capacitors.

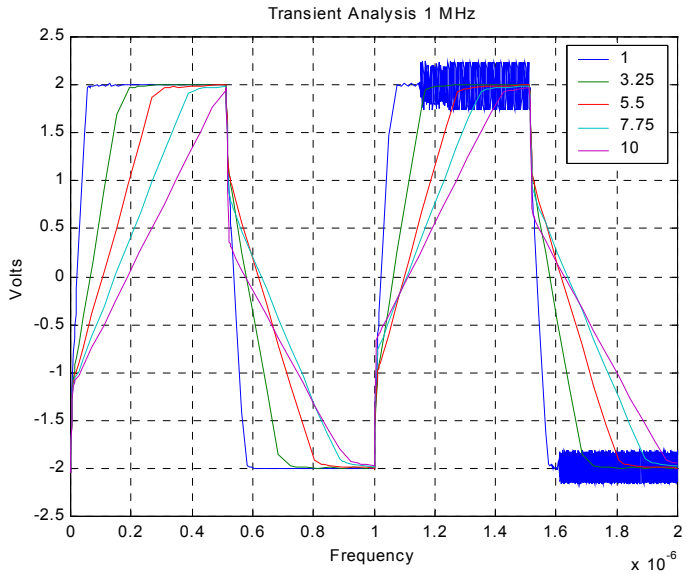

Figure 3.25. Slew Rate Analysis for Varying Capacitors.

Table 3.4. Slew Rate for Varying Frequency and Capacitor Values.

	250 kHz	500 kHz	1 MHz	Notes
1.00 pF	60 V/µs	60 V/µs	140 V/µs	Unstable
3.25 pF	20 V/µs	20 V/µs	40 V/µs	
5.50 pF	12 V/µs	10 V/µs	10 V/µs	
7.75 pF	7.5 V/µs	7.5 V/µs	8.0 V/µs	
10.0 pF	6.0 V/µs	6.0 V/µs	7.0 V/µs	

2. Linear Response and Offset Voltage

A 3.25 pF capacitor was selected because it produces the smallest distortion without instability and generates a reasonable slew rate. Therefore, the opamp now being tested is the Lee configuration B with a 3.25 pF compensating capacitor. The sinusoidal outputs in Figures 3.26 and 3.27 were produced from sinusoidal inputs at the same frequency; therefore, linearity between input and output holds very well. The offset voltage for the 1kHz signal is 0.25V. This offset was derived from a circuit with a gain of 100 (Figure 3.16,) therefore the input offset voltage is 2.5mV. The offset voltage for the 500 kHz signal is 0.3 V. Through a similar extrapolation the input offset voltage is 3.0mV.

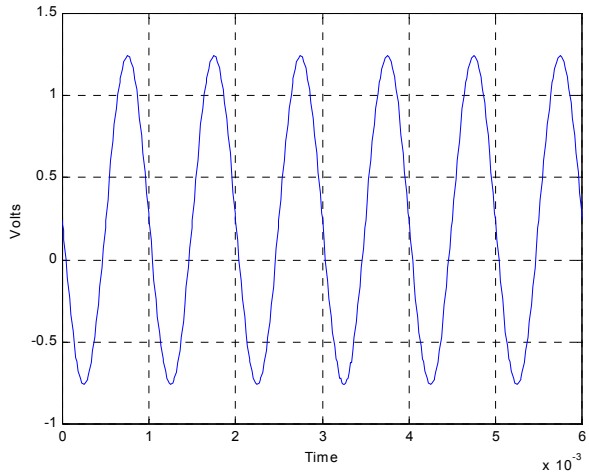

Figure 3.26. Output from 0.01 V 1kHz Sinusoid.

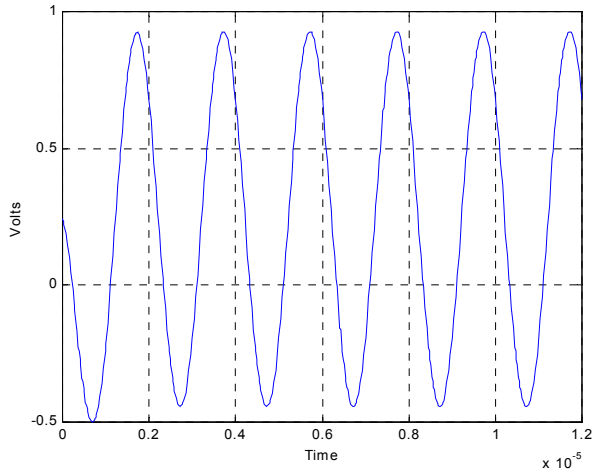

Figure 3.27. Output from 0.01 V 500kHz Sinusoid.

3. Current and Power Consumption

The closed loop gain circuit (Figure 3.16) with an input voltage of 10 mV (producing a 1V sinusoidal output) was used to test the current flowing from the power rails. The average current from V_{DD} was 0.2546 mA and the average current from V_{SS} was –0.2544 mA. Thus the average power consumption is the voltage times the current for both V_{DD} and V_{SS}: 2.54 mW. Because the current is well below the 1mA limit, minimum sized supply lines can be used. Figure 3.28 depicts the output current for the input sinusoid. The opamp was also tested using a power supply of 3.3V. The current in each rail had a magnitude of 83.3 μA for a total power consumption of 0.55 mW.

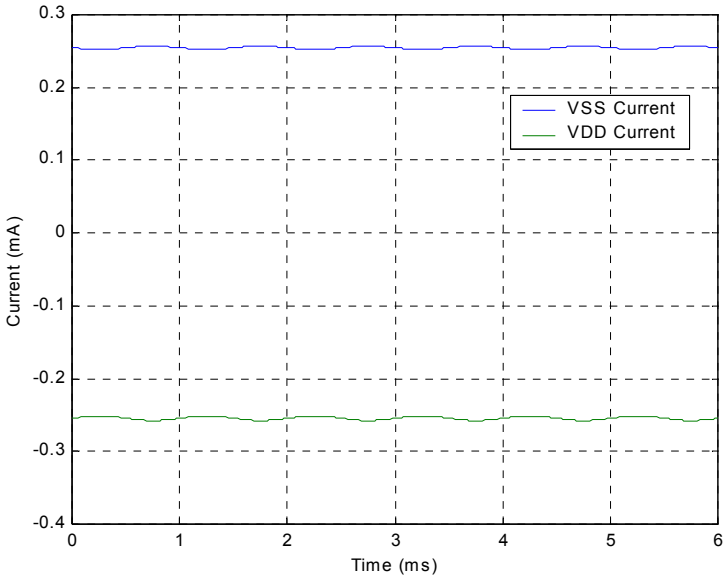

Figure 3.28. Current from Power Rails for Closed Loop Gain = 100.

G. LAYOUT

The VLSI layout was produced using Layout System for Individuals (LASI) 6.0 loaded with the MOSIS process design rules.

1. NPN Transistors

Lateral bipolar transistors have always been available in standard CMOS processes. A lateral PNP transistor is shown in figure 3.29. However, theses transistors have typically demonstrated poor performance. Additional process steps can be added to make vertical transistors with dramatic performance improvements over their lateral counterparts. The MOSIS process has an additional P-BASE layer that allows the possibility of using the vertical NPN transistor shown in Figure 3.30.

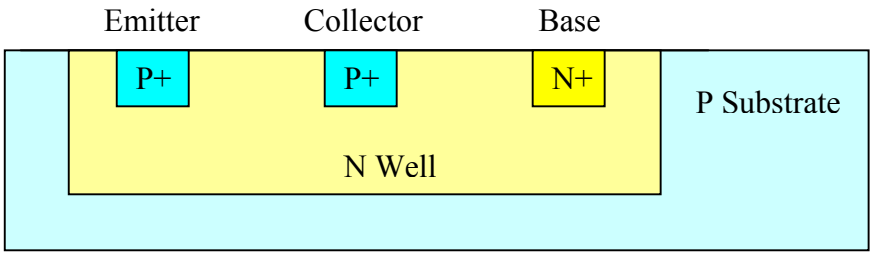

Figure 3.29. Cross-section of Lateral PNP Transistor.

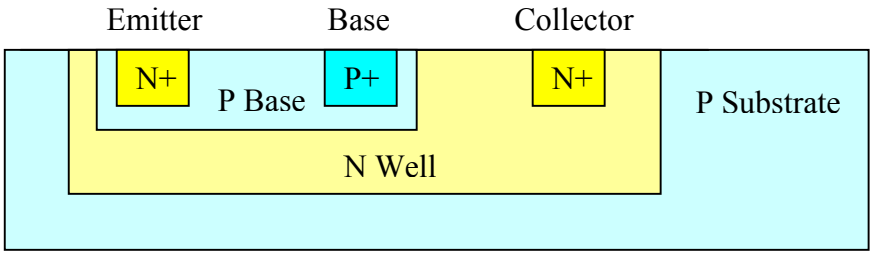

Figure 3.30. Cross-section of Vertical NPN Transistor.

Figure 3.31 depicts the NPN transistor layout designed for the MOSIS process. Note that the N+ collector region was designed to surround the entire n-well so that it would have ample opportunity to "collect" current from the emitter.

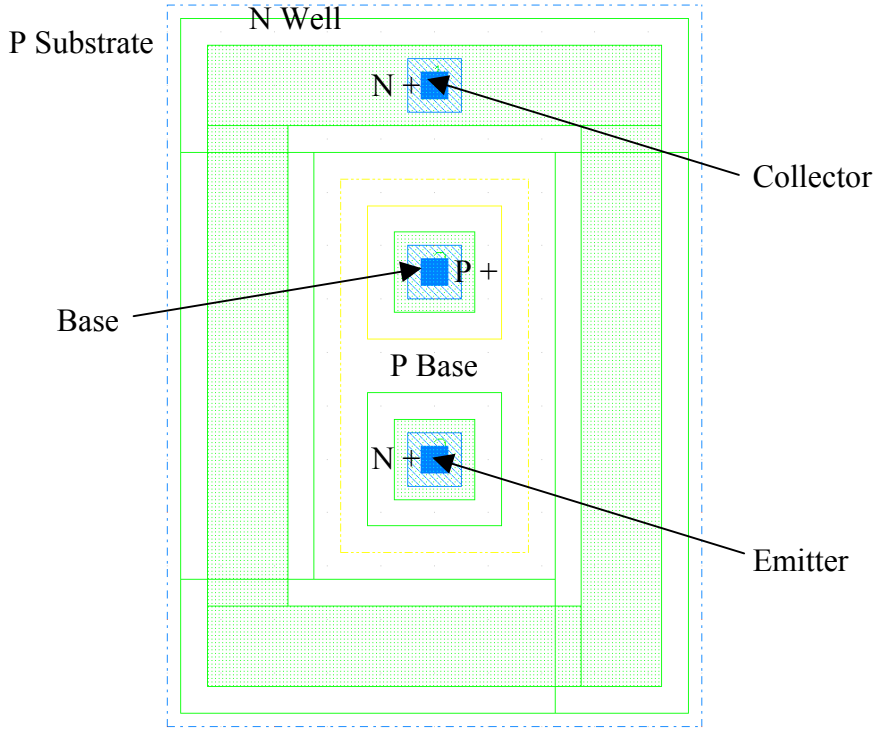

Figure 3.31. NPN Transistor Layout.

2. CMOS Transistors

No changes were made to the previous CMOS transistor designs. Figure 3.32 shows the cross section of a P-channel and an N-channel CMOS transistor. The PFET is on the left and the NFET is on the right.

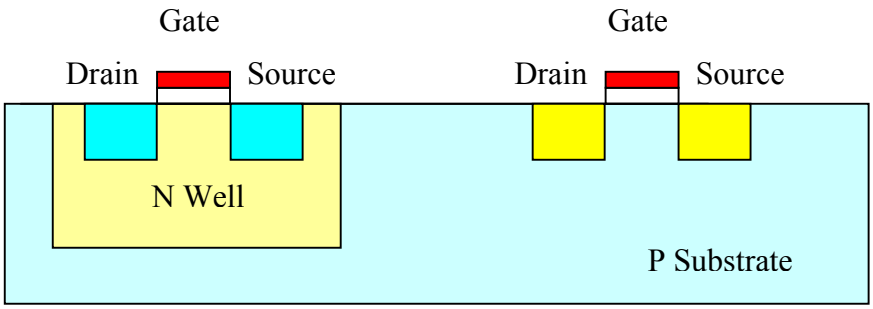

Figure 3.32. Cross Section of CMOS Transistors.

If an NFET and a PFET are connected together in the proper manner an inverter can be constructed. Figure 3.33 is the layout of a CMOS inverter. The PFET is on top and the NFET is on bottom. The two gates (polysilicon in red) are connected and the two drains are connected together on the right (gray metal2 connected to blue metal1.) The source on the PFET is connected to V_{DD} and the source on the NFET is connected to V_{SS}.

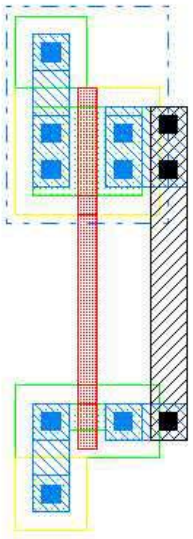

Figure 3.33. CMOS Inverter.

3. Capacitors

VLSI capacitors are designed from choosing two layers of conductive material to act as capacitor plates. Capacitance between two materials is usually measured and given in unit capacitance per unit area. To conserve layout area and minimize capacitor size, a designer might choose the two materials with the largest capacitance per area. The MOSIS website lists the capacitance parameters between several material layers as outlined in Table 3.5.

Table 3.5. Capacitance Parameters.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	N_WELL	UNITS
Area (substrate)	289	300	37		25	15	55	aF/um^2
Area (N+active)			1109	712	49	27		aF/um^2
Area (P+active)			1092	705				aF/um^2
Area (poly1)				594	44	23		aF/um^2
Area (poly2)					44			aF/um^2
Area (metal1)						40		aF/um^2
Fringe (substrate)	114	198			31	37		aF/um
Fringe (poly)					57	45		aF/um
Fringe (metal1)						57		aF/um
Overlap (N+active)			171					aF/um
Overlap (P+active)			219					aF/um

From the table it is clear that the highest capacitance per area is N+ active to polysilicon. This layout for this type of capacitor is illustrated in Figure 3.34. The figure does not illustrate the contacts to the polysilicon or to the N+ region that forms the two leads to the capacitor. This type of capacitor is highly voltage dependant (Sedra, 1998) and is therefore not used in this design. However, this type of capacitor was used in the previous design of the GIC filter, but a mistake was made. The N well was not included in the previous design, which produces a much smaller capacitance than desired.

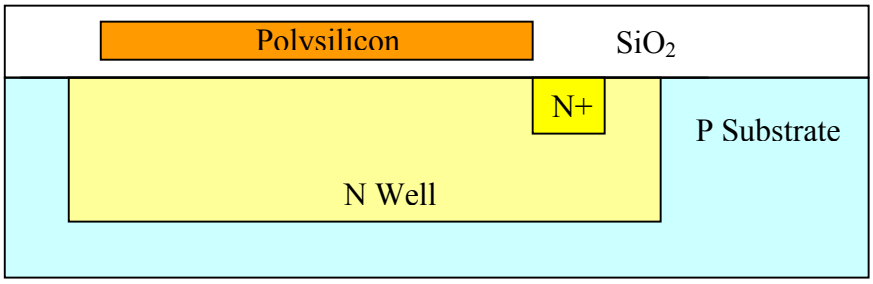

Figure 3.34. Polysilicon to N+ Active Capacitor.

Using the additional polysilicon layer of the MOSIS process can produce a better capacitor design. A poly1 to poly2 capacitor has a reduced capacitance per area and requires and additional process step, but it is isolated from the substrate by a thin layer of oxide and thus exhibits near ideal characteristics (Sedra, 1998.) Figure 3.35 depicts the design used for the BiCMOS compensating capacitor.

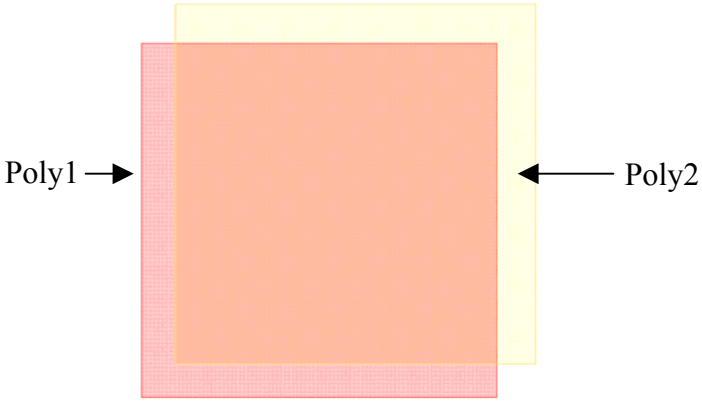

Figure 3.35. Poly1 to Poly2 Capacitor.

An additional technique can be used to further reduce the size of a VLSI capacitor. Using several stacked layers of different materials can add to the overall capacitance, thus reducing the area required. A conceptual diagram is illustrated in Figure 3.36. With this design, the capacitance between each level can be added together, thus reducing the overall area of the capacitor.

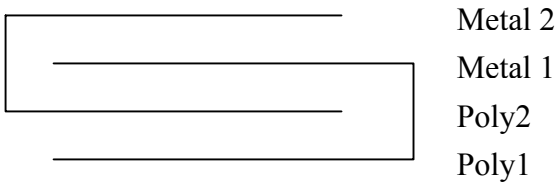

Figure 3.36. Conceptual Diagram of Multi-Layer Capacitor.

Figure 3.37 shows a three dimensional view of a multi-layered capacitor to further demonstrate the concept.

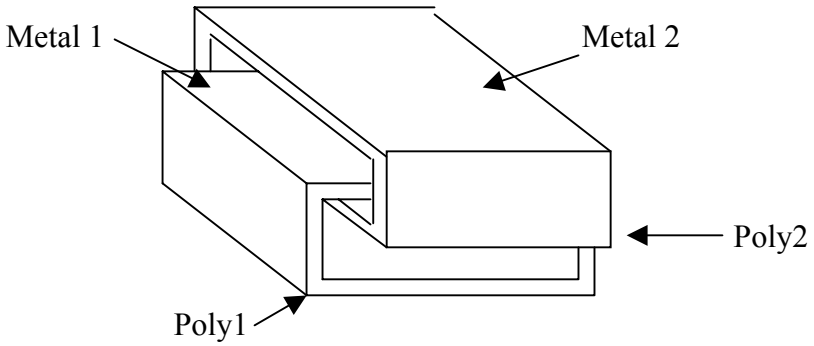

Figure 3.37. Thee Dimensional Conceptual Diagram of Multi-Layer Capacitor.

Although this concept can certainly lead to a capacitor with less surface area the actual savings is very small. The capacitance per unit area for metal1 and metal2 just isn't large enough in comparison with that of poly1 and poly2 to make a considerable difference in capacitor size. Table 3.7 illustrates this principle.

Table 3.7. Capacitor Width for a Square Capacitor.

Capacitor Value	1pF	2pF	3.25pF	13.0pF
N+ Active to Poly	30 µm	42 µm	54 µm	108 µm
N+ Active/Poly/Met1/Met2	29 µm	41 µm	52 µm	104 µm
Poly to Poly2	41 µm	58 µm	74 µm	148 µm
Poly/Poly2/Met1/Met2	38 µm	54 µm	69 µm	138 µm

4. Opamp Layout

Figure 3.38 depicts the layout for the BiCMOS Operational Amplifier. The two NPN transistors are clearly seen in green, left-center in the figure. At the bottom right is the 3.25 pF capacitor. The PFETs line the top of the figure while the NFETs are across the bottom.

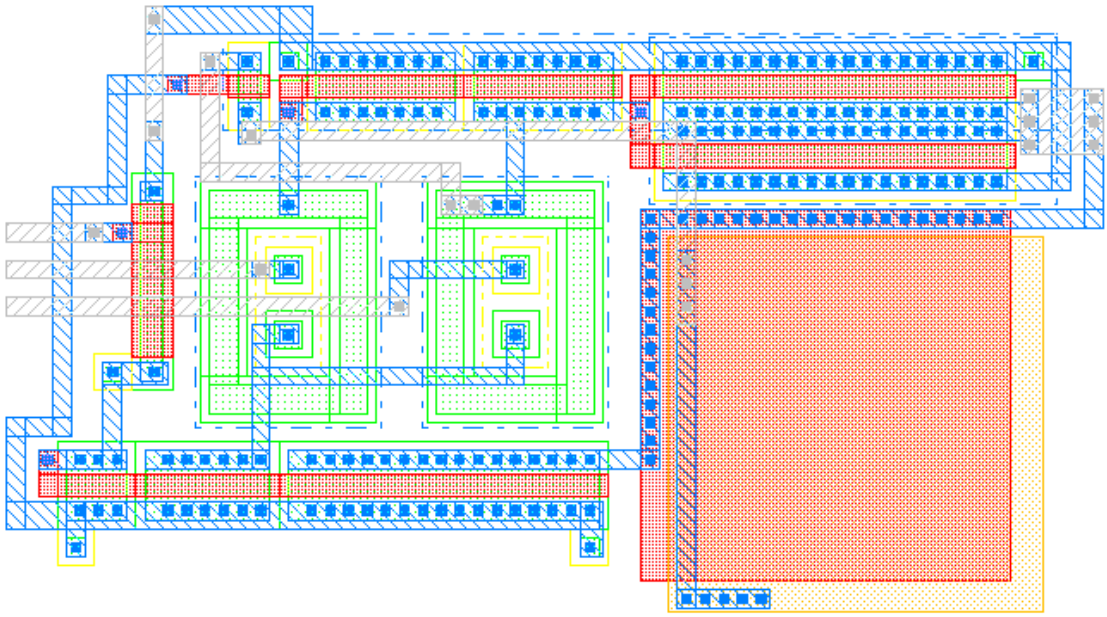

Figure 3.38. BiCMOS Opamp Layout.

H. SUMMARY

Two operational amplifiers were considered for inclusion in the BiCMOS GIC filter design. The first design, Sone and Yotsuyanagi had undesirable characteristics. Those characteristics could be adjusted to produce a desirable opamp, but not without considerable research. The Sone and Yotsuyanagi design was therefore rejected for inclusion in this design. The second design, a modified version of the Lee design, met both of the design criteria established for this thesis: improved performance and simplicity to implement. Table 3.7 contains a summary of the BiCMOS opamp characteristics. The GBWP is larger in the 3.3 Volt version because the compensating capacitor was reduced from 10 pF in the 5 Volt version to 3.25 pF.

Table 3.7. Summary of Opamp Characteristics.

	5 Volt Rails	3.3 Volt Rails
GBWP	14.6 MHz	17.9 MHz
Slew Rate	20V/μs	
Offset Voltage	3.0 mV	
Power Consumption	2.54 mW	0.55 mW

IV. THE BILINEAR RESISTOR

Switching a capacitor between two circuit nodes can approximate resistor operation (Laker, 1994.) Figure 4.1 depicts just such an approximation, a floating bilinear resistor.

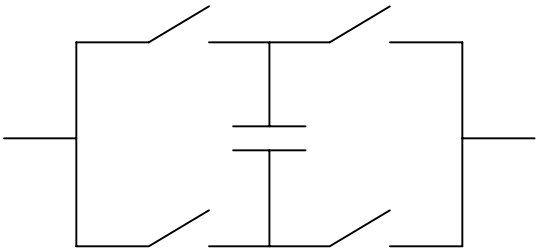

Figure 4.1. Bilinear Resistor.

A. NON-OVERLAPPING CLOCK

In order to realize a bilinear resistor, a special clock must be used to control the switching. The circuit design requires that the pulses that control the switches must be timed such that two switches in a direct path are not closed at the same time, thus preventing a short circuit. This requires a clock that generates two out of phase non-overlapping clock signals.

This arrangement of clock signals can be produced by utilizing a standard input clock signal and standard CMOS logic gates. The two out of phase clock signals are generated by two cross-coupled nor gates and an inverter. The non-overlapping property is generated by using the gate delay of the nor gates plus any additional inverters. Figure 4.2 depicts the circuit diagram for the non-overlapping clock. In addition, the last pair of inverters should be large enough to drive all the bilinear resistors in the design.

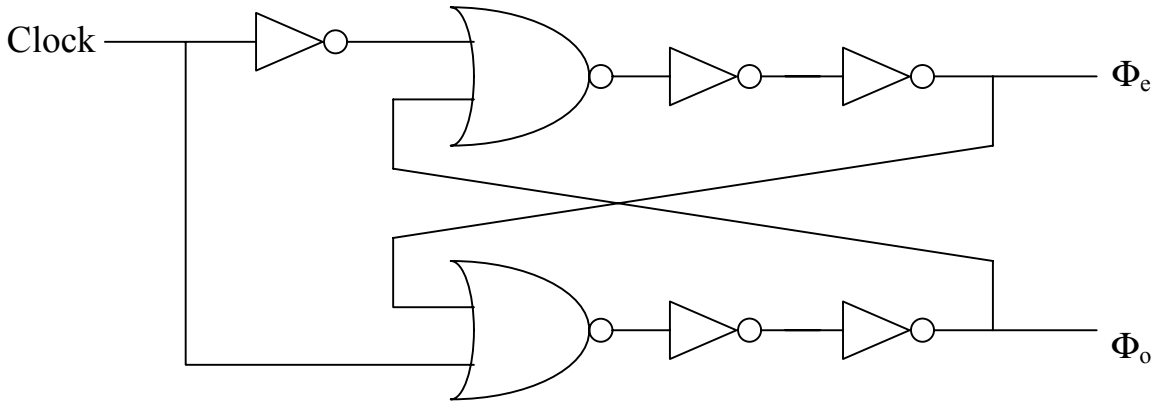

Figure 4.2. Non-Overlapping Clock.

The ideal non-overlapping clock should have the waveforms depicted in Figure 4.3 for the bilinear resistor shown in Figure 4.4. Φ_e denotes the even waveform and Φ_o denotes the odd waveform. Figure 4.4 also shows how the waveforms relate to the switch controls.

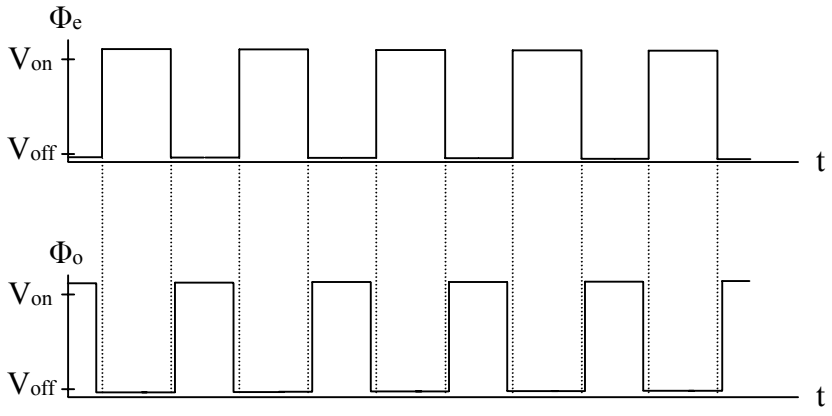

Figure 4.3. Ideal Non-Overlapping Clock Output (from Lee, 2000).

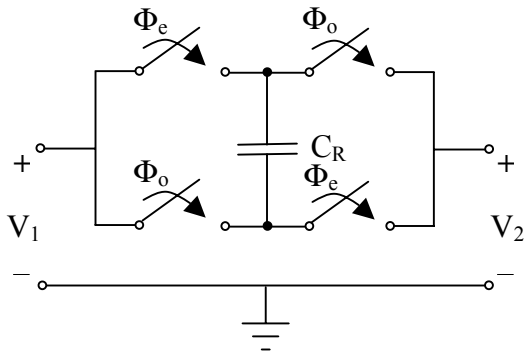

Figure 4.4. Bilinear Resistor with Switch Controls (from Lee, 2000).

Table 4.1 lists the delay for several clock circuit configurations. Although the clock must operate over the entire voltage range, all the data in the table is useful in determining the relationship between circuit configurations and non-overlapping delay.

Table 4.1. Non-Overlapping Clock Delay.

Clock Speed	1 MHz	1 MHz	1 MHz	10 MHz
Voltage Range	0 to 5V	0 to 3.3V	-3.3 to 3.3V	-3.3 to 3.3V
2 Inverter	1.36 ns	1.96 ns	2.00 ns	1.99 ns
4 Inverter	1.77 ns	2.62 ns	2.08 ns	2.06 ns

Note that the extra inverters add delay, but not a considerable amount. This is because their size is small in comparison with the last pair of driver inverters and the NOR gates.

To match the opamp voltage range the –3.3V to +3.3V clock was selected. Because the delay between two and four inverters is insignificant, the configuration with two inverters was selected. Figure 4.5 shows the output for a –3.3V to +3.3V non-

overlapping clock with a two inverter delay. Figure 4.6 displays a close-up view of the delay.

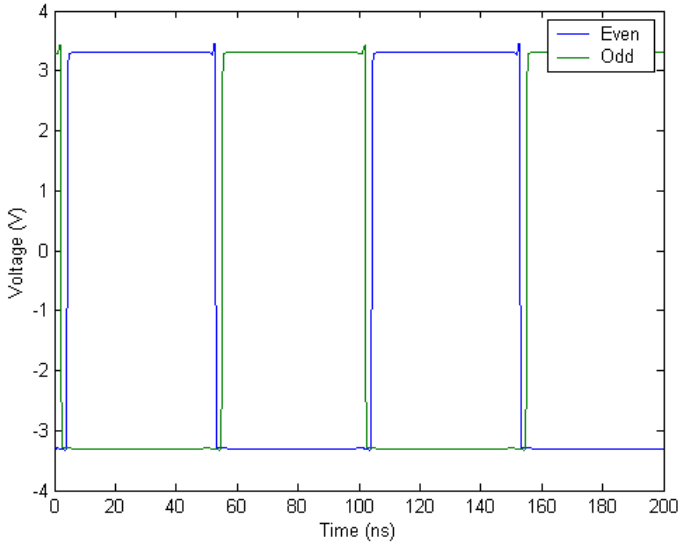

Figure 4.5. Non-Overlapping Clock with Two Inverter Delay.

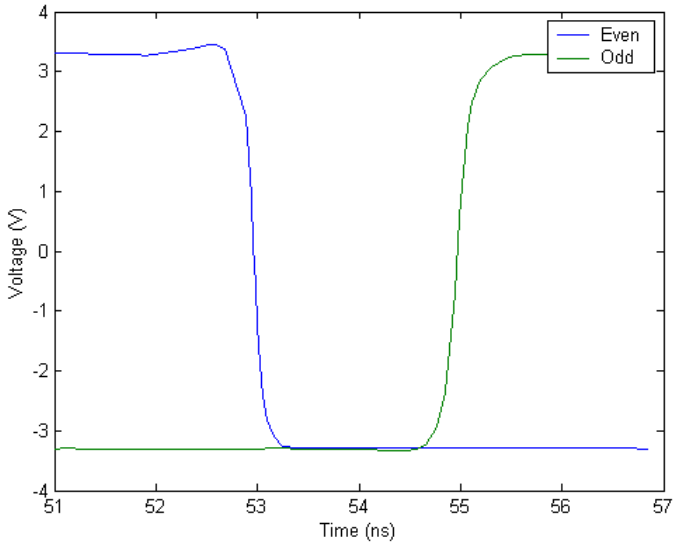

Figure 4.6. Non-Overlapping Clock with Two Inverter Delay.

Figure 4.7 shows the timing of the clock and the switches. In the diagram, a high voltage level turns the switch on (closes the switch) and a low voltage level turns it off

(opens the switch.) Likewise, the high voltages for the waveforms labeled “Switch A” and “Switch B” denote the switch is closed and a low voltage denotes the switch is open.

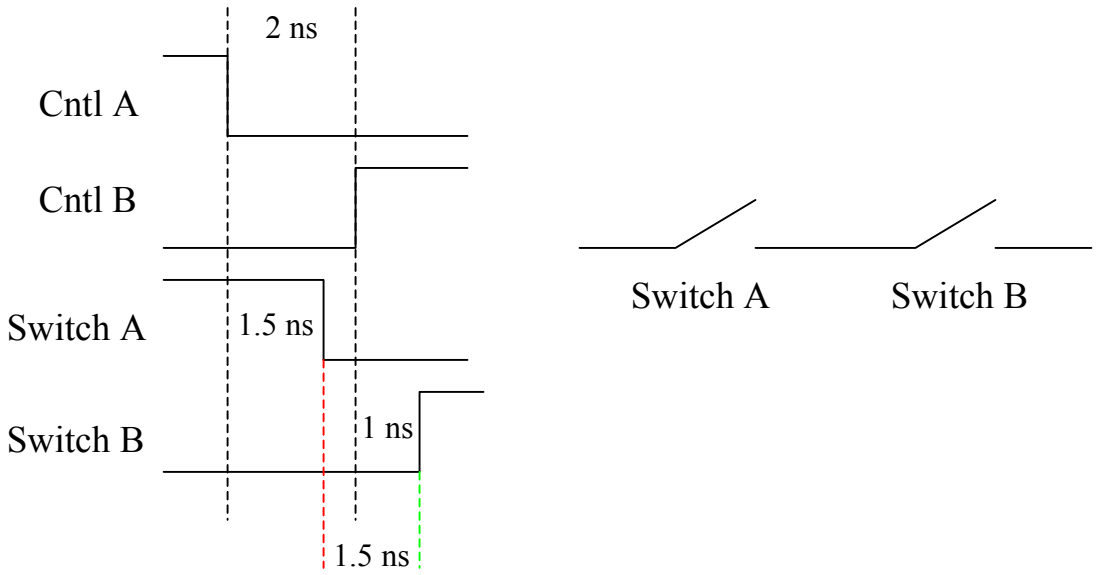

Figure 4.7. Non-Overlapping Clock with Two Inverter Delay.

An analysis of the timing is required because it is imperative that the switches are not both closed at the same time. The delay for a switch to open is 1 ns and the delay for a switch to close is 1.5 ns. For these switch characteristics and a clock delay of 2 ns, there is a 1.5 ns gap during which both switches are open. The non-overlapping clock in past designs used two pairs of inverters; however, one pair of inverters is sufficient to produce an appropriate delay.

B. PASSGATES

Switches are a necessity for the proper operation of the bilinear resistor. As such, several switch designs were considered as candidates for inclusion in the bilinear resistor circuit. A single CMOS transistor, a minimum sized passgate, and an enhanced passgate were all examined. Previous designs used a simple passgate constructed from two opposing minimum sized CMOS transistors (Figure 4.8.) The enhanced passgate was designed to maintain linear operation of the passgate by adjusting the length and width

parameters of the constituent transistors. The major design criteria considered for switch construction was linearity, resistance, and timing.

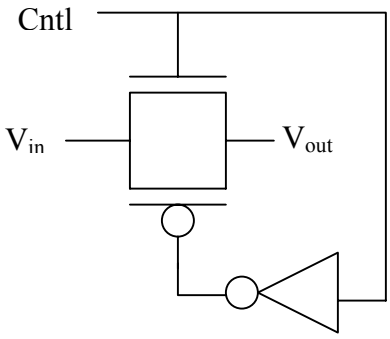

Figure 4.8. Standard Passgate Design.

The addition of nonlinear switches could affect the linear operation of the GIC filter; therefore, nonlinear passgate effects should be minimized. It is also desirable to minimize the resistance of the switch such that the operating characteristics are as close as possible to that of an ideal switch. However, increasing the size of transistors to reduce the resistance has the opposing effect of increasing capacitance and could possibly affect switching speed.

Figure 4.9 shows the output from the enhanced passgate in comparison with other switches (the label "matched passgate" in the figure is the same as "minimum passgate.") This comparison was obtained from the output of the circuit in Figure 4.10. The PFET switch has the most resistance of all the switches tested. In addition to this, the output is skewed and has more resistance when the output is negative and less resistance when the output is positive. The NFET switch has similar but opposite characteristics, its increased resistance is in the positive voltage range. The minimum sized passgate is an attempt to equalize the output by using an NFET and PFET together. However, as the figure shows, the output offers marginal improvements over that of the NFET by itself. As a result, the non-linearity is still significant for the minimum sized passgate. However, the resistance of the enhanced passgate is not only significantly smaller but also very close to linear in both the negative and positive voltage ranges. Therefore, the

enhanced passgate was selected to act as the switch in the bilinear resistor. Table 4.2 summarizes these results.

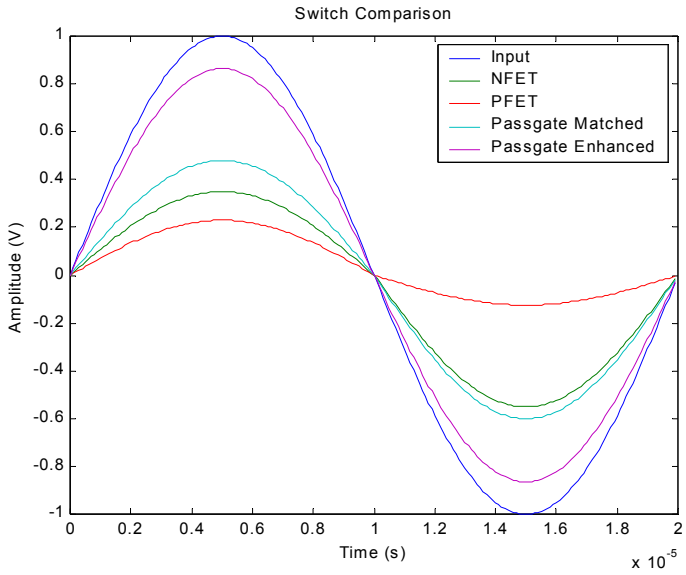

Figure 4.9. Switch Resistance Comparison.

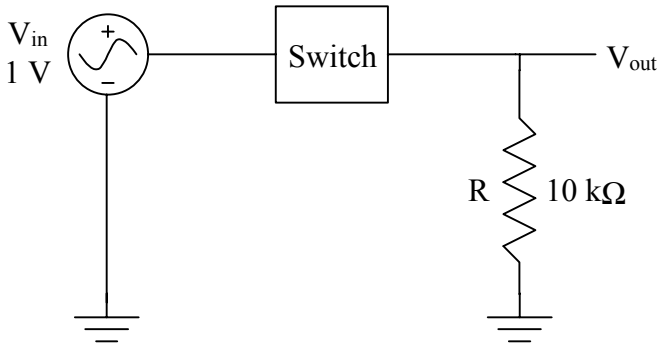

Figure 4.10. Switch Comparison Circuit.

Table 4.2. Switch Comparison Summary.

	Pos. Amplitude	Neg. Amplitude	Pos. Resistance	Neg. Resistance
NFET	0.35	-0.55	18.6k	8.18k
PFET	0.23	-0.125	33.5k	70.0k
Passgate Minimum	0.48	-0.60	10.8k	6.67k
Passgate Enhanced	0.864	-0.865	1.57k	1.56k

C. BILINEAR RESISTOR DESIGN

The previous design utilized a 2.03 pF capacitor and a 10 MHz clock frequency producing a resistance of 12,315 Ω. In order to maintain consistency, a 2 pF capacitor was selected for this design as well. The resistance measured from the initial simulation was 11.5 kΩ. The circuit used for this test was similar to the circuit in Figure 10 except that the switch was replaced with the bilinear resistor.

In addition to the standard bilinear resistor, an additional resistor is required to control the quality factor. The circuit diagram is shown for this variable resistor in Figure 4.11. The boxes represent digital logic controlled switches that are used to arrange the capacitors in six configurations – covered in the next chapter.

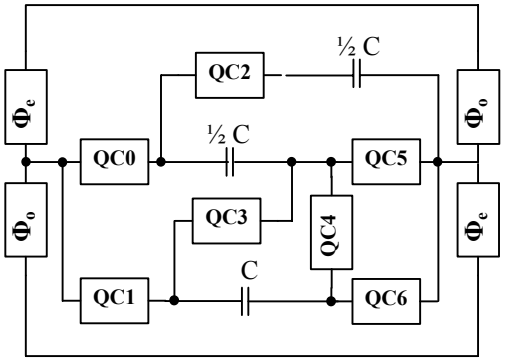

Figure 4.11. Variable Bilinear Resistor.

Table 4.3 shows the results from the variable bilinear resistor. Also shown in the table are the results from a standard bilinear resistor with the values of capacitance that should result from the 6 switch arrangements. The values for the variable bilinear resistor are considerably larger than expected. The quality factors listed in the table are based on the ratio of the resistance to the resistance for the 2 pF resistor. This normalization of the quality factor was performed in order to further illustrate the difference between the two resistance values calculated for each capacitance.

Table 4.3. Resistance and Quality Factors.

Regular bilinear resistor	10.0 kΩ	11.4 kΩ	22.0 kΩ	35.6 kΩ	50.5 kΩ	65.4 kΩ
Variable bilinear resistor	42.4 kΩ	46.0 kΩ	63.8 kΩ	91.1 kΩ	112 kΩ	144 kΩ
Expected value	9.9 kΩ	12.3 kΩ	24.6 kΩ	36.9 kΩ	49.3 kΩ	61.6 kΩ
Regular quality factor	0.9	1.0	1.9	3.1	4.4	5.7
Variable quality factor	0.9	1.0	1.4	2.0	2.4	3.1
Expected quality factor	0.8	1.0	2.0	3.0	4.0	5.0
Value of internal capacitor	2.5 pF	2 pF	1 pF	0.67 pF	0.5 pF	0.4 pF

Many simulations were performed in order to verify these results. They were also compared to the results from LCDR Lee's thesis. Passgate switches were minimized to match the design in Lee's thesis (NFET 2X3, PFET 2X9.) However, the regular bilinear resistance was 21.1 kΩ instead of the 12.3 kΩ expected value. It could not be determined what parameters were used by LCDR Lee to simulate the bilinear resistor. This simulation used the BSIM3 transistor parameters from MOSIS. In an attempt to reproduce the values attained by LCDR Lee, the Level 3 parameters were used instead (both sets of parameters are included in the appendix.) The new result was a 14.8 kΩ resistor. The passgate was also minimized in the variable bilinear capacitor and modeled with the BSIM3 parameters. The result for the enhanced passgate design was 46.0 kΩ and the result for the minimized passgate was 77.6 kΩ. It is clear that passgate resistance dramatically changes the value of the bilinear resistor, especially in the case of the variable bilinear resistor where several passgates are used as switches. In addition, the transistor model parameters are critical in getting accurate simulation results. Because it is difficult to discern which simulation results are accurate, the design will not be adjusted to compensate for the simulation results. Testing must be performed on the fabricated bilinear resistors to determine what model parameters yield accurate results.

D. LAYOUT

Figure 4.11 depicts the layout for the enhanced passgate. The inverter is on the left and the passgate is on the right. The optimized size of the NFET transistors in the passgate is L=2µm and W=7µm. The optimized size of the PFET is L=2µm and W=23µm.

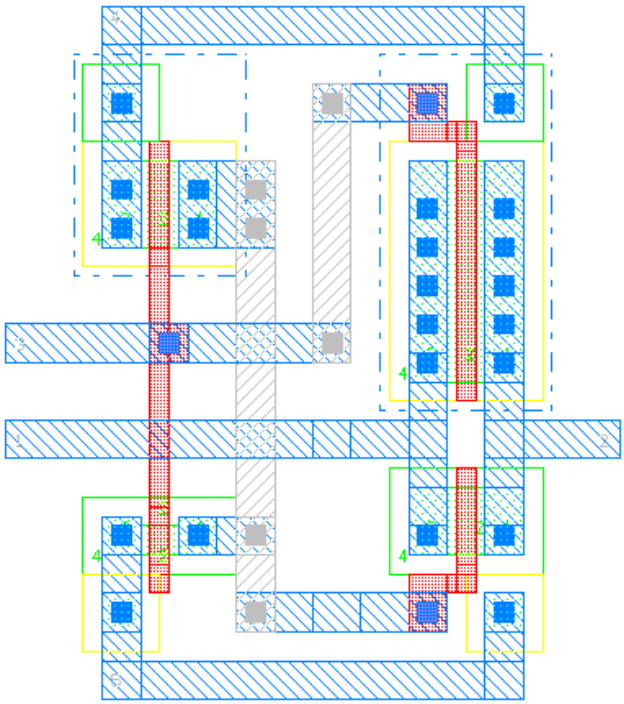

Figure 4.11. Passgate Layout.

Figure 4.12 depicts the layout for the non-overlapping clock. The large inverter pairs can be clearly seen on the right of the layout. The NOR gates are in the center and the initial inverter is seen to the upper left.

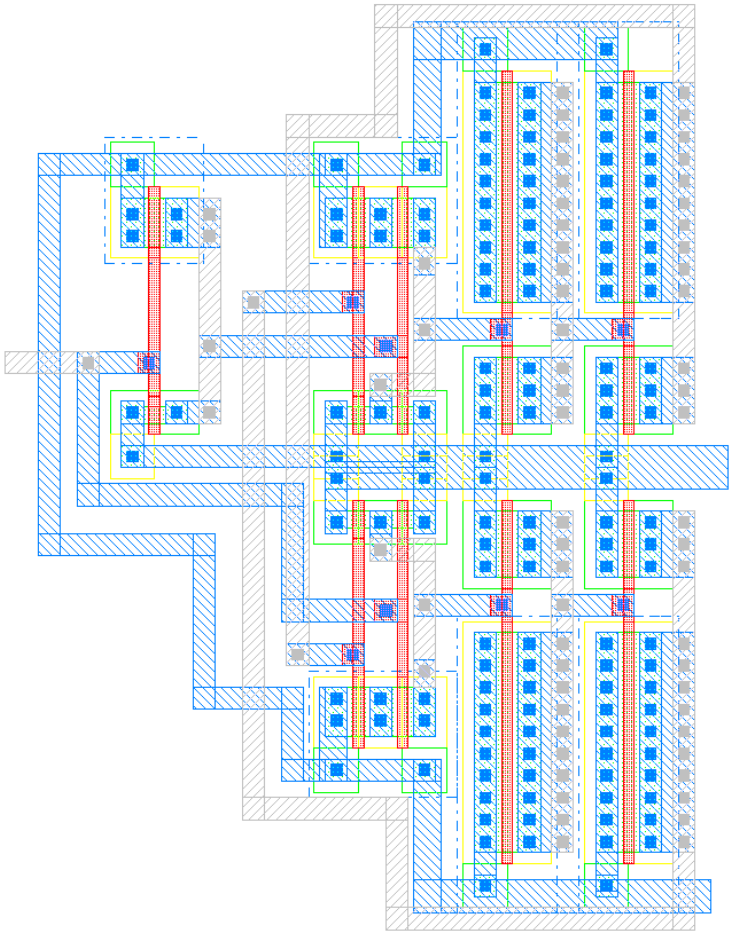

Figure 4.12. Non-Overlapping Clock Layout.

Figure 4.13 shows the layout for the bilinear resistor. The 2pF capacitor is in the center and a passgate is at each of the four corners. Figure 4.14 depicts the variable bilinear resistor. The control logic (covered in the next chapter) for the variable bilinear resistor is on the left, the three capacitors are in the center, seven passgates are used to switch in the correct capacitance value, and the four rightmost passgates are the standard four switches for the bilinear resistor.

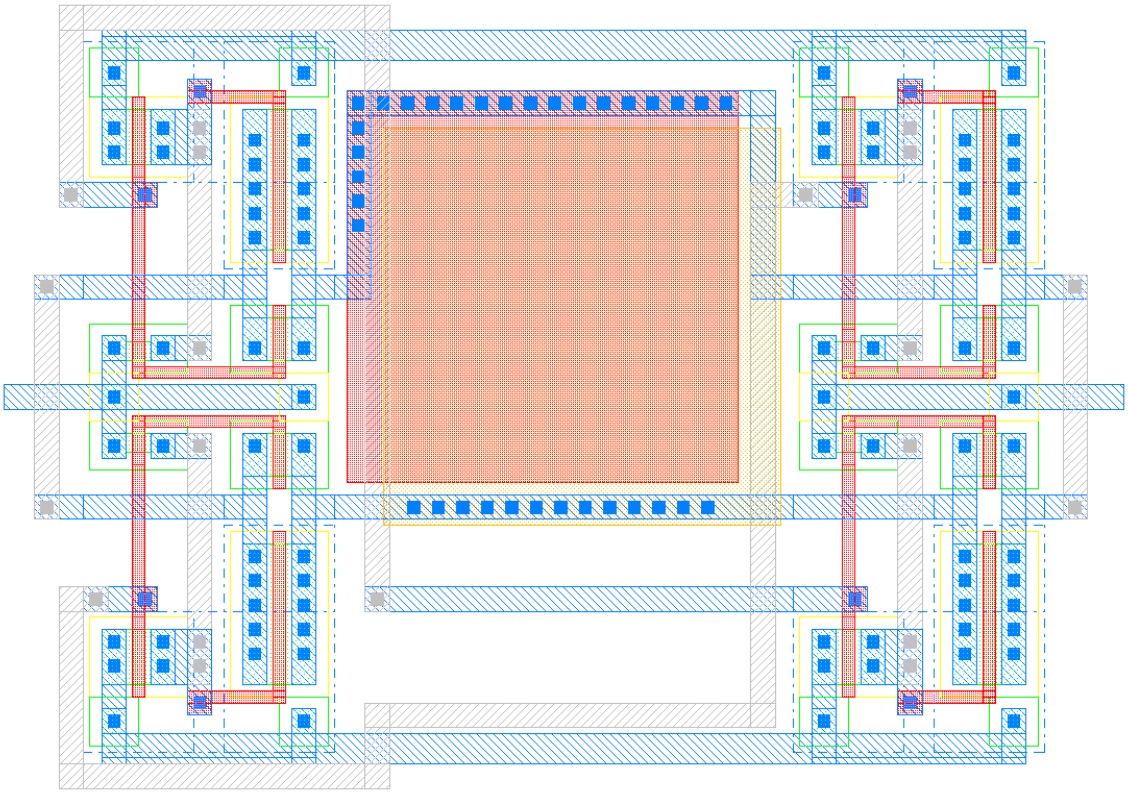

Figure 4.13. Bilinear Resistor Layout.

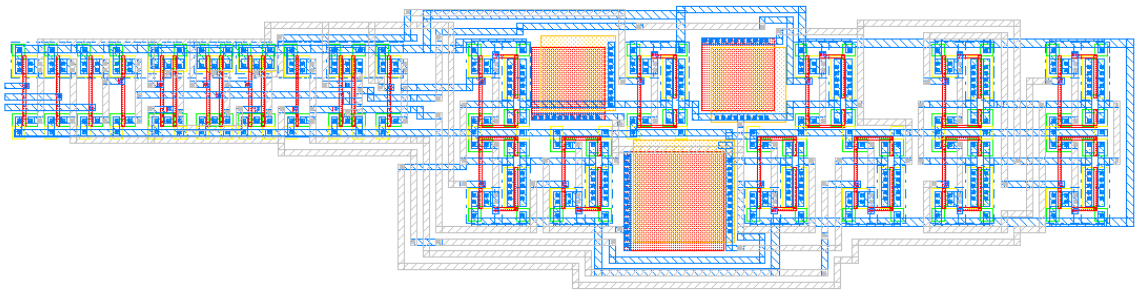

Figure 4.14. Variable Bilinear Resistor Layout.

V. THE GIC LOGIC CONTROL DESIGN

Digital logic is used to program the GIC filter for certain frequency response configurations. Given a certain input clock frequency, the filter is selectable for 4 topologies, 8 center frequencies, and 6 quality factors.

A. TOPOLOGY SELECTION

The four topologies that are allowable for selection are low pass, band pass, high pass, and notch as shown in Table 1. The topology selection is accomplished by a logic function that controls a set of 18 switches. The switches allow certain components to be connected or disconnected from the filter circuit. Figure 5.1 shows the selection logic. Figure 5.2 depicts the switch placement. Figure 5.3 is the VLSI layout for the logic selection circuit. The layout depicts from left to right, two inverters, four NAND gates and four more inverters.

Table 5.1. Topology Selection Truth Table.

Input		**Topology Controls**								**Topology**
S0	S1	C0	C1	C2	C3	C4	C5	C6	C7	
0	0	0	1	1	0	1	0	1	0	Notch
0	1	1	0	1	0	1	0	0	1	High Pass
1	0	1	0	1	0	0	1	0	1	Band Pass
1	1	0	1	0	1	0	0	0	1	Low Pass

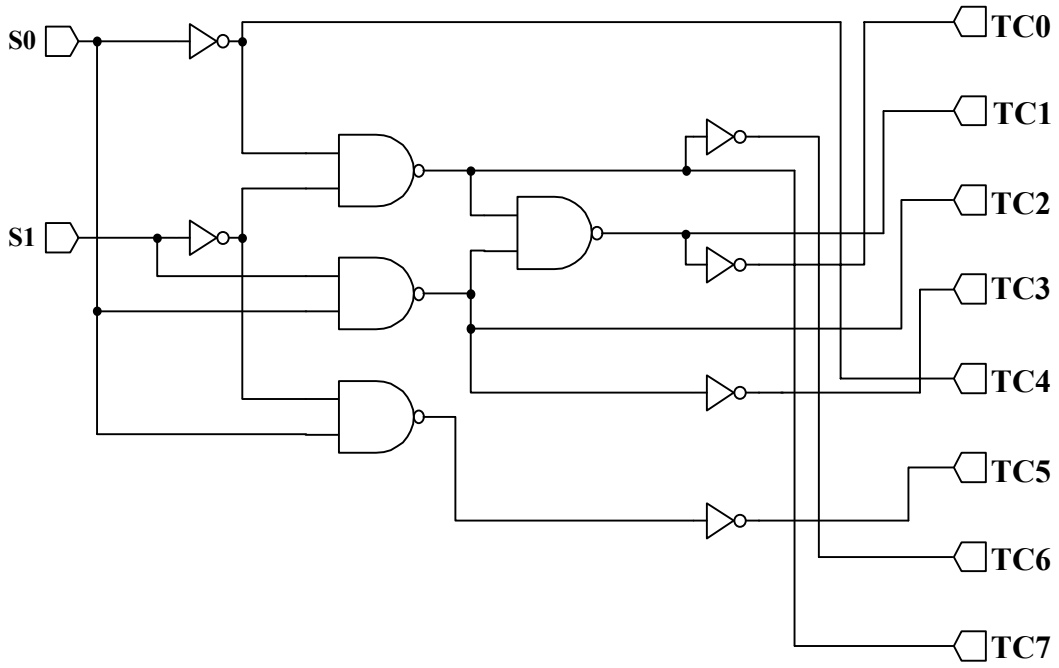

Figure 5.1. Topology Selection Logic (from Lee, 2000).

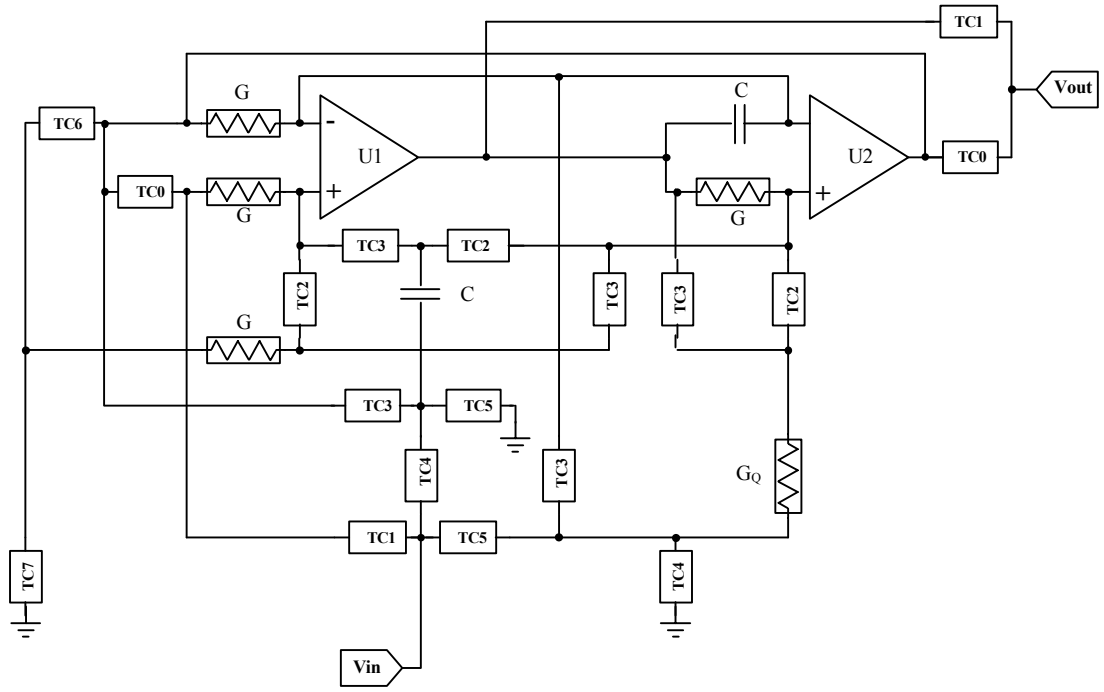

Figure 5.2. Topology Switch Placement (from Lee, 2000).

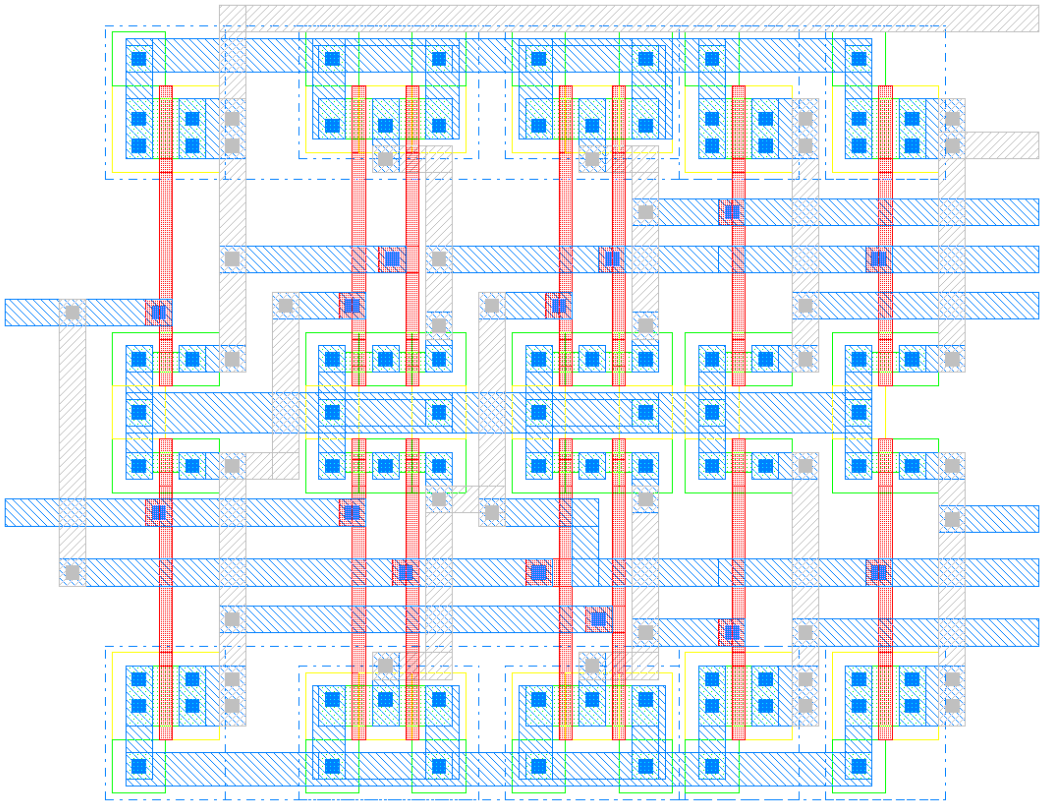

Figure 5.3. Topology Selection Logic Layout.

B. FREQUENCY SELECTION

Frequency selection is accomplished by varying the two standard capacitors in the filter. If the resistors are assumed to be fixed at a certain value (based on the input clock frequency to the bilinear resistors) it can be determined from Equation 2.7, which can be rewritten as

$$R = \frac{1}{4C_R f_C} \qquad \text{(Eq. 5.1)}$$

This equation yields a value of 12.3 kΩ, however, simulation showed this resistor to have a value of 10.5 kΩ. If it is assumed that the simulation results are accurate, then the center frequency can be determined from the resistance value and each variable capacitor. Table 5.2 gives the center frequencies for each value of the variable capacitor for the ideal bilinear resistor.

Analysis of Equation 5.1 shows that varying the bilinear resistor clock frequency changes the value of the resistor. By changing the value of the resistors, the center frequency of the filter will also vary. However, varying the input clock frequency by too large a value may cause improper operation of the bilinear resistor. Therefore, a wide range of center frequencies can be attained by a combination of digital input and clock frequency variation, though caution must be used in selecting appropriate clock frequencies.

Table 5.2 shows the truth table for the variable capacitor and Figure 5.4 shows the circuit diagram. The VLSI layout is shown in Figure 5.5. The capacitor in the upper left and the capacitor in the lower left of the figure are 13 pF capacitors. The 26 pF capacitor is in the center of the figure at the top. The 54 pF capacitor is at the bottom of the figure and extends up the right side of the figure in an "L" shape. It can be seen from Figure 5.4 that one plate on each of the capacitors is connected to a common node. Poly1 was used to represent this plate in Figure 5.6. The figure shows a solid layer of Poly1 under all the capacitors except the region where the switches lie. Figure 5.6 is a close-in view of the switches in the variable capacitor. The three switches are formed using passgates.

Table 5.2. Frequency Selection Truth Table (from Lee, 2000).

Input			**Frequency Controls**			**Capacitor**	**Frequency**
S2	S3	S4	C0	C1	C2		
0	0	0	0	0	0	13 pF	994.1 KHz
0	0	1	1	0	0	26 pF	497.1 KHz
0	1	0	0	1	0	39 pF	331.3 KHz
0	1	1	1	1	0	52 pF	248.5 KHz
1	0	0	0	0	1	65 pF	198.8 KHz
1	0	1	1	0	1	78 pF	165.7 KHz
1	1	0	0	1	1	91 pF	142.0 KHz
1	1	1	1	1	1	104 pF	124.0 KHz

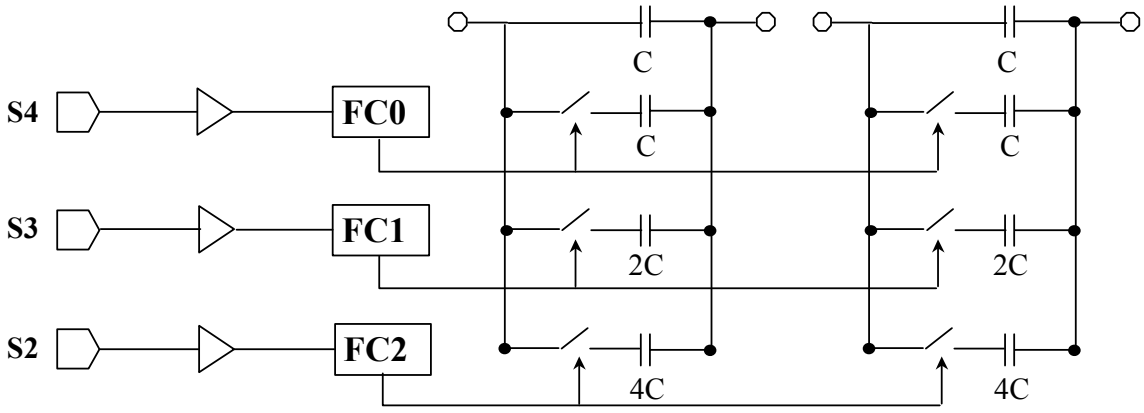

Figure 5.4. Variable Capacitor.

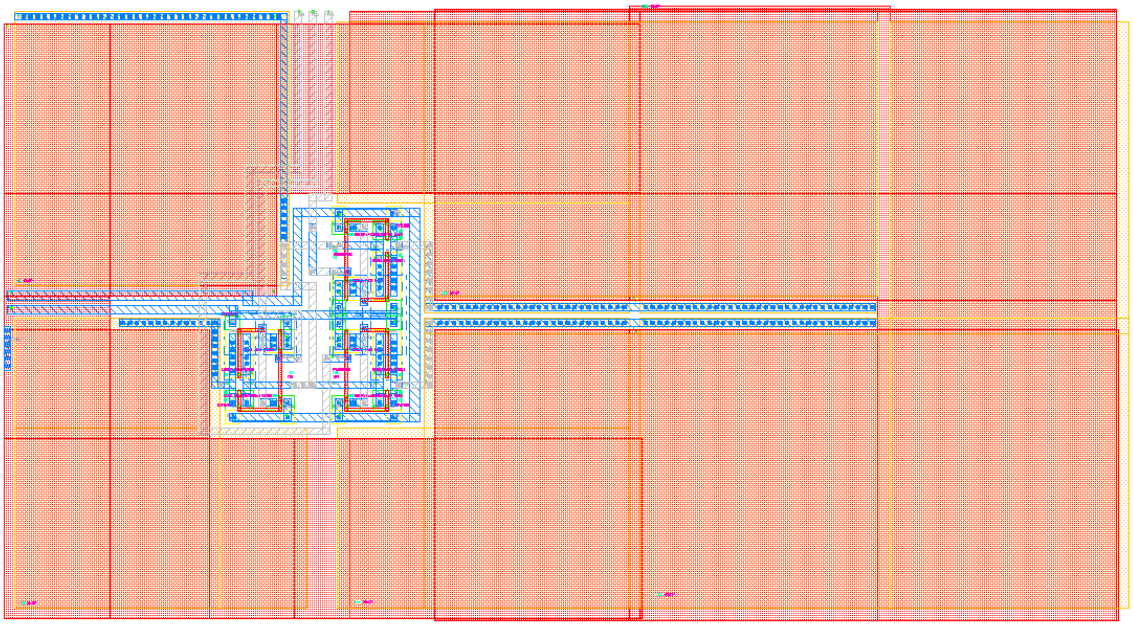

Figure 5.5. Variable Capacitor Layout.

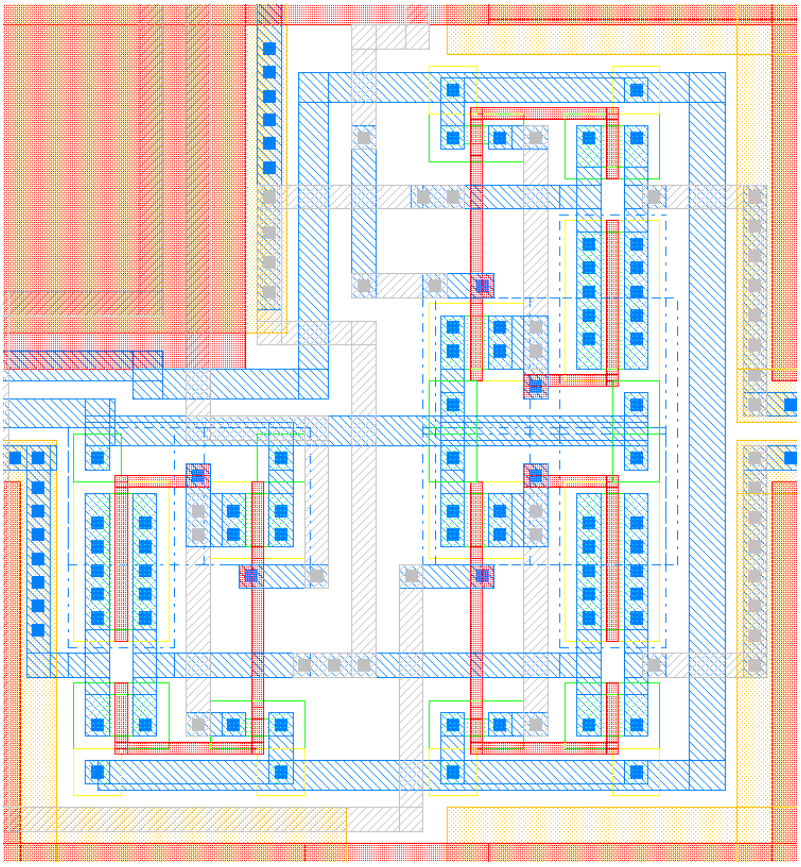

Figure 5.6. Variable Capacitor Switch Layout.

C. QUALITY FACTOR SELECTION

A modified bilinear resistor controls the quality factor. The capacitor internal to the resistor is replaced with a variable capacitor. The variable capacitor is composed of three capacitors and a set of switches that are controlled by 3 digital inputs. Table 5.3 shows the available quality factors. Figure 5.7 is the circuit used to control the quality factor and Figure 5.8 is the VLSI layout of the control circuit. Figure 5.9 is the VLSI layout of the quality factor selection circuit with the variable capacitor.

Table 5.2. Frequency Selection Truth Table (after Lee, 2000).

Input			Quality Factor Controls							Quality Factor
S5	S6	S7	QC0	QC1	QC2	QC3	QC4	QC5	QC6	
0	0	0	0	1	1	0	1	0	0	5
0	0	1	0	1	1	1	1	0	0	4
0	1	0	0	1	0	0	0	0	1	1
0	1	1	0	1	1	1	0	0	1	0.8
1	0	0	1	0	0	0	1	1	0	2
1	0	1	1	0	0	1	1	1	0	Not Used
1	1	0	1	0	0	0	0	0	1	Not Used
1	1	1	1	0	0	1	0	0	1	3

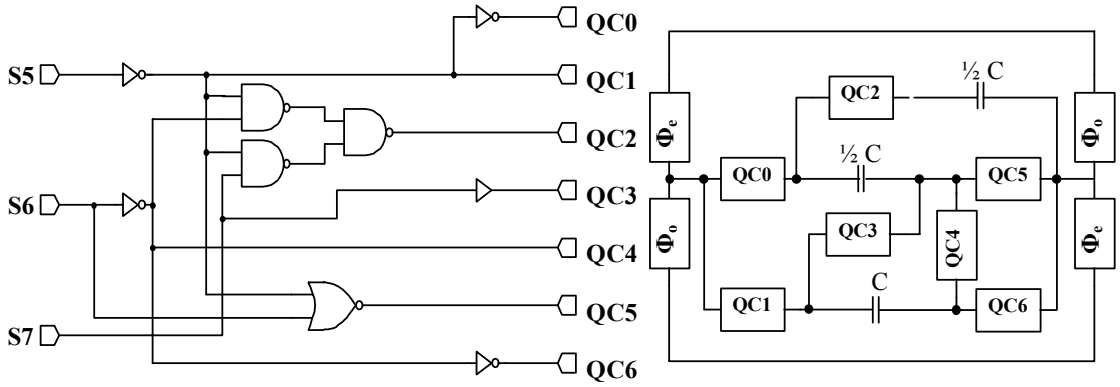

Figure 5.7. Variable Capacitor (from Lee, 2000).

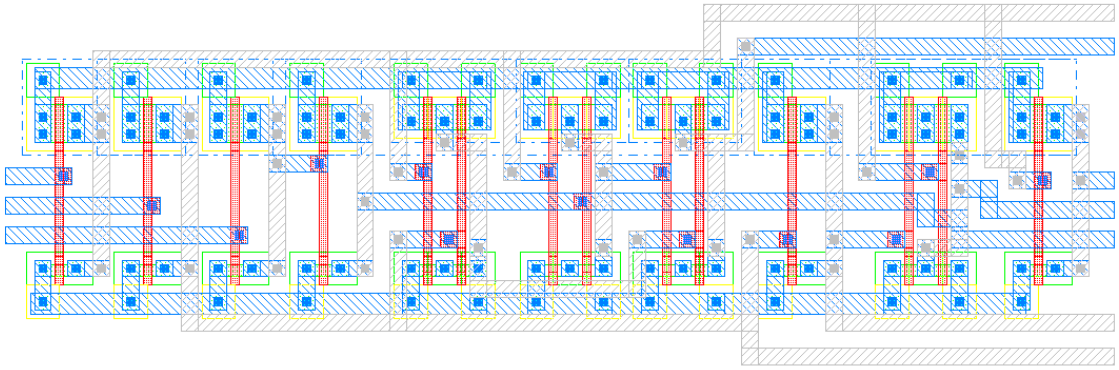

Figure 5.8. Variable Capacitor Switch Layout.

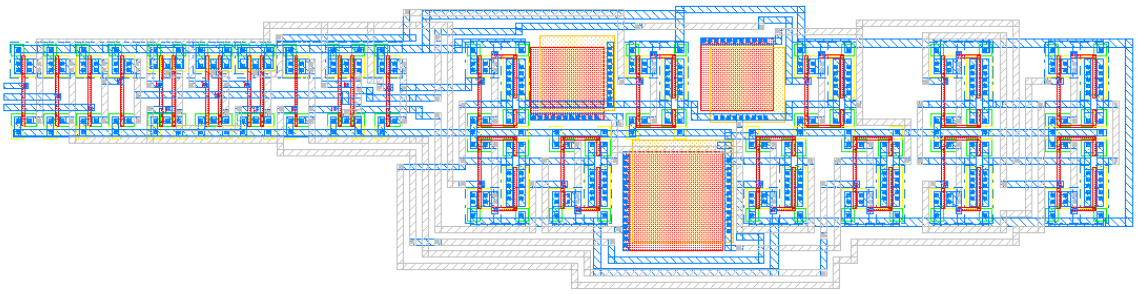

Figure 5.9. Variable Capacitor Switch Layout.

VII. CHIP LAYOUT

A. PROGRAMABLE GIC LAYOUT

The floor plan of the programmable GIC Filter is depicted in Figure 7.1. The actual VLSI layout is shown in Figure 7.2. The floor plan depicts the size and location of each subcomponent in the filter.

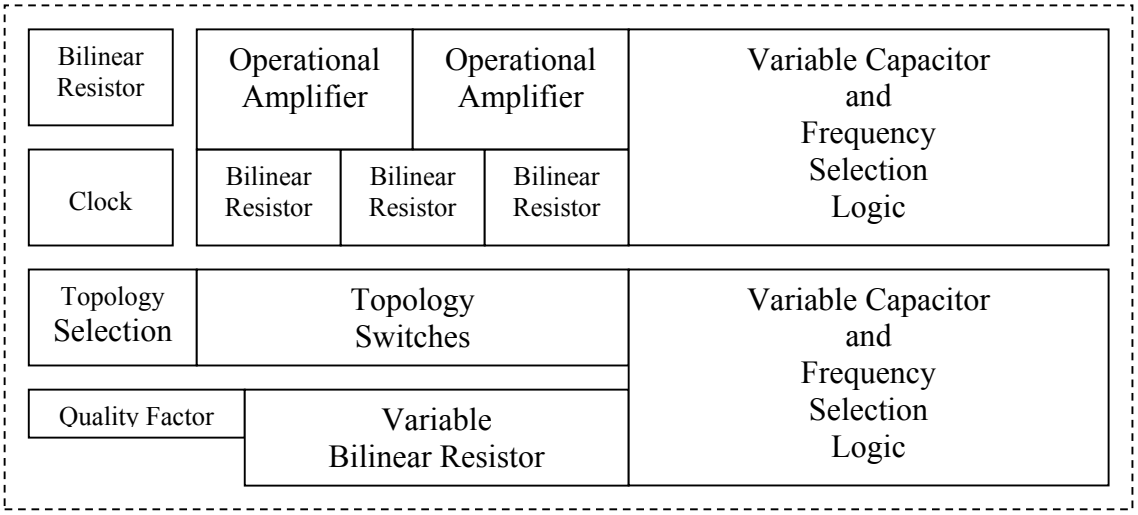

Figure 7.1. Programmable GIC Filter Floor Plan.

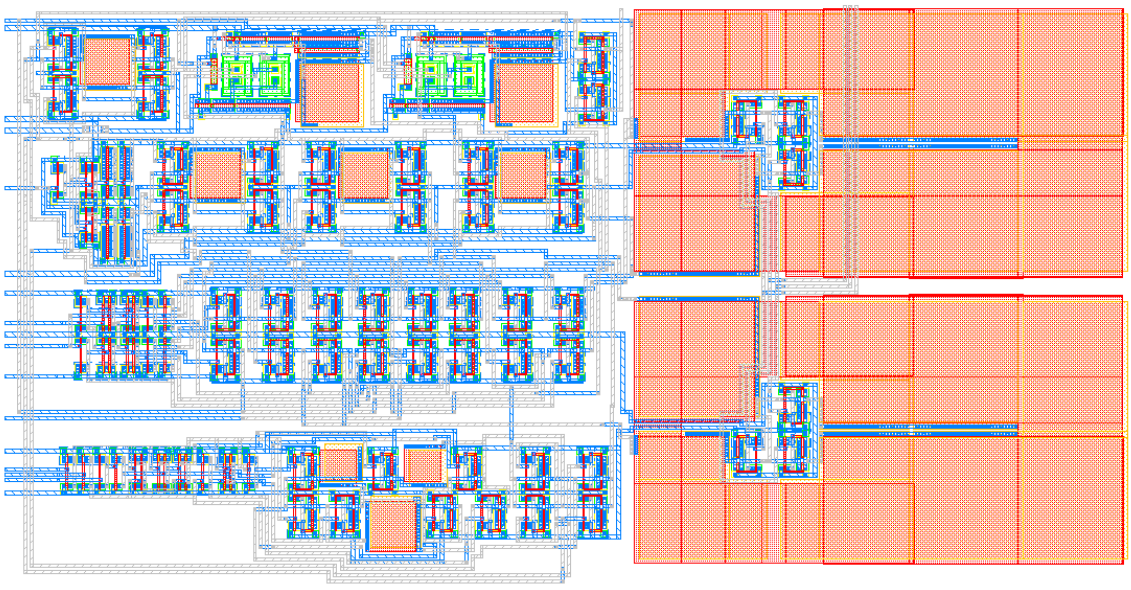

Figure 7.2. Programmable GIC Filter VLSI Layout.

B. FINAL CHIP LAYOUT

The final chip floor plan is depicted in figure 7.3. Two GIC Filters with completely separate power supplies and input pins are included so that they can be tested independently and cascaded or otherwise connected together.

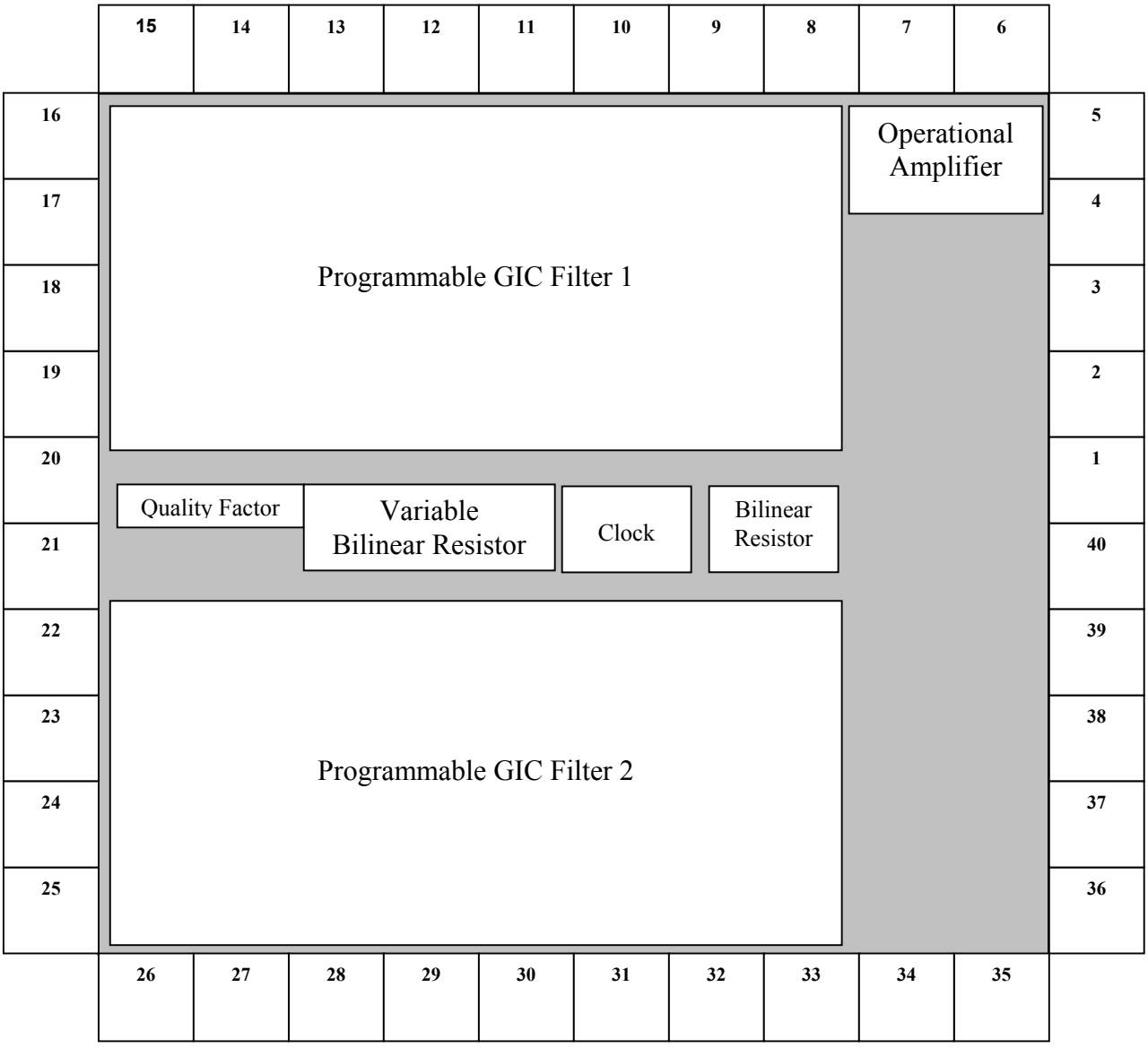

Figure 7.3. Final Chip Floor Plan.

In addition to the filters, a BiCMOS opamp is included so that its respective parameters can be compared to simulation results. Also, a bilinear resistor and a variable bilinear resistor are included for comparison to simulation results. The bilinear resistors share the input clock line and quality factor selection lines from the second programmable GIC Filter. Figure 7.4 shows the VLSI layout of the final chip.

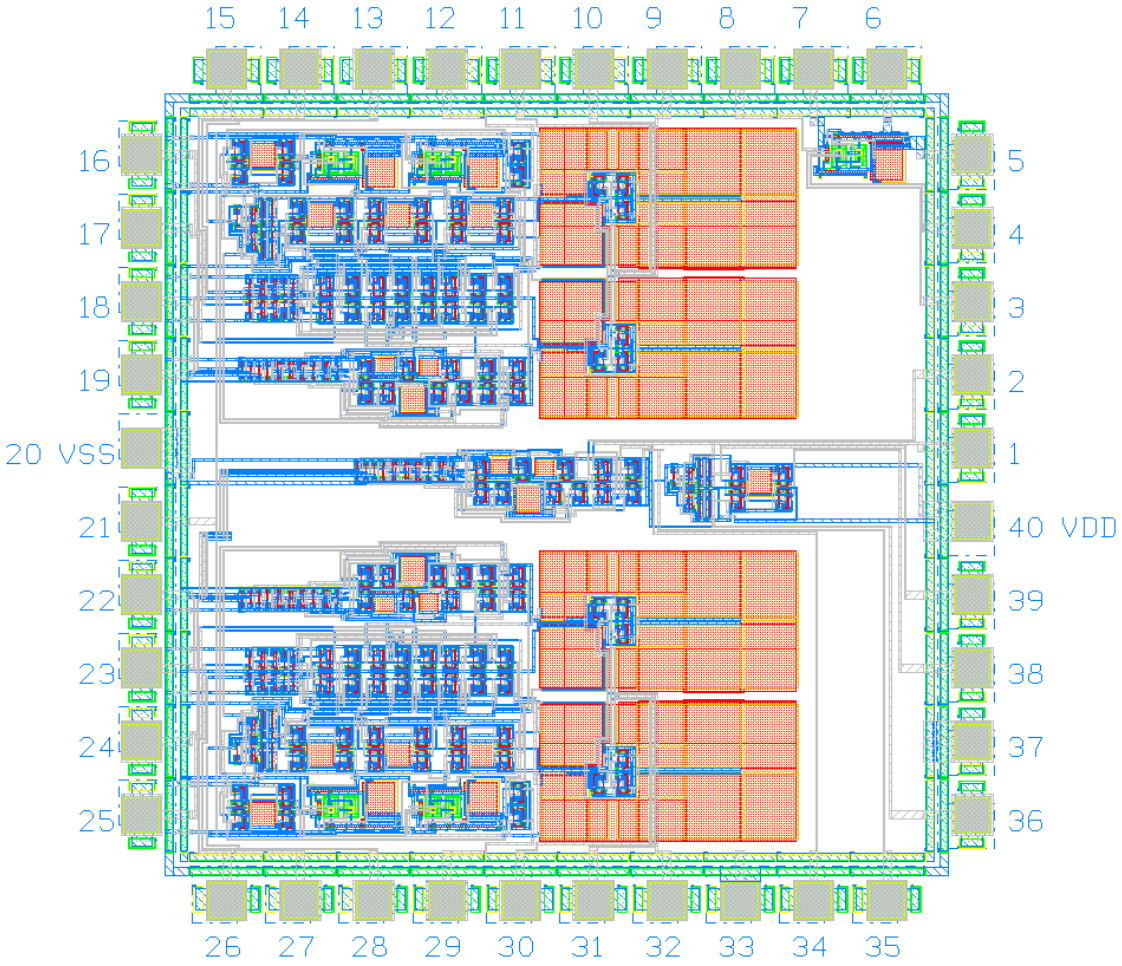

Figure 7.4. VLSI Layout of the Final Chip.

Table 7.1. Pin Identification.

Pad	Function
GND (21)	Chip Ground
Vss (20, 37)	Negative Power (-3.3 V)
Vdd (40, 33)	Positive Power (+3.3 V)
Clk1 In (13), Clk2 In (28)	Clock Input for GIC Filter
GIC1 Out (12), GIC2 Out (29)	Output Signal from GIC Filter
GIC1 In (16), GICII In (25)	Input Signal to GIC Filter
GIC1 S0-S1 (15, 14)	Topology Selection Bits for GIC Filter
GIC2 S0-S1 (26, 27)	Topology Selection Bits for GIC Filter
GIC1 S2-S4 (9, 10, 11)	Frequency Selection Bits for GIC Filter
GIC2 S2-S4 (32, 31, 30)	Frequency Selection Bits for GIC Filter
GIC1 S5-S7 (17, 18, 19)	Quality Factor Selection Bits for GIC Filter
GIC2 S5-S7 (24, 23, 22)	Quality Factor Selection Bits for GIC Filter
Opamp Vdd (6)	Test Opamp Positive Power (+3.3 V)
Opamp Vss (7)	Test Opamp Negative Power (+3.3 V)
Opamp Gnd (8)	Test Opamp Ground
Opamp + (4)	Test Opamp Non-Inverting Terminal
Opamp - (3)	Test Opamp Inverting Terminal
Opamp Out (5)	Test Opamp Output Terminal
Res In (39)	Test Bilinear Resistor Input Node
Res Out (38)	Test Bilinear Resistor Output Node
Vres In (2)	Test Variable Floating Bilinear Resistor Input Node
Vres Out (35)	Test Variable Floating Bilinear Resistor Output Node
Clock Input (34)	Test Non-Overlapping Clock Input Node
Clock Out Even (1)	Test Non-Overlapping Clock Even Output Node
Clock Out Odd (36)	Test Non-Overlapping Clock Odd Output Node

VIII. CONCLUSIONS AND RECOMMENDATIONS

The programmable GIC filter developed in several theses at NPS has undergone several changes over the course of this thesis research. First, a BiCMOS opamp was simulated and included in the design. Two CMOS opamps were tested by replacing n-channel MOSFETS with NPN bipolar transistors. A modified version of the opamp in LCDR Lee's thesis was selected. Switch simulation led to the development of an enhanced passgate with a minimized resistance. SPICE simulations of bilinear resistors showed a need to validate the model parameters and simulations with the fabricated design. The capacitor design from LCDR Lee's design was upgraded to a less voltage dependent design that uses two levels of polysilicon. The VLSI layout was completed and submitted for fabrication. The layout includes two independent programmable GIC filters, one BiCMOS opamp, one floating bilinear resistor, and one variable bilinear resistor. Further research and design are expected to further improve this design.

Although many avenues exist for furthering the development of the GIC filter, the area that needs the most emphasis is the testing of LCDR Lee's design and this design, especially, the operational amplifiers and bilinear resistors. Further research might include research into a filter with more functionality. Control inputs could be loaded serially into a register to control the filter operation. This would not limit the number of pins necessary for filter operation and could improve the range of selectable frequencies. Other approaches might include an implementation in Gallium Arsenide or in other new technologies. Whatever the chosen avenue, the programmable GIC filter has a tremendous amount to offer to the analog VLSI designer.

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APPENDIX

A. CONTENTS OF THE FILE T0AEBSIM3.TXT FROM MOSIS

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* MOSIS PARAMETRIC TEST RESULTS
* RUN: T0AE     VENDOR: AMI
* TECHNOLOGY: SCN15     FEATURE SIZE: 1.6 microns
* T0AE SPICE BSIM3 VERSION 3.1 PARAMETERS
* SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Dec  5/00
* LOT: T0AE                  WAF: 03
* Temperature_parameters=Default

.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 3.18E-8
+XJ      = 3E-7          NCH     = 7.5E16          VTH0    = 0.5688737
+K1      = 0.9793712     K2      = -0.0789892      K3      = 10.8093505
+K3B     = -4.4249704    W0      = 4.007982E-6     NLX     = 1E-8
+DVT0W   = 0             DVT1W   = 0               DVT2W   = 0
+DVT0    = 0.8727879     DVT1    = 0.3962478       DVT2    = -0.25866
+U0      = 640.0977349   UA      = 1.044798E-9     UB      = 2.152476E-
18
+UC      = 1.714891E-11  VSAT    = 1.089709E5      A0      = 0.6580654
+AGS     = 0.107293      B0      = 1.81304E-6      B1      = 5E-6
+KETA    = -3.881632E-3  A1      = 0               A2      = 1
+RDSW    = 3E3           PRWG    = -0.0171147      PRWB    = -0.0282865
+WR      = 1             WINT    = 6.141026E-7     LINT    = 2.622217E-
7
+XL       = 0                XW       = 0                DWG      = -
9.206316E-9
+DWB     = 3.515083E-8   VOFF    = -0.0370395      NFACTOR = 0.4940922
+CIT     = 0             CDSC    = 0               CDSCD   = 0
+CDSCB   = 3.315397E-5   ETA0    = -0.9976905      ETAB    = -0.3274482
+DSUB    = 0.9976896     PCLM    = 1.2264621       PDIBLC1 = 7.977558E-
3
+PDIBLC2 = 1.935464E-3   PDIBLCB = -0.1            DROUT   = 0.0556299
+PSCBE1  = 5.875324E9    PSCBE2  = 2.081686E-9     PVAG    = 0.1258073
+DELTA   = 0.01          RSH     = 54.4            MOBMOD  = 1
+PRT     = 0             UTE     = -1.5            KT1     = -0.11
+KT1L    = 0             KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0             WLN     = 1               WW      = 0
+WWN     = 1             WWL     = 0               LL      = 0
+LLN     = 1             LW      = 0               LWN     = 1
+LWL     = 0             CAPMOD  = 2               XPART   = 0.4
+CGDO    = 1.69E-10      CGSO    = 1.69E-10        CGBO    = 1E-9
+CJ      = 2.865531E-4   PB      = 0.99            MJ      = 0.5301804
+CJSW    = 1.354137E-10  PBSW    = 0.9793305       MJSW    = 0.1
+CF      = 0              )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 3.18E-8
+XJ      = 3E-7          NCH     = 2.4E16          VTH0    = -0.7422198
+K1      = 0.4570792     K2      = -2.847612E-6    K3      = 12.8110353
```

```
+K3B     = -1.7938551     W0      = 9.414664E-7    NLX     = 1E-6
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.1734001      DVT1    = 0.3735045      DVT2    = -0.0808532
+U0      = 256.3386879    UA      = 4.548803E-9    UB      = 1E-21
+UC      = -9.46031E-11   VSAT    = 2E5            A0      = 0.4170862
+AGS     = 0.2085241      B0      = 3.96061E-6     B1      = 5E-6
+KETA    = -5.078415E-3   A1      = 0              A2      = 0.364
+RDSW    = 3E3            PRWG    = 0.1003856      PRWB    = -0.051608
+WR      = 1              WINT    = 7.403092E-7    LINT    = 8.173497E-
8
+XL       = 0                 XW       = 0                 DWG      = -
3.168213E-8
+DWB     = 4.611425E-8    VOFF    = -0.0886289     NFACTOR = 0.2636937
+CIT     = 0              CDSC    = 1.13364E-4     CDSCD   = 1.076153E-
4
+CDSCB    = 0                 ETA0     = 0.06903          ETAB     = -
1.349554E-3
+DSUB    = 0.2873         PCLM    = 5.91338        PDIBLC1 = 1.435299E-
4
+PDIBLC2 = 1E-3           PDIBLCB = 4.52541E-3     DROUT   = 0.0888201
+PSCBE1  = 3.309414E9     PSCBE2  = 6.845333E-8    PVAG    = 9.8878091
+DELTA   = 0.01           RSH     = 79             MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.4
+CGDO    = 1.95E-10       CGSO    = 1.95E-10       CGBO    = 1E-9
+CJ      = 2.832532E-4    PB      = 0.73352        MJ      = 0.4211282
+CJSW    = 1.740847E-10   PBSW    = 0.99           MJSW    = 0.1361309
+CF      = 0               )


.MODEL QNL NPN(BF=130)
```

B. CONTENTS OF THE FILE T0AE.TXT FROM MOSIS

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* MOSIS PARAMETRIC TEST RESULTS
* RUN: T0AE     VENDOR: AMI
* TECHNOLOGY: SCN15     FEATURE SIZE: 1.6 microns
* T0AE SPICE LEVEL3 PARAMETERS
* DATE: Dec  5/00
* LOT: T0AE     WAF: 03

.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.1800E-08 XJ=0.200000U
TPG=1
+ VTO=0.6897 DELTA=0.0000E+00 LD=1.0250E-07 KP=7.2950E-05
+ UO=671.8 THETA=9.0430E-02 RSH=2.5430E+01 GAMMA=0.8102
+ NSUB=2.3320E+16 NFS=5.9080E+11 VMAX=2.0730E+05 ETA=1.1260E-01
+ KAPPA=3.1050E-01 CGDO=1.6696E-10 CGSO=1.6696E-10
+ CGBO=5.0828E-10 CJ=2.8655E-04 MJ=5.3018E-01 CJSW=1.3541E-10
+ MJSW=1.0000E-01 PB=9.9000E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.4578E-06
```

```
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.1800E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.7574 DELTA=2.9770E+00 LD=9.8570E-08 KP=2.0817E-05
+ UO=191.7 THETA=1.2020E-01 RSH=3.5220E+00 GAMMA=0.4246
+ NSUB=6.4040E+15 NFS=3.5000E+11 VMAX=2.6200E+05 ETA=1.4820E-01
+ KAPPA=1.0000E+01 CGDO=1.6055E-10 CGSO=1.6055E-10
+ CGBO=4.2370E-10 CJ=2.8325E-04 MJ=4.2113E-01 CJSW=1.7408E-10
+ MJSW=1.3613E-01 PB=7.3352E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.0582E-06

.MODEL QNL NPN(BF=130)
```

C. SPICE SUBCIRCUITS

```
*** SPICE Circuit File of CHIP made by LASICKT on 09/24/01 10:06:18 ***

.SUBCKT PADFRAME
.ENDS

.SUBCKT INV InvIn InvOut VDD VSS
M2 InvOut InvIn VSS VSS CMOSN L=2U W=3U
M1 InvOut InvIn VDD VDD CMOSP L=2U W=9U
.ENDS

.SUBCKT SWITCH SwIn SwOut Cntr1 Cntr2 VDD VSS
M2 SwOut Cntr1 SwIn VDD CMOSP L=2U W=23U
M1 SwOut Cntr2 SwIn VSS CMOSN L=2U W=7U
.ENDS

.SUBCKT PASSGATE PGIn PGOut PGCntl VDD VSS
X1 PGCntl Cntr1 VDD VSS INV
X2 PGIn PGOut Cntr1 PGCntl VDD VSS SWITCH
.ENDS

.SUBCKT VARCAP VCAPIN VCAPOUT FC0 FC1 FC2 VDD VSS
C1 VCAPOUT VCAPIN 13.0P
X1 VCAPIN VN3 FC0 VDD VSS PASSGATE
X2 VCAPIN VN2 FC1 VDD VSS PASSGATE
X3 VCAPIN VN1 FC2 VDD VSS PASSGATE
C2 VCAPOUT VN3 13.0P
C4A VCAPOUT VN1 13.0P
C3A VCAPOUT VN2 13.0P
C3B VCAPOUT VN2 13.0P
C4B VCAPOUT VN1 39.0P
.ENDS

.SUBCKT OPAMP VIN+ VIN- VOUT VDD VSS GND
Q1 VN1 VIN- VN5 QNL
Q2 VN2 VIN+ VN5 QNL
M3 VN5 VN4 VSS VSS CMOSN  W= 27U  L= 5U
M4 VN4 VN4 VSS VSS CMOSN  W= 13U  L= 5U
M5 VDD GND VN4 VN4 CMOSN  W= 5U  L= 33U
```

```
M9 VDD VN2 VOUT VDD CMOSP  W= 150U  L= 5U
M6 VOUT VN4 VSS VSS CMOSN  W= 67U  L= 5U
C1 VOUT VN3 3.25P
M10 VN3 VSS VN2 VDD CMOSP  W= 5U  L= 5U
M7 VN1 VN1 VDD VDD CMOSP  W= 30U  L= 5U
M8 VN2 VN1 VDD VDD CMOSP  W= 30U  L= 5U
.ENDS

.SUBCKT BILIN EVEN ODD BIN BOUT VDD VSS
X3 VN2 BOUT ODD VDD VSS PASSGATE
X2 BIN VN1 ODD VDD VSS PASSGATE
X1 BIN VN2 EVEN VDD VSS PASSGATE
X4 VN1 BOUT EVEN VDD VSS PASSGATE
C1 VN2 VN1 2.00P
.ENDS

.SUBCKT NOR2 INA INB OUT VDD VSS
M3 OUT INA VSS VSS CMOSN L=2U W=3U
M4 OUT INB VSS VSS CMOSN L=2U W=3U
M1 VN1 INA VDD VDD CMOSP L=2U W=9U
M2 VN1 INB OUT VDD CMOSP L=2U W=9U
.ENDS

.SUBCKT INV_LG InvIn InvOut VDD VSS
M1 InvOut InvIn VDD VDD CMOSP L=2U W=40U
M2 InvOut InvIn VSS VSS CMOSN L=2U W=12U
.ENDS

.SUBCKT CLOCK EVEN ODD CIN VDD VSS
X2 ODD VN1 VN2 VDD VSS NOR2
X3 EVEN CIN VN4 VDD VSS NOR2
X4 VN2 VN3 VDD VSS INV_LG
X6 VN3 EVEN VDD VSS INV_LG
X5 VN4 VN5 VDD VSS INV_LG
X7 VN5 ODD VDD VSS INV_LG
X1 CIN VN1 VDD VSS INV
.ENDS

.SUBCKT NAND2 INA INB VN1 VDD VSS
M3 VN2 INA VSS VSS CMOSN L=2U W=3U
M1 VN1 INA VDD VDD CMOSP L=2U W=6U
M4 VN2 INB VN1 VSS CMOSN L=2U W=3U
M2 VN1 INB VDD VDD CMOSP L=2U W=6U
.ENDS

.SUBCKT TOPO S0 S1 TC0 TC1 TC2 TC3 TC4 TC5 TC6 TC7 VDD VSS
X1 S0 TC4 VDD VSS INV
X2 S1 VN1 VDD VSS INV
X3 VN1 TC4 TC7 VDD VSS NAND2
X4 S1 S0 TC2 VDD VSS NAND2
X5 TC2 TC7 TC1 VDD VSS NAND2
X6 S0 VN1 VN2 VDD VSS NAND2
X7 TC1 TC0 VDD VSS INV
X8 VN2 TC5 VDD VSS INV
X9 TC7 TC6 VDD VSS INV
X10 TC2 TC3 VDD VSS INV
.ENDS
```

```
.SUBCKT QFACT S5 S6 S7 QC0 QC1 QC2 QC3 QC4 QC5 QC6 VDD VSS
X4 VN1 QC3 VDD VSS INV
X3 S7 VN1 VDD VSS INV
X2 S6 QC4 VDD VSS INV
X1 S5 QC1 VDD VSS INV
X5 QC1 QC4 VN3 VDD VSS NAND2
X6 QC1 QC3 VN2 VDD VSS NAND2
X7 VN2 VN3 QC2 VDD VSS NAND2
X8 QC4 QC6 VDD VSS INV
X9 QC6 QC1 QC5 VDD VSS NOR2
X10 QC1 QC0 VDD VSS INV
.ENDS

.SUBCKT FBR S5 S6 S7 VRIN VROUT EVEN ODD VDD VSS
C1 VN2 VN5 2.00P
C2 VN4 VN3 1.00P
C3 VN6 VN7 1.00P
X8 S5 S6 S7 QC0 QC1 QC2 QC3 QC4 QC5 QC6 VDD VSS QFACT
X1 VN4 VN6 QC5 VDD VSS PASSGATE
X2 VN5 VN4 QC4 VDD VSS PASSGATE
X3 VN3 VN7 QC2 VDD VSS PASSGATE
X4 VN5 VN6 QC6 VDD VSS PASSGATE
X5 VN2 VN4 QC3 VDD VSS PASSGATE
X6 VN1 VN3 QC0 VDD VSS PASSGATE
X7 VN1 VN2 QC1 VDD VSS PASSGATE
X11 VN1 VROUT ODD VDD VSS PASSGATE
X10 VRIN VN6 ODD VDD VSS PASSGATE
X9 VRIN VN1 EVEN VDD VSS PASSGATE
X12 VN6 VROUT EVEN VDD VSS PASSGATE
.ENDS

.SUBCKT FILTER
X1 VA1 VM1 S4 S3 S2 VN2 VSS VARCAP
X2 VEE VHH S4 S3 S2 VDD VSS VARCAP
X3 VP1 VM1 VA1 VDD VSS GND OPAMP
X4 VP2 VM1 VA2 VDD VSS GND OPAMP
X5 EVN ODD VA2 VM1 VDD VSS BILIN
X6 EVN ODD VCC VP1 VDD VSS BILIN
X7 EVN ODD VAA VPP VDD VSS BILIN
X8 EVN ODD VP2 VA1 VN2 VSS BILIN
X9 EVN ODD CIN VDD VSS CLOCK
X11 VM1 OUT TC1 VDD VSS PASSGATE
X12 VA2 OUT TC0 VDD VSS PASSGATE
X13 VAA VA2 TC6 VDD VSS PASSGATE
X14 VAA GND TC7 VDD VSS PASSGATE
X15 VA2 VCC TC0 VDD VSS PASSGATE
X16 VA2 VHH TC3 VDD VSS PASSGATE
X17 VPP VP1 TC2 VDD VSS PASSGATE
X18 VHH GND TC5 VDD VSS PASSGATE
X19 VP1 VEE TC3 VDD VSS PASSGATE
X20 VHH VIN TC4 VDD VSS PASSGATE
X21 VEE VP2 TC2 VDD VSS PASSGATE
X22 VCC VIN TC1 VDD VSS PASSGATE
X23 VP2 VPP TC3 VDD VSS PASSGATE
X24 VIN VJJ TC5 VDD VSS PASSGATE
X25 VP2 VKK TC2 VDD VSS PASSGATE
```

```
X26 VJJ GND TC3 VDD VSS PASSGATE
X27 VKK VA1 TC3 VDD VSS PASSGATE
X28 VJJ VM1 TC4 VDD VSS PASSGATE
X10 S0 S1 TC0 TC1 TC2 TC3 TC4 TC5 TC6 TC7 VDD VSS TOPO
X30 S5 S6 S7 VJJ VKK EVN ODD VDD VSS FBR
.ENDS
```

D. SAMPLE SMARTSPICE FILE

```
Non-Overlapping Clock

.INCLUDE t0aeBSIM3.txt

.PARAM FREQ = 1MEG
.PARAM PERIOD = '1/FREQ'
.PARAM DUTY = 'PERIOD/10'
.PARAM DUR = 'PERIOD'
.PARAM OFFSET = 'DUR/2'
.PARAM POINTS = 'PERIOD/1000'
.PARAM WIDTH = 18U
.PARAM RES = 1k
.PARAM MAG = 3.3
.PARAM SKEW = '0.01*PERIOD'

* Power Supplies
VDDD   VDD   0   3.3
VSSS   VSS   0  -3.3

* Input Signals
*VIN  INPUT  0  DC 0  SIN(0 1.0 'FREQ/200')
VC1  CIN    0  PULSE(MAG '-MAG' 1n SKEW SKEW 'DUTY*5' PERIOD)

*** SPICE Circuit File of CLOCK made by LASICKT on 08/30/01 13:16:38
***

.SUBCKT NOR2 INA INB OUT VDD VSS
M3 OUT INA VSS VSS CMOSN L=2U W=3U
M4 OUT INB VSS VSS CMOSN L=2U W=3U
M1 VN1 INA VDD VDD CMOSP L=2U W=9U
M2 VN1 INB OUT VDD CMOSP L=2U W=9U
.ENDS

.SUBCKT INV_LG InvIn InvOut VDD VSS
M1 InvOut InvIn VDD VDD CMOSP L=2U W=40U
M2 InvOut InvIn VSS VSS CMOSN L=2U W=12U
.ENDS

.SUBCKT INV InvIn InvOut VDD VSS
M2 InvOut InvIn VSS VSS CMOSN L=2U W=3U
M1 InvOut InvIn VDD VDD CMOSP L=2U W=9U
.ENDS

*MAIN CIRCUIT CLOCK
X2 ODD VN1 VN2 VDD VSS NOR2
X3 EVEN CIN VN4 VDD VSS NOR2
```

```
X8  VN2 VN6 VDD VSS INV
X9  VN6 VN7 VDD VSS INV
X10 VN4 VN8 VDD VSS INV
X11 VN8 VN9 VDD VSS INV

X4 VN7 VN3 VDD VSS INV_LG
X6 VN3 EVEN VDD VSS INV_LG
X5 VN9 VN5 VDD VSS INV_LG
X7 VN5 ODD VDD VSS INV_LG
X1 CIN VN1 VDD VSS INV

* Simulation Parameters
.TRAN POINTS '4*DUR'

.SAVE v(CIN)
.SAVE v(ODD)
.SAVE v(EVEN)
.SAVE v(VN7)
.SAVE v(VN9)
.END
```

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