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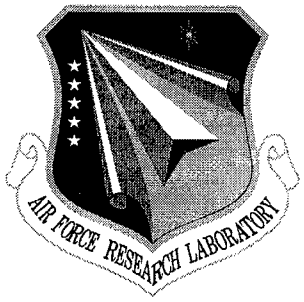

INTEGRATED MICROELECTROMECHANICAL SYSTEM (MEMS) INERTIAL MEASUREMENT UNIT (IMIMU)

Carnegie Mellon University

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13. ABSTRACT *(Maximum 200 words)*

Processes, designs and design tools are developed to enable the monolithic integration of arrays of inertial microsensors with electronics. Accelerometers and gyroscopes, fabricated in a single CMOS process, are functional and demonstrate a single chip IMU. Two integrated post CMOS micro-machining processes are demonstrated. Thin-film microstructures are defined from the metal-dielectric stack of a conventional process. In the second process, a back-side silicon etch, followed by front-side DRIE produces bulk silicon microstructures.

Accelerometer and gyroscope designs are developed with accompanying low noise electronic circuitry. Noise performance was limited to 1/f circuit noise. The chip output sensibility is set by the interface circuit design. A thermally stabilized accelerometer and circuit design is demonstrated using embedded polysilicon resistors as temperature sensors and heaters in a closed loop. Nested gyroscope topologies are demonstrated with a lateral MEMS accelerometer used as a coriolis acceleration sensor.

Modeling and simulation tools that simultaneously consider the electromechanical transducer and the electronic circuit to predict system performance are developed. Electrical, electromechanical and mechanical parasitics required to enable predictive lumped parameter simulation are identified and can be extracted, enabling a designer to confidently estimate design performance prior to fabrication. Generic physics-based fault models for surface-micromachined actuators and sensors are developed that enable effective testing, diagnosis and design for manufacturability.

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Abstract

Processes, designs and design tools are developed to enable the monolithic integration of arrays of inertial microsensors with electronics. Lateral-axis and vertical-axis accelerometers and lateral-axis and vertical-axis gyroscopes made in a single CMOS process are functional and demonstrate the feasibility of a single-chip inertial measurement unit. Two integrated post-CMOS micromachining processes, which are used to fabricate inertial sensors, are demonstrated. In the first process, thin-film microstructures are defined from the metal-dielectric stack fabricated in conventional CMOS processes, enabling low-cost integration of CMOS electronics with MEMS sensors. In the second process, a timed back-side silicon etch followed by deep reactive-ion etching of the front-side substrate produces bulk silicon microstructures with metal-dielectric microstructure connected on top. This second process is favorable for applications where the mechanical properties of single-crystal silicon may be exploited, and where more proof mass is desirable.

Several accelerometer and gyroscope designs as well as low noise and thermally stable electronic circuit designs are developed. The CMOS-MEMS accelerometers have noise between 0.1 to 0.5 mg/$\sqrt{\text{Hz}}$ for lateral designs, and 6 mg/$\sqrt{\text{Hz}}$ for vertical designs. The noise performance in both the accelerometers and gyroscopes is limited by 1/f circuit noise in the digital CMOS, not thermomechanical noise. Transducer sensitivity ranges from 0.5 to 1 mV/g/V. As amplifiers can be included on chip, the chip output sensitivity is set by the interface circuit design. A thermally stabilized accelerometer design with a temperature insensitive capacitive sensing circuit is demonstrated. Embedded polysilicon resistors in the microstructure act as temperature sensors and heaters in a closed loop to control the local temperature of the microstructure. Using the lateral CMOS-MEMS accelerometer as a coriolis acceleration sensor, nested gyroscope topologies are demonstrated with 0.03 °/s/$\sqrt{\text{Hz}}$ for z-axis, and 1 % linearity between ±1 rev/s.

Modeling and simulation tools that simultaneously consider the electromechanical transducer and the electronic circuit to predict system performance are developed. Electrical, electromechanical, and mechanical parasitics required to enable predictive lumped parameter simulation are identified, and can be extracted enabling a designer to confidently estimate design performance prior to fabrication. Generic physics-based fault models for surface-micromachined actuators and sensors are developed that enable effective testing, diagnosis and design for manufacturability.

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1. Summary

The goal of this project is development of an Integrated MEMS Inertial Measurement Unit (IMIMU) as a monolithically integrated microsystem, taking advantage of developing capabilities for the design and implementation of *application-specific single-chip* MEMS. Successful implementation utilizes a CMOS-compatible MEMS process, and design complexity is managed through the use of hierarchical design methodology. The resulting effort developed CMOS-based MEMS processes, component designs and computer-aided design (CAD) tools that ensure first-pass success in fabrication of the IMIMU and other integrated MEMS.

The IMIMU integrates arrays of accelerometers and gyroscopes with analog signal conditioning circuitry and digital signal processing (DSP). The individual inertial sensors provide raw data with imperfections such as finite offsets, finite cross-axis sensitivities, and limited range. Data from an array can be combined to compensate for these imperfections. Ultimately, on-chip fusion of the sensor signals can be accomplished by digitizing the signals and using DSP.

Due to the need for integration of microsensors with electronics, the IMU is implemented in a post-CMOS micromachining fabrication process. Micromechanical devices are made from the CMOS interconnect dielectric and metal layers. CMOS electronics may be placed nearby the microstructures; the conservative design rule for spacing of electronics from microstructures is 30 μm. We have primarily used the Hewlett-Packard (HP) 3-metal 0.5 μm n-well process from MOSIS for our starting CMOS fabrication. After the foundry completes the CMOS processing, a reactive-ion etch (RIE) of the stacked CMOS dielectric layers is used to define composite dielectric/metal microstructures. Following the dielectric etch, a plasma etch undercuts the microstructures for release. This process has advantages of full integration of MEMS and circuits, low cost, rapid prototyping, accessibility, very low parasitic capacitances, and the ability to place multiple isolated conductors on movable structures. The thin-film CMOS-MEMS process just described may be augmented to include deep Si RIE structures. This relatively new process has advantages of providing larger proof mass and more stable Si springs. Some prototype devices are tested, however the more mature inertial sensors within this project are fabricated in the thin-film CMOS-MEMS process.

Topologies are designed, fabricated and tested for all six degrees of freedom in an IMU. All devices have their noise performance currently limited by the interface circuit flicker noise, which

is relatively high in the digital CMOS processes. Improvement of these circuits is one topic for further research and development The lateral (x-axis or y-axis) accelerometer topology is implemented in several different sizes, with several different interface circuits. A perforated plate proof mass is suspended by four meander springs at the corners. A cantilevered semi-rigid frame for stator comb fingers is designed to curl in the same manner as the rotor fingers. This special design ensures aligned finger sidewalls to maximize capacitance and sensitivity. The best lateral accelerometer design to date provides 100 $\mu g/\sqrt{Hz}$ noise performance. The vertical (z-axis) accelerometer uses a similar topology, except that the spring suspension is made soft in the vertical direction and stiff in the lateral directions. The vertically compliant spring is made with relatively thin microstructures using only the first CMOS metal interconnect layer. The vertical-axis vibratory rate gyroscope incorporates an x-axis accelerometer inside a mechanically and electrically decoupled suspension. The accelerometer within the gyroscope reuses the topology from the lateral accelerometer. It is dithered in the y-axis with an electrostatic comb drive. The accelerometer then detects motion from coriolis acceleration arising from chip rotation about the z-axis. The best z-axis gyroscope design to date has a $0.03°/s/\sqrt{Hz}$ noise floor. The lateral-axis vibratory-rate gyroscope design has the same topology as the vertical-axis gyroscope, except the accelerometer is dithered vertically along the z axis. This actuation is accomplished with special vertical electrostatic comb drives. Separate electrodes are routed to the top and bottom of each comb finger to provide an independent control force for pulling up or down on the frame surrounding the accelerometer.

Management of curl in the microstructures is an important aspect of thin-film CMOS-MEMS design. One robust way of controlling comb finger alignment is to stabilize the temperature of the device. Thermal stabilization of a CMOS vertical-axis accelerometer is successfully demonstrated with current flow through polysilicon heater resistors embedded within the stator and rotor structures. Initial testing demonstrates a ten-fold reduction in temperature sensitivity over a 70°C range.

Design complexity is managed using the top-down design methodology and associated tools developed at Carnegie Mellon. For this project, we have used the modeling and simulation capabilities developed under DARPA/MTO Composite CAD 96-16 project on "Foundations for Microelectromechanical System Synthesis" and have developed CAD algorithms for the back-end of this

design methodology: feature recognition for extraction and MEMS testing. Extraction involves converting the design layout into a schematic with parasitics that can be simulated in NODAS (NOdal Design of Actuators and Sensors) thereby enabling design verification. The MEMS testing task has developed generic fault models for surface-micromachined actuators and sensors that enable effective testing, diagnosis and design for manufacturability.

All designs are saved and documented through schematic and layout representations in the CAD tools. These designs constitute a set of inertial-MEMS intellectual property, which can be reused to make new devices, or can be combined to form inertial sensor arrays, or can be improved and augmented with signal processing electronics and digital interfaces.

2. Introduction

The IMIMU has a direct insertion path in a variety of high-impact military and commercial applications. Its targeted performance of down to 40 °/hr rotational rate bias drift and 100 μG accelerometer bias can be used to fill in gaps in primary GPS land navigation when reception is blocked or when spurious signals are received. The system will fulfill less demanding specifications (e.g., 1°/min drift) required for robotic control applications, most notably head tracking for virtual reality systems and platform stabilization for vehicles.

An on-chip inertial measurement unit requires a very high level of integration. In a brute-force approach, at least six inertial sensors, one for each degree-of-freedom (x, y, z, θ_x, θ_y, θ_z) must be integrated on chip. Inclusion of fewer sensors may be possible by detecting multiple degrees of freedom in single-transducer elements. For example, it is possible to create a single-transducer tri-axial accelerometer. More sensors may be desirable for extended range operation, redundancy, or to perform additional measurements for systematic error compensation.

Precision alignment of the relatively large number of IMU components is accomplished by design with on chip integration. Capacitive inertial sensors have better sensitivity when the parasitic capacitance on high-impedance output nodes is minimized, as is the case when interface electronics are combined on chip. Ultimately, it is desirable to combine all computation on chip to achieve the most compact size. Therefore, the approach in this project is to develop the IMIMU in a base technology that will support full system-on-chip integration of MEMS, analog and digital sub-systems.

The base fabrication, device and design technology to create the IMIMU has been developed and demonstrated in this project.

Several MEMS processes are possible for integration of inertial sensors. The microfabrication approach taken in this project is a form of post-CMOS micromachining in which foundry digital CMOS is used as the starting technology platform. In the post-CMOS micromachining, micromechanical structures are dry etched out of the thin-film dielectric and metal interconnect stack made as part of the CMOS "back-end" process steps. The microstructures are released by dry etching the underlying silicon substrate. Other post-CMOS micromachining uses wet silicon etching, or adds other low-temperature microstructural materials. The initial development of the post-CMOS micromachining technology for this project started in 1995 in conjunction with the DARPA-supported "Silicon Micro-Disk Drives for Data Storage" project [1]. The IMIMU project continued development of this base technology for inertial sensor applications.

Leveraging conventional CMOS processing for the IMIMU enables fast, reliable, repeatable, economical IM fabrication. Integrated MEMS capabilities, built into the process, improve with the scaling of CMOS technology. Specific advantages to post-CMOS micromachining are access to sub-micron design rules, fast CMOS transistors, low parasitic capacitance (*i.e.,* excellent capacitive sensor performance), gate polysilicon for embedded thermal control heating elements, and rapid fabrication turnaround of two to three months.

The second key technology developed in the project is a design methodology and tools to support computer-aided design of the complete inertial measurement system. MEMS device design tools are well established, and rely heavily on finite-element analysis of micromechanics and boundary element analysis of electrostatics. These direct numerical analysis techniques become bogged down in execution time and resource consumption when the complexity approaches that of an integrated inertial sensor, and especially for systems with multiple integrated sensors. A new MEMS system design methodology and supporting tools are required for the IMIMU design.

The foundations of the MEMS system design methodology originated with the DARPA Composite CAD project "Foundations of MEMS Synthesis," started in 1996. In this prior project, a schematic-based design was introduced for MEMS, in which basic beam, plate, anchor, and electrostatic gap elements were used in a hierarchical fashion to build devices. The tools are built on a

standard electronic design automation framework, the Cadence Design Environment. The enhanced environment provides a way to design and simulate microelectromechanical structures combined with electronics. Behavioral models of the schematic elements are implemented in an analog hardware definition language. Other interoperable elements may be added by simply conforming to the model pin conventions.

As part of the IMIMU project, the system design tools are further enhanced. Developments include refined models, automatic layout generation and layout extraction of elements, faults and parasitic capacitance. Detailed models of CMOS micromachined beams and gaps are critical to simulation accuracy. Manual layout in multi-layer CMOS processes is extremely tedious and prove to error. Schematic to layout generators provide an important productivity enhancement. Extraction is crucial to verifying the correctness of layout prior to submission to a foundry. Automated extraction to schematic with embedded parasitic elements provides such verification.

3. Methods, Assumptions, Procedures

3.1 IMIMU Fabrication

Fabrication of the IMIMU is accomplished using the post-CMOS micromachining technology developed at Carnegie Mellon University. Our choice of CMOS micromachining is based on the ability to form monolithically integrated MEMS with electronics, the high accessibility and low cost of the process, and the ease in performing technology transfer for commercialization.

Foundry digital CMOS is the starting point for the fabrication. CMOS foundries used in the project include Agilent (formerly Hewlett-Packard) 3-metal 0.8 μm, 3-metal 0.5 μm and 4-metal 0.35 μm CMOS, TSMC 3-metal 0.35 μm CMOS, AMS 3-metal 0.6 μm CMOS and UMC 6-metal copper low-k dielectric 0.18 μm CMOS. The primary starting processes in the project are the Agilent 3-metal 0.5 μm CMOS and AMS 3-metal 0.6 μm CMOS. All processes, except from AMS and UMC, are accessed through the Information Science Institute (ISI) MOS Implementation Service (MOSIS).

The post-CMOS processing provides composite micromechanical structures formed from the CMOS dielectric and metallization layers. MEMS devices first start with completion of the CMOS process flow. Reactive-ion etch of the exposed dielectric layers on individual CMOS dice is

performed in a Plasma-Therm 790 reactor with CHF_3 and O_2 gases. The metal interconnect layers act as an etch mask. Etch parameters are chosen to produce straight sidewalls in the dielectric layers, while not completely eroding the metal etch mask. The etch is timed to stop at the silicon substrate. The dice are then transferred to a Surface Technology Systems (STS) inductively coupled plasma system that runs the Bosch deep silicon RIE process. Trenches with nominal depth of 20 to 50 μm are etched into the silicon substrate. This depth sets the spacing between the microstructures and the substrate. The STS equipment is then setup to perform an isotropic silicon etch, which undercuts the microstructures and releases them from the substrate. This step is usually set for around 15 μm lateral etch, but can be modified depending on the user's objective. Wafer-scale post-CMOS micromachining is not in the scope of this effort, and is covered in another DARPA/MTO sponsored project, "Application-Specific Integrated MEMS Process Service."

Several features of the post-CMOS micromachining allow new design concepts to be implemented, which improve inertial sensor performance. Parasitic capacitance on high-impedance capacitive sense nodes can be kept extremely small. Sensor signals are routed on aluminum interconnect with low capacitance to ground to electronics as close as 30 μm from the sensor etch pit. Therefore, in a proper design, the parasitic capacitance is limited by the gate capacitance of the sense transistor. Multiple conductors may be built into micromechanical beams, enabling novel capacitive sensor and electrostatic actuator designs. Full-bridge differential sensing and actuation is

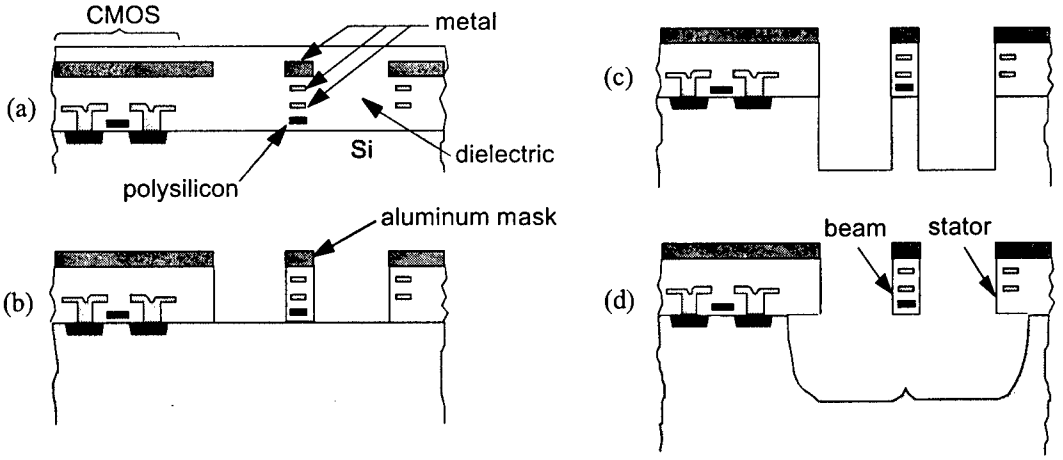


FIGURE 1. Cross-sections of the post-CMOS micromachining process flow. (a) After CMOS processing. (b) Directional oxide etch. (c) Silicon DRIE (d) Isotropic silicon etch for release.

achievable, as are common-centroid sense capacitor topologies. Built-in polysilicon heater resistors, thermistors, and aluminum/polysilicon thermocouples are available to implement oven control of micromechanical devices. Temperature stabilization eliminates a major source of bias drift in inertial sensors.

The primary potential disadvantages of the post-CMOS micromachining process are the large compressive residual stress and stress gradients in the micromechanical structures. The residual stress (around 69 MPa) can cause fixed-fixed structures to buckle. Stress gradients cause out-of-plane curl. Very thin beams can experience lateral curl from misalignment of inner metal layers in the beams. The various deleterious stress effects are mitigated through appropriate design techniques. Other effects to consider are reliability and bias drift from charging of dielectrics. Qualitative results show that the microstructures are robust unless subjected to stresses over the fracture stress (around 1% strain), however long-term studies are not available and are outside the scope of this project. Also, long term studies of bias drift are not currently available.

3.2 Inertial Sensor Design

The effort is focused on demonstrating CMOS-MEMS inertial sensor designs in all six degrees of freedom (DOF) for eventual integration on a single chip. The overarching strategy is to develop the IMIMU hierarchically by first developing subsystems, then device systems, then the full array. All of the sensors leverage the excellent capacitive detection performance achievable from CMOS micromachined structures with on-chip interface circuits. The basic MEMS design concepts are reused for all of the sensors. Many of the subsystems are reused across sensors.

Development in this project is focused on four primary single-axis sensor topologies: a lateral axis accelerometer, a vertical axis accelerometer, a lateral axis gyroscope, and a vertical axis gyroscope. Single-DOF lateral-axis accelerometers and gyroscopes are simply rotated by 90° to achieve two-axis sensing. Variations are designed with different sizing of proof masses, springs and combs. Devices have other variation of comb placement and inclusion of self-test combs. An additional vertical-axis accelerometer topology is independently developed to demonstrate on-chip thermal stabilization techniques.

The primary topology for the inertial sensors is shown in Figure 2. Proof mass is made from

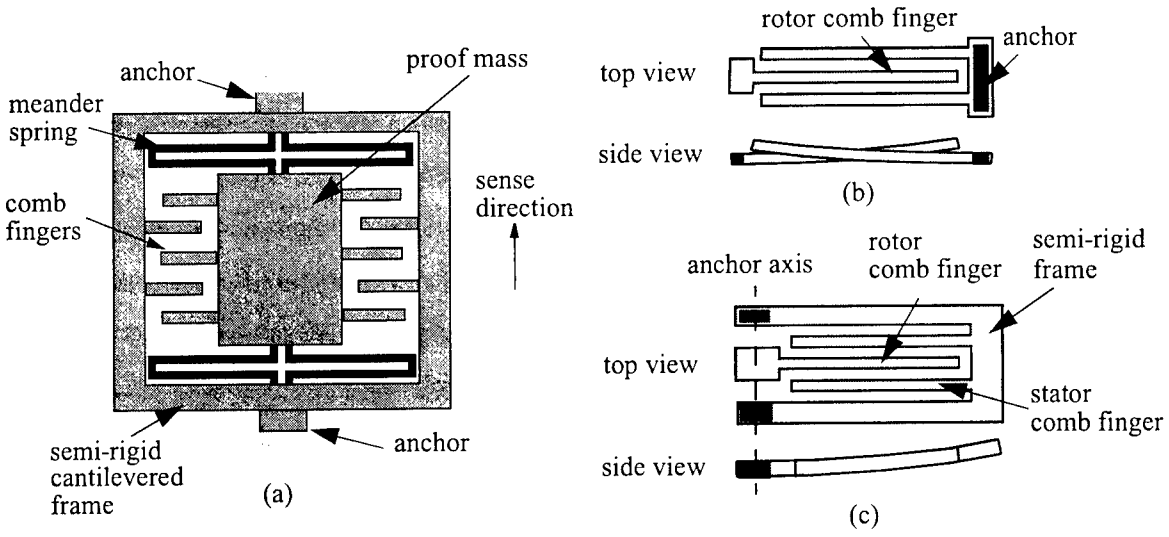


FIGURE 2. Primary post-CMOS micromachined inertial sensor topology. (a) Layout view. (b) Comb fingers without curl matching frame, (c) Comb fingers with cantilevered curl matching frame.

perforated multilayer metal-dielectric plates in the thin-film CMOS micromachining process, and from bulk silicon plates in the DRIE CMOS MEMS process. A 150 μm by 350 μm by 5 μm-thick plate mass made from the CMOS interconnect layers has about 4 μg of mass. The bulk silicon plates use the metal-dielectric layers on their topmost surface for interconnect, but have much more mass than the thin-film counterparts. Most of the suspension topologies in the designs are made from meander beam springs to achieve lower than 1 N/m spring constant in a compact area. For example, a five-meander spring with 120 μm-long 2.1 μm-wide 5 μm-thick beams made from the CMOS interconnect layer stack has a spring constant of 0.1 N/m. The 4 μg mass and 0.1 N/m spring provides a 36 nm/G sensitivity. The accelerometers have damping dominated at 1 atm by squeeze damping of the comb fingers. A typical quality factor is 10, leading to a thermomechanical (Brownian) noise of 27 $\mu G/\sqrt{Hz}$ for a 4 μg mass.

Motion sensing is accomplished with interdigitated comb finger arrays, which maximize capacitance for a given design area constraint. Separate comb finger arrays may be designed for use as electrostatic actuators for self test or for dithering of proof mass for vibratory-rate gyroscopes. Minimum finger-to-finger gaps and maximum structural height provide the most capacitance. Lateral motion sensing is performed by sensing the change in finger-to-finger parallel-plate capaci-

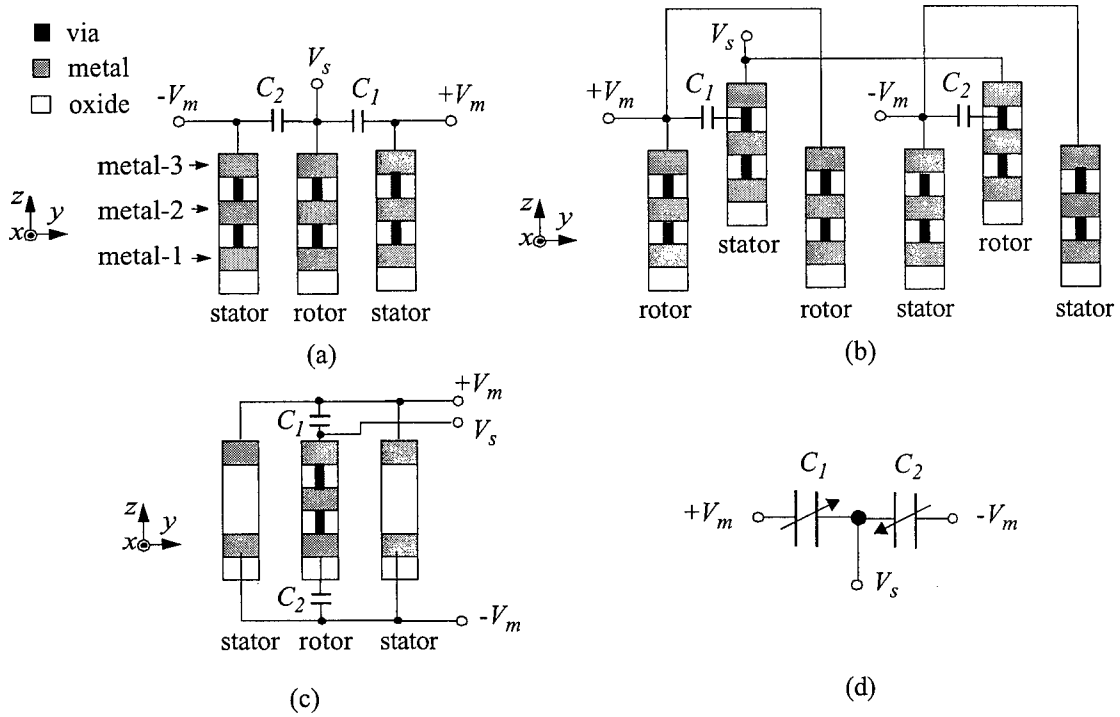


FIGURE 3. Comb-finger cross-sections for capacitive sensing and electrostatic actuation. (a) Cross-section of lateral-axis comb fingers. (b) Cross-section of vertical-axis comb fingers with vertical offset. (c) Cross-section of vertical-axis comb fingers with embedded bridge electrodes. (d) Equivalent sensing circuit for all comb configurations.

tance as a function of gap distance, as indicated in Figure 3(a). Vertical motion sensing is performed in one of two ways. The change in capacitance in fingers that are offset vertically may be sensed, as shown in Figure 3(b). Alternatively, the embedded conductors in each beam may be wired to form a capacitive bridge, as shown in Figure 3(c) [47][53][75]. With this electrode arrangement, there exists a significant capacitive sensitivity to vertical motion even when the fingers are aligned vertically.

In most cases, comb finger electrodes are connected in a capacitive divider configuration, as shown in Figure 3(d). The modulation signals, V_{m+} and V_{m-}, are supplied across the divider, and are either sinusoidal or square wave signals depending on the choice of interface electronics. The high-impedance sense node, V_s, is routed to the interface electronics. The sense node must be carefully routed to minimize parasitic capacitance to the substrate and to avoid any capacitive coupling to other signal lines. By adding more comb finger arrays, the capacitive sense circuit can be made

fully differential to reject common mode interference and with a common-centroid layout to reject offsets from linear manufacturing variations across the chip. A typical design has 40 5 μm-tall rotor fingers, finger overlap of 50 μm and gap of 1.5 μm. The total capacitance in the bridge is then about 120 fF, or 30 fF per capacitor. The sensitivity is around 20 aF/nm for lateral motion and 6 aF/nm for vertical motion. Given the 4 μg mass and 0.1 N/m spring example, the sensitivity is 0.7 fF/G. Assuming a total parasitic capacitance to ground of 120 fF on the inputs, the sensitivity of the example capacitive bridge is 12 mV/G/V, normalized to the voltage applied across the bridge.

Almost all of the accelerometers and gyroscopes developed in this effort display two-axis symmetry, which provides a balanced structure that is not prone to cross-axis mechanical coupling. Most devices are anchored at two opposing sides along a central axis, as shown in Figure 2. This anchor configuration allows design of cantilevered semi-rigid stator frames. This frame plays an important role in compensating for curl in the microstructures. Composite metal-dielectric structural layers made from the CMOS interconnect experience larger vertical stress gradient than their homogenous polysilicon counterpart and tend to curl out-of-plane. The typical radius of curvature of the structural layer can be relatively small, between 1 mm to 5 mm, compared with a radius of curvature at the order of hundreds of millimeters in an optimized polysilicon surface-micromachining technology. Without proper design, proof-mass fingers and stator fingers will curl in opposing directions as shown in Figure 12(b) and the sidewall sensing capacitance will be significantly reduced. Moreover, the sidewall capacitance will change dramatically with temperature and from run to run. The design technique shown in Figure 12(c) takes advantage of good local matching of curl to solve the problem of indeterminate sidewall capacitance. The stator sense fingers are connected to the frame such that their vertical curl matches the curl of the rotor fingers. Both stator and rotor structures are anchored along a common axis. As a result, the interdigitated fingers will curl in line and provide maximum sidewall capacitance.

3.3 Capacitive Interface Circuits

All of the inertial sensors developed in this project detect proof mass motion with micromechanical sidewall capacitive transduction. Each capacitive sensor is custom designed, however all designs have shared many characteristics. Different designers developed each inertial sensor with different interface circuits. These interface circuits must provide a stable dc voltage bias at their

input. Three primary interface circuit concepts are explored. The first topology is a simple input buffer amplifier with diode for dc biasing. The second topology is a transconductance amplifier, with a threshold-biased transistor for dc feedback to the input node. The third topology is a buffer amplifier with a reset switch transistor for dc biasing. Each of these topologies have positive and negative attributes that will be discussed in the results sections.

The values from the accelerometer example give order-of-magnitude estimates and set the expectation of the interface electronics. Electronics must be able to measure sub-attofarad capacitance changes of capacitances with nominal values of 10's of femtofarads. The equivalent Brownian noise referred to the interface circuit input is around 0.3 μV/V/rtHz.

The CMOS-MEMS thin-film accelerometers have a resonant frequency of a few kilohertz and a Q factor of 10 or lower. Accordingly, the theoretical thermomechanical Brownian noise floor is around 100 $\mu G/\sqrt{Hz}$. However, the noise floors of most of the CMOS-MEMS fabricated accelerometers are around 1 $mG/\sqrt{Hz}$, indicating the dominance of electrical noise. Major electrical noise sources in CMOS-MEMS process includes MOSFET thermal noise, MOSFET flicker (1/f) noise, noise from biasing devices, and noises coupled from substrate and air. As the flicker noise corner is between 100 kHz to over 1 MHz, modulating the input signal at MHz frequencies and providing 80 dB gain at modulation frequency greatly reduces the flicker noise. This also minimizes the noise from biasing devices because the large resistance of biasing devices, together with input capacitance, form a low-pass filter (f_c < 100 Hz) for noise. The acceleration noise contributed by input MOSFET thermal noise is given by the following equation:

$$\bar{a}_n \propto \frac{2C_s + C_p + \frac{2}{3}C_{ox}WL + (2+A)C_{ox}WL_{ov}}{2C_s\sqrt[4]{W/L}},$$

where C_s is sensing capacitance, C_p is parasitic capacitance, W and L are the width and length of MOSFET channel, C_{ox} is gate-oxide capacitance, and A is the gain of input stage. With relatively low parasitic capacitance in CMOS-MEMS, by properly sizing the input MOSFET and using a low gain (A = 3) input stage, the minimum noise floor given by this equation is 3 $\mu G/\sqrt{Hz}$.

Therefore, the thermal circuit noise can be made much smaller than the Brownian noise.

However, it is found that the flicker noise of the digital CMOS used in this project is larger than thermal noise for frequencies less than 1 MHz. This flicker noise limits the resolution of the inertial sensors.

3.4 Integrated MEMS Design Tools

The overall goal of the design tool tasks is to verify that integrated MEMS designs will work after the first fabrication run, requiring no iterations. Designs are developed using the Carnegie Mellon NODAS design methodology as implemented within the Cadence Design Environment. Inertial devices are defined in a MEMS schematic and simulated. The devices are then layed out using semi-automated techniques. Mechanical and electrical connections are verified through extraction. Capacitive parasitics are extracted in both in the MEMS and electrical areas of the design. These parasitics are combined into a final schematic and simulated for final verification of design functionality.

The design flow outlined above leverages the past achievements of the Carnegie Mellon "Foundations of MEMS Synthesis" project funded through the DARPA Composite CAD program. The schematic design methodology and microresonator layout synthesis algorithms were developed in this prior effort. Refined behavioral models for schematic simulation, extraction algorithms for design verification, algorithms for accelerometer and gyroscope layout synthesis, and fault modeling algorithms for MEMS are developed as part of the IMIMU effort. These CAD research tasks support the overall IMIMU design.

4. Results, Discussion

4.1 Processing of inertial MEMS structures in foundry CMOS

During this project we followed two primary thrusts in CMOS micromachining process development using foundry CMOS to enable integration of arrays of inertial sensor components. Our initial focus was on robust processing of thin-film surface-micromachined CMOS-MEMS structures. The integration of bulk silicon processing with foundry CMOS was pursued for enhanced IMU performance.

4.1.1 Thin-film CMOS micromachining

We characterized the existing two-step post-CMOS micromachining process [1][3] and optimized it by inserting the deep reactive-ion-etching for silicon release. The first step is the dielectric etch, for structural sidewall definition. The second step is the silicon etch for structure release. We have primarily used the Hewlett-Packard 0.5-micron n-well CMOS in die form from the MOSIS fabrication service with recent experiments using the AMS 0.5-micron n-well CMOS (as part of the DARPA/MTO MEMS sponsored "Application Specific Integrated MEMS Process Service").

Dielectric Etch. The first step involved a study of reactive-ion etching for definition of the microstructural sidewalls in the CMOS dielectric layers using our Plasma-Therm 790 etcher. A Box-Behnken factorial experiment was used to analyze the effects of pressure, power and gas flow ratio. Through our collaboration with the Jet Propulsion Laboratory, we determined that for high power and low pressure settings, the RIE isotropically attacks the refractory metal layer present on either side of the aluminum metallization layers. This etch causes electrical vias to become open circuits after the microstructural etch. High pressure produces unacceptable polymerization. Low power levels have very low etch rates (up to 9 hours to etch the structures). Suitable equipment settings have been determined that provide relatively high etch rate, straight sidewalls, no polymerization in the field and high manufacturing yield of electrical vias. The process settings are gas flows of 22.5 sccm CHF_3 and 16.0 sccm O_2, pressure of 125 mTorr, and power of 105 W. The etch rate is 424 Å/min over 48 dice in two runs with a standard deviation of ±6%. More detailed information about the process development is available from [25].

Anisotropic Si etch. Previous to this project, the post-CMOS processing steps involved a SiO_2 anisotropic etch to define the structural sidewalls and a Si etch to release the structure, all performed using a single-step parallel-plate plasma-etch-based process. In this project, we focused on inserting an inductively coupled plasma (ICP) etch to improve the quality of the released devices. In an ICP system, the Si release step can be further divided into an initial anisotropic Si etch (the traditional use of MEMS ICP systems), to increase the vertical gap between the microstructures to the substrate, followed by an isotropic Si etch for actual device release. The first step involved demon-

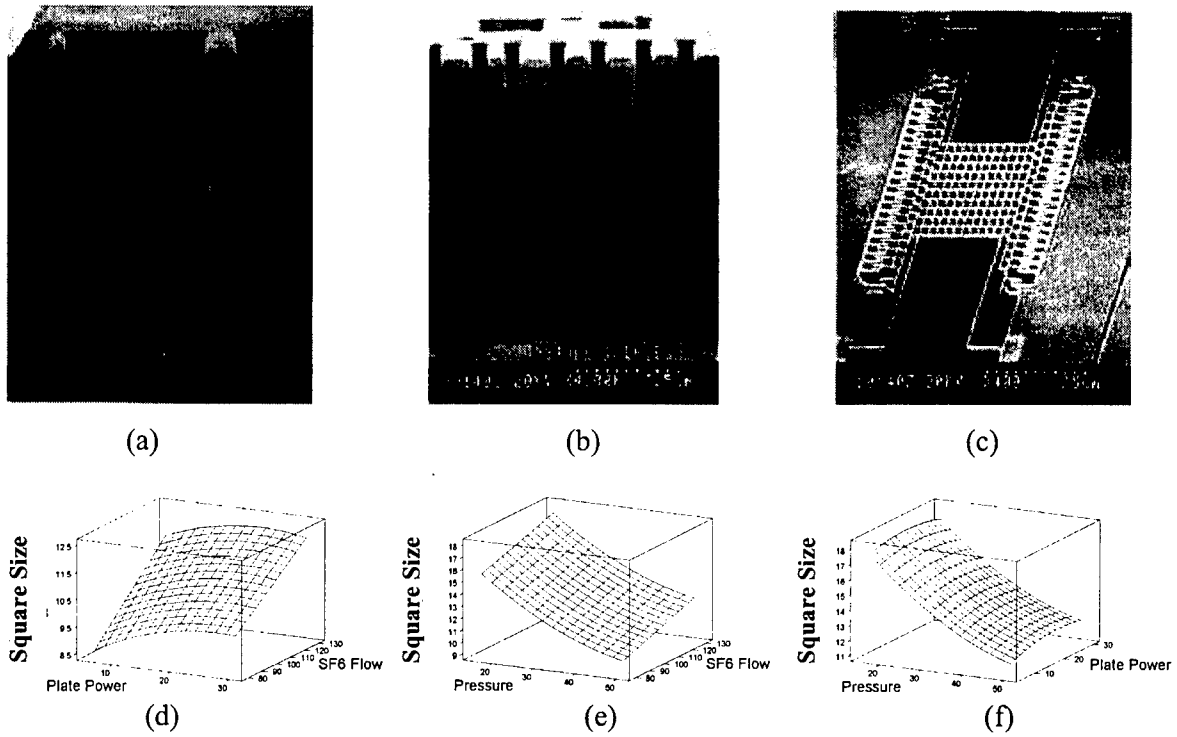


FIGURE 4. DRIE release showing (a) 3 μm spaced structures; (b) 0.9 μm spaced structures; (c) a released crab-leg resonator. Characterization of square size with (d) SF_6 flow and plate power; (e) SF_6 flow and chamber pressure; and (f) Plate power and chamber pressure.

strating that the ICP-based anisotropic silicon etch was functionality in the range of gaps (>0.9 μm) and substrate-substrate spacing (<15 μm) of interest for inertial sensors (Figure 4). These parameters were chosen to allow the placement of electronic circuits to about 15~20μm from the metal mask edge defining the protective region. A joint characterization study with MCNC/Cronos (on subcontract from this project) was initiated as a screening step as there was little data regarding the anisotropic Si etch from an ICP system. Figure 4(d), (e) and (f), shows that squares spaced with a pitch of 5x the square size are undercut. Additionally, a faster lateral etch can be obtained by lowering the pressure and increasing the SF_6 flow rate, whereas the etch rate is insensitive to the plate power.

Isotropic Si etch. The final step in the process sequence involves an isotropic silicon etch to release the microstructure. A Box-Behnken factorial experiment was used to characterize the isotropic Si etch process in an STS ICP system with 4" wafers including key mask features used in CMOS-MEMS structures. The effects of varying three major processing parameters: process pressure, platen power and SF_6 flow were measured. As an example of the success of the Si etch process, a released three-fold symmetric gyroscope [4], with the mechanical structure suspended about 100 μm above the silicon substrate using long metal-dielectric composite beams (200 μm by 1.8 μm) is shown in Figure 5. The long beams are not delaminated and have not lost critical dimension after the long etch (both crucial problems with the previous process). Etch lag effects can be seen on the silicon under the proof mass. This release process will be used in the fabrication of future IMIMU devices.

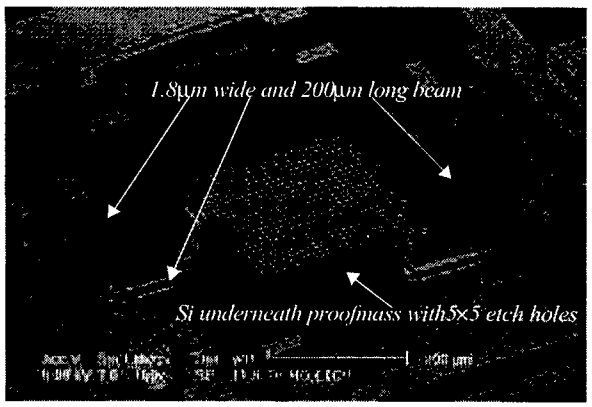


FIGURE 5. Demonstration of deep silicon etch combined with silicon isotropic etch.

The result of these efforts has been a more robust three-step post-CMOS micromachining process. As shown in Figure 6, the process flow starts with an anisotropic parallel-plate plasma etch of the CMOS dielectric stack, then an anisotropic silicon etch and finally an isotropic deep silicon etch. The two silicon etch steps decouple the vertical and lateral etches for enhanced reliability and yield of post-CMOS micromachining.

Curl Minimization. Thin-film CMOS micromachining has many advantages, but micromechanical designs are constrained because of out-of-plane curling of the composite structural layer [6][9]. Vertical curling of post-CMOS micromachined structures occurs due to the difference in residual stresses of each of the layers in the structure. The field oxide layer in the structure has the largest residual stress, as shown by the two failure test structures in Figure 7. The structure in Figure 7(a) includes field oxide while the structure in Figure 7(b) does not include field oxide (controlled by the choice of mask layers used during CMOS processing). Lateral curl also occurs in CMOS micro-

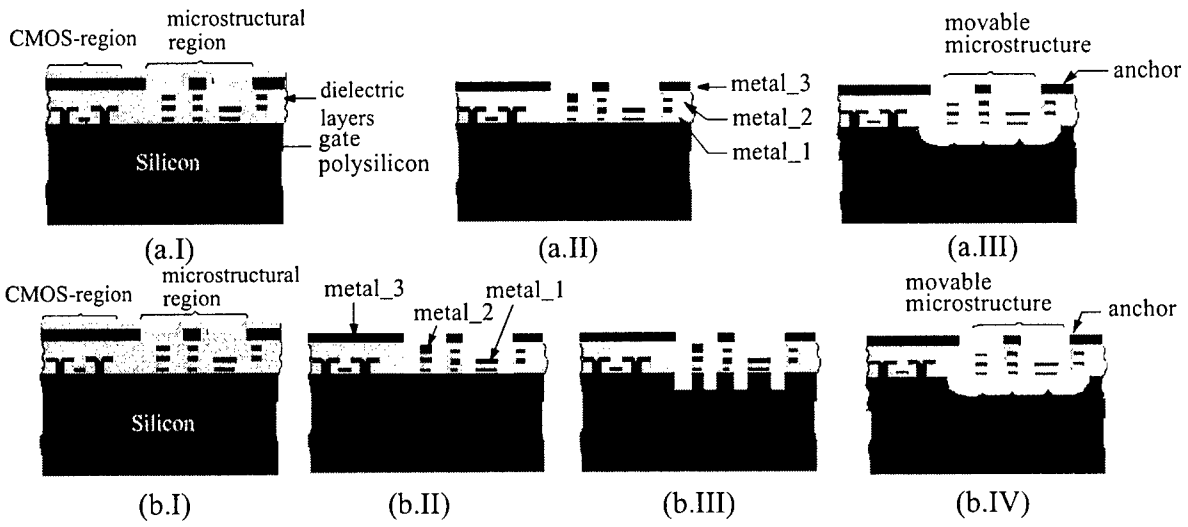


FIGURE 6. Process flow comparing the (a) original anisotropic and (b) isotropic silicon etch to release thin film CMOS microstructures with minimum undercut.

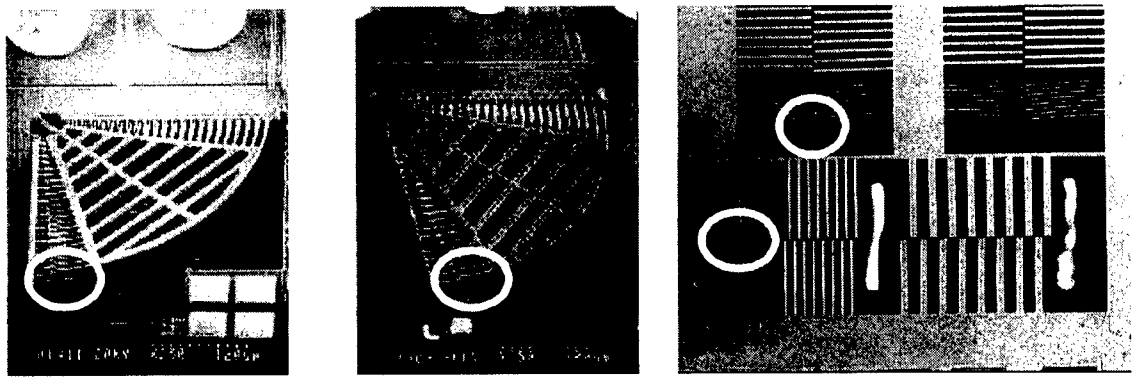
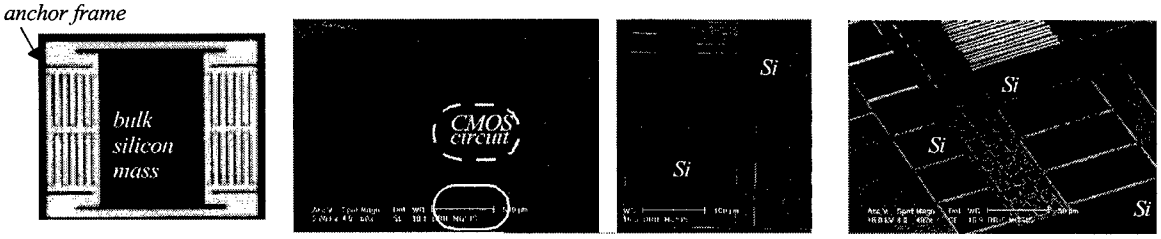


FIGURE 7. Failure testing structure with (a) and without (b) field oxide under the bottom of the structure. (c) Cantilever beam test suite showing lateral curl of narrow beams arising from layer misalignment.

structures and is caused by misalignment or stress gradient directions, as shown on the right graphic in Figure 7.

4.1.2 DRIE-CMOS micromachining

An alternate approach to curl minimization is the use of the mechanical properties of the silicon substrate itself. For the case of the IMU, the bulk silicon provides additional mass and enhanced performance. Two alternative approaches to integrating DRIE-based bulk silicon etching with CMOS have been investigated. The first approach employs the entire wafer thickness while



(a) (b) (c) (d)

FIGURE 8. (a) Backside illuminated top view of the device completely etched through; (b) Top-view, (c) and (d) zoomed-in view of SEM of processed bulk devices completely etched through. Support frame and comb drive fingers are separated from bulk silicon by more than 100 μm, but still much less than device thickness, 500 μm, due to etch lag effects.

the second approach combines front- and back-side etching for dialing in the desired structure thickness.

As inertial sensor proof mass is the primary parameter determining the sensor resolution, we initially developed a through-wafer DRIE-CMOS process, as demonstrated by the bulk accelerometer shown in Figure 8.The through-wafer DRIE-CMOS process combines the standard dielectric etch used in the thin-film CMOS-MEMS structures with a through-wafer isotropic silicon etch to both define the structure sidewalls and release the structure. This type of device has the highest integrable proof-mass possible for MEMS inertial sensors. Additionally, the capacitive sensing circuit can be placed on the proofmass, reducing routing parasitics, as well as device area. The aspect ratio limitations in the DRIE Si etch process (35:1) combined with the large Si wafer thicknesses (500 μm) leads to large comb finger separations, limiting the potential design space.

Therefore, for maximum possible design freedom, we have focused on a DRIE CMOS-MEMS process that combines front- and back-side etching for dialing in the desired structure thickness while still retaining integration with CMOS circuitry [57]. The post-CMOS bulk micromachining process (illustrated in Figure 9), starts from a die fabricated in foundry CMOS. A deep anisotropic backside etch defines a 10 to 100 μm thick silicon membrane (Figure 9(b)) using the ICP process. There is no need for high backside to front-side alignment accuracy. Next the standard CMOS micromachining anisotropic dielectric etch is performed from the front-side (Figure 9(c)). Then in contrast to the thin-film post-processing, we use an anisotropic instead of an isotropic silicon etch for release (Figure 9(d)). The thick silicon layer now underneath the CMOS structures eliminates vertical curling which results in higher design flexibility without losing the advantages

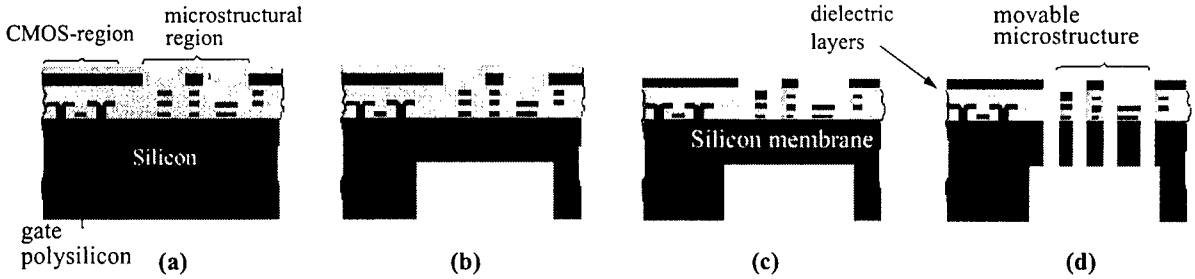


FIGURE 9. (a) The process-flow for DRIE-CMOS micromachining. (a) CMOS chip, (b) CMOS-chip with backside etch, (c) anisotropic dielectric etch, (d) anisotropic silicon etch.

of the standard CMOS micromachining process. Furthermore for CMOS-MEMS based inertial sensors, the proof mass can be significantly increased.

A comb-drive actuator and a beam-resonator were fabricated using this process sequence. A high aspect ratio (20:1) and undetectable vertical curling were achieved (Figure 10(a)). The fabricated devices were actuated electrostatically and characterized using interferometric measurements. Figure 10(b) is a close-up of the comb-drive actuator. The underlying silicon layer has a thickness of 30 μm. The micrograph shows the typical scallops of deep Si etch and a mask undercut of 0.3 μm. The lateral displacement versus the squared applied DC voltage is plotted in Figure 10(c). The plot shows that the spring constant of the serpentine springs is increased by a factor of 4 due to the underlying silicon layer. A resonance peak for the deep etched comb-drive actuator was not observable at atmospheric pressure, most likely due to squeeze damping in the deep trenches. For the released beam-resonator (Figure 10(b)) the measured resonant frequency is 254 kHz, which is in good agreement with the simulation result of 237 kHz. Figure 11(a) shows the depth differences for three trench-widths due to well known microloading of the deep Si etch process. Wider trenches are etched faster; therefore large open areas are etched through to the backside before the narrow gaps. This results in polymer-deposition on the remaining silicon backside during the passivation steps of the deep Si etch (Figure 11(b)). We removed this polymer layer with a zero-bias oxygen plasma clean at the end of the process.

For evaluating the topography of the released structures we employed a Linnik-type Michelson interferometer ($l = 633$ nm). The z-curling due to residual stress and thermal coefficient mismatch of the comb-drive actuator is less than 0.3 μm (limit of our measurement technique) for the

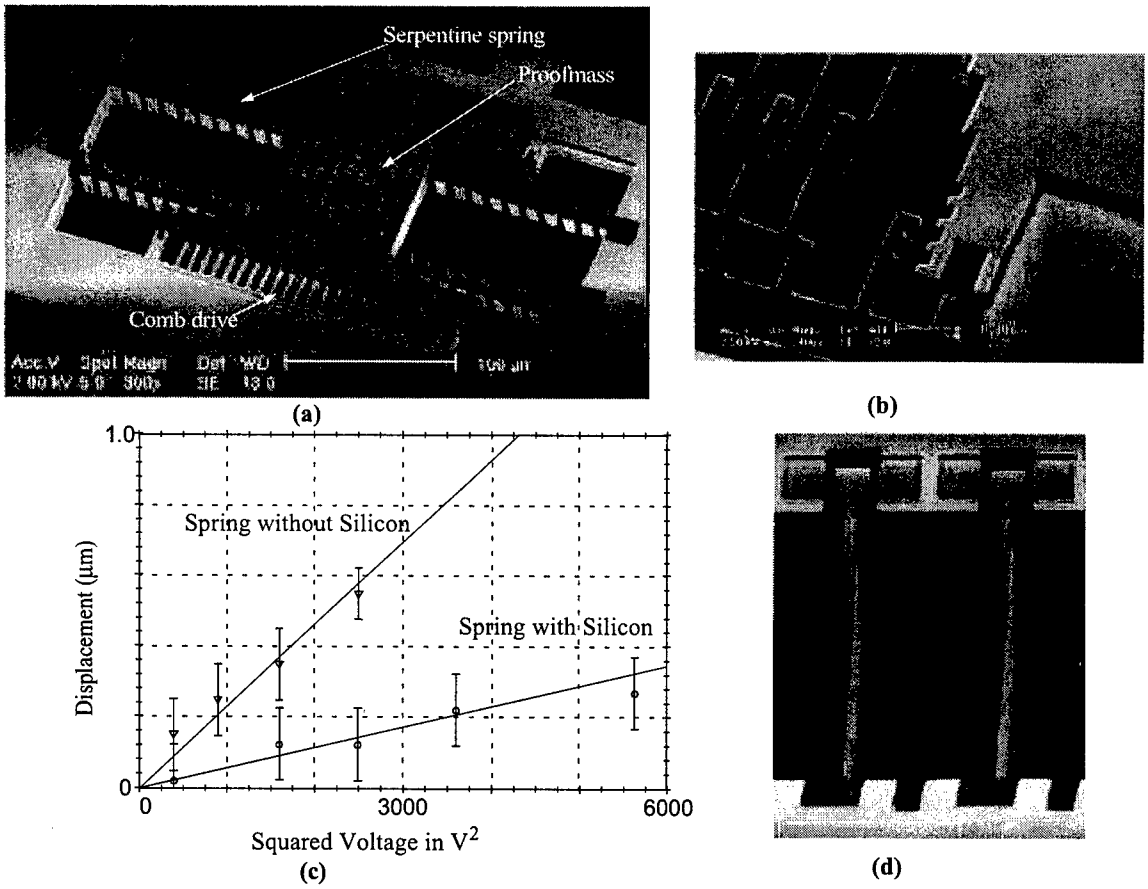


FIGURE 10. SEM-micrograph of the comb-drive actuator released with the new post process; (b) Close-up of one corner of the comb-drive actuator; (c) Measured displacement of comb drive actuators versus squared voltage; and (d) SEM of beam-resonators released with the DRIE-CMOS MEMS process

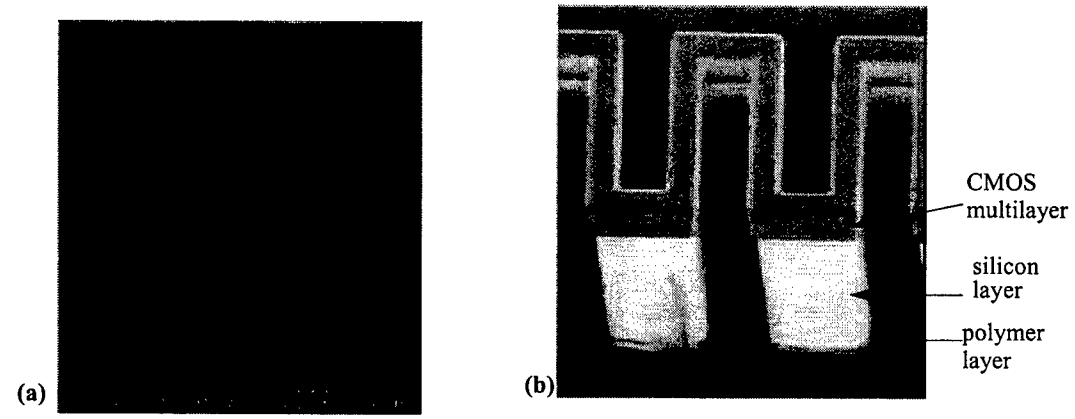


FIGURE 11. (a) Microloading effect of the deep Si etch-process and (b) SEM close-up of the serpentine spring of the comb drive actuator showing the deposited polymer layer underneath the silicon.

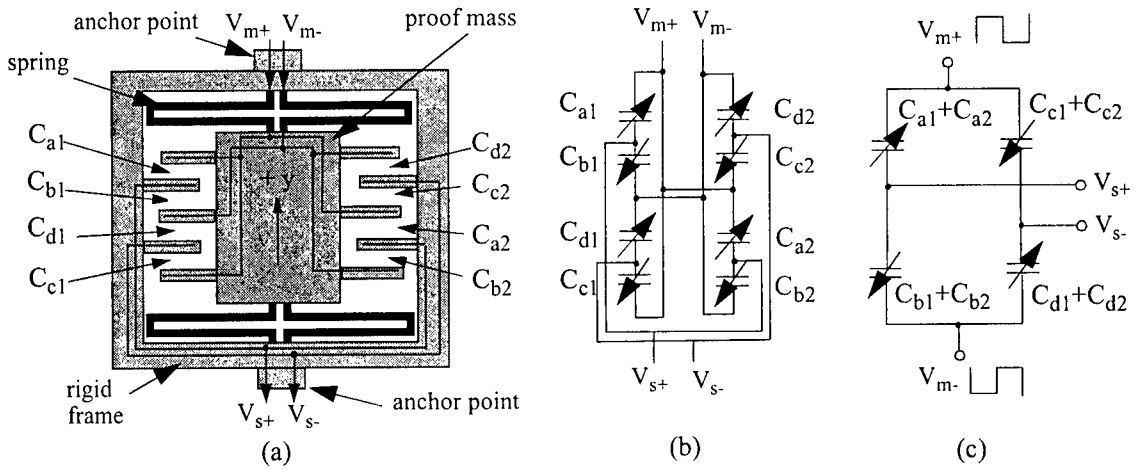


FIGURE 12. (a) A simplified layout view of the post-CMOS micromachined lateral accelerometer topology, illustrating the common-centroid and fully differential features. Eight sense capacitors are formed from the interdigitated comb fingers. (b) Equivalent electrical schematic. (c) Reduced electrical schematic.

new process but larger than 1.2 μm for the standard process.

4.2 Inertial Sensor Designs

Four primary single-axis sensor topologies are designed, fabricated and successfully tested. The results below are for the lateral axis accelerometer, vertical axis accelerometer, lateral axis gyroscope, and vertical axis gyroscope. A second vertical-axis accelerometer design is also designed, fabricated and successfully tested as a testbed for thermal stabilization studies.

4.2.1 Thin-film CMOS-MEMS Lateral Accelerometer

A simplified topology of the lateral accelerometer, shown in Figure 12, is similar to that of Analog Devices' ADXL05 accelerometer, however there are important differences in the wiring and stator mechanics. The proof mass is a micromechanical plate suspended by springs connected at each corner. Perforations in the plate mass are required to successfully undercut the silicon and release the device. The mechanical design is symmetric about the x and y axes, with sensed motion along the y axis. The springs are made from meandered beams, where the number of meanders is variable depending on the desired system spring constant. A typical beam size is 2.1 μm wide, 150 μm long, and 5 μm thick.

The first distinct feature of the accelerometer is that the suspension springs and stator fingers

are connected to a rigid cantilevered frame that is released from the substrate. A critical aspect of the design is the match of the beam layers and widths between the frame and the proof mass and comb fingers. Ideally, the beam layers and width should be constant across any given y-axis cross-section through the device. In practice, there must be some deviation to account for electrical interconnect.

The second distinguishing feature of the accelerometer architecture is the fully differential, common-centroid capacitive sense layout. Each capacitor shown in Figure 12(a) comprises several interdigitated comb fingers. Typical design values are 10 rotor fingers, each 50 μm-long with 1.5 μm-wide gaps. The two modulation signals, V_{m+} and V_{m-}, are routed to the proof mass through the suspension springs. The high-impedance sense nodes, V_{s+} and V_{s-}, are routed through the suspended rigid frame to the interface electronics. This arrangement minimizes parasitic capacitance to the substrate. This fully differential topology approximately doubles the sensitivity of the half-bridge topology with the same value of sensing capacitance. In principle, high CMRR can be achieved at the outputs, although careful attention to matching parasitic capacitance is of paramount importance.

The multiple wiring in the proof mass enables the common-centroid topology, which minimizes offset to manufacturing variation. Sensing fingers are split into four groups of differential capacitor pairs. The upper-left group and lower-right group are connected to form one half of capacitor-bridge, and the upper-right group and lower-left group to form the other half. Displacement along the y-axis will cause capacitors to change as shown in Figure 12, resulting in a differential output. In-plane cross-axis translation and rotation are rejected by the common-centroid differential layout. Out-of-plane translation affects sensitivity, which must be compensated at the system level.

An SEM of the first-generation symmetric accelerometer design is shown in Figure 13(a), Displacement of the U-spring mounted mass is sensed with a transverse comb-drive. A second-generation design, shown in Figure 13(b), incorporates a common-centroid connection arrangement to the comb sense capacitors in order to cancel manufacturing variations across the die. The device had an accelerometer sensitivity is 30 mV/g/V (amplified on chip), noise floor is 0.5 mg/$\sqrt{\text{Hz}}$, and

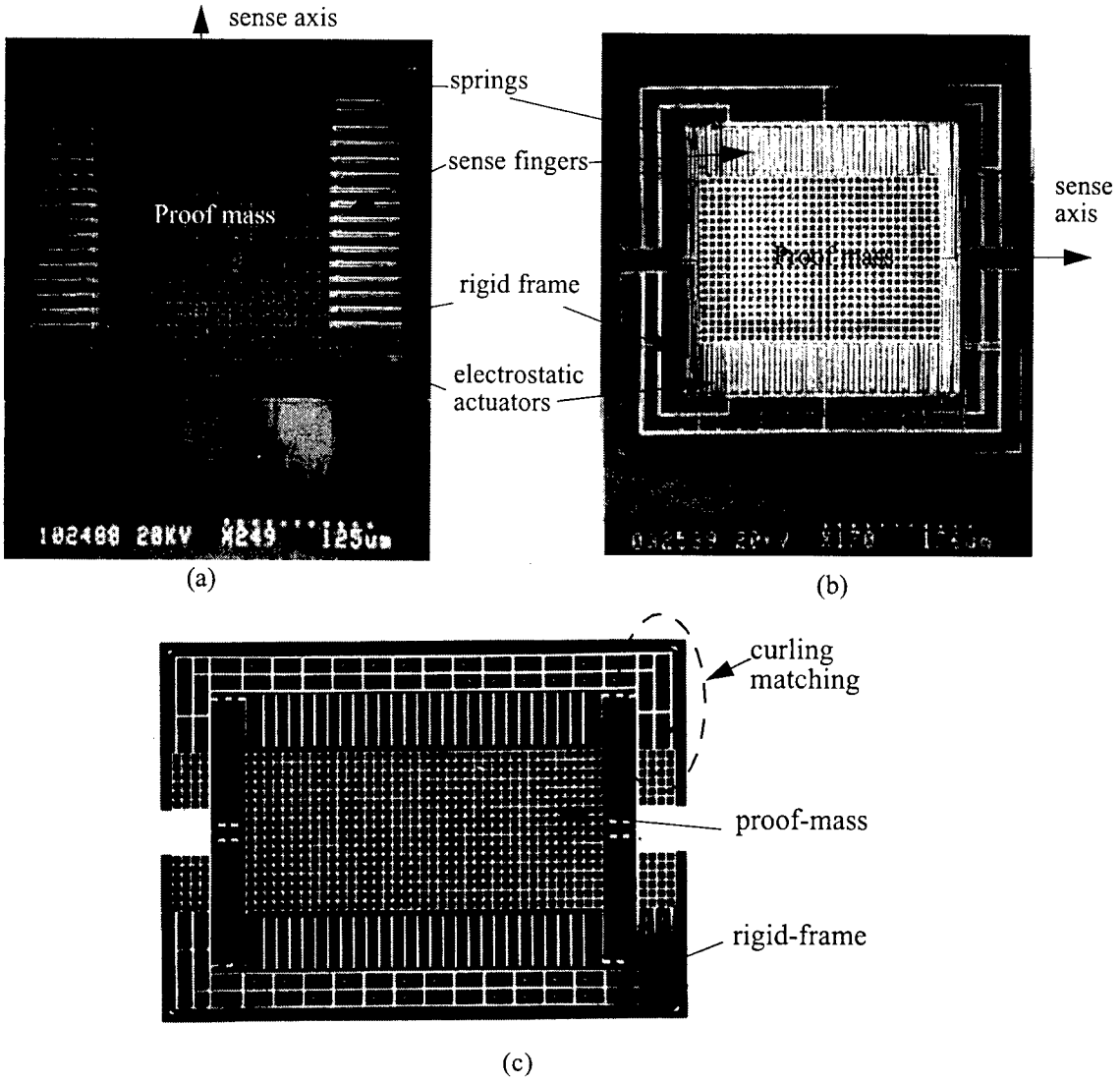


FIGURE 13. (a) SEM of the first-generation symmetric lateral accelerometer, (b) SEM of the second-generation common-centroid lateral accelerometer, (c) SEM of 3rd-generation common-centroid lateral accelerometer.

linear response range is -3.5 g to +3.5 g [28]. A linear offset drift with time was observed of about 0.2 mV/min/V (lateral curl in the narrow spring beams result in mechanical contact of the spring suspension, and believed to cause the observed drift).

The 3rd-generation common-centroid lateral accelerometer design (shown in Figure 13(c)) uses wider spring beams and wider gaps to prevent mechanical contact. Additionally, the rigid frame on which the stator fingers are attached is designed to be axi-symmetrical to the suspension/

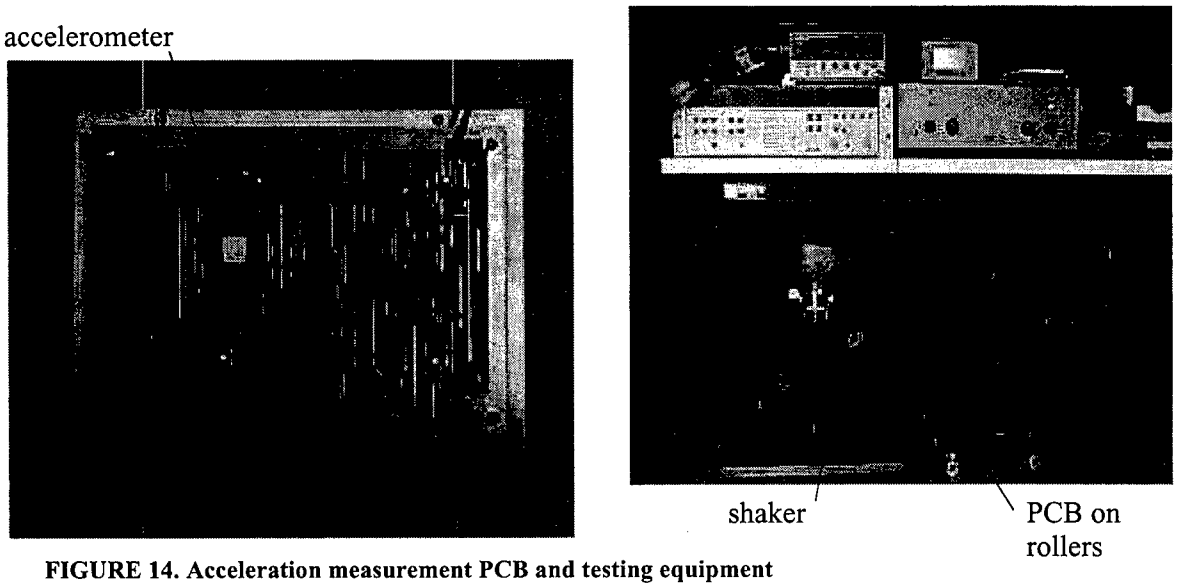


FIGURE 14. Acceleration measurement PCB and testing equipment

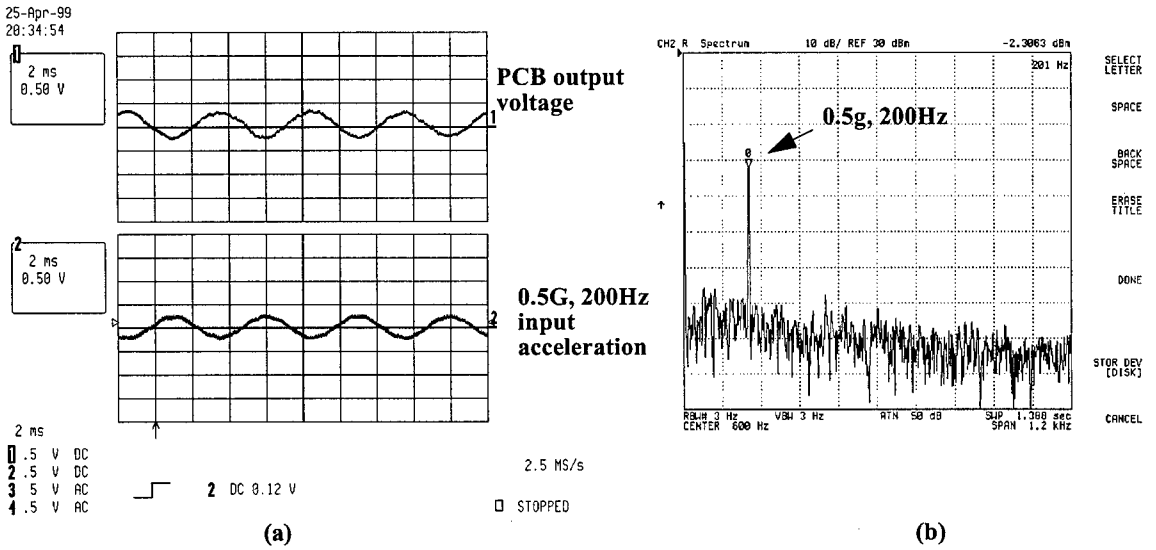


FIGURE 15. (a) Accelerometer output voltage and input acceleration. (b) Output voltage spectrum.

mass structure on which the rotor fingers are attached to for close curl matching. The measurement shows that the vertical curvatures of the outer rigid frame and inner proof-mass frame are matched to within 1%, and the lateral curling was too small to be measured.

The accelerometer is mounted on a printed circuit board (PCB) containing interface electronics as shown in Figure 14. The complete test-bed that includes a Brüel & Kjær 4808 vibration exciter, a HP4295A spectrum analyzer and a LeCroy 9354L digital oscilloscope. Figure 15(a)

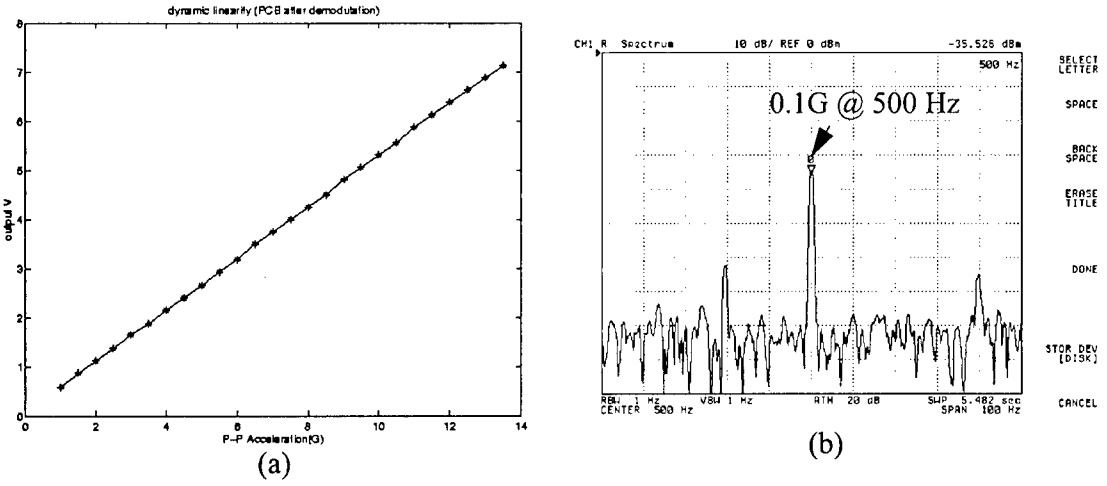


FIGURE 16.
Fourth-generation accelerometer measurements. (a) Dynamic output response. (b) Output signal spectrum.

shows the output voltage when excited by the shaker, with the bottom trace from the reference accelerometer on the shaker table, and the top trace from the PCB-based test-bed. An output sensitivity of 0.53 V/G was obtained. The output voltage spectrum is shown in Figure 15(b). The peak is due to the response of a 0.5 G input, and the noise floor is about 10 mG/$\sqrt{\text{Hz}}$. The linearity characteristics of the accelerometer, shown in Figure 16(a) is limited by the shaker table power. Multiple crash tests indicated that the device can sense up to at least a 30 G acceleration. The device has operated in a robust and repeatable fashion throughout these tests.

A fourth-generation design with minor layout modifications to compensate for lateral curl, and including an integrated version of the readout circuitry was designed, fabricated, released, and tested. The test PCB for this integration is about a tenth of the size of the PCB supporting the third-generation device. The output signal spectrum is shown in Figure 16(b). The peak is due to the response of 0.1 G acceleration. As can be seen, the noise floor is about 1 mG/$\sqrt{\text{Hz}}$ [48].

4.2.2 Thin-film CMOS-MEMS Vertical Accelerometer

Two different z-axis accelerometer architectures were explored during this project. In this section we describe one of these sidewall capacitance accelerometer designs. The second z-axis

Table 1: Summary of 4th-generation lateral accelerometer performance

	Conditions	Value
Measurement range	shaker	-5 G ~ +5 G
Sensitivity	gravity calibration	0.19 V/G
Noise performance	20 °C	1 mG/$\sqrt{\text{Hz}}$
Bandwidth	with test PCB (7 cm by 10 cm)	600 Hz

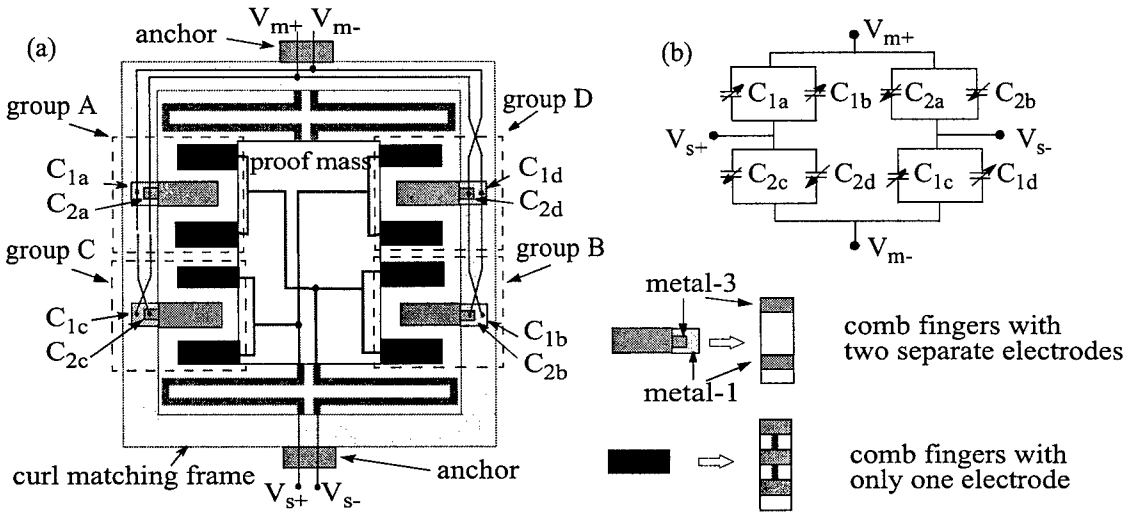


FIGURE 17. Topology design and wiring configuration of the *z*-axis accelerometer. (a) Schematic of the top view of the layout with a common-centroid configuration. (b) Equivalent full-bridge differential capacitive interface.

accelerometer, described in Section 4.4, is designed for demonstration of temperature control to overcome the temperature-dependent curl inherent in thin-film CMOS-MEMS devices.

Figure 17(a) shows the topology of a z-axis accelerometer consisting of a central proof mass, two symmetric z-spring beams and two sets of comb fingers. The vertical gap between the thin-film structures and the bottom silicon surface in thin-film CMOS-MEMS devices is impractical to use for detection of the z displacement. The gap to substrate is made relatively large (about 20-30 μm), so the capacitance is small. The substrate must be connected to the most negative power

supply, and so makes a poor choice as an electrode for capacitive detection. Instead the thin-film vertical accelerometers take advantage of the multiple conductors within the CMOS dielectric stack to form a sidewall capacitance based sensor, as shown in Figure 17. The device uses the same basic topology as the lateral accelerometer, with a released rigid frame is used to ensure sidewall alignment between the rotor and stator fingers.

The CMOS-MEMS process provides beams with different thicknesses by choosing different interconnect metal layers as the etching mask. Typically, beams with metal-1, metal-2, metal-3 on top are 1.8 μm, 3.5 μm, 5.0 μm thick, respectively. Suspensions can be designed very flexible in the vertical direction by using the thinner beams while being stiff in the lateral directions by using relatively wide beams. Therefore, a vertically compliant spring (z-spring) is realized by using wide, thin beams with metal-1 on top, while a lateral-compliant spring is realized by using narrow, thick beams with metal-3 on top. For example, assuming a z-spring has a beam width of 10 μm and thickness of 1.8 μm, the z-axis stiffness will be about 30 times smaller than the x-stiffness.

The multi-conductor layer structures make it possible to construct multiple capacitors between comb fingers. For combs with three metal layers, there are 22 different electrode-pair configurations that provide vertical electrostatic actuation and capacitive displacement sensing. The cross-sections of the lateral and vertical configurations of comb fingers are shown in Figure 3(a) and (c), respectively. The comb fingers have two or three metal layers and are located about 25 μm above the substrate, which leaves ample room for vertical motion. This large gap is also an advantage for capacitive comb-finger sensing because the parasitic capacitance to the substrate is greatly reduced. As shown in Figure 3(a), if the three metal layers on the stators are electrically connected, as are the corresponding metal layers in the rotor, the CMOS comb drive functions equivalently to a lateral-axis polysilicon comb drive. If all three metal layers in the rotor are electrically connected while the metal-1 and metal-3 in the stator are separately connected, two sidewall capacitors, C_1 and C_2, are formed, as shown in Figure 3(c). When a voltage is applied across C_1 or C_2, the rotor will actuate in the z-direction. If the rotor finger moves up or down by an external force (such as acceleration), C_1 and C_2 will change value in opposite directions.

The full-bridge differential capacitive combs on the accelerometer are divided into four groups as shown in Figure 17. All comb fingers have exactly the same cross-section as shown in

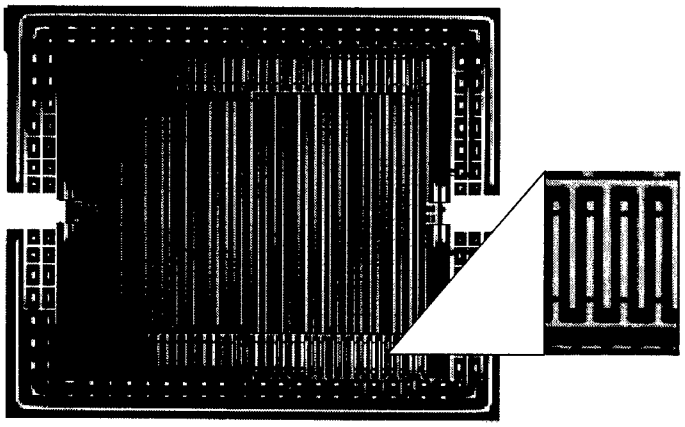
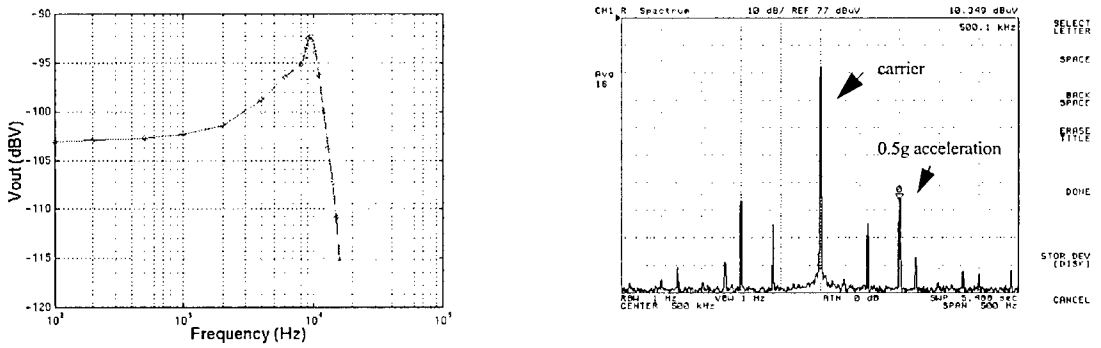


FIGURE 18. A z-axis accelerometer using vertical capacitance sensing with zoom into finger area.

Figure 3(b). In groups A and B, the top metal layer is connected to V_{m+}, and the bottom metal layer to V_{m-}. In groups C and D, the wiring is reversed to obtain a full-bridge differential capacitive interface. Moreover, the four groups constitute a common-centroid configuration which reduces the lateral-axis sensitivity and the influence of process variations.

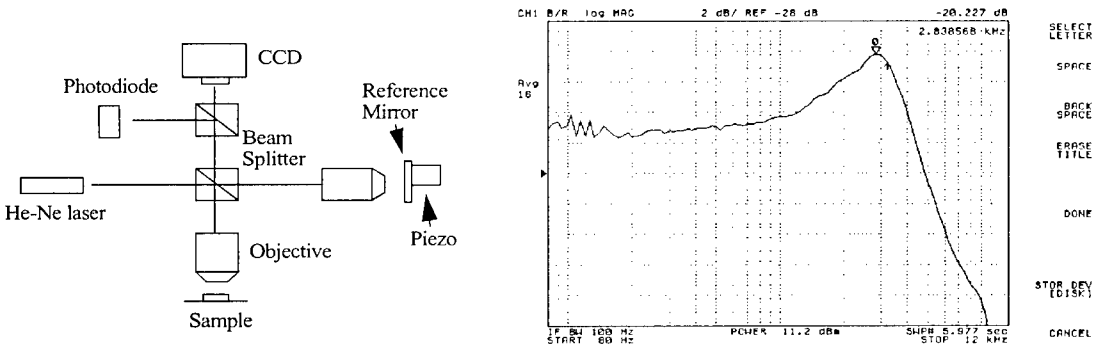
A photograph of the first generation released device (shown in Figure 18) shows that stator and rotor fingers match each other very well vertically (less than 0.5 μm) and have less than 0.1 μm lateral offset. The frequency response of the accelerometer (Figure 19(a)) indicates a resonance frequency of 9.2 kHz and a Q factor is about 3. The Q factor is quite low because of the appreciable squeeze damping of the proof mass suspended about 15 μm above the substrate. The spectrum of the output signal when a 100 Hz, 0.5 G acceleration (generated by a shaker table) is applied is shown in Figure 19(b). The modulation frequency is 500 kHz. The noise floor of the accelerometer is about 20 mG/$\sqrt{\text{Hz}}$. This noise is dominated by circuit noise, and is not as low as the lateral accelerometer. The difference in noise performance is believed to be due to the different interface circuits, modulation frequencies, and the degree of integration of the mixing and output circuitry.

The accelerometer's motion in the z-direction was measured using the optical interferometry setup shown in Figure 20(a). A photodiode is used to detect the shift of interference fringes due to the z-motion proof mass, and a conventional piezoelectric actuator is used to search for the most sensitive working point. A 632 nm He-Ne laser is used as the light source. Figure 20(b) shows the z-displacement versus the frequency of the external applied voltage. The dominant mode with a reso-



(a) (b)

FIGURE 19. Test results from the sidewall capacitance based z-axis accelerometer with (a) the frequency response, and (b) the spectrum of the output signal (modulated).

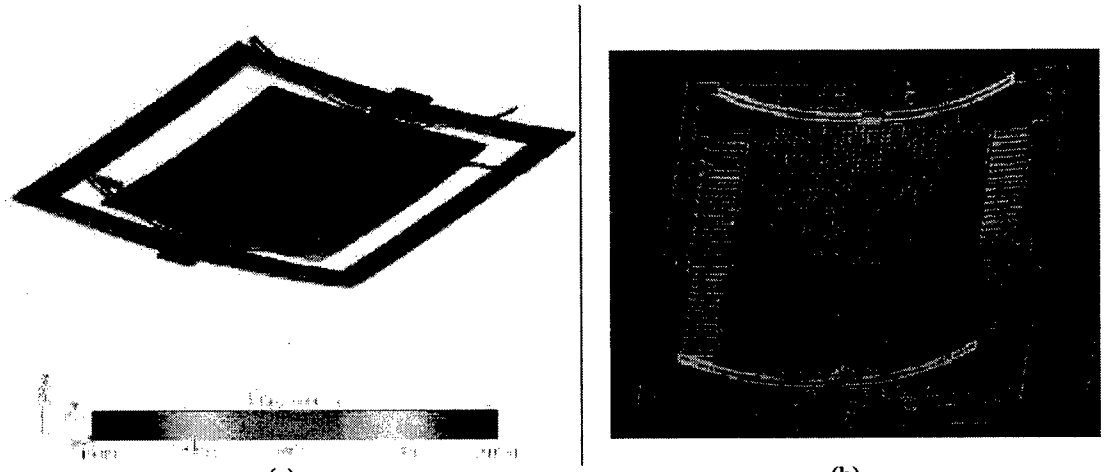


(a) (b)

FIGURE 20. (a) Optical interferometer set-up and (b) z-displacement at the proof mass edge versus the frequency of external drive voltage.

nant frequency of 2.9 kHz represents the rotation along the x-axis. A smaller peak at 9 kHz corresponds to the translational z mode, which is in agreement with the self-test result (shown in Figure 19(a)). The unique side-wall capacitance based sensing configuration makes the accelerometer insensitive to the twisting motion along the x-axis, thus the dominant Figure 20(b) peak is not seen in Figure 19(a).

Memcad 4.5 was used to simulate the behavior of the z-axis accelerometer. Figure 21(a) shows the predicted shape of the microstructure after release, and Figure 21(b) is a SEM photo of an actual released accelerometer. The maximum vertical curl at the spring tips is simulated to be



(a) (b)

FIGURE 21. Shape of z-axis accelerometer after release (a) curl simulation in MEMCAD and (b) SEM photo.

Table 2: Simulation and measurement results of z-accelerometer resonant modes

Resonant modes		Memcad simulation (kHz)	Vertical capacitive sensing (kHz)	Optical interferometry (kHz)
Mode 1	θ_Y	3.95	None	2.9
Mode 2	Y	6.57	None	None
Mode 3	Z	10.1	9.3	9.0

60 μm, while the actual measurement value is 50±5 μm. The predicted modes and measured modes are listed in Table 2. From Table 2, we can see that the z-axis accelerometer is insensitive to the first two modes, which actually is one of the advantages of this sensor. Since the optical interferometry can only detect the z-axis motion, the first and third modes, which are the rotation along the y-axis and the pure z-axis motion, respectively, have been measured, while the second (lateral) mode has not been measured (see Figure 20(b)). The vertical motion (mode 3) is our primary concern. The resonant frequency values measured by the z-axis accelerometer electronics and by optical interferometry differ by about 3%. This difference is believed to be due to an electrical softening effect. For the optical interferometry, a 5 V DC offset is applied with a 1 V AC sinusoidal voltage signal, while the z-axis accelerometer's self-test, only 8 V AC sinusoidal signal is applied. There is about 10-30% error for the MEMCAD simulation. This is mainly due to the simplification of the model in

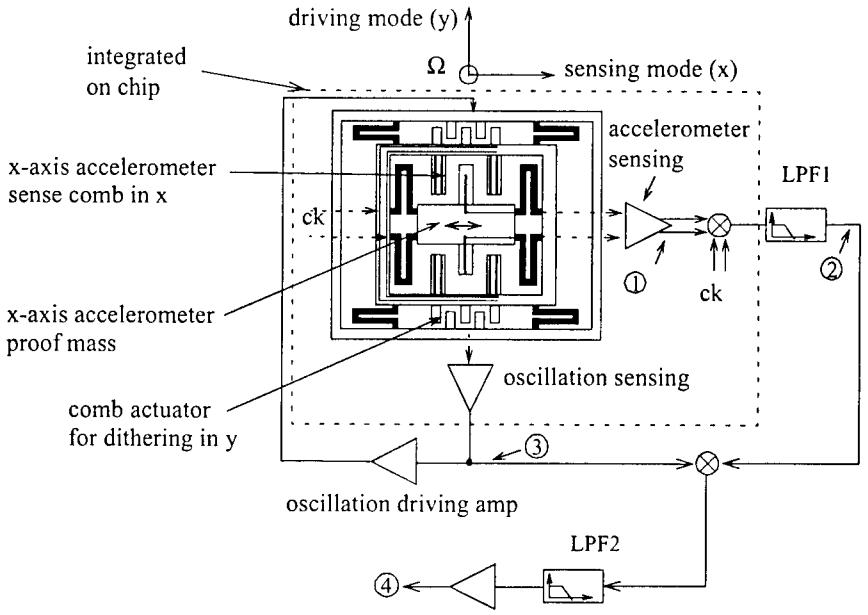


FIGURE 22. Schematic of the vertical-axis gyroscope.

order to reduce the simulation time. The latest generation z-axis accelerometer using this topology has a measured resonant frequency of 9.3 kHz, sensitivity of 0.5 mV/G, cross-sensitivity of 40 dB, noise floor of 6 mG/$\sqrt{\text{Hz}}$ and linear range of ±27 G [47].

4.2.3 Thin-film CMOS-MEMS Vertical Gyroscope

Coriolis acceleration of a structure is proportional to the cross-product of velocity V and the external rotation rate Ω. Vibratory-rate gyroscopes measure rotation rate indirectly by detecting the Coriolis acceleration due to the sinusoidal velocity V of the vibrating structure. The vertical-axis (z-axis) CMOS-MEMS gyroscope is composed of an x-axis accelerometer nested in a movable rigid frame as shown schematically in Figure 22. A comb drive actuates the rigid frame in one lateral direction (y-axis), and the inner accelerometer measures the orthogonal deflection arising from the Coriolis force. The elastically gimbaled structure decouples the Coriolis sense mode from the vibration drive mode, except for manufacturing-induced imbalance.

The sensing buffer and the first stage demodulator are implemented on chip. The oscillation driving amplifier and output low-pass filters and rotational-rate mixer are implemented off-chip. This partitioning of electronics helps focus research on the micromechanical parts of the device and

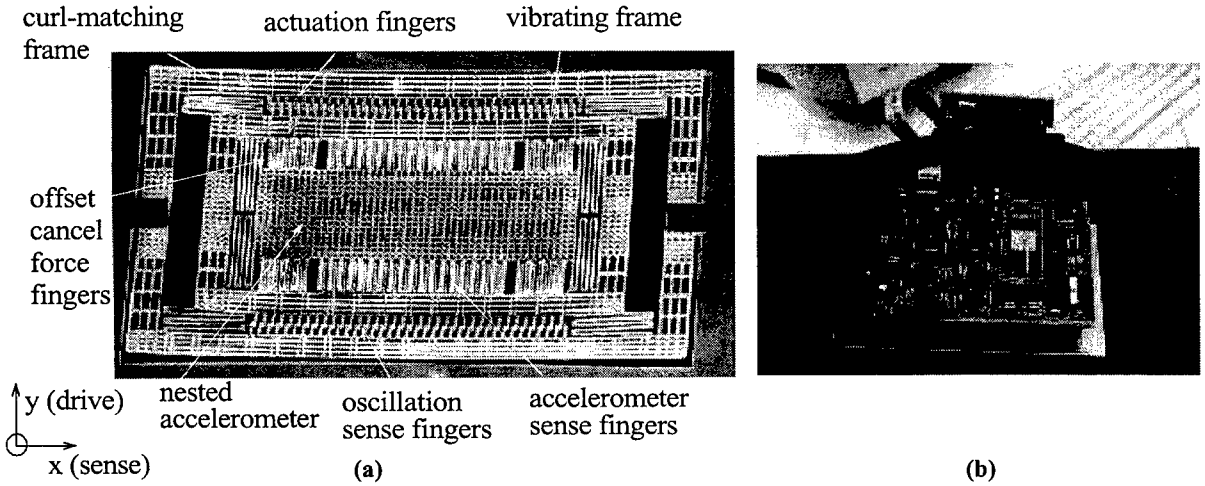


FIGURE 23. (a) SEM of released third-generation gyroscope; (b) rotation table test setup.

on the interface circuit. Ultimately, the complete electronics should be placed on chip for a fully integrated product.

The first-generation gyroscope design highlights limits in the post-CMOS processing of large micromechanical structures. The large gyroscope plate mass curls during release to the point of touching the underlying substrate. This reduces the amount of undercut in the release etch. Most of these structures therefore remain attached to the substrate. The 2nd-generation vertical gyroscope used short suspensions to enable successful release without the problem of plate mass bending to the substrate. The rigid frame is meant to self-align the rotor and stator fingers in the dither combs and the accelerometer combs. However, this 600 μm by 500 μm-sized device suffered from vertical curl mismatch and required significant external circuitry for operation. The curl mismatch arises from the two-dimensional curl of the plates and frames. The alignment technique of using cantilevered frames compensates for only one dimension of the curl. The techniques is adequate for the smaller accelerometers, but breaks down for the larger gyroscope designs.

The third-generation z-axis gyroscope was the first fully functional CMOS-MEMS gyroscope. As with earlier designs, it is composed of the lateral accelerometer nested in a movable rigid frame (shown in Figure 23(a)). A comb drive actuates the rigid frame in one lateral direction, and, when the device is rotated around the z-axis, the inner accelerometer measures the orthogonal

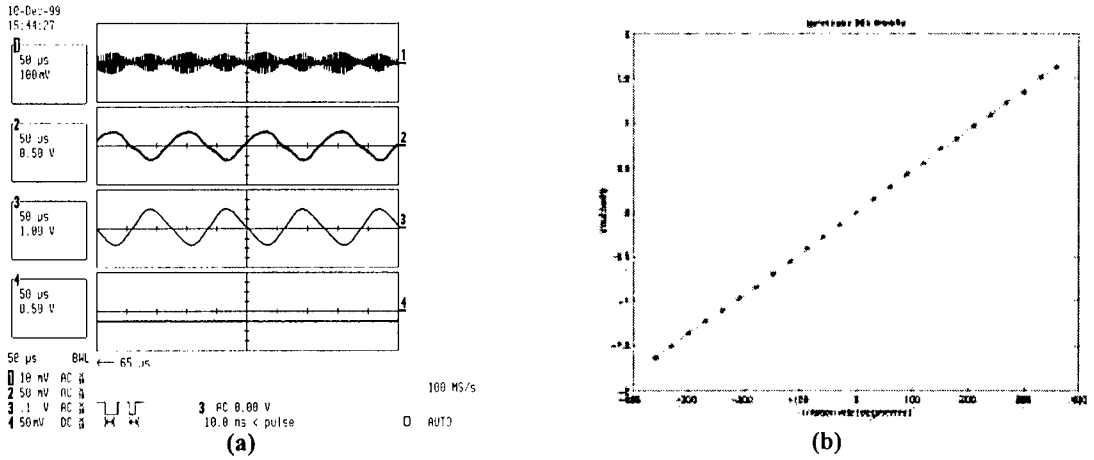


FIGURE 24. (a) Waveform captured at nodes (refer to gyroscope schematic) and (b) DC characteristics showing output vs. rotation rate.

deflection due to the Coriolis force. The elastically gimbaled structure completely decouples the Coriolis sense mode from the vibration drive mode. The benefit of low parasitic capacitance in the CMOS-MEMS process gives the sensor relatively high sensitivity and makes it possible to operate at atmospheric pressure. The measured circuit-input-referred sensitivity is 4.5 mV/°/sec and the noise floor is 0.4 °/sec/$\sqrt{\text{Hz}}$. Measured linearity is within 1% in the range of -360 °/sec to 360 °/ sec. Actual working range is greater, however the experiments are limited by the maximum output of the rotation table. Figure 23(b) shows the gyroscope test setup which includes the gyro and the rotation table. The waveforms of nodes marked in the schematic of Figure 22 are displayed in Figure 24(a), showing output of each stage. The dc characteristic is shown in Figure 24(b).

The fourth-generation gyroscope is shown in Figure 25(a) and (b). Compared to the previous generation, the newly designed structure has better performance in decoupling the two modes and has higher sensitivity. The measured noise floor is 0.03 °/s/$\sqrt{\text{Hz}}$. Measured linearity is within 1% in the range of -360 °/s to 360 °/s [59]. The gyroscope dc characteristics are shown in Figure 26(a). The motions of inner structure and outer frame are measured with the MIT Microvision system (Figure 26). Table 3 summarizes the technical data.

4.2.4 Thin-film CMOS-MEMS Lateral Gyroscope

A lateral-axis microgyroscope requires either vertical actuation with lateral motion sensing

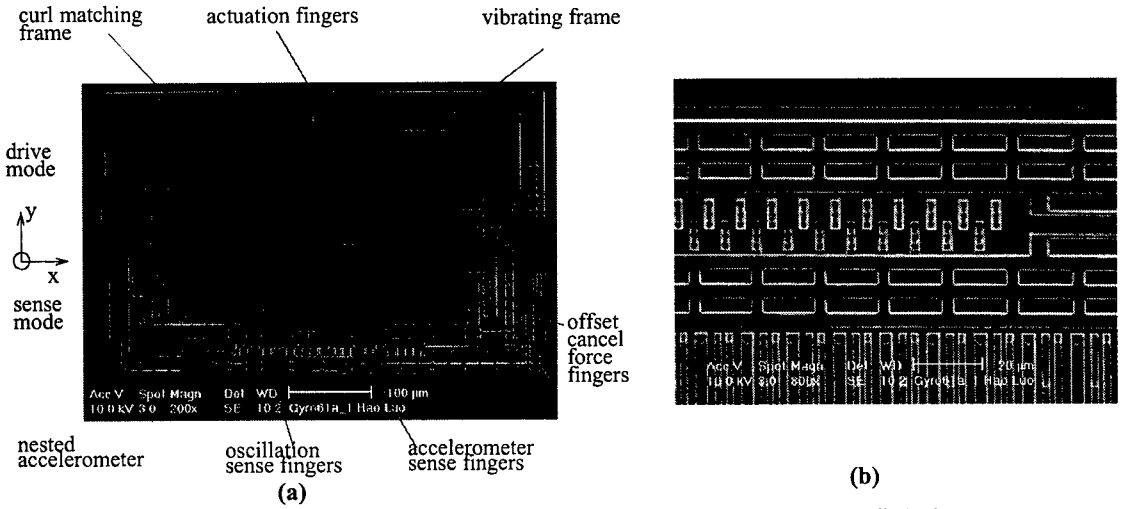


FIGURE 25. Fourth-generation gyroscope. (a) SEM of the device. (b) An amplified view at one corner.

Table 3: Technical data of the fourth-generation gyroscope.

Parameter	Measured result
On-chip circuit power supply voltage	5 V
Vibration drive voltage	DC=24 V, AC=10 V
Working ambient	760 Torr
Driving mode resonant frequency	9.2 kHz
Sensing mode resonant frequency	11 kHz
Sensitivity	2.2 mV/°/sec
Noise (over 20 Hz BW)	0.03°/sec/$\sqrt{\text{Hz}}$
Linearity (-360~360 °/sec)	1%

or lateral actuation with vertical motion sensing. Both of these architectures are explored, however the vertically actuated gyroscope is described here in detail since it is most fully developed. The thin-film CMOS-MEMS lateral gyroscope topology, shown in Figure 27(a), includes three key components: a z-axis comb-drive, a y-axis accelerometer and a z-axis position sensor used for feed-back control of the z-axis actuation. The topology of the lateral-axis gyroscope shown in Figure 27(a) is similar to the vertical-axis gyroscope, however the y-axis accelerometer is dithered verti-cally instead of laterally. The structure is a two-fold, orthogonal spring-mass system where the

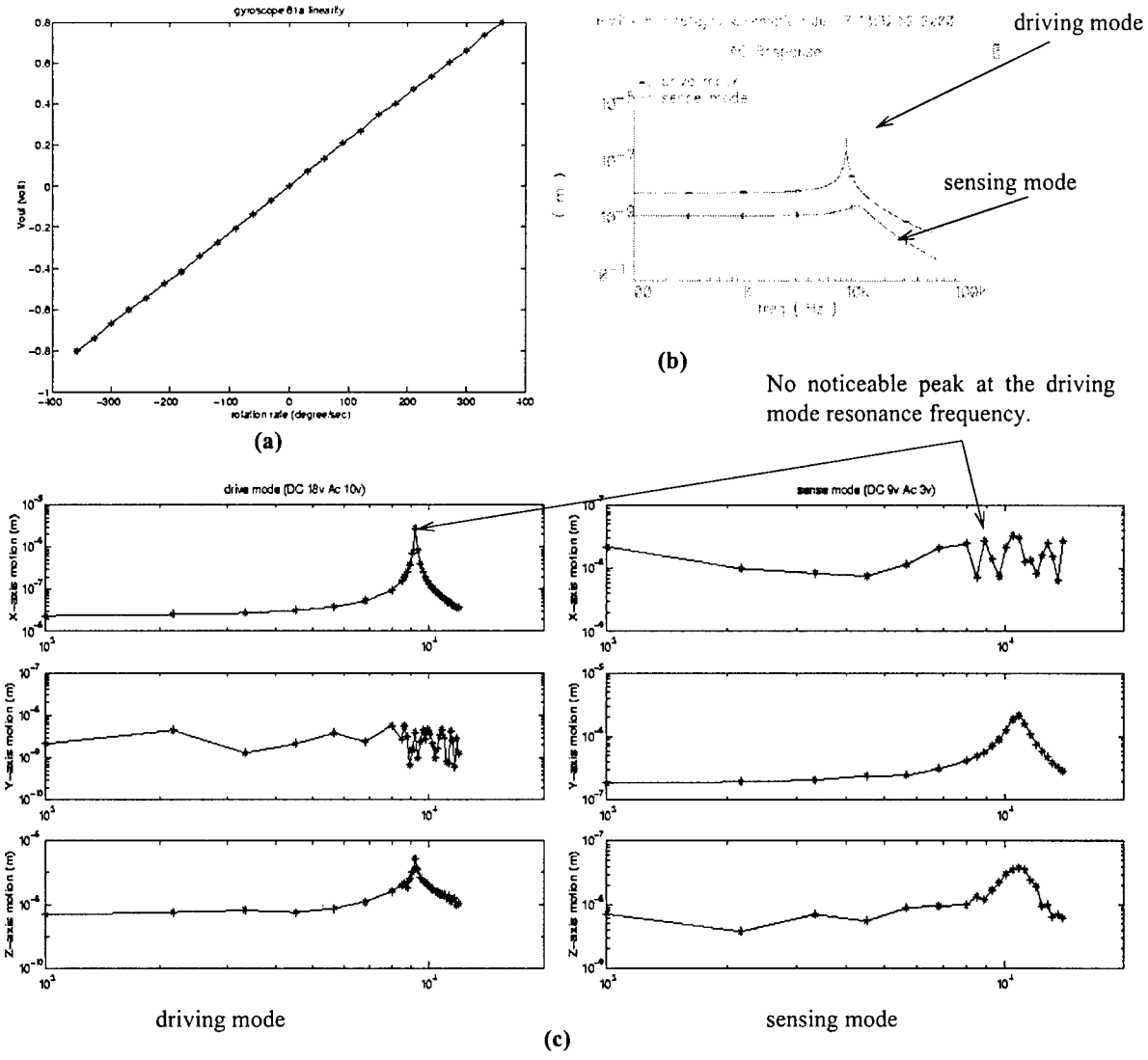


FIGURE 26. (a) Fourth generation gyroscope DC characteristics. (b) Simulated sensing and driving mode motions. (c) Measured motion in the two modes. The absence of a well-defined resonant peak in the x-axis (sensing mode) means the two modes are decoupled.

inner frame together with the proof mass is vibrated in the z-direction by the comb drive, while the induced Coriolis acceleration is sensed by the accelerometer. Thus, the rotation sense axis of this device is along the x-axis.

Thin and wide suspension beams are connected to the outer proof-mass for the z-drive. The z-axis position sensor utilizes the sidewall capacitance divider scheme in Figure 3(c). As with the

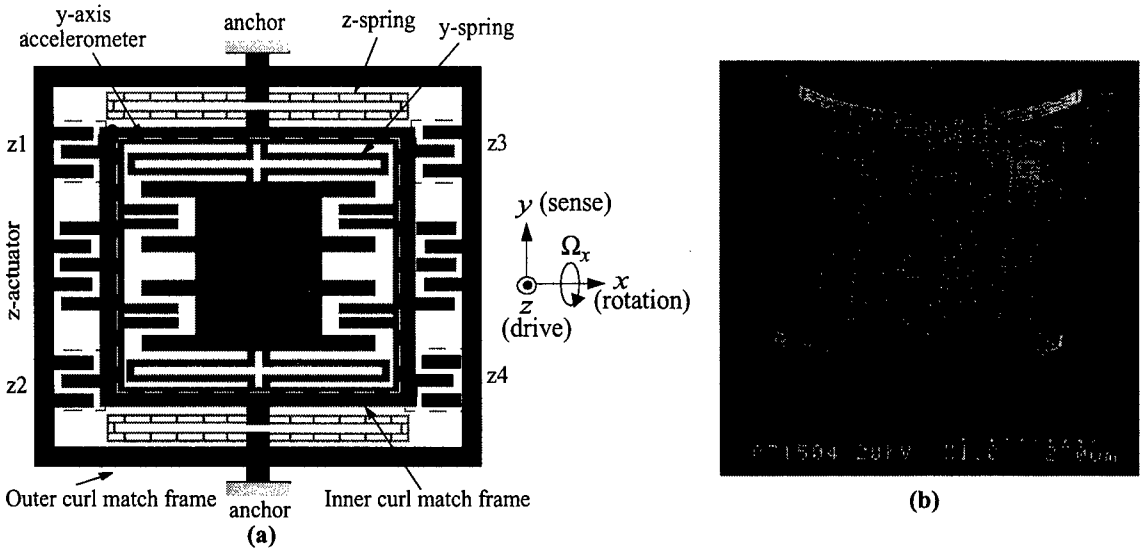


FIGURE 27. (a) Topology of the lateral-axis gyroscope and (b) SEM of a released gyroscope.

lateral accelerometer and vertical gyroscope, the designs incorporate an integrated, fully-differential capacitive interface circuit. A y-axis actuator is included inside the embedded y-axis accelerometer to compensate any off-axis motion coupled directly from the z-axis input excitation. Such coupling arises from manufacturing variations that cause imbalance in the proof mass and springs. As with the stand-alone accelerometer designs, the y-axis accelerometer in the gyroscope has four groups of comb fingers forming a common-centroid configuration to reduce the influence of process variation.

Figure 27(b) shows an SEM of a released first generation lateral gyroscope. The primary test shows that the minimum detectable rotation is about 10 °/sec at atmospheric pressure, and the scale factor is 0.12 mV/°/s. One of the major differences from other surface-micromachined gyroscopes is that the excitation vibration is driven in the z-direction using comb-fingers. The z-axis actuator utilizes the sidewall capacitance configuration shown in Figure 28. The gyroscope is modeled as a nonlinear time-varying system dependent on the external rotation, Ω. The simulation results in Figure 29 show that vibrating at resonance can significantly suppress harmonics.

The z-spring beams, which consist of only metal-1 and polysilicon, curl up about 75 μm at their ends due to the residual stress and thermal coefficient mismatch in the embedded layers inside the beams. However, the vertical misalignment between the stator and rotor fingers is kept between

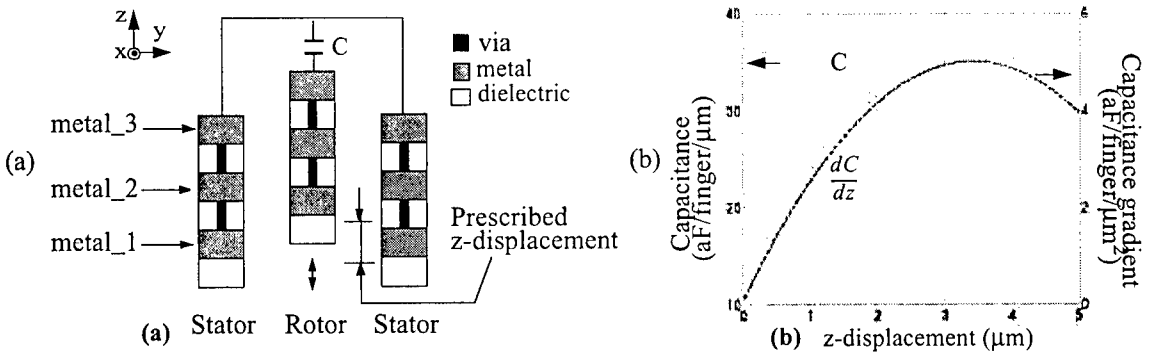


FIGURE 28. Operational principle of z-axis comb-finger actuation: (a) Cross-section of comb-fingers of z-actuator; (b) Field simulation results of capacitance and capacitance gradient versus z-displacement.

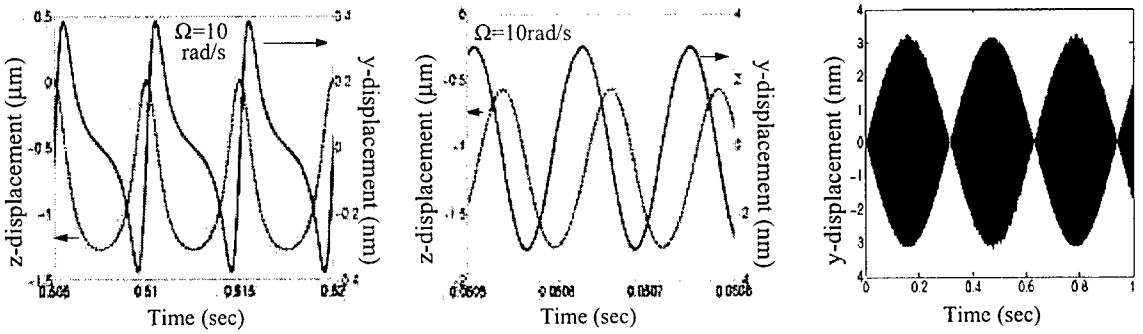


FIGURE 29. Modeling of the system: (a) y- and z-displacements when driven off resonance at 100 Hz and Ω constant; (b) y- and z-displacements when driven at resonance and Ω constant; (c) y-displacement when driven at resonance and Ω=10 sin(10t) where the envelope of the waveform is proportional to Ω(t).

2-3 μm through use of a curl matching frame. The z-springs consist of two parallel narrow beams connected by short trusses to suppress the y-axis vibration. Figure 30 shows the close-up of a z-spring and the stiffness change with respect to the curling, which provides another frequency tuning method. The polysilicon underneath metal_1 functions as a heater. The lateral curling of springs [41] is overcome by a beam designed such that there is no oxide beside any metal layers even when misalignment between metal layers occurs, as shown in Figure 31(a).

The actuator and accelerometer were individually characterized and the measured results are listed in Table 4. The rotation test result by using a turntable is shown in Figure 31(b).

An electrostatic force was applied to the outer frame and displacements at the four marked locations (shown in Figure 27(a)) were measured with the MIT Microvision system. The results are

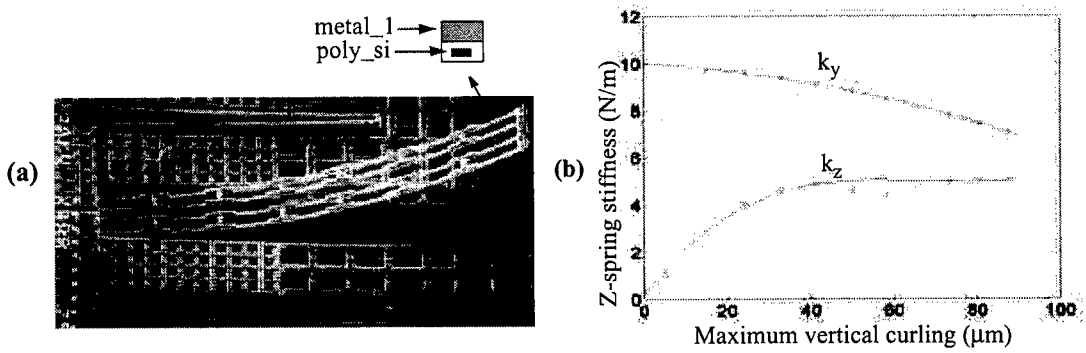


FIGURE 30. Vertical curling: (a) Close-up of a z-spring beam; (b) MEMCAD simulation result of stiffnesses in the y- and z- directions versus the vertical curling at the ends

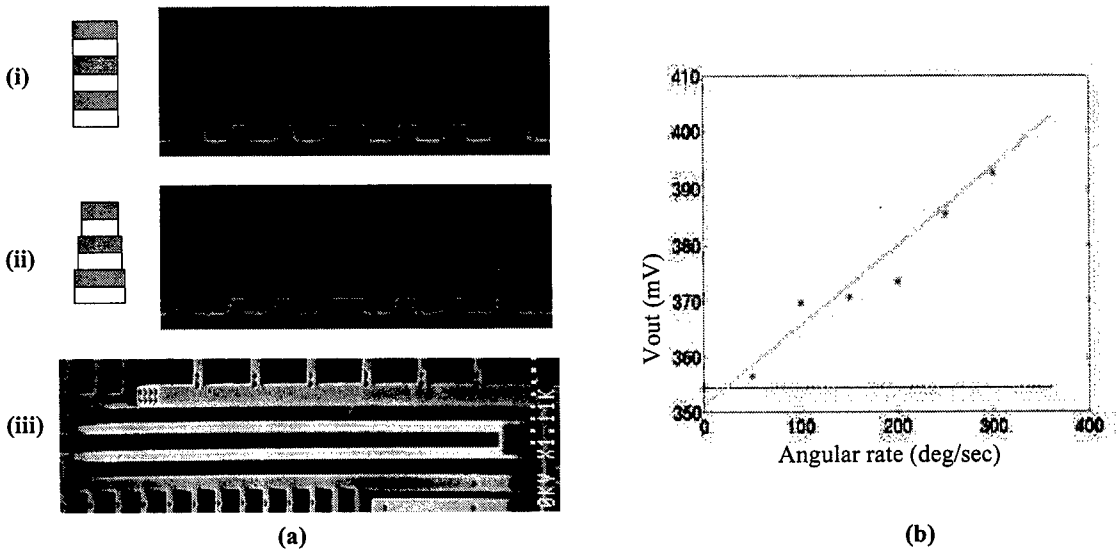


FIGURE 31. (a) Lateral curling elimination: (i) Normal beam in which three metal layers have the same width; (ii) Tapered beam in which lower level metal layers are wider; (iii) The y-axis spring with tapered beam structure demonstrating near perfect lateral alignment; (b) Constant rotational rate measurement. A large DC offset was present. Newly packaged devices are ready for test and better performance is expected.

shown in Figure 32. The embedded y-axis accelerometer detects the Coriolis acceleration which is proportional to the x-axis rotation. The y-accelerometer response is plotted in Figure 33 showing a resolution of $100\ \mu g/\sqrt{Hz}$. The 0.05 G 500 Hz external acceleration was generated by a shaker table.

Shortcomings identified during characterization motivated a re-design that focused on gyroscope non-ideality compensation schemes as shown by the topology and layout in Figure 34. The

Table 4: Parameter design and measurement results from first generation lateral gyroscope

Parameter		Designed	Measured	Parameter		Designed	Measured
Dimension		650μmx800μm	-	Proof mass		1.7 μg	-
Drive mode	Resonant frequency	4.1 kHz	4.2 kHz	Sense mode	Resonant frequency	4.1 kHz	3.9 kHz
	Maximum displacement	1.2 μm @25Vac	1.5 μm @25Vac		Noise floor (mg/rtHz)	0.6	5
	Q-factor	-	3		Q-factor	-	8
Minimum detectable rotation		1.0 deg/s	10 deg/s	Scale factor (mV/deg/sec)		0.4	0.12

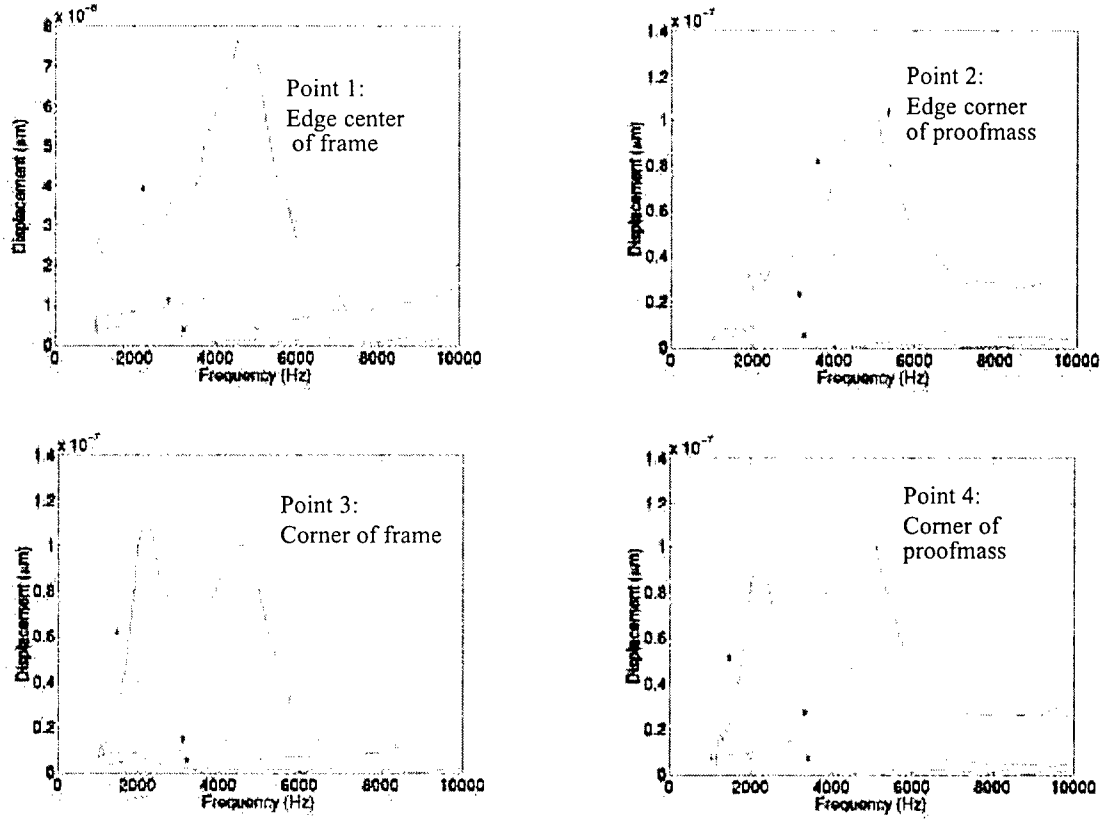


FIGURE 32. Vibration measurement showing the excitation vibration and its induced motion in the sense mode

features of this design include: orthogonal placement of drive spring and sense spring for reduced mode coupling; a four-part individually controllable *z*-drive for compensation of unbalanced driving force; integrated *x*- and *y*- actuators for compensation of off-axis motion; improved curl-match-

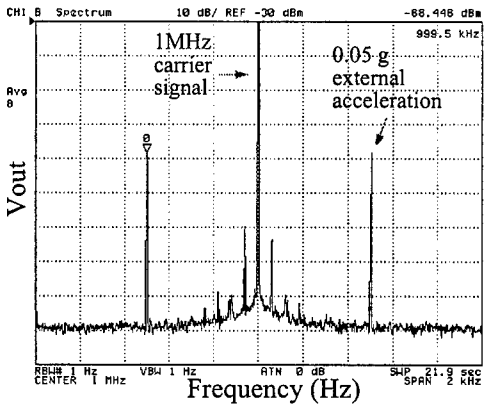


FIGURE 33. A spectrum of the output signal of the y-axis accelerometer responding to an external acceleration.

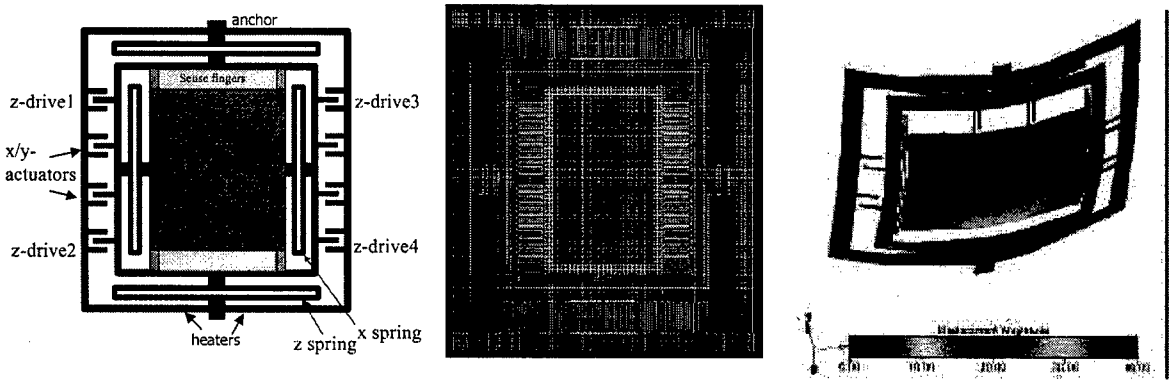


FIGURE 34. (a) Topology of second generation lateral gyroscope with orthogonal sense and drive springs; (b) actual CMOS-MEMS physical design; (c) MEMCAD curl simulation.

ing frame design (MEMCAD simulation using previously characterized thermomechanical curl properties shows that the inner comb fingers match very well but the outer comb fingers have a mismatch of about 10 μm (Figure 34(c)); and integrated polysilicon heaters to control the mismatch of the comb fingers on the outer frame [62]. This new design is not yet tested at the time of this report, however.

4.2.5 DRIE-CMOS Inertial Sensors

The DRIE CMOS-MEMS process incorporates the silicon substrate into the microstructures, and thus accelerometers with larger proof mass can be designed without increasing area. The thick silicon substrate also provides extremely small out-of-plane curl. The lateral DRIE-CMOS accelerometer is based on the thin-film lateral accelerometer design. However, curl matching

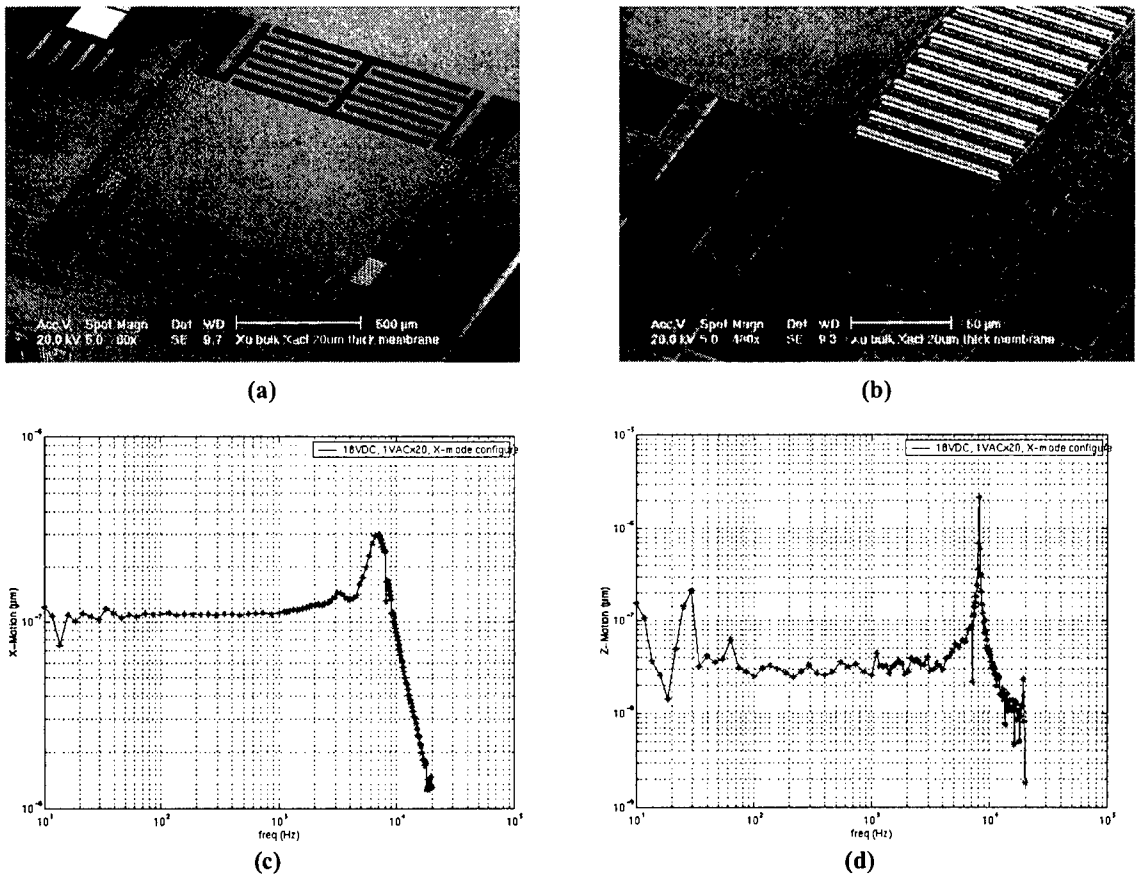


FIGURE 35. Bulk accelerometer with 25 μm thick silicon structure. (a) entire device with (b) zoom into bottom right corner. Mechanical response of bulk Si-CMOS mechanical structure with 18 VDC with 1 V_{AC} applied showing (c) x-direction resonance near 7 kHz and (d) z-direction resonance near 8 kHz.

frames are not required and simplify the designs. Figure 35(a) and (b) show an SEM of the accelerometer with 25 μm thick structural silicon underneath the CMOS interconnect stack. The micromechanical device is functional, as verified with MIT Microvision frequency response results in Figure 35(c) and (d).

A DRIE *z*-axis accelerometer, shown in Figure 36, has been designed, fabricated and tested. It consists of *z*-compliant springs, a proof mass, comb fingers for z-axis motion sensing, z-axis self-test actuators. Unlike the bulk accelerometer of Figure 35, the *z*-compliant springs in the z-axis accelerometer in Figure 36 constitute only CMOS interconnect layers where the underlying silicon is removed away by the undercut of the DRIE etching. Both accelerometers have a bulk proof mass.

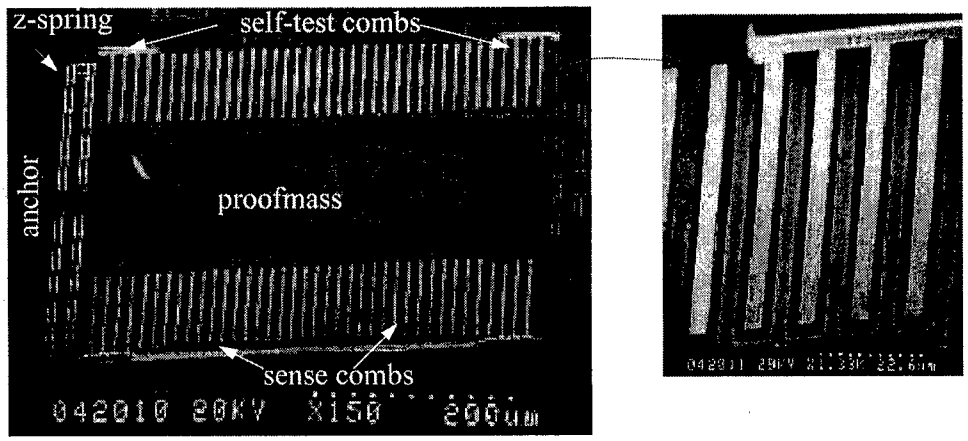


FIGURE 36. SEM of a DRIE CMOS z-axis accelerometer.

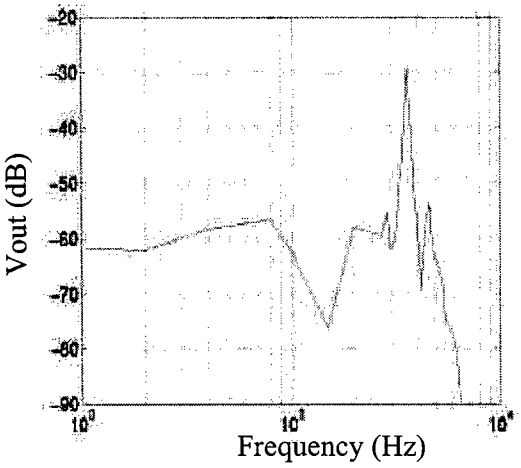


FIGURE 37. Frequency response of the DRIE CMOS accelerometer.

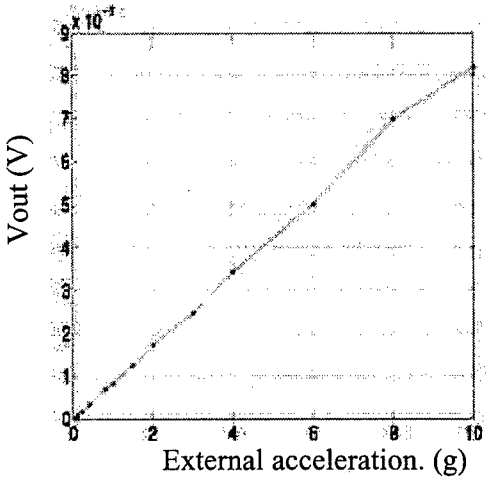


FIGURE 38. Dynamic response of the DRIE CMOS accelerometer.

A shaker table was used to characterize the *z*-axis accelerometer. The frequency response is plotted in Figure 37 showing a resonant frequency of 3.65 kHz and a quality factor (Q) of 35. The Q is about ten times larger than the Q observed from the thin-film z-axis accelerometers. The DRIE *z*-axis accelerometer has no substrate under the microstructure, thereby reducing squeeze-film air damping. Figure 38 shows the dynamic response which has a linear range of ±10 G. Figure 39 shows the spectrum of the output signal at the presence of a 0.5 G, 100 Hz external acceleration. The noise floor is about 0.5 mG/$\sqrt{\text{Hz}}$ which is similar to the measured noise in the thin-film z-axis

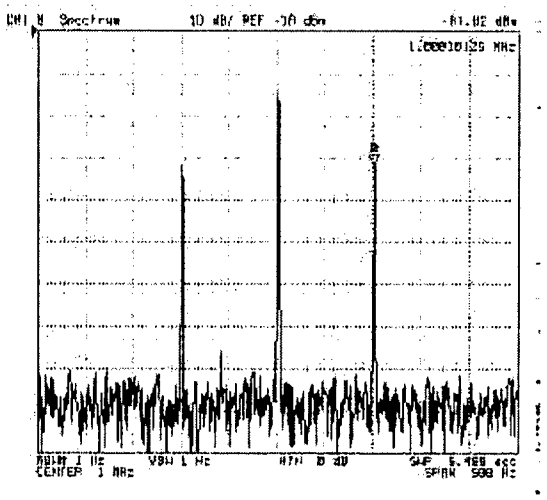


FIGURE 39. Output signal spectrum of the DRIE CMOS accelerometer.

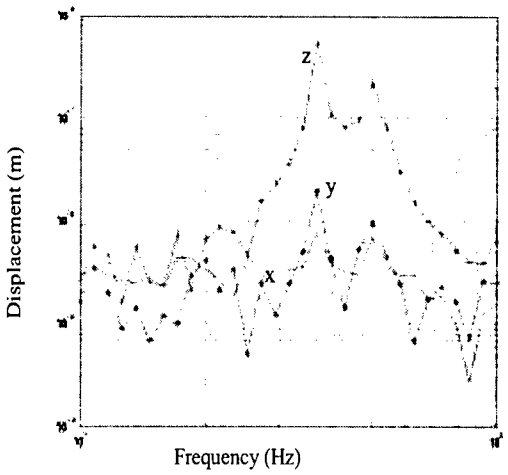


FIGURE 40. Vibration excited by self-test actuators on the DRIE CMOS accelerometer (measured with the MIT Microvision system).

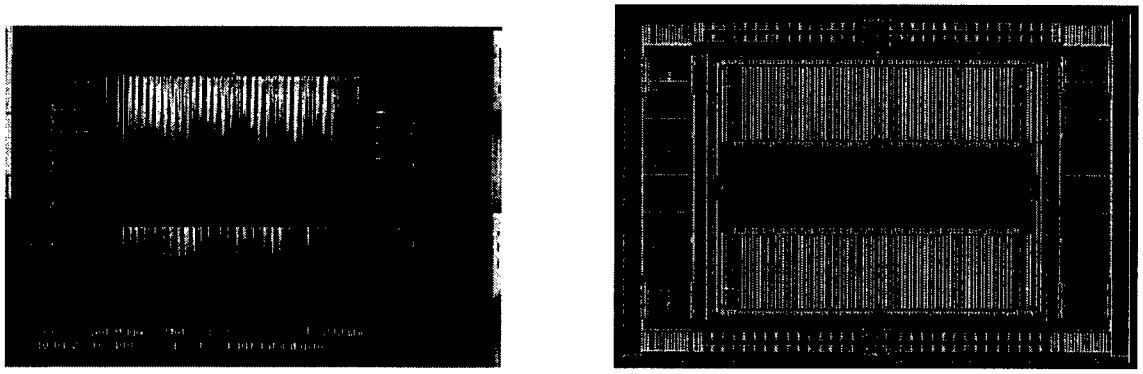


FIGURE 41. (a) SEM of the first DRIE lateral-axis gyroscope and (b) updated layout design of second generation DRIE lateral axis gyroscope.

accelerometers. Currently, the limitation in the inertial sensors is circuit noise, not thermomechanical noise.

The MIT Microvision system is used to study the vibration excited by the integrated self-test actuators, as shown in Figure 40. There two out-of-plane modes, z and θ_z, which have resonant frequencies of 3.7 kHz and 5.0 kHz, respectively. The Q is about 40, which is consistent with the acceleration measurement (see Figure 38).

Figure 41(a) shows the first design of DRIE CMOS-MEMS lateral-axis gyroscope. As in the

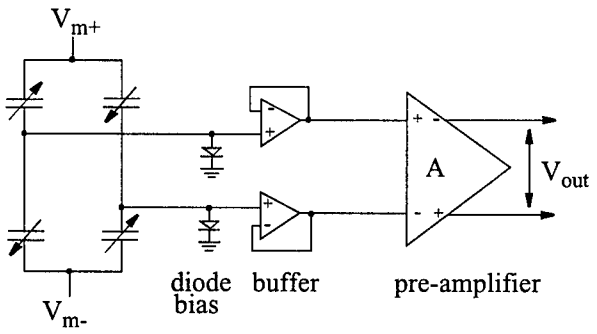


FIGURE 42. Schematic of on-chip sensor and circuitry.

thin-film design described above, the *z*-drive is divided into four individually controllable parts, which can be used to balance the *z*-motion. In addition, there are *y*- and *x*- axis comb drives for compensating off-axis motion. The gap between most of the comb fingers was designed to be 1.5 μm. Due to metal debris between the comb fingers, the microstructure was not released, hence a new design with 2 μm between comb-fingers (Figure 41(b)) is in fabrication at the time of this report.

4.3 Interface Circuits

In early inertial sensor designs, differential front-end interface circuitry consisting of unity-gain buffers and pre-amplifiers was integrated on chip. One such circuit is shown in Figure 42. Diodes are used at the inputs of the buffers to provide dc bias. No driven shielding is used due to small parasitic capacitance. The circuit is simple, however it has a major problem with dc biasing. The n-well diodes may be placed in the circuit with either polarity, however the n-well has a parasitic diode to the substrate. In either case, the input voltage tends to drift to the supply rail that maximizes reverse bias on the diode. This saturates the buffer and renders the circuit inoperable.

In the lateral accelerometers and vertical gyroscope, a transresistance amplifier is used at the input stage, as indicated in Figure 43. The dc bias is set by the feedback transistor. The influence of the parasitic capacitor at the input node is reduced by the gain of the input amplifier. A readout circuit for the lateral accelerometer consists of a low noise amplifier (LNA), a multiplier-based mixer, and an operational transconductance amplifier (OTA) as shown in Figure 44. It offers low input-referred noise level and high electrical gain. A fully differential signal path is used from the differ-

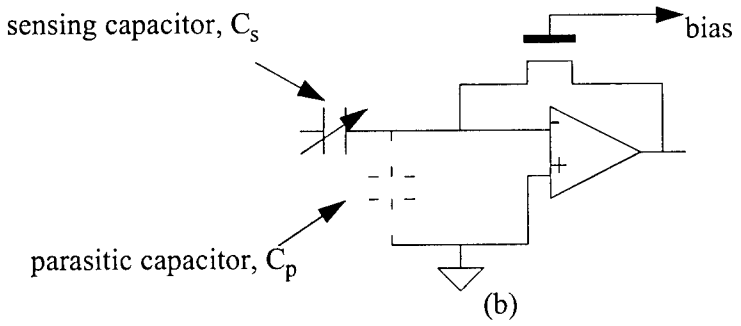


FIGURE 43. Transresistance amplifier sensing.

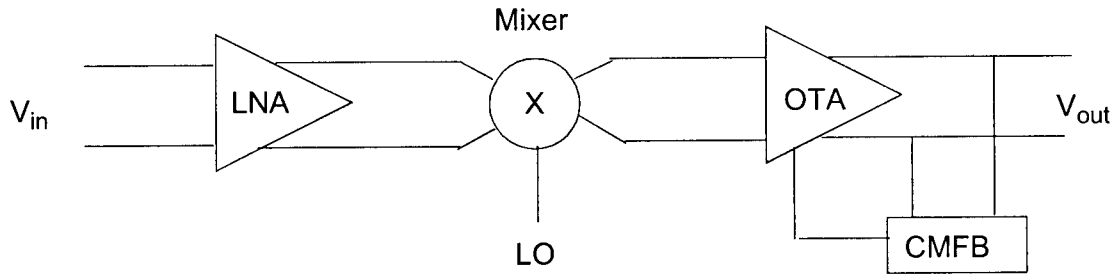


FIGURE 44. Readout Circuit

ential capacitive sensor to the differential linear actuator for closed-loop force-balanced operation. The output common-mode feedback circuit (CMFB) controls the gain of the electrostatic actuator.

A design trade-off has been made between input-referred noise and input capacitance. The LNA uses transistors with large aspect ratio (W/L) driving large current to achieve superior thermal noise performance, but has much larger input capacitance. Compared to traditional voltage buffering, simulation shows the LNA improves the signal-to-noise ratio (SNR) by at least 10 times while offering 5x signal gain. A current reuse scheme is used in LNA design, in which an n-transistor and a p-transistor are both used as input transistors. The mixer uses n-transistors with large W/L as input transistors, therefore, also have good thermal noise performance. The OTA provides large gain (>500) and its thermal noise performance is of less importance. The OTA has p-type input transistors to reduce the low-frequency flicker noise. HSPICE simulation results show a nominal input-referred electrical noise floor equivalent to 4 $\mu g/\sqrt{Hz}$. However, the measured noise of the accelerometers using this circuit are limited by the flicker noise of the input stage.

Monte-Carlo simulations were performed on several capacitive sensor readout circuits, with

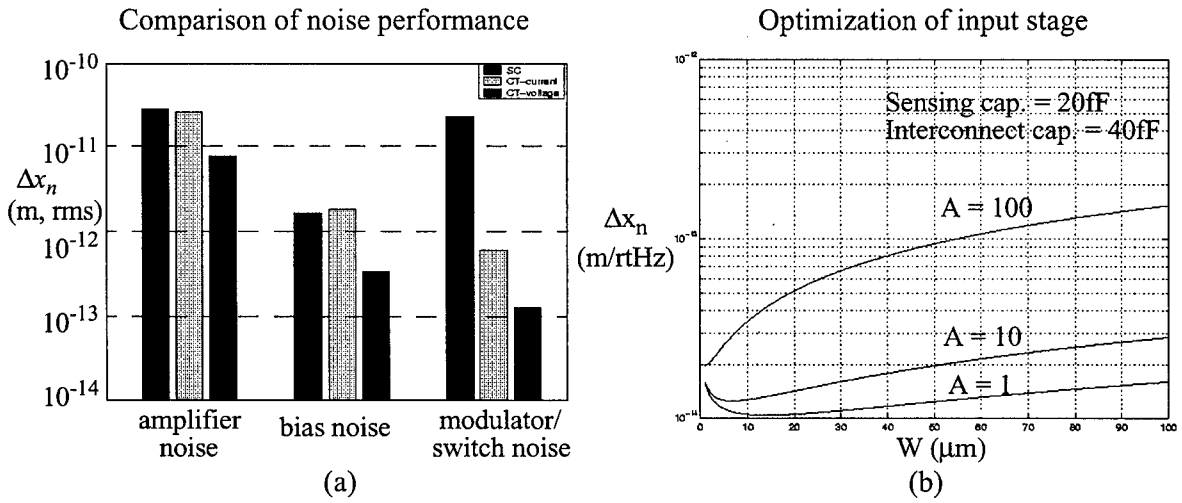


FIGURE 45. Noise in capacitive sensor readout circuits: (a) Comparison of noise performance of different readout schemes by Monte-Carlo Simulation. SC = switched-capacitor readout, CT-current = continuous-time transresistance current readout, CT-voltage = continuous-time voltage readout; (b) Optimization of transistor sizing and gain in the input stage

a summary of the results in Figure 45(a). The results showed that the continuous-time voltage readout can achieve up to 10 times lower noise floor than the commonly used switched-capacitor and transresistance current readout circuits. A study on voltage readout amplifiers suggested that the sizing and gain of the input stage should be optimized to obtain minimum sensor input-referred noise floor, as illustrated in Figure 45(b). Tests on previously fabricated CMOS-MEMS devices indicated that one failure mode was the saturation of high-gain CMOS amplifier by offset voltage.

From the simulations, voltage amplifiers are seen to have superior noise performance than both switched-capacitor charge integrators and transresistance current amplifiers. However, two major issues with open-loop voltage amplifiers are: the high-impedance input nodes must be properly biased; and the offset must be controlled to prevent saturation and preserve dynamic range. As our original diode-biased capacitive sense circuit is adversely sensitive to input dc drifts, a switched-reset correlated-double-sampling circuit architecture was developed and is shown in Figure 46. A temperature independent capacitance sense circuit was implemented. The gain of the circuit is determined by the ratio of polysilicon resistors that remains constant with temperature by placing both resistors on a micromachined thermally isolated platform. On-chip voltage references also use thermally tunable polysilicon resistors suspended on micro-plates. A constant g_m bias circuit ensures the open-loop gain of the op-amp is greater than 100 dB over the 0° to 100° range. The

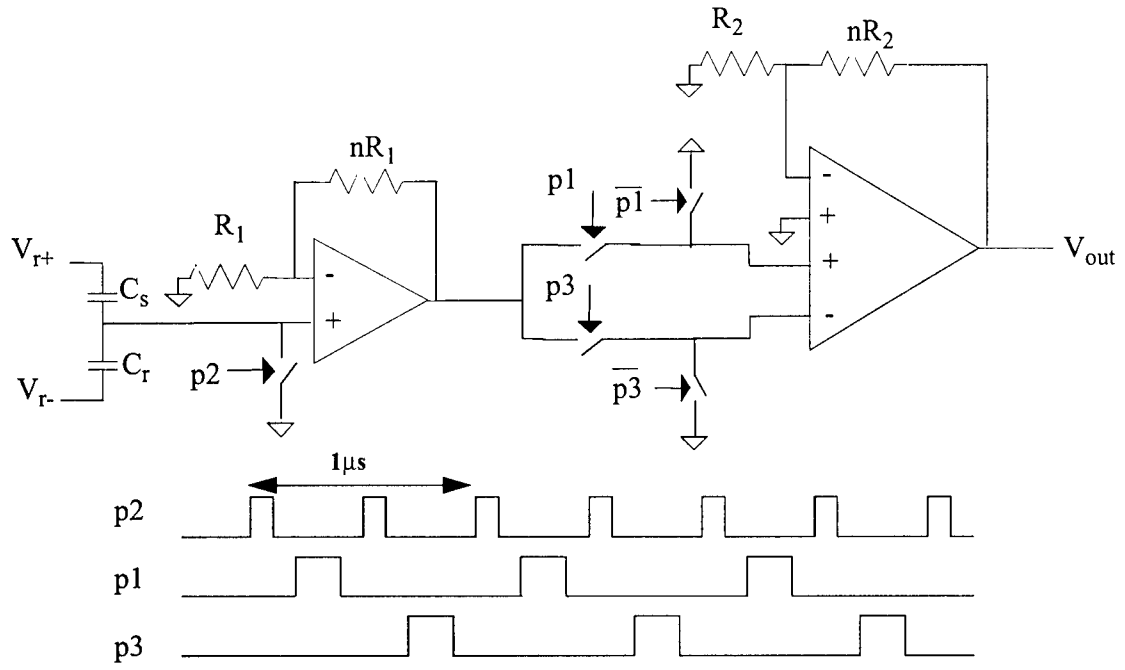


FIGURE 46. Schematic of the chopper stabilized capacitance sense circuit. C_s and C_r are the sense and the reference capacitors. V_{r+} and V_{r-} are the DC reference voltages. The reset signal p2 is shown activated every cycle, but can be activated every N cycles.

switch charge feedthrough that can reduce the dynamic range of the circuit has been minimized by a dynamically compensated switch. The fabricated circuit shows that the resetting bias scheme, without tuning, prevents input bias drift observed in other biasing methods. This scheme poses no limits on bandwidth which indicates no noise injection from bias circuit as shown in Figure 47.

4.4 Temperature Control of CMOS Micromachined Inertial Sensors

We report a scheme for control of temperature-dependent structural curl in CMOS micromachined sensors [1] to improve the thermal drifts in sensitivity and offset. As discussed previously, one concern in design of CMOS micromachined sensors is structural curling due to the multilayer material. Residual stress gradients due to manufacturing, and differences in temperature coefficient of expansion (TCE) of the metal and the oxide layers lead to temperature dependent curling in the structure. The change in structural curl causes variation of sensitivity and offset in inertial capacitive sensors, as the overlap area of the sense capacitance changes with curl. It is desirable to control local temperature of the structures to compensate both vertical and lateral curl induced due to man-

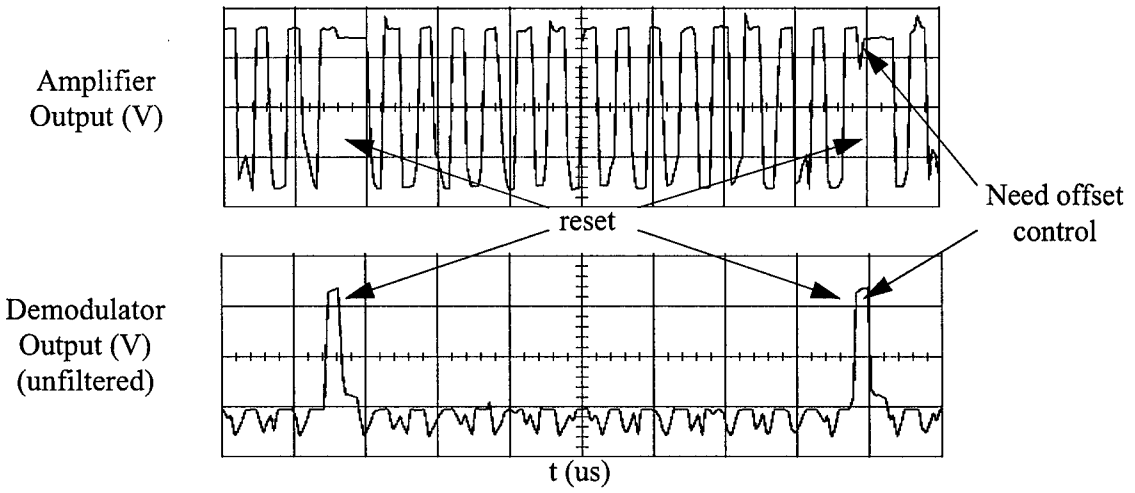


FIGURE 47. Measured chopper stabilized readout amplifier output waveforms

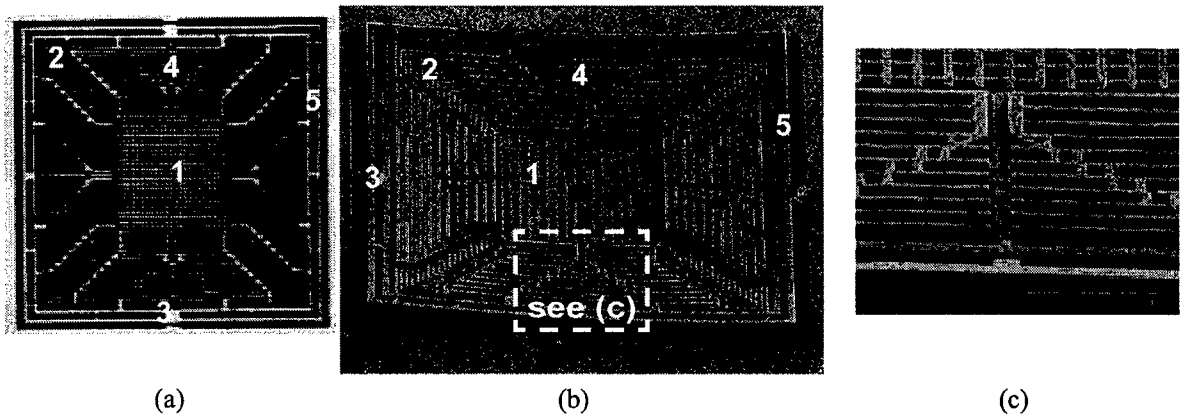


FIGURE 48. Thermally stabilized vertical accelerometer. (a) Optical photograph. (b) SEM. (c) Close-up of comb fingers. 1) Proof mass with embedded polysilicon heater, 2) Meander spring, 3) Thermally insulating anchor, 4) Sense comb, 5) Semi-rigid frame for stator comb, with embedded polysilicon heater.

ufacturing variations that contributes to DC offsets.

As a testbed for studying temperature control, a topology is studied that is different from the vertical-axis accelerometer described earlier in Section 4.2.2. The alternative design, shown in Figure 48, has two-axis symmetry. It incorporates a custom mender-spring suspension with comb "trees" connected to the central proof mass plate.

The capacitive comb for vertical motion sensing exploits beam curling to create a vertical offset between the stator and rotor fingers. All three conductors in the fingers are electrically con-

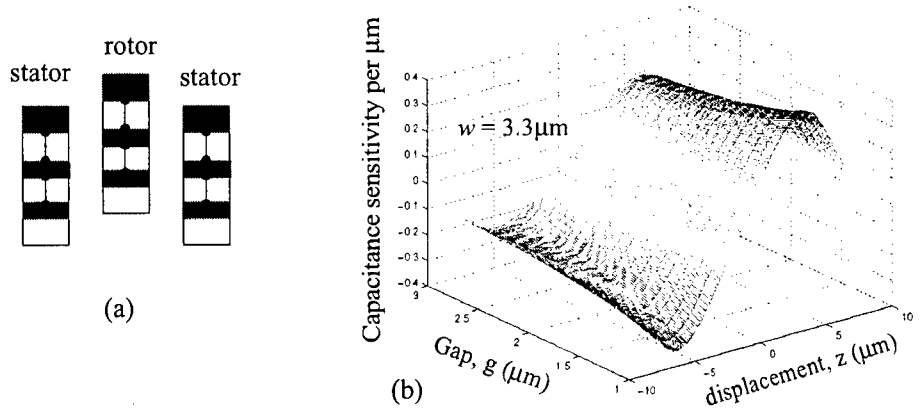


FIGURE 49. (a) Cross section of comb fingers (b) Variation of 3.3µm-wide comb finger sensitivity capacitance as a function of varying gap and z displacement.

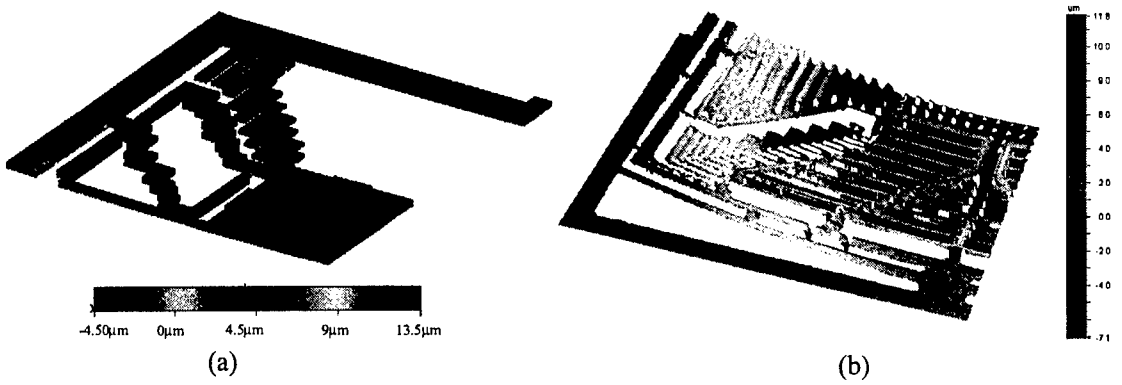
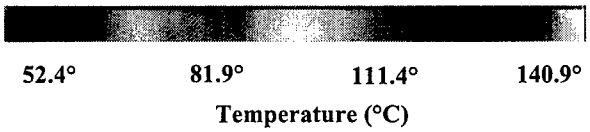


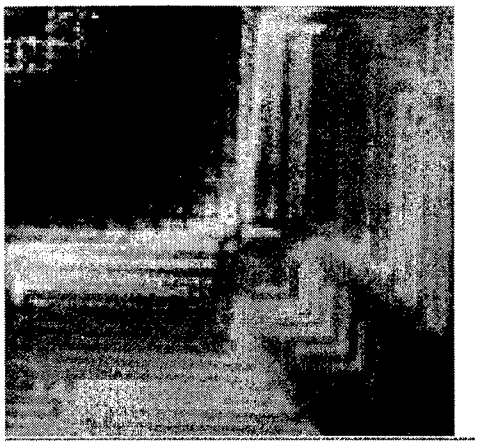
FIGURE 50. (a) FEM simulation of the structural curl using the techniques in [38]. (b) Structural curl at room temperature measured using a white light interferometer. The rotor and stator combs are out-of-plane by more than 10 µm at the point furthest from the anchor.

nected together as shown in the inset of Figure 49. The comb drive is designed by using measured curl values of various beams with different metal and oxide combinations [9]. A thermomechanical finite-element analysis of the device curling is shown in Figure 50(a). The sensitivity of the device is a function of the z overlap of the comb fingers and thus is a function of ambient temperature. The accelerometer curl at room temperature, measured using a white-light interferometer, is shown in Figure 50(b).

The capacitance of the device is sensed by temperature-independent, constant-gain on-chip circuits using a chopper-stabilized scheme. The schematic of the circuit along with the clock

FIGURE 51. Temperature distribution within the proof mass of the Z accelerometer with ohmic heating of the rotor polysilicon resistor.





sequence is shown in Figure 46. For the final design iteration, the sensitivity of the transducer before circuit gain is 0.13 mV/G/V (for 1 V p-p modulation input voltage), and 9.3 mV/G after on-chip amplification. The noise floor is $2\text{mG}/\sqrt{\text{Hz}}$, limited by circuit noise. The dominant mechanical mode of the sensor is out-of-plane at a resonant frequency of 3.2 kHz.

Thermal stabilization is implemented by controlling device temperature through joule heating of the entire device by three optimally embedded polysilicon resistors in the rotor proof-mass, rotor comb, and stator. Previous work by Nguyen has focused on temperature stabilization of resonators using polysilicon heaters on a micro-fabricated hotplate external to the device; this is the first report of polysilicon heaters for temperature control embedded in the inertial sensing device structure. This leads to better temperature distribution and lower power. The polysilicon of the CMOS process is not normally used in microstructure design and therefore the thermal stabilization design is independent of the mechanical design of the device. The width of the heaters was designed using a finite difference modeling technique and modified Levenberg algorithm for the optimization to ensure uniform temperature distribution. The device temperature is measured *in situ* by monitoring the resistance of the polysilicon. The temperature of the polysilicon heaters is set by a digital controller. The temperature coefficient of polysilicon is obtained by calibration in a oven to be $0.00459\ \text{K}^{-1}$ and the thermal time constant of the device is 3 ms.

Measurements were made on the *z*-axis accelerometer with integrated heater embedded in the rotor using an infrared camera, as shown in Figure 51. The temperature distribution within the proof mass is not uniform due to conduction losses from the heated rotor to the substrate. These

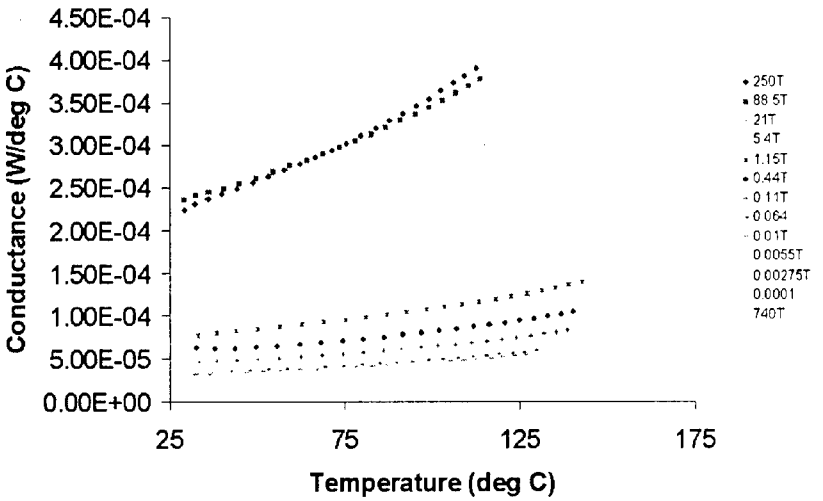


FIGURE 52. Conductance of the Z axis accelerometer with integrated heater with temperature under different vacuum conditions.

results were used to optimize the placement of polysilicon heater elements by varying the power dissipation per unit length of the polysilicon resistor.

The CMOS micromachined *z*-accelerometer with integrated polysilicon heaters was tested to obtain the thermal conductivity of air and that of the anchors. The plates were heated in vacuum to isolate the heat loss from air. The thermal conductance of the anchor was $31.8\mu WK^{-1}$ and that of the entire structure was $250\mu WK^{-1}$. The thermal capacity of the proof mass was measured to be 3.88 JK^{-1}. The conductance of the device is shown in Figure 52. The substrate temperature was measured using the variation of the diode threshold voltage with temperature. The threshold voltage variation of the on-chip diode was calibrated by measurements in a temperature controlled oven.

To measure the curvature of CMOS micromachined devices, four phase-shifted images were recorded to obtain the phase change information. The phase information was unwrapped to obtained the *z*-axis deflection at various points of the structure. The phase unwrapping algorithms were combined with mask data derived from the image to obtain good quality data. Different phase unwrapping algorithms were evaluated for this application. The Goldstein's algorithm was found to be the best when combined with the masking data. The curvature of the *z*-axis accelerometer proof mass was measured at various temperatures, as illustrated by the representative data in Figure 53.

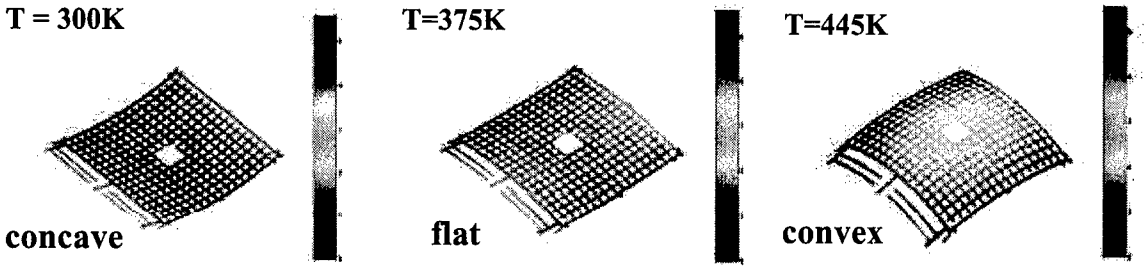


FIGURE 53. Variation of proof mass shape with temperature

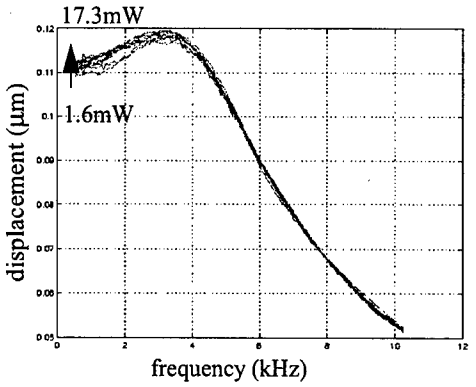


FIGURE 54. Sensor mechanical frequency response with different rotor heating power.

The mechanical frequency response of the structure at different rotor heating power inputs is shown is Figure 54. The measured capacitance change with rotor heater temperatures at various chip temperatures is shown in Figure 55(a). The acceleration sensitivity of the device was measured, at various temperatures, using a shaker table and is shown in Figure 55(b). Successful thermal control is demonstrated in Figure 56, where the device capacitance is stabilized over a 100°C temperature range. This initial experiment is not optimized because only the rotor temperature is controlled, not the stator temperature. Characterization of three-heater control will be reported in [71].

Thermal Frequency Tuning

Z-compliant spring beams used in the lateral gyroscopes and some *z*-axis accelerometer designs are realized by using the first CMOS metal layer as the etching mask. These structures are only about 1 μm thick and experience a very large out-of-plane curl. Figure 57 shows the close-up of a *z*-spring beam whose end curls up about 70 μm due to the residual stress and thermal coeffi-

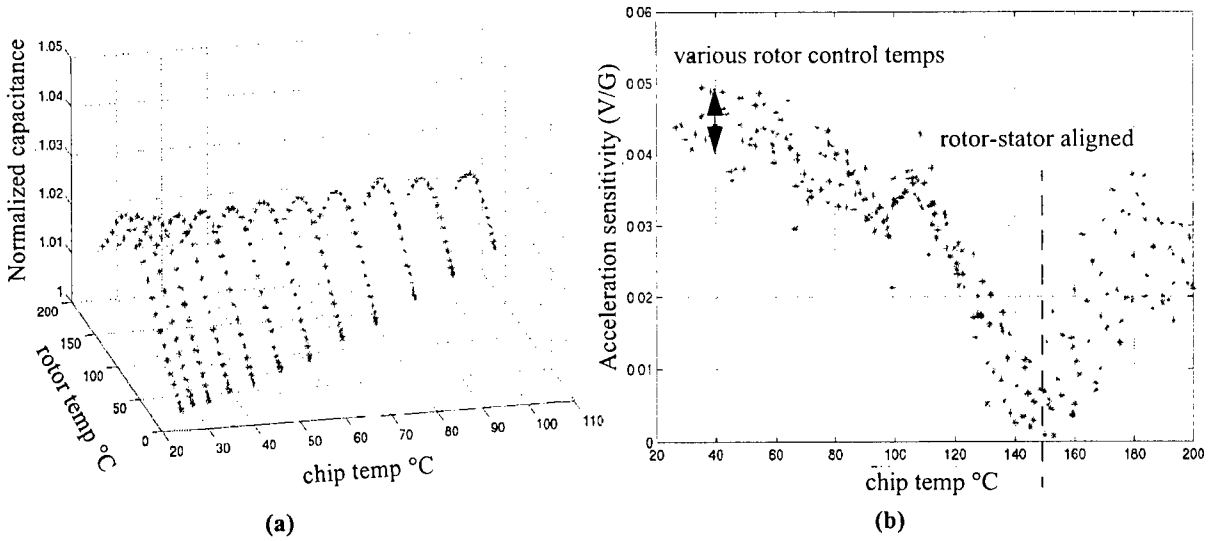


FIGURE 55. Normalized capacitance change measured with different control temperatures of rotor heater. The rotor moves from above the stator to below. (a) Variation of nominal capacitance. (b) Sensitivity to acceleration measured at various rotor control temperatures. The sensitivity is minimum when the rotor and stator are aligned.

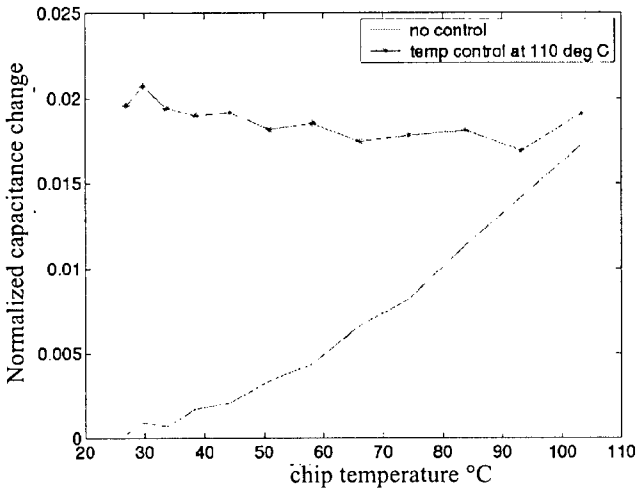


FIGURE 56. Improvement of accelerometer temperature performance without and with temperature control at 110 deg. C. The small reduction in device capacitance in these initial measurements is because only the rotor heater is activated.

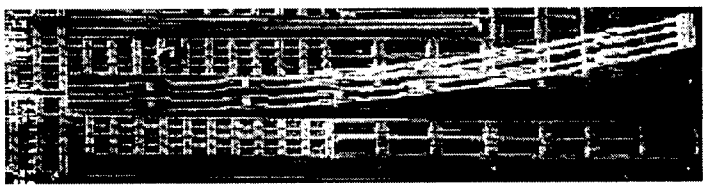


FIGURE 57. SEM of a vertically compliant spring with an embedded polysilicon heater, showing large out-of-plane curl of the metal-1 structure at room temperature.

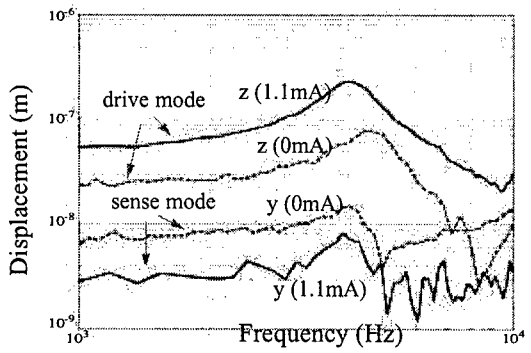


FIGURE 58. Frequency response of the drive and sense modes with and without heating current.

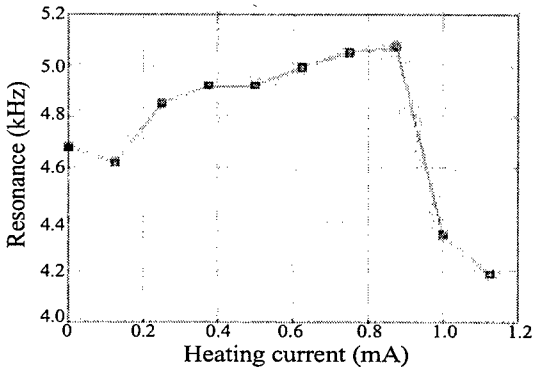


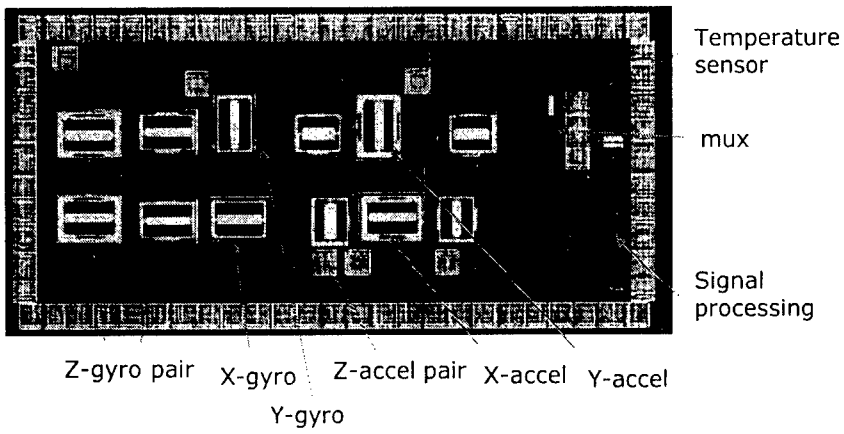
FIGURE 59. Resonant frequency change of the drive mode with respect to heating current.

cient mismatch in the embedded layers inside the beams. This curling can be compensated by injecting a current through a polysilicon resistor inside the spring beams. With the aid of the MIT Microvision system, it was observed that flattening the spring beams suppresses mode coupling and changes the resonant frequency of the drive mode (Figure 58). Meanwhile the resonance of the sense mode stays almost unchanged, due to the gimbaled topology. Therefore, the integrated heater provides an alternative method to match the resonant frequencies of the sense and drive modes. The measured dependence of the resonant frequency of the drive mode to the heating current is shown in Figure 59 in which the rapid change occurs when the spring beams are approaching to the flat state. These trends are predicted by MEMCAD thermomechanical simulation.

4.5 Inertial Sensor Arrays

The individual designs described above are all intended to support the array-based integration of a single-chip IMU. A first iteration monolithic IMU was designed and submitted in an ASIMPS alpha run, and is currently being fabricated (Figure 60). ASIMPS is the DARPA-sponsored Application-Specific Integrated-MEMS Process Service to make CMOS-MEMS available for prototyping. The IMU has three axis acceleration and three axis rotation sensing and an integrated temperature sensor. The array incorporates a newly designed vertical-axis gyroscope that suffers less curling, requires lower actuating voltage, and has auto-gain-control (AGC) circuits. Also included is a newly designed lateral-axis gyroscope that incorporates lateral vibration and vertical sensing to overcome the severe damping in the vertical vibration scenario.

FIGURE 60. CMOS-MEMS monolithic IMU.



4.6 Layout Extraction

The IMU being considered as part of this project consists of several MEMS inertial sensors, each of which involves design trade-offs in the geometrical design of the transducer, as well as the interface between the sensor and its electronics signal processing circuitry. At the start date of the project, the existing verification techniques involved solid model generation and meshing from the layout for continuum simulation of the MEMS transducer [5]. Even so, only two physical effects tended to be captured (electrostatic and elastostatic). As inertial sensors are dynamic components, modeling of the static as well as dynamic effects (dominated by parasitic damping and mode coupling in the mechanical domain and capacitance and resistance in the electrical domain) is essential. Unfortunately no tools were available at that time. Therefore, we embarked on developing an extraction-based MEMS layout verification flow that mimicked the VLSI extraction flow, and exploited the NODAS schematic simulation capabilities developed in the "Foundations of MEMS Synthesis" project supported by DARPA MTO's Composite CAD program [7].

Our initial efforts focused on developing an overall algorithm to convert MEMS layout into a schematic representation that can be simulated using our hierarchical front-end simulation strategy, NODAS (NOdal Analysis of Actuators and Sensors). At that time NODAS was based on the Saber simulation environment and was targeted to the polysilicon MUMPS process. Therefore we initially focused on just the MEMS part of the layout, and on the MUMPS process. The overall algorithm includes: reading in the MEMS layout as a CIF file, using the canonical representation algorithm to generate a unique representation of the MEMS layout, using feature recognition heu-

ristics for identification of atomic elements such as beams in the layout, using component extraction algorithms for identification of components such as comb drives and complex beam-springs in the layout, and finally schematic generation to create a NODAS compatible schematic.

The initial polysilicon MEMS extractor, capable of identifying beams and plates, was demonstrated in fall 1998, and was made available to the MEMS community via the Carnegie Mellon MEMS Laboratory web site [20][74]. A second generation extractor was developed in 1999 for MEMS component extraction (of comb-drives and springs) [33]. Also in 1999, we demonstrated how the canonical recognition algorithm generates the simplest mesh for continuum simulation, and could be tied with the layout recognition heuristics to automatically mesh the layout for simulation in continuum MEMS simulators such as CoventorWare (then called MEMCAD) and CFD-ACE [32]. In 2000 and 2001 the focus was on CMOS-MEMS extraction, particularly of the parasitic elements required for the verification of inertial sensors [65][70]. We now provide short descriptions of select components of the layout extraction algorithm.

4.6.1 Canonical Representation

Designers tend to design layouts in their own specific way resulting in non-unique representations of the same layout. The extraction tool converts such representations to an unique representation in order to simplify the recognition algorithms used later for extraction. There are various types of unique representations that are followed in VLSI CAD, out of which the tile plane representation is well known. The *canonical representation* is a derivative of the tile plane representation. Unlike the tile plane representation, where each tile can have multiple neighbors on each of its sides, the polygons in canonical representation can either have one or no neighbors on each edge. Having such an unique neighbor information makes the neighbor based recognition algorithms simpler to implement.

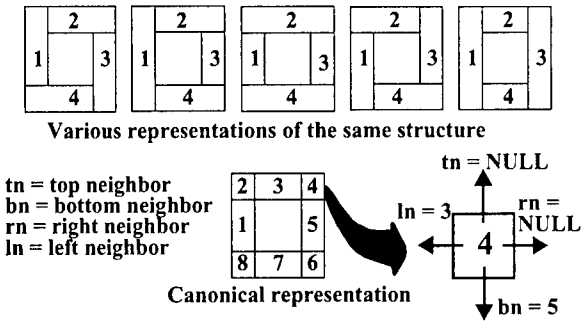


FIGURE 61. Fully partitioned canonical representation

As a vast majority of MEMS layouts are Manhattan, the prototype implementation is limited to Manhattan designs only. Figure 61 explains canonical representation in the context of Manhattan designs. We define the *canonical representation* of the layout to be the *one which uses minimum number of rectangles to cover the given layout area, such that infinitesimal outward extensions of an edge of any rectangle never intersects with the interior of the layout area.* We use the term *layout area* to define the area which represents the actual component in the layout, *i.e.* it is the interior area(s) defined by the boundary/boundaries of the geometrical representation of the component in the layout. Thus, in the canonical representation, the Manhattan layout is made up of rectangles such that each rectangle has *at most one neighbor per edge and each edge is either fully covered by a neighbor or not covered at all.* This can be easily achieved by extending the boundary edges into the interior of the layout area till it meets another boundary edge. The resulting representation uniquely partitions the layout area. Extension to non-Manhattan geometries can be accomplished by following the same principle after replacing rectangles by polygons.

The process of canonization starts from the input geometric description of the chip (written, perhaps, in CIF, *i.e.* Caltech Intermediate Form). The hierarchical layout description of the chip is first flattened followed by the removal of all overlaps between polygons. An initial rectangular cover of the layout is then obtained for the suspended structural pattern in the structural polysilicon mask. This serves as input to the actual canonization routine.

The primary interaction in the canonization process takes place between two sets; the input set and the output set. The output set is always kept in canonical state with respect to its contents and will eventually contain the canonical version of the input set. Elements from the input set are selected sequentially and added to the output set. Whenever there is an addition to the output set, its equilibrium might be destroyed (*i.e.*, the output set might no longer be a canonical set). If this occurs, a series of operations is initiated which ultimately brings the output set back to its equilibrium or canonical state. This is repeated till the input set is empty at which point the output set will

contain the canonical representation of the input layout. The process which drives the output set to equilibrium, after it is disturbed by the insertion of a new element, is described below:

ADJACENT(***rectangle*** *a,* ***rectangle*** *b*): returns ***TRUE*** if *a* and *b* have a common edge

SPLIT(***rectangle*** *a,* ***rectangle*** *b*): splits *a* by edges of *b,* if any of the vertices of the edges of *b* lies on any edge of *a,* and also updates the neighbor information

```
CANONIZE(rectangle_set R)
  G = NULL
  while R != NULL
    r = pop[R]
    P = NULL
    push[P, r]
    Q = {x|ADJACENT(x, r); x is an element of G}
    G = G - Q
    for i = 0 to length[Q]
      for j = 0 to length[P]
        SPLIT(P[j], Q[i])
    for i = 0 to length[P]
      for j = 0 to length[Q]
        SPLIT(Q[j], P[i])
    M = Q
    until M = NULL
      N = NULL
      for i = 0 to length[M]
        S = {x| x is neighbor of M[i]; x is element of G}
        G = G - S
        for j = 0 to length[S]
            SPLIT(S[j], M[i])
        N = N + S
      P = P + M
      M = N
    G = G + P
  return
```

The neighbor information of each rectangle in the resulting canonical representation comes as a by-product of the algorithm. Each rectangle in this representation has four pointers which point to the neighbor, if it exists, on each of the sides (as shown in Figure 61). The algorithm has a worst case asymptotic upper bound of $O(n^{1.5})$, where n is the number of rectangles in the final canonized

representation. Though this is much greater than the usual complexity of VLSI CAD tools, which normally tend to be *O(nlgn)*, it does not pose a serious time restriction since the problem size is much smaller (~1000) than that encountered in VLSI world. Nevertheless, the algorithm does have ample scope of improvement in terms of time and storage requirements if the problem size increases.

4.6.2 Extraction of Atomic Elements

Atomic elements form the fundamental building blocks of MEMS components [44]. Suspended MEMS essentially consists of structural areas suspended over the substrate. Such suspended areas can be partitioned into two groups based on their relative rigidity: *plates* and *beams*. The suspended areas of the structure, which are relatively rigid to forces along the plane of the structure, are defined to be *plates*. They are the major contributors to the mass of the suspended structure. The structural compliance of the suspended structure is decided by the *beams*. Geometrically these are rectangular areas having neighbors only on their shorter sides. Cantilever beams are often classified separately as *fingers* and are extensively used to design electrostatic actuators and sensors. Sometimes fingers are provided with pedestals to reduce the inter-finger gap below the lithography limit for higher sensitivity of the mechanical to electrical transfer function for the electrostatic transducer. Two or more beams are connected by *joints* which can be modeled in the adjacent beams for simplicity. Hence joints serve as logical connectivity elements. The suspended structure is connected to the base (interconnect polysilicon) at the *anchors* which are defined by the anchor-cut mask. These areas provide electrical connection to the suspended structure and also act as mechanical pillars supporting the suspended areas.

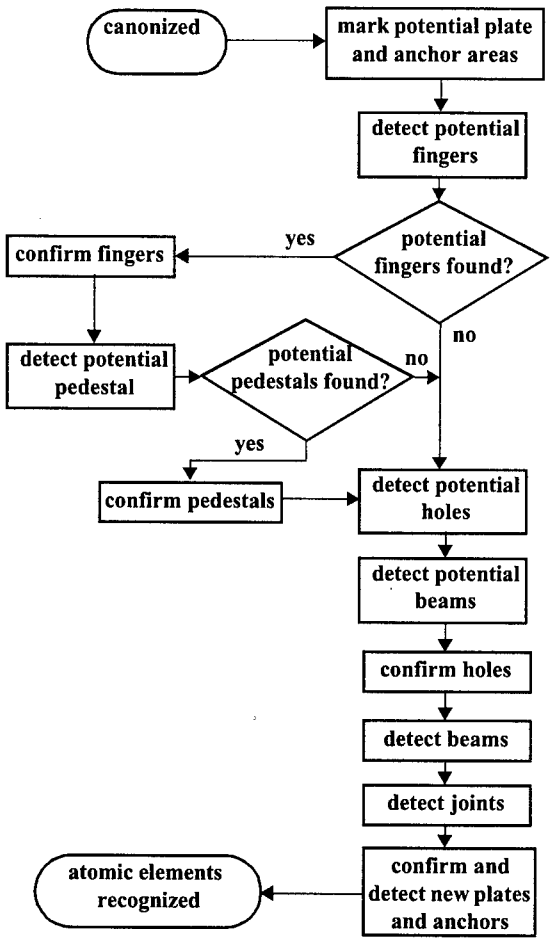
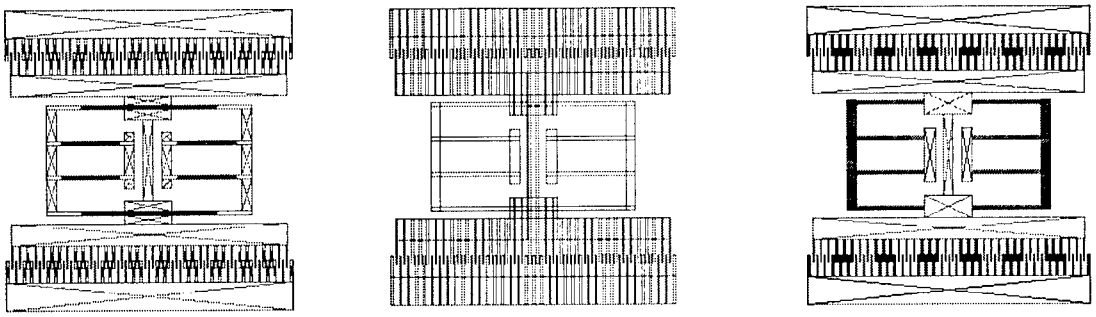


FIGURE 62. Flow chart for extraction of atomic elements

At this stage of extraction, a canonical representation of the layout geometry is available and the objective is to tag each rectangle in the canonical representation by the correct element type (anchor, plate, finger, beam or joint). The recognition of each type of elements is a two step process as shown in the flow diagram in Figure 62. The first step marks probable elements which are confirmed in the second step using stricter rules.

The first step in the recognition process is to mark potential plate and anchor areas using information from the non-structural masks. For example, overlap of the structural mask with the *anchor-cut mask* is used to tag potential anchors. Similarly overlap with *hole mask* and *bushing mask* are used to tag potential plate rectangles.

The next step is to mark potential fingers from the neighbor information of the rectangles. These are rectangles having a neighbor at one of its shorter sides. The subroutine to confirm fingers selects those rectangles or connected sets of rectangles (fingers split into multiple rectangles during the canonization process), out of the set of potential fingers, which satisfy the criteria that a finger can have only one neighbor and it should lie only on one of its shorter side. If fingers are detected they are removed from the total set of rectangles and the remaining structure is recanonized. This reduces the number of rectangles being checked by the subroutines and also helps in detecting pedestals which come out as fingers in the remaining geometry. The worst case complexity of the finger detection is $O(n + mp)$ where, n is the initial number of rectangles, m number of rectangles tagged in the first loop and p is the remaining rectangles (n-m). Though theoretically this implies quadratic time complexity, in reality it does not



(a) Input layout (CIF) (b) Canonical Representation (c) Heuristic-based recognition

FIGURE 63. Folded Flexure resonator (a), its derived canonical representation (b), and initial heuristic-based recognition results (c).

create any serious time limitation because the problem size is small ($m \sim 100$).

In the next step, any rectangular empty space surrounded by filled rectangles on each side is tagged as a potential hole. This is achieved by sieving out rectangles in the canonized representation of the geometric *not* of the structural geometry. This is followed by the detection of potential beams which are rectangles having neighbors on each of their shorter sides. This is used by the hole confirmation routine which removes potential holes that are actually gaps between beams. The holes detected are then replaced by filled rectangles followed by a recanonization of the resulting geometry. The change in physical parameters (like mass-factor, center of mass, *etc.*) due to the addition of these filled rectangles is annotated to the corresponding rectangles. In addition to reducing the number of rectangles in the representation of the layout, the recanonization also reduces the chances of split beams.

The next step detects beams and joints using neighbor-based heuristics followed by the final detection of plates and anchors. Previously marked potential plate and anchors are used as seeds to recursively expand into unrecognized areas and mark them as plates or anchors. The expansion process checks each rectangle only once and hence runs in linear time. The final recognized set of rectangles can be used to generate an atomic level schematic or can be used to proceed to functional level extraction. An example of the process from input layout, through canonical representation and atomic element recognition is shown in Figure 63.

4.6.3 Extraction of Functional Elements

Complex MEMS components are best modeled in the functional level schematic. Such schematics have fewer elements than atomic level schematics and hence allow faster simulations without any significant change in accuracy of result [55]. This motivates the extraction to the functional level instead of stopping at the atomic level. This section describes the various types of functional elements and the algorithms that are used for extracting them.

Plate and anchor. The canonization process results in a large number of interconnected plates and anchors in the atomic level schematic. Combining such interconnected rigid plates and anchors to get a minimal representation would result in a significant decrease in the number of elements in the schematic. The plates and anchors in such a minimal representation are referred to as functional plates and anchors. The algorithm described below is used to achieve a maximal horizontal or maximal vertical representation of interconnected sets of similar atomic elements depending on which representation results in smaller number of elements.

HORIZONTAL(***rectangle_set*** *A*): returns the maximal horizontal representation of *A*

VERTICAL(***rectangle_set*** *A*): returns the maximal vertical representation of *A*

PATH(***rectangle*** *a*, ***rectangle*** *b*): returns ***TRUE*** if a path exists from *a* to *b* such that every element of the path including *a* and *b* are of the same type

```
OPTIMIZE_ELEM(rectangle_set G)
   H = NULL
   V = NULL
   while G != NULL
      g = pop[G]
      P = NULL
      push[P, g]
      Q = {x|PATH(g, x); x is an element of G}
      P = P + Q
      G = G - Q
      A' = HORIZONTAL(P)
      A = VERTICAL(A)
      B' = VERTICAL(P)
      B = HORZONTAL(B')
      H = H + A
      V = V + B
   if length[H] < length[V] then return(H)
   else return(V)
```

Since the neighbor information for each rectangle is already available from the canonization algorithm, the sets Q can be easily obtained by visiting each rectangle only once. The merging algorithms also make use of the neighbor information and hence check each rectangle in the set only once. Hence the entire algorithm runs in linear time.

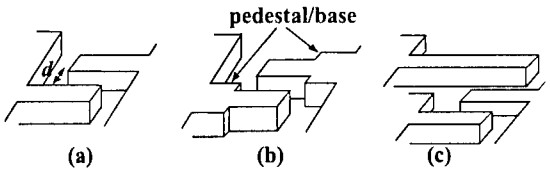


FIGURE 64. different types of finger arrangement (a) pair of cantilever beams forming the building block of electrostatic comb drive, (b) fingers with pedestals, (c) differential comb finger arrangement

Electromechanical comb actuators. Silicon microstructures have long been actuated and sensed electrostatically. A widely used electrostatic actuator is the linear comb drive made up of interdigitated fingers which may or may not have pedestals (Figure 64(a) & (b)). One side of the comb is fixed (stator) while the other side is allowed to move (rotor). Another popular electrostatic actuator is the differential comb drive (Figure 64(c)) using three sets of electrically isolated comb fingers arranged such that the rotor set of comb finger sees different sets of capacitances on its two sides. Such a structure is used to sense transverse motion via differential sensing of the two sets of capacitances and has an added advantage of reduced levitation problems.

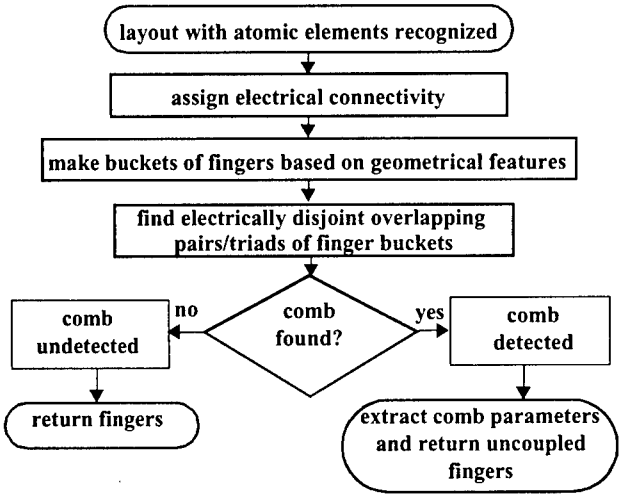


FIGURE 65. Comb drive extraction flow chart

The comb drive extraction flow is shown in Figure 65. It starts with a connectivity analysis of the set of recognized fingers. Electrically connected fingers are given the same connectivity number and then sorted into buckets based on their orientation and connectivity. Each such finger bucket is then checked for uniformity of the fingers with respect to their geometrical parameters like, region of occurrence, length of fingers, width of fingers and inter-finger gap. If the fingers have pedestals, then the geometrical parameters of the pedestal (like region of occurrence, length and width of the pedestal, inter-pedestal gap and the relative position of the pedestal with respect to the thin cantilever finger) are also checked. The buckets are partitioned whenever any non-unifor-

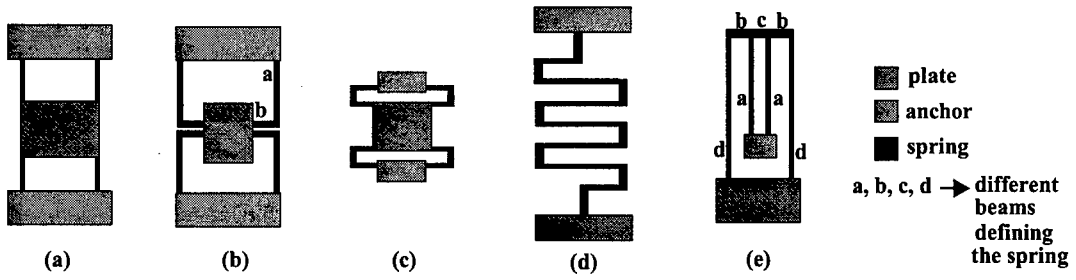


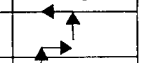
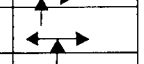
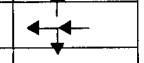
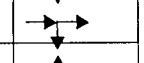
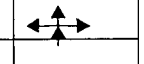
FIGURE 66. Springs in the spring library: (a) fixed-fixed, (b) crab leg, (c) U-spring, (d) meander spring, (e) folded flexure

mity is found in any of these parameters. A set of overlapping pair or triad of such buckets with different electrical connectivity numbers will result in a linear or differential comb drive respectively. The box covers of the buckets are checked using box overlap rules to find such pairs or triads. Any such set is then checked to avoid uncoupled fingers and finally grouped together to form a linear or differential comb drive.

Mechanical springs. Springs are composed of beams and joints and connect the suspended plate to the anchors. Few commonly used springs are shown in Figure 66. The fixed-fixed flexure (Figure 66(a)) consists of a simple straight beam connecting the suspended plate to the anchor and has a high spring constant because of extensional axial stress in the beams. Crab-leg springs and U-springs (Figure 66(b) & (c)) are modifications of the fixed-fixed beam to reduce peak stress in the flexure at the cost of reduced stiffness in undesired directions. A meander spring (Figure 66(d)) is also a modified version of fixed-fixed flexure which helps achieve more compliance using less space. A folded flexure (Figure 66(e)) design reduces axial stress and also has the advantages of providing more compliance while occupying less area. The springs types (like crab leg, serpentine spring, folded flexure, etc.) to be recognized are stored in the form of graphs in a library file. The spring detection routine reads in this library file to create an internal copy of the graphs. Any spring consisting of a contiguous set of beams and joints that can be represented in the manner described below can be recognized by the spring detection routine. However, the methodology described can be generalized to handle springs made of other atomic elements by incorporating user definable atomic elements.

The spring detection routine stores the spring library by creating a finite state machine

Table 5: Dictionary of joints

Joint name	m - param	t- param	ports	example
J_+	+1	0	2	
J_-	-1	0	2	
J_{T0}	0	0	3	
J_{T+}	+1	+1	3	
J_{T-}	-1	+1	3	
J_0	0	+1	4	

(FSM) for each of the springs defined in the library. Each of the FSMs can be defined by M={Q, S, L, G, F, X}, where

Q = states = {S, {intermediate states}, F, X};
S = start state = anchor point;
L = inputs = {{joints}, {beams}, NULL};
G = transition rules;
F = set of final states; and
X = exit state.

A joint, in such a language, is defined to be a node having one input port and at most three output ports and is labelled using the '*m*' (from moment) and '*t*' (from transition) parameters. The *t*-parameter is 1 only if there is an output port along the direction of the input port. An output port at right angles to the input port contributes a +1 or -1 to *m*-parameter depending on the direction of (counterclockwise or clockwise respectively). The six types of joints possible using such a convention are shown in Table 5.The set of beams for the language depend on the spring to be detected. For example, a crab leg spring requires two beams (Figure 66(b)) which may or may not be equal in dimension, while a folded flexure requires four type of beams which must be arranged as shown in Figure 66(d).

Connected sets of beams and joints obtained after the atomic recognition are passed through each of these FSMs to recognize their type. For each such set, the input is started from a beam which is connected to an anchor rectangle. The flow of the spring detection algorithm is shown in Figure 67. Any undetected spring is replaced by its atomic level representation, *i.e.* in the form of beams and joints.

Figure 68 shows the FSM that defines a crab leg. For a connected set of beams and joints,

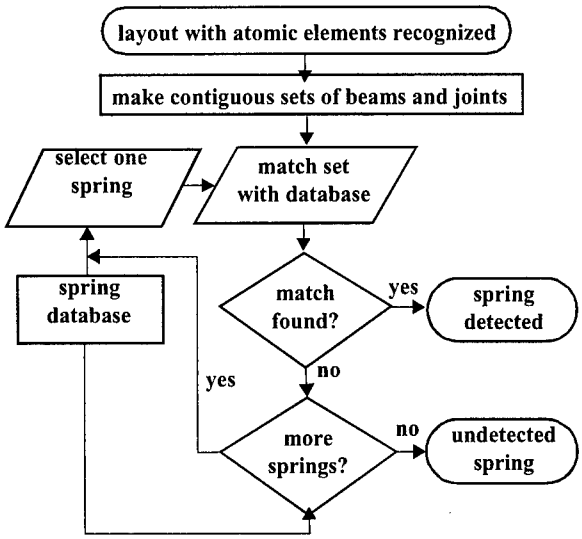


FIGURE 67. Spring extraction flow chart

the algorithm first detects the beam that is connected to an anchor rectangle and initializes the *current state* to be the *start state* (S in Figure 68) of the FSM. At every state the algorithm uses the next element in the connected set of beams and joints as the input to decide the next state. For example, for the *start state*, if the next input is a beam (which, being the first instance of beam, will be registered as *beam a*) then the *current state* advances to *state 1*. If the input is not a beam (i.e if it is a joint or if there are no other elements in the set) then the *current state* advances to *state x*. Reaching *state x* implies that the given set is not a crab leg and the algorithm exits from the current spring type (crab leg). It then tries to match the set with some other spring type in the library. If there are no more spring types remaining in the library, the current set is marked as an unrecognized spring. For a set that forms a crab leg, the first input will be a beam (*beam a*) followed by either a J_+ or J_- joint and finally another beam (which will be marked as *beam b*). At this point the *current state* will reach *state 4*. For a crab leg, there should be no more elements (beams or joints) left as input. If this is the case (i.e the input is NULL, symbolized by ϕ in Figure 68), then the current state reaches *final state* (F) and the set of beams and joints is recognized as a crab leg.

In 1999, we combined the capabilities described above with a netlist generator that directly interfaces with the Cadence Spectre version of NODAS, and demonstrated the first layout verification experiments ever. As an example of this capability, the steps in the extraction and simulation of

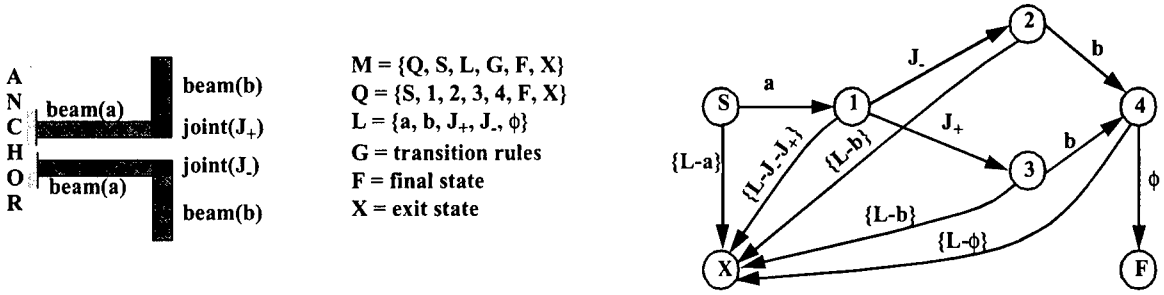
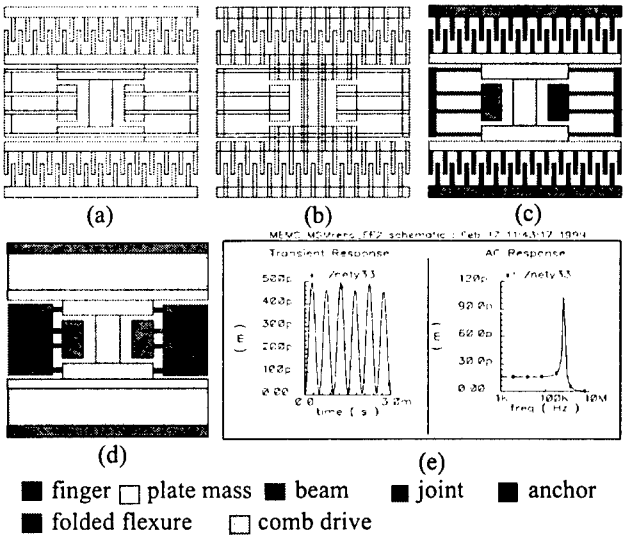


FIGURE 68. Finite State Machine to recognize a crab leg

FIGURE 69. Folded flexure resonator; (a) layout, (b) canonical representation, (c) recognized layout, (d) component extraction, (e) transient (1 KHz source) and ac (resonant frequency = 691.8 KHz) analysis of extracted netlist



a folded-flexure resonator is shown in Figure 69. A detailed report of these capabilities is available in the form of an M.S. thesis [37][74]. This milestone combined with increasing availability of test layouts from the inertial sensor designers allowed us to switch focus from the MUMPS process to the CMOS-MEMS process.

4.6.4 CMOS-MEMS Layout Extraction

The initial translation of the MUMPS extractor to CMOS-MEMS indicated that the increased data size in CMOS designs (each layout has more geometry to the multi-layer nature of CMOS microstructures) coupled with the $O(n^{1.5})$ runtimes of the algorithms in the prototype implementation resulted in exceedingly long run times. We detail the combined MEMS and electronics extraction flow, the improved scan-line based algorithms developed for faster extraction, and some

CMOS-MEMS extraction results.

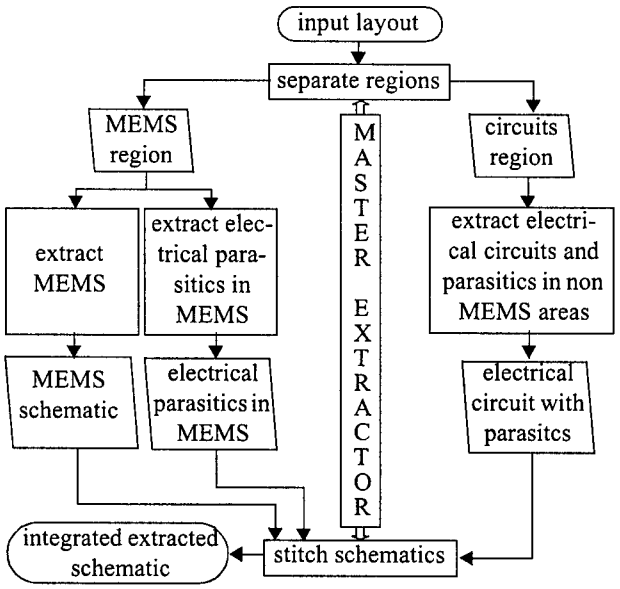


FIGURE 70. Overall extraction flow

CMOS-MEMS Extraction flow. The CMOS-MEMS extractor consists of a top-level master-extractor which uses two separate extractor modules to extract the MEMS and the electronics. Design rules for post-CMOS etching are used to determine the areas of the layout where the underlying silicon will be etched away to result in suspended MEMS areas. The on chip circuitry and the parasitics of the entire layout is extracted using commercial VLSI extraction tools. The information of etched silicon substrate is accounted accurately while extracting parasitic capacitances in the MEMS areas. The MEMS schematic is extracted from the layout using the MEMS-extractor. Finally, all the sub-schematics are 'stitched' together by the master-extractor to create the integrated schematic which can be simulated to verify the performance of the integrated microsystem. The overall extraction flow is shown in Figure 70.

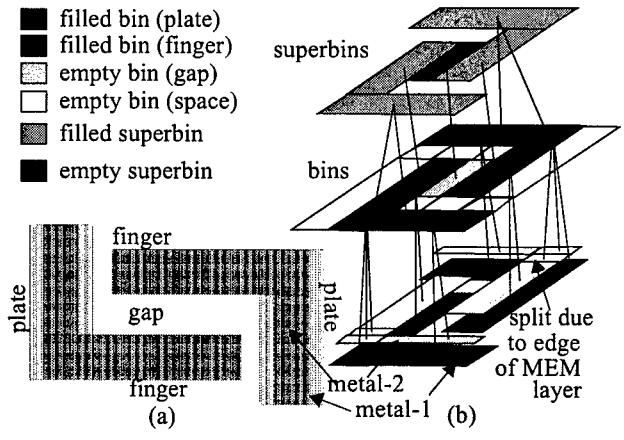


FIGURE 71. Hierarchical bin data structure; (a) example layout of two cantilever fingers made of metal-1 and metal-2; (b) its bin storage

MEMS extraction starts by the creation of the derived layers (*anchor* layer, *hole* layer, *gap* layer and the *structural* layer), using the layer definitions from the user. The *structural* layer is obtained by a geometric *or* of the topmost metal layer which defines the MEMS structure. The holes in the *structural* layer increases its complexity. A secondary layer (referred to as *MEM* layer) is derived from the *or* of the *structural* layer and the *hole* layer, thereby reducing the number of elements

needed to represent the layer. The extra area added thereby is annotated to the corresponding rectangle and is accurately reported in the final schematic. The *MEM* layer acts as the top level layer on which all the heuristics are applied to recognize the MEMS components. All the layers are stored in the canonical format explained in [20]. The canonical representations of the *MEM* layer and the gap layer are used to store the connectivity and structural information and are referred as bins in the hierarchical data structure used by the extractor (Figure 71). The structural layers are further split by the edges of the *MEM* layer so that each rectangle in the layer has an unique bin. This is followed by the atomic level recognition in which the filled bins (obtained from the *MEM* layer) are tagged with the atomic element type. The valid gaps are also recognized amongst the empty bins (obtained from the *gap* layer). Recognized bins of the same type are merged together to form the topmost storage level (referred to as superbins). Such a representation simplifies the heuristics and algorithms used for functional level recognition.

Scan-line Canonization. In order to simplify the recognition heuristics used during extraction, the geometrical information of the layout needs to be represented in an unique way irrespective of the designed geometry. We use a fully fractured representation, the *canonical representation*, which uses *minimum number of rectangles to cover the layout area such that each rectangle has at most one neighbor per edge and each edge is either fully covered by a neighbor or not covered at all.* The prototype implementation described here deal with Manhattan layouts only and can be extended to non-Manhattan geometry by replacing the rectangles by polygons.

Unlike the incremental algorithm used in [20], the new canonization routine uses scanline algorithm which relies on the sorting of outer edges of the input geometry. Our algorithm works in two phases. The initial *scan phase* creates the canonical set of rectangles by sweeping a vertical scanline in the horizontal direction across the layout geometry. Only vertical edges of the layout geometry are considered, thereby reducing the problem size by half. The horizontal sweep produces the canonized representation and also the horizontal neighbor information of its rectangles. The final *neighboring phase* is then used to create the vertical neighbor information.

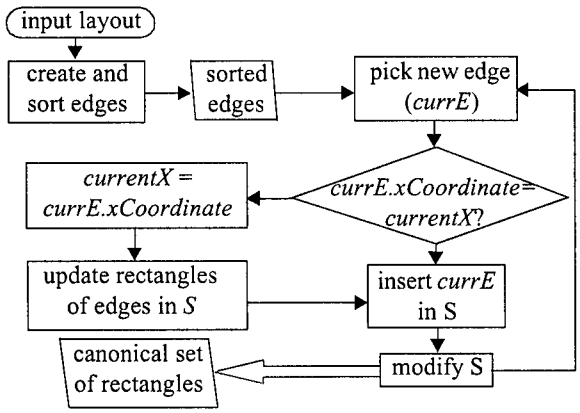


FIGURE 72. Flow diagram for the scanline-based canonization algorithm

The data structures used by the *scan phase* of the algorithm are a variable *currentX*, which stores the current position of the scanline, and the list of edges S in the scanline. The flow of the algorithm is shown in Figure 72. The direction of the edges is chosen such that while traversing along the edge in the given direction, the filled area of the geometry always lies to the left. The vertical edges are sorted first by their abscissa (x-coordinate), then by their ordinate (y-coordinate) and finally by their angle with the abscissa (90^o or 270^o from x-axis). Each edge is then sequentially inserted into the scanline and begins a new rectangle to its left. As the scanline moves, it drags the vertical edges in it, thereby extending the rectangles associated with those edges. When a new edge is inserted, it completes the rectangles associated with all the contiguous edges it can reach on the scanline, and starts new rectangles for those edges. If the end points of the new edge lie between any of these connected edges, the connected edge is split at that point. This split is propagated to the neighboring boxes on the left. If the scanline is maintained as a balanced binary tree, the insertion of each edge takes $O(\log m)$ time, where m is the current number of elements in S; and the connected edges can be found from the *predecessors* and *successors* of the inserted edge. The total number of such comparisons is equal to the number of rectangles in the final canonized representation (n), and the total time in insertion is $O(e \log m)$, where e is the initial number of vertical edges and m has an expected value of $O(\sqrt{n})$. If the edge inserted has a positive direction (angle = 90^o), then the edges of S overlapping with it are deleted from the scanline.

The algorithm is explained with the help of an example in Figure 73. Notice that when edge c is inserted (at *currentX* = 2), the rectangle A gets completed while rectangle B is not completed as edge a on S can be reached from c while edge b cannot be reached. Also when edge e is inserted (*currentX* = 4), the edge a, and the rectangles to its left, are split by the top of edge e. Note that the edge e is not split because

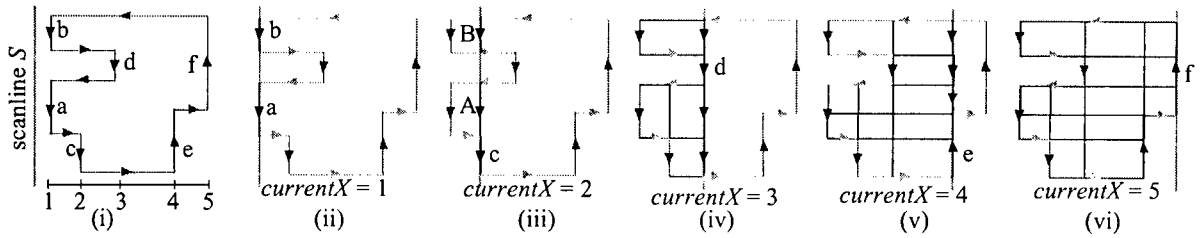


FIGURE 73. Example demonstrating the canonization procedure. The contents of scanline *S* and the state of the canonical set of rectangles are shown in consecutive figures are shown for each value of *currentX*

The *neighboring phase* sorts the canonized rectangles, first with their x-coordinate and then with their y-coordinate. It then checks whether the top edge of each rectangle coincides with the bottom edge of the next rectangle. If they coincide then they form a vertical neighbor couple and the information is entered. The inter-layer canonization and the binning algorithms follow a similar scanline approach where the edges of different layers are colored differently and the decision at every step uses the color of the edge along with its direction. Additional details are available in [65].

CMOS-MEMS Extraction Examples. The extraction tool is tightly integrated into the NODAS design methodology to form a complete integrated MEMS extraction environment, complete with user customization capabilities (similar to VLSI extraction flows). We show two examples to outline the capabilities of the extraction methodology: the first example (an accelerometer) shows how integrated simulation leads to better designs. The second example (a filter) shows a comparative study between the results from designed schematic, extracted schematic and experimental data.

- **Accelerometer**: Consider the CMOS-MEMS y-accelerometer [48] with an on-chip capacitive sensing interface. The initial design uses a differential comb drive on each side of the accelerometer as the electromechanical transducer (Figure 74(a)). When the integrated schematic was simulated, a cross axis signal was observed (experiment 1 of Table 6). This can be explained from the dc voltage on the sense fingers of the comb drives, resulting from the sense circuit's operating point, which results in an unbalanced moment. This moment leads to a dc displacement in the x and y directions and in turn causes the cross axis coupling. To verify this effect, the MEMS schematic (without the circuit) was simulated with different dc voltages on the sense fingers. The results plotted in Figure 74(c) show the effect of a dc voltage on the sense finger. The dependence on the dc voltage can be removed if the common centroid topology (shown in Figure 74(b)) is used. Such an arrangement leads to complete balancing of the forces and the

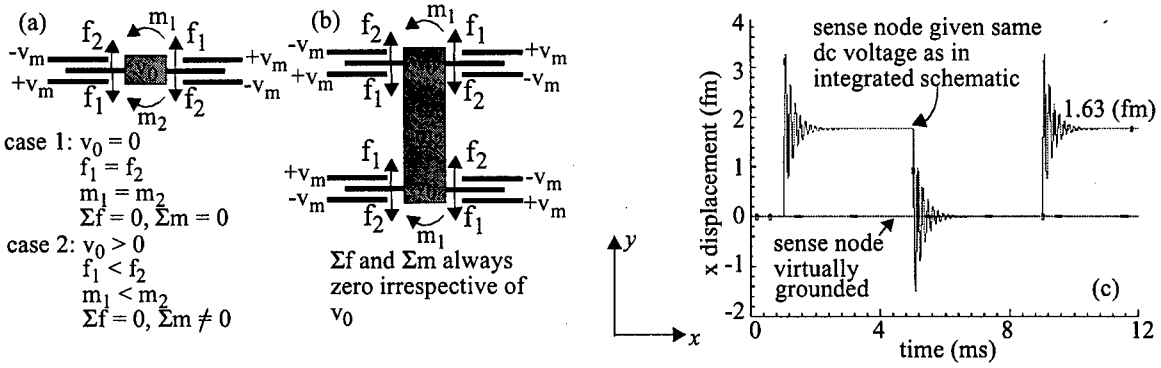


FIGURE 74. (a) Symbolic picture of a rotor (center) with differential comb drive showing all the forces and moments due to a dc voltage on the sense finger, (b) arrangement of four comb drives to remove moment due to dc voltage, (c) cross axis displacement for 1g input pulse with and without dc voltage at the sense node of the MEMS schematic in (a)

Table 6: Results for accelerometer when a 1g input pulse acceleration was applied in y direction (D_{ma} stands for MEMS designed schematic with single comb drive, D_{mb} stands for common centroid MEMS schematic, D_{ca} stands for designed schematic for circuit, E_{ca} stands for extracted schematic for layout using metal2 for wiring sense comb, E_{cb} stands for extracted schematic for layout using metal1 layer for wiring, E_{ma} stands for extracted schematic for the MEMS part of device

Experi-ment	Circuit	MEMS	x dis-placement (fm)	y dis-placement (nm)	o/p of sense circuit (mV)
1	D_{ca}	D_{ma}	1.63	5.37	4.44
2	D_{ca}	D_{mb}	0	5.37	4.44
3	E_{ca}	E_{ma}	47.82	5.03	4.12
4	E_{cb}	E_{ma}	47.82	5.03	4.16
5	D_{ca}	E_{ma}	47.82	5.03	4.16

moments thus eliminating cross coupling (experiment 2 in Table 6).

The layout of the common centroid accelerometer (with integrated electronics) is shown in Figure 75(a), with the extracted MEMS schematic in Figure 75(b). Comparison between the results of designed and extracted schematics (experiments 2 and 3) show a 6.3% degradation in y displacement and 7.2% degradation in the output. This is in accordance to the sensitivity equations for the accelerometer, which are given by $V_0/a = (2C_0 m V_m)/(k g_0 (2C_0 + C_p))$ and $y/a = k/m$ where, V_0 is the output voltage, a is the input acceleration, C_0 is the initial capacitance between fingers, m is the effective mass, V_m is the applied bias, C_p is the parasitic capacitance, k is the spring constant, g_0 is the initial inter-finger gap and y is the displacement in y. The extracted schematic captures the actual metal1 and metal2 areas used for signal routing in the plate, leading to as smaller mass (m) than in the designed schematic. The parasitic joints (identified by the

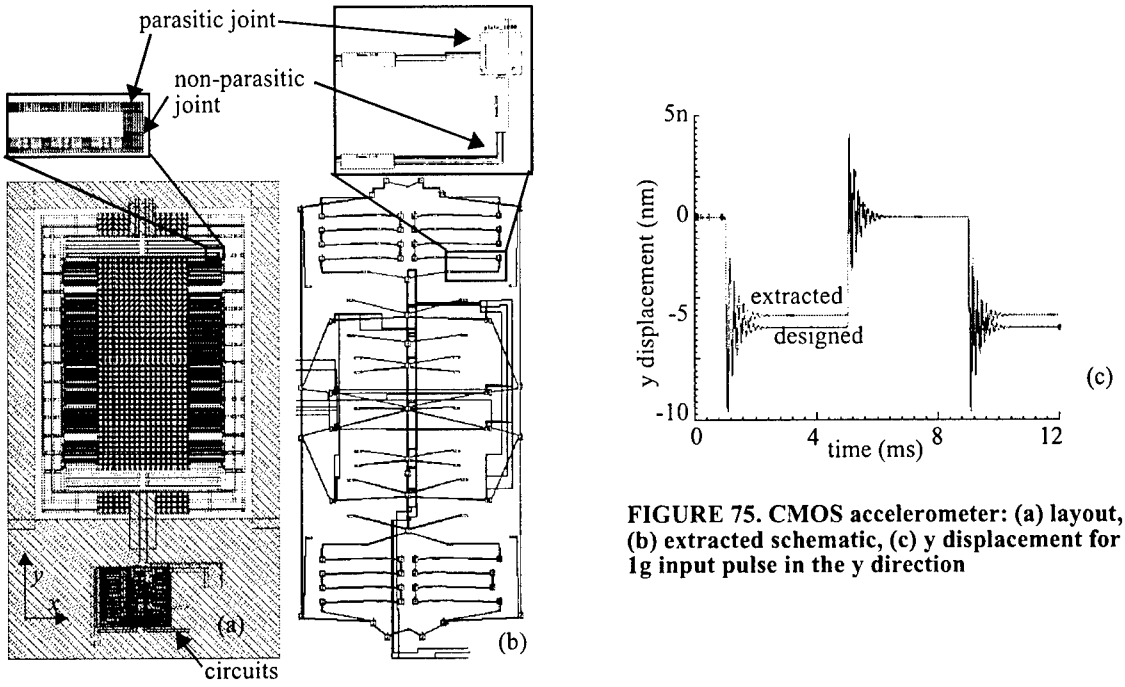


FIGURE 75. CMOS accelerometer: (a) layout, (b) extracted schematic, (c) y displacement for 1g input pulse in the y direction

extractor) in the springs lead to a smaller spring constant (k) in the extracted schematic, as compared to the design schematic. The additional degradation in the transducer output was due to the parasitic capacitance originating primarily from the routing for the sense finger of the comb drives which was done using metal2. To reduce this parasitic capacitance, the layout was regenerated using metal1 as the routing layer (since metal1 is further away from top most metal layer which is grounded); and the results are shown in experiment 4 of Table 6. The parasitic capacitance is negligible in this case which is highlighted in experiment 5 where the extracted MEMS schematic was simulated with the circuit schematic without the parasitic capacitances.

This example demonstrates the capability of the integrated simulation methodology in capturing the mutual interaction of the mechanical, electromechanical and electronic domains in an integrated device and also shows the usefulness of the extractor in capturing the various parasitics.

- **Filter** Figure 76 (a) shows an SEM of a CMOS-MEMS bandpass filter [49] with an on-chip electrical interface. The frequency responses of the extracted schematic (Figure 76(b)) and the designed schematic are shown in Figure 76(c) together with the experimental data [49]. Table 7 shows the details of the simulation results for the first resonant peak. The additional routing mass resulted in a decrease in the resonant frequencies by 2% while increasing the overall dis-

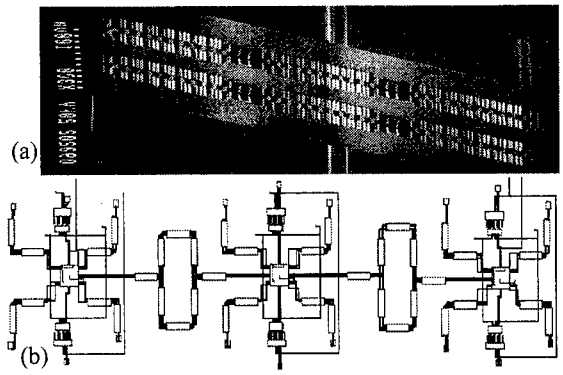


FIGURE 76. (a) SEM of the filter, (b) extracted schematic, (c) comparison of results

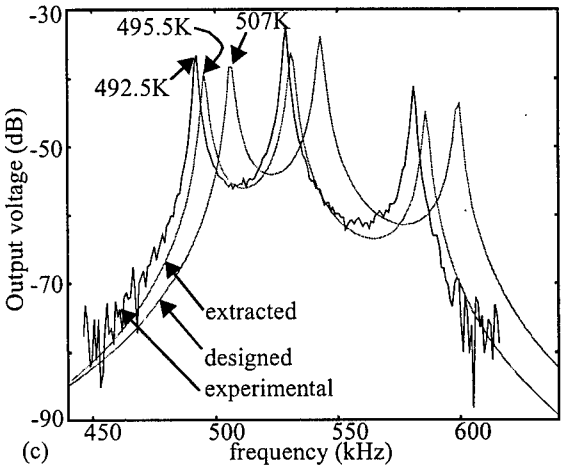


Table 7: Comparison of data for the first resonant peak in the band pass filter for the designed and extracted schematics (ac i/p 1V, bias ±20V)

	o/p voltage (mV)	transducer o/p (mV)	displacement (nm)	resonant frequency (kHz)
designed	12.86	86.24	32.09	507
extracted	10.88	72.98	36.74	495.5

placement at the resonant peaks by the same factor. However the effect of parasitic capacitance at the sense comb drive dominates and results in an overall degradation of the output by 15.4%.

Summary. Integrated simulation is essential to capture the true behavior of a device containing MEMS and electronics. Such a simulation can only be performed at the schematic level. This paper introduces the concept of mechanical parasitics that are needed in addition to electrical parasitics in order to accurately represent the device layout as a schematic. The extractor developed in this project uses a Layout Parasitic Extraction (LPE) file to automatically generate an integrated schematic representation from the layout [70]. Examples showing how the extractor can be used to identify and minimize the impact of deleterious parasitics demonstrate its potential impact in any integrated MEMS design flows of interest to the DoD.

4.7 Fault Models

Robust manufacturing test techniques for MEMS are required to ensure high-quality devices can be produced in a cost-effective manner. Developing effective test methods requires an understanding of the failure mechanisms that are unique to MEMS. Focusing on the surface-micromachining techniques utilized in our program, we developed a software flow called CARAMEL.

CARAMEL uses process simulation, finite-element mesh generation and behavioral simulation to analyze the impact of foreign particles introduced into the manufacturing process on both MEMS structure and behavior [2][34][40][43]. Case studies of beam, plate, anchor, and other primitive MEMS elements led to models of failure for common mechanical structures such as resonators and accelerometers [8][21][56][73]. CARAMEL has also been combined with our synthesis capabilities to develop design flows that create MEMS layout that is less susceptible to manufacturing defects resulting from particles [31][72]. The scope of our analysis expanded to include failures resulting from stiction [22], residual stress, fabrication variations, and combinations thereof. Analysis of multiple failure sources revealed that potentially harmful defects can go undiscovered if typical testing techniques are employed [61]. To address this problem, we are now developing built-in self-test design techniques that allow these defects to be easily detected by the MEMS itself.

4.7.1 CARAMEL

CARAMEL (Contamination And Reliability Analysis of Microelectromechanical Layout) is the first automated tool available for contamination analysis of MEMS layouts. CARAMEL is based on the IC contamination analysis tool CODEF and is capable of analyzing the impact of contamination particles on the geometrical and material properties of microelectromechanical systems. CARAMEL requires a MEMS layout, a process recipe, and contamination information and generates as output a mechanical mesh that captures the impact of the contamination. Output generated by CARAMEL indicates that a wide range of defective structures are possible due to the presence of particulate contaminations. The three parts of CARAMEL are shown in Figure 77:

Process Simulation: We use the CODEF process simulator (previously developed at Carnegie Mellon) to map process contaminations into defects. The CODEF process simulator has been made more amenable to MEMS analysis by extending it to include the complete MUMPS process flow.

Structure Extraction: Our modified version of CODEF creates a three-dimensional representation of defective MEMS structures. A meshing capability to the tool to generate ABAQUS compatible meshes for subsequent mechanical simulation was developed in 1998. An electrical analysis capability within HSPICE was added in 1999. ABAQUS is used to simulate the resulting mesh to determine the mechanical misbehaviors resulting from contaminations. Hspice models of the defec-

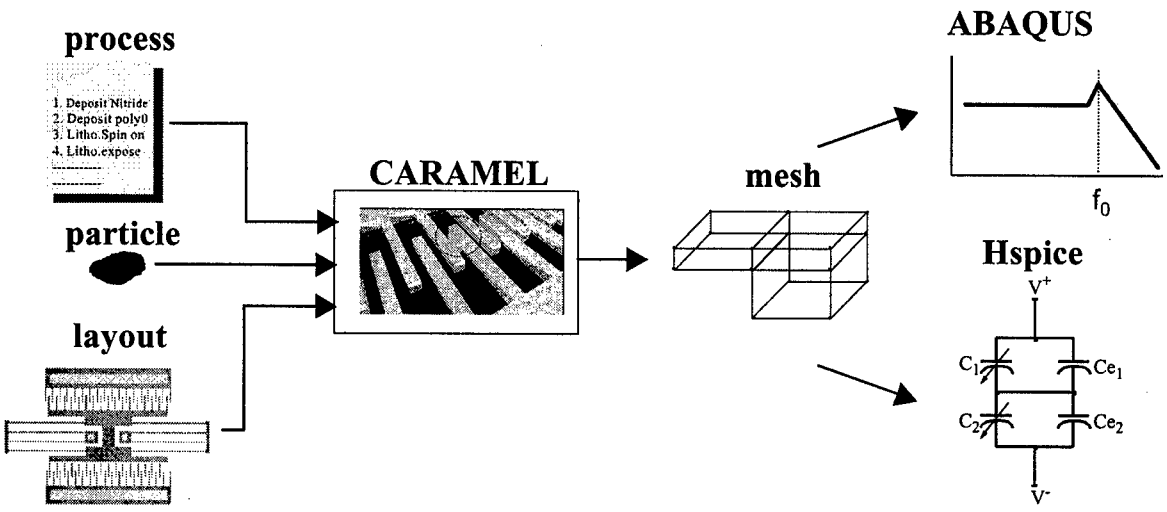


FIGURE 77. CARAMEL analysis flow for MEMS fault modeling.

tive structures are then (manually) created and simulated to determine the resulting electrical misbehaviors.

Parameter Analysis: This final sub-task performs systematic fault categorization in order to identify various fault classes. Categorization will be based on the results of mechanical simulations, *i.e.*, deviations of the mechanical parameters (like resonant frequency, stiffness, *etc.*) from the desired nominal values.

4.7.2 Classification of Mechanical Misbehaviors

Monte Carlo use of CARAMEL has produced the full spectrum of defective structures caused by particle contaminants. These results are used to perform defect classification according to the geometrical features of the defective structures. The identified defect types fall into three categories: surface, anchor and broken structure, each of which can be further divided into a number of sub-defect categories dependent upon the exact particle and/or defective structure location. Figure 78 shows representative examples of these defect classes.

The relative probability of occurrence (RPO) of each defect type was extracted from the process simulation results and compared with theoretical calculations. RPO is a probability that estimates the likelihood of a particular defect type given the presence of a single contamination. We

(a) (b) (c)

FIGURE 78. Representative examples of the defect categories caused by particles: (a) Surface protrusion located on the shuttle, (b) surface finger protrusion that welds two adjacent fingers, (c) lateral finger protrusion that reduces finger gap in the overlap region.

also have classified all the process steps involved with manufacturing the microresonator as either resistant or vulnerable to the particle contaminants.

CARAMEL was used to perform 721 unique contamination simulations of the surface micromachined comb-drive resonator. We analyzed contaminations of various sizes and material properties. In addition, contaminations were placed at many different resonator locations and were introduced at many different steps of the MUMPs process. Out of 721 contaminations, 263 were physically in contact with the resonator structure. The effect of each of these 263 contaminations was observed at each phase of CARAMEL's operation. The mechanical simulator ABAQUS was also used to compute the resonant frequency of each of the mechanical meshes generated by CARAMEL. The resonant frequency was analyzed because it is one of the crucial parameters for determining if the resonator is functioning properly. The results obtained were classified under three broad fault classes: *catastrophic*, *parametric*, and *harmless*. The defect statistics generated by CARAMEL indicates the comb drive as the most defect-prone region of the microresonator. Most of the comb drive defects resulted in the catastrophic failures. Contaminations introduced during Poly0 deposition caused the maximum number of faults found in the microresonator. Such defect-to-fault mappings provide an essential tool for the MEMS fault model generation process. Simulation results presented in A. Kolpekwar's M.S. thesis [13] confirm that CARAMEL can be used as an effective tool for development of realistic fault models for MEMS.

4.7.3 Classification of electromechanical misbehaviors

Four thousand CARAMEL runs were performed resulting in 492 defective structures. Analysis of the results have led to several preliminary classes for mechanical and electrical faults. Each class has an associated misbehavior (deviation of sensing voltage, resonant frequency, etc.) and rel-

ative probability of occurrence.

Our latest results have identified a new defect type termed a *crossing lateral protrusion*. A crossing lateral protrusion is a particle-induced protrusion of unwanted material that is located across the overlap and non-overlap region of two adjacent fingers. This unlikely defect has two major effects on behavior: it introduces a significant offset to the final output sensing voltage and changes the sensitivity of the device. Our assumptions on possible protrusion size and location revealed that device sensitivity can increase as much as 92% from the presence of this kind of defect.

Mechanical and electrical analysis were performed to evaluate the misbehaviors of the defective structures. In mechanical simulation, we applied an inertial force, and measured the displacement of the microresonator under this force. In electrical simulation, we measured the output sensing voltage from the differential capacitive-sensing model formed by the microresonator. Our results show that defects cause a range of misbehaviors. Based on the amount of deviation measured value the nominal, we have categorized defects as either catastrophic (deviation > 30%), parametric (5% ≤ deviation ≤ 30%) and harmless (deviation < 5%) based on displacement and sensing voltage. An important result discovered is that some defect types (those that affect finger gap) virtually have no impact on displacement, but dramatically affect sensing voltage.

4.7.4 Summary

Commercial MEMS are affected by multiple failure sources acting simultaneously, requiring an understanding of the interactions among failure sources. We have demonstrated that MEMS behavior/misbehavior is very similar to that of analog and digital electronics as MEMS exhibit behavior overlap, dominance, construction and masking and that a single specification-based test is insufficient for diagnosis of all failure sources. During the reporting period, the effect of failure sources, namely, etch variation and particulates, on the surface micromachined MUMPS folded-flexure resonator and accelerometer were analyzed. Behavior construction is the mutual reinforcement of the (mis)behavior due to two or more defects. Behavior masking is the opposite case where the (mis)behavior due to one defect is neutralized partially or totally by that of another defect. For each device there is behavior construction between particulates and under-etch. Also, for both devices there is behavior masking between particulates and over-etch. For the accelerometer, the

behavior of one type of beam defect was shown to dominate one type of finger defect. It was shown that besides resonant frequency test, other performance specifications such as sensitivity have to be included for failure diagnosis and calibration.

5. Conclusions

The primary conclusion of this work is that it is possible to integrate a full 6-DOF IMU in conventional CMOS using post-CMOS micromachining. The low cost of the CMOS and the MEMS processing makes this possibility very attractive. The accelerometers and gyroscopes designed in the thin-film CMOS-MEMS process have a current measured best performance of $100\ \mu g/\sqrt{Hz}$ and $0.03°/s/\sqrt{Hz}$ respectively. This performance provides capability for head tracking and perhaps some GPS-aided land navigation applications. The noise performance is found to be limited by flicker noise in the CMOS interface circuits, not by the micromechanical noise. Design of circuits to operate at well over 1 MHz modulation frequencies is necessary to ensure that flicker noise is reduced below thermal noise.

The DRIE Si CMOS-MEMS process provides larger proof masses that can lead to better performing IMU components. However, the interface circuits must be improved to take advantage of the increased proof mass.

The designs in this project were developed with tools that support schematic construction, simulation and layout extraction. The use of these tools encodes the design information into a reusable form. This design information can help improve future designs, or can be assembled into larger integrated systems. Without these CAD tools, such reuse and levels of integration would not be possible.

6. Recommendations

Further development of IMU's using the post-CMOS micromachining processes should proceed. Better interface circuits that eliminate the flicker noise limitation are required and should be designed. More complete characterization of individual inertial components should be undertaken. This characterization should include studies of drift, nonlinearities, high-G performance, and cross-axis sensitivity. DRIE Si CMOS-MEMS inertial devices have the potential for low-cost navigation-

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