International Technology Research Institute
Technology Transfer (TTEC) Division

TTEC Panel Report on

High-Temperature Electronics in Europe

Vladimir Dmitriev (Chair)
T. Paul Chow
Steven P. DenBaars
Michael S. Shur
Michael G. Spencer
George White

August 2000

International Technology Research Institute
R.D. Shelton, Director
J. Brad Mooney Jr., TTEC Director

4501 North Charles Street
Baltimore, Maryland 21210-2699

TTEC PANEL ON HIGH-TEMPERATURE ELECTRONICS IN EUROPE

Sponsored by the Office of Naval Research and the National Science Foundation of the United States government.

Vladimir Dmitriev
TDI, Inc.
8660 Dakota Drive
Gaithersburg, MD 20877

Steven P. DenBaars
Materials Department
University of California
Santa Barbara, CA 93106

Michael G. Spencer
418 Phillips Hall
Cornell University
Ithaca, NY 14850

T. Paul Chow
ECSE Department
Rensselaer Polytechnic Institute
Troy, NY 12180-3590

Michael S. Shur
CIEEM CII Room 9017
Rensselaer Polytechnic Institute
Troy, NY 12180-3590

George White
Packaging Research Center
Georgia Institute of Technology
813 Ferst Drive NW
Atlanta, GA 30332-0560

INTERNATIONAL TECHNOLOGY RESEARCH INSTITUTE
Technology Transfer (TTEC) Division

The Technology Transfer (TTEC) Division at Loyola College's International Technology Research Institute (ITRI) provides assessments of foreign research and development in selected technologies. Dr. R.D. Shelton is Director of ITRI. Support is provided by a variety of U.S. government agencies, including ONR, DoC, and NSF.

ITRI's mission is two-pronged: (1) to inform U.S. policymakers, strategic planners, and managers of the state of selected technologies in foreign countries in comparison to the United States; and (2) to identify opportunities for international cooperation among countries and collaboration among researchers. ITRI assessments cover basic research, advanced development, and applications. Panels of typically six technical experts conduct these assessments. Panelists are leading authorities in their fields, technically active, and knowledgeable about U.S. and foreign research programs. As part of the assessment process, panels visit and carry out extensive discussions with foreign scientists and engineers in their labs.

The ITRI staff at Loyola College helps select topics, recruits expert panelists, arranges study visits to foreign laboratories, organizes workshop presentations, and finally, edits and disseminates the final reports.

Dr. R.D. Shelton
ITRI Director
Loyola College
Baltimore, MD 21210

RADM J. Brad Mooney Jr., USN (Ret.)
TTEC Director
2111 Jeff Davis Hwy.
Arlington, VA 22202

Dr. George Gamota
ITRI Associate Director
17 Solomon Pierce Road
Lexington, MA 02173

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Vladimir Dmitriev (Chair)
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ABSTRACT

This final report of ITRI's panel on high-temperature electronics in Europe consists of an executive summary, an introductory chapter, and six chapters by panel members on various aspects of wide bandgap electronics. The report also contains site reports for the various companies, labs, universities, and government offices that the panel visited in Europe. Comparisons are made between developments in Europe and the United States. Principal findings include: • European scientists and engineers see optoelectronics and high-power, high-frequency electronics as the major application opportunities for wide bandgap semiconductors. • The size of the GaN and SiC technology and device development effort in Europe is comparable with that in the United Statews. • Europe is ahead of the U.S. in in bulk GaN growth technology. • The United States is currently ahead in GaN-based device developments for light emitters, and high-power/high-frequency applications. • In silicon carbide technology, the U.S. is ahead in SiC bulk crystal and epitaxial production. • In R&D silicon carbide effort, European organization both academic and industrial have recently demonstrated outstanding results in both material growth (bulk and epi) and device development proving the leading position in the world; in the area of SiC power switching devices Europe is leading in both R&D and pre-production activity. • Strength of European approach is in the powerful combination of national and international projects both R&D and product oriented.

International Technology Research Institute (ITRI)

R.D. Shelton, Principal Investigator, ITRI Director
George Mackiw, Deputy ITRI Director
George Gamota, ITRI Associate Director

Technology Transfer (TTEC) Division

J. Brad Mooney Jr., Division Director
Bobby A. Williams, Head, TTEC Studies (to 12/99)
Stephen Gould, Head, TTEC Studies Section
Elliot King, Head, Education Section

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EXECUTIVE SUMMARY

INTRODUCTION

Wide bandgap semiconductors (SiC, GaN, AlN) have great potential for high-temperature, high-power, high-frequency electronics, and for short-wavelength optoelectronics. Now, the rapid progress of the last few years in SiC and group III nitrides technology and device development is providing us with unique opportunities for development of the next generation of semiconductor electronics—semiconductor electronics for the 21st century.

In 1999, the U.S. National Science Foundation and the Office of Naval Research assembled a panel on "High-Temperature Electronics" to evaluate and compare the status, trends, and perspectives of wide bandgap semiconductor electronics in the U.S. and Europe, with particular emphasis on Europe. This panel was composed of individuals representing industry, academia and government organizations: Prof. T.P. Chow, Rensselaer Polytechnic Institute; Prof. S.P. DenBaars, University of California at Santa Barbara; Dr. V.A. Dmitriev, TDI, Inc. (Panel Chair); Prof. M.S. Shur, Rensselaer Polytechnic Institute; Prof. M.G. Spencer, Cornell University; and Dr. G. White, Georgia Institute of Technology. Accompanying and working with the panel during its site visits in Japan were Dr. U. Varshney of the National Science Foundation and Dr. J. Zavada of the European Research Office. This study was a continuation of the "High Temperature Electronic in Japan" study, which was managed by ITRI in 1998.[1]

In its investigation, the panel focused on the following topical areas:

- basic research on wide bandgap semiconductors (SiC and Group III nitrides)
- bulk crystal growth of wide bandgap semiconductors
- epitaxial growth of wide bandgap semiconductors
- post growth technology for device fabrication (etching, metallization, edge termination, and passivation)
- packaging technology for high-temperature/high-power/high frequency applications
- design of high-temperature devices on SiC and group III nitrides
- applications and markets of high-temperature/high-power/high frequency electronics

In June 1999, as part of this study, panelists traveled to Europe where they visited companies, universities, and government research institutes at 11 sites. The organizations visited were chosen because they have established leadership roles in important aspects of wide bandgap semiconductor research and development. All of them have significant efforts, either in the field of SiC or in group III nitride materials and devices - some in both.

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[1] TTEC Panel Report on High-Temperature Electronics in Japan, International Technology Research Institute, Loyola College, 1999.

Results of the study have been reported and discussed at the 1999 Fall Material Research Society Meeting in Boston and The US-Europe Conference on Wide Bandgap Semiconductor Technology for Next Generation Electronic and Photonic Devices.

This report is based on: the panel's observations during site visits in Europe; discussions with our hosts and colleagues in the Europe companies, universities, and government laboratories visited; and on published literature that details recent work in Europe and United States.

PRINCIPAL CONCLUSIONS

There is a strong interest in both the United States and Europe in advanced electronics based on wide bandgap semiconductors. European countries most active in the field are Germany, Sweden, and France. The European Union has recently initiated a few R&D programs in this area, including projects on silicon carbide and gallium nitride crystal growth and device fabrication.

Other major conclusions include:

European scientists and engineers see optoelectronics and high-power, high-frequency electronics as the major application opportunities for wide bandgap semiconductors. In Europe, high-temperature electronics is not considered a major applications field.

- **The size of the GaN and SiC technology and device development effort in Europe is comparable with that in the United States.**

- **Europe is ahead of the U.S. in bulk GaN growth technology and related homoepitaxial technology.**

- **The United States is currently ahead of Europe in GaN-based device developments for light emitters, and high-power/high-frequency applications**. *However*, the strong GaN R&D effort that is rapidly progressing in Europe will provide a foundation that will help enable both photonic and electronic markets. The earlier assessment concluded that Japan lead the U.S. in this field.

- **In silicon carbide technology, the U.S. is ahead in SiC bulk crystal and epitaxial production.** Excellent bulk growth research is being done in Europe, but at present there is no 3-inch commercial product and no semi-insulating wafers.

- **In silicon carbide R&D**, European organizations both academic and industrial have recently demonstrated outstanding results in both material growth (bulk and epi) and device development proving their leading position in the world. In the area of SiC power switching devices, Europe is leading in both R&D and pre-production activity.

- **Strength of European approach** is in the powerful combination of national and international projects both R&D and product oriented. These projects are usually coordinated by one or a few industrial organizations highly motivated by new product development. They involve a number of leading research teams from academia and are funded by a national government or European Union. A number of such projects involve research teams from Eastern Europe having unique experience in R&D work in the field of wide band gap semiconductors.

The conclusions of the panel and of this report are summarized in Table 1, in which SiC and GaN-based R&D and production activities of Europe and the United States are compared.

Table ES.1

SiC and GaN-based Technology and Devices.
Europe (All Countries) Compared to United States

		Research and Development		Production	
		Status	Trend	Status	Trend
Bulk Materials	SiC	+	↑	-	↑
	GaN	+	→	NA	NA
Epitaxy	SiC	+	→	-	→
	GaN	-	↑	0	↑
Process Technology	SiC	+	↗	0	↗
	GaN	0	↗	-	↑
Electronic Devices					
Microwave Devices	SiC	-	↑	-	↗
	GaN	-	↑	-	↑
Power Switching	SiC	+	↗	+	↗
Optoelectronic Devices	GaN	-	↗	0	↗
Applications					
Microwave Devices		0	↑	-	↗
Power Devices		+	↗	+	↗
High temperature Sensors		+	↑	0	↑
High Temperature Packaging		0	↗	0	→
Infrastructure		+	↗	+	↗

+	**Europe ahead**	↑	**Europe gaining ground**
0	**About even**	→	**Progressing equally**
-	**Europe now behind**	↓	**Europe losing ground**

CHAPTER 1

INTRODUCTION

Vladimir A. Dmitriev

GOALS OF THE STUDY

In 1999, U.S. Government agencies requested the International Technology Research Institute (ITRI) to assess the state of high-temperature electronics basic research, development, manufacturing, and applications in Europe compared to that in the United States. A similar study was conducted in 1998 examining the status of high temperature electronics in Japan and the USA. ITRI assembled the High-Temperature Electronic (HTE) Panel to conduct a study on silicon carbide (SiC) and gallium nitride (GaN) R&D and production activities in Europe. The study was focused on the following topical areas:

- basic study of wide band gap semiconductors (SiC and group III nitrides);
- bulk crystal growth of wide band gap semiconductors;
- epitaxial growth of wide band gap semiconductors for device structures;
- post growth technology for device fabrication (etching, metallization, edge termination, and passivation);
- packaging technology for high temperature applications;
- design of high temperature devices on SiC and group III nitrides;
- applications and market for high temperature electronic devices.

THE STUDY PANEL

Six experts served as panel members for this study. (Short biographies are in Appendix A). Coming from both academia and industry, they reflect the diversity of professional backgrounds currently contributing to the advancement of wide band gap semiconductor electronics in the United States.

- Vladimir A. Dmitriev (Panel Chairman), President, TDI, Inc. Expertise: wide band gap semiconductor epitaxial growth and device development.
- T. Paul Chow, Associate Professor, Rensselaer Polytechnic Institute. Expertise: power semiconductor devices.
- Steven P. DenBaars, Associate Professor, University of California at Santa Barbara. Expertise: growth and characterization of wide band gap semiconductors and device structures.

- Michael S. Shur, Patricia W. and C. Sheldon Roberts '48 Professor, Rensselaer Polytechnic Institute. Expertise: solid state device physics.

- Michael G. Spencer, Cornell University. Expertise: epitaxial and bulk growth of wide band gap semiconductors.

- George White, Georgia Institute of Technology. Expertise: electronic device packaging.

The panelists were accompanied on site visits to European organizations by the following representatives from the sponsoring organizations (Appendix A):

- Usha Varshney, Program Director, National Science Foundation.

- John Zavada, European Research Office.

APPROACH

Panelists and government sponsors prepared a list of organizations that have established leadership in some important aspects of high temperature electronics and wide band gap electronics in Europe. ITRI then contacted these organizations with letters of introduction from individual panelists to determine if they were willing to host a visit by the panel.

Before the trip, panel members collected information on recent achievements in high temperature electronics and wide band gap electronics in the United States. To provide some reciprosity, panel members gave presentations during site visits reviewing the status of high-temperature electronics in the USA.

Site visits took place from June 6 to June 12, 1999. Members of the panel arrived in Europe and had a planning meeting on Sunday 6 in Grenoble. On June 7, the panel had a meeting with leading French scientists from different organizations working on wide band gap semiconductors. This full-day meeting organized at CEA LETI gave the panel members an opportunity to obtain very helpful information on wide band gap electronics R&D in France. For the following site visits, the panel was divided in two teams. The visit schedule is shown in Table 1. On Friday June 11, both teams had joint meetings at Stockholm, visiting ABB, IMC, and RIT. On Saturday morning, June 12, we had a debriefing meeting at Stockholm to compare notes and come to some conclusions.

While the site visit format varied from site to site, mostly they had the following format:

1. Introduction of participants and a brief discussion of the visit. At some sites, panel members gave short background presentations on the status of wide band gap electronics in the United States. These presentations lasted 40 – 60 minutes.

2. Presentation of the organization's background and technical objectives in the wide band gap semiconductor field; some of these presentations gave details such as company size, income, research and production goals.

3. Discussion, extended question and answer period. These discussions, which typically lasted between two and four hours, were based on a detailed questionnaire sent earlier to the organizations. The panel did not ask organizations to answer every question on the questionnaire, but rather to focus on those issues most relevant to their own work. Before or after discussion, some host organizations provided laboratory or plant tours.

For each site visited, one attending panelist or other traveling team member had the task of writing a detailed site report. Each draft site report was circulated to other members of the site visit team, who drew from their own notes to make additions to or deletions from the draft to ensure accuracy and completeness. ITRI then submitted each draft site report to the host organization for its own editing of the contents to ensure that the report is accurate and does not inadvertently compromise proprietary information.

The results of the study were reported at the 1999 Fall MRS Meeting in Boston on December 1, 1999. A special session devoted to the panel report was organized by Michael Shur and Randall Feenstra (co-chair of the MRS Symposium "GaN and Related Alloys") and chaired by Vladimir Dmitriev. At the session, John Zolper (ONR) and John Zavada (European Research Office) shared with the participants their views on the future of high-temperature electronics. Professor Sylwester Porowski (HPRC) gave an overview of bulk GaN effort in Europe.

Table 1.1

Site Visit Schedule in Europe

	Team A	**Team B**
	S. DenBaars	V. Dmitriev
	M. Shur	P. Chow
	G. White	M. Spencer
	J. Zavada	
	U. Varshney	
June 6	Panel business meeting, Grenoble, France	
June 7	CEA LETI, Grenoble, France	
June 8	University of Ulm	Siemens (Erlangen)
June 9	Siemens (Munich)	University of Erlangen
June 10	HPRC, Warsaw	University of Linkoping
June 11	IMC/ABB/RIT, Stockholm, Sweden	
June 12	Panel business meeting, Stockholm, Sweden	

THE US-EUROPE CONFERENCE

It is ITRI's practice to hold workshops in the Washington, DC area to present the findings of its panels. For this study, it was decided to organize a US-Europe Conference on **Wide Bandgap Semiconductor Technology for Next Generation Electronic and Photonic Devices**. Leading European scientists and engineers were invited to report the latest results in the field. The conference was held in Arlington, Virginia on December 9 – 10, 1999. The following reports were presented at the conference on December 9:

1. Michael G. Spencer, Cornell University, SiC growth and processing technology
2. Vladimir Dmitriev, TDI, Inc., Progress and issues in SiC technology
3. T. Paul Chow, Rensselaer Polytechnic Institute, High voltage SiC power switching devices
4. Heinz Lendenmann, ABB Corporate Research, Application and operation of high voltage, high current SiIGBT / SiC diode modules
5. Steven DenBaars, University of California, Santa Barbara, GaN-based materials research in Europe

6. Sylwester Porowski, High Pressure Research Center, PAS, Application of pressure grown GaN substrates to epitaxy
7. Michael Shur, Rensselaer Polytechnic Institute, GaN-based electronic device research in Europe
8. Christian Brylinski, Thomson CSF, Wide bandgap microwave power devices
9. George White, Georgia Institute of Technology, High temperature electronic packaging in Europe
10. Roumen Kakanakov, Institute of Applied Physics, BAS, Ohmic contacts and packaging for wide bandgap semiconductors

On December 10, there was a general discussion on different aspects of wide band gap electronics. The following reports were presented after the discussion:

1. NSF programs (U. Varshney)
2. ONR programs (I. Mack)
3. DARPA programs (E. Martinez)

More than 100 experts in the field of wide band gap semiconductors attended the conference. Viewgraphs presented at the conference are available on the ITRI Web site (http://itri.loyola.edu/ttec/).

OVERVIEW OF THE REPORT

This written report is the final evaluation of the panel on the current status of silicon carbide and gallium nitride electronics in Europe and the United States. It consists of six chapters devoted to specific aspects of wide band gap electronics written by panel members and site reports. Brief biographies of panel members are given in Appendix A.

CHAPTER 2

STATUS OF SiC TECHNOLOGY: BULK AND EPITAXIAL GROWTH

Vladimir A. Dmitriev

INTRODUCTION

Recent progress in silicon carbide (SiC) technology may be illustrated by Fig. 2.1 showing data on blocking voltage of SiC devices vs. device area reported in the year 1996 and in the year 1999 [Syrkin and Dmitriev 1999]. It is clear that in a few last years both device size and blocking voltage of SiC devices have been increased. This progress is based on significant material quality improvement, which has been achieved for both substrate and epitaxial materials. However, to realize the full potential of SiC for high-power devices many existing technological issues must be solved. This paper reviews the status of SiC technology for bulk and epitaxial growth. We do not describe technological processes, but focus on recent findings, which have been reported in 1998 – 1999. A detailed review on SiC growth technology has been published recently [Dmitriev and Spencer 1998].

BULK SIC GROWTH

The accepted technology for bulk SiC crystal growth is physical vapor transport (PVT). This method, also known as modified Lely method, seeded sublimation growth, Tairov-Tsvetkov method, has been described in details elsewhere (Tairov and Tsvetkov 1981, Dmitriev and Spencer 1998). In this section we review two main issues in PVT SiC technology, crystal size and defects in bulk SiC crystals.

Size of SiC Bulk Crystals

Two companies, Cree (Compound Semiconductor 5(9) November/December 1999, p. 14) and II-VI Incorporated (Snyder et al. 1999), have recently demonstrated 4-inch SiC wafers fabricated using the PVT method. Three-inch diameter 6H-SiC wafers are commercially available (Cree, Inc. Durham, NC 27003). The properties of commercial 3-inch wafers including crystal quality are not studied in detail yet. High-resolution x-ray diffraction rocking curve measurements performed for 4H-SiC 3-inch wafer (Kuhr et al. 1999) showed ω-peak position shift across the wafer of 0.4 degrees, indication a non-uniform bending of the wafer. The full width at tenth maximum (FWTM) of ω-scan rocking curve varies from 50 to 750 arc sec depending on position on the wafer. In comparison, typical 2-inch n-type SiC wafers, which are being produced by a number of companies (Table 2.1), have the FWTM values less than 100 arc sec over the entire area.

Recently, a Title III program (*Compound Semiconductor* 5(9) November/December 1999, p. 14) has been announced to establish a manufacturing process (crystal growth, slicing, polishing) capable to produce consistent, high quality, large diameter (3-inch), electronic grade SiC substrates. Three multi-million dollar awards have been awarded to Cree, Litton Airtron, and Sterling/ATMI targeting a 75 KSI (kilo square inch) annual production capability for 3-inch SiC substrates.

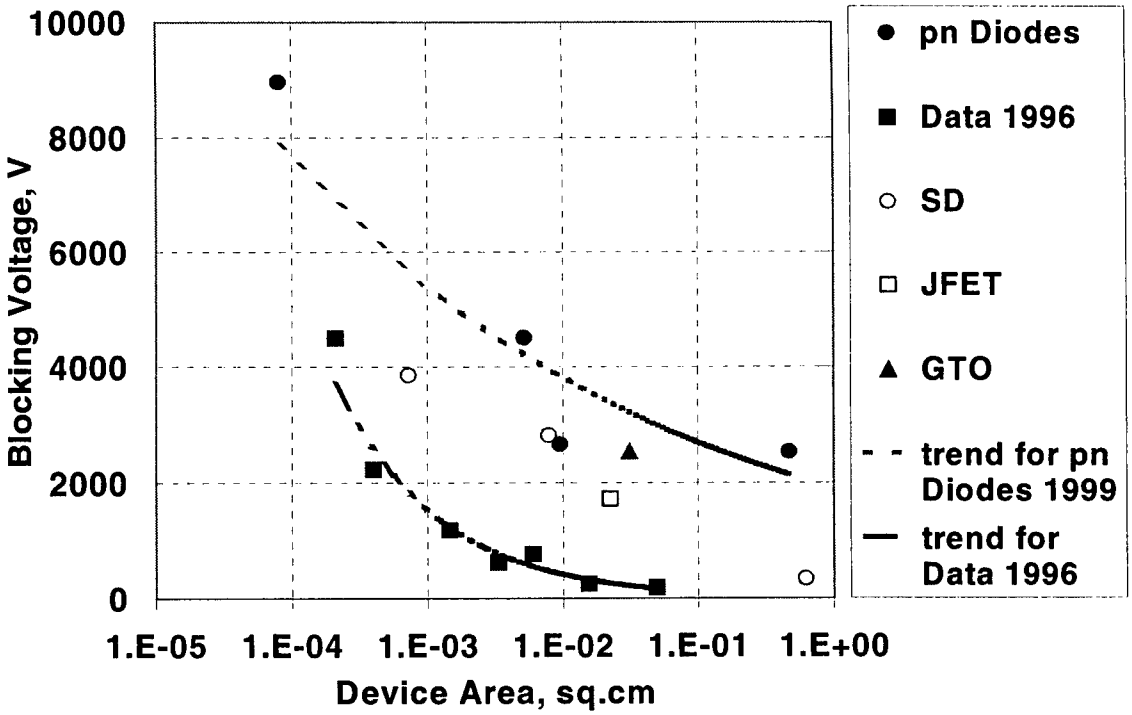


Fig. 2.1. Progress in SiC device development. Blocking voltage for different types of SiC devices vs. device area reported in 1996 and 1999 (Syrkin and Dmitriev, 1999).

The above results on the increase of SiC bulk crystal diameter have been achieved by gradual increase in crystal size during the crystal growth. Starting from a 2-inch diameter seed, it is possible to obtain an SiC ingot having diameter of 2.5 inches in one growth run. In order to make a leap in SiC crystal size, it is necessary to have a large diameter seed. Rendakova and Morozov recently demonstrated that large SiC wafer may be obtained by "gluing" together smaller SiC wafers (Rendakova and Morozov, 1999). This idea was proved when two 1x1 cm^2 pieces of SiC wafer were connected to each other by single crystal SiC epitaxial layer grown by liquid phase epitaxy (LPE) on both pieces in a single epitaxial run (Fig. 2.2). The single crystal nature of the resulting sample was proved using x-ray diffraction measurements. This technical approach may be applied to fabricate large area SiC seeds for $\geq$6-inch SiC bulk growth.

The progress in the development and production of large-size SiC wafers is demonstrated in Fig. 2.3. Using the trend shown, we may predict that 4-inch and 6-inch SiC wafers will be commercially available in 2001 and 2005, respectively.

Defect density reduction

Defects in SiC substrates currently are the main obstacle for realization of large area (>0.1 cm^2) high-power devices. Typical defects in SiC commercial wafers (Fig. 2.4) are voids, dislocations, misoriented blocks, and foreign polytype inclusions. In the past few years, defect density in SiC wafers has been significantly reduced. Cree, Inc. has demonstrated 2-inch SiC wafers having 1.1 cm^{-2} micropipe density over an entire wafer (Hobgood et al. 1999). An ATMI–Sterling research team reported 30 mm diameter wafer having 4 cm^2 area without micropipes (an average micropipe density for the whole wafer was of 3.1 cm^{-2}) (Powel et al. 1999). However, defect density in commercial SiC wafers is still high and must be reduced to much lower level in order to demonstrate devices with operating area from 1 to 10 cm^2.

Table 2.1

List of organizations manufacturing SiC bulk crystals

Organization	Demonstration	Production
Cree, Inc	4 inch	3 inch
Sterling Semiconductor/ATMI	3 inch	2 inch
SiCrystal	2 inch	2 inch
Nippon Steel	2 inch	1 inch
Northrop Grumman/Litton Airtron	3 inch	No information
II-VI Incorporated	4 inch	No information
Freitronics Wafer	No information	No information
OKMETIC	No information	No information
FTIKKS	3.5 inch	No information

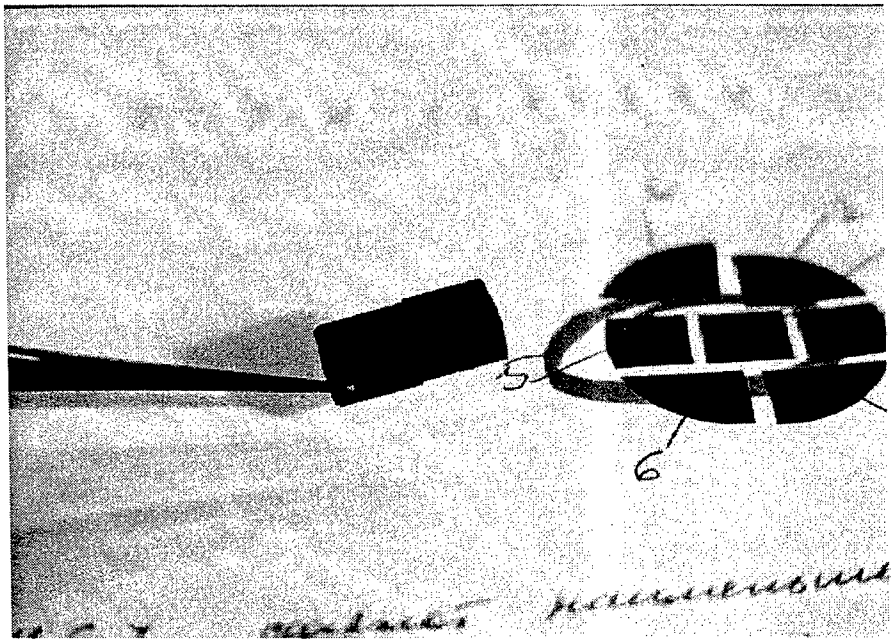


Fig. 2.2. Two SiC pieces connected together by lateral overgrowth process performed by liquid phase epitaxy (Rendakova and Morozov, 1999). Initial SiC wafer cut in pieces is shown in the right.

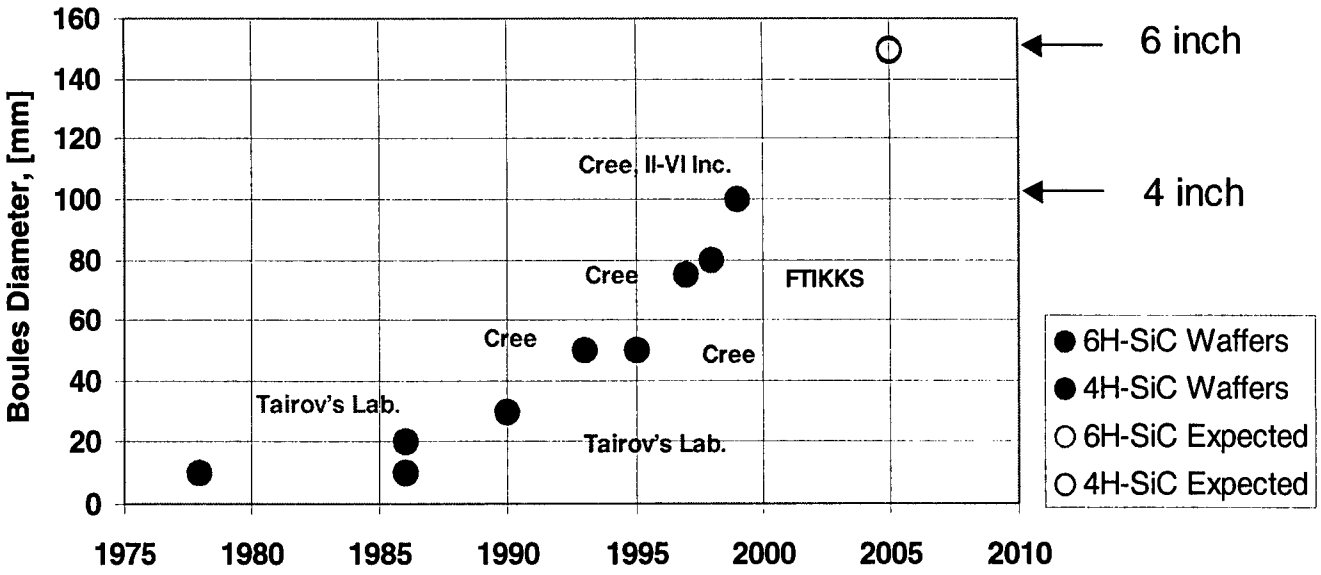


Fig. 2.3. Progress in SiC bulk crystal development performed at Leningrad Electrotechnical Institute (Tairov's Lab), Cree, Inc., FTIKKS (St. Petersburg, Russia), and II-VI Incorporated.

Progress in defect reduction in SiC crystals is much more pronounced for smaller size SiC crystals. Usually it takes a few years to reduce defect density for SiC crystals of a particular size (Fig. 2.5) (Carter, Jr. et al 1999). Note that the record size SiC pn diodes with the area of 7x7 mm^2 were fabricated in 1999 on 35 mm SiC wafers, although 41 mm and 50 mm SiC wafers were commercially available (Lendenmann et al. 1999). This development was possible because defect density in 35 mm wafer was low. In this section we review recent results on defect investigation and defect density reduction for SiC bulk crystals.

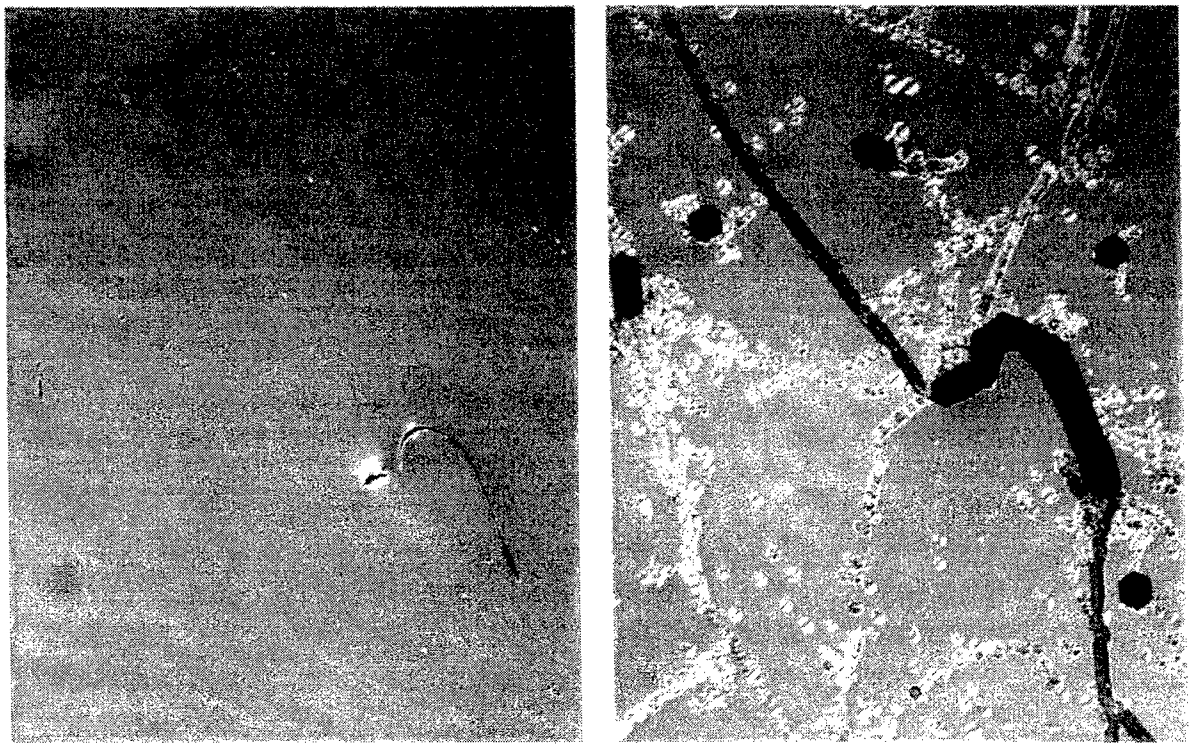
Voids in SiC wafers

Hofmann and co-authors (Hofmann et al. 1999a) gave a classification of void defects in SiC bulk crystals. The following three categories of voids were selected: (1) micropipes and nanopipes, (2) macrodefects (pipes), and (3) planar voids. Micropipes, nanopipes, and macropipes propagate through SiC crystals in the growth direction, which is usually close to ***c*** axis direction. In the [0001] plane, nanopipes, micropipes and macropipes have a typical size less that 1 micron, from 1 to 10 microns, and larger that 10 microns, respectively. Planar voids usually have the largest dimension in the direction perpendicular to the ***c*** axis. There has been practically no investigation of the nature and properties of nanopipes in SiC crystals. Micropipes were studied by a several research teams (Giocondi et al. 1996, Heindl et al. 1998, Huang et al. 1999, Pirouz 1998, Yamaguchi et al. 1999a). Some micropipes are related to hollow core dislocations. In SiC wafers, micropipe and dislocation densities range from 10 to 100 cm^{-2} (Anikin et al. 1999) and 10^4 to 10^6 cm^{-2} (Kalinina et al. 1999a), respectively. Usually micropipe density is higher at the periphery of SiC wafer. Planar defects (Sudarshan et al. 1999) are rather random in commercial SiC wafers.

Macropipes (Fig. 2.6) usually have diameter ranging from 10 to 100 microns and are not associated with dislocations. Macropipes are often located at boundaries of foreign polytype and misoriented block. They are also observed to start at the interface between the SiC seed and the graphite crucible lid (Sanchez et al. 1999a). These defects are believed to be formed due to local decomposition and evaporation of seed crystal. The micropipe defects may be reduced by the formation of continuous uniform graphite layer on the back side of SiC seed.

Defect generation during SiC bulk growth was investigated by Hofmann and co-workers (Hofmann et al. 1999b). SiC crystals having diameter from 1.2 to 1.5 inch were grown on seeds with different micropipe density in order to study the defect formation. The source material was synthesized from elemental high

purity Si and C. After heating up to about 2100 – 2300°C, the growth was initiated by lowering the system pressure from the starting value of 800 Torr to the growth pressure of 5 – 40 Torr. The pumping time constant (Tairov and Tsvetkov 1983), τ, was varied between 120 sec and 2400 sec, to control supersaturation. Besides the micropipes penetrated from the seed, no other micropipes were created at the initial stage of SiC crystal growth. The authors indicted that sublimation etching of the seed was not necessary to avoid defect formation and pumping time variation did not provide significant effect on the defect generation. The micropipe formation strongly correlated with occurrence of second phases in SiC like carbon inclusions. Carbon inclusions formed in grown SiC crystal often caused micropipe formation. Other inclusions, possibly Si droplets, also acted as a starting point of micropipes. Crystals grown on micropipe-free substrates had micropipe density ranged from 100 – 200 cm^{-2}. Although most of the micropipes were caused by inclusions, no obvious correlation between the density of inclusions and the density of micropipes was found. Two additional sources of micropipe formation were identified such as polytype inclusions and micropipe multiplication from large diameter micropipes. A remarkable micropipe density reduction (factor 2 – 4) was observed in the case of temperature gradient reduction in growth zone.



a b

Fig. 2.4. Defects in 6H-SiC commercial wafers (image size is 450x575 μmxμm): (a) surface of as received commercial 6H-SiC wafer, optical photo of polished (0001)Si surface, (b) the same wafer after 2 minutes chemical etching in molten KOH at 500°C, black hexagonal pits are micropipes, white etch pits are probably related to dislocations.

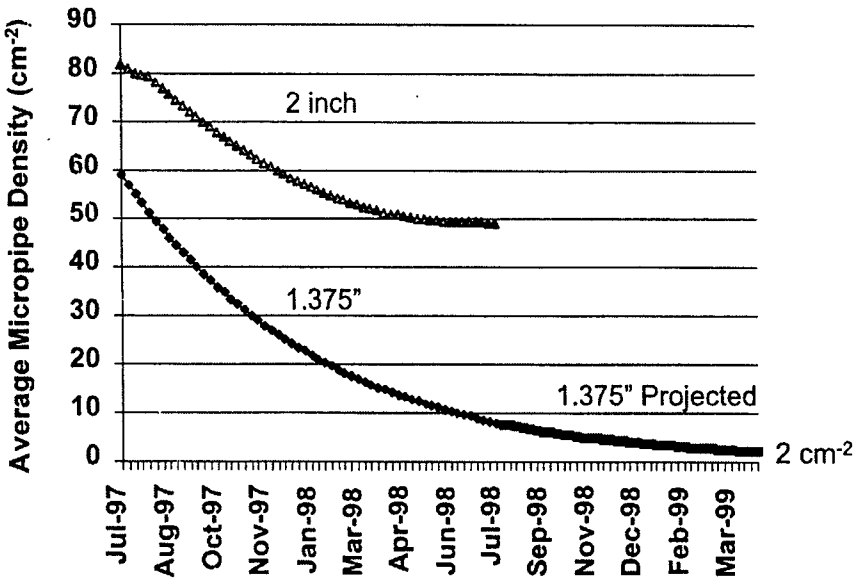


Fig. 2.5. Progress in defect density reduction in SiC wafers reported by Cree, Inc. (Carter, Jr. et al. 1999).

Micropipe formation was investigated by Okamoto and co-workers (Okamoto et al. 1999). Crystals were grown by PVT method using "standard" source material and source material enriched with silicon. Micropipe density was about 22.5 cm^{-2} for SiC crystal grown using a source with added Si. Crystal grown without Si addition had no micropipes. Quantitative Auger electron spectrometry measurements revealed neither Si-rich nor C-rich compositions at the starting point of micropipe. It was suggested that a micropipe formation is related to the multiple nucleation, which would occur in the surface region with high supersaturation. Oxygen contamination as a driving force for micropipe formation was suggested in ref. (Rauls et al. 1999).

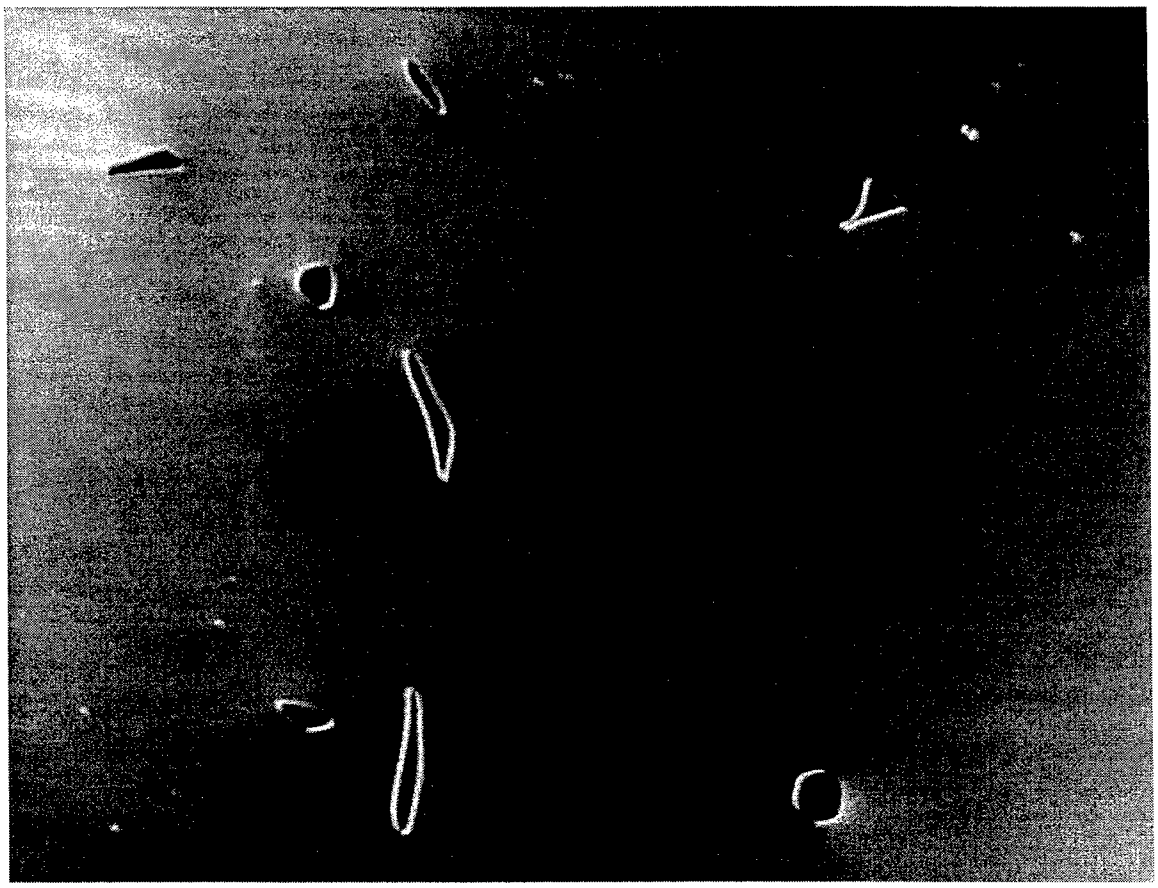


Fig. 2.6. Optical microscopical image (image size is 1150x1500 μmxμm) of macropipes in SiC commercial wafer.

Properties of SiC bulk material around micropipes were investigated by Raman microprobe imaging (Harima et al. 1999). Electron concentration near micropipe was found smaller ($3.2x10^{17}$ cm^{-3}) than that in material without micropipes ($1.3x10^{18}$ cm^{-3}). Electron mobility was found to be smaller than in the bulk of the material (20 cm^2/Vs vs. 32 cm^2/Vs). Stress around micropipes in SiC crystals was investigated using interference pattern by a polarizing optical microscope (Kato et al. 1999a).

It was shown that proper seed surface preparation is an important factor for defect density reduction in SiC grown by PVT (Pelissier et al. 1999). In situ sublimation etching was used to remove damaged and contaminated surface layers of a seed. At seed temperature of 1800°C, Ar ambient pressure of 50 Torr, and etch duration of 10 min, high quality surface of 6H-SiC seeds was obtained. For 4H-SiC, the optimum etching temperature was 1850°C. In order to promote lateral growth, special attention was paid to SiC source preparation. Before the growth process, the SiC powder was heated in vacuum and then sintered in the sublimation growth reactor at high temperature and atmospheric pressure level. For non-sintered powder source, less homogeneous steps were observed on the seed surface after the etching. Pressure and temperature conditions before the growth are shown to be also critical for high quality seed surface formation.

Kitou and co-workers (Kitou et al. 1999) investigated pressure effects on sublimation growth of bulk SiC. During the sublimation growth of 6H-SiC, pressure in growth chamber was varied from 1 to 100 Torr. It was found that crystal regions grown at 1 Torr contain many black particles of 5 – 20 microns in size. These particles initiated formation of pits and voids.

Sasaki and co-workers (Sasaki et al., 1999) investigated SiC growth performed at Ar gas pressure of about 5 – 10 Torr, source temperature range of 2250 – 2350°C, and substrate temperature of 1800°C. SiC crystals were grown in two growth runs. Source material was recharged between these two growth runs. A highly nitrogen doped region of about 0.5 mm thick was detected on the interface between materials grown in the first and second growth runs. In the course of growth, nitrogen concentration dropped down to the 10^{17} cm^{-3} level. It was found that half of the micropipes disappeared at the interface between two growth regions (Table 2.2). Micropipes annihilated by meeting planar defects or other micropipes. These results show the possibility to control micropipe formation and annihilation in sublimation process.

Residual stress in SiC boules grown by sublimation was investigated (Ha et al. 1999a). The radial and axial temperature gradients imposed on a growing crystal create thermal stresses in the crystal even in the absence of external mechanical forces. During the growth the center part of a crystal is cooler than the periphery, putting the center in tension while the periphery region is under compression. If plastic expansion occurs during the growth, crystal periphery is expected to be under tension while the center is under compression. X-ray diffraction measurements were used to determine the plastic deformation frozen in SiC crystals. It was found that the total misorientation of the basal plane across boule diameter was typically between 100 – 2000 arc sec. A continuous reduction of the *c*-lattice spacing was observed along the radii of crystals from the center to the edge. The amount of strain of the c-lattice spacing at the edge compared to the center was (~0.003) ~ (~0.002)%.

Table 2.2

Micropipe densities in SiC crystals grown in two subsequent runs [Sasaki et al. 1999].

		Number of micropipes
2nd growth	Surface	9
	Interface between 1st and 2nd growth	20
1st growth	Interface between 1st and 2nd growth	38
	Seed	39
Micropipe penetrated from seed to the surface		7

Defect formation during SiC bulk sublimation growth was investigated by a few research teams. X-ray imaging technique was applied during SiC crystal growth. This method allowed Wellmann and co-workers (Wellmann et al. 1999) to monitor SiC crystal growth interface, change of source material, and crystal growth stability.

In-situ investigation of defect formation during bulk SiC sublimation growth has been reported (Yamaguchi et al. 1999b, Kato et al. 1999b). X-ray topography technique has been used. The growth chamber was equipped with x-ray goniometer, x-ray source (a rotating-anode 18 kW generator with molybdenum target) and CCD camera. The x-ray beam was transmitted directly from the bottom to the top of the crucible through the growing crystal and x-ray intensity was measured by a scintillation counter. Low defect density Acheson and Lely crystals were used as seeds for SiC bulk sublimation growth. Formation of micropipes and domain boundaries were detected during the growth. Evolution of these defects during the growth was tracked using x-ray topography imaging. The same technique has been used for growth rate measurements (Oyanagi et al. 1999). This technique may become a very important tool for the development of low defect density SiC bulk crystals.

One way to avoid micropipe formation has been reported by a Erlangen University research team. 6H-SiC micropipe-free bulk crystals were grown by PVT method at the average thermal gradient inside the growth container less than 5 K cm^{-1} (Schulze et al. 1999). It was found that a crucial point in avoiding micropipes is

the annealing step of the seed prior to the growth and the initial slow nucleation at thermal equilibrium conditions. It was also noticed that (1) micropipes already contained in the seed penetrate the entire boule, and (2) micropipes are formed in the neighborhood of polytype inclusions. SiC growth rates for micropipe-free growth was less than 0.3 mm/hr due to low temperature gradient. It is still an open question if micropipe-free SiC sublimation growth is possible at growth rates suitable for bulk crystal growth.

Makarov and co-workers (Makarov et al. 1999) used a tantalum container to reduce defect density in SiC crystal grown by sublimation. It was shown that the Ta container suppresses graphitization of the SiC source and reduces formation of graphite inclusions at the surface of the seed. An additional advantage of the use of a Ta container is low chemical reactivity of the container side walls compared to the graphite crucible usually etched during the SiC sublimation growth process. Sublimation growth technology with a Ta container allowed bulk SiC crystals growth at rates of 0.5 – 0.8 mm/hr with micropipe density less than 30 cm^{-2} and source utilization efficiency higher than 90%.

Another growth technology for SiC crystals with low defect density was proposed based on an idea of lateral crystal growth without crystal contact with crucible walls. It is known that free-standing SiC crystals grown by Lely method (Lely 1955) have lower defect density than SiC crystal grown by seeded sublimation technique. Vodakov and co-workers (Vodakov et al. 1999) used the same approach to grow 40 mm diameter SiC free-standing crystals. Sublimation growth was performed in closed Ta or graphite containers at temperatures 2000-2300°C and Ar gas pressure 10^{-3} – 50 Torr. Micropipe density in grown material was less than 20 cm^{-2}. Dislocation density ranged from 100 to 1000 cm^{-2}.

Another way to fabricate SiC wafers with low micropipe density is to "reaper" micropipes in commercial SiC wafers. A few research teams have demonstrated micropipe closing during liquid phase epitaxial growth of SiC (Yakimova et al. 1996, Hofmann and Muller 1999).

Micropipe filling process has been developed at TDI, Inc. (TDI, Inc., Gaithersburg, MD 20877). This "repairing" process is based on SiC growth inside micropipe channels. The micropipe filling technique can reduce micropipe density by a few times and resulted in zero micropipe density in best R&D 35 mm and 41 mm 6H-SiC and 4H-SiC wafers (Dmitriev et al. 1999). Micropipe density in the initial SiC wafer before micropipe filling process exceeded 100 cm^{-2}.

Dislocations

Recently, it has been recognized that not only voids but dislocations also limit the performance of SiC devices (Chelnokov et al. 1998). It was shown that dislocations in SiC epitaxial structures may lead to premature electric breakdown and increase leakage current in SiC device structures (Neudeck et al. 1998a). These results triggered intense investigation of dislocation formation in SiC bulk crystals. One source of dislocations in bulk SiC crystals was identified to be defects of seed surface treatment (Sanchez et al. 1999b). Screw dislocation densities for SiC grown by sublimation on Lely crystal seeds varied from less than 10^3 cm^{-2} for hydrogen etched seeds to 10^6 cm^{-2} for roughly polished seeds. Graphite inclusions (artificially created graphite dots) on the seed surface were found to be another source of dislocations. The screw dislocation density over the graphite inclusions was in the order of $5x10^5$ cm^{-2}, while in the other areas of the grown material it was below 10^4 cm^{-2}.

It was shown (Neudeck et al. 1998b) that most 4H-SiC pn diodes containing no dislocations in device area exhibited excellent current-voltage (I-V) characteristics. In contrast, devices that contained at least one elementary screw dislocation exhibited 5-35% reduction in breakdown voltage and a softer (higher leakage) reverse I-V characteristic. A mechanism of threading dislocation formation in bulk SiC crystals was investigated (Ha et al. 1999b).

Dislocation density reduction in SiC grown by sublimation has been reported by using porous buffer layers (Mynbaeva et al. 1999a). Porous SiC substrates were fabricated by surface anodization of SiC commercial wafers. Thickness of SiC material grown on porous buffer was about 10 microns. X-ray topography showed defect density and stress reduction in SiC grown on porous material (see section on Defects in Epitaxial Layers).

Alternative Methods for SiC Bulk Crystal Growth

Two alternative methods to grow bulk SiC crystals are under investigation, high-temperature chemical vapor deposition (CVD) and liquid phase growth. High-temperature CVD (Ellison et al. 1999) provides SiC growth rate up to a few millimeters per hour. SiC crystals 6 mm thick and 30 mm in diameter were grown by this method. Micropipe density was about 50 cm^{-2}.

SiC bulk crystals 30 mm in diameter and up to 10 mm in length were grown from the liquid phase (Epelbaum et al. 1999). SiC crystals were grown using silicon melt as solvent at temperatures 1900-2400°C and ambient Ar gas pressures of 100-120 bar. This technique is in the development stage and may lead to SiC substrates without micropipes and a high doping level for both n- and p-type materials (Rendakova et al. 1998).

3C-SiC crystals were grown from carbon-silicon melt-solution (Wollweber et al. 1999). Conventional Floating Zone method was utilized to grow 3C SiC boules up to 11 mm in diameter and 3-4 mm in length. Growth rate of 0.1 to 0.4 mm/hr has been reached.

Currently, these methods are far away from industrial use, but they may become important tools for SiC bulk crystal fabrication if PVT method will be insufficient to further increase SiC boule size and eliminate micropipes.

EPITAXIAL SIC GROWTH

The main epitaxial technology used for SiC device structure fabrication is CVD. Northrop Grumman reported results on preproduction growth of 4H-SiC epitaxial layers employing multi-wafer CVD reactor (Nordby et al. 1999). For 13/8-inch diameter substrates, reported layer uniformity was typically better than ±5% (standard deviation/mean) for doping and ±3% for thickness. In a multi-wafer run, interwafer uniformity is typically better than ±8% for doping and ±3% for thickness. For 2-inch diameter wafers, reported doping and thickness uniformity was approximately ±5%. Cree reported thickness non-uniformity for SiC epitaxial layers grown over a 50 mm wafer about 1% and doping non-uniformity less than 5%.

Bergman and co-workers (Bergman et al. 1999) investigated uniformity of carrier lifetime in 4H-SiC epi layers using photoluminescence technique. The highest value for the carrier lifetime of 2.9 μs has been measured for a 80 μm thick epi layer grown by a hot-wall CVD technique with concentration N_d-N_a < $5x10^{15}$ cm^{-3}. An average lifetime in epi layers for four wafers ranged from 0.29 to 0.39 μs. Results of this study indicated that substrate defects propagate into the epi layer and creates intrinsic defects, which influence the lifetime.

Thick epitaxial layers

In order to fabricate SiC devices for high voltage applications, thick SiC epitaxial layers with low background doping concentration are needed. For example, SiC devices designed for 10 kV reverse voltage require about 100 microns thick base region with concentration N_d-N_a less than $5x10^{14}$ cm^{-3}.

4H-SiC diode with breakdown voltage of 5.5 kV was fabricated at Cree based on 85 μm thick epitaxial layer grown by CVD technique using a horizontal hot-wall reactor (Irvine et al. 1998). Silane and propane were used as the precursors. Growth temperatures and the C/Si ration were varied from 1500 to 1700°C and 1 – 2, respectively. Growth rate was 10 μm/hr. The concentration N_d-N_a was controlled from high 10^{14} cm^{-3} to low 10^{19} cm^{-3} using nitrogen gas for doping.

4H-SiC 120 μm thick epitaxial layers have been reported by Rowland and co-workers using CVD process (Rowland et al. 1999). Concentration N_d-N_a was of $9x10^{15}$ cm^{-3}. Growth rate was <5 μm/hr. Small changes in C/Si ratio lead to high background doping. Even a 10% change in C/Si value from the optimum one gave a background doping in the 10^{17} cm^{-3} range.

High-temperature (1800 – 1900°C) CVD method was used to grow 4H-SiC layers with growth rate of 16-27 μm/hr [Zhang et al. 1999]. Background concentration N_d-N_a ranged from mid 10^{13} to low 10^{16} cm^{-3}. Usually, the epitaxial layers grown at temperatures higher than 1870°C or with high SiH_4 flow rates showed a much

smoother surface than those grown at lower temperatures or lower SiH_4 flows. Surface of epitaxial layers was smooth even for 80 μm thick layers. The C-face samples showed much smoother surface than Si-face samples. Pit-like defects with density of about 10^4 cm^{-2} were on epi surface. Size of the pits monotonically increased with layer thickness, while pit density did not depend on layer thickness.

Another technique to grow thick SiC epitaxial layers is sublimation epitaxy. Sublimation epitaxy is promising for epitaxial growth of SiC with high growth rates (Syvajarvi et al. 1999a, Segal et al. 2000). Thick 4H-SiC layers have been grown with an average growth rate of 100 mm/hr at 1775°C on 35 mm diameter wafers (Syvajarvi et al. 1999b). The window for morphological stability was determined by growth rate ramp-up, growth rate, temperature gradient, source to substrate distance, and substrate surface orientation. For 100 μm thick layer, macrosteps were not resolved with optical microscopy, although the growth mode was given by the step flow mechanism. The thickness non-uniformity of the layers (expressed by σ/mean) was less than 5% for 32 mm. Crystal structure was improved by sublimation epitaxial growth. Average values of the FWHM for ω-rocking curves are 64 arcsec for the substrate and 15 arcsec for the epitaxial layer. The layer was n-type with a concentration N_d-N_a of about (1-2)x10^{15} cm^{-3}. Intentional doping with B (3x10^{16} cm^{-3}) provided compensated material with a resistivity of 6x10^4 Ohm cm. Additional V doping ((2-3)x10^{16} cm^{-3}) resulted in semi-insulating material with a resistivity of about one order of magnitude less than commercial SiC. Degradation of surface morphology or structural quality due to V doping was not observed.

Summarizing, CVD and sublimation epitaxial method are promising techniques for deposition of thick low-doped SiC layers for high-power devices. Two material parameters will determine the method to win this competition, defect density and minority carrier diffusion length.

Defects in Epitaxial Layers

Elimination of defects in SiC epitaxial layers is the key issue in the fabrication of large area high power SiC devices. Information on defect formation in SiC epitaxial layers is limited. Surface defects called "tetrahedral pits", "comet tails", "carrots", "shallow round pits", and "half-moon" have been described in literature (Seshadri et al. 1999, Kimoto et al. 1999). Formation mechanisms for these defects are not clear yet. Micropipes and dislocations are usually present in SiC epitaxial layers. Step-bunching on SiC surface was investigated for epitaxial layers grown by CVD, sublimation, and LPE (Syvajarvi et al. 1999c).

Surface morphology of thick 4H-SiC epitaxial layers was investigated for materials grown by CVD using SiH_4 and C_2H_4 in the temperature range from 1800 to 1900°C (Zhang et al. 1999). It was found that the epitaxial layers grown at temperatures higher than 1870°C or with high SiH_4 flow rates have much smoother surface than those grown at lower temperatures or lower SiH_4 flows. Most of observed pit defects were substrate related defects. For high growth temperatures, a smooth surface was obtained even for 80 μm thick epitaxial layers. These layers were used to demonstrate 3 kV Schottky diodes.

Defects in 4H-SiC 25 μm thick epitaxial layers grown by hot-wall CVD in SiH_4-C_3H_8-H_2 gas system at 1600°C were studied by Wahab and co-workers (Wahab et al. 1999). Doping level in the epilayer was about 2x10^{15} cm^{-3}. Schottky diodes were formed by direct "writing" technique on the top of selected defects. All diodes formed on material having micropipes exhibited breakdown voltage less than 1 kV. The diodes placed on triangular defects showed low breakdown voltage and high leakage current. Carrot shaped ditches in epilayer surface were not found to be harmful with respect to the absolute value of breakdown voltage. Diodes placed on other defects such as foreign polytype inclusions did not show device performance. Only 20% of diodes, which were placed on surface areas containing no defects, were found to block 2 kV or higher voltages. The clear correlation between breakdown voltage and screw dislocation density was observed (Fig. 2.7).

Defects in SiC epitaxial layers grown by sublimation and LPE were investigated using KOH etching and sample cleavages (Syvajarvi et al. 2000). From examination of cross-sectional cleavages with optical microscopy, defects in homoepitaxial SiC layers including stacking faults, stripe defects, and micropipes were studied. For 6H and 4H-SiC layer grown by sublimation, it was shown that smooth surface can be obtained even for 120 μm thick layers (Syvajarvi et al. 1999d).

Defect formation in sublimation epitaxy was studied by Furusho and co-workers (Furusho et al. 1999). 3C-SiC polycrystalline semiconductor grade plates were used as SiC source material while 4H-SiC (0001) 8° off-axis oriented wafers were used as substrates. SiC epitaxial layers were grown at source temperature ranging from 1900 to 2100°C, temperature gradient of about 3.7 - 8°C/mm, growth pressure from 0.3 to 100 Torr, and source to substrate distance of 1.5 mm. Growth rate depended on temperature gradient at all pressures. Surface morphology was smother for layers grown with lower growth rate (60 μm/hr vs. 10 μm/hr). Micropipes penetrating into the epitaxial layer from the substrate were found.

Material quality and device performance improvement has been reported (Dmitriev et al. 1999, Kalinina et al. 1999b) for 4H-SiC grown on SiC substrate materials with reduced micropipe density (TDI, Inc., Gaithersburg, MD 20877). Large area Schottky diodes (up to 8 mm^2) based on 4H-SiC epitaxial layers grown on SiC wafers with reduced micropipe density capable to withstand electric breakdown field exceeding 1 MV/cm were fabricated. Initial micropipe density in 4H-SiC substrate was about 100 cm^{-2}. After micropipe filling process the micropipe density was reduced to 0.1 cm^{-2}.

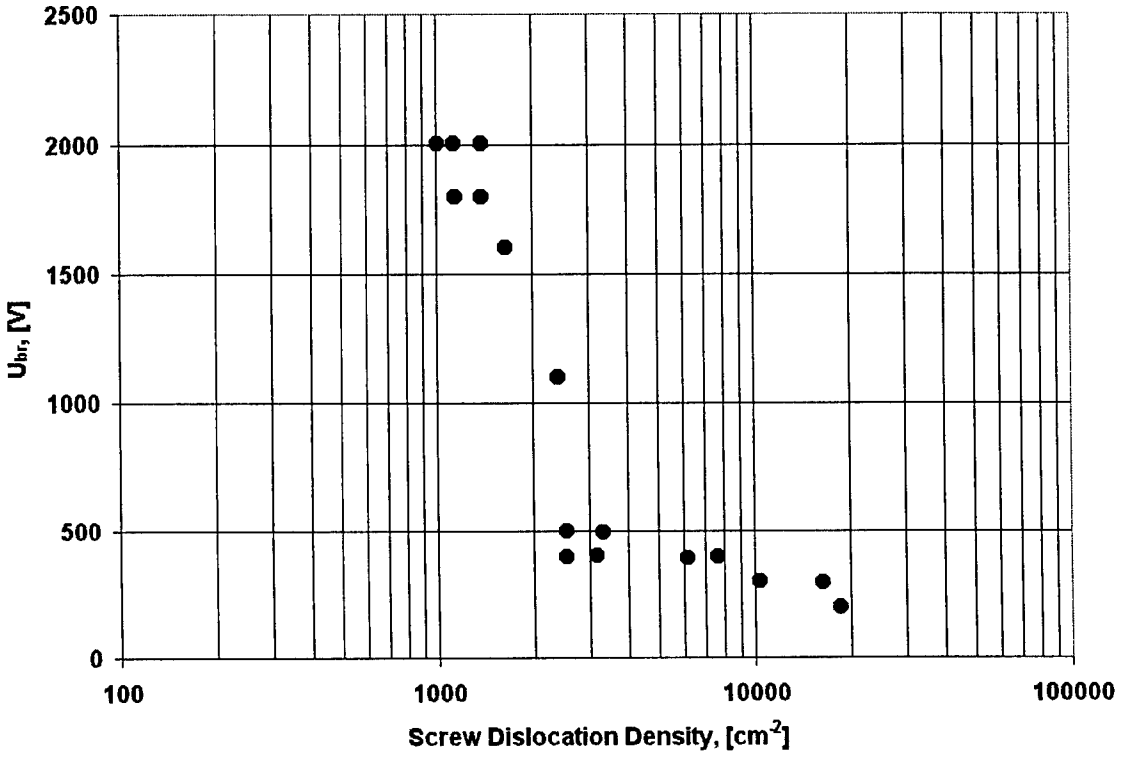


Fig. 2.7. Breakdown voltage of Schottky diodes vs. screw dislocation density (Wahab et al. 1999).

The study performed on SiC epitaxial layer grown by CVD on SiC wafer with filled micropipes showed that micropipe density in CVD material was at least 5 times less than that in the initial SiC wafer before micropipe filling process (Saddow et al. 1999). It is important that micropipe-filling technique is not sensitive to wafer diameter. Micropipe density reduction process has been applied with the same efficiency to 35 mm and 50 mm wafers (Rendakova and Dmitriev 1999).

The stability of filled micropipes was tested by growing an epitaxial layer by sublimation at about 1800°C on the top of SiC wafers with filled micropipes (Yakimova et al. 1999). Micropipes were mapped before filling process. After sublimation epitaxy, inspection under reflection and transmission light and crossed polarizer did not show any indications of micropipe propagating from the substrate. KOH etching did not reveal such

as well. Furthermore, on cross-sectional samples it was observed that micropipes terminate close to the substrate/LPE layer interface. Surface morphology of 30-50 μm thick epitaxial layers grown by sublimation is featureless under optical microscope examination, even being grown on a rather stepped initial surface after micropipe filling process.

Recently it was discovered (Mynbaeva et al. 1999b) that defect density in SiC epitaxial layers could be reduced using porous SiC buffer layers (Fig. 2.8). Surface of SiC layers grown by sublimation on porous SiC was flat and mirror-like. The structural perfection of epitaxial layers grown on porous substrates was characterized by x-ray diffraction and x-ray topography. The x-ray topographs indicated that defect related stress in the epitaxial layer was much less than that in initial SiC substrate, as measured before anodization. Defect density reduction in about 10 times was estimated.

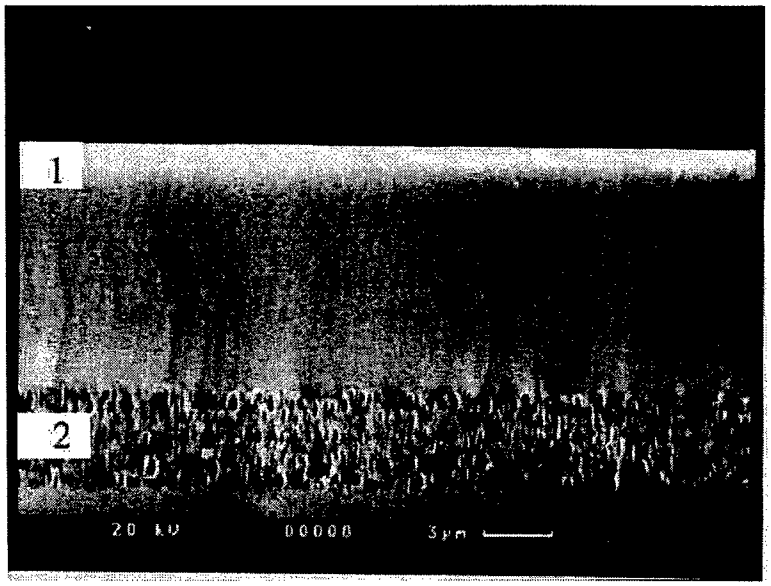


Fig. 2.8. SEM photograph of cross-section of SiC layer (1) grown by sublimation on porous SiC (2) (Mynbaeva et al. 1999a).

CONCLUSIONS

SiC technology is progressing rapidly showing expressive improvement in both material quality and device performance. 4 inch SiC wafers have been recently demonstrated and 6 inch material is expected to be developed in a few years. Thick (~100 μm) low doped SiC epitaxial layers, which are required for high voltage devices, have been demonstrated by a number of research teams. However, defects in substrate and epitaxial SiC materials are the main limiting factor for the development of high power SiC devices. Mechanisms of defect formation during SiC bulk and epitaxial growth must be investigated and technical approaches to low defect density SiC materials must be explored.

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CHAPTER 3

GALLIUM NITRIDE MATERIALS TECHNOLOGY

Steven P. DenBaars

INTRODUCTION

The Group-III nitride-based semiconductors have emerged as the leading material for the production of blue LEDs, blue laser diodes, and high power, high temperature electronics. The achievement of high brightness (HB) blue InGaN LEDs has basically led to a revolution in LED technology and opened up enormous new markets that were not accesible before. The historical evolution of GaN materials and device technology in Japan to the USA and Europe in the early 1990's is regarded as one the key developments in solid-state devices today. In Europe gallium nitride materials and devices have gained increasing attention from both academic institutions and industry. The industrial effort is being led by the Siemens/Osram joint venture (Osram Opto Semiconductors), which is in full scale production of blue and white LEDs. In addition, Philips lighting has a joint venture with Agilent technologies (LumiLedsLighting LLC) to develop GaN-based solid-state lighting. The automotive industry in Europe is leading the world in implementing GaN LED backlights in dashboards with several models of Volkswagen automobiles already in production. Europe also possesses leading efforts in both bulk crystal growth and the leading producer of epitaxial systems (Aixtron). The purpose of this chapter is to review the status of GaN materials technology with an emphasis on epitaxial growth.

MATERIALS TECHNOLOGY FOR GAN

Substrates

Several problems in the epitaxial growth of nitrides originate from the non availability of single crystalline GaN substrates or other high quality single crystalline substrates with the same lattice parameters as GaN. For this reason, so far, most of the epitaxial growth of nitrides has been performed on sapphire or SiC substrates. In both cases, problems due to the lattice mismatch between the nitride epi-layer and the substrate (16% for sapphire and 3.5 % for SiC) have to be overcome. One of the major breakthroughs in the growth of device quality group-III nitride material was the implementation of nucleation layers. Using sapphire substrates, thin AlN or GaN nucleation layers deposited at temperatures between 500 and 750 °C showed to remarkably improve the quality of the GaN film grown at temperatures above 1000 °C (Akasaki, et al. 1989; Nakamura 1991). In the case of SiC substrates, the growth is usually initiated with the deposition of a thin AlN nucleation layer at high temperatures (Weeks, et al. 1995).

By this means, GaN material of comparable quality on both types of substrates could be achieved. Since so far, most GaN growth has been performed on c-plane sapphire substrates, in the following section just the growth on c-plane sapphire will be discussed.

Additional substrate materials are currently being examined to determine if the properties of the GaN thin films can be enhanced by improved structural matching. From Figure 3.1 we can see that in addition to sapphire several other substrates offer potentially much better latticed and thermal matching. To this end,

6H-SiC, ZnO, and 3C-SiC, MgO are alternative substrate materials. ZnO has a wurtzite structure with lattice constants of (a=3.32A, c=5.213A) and thus offers an better structural match to the equilibrium wurtzite nitride. 3C-SiC and MgO are both cubic zinc-blende structures having better structural and thermal match to the nitrides than sapphire. 3C-SiC and MgO have cubic lattice constants of a=4.36A and a=4.22A, respectively. Although the nitrides are most commonly observed as the wurtzite (2H) polytype, they can also crystallizes in a metastable zinc-blende structure (a=4.52A) when using non-equilibrium based growth techniques. The identification of a suitable substrate material that is lattice matched and thermally compatible with GaN wurtzite structure (a=3.19A, c=5.185A) will alleviate many of the difficulties associated with the deposition of device quality material.

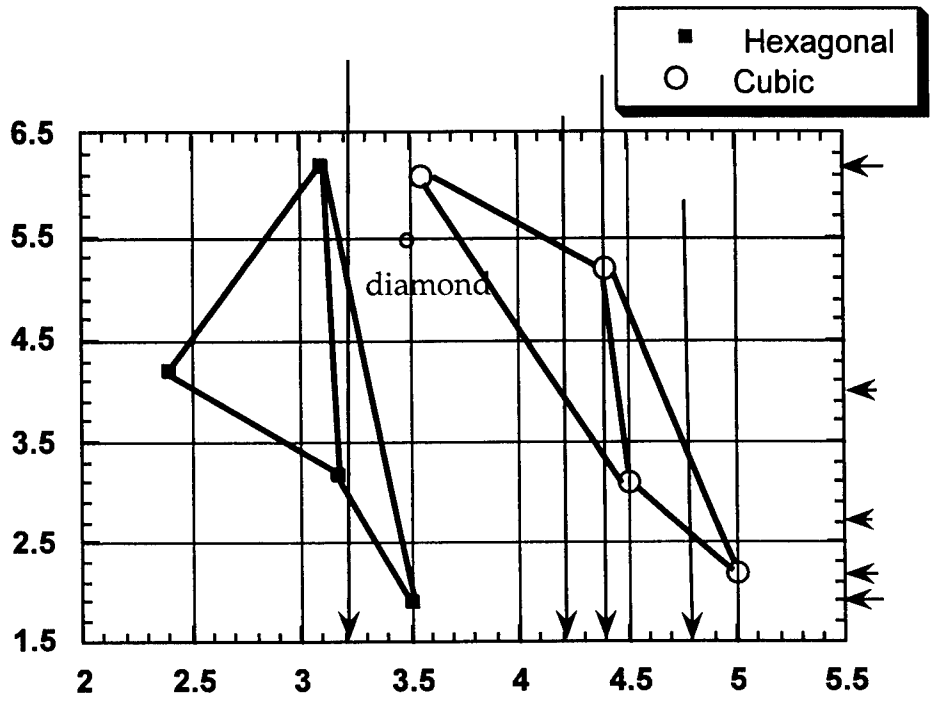

Fig. 3.1. Bandgap and Wavelength of III-V Nitrides versus Lattice Constant.

MATERIALS GROWTH

Metalorganic Chemical Vapor Deposition (MOCVD)

In the past few years, metalorganic chemical vapor deposition (MOCVD) has evolved into a leading technique for production of III-V nitride semiconductor optoelectronic devices and electronic devices. For commercial GaN device applications MOCVD has emerged as the leading candidate because of the achievement of super-bright blue LEDs (Nakamura, et al. 1994) and the large scale-manufacturing potential of the MOCVD technique. The majority of all GaN based p-n junction light emitting diodes (LEDs) typically employ impurity related transition for blue and green emission (Pankove 1972; Nakamura, et al. 1994; Akasaki, et al. 1993; Kahn, et al. 1995). Recently, direct bandgap emission in the blue-green spectral region has been obtained using high In content in single quantum well (SQW) LEDs and lasers using the two-flow MOCVD technique (Nakamura, et al. 1996). Full-color LED displays can now be made entirely with the MOCVD technique when combining the blue and green GaN LEDs with the very high brightness yellow and orange emitting LEDs which were demonstrated in the AlGaInP materials system in the early 1990's (Kou, et al. 1990; Sugawara, et al. 1991). Understanding the growth of AlInGaN/GaN based materials by metalorganic chemical vapor deposition (MOCVD) is therefore of extreme importance in improving the properties of these optoelectronic and high temperature electronic devices.

MOCVD Reaction Chemistry

The basic MOCVD reaction describing the GaN deposition process can be described by the following reaction:

$$Ga(CH3)3(v) + NH3(v) \rightarrow GaN(s) + 3CH4(v)$$

where (v)=vapor and (s)=solid

This balanced expression ignores that the specific reaction path and reactive species are largely unknown. The details of the reaction are not well known and the intermediate reactions are thought to be complex. A more likely reaction pathway leading to growth of the GaAs epitaxial layers involves the homogeneous decomposition of TMGa as reported in an earlier study on GaAs epitaxy (Nishizawa, et al. 1985; DenBaars, et al. 1986).

$$Ga(CH3)3(v) \rightarrow Ga(CH3)2(v) + CH3(v)$$

$$Ga(CH3)2(v) \rightarrow GaCH3(v) + CH3(v)$$

$$Ga(CH3)(v) \rightarrow Ga(v) + CH3(v)$$

The Group-V hydride source, is thought to decompose heterogeneously on the GaN surface or reactor walls to yield atomic nitrogen or a nitrogen containing radical at high growth temperatures. Abstraction of the first hydrogen bond is thought to be the rate limiting step in the decomposition of ammonia.

$$NH3(s/v) \rightarrow NH(3-x)(s/v) + x\ H(s/v)$$

Therefore one possible growth mechanism of GaN that might occur at the solid vapor interface could be expressed as follows:

$$GaCH3(s/v) + NH(s/v) \rightarrow GaN(s) + 1/2H2$$

However, the level of understanding of the growth process is inadequate at best. The most difficult topic, and certainly the least developed, is the area of the kinetics of the process and growth mechanisms occurring at the solid/vapor interface during MOCVD growth. Pyrolysis and diffusion of the group-III source through the boundary layer is the main pathway controlling the growth rate. However, parasitic side reactions such as solid adduct formation between TMAl and ammonia will decrease the growth rate by limiting the flux of group-III sources to the growing interface.

Optimization of MOCVD growth is typically done by empirical studies of external parameters such as growth temperature, V/III ratio, substrate tilt and mass flow rates. These studies have identified three regions of growth: mass transport limited, desorption and surface kinetically limited regimes. Conventional GaN MOCVD is usually performed in the mass transport limited regime that occurs over a wide temperature range (600°C–1100°C). In this temperature region growth is limited by mass transport of the column III reactant to the growing interface. Because the diffusion process is slightly temperature dependent, there exists a slight increase in the growth rate in this temperature range.

MOCVD System and Reactor Design Issues

Both atmospheric-pressure and low-pressure MOCVD reactors are employed by various research and industrial groups in the growth of GaN. Atmospheric pressure reactors are favored because a high partial pressures of ammonia or nitrogen containing precursor is achievable. MOCVD Reactor design for GaN growth must overcome problems presented by high growth temperatures, prereactions, flow and film non-uniformity. Typically in GaN growth very high temperatures are required because of the high bond-strength of the N-H bond in ammonia precursors. Compounding this fact is the thermodynamic tendency of ammonia to prereact with the group-III metalorganic compounds to form non-volatile adducts. These factors

contribute to the difficulties currently facing researchers in the design and scale-up of III-V nitride deposition systems. Further research and development is needed in the scale-up and understanding of the mechanism of gallium nitride growth by MOCVD.

MOCVD Systems for Production

Currently, several types of MOCVD reactor geometries are being developed for the mass production of GaN based materials and devices. Both atmospheric pressure and low-pressure systems are being produced by the major MOCVD equipment manufacturer (Aixtron GmbH, Emcore Corp., Nippon Sanso, and Thomas Swan, Ltd. (Now Aixtron Subsidary). The two types of geometries used by Aixtron and Swan are illustrated in figure 3.2. This figure shows a closed space RDR for atmospheric pressure growth, and a two-flow horizontal flow pancake reactor. Both reactor designs are producing high quality GaN materials and it is not the intent of the author to judge one superior to the other. The benefits to each approach will be specific to the ultimate device and materials being grown.

The closed space RDR has the benefit of atmospheric pressure operation because the low free height eliminates free convection. The two-flow horizontal planetary rotationTM reactor from Aixtron can also be operated at near atmospheric pressure and can accommodate large wafer volumes (>7 wafers). The selection of any reactor has to be carefully considered against factors such as: material quality, high throughput, reproducibility, maintenance, and source usage.

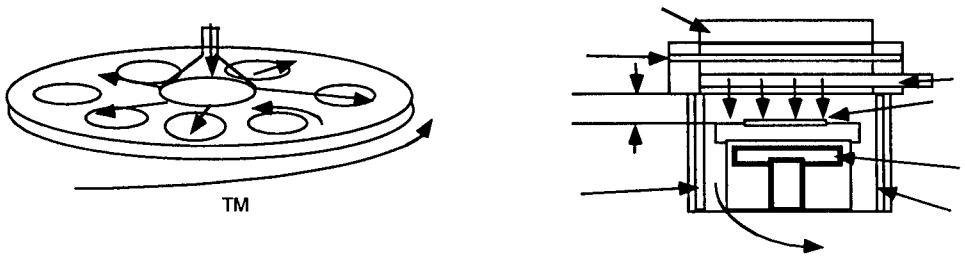

Fig. 3.2. Two types of MOCVD reactors currently produced in Europe, planetary rotating discs (Aixtron) and closed space RDR by Swan (now Aixtron)

GaN p-type and n-type doping

One of the key breakthroughs in the development of GaN technology was the achievement of p-doping using Mg and LEEBI treatment. Akasaki et al. (1989), observed that under low electron beam irradiation (LEEBI) Mg-doped GaN exhibited much lower resistivity and the PL properties drastically improved. This achievement subsequently leads to the development of p/n GaN diodes with good turn on characteristics. Nakamura et al. (1993) built upon this fundamental breakthrough to achieve even higher p-doping and uniform activation of Mg by using high temperature thermal annealing under a nitrogen ambient. The passivation requires post growth treatment for MOCVD material to activate the dopants. During the growth, interstitial hydrogen is incorporated and a H-Mg acceptor complex forms which passivates the acceptor. This H-Mg bond can be broken by a high temperature annealing step under an inert environment. This work demonstrated that hydrogen compensation of Mg in the MOCVD growth of GaN was the principal problem that plagued previous researchers. High room temperature p-doping is further complicated by the high activation energy of magnesium as the most commonly used dopant (270 meV) and the passivation of acceptors with hydrogen during CVD growth. The binding energies of dopants are dependent of the dielectric constant and effective mass of the material. The nitride system has low dielectric constant (GaN, e(0)=9.5)

and large effective masses (GaN, me=0.2 mo, mhh=0.75mo) resulting in large binding energies. This is especially pronounced in p-type doping when comparing GaN to GaAs the acceptor levels are very deep because of the large hole mass. This has led to difficulty in high p-type doping. This is the result of two effects: high n-type background concentration compensating the p-dopant and the incomplete activation of the dopants at room temperature. The low p-type doping (typical values are 1017 /cm3) leads to high contact resistance's and problems with current spreading. Further work on increasing the p-doping level and developing new p-dopants will result in substantial payoff in producing LEDs and lasers with lower operating voltages and higher power efficiencies.

Doping n-type is rather straightforward in GaN with silicon being the typical n-dopant. The as-grown material is typical unintentionally n-type, which is widely believed to be due to intrinsic nitrogen vacancies. The Si donor lies just below the conduction band (Ea = 15-25 meV). Therefore well-controlled n-type doping can be easily accomplished using silicon as the donor. The typical MOCVD precursor for n-type doping are silane (SiH4) and disilane (Si2H6) which are typical diluted with hydrogen in the 200 ppm range. Doping levels between $1(10)^{17}$ to $2(10)^{19}$ cm-3 are easily achieved in the doping of GaN with silane.

Growth of AlGaN and AlGaN/GaN Heterostructures

High quality AlGaN films have been demonstrated by atmospheric pressure MOCVD as well as epitaxy performed under low pressure conditions. At growth temperatures below 1100 °C, the mole fraction of aluminum in the AlGaN epitaxial layer was found to be almost directly proportional to the mole fraction of TMAl in the gas phase. At temperatures above 1100 °C, the incorporation efficiency of gallium atoms decreased. This behavior was explained by a decreased sticking probability of Ga molecules at this high temperatures (Hirosawa, et al. 1993).

High quality AlGaN/GaN heterostructures are characterized by a very high mobility of the two dimensional electron gas at the interface (Kahn, et al. 1991). Values as high as 1500 cm2/Vs at room temperature have been achieved in the authors' laboratory (Wu, et al. 1996). The optical properties of AlGaN/GaN quantum wells (Kahn, et al. 1990) were found to be determined by both, quantum and strain related effects (Krishnankutty, et al. 1992; Krishnankutty, et al. 1992b). MOCVD AlN films showed a full width of half maximum of the (002) x-ray rocking curve peak as low as 97 arcseconds (Saxler, et al. 1994). AlN/GaN Superlattices of high structural and optical quality have also been fabricated by switched atomic layer MOCVD (Kahn, et al. 1993).

Growth of InGaN and InGaN/GaN Heterostructures

Growth of high quality InGaN is necessary to obtain good electrical and optical characteristics from LEDs. However, the growth of high quality InGaN has proven to be more difficult than GaN. InGaN growth needs to be performed at much lower temperatures than that of GaN, due to the low dissociation temperature of InN (Matsuoka, et al. 1988; Koukitu, et al. 1996). Furthermore, the decomposition of ammonia becomes less efficient with decreasing temperature due to the high kinetic barrier for breaking the nitrogen - hydrogen bonds. The growth of InGaN has to be performed at temperatures below 850 °C because of the high volatility of indium at common GaN growth temperatures of above 1000 °C. But even on InGaN layers grown at temperatures below 800 °C, In droplet formation was observed (Shimizu, et al. 1994).

Molecular Beam Epitaxy (MBE)

Several researchers in Europe have begun developing MBE for growth of the III-V nitrides. Several approaches have been investigated for supplying an atomic source of nitrogen. RF plasma and electron cyclotron resonance (ECR) microwave plasma sources are the two most successful techniques discovered to date (Lei, et al. 1991; Strite, et al. 1991; Paisley, et al. 1989). In these systems the plasma source is used to crack molecular nitrogen. The plasma sources use a cylindrical cavity geometry to efficiently couple microwave energy into the nitrogen discharge area. The plasma stream is a complex mixture of atomic, molecular, and ionic N radicals. When using ECR sources a tradeoff between growth rate and ion damage has been observed (Lei, et al. 1991) under normal ECR use the flux of low energy reactive N species is so low that only low growth rates of 500Å/hr can be achieved. At higher microwave powers high growth rates can be achieved, but ion damage leading to deep levels and semi-insulating electrical properties is observed. A major advantage of MBE for nitride growth is the low growth temperature that can be achieved due to the

atomic nitrogen source. This is in contrast to MOCVD which must employ high growth temperatures (>1000C) to crack the ammonia molecules. The lower growth temperature should result in lower thermal stress upon cooling, less diffusion, and reduced alloy segregation. This is especially important in the AlGaN alloys which posses a large mismatch in the thermal expansion coefficient.

The GaN molecular beam epitaxy (MBE) effort at Siemens was reviewed in detail by Dr. Henning Reichert. Currently the MBE effort is shifting its focus away from optoelectronics and is emphasizing the high microwave power electronic devices. However, very good fundamental study of GaN and InGaN growth by MBE was recently carried out by Dr. Reichert. P-type doping as high as 1E+18cm-3 was achieved by MBE. This is important for low contact resistance to LED's and lasers. A high growth rate of 1.4microns/hr was achieved and mobilities as high as 460cm2/Vsec by MBE growth of GaN on MOCVD GaN templates. An impressive study of InGaN growth yielded good PL as long as 540nm. Recently single crystal InN was achieved at a growth temperature of 400C. Dr. Reichert observes at thermal decomposition temperature of 530C in MBE which is close to the value obtained by Ombacher et al in 1999. P-type GaN studies indicate activation energy of 150meV.

GaN Bulk Crystal Growth

In Poland, world-leading bulk GaN crystal growth is being achieved at Unipress. The Unipress research group is located at the High Pressure Research Center (HPRC) in Warsaw, where they employ GaN bulk crystal growth from a melt. As shown in figure 3.3 pressure as high as 10Kbar are required to growth GaN from a melt. One of the most impressive achievements the panel saw in Europe was the "defect free" bulk GaN wafers grown from melt under extremely high pressure. Dr. Isabel Grzegory gave an overview of the high-pressure solution growth method used for depositing the bulk single crystals.

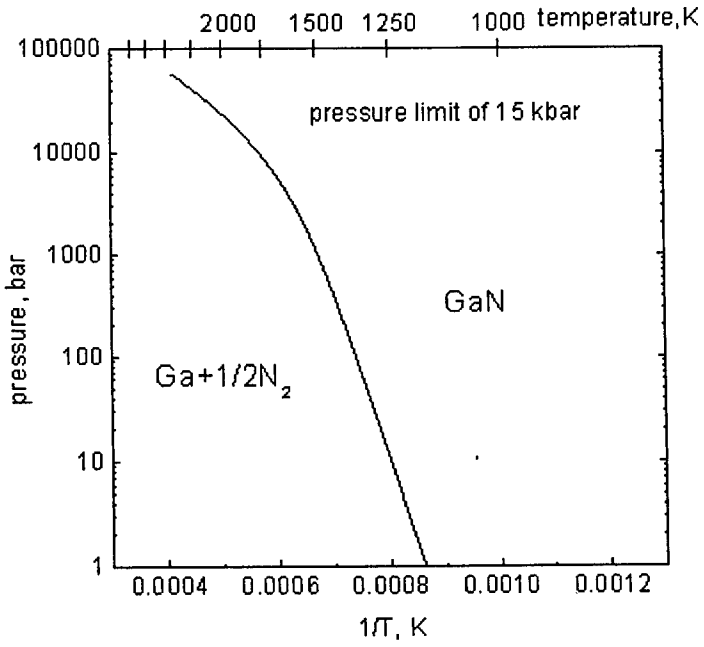

Figure 3.3. Nitrogen pressure vs. growth temperature for bulk gaN substrate growth.

The size of the substrates has steadily increased up to 1cm in 1999 from 5mm in 1997. In comparison to GaN on sapphire technology which exhibits 1e+9cm-2 defect densities, or ELO films which are in the 1E+6cm-2 to 5E+5cm-2 range the bulk GaN crystals possess 10 to 1 defect per square centimeter. Figure 3.4 shows a image of a 1cm diameter crystal grown by the Unipress group. These densities were estimated from

etch pit counts and correlated to TEM measurements of higher defect densities found on standard GaN sapphire technology. The team was allowed to observe the bulk crystals under both optical microscopes and field emission SEM. Both n-type bulk crystals and semi-insulating bulk crystal have been grown. The semi-insulating substrates were highly resistive 1E+5ohm-cm and could be used for thin film deposition of high power AlGaN/GaN microwave amplifiers (Litwin-Staszewska, et al. 1999). Very high quality homoepiatxial growth of GaN by MOCVD was obtained on top of these substrates and the films exhibited narrow double-Crystal x-ray diffraction (DCXRD) linewidths a s low as 21 arcsec. The group at University of Ulm in collaboration with Unipress has obtained thin films which exhibit the narrowest reported PL linewidths at low temperature (0.1meV) which is indicative of the uniform high quality film (Kornitzer, et al. 1999). MBE has also been performed on the bulk crystals. Both Ga-face and N-face polarity bulk substrates have been produced. The bulk crystals also display extremely smooth cleaved facets with rms roughness of 5 angstroms which would make excellent laser facets.

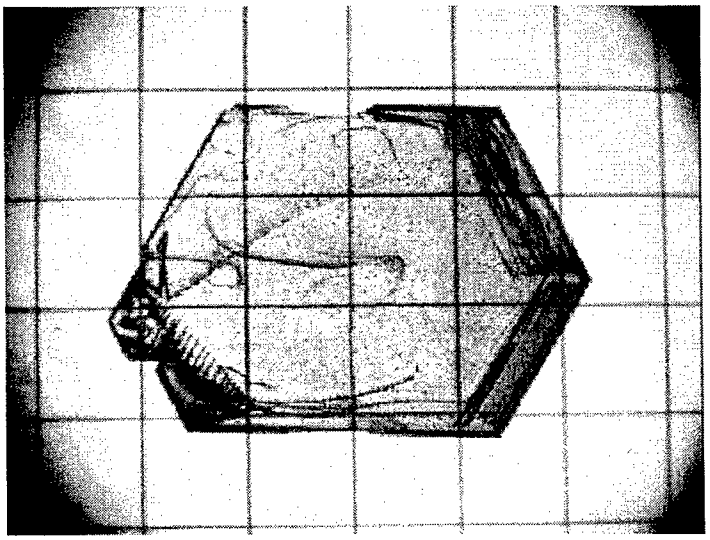

Fig.3.4. 1cm Diameter Bulk GaN Substrate

Lateral Epitaxial Overgrowth

Lateral Epitaxial Overgrowth (LEO) is an attractive method to produce GaN films with a low density of extended defects, which is beneficial both to studies of the fundamental properties of the GaInAlN materials system and to GaN-based device technology. The basic concept is to reduce defect propogation in masked regions of the substrate where the laterally overgrowing GaN is defect free. This is illustrated in the transmission electron micrograph in Figure 3.3. Recent studies in Europe, Japan and USA have confirmed that the density of threading dislocations (TDs) is reduced by 3-4 orders of magnitude in the LEO material grown on 6H-SiC (Zheleva, et al. 1997) and Al2O3 (Sakai, et al. 1997; Marchand, et al. 1998; Marchand, et al. 1998b) substrates, and the mechanisms of threading dislocations evolution during LEO have been investigated. Studies of the optical properties of LEO GaN (Chichibu, et al. 1998; Freitas, et al. 1998) and InGaN quantum wells (Rosner, et al. in press) have revealed that TDs act as non-radiative recombination centers. However, the minority carrier diffusion length (<200 nm) is smaller than the average distance between Tds such that the emission mechanisms of the carriers that do recombine radiatively appear to be unaffected by moderate TD densities (~106-109 cm-2). On the other hand, reducing the TD density has been shown to reduce the reverse leakage current by ~3 orders of magnitude in GaN p-n junctions (Kozodoy, et al. 1998), InGaN single (Mukai, et al. 1998) and multiple (Sasaoka, et al. 1998) quantum well light emitting diodes, and GaN/AlGaN heterojunction field-effect transistors (Vetury, et al., 1998) fabricated on LEO GaN. More recently, ultraviolet p-i-n photodetectors fabricated on LEO AlGaN have exhibited a similar reduction of the reverse leakage current by up to 6 orders of magnitude (Parish, et al. 1998). The use of LEO GaN has also resulted in marked improvements in the lifetime of InGaN/GaN laser diodes (Nakamura, et al. 1998).

OPTOELECTRONIC MATERIALS

LED Materials

A recent development is that Seimens has recently spun off Infineon Technologies, which will be responsible for semiconductor components. Infineon and Osram also have a joint venture (Osram Opto Semiconductors) to develop GaN blue LEDs and solid-state white lighting using GaN based LEDs. Infineon has a large GaN on SiC LED fabrication facility at Regensburg Germany. White LED products have recently been introduced by Osram under the trademarked name of TOPLED. The advances in GaN based LEDs has enabled many new markets to be opened for LEDs. Only now can one use three LEDs to tune to any color in the visible range, or even use a single blue LED in combination with phosphors to make "white LEDs". This concept is particularly attractive because the solid state nature of semiconductor devices produce very high reliability. The average lifespan of an LED is on the order of tens of years (Craford 1977). In addition, Philips Lighting BV, has also formed a joint venture with Agilent Technologies in the US, to focus on solid state lighting. Lumileds lighting is the name of the Philips JV and is 50% owned by the parent companies.

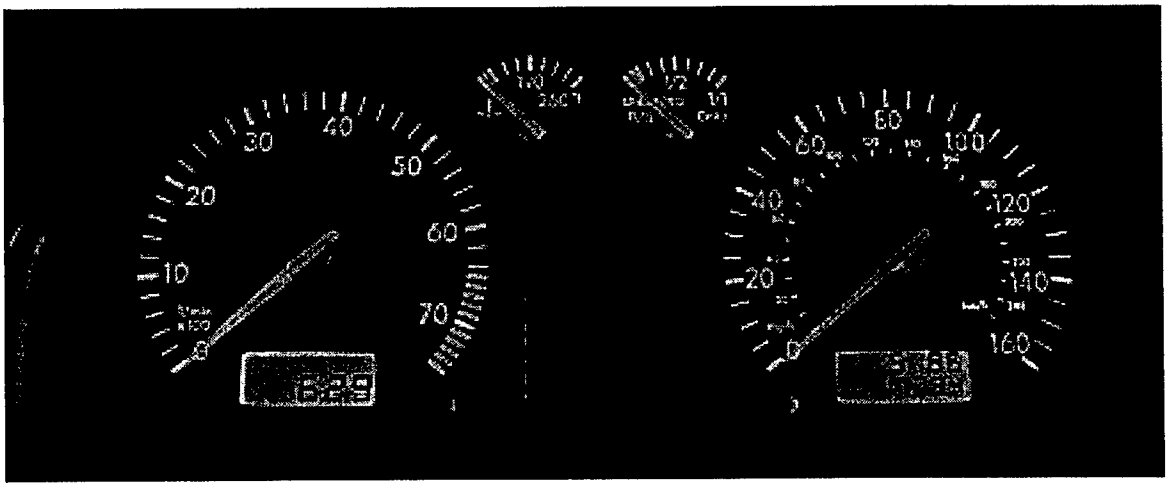

Fig. 3.5. Automotive dashboard back-lit with blue LEDs.

Full-color and white LEDs are now appearing in numerous applications ranging from in figure 3.5, Volkswagen is using blue LEDs to back-light the dashboard in the 1999 VW Passat. Another potentially large application of GaN is in for fabricating blue laser diodes (LDs) for extremely high-density optical storage systems. Because the storage density of optical compact discs (CDs) and digital video discs (DVDs) is inversely proportional to the square of the laser wavelength, a 4-8 fold increase in capacity could be realized with short wavelength laser diodes. Future research is needed to commercialize GaN for optical storage, energy efficient lighting, communications, printing, projection TV, and even surgery. As GaN manufacturing volumes increase and costs decrease one can expect to see GaN LEDs and LDs in an ever increasing number of applications wherever economical and reliable illumination is needed.

Two types of Blue LEDs are commercially available: Laterally contacted devices with quantum well (QW) InGaN active regions on sapphire substrates from Nichia Chemical Industries, Ltd., Toyoda Gosei, Hewlett-Packard Optoelectronics, and vertically contacted GaN/AlGaN double heterostructure (DH) devices on conducting SiC substrates by Cree Research, Inc. and Siemens. The SQW LEDs are extremely efficient currently. The best external efficiency achieved by Nichia for the blue and green LEDs is 10% and 12% external quantum efficiencies, respectively (Nakamura & Fasol 1997). The white LEDs are approximately 7% and have a luminous efficacy of 15 lumens/watt, which is becoming competitive with existing incandescent sources. In addition, newly developed InGaN amber LEDs are superior to conventional AlGaInP amber LEDs in terms of temperature performance. The wavelength shift as a function of temperature is much smaller in GaN than in GaAs based LEDs.

The second type of LED structure is grown on SiC substrates and is made by Cree Research Inc. These devices feature a MOCVD grown GaN-AlGaN p-n junction grown on 6H-SiC substrates. SiC has the

advantage of having a smaller lattice misfit to GaN and the possibility of providing n-doped substrates. Another advantage is the vertical conduction pathway allows for a drop in replacement part similar to the other GaP and GaAs based structures, which have the same vertical geometry. The high thermal conductivity of SiC substrates might also benefit the high temperature high output power applications of GaN LEDs.

Blue Laser Materials

Several groups in Japan, USA, and now Europe have recently reported obtaining laser diodes in the GaN materials system. Osram Opto Semiconductors was the first European group to achieve reasonable pulse blue laser performance in 1999 (HÄRLE 2000). Of all the groups in the world to date, only Nichia has obtained long-life continuous wave (CW) emission, and the laser diode was market released in January 1999. Nichia was the first company in the world to successful achieve a blue laser diode in GaN materials system. Initially the GaN laser lasted only a few seconds but reliability has improved dramatically to the current state at which Dr. Nakamura has achieved CW operation up to 10,000 hours at room temperature, elevated temperature testing at 50°C has projected the actual lifetime is in excess of 20,000 hours at 2mW. Current estimates are the reduction in the spot size which can be achieved with blue GaN lasers will yield a storage capacity of 12GB per 5.25 inch diameter discs, enough for recording a full-length motion picture in high resolution mode.

CONCLUSIONS

The Group-III nitride semiconductors have emerged as the leading material for fabricating high reliability short wavelength emitters, and emerging high power electronic devices. MOCVD and MBE are the leading growth technologies for depositing high quality GaN/InGaN heterostructure based devices. Lateral epitaxial overgrowth (LEO) and bulk crystals are some of the key technologies requiring further study to enable the next generation of GaN based devices.

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CHAPTER 4

SiC GROWTH TECHNOLOGY IN EUROPE

Michael G. Spencer

INTRODUCTION

This chapter gives a review of SiC growth technology and then discusses the results of the TTEC panel review of European growth technology.

SIC BULK CRYSTAL GROWTH

Silicon carbide substrates are the key elements in the development of SiC electronics. Because of the phase equilibria in the Si and C materials system, (specifically the material sublimes before it melts) the most popular bulk growth techniques are based on physical vapor transport. These techniques were initially developed in the late fifties and have been modified and introduced for production in the early eighties. Although sublimation techniques are relatively easy to implement, (at the high growth temperatures required) these processes are difficult to control particularly over large substrate areas.

Bulk Growth by Physical Vapor Transport

Physical vapor growth is accomplished by the sublimation of a SiC source placed in the hot zone of the growth furnace, and the subsequent mass transport of the vapor species to a cooler region of the furnace. Single crystal SiC material is formed from deposition of the supersaturated vapor species. Source materials may be composed of SiC powder, Si and C powders mechanically mixed, or crystalline SiC. The vapor transport is performed in either a vacuum or gas ambient. Single crystal growth can be realized either seeded or unseeded. Typical temperature and pressure ranges for SiC sublimation growth are 1600 to 2700°C and 10^{-6} to 20 torr, respectively. Usually, the lower temperatures are employed for sublimation epitaxial SiC growth, while bulk SiC growth is performed at the higher temperatures.

Modified Lely Process

Growth of SiC boules is possible using the modified, or seeded Lely method, also called the Tairov - Tsvetkov method (Tairov & Tsvetkov 1978; Tairov & Tsvetkov 1981) or physical vapor transport technique. In this technique, a seed crystal of SiC is introduced into the Lely chamber, and growth proceeds (usually along the **c**-axis) by vapor transport of carbon and silicon bearing species from the source (or carbon species from the graphite walls). For a typical 6H- and 4H-SiC bulk sublimation growth process, the SiC source temperature is 2100 - 2400°C (Barrett, et al. 1992), growth pressure is less than 20 Torr and the temperature gradient between source and seed ranges from 20 to 35 °C/cm. Currently the maximum commercially available 4H and 6H-SiC crystals are 2" in diameter, however record 4" boules of SiC have been recently demonstrated. Sublimation growth is usually performed on {0001} (Si or C face) of either 6H-SiC or 4H-SiC seeds. Growth on faces perpendicular to the (0001) basal plane has also been reported (Takahash, et al. 1994) in an effort to reduce micropipe defects.

Vapor phase equilibria in SiC

The equilibrium gas species over SiC have been measured by Drowart et. al. (1958; 1960) and Behrens and Rinehard (1979). The principal molecular species are Si, SiC_2, and Si_2C. In the Si-C vapor system, carbon is transported by the Si bearing compounds. The vapor pressure of all the major species are related to the pressure of Si. In thermal equilibrium, the vapor equilibria over SiC has only one degree of freedom. If any of the species are specified by the temperature, source powder composition and/or crucible wall interactions the remaining species are uniquely determined. Because Si bearing species are the most prevalent, it is usually convenient to discuss the vapor composition in terms of Si partial vapor pressure. Using the experimental data together with thermodynamic calculations, the relationship between the partial pressure of Si and that of Si_2C and SiC_2 for the SiC-C vapor equilibria is given by Eqns 1 and 2 (Glass, et al. 1997):

$$P_{Si_2C} = 2.85x10^2 e^{(-1.79x10^4/T)} x P_{Si} \qquad (1)$$

$$P_{SiC_2} = 9.41x10^{28} e^{(-14.35x10^4/T)} \frac{1}{P_{Si}} \qquad (2)$$

The partial pressure of the vapor species varies dramatically between the SiC- C equilibrium and the SiC-Si equilibrium. However, due to the large amount of carbon present in the growth chamber of most systems, the vapor interactions with the graphite walls of the crucible usually will cause the system to operate close to the SiC-C part of the curve. Since the composition of the vapor has such a large allowed existence region, the composition of the powder has important consequences for the vapor composition and the growth rate. Source graphitization is also an important problem for bulk growth. Graphitization occurs under growth conditions when it is possible to preferentially lose Si and obtain a carbon layer over the source which prevents further sublimation of the source. This has been treated in detail by Karpov et. al. (1995).

Growth Rate

Typical growth rates for the bulk growth of SiC are in the range of 0.5-5 mm/hr.

Structural defects

There has been significant progress in the quality of material produced by seeded sublimation technology (Hobgood, et al. 1993; Tsvetkov, et al. 1995). Dislocation density and micropipe density in SiC bulk crystals grown by the modified Lely method currently range from 10^3 to 10^4 cm^{-2}. Other types of crystal defects found in sublimation grown SiC crystals include basal plane tubes, cracks, and crystal domains (Tuominen, et al. 1994). However, micropipes are defects unique to the growth of SiC. These micropipes which are physical holes can travel large distances in the crystal. It was shown that micropipes are "killer" defects if they intersect the active regions of a device (Neudeck & Powell 1994). The density of the micropipes could be correlated with domains in the crystals (Glass, et al. 1997). These domains are thought to be related to growth spirals which are nucleated and interact. The relationship between micropores and growth spirals was originally suggested by Frank (1951), and later papers on the subject by Krishna et. al. (1985) have expanded on this theme. More recently, x-ray studies by Fazi et. al. (1993) also has suggested this mechanism. There are, however, other views as to the origin of the micropipe defects. Some have observed that these defects are nucleated at the seed. Other investigators suggest that impurities, inclusions (or Si droplets) are responsible for micropipe formation. Support of alternate views of micropipe formation comes from the experimental observation that many of these defects are nucleated in the bulk of the materials and are not continuous. It is generally conceded that micropipes are the most important current obstacle to the production of high quality SiC devices. The possible mechanisms of micropipe formation are summarized by Tsvetkov et. al. (1995).

Recently, x-ray and TEM techniques have been applied to the study of the quality of bulk SiC (Barrett, et al. 1993). Lely platelets as well as substrates grown by the modified Lely method have been investigated. In general, the results of various investigations suggest that Lely crystals exhibit higher material quality. The full width at a half maximum (FWHM) of the x-ray rocking curve is ~7-10 arc sec for Lely platelets, while for modified Lely crystals this value ranges from 20-100 arc sec. For Lely crystals, a single x-ray diffraction peak is observed for each x-ray reflection. Conversely for modified Lely crystals several peaks are observed indicating a mosaicity in the material.

Electrical characteristics

Undoped SiC bulk material usually is contaminated by nitrogen which produces n-type conductivity. The typical background level of electron concentration at room temperature for undoped SiC crystals grown by modified Lely method is 10^{16} -10^{17} cm^{-3}. High purity undoped SiC crystals with room temperature resistivity from 10^2 to 10^3 • cm have been reported by Hobgood et. al. (1993). These crystals had p-type conductivity with a background carrier concentration of 10^{15} cm^{-3} due to residual boron impurities.

N-type SiC crystals with carrier concentrations up to 10^{20} cm^{-3} were produced using nitrogen doping (Onoue, et al. 1995). The minimum reported resistivity for 6H-SiC and 4H-SiC bulk crystals are 1.6 m• cm and 2.8 m• cm, respectively (Glass, et al. 1997). No information on defect density in highly doped n-type material is available. P-type SiC crystals with carrier concentrations up to 10^{20} cm^{-3} were obtained using aluminum doping (Glass, et al. 1997). Information about Al doping during bulk SiC growth is limited. No information on defect density in highly doped p-type material is available.

Semi-insulating 6H-SiC crystals were produced using vanadium doping (Hobgood, et al. 1995). The amount of vanadium soluble in the material is limited by the precipitation of vanadium silicide. The material resistivity at room temperature can be estimated by high temperature resistivity measurements and was determined to be in the range of 10^{15}•• cm. Semi-insulating 4H-SiC crystals with comparable resistivities have also been reported (Tsvetkov, et al. 1995; Glass, et al. 1997).

Bulk growth by chemical vapor deposition

6H-SiC crystals have been grown by high temperature CVD with growth rates of 0.5 mm/hr (Kordina, et al. 1996). This technique is a direct adaptation of the CVD epitaxial technique for growth of SiC. The control of the Si/C ratio in such a system is excellent compared with sublimation growth and additional results have been presented in the recent SiC conference.

Bulk Growth from the Liquid Phase

Crystal growth from melt-solutions is widely used for many semiconductor materials. Liquid phase growth of SiC has not been considered promising based on results obtained during the early stage of SiC development. Two main objections to liquid phase technology are low solubility of SiC in the Si melt (which limits the growth rate), and inclusions incorporated in grown crystals due to parasitic phase formation. On the other hand, it has been shown that high quality SiC can be grown from melt-solutions (Nelson. Et al. 1966; Marshall 1969; Wolff, et al. 1969): undoped cubic SiC crystals grown from a silicon melt at ~1500°C exhibited a mobility of 980 cm^2/V s and carrier concentration of $4x10^{16}$ cm^{-3} (300 K). Significant progress has also been made in understanding the nature of SiC growth from liquids (Dmitriev 1995; Yakimova, et al. 1995). It has been shown that high quality SiC epitaxial layers with no micropipes and low dislocation density can be grown from a Si melt (Rendakova, et al. 1997). Epitaxial layers of 6H- and 4H-SiC were grown from Si melts on 35 mm diameter substrates indicating the possibility of liquid phase growth of large crystals. It was also found that the solubility of SiC in Si melt does not severely limit the growth rate, and a SiC growth rate of about ~0.2 mm/hr has been obtained at 1650°C.

SIC EPITAXIAL GROWTH

In order to improve the quality of bulk material and produce complicated device structures, epitaxial techniques are necessary. As with other semiconductor material systems, liquid phase epitaxial techniques and CVD were used early in the development of SiC to produce device structures. Although the material produced by LPE was of high quality, difficulties with molten Si (used as the melt) prompted the development of vapor phase techniques such as sublimation epitaxy and CVD. Chemical vapor deposition is presently the most widely used epitaxial technique for growth of SiC device structures.

Chemical Vapor Deposition

Chemical vapor deposition is a growth process in which gaseous compounds are transported to the substrate surface where chemical reactions occur resulting in formation and growth of the desired material. The growth of 6H-SiC layers on 6H-SiC {0001} substrates by CVD in the temperature range from 1500 to 1850°C have been reported since the sixties (Campbell & Chu 1966; Jennings, et al. 1966; Minagawa & Gatos 1971; Wessels, et al. 1974; Matsunami, et al. 1975; Muench, et al. 1975; Muench & Pfaffeneder 1976; Nishino, et al. 1978). A significant lowering of the growth temperature and improvement of material quality has been achieved by using substrates which are mis-oriented a few degrees off the {0001} plane toward the $<11\bar{2}0>$ direction. This growth on mis-oriented substrates has been termed "step controlled epitaxy" and has the added advantage of stabilizing the polytype structure.

A review of CVD growth of SiC has been published by Nishino (1995) and Larkin (1997). Growth temperatures for typical SiC CVD processes range from 1200-1800°C while growth pressures vary from 100-760 torr.

Growth Equipment

Three types of growth apparatus are used for SiC CVD: 1) cold-wall horizontal atmospheric pressure reactors have been used for many years with results reported by Siemens AG (Karmann, et al. 1993), Kyoto University (Matsunami 1992), NASA Lewis Research Center (Mandel 1962). A commercial horizontal water-cooled reactor for SiC CVD operating in the pressure range from 10 to 1000 mbar was developed by AIXTRON GmbH (Sculte, et al. 1994). This system uses low pressure and a specially designed inner sleeve to maintain laminar gas flow. 2) hot-wall horizontal atmospheric pressure reactors have been designed at Linkoping University (Kordina, et al. 1993). Still another hot wall horizontal reactor design was proposed by the Industrial Microelectronic Center in Sweden (Nordell, et al. 1995). 3) cold-wall vertical low pressure reactors (Feng, et al. 1996) have been built commercially by EMCORE Corp. and used at Howard University and Siemens AG (Rupp, et al. 1995). In these reactors, laminar flow is obtained by a high speed rotating disk (in conjunction with high gas flow velocities) which produces a pumping action.

High temperatures in SiC epitaxial reactors can be obtained with either resistive or rf heating. In most systems the susceptor is made from graphite. Because of the reaction between graphite and H_2 at temperatures in excess of 1300°C a thin SiC coating layer has been used by many researchers. Unintentional incorporation of contaminants from the susceptor during SiC CVD was studied by Karmann and coworkers (Karmann, et al. 1995). In these experiments, 6H-SiC layers were grown in an atmospheric pressure reactor at 1390°C with a growth rate of 0.7 •m/hr. Uncoated and SiC coated (100 - 120 •m thick) graphite susceptors were used for comparison. For the uncoated susceptors, the layers were found to be contaminated with aluminum, boron and nitrogen. Conversely, using a SiC coated graphite susceptor in the same system, SiC layers with concentration $N_d - N_a$ of $4x10^{15}$ cm^{-3} could be grown. In a low pressure vertical reactor with high speed substrate rotation, SiC with background concentrations in 10^{14} cm^{-3} range was demonstrated without use of SiC-coated parts (Rupp, et al. 1995). This low amount of contamination is attributed to the favorable gas flow patterns generated in this reactor

Temperature measurement is a major equipment issue for CVD growth at high temperatures. During growth, substrate temperature is usually measured by an optical pyrometer calibrated by melting of Si or Ge. The temperature of the susceptor typically is found to be 50 - 100°C higher than that of the SiC substrate. Power settings are often used to calibrate the substrate temperature.

Precursors and Reaction Chemistry

A number of precursors have been used for the growth of silicon carbide. For transport of the Si species the most popular choice is SiH_4 (Powell, et al. 1987), but Si_2H_6 (Nishino & Saraie 1989a) and $SiCl_4$ (Muench & Pfaffeneder 1976) have also been used. For growth of Si, the hydrocarbon species most reported is C_3H_8. However, there are also reports of SiC growth using C_2H_2 (Liaw & Davis 1985), CH_3Cl (Ikoma, et al. 1991), CH_4 (Rai-Choudhury & Formigoni 1969), CCl_4, C_7H_8, or C_6H_{14} as carbon sources. In addition to the use of individual gas species, single precursors have also been investigated, among them CH_3SiCl_3 (Nishino & Sarate 1989b) and $(CH_3)_2SiCl_2$ (Rai-Choudhury & Formigoni 1969).

Gas-phase equilibrium calculations were reported for Si-H-C gas mixtures (Allendorf 1993) in the temperature range used in CVD growth of SiC. Modeling of the gas phase chemical processes which occur during growth as a function of distance from the heated susceptor was reported by Stinespring and Wormhoudt (Stinespring & Wormhoudt 1988). The results of the modeling study shows that the injected C species are not fully decomposed to equilibrium values at the growth interface. Gas-phase reactions in SiC CVD growth using the SiH_4-C_3H_8-H_2 gas system were experimentally investigated by Hong et. al. (1993) using a microcavity technique. The microcavity study suggested 1) that multiple species contribute to the film growth in the system, and 2) possible precursors in the chamber contain SiH_2 (a gas-phase intermediate derived from SiH_4), and another species containing Si and C derived from SiH_2 and C_3H_8. Under certain experimental conditions Si droplets and graphite inclusions have been observed in SiC epitaxy. Modeling of these Si-droplets and graphite inclusions formation in the CVD process was done (Karpov, et al. 1995) considering several homogeneous and heterogeneous chemical reactions.

Growth Rate

Increasing the growth rate in SiC epitaxy is important because of the demands of SiC power device structures. A typical base layer in a power thyristor can be as thick as 100 •m. Since growth rates of SiC films vary from 0.1 to 6 •m/hr for a growth temperature of 1500°C, the minimum growth time for a single structure can be as long as 15 hours. Growth under normal conditions is determined by the diffusive transport of the Si species through the stagnant layer, although control of the growth by carbon species has been observed. Since the growth rate of 6 mm/hr is too low for layers greater than 10-12 •m there are several studies in progress on increasing the CVD growth rate. Growth rates of 500 •m/hr were obtained by high temperature CVD (1800 to 2300°C) (Kordina, et al. 1996) with a maximum crystal thickness of 2 mm. This result looks very promising for growth of thick layers (>100 •m) for high power SiC devices, but many questions about this technique, including possible material contamination at high temperature, remain unanswered.

The temperature dependence of SiC CVD growth rate has been investigated by several researchers. If the growth rate is determined by surface kinetics, the activation energy of the growth is expected to be relatively large. If on the other hand the growth is transport limited, the observed activation energy is expected to be small. For the $SiCl_4$-CCl_4-He gas system, an activation energy of 20 kcal/mol was reported for growth on well-oriented substrates (Jennings, et al. 1966). An activation energy of 22 kcal/mol was obtained for SiC growth on the $(000\bar{1})$C face of well-oriented substrates for the C_3H_8-SiH_4-H_2 gas mixture (Wessels, et al. 1974), however the same investigators observed a complicated temperature dependence on well-oriented (0001)Si faces. The complicated temperature dependence of growth rate on the Si face was explained using a growth model in which the growth rate is limited by the adsorption-desorption of reactants at the growth interface. For step-controlled epitaxy an activation energy of SiC growth rate was measured to be 3.0 kcal/mol (Kimoto, et al. 1993). The layers were grown at atmospheric pressure in the temperature range from 1200 to 1500°C on 6H-SiC {0001} substrates (with 6° off-orientation) using SiH_4-C_3H_8-H_2 precursors. The small value of activation energy is attributed to the fact that the growth in step-controlled epitaxy is mass transport limited and the temperature dependence is due diffusion through the stagnant layer.

Homoepitaxy of •-SiC

Homoepitaxial growth of •-SiC (6H-SiC, 4H-SiC, 21R-SiC) by CVD has been advanced at Kyoto University using off-oriented SiC substrates (Itoh, et al. 1994; Hong, et al. 1995). This technique is called step-controlled epitaxy because the growth process is determined by the lateral growth rate of the terraces. The growth rate, substrate mis-orientation and growth temperature determine if growth will occur via the step controlled mechanism. If the growth is step controlled, the epilayer will replicate the stacking order of the substrate. The growth mechanism for SiC homoepitaxial CVD has been discussed by a number of researchers (Kimoto, et al. 1993; Kimoto & Matsunami 1993; Hong, et al. 1995). Nucleation processes during SiC CVD growth were investigated by Kimoto and Matsunami (1993) and the surface kinetics of adatoms in CVD growth of SiC were analyzed based on Burton-Cabrera-Frank theory (Kimoto & Matsunami 1994).

Typical growth of epitaxial 6H-SiC is performed on wafers which are mis-orientated 3.5° toward the $<11\bar{2}0>$ direction. The growth temperatures are about 1500°C. 6H-SiC is usually grown with large amounts of H2 in the chamber, gas ratios of 1:1000 (SiH4+C3H8):H2 are usual. 4H-SiC layers are typically grown (the growth is performed at temperatures somewhat higher than those used for 6H growth) on 5-8° off-oriented 4H-SiC substrates using the same gas system. The (0001)Si face 4H substrates are misoriented toward the $<11\bar{2}0>$ direction. A typical growth rate is about 2.5 •m/hr.

At high growth temperatures (1500°C or greater) used for 6H-SiC and 4H-SiC deposition, a wide range of Si/C ratios have been used (Rupp, et al. 1995b). The Si/C ratio affects not only the growth rate and crystal quality but also the dopant incorporation. A major problem in the epitazial growth of SiC is the unintentional incorporation of C in the gas phase which comes from various parts of the reactor. This unintentional C is transported to the substrate via reaction with H2 in the gas stream and the subsequent formation of hydrocarbons makes it difficult to maintain a proper Si/C ratio.

Details of several epitaxial growth processes have been published. A growth process employing the SiH4-C2H4-H2 gas system was described by researchers from North Carolina State University (Wang & Davis 1991). In this process, SiC substrates were initially heated to the growth temperature (1350-1600°C) for 10 minutes in H2 flow to clean the surface. In the growth procedure developed at NASA Lewis Research Center (Powell, et al. 1995) for 6H-SiC and 4H-SiC CVD, the samples are initially etched by HCl at 1350°C prior to the growth. The initial HCl purge reduces the density of surface defects in resulting SiC layers. The importance of pre-growth treatment of the substrates was emphasized in this study. A high resolution x-ray diffraction study on 6H-SiC layers grown by CVD (Bakin, et al. 1995) also demonstrated the importance of pre-growth treatment. The layers in the study were grown in the temperature range from 1500 to 1600°C with the growth rate of 2 to 2.5 •m/hr using a C/Si ratio of 2.5 to 3. Prior to the growth, the substrates were etched in H2 gas flow at 1500-1600°C for 10 - 30 min. A 9 arcsec full width at the half maximum x-ray rocking curve was obtained for layers grown on substrates having a FWHM of 72 arcsec. Without H2 etching, the FWHM for the layer was often observed to be larger than the FWHM of the substrate.

All the CVD processes discussed up to this point were developed for SiC deposition on polar {0001} (C or Si face) substrates. Epitaxial growth of SiC has also been investigated on the two nonpolar crystal planes, namely, the $(10\bar{1}0)$ and $(\bar{1}2\bar{1}0)$ planes (Burk, et al. 1993).

Structural Properties

The surface of SiC epitaxial layers can contain a large number of imperfections. Surface defects observed in SiC CVD layers are growth pits, polytype inclusions (which sometimes appear as triangular features), macro-steps (often referred to as step bunching), and micropipes. Some of these defects are relatively large (tens of microns), while others have an average size less than one micron.

Attempts to understand the nature of surface defects in SiC CVD layers have appeared in several recent studies (Burk, et al. 1996; Powell, et al. 1995; Powell, et al. 1995b; Powell, et al. 1996; Kimoto, et al. 1993d; Rupp, et al. 1995; Rupp, et al. 1995b). A large number of factors influence the production and density of

surface defects. These include substrate characteristics (orientation, face polarity, tilt angle, crystallographic direction of the misorientation), mechanical and chemical treatment of the substrate before the epitaxy, substrate pre-growth treatment in the reactor, and growth conditions such as Si/C ratio, growth rate, and growth termination procedure. The best reported results thus achieved indicate surface defect densities of 10^3 cm^{-2}. It is noteworthy that this value corresponds to the density of unknown defects in SiC pn structures which appear to cause pre-mature junction breakdown (Chelnokov, et al. 1996). Investigation of surface defects in 6H-SiC and 4H-SiC layers have shown that the morphological defect density varies widely from run to run.

Growth pits are a common morphological defect observed in the growth of SiC. The relationship between growth pits on the epitaxial layer and surface imperfections in the starting substrates has been studied by Powell et. al. (Powell, et al. 1995). It was concluded that the main factor in the formation of growth pits is the polishing and preparation of the substrate rather than bulk defects such as micropipes and dislocations. This conclusion has lead to improved substrate polishing techniques such as the use of colloidal silica for chemo-mechanical polishing (Powell, et al. 1997).

Step bunching (which is the combination of atomic steps on the surface to form large macro-steps) often occurs in the CVD growth of SiC. Results on the initial investigations of step bunching on 6H-SiC epitaxy (which enhances terrace nucleation) was discussed by Kong et. al. (1988). Step bunching in 6H- and 4H-SiC growth by step-controlled CVD on mis-oriented {0001} substrates was investigated by AFM and TEM techniques (Kimoto, et al. 1993d). In this study, the SiC {0001} substrates were mis-oriented 3-5° toward the $<11\bar{2}0>$ irection. It was observed that epitaxial growth on (0001)Si face yielded macrosteps with an average terrace width of 280 nm and an average step height of 3 nm. On the $(000\bar{1})$C face, the surface was relatively flat and no microsteps were observed. On the (0001)Si faces, 3 bilayer-height steps were the most dominant type of step seen using 6H-SiC samples while 4 bilayer-height steps predominated on 4H-SiC samples. Step bunching as a function of tilt angle (0.1-3.5°) was studied by Powell et. al. (1995b) with a conclusion that step bunching in epitaxial growth can actually be reduced at higher substrate mis-orientations. A TEM study as well as a qualitative model of the step bunching phenomena was reported by Chein et. al. (1994). In their model, Chein and co-workers show that variations in the surface energies of the different steps which comprise the 6H unit cell are responsible for the different lateral growth velocities and consequently the step bunching.

Typical 4H-SiC and 6H-SiC epitaxial layers also contain dislocations and micropipes. In all cases in which micropipes were observed at an layer/substrate interface, the micropipes originated in the substrate and propagated into the epitaxial layer (Powell, et al. 1993). This result implies that if micropipes in the substrate are eliminated or closed (such as by liquid phase techniques), the epitaxial films will be micropipe free.

Polytype inclusions are a common type of crystalline defect in 6H and 4H-SiC epitaxial layers grown by CVD These polytype inclusions (usually 3C-SiC) are formed due to nucleation on terraces or dislocation sites. It was found that with proper pre-growth surface treatment with HCl etching, 6H-SiC layers without 3C-SiC inclusions can be grown by CVD on {0001} 6H-SiC substrates with small tilt angles (0.1°-0.6°) (Powell, et al. 1991). Conversely if a pre-growth HCl etch at 1375°C for 20 minutes was used, predominantly 6H-SiC growth was obtained. The etching process appears to be effective in removing unintentional 3C nucleation sites on 6H-SiC wafers. However, deviation from the optimal etching conditions lead to 3C-SiC growth on the 6H-SiC substrates. It was also found that 4H-SiC homoepitaxial layers are more susceptible than 6H layers to 3C inclusions (Powell, et al. 1995). The mechanism of cubic SiC nucleation on off-axis 6H and 4H substrates has been investigated by Hallin et. al. (1995). These investigators showed that the 3C-SiC nucleation occurs via the formation of triangular stacking faults at substrate imperfections. In 6H-SiC, these defects are usually found in on-axis material where the probability for 2-dimensional nucleation of 3C-SiC is increased. In 4H-SiC epitaxial layers, 3C-SiC inclusions having a triangle shape are found even if substrates have a tilt angle of 3.5°. In order to reduce the density of inclusions in 4H material, a 8° tilt angle was found to be necessary. In the 4H-SiC epitaxial layers grown on 8° off-substrates, the 3C-SiC inclusions are almost eliminated.

Although some progress has been made in understanding the nature and cause of structural defects such as step bunching and polytype inclusions, the origin and control of many defects in epitaxial SiC remains to be investigated.

Electrical Properties

Significant progress has been achieved in producing epitaxial layers of 6H and 4H-SiC with superior electrical properties. 6H-SiC epitaxial layers having a low background doping concentration were grown and characterized by Kordina et. al. (1994). It was shown that using propane as a carbon precursor uncompensated SiC layers with donor concentrations less than 10^{15} cm^{-3} may be grown, whereas with methane uncompensated layers can be produced with electron concentrations in the mid 10^{14} cm^{-3} range (however with a slightly worse morphology). The optimal growth temperatures for these films was found to vary between 1550 and 1600°C. At higher temperature, contamination from graphite parts became noticeable and bake-out of the growth system had a significant impact on the background doping. The effect of unintentional hydrogen doping by CVD was studied by Clemen et. al. (1993).

4H-SiC layers with electron concentrations as low as $2x10^{14}$ cm^{-3} were reported (Kordina, et al. 1994; Itoh, et al. 1993; Kimoto, et al. 1995) (to obtain the low impurity concentration, the growth system was pumped for several hours prior to growth according to some of the authors). Electrical and optical measurements on high quality 4H-SiC layers were reported by Kimoto and co-authors (1995). The background doping concentration in the layers was determined to be $3x10^{15}$ - $2x10^{16}$ cm^{-3} and electron mobility in the {0001} basal plane was 600 - 720 cm^2/V s (300 K). Deep level transient spectroscopy (DLTS) measurements on these films showed that the concentration of electron traps was approximately 10^{13} cm^{-3} independent of substrate polarity. Minority carrier lifetimes have been measured on 6H-SiC layers with N_d - N_a ranging from 10^{14} to 10^{17} cm^{-3}. Lifetimes as high as 0.45••s (300 K) have been achieved for thick low doped samples (Kordina, et al. 1995a). However the maximum reported values of minority carrier diffusion length for CVD grown SiC pn structures do not exceed 3 •m.

Doping of SiC homoepitaxial layers grown by CVD has been reported in numerous publications. Nitrogen is commonly used as a donor and aluminum is the acceptor of choice. Nitrogen doping has been investigated for several years as a n-type dopant (see for example Rupp, et al. 1995b; Karmann, et al. 1992). Nitrogen doping in these studies produced donor concentrations ranging from 10^{16} to 10^{19} cm^{-3}.

P-type doping has been achieved by using Al as a dopant (see for example Nordell, et al. 1995). Epitaxial layers in this study were grown using SiH_4-C_3H8-H_2-TMA (Trimethylaluminium) precursors at a C/Si ratio of 2.5. The reactor pressure was 800 mbar and growth temperature was 1550°C. A growth rate was about 2 •m/hr. The atomic Al concentration in 6H-SiC was controlled from 10^{17} to 10^{21} cm^{-3}. When the Al concentration exceeded $2x10^{20}$ cm^{-3}, impurity banding occurred and the Al acceptors were completely ionized while 1% ionization was observed at lower doping levels (in keeping with the measured Al ionization energy of ~0.25 eV). Schoner and coworkers (1995) found that the Al ionization energy varied with doping concentration as well as the degree of compensation. As expected, at high doping levels crystal quality was degraded.

A greater range of doping control is possible with site-competition epitaxy (Larkin, et al. 1993, 1994; Larkin 1995). The method is based on varying the Si/C ratio within the CVD reactor in order to control the dopant incorporation in SiC during epitaxial growth. Site-competition epitaxy has been used for control of nitrogen, phosphorus, aluminum and boron incorporation in 6H-SiC and 4H-SiC films. The layers were grown using SiH_4-C_3H_8-H_2 gas precursors at 1450°C with a typical growth rate of 3-4 •m/hr. Secondary ion mass spectroscopy (SIMS) determined that the Al incorporation increased as the propane flow was increased and also when the silane flow was decreased. It was found that results of site-competition doping control is similar for 6H-SiC and 4H-SiC epitaxial layers grown on (0001)Si faces of the substrates. The effect of surface polarity and the chemistry of the particular impurity on site-competition doping control are discussed by Larkin (1995). Deep-level impurities in SiC pn structures grown by site-competition epitaxy have also been investigated also by Saddow et. al. (1995).

Impurity memory effects on dopant concentration profiles in 4H and 6H-SiC were investigated by SIMS (Nordell, et al. 1997). It was found that dopants were absorbed by the reactor walls and re-evaporated after the dopant precursor flow was switched off. These memory effects limit the doping control range to about three orders of magnitude for aluminum, and two orders of magnitude for boron. The dynamic range for Al doping was increased up to five orders of magnitude by controlling the Si/C ratio and using HCl etching during the 10 min growth interruption after gas switching. For boron, a dynamic range of more than three orders of magnitude was obtained. Doping spikes at the substrate/layer interface were also reduced by an in situ HCl etch (Burk, et al. 1996).

Liquid Phase Epitaxy

SiC LPE growth takes place from a supersaturated solution of Si and C in a melt solvent. The main feature of LPE is that the growing films are in equilibrium with the liquid phase. The endpoints of the process are determined by the phase diagrams for Si, C and the solvent material. Liquid phase epitaxy was used early in the development of SiC technology. Growth from Si melt as well as alloy melts were demonstrated. LPE has been performed in graphite boats, by vertical dipping and by a novel levitation process called container-free epitaxy. Doping of SiC was accomplished in LPE over a large range of concentrations. Due to the difficulty in control of surface morphology, LPE techniques have lost ground in favor of CVD approaches. However, recently discovered unique properties of LPE such as micropipe closing (Yakimova, et al. 1995; Rendakova, et al. 1997) and the ability to produce very heavily doped p-type films ($>5x10^{20}$ cm^{-3}) (Rendakova, et al. 1997) may secure this technology a future role. The usual melt for SiC LPE is silicon, but alternative materials like Sn, Ge, Ga, and their mixtures are also used for SiC LPE (see Dmitriev 1995 for a review).

Sublimation Epitaxy

The mechanism and principals of SiC sublimation epitaxy are similar to those for bulk SiC sublimation growth discussed at the beginning of this chapter. However, sublimation epitaxy is usually performed at lower temperatures with smaller growth rates and for shorter time periods than bulk SiC sublimation growth. Growth of epitaxial SiC using the sublimation process had been the subject of many early investigations (for early work, the reader is refereed to the Proceedings of 1st, 2nd, and 3rd International Conferences on Silicon Carbide0. The breakthrough in sublimation epitaxial technology was achieved with the development of "sublimation sandwich method" by Vodakov and Mokhov (1970). They employed a nearly flat source positioned close to the substrate and performed the growth under near-equilibrium conditions. This method allowed for the vapor equilibrium to be constant over the substrate. The "sublimation sandwich method" made it possible to grow high quality SiC layers in the temperature range 1600 - 2100°C (Vodakov, et al. 1979; Mokhov, et al. 1992; Tairov, et al. 1976; Anikin, et al. 1992). An excellent review on SiC sublimation epitaxy was written by Konstantinov (1996).

ION IMPLANTATION IN SIC

Ion implantation currently is the only alternative to doping during growth and is widely used in SiC device fabrication technology. For a review of ion implantation in silicon carbide see Davis, et al. 1991; Ivanov & Chelnokov 1992; and Wongchotigul 1995. Ion implantation has been used for: 1) pn junction formation (Anikin, et al. 1984; Ramungul, et al. 1995; Shenoy & Baliga 1995; Xie, et al. 1995; Wang, et al. 1995; Palmour, et al. 1995), 2) light emitting diode fabrication (Gusev, et al. 1983), 3) highly doped contact layers (Spieb, et al. 1995; Slater, et al. 1995), (4) field effect transistors channels (Alok & Baliga 1995; Slater, et al. 1995) and (5) device isolation and termination (Nadella & Capono 1997).

Since the sixties, many elements have been implanted into silicon carbide (Al, B, Ga, In, Tl, N, P, Sb, Be, Bi, Kr, Ar, Er, Si, C) (Leith, et al. 1967; Dunlap & Marsh 1969) although, the most commonly used are Al, B, and N. Ion implanted dopant activation is achieved by thermal annealing using resistively or rf heated furnaces (Gardner, et al. 1997). Excimer laser activation has also been reported (Ahmed, et al. 1995). Simulation of implantation profiles in SiC and their comparison with experimental results has been performed (Ahmed, et al. 1995; Pan, et al. 1997).

N-type doping by ion implantation has been developed into a production process. Annealing of nitrogen implantation has in general resulted in low residual damage due to the small size of the nitrogen atom. Nitrogen ion implantation is usually performed in 6H-SiC at elevated temperatures. Annealing at 1500 and 1600°C for 15 min performed in SiC crucibles results in Reserford back scattering yields at the virgin crystal level indicating a good recovery of the crystalline quality. Recently, activation processes of high-dose ($3.8x10^{15}$ and $7.1x10^{15}$ cm^{-2}) nitrogen implants into 6H-SiC has been investigated (Pan, et al. 1997). It was shown that low resistivity of the implanted material can be obtained after long time (2000 min) anneals at 900°C.

One of the current problems in ion implantation technology is activation of the p-type dopants. Because Al is a large atom, higher annealing temperatures and times are required to produce device quality p-type layers. Amorphization and re-crystallization of Al-implanted 6H-SiC were investigated (Pan, et al. 1997). Ion implantation was performed in n-type 6H-SiC in the temperature range from room temperature to 1000°C. Al ions were implanted with a dose ranged from $5x10^{13}$ to $5x10^{16}$ cm-2 and implant energies of 180 and 360 keV into 6H-SiC epitaxial layers having doping concentrations of $1x10^{16}$ cm^{-3}. After implantation, the samples were annealed between 800 and 1600°C for 30 min in an Ar flow. It was shown that density of defects induced by implantation decreased exponentially with implantation temperature. However residual defects were detected even after annealing at 1600°C. At 1600°C anneal temperature, sublimation of SiC was observed. Carrier concentration and mobility were found to be independent of the implantation temperature and the carrier concentrations at room temperature was measured to be about 5% of implanted dopant. The measured hole mobility was less than 1 cm^2/Vs (300 K). Annealing p-type implants at lower temperatures has proven ineffective. For example, annealing at 1400°C resulted in hole concentration of only $5x10^{17}$ cm^{-3} (Rao, et al. 1995). Also C or Si co-implantation also did not improve Al activation efficiency (Rao, et al. 1995). Experimental data on ion implantation in other than 6H polytype are limited.

RESEARCH ON SIC GROWTH AND PROCESSING IN EUROPE

In this section the results of the TTEC panel trip to Europe will be discussed. In this chapter the efforts on SiC growth and processing will be highlighted

Wide Band Gap Efforts in France

The SiC efforts in France are centered in several universities, Laboratoire d'Electronique de Technologie et d'Instrumentation (LETI), and Thompson CSF. Leti is perhaps the largest French research institute with over 950 people. LETI consists of five departments and several programs. LETI is particularly known for it's contribution to wafer bonding technology. At LETI the Smart Cut ® process was described. It was pointed out that the quality of Si bonded using the Smart Cut ® process is similar to that of the starting material. This technology is applicable not only to Si but also to GaAs-based materials and SiC. The current status of SiC growth research in France is that crystal growth is in the research stage and development has just started for wafers. SiC epitaxy activity is primarily in LETI and in approximately 10 universities.

The funding sources for the effort include: CNRS, industry, and defense programs. SiC projects are divided into national programs and European programs. The two national programs in SiC include "Saut Technologique", which is a three-year program (funded by the government and coordinated by industry, with industrial partners contributing some funding as well). The European SiC program has a goal to achieve 3-inch wafers with no micropipes in three and to achieve a low defect density on two-inch wafers (less than 10 micropipes per cm^2). Under the auspices of this project, the French teamed with a Swedish-Finnish company, Okmetic. More detailed goals include cheaper and bigger crystals, a lower defect density, and the development of SiC fabrication process compatible with a silicon line. The bulk SiC material grown at LETI was described. The boule diameter was 50 mm. However, the material quality was inferior at the edges. The effort at LETI also includes the simulation of crystal growth. Results of ion implantation investigations were also discussed. The best results achieved at LETI include 95 mohm cm, $p = 10^{19}$ cm^{-3}, 14% activation for 10^{21} cm^{-3} of Al acceptors.

Wide Bandgap Efforts in Germany

The SiC research efforts in Germany is dominated by the work at Erlangen University and Siemens Corporation. Both institutions have a long history of contribution to SiC technology. In Siemens the main effort is at Siemens Erlangen, although some work is also being done in the coporate research laboratory. Two spinoff institutions were discussed. The first, Infineon Technologies, will be responsible for semiconductor components. Not much information was available on the second institution, Frielectronics, but there was speculation that this organization could do bulk crystal growth. In Seimens Erlangan the focus of the work is on power switching electronics. Over the last few years investigators in Erlangan have made significant contributions to the understanding of epitaxial growth technology (see the technology discussion above). In the last few years they have advanced their understanding of the growth and fabrication processes. The investigators in Seimens have reported detailed studies of the reliability and failure mechanisms of their high voltage diodes. Their understanding of these mechanisms has put them in the position to go into high volume production of SiC diodes. This would be the first high volume production of a SiC product (discounting the early effort on SiC LED's). In addition to the work on optimization of their 6H and 4H processes, they have demonstrated the advantage of using 15R polytype for MOSFET, instead of 4H polytype. The reason for this is that there are apparently few localized trap states near the conduction band edge in 15 R-SiC and, consequently, a much higher inversion electron mobility can be achieved than in 4 H-SiC (33 vs. 0.4 cm^2/V-s). Besides, while 6 H-SiC also has similar inversion electron mobility values, the anistropy in bulk mobilities is much less in 15 R-SiC than in 6H-SiC. The Siemens researchers are working with Erlangan University to characterize the 15R polytype.

The University of Erlangan has two separate departments with active SiC programs. The first is the Department of Material Science and Engineering. This department forms part of the Technische Fakultat (Faculty of Engineering Sciences). Conversely the second group visited was a part of the traditional Physics Department of the University. In the Department of Materials Science most of the work in wide bandgap technology is done in the Electronic Engineering Materials group. The TTEC group received a detailed presentation on the research for the bulk growth of SiC. Most of this effort is supported by a research grant from Bavaria. This research grant ~ $1 million/year has also supported SiCrystal (a startup wafer company) in their effort to commercialize bulk crystal growth in Germany. SiCrystal was present and gave a brief overview of the progress and direction of the company. In the Materials Science Deptment there are efforts to understand the basic thermodynamics of bulk crystal growth and defect formation. Of special interest, micropipes and their formation and research results on formation mechanisms were presented. These topics are investigated experimentally in a sublimation reactor, which is currently growing 1.5" SiC boules. Theoretical modeling of heat transfer is closely linked to this effort. Another technique for the production of bulk SiC is Liquid Phase Growth. The group in Erlangen and another group in Russia are unique in their efforts to investigate the possibility of large area growth of SiC by this technique. The Erlangen group is producing SiC at 2100°C and 150 torr of pressure. Under these conditions the growth rate is .6 mm/hr. The potential advantages of this technique include improved mass transfer and easier scaling.

SiCrystal was formed in August 1996. They are currently producing SiC principally for use in LED technology. This material is 2" in diameter. The company estimates that 90% of their market is based on nitride technology. They expect this number to decrease to 50% when manufacture of SiC based devices commences. When the demand for SiC material increases they will start production of 4" SiC.

The other SiC research community is in the Department of Physics. In the Department of Physics there is significant activity on crystal growth and characterization. The specific topics were:

- Bulk Crystal Growth-zero micropipes (6 H), 15 R polytype (in collaboration with Kyoto University)
- Ion Implantation –intrinsic defects, effects of non stociemetry, diffusion (Boron)
- Reconstruction of SiC surface
- MOS interface state density studies-admittance and constant capacitance DLTS

Most of the work is funded by the German Science Foundation. There is however no national program on SiC. The group does participate in a European program, which funds some of the ion implantation work.

Wide Bandgap Research in Sweden

In Sweden the SiC research is conducted in four main locations: Linkoping University, IMC, ABB and the Royal Institute. In Linkoping the TTEC panel visited the Department of Physics and Measurement Technology. The SiC activities in Sweden are funded from several sources:

SiCep

This is a national program on SiC, which provides a total of 18 million SEK of funding for SiC per year. Of that total Linoping receives 8 million SEK.

Jesica

Joint European SiC Activity. This program funds one million SEK/year. This money is split with Okmetic, a wafer growth startup company.

Okmetic

A wafer growth startup company which is partnering with Grenoble to grow semi-insulating and n+ SiC.

ABB

Linkoping is in direct partnership with ABB (a major multi-national company) for development of materials growth processing and basic understanding necessary to fabricate high voltage rectifiers.

Other

Linkoping receives about 3 million SEK from the Swedish Engineering Research Council (TFR), Science Research Council (NFR), Defense Department (FOA).

The emphasis in the Linkoping group was to provide a technology for high voltage devices. To that end they have developed high temperature epi for SiC and are using a variant of this technology for bulk crystal growth. The results for the high temperature epi are impressive. They have obtained a background doping of 2-4 $10^{14}cm^{-3}$ with a growth rate of 40 microns/hr. For the HTCVD (as applied to bulk growth) they have achieved a growth rate .5 - .8 mm/hr. The TTEC Panelists were shown the facilities at Linkoping. All the growth equipment was designed in collaboration with EPIGRISS (a local equipment supplier). After development at Linkoping this equipment is now available on the open market. The Linkoping facilities were about three years old and very impressive. All the equipment was "state of the art" and often brand new. The panel was told that the equipment was purchased with funds from a private foundation as indicated earlier in the report. In addition to the growth effort there is an extensive effort to characterize the defects and impurties in SiC. This characterization is both experimental and theorectical. As a result of this effort the Linkoping can sustainally support ABB in it's effort to commercialize SiC

IMC is an applied research company that facilitates technology transfer from the research and development stage to prototyping and manufacturing. It has received both industrial (80%) and government (20%) support to enhance Swedish competitiveness. Recently, it has merged with IOF to form a new company called ACLEO. IMC has mostly performed research in microelectronics and IOF on optoelectronics, the new company has a wide range of interests in both of these technical areas and has more European presence. IMC has locations in Kista and Linkoping. The Linkoping location focuses on interconnect and packaging of electronics and optoelectronics systems.

There are 53 employees in Kista and 27 in Linkoping. The budget for 1998 was 85 million SEK ($10.5 million) and 120 million SEK ($15 million) respectively. It spins off one new company per year on the average. There is a high turnover rate (15-20% per year) with the average age of its employees being 34. IMC utilizes the growth technology developed by EPIGRESS and Linksoping. However IMC has developed novel processing technology. An example of this is the high-temperature sensor research. One approach is to use high-temperature gas-absorbing metal-gate MOSFET. Using a Pd gate, hydrocarbons (CH_x) decompose

after adsorption to the Pd and the resulting H^+ ions diffuse to the interface, thereby shifting the barrier height (sensor arrays). The TTEC panel was given a facility tour of the clean room area that is on the ground floor and where all the micro-electronics device processing facilities of three institutions are housed, though separately. The IMC processes a large variety of compound semiconductors for several applications (such as solar cells and optoelectronics). These facilities are very impressive and world-class.

ABB is a large international industrial company that has a major presence in power generation, transmission and distribution. It was instrumental in getting the SiC program started in Sweden in 1988 and has sponsored many programs in developing the SiC infrastructure in Sweden. ABB is very focused in getting SiC devices into power electronics systems. For example, for a 1-5 MW industrial converter system, it is estimated that Si device replacement with SiC can reduce the size by 1/3. Significant improvement in HVDC system is also projected with SiC devices, with the goal of 50 MW plant in 300 m^2 area. The goal is to first implement SiC diodes with Si IGBT, with the implementation of SiC three-terminal switching devices later. Actually, they project that at higher frequencies, the Si IGBT will be thermally limited. At present, there is no GaN work at ABB. In summary, ABB focuses on the system application and leverage of SiC devices and is perhaps most advanced in the world in incorporating SiC devices into power electronics systems.

The SiC work at the Royal Institute of Technology (KTH – Kungl Tekniska Hogskolan a University) was presented, including efforts on the heterojunction SiC HBT with GaN emitter. The SiC/GaN HBT consists of 10^{18} cm^{-3} SiC p-base, over which a n+ GaN emitter was grown by MBE. The p-base thickness can be either optimized for high-voltage power (1 μm) or microwave power (optimized for 2 GHz). The device work is largely supported by SiC EP program of the Swedish government. The heterojunction GaN/SiC diode has been improving, reaching a low value of $I_R \sim 10^{-4}$ A/cm^2 at –50V, which is close to ideal. Contact work on SiC was also presented. TiC formation with $CoSi_2$/Ti bilayer after 900^{oC} anneal leads to a low contact resistivity ($^{10\text{-}6}$ Ω-cm^2) on p-type, 10^{19} cm^{-3} doped epi of 6H-SiC.

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CHAPTER 5

GaN-Based Electronic Devices

Michael S. Shur

INTRODUCTION

Glory, silicon carbide!
Schottky, switch, and polytype
Cree Research and A-T-T,
F-E-T and S-I-T!

Glory! Gallium nitride.
Nakamura and blue light.
Higher current, higher goal.
Thank you, Yoder, thank you all.

(A poem dedicated to the MRS Panel in the fall of 1998, which summarized SiC and GaN-based research in Japan.)

Material properties of GaN-based and related semiconductors make them very attractive for high temperature applications (a summary of these properties can be found at http://nina.ecse.rpi.edu/shur/GaN.htm). The material quality has been steadily improving over the past few years, and this improvement opened up new opportunities for a rapid progress in GaN related devices. Of course, the cost of this emerging technology is an issue to be addressed. The following Table illustrates an overwhelming cost advantage of silicon:

However, one can be virtually certain that the cost of GaN-based technology will drop by orders of magnitude as this technology matures.

This chapter will attempt to cover the state-of-the-art in GaN-related electronic devices with a special emphasis on some of the recent work in Japan and Europe, since this book originated as a result of the TTEC-sponsored panels that traveled from the US to Japan and Europe in order to assess the state-of-the-art.

Table 5.1
Technology Cost

Technology	Cost (US \$/mm^2)
CMOS wafer	10^{-4} (after Rin 1995)
GaN HEMT wafer	5
New York real estate of this technology.	10^{-4}

MATERIAL PARAMETERS AND TRANSPORT PROPERTIES OF NITRIDES RELEVANT TO DEVICE PERFORMANCE

The transport properties of GaN, AlN, and InN have been studied using analytical calculations (Shur, et al. 1996) and Monte Carlo simulations (see, for example, Littlejohn, et al. 1976; Joshi & Raha 1994; Bhapkar & Shur 1997; Foutz, et al. 1998; O'Leary, et al. 1998; O'Leary, et al. in pub; Kolnik, et al. 1997; Foutz, et al. 1997). These properties depend on materials quality, and the values given in Table 1 represent typical or theoretically predicted values.

Table 5.2

Parameters of GaN, AlN, and InN. Wurtzite crystal structure, crystal symmetry C_{6v}^4 ($P6_3mc$).

	Units	GaN	AlN	InN
Symmetry	-	Wurtzite/ zinc blende	Wurtzite	Wurtzite
Density	g/cm	6.15	3.23	6.81
Static Dielectric Constant		8.9	8.5	15.3
High-Frequency Dielectric Constant		5.35	4.77	8.4
Energy Gap (Γ Valley)	eV	3.39	6.2	1.89
Effective Mass (Γ Valley)	m_e	0.20	0.48	0.11
Polar Optical Phonon Energy	meV	91.2	99.2	89.0
Lattice Constant, a (c)	Å	3.189 (5.185)	3.11 (4.98)	3.54 (5.70)
Electron mobility	cm^2/Vs	1000	135	3200
Hole mobility	cm^2/Vs	30	14	
Saturation velocity	cm/s	2.5×10^7	1.4×10^7	2.5×10^7
Peak velocity	cm/s	3.1×10^7	1.7×10^7	4.3×10^7
Peak velocity field	kV/cm	150	450	67
Breakdown field	V/cm	$>5 \times 10^6$		
Light hole mass	m_e	0.259	0.471	
Thermal Conductivity	W/cm-K	1.5	2	
Melting Temperature	°C	2530	3000	1100

More detailed information about parameters of GaN, AlN, InN and BN is given in Levinshtein (in pub.) and http://nina.ecse.rpi.edu/shur/GaN.html. Many of these parameters are still to be determined more accurately. Nevertheless, Table 5.2 illustrates some important differences between GaN-based semiconductors and their

more conventional counterparts, such as Si, Ge, III-V or II-VI compounds. This difference is, first of all and most of all, the crystal symmetry. GaN-based semiconductors more often have hexagonal (wurtzite) crystal structure and grow along the hexagonal (polar axis). These have very pronounced piezoelectric and pyroelectric properties that play an important role in the physics of GaN-based devices (see Fig. 5.1).

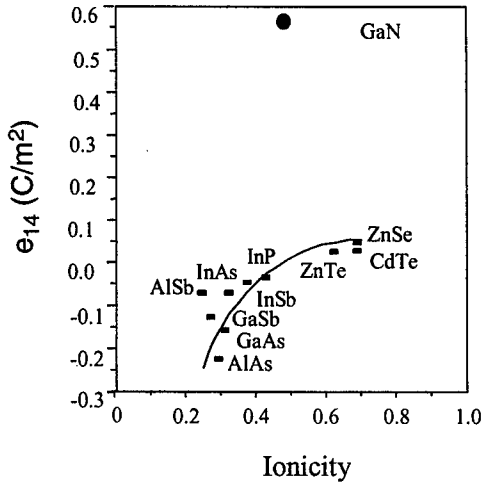

Fig. 5.1. Piezoelectric constant versus bond ionicity.

Another difference is a much larger polar optical phonon energy (91.2 meV for GaN compared to only 35 meV for GaAs, for example). This leads to a big difference in polar optical scattering that in GaN and related compounds can be approximated by a two-step elastic process – first absorption and immediate emission of a high energy polar optical phonon (Shur, et al. 1996). Fig. 5.2 shows the calculated Hall mobility in GaN versus temperature. As can be seen from the figure, the mobility is quite high (higher than for Si) and remains fairly high even at elevated temperatures.

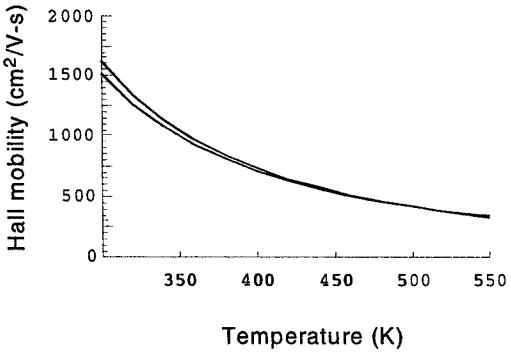

Fig. 5.2. Hall mobility in GaN versus temperature. Top and bottom curves are for $n_s = 10^{13}$ cm^{-2} and $5x10^{12}$ cm^{-2}, respectively.

The electron velocity in GaN is also very high and remains very high even at elevated temperatures. Fig. 5.3 compares the electron velocity for GaN computed using the Monte Carlo technique for different temperatures with that for GaAs (Shur 1998).

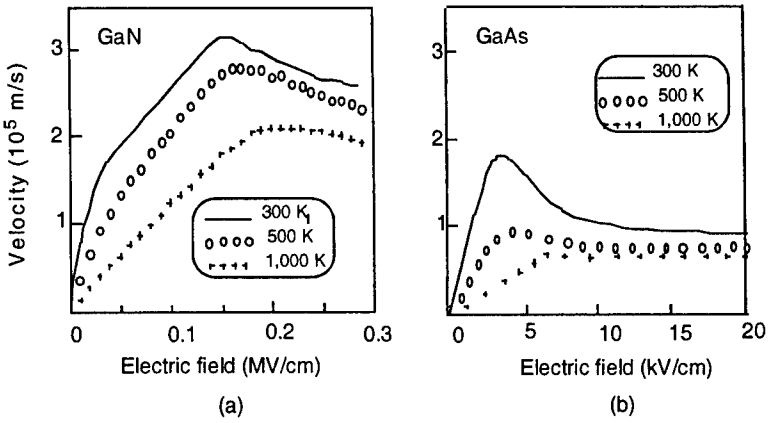

Figure 5.3. Velocity-field characteristics of GaN (a) and GaAs (b).

Fig. 5.3b was computed using the fit to the Monte Carlo calculations reported in Xu & Shur (1987) for the following values of the low field mobility: 7,000 cm^2/V-s at 300 K, 3,000 cm^2/V-s at 500 K, and 1,100 cm^2/V-s at 1,000 K.

Figure 5.4 shows the velocity versus electric field dependences for GaN at different temperatures and doping levels computed by the Monte Carlo technique (Foutz, et al. 1997). As can be seen from the figure, even at very high doping densities and/or at elevated temperatures, the predicted electron saturation velocity in GaN exceeds that in GaAs or in Si (which about 10^5 m/s) by a factor of two or so.

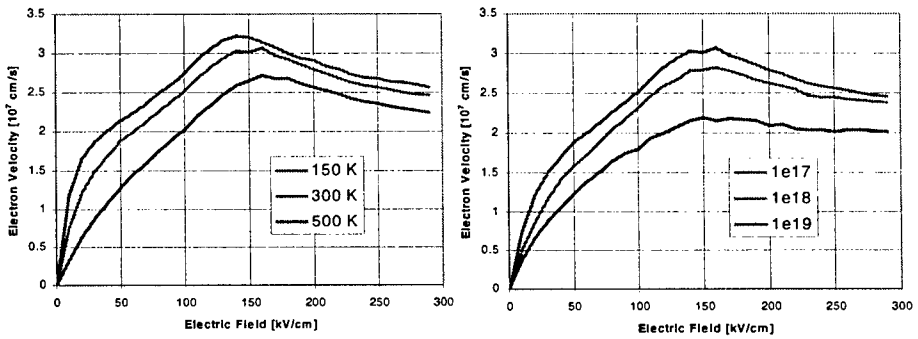

Figure 4. Velocity-field characteristics of GaN at different temperatures and doping levels. [11]

Recent Monte Carlo calculations show that overshoot effects in very high electric fields may play an important role in GaN and, as a result, the transit time in very small GaN devices may actually be shorter than for GaAs. Foutz et al. (1997) compared the computed velocity of electrons injected with low velocities into a constant electric field region into GaN and GaAs (see Fig. 5.5). This result is important for both short channel GaN devices.

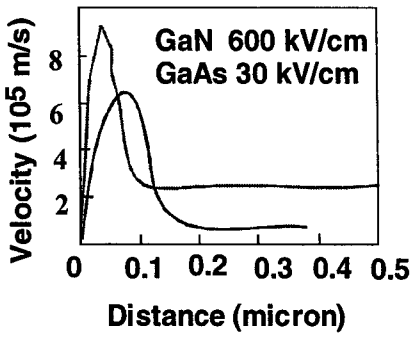

Fig. 5.5. Transient velocity in GaN and GaAs (after Foutz et al. [10])

InN is expected to have even better transport properties than GaN, including a much higher mobility (3,200 cm^2/V-s at room temperature), a much higher peak velocity, and more pronounced overshoot and ballistic effects, see Fig. 5.6 and 5.7 (O'Leary, et al. 1998; Foutz, et al. 1998; Foutz, et al. 1998b).

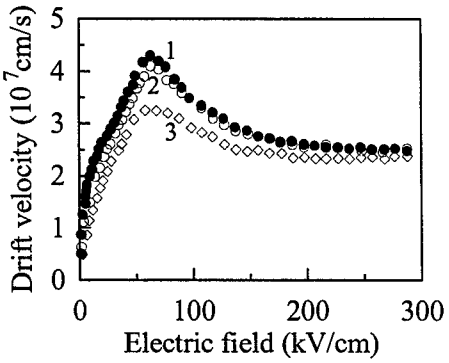

Fig. 5.6. Calculated steady state drift velocity of InN as a function of electric field at different doping concentrations N_d. T = 300 K. N_d (cm^{-3}): 1 - 10^{17}; 2 - 10^{18}; 3 - 10^{18}. After O'Leary et al. (1998)

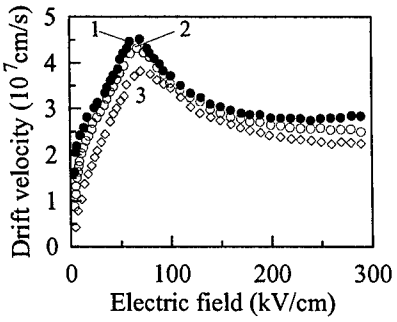

Fig. 5.7. Calculated steady state drift velocity of InN as a function of electric field at different temperatures. Doping concentration N_d= 10^{17} cm^{-3}. T (K): 1 -150; 2 - 300; 3 - 500. O'Leary et al. (1998)

However, at the present time, no device quality InN is available and the growth of InGaN with a high molar fraction of In presents a problem.

Even in InGaN alloys, the electron velocity is quite high, in spite of strong alloy scattering (see Fig. 5.8).

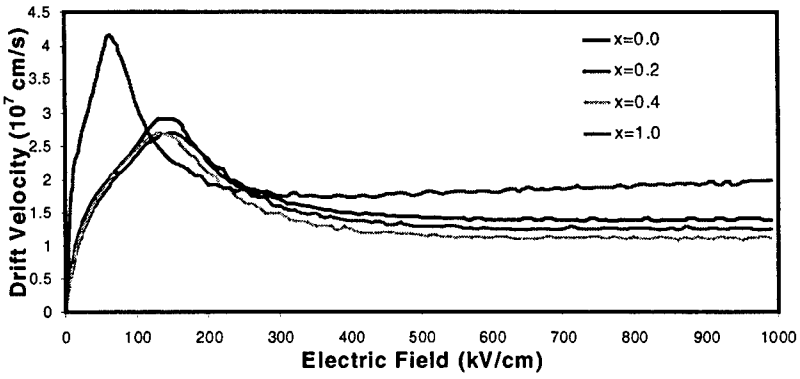

Fig. 5.8. Velocity versus electric field for $In_xGa_{1-x}N$ computed by Monte Carlo technique. (Foutz, et al. 1998)

Large energy gaps for GaN-based compounds result in large energy gap (and conduction band) discontinuities at heterointerface between AlGaN and GaN. Fig. 5.9 shows the dependence of the energies of the first two subbands (E_0 and E_1) and of the Fermi level for the two-dimensional electron gas in GaN at the AlGaN heterointerface on the density of the two-dimensional electron gas (Shur & Gaska 1998). Also shown is the molar fraction of Al needed in order to have the conduction band discontinuity that is equal to the energy shown on the left axis.

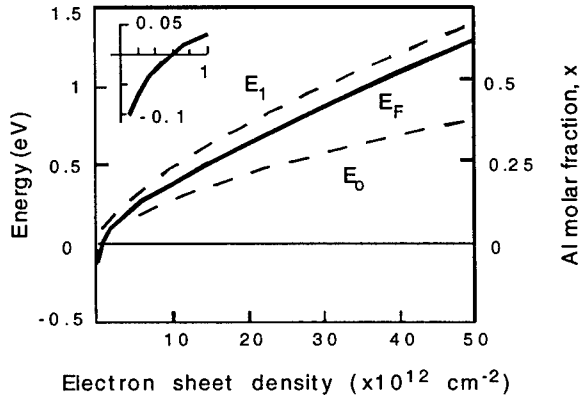

Fig. 5.9. Dependence of the energies of the first two subbands (E_0 and E_1) and of the Fermi level for the two-dimensional electron gas in GaN at the AlGaN heterointerface on the density of the two-dimensional electron gas (Shur & Gaska 1998). Also shown is the molar fraction of Al needed in order to have the conduction band discontinuity that is equal to the energy shown on the left axis.

As can be seen from the figure, the sheet densities of the 2D electron gas at the heterointerface can reach values of 2 to $5x10^{13}$ cm^{-2}. This is more than an order of magnitude larger than for GaAs-based heterostructures.

Recent studies revealed another important materials property of GaN-based compounds: an ability to independently control the band offset and strain at heterointerfaces using an approach that we called Strain Energy Band Engineering (SEBE). In this approach, one uses quaternary AlInGaN compounds. An Al atom is slightly smaller than a Ga atom. However an In atom is considerably larger. Hence, the addition of Al and In causes compensating strains at AlInGaN/GaN heterointerface, and it takes roughly one In atom to compensate the strain created by 6 Al atoms (see Fig. 5.10).

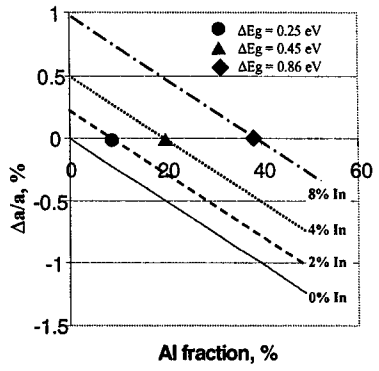

Fig. 5.10. Relative lattice mismatch as a function of Al molar fraction for different molar fractions of In. Bullets show the band gap offsets for lattice-matched Al-In compositions (Asif Khan, et al.).

As a consequence of the strain compensation, it should be possible to obtain higher sheet densities of the 2D electron gas using the SEBE approach (see Fig. 5.11).

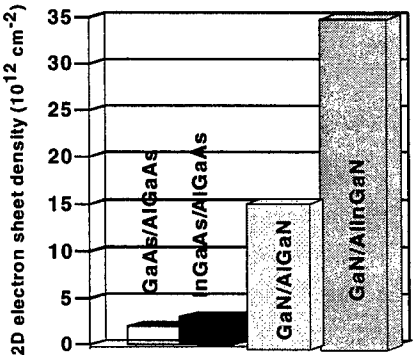

Fig. 5.11. Typical 2D sheet electron densities for different materials systems.

A high electron sheet density translates into high current carrying capabilities. This property combined with high breakdown voltages typical for wide band gap semiconductors (see Fig. 5.12), high electron velocities, and high thermal conductivity (see Fig. 5.13) makes GaN-based semiconductors very promising for high-power, high-frequency applications.

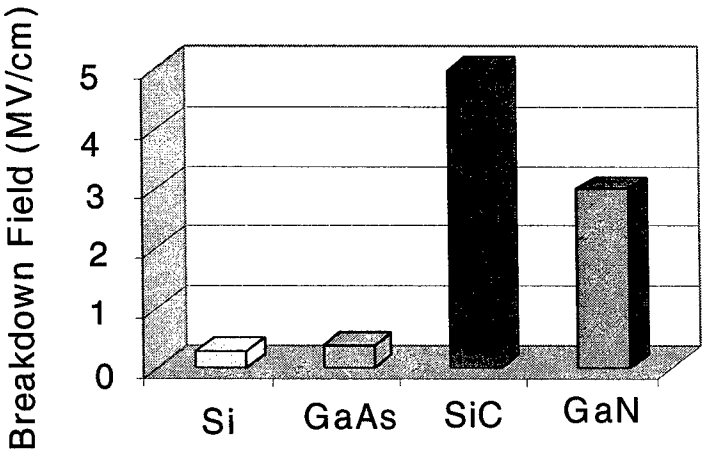

Fig. 12. Breakdown voltages for different semiconductors materials. The breakdown field for GaN might be even higher (depending on materials quality).

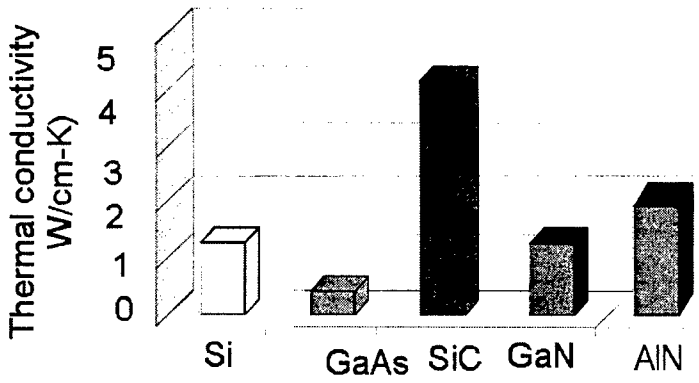

Fig. 5.13. Thermal conductivity for different semiconductors materials.

GaN and, especially AlN, have very strongly pronounced piezoelectric properties. Moreover, the crystal growth direction for these heterostructures (in the c-axis direction of the wurtzite crystal structure) is such that these properties directly affect the electric field in the direction perpendicular to the heterointerface.

Bykhovski et al. (1993-97), Asbeck et al. (1997), Gaska et al. (1997-98), Shur et al. (1999) and Ambacher et al. (1999) reported on the results of the studies of strain, piezoelectric effects, and piezoresistive effects in GaN/AlGaN heterostructures.

The studies of the piezoresistance effect in GaN/AlGaN structure point out to the possibility of the "domain" structure of the top surface, which might include domains of opposite atoms (Ga or N).

Fig. 5.14 shows a schematic charge distribution in an AlGaN/GaN heterostructure.

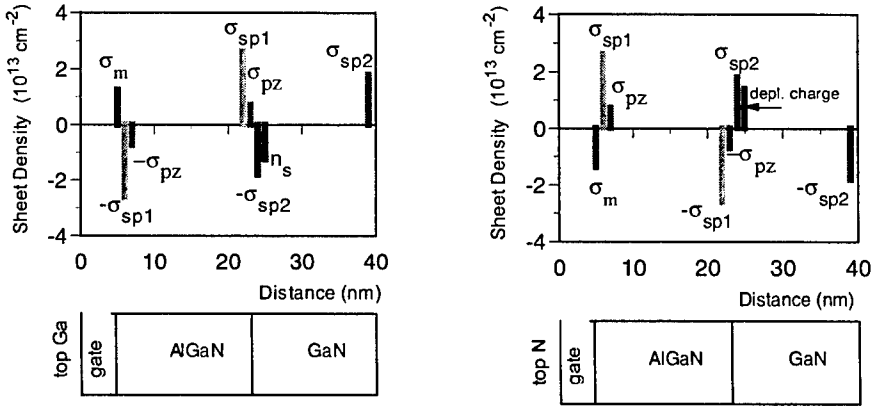

Fig. 5.14. Computed charge distribution in AlGaN/GaN heterostructure with top gallium and nitrogen surfaces.

As can be seen from Fig. 5.14, the density of the 2D electrons is enhanced in the heterostructures with the top gallium surface and greatly diminished in the heterostructures with the top nitrogen surface. As a result, these structures can be used to obtain enhanced sheet concentrations of electrons and holes, respectively. Fig. 5.15 and 5.16 show the results o the calculations predicting such enhancements.

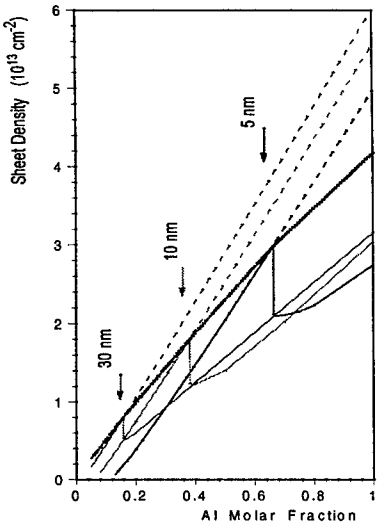

Fig. 5.15. Electron sheet density versus Al molar fraction. Numbers show the thickness of AlGaN barrier. Dashed lines neglect relaxation due to development of dislocation arrays (Shur, et al. in pub.).

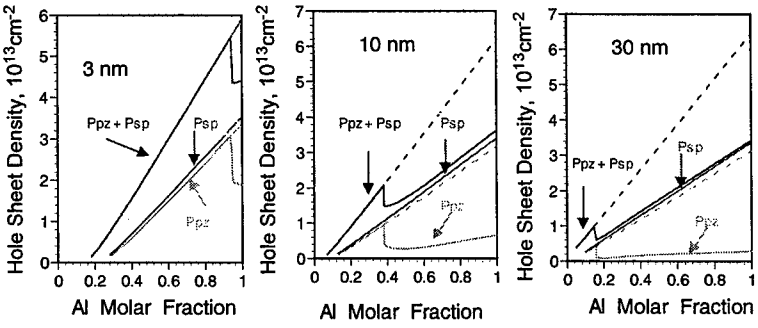

Fig. 5.16. Hole sheet density versus Al molar fraction. Numbers show the thickness of AlGaN barrier. Dashed lines neglect relaxation due to development of dislocation arrays. (Shur, et al. 1999)

MATERIALS GROWTH

GaN and AlGaN/GaN heterostructures have been grown epitaxially on different substrates - sapphire, spinel, 6H-SiC, 2H-SiC, Si, and, more recently on bulk AlN and GaN. A typical technique of GaN growth is Metal-Organic Vapor Phase Epitaxy. Most GaN-based devices use the epitaxial layers deposited using low pressure MOCVD over basal plane sapphire substrates. A typical MOCVD growth (see, for example, Khan, et al. 1991; Khan, et al. 1992; Khan, et al. 1995) uses triethylgalium, triethylaluminum and ammonia as the precursors for 'Ga', 'Al' and 'N'. Typical growth pressure and temperature reported by the APA Optics group are 76 torr and 1000 °C. Typical flows for the two metalorganics are in the range of 1 to 10 and 1.5 to 0.6 mmoles/min, respectively. As deposited, the GaN layers are highly resistive with a carrier density well below 10^{15} cm^{-3}. The insulating GaN layers can be doped n-type using disilane (Si) as the dopant.

Studies of transport properties and of the 1/f noise have shown that the quality of the epitaxial GaN depends on the quality of the substrates. Therefore, there is a considerable interest in developing bulk GaN crystals for homoepitaxy. A pioneering effort in high-pressure bulk growth of GaN is underway at Interpress in Warsaw, Poland under the direction of Professor Sylvester Porowski. The typical crystal sizes now reach

over a square centimeter. The quality of epitaxial layers grown on these substrates is excellent, with no interface detected and with the dislocation density below the detection limit.

Recently, a lot of attention has been paid to Lateral Epitaxial Overgrowth (LEO), which allows production of GaN films with the density of threading dislocations, which is up to 4 orders of magnitude smaller than for GaN films grown on sapphire (Sakai, et al. 1997; Marchand, et al. 1998; Marchand, et al. 1998b) and 6H-SiC (Zheleva, et al. 1997) substrates. UCSB group reported on studies of threading dislocations in GaN films and investigated the LEO-grown GaN films (Nam, et al. 1997; Sakai, et al. 1998; Sakai, et al. 1998b). The reduction of the dislocation density results in a dramatic drop in the leakage current in GaN-based p-n junctions (Kozodoy, et al. 1998) and GaN/AlGaN heterojunction field-effect transistors (Vetury, et al. 1998) grown by LEO.

Other techniques of the epitaxial growth of GaN include Molecular Beam Epitaxy (MBE), (see, for example, Birkman & Steckl 1997; Cheng, et al. 1997) and Hydride Vapor Phase Epitaxy (HVPE) (Molnar 1997). GaN layers grown by MBE are similar in quality to the layers grown by MOCVD. HVPE can yield thick GaN layers, which is important for potential applications of GaN-based materials in power devices. Recently, this technique was used for the epitaxial growth of AlN/AlGaN/GaN heterostructures on SiC substrates (Yu, et al. 1997).

One interesting emerging direction in the epitaxial growth of GaN, AlN, and InN materials is the fabrication of quantum dots (Tanaka, et al. 1997).

N-type GaN can be obtained with electron density higher than 10^{19} cm^{-3}. However, p-doping remains a serious problem, and the highest reported hole concentration in p-GaN was around low 10^{18} cm^{-3} (using Mg as an acceptor) (Nakamura & Fasol). This is because the ionization energy of this acceptor is quite high (160 meV) so that less than 1% of Mg acceptor is activated at room temperature.

OHMIC CONTACTS

Low-resistance, thermally stable ohmic contacts to GaN are crucial for obtaining good device performance and for fabricating devices operating in a wide temperature range. At first, Al and Au ohmic contacts to GaN were used. These contacts yielded specific contact resistances of 10^{-4} and 10^{-3} Ωcm^2, respectively (Foresi & Moustakos 1993). The use Ti in ohmic contacts to GaN resulted in much smaller contact resistance. Lin et al. described an Al/Ti ohmic contact to n-GaN with a specific contact resistance of $8x10^{-6}$ Ωcm^2 (Lin, et al. 1994). Later, Fan et al. (1996) reported on the Al/Ni/Al/Ti contact to n-GaN, and obtained the specific ohmic resistance as low as $9x10^{-8}$ Ωcm^2 using this approach. The mechanism of obtaining such low contact resistance was shown to be the formation of TiN, which leads to a large concentration of N vacancies (that behave as donors in GaN) near the surface (Ruvimov, et al. 1996). (The dependence of the specific contact resistance on doping was studied by Khan et al (1996).

Wolter et al. (1999) studied ZrN/Zr ohmic contact to GaN that showed promise of a better thermal stability with a reasonable specific contact resistance of $2x10^{-5}$ Ωcm^2 for GaN with the electron concentration of $7x10^{17}$ cm^{-3} and sheet resistance of 44 Ω/square. These contacts exhibited excellent thermal stability in evacuated quartz tubes at 600 °C for 1000 hours.

Holloway et al. (1997) reviewed the results obtained for ohmic contacts to GaN. A low contact metallization for ohmic contacts was reported in Qiao, et al. (1999)

Low-resistivity ohmic contacts to p-GaN layers are crucial building blocks for GaN based bipolar electronic and optoelectronic devices, such HBTs, LEDs, and lasers. Lunev et al. (1999) compare a new Pd/Au and the commonly used Ni/Au metallization schemes for such contacts and demonstrated contact resistances as low as 10^{-4} Ωcm^2 at room temperature and $1.5x10^{-6}$ Ωcm^2 at 250 °C for Pd/Au contacts. The p-GaN layers for this study were grown on sapphire substrates using a standard low-pressure MOCVD process with Mg as the p-dopant. Prior to the 0.5-μm thick p-GaN layer, a 1-μm thick layer of insulating GaN was also grown. Using standard Van-der Pauw geometry, the carrier concentration in the p-GaN was measured to be 3×10^{17} cm^{-3} at room temperature and 10^{18} cm^{-3} at 250 °C. With annealing the Pd/Au contact resistance decreases to a value

of 1 x 10^{-4} Ωcm^{-2}. The contacts remain stable (and linear) up to 250° C and the contact resistivity for the Pd/Au metallization decreases to a value of $1.5x10^{-6}$ Ωcm^2 (at 250° C).

In order establish the viability of the Pd/Au contact for p-n-junction devices, Lunev et al. fabricated 200 x 200 mesa GaN-InGaN MQW LEDs over sapphire substrates. The LED structure consisted of four GaN (3 nm)/$In_{0.14}Ga_{0.86}N$ (3 nm) quantum wells deposited over 1 micron thick Si-doped n^+ GaN layer ($1x10^{18}$ cm^{-3}) and capped with a p-GaN layer with a carrier density of 3 x 10^{17} cm^{-3}. The peak emission was at 430 μm and forward current as high as 100 mA at 7V bias have been achieved with a differential resistance as small as 25 Ω.

GAN-BASED TRANSISTORS

GaN and AlGaN/GaN FETs.

All basic processing and technological steps are available for fabrication of GaN and AlGaN/GaN field effects transistors of different types. Most of these devices use GaN or AlGaN/GaN layers grown by MOCVD but some devices have been fabricated using ion-implantation of active layer and contact regions. Different GaN-based FETs, including Metal Semiconductor Field Effect Transistors (MESFETs), GaN Metal Insulator Field Effect Transistors (MISFETs), Doped Channel AlGaN/GaN HFETs, and Inverted Channel AlGaN/GaN HFETs have all been developed. Binari et al. (1994; 1994b) reported on the microwave performance of the AlGaN/GaN Inverted HFETs, GaN MESFETs, and Si_3N_4/GaN MISFETs with the gate length of 0.8 μm at room temperature. Binari presented the results of the dc and microwave measurements showing that these devices can operate at least up to 360 ^oC (see also Shur & Khan 1996).

Typical FET epilayer structures are deposited over basal plane sapphire substrate using a low pressure MOCVD system. Devices on doped 6H-SiC and semi-insulating 4H-SiC (Sriram, et al. 1997) substrates have also been developed. An important technology for fabricating GaN-based FETs is ion-implantation. HFET structures with varying gate lengths and widths and source-to-drain spacing are usually fabricated on isolated mesas formed using reactive ion etching in a CCl_4 plasma and using photoresist as an etch mask. Often, Ti/Al is used as the source and drain metal and Ti is used as the Schottky barrier metal for the gate.

Fig. 5.17 shows the basic device structure of an AlGaN/GaN HFET along with proposed improvements in the device design (Shur & Khan 1997). Eastman et al. already demonstrated an improvement from using a recessed gate for AlGaN/GaN HFETs (Burm, et al. 1996). Binari (1995) and Ren et al. (1997) fabricated recessed gate GaN MESFETs. Wu, et al. (1998) demonstrated improvements resulting from increasing the Al molar fraction in the barrier layer.

In most fabricated DC-HFETs, the AlGaN barrier layer thickness was on the order of 200 to 300 Å. Simulations based on the charge control model show that the device characteristics can be substantially improved if the barrier layer thickness is scaled down to 100 Å. Transconductances close to 1000 mS/mm and drain currents up to 25 A/mm might be possible.

At room temperature, GaN-based Doped Channel HFETs (DC-HFETs) demonstrated the highest cutoff frequency and the highest maximum frequency of operation among all wide band gap devices. The best reported values of the cutoff frequency-gate length product for one micron AlGaN/GaN DC-HFETs (18.9 GHz·micron) are close to those for GaAs MESFETs (Khan, et al. 1996; Shur, et al. 1997).

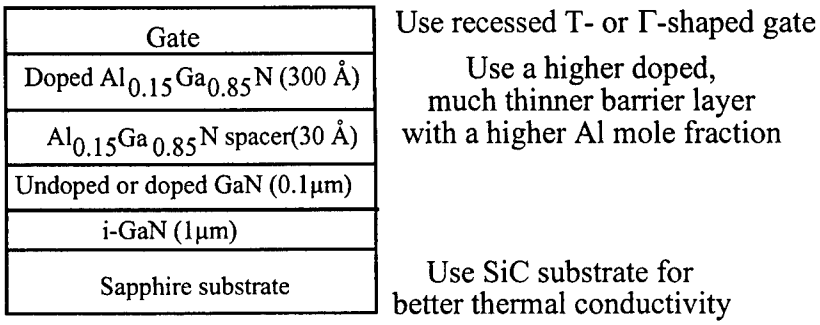

Fig. 5.17. Basic device structure of an AlGaN/GaN HFET along with proposed improvements in the device design.

Fig. 5.18 shows the measured values of the cutoff frequency, f_T, and the maximum frequency of oscillations, f_{max}, as functions of temperature at a drain bias V_{ds} = 20 V.

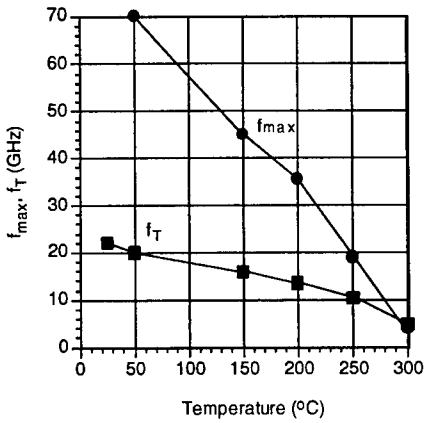

Fig 5.18. f_T and f_{max} versus temperature. V_{ds} = 20 V, V_{gs} = – 0.8 V (Khan, et al. 1995).

The velocity saturation HFET model links the cutoff frequency, f_T, to the low field mobility, saturation velocity, gate length, and intrinsic gate voltage swing. The analysis of this model showed that f_T could be significantly improved by increasing the sheet carrier density in the channel. This gave an incentive to using doped channel devices in order to increase n_s. This approach is similar to that for doped channel AlGaAs/GaAs HFETs (Ruden, et al. 1990). However, in AlGaN/GaN structures, the doped channel is even more advantageous since the additional impurity scattering has less of an effect in GaN than in GaAs. Two principal scattering mechanisms determining the electron mobility in GaN are the polar optical scattering and ionized impurity scattering. Because of a higher electron effective mass, the impurity scattering plays a smaller role than in GaAs at the same doping level. The AlGaN/GaN DC-HFETs exhibited transconductances up to 270 mS/mm and maximum saturation currents in access of 1.5 A/mm.

The channel doping also dramatically reduces the contact resistance. In a doped channel structure, the sheet electron concentration, n_s, can be very high. Gaska et al. reported on the values of n_s higher than approximately $4x10^{13}$ cm^{-2} with the sheet concentration-mobility products up to approximately $4x10^{16}$ 1/Vs. (This value of n_s included both 2D-electrons and 3D-electrons in the doped channel.) At high gate biases, the current-voltage characteristics of these devices exhibit the negative differential resistance, which is usually related to device self-heating (see, for example Shur 1987). This means that with a better heat sinking, the device characteristics should improve further. The microwave measurements for 1 μm gate AlGaN/GaN DC-HFETs yielded the cutoff frequency times gate length product of 18.9 GHz·micron, which is the highest values achieved for a wide-band gap FET.

The importance of a large electron sheet concentration in the channel for the improved FET performance was confirmed by a transconductance increase in an $Al_{0.15}Ga_{0.85}N/GaN$ HFET under UV illumination. The illumination acted as "optical" channel underdoping. A relatively modest positive trapped charge in the active channel ($4x10^{11}$ cm^{-3}) was sufficient for a considerable shift in the threshold voltage and, consequently, for the enhancement of the n_s value. The maximum transconductance, g_m, reached 64 mS/mm, nearly three time higher than for similar devices with a comparable threshold voltage and many times larger than for the same device in the dark. This enhancement was explained by a large reduction in the source and drain series resistances and by the enhancement of the n_S value. Calculations (based on the HEMT model developed in Lee, et al. 1993) confirm that the g_m enhancement is caused by the reduction in R_s, and by a larger n_s.

For deep sub-micron gate GaN/AlGaN DC-HFETs, record values of the cutoff frequency, f_T, and the maximum frequency of oscillations, f_{max}, are 46.9 GHz and 103 GHz, respectively (Khan, et al. 1996).

The advantages of DC-HFETs compared to other GaN-based devices should be even more pronounced at elevated temperatures. The reason for the expected good performance of AlGaN-GaN DC-HFETs at elevated temperatures is the decrease in ionized impurity scattering with an increase in temperature. The measured I-V characteristics of AlGaN-GaN DC-HFETs and the investigations of microwave characteristics of these devices at elevated temperatures support this assumption.

AlGaN/GaN HFETs reached record power levels at microwave frequencies as high as 9.2 W/mm. These results show that, in spite of a smaller thermal conductivity than for SiC, excellent transport properties of GaN at elevated temperatures make these devices a viable alternative for high-temperature and high-power microwave and digital applications. A further improvement in high temperature performance can be achieved if self-heating effects are reduced. The replacement of sapphire substrates with SiC substrates drastically decreases the thermal impedance of the Doped Channel AlGaN/GaN HFETs and self-heating effects.

Tables 5.3 and 5.4 (from) summarize parameters of GaN-based HFETs.

Table 5.3

State-of-the-art parameters of GaN-based HFETs (Khan, et al. 1999).

PARAMETER	UNIT	L_{sd} (μm)	L_g (μm)		REFERENCE
Saturated Current I_{sat} (25C)	mA/mm	2	0.25	1.7	Khan et al., Elec. Lett. 1997
		5	2.0	1.35	Gaska et al., ICNS2 1997
		2	0.25	1.2	Mishra et al. EDL 1996
Transconductance g_m	mS/mm	2	0.25	220	Khan et al., Elec. Lett. 1997
		2	0.25	250	Gaska et al. Elec. Lett. 1998
		2	0.25	270	Mishra et al. Elec. Lett. 1997
		2	0.25	270	Eastman et al. 1999
		1.4	1.2	400*	Mishra et.al 1999
f_t/f_{max}	GHz	2	0.25	38/81	Khan et al., Elec. Lett. 1997
		2	0.12	47/103	Burm/Khan et. al, EDL 1997
		2	0.15	67/140*	Chu et al. WOCSEMMAD 1998
		2	0.4	28/114	Shephard et al. EDL 1999

Table 5.4

Microwave performance (Khan, et al. 1999).

Gate length (μm)	f_T (GHz)	f_{max} (GHz)	I_{ds} (A/mm)	Power (W/mm)	g_m (mS/mm)	Reference
0.45	28	114	0.68	6.8 at 10 GHz	200	83
0.4				9.2 at 10 GHz		84

At the moment of writing, the maximum reported output power values are 9 W at 7.4 GHz and 9.8 W at 10 GHz reported by Cree, Inc. and Nitres, Inc., respectively (Sheppard, et al. 1998; Sheppard, et al. 1999; Wu, et al. 1999).

In principle, the effective velocity of the order v ~ of $2x10^5$ m/s and the sheet carrier concentration on the order of $n_s \sim 5x10^{13}$ cm^{-2} can be reached in GaN/AlGaN heterostructures. This corresponds to the maximum drain current of $I_{ds}/W = qn_sv_s \sim 16$ A/mm.

Monte Carlo simulations predict the value of the breakdown electric field in wurtzite GaN to be on the order of 3 MV/cm (Bykhovski, et al. 1995; Oguzman, et al. 1997). This agrees with a recent estimate of the characteristic field of the impact ionization extracted from the measurements of the Doped Channel GaN-AlGaN HFETs (Dyakonova). Assuming a 5-micron long high field region (which can be realized using an offset gate design, see Gaska, et al. 1997) we estimate the drain breakdown voltage to be 1,000 V for the total power dissipation of 16 kW/mm (probably not realistic)! Even higher values of the current may be obtained using a multi-channel HEMT design (Gaska, et al. 1998).

The highest measured currents are typically on the order of 1 A/mm to 1.5 A/mm, i.e. much lower than predicted upper bounds for the drain-to-source current. However, we expect that this gap will be bridged with improved device designs and better materials quality.

The measured breakdown fields are also lower than the theoretical values expected. Fig. 5.19 shows the breakdown voltage of GaN/AlGaN HEMTs as a function of the gate-to-drain distance

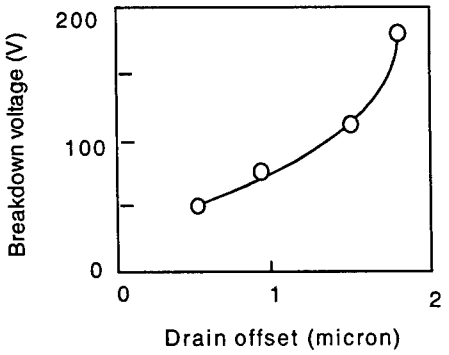

Fig. 5.19. Breakdown voltage of GaN/AlGaN HEMTs as a function of the gate-to-drain distance (after Gaska et al. 1997)

The breakdown field deduced from these data is on the order of 1.3 MV/cm. It is limited by non-uniform field distribution and will be improved when the device design is optimized.

As follows from the estimates and measurements of the maximum currents and voltages for GaN/AlGaN HEMTs, these devices might dissipate a very large power. Therefore, problems related to self-heating become very severe, especially for the devices grown on sapphire substrates, which have a low thermal conductivity. Conventional heat-sinking designs, such as a flip-chip (see, for example, Shur 1987) can be used in order to reduce self-heating. Thibeault et al. obtained excellent results for AlGaN/GaN HFETs using this approach. Another approach involves using SiC substrates. Recent studies of GaN/AlGaN on SiC

substrates showed that these substrates reduce the device thermal impedance by more than an order of magnitude (down to approximately 2 °C mm/W, i.e. about 20 times smaller than for typical GaAs power FETs.) The dissipated values of the DC power were up to 0.8 MW/cm^2.

The epitaxial GaN structures grown on SiC also have an advantage of a much smaller lattice mismatch (only 3-4%). Our comparative studies of the Hall mobility, Quantum Hall Effect, and Shubnikov-de-Haas effect on AlGaN/GaN heterostructures grown by MOCVD on sapphire and 6H-SiC substrates using an isolating AlN buffer show that the material quality is much better for the heterostructures grown on 6H-SiC (Gaska, et al. 1998).

Doped p-type and n-type 6H-SiC and semi-insulating 4H-SiC substrates have been used for AlGaN/GaN fabrication. Semi-insulating SiC substrates are expected to yield a much better microwave performance because of sharply reduced parasitics.

At the Third European Workshop on GaN (EGW-3) in Warsaw, I. Daumiller of University of Ulm, Germany, reported on the operation of doped channel GaN-based HFETs at temperatures up to 750 °C (see Fig. 5.20).

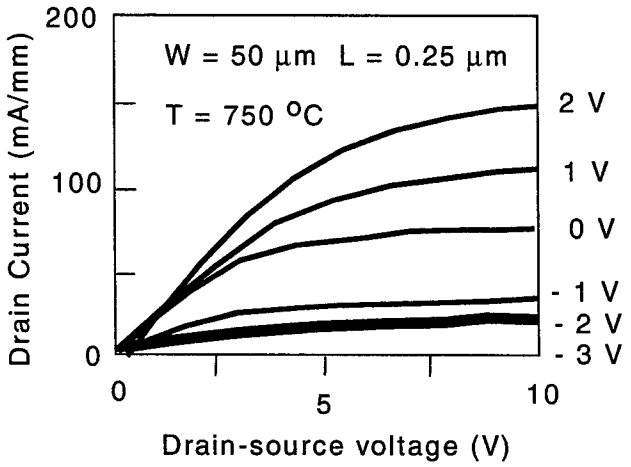

Fig. 5.20. Operation of doped channel GaN-based HFETs at 750 °C HFET (after Kamp 1998).

GaN Bipolar Transistors.

In the future, GaN bipolar devices might compete with GaN-based FETs for high-power applications. Bandic et al. measured the hole lifetime in GaN to be approximately 7 ns (Bandic, et al. 1997). They estimated that GaN/AlGaN thyristors might support up to 5 kV operating voltages with current densities of 200 A/cm^2 and operate at frequencies exceeding 2 MHz.

Pankove et al. (1996) reported on a new Heterojunction Bipolar Transistor that used a heterojunction between GaN and SiC. The transistor exhibited an extremely high gain of ten million at room temperature, decreasing to 100 at 535°C.

Recently, the University of Florida and UCSB groups reported on the first demonstration of an AlGaN/GaN HBT (MacCarthy, et al. 1998; Han, et al. 1999; Ren, et al. 1998). There is also a proposal for a unipolar Induced Base Transistor that operates in a way similar to that of a bipolar device (Bykhovski, et al. 1999).

GAN ELECTRONIC DEVICE RESEARCH IN JAPAN

At the present time, Japanese researchers are more interested in GaN-based light emitters. The pioneering work of Professor Akasaki at Meijo University in Nagoya and Dr. Nakamura and his team at Nichia in Tokushima led to the room temperature CW operation of a blue GaN laser, and this success has inspired

many groups world wide to pursue GaN light emitters (Nakamura, et al. 1997) and photodetectors (Shur & Khan 1997; Shur & Khan 1998).

However, the effort in GaN-based electronic devices (or, at least planning for such research and development) has started as well. Examples include NEC, Nippon Steel, Hokkaido University (Koyama, et al. 1998), and Tokushima University. Professor Shiro is interested in developing GaN FETs for wireless communication applications and for collision avoidance radars. Low toxicity of GaN is seen as a major advantage compared to GaAs-based FETs. Furukawa group, which pursues epitaxial growth of GaN by gas source MBE is planning to develop high voltage, GaN-based high power devices, in addition to pursuing GaN laser diodes. They are also investigating high temperature GaN MESFET with Pt gate, oxide passivation on GaN, GaN Schottky diodes, and AlN/GaN MISFETs.

ETL and Sony also have GaN research programs, even though in electronic device the emphasis at the present time is on SiC and, to a lesser degree, diamond devices.

Prof. Egawa of Nagoya is doing research on GaN on Si. His interests include geothermal applications of GaN-based electronic devices. He demonstrated GaN MESFET operation at 300 °C.

Professor Akasaki sees possible applications of GaN-based devices in radiation hard electronics and for atmospheric pollution monitoring. However, most of his research is still focused on optical GaN devices.

Nippon Steel, which produces SiC substrates grown by modified Lely method, has interest in expanding their SiC program to include epitaxial growth of SiC and, possibly, of GaN-based materials. Plans are under way to develop 2-inch SiC bulk technology and (in a more distant future) 3-inch bulk SiC technology. This will be important for GaN-based devices grown on SiC substrates. Nippon Steel projects the development of high-temperature GaN electronics after year 2,000.

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NEC at Tsukuba is planning to use GaN for microwave power at power levels above 100 W and at frequencies above 10 GHz (up to 100 GHz). Their target is to obtain 100 W at 20 GHz (for applications in base stations). They are also evaluating radar and collision avoidance applications.

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Many Japanese researchers predict that the "environmentally friendly" nature of GaN and SiC, as opposed to GaAs, is a big incentive for commercial development. Professor Sakai of Tokushima University used cellular phones as an example. These phones contain toxic GaAs chips, which may be replaced with GaN or SiC chips.

NEC at Tsukuba is planning to use GaN for microwave power at power levels above 100 W and at frequencies above 10 GHz (up to 100 GHz). NEC is interested in both the electronic and optoelectronic applications of wide bandgap semiconductors. Currently NEC is focusing on GaN, since they believe it to be the least expensive wide bandgap material to commercialize. The GaN electronic effort started in 1997. Dr. Ohno of NEC who is involved in this effort believes that the main advantages of wide bandgap semiconductors are the large breakdown voltage, the small Schottky gate leakage, and the small hole generation rate. The high breakdown field and high frequency performance of GaN make it attractive for applications in microwave power devices. The higher maximum operation temperature of GaN is also an advantage, since it allows for higher heat removal due to the increase in the temperature gradient. NEC envisions the applications of the microwave power GaN High Electron Mobility Transistors in 100 W CW RF power modules for 50-100 GHz region as well as in 100 W parts and 500 W modules.

Dr. Ohno sees the GaN electronics market primarily in high frequency Satellite and communication base station applications. For cellular phone applications the competition will be fierce with Si LDMOS coming to 5 GHz power region soon. Other potential applications of wide bandgap electronics include anti-collision automobile and boat radars, and microwave ovens.

A very interesting and promising work on bulk growth of GaN is performed at the Satellite Venture Business Laboratories (SVBL) at Tokushima University. This laboratory is 1 of 24 national labs created from the Ministry of Education's supplementary budget to stimulate the creation of new ideas and new businesses. The SVBL at Tokushima University is a 4 story world-class facility. The facility was opened in June 1997 with the research focused on "Nitride Photonic Semiconductor". The laboratory has excellent materials characterization, bulk GaN crystal growth, and thin film deposition facilities. Four foreign post-doctoral researchers, several Ph. D. candidates, and several master's and bachelor students are working in the facility.

Professor Sakai's group at Tokushima University is interested in applications of nitrides in electronics. The group is working on the bulk GaN crystal growth by sublimation technique. They have already achieved bulk GaN crystal a few mm in diameter and have deposited epitaxial layers on these crystals by MOCVD. These films have a lower defect density than GaN films grown on sapphire. Professor Sakai and his associates investigated the cathodoluminescence in their films and compared the results with those for the GaN films grown on sapphire (see Table 5.4).

Table 5.4

Properties of Sapphire

Crystal symmetry	R3c	
Lattice constants	a = 4.765 Å, c = 13.001 Å	
Density	3.98 g/cm^3	
Young's modulus	380 GPA	
Melting point	2053 °C	
Specific heat	0.1 cal/g m	
Thermal conductivity	0.11 cal/cm, C, sec	@ 0 °C
	0.06 cal/cm, C, sec	@ 100 °C
	0.03 cal/cm, C, sec	@ 400 °C
Thermal expansion coefficient	5.3×10^{-6} K^{-1} (parallel to c-axis)	
	4.5×10^{-6} K^{-1} (perpendicular to c-axis)	

They observed that, in the films grown on sapphire, defects lead to dark spot regions. In contrast, they observed almost no dark spots on the bulk like film. The number of dark spots on the GaN on sapphire appears to correlate with the defect density measured by TEM. Hence, bulk GaN crystals may have improved optical properties (Suguhara, et al. 1998).

Professor Sakai at Tokushima University is growing two-inch GaN wafers in his MOCVD system. His group has found that GaN low temperature buffers work better than AlN buffers for GaN films grown on sapphire. Professor Sakai believes that GaN MOCVD films have a higher quality and will more suitable for mass-production.

Matsushita Electronics Laboratory group, jointly with the Osaka University group, reported on a detailed study of the growth of GaN thin films on sapphire substrate by MOCVD (Ishida, et al. 1997). They studied the effects of nitridation and buffer layer thickness on the quality of the overgrown GaN films (see Fig. 5.21).

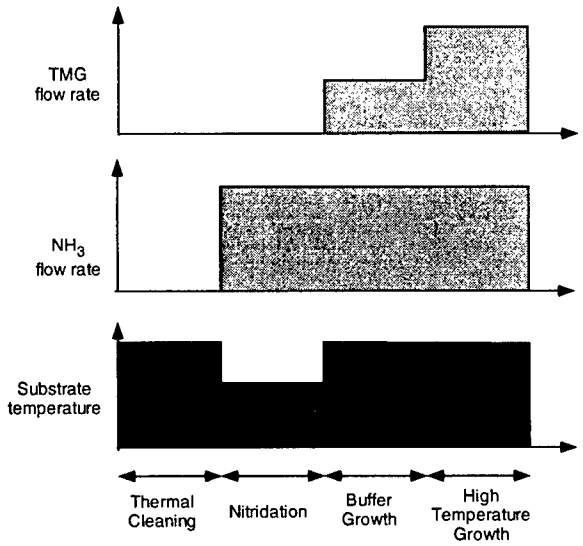

Fig. 5.21. Flow and temperature patterns for GaN MOCVD growth reported by Matsushita/Osaka University group. Substrate temperature varies from 1000 °C to 600 °C. TMG flow rate 15.3 μmol/min to 30.7 μmol/min. N flow rate 170 mmol/min. Pressure and H flow rate are constant at 50 Torr and 9 slm, respectively. Thermal cleaning takes 15 minutes; high temperature growth takes 60 min. Nitridation and buffer growth times varied from 5 to 30 minutes.

The nitridation time of 30 minutes and the buffer thickness of 60 nm yielded the best smoothness of the film surface (determined by the atomic force microscopy (ATM)). However, a thin buffer layer (10 nm) yielded the lowest dislocation density ($2x10^9$ cm^{-2}) and the best photoluminescence spectra.

The Matsushita/Osaka University group also reported on the growth of wurtzite and cubic GaN layers on the 3C-SiC/Si (001) substrates (Hashimoto, et al. 1996) and on the growth of InGaN films on GaN (0001)/Al_2O_3 (0001) substrates (Ishida, et al. 1997b). The InGaN films were grown at lower temperatures (~ 700 – 750 °C). The bowing parameter determined from the compositional dependence of the photoluminescence peak was 4.1 eV at room temperature for the relaxed films (compared to the value of 3.3 eV reported for the strained InGaN films in Takeuchi, et al. 1997).

Dr. Usui of NEC has achieved the defect reduction in GaN with the lateral epitaxial overgrowth (LEO) method. He used the acronym Facet Initiated Epitaxial Lateral Overgrowth (FIELO) in order to describe the NEC technique for defect reduction in GaN. Defect density is reduced from 10^9 cm^{-2} to less than 10^7 cm^{-2}. He has even made "bulk like" GaN substrates by lifting off thick GaN epitaxial films from the sapphire substrate by an NEC proprietary technique. These bulk like GaN films are 100 to 200 microns thick and 1cm by 1cm wide.

All in all, Japanese scientists and engineers see short-term applications of GaN technology in optical devices, mostly light emitters. However, in year 2000 and beyond, a larger market is expected to develop for high temperature, high power GaN electronics components.

GAN DEVICE RESEARCH IN EUROPE

Many universities, government and private research laboratories and electronics companies in France, Germany, Sweden, Italy, Great Britain, Spain, and other European companies are now involved in GaN-related research. Most of their efforts involve studies of fundamental properties of GaN-based compounds and materials growth. However, the device research is being ramped up.

French effort is representative of the overall European effort. CRNS in Lille is involved in device processing and electronic applications, CNRS and University in Caen are studying crystallography; CNRS group in Strasbourg is doing research on nonlinear optics applications of GaN. The university group in Clermond Ferran is involved with crystal growth and optical properties. The optical properties are also studied by the University of Lyon group, by CEA in Grenoble, and by CRNS in Valbolne. CEA in Grenoble and the University of Montpellier groups are working on MBE and MOCVD growth, respectively. CRNS in Valbolne is involved in growth and optical characterization studies. This effort is funded by several European and EEC projects such as ANISET (which is materials oriented research project), LAQUANI (which is both material and device oriented), RAINBOW (which is concentrated on multicolor LEDs and blue lasers), MIGHT (material and device oriented and targeted toward high power, high frequency electronics, with the goal of getting 3 W at 10 GHz). A typical budget for these projects is 3 to 4 million Euro per year.

In Poland, High Pressure Research Center and Unipress (which is the research group within HPRC working of GaN bulk crystal growth from a melt) developed the "defect free" semi-insulating (10^5 ohm-cm) and doped bulk GaN wafers grown from melt under very high pressure. The bulk crystals have extremely smooth cleaved facets with RMS roughness of 0.5 nm. Both Ga-face and N-face polarity bulk substrates have been demonstrated. The size of the substrates has reached 1cm in 1999 (Litwin-Staszewska, et al. 1999). MOCVD and MBE growth has also been performed on these bulk substrates. The group at University of Ulm in collaboration with Unipress demonstrated epitaxial films, which exhibited the narrowest reported photoluminescence line widths at low temperature (0.1meV) (Kornitzer, et al. 1999). The UNIPRESS group is also working high power HEMTs, Schottky diodes, and UV detectors.

In Germany, Siemens has recently spun off Infineon Technologies, which will be responsible for semiconductor components. Infineon and Osram have a Joint Venture, which is developing GaN blue LEDs and solid-state white lighting using GaN based LEDs. In Munich, Siemens Munich Corporate research laboratory has a GaN MBE facility, which is geared towards high microwave power electronic devices. The future work in the Siemens MBE lab will be on AlGaN/GaN electronic devices and GaAsN for long wavelength lasers.

There is now a considerable and growing interest in GaN research in Russia. Fig. 5.22 shows the number of GaN-related papers at the All-Russian Conference on Nitrides of Gallium, Indium, and Aluminum: structures and devices.

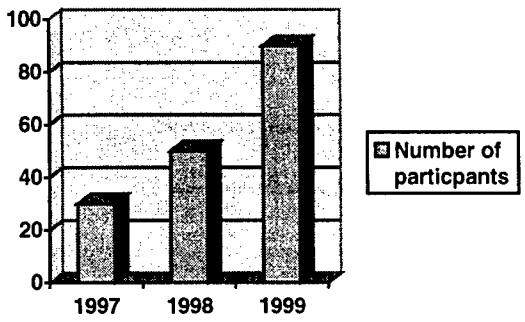

Fig. 5.22. Number of GaN-related papers at the All-Russian Conference on Nitrides of Gallium, Indium, and Aluminum: structures and devices.

The Russian universities and research organizations involved include A. F. Ioffe Institute of Physics and Technology of the Russian Academy of Sciences, Lomonosov Moscow State University, Lebedev Institute of Physics and Technology of the Russian Academy of Sciences, GIREDMET, NPVF "Svecha", Crystal Growth Research Center in St. Petersburg, ELMA-MALAKHIT in Zelenograd, Moscow Institute of Electronic Technology, Institute of Physics and Chemistry of the Russian Academy of Sciences, Moscow State Institute of Steel and Alloys, St. Petersburg State Technical University, Institute of Physical Chemistry of the Russian Academy of Sciences, Institute of Crystallography of the Russian Academy of Sciences, Institute of Nuclear Physics, Sigma Plus in Moscow, Baikov Institute of Metallurgy of the Russian Academy of Sciences, "Polyprovodnikovye Pribory" in St. Petersburg, "SAPHFIR" in Moscow, Institute of Chemistry of Silicates in St. Petersburg, Vologda State Technical University, Udmurtsky State Technical University, VNII of Optical and Physical Measurements in Moscow, OPTEL in Moscow, St. Petersburg Institute of Technology, Frumkin Institute of Electrochemistry, NITI "TEKHNOMSH" in Moscow, MAR State Technical University in Iohskar-Ola.

Russian international collaborations include TDI, Inc., Howard University in Washington, DC, Rensselaer Polytechnic Institute in Troy, NY, Naval Research Laboratory in Washington, DC, University of Ulm in Germany, University of Karlsruhe in Germany, Technical University of Berlin in Germany.

The largest effort is at A. F. Ioffe Institute. The areas of research and development include crystal growth (with emphasis on HVPE, MOCVD, MBE, and sputtering), fabrication and characterization of ion-implanted p-n junctions, the development of production equipment (at ELMA-MALKHIT), research on ternary and quaternary AlGaInAs solid state solutions, investigations of basic materials properties, growth and characterization of wurtzite and cubic BN, research on GaN and InGaN based LEDs and optically pumped lasers, white LEDs, research on doping of GaN, the development of GaN/GaP and GaN/Si heterostructures, studies of piezoelectric properties, the research on defects, studies of mechanical properties, cathodoluminescence studies, Raman and lattice dynamics studies, applications of blue, green, orange, and red LEDs for materials testing, and studies of acoustic surface waves.

The Russian company SVECHA has taken a lead in production of traffic signals using green GaN LEDs. They had the first installation of such traffic signals in Moscow in 1997. They are involved in the development of LED-based lighting for airplanes, of LED-based navigation lights, and lighting sources for other applications. NII OPTEL is using imported green InGaN LEDs for river navigation lights. One blue LED is visible for two kilometers.

The research level on devices is relatively small compared to the US. Only two teams demonstrated p-type GaN (Alferov's team by MOCVD and Dmitriev's team by HVPE). However, several excellent groups are involved in basic GaN research. Even at this level, there is a company pursuing practical applications (traffic lights) using imported GaN LEDs

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CHAPTER 6

HIGH-TEMPERATURE ELECTRONICS PACKAGING IN EUROPE

George White

INTRODUCTION

To understand the meaning of high temperature electronic packaging one would have to have a clear understanding of high temperature electronics in general. High temperature electronics may be defined as those devices and/or subsystems that operate at elevated temperatures above 200°C. Similarly high temperature electronic packaging may be defined as establishing interconnections and a suitable operating environment for these electronic devices (e.g., SiC, GaN or Si) at temperatures above 200°C. These definitions can be argued as too vague or inadequate since many researchers have varying opinions on what constitutes high temperature (i.e., electronics operating above 300 °C, above 400 °C, etc.). However, most researchers would agree that there needs to be significant consideration given to addressing both the components and packaging needs for high temperature applications to achieve similar levels of integration and functionality to what is currently being practiced at ambient and near ambient conditions for today's silicon and III-V compound IC's.

Most high temperature applications will find their niche in harsh environments, such as under the hood for exhaust gas sensors and in exposed areas of an aircraft. Applications such as these may be impractical for conventional silicon, unless one introduces highly complex and expensive packaging techniques involving liquid cooling, etc. Although these are very important issues to address, many in the silicon IC world are very reluctant to make the necessary investments to produce the high quality devices necessary to meet these challenges. As a result, the electronic packaging community, which is under tremendous pressure to find low cost solutions to package IC's, will also be slow to address the packaging needs for high temperature applications. In addition to business pressures and challenges, there are also significant technical challenges to package wide band gap materials for high temperature applications.

To package wide band gap materials for high temperature applications a number of alternative materials, including substrates and solders, and fabrication techniques have to be considered over conventional packaging practices. Today most devices are packaged using glass epoxy boards and organic encapsulants. At the temperatures of interest in this study, these components would melt or significantly degrade thermally, thus proving impractical for use. Eutectic solders as well as conventional die attach materials will also need to be addressed. Passive device selection and reliability testing are also critical issues as well.

The following chapter will address some of these issues as they were discussed during the TTEC sponsored study on "High Temperature Electronics in Europe". I should caution however, the amount of interaction was very limited for this subject matter, as many of the researchers whom the team visited were not directly involved in electronic packaging and had little knowledge regarding plans and future directions for the packaging of their devices. However, some were knowledgeable, including experts at Siemens and IMC. It is therefore our intention to present in this chapter their views as well as some of the views of the author on

the status and direction for some key technology elements of packaging for some high temperature applications involving SiC, GaN and Si.

PASSIVE DEVICE SELECTION

A critical question in the packaging of high temperature electronics is what do you do about the passive components? Two of these components involve resistors and capacitors. Since there is a component of resistivity which can be expressed as function of temperature due to lattice vibrations (or phonons) it stands to reason that one must exercise care when laying out their designs, for instance for a MCM which may utilize high temperature devices. An important characteristic for resistor components is its TCR or Temperature coefficient of resistivity. If the TCR of a resistor is properly characterized and quantified then it should not cause premature failure of a system or parameter drifts, since it can be addressed by careful circuit

Table 6.1

TCR for Common Resistor Materials (Pecht and Lall 1994; Elshabini-riad 1991; Heidler 1969)

Resistor Types	*Max Operating Temp (°C)*	*TCR (ppm/K)*
Wirewound resistor		
Precision	145	10
Power	275	260
Metal-film resistor		
Precision	125	50-10
Power	165	20-100
Composition resistor		
General Purpose	130	1500
Deposited resistor		
Thin Film		
Tantalum	>200	+/-100
Tantalum Nitride	>200	-85
Titanium	>200	+/-1000
SnO2	>200	-1500 to 0
Ni-Cr	>200	+/-100
Cermet		+/-150
Thick Film		
Ruthenium silver	>200	+/-200
Palladium silver	>200	-500 to 150

design that balances the characteristics of several resistors to create a network unaffected by temperature (Pecht 1994). However, other factors such as humidity, stress, etc. can alter the performance of a resistor depending upon the material choices. Table 6.1 shows the TCR for some common resistor materials.

On the other hand, capacitors are very difficult to design for in high temperature applications since the dielectric constant and the loss tangent will fluctuate with increasing temperature. Typically designers will use either polymer film dielectric materials, thin films, or ceramic materials. Table 6.2 illustrates some of the material choices and their properties for high temperature polymers.

Table 6.2

Dielectric Film Candidates for Elevated Temperature Wound Capacitors (McCluskey 1997)

Dielectric Material	**Commercial Source**	**Properties and Advantages**
Polysilseqioxane	David Sarnoff Labs	Good electrical properties up to 250C
Teflon Perflouroalkoxy	DuPont	Good mechanical and electrical properties up to 200C
Polyimide	DuPont	Small variations in dielectric loss up to 200C
PBO	Foster-Miller, Dow	Good temperature stability, 300 to 350C
PBO-flourinated IPN	Foster-Millier	High temperature stability
Organo-ceramic hybrid nano composites	Garth Wilkes, VPI	Resistant to ionizing radiation; high thermal stability
Polybenzimidazole	Hoechst Celanese	Thermoplastic; excellent thermal stability above 300C
Flourinated PBO-PI	Hoechst Celanese	Combines polyimides with high temperature properties of LCP's

Thin films will also have a place when there is a need to integrate capacitors either onto high temperature electronic packages, or off chip as it is sometimes referred. A number of dielectric materials have been deposited in the form of thin films using techniques like MOCVD (Stauf 1998; Nami 1997), PECVD (Trigg 1998; Lenihan 1996), Anodization (Nelms 1998), Sputtering (Kapadia 1998; Kim 1998; Tsukada 1995; Simamoto1992; Vorotilov 1999; Suu 1998), Hydrolysis (Sakabe 1998), and PLD (O'Neill 1998; Noda 1999) etc.

Recently there has been a tremendous amount of interest in deposition of inorganic thin films using the sol-gel method. Very thin films of perovskite materials like $BaTiO_3$ or Lead based relaxor ferroelectrics have been fabricated by Vorotilov et al. to yield capacitance densities as high as 7 –9 $\mu F/ cm^2$.

Table 6.3

Some selected ceramic candidates for high temperature capacitors

Industry/Institution	Materials	Approach	Highest ε_r Achieved	Highest C (nF/cm^2)	Reference
Cornell University	Polymer/ceramic	Collodial dispersion	40		[Liang98]
TPL Industries	Nanocomposites	Surface treatment		25	[Slenes98]
3M Corporation		Roll to roll process		10	[O'Bryan98]
Georgia Institute of Technology		Dispersion control	135	22	
IBM		Conventional mixing	47		[Agarwal98]
Chalmers University of Tech, Sweden	Polymer/$BaTiO_3$/ Carbon	Conventional mixing	1960		[Levy98]
Ormet Corporation		Dry film/curtain coating	40	4	[Ardi97]
Institute for surface chemistry, Sweden	Nanocomposites	Dispersion optimization			[Brandt98]
Matsushita Electric Works	Polyphenyleneoxide-TiO_2	Lacquered film-gravure coat	12		[Bergstrom 97] [Simamoto 92]
Sandia National Laboratories	PZT and PLZT	Sol-gel	900		[Dimos94]
University of Delhi, India	$BaTiO_3$		370		[Sharma98]
Princeton University	Hydrothermal BT	Organo-metallic precursors			[Slamovich 96]
Hitachi Res. Lab., Hitachi Ltd., Japan	Ta_xO_y		28		[Ohishi92]
Electr.&Automation(Tech.Univ),Russia	PZT, SrBiTa Oxide films	Sol-gel; Photo Irradiation		7000-9000	[Vorotilov99]
Nanyang Tech. University, Singapore	Ba-Ti-B Glass Ceramic	Sol-gel	1000		[Yao98]
AVX Corporation	PbZT	Sol-gel, thick film printing		2500	[Liu99]
		Sol-gel			

European Input on Passive Device Selection

Unfortunately there was very little discussion on this study tour on passive device selection for high temperature applications. All who spoke were in agreement that much more work needs to be done in this area. Dr. Roumen Kakanakov of the Institute of Applied Physics in Bulgaria indicated that his team had a

little experience with passive integration as well as passive component attachment using high temperature solders.

FIRST LEVEL PACKAGING

In this section we will consider some major elements of first level packaging that require serious consideration when packaging devices at elevated temperatures. These are the technology elements, which were discussed with the European researchers. For first level packaging we will only consider wirebond, die attach materials and contact metallization. Other issues such as encapsulants, hermetic lids, and C4 will not be discussed.

Wirebond

Connections between the IC device and the electronic package are commonly performed by one of three technologies: wirebond, solder, or controlled collapsed chip connection (C4). Of the three technologies, wirebond will be discussed here because it is the most prevalent and cost effective of the three and is being practiced by the Europeans as the desired interconnection method for connecting the wideband gap devices to the package. It should also be noted that wirebonding concurrently provides for thermal dissipation by backbonding or diebonding the chip to the substrate, as illustrated in Figure 6.1. This configuration allows for the designer to utilize some of the more thermally conductive substrates to facilitate heat removal from the backside of the die. However, the designer must also keep in mind that with wirebond, he or she will pay a price for lead inductance.

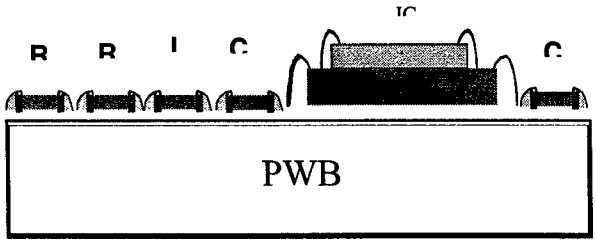

Fig. 6.1. Schematic representation of a wideband gap IC device mounted on a substrate and connected to it using wirebonds, which in turn is mounted to a PWB motherboard and connected by wirebonds.

Another critical factor that one must consider when operating at an elevated temperature is the material interactions that will occur between the wire and the pad to which it is being bonded to. Most high temperature applications tend to use aluminum wire to aluminum contacts. This particular union can withstand temperatures up to 600°C. Gold to gold bonding is also very reliable and can withstand temperatures up 1000°C. Designers should try to avoid bonding dissimilar metals such as Al to Au or Cu to Al, because of the brittle intermetallic phases that could form at elevated temperatures, which could thereby cause premature failures at the interface (Newsome 1976).

The researchers at Siemens, led by Professor Eckhard Wolfgang, were well aware of these concerns. They shared with us a six-chip multichip module that was being used in the braking system of a locomotive engine. Each locomotive would require 18 to 24 modules and would operate at temperatures between 110°C and 125°C. The module contained six thyristors that had 30 to 40 I/Os per chip and were wirebonded using aluminum wire to aluminum contacts. Professor Wolfgang's focus is in applications below 200°C.

In France, the researchers at LETI also showed us a packaged device, which was wirebonded onto a lead frame that they believed to be made of Mo-Cu. The researchers there did not know much detail regarding this package, since they outsource their packaging. We were later told the package was procured from Dr. Kakanakov of Bulgaria. It was unclear who performed the wirebonding.

Die Attach

Another critical element in the packaging of high temperature electronic devices is the die attach material. The die attach material is used to ensure that the device remains in place throughout the entire lifetime of the system. The die attach material should also have good thermal conductivity, as well as good contact resistance. There are a number of die attach materials, which have inherent advantages and disadvantages depending on the temperature of operation of the device. Table 6.4 displays temperature guidelines for a select number of die attach materials.

Table 6.4

Temperature guideline for Some Die Attach Materials (Manko 1992; Pecht 1994; Feinstein 1989; Khatchatourian 1995; Olson 1995)

Die attach material	Maximum use temperature	Reason
Au80Sn20	280°C	Eutectic melting point
Au88Ge12	356°C	Eutectic melting point
Au97Si3	363°C	Eutectic melting point
Sn96Ag4	221°C	Solidus
Sn95Sb5	235°C	Solidus
Sn92Sb8	236°C	Solidus
Sn65Ag25In10	236°C	Liquidus
Polyimide	300°C	Glass transition temperature
Silver filled glass	450°C	Softening point

In Europe, significant input on die attach materials was provided by Dr. Kakanakov. The following is a summary of our discussion relative to die attach materials and his rationale for material selection. After completion of this project in 1997, Kakanakov continued to make a small series of packages for power SiC MESFET'S from Thomson CSF. In early 1999 work began on the NATO project "High Power and High Frequency Devices on LPE-grown SiC films", where Kakanakov's group was responsible for R&D of packages and packaging of power SiC diodes (Kakanakov 1999). Two gold-based alloy materials were used as attach materials. The attach materials were gold based alloys of Au and (6%) Si, (12%) Ge. The 6% alloy has a melting point of 373°C, and the 12% alloy melts at 363°C. Kakanakov mentioned (but did not go into great detail) that his group also investigated AuSn (20%) alloy and an AuIn (25%) alloy which had a melting point of 450°C. The AuIn system exhibited a favorable melting point but there was significant concern regarding the oxidation of In at the high temperatures.

Contact Metallization

The contact metallization is very critical as it serves a number of purposes such as providing a wetting layer for the die attach material, as well as ensuring optimal adhesion between the device and the die attach material. The contact metallization should be resistant to oxidation and be thermally stable at elevated temperatures. Typically this metallization is accomplished in a multilayering arrangement. The first metal layer is usually an adhesive layer, typically Cr or Ti. The second layer in this metal stack is usually referred to as the barrier layer metal. It serves to protect the adhesive layer. Typical barrier metals may be Ni, Ni alloys, Co, Co alloys, Pt and phased CrCu alloys. The third layer is typically called the wetting layer. This layer allows for wetting of the die attach alloys to ensure a reliable contact. Work by Kakanakov showed that the contact metallization of TiPtAu was suitable for SiC MESFET devices up to joining temperatures of

400°C. The advantages here were that there was no change in thermal resistance during high temperature testing. However, Pt and Ti will dissolve in both of the solders when it is liquified, thereby indicating that more suitable barrier metallurgies will have to be identified at the temperature extremes. Kakanakov et al indicated that the solders used in this study were only in liquid state during chip attachment and not during actual device operation. To limit the solubility of their barrier metallization of platinum and increase adhesion, a new process was developed in their laboratories. The new process involved vibrating the device during attach. This resulted in a reduction of the bonding time and reduced dissolution of the Pt in the Au alloy solders, thereby enhancing adhesion and improving reliability. No additional details were given. Gold wiring bonding is performed using a ball bonder from K&S when making connections from the chip to the second level of packaging, the substrate. The substrate in this case is made of a CuMo alloy.

SECOND LEVEL PACKAGING

Second level packaging includes substrates, solders, connectors, housing and cables. However, in this section we will only discuss substrates and briefly mention solders since our discussions in Europe were limited to these areas. Dr. Kakanakov and Professor Wolfgang of Siemens provided the majority of the input from Europe for this section.

As mentioned earlier plastic substrates such as glass reinforced epoxy boards may not be satisfactory due to its low Tg and melting point. However, many designers are looking to a new class of organic boards called BT Resins, which offer the opportunity to meet some of the high temperature requirements just above 200°C. Although these organic materials have a fairly high Tg, they still are poor conductors of heat and therefore will require intricate cooling schemes to efficiently remove heat. Also organic materials such as BT resins will provide challenges from a thermal mismatch standpoint because of its large CTE > 17ppm/°C and polyimide another high temperature organic, which has a CTE of > 30ppm/°C. These materials may warrant consideration because of their low cost nature and the ability to procure them in bulk quantities.

On the other hand, there are a number of inorganic candidates, which should be satisfactory, both from a performance and cost standpoint to meet the needs of most of these high temperature applications. A leading candidate would certainly have to be ceramic substrates. Ceramics have typically been used for a number of high temperature applications such as Al_2O_3, AlN and glass ceramic. The majority of high temperature packaging, including the majority of automotive under the hood applications, consists of thick film hybrid cermet and ceramics (Aday 1993). One drawback of the ceramic however, is its thermal conductivity and its high cost relative to organics. DuPont addressed these cost issues with the introduction of their low temperature co-fired ceramic (LTCC) material. Here layers of unfired or "green tape" materials are circuitize and laminated to form a circuit and then simultaneously fired to form the final product at a low temperature.

Other inorganic substrate materials include silicon and metal alloys, such as Mo-Cu. Here one is afforded the ability to closely match the CTE of the high temperature device. However, there is one inorganic material, which has almost all of the desirable properties from a mechanical standpoint. That material is diamond, although cost remains a question mark (Tummala, 1989).

Another class of materials that may warrant consideration from a substrate standpoint are composites. These composites include fiber and particle reinforced metals and polymers as well as metal matrix composites. Because of the large amount of potential combinations of materials that may be suitable candidates, a summary of these materials is presented in Table 6.5.

Table 6.5

Potential composite material candidates

Fibers	**Advantages or Disadvantages**
Carbon	Inexpensive, Good thermal properties
Aramid	Good CTE match
High density polyethylene	Limited temperature capability
PBO, PBT, PBZT	Environmental out of favor now
Particles	
Silicon Carbide	Tailor CTE, good thermal
Aluminum Nitride	Tailor CTE, good thermal
Cubic Boron Nitride	
Matrices	
Aluminum	Lightweight, good thermal, CTE match
Cu	Lightweight, good thermal

At Siemens, Professor Wolfgang utilized ceramic substrates for the locomotive application. At IMC in Sweden, we were informed that ceramic substrates were also being used and being considered for gas sensor applications. At the University of Ulm, diamond substrates were being considered to package GaN devices, and in Bulgaria, Dr. Kakanakov is working with Mo(40%)Cu(60%) alloy substrate. It should also be mentioned here that Dr. Kakanakov is supplying a majority of the packaging for the SiC and GaN devices in Europe. It appears that the MoCu alloy that he is working with has been very well characterized and appears to perform well in reliability testing. The CTE of this alloy ($\alpha = 3.5 \times 10^{-6}$/K) is very close to that of SiC which is ($\alpha = 4.2 \times 10^{-6}$/K). The thermal conductivity of this alloy is also very good, with k = 245 W/mK.

Solders

I will briefly touch upon solders for high temperature applications. Solders are used for making connections from the device to first level packaging via C4 technology and connecting first level packaging to second level packaging via ball or stud grid array and in surface mount technology (SMT). In conventional packaging, eutectic Pb/Sn solders have been the primary workhorse for solder connections. However, for high temperature applications above 300°C this solder may not be satisfactory. Another force against Pb based solders is the drive towards green packaging technologies, or environmentally friendly materials, which precludes the use of Pb based solders in electronic applications. Materials currently receiving considerable attention as potential replacements to Pb/Sn solders include AgSn, AuSn, Cu, Sb and Bi as ternary alloys. High temperature conductive adhesives are being considered as well.

Reliability

We have listed a number of technical challenges and issues in the earlier sections of this chapter confronting the development and implementation of electronic packaging for high temperature devices. Another significant concern manifests itself in the ability to perform meaningful reliability testing, and data interpretation. A chief concern here is that there really does not exist an infrastructure for high temperature reliability testing. Most of the test equipment and chambers are set up for conventional package reliability

testing and therefore only cover a limited temperature range. All of the European researchers who are actively involved in packaging also realize that this is a valid concern, and are exploring means to fill this void. Professor Wolfgang of Siemens indicated that there is a real need to perform extended life cycle tests out to 35 years due to the fact that some products will have to survive in the field with no failures for that long. Siemens has also put a task force in place (RAPSDRA) to identify failures and failure mechanisms through accelerated testing, and develop a set of standards for power electronics that correspond to a 35 year life cycle. In addition Siemens is pursuing the following to gain more understanding on the reliability of their electronic packages at elevated temperatures of operation:

- Siemens would like built in reliability (monitor process parameters and materials)
- Developing standardization for accelerated testing (100x)
- Monitor operation of devices in real time (in-situ) using optical fibers
- Explore the theoretical limit for Si device operation (may be higher than 250°C)

Siemens has also developed reliability models that can be downloaded from their website at www.Infineon.com "SFET".

Dr. Kakanakov agrees that new reliability test equipment and methodologies may be needed for high temperature reliability assessment. Limited reliability data exists for some of his systems; however, some reliability studies were done using thermal resistance measurements. An important need for the advancement of high temperature electronic packaging will be the advent of better reliability modeling and simulation tools over and above what is currently being used today.

SUMMARY

I have tried to convey some of the challenges for the packaging of high temperature devices such as GaN and SiC. These challenges are not insurmountable and will be overcome when the proper resources are put into place to address specific areas. It appears that the Institute of Physics in Bulgaria, as well as Siemens in Germany are addressing a number of these issues already and have made significant progress in finding potential solutions for some applications. Of course there are a number of vertically integrated companies around the world, which have found solutions to most of the high temperature applications but at a cost premium. Here the challenge is to find similar cost performance packaging solutions for high temperature applications much like that of conventional Si IC packaging.

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CHAPTER 7

HIGH VOLTAGE SiC POWER DEVICES

T. Paul Chow

INTRODUCTION

Silicon has long been the dominant semiconductor of choice for high-voltage power electronics applications (Ghandhi 1998; Baliga 1996). However, recently, wide bandgap semiconductors, particularly SiC and GaN, have attracted much attention because they are projected to have much better performance than silicon (Shenai, et al. 1989; Baliga 1989; Bhalla & Chow 1994; Chow & Tyagi 1994). Compared to silicon, these wide bandgap semiconductors, SiC, GaN and InN can be categorized into one group while diamond, BN and AlN into another, because the former has bandgaps of 2-3.5 eV and the latter 5.5-6.5 eV. On the other hand, the Group IV or IV-IV semiconductors have indirect bandgaps whereas most of the Group III-nitrides are direct (except BN). The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10 to 35 orders of magnitude), a higher electric breakdown field (4-20 times), a higher thermal conductivity (3-13 times), a larger saturated electron drift velocity (2-2.5 times), when compared to silicon (See Table 7.1).

SiC has over 150 polytypes (which are different crystal structures with the same stoichiometry of a compound semiconductor). Also, only the 6H- and 4H-SiC polytypes are available commercially in both bulk wafers and custom epitaxial layers. Between the two polytypes, 4H-SiC has become preferred due to the more isotropic nature of many of its electrical properties. Besides these properties, the impact ionization coefficients of electron and hole are also very important for power device considerations. The experimental coefficients, usually extracted from breakdown characteristics of reverse-biased pn or Schottky junctions, are shown in Fig. 7.1 for both 6H- and 4H-SiC (Kyuregyan & Yurkob 1989; Konstantinov, et al. 1997; Raghunathan & Baliga 1997). Also included in the figure is the average ionization coefficient for 6H-SiC. Such an average ionization coefficient, usually modeled by a power law dependence on the electric field ($\alpha \propto \xi^n$, where n is 5 or 7), allows one to estimate analytically the breakdown voltage and depletion width at breakdown. (See Fulop 1967 for the silicon case and Ramungul, et al. 1995 for 6H-SiC.) For GaN, there are very little experimental data on the ionization coefficients, probably due to the high defect density of the heteroepitaxial grown layers (Dmitriev, et al. 1996). Theoretically calculated coefficients for both 3C-and 2H-GaN have been recently performed (Kolnik, et al. 1996; Oguzman, et al. 1997) and are shown in Fig. 7.2. It should be emphasized that, unlike in silicon, the hole ionization coefficient is mostly higher than the electron one within the electric field range shown in both SiC and GaN cases. Such trends have significant impact on bipolar transistor structure (npn vs. pnp) considerations, as will be discussed later. Another important parameter is carrier lifetime, and SiC, like silicon, is an indirect semiconductor whereas GaN, like GaAs, is a direct semiconductor. Consequently, SiC has minority carrier lifetimes much longer than those in GaN. Experimentally, recombination lifetimes > 1 μs have been extracted in 4H-SiC (Singh, et al. 1998) vs. 6ns in 2H-GaN Bandic, et al. 1998) experimentally).

In this chapter, the figures of merit for unipolar and bipolar devices for power electronic applications will be first discussed to demonstrate the potential performance improvement using wide bandgap semiconductors.

Then, the basic physics of operation and key device parameters of two-terminal rectifiers and three-terminal transistors and thyristors will be presented. Recent experimental highlights on high-voltage SiC devices are summarized. Also, the outstanding material and processing issues that need to be overcome for device commercialization will be pointed out.

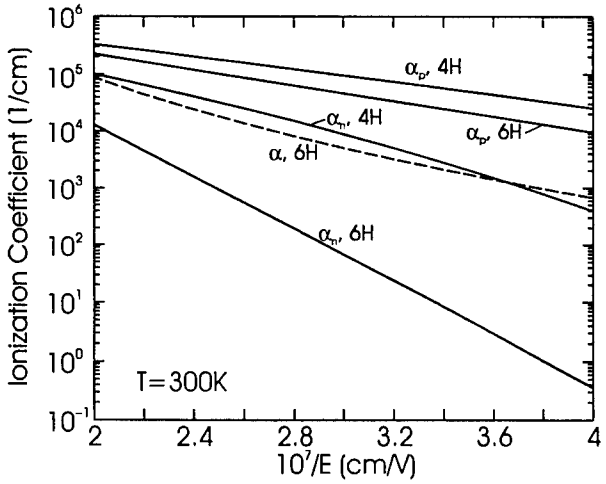


Fig. 7.1. Experimental impact ionization coefficients of electron and hole in 6H- and 4H-SiC

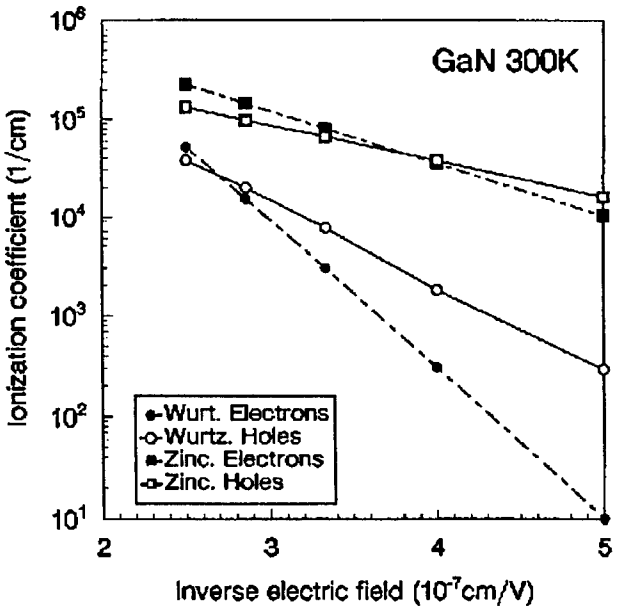


Fig. 7.2. Calculated impact ionization coefficients of electron and hole in 3C- and 2H-GaN

Table 7.1

Physical properties of important semiconductors for high-voltage power devices.

Material	E_g (eV)	n_i (cm^{-3})	ε_r	μ_n ($cm^2/V \cdot s$)	E_c (MV/cm)	v_{sat} (10^7 cm/s)	λ ($W/cm \cdot K$)	*Direct/ Indirect*
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim 10^{3}$	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3	D
3C-SiC	**2.2**	**6.9**	**9.6**	**900**	**1.2**	**2.0**	**4.5**	**I**
4H-SiC	**3.26**	**8.2×10^{-9}**	**10**	**720[a] 650[c]**	**2.0**	**2.0**	**4.5**	**I**
6H-SiC	**3.0**	**2.3×10^{-6}**	**9.7**	**370[a] 50[c]**	**2.4**	**2.0**	**4.5**	**I**
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0*	13	I
ALN	6.1	$\sim 10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Note: *a* — mobility along a-axis, *c* — mobility along c axis, *— estimate.

FIGURES OF MERIT

To quantify the performance enhancement possible with SiC and GaN, several unipolar and bipolar figures of merit have been proposed (Shenai, et al. 1989; Baliga 1989; Bhalla & Chow 1994; Chow & Tyagi 1994). For the high-voltage power FET's, such as MOSFET, JFET and HEMT, unipolar figures of merit apply (though the channel mobility may depend on the FET structures). In Table 7.2, the various unipolar figures of merit for the semiconductors are shown, and SiC and GaN offer more than an order of magnitude improvement over silicon. These figures assume different heat sinks and operating frequency (Shenai, et al. 1989). Bipolar transistors, such as BJT, IGBT and HBT, need to use bipolar figures of merit. Among the bipolar transistors, we can classify them into two groups, those with odd number and those with even number of junctions. The BJT has an even number of junctions and hence its on-state voltage can be minimized through cancellation of junction voltages when it is in saturation. In this case, SiC clearly excels over Si over all switching frequencies and the power dissipation is clearly smaller in SiC transistors, as shown in Table 7.3. By contrast, the Insulated-Gate Bipolar Transistor (IGBT) (Baliga 1996), which is the dominant silicon power transistor structure, has an odd number of junctions in its structure and its forward drop cannot be

reduced to less than a diode drop. Since SiC has a large diode turn-on voltage due to its larger bandgap, its conduction loss cannot be less than the silicon device at low to medium current density and only yields a lower total power loss when the switching frequency exceeds a certain frequency, f_{inin} (Bhalla & Chow 1994).

Table 7.2

Normalized unipolar figures of merit of important semiconductors for high-voltage power devices (Baliga 1989).

Material	λ	JM $(E_c v_{sat}/\pi)^2$	MJM λ*JM	KM $\lambda(v_{sat}/\varepsilon_r)^{1/2}$	Q_{F1} $\lambda\sigma_A$	Q_{F2} $\lambda\sigma_A E_c$	BM (Q_{F3}) $\varepsilon_r \mu E_c^3$	BHFM μE_c^2
Si	1	1	1	1	1	1	1	1
Ge	0.4	0.03	0.012	0.20	0.06	0.02	0.2	0.3
GaAs	0.33	7.1	2.4	0.45	5.2	6.9	15.6	10.8
GaP	0.53	37	20	0.7	10	40	16	5
InN	-	58	-	-	-	-	46	19
GaN	0.87	760	655	1.6	560	6220	650	77.8
3C-SiC	3	65	195	1.6	100	400	33.4	10.3
4H-SiC	3	180	540	4.61	390	2580	130	22.9
6H-SiC	3	260	780	4.68	330	2670	110	16.9
Diamond	13.3	2540	33800	32.1	54860	1024000	4110	470
BN	8.7	1100	9700	11	715	23800	83	4
AlN	1.7	5120	8700	21	52890	2059000	31700	1100

Table 7.3

A bipolar figure of merit applied to the power pin junction rectifier (calculated at J_F = 100A/cm^2, BV = 1000V) (Baliga 1989).

Name	N_d (cm^{-3})	W_{N^-} (μm)	V_F (V)	J_{end} (A/cm^2)	J_{off} (A/cm^2)	t_s (μs)	t_{f1} (μs)	t_{f2} (μs)	E_{off} (mJ)	f_{min} (KHz)
Si	1.3×10^{14}	100	0.88	9.7	2×10^{-5}	7×10^{-3}	0.81	0	5.4×10^{-3}	-
Ge	4.4×10^{13}	285	0.60	8.3	8×10^{-2}	7.6×10^{-3}	1.8	0	6.2×10^{-3}	0
3C-SiC	3.8×10^{15}	33.1	2.00	42.8	2×10^{-15}	4.4×10^{-3}	0.2	2.2×10^{-3}	2×10^{-2}	1.62
6H-SiC	1.6×10^{16}	23.9	2.65	46.2	3×10^{-21}	1.0×10^{-2}	0.14	4.6×10^{-3}	5.5×10^{-3}	1.82
Diamond	1.2×10^{17}	72.0	5.21	93.4	5×10^{-44}	2.6×10^{-5}	0.02	1×10^{-2}	1.1×10^{-3}	4.12

This f_{min}, at which the conduction loss is equal to the switching loss (at 50% duty cycle), has been considered as the bipolar figure of merit, and, in the case of a 1000V IGBT, is about 20KHz for SiC when compared to silicon, as illustrated in Table 7.4.

Table 7.4

A bipolar figure of merit applied to the power npn BJT (calculated at J_F = 100 A/cm^2, BV = 1000V, β = 10) (Bhalla & Chow 1994).

Name	N_d (cm^{-3})	W_{N^-} (μm)	V_F (V)	J_{off} (A/cm^2)	t_s (μs)	t_f (μs)	E_{off} (mJ)	P_1* (KW/cm^2)	P_{100}* (KW/cm^2)
Si	1.3×10^{14}	100	22.9	2.0×10^{-5}	1.0	0.02	3.3	1.15	1.48
Ge	4.4×10^{13}	200	50.6	6.8×10^{-2}	1.0	1.4×10^{-2}	6.4	2.57	3.20
3C-SiC	3.8×10^{15}	16.7	0.067	2.0×10^{-15}	6.3×10^{-4}	9.6×10^{-2}	13	0.016	1.3
6H-SiC	1.6×10^{16}	8.33	0.086	2.8×10^{-21}	1.9×10^{-3}	0.02	27	0.031	2.7
Diamond	1.2×10^{17}	2.3	0.094	5.5×10^{-44}	1.7×10^{-4}	0.42	5.8	0.011	0.58

Note: *P_1 and P_{100} is the power density dissipated at a switching frequency of 1 and 100 KHz respectively.

No figure of merit applicable to any unipolar or bipolar heterojunction transistor structure has been proposed. However, if we consider the SiGe as the equivalent silicon standard in heterojunction devices, we can readily compare it to AlGaAs and AlGaN system and conclude qualitatively that the latter two have similar magnitudes of improvement over the silicon case as in the FET case in Table 7.2. Heterojunction bipolar transistor comparisons are more complicated and dependent on whether the semiconductors have direct and indirect bandgaps. Simplistically, since we have already concluded that SiC is better than Si, it is fair to analogously point out that the AlGaN/GaN HBT is superior to the AlGaAs/GaAs HBT due to higher avalanche field and better thermal conductivity.

Table 7.5

A bipolar figure of merit applied to n-channel IGBT (calculated at J_F = 100 A/cm^2, BV = 1000V, α_{PNP} = 0.14) (Bhalla & Chow 1994).

Name	N_d (cm^{-3})	W_{N^-} (μm)	τ_{n0} (μs)	V_F (V)	W_R (μm)	J_{off} (A/cm^2)	τ_B (μs)	E_{off} (mJ)	f_{min} (KHz)
Si	1.3×10^{14}	100	1.0	1.2	6.0	2.0×10^{-5}	0.285	2.55	-
Ge	4.4×10^{13}	200	0.95	0.63	12.0	8.5×10^{-2}	0.302	2.70	<190
3C-SiC	3.8×10^{15}	16.7	0.37	2.74	1.0	5.4×10^{-15}	0.058	0.55	38.4
6H-SiC	1.6×10^{16}	8.33	0.15	2.97	0.5	1.8×10^{-20}	0.016	0.15	36.9
Diamond	1.2×10^{17}	2.3	0.0011	5.04	0.14	5.0×10^{-44}	0.6×10^{-4}	5.0×10^{-4}	75.3

Table 7.6

A bipolar figure of merit applied to gate turn-off (GTO) thyristor (calculated at J_F = 100 A/cm^2, BV = 1000V, turn-off gain of 4) (Bhalla & Chow 1994).

Name	N_d (cm^{-3})	W_{N^-} (μm)	V_F (V)	J_{off} (A/cm^2)	β_{max}	J_{ATO} (A/cm^2)	t_s (μs)	t_{fl} (μs)	E_{tfl} (mJ)	E_{tail} (mJ)	f_{min} (KHz)
Si	1.3×10^{14}	144	0.99	2.9×10^{-5}	5.8	1.1×10^{3}	0.3	0.58	9.6	24	-
Ge	4.4×10^{13}	285	0.60	1.1×10^{-1}	5.5	3.0×10^{3}	0.26	0.62	10	24	<53.7
3C-SiC	3.8×10^{15}	33.1	2.00	3.9×10^{-13}	25.1	2.6×10^{3}	1.4×10^{-2}	0.29	4.8	24	10.5
6H-SiC	1.6×10^{16}	23.9	2.65	7.9×10^{-19}	88	1.8×10^{4}	1.1×10^{-2}	0.19	3.1	24	12.6
Diamond	1.2×10^{17}	72.0	5.21	1.7×10^{-41}	2.3×10^{4}	8.0×10^{8}	4.1×10^{-5}	0.029	0.48	24	23.2

One of the basic building blocks of a power circuit is the half-bridge circuit (Fig. 7.3), in which two parallelly connected dc three-terminal switch and two-terminal flyback rectifier combinations are connected in series. Thus, it can be seen that both two- and three-terminal switching devices are needed. There are basically two families of two- and three-terminal power semiconductor switching devices - the Schottky rectifier and the power FET representing the unipolar family and the junction rectifier, the bipolar junction transistor and the thyristor belonging to the bipolar family. Also, for three-terminal devices, dependent whether a current or voltage signal is used for control, it can be separated into two more branches. While traditional power device switches use current for control (like the power Bipolar Junction Transistor (BJT), Silicon-Controlled Rectifier (SCR) and Gate-Controlled Thyristor (GTO) (Ghandhi 1998), modern power devices (like the power MOSFET, Insulated-Gate Bipolar Transistor (IGBT) and MOS-Controlled Thyristor (MCT) (Baliga 1996) prefer the usage of a MOS voltage control for reduced control circuit complexities and enhanced device diagnostics features, but at the expense of device yield limitations from gate oxide failures. As will be shown below, at a system dc voltage of 5000V or higher and a device operating temperature higher than 150°C, we expect MOS-gated bipolar transistors and thyristors to be superior to unipolar transistors and are the devices of choice for electrical vehicle applications. Due to the fact that all (except BN) of the Group III-nitrides are direct bandgap semiconductors and hence low minority carrier lifetimes, only Schottky rectifiers and field-effect transistors (FET's), such as JFET, MESFET, MOSFET or HEMT, and low-voltage (< 1000V) Heterojunction Bipolar Transistor (HBT) need to be considered.

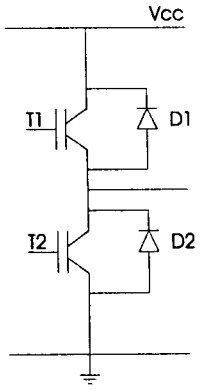


Fig. 7.3. Schematic of a half-bridge circuit

The unipolar and bipolar figures of merit mentioned above compare silicon devices with the wide bandgap ones of the same type. However, for each semiconductor, dependent on its bandgap, there is a crossover in voltage rating above which bipolar devices are preferred over unipolar ones due to the reduced drift-layer resistance from conductivity modulation of bipolar carrier injection. For silicon, this voltage is about 300V whereas, for SiC, it is about 3000V. Also, with increasing operating temperature, this crossover voltage is expected to decrease since the ON-resistance of unipolar devices varies inversely as the second power of temperature while the turn-on voltage decreases and carrier lifetimes increase. We will discuss this crossover in more detail in the rectifier and transistor sections below.

Besides device type, n-channel or npn type devices are chosen over p-channel or pnp counterparts in silicon. The reason for this is the higher electron mobility and lifetimes. On the other hand, the higher impact ionization of electrons leads to a poorer SOA. In SiC, electron also has a higher mobility but has a lower impact ionization capability than holes. These considerations lead to the inclusion of p-channel IGBT in SiC.

For AlGaInN alloys, since the MOSFET's are usually normally off whereas JFET's, MESFET's and HEMT's are usually normally on, the latter has disadvantages for power switching applications due to the excessive off-state loss unless a diode is connected in series and the resulting performance is degraded. While the conventional JFET's and HEMT's can be designed to have a normally-off mode of operation, they have a more limited gate voltage swing and increased channel resistance. On the other hand, the separation of the doping layer from the channel conduction layer in the HEMT drastically reduces carrier-impurity scattering in the channel and significantly improved the carrier channel mobility and thus on-resistance. Furthermore, among the wide bandgap semiconductors, the MOS technology has been developed only for SiC while the heterojunction HEMT has only been shown for the III-nitrides. Also, the gate capacitance is higher for MOSFET than for HEMT or MESFET. Details of the homojunction FET's will be discussed later in this chapter.

As mentioned earlier, we have approximated the electron and hole ionization coefficients using a power law. Then, we obtain the ideal breakdown voltage (BV_{pp}) and depletion layer width at breakdown (W_{pp}) as a function of background doping, as shown in Fig. 7.4 for 6H- and 4H-SiC. These analytical calculations have been corroborated well with numerical simulations and experimental results. It can be seen that, for the same background doping and along the c-axis, 6H-SiC has a 10-15% higher BV than 4H-SiC, despite the larger bandgap of the latter. Also, the effective avalanche field estimated for doping concentration of 10^{15} to 10^{17} cm^{-3} is the range 2.5 to 5 x 10^6 V/cm, close to the experimental value of 2-3 x 10^6 V/cm. Also, in contrast to silicon, the breakdown voltage of SiC was observed to decrease when temperature increases, but is now attributed to defect influence. The BV of high-quality (and small-area) 6H- and 4H-SiC devices has been shown to have a positive temperature coefficient (Neudeck & Fazi 1997).

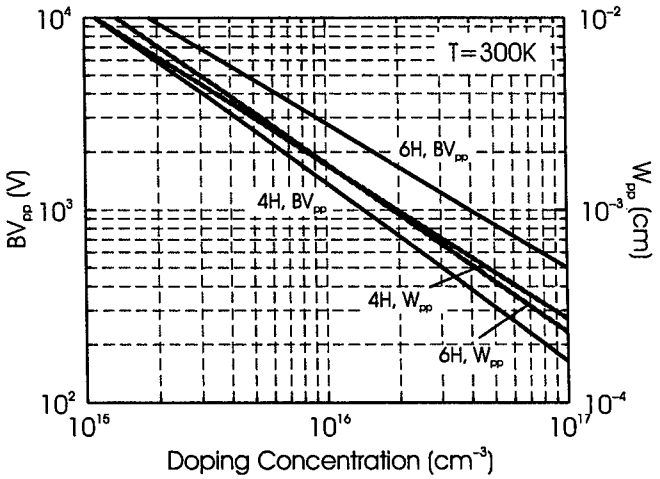


Fig. 7.4. Breakdown voltage of parallel-plane, one-sided abrupt junction (BV_{pp}) and its depletion layer width at breakdown (W_{pp}) for 6H- and 4H-SiC at 300K

The breakdown voltages of bipolar transistor structures are generally lower than those of pn junctions due to current gain. Fig. 7.5 shows the breakdown voltage of open base transistor in 6H-SiC for several carrier diffusion lengths. High voltage open-base bipolar transistor BV (BV_{CEO}) design depends primarily on minority carrier lifetime and $BV_{CEO} \propto (1 - \alpha_0)^{1/n}$, where α_0 is the common-base current gain, n is 4 for npn and 6 for pnp transistors in silicon. For 4H-SiC, we have found that n is 13 for npn and 3 for pnp (Fig. 7.6). Proper termination (Ghandhi 1998; Baliga 1996) must also be designed and processed to minimize the effect of junction curvatures.

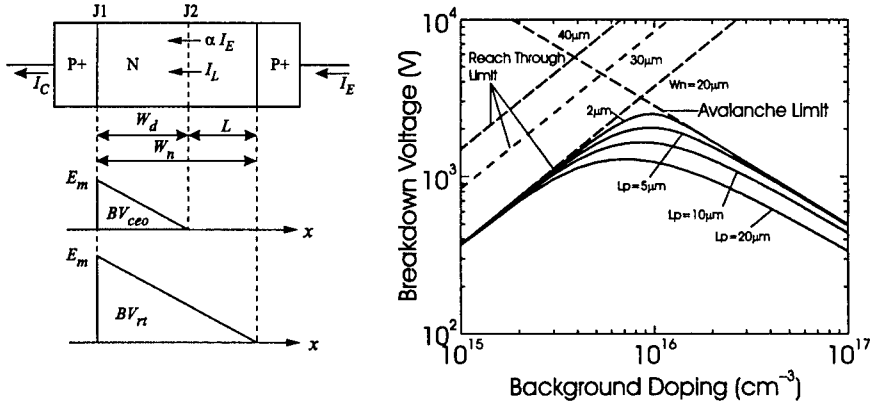


Fig. 7.5. Breakdown voltage of open base bipolar transistors in 6H-SiC

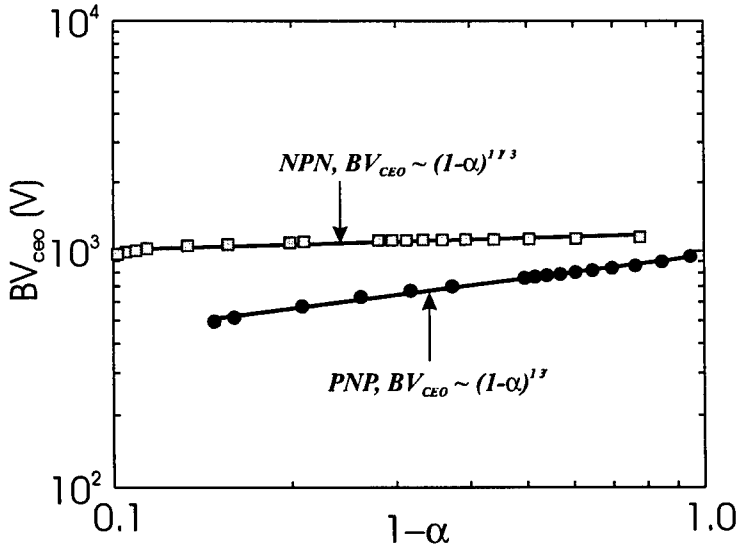


Fig. 7.6. Breakdown voltage of open base bipolar transistors in 6H-SiC

POWER RECTIFIERS

Generally, high-voltage power rectifiers are categorized into two classes – the unipolar Schottky rectifier and the bipolar junction rectifier (Baliga 1996). The schematic cross-sections of the basic structures of these two rectifiers are shown in Fig. 7.7. High-voltage Schottky rectifiers offer fast switching speed but suffers from high on-state voltage drop and on-resistance because mostly majority carriers participate in its forward conduction. By contrast, the pin junction rectifier has low forward drop and high current capability due to conductivity modulation, but has slow reverse recovery characteristics due to minority carrier storage. To combine the best features of these two rectifiers, hybrid rectifier structures, such as the Junction Barrier Schottky (JBS), Merged Pin/Schottky (MPS) and MOS Barrier Schottky (MBS) rectifiers have been proposed and have been demonstrated in silicon (Wilamowski 1983; Baliga 1984; Baliga & Chang 1987;

Mehrotra & Baliga 1995). The trench version of the MBS rectifier is schematically shown in Fig. 7.8(a) while the planar version of the JBS/MPS rectifiers are shown in Fig. 7.8(b).

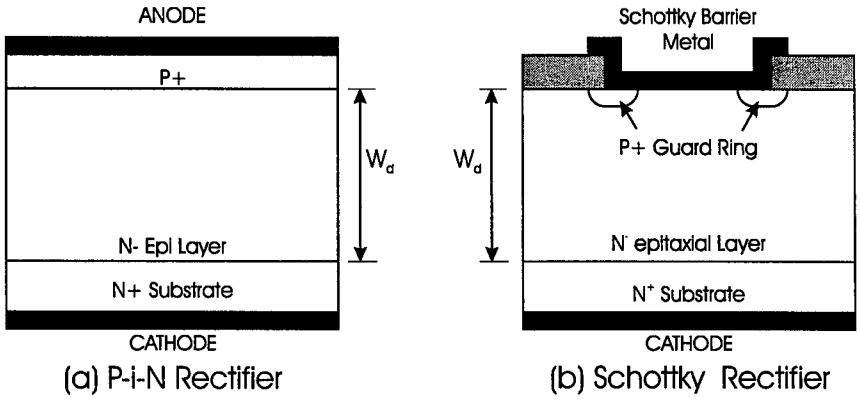


Fig. 7.7. Schematic device cross-sections of (a) pin junction rectifier (b) Schottky barrier rectifie

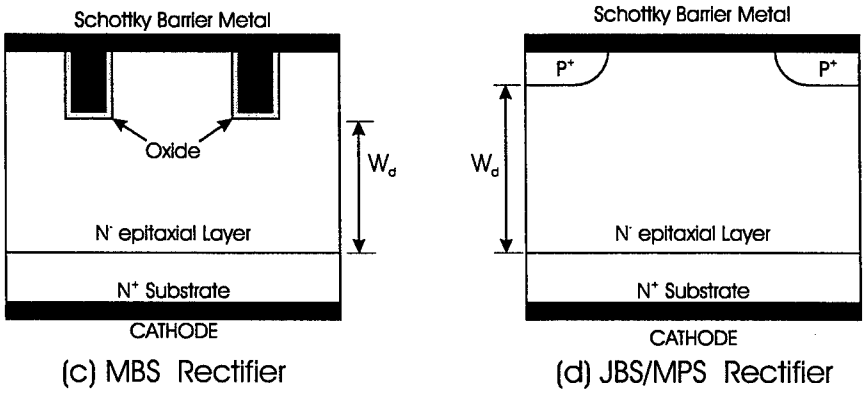


Fig. 7.8. Schematic device cross-sections of (a) Trench MOS-Barrier Schottky (TMBS) rectifier, and (b) planar Junction Barrier Schottky (JBS) or Merged PiN/Schottky (MPS) rectifier

Whether a unipolar or a bipolar rectifier is preferred depends on many device parameters, such as reverse blocking voltage, forward current density, maximum allowable reverse current density, operating temperature and switching frequency. The particular device type is often chosen to either minimize the total power dissipation or maximize the safe-operating-area (SOA) during device turn-on or turn-off. If we only focus on forward conduction, we note that the turn-on voltage of silicon rectifier is only 0.7V while that of the 4H-SiC rectifier is about 2.5V (the turn-on voltage is approximately 75% of the bandgap). Consequently, as shown in Fig. 7.9, the crossover voltage for 6H-SiC rectifier operating at 100 A/cm^2 exceeds 3000V at room temperature but drops to about 2000V at 300°C. (That for 4H-SiC devices is slightly higher due to the 0.2eV larger bandgap.) Practically, the crossover voltage is below this estimate because other factors, such as reverse leakage current density and forward over-current density tend to lower this crossover voltage. For example, while the crossover voltage based on forward conduction considerations alone for silicon would be 300V, the maximum reverse voltage for commercial silicon Schottky rectifiers is only 100V. We estimate the practical upper reverse blocking voltage limit for 4H-SiC rectifiers is about 2000V. Similar considerations also apply to the crossover voltage between unipolar and bipolar transistors.

As far as the process technology is concerned, the Schottky rectifier is constructed on the metal-semiconductor junctions whereas the junction rectifier is based on the pn junctions. The device process technology of the former depends on the choice of the Schottky metal as well as on the surface cleaning techniques and post-metal deposition annealing procedure. By contrast, the junction rectifier characteristics are controlled by the pn junction formation technology, the most popular of which are in-situ doped epitaxy

and compensation doping by ion implantation. Due to its bipolar nature, the junction rectifier is very sensitive to the carrier lifetimes of the material.

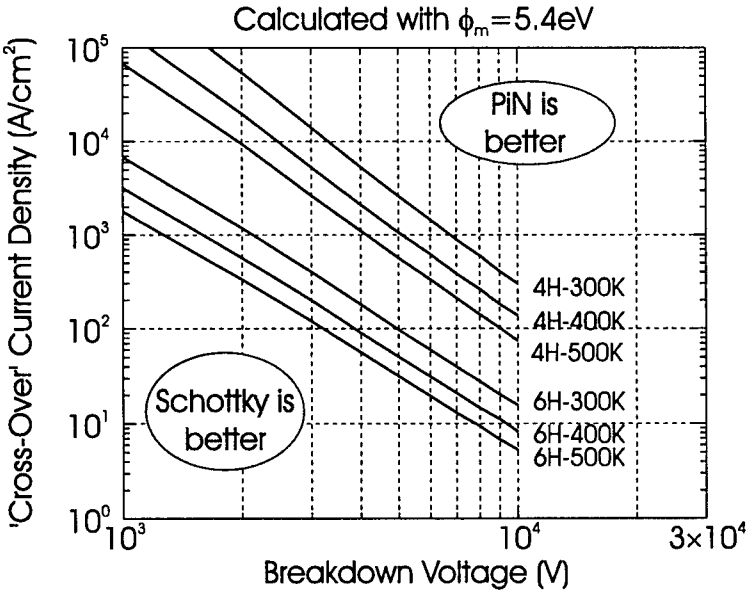


Fig. 7.9. Crossover voltage between Schottky and junction rectifiers at different operating temperature for 6H-SiC and 4H-SiC

We will examine the characteristics of these rectifiers and their SiC experimental realizations in the following sections. A list of experimental results on high-voltage rectifiers in 6H- and 4H-SiC is shown in Table 7.7.

SCHOTTKY RECTIFIERS

The Schottky barrier rectifiers are attractive due to their fast switching speed. This device exhibits fast reverse recovery with no reverse current and no forward over-voltage transient because the forward current transport is mainly carried out by majority carriers and minority carriers are mostly absent.

The electrical parameters of the Schottky rectifier is primarily determined by the drift layer thickness (W_d) and doping (N_d), and the metal-to-semiconductor Schottky barrier height (ϕ_B). The drift layer design can be performed using Fig. 7.4. For example, for a 1000V 4H-SiC Schottky rectifier, a drift layer thickness of 12μm and doping of $1.3\text{x}10^{16}$ cm^{-3} are needed. Besides the one-dimensional breakdown design, termination is necessary to prevent edge breakdown at the device peripheries due to electric field crowding. As can be seen from Fig. 7.5(a), a pn junction guard ring is almost always placed at the edges. In addition, termination techniques, such as floating field rings, field plates and junction termination extension, are used to eliminate the effect of junction curvature on the BV, leading to device BV that is within 95% of the BV of a parallel-plane junction.

In the on-state, unlike the low-voltage counterpart, the on-state voltage of the high-voltage power rectifier is determined by the voltage drops across the metal-semiconductor junction, the lightly doped drift region and the heavily doped substrate (Baliga 1996). To estimate the voltage drop across the metal-semiconductor junction, a thermionic emission model (Sze 1981) is often employed for Si and apparently can be extended to

Table 7.7

A list of SiC power rectifiers that have been experimentally demonstrated.

DEVICE TYPE	POLYTYPE	Power Ratings	Features	Developer
Schottky	6H-SiC	1100V	Ni, Field plate term.	U. of Cincinnati, 1995
	4H-SiC	1750V	Ti, C-Face, B+ edge term, n= 1.02, V_{F100}= 1.12V, 5mΩ·cm^2	Kyoto U., 1995
	4H-SiC	1720V	Ni, B+ edge term, 5.6mΩ·cm^2	Purdue U., 1997
	4H-SiC	3KV	Ni, Field plate term., V_{F100}= 7.1V, 34mΩ·cm^2	Linköping U./ABB, 1997
Junction	6H-SiC	2000V, 1mA		NASA, 1993
	6H-SiC	4.5KV, 20mA	V_{F100}= 6V	Linköping U./ABB, 1995
	6H-SiC	1325V	Floating field rings term.	ABB, 1995
	4H-SiC	3.4KV	JTE, V_{F100}= 6V	ABB, 1997
	4H-SiC	> 5.5kV		Cree, 1998
	4H-SiC	2KV, 5A	JTE, V_{F500}= 4.0V, 2.2mΩ·cm^2, Al-implanted	Siemens, 1998
	4H-SiC	3KV, 7A	JTE, V_{F500}= 4.8V, 3.0mΩ·cm^2, Al-implanted	Siemens, 1998
	4H-SiC	600V	JTE, V_{F100}= 6.0V, n+pp+ Phosphorus-implanted	RPI, 1998
	4H-SiC	1.1KV	JTE, V_{F100}= 3.4V, Al/C- and B-implanted	RPI, 1999
	4H-SiC	3.5KV	JTE, V_{F100} < 4V Al- and B-implanted	ABB, 1999
	4H-SiC	> 4.5KV	JTE, V_{F100}= 4.2V Al/C- and B-implanted	RPI/GE, 1999
	4H-SiC	4.9KV	JTE, V_{F100}= 4.2V Al-implanted	Siemens, 1999
MPS/JBS	4H-SiC	~ 750V	Ti, V_{F100}~ 1.5V	Daimler-Benz, 1997
JBS	4H-SiC	870/1KV	Ti, V_{F100}= 3.1V, 19mΩ·cm^2	Royal Inst./ABB, 1997
	6H-SiC	540/850V	Ti, V_{F100}= 5.3V, 43mΩ·cm^2	**Royal Inst./ABB, 1997**

SiC. The Schottky barrier height, ϕ_B, which controls the asymmetric current flow across the Schottky junctions, is ideally described as

$$\phi_B = \phi_M - \chi \qquad (1)$$

where ϕ_M is the metal work function and χ is the electron affinity. For silicon and GaAs, due to surface states, such an ideally relationship has been found not to hold. For 6H-SiC, the Schottky barrier of several metals has been experimentally measured and found to be closer to ideal with a slope of about 0.7 in the ϕ_B vs. ϕ_M plot (vs. unity for the ideal case) (Itoh, et al. 1995).

The specific on-resistance, $R_{ON,sp}$, of the Schottky rectifier can be expressed as a sum of the drift layer and substrate specific resistances, R_d and R_{sub}, respectively.

$$R_{ON,sp} = R_d + R_{sub} = R_d + \rho_{sub} W_{sub} \qquad (2)$$

where ρ_{sub} and W_{sub} are the resistivities and thickness of the substrate respectively. The specific drift layer resistance is

$$R_d = 4 (BV)^2/(\mu \varepsilon_S \xi_C^3) = 2.78 \times 10^{-12} (BV)^{2.5} \quad \text{in } \Omega\text{-cm}^2 \text{ for 4H-SiC} \qquad (3)$$

where μ is the carrier mobility, ξ_C is the critical field at breakdown, and ε_S is the semiconductor permittivity. Fig. 7.10 illustrates the $R_{ON,sp}$ vs. BV relationship calculated for n-type Schottky rectifiers on silicon, 6H-SiC and 4H-SiC. The substrate thickness and resistivity to be 300 μm and 0.01, 0.03 and 0.015 Ω-cm for Si, 6H-SiC and 4H-SiC, respectively. Also, the electron mobility in the drift layer is taken to be 450 and 1000 cm^2/ V-sec for 6H-SiC and 4H-SiC, respectively. At low values of BV (< 500V for SiC), the specific on-resistance is dominated by the substrate resistance. When the BV exceeds 1000V, the drift resistance starts to be the main limiting factor and the increase in R_d is a direct consequence of the increase in drift layer thickness and reduction in drift layer doping.

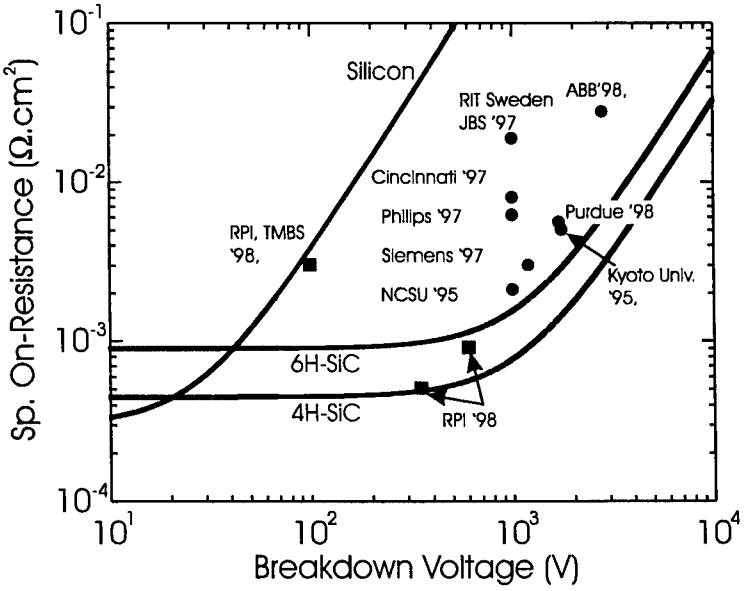


Fig. 7.10. Specific ON-resistance vs. reverse blocking voltage for Schottky rectifiers on Si, 6H- and 4H-SiC

We have also included recent published experimental results (Bhatnagar, et al. 1992; Raghunathan, et al. 1995; Itoh, et al. 1995; Ueno, et al. 1995; Weitzel, et al. 1996; Mitlehner, et al. 1997; Saxena & Steckl 1997; Sing & Palmour 1997; Wahab, et al. 1998; Schoen, et al. 1998; Khemka, et al. 1998) in Fig. 7.10. As seen in the figure, experimental SiC Schottky rectifiers have achieved significant improvement over Si counterparts,

but they are still far from the theoretical predictions. The highest reverse blocking voltage reported so far for a 4H-SiC Schottky rectifier is about 3000 V. Several termination techniques (Itoh, et al. 1995; Ueno, et al. 1995; Bhatnagar, et al. 1993; Alok & Baliga 1997) have tried to maximize the BV and minimize the reverse leakage current.

Based on the modified thermionic emission model, the total voltage drop across the Schottky rectifier can be written as (Baliga 1996)

$$V_F = (nkT/q) \ln (J_F/A^{**} T^2) + n \phi_B + R_{ON,sp} J_F \qquad (4)$$

where n is the ideality factor, k is the Boltzmann's constant, J_F is the forward conduction current density and T is the temperature. A** is the Richardson's constant whose value has been experimentally determined to be 140 A/cm^2-K^2 on 4H-SiC using log J-V-T measurements and is in good agreement with the theoretical estimated value of 146 A/cm^2-K^2 (Khemka, et al. 1998). When the BV of the Schottky rectifier increases, the forward drop increases with $R_{ON,sp}$ as shown in Eq. (4). Changing the barrier height also influences V_F directly. Fig. 7.11 shows the calculated forward drop of 4H-SiC Schottky rectifier at 100 A/cm^2 as a function of BV for barrier heights ranging from 1 to 1.75 V. V_F does not increase up to a breakdown voltage rating of 2000 V, beyond which a rapid increase is observed, mainly due to the increase in $R_{ON,sp}$. Also included in Fig. 7.11 are the recently reported values of V_F of many Schottky rectifiers at 100 A/cm^2. While several metals have been employed to form Schottky rectifiers, the most popular metals are titanium (Ti) and nickel (Ni) because near-ideal junction characteristics have been reported for these. Barrier heights of 1.25 and 1.69 V have been measured for Ti and Ni respectively. However, the experimental characteristics of many of the high-voltage rectifiers still fall short of the theoretically predicted values, usually attributed to parasitic contact resistance, resistive shunt defects across the metal-SiC junction, and bulk defects.

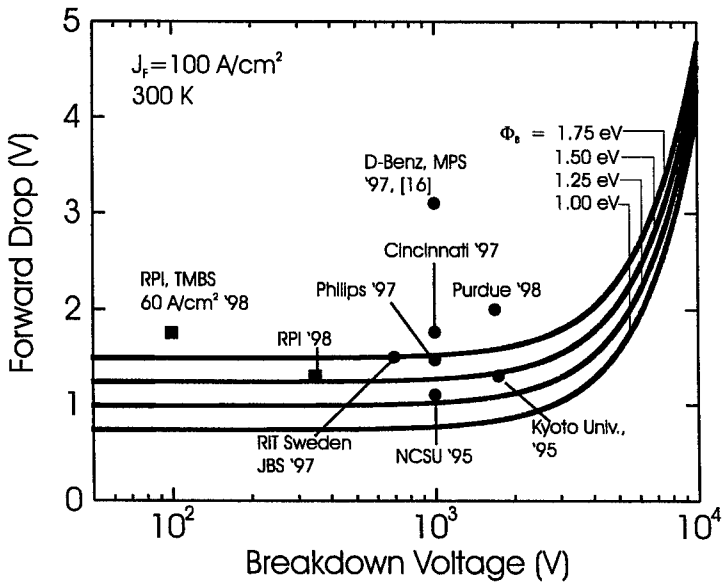


Fig. 7.11. Forward voltage drop vs. breakdown voltage for various Schottky rectifiers on 4H-SiC

The forward drop of a Schottky rectifier is also a function of temperature (Eq. (4)). With increasing temperature, the drift layer resistance increases because of a decrease in mobility. Consequently, the forward drop increases with temperature. Although it is also possible to decrease the forward drop with a Schottky metal having a low ϕ_B, such a choice is not utilized because it leads to a drastic increase in reverse leakage current density, and, in turn, an increase in off-state power dissipation.

The off-state reverse leakage current in SiC Schottky rectifiers can have contributions from thermionic emission, field emission, space-charge generation, edge and surface leakage as well as defect-related leakage. In addition, the thermionic emission component is affected by barrier lowering due to image force (Sze 1981). In the case where this current component is dominant, the reverse current can be expressed as

$$J_R = - A^{**} T^2 \exp [- q (\phi_B - \Delta\phi_B)/ kT] \qquad (5)$$

where $\Delta\phi_B$ is the decrease in Schottky barrier height due to image force and it can be written in terms of the maximum electric field at the junction

$$\Delta\phi_B = (q \xi_m / 4\pi\varepsilon_S)^{1/2} \qquad (6)$$

where ξ_m is the peak electric field at the Schottky junction. Experimental reverse leakage current in SiC Schottky diodes have been reported to have orders of magnitude higher than that predicted by the thermionic emission model and a stronger voltage dependence than that given by the image-force induced barrier lowering (Khemka 1998). To provide additional leakage current mechanisms, surface inhomogeneities have been proposed as possible shunt paths across the metal-semiconductor junctions (Bhatnagar, et al. 1996). Fig. 7.12 summarizes the measured reverse leakage current of 4H-SiC Schottky diodes at room temperature reported in the literature. While some of the data points have been measured at reverse biases near the breakdown voltage where pre-avalanche multiplication has a significant contribution to the leakage current, the leakage current of all of the Schottky devices are orders of magnitude higher than the theoretical prediction, even on devices with edge terminations. Recently, a large improvement in the leakage current was achieved on Schottky rectifiers fabricated on 4H-SiC films grown using a hot-wall CVD technique (Wahab, et al. 1998), indicating that bulk defects, rather than surface passivation, may be responsible for a major part of the leakage current.

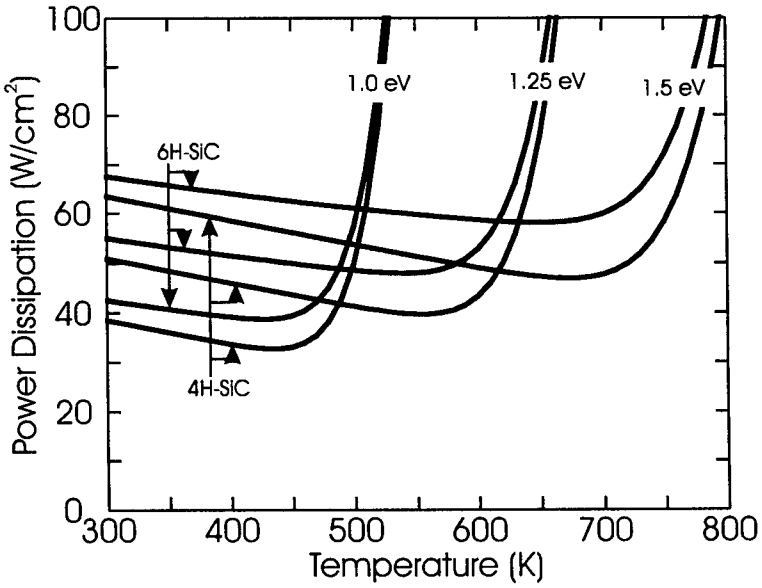


Fig. 7.12. Theoretical reverse leakage current, as predicted by the thermionic emission model and including Schottky barrier lowering as a function of reverse blocking voltage

It should be pointed out that both forward and reverse currents can be strongly influenced by processing conditions, such as surface cleaning techniques (Itoh, et al. 1995; Alok, et al. 1998) and plasma etching damage (Khemka, et al. 1998). Since the details of device fabrication are usually not described, it makes comparisons of experimental data from different research groups very difficult.

The power dissipation (P_D) of a Schottky rectifier consists of only the on-state conduction loss and the off-state leakage loss and it can be optimized with the choice of Schottky barrier height.

$$P_D = J_F V_F D + J_R V_R (1-D) \qquad (7)$$

where D is the duty cycle and no switching loss is assumed. Fig. 7.13 shows the calculated power dissipation of 1000 V Schottky rectifiers on 6H-SiC and 4H-SiC with three different barrier heights. $J_F = 100$

A/cm^2, V_R = 500 V and D = 0.5 (or 50%) are assumed. It can be seen that the power dissipation can be lowered by decreasing the barrier height employed but is accompanied with a lower maximum operating temperature from increased leakage current. For the silicon Schottky with the same voltage rating, the power dissipation has been estimated to be at least an order of magnitude higher. A silicon junction rectifier with the same rating, the power dissipation increases rapidly with increasing switching frequency due to minority carrier storage. Consequently, the advantages of high-voltage SiC Schottky rectifiers are clearly established.

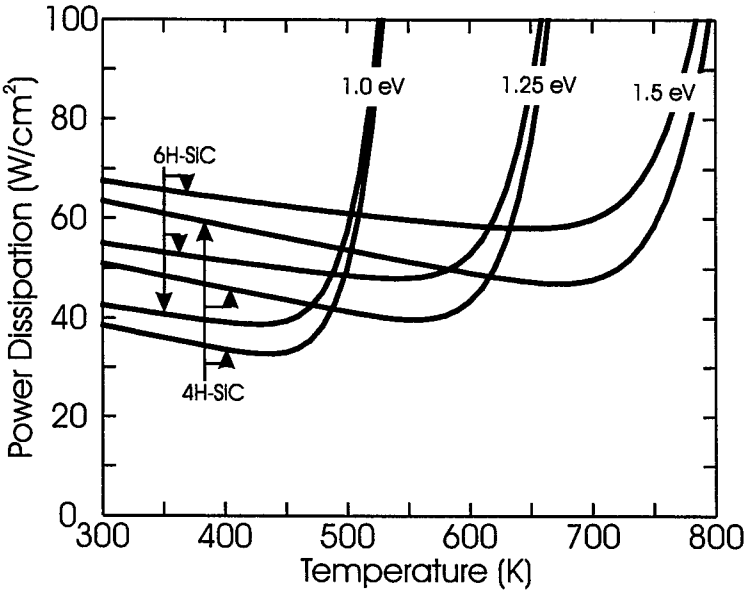


Fig. 7.13. Estimated power dissipation as a function of temperature for 1000V Schottky rectifiers on 6H-SiC and 4H-SiC

PIN JUNCTION RECTIFIERS

PiN power junction rectifiers are very useful because of their special asymmetric current-voltage characteristics and their effectiveness in supporting high reverse voltage. To estimate the drift layer thickness and doping for a specific reverse voltage, we can again use Fig. 7.4.

The forward voltage drop of a pin junction rectifier consists of the drop across the middle region (V_m) and the drops across the two end junctions according to

$$V_F = V_{P+} + V_m + V_{N+} \qquad (8)$$

where V_{P+} and V_{N+} are the voltage drops across the anode and cathode junctions respectively and their sum can be expressed (Ghandhi 1998) as

$$V_{P+} + V_{N+} = (kT/q) \ln (n(-d)n(+d) / n_i^2) \qquad (9)$$

where n(-d) and n(+d) are the electron concentrations at the anode and cathode junctions respectively. The mid-region drop, V_m, depends strongly on carrier recombination lifetimes and can be expressed as transcendental functions of d/L_a (see Ghandhi 1998, Eq. (3.81)). Approximately,

$$V_m = (3\,k\,T/\,q)\ (d/L_a)^2 \quad \text{for } d < L_a \qquad (10a)$$

$$V_m = (3\,\pi\,k\,T\,/8\,q) \exp (d\,/\,L_a) \quad \text{for } d \geq L_a \qquad (10b)$$

where 2d is the middle drift layer width and L_a is the ambipolar diffusion length. Fig. 7.14 shows the dependence of the normalized middle region voltage drop ($V_m/(kT/q)$) on the normalized middle region width (d/L_a). Combining Eqs.(9) and (10), we can get (Ghandhi 1998)

$$J = (2\, q\, D_a\, n_i / d)\, F(d/L_a)\, \exp(q\, V / 2\, k\, T) \qquad (11)$$

where $F(d/L_a)$ is a function of d/L_a and V_m but not a function of the current density (see Ghandhi 1998, Eq. (3.91)) and no end recombination is assumed. We can observe that Eq. (11) has a strikingly resemble to the I-V relation of a conventional pn junction under high-level injection.

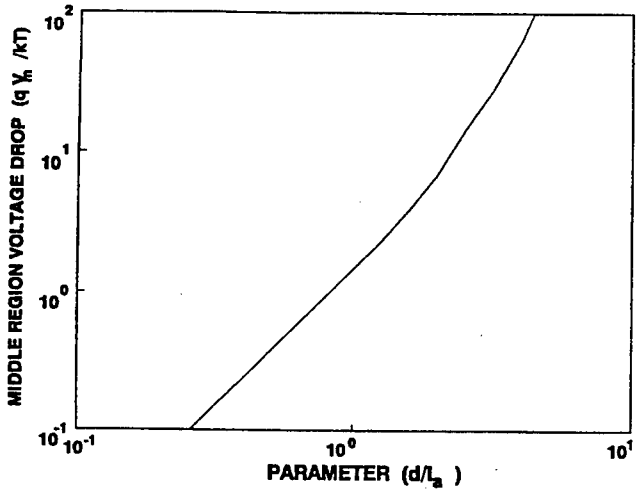


Fig. 7.14. Voltage drop in the middle drift region vs. the parameter d/L_a

The off-state leakage current of a silicon junction rectifier is dominated by the space-charge generation current, which is

$$J_{gen} = q\, n_i\, W / \tau_{eff} \propto n_i \sqrt{V} / \tau_{eff} \qquad (12)$$

where the effective generation lifetime τ_{eff} contains both bulk space-charge generation lifetime, τ_{SC}, and surface generation velocity, s_g. Also, W becomes constant once the mid-region is completely depleted.

The switching of the junction rectifier can be modeled with a charge-control model and unlike the low-voltage diodes, the switching from the forward to reverse conditions usually goes through a constant di/dt ramp (Baliga 1996). The switching times (t_{rr}, t_A, t_B) as well as the peak reverse current are dependent on the di/dt ramp rate as shown in Figs. 7.15 and 7.16, respectively (Ramungul & Chow unpublished). Besides the circuit-imposed di/dt, the reverse recovery, the reverse recovery time is also dependent on lifetime. The tradeoffs between the on-state voltage and switching performance are illustrated in Figs. 7.17 through 7.19. Fig. 7.17 shows the estimated forward voltage at $100A/cm^2$ as a function of reverse voltage for Si, 6H- and 4H-SiC with $\tau_{n0} = 10\, \tau_{p0} = 100$ ns. Even with such a low lifetime value, 4H-SiC junction rectifiers have low forward drops up to 6000V. Due to the reduced drift region width, a less demanding lifetime is needed to achieve conductivity modulation, as illustrated in Fig. 7.19. Fig. 7.19 compares the forward drop vs. ambipolar lifetime tradeoff curves for 1000 and 5000V Si and 4H-SiC. Recent experimental data have been included in Figs. 7.17 and 7.19 to assess the degree of optimization of these devices. Usually, the junction rectifiers are designed to have a mesa-isolation for epi-grown anode and planar structure for ion-implanted anode, as illustrated in Fig. 7.20.

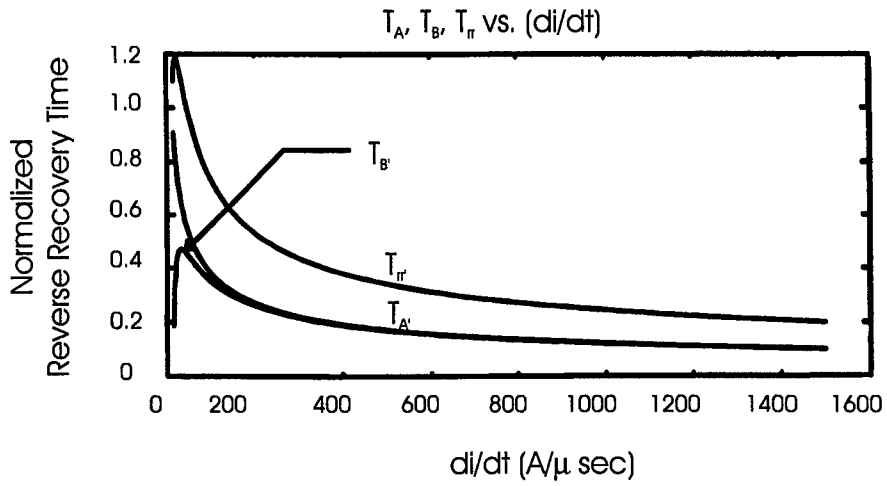


Fig. 7.15. Switching times as a function of di/dt of a pin junction rectifier

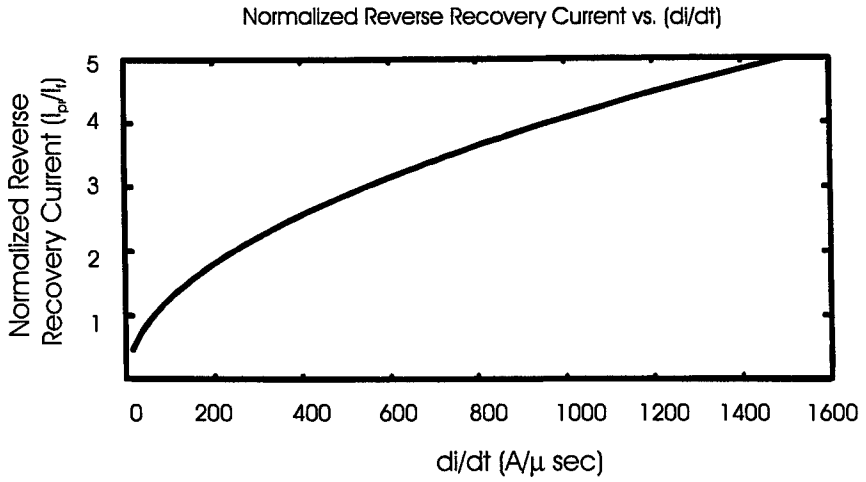


Fig. 7.16. Peak reverse current vs. di/dt of a pin junction rectifier

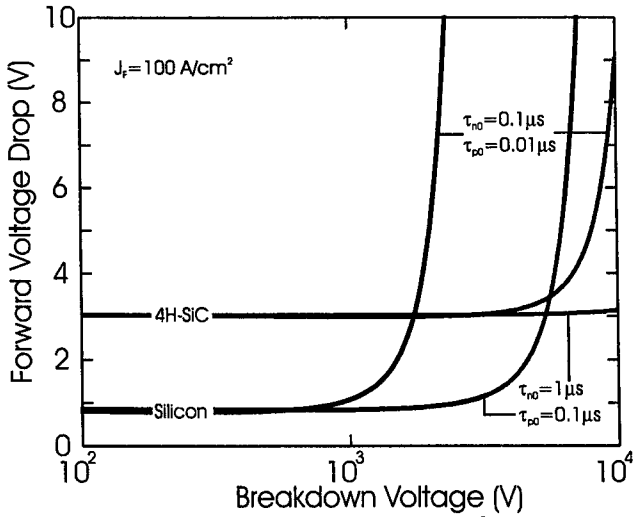


Fig. 7.17. Calculated forward voltage drop (V_F) at 100A/cm² vs. breakdown voltage for pin junction rectifiers on Si and 4H-SiC to illustrate the effect of minority carrier lifetime

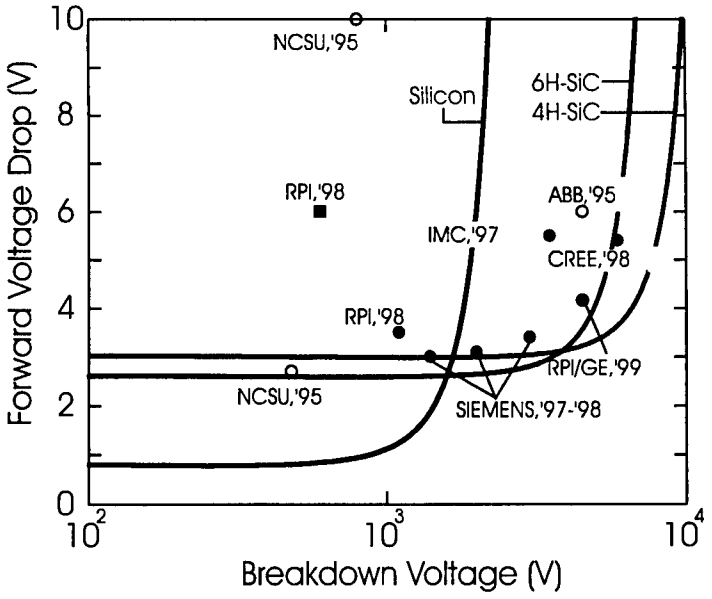


Fig. 7.18. Forward voltage drop vs. breakdown voltage for various pin junction rectifiers on 4H-SiC

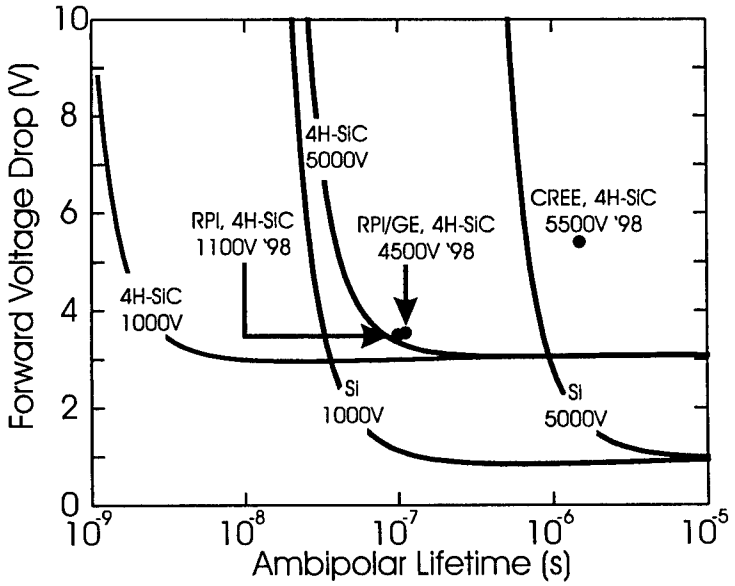


Fig. 7.19. Forward voltage drop at 100A/cm^2 vs. lifetime tradeoff curves estimated for 1000 and 5000V power junction rectifiers on silicon and 4H-SiC

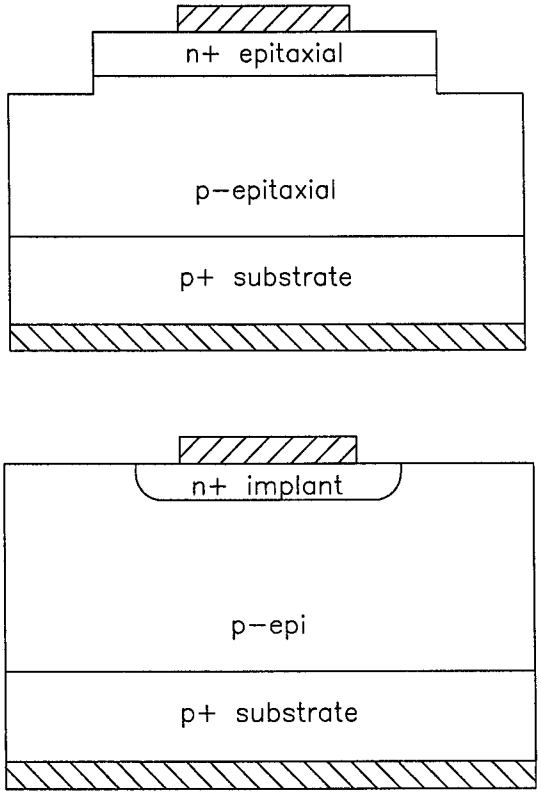


Fig. 7.20. Schematic cross-sections of pin junction rectifiers with (a) mesa-isolated, epitaxially grown anode and (b) planar, ion-implanted anode

To model the actual forward I-V characteristics of SiC pn junction rectifiers (Neudeck, et al. 1993; Shenoy & Baliga 1995; Kordina, et al. 1995; Alok & Baliga 1996; Rottner, et al. 1997; Peters, et al. 1997; Takemura, et al. 1997; Ramungul, et al. 1998; Mitlehner, et al. 1998; Patel, et al. 1998; Rottner, et al. 1998; Khemka, et al. 1999; Li, et al. 1999), particularly those fabricated with planar implanted anode or cathode junctions, it has been found that the theory established for silicon presented above is often inadequate. Modifications to the silicon equations are needed to account for the new phenomena observed.

Typical forward current conduction according to the widely accepted Sah-Noyce-Shockley (SNS) model consists of diffusion current and recombination current components (Ghandhi 1998; Baliga 1996; Sze 1981). Diffusion current (J_d) originates due to the recombination of electrons and holes in the quasi-neutral regions outside the space-charge region, whereas the recombination current component (J_{sc}) is due to recombination via single-level, uniformly distributed centers located at or near the intrinsic level. The current-voltage characteristics according to the SNS model can be written as:

$$J_F = J_{SC} + J_d = J_{S1} \exp(qV/2kT) + J_{S2} \exp(qV/kT) \qquad (13)$$

where J_{s1}, J_{s2} are the saturation current densities for recombination and diffusion current components, respectively. The activation energy, obtained by an Arrehenius plot of J_{s1}, is approximately equal to the half of the energy bandgap of the semiconductor. However, the above analysis cannot be directly applied to SiC junctions where experimental results have shown the $J_F \sim J_0 \exp(qV/nkT)$ and n, the ideality factor, lies between 1 and 2. The origin of the discrepancy is due to the existence of multiple number of deep and shallow impurity levels in the bandgap of SiC which act as effective recombination sites. A multiple level recombination model was formulated and proposed for wide bandgap compound semiconductors (Evstropov, et al. 1983; Evstropov, et al. 1984; Anikin, et al. 1989). We have applied this multiple level model to explain the forward characteristics of 4H-SiC power junction rectifiers (Patel, et al. 1998; Li, et al. 1999).

The multiple level model considers the current in the $1 < n < 2$ region also as a space-charge recombination current, but through two groups of arbitrarily called shallow and deep levels as illustrated in Fig. 7.21(a). In deep levels group, there are d identical deep sites located at an average energy level E1 and in the shallow levels group there are s identical shallow sites at an average energy E2. The forward characteristics of the power rectifiers can now be separated in four different exponential regimes as shown in Fig. 7.21(b). Regions 1 and 2 are similar to that predicted by the SNS theory but regions 3 and 4 are modified from the standard theory to include the effect of multiple recombination sites. We shall concentrate only on region 2 and 3 as they have been verified experimentally. Fig. 7.22 shows the forward characteristics of an experimental 4H-SiC phosphorus-implanted n+pp+ rectifier. Regions 2 and 3 are clearly demarcated whereas region 4 is hard to separate due to the series resistance drop. According to the multiple-level model the first term in the SNS current (Eq.(10)) is expanded to include the contribution from multiple recombination sites and can be rewritten as:

$$J_{SC} = J_{01} \exp(qV/2kT) + J_{02} \exp(qV/nkT) \qquad (14)$$

where ideality factor n is discrete and has been related to the number of recombination sites by (Li, et al. 1999):

$$n = (s+2d)/(s+d) \qquad (15)$$

For the single recombination level case ($s = 0$, $d = 1$), we obtain $n = 2$ and the multiple level model reduces to the conventional SNS model. According to above, n is temperature independent. The thermal activation energies E_{A1} and E_{A2} associated with the two saturation current densities, J_{01} and J_{02}, are predicted by the SNS and multi-level models to be $E_g/2$ and E_g/n, respectively. We have extracted an ideality factor of 1.28 (vs. 6/5 from the theory with 4 shallow and 1 deep levels) and activation energies of 1.65 and 2.71eV (vs. 1.63 and 2.72eV from theory) for phosphorus-implanted n+pp+ diodes.

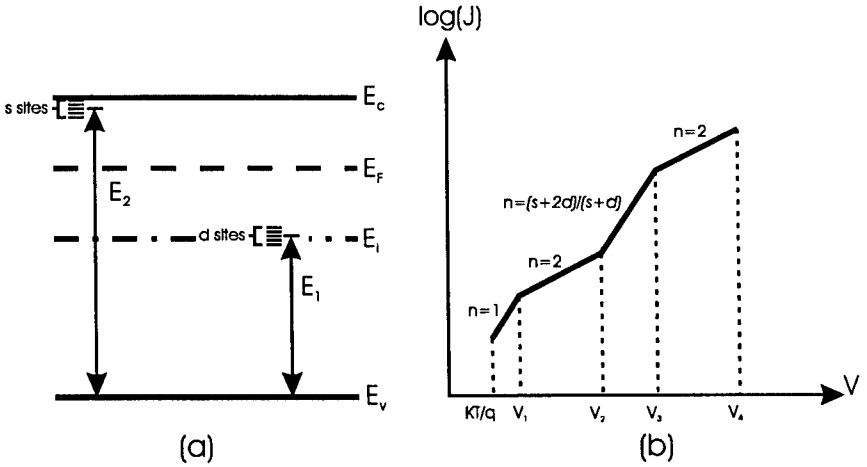


Fig. 7.21. (a) Energy levels of the shallow levels and deep recombination centers for the multiple-level model, (b) the schematic forward characteristics of the recombination current due to multiple-level centers in the space charge region

Besides the generalized SNS model, we sometimes also encounter situations in which a CCNR in the forward I-V characteristics is observed in both 6H- and 4H-SiC junction rectifiers (Ramungul & chow 1999). This forward CCNR characteristic will happen when the carrier diffusion lengths are shorter than the drift region width (Ghandhi 1998). The measured forward log J - V characteristics of epitaxial and implanted n+pp+ 6H-SiC rectifiers are shown in Fig. 7.23. To explain these behaviors, we need to use a space-charge-limited (SCL) current transport model (Ghandhi 1998).

The SCL model considers the injection of carriers into a space-charge region, which can be an insulator, a lightly doped or a depleted region in a semiconductor. The origin of the SCL current is a strong unbalanced between electron and hole lifetimes. When the recombination centers inside the space-charge region are filled, electrons injected from the cathode will have infinite lifetime and move toward the the edge of space-charge region under the influence of electric field. Since all recombination centers are available for hole capture, the lifetime for holes is short. Thus, only electrons are able to traverse across the space-charge region under the influence of the applied electric field. The injection current caused by single carrier in transit sets up a retarding field. Depending on the value of the injected current, the total electric field at the cathode can be zero or even negative. This, in turn, limits further carrier injection into the space-charge region. Since there is only one type of carrier involved in the current transport, this process is called single injection.

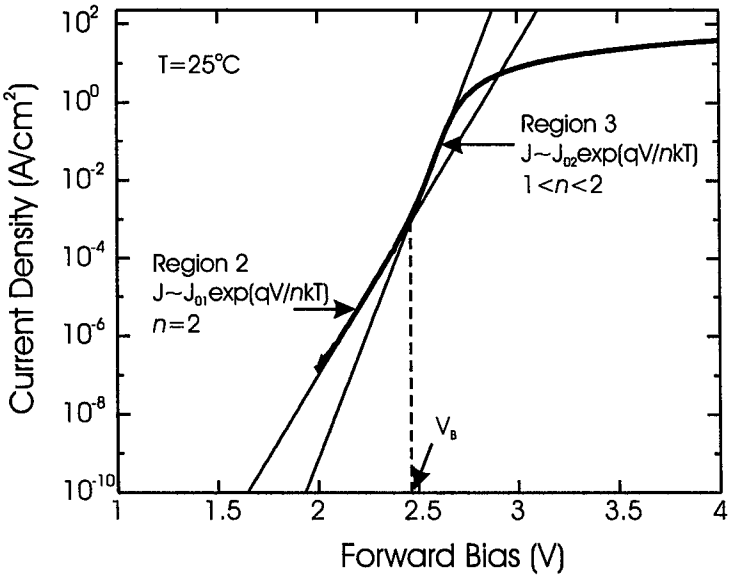


Fig. 7.22. Forward log(J) - V characteristics of phosphorus implanted, 4H-SiC n+ip+ rectifier at room temperature

In the case of wide bandgap material with a background doping N_B, the current is initially conducted by the thermally generated carrier (n_0) and the J-V relationship in this range is ohmic until the injected carrier density exceeds n_0 where the SCL current becomes dominant and the J-V relationship changes to $J \propto V^2$. In addition, if the semiconductor has localized shallow traps that are partially filled, the J-V relationship starts with an ohmic region followed by a $J \propto V^2$ region up to a cross-over voltage, V_{TFL} --- the Trap-Filled-Limited voltage, where all traps are filled. The J-V curve, then, abruptly jumps to another $J \propto V^2$ region. Moreover, for semiconductors with localized deep traps, the log(J)-log(V) curve starts with an ohmic region, followed by a sharp transition to $J \propto V^2$ when all traps become filled. Finally, $J \propto V^n$, where $n > 2$ for traps distributed in energy band (Lampert & Mark 1970; Ozarow & Hysell 1962; Patrick 1957).

As the applied voltage increases, the electric field across the space-charge region eventually becomes high enough to allow holes to transit across, where they proceed to reduce the electron space charge via recombination and causes the retarding field that blocks the flow of electron to collapse. Since both electrons and holes are involved in this process, it is called double injection. The J-V relationship for this process consists of a distinct current-controlled negative resistance (CCNR) characteristic (Ghandhi 1998). The hole transit time increases with increasing bias voltage from zero to V_T where the hole lifetime equals transit time. After the double injection is initated, the hole lifetime (τ_p) continutes to increase, creating more empty recombination sites, and increases electron capture probability, resulting in an electron lifetime (τ_n) decrease. The collapse of the electron injection barrier allows more electrons injection while the increasing in τ_p permits more holes to transit the bar. This regenerative process causes the resistivity to drop drastically. The process persistes until a new balance where $\tau_p = \tau_{pn}$ is established. Beyond that point, the injection rate

exceeds the recombination rate, making it possible for space charge to build up again. The J-V relationship in this two-carrier space-charge limited region can be characterized by a $J \propto V^3$ law (Ghandhi 19981].

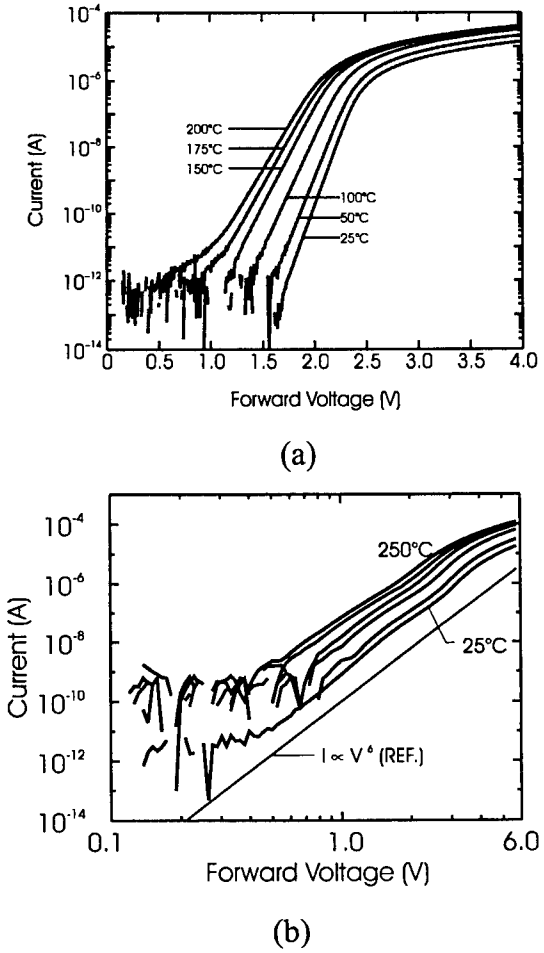


Fig. 7.23. Measured log J vs. V characteristics of epitaxial and implanted n+pp+ 6H-SiC rectifier

The triggering or threshold voltage, at which the electron transit time is equal to the electron lifetime under low level injection, can be estimated as (Ghandhi 1998)

$$V_T \sim L^2 / (\mu_n \tau_{n,low}) \qquad (16)$$

This simple model has been applied to both nitrogen- and boron-implanted 6H-SiC junction diodes (Ramungul & Chow 1999), as shown in Fig. 7.24. The deep levels responsible for such CCNR characteristics can be either due to epitaxial material quality or implantation-induced defects that have not been completely annealed out. Deep levels from nitrogen implantation is also responsible for other anamolous behaviors, such as a new charge trapping phenomenon (Ramungul & Chow 1997).

The reverse leakage current has been found to be orders of magnitude higher than that predicted by standard silicon theory extensions. Obviously, material defects, such as screw dislocations, play a role in determining the reverse current (Neudeck, et al. 1999). With the improvement in material quality, fairly low reverse current densities ($< 10^{-5}$ cm^2) have been observed, at least for small area devices (Takemura, et al. 1997; Ramungul, et al. 1998; Mitlehner, et al. 1998; Patel, et al. 1998; Rottner, et al. 1998; Khemka, et al. 1999). Fig. 7.25 shows the reverse log J vs. V of a 4H-SiC, 1100V, Al/C/B-implanted pin junction rectifier

(Khemka, et al. 1999). At high reverse bias, some of the SiC junction rectifiers show an increase in reverse current (Patel, et al. 1998) that resembles a band-to-band tunneling characteristic, which has been observed in Si on insulator (Arnold, et al. 1996). In another case, a space-charge-limited current flow mechanism due to deep traps is also used to explain the dependence of the reverse current on reverse bias ($J_R \sim V_R^n$, where $2 < n < 5$) (Anikin, et al. 1989).

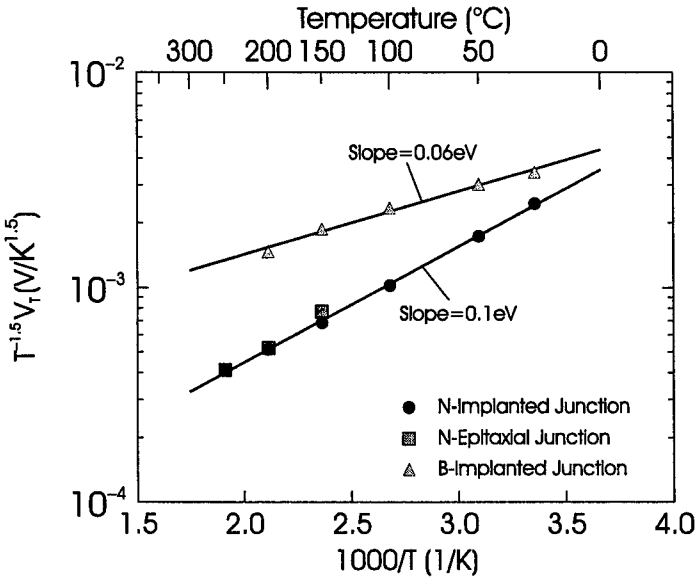


Fig. 7.24. Thermal activation energy plots of the CCNR triggering voltage in both nitrogen- and boron-implanted junction diode

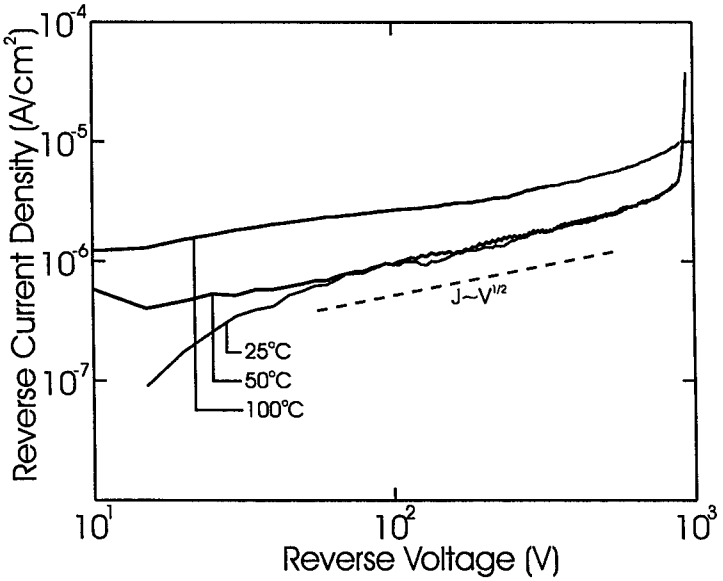


Fig. 7.25. Reverse log J-V characteristic of a 1100V Al/C/B-implanted 4H-SiC pin junction rectifier

The reverse recovery current waveforms of both epitaxial and implanted junction rectifiers have an interesting temperature dependence that has not been seen in Si devices (Peters, et al. 1997; Mitlehner, et al. 1998). In Fig. 7.26, typical reverse recovery current waveforms of a 1100V, p^+n implanted diode are measured up to 200°C. Interestingly, the reverse recovery charge (Q_{rr}) and recovery time (t_{rr}) remains constant with increasing temperature, which may indicate the deepness of the energy level of the

recombination centers. Also, their values (18nC and 0.1μsec, respectively) are significantly lower than those for an equivalent silicon rectifier of the same voltage rating.

HYBRID RECTIFIERS

In order to achieve good reverse blocking characteristics while maintaining a Schottky forward conduction and fast reverse recovery characteristics, several modern rectifiers, such as Junction Barrier Schottky (JBS) (Wilamowski 1983; Baliga 1984), Dual Metal Trench (DMT) Schottky (Schoen, et al. 1998) and Trench MOS Barrier Schottky (TMBS) (Mehrotra & Baliga 1995) rectifiers, have been explored. The physical principle used to reduce the leakage current is the same - to completely deplete the Schottky mesa regions under the Schottky junction so as to suppress the electric field from rising at the Schottky junction when the bias at the substrate cathode is increased. In the JBS rectifier, reverse biased pn junctions are used, while in the DMT and TMBS rectifiers, Schottky junctions with a higher barrier height and MOS capacitors are used respectively.

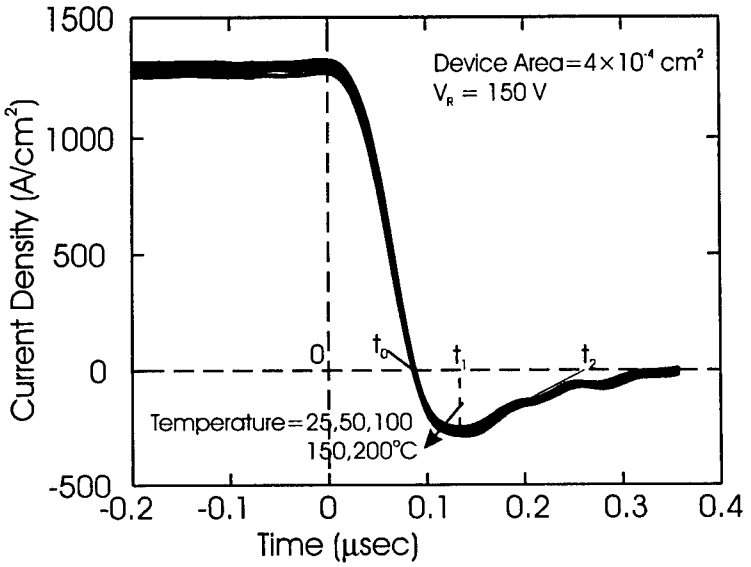


Fig. 7.26. Reverse recovery current waveforms measured on 1100V, planar, Al/C/B-implanted 4H-SiC junction rectifier at different temperatures

While both JBS and MPS rectifiers have similar device structures as both have deep implanted interdigitated p+ grids adjacent to Schottky junctions, the main junctions in the MPS rectifier are the pin diode regions (Baliga & Chang 1987). The p+ anode injects holes into the drift region, resulting in a drastic reduction in the series resistance via conductivity modulation. Also, the auxiliary Schottky regions are placed next to the pn junction so as to reduce reverse peak current and to speed up reverse recovery. In addition, the Schottky regions are designed not to degrade the reverse leakage current at reverse bias. Furthermore, while the injection level in MPS is not as high as PiN rectifiers, the Schottky region also participate in the forward conduction by injection majority carriers into the conductivity modulated drift region.

An analytical model has been developed for the JBS rectifier (Baliga 1985) to describe the forward conduction and reverse blocking characteristics. The key design parameters are the mesa width, junction depth and the junction diffusion window width.

Both MPS and JBS rectifiers have been experimentally demonstrated in SiC (Dahlquist, et al. 1997; Held, et al. 1997). Although these reported devices achieved breakdown voltages as high as 1000V, the unit cell size design is not optimal and more work is needed to realize the full advantages of these concepts.

The DMT rectifier, reported recently (Schoen, et al. 1998), utilizes a Schottky metal with a higher barrier height than the main Schottky junction to achieve field shielding. The reported device had Ti deposited to

achieve a low barrier height on top of the mesa followed by conformal deposition of Ni over the entire device to achieve a higher barrier height at the bottom of trenches. The forward drop and reverse leakage current reported for this device were between Ti and Ni Schottky diodes. In particular, a forward voltage drop close to that of Ti Schottky junctions but with leakage current two orders of magnitude lower than Ti SBD but about a factor of two higher than the Ni devices. Although the leakage current measurements were shown up to a reverse voltage of 300V, no information on the true breakdown voltage of the device was given.

Embedding a UMOS trench like grid instead of a PN junction grid as in JBS/MPS rectifiers yields a structure known as the TMBS rectifier. The original Si device reported in (Mehrotra & Baliga 1995) was shown to be capable of achieving higher than parallel plane breakdown voltage with little compromise in the forward conduction capability. We have fabricated a polysilicon planarized Ni-TMBS in 4H-SiC, the forward and reverse characteristics of which are compared to that of simultaneously fabricated Ni SBD and PiN rectifiers are illustrated in Fig. 7.27 (Khemka, et al. 1999). A significant improvement over the SBD leakage current is observed with little sacrifice in the forward voltage drop. The reverse leakage current and forward voltage drop, as expected, was observed to scale with the percentage Schottky area. An increase in mesa width would reduce the amount of field shielding under the Schottky contact at the same time it will increase the percentage Schottky area. Both the effects combined would result in an increase in the leakage current and reduction in the forward voltage drop. Depth of the trench would also alter the device performance significantly as it will alter the aspect ratio directly thereby affecting the field shielding under the Schottky mesa. This indicates that an optimized device design would involve a careful selection of mesa width and trench depth.

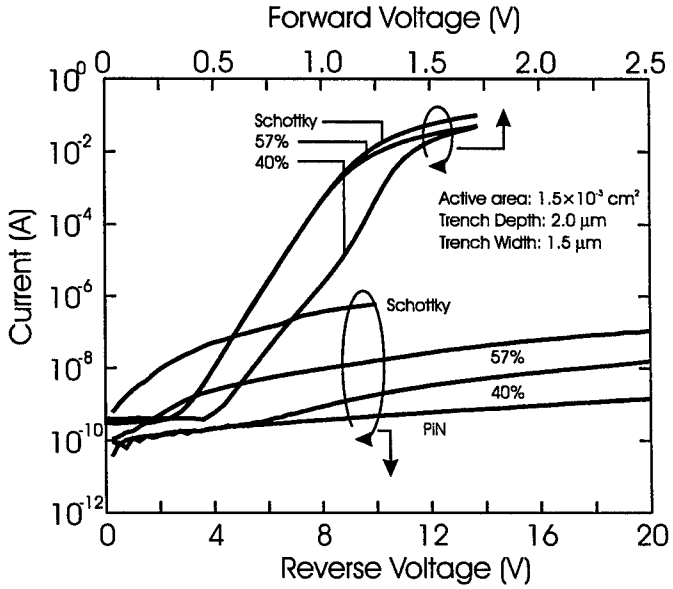


Fig. 7.27. Forward and reverse characteristics of the Trench MOS Barrier Schottky rectifier in 4H-Si

POWER TRANSISTORS

In general, the power transistors can be classified as the unipolar and bipolar transistor families. Within each family, they can be further divided into current- and voltage-controlled devices. The MOSFET and JFET are unipolar transistors that usually use voltage for control. On the other hand, the bipolar junction transistor and the IGBT are bipolar transistors, with the former using current for control and the latter using voltage control. A voltage-controlled transistor is often preferred for ease of integrating IC-based gate driving circuitry. Table VIII summarizes the recent experimental results on unipolar and bipolar power FET structures in 6H- and 4H-SiC. Clearly, the MOSFET is the FET structure that has been most widely explored.

UNIPOLAR TRANSISTORS

MOSFET

Since the 1970's, the silicon power MOSFET has become a dominant power switching transistor in the low voltage, low power, high-frequency applications. Generally, the vertical power MOSFET structures can be grouped into employed Double-diffused MOS (DMOS) and UMOS FET's (see Fig. 7.28). In the planar DMOSFET, the channel is lateral along the MOS surface whereas in the UMOS structures, the channel is vertical. In both cases, the channel length is determined by the difference in the diffusion depths of the p-body and n+ source. The UMOSFET has a higher channel density (channel width per unit active area) than the DMOSFET.

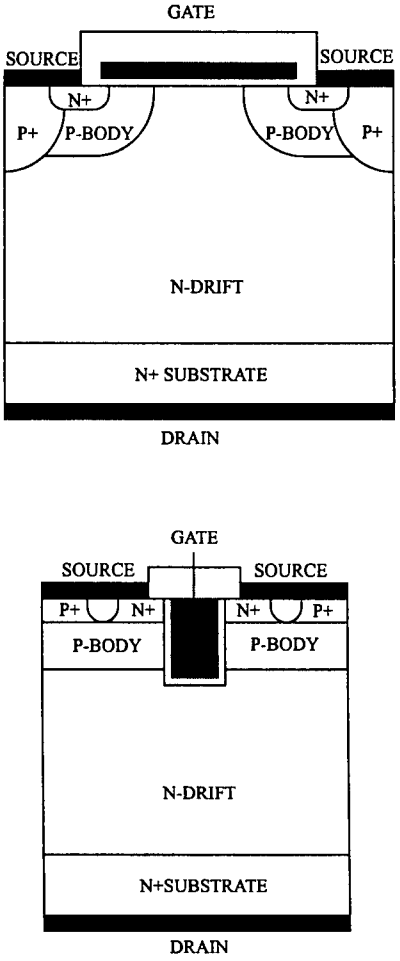


Fig. 7.28. Schematic cross sections of vertical DMOS and UMOS FET's

The breakdown voltage of a power MOSFET is determined by the doping and thickness of the drift region, like a pin junction diode. In the DMOS, the surface MOS unit cell can degrade the BV and must be spaced optimally so that the depletion layers of adjacent p body regions merge at relative low drain voltage, thus isolating the surface channel from the high drain potential. In the UMOSFET, the trenches must be place close to each other so as to prevent the electric field from converging at the trench corners.

In the on-state, the power MOSFET is basically a gate-controlled resistor. The various resistance components of a vertical DMOSFET are shown in Fig. 7.29. The JFET component is negligible in the UMOSFET. Also, the dominant resistance components are usually the channel resistance (R_{ch}), accumulation

layer resistance (R_A), JFET resistance (R_{JFET}) and the drift region resistance (R_D). In particular, the specific resistances of these are (Baliga 1996)

$$R_{ch,sp} = L_{ch} (L_G + 2m) / (2 \mu_n C_{ox} (V_{GS} - V_T)) \quad (17)$$

$$R_{A,sp} = K (L_G - 2x_P) (L_G + 2m) / [2 \mu_n C_{ox} (V_{GS} - V_T)] \quad (18)$$

$$R_{JFET,sp} = \rho_D (L_G + 2m) (x_p + W_0) / (L_G - 2x_P - 2W_0) \quad (19)$$

$$R_{D,sp} = (\rho_D (L_G + 2m) /2) \ln [(L_G + 2m)/(L_G - 2x_P - 2W_0)] + \rho_D (t - m - x_P - W_0) \quad (20)$$

where L_G is the poly-Si gate electrode length between adjacent cells, 2m is the p-body diffusion window size, L_{ch} is the channel length, K is the spreading factor ($K \approx 0.6$ for DMOS), x_p is the p-body junction depth, W_0 is the zero-bias depletion width of the p body/n drift layer junction, ρ_D is the drift region resistivity, and t is the thickness of the drift region.

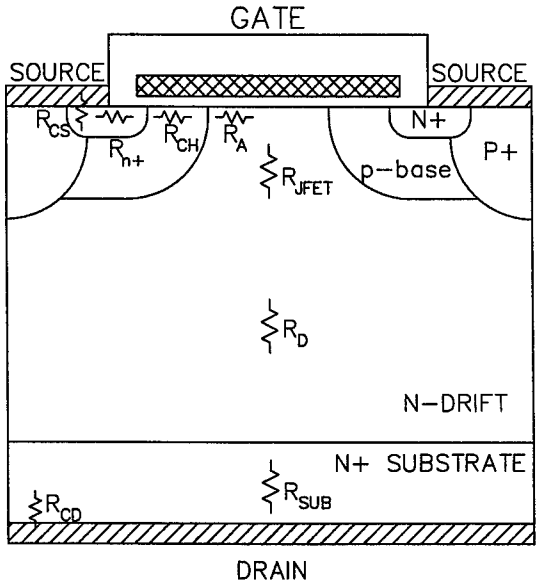


Fig. 7.29. The resistance components of a vertical DMOS FET in the on-state

Due to the absence of minority carriers, the switching speed of MOSFET's (indeed, all FET's) is very high and determined by the parasitic capacitances (gate capacitances) and inductances (package wire inductances). Typically, switching times of 1 ns are common even though the ultimate limit (dielectric relaxation time) is actually 1ps.

In SiC, several high-voltage MOSFET structures have been reported over the last five years. Similar to silicon, with the availability of acceptable MOS interface properties and electron mobility significant higher than hole mobility, n-channel MOSFET's are mostly considered. UMOS in SiC is popular (Palmour, et al. 1994; Palmour, et al. 1995; Casady, et al. 1997; Agarwal, et al. 1998; Sugawara & Asano 1998) since the p-body layer is formed by epitaxy, not by diffusion, which is difficult due to slow diffusion of most dopants. Nevertheless, DMOSFET's in 6H- and 4H-SiC using ion implantation have been demonstrated by several groups (Casady, et al. 1997; Shenoy, et al. 1997).

These trenched UMOS structures present two undesirable features that must be suppressed. First, the dry-etched sidewalls have very low inversion mobility when compared to planar inversion mobility. This degradation has been found to be very significant for both 6H- and 4H-SiC polytypes. Experimentally, the inversion electron mobilities are typically only 1% or less than bulk mobility. Second, the sharp trench corners lead to severe breakdown degradation unless field shielding is employed. The dependence of the breakdown voltage on trench unit cell spacing is shown in Fig. 7.30 (Ramungul, et al. 1995). It can be seen

from these simulations that a maximum esa width of 2 um is to be designed. Utilizing such design rules, experimental UMOSFET's with a BV over 1000V have been realized (Casady, et al. 1997). In addition, the MOS capacitors at the bottom of the trenches also experience a more severe field stressing than in the silicon case. The reason for the high field problem in SiC MOS is the higher avalanche field in SiC vs. Si (2-3 vs. 0.2 MV/cm) and a lower permittivity of SiC vs. Si (10 vs. 12), resulting in an oxide field of ~7 MV/cm or ~70% of the oxide breakdown field. Such a high field could reduce device yield and lead to potential device reliability problems. By comparison, the oxide field in Si is less than 1 MV/cm when the silicon reaches avalanche condition. Replacing SiO_2 with a dielectric of a higher permittivity is not as an attractive as it may first appear. Besides the need to have MOS interface properties close to those obtained for oxide/SiC, while replacing the oxide with a dielectric with higher permittivity leads to a low field, the decreasing breakdown field with increasing permittivity trend (see Fig. 31) ($\xi \propto \varepsilon^{-2}$) (Chow & Ramungul) negates much of the gain with this technique. Novel device structures can also be used to circumvent this issue (Agarwal, et. Al. 1997).

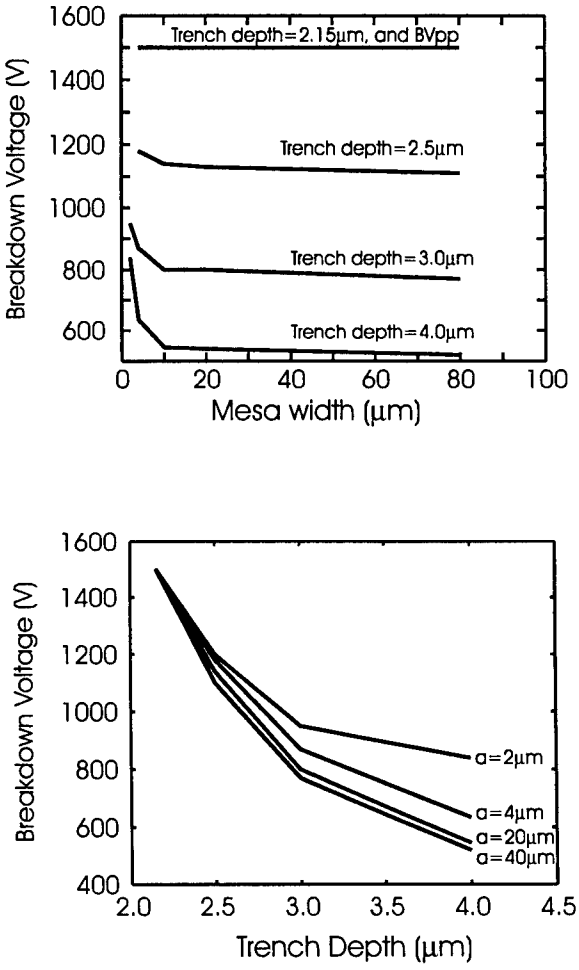


Fig. 7.30. Breakdown voltage as a function of UMOS (a) mesa width and (b) trench depth

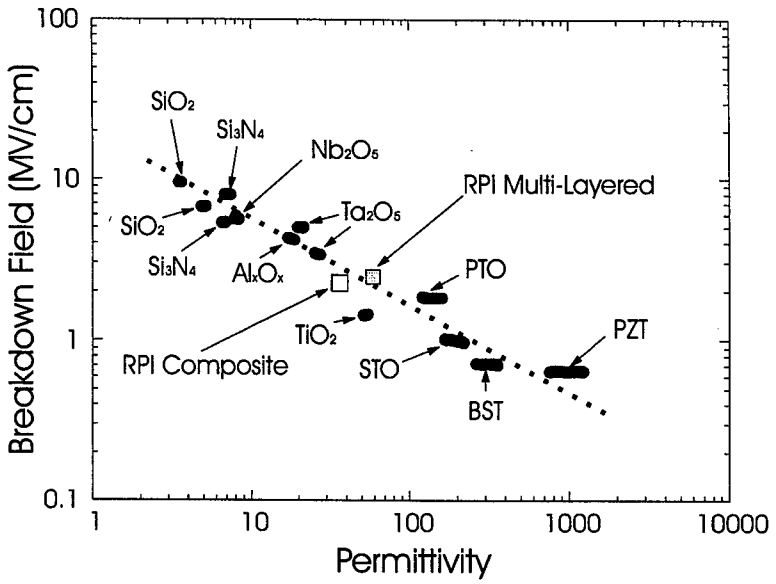


Fig. 7.31. Dielectric breakdown field as function of permittivity

Besides the field problem in the oxide, the band offsets between the 6H-SiC or 4H-SiC and SiO_2 in both the conduction and valence band edges are smaller than those between silicon and oxide (Agarwal, et. al. 1997). Consequently, it is easier for electrons and holes to surmount the barrier and inject into the oxide when they are confined to the SiC/SiO_2 interface, particularly at elevated temperatures. Fowler-Nordhelm tunneling has been measured for SiC MOS capacitors and found to be quite severe at 300°C (Agarwal, et. al. 1997; Bano, et. al. 1997).

To circumvent the low electron inversion layer mobility, normally-off accumulation type MOSFET's have become popular and have been demonstrated (Hara 1998; Shenoy & Baliga 1997; Tan, et. al. 1998; Seshadri, et. al. 1998; Crofton, et. al. 1997; Peters, et. al. 1999). However, these devices have higher leakage currents, particularly at elevated temperatures and near BV. In Fig. 7.32, the specific on-resistance of the various UMOS, DMOS and accumulation-mode FET's are plotted as a function of breakdown voltage. It can be seen that many of the experimental MOSFET's have already exceeded the silicon material limit. However, as indicated in Table 7.8, the current level is still low (< 5A). Also, since the inversion layer mobility of electrons in 4H-SiC is usually very low (< 10 cm^2/V-sec) while that in 6H-SiC is acceptable (30-50 cm^2/V-sec), the best inversion-mode vertical SiC MOSFET's have been shown in 6H-SiC so far (Seshadri, et. al. 1998; Crofton, et. al. 1997). Furthermore, it has been suggested that the 15R polytype may be most suitable for SiC power MOSFET due to its high electron inversion mobility (33 cm^2/V-sec) (like 6H-SiC) but more isotropic bulk mobilties (like 4H-SiC) (Chatty, et. al. 1999).

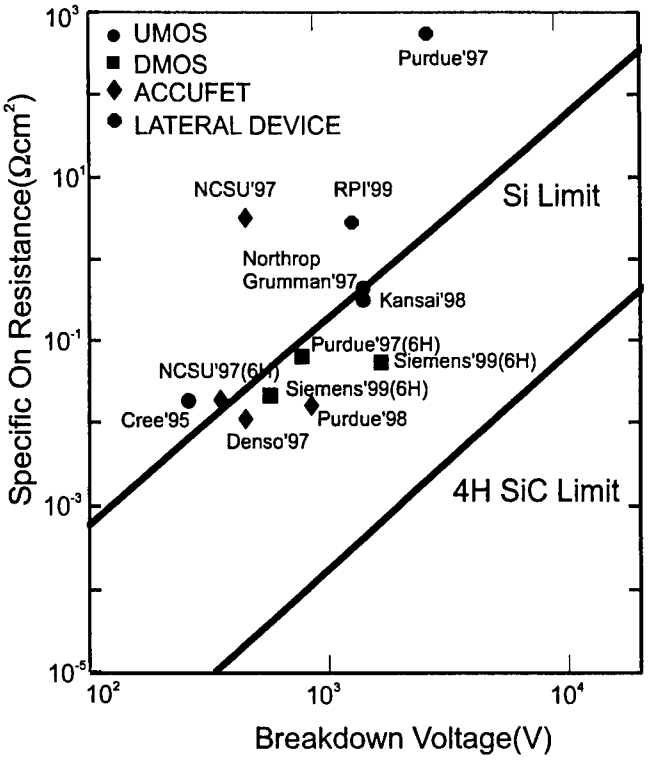


Fig. 7.32. Specific on-resistance of 4H-SiC power MOSFET's vs. breakdown voltag

JFET

Instead of using a MOS-gate to control the carrier flow in the channel of the FET, a pn junction gate can also be used. However, there are two major differences. First, while no dc current can flow from the gate to the channel through the MOS gate dielectric, significant current can flow the the gate-channel junction if the junction is sufficiently forward biased. For silicon, the forward bias needed is only 0.7V while that for 6H-SiC and 4H-SiC is over 2.5V but it decreases with increasing temperature. Due to this current flow, accumulation-mode type devices are not possible in the JFET's. It should also be noted that once the gate-channel is sufficiently turned on, minority carrier injection into the channel causes bipolar conductivity modulation, resulting in a lower on-resistance but increases the turn-off time. Second, whereas the channel can be formed with inversion layer or epitaxial or implanted regions in MOSFET's, only the latter type of channels can be used for JFET's.

The drain current with respect to the gate and drain bias can be described similar to the MOSFET (Sze 1981). Most of the JFET's reported are normally on because a normally off channel doping and thickness is difficult to design and has a limited gate voltage swing. The reason for the limited gate voltage swing in the enhancement mode is that forward biasing of the gate-channel junction above the turn-on voltage would cause minority carrier injection. In the depletion mode JFET, the pinch-off voltage, which is the gate voltage necessary to completely deplete the channel and cut off drain current, is the equivalent to the threshold voltage of the MOSFET and can be expressed as

$$V_P = q N_D a / (2 \varepsilon_S) \qquad (21)$$

where N_D is the channel doping and a is the channel width. Also, the on-resistance for this type of JFET is usually evaluated at no gate bias and the specific on-resistance is similar to that for the MOSFET where $R_{ON,sp} \sim (BV)^{2.5}$. For high-voltage power devices, the blocking gain is a key parameter and is defined as the ratio of the drain voltage to the gate voltage at a specified leakage current. It improves with increasing L/p aspect ratio, where L is the channel length and p is the gate grid pitch. It generally ranges from 5 to 10.

Other relevant parameters, such as transconductance, are defined similar to the MOSFET case. (See Chapter 4 of Baliga 1987 for more details.)

Table 7.8

A list of SiC power transistors that have been experimentally demonstrated.

DEVICE TYPE	POLYTYPE	Power Ratings	Features	Researcher
MOSFET	6H-SiC	60V, 125mA	UMOS, 38mΩ·cm^2	**Cree, 1993**
	4H-SiC	150V, 150mA	UMOS, 33mΩ·cm^2	Cree, 1993
	4H-SiC	260V, 100mA	UMOS, 18mΩ·cm^2	Cree, 1995
	4H-SiC	1100V	UMOS, 74mΩ·cm^2@100°C	Northrop Grumman, 1997
	4H-SiC	1400V	UMOS, 311mΩ·cm^2	Kansai Elec., 1998
	6H-SiC	760V, 3mA	DMOS, 125mΩ·cm^2	Purdue U., 1996
	4H-SiC	900V	DMOS, ? mΩ·cm^2	Northrop Grumman, 1997
	6H-SiC	550V, 1A	DMOS, 25mΩ·cm^2	Siemens, 1997
	6H-SiC	1800V, 0.45A	Triple-Implanted DMOS, 82mΩ·cm^2	Siemens, 1999
	6H-SiC	600V, 5A	Triple-Implanted DMOS, 22mΩ·cm^2	Siemens, 1999
	6H-SiC	1600V, 1A	Triple-Implanted DMOS, 40mΩ·cm^2	Siemens, 1999
	4H-SiC	2.6KV, 1μA	Lateral DMOS	Purdue U., 1997
	4H-SiC	1200V, 1 mA	Lateral RESURF, 4 Ω·cm^2	RPI, 1999
	6H-SiC	500V	Lateral RESURF, 40mΩ·cm^2	NRL/Northrop Grumman, 1999
	4H-SiC	450V, 100mA	Accumulation mode FET, 11mΩ·cm^2	**Denso, 1997**
	6H-SiC	350V, 100mA	Accumulation mode FET, 18mΩ·cm^2	**N. Carolina SU, 1997**
	4H-SiC	450V, 5mA	Accumulation mode FET, 3.2Ω·cm^2, 128mΩ·cm^2 @150°C	**N. Carolina SU, 1998**
	4H-SiC	850V, 25mA	Accumulation mode FET 27mΩ·cm^2	**Purdue U., 1998**
JFET	4H-SiC	550V, 6A	Cascoded with Si MOSFET, 18mΩ·cm^2	**Siemens, 1999**
	4H-SiC	950V, 1.2A	Cascoded with Si MOSFET, 40mΩ·cm^2	**Siemens, 1999**
MESFET	6H-SiC	450V, 10mA	Lateral, 83mΩ·cm^2	**N. Carolina SU, 1996**

There are many investigations of SiC JFET studies reported in literature (Zolper 1998; Kelner, et. al. 1991; Alok & Baliga 1995; Raynaud, et al. 1997; Konstantinov, et. al. 1997; Sheppard, et. al. 1998) (see Zolper 1998 for a recent review). The applications considered are high-frequency amplification, high-temperature

and high-voltage power switching as well as radiation hardened applications. In addition, there are several gate structures that have been experimentally explored. These include surface gate, buried gate and substrate gate configurations. Source and gate regions are usually ion implanted. Up to 700V BV has been demonstrated in 6H-SiC with a turn-off gate voltage of -40V (Konstantinov, et. al. 1997). Operation of up to at least 400°C has been shown with an on-off saturated drain current ratio of 10^6 (Sheppard, et. al. 1998). Very recently, high-voltage (600-1000V) 4H-SiC vertical JFET's with cascoded low-voltage (50V) Si MOSFET have resulted in a normally-off high-voltage switch with specific on-resistance in the range of 18-40mΩ-cm^2 (Peters, et. al. 1999).

MESFET

While the MESFET structures have been widely explored for microwave power amplifier applications, there relatively are relatively few reports on their power switching applications. They avoid the oxide problem in MOSFET's but, similar to the JFET's, they tend to be in the normally on mode and their off-state leakage currents are generally higher than those in the inversion mode MOSFET's. On the other hand, their depletion mode operation yields a majority-carrier mobility in the channel which is higher than the inversion layer mobility. Due to the metal gate, the MESFET has the highest intrinsic switching frequency among the power FET's.

Actually, only a high-voltage (450V), 2μm channel, lateral MESFET in 6H-SiC has been reported (Alok & Baliga 1996) so far, with an on-resistance of 83mΩ-cm^2 and a transconductance of 2mS/mm and a drain-gate separation of 15μm. The off-state leakage current near BV is very high, approaching 20% of the on-state current. Also, it has been proposed (Baliga 1996) that a Si MOSFET/SiC MESFET combination would avoid the oxide problem in the SiC MOSFET but the Si MOSFET cannot stand the high-temperature environments to which the SiC devices may be subjected.

HEMT

Unlike AlGaAs or AlGaN, heterojunctions between different SiC polytypes are very difficult to form and control. Thus, no SiC HEMT has been reported to date.

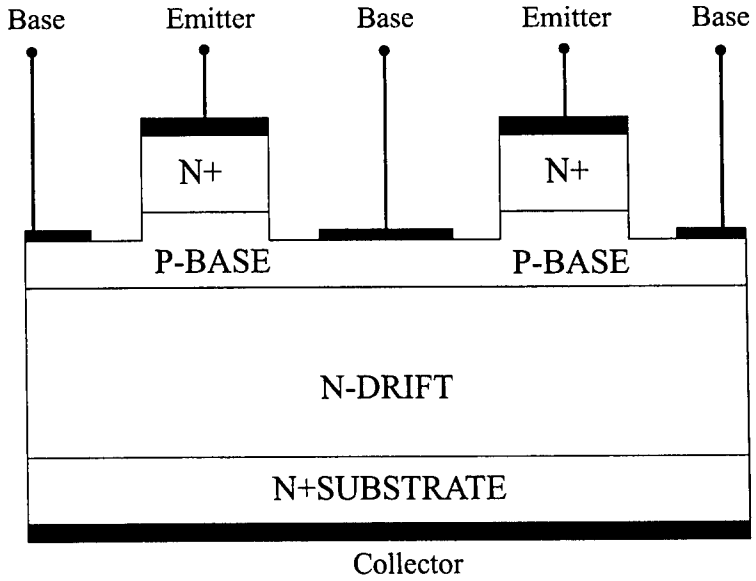


Fig. 7.33. Schematic cross-section of a SiC bipolar junction transistor

BIPOLAR TRANSISTORS

Shown in Figs. 7.33 and 7.34 are the schematic cross-sections of several three terminal power bipolar transistors and thyristors that can be implemented in SiC. Besides the BJT and GTO, the UMOS devices include the power MOSFET, IGBT and MOS-Controlled Thyristor (MCT). A lesser-known MOS-controlled bipolar transistor, called the MOS-Gated Transistor (MGT), is also included and shown in its UMOS version (Fig. 34e). The DMOS version of the MGT has been previously demonstrated in silicon (Tanaka, et. al. 1986) but has not widely used due to a less and more non-uniform conductivity modulation than the IGBT. However, the MGT deserves considerations in SiC due to the use of a n+ substrate, which can be doped heavier than the p+ substrate for the n-channel IGBT as well as a larger safe operating area (SOA).

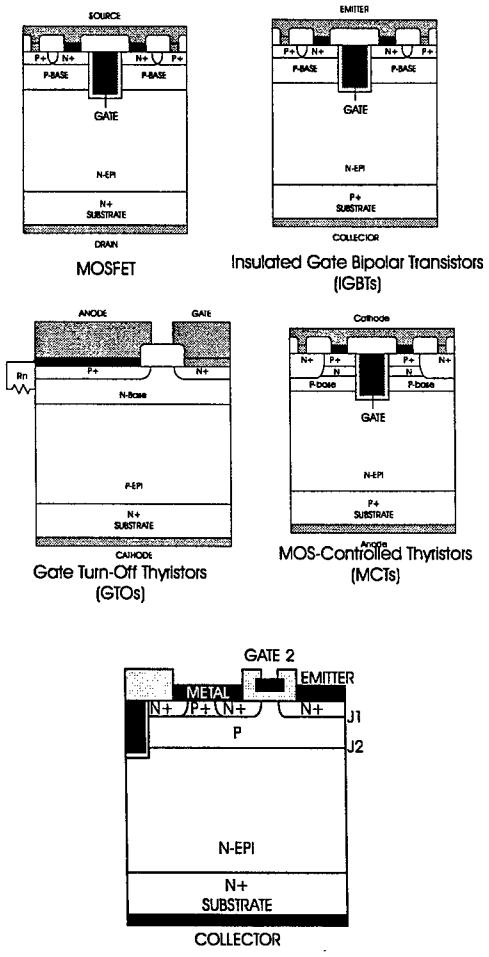


Fig. 7.34. Schematic cross-sections of several three-terminal vertical power semiconductor devices

BJT/Darlington

The Bipolar Junction Transistor (BJT) uses a base current to control the on-off conditions of the transistor. To design it to support high voltage, a lightly doped collector region is used. Also, the base thickness and doping must be sufficient from preventing punchthrough breakdown. The details of the basic operation of the power BJT can be found in (Ghandhi 1977; Baliga 1996).

The major distinguishing feature of the forward I-V characteristics of the power BJT is the quasi-saturation region, which is a direct consequence of the lightly doped and is not present in low-voltage BJT's. This region reduces the output current and slows down the switching speed. The slope (dI/dV) is proportional to the reciprocal of the collector region resistance. At high current densities, part or the entire n^- collector

region is flooded with a e-/h+ plasma and is conductivity modulated and hence the voltage drop across it decreases (Baliga 1996). Once the n- region is no longer highly resistive, the conventional saturation region commences and the base collector junction is forward biased, leading to a junction voltage cancellation and a low forward voltage drop. However, with increasing level of carrier injection, the recombination rate in the base/collector region increases, decreasing the current gain and requiring a larger base current drive. Other second order effects, such as emitter crowding, also need to be considered so as to avoid current non-uniformities and excessive local heating. Usually, an interdigitated emitter/base finger layout is adopted to maximize the emitter periphery per unit area and the emitter finger width is minimized. Another effect, known as the Kirk effect, shifts the peak electric field from the p base/n^- collector junction to the n^-/n^+ junction at high collector bias when the collector current density increases. Both of these effects tend to lower the current gain and degrade the conduction performance of the BJT. To enhance the current gain, a two-stage, Darlington configuration can be realized by cascading two BJT's with a common collector (Baliga 1996). This Darlington configuration has a current gain, β_D,

$$\beta_D \sim \beta^2 \qquad (22)$$

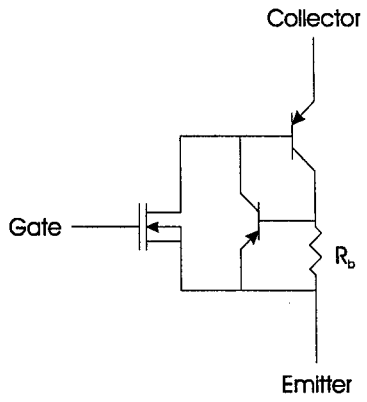
where β is the current gain each BJT stage, and the base current requried is significantly reduced.

During turn-off, there are several phases that the BJT undergoes several carrier removal stages. Also, besides the open base turn-off during which the carriers are removed with recombination, one can use the base drive circuitry to extract the excess carriers from the device via the base terminal. The turn-off process can be divided into the two phases - the initial storage phase, followed by a decay phase. In the storage phase, the collector phase remains constant while the excess carriers are removed from the modulated collector. When the carrier concentration in the collector starts to fall below the background doping level, the decay phase commences, with at first gradual and then more rapid decrease in the collector current. Both the base and collector current cease to less than 10% of the initial value when the decay phase terminates. The actual rate of voltage increase across the BJT is dependent on the nature of the load, more rapidly for an inductive load than a resistive load. Due to the 10x reduced collector drift region to support the blocking voltage, the SiC BJT has less stored charge and can have a switching frequency up to at least 200 KHz.

A few reports on SiC npn BJT's have been presented (von Munch & Hoeck 1978; Palmour, et. al. 1993; Wang, et. al. 1996). Almost all of the emitter regions are epitaxially grown and typically a current gain of 5-10 was obtained. A breakdown voltage of 200V and an on-resistance of 126mΩ-cm^2 have been reported for a 6H-SiC BJT (von Munch & Hoeck 1978).

IGBT

We have previously indicated that the most popular silicon power bipolar transistor is the IGBT, in which a MOSFET is connected to the base of a bipolar transistor in a Darlington configuration, as shown in Fig. 7.34(b) for an n-channel, UMOS device. In the on state, the n-channel IGBT can be considered as an n-channel MOSFET driving a wide-base pnp bipolar transistor. In parallel with the MOSFET is a parasitic narrow-base npn transistor, which is usually emitter-base shorted and, together with the wide-base pnp, forms a parasitic thyristor. The equivalent circuit of the IGBT is depicted in Fig. 7.35. In silicon, the n-channel MOSFET has a better transconductance than the p-channel one due to a higher electron mobility but the npn has a higher current gain than the pnp. Consequently, n- and p-channel silicon IGBT's have similar forward drops (Baliga 1996). In this regard, the SiC has similar asymmetric electron and hole mobilities and lifetimes and hence n- and p-channel IGBT's will have the similar forward drops. On the hand, in silicon, the pnp is more rugged and less susceptible to second breakdown than the npn due to a larger electron ionization coefficient. As shown in Fig. 7.1, both 6H-SiC and 4H-SiC have a larger hole ionization coefficient and npn is more rugged than npn in both SiC polytypes. Hence, the n-channel IGBT has a larger safe-operating area than and is preferred over the p-channel one.



IGBT Equivalent Circuit

Fig. 7.35. Equivalent circuit diagram of the IGBT

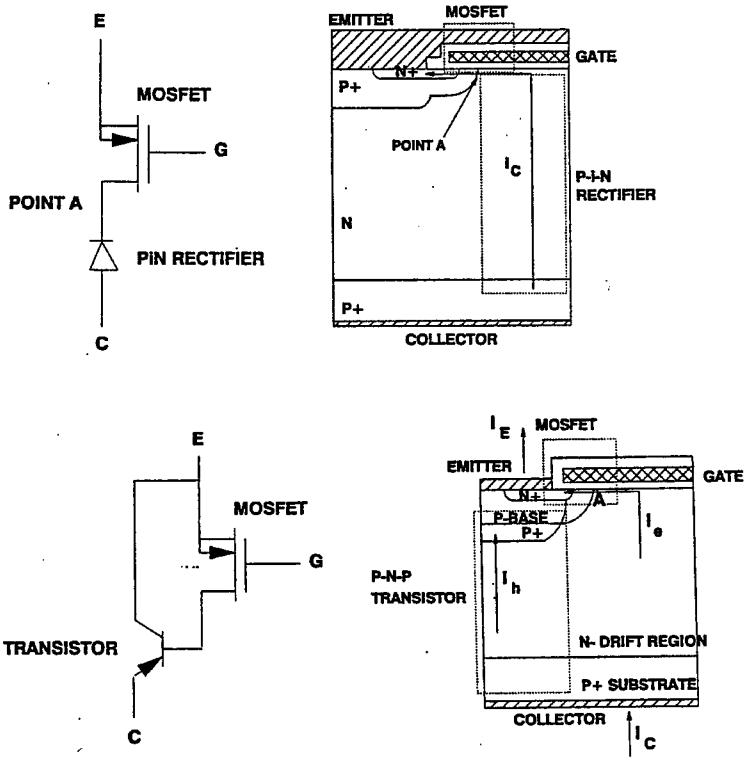


Fig. 7.36. Two models for describing the forward I-V characteristics of the IGB

In the IGBT, the lower wide-base bipolar transistor in the open-base configuration supports the forward blocking voltage. Hence, we can use Fig. 7.6 to design the base doping and thickness necessary. There are two designs. One is have a uniform base doping and maximize the base width so that some undepleted base width is left at the maximum blocking voltage. This is called the non-punchthrough case. If we put a buffer layer of a higher doping than the base between the substrate and base, we can thin down the base and use the buffer layer to prevent the depletion layer from reaching the substrate. The electric field must reduce to zero within the buffer layer so the minimum net space charge needs to be

$$Q_B = d_B N_B \geq \varepsilon_s \xi_C \text{ (Gauss' Law)} \approx 2 \times 10^{13} \text{ q/cm}^2 \text{ for 6H- and 4H-SiC} \qquad (23)$$

where d_B and N_B are the buffer layer thickness and doping respectively. The buffer layer can also be used to control the emitter injection efficiency of the bipolar transistor in the on-state.

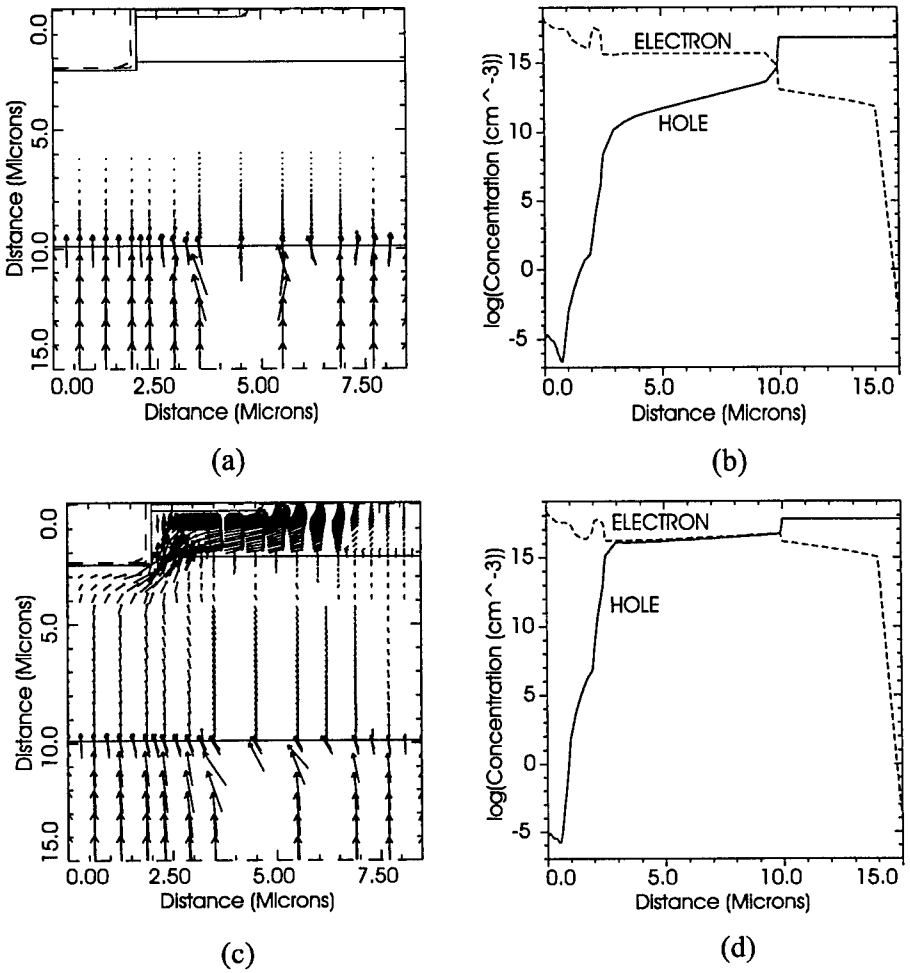


Fig. 7.37. Current flow and carrier profiles for an UMOS 6H-SiC IGBT with two different channel mobilities

In general, the forward conduction characteristics of the IGBT can be modelled with two models: (a) a MOSFET/pin rectifier model and (b) a MOSFET/bipolar transistor model (Fig. 7.36). Actually, dependent on the cell design, DMOS vs. UMOS, carrier lifetime and other device/material parameters for the particular IGBT, one of the two models is more applicable. In the MOSFET/pin rectifier, all the minority carriers injected from the substrate recombine in the drift region and the forward conduction can be expressed as having the cathode (for the n-channel IGBT) current supplied by the MOS channel. So, the forward I-V relation can be expressed (Baliga 1996) as

$$V_F = (2\,k\,T/\,q)\,\ln\,[\,I_C\,d\,/(\,2\,q\,W\,Z\,D_a n_i\,F(d/L_a))] + I_C\,L_{ch}\,/[\,\mu_n\,C_{ox}\,Z\,(V_{GE} - V_T)] \qquad (25)$$

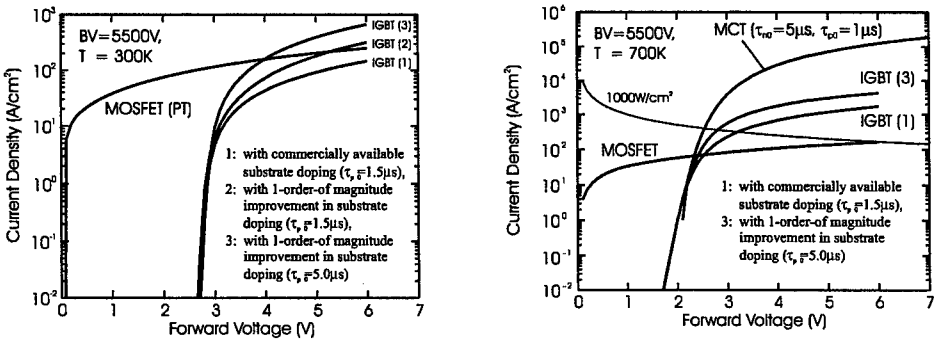
where $F(d/L_a)$ has been defined in the pin rectifier section, L_{ch} is the MOS channel length, Z is the channel width and W is the accumulation layer width under the MOS gate. Due to the small values of n_i for 6H-SiC and 4H-SiC, the turn-on voltage exceeds 2.5V. This model applies to situations in which the ambipolar carrier diffusion is short compared to the drift layer thickness and the poly-Si gate area is dominant over the planar diffused p+/p region (in the n-channel case). With increasing carrier lifetime and an increasing percentage of the injected minority carriers from the substrate can reach the upper p+/p region, the MOSFET/bipolar transistor model is more appropiate. In this model, the forward drop is

$$V_F = (2\,k\,T/\,q)\,\ln\,[\,I_C\,d\,/(\,2\,q\,W\,Z\,D_a n_i\,F(d/L_a))] + (1 - \alpha_{PNP})\,I_C\,L_{ch}\,/[\,\mu_n\,C_{ox}\,Z\,(V_{GE} - V_T)] \quad (22)$$

where α_{PNP} is the common base current gain of the main wide base bipolar transistor. When the current gain decreases and $\alpha_{PNP} \rightarrow 0$, this model reduces back to the MOSFET/pin rectifier model.

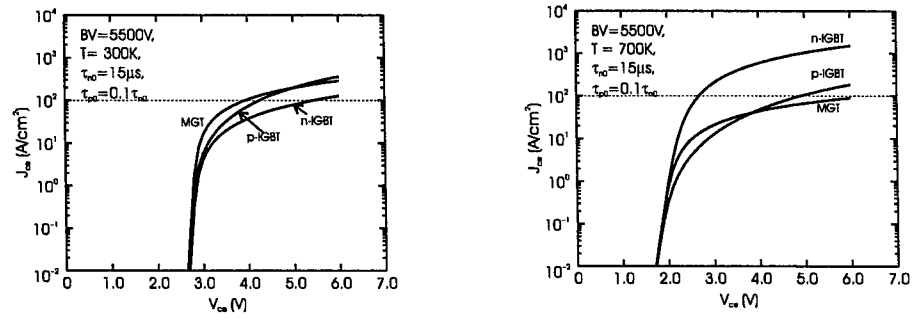
Readily observable from both models is the importance of the MOSFET channel current in determining the IGBT forward drop. In SiC, particularly the trench UMOS structures, the inversion electron layer mobility is often quite small (< 1 cm^2/V-s). To illustrate the importance of the channel mobility, the current flow vectors of a 6H-SiC UMOS IGBT have been shown in Fig. 7.37 for two different channel mobilities. With reduced channel mobility, the conductivity modulation of the drift region is significantly decreased.

To compare the performance of the IGBT with the power MOSFET and MCT, the forward I-V characteristics of these devices with 5000V rating are shown in Fig. 7.38. The IGBT has a lower forward drop than the power MOSFET but higher than the MCT, due to the different levels of conductivity modulation. Also, the forward I-V characteristics of 5000V n- and p-channel IGBT's and a n-channel MGT at 25 and 400°C are compared in Figs. 7.9(a) and (b) respectively. The n-channel IGBT is superior over p-IGBT and n-MGT at room temperature but at elevated temperatures, the higher current gain of the npn over pnp results in making p-IGBT and n-MGT very competitive in terms of forward drop. Also, the material parameters, such as lifetime and substrate resistivity, can significantly impact the on-state characteristics.



(a) (b)

Fig. 7.38. Calculated forward I-V characteristics of 5000V 4H-SiC UMOS FET, IGBT and MCT at (a) room temperature and (b) 400°C



(a) (b)

Fig. 7.39. Calculated forward I-V characteristics of 5000V SiC UMOS n- and p-channel IGBT and MGT at (a) room temperature and (b) 400°C

As shown in Fig. 7.40 for the DMOS IGBT case, the total forward drop across the IGBT consists of several components. These include the MOS channel drop (V_{MOS}), the JFET region drop (V_{JFET}), the drift region drop (V_{drift}) and the junction drop. The JFET region drop can be neglected and the drift region drop can be significantly reduced with increasing trench depth for the UMOS IGBT case.

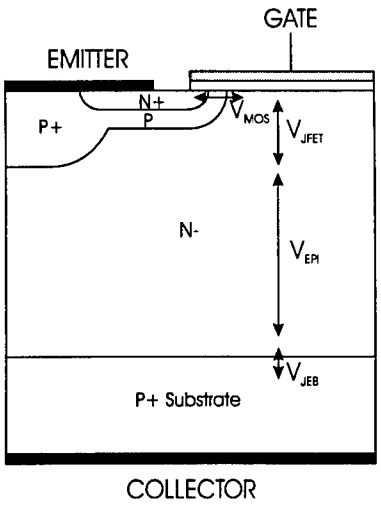


Fig. 7.40. Schematic cross-section of the DMOS IGBT, showing the various components of the forward voltage drop in the on-state

Besides on-state performance, the switching characteristics of these bipolar transistors need to be optimized so as to minimize the switching energy loss. Due to the much reduced drift layer and higher background possible with SiC, the turn-off time is substantially faster in SiC than silicon devices. In Fig. 7.41, the turn-off time for a 5000V IGBT and MGT as a function of lifetime is shown. It can be seen that the open-base turn-off of the IGBT leads to a turn-off time dependence on the minority carrier lifetime and, in this case, the turn-off time is less than 1 μs. To minimize the power transistor for total power loss, a forward drop vs. turn-off time is usually performed. Such a tradeoff curve is calculated for a 5000V IGBT and shown in Fig. 7.42.

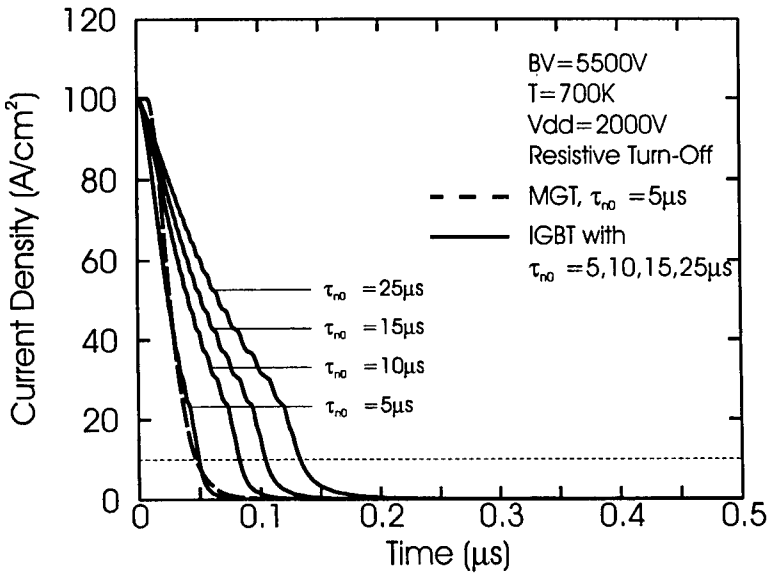


Fig. 7.41. Turn-off characteristics of 5000V 4H-SiC UMOS IGBT with different lifetimes

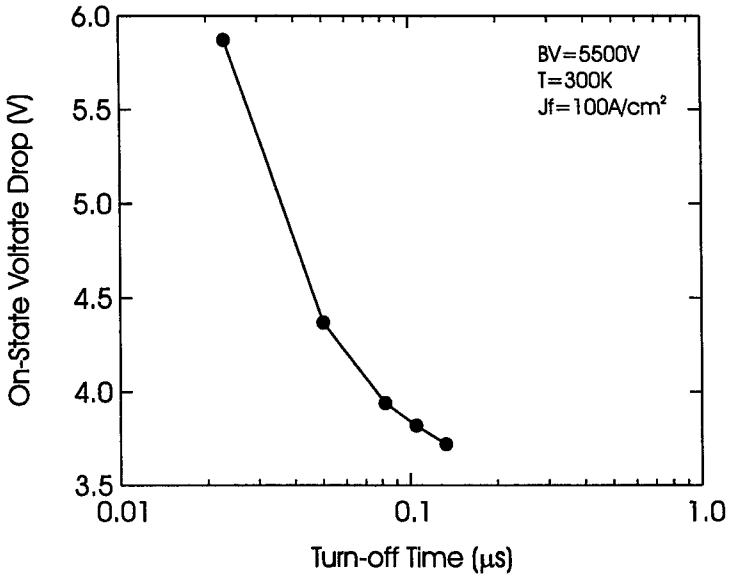


Fig. 7.42. Forward drop vs. turn-off time tradeoff for 5000V 4H-SiC IGBT

To quantify the ruggedness of the power transistor under high-voltage switching, safe-operating-areas are often defined. The most demanding switching condition imposed on the transistor is the high-current turning off under high-voltage inductive loads and the transistor capability can be assessed by the reverse-biased SOA (RBSOA). The reverse-biased SOA's of n- and p-channel IGBT's with non-punchthrough and punchthrough designs are shown in Fig. 7.43(a). Unlike silicon, the p-channel IGBT's have larger RBSOA's than those of the n-IGBT's in SiC, due to the larger hole ionization coefficient.

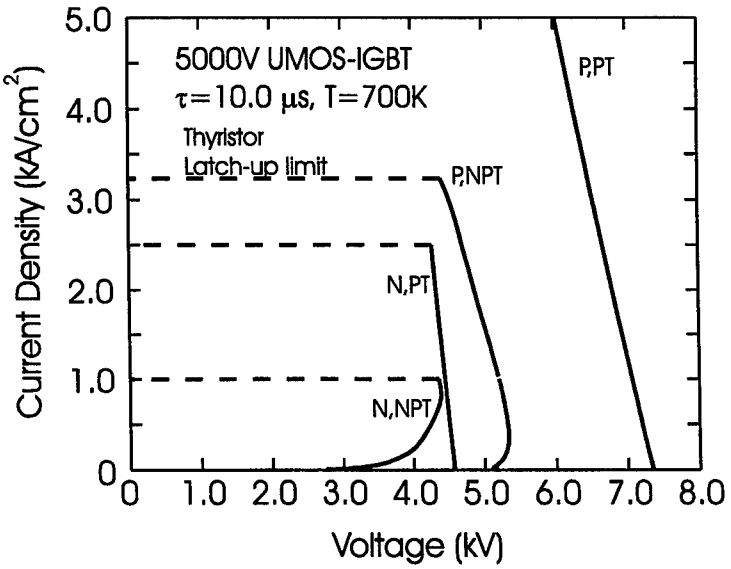


Fig. 7.43. Reverse-biased safe-operating-area (RBSOA) of 5000V UMOS n- and p-channel IGBT's with punch-through and non-punch-through structures

Experimentally, only three reports on SiC IGBT's have been reported. The first IGBT is a n-channel planerized UMOS IGBT on 6H-SiC. Due to the large unit cell size, the BV is limited by the trench corner breakdown to 300V and the channel mobility is low so that only a small current (< 1mA) (Ramungul, et. al. 1996). A p-channel 4H-SiC UMOS IGBT with a smaller unit cell yielded a BV as high as 800V but the output current is still limited by the channel mobility (Chow, et. al. 1997). Recently, a p-channel 4H-SiC UMOS IGBT (> 10 mA) with higher current was reported but the BV is less than 200V (Palmour).

MGT

Structurally, the n-channel MOS-Gated Transistor (MGT) (Fig. 7.34(e)), which can be fabricated in the same IGBT process, has an n-channel MOSFET driving a narrow-base high-voltage npn transistor. The equivalent circuit of the MGT is shown in Fig. 7.44 and it is worth pointing out that the turn-off MOSFET is an optional feature of this device. This turn-off MOSFET can facilitate greatly the turn-off process. A 600V, DMOS version of the MGT has previously been demonstrated in silicon (Sheppard, et. al. 1998). For SiC, the MGT has the optimum device structure because the n-channel MOSFET provides a higher transconductance than a p-channel MOSFET and the npn bipolar transistor has a higher current gain and BV_{CEO} than the pnp counterpart. Also, when compared to the IGBT, it does not have a four-layer parasitic thyristor and thus has a better forward-biased SOA and has an optional n-channel turn-off MOSFET. In addition, the hole ionization coefficient is larger than the electron coefficient in SiC and, thus, the npn is now more rugged than the pnp. Furthermore, the MGT uses a n+ substrate, which can be doped heavier than the p+ substrate for the n-channel IGBT in SiC. Considering the drawbacks of the MGT, we note that this device has more current non-uniformity and less conductivity modulation in the drift layer in the on-state when compared to the IGBT. Also, the inclusion of the turn-off gate increases the unit cell size and the device layout is less straightforward than the IGBT. In light of these considerations, it is worth considering the MGT together with IGBT in SiC.

The simulated forward I-V characteristic of a 5000V 4H-SiC n-channel MGT is shown in Fig. 7.39. At room temperature, it is similar to both that of the n- and p-IGBT, mainly due to a larger device unit cell size. An analytical I-V model, like the ones shown for the IGBT, has not been developed. Nevertheless, the forward voltage drop can be estimated, to the first order, by combining the models that we have shown for the power BJT and MOSFET.

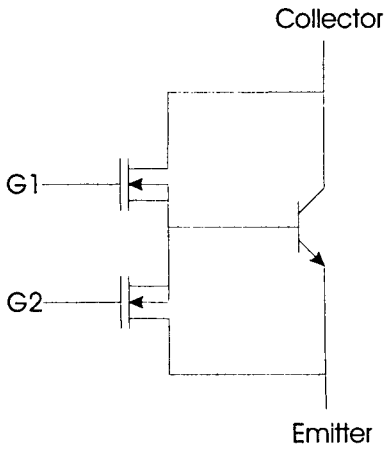


Fig. 7.44. Equivalent circuit diagram of the MGT

Unlike the IGBT, the turn-off characteristics are not necessarily open base and can be controlled by the turn-off MOSFET (M_2). The active turn-off case is to short the gate of the MGT to ground through M2 and the minority carriers that are stored in the base region can be extracted out of the device, similar to the BJT. In this mode, the turn-off time is much faster (~0.2 μs) and almost independent of carrier lifetime. By comparison, the turn-on time in the passive (open base) mode is larger, as shown in Fig. 7.45.

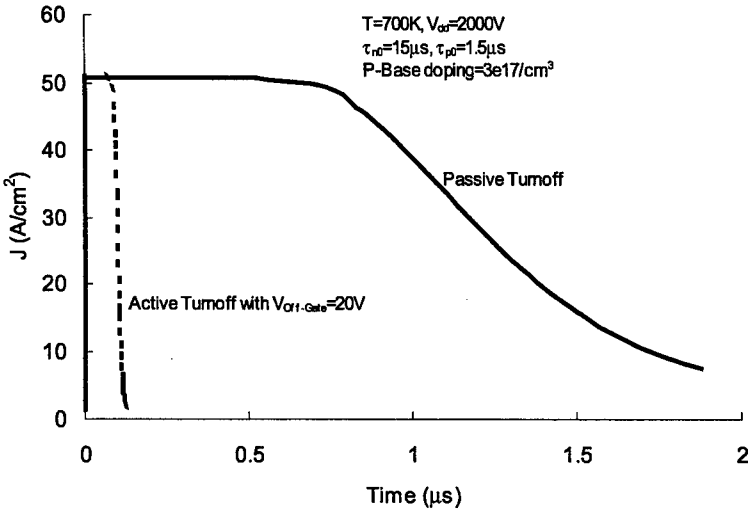


Fig. 7.45. Passive and active turn-off characteristics of a 5000V 4H-SiC MGT

The main bipolar transistor of the MGT has a narrow-base, lightly doped collector structure. At high current densities with high-level injection, the base region will extend into the collector region and the peak electric field at the p base/n- collector junction will shift to the n^-/n^+ collector junction (the Kirk Effect). As a result, the reverse-biased SOA of the MGT, as shown in Fig. 7.46, is unusual in that when the collector current increases, the maximum sustainable collector voltage actually increases. Eventually, the MGT still fails with the formation of current filaments and second breakdown commences. Nevertheless, because of the Kirk effect, the n-channel 4H-SiC MGT has been projected to have a larger RBSOA than those of n- or p-channel IGBT's.

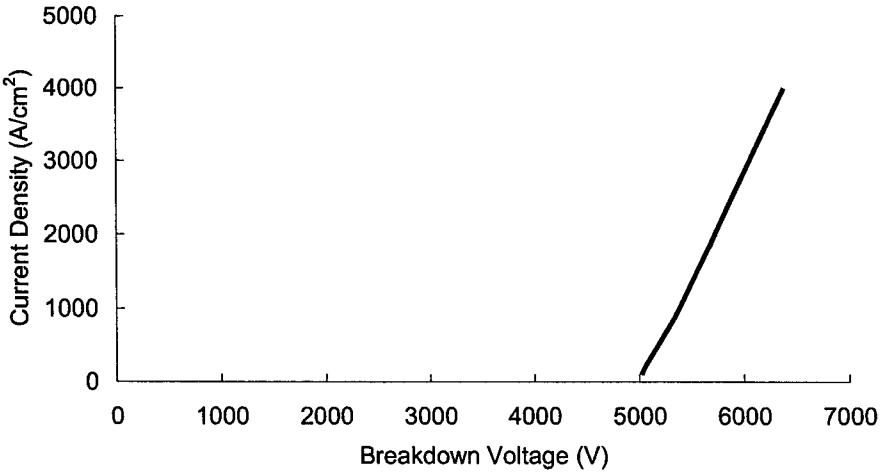


Fig. 7.46. Reverse-biased safe-operating-area (RBSOA) of 5000V UMOS n-channel MGT

The development of the SiC MGT is still in its early stage so that no experimental device has been demonstrated. Also, we can observe that the MOSFET in the structure can be replaced with a JFET or MESFET, particularly if one is concerned with the gate oxide reliability.

HBT

Similar to the HEMT, no HBT in the SiC system has been realized. However, a HBT with heteroepitaxially grown GaN emitter on 6H-SiC substrate has been reported (Pankove, et. al. 1996). An extraordinarily high common-base current gain of $>10^6$ has been reported but no common-emitter characteristic was shown. A high leakage current across the collector-base junction is attributed.

POWER THYRISTORS

Thyristors belong to a family of switching devices that have been specifically developed for power electronics applications.

SCR

The silicon controlled rectifier (SCR) is a thyristor that ultilizes gate current for triggering into the conduction state. The schematic cross-section of a typical SCR is shown in Fig. 7.47 (Ghandhi 1997; Baliga 1996).

In silicon, a wide-base pnp and a narrow base npn is usually used because the higher gain npn can be more easily controlled with the gate terminal and the wide-base pnp has a larger SOA than npn. Since

$$I_A = \alpha_{PNP} I_A + \alpha_{NPN} I_K + I_L \qquad (26)$$

and

$$I_K = I_G + I_A \qquad (27),$$

$$I_A = (\alpha_{NPN} I_G + I_L) / (1 - \alpha_{NPN} - \alpha_{PNP}) \qquad (28)$$

To prevent the thryistor from inadvertent firing, cathode shorts are usually placed on the top cathode surface (Ghandhi 1977; Baliga 1996). An involute gate pattern is adopted to ensure an equi-distance between the cathode and the gate edge. With a cathode short, the gate triggering current is (for a linear stripe geometry)

$$I_{GT} = (V_{bi} / \rho_{SB}) (Z / L) \qquad (29)$$

Where V_{bi} is the built-in potential, ρ_{SB} is the base sheet resistance, Z is the emitter width and L is the emitter length between cathode shorts. It should be noted that the gate triggering current is strongly controlled by the surface geometry design. Another important parameter is the holding current, which is the minimum current needed to sustain the thyristor in the on-state and it is given by

$$I_{HA} = 2 V_{bi} Z / [(1 - \alpha_{NPN}) \rho_{SB} L] \qquad (30)$$

It can be seen that the holding current can be minimized by increasing the sheet resistance of the upper base region and the distance between cathode shorts.

For SiC, due to the difficulties in heavy p-type doping in the substrate, a n+ substrate is usually used. Consequently, the actual thyristor structure studied is complementary to that of conventional silicon SCR's. Fig. 7.48 shows the schematic cross-section of a SiC gate turn-on thyristor (Palmour). From device considerations, the lower transistor being npn improves the BV_{CEO} and safe-operating area but the upper pnp transistor requires a larger gate current to turn on due to lower n-base sheet resistance and current gain. To quantify the performance between pnpn and npnp SCR's, we have calculated their respective holding currents, as illustrated in Fig.7.49 for 5000V 4H-SiC devices. Clearly the SCR with the cathode as substrate is favored.

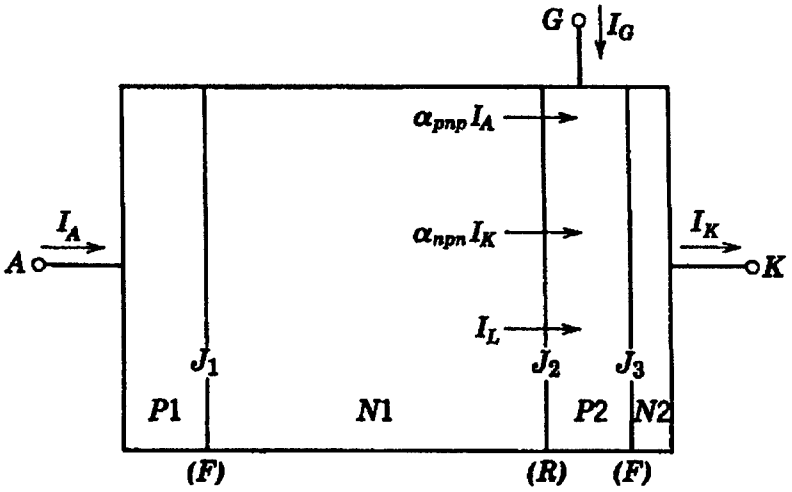


Fig. 7.47. Schematic cross-section of the silicon controlled rectifier (SCR)

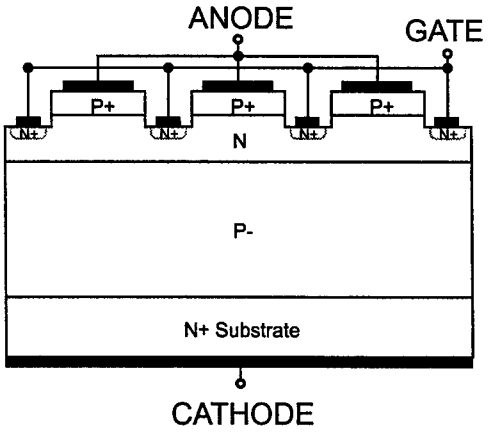
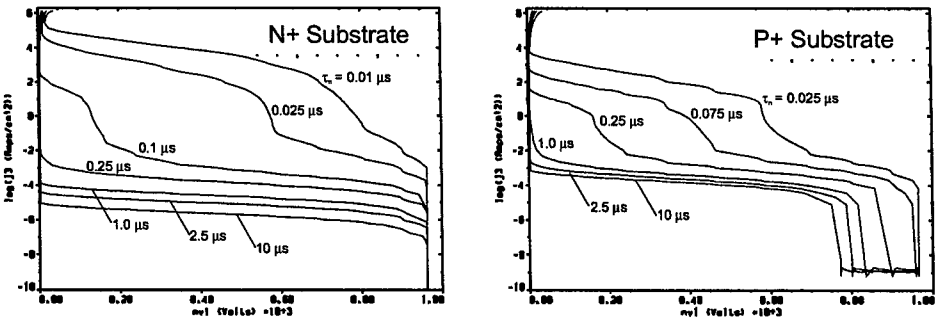


Fig. 7.48. Schematic cross-section of the silicon controlled thyrister



(a) (b)

Fig. 7.49. Simulated holding currents for 5000V 4H-SiC pnpn and npnp SCR's

Once triggered on, the thyrisor on-state characteristics strongly resembles that of a pin junction rectifier, as shown earlier in this chapter. With both the upper and low base conductivities moduated with carriers injected from the anode and cathode, the forward drop approaches that of the pin diode.

GTO

To facilitate turn-off, the thyristors can be designed so that a gate current (in opposite direction to the gate triggering current) is used without device commutation (or anode-cathode voltage reversal). The condition for gate turn-off is (Ghandhi 1977; Baliga 1996)

$$I_G > (\alpha_{PNP} + \alpha_{NPN} - 1)\, I_A / \alpha_{NPN} \qquad (31)$$

and the turn-off gain, β, is defined as the ratio the anode current to gate current. In particular, the maximum turn-off gain is

$$\beta_{max} = \alpha_{NPN} / (\alpha_{PNP} + \alpha_{NPN} - 1) \quad (32)$$

Besides controlling the current gain of the constituent transistors, the surface geometry design, such as the emitter stripe width, plays a critical role in determining the maximum gate controllable current with device failure due to second breakdown (Ghandhi 1977; Baliga 1996).

Shown in Table 7.9 are the experimental thyristors that have been demonstrated. Symmetric and asymmetric 6H- and 4H-SiC gate-controlled thyristors reported have BV up to 3000V and 6A at present (Palmour 1994; Palmour, et. al. 1995). All the published thyristor structures use epi p+ emitter and n+ substrates. The effect of the parasitic contact resistance on the thyristor forward drop has been quantified (Xie & Zhao 1996). The thyristor turn-on process has been studied in (Levinshstein, et. al. 1996) but only some of the dynamic switching characteristics have been measured in detail (Fedison, et. al. 1999). Interestingly, unlike silicon devices, the SiC thyristor turns on faster with increasing temperature (Fig. 7.50) because of an increase in acceptor activation improves hole injection from the p+ emitters. The turn-off characteristics are shown in Fig. 7.51 and the turnoff time increases with temperature because of an increase in recombination lifetime. A maximum turn-off current density of over 100A/cm^2 is possible at 190°C.

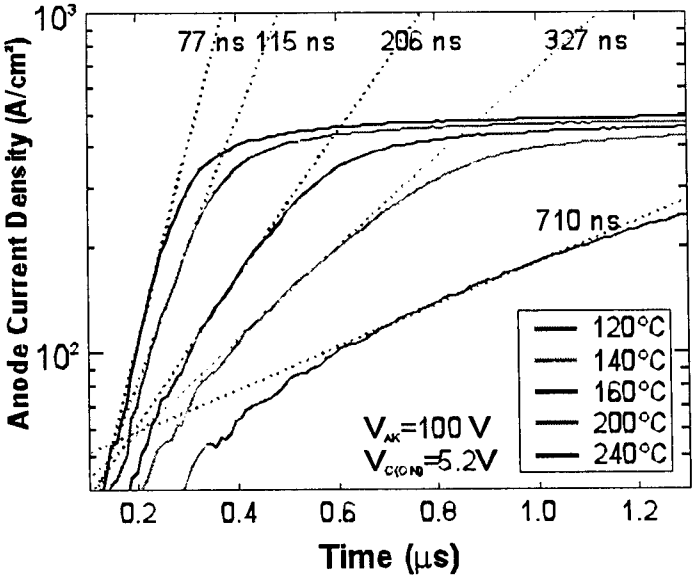


Fig. 7.50. Turn-on current waveforms of an 1100V 4H-SiC GTO at various temperatur

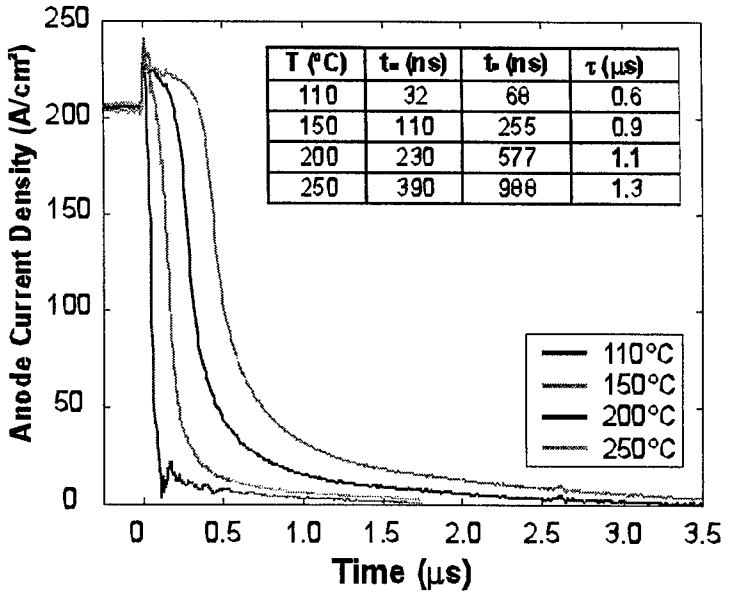


Fig. 7.51. Unity gain turn-off characteristics of an 1100V 4H-SiC GTO at various temperatures

Table 7.9

A list of SiC power thyristors that have been experimentally demonstrated.

DEVICE TYPE	POLYTYPE	Power Ratings	Features	Developer
Thyristors	6H-SiC	100V, 20mA	Gate Triggered	Cree, 1993
	4H-SiC	900V, 2A	Gate Triggered, 0.82 mΩ·cm^2	Cree, 1996
	6H-SiC	100V, 1.8A	Gate Turn-Off (GTO) V_{F100}= 2.9V, J_{max}= 5200A/cm^2	**ARL, 1995**
	4H-SiC	600V, 4.2A	Gate Turn-Off (GTO), Involute Gate, (1600A/cm^2, V_F= 4.5V)	Northrop Grumman, 1997
	4H-SiC	600V	Implanted p+ Emitter	**RPI, 1997**
	4H-SiC	1100V	Gate Turn-Off(GTO), V_{F100} ~ 5V	GE/RPI, 1999
	4H-SiC	600V	Implanted n Base	RPI, 1999
	4H-SiC	2600V, 12A	GTO, V_{F100} ~ 4V	Cree, 1999

Note: V_{F100} is defined as the forward voltage drop at J_F= 100A/cm^2.

Probably due to reduced injection emitter from residual implant defects, only GTO's with epi-grown emitter have been reported so far. We have tried an implanted p+ emitter process with Al/C/B on a symmetric thyristor structure with a drift layer of 10μm and have obtained BV of 600V (Fedison, et. al.) but the forward drop (5-20V) is higher than expected. The sheet resistance of the implanted p+ emitter needs to be further improved to enhance the injection efficiency and lower the contact resistance. Furthermore, the turn-off gain of SiC GTO is expected to be less than the silicon counterpart if the complementary structure is adopted. The reason is that the upper transistor is pnp in the SiC case and hence it has less current gain. According to Eq. (32), β_{max} is thus smaller. Experimentally, turn-off gains between 3 and 7 have been measured on 700V 4H-SiC GTO's (Agarwal, et. al. 1997). The field-controlled thryistor (Baliga 1987) has also been experimentally demonstrated in 4H-SiC (Singh, et. al. 1997) but it is usually a depletion mode device similar to the JFET. Finally, with the reduced base widths, SiC thyristors can switch at a higher frequency than Si devices of the same rating. For example, 700V 4H-SiC GTO's with a switching frequency up to 250KHz have already been reported (Palmour, et. al. 1997).

MOS-gated Thyristors

MOS-gate thyristors use a gate voltage for turn-on and turn-off and they have been actively studied in silicon. Examples of these are the MOS-Controlled Thyristor (MCT) and Emitter Switched Thyristor (EST) (Baliga 1996). Usually, a MOSFET is connected in series with the emitter terminal like the EST or connected in parallel across the emitter-base junction like the MCT. Due to the process complexities, 4-layer MOS-gated thyristor structures are preferable 5-layer ones. The MCT, usually implemented with 5 layers, has a 4-layer version though the turn-off performance is not as good as the 5-layer counterpart. No functional MOS-gated thyristor in SiC has been reported so far.

MATERIALS AND PROCESS CHALLENGES

At present, commercial 4H-SiC substrates of up to 2 inches in diameter are available and custom n- and p-type epitaxial layers up to 50 μm can be ordered. For high- voltage devices, total epitaxial layer thickness of at least up to 30μm with acceptable surface flatness and doping uniformity and minimum compensation is needed. To minimize parasitic substrate resistance and maximum carrier concentration, a doping of 10^{19} cm^{-3} would be desired. Such a high doping level seems to be difficult with p+ substrates. The most severe structural defect is the micropipe but its density has been substantially improved (to a recently reported value of less than 1 micropipes/cm^2). A micropipe density of less than 1/cm^2 is needed to realize devices of current ratings larger than 100A with reasonable yield. Other structural defects, such as screw dislocations, appear to correlate with excessive leakage current in 4H-SiC pn junctions (Neudeck, et. al. 1999). Despite the continuing improvement of SiC MOS interfacial parameters (to, at present, a fixed oxide charge density close to $10^{11}/cm^2$ and an interface state density less than $3x10^{10}/cm^2$), the correlation between surface state densities with inversion layer mobility is weak. Hence, the inversion layer mobility in 6H- and 4H-SiC needs to be optimized and correlated to surface process conditions. Recent advances in n-type implantation (Patel, et. al. 1998; Khemka, et. al. 1999; Capano, et. al. 2000; Singh & Palmour) yield sheet resistance values approaching those in silicon (as low as 50 Ω/square) but p-type implanted layers still have too high a sheet resistance (> 5 KΩ/square) (Itoh, et. al. 1998; Seshadri, et. al. 1998). Ohmic contacts of reasonable contact resistivities (< 10^{-4} Ω-cm^2) have been made to SiC (Crofton, et. al. 1997). Usually, Ni is used on n-type contacts and Al is used for p-type contacts. A relatively high (around 1000°C) sintering step is performed for contact formation. Formation of p-type contacts is more difficult because a high surface hole concentration is often hard to achieve due to the deepness of the acceptor levels (> 180meV).

SUMMARY

W e have reviewed the progress in SiC power devices in the last few years. Besides the figures of merit, we have discussed the physics of operation of major two- and three-terminal homojunction devices that are applicable to SiC. The performance potential, tradeoffs, and limitations of these SiC devices are discussed, together with their recent experimental demonstrations. We expect continuing technological improvement and device commercialization in this area in the next two years.

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APPENDICES

APPENDIX A: BIOGRAPHIES OF PANELISTS AND OTHER TEAM MEMBERS

PANELISTS

Name: **Vladimir Dmitriev, Panel Chair**
Address: TDI, Inc.
8660 Dakota Drive
Gaithersburg, MD 20877

Dr. Dmitriev has over 18 years of research experience in the epitaxial growth of wide bandgap semiconductors and device fabrication. He received his masters of science degree at Leningrad Electrotechnical Institute in 1978, Ph.D. in 1986 and Doctor in Science degree in 1996, both at the Ioffe Institute. His experience includes four years at Cree Research, Inc., where he was primarily responsible for the development of epitaxial process for III-V nitrides for blue light emitters. From 1992-96 he also directed Cree Research Eastern European Division, the Russian affiliate of Cree.

His particular interest is in mechanisms of epitaxial growth of semiconductors, and in the physics of wide bandgap semiconductor pn structures. He has published over 60 scientific papers and is co-inventor on eight USSR and three U.S. issued patents.

Name: **T. Paul Chow**
Address: ECSE Department and Center for Integrated Electronics
Rensselaer Polytechnic Institute
Troy, NY 12180-3590

Dr. Chow received his B.A. (mathematics and physics, summa cum laude, 1975) from Augustana College, Sioux Falls, South Dakota, M.S. (Materials Science, 1977) from Columbia University, and Ph.D. (electrical engineering, 1982) from Rensselaer Polytechnic Institute, Troy, New York. From 1977-89 he worked at General Electric Corporate Research and Development, Schenectady, NY. He was first involved with developing CVD processes and characterization of doped tin oxide and indium oxide thin films for transparent electrode applications in solid-state imagers, and with refractory metals and metal silicides for MOS VLSI applications. From 1982 to 1989, he participated in the design and process development of various discrete and integrable MOS-gated unipolar and bipolar devices (such as the MOSFET, IGBT, and MCT), and in process architecture and integration of high-voltage integrated circuits. Since 1989, he has been on the faculty of the Electrical Systems and Computer Engineering Department of Rensselaer Polytechnic Institute as an associate professor.

His present research interests are in developing new device concepts and circuit models for high-voltage power devices and integrated circuits, process integration of ULSI metallization, and in process research of silicon and wide bandgap compound semiconductors. He has published over 50 papers in scientific journals, presented over 70 conference talks, contributed three chapters in technical textbooks and has over ten patents. He received the Solid State Science and Technology Young Author Award of the Electrochemical Society in 1982 and the Horizon Award from Augustana College in 1986. He is a senior member of the IEEE and a member of the Electrochemical Society. In 1990-97, he was the Editor for *Solid State Power* in the IEEE Transactions on Electron Devices. At present, he is the Chair of the Membership Committee of the IEEE Electron Devices Society.

Name: **Steven P. DenBaars**
Address: Materials and ECE Depts.
University of California
Santa Barbara, CA 93106

Dr. DenBaars is a Professor of Materials and Electrical Engineering at the University of California, Santa Barbara. He received his Ph.D. Degree in Electrical Engineering from the University of Southern California in 1988 under the direction of Professor P.D. Dapkus. From 1988 to 1991 Professor DenBaars was a member of the technical staff at Hewlett-Packard's Optoelectronics Division involved in the growth and fabrication of visible LEDs.

His current research interests are in metal organic chemical vapor deposition (MOCVD) of III-V compound semiconductor materials and devices. Specific research interests include growth of wide bandgap semiconductors (GaN based), and their application to blue LEDs and lasers and high power electronic devices. This research has lead to the first U.S. university blue laser demonstration and over seven patents pending on GaN growth and processing. He is the principal investigator of the DARPA-funded Multi-university Nitride Consortium, which will develop and transfer GaN technology to industry. In 1994 he received a NSF Young Investigator award. He has authored or co-authored over 75 technical publications, given 60 conference presentations and has ten patents.

Name: **Michael S. Shur**
Address: Center for Integrated Electronics and Electronics Manufacturing
CIEMM CII #9017
Rensselaer Polytechnic Institute
110 8th St.
Troy, NY 121180-3590

Dr. Shur received his MSEE degree (with honors) from St. Petersburg Electrotechnical Institute in 1965 while he received his Ph.D. in Physics (1967) and Doctor of Physics and Mathematics degree (1992) from Ioffe Institute. He has held research or faculty positions at A.F. Ioffe Institute, Wayne State University, Oakland University, Cornell University, IBM T.J. Watson Research Center and the University of Minnesota. In 1989-1996, he was John Marshal Money Professor at the University of Virginia, where he was also a member of the Center for Advanced Studies from 1989 to 1991 and the Director of the Applied ElectroPhysics Laboratories in 1996. Since 1996 he has been Patricia W. and C. Sheldon Roberts '48 Professor of Solid State Electronics at Rensselaer Polytechnic Institute, where he is also Associate Director of the Center for Integrated Electronics and Electronic Manufacturing. Dr. Shur has served as a consultant to major electronics companies, published more than 600 technical papers, has given many invited, keynote and plenary talks and lectures, authored, co-authored and edited 17 books and holds 25 patents on solid state devices.

He is a Fellow of IEEE, a Fellow of the American Physical Society, a member of Eta Kappa Nu and Tau Beta Pi, a member of the Electrochemical Society, SPIE, and Commission D (electronics and photonics) of the International Union of Radio Science. In 1987-96 he served as Secretary, Vice-Chair and Chair of the U.S. Commission D. In 1990-93 he served as an Associate Editor of *IEEE Transactions on Electron Devices*. He is now co-Editor-in-Chief of the *International Journal of High Speed Electronics and Systems* and Member, Honorary Advisory Board of *Solid State Electronics* magazine. He has also served as General Chair, Program Committee Chair, Committee Member, Session Chair and Organizer at many national and international conferences. In 1994, the Saint Petersburg State Technical University awarded him an Honorary Doctorate.

Name: **Michael Spencer**
Address: 418 Phillips Hall
Cornell University
Ithaca, NY 14850

Dr. Michael Spencer, Professor of Electrical Engineering, Cornell University was born in Detroit, Michigan and raised in Washington, DC. Dr. Spencer has over fourteen years of research experience in the epitaxial and bulk growth of compound semiconductors such as GaAs, SiC and AlN (growth techniques include molecular beam epitaxy, vapor phase epitaxy, liquid phase epitaxy, and sublimation), microwave devices, solar cells and electronic materials characterization techniques (including deep level transient spectroscopy and photoluminescence). His particular interest has been in the correlation of device performance with material growth and processing parameters. Recent work has emphasized wide bandgap materials and Dr. Spencer's group was the first to produce conducting AlN and thick films of beta SiC grown by the bulk sublimation technique.

Dr. Spencer, has received a Presidential Young Investigator Award for 1985, the Alan Berman Research Publication Award from the Naval Research Laboratories in 1986 (for research leading to the first identification of a self interstitial defect in AlGaAs), the White House Initiative Faculty Award for Excellence in 1988, a Distinguished Visiting Scientist appointment at Jet Propulsion Laboratories in 1989 and a 1992 recipient of a NASA Certificate of Recognition. He received his B.S. and M.S. in Electrical Engineering and his Ph.D. in Electro-Physics from Cornell University. Dr. Spencer's experience includes two years at AT&T Bell Laboratories, where he supervised and managed the design, prototype production and manufacture of two different product lines of power rectifiers. Dr. Spencer has served as a research scientist and/or consultant to General Electric, the Naval Research Laboratories, Jet Propulsion Laboratories, Lawrence Livermore National Laboratories and (NASA) National Aeronautics and Space Administration.

He has authored over 50 publications in the area of compound semiconductor research. He has also presented numerous scientific papers. Dr. Spencer is on the permanent committee for the Electronic Materials Conference, the Compound Semiconductor Conference, as well as helped initiate and form the International Conference on Silicon Carbide and Related Materials. Dr. Spencer is currently one of the Directors of the NSF sponsored National Nano-Fabrication Network (NNUN). He currently has co-authored three U.S. patents with several patents pending.

Name: **George White**
Address: Packaging Research Center
Georgia Institute of Technology
813 Ferst Drive NW
Atlanta, GA 30332-0560

George White is currently the Associate Director for Research of the Packaging Research Center at the Georgia Institute of Technology in Atlanta. Prior to joining the Packaging Research Center in November of 1998, he was employed by the Motorola Corporation of Schaumburg, Illinois was he was the Government Programs Manager for the Applied Simulation and Modeling Research Group of the Corporate Computer Software Center. There he served as program manager for the Motorola led embedded mass formed passives consortium, the demonstration of electrical and mechanical design of low cost mixed mode modules and the holographic optical interconnect technology consortium. Prior to joining Motorola, he was employed at the International Business Machines, Corporation as a Development Manager for the Advanced Thin Films Group in Fishkill, NY. There he developed low cost thin film processes for electronic packaging for IBM's mainframe and cost performance products. He holds over 11 US patents, and a number of publications. He received his Ph.D. and M.S. degrees from the University of Illinois in Metallurgical Engineering in Urbana, Illinois, and his bachelor's degree in Physics from Hampton University in Hampton, VA.

OTHER TEAM MEMBERS

Name: **Usha Varshney**
Address: Program Director,
Div. of Electrical and Communications Systems
Directorate of Engineering
National Science Foundation
4201 Wilson Boulevard, #675
Arlington, VA 22230

Dr. Varshney received her B.Sc. Honors School and M.Sc. Honors School degrees from Panjab University. She was awarded the Ph.D. degree in Physics by the Indian Institute of Technology, New Delhi in 1983. She joined the National Science Foundation in 1997 as Program Director of the Physical Foundations of Enabling Technologies and Integrative Systems programs in the Division of Electrical and Communications Systems. She comes from an industrial background and maintains a strong interest in the interdisciplinary nature of scientific and engineering research. She has conducted research in industry/university/government cooperative programs. She has been involved with research in the areas of electro-ceramic materials and thin films for integrated microelectronic components and devices including non-volatile random access memories using ferroelectrics, uncooled focal plane arrays using pyroelectrics, radiation-resistant solar cells and photovoltaic devices using optoelectronic materials, thermal detectors and antennas using high Tc superconducting fibers, thin and thick films, and flat panel displays using phosphors, magnetic materials, thin films and devices including integrated planar magnetic components and circuits, monolithic magnetics for megahertz frequency high density power supplies and giant magnetoresistance sensors and devices. Dr. Varshney has also been involved with laser and plasma processing of materials and devices, and high temperature, high frequency wide bandgap semiconductor materials and associated devices including silicon carbide, aluminum nitride, diamond and iron titanates. She has a strong interest in the area of processing of bulk material, epitaxial growth of films and patterning techniques for high temperature electronic devices. She also has interests in electronic packaging and interconnections for high temperature applications, sensors, microelectromechanical systems (MEMS) and nanotechnolgy.

Name: **John M. Zavada**
Address: ARL-European Research Office
223 Old Marylebone Road
London NW1 5TH, UK

John M. Zavada is the Director of the U.S. Army Research Laboratory - European Research Office in ondon and also serves as Chief of the Electronics and Physics Branch. Previously, he managed a research program in optoelectronics at the U.S. Army Research Office in Durham, NC. He earned his BA from the Catholic University of America and his MS and PhD degrees in physics from New York University. Later he worked as a research physicist at Army laboratories in Philadelphia, PA, and at Picatinny, NJ. Dr. Zavada has authored more than 100 papers in the areas of scattering of light from rough surfaces, ion implantation, optical characterization of semiconductors, and hydrogen and rare earth impurities in materials. He has served on numerous advisory panels, including the Joint Services Electronics Program and the Advisory Group on Electronics, and on program committees for international conferences in solid state physics and electronics. He has held adjunct academic positions at Drexel University, North Carolina State University, and the Imperial College of Science and Technology. He is a member of the American Physical Society, the Materials Research Society, and is a Fellow of the Optical Society of America.

APPENDIX B: EUROPEAN SITE REPORTS

Site: **DaimlerChrysler**
Ulm, GERMANY

Date Visited: 9 June 1999

TTEC Attendees: J. Zavada (report author)

Hosts: Prof. Hermann Schumacher, University of Ulm
Dr. Andrei Vescan, DaimlerChrysler
Dr. Helmut Leier, DaimlerChrysler

DAIMLERCHRYSLER

Introduction

DaimlerChrysler is a German-American company that was formed by the merger of two industrial giants, Daimler-Benz and Chrysler, in 1997. On Wednesday afternoon, Dr. Zavada met with Dr. Helmut Leier, who is director of the high frequency electronics department, and with Dr. Andrei Vescan, who is involved with research technology of III-V components.

Dr. Leier gave an overview of DaimlerChrysler and its research activities. The central research center employs about 1,800 people and sponsors nearly 500 students. Since the main activity of the company is automobiles, much of the research activities concentrate on cars and traffic.

There are three main areas of research: microelectronics and micro-systems; information and communications; and high frequency devices. Currently, most of the high frequency device work is based on GaAs. High power (> 1 W/mm), high frequency (> 10 GHz) HEMTs and MESFETs are being developed. The research on GaN is directed at extending the performance of the GaAs devices. Dr. Leier emphasized the importance of minimizing the cost while extending device performance. High power GaN devices will not make a major impact until fabrication costs are competitive with GaAs devices. Dr. Leier also mentioned that DaimlerChrysler is part owner, with Thomson-CSF, in United Monolithic Semiconductor (UMS). DaimlerChrysler acquires the GaAs wafers for high power devices from UMS.

III-V Components

Dr. Vescan gave Dr. Zavada a presentation on the research at DaimlerChrysler concerning high frequency, high power GaN-based devices. He said that DaimlerChrysler is not presently involved with growth of GaN films. SVT Associates, in the United States, is collaborating with DaimlerChrysler and currently provides the necessary films. The work at DaimlerChrysler centers on the design, processing, and fabrication of GaN-based devices. Dr. Vescan said that the optimum processing conditions are very dependent upon the source of the GaN films. These conditions can be determined only after repeated trials and device testing. The group at DaimlerChrysler has been working in close collaboration with Prof. Kohn at the University of Ulm on device properties of AlGaN/GaN MODFETs (modulation doped field effect transistors).

Clean Room Facilities

Later in the afternoon, Dr. Leier and Dr. Vescan took Dr. Zavada on a tour of the clean room facilities at DaimlerChrysler. The clean rooms are similar to the ones at the University of Ulm; however, they are larger, measuring approximately 1,000 sq. meters. Some areas are class 100 and others are class 10. Following the merger of Daimler-Benz and Chrysler, half of the clean space was divided between DaimlerChrysler and UMS. I was only shown the DaimlerChrysler clean rooms. Still they comprise a first-rate facility for processing III-V materials.

Site: **High Pressure Research Center (Workshop)**
Polish Academy of Sciences
Ul. Sokolowska 29/37
01-142 Warsaw POLAND
+48-226-32-5010
www.unipress.waw.pl

Date Visited: 10 June 1999

TTEC Attendees: S. DenBaars (report author), M. Shur, U. Varshney, G. White

Hosts: Dr. W. Porowski (HPRC)
Dr. I. Grzegory (HPRC)
L. Leszynski (HPRC)
L. Dobrzauski (IEMT)
W. Wolosinski (Warsaw Univ. of Tech.)
A. Jelenski (IEMT)
J. Szmidt (Warsaw Univ. of Tech)
Dr. J. Weyher (HPRC)
R. Beck (Warsaw Univ. of Tech.)

BACKGROUND

A comprehensive workshop on GaN activities in Poland was held for the panel members at the High Pressure Research Center (HPRC) in Warsaw, Poland. This included groups from Warsaw University of Technology, the HPRC research group Unipress, and the Institute of Technology of Materials and Electronics (IEMT).

TECHNOLOGY DISCUSSION

Dr. Porowski of Unipress hosted the meeting at the High Pressure Research Center and had also invited representatives of several of the other leading Polish research efforts in wide bandgap semiconductors to the workshop. Within Poland there are 14 research efforts developing GaN materials and devices. Recently the Polish government has approved funding of the large national project "Development of Blue Optoelectronics". This program will focus on blue lasers, solar blind detectors, and full-color industrial displays.

GaN Bulk Substrate

Unipress is the research group within HPRC working on GaN bulk crystal growth from a melt. One of the most impressive achievements the panel saw in Europe was the "defect free" bulk GaN wafers grown from melt under extremely high pressure. Dr. Isabel Grzegory gave an overview of the high pressure solution growth method used for depositing the bulk single crystals.

The size of the substrates has steadily increased up to 1 cm in 1999 from 5 mm in 1997. In comparison to GaN on sapphire technology which exhibits 1 E+9 cm^{-2} defect densities, or ELO films, which are in the 1 E+6 cm^{-2} to 5 E+5 cm^{-2} range, the bulk GaN crystals possess 10 to 1 defect per square centimeter. These densities were estimated from etch pit counts and correlated to TEM measurements of higher defect densities found on standard GaN sapphire technology.

The team was allowed to observe the bulk crystals under both optical microscopes and field emission SEM. Both n-type bulk crystals and semi-insulating bulk crystal have been grown. The semi-insulating substrates were highly resistive 1 E+5 ohm^{-cm} and could be used for thin film deposition of high power AlGaN/GaN microwave amplifiers (Litwin-Staszewska et al. 1999). Very high quality homeoepitaxial growth of GaN by MOCVD was obtained on top of these substrates and the films exhibited narrow double-crystal x-ray diffraction (DCXRD) linewidths as low as 21 arcsec. The group at University of Ulm, in collaboration with

Unipress, has obtained thin films that exhibit the narrowest reported PL linewidths at low temperature (0.1 meV)—which is indicative of the uniform high quality film (Komitzer et al. 1999). MBE has also been performed on the bulk crystals. Both Ga-face and N-face polarity bulk substrates have been produced. The bulk crystals also display extremely smooth cleaved facets with rms roughness of 5 angstroms, which would make excellent laser facets.

Unipress is also investigating high power HEMTs, Schottky diodes, and UV detectros. Using MOCVD AlGaN/GaN materials have been grown with sheet carrier charge of 1.2 e+12 cm^{-2}. Large geometry, 1 micron gate length FETs have been fabricated and FET characteristics obtained. High quality Schottky contacts were obtained using Pd/Au metallization, which exhibited barrier heights of 0.8 eV.

IEMT

Researchers at the Institute of Technology of Materials and Electronics are focusing on device fabrication and bulk growth of novel substrates. Panelists toured the facilities for fabricating laser diodes and detectors. Dr. Dobrzauski has already fabricated a GaN UV detector, which showed a peak responsivity at 364 nm. Numerous bulk crystal pullers were in operation. Also, a wide range of high quality optical bulk substrates was being grown such as: Si, GaAs, InP, ZnSe, YAG, LiGaO2, and LiAlO2. Large banks of UPS backup are needed to ensure safe operation in event of a power failure.

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Kornitzer, K., T. Ebner, M. Grehl, K. Thonke, R. Sauer, C. Kirchner, V. Schwelger, M. Kamp, M. Leszczynski, I. Grzergory, S. Porowski. 1999. High Resolution PL and Reflectance Spectra of Homoepitaxial GaN Layers. Paper Tu-17, Proceedings of Intl. Conf. on Nitride Semiconductors, Montpellier, France. pg. 49.

Site:	**IMC, ABB, and KTH** **Electrum Building** **Kistagangen 15** **Kista, Stockholm, SWEDEN**
Date Visited:	11 June 1999
TTEC Attendees:	T.P. Chow (report author), V. Dmitriev, M. Spencer, S. DenBaars, M. Shur, U. Varshney, G. White
Hosts (IMC):	Dr. Christopher Harris, SiC Project Manager Dr. Meitek Bakowski Dr. Andrey Konstantinov
Hosts (ABB):	Dr. Heinz Lendenmann, Project Leader, Switch Development, SiC Project
Hosts (KTH):	Dr. Mikael Oostling Dr. Nils Nordell

IMC

IMC is an applied research company that facilitates technology transfer from the research and development stage to prototyping and manufacturing. It has received both industrial (80%) and government (20%) support to enhance Swedish competitiveness. Recently, it has merged with IOF to form a new company called ACLEO.

IMC has mostly performed research in microelectronics and IOF on optoelectronics. The new company has a wide range of interests in both of these technical areas and has more European presence. IMC has locations in Kista and Linkoping. The Linkoping location focuses on interconnect and packaging of electronics and optoelectronics systems.

There are 53 employees in Kista and 27 in Linkoping. The budget for 1998 was 85 million SEK ($10.5 million) and 120 million SEK ($15 million) for Kista and Linkoping, respectively. It spins off one new company per year on the average. There is a high labor turnover rate (15-20% per year) with the average age of its employees being 34.

Dr. Harris indicated that the researchers in the Kista facility perform work in a variety of areas, including (a) radiation detectors (QWIP, bolometers), (b) optoelectronics, (c) SiC electronics, particularly power devices and (d) microsystem technology (microstructures, sensors). The wide bandgap semiconductor technology has mostly focused on SiC and the application areas are:

- power devices (development for ABB)
- microwave electronics (Ericsson)—high power amplifiers for base stations, 3 GHz, 100 W, entirely SiC so far, but expecting GaN to be applicable at higher frequencies
- high temperature electronics
- sensors, e.g., SiC as X-ray detectors, sensitivity close to human tissues

The highlights of specific technical activities are:

- numerical simulations and design—TMA software based
- portfolio of SiC specific process technologies
  - epi growth (Emcore and Epigress reactors, process support for Epigress)
  - ion implantation
  - dry etching (ECR etching)

  - dielectric growth and deposition
- device and characterization
  - IV, CV, DLTS, Hall
  - optical
  - SEM/TEM/SPM

One example of the application of these process technologies in device fabrication is the demonstration of a 16 GHz (f_{max}) 4 H-SiC implanted-channel SiC MESFET. The gate width is 0.8 μm with optical lithography and 2x smaller with e-beam lithography. A channel mobility of 200 cm^2/V-s has been achieved. Also, measurements of basic material properties of SiC are also performed as part of the Swedish National SiC Program (SiCEP).

Dr. Bakowski presented the high temperature electronics work. This area can be broadly categorized into two sub-areas:

- 200-300°C
  - integrated motor control
  - smart fuel pumps
  - brake by wire
- 400-800(C
  - combustion
  - geothermal

The multi-chip module (MCM) concepts that are devised for these two temperature ranges are different.

- 200-300°C
  - power electronics SiC
  - sensor SiC
  - control electronics Si SOI
- 400-800°C
  - power electronics, sensors, control electronics, all SiC

Besides active devices, high temperature passive components also need to be addressed.

Dr. Konstantinov presented the high temperature sensor research. One approach is to use high temperature gas-absorbing metal-gate MOSFET. Using a Pd gate, hydrocarbons (CH_x) decompose after adsorption to the Pd and the resulting H^+ ions diffuse to the interface, thereby shifting the barrier height. The advantages of using SiC are:

- high operating temperature (e.g., engine exhaust at 600°C)
- fast operation

Other devices that can also be used are MOS capacitors, metal-semiconductor diodes (I-V shift) and MESFETs.

For automotive applications, compared to the conventional Lambda sensor which utilizes a thick Zr layer, the gas-sensor SiC MOSFET developed at IMC offers much faster feedback so that adjustment to each engine cylinder can be made. The salient features of this SiC MOSFET are:

- buried channel
- low threshold voltage
- high temperature operation (17 hrs at 600°C so far)
- high gas response

The goals of this program are:

- long term stability at 600°C
- sensitivity to exhaust products other than hydrocarbons
- electronic noses (MOSFET sensor arrays)

Different metal gates may be used to sense different gas products.

The panel was given a facility tour of the clean room area that is on the ground floor and where all the microelectronics device processing facilities of the three institutions are housed, though separately. The ABB facility includes a high-energy (3 MeV) ion implanter that has a heated end station and a laser direct write aligner. IMC processes a large variety of compound semiconductors for several applications (such as solar cells and optoelectronics). These facilities are very impressive and world-class.

ABB

ABB is a large international industrial company that has a major presence in power generation, transmission and distribution. It was instrumental in getting the SiC program started in Sweden in 1988 and has sponsored many programs in developing the SiC infrastructure in Sweden.

Dr. Lendenmann presented an overview of the ABB businesses and elements of the SiC device program. The power generation plants include hydro, "clean coal," nuclear power and fuel gas cleaning types. ABB is very focused in getting SiC devices into power electronics systems. For example, for a 1-5 MW industrial converter system, it is estimated that Si device replacement with SiC can reduce the size by 1/3. Significant improvement in HVDC system is also projected with SiC devices, with the goal of 50 MW plant in 300 m^2 area.

A 3.5 kV, 200 A 4 H-SiC pin junction rectifier was presented. The diode structure consists of a deep boron junction for good junction leakage and a shallow aluminum implant topped with a p+ epi regrown region for optimal contact resistivity. A multiple-zone boron-implanted JTE has been used for junction termination, in conjunction with a SiN/polyimide over the field oxide as the passivation layer. A phosphorus-implanted n+ region was used as channel stop. Sensitivity analysis between device on-state voltage (V_F < 4 V) vs. epi thickness has been shown for correlation. The leakage current density for diodes with three different areas was shown, with the largest device (7 x 7 mm^2) size having a value of less than 10^{-5} A/cm^2, the best value to date for large-area devices. Dynamic switching of 150 A to 800 V with a dI/dt > 200 V/μsec results in an $I_{RP} < 0.2\ I_F$. The goal is to first implement SiC diodes with Si IGBT, with the implementation of SiC three-terminal switching devices later. Actually, they project that at higher frequencies, the Si IGBT will be thermally limited. At present, there is no GaN work at ABB.

In summary, ABB focuses on the system application and leverage of SiC devices and is perhaps most advanced in the world in incorporating SiC devices into power electronics systems.

ROYAL INSTITUTE OF TECHNOLGY (KTH – KUNGL TEKNISKA HOGSKOLAN)

Prof. Oostling presented his work on semiconductor devices, including heterojunction SiC HBT with GaN emitter. Prof. Oostling collaborates with many researchers around the world. The SiC/GaN HBT consists of 10^{18} cm^{-3} SiC p-base, over which a n+ GaN emitter was grown by MBE. The p-base thickness can be either optimized for high-voltage power (1 μm) or microwave power (optimized for 2 GHz). The device work is largely supported by SiC EP program of the Swedish government. The heterojunction GaN/SiC diode has been improving, reaching a low value of $I_R \sim 10^{-4}$ A/cm^2 at –50V, which is close to ideal. SiC MISFET with MBE grown 17 nm AlN has also been fabricated. The device is functional but the gate is still leaky. Prof. Oostling is well known for his contact work on SiC. TiC formation with $CoSi_2$/Ti bilayer after 900°C anneal leads to a low contact resistivity (10^{-6} Ω-cm^2) on p-type, 10^{19} cm^{-3} doped epi of 6H-SiC. He is also exploring epi TiC layer on SiC that can be formed at 500°C or lower.

Dr. Nordell presented the clean room organization, funding structure and the various programs that utilize the facilities.

Addendum: High Temperature Packaging Capability (George White)

Dr. Chris Harris indicated to us that most of the packaging efforts for IMC were being conducted in Linkoping. However, the effort there is focused primarily on Si multi-chip modules. There they have demonstrated a 3" x 2" compact computing module which consists of a processor and memory chips.

Dr. Vladimir Dmitriev introduced us to Dr. Roumen Kakanakov of the Institute of Applied Physics of Plovdiv, Bulgaria. Dr. Kakanakov, who by chance was working at the offices of IMC during our visit, is a leading authority on high temperature packaging. He has started a small company, which is doing R&D in microelectronics, optoelectronics and sensor semiconductor devices, on Si, GaAs and SiC substrates. Their expertise is in the field of ohmic contacts and packaging. Unfortunately, we were unable to meet with Dr. Kakanakov for any useful length of time, but we subsequently communicated with him via telephone and e-mail. Below is a summary of the conversation and correspondence with Dr. Kakanakov.

In our evaluation of high temperature electronics in Europe, there were very few programs associated with packaging of components for temperatures above 300°C. Therefore, Dr. Kakanakov was asked to comment on a number of questions. Below is a summary of his responses.

Q: What plans are in place to package SiC and GaN devices at temperatures above 300°C ?

A: The problems of high temperature electronics packaging were addressed through European project CP 94063 "Contacts encapsulants and packaging for high temperatures silicon carbide microelectronics", where Kakanakov et al. were responsible for:

- development and manufacture of high temperature packages for power SiC MESFET'S (300-350°C)
- R&D work on packaging processes for SiC chips, which involved the choice of SiC back side metallization, high temperature attach material and chip attachment process to the package—all of which contribute to device reliability at high temperatures (300-350°C)
- evaluation of the reliability of the SiC MESFETs and the packaging process during a 350°C storage test
- measurement of thermal resistance (R_{th})and its behavior during the storage test

After completion of this project in 1997, Kakanakov continued to make a small series of packages for power SiC MESFETs from Thomson-CSF. In early 1999, work began on the NATO project "High Power and High Frequency Devices on LPE-Grown SiC Films", where the packaging group was responsible for R&D of packages and packaging of power SiC diodes. It was also indicated that Kakanakov may have the possibility to get involved in packaging of GaN/SiC HBTs for this project.

An important element in the packaging of high temperature electronics is the base substrate material and attach material. Kakanakov was asked to comment on his work in this area.

As a material for the package base plate, Kakanakov chose a Mo-Cu alloy because of its high electrical and thermo conductivity, and good mechanical properties at high temperatures. Two gold based alloy materials were used as attach materials. The attach materials were gold based alloys of Au (6%) and Si, and Au (12%). The 6% alloy has a melting point of 373°C, and the 12% alloy melts at 363°C. Eventually the group primarily concentrated on the first alloy as the attach material. The backside contact metallization that was used was Ti-Pt-Au on SiC. The advantage here was no change in thermal resistance during high temperature testing. However, Pt and Ti will dissolve in the Au/Si solder when it is liquidus, thereby indicating that more suitable barrier metallurgies will have to be identified at the temperature extremes. Gold wiring bonding is performed using a ball bonder from K&S when making connections from the chip to substrate. When asked about the packaging of passive components, Kakanakov indicated that in principle the same attach material

could be used to attach the passives, but they have no experience with attaching cermet components at high temperature.

From a reliability standpoint Kakanakov agrees that new reliability test equipment and methodologies may be needed for high temperature reliability assessment. Limited reliability data exist for some of their systems; however, some reliability studies were done using thermal resistance measurements. An important need for the advancement of high temperature electronics packaging will be the advent of reliability modeling and simulation.

Site: **Infineon Corporate Research (formerly Siemens AG)**
Siemens Munich Corporate Research Laboratory
Otto-Hahn-Ring 6
D-81-730 Munich GERMANY
Tel: +49-89656-45230
Fax: +49-89656-53294

Date Visited: 9 June 1999

TTEC Attendees: S. DenBaars (report author), M. Shur, U. Varshney, J. Zavada, G. White

Hosts: Dr. Henning Reichert
Dr. Walter Kellner
Dr. Eckhard Wolfgang
Dr. Peter Turkes

BACKGROUND

The Siemens Munich Corporate Research Laboratory is the main research arm of Siemens' semiconductor business. Siemens has recently spun off Infineon Technologies which will be responsible for semiconductor components. Infineon and Osram also have a joint venture to develop GaN blue LEDs and solid-state white lighting using GaN based LEDs. Infineon has a large GaN on SiC LED fabrication facility at Regensburg, Germany. White LED products have recently been introduced by Osram under the trademarked name of TOPLED. In Munich the Central Research Laboratory is involved in GaN MBE (lead by Dr. Reichert), while the GaN optoelectronics effort at Regensburg is primarily using MOCVD.

TECHNOLOGY DISCUSSION

Dr. W. Kellner gave a review of Infineon GaAs products and developments in electronics. As wide bandgap semiconductors may play a role in the microwave power electronic area, Dr. Kellner informed the panel of some recent developments in power electronics. Cellular phone base stations, radio links, and automotive radar are three large applications where semiconductor products are beginning to appear. The automotive radar application requires 77 GHz and only 20 mW; therefore GaAs products are most likely to be marketed first. In the cellular base station application very high powers of 20 to 100 Watts are required at frequencies above 2 GHz. It is unclear if GaN or SiC can address this market at this stage of development, but development on both materials is progressing.

The GaN molecular beam epitaxy (MBE) effort at Siemens was reviewed in detail by Dr. Henning Reichert. Currently the MBE effort is shifting its focus away from optoelectronics and is emphasizing the high microwave power electronic devices. However, Dr. Reichert recently carried out very good fundamental study of GaN and InGaN growth by MBE. P-type doping as high as 1 E+18 cm^{-3} was achieved by MBE. This is important for low contact resistance to LEDs and lasers. A high growth rate of 1.4 microns/hr was achieved and mobilities as high as 460 cm^2/V-sec by MBE growth of GaN on MOCVD GaN templates. An impressive study of InGaN growth yielded good PL as long as 540 nm. Recently single crystal InN was achieved at a growth temperature of 400°C. Dr. Reichert observes a thermal decomposition temperature of 530°C in MBE, which is close to the value obtained by Ombacher et al in 199???. P-type GaN studies indicate an activation energy of 150 meV. The future emphasis in the MBE lab will be on AlGaN/GaN electronic devices and GaAsN for long wavelength lasers.

Siemens Corporate Research Laboratory also has a high temperature silicon electronics effort underway. Dr. Eckhard Wolfgang reviewed the status of silicon on insulator (SOI) and SiC technology at Siemens. SOI is the main material being developed, with SOI technology way ahead of other materials in terms of commercialization. Currently SOI is used for 8 kV thyristors and IGBT 3 kV with are used in railway tram. Eighteen modules are used for power switching of megawatts in railway systems. There is a small research effort on investigating the new wide bandgap semiconductors (mainly SiC) for higher temperature operation.

SiC is mainly being look at for high temperature applications. Currently, silicon is limited to operation temperatures below 200°C. Therefore SiC and GaN could play a role above 200°C. In automotive applications several areas have temperatures in which silicon based devices can be placed. These are in combustion, exhaust, on the engine, and mounted near the brakes. Even if wide bandgap semiconductors can operate at these temperatures, new packaging technology is needed to make devices stand-up to these harsh environments. In addition, reliability of 35 years before failure needs to be designed into the parts. Dr. Wolfgang concluded by saying that much work is needed before WBS can play a role in the high temperature automotive markets.

Pspice models for modeling power electronic devices are available on the web at www.infineon.com.

Site: **Laboratoire d'Electronique de Technologie et d'Instrumentation (LETI)**

Date Visited: 7 June 1999

TTEC Attendees: M. Shur (report author)

Hosts: Dr. Serge Valette, Head of LETI programs
Dr. C. Brylinski, Thomson-CSF
Dr. Joly
Dr. J. Duboz
Dr. M. Deneville
Dr. H. Bergonzo

LETI: THE LARGEST CLEAN ROOM IN EUROPE

LETI (Laboratoire d'Electronique de Technologie et d'Instrumentation) is one of France's largest research institutions. Nine hundred fifty people worked at LETI as of the end of 1998 (722 CEA personnel and 212 personnel of different affiliations, including 165 industrial researchers). LETI consists of five departments and several programs. Fig. 1 shows the organizational structure of LETI.

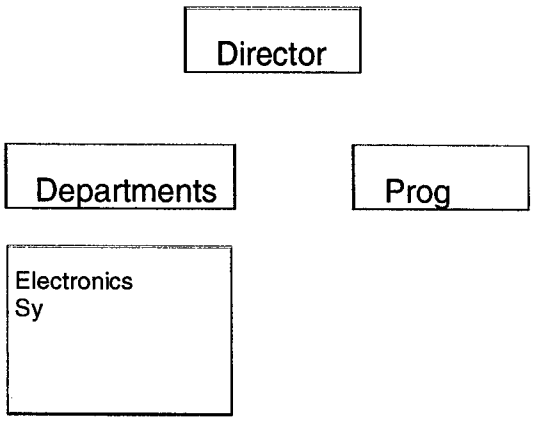

Fig. 1. LETI organizational structure.

LETI strongly emphasizes technology transfer. Feedback loops exist between LETI and French and European industry; LETI possesses hundreds of patents and encouraged spin-offs.

The largest efforts (by percent of total personnel involved) are in microelectronics (27%), defense (22%), nuclear electronics (13%), medical/biological electronics applications (8%), professional electronics (7%), information technology—hardware and software (7%), computer peripherals (6%), telecommunications (5%), and aerospace (5%).

Dr. Serge Valette, Head of LETI programs, described the LETI organizational chart and the major research thrusts. The areas of research and development include

Microelectronics

- CMOS 0.12 - 0.18
- SOI
- Single electron transistor

Microtechnologies

- Sensors

- MEMs
- Recording and displays (fluorescent tip displays)
- Silicon microwave power
- Packages and interconnects

Optoelectronics

- Infrared photodetection (cooled and uncooled)
- Materials for optics

Microlasers

- Laser induced damage threshold from UV to infrared
- Physico-chemical characterization of materials and thin films

Systems

- Electronics for medical applications
- Medical imaging
- Biochip
- Information technology
- Nuclear instrumentation
- Sensors
- Organic components (polymers for optical applications)
- Organic LEDs and flat screens

SILICON-ON-INSULATOR

Drs. B. Aspar and J. L. Pelloie presented the results of silicon-on-insulator (SOI) research at LETI. He described the Smart Cut® process and demonstrated that the quality of Si bonded using the Smart Cut® process is similar to that of the starting material. This technology is applicable not only to Si but also to GaAs-based materials and SiC. For silicon technology, SOI technology demonstrates a higher temperature performance.

SIC ACTIVITIES IN FRANCE

Dr. C. Brylinski of Thomson-CSF reported on the results of SiC research in France. This is his summary of the status of SiC research in France:

- Crystals: research stage
- Wafers: started development
- Devices: started development
- Equipment: first demonstration

SiC epitaxy activity is primarily in LETI and in approximately 10 universities.

Funding sources include: CNRS, industry, and defense programs. SiC projects are divided into those that are part of national programs and those that are part of European programs.

Two national programs in SiC include "Saut Technologique", which is a three-year program (funded by the government and coordinated by industry, with industrial partners contributing some funding as well).

The European SiC program has a goal of achieving 3 inch wafers with no micropipes in three??? and to obtain a low defect density on 2 inch wafers (less than 10 micropipes per cm^2). Under the auspices of this project, the French have teamed with a Swedish-Finnish company, Okmetic.

More detailed goals include cheaper and bigger crystals, lower defect density, the development of a SiC fabrication process compatible with a silicon line, the development of MOS and HBT devices.

Thomson-CSF is developing recessed SiC MESFETs. They fabricated modules with the total 14.4 mm gate periphery with four chips. For devices with wide gates (a few mm), the microwave power was on the order of 1 W/mm; for narrow gate devices, it was about 4 W/mm. The devices were operational up to 500°C in Copernicus package (AlCuMo frame package). In devices fabricated on semi-insulating SiC substrates, the current decreased with time and disappeared in approximately 100s. (Most likely this is a trapping program, most likely associated with vanadium.) The devices fabricated on conductive substrates did not exhibit this effect.

Dr. Joly described the bulk SiC material grown at LETI. The boule diameter was 50 mm. However, the material quality was inferior at the edges. They are using an Epigress two reactor system. The effort at LETI also includes the simulation of crystal growth. Best results achieved at LETI include 95 mohm cm, $p = 10^{19}$ cm^{-3}, 14% activation for 10^{21} cm^{-3} of Al acceptors. A p-n junction operated at 650°C. The junction depth was 220 nm.

There are two European projects dealing with SiC. The funding scale is on the order of one million dollars per year. The first project is called TECSICA. This project provided the basic research funding.

The participants are:

- T.U.B. Berlin
- UAB/CCM (Barcelona)
- Aristoyeles Univ. (Thessaloniki)
- F.O.R.T.H. (Crete)

Endorsers:

- Schlumberger (Clamart)
- C. S. GmbH (Munich)
- LETI (Grenoble)

The second project is called SICOIN. This is an industrial project. Its main goal is to develop a high temperature pressure sensor.

The participants are

- Daimler
- Schlumberger (Clamart)
- T.U.B Berlin
- Aristoyeles Univ. (Thessaloniki)
- Epichem

GaN-RELATED RESEARCH IN FRANCE

Dr. J. Duboz gave an overview of GaN-related research in France.

- Lille: CNRS—Process, electronics
- Caen: CNRS and University—Crystallography
- Strasbourg: CNRS—Nonlinear optics

- Orsay: Thomson-CSF—Everything
- Clermond Ferran: University—Growth, optical
- Lyons: University—Optical
- Grenoble: CEA—Growth (MBE), optical
- Montpellier: ???—Growth (MOCVD), characterization)
- Valbonne: CNRS—Growth optical studies
- EEC project

ANISET: Material oriented. Developed a commercial reactor (available from Riber). Also ECR source and thermal cracker

LAQUANI: Material and device oriented

- Nottingham, Madrid, Lausanne, CNRS (finished), EPFL
- Valbonne (finished)

RAINBOW: Multicolor LEDs and blue laser

- Thomson-CSF
- Philips
- Axion
- Epichem
- University of Seville
- Valbonne
- Erlangen
- Surrey
- Aveires

MIGHT: Material and device oriented high power, high frequency electronics ???/ HEMT 5 W, 10 GHz, - goals;

- GEC, Thomson-CSF
- Siemens
- Thomas Swan, Univ. Nottingham, Univ. of Gent

Started this year

Total budget 3-4 million Euro per project per year

Results:

Materials

- P doping 5 x10^{17} (Valbonne, 3 MBE, 5 MOCVD), conductivity 1 ohm-cm
- InGaN bulk FWHM 50 meV at 10 K, 400 nm, Stokes shift < 30 meV
- InGaN QW FWHM 35 meV at 10 K
- GaN/AlGaN QW FWHM 15 meV at 10 K

ELOG-HVPE

- GaN on Si (111) quality similar to sapphire

- GaN/AlGaN quantum dots: intense, large Stark effect (red PL)

Process:

- n-contact 10^{-6} ohm cm^2
- p-contact 10^{-3} ohm cm^2
- Etching: vertical facets by CAIBE and optically pumped laser

LEDs

- <-/1 mW ???
- GWHM 15 nm at 235 nm
- High turn-on voltage

Laser

- Optical pumped

FETs

MESFETs

2 micron gate, breakdown ~ 300 V, for a 0.3 micron gate, f_t = 12 GHz f_{max} = 25 max I_{dss} = 330 mA/mm

Photodetectors

Photoconductive

3000 A/W

UV-visible 10^4 to 10^7

1/f noise is large

Schottky photovoltaic on GaN

n_s response

10^{-8} A reverse current

Johnson noise low bias

$r_o A$ 10^8 W cm^2

Schottky photovoltaic on AlGaN

Cutoff at 320 nm

4-year delay compared to US

Materials are catching up. Devices behind, except for photodetectors (state of the art)

DIAMOND RESEARCH IN FRANCE

Drs. M. Deneville and P. H. Bergonzo discussed diamond research in France.

Applications

- window (microwave and laser)

- pressure sensors and SAW
- UV,V, X, and particle detectors

Coating

- Electrochemical reactions

p-n junction 900°C

Schottky 700°C

MESFET 500 °C

Groups in France

Window (microwave and laser)

Thomson, CEA in Bordeaux

LPL Paris

SAW (with AlN), Univ. Lens

Pressure sensors and SAW

Univ. of Nancy

UV,V, X, and particle detectors

Coating

University of Orleans

Electrochemical reactions:

LCTMR, CNRS

Basic research

Reactor modeling

Large monocrystalline substrates

Physical and electrical properties

Device

Schottky

MESFET

Surface studies

At LETI, they have grown 0.5 cm 250 micron diamond crystal film.

Site: **Russian GaN-based Research**
Virtual Site Report

Date: 12 June 1999

Report Author: M. Shur

There is now a considerable and growing interest in GaN research in Russia. Fig. 2 shows the number of GaN-related papers at the All-Russian Conference on Nitrides of Gallium, Indium, and Aluminum: structures and devices—altogether, reaching approximately 90 participants in 1999.

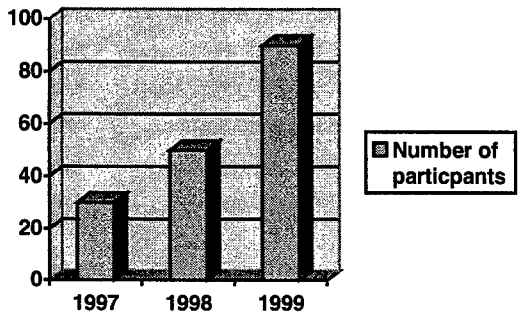

Fig. 2.

The Russian universities and research organizations involved include:

- A.F. Ioffe Institute of Physics and Technology of the Russian Academy of Sciences
- Lomonosov Moscow State University
- Lebedev Institute of Physics and Technology of the Russian Academy of Sciences
- GIREDMET
- NPVF "Svecha"
- Crystal Growth Research Center in St. Petersburg
- ELMA-MALAKHIT in Zelenograd
- Moscow Institute of Electronic Technology
- Institute of Physics and Chemistry of the Russian Academy of Sciences
- Moscow State Institute of Steel and Alloys
- St. Petersburg State Technical University
- Institute of Physical Chemistry of the Russian Academy of Sciences
- Institute of Crystallography of the Russian Academy of Sciences
- Institute of Nuclear Physics
- Sigma Plus in Moscow
- Baikov Institute of Metallurgy of the Russian Academy of Sciences
- "Polyprovodnikovye Pribory" in St. Petersburg
- "SAPHFIR" in Moscow
- Institute of Chemistry of Silicates in St. Petersburg
- Vologda State Technical University

- Udmurtsky State Technical University
- VNII of Optical and Physical Measurements in Moscow
- OPTEL in Moscow
- St. Petersburg Institute of Technology
- Frumkin Institute of Electrochemistry
- NITI "TEKHNOMSH" in Moscow
- MAR State Technical University in Iohskar-Ola.

INTERNATIONAL COLLABORATIONS

Russian international collaborations include:

- TDI, Inc. in Gaithersburg, Maryland
- Howard University in Washington, DC
- Rensselaer Polytechnic Institute in Troy, NY
- Naval Research Laboratory in Washington, DC
- University of Ulm in Germany
- University of Karlsruhe in Germany
- Technical University of Berlin in Germany

RESEARCH AREAS

The largest effort is at A.F. Ioffe Institute. The areas of research and development include:

- crystal growth (with emphasis on HVPE, MOCVD, MBE, and sputtering)
- fabrication and characterization of ion-implanted p-n junctions
- the development of production equipment (at ELMA-MALAKHIT)
- research on ternary and quaternary AlGaInAs solid state solutions
- investigations of basic materials properties
- growth and characterization of wurtzite and cubic BN
- research on GaN and InGaN based LEDs and optically pumped lasers
- white LEDs
- research on doping of GaN
- the development of GaN/GaP and GaN/Si heterostructures
- studies of piezoelectric properties
- the research on defects, studies of mechanical properties
- cathodoluminescence studies
- Raman and lattice dynamics studies
- applications of blue, green, orange, and red LEDs for materials testing
- studies of acoustic surface waves

APPLICATIONS

The Russian company, SVECHA, has taken a lead in production of traffic signals using green GaN LEDs. They had the first installation of such traffic signals in Moscow in 1997. They are involved in the development of LED-based lighting for airplanes, of LED-based navigation lights, and lighting sources for

other applications. NII OPTEL is using imported green InGaN LEDs for river navigation lights. One blue LED is visible for two kilometers.

CONCLUSION

The research level on devices is relatively small compared to the United States. Only two teams have demonstrated p-type GaN (Alferov's team by MOCVD and Dmitriev's team by HVPE). However, several excellent groups are involved in basic GaN research. Even at this level, there is a company pursuing practical applications (traffic lights) using imported GaN LEDs.

Site: **Siemens-Erlangen**
Paul-Gossen Str. 100
D-91052 Erlangen GERMANY

Date Visited: 8 June 1999

TTEC Attendees: T.P. Chow, (report author), V. Dmitriev, M. Spencer

Hosts: Dr. Dieter Stephani
Dr. Roland Rupp
Dr. Mitlener
Dr. Peter Friedrichs

INTRODUCTION

Siemens is an international industrial company that has major businesses in power generation, transmission and power electronics. There are significant technology development efforts in its research and development laboratory in Erlangen, involving SiC materials growth and processing, device design, fabrication and characterization and prototype device/circuit demonstrations. This group is expected to remain with Siemens after the Infineon spinoff, though some SiC team members have left to join the new company.

Dr. Stephani, who is the project leader, gave an overview of their SiC device program, emphasizing exclusively power electronics applications. The focus of their effort is to replace silicon power devices where SiC can offer better performance, including large-volume applications. There are about 20 people in their group, including epitaxial growth, device design, fabrication and characterization. Over the last few years, the researchers at Siemens have demonstrated many high-voltage power switching devices. They are clearly one of the top SiC device research groups in the world. The devices they have reported include:

- 600-1,200 V Schottky rectifiers
- 3,000 V (soon to be 5-6 kV) pin junction rectifiers in 4 H-SiC
- 1,800 V power DMOSFETs in 6 H-SiC
- high voltage JFET in 4 H-SiC (with a Si MOSFET gate driver)
- first 15 R-SiC MOSFET

They all have very impressive performance characteristics, such as specific on-resistance and short circuit capabilities. For example, 1,200 V 4 H-SiC Schottky diodes have a specific on-resistance of 2 $m\Omega cm^2$. Their vertical DMOSFETs have the lowest specific on-resistance of 25 $m\Omega cm^2$ for an 1,800 V inversion mode SiC MOSFET. Actually, panelists were shown a hybrid package that incorporates the SiC JFEET and Si power MOSFET driver. Also, they have demonstrated the advantage of using 15 R polytype for MOSFET, instead of 4 H polytype (Schorner et al. 1999). The reason for this is that there apparently are few localized trap states near the conduction band edge in 15 R-SiC and, consequently, a much higher inversion electron mobility can be achieved than in 4 H-SiC (33 vs. 0.4 $cm^2/V\text{-}s$). Besides, while 6 H-SiC also has similar inversion electron mobility values, the anistropy in bulk mobilities is much less in 15 R-SiC than in 6 H-SiC. Nevertheless, there is no 15 R-SiC commercial wafer supplier at present.

In summary, the SiC research performed in the Siemens group is extremely impressive due to its breadth and outstanding performance characteristics.

REFERENCES

Schorner, R., P. Friedrichs, D. Peters, and D. Stephani. 1999. *IEEE Electron Device Letters*, vol. 20, pp. 241-244.

University of Erlangen-Nurnberg
Marenstrasse 7/ Institute Bld. V, Rm 368
D 91058 Erlangen, Germany
Tel: +49 9131 852 7634 or +49-91 31 852 8426

Date Visited: 9 June 1999

TTEC Attendees M.G. Spencer (report author), T.P. Chow, V. Dmitriev

Hosts Dr. Dieter Hoffmann, Electronic Engineering Materials Group
Prof. Gerhardt Pensel, Dept. of Physics
Prof. Winnacker, Dept. of Physics
Dr. Eckstein, SiCrystal

INTRODUCTION

At the University of Erlangen the panel visited two separate departments. The first department was the Department of Materials Science and Engineering. This department forms part of the Technische Fakultat (Faculty of Engineering Sciences). The second group that we visited was a part of the traditional physics department of the university. Both groups were extremely active in materials growth and characterization of SiC.

DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

In the Dept. of Materials Science and Engineering most of the work in wide bandgap technology is done in the Electronic Engineering Materials Group. Professor Winnacker gave an overview of the efforts in that group. Major topics under investigation were:

- bulk crystal growth of GaAs, InP and SiC
- modeling of the growth process
- development of phosphorus for blue light conversion

Dr. Dieter Hoffmann gave the panelists a detailed presentation on the research for the bulk growth of SiC. Most of this effort is supported by a research grant from Bavaria. This research grant, ~ $1 million/year, has also supported SiCrystal in their effort to commercialize bulk crystal growth in Germany.

Dr. Eckstein of SiCrystal was present and gave a brief overview of the progress and direction of the company. During the talk by Dr. Hoffman he described efforts to understand the basic thermodynamics of bulk crystal growth and defect formation. Of special interest, micropipes and their formation and research results on formation mechanisms were presented. These topics are investigated experimentally in a sublimation reactor, which is currently growing 1.5" SiC boules. Theoretical modeling of heat transfer is closely linked to this effort.

Another technique for the production of bulk SiC is Liquid Phase Growth. The group in Erlangen and another group in Russia are unique in their efforts to investigate the possibility of large area growth of SiC by this technique. The Erlangen group is producing SiC at 2100°C and 150 torr of pressure. Under these conditions the growth rate is 0.6 mm/hr. The potential advantages of this technique include improved mass transfer and easier scaling.

Dr. Eckstein described SiCrystal, which was formed in August 1996. They are currently producing SiC principally for use in LED technology. This material is 2" in diameter. The company estimates that 90% of their market is based on nitride technology. They expect this number to decrease to 50% when manufacture of SiC based devices commences. When the demand for SiC material increases they will start production of 4" SiC.

DEPARTMENT OF PHYSICS

In the afternoon panelists met with Professor Pensel and Professor Helbig of the Dept. of Physics. In the Department of Physics there is significant activity on crystal growth and characterization. The specific topics were:

- bulk crystal growth—zero micropipes (6 H), 15 R polytype (in collaboration with Kyoto University)
- ion implantation—intrinsic defects, effects of non stoichiometry, diffusion (Boron)
- reconstruction of SiC surface
- MOS interface state density studies—admittance and constant capacitance DLTS

Most of the work is funded by the German Science Foundation. There is, however, no national program on SiC. The group does participate in a European program, which funds some of the ion implantation work.

In informal discussions with Professors Pensel and Helbig, they both agreed that 15 R had great potential for MOS applications. They indicated that in collaboration with Prof. Matsunami of Kyoto they had obtained inversion layer mobility of 70 cm^2/V-sec.

Site:	**University of Linkoping** **Dept. of Physics and Measurement Technology** **IFM-FOA S-581 83 Linkoping, Sweden** **Tel 46 13 8 1765 or 46 13 28 1797**
Date Visited:	10 June 1999
TTEC Attendees	M.G. Spencer (report author), T.P. Chow, V. Dmitriev
Hosts	Professor Bo Monemare Professor Erik Janzen

INTRODUCTION

In Linkoping the panel visited the Dept. of Physics and Measurement Technology. This organization employs over 350 people, including approximately 115 graduate students (who are government employees). The concentration in solid state physics and materials studies is broken down into several topics:

- materials physics—125 people
- thin film physics
- chemical physics
- surface physics—this where the sensor work is taking place
- theory group
- device modeling
- biology
- chemistry

The materials under study, ordered by research support, are:

- SiC—good support from several sources
- III/V nitrides /II-VI –III/ V nitride do not currently have local industrial support ???
- III/V quantum structures
- silicon and SiGe

In general the group at Linkoping is interested in the studying the physics of the material topics are: ???

- Electronic Properties of Quantum Structures
- Electronic Properties of Defects
- Properties and Characterization of Epi and Bulk Material
- Bulk and Surface Band Structures

SIC ACTIVITIES

Professor Janzen described the SiC activities, which involve two professors, 20 seniors???, 7 PhD students and 6 technical support staff. These activities receive funding from several sources:

SiCep

This is a national program on SiC which provides a total of 18 million SEK of funding for SiC per year. Of that total Linkoping receives 8 million SEK.

Jesica

Joint European SiC Activity: funding from this program totals one million SEK/year. This money is split with Okmetic, a wafer growth startup company.

Okmetic

A wafer growth startup company which is partnering with Grenoble to grow semi-insulating and n+ SiC.

ABB

Linkoping is in direct partnership with ABB (a major multi-national company) for development of materials growth processing and the basic understanding necessary to fabricate high voltage rectifiers.

Other

Linkoping receives about 3 million SEK from the Swedish Engineering Research Council (TFR), Science Research Council (NFR), and the Defense Department (FOA).

Looking in more detail at SiCep, the work is split as follows:

- technology (bulk growth, epi and defects)— 8 million SEK, Linkoping
- devices (power devices, high voltage diodes, high voltage switches)—KTH (KTH is also known as the Royal Institute)
- ion implantation, contacts—KTH
- dielectrics—Chambers

The SiCep program is funded by a private foundation (strategic research foundation???) with government interest or direction; the funds are only for universities. A separate foundation funds equipment.

The emphasis in Janzen's group is to provide a technology for high voltage devices. To that end they have developed high temperature epi for SiC and are using a variant of this technology for bulk crystal growth. The results for the high temperature epi are impressive. They have obtained a background doping of 2-4 x $10^{14}cm^{-3}$ with a growth rate of 40 microns per hour. For the HTCVD (as applied to bulk growth) they have achieved a growth rate 0.5 - 0.8 mm/hr.

III/V Nitrides

Professor Bo Monemare discussed the nitride efforts. The goal of the work is to measure the basic materials parameters. Professor Monemare feels that because the quality of the material is currently so poor all the basic measurements are suspect and need a second look. In an effort to obtain high quality material the group has decided to develop HVPE. The specific topics mentioned were:

- homo epi—HVPE
- thick epi—HVPE
- bulk GaN—high speed HVPE
- physics of AlGaN/GaN and GaN/InGaN multi quantum wells

FACILITIES TOUR

Panelists were shown the facilities at Linkoping. All the growth equipment was designed in collaboration with Epigress (a local equipment supplier). After development at Linkoping this equipment is available on the open market. The Linkoping facilities were about three years old and very impressive. All the equipment was "state of the art" and often brand new. The panel was told that the equipment was purchased with funds from a private foundation as indicated earlier in the report.

Site: **University of Ulm**
Albert-Einstein-Allee 45
D-89081 Ulm, Germany
Tel: +49-73150-26454-26050
Fax: +49-73150-26454-26049

Date Visited: 8 June 1999

TTEC Attendees: J. Zavada (report author), S. DenBaars, M. Shur, U. Varshney, G. White

Hosts: Dr. Markus Kamp
Prof. Erhard Kohn
Prof. Hermann Schumacher

INTRODUCTION

At the University of Ulm, the panel visited the Department of Electron Devices and Circuits and the Department of Optoelectronics, each of which is headed by two professors.

Prof. Kohn, who is with the Department of Electronics and Circuits, gave the panel an overview of the University of Ulm. There are approximately 5,000 students at the university, which is only 30 years old. There are nearly 300 students in the Electrical Engineering Department. Only five students are involved with GaN research at present. However, there is a very active program in GaN materials growth, optical and electrical characterization, and device fabrication and testing.

DEPARTMENT OF OPTOELECTRONICS

Professors K. Ebeling and P. Unger are the two professors in charge of Optoelectronics. Neither one was at the university during the panel's visit. Dr. Kamp gave the panel an overview of the research activities in this department. At present, the main areas of investigation are:

- vertical cavity surface emitting lasers (VCSELs) having low threshold currents
- optical interconnects for high data rate transmission
- high power laser diodes based on InAlGaAs compounds
- high brightness light emitting diodes (LEDs), which encompasses the GaN research

Dr. Kamp gave panelists a detailed presentation on the research on GaN LEDs and laser diodes. Most of this effort is supported by a research grant from state government and includes GaN growth, optical characterization, device fabrication and testing.

Initially, Dr. Kamp's group was using gas source molecular beam epitaxy (MBE) to synthesize the GaN layers. However, due to the unimpressive device results with this method, the group is now using chemical vapor deposition (CVD) to grow the GaN layers. Much improved optoelectronics devices have resulted using this approach.

The group has grown GaN LED structures on sapphire substrates and on GaN bulk crystals obtained from UNIPRESS in Poland. In general, GaN homoepitaxy leads to much improved optical characteristics. Photoluminescence (PL) taken at 20 K shows all of the relevant exitonic features and linewidths as narrow as 1 meV. The LEDs grown on GaN substrates are nearly twice as bright as the ones grown on sapphire. These results are similar to those found with LEDs grown on GaN lateral overgrowth epitaxy (LEO) substrates. In spite of the large reduction of dislocation defects in the GaN films, the LEDs only show a two-fold improvement in brightness.

Dr. Kamp also described efforts to develop GaN waveguide structures. The intent is to design and fabricate suitable laser structures and to produce a room temperature, cw laser.

DEPARTMENT OF ELECTRON DEVICES AND CIRCUITS

Prof. E. Kohn and H. Schumacher are the two professors in charge of Electron Devices and Circuits. The main research activities in this department relating to GaN are electronic device modeling and characterization.

Prof. Hermann Schumacher's group is mainly involved in the modeling and device characterization of SiGe heterostructure bipolar transistors. This research is being done in close collaboration with Temic Semiconductors GmbH, which is a spin-off company of Siemens AG.

Prof. Schumacher gave a presentation on the advantages of SiGe devices for telecommunications. He described his research in exploring the performance potential of SiGe integrated circuit technology, at frequencies above 3 GHz, for front-end receivers.

Prof. Kohn gave the panel a detailed presentation on his research concerning electrical characterization of GaN-based devices. His group has been involved in the small and large signal dispersion analysis of AlGaN/GaN MODFETs (modulation doped field effect transistors) and AlN/n-GaN FETs (field effect transistors). The device structures were grown by SVT Associates, in the United States, and processed into devices at DaimlerChrysler in Ulm. Their results indicate that the I-V characteristics of these devices change with heat treatment. A degradation of the I-V curves occurs after treatment at 600°C. These effects may be due to a materials problem (defects in the buffer layer) or to changes in the electrical contacts (surface charge).

Later Prof. Schumacher gave a tour of his labs for device characterization. These labs have also been used for the signal dispersion analysis of AlGaN/GaN MODFETs done by Prof. Kohn's group. Some of the research concerning electrical characterization of GaN-based devices has not as yet been published.

CLEAN ROOM FACILITIES

Later in the day, Dr. Kamp took the panel on a tour of the clean room facilities in the microelectronics technology center at the University. There is approximately 600 sq. meters of clean room space; some areas are class 100 and others are class 10. All the growth equipment was located in the center. There are a total of seven growth reactors for synthesis of different compound semiconductors. Currently, no synthesis of Si is being undertaken.

At present two Aixtron reactors are being used for GaN thin film growth, one for CVD and the other for hydride vapor phase epitaxy. Three other reactors are being used for growth of InAlGaAs compounds. One reactor is not presently in service.

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14. ABSTRACT

This final report of ITRI's panel of experts consists of an executive summary, an introductory chapter, and six chapters by panelists on various aspects of wide bandgap electronics. The report also contains site reports for the various companies, labs, universities, and government offices that the panel visited in Europe. Comparisons are made between developments in Europe and the United States.

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Technology Transfer (TTEC) Division

The Technology Transfer (TTEC) Division of Loyola College in Maryland is a division of Loyola's International Technology Research Institute (ITRI). It was originally established in April 1993 with funding from the U.S. Department of Transportation to conduct a series of assessments of foreign transportation technology. Under DoT funding, eight delegations of U.S. experts visited developed countries in Europe and the Pacific Rim to gather information on technological innovations and research advancements in the transportation area. In 1996 TTEC broadened its scope to include a variety of foreign technology transfer services.

The Department of Transportation developed the International Technology Scanning Program in response to Section 6003 of the Intermodal Surface Transportation Efficiency Act (ISTEA) of 1991. Under this program, TTEC conducted a number of "scanning" tours for DoT. As applied in this program, the term "scanning" referred to the approach generally known as benchmarking.

TTEC assembled delegations of U.S. professionals, composed of representatives from Federal, State, and city planning levels, from academia, and from the private sector. They identified foreign transportation experts in governments, universities, and the private sector, established contact, coordinated meetings, and provided logistical arrangements. Upon completion of the study tour, a member of the delegation compiled the information collected into a report of results. TTEC also disseminated the results to the highway community through workshops and technical presentations.

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