October 28 - November 2, 2001
Tsukuba International Congress Center

Technical Digest

ICSCRM2001
TSUKUBA

International Conference on Silicon Carbide and Related Materials 2001

20020405 052



TSUKUBA JAPAN

ICSCRM2001

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 2001	October 28 – November 2, 2001 Final

4. TITLE AND SUBTITLE
International Conference on Silicon Carbide and Related Materials 2001 (9th) (ICSCRM2001) Held in Tsukuba, Japan on October 28-November 2, 2001. Technical Digest.

5. FUNDING NUMBERS

6. AUTHOR(S)

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
The Japan Society of Applied Physics

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Office of Naval Research,
European Office
PSC 802 Box 39
FPO AE 09499-0039

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
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12b. DISTRIBUTION CODE

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12. ABSTRACT (Maximum 200 words)
The Technical Digest contains the abstracts of 506 papers presented at the International Conference on Silicon Carbide and Related Materials 2001 held on October 28-November 2 in Tsukuba, Japan. Topics include crystal growth, characterization, device process, and device modeling of wide bandgap materials such as silicon carbide, III-V nitrides and carbon nanotube. Because of recent progress in device application, a special symposium on "Device and Peripheral Technology" was

13. SUBJECT TERMS
ONRIFO, Foreign reports

15. NUMBER OF PAGES

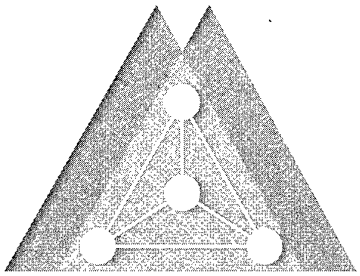
16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18
298-102

TECHNICAL DIGEST



International Conference on Silicon Carbide and Related Materials 2001

—ICSCRM2001—

October 28–November 2, 2001
Tsukuba International Congress Center
(Epochal Tsukuba, Ibaraki, Japan)

Sponsored by
The Japan Society of Applied Physics

In Cooperation with
Association for Promotion of Electrical, Electronic and Information Engineering
The Ceramics Society of Japan
The Institute of Electronics, Information and Communication Engineers
The Institute of Electrical Engineers of Japan
Japanese Association for Crystal Growth
Science Academy of Tsukuba
The Surface Science Society of Japan
The Vacuum Society of Japan

AQ F02-07-1184

Message from Organizing Committee Chairperson



On behalf of the Conference Organizing Committee, it is my great pleasure to welcome you to the International Conference on Silicon Carbide and Related Materials 2001. Following the eight previous conferences in the USA, Japan, and Sweden, this the 9th meeting will be the first conference of the 21st century.

This conference series started in 1987 in Washington D.C. with the following four conferences held at Santa Clara and Washington D.C., alternately. At the 5th conference held in Washington D.C. in 1993, it was decided that the conferences will rotate every two years between the USA, Japan and Europe. In 1995, the first conference held outside the USA was held in Kyoto, Japan. This is therefore the second opportunity to host the conference in Japan.

For this conference, we have arranged to have 20 invited talks focused on different aspects of SiC, nitrides and related materials, providing a survey of the present status of various topics of particular current interest. We have put emphasis on clarifying the problems to be solved in achieving SiC devices. With this in mind we have decided to hold a special symposium on "Device and Peripheral Technology" during the conference.

More than 400 contributed papers will be presented as oral and poster sessions. They are intended to cover all aspects of SiC and related materials, e.g., crystal growth, characterization, device processing, and device performance and applications. I sincerely hope that all of you will participate in a lively fashion during the five days of the conference and further your knowledge on wide bandgap semiconductors.

This conference is sponsored by the Japan Society of Applied Physics and in cooperation with several institutes and societies. The Science and Technology Promotion Foundation of Ibaraki as well as more than 40 other foundations and private companies have contributed to the conference financially. I would like to express my deepest appreciation to these organizations and companies.

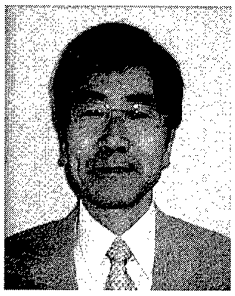
Tsukuba is located about 60 km northeast of Tokyo, and 40 km northwest of Narita New Tokyo International Airport. Tsukuba was planned and constructed about 30 years ago for the promotion of science and education. There are several universities and more than 200 research institutes affiliated with both the public and private sectors. I am sure you will enjoy your stay in this modern Japanese city surrounded by some beautiful natural scenery including Mt. Tsukuba, the symbol of the conference.

It will be our greatest joy if all participants at the conference take home valuable and worthwhile experiences.



Sadafumi Yoshida
Chairperson
Conference Organizing Committee
(October, 2001)

Preface



This technical digest contains the abstracts of the papers, including 20 invited papers, 416 contributed papers including 70 Late News papers, which will be presented at the International Conference on Silicon Carbide and Related Materials-2001 held on October 28–November 2 in Tsukuba, Japan.

The Program Committee has received a large number of abstracts submitted for the conference from 17 different countries of all over the world. The abstracts submitted cover crystal growth, characterization, device process, and device modeling of wide bandgap materials such as silicon carbide, III–V nitrides and carbon nanotube. Most of the sessions are carried out simultaneously, as the case of the last conference. Considering recent progress in device application, a special symposium entitled "Device and Peripheral Technology" is planned. What's more, in addition, three rump sessions topics from basic physics to practical SiC devices are also scheduled. The Program Committee has invited 20 key researchers in different aspects of these fields to help us gain a closer understanding of state-of-the-art science and engineering in these fields. The sessions with invited speakers are scheduled not to overlap with each other so that all can be attended.

On behalf of the Program Committee, I would like to express a warm welcome to you all. I sincerely hope that those participating in the conference will benefit from their time at the conference and that by combining our shared knowledge we can make further progress in the fields of wide bandgap science and technology. It would be the greatest of pleasures, if this conference is a worthwhile experience for all those concerned.

Shigehiro Nishino

Shigehiro Nishino
Chairperson
Program Committee
(October, 2001)

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Acknowledgements

The Conference Organizers wish to acknowledge the financial support from the following organizations and companies.

The Science and Technology Promotion Foundation of Ibaraki

The Commemorative Association for the Japan World Exposition (1970)
Foundation for Promotion of Material Science and Technology of Japan
Kansai Research Foundation for Technology Promotion
The Murata Science Foundation
The Ogasawara Foundation for the Promotion of Science & Engineering
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We will greatly appreciate AIXITRON AG/EPIGRESS AB for the sponsorship of welcome reception and congress bags, and SiCrystal AG/Ceramic Forum Co., Ltd., SiXON Ltd./Mitsubishi Corporation, Universal Systems Co., Ltd. for providing coffee break service.

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ALTEDEC, Japan

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[1]Linköping University, Sweden; [2]University of Cambridge, Great Britan; [3]ABB Corporate Research, Sweden; [4]Helsinki University of Technology, Finland

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[1]National Institute of Advanced Industrial Science and Technology, Japan; [2]R&D Association for Future Electron Devices, Japan; [3]Ultra-Low-Loss Power Device Technology Research Body, Japan

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[1]National Institute of Advanced Industrial Science and Technology, Japan; [2]R&D Association for Future Electron Devices, Japan; [3]Ultra-Low-Loss Power Device Technology Research Body, Japan

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[1]Politehnica University, Romania;
[2]Microtehnology Institute, Romania;
[3]Centro National de Microelectrnica, Spain;
[4]Cambridge University, UK

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[1]R&D Association for Future Electron Devices, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan; [3]Ultra-Low-Loss Power Device Technology Research Body, Japan

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[1]Linköping University, Sweden; [2]Volvo TU, Sweden; [3]ACREO AB, Sweden; [4]Volvo PV AB, Sweden; [5]Applied Sensor AB, Sweden; [6]fLVKARLEBY, Sweden; [7]Ford Motor Company, USA

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[1]Linköping University, Sweden; [2]Okmetic AB, Sweden

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[1]Toyota Central R&D Labs, Inc., Japan; [2]DENSO Corporation, Japan

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[1]Friedrich-Schiller-Universität Jena, Germany; [2]Institute of Catalysis, Russia; [3]Bell Laboratories, USA; [4]University of Pittsburgh, USA

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[1]Linköping University, Sweden; [2]Helsinki University, Finland

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[1]CRHEA, France; [2]NOVASiC, France; [3]UM2-CNRS, France; [4]Russian Accademy Sciences, Russia

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[1]Mitsubishi Electric Corporation, Japan; [2]Ultra-Low-Loss Power Device Technology Research Body, Japan

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[1]Alabama A&M University, USA; [2]Oak Ridge National Laboratory, USA; [3]NASA Glenn Research Center, USA

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[1]Université Claude Bernard Lyon 1, France; [2]Novasic, France

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[1]NASA Glenn Research Center, USA; [2]State University of New York at Stony Brook, USA

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[1]National Institute of Advanced Industrial Science and Technology, Japan; [2]Saitama University, Japan

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[1]Budapest University of Science and Technology, Hungary; [2]Research Institute for Technical Physics and Materials Science of the H.A.S., Hungary

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[1]University of North Carolina, USA; [2]University of Illinois, USA

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[1]DSM-DRECAM-SPCSI-SIMA, France; [2]Bell Labs, USA; [3]Academia Sinica, Taiwan; [4]LPPM-CNRS, France; [5]THALES, France; [6]STMicroelectoronics, France

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[1]University of Erlangen-Nürnberg, Germany; [2]Fritz-Haber-Institute, Germany; [3]La Trobe University, Australia

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[1]Kyoto Institute of Technology, Japan; [2]Indian Institute of Technology, India

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[1]Carnegie Mellon University, USA; [2]Sterling Semiconductors, Inc., USA

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[1]Linköping University, Sweden; [2]Royal Institute of Technology, Sweden

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[1]Naval Research Laboratory, USA; [2]Cree Inc., USA

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[1]Yale University, USA; [2]Southern Connecticut State University, USA; [3]United Technologies, USA

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[1]Chalmers University of Technology, Sweden; [2]National Academy of Sciences of Ukraine, Ukraine

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[1]Saitama University, Japan; [2]JAERI, Japan; [3]National Institute of Advanced Industrial Science and Technology, Japan

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[1]Pohang University of Science and Engineering (POSTECH), Korea; [2]Korea Electrotechnology Research Institute (KERI), Korea; [3]Chonnam National University, Korea

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[1]KTH, Royal Institute of Technology, Sweden; [2]Lund University, Sweden; [3]Ericsson Microelectronics AB, Sweden

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[1]NASA Glenn Research Center, USA; [2]Ohio Aerospace Institute, USA

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[1]Friedrich-Schiller-Universität Jena, Germany; [2]Institute of Catalysis, Russia; [3]Bell Laboratories, USA

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[1]Ioffe Physical-Technical Institute, Russia; [2]Crystal Growth Research Center, Russia

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[1]Sun Moon University, Korea; [2]Soonchunhyang University, Korea

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[1]Bulgarian Academy of Sciences, Bulgaria; [2]Linköping University, Sweden

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[1]Mississippi State University, USA; [2]Wright-Patterson Air Force Base, USA

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[1]Rutgers University, USA; [2]United Silicon Carbide, Inc, USA

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[1]University of California at UCI, USA; [2]LG Electronics Inst. of Tech., Korea; [3]Myong Ji University, Korea

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[1]INSA Lyon, France; [2]Institut Franco-Allemandde Recherche de St. Louis, France

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[1]Cree Inc., USA; [2]Ioffe Physico-Technical Institute, Russia

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[1]Ioffe Physical-Technical Institute, Russia; [2]ISP, Ukraine; [3]INSA de Lyon, France

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[1]Rutgers University, USA; [2]United Silicon Carbide, Inc, USA

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[1]Rensselaer Polytechnic Institute, USA; [2]Cree Inc., USA

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[1]Centro Nacional de Microelectronica, Spain; [2]Istituto LAMEL, Italy; [3]Instituto de Ciencias de Materiales, Spain

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S. C. Kang, M. W. Shin
Myong-Ji University, Korea

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H. Miyamoto
NEC Corp., Japan

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T. Ide[1], M. Shimizu[2,4], A. Suzuki[3], X. Q. Shen[2,4], H. Okumura[2,4], T. Nemoto[1]
[1]Graduated School of Meiji University, Japan; [2]National Institute of Advance Industrial Science and Technology, Japan; [3]Tokai University, Japan; [4]Ultra-Low-Loss Power Device Technology Research Body, Japan

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[1]Oki Electric Industry Co., Ltd., Japan; [2]Nagoya Institute of Technology, Japan; [3]Ultra-Low-Loss Power Device Technology Research Body, Japan

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[1]University of Florida, USA; [2]Ioffe Physical-Technical Institute, Russia; [3]TDI, Inc., USA

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S. Yoshida, H. Ishi, J. Li
The Furukawa Electric Co., Ltd., Japan

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M. Pons[1], J. Meziere[1], J. Dedulle[1], S. Wan Tang Kuan[2], E. Blanquet[1], P. Ferret[2], L. Di Coccio[2], T. Billon[2], R. Madar[1]
[1]INP Grenoble, France; [2]CEA/LETI Grenoble, France

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Linköping University, Sweden

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A. Schöner[1], A. Konstantinov[1], S. Karlsson[2], R. Berge[3]
[1]ACREO AB, Sweden; [2]ADC, Sweden; [3]Epigress AB, Sweden

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Central Research Institute of Electric Power Industry, Japan

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A. O. Konstantinov, P. Ericsson, C. Harris
ACREO AB, Sweden

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[1]LPCS, France; [2]THALES, France

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Rockwell Science Center, USA

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[1]INSA Lyon, France; [2]THALES, France

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Cree Inc., USA

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[1]University of Erlangen-Nürnberg, Germany; [2]Institut für Kristallzüchtung, Germany

—Thursday, November 1—

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Y. Okui[1], C. Jacob[2], S. Ohshima[1], S. Nishino[1]
[1]Kyoto Institute of Technology, Japan; [2]Indian Institute of Technology, India

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P. G. Neudeck[1], J. A. Powell[1], A. J. Trunek[2]
[1]NASA Glenn Research Center, USA; [2]Ohio Aerospace Institute, USA

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The Furukawa Electric Co., Ltd., Japan

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[1]Institute of Space and Astronautical Science, Japan; [2]Science University of Tokyo, Japan

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[1]University of Tokyo, Japan; [2]Kyoto Institute of Technology, Japan; [3]National Institute of Advanced Industrial Science and Technology, Japan

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[1]INSA-Lyon, France; [2]Campus Universidad de Barcelona, Spain; [3]Ferraz Shawmut, France

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[1]Hosiden Corporation, Japan; [2]Osaka Prefecture University, Japan

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State Electrotechnical University of St.-Petersburg (LETI), Russia

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[1]Linköping University, Sweden; [2]Okmetic AB, Sweden

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S. E. Saddow[1], T. Elkington[2], M. C. D. Smith[3]
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[1]Kyoto Institute of Technology, Japan; [2]SiXon Ltd., Japan

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T. Aoyama[1], Y. Hisada[2], S. Mukainakano[2], A. Ichimiya[1]
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Hosei University, Japan

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[1]University of Newcastle upon Tyne, UK; [2]Ioffe Institute, Russia

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S. Mitra[1], M. V. Rao[1], N. Papanicolaou[2], K. Jones[3]
[1]George Mason University, USA; [2]Naval Research Laboratory, USA; [3]Army Research Laboratory, USA

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[1]Saitama University, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan; [3]R&D Association for Future Electron Devices, Japan; [4]Ultra-Low-Loss Power Device Technology Research Body, Japan

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—Thursday, November 1—

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MoA2 Plenary Session

MoA2-1
(Invited)

Silicon Carbide Technology in New Era

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Owing to the significant progress in the growth of large and high-quality silicon carbide (SiC) bulk crystals without polytype mixing by sublimation above 2000°C and high-quality epitaxial layers on off-axis SiC(0001) at rather low temperatures around 1500°C, various types of SiC devices have been reported. Nowadays, 3-inch wafers of 6H- and 4H-SiC are commercially available, and Schottky diodes using the epitaxial layers have been delivered in the real semiconductor world.

Although many outstanding potentials of SiC have been demonstrated in various prototype devices projected for high-power, high-frequency, and high-temperature electronic devices including Schottky diodes, there are still many issues in technology for advanced SiC electronics. At the beginning of new era, a review on present-day SiC technology is necessary. Problems in bulk crystal growth, epitaxial growth, processes, and devices are briefly discussed.

Among them, the author raises the low-channel mobility in 4H-SiC MOSFETs, and introduces a trial to improve it. 4H-SiC has been regarded as the most promising polytype owing to its higher bulk mobility and smaller anisotropy than 6H-SiC. However, inversion-type MOSFETs fabricated on off-axis 4H-SiC(0001) wafers generally show an unacceptably low channel mobility, typically below $10cm^2/Vs$, which severely increases the on-resistance of SiC power MOSFETs. There have been several trials to improve the low channel mobility, either by annealing after device fabrication or to use a buried channel. Although the values of channel mobility have been improved actually, there would be barriers to use such processes or structures.

The author's group has proposed to use (11-20) at the last ICSCRM. A remarkable improvement in the values of mobility was shown together with the negative temperature dependence. The author reviews successful homoepitaxy on (11-20) and the inversion-type planar MOSFET performance. The origin of the high channel mobility on (11-20) substrates, which has been made clear after the last ICSCRM, is discussed based on the detailed analysis. In addition, other superior properties of (11-20) for the power devices will be reported.

Characterization and Defects in SiC

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SiC is a material of increasing interest for high power and high frequency applications. The material quality including understanding and control of defects is currently a limiting factor for many of the device applications. We have during the last years combined growth development of both epitaxial layers and bulk substrates, with a strong activity on defects and characterization. In this paper we will present suitable characterization techniques and recent results regarding important defects in epitaxial and semi-insulating bulk 4H SiC. This will include point and extended defects, defects created by irradiation techniques and finally defects created during processing or device operation.

One of the most important and most studied defects in SiC is the so called D1. This is an intrinsic defect always present after different particle irradiation and are formed after temperature annealing, and are then temperature stable. The defect can also be seen in as-grown material. The D1 is observed as an sharp BE at lower temperatures, and was recently correlated to the electrically observed hole trap HS1 seen in minority carrier transient spectroscopy (MCTS). The D1 defect has been explained as in its initial state, which has a tigthly bound hole and a loosely bound electron, pseudodonor. It is assumed to have important influence on device performance.

Another important defect that at the moment is subject to an extensive study, is the deep probably intrinsic defects that are seen in semi insulating Vanadium free SiC grown by HTCVD. The origin of the residual defects causing the semi-insulating behavior is not yet understood, but the presence of deeper states, labeled as UD1 and UD2, has been seen using FTIR spectroscopy.

We will also show results about lifetime limiting defects, which is an important parameter for bipolar devices. Special attention will be towards the influence of structural defects on the electrical properties such as the carrier lifetime.

Finally, we will describe the formation and properties of critical defects in high power SiC bipolar devices, under operation. We have shown that these phenomena are related to the generation of stacking faults in the SiC basal plane. This can be seen as a local reduction of the carrier lifetime, in triangular or rectangular shape, which explains the increased forward voltage drop in the diodes. The stacking faults and their associated partial dislocations are seen and identified using synchrotron topography. The entire stacking faults are also optically active as can be seen as dark triangles and rectangles in low temperature cathodeluminescence and as bright emitting features at higher temperatures. This defect is a critical defect for bipolar high power devices.

Opportunities and Technical Strategies for SiC Device Development

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The number of people worldwide working on SiC is small compared to the number working on silicon or GaAs, so our development efforts need to be *carefully focused.* We must identify devices and applications where SiC offers the greatest advantage, and where the technical and economic challenges are manageable. We must focus on *high value-added applications,* where SiC offers *system advantages (*such as high temperature operation) or capabilities not otherwise available in silicon or GaAs. We must be *innovative* in exploring new device structures and concepts to overcome the limitations of SiC materials. Finally, we must focus on material science issues that *really matter* to devices, and perform fundamental studies to resolve these issues. The most pressing materials, processing, and device design issues will be discussed in this presentation, and the current status of SiC power and microwave devices is summarized below.

POWER SWITCHING DEVICES

Virtually all SiC power MOSFETs developed to date are limited by the low MOS channel mobility, particularly on 4H-SiC. Recently, workers at Auburn and Vanderbilt Universities have shown that post-oxidation annealing in nitric oxide (NO) reduces the interface state density in the upper half of the bandgap by an order of magnitude, and increases the mobility dramatically [1, 2]. In addition, Fukuda et al. [3] have found that annealing in H_2 increases the mobility on the (11-20) surface of 4H-SiC to 110 cm^2/Vs.

UMOS vs. DMOS: which geometry is best? DMOS requires activation of p-type implants, resulting in poor surface morphology and lower channel mobility [4, 5], but the use of doped channels can mitigate this problem [6]. The inversion channel in UMOS devices is formed on a-axis surfaces exposed by RIE, where sidewall surface morphology is an issue, but recent results on un-etched planar (11-20) surfaces are very encouraging [3, 7]. Trench oxide breakdown in UMOSFETs can be overcome by the use of trench implants and current spreading layers [8]. The SIAFET mode of operation [9] is an intriguing innovation; look for more results later in this conference.

Enhancement-mode JFETs have recently been reported by workers at KEPCO and Cree [10]. These devices avoid the mobility and oxide reliability issues of MOSFETs, and exhibit attractive figures of merit, as shown in Fig. 1. Like JFETs, SiC BJTs avoid the critical MOS oxide issues and can operate at higher temperatures than MOSFETs. They are simpler to fabricate than MOSFETs, and are capable of higher current densities. However, they require substantial base current, which places demands on the drive circuitry. To minimize this, betas greater than 25-30 are needed. Cree has recently reported SiC BJTs [11] that substantially outperform the best SiC MOSFETs reported to date (see Fig. 1).

MICROWAVE DEVICES

SiC microwave MESFETs have demonstrated 120 W (pulsed) at 3.1 GHz with 41% PAE [12] and 5.2 W/mm at 3.5 GHz with 63 % PAE [13]. f_T of 22 GHz and f_{MAX} of 50 GHz have also been demonstrated [14]. Although these performance numbers are not as high as recently achieved with GaN HFETs, the relative simplicity of the SiC MESFET and the availability of a lattice matched substrate makes it an attractive device for many applications. Microwave SITs offer high power density in pulsed applications, but are restricted to low microwave frequencies (L to C band) [15, 16]. Recently, two groups have reported the first IMPATT diodes in SiC [17, 18]. Because of the high breakdown field, the pf^2 figure-of-merit for SiC IMPATT diodes is about 100x higher than either silicon or GaAs, and the small area makes IMPATTs ideal for an emerging material like SiC.

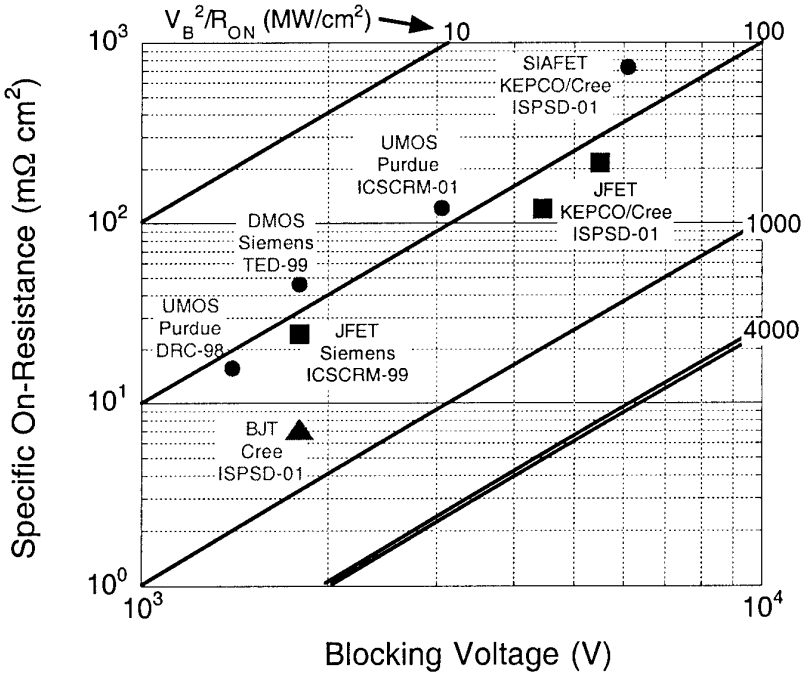


Figure. 1. On-resistance versus blocking voltage for several leading MOSFETs, JFETs, and BJTs. Diagonal lines are loci of constant figure-of-merit V_B^2/R_{ON}. The double diagonal line at 4000 MW/cm^2 is the theoretical limit for 4H-SiC unipolar devices. More results will be reported at this meeting. ***Use this chart to "pencil in" new data points as they are reported!***

Preparation of this paper was supported by grants N00014-01-1-0072 and N00014-01-0077 from the Office of Naval Research, and by the Indiana 21ST Century Research & Technology Fund.

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MoA3 Bipolar and PN Junction

Measurements and device simulations of avalanche breakdown in high voltage 4H-SiC diodes including the influence of macroscopic defects

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SiC high voltage diodes have important applications as freewheeling diodes in motor drives and power transmission systems. A stable avalanche, which is very important for diode reliability, cannot be taken for granted in SiC due to high concentrations of macroscopic defects. The influence of screw dislocations (SDs) on avalanche breakdown in 4H-SiC was examined by Neudeck [1] who found a typical breakdown voltage reduction by 30 % in low voltage diodes (V_{br}=90 V) with SDs, but a high and similar avalanche energy to fail for diodes with and without SDs. This paper addresses the breakdown characteristics of high voltage 4H-SiC diodes with an area large enough that screw dislocations are most likely present. An important effect at high voltages, in addition to a high power dissipation, is that the space charge of free carriers can produce a negative resistance [2]. This effect becomes most pronounced for high voltage diodes since it occurs as the free carrier concentration in the drift region becomes roughly equal to the doping concentration [2]. Device simulations of reverse I-V characteristics were performed using the commercial software AVANT! Medici with physical models according to [3]. The high voltage diodes, which were experimentally investigated, are p^+nn^+ diodes with an implanted p^+ emitter and a similar design as described in [4]. The expected breakdown voltage is 3000-4000 V. The critical field strength (E_{crit}) was reduced by 20 % (to obtain ~30 % V_{br} reduction) in simulations to model breakdown in a SD, since each of the investigated 1 mm^2 area diodes should contain several SDs. Fig. 1 shows a 1D simulation of the reverse I-V characteristics in breakdown together with 2D cylindrical coordinate simulations (to be described). The onset of negative resistance in the 1D simulation occurs at a current density of 6000 A/cm^2, as the average carrier concentration differs only 2 % from the n-base doping in good agreement with [2]. To include current spreading in the n-base, 2D cylindrical coordinate simulations were performed with E_{crit} reduced by 20 % only inside a cylindrical region of varying radius (R) with base areas at anode and cathode. Fig. 1 displays simulated normalized current density (J_{norm}), i.e. the current divided by the area of the region with reduced E_{crit}. The reason for the much higher J_{norm} at the onset of negative resistance in the 2D simulations compared to 1D is current spreading which reduces the free carrier space charge in the n-base. As the onset of negative resistance is reached, however, a high current density filament is formed through the cylindrical region with a reduced E_{crit}. This current filamentation is assumed to be destructive. The isothermal conditions simulation conditions are valid only during very short times for the highest current densities in Fig. 1. The results indicate, however, that an unstable avalanche can occur at lower current densities in a macroscopic defect with a larger area, such as for instance a micropipe, for which a lower value of E_{crit} should be used in simulation.

Five diodes, of similar design as in ref. [4], with 1 mm^2 area and an expected breakdown voltage of 3000-4000 V were tested with reverse bias pulses of 4 μs pulse-width. Three of the diodes which had static breakdown voltages of 2000, 3400 and 2700 V failed destructively in

pulsed measurements at the voltages 3200, 3670 and 3700 V, all within 2 μs after reverse biasing after a maximum avalanche current of 5 mA. All three diodes had a visible damage at the junction edge along the surface and this edge breakdown presumably damaged the diodes before a significant avalanche was reached in a SD as can be expected above 4000 V (see Fig. 1). The remaining two diodes (D1 and D2) had a low static breakdown voltage of about 700 V but could be pulsed into breakdown at high currents. Fig. 2 shows the quasi-static reverse I-V characteristics of D1 and D2 as obtained during 4 μs pulses. Also shown in Fig. 2 are simulations with a 70 % reduction of E_{crit} in a cylindrical region with R=15 μm, in one case through the whole epilayer and in the other only in the pn junction region. The results in Fig. 2 suggest that the diodes D1 and D2 have a reduced critical field strength mainly in the pn junction region. The high resistance of the diode in simulations is caused by the space charge limited current and is hence quite sensitive to the radius of the region with reduced E_{crit}. The diodes D1 and D2 also survived a fast turn-off from 1 A forward current to 1500 V reverse bias with a visible avalanche current. A negative temperature coefficient of the breakdown voltage was seen for D1 and D2 as an increasing current during longer pulses. Additional measurements are planned for diodes with even higher breakdown voltages.

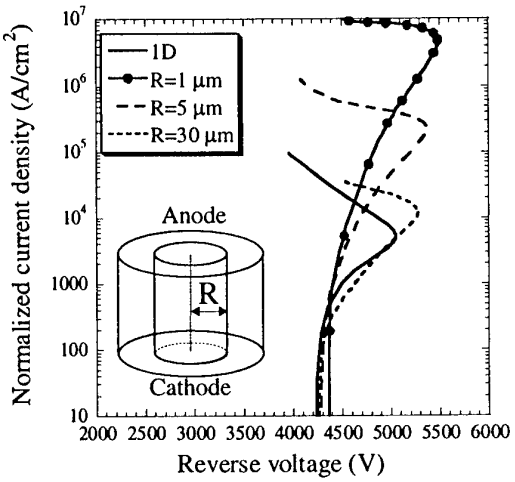


Figure 1: Simulated reverse I-V characteristics of diodes with 20 % reduced E_{crit}, 1D simulation and 2D cylindrical coordinate simulations with E_{crit} reduced inside R=(1, 5, 30) μm

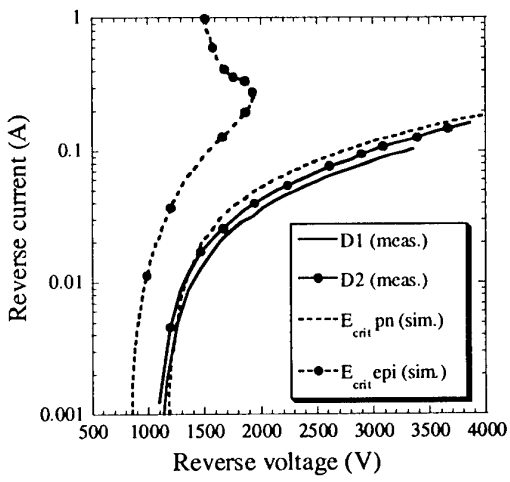


Figure 2: Pulsed reverse I-V measurements for diodes D1 and D2 and cylindrical coordinate simulations with 70 % reduced E_{crit} inside R=15 μm in the pn junction region (pn) and through the whole n-base (epi)

Acknowledgements

The ABB SiC project is kindly acknowledged for supplying the investigated high voltage diodes, ELFORSK is acknowledged for financial support.

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High-Voltage SiC pin Diodes with Avalanche Breakdown Fabricated by Aluminum or Boron Implantation

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The characteristics of planar pn junction are a key issue which controls the performance of various power devices such as pin diodes and DIMOSFETs. In SiC processing technology, high-dose Al^+ implantation has been a major obstacle, because of its high sheet resistance of 10 k$\Omega/\square$ [1]. Regarding the pn junction characteristics, a positive temperature coefficient of breakdown voltage is one of the most crucial requirements for reliable power devices. Many SiC diodes generally show, to our knowledge, negative temperature coefficients except one report [2]. In this study, the authors realized a low sheet resistance below 4 k$\Omega/\square$ by hot implantation of Al. A clear positive temperature coefficient of breakdown voltage is also demonstrated.

N-type 4H-SiC (0001) epilayers with a donor concentration of 4×10^{15} cm^{-3} grown in the authors' group were used in this study. Multiple implantation of Al^+ (10$\sim$180 keV) was carried out to obtain a 0.25 μm-deep box profile of Al. The implantation temperature was RT or 500 °C. Post-implantation annealing was performed at 1600$\sim$1700 °C for 30 min in Ar ambience.

Figure 1 shows the measured sheet resistance of Al^+-implanted regions as a function of total implant dose. The sheet resistances and electrical activation of Al^+-implanted regions were significantly improved by hot implantation and by increasing annealing temperature up to 1700 °C. A low sheet resistance of 3.6 k$\Omega/\square$ was obtained by implantation at 500 °C followed by annealing at 1700 °C, when the total implant dose was 4×10^{15} cm^{-2}.

Pn junction diodes with planar structure were fabricated by employing B^+ or Al^+ implantation at room temperature. The junction depth was 0.4 or 0.7 μm with an implanted impurity concentration of 2×10^{18} cm^{-3}. The implantation was carried out for 20 μm-thick n-type 4H-SiC epilayers ($N_d = 3.5\times10^{15}$ cm^{-3}). To reduce the contact resistance on the implanted regions, surface p^+-regions were formed by Al^+ implantation at 400 °C. The diodes were annealed at 1700 °C for 30 min. The surface of diodes was passivated with SiO_2 formed by wet oxidation.

Figure 2 demonstrates the current density vs voltage characteristics of deep B^+-implanted diodes with a diameter of 100 μm measured at RT. The specific on-resistances determined at 100 A/cm^2 level were 6.3$\sim$9.1 mΩcm^2. These on-resistances include the substrate resistance of 4.1 mΩcm^2, so that, the contact resistances onto the shallow Al^+-implanted p^+-region estimated to be less than 2.2 (6.3 − 4.1) mΩcm^2. These results indicate that good ohmic contacts were formed by shallow Al^+ implantation at 400 °C. The diodes exhibited stable and reversible breakdown, in particular, deep B^+-implanted diodes did not extend to destructive breakdown even at a high reverse current density of 3.0 A/cm^2 and a reverse voltage of 2600 V. This 2600 V is 80 % of the ideal (parallel

plane) breakdown voltage (about 3200 V) in this device structure. This unusually high breakdown voltage might originate from the formation of a thick i-layer due to the in-diffusion of B [3] and/or from the extension of space charge regions caused by effective negative charges at the SiO_2/n-SiC interface [4]. Regarding switching, the diodes showed fast switching with a turn-off time of 10 ns.

Figure 3 shows the reverse blocking characteristics of (a) Al^+- and (b) deep B^+-implanted diode, measured at RT, 335 K, and 373 K. At RT, the Al^+- and deep B^+-implanted diodes could block 1020 and 2900 V, respectively, which were approximately 32 and 90 % of the ideal breakdown voltage. The breakdown voltage of each diode increased with increasing temperature. This positive temperature coefficient of reverse breakdown voltage means avalanche breakdown, not other mechanism such as defect-assisted tunneling.

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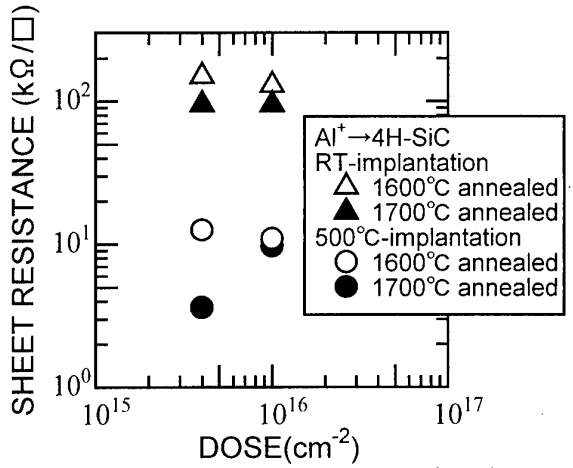


Fig. 1. Dependence of sheet resistance for Al^+-implanted 4H-SiC layers on total implant dose after 1600℃ and 1700℃ annealing.

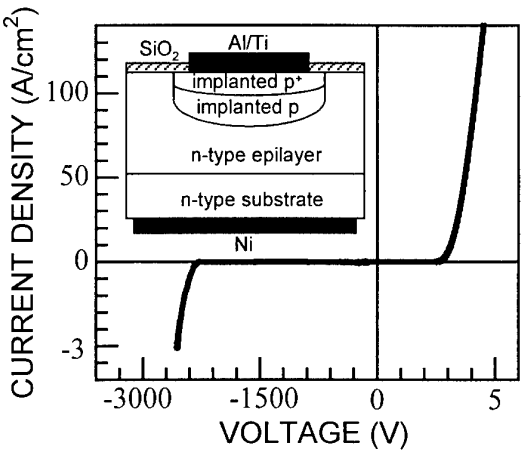


Fig. 2: Current density vs voltage characteristic of deep B^+-implanted diode.

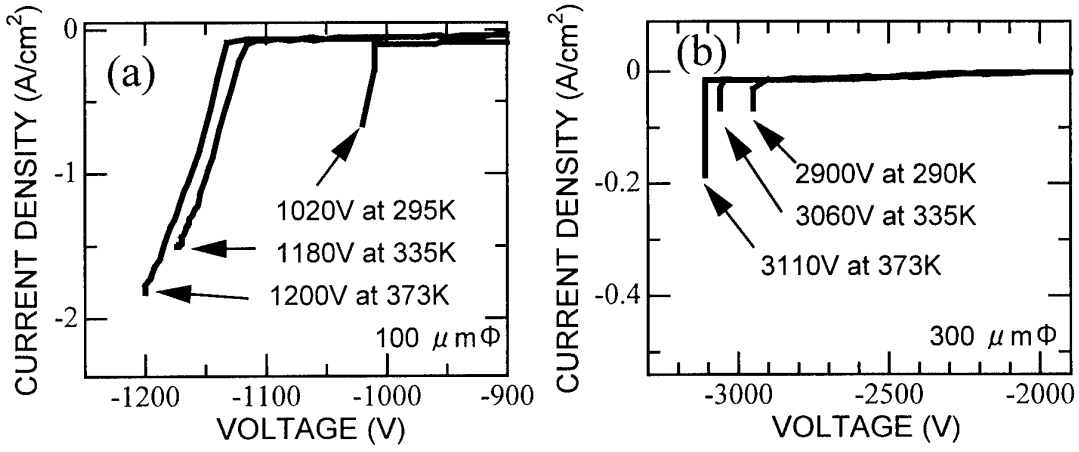


Fig. 3: Reverse blocking characteristics of (a) Al^+- and (b) deep B^+-implanted diode.

Recombination-enhanced defect formation in high voltage SiC diodes

J. Liu, M. Skowronski

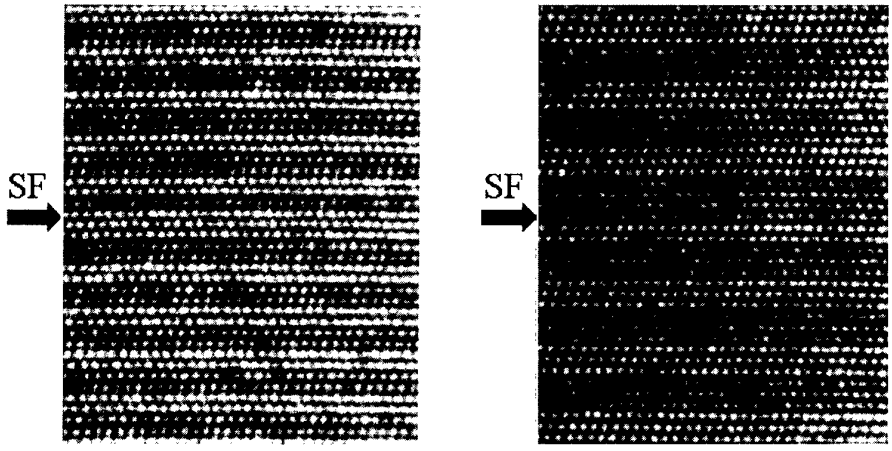
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Recent long term reliability tests of SiC p-n diodes revealed increase of forward voltage drop occurring over a period of hours or days under forward bias[1]. The electrical characterization results were interpreted as a consequence of recombination-enhanced stacking faults formation based on x-ray topography and luminescence characterization results[2]. This report describes the structure of bias-induced defects studied by conventional and high resolution transmission electron microscopy and discusses the formation mechanism.

High voltage 4H and 6H-SiC p+-n- junctions were stressed at current density of 100 A/cm^{-2}. Cross-sectional samples have been prepared and analyzed using Philips 420 microscope operating at 120 kV and JEOL 400EX microscope operating at 400 kV. Stressed diodes contained typically between $0.2x10^4$ and $2x10^4$ cm^{-1} faults distributed between the metal/semiconductor and epilayer/substrate interfaces. The cross sections of "virgin" device structures were defect free. The stacking sequences of multiple faults in both 4H- and 6H-SiC polytypes have been analyzed using high resolution microscopy. The structure of all defects was consistent with isolated Shockley-type faults (Fig. 1). Such faults in silicon carbide crystals were reported to form during plastic deformation at low temperatures[3]. The analysis of stacking sequences and of partial dislocations bounding the faults indicates that the driving for formation of defects is shear stress present in the diode structure. The stress is macroscopic in origin.



(a) (b)

Fig. 1 High resolution TEM images of recombination-induced stacking faults in (a) 4H-SiC and (b) 6H-SiC high voltage diode.

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Electrical characterization of high-voltage 4H SiC diodes on high-temperature CVD grown epitaxial layers

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Silicon Carbide power devices designed for blocking high voltages are known to require comparatively thick low-doped drift zones. Those regions are most often provided by epitaxial layers due to the comparatively high concentration of impurities still present in available bulk 4H silicon carbide material. The growth rate of conventional chemical vapour deposition (CVD) however is limited to a few micrometers per hour when the requirements for residual doping and surface morphology are as high as for base material in power device applications [1]. High-temperature chemical vapour deposition (HTCVD) in vertical chimney reactors has recently been developed and was shown to produce high quality epitaxial layers with low background doping and smooth surface morphology at growth rates of up to $100\,\mu$m/h [2]. So far only limited results exist for the application of these epitaxial layers in electronic devices [3]. In this study high-voltage diodes of different types have been processed on two samples of HTCVD epitaxial layers.

The epitaxial layers were grown on a commercial 4H-SiC wafer (Cree, n-type $7.8 \cdot 10^{18}\,\mathrm{cm}^{-3}$) at Linköping University, Sweden and have a nominal epilayer thickness and net n-type doping of $60\,\mu$m, $\leq 2 \cdot 10^{14}\,\mathrm{cm}^{-3}$ (sample A) and $65\,\mu$m, $\leq 9 \cdot 10^{15}\,\mathrm{cm}^{-3}$ (sample B) measured by photoluminescence and Schottky barrier capacitance-voltage (CV) technique after growth. Sample A has an additional highly doped buffer layer grown underneath the low-doped epilayer to prevent electrical punch-through into the substrate.

Both Schottky and Al implanted pn diodes as well as merged pn/Schottky diodes (MPS diodes, [4]) were manufactured in a standard process developed at our institute [5]. A titanium-tungsten alloy was used both for the ohmic contact to the p-type implanted regions and the large area backside contact, as well as contact metal for the Schottky barriers. The diodes were equipped with different termination schemes to reduce edge effects under reverse bias operation [6]. Field rings were implanted simultaneously with the anode structures of both pn and MPS diodes through a wet etched beveled silicon dioxide mask. Field plates were formed in the contact metallization layer on top of a $2\,\mu$m thick silicon dioxide layer deposited in a CVD process using TEOS as precursor.

Forward operation of both pn and MPS diodes show distinct areas of negative resistance attributed to plasma injection into the low-doped drift zone. The forward voltage drop of a limited number of diodes was increasing when operated under a continuous current density above $100\,\mathrm{Acm}^{-2}$ for a couple of hours (see Fig. 1). Similar degradation was observed by Lendenmann et. al. [7] on pn diodes made of conventional CVD material.

The reverse leakage current was found to depend on the presence of up to $2 \cdot 10^4\,\mathrm{cm}^{-2}$ surface defects of the half-moon type [2] (see Fig. 2) on the active area of the samples. Some pn diodes free of, or only containing a few surface defects and with working termination schemes have electrical breakdown above 3500 V while others containing surface defects show soft breakdown already at as low as 800 V (see Fig. 3).

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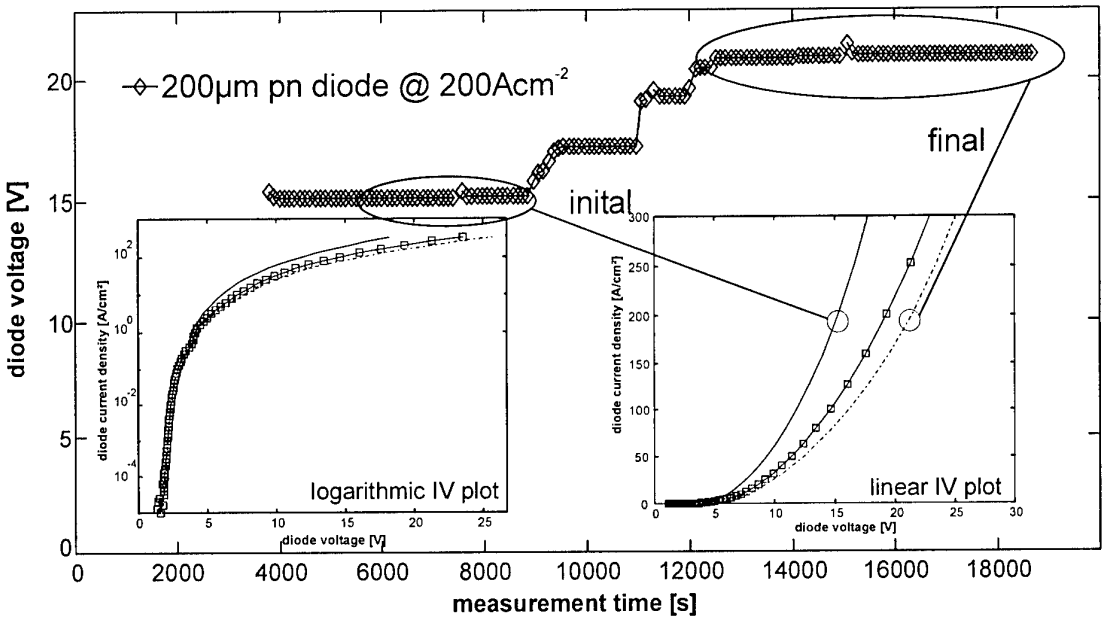


Figure 1: *Long term stability measurement of the forward voltage drop of an implanted* 200 μm *diameter pn diode at a constant forward current density of* 200 A cm^{-2}. *Insets show static IV measurements at the indicated times.*

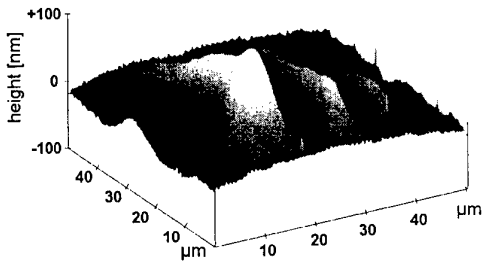


Figure 2: *AFM micrograph of a surface defect of the half-moon type. The peak-to-valley height is about* 200 nm, *the lateral dimension typically* $\geq$ 50 μm.

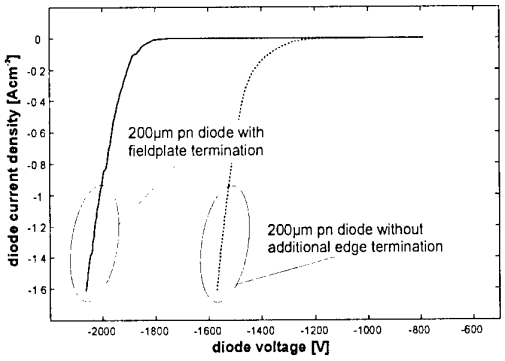


Figure 3: *Reverse breakdown of two pn diodes with* 200 μm *diameter. The fieldplate terminated diode contains 4 single half-moon defects in its active area.*

Investigation of thermal properties in fabricated 4H-SiC high power bipolar transistors

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Recent research on switch devices has been focused mainly on field effect devices (e.g. MOSFET, MESFET, and JFET). In contrast to this, only a few publications have been presented on SiC bipolar junction transistors (BJT) [1, 2]. One of the main reasons for this is the short minority carrier lifetime in p-type layers, which is detrimental to the current gain. However, as the material quality improves and epi layer growth develops, SiC bipolar transistors can be very competitive. As a switch element the bipolar transistor has the advantages of carrier modulation and better current capabilities compared to most FETs. In Thyristors and IGBTs, the main current flow has a pn-barrier to cross, resulting in an initial forward voltage-drop almost equal to the built-in voltage (~3 V for 4H-SiC). In comparison, the BJT switch device has junction cancellation between the emitter and collector, which results in a lower initial voltage drop over the switch [3]. In the study reported here a 4H-SiC BJT was fabricated using an etched mesa structure from an epi layer stack. The doping and epi layer thicknesses were designed for high voltage operation (~1.5 kV parallel breakdown), see schematic device structure in Fig. 1. Measurements of the fabricated transistors were performed with a HP4156 and a probe station equipped with a hot chuck, allowing measurements up to temperatures of 300 °C.

The measured transistors showed a strong self-heating effect when the power dissipation was increased, which led to a lowered current gain. This temperature dependence was investigated with relatively small self-heating conditions (V_{CE} = 20 V), and the current gain decreased from 10 at 25 °C to 6 at 300 °C. By assuming that the current gain only depends on temperature, the junction temperature can be extracted from three V_{CE}-diagrams at three different temperatures on the heat sink at the backside contact [4]. This extraction technique was used on the fabricated transistors at heat sink temperatures of, 25 °C, 50 °C, 75 °C, see Fig. 2. The extracted junction temperature at I_C = 60 mA was 120 °C, which is approximately 100 °C above the heat sink temperature. In addition, the total thermal resistance to the heat sink was estimated to 27 K/W at 25 °C. The measured device in Fig. 2 had an emitter area of $1.5 \cdot 10^{-4}$ cm^2 (i.e. 50 mA corresponds to 333 A/cm^2).

Furthermore, thermal device simulations have been performed in order to investigate the origin of the current gain reduction, and also to confirm the thermal dependence in the included device simulation models. The measured data presented in Fig. 2 has a much steeper drop in current gain (β), in comparison with a temperature dependent simulation with models taken from [5] and [6]. In this work various simulation geometries and models have been investigated to explain the thermal behavior (e.g. 3D-simulation, surface recombination, Auger recombination, and temperature dependent life-times). The model parameters are taken from literature, and a discussion on minor adjustments of these values is undertaken. Furthermore, pulsed measurements are compared with transient simulations in order to investigate the self-heating transients, which have been shown to be very fast in SiC.

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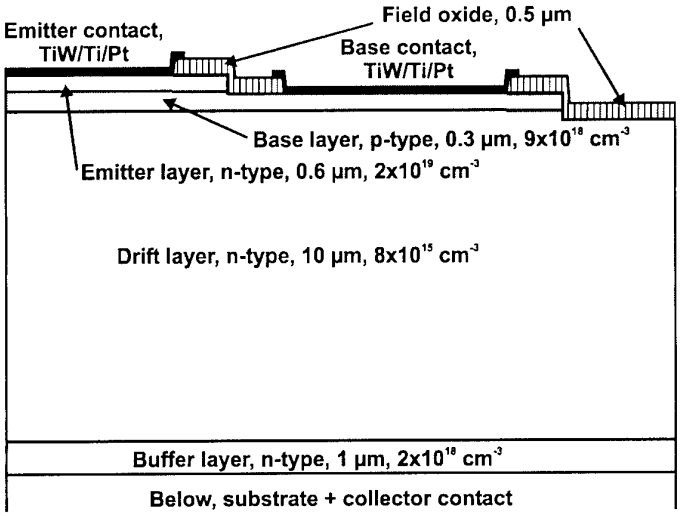


Fig. 1. A schematic cross-section of the fabricated devices.

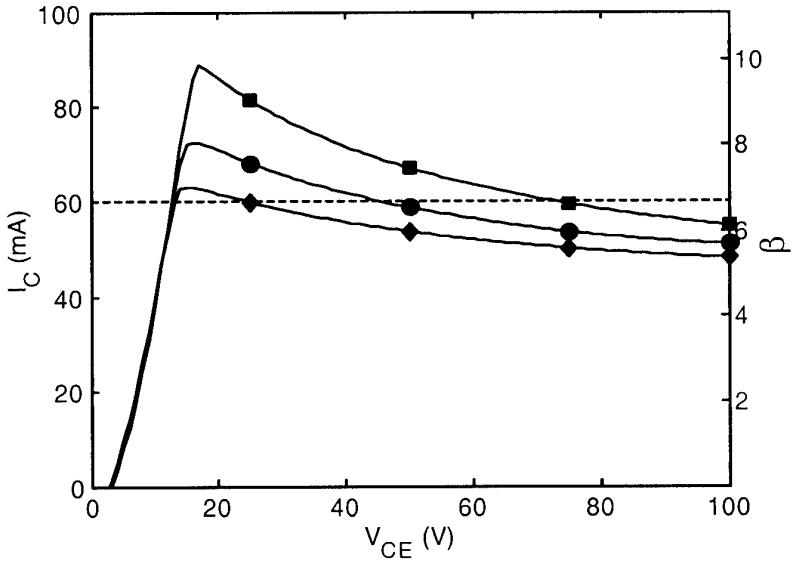


Fig. 2. Measured V_{CE}-diagrams at three different temperatures, ■ 25 °C, ● 50 °C, and ♦ 75 °C. The intersections with the dashed line was used for the extraction of T_j = 120°C.

Improvement and Analysis of Implanted-Emitter Bipolar Junction Transistors in 4H-SiC

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SiC has long been recognized as the choice for high voltage, high temperature, high power applications. Significant progress has been made in SiC bipolar junction transistors, most of which on epi-emitter BJTs [1-4]. The implanted-emitter BJTs offer ease of controlling base width by varying the emitter implants. We reported the first implanted-emitter BJT in 4H-SiC [5]. The device showed a record-high common emitter current gain of 40, and forward drop of 1V at 50A/cm^2. The open-base breakdown voltage was less than 60V due to base punch through. In this work, high voltage, implanted-emitter, npn BJTs were fabricated. Different emitter implantation species and annealing cycles were used to study the effect of emitter implant. The devices showed maximum blocking voltage of 500V and common emitter current gain of 8.

The device cross-section is shown in Fig. 1. The starting wafers were (0001), Si face, $P^+/P/N^-/N$ substrate wafers. The top P^+ epi layer ensures good P-base contact and also avoids high temperature anneal of P^+ implant. The emitter was formed by implanting into P-base region at 600°C using five successive implants. Four samples were fabricated with different implantation species and annealing cycles, but all with the same dose of 3×10^{15}cm^{-2}. The implantation splits and the measured sheet resistances are shown in table 1. Previous study has shown that low sheet resistance can be obtained for phosphorus and arsenic when annealed at 1200°C [6,7].

The distribution of the common emitter current gain of the four samples and their medians are shown in Fig. 2. At room temperature, maximum common emitter current gain of 8 was measured on 300 μm×300 μm devices of sample C with phosphorus implantation and 1600°C anneal. Fig. 3 shows the effect of emitter periphery on current gain for sample C, it is seen that current gain increases proportionally with the increase of emitter periphery. At high temperature, specific on-resistance increases as shown in Fig. 4, making this device attractive for paralleling and for preventing thermal run-aways. The reason is that base carrier concentration increases at high temperature due to increased ionization of deep level acceptors. As a result, β decreases with temperature, leading to the increase of specific on-resistance at high temperatures. This feature was also observed in the previous samples [5].

The distribution of the open-base breakdown voltages of the four samples are shown in fig. 5. The As sample does not have a high blocking voltage. The majority of the other samples show BV_{CEO} ranging from 100V to 500V, the highest blocking is 550V. The increase of the breakdown voltage and the decrease of the current gain are both due to the increased base width.

Fig. 6 shows the open-base turn-off transient of sample A and sample C. During open-base turn-off, the device is turned off mainly by recombination. The turn-off time is ~ 1μs.

Acknowledgement: The authors gratefully acknowledge the support from MURI of the Office of Naval Research (# N00014-95-1-1302) and NSF Center for Power Electronic Systems (# EEC-9731677).

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TABLE I Emitter implantation splits and measured sheet resistance

Sample	Emitter implant species	Annealing temperature (°C)	Annealing time (min)	Sheet resistance (Ω/sq)
A	Nitrogen	1600	15	3000
B	Arsenic	1200	30	3400
C	Phosphorus	1600	15	230
D	Phosphorus	1200	30	1200

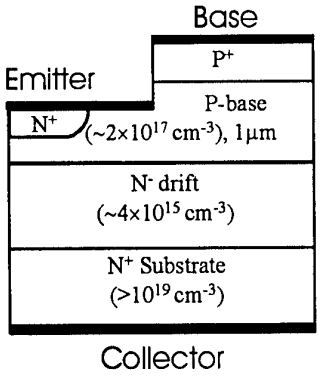


Fig.1 Schematic cross-section of implanted-emitter 4H-SiC BJT studied in this work

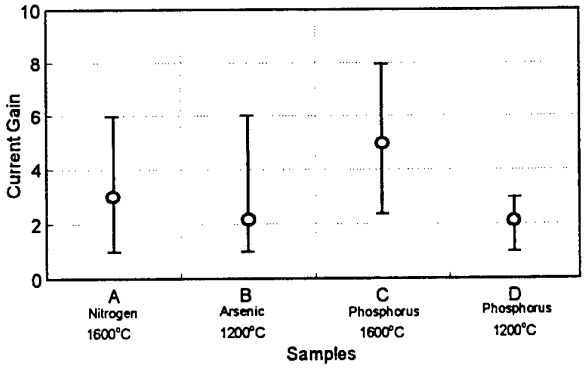


Fig.2 Distribution and median of maximum common emitter current gain at V_{CE}=10V

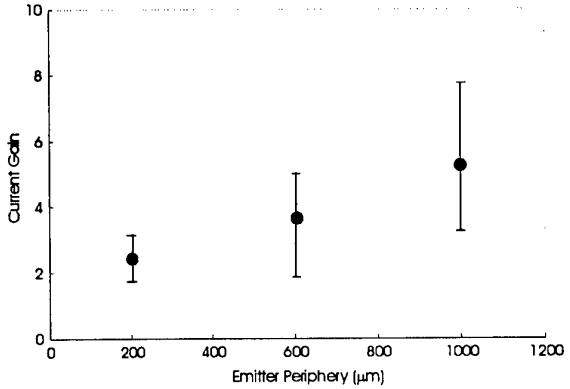


Fig.3 Effect of emitter periphery on current gain of sample C

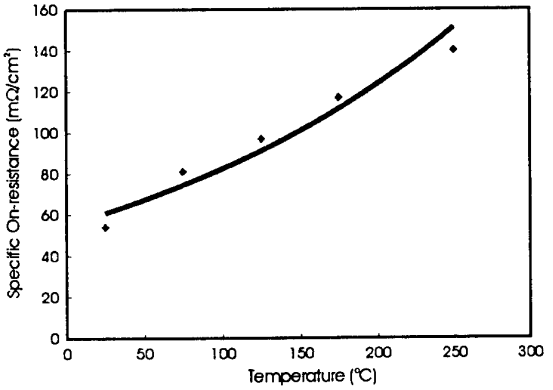


Fig.4 Temperature effect on specific on-resistance of sample C

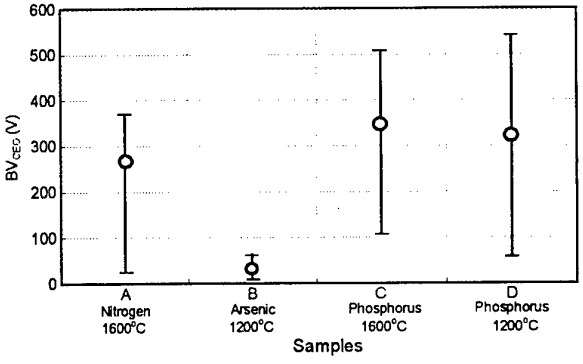


Fig.5 Distribution and median of open-base breakdown voltage

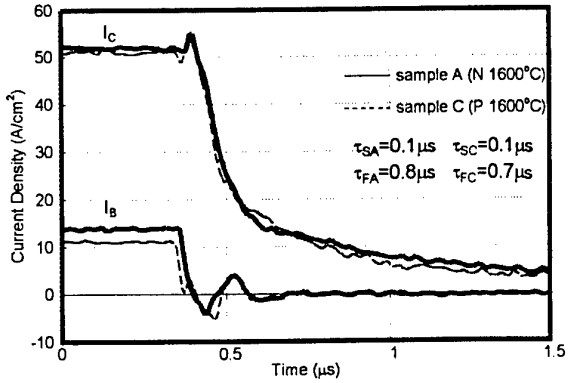


Fig.6 Open-base turn-off transient of sample A and C at room temperature

All-SiC Half-Bridge Inverter Characterization of 4H-SiC Power BJTs Up To 400V-22A

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SiC BJT has the advantage of being free of gate oxide, which makes it suitable for applications under high temperatures (over 150 –200 C). It is also a better candidate for many high temperature applications when compared to the latch-on SiC GTOs. 6H-SiC BJTs capable of blocking 50V were first fabricated and measured up to 0.8mA with a current gain of 4~8 in 1978 [1]. The first 4H-SiC power BJT was reported in 2000 with a capability of 800V-2.7A and a current gain of 9 [2]. High gain and high voltage 4H-SiC BJTS were subsequently reported [3,4], showing increased interests in 4H-SiC power BJTs. In this paper, we report BJTs fabricated in 4H-SiC with emitter current measured up to 16A (312A/cm$^{2)}$ with a maximum common emitter current gain of 7. Blocking voltage BV_{CEO} measured up to 600V is achieved, with some devices blocking more than 900V.

The 4H-SiC wafer used for the BJT fabrication is purchased from Cree Inc. Fig. 1 shows a section of the cross sectional view of the BJT structure. The BJTs have six 96μm x 990μm emitter fingers surrounded by seven base fingers. The base–emitter spacing is 6 μm. The total collector area, including the three MJTE regions, is 1.57x1.66 mm^2. The BJT p-base is ion implanted with Al and C co-implantation to $6x10^{20}cm^{-3}$ to reduce base contact resistance. To improve device blocking capability, the base-collector junction is terminated by multi-step junction termination extension (MJTE), as shown in Fig.1. After MJTE etching, sacrificial oxide and about 40nm of passivation oxide is grown thermally followed by 1 μm LPCVD SiO_2. Then oxide window is opened. Al/Ti/TiN multiple-layer base contact metal is sputtered and patterned by lift-off. Emitter contact metal (Ni) is then sputtered after opening the emitter oxide window. Following Ni sputtering onto the backside of the samples, all the contacts are annealed in nitrogen forming gas (5% H_2 in N_2) at 1050°C for 5 min. The multi-cell BJTs are packaged in nitrogen ambient at 390°C and Au ribbon bonding is conducted at 180°C.

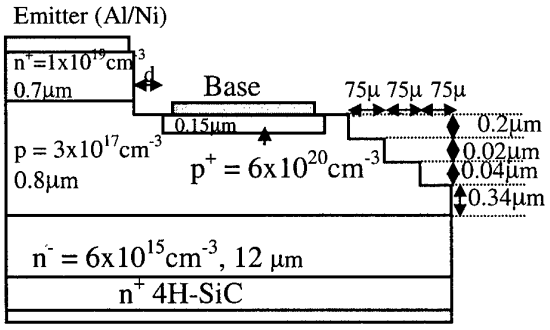


Fig.1 Cross-sectional view of BJT structure

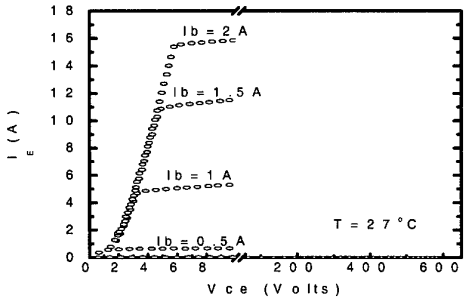


Fig.2 Ic-Vce characteristics of 4H-SiC npn BJT

Fig.2 shows the common emitter I_E vs. V_{CE} characteristics at room temperature for a packaged BJT with 9 cells in parallel. The BJT shows a common emitter current gain I_C/I_b of 7 with a

forward blocking voltage (BV_{CEO}) measured up to around 600V. The DC emitter current is measured up to 16A at a base current of 2 A, corresponding to an emitter current density of 312 A/cm^2. Poor sidewall passivation and surface recombination contribute to the first 2V drop without current gain. Low carrier diffusion length in base region and low conduction modulation in the drift region may partly contribute to the large voltage drop at high current (I_E=15.5 A with V_{CE} = 5.8 V). The large emitter size is designed for high quality 4H-SiC with long minority carrier lifetimes. With the base minority carrier lifetime still quite low (sub-microsecond), current crowding and low carrier diffusion length reduce area efficiency of the emitter. Devices with smaller cell pitch sizes are being processed and the result will be reported.

The packaged 4H-SiC BJTs have been tested in an all-SiC inductively loaded half-bridge inverter by using 4H-SiC MPS diodes as the free-wheeling diodes. The inductive load used in the switching measurements is chosen to be as high as 1 mH to simulate a high power AC induction motor. Fig.3 shows 400V-22A switching waveforms of SiC BJT with a base driving current around 3 A. The effect of SiC MPS diodes on the SiC BJT switch turn-on loss is shown in Fig.4. It is seen that, when compared to the ultrafast commercial Si PiN free-wheel diodes, 4H-SiC MPS diodes result in reduced SiC BJT switching loss. Further measurements are underway to compare all-SiC half-bridge inverter BJT turn-on and turn-off losses with Si-IGBT based half-bridge inverters. The results will be reported.

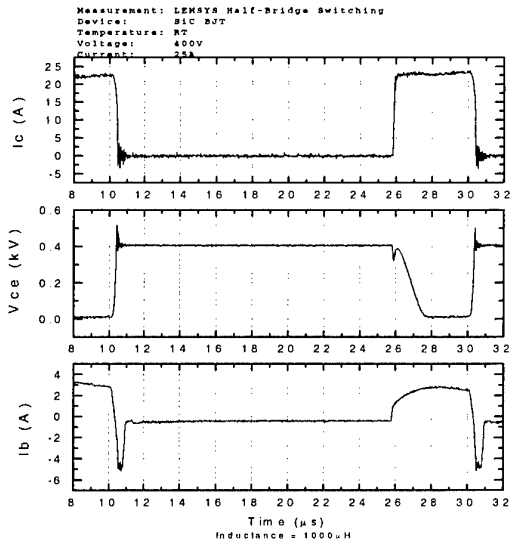


Fig. 3 Half-bridge inverter switching waveforms for the 4H-SiC BJT.

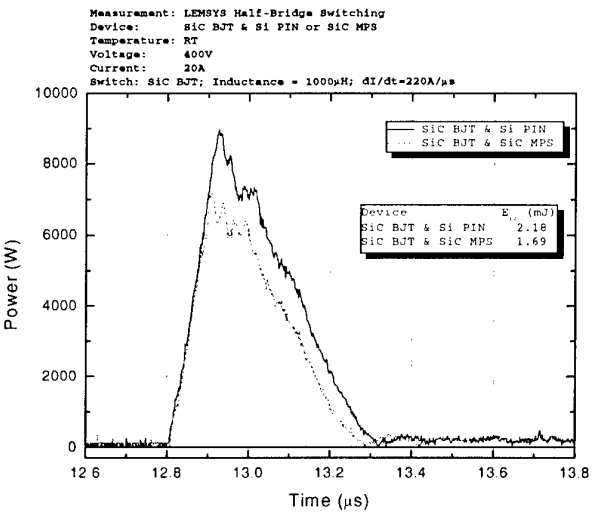


Fig.4 Turn-on power loss of 4H-SiC BJT in a half-bridge inverter using either Si PiN or SiC MPS free-wheeling diodes.

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MoB3 Defects and Dopants

Impurity Controlled Dopant Activation : The Role of Hydrogen in the p-type Doping of SiC.

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Hydrogen is a natural contaminant of the SiC growth processes and may occur in large quantities in as grown epilayers. Its presence might affect doping efficiency by influencing the site competition process or by passivating or compensating the dopants. Passivation by complex formation with hydrogen has been proven both for Al and B [1], however, the experimentally observed reactivation energies seem to differ by about ~1 eV [2]. Furthermore, hydrogen incorporation proportional to that of boron was observed in B-doped as grown CVD samples [3,4] while the amount of hydrogen was found to be two orders of magnitude less than the aluminum concentration in case of Al-doping [5].

Extensive calculations regarding geometry and formation energy of *p*-type substitutional dopants (B, Al) and their complexes with hydrogen have been carried out. The local density approximation of the density functional theory was used with plane wave basis and norm-conserving pseudopotentials. Our results indicate that hydrogen plays a key role in the in-growth doping of epilayers with boron. In the absence of hydrogen, boron prefers the carbon site. If hydrogen is present, as in typical CVD conditions, boron is incorporated together with hydrogen (in equal amounts) and the B+H complex favors the silicon site. Annealing around 500 °C may remove hydrogen leaving the Si site substitutional boron behind. Since boron at different sites gives rise to different electrical activities, the effect of hydrogen influences its activation as a shallow acceptor.

In contrast to boron, aluminum is always incorporated as isolated substitutional at the silicon site, independent of the presence of hydrogen. The calculated amount of incorporated hydrogen in that case is in good agreement with experimental findings for aluminum doped samples. Dissociation of the stable dopant plus hydrogen complexes for boron and aluminum has also been investigated. Our calculations yields a dissociation energy difference of ~0.9 eV between the stable B+H and Al+H complexes, in good agreement with experiment. Characteristic local vibration modes of the complexes are predicted.

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Incorporation of Hydrogen (^{1}H and ^{2}H) in 4H-SiC during Epitaxial Growth

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Hydrogen in semiconductors is known to be trapped by donors and acceptors as well as "dangling bonds" in vacancies, dislocations and grain boundaries [1]. The presence of hydrogen can drastically change the electronic properties and strongly influence device performance. In SiC technology hydrogen is extensively used and there are many opportunities to introduce hydrogen into SiC structures [2]. Redistribution may occur during subsequent annealing steps. In p-type SiC hydrogen will form complexes with boron and aluminum acceptors [3,4]. Unfortunately, possible hydrogen trapping centers in n-type are not well documented. Trapping centers are actually necessary to detect the migrating hydrogen with secondary ion mass spectrometry (SIMS) since free hydrogen diffuses at concentration levels well below the detection limit.

In this work we have studied the incorporation of deuterium (^{2}H) and normal hydrogen (^{1}H) from the carrier gas during epitaxial growth. SIMS has been utilized to obtain the depth distribution of hydrogen. There are two reasons for the use of ^{2}H in combination with ^{1}H. First ^{2}H relative to ^{1}H increase the SIMS-sensitivity by three orders of magnitude and second, sequential use of ^{1}H and ^{2}H gives information about when hydrogen is retained in SiC. 4H-SiC epitaxial structures with alternating aluminum and nitrogen doped layers separated by undoped material have been grown at 1600°C (se Fig.1). A mixture of 77% ^{2}H and 23% ^{1}H (in total 13 l/min) were used as carrier gas during the growth of the first four doped layers while only ^{1}H (13 l/min) was employed for the growth of the remaining structures and cool down procedure. The same type of structure has also been grown starting with pure ^{1}H followed by a deuterium mixture as carrier gas. Both n and p-type substrates have been used.

Fig.1 shows that ^{1}H get trapped in a heavily Al doped layer. Deuterium is also detected in this layer at a concentration close to natural abundance (0.015%). In this case the second part of the growth and the cooling down procedure has been performed in a $^1H_2$ ambient. Besides from the layer of the highest Al content the ^{2}H concentration is below detection limit, $1x10^{14}$ cm^{-3}. When the sequence of used carrier gases is changed i.e. the deuterium mixture is used in second part of the epitaxial growth no ^{1}H is recorded in the sample above the detection limit ($1x10^{17}$ cm^{-3}). ^{2}H is found in layers with Al concentrations above $5x10^{17}$ cm^{-3} while ^{2}H is below the detection limit in the N doped layers. However, the ^{2}H concentration in both n-type and p-type substrates are $1x10^{15}$ cm^{-3}.

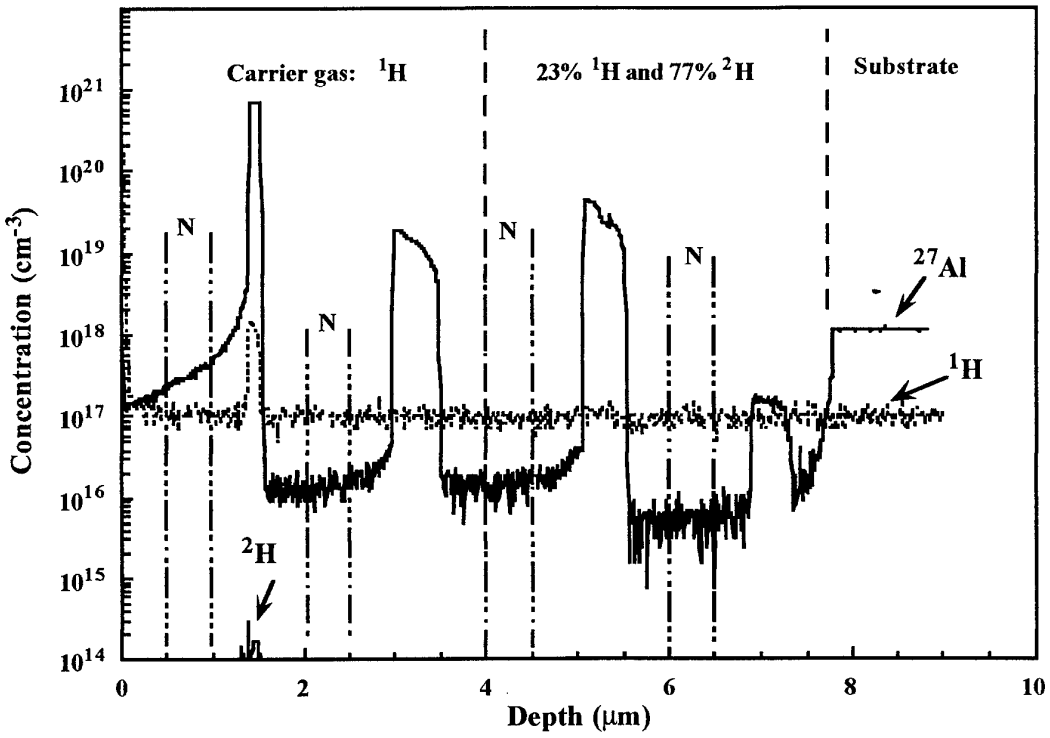


Fig.1. SIMS measurement of depth distribution of ^{1}H and ^{2}H in an Al and N doped epitaxial grown 4H-SiC structure. A mixture of ^{2}H and ^{1}H has been used in the first part of the growth and pure ^{1}H has been employed in the second part and during cool down.

Our results show a very high mobility for hydrogen in SiC at the growth temperature, 1600°C. Only the carrier gas (^{1}H or ^{2}H) used at the later part of the epitaxial growth will be incorporated in SiC. Hydrogen may be incorporated in both p- and n-type SiC if suitable traps are available. Comparing the ^{2}H incorporation in the epitaxial structures and n-substrate eliminates N as a probable trapping center for hydrogen. The difference between the Al to ^{2}H ratio in the epitaxial material and the p-type substrate indicates that Al may not be the main hydrogen trap in the substrate. Furthermore, if the hydrogen concentration is constant through the whole substrate (thickness ~0.4 mm) it will be a large hydrogen source, which may redistribute in subsequent annealing steps.

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Physical mechanism for the anomalous behavior of n-type dopants in SiC

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The selective doping of SiC by ion-implantation is a key process for fabricating the planar devices. A donor (N, P, As) and an acceptor atoms (Al, B, Ga) are required for the tailored n- and p-type doping profiles. Recent reports on n-type SiC doping indicate that P is a potential candidate for power device applications which require low source/drain contact resistance. Capano et al.[1] reported that P is the better choice for the high doses due to higher electron mobility, however, N is preferred for the moderate doping levels. Khan et al.[2] reported about four times lower dielectric strength of thermal oxide grown over a P implanted region than a non-implanted region and about two times lower than the N implanted region under the identical conditions. However, the average ionization energies (h- and k-lattice sites) of the P donor is relatively higher than that of the N donor in 4H-SiC. A physical explanation for the P and N anomalous behavior is needed, although this is usually correlated with the dopant lattice site difference and/or the high implantation-induced lattice damage by P due to heavier atomic mass than N atom. In this work, we carefully investigated the electrical activation of P, N, P+N (identical profiles) and P/N (sequential profiles) implanted 4H-SiC and also considering the first principle calculations for a possible physical mechanism. The P and N implantations were performed at elevated temperatures to minimize implantation-induced lattice damage[3] and subsequently annealed at temperatures in the range of 1200~1700℃ for 30 min. in Ar gas ambient. The electrical activation investigations indicate an order of magnitude lower sheet resistance for P implanted samples compare to the N implanted one at higher annealing temperatures as shown in Fig.1. We also observed that at lower annealing temperature around 1200℃, the sheet resistance for P or N implanted 4H-SiC is relatively higher than that for the P+N or P/N implanted samples (Sheet resistance>1kΩ/sq.). However, at higher activation annealing temperature, there was no remarkable difference in the sheet resistance of the P single or co-implanted 4H-SiC. Sheet resistance of N implanted samples were higher in the entire annealing temperature range. These results indicate that it may be possible to reduce the thermal budget for device processing simply by considering the P and N co-implantation as well as the pn leakage currents by trimming and/or tailoring the implantation profiles.

For a possible physical explanation of the experimental results, we calculated the electronic structure of N and P donor substitutional models. The calculations are based on the local density functional (LDF) approximation and norm-conserving pseudopotential method[4]. A 64-atom cubic super cell structure was considered to study the dopant interactions under the high doses of implanted species. Considering that N has atomic covalent radius and electro-negativity values more close to the C-atom compare to Si-atom. The probability of N to occupy the C-lattice site is very high, compare to Si-lattice site. Earlier, we reported that the N dopant on the C-lattice site (N_C) acts as a shallow donor (ΔE=180meV). Similarly, the probability of P to occupy the Si-lattice site (P_{Si}) is very high in SiC, therefore, acts as a shallow donor (ΔE=680meV). The co-implantation of P and N can extend the maximum obtainable activation by occupying both C- and Si-lattice site, respectively. The calculated square wave function of the half-occupied highest state of considered models, which is equivalent to the donor densities is shown in Fig.2. The donor density of $Si_{32}C_{30}N_2$ models is widely spread over the crystal. The density is high at the anti-bonding sites around Si atoms. The calculated eigen values of substitutional models are summarized in Table-1. The absolute values of the eigen values are not realistic because of the small size of the model ($Si_{32}C_{32}$) considered for the present calculations. The presence of two N atoms in very close vicinity results in the eigen value shift (ΔE_{shift}) of about 140meV. Similarly, the donor density of $Si_{30}C_{32}P_2$ model is also well spread over the crystal and ΔE_{shift} of about 50meV was observed. The difference of electro-negativity between Si and P is less than that of C and N. In $Si_{31}C_{31}PN$ model, as the donor density around N and P have different symmetries, therefore, the overlap between these wave functions is small compare to $Si_{32}C_{30}N_2$ and $Si_{30}C_{32}P_2$ models. The shallow levels will not be disturbed in case of high doses of implanted species.

The ΔE_{shift} of about 20meV and 40meV was observed for N and P, respectively in the $Si_{31}C_{31}PN$ model. These calculations confirm that the co-implantation of P and N can extend the maximum obtainable activation for the n-type SiC doping by implantation. In addition, the excess Si interstitials generated during the P implantation process leads to the formation of C vacancies (V_C) that works as a shallow donor level (ΔE=10meV). The formation of V_C, thus the shallow donor level can explains the observed low sheet resistance for P doped SiC, compare to the N doped one. Also, the possible cause for the lower activation for N doped SiC is either due to the dopant interactions that results in the large ΔE_{shift} or due to presence of excess C atoms in the SiC lattice. The excess C atoms either occupies Si-lattice site (C_{Si}) or interstitial position to form complex defects with substitutional N, which produces a localized electronic state [3,5]. The experimental data also supports the hypothesis that the dopants that occupies the C-lattice site, leads to lower activations as compare to the one that occupies the Si-lattice site.

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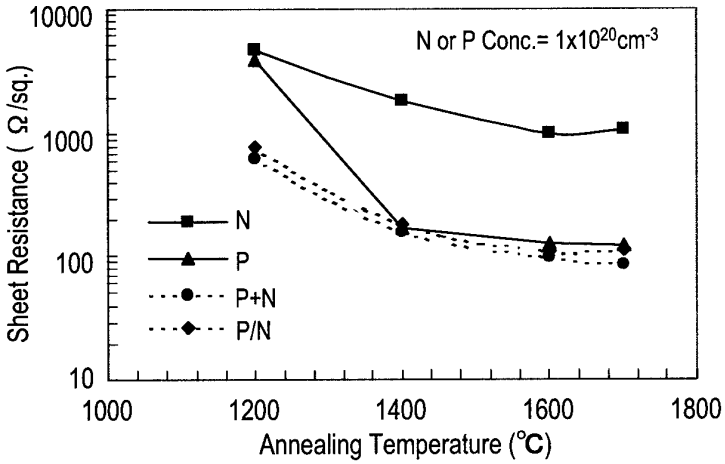


Fig.1 Dependence of sheet resistance of N, P, P+N (identical profiles), and P/N (sequential profiles) implanted 4H-SiC on the activation annealing temperature.

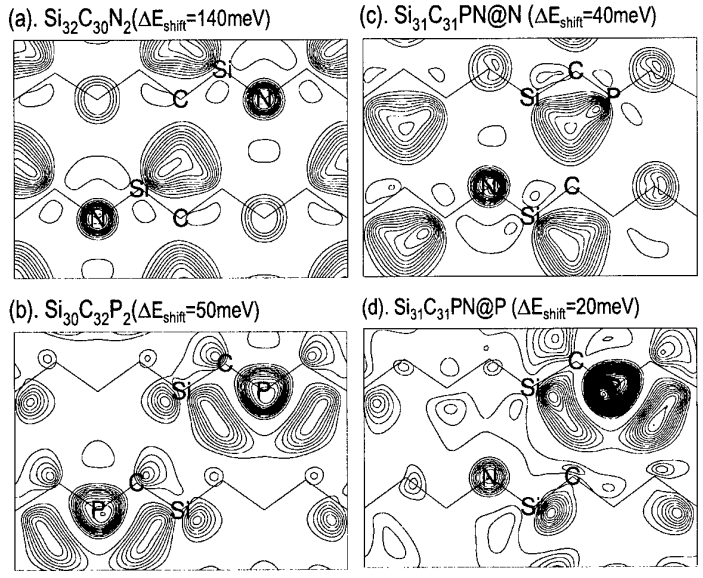


Table-1: Eigen values of impurity states*.

	$Si_{32}C_{31}N$	$Si_{31}C_{32}P$
N-atom (meV)	180	
P-atom (meV)		680

(*64atom super cell cubic model)

Fig.2 Square wave function of the impurity state around the (a) N atom in the $Si_{32}C_{30}N_2$ model, (b) P atom in the $Si_{30}C_{32}P_2$ model, (c) N atom in the $Si_{31}C_{31}PN$ model, and (d) P atom in the $Si_{31}C_{31}PN$ model. The contour spacing is 0.0004au (e/Bohr^3).

Damage evolution and recovery in Al-implanted 4H-SiC

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Epitaxial growth 4H-SiC layers have been implanted with 1.1 MeV Al_2^{2+} molecular ions at a tilt angle of 60° relative to the surface normal to fluences ranging from 1.5×10^{13} to 8.00×10^{14} Al cm^{-2} at 150 K. Isochronal annealing for 20 minutes was performed from 200 up to 870 K. Damage evolution and recovery on the Si and C sublattices have been studied simultaneously using in situ Rutherford backscattering spectroscopy and nuclear reaction analysis along the <0001> channeling direction (RBS/C and NRA/C), as well as at an off-channel direction (RBS/R), with 0.94 MeV D^+ and 2.0 MeV He^+ at a scattering angle of 150° relative to the incoming beam. The in situ RBS/C and NRA/C spectra from samples implanted with various ion fluences are shown in Fig. 1, along with random and virgin spectra. The results indicate the increase in disorder on both the Si and C sublattices with increasing ion fluences. Once the random level is reached, the width of the damage peak also increases with further irradiation.

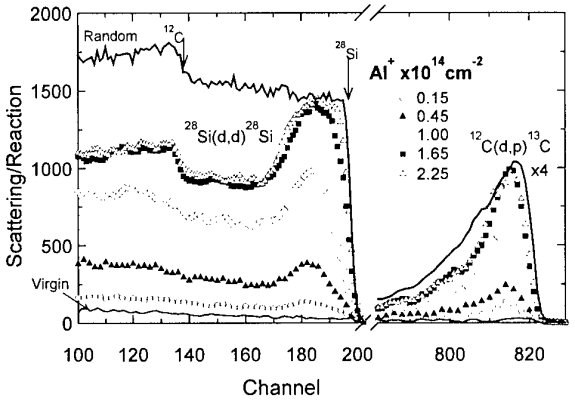


Fig. 1. RBS/C and NRA/C spectra for 4H-SiC irradiated with 1.1 MeV Al_2^{2+} molecular ions to different ion fluences at 150 K measured with 0.94 MeV D^+.

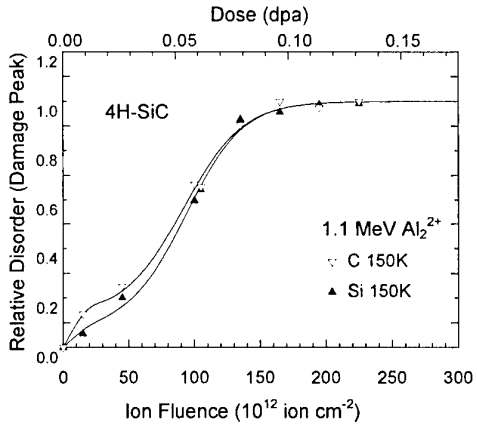


Fig. 2. Relative disorder as a function of ion fluence at the damage peak for 1.1 MeV Al_2^{2+} implanted 4H-SiC at 150 K.

The depth profiles of relative disorder on the Si and C sublattices were determined from the RBS/C and NRA/C spectra using the ratio of aligned spectra to random spectra and correcting for the background dechanneling fraction. The relative disorder on the Si and C sublattices at the damage peak is shown in Fig. 2 as a function of the ion fluence and local dose (dpa). The results indicate a departure at this irradiation temperature from the sigmoidal dependence that is normally observed at higher temperatures. The higher rate of C disordering at low ion fluences is consistent with the low threshold displacement energies for C atoms.

Isochronal annealing was carried out sequentially at temperatures from 200 up to 870 K. The relative residual disorder at the damage peak for both the Si and C sublattices after annealing

is shown in Fig. 3 for 0.45 and 1.65 × 10^{14} Al cm^{-2} samples. Three distinct recovery stages are present in Fig. 3. At low ion fluences (4.5 × 10^{13} Al cm^{-2}), where the damage states are far below the fully amorphous state, two distinct recovery stages are observed on both the Si and C sublattices. The first recovery stage (I) occurs between 250 and 420 K, and the second recovery stage (II) occurs between 470 and 570 K. At intermediate ion fluences (1.65× 10^{14} Al cm^{-2}), where the relative disorder is just below the fully amorphous state, the first stage is largely absent while second stage is still present; however, a third recovery stage (III) is observed between 600 and 700 K. At high irradiation fluences, where a buried amorphous layer is produced (>1.95 × 10^{14} Al cm^{-2}), the onset of a fourth recovery stage (not shown) is observed above 800 K. A more detailed description of the recovery processes over the range of ion fluences from 1.5×10^{13} to 2.25× 10^{14} Al cm^{-2} will be presented, and the recovery stages will be more apparent, since the amount of specific recovery in each stage depends on the initial damage state prior to annealing.

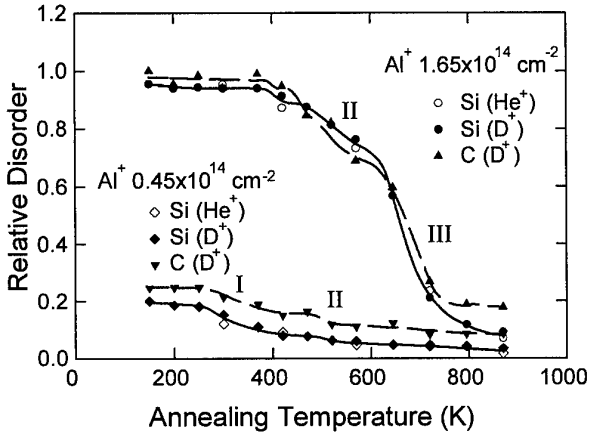


Fig. 3. Isochronal recovery of relative disorder for both Si and C sublattices at the damage peak

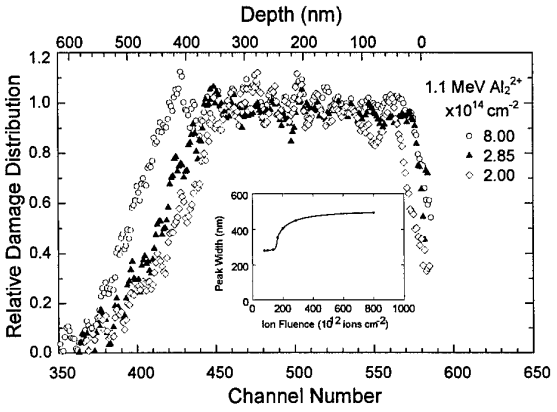


Fig. 4 Profiles of the relative damage distribution along <0001> at 300 K in 4H SiC irradiated with 1.1 MeV Al^{2+}. The inner plot is the width of as-implanted damage peak as a function of ion fluence.

Fig. 4 shows the profiles of the relative damage distribution along <0001> at 300 K for the Si sublattice as a function of channel number and depth in 4H-SiC implanted with high fluences. The inner plot indicates the width (FWHM) of the damage peak or the amorphous layer as a function of ion fluence. The width keeps constant at lower ion fluences, and increases significantly when close to the critical amorphization dose (Fig. 2) of 0.11 dpa or 1.90×10^{14} Al cm^{-2}. The thickness of the amorphous layer increases at a reduced rate with further irradiation. Different thicknesses of the amorphous layers and damage levels just below the surface were produced by irradiation of 2.00, 2.85 and 8.00 × 10^{14} cm^{-2} as shown in Fig. 4. After isochronal annealing, different crystal recovery can be observed. For the lower fluence implanted samples, the crystal recovery occurs from both the front and rear amorphous/crystal interfaces. For the 8.00 × 10^{14} cm^{-2} irradiated samples, the crystal re-growth starts only from the rear interface. The nonlinear temperature dependence of the recrystallization is attributed to distinct recovery processes.

COMPARISON BETWEEN CHEMICAL AND ELECTRICAL PROFILES IN AL^+ OR N^+ IMPLANTED AND ANNEALED 6H-SIC.

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This work compares the measurements of chemical and electrical profiles in ion implanted and annealed 6H-SiC samples. Secondary Ion Mass Spectrometry (SIMS) and Scanning Capacitance Microscopy (SCM) were used to measure the first and the latter profiles, respectively.
6H-SiC <0001> bulk wafers with a carrier concentration in the decades 10^{17}-10^{18} cm^{-3} were used. Al^+ and N^+ ions were implanted in n- and p-type wafers, respectively, at various energies and fluence values so to produce an almost box shape profile about 1 μm thick at the sample surface with a plateaux concentration in the decade 10^{19} cm^{-3}. The implantation and annealing temperatures were 300°C and 1700°C, respectively. The annealing was done in a RF furnace in Ar ambient and was 30 min long.
The structural analysis of the recovered layers showed the presence of a weak density of secondary defects which perturbed the crystal lattice preferentially along the planar (11-20) and (10-10) directions than along the axial <0001> one, as described in [1].
Fig.s 1 and 2 show the comparison between SIMS and SCM profiles for both the p- and the n-type implanted species. The profile shapes qualitatively agree except for the junction depth value. Taking into account that both the diagnostic techniques claim a depth resolution equal to 10-20 nm, such a difference remains a puzzle to solve. This remark can be done: the relative position of the chemical to the electrical junction depth is the same with respect to the n- and p-type sides of any sample.
Hall measurements are in progress to convert the SCM capacitance profiles in carrier density profiles. That is possible because, in spite of the high doping level of the substrates, p/n junction were formed.

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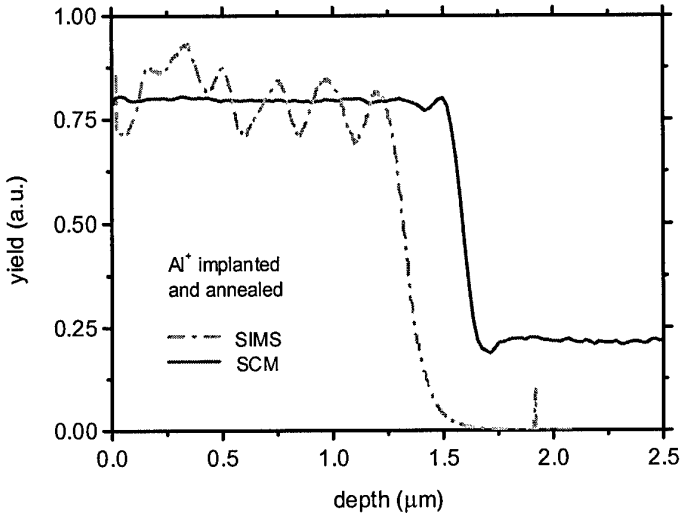


Fig. 1. Comparison between the SIMS and the SCM profiles for the sample Al^+ implanted.

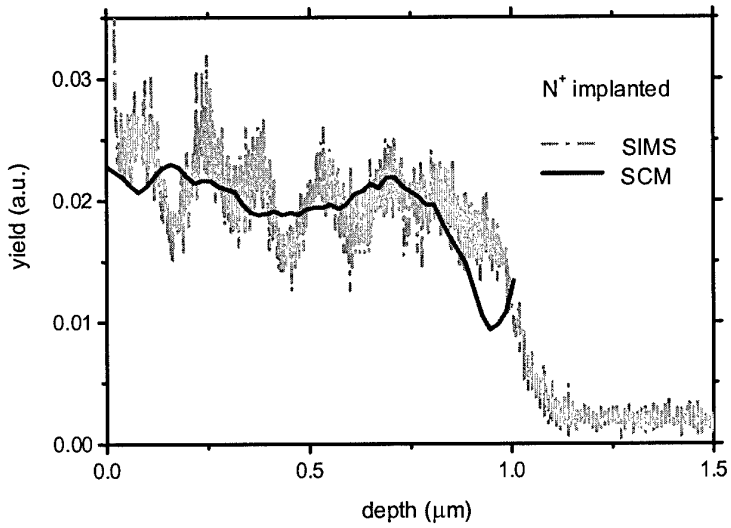


Fig. 2. Comparison between the SIMS and the SCM profiles for the sample N^+ implanted.

POLYTYPE-DEPENDENCE OF TRANSITION METAL-RELATED DEEP LEVELS IN 4H-, 6H AND 15R-SiC

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Besides the known deep level data of Ti, Cr, V in the polytypes 4H- and 6H-SiC [1-4], we present additional results and thus provide an extensive data set about deep levels of transition metals in silicon carbide (SiC). The data were obtained by means of Radiotracer Deep Level Transient Spectroscopy (DLTS) involving radioactive isotopes of the elements of interest. Observing characteristic concentration changes of deep levels during the radioactive decay by means of repeated DLTS-measurements we could definitely identify deep levels of Ti, Cr, V, Ta, and W in the band gap of the three SiC-polytypes investigated (see Fig.1).

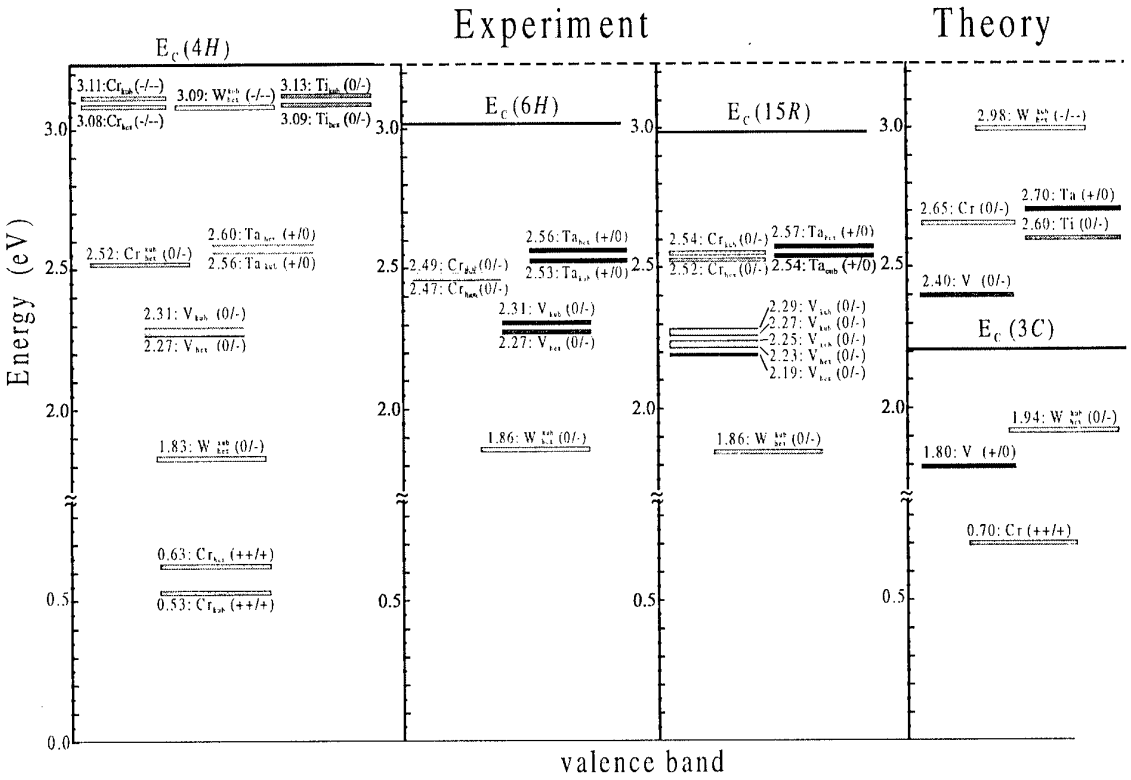


Fig.1: *Energy scheme of the SiC polytypes 3C, 4H, 6H, and 15R. It is based on the assumption, that the valence bands of the SiC polytypes are energetically aligned [6].The trap positions in the band gap of the polytypes are given by their energetical distance to the valence band. The values for 3C-SiC are theoretical predictions [8].*

The level energies of each element in 4H-, 6H-, and 15R-SiC are compared and the conduction band offsets between the polytypes are derived according the Langer-Heinrich rule [5]. Obviously the valence bands of all polytypes are energetically aligned. This fact is also confirmed by other experimental [6] as well as theoretical studies [7]. Considering this information and the rule of Langer and Heinrich we present a comparison between the experimental data and theoretically predicted values [8] for the trap energies of transition metals in SiC. If we also include conduction band resonances, the theoretical and experimental data concerning level energies are in good agreement.

Some transition metals (Cr, V, Ta, Ti) exhibit a level splitting of there corresponding deep state. This splitting is due to the occupation of inequivalent lattice sites in SiC and varies in magnitude depending on the investigated polytype and/or element. Though, the level splitting does not affect the application of rule of Langer and Heinrich in SiC. To energetically align the trap positions it is sufficient to calculate a mean activation energy in each polytype.

For all polytypes investigated (4H-, 6H-, 15R-SiC), the splitting of the V levels is larger than for other elements and increases from 4H-, over 6H- to 15R-SiC. The same tendency is observed for Cr where a splitting is resolved by DLTS in the polytype 15R only.

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Electronic localization around stacking faults in silicon carbide

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In order to fully develop SiC based technology, there are still material problems that need to be understood. One such problem is the occurrence of stacking faults (SF). In general, the SF energy of SiC is believed to be very small (around 3mJ/m^2 and 15 mJ/m^2 for 6H- and 4H-SiC, respectively) compared to other semiconductors such as Si (55 mJ/m^2), diamond (280 mJ/m^2), or GaAs (45mJ/m^2) [1-3]. Because of the small SF energy it is relatively easy to develop extended SF regions in SiC crystals, which, if electrically active, can seriously affect device performance.

We report on a first-principles study of all the structurally different SFs that can be introduced by glide along the (0001) basal plane in 3C-, 4H-, and 6H-SiC (see Fig.1), based on the local-density approximation within the density-functional theory. Our band structure calculations using supercells containing 96 atoms have revealed that both types of SF in 4H-SiC, and two of the three different SFs in 6H-SiC (type I and II), give rise to quasi-2D energy band states in the band gap at around 0.2 eV below the lowest conduction band (see Fig.2), thus being electrically active in n-type material. Although SFs, unlike point defects and surfaces, are not associated with broken or chemically perturbed bonds, we find a strong localization, within roughly 10-15 Å, perpendicular to the SF plane, of the wave functions of the SF gap states in both 4H- and 6H-SiC (see Fig.3). In 3C- and type III SF in 6H-SiC, the states in the immediate vicinity of the valence band maximum show some degree of localization, as do also the states in the vicinity of the lowest conduction band for type III SF in 6H-SiC. These states are less localized, however, than the gap states for the SF of type I and II in 4H- and 6H-SiC. We find that this quantum-well-like feature of certain SFs in SiC can be understood in terms of the large conduction band offsets between the cubic and hexagonal polytypes [4].

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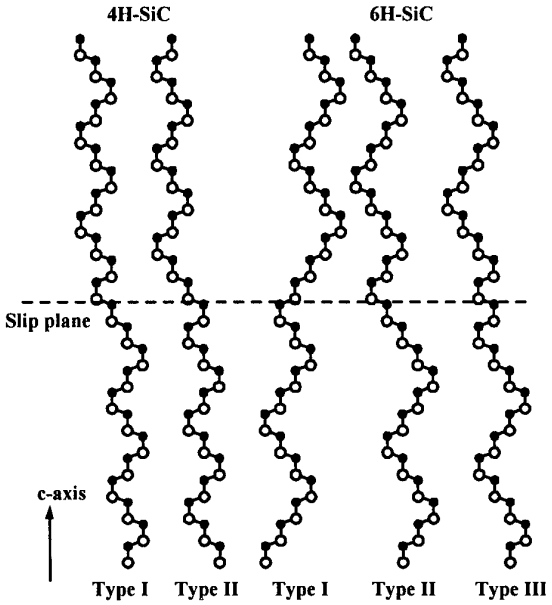


Fig.1. Geometrically distinguishable SFs in 4H- and 6H-SiC

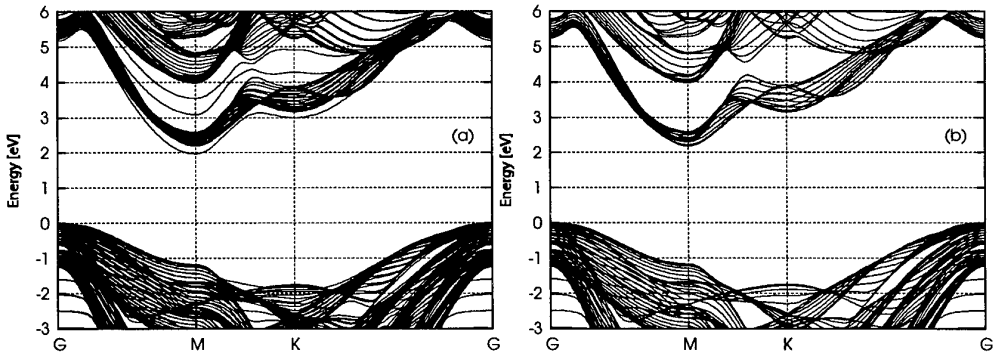


Fig.2. Band structures of 4H-SiC (a) with and (b) without SF of type I.

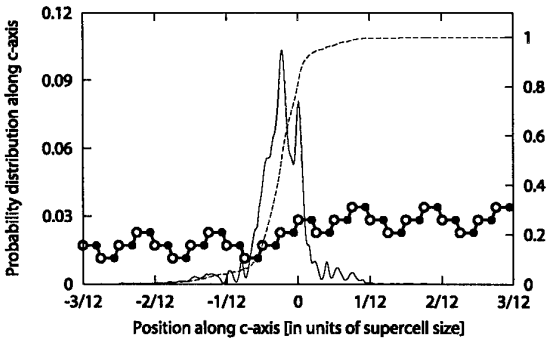


Fig.3. Squared wave function distribution along the c-axis, $f(z) = \iint |\psi(x,y,z)|^2 dxdy$, where the integration for each value of z along the c-axis is performed in the basal plane within the supercell for the wave function at the M-point for the split-off conduction band in 4H-SiC with SF type I. The normalization integral, $I(z) = \int^z f(z')dz'$, is also shown (right y-axis), together with the corresponding stacking sequence.

MoA4 Implantation

[redacted]

Annealing of Implanted Layers in (1$\bar{1}$00) and (11$\bar{2}$0) Oriented SiC

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The ion implantation is of importance for the doping of impurities to SiC in the fabrication of the heavily doped region such as source and drain in field-effect-transistor. However, the high-dose ion implantation to (0001)-oriented SiC accompanied by the amorphization leads to a regrowth inducing 3C-SiC crystals during the post-implantation annealing, as shown in Fig. 1. Therefore, the ion implantation to (0001)-oriented SiC has been performed at the elevated sample temperature or at the low dose, which would restrict the device process of SiC.

For the (0001)-oriented SiC, the regrowth of 3C-SiC from the implantation-induced amorphous layer is attributed to the lack of the atomic stacking sequence at the amorphous-crystalline substrate (a/c) interface. For the (1$\bar{1}$00)- and (11$\bar{2}$0)-oriented SiC, however, the atomic stacking sequence of the polytype structure is preserved at the a/c interface even if the amorphous layer is formed by the high-dose implantation. Author and co-workers reported that the implantation-induced amorphous layers on (1$\bar{1}$00)- and (11$\bar{2}$0)-oriented SiC are recrsytallized to the original polytype structure according to the underlying substrate during the post-implantation annealing[1-3]. Figure 2 shows Rutherford backscattering (RBS) spectra and the electron diffraction taken from the (1$\bar{1}$00)-oriented 6H-SiC implanted with 100 kev Ar ions at 2 x 10^{15} /cm^2 at room temperature. RBS spectra reveal that the implantation-induced amorphous layer is recrystallized by annealing at 1000 °C for 5 min. The electron diffraction shows the polytype of the regrown layer is identical to that of the underlying substrate. Also, for the (11$\bar{2}$0)-oriented SiC, the implantation induced amorphous layer is recrystallized to the original structure and the similar results have been obtained for the implantation to 4H-SiC. These results suggests that the high-dose implantation to the (1$\bar{1}$00)- and (11$\bar{2}$0)-oriented SiC can be carried out at room temperature.

The series of spectra shown in Fig. 3 show the reduction in thickness of the amorphous layer as a function of annealing time for the (11$\bar{2}$0)-oriented 6H-SiC at 750 °C[4]. The a/c interface on (11$\bar{2}$0)-oriented 6H-SiC shifts to the surface in equal thickness interval for equal time intervals indicating a uniform regrowth velocity. The regrowth rate at 750 °C is estimated to be 3.5 nm/min. The reduction in thickness of the amorphous layer can be observed by the annealing above 700 °C. The successive decrease of thickness of the amorphous layer indicates that the implantation-induced amorphous layer is epitaxially regrown by annealing above 700 °C. Figure 4 shows the Arrhenious plots of the regrowth rate for (1$\bar{1}$00)-, (11$\bar{2}$0)- and (0001)-oriented 6H-SiC[4,5]. In the case of (0001) SiC, the regrowth rate of 3C-SiC is not uniform. The activation energy of the regrowth rate for the amorphous layer on 6H-SiC is estimated to be 3.4 eV, which is independent to the crystal orientation. The obtained results for the regrowth of the amorphous layer on (1$\bar{1}$00)- and (11$\bar{2}$0)-oriented SiC suggest that the implantation damage can be annealed out at temperatures below 1000 °C.

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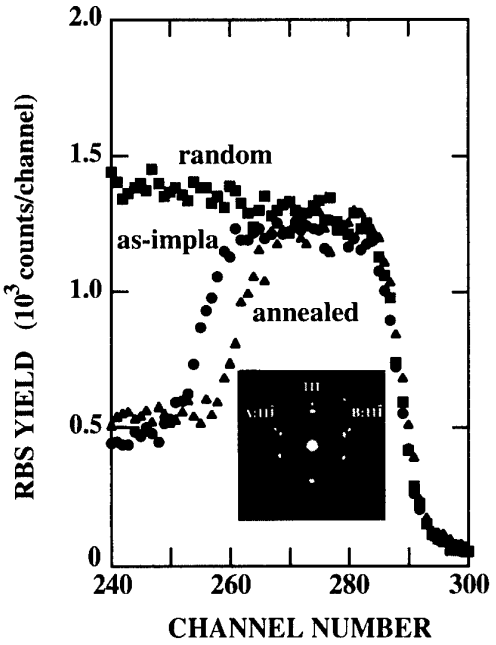


Fig. 1: RBS spectra taken from the 100 keV Ar ($2 \times 10^{15}/cm^2$) implanted 6H-SiC(0001) before and after annealing at 950 °C for 30 min. The electron diffraction shows that the amorphous layer is recrystallized to 3C-SiC.

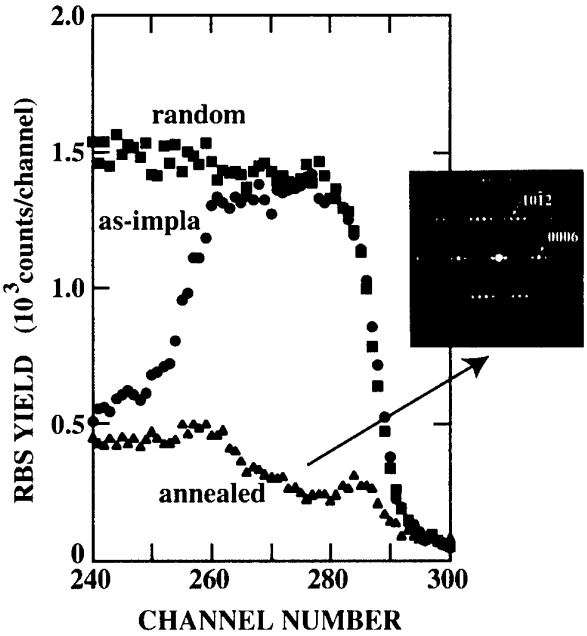


Fig. 2: RBS spectra take from 100 keV Ar ($2 \times 10^{15}/cm^2$) implanted 6H-SiC($1\bar{1}00$) before and after annealing at 1000 °C for 5 min. The electron diffraction shows that the regrown layer is 6H-SiC.

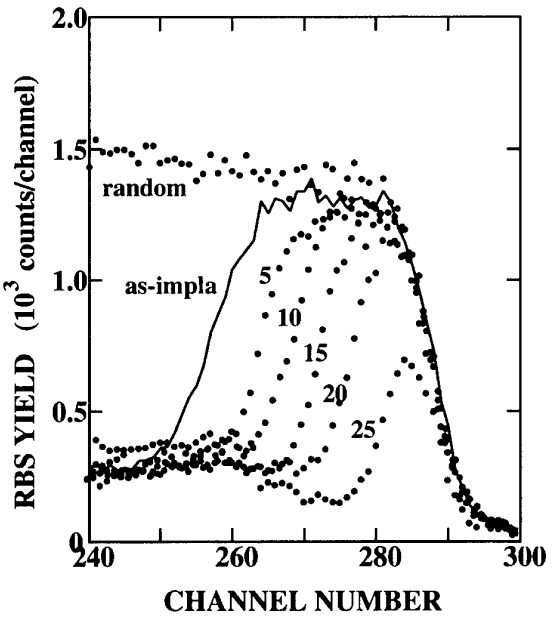


Fig. 3: RBS spectra taken from 100 keV Ar ($2 \times 10^{15}/cm^2$) implanted 6H-SiC($11\bar{2}0$) as a function of annealing time at 750 °C. The numbers in figure represent the annealing time in minutes.

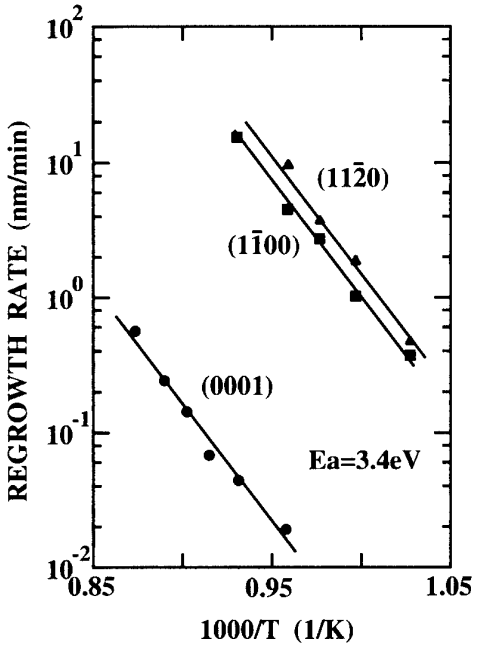


Fig. 4: Arrhenious plots of the regrowth rate of the amorphous layer in 6H-SiC. The amorphous layer on 6H-SiC(0001) is recrstallized to 3C-SiC.

Codoping of 4H-SiC with N- and P-Donors by Ion Implantation

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In order to reduce the series resistance in SiC-based power devices, highly doped areas are required. In the case of n-type SiC, usually nitrogen (N) atoms residing at carbon lattice sites [1] are employed as the dominating donor. For N concentrations [N] greater than $2x10^{19}$ cm^{-3}, the incorporated N atoms start to form partially electrically inactive centers (probably precipitates) and, in addition, such SiC wafers show a high internal tension and become easily brittle.

One possible way to increase the conductivity in n-type SiC and to simultaneously avoid the drawbacks of high N concentrations - as described above - is the codoping of SiC by nitrogen and phosphorus (P). P atoms also act as donors residing, however, at Si lattice sites [2]. They have an ionization energy which is close to the ionization energy of N donors [3, 4].

In this paper, we successfully demonstrate codoping by implantation of N and P. Identical box profiles of N and P to a depth of 1.3 μm are generated by multiple implantation. We have implanted two sets of p-type 4H-SiC epilayers (N_{Al}-N_{comp} = $4x10^{16}$ cm^{-3}) with different mean donor concentrations:

Implantation 1 : [N] = [P] = $1x10^{18}$ cm^{-3} / Implantation 2 : [N] = [P] = $2x10^{19}$ cm^{-3}

Each set consists of sample a), sample b) and sample c) implanted with N, P and (N+P), respectively. All the samples have been annealed in a SiC container at 1700°C for 30 min resulting in a complete electrical activation of implanted ions. The parameters of implanted donors have been determined by Hall effect investigations in van der Pauw arrangement. In order to avoid leakage currents over the implanted n-p junction, mesa structures have been fabricated by reactive ion etchting. Results of the Hall effect analysis are summarized in Table I and partially revealed in Figs. 1 and 2; the main features are:

1. The total implanted concentration [N+P] is electrically active.
2. Implantation 1 and 2 (samples c)) result in low resistivities of 0.05 Ωcm and 0.014 Ωcm, respectively, at 300K.
3. At identical implanted concentration, the Hall mobility in P-implanted layers is higher than in N-implanted layers in the temperature range from 80K to 400K (not shown here).

Hot N/P-coimplanted samples at total mean concentrations of [N+P] > 10^{20} cm^{-3} are in process, the corresponding Hall effect results will be compared with those, which are taken on layers only implanted with N at identical concentrations.

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Table I.
Donor parameters determined by fit of the neutrality equation to the measured Hall effect data taken on (N+P)-coimplanted samples c). $\Delta E(h)$, $\Delta E(k)$ denote the ionization energy of donors residing at hexagonal (h) or cubic (k) lattice site. $N_D(h/k)$ denotes the total donor concentration. ρ and $\mu_{H,e}$ are the room-temperature (RT) values of resistivity and electron Hall mobility, respectively.

Hall effect parameter	Implantation 1 sample c)	Implantation 2 sample c)
$\Delta E(h)$ (meV)	59	26
$\Delta E(k)$ (meV)	103	
$N_D(h/k)$ (cm^{-3})	1.9×10^{18}	4.3×10^{19}
ρ at RT (Ωcm)	0.05	0.014
$\mu_{H,e}$ at RT (cm^2/Vs)	170	42

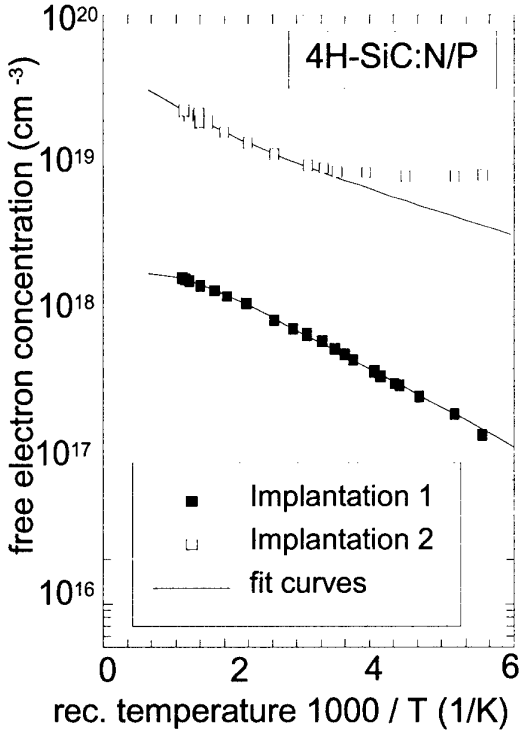


Fig. 1. Free electron concentration as a function of the reciprocal temperature obtained from Hall effect measurements on the (N+P)-codoped samples c). Symbols represent the experimental data (filled squares: implantation 1, open squares: implantation 2). The solid lines correspond to a least-squares-fit of the neutrality equation to the experimental data. The fit parameters are given in Table I.

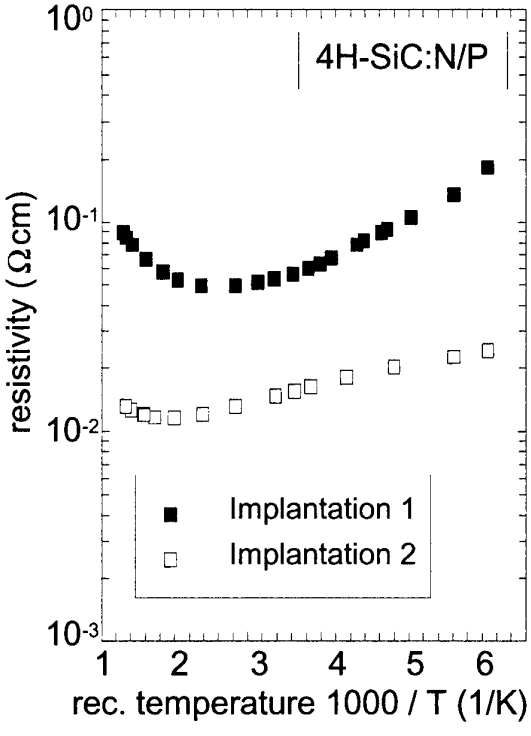


Fig. 2. Resistivity as a function of the reciprocal temperature. Filled squares correspond to implantation 1 sample c), open squares to implantation 2 sample c).

Phosphorus Implantation into 4H-SiC (0001) and (11$\bar{2}$0)

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To form selective n^+ regions in SiC, phosphorus ion (P^+) and nitrogen ion (N^+) implantation are commonly employed. Recently P^+ implantation, instead of N^+ implantation, has attracted increasing attention to obtain lower sheet resistances. P^+ implantation at an elevated temperature followed by annealing at a high temperature above 1600 °C is effective to reduce sheet resistances [1, 2]. However, a recent report has shown that when activation annealing is performed at a high temperature in Ar, considerable roughening and macrostep formation is observed [3]. To establish a similar process in Si technology, the major challenges include successful implantation at RT, the reduction of annealing temperature, and keeping surface flatness during annealing processes. In this work, the authors demonstrate that SiC (11$\bar{2}$0) may be a solution to meet these requirements.

P-type 4H-SiC (0001) and (11$\bar{2}$0) epilayers with an acceptor concentration of $1\sim5\times10^{16}$ cm^{-3} grown in the authors' group were used in this study. Multiple implantation of P^+ was carried out to obtain a 0.25 μm-deep box profile of P (10~180 keV, total dose: 4×10^{15} cm^{-2}) or a 0.45 μm-deep box profile of P (10~360 keV, total dose: 1×10^{16} cm^{-2}). The implantation temperature was RT or 800 °C. Post-implantation annealing was performed at 1100~1700 °C for 30 min in Ar ambience. The electrical properties of implanted regions were characterized by Hall effect measurements using the van der Pauw configuration at RT. The implantation-induced damage was analyzed by RBS channeling measurements with a 2.0 MeV He^{2+} primary beam.

Figure 1 (a) shows the aligned spectra of as-implanted and 1700 °C-annealed 4H-SiC (0001) samples. The aligned yields of the damaged region (channel number: 230-280) are close to the random yields in the case of RT-implantation without annealing. Although the yields decrease by annealing at 1700 °C, severe damages near the surface still remain. In contrast, the damage is considerably decreased for a 800 °C-implanted and 1700 °C-annealed sample. Figure 1 (b) shows the aligned spectra of 4H-SiC (11$\bar{2}$0) samples implanted at RT followed by annealing at 1700 °C. The figure demonstrates that implantation-induced damages are reduced down to the virgin (unimplanted) level even with RT-implantation followed by annealing at 1700 °C. This indicates that significantly better lattice recovery is realized in 4H-SiC (11$\bar{2}$0) than (0001), owing to a much faster recrystallization rate along the $\langle11\bar{2}0\rangle$ direction [4]. Thus, 4H-SiC (11$\bar{2}$0) may possess much potential to reduce implantation and annealing temperature.

Figure 2 shows an AFM image of RT-implanted and 1300 °C-annealed 4H-SiC (11$\bar{2}$0) sample. The surface exhibits a smooth surface as observed even by an AFM. The surface was mirror-like, and the value of root-mean-square (Rms) surface roughness was as low as 1.5 nm (10×10 μm^2).

Figure 3 shows the measured sheet resistance of P^+-implanted regions as a function of annealing temperature. In the case of 800 °C-implantation into 4H-SiC ($11\bar{2}0$), the sheet resistance takes a minimum value of 27 Ω/□ at an annealing temperature of 1700 °C. This is the lowest value ever reported. RT-implantation into ($11\bar{2}0$) resulted in significantly lower sheet resistances compared to RT-implantation into (0001). A reasonable sheet resistance of 460 Ω/□ was obtained even by RT-implantation followed by 1300 °C-annealing, when ($11\bar{2}0$) was employed. This may bring considerable improvement in SiC device processing technology as well as device performance.

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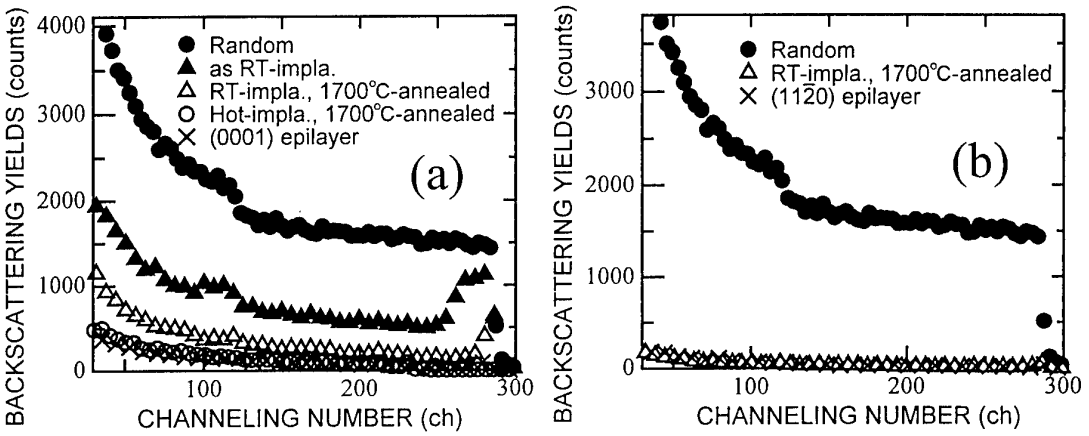


Fig. 1. RBS spectra of 4H-SiC layers before and after annealing. P^+ implantation was done with a total dose of 4×10^{15} cm^{-2} at RT and 800℃: (a) 4H-SiC (0001), (b) 4H-SiC ($11\bar{2}0$). The spectrum of a virgin sample is also shown as reference.

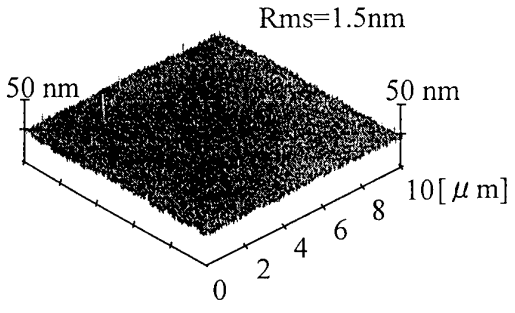


Fig. 2. AFM image of RT-implanted and 1300℃-annealed 4H-SiC ($11\bar{2}0$).

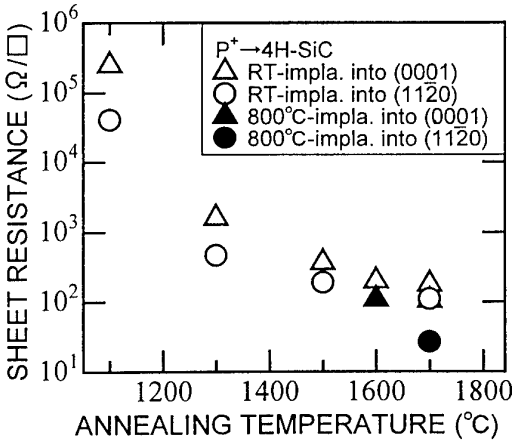


Fig. 3. Dependence of sheet resistance on annealing temperature of P^+-implanted 4H-SiC (0001) and ($11\bar{2}0$).

Low temperature activation of the ion-implanted dopants in 4H-SiC by excimer laser annealing

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Annealing process at extremely high temperature (>1500°C) for the activation of the ion-implanted dopants in SiC causes some serious problems, e.g. the evaporation of the surface atoms and the redistribution of the ion-implanted dopants. Therefore it has been expected that a new annealing process at low temperature below 1000°C will be developed. Excimer laser annealing will be a very hopeful technique to activate the ion-implanted dopants in SiC at low temperature. Although several groups[1],[2] reported the effect of the laser annealing of the ion-implanted SiC, there was a little description of the electrical property. Hishida et al.[3] reported the effect of the excimer laser annealing(XeCl) in Al^+ and N^+ implanted 6H-SiC. Howevere, in their study the activation efficiencies in both cases were too low to apply the laser annealing to SiC device process instead of the furnace annealing. In this study, by the improvement of the condition of the ion implantation and the excimer laser irradiation we succeeded to achieve extremely high activation efficiecy of phosphorus(P^+) ion-implanted 4H-SiC at low temperature as ~800°C.

In this study we used 4H-SiC(0001) wafer with epitaxial layer (p-type, N_a-N_d~ $5.0\times10^{15}/cm^3$, Si-face, 8° off, 5μm thickness) purchased from Cree Research Inc. and cut them into $4\times4mm^2$ for the P^+ ion implantation. To make a box profile layer we performed the multiple energy ion implantation in the energy range of 30-100keV with the total dose of $5.7\times10^{15}/cm^2$. The substrate was heated at 500°C during the ion implantation in order to prevent the amorophization of the implanted layer. The implanted sample was irradiated by XeCl excimer laser (λ=308nm) in ultra high vacuum chamber(3.0×10^{-7}Torr). The laser irradiation was carried out by 4 steps as shown in Table 1. By using this "step irradiation" method the photon energy is effectively provided to the ion-implanted layer without surface evaporation. During the laser irradiation the substrate was heated from room temperature to 800°C to investigate the combination effect of the laser annealing and the thermal annealing.

Figure 1 shows the substrate temperature dependence of the free electron concentration and sheet resistance of the laser annealed samples. Those of the furnace annealed sample at 1600°C for 5min in Ar ambient are also shown in this fiugure. Although the implanted phosphorus was electrically activated even at room temperature, the free electron concentration is considerably lower than that of the furnace annealed sample. The free electron concentration, however, abruptly increases above 500°C and reaches $2.95\times10^{20}/cm^3$ at 800°C which corresponds to three times as much as that of the furnace annealed sample. At the same temperature sheet resistance is 164.7Ω/□ enough to use for the source or dorain

	step 1	step 2	step 3	step 4	total
Energy density [J/cm^2]	0.8	1	1.2	1.3	
shots	600	600	600	600	2400

Table 1 Condition of the excimer laser irradiation : the excimer laser was irradiated on the implanted sample by 4 steps from low to high energy density.

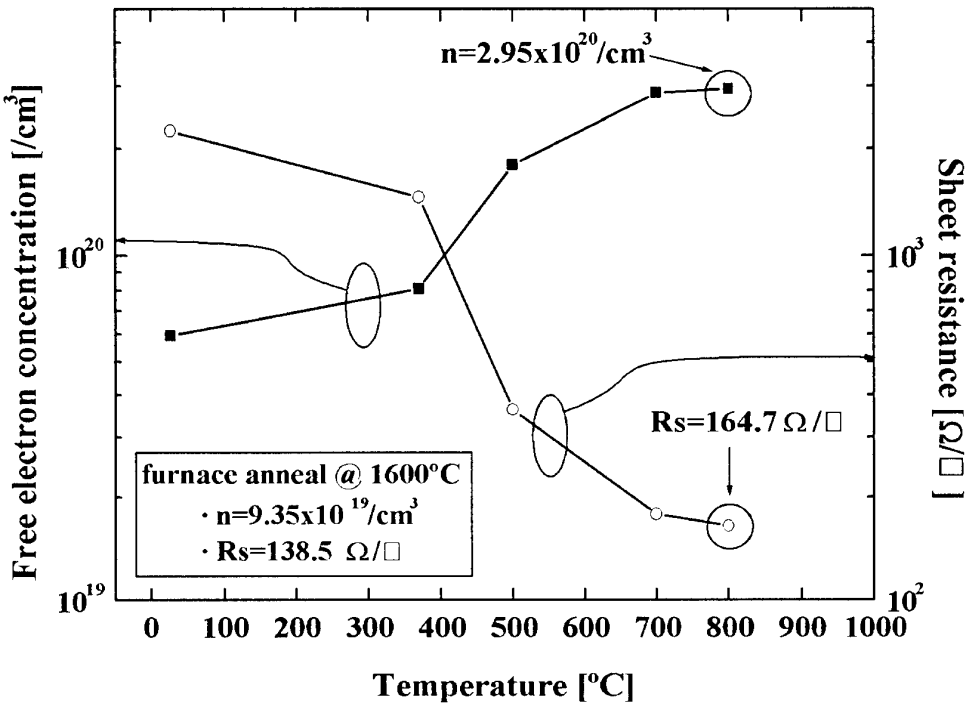


Figure 1 Substrate temperature dependence of the free electron concentration and sheet resistance of the laser annealed samples. Those of the furnace annealed sample are also shown in this figure.

region in SiC-MOSFET or MESFET. The further reduction of seet resistance will be expected by optimizing the condition. From the results of SIMS and AFM there are no redistribution of the dopants and no surface roughness that is observed in the furnace annealed sample. In the presentation I will also talk about the electrical property of pn-junction fabricated by the laser annealing.

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Low-Dose aluminum and boron implants in 4H- and 6H-SiC

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Due to the difficulty of fabricating doped layers in SiC by diffusion, doping of SiC by implantation has been studied extensively. To date, most research on n- and p-type implants has concentrated on heavily doped layers suitable for transistor source/drain regions, ohmic contacts, etc. [1]. Here we report on boron and aluminum p-type implants in 4H- and 6H-SiC at low doses suitable for active regions in SiC power devices.

For this work two main types of samples have been fabricated: (a) MOS capacitors, fabricated on p-type SiC substrates, used to obtain depth profiles of the activated acceptor concentrations, and (b) Hall bars, fabricated on n-type substrates, used to obtain free hole densities and hole mobilities as a function of temperature. In addition, samples from the same wafers were obtained for SIMS measurements of implanted profiles and for AFM studies of surface roughness. Multiple-energy implants were performed on heated substrates to obtain "box" profiles with doping densities of ~$1x10^{17}$ /cm^3 and ~0.5 μm thick. Anneals at 1300-1500°C were performed in an argon ambient, while anneals at 1600°C were performed in a silicon-overpressure ambient.

Due to limited space, we present here a few selected (mostly 4H) experimental results:

- The best results for surface roughness (<0.3 nm rms) were obtained using a si-overpressure ambient at 1600°C, independent of the type of implant or the SiC polytype.
- SIMS results show good correlation between implanted B profiles and simulations (Fig. 1) at all anneal temperatures. Some depletion of the boron is clearly observed at the surface.
- Excellent, uniform activation of implanted Al is observed for anneal temperatures ≥ 1400°C (Fig. 2). The calculated activation rate is ~75% (4H-SiC). Despite this high activation rate, high quality layers are not produced in 4H for anneals below 1600°C (see Fig. 4). Poor activation is obtained at 1300°C.
- Activation of implanted boron is much smaller (at ~10-20%) compared to Al, as is well-known. Surprisingly, however, the activation rates appear to depend on position (Fig. 3). Peaks in the activated boron correlate with the implant peaks for each implant energy.
- Hall measurements have been made over a wide temperature range (150K - 400°C) in order to determine free hole densities and hole mobilities in the implanted layers. Free hole density is shown as a function of inverse temperature in Fig. 4. From these data and standard models [1], it is possible to extract the true density of activated acceptors and the levels of compensation (which presumably arise from un-annealed implant damage). For example, from the fit of the model to the data in Fig. 4, within experimental accuracy, ~100% of the implanted Al ions are activated. However, about 25% of the doping is compensated with deep donors even for the highest anneal temperature (1600°C). The level of compensation is much higher for anneal temperatures at or below 1500°C, implying that anneal temperatures of ~1600°C or higher are necessary to produce near-device-quality layers.
- Hole mobilities have been measured as a function of temperature for both B and Al implants.

Mobilities close to bulk values are observed at $T \geq 400K$. At $200 \leq T \leq 400K$, hole mobilities are considerably reduced compared to bulk, probably due to scattering from charged compensating defects. Interestingly, hole mobilities in B-implanted layers are up to 30% higher compared to Al-implanted layers at low temperatures (~250K), suggesting that there are fewer compensating defects in B-implanted layers.

In summary, device-quality, lightly doped p-type layers can be fabricated by B- and Al-implantation using Si-overpressure annealing at 1600°C for both 4H- and 6H-SiC. Aluminum implants would be preferred when a known doping profile is required, e.g., for the p-well of a DMOS power FET [2], due to the low post-implant diffusion and high activation of Al. On the other hand, higher quality layers, with higher hole mobility and reduced compensation, are obtained with boron implantation, which may be preferable for other applications.

Acknowledgement: This work was partially supported by Dr. G. Campisi of ONR.

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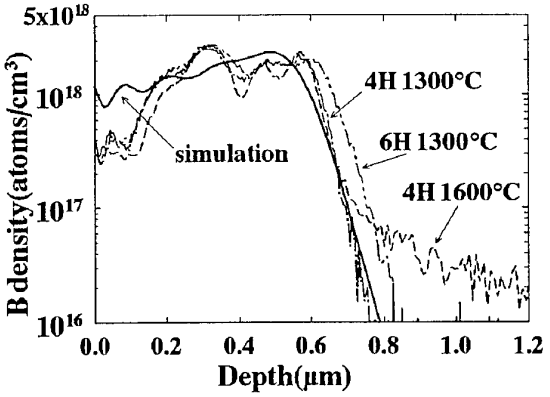


Fig. 1: SIMS profile of Al implants in 4H- and 6H-SiC vs. anneal temperature.

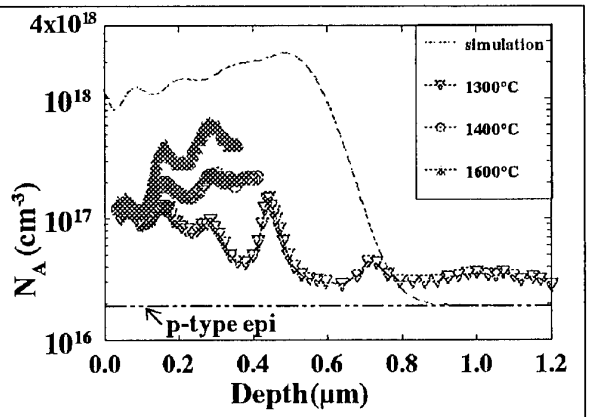


Fig. 3: Depth profile of activated implanted B acceptors vs. anneal temperature.

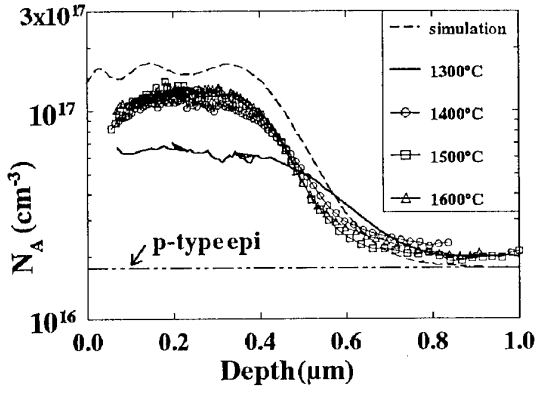


Fig 2: Depth profile of activated Al acceptors vs. anneal temperature (from C-V).

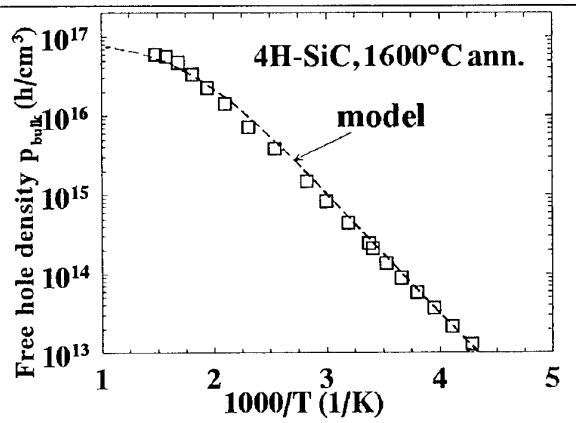


Fig. 4: Comparison of free hole density in Al-implanted layer to theoretical model.

Comparison of Al and Al/C Co-Implants in 4H-SiC Annealed with an AlN Cap

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Implants into SiC can be activated only at temperatures at which silicon also preferentially evaporates at detectable rates and modifies the surface region - the region that is often being probed. The problem is most severe when the samples are annealed in a vacuum or in argon, but even when the samples are annealed in a silane over pressure or in the presence of SiC powder, silicon evaporates at the same rate; only the silicon deposition rate increases. The process of recovery and evaporation go on simultaneously, and one affects the other so the state of activation is determined by the annealing atmosphere as well as the time and temperature. Also, the evaporation will completely dominate the process unless severe limits are placed on the annealing times and temperatures that can be used. This greatly limits the range of times and temperatures that can be studied.

We have developed a method that impedes the evaporation of silicon by using an AlN cap that is stable up to ~1600°C, does not react with the SiC, and can be removed preferentially with a KOH etch. Not only does this enable us to minimize the effects of silicon out-diffusion, we can also use higher temperatures for longer times which allows the sample to more closely approach its equilibrium state. In this paper we examine and compare how annealing 4H-SiC box implanted to a depth of 0.3 μm with 10^{20} cm^{-3} Al or co-implanted with 10^{20} cm^{-3} Al and 10^{20} cm^{-3} C between 1300 and 1700°C affects the electrical and optical properties of the material. This is done by measuring the sheet resistance as a function of temperature, recording the electron paramagnetic (EPR) spectra, and examining the low temperature cathodoluminescence (CL) spectra.

The log of the sheet resistance versus annealing temperature plots in Fig. 1, show that the implants do start to become electrically activated at annealing temperatures ~1400°C. The percent activation in the co-implanted sample is significantly larger after the 1400 and 1500°C anneal compared to the Al implant. However, the resistance of the co-implanted sample is higher after the 1600°C anneal than it is after the 1500°C anneal, whereas the resistance of the Al implanted material continues to decrease as the annealing temperature increases, and it is now lower than that of the co-implanted sample.

This suggests that some of the Al dopants in the co-implanted material have ceased to be electrically active as the material more closely approaches its equilibrium configuration. One explanation is that the solubility of Al in the more C rich region is smaller and that some of the Al has precipitated out, possibly as Al_4SiC_4. We show that this explanation is consistent with dilute solution theory as Al is less soluble in C than it

is in Si due, in part, to the strong Al - C bonds. The greater degree of electrical activation in the co-implanted sample at the lower annealing temperatures can be explained by a smaller activation energy required to form a precipitate than to occupy a Si site in a solid solution. This implies that the Al can be an electrically active dopant when it is in an activated complex as it moves from its as-implanted state towards its equilibrium position.

That the Al atoms are "in transit" to their equilibrium positions is supported by the observation that the Al_{Si} EPR signal is not detected in either type of sample even after the 1600°C anneal. We estimate that we would be able to detect this signal near 2777 G if only 1% of the Al atoms were at equilibrium Si sites. Rather, a broad signal centered near 3100 G is observed in some samples. Interestingly, the signal is detected at different annealing temperatures for the two types of samples. It is observed in the as-implanted Al doped sample, as well as in the Al doped samples annealed at 1300 and 1500°C. In the co-implanted samples this signal was detected in the wafers annealed at 1400 and 1600°C. There is virtually no anisotropy in this signal suggesting that the paramagnetic defect centers responsible for it are not strongly bonded to the crystal lattice.

This annealing technique also enables one to obtain well defined CL spectra to complement the paucity of data on the 4H polytype as most of the data in the literature is for 6H-SiC. Examples are the 5 and 10 KeV spectra for the Al implanted sample annealed at 1300°C shown in Fig.2. In addition to the pair of D_I peaks near 2.9 eV and the D_{II} peak near 3.2 eV and its phonon replicas between 3.2 and 3.05 eV, there are peaks near 3.0, 3.25 and 3.35 eV. One of the many interesting trends we observe is that the height of the higher energy peak in the doublet near 2.9 eV increases with the annealing temperature, and for the same annealing temperature its relative height is larger in the co-implanted samples. Because each peak is thought to be associated with inequivalent atomic sites, one can possibly decipher what sites they are by learning what is happening during the annealing process.

We should soon be able to shed more light on what these processes are as we have recently learned how to anneal wafers at 1700°C by capping the AlN cap with an Al_2O_3 cap. We expect to have the electrical and optical data for samples annealed at this temperature by the time of the meeting. RBS is also being done on these samples.

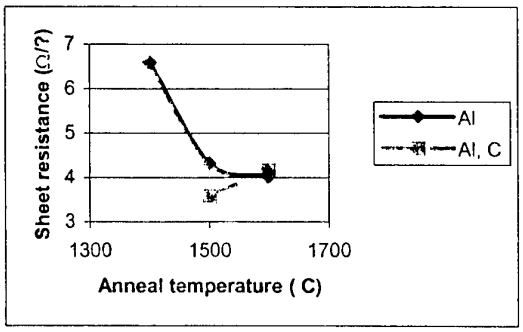


Fig. 1. Sheet resistance of Al and Al, C co-implanted samples plotted as a function of their annealing temperatures.

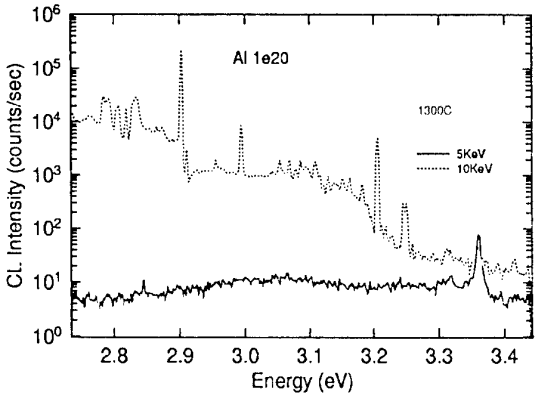


Fig. 2. 5 and 10 KeV CL spectra of the Al implanted sample annealed at 1300°C.

MoB4 Structural Defects

[redacted]

Structural Defects in Electrically Degraded 4H-SiC pin Diodes

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Abstract

One of the proposed main applications for SiC devices is in high power systems such as voltage source converters in motors or HVDC transmission systems. For this kind of applications, the stability of the processed device is crucial. Recently it was shown that some devices can become electrically degraded during long term operation and that this degradation is related to the formation of structural defects in the material. [1] At this stage a comprehensive knowledge of the actual structure of the defects and most of all, the nucleation source for these, is required for a successful outcome of the SiC bipolar device technology. In this work the structural defects in degraded 4H-SiC pin diodes were studied by synchrotron white beam X-ray topography (SWBXT), scanning electron microscopy (SEM) with *in situ* cathodo luminescence (CL) and transmission electron microscopy (TEM).

Figure 1 displays a back-reflection topograph obtained from a reflection towards $<01\bar{1}l>$ of a degraded diode (edges outlined) as recorded by SWBXT. This image outlines triangular areas of dark contrast which are interpreted as stacking faults.

Figure 2a shows a TEM image of a cross-sectional sample prepared by FIB. The picture was taken in a condition where the SiC $<1\bar{1}00>$ crystal zone-axis was parallel to the electron beam. The straight line seen in Figure 2a makes an angle of about 8° with respect to the surface. This shows that the defect is a stacking fault residing on the SiC basal plane. Figure 2b shows another area of the sample where also sets of parallel stacking faults were present. A defect was studied by high-resolution electron microscopy and the results are shown in Figure 2c. The image was obtained by orienting the $<2\bar{1}\bar{1}0>$ zone axis in a condition so as to be parallel to the electron beam. It can be seen that the 4H stacking sequence **ABACABAC** is replaced by **ABCBCACB**.

We show that the particular stacking fault crystal defect is formed from an existing dislocation which splits into two partial dislocations resulting in a glide type [2] slip on the close packed (0001) basal plane. The slip is nucleated from a stress, acting upon the SiC epilayer, originating from the contact/epilayer interface. [3]

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Figure 1. This image was recorded from a reflection towards $<10\bar{1}0>$. The diode edges are outlined and a dark contrast appears in the area of the triangular stacking fault.

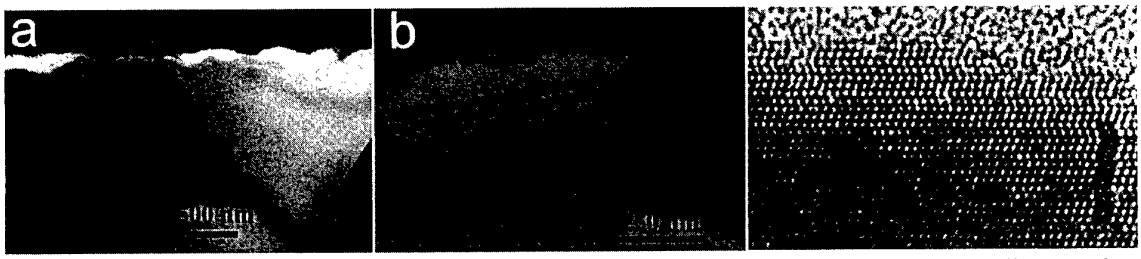


Figure 2. TEM image of the sample prepared by FIB. A straight line corresponding to the stacking fault runs through the crystal in a) and in b) this set of stacking faults was found. A high resolution TEM image of the defect is finally shown in c).

Propagation of Current-Induced Defects and Forward Voltage Degradation in 4H-SiC PiN Diodes

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Bipolar semiconductor devices stand to benefit greatly by replacing silicon with SiC, especially in high-voltage and high-temperature applications. In addition to the increase in performance afforded by the physical properties of SiC, SiC devices are expected to exhibit higher tolerance to extreme ambient conditions. For these devices to be used in industrial or military applications, their stability and reliability must be proven. Recently, long-term reliability tests of 4H-SiC PiN diodes have indicated that while leakage currents remain stable at constant reverse bias, some devices exhibit increased forward on-state voltage with time under constant forward current [1].

This paper investigates current-induced defect propagation in implanted anode 4H-SiC PiN diodes fabricated on 10-15 μm n-type epi layers grown on n^+ substrates. The p^+ anode, three-zone p-type junction termination extension (JTE), and n^+ field stop were sequentially implanted achieving a planar device structure. The anode area is 6.3×10^{-3} cm^2. Devices with windows in the anode metallization were also incorporated to allow for the observation of light emission across the device under electrical bias.

The characteristics of defect propagation have been examined by combining electrical measurements with optical imaging of the defects. Two striking features were that the degradation of diodes on the same wafer can vary by an order of magnitude and that the degradation varied smoothly as the wafer is traversed. Long-term electrical test data from a row of diodes from wafer center (0,0) to wafer edge (-10,0) are shown in Fig. 1. These devices have an anode with a continuous metal overlay. At room temperature, with a stressing current of 0.5 A (80 A/cm^2) the voltage degradation ranged from 0.2 to 2 V. The voltage increase with time for this set of diodes is shown in Fig. 2. While the magnitudes of the voltage increases were very different, all exhibit the most rapid increase within the first few hours and changed much less slowly after 5 hours. Fig. 3a-f shows a sequence of images for one of the window anode devices where the diode is held in forward bias at a constant current of 0.5 A (80 A/cm^2) at room temperature. The images show dark line features in the light emission, which appear within 20 minutes and propagate perpendicular to the primary wafer flat. After greater than 3 hours of constant bias, no further dark-line propagation was observed for this device. This time dependence is consistent with the forward voltage increase plotted in Fig. 1. Increasing the current to 1 A (160 A/cm^2) strongly accelerated the rate of defect formation.

Based on our electrical results and time-lapse sequences of images, it is possible to make a number of observations about the degradation mechanism. The dark line features are attributed to a localized reduction of carrier lifetime caused by an extended defect, most likely a stacking fault [2]. In these regions of low carrier lifetime, the electron-hole plasma in the drift layer is suppressed, resulting in weaker light emission and lower current. Before current stressing few, if any, defects are observed. However, we assume that there are pre-exxisting and unobserved defects that are present and the density of these defects is not uniform. The identity of these pre-existing defects has not yet been determined. Based on the smooth variation of degradation observed in Fig. 1, the density of these defects appears to vary on a length scale on the order of a few mm. Once defects nucleate and start propagating, all have a similar growth velocity. This velocity strongly depends on the current. The defects grow in the $< 1\bar{1}00 >$ direction and often grow until they span the diode. In other cases, growth abruptly stops as the growth front is pinned. During the operation of the diode, new dark line defects are continually being generated. Defect generation rates are greatest during the first minutes of operation. Initially, new defects are started at the highest rate. At longer times, when the electrical degradation has saturated, the rate of new defect starts is much lower. The growth dynamics of individual defects that start later do not appear to be different from those that start earlier.

Work is in progress to study the current dependence of defect formation in more detail and to examine its temperature dependence. We are also investigating possible precursors for this effect by looking at micropipe maps and cross-polarizer images on starting material.

In conclusion, the combination of electrical measurements and emission images provides a powerful approach to examining the defects responsible for the degradation of the forward I-V characteristics of SiC PiN diodes.

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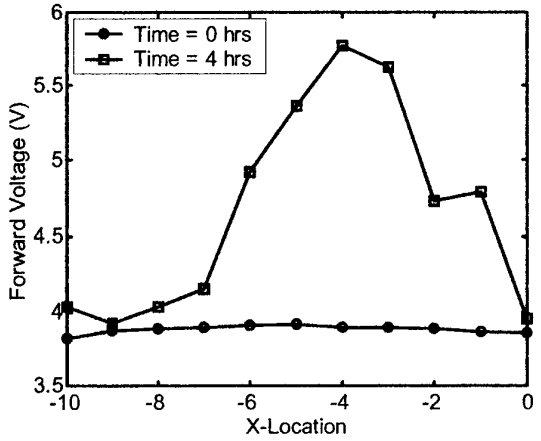


Fig. 1 PiN diode forward voltage versus time at various locations at a constant current of 0.5 A.

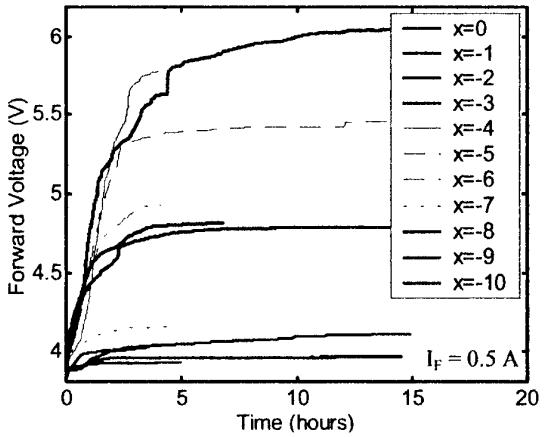


Fig. 2 PiN diode forward voltage versus position on wafer at 0 and 4 hours. The wafer center is denoted (0,0) and the edge as (-10,0).

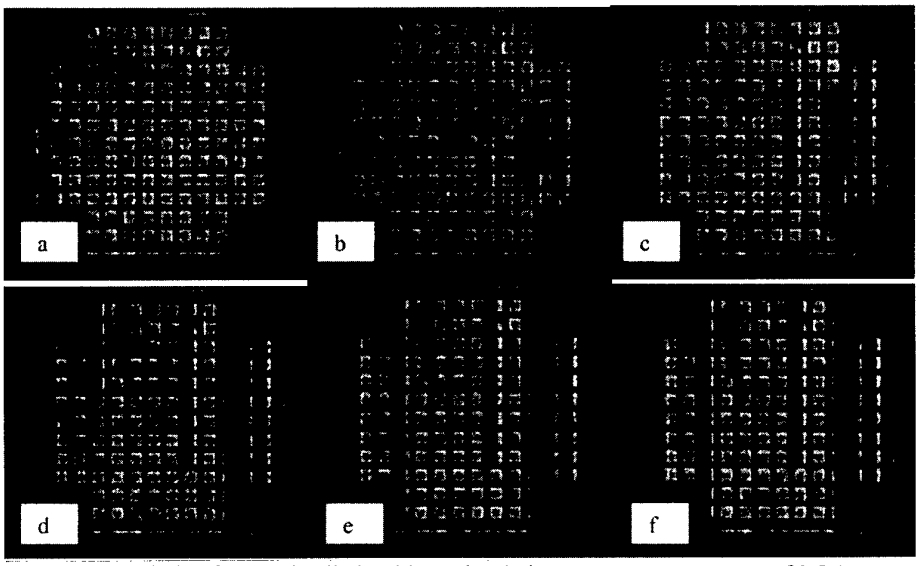


Fig. 3 Light emission from a PiN diode with anode windows at a constant current of 0.5 A at various time intervals (a) 0 hr, (b) 0.3 hr, (c) 1 hr, (d) 2 hr, (e) 3 hr, (f) 3.7 hr.

Optical Emission Microscopy of Structural Defects in 4H-SiC PIN Diodes

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A phenomenon apparently affecting the long-term stability of SiC power device performance was recently introduced by [1]. In present work, we report studies of inherent and long-term operation induced structural defects in 4H SiC PIN structures by employing an optical emission microscopy (OEM) technique. This experimental method was further developed to provide spectrally resolved 3D information by combining imaging of recombination radiation emitted from the backside and cross-sectional plane of forward biased diodes (EL) with a dark field photoluminescence (PL) technique. A variable wavelength laser source was utilized for either resonant band-to-band, or below-band excitation and ensured a homogeneous pump light penetration throughout the probed volume. The PL imaging has exhibited a good correlation with EL data and also revealed presence of some structural features in the active region not observable in EL patterns. The utilized combination of PL and EL methods with OEM is proved to be an extremely effective tool in mapping and analysis of structural defects.

We demonstrate that a successive imaging of emission from the investigated 4H-SiC PIN structures makes possible real time monitoring of the electrical stress related phenomena. In this way, a rapid migration (>50 μm/s) of dislocation pairs across the active area of devices was observed *in situ* using backside EL geometry. This propagation is presumably originated by thermal-stress and seems to be terminated once a structural defect is met on the way. An extensive planar defect with a characteristic bright-line edging is then generated throughout entire epitaxial layer. An enhanced, i.e., digitally processed cross-polarized EL imaging was utilized to expose the built-in strain fields around individual dislocations and to reveal the locations of micropipes and elementary screw dislocations. Interestingly, some of EL patterns indicate that these defects could also be responsible for the pinning of the further bright-line expansion. Finally, a cross-sectional imaging has directly provided a 3D outline of the stress-induced defects, indicating clear match with the basal plane. A spectral content of emission obtained solely from the stress-induced features is compared with the luminescence spectra from defect-free areas at different current densities and temperatures.

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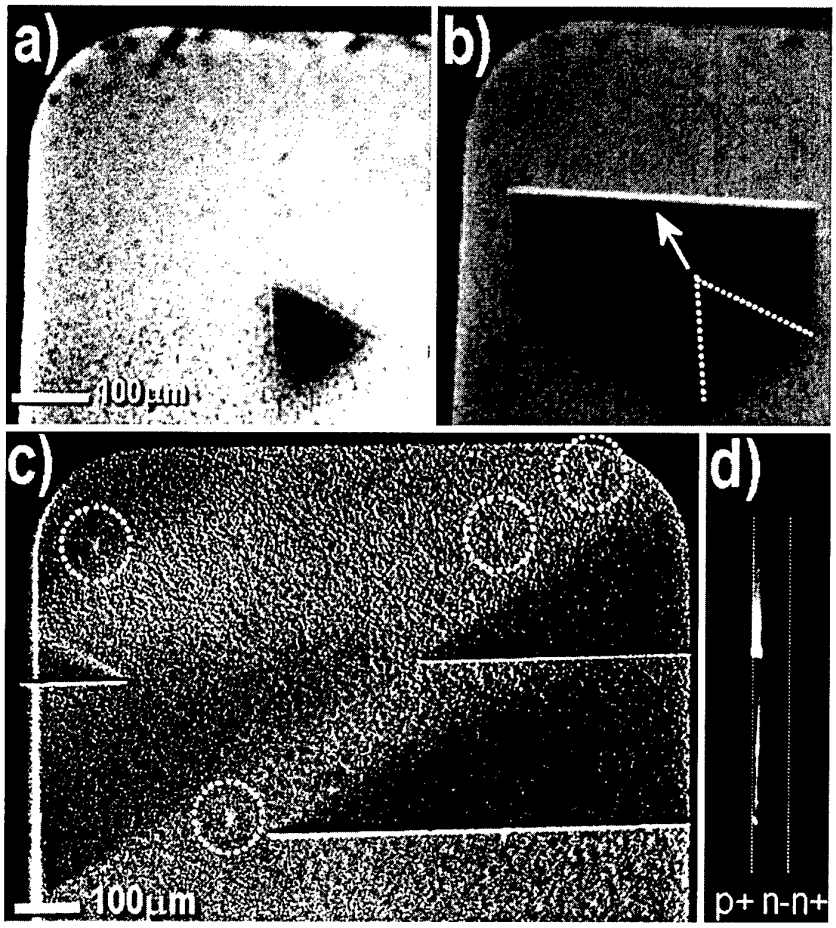


Fig. 1. Imaging of the EL emission from 4H-SiC p+/n-/n+ structures: fast migration (>50 μm/s) of dislocation pairs across the active area of electrically stressed devices was observed in real time (a). This propagation seems to be terminated once a structural defect is met on the way, and an extensive planar defect with a characteristic bright-line edging is generated throughout entire epitaxial layer (b). An enhanced (cross-polarized) EL imaging was utilized to expose locations of the built-in strain fields around micropipes and screw dislocations (c). A cross-sectional imaging has provided both a 3D outline and spectral contents of emission solely from the stress-induced features (d).

Polytype Identification and Mapping in Heteroepitaxial Growth of 3C on Atomically Flat 4H SiC Mesas using Synchrotron White Beam X-ray Topography

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The identification and mapping of the polytype distribution in nominally 3C heteroepitaxial films grown on atomically flat regions of 4H-SiC using synchrotron white beam X-ray topography (SWBXT) is reported. The procedure for producing the atomically flat regions, which was recently reported [1], consists of promoting step-flow growth on commercial SiC wafers, with surface orientations nominally (0001) (which, in fact, means slightly offset from (0001) by a fraction of a degree), which have had arrays of device-size mesas etched onto them prior to epitaxial growth. Some of these mesas encompass axial screw dislocations that typically occur scattered across the area of SiC semiconductor wafers [2] and some do not. The step flow mode of growth causes the atomic steps to grow out of existence on the vast majority of mesas free of the axial screw dislocations, leaving these mesas with a large basal plane surface tilted with respect to the original surface. Such a large, step-free basal plane surface is potentially useful for improved heteroepitaxy, as the presence of substrate surface steps has been shown to cause defects, in particular double positioning boundaries (DPB's), in heteroepitaxial films [3,4]. To confirm the feasibility of this approach, SWBXT was carried out to identify and map the distribution of polytypes in wafers subjected to these procedures. In order to achieve this, specific use must be made of both the structural and microstructural capability of the technique. This requires analysis of the spatial distribution of those regions of crystal that produce diffracted intensities which indicate the presence of one or other of the two 3C variants (3C I and II, related by a 60°, or equivalently, a 180° rotation about the 4H [0001] axis). Here we report on such studies carried out on two wafers. The first (wafer 1), was a non-optimal sub-region of one of the 4H-SiC wafers that was described in [1] that was subjected to the procedure for production of atomic flatness. The sub-region of interest, located near the wafer edge, experienced imperfect control of the local supersaturation and significant 2D terrace nucleation of the two variants of 3C polytype was inadvertently produced. This sample served to demonstrate the capability for polytype mapping. The second (wafer 2) consisted of a 4H wafer where more controlled heteroepitaxy was carried out following the successful production of the atomically flat mesas. This sample served to demonstrate proof of concept of two issues: (1) to confirm that dislocation-free mesas could be made atomically flat and (2) that complete DPB-free coverage of these atomically flat mesas by one or other of the 3C polytype variants could be achieved. In addition to SWBXT, supplemental thermal oxidation color mapping, Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) was carried out.

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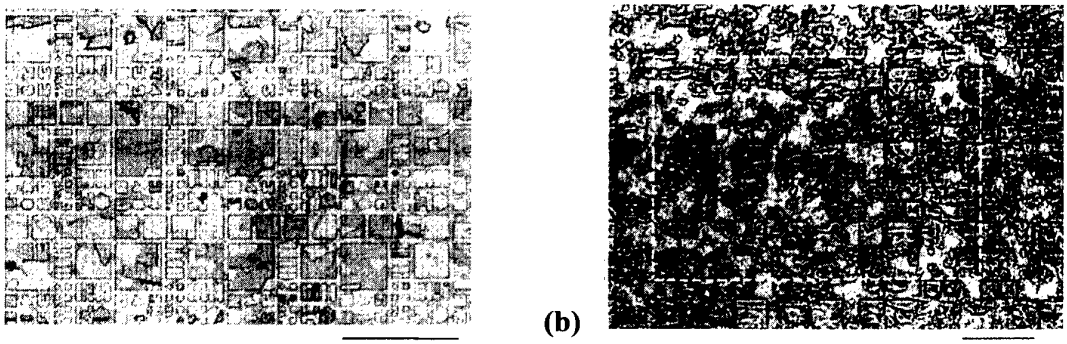


Fig. 1(a) Oxidation color map of part of wafer 1, with unintentional nucleation of 3C polytype; **(b)** Back-reflection SWBXT image showing defect microstructure. The area of correspondence with Fig. 1(a) is outlined. Regions where 3C has nucleated are surrounded by dark line contrast associated with a small tetragonal distortion. Scale marks = 1mm.

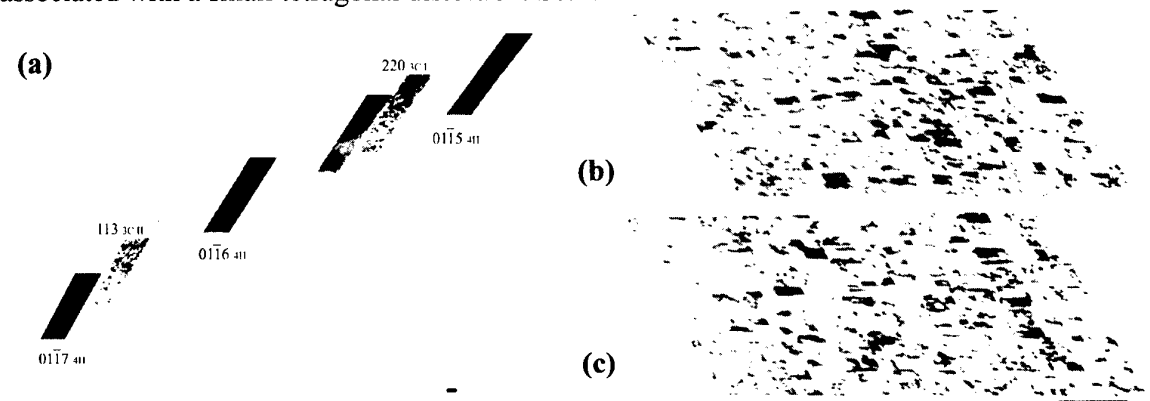


Figure 2(a) Selected area from reflection diffraction pattern recorded from wafer 1; **(b)** and **(c)** composite images showing the distribution of 3CI (b) and 3CII (c). Colors were then assigned to these images and, following image processing to remove the geometric distortion, they were superimposed on Fig. 1(b), as shown in Fig. 3(a). Scale marks = 1mm

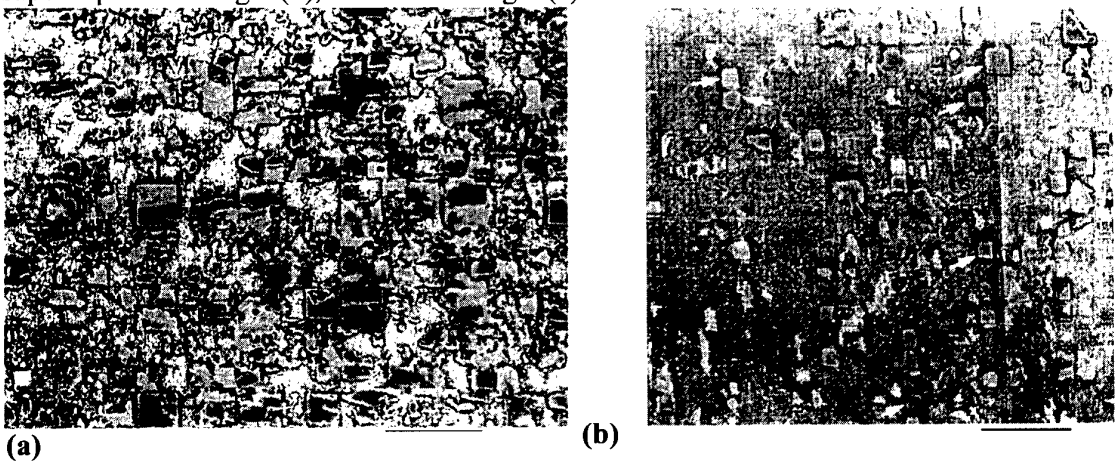


Fig. 3 Composite images showing the distribution of 3CI and 3CII over the surface of **(a)** wafer 1, and **(b)** wafer 2. Note mixtures of 3C polytypes on mesas in (a) and the presence of mesas with complete, uniform 3C overgrowth, as indicated by arrows, in (b). Scale marks = 1mm.

Behavior of the micropipes during growth in 4H-SiC

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The improvement of the SiC wafers is substantial for the increase of the yield of the fabricated devices. The SiC wafers suffer from different types of defects, as dislocations, planar defects, carbon and silicon inclusions, low angle boundaries and micropipes. Especially the last ones are detrimental for the device performance, due to their large diameter [1]. A micropipe is usually formed after the breakdown of a screw superdislocation at high temperature, when a hollow core is spontaneously generated [2, 3] Micropipes can be also generated at inclusions or voids [4]. The last few years the micropipe density has been significantly reduced by better controlling of the kinetics during growth [1], or by micropipe healing using liquid phase epitaxy [5]. It is evident that the better understanding of the behavior of the micropipes during growth can lead to a further reduction of the their density.

In this paper evidences for the role of micropipes in extended defect formation are presented. The study is based on Atomic Force Microscopy (AFM) and Transmission Electron Microscopy (TEM) observations.

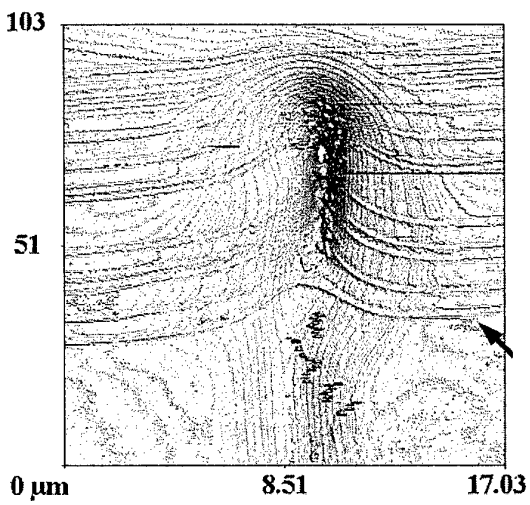


Fig. 1. AFM image of a trench-like defect extended from a micropipe. The arrow points to the steps.

The 4H-SiC specimen with a thickness of about 50 μm was grown by sublimation epitaxy at 1750C on Si-face, 8 degree off 4H substrate. Details of the growth geometry and procedure are described elsewhere [6]. From the AFM images, it was evident that in some cases the micropipes were related to a shallow trench at the surface as shown in Fig.1. The trench is always extended from the one side of the corresponding micropipe. The trenches coincide with the direction of the growth steps and they may extend up to 500μm in length. In general the width of the trench corresponds to the diameter of the micropipe, the depth of the trench is between 30 to 140nm as measured by the corresponding profiles. Inside the trench the growth steps due to the lateral growth are distorted towards the direction of the pipe. Therefore the shallow trenches were related with a retardation of the steps due to the micropipe. It is worth noting that the steps are not broken in the trench, but they remain continuous.

The characterization of the trenches was completed by TEM observations. Due to the very large size (a few μm) and the very low density (10 to 100 cm^{-2}) of the micropipes it was difficult to locate the area of interest due to the very small field of observation provided by the TEM. Due to these limitations the specimen for the TEM characterization was prepared after location of the trench by the AFM. The area of interest was thinned only from the backside up to a thickness of about 200nm. The TEM micrograph including a part of the trench is shown in Fig.2. The bending of the periodic growth steps inside the trench is evident. In the inset in the left upper corner of the picture a magnified image of the origin of the defect is shown. The contrast of these fringes is attributed to surface ripple due to the step propagation and disappears when the specimen is thinned from the front side. The corresponding diffraction pattern from this area confirms the propagation of the trench along the [1 1-2 0] direction.

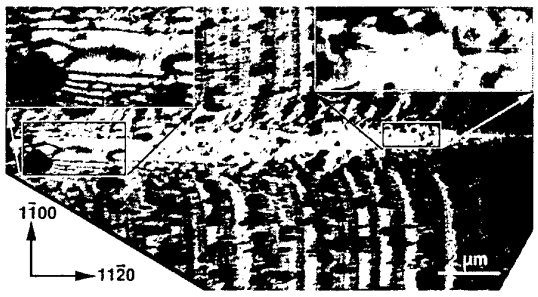


Fig. 2. TEM micrograph of the defect showing the bending of the steps and two insets with details.

A planar defect was also observed running inside the trench and parallel to its axis, as shown in Fig.2. The planar defect lies on the (1-1 0 0) plane seeing edge on in Fig.2. Details are shown in the upper right inset in Fig.2. In additional images it was evident that a dislocation can be found in the vicinity of the planar defect. We believe that this defect is a stacking fault, which is formed due to misalignment of the growth planes. In order to exclude the case of an artifact produced by a step parallel to [1 1-2 0] direction the same specimen was thinned from the front side so that the growth steps and the trench were smeared out. The contrast of the planar defect persists revealing that it is related with the bulk SiC. The formation of the trench-like defect starting from pipes and extending along the flow direction of growth steps may related the high V_C/V_A ratio, where V_C is the normal growth velocity and V_A is the tangential component. Synchrotron X-ray topographs reveal dark contrast associated with the defect which might suggest that are stress present during the layer growth. Additional information regarding the relation of the planar defect with the slip trace will be presented.

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Stress distribution of 2 inch SiC wafer measured by photoelastic method

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1. Introduction

Large size defects (for example micropipe and planar defects) were studied for years. SiC-based device technology has made remarkable progress in recent years with decreasing the defects density year by year [1] and the supplier is demanded to decrease more small size defects and stress field.

Sub-grain boundaries were made from stress fields [2]. Not only sub-grain boundaries, but also almost defects occurred by the stress field, which has several origins, thermal, physical and so on. But it is difficult to make clear how to occur these stress fields and the distribution in situ. Because SiC bulk grown by sublimation is occurred in the closed graphite crucible.

So, we tried to observed stress field of the grown SiC wafer by several methods. Kato et. al researched internal stress around the micropipe by the polarizing optical microscope[3]. And the area of existing sub-grain boundary was corresponded with the stress field by cross polarizer and the FWHM(Full Width at Half Maximum) of the rocking curve of X-ray diffraction became large[2]. But we want to know easily the distribution of stress field in the SiC wafer. So we made photoelastic system using the sensitive color plate between the polarizer and analyzer and observed the little double refraction and this orientation.

2. Experiment

The samples were 2 inch 6H-SiC (0001) just wafers made by sublimation method. The wafer thickness was 1mm. Figure.1 shows the schematic system of photoelastic method. The source of light was the white light. The sensitive color plate was cellophane paper, whose retardation was about 500nm and color was orange. We observed the change of color by rotating the sample. If the sample has retardation about +200nm, the color-changed blue, if it has the retardation about –200nm, the color changed yellow. We can know which the force is compress stress or tensile stress from these results.

If the sample is not (0001) just wafer and has some off direction, the oval polarized light is occurred. So we confirmed the samples which are (0001) just wafers.

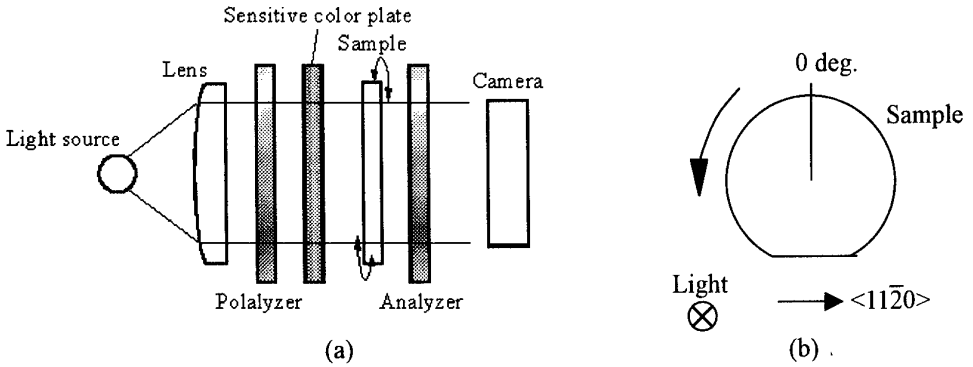


Fig.1 Schematic photoelastic method system

3. Results

Fig.2 (a) and (b) show the photoelastic images whose wafers position were 0 degree and 60 degree, respectively. We decided the wafer position named 0 degree when the wafer positioned like fig.1 (b) and 60 degree means the wafer rotated 60 degree to counterclockwise direction. By comparing with fig.2 (a) and (b), we found the violet area moved to counterclockwise direction but the violet color of (b) became lighter than that of (a). It means the x-axis of sample (x-axis corresponded with the short axis of the ellipse) is <1-100> direction. This sample is compressed in x-axis direction. Normally the sample was influenced with compress stress along <1-100> direction and with tensile stress along <11-20> direction. And from fig.2, the color-changed area exist at peripheral area very much.

And we can observe easily stripes, which corresponded with sub-grain boundary. The crystal is closed to graphite crucible wall in sublimation method. So we think the one of the origins of the sub-grain boundary at peripheral area were the thermal expansions between graphite and SiC grown crystal[2].

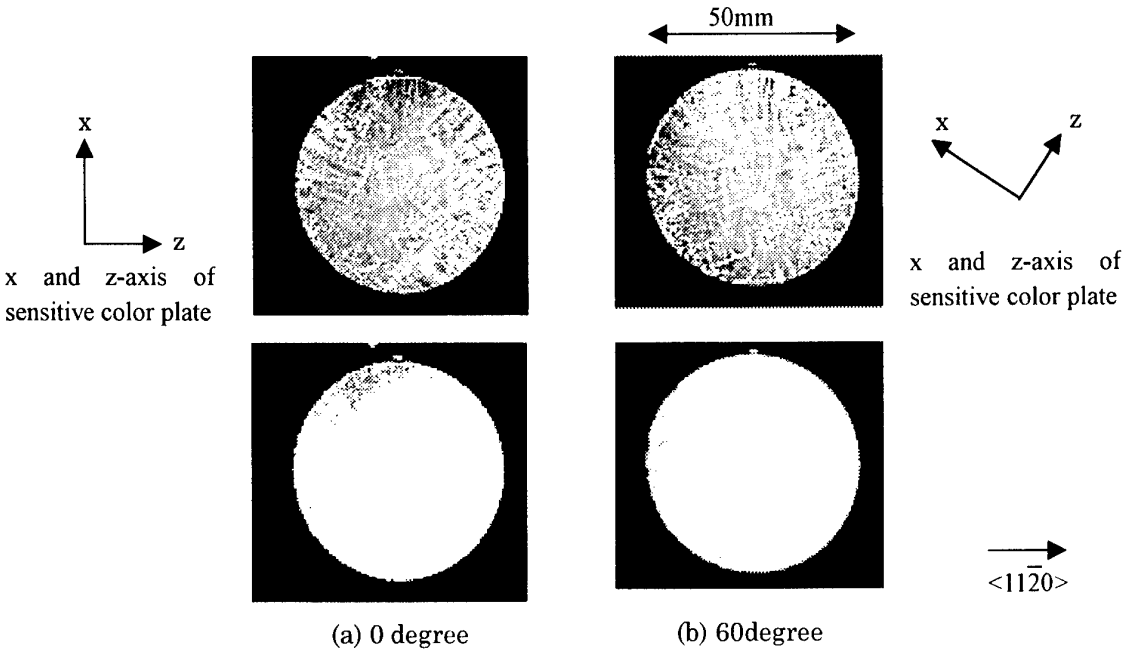


Fig.2 Photo elastic image of 2 inch SiC wafer. The upside images of (a) and (b) were changed to gray scale image, but almost area looked orange and downside images were extracted the violet area.

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The Brittle to Ductile Transition in 4H-SiC

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The brittle-to-ductile transition (BDT) temperature, T_{BDT}, in semiconductors is an important parameter separating the temperatures over which the material yields by plastic deformation from those at which it fails catastrophically by fracture. Extensive work on this transition in many semiconductors has shown that T_{BDT} is very sharp generally occurring over a temperature range of a few degrees centigrade and it shifts to lower temperatures at lower strain rates. In this paper, we have used the technique of 4-point bend test to measure the BDT temperature of pre-cracked single crystal 4H-SiC. The samples were deformed at temperatures from 800°C to 1300°C and at two different strain rates, $\dot{\varepsilon} \approx 5\times10^{-7}\ s^{-1}$ and $\dot{\varepsilon} \approx 5\times10^{-6}\ s^{-1}$. At $\dot{\varepsilon} \approx 5\times10^{-7}\ s^{-1}$, the BDT temperature has been determined to be ~1005°C while at $\dot{\varepsilon} \approx 2.6\times10^{-6}\ s^{-1}$, T_{BDT} shifts up to ~1175°C. The shear stresses at which the samples yield plastically above T_{BDT} are consistent with the values measured by direct compression experiments, and the values of T_{BDT} appear to be consistent with the transition temperature measured by direct plastic deformation of 4H-SiC. The experimental results will be presented and discussed in the light of a new model for the brittle-ductile transition in tetrahedrally coordinated semiconductors.

MoP Poster Session I

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Micropipe Formation Model *via* Surface Step Interaction

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Silicon carbide (SiC) single crystals, a promising material for high power and high temperature semiconductor devices, still suffer from crystallographic defects, so-called "micropipes." Micropipes are known to be hollow defects aligned along the growth direction of the crystal. As they penetrate the entire crystal, they are a significant problem in growing high quality SiC single crystals, since they become "killer" defects if they intersect the active regions of SiC devices. The origin of such hollow defects was proposed by Frank [1] who considered dislocations with an extremely large Burgers vector. If the Burgers vector of a dislocation exceeds a critical value (approximately 2nm), then it is, due to large strain energy, energetically favored to remove the core material and to produce an additional surface in the form of micropipe.

The magnitude of the Burgers vector of micropipes in SiC crystals ranges from 2 to greater than 10 times the unit c lattice parameter. In principle, a dislocation with a Burgers vector of multiple unit cell size $\boldsymbol{b}=n\boldsymbol{c}$ is energetically unfavorable compared to a distribution of n elementary dislocations with a Burgers vector $\boldsymbol{b}=\boldsymbol{c}$. Thus, if a screw dislocation with a Burgers vector $n\boldsymbol{c}$ (super screw dislocation) exists, it would tend to dissociate into n separate unit $\boldsymbol{c}$ screw dislocations. In other words, screw dislocations with the same-sign Burgers vector repel each other. However, super screw dislocations (micropipes) are easily produced in SiC crystals and stably propagate during crystal growth. These experimental observations are not satisfactorily understood yet, and how dislocations are brought together to produce micropipes and why such super screw dislocations are stable in SiC crystals are still puzzling questions.

In this paper, we propose a micropipe formation model *via* surface step interaction, where the strong repulsive interaction between surface steps on the SiC(0001) surface is a major driving force for coalescing unit cell size screw dislocations.

There are three elements that are necessary for this mechanism to be operative. First, a high density of screw dislocations is needed to feed the process. Micropipes are very often observed at the foreign polytype and secondary phase inclusions during growth, where high density screw dislocations are introduced. Second, a large repulsive interaction between surface steps is required for the coalescence of unit c screw dislocations. This is explained by the large step height and stiffness observed on the SiC(0001) surface [2]. Finally, once micropipes are formed, they need to stably propagate in SiC crystals. Spiral growth mechanism ensures stable lateral advancement of steps of multiple unit cell height, which kinetically prevents the dissociation of the bunched steps and thus prevents micropipes.

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The development of 2in 6H-SiC wafer with high thermal conductivity

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1 Introduction

6H type SiC, which is known as a wide gap semiconductor, is recently taken notice as substrates for GaN and SiC epitaxial layers. Their applications of optical and high frequency devices require high quality substrates with high and low-resistivity, respectively.

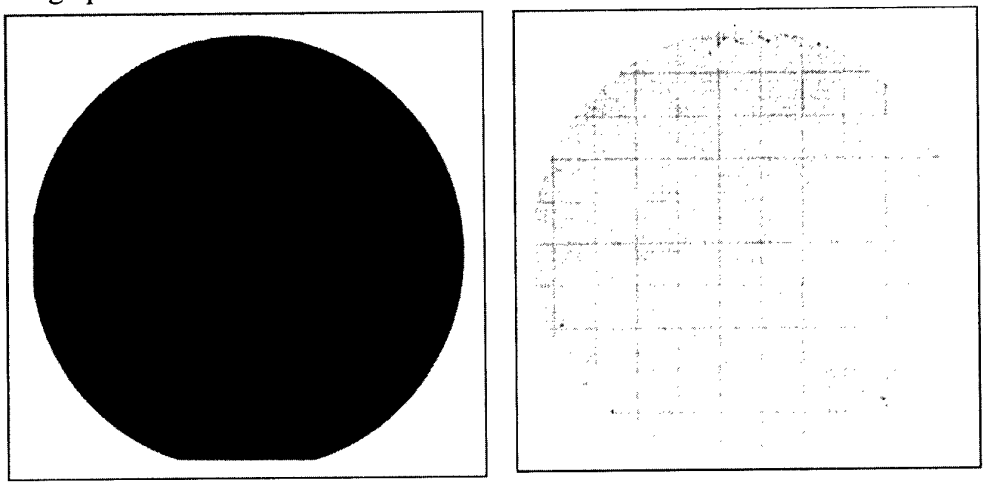
In this research, we made 2 in, high quality 6H type SiC bulk single crystals by the sublimation method, and successfully controlled their conductivities.

2. Experiments

Bulk single crystals were grown by the sublimation method. The crucible assembly consisted of a graphite support to which the seed crystal was attached and a graphite crucible containing the source powder. Mirror-polished SiC wafer was used as the seed crystal. The seed crystal and the source powder in the crucible were heated between 2200 ℃ and 2400 ℃ in the atmospheric pressure of inert gases. During the crystal growth, total pressure was 1 ～ 10kPa, and nitrogen gas was introduced into the furnace as the dopant for the crystal with low resistivities .

3. Results

We successfully made 2 in N-doped and undoped 6H type SiC single crystals. Fig.1 shows N-doped and undoped 2in 6H-type SiC. We measured the electrical, crystallographic and thermal characteristics.



(a) (b)

Fig.1 (a)N-doped and (b)undoped 6H-SiC wafer

(1) Electrical characterization

The resistivities of N-doped and undoped wafers, measured on the van der Pauw method at room temperature, were 0.04 Ω·m and $>10^5$ Ω·cm, respectively. We confirmed that these values are low and high enough for optical and high frequency respective device applications

(2) Crystallographic characterization

We etched these wafer surfaces by molten KOH at 500 ℃, and observed them by the optical microscopy. The micropipe densities of low and high-resisitivity wafers were $29cm^{-2}$ and $22cm^{-2}$, respectively.

X-ray diffraction measurement was conducted using a double-axis diffractmeter, where a four-crystal monochrometer was used for Cu K α 1 radiation. The rocking curves of both low and high-resisitivity wafers showed a narrow single diffraction peak with FWHM of 34 arcsec at the center of each wafer. We confirmed that each wafer has low dislocation densities and the low disorder of lattice arrangement.

(3) Thermal characterization

We measured the thermal conductivity of the undoped wafer and the N-doped wafer, which were 471W/mK and 420W/mK, respectively, by the alternative optical method at room temperature (300K). These are above that of Cu (400 W/mK) and as high as the value ever reported on the 2 in wafer grown by the seeded sublimation method. Fig.2 shows the temperature dependence of the thermal conductivity. At 600K, the thermal conductivity of the undoped wafer and the N-doped wafer were 190W/mK and 210W/mK, respectively.

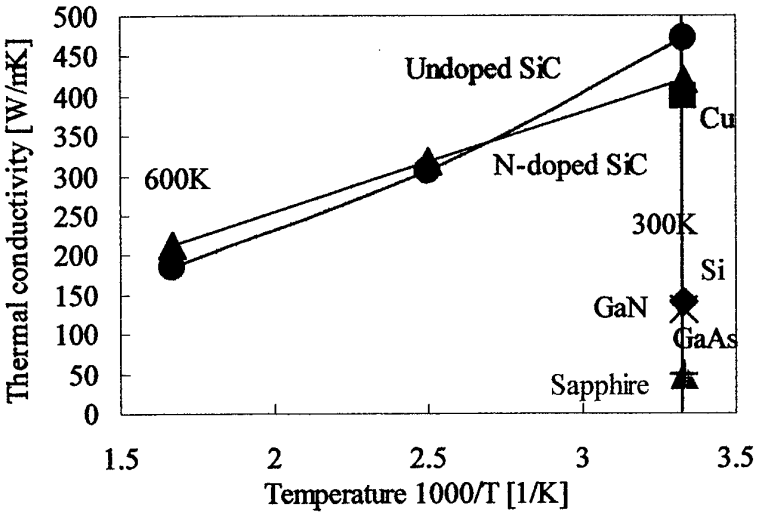


Fig.2 Temperature dependence of thermal conductivity

When the temperature was raised, the thermal conductivity of the 6H-SiC with low-resistivity came to exceed that of the 6H-SiC with high-resistivity. In the thermal conductivity model, there are two mechanisms, which are due to the lattice vibration and the free electron. In general, the thermal propagation by the lattice vibration becomes predominant at the low temperature and the thermal propagation with the free electron becomes predominant at the high temperature. The nitrogen impurities in 6H-SiC promotes the thermal propagation with the free electron though suppresses the thermal propagation with the lattice vibration. Therefore the thermal conductivity of N-doped SiC has less temperature dependency and is even higher than that of undoped SiC at high temperature.

4. Summary

We successfully made 6H-SiC with high thermal conductivity and confirmed that they had low dislocation density and low disorder of lattice arrangement.

Flux Controlled Sublimation Growth by an Inner Guide-Tube

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Silicon carbide (SiC) power devices are expected to reduce energy loss of the electric power converter dramatically. The improvement of the quality and the enlargement of SiC substrate are problems for practical use of the SiC power devices and their applications. Single crystal growth of a high quality and large diameter bulk SiC is the technological point for the above problems. Single crystal of the bulk SiC has been grown by modified Lely method (sublimation method) [1]. Enlargement of single crystal from small seed crystal has been investigated using the modified platform on which the seed crystal was attached [2]. But we found that the quality of the single crystal was degraded by polycrystals grown around the single crystal. In this work, we newly developed the inner structure of the crucible in order to enlarge the single crystal without polycrystal around it. The effect of the growth parameters on the shape and the quality of the crystal was investigated.

SiC bulk single crystals were grown in an RF induction furnace. An inner guide-tube in the shape of a hollow truncated cone was installed between a seed crystal and source material. It was supported on the inner wall of a cylindrical graphite crucible. (Fig.1) This guide-tube functioned to control flux of sublimation gas from source material and formed a growth space separated from the polycrystal and the extra space. The geometrical parameters of the guide-tube are shown in Fig.1. The temperatures of the top and bottom of the crucible were in the range of 2150-2250°C(T_{top},T_{bottom}). Since the temperature of the guide-tube(T_g) was important for the crystal growth, T_g was controlled indirectly changing the RF coil position and/or the geometrical parameters of the guide-tube. The effect of the growth conditions such as the geometrical parameters and temperatures on the shape and the quality of the grown crystals was examined. In comparison, crystals were also grown in a simple crucible without the guide-tube. The crystal quality was characterized by polarizing microscopy and X-ray topography.

A crystal ingot grown in the crucible with the guide-tube is shown in Fig.2. The single crystal was successfully grown separated from polycrystal. The ratio of the growth rate of single crystal and polycrystal was the range of 1.5-4 depending on the growth parameters and typical value was around 2. That ratio was 0.7-1 in the case of growth without the guide-tube. This means that the guide-tube enhanced the growth rate of the single crystal relatively compared with that of the polycrystal by controlling flux of sublimation gas. It is possible that the single crystal is grown separated from polycrystal selecting the height of platform(H), the gap between the platform and the guide-tube(x,y) and growth time. The broadening angle of the single crystal could also be controlled by changing the taper angle of the guide-tube(θ) and the angles in the range of 0-30° were practically obtained. Crystal defects such as crack, subgrain boundary and macrodefect were drastically reduced compared with that of the crystal grown together with the polycrystal. X-ray topography images of the single crystals

with and without the polycrystal are shown in Fig.3. Misoriented areas in the periphery were observed in the both crystals but the patterns were different. The periods of the patterns was larger in the crystal without polycrystal. There still remained misoriented areas even though the effect of the polycrystal vanished from the single crystal. This would be due to the thermal stress and/or the high enlargement rate as discussed by Bakin et al in Ref.[3].

In conclusion, the single crystal was successfully grown separated from polycrystal using a new type of crucible with an inner guide-tube. Consequently, the quality of the grown crystal was improved. High quality and large size bulk SiC is expected to be produced by the present method.

This work is financially supported by METI partly through NEDO.

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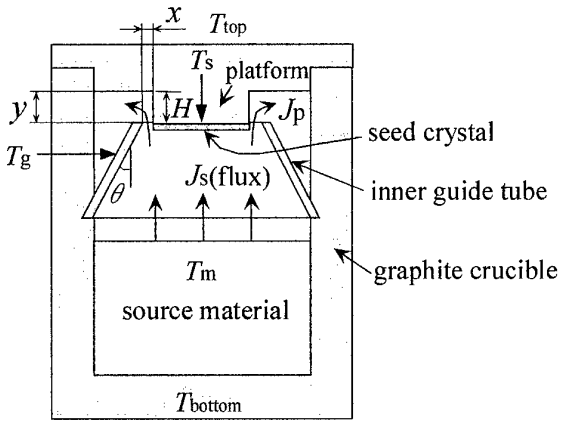


Fig.1 Schematic diagram of the growth crucible. The growth parameters are shown.

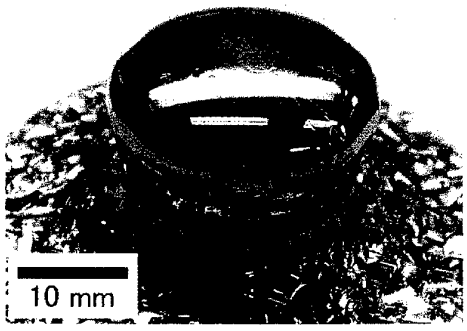
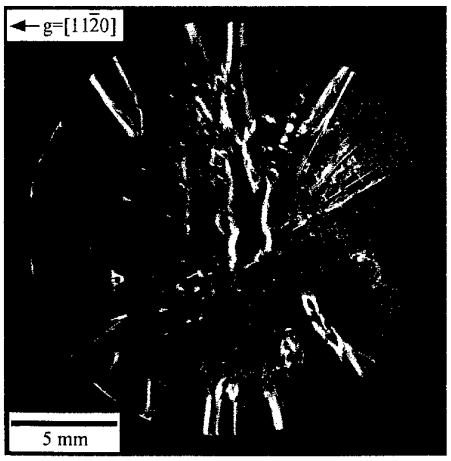


Fig.2 Photograph of the grown crystal.



(a)



(b)

Fig.3 X-ray topography images of the grown crystals. (a) grown with polycrystal by conventional crucible, (b) grown without polycrystal by the inner guide-tube.

Growth and evaluation of high quality SiC crytal by sublimation method

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Various defects which exist in a substrate are taken over to epitaxial film and they have a bad influence on electronics devices. [1] [2] Consequently the performance of electronic devices are not enough.

In order to reduce these defects, it needs to analyze them in detail and obtain a detailed information of these defects. However, as the conventional crystal made by the sublimation method of defect density was very high, their detailed information was not able to be obtained. In this study we grew the low defect density SiC crystal by the sublimation method, and we report the defect of the crystal.

The crystal was grown by the sublimation method that utilizes the lely crystal as a seed crystal. The source was polish abrasive powder of #240. The seed crystal and source powder was installed in the graphite crucible, and was overheated to 2200 degrees C. The atmosphere of growth system was argon at 13.3kPa. Growth was performed on Si-face. The optical microscope observation, X-ray topograph, and the etch pit observation by KOH etching were performed for the crystal evaluation.

The polarizing microscope photograph is shown in Fig. 1. The micro pipe could be confirmed by interference patterns observed by photoelastic measurements under the crossed polars condition. The sample shown in the photograph has contrast with the uniform whole surface, we don't observe interference pattern by photoelastic measurements. Hence this crystal does not have a large strain and there is no micro pipe.

The result of section topograph was shown in Fig.2. The direct image and dynamic image by defects was observed in the section topographic image. The direct image that is black point is mainly edge dislocation. And the dynamic image that is white diagonal line seems to be stacking fault. Pendellösung fringes is also observed. It means that the crystal quality is very high.

According to the etch pit observation by KOH etching, the etch pit density was $4x10^3cm^{-1}$ and there was no deviation in a distribution of etch pits.

This work was performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO

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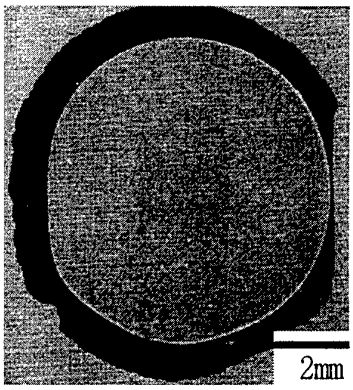


Fig.1 High quality SiC crystal of polarizing optical microscope image

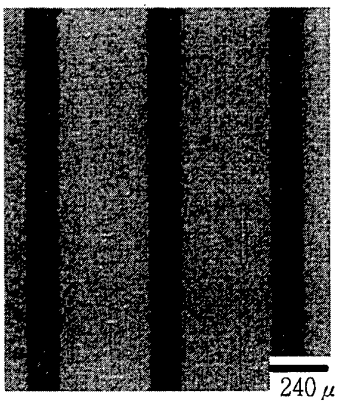


Fig.2 (11-20) Section topograpfs of SiC crystal by sublimation method. Mo Kα radiation. Sample thickness of 270μm

REDUCTION OF MACRODEFECTS IN BULK SiC SINGLE CRYSTALS

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Keywords: bulk crystal growth, macrodefects, sublimation, crystal quality

Modern semiconductor industry yearns for Silicon Carbide (SiC) monocrystalline substrates because its unique electrical and thermal properties. SiC single crystal substrates are wanted for electronic devices (such as HF transistors, power rectifiers, high temperature sensors and controllers, etc), as well as for opto-electronics because SiC appears to have a very low mismatch of lattice parameters with basic active opto-electronic materials. It is common sense that an industrial scale SiC electronics starts as soon as market offers 4-inch diameter wafers with low defect density at reasonable price. Peculiarities (high temperatures, spatial and temporal instabilities of gas/vapor distribution, existence of porous graphite elements in growth zone, intricate temperature distribution in the growth chamber) of sublimation method of the crystal growth make this task at least very complicated one. To challenge this requirement Sterling has developed a proprietary technology that provides the feasibility to increase the grown boule diameter without deterioration by macrodefects. As far as the boule enlargement is concerned, a proper choice of a ratio between a vertical and radial components of the temperature gradient is critical to this process. Therefore the boule diameter has been realized through the development of proper technology for gradual increase of the grown crystal size and the design of a specific crystal growth chamber.

Macrodefects and imperfections in bulk SiC single crystal destroy the crystal quality. Crystal perfection is a critical issue for device performance, as in many applications the functional capability of the electronic device is limited by the size of the defect-free area. The aim is to eliminate or to reduce the defect density to the lowest possible level. Macrodefects include micropipes, low-angle-grain-boundaries, hexagonal voids, foreign material inclusions, and other attributes such as lattice/wafer bending originating from lattice distortion. It was observed that the defective portion of the crystal boule correlates strongly with quality of growth in the near-seed region. The seed attachment and treatment are factors playing the main roles in the defect generation. Therefore, the seed treatment, type of attachment of the seed, seem to be the crucial factors connected with effects taken place at the interface between the seed and seed attachment. Other factors having an impact on the increase of the defect-free region are the seed polarity (Si or C-face), seed quality, and source material. Methods of statistics and design of experiments were explored to clarify factors influencing the crystal quality. Now Sterling produces 2"-diameter SiC wafers with less than 7 micropipe/cm^2 without other macrodefects, and a radii of wafer lattice curvature exceeding75 m. On its way to 4" diameter wafer commercial production, Sterling has demonstrated successful R&D growth of the single crystal boules of 92 mm diameter (See Fig. 1 as an example).

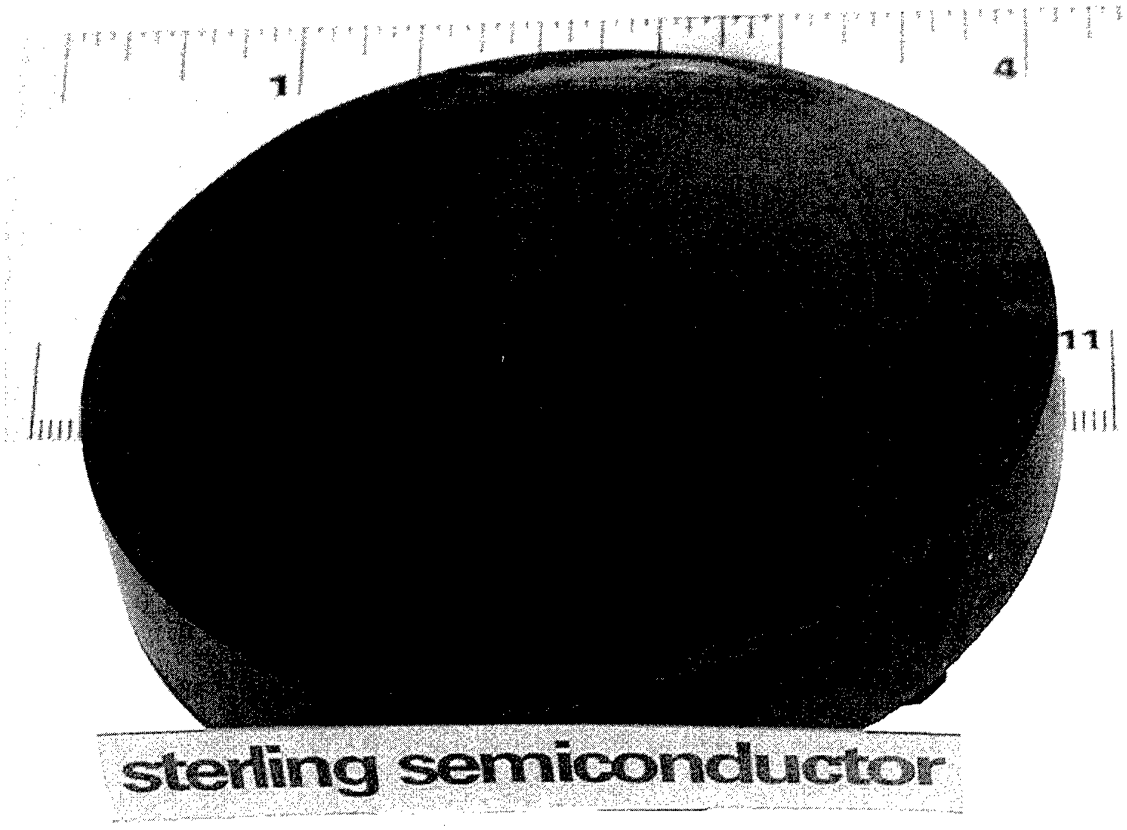


Fig. 1 Photo of Sterling's boule (after grinding)

Evolution of crystal mosaicity during physical vapor transport growth of SiC

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Recent reports on device degradation due to crystal mosaicity (domain structure) in SiC substrates have prompted interest in the origin and cause of crystal mosaicity in SiC crystals. The present authors revealed in the previous report [1] that the mosaicity originates in low angle grain boundaries existing in SiC crystals. Low angle grain boundaries are a critical defect which prevents the implementation of large-size ($\geq 1 cm^2$) SiC devices. We have found that one of the major causes of low angle grain boundaries and the resulting mosaicity is the inclusion of foreign polytypes during growth [1]. The non-basal plane interfaces between the different polytypes accommodate crystallographic imperfections which relax into polygonized low angle grain boundaries during growth.

In this paper, an experimental investigation of the crystal mosaicity in SiC crystals grown by the physical vapor transport (PVT) method is presented. We investigate how the mosaicity in SiC crystals evolves during PVT growth. High resolution x-ray diffractometry (HRXRD) was employed to examine the relative misorientation between adjacent domains as well as elucidate the formation mechanism of crystal mosaicity in SiC crystals.

6H- and 4H-SiC crystals were grown along the [0001] and [$11\bar{2}0$] directions by the PVT method, and the grown crystals were sliced into wafers having (0001), ($1\bar{1}00$) and ($11\bar{2}0$) orientations. HRXRD measurements were performed using a double-axis diffractometer, where a four-crystal monochromator was used for Cu_{Ka1} radiation. Analysis of x-ray rocking curves was used to quantitatively assess the lattice misorientation. In these experiments, the symmetric reflections of 0004, 0006, $11\bar{2}0$ and $3\bar{3}00$ in the rocking curves for 6H- and 4H-SiC crystals were acquired.

For the vertically sliced wafers along the growth direction, the incident plane was chosen either parallel or perpendicular to the growth direction. Analysis of such wafers showed that the domain structure was grown-in and originated in the seed crystal. We have examined polytype-mixed SiC crystals, *e.g.* 6H inclusions in 4H-SiC crystals. A series of rocking curves were measured from vertically sliced wafers from such crystals, where the shape and width of rocking curve varied for different diffraction scans along the growth direction. The rocking curves with the incident plane parallel to the growth direction showed a narrow single diffraction peak across the wafers, while the ones with the incident plane perpendicular to the growth direction exhibited a broader peak and often split into multiple peaks as the scans went far from the near seed polytype-mixed regions.

The polytypic inclusions would result in stresses due to the differences in the lattice constant and the coefficient of thermal expansion between different polytypes. During growth, the stresses are released by the introduction of dislocations, which are further activated to glide and climb in the crystals to minimize their total strain energy by aligning themselves along <$1\bar{1}00$>, forming low angle grain boundaries.

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4H Polytype Grain Formation in PVT-grown 6H-SiC Ingots

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Recent progress in SiC sublimation growth technology based on the modifiedLely method has spurred both a reduction of defect densities in SiC wafers and an enlargement of the wafer diameter. 4 inch-diameter 6H-SiC wafers have already been demonstrated, and remarkably smaller values of the micropipe density of the order of $<10cm^{-2}$ have been achieved for commercial 2 inch-SiC wafers [1]. A key for further development of device applications exploiting the attributes of SiC is to establish the control of optimum SiC growth with higher accuracy, which could be a path to larger SiC wafers of much improved crystal quality. In Nippon Steel Corporation, continuous challenges for fuller understanding of the growth mechanism have enabled us to accomplish the industrial production of SiC wafers with extremely low mosaicity over the whole wafer area [2], and further active R&Ds for the realisation of commercially-available 4 inch single crystal wafers are now underway.

Unwanted turbulence in optimum SiC growth still sometimes occurs, causing fatal failure in obtaining single crystal SiC ingots. A typical example of such flawed ingots is the multi-domained ingot in which large SiC grains are formed with their crystal directions strongly misoriented with regard to the SiC matrix. Similar multi-domained crystals have been reported by Tuominen *et al.* [3], suggesting that microcavities or micropipes created due to back-side evaporation could be responsible for such grain formation. Rost *et al.* [4] have pointed out another possibility that carbon inclusions could also cause the misoriented grains. Intense analyses of the multi-domained ingots we have obtained so far have been carried out in order to understand the generation mechanism of the misoriented grains, and the results obtained are presented in this paper.

Particular interest is to be addressed to our experimental fact that almost all the misoriented grains in the flawed 6H-SiC ingots we studied in this paper have the 4H polytype structure. Detailed analyses of the grains by means of X-ray pole figure measurements have suggested that the crystallographic direction of the grains has apparent correlation with that of the 6H-SiC matrix. Microstructural investigations have clarified that there exists a band region consisting of randomly-distributed fine SiC inclusions of around several tens μm in diameter. Raman analyses using a conventional Raman spectrometer are now underway for the detailed polytype identification of the inclusions. Although the formation mechanism is still in debate, we suggest that, upon the fact that the misoriented grains start from this band region, the inclusions observed are likely to be embryos of the misoriented grains, and some of which grow faster to become larger in the subsequent PVT growth.

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PVT Bulk Process Investigation: Experimental and Theoretical Approach

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Growth rate is one of the primary factors determining the crystal morphology and the density of defects in SiC crystals grown from vapor phase. It has been indicated [1] that there is an upper limit of the growth rate at which formation of inclusions, bubbles, veils, pipe-like channels, twinning and misoriented regions occurs in the growing boule of SiC. Therefore, defects in SiC are closely related to the growth rate value and the magnitude of temperature gradients in the crystal. Our experimental observations of SiC crystals grown by PVT technique show that majority of the defects listed above are located near (~2 mm) to the seed. As growth proceeds the defect density reduces. It has been found that the transition layer thickness reduces for a low axial temperature gradient condition. This resulted in the defect density reduction within the transition layer and SiC wafers production having micropipe density $<25/cm^2$. The analytical study presented here describes dynamics of the growth process at the initial stage of crystallization.

The source/seed temperature difference $\Delta T = (T_V - T_S)$ as well as the pressure in the system, are the main parameters that determine the growth rate via vapor flux intensity across the source/seed gap in the crucible (where T_V is the sublimation temperature of SiC source material and T_S is the temperature at the surface of growth). The mass conservation law applied to the total vapor flux is a fundamental relationship used for growth rate calculations: $dS/dt = \Omega \cdot F$ (Ω is the volume of SiC molecule; F is the total flux containing all the SiC vapor components [1,2]). However, the phase transformation heat released at the growth front and the heat radiated from the internal surface of the mass transport gap in the growth cell will also affect the dynamics of crystal growth. There is evidence [1] that inefficient heat dissipation in the growing crystal limits crystallization even at the initial stage of growth, when the crystal thickness is relatively small, $S(t) \cong 1.0$ mm. To maintain a necessary growth rate, an appropriate intensity of heat dissipation through the crystal volume must be ensured. In this case the Stefan's condition defines the correlation between heat balance at the surface of phase transformation and the appropriate growth rate: $\lambda \cdot \nabla T|_S = \Delta H \cdot \gamma \ dS/dt + Q$ (where λ is the thermal conductivity of SiC; $\nabla T|_S$ is the temperature gradient in the crystal; ΔH is the enthalpy of crystallization; γ is the density of SiC and $Q = Q_V + Q_W$ is the total amount of heat absorbed by the growing surface (Q_V – from the source top surface and Q_W – from the walls of the mass transport gap). Both theses factors (vapor flux intensity and heat dissipation through the crystal) will simultaneously define self-consistent thermal conditions at the surface of phase transformation that determine dynamics of crystal growth during the entire time of the process.

To enable direct analytical analysis of the growth dynamics, dependent on mass (vapor) transport and heat dissipation, the rate of growth must be expressed in terms of mass/heat transport parameters. This can be done on the basis of a solution to the mass conservation and the

heat balance equations, resulting in an expression of the growth rate as a function of the instantaneous thickness of the growing crystal:

$$dS/dt = \Omega \cdot \theta \cdot \Delta T_G \cdot G(S), \quad (1)$$

where $G(S) = (1 - \mu \cdot S)/(1 + \eta \cdot S)$, $\mu = 2 \cdot \lambda \cdot Q_W / \Delta T_G \cdot (\pi)^{1/2}$ and $\eta = 2 \cdot \lambda \cdot (Q_V + \Delta H \cdot \gamma \cdot \Omega \cdot \theta)/(\pi)^{1/2}$. The μ and η parameters determine the maximal possible thickness of the crystal and the dynamics of growth; $\Delta T_G = (T_V - T_C)$ is the temperature difference between source and backside of the crystal; $\theta \cong P_V \cdot W/R \cdot T^2 \cdot \beta$, where P_V is equilibrium pressure in the crucible at the temperature of sublimation T_V, W is the activation energy of SiC sublimation [3], R is the universal gas constant, T is the average temperature in the crucible; $\beta = \Delta T/R_D$, R_D is the diffusive resistance of the growth cell. As is clear from (1), the growth rate has its maximal value at the initial stage of growth that is determined only by mass transportation conditions $dS/dt \cong \Omega \cdot \theta \cdot \Delta T_G$, ($T_S = T_C$ at $S \cong 0$). Further, the growth rate decreases with increasing crystal thickness, approaching zero when $\mu \cdot S \sim 1$. Furthermore according to (1), the maximal thickness of SiC crystal, which is possible to obtain at a given thermal condition, is proportional to the temperature difference in the crucible, ΔT_G: $S_M \cong \Delta T_G \cdot (\pi)^{1/2}/2 \cdot \lambda \cdot Q_W$. The dynamics of growth rate variations is mostly determined by the dimensionless parameter $\eta = 2 \cdot \lambda \cdot (Q_V + \Delta H \cdot \gamma \cdot \Omega \cdot \theta)/(\pi)^{1/2}$. As follows from this formula the parameter η is the function of the vapor flux intensity, $\Omega \cdot \theta$. Hence the vapor flux intensity does not have a significant influence on the growth rate dS/dt, and the influence of heat dissipation becomes dominant, when the crystal thickness is sufficiently large. If during a growth processes the temperature difference ΔT_G is maintained constant (the source temperature T_V as well as the crystal backside temperature T_C are strictly controlled), the temperature at the surface of phase transformation will asymptotically approach the temperature of sublimation:

$$T_S(S) = T_V - \Delta T_G \cdot G(S). \quad (2)$$

The growth rate can be stabilized at a given value V_0 for any crystal thickness by tailoring the temperature (heat dissipation) at the crystal backside. As it follows, the temperature difference $\Delta T_G(S)$, stabilizing the rate of growth, is a linear function of crystal thickness:

$$\Delta T_G(S) = V_0/\chi + ((V_0/\chi) \cdot \eta + \omega) \cdot S, \quad (3)$$

where $\chi = \Omega \cdot \theta$ and $\omega = 2 \cdot \lambda \cdot Q_W / (\pi)^{1/2}$. As can be seen from (3), the latent heat of crystallization becomes dominant and defines the heat balance conditions at the growth surface when the rate of growth is sufficiently high $(V_0/\chi) \cdot \eta >> \omega$.

As a result of the increasing temperature difference ΔT_G, one can expect corresponding increase of thermal stresses in the growing crystal. A 2-D analysis showed that the axial temperature distribution is almost linear, and has no significant influence on the formation of thermal stress in the crystal. However the radial temperature gradient is a primary factor in the development of thermal stress that can lead to generation of dislocations in the crystal volume if the stress exceeds $\sigma_{CRS} \cong 1$ Mpa, which is the critical resolved shear stress in SiC.

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Resistivity Mapping of Semi-insulating 6H-SiC Wafers

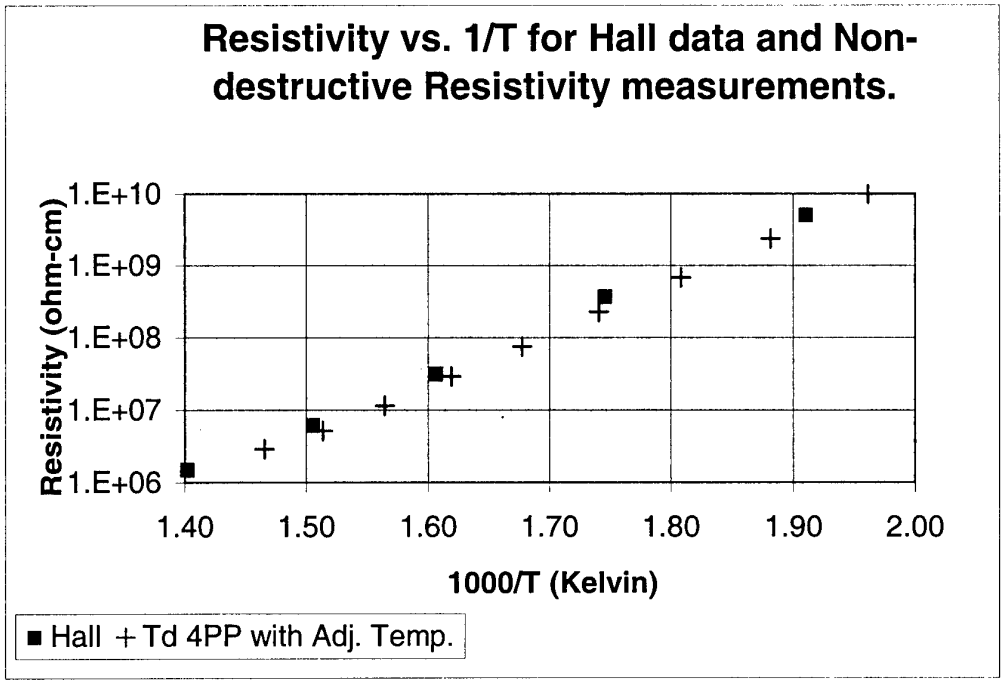
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Keywords: Semi-insulating, 6H-SiC, Silicon Carbide, Resistivity, Activation Energy, Uniformity, Hall Effect

Abstract. Semi-Insulating 6H-SiC wafers with room temperature resistivity data from 10^6 ohm-cm to 10^9 ohm-cm and greater are compared with Hall effect measurements. The transport data observed by Hall effect are compared to multi-point non-destructive resistivity maps of semi-insulating wafers. A high degree of agreement is obtained from non-destructive resistivity measurements and Hall effect measurements on corresponding regions. The spatial distribution and nature of the high resistivity behavior are also discussed.



Polytype Control in Sublimation Growth of 4H-SiC Single Crystals

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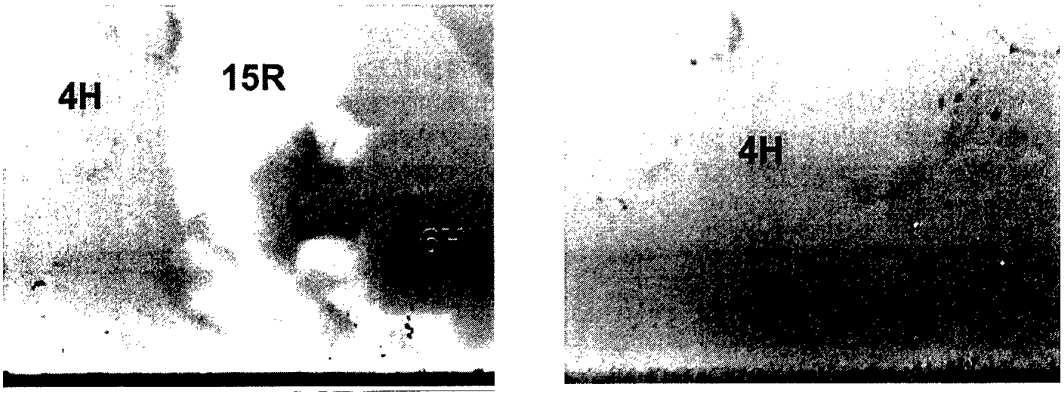
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Among the common SiC polytypes, 4H-SiC is desirable for fabrication of high power and high temperature semiconductor devices. Commercially available 4H-SiC crystals are grown by using the sublimation physical vapor transport technique. In sublimation growth of SiC, 6H is generally believed to be the most stable polytype and 4H-SiC crystals grown under certain growth conditions were observed to have 6H or 15R inclusions. These polytype inclusions in 4H-SiC crystals are believed to be responsible for generating defects, particularly micropipes, in the crystals and therefore they should be eliminated.

Several recent studies on control of 4H formation were published in the literature [1, 2]. Since each study was done in a somewhat unique sublimation growth environment, a detailed investigation of our own 4H sublimation growth process will provide further information leading to a better understanding of 4H polytype formation. In this investigation, we examined the influence of several growth parameters on the formation of 6H and 15R polytype inclusions in the sublimation growths that were intended to produce 4H-SiC crystals. Among the growth parameters, temperature, pressure and thermal gradient were studied extensively. 6H and 4H seeds of on-axis and off-axis types were used in the study. One focus of this study was on the effectiveness of the use of 4H seeds with off-axis angles up to 8° to control the formation of 4H at the seed/newly-grown-crystal interface regions in a way similar to the step-flow mechanism that is used widely in CVD epitaxial growth of 4H thin films on 4H SiC wafers. To avoid the interference of impurities with the growth parameters under study, ultra-high purity SiC source materials, as well as graphite parts, were used in all the sublimation growth experiments. The sample SiC boules were sliced both parallel and perpendicular to the growth axis for characterization. The SiC boules under study were n-type doped with nitrogen at concentrations of approximately 5e18 atm/cm3. In SiC crystals with such high nitrogen doping concentrations, all three major polytypes, i.e. 4H, 6H and 15R, in the crystals can be identified by examination under an optical microscope because these polytypes appear in distinctively different colors. X-ray transmission Laue diffraction technique was also used for the identification of polytype inclusions in the SiC samples.

Our experimental results suggested that, among the major growth parameters, the growth temperature played the most important role. Under the growth conditions in this study, lowering growth temperature favored the formation of 4H and increasing growth temperature favored the formation of 6H, while within a range of growth temperatures, 4H, 6H and 15R mixed polytypes were frequently observed, particularly at seed/crystal

interfaces. When on-axis seeds were used, 4H seeds seemed to help stabilized 4H polytype better than 6H seeds. On the other hand, under the growth conditions that favored 4H growth for on-axis seeds, using 4H off-axis seeds essentially guaranteed a uniform 4H to 4H growth at the seed/crystal interfaces. In figure 1, two optical micrographs of 4H wafers containing the seed/crystal interfaces were shown where (a) the existence and (b) the absence of 6H/15R inclusions in 4H crystals were demonstrated. Based on the results of the current study, 4H off-axis seeds should be used in order to achieve a uniform 4H-to-4H growth at the seed/crystal interface.



(a) (b)

Figure 1. Optical micrographs of 4H wafers containing the seed/crystal interfaces show that (a) the existence and (b) the absence of 6H/15R inclusions.

Details of the sublimation growth and polytype characterization results will be presented and crystal defects, such as micropipes and grain boundaries, in the 4H-SiC crystals under study will also be analyzed and discussed.

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Acknowledgements

This research is funded partially by Air Force Research Laboratory, U.S. Department of Air Force, under the contract number: F33615-99-C-5317.

Model for Macroscopic Slits in 6H- and 4H-SiC Single Crystals

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Abstract

The development of defects in SiC bulk crystals at the MLM growth is often caused by too large axial temperature gradients in the growing crystal. The axial temperature gradient can be decreased by optimisation of the graphite crucible or by changing the position of the induction coil.

Additionally, a smaller seed temperature has the same effect, because the radiation heat loss at the backside of the seed holder is proportionally T^4. Furthermore, 4H should grow more stable at lower temperatures.

This temperature influence was used for the growth of 6H and 4H single crystals under stable conditions. The single crystals were grown with 30-36 mm in diameter and a micropipe density between 50-200 cm^2. A short-time nitrogen doping marked different growth sections.

The seed temperature was varied between 2050°C and 2250°C. The seed polytype was selected corresponding to the wanted polytype and cutted with 3.5° off for 6H and 8° for 4H to $<11\bar{2}0>$ orientation. To ensure the polytype stability the C-terminated surface was used for 4H-crystals. 6H-crystals could generally be grown on both sides although a higher polytype stability on the Si-terminated surface was observed.

The investigations of wafers and axial slices were realized by means of microscopy in polarised light, photoluminescence at room temperature, and Scanning Electron Microscopy (SEM).

Decreasing the seed temperature macroscopic slits will be developed in growth direction (fig.1,2). The lateral extension is orientated preferentially in $<1\bar{1}00>$- and $<11\bar{2}0>$-directions.

The origin for such defects can be localized at other defects extended nearly perpendicular to the growth direction. Examples for such source defects are lamellas of other polytypes (15R) and a new kind of macropipes which are oriented vertical to the growth direction.

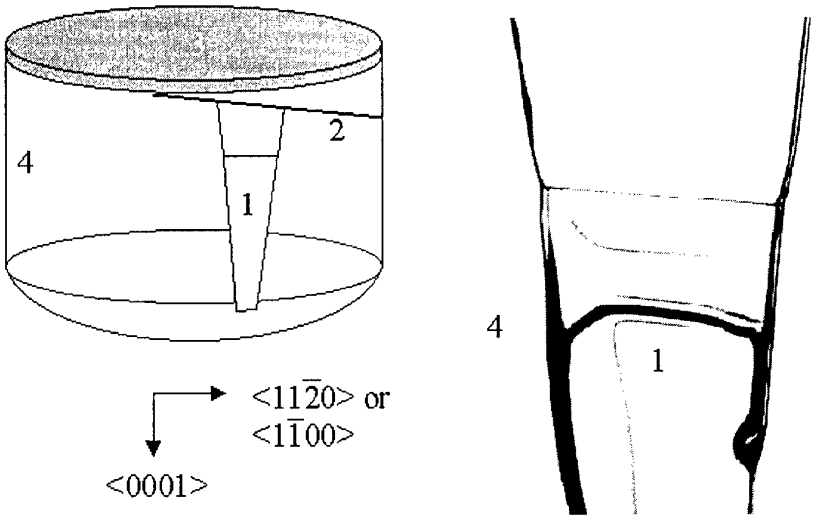


Fig.1: Sketch and micrograph of a macroscopic slit in SiC-crystals; 1- macroscopic slit, 2- needle like inclusion (15R), 3- seed, 4- bulk

As a first attempt of explanation the influence of the mechanically induced stress field on the supersaturation can be used. In accordance with the argumentation in [1] a step train can be blocked by a stress field elongated parallel or almost parallel to the surface. Following growth steps cannot enter this step bunching like region. A stable slit is formed. Then a „Schwoebel effect" is responsible for the stable enlargement also in the growth direction [2]. Typically the size of slits is 3-100µm in width and 2mm up to 15mm in length. This geometry shows a good accordance with the theoretical considerations.

The main responsibility of polytype changes for the formation of the macroscopic slits is shown when polytype changes are prevented by increasing the seed temperature or other measures. Macroscopic slits are quite rare under such conditions.

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Nucleation-induced stacking faults in PVT SiC layers grown on (0001) Lely seeds

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The structure of seed/crystal interfaces has been investigated by conventional and high resolution transmission electron microscopy (TEM). 6H-SiC layers have been deposited by Physical Vapor Transport method on high quality on- and off-orientation Lely seeds. Growth experiments have been performed between 2200 and 2300 °C with 20 °C/cm axial temperature gradient and argon pressure between 10 and 500 Torr. The seed surfaces have been etched in hydrogen in order to remove the residual damage due to seed surface polishing. Screw dislocation free Lely platelets have been carefully selected in order to eliminate step sources on the seed surface and force growth by two dimensional island nucleation.

Cross-sectional TEM of seed/layer interface revealed presence of a band of stacking faults (Fig. 1) with thickness between 1 and 20 μm. The total number of faults in the band was between 2 to 100. The stacking sequences of the faulted band have been analyzed by high resolution TEM as a function of growth conditions. With the increasing growth rate and the silicon overpressure, the probability of cubic stacking is increasing. Bands of up to 6 bilayers with the cubic stacking were observed. This stacking disorder was interpreted as due to low stacking fault energy in SiC polytypes and 2D island nucleation on step free seed surface.

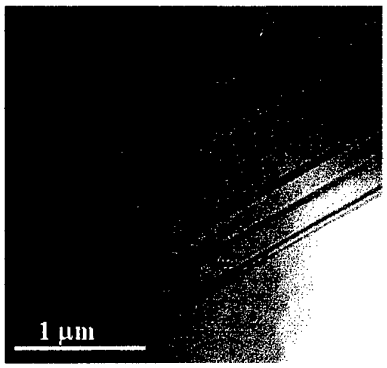


Fig. 1 Stacking faults observed by TEM at the Lely seed-crystal interface.

After island coalescence, different stacking sequences in neighboring islands are accommodated in the form of partial dislocations with the dislocation line in the basal plane. Existence of both Shockley and Frank partial dislocations has been inferred from the analysis of stacking sequences. A model of threading edge and screw dislocation nucleation associated with the presence of stacking faults along the interface is proposed.

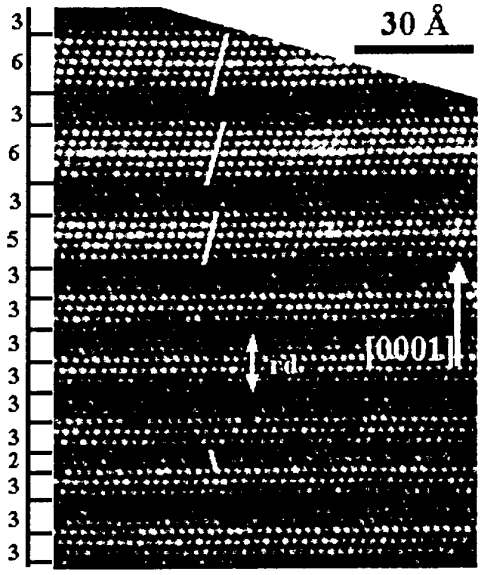


Fig. 2 High resolution TEM image showing stacking disorder during 2D SiC growth.

Solid phase epitaxial growth of different polytypes of bulk single SiC crystals

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Introduction

Physical Vaport Transport (PVT), Liquid Phase Epitaxy (LPE) and High Temperature Chemical Vapor Deposition (HTCVD) are the main reported growth techniques for the fabrication of bulk SiC single crystals. More recently, solid phase epitaxy has proved its potential to process high quality bulk 6H-SiC bulk crystals [1].
In this paper, the solid phase epitaxial growth of different SiC polytypes is described and discussed.
A single crystal seed of 35 mm in diameter and a 50 mm polycristalline 3C-SiC wafer were miror-polished and firmly assembled. Seeds of different polytypes has been used. The solid phase epitaxial growth was conducted in a graphite crucible heated at high temperature (2600 K) and for an argon pressure of 400 Pa. SiC powder surrounds the crucible chamber. A thin wall of porous graphite separates the chamber from the powder. The other parts of the reactor were kept identical as in our sublimation reactor [2]. In figure 1, the thermal fields in the standard reactor used for PVT and the modified reactor for SPE are shown.

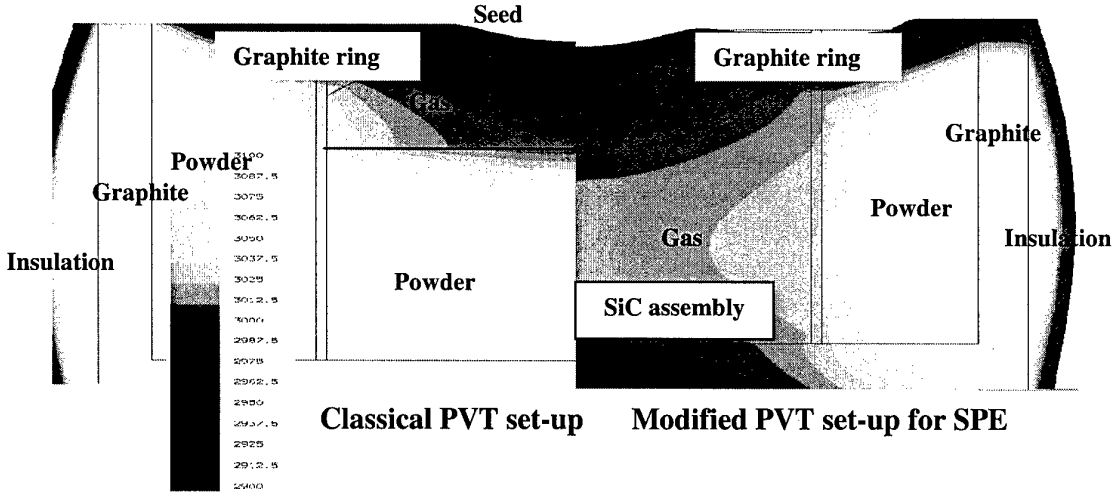


Figure 1 : Thermal fields in the PVT reactor (right) and in the modified reactor for SPE (left).

Results and discussion

The results show that solid phase epitaxy has been effective for the growth of bulk single crystals. The epitaxial alignment of the polycrystalline 3C wafer in the polytype of the seed

can be induced in the temperature and temperature gradient fields depicted in figure 1 and in an ambiance containing Ar, Si_2C, SiC_2 and Si.
Milita et al. [3] have already analyzed by X-Ray synchrotron topography the solid phase epitaxy process. In the classical PVT seeded technique, the SiC crystal growth occurs in two distinct region. In its core, there is the main crystal which is of high crystalline quality and grows directly above the seed. Around the main crystal, on the graphite lid, grows at first small misoriented crystallites. The crystallites with a common axis and similar in orientation to the main crystal grow faster at the expense of the randomly growing crystallites, which finally disappear. The correlated crystallites finally are integrated into the main crystal. This in situ solid phase epitaxy allows the enlargement of the growing crystal. This phenomenon is the driving force for the SPE process.

Conclusions

We have shown that the recrystallization of polycrystalline 3C-SiC wafers can be induced from single SiC crystal seeds by a solid phase transformation at temperatures above 2300 K and in an ambiance containing Si- and C- gaseous species. The rate of transformation is about 300 μm/h. If the annealing time is prolonged, the crystal quality of the grown crystal improves and the resulting epitaxial layer contained only a small amount of crystallographic defects.

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Dislocation constraint by etch back process of seed crystal in the SiC bulk crystal growth

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In this study, we report on the dislocation and defects constraint in the initial SiC growth using the etch back process by the modified Lely method. The seed crystals for the growth were prepared by three kinds of 6H-SiC crystals. One is the as-grown crystal with 3mm thickness developed by the Lely method, which has a shell like shape composed of (0001) plane and hexangular pyramidal planes. Others are (0001) plate crystals with 0.5~7mm thickness grown by the Lely and the modified Lely methods. The seed was fixed on the lid (ϕ10x5mm) projected from the top to the inside of the carbon crucible, and the raw material of the SiC powder was filled in the bottom. In this structure, the seed crystal more than 2mm thick initially is etched back soon after reaching the general growth condition in the crucible. The turning from the pre-growth etch back to the growth could be performed without changing heating condition of the crucible. This process has been performed for optimizing the surface condition on the seed crystal and effected on the dislocation and defects constraint in the initial growth. Possible reasons of the etching mechanism and the defects constraint will be discussed in the session.

Fig. 1 is an X-ray topograph obtained with $g=11\bar{2}0$ from the sectional specimen of the SiC crystal grown by the modified Lely method on a (0001) Lely plate seed crystal with 0.5mm thick. As the seed crystal is less than 2mm thick, the pre-growth etch back process could not be performed in this case. The crystal quality of the Lely seed crystal seems to be perfect, however, an intense broad line (A) on the interface between the seed and the grown crystal and many fine lines (B) elongated along the growth direction from the seed surface can be observed. (A) shows that the grown crystal layer is distorted by the high density of dislocation [1]. On the other hand, (B) shows strain fields from line defects such as micropipes and screw dislocations. It seems that the high density of dislocations are connecting each other during the growth, and release stress as a result of their combination. If the stress is released imperfectly, the dislocations appear like a line defect of micropipes and/or screw dislocations, which is considered as one of the reasons for defects generation in the modified Lely crystals.

The second SiC growth was performed on the as-grown Lely seed crystal. Fig. 2 is an optical micrograph obtained from the sectional specimen of the grown crystal, which contains both images of the seed crystal and the grown crystal. The figure shows that the grown crystal has no micropipe. The top part of the crystal in Region α was sublimed and was etched back before the start of the growth, the height of the seed crystal was decreased from 3mm to 2mm till the dome like shape. This etch back was automatically switched over to the growth. On the other hand, the Region β is the grown area on the unetched surface that is original surface of hexangular pyramidal planes of the as-grown Lely seed crystal. Therefore, before the start of the growth, the top surface first converts to the dome like shape drawn by dots line of L in the

schematic figure, and then the crystal became thicker with the further growth. Fig. 3 is it's x-ray topographs obtained with $g=11\bar{2}0$. The high density of dislocation is only observed between the unetched surface of the seed crystal and the grown crystal (Region β). Moreover, many line defects are propagated from there. However, the grown crystal on the etched top of the seed crystal shows no high density of dislocation and low line defects (Region α). It seems that the pre-growth etched surface of the seed crystal is effective to restrain of defect propagation in the SiC crystal growth.

When the pre-growth etch back process was performed for the seed crystals prepared from modified Lely crystals, we succeeded to constrain not only the high density of dislocation but also micropipes. This interesting phenomenon could be found in the interface between the seed crystal and the grown crystal from the observation using optical microscope as shown in Fig.4. We observed that many micropipes terminate just below the interface, which is the first observation in the SiC crystal growth by the modified Lely method. The density of the micropipes in the grown crystal decreases to about 1/10 comparing with the seed crystal.

This work was performed as a part of the MITI NSS Program (Ultra-Low Loss Power Device Technology Project) supported by NEDO.

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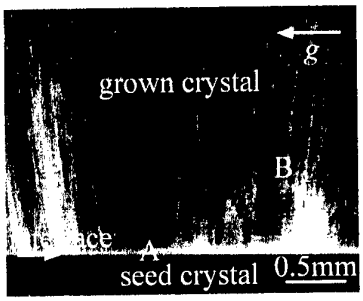


Fig. 1 X-ray topograph of the SiC crystal grown in the (0001) Lely plate crystal.

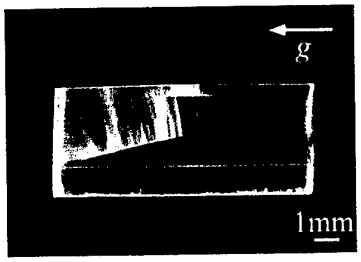


Fig. 3 X-ray topograph obtained with $g=11\bar{2}0$ from the same specimen observed in Fig. 2.

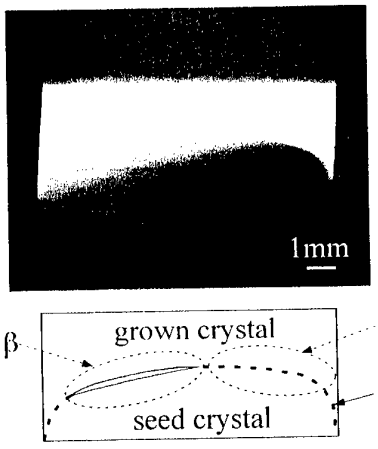


Fig. 2 Optical micrograph obtained of the SiC crystal grown on the as-grown Lely seed crystal.

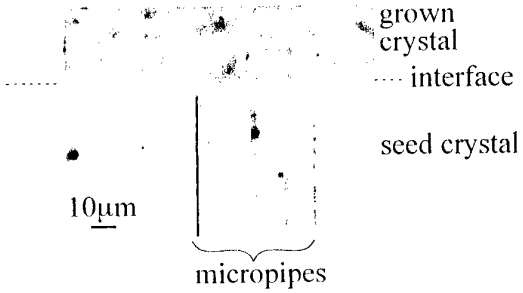


Fig. 4 Optical micrograph showing several terminated micropipes in the interface region between the seed crystal and the grown crystal.

The Nucleation of Polytype Inclusions During the Sublimation Growth of 6H and 4H Silicon Carbide

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Silicon carbide (SiC) possesses a host of electrical and physical properties that make it ideally suited for use in high temperature, high frequency, and high power devices. One of the most interesting properties of SiC is that it can take the form of over 200 different polytypes, a one-dimensional version of polymorphism. Each polytype has a set of electrical and physical properties that is unique. Therefore, controlling the formation of different polytypes is a key ingredient in controlling the properties of SiC devices. Recent progress in the physical vapor transport (PVT) growth of silicon carbide crystals has resulted in single crystal wafers of the two most common polytypes, 4H and 6H, up to 100 mm in diameter [1]. However, the nucleation, or switching of different polytypes during PVT growth is still not understood and has been shown to result in the formation of micropipes and dislocations in SiC crystals. [2].

In this study, polytype nucleation during the growth of both 6H and 4H single crystal SiC was investigated. The polytype inclusion's morphologies were examined and related to growth conditions. It was observed that polytype inclusions nucleate at the outer edge of the central growth facet. They then propagate along the a-direction toward the edge of the wafer in a fan like band. Cross-sectional investigation showed that these polytype inclusions were arranged in bands of c-planes, which originate at a single point on one c-plane, see figure 1. The inclusions were observed to then grow outward along the c-plane and upward along the c-direction. Investigation of the nucleation point revealed the existence of voids or inclusions of an as yet unknown origin. The existence of these voids and their possible relevance to polytype inclusions will be discussed, along with an explanation of what may be occurring at the growth surface during polytype switching.

It was also observed that the polytype inclusions have a devastating effect on the crystal quality. In particular, the nucleation of polytype inclusions was linked to the nucleation of micropipes. The boundaries between different polytypes are aligned with micropipes, suggesting that the inclusions were a nucleation point for these micropipes. In cross-section, the micropipes were indeed observed to originate on the c-plane where the polytype changed, see figure 1. The micropipes were also seen to bend at different angles when propagating through different polytypes. An explanation of this observation is presented and its possible relevance to the polytype nucleation discussed.

A detailed investigation of the PVT growth of both 4H and 6H SiC will be presented to explain the formation mechanisms involved in polytype inclusion nucleation, based on the morphologies, growth conditions and experimental evidence obtained during PVT growth.

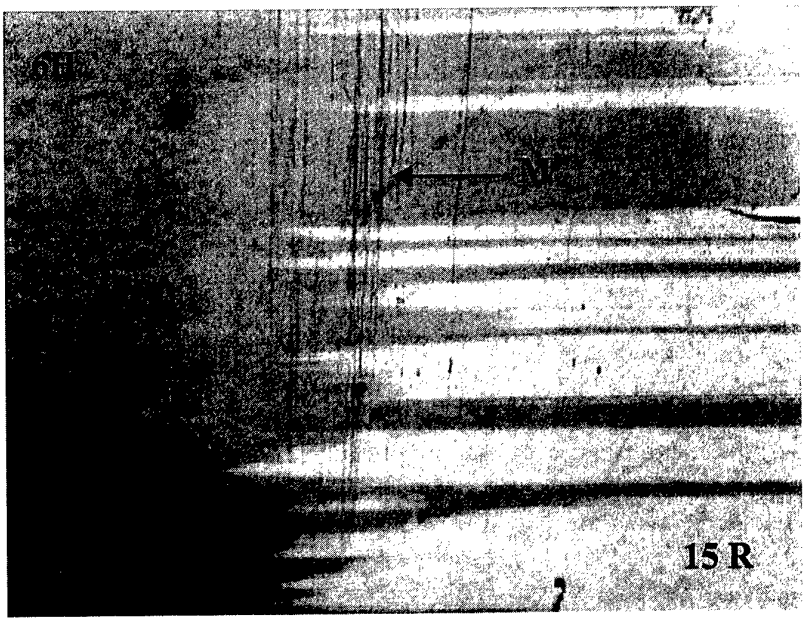


Figure 1 - Optical transmission image of a 6H SiC boule with 15R inclusions. The polytype inclusions all start at a point (such as the one labeled P) at the edge of the central growth facet. Micropipes (labeled M) can be seen originating at the polytype nucleation point and propagating into the growth.

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Acknowledgements

This research is funded partially by Air Force Research Laboratory, U.S. Department of Air Force, under the contract number: F33615-99-C-5317.

Aluminum Doping of 6H and 4H SiC with a modified PVT Growth Method

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Aluminum doping of SiC single crystals with powder source results in a exponential axial decrease in charge carrier concentration caused by aluminum source depletion and defect generation through high initial aluminum concentrations [1]. Therefore we applied an additional gas flow to the PVT-Growth-Setup leading direct into the growth cell [2]. Thus a continuous supply of aluminum atoms out of an external reservoir was possible. The concept will be discussed.

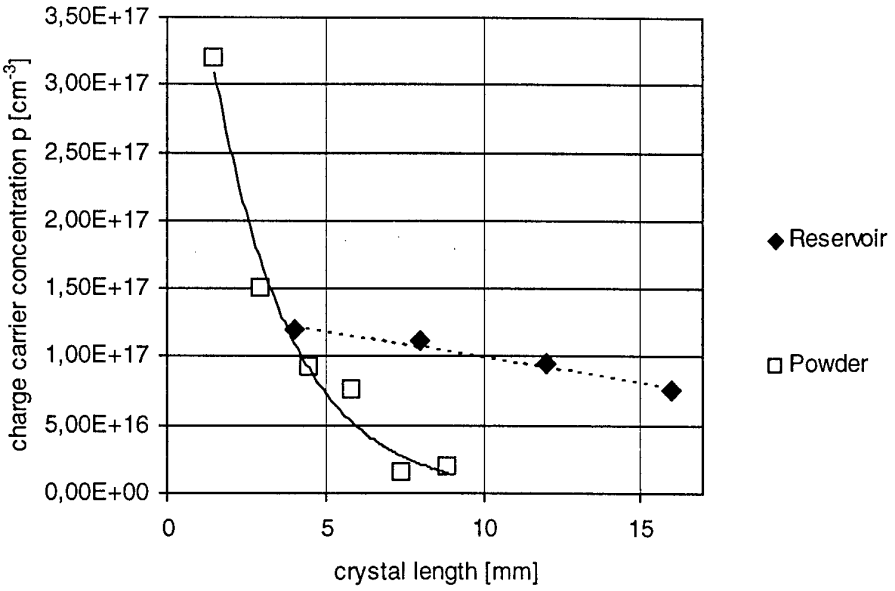


Fig.1: Axial charge carrier distribution (Hall measurement) in 6H-SiC-crystals grown on the Si-side with aluminum in the powder (white squares) and with external source (black rhombuses).

With the Modified-PVT-Method high quality crystals with improved axial (4H: $2 \cdot 10^{16} cm^{-3} < p < 4 \cdot 10^{16} cm^{-3}$; 6H: $8 \cdot 10^{16} cm^{-3} < p < 1{,}2 \cdot 10^{17} cm^{-3}$, Fig. 1) and lateral (4H: $\Delta p/p < 10\%$; 6H: $\Delta p/p < 25\%$, Fig. 2) charge carrier homogeneity were grown.

The Dependence of the remaining doping variations on compensation with residual nitrogen and growth mechanisms and measures for further improvement will be discussed.

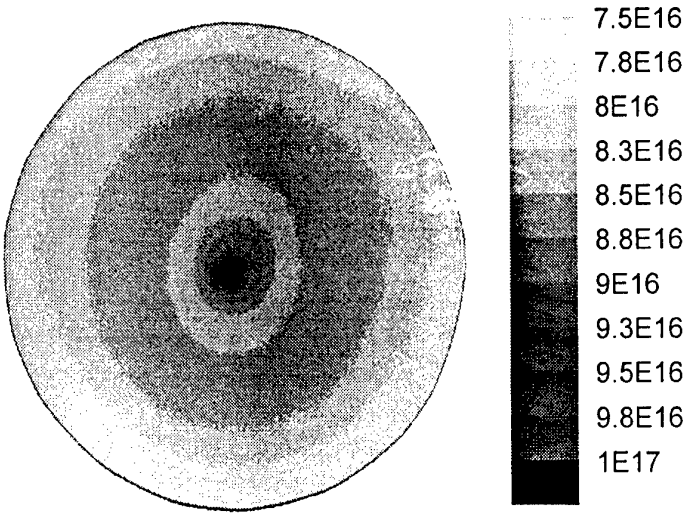


Fig.2: Absorption mapping of a 6H wafer with monochromatic light of 570 nm [3]. The bright parts indicate areas with low charge carrier concentration. Units: cm^{-3}.

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Macro Defect Generation in SiC Single Crystals Caused by Polytype Changes

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The generation of macroscopic defects like radial cracks [1] was discussed in terms of stress induced micropipe formation and agglomeration. Low angle grain boundaries (frequently referred to as domains up to some millimetres in length are visible as linear features extending radial inward from the wafer edge and generally following low-index crystal planes. They may sometimes extend through the entire wafer thickness [2]. Recently, the domain structure was attributed to the polygonization of threading edge dislocations, resulting in a low angle tilt boundary array [3].

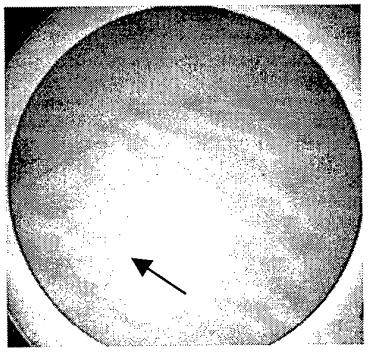


Fig.1
Extended slits perpendicular to the basal plane
(wafer diameter 32mm)

Another category of grown-in type macro defects will be discussed in this paper. They can be described as slits bordered by two walls with a linear extension up to some millimetres and a distance between them in the micrometer range (Fig.1). The slits are extended in the basal plane, preferentially in $<1\bar{1}00>$ respectively $<11\bar{2}0>$ direction, and are running in a plane parallel to the growth direction. They are often bordered by macro-pipes [4]. In dependence on the growth conditions the slits are stabilised and may penetrate the whole crystal or disappear.

Single crystals of the 4H- and 6H-polytype with diameters up to 35mm and micropipe densities between 50 and 200 cm^{-2} were grown in a temperature range from 2100°C to 2250°C. Seeds with 3.5° (6H) respectively 8° (4H) off-orientation to $<11\bar{2}0>$ were used. For 4H-crystals only the C-terminated surface was considered. Crystals were nitrogen doped with concentrations from 7 x 10^{16} - 10^{19} cm^{-3}. The defect evolution within the crystals was investigated using Optical Microscopy, Scanning Electron Microscopy (SEM), Electron Beam Induced Current (EBIC) and KOH-etching methods.
EBIC images revealed that bundles of preferentially basal dislocations are located between isolated slits (Fig 2) and are assumed to be responsible for the slit generation across a long distance in the basal plane as well as in regions below the starting point of the slits (Fig.3). Under certain conditions the induced dislocation bundles may prevent the growth of material above it resulting in a slit. Their existence itself is strongly correlated to the presence of polytype changes. Therefore, the deterioration of the crystal perfection at the polytype borders seems to be the origin of the slit generation, which is especially observed during the growth of 4H-crystals. Polytype stabilising parameters, useful to suppress the generation of the described defects, will be discussed.

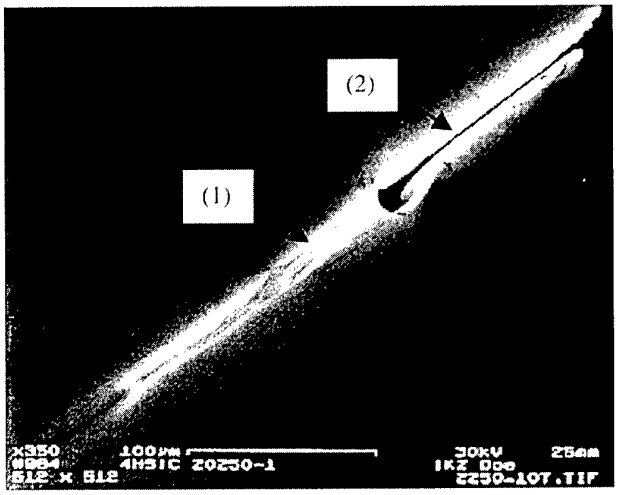


Fig. 2 Dislocation bundle (1) associated with a slit (2) (basal plane), EBIC

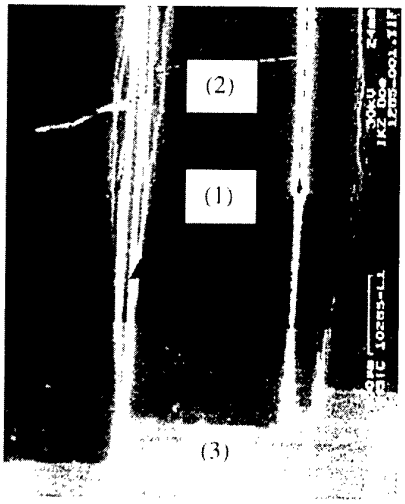


Fig.3 Dislocation bundles (1) below the slit (2) starting at steps of polytype lamellas (3), (EBIC) (growth direction upwards)

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Chemical vapor deposition growth and characterization of shape memory SiC nanorods

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Nano-sized SiC structures are useful for the improvement of mechanical and thermal properties of nanocomposite materials due to their high strength, high elastic modulus, low density, high thermal and chemical stability. The large bandgap property of SiC also enables SiC nanostructures to be potentially applicable for nanoelectronic and nanophotonic devices designed to operate at high temperature, high frequency, etc [1-3].

In this work, we report a shape memory synthesis of SiC nanoscale structures at lower temperature. Our technique consists of the growth of carbon nanotube over Fe-Co catalyst loaded SiC wafer and the subsequent growth of SiC nanorods by a chemical reaction of CNT with TMS in a rapid thermal chemical vapor deposition (RTCVD). The Fe-Co catalyst was supported on an ultrasonic cleaned Si(100) wafer by dipping into aqueous solution (10^{-3}M) of corresponding metal salts ($Fe(NO_3)_3 \cdot 9H_2O$: $Co(NO_3)_2 \cdot 6H_2O$ = 1 : 1). After Fe-Co supported Si wafer was washed with DI water, it was dried in an oven at 100^0C for 1 h. For the growth of CNT, the metal loaded substrate was placed in the base area of a quartz plate and fixed in the central hot region of a RTCVD reactor [4]. The grown CNTs was insitu etched for 5 min by 200 sccm H_2 gas at 900^0C and the growth of SiC was performed for 30 min over the CNT at 1100^0C with 1.0/200 sccm TMS/H_2. The structural and optical properties were investigated using various analytic techniques.

Figure 1 shows SEM images of the grown SiC nanostructures. The figure reveals the growth of large quantities of straight and curved nanorods across the whole substrate surface. The nanorods with approximately 1 μ m length are randomly oriented over CNT grown for 1 min (Fig. 1(a)). However, the length of SiC nanorods significantly increases as the growth time of CNTs increases (Fig. 1(b)). IR spectra for both the samples showed a strong C-Si stretching vibration absorption peak at 805cm^{-1}, which confirms the growth of SiC. The appearance of a XRD peak at $2\theta = 17.5^0$ also indicates the growth of the zinc blend β-SiC nanorodes [1,5]. The intensity of the SiC peak at

$2\theta = 17.5^0$ increased with the growth time.

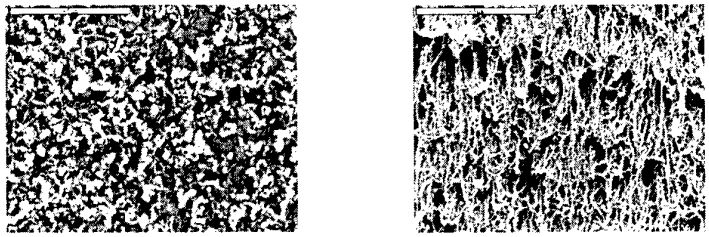


Fig. 1: SEM images for SiC nanorodes; (a) CNTs grown for 1 min. (b) CNTs grown for 10 min.

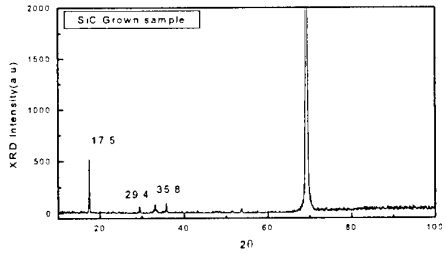


Fig.2: XRD spectrum for SiC.

We have also investigated the temperature effect on SiC growth. No evidence of the growth of the SiC nanorodes was found from the samples grown at 900 and 1000^0C, respectively. The presence of a sharp peak at $950cm^{-1}$ in the Raman spectrum recognized the LO mode of the SiC lattice [6]. The intensity of the Raman peak at $950cm^{-1}$ increases as the relative growth time of SiC increases, indicating that SiC nanorods are formed by the conversion of CNTs into SiC. EDX was also showed the stoichiometric growth of SiC nanorods. PL peak was observed at an emission energy of 2.3 eV, indicating the growth of the SiC nanorods [6].

Acknowledgements

This work was supported by KRF Grant (KRF-99-005-D00036) through the Semiconductor Physics Research Center at Chonbuk National University.

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OPTIMIZATION OF INTERFACE AND INTER-PHASE SYSTEMS : THE CASE OF SiC AND III-V NITRIDES

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Modern crystal-growth techniques can now afford a wide panoply of heterosystems for applied physics purposes. A comprehensive understanding of the problems involved in growth experiments implies the macroscopic and microscopic aspects of interface physics. Although the latter aspect is relevant to the very first stages of the growth process, the first aspect (of heteroepitaxy) must be taken into account because not only local features but also periodic and long-range features can influence the process. This is for example the case of Lomer dislocations which may be created at the interface between two host materials with mismatched lattice parameters when the overlayer thickness exceeds a critical value. An energy balance between strain-associated elastic energy and dislocation formation energy determines the overlayer critical thickness beyond which misfit dislocations (MD's) are energetically more favored than strains.

The lattice misfit between two materials A and B is related to the difference between their lattice parameters $\Delta=|a_A-a_B|$. The dislocations which are created when the conditions of strain relief are fulfilled are characterized by a geometric feature, namely the associated Burgers vector. At a nanometric scale, the elementary quantity which we may define is a "small" Burgers vector $b_e=a_B-a_A$, with $a_B>a_A$: b_e represents a rather small fraction of the lattice parameters. In the case of perfect epitaxy, b_e corresponds to small epitaxial dislocations. By a vernier effect, we end up with a network of epitaxial MD's which are fairly parallel with a lattice spacing equal to L. Their density is low when Δ is small: if $b_e \rightarrow 0$, one may expect that $L \rightarrow \infty$, ensuring a very small dislocation density. The appearance of the MD's corresponds to a negative free energy associated with these defects, as they aim at relaxing interface strains. The lattice spacing L is usually obtained by applying the following geometric conditions:

$$(n_1+1)a_A=n_1a_B\ ;\ n_1=a_A(a_B-a_A)^{-1}\ ,\ \text{if } a_A<a_B \qquad (1)$$

$$(n_1+1)a_B=n_1a_A\ ;\ n_1=a_B(a_A-a_B)^{-1}\ ,\ \text{if } a_A>a_B \qquad (2)$$

If we consider , e.g., Eq. 1, it states that after n_1 jumps on the lattice B and (n_1+1) jumps on the lattice A, we may find in coincidence two interface sites belonging respectively to A and B. In the framework of the geometric approach L is then calculated by using the value of n_1 and the expression of the corresponding Burgers vector. Within this approach, we can learn that the best host materials for heteroepitaxy are those providing the highest value of L, i.e., eventually the lowest MD density.

In what follows, we will show that not only the geometric features of host materials are relevant to heteroepitaxy but also those features related to their elastic properties, through which the temperature effects are also involved as these elastic features are temperature dependent. The idea of taking account of these elastic features can be derived by analyzing the elasticity theory equations. These equations relate strain to lattice dynamics features

through relationships involving the $S=f(C_{ij})/\rho$ factor, where ρ is the density. For each interface configuration, i.e., for a specific growth plane, the dynamics equations involve effective elastic constants $f(C_{ij})$ which correspond to elastic waves propagating along the principal symmetry directions in cubic crystals. The expressions of $f(C_{ij})$ for the longitudinal and transverse modes are given below respectively for the [100], [110] and [111] directions:

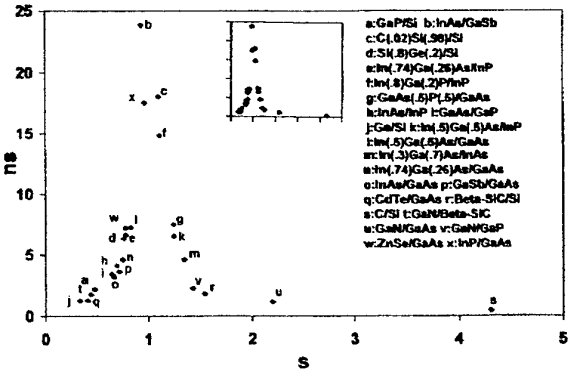
- For longitudinal modes:

$$f(C_{ij})=C_{11}\ (a),\ f(C_{ij})=C_{11}+C_{12}+2C_{44}\ (b),\ f(C_{ij})=C_{11}+2C_{12}+4C_{44}\ (c) \qquad (3)$$

- For transverse modes:

$$f(C_{ij})=C_{44}\ (a),\ f(C_{ij})=0.5(C_{11}-C_{12})\ (b),\ f(C_{ij})=(\ C_{11}-C_{12}+C_{44})/3\ .\ (c) \qquad (4)$$

The relevance of these elasticity-related features for a number of effects characteristics of coherent epitaxial solids and for epitaxy-induced structural phase transformations has been discussed in refs. In our approach, we derive renormalized expressions -n_S - of the geometric factor n_1 showing the effect of the ratio S of the $S_{A,B}$ factors (effective elastic constants) of the substrate and the epilayer in the case of B/A heterostructur involving one interface. The relevance of S is depicted on the following figure for several heterostructures including nitrides-based systems. One can see that the highest values of n_S, i.e., the smallest MD's densities are obtained for $S\cong 1$ and that n_S decreases when the mismatch of the S_A and S_B factors increases.



For systems where a large lattice mismatch exists between the host materials, the strategy of growing buffer layers before the elaboration of the final overlayer is currently widely used. These transitional layers are aimed at ensuring a continuous matching of the relevant features of the host materials (substrate and overlayer) selected for the growth experiment. It is then important to develop reliable and well-based criteria in order to make an optimized choice of the buffer layer. These criteria are formulated by the continuity conditions for geometric (n_S) and elastic factors (S).

The epitaxial growth of GaN by modern growth techniques as metalorganic chemical vapor deposition is usually made by using sapphire as substrate. Despite the large lattice mismatch between these two materials (> 12 %), which implies, in principle, that a high density of dislocations may be present in the epilayer, it has been demonstrated that devices showing surprisingly high performance may be obtained. Defects which could damage the interface quality of the heterostructure are related to the existence of interface defects between misoriented domains in the GaN overlayer, consisting in low-angle grain boundaries. An alternative to the use of sapphire substrates can be provided by SiC because of a better lattice matching and closer thermal expansion. This is expected to give improved crystalline characteristics. One possible strategy to increase this crystalline quality is to introduce a AlN buffer layer. Thus we demonstrate that the matching at the AlN/SiC interface of the dynamics-strain related factors is improved. These previsions show that the SiC-substrate alternative with the use of AlN buffer layer is a valuable approach for GaN heteroepitaxy.

Theoretical investigation of an intrinsic defect in SiC

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Many unidentified intrinsic defects have been measured in the photoluminescence (PL) and Raman spectra of irradiated SiC. The best known ones are the so-called D_I and D_{II} PL centers [1,2] found in H^+, He^+ and C^+ bombarded SiC samples. These are stable up to 1700 °C. The D_{II} center shows five localized modes above the phonon continuum from 1031 cm^{-1} up to 1328 cm^{-1}. Since the D_{II} center is formed after carbon implantation, local a carbon excess is expected to give rise to these bands. Dramatic changes occurred in the Raman spectrum as the implant concentration was varied from 10^{20} H^+ ions/cm^3 to 10^{22} H^+ ions/cm^3. New peaks appeared at 1080 and 1435 cm^{-1} and at 1400 and 1600 cm^{-1} [3].We call these centers R1 and R2, respectively. The first two peaks disappeared simultanously at 800 °C, while the last two at 600 °C. Based on the higher dose of implants it is expected that more Si vacancies are created while the annealing behavior shows that these centers contain mobile ingredients, most probably carbon interstitials. These centers have been known since decades but very little additional information is available about them.

The conditions of the creation of these centers imply that carbon interstitals play a crucial role in them. We have investigated the carbon di-interstitial defect in a silicon vacancy in 3C- and 4H-SiC. *Ab initio* calculations using the local density approximation of the density functional theory and norm-conserving pseudopotentials have been carried out on supercells in both polytypes. The LVMs and the occupation levels have been determined.

The calculated LVMs of this complex are at 1413 cm^{-1} and 1155 cm^{-1} (double degenerate) in 3C-SiC. Both modes are Raman active. The calculated frequencies are reasonably close to the measured ones (at 1435 and 1080 cm^{-1}) in the Raman spectrum, thus we suggest this defect as the microscopic model for the R1 center. The carbon isotope shifts in the vibration modes are predicted as a means to confirm our model experimentally. It is found that the defect complex can act both as a double electron and as a hole trap. The predicted occupation levels should be measurable by deep level transient spectroscopy (DLTS).

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Modification of SiC Properties by Insertion of Ge and Si Nanocrystallites — Description by *ab initio* Supercell Calculations

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The use of SiC for optical applications is limited by its indirect character. According to the k-conservation rule, at the fundamental gap direct transitions cannot contribute to luminescence or absorption. However, defects or nanostructures destroy the translational symmetry and thus make it possible to circumvent this problem. Hence we study Ge and Si nanocrystallites embedded in SiC. These structures are expected to be suitable for luminescence in the visible spectral range even including the blue [1]. Nanostructures of this kind have been produced by ion implantation in amorphous SiO_2 matrices, by electrochemical etching, or by Stranski-Krastanov growth in molecular beam epitaxy [2,3].
In order to achieve electroluminescence, a host material which can be doped, and which has an appropriate band gap is needed. The wide-gap material SiC will be a convenient matrix material. In fact, recent results of ion implantation with subsequent annealing of Ge nanocrystallites in SiC provide the experimental background and the incentive of our work. An example of such a Ge dot is shown in Fig. a) [4]. The questions to be answered by experimentalists and theorists include those of composition and structure of the embedded dots as well as the influence of the embedment on the structure of the inclusions. Indications have been found of hexagonal Ge as well as of GeC phases embedded in hexagonal SiC.
Our main goal is the parameter-free description of the optical properties of these systems. The qualitative description of the different influences allows recommendations to experimental groups in order to achieve luminescence from embedded nanocrystallites.
The spectral properties of the nanocrystallites are described within Density Functional Theory (DFT) in Local Density Approximation (LDA) and by means of the Projector-Augmented Wave (PAW) Method. The dielectric function is calculated from transition matrix elements and band energies using a quadratically extrapolative tetrahedron method [5]. We study spherical Ge and Si nanocrystallites of 5 to 239 atoms embedded in cubic SiC as well as free, hydrogenated nanocrystallites to simulate embedment in a wide-gap semiconductor. Finally, we also show results for nanocrystals in hexagonal SiC.
We use the supercell method which starts from one large cell of host material with one nanocrystallite. This building block is now repeated infinitely in all space directions. Thus our material is a composite made of the nanocrystals surrounded by SiC. We show that by means of an effective medium theory it is possible to extract the optical properties of the nanocrystals and to calculate the behavior of a new composite material with other filling factors. The dot-related quantities are size dependent due to quantum confinement effects. They depend on the type of dot material, the dot-host interface, and the shape of

the nanocrystals as well as on strain. Furthermore, the insertion of the quantum dots also alters the behavior of the host. Along with the interaction of neighboring nanocrystals, this is one limitation to the applicability of effective medium theories for systems with low barrier heights for electrons and holes or even for type-II heterostructures, e.g., Ge nanocrystals in cubic SiC. For systems with high barriers, the extraction of $\varepsilon_{\mathrm{dot}}(\omega)$ is simple and precise. We compare the results to absorption spectra of embedded Ge crystallites.

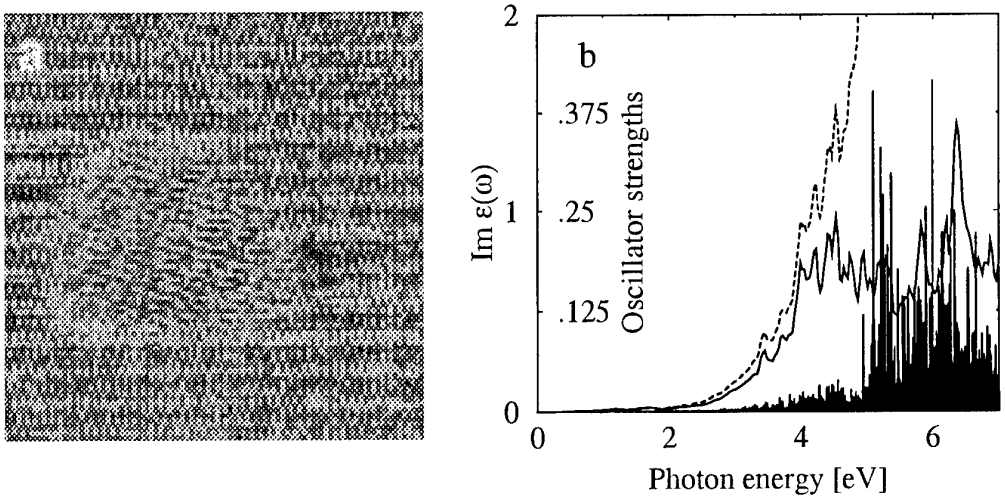


Fig. a) Example of a Ge dot in SiC, TEM picture [4], and b) Contribution of the gap states (solid line) to the total $\varepsilon(\omega)$ (dashed) and oscillator strengths (bars) of 41-atom Ge dot in 512-atom SiC cell.

The luminescence properties of any material are governed by the lowest few transitions. An example of oscillator strengths and the contribution of the gap states to the spectrum are shown in Fig. b). We have identified the origin of the important transitions, i.e., we have allocated them to the respective electronic states. It has been shown that the oscillator strengths and energies depend strongly on the shape and the strain of the crystals as well as on the dot-host interfaces. After all, a consistent picture encompasses the densities of states, the bandstructures, and the optical spectra.

In order to obtain results which represent real systems it is necessary to include the excitation aspect and to go beyond the LDA approximation in the electronic structure calculation. First results of self–energy calculations within the GW approximation are presented. Furthermore, excitation energies are calculated within the ΔSCF method.

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Theoretical calculation of stacking fault energies in silicon carbide

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We report on a first-principles calculation of stacking fault (SF) energies in 3C-, 4H-, and 6H-SiC based on density-functional theory within the local-density approximation. All the structurally different SF in 3C-, 4H-, and 6H-SiC, which can be introduced by glide along the (0001) basal plane, are considered: 3C-, 4H-, and 6H-SiC have one, two, and three geometrically distinguishable SF, respectively, as shown in Fig.1. The SF energies are calculated using both a supercell method and the generalized axial next-nearest-neighbor Ising (ANNNI) model [1,2]. To confirm the accuracy of our calculation, the SF energies of Si and diamond are also calculated using the supercell method since the corresponding experimental values are known and relatively well established. Our theoretical calculations show very good agreement with available experimental results. Our calculation confirms that the SF energy of 3C-SiC is negative [3], and we also find that one of the three types of SF in 6H-SiC has considerably higher SF energy than the other two types (see Table I) [4].

The ANNNI model allows a simple, but still rather accurate, calculation of the SF energy in SiC from the results of several total energy calculations for perfect crystals (in this case from 2H-, 3C-, 4H-, and 6H-SiC). In order to model SF with the supercell approach, a very large number of atoms in the supercell is required (in the present study 96 atoms), and it is therefore very time-consuming. Our calculated inter-layer interaction parameters for the ANNNI model, from which one can determine approximately the SF energy for other SiC polytypes, give values which are very close to the available experimental data in the literature [2,4].

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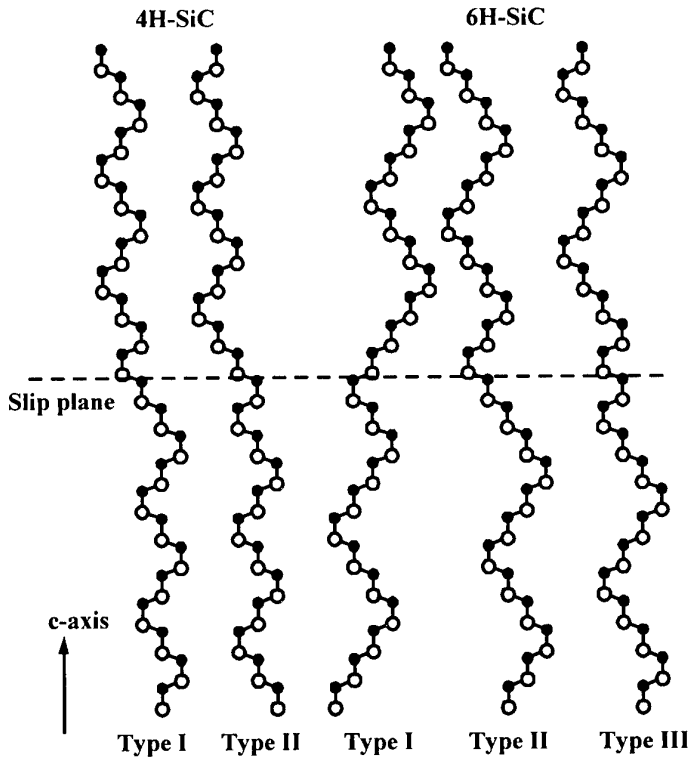


Fig.1. Geometrically distinguishable SFs in 4H- and 6H-SiC

Table I. Theoretical and experimental SF energies in 3C-, 4H-, and 6H-SiC (in mJ/m^2). Note that the ANNNI model does not distinguish between type I and type II SF in 4H- and 6H-SiC. To the authors' knowledge, structural differences between SFs have not been considered in the literature.

		3C-SiC	4H-SiC	6H-SiC
Supercell method				
	Type I	-1.80	17.7	3.35
	Type II	—	18.1	3.10
	Type III	—	—	40.1
ANNNI model				
	Type I	-6.27	18.3	3.14
	Type II	—	18.3	3.14
	Type III	—	—	36.6
Experiment				
	Ref.2	—	14.7±2.5	2.9±0.6
	Ref.5	—	—	2.5±0.9

Stacking fault interactions and cubic polytype inclusions in 4H-SiC

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A first-principles study of interacting stacking faults (SF) and polytype inclusions in silicon carbide, based on density-functional theory within the local-density approximation will be reported [1]. Polytype inclusions, i.e., the presence of different polytypes in a host crystal, have often been observed in hexagonal SiC polytypes. Although the mechanism for the creation of polytype inclusions is not known with certainty, one possibility is the motion of partial dislocations [2], each leaving behind an imperfect crystal containing a SF. If two partial dislocations having the same Burgers vector appear in neighboring (0001) planes, then a 3C-like inclusion can be created in the hexagonal crystal as shown in Fig.1. If still more partial dislocations are introduced, the thickness of the 3C-inclusion can increase (see Fig.1).

In another paper at this conference [3,4], we studied the effect of a single SF in SiC. In the present paper we introduce additional SFs in neighboring (0001) planes (note that SFs can not be present in all neighboring planes without violating the close-packing stacking sequence) and study the effect on the band structure. The calculations are performed using a supercell technique with 96 atoms per supercell (corresponding to 12 primitive unit cells for 4H-SiC). Figure 2 shows how the band structure changes as 1, 2, and 4 SFs in neighboring planes are introduced so as to convert a part of the 4H-SiC crystal to a 3C-like region. In the case of 4 SFs, the thickness of the 3C-like region is around 2.5 nm. We can see that, and as reported earlier [3,4], 1 SF splits off a band from the continuum of conduction band states, and that on increasing the number of neighboring SFs, this split-off band moves down in energy. This situation is of course consistent with a quantum well (QW) picture (the depth of the QW being equal to the conduction band offset between 3C- and 4H-SiC), where the ground state goes down in energy when the QW thickness increases.

The method has allowed us to study the effect of further SFs, SF-SF interactions and to analyze the wave functions, and will be discussed in the presentation.

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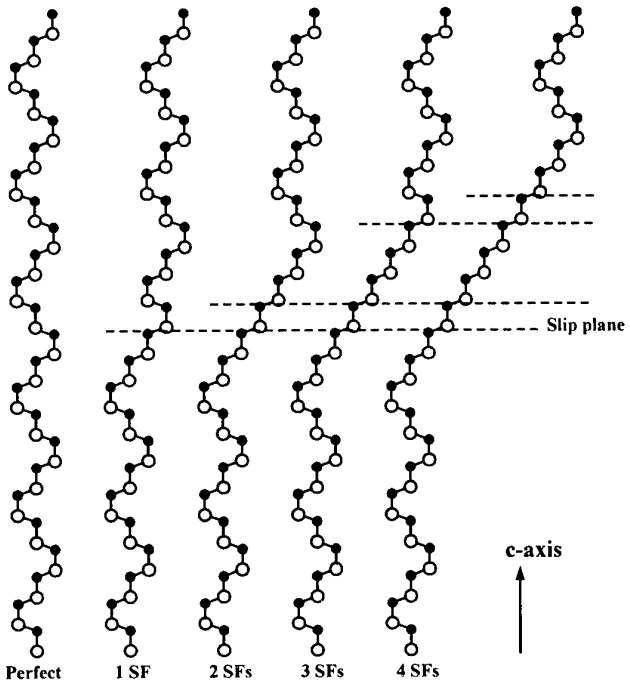


Fig.1. The creation of 3C-inclusions of various thicknesses in 4H-SiC by the stacking of SFs.

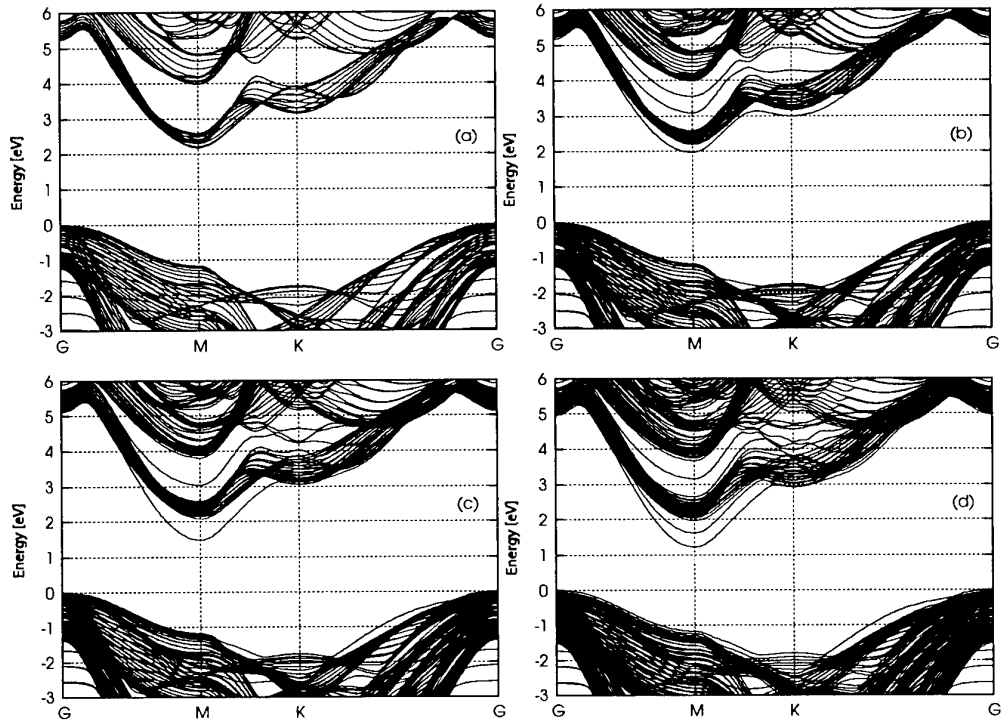


Fig.2. Band structures of (a) perfect 4H-SiC, (b) 4H-SiC with one SF, (c) 4H-SiC with two SFs, and (d) 4H-SiC with four SFs.

Ab initio calculation of B diffusion in SiC

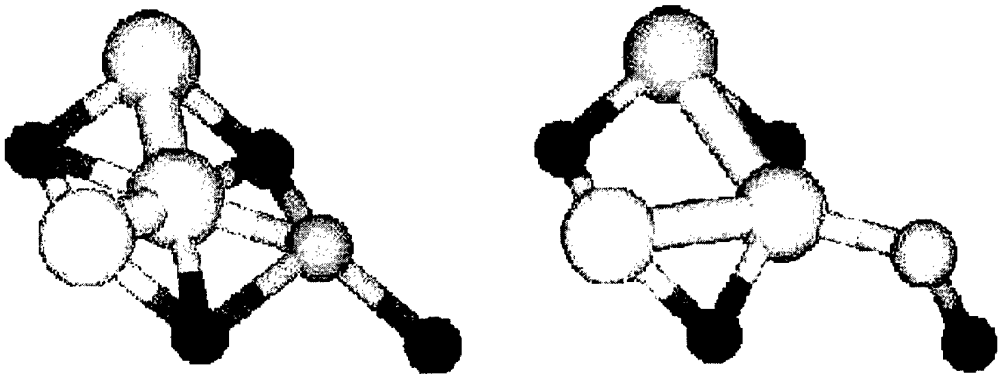
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Abstract
Boron diffusion in silicon has always been a high interest topic, experimentally and theoretically, due to the key role it plays in semiconductor doping processes. In silicon carbide, another material of growing interest in microelectronics, there are to date no theoretical studies on this topic.
Spin polarised *ab initio* calculations at DFT - LDA level were performed with a reasonable cell size (64 atoms) and a well-converged *k-point* sampling of the Brillouin zone. This combination of methods can be considered the *state of the art* in computational material science.
First the main defect configurations and their energy stability were analysed, both for the self interstitials (Si and C) and for B interstitial, in order to probe possible diffusion mechanisms, like Si kick-out [fig.1]. Then a path between two energy minima of a B interstitial was sampled, performing structural relaxations, but constraining the B atom to lay on a plane orthogonal to the selected path. This approach gave us valuable insight as to the diffusion path along the intermediate positions through which the B atom must go through, which normally are not taken into account in conventional studies, and how high the barrier to the diffusion is there.
B diffusion appears to be feasible, as the energy barrier to overcome is not very high (~ 0.6 eV). Moreover, another main feature of our calculations is that the diffusion mechanism that is conventionally postulated, consisting of a hopping process between a tetragonal position and a hexagonal position, appears to be too simplified and may give rise to lower barriers than the real ones. An unexpected result was that more than one, non-equivalent path between two minimum energy positions do exist [fig.2].

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Figures



(a) (b)

Figure 1 –B kick out. The configuration with a substitutional B in a Si site is made unstable in presence of an interstitial Si gets closer (a). The relaxed configuration (b) shows that to achieve equilibrium B is displaced and Si almost takes its own site back.

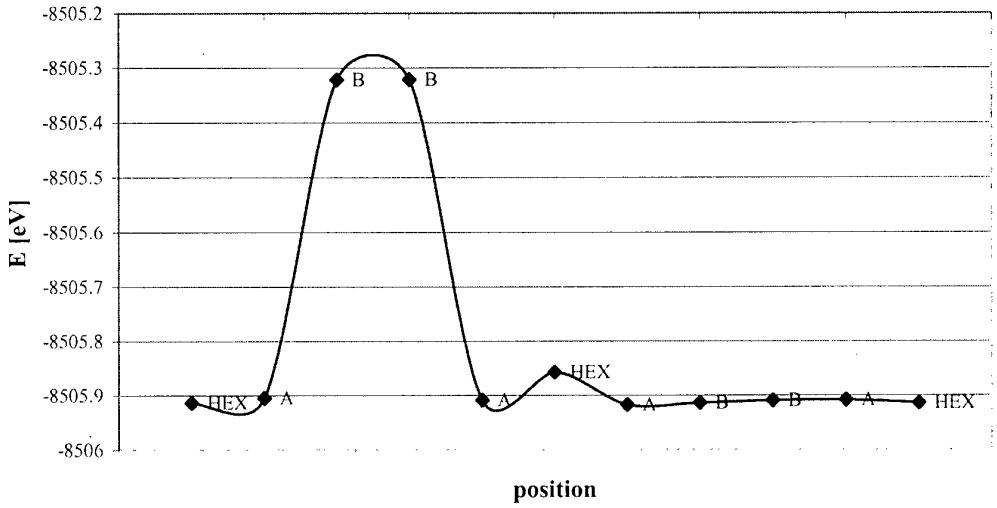


Figure 2 – Diffusion barrier. B diffusion along two different hexagonal-hexagonal paths. One presents a diffusion barrier around 0.6 eV, the other has no barrier.

Theory of Boron-Defects in SiC

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Boron as an acceptor-center in SiC has attracted much attention. Experiments have been focused on the electronic structure of boron-related centers [1,2], the electrical activation of the acceptor [3] and the properties of boron diffusion [4]. Though progress has been made in the understanding of the boron diffusion [5,6], the origin of experimentally observed boron centers is still unclear. While theory predicts substitutional boron acceptors on the carbon and silicon sublattice [5,7], in experiments only the shallow boron acceptor at a silicon site (B_{Si}) has been identified [1]. On the other hand, a recently proposed model [2] for the deep boron acceptor is at variance with theoretical predictions [5]. To obtain a microscopic picture of the properties of boron in 3C-SiC we have investigated by an *ab initio* method boron related defects and the boron diffusion. Our results show that substitutional boron may react with intrinsic point defects to form deep defect complexes or boron interstitials. Under p-type conditions, boron-carbon-vacancy complexes (B_{Si}-V_C and B_C-V_C) and the tetrahedral carbon coordinated boron interstitial (B_{TC}) occur in comparable concentration as substitutional centers. Similarly we have found that boron pairs form. While the second nearest neighbor pair on the silicon sublattice (B_{Si}-B_{Si}) is only weakly bound, the nearest neighbor pair (B_{Si}-B_C) and the second nearest neighbor pair on the carbon sublattice (B_C-B_C) have a binding energy of about 1 eV. The latter two boron pairs have acceptor levels at 1.0 eV and 0.7 eV, respectively. This indicates that these pairs, besides substitutional boron on the carbon sublattice, may be responsible for the experimentally observed deep acceptor level. Yet, the spin density of the boron pairs cannot explain the EPR-data, that originally has been attributed to the deep acceptor. The electrical activation of boron is determined by three effects: (1) the binding of implanted boron in pairs, the formation of boron-carbon-vacancy complexes and boron interstitials, (2) the compensation of shallow boron by positively charged boron-carbon-vacancy complexes, the boron interstitial B_{TC} or other defects and (3) the out-diffusion of implanted boron during the anneal. According to our findings all these effects are operative. However, the electrical activation rises with the C/Si-ratio as the concentration of shallow boron increases and at the same time the compensation by the boron-related deep centers decreases. Our results indicate that boron migration in p-type material is governed by an interstitial mechanism preceeded by a kick-out reaction with a silicon interstitial. This result supports the findings of recent experiments [6].

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THEORETICAL STUDIES ON VANADIUM IMPURITY IN β-SiC

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The studies of a vanadium impurity in silicon carbide are especially actual, as being an amphoteric impurity and forming deep levels near to the middle of the bandgap it allows to receive a semi-insulating material.

The vanadium impurity atom in silicon carbide crystal lattice can be localized in several structural nonequivalent interstitial (i) or substitutional (Si) positions. Besides in view of differences of atoms radiuses of silicon and vanadium in doped silicon carbide it is necessary to expect the effects of local structural relaxation. Till now the problems of shaping thin features of electronic allocations and nature of interatomic bonds in the system SiC:V in view of the marked circumstances remained practically uninvestigated.

In the present study *ab initio* X_α- discrete variation method (X_α- DVM) calculations of electronic structure and chemical bond parameters has been carried out for the clusters, which simulate possible versions of the isolated vanadium atom impurity intrusion into the β-SiC lattice.

The lattice structural and chemical distortions as a result of vanadium doping has been taken into account within the framework of the tight-binding theory in Harrison's bonding orbitals approach. It was supposed, that the perturbations introduced by the impurity atom, spread not further than next nearest neighbor and, accordingly, the interaction between vanadium impurity atoms was not under consideration.

The following main preliminary results should be marked:

1) for tetrahedrally coordinated substitutional impurity (V_{Si}) there is a considerable split of V3*d*-orbitals by a crystalline field; at C-octahedrally coordinated interstitial position of vanadium (V_i) the impurity states forms an isolated level of V3*d*-states inside the bandgap;

2) the external orbitals of V_{Si} form hybrid bonds with carbon atoms, for V_i the atom orbits overlap of vanadium and proximate silicon atoms is observed,

3) there is the local magnet moment (LMM) on vanadium atom for all of the surveyed positions; the LMM makes ~ (1.4 and 2.0) and (0.0 and 1.1) μ_B for each of two variants V_{Si} and V_i. The results regarding the electronic structure, the formation energies, the ionization levels and the geometry of the relaxed structures of the defects caused by vanadium impurity intrusion into structurally nonequivalent SiC lattice positions will be reported and discussed.

This work was supported by RFBR (project N 01-03-33175).

Evaluation of 6H-SiC(0001) surface after high-temperature hydrogen annealing by reflection high-energy positron diffraction and atomic force microscopy

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1. Introduction

To use SiC as the high performance device materials, it is necessary to make flat, oxide free and inactive surfaces. For this purpose, high-temperature hydrogen annealing is proposed. It is known that damages on SiC surfaces are removed and dangling bonds of SiC surfaces are terminated with atomic hydrogen after hydrogen annealing above 1100 ℃ [Ref.1]. We observed the dependence of 6H-SiC surface morphology on hydrogen annealing temperature using reflect high-energy positron diffraction (RHEPD) and atomic force microscopy (AFM). Using the total reflection mode, RHEPD can convey information about the topmost surface.

2. Experimental and results

Commercial 6H-SiC(0001) specimens were dipped in 5%-HF to remove surface oxides after boiling in acetone, H_2SO_4 and aqua regia to remove the organic substances and metal contaminants. Hydrogen annealing was conducted from 1000 to 1400 °C for 8 hours with H_2 gas pressure and flow rate of 100 Torr and 2 sl/m, respectively. Figures 1 and 2 show the AFM images after H_2 annealing at 1000 °C and 1400 °C, respectively [Ref.2]. In both annealing conditions, flat terraces and step structure are observed. The specimen which was

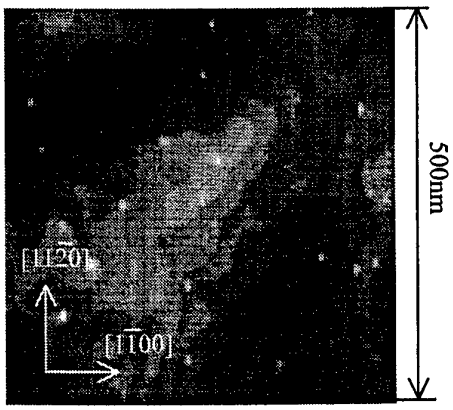


Fig. 1 AFM image for 6H-SiC (0001) after H_2 annealing at 1000 °C for 8 hours.

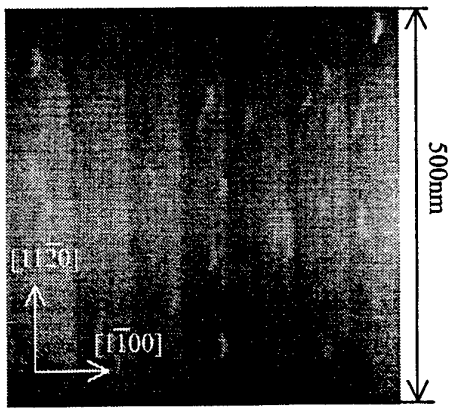


Fig. 2 AFM image for 6H-SiC (0001) after H_2 annealing at 1400 °C for 8 hours.

simply boiled in ultra pure water after dipping in 5%-HF, any terraces were not observed and root mean square roughness (Rq) was several tenths of Å. Thus, terraces appear due to hydrogen annealing. Typical step height between each terrace and Rq in terraces were several Å and less than 1 Å, respectively, after hydrogen annealing at 1000 °C. Nevertheless, the peripheries of terraces are not straight. Much more wider terraces and well-ordered step structure are observed after hydrogen annealing at 1400 °C. The step height between each terrace and Rq of terraces were approximately 1～2 Å, which are comparable to the Si-C bond length (1.87 Å). The step height and Rq are similar to the case of H_2 annealing at 1000 °C.

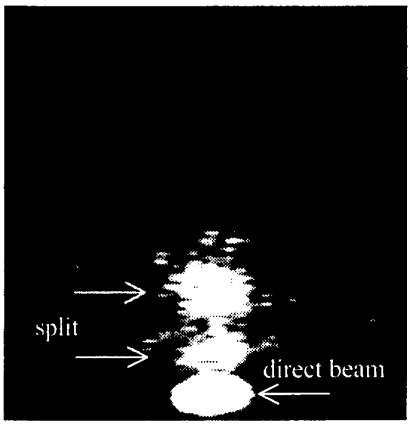


Fig. 3 RHEPD specular pattern for 6H-SiC(0001) after 5%-HF dipping and H_2O boiling.

RHEPD total reflection (at glancing angle of 1.1°) patterns are shown in Figs. 3 through 5 at $[1\bar{1}00]$ incidence. The lowest spot indicates the direct beam. Figure 3 was obtained from the specimen simply boiled in ultra pure water after dipped in 5%-HF. The pattern is heavily splitted. This suggests that the as received 6H-SiC surface was rather rough. From Figs. 4 and 5, it is seen that the specular patterns are spot like. This suggests that H_2 annealing at over 1000 °C make 6H-SiC surface atomically flat. These results are consistent with AFM observations.

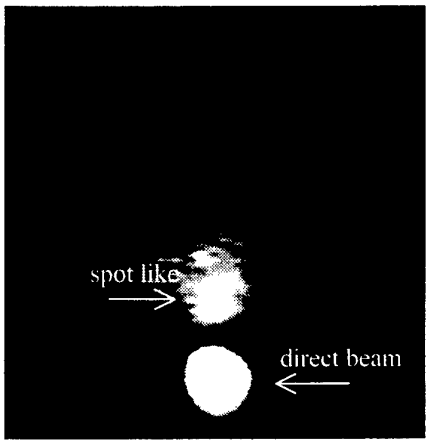


Fig. 4 RHEPD specular pattern for 6H-SiC(0001) after H_2 annealing at 1000 °C for 8 hours.

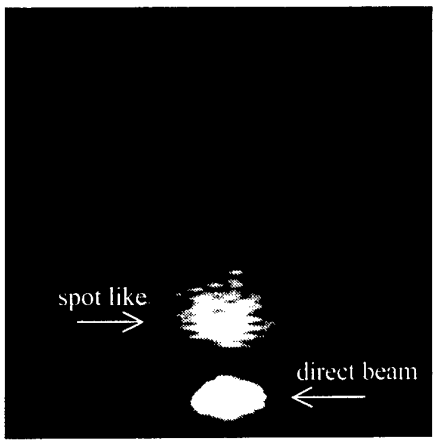


Fig. 5 RHEPD specular pattern for 6H-SiC(0001) after H_2 annealing at 1400 °C for 8 hours.

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Ion-implantation induced deep levels in SiC studied by Isothermal Capacitance Transient Spectroscopy (ICTS)

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Ion implantation is well known as one of the most potential selective doping technology to produce planar SiC devices, applicable for vertical types devices such as MOSFET and JFET. During the implantation, however, generally followed with generation of damage, destroying the crystalline structure of SiC. Although post-implantation annealing can recover the crystallinity, in contrast it causes new-secondary defect. In SiC, 3 types of implantation and successive post-implantation annealing induced defects have been reported [1)]. These defects might work as origin of deep levels, act as trapping or recombination center and greatly limit device performances.

Concerning deep levels associated with these defects, recently, Dalibor et al have overviewed some intrinsic deep defect centers induced by ion-implantation together with the subsequent annealing in several SiC polytypes [2)]. Their results, however, have insufficient clarifications of which process and which region mostly involved with these defects. Moreover, there seem to be a lack for discussion the behaviors of these defects especially for elucidating the defect origins and the information of deep levels in as implanted sample as well as in post-annealed implanted one. In this contribution, we will give valuable data of deep levels related these defects particularly in as implanted 4H-SiC schottky device, their depth profile and the effect of post-implantation annealing, analyzed by isothermal capacitance transient spectroscopy(ICTS) [3)].

In this study we used n-type 4H-SiC(0001) substrate with 8^{o} off-angle and n-type epitaxial layer purchased from CREE. The effective carrier density (Nd-Na) in epitaxial layer was $5x10^{15}$ cm^{-3}. Multiple implantations of N were carried out at room temperature in order to form box-shape profiles with a depth of 0.3 μm. The total dose was $1x\ 10^{13}$ cm^{-2}. The subsequent annealing was carried out in Ar-ambient at 1500°C for 5 minutes. Ni electrodes were formed on SiC back surface by electron beam evaporation and annealed at 1000 C for 2 min, which leads to ohmic contact. To form the Schottky contact Ni was deposited on the ion implanted SiC-surface. The

ICTS measurements were performed in 10^{-2} Torr vacuum, at various temperatures, using sensitive-capacitance measurement apparatus (1MHz) with typical measurement condition of; reverse voltage Vr = -2 V, forward pulse voltage Vp = 1 V, and pulse width Wp = 1 ms.

In as-implanted SiC device, we found three typical deep levels i.e., E1, E2 and E3 with energy levels located at 0.375, 0.76 and 0.86 eV below conduction band, respectively. Since our measurement was limited at temperature range of $\pm 190\,^{\circ}C$, we suggest that deeper energy level might be detectable at higher temperature. Figure 1a and 1b show representative ICTS signals and Arrhenius plot of E1 taken at around ambience temperatures. From the depth profile results, interestingly, E1 and E2 were detected at depth region up to 0.8 μ m from metal/ion-implanted SIC interface. On the other hand, ICTS signal of E3 appeared at deeper position. Two suggestions might be applicable here; one is that E1 and E2 are probably of deep levels associated with ion-implantation induced defects, where the densities decrease toward to deeper position. Second is that E3 may be due to a defect originally existing in the epitaxial layer, but as the defect concentration is much less than that of E1 an E2, it was undetectable at shallower region. Although further investigation to clarify the origin of these defect is required, these results prove that ICTS method is powerful for characterization such kind of these defects.

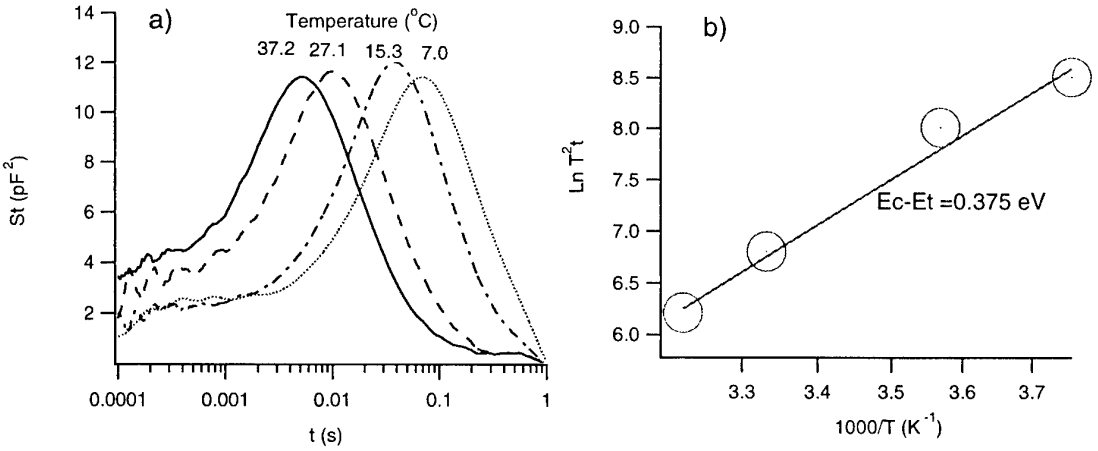


Fig.1 ICTS signals in as-implanted SiC schottky device (a) and Arrhenius plot of corresponding data (b) determined at around room temperature. This is identified as E1 with energy level located at 0.375 eV below the conduction band.

This work was performed under the management of FED as a part of the MITI NSS Program (R&D Ultra-Low-Loss Power Device Technologies) supported by NEDO, Japan.

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Wafer-scale Defect Characterization of SiC Wafers Based on an Optical Technique

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Recent investigations have shown the large potential of SiC for high-power, high-temperature and high frequency electronics. Different wafer types (6H and 4H) grown by the modified Lely method are available at relatively low prices. However, silicon carbide wafers are far from being free of micropipes and other structure defects, which are deleterious to high quality epilayer growth for SiC device applications.

Characterization of structural and crystallographic defects in SiC single crystals is mainly established by X-ray topography, SEM/TEM, AFM, and etching methods. These methods are time-consuming, expensive, and sometimes destructive due to the necessary special techniques for sample preparation. Moreover, the most commonly used etching methods for defect delineation are destructive. It is very difficult to realize wafer-scale defect characterization of SiC wafers using the above methods. Therefore, it is essential to develop an economic, rapid, and nondestructive characterization technique for SiC wafer-scale evaluation of structural and crystallographic defects.

In this work, an optical technique has been developed successfully to characterize the structural and crystallographic defects in SiC wafers. A rapid, nondestructive and low-cost visualization technique is demonstrated. The technique allows revealing of micro- and nano-pipes as well as dislocations in basal-cut hexagonal SiC wafers. A comparison between the results from this technique and X-ray topography, AFM, and KOH etching is also presented.

Figure 1 shows typical dislocation distribution of a 6H-SiC wafer. The presented surface area is about 0.7×0.7 mm^2.

This technique offers a method of observation of macro defects, such as micropipes on a wafer-scale, but also enables us to study micro scale defects, such as dislocations, and thus offers a wide range of possibility for material characterization in a completely non-destructive manner. It is especially effective for investigations of defect distribution and density influence on the device performance.



Figure 1. Dislocation distribution in 6H-SiC wafer

Luminescence and Electron Paramagnetic Resonance in AlN Layers Implanted with Er and O Ions

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The interest in the study of the luminescence of Er ions in semiconductors is due to the prospects of employing them in optoelectronics. To obtain a better understanding of the defect-formation processes and the luminescence of Er^{3+} ions, various semiconductors have been investigated. According to the results, the thermal quenching of the photoluminescence (PL) intensity of Er ions decreases significantly as the gap width of the semiconductor increases. For example, in Si:Er the PL intensity of Er ions decreases by several orders of magnitude as the measurement temperature is raised from 77 K to 300 K [1], whereas in GaN:Er a severalfold decrease in the intensity is observed [2]. The purpose of the present work was to study the optical and magnetic properties of Er-doped aluminum nitride layers.

Erbium ions with an energy E = 1 MeV and dose D = $5x10^{14}$ cm^{-2} and oxygen ions with E = 0.115 MeV and D = $5x10^{15}$ cm^{-2} were implanted at room temperature. The implanted samples were annealed in a furnace for rapid thermal annealing at 1300^0C during 30 s in a stream of nitrogen. The PL was excited by the emission of a halogen lamp and recorded by means of a monochromator with 3-nm resolution and an InGaAs photodetector operating at room temperature. The magnetic resonance was measured by an ER-220D electron paramagnetic resonance spectrometer in 3 cm range at temperature from 3.5 K to 120 K.

Figure 1 shows the PL spectra, measured at 80 K and 300 K, for a AlN:Er sample. In addition to the emission peak with a maximum at the wavelength λ = 1.536 μm due to transitions of Er^{3+} ions from the first excited state $^4I_{13/2}$ to the ground level $^4I_{15/2}$, the spectra also contain a series of small peaks in the vicinity of $\lambda \approx 1$ μm, which can be attributed to the ion transitions from the second excxited state $^4I_{11/2}$ to the ground state, and a broad luminescence band in the interval $\lambda \sim$ 1.02-1.12 μm. The Er-related PL intensity at λ = 1.536 μm increases by a factor of 2 when the measurement temperature is lowered from 300 K to 80 K. The broad emission band is associated with the PL of defects in AlN, since the PL intensity increases after additional implantation of oxygen ions. The Er-related PL intensity at λ = 1.536 μm in AlN:Er is higher than that in AlN:(Er,O) by several orders of magnitude.

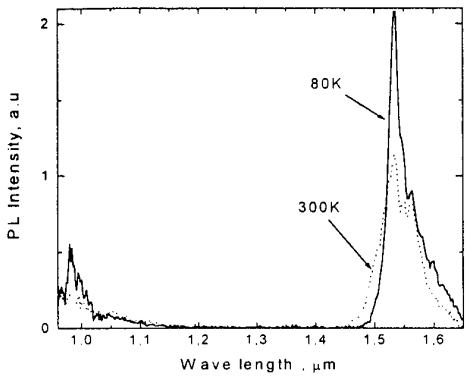


Fig. 1. PL spectra of AlN:Er sample. Spectra were measured at 80 K and 300 K.

The magnetic resonance signals in AlN:Er and AlN:(Er,O) are observed from 60 K to 110K and from 4.1 K to 110 K, respectively. A spectrum contains one isotropic line with parameters strongly dependent on temperature (Fig. 2). The inversion of magnetic field is not followed by the reproducibility of position and intensity of the line in the AlN:(Er,O) sample. Observation of magnetic resonance at high temperatures shows the magnetic centers have zero orbital momentum. We believe that the centers are formed by lattice intrinsic point defects. Temperature dependence of resonance signal parameters can be explained by changes of the internal magnetic field. This field can appear due to exchange interaction between erbium atoms, without exchange interaction with other defects. So, magnetic resonance studies show the presence of lattice defects surrounding the magnetically ordered clusters of erbium ions.

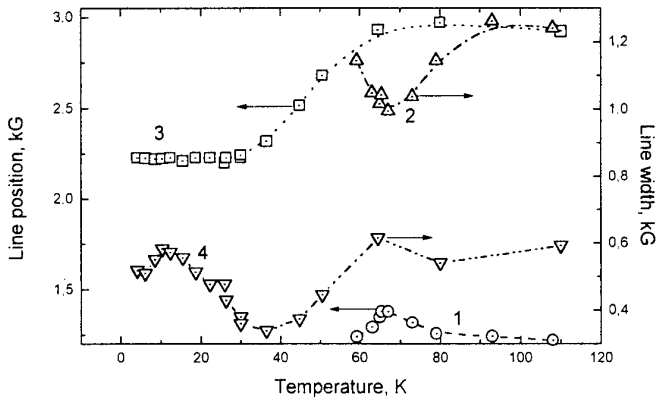


Fig. 2. Temperature dependencies of the line position (1,3) and line width (2,4) for AlN:Er (1,2) and AlN:(Er,O) (3,4) samples.

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Electrical characterization of SiC/Si heterostructures with modified interfaces

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The problems to grow 3C-Bulk crystals has retained over the years the interest to the thin film heteroepitaxy on silicon substrates. Beneath the fundamental question of the heteroepitaxial growth in a material system with large lattice mismatch, the SiC - Si system has certain attractive applications. The first is in the field of robust sensors operating at high temperatures and harsh environments. The second is in the field of substrates for the nitride epitaxy. The common technique to grow SiC on Si is a two step process consisting of a carbonization process followed by epitaxial growth. The grown layers suffer from the high lattice and thermal lattice mismatch between these two materials leading to high residual stresses and lattice defect densities in the grown silicon carbide layer and the heterojunction. The properties oft the SiC layer can be improved by using one of the following substrate modification methods: (1) silicon on insulator, (2) porous silicon, (3) modification of the silicon substrate with group IV elements. Only the last method is applicable if the electrical properties of the heterojunction are of interest.

To have an insight in the influence of the surface preparation techniques on the properties of the SiC/Si system the following methods of creating a SiC pseudosubstrate were used: (1) conversion of Si(111) into SiC(111) by RTCVD using propane diluted in hydrogen, (2) conversion of Si(111) into SiC(111) by solid source molecular beam epitaxy, i.e. in a hydrogen poor environment, (3) conversion of Si(111) modified by Ge predeposition into SiC(111) by SSMBE. On these substrates 3C-SiC epitaxial layers were grown at 1000°C with a growth rate of 1nm/min. The growth were carried out at Si rich conditions and continuously operating Si and C sources. The stability of the growth conditions were controlled by using the (3×3)-Si (111)SiC surface reconstruction. The growth process was monitored by *in situ* reflection high energy electron diffraction and *in situ* spectroscopic ellipsometry in real time. The films were investigated *ex situ* by atomic force microscopy, X-ray diffraction,. For electrical characterization heterodiodes were prepared.

The results obtained show that the epitaxial layers are characterized by a single domain 3C-SiC structure.The layers grown on RTCVD carbonized material shown a carbon face where as the layers grown on MBE carbonized material exihibit a silicon face [1]. In dependence on the polarity of the deposited layers different built in voltages were observed indicating on a band offset in dependence on the SiC polarity on Si. For both cases it was observed that Ge predeposition lead to an improved electrical properties of the formed heterojunction. This was obtained for the forward direction were the ideality factor was improved from 1.8 to 1.3 as well as for the reverse direction were the reverse currents which decreases with increasing Ge coverage. The obtained current-voltage and capacity-voltage charcteristics were analysed in terms of interface state densities and band offsets. Detailed band diagrams in dependence on the interface modification method will be presented.

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Carrier concentrations in implanted and epitaxial 4H-SiC by Scanning Spreading Resistance Microscopy

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Developments in process technology and electrical characteristics of silicon carbide based devices require precise knowledge of the charge carrier distribution in the material. Especially, the activation of implanted species in SiC is crucial for device performance, but can not be determined using the standard dopant profiling techniques of today. Attempts have been made to measure p-type aluminum and boron implantation profiles in 4H-SiC by spreading resistance profiling (SRP), but the hardness and electrical barrier between the probe and sample were found to limit the dynamic range and prevent contact formation for low carrier concentrations [1, 2]. Other types of dopant profiling techniques have also been investigated, none of which have been able to provide sufficiently reproducible and, in particular, quantifiable data [2].

In contrast to the results from conventional SRP however, we report here of the successful application of a novel spreading resistance method for wide range and high gradient free carrier concentration measurements in SiC, namely scanning spreading resistance microscopy (SSRM). SSRM is a recently developed scanning probe microscopy (SPM) based technique, using an atomic force microscope (AFM). It has previously been applied for dopant profiling/imaging in Si [3] as well as three-five materials such as InP [4].

The SSRM set-up consists of a Digital Instruments Dimension 3100 AFM system with a commercially available SSRM add-on module equipped with logarithmic current amplification, which utilizes boron doped diamond coated tips. The arrangement enables penetration of the native oxide by high forces and provides continuous (or single-step) one or two dimensional SR measurements, with spatial resolution of about 30 nm and a dynamic range of up to seven orders of magnitude, typically 10^{14} to 10^{21} cm^{-3} [5].

An example demonstrating the wide dynamic range is depicted in Figure 1 (a), which shows the averaged SSRM current across an Al-doped epitaxial stair-case structure of 4H-SiC together with the corresponding secondary ion mass spectrometry (SIMS) data in (b). The step-heights are in very good agreement with SIMS, except at the highest peak, which may be attributed to the reduced activation and/or mobility observed for Al concentrations > 10^{20} cm^{-3} [6]. It should also be mentioned that conventional SRP measurements of the same structure had difficulties to detect concentrations already below the maximum peak at $2x10^{20}$ cm^{-3}. In Figure 2 (a) the combination of SSRM and SIMS data has been used to produce a calibration curve, which for the specific tip it is calibrated for, enables quantification of e.g. implantation profiles. As an example, we employ the calibration curve to evaluate an Al and B implantation profile of 4H-SiC in Figure 2 (b) and (c), measured after 10 min annealing at 1700 °C. The SSRM data reveals a much higher resistance in the highly Al doped region than suggested by the chemical concentration of > 10^{20} cm^{-3}. The measured current in this region corresponds in fact to the resistance found at a concentration as low as about 10^{18} cm^{-3} in the epi layer calibration curve. The observation may be explained by the presence of remaining implantation induced defects in the material, even after annealing. Furthermore, the long diffusion tail of B into the material can be detected also electrically by this method, until the concentration reaches the level of the background n-type epi layer doping ($2x10^{15}$ cm^{-3}) at about 3μm depth.

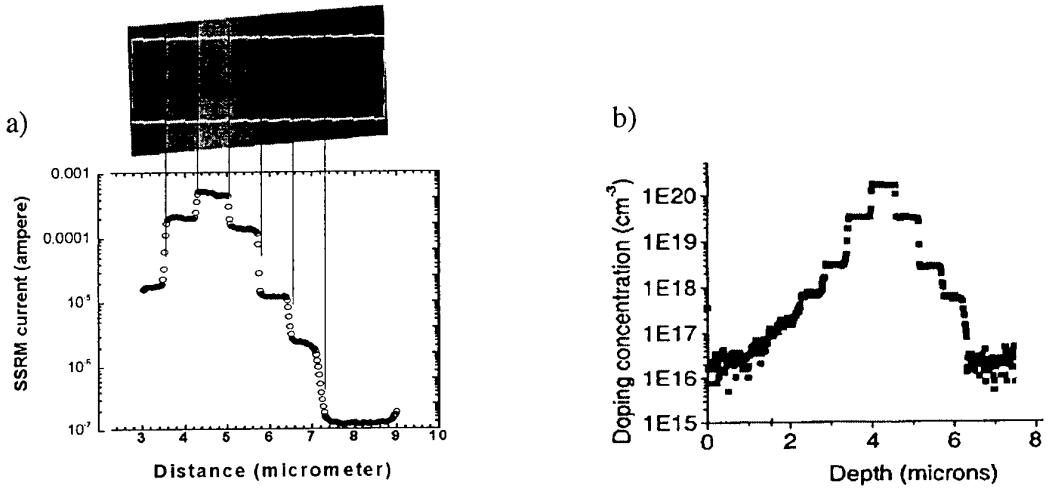


Fig 1. (a) SSRM and (b) SIMS depth profiles of an Al doped epi layer of 4H-SiC. The SSRM signal represents the average of multiple scans (> 50) selected from a surface region free from topographical gradients, which is marked by white lines in the two-dimensional SSRM image shown as inset above (a).

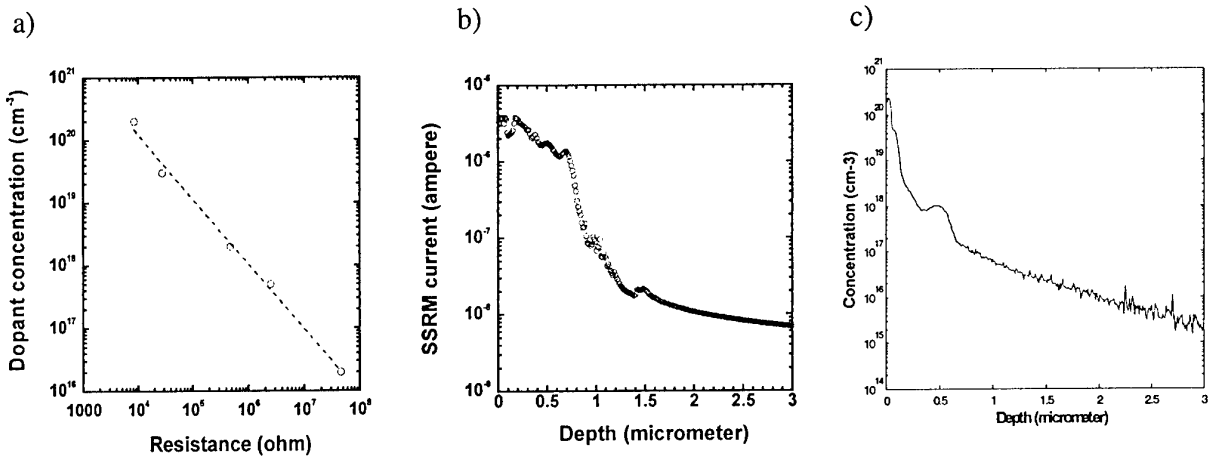


Figure 2. a) Calibration curve for extraction of carrier concentration from measured resistance. The data is tip-specific for each diamond coated SSRM tip. b) SSRM line scan of an Al and B implantation profile using the same tip as in a) at a bias voltage of 5V. c) SIMS measurements the same implantation, for comparison plotted as the sum of both Al and B.

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Thermoelectric properties of β-SiC produced by silicon carbonization

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Introduction

Silicon carbide (SiC) is a wide-band-gap semiconductor with high chemical stability at high temperatures. Therefore, SiC may be an excellent candidate of the materials for devices which can operate at high-temperature, -frequency or -power conditions. However, it is generally considered that SiC is unsuitable for thermoelectric applications due to its rather high thermal conductivity. This is because the thermoelectric figure of merit Z retains lower values for materials with a higher thermal conductivity. Here, Z is defined by the equation, $Z=\alpha^2\sigma/\kappa$, where α, σ, and κ are the Seebeck coefficient, the electric conductivity, and the thermal conductivity, respectively. To get a large Z value it is required to increase both α and σ, and to decrease κ, simultaneously. We tried to fulfill these requirements by adopting a novel synthesizing method for SiC, in which β-SiC is fabricated by the carbonization of commercial Si wafers doped with different concentrations of impurities.

Experimental Procedure

We used 0.5 mm thick Si-wafers as a silicon source, and graphite powders of 99.98 % purity as a carbon source. The wafers were put into a carbon case filled with graphite powders. The case was evacuated in a chamber down to 1×10^{-3} Pa at 600 ℃, and subsequently the chamber was filled with Ar gas of 1 atm. The carbonization of Si-wafers was carried out at 1300 ℃ for 24 hours. During this process, the surfaces of the wafers were carbonized, and SiC layers were formed. The crystal structure and composition of these samples were studied by X-ray diffraction (XRD) and electron probe microanalysis (EPMA). The microstructures were characterized by using transmission electron microscopy (TEM) and field emission scanning electron microscopy (FE-SEM). The thermoelectric properties of the samples were evaluated by measuring the DC conductivity and the Seebeck coefficient at elevated temperatures (R.T.~1000 ℃).

Experimental Results

Structure and composition

The XRD patterns of the carbonized samples showed the formation of β-SiC on the surfaces of the wafers. The cross sectional SEM observation revealed that the thickness of the SiC layer was about 55 μm beneath the original surfaces of the wafer. (Fig. 1)

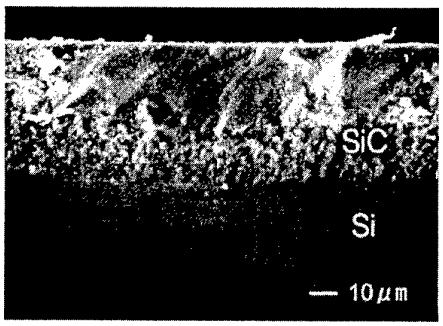


Fig.1 Cross section SEM micrograph of sample

Since the relative density of the β-SiC layer was approximately 60 %, it is expected that the present carbonization process has a role to make the SiC layer porous. The size of SiC crystallites and pores was estimated to be about 10~50 nm and 10~100 nm, respectively, by TEM observations. In addition, HR-TEM indicated the presence of grain boundary amorphous layers. The composition of the β-SiC layer analyzed by EPMA was C-rich (Si/C ≃ 0.8) and the amount of oxygen was rather high. The excess Si and oxygen are assumed to be due to the presence of

the grain boundary amorphous phase (SiO_2), since the XRD pattern of the β-SiC phase showed no apparent peak shifts.

Electrical Properties

It is interesting to see the effects of impurities, already doped in the Si-wafers, on the electrical conductivity of the SiC prepared by the carbonization process. Figure 2 shows the Arrhenius plots of σ for two different samples. The sample formed from the high-doped wafer indicates higher conductivity values of the order of 10^4~10^5 $\Omega^{-1}m^{-1}$, whereas that formed from the low-doped wafer has low conductivity values ranging 10^2~10^3 $\Omega^{-1}m^{-1}$. With increasing temperature up to 600~1000 ℃, however, the conductivity of these samples came to similar values which can be fitted to a straight line.

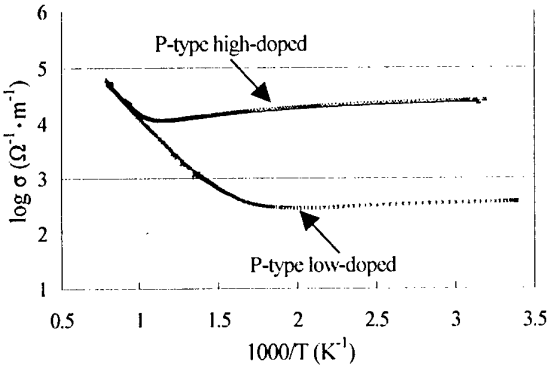


Fig.2 Arrhenius plots of electrical conductivity for samples.

The temperature dependence of the Seebeck coefficient for the SiC samples is shown in Fig.3. The sign of α depended on the conduction type of the wafer used. A negative sign was observed for the samples prepared from the n-type wafers, and a positive sign was found for those prepared from the p-type wafers, though the sign changed to negative at high temperatures > 850 ℃. It is also found that the samples formed from the high-doped wafers gave very high values of the Seebeck coefficient ≃ 600 μ V/K at a temperature range 400~500 ℃.

An example of the power factor P ($=\alpha^2\sigma$) for the SiC sample is given in Fig.4. It is clear that β-SiC obtained by the present carbonization process exhibits very large power factor values greater than 10^{-3} W/mK^2 at 300~600 ℃, which is quite attractive from a practical view point of thermoelectrical applications.

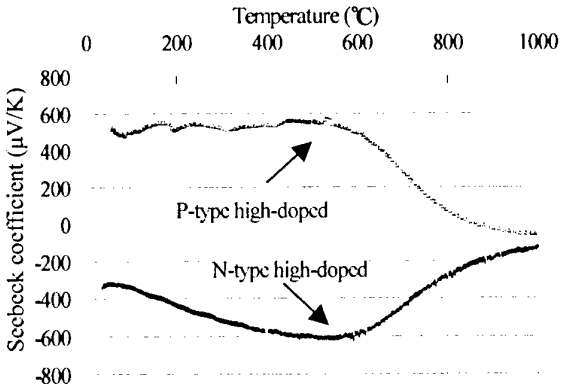


Fig.3 Temperature dependence of Seebeck coefficient.

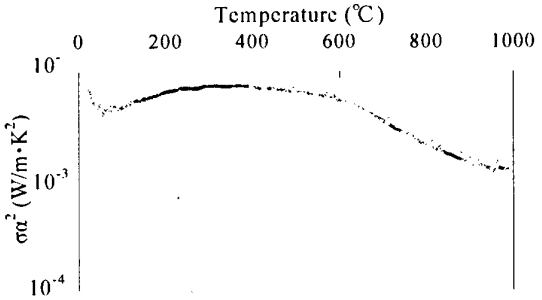


Fig.4 Temperature dependence of power factor.

Conclusions

We successfully produced porous β-SiC on Si-wafers by a silicon carbonization process. The results of thermoelectric characterizations showed that the SiC samples prepared from the high-doped wafer have high electrical conductivities and high Seebeck coefficients, which may be suitable for high temperature thermoelectric applications. It could also be expected that the thermal conductivity of the SiC samples must be reduced extremely because of its porous structure.

Distribution profile of deep levels in SiC observed by isothermal capacitance transient spectroscopy

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Silicon carbide (SiC) has been attracting much attention as a material for high-power, high-frequency, and high-temperature devices. To realize the SiC devices, it is quite important to obtain information about deep levels in SiC, since deep levels in semiconductors, which are due to impurities or point defects, can be trapping or recombination centers and influence device performance. Attempts to evaluate deep levels in SiC have been done and several deep levels have been found in SiC.[1)] In the present work, we have tried to observe the distribution of deep levels in SiC by use of isothermal capacitance transient spectroscopy (ICTS).[2)]

Samples used were n-type 4H-SiC (0001) substrate with effective carrier density (N_d-N_a) of 2.6×10^{17} having 8° off-angle purchased from CREE. A part of the substrate was cut into 12×12 mm squares, and a 4H-SiC epitaxial layer was deposited on the Si face of the substrate by the low-pressure, hot wall type, horizontal chemical vapor deposition method. The epitaxial layer was n-type with effective carrier density of 2×10^{15} cm^{-3}. Nickel Schottky contact and Mg ohmic contact were formed on the Si face and on the C face of the samples, respectively. The ICTS measurements were performed in 10^{-2} Torr vacuum at the temperature range from 80 to 470 K. The applied forward pulse voltage and the pulse width were 1 V and 10 ms, respectively. Depth profiles of the deep levels were obtained by changing the applied reverse voltage.

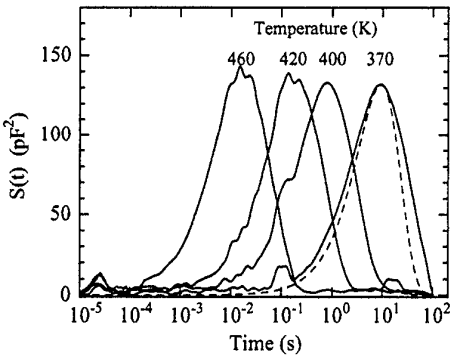


Fig. 1. ICTS spectra observed in the substrate sample at the temperature range from 370 to 460K.

Figure 1 shows the ICTS spectra observed in the substrate sample. The energy level of the deep level showing the ICTS signal was calculated to be *E*c-0.94 eV from the shift of the peak with temperature, where *E*c indicates the energy level of the

conduction band. Figure 2 shows the depth profile of the concentration of the deep level from the sample surface. This result indicates that the deep level was uniformly distributed in the substrate.

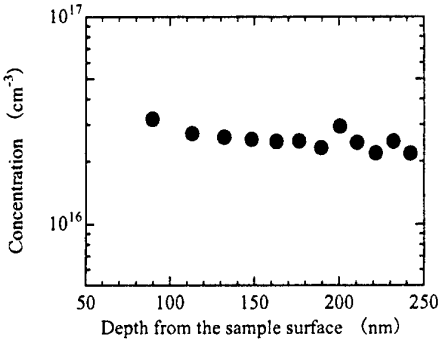


Fig. 2. Depth profile of the concentration of the deep level observed in the substrate sample.

Figure 3 shows the ICTS spectrum observed in the epitaxial layer at 290 K. The calculated energy level of the deep level was *E*c-0.6 eV. This deep level is considered to be due to the Z_1 center reported in Ref. 1. The distribution of the Z_1 center in the sample is shown in Fig. 4. The concentration of the Z_1 center in the epitaxial layer close to the substrate is in the order of 10^{14} cm^{-3}, while it is about 1×10^{13} cm^{-3} at the sample surface. This result indicates that the Z_1 center was mainly introduced at the initial phase of the epitaxial growth.

The Z_1 center is not always observed in the epitaxial layers grown by the CVD apparatus. It has been observed that there in no correlation between the generation of Z_1 center and bulk substrate conditions. These facts indicate that the introduction of Z_1 center strongly depends on the epitaxial conditions.

This work was performed under the management of FED as a pert of the METI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

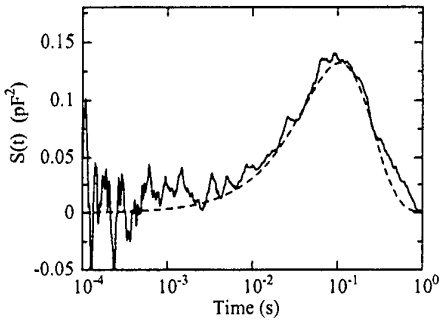


Fig. 3. ICTS spectrum observed in the epitaxial layer at 290 K.

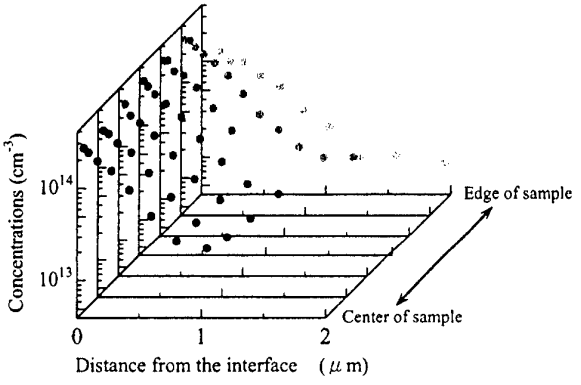


Fig. 4. Distribution of the Z_1 center in the epitaxial layer.

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Oxidation of porous 4H-SiC substrates

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Porous silicon carbide (por-SiC) has been investigated recently because of its potentially attractive properties for light emitting diodes[1], efficient photodetectors[2], and as templates for nano-structure epitaxial nucleation, and surface layer modification. Commonly, in device technology, the silicon dioxide formation plays a significant role. Moreover, the oxidation of a porous surface might modify the morphology of the surface that would result in changing of the optical and electrical characteristics of the modified surface. For these reasons, it is necessary to understand the kinetics of the oxide growth on a por-SiC substrate.

In this research we have been studying the influence of SiC crystal orientation (carbon vs. silicon terminated faces) on the kinetics of porous 4H-SiC substrate oxidation.

Anodization of n-4H-SiC samples purchased from CREE Research and Bandgap Technologies was carried out in dark mode at current densities from 10 to 60 mA/cm^2 in 2.5% HF solution for 2-10 min. After RCA cleaning, oxidation of the porous samples was performed in wet oxygen at 1000°C for 60-180 min.

Thecknesses of the grown oxide layers both on the porous and non-porous regions were measured by Dektak profilometer and by Rudolph ellipsometer as well. Also, the steps between porous and non-porous regions before and after the oxide removal were measured on each face to obtain data about the oxide propagation into por-SiC. Surface morphology of porous silicon and carbon faces before and after oxidation was analyzed by means of AFM.

It was found that the interface between the oxide layer and a porous substrate is always below that for non-porous substrate in both Si- and C-faces. However, the oxidation rate of porous substrate on the both faces is less than the plain carbon face but higher than the plain silicon face. This difference in the oxidation rates results in a thicker oxide layer grown on a non-porous C-face than on porous carbon and silicon faces, and thinner oxide layer grown on a non-porous Si-face than on porous carbon and silicon faces. The kinetics of oxidation of the porous layer is discussed in detail in this presentation.

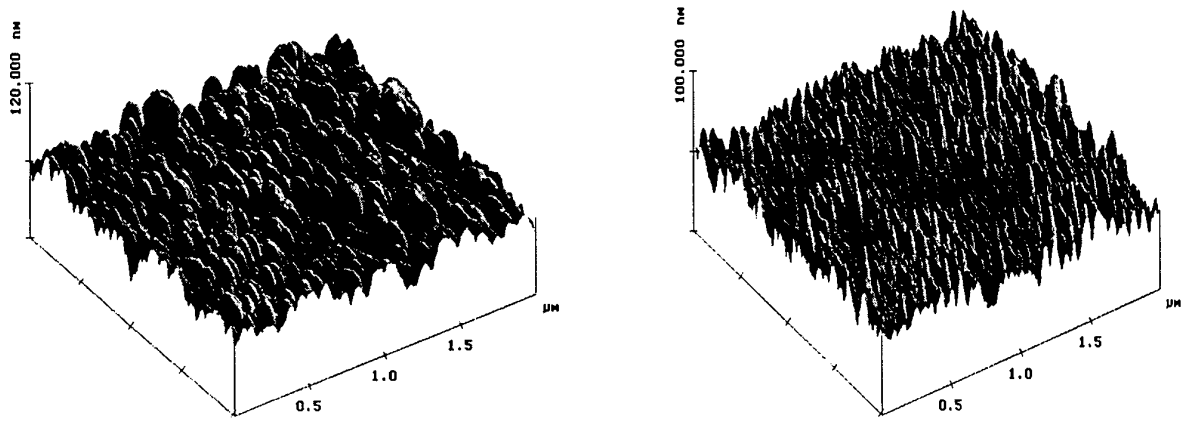
The AFM images shown in Fig.1 have been taken from porous C-face before oxidation (Fig.1a) and after oxidation and subsequent removal of the oxide layer (Fig.1b). It is seen clearly that after oxidation of the porous c-face the surface peaks become more sharp. This surface modification will be discussed in terms of the anisotropy character of the silicon carbide oxidation.

Acknowledgments

The authors are grateful to Dr. X. Ma for AFM measurements.

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a) b)

Fig.1. AFM images of (a) porous C-face before oxidation and (b) after oxidation and subsequent oxide removal.

Plasma Oxidation of SiC at Low Temperature below 300 °C

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The thermal oxidation of SiC is of important for the fabrication of metal-oxide-semiconductor structure and the insulating layer on SiC devices. The growth rate of SiO_2 layer on SiC due to the thermal oxidation is much slower than that of Si even at temperature of 1150 °C. On the other hand, it has been reported that Si can be oxidized by the plasma oxidation at extremely low temperature as low as 400 °C[1]. It is expected also that the plasma oxidation of SiC is useful to form the SiO_2 layer on SiC at low temperature. In this study, we report the plasma oxidation of SiC at temperature below 300 °C.

Samples used in this study were (0001)-oriented n-type 6H-SiC epitaxial layer (net donor concentration: 1×10^{16} cm^{-3}) grown on n-type substrate, which were provided from Cree Research. Figure 1 schematically illustrates a microwave-equipment used in this study, in which the introduced gas is discharged by microwave from 2.45 GHz magnetron at a power of 500 W. After a sacrificial oxidation and HF treatment of sample, the O_2-plasma oxidation was carried out with a O_2 flow of 0.4 sccm and Ar flow of 5.6 sccm at a pressure of 100 mTorr. In order to estimate the temperature dependence of oxidation rate, the temperature of samples were ranged from 100 to 300 °C. The composition of the growth layer was evaluated by using X-ray photoemission electron spectroscopy (XPS) with Mg Kα X-ray. The thickness of grown layer was evaluated by means of elipsometry.

Figure 2 shows XPS spectra of Si2*p*, C1*s*, and O1*s* electrons taken from the Si-face sample, which was processed for 20 min at the temperature of 200 °C. The binding energies of Si 2*p* and O 1*s* in the growth layer were evaluated to be 103 and 532 eV, respectively. The obtained binding energies of Si 2*p* and O 1*s* in the grown layer are identical to those of the thermally oxidized layer of SiC. It is concluded that the growth of SiO_2 layer on SiC can be achieved by O_2 plasma processing at 200 °C. Also, it should be noted that there are no singles attributed to C atoms in the plasma-grown SiO_2 layer. At the surface, the binding energies of Si and O may be influenced by C contaminations. At the interface, the binding energies of Si 2*p* and C 1*s* are lower than those in SiC. Since the binding energies of Si 2*p* and C 1*s* correspond to those of Si crystal and graphite, respectively, it is suggested that the dissociation of SiC at the interface between SiO_2 and SiC is caused during the plasma oxidation.

Figure 3 shows the oxide thickness as function of the oxidation time. The oxidation rate for the dry thermal oxidation at 1150 °C for Si-face of 6H-SiC is also shown. For the Si-face sample, SiO_2 layer with a thickness of 74 nm was obtained after the plasma oxidation for 20 min, while that for the thermal oxidation was evaluated to be 2 nm for Si-face of 6H-SiC. Furthermore, the oxide thickness for C-face is thicker than that of the case of Si-face. The larger oxidation rate of C face than Si-face in O_2 plasma oxidation is similar to the case of the thermal oxidation of (0001)-oriented SiC. The oxidation time dependences of the oxide thickness for Si- and C-face show the slope of 1.5 and 0.72 below 30 min and 0.4 and 0.2 above 30 min, respectively, while the slope of thermal oxidation is estimated to be 1.0. For the plasma oxidation of C-face SiC sample, the obtained slopes are in good agreement with

those in the case of Si. The initial growth with a slope of 0.72 is connected to both Si-SiO_2 interface reaction controlled and diffusion controlled in the SiO_2 layer, while the growth with a slope of 0.2 has been correlated to the Cabrera-Mott model [1]. The plasma oxidation of Si-face SiC sample shows 2 times larger slopes than the case of C-face. It is suggested that the unknown phenomena are involved in the plasma oxidation of Si-face. The activation energy of the plasma oxidation of 6H-SiC was estimated to be about 0.04 eV for both Si- and C-face in the temperature range from 100 to 300 °C. The low activation energy indicates that the plasma oxidation is dominantly activated by O_2 plasma processing of SiC.

In summary, the low-temperature oxide growth on 6H-SiC was observed at extremely low temperature of 200 °C with the much faster growth rate, as compared to the case of the thermal oxidation at 1150 °C, which is useful to the rapid oxidation of SiC at low temperature.

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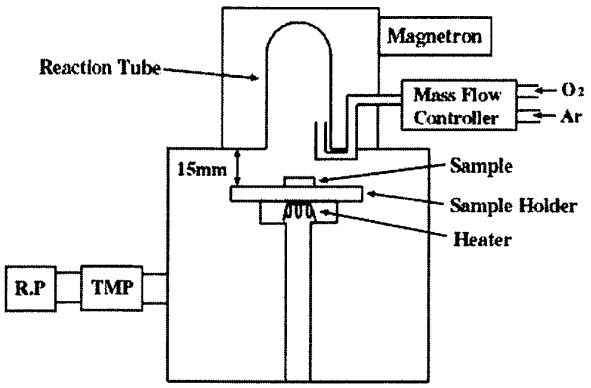


Fig. 1

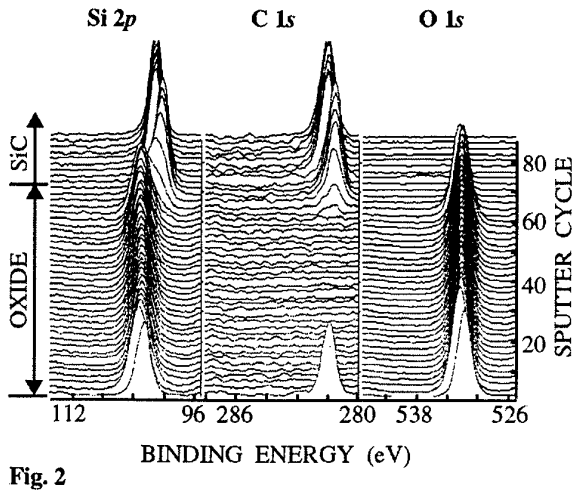


Fig. 2

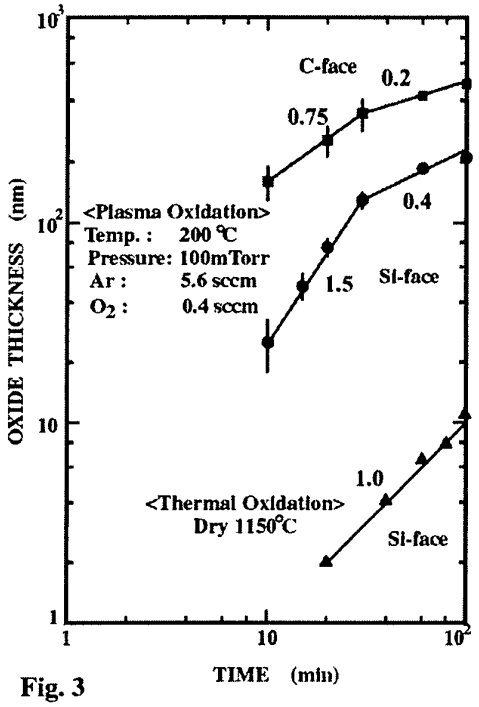


Fig. 3

4H-SiC ACCUEFT with stacked gate oxide consisting of two layers

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Channel mobility in 4H-SiC MOSFETs is rather low regardless of the high bulk mobility. One cause of low channel mobility is attributed to the capturing of carrier electrons by the many interface traps that are present in 4H-SiC MOS structures [1]. This paper describes an effective way to reduce interface state density, *Dit*, using a stacked gate oxide having two layers. Improved channel mobility has been achieved with this stacked gate oxide.

Figure 1 shows a dependence of *Dit* on the thickness of thermally grown oxide. The *Dit* distribution as a function of energy from the conduction band was measured with the high-low CV method. A 4H-SiC (0001) n-type epi-wafer ($Nd = 3\times10^{16}\,cm^{-3}$) was used and the thermal oxide was grown at 1100 ℃. It is seen that *Dit* in the SiO_2/4H-SiC interface increased as the thermal oxide became thicker. Figure 2 shows a comparison of *Dit* between samples using either the thermal oxide or the stacked gate oxide. The stacked gate oxide was created in a three-step process. First, a high quality thermally grown oxide was formed to a thickness of about 20 nm. Then an additional 30 nm of non-doped silicate glass (NSG) was deposited by CVD. The stacked oxide was then annealed at 1000℃ for 30 minutes in a H_2 or N_2 atmosphere. The highest *Dit* value was observed near the conduction band edge of the sample with the 50-nm-thick thermal oxide. N_2 annealing was more effective for reducing *Dit* of the stacked oxide than H_2 annealing and the lowest *Dit* value was obtained from the stacked oxide that was N_2 annealed at 1000 ℃ for 30 minutes.

Planar 4H-SiC accumulation-mode MOSFETs (ACCUFET) with a thermally grown oxide or a stacked oxide were fabricated on p-type epi-layers ($Na = 3\times10^{16}\,cm^{-3}$) grown on n-type (0001) Si-face substrates. Figure 3 shows a cross sectional view of the ACCUFET. The channel length and width were 3 and 100 μm, respectively. Source and drain regions were formed by phosphorous ion implantation and nitrogen was implanted in the channel region at 800 ℃ with a total dose of $2.2\times10^{12}\ cm^{-2}$. The regions were activated at 1600 ℃ for 20 minutes in Ar. The thermally grown oxide was formed at 1100 ℃ to a thickness of 50 nm. The stacked gate oxide consisted of a 20-nm-thick thermal oxide and 30-nm-thick NSG. The sample with the stacked oxide was then annealed at 1000 ℃ for 30 minutes in N_2. The ohmic contacts for the source and drain were Ti/Al and the gate electrode was poly-Si.

Figure 4 shows the $I_D - V_D$ characteristics of the ACCUFET with the stacked gate oxide. The accumulation layer channel mobilities (μ_{FE}) of the samples were calculated with Eq. (1) and plotted with the gate voltage in Figure 5.

$$\mu_{FE} = Gm \cdot Lg/(W \cdot Cox \cdot Vd) \quad at\ Vd = 0.1\ V \qquad (1)$$

Higher channel mobility of 35 cm^2/Vs was obtained using the stacked gate oxide compared with 21cm^2/Vs for the thermal oxide only. *Vth* of the stacked oxide ACCUFET was 0.3 V, while that of the thermal oxide ACCUFET was 1.0 V. This indicates that more negative charges existed in the MOS structure with the thermal oxide only than with the stacked oxide. These negative charges may have been electrons captured by acceptor-like interface traps. Since 4H-SiC ACCUFETs with a stacked gate oxide have lower density of electron traps, they can achieve higher channel mobility than ACCUFETs with a thermal oxide only.

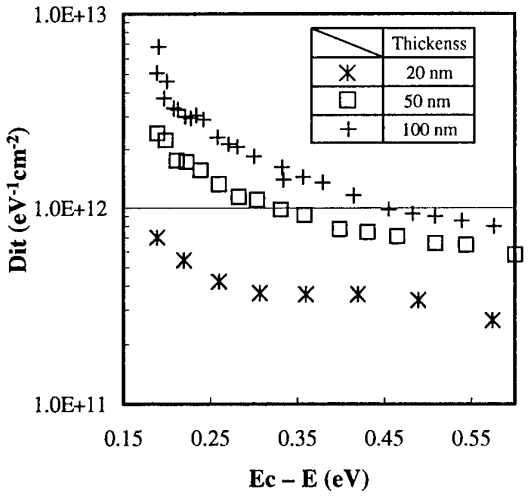


Fig. 1. Dependence of Dit on the thickness of thermally grown oxide

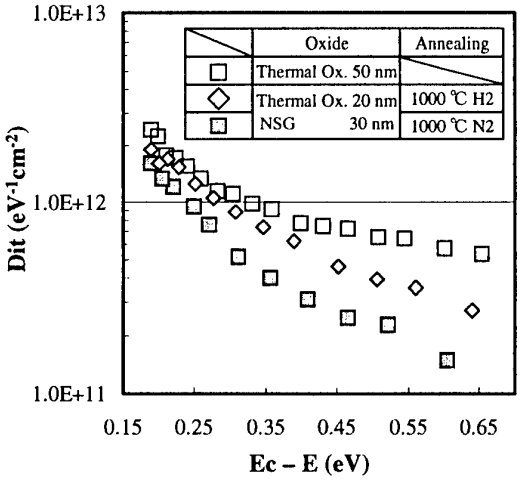


Fig. 2. Dit for samples with thermally grown oxide or stacked gate oxide

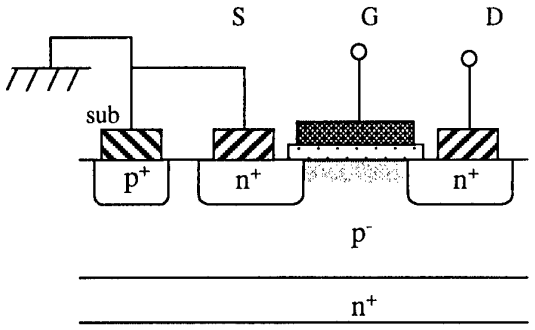


Fig. 3. Cross section of 4H-SiC ACCUFET

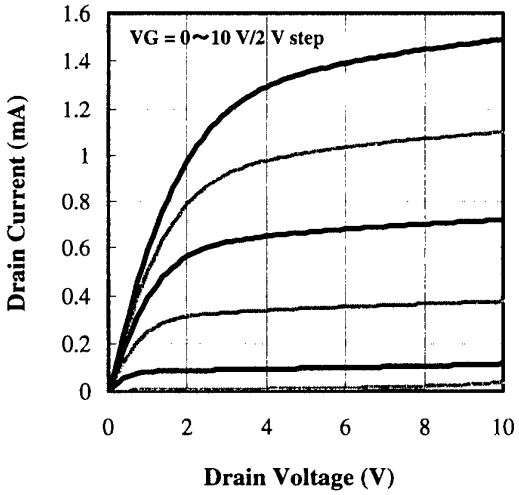


Fig. 4. I_D-V_D characteristics of 4H-SiC ACCUFET with stacked gate oxide

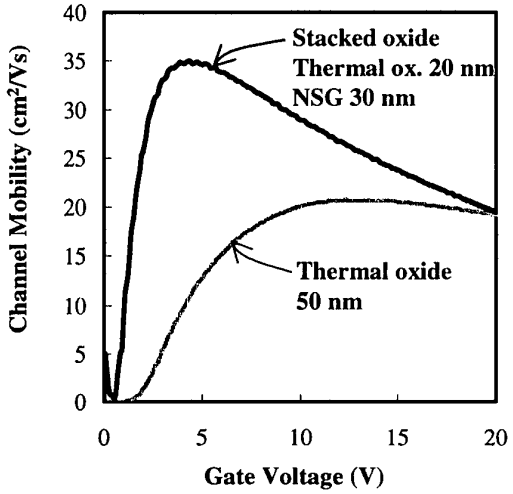


Fig. 5. μ_{FE} of 4H-SiC ACCUFET with thermal oxide or stacked oxide

Reference
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Correlation between inversion channel mobility and interface traps near the conduction band in SiC MOSFETs

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SiC MOSFETs are attractive switching devices in high-power and high-temperature electronic field. However, poor inversion mobility in the *n*-channel SiC MOSFETs is a serious problem especially in the 4H polytype. Several groups have reported that channel mobility is affected by an anomalously high interface trap density (D_{it}) near the conduction band edge (E_c). In this work, we evaluated the D_{it} near E_c by making capacitance-voltage (*C-V*) measurements for gate-controlled diodes (GCDs)[1]. Measurements of GCDs can be performed with MOSFETs, it makes possible a direct characterization between the interface traps and MOSFET channel mobility.

N-channel MOSFETs were fabricated on p^+ substrates with either a *p*-type 4H- or 6H-SiC homo-epitaxial layer (Si-face, N_A-N_D~$5x10^{15}/cm^3$), purchased from CREE Research. Source and drain regions were formed by phosphorous ion implantation. A gate oxide 40 ± 2 nm thick was grown at 1200°C in dry or wet O_2. Post-oxidation annealing was performed for some samples in pure hydrogen at 800°C for 30 min (H_2 POA) [2] or in wet oxidation ambient at 950°C for 180 min (wet re-oxidation annealing; wet ROA) [3]. The μ_{fe} values for the MOSFETs prepared using various gate-oxidation procedures are summarized in Table I. The data listed there are the average values for 30 MOSFETs prepared on the same wafer. The wet ROA treatment improved the μ_{fe} much more than H_2 POA.

The *C-V* measurement of the GCDs was performed with a frequency of 20 Hz at room temperature. N^+ source and drain regions were tied to the *p*-type substrates during the measurements. As in the operation of *n*-channel SiC MOSFETs, the minority carriers were available from the adjacent n^+ regions. Typical *C-V* property for the 4H-SiC GCD with the dry-oxidized gate oxide is shown in Fig.1. This curve show a clear accumulation and inversion property with some peculiar structures similar to those in the curves reported in *Ref.*4, where the "*hook and ledge*" feature of the curves was attributed to the charge trapping in the interface states. Occurrence of the strong inversion at the SiC surface is shifted from point B to C due to the existence of the deep interface traps, the surface potential $\Psi_S=2\Psi_B$ at point C (Ψ_B: bulk Fermi potential).

Here we define the difference between the gate voltages at C and D as $V_{C\text{-}D}$, where the capacitance at point D is equal to the flat band capacitance. The surface Fermi level moves toward the conduction band edge as increasing the gate voltage from point C to D. The values of the E_c-E_F at the SiC surface were calculated to be about 0.2 and 0.1 eV at point C and D, respectively. The interface trap density N_{it} within the energy range of E_c-E~0.1-0.2 eV can be estimated from $N_{it} = C_{ox} \times \Delta V_{C-D} / q$, where $\Delta V_{C\text{-}D}$ is the difference of the $V_{C\text{-}D}$ between the experimental and theoretical value, C_{ox} is the oxide capacitance per unit area and q is electronic charge.

The values of N_{it} were calculated for all the devices whose μ_{fe} values are listed in Table I, and the normalized channel mobility μ_{fe}/μ_{bulk} of the MOSFETs is plotted in Fig.2 as a function of N_{it}. The values of the μ_{bulk} used for the normalization were 800 cm^2/Vs for 4H and 400 cm^2/Vs for 6H. A close correlation between the channel mobility and shallow trap

density is clear in this figure. The μ_{fe}/μ_{bulk} of the MOSFETs is rapidly reduced as increasing N_{it} independent on the polytype and the preparation procedures. Therefore, this correlation strongly indicates that the significant cause of the low inversion channel mobility of SiC MOSFETs is the high density of shallow traps between the E_c and the surface Fermi level at strong inversion. Our results are further evidence that the degraded channel mobility is caused by the reduction of the free carrier density due to the charge trapping in the shallow traps and the consequent Coulomb scattering by the negatively charged traps[5].

This work was performed under the management of FED as a part of the METI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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Table I. The field effect mobility μ_{fe} in 4H- and 6H-SiC MOSFETs with different gate-oxide preparation procedures.

Oxidation	Post annealing	μ_{fe} (cm^2/Vs)	
		4H	6H
Dry	None	6.2	38.5
	H_2 POA	7.4	38.3
	Wet ROA	24.8	76.3
Wet	None	5.6	34.7
	H_2 POA	6.1	
	Wet ROA	15	52.2

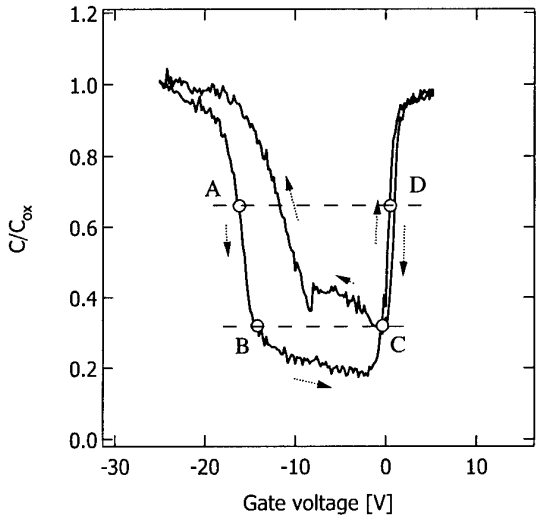


Fig.1. C-V curves obtained at room temperature for a 4H-SiC GCD with a dry-oxidized gate oxide.

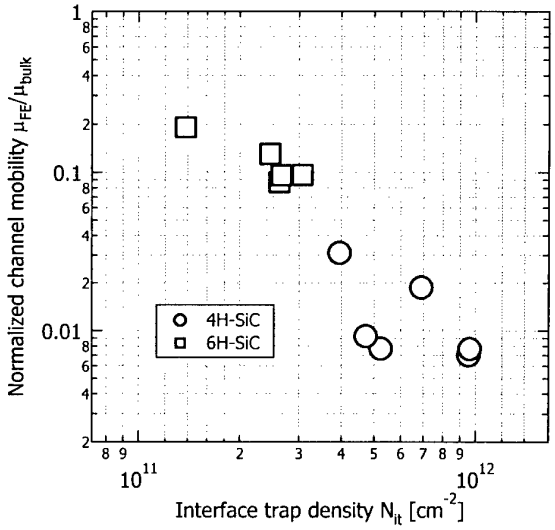


Fig.2. Normalized channel mobility μ_{fe}/μ_{bulk} of the 4H- and 6H-SiC MOSFETs plotted as a function of N_{it}.

LOW TEMPERATURE THERMAL OXIDATION OF ION AMORPHIZED 6H-SiC

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In this work the wet thermal oxidation of ion amorphised 6H-SiC was studied at temperature lower than 1100°C. The Rutherford Back-Scattering technique in the Channeling geometry was used to characterise the as-implanted and thermally treated samples.
6H-SiC on-axis and off-axis, p-type and n-type bulk substrates were ion implanted by Ar^+ at fluence and energy values such to produce an amorphous surface layer less than 200 nm thick. These samples were thermally oxidised in a wet ambient for different temperatures and time intervals in the ranges 750-1100°C and 15 - 40 min, respectively. Some polycrystalline, mostly 3C-SiC, and crystalline 6H-SiC samples were also processed for comparison.
Fig. 1 compares the oxide layer thickness grown for increasing temperature and fixed time (30 min) on samples ion amorphised, ion amorphised and re-crystallised, i.e. mostly polycrystalline 3C-SiC as described in [1], and crystalline 6H-SiC. For the amorphous samples two temperature intervals were identified: below and above 900°C, where the

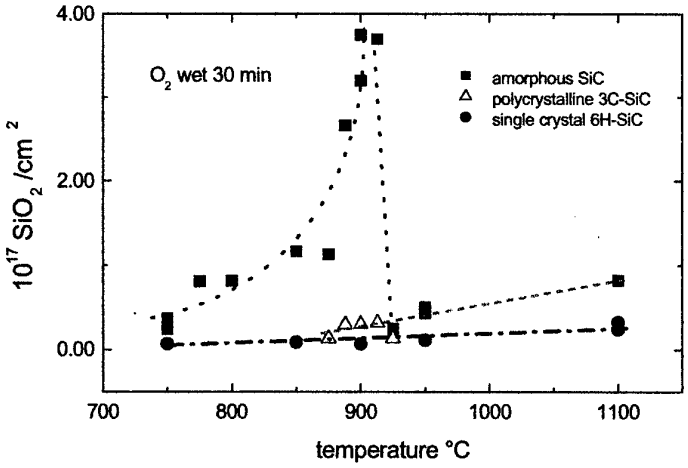


Fig. 1 Comparison among the oxidation of amorphous, polycrystalline and single crystal SiC for different annealing temperatures and constant anneling time. The rich oxygen ambient is wet.

oxidation rate were, respectively, fast and slow. The comparison with the reference samples shows that the trend above 900°C fits that of the polycrystalline samples, while below 900°Cit is much higher. Over all the temperature range the 6H-SiC phase showed the lower oxidation rate. The data about the ion amorphised samples were independent on substrate type and orientation.
The hypothesis of an epitaxial regrowth of the ion amorphised 6H-SiC at a temperature as low as 900°C can explain the trend of Fig. 1. In fact, the drop of the oxidation rate at 912°C may be due to the touch between a polycrystalline regrowth front and on oxide one. The analysis of samples oxidised at 900°C for different time confirmed such hypothesis.

[1] R. Nipoti and A. Parisini, Phylospphical Magazine B 80 (2000) 647-659

Study of Surface Morphology and Chemistry of 4H- and 6H-SiC After Cyclic Oxidation

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Abstract

In-depth Atomic Force Microscope (AFM) and X-ray Photoelectron Spectroscopy (XPS) studies were performed on the surface morphology and chemistry of heavily doped n-type 6H- and 4H-SiC epilayers after cyclic dry oxidation and oxide removal in 49% HF, and pirhana clean (p-clean). The objective was to determine the fundamental differences and changes on the surface morphology and chemistry between the two polytypes after similar oxidation and oxide stripping processes. The goal of this oxidation study was to identify the optimum surface quality that would support improved homogeneous electrical contact interface characteristics across the wafer. The result shows that the progression toward smoother surface morphology is tracked by the disappearance of C 1s binding energy spectral peaks due to adventitious carbon and related compounds.

AFM scans of 1 cm^2 samples measured at five locations showed the 6H-SiC roughness to average RMS = 0.58 nm (Fig. 1a), followed by an of average RMS = 0.54 nm (Fig. 1b) after the first four-hour 1150°C dry oxidation/HF strip/p-clean. The second five-hour oxidation/HF strip/p-clean had an average of RMS = 0.4 nm (Fig.1c). For the 4H-SiC, the as-received sample had an average roughness of RMS= 0.39 nm (Fig. 2a), and after the first oxidation/HF strip/p-clean the average was RMS=0.26 nm (Fig. 2b). The roughness after the second oxidation/HF strip/p-clean was measured as 0.31 nm (Fig. 2c).

The XPS survey spectra of the chemical species on the surface of both polytypes after each process cycle are shown in Figs. 3a and b. The as-received samples show up to 2.5 at. % chlorine (origin unknown) present on the surface. The chlorine concentration dropped below detection limits (0.1%) after the first four-hour oxidation/HF strip/p-clean. In the C 1s spectra of both the as-received 6H- and 4H-SiC shown in Figs. 4a and b, respectively, additional C 1s peaks at higher binding energies can be seen in addition to the primary carbide peak at 282.7 eV. After the first four-hour oxidation/HF strip/p-clean, the XPS C 1s spectrum of the 6H-SiC polytype still shows adventitious carbon as a higher binding energy shoulder while the C 1s spectrum of the 4H-SiC, on the other hand, shows a much cleaner carbide peak with minimal shoulder. The result in 6H-SiC was reproduced in three different sample sets. After the second oxidation/HF strip/p-clean, the three 6H-SiC sample sets looked more like the single carbide peak observed in 4H-SiC after only one oxidation.

It is not clear at the moment why the 6H-SiC samples required two oxidations and 49%HF stripping cycles to stabilize its surface (i.e. eliminate the extra C 1s shoulder) while the 4H-SiC required only one. It is worth noting that after the first oxidation, the 4H-SiC achieved a surface roughness equivalent to a Si-C bilayer step height (0.25 nm) while 6H-SiC has an average roughness equivalent to about a two Si-C bilayer step height. Reaction kinetics are known to be surface area driven[1]. In this particular experiment, the 4H-SiC will offer less area for adventitious reactions to take place after the first oxidation cycle. We will discuss these issues in broader terms within the context of relationships between surface morphology, surface chemistry, and the observed orientation dependency of specie concentration.

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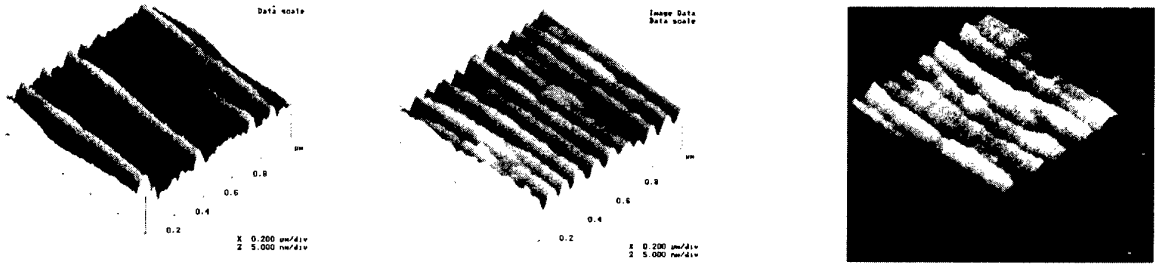


Fig. 1 (a) (b) (c)

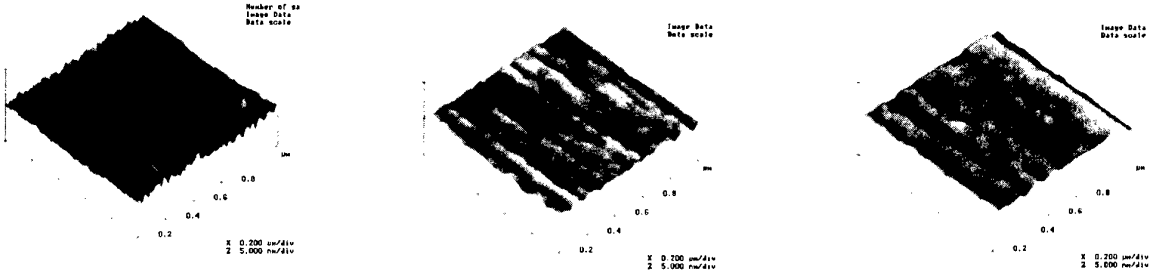


Fig. 2 (a) (b) (c)

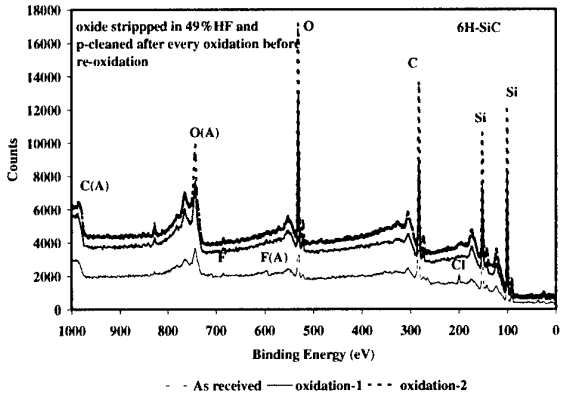
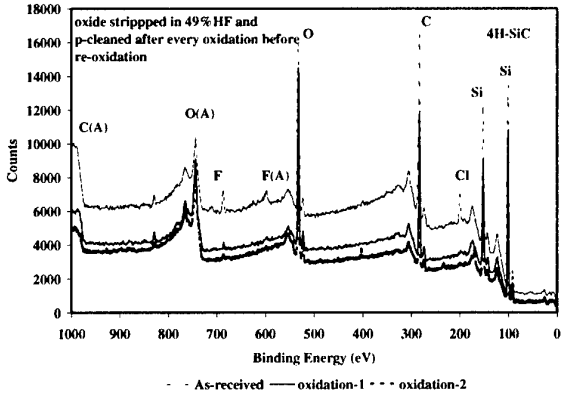


Fig. 3 (a)



(b)

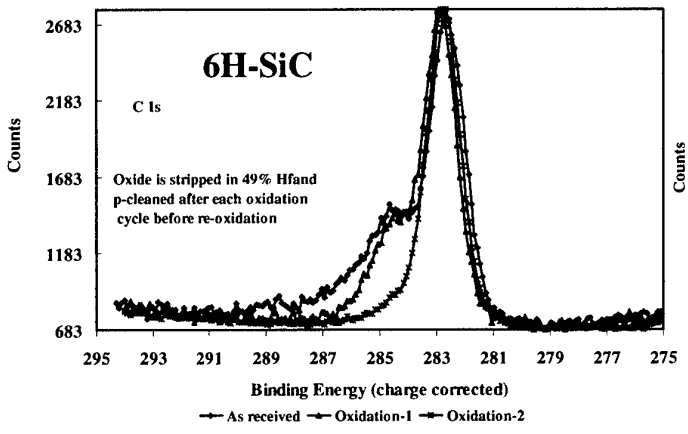
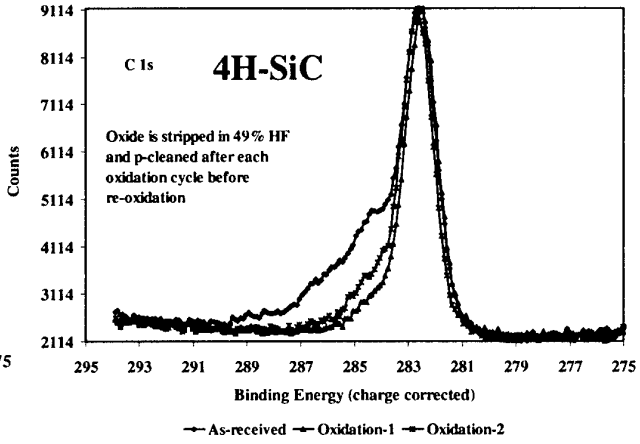


Fig. 4 (a)



(b)

Effects of successive annealing of oxides on electrical characteristics of SiC MOS structures

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Insulators on SiC are easily made by thermal oxidation process similar to the fabrication process of Si metal-oxide-semiconductor (MOS) technology. This is one of the most important characteristics of SiC for device applications. In order to realize SiC MOS devices with high performance specifications, it is important to fabricate the SiO_2/SiC interface with fine electrical properties. A few years ago, it was reported that the electrical characteristics of SiO_2/SiC interface are improved by the annealing in steam at 950°C for 3 hours (re-oxidation) [1]. However the re-oxidation is not optimized at present. In this conference, we propose the successive annealing of oxides in steam at different temperatures and report the decrease of interface defects in oxide layers of 4H-SiC MOS structures.

The 4H-SiC chips (5-mm in squire) with epilayers were made by cutting from 2-in. n-type (0001) wafers purchased from Cree Research Inc. The substrates were boiled with acetone and sulfuric acid to degrease their surfaces, and then sacrifice oxidation was performed twice. Thereafter, pyrogenic oxidation was carried out at 1100°C for 1 hour to form gate oxide layers of approximately 25 nm in thickness. At the final stage of the oxidation, annealing in steam at 950°C for 3 hours was performed and that at 800°C for 3 hours was successively carried out (successive annealing in steam). The successive annealing profile is shown schematically in Fig.1. After the process, gold was deposited thermally on the oxide layers to form gate electrodes of 25 nm in thickness. To make an ohmic electrode, the oxide layers on the backside of substrates were removed and aluminum was evaporated on the bared surface of the substrates. The simultaneous *CV* (*SCV*) characteristics were measured for the 4H-SiC MOS structures to obtain the gate

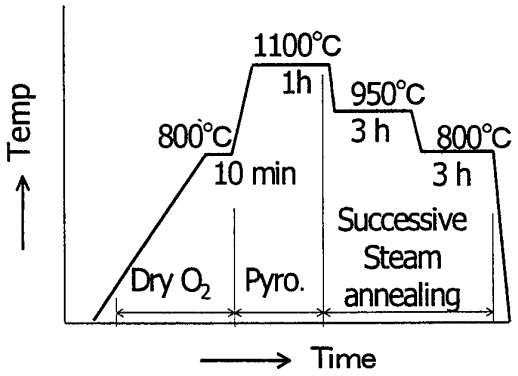


Fig.1 Successive annealing profile.

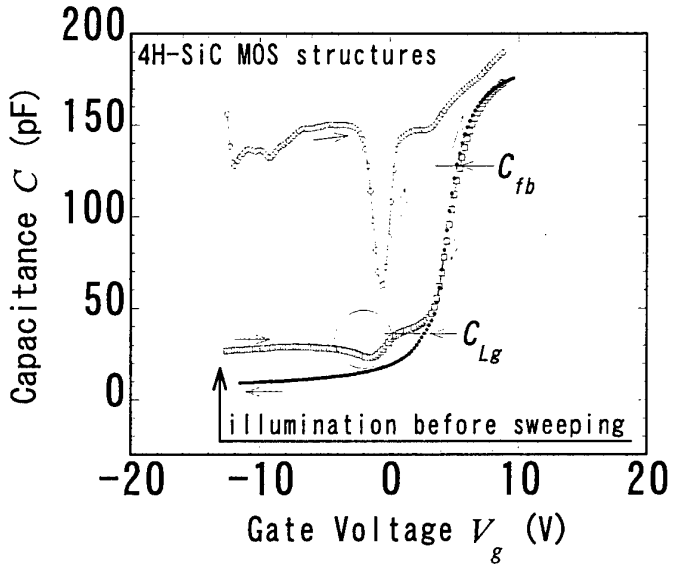


Fig.2 *SCV* characteristics of MOS structures on the Si face of a 4H-SiC substrate. The oxide layer is annealed in steam at 950°C for 3 hours and subsequently at 800°C for 3 hours. For *SCV* measurements, MOS structures were illuminated with a low-pressure mercury lamp to induce an inversion layer before sweeping the gate voltage.

voltage corresponding to flat band condition (V_{fb}) and the energy profile of interface trap density per unit area (D_{it}) near the conduction band edge. The *CV* curve swept rapidly from positive to negative gate voltage side was also measured for the same sample before and after the *SCV* measurements to calculate the net number of interface traps per unit area (N_{it}).

Figure 2 shows the *SCV* characteristics of MOS structures on the Si face of a 4H-SiC substrate, which is fabricated using the successive annealing in steam. The notations C_{fb} and C_{Lg} indicate the capacitance values corresponding to the flat band condition and the ledge of the high-frequency *CV* curve swept from negative to positive gate voltage side, respectively. There is a split near the depletion region between the high-frequency *CV* curves. This indicates that the interface traps exist around the mid-gap region. The difference in gate voltages at C_{Lg} level is found to be about 1.8 V. The high-frequency *CV* curve obtained by illumination winds down near the ledge and the quasi-static *CV* curve has a narrow valley near the region. The winding curve means the minority carrier redistribution [2]. These suggest that the number of interface traps near the valence band edge is scarce. The narrow valley and the winding for the *SCV* characteristics were not observed for the sample annealed in steam at 950°C for 3 hours only. On account of the difference, the number of interface traps near the valence band edge can be concluded to decrease by the successive annealing in steam. The successive annealing is effective method for the fabrication of MOS structures with fine electrical property.

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Gamma-ray irradiation effects on the electrical characteristics of 6H-SiC MOSFETs with annealed gate-oxide

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Since silicon carbide (SiC) has a strong radiation resistance[1], it is expected to be applied to electronic devices used in harsh radiation environments such as space. In the development of radiation resistant devices based on SiC, it is both important to improve their electrical characteristics before irradiation and to understand the degradation of the electrical characteristics of SiC devices due to irradiation. Recently, we have demonstrated that the electrical characteristics of SiC MOSFETs are improved by hydrogen (H_2) or steam annealing of the gate oxide just after the oxidation process[2]. Since the radiation response of MOSFETs strongly depends on the fabrication process of gate oxide, we have studied the influence of γ-ray irradiation on the electrical characteristics of SiC MOSFETs of which gate oxide was formed with different post-oxidation annealing conditions.

The MOSFETs used in this study were fabricated on p-type 10 μm thick epitaxial 6H-SiC films grown on 6H-SiC substrates (3.5° off, Si-face). The net acceptor concentration of the epitaxial films ranges from $5x10^{15}$ to $1x10^{16}$ /cm^3. The source and drain of the MOSFETs were formed using phosphorous ion implantation at 800 °C and subsequently annealed at 1500 °C for 20 min in an Ar atmosphere. The gate oxide was fabricated by pyrogenic oxidation (H_2:O_2 = 1:1) at 1100 °C for 60 min. Steam annealing for the gate oxide was carried out at 800 °C for 30 min in the same ambient as the pyrogenic oxidation. Hydrogen annealing was carried out at 700 °C for 30 min at a pressure of 20 Torr. The thickness of the gate oxide was determined by *C-V* measurements. The gate length and width of the MOSFETs are 10 μm and 200 μm, respectively. Gamma-ray irradiation was performed up to 530 kGy (SiO_2) at a rate of 8.8 kGy/h at room temperature (RT) During the irradiation, no electrical bias was applied to the gate, the drain and the source of the MOSFETs. The electrical characteristics were measured at RT under dark conditions. The channel mobility (μ) of the MOSFETs was derived based on the following procedures: First, the values of μ were estimated from the linear region of the drain current (I_D) versus drain voltage (V_D) curves in various gate voltage (V_G). Then, the best value obtained from the V_G dependence of μ was used as the value of μ in this study. The threshold voltage (V_T) was determined as the value at the intersection between the V_G axis and the line extrapolated from the curve of the square root of the drain current (I_D). Here, SiC MOSFETs with H_2-annealed gate oxides and steam-annealed gate oxide are referred to as SiC(H_2) MOSFETs and SiC(H_2O) MOSFETs.

Figure 1 shows the absorbed dose dependence of μ for SiC(H_2O) and SiC(H_2) MOSFETs. The value of μ in the un-irradiated SiC MOSFET fabricated without post-

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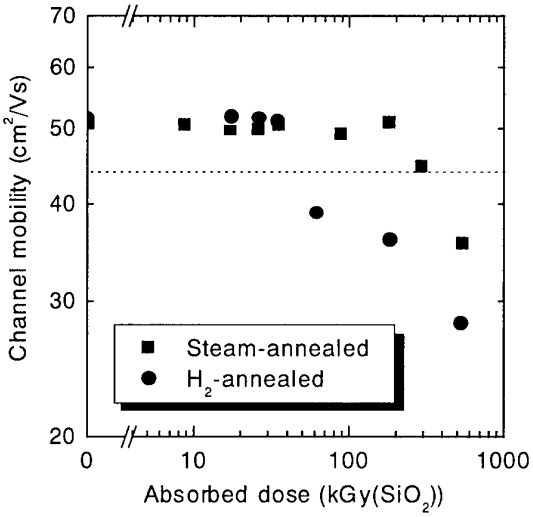


Fig. 1 Absorbed dose dependence of channel mobility for $SiC(H_2O)$ and $SiC(H_2)$ MOSFETs. The value of channel mobility for un-annealed SiC MOSFETs before irradiation is also indicated as the broken line.

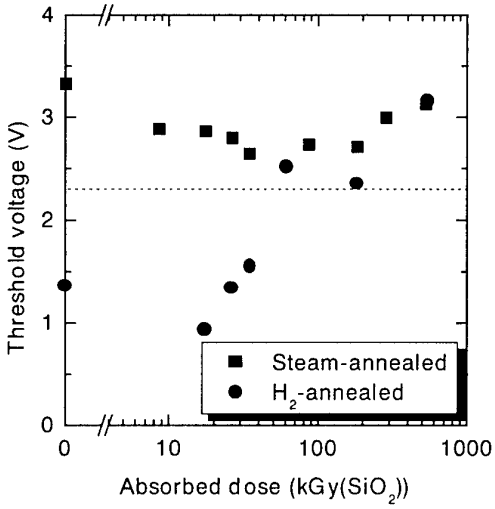


Fig. 2 Absorbed dose dependence of threshold voltage for $SiC(H_2O)$ and $SiC(H_2)$ MOSFETs. The value of threshold voltage for un-annealed SiC MOSFETs before irradiation is also shown as the broken line.

oxidation annealing (un-annealed SiC MOSFETs) is also shown as the broken line. Before irradiation, μ for both $SiC(H_2)$ and $SiC(H_2O)$ MOSFETs was 52 cm^2/Vs. As for $SiC(H_2)$ MOSFETs, the value of μ decreases at doses above 60 $kGy(SiO_2)$, and becomes 28 cm^2/Vs at 530 $kGy(SiO_2)$. On the other hand, μ for $SiC(H_2O)$ MOSFETs is not changed up to 200 kGy, and at 530 kGy, the value of μ is 35 cm^2/Vs.

Figure 2 shows the absorbed dose dependence of V_T for $SiC(H_2O)$ and $SiC(H_2)$ MOSFETs. The value of V_T for $SiC(H_2)$ MOSFETs decreases slightly at 17 kGy, and increases with increasing absorbed dose above 17 kGy. The change of V_T by irradiation up to 530 kGy is 2.2 V (from 0.9 to 3.1 V). With respect to $SiC(H_2O)$ MOSFETs, V_T decreases slightly with increasing absorbed dose below 34 kGy, and slightly increases with increasing absorbed dose once above 87 kGy. The change of V_T by irradiation is only within 0.6 V (2.7 to 3.3 V). For the radiation resistant devices, the stability of their electrical characteristics such as V_T under irradiation is very important. Thus, our results suggested that the radiation resistance of $SiC(H_2O)$ MOSFETs is higher than that of $SiC(H_2)$ MOSFETs.

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A large reduction of interface-state density for MOS capacitor on 4H-SiC (11$\bar{2}$0) face using H_2 and H_2O vapor atmosphere post-oxidation annealing

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SiC MOSFETs are expected as switching devices because of its high-speed ability. The field-effect channel mobility (μ_{FE}) of 4H-SiC MOSFETs is predicted to be higher than that of 6H-SiC because of higher bulk Hall mobility of 4H-SiC. However, actual μ_{FE} of 4H-SiC MOSFETs is much lower than that of 6H-SiC MOSFETs, which is originated from higher interface state density(D_{it}) at SiO_2/4H-SiC interface. Yano et al. reported the effective mobility as high as 30cm^2/Vs for 4H-SiC MOSFETs on (11$\bar{2}$0) face [1]. However, this value is not sufficient for the reduction of on-resistance (R_{on}) of 4H-SiC power MOSFETs with the relatively low blocking-voltage below 1kV. In this work, we have researched the effect of oxidation method and post-oxidation annealing (POA) on the D_{it} of MOS capacitor formed on 4H-SiC (11$\bar{2}$0) face.

N-type 4H-SiC (11$\bar{2}$0) bulk substrates were purchased from Cree Research Inc. The three n-type epitaxial layers were grown on bulk substrates. The thickness and effective carrier density (N_d-N_a) of bottom layer are 1.5μm and 1×10^{18} cm^{-3}. Those of middle layer are 0.5μm and 1×10^{17} cm^{-3}. Those of top layer are 0.1μm and 5×10^{15} cm^{-3}, respectively. The RCA cleaning was carried out. Next, a sacrificial oxide of 10nm thickness was grown, and then it was removed with 5% HF solution. Oxide films were thermally grown at 1150°C in dry O_2 (dry oxidation, samples (a),(c) and (e)), and in H_2O vapor atmosphere (wet oxidation, samples (b),(d) and (f)). The thickness of the oxide film was 50 ± 5nm. After both oxidations, all samples were annealed in argon for 30 min at 1150°C. In addition, the samples (c) and (d) were annealed in H_2 at 800°C for 30 min. The samples (e) and (f) were annealed in H_2O vapor atmosphere at 750°C for 3 h. Aluminum on the top of the oxide films and on the back of the samples was evaporated to make gate electrodes and ohmic contacts, respectively. The D_{it} estimations were performed using high-low technique and a KI82 system.

Figures 1 and 2 show the D_{it} distributions of the samples (a)~(f). The D_{it} of the sample on (0001) face with dry or wet oxidation following Ar annealing at 1200℃ are also shown for comparison. In the case of samples with the dry oxidation, the D_{it} of sample(a) on (11$\bar{2}$0) face with only Ar annealing is much higher than that of sample on (0001) face. This suggests that the μ_{FE} of 4H-SiC MOSFETs on (11$\bar{2}$0) would be lower than that of 4H-SiC MOSFETs on (0001) face. As shown in sample(c), the H_2 POA decreases the D_{it} in the shallow level from the conduction band edge (E_c). The D_{it} becomes the same value as that of (0001) face

near E_c-E =0.2eV. However, at the Ec-E=0.6eV, the D_{it} is one order of magnitude higher than that of sample on the (0001) face. The H_2O POA decreases the D_{it} in the energy level from 0.2eV to 0.6eV (sample(e)), which results in the almost same value as that of (0001) face. Hence, it is considered that the H_2O POA much improves the μ_{FE} of sample with the dry oxidation. On the other hand, in the case of samples(b),(d) and (f) with the wet oxidation, the D_{it} in Ec-E < 0.3eV is much lower than that sample on the (0001) face. This is the reason why the μ_{FE} of 4H-SiC MOSFETs on (11$\bar{2}$0) face with the wet oxidation is higher than that on (0001) face as reported by Yano et al. The H_2O POA reduces the D_{it} in the energy level from 0.2eV to 0.6eV (sample (f)). Moreover, H_2 POA reduces the Dit in the energy level deeper than 0.35eV(sample(d)). This means the H_2 POA much improves the μ_{FE} of MOSFETs on (11$\bar{2}$0) face. Indeed, we found that the μ_{FE} reached 110cm^2/Vs using the wet oxidation and H_2 POA technique[2]. Therefore, both the wet oxidation and H_2 POA technique is excellent for the gate-oxide formation process of 4H-SiC MOSFETs on (11$\bar{2}$0) face.

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Acknowledgement

This work was performed under the management of FED as a part of the METI NSS Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

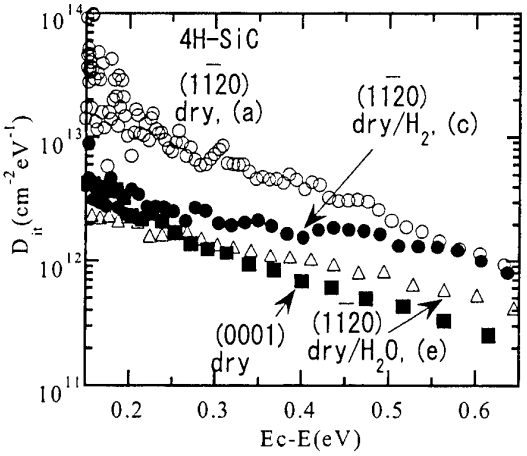


Fig. 1 Effect of POA on D_{it} distribution of samples with the dry oxidation.

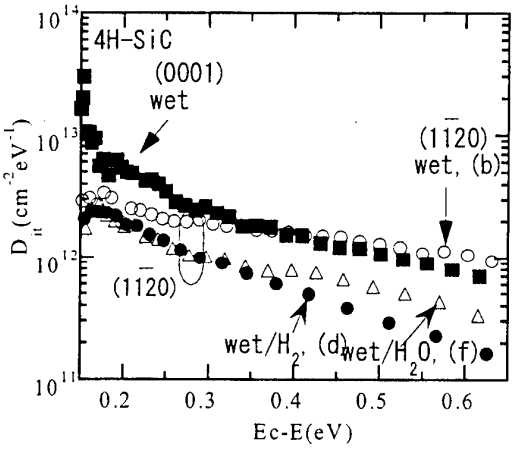


Fig. 2 Effect of POA on D_{it} distribution of samples with the wet oxidation.

Influence of the wet re-oxidation procedure on inversion mobility of 4H-SiC MOSFETs

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SiC-based metal-oxide-semiconductor field effect transistor (MOSFET) is one of the candidates for high power and high frequency electric device applications, because SiC can be thermally oxidized to form a SiO_2/SiC structure. Among many SiC poly-types, recent interesting has shifted to the 4H- from 6H-SiC, because the former has higher electron mobility with its small anisotropy. However, the channel mobility of 4H-SiC(0001) based MOSFETs is far below the predicted value from 4H bulk electron mobility. It has been reported that a wet re-oxidation treatment after gate oxide formation is effective to improve the low channel mobility of 6H-SiC MOSFETs by several researchers[1]. In this study, we applied the wet annealing treatment with various conditions to 4H-SiC(0001) MOSFETs and investigated the dependence of the MOSFET characteristics on those conditions.

N-channel MOSFETs were fabricated on the 8° off angled p-type 4H-SiC(0001) substrates with p-type epitaxial layer from Cree Research Inc. Effective doping density (N_d-N_a) of the epitaxial layer was about $5x10^{15}$ cm^{-3}. The channel length and width were 100 and 150 μm, respectively. Source and drain were formed by phosphorous ion implantation and an activation annealing for the implanted layer was conducted at 1500°C for 5min. Gate oxide was formed at 1200°C for 140 min in dry O_2 ambient following a post oxidation annealing (POA) in Ar ambient at the same temperature. Wet re-oxidation annealing (wet ROA) was carried out after the Ar POA on various conditions, (a) at 950°C for 180 min, (b) at 850°C for 180 min, (c) at 1050°C for 180min, (d) at 950°C for 60 min. Al was evaporated as both the gate metal and the contact metal for source and drain. No contact annealing was done after the Al deposition.

Figure 1 shows typical drain current-voltage (I_d-V_d) characteristics of FET(a), where the gate voltage (V_g) changed between 0 to 12 V with 3 V steps. The I_d-V_d characteristics exhibit good linear and saturation regime, and positive threshold voltage (V_{th}). This trend was observed for all FETs fabricated in this study (not shown here). A field-effect mobility (μ_{FE}) was calculated from the slop of the I_d versus V_g characteristics. Fig. 2 shows a typical μ_{FE} as a function of V_g at V_d=100mV for FET(a)-(d). The peak values of μ_{FE} depend extremely on the wet annealing conditions. That is, the μ_{FE} value increased critically on the FET(a) of 38 cm^2/Vs and no significant improvements were observed on the FETs(b)-(d) of

8-9 cm^2/Vs compared with those of standard SiC MOSFETs. This dependence of the μ_{FE} was relevant to the measured effective charge density of the MOS capacitors formed on each test elemental group. The V_{th} was extracted from the intercept on V_g axis made by the tangent line of $I_d^{1/2}$-V_g plot at V_d=10V. The average value of μ_{FE}, V_{th} and μ_{sat} was summarized on the table I. Thus, it was found that the wet ROA improved the channel mobility of 4H-SiC MOSFETs and the effects largely depend on the annealing conditions.

Another interest of this work is why the channel mobility increased by the wet ROA. Recently, it was reported that the wet ROA caused a conformational change in the structure of the SiO_2/SiC and resulted in converting the Si-Si transition layer into SiO_2 thereby shortening the transition region[2]. To examine whether the effects of the wet ROA remain after the following annealing in inert gas ambient, Ar annealing at 1000°C for 30min was conducted after the wet ROA at 950°C for 180min. The peak value of μ_{FE} after the Ar annealing reduced approximately one-third of that for FET(a). This suggests the wet annealing treatment seems not to be irreversible effects such as the structural change as mentioned above and/or the removal of the interfacial carbon rich region[3]. We believe that the wet annealing causes some sort of inactive effect by –H and/or –OH termination and the effect was diminished by the following Ar annealing. This work was performed under the collaboration of AIST and FED as a part of the METI NSS program (R&D of Ultra-low-Loss Power Device Technologies) conducted by NEDO.

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Table I Summary of μ_{FE}, V_{th} and μ_{sat}

	μ_{FE} [cm^2/Vs]	V_{th} [V]	μ_{sat} [cm^2/Vs]
(a)	33.5	4.6	19.3
(b)	8.9	6.9	3.4
(c)	8.3	8.2	2.4
(d)	8.2	7.9	3.2

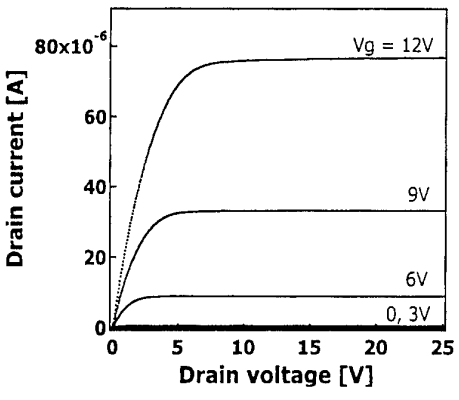


Fig. 1 Output characteristics of FET(a)

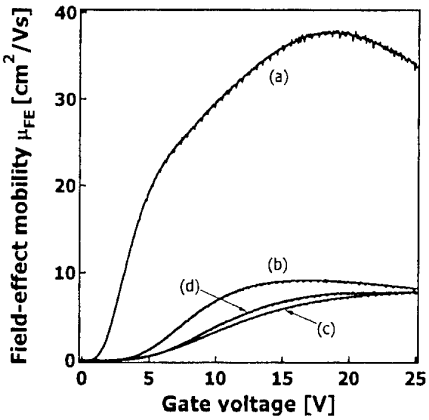


Fig. 2 Field-effect mobility for FETs(a)-(d)

Reduction of Interface Trap Density in 4H-SiC MOS by High-Temperature Oxidation

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4H-SiC semiconductor has the excellent physical characteristics for power-application devices. However, 4H-SiC MOSFET have never realized the ideal on-resistance performance because of the very low channel mobility. One of the origin for the low channel mobility is the high interface trap density, especially at the interface energy near the conduction band edge[1]. R.Schorner et al. reported that the residual carbon at MOS interface might make the interface trap density high [2].

In this paper, the reduction of the residual carbon and of the interface trap density have been realized by the thermal oxidation at high temperature (higher than 1200℃).

We reported that a carbonized layer on 4H-SiC Si-face, on which a thermal oxide layer on Si was located as face to face, can be reconstructed to SiC[3]. The carbonized layer was made by the Si sublimation in Ar ambience (50mTorr) at 1600℃. Gibbs free energy of the chemical equation(1) indicates that the carbon and the oxide should be SiC at high temperature(>1200℃) condition.

$$SiO_2 + 3 \cdot C \rightarrow SiC + 2 \cdot CO \cdots\cdots\cdots\cdots (1)$$

The reconstructed SiC should be made by the reaction between the carbon layer and the oxide. If the reconstruction velocity from carbon and SiO_2 to SiC is sufficiently larger than the generation velocity of the residual carbon, the generation of the residual carbon during the oxidation process should be vanished and the interface trap density will be reduced. So, we carried out the high temperature (>1200℃) oxidation.

We fabricated the MOS diodes for estimating the residual carbon and the interface trap density. 4H-SiC epitaxial wafers with (0001) Si face were prepared. The gate oxides were thermally grown in wet or dry O_2 ambience at 1080～1250℃. The oxide thickness is about 40nm. The gate electrodes and the back-side ohmic contacts are Al and Ni (annealed at 1000℃), respectively.

The residual carbon at MOS interfaces were analyzed by the low-take-off angle XPS method, after removing the oxides by HF. The low-take-off angle ($\leqq 15^\circ$) XPS method can estimate the binding energy of the atom at only the SiC surface(electorn escape depth $\leqq$ 0.3nm). The residual carbon at the interface of the 1250℃ dry oxide is 40% lower than the one of the 1080℃ wet oxide.

Figure 1 shows the interface trap density (Dit). Dit was estimated from the Capacitance-Voltage measurements and Hi(100kHz)-Low method at RT. The voltage scanning rate of the C-V measurement was 0.1V/sec. It clearly shows that the Dit is more reduced as higher the oxidation temperature in both ambience, wet and dryO_2. However, the Dit in wet and dryO_2 ambience is different. It is not cleared why the phenomena took place, but we guess that the ratio between the reconstruction velocity and the the oxidation velocity might be different in the oxidation ambience because the oxidation velocity in wet ambience is much lager than the one in dryO_2 ambience.

In conclusion, the oxidation process at higher temperature than 1200℃ reduce the residual carbon and the interface trap density(Dit). Especially, the Nit (which is integrated Dit between 1.0～1.4eV) of the oxide thermally grown at 1250℃(in dryO_2 ambience) is 60% reduced as compared to the one at 1080℃(in wet ambience).

[1]M.K.Das, B.S.Um, and Cooper,Jr, Materials Science Forum Vols.338-342, p1069 (2000)
[2]R.Schorner et al.,IEEE Electron Device Let., Vol.20, No.5, p241 (1999)
[3]E.Okuno et al.,Proc. of 9th Meeting on SiC and Related Wide Bandgap Semiconductors, p29 (2001), in Japanese

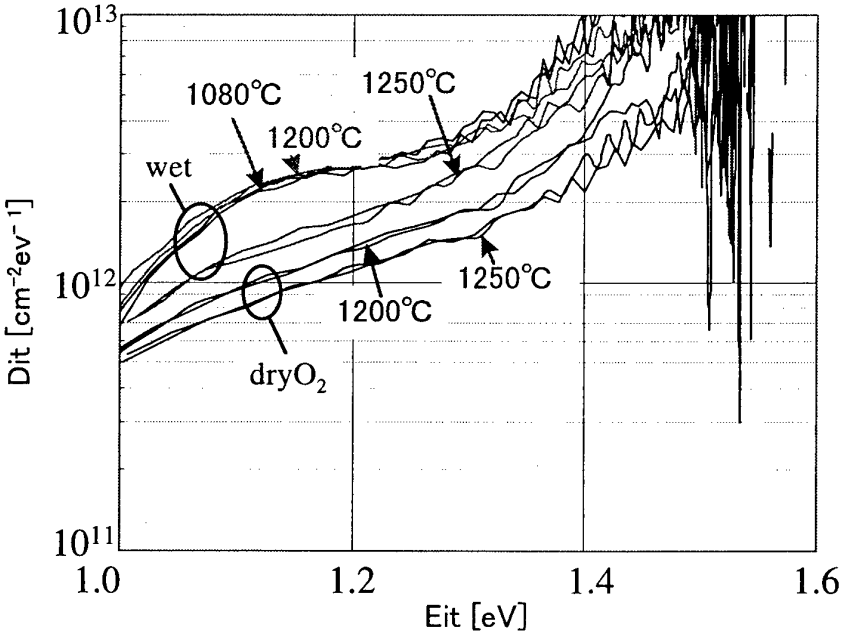


Figure 1 Interface Trap Density(Dit) dependence on Eit (Eit is the energy from Midgap)

INFLUENCE OF DEPOSITION PARAMETERS AND TEMPERATURE ON STRESS AND STRAIN OF IN-SITU DOPED PECVD SILICON CARBIDE

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Abstract

Thin films of silicon carbide (SiC) deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) technique are very attractive for IC-compatible MEMS as structural material and as coating layer. These amorphous films, although deposited at temperature lower than 400°C, maintain most of SiC excellent properties such as high mechanical strength, high thermal conductivity and extreme chemical inertness in several liquid electrolytes.

In this paper we present the influence of deposition parameters such as pressure, temperature, power, gas flow rate on stress and strain of in-situ doped and undoped PECVD SiC films. In fact the mechanical properties of the SiC films that are crucial for its application to MEMS, are affected strongly by the deposition parameters. The thickness of SiC films is measured by using spectroscopic ellipsometry. The density of these films depends on the deposition parameters and is calculated in range of $2mg/mm^3$ to $2.5mg/mm^3$. The values of the parameters investigated are varied in the range indicated in Table 1.

Both compressive and tensile stress films can be deposited. Stress values between - 700MPa and + 400MPa can be obtained. A shift from compressive toward the tensile region is observed for increasing SiH_4/CH_4 gas ratio (see Fig.1) and for increasing pressure. This tendency is reversed for increasing total RF power or its LF component. A strong change in stress is measured when doping gas is added or after an annealing cycle up to 650°C (see Fig.2). The influence of two commonly used substrates, thermal silicon oxide and PSG (phosphosilicate glass) on the stress of undoped and in-situ doped SiC is indicated in Fig.3.

The process flow schematically depicted in Fig.4 is used to release the rotating structure that is capable of measuring both compressive and tensile strain. The displacement of the pointer due to the strain is shown in Fig.5 for an undoped and a phosphorous-doped film. The study presented here allows us to establish the proper values for the deposition parameters to obtain as-deposited low-stress films for both undoped and p-or n-type SiC films.

Keyword: *Silicon carbide, stress, strain, PECVD, IC compatibility*

Table 1: Preparation condition of in-situ doped and undoped silicon carbide layers

Parameter	Value
Temperature	300°C ÷ 400°C
Pressure	1.5 ÷ 3 Torr
SiH_4 flow	0.05 ÷ 0.25 slm
CH_4 flow	fixed at 3 slm
PH_3 flow	4% of total gas
B_2H_6 flow	4% of total gas
Total power	600 ÷ 2500 watts
LF power	25%, 50%, 75%

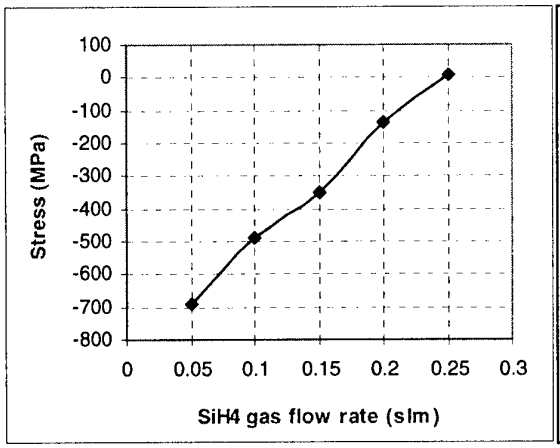


Fig.1: Stress of silicon carbide as a function of SiH_4 flow rate.

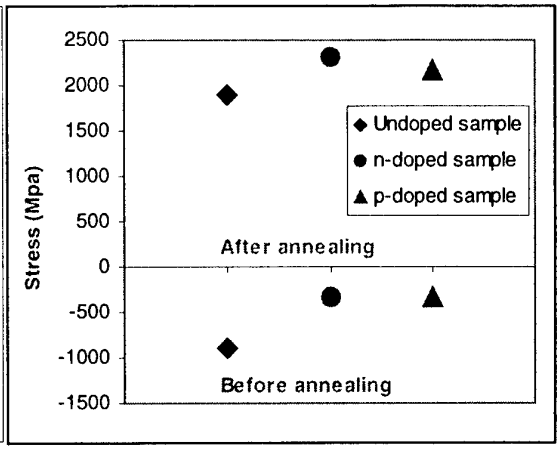


Fig.2: Stress of undoped and doped silicon carbide before and after annealing

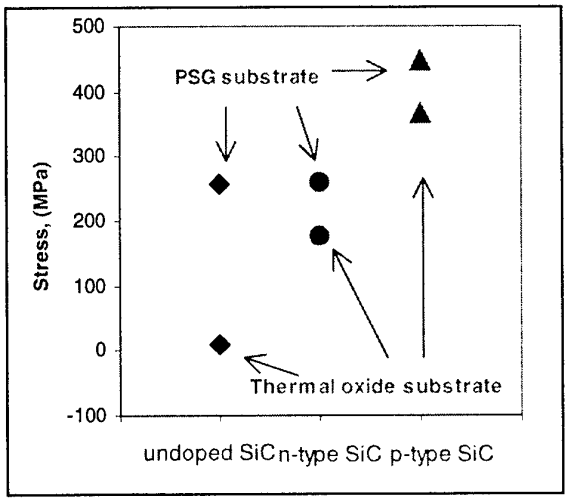


Fig.3: Stress of undoped and doped silicon carbide film depends on different substrates

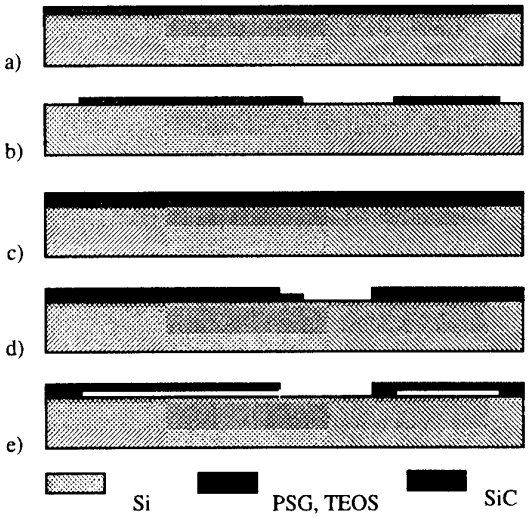


Fig.4. Schematic view of the process flow to release the strain measurement structure.

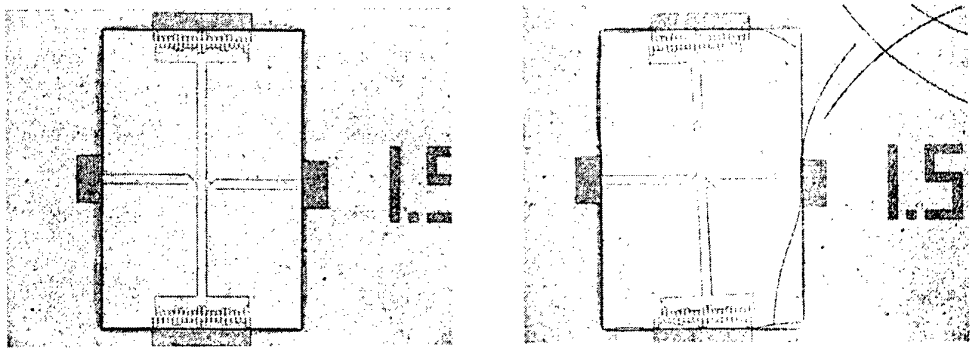


Fig.5: Optical image of the strain measurement rotating structure after release for an undoped (left) and a Phosphorus – doped (right) silicon carbide layer

Development of a Multilayer SiC Surface Micromachining Process with Capabilities and Design Rules Comparable Conventional Polysilicon Surface Micromachining

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SiC is well known for its excellent mechanical, electrical and chemical properties, making it attractive for microfabricated sensors and actuators operating in harsh environments. Recent advances in SiC patterning techniques have led to the development of surface micromachining processes that are successful in both single and multilevel implementations [1]. To date, however, a multi-user fabrication process with capabilities and design rules comparable to conventional polysilicon processes has not been developed for SiC. This paper details our development of such a process, which we call the Multi-User SiC (MUSiC) process.

The MUSiC process is an eight-mask, four structural layer polycrystalline SiC (poly-SiC) surface micromachining process that generally embodies the Cronos Integrated Microsystems polysilicon MUMPs™ design rules. Due to limitations associated with SiC RIE (e.g., poor selectivity to SiO_2 and polysilicon, micromasking, and low etch rates), the MUSiC process cannot currently be realized by directly implementing the MUMPs fabrication process sequence using poly-SiC. Instead, a micromolding technique that uses SiC film deposition into microfabricated polysilicon and SiO_2 sacrificial molds, followed by mechanical polishing and chemical etching, is used to create patterned poly-SiC structural layers on sacrificial layers (Fig 1). The mechanical polishing steps are used to expose the molds and to create globally planar surfaces at each structural layer. The polysilicon sacrificial molds are dissolved in KOH, and the SiO_2 sacrificial molds in HF to release the devices. The micromolding technique creates featureless field areas, microstructures with smooth and vertical side walls, and top surfaces that are ideal for multilevel processing.

The inaugural MUSiC layout incorporates eight different chip designs replicated 6 times across a 100 mm-diameter wafer. The chip designs include accelerometers, lateral resonators, mechanical characterization structures, micromirrors, capacitive pressure sensors, shear stress sensors, micromotors, and flow sensors. The fabrication process was carried out on 100 mm-diameter Si wafers using poly-SiC films deposited by APCVD in a rf-induction heated reactor designed for epitaxial growth. SEM micrographs of a representative collection of completed SiC devices are shown in Figs. 2, 3, and 4. The first run of the MUSiC process has been successful in terms of pattern generation (~80%). However, issues related to residual stress, stress gradients, polishing selectivity, and deposition uniformity adversely affect fabrication yield and device performance. These issues can be attributed to the APCVD process, leading us to develop a LPCVD furnace to deposit poly-SiC films on large numbers of Si substrates.

The extended paper will detail issues related to the fabrication process, implementation of micromolding on large-area wafers, results from the mechanical and electrical properties test chips, and other issues pertinent to the successful development of the process. Initial results using the LPCVD furnace will also be presented.

[1] M. Mehregany and C.A. Zorman, "SiC MEMS: opportunities and challenges for applications in harsh environments", *Thin Solid Films,* vol. 355 – 356, pp. 518-524, 1999.

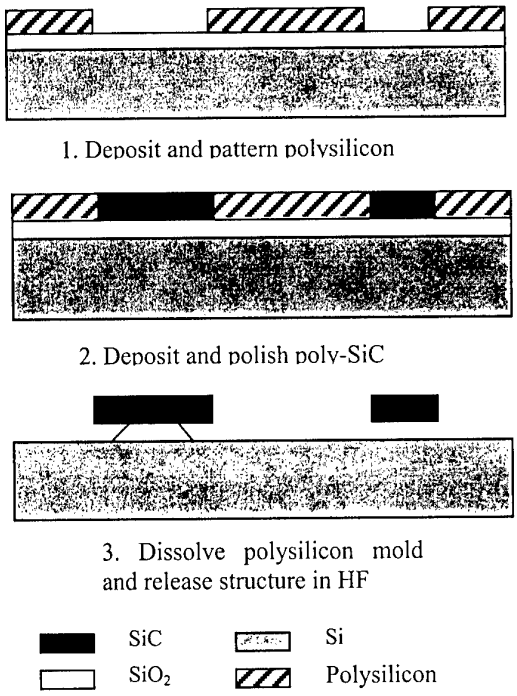


Fig. 1 Cross sectional schematics of the micromolding process.

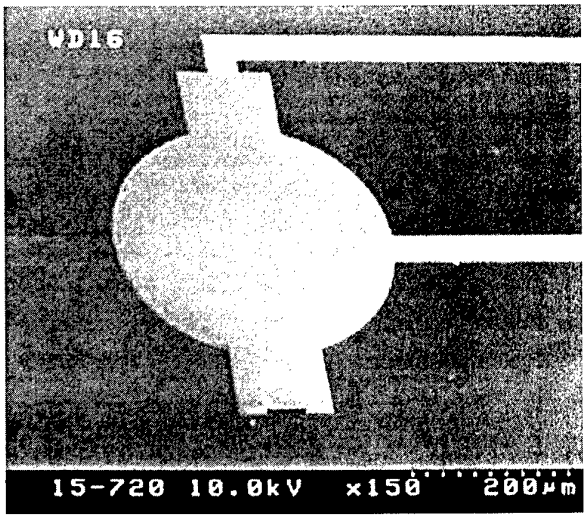


Fig. 2. SEM micrograph of a SiC capacitive pressure sensor.

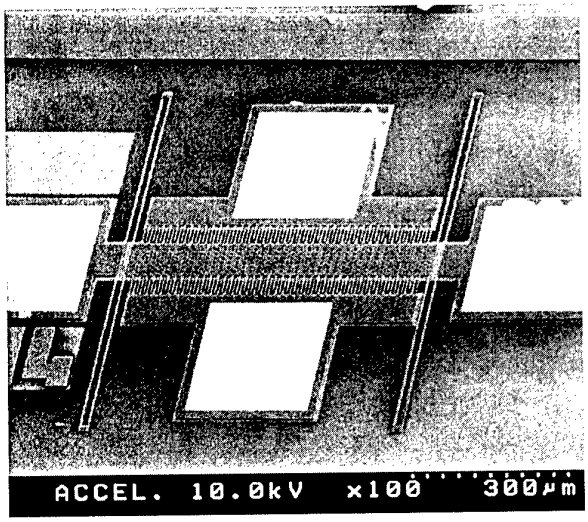


Fig. 3. SEM micrograph of a SiC shear-stress sensor.

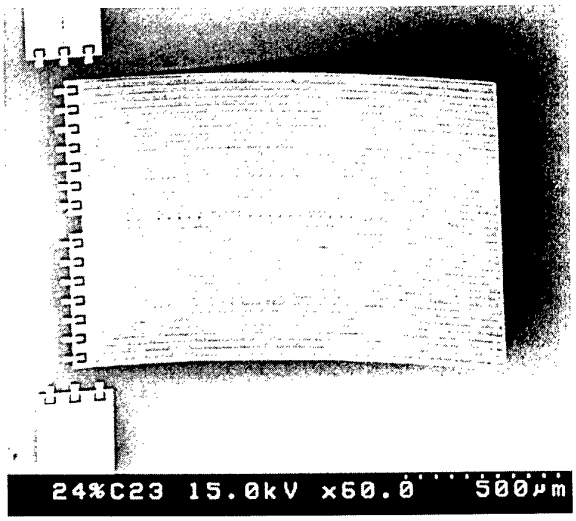


Fig. 4. SEM micrograph of a SiC micromirror showing the effects of residual stress gradient.

Reverse Characteristics of 4H-SiC Schottky Barrier Diode

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The Schottky barrier diode (SBD) on silicon carbide (SiC), a wide-gap semiconductor material, has the outstanding feature of high speed and low loss compared with the conventional SBD on Silicon (Si). A SiC SBD is designed so that the electric field at the Schottky interface is about 10 times as large as that of a Si SBD, when the reverse voltage is applied. Thus, it is necessary to investigate the effect of high electric fields on the reverse leakage current of SBDs. In this work, the reverse characteristics of a 4H-SiC SBD are analyzed using a device simulator, which can consider the tunneling process in addition to the thermionic emission. In the device simulator, the tunneling process is handled by setting up a generation/recombination probability, which takes the tunneling process into consideration, for each node of the mesh in the vicinity of a metal/semiconductor interface [1].

The calculated reverse characteristics of a 4H-SiC SBD are shown in Fig. 1. The solid line shows the leakage current calculated by the tunnel model. The broken line shows the leakage current calculated by the barrier-lowering model, which considers the Schottky barrier lowering by the image force. The dotted line shows the leakage current calculated by the conventional thermionic emission model. Figure 1 shows that the tunneling process dominates the reverse leakage current of a SiC SBD when a high reverse voltage is applied. The reverse characteristics of a Si SBD are also shown in Fig. 2, for comparison. In the reverse characteristic of a Si SBD, the increase in the leakage current induced by the barrier lowering is also important, and the effect of the tunneling process on the leakage current is relatively small compared with a SiC SBD, because the electric field applied to the metal/semiconductor interface is much lower than that of a SiC SBD.

If off-state loss due to the leakage current of a SiC SBD limits the total loss, we have the option of decreasing the electric field at the metal/semiconductor interface, or increasing the Schottky barrier height in order to reduce the off-state loss. However, both of these actions increase the on resistance. We have investigated whether a junction-barrier Schottky diode (JBS) would improve the trade-off between the leakage current and the on resistance by device simulation, considering the tunneling process for the first time. The schematic cross-section of a JBS is shown in Fig. 3, where the electric field at the metal/semiconductor interface is relaxed by the static induction effect from the p well. Figure 4 shows the forward (a) and reverse (b) characteristics of the 4H-SiC JBS. It can be seen from Fig. 4 that the reverse leakage current decreases by order without an increase in the on resistance, as the dimensions of the striped pattern of the p well and Schottky junction decreases.

This work was performed under the management of FED as a part of the METI project (R & D of Ultra-Low Loss Power Device Technologies) supported by NEDO.

[1] M. Ieong et al., IEDM-98, pp. 733-736, 1998

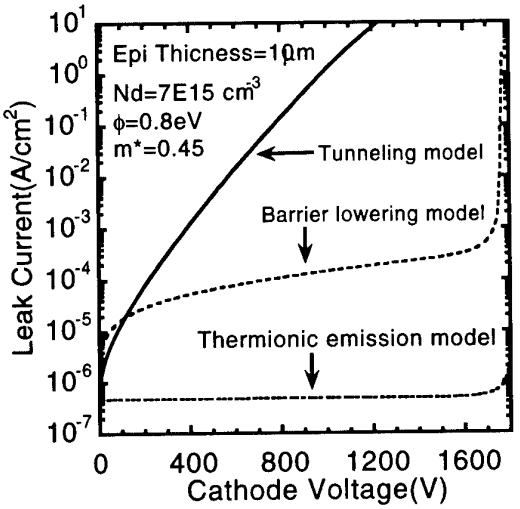


Fig.1: Calculated reverse characteristics of 4H-SiC SBD.

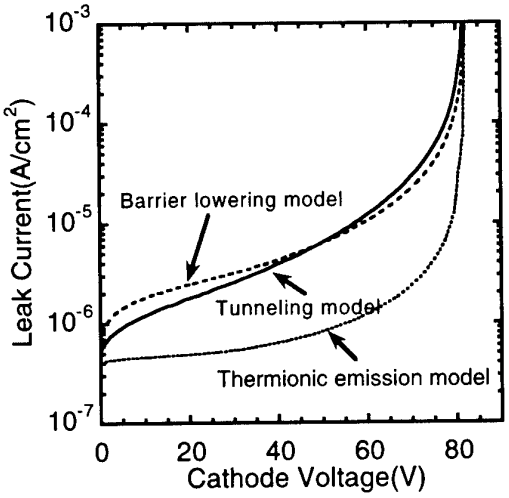


Fig.2: Calculated reverse characteristics of Si SBD.

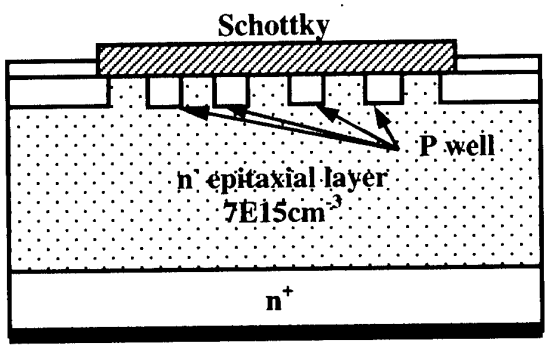


Fig. 3: Schematic cross section of a SiC Junction Schottky Barrier Diode (JBS)

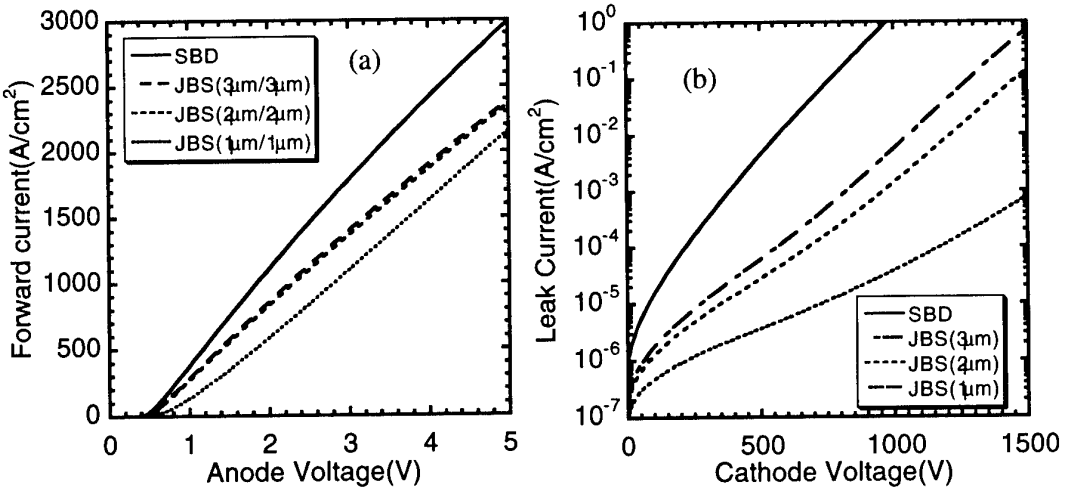


Fig. 4: Current-voltage characteristics of 4H-SiC JBS. (a) Forward characteristics of JBS. (b) Reverse characteristics of JBS. SiC SBD characteristics are shown for comparison.

High Voltage SiC Diode Design—An Experimental Study

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Abstract: High voltage SiC Schottky diode, device and process optimization is presented with experimental demonstration for 2.5KV and 1KV Schottky design. 2.5KV diodes were fabricated with a mean on-voltage of 1.85V at 2.25A (current density of 100A/cm^2) and a differential on-resistance of 6mΩ-cm^2. At 5A, these devices have an on-voltage of 2.6V. These devices were fabricated with a yield of 20%. Smaller sized devices 1mmx1mm in dimension were fabricated with a yield of 40%. Fig. 1 and 2 show the reverse bias characteristics and forward bias characteristics for a typical diode. To our knowledge this is the best result reported thus far for this voltage/current rating. Many process and design parameters control the outcome of the device. The most critical parameters are implant species, implant activation, termination design, Schottky surface preparation, Schottky metal, epitaxial layer doping and thickness. We present the impact of these parameters briefly here, in the paper we will explain the concepts in detail along with experimental data.

Implant activation is essential for the devices to work. The key issues facing implant activation are step bunching, and surface decomposition. There have been many reports on activation placing the wafer in the vicinity of another SiC source. However, even with this technique activation at 1700C causes step bunching. We have addressed this issue by doing the activation very fast, only a few seconds at 1700C, with the wafer enclosed in a SiC container. While this time is insufficient to cause surface damage, it is enough to allow good activation. Fig. 3 shows an SEM picture of the surface after implant activation. It includes three regions: a) unetched/non-implanted, b) etched and implanted and c) etched but non-implanted. From the picture it can be seen that regions b and c which were etched show step bunching while the unetched region is free from such irregularities.

Aluminum and boron are the two practical choices for p-type dopants for SiC. Boron is lighter than aluminum and hence is implanted deeper for the same energy. Further boron diffuses during activation [ref], and hence deeper junctions can be formed using boron. Hence boron is preferred over aluminum for termination design. However for a good termination design we found the difference to be small. To optimize the termination design, we made devices with different termination structures including various field plate designs, floating field rings, and JTE termination. Highest breakdown voltage, 3000V, was obtained using aluminum implant with a floating field ring design. Boron JTE (2600V) performed better than aluminum JTE (2200V). These results will be presented in greater detail in the full paper.

The ideality factor of the Schottky contact plays a principal role in determining the on-state voltage of the diode. Poor ideality factors usually result in lower leakage current at the expense of large increase in the on-voltage. A small change in ideality factor, for example from 1.1 to 2.5, could easily increase the on-state voltage by two volts. Figure 5 compares the forward conduction characteristics for the two cases—ideality factor=1 and 2. Notice that the on-state voltage is increased from 1.4V to 2.4V. The Schottky ideality factor is very sensitive to the surface conditions. We have found that RIE etch of the Schottky surface prior to the implant activation results in poor ideality factors. Further RIE etching using CF4 or CHF3 chemistry, after implant activation significantly increases the ideality factor. Hence care needs to be taken to protect the Schottky surface.

We have performed theoretical calculations on the epitaxial layer doping and thickness for device optimization, and obtained a correlation for Epi thickness $W=1.5xBV/E_{critical}$ where BV is the desired breakdown voltage and $E_{critical}$ the breakdown electrical field. Detailed analysis will be presented in the paper. High temperature results, including measurements at 250C will also be presented in the paper.

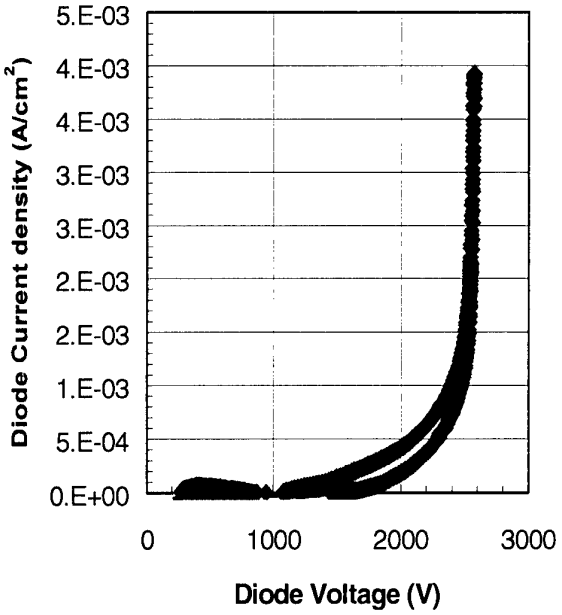


Fig. 1 Shows the reverse blocking characteristics of the diode. Size 2.25mm^2.

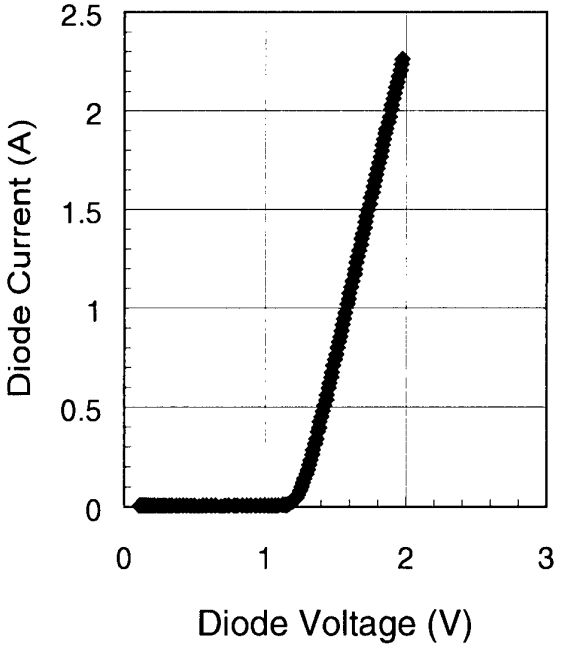


Fig. 2 Shows forward bias characteristics of the diode. Size 2.25mm^2.

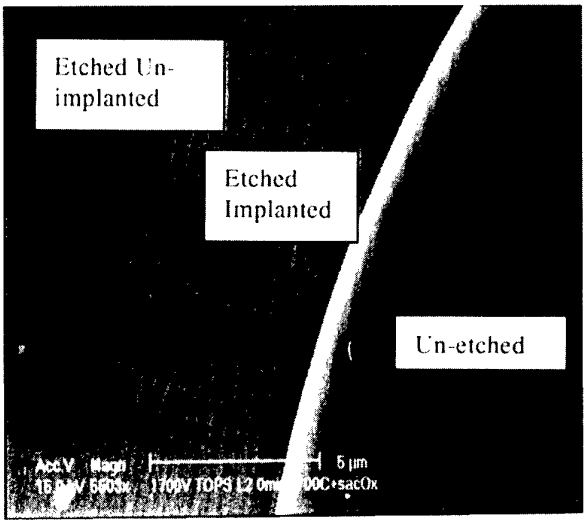


Fig. 3 Shows the SEM picture of a wafer showing three regions, a) Unetched SiC, b) Implanted and etched SiC, and C) Etched and Un-implanted SiC, after 1700C anneal.

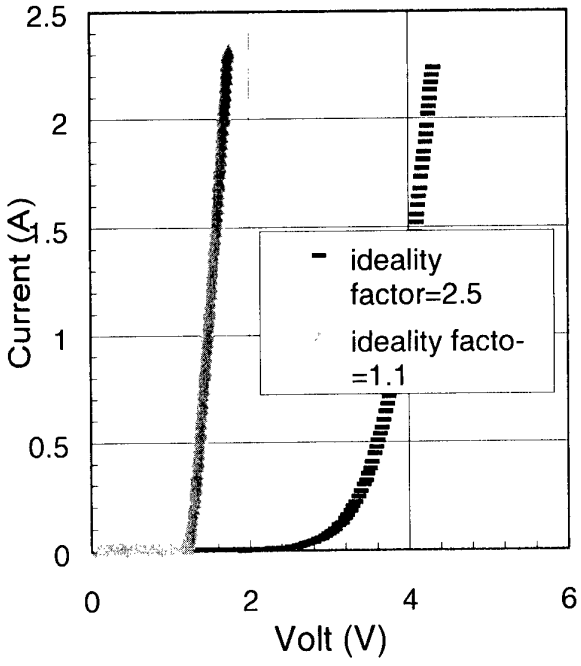


Fig. 4 Shows forward bias characteristics of two diodes with different schottky contact ideality factors.

Optimisation of Implanted Guard Ring Terminations in 4H SiC Schottky Diodes

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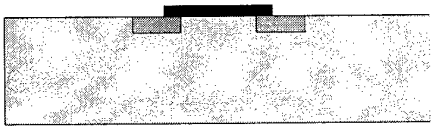
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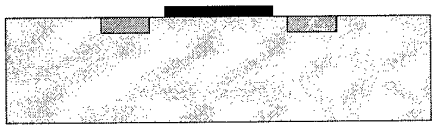
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Junction termination of Ni Schottky contacts on 4H SiC has been performed using floating guard ring structures. These structures are widely used in silicon technology as an effective means of planar edge termination. The major advantage of these structures is in the relative ease of fabrication compared to JTE techniques and the increased reliability over field plate designs.

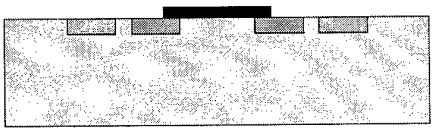
In order to determine the merits of guard ring structures four designs were fabricated. In each case the guard ring width is 20μm. Type 1 has the guard ring overlapping the edge of the Schottky contact by 5μm, whilst type 2 has a 5μm gap. Type 3 is equal to type 1, but with a subsequent 20μm ring, 5μm outside the first. Similarly, type 4 has one guard ring more than type 2. The structures are shown below.



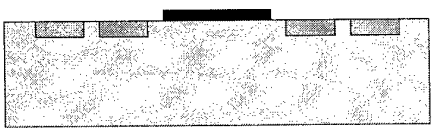
Type 1



Type 2



Type 3



Type 4

Commercial 4*H*-SiC n-n^+ epitaxial wafers from Cree Inc. were used to fabricate the diodes. The n layer had a donor concentration of $3\times10^{15}cm^{-3}$ and a thickness of 10μm. The samples were cleaned by degreasing with organic solvents followed by RCA procedure. Photo resist S1828 2μm in thick was used as a mask for ion implantation. Boron implants of energies up to 200keV and total dose $5\times10^{13}cm^{-2}$ were annealed under Ar flow in a RF furnace at 1600°C for 20 minutes. After annealing the samples were cleaned by an RCA procedure. All metal depositions were made by thermal evaporation at a base pressure of 8×10^{-6} Torr with no sample heating. Immediately prior to placing the samples in the vacuum chamber, they were immersed in 10% HF for 20 s at room temperature followed by blow drying. Nickel 100 nm thick was deposited on the back side of the wafer. Annealing of the back side contact was performed at 1100°C for 180 sec in vacuum chamber pumped down to 8×10^{-6} Torr. Nickel of 100 nm thick with titanium sub-layer (~5 nm) was deposited on epitaxial layer as a Schottky contact. After annealing at 420°C for 20 min, the geometry of the contacts was defined by contact UV lithography.

IV characteristics of the diodes were measured using an HP4155A semiconductor parameter analyser and breakdown tests performed using a Tektronix 371 curve tracer.

The ideality of the fabricated diodes was found to be weakly dependant on the diode type. This can be seen below.

Diode Type	Ideality
Unimplanted	1.04
Type 1	1.07
Type 2	1.10
Type 3	1.10
Type 4	1.07

The low ideality factor for the samples suggests that the surface quality under the Schottky contact is high. This is of importance for diode types 1 and 3 where the Schottky contact overlaps the implanted guard ring, with the associated surface roughness and implantation damage.

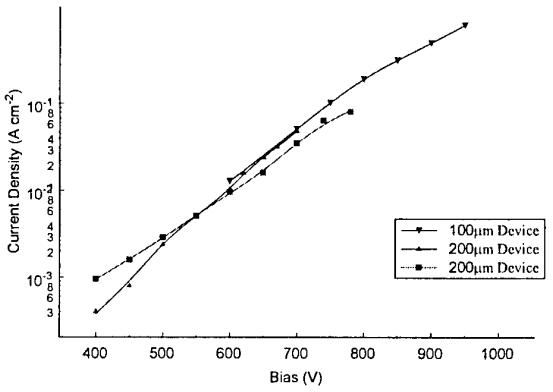
The breakdown voltage of the diodes fabricated on bare epitaxial material with no guard ring structures shows an average breakdown voltage of 451V. The breakdown voltage of diodes on the sample annealed at 1600°C is shown below.

Diode Type	Breakdown Voltage
1	783
2	631
3	912
4	764

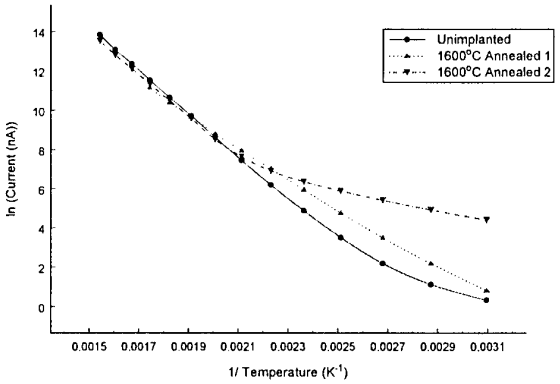
From this it can be seen that the addition of subsequent guard rings increases the average breakdown of the device (Type 3 c.f. Type1) by approximately 18%. This is consistent with other observations made in both silicon and SiC devices. The change in diode type from gapped structures (Types 2 & 4) to overlapped structures (Types 1 & 3) also sees an increase in breakdown voltage of approximately 22%. From this the double overlapped guard ring structure appears to be the most promising.

For the type 3 diode structures, the leakage current at high reverse bias is dependent on the contact area and not the termination circumference. This would suggest that the current is determined by the behaviour of the contact itself and not the guard ring structure.

The leakage current at –100V bias for a series of 200um diameter diodes has been



measured as a function of temperature. The unimplanted diode behaviour shows the effect of the intrinsic material properties on the temperature dependence. At low temperatures the guard ring structures dominate the leakage current, but as the temperature rises above 225°C the leakage current is independent of the termination, suggesting a common mechanism. This can be seen by the overlay of the data from both terminated and unterminated devices



Overlapped guard ring structures have been shown to give the greatest increase in breakdown, without adversely affecting forward characteristics or high temperature leakage. Further work will concentrate on establishing the mechanism responsible for the leakage current behaviour at high temperatures.

Minimization of Electric Field Enhancement at Electrode Edge by Surface High Resistive Layer in Ti/4H-SiC Schottky Barrier Diode

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SiC material has attracted much attention for high-power semiconductor devices because of high breakdown electric field. SiC Schottky barrier diode (SBD) is expected to decrease on-resistance and switching loss compared to Si pin diode. Hence, we fabricate Ti/4H-SiC SBD without any intentional edge termination. The measured breakdown voltage is equal to the value expected from breakdown field of SiC, and is evaluated by device simulation.

Wafers with structures of n-epitaxial layer on n-type substrate purchased from Cree were employed. N-type back contact was formed by Ni evaporation and rapid thermal annealing. Schottky electrode was formed by Ti sputtering on n-type 4H-SiC epitaxial layer with carrier concentration of $5x10^{15}$ cm^{-3} and thickness of 10 μm. As a pre-treatment before the Schottky electrode formation, $HCl+HNO_3$ and HF treatment was carried out. Devices with 100 or 500 μm diameter were fabricated by wet etching of Ti. The measured current-voltage (I-V) characteristics are shown in Fig. 1. Low on-resistance of 3 $m\Omega cm^2$, low leakage current of 10^{-5} A/cm^2 at 1000 V, and relatively high breakdown voltage of 1500 V are obtained. Schottky barrier height is evaluated to be 1.2 eV, shown in the figure. The barrier height is relatively high compared to the estimated value from workfunction of Ti, and close to the value estimated from hybrid orbital reference energy level for surface pinning [1]. Therefore, influence of thin surface high resistive layer, which brings surface pinning, is investigated.

I-V characteristics are investigated by device simulation with impact ionization coefficients reported by Konstantinov et al [2] and barrier tunneling effective mass of 0.66, which is effective density mass employed. Trap level of high-resistive layer is assumed to be acceptor type with activation energy of 0.5eV. In the same barrier heights, the forward rise-on voltage of devices with thin surface layer is calculated to be larger than that of device without thin surface layer. For devices without thin surface high resistive layer, the barrier height used for the calculation was 1.2 eV, which is equal to the measured value. In order to fit to the measured forward I-V characteristics, the barrier heights of devices with thin surface high resistive layer were set to 0.55-0.85 eV for calculation, depending on thickness and concentration of traps in thin surface high resistive layer.

The calculated results are also shown in the figure. The calculated breakdown voltage of one-dimensional (1D) device without thin surface high resistive layer is 1900 V,

which shows that the breakdown voltage of fabricated devices is 79 % of 1 D estimated value. Though the breakdown voltage of 2D device without thin surface layer is fairly low (below 50V, 1.5 % of 1D device), that of SBD with surface layer is calculated to be 40-85% of 1D devices, as shown in the figure. For higher trap concentration (1.5-2x10^{19} cm^{-3}), the electric field enhancement is minimized by the effect of thin surface layer and the breakdown is occurred by avalanche above 1200 V. Otherwise, the breakdown is occurred by Schottky barrier tunneling at the electrode edge near 700 V for lower trap concentration (1x10^{19} cm^{-3}). Hence, the breakdown voltage over 1200 V is brought by the minimization of the electric field enhancement at the Schottky electrode edge by the effect of thin surface high resistive layer. The origin of leakage current of SBD is considered to be Schottky barrier tunneling currents.

In summary, Ti/4H-SiC SBD without any intentional edge termination, with low on-resistance of 3 mΩcm^2, low leakage current of 10^{-5} A/cm^2 at 1000 V, and relatively high breakdown voltage of 1500 V, is fabricated. The relation between obtained breakdown voltage, Schottky barrier height, and thin surface layer is made clear. Influence of trap parameter on device properties will be also discussed.

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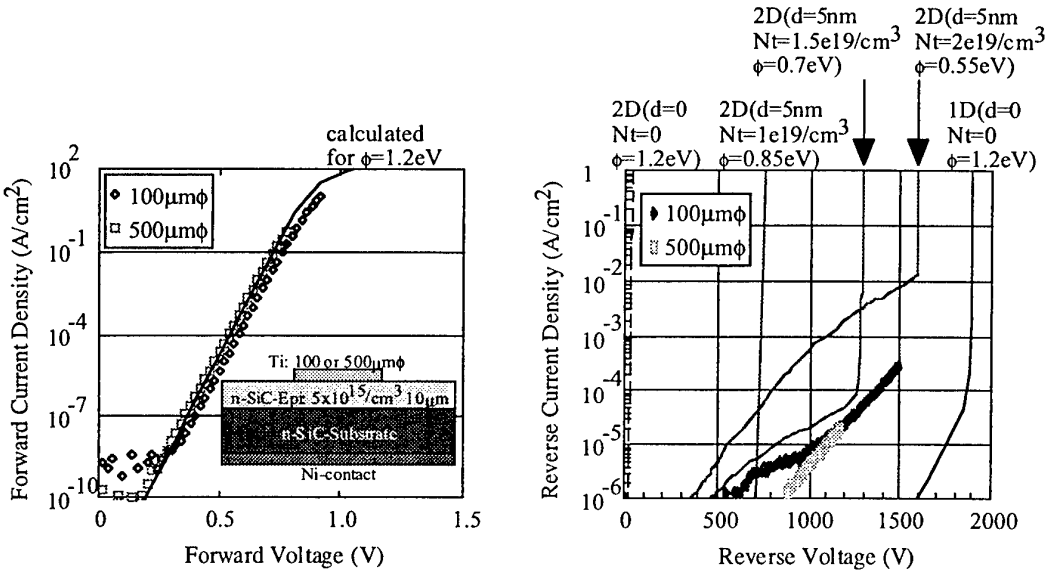


Fig. 1. Measured and simulated I-V characteristics of Ti/4H-SiC SBD.

Influence of epitaxial layer on SiC Schottky diode gas sensors operated in high temperature conditions

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Gas sensor devices operated under high temperature conditions have been investigated using catalytic metal-insulator-silicon carbide, MISiC, structures. The sensors have been tested for several industrial applications [1]. We have studied the influence of CO and O_2 in the ambient in terms of both gas response and device characteristics of the sensor devices [2]. Usually an epitaxial SiC layer grown on a low resistance SiC substrate is used for the sensor device. It is expected that the property of the epitaxial layer strongly affect the electrical characteristics of the diode. In this contribution, experimental results under high temperature conditions are discussed regarding the electrical properties, as well as gas sensing properties, of gas sensor Schottky diodes with different thickness and doping of the epitaxial layer.

The three types of diodes, which were compared, are described in Table 1. These diodes have different thickness and doping of the epitaxial layers, that are grown under different conditions [3-5]. The carrier density of the epitaxial layers was estimated from the capacitance-voltage characteristics. The devices have gate contacts of porous Pt, with an area of about 7.8×10^{-3} cm^2, and ohmic back contacts of $TaSi_x$ + Pt [1]. One Schottky diode was placed on a Pt disc in a quartz tube, and its top electrode was contacted by a Pt wire. The quartz tube chamber was placed in an oven. Forward and reverse current-voltage characteristics were measured in 4000 ppm O_2 in Ar and 8000 ppm CO in Ar, respectively, during steady state conditions at each investigated temperature, 22~600°C.

Figure 1 shows the temperature dependence of the series resistance calculated from the I-V characteristics in the high current region. The thickness and carrier density of the epitaxial layer mainly determines the value of the series resistance. For diodes of type.3, the resistance decreased, with a slope of about –1.5, with increasing temperature in the lower temperature region. This is suggested to be a result of the higher impurity concentration in the epitaxial layer of diodes type 3. The slope of about 1.5 in the higher temperature region suggests that here the resistance increases due to lattice scattering. The series resistance of diodes type 2 monotonously increased with increasing temperature. This means that the resistance is affected by lattice scattering. Further studies are needed to find the reason why the resistance of diodes type 1 has a maximum at about 670K.

In Fig. 2 the ideality factors are plotted versus the temperature. Diodes of type 1 have a higher value of the ideality factor than diodes type 2 and 3 at $T \leq 670K$. The value of the Schottky barrier height was evaluated for each diode from the temperature dependence of the I-V characteristics and was always about 1.5 eV. The change of the barrier height caused by a change from oxygen to carbon monoxide in the gas ambient was estimated from the forward and reverse current-voltage characteristics. The barrier height change was ≤ 0.3 eV and had a tendency to increase with increasing temperature for all three types of diodes, that is, the difference in epilayers did not seem to have an influence. The gas response of the devices is

measured as the voltage change at a constant current for a change in the gas ambient. The gas response for a change from oxygen to carbon monoxide in the ambient is higher for the type 1 diodes, above 0.5 V, than for diodes of type 2 and 3. Thus the difference in gas response may be connected to the value of the ideality factor, but not to the change in barrier height, since the latter is similar for the three devices.

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Table 1 Condition of three types diode with different epitaxial-layer.

No.	Thickness (μm)	Condition of epitaxial layer	Carrier concentration estimated by C-V method (cm^{-3})
1	10	Purchased from Cree [3]	$3.4x10^{15}$
2	24	Hot wall CVD epitaxy [4]	$8.1x10^{14}$
3	50	Sublimation epitaxy [5], Growth rate=100μm/h	$2.1x10^{16}$

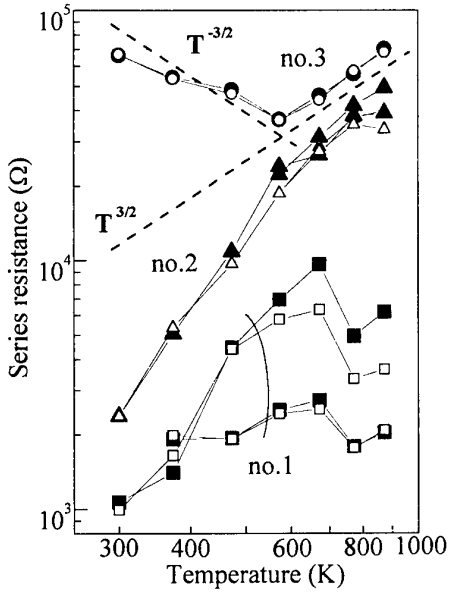


Fig. 1 The temperature dependence of the series resistance of the Schottky diodes in Table 1. A solid and open symbol represents O_2 and CO in the ambient, respectively.

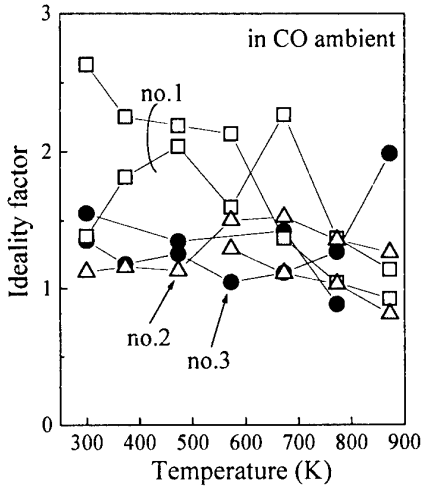


Fig. 2 Temperature dependence of the ideality factor for three types of diodes.

Performance of 4H-SiC Schottky Diodes with Al doped p-Guardring Junction Termination at Reverse Bias

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1 Introduction

In recent years, a large variety of promising SiC devices have been realised in the fields of high power, high temperature, and high frequency applications. In this work we especially concentrate in particular on 4H-SiC Schottky diodes which, due to their physical properties, have proven to show excellent performance for the realisation of fast switching applications with nearly negligible power loss [1]. High power switching implies the requirement of getting very low current at high reverse bias and very high current at low forward bias. SiC, with a critical field 10 times higher than Si, with a band gap of 2.5-3 times larger than that of Si, a thermal conductivity better than copper and large saturation velocities for electrons and holes offers these qualities for high power devices. Using numerical simulation, we investigated the principal mechanisms govering the device operation.

2 Device structure, surface conditions and simulation

Figure 1 shows a schematic view of the Schottky diode, featering a junction termination to avoid high electrical field peaks at the edges of the contacts, a boundary passivation and a highly doped field stop. In the simulations the Schottky diode was treated as a 2-dimensional structure. Experimental results [3] and [4] suggest, in view of the surface quality of SiC, surface charges may affect the device characteristics and, hence have to be considered in device simulation. As location of such surface charges we assumed the interface of the p-guardring and the boundary passivation and examined the effects on the reverse

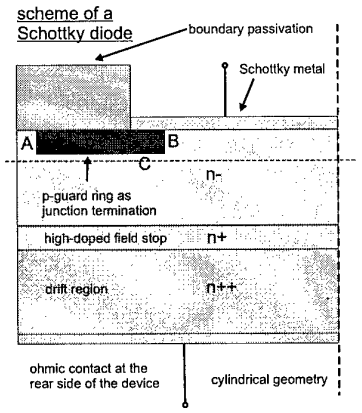


Figure 1: Cross section of the analysed structure

characteristics. The device analysis was performed using the multi-dimensional device simulator $Dessis_{ISE}$ which features a rigorous thermodynamic model of the device behavior based on the solution of the coupled system of Poisson's equation together with the electron continuity and hole continuity equations. The calculations assumed quasistationary conditions in reverse bias.

3 Simulation results

For varying Al doping of the p-guardring and without additional surface charges along the interface of the p-guardring and the boundary passivation our results show, in confirmity with former works [2], that different locations can be identified at which avalanche breakdown occurs. Low doping leads to critical field peaks at the outer edge (A) of the p-guardring, whereas at high doping concentration this point moves to the surface underneath the Schottky contact (B). The maximum breakdown voltage is observed if the region with maximum electric field is located at

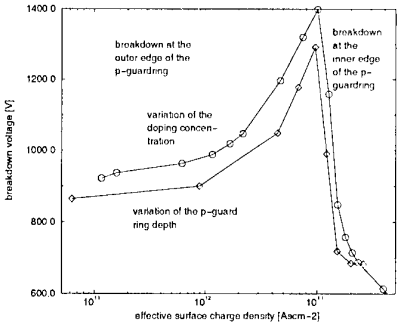


Figure 2: Breakdown voltage versus the surface charge

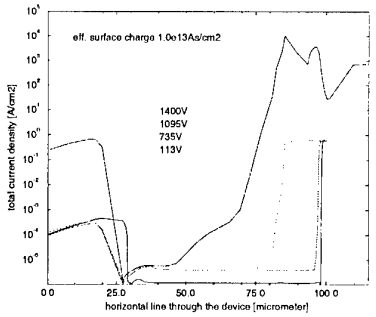


Figure 3: Total current density along a horizontal cut-line through the device

the inner edge of the p-implantation deep in the bulk (C). In this way the doping concentration of the p-guardring controls the breakdown voltage and determines the location where avalanche breakdown takes place (see Figs. 1 and 2).
Assuming a surface charge of $6.0 * 10^{12} As/cm^2$ along the interface of the p-guardring and the boundary passivation, the breakdown voltage is drastically reduced. As example for a Schottky diode with an effective surface charge at the p-guardring of $1.0 * 10^{13} As/cm^2$ and the same structure with an additional surface charge as mentioned above, the breakdown voltage is reduced from 1400V to 1095V. The device behavior under the influence of additional surface charges, was analysed in detail by studying the profile of the space charge, the total current density, the impact ionisation rate and the distribution of the electrical field. Comparing the respective total current densities shows that, for the assumed surface charges, the total current density at the outer edge of the p-guardring rises (see Figs. 3 and 4), while the impact ionisation rate shows equivalent behavior. The maxima of the electric field are located at the same points as they occur without additional surface charges.

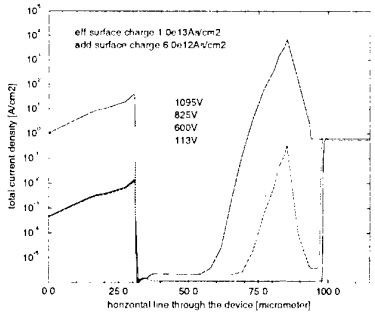


Figure 4: Total current density along a horizontal cut-line through the device

4 Conclusion

The effect of a p-guardring junction termination of Schottky diodes on its breakdown behavior has been discussed. The results of an earlier analysis [2] were corroborated and extended by studying in detail the spatial distribution of the total current density, the electric field and the impact ionisation rate, considering additional charges along the interface of the boundary passivation and the p-guardring.

5 Acknowledgements

We gratefully acknowledge the collaboration of R. Rupp and his group from Infineon Technologies. This study was sponsored by the German Ministry for Education and Research under the contract number 01BM903/1.

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Demonstration of 4H-SiC Avalanche Photodiode Linear Arrays

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Avalanche photodiode (APD) linear array is of great importance for spectroscopic and imaging applications. The demonstration of 4H-SiC APDs[1] makes 4H-SiC APD linear array possible. A high yield of APDs is the prerequisite for APD linear array demonstration. The control of the uniformity of breakdown voltage and the leakage current is also very critical. In this report, we present design, fabrication and characterization of 4H-SiC APD linear arrays.

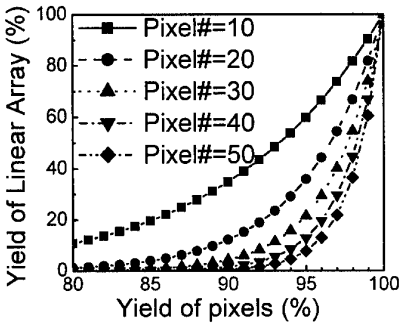


Fig.1: The yield of linear array with different pixel number as a function of the yield of pixels

The present SiC wafers are still very defective. Achieving high enough yield is therefore a very challenging issue. The pixel area has to be sacrificed to achieve a yield high enough for linear array demonstration. As shown in Fig.1, in order to have a substantial yield on an array with pixel number higher than 10, the yield of the pixels has to be higher than 90%. Since the density of the elementary screw dislocation, the major detrimental factor for an 4H-SiC APD, is typically in the range of 10^3-10^4/cm^2,[2] the pixel area should be smaller than $10^4\mu m^2$ so as to have a yield of pixels higher than 90%.

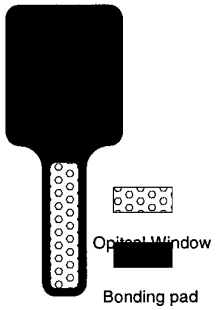


Fig.2: The top view of a pixel of 4H-SiC linear array.

4H-SiC APD linear arrays containing 40 pixels with the pixel area of $4.3\text{x}10^3\mu m^2$ are designed and fabricated. Figure 2 shows the top view of a pixel. The sizes of 4H-SiC APD mesa, their optical window, and wire-binding pad are 35x122, 84x19, and $80\text{x}100\mu m^2$, respectively. A $p^+pn^-nn^-n^+$ reach-through structure is used in our fabrication. The doping concentrations and thicknesses from p^+ to n^- are $3\text{x}10^{19}$/cm^3 and 0.2μm, $1.3\text{x}10^{18}$/cm^3 and 0.25μm, $5\text{x}10^{15}$/cm^3 and 0.22μm, $1\text{x}10^{18}$/cm^3 and 0.11μm, and $4\text{x}10^{15}$/cm^3 and 2μm, respectively. The targeted breakdown voltage is 116V. The substrate is n^+. Edges of APDs are terminated by 1.5μm deep mesa and passiviated by SiO_2.

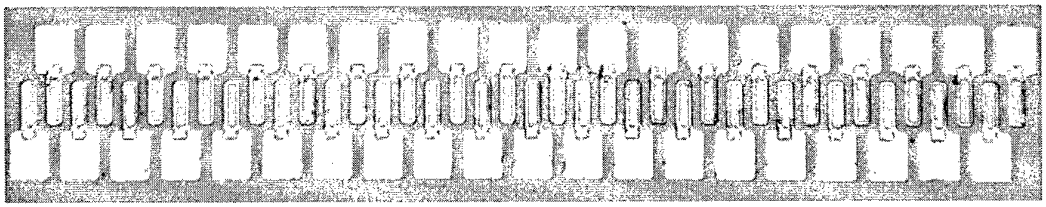


Fig.3: The top view of a fabricated 4H-SiC linear array with 40 pixels

Figure 3 shows a photo of a fabricated 4H-SiC linear array with 40 pixels. The period of pixels is 50μm and the total length of an array is 2mm.

The reverse I-V characteristics of pixels are tested and mapped. Fig.4 shows mapping of the breakdown voltage (V_B) and the leakage current at 120V (about 95% of V_B) for one of the best arrays. It can be seen that V_B is very uniform except for the 13th pixel. The average of V_B without the 13th pixel is 126.8V with a standard deviation of 0.9V. Most of pixels show a leakage

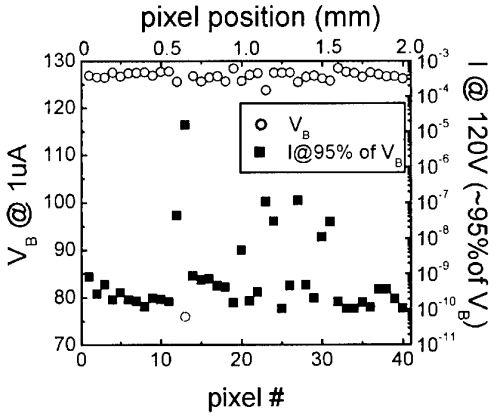


Fig.4: The V_B and the leakage current mapping of a 4H-SiC APD linear array

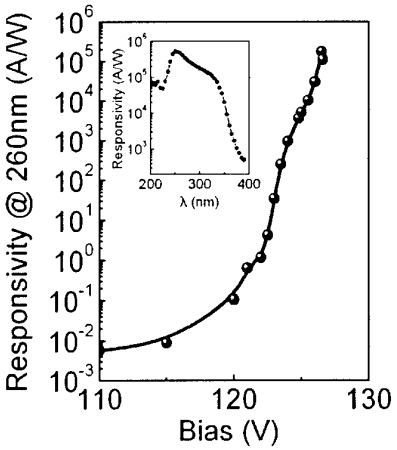


Fig.5: The peak responsivity as the function of reverse bias voltage. The inset is the response spectra at 126.5V.

current lower than 1nA at 95% of V_B. Compared with the high uniformity of V_B, the uniformity of the leakage current is lower. Still, mapping shows that pixels from 1 to 11 and 31 to 40 demonstrate uniform low leakage current at 95% of V_B. They can be packaged for APD linear array applications.

A total of 200 pixels have been tested. The accumulative yield of pixels with breakdown voltages higher than 116V is 91%. The limiting factor is believed to be the elementary screw dislocations. The yield of pixels with the leakage current lower than 1nA at 95% of V_B is 50%. The uniformity of leakage current is much poorer than that of V_B. The poor uniformity of leakage current is, therefore, the major barrier toward achieving 4H-SiC APD linear arrays containing more pixels. Experimental results show that leakage current is dominated by peripheral leakage current.

Figure 5 shows a typical peak responsivity of pixels as a function of the reverse bias. The inset is the response spectra at 126.5V. The peak of the response spectra is located at 260nm and the maximum achievable responsivity is higher than $1x10^5$A/W. Assume unity quantum efficiency, the corresponding optical gain is $4x10^5$A/W. The true optical gain should be higher because the APDs do not have unity quantum efficiency.

In summary, 4H-SiC APD linear arrays have been demonstrated. An array containing up to 11 pixels with a good uniformity of V_B and a low leakage current has been demonstrated for the first time.

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A New Type SiC Gas Sensor with a pn-Junction Structure

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1. Introduction

Silicon Carbide (SiC) devices are expected for use in high temperature environments under the high power and low loss conditions[1)]. In addition to these power devices, sensor applications such as ultraviolet sensitive diodes [2)] and gas sensors[3)] are other fields of targets for SiC devices. Basic device structures of gas sensors utilize catalytic gate Metal/Insulator/SiC substrate structures such as MIS-Schottky contacts, MIS-capasitors, and MISFETs. For the reliable operation of these devices, both metal contacts and intermediate thin insulator films have to stand high temperature gas environments. Present paper reports on a new and simple type gas sensors utilizing 6H-SiC pn-junction and ohmic contacts, which are operable at 500°C in gas ambient such as hydrogen and hydrocarbons. Present device structures are composed of catalytic metal layer/ohmic contact layer/SiC pn-junction/ohmic contact layer. In this device ohmic contact layers play roles for adhesion and barrier layer to the catalytic metal material. Device fabrication, contact stability at the elevated temperature and the device response to the gas components are discussed.

2. Experimental

PN-junctions were made with Al-doping with ion implantation (70~300keV, $2x10^{17}$~ $5x10^{19}$ Al/cm^3 in box profiles) or laser doping in n-type epitaxial layers ($1.8x10^{16}$ N/cm^3) on n-type bulk 6H-SiC substrates. After ion implantation the substrates were annealed in Ar flowing atmosphere at 1600 to 1650°C for 30 min. PtSi or PtSi/p^+-Si thin layers for ohmic contacts to p-type doped layer were deposited by laser ablation with an KrF excimer laser, and Ta metal layer were used for the n-type back contacts. Pt metal films 50 nm thick was sputter-deposited on the both ohmic contacts, which function as a catalytic layer and a cap layer to prevent from oxidation. Ohmic contacts on the thin-doped layer were fabricated with the laser processing technique to ensure a steep and shallow contact interface[4)]. I-V characteristics of the diodes were tested at 500°C in atmospheres of flowing test gas mixtures. At the constant current in the forward bias condition, test samples show voltage-sensitivity to hydrogen and hydrocarbons (typical example; C_3H_6) in concentration of 2 to 500 ppm contained in N_2 gas.

3. Results and Discussions

Figure 1 shows a device structure under investigation. A PtSi ohmic contact was made by irradiating the deposited PtSi film (~25nm thick) with a KrF excimer laser (energy density;2.5J/cm^2, numbers of pulses;1000). An additional PtSi film 75 nm thick was *in situ* deposited on the contact to ensure the ohmic property, to increase in adhesion of the Pt catalytic electrode, and to allow function as a barrier metal against Pt. A Ta film for the n-type back contact was deposited at 350°C with a DC-sputter method. Al ions were implanted at 100 keV with doses $1x10^{13}$ cm^{-2}, which correspond to an Al peak concentration of $1x10^{18}$ cm^{-3}. The projected range R_p of Al ions is estimated to be 120nm. In addition, $1x10^{13}$ Al/cm^2 were implanted at 30 keV ($3x10^{18}$ cm^{-3}) to decrease in the contact resistance.

Fig.2 shows I-V characteristics at 500°C both in the pure N_2 and the mixture of N_2 and H_2 (100 ppm) gas ambient. As shown in the figure, the voltage drop of the device slightly decreases at a constant forward current, which is dependent on the gas species and their contents. Three kinds of gas mixtures H_2/N_2, C_3H_6/N_2, and CO/N_2 were tested in the gas fraction ranging from 2 to 500 ppm. The sensor response is defined as the measured change in voltage at a constant forward current 20 mA as the gas is switched on from the pure N_2 gas to a test gas mixture. Fig.3 shows an example of the response at 500°C for the H_2/N_2 gas mixture containing 20 and 100 ppm H_2. The sensor response is smaller to C_3H_6 than to H_2, and is very weak to CO.

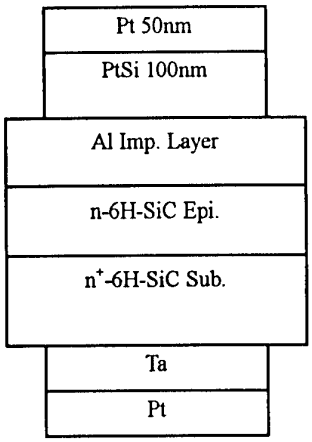


Fig.1 Device structure with a pn-junction and ohmic contacts. A top Pt layer functions as a catalytic electrode.

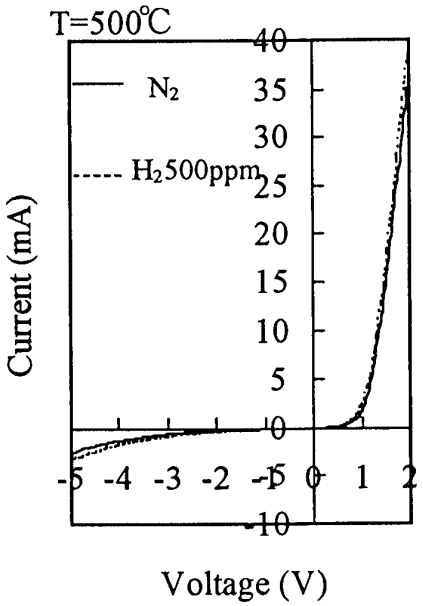


Fig.2 I-V characteristics of an Al-doped pn-junction sensor diode. The device temperature is monitored with a thermocouple attached to the sensor.

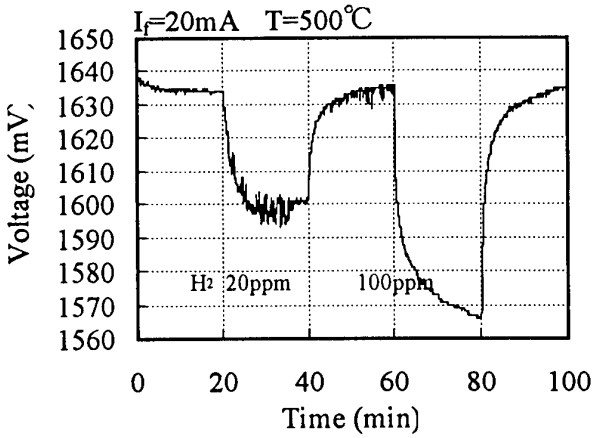


Fig.3 The sensor response to H_2 diluted in N_2 gas. The base voltage for the pure N_2 gas is stable within a few mV during measurements.

In conclusion, the present paper proposes a new gas sensor with a simple device structure. The sensor response time, sensitivity, and thermal stability are discussed in terms of the device structure, impurity profile, and electrode materials.

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N AND P TYPE 6H-SiC FILMS FOR THE CREATION DIODE AND TRIODE STRUCTURE OF NUCLEAR PARTICLE DETECTORS

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Recently, considerable progress has been made in the fabrication of high-quality single-crystal SiC substrates and epitaxial film [1]. The interest of nuclear physicists in SiC is due to the potentially high radiation and chemical hardness of SiC-devices and the possibility of their operation at elevated temperatures [2]. For detectors fabrication were used 6H- SiC films n- and p-type conductivity grown by vacuum sublimation epitaxy [3].
1.N-type epilayers (about d=10mkm thick, net doping concentration $|N^+_D-N^-_A| \sim 2.\ 10^{15}$ cm^{-3}) were used for Schottky diodes (barrier were formed by magnetron sputtering of Ni) producing. Diodes were irradiated with a 1 GeV proton beam extracted from the synchrocyclotron. The first doze is $\sim 3*10^{14}$ cm^{-2}. The overall dose of irradiation with relativistic protons was $1.3*10^{15}$ cm^{-2}.
The next detectors parameters were measured: charge collection efficiency (CCE) and energy resolution by alpha-spectrometry; width of the sensitive region (W_{eff}) and capacitance; diffusion length of holes (L_D); deep levels contents by DLTS method. It was shown that dose $(3\text{-}5)*10^{14}$ p/cm^2 corresponded the initial stage of the detectors degradation. The value L_D decrease up to 20-30%, but W_{eff}-voltage dependence remains unchanged. Under dose $\sim 10^{15}$ p/cm^2 high R-center concentration causes compensation conductivity of the base [4]. Also conditions of the charge carrier transport deteriorated. For realization CCE=1 3 times larger voltage (U) one must be applied.
2. *P-type films* ($d \approx 10$ μm, $N^-_A - N^+_D \sim 2{,}8.\ 10^{15}$ cm^{-3}) were used for fabrication triode n-p- n^+ - structure. Triode was realizing by grown of p –type epilayers on base of 6H n^+-SiC substrate.. The triodes were studied in a floating-base mode with alpha particles (5,8 MeV) coming in from the Schottky barrier side. The range of the alpha particles (20 mkm) exceeded the film thickness so that the nonequilibrium charge appearing in the base corresponded (with account of the Bragg ionization curve) to absorption of the energy E=2 MeV
Capacitance measurements demonstrated that the p-n^+ junctions of the structure are not identical. The Schottky barrier corresponds to an "abrupt" junction, whereas at the n^+ substrate the transition to the p-type conduction is gradual. Therefore, two connection polarities were tested, with either the p-n^+ -junction of the substrate or the Schottky barrier serving as collector.
In the last regime the E(U) dependence becomes superlinear. The signal corresponds to a value of about 60-80 MeV. The shape of the spectrum is Gaussian. So it was shown possibility of the ≈50 times amplification of nonequilibrium charge created by short-range ions.
To describe the effect quantitatively, the first place take into account that the structure under study is equivalent to a phototransistor. It is known that the primary current of the

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phototransistor is amplified in $(1-\alpha_T)^{-1}$ times, where α_T is the base-transport factor for electrons. In accordance with [5] we have for our case $\alpha_T = [(d-W)/L_D] / sh[(d-W)/L_D]$.

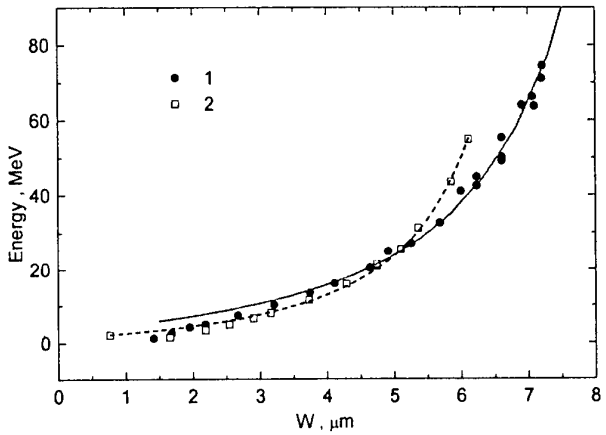


Fig. 1. Signal from alpha particle (in energy units) versus the width of the space charge region at the collector junction (Schottky barrier); fitting data: L_D = 8.85 and 5.85 (μm); film thickness d = 10.75 and 8.53 (μm) for samples 1 and 2, respectively.

Here W, and L_D are width of the space charge region at the collector junction and diffusion length of electrons, respectively.

Note that the signal as a function of the width region W (see Fig. 1.) is more convenient for approximating experimental data, with d and L_D used as parameters. The accuracy of fitting is characterized by the values d = 8.53±0.09 (μm) and $1/L_D$ = 0.171±0.005 (1/μm), obtained for sample 2.

In view of the high radiation hardness [6] and chemical resistance of SiC, structures of the above kind must be, in our opinion, of practical interest, e.g. for recording neutrons after their reactions with light elements, of the type ^{10}B (n, α) ^{7}Li, accompanied by alpha particle escape.

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An Effective High Voltage Termination for SiC Planar pn Junctions for Use in High Voltage Devices and UV Detectors

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We had previously proposed a simple planar edge termination based on a field plate overlapping an oxide ramp at the periphery of the contact. This technique which was successfully tested on SiC Schottky barrier diodes is for the first time extended to *pn* junction barrier diodes (JBDs). Extensive numerical simulations have been carried out to design an optimum SiC oxide ramp termination. We have also fabricated high voltage 6H-SiC *pn* junctions and UV detectors to verify the efficiency of this termination.

From Table 1 one can see that indifferent of the doping/thickness of the *n* epitaxial layer, a near ideal 1D parallel-plane breakdown is obtained as long as the slope of the oxide ramp remains below 5°. A insulating sandwich consisting of an undoped oxide layer and an 8% phosphorus doped oxide layer with a total thickness of 1 μm has been successfully used in the fabrication of planar implanted 6H-SiC *pn* diodes. Experimental measurements indicate that an angle of less than 3° was achieved using two step wet etching, first in a standard oxide etch solution and then an overetching in a P-etch solution. As predicted by numerical simulations this angle results in uniform spreading of the potential lines in the proximity of the junction (see Fig. 1). The oxide ramp termination is not limited to Schottky or *pn* junctions but can be used as a general termination technique in any high voltage SiC devices.

The termination is also highly suitable for photodetectors and charged particle detection. UV detection properties of epitaxial 6H-SiC JBD with oxide ramp termination are illustrated in Figs. 2-4. Similar behaviours have been observed on Schottky barrier structures with the same epilayer and termination. The photocurrent (J_{ph}) is almost flat (Fig. 2a) and responsivity (R) increases linearly (Fig. 2b) over the spectral range from 250 to 350 nm. The highest responsivity (over 200 mA/V) is obtained at 320nm, which corresponds to a quantum efficiency about 75%. The responsivity increases with the increase in the bias voltage up to 10V and also with the decrease in the doping of the *n* epilayer. A weak dependence of R with the epilayer thickness and with the increase in the reverse bias over 10V can be observed. Fig. 3 shows the variation of the total current of JBD ($J(K)$) and the photocurrent (J_{ph}) with temperature. As expected $J(K) = J_{ph}$ up to elevated temperatures where the dark current is two to seven orders of magnitude less than the photocurrent. At temperatures higher than 800K thermal generation is comparable with photogeneration and the contribution of J_{ph} at $J(K)$ decreases. Therefore, one can conclude that the JBD with oxide ramp termination can perform as an effective high performance UV detector up to 800K. Fig.4 shows the transient photoresponse of the JBD with oxide ramp termination. During the pulse light time the photocurrent increases exponentially. It subsequently decays exponentially when the recombination process becomes predominant (Fig. 4a). The transient time within the depletion region and the necessary time of the carriers generated in the neutral region to diffuse to junction result in a considerable time delay between the pulse end and the time at which the current reaches its maximum value. The difference between this maximum value and the photocurrent value which corresponds to the uniform illumination for reverse biases smaller than the punch-through reverse voltage, is due to photogeneration and recombination outside the depletion region (Fig. 4).

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Table 1. Breakdown voltage versus oxide ramp for several n epilayer parameters.

N_d/x_e ($cm^3/\mu m$)	Breakdown Voltage(V)			
	Ideal	Ramp 2°	Ramp 5°	Ramp 10°
$2x10^{15}cm^{-3}/25\mu m$	3700	3475	3275	2925
$2x10^{15}cm^{-3}/8\mu m$	1465	1460	1420	1350
$8.5x10^{15}cm^{-3}/8\mu m$	1335	1255	1195	1055

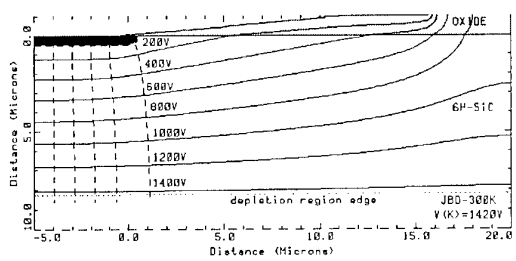
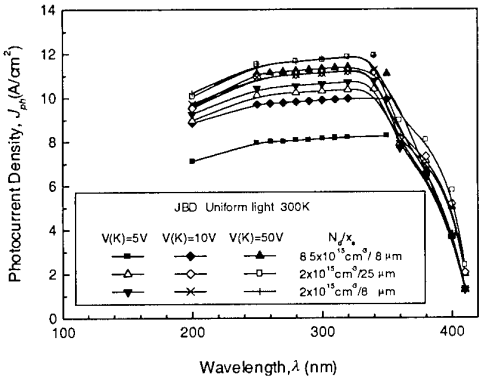
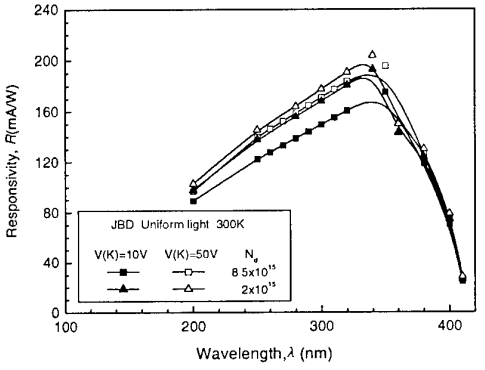


Fig. 1. The potential distribution at breakdown voltage of JBD with $N_d = 2x10^{15}$ cm^{-3} and $x_e=8\mu m$.



(a)



(b)

Fig. 2.(a)Photocurrent density and (b)spectral responsivity versus wavelength for several reverse biases of JBD with different n epilayer parameters. The incident photon flux is $10^{20}cm^{-2}.s^{-1}$

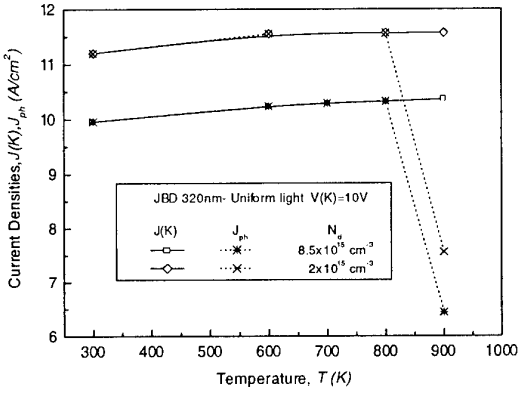
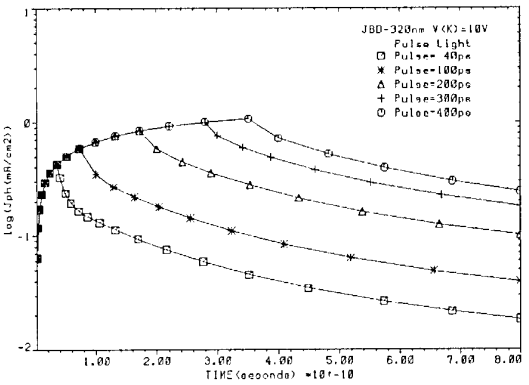
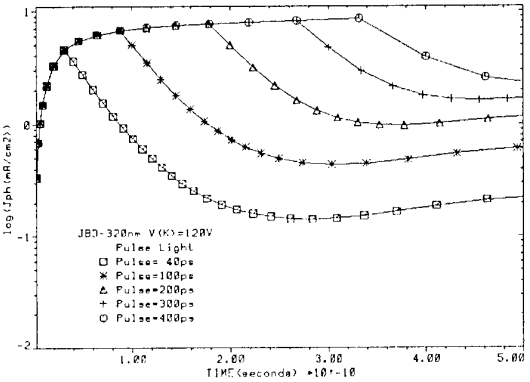


Fig. 3. Total current J(K) and photocurrent (J_{ph}) as a function of temperature for uniform illuminated JBD with an incident photon flux of 10^{20} $cm^{-2}.s^{-1}$, having λ=320nm.



(a)



(b)

Fig. 4. Photocurrent density response at different light pulse excitation (with λ=320 nm) of JBD reverse biased at: (a) 10V and (b) 120V (punch-through voltage).

TuA1 Technical Symposium



Technical Digest of Int'l Conf. on SiC and Related Materials –ICSCRM2001–, Tsukuba, Japan, 2001

TuA1-1
(Invited)

Application oriented unipolar SiC switching devices

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Following industries dreams of solid state power devices, an ideal switch with zero static and zero dynamic losses and a price close to electromechanics should be created with silicon carbide. Nice dreams, of course, this is not even visible at the horizon of ten years or more. However, this kind of thinking strongly influences the decisions whether silicon carbide has a successful future or is intended to end with glory. Thus, it is necessary to approach these demands as close as possible in order to get over the barrier existing for the introduction of a new and on a first glance much more expensive material concept.

Principally, there are two ways to do this. Firstly, one can look for an application were today's devices are not able to fulfill the requirements (e.g. high voltage, high current and high switching speed). In these fields, however, the margins are probably large, but the number of necessary devices is so small, that it becomes hard to find manufacturers which are willing to take over the investment for a fabrication since SiC despite its technological vicinity to silicon does not match to any existing production line. The second way is to look for applications with valuable system advantages and high volume. Also if these two items are often contrary, there seems to be a special kind of SMPS (Switch Mode Power Supplies) topologies which can probably serve similar to the PFC (Power Factor Corrector) as a driver for the introduction of SiC Schottky diodes as the entry for SiC switches into mass production. In such applications, low currents in the range of some amps and high switching speeds combined with blocking voltages above 1000V are recommended. Since in addition, the control power should be comparable to conventional devices like MOSFETs or IGBTs , the talk will outline that currently, the solution in silicon carbide represents a unipolar switch. In order to keep the costs as small as possible, the specific on-resistance must be as low as possible for small consumption of SiC area. However, thermal considerations must not be neglected at all since with smaller total device areas the thermal resistance increases.

In order to realize such a device, the first approach could be a MOSFET like structure. However, attempts to realize a powerful MOSFET in silicon carbide are still not successful due to interface and reliability problems which will be thoroughly discussed /1,3/. Bipolar devices with an non-even number of pn-junctions exhibit unacceptable high threshold voltages while the classical bipolar transistor (even with a current gain of 20) is not easy to control powerless and can't be paralleled easily. Thus, we currently favor the JFET concept in connection with a low voltage silicon power MOSFET presented as published earlier /2,4/. Up to now, we have two JFET configurations investigated, one type with extremely small on-resistance but limited switching speed and a second type with superior switching speed on the costs of a nearly doubled specific on-resistance. Figure 1 compares the turn-off for both devices as an indicator for the switching speed. As a good indicator for the dynamic performance serves the potential at the MOSFET drain during the transient phase. It can be seen that for the first type (left graph), the voltage at the MOSFET drain increases up to ist avalanche. This is due to an RC delay caused by the high p-type resistance in the buried p-layer. In the second type (right graph), the p-gate has everywhere an ohmic connection to the gate metallisation layer. Thus, the device is able to turn off very fast. In fact, the measurements show that for the second type the switching speed of the complete circuit is nearly independent on the JFET and can be influenced by a proper choice of the MOSFET. Possible future

structures with special respect to switching speed, overload behavior and still lower specific on-resistances will be discussed at the conference.

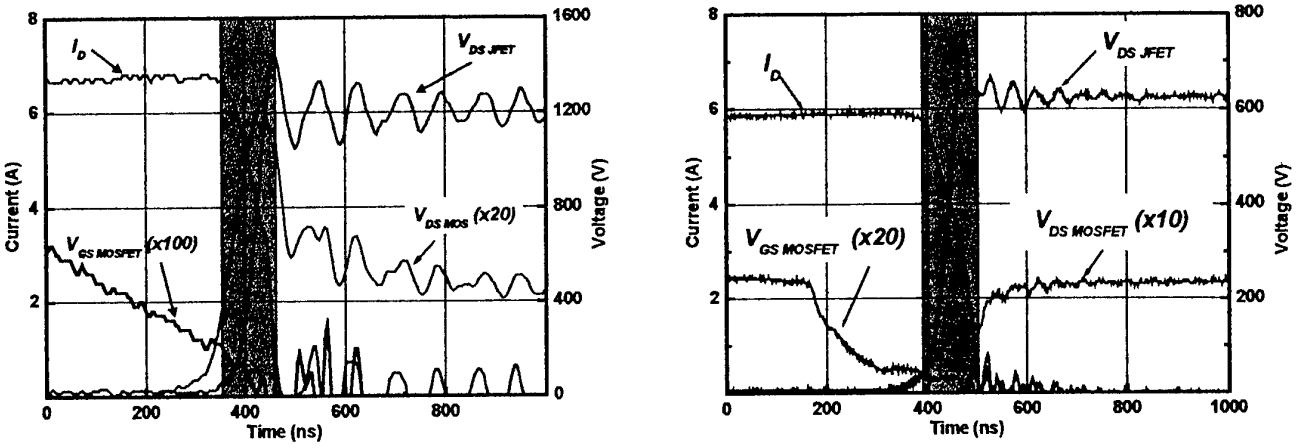


Figure 1: Turn off behavior of a Si MOSFET/ SiC JFETcascode with unsatisfactory dynamics (left) and the fast type (right), in a chopper circuit with clamped inductive load

A further item worth to discuss is the question what will follow such a device with broad application. Often high voltage applications with blocking voltages exceeding 3kV are mentioned. However, still open is the question of the upper limit for unipolar devices with respect to their blocking voltages. Recently, we have fabricated 3,5kV JFETs with a specific on-resistance of only 26mΩcm^2. We believe that these results will further shift the introduction of bipolar SiC-devices to blocking voltages of about 6,5kV or even higher since it now becomes possible to implement fast unipolar switches in high voltage applications. Additionally, with respect to bipolar SiC-devices, the problem of the poor p-type conductivity in epilayers as well as in the substrate is a hurdle hard to overcome in the near future. Thus, the unipolar SiC device concept will be most suited at least the next generations of silicon carbide power devices.

Acknowledgement

The author would like to thank all his co-workers at SiCED for their help and engagement in fabricating and analyzing the here presented devices as well as for the fruitful discussions of the results.

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High power SiC diodes: Characteristics, Reliability, and relation to material defects

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One of the most important device applications for SiC is for high power unipolar and bipolar devices. In this paper we present state-of-the-art results and performance of unipolar Junction Barrier Schottky (JBS) diodes intended for the voltage range of 600-3300V and for bipolar PiN diodes for the range between 3kV and 6 kV.

JBS diodes with 1200 V blocking voltage show a forward voltage drop of 1.25 V at 5.2 A (100A/cm^2) and 1.5V at 10A at 30°C. For 125°C, the voltage drop increases to 1.3 and 1.7 V, respectively. The diodes sustained surge currents of 2000A/cm^2 and show stable avalanche in reverse direction. Reliability tests of over 3000h for reverse bias and frequency operation proved stable parameter values for all diodes. The epitaxial design for the JBS diodes can be done for 80% critical electric field, while Schottky diodes have shown blocking voltages corresponding to only 70% of the theoretical junction field strength. This results for the JBS diode in a lower on-resistance than a Schottky diode on the same wafer despite the extra resistive contribution from the integrated p-grid (Fig. 1,2).

PiN bipolar diodes for 4.5kV using different anode technologies proved, that ideal on-state voltages of 3.1V at 100A/cm^2 can be achieved. Using a balance between epitaxial and implanted emitters, a speed-to-forward voltage trade-off can be implemented similar as in advanced Si devices. Using such chips (5mm edge length) power modules were assembled connecting 8 diodes in parallel. Switching tests for power ratings of about 1MW were made with 200ns turn-off operations of 300A against 3000V with 3800V peak voltage at the SiC diode. Blocking reliability of such diodes was also proven to be stable over > 5000h and unaffected by screw dislocations or other structural crystal defects. Other reliability functions such as frequency switching, surge current pulses, reverse avalanche stability as well as the cosmic ray failure rate testing, were executed according to power devices standards and did not show any concern (Fig. 3, 4).

However, bipolar SiC devices exhibit an increase of the conducting state characteristics called "forward degradation" (Fig. 5). An extremely wide statistic ranging from stable elements to such shifting their forward voltages more than 15V, during time spans of milli-seconds to kilo-hours are observed for nominally identical devices. The phenomenon was first observed by us. Since then have identified the cause as recombination-enhanced movement of dislocations, forming extended single stacking faults (SF) in the epitaxial layer. Electrically these SF decrease the carrier lifetime and create barriers for the current flow. The SFs are nucleated at dislocations present in the virgin material. Identification was carried out and densities were mapped over entire wafers. It is shown that at least some of the several different types of observed dislocations, including basal plane dislocations are actually present in the wafer substrate and cannot be eliminated at the substrate epi interface. Mature processing induces no additional faults in the epitaxial layer. However, continued material development must significantly reduce these dislocations, as well as the conventional crystal defects, before bipolar devices will achieve stable device operation.

Unipolar SiC devices for 300-2000V

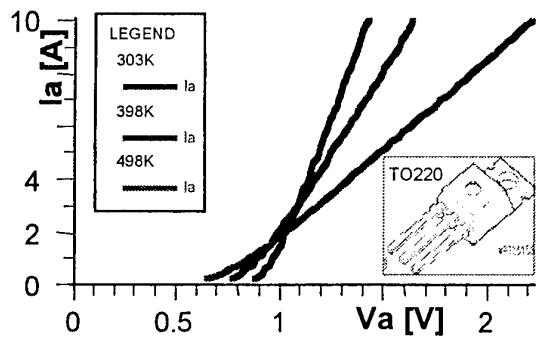


Figure 1 Measured forward characteristic of JBS diodes for 1200V for RT-225C. The device area is 5.2mm^2.

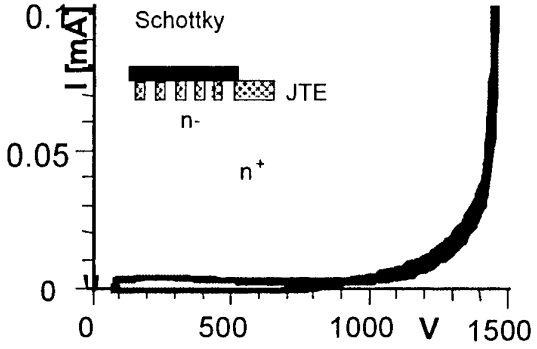


Figure 2 Reverse characteristic of the diode in Fig.1. The inset shows the diode cross-section with ca. 4um schottky spacing.

Bipolar SiC devices for over 3000V

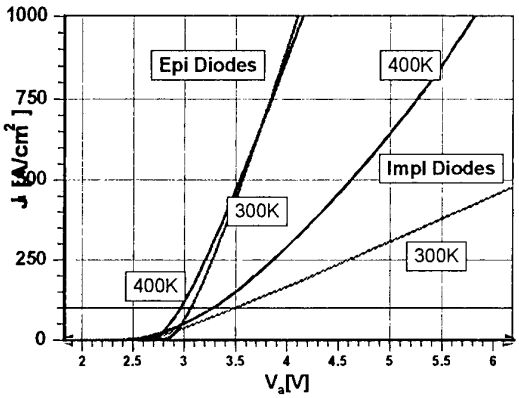


Figure 3 Measured on-state characteristic of bipolar diodes for 4.5kV with epitaxial and implanted anode emitter at RT and 400K. The device area is 2.5mm^2.

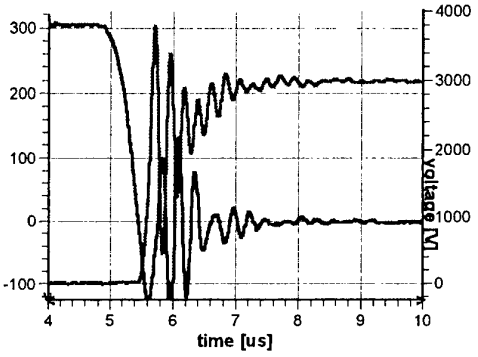


Figure 4 Switching characteristic at Tj=125C of a power module with 8 parallel 4.5kV diodes in a high power circuit. Turn-off at 300Amp, 3000Vdc shows only capacitive reverse recovery. The ringing is due to the very fast transient and circuit/device capacitances.

Dislocations causing the bipolar forward instability in SiC

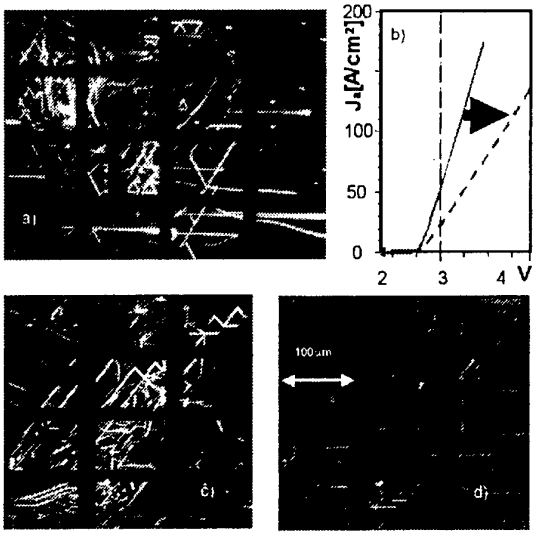


Figure 5 The pictures a), c) show electrically active dislocation maps of virgin epi layers. Dislocation motion creates stacking-faults causing the forward voltage to increase b). In d) the identical area as in c) shows the bounding partial dislocations of the created SF after forward current operation.

defect type	typical dens.	device effect
Micropipes	1-30cm^{-2}	<50 - 70% E_{cr}
Carrots	0.1-10cm^{-2}	E_{cr}, J_L, n
Major pits	1-100cm^{-2}	-, E_{cr}, J_L
Screw disloc.	10^3cm^{-2}	< 80%E_{cr}, τ_{HL}
Edge dislocations	10^4-10^5cm^{-2}	not known
Basal plane disloc.	10^1-10^5cm^{-2}	nucleate ext. SF
Misfit disloc.	0 - 10^3cm^{-2}	nucleate ext. SF
inital small StackFlt	0 - 10^5cm^{-2}	nucleate ext. SF
ingrown StackFault	0 in soa epi	high V_F
Low angle grain boundaries	10^2-10^3cm^{-2}	τ-reduction, forward char.
threading dislocs.	few cm^{-2}	not known
extended stacking faults	0-10^6cm^{-2}	high forward voltage

Table 1 Most common defects in 4H SiC, typical density, and effects on power device characteristics.

Low resistivity ohmic contacts sequentially formed in n- and p-type regions on the same 4H-SiC substrate

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1. Introduction

A widely used technique to form low resistivity ohmic contacts on SiC is to deposit electrode materials such as Ni for the n-type region and layered or alloyed Al/Ti for the p-type region, followed by post-deposition annealing (PDA), typically at 800℃-1000℃ [1]. However, this technique, as is well known, has various drawbacks. PDA causes electrode materials to penetrate the thin n^+ or p^+ layer, to spill over or to attack the field oxide, and markedly degrades electrode surface morphology. This paper proposes an ohmic contact structure and fabrication process that can overcome these issues and are applicable to the manufacture of practical devices, such as JFETs and MOSFETs. It is also shown that specific contact resistances in the range of 10^{-7} Ωcm^2 and $10^{-6}\Omega cm^2$ can be obtained in the n-type and p-type regions, respectively, on (0001) 4H-SiC substrates.

2. Contact Structure and Fabrication Process

Figure 1(i) shows a cross-sectional view of one of the proposed contact, where two different contacts are formed in the source and the gate on a vertical channel 4H-SiC JFET [2] as a example. The major structural features of these contacts are: they are formed on heavily doped n^+/p^+ regions leading to field emission conduction; the contact materials are thin Ni for the source and layered Ti/Al for the gate (the notation Ti/Al means Ti deposition followed by Al deposition); both the contact materials are defined just in the contact windows leaving a constant and fine clearance to the field oxide; and this field oxide consists of a thin thermal oxide and a thick CVD oxide.

Figure 1 outlines the fabrication process of the contact structure. (a) Using selective-area multiple-energy ion-implantation and impurity-activation annealing, the p and p^+ gate regions and the n^+ source region are formed on a vicinal (0001) n^+ 4H-SiC substrate with a lightly N-doped epitaxial layer. (b) The field oxide is grown on the surface by thermal oxidation and atmospheric pressure CVD. (c) Then, contact window is opened in the field oxide over the p^+ gate region by photolithography using a buffered hydrofluoric solution and (d) 80-nm-thick Ti and about 350-nm-thick Al are successively deposited by electron beam evaporation on the surface which still has the photoresist. (e)When the photoresist is lifted off, the well-defined Ti/Al is left on the the bottom of the gate-contact window. (f) In the same manner, 50-nm-thick Ni is defined on the bottom of the source-contact window. (g) Then, after 50-nm-thick Ni is deposited on the back side of the substrate, (h) all the contacts are simultaneously annealed at 1000℃ for 2 min in Ar by rapid thermal annealing. (g) Finally a thick metal over-layer such as Al is deposited on the surface by DC magnetron sputtering and patterned by photolithography using RIE.

3.Results

Ni and Ti/Al contact test structures with the linear transmission line model configuration were fabricated in the heavily N- and Al-doped regions, respectively, on a vicinal (0001) 4H-SiC epitaxial substrate. TLM analysis indicated, as is shown in Fig. 2, that these alloyed contacts had low specific contact resistances of typically 3.3×10^{-7} Ωcm^2 for n-type SiC/Ni and 9.5×10^{-7} Ω

cm^2 for p-type SiC/Ti/Al at room temperature. A 30-min annealing test from 50℃ to 500℃ in 50℃ increments revealed that a significant increase in contact resistance did not occur for either type of contact.

Acknowledgements

This work was performed under the direction of FED as part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by The New Energy Development Organization (NEDO).

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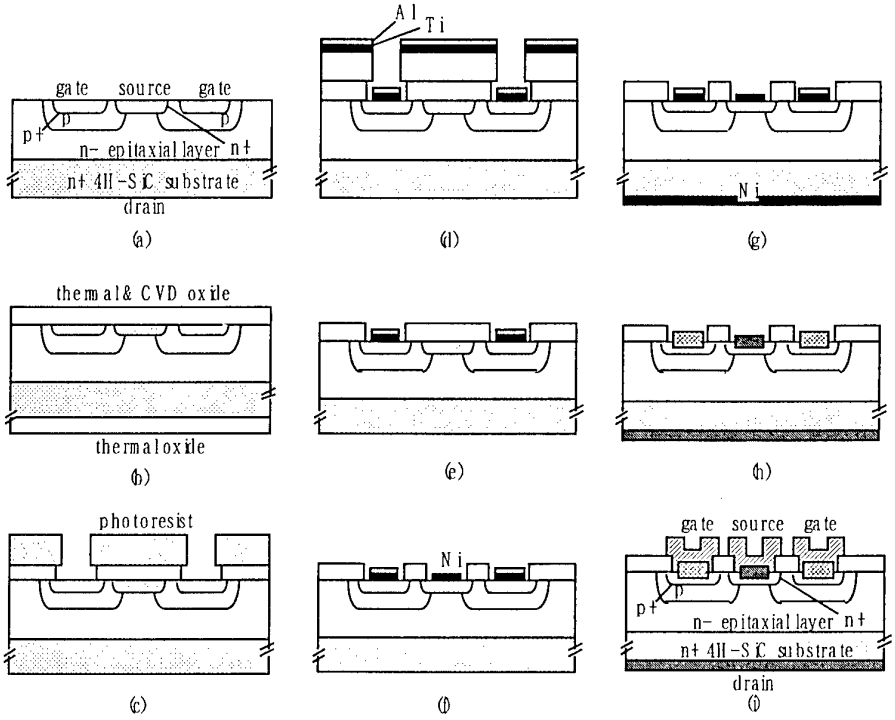


Fig. 1 A fabrication process of proposed contacts combined with JFET structure

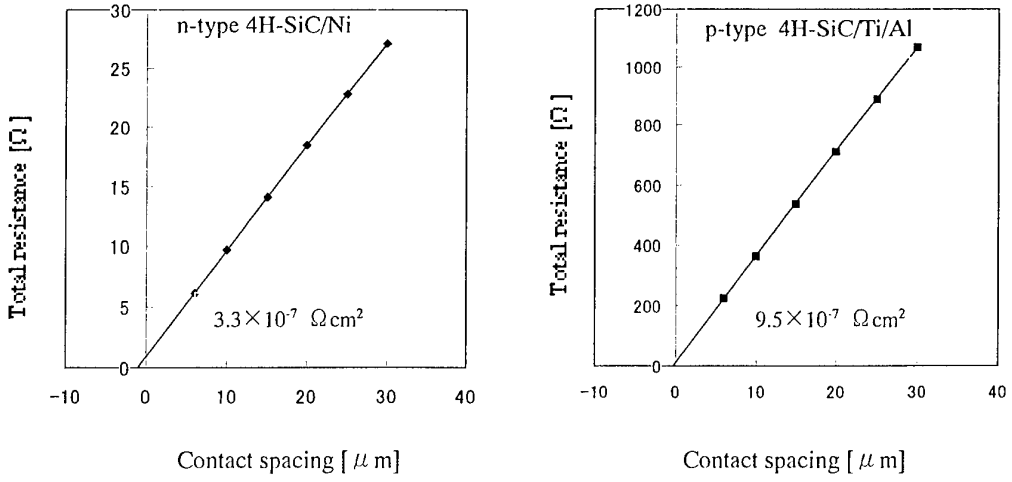


Fig. 2 Plots of total resistance of as a function of contact spacing

TuA2 Special Symposium



Passivation of the 4H-SiC / SiO_2 Interface with Nitric Oxide

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Silicon carbide material properties such as high breakdown field strength (x10 Si), high saturated electron drift velocity (~ x2 Si) and excellent thermal conductivity (~ x2.5 Si) make this wide band gap semiconductor a promising material for high power devices. Silicon carbide is also the only wide band gap semiconductor that has a native oxide. The same thermal techniques that are used to grow oxide layers on Si can be used to oxidize SiC – the one difference being that normal oxidation temperatures are higher for SiC by 200-300°C.

Bulk electron mobility is higher for 4H-SiC than for the 6H-polytype (~ 900cm^2/V-s compared to about 450cm^2/V-s), and hence 4H-SiC is the polytype of choice for power MOSFET fabrication. However, the problems of surface roughness produced by ion implantation / activation prior to oxidation and a high interface state density near the conduction band edge following oxidation [1] have hindered the development of *n*-channel, inversion-mode 4H-SiC MOSFETs. Much attention has been focused on improving the performance of these devices – particularly with regard to the characterization and passivation of the interface states near the conduction band edge $D_{it}(E_c)$ [2-4]. Efforts have included the use of deposited oxides [5], low dose ion implantation in the channel region [6] and oxide growth on the "a-face" of 4H-SiC [7]. Herein, we describe an interface state passivation process based on post-oxidation, high temperature anneals in nitric oxide [8]. This process reduces $D_{it}(E_c)$ by an order of magnitude (Fig. 1) and increases the effective channel mobility for *n*-channel MOSFETs from single digits to ≅ 30cm^2/V-s and higher, as shown in Figure 2 and as reported in other papers at this conference [10,11]. The temperature dependencies of the effective channel mobility and the threshold voltage are shown in Figures 3 and 4 for lateral 4H-MOSFETs passivated with nitric oxide. The results for channel mobility may be compared with results reported by others for unpassivated devices fabricated with standard 4H-SiC [12-13] and for devices fabricated with oxide layers that were grown on the 4H-SiC a-face [7]. Unpassivated, standard devices exhibit increasing field effect mobility with increasing temperature, while the low field mobility for a-face MOSFETs decreases with increasing temperature. In Figures 3 and 4, the observed trends for both devices (passivated and unpassivated) are consistent with the thermal liberation of electrons trapped near the conduction band edge. Mobility increases as the result of reduced Coulomb scattering, and V_{th} decreases because there is less negative charge at the oxide-semiconductor interface.

Details of the NO passivation process will be discussed. Other papers to be presented at this conference [10,11] show that the process is compatible with additional processing steps that are required for SiC MOSFET fabrication – e.g., *p*-well implantation and source / drain contact annealing. The NO passivation technique is the first process that significantly improves the channel mobility of devices fabricated using standard 4H-SiC. However, after passivation, $D_{it}(E_c)$ remains approximately 100 times higher for SiC compared to Si. This is an indication that work must continue to further improve the 4H-SiC / SiO_2 interface.

This work was supported by DARPA Contract MDA972 98-1-0007, EPRI Contract W0806905, ONR Contract N000140110616, and at Oak Ridge National Laboratory by DOE Contract DE-AC05-00OR22725.

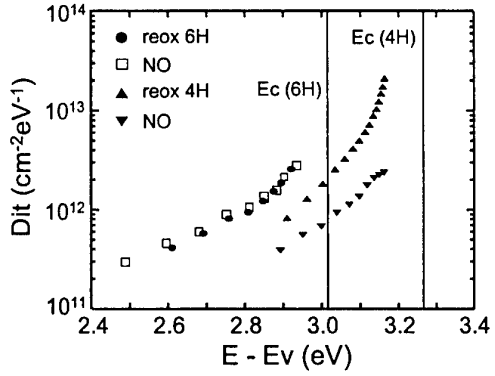


Fig. 1. Effect of NO passivation on *n*-4H-SiC.

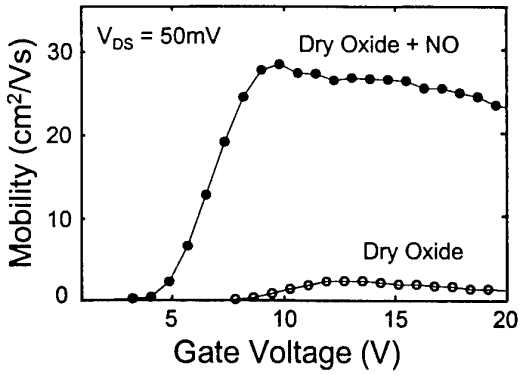


Fig. 2. Channel mobility for lateral 4H-SiC MOSFETs.

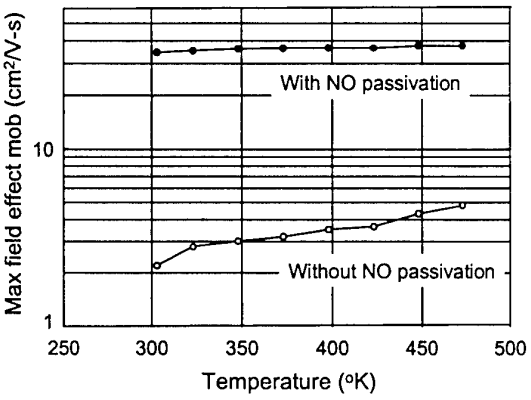


Fig. 3. Temperature dependence of the effective channel mobility for lateral 4H-SiC MOSFETs.

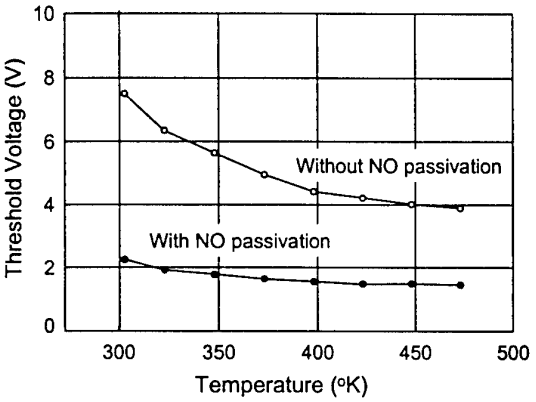


Fig. 4. 4H-SiC MOSFET threshold voltage as a function of temperature.

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Recent Achievements and Future Challenges in SiC Homoepitaxial Growth

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Introduction

SiC homoepitaxial growth has been a key technology to fabricate high-performance SiC device structures. Major requirements for SiC epitaxy include good morphology, high purity, low defect density, wide-range and abrupt doping control, thickness and doping uniformity, and high growth rate. Although SiC growth technology is becoming mature to fulfill most of these demands in a 2~3 inch wafer level, further improvements and understanding of growth itself such as doping and defect generation mechanisms are required. In this paper, the authors present three topics of SiC epitaxy: growth of high-purity SiC, fast epitaxy, and a proposal of a new crystal face. Remaining issues in SiC epitaxy are also discussed.

Growth of high-purity SiC

High-purity and thick 4H-SiC(0001) epilayers have been grown by a horizontal hot-wall CVD system, which was designed and built at the authors' group. Typical flow rates of SiH_4, C_3H_8, and H_2 were 1.5 sccm, 0.75 sccm, and 5~10 slm, respectively. Most growth runs were carried out at 1550 °C and at reduced pressure, by which a growth rate of 5 μm/h was obtained. Figure 1 shows the donor concentration of unintentionally doped epilayers vs. the reactor pressure during CVD. The donor concentration showed significant decrease by reducing the pressure. Preliminary experiments on intentional nitrogen doping have also indicated that the doping efficiency of nitrogen is suppressed at low pressure. A probable reason for this effect might be the enhanced desorption of nitrogen from a growing surface at reduced pressure, but more complicated surface kinetics should be involved. In the present system, the reproducible donor concentration is $1\sim3\times10^{13}$ cm^{-3} in CVD at 80 Torr. Free exciton peaks dominated in low- and room-temperature photoluminescence spectra without Ti or point-defect related peaks. The electron mobility reaches 981 cm^2/Vs at 290 K and 46,200 cm^2/Vs at 42 K. The total trap concentration could be reduced to as low as 4.7×10^{11} cm^{-3} by increasing the input C/Si ratio.

Fast epitaxy of high-quality SiC

Fast epitaxial growth of SiC has been realized by chimney-type vertical hot-wall CVD, also designed at the authors' group. High-temperature growth at 1700 °C enables higher precursor flow rates and thereby a higher growth rate, keeping a specular surface. Typical growth was performed at 100 Torr in a SiH_4-C_3H_8-H_2 system. Figure 2 represents the C/Si ratio dependence of growth rate, donor concentration, and deep trap concentration of undoped 4H-SiC(0001) epilayers. The lowest background doping level is 1×10^{14} cm^{-3} (n-type) or less. By increasing the C/Si ratio, the trap concentration, the Z_1 center being dominant, was reduced to 5×10^{12} cm^{-3}, in spite of a high growth rate of 25 μm/h. The authors have fabricated high-voltage (> 3 kV) implanted pin diodes using these epilayers. We will present characterization of more than 100 μm-thick epilayers by various techniques [1].

Epitaxial growth on new faces: 4H-SiC(11$\bar{2}$0) and (03$\bar{3}$8)

Micropipes and low MOS inversion channel mobility have been recognized as the most severe obstacles to realize high-current and low-loss SiC power MOSFETs. At ICSCRM'99, the authors presented successful homoepitaxy of 4H-SiC(11$\bar{2}$0) and greatly improved performance

of 4H-SiC MOSFETs. In this conference, we propose a novel crystal face: 4H-SiC(03$\bar{3}$8). 4H-SiC(03$\bar{3}$8) is the face inclined by 54.74° toward <01$\bar{1}$0> from (0001), and is semi-equivalent to 3C-SiC(001), as illustrated in Fig.3. 4H-SiC(03$\bar{3}$8) wafers were prepared by slicing ingots grown at SiXON [2]. Homoepitaxial growth on this face has been carried out by both cold-wall and hot-wall CVD reactors. As in the 4H-SiC(11$\bar{2}$0) growth, homoepitaxial layers with a very flat surface can be obtained on 4H-SiC(03$\bar{3}$8) without intentional off angle, as shown in Fig.4. Formation of macrosteps and triangular defects has never been observed. The doping efficiency of nitrogen on this face is slightly higher than on (0001), but a low background doping concentration of 3×10^{14} cm^{-3} (n-type) can be achieved. Successful homoepitaxy, the possible availability of micropipe-free wafers, and low interface state density in MOS structure [3] make this face an attractive alternative for high-power SiC devices.

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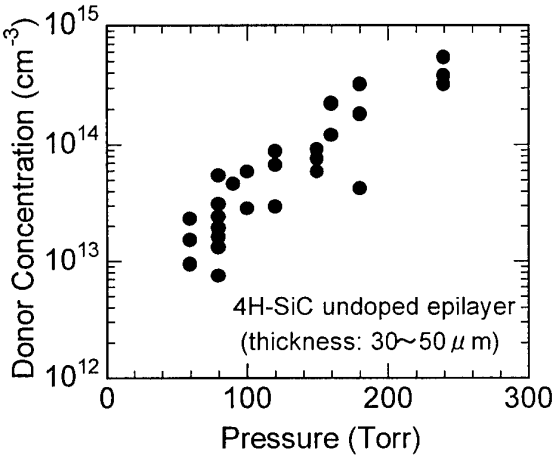


Fig.1 Pressure dependence of donor concentration for unintentionally doped 4H-SiC(0001) epilayers. (horizontal hot-wall CVD)

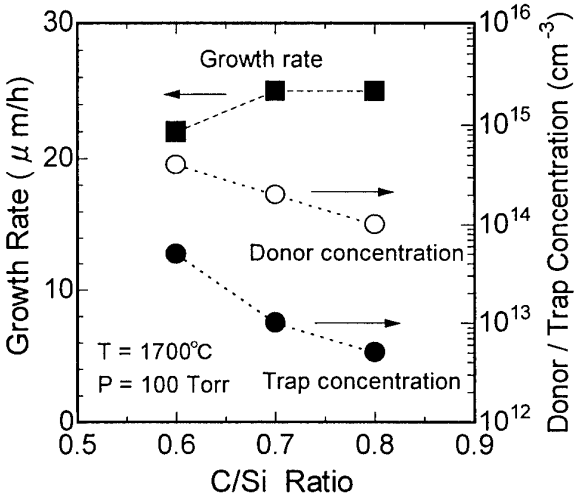


Fig.2 C/Si ratio dependence of growth rate, doping level, and trap concentration of 4H-SiC(0001) epilayers. (chimney-type vertical hot-wall CVD)

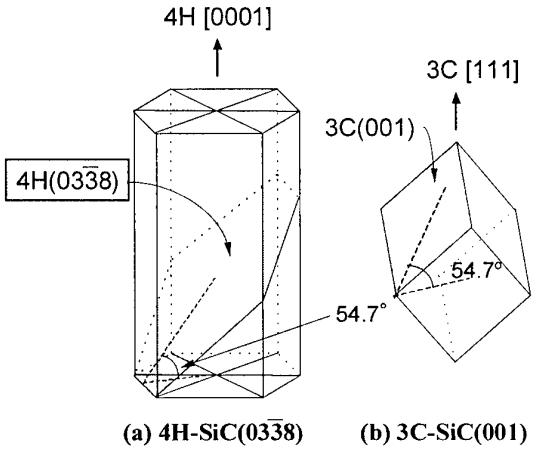


Fig.3 Illustration of 4H-SiC(03$\bar{3}$8) and 3C-SiC(001).

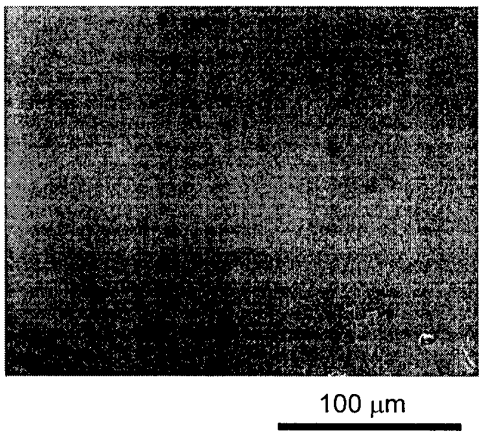


Fig.4 Typical surface morphology of a 4H-SiC(03$\bar{3}$8) epilayer.

HIGH QUALITY SIC SUBSTRATES FOR SEMICONDUCTOR DEVICES: FROM RESEARCH TO INDUSTRIAL PRODUCTION

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The production of large diameter, high quality SiC substrates is essential to realize the full potential of this important semiconductor material. Within the last several years SiC bulk sublimation growth has matured from a research state to a volume process for the production of these substrates. The current state of the art of SiC sublimation growth is reviewed from an industrial point of view. Specific efforts towards larger diameter high quality substrates have led to the production of 50 mm and 75 mm diameter 4H and 6H wafers, which are now commercially available and the demonstration of high quality 100 mm wafers. In SiC, micropipes remain the most critical defects for SiC device production. The unique properties of these defects are characterized by etching and x-ray white beam topography. Results at Cree have allowed us to steadily decrease the micropipe density both in our best R&D results and average production values over the past several years. The analysis of KOH-etched SiC wafers from low micropipe density boules has determined micropipe-free 4H-N material on a diameter of 25 mm, densities as low as 0.9 cm^{-2} for an entire 50 mm 4H-N wafer, and 8 cm^{-2} for a 6H-N 75 mm wafer. For further defect reduction in SiC substrates of increasing diameter, continued refinement of our understanding of the growth process is essential. We will summarize results of modeling the growth process, focussing on the thermoelastic stress in the growing crystal and the effect on dislocation formation. Recent R&D progress at Cree has resulted in the seeded sublimation growth of high purity 4H SiC bulk crystals of 50 mm and 75 mm diameter exhibiting semi-insulating behavior without resorting to the intentional introduction of deep level elemental dopants, such as vanadium. Additionally, these crystals exhibit micropipe densities in the range of 10 - 150 cm^{-2} on a 50 mm diameter. Based on high temperature Hall-effect measurements, the semi-insulating behavior is characterized by a range of activation energies from 0.9 to 1.6 eV. The absence of vanadium was confirmed by SIMS measurements, optical absorption, and EPR spectra of this new material. Correlation of EPR signatures with intrinsic deep level defects will be presented. We present thermal conductivity data for this new high resistivity material and compare it to values of materials of different doping levels. The corresponding doping and temperature dependencies and the relevance for device applications are discussed.

This work was partially supported by the Air Force Research Laboratories, the Office of Naval Research, and BMDO.

Growth and Defect Reduction of Bulk SiC Crystals

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Silicon carbide (SiC) is a wide band gap material with a well-recognized potential for high-power, high-temperature electronics. The fundamental material parameters of SiC are very attractive for the fabrication of semiconductor devices with superior characteristics for high current and high voltage devices. The unique physical properties of SiC include a large energy bandgap, high thermal conductivity and high breakdown electric field. Because of their fundamental material parameters, SiC devices have been predicted to have a higher breakdown voltage (at the same doping level) and to operate at a higher forward current density than Si devices. Recently, because of significant progress in SiC technology, these predictions have become a reality. However, the commercialization of SiC devices is still not fully achieved, and factors limiting the commercialization are largely related to the material quality of available SiC crystals.

In this paper, we discuss the bulk crystal growth of SiC single crystals by highlighting recent advances in crystal diameter enlargement and improvements in crystal quality.

Seeded sublimation growth, also known as physical vapor transport (PVT) growth, has been the most successful method to date for growing large SiC single crystals. In this method, an SiC source powder in a semi-closed crucible is sublimated and recrystallized on a seed crystal maintained at a slightly lower temperature. Although the sublimation technique is relatively easy to implement, having in mind that extremely high temperatures (over 2300°C) are needed, the process is difficult to control, particularly over large seed crystal area. Although significant progress has been made in the growth of SiC crystals, the growth processes governing the polytype control and the defect formation are still poorly understood.

Increasing the wafer diameter is crucial for reducing the cost of SiC devices through economies of scale and the use of Si or GaAs device fabrication lines. In this respect, much effort has been made over the last decade, leading to the recent fabrication of fully single crystal wafers with a diameter of up to 100mm [1]. The crystal quality, however, is generally largely degraded as the crystal diameter increases. This is due to the lack of an established methodology for expanding the single crystal area without degrading crystal quality. To achieve this, a high degree of control of both the transient and continuous thermal profiles during growth is required. We utilized the results of numerical simulation of the temperature profiles inside the crucible, taking into account heat transfer through conductive and radiative mechanisms, and then the results were combined with our compiled experimental database to figure out the key growth parameters for SiC crystal growth. This approach successfully allowed for diameter enlargement of up to three inches in our laboratories.

The most harmful defect in SiC bulk crystals is the so-called "micropipes" which are small pinhole defects that penetrate the entire crystal and cause critical flaws in SiC devices. We have recently proposed a surface step model for the micropipe formation in SiC crystals, taking into account several important aspects experimentally observed for micropipe formation [2]. Micropipes are very often observed at the foreign polytype and secondary phase inclusions during growth, where high density screw dislocations are introduced and the

spiral steps emanating from them interact with each other. The model assumes that the strong repulsive interaction between these steps [3] coalesce the unit *c* screw dislocations through the energetic bunching of the spiral steps. Spiral growth mechanism ensures stable lateral advancement of steps of multiple unit cell height, which kinetically prevents the dissociation of the bunched steps and thus prevents micropipes.

The presence of low angle grain boundaries and associated mosaicity in SiC crystals is also commonly observed, and they are fully replicated from the substrates into the device epitaxial layers by the thin film growth process and consequently have a major impact on the performance of SiC devices made on them. We have recently revealed that PVT SiC crystals have a strong [0001] texture around etch pit rows due to edge dislocation walls aligned along $<1\bar{1}00>$ directions [4]. The x-ray rocking curve with the incident plane parallel to the etch pit rows showed a narrow single diffraction peak, while the one with the incident plane perpendicular to the rows showed a much broader peak (40–80arcsec), often splitting into multiple peaks. Based on these results, we concluded that the tilting of the (0001) lattice plane has an axis of rotation parallel to both the boundary plane and the (0001) basal plane. We have also found that a major cause of the low angle grain boundaries in PVT SiC crystals is the inclusion of foreign polytypes during growth. The non-basal plane interfaces between the different polytypes accommodate crystallographic imperfections which relax into polygonized low angle grain boundaries during growth.

Over the past several years, a significant reduction in defect density has been achieved, and SiC substrates with low micropipe density and mosaicity have been successfully obtained. We discuss the causes and mechanisms of these crystallographic defects and demonstrate successful reduction of defect density in SiC crystals.

The final part of this paper deals with the growth of bulk SiC crystals perpendicular to the $<0001>$ *c*-axis direction. Drastically enhanced channel mobility has been demonstrated for SiC MOSFET fabricated on the $(11\bar{2}0)$ surface [5]. This achievement naturally spurred crystal grower's interest in bulk crystal growth in the $[11\bar{2}0]$ direction, which is essential for the fabrication of SiC$(11\bar{2}0)$ substrates having a large diameter and reasonable uniformity of doping concentration. In this growth direction, the polytypic structure of grown crystals perfectly succeeds to that of the seed, and thus polytype mixing never occurs during growth, and more importantly, the growth prevents micropipe formation. However, the growth tends to yield a large number of basal plane stacking faults in SiC crystals, and the density of the stacking faults strongly depends on the crystal growth direction and polytype. We present an atomistic surface model for the stacking fault generation and discuss a possible way to circumvent this problem.

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TuA3 MOS -Interface

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Oxidation of Silicon Carbide: Problems and Solutions

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Among compound semiconductors the unique property of silicon carbide (SiC) to form a wide-bandgap native oxide attracted great interest for development of SiC-based metal-oxide-semiconductor (MOS) electronic devices. The core process in MOS-technology— thermal oxide growth— when applied to SiC was demonstrated to yield silicon dioxide (SiO_2) layers of comparable insulating quality as in the case of silicon, where it has secured the continuing triumph of Si MOS electronics. However, in the case of SiC, the development of practical MOS devices is still hampered by the much inferior electrical quality of the SiC/oxide interfaces than the Si/SiO_2 ones, mostly in terms of interface defect density. Moreover, additional problems arise because SiC MOS devices are intended to extend the range of application of solid-state electronics to high temperatures and electric fields. As the result, the SiO_2 gate insulator faces exposure to an environment it never had to tolerate before, and hence, reliability issues become important even for relatively thick gate oxides. Therefore, the future progress of SiC MOS applications will significantly depend on the basic understanding of these problems, which can pave the way to their solution.

The goal of the present review is to combine the available experimental and theoretical results, both regarding SiC/SiO_2 and Si/SiO_2, with the view to address the current understanding of physical and chemical nature of the SiC/SiO_2 interface imperfections and the oxide degradation. On the basis of this understanding, possible approaches to improvement of the SiC/insulator properties will be discussed.

The first major problem concerns the SiC/SiO_2 interface states: While the oxide itself exhibits densities of electron and hole traps comparable to the densities encountered in the oxides grown on silicon, the typically reported densities of the SiC/oxide interface defects are by orders of magnitude larger than at Si/SiO_2 interfaces. The latter is largely related to the fact that a considerable number of SiC/SiO_2 interface states appear stable against inactivation (passivation) by hydrogen. Though typical for the (111)Si/SiO_2 interface (isomorphic to Si-faces of hexagonal SiC), Si-dangling-bond type defects are also present at the SiC/SiO_2 interface, they, however, can be easily passivated by H, and so, do not represent an immediate danger. The possible origin of the states stable against interaction with H has been discussed for years, and currently, two suggestions have received substantial experimental support: clustering of excess carbon at the SiC/SiO_2 interface, and the presence in the near-interfacial oxide layer of defects with energy levels within the SiC bandgap. To battle these imperfections several approaches have been used recently, like SiC surface engineering, low-temperature post-oxidation, oxide nitridation, etc. There is, however, a general trend suggesting that the

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processes determining the elimination of the defects in the upper and lower parts of the SiC bandgap are not always correlated. This might be related to the different origin of the donor-type states dominant in the lower half of SiC bandgap and the acceptor-type states near the conduction band edge. So, it is possible that there exists no single technological solution which would enable simultaneous elimination of these defects. Interestingly, it will be shown that the growth of ultra-thin (< 5 nm) oxides might be of advantage because it allows one to reduce the total amount of excess carbon by minimizing the consumed SiC volume. At the same time, thin oxides can easily be nitrided, which was shown before to reduce the oxide defect density.

As regards the second problem, the basic features of electrical degradation and breakdown of SiO_2 have been studied in detail in Si MOS devices. The degradation appears to be determined by injection of electrons and holes into the oxide accompanied by the release of atomic hydrogen, acting as catalist in bond-rupture processes. In the case of SiC, the injection-induced degradation may be considerably accelerated because the lifetime of a "hot" charge carrier increases in a wide bandgap semiconductor as compared to Si, leading to an enhanced carrier injection probability. Moreover, the high strength of electric field expected to be present in the gate oxide (particularly near p-n junction regions) may cause further "heating" of the electrons injected into SiO_2 ultimately leading to its breakdown. To counter these injection-induced effects one might consider reduction of the electric field strength in the oxide by employing a gate insulator with higher dielectric constant than that of SiO_2 (ε= 3.9). Such insulators are currently under intense investigation for deep-submicron Si MOS technology, and several materials like Al_2O_3 ($\varepsilon\approx$7-8), ZrO_2 ($\varepsilon\approx$15-20), and HfO_2 ($\varepsilon\approx$20-25) were shown to be compatible with standard MOS processing. The major constraint in the application of these materials to SiC consists in their relatively narrow bandgaps (5-6 eV wide) which would result in low valence band offsets and, consequently, in high leakage current. Nevertheless, the experience gained on Si substrates indicates that this problem may be successfully overcome by applying a stack of ultra-thin SiO_2 and high permittivity oxide because the latter can be deposited in amorphous phase at temperatures as low as 300-350 °C.

A more complex reliability issue concerns the degradation of the SiC/oxide interfaces observed upon electrical biasing at elevated temperatures. This phenomenon, known in Si MOS structures as the bias-temperature instability, is basically related to the formation of protonic species in the near-interfacial SiO_2 (by trapping holes from the semiconductor) and their subsequent interaction with the semiconductor surface. Moreover, even without application of an electric field, proton-like species can be created by interface ionization of hydrogen observed both for Si and SiC at temperatures above 500 °C. As hydrogen passivation of defects necessary to fabricate an operational MOS device, its uncontrolled release afterwards cannot be excluded, particularly under conditions of current flow. The obvious (but only partial) solution consists in reduction of electric field at the SiC/oxide interface in devices intended for operation at elevated temperature. However, for the surface-channel MOS devices, the H-related degradation may appear the factor that will limit the temperature range of SiO_2 application as a gate insulating material.

High Current, NO Annealed Lateral 4H-SiC MOSFETs

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Recent advances in 4H-SiC MOS technology has rejuvenated interest in developing this structure for power MOSFET applications. The incorporation of post oxidation annealing in pure nitric oxide (NO) ambient at elevated temperatures has shown dramatic reductions in interface state density and significantly improved performance on test MOSFET devices[1]. However, before this breakthrough can be applied to real power MOSFET devices, we must understand how the NO annealed MOS interface is affected by process and design constraints relevant to power device fabrication. In this paper we show that the benefits of the NO anneal are not lost in the presence of an implanted p-well and the high temperature anneal necessary to activate the p-type implants. For the first time, we present Hall Effect measurements that further verify the improved mobility of electrons in the inversion layer due to NO. And, thanks to the uniformity and isotropy of the NO passivation, we are able to scale-up to large area (1 mm x 2 mm) devices delivering 2 A of on-state current at a 2.05 V forward drop!

4H-SiC n-channel MOS devices were fabricated on a 3 μm epilayer doped in the high 10^{15} cm^{-3}. Half of the wafer was aluminum implanted in order to simulate the effects of forming the MOS channel on a p-well. Nitrogen was implanted to form the source/drain regions. The implants were activated with a 5 min 1600°C argon anneal. A control sample was oxidized using the standard 1200°C dry + 950°C wet recipe [2]. A second sample was oxidized at 1150°C wet for 2.5 hr and then annealed in NO at 1175°C for 2 hr. Molybdenum and nickel were used for the gate and contact metallizations respectively. Figure 1 shows a collection of field effect mobility from 100 μm x 100 μm MOSFETs on these two wafers. Note that the NO annealed devices show higher mobility which is independent of location and channel orientation—necessary criteria for successfully scaling to large area devices. A particular concern for DMOS structures is the MOSFET mobility on implanted p-wells where mobility has been shown to degrade by at least an order of magnitude. The NO annealed MOSFETs remarkably exhibit very minimal mobility reduction on implanted p-wells—a very encouraging result for the DMOSFET.

Extracting true carrier transport properties can be difficult with MOSFET-based techniques due to the large amount of trapping that occurs at the MOS interface. However, the Hall Effect measurement does not suffer from such drawbacks[3]. Figure 2 shows the result of Hall measurements on a Van der Pauw MOS Hall bar for both NO annealed and unannealed samples. Consistent with the drift result, the NO sample shows a higher channel mobility surpassing 60 cm^2/Vs. Hall data can also be analyzed to extract interface trap density near the conduction band (Fig. 3) on p-type MOSFET-like structures instead of n-type MOS-capacitors[4]. A small but significant reduction in interface trap density is observed in the NO-annealed sample.

To test the scalability of the NO anneal technology, we fabricate interdigitated 1 mm x 2 mm lateral MOSFETs. These devices have 20 μm wide source/drain fingers separated by 3 μm channels resulting in a cell pitch of 23 μm. The forward characteristics of such a device are given in Fig. 4. The aforementioned high current level (2 A) is obtained by applying 20 V on the gate (16 V above threshold resulting in 3.5 MV/cm stress on the gate oxide) and 2.05 V of

forward bias. This results in a specific on-resistance of 10.3 $m\Omega cm^2$ which is the lowest reported value for any inversion-mode 4H-SiC MOS device. In conclusion, we have found the NO anneal to outperform the previous state-of-the-art MOS process in 4H-SiC, making this an ideal candidate for implementation in power MOSFET processing thereby ushering in a new era of SiC power MOS devices.

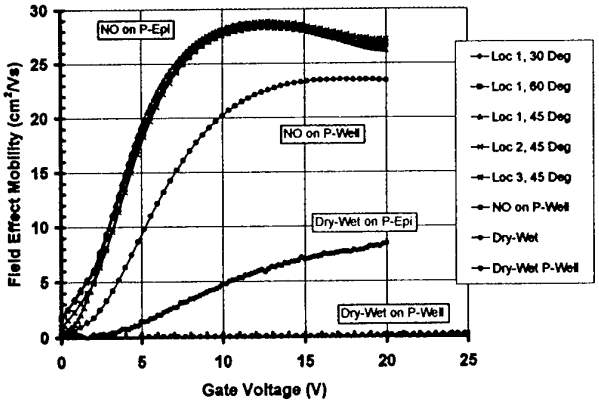


Figure 1. Collection of mobility data for NO annealed 4H-SiC FatFETs at various locations, channel orientation and channel makeup (epi or well). Dry-wet MOSFET data is also plotted.

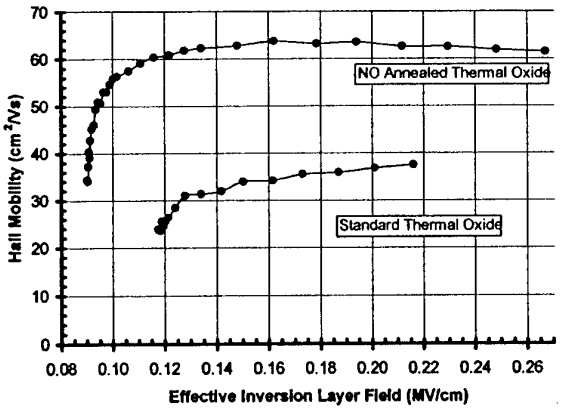


Figure 2. Improved Hall mobility of electrons in the 4H-SiC inversion layer due to a post oxidation NO anneal. Both MOS Hall bars are fabricated on unimplanted epilayers.

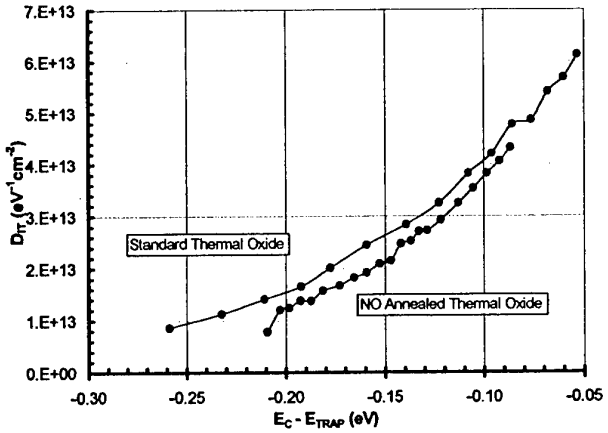


Figure 3. Reduced Hall interface state density near E_C in 4H-SiC due to a post oxidation NO anneal.

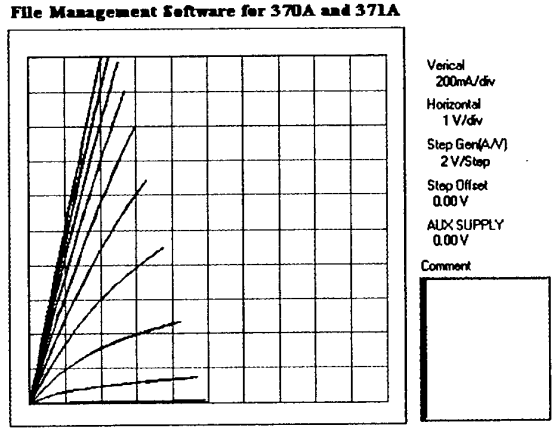


Figure 4. Forward characteristics of a 4H-SiC NO annealed 1 mm x 2 mm lateral MOSFET.

This work is supported by AF Wright Labs Contract F33615-99-C-2914 (monitored by Richard Domingo), DARPA Contract MDA972 98-1-0007 and EPRI Contract W0806905.

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N_2O Processing Improves the 4H-SiC:SiO_2 Interface

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SiC Metal Oxide Semiconductor (MOS) devices are severely impacted by the large density of interface states present at the SiC:SiO_2 interface. Interface states near the conduction band-edge are particularly effective at inhibiting SiC device performance. Early improvements in oxidation processes reduced interface states only from the valence band to mid-gap.[1] More recent progress has been accomplished using an NO anneal[2,3], which lowers the interface state densities near the conduction band-edge. While these improvements using NO annealing are important, use of this gas in traditional furnaces is not desirable with the health risks associated with pure NO. Use of N_2O has been pursued and effectively developed as an alternative to NO.

As shown in Figure 1, the temperature of the N_2O processing is critical. At lower temperatures (1100°C), exposing an existing oxide to N_2O increases the interface state density, as shown by comparing the heavy solid line representing a thermal oxide to the data for the same thermal oxide exposed to an 1100°C N_2O anneal. At 1200°C, the thermal oxide is dramatically improved with the N_2O anneal. Thermal oxides processed in a wet ambient are more improved by the 1200°C N_2O anneal, as seen by comparing the solid circle to the open circle data.

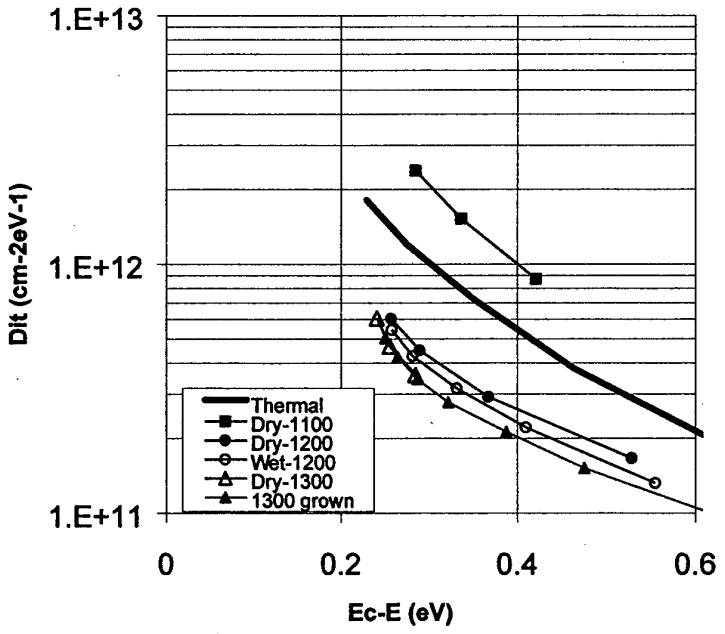


Figure 1. Interface State Density Near the Conduction Band-Edge for 4H-SiC. Samples with thermal oxides with different temperature N_2O anneals and one sample grown in N_2O are compared.

The best results are obtained using a 1300°C N_2O process. At this temperature, the oxidation of SiC is significant. So, in addition to annealing existing oxides in N_2O, some oxides were grown in the N_2O ambient (500 Å was grown in 3 hours). Growing the oxide in N_2O saves about 9 hours of processing time over annealing an existing oxide in N_2O, by eliminating the oxidation step. The same superior results are obtained regardless of whether the oxide is grown prior to N_2O processing or grown in N_2O.

MOSFETs processed with our earlier 1200°C N_2O annealed oxide had higher effective surface channel mobility than devices that did not receive the N_2O anneal, as shown in Figure 2. The interface state densities measured on nearby p-type capacitor structures and corresponding n-type capacitors are shown in Figure 3. The reduction in interface state density directly correlates with an improvement in effective surface channel mobility.

We will also have effective surface channel mobility data on 4H-SiC MOSFETs with oxides grown in N_2O at 1300°C to present at the conference.

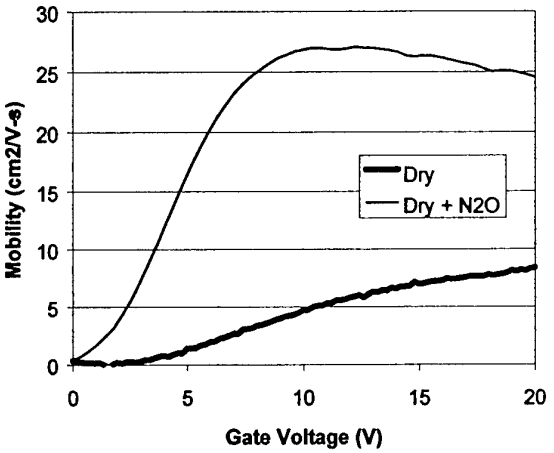


Figure 2. Effective Surface Channel Mobility for 4H-SiC planar MOSFETs, with and without N_2O processing.

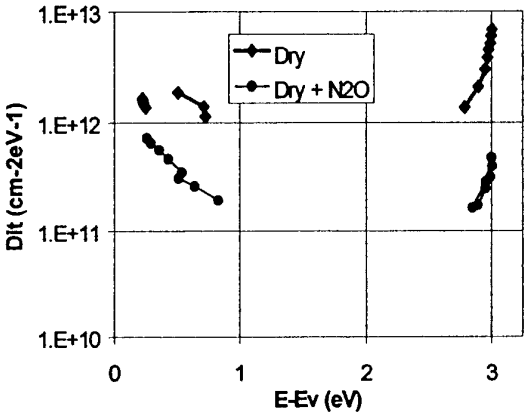


Figure 3. Interface States across the entire band-gap for the oxides of Figure 2.

Acknowledgements

This work was supported in part by the Army Research Laboratory, contract DAAD17-99-C-0009, monitored by Skip Scozzie, and Air Force Wright Laboratory, Contract F33615-99-C-2914, monitored by Richard Domingo.

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Significant Improvement of Inversion Channel Mobility in 4H-SiC MOSFET on (11$\bar{2}$0) Face using Hydrogen Post Oxidation Annealing

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4H-Silicon carbide (SiC) metal-oxide-semiconductor field-effect-transistor (MOSFET) is expected as a promising candidate for a high-speed and low-loss switching power device. However, there have been few satisfactory results regarding the fabrication of 4H-SiC MOSFET with high inversion channel mobility. It has been pointed out that high interface trap density (D_{it}) at SiO_2/SiC interface lowers the inversion channel mobility, resulting in high on-resistance (R_{ON}) of 4H-SiC MOSFET. Yano et al. reported that the inversion channel mobility of around 30 cm^2/Vs in 4H-SiC MOSFET was obtained utilizing (11$\bar{2}$0) face instead of conventional (0001) Si face, but was not sufficient to reduce the R_{ON}.[1] We have reported that hydrogen post oxidation annealing (H_2 POA) reduce the D_{it} near the conduction-band edge of the n-type 4H-SiC MOS structures on (0001) Si face.[2] In this study, the significant improvement of the inversion channel mobility in 4H-SiC MOSFET fabricated on (11$\bar{2}$0) face using H_2 POA is reported.

N-channel MOSFETs were fabricated on p-type epitaxial layers grown in our group on n-type 4H-SiC substrates with the (11$\bar{2}$0) face orientation purchased from Nippon Steel Co. The thickness and the effective doping density of the epitaxial layers were 3.5 μm and $1x10^{15}$ cm^{-3}, respectively. Source and drain regions were formed by phosphorus ion implantation at 500°C with the total dose of $7x10^{15}$ cm^{-2}. Post implantation annealing was performed at 1500°C for 5 min in Ar. Gate-oxides were thermally grown in water vapor atmosphere [wet oxidation, samples (a) and (b)] at 1150°C and were *in-situ* annealed in Ar at the oxidation temperature for 30 min, resulting in oxide thickness of 49 nm. In addition, the sample (b) was annealed in pure hydrogen at 800°C for 30min [H_2 POA]. Aluminum was evaporated as the gate and source/drain contact metals. The channel length (L) and width (W) were 100 and 150 μm, respectively. Electrical measurements were carried out at room temperature using a Hewlett-Packard Semiconductor Parameter Analyzer 4156B. The drain

current was measured along [0001] direction.

Figure 1 shows typical drain current (I_D) – drain voltage (V_D) characteristics of 4H-SiC MOSFET with gate-oxide prepared by wet oxidation following H_2 POA fabricated on the (11$\bar{2}$0) face [sample (b)] for different gate voltages (V_G) between 0 and 12 V. The I_D-V_D characteristics exhibit excellent linear and saturation regions. The results of a field-effect mobility (μ_{FE}) measurement for both the wet gate-oxide 4H-SiC MOSFETs with and without H_2 POA are shown in Fig. 2. The μ_{FE} was calculated from I_D-V_G characteristics at V_D=0.1 V. The peak μ_{FE} of the sample (a) is almost the same value with that reported by Yano et al.[1] The gate-oxide preparation process including the H_2 POA drastically enhances the μ_{FE} and results in the peak μ_{FE} of 110 cm^2/Vs in the samples (b). The values of a subthreshold voltage swing for the samples (a) and (b) are 204 and 85 mV/decade, respectively. This result suggests the H_2 POA reduces the D_{it}. To our knowledge, the inversion channel mobility of 110 cm^2/Vs is the highest for lateral n-channel 4H-SiC MOSFETs with a thermal gate-oxide reported until now.

This work was performed under the management of FED as a part of the METI NSS program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

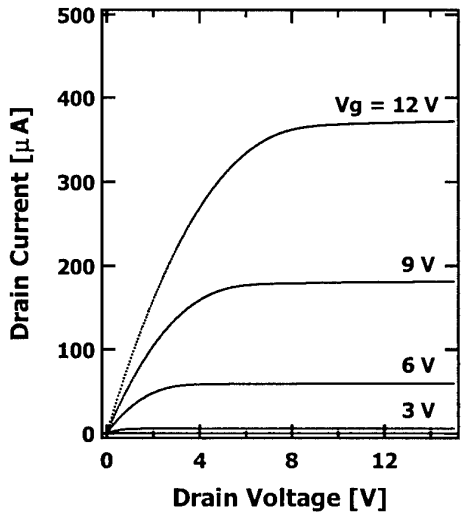


Fig. 1. I_D-V_D characteristics of 4H-SiC MOSFET with gate-oxide prepared by wet oxidation following H_2 POA fabricated on the (11$\bar{2}$0) face.

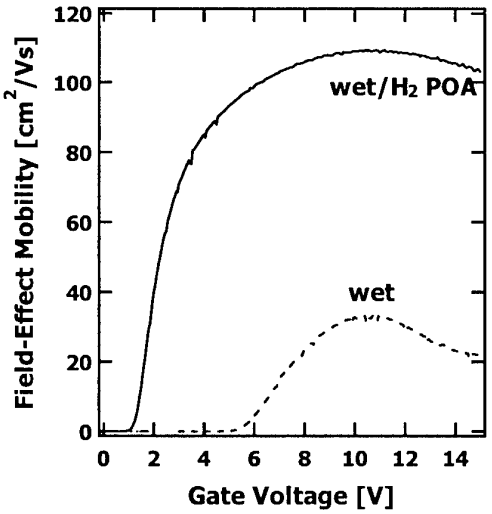


Fig. 2. μ_{FE}-V_G characteristics of wet gate-oxide 4H-SiC MOSFET with and without H_2 POA fabricated on the (11$\bar{2}$0) face.

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SiC-based MOS structure with an SiO_2 layer formed at ~200 °C by use of perchloric acid

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1. Introduction

SiC is a wide-gap semiconductor that is less reactive than Si, and thus thermal oxidation of SiC requires high temperatures above 1050°C [1-4]. Such high temperature heat treatments degrade interfacial properties, e.g., high interface state density more than 10^{11} $cm^{-2}eV^{-1}$ [3,4]. We have recently found that the Si oxidation proceeds at ~200 °C by use of perchloric acid [5,6] and the resulted silicon dioxide (SiO_2) layers possess a low interface state density of $1.5x10^{10}$ $cm^{-2}eV^{-1}$ even without hydrogen treatment [6]. In the present study, this noble method is employed in the formation of SiC-based MOS structure. We have found that the concentration of graphitic carbon at the interface is very low in cases where post-oxidation heat treatment is performed at 950 °C, resulting in the low interface state density of $1x10^{11}$ $cm^{-2}eV^{-1}$.

2. Experiments

MOS structure was fabricated using a nitrogen-doped n-type SiC epitaxial layer of ~10 μm thickness with the donor density of $6x10^{15}$ cm^{-3} formed on a 6H-SiC(0001) wafer. An SiO_2 layer was formed by the immersion of the wafer in concentrated perchloric acid ($HClO_4$) at the boiling temperature of 203 °C. Post-oxidation heat treatments were performed at temperatures ranging between 950 and 1150 °C in nitrogen. Then, aluminum (Al) dots of 0.15 mm diamter were formed on the surface, resulting in <Al/SiO_2/6H-SiC(0001)> MOS structure.

3. Results and discussion

Figure 1 shows the plot of the thickness of the SiO_2 layer vs. the immersion time in $HClO_4$ at 203 °C. It is seen that thick SiO_2 layers of ~80 nm thickness can be formed in spite of the low oxidation temperature. The plot is almost linear, indicating that the oxidation is reaction-limited [7], in contrast to diffusion-limited conventional thermal oxidation [8]. This result shows that diffuison of the oxidizing species (i.e., O^- ions formed by the decomposition of ClO_4^- ions [5,6]) through the growing SiO_2 layer proceeds smoothly. The inward migration of O^- ions is likely to be promoted by the electrical field induced in the SiO_2 layer by ClO_4^- ions at the surface [6]. The reaction at the interface proceeds at the low temperature because of the high reactivity of O^- ions.

We have found that the leakage current density of the <Al/SiO_2/6H-SiC(0001)> MOS diodes was high without post-oxidation heat treatment due to the presence of Cl^- and ClO_4^- ions in the SiO_2 layer, while with post-oxidation heat treatment above 900 °C in nitrogen, it became sufficiently low, i.e., less than 10^{-8} Acm^{-2} at the gate bias of 5 V.

Figure 2 shows the capacitance-voltage (C-V) curves of the <Al/SiO_2/6H-SiC(0001)> MOS diodes. When the post-oxidation heat treatment was performed at 1100 °C (curve a), the high-frequency (solid line) and quasi-static (dotted line) C-V curves deviated from each other, due to the presence of high density interface states. From these curves, the interface state density at 0.5 eV below the conduction band minimum is estimated to be $3x10^{11}$ $cm^{-2}eV^{-1}$. When the post-oxidation heat treatment temperature was lowered to 950 °C, the deviation between the high-frequency and quasi-static C-V curves became much smaller (curve b). In this

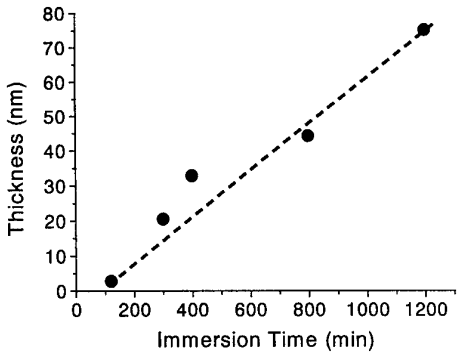


Fig. 1 Thickness of the SiO_2 layers vs. the time of immersion of SiC in $HClO_4$ at 203 °C.

case, the interface state density at 0.5 eV was estimated to be $1x10^{11}$ cm^{-2} eV^{-1}.

Figure 3 shows the XPS spectra for the SiO_2/6H-SiC(0001) interface. For XPS measurements, thick SiO_2 layers were formed by the immersion in $HClO_4$, followed by etching of the layers with a 1 % HF solution. The etching was stopped when the substrate Si 2p peak as well as the oxide peak was observed with considerable intensities (SiO_2 thickness: 2.5 nm). After post-oxidation heat treatment at 1150 °C, a C 1s peak due to graphitic carbon was observed in the higher energy side of the SiC substrate peak (spectrum a), and its amount is estimated to be 1.3 monolayer. The intensity of the C 1s peak due to graphitic carbon was markedly reduced by lowering the post-oxidation temperature to 950 °C (spectrum b), and in this case its concentration is estimated to be 0.6 monolayer. It should be noted that for the thick SiO_2 layers formed with $HClO_4$, no C 1s peak due to graphitic carbon was observed, indicating that carbon was not present in the bulk of the SiO_2 layer.

Comparison of Figs. 2 and 3 leads to the conclusion that the interface states are mainly due to graphitic carbon. In the case of thermal oxidation at high temperatures, loss of Si occurs, resulting in the formation of graphitic carbon at the interface [9]. For the oxidation by $HClO_4$, the formation of graphitic carbon does not occur because of the low temperature oxidation in addition to the high reactivity of $HClO_4$ with carbon. However, the SiO_2 layers include Cl^- and ClO_4^- ions with the total concentration of 0.2 atomic%, and these species act as trap states, resulting in the high leakage current density. For the removal of the Cl-species, post-oxidation heat treatment is necessary. In this case, however, post-oxidation heat treatment should be performed

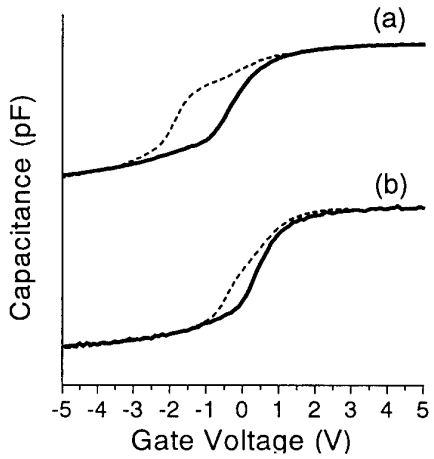


Fig. 2 C-V curves for the <Al/SiO_2/6H-SiC(0001)> MOS diodes having an SiO_2 layer formed in $HClO_4$ at 203 °C with post-oxidation heat treatment at the following temperatures: a) 1100 °C, b) 950 °C.

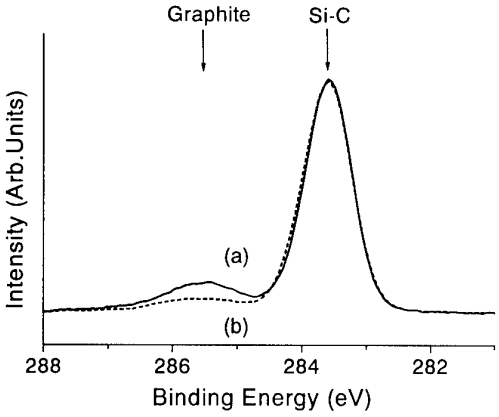


Fig. 3 XPS spectra in the C 1s region for the SiO_2/SiC interfaces with post-oxidation heat treatment at the following temperatures: a) 1150 °C, b) 950 °C.

at temperatures lower than 950 °C in order to prevent the formation of graphitic carbon at the interface.

4. Conclusions

We have developed a low temperature fabrication method of SiC-based MOS structure by use of $HClO_4$. In spite of the oxidation at 203 °C, an SiO_2 layer sufficiently thick for the MOS application can be formed. When the post-oxidation heat treatment is performed at 950 °C, the concentration of the interfacial graphitic carbon is very low, resulting in the low interface state density of $1x10^{11}$ $cm^{-2}eV^{-1}$ at 0.5 eV below the conduction band minimum.

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TuB3 Optical Properties 1



Experimental Determination of the Phonon-Eigenvectors of Silicon Carbide by Raman Spectroscopy

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The phonon frequencies of silicon carbide (SiC) depend on the atomic masses of the constituent elements Si and C. In general, the frequency decreases, when the mass of one kind of atom is increased by isotopic substitution. Quantitatively, the frequency shift $\Delta\omega(\vec{q})$ of a phonon mode of wave vector $\vec{q}$ depends on how much of the energy contained in that mode is carried by the sublattice of substituted atoms. This energy is proportional to the square of the phonon eigenvector $|e_i|$ according to [1]:

$$\frac{\Delta\omega(q)}{\omega(q)} = \frac{\Delta M_i}{2M_i} |e_i(q)|^2 , \qquad (1)$$

where $\Delta M_i/M_i$ is the relative mass change of element i. By measuring $\Delta\omega(q)$ one is thus in the position to determine $|e_i(q)|$ for one of the sublattices (C or Si).
We have grown 6H-, 4H-, and 15R-SiC polytypes enriched to 83% with the ^{13}C-isotope. The frequencies of all Raman active phonon modes have been measured accurately in back-scattering geometry along the c-axis direction.
The absolute values of the carbon eigenvector e_C for the transversal and longitudinal branches as a function of the phonon wave vector q evaluated with Eq. 1 are shown in Figs. 1 and 2, respectively. For these figures, the large Brillouin zone of 3C-SiC has been used and the observed phonon modes of the different SiC polytypes are plotted with q-vectors assigned by use of the zone folding concept[2]. The experimental data are compared to eigenvectors calculated with a linear chain model employing the force constants given in the literature[2,3]. Good agreement is observed for the transversal modes in Fig. 1, whereas there are larger deviations for the longitudinal modes. We discuss these deviations that are most probably due to deficiencies in the values of the force constants used in Ref. [3].

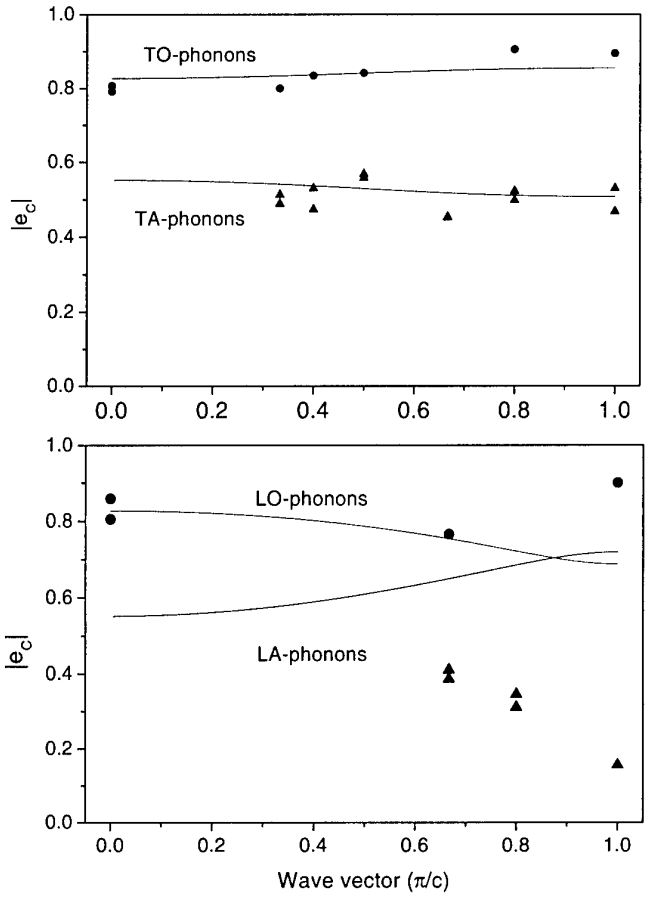


Fig.1: Absolute values of the phonon eigenvector $|e_C(q)|$ of carbon atoms for the transversal modes as derived from the isotope shift of Raman frequencies. Circles: TO-modes, triangles: TA-modes. Lines are calculated with a linear chain model according to [2].

Fig.2: Absolute values of the phonon eigenvector $|e_C(q)|$ of carbon atoms for the longitudinal modes as derived from the isotope shift of Raman frequencies. Circles: LO-modes, triangles: LA-modes. Lines are calculated with a linear chain model according to[3].

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Raman Microprobe Study of Carrier Density Profiles in Modulation-doped 6H-SiC.

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Electrical properties such as carrier concentration and mobility of semiconductors have mainly been studied by Hall and C-V measurements so far. Recent studies have demonstrated that the Raman spectroscopy can also be used to characterize the electrical properties of polar semiconductors[1,2]. Raman microprobe measurement has a great advantage for characterization of the electrical properties of local areas on the micron meter scale, because it is non destructive and contactless technique. Up to now the Raman microprobe has been applied to determination of carrier density profiles of GaP diode [3], SiC wafers[4] and around micropipes in SiC [5] .

In this work we have measured Raman images for LO-phonon plasmon coupled mode (LOPCM) in modulation doped 6HSiC crystals and determined spatial distribution of N-donors. From the analysis of the Raman profile the dependence of the carrier mobility on the impurity concentration and the residence time of the N_2 dopant gas on the surface of growing crystals after switch-off of the doping gas are inferred. The residence time thus inferred is in agreement with that estimated from the test of the furnace system.

6H SiC crystals were grown by modified-Lely method. Modulation doping was made by on-off switch of the N_2 gas [6] so that the doped impurity has a step -like distribution as shown in Fig.1(a). The surface of the sample used is (0001). Raman spectra were measured using a triple spectrometer (f=0.6 m) with an image expander of 2 magnification and a cooled CCD detector. One-dimensional images of the LOPCM were obtained using an optical microscope. Laser beam was linearly expanded with a cylindrical lens and illuminated on the sample surfaces.

The measured line shape of the LOPCM was fitted to the theoretical curve using carrier concentration (n) and mobility (μ) as adjustable parameters[7]. The carrier concentration thus determined is plotted as a function of the distance in Fig.1(b). The carrier concentration rises steeply after

the dopant-gas supply and decreases slowly after the stop of the gas. The transition region between the doped and undoped zones is ~20 μm in the switch-off case and ~8μm in the switch–on case. This result indicates that N_2 gas remains for a while after the stop of the dopant-gas supply. The residence time of N_2 gas on surface of the growing crystals inferred from the width of the transition region and the growth rate (1mm / h) is 74 s, which is in close agreement with that (75 s) determined in advance from the test of the growth furnace. The relationship between the carrier mobility and concentration is also obtained by the line shape analysis of the LOPCM.

The above results demonstrate that Raman microprobe imaging is useful to analyze the doping process of impurity in bulk and epitaxial SiC.

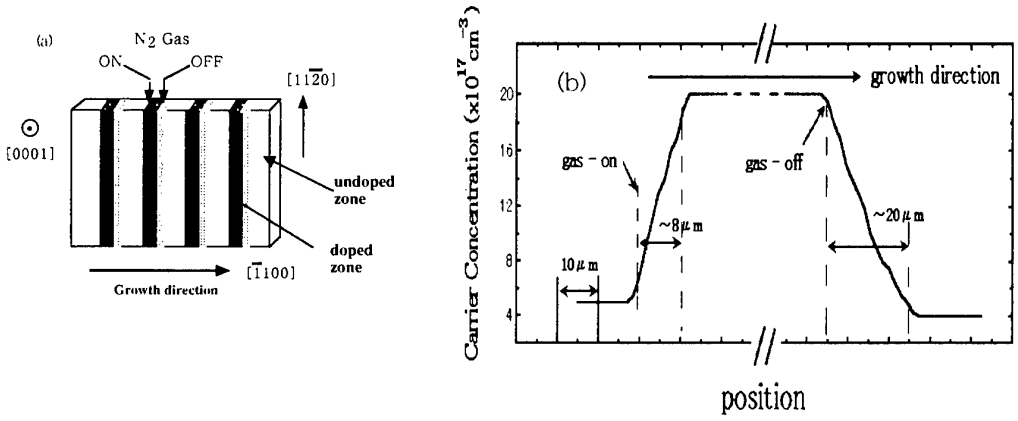


Fig.1 (a) Schematic structure of modulation–doped SiC and (b) profile of the carrier concentration determined from the Raman analysis.

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A Raman Study on Metal-SiC Interface Reactions

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An important problem for fabricating variety of SiC-based electronic devices is to find suitable electrode materials with their processing technique to obtain low-resistance (ohmic) contacts with SiC layers. Obviously, the contact resistance depends on the electrode-SiC interface reactions. Therefore, in order to reveal the mechanisms for lowering the contact resistance, it is crucial to probe the interface reactions at various processing conditions.

A common method for this purpose is bombarding charged particles to extract relative abundance of constituent elements; i.e., Auger-electron spectroscopy (AES), secondary ion mass spectrometry (SIMS), and Rutherford back scattering (RBS). These methods are, however, all destructive, expensive, and sometimes very time-consuming. We would like to propose here a Raman scattering technique that provides an easy test for interface reactions. It is an optical method, therefore, non-destructive, and enables 2-dimensional analysis with micrometer resolution, which is suitable for diagnosis of future integrated circuits.

Here we selected Ti or Ni as a standard electrode material. The metallic layer was deposited in vacuum on 6H-SiC commercial wafers (both sides polished). Both Si- and C-faces were tested for deposition, changing the metallic-layer width, annealing gas species (N_2 or Ar), temperature (500-1100°C) and time. The Raman spectra were observed at room temperature by back scattering using a microscope. The Ar^+ laser line at 5145 Å was used for excitation. Figure 1 shows a typical result for Ti/SiC, annealed in Ar at 1000°C for 5 min.

Here, (a) shows a result when Ti was deposited on SiC (C-face), and the probe laser was focused on the electrode top surface, while (c) was observed when the probe laser was focused through the SiC layer on the Ti/SiC interface. The spectrum (b) was obtained like (c), but the Si-face was selected for Ti-deposition. The optical arrangement like (b) or (c) is possible because of the large band gap nature of SiC, which is an important advantage in our optical detection as mentioned below. The common sharp peaks in (b) and (c) are phonon signals of SiC. Figure 1 shows distinctly different features depending on the observed portions; (a) is dominated by broad peaks for TiC_{1-x}, while (c), enhanced in scale in Fig.2, shows faint but sharp structures ascribed to $TiSi_2$. Contrary to (c), Ti/SiC (Si-face) interface shows strong TiO_2 signals as depicted in Fig.1 (b).

These results show various findings for this annealing condition; First, decomposition of SiC is enhanced at the C-face, which promotes Ti-silicidation reaction. On the contrary, Ti-oxidation due to inevitable oxygen impurities incorporated in the annealing process is promoted on the Si-face. Second, carbon atoms reach the top surface of electrode by thermal diffusion, which reflects superior diffusivity of carbon atoms than Si in Ti.

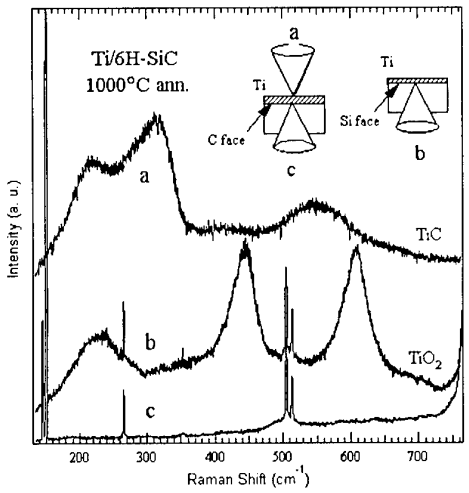


Fig.1 Typical Spectra

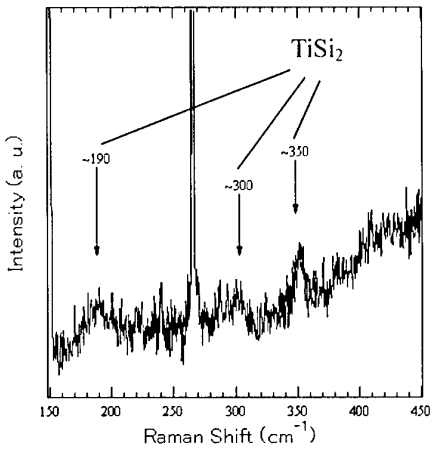


Fig.2 Spectrum Fig.1 (c) is enhanced.

Optical, surface and interface properties of ion implanted 4H-SiC

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A series of Al ion-implanted and C^+-Al^+ co-implanted 4H-SiC epilayers have been studied by optical transmission (OT), micro-Raman scattering and Fourier transform infrared (FTIR) spectroscopy measurements. The damage and amorphization of SiC layer by ion-implantation, and the elimination or suppression of the implantation induced amorphous layer via high temperature annealing are evidenced. The recovery of the crystallinity and the activation of the implant acceptors are confirmed.

SiC is a promising material for electronic and optoelectronic devices operating in high temperature, high power and other extreme environments. In recent years, much progress has been made in the research and development of 6H- and 4H-SiC materials and devices, for which, a critical issue is the doping technique. It is limited to use conventional diffusion methods to produce the SiC-based p-n junction and devices due to the very low thermal diffusion coefficient. The ion implantation into SiC appears to be the primary method to produce selective structured p-doped layers. Al is a preferred acceptor in SiC due to its lower activation (ionization) energy (0.24 eV). In order to improve the efficiency of Al^+ to substitute Si atom sites, co-implantation of C ions is expected to enhance to break the balance of stochiometry towards C enrichment and thus improve the chance of Al dopants to settle at Si atom sites. Ion implantation can cause severe damage of the crystallinity. Post-annealing is necessary for crystal recovery and electrical activation of implanted species. In this paper, investigation is focused to analyze the effects of Al^+ and C^+-Al^+ implanted/annealed 4H-SiC, and to establish the correlation of their optical, surface and interface properties with process.

Experimental samples are epitaxially grown n^-/n^+ 4H-SiC/4H-SiC. Multiple-energy implantation, 65-196 KeV for Al ions and 32-160 KeV for C ions, at room temperature (RT), were carried out to obtain a box-like implantation profile. C ions were implanted preceding Al ions. Annealing in an ultrahigh purity Argon ambient in a conventional furnace was performed at 1550 °C for 30 min. By means of UV-Visible OT, micro-Raman and FTIR spectroscopy, the surface and subsurface modifications induced by ion implantation and post-annealing are examined.

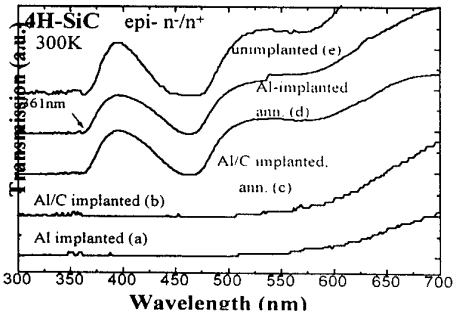


Fig. 1 OT spectra recorded on as-implanted (a)-(b), post-implantation annealed (c)-(d), and one virgin (e) 4H-SiC.

Fig. 1 shows optical transmission spectra, indicating the damage and amorphization of SiC layer by ion-implantation, for Al^+ implanted, in (a), and Al^+/C^+ co-implanted, in (b), samples. After 1550°C annealing, a sharp transition edge near 360 nm (3.4 eV) appears, as shown in (c) and (d). It presents the optical absorption gap of crystalline 4H-SiC, in comparison with

the OT spectrum from a virgin sample, in (e). Therefore the elimination or suppression of the implantation induced amorphous layer via high temperature (HT) annealing is evidenced.

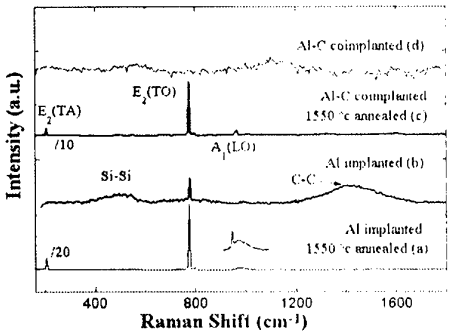


Fig. 2 Comparative Raman scattering for implanted and annealed 4H-SiC.

Fig. 2 shows micro-Raman measurements on four samples. It is seen that after Al^+ implantation at RT, only weak peaks and two broad bands are observable. These broad bands at ~500 cm^{-1} and 1400 cm^{-1} are typical for amorphous SiC, indicating the damage of 4H-SiC crystallinity and the formation of an amorphous phase. After HT annealing, Raman spectra close to that of crystalline 4H-SiC appear, predicting the recovery of the SiC crystalline structure.

Figure 3 exhibits the IR reflectance for four implanted samples and a virgin (un-implanted) one. Significant variations are seen after both Al/C and Al implantation, comparing with the un-implanted one, especially in reststrahlen band: the intensity decreases greatly; one notch at 934 cm^{-1}, with the minimum as low as 30%, becomes a dominant feature in the reststrahlen band. However, HT annealing recovered the optical behaviour, both in intensity and line shape, but in different degree.

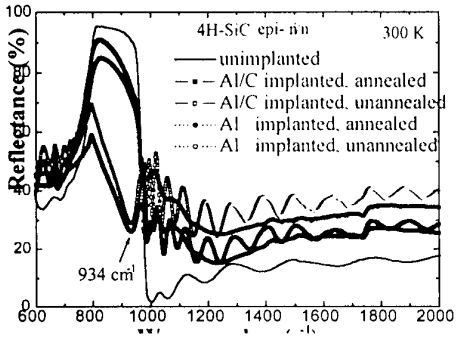


Figure 3 IR reflectance spectra from Al$^+$ and C$^+$/Al$^+$ implanted/annealed n-/n+ epitaxial 4H-SiC, and an unimplanted sample for comparison.

To explain these experimental findings, we have developed a multiple-layered model and applied to the reflectance profiles. Samples are defined as three-layer structural matrix in the configuration of amorphous layer/crystalline 4H-SiC/substrate. For amorphous SiC, the Si-C stretching mostly appears as a broad band in IR absorption, and it is treated as an adjustable parameter in the fitting process. The reststrahlen band can be fitted by the classical dispersion theory with proper choice of the dispersion parameters related to the materials properties.

Our detailed simulation and analysis have produced significant results. The notch at 934 cm^{-1} was found to originate from amorphous SiC, i.e. a continuous buried amorphous layer close the surface. The Si-C stretching frequency derived from fitting is at 780cm^{-1}, which is consistent with previous results in a-SiC:H films. The thickness of amorphized layer derived from FTIR fitting is about 0.32 μm for Al/C co-implanted and 0.35 μm for Al single implanted samples. After HT annealing, the structural matrix in the implanted region changes from amorphous phase into crystalline one with high carrier concentration. Acceptor activation is evidenced by the increase of the plasma frequency, ω_p, up to 600 cm^{-1} (corresponding to N=1.3x10^{19}cm^{-3}) after annealing. Better recovery of optical properties in Al/C co-implanted than Al single implanted sample is verified. The correlation is established between the observed variation of optical, surface and interface properties with the structural modifications induced by implantation and annealing. All these results indicate that high temperature annealing successfully refreshes the 4H-SiC crystallinity, even though the degree of recovery strongly depends on implantation conditions.

Raman scattering from wurtzite GaN bulk crystal

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GaN has long been considered as a promising material for semiconductor device applications due to its unique electronic and mechanical properties and has been the focus of intensive studies in the resent years. With a direct wide band-gap and high thermal stability, GaN is a suitable material for the blue and near-UV light emitting devices and high temperature electronics [1]. However, the major difficulty that has hindered GaN epilayer research and its commercial applications is the lack of a suitable substrate material that is lattice-matched and thermally compatible with GaN. Nevertheless, GaN has been grown commonly on SiC, ZnO and Al_2O_3. In fact, several other materials have also been used as the substrate, but the optical and electrical properties of the grown epilayers have not been satisfactory. GaN bulk material itself is the best choice as the substrate material, however, there has hardly been any success in the growth of good quality bulk GaN, which is mainly due to the high melting temperature of GaN and low reactivity between gallium and nitrogen. Moreover, in spite of the technological perspective of this material, only little work has been performed on the fundamental properties of GaN compared to the other III-V semiconductors, which is partly due to the unavailability of good GaN crystals. Under ambient conditions, GaN crystallizes in the hexagonal wurtzite (2H) structure with the space group C_{6v}^4. However, some epitaxial growths have also resulted in cubic zinc blend (3C) structures. The two structures basically differ in the stacking of the Ga-N bilayers perpendicular to the hexagonal [0001] and cubic [111] directions, respectively. Recently, there has been some success in the growth of large size 2H bulk GaN with good crystalline qualities. In this paper, we report, for the first time, some basic characterization of 2H bulk GaN crystal in a view to understand the fundamental vibronic and electric properties of this material, studied by polarization-dependent Raman

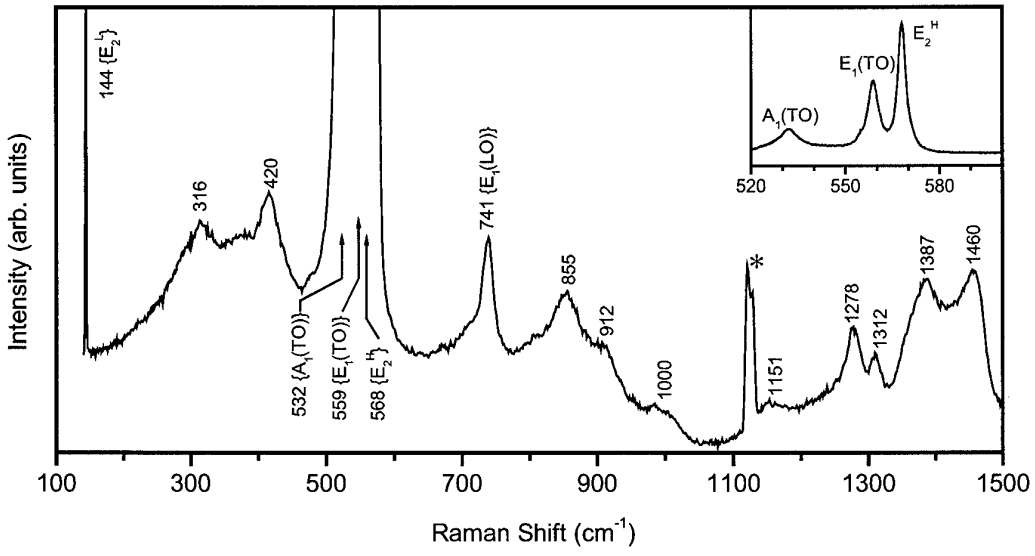


Fig. 1 Unpolarized room-temperature Raman spectrum from GaN bulk crystal in combined [x(y,y)-x + x(y,z)-x] backscattering configuration. The numbers indicate phonon frequencies in cm^{-1}. Inset shows the details of phonon modes between 520 and 580 cm^{-1}.

scattering technique under various scattering configurations. The as-grown GaN crystal was cut in to a 0.5 mm thick, 1 cm square-shaped wafer and was mirror polished for better scattering. Raman scattering studies were performed under various scattering configurations at room temperature. GaN is transparent to the probing laser wavelength (514.5 nm), which brings an advantage of large scattering volume, resulting in strong scattering intensities. Due to the momentum conservation, the first-order Raman spectrum shows phonons corresponding to the Γ-point ($k = 0$). In the wurtzite structure, the group theory predicts eight types of phonons, $2A_1$, $2E_1$, $2B_1$, and $2E_2$, out of which $1A_1$ and $1E_1$ modes are acoustic and the rest are optic. Depending upon the scattering configuration, all or some of these optic phonons along with various combination modes can be observed in a Raman spectrum. Taking the z direction along the c-axis, an unpolarized scattering in the backscattering geometry can be described by the combined configuration [x(y,y)-x + x(y,z)-x], where the symbols, from left to right, outside the bracket indicate the direction of incident and scattered light and inside bracket indicate the polarization direction of incident and scattered light, respectively. Figure 1 shows a Raman spectrum measured from bulk GaN crystal in the [x(y,y)-x + x(y,z)-x] scattering configuration. The details of phonon structures between 520 and 580 cm^{-1} are displayed in the inset. The LO modes in Raman spectrum have very weak intensity, which indicates that the sample has large charge carriers, which screen the LO phonons. Although a phonon-plasmon coupled mode could not be observed, it was otherwise confirmed that the sample has a charge carrier density of about 10^{18} cm^{-3}. The low-frequency E_2 mode shows fairly small line width, indicating long lifetime. We could not observe the B_1 modes in our experiments, probably due to their weak intensities. Figure 1 displays all other first-order optic phonons and various combination modes along with their frequency positions. The origin of an unidentified mode assigned by asterisk (*) could not be understood at this time. Further, Raman scattering experiments were performed in various scattering configurations, where a weak E_1(LO) phonon mode was observed with z(x,x)-z scattering configuration, the A_1(TO) mode was observed in both x(y,y)-x and x(z,z)-x scattering configurations and the E_1(TO) mode was observed in both x(y,z)-x and x(y,z)y scattering configurations. The E_2 modes were observed in four different scattering configurations. Figure 2 displays Raman spectra between 520 and 580 cm^{-1} in three different scattering configurations. The assignment of all observed modes and their frequency positions are in good agreement with those reported earlier [2] for wurtzite GaN crystal, which was not bulk, but epitaxially grown crystal.

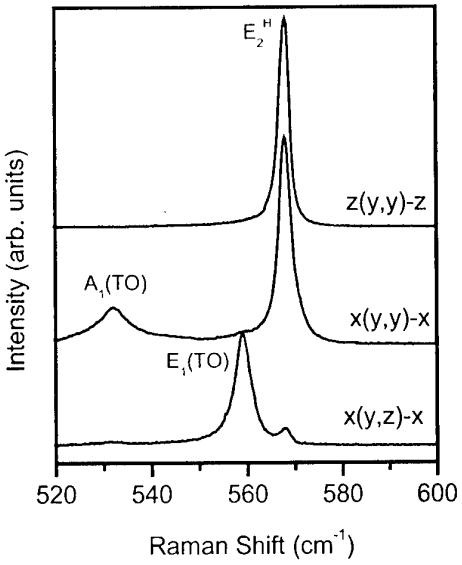


Fig. 1 Some of the Raman spectra in the spectral range of 520 to 580 cm^{-1} from bulk GaN in the indicated scattering configurations.

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Characterization of SiC band-edge absorption properties by free-carrier absorption technique with variable excitation spectrum

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Optical absorption at the edge of the fundamental bandgap is an important parameter for various characterization techniques where excitation effect is employed. In silicon carbide (SiC) optical excitation is relatively weak due to the indirect bandgap nature of this material, and therefore assessment of the band to band absorption coefficient α_{bb} becomes a complicated issue. Conventional methods like transmission or photo-thermal deflection can detect only the overall absorption of the incident radiation. Such measurements require thick samples, thus high quality but thin SiC epilayers appear to be beyond the sensitivity limits. On the other hand, available bulk SiC samples are usually moderately or heavily doped, making measurements of the intrinsic absorption edge strongly influenced by intra-band transitions of the extrinsic free-carriers. As a consequence, an intrinsic band tail and doping-induced band-gap narrowing in different SiC polytypes are not determined yet.

In this paper we present optically induced free-carrier absorption (FCA) as a sensitive tool to analyze spectral dependencies of the band to band absorption coefficient $\alpha_{bb}(h\nu)$ for photon energies $h\nu$ near and below the indirect band gap. The major advantage of this method is that absorption coefficient α_{bb} could be studied in high-quality low-doped SiC epilayers avoiding interference with the extrinsic free-carrier absorption. Another benefit comes from the fact that the FCA cross-section σ_{eh} for the IR-light used to probe SiC is rather large for a specific polarization [1] allowing the detection of very small absorption coefficients possible. Moreover, a linear relationship between FCA and the injected carrier density in SiC polytypes has been proven over a wide injection range (10^{13}-10^{19} cm^{-3}) and a wide temperature interval. In addition, due to a tight focusing of the probe beam down to a few microns relatively high spatial resolution could be achieved even for thin epilayer samples. The FCA technique with variable excitation spectrum has been already applied to crystalline silicon, where a perfect agreement between the measured and literature reported $\alpha_{bb}(h\nu)$ values has been obtained [2].

In this work, FCA measurements were performed on the high-quality (>500 ns lifetime at room temperature) free-standing 4H and 6H epilayers with extrinsic carriers concentrations of 10^{15} cm^{-3}. Perpendicular pump-probe measurement geometry has been applied as shown in the insert of Fig. 1. A short exciting laser pulse from a tunable optical-parametric-oscillator (OPO) penetrates the sample from the narrow facet. Excited free-carriers concentration is detected by the FCA of the 1.3 μm probe beam aligned parallel to the excitation surface. The advantage of such configuration is that both $\mathbf{E} \parallel \mathbf{c}$ and $\mathbf{E} \perp \mathbf{c}$ measurements can be performed while the polarization of the excitation light is rotated. The amplitude of the FCA signal is proportional to the photo-generated carrier density according to the relation: $\Delta\alpha_{FCA} = \sigma_{eh}\Delta n = I_o \cdot (1\text{-}R) \cdot \alpha_{bb}(h\nu) \cdot \exp(\alpha_{tot}(h\nu) \cdot x)$, where Δn is concentration of the excited carriers, I_0 - density of the incident phonons, R - reflectivity and x - the distance from the excited facet. The total absorption is $\alpha_{tot}(h\nu) = \alpha_{bb}(h\nu) + \alpha_{fc}(h\nu)$, where $\alpha_{fc}(h\nu)$ stands for an extrinsic free-carrier absorption and is assumed to be negligible in the vicinity of

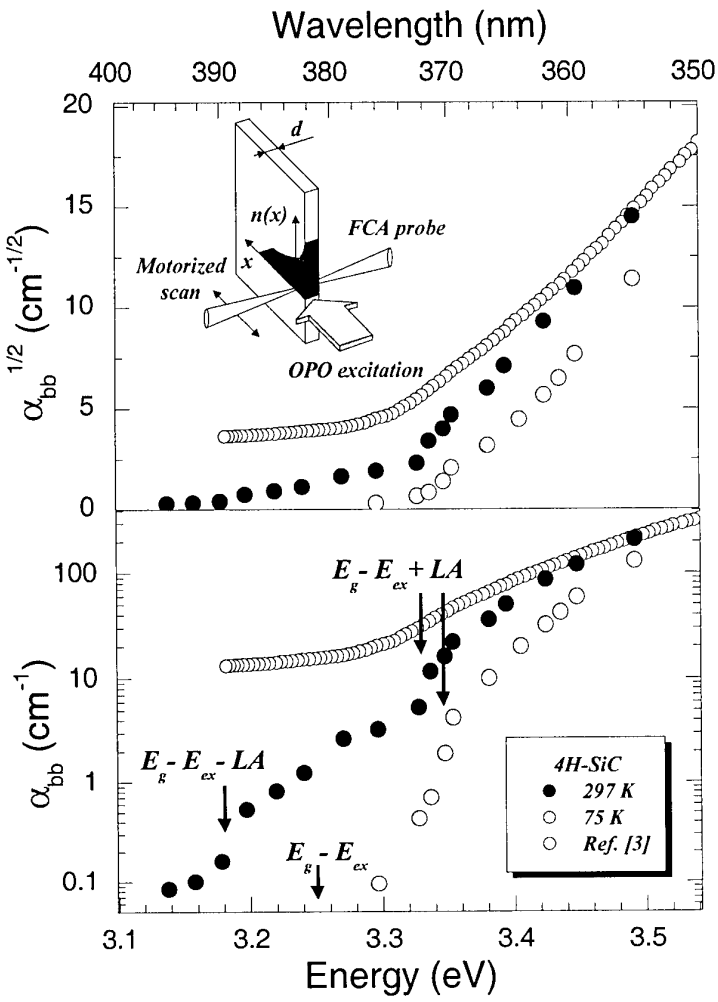


Fig. 1. Band to band absorption coefficient α_{bb} versus the excitation energy in 4H-SiC at 75 and 297 K. Inset - measurement geometry.

the injected facet, since $[\alpha_{tot}(h\nu)\cdot x] << 1$. More detailed considerations about the technique are provided in Ref. [2].

Fig. 1 shows the measured $\alpha_{bb}(h\nu)$ dependencies in 4H-SiC for **E** ⊥ **c** at the temperatures 75 and 297 K. In the high-energy range (>3.35 eV) the absolute α_{bb} values were extracted from the exponential penetration slopes. The low energy part of the spectra was determined in the vicinity of the excitation facet where the FCA amplitude $\Delta\alpha_{FCA}$ was calibrated with the high-energy α_{bb} values. Our data at high energies are comparable to those obtained by conventional transmission measurements for *n*-type 4H SiC boule slice with a doping concentration of about 10^{16} cm^{-3} [3] (open symbols in the plot). However, the low-energy side of these published spectra exhibits an interference with extrinsic free-carrier absorption due to the relatively high doping. In the same region around the band edge we are able to detect nearly two orders of magnitude smaller α_{bb} values. Despite the relatively low spectral resolution in our measurement (around 25 meV) the main sharp feature in our spectra at 75 K suggests the absorption step to the 76 meV *LA* phonon (loger arrow near the E_g–E_{ex}+*LA* indication). This most pronounce singularity was as well observed in the differential absorption spectra at 2 K [4]. At room temperature a wide tail rises up in the low energy side of the spectra and we assign this feature to the emission of the same *LA* phonons. Thus the middle point between two step features (indicated by E_g–E_{ex}+*LA* and E_g–E_{ex}-*LA* with short arrows) could be estimated as the excitonic band gap E_g-E_{ex} = 3.255 eV of the 4H-SiC which is in good agreement with a value extrapolated from PL measurement [5].

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TuA4 MOS -Mobility



Effect of Process Variations on 4H Silicon Carbide MOSFET Mobility

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The critical field for avalanche breakdown in SiC is about 10x higher than in silicon, so SiC unipolar power devices are theoretically capable of specific on-resistances about 400x lower than silicon devices. However, the on-resistance of 4H-SiC power MOSFETs reported to date has been limited by the resistance of the MOS channel, and not by the drift region. This is because of the low electron mobility in SiC inversion layers. Recently it has been shown that a post-oxidation anneal in nitric oxide (NO) can significantly reduce the interface state density in the upper half of the bandgap, with a corresponding improvement in mobility [1]. To determine the effect of processing variables on MOSFET mobility in 4H-SiC, we have conducted a comprehensive set of experiments that will be reported here.

Figure 1 illustrates the matrix of experimental conditions. The experiment consists of the following comparisons: (1) S/D implant anneal (1200 C or 1400 C), (2) oxidation procedure (Auburn or Purdue), (3) post-oxidation anneal (none or NO), (4) gate material (polysilicon or molybdenum), and (5) ohmic contact anneal (before and after). Nine samples are reported here. Samples A - F are fabricated on the same p-type epilayer wafer and oxidized at Auburn, while W - Z are fabricated on a second p-type epilayer wafer and oxidized at Purdue.

Figure 2 shows drain current vs. gate voltage for eight samples, with and without a post-oxidation anneal in nitric oxide (NO) at 1175 C for 120 min. The post-oxidation anneal in NO produces an order of magnitude higher drain current in all samples. Figures 3 and 4 show field-effect mobility μ_{FE} of samples oxidized at Auburn ***with*** (B, F) and ***without*** (A, E) the post-oxidation NO anneal. Suffixes (a) and (b) denote these samples ***before*** (b) and ***after*** (a) an 850 C ohmic contact anneal. The NO anneal produces a dramatic increase in field-effect mobility. The 1400 C implant anneal (E, F) does not significantly degrade the mobility as compared to the 1200 C anneal (A, B), and the ohmic contact anneal likewise has little effect on mobility. Figure 5 shows that the choice of gate material also has little effect.

Figures 6 and 7 show similar results for samples oxidized at Purdue. Suffixes (a) and (b) denote these samples ***before*** (b) and ***after*** (a) a 770 C ohmic contact anneal. The mobilities are slightly higher for the Purdue samples as compared to the Auburn samples, due possibly to slight differences in oxidation procedure. Since these are field-effect mobilities (as compared to effective mobilities), the drain current is proportional to the *integral* of μ_{FE} with respect to gate voltage. As shown in Fig. 8, samples W and X carry slightly higher drain current than B and F, even though at gate voltages of 20 V the mobilities are comparable.

Details of the oxidation and anneal procedures will be reported at the conference. Mobility measurements are performed by a new "constant current" technique that eliminates the effect of source and drain resistances. This technique will also be described at the conference.

This work is supported by ONR MURI grant N00014-95-1-1302 (Purdue) and by DARPA/EPRI grant MDA972-98-1-0007/W08069-05 (Auburn and Vanderbilt).

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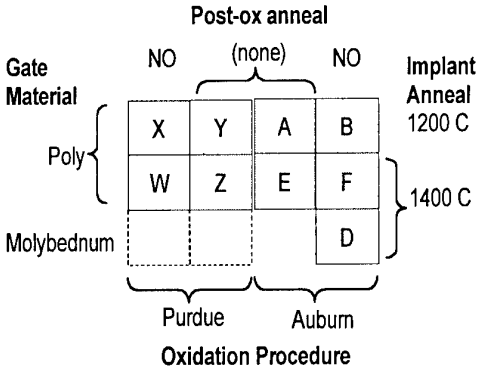


Fig. 1. Matrix of experimental conditions. Letters A - F identify samples oxidized at Auburn and W - Z designate samples oxidized at Purdue.

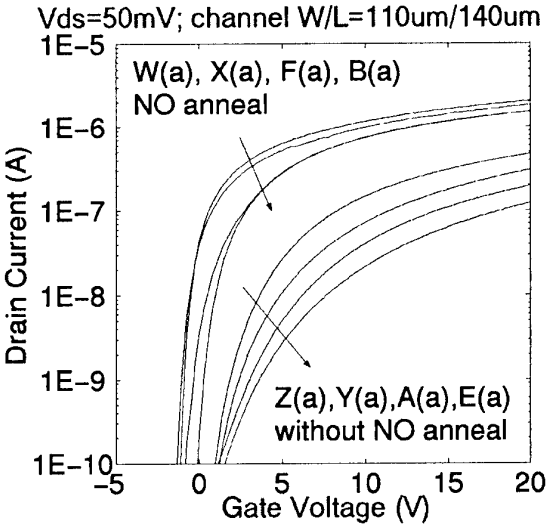


Fig. 2. Drain current vs. gate voltage for samples with a post-oxidation anneal in NO (upper curves) and without (lower curves).

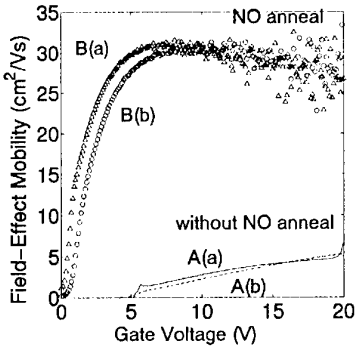


Fig. 3. 1200 C implant anneal, AU oxide, before (b) and after (a) an 850 C contact anneal.

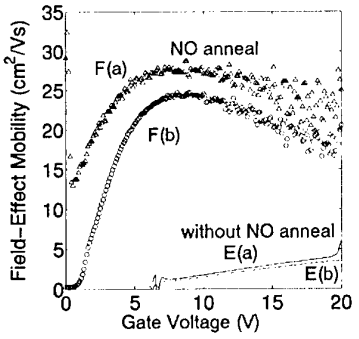


Fig. 4. 1400 C implant anneal, AU oxide, before (b) and after (a) an 850 C contact anneal.

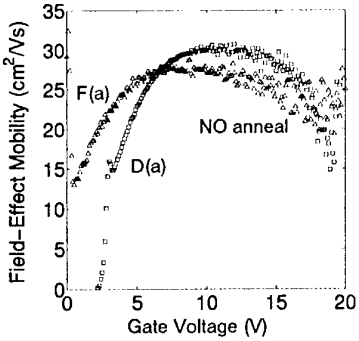


Fig. 5. 1400 C implant anneal, AU oxide, polysilicon gates (F) and molybdenum gates (D).

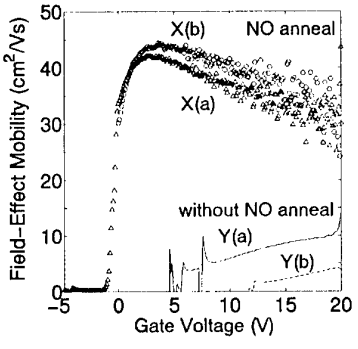


Fig. 6. 1200 C implant anneal, PU oxide, before (b) and after (a) a 770 C contact anneal.

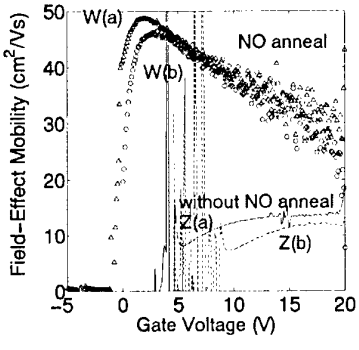


Fig. 7. 1400 C implant anneal, PU oxide, before (b) and after (a) a 770 C contact anneal.

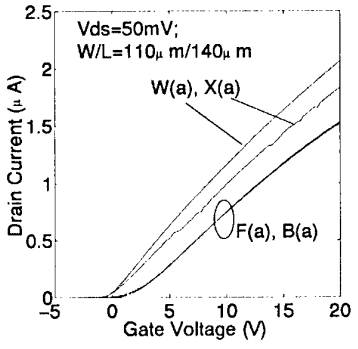


Fig. 8. Drain current at a drain voltage of 50 mV for samples W, X, F, and B of Fig. 2.

Improved Channel Mobility in Normally-off 4H-SiC MOSFETs with Buried Channel Structure

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4H-SiC metal-oxide-semiconductor field effect transistor (MOSFET) is a promising candidate for a high-power switching device. The most important problem for this device is to improve the channel mobility in the inversion layer. The reported channel mobility until now is extremely lower than the bulk electron mobility [1, 2]. It is generally believed that high density of interface traps at the SiO_2/4H-SiC interface degrades the channel mobility [3, 4]. One possible solution for the improvement of the channel mobility is to utilize the buried channel structure. In this structure, more electrons can flow away from the MOS interface. Threfore, the channel mobility may be significantly improved in 4H-SiC MOSFET. In this study, we have fabricated the buried channel MOSFETs on 4H-SiC. Oxidation conditions for the gate oxide and the doping depth of the buried channel region were optimized. The channel mobility of 140 cm^2/Vs was achieved in the normally-off 4H-SiC MOSFET.

The buried channel MOSFETs were fabricated on the p-type 4H-SiC (0001) wafer with an effective doping concentration (N_A-N_D) of approximately $5x10^{15}$ cm^{-3}. Figure 1 shows structural cross section of the MOSFET. The channel length and width were 100 and 150 μm, respectively. The buried channel region was formed by nitrogen ion implantation at room temperature and following activation annealing at 1500 °C. The nitrogen concentration was $1x10^{17}$ cm^{-3}, and the depth of the buried channel region (D_{ch}) after the gate oxidation were 0.15, 0.20, 0.25 μm. The gate oxide was grown by dry or wet oxidation at 1200 °C and following Ar annealing at the oxidation temperature. Some samples were then subjected to a wet re-oxidation at 950 °C for 3 hours. Aluminum was deposited as the gate and the source/drain contacts.

Figure 2 shows field effect mobility (μ_{FE}) as a function of gate voltage for the buried channel MOSFETs with the gate oxide processed by different condition. Drain voltage for this measurement was 0.1 V. The peak values are much higher than those in the inversion-type 4H-SiC MOSFET [5], indicating that the channel mobility is significantly improved by the buried channel structure. Threshold voltage (V_{th}) was extraced from $I_D^{1/2}$-V_G plot at V_D=10 V. Wet, dry/wet and wet/wet oxidation samples have positive V_{th} due to the normally-off operation. The highest μ_{FE} in the normally-off MOSFET is 140 cm^2/Vs for the gate oxide prepared by the dry/wet oxidation. Figure 3 shows the μ_{FE} as a function of gate voltage and D_{ch}. The gate oxide was formed by the dry/wet oxidation. The peak values for the D_{ch} of 0.15, 0.20, and 0.25 μm are 45, 140, and 230 cm^2/Vs, respectively. The V_{th} for the D_{ch} of 0.15 and 0.20 μm are positive values. These results reveal that the optimum D_{ch} for the normally-off buried channel MOSFET is 0.2 μm when the doping concentration is $1x10^{17}$ cm^{-3}. The channel mobility of 140 cm^2/Vs is the highest reported so far for normally-off 4H-SiC MOSFETs with a thermally grown gate oxide.

This work was performed under the management of FED as a part of the METI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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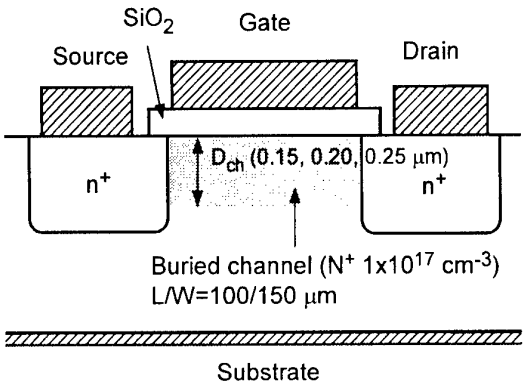


Fig.1. Schematic cross section of a 4H-SiC buried channel MOSFET.

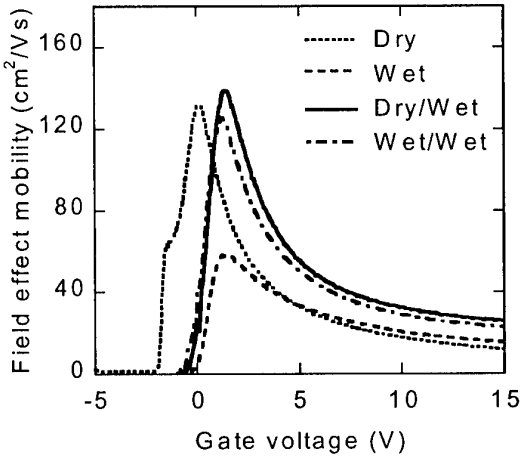


Fig.2. Field effect mobility as a function of gate voltage in the buried channel MOSFETs with the gate oxide processed by different condition. Drain voltage is 0.1V. The depth of the buried channel region and the concentration are 0.2 μm and $1x10^{17}$ cm^2/Vs, respectively.

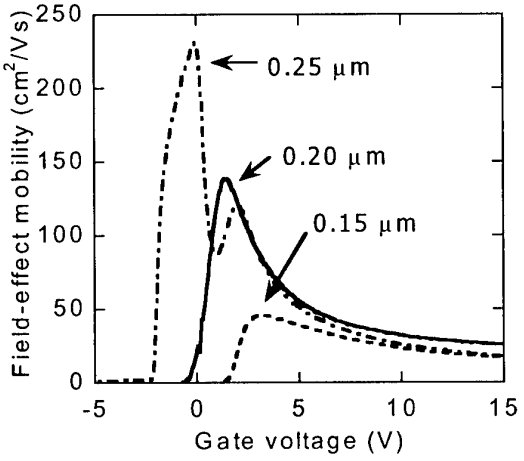


Fig.3. Field effect mobility as a function of gate voltage and depth of the buried channel region. The gate oxide is grown by dry oxidation and following wet re-oxidation.

Channel Engineering of Buried-channel 4H-SiC MOSFET based on the Mobility Model of the Oxide/4H-SiC interface

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In a buried-channel SiC MOSFET, it is indispensable to perform channel engineering by simulation in order to set threshold voltage at an appropriate value and to avoid the mobility fall near a SiC/oxide interface. In the simulation of MOSFET, it is important to set the proper mobility model at a semiconductor/oxide interface. However, the mobility model of a SiC/oxide interface has not been proposed until now. In this study, we modeled the mobility in the vicinity of the SiC/oxide interface, for the first time, from the experimental results of a surface channel SiC MOSFET and a buried-channel SiC MOSFET.

Figure 1 shows the field effect mobility of a surface channel SiC MOSFET. It should be noted that the electric field dependence of mobility is very small. Thus, we assumed that the inversion layer mobility is a constant of 25cm^2/Vs [1], and the degradation of mobility due to interface decays exponentially as the distance from the interface increases. Figure 2 shows the comparison of an experimental result and a simulation result with this mobility model. In this mobility model, the characteristic length (l_{crit}) of the mobility degradation due to interface is another important parameter. From the experimental results of a buried-channel SiC MOSFET, we try to calibrate l_{crit}, because the simulation results of a surface channel SiC MOSFET are almost independent of l_{crit}. Figure 3 shows the comparison of an experimental result of a buried-channel SiC MOSFET and a simulation result with the optimized l_{crit} of 30nm[2].

With this SiC/oxide interface mobility model, we performed channel engineering of a buried-channel SiC MOSFET. Figure 4 shows an example of an optimized new structure. A p layer is stacked between oxide and buried channel. Figure 5 shows the comparison of a simulation result of a p layer-stacked buried-channel MOSFET with that of a conventional buried-channel MOSFET. It can be seen that a remarkable increase of drain current is obtained in a p layer-stacked buried-channel MOSFET.

This work was performed under the management of FED as a part of the MITI NSS Program (Ultra-Low Loss Power Device Technology Project) supported by NEDO.

[1] S. Suzuki et al., submitted to Applied. Physics Letters
[2] S. Harada et al., to be published in IEEE Electron Device Letters

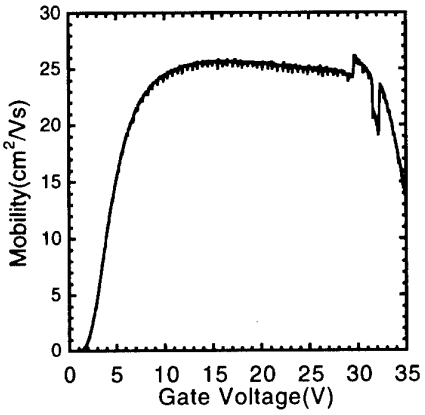


Fig. 1: Field effect mobility of surface channel SiC MOSFET.

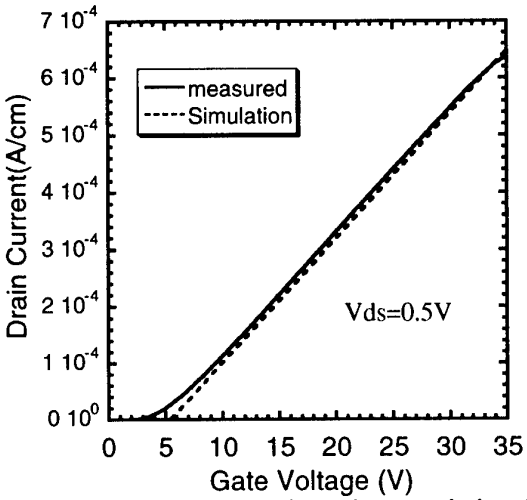


Figure 2: Linear region characteristics for the surface-channel MOSFET. Line shows the measured results and broken line shows simulated results wtih constant mobility model at the SiC/oxide interface.

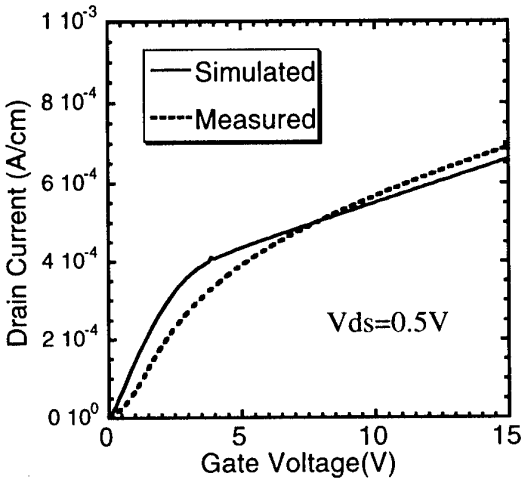


Figure 3: Comparison between the measured results of gate voltage versus drain current characteristics of buried-channel MOSFET and simulated results with optimized mobility model.

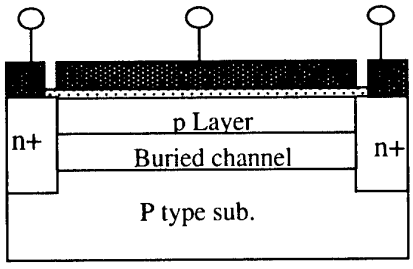


Figure 4: Schematic cross section of p layer- stacked buried-channel MOSFET.

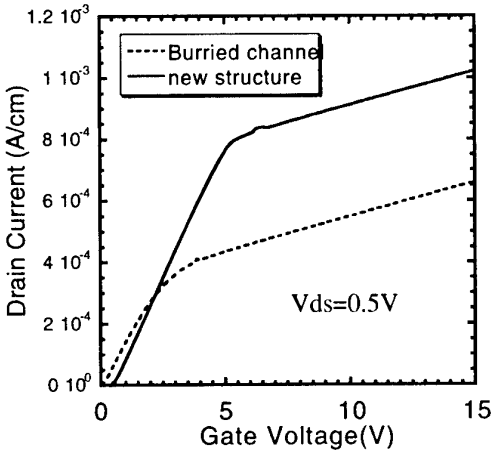


Figure 5: Comparison between the gate voltage vs. drain current characteristics of conventional buried-channel MOSFET and that of p layer-stacked buried-channel MOSFET.

4H-SiC MOSFETs on (03$\bar{3}$8) Face

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The selection of surface orientation is important for fabrication of MOSFETs on 4H-SiC, since a higher inversion channel mobility has been obtained on the (11$\bar{2}$0) face compared to the (0001) face[1]. In general, Si MOSFETs are fabricated on the (001) face, because the lowest density of interface states is obtained on the (001) face. The (0001) and (11$\bar{2}$0) faces of 4H-SiC (hexagonal crystal structure) correspond to the (111) and (110) faces of Si (cubic structure), respectively. The surface orientation which corresponds to the (001) face for the cubic structure is the (03$\bar{3}$8) face of 4H-SiC. 4H-SiC(03$\bar{3}$8) is the face tilted by 54.7° toward $\langle 01\bar{1}0 \rangle$ from 4H-SiC(0001) as illustrated in Fig.1. In this paper, the interface characterization of MOS capacitors and the MOSFET performance on 4H-SiC(03$\bar{3}$8) are reported for the first time.

4H-SiC(03$\bar{3}$8) substrates were prepared by slicing ingots grown by a modified-Lely method on (000$\bar{1}$) at SiXON Ltd. with an angle of 54.7° toward the $\langle 01\bar{1}0 \rangle$ direction. For comparison, 4H-SiC(0001) substrates were also examined. N-type and p-type epilayers were grown by CVD for fabrication of n-MOS capacitors and inversion-type n-channel MOSFETs, respectively (n-epi; N_d=3.1×10^{17}cm^{-3} for (03$\bar{3}$8), 8.9×10^{16}cm^{-3} for (0001), p-epi; N_a=9.6×10^{15}cm^{-3} for (03$\bar{3}$8), 1.1×10^{16}cm^{-3} for (0001)). After RCA cleaning, wet oxidation was carried out at 1150°C to grow a thermal oxide followed by in-situ Ar annealing at 1150°C for 30min. The oxidation time and resulting thickness were 25min and 70nm for (03$\bar{3}$8), and 120min and 50nm for (0001), respectively. The oxidation rate on (03$\bar{3}$8) was 6-7 times higher than that on (0001). The gate metal was Al for both MOS capacitors and MOSFETs. The gate length (L) and width (W) of MOSFETs were 50 and 200μm, respectively.

Figure 2 shows the distribution of interface state density (D_{it}) in n-type MOS capacitors estimated by a conductance method measured at room temperature. Though D_{it} on (03$\bar{3}$8) is larger than on (0001) at relatively deep energy ($E_C - E > 0.4$eV), MOS capacitors on (03$\bar{3}$8) indicate 3-5 times smaller D_{it} at shallow energy ($E_C - E$ = 0.1-0.2eV) than on (0001). In high-frequency C-V measurements, when the measurement temperature was cooled down from 300 to 100K, an increase of flatband voltage shift and hysteresis was small for MOS capacitors on (03$\bar{3}$8) while that was large on (0001). This result also revealed smaller D_{it} near the conduction band edge on the (03$\bar{3}$8) face.

All MOSFETs showed clearly the linear region and the saturation region. The drain current (I_D) - gate voltage (V_G) characteristics in the linear region (drain voltage (V_D) = 0.1V) are shown in Fig.3, in which I_D is normalized by the oxide capacitance (C_{ox}) to compare MOSFETs with different oxide thickness graphically. The higher drain current and steeper slope on (03$\bar{3}$8) in Fig.3 suggest that a higher channel mobility was obtained

by using the (03$\bar{3}$8) face instead of (0001) face in 4H-SiC. The threshold voltages determined from the onset of drain current in Fig.3 are also clearly different for both faces. A lower threshold voltage ($\sim$ 5V) was observed for MOSFETs on (03$\bar{3}$8) compared to MOSFETs on (0001) ($\sim$ 9V). Effective mobilities calculated from the slope of I_D-V_G curves in Fig.3 are plotted in Fig.4 as a function of the threshold voltage for corresponding MOSFETs. The maximum low-field mobility was 22cm^2/Vs for (03$\bar{3}$8) and 5cm^2/Vs for (0001) samples. The improvement in channel mobility by a factor of 3-5 was achieved by using the (03$\bar{3}$8) face in 4H-SiC. The temperature dependence of MOSFET performance and comparison of MOSFETs on (11$\bar{2}$0) will be presented at the conference.

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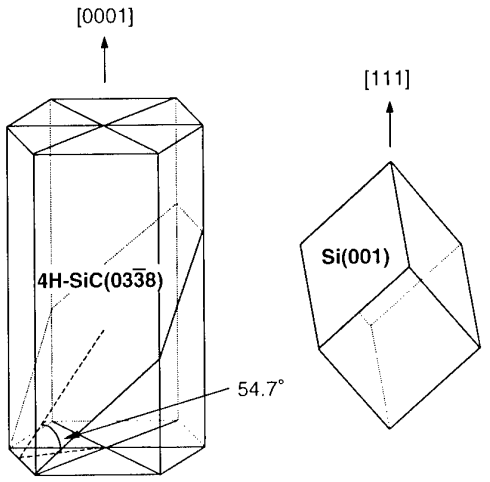


Fig.1: 4H-SiC(03$\bar{3}$8) and Si(001).

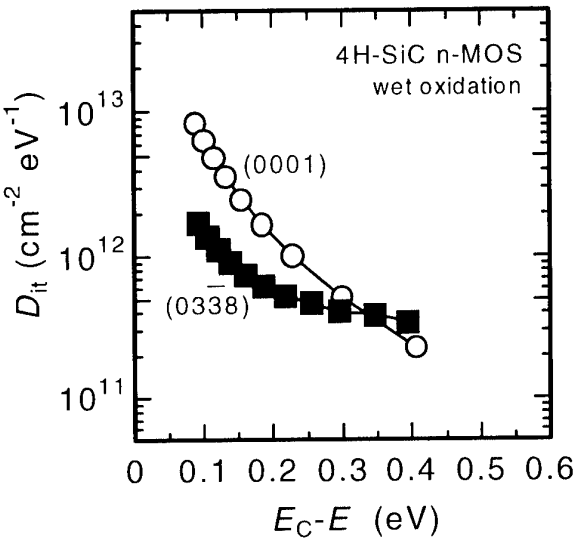


Fig.2: Interface state distributions.

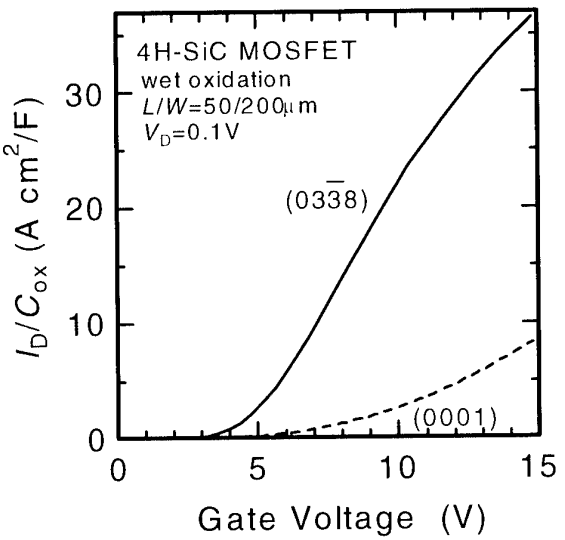


Fig.3: Linear-region I_D-V_G characteristics.

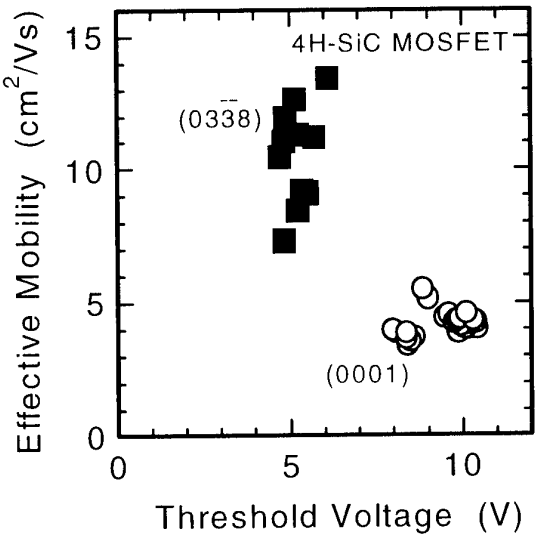


Fig.4: Relation between effective mobility and threshold voltage.

MISiCFET chemical gas sensors for high temperature and corrosive environment applications

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A silicon carbide chemical gas sensor has been under development in a co-operative effort between S-SENCE and ACREO [1-6]. The sensor is based on a field-effect transistor (FET), which was designed and processed by ACREO [1]. The metal insulator silicon carbide field effect transistor, MISiCFET, functions as a gas sensor by the application of catalytic gate metals, Pt, Ir. The device design is shown in Fig. 1. The source and gate of the device are connected to create a convenient two terminal sensor device. A voltage applied between the source and drain contacts causes a current to flow between these contacts through the buried channel region. The catalytic metal is placed over the channel region. Gas molecules in the atmosphere, which react with the gate metal will charge the gate region of the device and hence cause the concentration of mobile carriers in the channel to change. This in turn will shift the IV characteristics in a similar way to that shown in Fig 2. In order to promote high-temperature stability, the source, drain and channel region are buried. This moves the conducting path in the device away from the surface of the SiC, thus reducing the influence of surface effects. Batch number three of the devices has been completed and successfully tested in several applications at temperatures up to 600°C. The devices show excellent stability. Further testing of their performance limits is under way.

We have identified several applications in car exhausts where the excellent properties of SiC are a prerequisite. A cold start sensor needs to tolerate temperatures from -20°C to 1000°C and should even tolerate water splashes at its operation temperature (around 600°C). Promising results have been obtained to date. During Selective Catalytic Reduction of diesel exhausts, NO_x is reduced by NH_3 in the catalytic converter. An ammonia sensor for control of ammonia injection should not be contaminated by particulates and should show very low cross sensitivity to NO_x. The MISiC sensor operated at 300°C has demonstrated very promising results.

In flue gases a sensor array is needed to identify different modes of the combustion in a boiler. It is intended that a prototype version of a sensor system will be constructed, including software for control of the combustion process.

At the conference, typical results from the different applications will be shown.

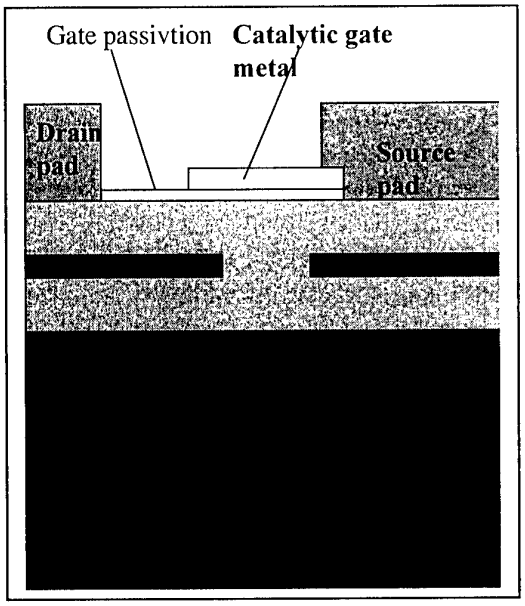


Fig. 1. . Cross-section of silicon carbide FET (MISiCFET) sensor with a buried gate design [1].

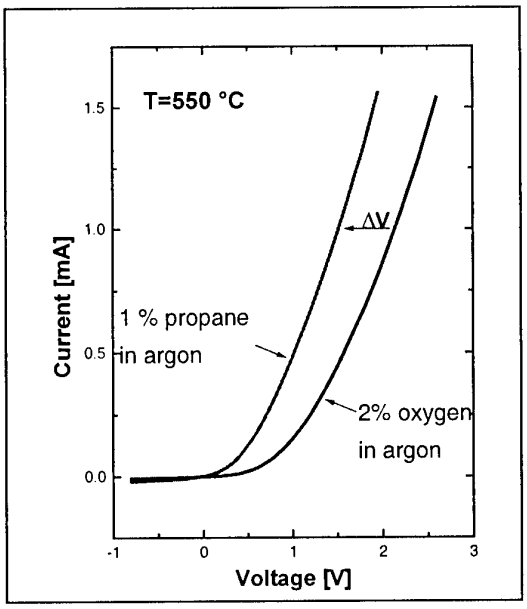


Fig. 2. Current voltage, IV, characteristics of a MISiC sensor. The voltage at a constant current is the sensor signal, which shifts in different gas ambients.

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4H-SiC Material for Hall Effect and High Temperature Sensors Working in Harsh Environment

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Silicon carbide is a well-known material for the fabrication of devices working in harsh environment. In this work we show that this material is also a good candidate to produce magnetic sensors working at high temperature [1].

The electrical properties of n-type, nitrogen-doped, 4H-SiC samples are well-known [2]. Recently we investigated a series of samples grown by AP-CVD, with carrier concentration ranging from 3.5×10^{15} cm^{-3} to 7.5×10^{17} cm^{-3}. A model was developed, which gives a complete description of the electron density and mobility as a function of temperature in the range 30 K to 900 K and doping concentration 10^{14} cm^{-3} to 10^{18} cm^{-3}.

In the framework of this model, we could determine the doping conditions in which (starting from room temperature) the material is working in the exhaustion regime. To be fulfilled, the doping level has to be lower than 5×10^{15} cm^{-3}. This is shown in Fig. 1.

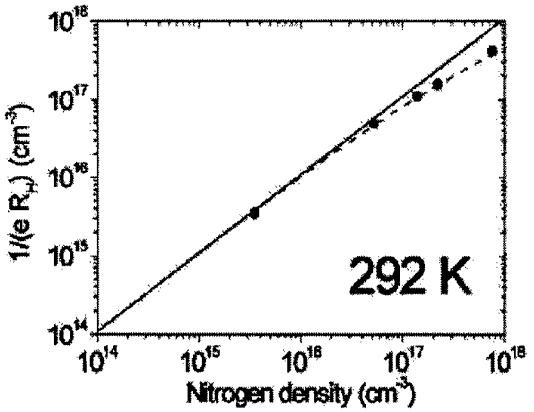


***Figure 1**: Hall electron density versus donor density. Full line - total ionization, dashed line – calculated values at 292 K, full circle – experimental data*

As prototype sensor, we have used a sample with 2.4 µm thick active layer doped at a concentration of 3.5×10^{15} cm^{-3}. The magnetic field sensitivity $K_H=1/(N_s\times e)$, in which N_s is the sheet carrier density, is K_{H0}= 930 V/A/T at room temperature. The temperature sensitivity S_T is only +75 ppm/K between 300 K and 550 K and -500 ppm/K between 550 K and 800 K (see Fig. 2). Such small values present a great advantage since no compensating circuit for thermal drift is needed for high temperature applications. They compare well with the one (-140 ppm/K) achieved in the case of metrology-type magnetic sensors based on III-V heterostructures between 230 and 380 K. Such stable structures with a GaAlAs/GaInAs/GaAs stacking are actually used for electrical metering applications[3].

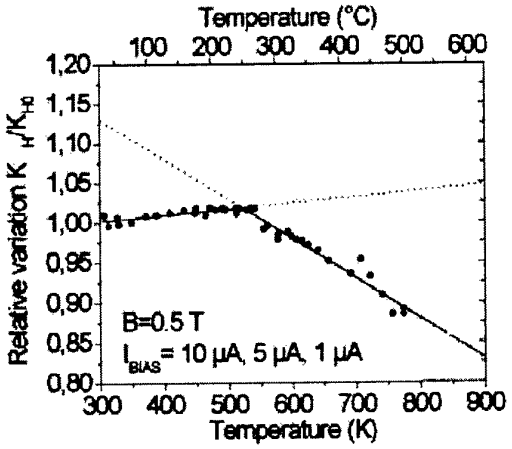


***Figure. 2** : Relative variation of the sensitivity K_H/K_{H0} of the sensor (experimental data – full circles). Lines show the thermal drift (between 300 –500 K: S_T= +75 ppm/K, between 500 –800 K: S_T= -500 ppm/K).*

When additional temperature knowledge is required, a bridge shape geometry can be used and, in this case, the input resistance of the device acts as a temperature sensor. In Fig. 3, we show the temperature dependence of the sheet resistance. The temperature sensitivity is equal to +3400 ppm/K between 500K and 800K.

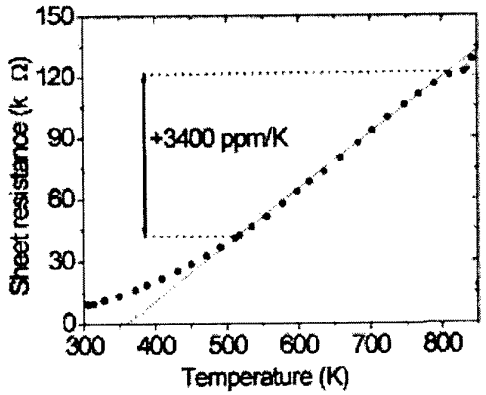


***Figure 3:** Variation of the sheet resistance versus temperature. The thermal sensitivity of the sheet resistance is +3400 ppm/K between 500 – 850 K. The solid line is a linear fit in this temperature range.*

As a result, using a well-suited geometry, we have found that the same component can be used for magnetic field and temperature measurements. Such monolithic structure avoids systematic errors introduced by temperature gradients inevitable when using two separated sensors.

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TuB4 Optical Properties 2



An Old Defect is Finally Understood and a New One Rises to Challenge Us

Part 1. Experiment and Theory of the Anharmonic Effect in C-H and C-D Vibrations of SiC

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Almost thirty years ago the C-H and C-D vibrations in polytypes of SiC were discussed in some detail [1-4]. At that time hydrogen in semiconductor was more of a curiosity than an important issue. Today, hydrogen in semiconductors in general and in SiC in particular is an area of important experimental and theoretical study [5,6]. With improved methods of crystal growth, ion implantation, spectroscopy and theoretical machinery we now revisit the anharmonic nature of the C-H and C-D vibrations in SiC.

Theory [6] has indicated that the V_{Si} + H complex is likely to be formed only in crystals where the Fermi level extends from the middle of the band gap to somewhere close to the valence band. This has not been fully confirmed by experiment but we believe that all the SiC used in these experiments was slightly p-type. Data is obtained from CVD films as well as boule and Lely crystals.

The C-H and C-D fundamental stretch modes and their higher harmonics observed here as vibrational replicas of bound exciton recombination can be discussed using a model based on the one dimensional Morse potential used by Fowler et al. [7] to analyze infrared OH stretch modes in insulators. Table I shows the measured energies of the fundamental and second harmonic of C-H and C-D stretch vibrations measured in a 6H SiC sample implanted with both hydrogen and deuterium. In the table the transitions are labeled $\Delta E_{nm} = E_n - E_m$ where the subscripts are the indexes of the energy levels of the anharmonic Morse potential. The two parameters ω and x are adjusted to precisely account for the energies of the fundamental and second harmonic of the C-H vibrations of H_3. The predicted values for the C-D fundamental and second harmonic are shown in Table I. The Morse potential accounts quite well for both the anharmonicity and the isotope effect. Table II lists the measured and predicted values for the C-H vibrations for the H_3 spectrum.

Table I

6H SiC:D,H	Data (meV)		Model (meV)	
Spectrum	ΔE_{10}	ΔE_{21}	ΔE_{10}	ΔE_{21}
H_3	369.5	353.6	369.5	353.6
D_3	273.7	264.7	273.9	265.3

Table II

6H SiC:H	ΔE_{10} (meV)	ΔE_{21} (meV)	ΔE_{32} (meV)
Data	369.1	353.5	337.7
Model	369.1	353.5	337.9

We have also carried out an ab initio density functional calculation for the V_{Si} + H complex in 3C SiC. The details of the calculation method and tools can be found in a paper by Aradi et al. [6]. To calculate the anharmonicity of the C-H stretch frequencies we use the method explained in Jones et al. [8]. The calculated energies of the second and third harmonics of the C-H vibrations are 349.6 meV and 335.1 meV in good agreement with the experimental values. The calculated anharmonicity parameter as it was defined in [8] is 14.5meV, close to the measured value of 15.6meV (using Table II). The calculations strongly support the fact that the measured H_1, H_2 and H_3 spectra in 6H SiC are indeed related to the fundamental and higher harmonic vibrational modes of the C-H bond in the V_{Si} + H complex.

Part 2. Spectra Associated with Stacking Faults in 4H SiC Grown in a Hot Wall CVD Reactor

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Bergman et al. [9] reported an interesting study on the effect of stressing hot wall CVD grown 4H SiC P-N junctions during extended high voltage testing. Of particular import to the work to be reported here is their finding of a new set of photoluminescence lines associated with areas of the junctions which are also found to have stacking faults after a long period of high voltage operation. We now report our findings of variations of this P-N junction spectrum in as grown films of 4H SiC and further evidence for their association with stacking faults.

The undoped epitaxial films of 4H SiC were grown at IKZ-Berlin in a hot-wall CVD reactor at about 1550°C and were about 30μm thick and in a vertical hot-wall reactor at Kyoto University and were about 70 μm thick.

How do our results compare with those of Bergman et al [9] in P-N junctions produced from hot-wall 4H SiC epitaxial films and also of approximately 30μm thickness? Dr. Bergman very kindly sent us a spectrum of the photoluminescence from a P-N junction with stacking fault features presumably induced by long term testing at high voltage. The spectrum was taken at 2K using a FreD laser. In our spectra, taken with a FreD laser we are in better agreement with the Bergman spectrum than those obtained using a He-Cd laser. We are in good agreement as to the temperature variation of this spectrum as well as to the relative decrease of room temperature lifetime in regions decorated by stacking faults.

We conclude that a number of spectra associated with stacking faults can be seen in hot-wall CVD grown 4H SiC. Possibly, the similarly observed spectra in P-N junctions exposed to long term high voltage operations were made on similar material as ours and the regions with spectra associated with stacking faults had these features amplified by the stress induced by the high voltage electrical testing. Finally, an interpretation of the nature of seven of these stacking fault spectra will be given.

We wish to thank NASA-Glenn Research Center (NAG3-2538) and ONR (N00014-01-1-0028) for partial support of this research.

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Characterization of bulk and epitaxial SiC material using photoluminescence spectroscopy.

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We are using low temperature photoluminescence (LTPL) to evaluate the quality of SiC wafers and are able to characterize up to 2 inch diameter wafers (with or without epilayers) at low temperature (2K).
Up-to six full wafers can be placed in a bath cryostat, which is mounted on a movable support. The luminescence excited either by the 244nm line or the 351 nm of an Ar^+ laser is dispersed by a single monochromator on which a UV sensitive CCD camera is mounted to detect rapidly the PL spectra.
At 2K sharp PL spectral lines are observed and their energy position depends on the particular polytype, which allows polytype identification (Fig.1) enabling us to draw some "polytype" map of wafers as shown in Fig.2. This technique is very useful when applied to low-doped semi-insulating wafers which are color-less, as opposed to highly doped material.
The dopants and residual impurities related LTPL lines (as such as Ti in Fig.1) can also be detected. For the nitrogen donor a quantitative analysis can be made.
For low doped material ($n < 3 \cdot 10^{16}$ cm^{-3}) the relative intensity between the nitrogen bound-exciton no-phonon line (such as Q_0 in 4H-SiC, see Fig.1) and one of free-exciton line (such as I_{76}) has allowed a quantitative estimation of the doping concentration [1]. This behavior has

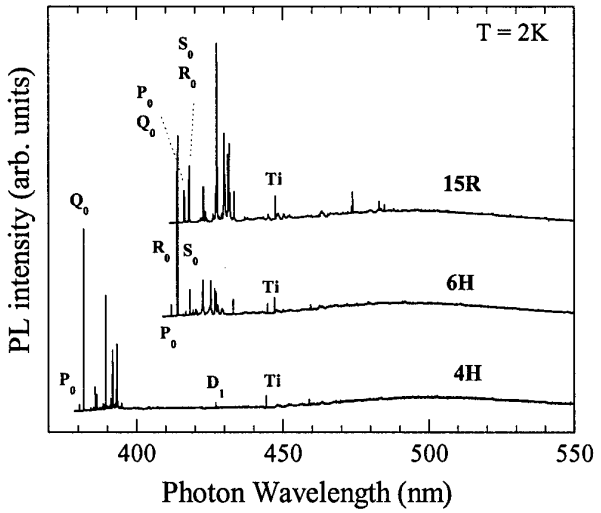


Fig.1 : PL spectra recorded on three bulk samples, at 2K showing three polytypes of SiC with low doping level ($n < 5 \cdot 10^{16}$ cm^{-3}).

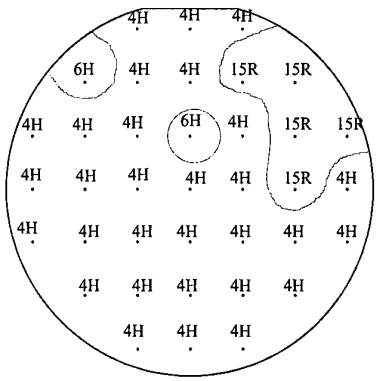


Fig.2: Polytype map of a substrate as determined from PL spectra at 2K.

been used to draw doping maps of 4H-SiC layers [2]. However this is limited to nitrogen concentration below $3 \cdot 10^{16}$ cm^{-3}. In this work we will shows that for medium doped samples ($1 \cdot 10^{16} < n < 3 \cdot 10^{18}$ cm^{-3}), the relative intensity between the two nitrogen bound-exciton no-phonon lines is correlated to the nitrogen doping concentration (see Fig.3). For highly doped 4H-SiC ($n > 5 \cdot 10^{18}$ cm^{-3}) a broad PL band (Fig.4) is observed which we recently have shown to be related to the heavy nitrogen doping itself [3]. The energy position of this band can thus be used for calibration of the doping concentration by comparison with data obtained by Secondary Ion Mass spectrometry. This behavior can also be used for bulk material to perform a nitrogen-doping map of the substrate.

This complete understanding of the near band gap emission for 4H polytype can be used and enables the determination of the nitrogen concentration by measuring the LTPL in the very large range of doping available today, e.g. from low 10^{14} to 10^{19} cm^{-3}.

Similar behavior is also observed for 6H-SiC material and will be presented.

Preliminary results for heavily Al-doped (p-type) epilayer show also the presence of a large band in the near band gap emission. Its energy position shifts towards lower energy with increasing doping, as in the case of n-type.

We will show that this knowledge is very useful for the understanding of the photoluminescence from thin epitaxial layer structures with various different epilayers such as MESFET structures, or from low doped epilayers when contribution from the substrate appears in the PL spectrum.

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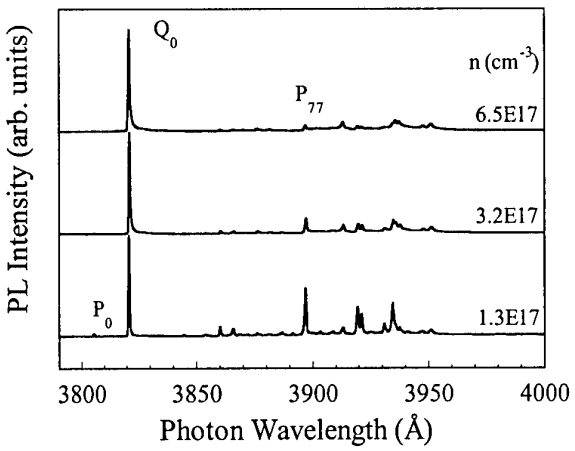


Fig.3 : PL spectra of medium doped 4H-SiC epilayers recorded at 2K

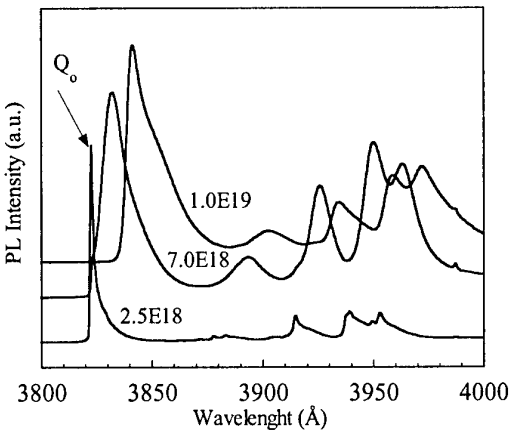


Fig.4 : PL spectra of heavely doped 4H-SiC epilayers recorded at 2K

Photoconductivity of Low-Doped and Semi-Insulating 4H-SiC and the Free-Exciton Binding Energy

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The free-exciton (FE) binding energy, E_{bx}, is a fundamental parameter, however, its exact value is far from being well established in any of the SiC polytypes. Values obtained in previous studies often do not agree (see Ref. [1] for a review), which determines the need in further experimental work employing techniques different from those used before. In a recent paper (Ref. [2]) we demonstrated the use of photoconductivity for studying the structure of the exciton absorption edge, and reported on the determination of E_{bx} in 6H-SiC. The purpose of the present work is to use similar approach for studying the structure of the excitonic bands in 4H-SiC, including the determination of the FE binding energy, as well as to develop further the interpretation of the photoconductivity spectrum near the fundamental absorption edge.

The basic idea behind the application of photoconductivity for finding the position of the conduction band edge (which coincides with the edge of the exciton continuum) is the electroneutrality of the excitons. Therefore, no contribution to the photocurrent from free excitons is expected, if the excitons are created by the exciting light in bound states (below the exciton continuum), whereas some current is anticipated if excitons are created in non-bound states (above the continuum). In this latter case, the electron and hole can be separated in the applied electric field before they form an exciton in a bound state, and thus contribute to the photocurrent. The threshold of this intrinsic photocurrent is at the conduction band edge E_g plus the lowest energy ($\hbar\Omega_0$) of a phonon insuring the momentum conservation in the light absortion process.

However, in real samples the threshold of the photocurrent occurs at the fundamental absorption edge (i.e., the excitonic bandedge plus $\hbar\Omega_0$). Thus even excitons created in bound states contribute to the photocurrent due to Auger recombination at impurities, as discussed in detail in Ref.[2]. Furthermore, this extrinsic photocurrent usually is much larger than the intrinsic one, so the latter is obscured (see Fig.1, sample B). However, in samples of exceptionally low residual doping, the extrinsic photocurrent is seen to saturate, and even decrease at higher photon energies, as shown in Fig.1 (sample A). This enables the observation of the intrinsic counterpart in the current, and also of additional thresholds in it due to involvment of different momentum-conserving phonons in the photon absorption process, as denoted by arrows in Fig.1. From the spectra, the free-exciton binding energy in 4H-SiC can be estimated to be in the interval 20 - 27 meV. This is close to the value of 20 meV, estimated in Ref.[3] from electroabsorption measurement. An estimation of this

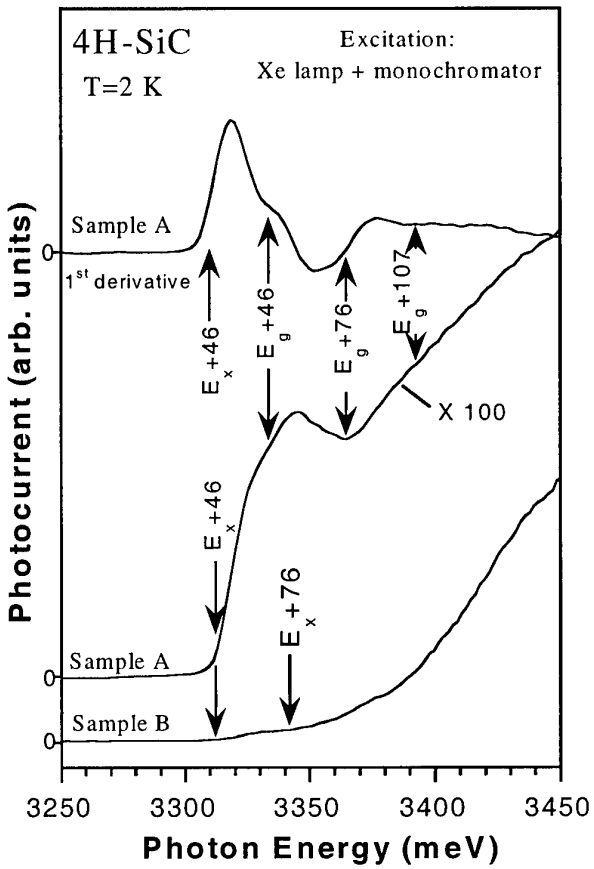


Fig.1. Comparison of the photoconductivity spectra of very low doped sample (A), showing saturation of the extrinsic photocurrent and contribution from the intrinsic one, and higher doped sample (B), dominated by the extrinsic photocurrent. The numbers above the arrows are the energies (in meV) of the main phonons assisting the light absorption. The derivative of spectrum A (on top) is provided in order to make more prominent the thresholds. Note the scale change for sample A.

quantity based on the isotropic hydrogenic model for 4H-SiC yields the value 34 meV, however, such calculation has very limited accuracy due to the high anisotropy of the electron and hole effective masses in 4H-SiC. Precise calculation accounting for this anisotropy are not available by now.

The reasons for saturation (and following decrease) of the extrinsic photocurrent are not simply in saturation of only residual impurity (as suggested previously in Ref. [2]), but are closely related to the presence of compensation. This is confirmed by the observation of saturation also in higher-doped (but compensated by deep levels) semi-insulating bulk 4H-SiC. The near-bandgap photoconductivity spectra of some highly doped semi-insulating samples do not show contribution from the intrinsic photocurrent because of the much higher rate of capturing of excitons. However, semi-insulating samples which exhibit free-exciton related emission in the low temperature photoluminescence spectrum, show also contribution from the intrinsic photocurrent. The photoconductivity properties of various semi-insulating samples is discussed in the paper. The temperature dependence of the photoconductivity spectra of various samples is also considered.

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UV Scanning photoluminescence spectroscopy investigation of 6H and 4H SiC

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Great progress have been made in the recent years in SiC bulk growth and epitaxy. Nevertheless, some problems still limit the rise of high performance and high reliability devices. In the case of SiC wafers, for instance, while the micropipes density has been strongly reduced down to 10 cm^{-2}, the dislocation density is still of typically 10^4 cm^{-2}. These defects, reproduced in the epitaxial layers, are deleterious for high power devices. Additionally, in the case of semi-insulating substrates, deep levels acting as carrier traps affect the devices performance [1]. For epitaxial layers, the main problem resides in the diminution of doping inhomogeneities exceeding 20% on a two inches wafer. The presence of polytypes inclusions in substrates as well as in epitaxial layers is also a recurrent problem in SiC wafers. In order to analyse these defects, to understand their origin and their impact on devices performance, non destructive and few time consuming characterization tools are strongly needed by the material growers.

For this tight quality control of the wafers, we have developed and adapted for the UV excitation a scanning photoluminescence (SPL) apparatus, initially conceived for III-V compounds analysis. Indeed the first reported results [2, 3] indicate that SPL is a very promising tool for SiC material characterization. In our equipment, the PL imaging is obtained by scanning the sample, fixed to an x-y stage with 1 μm minimal step. The excitation is provided by a doubled Ar^+ laser beam (244 nm) focused by an achromatic microscope objective (x52). With this excitation the spot diameter is about 2 μm and the penetration depth is below 1 μm in 4H-SiC. Nevertheless, one must keep in mind that the diffusion length of photoexcited carriers can be much more larger. In this case the spatial resolution is not limited by the apparatus but the material himself. The PL signal can be either directly collected, giving integrated PL intensity, either dispersed using a monochromator, giving spectrally resolved PL (1 nm of spectral resolution in the range 300 nm – 800 nm).

The optical signature of different defects have been investigated. For example, an exhaust of the photoluminescence intensity near the dislocations has been evidenced. This effect comes from the gettering effect of non radiative traps around dislocations which results in a denuded zone in the vicinity of the defect. From this observation, the density on epitaxial layers can be obtained without using chemical etching. The presence of micropipes can also be detected by photoluminescence mapping without using KOH etching. We will show that non emergent micropipes (not visible with optical microscope focussed on the surface) can be revealed. Some examples of polytypes mixtures on epitaxial layers (cubic inclusions) and bulk samples (4H and 6H distinct zone) will also be presented. An other application of SPL is the analysis of sample surface after different technological steps. Indeed, the PL signal intensity is very sensitive to the non radiative recombination at the surface. For example, we

have observed contrast inversion on etched surface (using RIE etching) before and after a H_2SO_4:H_2O_2 2:1 + HF cleaning. Before the cleaning, the integrated PL intensity is stronger on the etched zone. After cleaning, the PL intensity is strongly reduced and becomes lower than in the rest of the sample (Figure 1). The understanding of this effect is not clear yet. A possible explanation is that after etching, we collect a strong fluorescence from etching residue (polymerised carboxide group) which disappears after the cleaning.

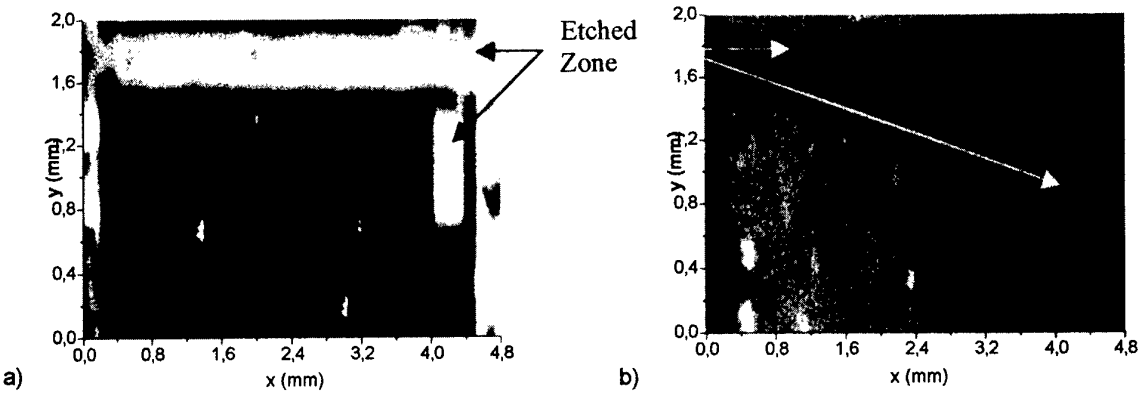


Figure 1 : a) Integrated PL intensity image of a MESA structure. The etched zone surrounding the central rectangle shows higher luminescence than the rest of the sample. b) Same image, after chemical cleaning. The etched zone has now a weaker luminescence.

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Photoluminescence Investigation of Hydrogen Interaction with Defects in SiC.

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Hydrogen interaction with donors and acceptors in SiC has been extensively investigated in the past. Hydrogen was shown to electrically passivate acceptors in 4H and 6H SiC.[1,2] Results of thermal admittance spectroscopy (TAS) measurements have shown that hydrogen can form complexes with both Al and B acceptors.[3] Hydrogen incorporation and out-diffusion were also investigated by monitoring changes in a PL emission attributed to a hydrogen-vacancy complex.[2,4] However, there were no successful attempts to correlate hydrogen-related processes in SiC with changes in acceptor-related photoluminescence. A possible passivation of lattice damage related defects with hydrogen also was suggested in the past[5] however no experimental data confirming this has been reported.

In this work, we investigated changes in hydrogen, aluminum, and lattice damage related PL lines in 4H and 6H-SiC samples subjected to hydrogenation in hydrogen plasma. Hydrogen incorporation in the epilayers was evidenced by appearance of H-related PL peaks (Fig.1). In addition a significant reduction in a relative intensity of Al bound exciton (Al-BE) photoluminescence in p-type epilayers occurred after hydrogenation (Fig. 1). It was also observed that the intensity of Al-BE PL in the hydrogenated sample was decreasing with time during the measurements. Prolonged excitation with above band-gap light caused a gradual reduction and finally a complete disappearance of Al-BE emission, which was accompanied with a slight increase of R_0+S_0 N-BE photoluminescence as shown in the bottom spectrum of Fig. 1. The kinetics of quenching of the Al-BE PL is shown in the inset to Fig. 1.

The possibility for passivateing lattice damage related defects with hydrogen was investigated by hydrogenating samples that had been implanted with nitrogen and annealed at 1500^{0}C to form D_I and D_{II} centers.[6,7] After the hydrogenation was performed under conditions that allowed the hydrogen incorporated in the epilayer to reach the depth of the maximum concentration of D_I centers, a significant reduction of the intensity of D_I photoluminescence with respect to the intensity of N-BE peaks was observed (Fig. 2). The stability of the passivated D_I complex was investigated by performing annealing at different temperatures. An annealing at 540^{0}C for 2 hr caused only partial recovery of D_I PL intensity (Fig. 2). The released hydrogen contributed to an increase of H-related PL as shown in the figure. A partial recovery of Al-BE PL was also observed after annealing at this temperature (not shown). Annealing at the higher temperature of 1100^{0}C for 1 hr caused further recovery of D_I PL, which was accompanied by a complete disappearance of H-related PL due to hydrogen outdiffusion from the epilayer (the bottom spectrum in Fig. 2). Also, the shape of Al-BE region of the spectrum was completely restored to its pre-hydrogenation form due to Al de-hydrogenation.

The observed changes in the Al-related and the D_I photoluminescence are attributed to a passivation of corresponding defects with hydrogen after the hydrogenation and to subsequent de-passivation of these complexes after the annealing. Possible mechanisms for the observed transient decay of the remaining Al-BE PL after hydrogenation caused by the light excitation are discussed in relation to

the recombination enhanced defect reaction.[8] Additional experiments are conducted to verify also a possible passivation of D_{II} centers that were formed after ion implantation and annealing.

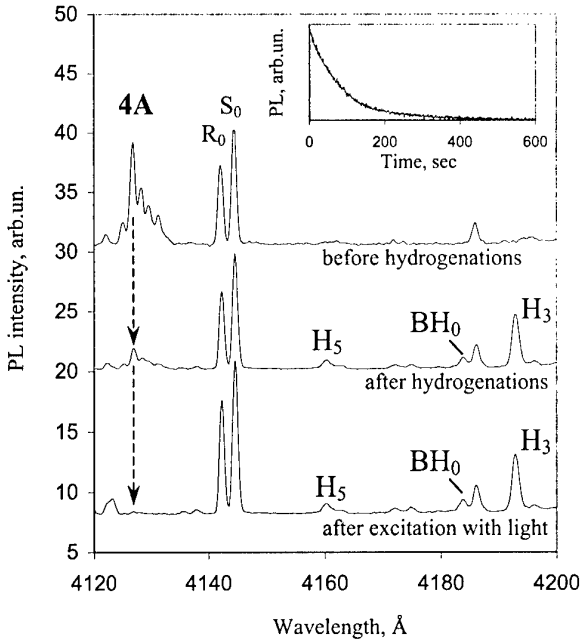


Fig. 1 Photoluminescence spectra before and after plasma hydrogenation, and after 40 min of excitation with above band-gap light. A reduction in 4A Al-BE PL line can be observed after hydrogenation. Light excitation caused further gradual reduction and disappearance of Al-BE PL line 4A. Quenching kinetics for 4A line under excitation is shown in the inset.

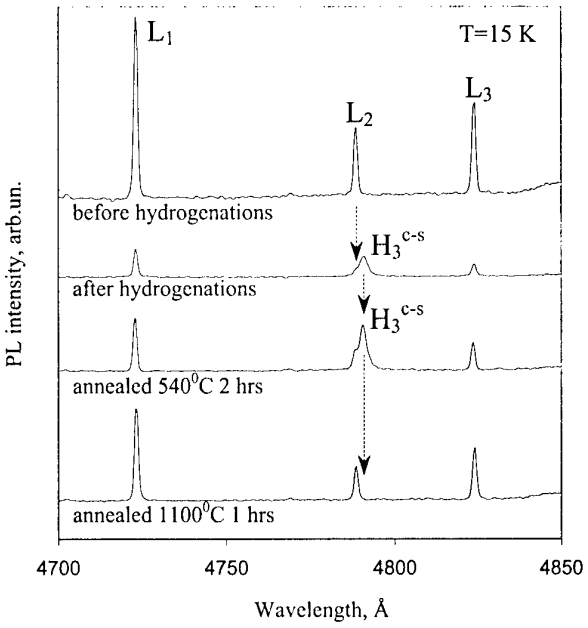


Fig. 2 Changes in D_I photoluminescence (lines L_1, L_2, and L_3) stimulated by hydrogenation and annealing. Hydrogenation caused significant reduction of D_I PL intensity and an appearance of the H-related PL (H_3^{c-s}). 540°C anneal stimulated partial de-hydrogenation of D_I centers accompanied with an increase of H-related PL. More D_I centers are de-passivated after 1100°C anneal, which is accompanied with a complete disappearance of H-related PL due to H outdiffusion from the epilayer.

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Properties of the UD-1 deep level center in 4H-SiC

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Deep levels have large impact on the electrical and optical properties of SiC. Besides the known deep levels with optical transitions in the infrared region such as vanadium, chromium and the silicon vacancy, there are a number of so far unidentified deep level centers. The UD-1 center (unidentified defect 1) in 4H SiC is one of the most interesting ones, since it gives rise to specific dominating infrared absorptions lines in semi-insulating HTCVD substrates[1]. This lines can also be found in the luminescence from commercial p-type substrates. The properties of the semi-insulating substrates have been studied after different annealing steps [2] and it is shown that the intensity of the UD-1 absorption increases after a 1600°C but it is unchanged after an 800°C annealing. Some of the optical properties and the electronic structure of the UD-1 defect in 6H-SiC were presented earlier [3] and indicate that the defect is either a substitutional defect or a complex along the c-axis.

More information of the defect is needed to understand the mechanism for how the semi-insulating material is compensated and which defect is the active deep level. Therefore we have in this study concentrated on the UD-1 defect in 4H-SiC. The measurements which earlier have been made on the 6H polytype are now also done in 4H together with new experiments such as photoluminescence excitation and absorption measurement at different temperature (from 2 K and up). The optical transitions of the UD-1 defect can be studied with both absorption and luminescence measurements. It consist of two sharp no phonon lines at 1.0585 and 1.0595 eV (Fig. 1.), the line width is less than 0.2 meV at low temperature.

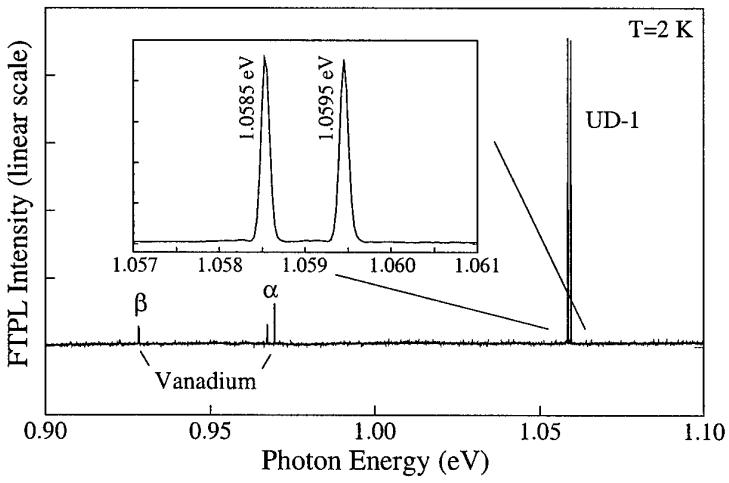


Fig. 1. FTPL spectrum of a semi-insulating 4H-SiC HTCVD sample annealed at 1600°C. Note that the vanadium FTPL is a factor 7 weaker than the UD-1 luminescence.

To be able to understand what role the UD-1 defect plays, the temperature dependence of the UD-1 absorption is studied. The absorption intensity is found to decrease with

increasing measurement temperature. At 80 K the absorption is completely quenched. From an Arrhenius plot of the temperature dependence of the intensity of the UD-1 absorption we can deduce that the thermal activation energy is less than 100 meV.

The Zeeman splitting of the UD-1 defect lines are presented in Fig. 2. The high energy line split into two lines and the lower energy line into four lines. The g values and the electronic structure for the defect will be presented.

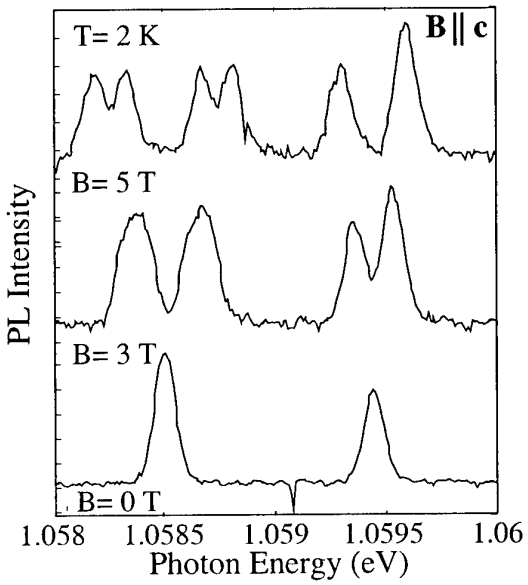


Fig. 2. The splitting of the two lines in the UD-1 defect at different magnetic field, with B parallel to the c-axis.

An isochronal annealing study of the UD-1 center will also be presented. The annealing behavior of the defect is investigated in detail between 800°C and 1600°C. This is important information to compare to how other defects in SiC behave at different annealings. It is also a result that could be used to compare the optical absorption signal to other measurement methods, such as EPR or DLTS.

The level scheme of the UD-1 defect and the annealing behavior of the defect will be discussed in detail in order to understand the origin of the absorption increase after high temperature annealing.

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WeA1 Bulk 1

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Growth-induced structural defects in SiC PVT boules

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The size and quality of silicon carbide crystals and wafers have been steadily improving over the last decade. Wafers with three inch diameter are now available commercially and the densities of micropipes, basal plane dislocations, and low angle grain boundaries have decreased by orders of magnitude. Nevertheless, the remaining defects can lead to significant yield loss of electronic devices and/or can severely degrade their performance. This presentation will present a concise summary of the currently observed extended defects in state-of-the-art SiC wafers with special emphasis placed on nucleation mechanisms active during the growth process.

There is an emerging consensus that the basal plane dislocations in SiC boules are due to the excessive thermal gradients imposed on crystal during growth. This effect can be additionally enhanced by the interaction of the growing boule and the graphite crucible. Arising long range thermoelastic stresses can exceed critical resolved shear stress and cause plastic deformation generating dislocations. Experimental evidence of basal plane slip active during growth will be presented and discussed. Threading edge dislocations can have several different origins including grown-in dislocations propagating from the seed wafers, plastic deformation associated with the prismatic slip system, and surface pinning of basal plane dislocations. The least understood is the origin of the elementary screw dislocations. New evidence indicates the connection between the nucleation of two dimensional islands on the (0001) growth surface and the formation of screw dislocations.

High growth temperatures used for the growth of bulk SiC crystals allow for relatively easy dislocation motion. This, in turn, leads to dislocations arranging themselves in characteristic patterns referred to as the domain structure or low angle grain boundaries. Two examples of such patterns (pure prismatic tilt boundaries and mixed prismatic and basal plane tilt boundaries) will be presented and discussed.

Sublimation grown SiC : growth modes, strains and defects

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In sublimation grown SiC crystals, structural defects may occur because of non-optimised growth initiation and also because of the relaxation of the embedded strain. A good understanding of these phenomena is a prerequisite for obtaining optimum quality crystals.
Firstly, and as commonly observed in epitaxy, the growth mode itself may be responsible for the occurrence of different types of defects. We have carried out a study of the growth front evolution in the early stages. It was found out that the two growth regimes, referred to as the 2-dimensional regime and the step-flow regime may occur simultaneously on different regions of the growth front. These depend upon the local temperature and upon the local surface misorientation. On the one hand, 2-D growth results into the formation of discrete nuclei which, upon coalescence, may give rise to some residual crystal mosaïcity. On the other hand, step flow growth is expected to be favourable in order to reproduce the underlying crystal structure. In this latter case, if the temperature is high enough, step bunching occurs, leaving wide terraces in between "macrosteps" where 2D growth can be favoured again. Figure 1 represents optical and AFM images of the SiC surface as seen at different magnifications.
Secondly, the evolution of the strain and mosaïcity in the crystal was followed by using either X-ray white beam synchrotron topography for assessing the whole crystal or monochromatic X-ray diffraction for assessing the structural quality of successive wafers from the same crystal. X-ray topography reveals that, if growth has been initiated properly, there is no drastic change in the crystal structure as growth proceeds. X-ray diffraction half width in the ω mode vary from 20 to about 80 arc sec., the higher value corresponding to the wafer taken from the wider part of the crystal from which one expects the higher concentration of thermo-elastic strains. Basal dislocations are commonly observed with a slowly decreasing concentration and c-aligned dislocations thread within the crystal with a density of about $10^4/cm^2$. Interestingly, if measured across a wafer, the threading dislocation density follows a variation which is the exact inverse of the variation of the strain (with a W profile), indicating that these dislocations are introduced in order to release the local strains rather than to compensate for mosaïcity (Cf.Figure 2). When used as a seed, the remaining strain in a wafer may be at the origin of a residual lattice misfit with the overgrown crystal; the misfit strain may be relaxed via the formation of "interfacial" dislocations which were analysed by TEM.

The optimisation of the growth initiation, the assessment of the growth regimes and the understanding of the different processes responsible for the strain and defect formation allowed us to obtain 4H crystals with state of the art structural quality.

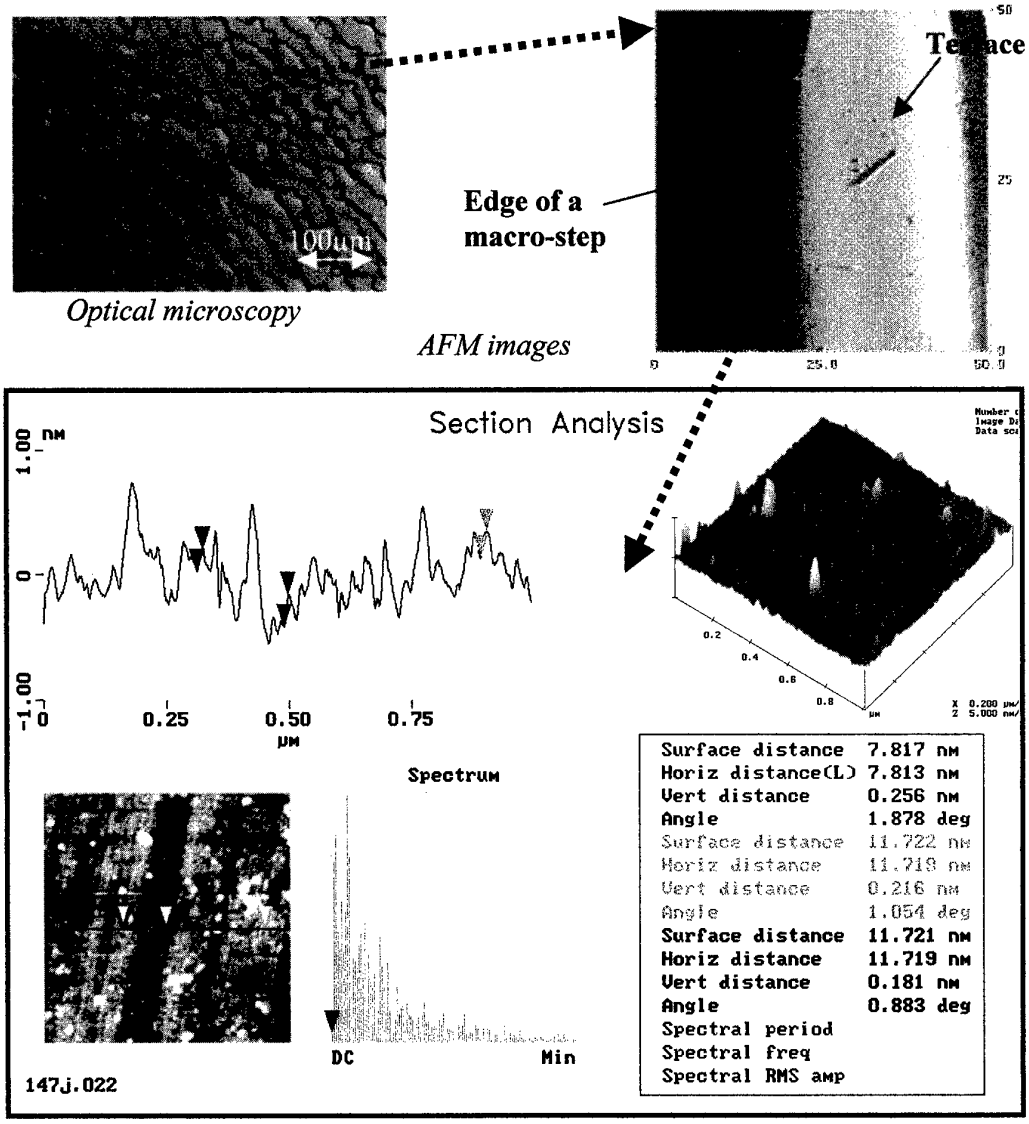


Fig.1. Surface morphology at the initial stages of growth: steps are visible at different scales

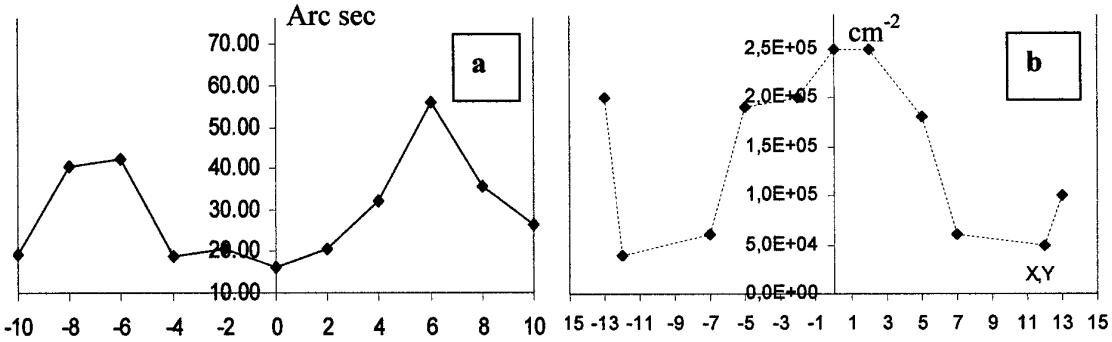


Fig.2. Relationship between the strain distribution (FWHM of the 2θ scan in arc sec, a) and dislocations density (in cm^{-2}, b). X –axis : distance from the center of the wafer on a diameter

On the Preparation of Vanadium-Doped Semi-Insulating SiC Bulk Crystals

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High resistivity, semi-insulating SiC single crystals are gaining more and more importance as substrates for high frequency electronic devices based on both SiC and GaN. Vanadium can act in SiC as a deep level for the electrical compensation of residual impurities. As nitrogen is the predominant impurity in nominally undoped crystals, V doping leads to the activation of the V acceptor level, resulting in a specific resistivity of about 10^{11} Ωcm at room temperature. Co-doping of V and a p-type dopant like Al or B is required to activate the almost mid-gap V donor level leading to specific resistivities up to 10^{15} Ωcm. In any case, the relatively low solubility limit of V in SiC must not be exceeded. For obtaining bulk crystals of semi-insulating SiC, doping homogeneity is crucial as will be discussed in this paper.

More than 30 bulk 6H-SiC crystals with 35...40 mm in diameter were grown by the modified Lely technique using on-axis seeds. The crystals were doped by boron, vanadium or B/V co-doped by adding solid sources to the SiC starting material. Results from the growth of nominally undoped crystals were taken as a reference. Here, nitrogen was found to be the residual impurity on a very low level, with charge carrier concentration n decreasing exponentially with growth time. Wafers with n as low as 8×10^{15} cm^{-3} were obtained. The dependence of seed polarity on nitrogen incorporation will be addressed. Assuming the residual impurity incorporation is the same for all of our growth experiments, the impact of impurity incorporation on electrical properties during doped SiC growth can be determined.

Tab. 1: Chemical analysis of the B concentration in the sublimation source and in the grown crystals for two experiments, measured both at the beginning and at the end of growth, respectively.

Boron [ppm wt.]		SiC powder	SiC crystal
B-doped #1	Start	2,7	2,0
	End	5,5	2,0
B-doped #2	Start	26,7	7,3
	End	5,4	4,6

The homogeneity of boron incorporation was measured by temperature-dependent Hall effect, absorption mapping and specific resistivity mapping. B incorporation was found to depend on seed polarity (growth on C or Si face). The hole concentration increases with growth time, whereas boron losses during growth lead to a decrease in the boron content of the source material (see Tab. 1). Compensation of boron by nitrogen impurity incorporation can explain this behavior only in the beginning of growth. A mechanism for the increase of hole concentration will be discussed. Also, the influence of dopant incorporation on crystal quality and defect nucleation was investigated with optical microscopy. Lateral homogeneity of a B doped wafer as measured with absorption mapping was as low as $\Delta p/p \approx 15\%$.

V incorporation was found to be related to partial pressure of the V species during growth. Additionally, V is incorporated in higher concentrations when growth on the Si face is

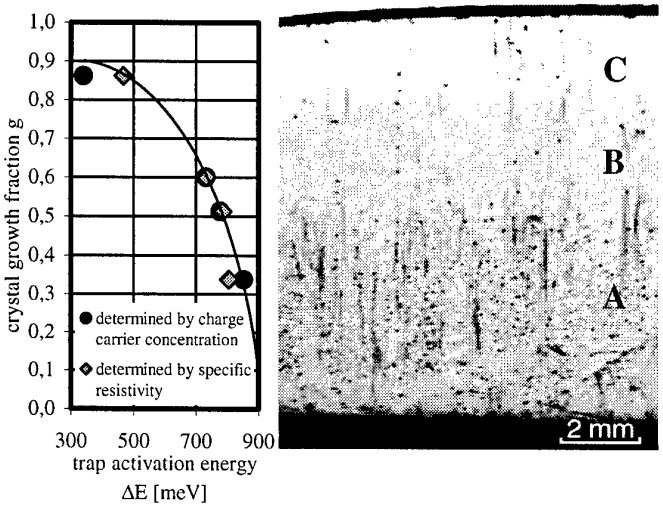


Fig. 1: Cross-sectional cut of a V doped SiC wafer (growth direction is upwards). On the left side, trap activation energies of the respective positions in the crystal are shown. For description of the regions A, B, C see text.

performed. As $p_{VC} > p_{SiC}$ at growth temperature, the V source depletes during growth. The obtained crystals exhibit axial and lateral inhomogeneities (see Fig. 1). When the V solubility limit of $3...5\times10^{17}$ cm^{-3} is exceeded, vanadium-rich precipitates form (Fig. 1, A), which were identified by EDX measurements. On the other hand, when the V source depletes, residual nitrogen becomes predominant leading to n-type conducting behavior (Fig. 1, C). By reducing V species evaporation rate, bulk SiC crystals exhibiting precipitate-free, semi-insulating behavior (Fig. 1, B) were obtained.

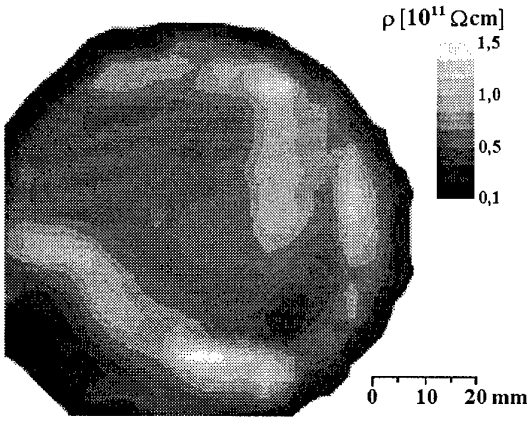


Fig. 2: Specific resistivity mapping on a V doped SiC wafer, obtained by the scanning capacitance method.

Characterisation of doping inhomogeneities and doping-related defects were carried out by optical microscopy and scanning electron microscopy. The electrical properties of V doped SiC crystals were measured by temperature-dependent Hall effect and by the scanning capacitance method. As a result, specific resistivities extrapolated to room temperature are about $2...8\times10^{10}$ Ωcm, while resistivity mappings reveal doping imhomogeneities (Fig. 2). The influence of V concentration and compensation ratio on the electrical behavior was analyzed. Optical absorption peak structures in the near infrared, which are attributed to inner shell transitions of V^{4+}, and electron spin resonance showing $^{51}V^{3+}$ were used to verify the compensation mechanism in the investigated crystals.

A combination of boron and vanadium doping allows growth of bulk SiC with a specific resistivity of $\rho_{293K} \approx 10^{15}$ Ωcm. First results on B/V co-doped SiC crystals show that boron and vanadium incorporation do not interfere with each other. Using the elaborated transfer coefficients for the dopants and their evolution of incorporation during growth time, semi-insulating bulk crystals of B/V co-doped SiC were obtained. Compensation behavior was studied using optical absorption. Specific resistivity mapping as well as temperature-dependent Hall effect measurements were used to determine electrical behavior and doping inhomogeneities.

Numerical Simulation of Heat and Mass Transfer in SiC Sublimation Growth

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Silicon carbide single crystal has been grown by modified Lely method in a closed carbon crucible. We have reported that grown crystal shape strongly depends on the temperature field, and it is possible to grow high quality crystal by modifying the temperature distribution inside a crucible[1]. We have demonstrated the high quality SiC single crystal growth by using a double-walled crucible[2]. Recently we demonstrated to grow SiC single crystal without poly crystal touching[3], and also proposed to grow high quality SiC single crystal by taking care of initial growth stage[4]. In those methods, the key technology is how to control the heat and mass transfer inside a crucible. In this paper, temperature and concentration field inside a closed carbon crucible was analyzed numerically, and effect to heat and mass transfer on grown crystal quality was discussed with comparing the experiment.

New crucible geometry to grow SiC single crystal separated from poly crystal was proposed.[3] Temperature distribution and mass flux was analyzed numerically. The grown crystal shape has strong relation with temperature distribution and mass flux inside a crucible. It was shown that by controlling them, grown single crystal shape could be controlled. This results shows that it is possible to control the macro crystal quality such as grown crystal shape by modifying the heat and mass transfer.

In-process etching was proposed as a new technique to reduce the defect density of grown crystal.[4] Temperature filed during that process, i.e. etching stage, quasi-equilibrium stage, and growth stage was analyzed. It was pointed out that SiC sublimation growth was composed of source–crystal mass transport and crystal-lid mass transport. Temperature distribution leads to decide which transport process is dominant. It was also shown that by taking care of temperature distribution on the seed surface, defect occurrence could be suppressed and high quality SiC single crystal could be grown. This results shows that it is possible to control the micro crystal quality such as defect density by modifying the heat and mass transfer particularly at the initial growth stage.

In conclusion, heat and mass transfer inside a crucible was analyzed numerically, and its effect on the macro and micro crystal quality was discussed with comparing the experiment.

This work was performed as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO, cooperating with FED.

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Self-Healing Phenomenon of Micropipes in Silicon Carbide

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Micropipes (MPs) are grown-in hollow tubes penetrating along the growth direction in Silicon Carbide (SiC) crystals. MPs have been also shown to have large Burgars vectors nc: b≥2c for 6H-SiC and b≥3c for 4H-SiC[1] where c is the lattice parameter and n is a positive integer. A unit screw dislocation (SD), namely, remains non-hollow core without the limits of the above magnitude. Therefore, we had believed that MPs would be diminished by decreasing the origins of SDs with large Burgars vectors[2] and reducing the magnitude of Burgars vectors. Recent reports presented the fabrication of SiC wafers with low MP density[3]. Yakimova *et al.* also found that MPs in seed crystal healed in grown layer during the liquid phase epitaxy (LPE)[4]. Note here that the feature of the methods is to reduce the MP density in new grown layers. On the other hand, we found the self-healing phenomenon of MPs in not new grown layers but SiC substrates. The self-healing of MPs was conducted by annealing the substrate with a material over the opening of MPs covered (Fig.1).

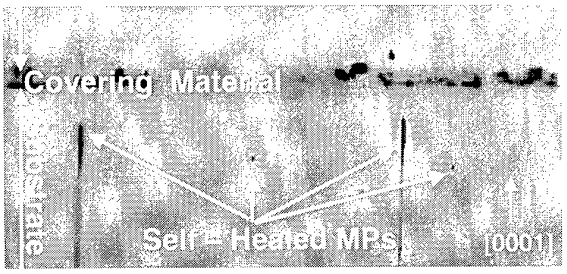


Fig. 1 Optical micrograph of a vertical sliced 6H-SiC substrate after annealing.

In this letter the self-healing phenomenon of MPs in SiC substrates has been preliminarily studied by means of the transmission electron microscopy (TEM) analyses and the optical observation, which is presented here for the first time. A TEM study in self-healed region revealed that some part of a hollow tube was transformed into non-hollow core which was composed of dissociated SDs, stacking faults and edge dislocations (Fig.2). There was also some strain in the self-healed region. Considering this experimental observation, one possible mechanism of the self-healing phenomenon of MPs will be discussed.

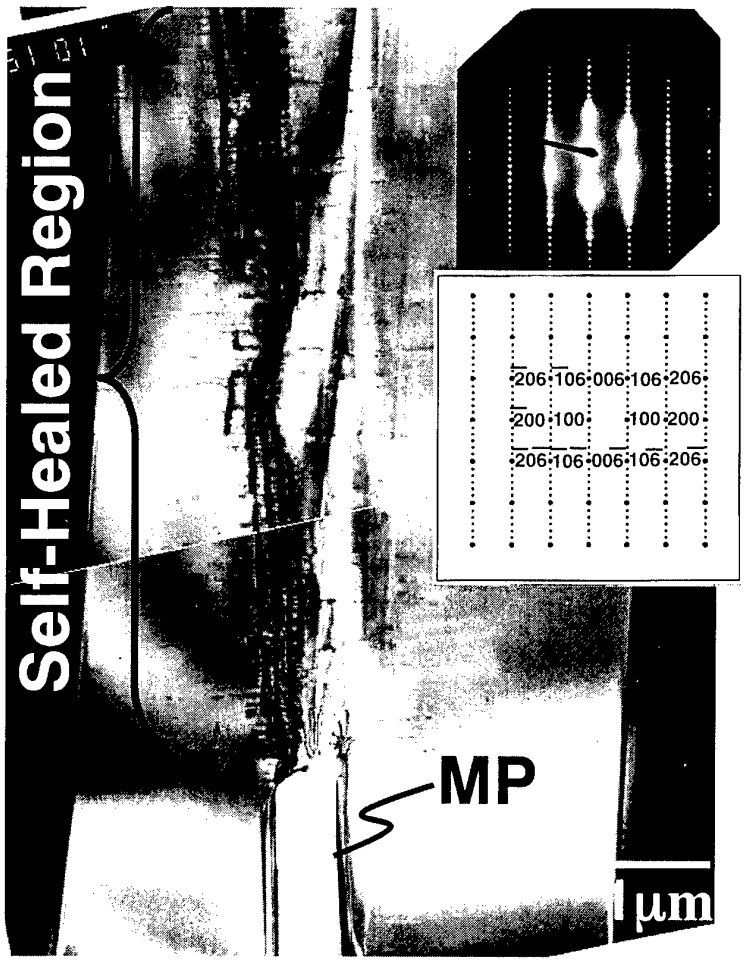


Fig. 2 Cross-sectional TEM bright-field image and diffraction pattern obtained from the annealed sample. Some part of a hollow tube has been transformed into non-hollow core with strains and mixed defects which consist of screw dislocations, stacking faults and edge dislocations.

Acknowledgment

The authors wish to thank Dr. K. Hara in DENSO CORPORATION for his helpful advice.

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WeB1 Electronic Structure



STRUCTURE OF NANOCRYSTALS IN HEXAGONAL SIC AFTER GE, SI AND ER IMPLANTATION

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Properties of bulk materials can be modified significantly if the material is manipulated at the nanometre scale. In particular, the growth of Si and Ge nanostructures constitutes a promising approach for the development of light emitting devices [1]. Hexagonal SiC is a promising matrix candidate because of its wide band gap. Techniques such as ion-implantation can be used to fabricate nanostructures in SiC [2, 3], in which effective interband transitions can be expected for Ge dots [4]. However only strained nanocrystals of defined uniform size (below 5nm) show significant quantum effects. Therefore basic structure determination of the nanocrystals is required.

The structure of nanocrystals in 4H and 6H SiC after Si 100keV, Ge 250keV and Er 400keV ion implantation and a fluence of ($1x10^{17}cm^{-2}$) at high temperature (700°C) followed by annealing at 1500°C and 1600°C has been investigated by advanced microscopy carried out in JEOL 3010, 2010F TEMs using high-resolution (HR) imaging, energy dispersive X-ray (EDX) spectroscopy, electron energy-loss spectroscopy (EELS) and high-angle annular dark field scanning electron microscopy (ADF-STEM) imaging. Digitally acquired HR images were analyzed to determine lattice fringe spacings within nanocrystals using the Diffpack plug-in from Digital Micrograph [5].

For the case of Ge and Er implantation, the nanocrystals have been revealed and their size distribution has been determined from Z-contrast images showing that the medium size is about 5nm with a distribution width from 2 to 10 nm. As results from lattice fringe spacing analysis of HRTEM images, main part of the Er-containing nanocrystals are unstrained $ErSi_2$ (P6/mmm) oriented with their c-axis parallel to the c-axis of the SiC matrix. For the case of Si implantation, hexagonal Si nanocrystals have been revealed with their c-axis parallel or inclined to the c-axis of

the matrix. The lattice fringe spacing analysis revealed nanocrystal strain of about 4 %. For the case of Ge implantation, GeSi crystals have been formed. Applying the strain value for the Si nanocrystals as a first approximation to the GeSi crystals, from the lattice fringe spacing analysis the Ge content could be determined and compared to results from EDX point analysis, EELS core level shift, and the ADF contrast (see the figure). Molecular dynamic (MD) simulations followed by high-resolution image simulations are carried out to investigate the strain state of the nanodots. Most nanocrystals revealed are strained hexagonal GeSi, with their c-axis parallel, inclined or perpendicular to the c-axis of the SiC matrix. For selected cases, the unoccupied densities of states for the GeSi nanocrystals have been obtained from EELS. Photoluminescence measurements on Er and Ge implanted specimens are carried out in addition.

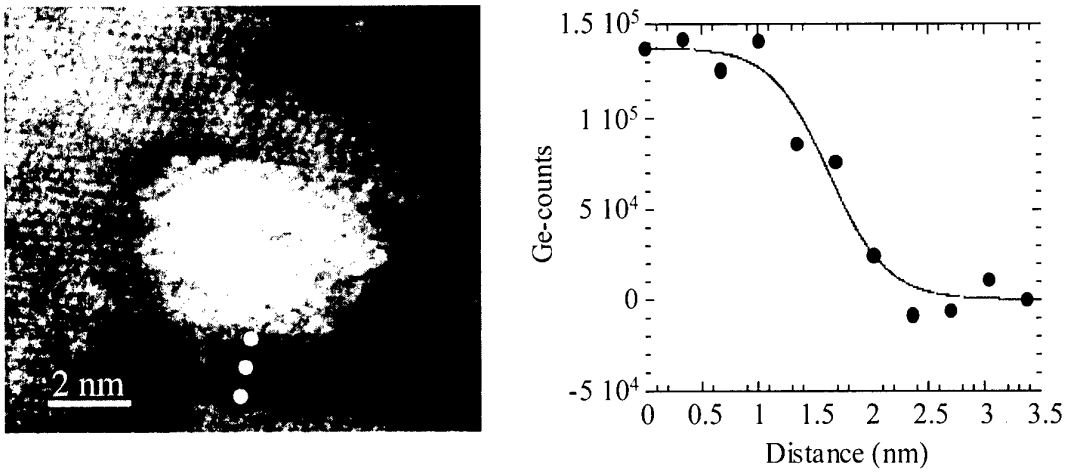


Figure Atomic resolution ADF-STEM image of a GeSi nanocrystal on the left and the Ge content along the dotted line obtained from EELS measurements.

The financial support of the Deutsche Forschungsgemwinschaft (SFB 196) is gratefully acknowledged.

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Hole and electron effective masses in 6H-SiC studied by optically detected cyclotron resonance

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The effective masses of electrons and holes in semiconductors are fundamental parameters, which are required for many analyses. The most direct method for determination of effective masses is cyclotron resonance (CR). The observation of a well-defined CR requires $\omega\tau>1$, with ω being the cyclotron frequency used in the experiments and τ the carrier scattering time. In SiC crystals available nowadays, the carrier mobility is rather low due to short carrier scattering time caused by high density of defects and residual impurities. It is therefore very difficult to satisfy the requirement of $\omega\tau>1$ for conventional CR experiments in SiC. Using optically detected cyclotron resonance (ODCR) with its advantages of improving the mobility due to photoneutralization of ionised impurities, we have previously been able to determine the effective masses of electrons and holes in 4H-SiC [1,2] and of electrons in 6H-SiC [3] at X-band (~9.23 GHz) and Q-band (~35 GHz) frequencies. However, in our previous studies [3], the electron effective masses in 6H-SiC were determined with a large uncertainty due to a very broad ODCR line width caused by short carrier scattering time. The hole mobility is often lower than that of electrons. This makes it difficult to satisfy the CR condition for holes, and therefore, the hole effective masses in 6H-SiC have not been experimentally studied so far.

In this work, we report our ODCR determination of the hole effective masses and more accurate effective mass values for electrons in 6H-SiC. Using high purity free-standing 6H-SiC layers grown by chemical vapour deposition with low concentration of residual impurities (N donor: ~4×10^{14} cm^{-3}, Al and B acceptors are below 10^{14} cm^{-3}), we have observed two well-separated ODCR peaks, which are labelled e-CR and h-CR and illustrated in figures 1(a) and 1(b). Complete angular dependencies of both ODCR peaks were obtained and analyzed. The angular dependence of the h-CR peak can be described by the usual cyclotron mass relation for the case of an elliptical energy surface, with the best fit values of the transverse mass $m_{\perp}(h)=(0.67\pm0.01)\ m_0$ and the longitudinal mass $m_{\parallel}(h)=(1.85\pm0.03)\ m_0$. The principal axis of the ellipsoid is parallel to the direction of the c-axis. Considering all possible alternatives, this ODCR signal can only be attributed to the CR of the hole. These values are similar to the hole effective masses in 4H-SiC [$m_{\perp}(h)=0.66\ m_0$ and $m_{\parallel}(h)=1.75\ m_0$] [2] and are close to the calculated values by Persson et al [4] with taking into account the polaron effect [$m_{\perp}(h)=0.65\ m_0$ and $m_{\parallel}(h)=1.80\ m_0$]. At low microwave power (~3.1 mW), no noticeable changes in the position or the line shape of the h-CR peak could be detected when rotating the magnetic field in the (0001) plane. This indicates that the hole effective mass is isotropic in the basal plane and the valence band close to its maximum is parabolic.

The e-CR peak is related to the CR of electrons. For the first time, a complete angular dependence of the e-CR has been obtained. When the magnetic field approaches the direction perpendicular to the c-axis, the peak moves to high magnetic fields and becomes very broad [the line width at half maximum is about 145 mT as can be seen in Fig. 1(b)]. Because of the

line broadening, it was not possible to resolve the anisotropy of the electron effective masses in the basal plane as predicted by theory [4]. The analysis of the angular dependence is therefore based on the model of an elliptical energy surface with the transversal mass, $m_\perp(e)$, being the average of the mass components in the basal plane and the longitudinal mass, $m_\parallel(e)$, is the mass along the direction of the c-axis. The obtained elecron effective masses are $m_\perp(e)=(0.48\pm0.01)\ m_0$ and $m_\parallel(e)=(5.65\pm0.15)\ m_0$. This $m_\perp(e)$ value is slightly larger than the value previously determined [$m_\perp(e)=0.42\ m_0$] in Ref. 3. The value determined in our previous work [3] is not so accurate (due to a small $\omega\tau$ value of only ~1.2, the OCDR peak is not well defined). The $m_\parallel(e)$ value of 5.65 m_0 in this case is much larger than the value $m_\parallel(e)=(2.0\pm0.2)\ m_0$ that we obtained before [3]. It is likely that in our previous work [3], the broad CR peak, which obtained at the magnetic field directions close to the direction perpendicular to the c-axis, was the CR of holes but not electrons (in this direction of the magnetic field, the CR of electrons may be not observable due to too short scattering time).

The influence of the polaron effect on the electron and hole effective masses in 6H-SiC will be discussed.

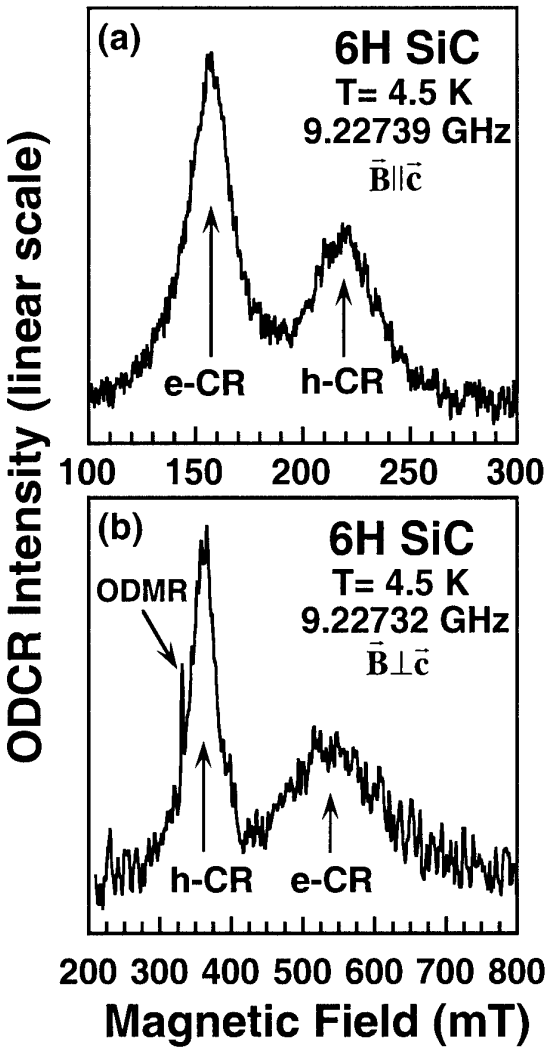


Fig. 1. ODCR spectra observed in 6H-SiC with monitoring the near band-edge luminescence for the magnetic field **B** (a) parallel and (b) perpendicular to the c-axis ($\mathbf{B}\|[11\bar{2}0]$). The peaks corresponding to the cyclotron resonance of the electrons and holes are labelled e-CR and h-CR, respectively. The microwave power is (a) 0.1 mW and (b) 3.1 mW. The sample was excited by the 334.5 nm line of an Ar ion laser with a power of 5 mW and the beam was defocused to a large spot on the sample. The sharp peak near 330.5 mT is related to an optically detected magnetic resonance (ODMR) signal of a defect.

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Photoreflectance Characterization of GaNAs/GaAs Multiple Quantum Well Structures

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Nitrogen containing III-V alloys like GaNAs have drawn considerable attention recently because of their interesting physical properties and a wide range of possible optoelectronic applications. However fundamental properties such as the bowing parameter, effective masses, the band alignment and the electronic states in the heterostructure systems are not well understood. There are still discrepancies among different experimental results and different theoretical predictions. Further experimental studies are needed. We report the photoreflectance (PR) spectroscopy studies of the GaNAs/GaAs multiple-quantum-well (MQW) structures at various temperatures.

The investigated structures were grown by the MOCVD. The MQW structures consist of 20 periods of GaN_xAs_{1-x}/GaAs layers. The GaAs layers were all 25 nm thick. The nitrogen compositions of the GaN_xAs_{1-x} layers in different MQW structures were varied up to x=0.04, and their thickness were 10nm or 6nm. A tungsten-halogen lamp with a monochromator provides the probing photons for the PR spectroscopy. The 514 nm line of an Ar^+ ion laser through a light chopper provides the pumping photons to generate electron hole pairs for the internal field modulation. Using the phase lock-in technique, the electro-modulated optical responses of the excitonic transition are enhanced, and the band edge transition exhibits Franz-Keldysh oscillatory (FKO) features whose period indicates the strength of the internal field. These spectral characters make the PR experiment one of the best spectroscopic probe for the electrooptical properties.

The PR spectra from different GaNAs/GaAs (MQW) structures at 75K are compared in the Fig. 1. Although the band gap energy of GaN is larger than that of GaAs, the GaN_xAs_{1-x} alloy show a considerable red shift of the band edge with increasing nitrogen concentration for low x-values. Instead of being barriers, the GaN_xAs_{1-x} alloys become wells in the GaNAs/GaAs (MQW) structures under investigation, and the excitonic interband transitions of the MQW systems were observed in the spectral range above $h\nu = E_g$ (GaN_xAs_{1-x}) as indicated in the Fig.1. Comparing spectrum (a) and spectrum (b) from MQW structures with the same nitrogen composition (x=0.04) but of different well width, the MQW transition

features are blue shifted while the well width reduced from 10 nm to 6 nm as shown in Fig.1. The blue shift is also observed when nitrogen composition is reduced from x=0.04 to x=0.017 as shown by spectrum (a) and spectrum (c) in Fig.1. A matrix transfer algorithm was used to match the GaN_xAs_{1-x}/GaAs boundary conditions and calculate the MQW subband energies numerically. The bowing parameter, effective masses, and the band-offset values were adjusted to obtain the GaN_xAs_{1-x}/GaAs MQW subband energies to best fit the observed optical transition features. These fundamental parameters are important for further studies of the optoelectronic properties of the GaNAs heterostructure quantum systems.

The oscillatory features labeled FKO(GaAs) and FKO(GaNAs) are the FKO cause by the pumping photons induced modulation of the internal electric field in the GaAs region and that in the GaN_xAs_{1-x} region respectively. The extrema in the FKO features of an electro-modulated spectrum are given by

$$n\pi = \phi + \frac{3}{4}\left[\frac{(E_n - E_g)}{\hbar\Theta}\right]^{3/2}, \quad (1)$$

Where n is the index number of the nth extrema, ϕ is an arbitrary phase factor, E_n is the photon energy of the nth oscillation extrema, and E_g is the band gap energy. The electrooptical energy $\hbar\Theta$ is defined by $(\hbar\Theta)^3 = e\hbar^2F^2/(2\mu)$, where F is the internal electric field, and μ is the reduced interband effective mass. A plot of $(E_n - E_g)^{3/2}$ versus n yields a straight line with a slop proportional to the internal electric field. The composition and the temperature variations of the internal electric field are analyzed.

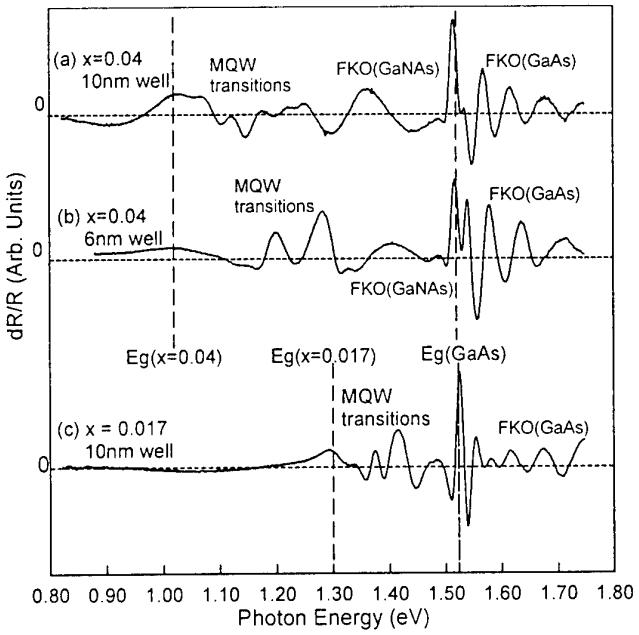


Fig1. Comparison of the PR spectra of GaNAs/GaAs MQW with different well witdths and N compositions x.

PHOTLUMINESCENCE AND ELECTROLUMINESCENCE CHARACTERIZATION OF InGaN/GaN MULTIPLE QUANTUM WELL LIGHT EMITTING DIODES STRUCTURES

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InGaN/GaN multiple quantum well (MQW) structures are currently of significant interest due to their application for the active region in blue-violet light emitting diodes and lasers. We report on optical studies, photoluminescence and electroluminescence, of heterostructures consisting of four InGaN quantum wells (QWs) (content of In is 11 %) grown on top of a GaN layer with micrometer-sized mass-transport areas [1]. Ti/Au and Ti/Al were used as contacts for anode and cathode, respectively. PL emissions are measured through the semitransparent top contact. The diode structure shows good structural and optical properties.
The combination of electroluminescence with photoluminescence using pulsed excitation provides an efficient methode to separately measure the contribution from the optical and the electrical injection, by synchronized time integration of the emission with the pulsed laser excitation. Using the pulsed optical excitation we have also studied the time decay of the different emissions.

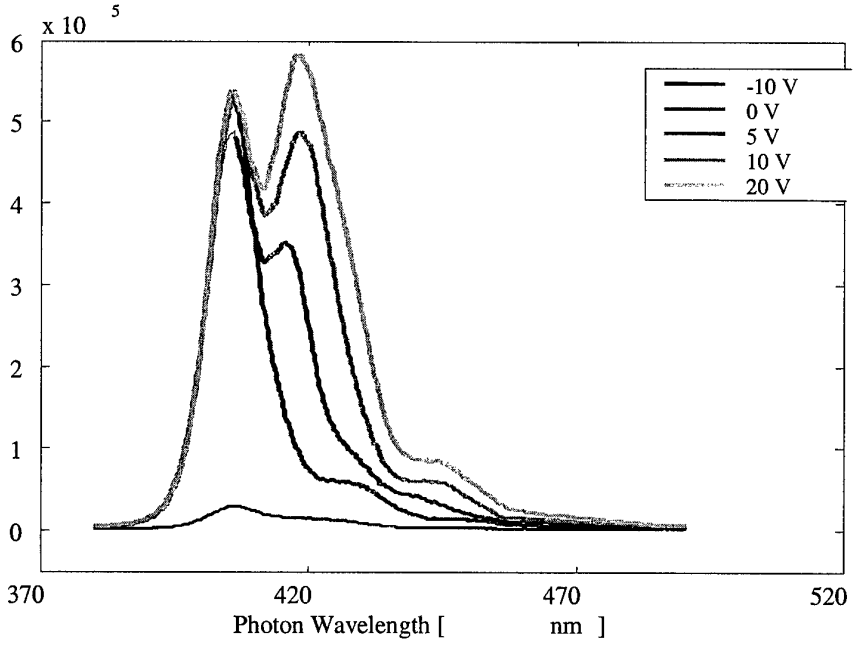


Fig 1 Time integrated PL spectra (0-20 ns) with different bias voltage.

The photoluminescence (PL) spectrum demonstrates several peaks at low temperature. The PL is dominated by the rather narrow near-bandgap emission at 3.07 eV with a linewidth of 40 meV.
This emission has a typical PL decay time about few ns at 2 K within the PL contour. However, we have observed an additional well-resolved line with the lower peak energy. Its position depends strongly on excitation conditions and is about 3.00 meV under a cw excitation with the laser beam power of 50 mW. The PL decay time for this second emission is longer than for the 3.07 eV line at least by one order of magnitude. To explain the origin of these two strong lines we suggested a model in which at least two nonequivalent quantum wells could be realized due to a potential gradient across the layers [1]. To verify this model we have applied an external electrical field to vary the internal potential across the heterostructure. Spectral positions, relative PL intensities as well as the PL transients and decay times have been measured as a function of electrical field and temperature for the different PL peaks. The PL data are comparable with electroluminescence spectra from the same diode. Our experimental data set, we believe, are helpful in understanding of the recombination mechanism in the InGaN/GaN MQW structures.

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Towards quantum structures in SiC

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The use of the quantum confinement effect to tailor the electronic, optical, and electrical properties is accompanied by an enormous progress in the field of semiconductor physics and devices. The fabrication of low-dimensional structures with electron confinement in one, two, or three dimensions is based on heterostructures of two different semiconductors. The different energetical positions of their conduction (valence) bands give rise to an energy barrier for the electrons (holes). Prototypical structures are semiconductor superlattices and quantum dot arrays.

From the point of view of quantum-confined structures, SiC is an extremely promising material. More than 200 polytypes with different stacking of the atomic Si-C bilayers in [0001] direction exist. The fundamental energy gap varies by about 1 eV between the cubic zinc-blende (3C) polytype and hexagonal (nH) polytypes with a number of n Si-C bilayers in a unit cell. Consequently, the growth of heteropolytypic structures makes it possible to build devices from heterostructures consisting of one specific semiconducting material but occurring in different crystal structures [1,2]. Indeed, there is a remarkable progress in the growth of heterpolytypic structures using solid-source molecular beam epitaxy (MBE) [3]. Another class of quantum structures are Si and also Ge dots. Embedding the group-IV dots in a wide-band-gap semiconductor, as hexagonal SiC, electroinjection of electron-hole pairs should be possible. Very recently the self-organized growth of Si and Ge dot arrays on a SiC surface has been demonstrated [4,5].

In this talk ideas, realizations, and properties of quantum structures based on SiC will be discussed. Two prototypical systems are studied. First, the attention is focussed onto SiC heterostructures. The MBE growth of the cubic polytype occurs preferentially under more Si-rich conditions, i.e. at lower temperatures (e.g. T = 1550 K). The hexagonal polytypes, however, were grown under less Si-rich conditions corresponding to slightly higher temperatures (e.g. 1600 K). As an example, a resulting 4H/3C/4H double heteropolytypic structure is presented in Fig. 1.



Fig. 1: TEM micrograph of a 4H /3C/4H-SiC(0001) double-heteropolytypic structure [3].

Meanwhile, the growth of multiple heterostructures consisting of some dozens of 4H-SiC barriers and of 3C-SiC wells was performed by solid-source MBE on 3° off-axis 4H substrates. The photoluminescence spectra measured for these multiple heterocrystalline structures show signals below the band gap of the 3C polytype, hence, indicating the type-II character of the heterostructure. A corresponding band structure calculated for a 3C/4H-SiC superlattice is presented in Fig. 2. The pronounced subband structure below the conduction

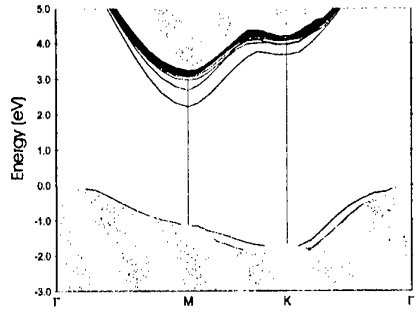


Fig. 2 Band structure of a $(3C)_3(4H)_{15}$-SiC(0001) superlattice. The shaded regions indicate the projected bulk band structure of 4H-SiC. Quasiparticle effects are taken into account.

band minimum of 4H-SiC indicates deep quantum wells for the electrons in the 3C regions. The band structure is still indirect in k-space parallel to the interfaces, so that the observed luminescence lines may be a consequence of the break of the k-selection rule by phonons and imperfections of the grown structure. An extremely large built-in electric field in the 3C layers allows a tunneling of the hole wave functions into the 3C regions resulting in a spatial overlap with the electron functions and, hence, optical transitions within the 3C regions.

Second, other interesting quantum structures are Si or Ge nanocrystallites embedded in SiC that can be fabricated by MBE or ion inplantation with subsequent annealing. From a theoretical point of view we suggest the preparation in particular of Ge dots in hexagonal SiC. Calculations [6] have shown that, even for Ge nanocrystallites with a diameter of about 2 nm, there are optical transitions at the absorption edge which possess oscillator strength comparable with those of III-V compounds. This tendency can be also seen from the absorption spectrum of Ge dots embedded in 3C-SiC in Fig. 3. A low-energy peak occurs which shows a redshift and an increasing strength with rising dot size. Whereas the k-selection rule is broken in the Ge case, the indirect character of Si occurs already for not too

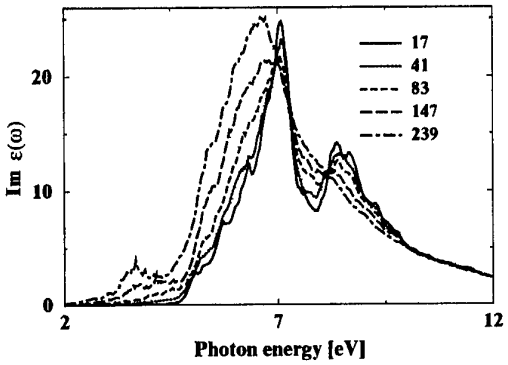


Fig. 3 Imaginary part of the dielectric function of Ge dots with varying number of atoms embedded in 3C-SiC. Results are obtained using a 512-atom supercell.

large nanocrystallites. The hexagonal SiC polytypes should be used as matrix material. Only in this case a type-I heterostructure situation with a localization of electrons and holes in the Ge nanocrystallites is predicted.

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Lateral enlargement of silicon carbide crystals

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Large seeds with low defect density are important for bulk growth of silicon carbide (SiC). At present, several kinds of crystallographic imperfections exist in SiC crystals. Many of these defects are inherited from the seed crystal. Micropipes and threading dislocations are defects that are continued from the seed crystal into the growing bulk crystal. These defects are normally observed when the growth proceeds in the c-axis direction, <0001>.

In this work crystals have been grown laterally along the a-axis direction in a modified sublimation growth system. The idea was to have a small crystal with few defects and enlarge the crystal in the a-axis direction without increasing the number of micropipes and other threading defects. The system was optimized for lateral growth concerning susceptor, pressure and temperature gradient. Simulation of the susceptor design was made to optimize the conditions for lateral growth. The growth mechanism for the lateral growth is different compared with that along the <0001> direction. No screw dislocations are formed in this case. The growth of the crystal proceeds in a hexagonal habit independent of the shape of the seed crystal depending on different growth velocity in different directions.

On-axis 6H-SiC Lely and 4H-SiC modified-Lely crystals with 8° off-cut were used as seed crystals. Due to a remaining small vertical temperature gradient in the center of the susceptor, growth also occured on top of the seed crystal at the center of the seed. The ratio between c-axis growth (normal) and a-axis growth (lateral) was around 1/20 in the center. Depending on the type of seed, the polytype of the grown material can be different in different growth direction (c- and a-direction). The lateral enlargement reached 6 mm, which is limited by the susceptor design. Growth temperature varied between 2320 and 2420 depending on seed crystal and the growth rate between 1.2-4.0 mm/hour. The polytype of the laterally grown 4H-material is stable in a certain temperature range according to PL measurements. The grown crystals have been studied concerning morphology and crystalline structure. The grown crystals have been investigated by high-resolution X-ray diffraction and synchrotron topography. The results show that this growth technique makes it possible to make enlargements of crystals without increasing the number of micropipes. The mechanism of the lateral growth will be discussed.

Figure 1 shows a demonstration of a laterally grown part of a crystal and the overgrowth of the crystal. Region *A* is the laterally grown part of the crystal, *B* is the overgrowth of the laterally grown part of the crystal. Particles on the surface interrupting the step-flow growth are marked with arrows. Figure 2 shows a section transmission topograph of the laterally grown part of the crystal and the interface with the seed crystal. The bands with different contrast seen in the topograph are due to strain probably caused by bending of the crystal. No micropipes are seen in the topograph.

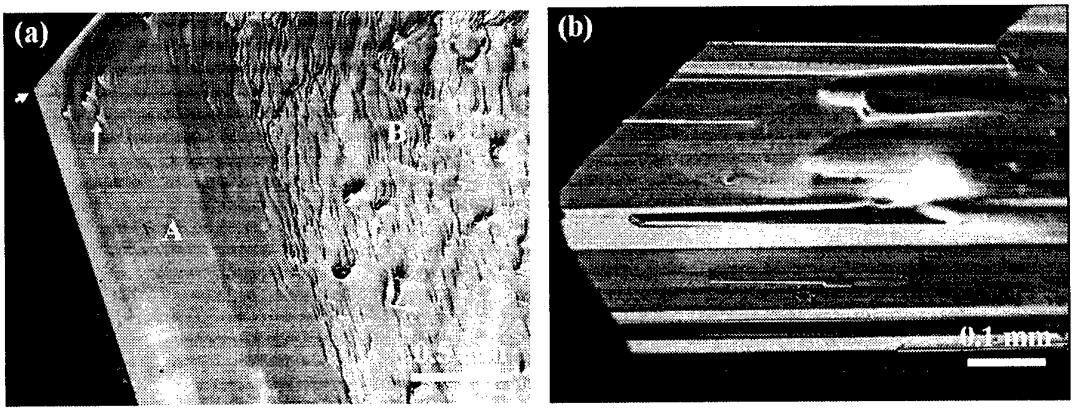


Fig. 1 (a) Region *A* shows the laterally grown part of the crystal, *B* shows the overgrowth of the laterally grown part of the crystal. Particles on the surface interrupting the step-flow growth are marked with arrows; (b) image taken at edge of laterally grown part (indicated by arrow in figure a).

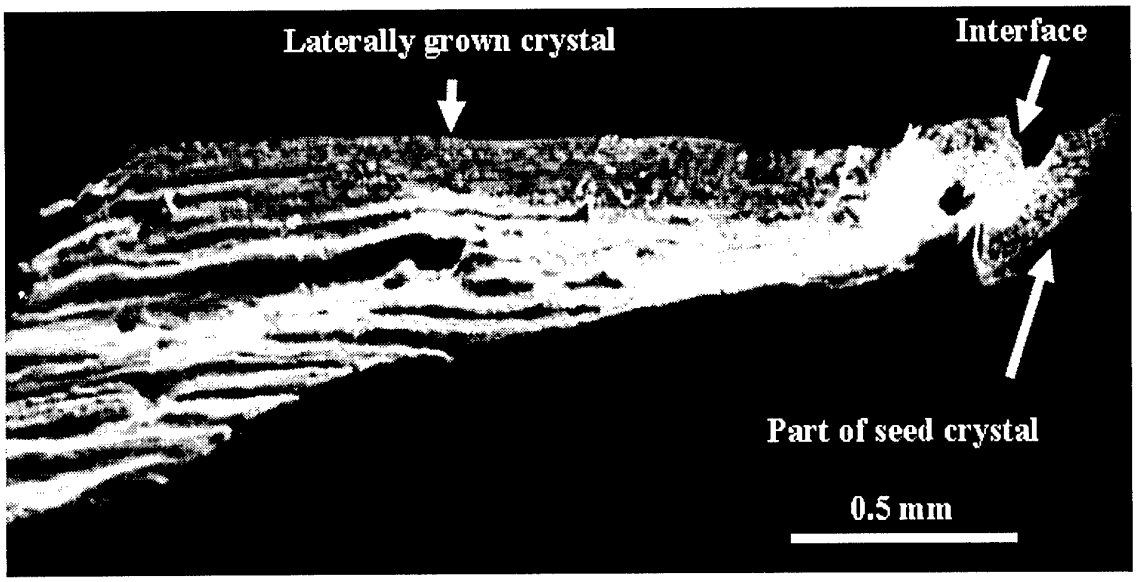


Fig. 2 Section transmission topograph of the laterally grown part and the interface with the seed crystal. The bands with different contrast seen in the topograph are due to strain probably caused by bending of the crystal. No micropipes are seen in the topograph.

"Insitu synthesis" of source material from elemental Si and C during SiC PVT growth process and characterization using digital x-ray imaging

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Today, SiC single crystals for commercial applications are grown by the physical vapor transport (PVT) method using SiC powder as source material, the latter being synthesized prior the real growth process during an extra technological step. In order to save one process step we have investigated the possibility to combine both, the SiC powder synthesis from elemental Si and C and the SiC crystal growth process into one technological step. First of all we had to prevent the SiC seed from raising SiC powder grains due to highly exothermal reactions during SiC synthesis from elemental Si and C (midrange temperatures, i.e. 1450°C). Secondly we had to guarantee comparable SiC crystal growth conditions (elevated temperatures, i.e. 2200°C) as in the original two step counterpart, i.e. adjust the same SiC powder grain size, etc.. In order to address these questions we used a recently developed digital x-ray imaging technique [1,2] which allowed an online visualization of the ongoing processes and an identification of problems at the time when they occur.

The insitu synthesis of the SiC source material was carried out at the same temperature (i.e. 1600°C) and for the same holding time as in the conventional two step PVT process. It turned out to be mandatory to prevent the SiC seed from the exothermal synthesis process. For this purpose

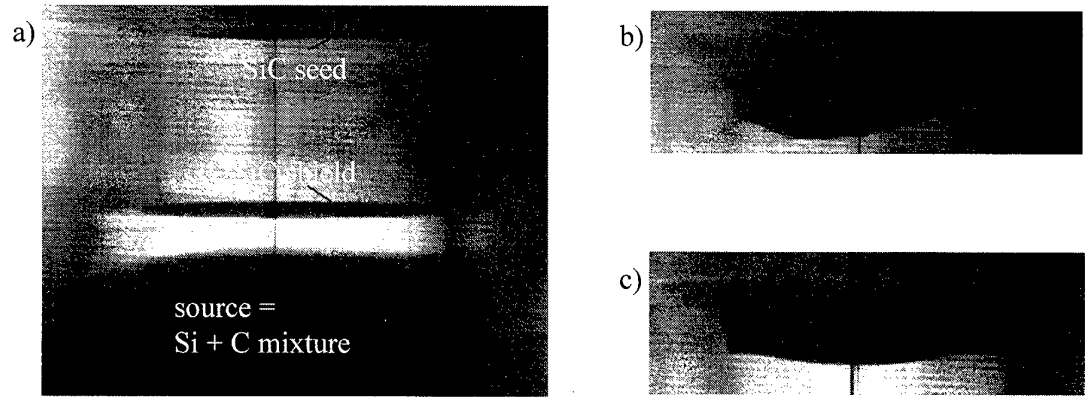


Figure 1. X-ray image of PVT crucible interior showing (a) the SiC seed, source material (mixture of high purity Si and C, and SiC shield between source and seed prior the growth process, (b) crystal growth interface with a broken SiC wafer shield after insitu Si + C synthesis process and (c) crystal growth interface using a modified, stable shield.

a SiC wafer was mounted as shield between the Si+C mixture (=source material) and the SiC seed (see Fig. 1a). Using this minor modification to the conventional growth procedure, 6H SiC single crystals with 40mm in diameter were grown. The strength of the underlying synthesis driving force became evident when the SiC shield broke one time at the Si+C synthesis temperature. In this case a rather inhomogeneous SiC sublimation occurred resulting in a highly non-uniform crystal shape (Fig. 1b). However, after modifying the shield in Fig 1a, homogeneous growth conditions were achieved leading to an uniform and flat growth interface (Fig. 1c) and low overall defect density comparable to the conventional SiC growth process (micropipe density $<200cm^{-2}$, high polytype stability, etc.).

The analysis of the x-ray images showed that the growth rate in the initial time (first 5h...10h of 72h) was smaller than in comparison to the convention PVT process with SiC powder as source material. It turned out that the smooth surface of the SiC shield limited the initial SiC sublimation. In the case of SiC powder, a large effective surface leads to a higher sublimation rate. After about 5h...10h both sources (SiC powder and Si+C mixture) developed a needle like surface morphology which serves as an optimized sublimation interface. The latter was supported by the SiC PVT growth experiment in which only a part of the SiC source surface was shielded by a smooth SiC wafer (Fig. 1b). In this case the crystal growth interface showed the above described non-uniformity, i.e. lower growth rate in the case of a smooth surface. Once a needle like structure was formed, typical (conventional) growth rates of about 250µm/h were reached.

We will demonstrate the successful application of the insitu synthesis of the SiC source material prior the real crystal growth process. We will discuss the arising problems and solutions like the application of a SiC wafer shield by showing several x-ray images which were taken online during different growth runs. Finally we will address fundamental aspects of the sublimation kinetics arising from the analysis of our experimental x-ray imaging data.

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Full Si wafer conversion into bulk 3C-SiC

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If obtained in a sufficiently good crystalline quality, cubic silicon carbide (3C-SiC) would be the most attractive SiC polytype. It exhibits superior electronic properties with respect to 4H-SiC and could be used as substrate for $Ga_{1-x}Al_xN$ growth. This would be true in the nitride cubic or hexagonal phases depending only on the [001] or [111] orientation of the cubic substrate. Half of the production of hexagonal SiC is used as substrates for nitride optoelectronics, and this application is far less demanding for residual doping than electronic devices. As a consequence, producing large area 3C-SiC substrates appears of very much interest.

3C-SiC is usually grown by CVD on Si wafers [1]. It can be obtained at much lower temperature than hexagonal SiC (and in much larger substrate dimensions). However crystal quality is poor, due to the large mismatch of lattice parameters and thermal expansion coefficients between Si and SiC. The effect is even worse in the <111> direction which corresponds to a more compact stacking.

To overpass this problem, we investigated the effect of completely converting a Si wafer into bulk SiC. The principle of the transformation is the following one [2]. A first SiC layer is grown by CVD on top of a Si wafer. Then the layer is put downwards to serve at the same time as a substrate and a crucible. After heating over the melting point of Si some propane is introduced and, provided a convenient temperature gradient exists, all Si converts into SiC by LPE (Liquid Phase Epitaxy) on the CVD SiC seed. No Si remains in contact with SiC and the overall stress is expected to release. All layers obtained is this way were light yellow and transparent, with thickness of 40 to 100 μm.

In Fig.1, we show the results of a cross sectional TEM investigation. The dark part is the CVD layer. This indicates a large dislocation density. Obviously, in the LPE region, the dislocation density reduces. In Fig.2, a plan view TEM shows no dislocation in the LPE layer which means that the dislocation density is of the order of (or lower than) 10^6 cm^{-2}. This is 2 to 3 orders of magnitude below the standard CVD part. The same figure shows that the density of stacking faults remains high (in the range of $5x10^8$ cm^{-2}, which is not different from the CVD layers). This means that the stacking faults are very difficult to control in 3C SiC while the density of dislocations can be lowered thanks to the combined effects of LPE, lack of external stress and increased thickness.



Fig.1: TEM micrograph of the cross section of LPE SiC/CVD SiC

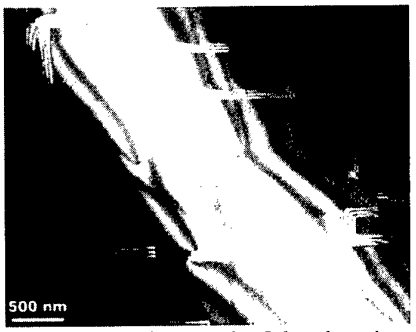
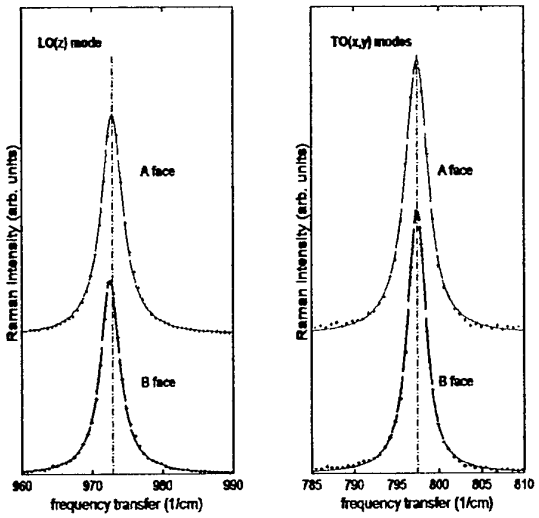


Fig.2: TEM micrograph of the plan view of LPE SiC/CVD SiC

A comparison of Raman spectra collected on the two different faces is shown in Fig.3 for the longitudinal and transversal modes, respectively. Concerning the longitudinal (Z-like) modes, the position on the B face is 972.6 cm^{-1} slightly shifted with respect to the A face. Notice that both lines remain symmetric. When fitted with simple Lorentzian forms (solid lines) they give a width (FWHM) of 3.7 and 3.3 cm^{-1} for the A and B faces, respectively.
The line shapes of the TO mode are more asymmetric and could not be fitted using a simple Lorentzian shape. To explain this asymmetry, we have to address the phonon-disorder interaction [3]. Because it results in a slower drop of the low-frequency wing in comparison with the high-frequency wing of the line, the line shape depends on the geometry of the defects.
The defects can have a point-like form, a line form (like dislocations, for instance) or a plane form (stacking faults, micro-crystal boundaries, etc...). In our case the best fit was achieved using a theory which includes the phonon interaction with plane defects. The position and width (797.5 and 3.16 cm^{-1} for the A face and 797.4 and 2.51 cm^{-1}.for the B face, respectively) are intermediate between the two extreme values obtained in a previous study of strain and strain-relaxation at the SiC/Si interface [3] and we conclude to that the strain relaxation is still not complete.

Fig. 3: Raman spectra collected on both sides of a LPE 3C-SiC layer obtained as described in the text.



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The Effect of Nitrogen on Crystal Growth of SiC on {11$\bar{2}$0} Substrate

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1. Introduction

High quality crystals have been grown by Chemical Vapor Deposition (CVD) on vicinal (0001) Si-plane, however, channel mobility of MOSFET on this plane has been miserably low. Recently, high channel mobility on {11$\bar{2}$0} was reported [1], so crystal growth on {11$\bar{2}$0} substrate is strongly focused. Nevertheless, SiC boules have been conventionally grown on {0001}, and growth mechanism on {11$\bar{2}$0} have not known well. Nitrogen doped "buffer layer" is introduced into the interface between substrate and epilayer to grow high quality epilayer on {11$\bar{2}$0} substrates in case of CVD [2]. However, the effect of nitrogen on crystal growth have not discussed well. Crystal growth on {11$\bar{2}$0} substrates were conducted and the effect of nitrogen was discussed.

2. Experiment

Sublimation growth was achieved using a quartz tube reactor with a water-cooled jacket. {11$\bar{2}$0} substrates were cut from the boule previously grown on {0001}, and they were put on the lid of graphite crucible. Abrasive SiC powder was charged into the crucible as a source material. The temperatures at the top and the bottom of the crucible were monitored by optical pyrometers, and they were kept at approximately 2200°C and 2500°C, respectively. Several crystals were grown under argon atmosphere and the others were grown under nitrogen atmosphere. The growth pressure was approximately 30 Torr. Surface morphology of grown crystals were observed by optical microscope, scanning electron microscope (SEM) and atomic force microscope (AFM).

3. Results and Discussion

3.1 Crystal Growth of 6H-SiC on {11$\bar{2}$0} Substrate

Surface morphology of the crystal grown by sublimation method on {11$\bar{2}$0} substrates have known as smooth [3], and reports concerning about the defects on {11$\bar{2}$0} is few. However, crystal grown on {11$\bar{2}$0} substrates contained hollow core defects if growth conditions were not optimized. Hollow core defects penetrated to the {11$\bar{2}$0} surface and pits were observed on the surface as shown in Figure 1. The pits observed here were also seen on the sidewall of grown crystal on {1$\bar{1}$00} substrates, namely {11$\bar{2}$0}. So, these pits could be thought as intrinsic defects on {11$\bar{2}$0} in the crystal growth of SiC.

From observing the pits on {11$\bar{2}$0}, we suggest a growth model of SiC on {11$\bar{2}$0} substrate. On flat {11$\bar{2}$0}, two-dimensional growth would proceed at optimum growth conditions. However, if substrate surface was not atomically flat or growth conditions were not optimized, surface diffusion length would become shorter and growth mode would change from two-dimensional growth to three-dimensional growth. As three-dimensional islands grow at all over the surface, they would coalesce each other. Hollow core defects would be created at the boundary of coalesced islands, if there was a misalignment between each island. Stacking faults might affect to this misalignment of islands. Though several mechanisms have been reported [3], generation mechanism of stacking faults on {11$\bar{2}$0} has not been cleared well. We contributed the stacking

fault generation on $\{11\bar{2}0\}$ to three-dimensional growth. Stacking fault density should be low on $\{11\bar{2}0\}$ as long as crystal grows two-dimensionally, because bonding configuration is always uniquely determined on $\{11\bar{2}0\}$. In case of three-dimensional growth, $\{1\bar{1}00\}$ facets would appear on the shoulder of islands because of growth rate anisotropy between $<1\bar{1}00>$ and $<11\bar{2}0>$. Stacking faults would be created easier on $\{1\bar{1}00\}$ by kinetically-induced misarrangement of surface adatoms [3]. Stacking faults could have harmful effect on coalescence of islands. Therefore, crystal growth on $\{11\bar{2}0\}$ substrate should be proceeded two-dimensionally so as not to increase the incorrect coalescence of islands. Atomically flat surface is thought to be significantly important to keep two-dimensional growth on $\{11\bar{2}0\}$.

3.2 Crystal Growth on $\{11\bar{2}0\}$ Substrate under Nitrogen Atmosphere

Similar treatment as CVD, that is introducing the nitrogen doped buffer layer into the interface between substrate and grown crystal, might be also useful for sublimation growth to grow high quality crystals on $\{11\bar{2}0\}$ substrate. To investigate the effect of nitrogen, sublimation growth on $\{11\bar{2}0\}$ substrates were carried out under nitrogen atmosphere for total growth duration. Another growth conditions were same as the growth under argon atmosphere. Significant improvement of surface morphology was achieved as shown in Figure 2. Pits were not observed on the surface.

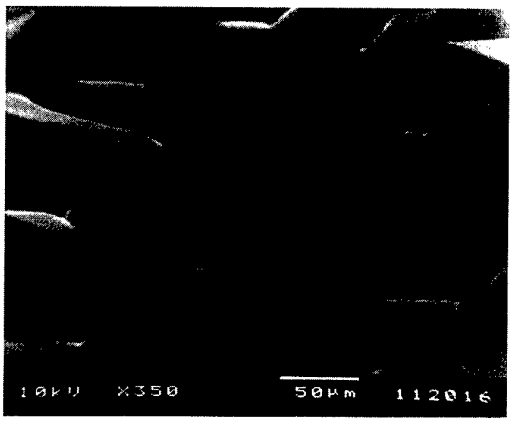


Figure 1.
SEM image of the pits observed on $\{11\bar{2}0\}$.

The effect of nitrogen in CVD growth has been considered as the reduction of lattice mismatch caused by doping difference between substrate and epitaxial layer [2]. In spite of small doping difference between substrate and grown crystal, nitrogen effected a lot to improve the crystal quality even in sublimation growth. Growth mode seemed to be changed from three-dimensional growth to two-dimensional growth by growing the crystal under nitrogen atmosphere. So, besides reducing the lattice mismatch, the role of nitrogen seemed to be flattening the surface and inactivating defects on the surface. Silicon nitride might be created from place to place on $\{11\bar{2}0\}$ surface. Selective growth using self-constructed silicon nitride mask might affect as slowing down the growth toward $<11\bar{2}0>$ and flattening the surface.

In addition, lowered C/Si ratio by using tantalum improved the surface morphology in the growth under both argon and nitrogen atmosphere. Lowered C/Si ratio might be contributed to increase the effective adsorption of nitrogen on $\{11\bar{2}0\}$.



Figure 2.
SEM image of flat surface grown on $\{11\bar{2}0\}$ substrate under nitrogen atmosphere.

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QuaSiC Smart-Cut® substrates for SiC high power devices

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Keywords : 4H SiC, polycrystalline SiC, tungsten silicide, wafer bonding, Smart-Cut®, epitaxy,

The development of SiC based electronic power devices, such as Schottky diodes, is today limited by both the availability and price of high quality low resistivity 4H SiC wafers.
One way to overcome cost and availability limitations is to propose an alternative material source suited to power electronic devices. The generic nature of the Smart-Cut® process, based on proton implantation and wafer bonding, is now recognized through successful demonstrations of Si [1], SiC [2], InP [3] and GaAs [4] thin film transfers. In the particular case of SiC, previous works have been first focused on the multiple transfer of high quality SiC thin layers onto dissimilar substrates, mainly such as silicon and polycrystalline SiC wafers, via oxide layers, for the fabrication and characterization of SiCOI substrates (SiC On Insulator) [5]. In these studies main results have concerned the control of the electrical properties of the transferred thin film.
One possible material solution for the SiC technology for power electronics is to transfer several times thin layers cut from a very high quality SiC substrate (low micropipe and dislocation densities) onto a lower cost substrate such as polycrystalline SiC or a lower crystal quality SiC substrate. This technology, as demonstrated for SOI wafers (Silicon On Insulator), is scalable to larger substrate diameters. This is particularly interesting as SiC wafers are shifting towards 4 inch diameter.
In this work, we present the last developments of this technology for the demonstration of vertical truly conducting SiC based substrates. We have particularly studied the development of structures such as monocrystalline 4H SiC thin film onto CVD polycrystalline SiC substrates. Wafer bonding between mono and polycrystalline SiC wafers with refractory and conductive tungsten silicide based bonding layers has been developed. This bonding layer has been chosen regarding physical considerations such as thermodynamical equilibrium with SiC, refractory behavior and ability to form ohmic contacts with SiC. This has led to the demonstration of SiC thin film transfer onto poly and mono SiC substrates using the Smart-Cut® .technology (QuaSiC substrates) (Figure 1). Successful CVD epitaxial regrowth using standard bulk conditions have also been demonstrated onto QuaSiC substrates.

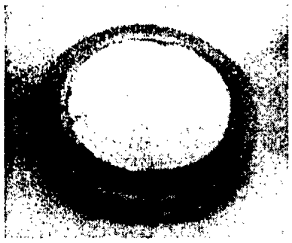


Figure 1 : 50.8 mm QuaSiC substrate obtained with the Smart-Cut® technology

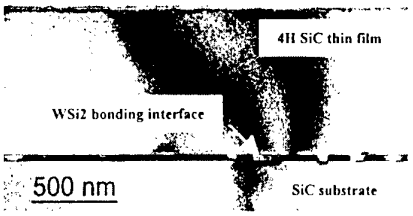


Figure 2 : TEM cross section of a QuaSiC substrate without epi regrowth

Both QuaSiC substrates with or without epitaxial regrowth have been physically and electrically characterized. TEM cross sections (Figure 2) have been performed for the investigation of the quality of the bonding layer as well as the crystalline transferred SiC thin film. TEM cross sections of QuaSiC substrates with epitaxial regrowth will be also presented and analysed regarding the quality of the different layers and interfaces.
Low temperature photoluminescence spectra show that the quality of the SiC epitaxial layer grown onto QuaSiC substrates is similar to epilayers grown on SiC bulk substrates (Figure 3).

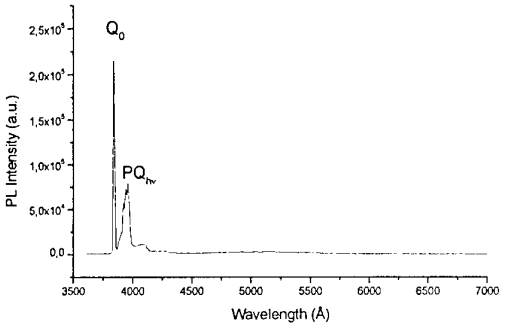


Figure 3 : LTPL of an epitaxial regrowth on QuaSic substrate.

Indeed, the photoluminescence is dominated by near band edge (NBE) emission with no evidence of deeper energy band associated with impurities or defects. This well known NBE emission for n-type 4H SiC is associated with nitrogen bound exciton luminescence (Q_0) and corresponding phonon replicas (PQ_{hv}). Finally, the capability of the interface bonding layer to conduct high current flow has been checked using I(V) measurements on specific patterns. The comparison of electrical characteristics between transferred and non transferred structures has been carried out. Encouraging results have been obtained and will be detailed in this paper.

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The development of 4H-SiC {03-38} wafers

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1. Introduction

Silicon carbide, which are known as the wide-gap-semiconductor, is expected for applications of the power devices such as the diodes or the power MOS FETs. However, in the crystal growth of SiC, the defects, such as the micropipe and the stacking fault, propagate along the growth direction and appear on the surface of ingots. Therefore, the development of high-quality wafer was very difficult.

We developed the crystal grown along <03-38> direction which inclines at c axis by 54.7° as shown Fig.1, to make the defects propagated diagonally, and so as not to allow the defects to reach the front surface of the ingots (Fig.2). We report the result of the crystal growth and the characteristics of the crystals.

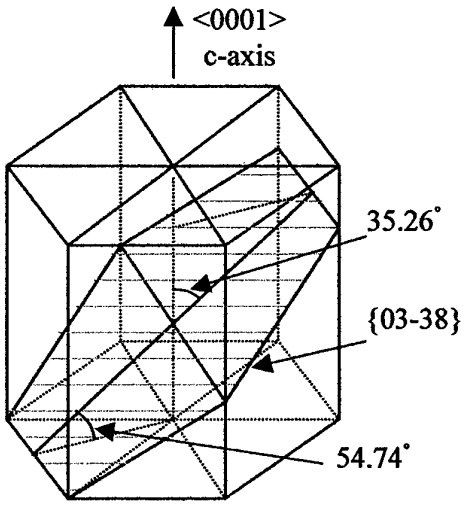


Fig.1 Lattice stracture of 4H-SiC

2. Experiment

Bulk single crystals were grown by the sublimation method. The crucible assembly consisted of the graphite support to which the seed crystal was attached and the graphite crucible containing the source powder. We used the seed 4H-SiC{ 03-38} crystal which was prepared by slicing diagonally the 4H-SiC{0001}

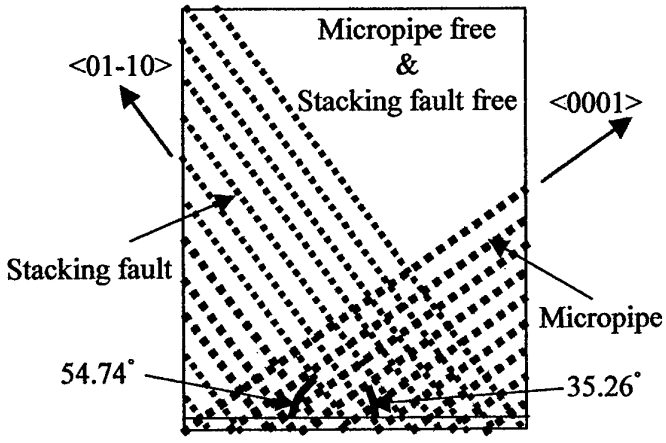
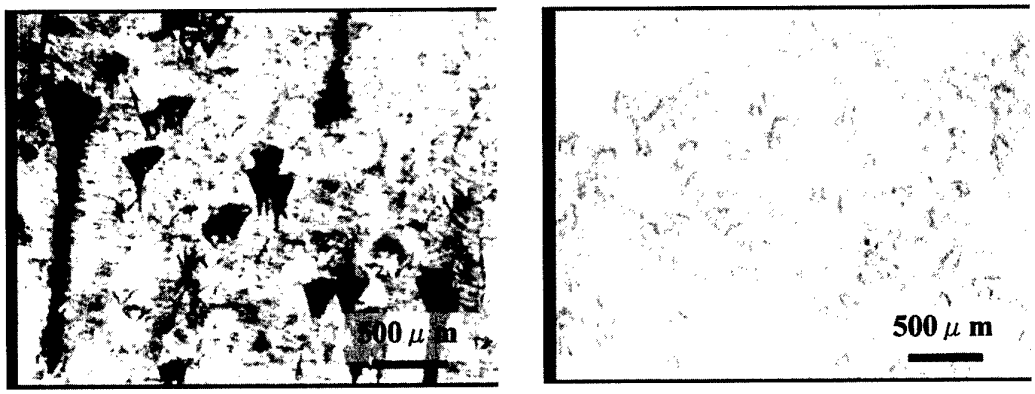


Fig.2 Schematic of defect propagation on crystal growth

ingot. The seed crystal and the source powder in the crucible were heated more than 2000 ℃. During the crystal growth, the growth pressure was less than 10kPa. N-doped crystals were prepared by adding controlled amounts of high-purity nitrogen to the inert ambient.

3. Result and Discussion

We obtained 4H-SiC{03-38} wafer by slicing the ingots grown along the <03-38> direction. We cut the ingots into the 4H-SiC{03-38} wafers. The micropipe densities of the seed crystal and the grown crystal (wafer) were determined by the optical microscopy with Nomarski interference contrast after etching wafers in the molten KOH. The micropipe was not observed on the surface of the grown crystal though there were some micropipes on the surface of the seed crystal (Fig.3). Moreover, when we observed the vertical section of the 4H-SiC{03-38} ingot, the stacking faults propagated diagonally and reached the side of the ingot.



(a) (b)

Fig.3 Micrographs of KOH-etched (a)seed (b)wafer

3. Summary

When the crystal was grown along the <03-38> direction, we confirmed the area of no micropipe and the diagonal propagation of the stacking fault.

WeB2 Electrical Properties 1

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Study of SiC PiN Diodes Subjected to High Current Density Pulses

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In this work, *SiC* PiN power diodes subjected to single high density forward current pulses have been studied both experimentally and by means of computer simulations. Two sets of diodes were studied. One set of diodes was manufactured by ion-implanting the p^+-emitter into an epitaxially grown n-base. The other set of diodes was manufactured by epitaxial growth of the p^+-emitter on an epitaxially grown n-base. Both sets of diodes have a similar set of design parameters. The epitaxial diodes show superior high forward current density properties (i.e. lower power losses and larger SOA).

In the experimental studies the dynamic IV characteristics and the surface temperature have been measured, while the diodes were being subjected to single 1 ms half-sine-wave current pulses having a density in the range 100 to 6200 Amps/cm^2. The recorded dynamic IV characteristics of both epitaxial and implanted diodes show as a main feature the presence of a single loop that steadily increases as the peak current density is augmented and the power losses become larger. This differs from previous investigations carried out on lifetime engineered 3.3 kV *Si* power diodes [1]. The dynamic IV curves seem to be dominated by the decreasing mobility as both the carriers' density and the device temperature increase.

The diode surface temperature has been measured using an IR microscope designed and built in our lab [2]. In spite of the high thermal conductivity of *SiC*, it has been observed that, for current pulses 1 ms long, the heating of the device occurs under almost adiabatic condition, i.e. almost no heat is lost during the time that the current pulse is applied. This has also been observed for *Si* diodes [2], and it is a consequence of the high thermal impedance between the diode and the metal electrodes [2].

After repeated exposure to high-density current pulses, both epitaxial and implanted diodes showed signs of degradation resulting in the deterioration of the dynamic IV characteristics. Degradation is manifested as an increase in the peak voltage drop and also as a change in the shape of the voltage-drop-as-a-function-of-time curve that results in an ever increasing area of the loop displayed by the dynamic IV characteristics.

Diode degradation has been quantitatively studied by subjecting the diodes to single 1 ms long 3000 Amps/cm^2 half-sine-wave current pulses, and recording the current and the voltage signals as a function of time. These signals have in turn been related to the accumulated supplied energy. In this way the extent of the generated damage has been quantitatively correlated to the total supplied energy.

The experimental data obtained (i.e. dynamic IV characteristics and surface temperature) have been compared to the results from computer simulations performed using the two-dimensional device simulation package *AVANT!* MEDICI.

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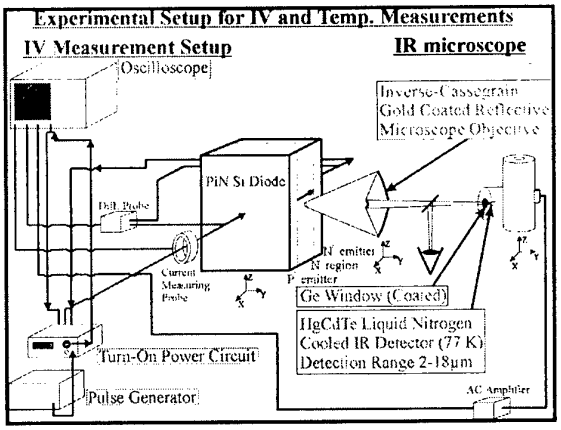


Fig. 1 Experimental set-up used to measure the diode's dynamic IV characteristics and the surface temperature as a function of position, time and current density.

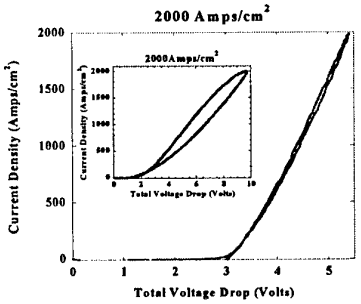


Fig. 2 Measured dynamic IV characteristics for a peak current density of 2000 Amps/cm^2 on an epitaxial diode. The size of the IV loop is negligible, indicating that the mobility is only slightly affected by the increase in carriers' concentration and temperature during the complete duration of the current pulse. As a comparison, the dynamic IV characteristics of a fast recovery 3.3 kV *Si* power diode [1] are shown in the inset.

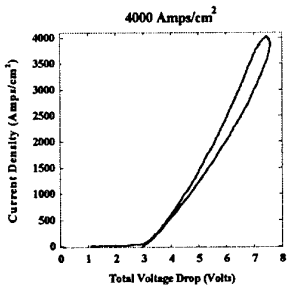


Fig. 3 Measured dynamic IV characteristics for a peak current density of 4000 Amps/cm^2 on an epitaxial diode. The hysteresis in the IV curve caused by the decrease in carriers' mobility due to device self-heating can be clearly seen.

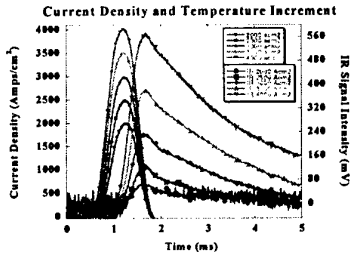


Fig. 4 Measured surface temperature as a function of current density and time on non-degraded diode. The peak temperatures are 101, 131, 166, 210 and 259 °C approximately.

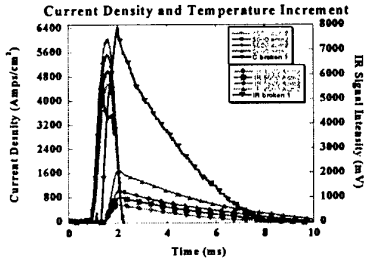


Fig. 5 Measured surface temperature as a function of current density and time on non-degraded diode. Observe the extremely large amplitude of the IR signal during the diode destruction pulse. This is an indication of large localized heating. The peak temperatures under normal operation are 302, 372, 454 and 570 °C approximately.

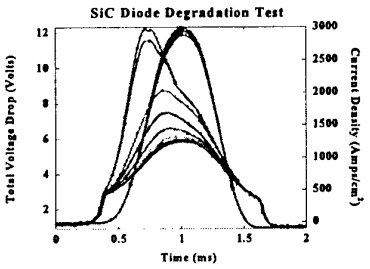


Fig. 6 Measured total voltage drop and current density as a function of time (degradation test). The total voltage drop increases as more energy is supplied to the diode. The curves have been recorded after 65.6 (700 pulses), 132.6 (1400 pulses), 201.9 (2100 pulses), 275.9 (2800 pulses), 358.2 (3500 pulses), 451.8 (4200 pulses) and 461.8 (4270 pulses) Joules have been dissipated by the diode.

The effect of hydrogen diffusion in p- and n-type SiC Schottky diodes at high temperatures

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Chemical gas sensors based on catalytic metal insulator silicon carbide, MISiC devices, have been operated at 600°C for extended periods and shortly up to 1000°C. The speed of response, when changing between an oxidising and reducing ambient at temperatures ≥600°C is a few milliseconds. Applications like cylinder specific monitoring in exhaust gases of a car engine, synthetic exhaust diagnosis, and flue gas monitoring have been demonstrated [1]. Devices based on Schottky diodes as well as FET transistor devices have been used for the applications [1-3]. Here we present the effect of a hydrogen anneal at 600°C for Schottky sensor devices based on n- and p-type 4H SiC.

We have investigated MISiC Schottky devices with epilayers grown by hot wall CVD epitaxy (N_d =6x10^{14}cm^{-3}) [4], sublimation epitaxy (N_d =2.5 10^{16}) [5] and devices processed on p- (N_a = 6×10^{15}) and n- type (N_d = 4,5×10^{15}) wafers purchased from Cree [6]. The devices have gate contacts of porous Pt, Ta + Pt, or $TaSi_x$ + Pt and ohmic back contacts of $TaSi_x$ + Pt. A thin oxide, 1 nm, is grown on the SiC surface by ozone exposure before the gate metal deposition [1].

It has been shown by SIMS spectroscopy that Pt facilitate deuterium incorporation in p-type SiC at 600-800°C [7]. This is due to the fact that hydrogen or hydrocarbons dissociate on the catalytic metal surface of Pt and hydrogen atoms are formed, which diffuse through the metal and into the SiC in an oxygen deficient atmosphere at T ≥ 600°C. The hydrogen may trap at different impurities, such as compensational doping atoms, in the SiC lattice, which in turn will effect the net carrier concentration in a device. This will show up as a change of the IV characteristics of a Schottky diode. For the applications of the devices in, for example, measurements of the air to fuel ratio in exhaust gases the ambient changes within milliseconds between oxygen in excess and fuel in excess [1]. Here the hydrogen atoms are produced and consumed (hydrogen and oxygen forms water on the Pt surface) very fast and adsorbed atoms at the metal SiC interface give rise to a gas response rather than diffuse into the SiC. But it is anyhow of large importance to study the phenomenon of hydrogen diffusion in SiC.

A number of Schottky devices have been studied by recording the IV curves in an oxygen ambient at 400°C after annealing 4-15 hours in 2 % H_2 / N_2 or 2 % O_2 / N_2 atmosphere at 500 and 600°C. The temperature is lowered to 400°C in the annealing ambient. Figure 1 and 2 show the effect on the forward current of annealing at 600°C for an n-doped and p-doped sample, respectively. Hydrogen seems to reversibly increase the doping of the samples, which was valid for all measured samples at this temperature. Surprisingly enough the p-doped sample behaves similarly to the n-doped samples. The effects of the hydrogen anneal at 500°C is much smaller. Here the p-doped sample shows a deviating behavior, hydrogen in fact seem to slightly decrease the doping. Samples with epilayers processed by different growth methods showed some additional behavior, which will be further discussed. SIMS measurements will be performed on both p- and n-type samples, which have been exposed to deuterium, in order to try to understand the effect of hydrogen in the SiC lattice.

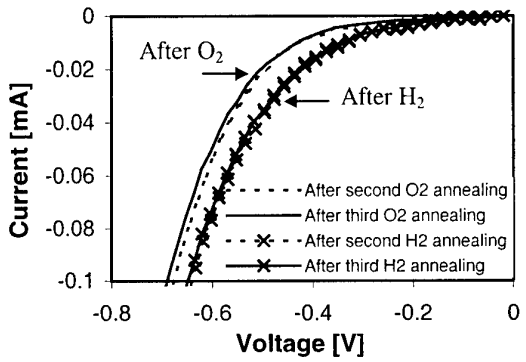


Figure 1. I-V characteristics at 400°C for a p-type Schottky diode after 4 h of annealing in hydrogen or oxygen ambient at 600°C.

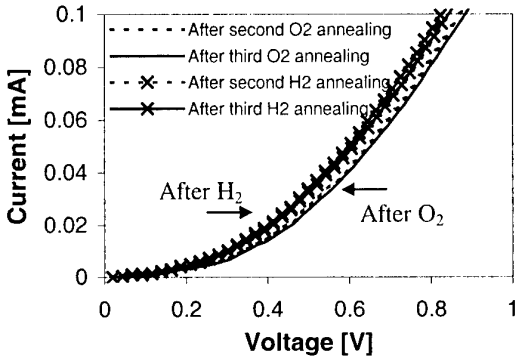


Figure 2. I-V characteristics at 400°C for an n-type Schottky diode after 4 h of annealing in hydrogen or oxygen ambient at 600°C.

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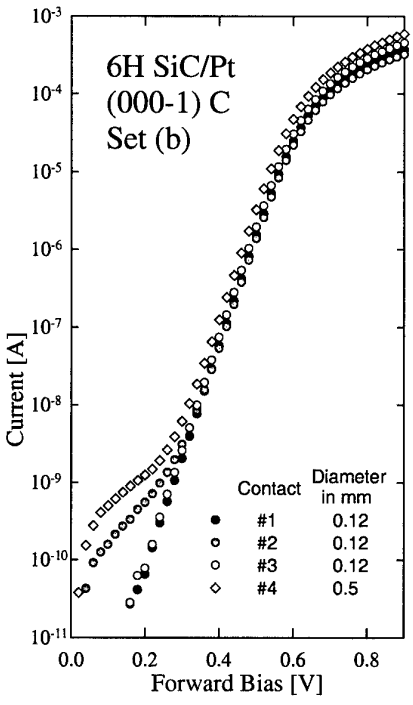
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Schottky Barriers for Pt on 6H and 4H SiC (0001), (000-1), (1-100) and (1-210) Surfaces Measured by I-V, C-V and Internal Photoemission

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Our measurements of the Schottky barrier heights (SBH) of 4H and 6H SiC/Pt contacts reveal a dependence on the crystallographic face of the SiC epilayer. The samples were prepared especially for this research. 6H and 4H SiC boule pieces were cut to make slices (thickness 0.5-1.0 mm) with the crystallographic faces (0001) (Si-face), (000-1) (C-face), (1-100) and (1-210). The Si- and C-face samples were cut 3.5° and 8° off ⟨0001⟩ towards ⟨1-210⟩ for 6H and 4H SiC, respectively, to optimize epitaxial growth. X-ray diffraction was used to accurately determine the orientations. The slices were mechanically polished down to 0.25 μm diamond and then chemical-mechanically polished at II-VI, Inc. The substrate doping concentration was $2\text{-}3\times10^{16}$ cm^{-3} for 6H SiC and 5×10^{17} cm^{-3} for 4H SiC.



N-type homo-epitaxial layers about 10 μm thick were grown by cold-wall CVD at 1520°C. The doping concentrations are of order 10^{18} cm^{-3} for 6H SiC and 10^{15} cm^{-3} for 4H SiC. The surface morphology for (1-100) face samples was not as good (scratches, hillocks) as for the other three faces.

Ni ohmic contacts were fabricated on the front sides of 6H SiC samples (due to the low doping concentration of the substrate) and on the back sides of 4H SiC samples by e-beam evaporation followed by annealing at 1000°C for ten minutes. Pt Schottky contacts were fabricated by sputtering with Ar ($0.9\text{-}2.0\times10^{-8}$ torr base pressure, Pt 99.99% pure). Before deposition the samples were RCA cleaned, etched in HF for five minutes and rinsed in deionized water. The circular contacts are 0.12 mm and 0.5 mm diameter and 2000 Å thick for Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements, and 1.0 mm diameter and 100 Å thick for internal photoemission.

The apparatus for internal photoemission (IPE) spectroscopy includes a quartz tungsten halogen lamp source, a Jarrell Ash double monochromator (1180 l/mm grating, blazed at 6000 Å), an optical chopper and a lockin amplifier. The incident light power was measured with a Labmaster Coherent photon detector.

The figure shows I-V data on a semilogarithmic plot for four contacts on one of the (000-1) C-face samples. Extended regions of linearity are required for extraction of the Schottky barrier height.

Table 1 shows SBH for two different sets of 6H SiC samples, indicated as (a) and (b). Table 2 shows SBH for a single set of 4H SiC samples. For I-V and C-V measurements each sample has 4-20 contacts. For IPE measurements each sample has 1-4 contacts. The tabulated uncertainties, which are likely due to spatial inhomogeneity of the SBH [1], are based on both experimental uncertainty and the statistical distribution of values.

Table 1		Schottky	Barrier	Heights	[eV]
6H		**(0001) Si**	**(000-1) C**	**(1-100)**	**(1-210)**
I-V (n-ideality factor)	a	0.98±0.03 (n=1.15)	1.01±0.03 (n=1.15)	- -	0.95±0.03 (n=1.21)
	b	0.92±0.05 (n=1.21)	0.94±0.03 (n=1.15)	0.89±0.03 (n=1.24)	0.82±0.03 (n=1.68)
C-V	a	1.37±0.05	1.46±0.05	-	1.31±0.05
	b	1.26±0.05	1.31±0.05	1.24±0.06	1.32±0.08
IPE	a	1.38±0.05	1.41±0.05	1.36±0.05	-

Table 2	Schottky	Barrier	Heights	[eV]
4H	**(0001) Si**	**(000-1) C**	**(1-100)**	**(1-210)**
I-V (n)	1.34±0.03 (n=1.06)	1.41±0.04 (n=1.05)	1.35±0.03 (n=1.09)	1.33±0.03 (n=1.08)
C-V	2.10±0.09	2.13±0.05	1.93±0.15	2.03±0.08
IPE	1.43±0.05	1.45±0.05	1.62±0.05	1.55±0.05

There are two trends in the dependence of the SBH on crystallographic orientation for 6H and 4H SiC. First, the samples with Pt on the (000-1) carbon face have higher SBH than the (0001) silicon face for all samples. This phenomenon was observed before [2,3], but to the best of our knowledge there has not been a satisfactory explanation. Second, the samples with basal plane orientation ((0001) and (000-1)) have higher SBH than the samples with (1-100) and (1-210) orientations for the majority of the samples. The comparatively large SBH measured by C-V for the (1-210) 6H SiC sample from Set (b) may be due to poor surface morphology. For this sample, there was only one high quality contact, which happened to have a high value for the SBH.

The relationship $\varphi_B = S(\varphi_m - \chi) + (1-S)(E_g - \varphi_0)$, where φ_B is the Schottky barrier height, φ_m the work function of the metal, χ the electron affinity of the semiconductor, E_g the energy gap and φ_0 the pinning level due to interface states is commonly used to interpret measurements on Schottky barriers. The coefficient S provides an interpolation between the Mott-Schottky (S = 1) and Bardeen (S = 0) limits. SiC is an intermediate case. In this work, we are considering areal densities of (idealized) SiC surfaces with 0.122 Si atoms/cm^2 for (0001), 0.122 carbon atoms/cm^2 for (000-1), or equal areal densities of 0.064 and 0.074 Si or C atoms/cm^2 for (1-100) and (1-210), respectively. In addition, the ideal (1-210) surface is atomically flat, whereas the (1-100) surface is not [4]. The surface double layer, and correspondingly the double layer for the metal-semiconductor interface, will likely be different for each crystallographic face [5]. Surface passivation, reconstruction, contamination, defects, etc., may also contribute. The larger atomic areal densities on the (1-100) and (1-210) faces may give rise to larger electron affinities, and thus lower Schottky barriers, a trend displayed by the data in Tables I and II.

This work was partially supported by the Office of Naval Research (Contract N00014-01-1-0028) and the NASA Glenn Research Center (Contract NAG3-2538).

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Hall Measurements on Inversion and Accumulation-Mode 4H-SiC MOSFETs

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Inversion and accumulation-layer electron mobility in n-channel 4H-SiC MOSFETs have been investigated using the Hall effect. In the inversion-mode MOSFETs, Hall mobilities of ~60-70 cm^2/V-s were obtained compared to a field-effect mobility (μ_{FE}) of ~5 cm^2/V-s. Accumulation-layer electron mobilities (μ_{acc}) of ~350 cm^2/V-s [1] and 200 cm^2/V-s were extracted on samples with different channel doping concentrations. In contrast, the μ_{FE} under accumulation was ~2-3 cm^2/V-s.

N-channel inversion- and accumulation-mode MOSFETs were fabricated on the same chip, starting with p-type 4H-SiC epilayers. The channel region in the accumulation-mode MOSFETs was implanted using nitrogen with a total dose of 1×10^{12} cm^{-2} and 3×10^{12} cm^{-2} in the "wet" and "dry" oxide samples respectively.

Carrier concentration (N_{inv}) and Hall mobility (μ_{Hall}) were extracted with MOS-gated bar structures. Fig. 1 shows the N_{inv} vs. V_G in the inversion-mode MOSFETs on the "wet" oxide sample for temperatures ranging from 25°C to 125°C. N_{inv} increases with increasing temperature due to the reduced trapping of inversion carriers by the interface traps at higher temperatures. Fig. 2 shows μ_{Hall} vs. V_G in the wet oxide sample for different temperatures; μ_{Hall} increases from ~70 cm^2/V-s at 25°C to ~150 cm^2/V-s at 125°C. The increase in μ_{Hall} with increasing temperatures is attributed to a decrease in coulombic scattering. N_{inv} and μ_{Hall} obtained on the "dry" oxide sample had similar temperature behavior. The interface trap density ($D_{it}=d(Q_F+Q_{it})/d\varphi_s$), extracted using Hall measurements, was slightly higher in wet oxide sample (~8×10^{13} cm^{-2} eV^{-1} at E_C-E=0.1eV) compared to dry oxide sample (~5×10^{13} cm^{-2} eV^{-1} at E_C-E=0.1eV) as shown in Fig. 3; the integrated trapped charge density in the wet oxide sample is larger.

N vs. V_G in accumulation-mode MOSFETs on the "wet" oxide sample extracted at temperatures ranging from 25°C to 125°C is shown in Fig. 4. At large V_G, under accumulation, the increase in N with temperature is due to the reduced trapping of field-induced accumulation electrons in the interface traps. Since the conduction of electrons occurs through both the bulk and a surface accumulation layer, μ_{Hall} extracted (Fig. 5) is a combination of the bulk and accumulation-layer mobility. μ_{acc} is extracted from the slope of the sheet conductance (σ_s) vs. N (as $(1/q)(d\sigma_S/dN)$. At room temperature, μ_{acc} in the wet oxide sample decreases from the bulk value (~350 cm^2/V-s) to 200 cm^2/V-s in strong accumulation (Fig. 6). The decrease in μ_{Hall} and μ_{acc} with increase in temperature is attributed to phonon scattering. Similar results on N, σ_S, μ_{Hall}, μ_{FE} and μ_{acc} have been obtained on the dry oxide sample.

The large difference between μ_{Hall} and μ_{FE} in the inversion-mode MOSFETs and μ_{acc} and μ_{FE} in the accumulation mode MOSFETs is attributed to the trapping of the field-induced carriers in the interface traps. At higher temperatures, a larger fraction of the field-induced charge contributes to the conduction resulting in an increase in μ_{FE}. Dry oxidation results in a lower interface trap density in inversion mode MOSFETs compared to wet oxidation resulting in a better transconductance, lower threshold voltage, better sub-threshold characteristics and higher carrier concentration. This work, for the first time, has separated the bulk and surface mobility of electrons in accumulation-mode MOSFETs using Hall measurements.

Acknowledgements: Authors from RPI would like to acknowledge support of this work by Philips Research, MURI, DARPA and CPES.

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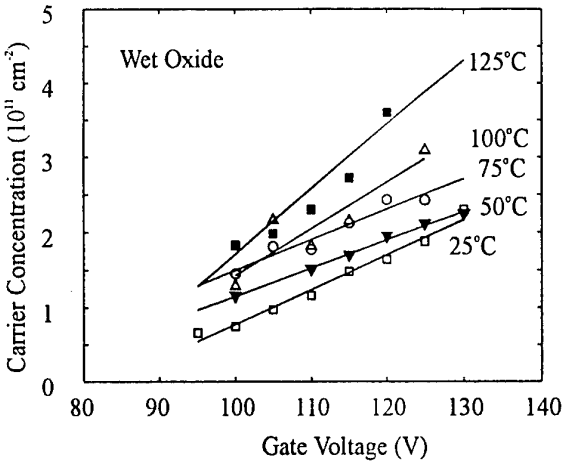


Fig. 1: Carrier concentration vs. gate voltage in inversion-mode MOSFETs in the wet oxide sample at high temperatures.

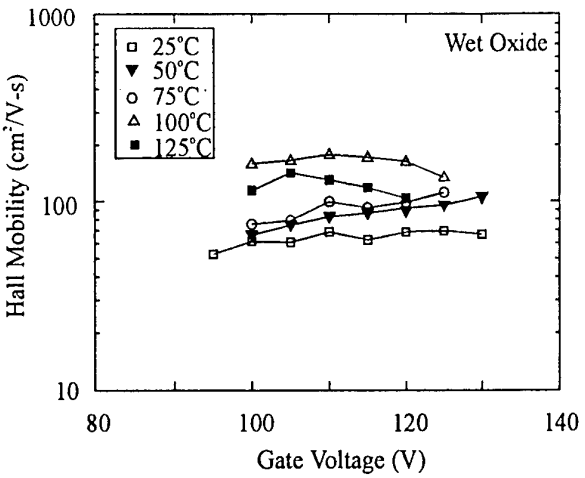


Fig. 2: Hall mobility in inversion-mode MOSFETs in the wet oxide sample at high temperatures.

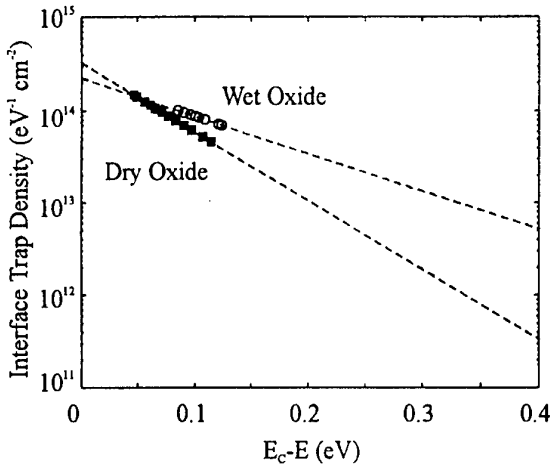


Fig. 3: Comparison of interface trap density in inversion-mode MOSFETs in wet and dry oxide samples.

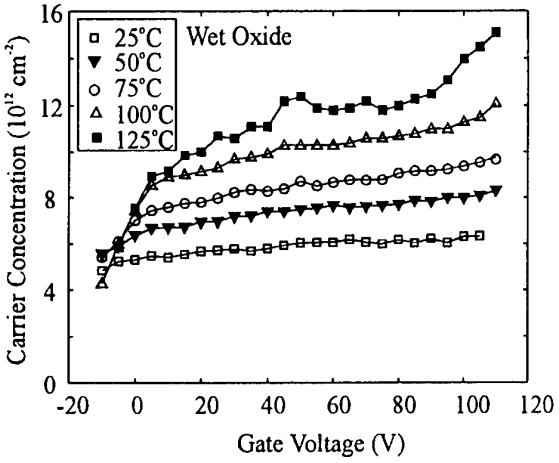


Fig. 4: Carrier concentration vs. gate voltage in accumulation-mode MOSFETs in the wet oxide sample

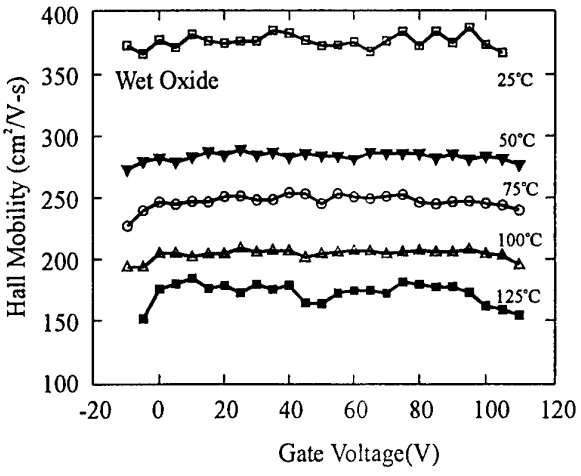


Fig. 5: Temperature dependence of Hall mobility in accumulation-mode MOSFETs in wet oxide sample.

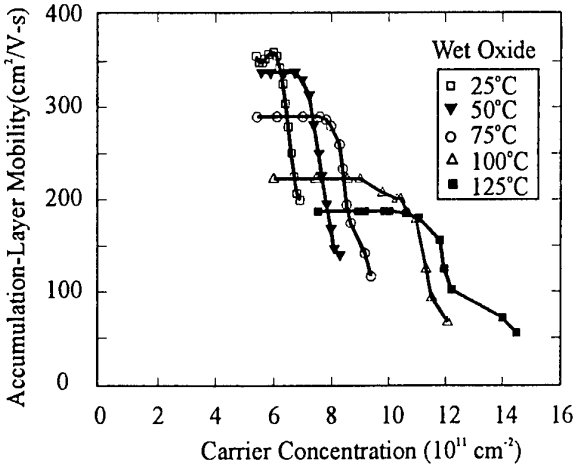


Fig.6: Accumulation-layer electron mobility in the wet oxide sample for different temperatures.

Quantitative high resolution two dimensional profiling on SiC by scanning capacitance microscopy

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Scanning Capacitance Microscopy (SCM) is one of the most interesting two-dimensional (2D) carrier profiling techniques in Silicon, and recently some attempts have been made to apply SCM to SiC. On the contrary, very little attempts have been done in order to quantify SCM doping profiles measured on SiC. We successfully performed reproducible measurements and quantification of the SCM profiles.

N^+ and Al^+ were implanted in the energy range 20 - 200 keV both in p- and n-type 6H-SiC substrates. The implants were performed at a temperature of 500 - 800 °C. The samples were annealed at a temperature higher than 1300 °C in Si supersaturated ambient. Secondary Ions Mass Spectroscopy (SIMS) has been performed to obtain the chemical profiles.

SCM measurements were performed on cross-sectioned n- and p-type 6H-SiC implanted and annealed samples, but a quantification of the SCM profile was carried out for unipolar samples, only since the direct inversion technique delivers reliable results when there is no junction. A DC bias of 1 Volt and an AC bias of 1 Volt peak to peak were applied to the sample to perform the SCM measurement. In fig.1 we report the SCM profiles measured on the n-type sample implanted with two doses of 1×10^{14} and 5×10^{14} cm^{-2}, respectively. The ion implanted region in the high resistivity 4 μm epitaxial layer and the underlying low resistivity substrate can be clearly identified. The two well defined (and known) concentration levels represents the ideal case for the quantification of SCM.

Reproducible measurements, being crucial for quantification, have been obtained by developing an appropriate sample preparation that will be described in details.

The direct inversion technique, we applied in order to perform the conversion of the SCM profiles to carrier concentration profiles is based on an extended database of capacitance-to-voltage curves obtained by solving the Poisson equation for the metal-insulator-semiconductor system. The metallic tip is described as a parabolic shaped gate contact terminating with a hemisphere of radius r. The tip is surrounded by air (modelled by a dielectric material with relative dielectric constant K_{air}=1). The thin oxide grown by low temperature oxidation is modelled by a uniform silicon dioxide layer (K_{oxide}=3.9) with thickness t_{ox}. The fixed charge density and the interface state density is assumed to be zero. The work function difference between metal and semiconductor is also taken into account. An uniform n-type dopant concentration N_d is assumed in the 6H-SiC substrate and another metallic contact is put on the back side. A voltage V is applied to the tip gate contact, while the back contact is assumed to be grounded. Because of the cylindrical symmetry of the system with respect the tip axis, the problem is basically 2-dimensional (2D). The 2D Poisson equation has been solved by the finite element method, by providing the charge distribution in the semiconductor and the induced charge on the tip for a given bias V. The differential capacitance C=dQ/dV is calculated by variation of the applied AC bias from 5 Volts to -5 Volts, yielding the C-V curve of a MOS capacitor, which ranges from the accumulation to depletion regime. The database produced, according to this scheme, includes 600 C-V curves (see Fig. 2). The calibration curve plotted in fig. 3 has been calculated for an applied DC bias of 1 Volt. It represents the calculated capacitance variation

dC (10^{-18} Farad) produced in the MOS system by a voltage variation dV=1 Volt (peak-to-peak) for different uniform concentration levels.

In fig. 4a and in fig. 4b we report the converted SCM profiles and the corresponding SIMS profiles for n-type 6H-SiC samples implanted at 500 °C with 200 keV N^+ ions respectively with doses 1×10^{14} cm^{-2} and 5×10^{14} cm^{-2} and then annealed at 1300 °C for 1 hour. The electrically active fractions estimated from converted SCM profiles are in good

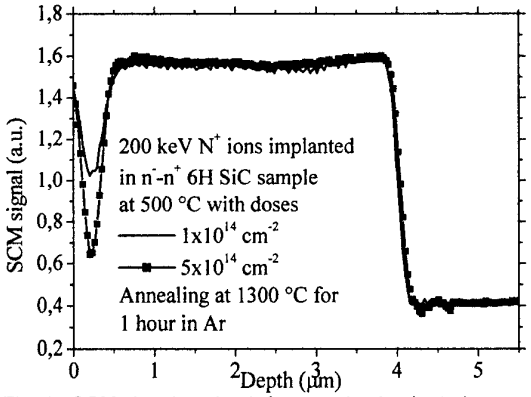


Fig. 1 - SCM signal vs depth for samples implanted with 200 keV N^+ at two different fluences

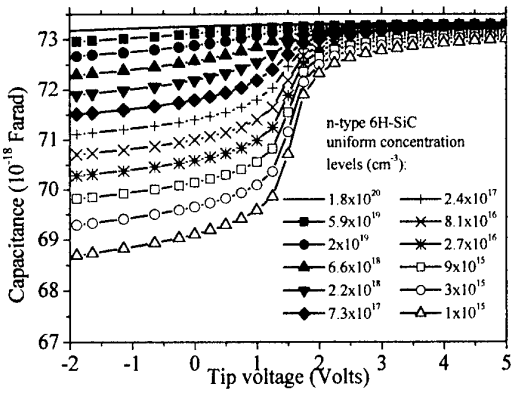


Fig. 2 - Calculated capacitance versus tip voltage for different concentration .

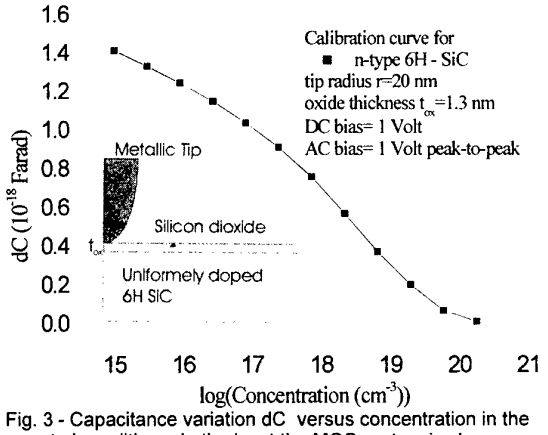


Fig. 3 - Capacitance variation dC versus concentration in the reported conditions. In the inset the MOS system is shown.

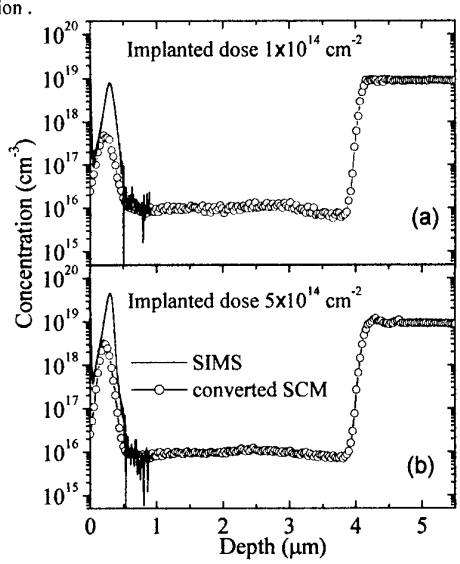


Fig.4 - Concentration profiles obtained by SCM and SIMS measurements for the two implanted samples.

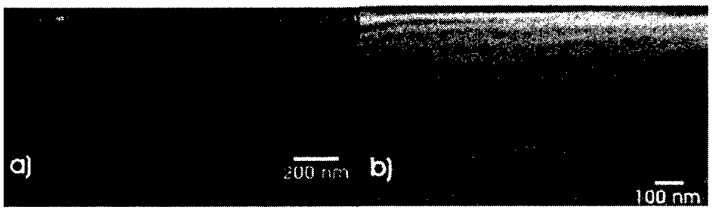


Fig. 5 – TEM analyses of samples implanted with N a) and Al b) and anneled at 1300 °C.

agreement with those obtained by Hall measurements (10%). A quite lower activation has been obtained for Al^+ implanted samples. Transmission electron microscopy allowed to image the defects present in the implanted and annealed samples. Loop dislocations were observed in the N^+ implanted sample while precipitates were present in the Al^+ implanted samples (see Fig. 5). A correlation with the electrically active profile has been done.

Scanning Capacitance Microscopy of SiC Multiple pn Junction Structure Grown by Cold-wall Chemical Vapor Deposition

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Silicon carbide is the most promising material for ultra-low-loss power switching devices because of its high breakdown field. Sophisticated (or complicated) device structures are required to accomplish a full potential of SiC in device performance. To fabricate such structures, device processes such as local impurity doping are extensively studied. It is also important to establish characterization techniques to evaluate such structures. Capacitance-voltage (*C-V*) measurement and secondary ion mass spectrometry (SIMS) are widely used for such a purpose. But these techniques are basically for one-dimensional (1-D) profiling. 2-D or 3-D analyses are needed for real device structures.

Scanning capacitance microscopy (SCM) is recently developed as one of scanning probe microscopy (SPM) techniques. This technique has realized a great success in 2-D doping profiling in Si VLSI-device technology. There are, however, only a few reports on SCM of SiC [1,2]. In this study, we demonstrate SCM of SiC multiple pn junction structure. The SCM result is discussed with SIMS analysis and a scanning electron microscope (SEM).

A sample used in this study was grown by atmospheric-pressure chemical vapor deposition (APCVD). A cold-wall type reactor was used, which is suitable for abrupt changing of doping gas (less memory effect compared to hot-wall CVD). Nitrogen (N_2) and diborane (B_2H_6) were used for n-type and p-type doping gases, respectively. The substrate was off-axis n-type 4H-SiC (0001). SCM was carried out with Digital Instruments D-3100 SPM system with a CoCr-coated conductive probe. The sample for SCM was prepared by a simple cleavage method.

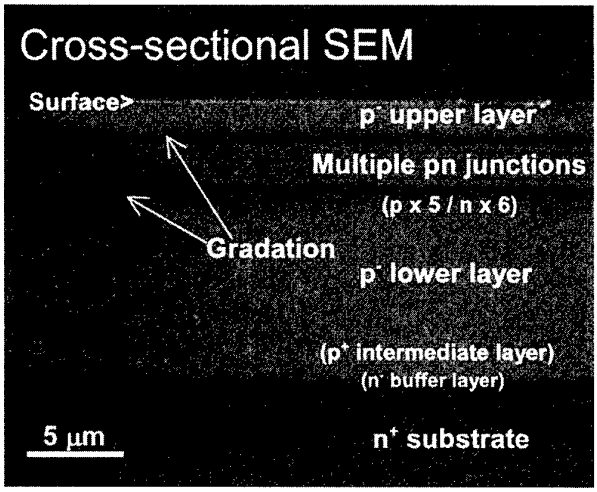


Figure 1: Cross-sectional SEM image for 4H-SiC multiple pn junction structure.

SIMS analysis revealed that uniform and abrupt multiple pn junctions are successfully fabricated. The concentration of both N and B atoms for 0.25 μm-thick n- and p-layers in multiple pn junctions is $1.5x10^{17}$ cm^{-3}.

Figure 1 shows a cross-sectional SEM image obtained with an acceleration voltage of 5 kV. A SEM is useful to determine pn junction structure. Because the efficiency of secondary electron collection depends on the potential of each portion, an SEM image reflects the potential distribution. Since an n-type region is positively charged, the collection efficiency is smaller than that of p-type region. Therefore, an n-type region appears as a dark contrast in a SEM image. Five bright stripes correspond to p-layers in multiple pn junctions. The widths of stripes are very uniform, consistent with a SIMS analysis. Six dark stripes correspond to n-layers. The gradation observed at the both sides of multiple junctions originates from the depletion layer between n-layer and p^- upper/lower layers. From the depletion layer widths, the doping concentrations of p^- upper and lower layers can be calculated to be $2x10^{15}$ cm^{-3}, $7x10^{14}$ cm^{-3}, respectively, which agrees with the doping levels expected from the CVD growth condition.

AFM (topology) and SCM (capacitance) images are shown in Fig. 2. Since there is no special feature in AFM images, the SCM image originates from local electrical properties. A positive dC/dV signal corresponds to p-type, and a larger $|dC/dV|$ signal means lower doping concentration. The polarity of observed SCM signal (Fig. 3) agrees with the SEM observation. For n-layers, the signal intensity is also consistent with the doping level of each layer. For p-layers, however, the p^- layer has a small dC/dV signal in spite of its light doping. Because the resistivity of B-doped layer with an acceptor concentration of $7x10^{14}$ cm^{-3} is, at least, $> 10^3$ Ω-cm. The SCM measurement was affected by the high series resistance. Combination with a SEM as well as SIMS is very effective to understand the SCM signal. The bias voltage dependence of SCM signal will be also discussed.

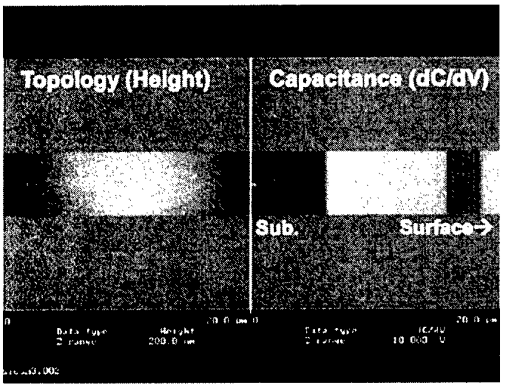


Fig. 2: Cross-sectional AFM and SCM images.

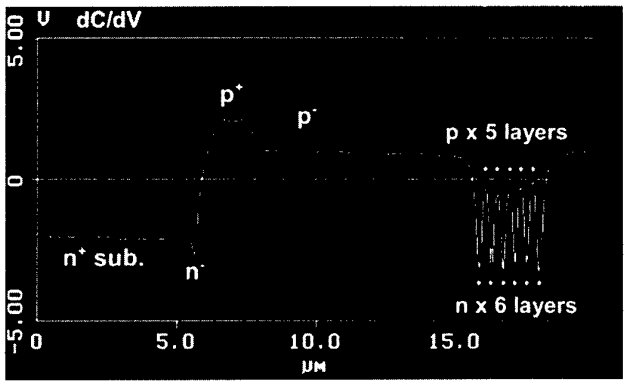


Figure 3: SCM signal along growth direction.

1. N. Nordell, S. Karlsson, and A. O. Konstantinov, Mat. Sci. Forum **264-268** 131 (1998).

2. A. Schöner, S. Karlsson amd T. Schmitt *et al.*, Mat. Scoe. Symp. Sroc. **512** 469 (1998).

WeA3 Shottky Barrier Diode

[redacted]

Advances in SiC material and technology for Schottky diodes applications

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Keywords : SiC – Schottky – diode – epitaxy - ion implantation - defect

Even when sampling and mass-production of Silicon Carbide Schottky diodes have just started, many studies are carried out on the "next generation" of devices. These R&D fields mainly concern the crystal quality improvement of large diameters 4H-SiC wafers but also the availability of accurate processes for reliable, lost cost and efficient devices. Therefore, the aim of this paper is to make a state of the art of the present research activities.

For the "bulk material", including the epitaxial growth, strong developments are dedicated to the reduction of structural defects. The electrical effects of specific defects like micropipes, scratches and dislocations were already published, showing either strong correlations between active area of devices and defect densities, or no influence on the electrical behaviour. At the present time, defect densities in the range of 10^0 and 10^3 cm^{-2} are obtained for micropipes and dislocations, respectively. Many researchs are also focused on the reduction of the low surface mosaïcity. Some correlations have been made between white beam X-rays topographies, FWHM rocking curves and electrical characteristics of Schottky diodes. Finally, accurate parameters are needed in epitaxial growth to get powerful devices. The key points concern the way to obtain reproducible and homogeneous doping level; this last parameter having a strong influence on the reverse characteristics and power losses.

For the device processing developments, the three main researchs are :

- the way to get reliable and efficient metallization processes; which are mainly based on Ti and Ni for Schottky and ohmic contacts, respectively. With Ti, the crucial point is the control of a stable barrier height that must be as low as possible to combine low forward drop voltage and low reverse leakage current. Additionally, the quality of the epitaxial layers strongly influences the metallization process.
- how to obtain powerful edge termination process; thus ensuring the lowest influence on the device; the goal is to get localized P-type regions. Beside the epitaxial approach, many works are based on ion implantation. Improved processes combine targeted doping levels and low surface roughness, even after high temperature post-annealing treatment.
- the control of efficient and high reliability passivations. Strong works concern the control of a good SiO_2/SiC interface. For Schottky diodes, high charge rates and/or high surface potential fluctuations can induce long term instabilities; nowadays, oxide charges in the range of 10^{11} cm^{-2} can be obtained. Using secondary passivation like polyimide on the top of the primary oxide layer, 600V Schottky diodes have demonstrated yields in the 50-75% range and promising aging features, even after 1000h @ 250°C.

All these R&D fields allow the manufacturing of reliable and powerful SiC Schottky diodes, which will supersede present Si bipolar diodes.

Development of 600 V / 8 A SiC Schottky Diodes with epitaxial edge termination.

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Thanks to its excellent properties such as high breakdown voltage and high thermal conductivity, 4H-SiC has emerged as the material of choice for power devices. Silicon carbide Schottky diodes are now coming on the market and can replace bipolar Si diodes for applications such as PFC converters, providing superior switching characteristics resulting from the absence of minority carriers.

Edge terminations, which consist of local p-type areas, are needed for all devices such as diodes operating over one hundred volts. They can be made by two ways. The first way is to perform localized ion implantation: this process requires very high temperature annealing to provide activation of the dopants (typically 1500 to 1700 °C for acceptor dopants in SiC). Processing at these temperatures is very critical due to the evaporation of SiC which causes surface damage. The other way is to deposit a p-type epilayer on top of the n- layer, and to etch this layer locally to provide the Schottky contact. Our paper will describe the development of high performance 600 V SiC Schottky diodes using epitaxial edge termination.

Process issues will be discussed in the paper. All devices are developed on 50.8 mm n-type substrates from Cree. The structure of the device is shown on figure 1.

Epitaxy: As shown on figure1, the stacking consist of three epilayers: N+ buffer layer; N- drift layer, and P-type edge termination layer. Epilayers are deposited at CEA/LETI, in an Epigress VP508 hot wall reactor.

Device processing: The fabrication of the devices required the development of key process steps such as:

- Patterning of Mesa structures with vertical slope using high density dry etching (fig. 2);
- Developing of specific lithography process compatible with the presence of the Mesa structures;
- Passivation process, using conventional silicon-technology materials (fig. 3), and providing high reverse voltage with high reliability.

Electrical performance: figure 4 shows typical reverse characteristics obtained on the devices. More detailed electrical results will be given, including reliability tests. Yield results will also be discussed.

As a conclusion, we have developed a process for manufacturing high performance 600 V SiC Schottky diodes. This process uses epitaxial p-type edge termination, which avoids penalizing process steps such as high temperature (1500-1700 °C) annealing required when using implanted p-type edge termination.

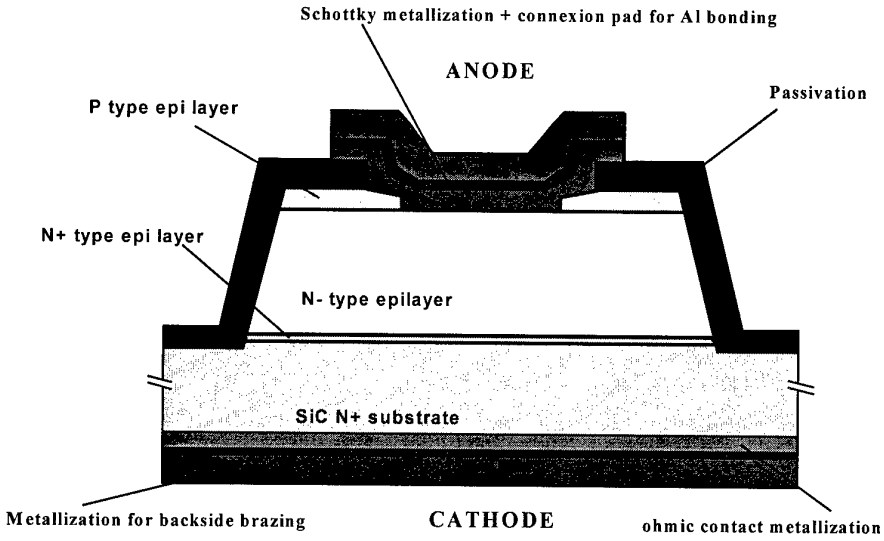


Figure 1: structure of 600 V Schottky diode using epitaxial edge termination.

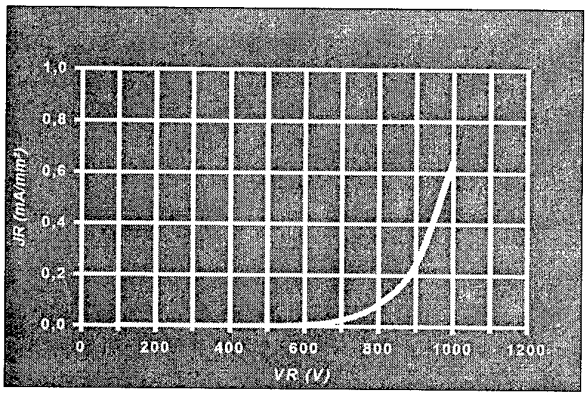


Figure 2: SEM cross sectional view of test pattern for Mesa vertical etching.

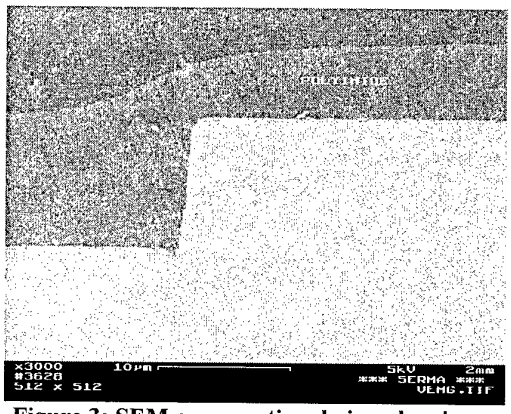


Figure 3: SEM cross sectional view showing passivation layers.

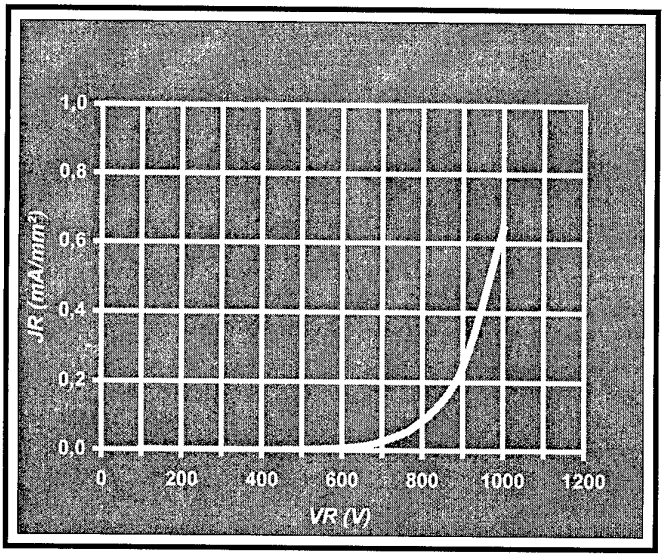


Figure 4: typical reverse bias characteristic of the diodes

Performance of SiC Bipolar (PiN) and Unipolar (SBD) Power Rectifiers in Current-Voltage-Frequency Parameter Space

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To select the optimal device for a particular application, power circuit designers must carefully analyze the tradeoffs between competing devices. Recent progress in SiC power rectifiers has resulted in the demonstration of high-voltage and high-current PiN and Schottky barrier diodes (SBDs) [1-3]. With both technologies maturing, power electronics engineers face the task of selecting between these two devices. Until recently, the choice was simple, since silicon SBDs are only available for relatively low voltage applications. The choice is not as clear when considering SiC diodes, and guidelines for determining the proper application of each are needed. This paper provides such guidelines, based on a simple, yet complete analysis of the tradeoffs involved.

The selection criteria used in this analysis can be summarized as follows: An application is defined as a unique combination of forward current density J_F , reverse voltage V_R , and switching frequency f. The appropriate choice of rectifier is the device which requires the least area for a given application. Therefore the device that carryies the highest current density J_F without exceeding the maximum power dissipation allowed by the package is the proper choice. We assume both PiN and Schottky diodes are independently optimized for each application, specified by a particular set of performance parameters (J_F, V_R, f). This requires independent optimization of the blocking layer thickness and doping of both diodes, and appropriate adjustment of the ambipolar lifetime τ_A in the PiN diode for each reverse voltage considered.

An ideal application for SiC rectifiers is as a replacement for the silicon fly-back rectifiers in inductive load switching circuits, such as electric motor drives. The components of power dissipation associated with the fly-back rectifier can be divided into two general categories: static and dynamic power. Static power includes power dissipated by the diode when in either the forward conduction or reverse blocking state. Dynamic power includes any energy dissipated by the circuit during switching events that can be directly attributed to the presence of the diode. Since these energy losses occur each time the circuit switches, the dynamic power dissipation is proportional to switching frequency. All power dissipation components are expressed as power densities, in units of W/cm^2.

The desired switching frequency determines which device technology provides the best solution for a given application. To illustrate the general framework for our comparison, Fig. 1(a) plots the maximum allowable current density $J_{F(MAX)}$, subject to the constraint that the total power dissipation equals the package limit, as a function of switching frequency for both types of devices. Since power dissipation in SBDs is essentially independent of frequency, $J_{F(MAX)}$ can remain almost constant as f is increased. However, power dissipation in a PiN diode increases with f, so the static loss must be reduced as f is increased to satisfy the package power limit. This requires increasing the area of the diode, which reduces the forward current density $J_{F(MAX)}$.

For each application there is a unique crossover of the PiN and SBD $J_{F(FMAX)}$ vs. f characteristics. Above this frequency any PiN, however well optimized, is less efficient than an optimized SBD. This crossover frequency can be determined for a range of operating voltages V_R . Figure 1 (a) can be thought of a constant-voltage slice in three-dimensional (J_F, V_R , f) space, as illustrated in Fig. 1(b). The resulting data can be best presented by projecting these crossover points onto the f - V_R plane.

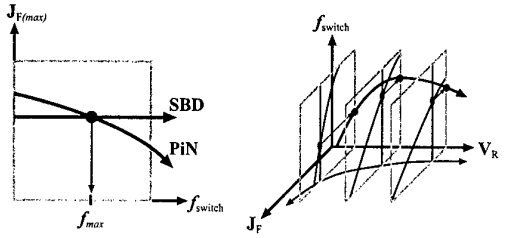


Figure 1: General framework for comparing bipolar (PiN) and unipolar (SBD) devices. We first find the frequency f_{MAX} at which the maximum J_F of PiNs and SBDs are equal, subject to the power dissipation limit of the package (a), and then we repeat for several voltages V_R, and project the resulting locus onto the f vs. V_R plane (b).

The result of this analysis, using a package dissipation limit of 1 kW/cm^2, is shown in Fig. 2. The bold curve is the frequency f_{MAX} at which a PiN diode has the same efficiency as a Schottky. For applications requiring switching frequencies above this curve, the PiN requires more area than the SBD and thus the SBD is preferred. For applications requiring lower frequencies, the PiN is preferred.

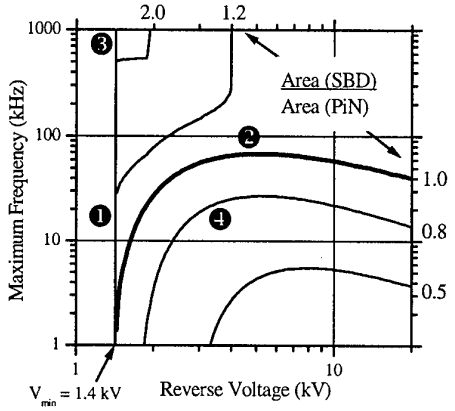


Figure 2: Contour plot of the area ratio for a 4H-SiC PiN diode relative to a 4H-SiC SBD as a function of V_R and f, assuming a package limit of 1 kW/cm^2, a 50% duty cycle, and a 50% voltage derating factor.

Referring to Fig. 2, the following conclusions can be drawn from this analysis: Region 1: PiNs require more area than SBDs for any $V_R < 1.4$ kV. Region 2: PiNs require more area than SBDs for $f > 70$ kHz, *regardless of voltage rating* V_R. (However, for $V_R > 4$ kV the difference is small, and other factors may determine the appropriate choice.) Region 3: SBDs are *highly* preferred at $V_R < 4$ kV for high frequency operation (> 300 kHz). Region 4: PiNs are preferred for $V_R > 2$ kV and $f < 30$ kHz. These general conclusions apply for other choices of package power dissipation limit, although the boundaries between the different regions change. These guidelines, with slight modifications, also apply to the analysis of other bipolar and unipolar devices, such as BJTs vs. power MOSFETs. More details of the analysis will be presented at the conference.

This work is supported by the Office of Naval Research under MURI grant N00014-95-1-1302.

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[2] R. Singh and J. W. Palmour, "High Temperature Characteristics of 8.6 kV 4H-SiC PiN Diode", *Proc. High Temperature Electronics Conf.*, Albuquerque, NM, June 13 - 15, 2000.

[3] H. M. McGlothlin, et al., "4 kV Silicon Carbide Schottky Diodes for High-Frequency Switching Applications," *IEEE Device Research Conf.*, Santa Barbara, CA, June 28 - 30, 1999.

4H-SiC MPS Diode Fabrication and Characterization In an Inductively Loaded Half-bridge Inverter up to 100 kW

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In this work, 600V 4H-SiC MPS diodes were designed, fabricated, packaged, and tested. The cross sectional view of the MPS diode is shown in Fig.1. The starting material used in the diode fabrication were 4H-SiC wafers purchased from Cree Research, Inc. with a 10μm $2.1x10^{16}cm^{-3}$ or 6μm $1.4x10^{16}cm^{-3}$ doped n^- epilayer on n^+ substrate. Multiple energy Al implantation was done to create simultaneously the p-region rings in the device active area and the p region for multi-step junction termination extension (MJTE). Implanted samples were annealed at 1,550°C for 30 min. The MJTE was formed by thinning the implanted region at the device periphery using dry etching. Thermal oxide with thickness 600Å and 1 μm LPCVD oxide were grown for surface passivation. Ni was sputtered on the substrate and annealed at 1050°C for 10 min in Ar forming gas to form ohmic contact. Contact windows in the oxide were opened by wet etching and Ti Schottky contact metal was then deposited by sputtering and defined by standard lift-off process. Finally Au layers were deposited over the contacts and multiple 1mm diameter cells were packaged in single packages, forming multi-cell high current capacity MPS diodes. The packaged devices were tested under DC conditions at temperatures up to 250°C. The termination technique used was shown to ensure excellent blocking voltages. The targeted blocking voltage was 600V, however the best blocking voltage for 1mm single-cell MPS diode was more than 900V. The highest blocking voltage measured on a small area control diode was 1550V and 1000V, respectively, for the 10 and 6 μm structures. They correspond to parallel-plane electric fields of 2.9MV/cm and 3.1MV/cm, respectively.

The diodes reverse voltage I-V characteristics (Fig.2) show excellent suppression of the Schottky reverse leakage current at temperatures up to 250°C. Forward I-V curve shows $291A/cm^2$ at Vf=1.5V and $1493A/cm^2$ at Vf=4V at room temperature. The highest forward current capability of a packaged 600V diode is 140A at 4V (Fig.2 (a)). SiC MPS diodes turn-off characteristics were tested from room temperature up to 250°C and compared to the characteristics of similarly rated commercially available ultrafast Si PIN diodes (Fig.3). Switching results of SiC MPS diode in an inductively loaded half-bridge inverter will be presented for up to 100 kW at RT, and 400V - 145A at 250°C. The substantial reduction of the diode reverse recovery current leads to a substantial decrease in the diode dissipated switching energy. At room temperature the diode energy loss reduction is 47%, and at 200°C the reduction is 84%. Our packaged SiC MPS diodes, as opposed to Si diodes, can be safely operated at temperatures around 250°C with energy losses comparable to the losses of Si diodes at room temperature. The use of SiC MPS diodes reduces not only the diode reverse recovery losses but also the losses in the IGBT switch. The IGBT energy loss reduction when a SiC MPS diode is used is 15% at room temperature and 45% at 150°C. It is clear that even using the existing Si IGBT switches the substitution of Si diodes with SiC diodes could significantly improve the overall performance of motor control inverters. Comparison will be made among different designs and key issues for high performance will be discussed.

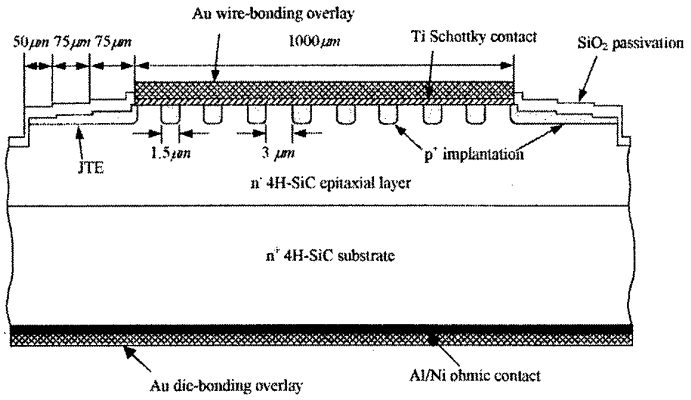


Fig.1: Cross-sectional view of a SiC MPS diode.

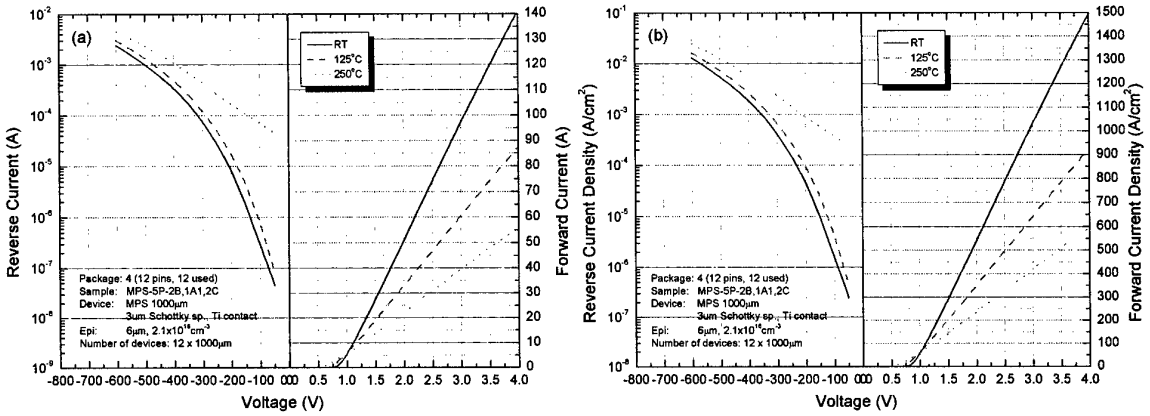


Fig.2: Current vs. voltage (a) and current density vs. voltage (b) of packaged multi-cell MPS diode on 6μm thick and $2.1\times10^{16}cm^{-3}$ doped epilayer, tested at room temperature, 125°C, and 250°C.

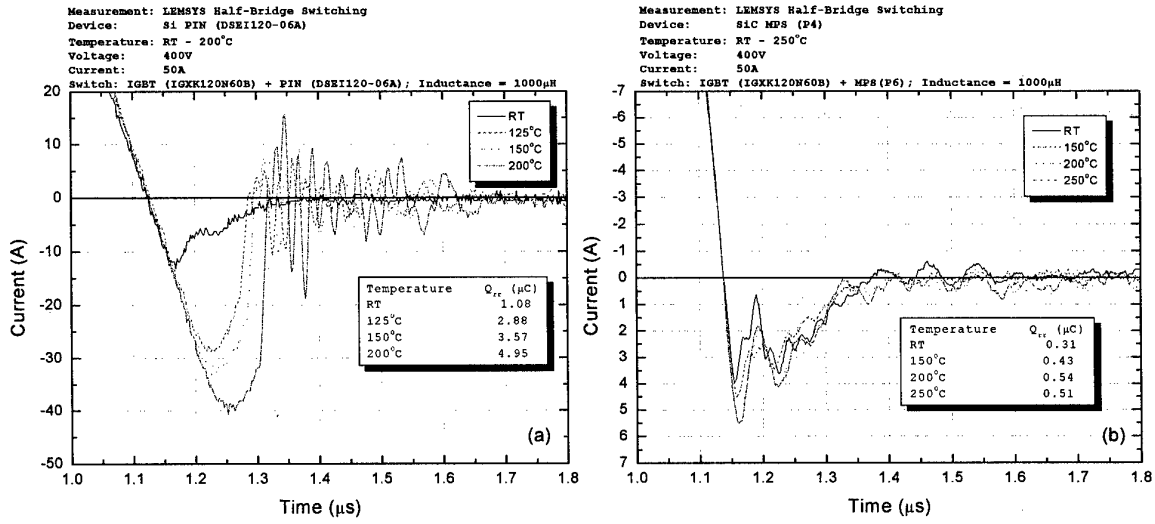


Fig.3: Reverse recovery part of the turn-off characteristics of an ultrafast Si PIN diode (a) and a SiC MPS diode (b) tested in an inductively loaded half-bridge inverter at different temperatures.

High-Voltage Pulse Instabilities in SiC Schottky Diodes with Implanted Resistive Edge Terminations

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Several reports have recently been published on pulse measurements of SiC PiN diodes [1, 2, 3]. Such measurements have been used to determine the temperature coefficient of breakdown voltage and to reveal breakdown voltage instabilities. High-voltage (HV) pulse characterization is performed by applying a fast (~ 5-50 ns risetime) reverse bias pulse to the device under test, and by monitoring the resulting transient voltage and current waveforms. A block diagram of the system used in this work is shown in Fig. 1.

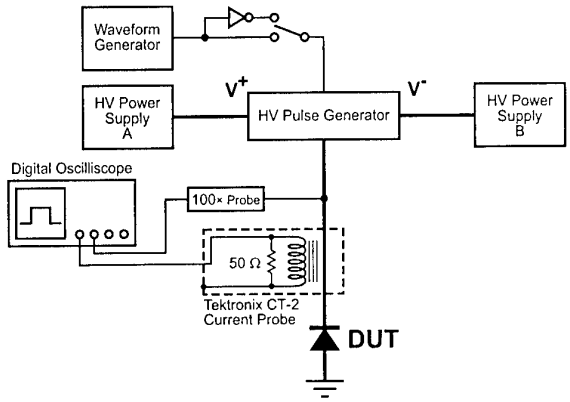


Figure 1: HV pulse characterization system

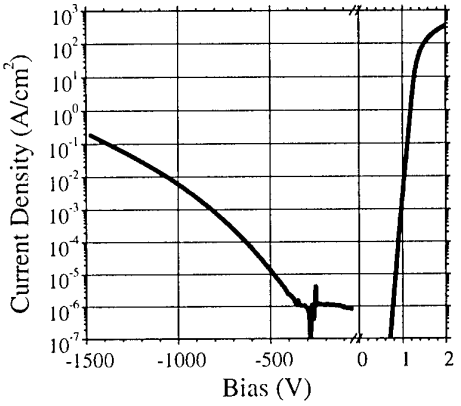


Figure 2: Nominal diode I-V characteristics

The study is conducted on 30 – 200 μm diameter circular Schottky diodes fabricated on an n-type 4H-SiC substrate with a 10 μm n-type epilayer doped 1×10^{16} cm^{-3} with nitrogen. A resistive edge termination is formed by implanting 1×10^{15} cm^{-2} boron atoms at 30 keV in 30 μm rings surrounding each diode. The implants are activated at 1050°C to remove lattice damage without activating the dopants [4]. Nickel Schottky contacts are deposited by E-beam evaporation and patterned by liftoff. Each diode is prescreened by measuring its static I-V characteristics, and only those that accurately reproduce the nominal characteristics shown in Fig. 2 are used in subsequent pulse testing. The reverse-bias measurements are limited to 1200 V to prevent damage.

Repetitive pulses similar to that shown in Fig. 3(a) are possible at low pulse amplitudes. Due to the limited resolution of the experimental configuration, reverse current cannot be measured for pulse amplitudes below approximately 200 V. As the pulse amplitude is increased above this threshold, the repetition rate must be progressively reduced to prevent damage to the devices. Reverse current waveforms at pulse amplitudes below ~300 V are relatively stable and repeatable. At pulse amplitudes between 300 V and 400 V the reverse current tends to increase with time and it is necessary to reduce the repetition rate to prevent device failure. Above 400 V it is impossible to reduce the repetition rate sufficiently, and single-pulse measurements must be used in order to capture useful data. Single-pulse capture is used for each measurement presented in this paper to insure repeatable results.

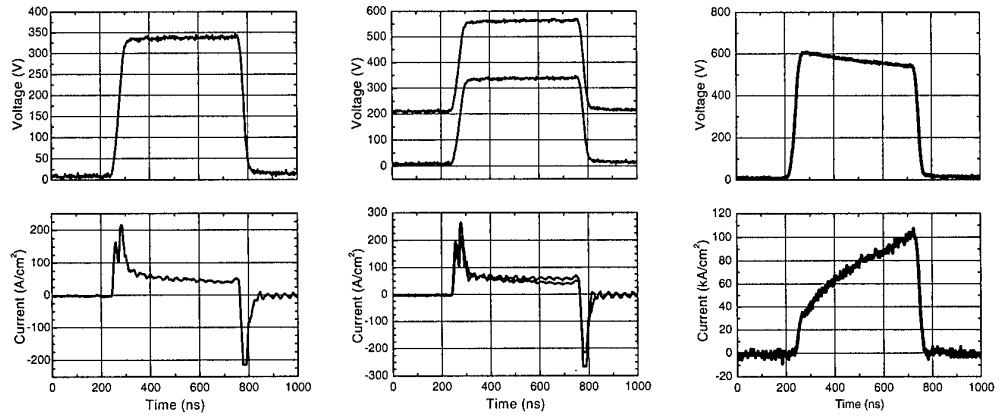


Figure 3. SiC Schottky barrier diode HV pulse characteristics
(a) 350 V pulse; (b) comparison of two 350 V pulses offset by a 200 V DC bias; (c) 600 V pulse

Figure 3(a) shows a typical measured pulse at an amplitude of approximately 350 V, and is characteristic of devices tested up to ~500 V. The magnitude of the pulse current (~50 A/cm^2) is many orders of magnitude higher than the static leakage current at the same bias (less than 1 μA/cm^2). This is the first of several indications that these devices do not behave properly under the application of fast high-voltage pulses. However, notice that the pulse current does show a negative temperature coefficient, indicating that at least at this amplitude the leakage mechanism is thermally stable. As illustrated in Fig. 3(b), the magnitude of the pulse current is dependent not on the maximum reverse bias, but on the *amplitude* of the pulse. This test is repeated for DC biases from 100 V to 1000 V using several different pulse amplitudes with the same result. When subjected to pulse amplitudes above 500 V, as illustrated in Fig. 3(c), the pulse current increases with time, indicating a thermally unstable condition. Every device subjected to *single-shot* pulses with amplitudes above ~ 500 V suffers catastrophic failure and is destroyed, regardless of the duration of the pulse.

We believe that the HV pulse instability illustrated above is caused by the deep-level traps introduced into the termination ring by implantation. The implanted boron impurities, which are intentionally not activated, produce a highly resistive surface layer. Shunt leakage through this layer under reverse bias results in a lateral voltage drop which reduces field crowding at the edge of the metal contact and increases the breakdown voltage of the device. However, when a high-speed pulse is applied to the device, the charge in these deep-level traps may not emit rapidly enough to follow the applied signal. The device then reacts as an unterminated device, breaking down between 200-400 V. The instability reported in this paper may limit the safe-operating-area (SOA) of SiC Schottky diodes fabricated with this termination method, or may require the use of an alternative edge termination.

This work is supported by the Office of Naval Research under MURI grant N00014-95-5-1302.

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WeB3 **Electrical Properties 2**

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Breakdown Fields along Various Crystal Orientations in 4H-, 6H-, and 3C-SiC

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To design power devices, breakdown field is one of the most important material parameters. For 6H- and 4H-SiC along the $\langle 0001 \rangle$ direction, the breakdown fields [1, 2] as well as the impact ionization coefficients [3, 4] of electrons and holes have been measured, and it was found that holes primarily involve in avalanche multiplication. The breakdown field is also known to have anisotropy: in 6H-SiC the breakdown field along the $\langle 11\bar{2}0 \rangle$ direction is approximately two thirds of that along the $\langle 0001 \rangle$ direction [5]. However, the anisotropy of breakdown field in 4H-SiC has not been reported. In this study, the breakdown fields along various crystal orientations in 4H-SiC were measured. In addition, the breakdown fields along the $\langle 001 \rangle$ direction in 3C-SiC and its corresponding directions in 4H- and 6H-SiC were also investigated.

To measure the breakdown field, epitaxial p^+n diodes were fabricated. Employing mesa structure, we can assume parallel-plane breakdown if the depletion region does not reach the bottom of mesa. The substrates used in this study were 4H-SiC (0001) with 8° off-axis toward $\langle 11\bar{2}0 \rangle$ and 4H-SiC $(11\bar{2}0)$ from Cree Research, Inc., 6H-SiC $(0\bar{1}1\bar{4})$ and 4H-SiC $(03\bar{3}8)$ from SiXON Ltd., and high-quality 3C-SiC (001) grown on undulated Si from HOYA corporation [6]. 6H-SiC $(0\bar{1}1\bar{4})$ and 4H-SiC $(03\bar{3}8)$ are semi-equivalent to 3C-SiC (001) in the sense that these faces are inclined by 54.7° toward $\langle 01\bar{1}0 \rangle$ from $(000\bar{1})$ and (0001), respectively. The epilayers were grown simultaneously in a horizontal cold-wall CVD reactor using SiH_4 and C_3H_8 as source gases and H_2 as a carrier gas. Nitrogen and trimethylaluminum were used as doping sources for n- and p^+-layers, respectively. The doping concentration and the height of mesa were designed for 4H-SiC (0001). In general, more nitrogen atoms are incorporated into other faces than (0001), which reduces the width of the depletion regions, leading to more accurate measurements.

Figure 1 shows typical *I-V* characteristics of the diodes fabricated on 4H-SiC $(11\bar{2}0)$ and $(03\bar{3}8)$ measured at room and elevated temperatures. The breakdown voltage clearly increases with increasing temperature, suggesting avalanche breakdown. The diodes fabricated on 6H-SiC $(0\bar{1}1\bar{4})$ showed similar tendency.

Figure 2 shows the breakdown fields calculated from the avalanche breakdown voltages at room temperature, together with the breakdown field in a literature [3]. The breakdown fields along 4H-SiC $\langle 11\bar{2}0 \rangle$ and 4H-SiC $\langle 03\bar{3}8 \rangle$ were found to be about 75% of that along 4H-SiC $\langle 0001 \rangle$. For 3C-SiC, the breakdown field along $\langle 001 \rangle$ should be at least the preliminary value found in Fig. 2 for the thickness of about 10 μm, but might be somewhat higher, since the yield of the diodes fabricated on 3C-SiC was much lower than those on other polytypes.

The authors would like to thank SiXON Ltd. for supplying 6H-SiC $(0\bar{1}1\bar{4})$ and 4H-SiC $(03\bar{3}8)$ substrates. The authors are grateful to HOYA corporation for providing high-quality 3C-SiC (001) substrates.

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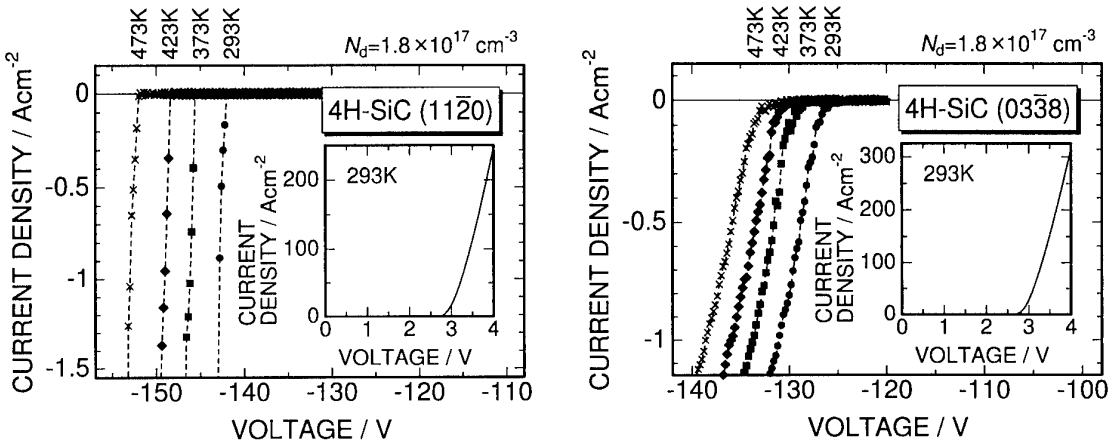


Figure 1: Typical reverse I-V characteristics of diodes fabricated on 4H-SiC (11$\bar{2}$0) and (03$\bar{3}$8) measured at room and elevated temperatures. Insets show forward I-V characteristics of the diodes measured at room temperature.

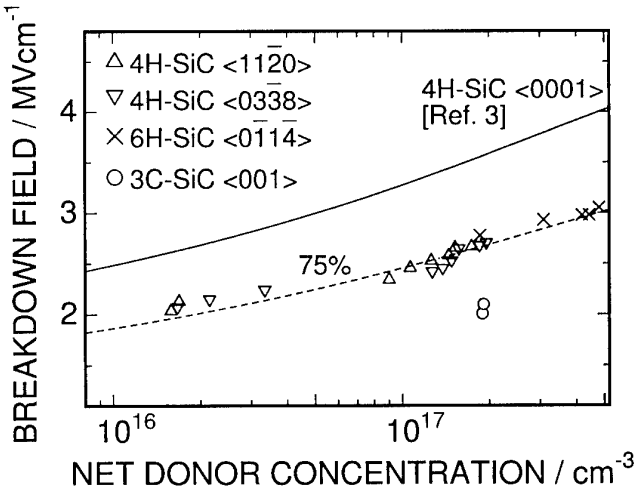


Figure 2: Breakdown field along various crystal orientations in three SiC polytypes at room temperature. The curve marked as 75 % denotes 75 % of the breakdown voltage along the ⟨0001⟩ direction in 4H-SiC suggested in Ref. 3.

A comparative study of the electrical properties of 4H-SiC epilayers with continuous and dissociated micropipes

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Micropipe is the most serious defect in SiC crystal which is included in 10^1 to 10^2 /cm^2 in commercial wafers, and it is well known that a micropipe in a substrate propagates into the epilayer by epitaxial growth. Its harmful features resulting from the early breakdown of pn diode and Schottky diode were reported. [1,2] Therefore, aiming at developing large capacity devices with high yield, It is necessary to decrease micropipe density.

Recently, we confirmed that some micropipes dissociated into several closed core screw dislocations through CVD growth. [3] In that study, KOH selective defect etching was applied for crystallographical evaluation. Continuous micropipe indicated large hexagonal etch pit with dark contrast, whereas dissociated micropipe showed several small assembled or aligned etch pits that were round in shape, which attributed to closed core screw dislocations dissociated from a micropipe. The probability of micropipe dissociation reached as high as 78% in the best result for an area of over 80mm^2.

With regard to vertical device application, a continuous hollow tube across the depression layer was closed by epigrowth; i.e. the SiC filled the entire depression layer instead of tubal air portion. Accordingly, an improvement of the electrical properties of the diode was expected as a result of the micropipe dissociation, even though several non-hollow core dislocations were generated. For this purpose, the electrical properties of the diodes fabricated on the epilayer have been investigate in this study.

Ni- Schottky barrier diodes in 0.5μm diameter with no edge termination were fabricated on 4H-SiC epilayer. The 21μm-thick epilayer was obtained using the radiant heating reactor with a growth rate as high as about 14μm/h. [4] Doping type and concentrations were determined as n-type ~5×10^{15}cm^{-3} by C-V characteristics. Nomarsky optical microscope observation and KOH etching were used for morphological and crystallographical study.

Continuous and dissociated micropipes accompanied by a linear depression along a [11$\bar{2}$0] step-flow direction were visible on the epilayer surface. Therefore, the presence or absence of micropipes within the device area was recognized by the Nomarsky optical microscope. Micropipe dissociation and penetration was also checked using the KOH technique and transmission optical microscope observation after removing Ni contact.

I-V characteristics were investigated with reverse voltage up to -1000V. Fig. 1 and Fig. 2 show the I-V characteristics of the diodes including dissociated and continuous micropipe, respectively. Comparing electrical properties between dissociated and continuous micropipe, significant improvement of blocking performance was recognized for micropipe dissociation. The diode including dissociated micropipe blocked -1000V, whereas the diode involving continuous micropipe failed at or below -400V.

Morphological observation of the diode reached to the breakdown revealed that the breakdown current was passed through the micropipe, because the Ni contact was melted at the point on the micropipe.

The leakage current at -1000V of the diodes including dissociated micropipes ranged from 10^{-6} to 10^{-2} A/cm^2, whereas, the best-performing diode with no micropipe suppressed its leakage current as low as 10^{-6} A/cm^2. Wide differences in the leakage current were presented between the diodes with dissociated micropipes, which might have depended on the amount of non-hollow core dislocations, however further study on this is needed.

The maximum electrical field at the device surface fabricated on a net carrier concentration of ~5x10^{15} cm^{-3} and a 21μm-thick epilayer was calculated at reverse voltage -200V, -400V and -1000V as 0.6, 0.85 and 1.33 MV/cm. Thus, the layer on dissociated micropipes sustained up to 1.33 MV/cm, whereas the epilayer of continuous micropipes failed below 0.85MV/cm. This attributed to the material-changing effect in the depression area from air in the tubal defect to the SiC in the closed core dislocations.

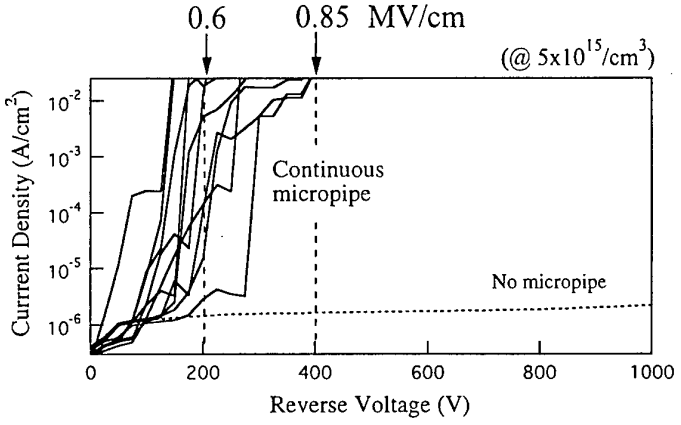


Fig. 1 I-V characteristics of diodes including continuous micropipe

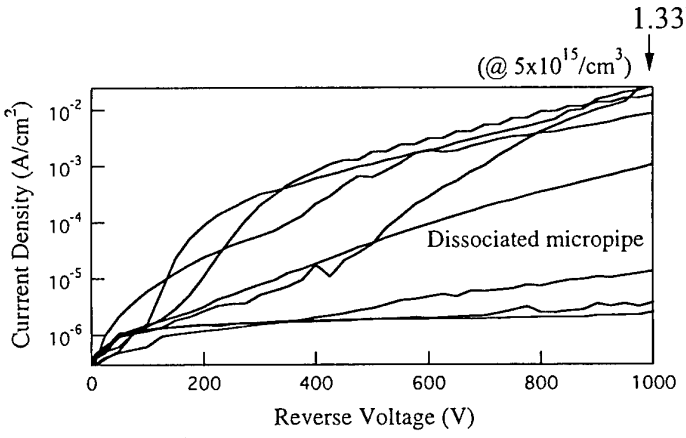


Fig. 2 I-V characteristics of diodes including dissociated micropipe

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Analysis of High Leakage Currents in 4H-SiC Schottky Barrier Diodes using Optical Beam Induced Current Measurements

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SiC Schottky barrier diodes (SiC-SBDs) have been expected to replace Si pin diodes by utilizing their properties with very low reverse recovery currents and high blocking voltages identical to Si pin diodes. However, there are several unsolved problems to show the great advantages against Si pin diodes. One of the challenges is to fabricate reproducible SBDs with low leakage currents especially in SBDs with large areas.

We have reported that these highly leaked SBDs include bright spots of optical beam induced current (OBIC) at the Schottky interfaces [1]. In this paper, we observed the cross sections under the bright spots of OBIC using cross sectional transmission electron microscopy (TEM) to clarify the origin of the bright spots. The dark regions due to the strain of the 4H-SiC crystal could be seen only under the bright spot of OBIC. These strains might be the cause of the high density of the deep levels, which could be the bright spots.

N-type 4H-SiC wafers, in which the c axis tilts 8 degrees to (11-20) direction, were purchased from Cree Research Inc. Epitaxial layers with the doping concentration of $10^{15}cm^{-3}$ were grown on (0001) Si face by hot wall LPCVD system [2]. After the implantation of guard rings, backside Ohmic contacts were formed with patterned windows, which correspond to the areas of Schottky contact. Schottky contacts were formed by sputtering of nickel and following annealing.

After the measurements of current-voltage characteristics of SBDs, OBIC measurements on the Schottky contacts were carried out from the polished backside of the wafer. The system is equipped with a He-Ne laser with a wavelength of 632.8nm (1.96eV). Since the energy is lower than the band gap of 4H-SiC, the laser can only excite carriers captured by the deep levels in the band gap. After putting marks by focused ion beam (FIB) close to the bright spots of OBIC, the sidewalls of the wafer were etched by FIB to observe the crystallinity under the Schottky interfaces using cross sectional TEM.

OBIC images at the Schottky interfaces are shown in figure 1 in thecase of high and low leakage currents. Bright spots could be observed at the Schottky contact with high leakage current as shown in figure 1(a). To the contrary, no bright spots appeared on the Schottky interface with low leakage current as shown in figure 1(b). A cross sectional TEM image, which includes the bright spot of OBIC pointed in figure 1(a), is shown in figure 2(a) with a normal region of TEM image for reference in figure 2(b). The dark

regions with the size of 0.2 - 0.3μm, which are due to the crystal strains, could be observed under the Schottky interface. It can also be recognized that the thickness of the nickel film is not uniform over the distance of morethan 10μm around the bright spot of OBIC. These results might be the origin of the bright spots of OBIC. Further investigation will be presented on the view of step bunching and the fabrication process.

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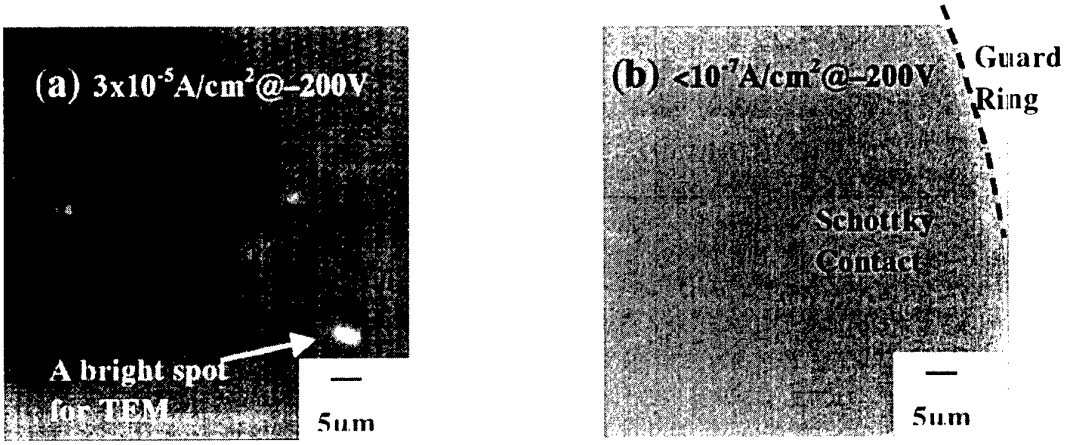


Figure 1 OBIC images at the Schottky interface in the case of high leakage current (a) and low leakage current (b)

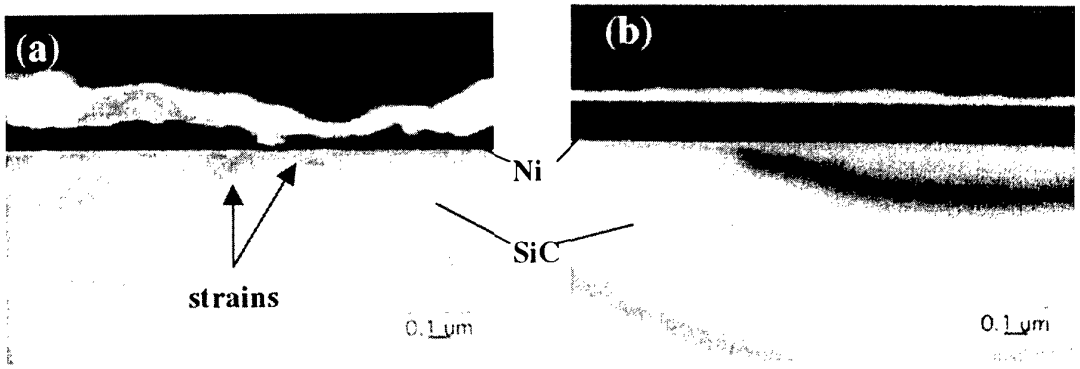


Figure 2 Cross Sectional TEM images under the bright spot of OBIC (a) and under the area without bright spots of OBIC for reference (b)

Electrical activity of residual boron in silicon carbide

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Control of residual boron in silicon carbide is an important issue when growing low doped crystals. However, the electrical properties of this common acceptor and its influence on material properties are little known. This is most probably due to the fact that sensitive electrical measurement techniques such as deep level transient spectroscopy (DLTS) are often limited to majority carrier traps and can not detect residual acceptor impurities in n-type material. DLTS measurements of p-type SiC are difficult to perform due to low temperature freeze-out of deep acceptors. In this work we have used minority carrier transient spectroscopy (MCTS) to avoid above mentioned complications. This technique does not require a *pn* junction in order to inject holes into depletion region, but uses above-bandgap illumination to create electron-hole pairs. A Schottky contact can then be used for the capacitance transient measurements.

We present a study of the boron acceptor in n-type CVD grown 4H silicon carbide. Using MCTS we were able to detect the presence of both shallow and deep boron (so called D-center) in the samples with the activation energies of 0.27 eV and 0.62 eV respectively (Fig.1). Effective capture cross-sections for holes obtained from the Arrhenius plot are $1.4 \cdot 10^{-13}$ and $9 \cdot 10^{-14}$ cm^2, respectively. By filling the traps with holes optically and then applying DLTS filling pulses, no noticeable decrease of the MCTS peaks amplitude was observed. This suggests that electron capture is inefficient, and that both defects act as very efficient hole trapping centers with large capture cross-section. From the capture cross-sections we estimate that even a low concentration in the order of $5 \cdot 10^{12}$ - 10^{13} cm^{-3} would limit the minority carrier lifetime to the level of 40 ns. This has also been confirmed experimentally where we have measured the boron concentration on different parts of a wafer with measured optical decay times ranging from 200 to 500 ns (Fig.1). These measurements were performed at relatively high injection, where some saturation of the trapping

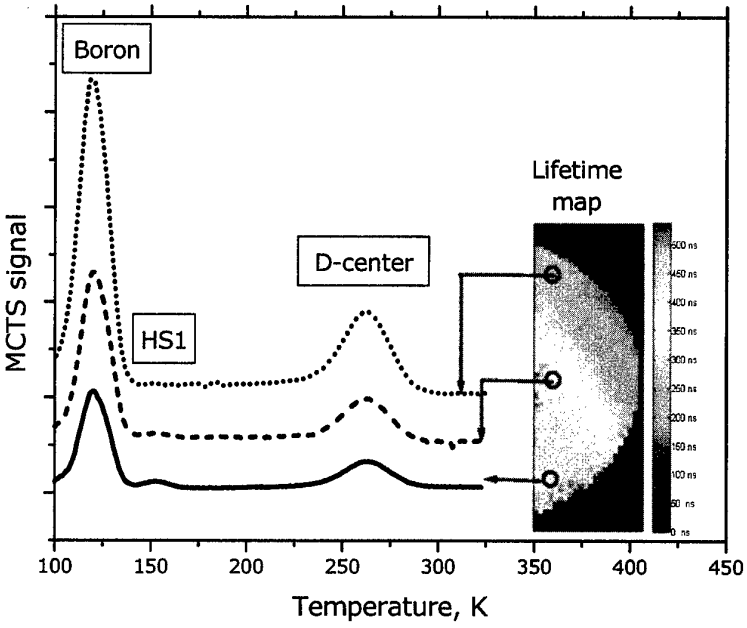


Fig. 1. MCTS spectra on wafer parts with different minority carrier lifetime

defects could be possible. The effect on low injection lifetime should be more pronounced. Optical decay measurements under different excitation conditions will be presented.

We have also performed a scanning-MCTS experiment by focusing the laser beam on different spots of a large Schottky contact. We were able to map the boron peak in different selected directions across the samples and compare with the data from minority carrier lifetime maps (Fig.2). We have found a clear correlation between the intensity of the boron signal and reduction of the minority carrier lifetime. Concentrations of other defects ($Z_{1/2}$, HS1) do not change remarkably in the low and high lifetime regions. Some reduction of the $Z_{1/2}$ peak was observed in the high-boron regions. This strongly indicates that the presence of boron is responsible for the observed lateral variation of minority carrier lifetime in high-quality silicon carbide.

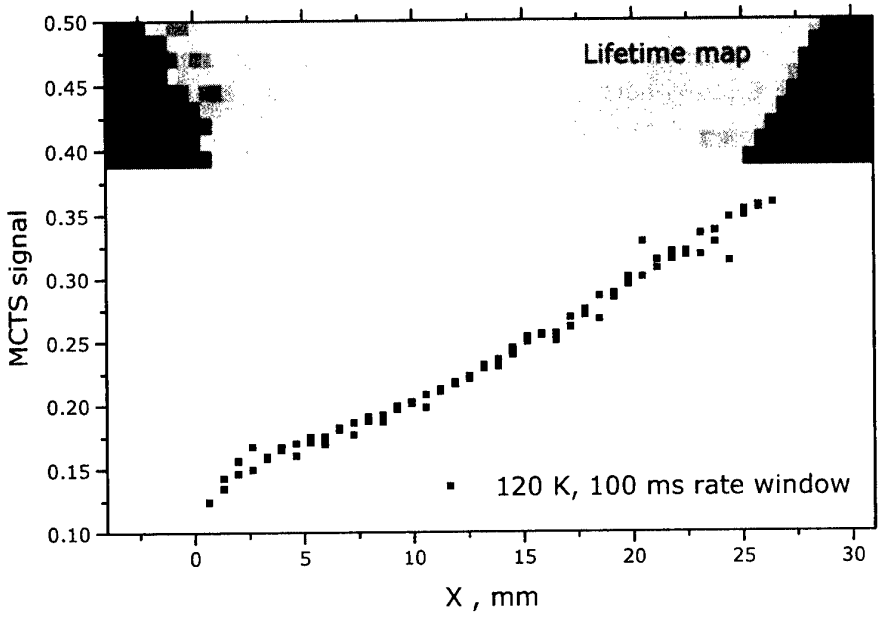


Fig. 2. Scanning MCTS at 120 K shows clear correlation between the intensity of the boron signal and reduction of the minority carrier lifetime

Mapping of the luminescence decay of low-doped n-4H-SiC at room-temperature

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For bipolar SiC power devices the lifetime of the carriers is a very important parameter (for a 5 kV p-n-diode a lifetime of approximately 400 ns should be reached). In order to control the decay time by a non-destructive method we use the time-resolved-photoluminescence (TRPL) at room-temperature to characterize low n-doped 4H-SiC epitaxial layers concerning the decay time and the homogeneity over the entire area.
The main part of the excited carriers recombines radiationless. Therefore the measured small fraction of radiative transitions is used to monitor the whole time behaviour of the recombination process.

For this we move the sample using a steppingmotor driven x-y-table to draw up a mapping of the luminescence decay after excitation with a short laser pulse. The experimental setup is shown in Fig. 1.

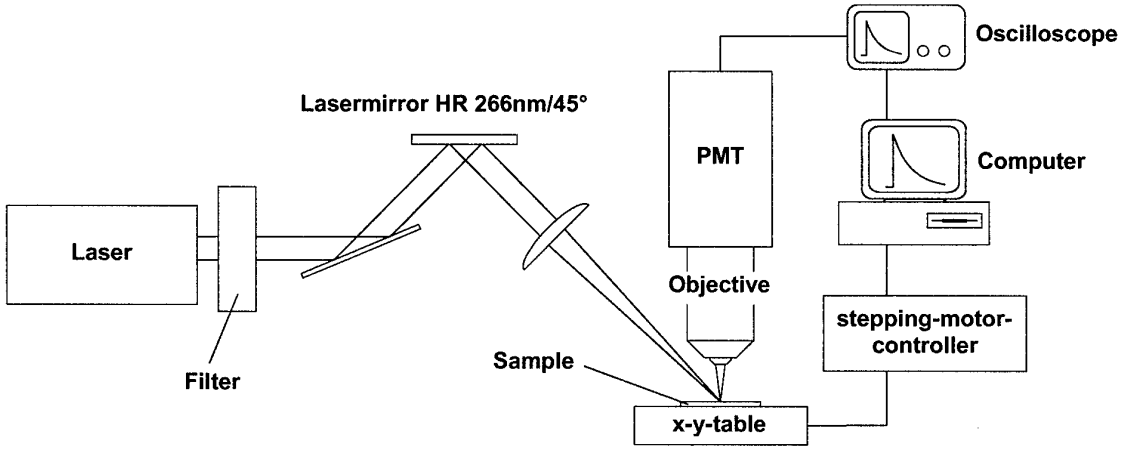


Fig. 1: Experimental setup of the TRPL

The excitation source is a frequency quadrupled pulsed Nd:YAG laser with a maximum repetition rate of 30 Hz, a pulse width of 4 ns (FWHM) and a wavelength of 266 nm. The penetration depth in 4H-SiC at room-temperature for this wavelength is about 0.5 µm [1]. The spot on the sample has a size of 10x15 µm so that also small structures can be measured.
Unlike most investigations using the TRPL-method [2] we use no spectral selection of single wavelengths of the PL-light. All the emitted light is collected by a quartz objective to a photomultiplier and the signal is recorded by a digital oscilloscope averaging over 150 pulses. Fig. 2 shows a typical signal.
Due to the time response of the photomultiplier we are limited to decay-times longer then 20 ns.

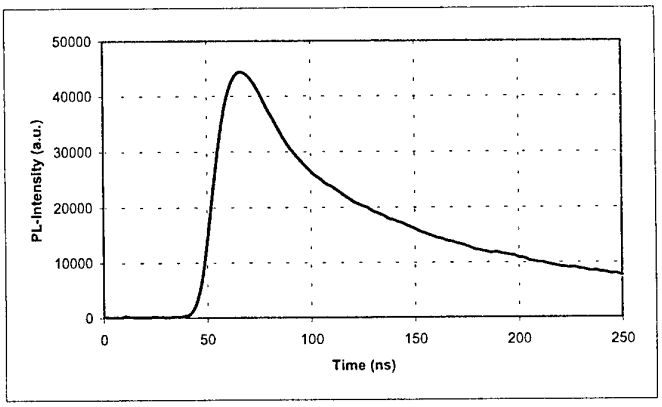


Fig 2: Typical luminescence decay signal (τ = 112 ns)

Epilayer:
thickness 40 µm,
doping 5.09 $10^{14}cm^{-3}$

In this abstract, we demonstrate first results of the time resolved photoluminescence on 4H-SiC. Substrates and low-n-doped epilayers have been measured.
The main features are:
- big differences concerning homogeneity and decay-constants can be observed,
- decay times mostly are in the range of 60 to 150 ns for epilayers and
- decay times up to 535 ns averaged over the measured area could be observed on single samples (Fig. 3).

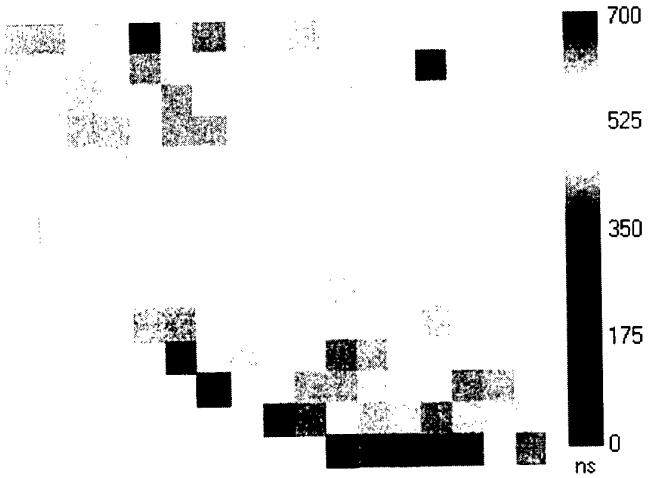


Fig 3: Mapping of the decay times (after 200 ns of the excitation pulse) of a part of a 4H-SiC epilayer from CREE

Epilayer:
thickness 50 µm,
doping 7.5 $10^{14}cm^{-3}$

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P-3C-SIC/N-6H-SIC HETEROJUNCTIONS: STRUCTURAL AND ELECTRICAL CHARACTERIZATION .

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The presence of a large number of crystalline modifications (polytypes), which have identical composition but may markedly differ in electrical properties, makes SiC a promising material for creating various heterostructures. Progress in the sublimation epitaxy in vacuum technology enabled fabrication of n-3C-SiC/n-6H-SiC epitaxial heterostructures with good quality of the 3C-SiC epilayer [1]. Aim of the present study is growth and and investigation heteropolytypes 3C-6H SiC pn structures.

Investigated p-n structures were grown by sublimation heteroepitaxy in vacuum on 6H-SiC (0001) Lely substrates. X-ray diffractometry confirm presents of SiC films of the both polytypes. An ohmic contact was formed on p-type region by deposition of Al and Ti and annealing at 1100°C. Mesa structures with an area $3x10^{-3}$ cm^2, 10^{-4} cm^2 and $8x10^{-5}$ cm^2 were formed by reactive ion-plasma etching using Al mask

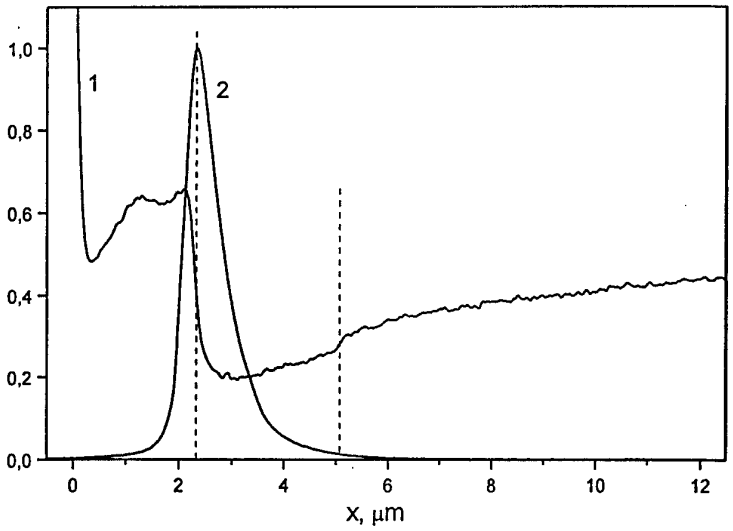


Fig.1. Line profiles of secondary electron (1) and EBIC (2) signals for investigated diodes.

The diode cross sections were studied by the methods of electron beam induced current (EBIC) and secondary electrons (SE) in a JSM-50A scanning electron microscope. In the SE mode, two regions with SE signal jump were observed (Fig. 1). One of these corresponds to the p-3C SiC--n- 6H SiC heterojunction, and the other, to n-6H SiC—n+ 6H-SiC substrate junction. In the given case, the SE signal jump was abrupt and exactly coincided

in position with the peak in the EBIC curve, thereby indicating that the given p--n junction is abrupt. The investigations demonstrated that the p-regions of diodes is homogeneous.

C-V characteristics of the diode was linear in coordinate C^{-2}–U, which mean that obtained pn junction was abrupt. The concentration Nd-Na was 1-2x10^{17} cm^{-3} in n-type layers, and Na-Nd ~ 3 10^{18} cm^{-3} on the surface of the p-type region. Capacitance cut of voltage (U_c^c) was 2,65 ± 0,05 V for this diodes . It was shown, that at low current densities the dependence of the current on voltage is exponential: $J = J_0 \exp(qV/nkT)$. The ideality factor is about 2.1--2.4.

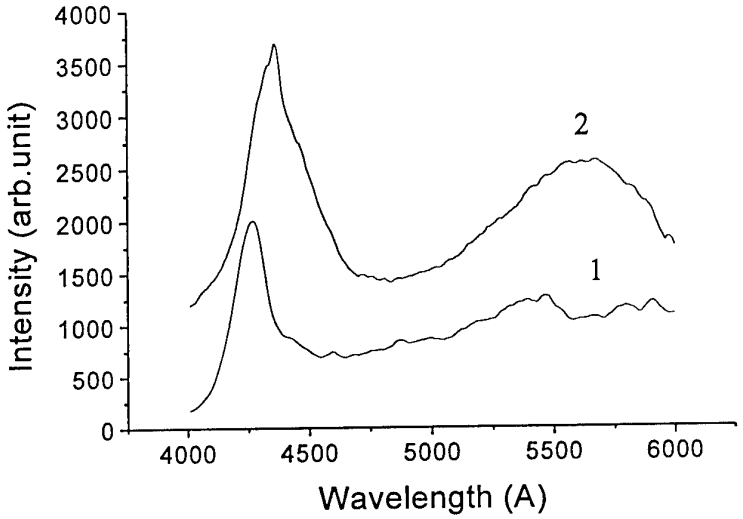


Fig.2 Electroluminescence spectra at forward current 70 mA, T = 300 K (1); 600 K (2) (curve 2 is shifted up on 1000 units)

Electroluminescence bands with $h\nu_{max} \approx 2.9$ eV and $h\nu_{max} \approx 2.3$ eV are observed simultaneously in the diodes in temperature range 300-600 K (fig.2). These EL bands in 3C-SiC and 6H-SiC are usually considered to be due to the free exciton annihilation.

The determined, from U_c^c value and Fermi level position, band discontinuities ΔEc = 0.55 ± 0,05eV and ΔEv = 0…0.05 eV are in good agreement with theoretical calculations [2] and experimental electron affinity values for 6H and 3C SiC [3]. The low ΔEv value does not hinder hole injection from p+ 3C SiC into n-6H SiC. At the same time, injection of electrons from the wide bandgap material into that with narrow band gap is also possible. Thus, the EL spectrum of such a structure may contain emissions bands associated with recombination in both 6H and 3C SiC, which is the case in the experiment.

The estimated band structure confirm the possibility in principle of creating a field-effect transistor with 2D electron gas (HEMT), based on the 3C--6H SiC heterojunction.

This work was partly supported by RFBR grant N 00-02-16688 and 01-02-17657

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A 600V SiC Trench JFET

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Abstract: 4H silicon carbide trench vertical JFET has been fabricated with a blocking voltage of 600V and specific on-resistance of 5mΩ-cm^2. 2A FETs with an average on-voltage of 1Vand 40% yield have been demonstrated. To our knowledge this is the lowest specific on-resistance for a 600V FET reported. Devices with similar voltage ratings reported in the past showed much higher specific on-resistance. For instance, 40mΩ-cm^2 for 700V, expected based on simulations for ACCUFET, by Motorola [1], 18mΩ-cm^2 for 600V VJFET, by Siemens [2], 18 mΩ-cm^2 for the best device, breakdown voltage 350-450V, by North Carolina State University. From a website [4] of the SiC research group at purdue, (updated Jan 20 2001), the lowest on-resistance reported by any group, is over 10mΩ-cm^2.

The structure of the device is shown in fig. 1.This trench JFET has 4μm deep trenches, with trench bottom implanted with p-type dopants and trenches filled with polysilicon to form the gate. The P$^+$ at the trench bottom serves to protect the trench corners from high electric fields, it is connected to the gate to make the device a JFET. Starting from an n/N$^+$ epi, with the epitaxial layer doped 1e16cm^{-3}, 10um thick, trenches using Ni mask, in an SF_6 chemistry based RIE process developed at the Rockwell Science Center. The oxide isolating the gate from the trench sidewalls is deposited by LTO and subsequently re-oxidized at 1150C. LPCVD deposition of polysilicon is then performed to fill the trenches. The polysilicon is then RIE etched to remove excess polysilicon on the source mesas. Fig. 2 Shows an SEM picture of the device after the polysilicon etching. Following the polysilicon planarization, contacts are defined and metal deposited. To simplify the process, the contacts were not sintered. In the following lots we plan to alloy the contacts to reduce the contact resistance.

Fig. 3 shows the family of drain current vs. drain voltage characteristic of the FET for various gate voltages. This is a normally on FET, and requires negative voltage to turn-off. It is possible to use this device under 'normally –off' conditions by use of a low voltage silicon MOSFET in series, in a cascode configuration, as described in [2]. Fig. 4 shows the blocking characteristics of the FET. It can be seen that the device blocking voltage is over 600V. However in order for the device to block 600V, -30V on the gate is needed. A plot of the blocking voltages vs. device position on the wafer is shown in Fig. 5 for the –20V gate bias. With –20V on the gate the working devices could block between 400-500V. Shown in Fig. 6 is the on-voltage vs. device position for the FET, at a drain current of 1A. It can be seen that over 90% of the devices have on-voltages between 0.4 and 0.6 v.

We will report the results of the FET with improved contacts in the paper. Further we will also describe the device design and process issues for this device. High temperature will also be presented in the paper.

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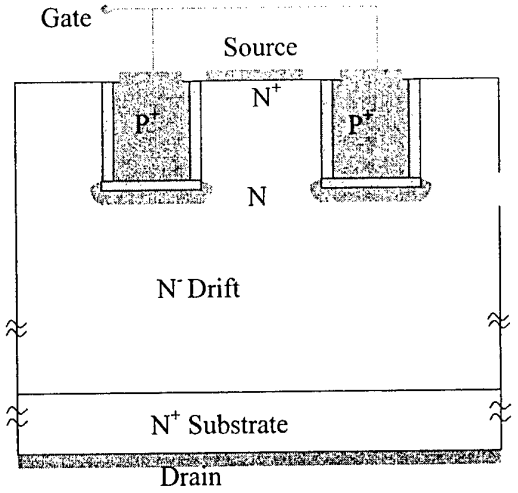


Fig.1 Cross-section of the device



Fig.2 SEM Picture of the device after polysilicon planarization

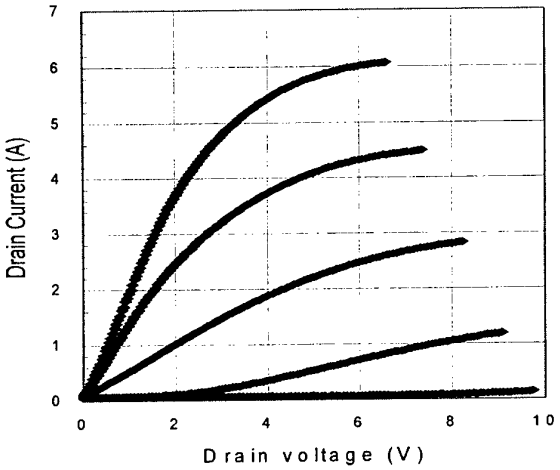


Fig. 3 Family of curves, Drain current vs. Drain voltage, Vg=0, -2, -4, -6, -8

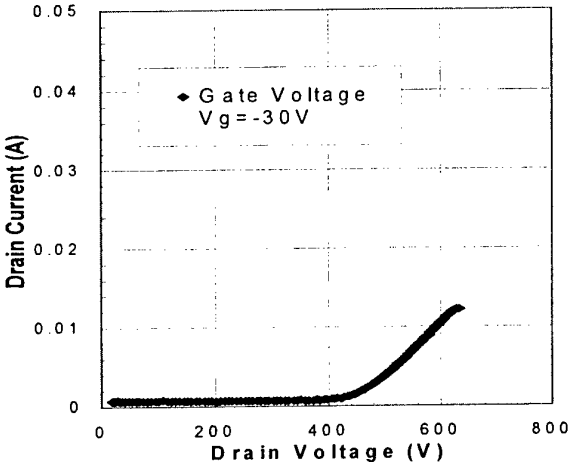


Fig. 4 Blocking characteristics of the FET. Vgs=-30V.

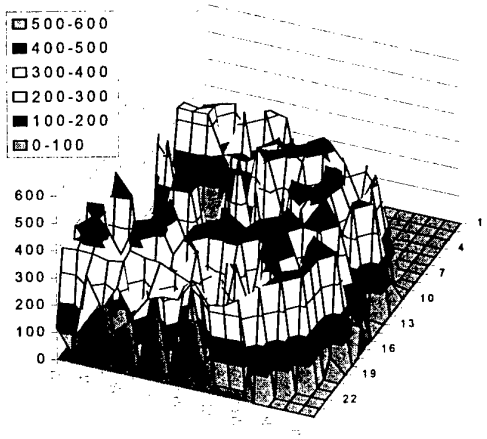


Fig. 5 Map of blocking voltage vs. device position for Vgs=-20V.

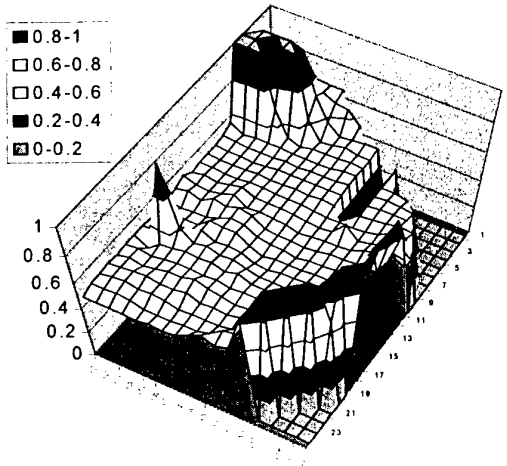


Fig. 6 Map of on-voltage vs. device position for Vgs=0V, at a current of 1A.

2 kV 4H-SiC Junction FETs

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The silicon carbide (SiC) SIT (static induction transistor) or Junction FET (JFET) will is expected to be appropriate for SiC devices because of no oxide-semiconductor interface in the channel [1]. A JFET with a novel gate structure, which can realize both low on-resistance and high blocking voltage, is proposed and demonstrated [2,3]. However, careful consideration of gate structures must be needed for reduce on-resistance. In this paper, vertical channel type 2 kV JFETs can successfully demonstrated and the effect of gate structure is also discussed.

Figure 1 shows schematic structures of fabricated JFETs. The doping level of n^- epitaxial layer is $2.5x10^{15}cm^{-3}$ and the thickness is 20 μm. In order to fabricate deep p gate and narrow channel, high energy multiple Al^+ implantation (730 keV and 870 keV) is used. Total dose of the p gate and the channel width are parameters for consideration. The n^+ source and p^+ gate contact are formed by N^+ and Al^+ implantation, respectively. After implantation, annealing at 1650 °C in argon is followed. Ni for the source electrode and Ti/Al for the gate electrode are evaporated and sintered. Figure 2 shows a top view of the fabricated source and gate electrodes. Figure 3 shows an example of measured drain I-V characteristics. Figure 4 shows a blocking property of a fabricated JFET, which indicates higher blocking capability than 2 kV. Figure 5 shows dependence of drain I-V curves on the channel width and the p gate dose measured at zero gate voltage. It can be found that on-resistance of high dose case ($2.9x10^{14}$ cm^{-2}) is higher than that of low dose case ($1.5x10^{13}$ cm^{-2}) shown in figure 6 as expected. Since the channel width dependence is not so strong, the low dose case is appropriate for fabrication. However, difference of on-resistance at 2 μm channel width is larger than expected value which is estimated by the simple model of depletion layer expansion. Two-dimensional effect is thought to be a reason of such large difference.

As a conclusion, vertical channel type JFETs are fabricated and higher blocking capability than 2 kV are demonstrated. The effect of gate structure is studied and it is found that low dose of the p gate is appropriate for the performance and fabrication process.

This work was performed under the management of FED as a part of the METI Program (R&D of Ultra-Low Loss Power Device Technologies) supported by NEDO.

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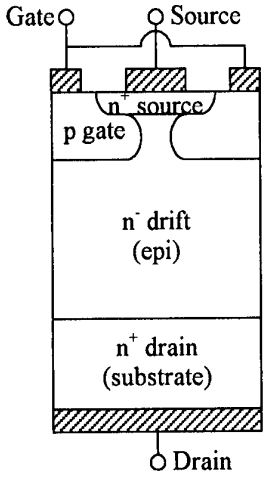


Fig.1 Schematic structure of a JFET

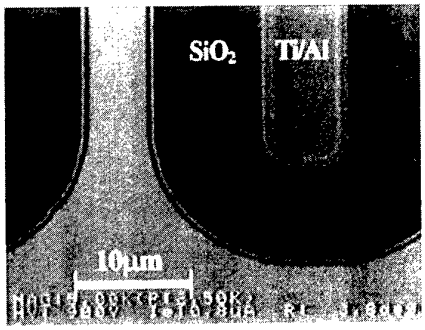


Fig.2 Top view a fabricated JFET.

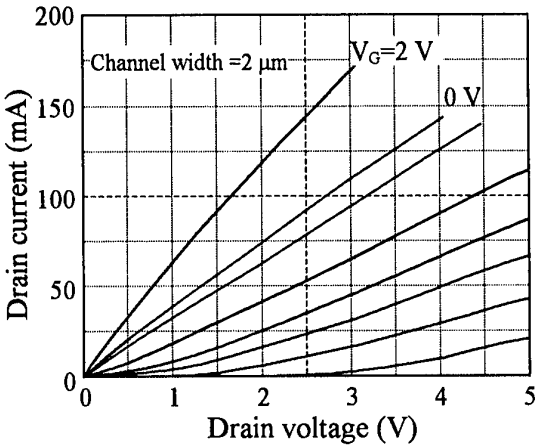


Fig.3 Gate voltage dependence of drain I-V characteristics

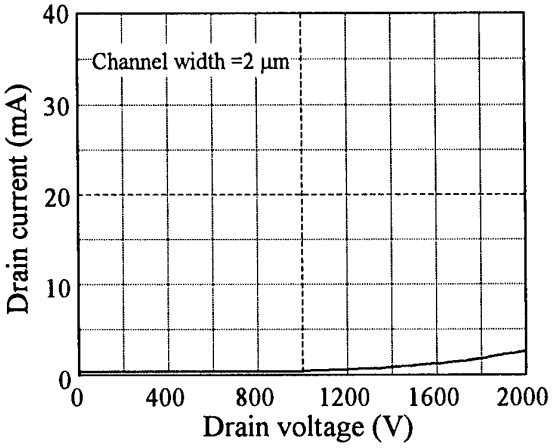


Fig.4 Broking characteristics

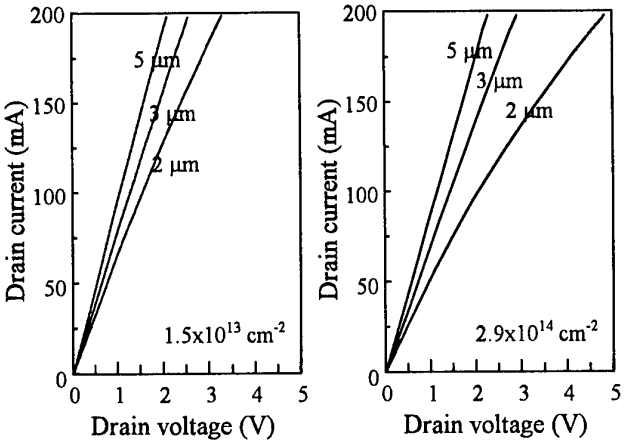


Fig.5 Dependence of drain I-V characteristics on channel width and p gate dose

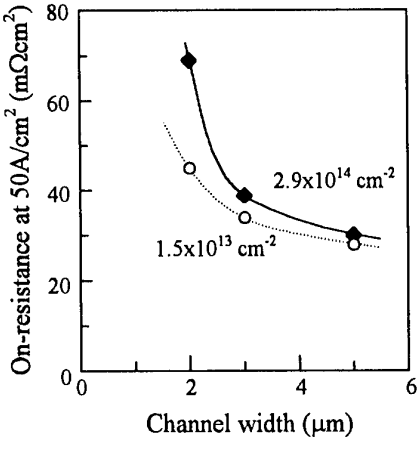


Fig.6 On-resistance versus channel width

A Novel High-Voltage Normally-Off 4H-SiC Vertical JFET

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The commercial availability of 3-inch wafers of 4H-SiC and the continuing effort in scaling up SiC substrates by a number of companies are creating the basis for an emerging SiC power electronic industry. Many 4H-SiC high voltage and high-speed devices have been demonstrated with the majority of them focusing on replicating the corresponding Si power devices in the hope of achieving higher power levels. It was pointed out in 1995 [1] that the reliability of gate oxide (SiO_2) in SiC power switches under both high temperature and high electric field is an intrinsic problem and gate-oxide free devices should be pursued. While many encouraging results have been reported over the years concerning the low inversion layer carrier mobility and different gate insulator reliability in 4H-SiC power switches a final solution suitable for practical applications may require a lot more research and investments. It is, therefore, desirable to develop SiC power switches free of gate oxide/insulator to take the full advantages of SiC material properties for high temperature power electronic applications. This work is focused on the development of a novel 4H-SiC unipolar power switch free of gate oxide/insulator.

Fig.1 shows the cross sectional view of a novel high voltage normally off vertical JFET (patent pending) in 4H-SiC based on MeV ion implantation technology. A buried P layer formed with MeV Al or Al plus C co-implantation is used to create the blocking junction and the horizontal channel. The semi-insulating layer formed by deep Vanadium implantation is used to terminate the horizontal channel so as to prevent the current conduction through the parasitic vertical PNP structure. The DC and transient characteristics of this switch are studied by way of two-dimensional numerical simulations with ISE-TCAD software. Fig.2 shows J-V curves of the device. It can be seen that the switch has a blocking voltage of 1644V at 300K and over 1,800V at 600K. The switch is normally-off and can be turned on to handle a high current density with gate voltages up to 2.75V and 2.06V at 300K and 600K, respectively, with a negligible gate current. The key design parameters for this device are vertical channel opening d and horizontal channel opening h. The optimized value for d is around 2.5μm as illustrated in Fig.3. It can be seen from Fig.4 that h=0.17μm can be used which

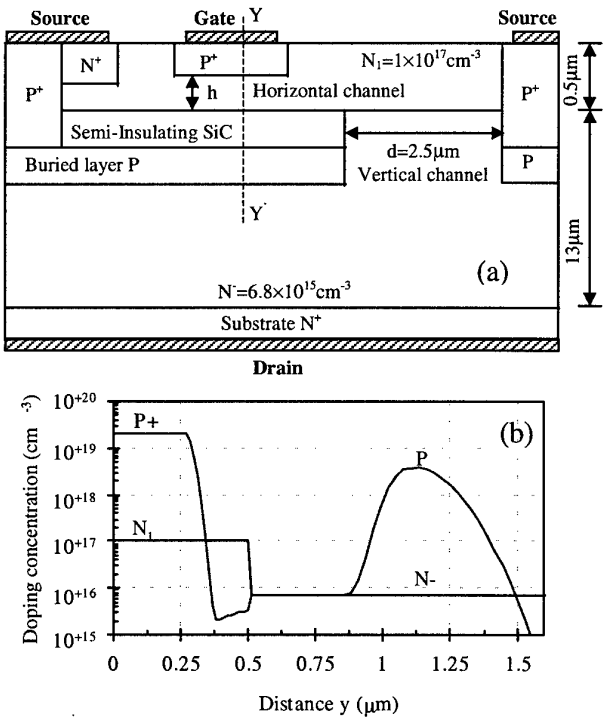


Fig.1 Normally-Off VJFET. (a) Cross sectional view. (b) Doping concentrations along the straight line YY'.

corresponds to a high J_F of 600A/cm^2 at a V_{Drain} of 3V. This unipolar switch has a very high switching speed. The results of transient simulations are presented in Fig.5 where the turn-on time of 211.5ns and the turn-off time of 144.7ns are basically limited by the applied dV_G/dt gating rate of 1.1×10^7V/s. With a drift layer doped mid-10^{15}cm^{-3}, a fully implanted planar 4H-SiC VJFET capable of blocking 1,790V has been demonstrated and the results will be presented.

Reference: [1]. J. H. Zhao, et al., "SiC UMOS and thyristor-based power switches", Proc. of 1st Workshop on HTPE for Vehicles, pp.36-43, 1995, Eaton Town, NJ.

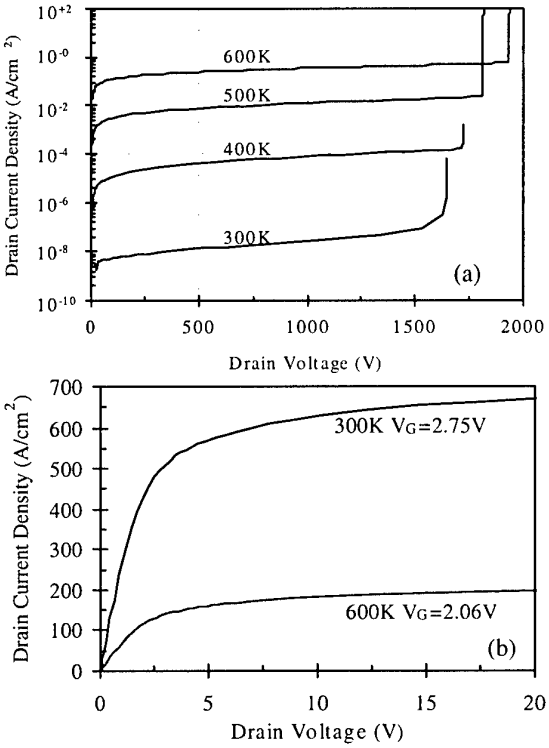


Fig.2 J_D-V_D curves at (a) off-state and (b) on-state.

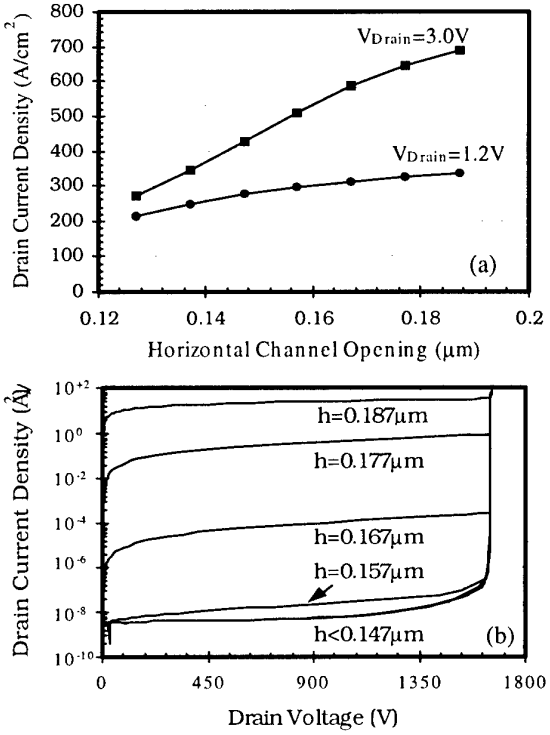


Fig.4. J_D-V_D curves with different horizontal channel opening h at 300K at (a) on-state and (b) off-state.

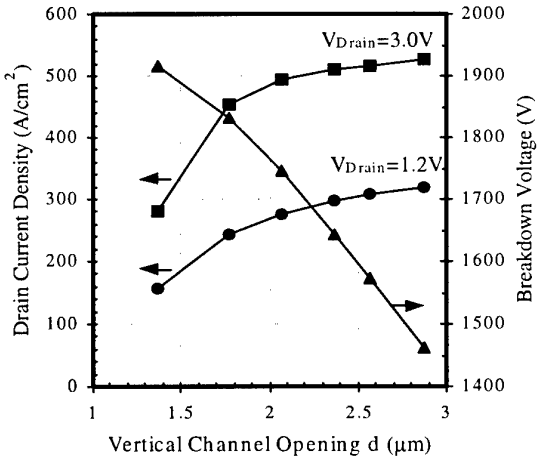


Fig.3 The effect of the vertical channel opening d at 300K.

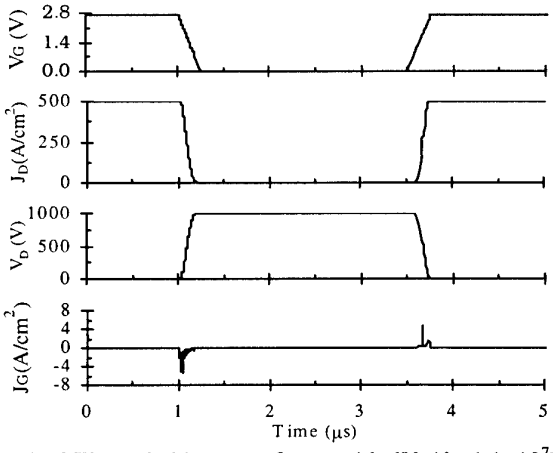


Fig.5 The switching waveforms with $dV_G/dt=1.1\times10^7$V/s at 300K.

Large Area (3.3mm x 3.3mm) Power MOSFETs in 4H-SiC

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This paper describes the design and fabrication of 4H-SiC Power MOSFETs. We have achieved 350 V, 10 A (V_F = 4.4 V) devices with an active area of 0.105 cm^2 (3.3 mm x 3.3 mm) which represents a specific on-resistance ($R_{on,sp}$) of 44 mΩ•cm^2. This has been made possible by using a buried channel device, resulting in a peak channel electron mobility of 195 $cm^2/V•s$. The previous results have been limited to less than 0.5 A in small area devices [1,2].

Figure 1 shows a schematic cross-section of the basic cell. A 25 μm thick, $2x10^{15}$ cm^{-3} doped n- type drift layer was grown on n+ 4H-SiC substrate. The cell pitch is 25 μm. The p-wells, JTE regions and the p^+ contacts are formed by aluminum implantation. The n^+ source regions are implanted with nitrogen. A buried n-type layer is created in the channel region with a charge of approximately $1.7x10^{12}$ cm^{-2}. All the implants are activated at 1600°C in Ar. The gate oxide is thermally grown in dry O_2 at 1200°C for 1 hr, followed by an anneal in at 1200°C Ar for 1 hr, followed by a re-oxidation anneal in wet O_2 at 950°C for 3 hrs. The gate metal consists of 0.5 μm thick sputtered Moly. The contacts to source, drain and p^+ regions are formed with 0.1 μm thick sintered Ni. Then, an inter-metal dielectric is deposited and via holes are opened. The final metal is a 2 μm thick Ti/Pt/Au layer.

The effective channel mobility measured on a 100 μm / 100 μm FATFET is shown in Figure 2. With zero bias to the p-well, the device is normally-on with a threshold voltage (V_{TH}) of -2 V and a very high peak effective channel mobility of 195 $cm^2/V•s$. This indicates the presence of a neutral n-type buried layer. At higher gate bias, the effect of the neutral n-type layer diminishes and all the curves come together to the surface electron mobility (~ 25 $cm^2/V•s$ at V_{GS} = 20 V). The V_{TH} shifts positive as the charge in the n-type buried layer is reduced by applying negative biases on the p-well. This clearly shows that the devices can be made to be normally-off by reducing the n-type charge in the buried channel.

The on-state I-V characteristics of a 3.3x3.3 mm^2 4H-SiC Power MOSFET are shown in Figure 3. An I_D of 10 A was measured at a 4.4 V forward drop. This device is normally-on with a V_{TH} of -2 V, due to the relatively high dose of n-type charge in the p-well. A $R_{on,sp}$ value of 44 mΩ•cm^2 is obtained for the large 3.3x3.3 mm^2 device at a relatively low gate bias of 2.5 V. The breakdown voltage for the large device is only 350 V and a high leakage current is observed (Figure 4). Figures 5 and 6 show on-state and off-state I-V characteristics of a smaller 0.75x0.75 mm^2 device with a cell pitch of 16 μm. The device showed a reduced $R_{on,sp}$ value of 23 mΩ•cm^2 due to the smaller cell pitch, which resulted in smaller JFET resistance, and was able to block 1620V (V_g = -19V).

Recently, NO annealing of the gate oxide was shown to be very effective in improving effective channel mobility in 4H-SiC MOSFETs [3]. Figure 7 shows IV characteristics of a NO annealed (performed at Auburn Univ.) 4H-SiC power MOSFET (0.75x0.75 mm^2) without any buried channel charge. The device showed a $R_{on,sp}$ of 55 mΩ•cm^2 and a breakdown voltage of 1950 V (Figure 8). These devices are normally-off. The shape of the breakdown characteristics suggests open base bipolar breakdown, due to the high resistance of the p-well regions.

Acknowledgements: This work was supported by DARPA (Dr. D. Radack) and monitored by Dr. G. Campisi of ONR under the contract # N00014-99-C-0377.

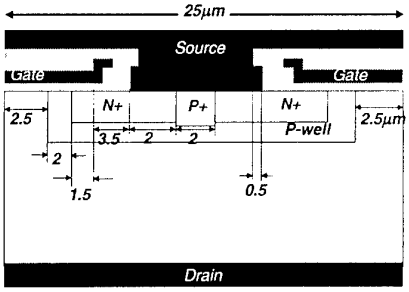


Figure 1. A schematic cross-section of the power MOSFET cell.

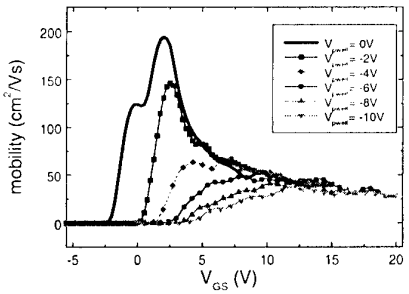


Figure 2. Effective channel mobility in a FATFET as a function of the gate bias and the back bias on the p-well.

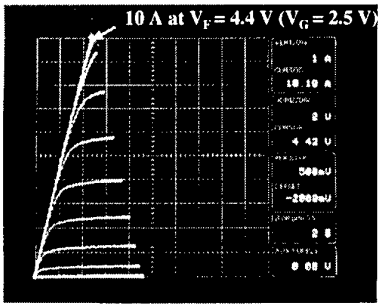


Figure 3. Forward I-V characteristics of a 3.3x3.3 mm^2 power MOSFET.

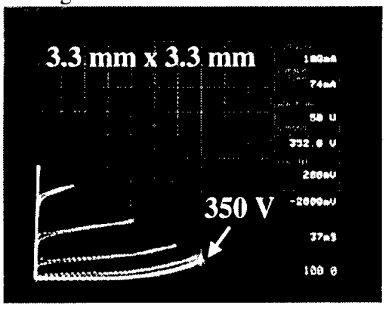


Figure 4. Blocking characteristics of the 3.3x3.3 mm^2 power MOSFET.

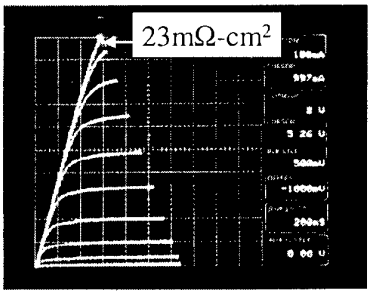


Figure 5. Forward I-V characteristics of a 0.75x0.75 mm^2 power MOSFET.

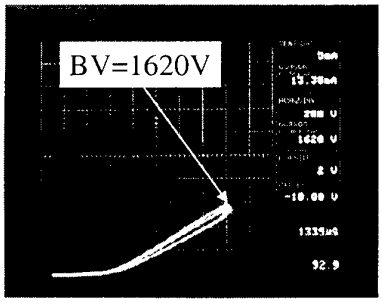


Figure 6. Blocking characteristics of the 0.75x0.75 mm^2 power MOSFET.

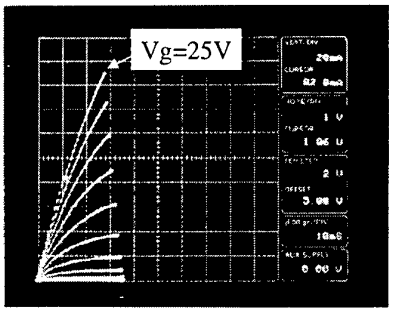


Figure 7. Forward I-V characteristics of NO annealed (courtesy of Prof. J. R. Williams) 4H-SiC power MOSFET (0.75x0.75mm^2).

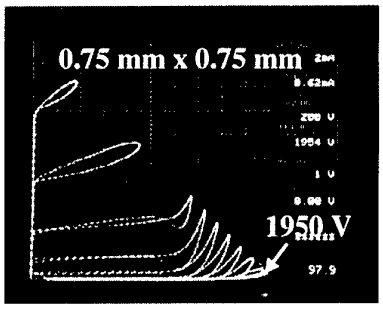


Figure 8. Blocking characteristics of the device shown in Figure 7. The device did not receive any buried channel charge.

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[3] M. K. Das et al., *58th IEEE Device Research Conference*, Denver, CO. June 19-21, 2000.

4H-SiC DELTA-DOPED ACCUMULATION-CHANNEL MOS FET

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We report on electronic properties of nitrogen-delta-doped SiC and propose its application for MOS-FET. Delta-doping distributions with high peak concentrations and narrow distribution widths were advantageous for a high Hall mobility. 4H-SiC delta-doped accumulation-channel MOS field effect transistors (DACFET) have been successfully fabricated. Delta-doping in CVD was performed by a pulse doping method using a pulse valve.[1] The valve can open and close within very short period less than 10 μs. The nitrogen gas as n-type dopant was injected into the reactor through the pulse valve. The delta-doped structure was confirmed by the C-V profiling technique. The doping distribution profile of the delta-doped SiC had strikingly narrow full width of half maximum (FWHM) of 10 nm, as shown in Fig.1. The peak concentration was as high as 10^{18} cm^{-3}. By Hall-effect of the delta-doped SiC, the temperature dependence of a Hall mobility and a carrier concentration was investigated. The Hall mobility enhancement was observed for the delta-doped structure over the corresponding uniformly doped SiC. The enhancement factor of 3 was obtained for the delta-doped SiC. The self-consistent calculation by the coupled sets of Poisson and Schrödinger equation suggests that the high mobility is related to the extension of the electron wave-function of the delta-doped layer to high purity SiC layers. The high mobility attracts considerable interest in MOS-FET having the delta-doped accumulation channel. Delta-doped accumulation-channel MOS-FET was fabricated. All epitaxial growth was carried out in the CVD on 4H-SiC (0001) off substrates. The device structure consisted of a 5 μm p-type SiC layer (9×10^{15} cm^{-3}), and an accumulation-channel layer consisting of a 10 nm delta-doped n^+-SiC layer and a 50 nm undoped SiC layer, as shown in Fig.2. The number of the delta-doped layers was five. N^+-source and drain regions were formed utilizing a multiple nitrogen implant profile at 30, 60, 100, 110, 130, 180, and 240 keV with doses of 5, 6, 8, 5, 10, 15, and 10 $\times10^{13}$ cm^{-2}, respectively. The implantation was carried out at 500 ℃. Implants were activated at 1500 ℃ for 30 min in an argon ambient. After standard RCA cleaning, the gate oxides (40 nm) was thermally grown using wet oxidation at 1100 ℃. The device was normally off and had a threshold voltage of 4.2 V although these gate-control properties depended on the delta-doped channel structure. The effective channel mobility derived from the I-V characteristics that was measured at low drain voltage of 0.5 V was higher than about 55 cm^2/Vs. The channel mobility increases with decreasing the gate voltage because of the reduction of the surface scattering. The excellent channel mobility of 113 cm^2/Vs was obtained at the gate voltage of 5 V, as shown in Fig.3. The device also had high drain current of up to 220 mA/mm at the drain voltage of 15 V.

Reference

[1] T. Yokogawa et al. J. Appl. Phys. 89, 1794 (2001).

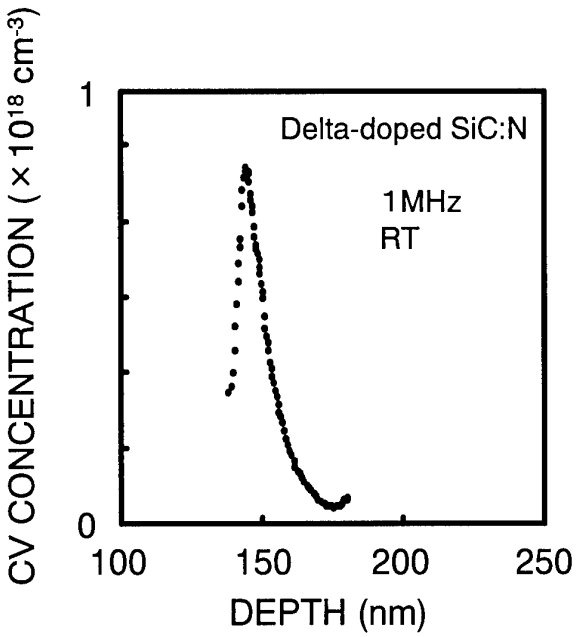


Fig.1. Room temperature capacitance-voltage profile for a delta-doped structure with nitrogen.

Nitrogen-delta-doped accumulation-channel
(5 periods : 10 nm delta-doped n⁺-SiC/ 50 nm undoped SiC)

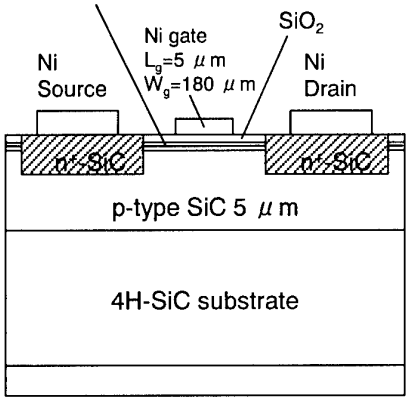


Fig.2. Schematic cross section of the delta-doped accumulation-channel MOS-FET.

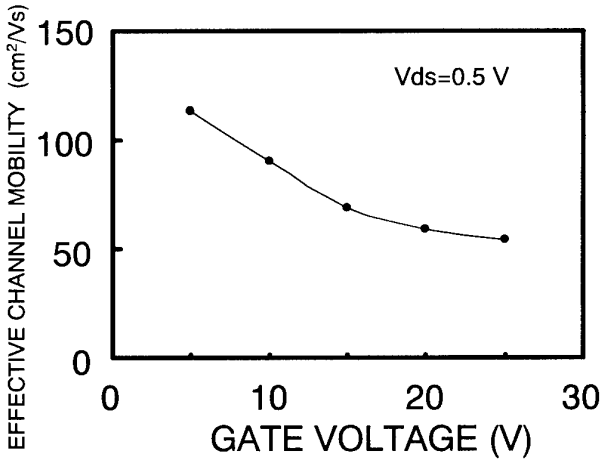


Fig.3. Effective channel mobility vs gate voltage.

5.0kV 4H-SiC SEMOSFET with low RonS of 88 m Ω cm^2

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SiC is expected to enable the realization of power semiconductor devices with better performance than Si devices, because of its superior electrical and physical properties. However, since the built-in junction potential of SiC is higher than that of Si due to its larger band gap, unipolar devices such as FETs and SITs are more suitable than bipolar devices for very low loss, high speed and high voltage applications. Recently, several SiC FETs with better performance than the theoretical limit of Si FETs have been developed [1-3], but their blocking voltages (BVs) are less than 1,800V. For the electric power utility applications, higher BV is needed therefore we have developed 4.5kV SIAFET [4]. In spite of the conductivity modulation in its channel region, its RonS is a relatively high 387 m Ω cm^2 primarily because of poor channel mobility obtained. Recently, we have developed the SEFET (Static channel Expansion FET) device concept and have fabricated 5.5 kV SEJFET with RonS of 130 m Ω cm^2 [5]. In this paper, we report the development of 4H-SiC SEMOSFET (Static channel Expansion MOSFET) with a high performance by an improvement of channel mobility and by an optimization of a device structure. The developed SEMOSFET has high BV of 5020V, low RonS of 88 m Ω cm^2 and high switching speed of about 40ns at the same time. In all reported FETs, the SEMOSFET has the best trade-off between RonS and BV, which exceeds the theoretical limit of 6H-SiC FET for the first time.

Fig.1 shows a cross-sectional structure of SEMOSFET. It has two gates, an accumulated MOS gate, Gm, and a p+ buried gate, Gp, which can electro-statically expand the channel by applying a positive bias and can reduce the channel resistance drastically. Fig.2 is a photograph of the developed SEMOSFET, with a 1.1 mm x 1.1 mm chip size. Fig.3 shows its reverse V-I characteristics. Its BV is 5.02kV and the leakage current density at 4.5kV is 3 x10^{-5} A/cm^2. Fig.4 shows its forward output characteristics. When applied voltages to Gp and Gm are 2.0V and 20V respectively, Ids is 22.8A/ cm^2 at Vds of 2V, therefore, RonS is 88 m Ω cm^2 Fig.5 shows its turn-off waveforms. Turn-off time is 31ns. Turn-on time has also been measured and is 39ns. Fig.6 shows the trade-off between RonS and BV of normally off type FETs reported. The developed SEMOSFET has the best trade-off and exceeds the theoretical trade-off limit of 6H-SiC. Its figure of merit, BV^2 / RonS, is 287MW / cm^2 and is the largest among the reported FETs. The RonS of 5.0kV SEMOSFET is about 1/140th that of the theoretical limit of a Si MOSFET for this BV.

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[4] Y. Sugawara et al.: Proceedings of ISPSD'2000, pp.105-108.
[5] K. Asano and Y. Sugawara et al.: Proceedings of ISPSD'2001, pp.23-26.

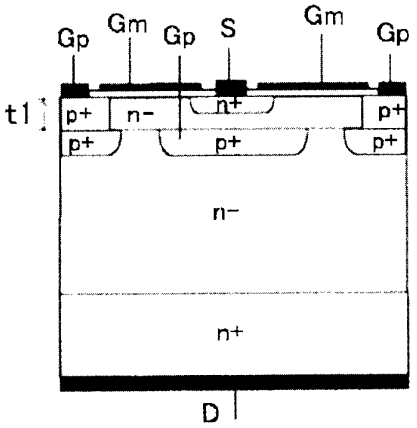


Fig.1. Cross-sectional structure of SEMOSFET.

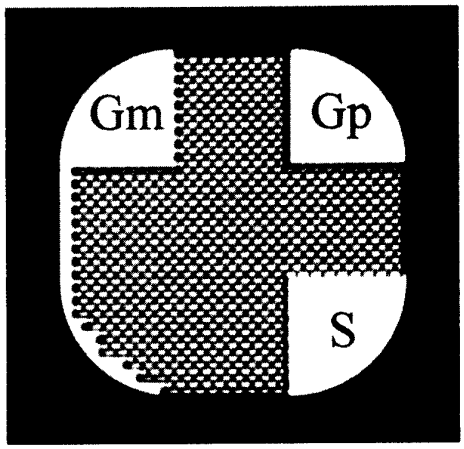


Fig.2. Photograph of developed SEMOSFET.

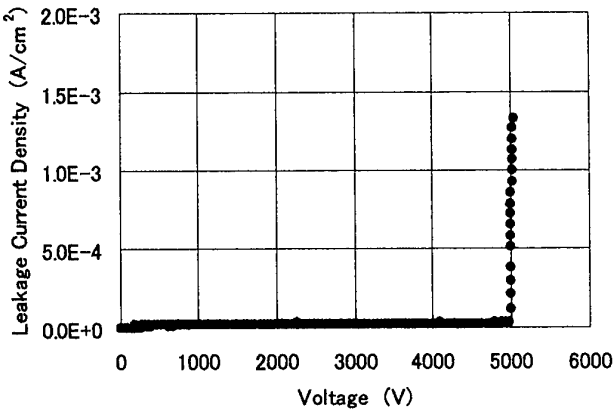


Fig.3. Reverse V-I characteristics.

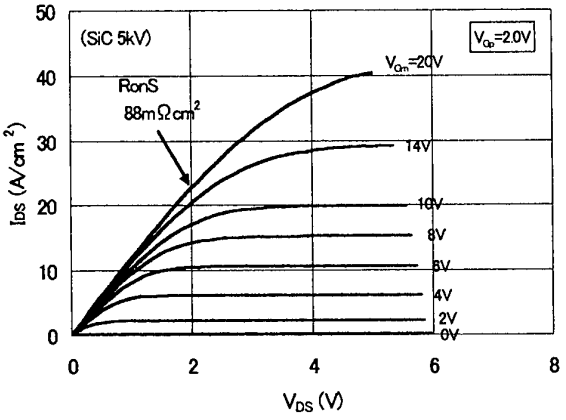


Fig.4. Forward output characteristics.

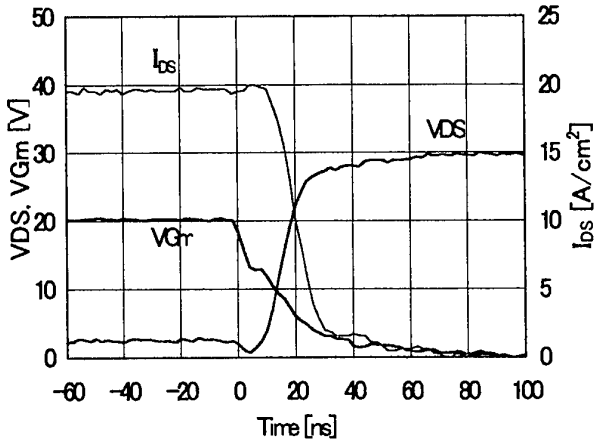


Fig.5. Turn-off waveforms.

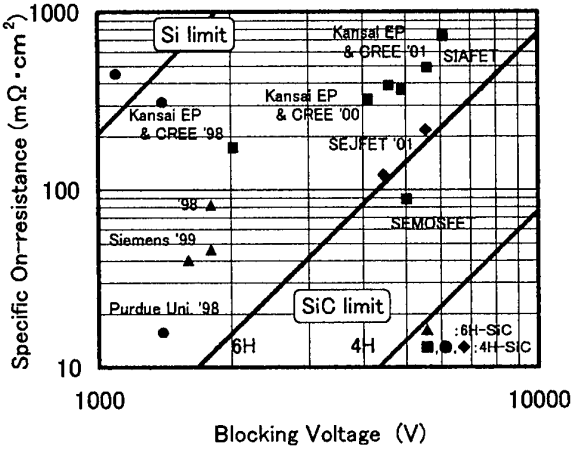


Fig.6. Trade-off between RonS and BV of normally off type FETs reported.

High Performance UMOSFETs on 4H-SiC

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As SiC power switching devices move toward higher operating voltages, it is imperative that proper field terminations be incorporated into the design. Without such terminations, two-dimensional field crowding can occur both internally and at the edges, reducing the breakdown voltage well below that of the theoretical plane junction.

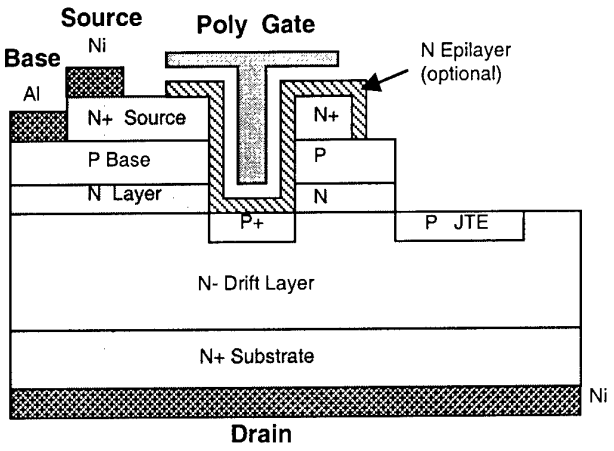
4H-SiC UMOSFETs having both gate trench protection [1] and JTE edge terminations [2] are reported for the first time. The basic device structure is shown in Fig. 1. Two versions of this device are investigated. One version has a thin n-type epilayer grown on the trench sidewalls following RIE to counter-dope the channel, while the other version lacks this feature. Both designs are optimized by extensive 2-D numerical simulations.

In both versions of the device, the gate trenches are protected by an Al implant of $4x10^{13}$ cm^{-2}, 800 nm deep, and the device edges are protected by a 50 μm JTE ring created by implanting Al to a dose of $1x10^{13}cm^{-2}$ and depth of 500 nm. Both implants are annealed at 1550 °C for 30 min. in Ar. A 275 nm gate oxide is formed by thermal oxidation of deposited polysilicon, and a 550 nm polysilicon gate is deposited by LPCVD and doped with phosphorus using spin-on dopant. Ni is used for source and drain ohmic contacts and Al for base and gate trench contacts. All contacts are annealed in Ar at 1000°C for 2 min. The minimum lateral feature size is a conservative 5 μm.

On-state characteristics of both devices are shown in Figs. 2 and 3, and the blocking characteristics in Fig. 4. Because of the thick gate oxide, the threshold voltage is ~ 30 V for the doped-channel FET and ~55 V for the standard FET. The gate voltage is kept below 100 V (oxide field below 4 MV/cm), thereby insuring the long term reliability of the oxide [3]. The doped-channel FET blocks 3,360 V with a specific on-resistance of 199 $m\Omega\text{-}cm^2$ ($V_B^2/R_{ON,SP}$ = 57 MW/cm^2), while the standard FET blocks 3,055 V with a specific on-resistance of 121 $m\Omega\text{-}cm^2$ ($V_B^2/R_{ON,SP}$ of 77 MW/cm^2). To our knowledge, these blocking voltages are the highest reported to date for UMOSFETs in SiC, and the $V_B^2/R_{ON,SP}$ values are close to the highest achieved to date, as shown in Fig. 5. More aggressive layout using 2 μm design rules could easily double this figure of merit.

This work is supported by ONR under MURI grant No. N00014-95-1-1302.

[1] J. Tan, J. A. Cooper, Jr., and M. R. Melloch, *IEEE Electron Device Lett.*, **19**, 487 (1998).
[2] V. A. K. Temple, *IEDM Tech. Dig.*, pp.423-426 (1977).
[3] M. M. Maranowski and J. A. Cooper, Jr., "*IEEE Trans. Electron Devices*, **46**, 520 (1999).



N+ Source: 1e19 cm^{-3} 0.5 μm
P Base: 2e17 cm^{-3} 1.0 μm
N Layer: 2e17 cm^{-3} 0.4 μm
N- Drift Layer: 8e14 cm^{-3} 50 μm
N+ Substrate: 21 mΩ-cm 410 μm
N Epilayer(opt.): 2e17 cm^{-3} 0.1 μm
Gate Oxide: 275 nm
Poly Gate: 550 nm
P+ Trench Impl.: 4e13 cm^{-2} 0.8 μm
P JTE Implant: 1e13 cm^{-2} 0.5 μm

Fig. 1. Structure of the UMOSFET, including JTE edge termination. The JTE is floating, while the gate trench is grounded. The optional N epilayer is present in the doped-channel FET only.

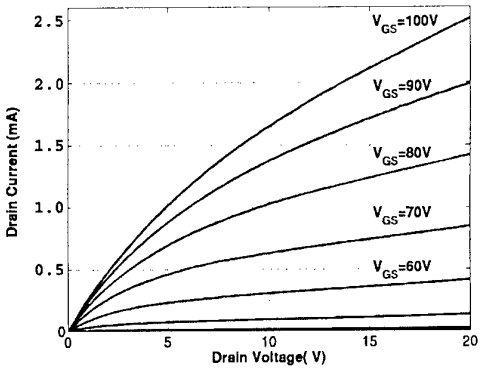


Fig. 2. On-state characteristics of the doped-channel FET. $R_{ON,SP}$ = 199 mΩ-cm^2.

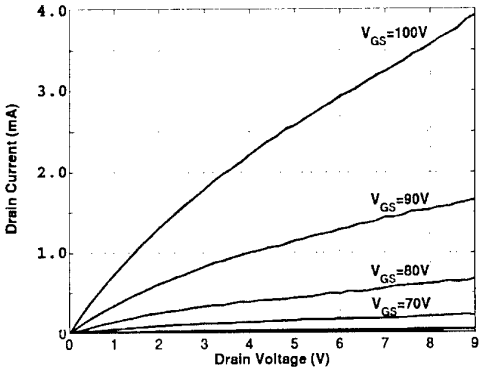


Fig. 3. On-state characteristics of the standard FET. $R_{ON,SP}$ = 121 mΩ-cm^2.

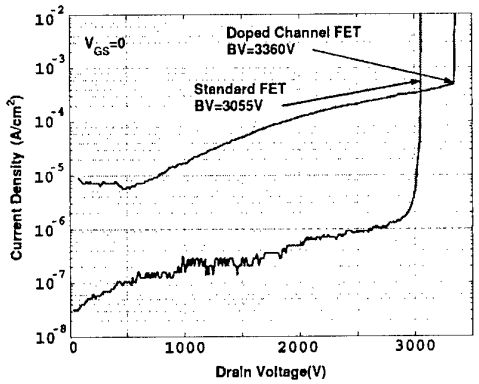


Fig. 4. Blocking characteristics of the doped-channel FET and standard FET.

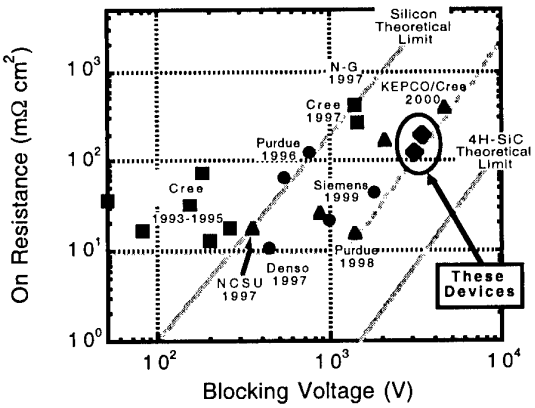


Fig. 5. Performance of recently reported SiC MOSFETs.

SiC Vertical DACFET (Vertical Delta-doped Accumulation Channel MOSFET)

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Makoto Kitabatake, Masao Uchida and Ryouko Miyanaga
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SiC is a promising material for low loss power device because of its high electric breakdown field and high thermal conductivity. However the low channel mobility of SiC MOSFET is a serious problem to be solved, because the low channel mobility leads to an increase of on resistance directly. Therefore much efforts have been made to increase the channel mobility. We have reported the novel SiC MESFET[1] with delta-doped layered channel and its enhanced channel mobility. Here, we fabricated SiC vertical DACFET that is double implanted MOSFET (DIMOSFET) with delta-doped layered channel and characterized.

The cross sectional structure of vertical DACFET is shown in Fig.1. The Delta-doped layered structure is applied as the channel of conventional DIMOSFET. A10 μm thick n^- epitaxial layer were grown on the low resistive n-type 4H SiC substrate(ρ =0.031 $\Omega \cdot$cm). P-well area was formed by aluminum implantation at 500℃ followed by RIE to remove surface unimplanted region and 1700℃ activation anneal. The carrier concentration of P-well was $1x10^{17}cm^{-3}$ and the junction depth was 1.5 μm from the surface. After the annealing the delta-doped layers were grown on the surface by the CVD system with pulse doping method[2]. The delta-doped layered structure consisted of 10nm thick delta-doped layers ($Nd=1x10^{18}cm^{-3}$) separated by 40nm thick undoped layers. The number of delta-doped layers was four. Source area was formed by nitrogen implantation at 500℃ followed by 1500℃ activation anneal. The gate oxidation was performed at 1100℃ for 3 hours in wet oxygen gas followed by re-oxidation at 800℃ for 2 hours in dry oxygen gas. The gate oxide thickness was around 40nm. Ni was deposited as source contact metal and also as back side drain ohmic contact followed by 1000℃ 5min. rapid thermal annealing (RTA). Al was deposited and patterned as gate electrode. The 500nm thick Silicon-oxide film was deposited with plasma CVD as inter level dielectric. The contact hole was made by RIE and Al was deposited and patterned as upper level metal. The gate length Lg is 10 μm and the spacing S between P-wells is 10 μm.

The typical DC current-voltage (I-V) characteristic of the FET is shown in Fig.2. The chip has 9 square cells. The total gate width and the active area of this device were 2.1mm and $7.0x10^{-4}cm^2$, respectively. Specific on resistance calculated from this active area was 110m$\Omega \cdot cm^2$ at a Vgs of 12V (S=10 μm).

References
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(2) K.Takahashi et al., Mater. Sci. Forum **338-342**,141(2000)

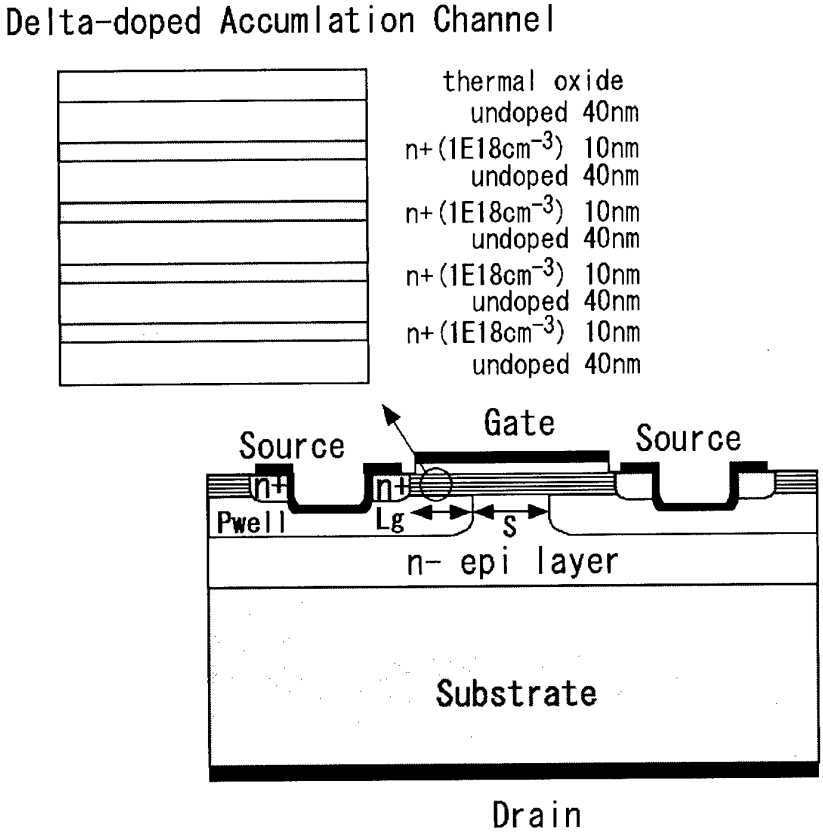


Fig.1 The cross section of SiC DACFET. Left above is the detail of delta-doped layered structure.

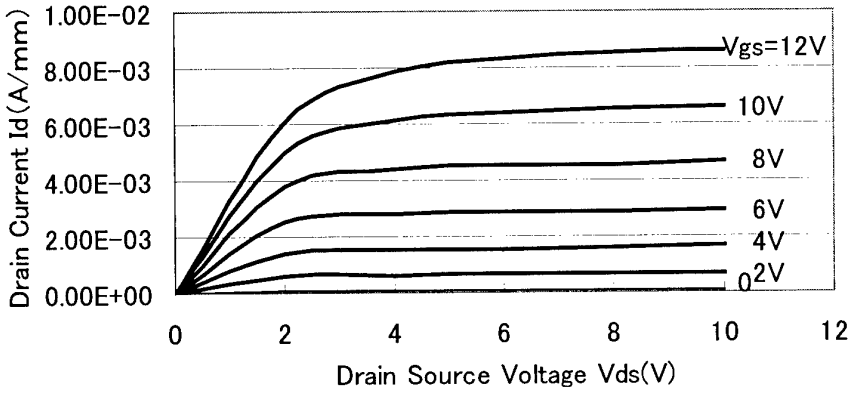


Fig.2 The typical I-V characteristic of SiC DACFET(Lg=10 μ m,W=2.1mm)

Silicon/Oxide/Silicon Carbide (SOSiC) – a new approach for high voltage, high frequencies integrated circuits

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Abstract

A novel device structure/technique termed SOSiC (Silicon On Silicon Carbide) is proposed here for the first time for use in Power Integrated Circuits (PICs). The new device structure is based on Silicon-on-Insulator technology with a SiC substrate in place of a conventional Si substrate. We demonstrate that the change to SiC substrate offers unique and major advantages for high voltage integrated circuits such as (i) significantly increased breakdown voltage due to extension of the depletion region in the SiC substrate, (ii) considerably reduced self-heating owing to the SiC higher thermal conductivity and (iii) higher switching frequency due to the reduced parasitic substrate capacitance. We demonstrate the crucial advantages of this structure in typical high voltage lateral devices through extensive numerical simulations.

SOI in high voltage power integrated circuits

SOI technology is every day winning more and more ground in Integrated Circuits. In particular in PICs, SOI offers a high level of isolation, reduced cross-talk and significantly reduced leakage current compared to standard Junction-Isolation technology. However, the SOI technology suffers from three main drawbacks: reduced breakdown voltage, overheating and lower switching frequency for unipolar devices. The first limits the applicability of the SOI technology to high voltage ICs and imposes a severe limit on the minimum buried oxide thickness. Typically, a thickness of 1-1.5 microns of the buried oxide is needed per 100 V blocking voltage. The higher the thickness of the buried oxide, the stronger the thermal barrier from the active structure to the heat sink leading to severe self-heating. Finally, the switching frequency of LDMOSFETs is lower than that of the Junction-Isolation high voltage ICs due to the absence of the substrate depletion region which serves to decrease the parasitic substrate capacitance during high voltage switching. The absence of the depletion layer in the Si substrate (indifferent of the doping of the substrate) is due to the field plate shield formed by the inversion/accumulation layer which appears under the buried oxide at high voltages.

SOSiC versus SOI

In this paper we propose a completely novel approach to high voltage PICs using a Si/oxide/SiC structure (Fig. 1). In the top Si layer, the active high voltage structures, compatible with CMOS or BiCMOS IC technology are formed. The SiC substrate serves to increase the device breakdown and frequency and, at the same time, reduce self–heating. The buried oxide acts as an electrical isolation layer between the active structures and the SiC substrate. The increase in the breakdown voltage on one hand, and reduction in the substrate capacitance which relates to higher switching frequency on the other hand, rely on the formation of a wide depletion region in the SiC substrate under the buried oxide. This is entirely different from conventional SOI using standard Si substrates. The reason for the depletion region is due to the wide-band gap of SiC substrate. Thus, the charge in the inversion/accumulation surface layer in the SiC substrate is very weak and the charge compensation across the buried oxide is mainly achieved through the formation of a depletion layer in the SiC substrate. Fig. 2 shows the breakdown characteristics for two identical PIN diodes in SOI and SOSiC configurations. The potential distributions at breakdown for a classical SOI and SOSiC structure are shown in Fig. 3 and 4 respectively. As seen in Fig. 4, the potential lines extend deeply into the depletion region of the SiC substrate thus resulting in a more efficient Resurf effect and hence significantly increased breakdown voltage (Fig. 2). Fig. 5 shows, as expected, that owing to the higher thermal conductivity of the SiC substrate, the SOSiC LDMOSFET is also less prone to self-heating than its conventional SOI variant. Finally, as already mentioned, the formation of the depletion region in the SiC substrate in the SOSiC LDMOSFET leads to a reduction in the drain/substrate capacitance, which in turn results in a faster switching. This is proven by looking at the inductive switching of an LDMOSFET in SOSiC compared to a conventional SOI in identical inductive conditions (Fig. 6).

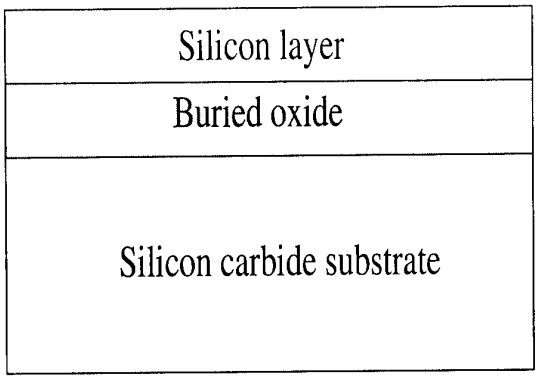


Fig. 1 Schematic cross section of the silicon/oxide/silicon carbide (SOSiC) structure

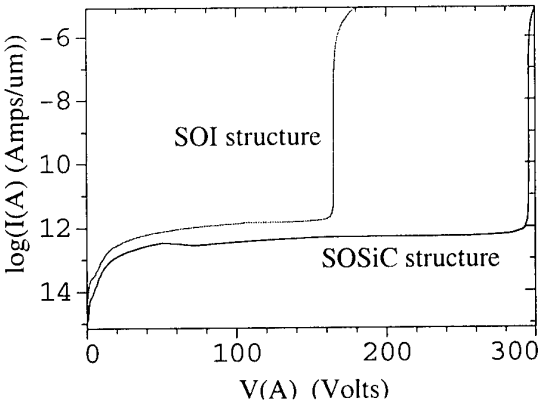


Fig. 2 The breakdown characteristics for two identical PIN diodes in SOI and SOSiC configurations

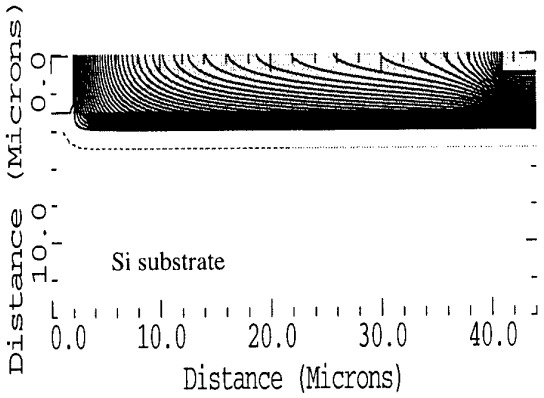


Fig. 3 The potential distribution at breakdown for a classical SOI PiN diode – V_{BR}=168V

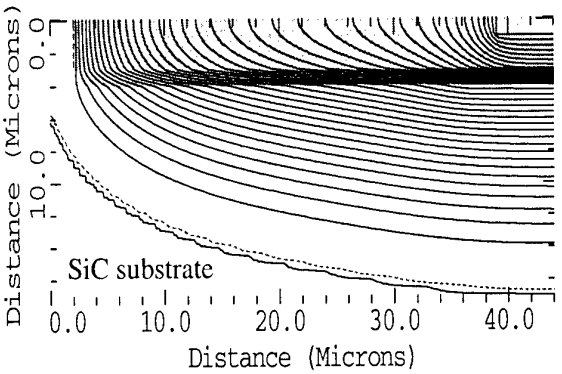


Fig. 4 The potential distribution at breakdown for a SOSiC PiN diode – V_{BR}=299V

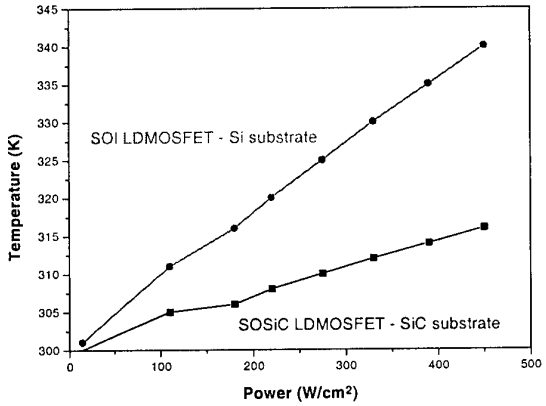


Fig. 5 The self heating effect represented in a conventional SOI LDMOSFET and in a novel SOSiC structure LDMOSFET.

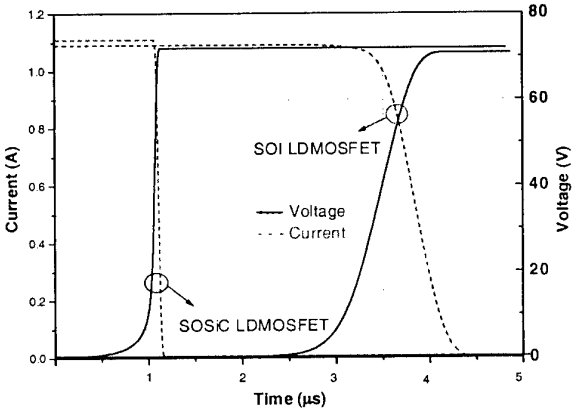


Fig. 6 The inductive switching behaviour of a conventional SOI LDMOSFET and a SOSiC LDMOSFET

WeB4 Intrinsic Defects

[redacted]

The nature and diffusion of intrinsic point defects in SiC

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In SiC intrinsic point defects inevitably occur. Incorporated during growth or induced by processing they can reduce the electronic quality of the material. In addition mobile intrinsic defects, namely vacancies and interstitials, play a pivotal role in the annealing kinetics and mass transport. For example in recent experiments [1] a transient enhanced dopant diffusion was observed that seriously affected the implanted dopant profiles. An analysis of diffusion profiles [2] indicates that most likely silicon interstitials drive the boron migration in SiC. However, any question related to the mechanisms of defect migration at the same time addresses the nature of the involved defects.

Based on an *ab initio* method we have developed a microscopic theory of the mobile intrinsic defects and their migration. The investigation of the ground state properties of interstitials, vacancies, antisites and their complexes forms the basis of our study. The calculation of hyperfine parameters and localised vibrational modes enables us to contribute to the identification of experimentally observed defect centers.

Our investigation of the defect hierarchy shows that silicon interstitials and carbon vacancies are the most abundant mobile intrinsic defects in p-type and intrinsic material. The latter also dominate under n-type conditions. Silicon vacancies, which in n-type material dominate over silicon interstitials, play a special role. Our calculation reveal that the vacancy is a metastable/bistable defect (3C-SiC and 4H-SiC rsp.) that can transform into a carbon-vacancy-antisite-complex. In p-type material this transformation is accompanied with a large energy gain. Therefore we find that silicon interstitials are the only mobile Si-related defects under these conditions. However, in n-type material we expect a relevant contribution from the vacancy to diffusion as its migration on the Si-sublattice has a lower barrier than the above mentioned transformation. The migration of carbon vacancies proceeds entirely on the carbon sublattice. According to our calculations they are rather immobile which is in contrast to the high mobility deduced from the annealing behaviour of the EPR-centers T5 [3] (3C-SiC) and EI5 [4] (4H-SiC) interpreted as carbon vacancies. Though our calculated hyperfine parameters do not support the assignment for the T5 center our results in 4H-SiC point to a correct interpretation of the latter. An explanation for the annealing behaviour is the recombination of the vacancy with carbon split-interstitials: their high mobility should be responsible for the observed effect. Another footprint of the mobile split interstitials is the D_{II} photoluminescence center which is kineticly formed during the annealing. We identify this center as a complex formed by a carbon antisite and a carbon split-interstitial. The calculated localised vibrational modes nicely agree with the experimentally observed phonon replica [5]. We discuss in detail the nature of the relevant intrinsic defects and the impact of our findings on the dopant and self diffusion.

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C-Interstitials in SiC: a Model for the D_{II} Center

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For decades the microscopic structure of the D_I and the D_{II} centers in SiC has been subject to thorough investigations. Both centers occur independently of the polytype and the implanted dopant which has led to the assumption that they are intrinsic defects. While the structure of the D_I center still remains uncertain, a C-di-interstitial configuration has been proposed for the D_{II} center to explain the results of photo luminescence experiments [1,2]. The characteristic spectra show five one-phonon lines related to diamond-like localized vibrational modes (LVM) above the SiC bulk phonon spectrum and two localized modes within the SiC phonon gap (gap modes). The spectra persist annealing above 1700°C. A strong binding between the C-di-interstitial and its carbon bonds would qualitatively account for the observed thermal stability of the spectrum and the diamond-like LVMs. Employing a density functional theory based *ab initio* method we have analyzed the phonon modes of relevant defects with diamond-like bonding in the polytypes 3C and 4H. For the di-interstitial configuration we find a high formation energy of approximately 12 eV. Energetically much more favorable are split-interstitial configurations, i.e. two C-atoms sharing a lattice site [3], which are natural candidates for the D_{II} center due to their C-dimer bond. The highly abundant carbon antisite is expected to be a thermally stable defect as well. It has much weaker carbon bonds, though, and hence cannot explain the observed high frequency LVMs. For a C-split-interstitial on an antisite ($C_{spC_{Si}\langle 100\rangle}$) we find the diamond-like localized phonon modes in good agreement with the experiment. Additionally we are able to reproduce the two gap modes within the phonon band gap. The interstitial $C_{spC_{Si}\langle 100\rangle}$ is formed during the diffusion of the most abundant C-interstitial $C_{sp\langle 100\rangle}$ in a reaction with a carbon antisite. The latter C-interstitial has the lowest migration barrier among the intrinsic interstitials and vacancies [4] and its mobility is most likely responsible for the annealing of the carbon vacancy by an interstitial-vacancy recombination. From the large binding energy of $C_{spC_{Si}\langle 100\rangle}$ (3.7 eV–4.5 eV) we expect a high thermal stability of this defect, which parallels the properties of the D_{II} center. We discuss in detail the relevance of $C_{spC_{Si}\langle 100\rangle}$ and the other defects as a model of the D_{II} center.

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Radiation-Induced Defects in 4*H* and 6*H* SiC Epilayers Studied by Positron Annihilation and Deep Level Transient Spectroscopy

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The understanding of fundamental properties of point defects in SiC is the key for device processing because the electronic characteristics of crystals are strongly altered by them. In this study, we characterized vacancy-type defects in 4*H* and 6*H* SiC epilayers induced by electron irradiation using positron annihilation and deep level transient spectroscopy (DLTS). From the correlation between positron annihilation and DLTS data using the same wafers, it is confirmed that complexes including silicon vacancies are the origin of the $E_{1/2}$ levels in 6*H* SiC and the $Z_{1/2}$ level in 4*H* SiC.

Specimens are chemical-vapor-deposition (CVD) grown *n*-type 4*H* and 6*H* SiC epilayers (5 μm thick) doped with nitrogen (the net donor concentration is 5×10^{15} cm^{-3}). These specimens were irradiated with 2 MeV electrons with doses from 1×10^{15} to 3×10^{17} e^-/cm^2 at room temperature. Isochronal annealing was conducted from 100 to 1700 °C for 30 min in vacuum or dry argon ambient. Positron annihilation (the Doppler broadening and

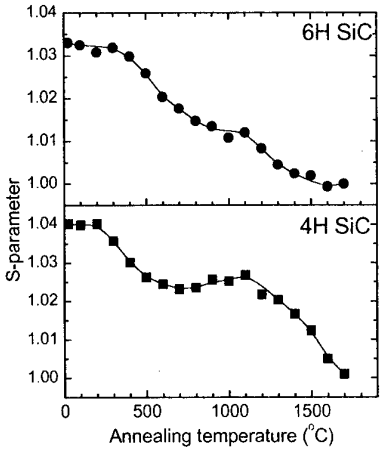


Fig. 1 Annealing behavior of *S*-parameters for the electron-irradiated 6*H* and 4*H* SiC specimens.

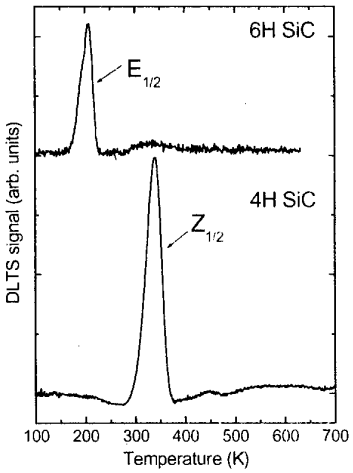


Fig. 2 DLTS spectra for the electron-irradiated 6*H* and 4*H* SiC specimens obtained after annealing at 1200°C.

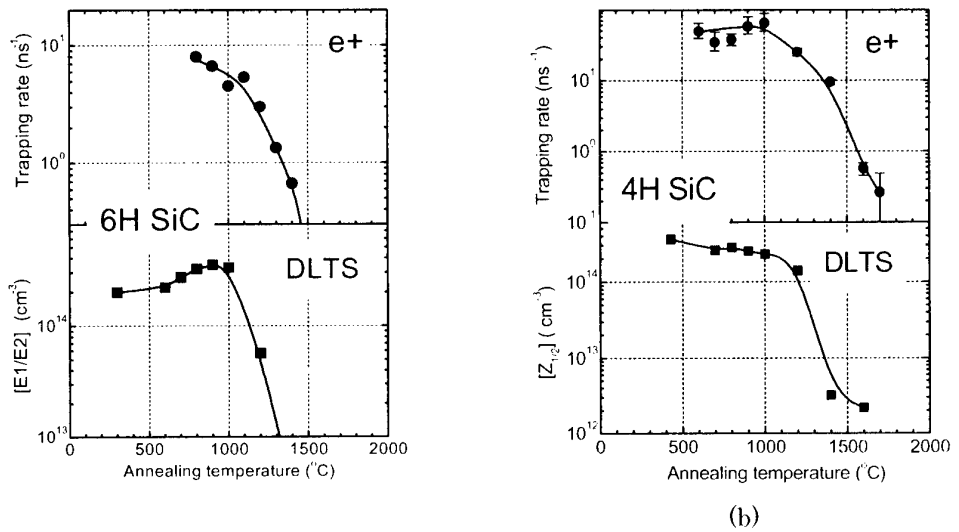
lifetime) measurements were performed using slow positron beams at room temperature. After fabricating ohmic and Schottky contacts using Ni, DLTS measurements were carried out in the temperature range from 100 to 700 K.

Figure 1 shows the annealing behavior of the *S* parameter after electron irradiation (dose: $3x10^{17}$ e^-/cm^2). It is found that the *S* parameter decreases in two steps, i.e., until 600 °C and above 1000 °C in both polytypes. This shows that vacancy-type defects disappear in these temperature regions. The further analyses using the *S-W* correlation and the coincidence Doppler broadening method shows that silicon vacancy-related defects dominate the above annealing processes [1]. Since isolated silicon vacancies are mobile below 1000 °C, the lower annealing stage can be attribute to the disappearance of isolated silicon vacancies and the other types of vacancies. The higher annealing stage should be interpreted in terms of complexes including silicon vacancies. From the DLTS measurements [2,3], a series of deep levels are found to be introduced in the upper half of the band gap. From Fig. 2, it is seen that the $E_{1/2}$ level in 6*H* SiC and the $Z_{1/2}$ level in 4*H* SiC, which are thought to have the same atomic arrangement in these polytypes, survive after annealing above 1000 °C. Consequently, these levels should be compared with the vacancy-type defects detected by positron annihilation. As shown in Figs. 3(a) and (b), the positron trapping rate (proportional to the defect concentration) of silicon vacancy related complexes and the concentration of the corresponding DLTS centers decreases in the similar way during the annealing between 1000 and 1500 °C. This allows us to conclude that the $E_{1/2}$ and $Z_{1/2}$ level in 6H and 4*H* SiC, respectively, are related to complexes including silicon vacancies.

[1] A. Kawasuso *et al.*, JAP to be published.

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(b)

Fig. 3 Comparison between the positron trapping rate related to silicon vacancies and the concentrations of (a) $E_{1/2}$ levels in 6*H* and (b) $Z_{1/2}$ levels in 4H specimens.

Chemical environment of atomic vacancies in electron irradiated silicon carbide measured by a two-detector Doppler broadening technique

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The paper presents a new positron annihilation technique [1] for the characterization of lattice defects in 6H-SiC in combination with the generation of defects by electron irradiation. The two-detector (2D) Doppler broadening technique allows the determination of the chemical environment of lattice defects which trap positrons. Coincident measurement of the energy of the two positron-electron annihilation photons gives the possibility to increase the signal to noise ratio up to 10^5 and extends the range of measurements of a Doppler broadened line up to (511±15) keV. The high energy part of the Doppler broadened spectrum is characteristic for the carbon and silicon core electron momentum distribution and therefore contains information about the chemical environment of a lattice defect in SiC.

For the present studies single crystals of 6H-SiC (Cree Inc., Durham, NC, USA) with n-type conductivity were used. Coincident measurements of the Doppler broadening of the positron-electron annihilation γ spectrum for background suppression were performed with a collinear set-up of two high-purity Ge detectors. The full-width at half-maximum (FWHM) of the energy resolution function was equal to about 1.2 keV. The positron lifetime was measured by means of a fast-slow $\gamma\gamma$ spectrometer with a time resolution of 205 ps (FWHM). For both techniques a ^{22}NaCl positron emitter stacked between two identical SiC specimen plates was used. The irradiation experiments on 6H-SiC for the generation of vacancies on both carbon and silicon sublattices by electrons of the energies: 0.5, 1, and 2 MeV and doses of about 10^{-23} m^{-2}, were performed at the Dynamitron accelerator of Stuttgart University.

The ratios of the coincident counts of the Doppler broadening measured for the electron irradiated SiC and for the reference materials are plotted in Fig.1. As determined by the model suggested in [2] and applied in [3] for 6H-SiC the electron momentum range lower than 20 $m_0c\cdot10^{-3}$ is due to annihilation of the positrons with valence electrons. Because of the low number of counts the range above 40 $m_0c\cdot10^{-3}$ is strongly affected by the background and all ratio curves independent of specimen meet there at the value of one (see Fig.1). Therefore, to obtain information about the chemical environment of the positron annihilation site in SiC only the shape of the ratio curves in the range from 20 to 40 $m_0c\cdot10^{-3}$ (see Fig.1) is considered. The position of the whole ratio curves with respect to the ordinate is proportional to the intensity of the core electron component or to the density of the material in the positron annihilation site and is independent from the chemical environment of this site.

In the range from 20 to 40 $m_0c\cdot10^{-3}$ the characteristic behavior of carbon core electrons shows a positive slope and that of silicon core electrons a negative slope of the ratio curve as obtained from the measurements on diamond and Si single crystals respectively (see Fig.1). The opposite slope of the ratio curves for carbon and silicon originates from positron annihilation with core electrons of both carbon and silicon atoms in as-grown SiC. The sum of two linear curves with opposite slope gives a horizontal line for as-grown SiC. The

delocalized positron wave function in this specimen overlaps the electron wave functions of both carbon and silicon core electrons and positrons are annihilated from the free state. The measured positron lifetime of 148 ps is close to the calculated free positron lifetime for SiC and supports this result.

The ratio curves for SiC irradiated by 1 MeV (Fig.1) and by 2 MeV electrons have positive slopes which are characteristic for carbon core electrons and therefore positrons are trapped by silicon vacancies in these specimens. The much lower position of the curve in comparison to non-irradiated carbide reflects the smaller overlap of the positron wave function with core electrons of atoms around the free volume of the vacancy. The positron lifetime of 210 ps measured for both of these specimens can be attributed to the silicon vacancy. The ratio curve for SiC irradiated by 0.5 MeV electrons has an intermediate position and almost no slope (Fig.1). Therefore, positrons are annihilated with core electrons of both carbon and silicon atoms in this specimen. This is in agreement with the positron lifetime of 179 ps which lies in between the silicon (210 ps) and the carbon (160 ps) vacancy positron lifetime. Therefore, the 0.5 MeV electrons displace nearly the same amount of C and Si atoms in SiC.

The present demonstration of the identification of vacancies on the two sublattices opens new potential for the attributing of energy levels in the band-gap of SiC to specific atomic defects.

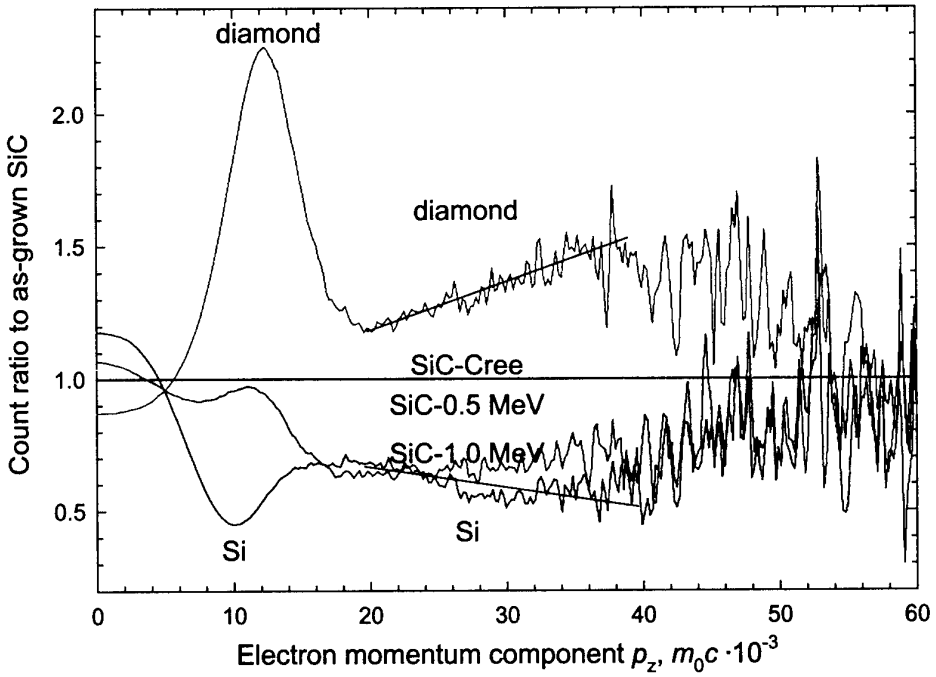


Fig.1. Count ratios of the 2D-Doppler broadened spectra of diamond, silicon, 6H-SiC after irradiation with 0.5 MeV and 6H-SiC after irradiation with 1.0 MeV electrons to the 2D-Doppler broadened spectrum of as-grown 6H-SiC. The lines for the diamond and Si single crystalls curves are guides for the eye.

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Vacancy defects in as-polished and in high fluence H+ implanted 6H-SiC detected by slow positron annihilation spectroscopy

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Electronic and optoelectronic devices performances lies particularly on the surface and subsurface quality of the substrate used to build the structure. It is necessary to eliminate the defects generated by cutting process and surface preparation. Furthermore hydrogen implantation is used in SiC for passivation, doping and the Smart Cut process. However, the role and type of defects controlling the electrical properties in 6H-SiC(H) is far from fully understood.

Different characterization methods have been used to investigate the defects in semiconductors. Positron annihilation spectroscopy is a non destructive technique, which showed its power in detecting native and induced vacancy type defects in semiconductors. Slow positron beam based techniques allow to probe vacancy defects as a function of depth in the few μm range below the surface.

In this work we used slow positron annihilation spectroscopy to study on one hand the elimination of defects in as-polished bulk n-type 6H-SiC wafers and on the other hand the charge state of vacancy defects in high fluence H^+ implanted and annealed epitaxial n-type 6H-SiC layers.

I Defects investigated after polishing

The positron annihilation experiments were performed with a slow positron beam (ref 1) at the CERI laboratory in epitaxial and bulk n-type 6H-SiC wafers, in as-received state or after two different polish process performed by Novasic: a mechanical one and a mechano-chemical one.

The positron-electron pair momentum distribution has been investigated. It was measured at 300 K by recording the Doppler broadening of the 511 keV annihilation line which is proportional to the momentum component of the annihilating electron-positron pair, p_L, along the emission direction of the photons: $2\Delta E_\gamma = cp_L$. Two parameters are used to characterize the shape of the momentum distribution. The low momentum parameter S corresponds to the fraction of annihilations taking place in the momentum range $(0\text{-}|2.80|) \times 10^{-3}\ m_0c$. The high-momentum parameter W corresponds to the fraction of annihilations taking place in the momentum range $(|10.61|\text{-}|26.35|)\times 10^{-3} m_0c$. To investigate the depth dependence of S and W, the curves S(E) and W(E) were recorded as a function of the beam energy E changed

in 0.5 keV steps in the 0.5 to 25 keV range. The positron mean implantation depth in 6H-SiC varies from 5 nm to 2.1 μm in this energy range.

S (E) and S(W) curves (Fig 1a and 1b) show that vacancy defects are present in the subsurface region in the only mechanically polished sample. These defects are not detected after the mechano-chemical polishing step.

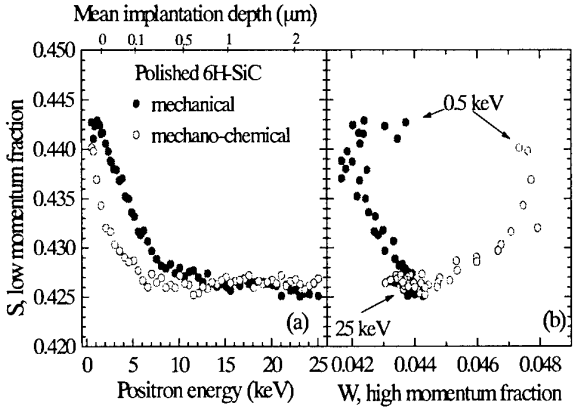


Figure 1. Low momentum fraction S as a function of positron beam energy (1a) and as a function of high momentum fraction W (1b) in 6H-SiC wafers polished in different conditions: only mechanical or mechano-chemical polishing .

II Negatively charged vacancy defects in 6H-SiC after low energy H+ implantation and annealing

The Smart Cut process is used to produce thin SOI heterostructures by low energy hydrogen implantation to fracture a thin layer after its bonding via SiO_2 to a SiO_2/Si substrate. In highly doped n-type 6H-SiC, a partial compensation of the electrical activity persists after the 900°C annealing inducing the fracture.

We have used pulsed-slow-positron-beam-based positron lifetime spectroscopy to investigate the nature of acceptors and charge states of vacancy-type defects in low-energy proton-implanted 6H-SiC(H). We can infer from the temperature dependence of the lifetime spectra that neutral and negatively-charged vacancy clusters exist in the track region. Depending on annealing, they give rise to positron lifetimes of 257 ± 2 ps, 281 ± 4 ps and 345 ± 2 ps, respectively. The 281 ps cluster has likely an ionization level near the middle of the bandgap. By comparison with theory, the 257 ps and 280 ps are identified as $(V_C\text{-}V_{Si})_2$ and $(V_C\text{-}V_{Si})_3$ clusters, respectively. In addition, other acceptors of ionic type act as strong trapping centers at low temperature (T<150 K). Neutral monovacancy-like complexes are also detected with a lifetime of 160 ± 2 after 900° C annealing.

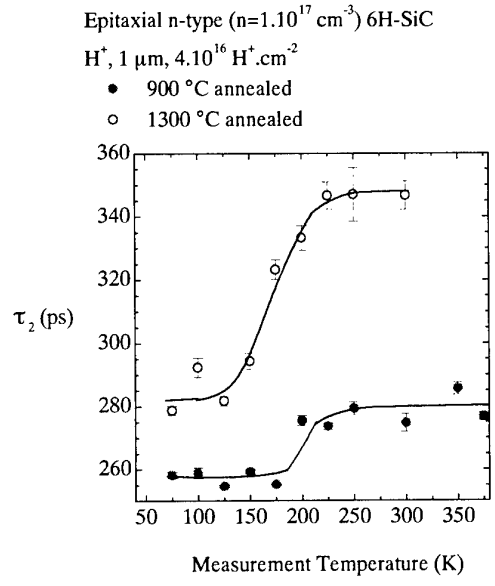


Figure 2: Long lifetime component extracted from positron lifetime spectra measured with 9keV positron as a function of temperature in H+ (1 μm, 4.10^{16} cm^{-2}) implanted 6H-SiC after annealing at 900 and 1300°C.

ESR characterization of SiC bulk crystals and SiO_2/ SiC interface

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Impurities and defects, even in low concentrations, often strongly affect the electronic properties of device materials. At present, the process technology of SiC still remains at such a stage as one that requires a considerable refinement in controlling impurities and defects. Improvement of the doping efficiency is one of major subjects in the ion implantation doping. For the substrate crystals, lowering the concentration of unwanted impurities and defects are highly demanded. Reduction of the interface defects is important for improving the SiC-MOS device properties. ESR (electron spin resonance) is a powerful tool for identifying impurities and defects by supplying detailed microscopic structural information. Definite identification of point defects such as impurities, vacancies, anti-site-defects in various semiconductor crystals as well as interface defects (P_b center) in SiO_2/Si have been attained by using ESR. In our present work, we have applied ESR technique to characterize SiO_2/SiC. Impurities and defects both in SiC substrate (i.e. bulk crystals) and at SiO_2/SiC interface have been studied.

1. Dangling bond type defect

The identification of the P_b center to be a silicon dangling bond at the silicon surface of the SiO_2/Si(111) interface has been well-established. Searching of an ESR signal that is arising from an interface defect having a structure similar to the P_b center has been, so far, failed in SiO_2/SiC. In the samples of SiO_2/*p*-6H-SiC(0001), we have found a new ESR spectrum (denoted here as PERC-1) that is arising from a silicon dangling bond along the [0001] axis. The carrier concentration of the substrate was$\sim 1\times10^{14}cm^{-3}$. The oxidation was performed at 1200°C in dry O_2. As shown in Fig.1, the spectrum consists of a set of primary line and ^{29}Si (I=1/2, natural abundance 4.67%) hyperfine lines with B//[0001]. With the crystal rotated around $[1\bar{1}00]$, the spectrum splits into two sets. We assume that the splitting is caused by site-splitting. The ^{29}Si hyperfine interaction determined by fitting of the angular dependence of the line positions is nearly axial with the three principal values 123.8, 123.9, and 172.2 G, respectively. The largest principal value is along [0001]. The wave function of the unpaired electron is described by the linear combination of atomic orbital approximation:

$$\Psi = \eta(\alpha\,\phi_{3s} + \beta\,\phi_{3p}) + \cdots.$$

The orbital parameters for the silicon atom giving the ^{29}Si hyperfine interaction are listed in

TABLE. We note that a high fraction (η^2=0.64) of the unpaired electron is localized on one silicon atom with a high *p*-character (*sp* ratio: β^2/α^2 = 4.6). The direction of the *p*-orbital is along [0001]. Thus, the PERC-1 center has a dangling-bond character expected for P_b-like interface defect. The signal does not exhibit a strong anisotropy of the line width that is distinctly observed in the P_b center and that is caused by distribution of structure. To identify that the PERC-1 spectrum is arising not from such centers in the bulk as dangling bonds at void and vacancy-impurity complexes but from interface defects, the location of the center needs to be determined.

An ESR signal similar to PERC-1 has been observed also in SiO_2/4H-SiC. In the samples of SO_2/4H-SiC, there exists a dominantly strong isotropic signal. To extract selectively the relatively weak signal of the dangling bond center which is hidden underneath the strong isotropic signal, pulsed-ESR technique has been utilized.

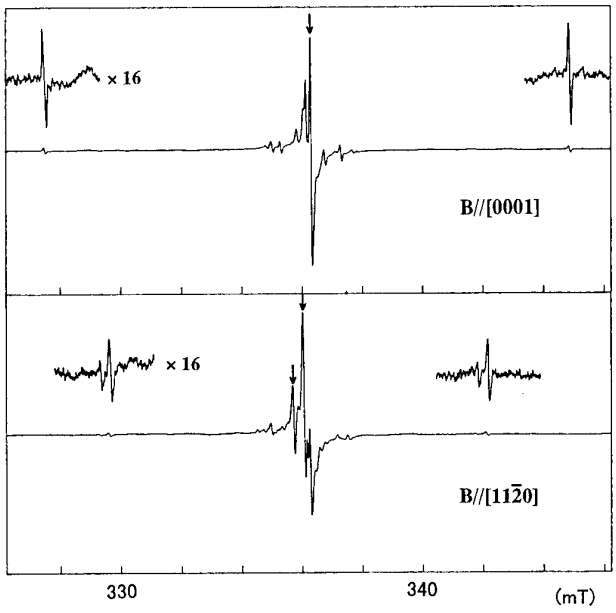


Fig.1 ESR spectrum of SiO_2/*p*-6H-SiC (R.T.)

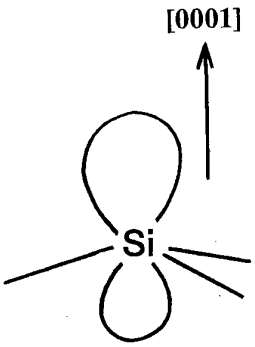


TABLE. Hyperfine and orbital parameters

	$A_{//}/g_e\beta_e$ (G)	$A_{\perp}/g_e\beta_e$ (G)	α^2	β^2	η^2
PERC-1	172	124	0.18	0.82	0.64
P_b center [1]	156	91	0.12	0.88	0.80

[1]K. Brower, Appl. Phys. Lett. 43, 1111 (1983)

2. Impurities

As demonstrated in Fig.2, the samples of SiO_2/*p*-6H-SiC exhibit a relatively large number of signals of impurities and defects. Most of them are arising from the substrate. ESR parameters and the structural models of these impurities will be presented.

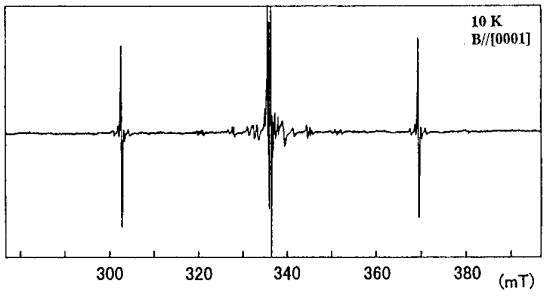


Fig.2 ESR spectrum of SiO_2/*p*-6H-SiC

EPR study on the single silicon vacancy related defects in 4H-, 6H-SiC

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The spin triplet (S=1) single silicon vacancy related defects in electron irradiated n-type 4H, p-type 6H-SiC were studied by electron paramagnetic resonance (EPR) spectroscopy. By laser irradiation, the hyperfine couplings (HFC) with nearest-neighbor (NN) atoms of T_{V2a} were observed for the first time. From the detailed analysis, T_{V2a} was unambiguously assigned to be the single silicon vacancy.

Vacancy is one of the most important intrinsic defects. It exhibits interesting physics and is extensively studied experimentally and theoretically in many semiconductors. Particularly in SiC, it is well known that vacancy is stable even at room temperature (RT).

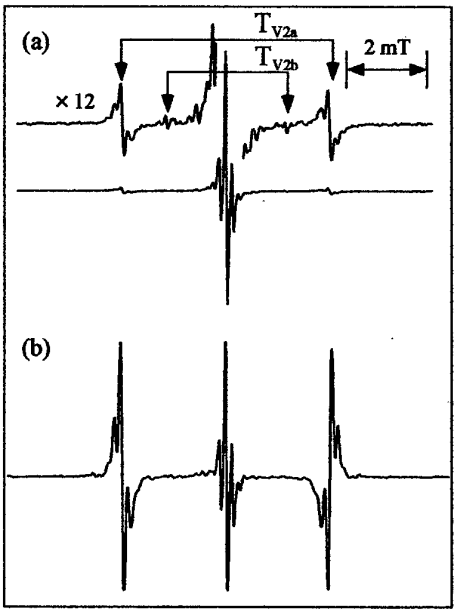


Fig. 1

In our electron irradiation condition (3 MeV, total fluence 4×10^{18} e/cm^2 at RT), thermal equilibrated EPR signals of T_{V2a} and T_{V2b} in 4H-SiC were observed at RT for the first time as shown in figure 1 (a). In the previous optically detected magnetic resonance (ODMR) studies of T_{V2a} by E. Sörman et al.,[1] they observed small HFC that are very similar with those of the next-nearest-neighbor silicon of silicon vacancy. From this observation by ODMR, they suggested that T_{V2a} is the silicon vacancy related defect. [1]

For the assignment of the vacancy, it is important to know information of the NN atoms of the defect center. Furthermore, by obtaining the HFC constants of the NN atoms of the defect center, the detailed structural information can be obtained. For the detailed analysis of

HFC, the improvement of the signal to noise ratio is necessary because the natural abundances of the ^{13}C (1.1 %) and ^{29}Si (4.7 %) isotopes are very small. Furthermore the selective amplification of the signal is also important not to be superimposed by other signals. To amplify the signal selectively, we irradiated the continuous wave laser light (808 nm; a Coherent FAP-system with 10 W) during the X-band EPR measurement and could amplify the signal of T_{V2a} selectively as shown in figure 1(b). From this success, the HFC of NN atoms of T_{V2a} were observed for the first time and are shown as C_1 and C_2 in figure 2. The spectrum shown is the one when the magnetic field is parallel to the [0001] (c-axis). The intensity ratio between their total integrated intensity and that of the central line was 4.5 %. It almost corresponds to the theoretically calculated value (4.2 %) in the case that the NN atoms are four C atoms. None of the HFC of the common impurities in SiC, such as N, Al, B, Ti, V, or H, is observed. From these facts, it is revealed that the NN atoms around the T_{V2a} are four carbons.

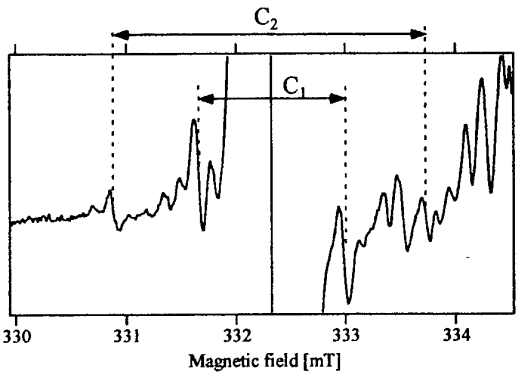


Fig. 2

We also investigated the angular dependence of the HFC of the NN. The obtained HFC constants are shown in Table. Obtained information from the analysis is summarized as follows. Its symmetry of the structure belongs to the C_{3v} point group. In the wavefunction of the unpaired electron, 57 % of the unpaired electrons is localized on the nearest four C atoms. From the observation of four ^{13}C around T_{V2a} and the dense electron spin density on those, T_{V2a} can be unambiguously assigned to be the single silicon vacancy. From the estimated spin density and the very small D-value, it is considered that the extent of distortion along the c-axis is considered to be very small. The details of analysis and structural information will be presented.

TABLE. Hyperfine coupling constants (A_{iso} ; isotropic part, A_{aniso} ; anisotropic part)

	A_{iso}(MHz)	A_{aniso}(MHz)
$A(C_1)$	44.8	15.5
$A(C_2)$	50.0	15.1

[1]E. Sörman, N. T. Son, W. M. Chen, O. Kordina, C. Hallin, E. Janzén, *Phys. Rev. B* **61**, 2613 (2000).

WeP Poster Session II

Liquid Phase Epitaxial growth of highly Al doped p-type contact layers for SiC devices and resulted Ohmic contacts.

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High Al doping level in Silicon Carbide layers is strongly desirable for most of SiC bipolar devices. Contact resistivity of such regions becomes a limiting factor for most types of SiC based power and microwave power devices (p-i-n diodes, IMPATT-diodes, microwave limiters, BJTs *etc.*).

Commonly used chemical vapor deposition (CVD) technique is not able to provide aluminum atomic doping concentration sufficient for reproducible fabrication of ohmic contacts with specific contact resistance lower than 10^{-4} Ω cm^2. Ion implantation can provide rather high Al atomic concentration, but the defects produced by implantation require post implantation high temperature anneal and can cause the additional problems for devices fabrication and operation.

In this paper we report on SiC doping with Al during liquid phase epitaxy (LPE) of thin (03-0.4 μm) 6H- and 4H-SiC layers for diode structures with a smooth mirror-like surface. Al doped 6H-SiC epitaxial layers were grown by LPE on the 6H-SiC (0001) 3.2° and 4H-SiC 8° off-axis substrates. We also grew p^+- 6H-SiC and p^+-4H-SiC layers on commercial p-n epitaxial structures. Growth was performed in a vertical dipping version of LPE reactor.

We achieved significant improvement of surface morphology for thin layers doped with Al by decreasing of growth temperature. Smooth layers with Al atomic concentration over 2×10^{20} sm^{-3} (as measured by secondary ion mass spectroscopy) were grown. Thickness of p+-layers was measured using scanning electron microscopy.

Ti-Al alloy was deposited to form ohmic contacts both by sputtering and e-beam evaporation. Test structures were formed for transmission line (TLM) resistivity measurements. Contact layers were annealed in vacuum at high temperature. TLM measurements show that reproducible Ohmic contacts with contact resistivity in low 10^{-5} Ω×cm^{2}range were fabricated. For the best contacts, 10^{-6} Ω×cm^2 level was achieved.

Highly doped p+-SiC layers were applied to fabricate SiC diodes with low on-state resistance. In this case p^+-SiC LPE layers were grown on the top of commercial pn epitaxial structures. Back contacts for diodes were formed by nickel evaporation and subsequent anneal in Ar flow. Diode mesa-structures of various sizes were formed by reactive ion etching in radio frequency glow discharge SF_6 plasma. We protected the top contacts against etching by the aligned Ni masks using lift-off lithography. To improve on-state resistivity of diodes back and topside contacts were enforced with gold. Resulted

in diodes show low on-state resistivity of ~8×10^{-4} $\Omega\times cm^2$. This value exceeds the level of contact resistivity to p-layers. The resistivity is possibly limited by the substrate and/or base n-layer resistance.

We may conclude that heavily aluminum doped p^+- SiC layers and resulted record low resistivity Ohmic contacts to p-type SiC have been demonstrated and implemented for diodes fabrication.

This work is supported by ONR (contract monitor John Zolper).

Abstract

submitted to THE INTERNATIONAL CONFERENCE ON SILICON CARBIDE AND RELATED MATERIALS 2001, October 28 - November 2, 2001
Tsukuba International Congress Center (Epochal Tsukuba), Japan

Homoepitaxial growth of 4H-SiC on porous substrate by chemical vapor deposition using bis-trimethylsilylmethane precursor

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Dislocations and micropipes in SiC wafers still limit the performance of SiC electronic devices such as MESFET, MOSFET and SBD. Therefore, it is prerequisite to reduce the dislocation in order to exploit high performance SiC electronic devices. Usage of porous silicon carbide (PSC) is one of the ways to reduce dislocations during epitaxial growth.

In this paper, 4H-SiC films were grown on 8° off-axis porous 4H-SiC (0001) by chemical vapor deposition using a single source material, bis-trimethylsilylmethane (BTMSM). The flow rate of the carrier gas H_2, which flows through liquid BTMSM source, and growth temperature were varied from 10 to 30 sccm and from 820 to 1390℃, respectively. The grown films were examined by atomic force microscopy (AFM), scanning electron microscopy (SEM), electron back scattering diffraction (EBSD), high resolution x-ray diffractometry (HRXRD) and transmission electron microscopy (TEM). The roughness of as-received substrate (1.2nm) was improved to 0.5 nm by hydrogen etching for 10 min at 1500℃. As the growth temperature and the flow rate of source material, BTMSM, increase, the rms roughness of the thin film was decreased, indicating that the growth follows the so-called step-controlled epitaxy model. It was found that the flow rate of source material,

BTMSM is critical growth parameter to polytype formation of thin film. At higher flow rate (>20sccm), parasitic 3C-SiC polytype was included in the grown film. The (111) Bragg spot position of 3C-SiC on PSC is displaced by 1.2×10^{-3} nm^{-1} along the Q_z-axis with respect to the (0004) Bragg spot position of 4H-SiC in reciprocal space, while the (111) Bragg spot position of 3C-SiC on the standard 8° off-axis 4H-SiC substrate is displaced by 3.4×10^{-3} nm^{-1}. The result suggests that 3C-SiC on PSC is more strained than that on standard substrate. This difference might be ascribed to the porosity of the substrate. However, at low flow rate (10sccm), homoepitaxial 4H-SiC films without parasitic 3C-SiC was grown. Although the FWHM of (0004) Bragg spot of the epilayer grown below 990℃ is larger than that of substrate, FWHM of thin films above 1200℃ is smaller than that of substrate. Monocrystalline 4H-SiC films were grown even at the extremely low temperature of 820℃. At optimum growth condition, the density of dislocation in the epilayer was reduced compared to that of typical commercial substrate.

Acknowledgement

This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea.

Keyword : PSC; 4H-SiC; Homoepitaxy; OMCVD

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SiO_2 as oxygen source for the chemical vapor transport of SiC

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Recently, the sublimation epitaxy method has attracted attention in order to grow thick homoepitaxial SiC layers at low cost. This technique is a simple transposition to lower temperatures of the modify Lely-process used for SiC boules. However, in most cases the temperature is higher than 1800°C [1,2]. Reduction of the growth temperature could help solving some problems such as thermal stress, defect generation or graphitisation of the source. However, the lowering of the temperature is critical for the growth rate because of the low sublimation rate of SiC. The addition of a chemical agent X in the growth chamber could assist the vaporization of SiC by forming SiX and CX gaseous species. In this case, the method should be called Chemical Vapor Transport (CVT).

In a first step, a thermodynamics study based on the total Gibbs free energy minimization was performed in order to evaluate the potential of oxygen as a transporting agent for SiC. The temperature ranged from 1500 K to 2200 K and isochore conditions were used. After fixing the initial Si, C and O contents, the equilibrium partial pressures were calculated at one temperature and inserted again for calculation at a different (lower or higher) temperature to simulate a thermal gradient. SiO and CO were found to be the main gaseous species forming. It is shown that SiC can be transported on a wide range of initial reactant content or temperatures without the co-formation of SiO_2, Si or C.

In a second step, the CVT of SiC was carried out in a sublimation like graphite reactor with an internal thermal gradient of 7 K/mm. The SiC seeds were 8° off oriented (0001) 4H-SiC substrates. The use of SiO_2 powder as the oxygen source is advantageous on many points : 1) it is easy to handle; 2) it can be introduced in the reactor in a precise amount; 3) the intimate mixing of both SiC and SiO_2 powders ensures an effective interaction of oxygen with the SiC source.

CVT experiments with SiO_2 addition to the source were compared to pure sublimation experiments performed with identical argon pressure and temperature. It was found that the addition of SiO_2 in the source enlarges the conditions of pressure and temperature for the SiC epitaxial growth. Indeed, epilayers could be grown at lower temperature or higher pressure than the ones required for sublimation epitaxy. It was also observed that, when SiO_2 was added, the SiC powder never showed any evidence of graphitisation after experiment. The effect of the SiC/SiO_2 molar ratio in the source has been studied in order to optimize the growth conditions and the quality of the epilayers.

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Surface Morphology of SiC Epitaxial Layers Grown by Vertical Hot Wall Type CVD

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Control of the surface morphologies of SiC epitaxial films is important for electronic device fabrication, particularly for high-frequency applications.[1] In this study, we investigate the surface morphology of epitaxial layers etched in the hydrogen annealing under the several conditions.

The vertical hot wall type CVD system was used to grow the epitaxial layers of SiC in this study.[2] The growth temperature and pressure were 1600°C and 90kPa, respectively. The flow rate of H_2 carrier gas was 2slm. The flow rates of SiH_4 and C_3H_8 were 3sccm and 2sccm, respectively. The surface morphologies of epitaxial layers were minutely evaluated by laser microscopy and atomic force microscopy (AFM). The epitaxial layers on the 6H- and 4H-SiC(0001)Si substrates with 3.5° and 8° off-angles, respectively, resulted in the formation of the macro-steps. Size of the steps was observed as 600-1300nm in width and 10-30nm in height on the 6H-SiC. The terrace width (700-2000nm) and step height (10-50nm) on 4H-SiC were larger than those on 6H-SiC.

The epitaxial films with macro-steps on 6H- and 4H-SiC were etched in the atmosphere of hydrogen. The etching experiments were performed in the CVD system described above. The substrate temperature, H_2-flow rate, and H_2 pressure were varied within 1400-1600°C, 0.5-2.0slm, and 3-90kPa, respectively. The etching rates were varied from 0.5μm/h to 30μm/h with the etching conditions. It is confirmed that the etching rate increases with increasing substrate temperature and H_2-flow rate, and is varied inversely with the pressure.

After etching in H_2 at the pressure of 90kPa, it is observed that the surface morphologies keep the same with macro-steps mentioned above. Under atmospheric pressure, it is considered that the etching reactions mainly occur on the terraces of the macro-steps, so that the width of wide terrace becomes wider as the reactions proceed. In low-pressure H_2 atmosphere, it is clarified that the step height is drastically reduced after hydrogen etching. After 30min. etching at 1500°C under the pressure of 6kPa, the average surface roughness of 6H- and 4H-SiC measured by AFM become 3nm and 5nm, respectively. There are little effects of substrate temperature and H_2-flow rate to the surface morphologies. These results suggest that the low-pressure H_2 atmosphere accelerates the etching reactions on the kink of the bunched terraces to reduce the step height and to proceed the effective flattening of the bunched surfaces.

In conclusion, the surface morphology of SiC epitaxial layers etched by hydrogen annealing has been investigated by laser microscopy and AFM. The step height of the bunched surfaces of epitaxial layers drastically reduces after hydrogen etching at low-pressure atmosphere.

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In situ RHEED analysis of the Ge induced surface reconstructions on 6H-SiC(0001)

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Germanium has attracted an interest in the SiC technology. Three fields of applications are in the focus of research. Firstly, Ge can be used to improve the heteroepitaxial growth of SiC on Si [1,2]. Secondly, Ge can act as a surfactant during the epitaxy of SiC [3] and more recently the formation of of germanium nanocrystals as potential candidates for optoelectronic application have been studied [4]. For all this application it is important to have a detailed knowledge about the structural evolution during early stages of Ge deposition to control the surface structure and composition, but only few reports are available on Ge induced surface structure [4]. In this paper, real time in situ reflection high energy electron diffraction (RHEED) studies of the surface structure evolution during Ge deposition on differently prepared SiC(0001) surfaces will be presented.

Cree silicon face 6H-SiC (0001) 3.5° off-oriented towards [11 $\bar{2}$ 0] were used as substrates. The substrates were cleaned in situ in a hydrogen plasma and by heating in a Si flux to get definite reconstuctions of (3×3)-Si, (√3×√3)-Si and (√3×√3)-C. Subsequently, these well prepared surface reconstruction were subjected to a Ge flux of 0.003 ML s^{-1} with respect to the SiC surface. The deposited Ge amount was in the range between 0.1 and 8 ML. The investigations were carried out at substrate temperatures between 250°C and 900°C.
Independent on the prepared surface reconstruction we observed the formation of a Ge wetting layer. The thickness of these layers was in the range of 1 to 3 ML in dependence of the initial surface reconstrution and substrate temperature. These wetting layers were stable against cluster formation at substrate temperatures below 480°C and Ge coverages below approximately 0.7 ML on (3×3)-Si, 1.4 ML on (√3×√3)-Si and 1.7 ML (√3×√3)-C reconstructed surfaces.
The following possible transition schemes were observed:

(3×3)-Si reconstructed surface:	(3×3)-Si → (3×3)-Ge →(4×4)-Ge →cluster formation
(√3×√3)-Si reconstructed surface:	(√3×√3)-Si → (2×1) or (2×2)-Ge → (4×4)-Ge → cluster formation
(√3×√3)-C reconstructed surface:	(√3×√3)-C → (√3×√3)-Ge →(2×1) or (2×2)-Ge → (4×4)-Ge → cluster formation

A detailed analysis of the RHEED time dependent RHEED intensity behaviour will be presentd.

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In situ etching of 4H SiC in H_2 with addition of HCl for epitaxial CVD growth

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Introduction Good surface morphology of the epitaxial layers is a basic requirement for both the processing and the performance of the devices. To improve the surface morphology, one important factor is the substrate surface condition prior to the growth. Etching of the SiC substrate before the CVD growth in pure hydrogen or in hydrogen with addition of either a hydrocarbon or hydrogen chloride (HCl) has been used to improve the surface quality of the epilayers [1, 2]. In this paper we investigate the etching mechanism of 4H SiC in H_2 with addition of HCl and the role of HCl in the etching.

Experimental The in situ etching and the subsequent CVD growth runs were performed in a horizontal hot-wall reactor, similar to the one described in [3]. A SiC-coated graphite susceptor was used and the small substrate pieces were placed on a poly-SiC plate lying on the susceptor floor. A small amount of hydrogen chloride (< 0.03% in volume) together with the hydrogen carrier gas was introduced during the etching. Silane (SiH_4) and ethylene (C_2H_4) were used as precursors for the subsequent growth. A 4H SiC epilayer (8° off-oriented towards the <11 $\bar{2}$ 0> direction), was etched and the thickness was measured before and after etching using Fourier Transformed Infrared Spectrometry (FTIR), and the etch rate was thereby obtained. The surface morphology of the etched substrates was examined in an optical microscope with Normaski contrast. The surface roughness profiling was conducted using light interference with a WYKO instrument. KOH etch of the SiC surface was conducted at ~ 500 °C for 5 - 15 s.

Results As shown in Fig. 1, the etch rate increases rapidly with increasing temperature. The activation energy is above 110 kcal/mol at 20 mbar (open squares), and decreases to around 72 kcal/mol at 100 mbar (black squares). The high activation energy values suggest that the limiting mechanism for the etching may be related to either the carbon removal through the reaction with hydrogen or the Si evaporation process. The pressure also has an impact on the etch rate, as indicated in Fig. 2. The etch rate decreases steeply with increasing pressure below a pressure of 100 mbar. Above this pressure, the etch rate further decreases very slowly and almost levels off after 600 mbar. Without addition of HCl (closed circles in Fig. 2), the etch rate is considerably lower at low pressures, but only slightly reduced in the high pressure range.

Etching in hydrogen with addition of HCl under proper conditions has shown to significantly improve the subsequently grown epilayer morphology. As illustrated in Fig. 3a, the epilayer grown without pre-growth etch displays a large density of pit-like defects, whereas on the epilayers grown after etch (Fig. 3b) the amount of the pit-like defects has been reduced considerably, with only a few half-moon defects encountered on the surface. The KOH etching of these epilayers shows that the pit-like defects mainly originate from dislocations, whereas the half-moon defects do not display etch pits after the KOH etch.

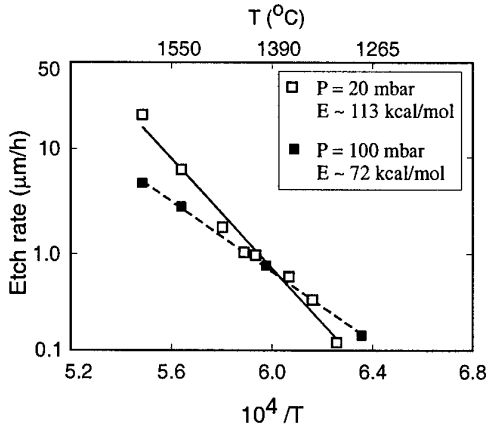


Fig. 1, Etch rate dependence on temperature at 20 mbar and 100 mbar, respectively, with 60 l/min H_2 flow and 20 ml/min HCl flow.

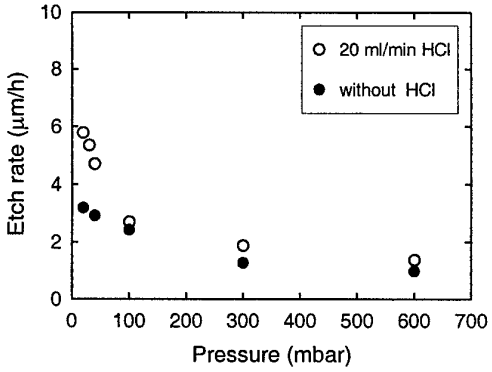
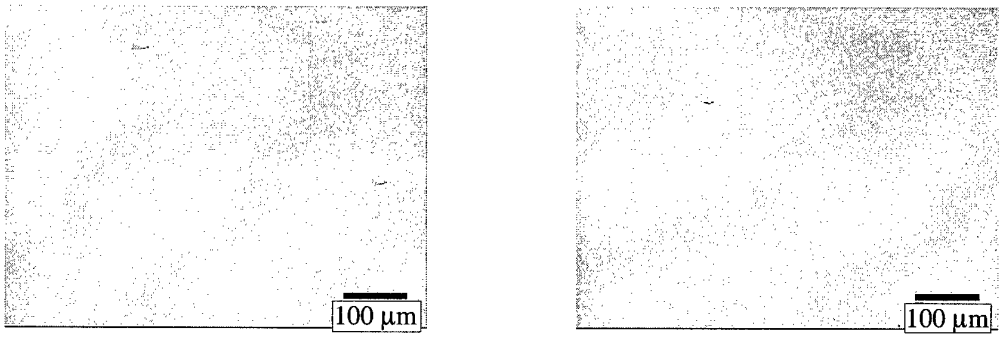


Fig. 2, Etch rate dependence on the pressure with 60 l/min H_2 flow at 1500 °C.



(a) (b)

Fig. 3, Normaski micrographs of: a) 17.5 µm epilayer grown for 3 h with no pre-growth etch; b). 9.5 µm epilayer grown for 2h after proper in situ etch in hydrogen with addition of HCl.

The surface roughness of the as-etched substrates has been measured systematically by the WYKO instrument. A too high etch temperature (> 1650 °C) is shown to give rise to rough surface, whereas a low etch pressure (around 40 mbar) results in very smooth surface.
To summarise, the pre-growth etching of SiC in hydrogen with addition of HCl has shown to effectively suppress the formation of dislocation related morphological defects after the epitaxial growth. The etch rate dependence on the etch parameters has been studied to understand the etching mechanism involving HCl.

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Fabrication of α-SiC hetero-epitaxial films by YAG-PLAD method

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I. Introduction

Silicon carbides (SiC), especially the high-temperature stable ones (such as 4H and 6H α-SiC) with hexagonal crystal structures are strongly expected to be the next-generation semiconductors, that are applicable for high power, high voltage, high temperature, and high frequency devices, since they have a wider band gap (3.0-3.2eV) than the low temperature type (β-SiC; 2.2eV), and have high melting point (m.p.>2400°C), large thermal conductivity, and large resistance for electric breakage. However, the high m.p. makes it difficult to prepare single crystals and needs complex processing for preparation of the devices, such as ion implantation and thermal annealing at high temperatures around 1600°C. Many trials were made for preparing SiC hetero-epitaxial films, however, they have failed except for β–SiC hetero-epitaxial growth by MBE techniques. Here we report the first preparation of hetero-epitaxial films of α–SiC at low temperatures around 1150°C by pulsed laser ablation-deposition (PLAD).

II. Experimental

The fabrication of α–SiC films have been studied by PLAD technique using the 4th harmonic of Nd:YAG laser (266nm). We tried the film growth using 6H α-SiC targets and seven kinds of single crystal substrates: Si(111), Si(110), Si(100), sapphire:Al_2O_3(0001), Mg(100), $SrTiO_3$(100), and LSAT(100). The epitaxial growth has occurred only on the Si(111) and sapphire(0001) planes.

III. Results and Discussions

Figures 1a, 1b, and 1c show the infrared absorption spectra of the films simultaneously fabricated on Si(111), Si(110), and Si(100) substrates in the following PLAD conditions: the substrate temperature =1150 °C, laser energy = 50 mJ/pulse, fluence = 5 J/cm^2/pulse, pulse frequency = 10 Hz, and vacuum pressure = 1x10^{-7} Pa. Every spectrum shows absorption of Si-C stretching vibration mode ν(Si-C) alone, unequivocally indicating formation of SiC thin films. The absorption frequency was 786±3 cm^{-1} for the film fabricated on Si(111). The X ray diffraction (XRD) pattern of the film is shown in Fig.2a. It is composed of SiC(0006) and SiC(00012) XRD lines expect for diffraction lines from the substrate, definitely indicating formation of c-axis oriented film of α-SiC on Si(111). On the other hand, the XRD patterns for other films prepared on Si(110) and Si(100) show XRD lines only from the substrates as shown in Figs.2b and 2c. These results along with those from the infrared spectra suggest formation of SiC polycrystalline films.

The crystallinity of the films was investigated by reflection high energy electron diffraction (RHEED). Figures 3a and 3b show RHEED images observed for the film fabricated on Si(111). Figure 3c is an image measured for film on Si(110), which did not change by rotation of the film. It is of Debye-Sherrer (ring-type) pattern, that is characteristic of polycrystalline samples. The film fabricated on Si(100) also gave essentially the same ring pattern. Thus it was confirmed that polycrystalline SiC films were formed on Si(110) and Si(100) planes, which have no C_6 symmetry (having C_2 and C_4). On the other hand, the film on Si(111) substrate shows symmetric streak patterns which is characteristic of epitaxial growth of α-SiC. Two spectra in

Figs. 3a and 3b are observed at the film-orientations that differ by 30° in each other and observed at an interval of 60°. This is evidence for the film having C_6 symmetry in the plane. The separation between streak lines is proportional to the reciprocal of the lattice constants. The ratio of the separations between the streak patterns in Fig.3a and Fig.3b was ~1.76±0.05, which agrees with the value of $3^{1/2}$ = 1.73 expected for the lattice with C_6 symmetry. These results along with those from XRD strongly indicate that the epitaxial film of α-SiC having hexagonal structure is fabricated on Si(111), rather than β-SiC with cubic structure. The lattice parameters of the film were estimated to be a = 3.09±0.04, c = 15.08 ±0.01Å from the RHEED and XRD measurements, in good agreement with the reported values for 6H α-SiC (3.07 and 15.08 Å). The IR absorption frequency ν(Si-C) =786±3 cm^{-1} observed for film prepared on Si(111) agrees with the reported value for α-SiC (789 cm^{-1}) rather than β-SiC (798 cm^{-1}), supporting the assignment to α-SiC film.

The epitaxial growth of SiC occurred only on Si(111) and Al_2O_3(0001) which have the same C_6 symmetry as α-SiC, implying that symmetry matching is an important factor for the growth. The present success of low-temperature preparation of α-SiC film by PLAD may provide a new device processing for production of p and n-type semiconductors.

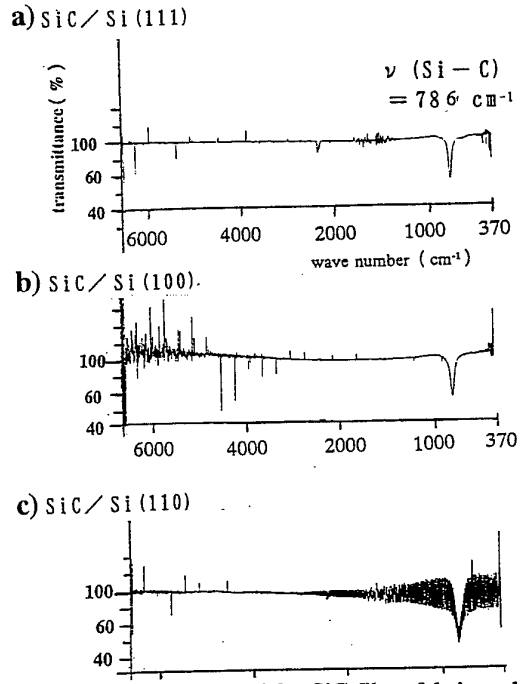


Fig.1 IR spectra observed for SiC films fabricated on Si(111), Si(100) and Si(110) substrates.

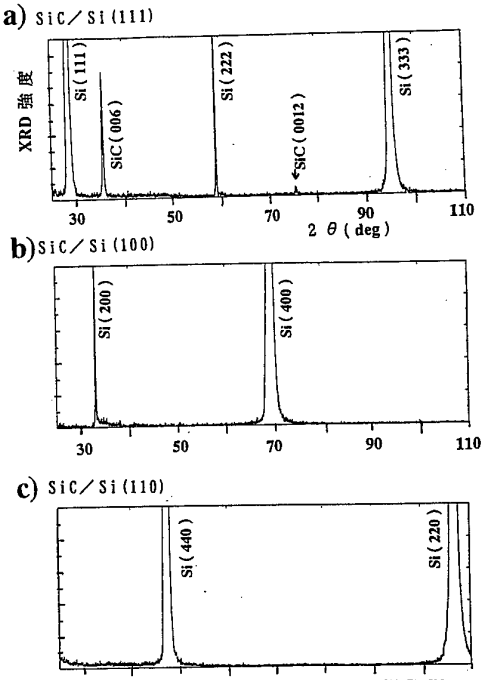


Fig.2 XRD patterns observed for SiC films on Si(111), Si(100) and Si(110) substrates.



Fig.3 RHEED images observed at <10$\bar{1}$0>(a) and <21$\bar{3}$0>(b) film-orientations for the SiC film fabricated on Si(111) and image (c) for the film prepared on a Si (110) substrate.

Comparativ Study of heteroepitxialy and homoepitaxialy Grown 3C-SiC Films

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Cubic silicon carbide (3C-SiC) is a promising candidate to overcome the device limit due to intrinsic silicon properties in the fields of, high power devices, high temperature devices and high radiation tolerant devices. Moreover, it may be a suitable substrate for the growth of cubic Ⅳ-nitrides. However, 3C-SiC crystals are not commercialy available now. It is important to develop higher device grade 3C-SiC crystals for the realization of 3C-SiC devices.

This paper presents the results of two growth processes of 3C-SiC epilayers, heteroepitaxial growth of 3C-SiC on Si (100) substrates and homoepitaxial growth on 3C-SiC substrates. The heteroepitaxial growth was carried out by low pressure CVD method using a vertical cold wall quartz reactor with two zone RF induction heating systems. Silicon (001) on-axis wafers, 50 mm square were used as substrates. Typical heteroepitaxial growth conditions were as follows; growth temperature: ~1250℃, growth pressure: 30 Torr, H_2 carrier gas flow rate: 8 slm, SiH_4 gas flow rate: 0.8 sccm, and C_3H_8 gas flow rate: 0.4 sccm. The growth rates were around 2 μm/hr. After 50 hours growth, the silicon substrates were etched off using HF+HNO_3 solution to fabricate free standing 3C-SiC films of 100 μm in thickness. These 3C-SiC thick films were used as substrates for the homoepitaxial growth. The homoepitaxial growth was performed by low pressure CVD method using another vertical cold wall quartz reactor, under the conditions; the growth temperature: 1530℃, the growth pressure: 47 Torr, and H_2, SiH_4, C_3H_8 reaction gas flow rates: 10slm, 30 sccm, 8 sccm, respectively . The growth rate were around 10 μm/hr. 1) The surface morphologies of these epilayers were observed using a Nomalski optical microscope and an AFM. The crystalinity of these epilayers were evaluated by XRD and PL spectroscopy.

The morphologies of the grown surfaces of the heteroepitaxial layers were rough , because of the formation of macro steps and protrusions caused by stacking fault. 2) as shown in Figure 1. While, the surface morphology of the back side of heteroepitaxial layers (interface with Si substrates) were very smooth as same as those of Si substrates. From this reason, we used the back side surface of the heteroepilayer as these substrates for the homoepitaxial growth, though the crystalinity was not so good compared with that of the grown surfaces. The typical values of the FWHM of XRD-ω scan rocking carve of the substrates were around 1200 arcsec.. After homoepitaxial growth of ~100 μm in thickness,

the FWHM reduced to around 150 arcsec. The surface of the homoepilayers were fairly smooth as shown in Fig. 2. The AFM image of the surfaces is shown in Fig.3. Step bunchings, the hight of which are 1~2 nm, can be seen in this figure, and the root mean square of the surface roughness were around 0.4 nm (10 μm X 10 μm). Figure. 4 shows the PL spectra of the homoepitaxial layer. A free exciton peak of 3C-SiC and N dopant originated peaks can be seen. The free exciton peak was not observed for the heteroepilayers. The improvements in the crystalinity, the surface morphology and the luminescent properties suggest the possibility of the growth of 3C-SiC crystals good for the device fabrications.

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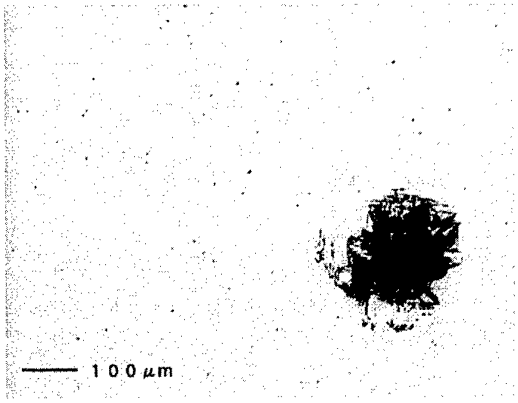


Fig. 1 Nomalski microscope image of a heteroepilayer surface.

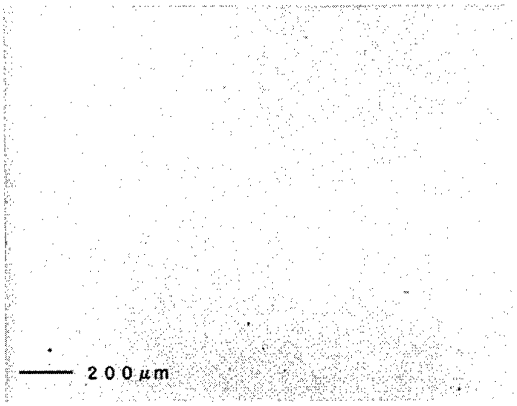


Fig. 2 Nomalski microscope image of a homoepilayer surface.

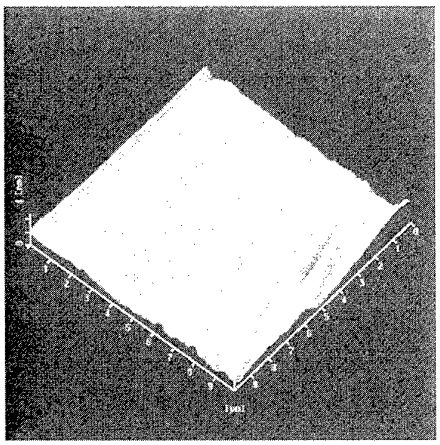


Fig.3 AFM image of a homoepilayer surface.

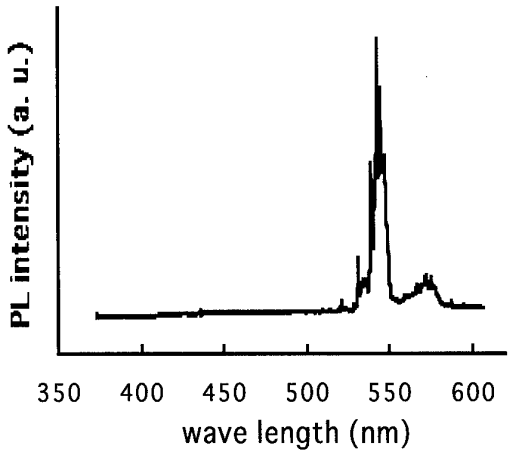


Fig. 4 Photoluminescence spectrum from a homoepilayer

In Situ Doping of 3C-SiC Grown on (0001) Sapphire Substrates by LPCVD*

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3C-SiC is a promising semiconductor material for high temperature and/or high power devices. The growth of 3C-SiC on sapphire or AlN substrates is quite interesting from the point view of semiconductor-on-insulator (SOI) structures. For most high-power applications, an insulating or semi-insulating substrate supporting the device is necessary to reduce parasitic effects and to increase the maximum power capabilities of the device. On the other hand, it is important to control impurity incorporation into epilayers for device applications. In this paper, we report the *in situ* doping of 3C-SiC grown on C-face (0001) sapphire substrates by LPCVD.

The heteroepitaxial growth of SiC on sapphire substrates has been performed with a supply of SiH_4, C_2H_4, and H_2 at a pressure of 200 Torr. The nitrogen and boron incorporation was accomplished by introducing ammonia (NH_3) and diborane (B_2H_6) precursors, respectively, into gas mixtures. The undoped and nitrogen-doped 3C-SiC epilayers were grown on the nitridized sapphires, which were formed by supplying NH_3 to the heated sapphire substrate at temperature of 1100 °C for 10 minutes. The boron-doped 3C-SiC epilayers were grown on pure sapphire substrates. Surface morphologies were characterized by Nomarski differential interference contrast optical microscopy and scanning electron microscope (SEM).

Crystallinity of SiC on (0001) sapphire substrates was characterized using x-ray diffraction (XRD). X-ray diffraction measurements of undoped and nitrogen-doped SiC samples (shown in Fig. 1) show the presence of SiC (111) and (222) peaks at 2θ=35.6° and 75.4°, respectively. The absence of any other reflections corroborates that the SiC film is epitaxial and cubic (3C-) form mono-crystalline as reported previously. X-ray rocking curve data confirmed the crystalline nature of as-grown 3C-SiC films.

The incorporation of nitrogen and boron into grown 3C-SiC epilayers was measured by Auger electron microscopy (AES) and secondary-ion mass spectroscopy (SIMS). Fig. 2 shows that the nitrogen concentration for the samples made at 1400 °C with a NH_3 gas flow rate of 1 SCCM increased from 2% to 15% with increasing the Si/C ratio from 0.33 to 0.5. The carbon concentration decreased from about 35% to 24%, while the silicon concentration kept the same (about 60%). This result indicates that nitrogen substitutes for carbon in the SiC lattice and the nitrogen dopant concentration incorporated into the 3C-SiC epilayers increased by increasing the Si/C ratio.

Preliminary Hall measurements were made at room temperature on undoped, nitrogen-doped and boron-doped samples using the van der Pauw technique. Undoped

and nitrogen-doped 3C-SiC epilayers were n-type conduction, and boron-doped epilayers were p-type and probably heavily compensated. Three undoped 3C-SiC samples showed n-type electrical conductivity with mobilities of approximately 2-7 cm^2/Vs and (N_d-N_a) of 1.3×10^{18}~4.7×10^{18} cm^{-3}. Four nitrogen-doped 3C-SiC samples yielded values of 0.021Ωcm to 0.0014 Ωcm for resistivity, 2-5 cm^2/Vs for the electron mobilities, and 2.5×10^{20} cm^{-3} to 2.7×10^{21} cm^{-3} for the electron carrier concentration. Four boron-doped 3C-SiC samples grown with diborane gas flow rate varied from 1.25 SCCM to 5 SCCM yielded values of 580 Ωcm to 7.7 Ωcm for resistivity, 1.7×10^{16} cm^{-3} to 1.3×10^{17} cm^{-3} for hole carrier concentration, and 3.1 to 7.7 cm^2/Vs for hole mobility.

* This work was supported by National Natural Science Foundation and Special Funds for Major State Basic Research Project G20000683.

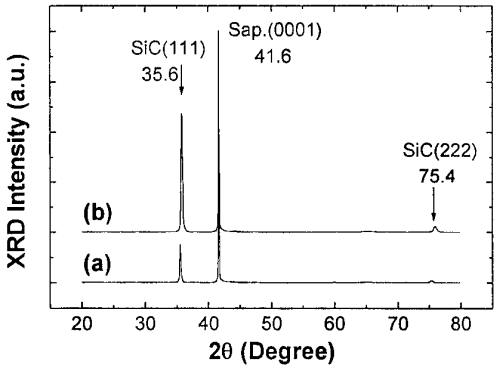


Fig. 1 X-ray diffraction patterns for (a) undoped and (b) nitrogen-doped 3C-SiC epilayers.

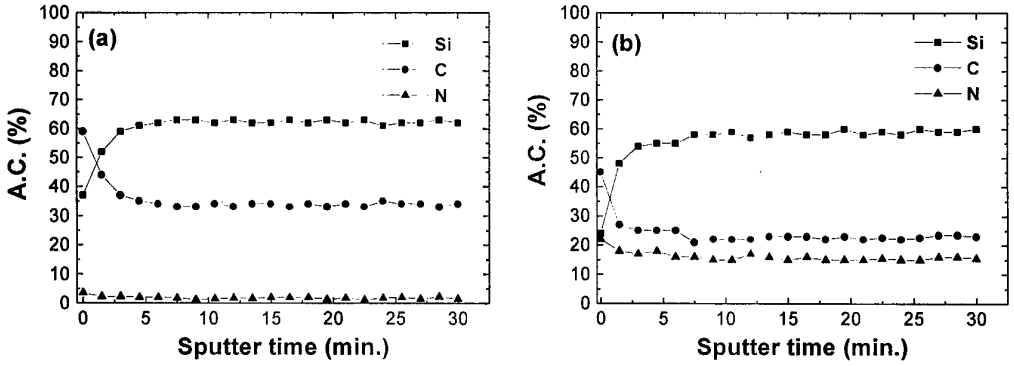


Fig. 2 Auger depth profile for N-doped 3C-SiC epilayers grown on nitridized sapphire substrates at 1400 °C with a Si/C ratio of (a) 0.33 and (b) 0.5. The ammonia gas flow rate was 1 SCCM.

SILICON CARBIDE BUFFER LAYERS FOR NITRIDE GROWTH ON Si

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Group III-nitride is one of the best candidate for UV laser-diodes and LEDs. Gallium nitride-based opto-electronic devices may possess high emission efficiency because of its electronic properties. In order to obtain high quality GaN crystalline films, the problem of finding an optimized substrate material must be solved. One possibility is to use sapphire with buffer layers because of the large lattice mismatch and thermal expansion mismatch between wurtzite GaN and sapphire. The reduction/annihilation of structural defects in GaN overlayers used as active layers is indeed a vital problem for device applications. The low lattice mismatch between SiC and GaN (~3 %) makes SiC a suitable substrate for GaN growth. However, this strategy is facing the problem of high cost of SiC wafers.

Among the different techniques which can smooth out the effect of host materials large lattice mismatch, the buffer layer technique has been widely used to assist heteroepitaxial growth. Thus one useful task is to use Si as substrate with SiC buffer layer. Large area Si wafers are indeed available with many advantages such as large area low cost, high surface quality and high conductivity. This option would also provide a route towards the integration of the group III-nitride technology into the silicon technology for which well-established processing methods exist.

However, when using this methodology, an important problem related to the lowering of residual stress existing at the SiC/Si interface must be solved since the crystalline quality of the SiC/Si interface and of the surface of the SiC buffer layer is a necessary condition to obtain GaN layers free of structural defects.

The carbonization of Si-substrate surfaces performed to grow SiC overlayers on Si generally introduces stresses at the SiC/Si interface because of host material physical properties differences: SiC and Si present indeed a disadvantage due to the large mismatches of their lattice constants and their thermal expansion coefficients respectively equal to 20 % and 8 %. Because of these mismatches and beyond layer critical thickness, extended defects, like for instance dislocations, can be favored from the formation energy point of view. However, these extended defects can not fully relax stresses introduced at the SiC/Si interface. The carbonization of clean Si surface using hydrocarbon radicals is generally performed at the early stage of the growth process. Gas source molecular beam epitaxy (GSMBE) experiments have shown that when one uses $(CH_3)_2GeH_2$ (DMGe) as carbon source, the morphology of the carbonized surface layer improves when compared with the one without Ge (carbon is then provided by hydrocarbon radicals from cracked $-C_3H_8$). The thickness of the smooth carbonized layer is ~ 40 Å with a Ge concentration showing a saturation around 0.4 % , and the purpose of using DMGe is to introduce a large size atom at the heterointerface.

In this work, our objective is to propose a strategy for the optimization of the SiC/Si structure as a subsequent substrate to grow high quality GaN layers. Several routes are investigated

within the framework of a theoretical approach which we have recently developped and which has prooved itself to be very useful in many aspects of the physics of heteroepitaxy. This approach is based upon the elasticity theory of strained interfaces which are thus analyzed in terms of their elastic and structural properties. It can predict the formation of stable phases induced by epitaxial strains as well as their composition and also can allow the evaluation of buffer layers for optimized heteroepitaxial growth needs. By constraining a material to grow on a substrate structure, effective stress, which acts as a phase-stabilizing factor, is induced in the hetero-system. However, we indeed know from X-ray and electron microscopy studies that the morphology of multiphase crystals can not be understood only on the basis of classic thermodynamics of phase transformations which involve bulk chemical free energy and interface energy terms. The effect of strain elastic energy due to host materials lattice mismatch is relevant too. One of the methods we consider relies on the effect of the incorporation of group IV atoms into the 3C-SiC/Si structure. This incorporation aims at elaborating an alloy-like buffer layer which has the property of improving the matching of SiC and Si host material lattices. The parameters involved in the theory are the elastic constant c_{ij}, the lattice constant a and the density ρ associated with each host material. The importance of these parameters in investigating the physics of epitaxially strained interfaces is recognized from Hooke's law which states that the resulting strain is directly proportional to the stress magnitude, i.e. to the magnitude of the force acting on a unit area in the solid. This provides a strain-dynamics relationship implying buffer layer composition-dependent parameters. Thus by optimizing this composition, we can provide a theoretical basis for further growth investigations on the GaN/SiC/Si system based on the buffer layer technique.

In-situ etching of SiC wafers in a CVD system using oxygen as the source

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Quality of a SiC epitaxial layer depends to a great extent on the quality of substrate surface. Hydrogen etching at the growth temperature is the conventional method used for removing scratches on the commercially available substrates. However, Si droplets usually form on the surface. Formation of droplets can be inhibited by adding a small amount of C_3H_8 in the H_2 flow. However, addition of C_3H_8 reduces the etching rate considerably. HCl gas phase etching is another method used to pre-etch SiC prior to epitaxial growth, but it is preferable to avoid the use of HCl in a CVD system. We have investigated a new method to etch SiC by adding a small amount of oxygen in the hydrogen flow to overcome the above problems. Etching experiments under various temperatures and oxygen flow rates are performed. The etched surfaces are examined by optical microscope, AFM and XPS.

Etching was performed in a horizontal water-cooled cold-wall CVD reactor. High purity oxygen diluted in Argon was used as the source, in addition to hydrogen as the bulk of carrier flow. The substrates used were (0001) Si-face, 3.5°-off 6H-SiC from Cree Research, Inc. Etching was carried out for 30 minutes at 100torr and at a temperature in the range from 1500 to1600°C with different flow rates of oxygen.

First, etch rate was measured at different temperatures and oxygen flow rates. The result shows that at a certain temperature, etch rate first increases rapidly (liner region) and then saturates with the increase of oxygen flow. When observed under the optical microscope, samples etched using a low oxygen flow (linear region) show a smooth and featureless surface, and samples etched under the saturation region show very poor morphology. The oxygen flow and the etch rate required for getting the rough surface increases with the etching temperature. Etch rate as high as 8μm/hr was obtained.

High-resolution XPS spectra from Si2p for etched samples were obtained. They can be fitted with four Gaussian peaks which are assigned to Si (99.2eV), SiC (100.4eV), SiO_x ($x<2$) (101.7), and SiO_2 (103eV). The fraction of each compound was calculated by determining the ratio of peak area. The result shows that SiO_2 on the surface increases while Si decreases with the increase of oxygen level in the system during etching. We believe that the saturation of etching rate and the rough surface obtained at higher oxygen concentration are the direct result of the formation of SiO_2 on the surface.

AFM on sample etched with pure hydrogen shows lots of sub-micron size white dots probably caused by Si droplets. They can be removed by dipping the sample into hot HF/HNO_3 solution for a few minutes. No white-dots can be seen on all H_2/O_2 etched samples. AFM also reveals the appearance of micro step bunching. The width and height of step increase with the increase of oxygen used during the etching. Excellent surface was obtained when epitaxial growth was carried out on this oxygen-etched surface.

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In-situ etching of SiC wafers in a CVD system using oxygen as the source (*continued*)

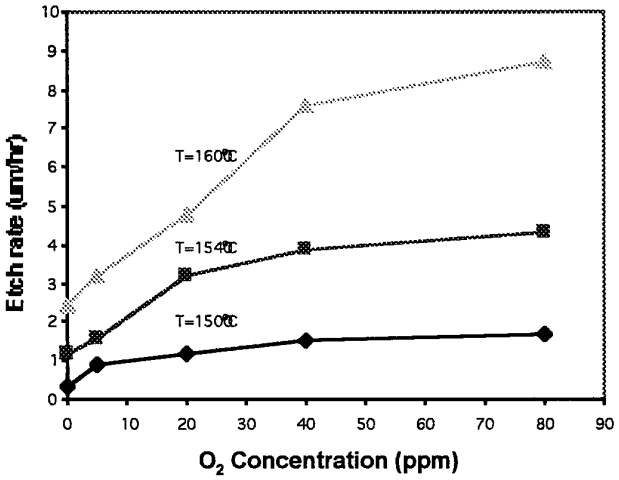


Fig. 1. Dependence of etch rate on O2 concentration at different temperatures

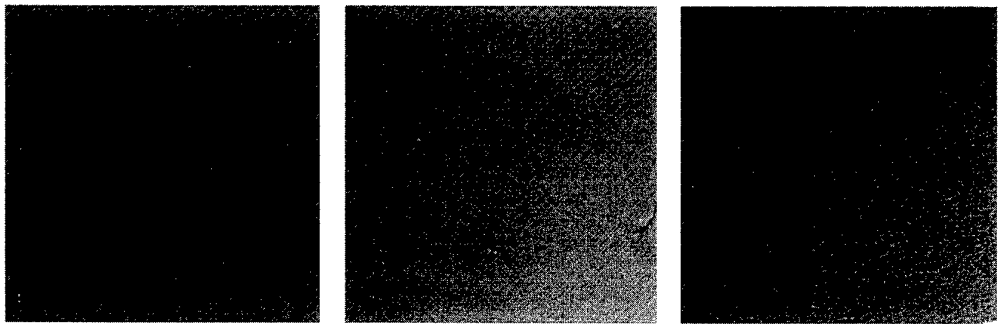


Fig. 2. Optical micrographs of SiC samples etched at 1540°C with 20ppm, 40ppm, and 80ppm of O_2, respectively

Improvement of the SiCOI structures elaborated by heteroepitaxy of 3C-SiC on SOI

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Silicon on Insulator (SOI) is a promising candidate to replace bulk Si for the hetero-epitaxial growth of 3C-SiC/Si. Large strain reduction in the 3C-SiC layer and improvement in the electrical insulation are expected [1]. However, large cavities in the buried oxide (BOX) have been observed after SiC deposition, resulting in the deterioration of the electrical properties. Increasing the deposition temperature or decreasing the silicon overlayer (SOL) thickness increased the size and density of the cavities [2, 3]. The origin of this phenomenon is not yet established, even if some initial defects in the SOI or thermal instability of the oxide were proposed.

In this work, we demonstrate improvement of the available SICOI (SiC On Insulator) structures by using new generations of UNIBOND substrates from SOITEC. Experiments have been carried out in a conventional vertical cold wall AP-CVD reactor with SiH_4 and C_3H_8 as reactants and H_2 as vector gas. Standard growth conditions were used: carbonisation at 1150°C with subsequent epitaxial growth at 1350°C. Three types of <100>-UNIBOND substrates with different SOL/BOX thickness were used : A) 205/200 nm; B) 75/50 nm; C) 85/18 nm.

After growing 3 μm thick SiC layers, all samples showed good surface morphology and crystalline quality very similar to that of comparative layers grown on bare Si substrates. No buckling of the layers was observed even for the thinnest SOI structure (sample C). From infrared reflectivity spectra and TEM observations, no deviation could be found for the SOL and BOX thickness as compared with the nominal UNIBOND values (table 1). No large cavity could be detected by optical microscopy, even at the highest magnification used (x1000). Only small cavities, with diameter ranging from 100 to 250 nm, could be found from TEM observations (figure 1). Estimated surface proportion of these holes at the SiC/SOI interface was only 0.03%, which is by far the lowest value ever reported. Balling up of the silicon around the cavities was also observed, suggesting bridges between the SiC layer and the substrate.

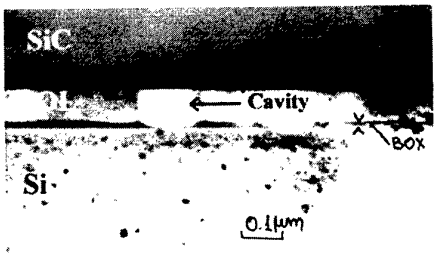


Figure 1 :TEM cross section of sample C

Table 1 : Physical parameters of the SiCOI structures

	Nominal SOI parameters	TEM data	IR data	IR Interface roughness (nm)	Cavity mean size (nm)	Density of cavities (cm^{-2})	Dislocation density in the SiC layer (cm^{-2})
Sample A							
3C-SiC (μm)	3.0	2.80	2.67	70	250	10^6	5.10^9
SOL/BOX (nm)	205/200	208/198	185/176				
SOL/BOX ratio	1.02	1.05	1.05				
Sample B							
3C-SiC (μm)	3.0	2.95	2.675	57	100	2.10^5	6.10^9
SOL/BOX (nm)	75/50	68/48	67.8/47.9				
SOL/BOX ratio	1.5	1.41	1.41				
Sample C							
3C-SiC (μm)	3.0	3.24	2.690	≈ 0	250	6.10^5	10^9
SOL/BOX (nm)	85/18	78/16	60.0/17.1				
SOL/BOX ratio	4.72	4.87	3.5				

The cavity density calculated from the TEM observations (about 10^5 cm^{-2}) is several orders of magnitude higher than the defect density in the SOI before heteroepitaxy. So, these holes cannot be related to the defect density of the SOI samples. The mechanism of formation of the cavities should be related to the high temperatures involved in the growth. The cooling stage may also be critical as the 3 μm thick SiC change the rigidity of the structure above the BOX so that the thermal mismatch changes. As SiO_2 is quite mobile at the deposition temperature, any strain imposed to the whole SOI structure can affect preferentially the BOX. One can also think to the following reaction occurring at the Si/SiO_2 interfaces : $SiO_{2(s)} + Si_{(s)} = 2\ SiO_{(g)}$. This reaction releases gas which can explain the ball like shape of the cavities. However, figure 1 shows that the quantity of oxide consumed to form a cavity is lower than the quantity of consumed Si. We believe that silicon out-diffusion at the SiC/Si interface is also probably occurring as this phenomenon is very difficult to avoid completely at the early stage of growth.

From table 1, one can see that the thinning of the SOL and/or BOX does not affect strongly the structural properties of the SICOI structure. However, the interface roughness, as calculated from IR spectra fitting, seems to decrease when the BOX gets thinner and/or when the SOL/BOX ratio increases. This roughness is not due to any inhomogeneity of the starting material as confirmed by TEM observations over several millimeters.

AFM, photolominescence and electrical characterizations are under progress in order to have a deeper evaluation of the benefit given by the use of this new generation of UNIBOND samples.

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Formation mechanism of interfacial voids in the growth of SiC films on Si substrates

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SiC/Si structures have been successfully used to fabricate microelectromechnical system (MEMS) such as microsensors and microactuators working at the temperatures above 200 ℃ and potentials above several tens of voltages [1,2]. However, crystal defects formed at the interface of the 3C-SiC/Si structures significantly influenced the crystal quality of the over-grown 3C-SiC films. Several research groups have discussed the way to improve the SiC/Si interface and the mechanism of void formation in the growth of SiC films on Si up to recently. However, most of the mechanisms have not clearly explained how the void formation initiates in the SiC growth. Therefore, the mechanism of void formation is still open to debate.

In this work, we measured the shape of voids formed during the growth of SiC film on different orientations of Si substrates and studied the origin of the voids. SiC films were grown on both p-Si(100) and (111) wafers using a single source tetramethysilane ($Si(CH_3)_4$, TMS) in a homemade RF-inductive chemical vapor deposition (CVD) system [3]. XRD measurements showed that the orientation of the grown SiC films followed that of the employed Si substrate. The cross-sectional SEM images (Fig. 1) shows that, in the silicon side of SiC/Si interface, reverse-triangle shaped voids were observed for the growth of SiC(100) on Si(100), whereas trapezoid shaped voids for the growth of SiC(111) on Si(111). Figure 2 shows SEM images for the initially etched Si(100) and Si(111) surfaces . The etched Si(100) uniformly produces rectangular shaped etch pits cross the wafer surface, whereas triangle shaped etch pits evenly appear from the etched Si(111) surface. This indicates that the shape of voids is mostly determined at the initial stage of the growth of SiC depending on the surface orientation of the Si substrate.

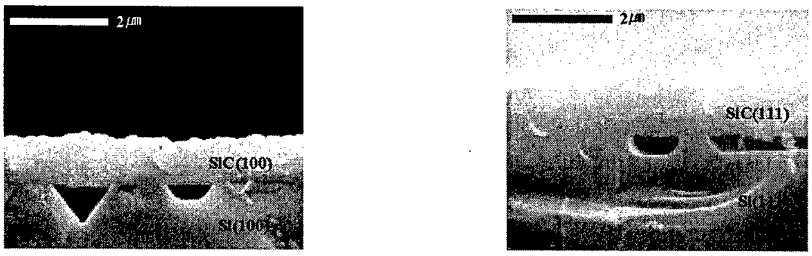
In conclusion, the mechanistic study revealed that the voids seems to be the oxygen-relative defects inherently existing in bulk Si wafers. The shape of the voids was determined by that of etch pit initially formed during the hydrogen etching process, which depends on the orientation of the silicon substrate. The mechanism of the void formation in the growth of SiC orientation of the silicon substrate.

Acknowledgements

This work was supported by KRF Grant (KRF-99-005-D00036) through the Semiconductor Physics Research Center at Chonbuk National University.

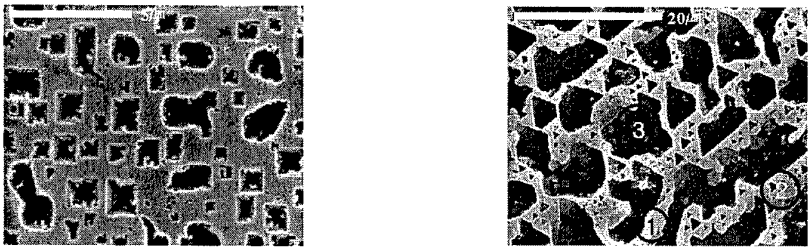
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(a) (b)

Figure 1. Cross-sectional SEM photographs for (a) SiC(100)/Si(100) and (b) SiC(111)/Si(111) structures. The growth was carried out for 60 min at 1250℃ and 50 torr with TMS/H_2 = 1.0/1000 sccm.



(a) (b)

Figure 2. SEM plane views for Si surfaces after removing SiC films from SiC/Si structure. (a) Si (100) and (b) Si (111).



(a) (b)

Figure 3. SEM plane views for the surfaces of (a) Si(100) and (b) Si(111) etched with 1000 sccm H_2 for 5 min at 1100℃.

Evaluation of Carbonized Layers for 3C-SiC/Si Epitaxial Growth by Ellipsometry

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Heteroepitaxial growth of 3C-SiC on Si substrate has been a promising method for obtaining large area 3C-SiC. Success in carbonization process has been important for continuous growing process. The reproducible carbonized layers were obtain, by holding the temperature of the Si substrate at the range of hydrogen desorption temperature, prior to carbonization [1]. In this work, to reproducibly obtain the single-crystalline 3C-SiC on (100)Si, carbonization process has been paid careful attention and carbonized layers were investigated by Ellipsometry. The heating-up of the Si substrate was examined in three different ways as shown in Fig. 1 and experimental procedures were showed in detail in previous work [1]. The substrate temperature at 600 °C in Type II and Type III were held for 5 min and 15 min respectively. The reproducible carbonized layers were obtained by using Type II and Type III , while were not obtain by using Type I as showed in previous work [1]. Fig. 2 shows changes in measured Δ and Ψ values by the ellipsometer and results of RED patterns of carbonized layers by using Type II and Type III. Prior to carbonization, Si surfaces are covered with amorphous carbon films at 600 °C and the carbonized layers are crystallized by out-diffusion of Si atoms at the carbonization temperature of 1000 °C and Si surfaces are covered by single-crystalline 3C-SiC carbonized layers. When Si surfaces are covered by single-crystalline 3C-SiC carbonized layer, Graphite layers are formed on 3C-SiC carbonized layer because of sealed up out-diffusion of Si atoms. In comparison between Type II and Type III, Si surfaces are completely sealed up out-diffusion of Si with single-crystalline 3C-SiC carbonized layer by using Type III. It is impossible to evaluate the carbonized layers by simple one-layer model of Ellipsometry, so multi-layers model of Ellipsometry was adopted to the carbonized layers by using Type II and Type III. Simulation of the carbonization layers by using interface layer between each layers agreed with changes of experimental data as a function of carbonization time as shown in Fig. 3. From these results, It is possible to suggest the model of the carbonization by using Type II and Type III as shown in Fig. 4.

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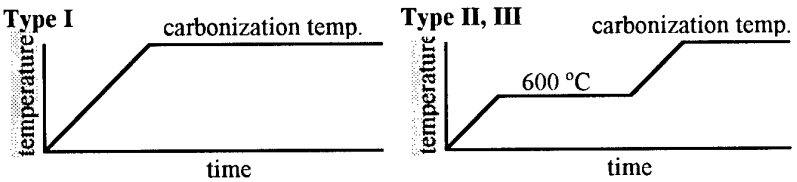


Fig. 1 Temperature program for carbonization process. Substrate temperature of Type II and Type III is held at 600°C for 5 min and 15 min respectively prior to heating up to carbonization temperature.

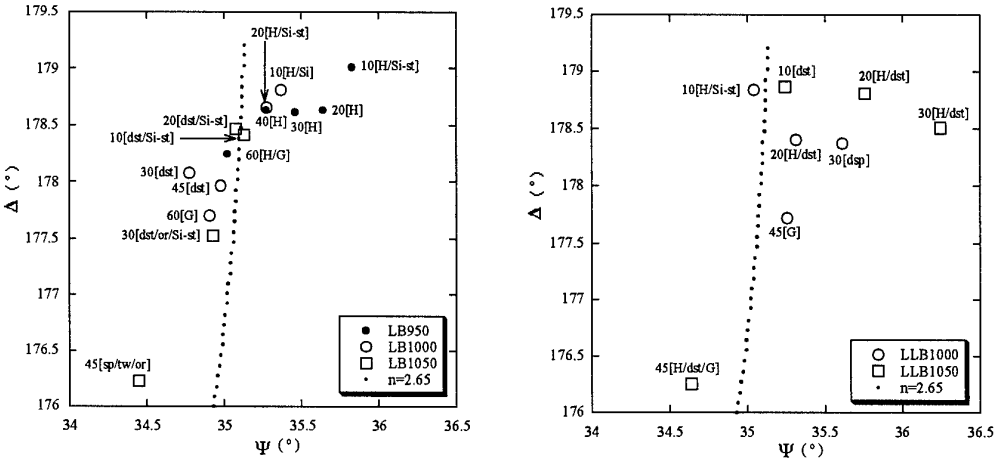


Fig .2 Changes in measured Δ and Ψ values and results of RED patterns of the films deposited by Type II (LB) and Type III (LLB). Theoretical line (one layer model) indicates n=2.65, k=0 for 3C-SiC. One dod indicates 2 Å. Number , H, Si-st, dst, sp, or, tw and G by plots indicate carbonization time, halo, Si-streak, 3C-SiC diffused streak,3C-SiC spot, oriented, twin and graphite ring of RED patterns.

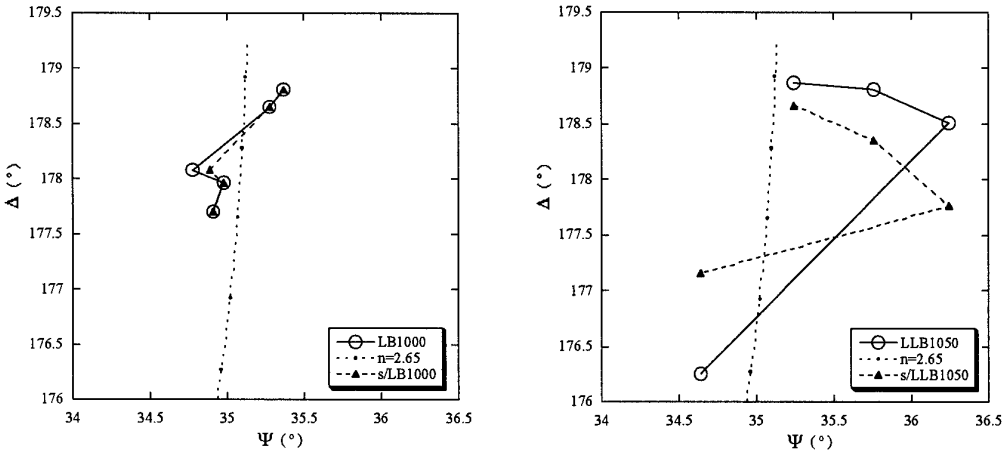


Fig.3 Simulation of carbonized layers for Type II and Type III by multi-layers model of ellipsometry. A solid and a broken line show experimental and simulation data respectively.

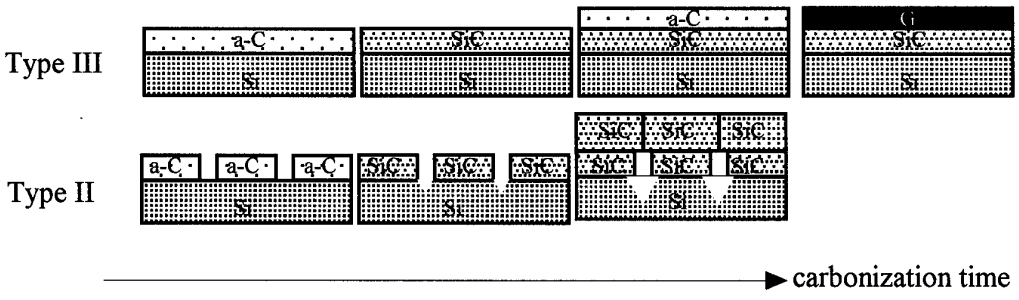


Fig. 4 Carbonization model for Type II and Type III

Carbonization process of a Si surface by subplantation of low-energy ions

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A novel carbonization process for 3C-SiC heteroepitaxial growth on Si (100) using subplantation of low-energy mass-separated carbon ion beams is proposed. SiC is an important candidate of the semiconductor materials for achieving the production of high temperature electronics, power devices, etc. In particular, the heteroepitaxial growth of 3C-SiC on Si substrates is a key technology for those electronic devices. It has been reported that a so-called carbonization process forms a SiC buffer layer which is required for the successful heteroepitaxial growth of 3C-SiC on Si. However, conventional methods such as MBE, CVD, etc. have required high temperatures ranging 700–1000 °C for achieving carbonization reaction. Those high temperatures cause serious problems of defects such as dislocations and stacking faults at the heterointerface. In this study, a carbonization process at lower temperatures has been tried using low-energy carbon ion beams for solving these problems.

Si (100) surfaces were directly irradiated by mass-separated low-energy (20–700 eV) carbon ion beams (e.g., C^-, C_2^-, C^+, CH_3^+ ions). Such energetic ion beams are implanted into a subsurface (subplanted) of the Si substrate, unlike thermal species used for MBE and CVD methods. The substrate temperatures were varied in the range 440–700 °C. RHEED measurements were performed during ion irradiation for in-situ characterization of the carbonization process. The base pressure of the deposition chamber was ~10^{-8} Pa and the beam-on-target pressure was 1–4 × 10^{-6} Pa.

Carbonization reaction was achieved at substrate temperatures of 500-700 °C with all kinds of carbon ions e.g.; C^-, C_2^-, C^+, CH_3^+ ions. There was almost no significant difference in the diffraction patterns between C^-, C_2^- and C^+ ion-beam carbonization. All the RHEED images after irradiation of these carbon ions consisted of spotty patterns indicating 3D-island growth of a 3C-SiC. On the other hand, the diffraction image after CH_3^+ irradiation exhibited streak patterns, suggesting a smooth surface and better crystallinity relative to

irradiation by other species.

The carbonization temperatures of 500-700 °C using ion-beams are relatively low compared to conventional methods. While the process with thermal gas species with less than 1 eV is basically thermal equilibrium or nearly-equilibrium reaction, carbon ion beams as energetic species with several to hundreds of electron volts employed in this study allow non-equilibrium reactions. The difference of reaction mechanisms between these has probably affected the carbonization temperature.

GROWTH AND CHARACTERIZATION OF SiC NANOROD STRUCTURES CONTAINING Si NANOCRYSTALS

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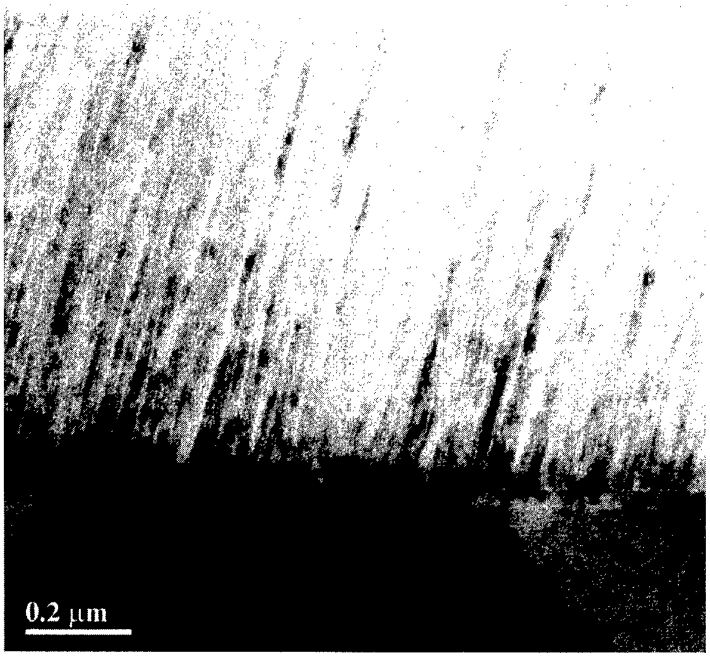
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The rapid developments taking place in the preparation and application of nonostructures is one of the most exciting areas of material science and technology. Since the discovery of carbon nanotubes, nanoscale materials have received widespread interest and nanorods of various materials have been synthesized so far. Nanorod structures, for example, have become an important material because of its excellent mechanical properties. Furthermore, devices made using nanorods can be critical for nanoelectronics. Moreover, the electron field emission properties of carbon nanotubes are of special interest for their potential application in flat panel displays. SiC nanorods were found also to be a promising material for applications in field emission technology. The electron field emission characteristics are similar to that one of carbon nanotubes. However, it is still difficult to control the rod size and orientation.

In this work we present results of the growth and the characterization of SiC nanorod structures. The nanorods were prepared on a SiC/Si(111) heterostructure under ultra high vacuum conditions at low temperatures of 1000 K using elemental silicon and carbon. Si and C were evaporated by means of electron-beam guns. The single-crystalline SiC of some nanometers thickness was grown before on Si(111) by molecular beam epitaxy.

The obtained SiC nanorod structures are homogeneous in the diameter and the length of the rods across the thickness of the structure (Figure). The diameter of the nanorods is in the range of 5-10 nm, the smallest values known so far. The rods consist of a high-density of stacking faults like a "one-dimensionally disordered" SiC polytype. This is supported by Raman scattering experiments, where the intensities of the SiC related phonon lines were very low and at different positions, depending on the structure. Furthermore, there is a strong alignment of the rods. However, the rods are tilted with respect to the [111] surface normal of the SiC layer by about 15°, which is about the [311] direction.

Between the rods, the material is amorphous and contains a high amount of Si nanocrystals, which is depending on the excess of Si in the Si/C ratio. The size of the Si nanocrystals was in the range of 1 nm. In Raman scattering experiments, the Si line was found to be broad and shifted to smaller wave numbers with respect to the Si bulk line. Moreover, a strong optical absorption in the nanorod structure occured in dependence on the structure. Si nanocrystals with sizes smaller than 1.5 nm should demonstrate quantum confinement effects, what increases the oscillator strength significantly. The obtained structures, therefore, also allow the investigation of the optical properties of Si nanocrystals embedded in an oxygen-free, high dielectric matrix.



High-resolution TEM image of a SiC nanorod structure grown on SiC/Si(111)

RHEED: A tool for structural investigations of thin polytypic SiC layers

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One of the exceptional challenges of SiC is the possibility of the formation of heteropolytypic structures for heterojunction based advanced semiconductor devices. For the experimental realization of such devices, the development of methods for the controlled formation of different polytypes, polytypic multilayers and their interfaces is necessary. In the last decade substantial progress was achieved in this field [1,2]. The most promising technique is molecular beam epitaxy (MBE) offering exceptional possibilities for controlling and adjusting growth conditions [2], but extended post- growth characterization is necessary in order to identify the appropriate growth conditions, leading to desired surface morphology and polytype structures [3]. Nevertheless the MBE technique offers the possibility to study the structure of the growing polytype layer in situ in real time by applying reflection high energy electron diffraction (RHEED). Up to know only, relatively few papers have dealt with such investigations. Most of them utilized the analysis of the three dimensional electron diffraction pattern for polytype analysis. In the case of two dimensional diffraction, because of the difficulty in the exact determination of the streak modulations and in the interpretation of them, no data is available. In this work it will be shown that even in the case of two dimensional diffraction it is possible to distinguish between different polytypes and surface polarities.
For this reason we determined the inner potential of the silicon carbide by analysing the geometry of the horizontal Kikuchi lines for our diffraction condition. A value of 15.4 V was obtained. The value RHEED pattern simulation was performed by using the semi-kinematical approximation described in [4]. The simulation was carried out for the 3C, 4H and 6H polytypes and silicon and carbon faces and angels of incidence between 0.5 and 4°. The results obtained allows the conclusion that the polytypes can be distinguished in the case of two dimensional diffraction if the penetration depth of the electron beam is not smaller than the characteristic period of the polytype, i.e. if the specific features of the polytypes can be detected by the electron beam. To distinguish different polarities of the growing surface the penetration depth has to be smaller than seven layers. The best sensitivity to the different polarities can be obtained if the penetration depth does not exceed three double layers. From the carried out simulations of the two dimensional diffraction features it follows that the optimal angel of incidence for RHEED diffraction analysis of different polytypes and polarities is in the range of 1 to 2.5°.

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MOLECULAR ADSORPTION OF OXYGEN ON SiC SURFACES

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The initial steps of the oxidation of Si surfaces have been extensively studies and most of the oxygen molecules absorb dissociatively on Si. However, at small oxygen exposures and low substrate temperatures a metastable molecular O_2 species has been observed [1,2,3]. Since the initial steps of oxidation of SiC are also of great interest and importance we have studied if a similar metastable molecular precursor for the dissociative adsorption of oxygen do form on SiC surfaces.

The O 1s photoemission spectrum recorded from a $\sqrt{3}x\sqrt{3}$ R30° reconstructed 4H-SiC(0001) surface after an oxygen exposure of 0.3 L (1 Langmuir = 10^{-6} torr sec.) is shown in Fig. 1. The substrate was cooled to liquid nitrogen temperature during both exposure and measurements and the spectrum was collected using a photon energy of 600 eV. The spectrum is seen to contain several components and included in the figure is a peak decomposition. Four components, labeled 1 to 4, are clearly distinguished similarly as on the Si(111) surface [3]. Components 3 and 4 are interpreted to originate from molecular O_2 and components 1 and 2 from atomic oxygen. The relative intensities of these components did vary with the amount of oxygen adsorbed on the surface.

Also with the substrate at room temperature some molecular O_2 was found to adsorb while no trace of molecular O_2 was discernable after adsorption with the substrate at an elevated temperature of 800° C. This is illustrated in Fig. 2 where the O 1s spectrum recorded after 1 L exposure is shown for the three different cases, LN, RT and 800° C.

Studies were carried out on both Si- and C-terminated 4H-SiC (0001) crystals and differences between the two surfaces were observed. The time evolution of the O 1s spectrum was monitored since the state was assumed to be metastable. Our findings, showing that a molecular state precedes the dissociated (atomic) stable adsorption states on SiC surfaces, will be presented and discussed.

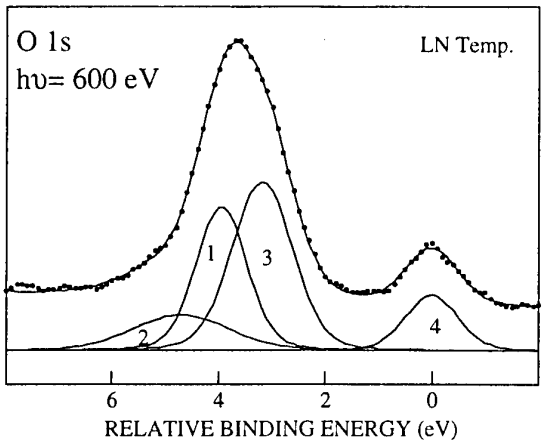


Fig.1. O 1s spectrum (dots) recorded using a photon energy of 600 eV after 0.3 L of oxygen exposure. The solid curve through the data points show the result of the curve fit and the curves underneath show the components used. See text for details.

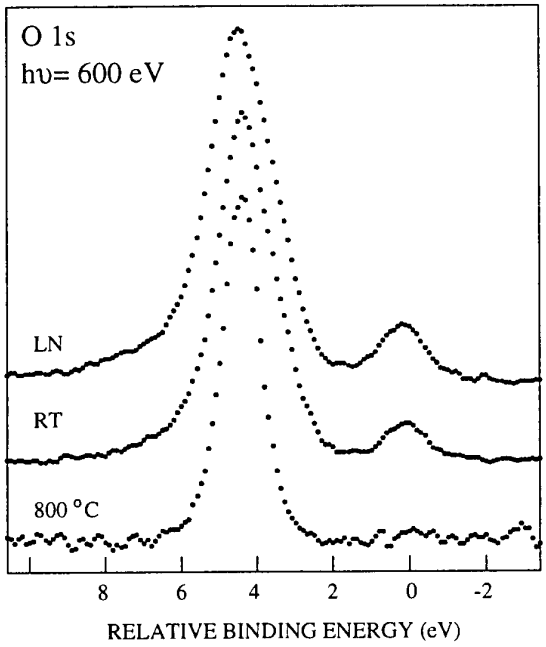


Fig.2. O 1s spectra recorded after 1 L of oxygen exposure at different substrate temperatures, LN, RT, and 800°C.

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3C-SiC pn -STRUCTURES GROWN BY SUBLIMATION EPITAXY ON 6H-SiC SUBSTRATES

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Cubic silicon carbide is of considerable interest for semiconductor electronics having, in particular, the highest charge carrier mobility of all SiC polytypes; besides, it is also known that β-SiC is sometimes found in the form of inclusions in epitaxial films of wider bandgap polytypes of α-SiC. Therefore, studies of β-SiC and identification of the effects caused by the presence of β-SiC in α-SiC are of unquestionable interest. Progress in the sublimation epitaxy in vacuum (SEV) technology enabled fabrication of n-3C-SiC/n-6H-SiC epitaxial heterostructures with good quality of the 3C-SiC epilayer [1].

The aim of the present study was to obtain 3C-SiC pn structures by SEV and study their properties. The investigated pn structures were grown by SEV on 6H-SiC (0001) Lely substrates. X-ray topography showed that the preliminarily grown n-type epilayer contains a large region of 3C-SiC, which is double-position (DP) twin. The area of the n-3C-SiC layer was about 25 mm^2 The pn junction was formed by SEV growth of a p^+ (Al)-layer. X-ray topographs confirmed that a p^+-3C region with DP twins of different sizes is formed on the n-type epilayer . An ohmic contact to the p-type region was formed by deposition of Al and Ti and annealing at 1100°C. Mesa structures of area $3x10^{-3}$ cm^2, 10^{-4} cm^2, and $8x10^{-5}$ cm^2 were fabricated by reactive ion-plasma etching (to a depth of about 3 μm) with an Al mask.

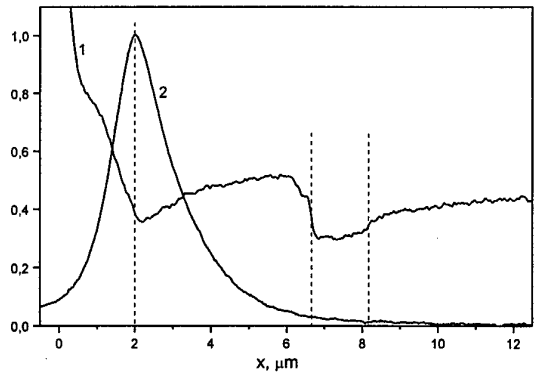


Fig.1. Secondary electrons (curve 1) and electron beam induced current (curve 2) signals for diode.

The diode cross sections were studied by the methods of electron beam induced current (EBIC) and secondary electrons (SE) in a JSM-50A scanning electron microscope. Figure 1 shows the coordinate dependencies of SE and EBIC signals obtained in scanning of the cross-sectional surface of diodes. The SE curve shows three jumps of the SE signal. The portion with the largest jump corresponds to the pn junction in 3C-SiC, which is also well manifested in the EBIC mode. The other two portions correspond to isotype n-3C SiC/n-6H SiC junctions and the n-6H SiC/substrate. Thus, in the initial stages of epitaxial growth on the 6H SiC substrate, a buffer n-6H SiC layer of thickness ~1.5 μm was formed. Then, there occurred polytype transformation and growth of an n-3C-SiC epilayer (4.5 μm thick). The pronounced jump of the secondary electron signal at the interface of the 3C-6H SiC isotype heterojunctions indicates a substantial potential jump at the interface between two semiconductors. An estimate of the hole diffusion length in the n-3C SiC layer, made on the basis of EBIC data, gave a value of ~1.5 μm. So a noticeable fraction of holes injected from

p-3C SiC can diffuse through the n-3C SiC layer to reach the interface with the buffer 6H-SiC layer.

The capacitance-voltage (C-V) characteristics of the diode were linear in the C^{-2} – V coordinates, which means that the obtained pn junction was abrupt. The capacitance cutoff voltage (U_c) was 2.05 ± 0.05 V for diodes, i.e. close to E_g for 3C-SiC (2.39 eV). It was shown, that at low current densities the dependence of the current on voltage is exponential: $J = J_0 \exp(qV/nkT)$ with the ideality factor n=2.5-2.6 (Fig.2.a). The J-V characteristics of the diodes were fairly close to those of anisotype homojunctions based on bulk 3C-SiC [2].

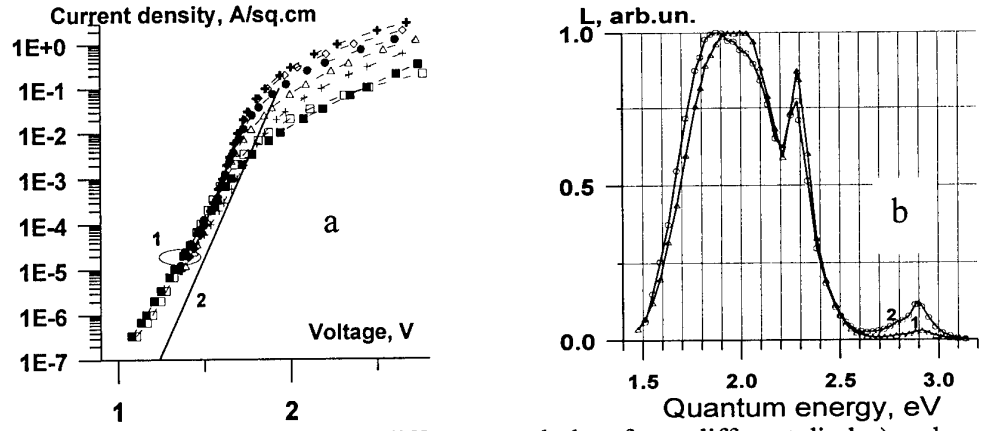


Fig.2. Experimental (curves 1; different symbols refer to different diodes) and calculated (curve 2; for 3C-SiC pn homojunction [2]) current-voltage characteristics at forward bias and room temperature (a); injection electroluminescence spectra for two diodes: of area $3x10^{-3}$ cm^2 (curve 1; current 150mA) and $8x10^{-5}$ cm^2 (curve 2; current 100mA) (b).

Injection electroluminescence spectra (IEL) for diodes are presented in Fig.2.b. The emission bands $h\nu_{max} \approx 1.8$-2.0 eV (red), $h\nu_{max} \approx 2.3$ eV (green) and $h\nu_{max} \approx 2.9$ eV (violet) are dominant; both the absolute and relative intensities of the emission bands at $h\nu_{max} \approx 2.9$ eV and $h\nu_{max} \approx 2.3$ eV grow with increasing current and the diode temperature. The spectral position of the EL bands at $h\nu_{max} \approx 2.9$ eV and $h\nu_{max} \approx 2.3$ eV, closeness of energies to the band gaps of 6H- and 3C-SiC, their narrow half-widths (compared, in particular, with the half-width of the so-called "defect" line (green in 6H SiC), and the characteristic change in their intensity with increasing current and stronger heating make it possible to relate these two EL bands to free exciton annihilation in 6H- and 3C-SiC. The red emission band appears to come from 3C-SiC and is believed to be due to transitions involving Al.

The characteristics of the structures under study correspond to those of homojunctions based on 3C-SiC. The emission band in the IEL spectrum of this kind of diodes, arising from recombination of free exciton in 6H SiC, is probably related to hole diffusion from p^+ 3C through the 3C SiC layer to the interface with the buffer 6H layer. The fact that this emission comes from within the base region, and not from the metallurgical boundary of the pn junction, is clearly seen on an edge cross-section of the sample under an optical microscope.

This work was supported by the RFBR (grant N00-02-16688 and 01-02-17657).

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Sensitive Detection of Defects in α and β SiC by Raman Scattering

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Raman spectra provide information on the structure of crystals. One can analyze defects from the difference of the Raman spectra for perfect and imperfect crystals. So far, we have developed a technique for sensitive detection of defects in 6H,4H [1] and 3C SiC. This technique is based on the measurement at Raman forbidden geometry and has been applied to the characterization of defects in bulk crystals and epitaxial layers of SiC. Electrical properties such as carrier concentration and mobility can also been analyzed by Raman spectroscopy [2]

In this work we have developed a method to detect low density of defects and analyze the local structure of the defects from band shape of the TO phonon bands. We also examined affect of defects on the distribution of the carrier concentration from Raman image measurements of the LO phonon plasmon coupled mode in doped SiC wafers.

In perfect crystals the wave vector selection rule and polarization selection rule hold strictly during the Raman scattering process. These selection rules break down partially when there are defects, because the periodicity and symmetry of the crystals are destroyed. The defect-induced Raman scattering signals are usually weak and buried in a strong background, which can be avoided by choosing a suitable scattering geometry. We found that the observation at the Raman forbidden scattering geometry is efficient for detecting the defect induced-Raman bands. For SiC the TO and folded TO modes are sensitive to the defects as compared with LO phonon modes. We used unfolded TO mode designated as FTO(0) at 796 cm^{-1} as a monitor band for the defects in 6H- and 4H-SiC, which is Raman forbidden at the back scattering geometry using the (0001) face [1]. The TO band in 3C-SiC is forbidden at the back scattering geometry using the (001) face.

We have measured Raman images of the (100) cross section of homoepitaxial SiC films. An epitaxial film (100 μm) was made on a heteroepitaxially grown SiC of 100 μm thick, for which the growth surface was originally the interface of the SiC and Si. Therefore, it is

anticipated that defects are concentrated in the central region of the film. In Fig.1, the intensity and half width of the forbidden TO band are plotted as a function of the distance. The intensity and the width of the TO band are large at around the central region. The TO band is broad compared with that observed using the (110) face, and is asymmetric. It has a tail on the low frequency side at the central region as shown in this figure. These results show that the defect density is high at the central region which was originally the SiC-Si interface. The asymmetry and broadening of the TO band is indicative of the presence of the stacking faults [3,4] and other defects such as antiphase boundaries and dislocations.

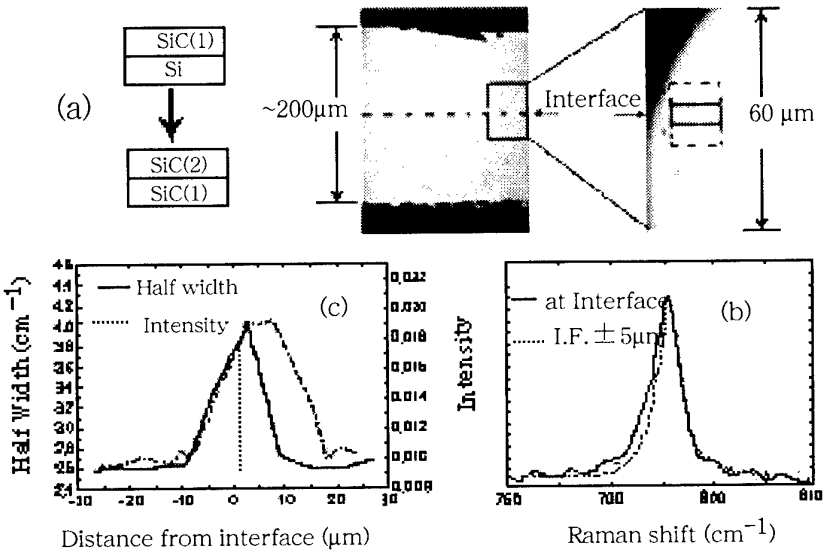


Figure 1 (a) optical microscope image of the (100) cross section of the homoepitaxial film , (b) Raman spectra of the TO band, and (c) the intensity and half width of the forbidden TO band vs distance.

The Raman images of the LO phonon plasmon coupled mode are also measured in doped 4H- and 6H-SiC wafers. The reduction of the free carrier concentration is found around some micropipes as reported before[5]. Change in the carrier concentration is also observed at defective portions which might be associated with threading dislocations , and for planar defects.

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LUMINESCENT PROPERTIES OF EPITAXIAL LAYERS OF SOLID SOLUTIONS BASED ON SiC.

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Solid solutions based on SiC make it possible to enlarge the range of application of optoelectronics devices. Specifically, LED's and injection lasers are very promising, since they can inherit, on the one hand, the unique properties of silicon carbide and, on the other, they can acquire properties which are characteristic of the second component of the solid solution.

$(SiC)_{1-x}(AlN)_x$ and $Si_{1-x}Nb_xC$ solid solutions have been received by sublimation in Ar + N_2 atmosphere on n-type 6H-SiC substrates. The composition of epitaxial layer (EL) has been set with source of vapor, and the type of electrical conductance – with regulation of Ar and N_2 partial pressure in the growth zone.

The spectra photo- (PL) and cathodoluminescence (CL) $(SiC)_{1-x}(AlN)_x$ and $Si_{1-x}Nb_xC$ solid solutions was investigated. The samples with such composition layers $(SiC)_{1-x}(AlN)_x$ ($x>0,55$) are used for which the light of N_2 - laser ($h\nu=3,68$ eV) lies in the transparency area ($E_g>4,8$ eV) and that is why so cannot effectively excite their emission. The CL spectra were measured at liquid – nitrogen temperatures and exitation energy of 15 kV.

It is observed that at liquid – nitrogen temperature two bands with $\lambda = 520$ nm ($h\nu_{max}$ ~2,4 eV) and $\lambda = 480$ nm ($h\nu_{max} \sim 2,6$ eV), which due to recombination on defects and donors – acceptor pairs are observed in $(SiC)_{1-x}(AlN)_x$ solid solutions spectra. As the AlN concentration in $(SiC)_{1-x}(AlN)_x$ solid solutions increases the bands shift continuously into the short – wavelength region and an ultraviolet "tail" with $\lambda = 390$ nm ($h\nu_{max} \sim 3,2$ eV) appears. The last peak indicates the solid solution formation in system SiC-AlN and a change in the structure of the band gap. The color of the emission changes from yellowish – green to pale blue.

PL intensity decreases with the x growth in $(SiC)_{1-x}(AlN)_x$ solid solutions, though the main bands and distances between them are practically preserved. On one hand, it is connected with increase of share of centers of nonradiative recombination, as far as at $x>0,40$ decreases the structural perfection of $(SiC)_{1-x}(AlN)_x$ solid solutions and presence of defects of layers grow. On the other hand, presence Al and N_2 reduces the efficiency of DL. And, at last, the change of intensity, perhaps, is stipulated by increase of probability of interbanded transitions, as far as at $x \approx 0,75$ the reorganization of structure of solid solution to direct gap happens.

The CL spectra of $Si_{1-x}Nb_xC$ solid solutions was investigated. It is differ already at $x = 0,01 – 0,02$ and the color of the emission changes to red - purple one. One intense band with $\lambda \sim 500$ nm is observed in $Si_{1-x}Nb_xC$ solid solutions CL spectra. The ultraviolet "tail" in the spectra disappears even at small x that indicates on change of nature of radiative centers.

Influence of the crystalline quality of epitaxal layer on the inversion channel mobility in 4H-SiC MOSFETs

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Silicon Carbide (SiC) is a promising material for high power, high frequency and high temperature electronic devices. SiC has many polytypes. Among them, 4H-SiC has wider band-gap and higher bulk electron mobility than 6H-SiC. 4H-SiC MOSFETs, however, show lower inversion channel mobility than that of 6H-SiC [1]. Many researchers have studied the effect of MOS process conditions on the channel mobility of 4H-SiC MOSFETs [2-4]. However, few investigations on the influence of the crystal quality of epitaxal layers on the channel mobility have been reported. In the present study, we have fabricated MOSFETs on epitaxial layers of different growth lot, and investigated the relationship between the inversion channel mobility and crystalline qualities of epitaxial layer.

As shown in Table 1, we have used three different p-type 4H-SiC epitaxial layers grown on conventional off-angled p-type (0001) Si face substrate for fabricating MOSFETs. Epi A was purchased. Epi B and Epi C were self-made that were grown by low-pressure, hot wall type, horizontal CVD reactor with $SiH_4 - C_3H_8 - H_2 -$ TMA system. The growth conditions were also summarized in Table 1. The crystal quality of epilayers was characterized by Hall effect measurement, AFM, x-ray diffraction and photoluminescence measurement. The MOSFETs were fabricated on these epilayers by the same process. The gate oxidation was formed at 1200°C for 140 min followed by post-oxidation annealing at the oxidation temperature for 30 min in Ar. The deatales of MOSFETs fabricating were described elsewhere [5].

Table 2 shows the channel mobility (μ_{FE}) and the threshold voltage (V_T) of MOSFETs. The value of the channel mobility obtained from MOSFETs on Epi A and Epi B is the same as that of previous report [6]. On the other hand, the channel mobility of Epi C is about three times higher than that of another epilayers. The fabrication process of these MOSFETs was the same as the process in this investigation. Therefore, the higher channel mobility in Epi C is probably caused by the difference in the crystal quality of epitaxal layers.

Table 1. Characteristics and growth conditions of epilayers

Sample	Epi A	Epi B	Epi C
N_a-N_d (cm^{-3})	5×10^{15}	1×10^{16}	3×10^{15}
Thickness (μm)	5	5	5
Ts (°C)		1600	1500
P (mbar)		250	250
H_2 flow rate (slm)		40	40
SiH_4 flow rate (sccm)		6.67	3.3
C_3H_8 flow rate (sccm)		3.33	0.88

Table 2. Values of channel mobility and threshold voltage

Sample	Epi A	Epi B	Epi C
μ_{FE} (cm^2/Vs)	6	5.4	14.1
V_T (V)	3.9	3.8	1.9

Then, we investigated the crystal

quality of epilayers. The results are summarized in Table 3. The bulk mobility (μ_H) of Epi C was slightly lower than that of Epi A and Epi B, although the channel mobility of Epi C is higher than that of Epi A and Epi B. The surface roughness (Rms) of Epi C is slightly smaller than that of Epi A and Epi B. The FWHM of x-ray rocking curve of ω scan in three epilayers was roughly the same. As seen above, we could not find clear correlation between the channel mobility and μ_H, Rms and FWHM.

Table 3. Crystal parameters of epilayers

Sample	Epi A	Epi B	Epi C
μ_H (cm^2/Vs)	99	95	91
RMS at 16μm^2 (nm)	1.2	0.82	0.71
FWHM of XRD (arcsec)	68.8	142.9	73.2

Photoluminescence measurements were also carried out at liquid helium temperature. The 244 nm line of Ar^+ ion laser was used as the excitation source. Zero phonon luminescence line of the neutral aluminum acceptor and phonon spectra of the neutral nitrogen donor bound exitons were observed in both epilayer as shown in Figure 1. The broad peak due to Aluminum related donor-acceptor (D-A) pair peak was also observed around 420 nm. In this figure, the intensity of spectra was normalized by that of D-A pair peak due to comparison of the PL intensity. The intensity of near band-gap emission with Epi C is quite strong as compared with that of Epi A and Epi B as can be seen from Figure 1. This indicates that the crystalline quality of Epi C is better than Epi A and Epi B. In conclusion, it is found that the channel mobility has a correlation to crystalline quality observed at the intensity of the near band-gap emission. The channel mobility becomes higher when the intensity of near band-gap emission is strong.

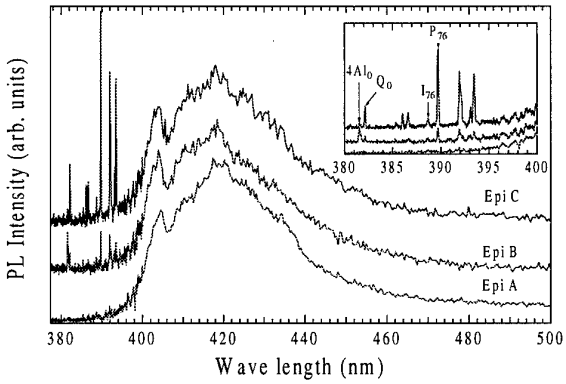


Figure 1 Photoluminescence spectra of epilayers. Near bang-gap emission of epilayer is shown in the inset.

Acknowledgement

This work was performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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Full band Monte Carlo simulation of electron transport in 3C-SiC

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ABSTRACT

Silicon Carbide is a very interesting semiconductor material for high temperature, high frequency and high power applications. The main reasons are its high saturation velocity, large thermal conductivity, high Schottky barriers and large breakdown voltages.
High quality 4H-SiC and 6H-SiC polytype substrates and expitaxial layers are commercially available today. 3C-SiC has been grown successfully in the form of films on Si(100). There are several theoretical studies on the charge transport in 3C-SiC. However, we present the first full band MC simulation of the electron transport at high electric fields. The full band Monte Carlo model is based on an ab initio band structure calculation using the Local Density Approximation (LDA) to the Density Functional Theory (DFT). The following scattering processes have been considered, acoustic phonon scattering, polar and non-polar optical phonon scattering, ionized impurity scattering as well as impact ionization. Fully k-dependent scattering rates for the phonon interactions and the transition rate for the impact ionization process have been directly extracted using the wave functions and the energy dispersion of the ab initio band structure. Coupling constants for the acoustic and the non-polar optical processes have been deduced from experimental data for the mobility as a function of temperature.
In Fig. 1. the simulated mobility as a function of temperature has been compared with experimental data by Yamanaka et al. [1]. The simulations are in very good agreement with the measurements. The saturation velocity in 4H-SiC and 6H-SiC has been measured to be close to 2.0 x 10^7 cm/s for an electric field applied perpendicular to the c-axis. There is no experimental data available for 3C-SiC. However, our simulations indicates that the value should be close to 2.2 x 10^7 cm/s which is in good agreement with results from the analytical Monte Carlo model used by Mickevicius et al. [2] (see Fig. 2.) and the measured values for 4H- and 6H-SiC. The effective mass in 3C-SiC is smaller for electrons than for holes and the impact ionization coefficients for electrons are expected to be higher than for holes. In Fig. 3. we present our simulation results together with the full band MC results by Bellotti et al. [3] for holes. The electron initiated impact ionization process is found to be much stronger than for holes, from 2 to 10 times stronger depending on the strength of the electric field.

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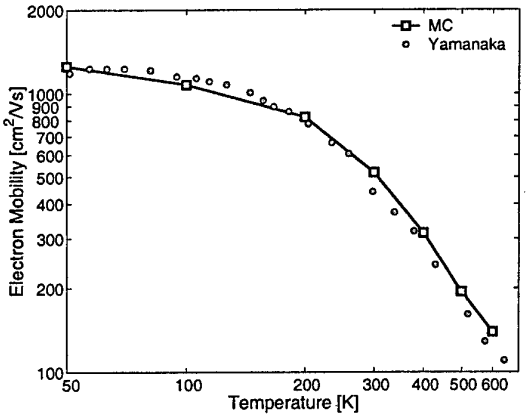


Figure 1. Electron mobility as a function of electrical field.

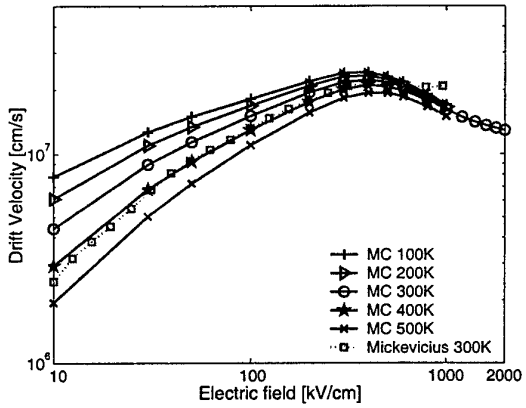


Figure 2. Drift velocity as a function of electrical field, plotted for different temperatures.

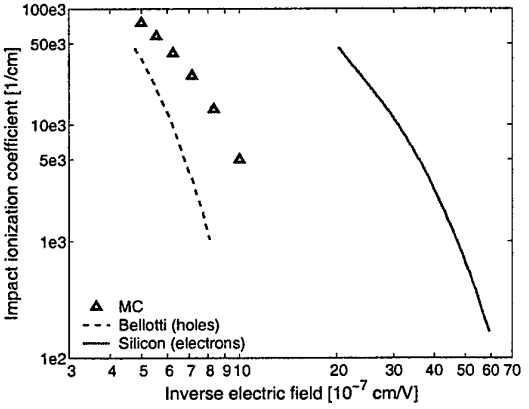


Figure 3. Electron ionization coefficient plotted for inverse electrical field.

Analysis of the surface damage caused by mechanical polishing of SiC wafers

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Dislocation free Lely platelets have been mechanically polished and used as seeds for the Physical Vapor Transport growth of 6H-SiC polytype. The type, density, and distribution of threading dislocations in the SiC overgrowth close to the interface has been analyzed by transmission electron microscopy (TEM) and interpreted in terms of the polishing-induced damage in the seed crystal.

Several characteristic features of dislocation distribution have been observed. Most of the threading dislocations present in the overgrowth are perfect edge dislocations propagating along [0001] direction with Burgers vector of 1/3<11-20>. The dislocations are arranged in form of cells typically between 0.2 – 0.5 μm in diameter with the nearly defect free central portion of the cell and high dislocation density along the cell walls. Walls are preferentially aligned along <1-100> directions with the average distance between neighboring dislocation of 0.05 μm. Such cell structure is consistent with a layer of a seed crystal distorted during polishing and rotated around the c-axis (and parallel to the basal plane) by approximately 1 degree. For this mechanism, the total Burgers vector for all dislocations in a single cell should be zero. An experimental evidence for this will be presented.

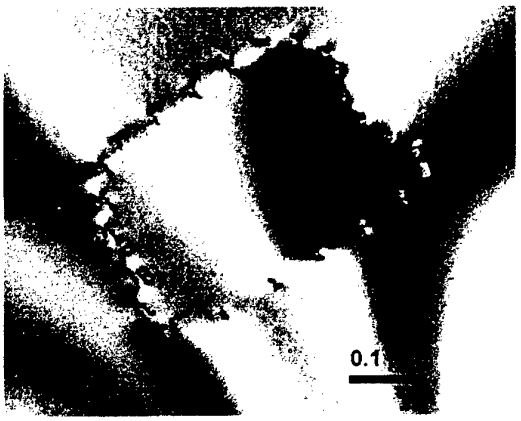


Fig. 1 Transmission electron microscopy image of a polishing-induced cell of threading edge dislocations.

The density of screw dislocations is approximately 10^5 cm^{-2} in the overgrowth and more than an order of magnitude lower than edge dislocation density. Threading screw dislocations are distributed in pairs with the average distance between nearest neighbors of about 0.3 μm. The Burgers vectors of screws in a pair dislocations are equal 1c and have opposite sign. A model for the polishing-induced deformation responsible for such configuration will be presented.

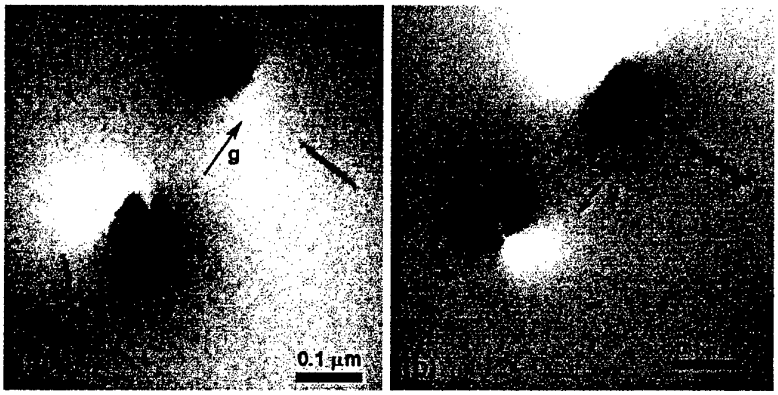


Fig. 2 Transmission electron microscopy image of a pair of threading screw dislocations

Gallium Nitride Metal-Insulator-Semiconductor Capacitors Using Low-Pressure Chemical Vapor Deposited Oxides

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Metal-Insulator-Semiconductor FETs (MISFETs) require low interface-state density interfaces in order to achieve gate-controlled devices. Also, interfaces play a key role in the DC, AC, and transient behavior of semiconductor devices, by providing locations for charge trapping and emission. Charge trapping at GaN-passivation interfaces can cause drain pinch-off, delayed turn-off transients, and reduced breakdown voltage. For the fabrication of GaN MISFETs, suitable dielectric materials and processes must be developed.

This study compares two low-pressure chemical vapor deposited (LPCVD) oxides on n-type GaN, namely a Low-Temperature Oxide (LTO) and a High-Temperature Oxide (HTO). On the unintentionally-doped n-type GaN samples, LTO was deposited at 450°C following the reaction:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

and the HTO was deposited at 900°C according to the reaction:

$$SiH_2Cl_2 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2HCl.$$

In both cases the target thickness was 50 nm, and aluminum dots were formed by evaporation through a shadow mask. A large area capacitor was used as an effective substrate contact and was observed to be equivalent to the use of an indium ohmic contact. Using this dual-capacitor technique with a small capacitor diameter of 0.5 mm, capacitance-voltage (C-V) characteristics and conductance-frequency (G-ω) characteristics of the two samples were measured.

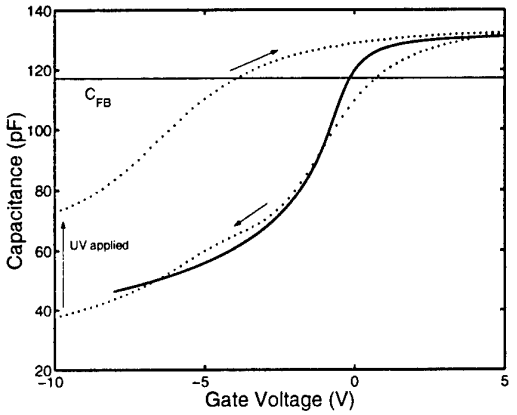


Figure 1: Measured (dotted) and ideal (solid) C-V curve at 1 MHz for LTO sample with UV excitation at -10 Volts.

As shown in Figure 1 for the LTO capacitor, the capacitors are biased from accumulation and reach deep-depletion. With ultraviolet (UV) light incident upon the sample, the capacitance reaches a steady-state inversion capacitance. The UV light causes a negative flat-band voltage shift by emptying trapped electrons, with

*The authors thank R. Wang, H. Lu, and I. Bhat for the GaN material used in this study, and M. Lazzeri, P. Gipp, and J. Balch from General Electric-Corporate Research and Development (GE-CRD) for oxide deposition. K. Matocha is grateful for fellowship support from GE-CRD. The authors acknowledge support from the NSF Center for Power Electronics Systems (Award #EEC-0731677).

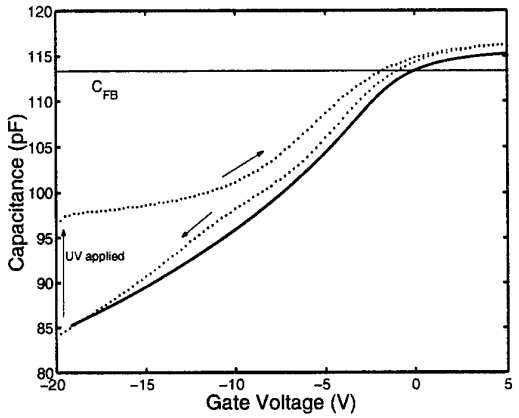


Figure 2: Measured (dotted) and ideal (solid) C-V curve at 1 MHz for HTO sample with UV excitation at -20 Volts.

flat-band voltage is given as

$$V_{FB} = \Phi_{MS} - \frac{Q_f + Q_{it}}{C_{ox}} \qquad (1)$$

From the flat-band shift of the LTO sample, Q_f and Q_{it} are calculated as 1.6×10^{12} and -2.0×10^{12} q/cm^2, respectively. Similarly, the HTO sample (Figure 2) exhibits lower Q_f and Q_{it} values, 6.4×10^{11} and -3.1×10^{11} q/cm^2, respectively. The C-V characteristic of the HTO sample shows only slight hysteresis when measured without UV light (Figure 3).

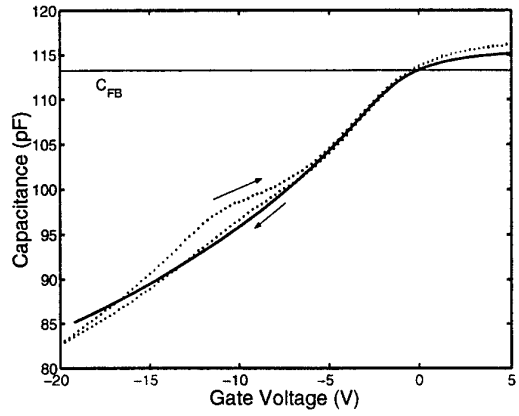


Figure 3: Measured (dotted) and ideal (solid) C-V curve at 1 MHz for HTO without UV excitation.

The G-ω technique is used to characterize

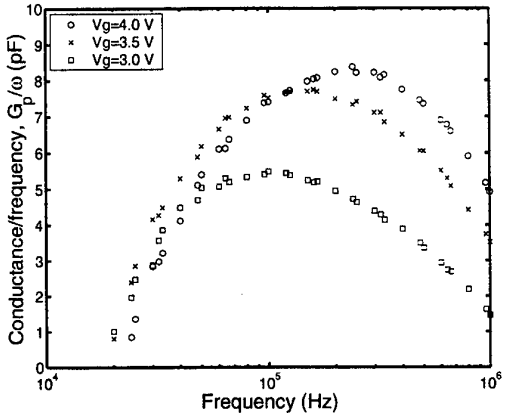


Figure 4: Conductance-frequency (G-ω) measurements on LTO sample.

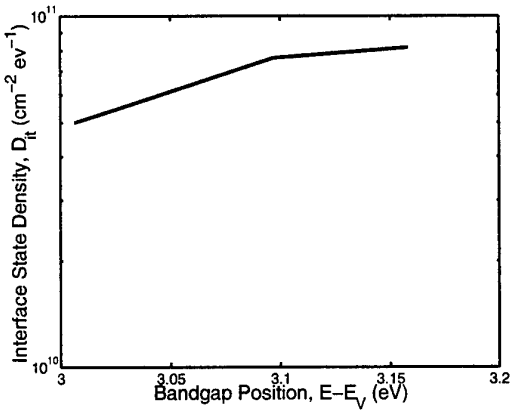


Figure 5: Interface-state density on LTO sample extracted from conductance-frequency (G-ω) measurements.

the interface-state density on the LTO sample as shown in Figure 4. The interface-state density near the conduction band is $\approx 8 \times 10^{10}$ cm^{-2} eV^{-1} as shown in Figure 5.

MOS capacitors using LTO have been fabricated on n-type GaN with an interface-state density of $\approx 8 \times 10^{10}$ cm^{-2} eV^{-1}. Capacitors with the HTO dielectric show a lower flat-band voltage shift with the application of ultraviolet light and are expected to have less fixed charge and a lower interface-state density than LTO capacitors. These results indicate that LTO and HTO LPCVD oxides are viable for GaN MISFET device gate dielectrics and passivation layers.

Characteristics of mobile ions in the SiO_2 films of SiC-MOS structures

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SiC (silicon carbide) is one of the most promising semiconductor material for high-power and high-frequency devices due to its wide bandgap, high breakdown field, high electron saturation velocity, and high thermal conductivity. SiC surface can be thermally oxidized in the same way as used for Si. The existence of mobile positive ions in SiO_2 layers of MOS (metal-oxide-semiconductor) structures is one of the important sources of instabilities in MOS devices. The behavior of these ions in Si-MOS devices has been extensively studied in order to stablize the device parameters.

Capacitance-voltage (C-V) & thermally stimulated currents (TSC) methods have been applied to characterize the mobile ions of MOS structures[1,2]. In this study, the characteristics of mobile ions in thermally grown oxide layers of 6H-SiC MOS capacitors are investigated by C-V and TSC measurements.

MOS samples used in this study are Au/SiO_2/6H-SiC structures. The wafers used were 6H-SiC epitaxial layers prepared by thermal CVD on n+ 6H-SiC (0001)Si-face substrates with 3.5° off-angle, which had undoped layers with doping concentration of about $1\times10^{16}cm^{-3}$. Oxide layers were obtained by thermal oxidation using dry oxygen or wet oxygen(95℃ steam, O_2 bubbling) at various conditions, and post-oxidation annealing was performed at 1150~1250℃ for 30 min in Ar-ambient. For the fabrication of MOS capacitors, gate electrodes were formed by sputtering of Au-dots with 200~500㎛ diameters, and backside ohmic contacts also formed by sputtering of W or Ni. In order to investigate the characteristics of mobile ions in oxide layers of SiC-MOS capacitors, C-V and TSC measurements were performed.

C-V characteristics of the MOS capacitors were measured at room temperature (300K) using a 1MHz C-V plotter in the dark. Figure 1 shows the C-V characteristics of a wet oxidized sample measured at 1MHz. In this case, it seems that the inversion dose not occur and the depletion layer spreads widely, probably owing to the absence of minority carriers because of the large bandgap of 6H-SiC[3]. After a C-V measurement at room

temprature, appropriate bias-temperature (B-T) stress is applied to a sample at an elevated temperature and then the sample is cooled down to room temperature with bias voltage still applied in order to measure the TSC. Then the sample is heated at a constant rate, and the short circuited current is measured. Figure 2 shows a typical TSC peak in the SiO_2 film of a wet oxidized 6H-SiC MOS capacitor. The bias voltage V_b = 3.0V is applied at a temperature T_b = 460K for t_b = 1.0 min. and the heating rate β is 0.1K/sec. It is found from Fig. 1 that a single peak is observed at T_p = 450K in the measured temperature ranges, and the peak is generated by positive mobile ions. The activation energy and Q_{TSC} obtained from the TSC curves increase as the bias voltage V_b increases.

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Acknowledgment

This Work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE(Ministry of Commerce, Industry and Energy), Korea.

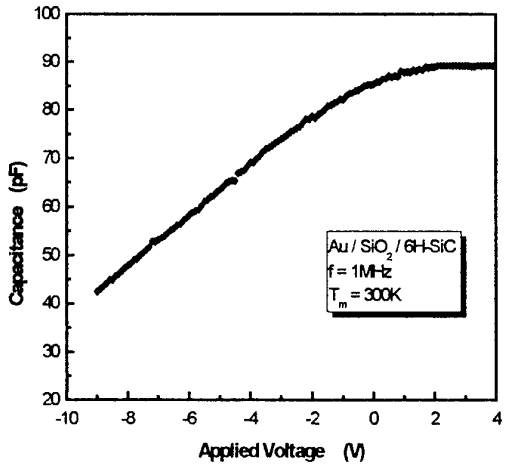


Fig. 1 C-V characteristics of a wet oxidized 6H-SiC MOS capacitor measured at 1MHz in the dark.

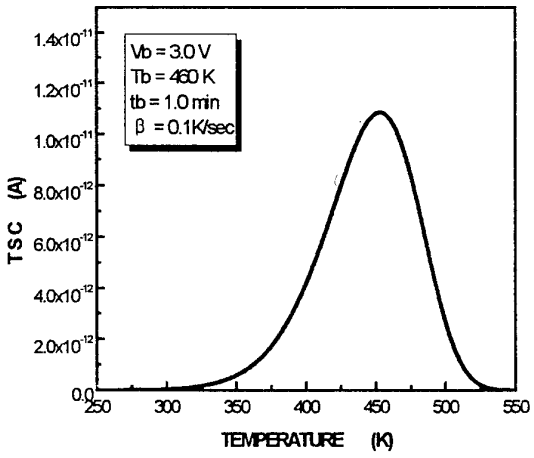


Fig. 2 A typical TSC peak in the SiO_2 film of a wet oxidized 6H-SiC MOS capacitor.

TEM (XHREM) and EDX studies of 6H-SiC porous layer as a substrate for the subsequent homoepitaxial growth

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Since the first report on electrochemical etching of bulk SiC crystal in hydrofluoric acid solution [1], large attention has been drawn to better understand physical properties of the material commonly known as a porous silicon carbide (PSC)[2,3]. In these papers the optical properties were being related with the microstructure of porous layers. Besides, hexagonal form silicon carbide, e.g. 6H-SiC polytype, is used as a substrate for growing high quality of GaN epitaxial layer and creating of semiconductor devices. This technology presents certain demands to the structural quality of bulk silicon carbide, whereas used for above purpose crystals (CREE) content micropipes and threading dislocations (10^2 cm^{-2}), which are inherited by epitaxial layer. Therefore the problem of receiving of the perfect substrates for the fabrication of the epitaxial technology based electronic devices continues to exist [4,5].

This paper focuses an attention on the microstructure analysis of the substrate/PSC/SiC epilayer cross-section by TEM (HREM). Misoriented by 3.5°, with respect to the c axis, commercial 6H-SiC crystal (CREE) was subjected to the electrochemical etching in HF : H_2O : C_2H_5OH = 1 : 1 : 2 solution at the illumination of the sample surface with UV light. At current density 10 mA/cm^2 and time of electrochemical etching 30 min the 34 μm thick pore layer was obtained. 6H-SiC 12μm thick epilayer was grown by the sublimation in vacuum over the PSC.

EM 4000EXII and EM 3000F electron microscopes were utilized. EDX spectra from area as small as 3 nm were recorded using SiLi detector. For preparing cross-section sample the conventional procedure (grinding, polishing, dimpling and Ar ion milling) was used.

It was shown that the substrate-porous layer boundary is extremely sharp unlike the upper boundary (porous layer-epitaxial one), which was subjected to sublimation etching prior the epitaxial growth. In addition, the porous layer is inhomogeneous along the layer thickness: near the upper interface there is ~1.5μm thick porous layer with enlarged pores in size (Fig.1). Near the bottom interface, at low magnification pores look like triangles. They are stacked and form the chains elongated approximately on the c- axis direction. Close to the upper boundary at intermediate magnification (100K) the pores seem as truncated triangles and in the shape they remind hexagons. At least one facet of the pore independent upon its size has the sharp interface parallel to the basal plane. Some images show clearly the amorphous structure of the internal surface of pores. High resolution image of pore crystalline-amorphous boundary show the gradual transition from crystalline region to amorphous one of the pore, certain atomic planes in this region being become diffused in character (Fig.2). Stronger contrast of (0001) lattice planes in the immediate vicinity of pores indicates on the stacking fault formation. The selected area electron diffraction pattern feature

in view of streaks in [0001] direction confirms the appearance of two-dimensional defects in the porous layer.

Comparison of EDX spectra recorded for different regions of cross-section sample shows that the amorphous internal surface of pore is significantly enriched by carbon (Fig.3). As to content of carbon in the epitaxial layer at the immediate vicinity of the porous layer, it is also higher than in SiC standard (substrate). The results received allow us to suggest that during electrochemical etching the selective extraction of silicon atoms occur. This process and high temperature growth give rise to the appearance of stacking faults and amorphous areas in the porous layer. No threading dislocations and any another defects have been observed in the epitaxial layer at all.

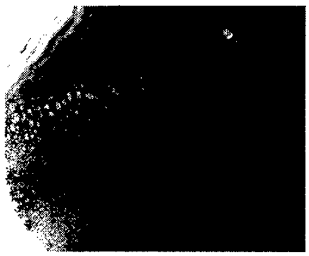


Fig.1. XTEM image of structure of porous layer at the vicinity of the epilayer

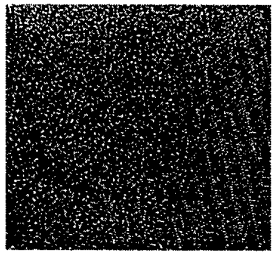


Fig.2. XHREM image of crystalline-amorphous part of pore

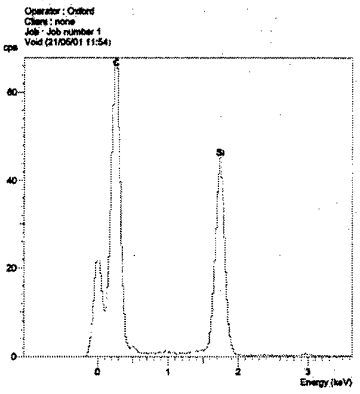


Fig.3a. EDX spectrum from the region containing the pore amorphous part

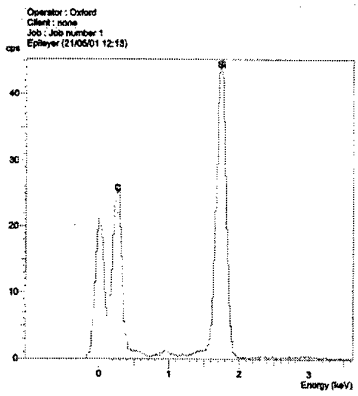


Fig.3b. EDX spectrum from the region of epilayer in the vicinity of porous layer

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This work is supported by RFBR grants 01-02-17907 and 01-02-17657.

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Measurements on linear TLM structures with TiW/Ti/Pt contacts for corrosive and high temperature applications

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Catalytic metal insulator silicon carbide, MISiC sensors, are routinely operated up to 600°C and short periods up to 1000°C [1] The speed of response, when changing between an oxidising and reducing ambient at temperatures ≥600°C is a few milliseconds [2]. Applications like cylinder specific monitoring in exhaust gases of a car engine, synthetic exhaust diagnosis, and flue gas monitoring have been demonstrated [3, 4]. We have used both Schottky diodes and transistor devices. Gas sensitive MISiCFET devices with catalytic gate metal have been designed and processed by ACREO AB [5]. They combine the advantage of high temperature stability, since these devices have a thick insulator, with simple electronic circuitry. The MISiCFET devices have been used in several high temperature applications [1].

Ohmic contacts, as well as an insulator, that performs in an oxidising atmosphere at temperatures up to 600°C are required for the MISiCFET devices used for car applications. The ohmic contacts to the 4H SiC used for the first three batches of transistors were made of evaporated Ni, 100 nm, annealed in an argon flow for 10 min at 950°C. On top of the Ni, 200 nm $TaSi_x$ and 400 nm Pt was sputtered as a protection to corrosion and to enable the bonding of gold wires. Linear TLM structures of this contact were tested and preliminary results were recently published [6].

Lee *et al.* has demonstrated earlier that TiW contacts on both p- and n-type 4-H SiC show good behaviour at high temperature under vacuum conditions [7]. We have performed further testing in corrosive environments. The contacts consists of 180 nm sputtered TiW, annealed at 950°C for 30 min. On top of this a 30 nm Ti layer and sequentially a 300 nm Pt layer were deposited using an e-beam evaporator. The top Pt top layer performs both as protection of the corrosive ambient and to improve gold bonding to the contacts. Linear TLM structures were processed and cut in 2×2 mm chip, which were glued on a heater. The heater is mounted on a 16-pin holder, which is put in an Al-block with a gas flow channel. A Pt-100 element is also glued on the heater for temperature control. Measurements of the resistance between the contacts were made with a Keithley 192 using four-point measurement technique.

Fresh samples had a specific contact resistance, ρ_c, of around 1×10^{-5} Ω/cm^2. Annealing in an oxygen containing ambient is interesting because many high temperature sensor applications involve that. The specific contact resistance was measured at the annealing temperature. The

results for two linear TLM contacts annealed at 500 and 600°C, respectively, in 2 % O_2 in N_2, is shown in Fig. 1. The contacts show a stable contact resistance at 500°C and some drift at 600°C in the oxidising atmosphere. To simulate car exhaust applications the contacts were exposed to a sequence of 3 min of 0.4 % O_2 in N_2, and 1 min of 1 % H_2 injected into this background gas, i.e. 3 min of oxidising ambient and 1 min of reducing ambient. During this annealing the contacts increased their specific contact resistance considerably, see Fig. 2, and it also had a detrimental effect on the gold bonding. Further testing of the long-term stability of the contacts will be performed at different temperatures.

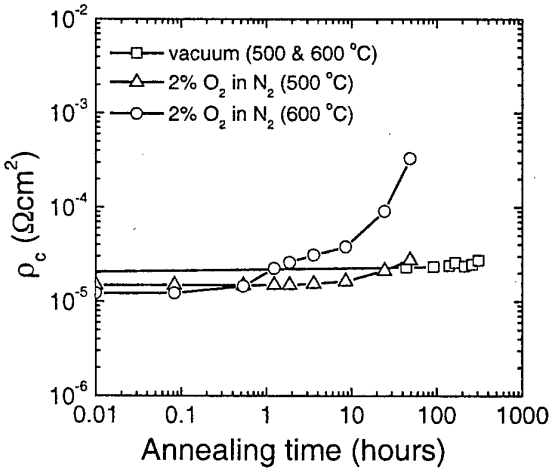


*Figure 1.*Contact resistance measured at the annealing temperature in 2 % O_2 /N_2 at 500 and 600°C, respectively In vacuum the temperature was 500°C for the first 140h and then 600°C for the final 168h [7].

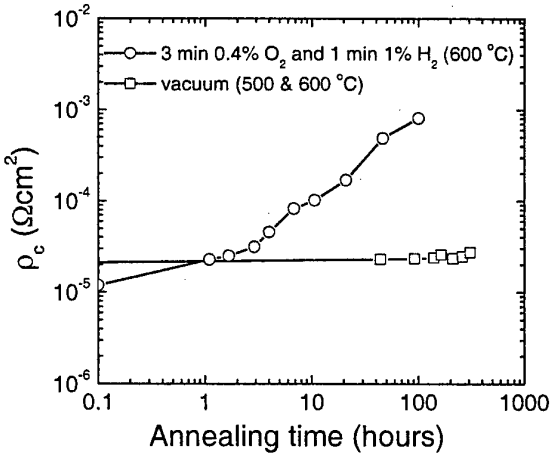


Figure 2. Contact resistance measured at 600°C in an alternating reducing and oxidising atmosphere.

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Point-contact current voltage technique for depth profiling of dopants in silicon carbide

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Introduction

Carrier concentration depth profiling is important in R&D of semiconductor devices, and many techniques have been invented. For silicon devices, spreading resistance profile (SRP) is useful since it has high spatial resolution and wide dynamic range. When SRP is applied to SiC, sensitivity of SR to doping concentration becomes low and the detectable concentration is limited to about 10^{17} cm^{-3} [1]. Since the drift layer concentration of high voltage (>1kV) devices is lower than about 10^{16} cm^{-3}, more sensitive technique is needed. For wider band gap materials, point-contact current voltage (PCIV), which is similar to SRP, is known to have higher sensitivity than SRP. SRP measures current at a low constant voltage between two-probes, on the other hand PCIV measures voltage at a constant current (Fig.1). We applied PCIV to characterize the doping profile of 4H-SiC.

Experimental

As the substrate, (0001)Si face of n-type 4H-SiC from Cree Inc. was used. The SiC wafer had a 10-μm-thick n-type epilayer with doping concentration of 1×10^{16} cm^{-3} and a n-type substrate with doping concentration of 1×10^{19} cm^{-3}. Phospher is implanted for 2×10^{15} ions/cm^2 with four energies up to 180kV as a ohmic contact layer, and activated at 1800°C. PCIV measurements were performed by a conventional SRP system, SSM-150 combined with SSM-350 from SSM Inc.

Results

Figure 2 shows current-voltage characteristics of point-contact for doping concentration of $10^{16}cm^{-3}$ and $10^{19}cm^{-3}$. The sensitivity of PCIV is determined by the voltage difference between the 2 curves. Though the voltage difference becomes large with current, it is limited by maximum voltage of potentiometer. We choosed 50nA as the constant current and depth profile is obtained as shown in Fig.3. Fig.3(a) shows doping profile of n^-/n^+ substrate showing flat doping in epilayer. Fig.3(b) shows doping profile of P implanted layer. PCIV result matches the TRIM calculated results.

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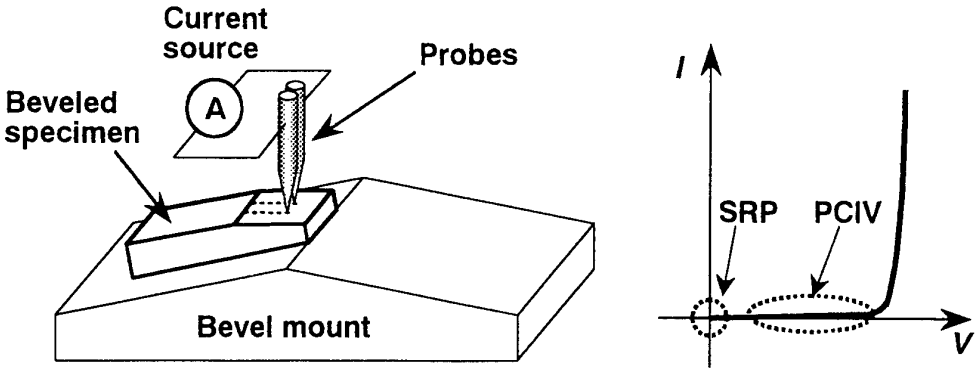


Fig.1 Schematic illustration of PCIV measurement. PCIV uses two probes as SRP, but uses a constant current source. PCIV measures higher voltage compared to SRP.

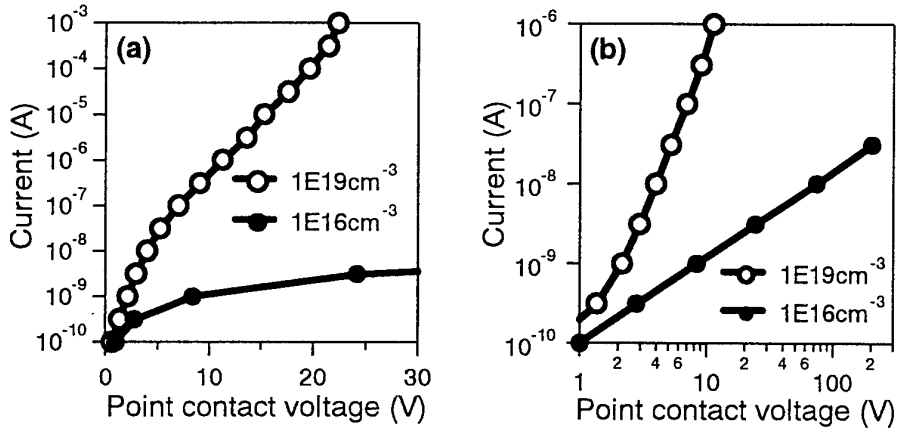


Fig. 2 Current voltage characteristics of point contact to 4H-SiC. Between 10^{-9} to 10^{-7}A, point-contact voltage changes almost linearly.

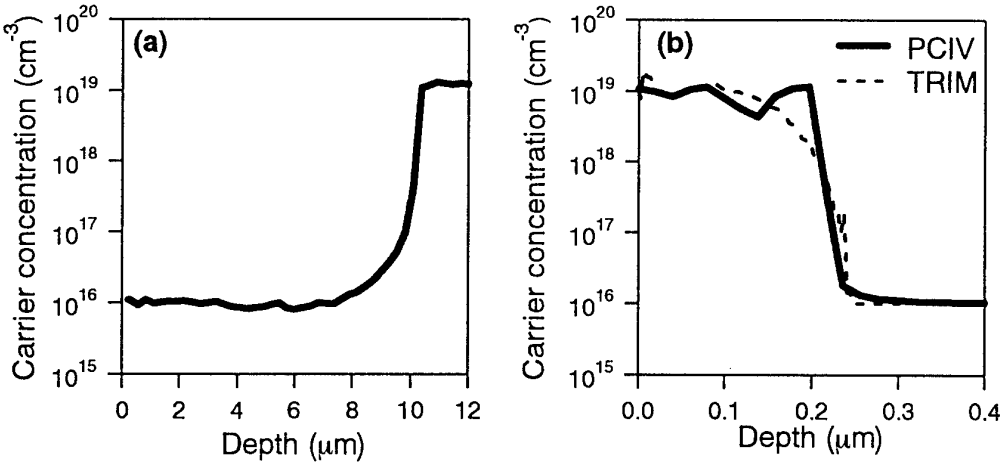


Fig. 3 Doping profile of (a) n^-/n^+ 4H-SiC substrate and (b) P implanted layer obtained by PCIV. In (b), simulated curve by TRIM is also shown.

Thermal conductivity and acoustic characterization of porous SiC

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ABSTRACT

Substrates were half-masked during anodization so that an epitaxial layer may be grown directly on both conventional 'STD' and porous 'PSC' substrates for comparison purposes. [1]. We will report on ultrasonic investigations of acoustic wave transport through both the porous surface regions and overgrown films on both as-received and porous surfaces. Both transmission and reflection measurements have been made. Acoustic inspection, in the frequency range of a few hundreds of MHz, is recognized as an advanced, non-destructive method for testing electronic materials for state-of-the-art microelectronic applications. Typical goals of acoustic imaging are to resolve and characterize internal bulk defects, delamination in packaged devices, and thin dielectric film metrology. Traditional Scanning Acoustic Microscopy (SAM) involves the use of peak amplitude information acquired while raster-scanning over a sample, to produce horizontal cross section images. One of important SAM features is a possibility to perform Tomographic Acoustic Micro Imaging (TAMI) where the entire image can be split into individual cross-sectional scans, analogous to physical sectioning of the sample.

We performed SAM in the TAMI mode to characterize and compare the elasto-mechanical properties of two 6H-SiC (0001)Si face off-axis wafers [2] SiC wafers prepared to be half control, half nanoporous by surface anodization utilizing an electrochemical cell, details of which are presented elsewhere [2]. Each wafer was processed to create a 3 μm or 12 μm thick porous layer on half of the substrate. With this approach the standard sample (STD) and porous sample (PSC) are on the same wafer. SAM was performed using the commercially available UHR-2000 system from Sonix, Inc. Measurements were performed at an operating frequency 260MHz in the pulse-echo mode. We also compared reflected and transmitted pulses at 75MHz frequency. The result of the TAMI scan taken on the wafer with the 12 μm thick porous layer is presented in Figure 1. The vertical line shows a border between the PSC (left) and STD (right) part of the wafer. Besides various micro-defects at the center of the wafer, the most remarkable feature is an enhanced acoustic reflection from the porous side (more white contrast). In different places on the wafer, the PSC displayed a 25-35% higher reflection

than the STD half. The scans correspond to the acoustic pulse reflected from the back surface of the substrate. In contrast, the SAM measured on the 3 μm thin PSC sample (not shown) reveals only minor variance between porous and reference halves. This difference is again towards a higher reflection from the porous side. We repeated the SAM study on the same wafers after deposition of 3-4 μm n-type SiC epitaxial layers on both full wafers. The result was very consistent with acoustic images of the pre-epi wafers. The 12 μm thick PSC region shows a higher acoustic pulse reflection compared to the STD region. Also, a minor difference was observed in a case of 3 μm porous layer.

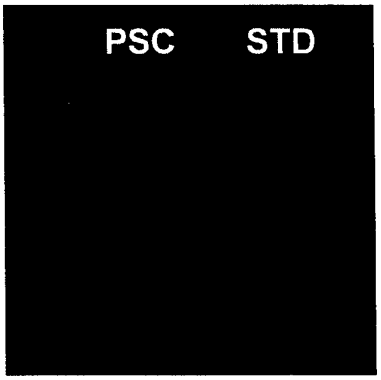


Fig. 1 TAMI scan taken on the wafer with 12 μm porous layer. Note that the porous region (PSC) has a lighter contrast indicating the material is of higher quality than the standard substrate region (STD).

Scanning thermal microscopy (SThM), which provides nondestructive, absolute measurements of the thermal conductivity (κ) with a spatial/depth resolution in the 2-3 μm range [3], was used to examine the room temperature κ of porous and non-porous SiC material. Wafers examined were processed in the same manner as described above. Thermal results were acquired by point-by-point type investigation on both halves of two samples labeled A and B. The porous film thickness was 3.5 μm (sample A) and 15 μm (sample B), respectively. For both investigated samples κ was found to be higher on the PSC region when compared to STD regions - about a 12% increase on sample A and 10% on sample B, respectively. Atomic force microscopy (AFM) investigation reveals that the influence of the surface roughness effects on κ cannot account for the observed behavior. A competition between a decrease in the phonon mean-free path and an increase of the specific heat of the porous material, with the predominant term being the specific heat, could account for these observations. The implications of these findings for device applications and design are being considered. These results are consistent with the SAM characterization, which was conducted independently. Results of these investigations will be presented along with initial thoughts on a model for the transport of phonons in PSC material.

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4H-SiC⇒3C-SiC Polytypic Transformation during Oxidation

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Abstract

We have observed a 4H-SiC⇒3C-SiC polytypic transformation in a highly doped n-type 4H-SiC epilayer following thermal dry oxidation. In addition to the 3.22 eV peak of 4H-SiC, cathodoluminescence spectroscopy (CLS) after oxidation revealed a spectral peak at 2.5 eV photon energy believed to correspond to 3C-SiC, that was not present in the sample prior to oxidation. To the best of our knowledge, the optical and structural results reported here are the first observation of a polytypic transformation of SiC (or any other semiconductor) as a result of thermal oxidation. CLS based on low energy electron nanoluminescence (LEEN) taken over a range of incident electron beam energies identifies the presence of localized states and their spatial distribution on a nanometer scale. With increasing excitation energy (E_B) the electron cascade and resultant generation of free electron-hole pairs occur at increasing depths, ranging from 25 nm at 1 keV to 150 nm at 4 keV for SiC's nucleon values and material densities. Electron-hole excitation rates peak at depth values (U_0) which are one-third of electron penetration depths. Fig. 1a depicts the 3.22 eV photon energy observed in the unoxidized sample, which peaks more sharply as E_B increases with further penetration into the epilayer. Emission at lower photon energies corresponds to a broad distribution of states in the band gap confined to the near-interface region. After four hours of oxidation followed by HF oxide stripping, the spectra changed dramatically as shown in Fig. 1b. A sharp 2.5 eV photon peak appears at all depths except 0-30 nm (0.5 keV $<E_B <$ 1 keV) from the metal/SiC interface, while a broad 3.2 eV photon peak slowly decays over the first 20 nm. The 2.5 eV emission at all depths probed indicates a substantial structural change occurring over hundreds of nanometers in the oxidized 4H-SiC sample. Cross section transmission electron microscope (XTEM) image of the as received sample shown in Fig. 2a indicates a uniform lattice structure confirmed by the 3.2 eV LEEN peak to be 4H-SiC. However, the TEM image shown in Fig. 2b of the sample that was oxidized for four hours and the oxide stripped reveals structural changes. Referencing from the top surface, discrete transformation bands (DTB's) of 4H-SiC and 3C-SiC can be seen propagating into the epilayer along the (0001) basal plane, with the thickness of each DTB gradually increasing with distance from the surface. High resolution TEM of Fig. 2c offers a closer look at one of the DTB's with the corresponding enlargement in the inset. The image shows seven Si-C bilayers with a 3C-SiC lattice periodicity sandwiched between 4H-SiC. The 3C-SiC layer is bounded by 4H-SiC structure. The transition boundary from the 3C-SiC to 4H-SiC at the top and bottom may offer clues to the mechanism that initiates the transformation.

We tentatively suggest that the observed polytypic transformation may be due to slipping of Si-C bilayers along the basal plane, which may be a strain relief mechanism due to the heavy doping ($1.7 \times 10^{19} cm^{-3}$) of the epilayer on a lightly doped substrate. Hallin *et al.*[1] used Raman spectroscopy to detect dopant-induced lattice mismatch in 4H-SiC, while Matsunami *et al.*[2] attributed the replication of stacking faults in a $\langle 11\bar{2}0 \rangle$ grown epilayer to difference in doping between an epilayer and a highly doped 4H-SiC substrate. Given the potential adverse effects in some applications, it becomes imperative that this observed transformation phenomenon in the crystal be critically investigated further.

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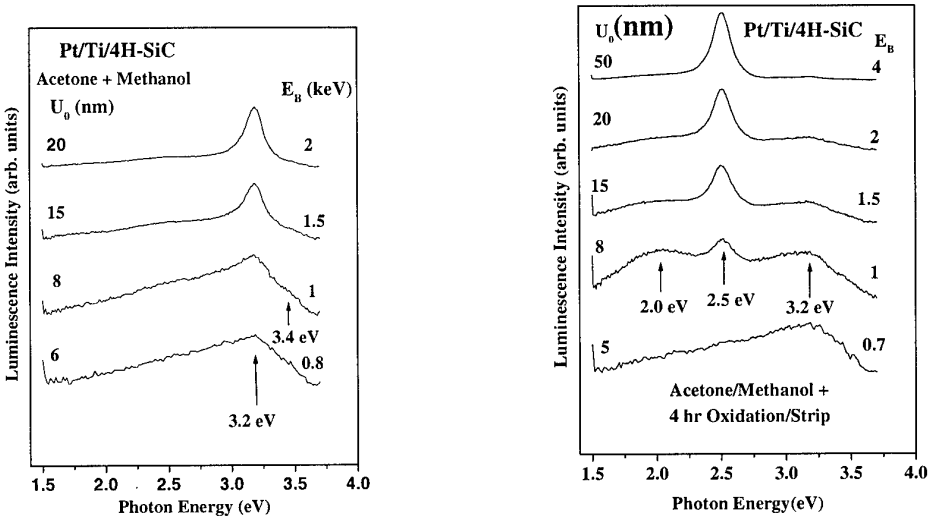


Fig. 1 **(a)** **(b)**

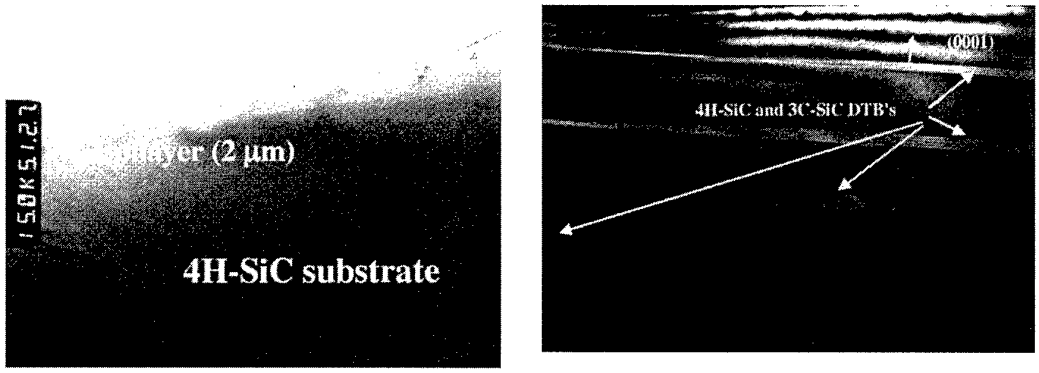


Fig. 2 **(a)** **(b)**

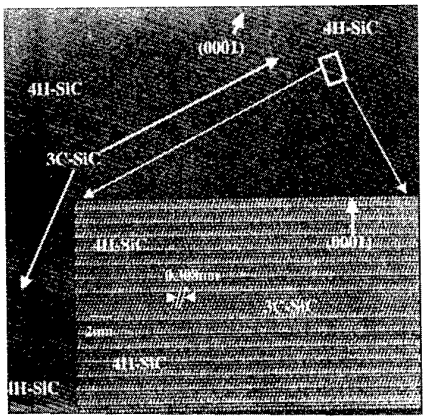


Fig. 2c

On the nature of E_1/E_2: a DLTS study of neutron irradiated n-type 6H-SiC

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The fluency-dependent properties and the thermal annealing behaviors of neutron-irradiation-induced defects in n-type 6H-SiC have been studied using deep level transient spectroscopy (DLTS). Deep levels NE_1/NE_2 at E_C-0.36~0.44 eV and NE_3 at E_C-0.51 eV are observed in DLTS measurement temperature range of 100~ 450 K. The energy levels and capture cross sections of NE_1/NE_2 and NE_3 agree well with that of the E_1/E_2 and E_i centers in electron-irradiated 6H-SiC, respectively. The present DLTS results reveal that concentrations of NE_1/NE_2 increase corresponding with decay of NE_3 in the isochronal annealing temperature range 400~ 650 K. The deep level centers NE_1/NE_2 are thought to be the same defects E_1/E_2. The NE_3 center is attributed to the same defect E_i that has been assigned as carbon vacancy V_C in electron-irradiated experiment. The present results of isochronal thermal annealing behaviors of NE_1/NE_2 support that E_1/E_2 should be differently charged states of carbon vacancy V_C, and argue against that E_1/E_2 were due to divacancy V_C-V_{Si}.

Hall mobility and carrier diffusion investigations in free-standing 4H-SiC epilayers

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Silicon Carbide (SiC) has become the semiconductor of choice for the new generation of semiconductor devices working under extreme conditions. However, still there are only few basic investigations performed on the electrical transport properties of SiC. Recently, the free carrier diffusivity as a key parameter governing plasma behavior in bipolar devices has been studied [1]. Extracted drift diffusivity data using the Einstein relation were compared to the Hall mobility data available in the literature. It was revealed that measured minority-hole diffusion mobility values are lower than majority-carrier (hole in particular) drift mobility values as well as significant difference exists in their temperature behavior. The results suggested that Hall mobility measurements have to be performed on the same set of samples for an appropriate comparison and to assure the structural quality of the material.

In this work we present temperature dependent Hall effect measurements on *n*-type 4H-SiC epilayers grown by chemical vapor deposition (CVD). Free standing 80 μm thick epilayers with extrinsic concentration $n_0 = 10^{15}$ and 10^{16} cm^{-3} were obtained by removing the substrate by polishing to avoid the influence from the heavily doped substrates in the measurements. Ohmic contacts on the epilayers were formed by implanting contact areas with multi-energy nitrogen doses along with subsequent annealing at 1650^{O} C and electrically contacting them with a silver paste. Extrinsic carrier concentration, carrier mobility and resistivity were deduced from measurement data obtained from Hall effect measurements using a van der Pauw configuration. The Hall scattering factor r_H was assumed to be equal 1. Experiments were performed in the temperature range from 70 to 450 K. The ionization energy and concentration of dopants governing the conductivity type as well as the degree of compensation were determined employing a least square fit of the charge neutrality equation to the experimental carrier concentration data. The charge neutrality equation was calculated numerically applying the material parameters for 4H-SiC.

The obtained Hall mobility values are equal to the highest values reported in the literature (930 cm^2/Vs at 300 K), which assures the structural quality of the material. Nevertheless, the earlier revealed differences remain between the ambipolar diffusion and the recalculated Hall mobilities temperature dependencies. The discrepancy can be attributed to the assumption of a Hall factor $r_H = 1$ in Hall effect measurements in *p*-type 4H-SiC, where its determination is limited due to a low hole mobility. Another explanation is that the minority-hole mobility (ambipolar diffusivity) may be reduced because of electron-hole scattering. Both consequences mentioned above could not be disregarded and also may come in parallel.

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Investigation of the Relationship between Defects and Electrical Properties of 3C-SiC epilayers

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Silicon carbide (SiC) is a promising material for electronic devices used with severe specification. Nowadays, 6H and 4H type SiC wafers are supplied commercially. However, their high price and difficulty to obtain large area prevent the industrialization of SiC devices. 3C-SiC heteroepitaxial growth on Si(100) substrate is one of the attractive ways which resolve problems mentioned. Many researchers have grown 3C-SiC on Si by atmospheric pressure chemical vapor deposition method (APCVD). However, the epilayers have many protrusions on the surfaces and poor surface morphology. As a result, APCVD grown 3C-SiC epilayers could not realize Schottky barrier diodes (SBD) with high reverse breakdown voltages, which is no more than several voltages. We have studied the growth mechanism of 3C-SiC by CVD and have found that the decrease of pressure during the growth brings about the suppression of the reaction between precursor in gas phase, resulting in the decrease of secondary nucleation [1,2]. Consequently, we can obtain atomically flat surfaces without protrusions and antiphase domains by low pressure CVD (LPCVD). The SBDs fabricated using the LPCVD grown epilayers showed good electrical properties, the ideality factor of 1.11 and the reverse breakdown voltage of 240 V [3]. Recently, we have grown 3C-SiC homoepitaxal layers on 3C-SiC thick free standing layers at 1500-1600 ℃, and have shown their excellent crystalline quality compared with those of heteroepitaxial layers. However, their SBD characteristics is not sufficient, compared with those on 6H and 4H epilayers. In this report, we study the influence of the defects in epilayers on the characteristics of Schottky barrier junction (SBJ).

Details of the heteroepitaxial growth and homoepitaxial growth of 3C-SiC and diodes fabrication have been described elsewhere [1,3]. 3C-SiC substrates with on-axis (100) surfaces, n type with carrier concentrations of 1×10^{17} cm^{-3} and the thickness of about 200 μm were supplied by HOYA corporation [4]. We have prepared 3C-SiC homoepilayers grown at different growth rates (2.5-8 μm/h). The properties of the grown layers was examined with a Nomarski differential interference contrast microscopy (NDIC) and the transmission electron microscope (TEM).

Figure 1 shows NDIC images of surfaces of homo-epilayers. The epilayers grown at the deposition rate of 2.5 μm/h and 8 μm/h are shown in Fig. 1(a) and (b), respectively. Macro steps of over 100 nm height and the terrace of less than 0.1 mm width were formed on the surfaces of the epilayers at high deposition rates. The density of macro steps increased with increasing the deposition rate. In order to investigate the origin of the macro steps, the TEM observation of the homoepilayers grown at high deposition rate was carried out. The TEM image near the interface between the homoepilayer and the substrate is shown in Fig. 2. Many line defects (stacking faults, twins, etc) along <111> directions, which do not exist in the 3C-SiC substrate, were observed in the homoepilayer. Bahng et al. have reported that

macro steps consist of twin bands in the case of 3C-SiC heteroepilayers on Si [5]. Therefore, in the case of homoepilayers, macro steps seem to relate with defects which were observed in Fig. 2. In order to make clear the relationship between the macro step and SBJ characteristics, we fabricated SBDs on many samples with the different densities of macro steps and measured their SBJ characteristics. Figure 3 shows the reverse current-voltage characteristics of homoepilayers grown at the deposition rates of 2.5 and 8 μm/h, respectively. Because we used Schottky electrodes of 0.1 mm in diameter, Schottky electrodes contain at least one macro step in the case of epilayer grown at 8 μm/h. However, the I-V characteristics of the high deposition rate sample is superior to those of low deposition sample, in which Schottky electrodes do not contain macro steps. These results indicate that the macro step do not affect on the breakdown voltage, and the characteristics of SBJ s may be determined by other micro defects.

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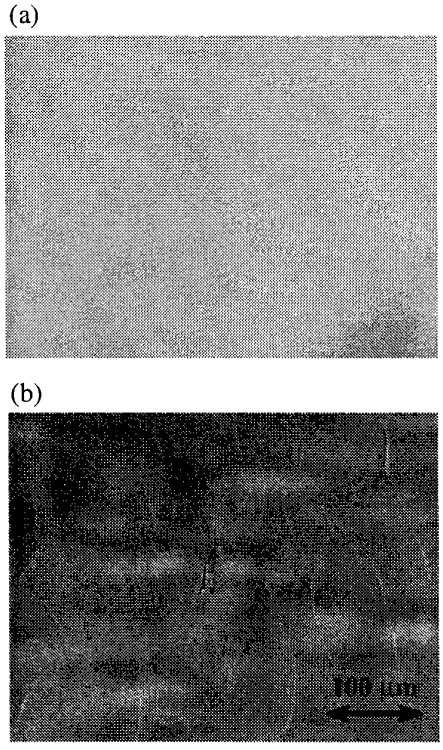


Fig. 1 NDIC image of the surface.
(a) 2.5 mm/h (b) 8 mm/h

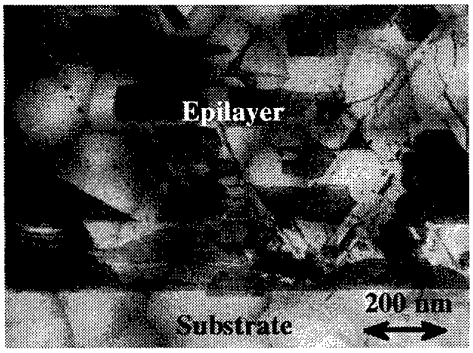


Fig. 2 TEM image of near the interface of homoepilayers and subatrates.

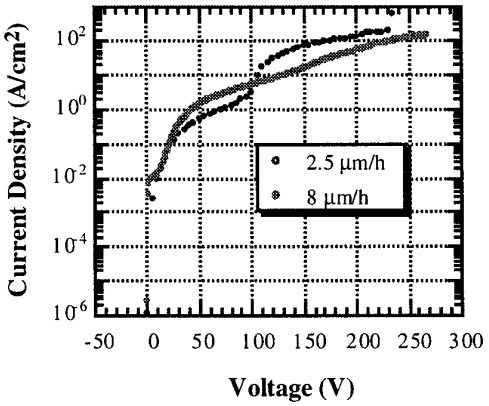


Fig. 3 The reverse I-V characteristics of SBD.

Suppression of Macrostep Formation in 4H-SiC Using a Cap Oxide Layer

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Ion implantation is the only planar, selective-area doping technology available for SiC due to the extremely low diffusion coefficients of dopants. Hence it is necessary to anneal at high temperature for the sufficient activation of dopants, so that macrosteps were easily formed on the surface of 4H-SiC device. Many researchers [1,2] have investigated several methods to suppress macrostep formation during the high temperature activation anneal using silane gas or carbon mask, since such surface ruggedness is known to deteriorating the channel mobility[3].

In order to suppress the macrostep formation we adopted a cap oxide layer thermally-grown or CVD-grown, which is expected to act a role of obstructing the mass flow between the surface of SiC single crystal and the ambient gas. Thermal oxide of 10nm and 50nm thick were grown on SiC wafers to examine the thickness effect of the cap layer. 4H-SiC wafers, supplied from Cree, U.S.A., with an off axis of 8° towards $<11\bar{2}0>$ were used as starting materials. The non-implanted and Al, B implanted wafers were annealed for 30~40min at the temperature of 1500, 1600, 1700°C, respectively. The samples were loaded into SiC capped graphite crucible and then heated under argon atmosphere. The characterization of surface roughening as well as formation of macrosteps was done using atomic force microscopy (AFM).

The annealing at 1600°C for 30 min resulted in a very clear and well-aligned macrostep structure in the SiC wafers with 10nm thick thermal oxide, as shown in Fig. 1(a). The thermal oxide cap was not found after the heating cycle, which implies that 10nm oxide layer was thin enough to be removed away during the initial stage of annealing and then the surface modification has occurred. It was revealed on the other hand that thicker cap oxide could suppress macrostep formation. Fig. 1(b) shows that no macrostep was found in the sample with a thermal oxide of 50nm thick after the same thermal history of annealing. The thermal oxide layer which was etched out chemically for AFM investigation still remained, even though it was partly damaged and partly evaporated, at the surface of SiC single crystal after the annealing. It means therefore that macrosteps could not be formed at the surface of the off-axis grown SiC single crystal as long as the cap oxide remains during whole the period of high temperature annealing and thus obstructs the mass flow between SiC surface and gas atmosphere. The small pits on the SiC surface in Fig.1(b), which seems to have been created

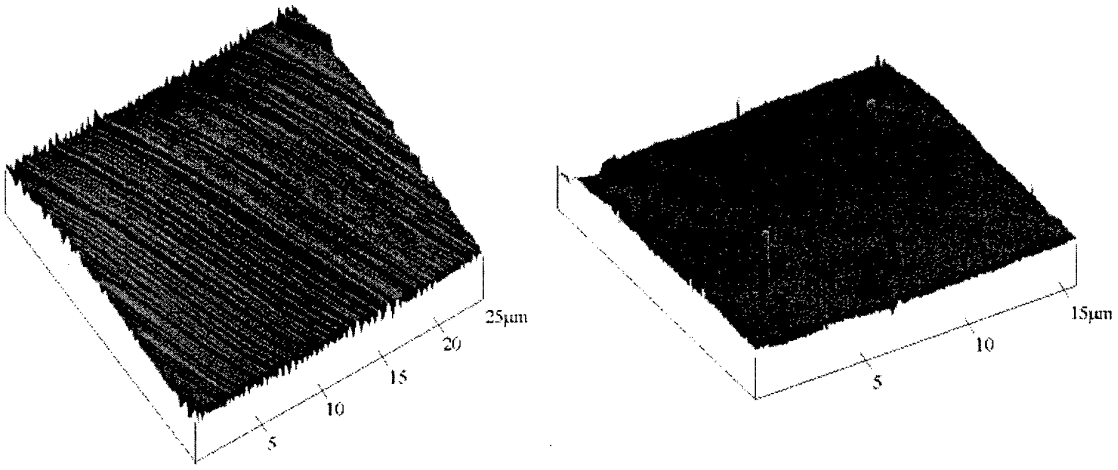


Fig. 1. Atomic force micrographs of high temperature annealed SiC surface. The samples were annealed at 1600°C for 30min with thermal oxide layers (a) 10nm thick and (b) 50nm thick, respectively. A micrograph (a) shows clear macrostep formation, otherwise (b) shows only small height steps.

during the growing of thermal oxide, are under investigation.

The stability of the cap oxide and the surface modification of SiC surface will be presented with respect to the annealing temperature and atmosphere. The characterization of high temperature annealed SiC surface with a thick(~1μm) CVD-grown oxide layer was also investigated and will be presented. The oxide formed and lithographed easily by semiconductor processing can be a good cap layer for suppressing macrostep formation during the high temperature annealing of silicon carbide.

Acknowledgement

The authors would like to thank Mr. S. Y. Han at Pohang University of Science and Engineering (POSTECH) for the help of AFM measurement. This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE(Ministry of Commerce, Industry and Energy), Korea.

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Influences of Implantation Temperature and Dose Rate on Secondary Defect Formation in 4H-SiC

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B^+ and Al^+ are used for p-type ion implantation and both ions have advantages and disadvantages, each other. For example, Al^+ implanted layer is easy for electrical activation and shows little redistribution of dopant by diffusion during annealing but Al^+ implanted pn junction has larger leakage current than B^+ implanted one [1]. The difference of reverse properties between B^+ and Al^+ implanted pn junctions may be related to the secondary defects formed during annealing. We studied the difference of secondary defect formation between B^+ and Al^+ implanted layers by Transmission Electron Microscope (TEM) and showed that at the same volume concentration of implanted ion, density of secondary defect in Al^+ implanted layer is higher than that in B^+ implanted layer. On the contrary, mean defect size in B^+ implanted layer is larger than that in Al^+ implanted layer [2]. These secondary defects are extrinsic dislocation loops composed of agglomerated interstitials formed by implantation [3]. The volume of the interstitials stored in dislocation loops roughly coincides the amount of implanted ions and this correlation doesn't depend on ion species [2]. This result means that B^+ and Al^+ implanted layers have different agglomeration of interstitials, which cause the differences of defect size and density between them. The activation energies of secondary defect formation were estimated for both B^+ and Al^+ implanted layers but they are not so different [4]. These activation energies are the self-diffusion activation energy of Si in SiC. From these results, we speculate the difference of secondary defects formation between ion species does not depend on the diffusion of interstitials in implanted layer but is owing to its initial nucleation, which means the secondary defect formation is strongly dependent on as implanted state. In this paper, we show the influences of dose rate and implantation temperature on secondary defect formation in Al^+ implanted 4H-SiC to clear this speculation.

N-type 4H-SiC wafers with a 10 μm thick n-type epilayer, obtained from Cree Research Inc., were used for implantations. The donor concentration of epilayers is about $5\times10^{15}cm^{-3}$. Single energy Al^+ implantations at 750keV were performed, using microwave multiply charged ion source and radio frequency quadrupole (RFQ) accelerator. This implantation system permits us high dose rate ion injection of 100 μA. While low dose rate implantation at 8 μA was also performed as a reference. Implantation temperatures were room temperature (RT) and 1000℃ for both dose rate conditions. Post implantation annealings were performed in Ar ambience at 1700℃ for 5min using lamp heated furnace.

Figure 1 shows the cross-sectional TEM images obtained from Al^+ implanted and post-annealed

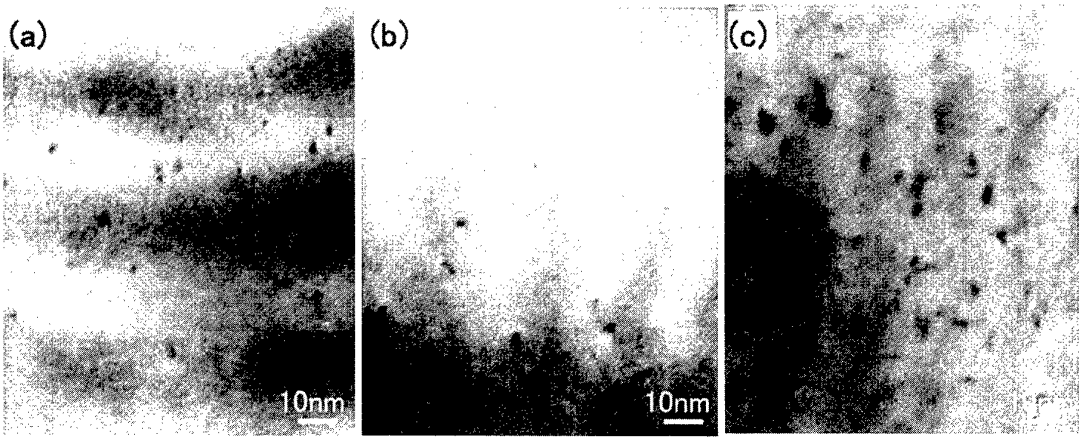


Fig. 1 Cross-sectional TEM images of Al^+ implanted 4H-SiC. Post-annealing was performed at 1700℃. Dose rates and implantation temperatures are (a) 8 μ A at RT, (b) 8 μ A at 1000℃ and (c) 100 μ A at RT.

epilayers. Dose rates and implantation temperatures are (a) 8 μ A at RT, (b) 8 μ A at 1000℃ and (c) 100 μ A at RT, respectively. Observations are along <1120> zone axis. In these TEM images, secondary defects are shown as black dots. At the dose rate of 8 μ A, secondary defects are reduced when implantation temperature is raised from RT to 1000℃. The mean defect size is also grows from 2.9nm to 4.1nm. On the contrary, defect density increases when dose rate is raised from 8 μ A to 100 μ A at RT. These results mean that during high temperature implantation, in-situ recombination of interstitials and vacancies is enhanced and supersaturation of them is reduced, which leads to the suppression of nucleation for secondary defect formation. As the result, the density of secondary defects decreases but the mean size of them grows. While, more interstitials and vacancies are survived at the high dose rate implantation than that of low dose rate condition and the increased supersaturation of interstitials causes the enhancement of nucleation of secondary defect formation. In the case of 100 μ A at 1000℃, TEM image is similar to Fig. 1 (c). The increase of interstitials by high dose rate implantation is too high to effectively recombine at 1000℃ during implantation. As the result, a lot of interstitials are remained after implantation, which leads to high density of secondary defect formation. High temperature implantation is effective only for low dose rate implantation to reduce the secondary defect formation and initial nucleation is also a key for secondary defect control.

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Acknowledgement

This work was performed under the management of FED as a part of the MITI NSS Program (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

Aluminum and boron diffusion into a-face SiC substrates

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Diffusion as a method of doping SiC has been used for a long time[1]. However, only recently it has been demonstrated that this method might be an alternative approach to ion implantation for the formation of selectively doped regions[2]. Diffusion became possible due new technology of graphite mask formation which enables this mask to sustain the high temperatures required for the diffusion process. Since, during selective doping through a mask lateral diffusion occurs as well, diffusion mechanisms and the kinetics of diffusion along the direction perpendicular to *c*-axis (*a*-face) must be studied in detail. Furthermore, because of silicon carbide crystal anisotropy, it is reasonable to expect a difference in impurity diffusion along different crystal orientations.

In this paper, we present a study of boron and aluminum diffusion into 4H-SiC substrates, cut from the same boule, both perpendicular and parallel to *c*-axis.

Single crystal wafers of n-4H-SiC from Bandgap Technologies, Inc. were used, having orientations of (0001), $(000\bar{1})$ and $(1\bar{1}00)$, and background carrier concentration of $4.1\text{x}10^{18}\text{cm}^{-3}$. Boron and aluminum diffusion were carried out simultaneously in argon ambient using an induction heating vertical quartz chamber with water-cooled walls. The temperature and time of diffusion varied from 1900 to 2000°C and from 5 to 15 min, respectively. A graphite crucible with a mixture of silicon carbide powder, elemental boron and aluminum carbide powder (source of the doping atoms) was used. The uniform temperature distribution with minimal gradients and equilibrium SiC vapor pressure were created inside the crucible to avoid undesirable evaporation and/or epitaxial growth during diffusion.

In order to accurately measure the depth profiles of the diffused impurities, secondary ion mass spectroscopy (SIMS) was performed. SIMS data of Fig.1 show that after diffusion at 1900°C for 10 min, both boron and aluminum atoms diffuse about two times faster along the direction

perpendicular to *c*-axis than parallel to it, while the impurity diffusion along the $\langle 0001 \rangle$ direction is practically the same as that along the $\langle 000\bar{1} \rangle$ direction.

Note, that the aluminum profile in the a-face substrate has a very shallow surface region with higher atomic concentration, while Si- and C-terminated substrates have lower Al concentration in the surface region. Possible reasons for this phenomenon are discussed in the presentation.

Acknowledgments

The authors are grateful to Dr. J. Baker for SIMS measurements which were carried out in the Center for Microanalysis of Materials, University of Illinois, partly supported by the U.S. Department of Energy under grant DEFG02-96-ER45439.

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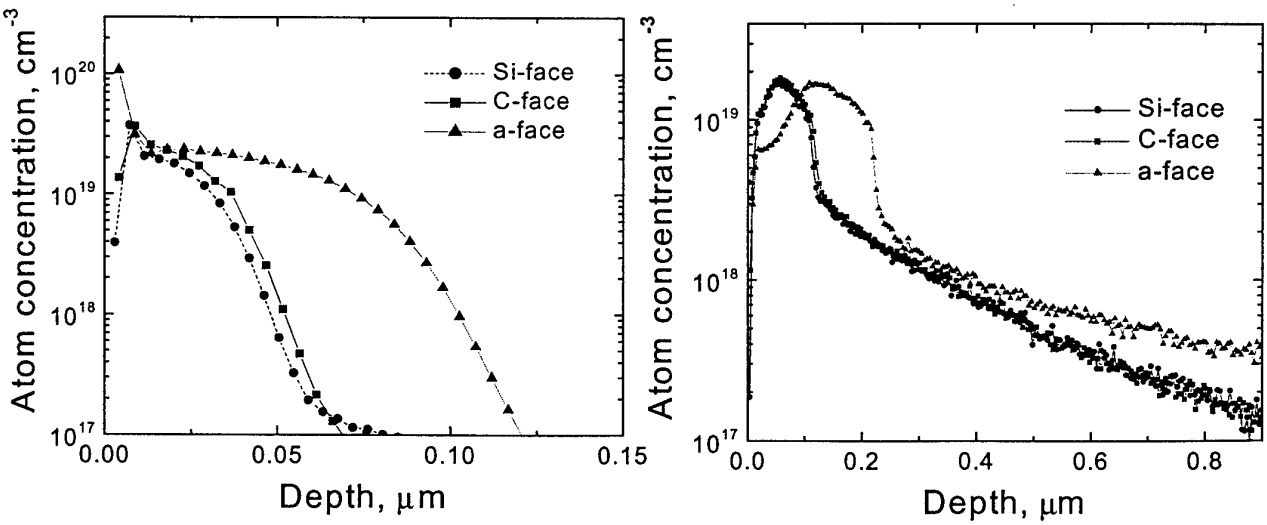


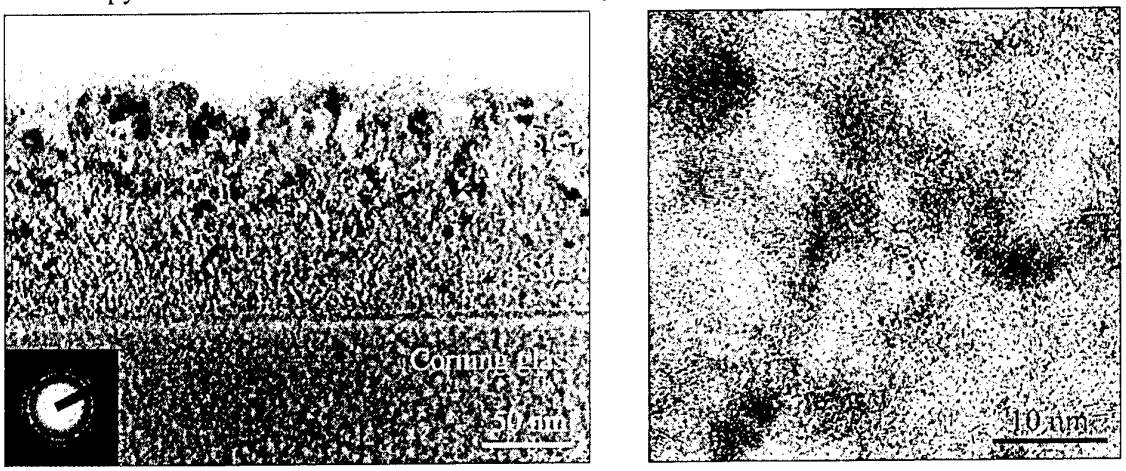
Fig.1. SIMS measurements of Al (left) and ^{11}B (right) vs. depth in 4H-SiC substrates after diffusion at 1900°C for 10 min

Laser Crystallization Mechanism of Amorphous SiC Thin Films on Glass

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Silicon carbide is an ideal material for high-power, high-frequency and high-temperature electronic devices. For these applications nanocrystalline, polycrystalline, or single-crystalline SiC films are required. Usually, crystalline SiC films are produced by CVD either at high substrate temperature or followed by a high temperature annealing step in which amorphous SiC is crystallized. These processing technologies have the disadvantage that large area and low cost materials such as glass cannot be used as substrates. However, high temperature annealing can be avoided by pulsed laser irradiation of amorphous material.
Amorphous, hydrogen free, SiC films with 100-400 nm thickness were produced on glass (Corning 7059) by pulsed laser deposition from a stochiometric, polycrystalline SiC target. The ablation was carried out using a pulsed KrF excimer laser (248 nm, 25 ns) at a repetition rate of 10 pulses per second, a pulse energy of 250 mJ, a laser fluence of approximately 2 J/cm² on the target surface with about 400°C substrate temperature. The amorphous character of the deposited films was confirmed by Raman measurements and transmission electron microscopy. The Si to C atomic ratio determined by EDX and RBS analysis is close to 1:1.



a) b)

Figure1: a) Cross sectional TEM image of laser crystallized SiC layer on a glass substrate (inset: selected area diffraction (SAED) pattern from the layer); b) corresponding high-resolution TEM image

The laser crystallization was carried out by single shots of the KrF laser in air at ambient pressure. A fluence in the range of 0.1 to 1 J/cm^2 was applied on a 5x2 mm^2 area of the amorphous film. A fluence above 250 mJ/cm^2 leads to crystalline SiC.
The crystalline character of the laser crystallized films above the crystallization threshold of 250 mJ/cm^2 was investigated by optical microscopy, Raman measurements, RBS

investigations, and transmission electron microscopy. Figure 1 shows cross sectional TEM images, Fig. 1b) a HRTEM image of a laser crystallized SiC layer. From the TEM images we conclude that the SiC crystallites have diameters of 10 to 30 nm. The corresponding selected area diffraction (SAED) pattern taken from the layer shows rings of polycrystalline material, the spacings of which fit to cubic silicon carbide. Additionally, from high resolution images a distance between atomic planes of 0.25 nm was found which corresponds to (111) planes distance (0.252 nm) in cubic SiC. Fluences well above the melting threshold lead to a segregation of the material.

The crystallization process was studied by time resolved reflection and transmission (TRRT) measurements during laser irradiation. A 10 mW cw He-Ne laser (633 nm) was used to probe the sample reflectivity and transmissivity. The He-Ne laser beam power was measured with a fast photodiode (2 ns time resolution) and registered by an oscilloscope. Since the transmissivity and reflectivity of liquid SiC is expected to differ remarkably from that of solid SiC, this method appears suitable to detect the liquid phase on the sample surface.

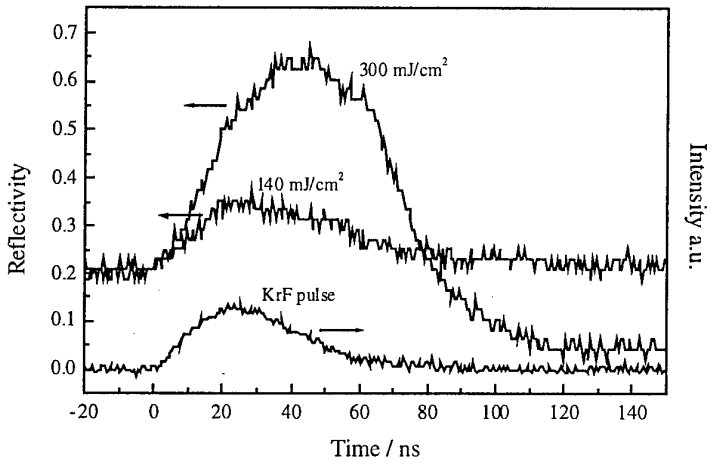


Figure 2: TRR curves and the crystallization pulse

Figure 2 shows the reflectivity results of TRR measurements during excimer laser irradiation with 140 mJ/cm^2 and 300 mJ/cm^2. In the low fluence irradiation curve the reflectivity increases weakly which is interpreted as a film heating. After the irradiation the reflectivity recovers to the previous value, so that no permanent modification of the film was detected. For the high fluence irradiation the reflectivity increases to 0.6. The high reflectivity value remains for approximately 50 ns, which is longer than the irradiation pulse of 30 ns. After 120 ns the reflectivity reaches a permanent value lower than before corresponding to a permanent modification of the film. The laser pulse leads to a crystallization of the amorphous material. According to the TRR measurements the crystallites result from a metastable SiC melt existing for approximately 50 ns. These findings are unexpected because they are in contradiction to the equilibrium phase diagram of SiC in which no liquid phase occurs at ambient pressure.

The rather high reflectivity value of 0.6 during laser irradiation indicates a metallic character of the melt comparable to l-Si and l-Ge. To confirm the existence of a metastable SiC melt time resolved transmission and conductivity measurements are discussed.

Experimental and Computer Simulation Studies of Defects and Ion-Solid Interactions in Silicon Carbide

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The results of experimental and computer simulation studies on defects and ion-solid interactions in silicon carbide (SiC) will be presented. The interaction of energetic ions with SiC results in the creation of interstitial, vacancies, antisite defects, and defect clusters that interact to produce long-range structural disorder. Ab initio calculations and molecular dynamic (MD) simulations are used to determine defect formation energetics, defect production as a function of cascade energy, and the effects of cascade overlap. Ion-beam-induced disordering in single crystals of 6H-SiC has been investigated experimentally for wide range of ions (H^+ to Au^{2+}). The accumulation and recovery of disorder on the Si and C sublattices is determined, respectively, by Rutherford backscattering spectrometry (RBS/C) and $^{12}C(d,p)^{13}C$ nuclear reaction analysis (NRA/C) in channeling geometry.

Density functional theory has been used to study the formation and properties of native defects in 3C-SiC. It is found that the most stable configurations for interstitials are C-C and C-Si split interstitials along the <100> and <110> directions. Multi-axial channeling measurements indicate that Si and C interstitials are well aligned along the <0001> axis in 6H-SiC, consistent with DFT results. Along other axes, the rate of C disordering is higher than for Si disorder, which is consistent with MD simulations that show lower displacement energies for C relative to Si. The results of MD simulations for the net displacements and antisite defects produced by a Si primary knock-on atom (PKA) are shown in Fig. 1 as function of PKA energy. The number of net displacements is defined as the sum of the total number of interstitials (or vacancies) and antisite defects. The number of C Frenkel pairs is nearly 3 times the number of Si Frenkel pairs. Similar behavior is observed for C PKAs. Antisite defects are produced by nearest-neighbor replacements during the collisional phase and some random interstitial-vacancy recombination during the subsequent relaxation phase.

MD simulations have also shown that large disordered domains, including amorphous clusters, are created in the cascades produced by Au PKAs; whereas, Si PKAs generate only small interstitial clusters, with most defects being isolated single interstitials and vacancies distributed over a large region. These predictions are in agreement with the interpretation of experimental results, as shown in Fig. 2, where the relative disorder on the Si sublattice in SiC at the damage peak is shown as a function of dose in displacements per atom (dpa) for 2 MeV Au^{2+} and 550 keV Si^+ ions at low temperatures. These

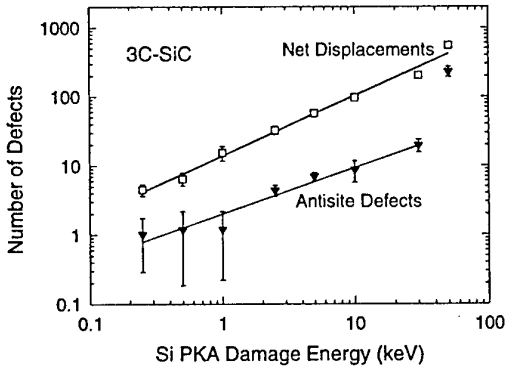


Fig. 1. Net displacements and antisite defects as a function of Si PKA energy.

results suggest that the higher disordering rate for Au^{2+} is associated with a higher probability for direct-impact amorphization or cluster formation during the cascade process.

MD simulations with 10 keV Si PKAs have been employed to simulate cascade overlap, damage accumulation and amorphization processes in 3C-SiC. A total of 140 cascades were overlapped in an MD simulation cell containing 40,000 atoms. At low dose, damage is dominated by single interstitials and small clusters consisting of interstitials and antisite defects, and their concentration increases with increasing dose. The coalescence of small and large clusters at higher dose is an important mechanism leading to amorphization in SiC, and the homogenous nucleation of small clusters at low dose is consistent with the homogenous amorphization process that is observed experimentally under similar irradiation conditions. Under these conditions, the driving force for irradiation-induced amorphization is the accumulation of both interstitials and antisite defects. The relative disorder as a function of dose shows a sigmoid behavior, as shown in Fig. 3, which is in good agreement with experimental measurements (Fig. 2). High-resolution TEM image simulations of defect accumulation processes in the MD simulation cell have been conducted to reveal the microstructural changes due to cascade overlap processes, as shown in Fig. 4, and the results are in good agreement with experimental HRTEM images.

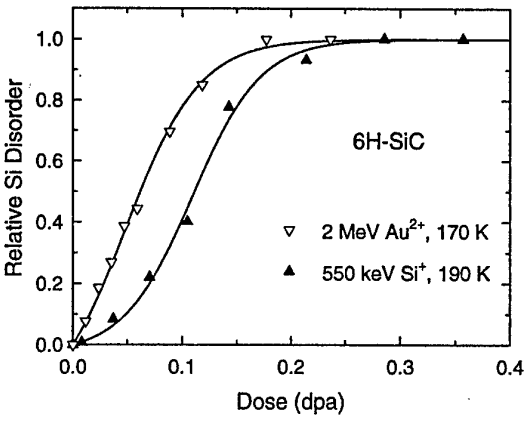


Fig. 2. Relative disorder as a function of dose in 6H-SiC irradiated by 2.0 MeV Au^{2+} at 170 K and 550 keV Si^{+} at 190 K.

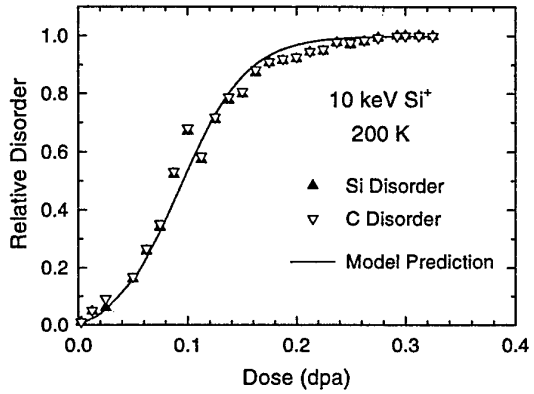


Fig. 3. Relative disorder in SiC based on MD simulations employing 140 cascades.

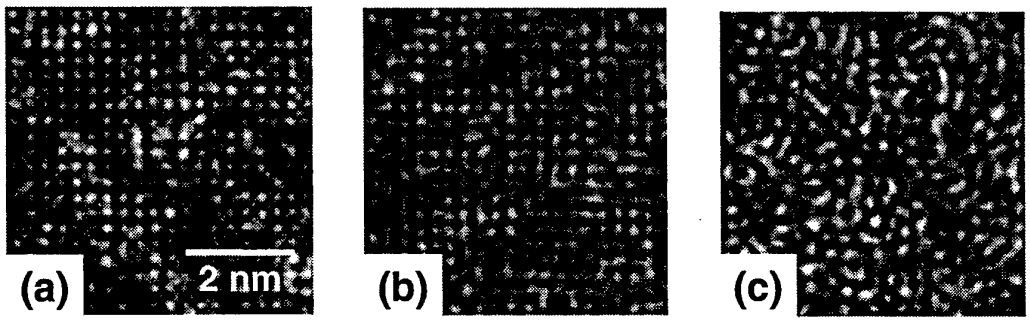


Fig. 4. HRTEM image simulations of MD damage states from accumulated cascade overlap: (a) 0.06 dpa, (b) 0.13 dpa, and (c) 0.28 dpa

ENHANCED DOPANT DIFFUSION EFFECTS IN 4H-SILICON CARBIDE

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ABSTRACT

Although doping of SiC by diffusion techniques is impractical (due to prohibitively slow diffusion rates of most common dopants), diffusion of implanted dopants at high anneal temperatures is more significant than is often considered to be the case. In simple single species implants, substantial implant profile broadening and implant tail lengthening have been observed - the latter linked to Transient Enhanced Diffusion (TED) - during high temperature annealing. Such effects are enhanced by the relatively high concentrations of lattice defects that occur in implanted SiC (due to the crystal lattice structure), and the high implant doses required (due to low activation levels). However although most realistic device structures contain more than one single implant species (e.g. complex n-p-n structures of bipolar devices), there is little published work on the effects of implant damage and dopant diffusion in such complex structures. In this paper, we present an experimental study of enhanced dopant diffusion in nitrogen/boron implanted n-p-n structures and propose a simple model which can be used to predict the extent of dopant diffusion (or migration) observed in such cases.

In order to investigate these effects, a detailed experimental study of nitrogen/boron interaction effects was performed. An implantation matrix of nested (one within the other) implants with varying nitrogen and boron implant profiles was fabricated and annealed over a range of temperatures between 1300C and 1700C. One resultant set of SIMS data obtained for implanted nitrogen into an implanted boron p-well region as a function of the anneal time at 1600C is shown in Figure 1. The boron implant fabrication schedule used was:- 20keV $1x10^{13}cm^{-2}$, 50keV $2x10^{13}cm^{-2}$, 100keV $3x10^{13}cm^{-2}$, 160keV $3x10^{13}cm^{-2}$. The wafers were then cleaned and re-patterned for nitrogen implant at the following energies and doses:- 20keV $8x10^{14}cm^{-2}$, 40keV $8x10^{14}cm^{-2}$ and 60keV $2x10^{15}cm^{-2}$. All implants were performed at room temperature. Under these conditions, boron and nitrogen diffusion in excess of that seen in equivalent single species implantation was observed. Figure 2 highlights the unexpectedly strong nitrogen diffusion found in the SIMS data of Figure 1, previously presumed to be due to the effect of implant damage from the earlier boron implant. Although quantifying the degree of nitrogen diffusion post-experiment is straightforward (by using a modified 'effective diffusion constant'), predicting the extent of such enhanced diffusion prior to device processing is difficult as it depends on the exact nature of the whole implant and anneal sequence. Complex calculations which model the interaction of the substrate crystal lattice with the incoming ion species and the effect of subsequent annealing can be performed by molecular dynamics techniques but are computationally expensive and impractical for all

but a limited number of special cases. There is thus a need for simple tractable models which enable predictive calculation of these enhanced diffusion (redistribution or migration) effects of both n- and p-type dopants in SiC in complex multi-species implant structures.

In this paper a simple and elegant physical model for these enhanced diffusion phenomena as observed in Silicon Carbide is proposed. The model allows possible mechanisms for dopant movement (or migration) within Silicon Carbide to be examined - based on the initial state of an ion implanted substrate. It will be shown that an accurate prediction of complex implanted multi-species profiles can be obtained by simple models detailing the interaction between ion species as a function of temperature. The proposed model accurately predicts the resultant implanted ion redistribution profiles following high temperature annealing. Additionally, isolated box implant profiles follow an expected modification profile consistent with implant depletion widths. Previously published findings and the extensive new experimental data presented here correlate and agree well with the predictions of our new model. Additionally, our new model predicts the temperature behavior of a wide range of published experimental results and also accounts for the time dependant behavior of the ion redistribution during the annealing process. To date, no other TED model or analytical process as published in the literature explains the high temperature annealed ion redistribution in SiC as well as the model proposed in this paper.

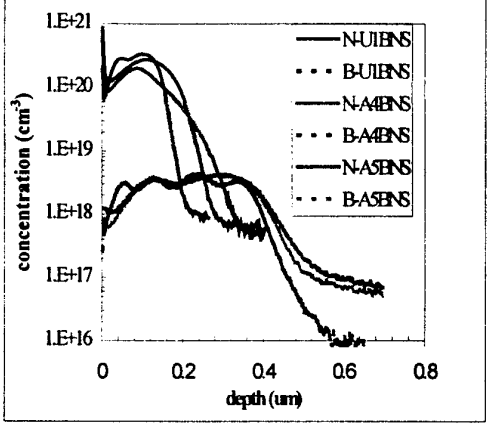


Figure 1: SIMS data showing nitrogen and boron profiles after anneal at 1600C for 10mins (sample A4BNS) and 20 mins (sample A5BNS) respectively. For comparison an unannealled sample (U1BNS) is also shown.

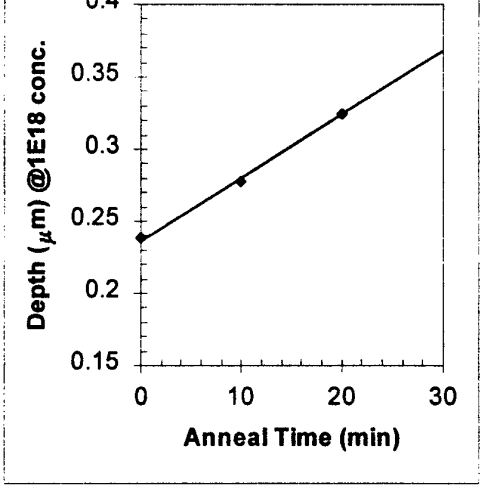


Figure 2: Nitrogen implant depth vs annea time at 1600C (note: line is guide to the eye only)

Ion implantation – tool for fabrication of advanced 4H-SiC devices.

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SiC is one of the most promising semiconductors for manufacturing electronic devices with stable operation in extreme environments. One major for device fabrication is the high resistivity of the p-material since the acceptor concentration is limited by the solubility in SiC. Nonequilibrium method - of ion implantation doping (ID) of SiC allows to introduce acceptors with concentrations exceeding their solubility limit in SiC. However, the task of the acceptor activation is not yet solved causing the formation of high resistive p-layers [1,2]. It has been shown that ID of SiC with Al followed by high temperature annealing allowed to produce p^+n junctions where ID p^+-layers did not introduce additional resistance in the device structures [3]. Recently, beneficial influence of short thermal annealing on structural perfection of Al ID 4H-SiC epitaxial layers grown by chemical vapor deposition (CVD) was revealed, for instance by a rise of the hole diffusion length values [4]. In this work the advantages of high dose Al ID in 4H-SiC CVD epitaxial layers followed by short high temperature annealing for high voltage diodes as well as in the detectors of UV radiation and α-particles were investigated.

4H-SiC CVD epitaxial layers with thickness 25 μm and the concentration N_d-$N_a = 4x10^{15}$ cm^{-3} were grown on commercial 4H-SiC wafers. Al ions with energy 150 keV and dose $5x10^{16}cm^{-2}$ were implanted in CVD layers followed by short thermal annealing for 15 s at 1700 °C in Ar ambient. Regular Cr ohmic contacts to n- as well Al regular and semitransparent contacts to p^+- SiC were produced by thermal vacuum evaporation. P^+n mesa structures with different areas were formed by reactive ion plasma etching.

The structural perfection in lateral and axial directions of the CVD layers before and after Al ID p^+n junction formations were investigated by scanning electron microscopy (SEM) using electron beam induced current (EBIC) imaging, by secondary ion mass spectrometry (SIMS) and SIMS imaging in Al ions, by x-ray photoelectron spectroscopy (XPS) and real color cathodoluminescence (CCL) mode in SEM. Diffusion lengths of the holes (L_p) were determined by SEM using standard treatment of EBIC signals. Electrical properties of the CVD layers and devices were revealed from capacitance-voltage as well as from forward and reverse current-voltage characteristics measured under different conditions. The produced structures were irradiated with 4.5-5.5 MeV α-particles and the pre-amplified signal was registered at 20 °C. The spectral photosensitivity characteristics of Al ID 4H-SiC p^+nn^+ structures were studied in the range of incident energies 2.8–6 eV under short-circuit condition for the photocurrent.

4H-SiC p^+nn^+ diodes with p^+n junction position of 0.6 μm and the area of $1x10^{-3}$ cm^2 exhibited forward current density of $3x10^3$ A cm^{-2} at 12 V voltage drop and differential resistance of $3x10^{-3}$ Ω cm^{-2}. The small differential resistance value was stimulated by a low resistivity of Al ID p^+-layers and ohmic contacts as well as partial modulation of the n-base region by injected holes due to the increase in L_p value. This effect is probably due to the

improvement of the structural quality CVD epitaxial layers after Al ID p^+n junction formation causing the absence of recombination centers of holes in Al AD p^+- layers and in CVD layers close to p^+n junction position [5]. Breakdown voltage of 1.7 kV limited by CVD structural imperfection were reached for these diodes, that had stable operation up to 500 °C.

Shallow Al ID p^+n junction position and small leakage currents, less than 10^{-8} A, were advantageous for the work of α-particle detectors. It has been revealed that these detectors exhibited the extremely low background levels due to the absence of the "dead window" like Schottky barriers. The amplitude permission values were 10% determined in spectrometric regimes.

Also UV photodetectors based on Al ID 4H-SiC p^+n junctions combine the advantages of photosensitive Schottky barrier structures and structures grown by epitaxy. The collection efficiency of nonequilibrium charge carriers nearly 100% was observed for this detectors [6]. The spectral sensitivity range of the photodiodes corresponded to 2.8-6 eV, peaking at 4.9 eV. This range is near to the spectrum of relative effectiveness of various wavelengths in bactericidal UV radiation, which indicates novel application areas for a SiC detector.

Thus, it has been shown that Al high dose implantation with short high temperature thermal annealing ensured the creation of narrow low resistive p^+ layers which can be used as effective hole injected regions in SiC devices. Improvement of SiC structural quality near Al ID p^+n junctions increased the Lp value that provided partial modulation of the n-base that reduced the resistance in device structures.

Influence of the Al ID with subsequent annealing on the quality of 4H-SiC CVD epitaxial layers will be discussed. Electrical and optical characteristics of high voltage diodes, spectral data and quantum efficiency of the photodetectors in temperature range 78-360 K, the collection efficiencies and counting characteristics of detectors of α-particles based on Al ID 4H-SiC p^+n junctions will be presented.

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This work was supported mainly by INTAS project 97-2141.

A comparative study of high temperature Aluminum post-implantation annealing in 6H and 4H-SiC, non-uniformity temperature effects

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Ion implantation, an indispensable technique to locally dope silicon carbide (SiC) still presents many problems in particular for p-type zone creation. High ionization energy of dopants imposes to raise the implanted dose above the amorphisation threshold for room temperature implantations. Structure recrystallization and electrical activation of dopants, i.e. their incorporation in active SiC atomic sites, require high temperature annealing, about 1700°C in special configuration, with an overpressure of silicon and carbide.

Aluminum (Al) implantations were carried out at room temperature on the whole surface ($5x5mm^2$) of n-type 6H and 4H-SiC epilayers (doping level $\sim 10^{16}$ cm^{-3}), cut out from CREE commercial wafers. A total dose of $1.75x10^{15}cm^{-2}$ was implanted in disoriented samples to avoid channeling effects in SiC crystal axes. Post-implantation anneals were realized in a dedicated SiC induction heating furnace [1] at the center of the susceptor. High heating ramp was utilized, 40°C/s, before to reach a constant temperature plateau in the 1600-1800°C interval during 5 min to 1 hour.

Rutherford Backscattering Spectrometry in the Channeling mode (RBS/C) measurements realized after ion implantation and before annealing illustrate spectral superposition for the 6H and 4H-SiC samples (Fig. 1). A 0,31μm amorphous layer up to the surface is found, the implant dose being superior to the threshold of an amorphous layer formation [2]. To convert energy to depth in RBS/C spectra a constant density value (3,21 g/cm^{-3}) was taken. The amorphous layer is found larger if we consider that the density of amorphous SiC is lower than of crystalline SiC. After annealing a better recrystallization is observed for 6H-SiC samples. After 1700°C annealing during 30 min the backscattering yield is 5,8% for the 6H-SiC sample and 6.3% for 4H-SiC sample, that proves nevertheless good crystallinity after annealing in the both cases.

As verified by Secondary Ion Mass Spectroscopy (SIMS) analyses on as-implanted and annealed samples, no dopant loosing occurs after high temperature annealing. The roughness of the sample surfaces after annealing increases with the temperature and the annealing time, this process becomes excessive for temperatures and times superior to 1700°C and 30 min.

Electrical activation of dopants on implanted and annealed samples was investigated by sheet resistance (R_{sh}) measurements with a four point probe technique. R_{sh} decreases when the annealing temperature or the annealing time increases. In Fig. 2 R_{sh} variations with the annealing temperature are represented, for a 30 min annealing time.

The linearity of the R_{sh} variations proves a non saturation of electrical dopant activation, nevertheless regression lines intersect temperature axe at 1819°C and 1801°C for the 6H-SiC and 4H-SiC respectively, which illustrates that these annealing conditions lead to nearly complete Al dopant activation.

For a deepen approach of the electrical behavior of Al-implanted layers, Van der Pauw (VdP) geometries and Transmission Line Method (TLM) structures were realized on SiC wafers (1.375'' diameter) by a photolithographic process. Bipolar diodes were also created to study the rectifying properties of the p^+-n junction realized by Al implantation. The same ion implantation parameters were utilized, and a 1700°C during 30 min thermal annealing was carried out on these wafers.

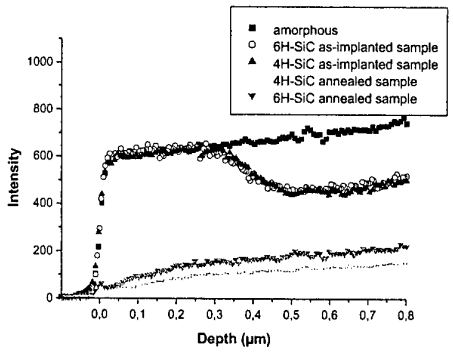


Fig. 1. RBS/C spectra on Al as-implanted and annealed 6H and 4H-SiC samples.

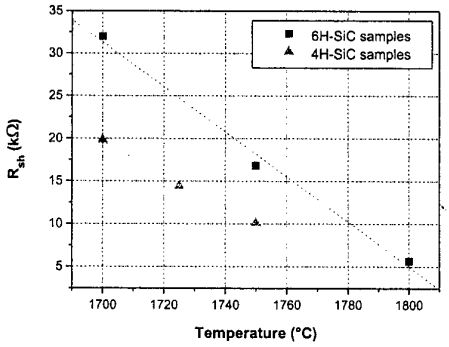


Fig.2. Sheet resistance variations with annealing temperature for 30min annealing duration.

Sheet resistance measurements made on VdP and TLM structures of 4H-SiC samples (Fig.3) show a linear dependence with the distance between the respective structure and the center of the wafer. Sheet resistance found by TLM measurements must be corrected by a geometrical factor. A linear variation is determined also for the carrier concentration by Hall effect measurements at room temperature, the mobility values preserving a relatively constant value (18 $cm^2V^{-1}s^{-1}$). High values of hall concentration involve a good electrical Al dopant activation.

A good agreement is found between the sheet resistance measured on the VdP structure placed at the wafer center and the values obtained by four point probe technique on 5x5mm^2 whole surface implanted samples, annealed in the susceptor center (19,5 kΩ Fig. 2 and 3). The linear variations of R_{sh} on VdP wafer structures compared with the results presented in Fig. 2 involve an almost linear temperature variation at the surface of the susceptor, due to the induction heating system, the temperature of the suceptor increases from the center to its periphery. A difference of 31°C is found between the center and the wafer periphery. This is in agreement with thermodynamic simulations of the susceptor induction heating process.

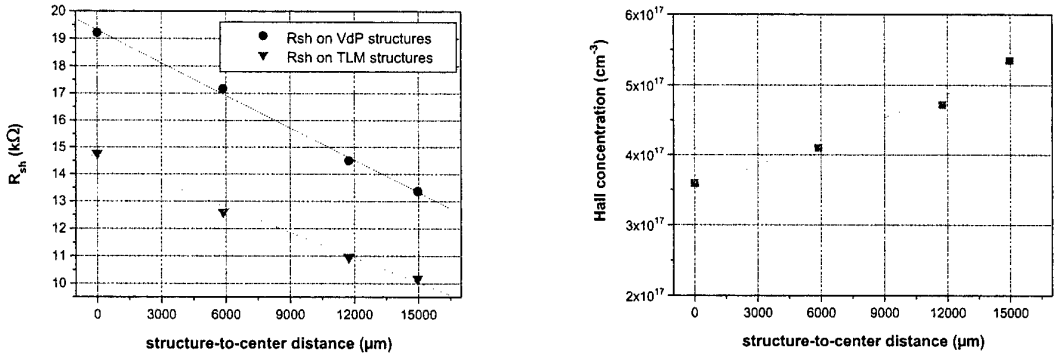


Fig3. Sheet resistance and hall concentration variation on a 4H-SiC wafer annealed at 1700°C during 30min.

I-V measurements on bipolar diodes show a good behavior in forward and reverse polarization. Current density of 60 A cm^{-2} is found at a forward bias of 5V and 10^{-7} A cm^{-2} under 100V reverse bias.

All these results will be detailed in the final paper and more comparisons between 6H and 4H-SiC will be developed.

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Improvements of electrical properties for n-type-implanted 4H-SiC substrates using high-temperature rapid thermal annealing process

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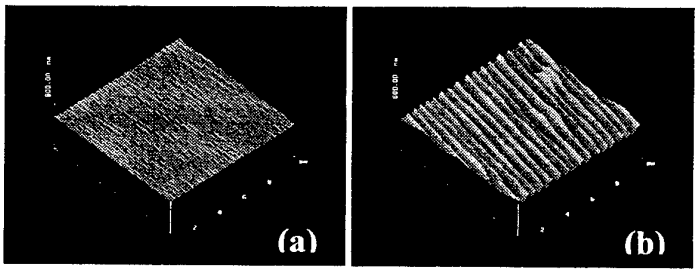
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Post implantation annealing is indispensable process for electrical activation of dopants implanted into SiC. To obtain the higher electrical activation of dopants, the post implantation annealing is generally carried out at higher temperature above 1500°C using conventional furnace annealing or a chemical vapor deposition reactor. However, selective preferential evaporation of Si atoms from the SiC surface during annealing causes local formations of C-rich phases and serious surface morphology roughening as the SiC substrates are placed on a heating holder or in a crucible for a long time. It is predicted that these degrade the performances of device fabricated on rough surface. We considered that short time annealing at high temperature is the most suitable method for the suppression of the surface morphology roughening as well as the high electrical activation of dopnats. In this study, the post implantation annealing process using high-temperature rapid thermal annealing (HT-RTA) has been investigated to reduce the surface morphology roughening and to realize higher electrical activation of n-type dopants in 4H-SiC.

4H-SiC(0001) substrates with an 8°-off-angle and p-type epitaxial layer purchased from Cree Research Inc. were used. The effective carrier density (N_A-N_D) in the epitaxial layer was $5x10^{15}$ cm^{-3}. Multiple ion implantations at 500°C were carried out through the oxide film in order to form a box-shaped profile with a thickness of 0.3 μm. The multi-energy ion implantations were performed in six steps (40 ~ 250 keV) for phosphorus (P) and nine steps (40 ~ 400 keV) for arsenic (As). The total implanted doses of $7x10^{15}$ and $2x10^{16}$ cm^{-2} were used. The post implantation annealing at 1700°C was conducted using the HT-RTA with the maximum raising rate of 1700°C/min in Ar atmosphere. The post annealing time (t_a) was varied between 0.5 and 30 min. To perform the measurements of sheet resistance (R_s) and Hall effect, Ni electrodes with a van der Pauw configuration were formed by electron beam evaporation and were annealed at 1000°C for 5 min. The surface morphologies of the implanted layers were observed using atomic force microscopy (AFM).

The AFM images of the surface morphology observed from P-implanted 4H-SiC (SiC:P) annealed at 1700°C for 1 min and for 30 min are shown in Figs. 1 (a) and (b), respectively. These images clearly show that the size and height of the groove structures on the SiC:P surface annealed for 1 min are less than those for 30 min. Average roughness (R_a) calculated from the AFM images of a 10x10 μm^2 observation area are 2.4 nm for 1 min and 13.3 nm for 30 min, respectively. Figure 2 shows the dependences of R_s, measured from SiC:P and As-implanted 4H-SiC (SiC:As), on t_a. The results show that HT-RTA reduces the R_s for both SiC:P and SiC:As. The R_s of 62 Ω/sq. for SiC:P annealed for 1 min and 160 Ω/sq. for SiC:As annealed for 2 min are obtained. According to Hall effect measurements at room temperature, an electrical activation ratio higher than 80 % is indicated in the SiC:P annealed at 1700°C for 1min. Finally, the minimum R_s of 38 Ω/sq. is achieved in SiC:P implanted with a dose of $2x10^{16}$ cm^{-2} and subsequently annealed at 1700 °C for 30 s. This R_s value is very small as a resistance of an n-type source region for SiC power devices. Consequently, it is demonstrated that the HT-RTA process is very useful for preventing the surface morphology roughening and lowering the R_s.

This work was performed under the management of FED as a part of the METI NSS program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.



Figs. 1. AFM images of surface morphology observed from P-implanted 4H-SiC annealed at 1700°C for (a) 1 min and (b) 30 min. z-axis length of image corresponds to 300 nm/div.

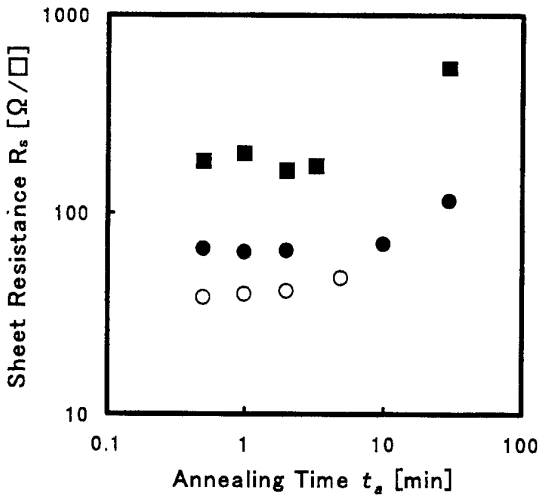


Fig. 2. Dependences of the sheet resistance R_s of P- and As-implanted 4H-SiC on the post implantation annealing time t_a. The closed circles and squares represent the R_s for P- and As-implanted 4H-SiC with a dose of $7x10^{15}$ cm^{-2}, respectively. The open circles represent the R_s for P-implanted 4H-SiC with a dose of $2x10^{16}$ cm^{-2}.

Masking process for high-energy and high-temperature ion implantion

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The ion implantation is promising process for manufacturing the silicon carbide (SiC) devices. As its particular nature, the high-energy and the high-temperature ion implantation is required. Especially, in the SIT(Static Induction Transistor) [(1)] as shown in figure 1, the width between p-gate and p-gate has an important role in the electric characteristics. It is important to establish the ion implantation to be able to form the deep p-layer selectively. However, the polymer photoresist which is commonly used in the silicon (Si) device manufacturing cannot be used for the SiC devices because of the high-temperature ion implantation. Then, we developed the silicon-dioxide (SiO_2) mask using the photolithography and the dry-etching processes. We obtained the mask of the line width of 1.2 μ m and the thickness of 3.2 μ m.

Figure 2 shows the aluminum ion distribution computed by the TRIM program. The energy of the ion is MeV. The aluminum ions are penetrated into the SiC substrate on the case of the SiO_2 thickness of 2.0 μ m. On the case of SiO_2 thickness of 2.6 μ m the aluminum ions are fully cut. We set the SiO_2 thickness of 3.2 μ m , which is estimated to calculate 20 % margins.

We used the chip of the size of 15mm x 15mm. The lithography and the dry-etching were performed using the chip fixed on a 5-inch Si wafer. The SiO_2 of the thickness of 3.2 μ m was deposited by the low-pressure chemical vapor deposition (LPCVD). Figure 3 shows the cross-sectional scanning electron microscopy (SEM) photograph of the SiO_2 which was dry-etched using the photoresist of the thickness of 4.2 μ m. The CHF_3 and the CF_4 gases are used on the dry-etching. The photoresist was completely lost and the SiO_2 was also etched. Then we performed the ultraviolet (UV) irradiation on the polymer photoresist. Figure 4 shows the cross-sectional SEM photograph of the SiO_2 which was dry-etched using the UV irradiated photoresist of the thickness of 2.5 μ m. The photoresist was remained the thickness

of 1.2 μ m and the SiO_2 was almost vertically etched. Particularly, the side of the SiO2 has no notches, and the dispersion of the electric characteristics keeps controllable.

We developed the SiO_2 mask of the width of 1.2 μ m and the thickness of 3.2 μ m which was wholly cut the aluminum ions implanted by the energy of the MeV.

This work was performed under the management of FED as a part of the MITI NSS Program (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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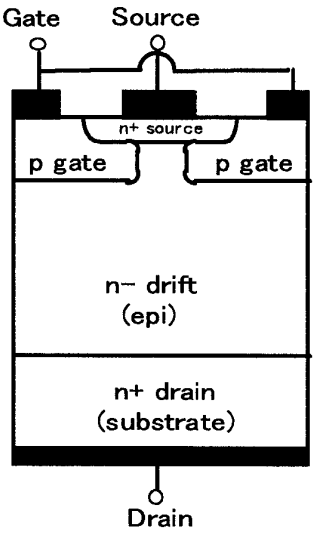


Fig.1 The device structure of SIT

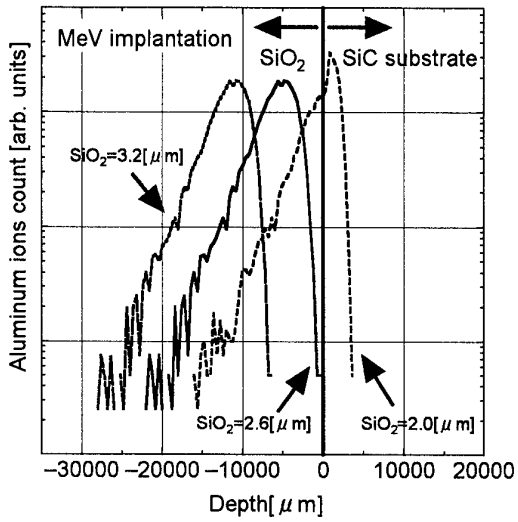


Fig.2 The aluminum ion distribution Depened on the SiO_2 thickness

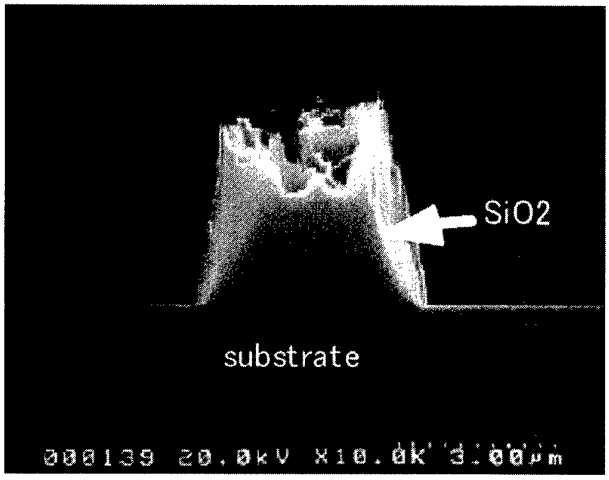


Fig.3 Cross sectional SEM photograph of the SiO_2 dry-etched using 4.2 μ m photoresist without the UV irradiation

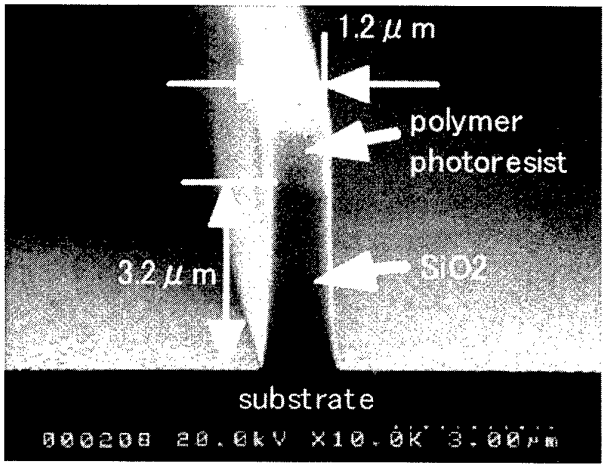


Fig.4 Cross sectional SEM photograph of the SiO_2 dry-etched using 2.5 μ m photoresist with the UV irradiation

Electrical characteristics of Al^+ ion-implanted 4H-SiC

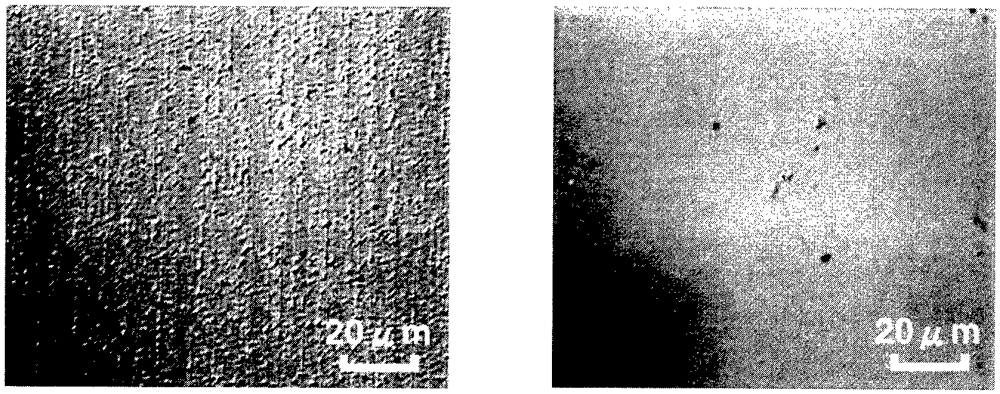
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4H-SiC is the most promising SiC polytype for manufacturing high-power, high-temperature and high-speed electronic devices with outstanding capabilities. Many efforts to obtain a good p-type SiC layer by ion implantation, using either aluminum or boron ions, have encountered difficulties such as high sheet resistance and low activation efficiency [1], [2]. In this work, an attempt was made to perform low-resistivity p-type doping in a 4H-SiC epilayer by using aluminum ion-implantation.

The target material, purchased from Cree Inc., was a 4H-SiC substrate with a 4-μm-thick epitaxial layer. The doping of the epitaxial layer was 1×10^{16} cm^{-3} n-type. Specific energy/dose schedules for aluminum implantation were 180 keV/2.7×10^{15} cm^{-2}, 100 keV/1.4×10^{15} cm^{-2} and 50 keV/9.0×10^{14} cm^{-2}. All implantations were performed at 800℃. Post-implantation annealing was done for 10 minutes at 1600～1800℃ in an argon atmosphere. In order to prevent morphological surface degradation, samples were encapsulated in a dummy-SiC wafer during annealing. Nomarski differential interference contrast (NDIC) micrographs of the samples annealed with and without the dummy-SiC wafer are shown in Fig. 1. Significant surface degradation is observed for the sample annealed without the dummy-SiC wafer. On the other hand, the sample annealed with the dummy-SiC wafer shows a smooth surface morphology. To investigate the electrical properties of the samples annealed with the dummy-SiC wafer, Hall measurements were performed with the conventional Van der Pauw method. Ohmic contacts were fabricated of Ti/Al, followed by annealing at 1000℃. Sheet resistance Rs is shown as a function of the annealing temperature in Fig. 2. The value of Rs decreases with increasing annealing temperature between 1600～1800℃. Rs as low as 2.3kΩ/□, a record low for any implanted p-type SiC layers, was obtained in the sample annealed at 1800℃. Sheet carrier concentration Ns and Hall mobility μ are shown in Fig. 3. Ns is about two orders of magnitude larger when the annealing temperature is increased from 1600℃ to 1800℃. The decline in sheet resistance Rs is mainly due to the improvement of Ns with a higher annealing temperature.

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(A) (B)

Fig. 1
Nomarski differential interference contrast (NDIC) micrographs of samples annealed (A) with and (B) without a dummy-SiC wafer.

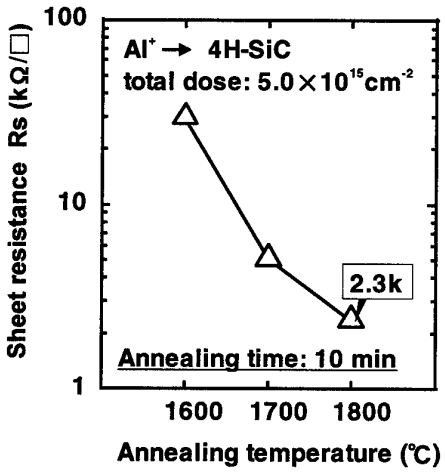


Fig. 2
Sheet resistance Rs as a function of annealing temperature.

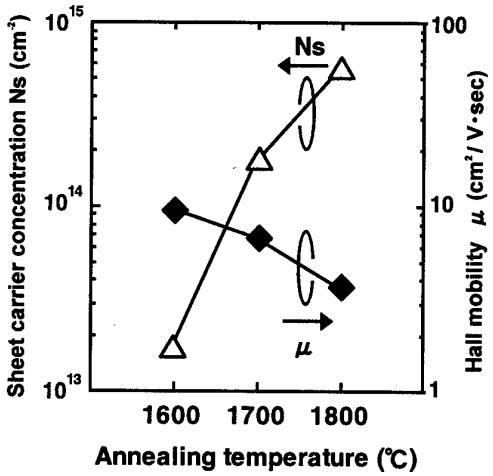


Fig. 3
Sheet carrier concentration Ns and Hall mobility μ as a function of annealing temperature.

Micro-structural and electrical properties of Al implanted & lamp annealed 4H-SiC

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The ion-implantation process has been a great success and being used extensively in Si-device technology, however, for SiC devices, it still lacks the critical know how related to the defect kinetics. One of the key issue for realizing the SiC planar devices is to eliminate the ion-implantation process induced damages as well as to achieve the high electrical activation for dopants to match the design requirements. However, the high temperature activation annealing process of SiC usually deteriorates the important chemical and morphological surface that eventually leads to poor electrical properties.

The micro-structural and electrical properties of Al implanted 4H-SiC annealed using a halogen lamp furnace has been investigated with the aim to minimize the effect of high temperature activation processing viz., step bunching and surface graphitisation. Earlier, Panknin et al.[1] reported high electrical activation for the Xenon array flash annealed Al implanted 6H-SiC, however, defect kinetics of the flash annealed samples were not discussed. A twin halogen lamp annealing system was used to electrically activate the implanted Al dopant. Al implantation dose was $1.0x10^{15}cm^{-2}$ and implantation was performed at 1000℃. The samples were subjected to lamp exposure from either or both sides to anneal at different temperatures. Transmission electron microscopy (TEM) was used to probe the micro-structural changes of lamp annealed 4H-SiC samples. During the activation annealing the micro-structural defects are formed and the generation of such defects upon annealing are investigated with respect to dopant electrical activation and leakage current to establish a possible correlation between the said properties. The electrical activation result suggests that the halogen lamp annealing process is as effective as conventional furnace annealing process and almost independent of time scale of performed experiments at high temperature region (~1800℃) for Al dopant. Also, contrary to the strong B transient enhanced diffusion in SiC, no significant diffusion of Al was observed [2]. The uncapped 4H-SiC samples show the improvement in the surface morphology after the high temperature lamp annealing process. However, the sublimation of the surface layer due to high surface temperature during the long direct lamp exposures was observed. TEM analysis confirms the suppression of surface graphitisation, which is commonly observed for conventional furnace annealing process. The observed circular dislocation loops, composed of either clustered interstitial atoms/ dopant Al residing on basal planes and/or an extra SiC plane show a strong dependence on the annealing time. The electron energy loss spectroscopy (EELS) was used to investigate the microstructure of dislocation loops. Basically, the implantation at elevated temperature of 1000℃ leads to the substantial amount of defect reduction. During the high temperature activation annealing process, density of these dislocation loops decreases with time, although they grow in size. The test structure of pn junction with no passivation and edge termination shows the low level of leakage currents ($<1x10^{-8}A/cm^2$). Any correlation between the dislocation loop density or size on the pn leakage current was not observed.

In summary, lamp annealing process is effective for the dopant activation process compare to the conventional furnace process as significant improvements in the sheet resistance and the pn leakage current were observed for the lamp annealed 4H-SiC samples. However, a relatively high density of dislocation loops were observed for the lamp annealed ones. The possible formation kinetics of these micro-structural defects will be discussed.

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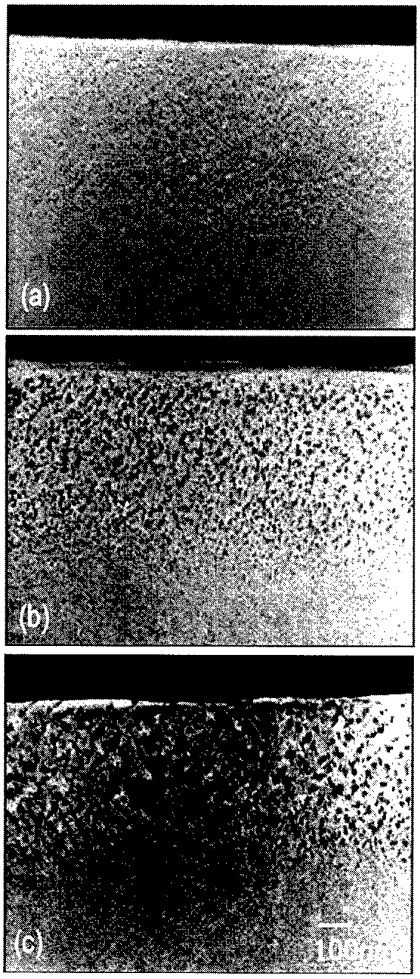


Fig.1 Cross-sectional transmission electron microscopy images of Al implanted 4H-SiC annealed using the halogen lamp furnace at (a) Temp.=1600℃ for 30 sec., (b) Temp. =1600℃ for 1min., and (c) Temp=1600℃ for 10min. The Al implantation dose was $1.0x10^{15}cm^{-2}$ and implantation was performed at 1000℃.

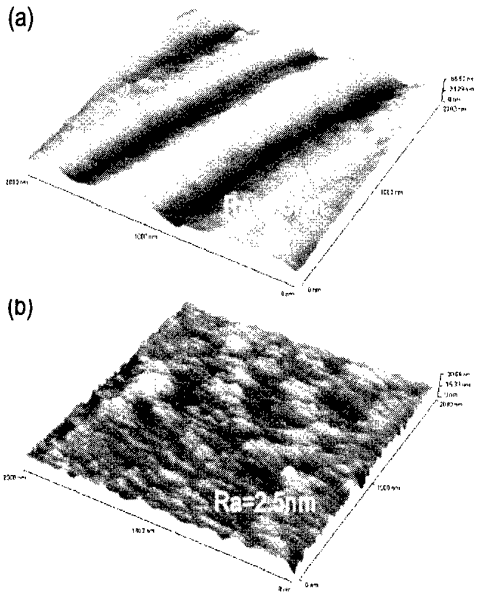


Fig. 2 AFM images of Al implanted 4H-SiC annealed using (a) the conventional furnace at Temp. =1600℃ for 30min., and (b) the halogen lamp furnace at Temp.=1600℃ for 30sec.

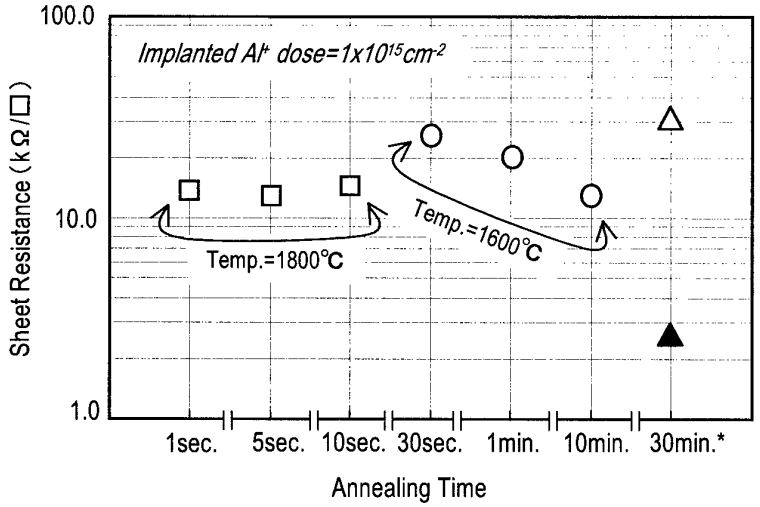


Fig. 3 Sheet resistance of Al implanted 4H-SiC as a function of activation annealing time# for different temperatures. The open and solid triangle data points represent the 1600℃ furnace annealed samples with Al dose of $1x10^{15}cm^{-2}$ and $1x10^{16}cm^{-2}$, respectively. (*Furnace annealed 4H-SiC sample; #Excluding the ramp-up/ramp-down time)

Range distributions of implanted ions in silicon carbide

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In modern semiconductor technology the access to precise process simulators has become vital to decrease the development time and cost for new devices. To predict ion implanted doping profiles two types of simulators are mainly used: (i) Simulators based on physical models of the ion stopping processes. Most of these use different types of Monte-Carlo algorithms and can be – with appropriate empirical fine tuning – very accurate, although too time consuming for the purpose of implantation profile design.[1] (ii) A convenient alternative is based on the fact that most ion range profiles can be represented, to a high degree of accuracy, by its first four distribution moments (R_p, ΔR_p, γ, and β) using Pearson frequency distribution functions.[2] In this way, depth profiles of multiple ion implantations can be quickly and precisely simulated by interpolation between established distribution moments, providing that the amount of experimental data is large enough.

In this contribution we have assembled range data from 120 single energy implantations into SiC of ^{1}H, ^{2}H, ^{7}Li, ^{11}B, ^{14}N, ^{16}O, ^{27}Al, ^{31}P, ^{75}As, and ^{69}Ga, in the energy range 1 keV – 4 MeV. The range data for more than 40 of these implantations are previously unpublished while the remaining distribution moments have been obtained from the literature. The implantations were performed, with few exceptions, using crystalline SiC and under conditions (implantation dose and temperature) so that amorphization and significant surface swelling was avoided. For the new data, the first four distribution moments were extracted using a least square fitting procedure of Pearson functions to the concentration versus depth profiles obtained by secondary ion mass spectrometry (SIMS), exemplified for ^{11}B in Fig. 1. To acquire a compact interpolation scheme for the experimental moments analytical functions, with 2 – 4 fitting parameters each, were fitted to the data (Fig. 2). The experimental data for ^{1}H, ^{7}Li, ^{16}O, and ^{69}Ga were to scarce for this fitting procedure. To compensate this deficiency, Monte-Carlo simulations were performed to fill up the empty gaps in the moments versus energy plots of these ions. In these simulations we used the newly developed ion implantation code SIIMPL [3] which is based on the binary collision approximation [1] and was carefully calibrated to the existing experimental data of each ion.

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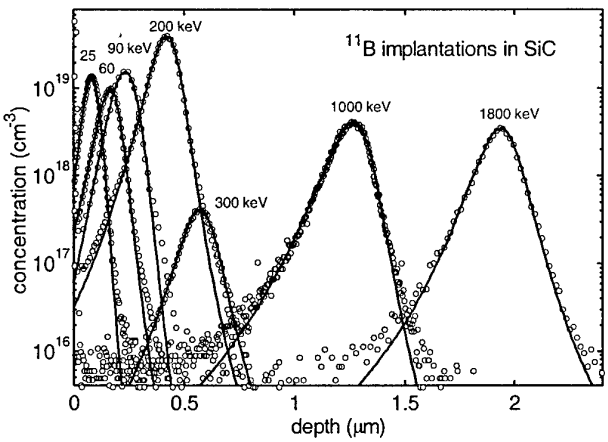


Fig. 1. SIMS measurements of concentration versus depth for ^{11}B implants into SiC (○). Pearson functions have been fitted to the profiles (solid lines) to extract the first four distribution moments of the implants.

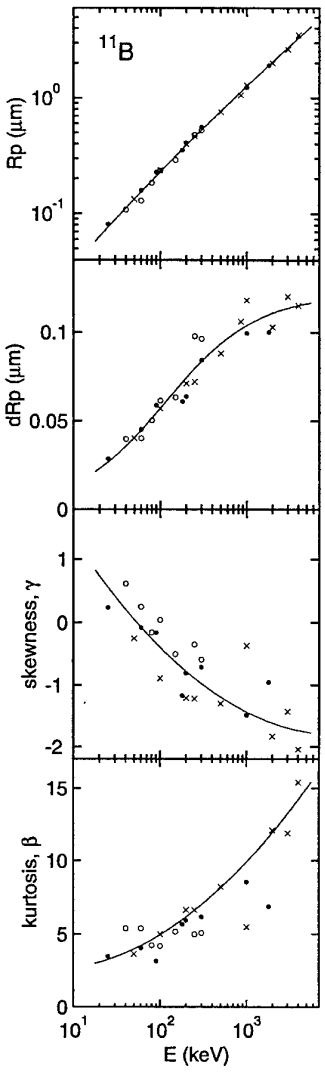


Fig. 2. First four distribution moments of ^{11}B implants into SiC originating from: (●) this study, (○) Ref.[4], and (×) Ref.[5]. The solid lines represent least square fits of moment functions to the experimental data.

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Post-implantation annealing effects on the surface morphology and electrical characteristics of 6H-SiC implanted with aluminum.

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Ion implantation is indispensable for the fabrication of electronic devices based on crystalline silicon carbide (SiC), because the conventional thermal diffusion technique cannot be applied to the device fabrication of SiC from the fact that donor or acceptor impurities like N or Al have quite low diffusion coefficients in SiC crystal. After ion implantation, annealing at high temperatures above 1500°C is necessary to activate the dopants electrically as well as to recover the crystallinity of SiC damaged by ion implantation. Annealing at such high temperatures often makes the surface of SiC rough, which is undesirable for fabrication of electronic devices based on SiC. Thus both the surface morphology and dopant activation should be considered when optimizing the post implantation annealing process. For this purpose, we have investigated the surface morphology and electrical characteristics of 6H-SiC implanted with Al and subsequently annealed under different conditions.

The samples used in this study were n-type, 3.5°-off 6H-SiC(0001) epitaxial films grown on 6H-SiC single crystals which were purchased from CREE Research Inc. Five fold (20, 50, 110, 200 and 340 keV) implantation of Al ions was carried out to form a box profile with a mean Al concentration of $2\times10^{18}/cm^3$ and to a depth of 0.5μm. The samples were subsequently annealed for 30 minutes in flowing Ar gas at different temperatures of 1550°C, 1650°C and 1750°C. Different annealing periods (3 and 10 minutes) were also carried out at 1650°C and 1750°C.

The surface morphology of these samples was characterized using atomic force

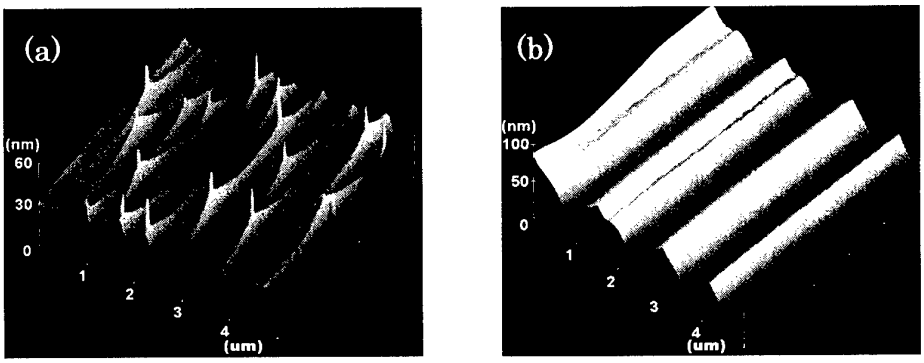


Fig.1 AFM images for Al^+ implanted 6H-SiC(0001) 3.5°-off surfaces after annealing at (a)1550°C and (b)1750°C for 30 minutes

microscopy(AFM). All samples showed rough surfaces after annealing. Figures 1(a) and 1(b) show AFM images after annealing at 1550°C and 1750°C, respectively, for 30 minutes. While the sample annealed at 1550°C shows slender and hillock like features with sharp spike, those annealed at the higher temperature exhibits straight grooves. The orientations of these features are parallel to each other. Each groove has a plane of which direction is approximately 3.5°-off from the sample face. Some large hillocks also have the 3.5°-off plane on their surfaces. Thus these features must be huge bunches of bi-layer steps and include the (0001)-Si face as a part of their surfaces. Figures 2(a) and 2(b) show the AFM images for the samples annealed at 1650°C for 3 and 30 minutes, respectively. By increasing the annealing time, hillock-type features in Fig. 2(a) disappeared and instead groove-type features appeared as shown in Fig. 2(b). The surface morphology of the samples annealed under the other conditions can be also classified at these two types, i.e., grooves and hillocks, although the size and density of the features (grooves or hillocks) changed with annealing condition. The height and lateral size of the features increased with increasing annealing temperature and time, whereas the density of the features decreased with increasing temperature. That is, the density of hillocks/grooves depends on annealing temperature only, even though the size and/or the type of the features change at different annealing duration.

These results imply that hillocks are the nuclei of the huge step bunching, i.e., the hillocks become grooves after their growing to a certain extent. The density of grooves depends strongly on the density of hillocks at the initial stage of groove formation, suggesting that the mean distance between adjacent grooves is controlled by changing the annealing temperature. It indicates the possibility that the formation of a large amount of nuclei and their growth by annealing at low temperatures and following annealing at higher temperatures (two step annealing) provide the surface with small roughness.

The electrical characteristics of these samples will be shown and discussed in conjunction with the surface morphology in the conference.

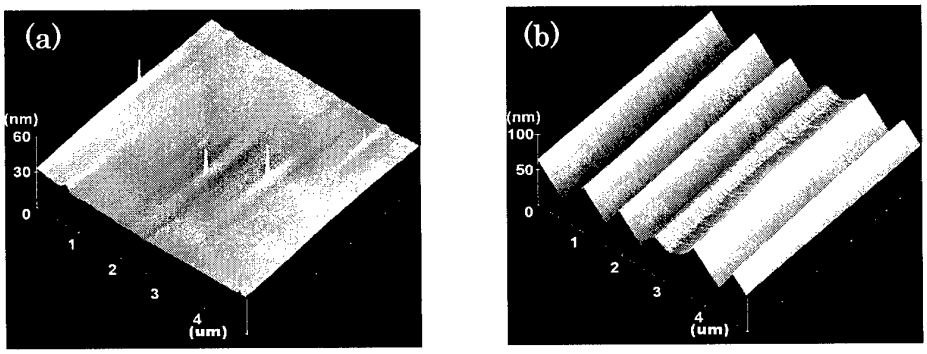


Fig.2 AFM images for Al^+ implanted 6H-SiC(0001) 3.5°-off surfaces after annealing at 1650°C for (a)3 minutes and (b)30 minutes

Realization of a high current and low R_{ON} 600V Current Limiting Device

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Silicon carbide technologies for the manufacturing of power devices seem to be promising in the near future. The first SiC power device commercially available is a Schottky diode proposed by Infineon society (ranging: 300 V / 10 A and 600 V / 4-6 A). In the field of the SiC switches, the current trends are the Accu-MOSFET and JFET structures which exhibit the best specific on-resistance/breakdown voltage ratio experimentally obtained (Accu-MOSFET: 16 $m\Omega.cm^2$/1600 V [1] ; JFET: 10 $m\Omega.cm^2$/600 V, 14 $m\Omega.cm^2$/1800 V [2]).

The aim of this paper is to show the first experimental results of a 600 V 4H-SiC current limiting device (Fig. 1). This device limits the current which flows through it as the bias voltage between its two contacts increases. The static curves obtained from the first run (T=300 K) show a current limitation ability with a saturation voltage ranging from 10 V to 15 V. The electrical device characterization shows a $R_{ON} \approx 150$ $m\Omega.cm^2$ and a current density of 100 $A.cm^{-2}$ under 50 V. The forward conduction is ensured by an N type implanted channel (doping species: nitrogen) over an P^+ implanted layer (doping species: aluminum). The electrical characterization of the $N_{CHANNEL}/P^+$ layer (analyzed by C(V) and SIMS methods) shows a good channel mobility (100 $cm^2.V^{-1}.s^{-1}$ for a 2×10^{17} cm^{-3} N compensated doping concentration). The prototypes of the second run reach a saturation current density of 900 $A.cm^{-2}$ (Fig. 2), with a specific on-resistance of 13 $m\Omega.cm^2$ (Fig. 3). The 4H-SiC current limiting devices of the second run belong to the best set of Accu-MOSFETs devices obtained in the literature.

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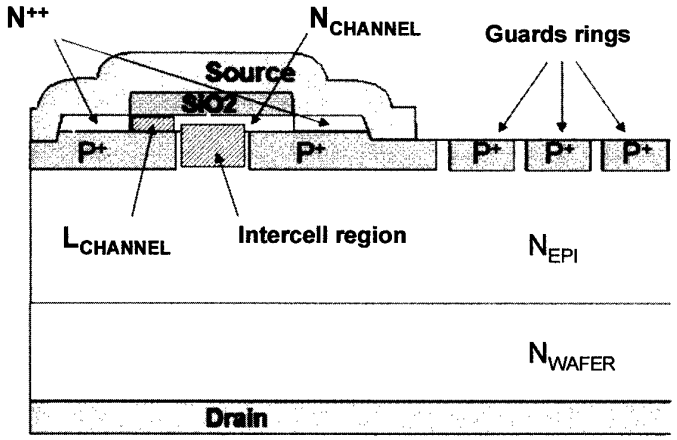


Fig. 1 : Vertical cross section of the device and its guard rings peripheral protection (the channel region, $L_{CHANNEL}$, and the 'intercell' region are noted).

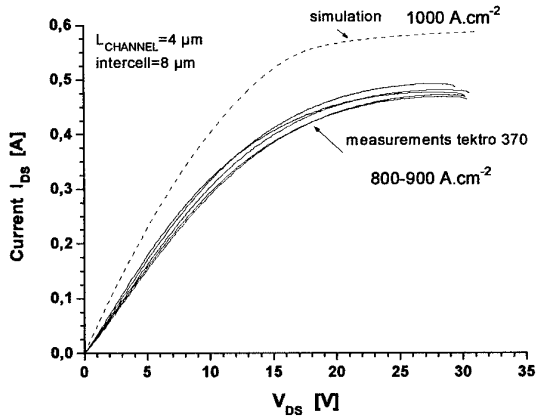


Fig. 2 : Comparison between a DESSIS ISE® simulation [3] and experimental results for a current limiting device (channel length : 4 µm / intercell length : 8 µm). In the experimental results using the tektronix 370 curve tracer, the temperature inside the device, particularly at the end of the channel is unknown.

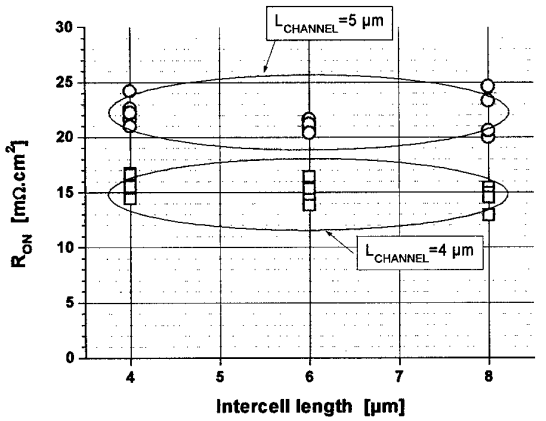


Fig. 3 : Experimental specific on-resistance plotted versus the 'intercell' length.

Unipolar and Bipolar SiC Integral Cascoded Switches with MOS and Junction Gate - Simulation Study

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Silicon carbide greatly expands the voltage range of unipolar and bipolar power devices as compared to silicon. Unipolar devices with blocking voltage of 4.5 kV and even more can ideally be made having lower conduction and switching losses as compared to bipolar devices. SiC unipolar devices thus cover the needs of most of the motor drives, switched mode power supplies and automotive applications. However, for power transmission and traction applications devices with blocking voltages higher than 10 kV are of interest. In these applications bipolar SiC devices have to be used [1].

In this study we investigated a family of integral cascode switches built upon the principle of a buried grid. The buried grid constitutes the gate of the vertical junction field effect transistor (VJFET) or thyristor (VJFETh). It is normally shorted to the source or emitter electrode and its primary function is to take up the high voltage applied to the drain or collector. The upper part of the structure contains a low voltage VJFET or UMOSFET. The buried grid shields the upper part of the structure giving reduced electrical field at the trench corners and at the surface grid, respectively [2,3]. The surface gate of the upper part of the structure constitutes the control gate of the entire switch. The investigated switches are designed to be controlled by a gate voltages between 2 and -10 Volts. With the buried gate shorted to the source, the device is blocking full voltage with a negative voltage $\geq$10 V applied to the surface gate and it is conducting with a positive voltage of maximum 2 V applied to the same gate. Connecting the high voltage grid to the source or cathode greatly reduces the switching losses [4]. The JFET with junction gate control constitutes an alternative to the MOS technology [5]. The attractiveness of the cascode concept is that it expands the range of application of a VJFET and facilitates realisation of both medium and very high voltage switches on the basis of a single technology.

Switches with two voltage designs, 3.3 kV and 10 kV, defined as 80% of the calculated bulk breakdown value, are investigated. The 3.3 kV switches are unipolar cascodes based on a VJFET controlled by a low voltage JFET and UMOSFET, respectively. The 10 kV switches are bipolar cascodes based on a VJFETh controlled by a low voltage JFET and UMOSFET, respectively. The 10 kV structures contain a p-type emitter at the collector side for hole injection. The cross-section of the 6 µm long upper part of the devices is shown in Fig.1. The n-base layer thickness and doping is 32 µm and 4e15 cm^{-3}, respectively, in the 3.3 kV design and 102µm and 8e14 cm^{-3}, respectively, (plus 50µm, 5e15 cm^{-3} n-stop) in the 10 kV design. The carrier lifetime is set to 2 µs for the bipolar switches and to 0.5 µs for the SiC antiparallel diode. The channel mobility of the UMOSFET is set to 10% of the bulk mobility value. In Fig 2 the simulated data for on state voltage with 2 V (JFET) and 10 V (UMOSFET) applied to the control gate are shown. As can be seen in Figs 5 and 6 the junction gate devices show softer switching behaviour as compared to the MOS gate devices.

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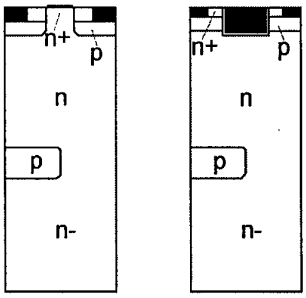


Fig. 1 Cross-section of simulated structures showing MOS and junction-type upper gates and buried lower gate.

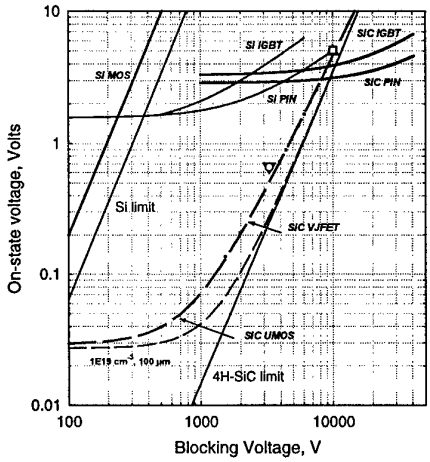


Fig. 2 On-state voltages of the simulated structures with MOS gate (empty symbols) and JFET gate (full triangles) at 100 A/cm^2. Other data based on simulations of simple structures without buried grid [1].

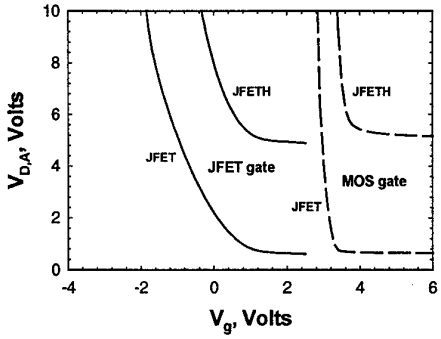


Fig. 3 On-state voltage at 100 A/cm2 as a function of control gate voltage.

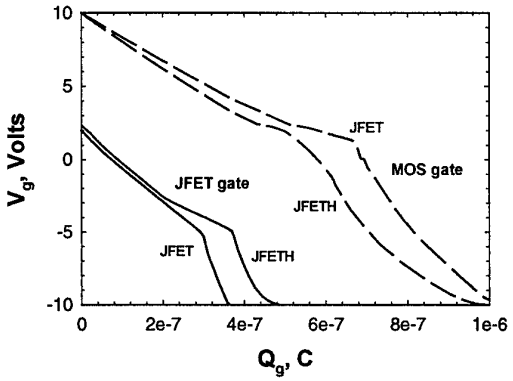


Fig. 4 Transfer characteristics (Turn-off).

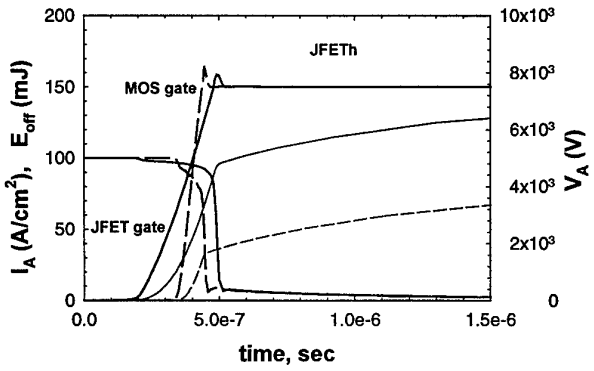


Fig 5 Turn-off of 10kV structures, R_g=10 Ω.

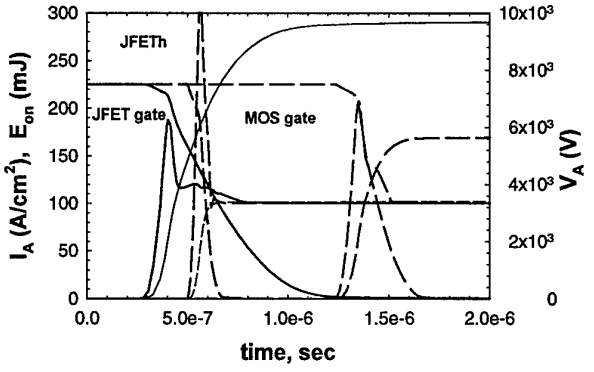


Fig 6 Turn-on of 10kV structures, R_g=20 and 50 Ω for MOS case and 50 Ω for JFET case.

Influence of the trenching effect on the characteristics of buried-gate SiC junction field-effect transistors

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Junction field-effect transistors (JFETs) in SiC have drawn attention due to the inherent stability of the p-n junction gate, compared to the Schottky or MOS interface, as well as their relatively simple structure. To date the viability of SiC buried-gate JFETs for high temperature and high voltage operation has been demonstrated by various groups [1,2].

For buried-gate SiC JFET structures, as in most of SiC power devices, the dry-etch is one of the most important process steps required. Plasma assisted dry etching methods are generally used techniques to etch SiC in the absence of proper wet etchants of SiC. However, deep cuts at the bottom of the sidewalls, the so-called trenching effect, are known to occur in most dry etching conditions [3]. The trenching effect is attributed to the deflection of ions on the sidewall inducing enhanced ion bombardment at the bottom.

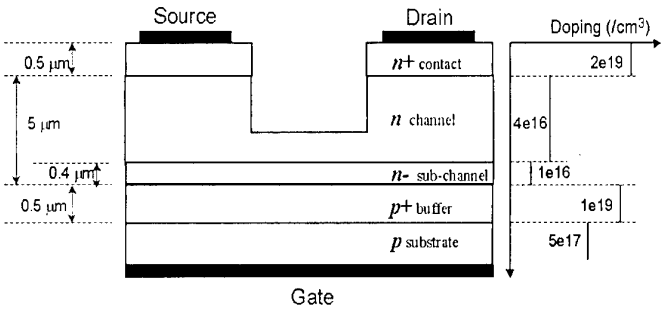


Fig.1 Cross-sectional Schematic diagram of a typical 4H-SiC buried-gate JFET

In this work, we investigate the influence of the trenching effect on the characteristics of SiC JFETs and processes for controlling the trench edge angle are presented. A 4H-SiC wafer from CREE Inc. with epitaxy grown at Linköping University is used for the experiments and the numerical simulation of the device was carried out using ATLAS software from SILVACO Inc.

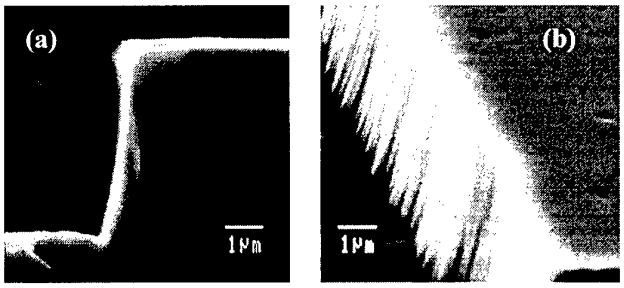


Fig.2 SEM images showing the trench effect on the bottom of the sidewall: (a) cross-sectional profile and (b) tilted view

Fig.1 shows a cross-section of the fabricated buried-gate JFETs using a two-mask layer process. The channel was formed using an inductively coupled plasma (ICP) dry etch in SF_6/Ar. Typical SEM images of the etched profile using a Ni mask, indicating good anisotropy with trenching effect, are shown in Fig.2. The etch

rate of SiC is ~110 nm/min and the trenching profile has depth of 0.2-0.3 μm for a ~4.5 μm deep etch. The simulated results on the typical structure with the trenching effect agree well with the measured data showing a slight decrease in the current density of around 10 %, but improved linearity in the gate-drain characteristics and maximum transconductances up to ~25 mS/mm from the measurements were obtained with devices with trenching. If the channel becomes too thin, the on-resistance increases while the pinch-off voltage decreases, which agrees well both with 1 dimensional analysis and 2 dimensional numerical simulations.

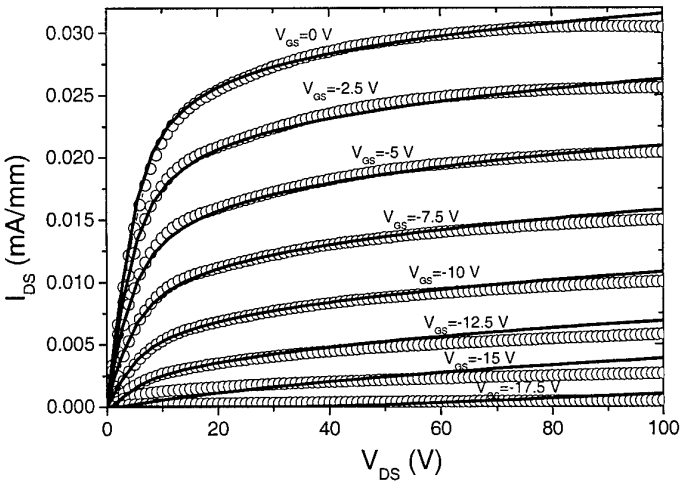


Fig.3 Comparison of simulated and measured drain current vs drain-source voltage for different gate voltages in a JFET of 5 μm channel length. Solid lines are from simulations and open circles are measured curves.

In Fig.3, typical I-V characteristics of well-saturated curves are shown. A decrease in the breakdown voltage of JFET is the most undesirable effect of trenching owing to the field crowding at the trench corner, see Fig.4-(a). To avoid this effect, a PECVD grown SiO_2 with wet-etched slope is used to transfer a sloped sidewall during dry etching of SiC as shown in Fig.4-(b) and Fig. 5. The design criteria will be discussed and an optimum design will be presented.

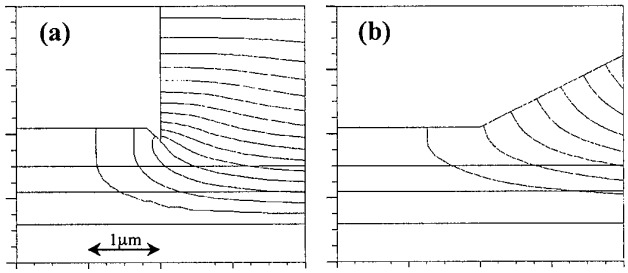


Fig.4 Simulation results showing potential distributions for two different different dry etch profiles, (a) with trenching effect and (b) with angled etching (V_{DS}=500 V, step of equi-potential lines = 56 V)

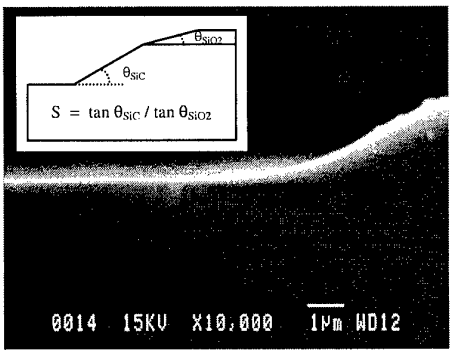


Fig.5 SEM image showing trench corner rounding using angled oxide mask after removal of oxide mask (inset; schematic diagram of oxide mask and SiC)

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Simulation study of a new current limiting device : a vertical α-SiC etched JFET- Controlled Current Limiter.

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Keyword : Silicon Carbide, current limiter, JFET, serial protection device.

Considering fault current limiters for serial protection, a lot of structures exist, from regulation to other complex systems. Up to now, only a few current limiters based on semiconductor structures have been described in papers [1],[2],[3],[4].
Although Current Regulative Diode component exist [5], their voltage and current capabilities (V_{BR}=100 V, I_{max}=10 mA), do not allow to use them in power systems. A Comparison between a Silicon and a 6H-SiC CRD (Current Regulative Diode) equivalent outline the benefits of a SiC CRD as current limiter (Fig. 1). Unfortunately, the required dimensions of implanted layers are too small in regard to current state of art of SiC technology.
Silicon carbide, owing to electrical properties, allows to foresee the realization of new power components with higher capabilities than silicon. Its band-gap energy (3eV@300K) and its thermal conductivity (λ=4.9 $W.cm^{-1}.K^{-1}$) allow to fabricate components such as diodes with reverse breakdown voltage up to 6.2 kV [6]. Figure 2 illustrates the capabilities of silicon carbide compared to conventional semiconductor materials. Factors of merits are introduced to compare those semiconductors : JFM [7], which outline the potentialities of silicon carbide, in terms of high power and high frequency with respect to silicon. Thermal and voltage capabilities of silicon carbide are advantageous to realize a current limiter. As in passive state, the voltage drop across the component must be as low as possible, in the active state, (limiting phase), a current limiter must sustain both high current and high voltage. The resulting power must not cause the component destruction. Therefore, a new bi-directional current limiter structure based on a vertical Silicon Carbide etched JFET, with both buried gate and source (figure 3) is proposed below.
This device was designed for applications like motor starting phase (figure 7), short circuit protection, circuit breaker with higher performances. Simulations were performed with ISE software [8] to evaluate static and transient electrical characteristics of the JFET, according to several specifications : voltage capability (1.7 kV), current rating (> 1A). Simulations allow to estimate geometrical and doping characteristics, (as presented in Fig. 4), as well as the technological steps required to realize such a component. Controllability (thanks to the buried gate P layer), self heating, peripheral effects on the electrical characteristics (such as fixed oxide charges) have also been analyzed (figures 5 and 6). Simulations have been performed for bi-directional devices in order to minimize power dissipation during limitation state, owing to the presence of the gate. Finally a combined peripheral protection with both field plate and JTE (Junction Termination Extension) was designed to sustain the required voltage (1.7 kV). The simulated resistance in the linear mode is 170 $m\Omega.cm^2$ for the 6H-SiC device for the 1.7kV application. The fabrication of this device is currently on the way and first electrical characterization results are expected within few months.

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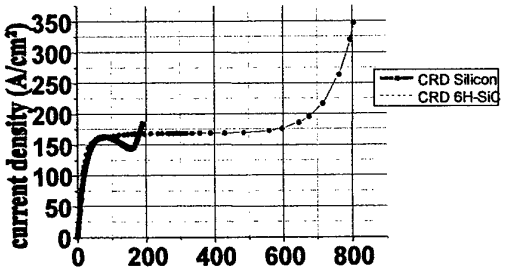


Figure n°1. Comparison between Si and 6H-SiC CRD.

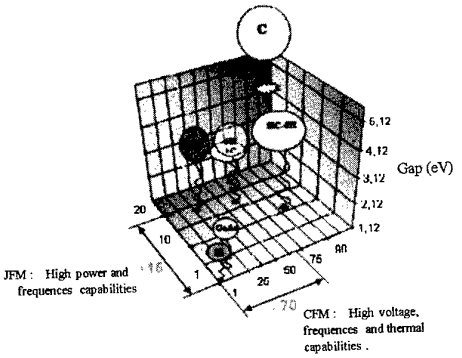


Figure n°2 : SiC versus Si, GaN...

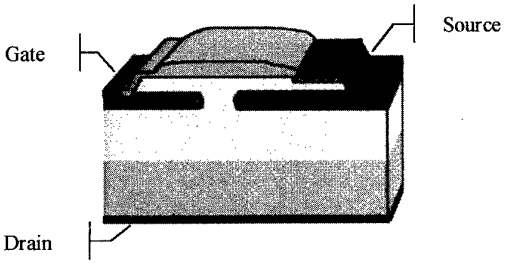


Figure n°3. Cross section view of the JFET. section

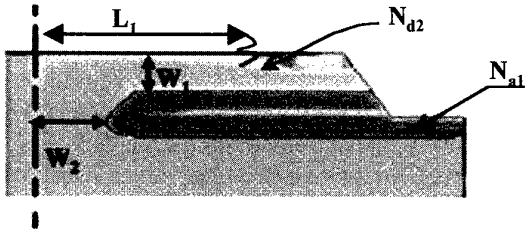


Figure n°4. Simulated cross section view of the JFET with main parameters to optimize

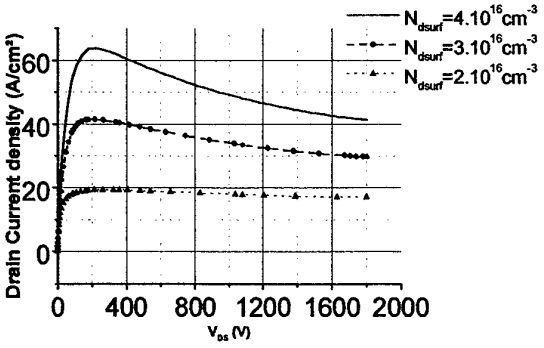


Figure n°5. Simulated drain to source characteristics of the JFET for various doping level of the top channel region.

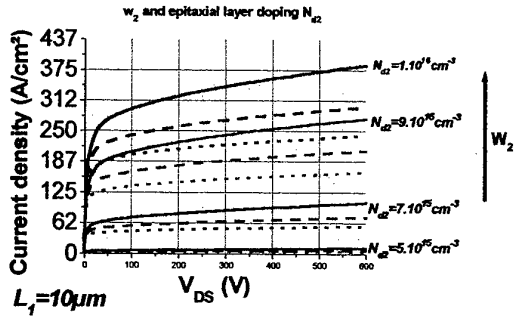


Figure n°6. Electrical characteristics for various epitaxical layer doping level and channel thickness

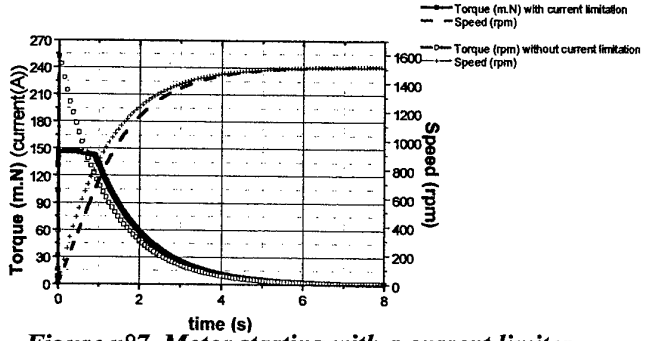


Figure n°7. Motor starting with a current limiter

Static and dynamic behaviour of SiC JFET/Si MOSFET cascode configuration for high performance power switches

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Abstract.

This paper is concerned with a detailed device and mix-mode circuit numerical analysis of SiC power switches. Two structures have been chosen, a SiC Trench MOSFET and SiC JFET coupled with a Si MOSFET in a Cascode configuration. The paper provides for the first time an insight into the physics of switching of the two structures and proves that the Cascode configuration is a superior alternative to the classical SiC Trench MOSFET owing to higher switching frequency, lower on-state resistance and reduced overall transient losses. In addition the SiC Trench MOSFET suffers from low channel mobility, may encounter oxide breakdown and punch-through during blocking mode.

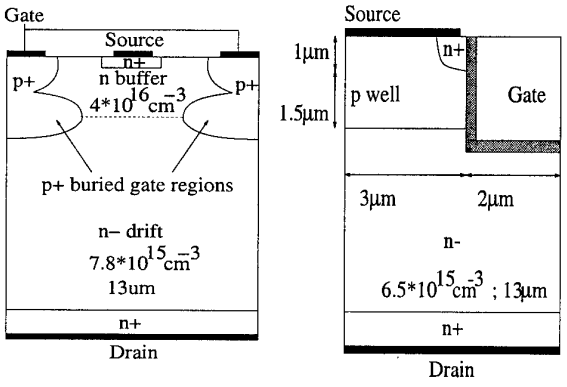
SiC JFET and SiC Trench MOSFET.

The cross sections of 1.2kV SiC JFET and Trench MOSFET are depicted in fig. 1a and 1b respectively. The SiC JFET structure consists of two main regions, the n- drift layer that supports high voltages, and the more highly doped n buffer layer, placed on the top which controls the conductive state and in particular the gate threshold voltage (i.e. pinch-off voltage) [1]. The buffer layer doping is carefully controlled to minimise the on-state resistance with no deterioration in the breakdown performance. Fig. 2 shows that the breakdown occurs below the buffer layer at the p+ gate/n-drift region interface. The doping of the drift region of the SiC Trench MOSFET is lower than that of the SIC JFET to avoid oxide breakdown. This, coupled with the high channel resistance on account of the poor channel mobility makes the on-state resistance of the SiC Trench MOSFET ($24m\Omega cm^2$) approximately one order of magnitude higher than that of the SiC JFET ($2.3\ m\Omega cm^2$).

Cascode Configuration.

The SiC JFET is a normally on device, and as such, not suitable in most of the power switching applications. To provide a normally-off operation and a full MOS voltage control the Cascode configuration was proposed in [2] and subsequently demonstrated in [3]. The idea is to connect the high voltage SiC JFET (e.g. 1.2 kV) in series with a low voltage Si MOSFET (e.g. 80 V) as shown in Fig. 3. The static potential sharing within the Cascode structure during the voltage blocking mode is shown in Fig. 4. An increase in the voltage supported by the Si MOSFET induces a more negative bias to the SiC JFET gate, thus blocking a higher voltage across the JFET drift region. The sharing is found to be linear in both static and dynamic conditions. No over-voltage spike is found during transient in the low voltage Si Trench MOSFET ensuring a safe high voltage switching operation. The inductive switching behaviour of the Cascode circuit has been evaluated using a load inductance of 50μH and a MOSFET gate resistance of 30Ω. The turn-off current curves are shown in fig. 5. The line voltage is 800V and the on-state current 10A. Interestingly, and unlike in the SiC Trench MOSFET, the voltage across the JFET drain –source terminals oscillates, thus producing corresponding current peaks. This behaviour is rather complex but can be briefly explained by the fact that whenever a voltage overshoot occurs on the JFET drain, the p+ gate/n- drift diode takes a high fraction of the current so that the load current is diverted through this gate junction. In fig. 6 the turn-off curves of a 1.2kV SiC trench MOSFET are shown. The device has been tested under the same conditions as the Cascode circuit. As can be observed, the SiC MOSFET turns off in 410ns, which means it is almost twice slower than the Cascode circuit, which switches off in 210ns. The difference is attributed to the reduced Miller capacitance of the SiC JFET/ Si MOSFET Cascode circuit.

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(a) (b)

Fig. 1 Cross-sections of the (a) - SiC 1.2kV JFET and (b) – 1.2kV SiC Trench MOSFET.

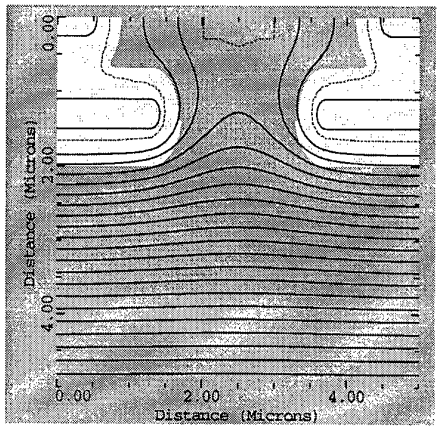


Fig. 2 Potential lines in the SiC JFET at V_{DS}=1400V

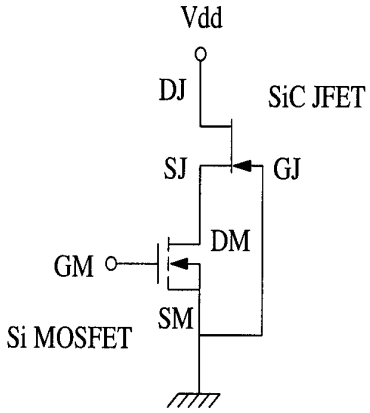


Fig. 3 The SiC JFET and the Si MOSFET connected in a cascode configuration.

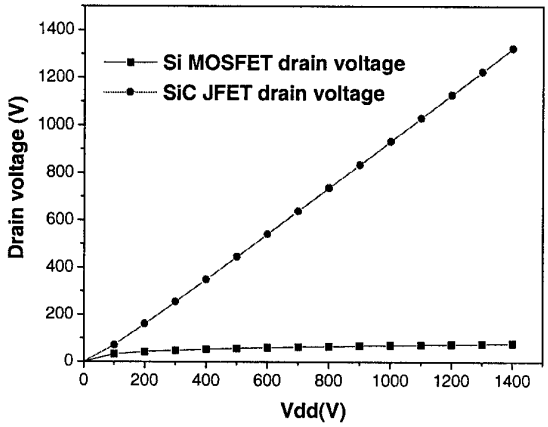


Fig. 4 The static share of the potential in the SiC JFET and the Si MOSFET

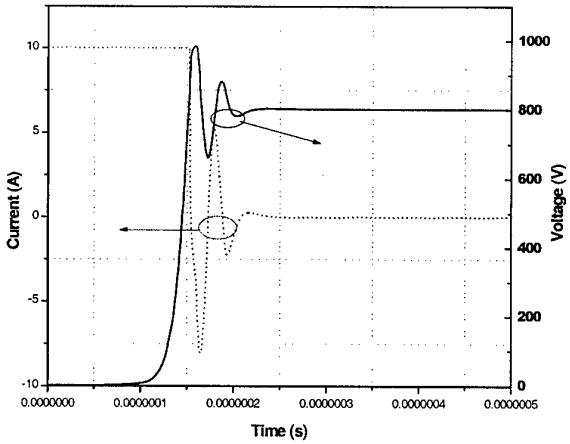


Fig. 5 The SiC JFET/Si MOSFET cascode circuit turn-off curves

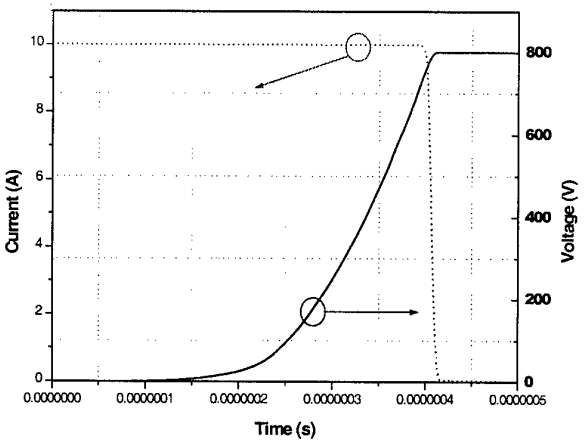


Fig. 6 The 1.2kV SiC trench MOSFET turn-off curves

Design and Processing of High-Voltage 4H-SiC Trench Junction Field-Effect Transistors

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SiC has been recognized as the choice for high-voltage, high power applications due to its superior properties such as high breakdown field and high thermal conductivity. The JFET is a basic voltage-control power device [1]. Compared with high-voltage power BJTs, JFETs have several advantages as power switching devices, such as its high input impedance and switching speed and has a larger safe operating area. Since SiC MOSFETs still need to address the low channel mobility problem [2], SiC JFET seems to be a promising alternative because the high mobility in a bulk channel. Recently, some progress has been made in SiC JFET [3].

The schematic cross-section of our vertical trench JFET structure is shown in Fig.1. The gate is formed by trench filled with P-type poly-silicon. Unlike conventional JFETs, the sidewalls of the p+ gates are isolated from the channel region with an insulating oxide. This sidewall oxide can decrease the leakage current during blocking. With the trench and sidewall oxide, it is possible to form an accumulation layer, thus will reduce the overall specific on-resistance. But the trench depth will decrease effective drift region length, this may have influence on the blocking characteristics. In this paper, we will show our recent progress in determining the performance of this JFET and proposed fabrication sequence.

In Fig.2a, we show the simulated unit cell of the JFET. The thickness of the N-epilayer is 12μm including the channel and the drift region. Fig.2 b shows the comparison of the forward blocking characteristics with different aspect ratios. Device with 2μm L_t(trench depth) and 1μm W_m (mesa width) achieves a blocking voltage as high as 1700V. Devices with aspect ratios of 4:2 and 3:2 have the same breakdown voltage. The electrical field at breakdown is shown in Fig. 3. The device breakdown occurs at the lower corners of the trench.

Since the drift region has a doping concentration of $1e16cm^{-3}$, this JFET is normally on. The simulation results of a 2μm L_t and 1μm W_m device and devices with different aspect ratios are shown in Fig.4. The specific on-resistance of the devices with different aspect ratios is ranged from 0.7 to 1.5mΩ-cm^2 with 0 gate bias. The specific on-resistance will decrease with the mesa width increases. Also, to reduce the on resistance, we need to increase the drift region doping. But both will degrade the forward blocking capability. The simulation results of the JFET are compared with other fabricated unipolar SiC devices in Fig. 5.

The fabrication of this trench JFET is now in progress. Devices are fabricated using 4H-SiC wafers. The steps of the fabrication sequence are illustrated in Fig. 6.

We are examining a novel vertical trench JFET with low specific-on resistance and high blocking voltage. The processing steps are also presented. Device fabrication is in progress.

ACKNOWLEDGEMENT: The authors gratefully acknowledge the support from NSF Center for Power Electronic Systems (under award # EEC-9731677).

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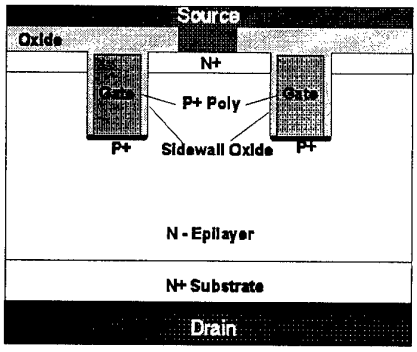


Fig.1 Schematic cross section of the trench JFET

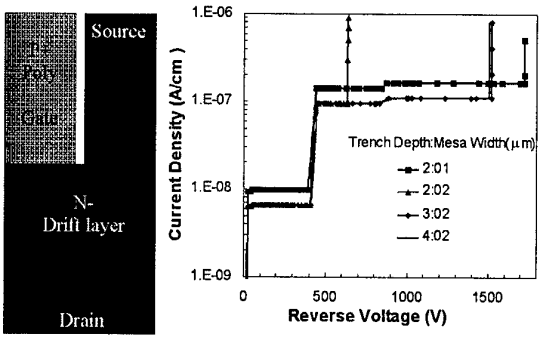


Fig. 2 Simulation structure (a: left) and forward blocking characteristics (b) of the trench JFET

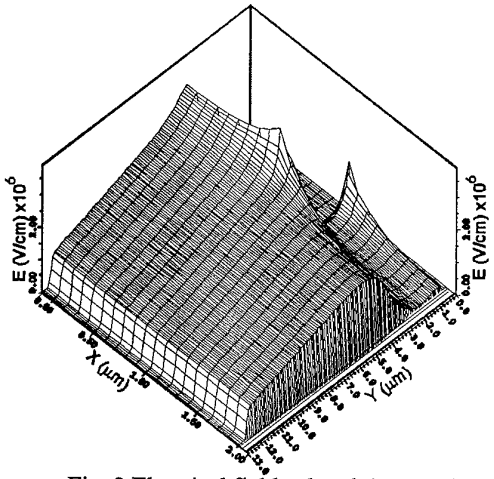
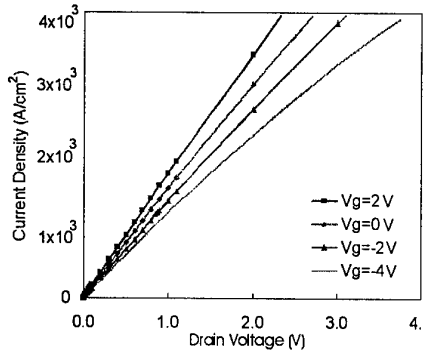


Fig. 3 Electrical field at breakdown voltage



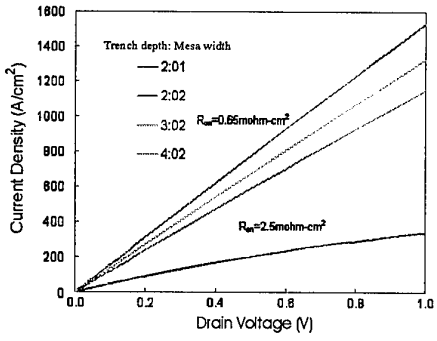


Fig. 4 Forward conduction characteristics

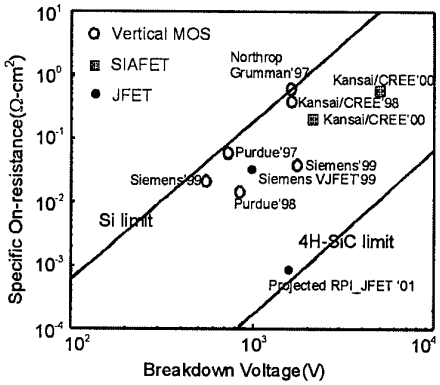


Fig. 5 Demonstrated MOSFETs and JFETs in 4H- and 6H-SiC and comparison with our projected JFET

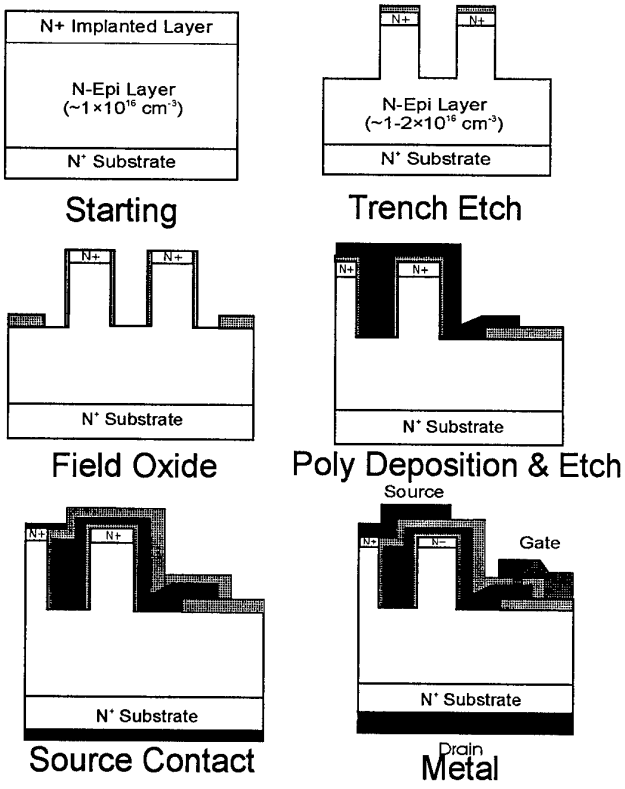


Fig. 6 Steps of the JFET Fabrication

Design and Fabrication of Dual-Gate 4H-SiC JFETs

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Dual-Gate JFETs, consisting of a buried p+ gate (4H-SiC(0001) Si-face substrate) layer, n-type channel layer doped in the low 10^{16} cm^{-3}, and top p+ gate layer were designed and fabricated. These particular devices were designed to be normally-on, with a pinch-off voltage of approximately minus one volt, for use in analog I.C.'s exposed to harsh environments. These desired parameters dictated the doping concentration and thickness of the n-type channel epitaxial layer. Following the one-dimensional design and two-dimensional simulation using Atlas software from Silvaco, the actual fabrication of these devices began with the growth of n channel and p+ cap epitaxial layers on 4H p-type SiC substrates. The growth was performed in a horizontal cold-wall CVD reactor on a graphite susceptor at a set point of 1535°C. The n channel layer and p+ cap layer were grown using a fixed Si/C ratio to establish an n-type doping level of 2×10^{16} cm^{-3} and the introduction of trimethlyaluminum (TMA) to establish degenerate p-type doping. The two layers were grown consecutively in separate n and p+ growth runs. All etching was conducted using reactive ion etching, and metal deposition was conducted using DC sputtering for nickel and thermal evaporation for titanium-gold. The source and drain implantation was conducted at 500°C using nitrogen, as follows: 1.12e15 cm^{-2} at 220 keV, 1.1e15 cm^{-2} at 190keV, 1.09e15 cm^{-2} at 150 keV, and 0.92e15 cm^{-2} at 90 keV. A photograph of the JFET die is shown in Fig. 1 along with the device cross-section. Both single-finger devices and multi-finger devices were fabricated, using gate widths of 290 μm and gate lengths of 12, 16, and 20 μm, along with test structures.

Subsequent characterization of the devices confirmed that the performance of the dual-gate JFETs was much improved over that of the single-gate JFETs. For the dual-gate JFETs, a typical pinch-off voltage around 2 volts was observed, with transconductance from 0.151 to 0.845 mS/mm. The single-gate JFETs exhibited a typical pinch-off voltage around 0.5 volts, with transconductance from 0.047 to 0.057 mS/mm. In Fig. 2, the improvements in current and gate control are clearly visible. As fabricated, the JFETs function as expected, but greater current and transconductance should be realized by simply scaling down the gate length and reducing the series resistance in the source and drain regions.

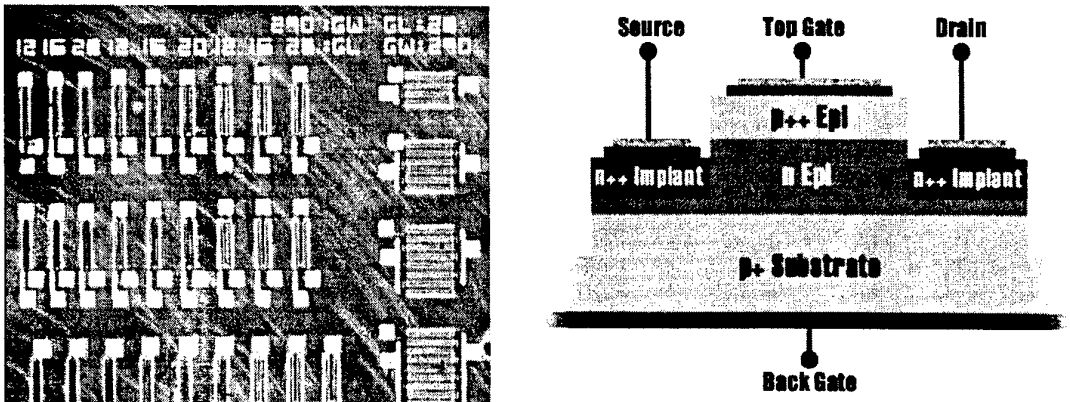


Fig. 1. Plan view (left) of the JFET die. Note varying gate lengths (12, 16, 20 μm), denoted by "GL". Also note the interdigitated multi-finger devices on the right and the TLM test structures at the bottom. The cross section (above) shows the device structure.

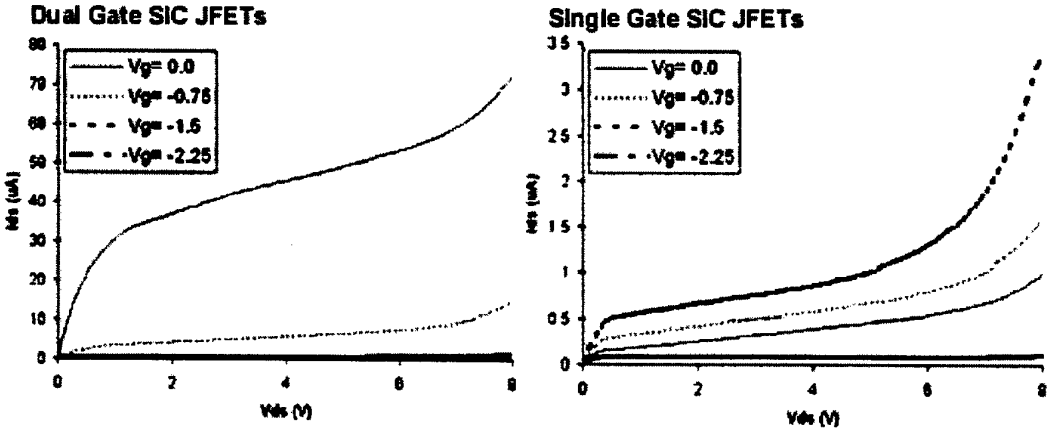


Fig. 2. Comparison of dual-gate versus single-gate single-fingered SiC JFETs with gate lengths of 20 μm and gate widths of 290 μm. Note that the ratio of I_{DS} (dual-gate) to I_{DS} (single-gate) is approximately 50 at a V_{DS} of 4V.

4H- and 6H-SiC MOSFETs Fabricated on Sloped Sidewalls Formed by Molten KOH Etching

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Introduction: SiC power MOSFETs, probably an ideal switch with normally-off operation, have suffered from an unacceptably low channel mobility. Vertical trench-gate UMOSFETs possess an advantage of higher cell density, leading to lower effective MOS channel resistance than planar DMOSFETs. SiC UMOSFETs have, however, exhibited very low inversion channel mobilities of 1~5 cm^2/Vs (the best: 14 cm^2/Vs [1]) and high threshold voltages of 8~15 V. This poor performance may be attributed to a high density of interface states as well as plasma damage on the sidewalls introduced during dry etching to create the trench structure. In this work, the authors have fabricated vertical 4H- and 6H-SiC MOSFETs on sloped sidewalls formed by molten KOH etching. The performance of MOSFETs on damage-free sidewalls with different slope angles and crystal orientations is discussed.

MOSFET fabrication: The schematic structure of a fabricated MOSFET is illustrated in Fig.1. The starting material was n^+/p/n-type 4H- or 6H-SiC epilayers grown on n^+-type off-axis $(000\bar{1})$ substrates. Sloped sidewalls were formed by molten KOH etching at 450~500°C with 1μm-thick Al as a mask. The slope of sidewalls could be controlled by adjusting etching temperature, the steeper slope for the higher etching temperature. A typical cross-sectional SEM image of the sidewall is shown in Fig.2. The slope angle is approximately 36° in this case, and the surface is rather flat without roughening and facetting. After sacrificial oxidation, 45~56 nm-thick gate oxides were formed by wet-oxidation at 1050°C for 70 min. The channel length is 8.5~10.7 μm, depending on the slope angle, and the channel width is 150 μm. MOSFETs were fabricated on sidewalls inclined toward $(1\bar{1}00)$ or $(11\bar{2}0)$ to investigate the crystal orientation dependence.

Results and Discussion: All the MOSFETs fabricated were operational with normally-off characteristics as shown in Fig.3. The channel mobility and threshold voltage strongly depend on the slope angle, crystal orientation, and polytype, as expected. The highest mobility was 15 cm^2/Vs for 4H-SiC and 32 cm^2/Vs for 6H-SiC MOSFETs which were obtained on the sidewall inclined toward $(1\bar{1}00)$ with an angle of 36° formed by etching at 475°C. These values are reasonably high as an inversion channel mobility, compared to previous works published by several institutes (It should be noted that the bulk mobility in 6H-SiC along this direction is low, ~140 cm^2/Vs, due to the large anisotropy). Figure 4 represents the average channel mobilities (μ_{FE} at V_G~10V) determined from transfer characteristics of several MOSFETs fabricated on various sidewalls. Higher channel mobility was obtained for MOSFETs with a larger slope angle in the investigated range. Since the SiC$(000\bar{1})$ face generally shows poor MOS interface quality, the channel mobility may have been improved by increasing the inclination (slope angle) from the SiC$(000\bar{1})$ face in this study. Surprisingly, the MOSFETs on the sidewall 36°-inclined toward $(1\bar{1}00)$ exhibited a higher channel mobility, compared to the MOSFETs inclined toward $(11\bar{2}0)$.

This result might be inconsistent with previous works [2,3], where the $(11\bar{2}0)$ face provides low interface state density and high channel mobility. However, the sloped sidewalls have specific bond configuration different from the exact $(11\bar{2}0)$ or $(1\bar{1}00)$ faces. The threshold voltage was determined to be 2.5~4.6 V for 6H-SiC and 5.5~7.1 V for 4H-SiC MOSFETs, and was high for a MOSFET with a low channel mobility. This correlation indicates that the electron trapping and Coulomb scattering may limit the channel mobility, as in SiC(0001) MOSFETs. Thus, the choice of crystal orientation is important even in fabrication of UMOSFETs on SiC{0001} wafers.

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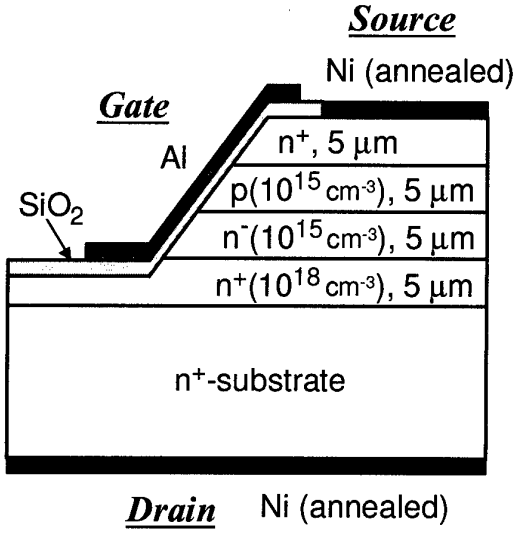


Fig.1 Schematic structure of a fabricated MOSFET.

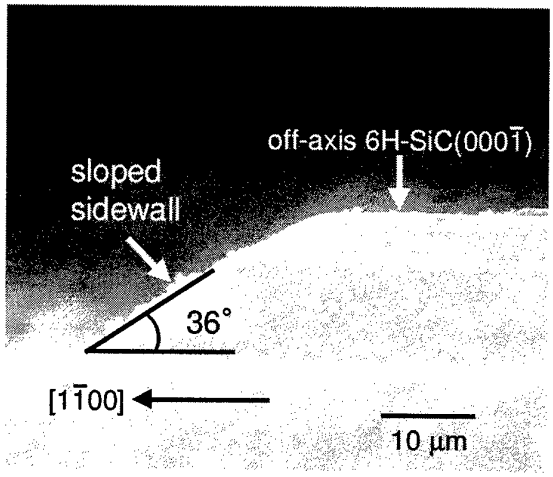


Fig.2 Cross-sectional SEM image of a sloped sidewall. (6H-SiC inclined toward $(1\bar{1}00)$, etching at 475°C)

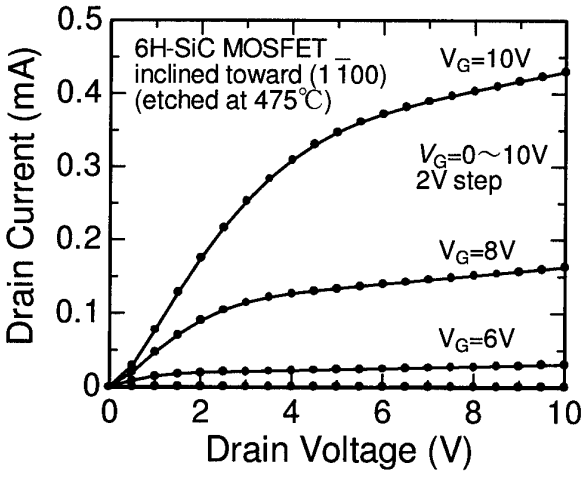


Fig.3 Typical drain characteristics of a MOSFET. (6H-SiC inclined toward $(1\bar{1}00)$, etching at 475°C)

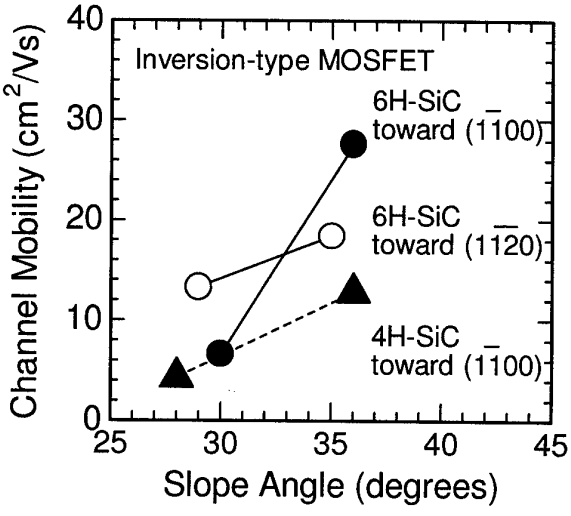


Fig.4 Channel mobility as a function of slope angle, crystal orientation, and polytype.

The development of ultra high frequency power 6H-SiC vertical static induction transistor with p-n junction as a gate

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Silicon carbide has attracted considerable interest as a material for high power, high frequency devices. The unique such properties as high thermal conductivity, anomaly large breakdown fields and others are perspective potential for a development effective devices for a microwave region particularly. During the last ten years new results from the strong field vertical (along C axis) transport study on silicon carbide polytypes were obtained which are very perspective for microwave operation [1]. In the first place it is the discovering of negative differential conduction caused by electron Bragg reflection from miniband edge in natural superlattice.

A transistor with static induction (SIT) is one of the highly efficient and power microwave device. A development of microwave SiC power transistor with vertical design has a great interest now [2]. Such transistor was formed with Shottky gate contact [3], that reduces the work temperature and radiation limits. The p- n junction employment instead the Shottky gate contact enhances these limits essentially.

On the base of n^+-substrate we created n^-- epi layer with concentration 10^{15} - 10^{16} cm^{-3} and width 2-5 μm, which is covered by n^+- top layer (0.2-0.3 μm). On the base of such n^+- n^- - n^+ structure by special technology the SiC unipolar static induction transistor with p-n junction as a gate have been developed for the first time. The current channel sizes were equaled to 40 x 2 x 3 μm^3, fig.1. So far we fabricated the simple variant of this transistor with the periphery 200 microns, therewith the effective devices have the periphery 1cm and more [3]. The I-V characteristic presented SIT shown in fig.1 has two ranges: linear and breakdown (there are experimental data proving its breakdown nature). The influence of the gate voltage on the linear range is the same as in transistor. The parameter S is equaled to S = 4 mA/V (fig.2, a). It is a little value due to the little periphery. If the periphery is increased in 50 times S will be 200 mA/V. The breakdown region is caused by mobile domain which arises because of negative differential conduction caused by electron Bragg reflection from miniband edge in natural superlattice [1]. It is unusual breakdown. It arises in a field equal 150 kV/cm. This field is much less than breakdown field in 6H-SiC equal 2000-2500 kV/cm. But the field in mobile domain is much more than surrounding field in the channel and it provides the breakdown. If it is right the breakdown has to be removed by the domain destroying. It is done by subjecting the cross field of the gate to the domain. Really, we are observing at the some gate voltage a drastic current drop in the channel (Fig.2 a, b). Such switch off effect perhaps is a very interesting from developing novel device of view. A future investigation will show as far as it is the power and rapid effect. But it should be emphasized that we know how to design such transistor to remove the breakdown range and to create the device with transistor effect only.

Thus, this investigation can give the base for developing such novel devices as:

1. The unipolar microwave SiC power transistor with vertical design or SIT.
2. The microwave generator and amplifier based on the Bragg reflection effect in natural SiC superlattice.
3. The power and rapid switch off SiC device.

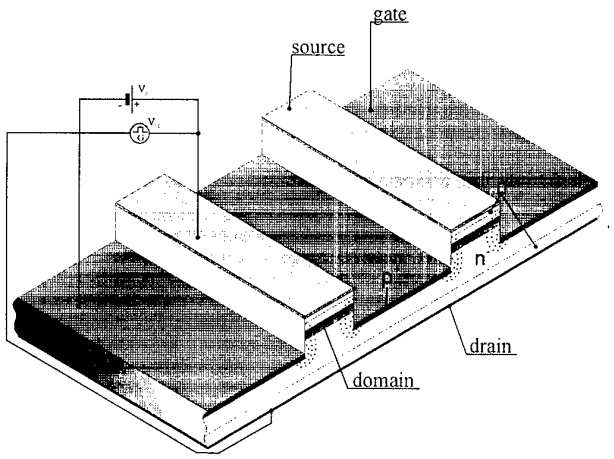


Fig.1. The common view of static induction transistor structure with mobile domain in channel.

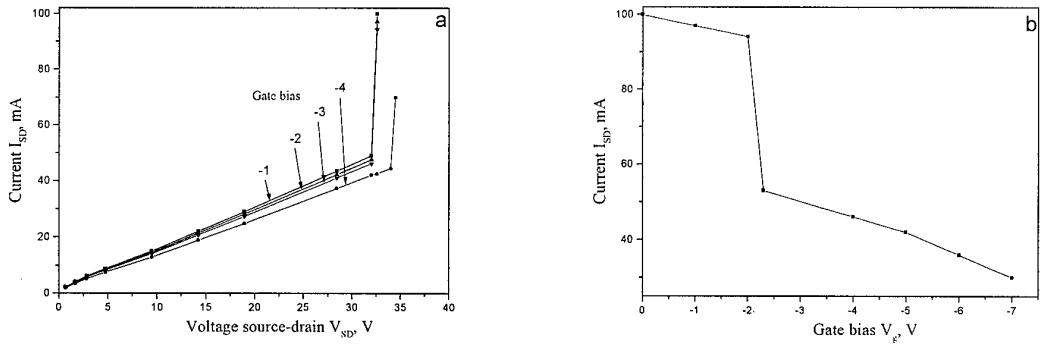


Fig.2. I_{DS}-V_{DS} characteristics (a) and I_{DS}-V_g characteristics (b).

The partial financial support of Russian Foundation of Fundamental Research project 00-02-16943 and Russian Science Program «Physics of Solid State Nanostructures» project 97-1038 is gratefully acknowledged

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Fabrication and initial characterization of 4H-SiC epilayer channel MOSFETs

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Power electronics technology wants SiC MOSFETs. Although steady progress has been made, many obstacles need to be overcome to realize practical SiC MOSFETs. A promising solution to improve the on-state characteristics of SiC MOSFETs is the use of accumulation epilayer MOS channel [1, 2]. In this paper, we report on fabrication processes (especially on channel epilayer growth) and initial characterization of newly-designed 4H-SiC single-implanted epi-channel MOSFETs.

The structure of the MOSFETs fabricated in this work is shown in Fig. 1. A substrate used for the MOSFET processing was 8° off (0001) 4H-SiC. A 14-μm-thickness n-epilayer (1st epilayer, 8e+15 cm^{-3}, drift layer) was grown on the substrate using our hot wall CVD system. The p-type body region (2e+18 cm^{-3}, 0.8μm thickness) was formed by box-profile Al ion implantation (1.8e+14 cm^{-2}, 40-700 keV) through a patterned SiO_2 mask. After removal of the SiO_2 mask, a 0.5-μm-thickness n-epilayer (2nd epilayer, 1e+17 cm^{-3}, channel layer) was grown onto the epiwafer. Recently, we investigated structural and electrical quality of epilayers grown on an Al-ion-implanted layer [3]. No degradation in the epilayer quality was observed for the Al implantation dose up to 1.8e+15cm^{-2}, thus we consider that the quality of the 2nd epilayer for the MOSFETs is high enough to fabricate MOS channel. Activation annealing for the p-body Al acceptors was performed just after the 2nd epilayer growth in the CVD reactor at 1750 °C for 45 min in an Ar ambient. In general, activation annealed SiC surfaces have several problems, such as bunched steps, selective desorption of Si atoms and impurity adsorption. In our case, neatly aligned steps of 30-40 nm height (this value is comparable to gate oxide thickness) were emerged and a thin layer of very low resistivity was formed on the surface. To remove the surface layer, we etched the epiwafer surface by RIE to the depth of 0.1 μm. Epitaxial growth is an effective measure to obtain flat SiC surface. To flatten the epiwafer surface, an n-type 3rd epilayer (1e+19 cm^{-3}, source contact layer) was grown onto the etched surface. After the 3rd epilayer growth, while grooves decorated by the epitaxial growth remained thinly on the surface, the surface roughness was improved markedly. Next, the surface epilayer in the channel and p-body contact regions were etched off by RIE. We set the remaining n-epilayer thickness in the channel region at 0.24 μm, aiming at normally-off MOSFET operation. A sacrificial oxide was grown at 1100 °C for 2 h. After removal of the sacrificial oxide, the gate oxidation was performed in an O_2/H_2O ambient at 1100 °C for 2 h, followed by a reoxidation in the same ambient at 950 °C for 2 h. p-Body contact and non-annealing ohmic contact to the n^+ source and backside drain regions were formed by Al. Al gate electrode was formed by e-beam evaporation. Fig.2 shows a top view photograph of the fabricated MOSFET. The comb shape gate of the MOSFET is 5 μm long and 20x600 μm wide. Ten gate electrode fingers (each gate finger contains two MOS channels) are aligned in the 600x630 μm^2 active area.

Fig. 3 shows I_D-V_D characteristics of the MOSFET. Normally-off operation with I_D at V_G=0 V being

in the system noise is obtained. On-resistance calculated from the slope for V_G=20 V is 102 mΩcm^2. Fig. 4 shows I_D-V_G characteristics of the MOSFET. Field effect mobility, μ_{FE}, is estimated to be 13.9cm^2/Vs in the low V_G range. However, with an increase in V_G, the μ_{FE} decreases steeply to the normal μ_{FE} value of 4H-SiC inversion MOS channel. Details of the V_G dependence of the μ_{FE} are not clear, but we speculate that the behavior is ascribed to the near conduction band edge carrier traps, which is a vital problem in 4H-SiC MOSFETs. Typical breakdown voltage at V_{GS}=0 V was 350-400 V. After breakdown, melting of electrode metal was observed on the periphery of electrodes near the guard ring. The immature breakdown is possibly due to the guard ring which is not optimized. Further extensive improvements are required to obtain practical SiC MOSFETs.

This work was performed under the management of FED as a part of the METI project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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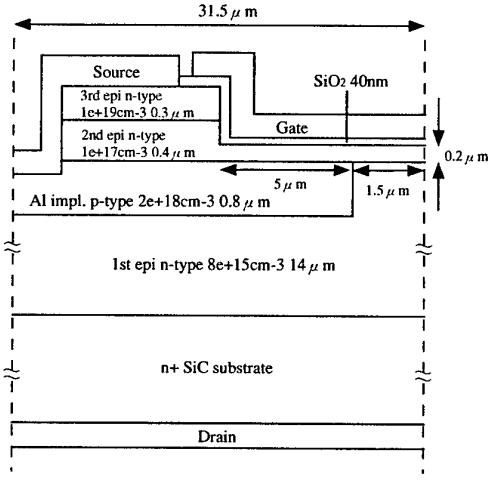


Fig.1 Schematic cross section of a MOSFET cell.

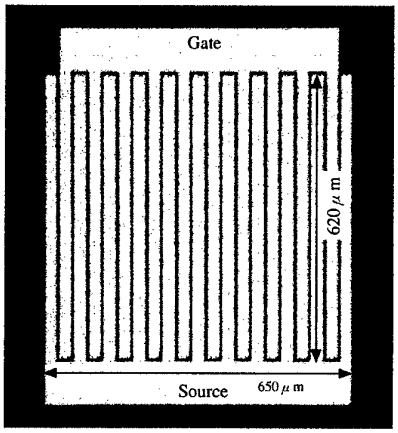


Fig. 2 Top view of fabricated MOSFET.

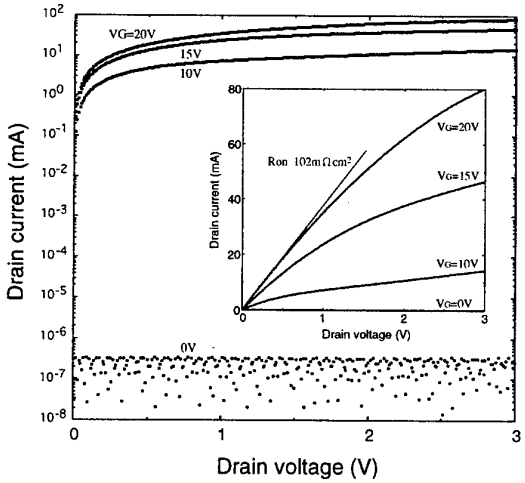


Fig. 3 I_D-V_D characteristics of fabricated 4H-SiC MOSFET.

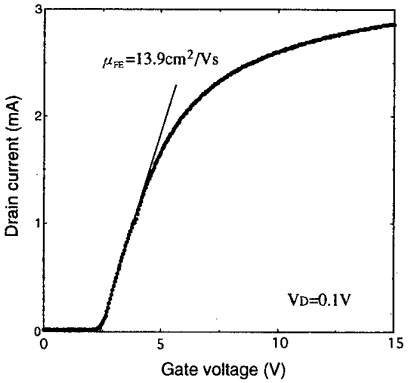


FiG. 4 I_D-V_G characteristics of fabricated MOSFET.

Evaluation of SiC MESFET structures using large signal time domain simulations

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The SiC MESFET is a promising component for applications such as high power amplifiers and high level mixers in the 2-12 GHz range. To realise these promises a good understanding of how to optimise the performance of the transistors when using real materials is needed. Semi-insulating 4H-SiC substrates have a high density of crystalline defects like micropipes, screw and edge dislocations. The substrates can also have a high density of intrinsic defects that create trapping levels in the band gap. To lessen the negative influence of the substrate, a p-type buffer layer is usually grown between the substrate and the channel layer. The resulting pn-junction aims to isolate the channel from the substrate. In this way a low parasitic output conductance at dc can be achieved. Experiments have however indicated that the large signal response of the transistor at higher frequencies can be very poor also when the dc-characteristics are good. It is therefore important to have a better understanding of how the p-type buffer layer doping and thickness affects the output rf power.

In this abstract we describe a novel way to investigate the large signal time domain response of 4H-SiC MESFETs. We have utilised the device simulator Medici in time domain circuit simulations of different SiC transistor structures. A simple amplifier circuit was used where a dc bias and an rf input voltage were applied to the gate while a dc bias and an rf output voltage were simultaneously applied to the drain terminal acting as an active matching to the transistor [1]. The matching conditions were adjusted by altering both the amplitude and phase difference of the rf voltage source at the gate and drain. The rf active matching voltage source connected directly to the drain terminal delivers a sine wave at the fundamental frequency thereby acting as a short at the higher harmonic frequencies. The results from the time domain simulations (terminal voltages and currents) were Fourier transformed and then input and output power and impedance, PAE etc as a function of frequency could be calculated. The method indicates the output power that can be achieved in the best case with pure sinusoidal input and output voltages, and we believe it to be a valuable design tool for the improvement of high frequency characteristics of power semiconductor devices. All simulations were performed with a fixed lattice temperature of 300 K. A number of SiC MESFET structures was simulated. Figure 1 shows the simulated class B drain current and voltage waveform for a structure with a 1500 nm thick p-type buffer layer with an unintentionally graded doping varying from 1×10^{17} cm^{-3} in the upper part to 1×10^{15} cm^{-3} next to the substrate. The channel layer had a nominal n-type doping of 2×10^{17} cm^{-3} and was 500 nm thick.

Measurements on a similar device showed a good dc characteristic with a complete channel pinch off at –9 V and a maximum of drain current of 250 mA/mm. The measured output rf power was however low.

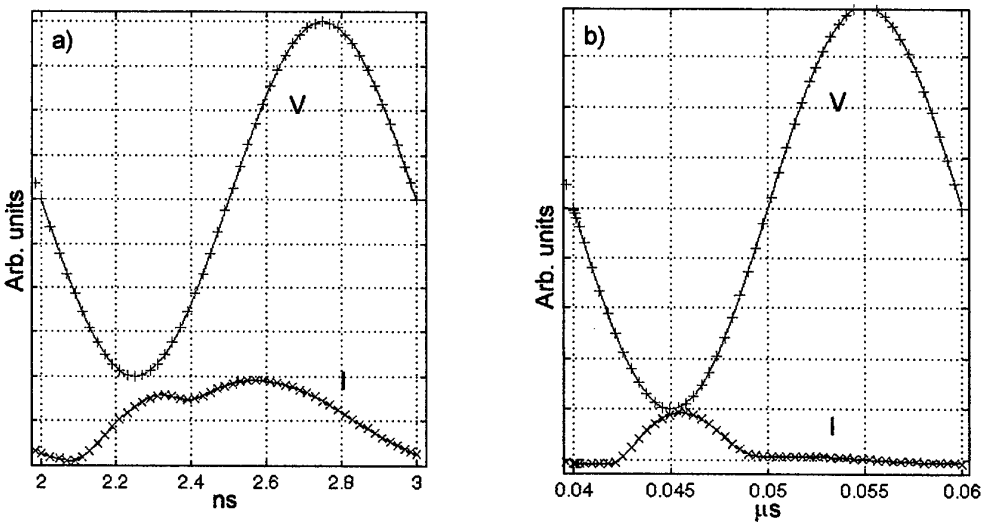


Figure 1. Class B drain current and voltage waveforms for a transistor with a thick buffer at 1 GHz (a) and 50 MHz (b).

As can be seen the device works well at 50 MHz but at 1 GHz the transistor is not delivering any power to the load due to the out of phase maximum of the drain current. The details of the simulation analysis indicated that this abnormality in the drain current is due to interaction with the p-type buffer layer. This phenomenon was not observed in dc or small-signal rf simulations.

Several other MESFET structures have been evaluated in order to obtain better rf powers. Figure 2 shows the simulated results for a structure with a 100 nm thick p-type buffer layer with a doping of 3×10^{17} cm^{-3}. The channel layer had an n-type doping of 4×10^{17} cm^{-3} and was 300 nm thick. The simulation indicates an output power of 4.5 W/mm with a 56% PAE at 1 GHz.

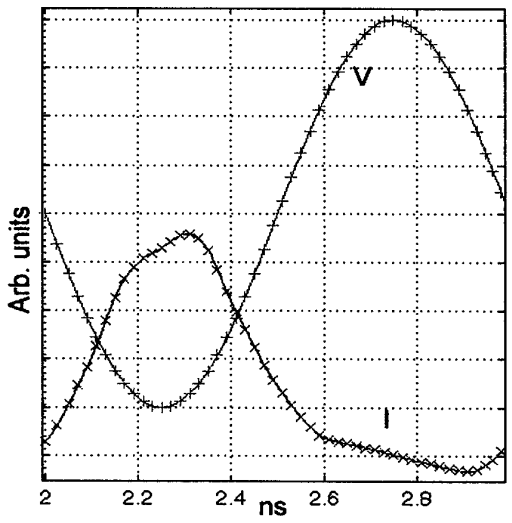


Figure 2. Class B drain current and voltage waveforms at 1 GHz for a transistor with a thin highly doped buffer.

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Surface control of 4H SiC MESFETs

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The high breakdown voltage, thermal conductivity, and saturated velocity make silicon carbide highly suitable for microwave device applications, with 80W CW and 120W pulsed demonstrated at 3.1GHz and >4W/mm power density demonstrated for SiC MESFETs [1]. However, SiC MESFETs have been reported to suffer from dispersion and instabilities in current with time. These instabilities take the form of "current collapse" when operated under CW bias conditions. This has serious implications for the use of these devices in microwave power amplifiers. The instability has been reported to be either due to surface charge trapping between the source and drain contacts on either side of the gate contact [2] or to bulk traps [3]. This work reports a significant reduction in this effect and demonstrates that the devices are capable of operation at temperatures as high as 400°C.

SiC MESFETs with sub-micron gates have been fabricated using conventional techniques as previously reported [4]. These devices have shown excellent rf power output under pulsed conditions, 17 watts has been achieved at 4GHz for a total gate width of 7.5mm, equivalent to 2.2W/mm. However these FETs show current collapse under CW conditions and the I/V characteristics are also light sensitive. Process improvements have been introduced which have virtually eliminated the light sensitivity and significantly reduced the amount of current collapse at CW. These have included an oxide passivation and a gate recess (figure 1). Devices have now been fabricated using this process and have achieved f_T=6GHz, f_{MAX}=18GHz for a 500/0.7μm device.

The improvement in current collapse may be illustrated by making pulsed measurements under different quiescent bias conditions. Figure 2 shows results using the modified process. The pulse measurements were made firstly with equilibrium quiescent conditions (Vds=0, Vgs=0). The pulse measurements were then repeated with a quiescent bias corresponding to class AB operating conditions (Vds=20V, Vgs=-15V). The pulse length was 0.5μs, with a 1000μs quiescent period. The optimised device shows only a small reduction in Idss for the class AB operating point indicating that current collapse has been significantly improved.

Figure 3 shows a slow swept IV characteristic for a device operating at an ambient temperature of 400°C with only a ~35% reduction in Idss. In addition, the gate current had only increased from <100pA/mm to 30μA/mm. This extremely good tolerance of high temperatures suggests these MESFET devices have the potential for highly reliable operation.

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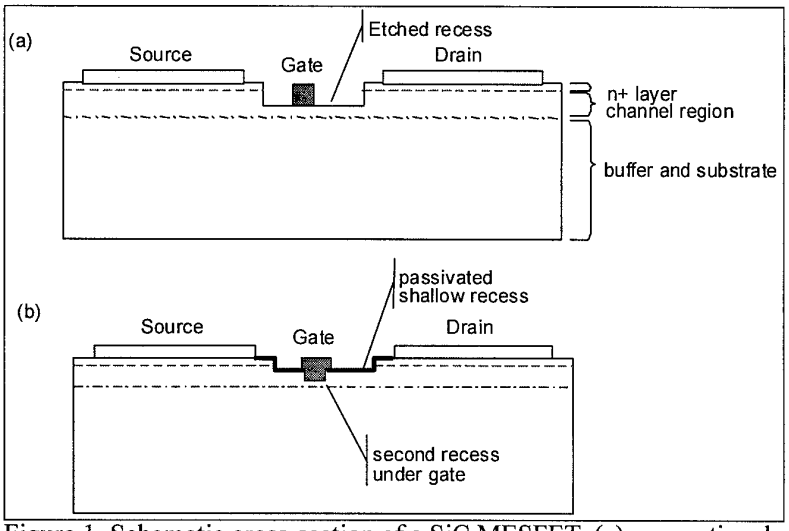


Figure 1. Schematic cross-section of a SiC MESFET. (a) conventional process, (b) improved process.

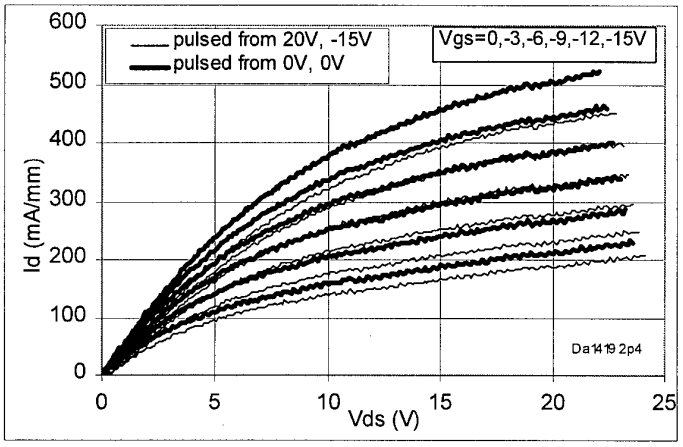


Figure 2. Pulse IV measurement of passivated 500/0.7μm MESFET.

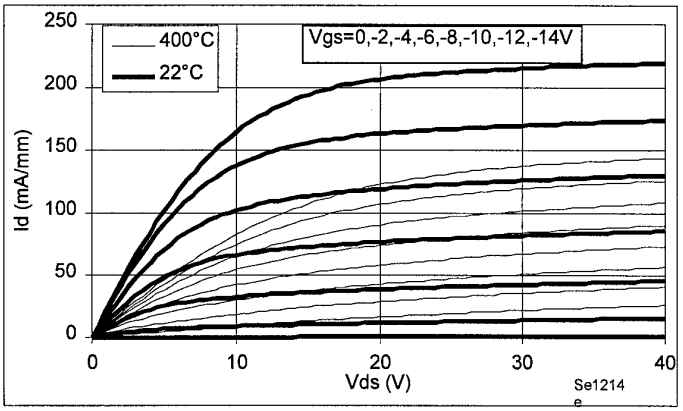


Figure 3. Comparison IV of 100/0.7μm MESFET at 22 and 400°C.

Photon emission analysis of defect-free 4H-SiC p-n diodes in the avalanche regime

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Knowledge of the actual uniformity of avalanche breakdown in 4H-SiC diodes is of great importance when developing electronic devices operating in this regime, i.e. SiC Zener [1] and IMPATT diodes [2]. Using a photon emission setup and observing through the substrate (Figure 1) the light associated with the avalanche, we have investigated the breakdown characteristics of silicon carbide p^+-n-n^+ 4H-SiC diodes.

For this work, the back side of epitaxial wafer has been polished before device processing in order to allow back side observations. Detailed description of other fabrication steps and electrical characterization of these diodes can be found elsewhere [1, 2]. The diodes exhibited a stable behavior under avalanche conditions and a positive temperature coefficient of breakdown voltage which indicated the absence of microplasma or defective sites. The avalanche regime occurs around 280 V at room temperature and is characterized by a strong luminescence in the optical range (from 1.1 to 3.1 eV) (Figure 2 and 3) which can be detected and spatially resolved by photon emission techniques.

The light emission properties and its relation with the current density (Figure 4 and 5) is first investigated at forward voltage bias as well as in avalanche regime in order to determine its physical origin. The electroluminescence is then used as a tool for assessing the breakdown uniformity of the diodes.

Our results show that in the detected range, light (noted I_ν) originates from the radiative recombination of injected holes in the n layer in the case of forward operation. In the case of avalanche operation, different hypothesis will be discussed. Whereas the light emission is uniform throughout the surface in the forward regime (Figure 2 (a) and (b)), it is not the case during avalanche breakdown. The breakdown seems to occur preferentially along parallel stripes independent of the diode location on the wafer and geometry (Figure 2 (c) and (d)). As the avalanche current is increased, the stripes widen and the emission tends to occur on the whole surface. To the best of our knowledge, this is the first time such observation is reported in 4H-SiC diodes. We believe that the stripes indicate regions of enhanced impact ionization but, contrary to microplasma, they do not seem to affect the electrical characteristics of the diodes and do not lead to catastrophic failure of the devices.

Similar electroluminescence striations in silicon p-n junctions at avalanche breakdown have been reported in 1963 [3]. At that time they were attributed to doping fluctuations due to the Czochralski process used to fabricate the diodes. In our case non uniform doping due to epitaxial growth can also be proposed as a mechanism for EL striations.

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This work was partially supported by INTAS – CNES 97-1386 grant. FORTH also acknowledges the support through NATO SfP 971879 grant.

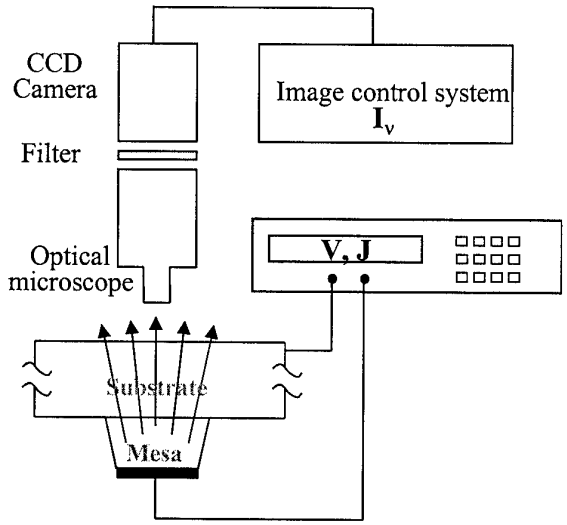


Figure 1 : Experimental setup (backside observation configuration).

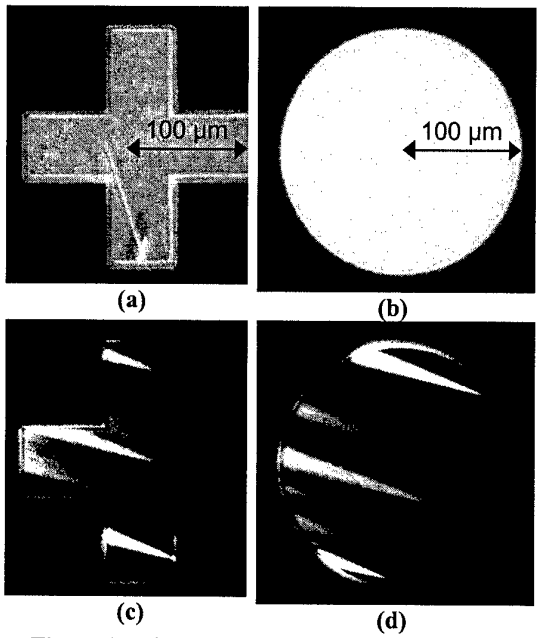


Figure 2 : Photon emission images of **(a)** & **(b)** forward biased diodes, **(c)** & **(d)** diodes under avalanche condition.

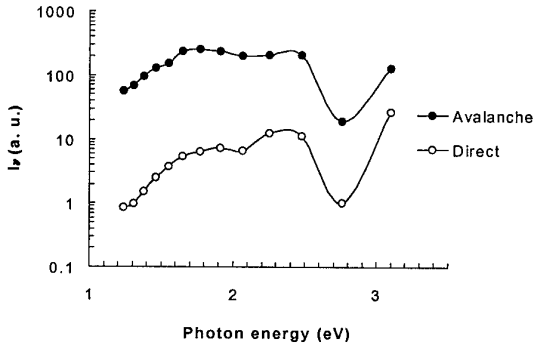


Figure 3 : Spectral analysis of the light emitted in direct and avalanche regimes.

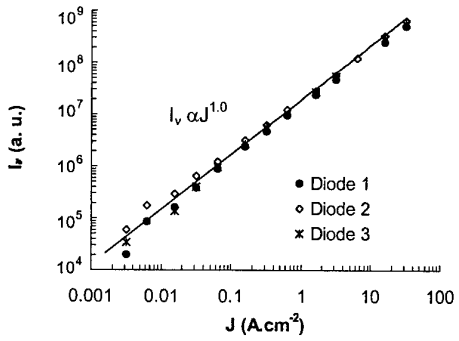


Figure 4 : Relationship between I_v and J in the avalanche regime.

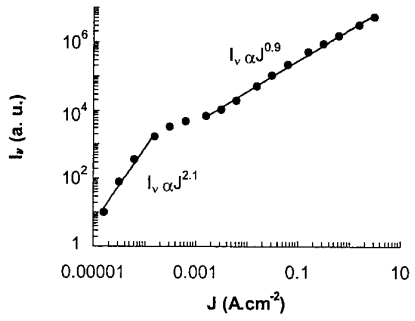


Figure 5 : Relationship between I_v and J in the recombination dominated ($I_v \propto J^{2.1}$) and injection dominated ($I_v \propto J^{0.9}$) forward regimes.

Silicon Carbide Microwave Limiters

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We report on the first microwave limiters fabricated from silicon carbide. Microwave limiters are two port microwave circuits intended to protect sensitive input circuits of communication and other microwave equipment against occasional power surges. Due to high thermo-conductivity, high operation temperature, and short recovery time, silicon carbide diodes are attractive devices to build high power microwave limiters.

We report on modeling and experimental results on development of SiC based microwave limiters. Ni based Schottky diodes were fabricated implementing all nickel technology for ohmic and Schottky contacts fabrication. We used 6H-SiC commercial epi-structure with base layer of 2.5 μm thick and doping level 2×10^{15} cm^{-3} for diode fabrication. Circular diodes of 200 μm diameter were fabricated. Diode chips were diced and assembled in microwave fixture for small signal microwave measurements. Small signal insertion and return loss were measured for 6H-SiC Schottky diode in the frequency band from 0.04 to 2.00 GHz. Small signal insertion loss for 6H-SiC diode loaded in parallel 50 Ω transmission line is lower then 1.5 dB up to 0.6 GHz. Return loss (reflection) varies from –25 dB at 0.04 GHz to –12 dB at 0.6 GHz and -6 dB at 2.0 GHz.

It was shown that simplified circuit consisting of two parallel back-to-back Schottky diodes with described above parameters can operate as microwave limiter up to 0.6 GHz. Broadening of operating frequency range requiring diodes and circuit optimization will be discussed.

This work is supported by ONR (contract monitor John Zolper).

4H-SiC MESFET Large Signal Modeling Using Modified Materka Model

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4H-SiC(silicon carbide) MESFET large signal model was studied using modified Materka-Kacprzak model [1]. The MESFET characteristics for the large signal model were obtained from a device simulation using Silvaco's 2D device simulator, ATLAS. The simulated device structure is shown at Fig 1 [2]. The device simulation results was compared with the reported data of the same strucutre [1] and showed a good agreement. The small signal and large signal model was established from the MESFET characteristics. For the large signal modeling modified Materka model was employed. Fig 2 and Fig 3 show the comparison between simulated and modeled data. The small signal model showed a good match between measured (simulated) and modeled data with a small error rate in S-parameters (Table 1). The modeled large signal parameters are shown at Table 2. Both measured (simulated) and modeled results showed identical DC characteristics, i.e., -8V pinch off voltage, Gm of 45㎳/㎜ and I_{DSS} of 270㎃/㎜ under V_{GS}=0V, V_{DS}=25V conditions. Based on the large signal parameters, power characteristics are predicted. From the Class A power simulation at 2GHz and at the bias of V_{GS}=-4V and V_{DS}=25V, a 10dB Gain, a 34dBm (1dB compression point) output power, a 7.6W/㎜ power density, and a 37% PAE(power added efficiency) were obtained (Fig. 4). The power simulation results are compatible with the reported results. As the IIP3 (input third order intercept point) is about 10 dB higher than input P1dB, IIP3 is expected to be around 34 dBm.

Acknowledgement

This work was done as a part of SiC Device Development Program(SiCDDP) supported by MOCIE(Ministry of Commerce, Industry and Energy), Korea.

Reference

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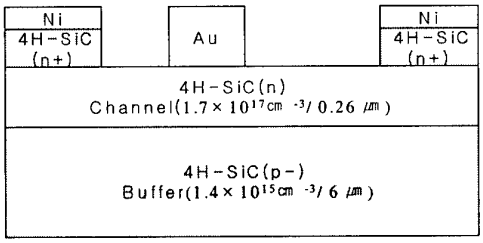


Fig 1. Cross section of a 4H-SiC MESFET

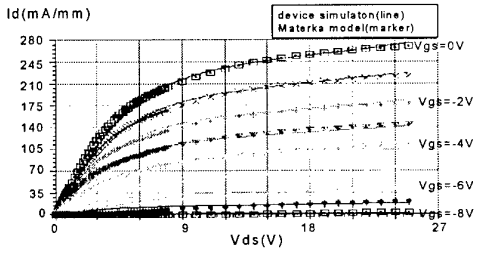


Fig 2. I-V characteristics of a 4H-SiC MESFET

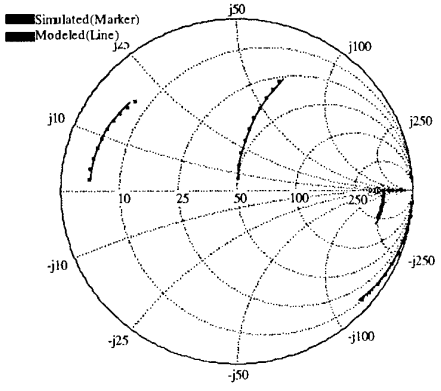


Fig 3. Simulated and Modeled S-parameter at V_{GS}=-4V,V_{DS}=25V, 1GHz-10GHz

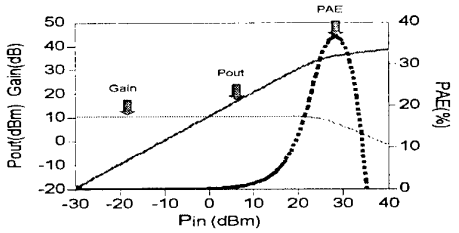


Fig 4. Power simulation for a 4H-SiC MESFET at 2GHz

S_{11}	S_{21}	S_{12}	S_{22}
2.2%	6.7%	3.6%	4.5%

Table 1. Error rate of simulated and modeled S-parameter

IDSS 0.6879E-1 (A)	*K1* 1.6
VP0 -8 (V)	*C1S* 0.127E-13 (F)
GAMA -0.125E-1 (1/V)	*CF0* 0.605E-13 (F)
E 0.92	*KF* 0.62 (/V)
KE -0.115 (1/V)	*RG* 3.45 (Ω)
SL 0.17E-1 (A/V)	*RD* 5.13 (Ω)
KG 0.25E-2 (/V)	*RS* 3.57 (Ω)
T 0.39E-13 (sec)	*LG* 0.54E-10 (H)
SS 0.95E-3 (A/V)	*LD* 0.19E-10 (H)
IG0 0.1E-30 (A)	*LS* 0.84E-09 (H)
AFAG 20.55 (/V)	*CDS* 0.11E-13 (F)
IB0 0.25E-2 (A)	*CDSD* 0.12E-08 (F)
AFAB 1.2 (/V)	*RDSD 706* (Ω)
VBC 200 (V)	*CGE* 0.82E-13 (F)
R10 13.99 (Ω)	*CDE* 0.85E-14 (F)

Table 2. Large signal model parameter of 4H-SiC MESFET at 1-10GHz

Optical Properties of Metallic Nanocrystals in SiC

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ABSTRACT

Nanocrystals of gold, silver, copper and tin are produced in 6H-SiC. This is accomplished by implanting Au, Ag, Cu, and keV Sn into SiC at room or elevated temperature followed by annealing at various temperatures. Using optical absorption spectrophotometry, we determined the location of the absorption band due to metal nanocrystals in SiC, as well as their average size. Elevated temperature implantation reduces optical absorption in the substrate due to ion implantation induced defects.

INTRODUCTION

The exceptional properties of SiC, as a high-temperature wide-bandgap semiconductor possessing a high index of refraction and high fracture toughness, make it a suitable candidate for device fabrication in harsh environments. In recent years, more attention has been given to both linear and nonlinear properties of the material caused by optical absorption due to the surface plasmon resonance frequency, which depends on the index of refraction of the host substrate and the electronic properties of the colloids formed in the host material. The nonlinear properties allow the manufacturing of a wide range of optical devices. Ion implantation followed by thermal annealing has been used to introduce similar effects near the surface and to change the nonlinear optical properties. An attractive property of ion implantation is that the ions can be focused to introduce the linear and nonlinear properties in a well-defined space in an optical device.

It has long been known that small metallic particles or colloids embedded in dielectrics produce colors associated with optical absorption at the surface plasmon resonance frequency. For clusters with diameters much smaller than the wavelength of light (λ), the theories of Mie can be used to calculate the absorption coefficient (cm^{-1}) of the composite:

$$\alpha = \frac{18 \cdot \pi \cdot Q \cdot n_0^{\,3}}{\lambda} \times \frac{\varepsilon_2}{\left(\varepsilon_1 + 2 \cdot n_0^{\,2}\right)^2 + \varepsilon_2^{\,2}} \qquad (1)$$

where Q is the volume fraction occupied by the metallic particles, n_0 is the refractive index of the host medium, and ε_1 and ε_2 are the real and imaginary parts of the frequency-dependent dielectric constant of the bulk metal. Equation (1) is a Lorentzian function with a maximum value at the surface plasmon resonance frequency (ω_p), where:

$$\varepsilon_1(\omega_p) + 2 \cdot n_0^{\,2} = 0 \qquad (2)$$

Values of ε_1 for the metals as a function of wavelength are tabulated and the published index of refraction for SiC is 2.655. The index of refraction, measured by prism coupling, for

the SiC used in this work was 2.26. From Equation (2) one can predict the photon wavelengths for the surface plasmon resonance frequencies for metallic colloids in the photorefractive host materials. For the in-house measured index, n_0 = 2.26, the absorption bands for SiC with Au, Ag, Cu, and Sn colloids shift to 625 nm, 509 nm, 617 nm, and 382 nm, respectively.

RESULTS AND DISCUSSION

We have implanted SiC crystals with ions such as 2.0 MeV Au, 3.0 MeV Ag, 2.0 MeV Cu, and 100 keV Sn at fluences between 5 x 10^{15}/cm^2 to 3 x 10^{17}/cm^2 both at room temperature and at 500°C.

Figure 1 shows typical optical absorption spectra for SiC implanted with MeV Au and annealed at 1000°C in ambient argon. As implantation fluence increases the absorption baseline shifts. Using the measured absorption band, 628 nm, and Equation (2), the calculated index of refraction for SiC at the implanted volume is 2.3. As the annealing temperature increases, the index of refraction becomes larger, resulting in a red shift in the absorption band.

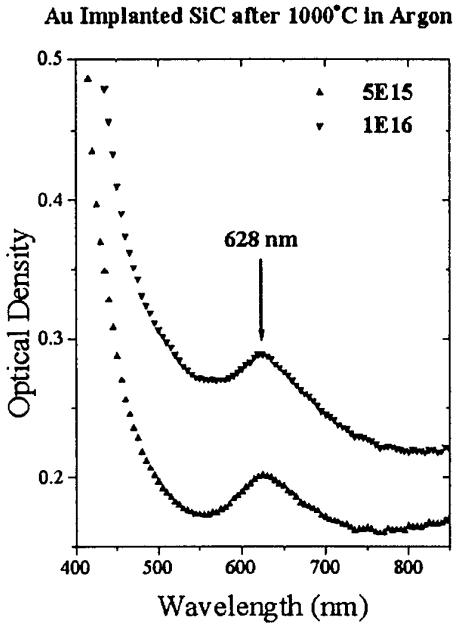


Figure 1. Gold implanted SiC, after heat treatment, at two different ion fluences.

Similar results for Ag, Cu and Sn implantations produced absorption bands at 493 nm, 659 nm, and 406 nm.

CONCLUSION

Metallic nanocrystals formation was observed in SiC implanted with Ag, Au, Cu and Sn ions. Implantation at room temperature results in a large increase in optical absorption that can mask the surface plasmon resonance absorption band. Implanting at elevated temperature (500°C), which inhibits the formation of defects, alleviated this difficulty. The broad plasmon resonance for each absorption band indicates that the nanocrystals are very small.

ACKNOWLEDGMENTS

This work is supported by the Center for Irradiation of Materials at Alabama A&M University and NASA-GRC Contract No. NAG3-2123. The work at ORNL was sponsored by the U.S. Department of Energy under contract DE-AC05-00OR22725 with the Oak Ridge National Laboratory, managed by UT-Battelle, LLC.

[redacted]

ThA1 Epitaxial Growth 1

Effect of the Si droplet size on the VLS growth mechanism of SiC homoepitaxial layers

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For some applications as electrical power conditioning and distribution, thick (several tens of μm) active drift SiC epilayers are required. Until now, only high temperature processes (> 1700°C) such as sublimation sandwich method, liquid phase epitaxy (LPE) and high temperature CVD are able to provide high growth rates suited for thick layer deposition. Vapour-Liquid-Solid (VLS) mechanism has demonstrated as high growth rate as several mm/h at 1100°C for SiC whiskers [1]. The transposition of such a mechanism to SiC epilayer growth would combine the advantages of the CVD technique (growth control) with the ones of the LPE technique (low supersaturation). However, the main problem to solve is the increase of the droplet size from few micrometers for the whiskers to the whole SiC wafer size. A promising attempt in this way was already made by A. Leycuras in a specially design reactor [2].

Experiments were carried out in a conventional vertical cold wall CVD reactor working at atmospheric pressure with SiH_4 and C_3H_8 as reactants and H_2 or Ar as vector gases. 3C-SiC epilayer grown on Si(100) and 8° off misoriented 4H-SiC (0001) crystals were used as substrates. Liquid silicon was chosen as the catalyst for the VLS mechanism. Temperatures ranged from 1500°C to 1700°C. We can separate our investigations in two configurations : 1) pieces of Si wafers as Si source were placed on top of the SiC seeds, and only propane was used as reactant; 2) CVD like conditions were used with a high excess of silane compared to propane (C/Si<1).

In the first configuration, a single and big droplet (few mm diameter and height) formed whereas a set of small droplets (several tens of μm diameter and height) formed on the entire surface in the second configuration. The size of the liquid droplet plays an important role on the VLS mechanism. Indeed, if the droplet is too big, it cannot be assumed as isothermal. This is the case in the first configuration where the VL interface should be enough cooler than the LS interface so that the liquid can dissolve less carbon at its free surface than at the LS interface. So the thermal gradient inside the droplet is opposed to the carbon activity gradient required for crystal growth at the SiC surface. However, due to the propane flux inside the chamber, a forced supersaturation regime is set inside the droplet giving rise to effective growth at the SiC surface. It was found that the growth rate increases and the morphology worsen from the center to the edge of the droplet. With the second configuration (several small droplets), the growth rate is homogeneous on the whole surface even if the morphology shows a more step-bunched structure under the droplets than outside. Proof will be given that a VLS mechanism occurred with this second configuration and uniform growth rates up to 35 μm/h at 1600°C were demonstrated.

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Hetero-epitaxial growth and characteristics of 3C-SiC on large-diameter Si(001) substrate

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A novel technique that eliminates planar defects in 3C-SiC hetero-epitaxial layer on Si(001) substrate was developed. Planar defects generated at an interface between 3C-SiC and Si substrate can be classified into two types: anti-phase boundaries (APBs) and twin boundaries (TBs). Although it is well known that step flow epitaxy of 3C-SiC on a slightly misoriented Si(001) substrate in the [110] direction (off-Si) result in elimination of APBs, TBs hardly be eliminated. This is because TBs are arranged in parallel with only (111) plane, with reduced possibility of elimination through combination with countered TBs with increasing 3C-SiC thickness. Therefore, TBs must be arranged in parallel, not only with the (111) plane, but with the $(\bar{1}11)$ plane equaling statistical ratio, to realize effective TB elimination at the intersection of two TBs. To satisfy above condition, Si(001) surface with countered slopes oriented in the [110] and $[\bar{1}10]$ directions (undulant-Si) was thought to be an effective substrate for 3C-SiC epitaxial growth.

To confirm above effects of the undulant-Si substrate, the entire surface of 6 inches Si(001) substrate was scraped by diamond slurry toward the $[\bar{1}10]$ direction to form continuous undulations, the ridges of which were arranged along the $[\bar{1}10]$ direction. Then the 3C-SiC layer was grown on undulant-Si substrate using 50 sccm of SiH_2Cl_2 as a Si source and 10 sccm of C_2H_2 as a C source, with 100 sccm of H_2 as a carrier gas at 1350 ° C. An epitaxial 3C-SiC layer of about 200μm in thickness was obtained on the undulant-Si substrate via five hours growth process.

3C-SiC epitaxial layer grown on undulant-Si exhibited a mirror-like surface even after etching by molten KOH unlike that case on off-Si. It appears that the undulant-Si eliminated with remarkable success not only APBs, but TBs, through the following mechanism. At first, the APBs generated at the initial stage of 3C-SiC growth were eliminated at each slope on undulant-Si by the same mechanism found on the off-Si. Although TBs remained in the 3C-SiC layer even after all

APBs had been eliminated, these were arranged in parallel along the (111) plane or the ($\bar{1}\bar{1}1$) plane, forming countered steps, as shown in Fig.1a). Thus, TB density, that is density of steps, on the surface of 3C-SiC grown on undulant-Si would decrease with increasing 3C-SiC thickness, through the combination of TBs which countered, as shown in Fig.1 b) and c). The most significant aspect of 3C-SiC growth on an undulant-Si substrate is that the vanishing probability of ($\bar{1}\bar{1}1$) paralleled TBs was quite similar to that of (111) paralleled TBs.

The crystallinity and electric properties of 3C-SiC grown on undulant-Si will be discussed at the conference using results of XTEM observation, x-ray diffraction, RBS, and Hall effect.

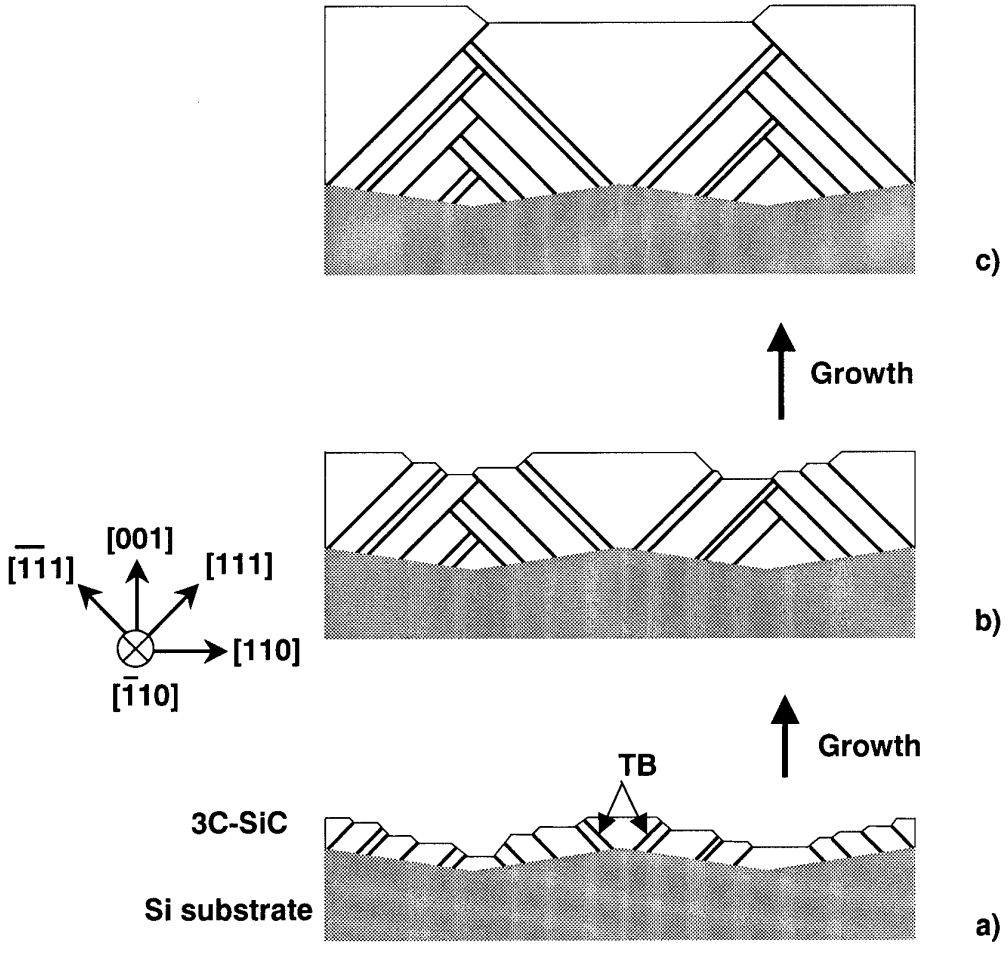


Fig.1 Vanishing model of TBs in 3C-SiC layer on undulant-Si: The ($\bar{1}$10) cross-sectional structure of 3C-SiC changes from a) to b) and c) as 3C-SiC growth progresses.

Homoepitaxial "Web Growth" of SiC to Terminate C-Axis Screw Dislocations and Enlarge Step-Free Surfaces

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Abstract

Homoepitaxial CVD growth of thin lateral cantilevers emanating from the edges of mesa patterns that were dry-etched into on-axis commercial 4H-SiC substrates prior to growth is reported. Cantilevers on the order of a micrometer thick extending tens of micrometers from the edge of a mesa have been grown. The termination of vertically propagating screw dislocations, including a micropipe, that are overgrown by the cantilevers has been demonstrated, in large part because the crystal structure of the cantilevers is established laterally from the mesa sidewalls. The cantilevers form in epitaxial growth conditions where the two-dimensional terrace nucleation rate is close enough to zero that device-size mesa top surfaces (as large as 0.4 x 0.4 mm observed to date) become entirely step free as previously described [1]. After stepflow growth removes almost all atomic steps from the top surface of a mesa, additional adatoms collected by the large stepfree surface diffuse to the mesa sidewall to find steps where they rapidly incorporate into the crystal near the top of the mesa sidewall. The lateral propagation of the step-free cantilevered surface is significantly affected by pregrowth mesa shape and orientation, with the highest lateral expansion rates being observed at the inside concave corners of V-shaped pre-growth mesas. The cantilevers exhibit well-known hexagonal crystal growth facets, with fastest growth observed along the $<11\bar{2}0>$ direction. Complete spanning of the interiors of V's and other mesa shapes with concave corners by "webbed cantilevers" is accomplished. Webbed cantilever surfaces up to approximately 0.4 x 0.7 mm have been realized to date, representing a 4-fold increase from the pre-growth mesa area. X-ray topography and AFM analysis of webbed regions formed over screw dislocations indicate that c-axis propagation of these defects is terminated. With very few exceptions, cantilevers are not observed on mesas that contain screw dislocations prior to epitaxial growth, as the screw dislocations readily provide steps for incorporating top surface adatoms into the crystal resulting in vertical growth of the mesa top surface [1]. Another factor observed to limit lateral cantilever growth is unintentional two-dimensional nucleation and growth of 3C-SiC that takes place on some mesa/cantilever surfaces.

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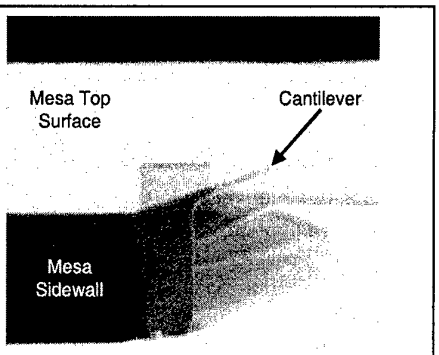


Fig. 1: SEM of thin lateral 4H-SiC cantilever emanating from the top of a flat mesa.

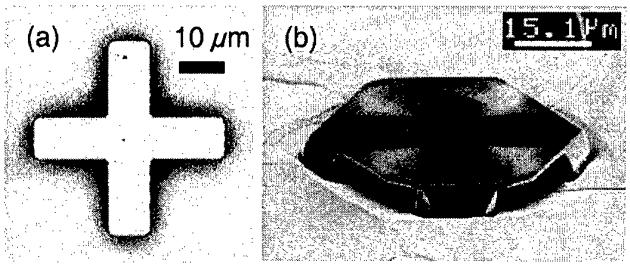


Fig. 2: (a) Pre-growth optical photo of cross-shaped mesa. **(b)** Post-growth SEM of step-free "webbing" formed by ordered merging of lateral cantilevers following 1-hour growth.

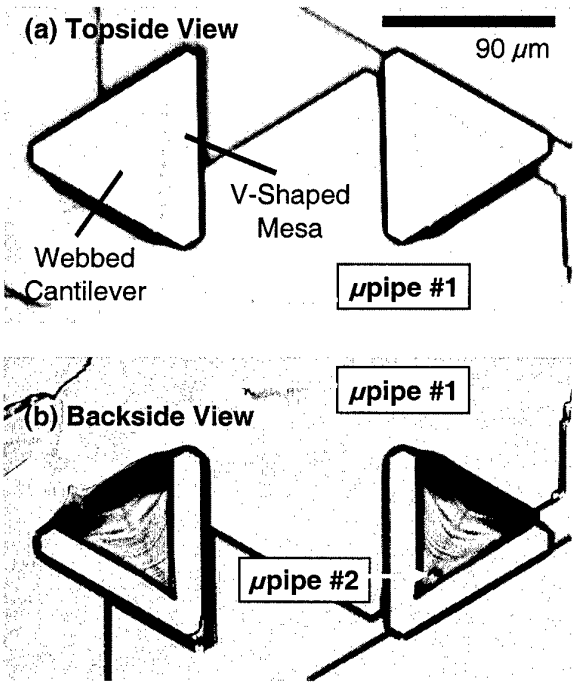


Fig. 3: (a) Top view of web growth fully spanning two V-shaped mesas following a 6-hour epitaxial growth. AFM scans of the right mesa did not detect the presence of any atomic steps, confirming that micropipe #2 did not propagate through the webbing. The presence of a few 0.25 nm steps was detected on the left mesa, indicating unintentional nucleation and growth of 3C-SiC on that particular mesa.
(b) View of the same mesas looking through the polished wafer backside, showing micropipe #2 beneath the webbing.

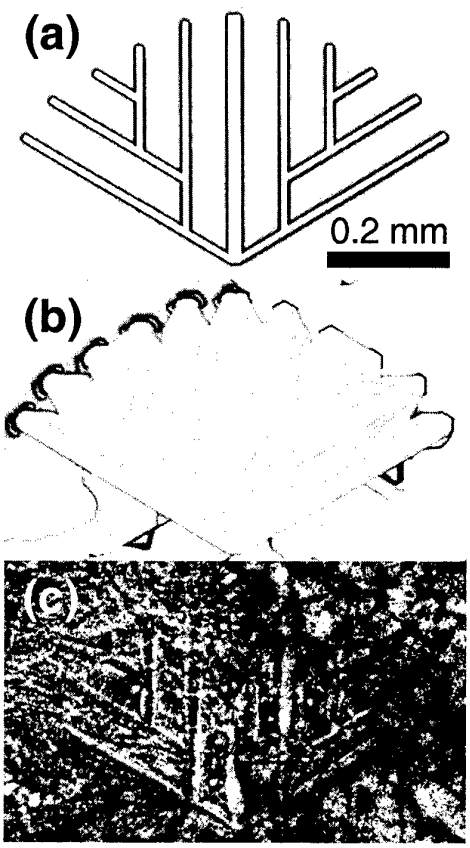


Fig. 4: (a) Pre-growth and **(b)** post-growth optical photo of large web growth test mesa. The webbing process increased the top surface area by over a factor of 4 following the 6-hour growth.
(c) X-ray back-reflection topograph used to study the defect microstructure around the post-growth mesa.

3C-SiC(100) Homoepitaxial Growth by Chemical Vapor Deposition and Schottky Barrier Junction Characteristics

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We have investigated 3C-SiC heteroepitaxial growth on Si using chemical vapor deposition method (CVD) and found out that atomically flat surfaces without protrusions and antiphase domain (APD) are obtained by using low pressure CVD (LPCVD) [1, 2]. And we have showed excellent Schottky barrier junction (SBJ) properties using the LPCVD epilayers compared with those reported for 3C-SiC on Si so far. However, the characteristics of the SBJ, like breakdown voltage and reverse leakage current, were not sufficient for practical use [3]. These poor characteristics have been attributed to the low crystallinity of the epilayers, namely the epilayers contain many defects such as stacking faults and twins. In the case of the growth of 3C-SiC on Si substrates, the growth temperature is limited by the melting point of Si, i.e., 1420 ℃. Therefore, it is difficult to improve the crystallinity by increasing growth temperatures. Recently, thick 3C-SiC free standing crystals, around 200 μm in thickness, were made by removing Si substrates from thick 3C-SiC heteroepitaxial layers [4]. In this report, we have used 3C-SiC free standing crystals as substrates and have carried out the 3C-SiC homoepitaxial growth. We have examined their crystallinity by studying the characteristics of the Schottky barrier junction fabricated on them.

The homoepitaxial growth of 3C-SiC were carried out by use of low pressure hot-wall reactor CVD system. The 3C-SiC substrates with on-axis (100) surfaces, n type with carrier concentrations of 1×10^{17} cm^{-3} and the thickness of about 200 μm were supplied by HOYA corporation [5]. We have grown SiC epilayers, 10 μm in thickness, with various growth conditions, *i.e.*, pressures between 90 and 300 Torr, Si/C ratio between 0.33 and 1 and growth temperatures between 1500 and 1600 ℃. The epilayers was examined with a Nomarski differential interference contrast microscopy (NDIC), an atomic force microscope (AFM) and X-ray diffraction (XRD). Schottky diodes were fabricated on these epilayers. Details of the process have been described elsewhere [3]. Ni films were deposited as Schottky electrodes and Al ohmic electrodes were formed on back side of the substrates. The diameter of the Schottky electrodes was 0.1 mm.

Figure 1 shows a NDIC image of the surfaces of homo-epilayers. Smooth surfaces on which any features could not be observed, as shown in Fig. 1, were obtained at the optimized conditions. Figure 2 shows an AFM image of a sample with smooth surface. The figure shows that the step bunching occurs. The width of the terrace is about 5 μm and the step height is 1-3 nm. The average roughness (16 μm square) was 0.85 nm, which is one order of magnitude smaller than those of hetero-epilayers reported. The full width at half maximum (FWHM) of the X-ray rocking curve for (400) peak were in the range from 163 to 484 arcsec. We could not find any relation between the value of FWHM and the growth conditions, because the variation of the FWHM values of substrates is larger than the difference of those

by the growth conditions. An example of the I-V characteristic of a Ni/n-type 3C-SiC Schottky diode is shown in Fig. 3. The figure shows the breakdown voltages and the on-resistance are 285 V and 3.35×10^{-3} Ωcm^2, respectively. The breakdown voltage and the on-resistances obtained from all samples were in the range of 90-305 V and $1.61\text{-}10.2\times10^{-3}$ Ωcm^2, respectively. We plotted on-resistance versus breakdown voltage for 3C-SiC Schottky diodes as well as the theoretical values of 3C-SiC and Si Schottky diodes in Fig. 4. These results indicate that the properties of the SBJs fabricated using homoepitaxially grown 3C-SiC exceed the theoretical limit of Si diodes, though still behind the theoretical limit of 3C-SiC.

References

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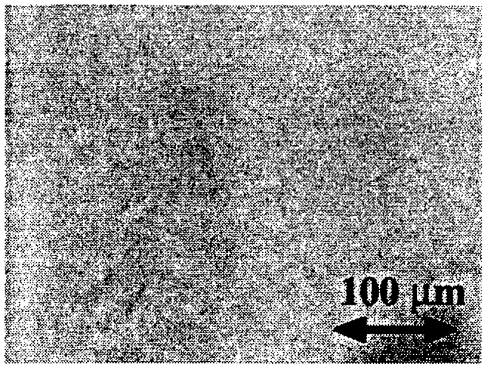


Fig.1 NDIC image of the surface.

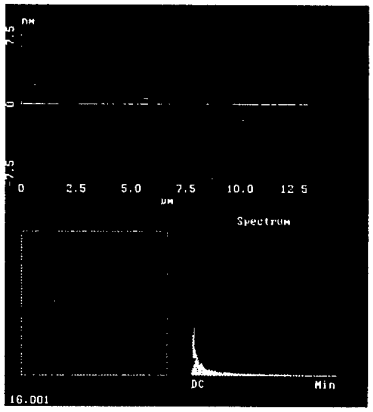


Fig. 2 AFM image of the surface.

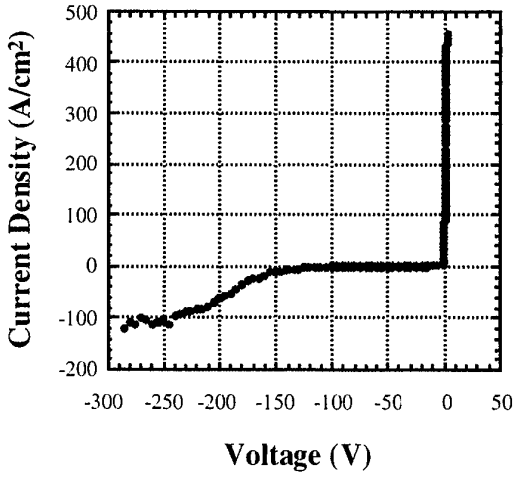


Fig. 3 I-V characterics of SBD on homoepilayer.

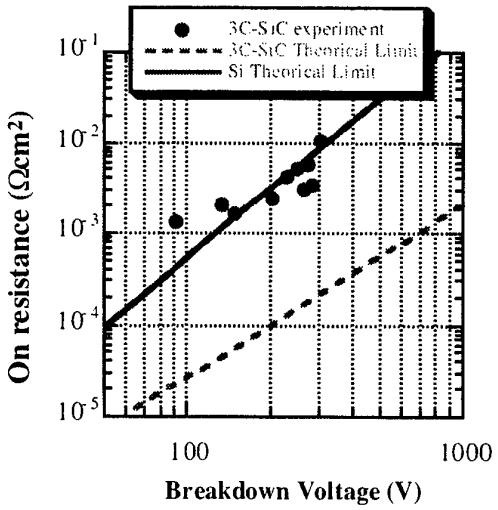


Fig. 4 On resistance versus breakdown voltage.

Void-free epitaxial growth of cubic SiC crystallites during CO heat treatment of oxidized silicon.

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Cubic SiC can be grown epitaxially on single-crystalline silicon substrates by, e.g., chemical vapor deposition (CVD)[1-6]. The first step of the 3C-SiC growth process on Si is the carbonization of the silicon surface to produce seeds for epitaxial growth [7]. Unfortunately the formation of regular shaped voids at the SiC/Si interface below the seeds greatly hinders the development of this technique. It has been shown that C^+ implantation at high temperature (1000-1100 °C) through a protective oxide layer produces epitaxially oriented SiC seeds at the interface, with better quality than those formed in the first stage of the CVD process [2]. The improved quality was explained by the slow growth rate of SiC due to the low carbon ion density. The driving force for diffusion was attributed to the presence of dangling and strained bonds, facilitating the formation of SiC at the interface. Indeed, SiC islands were also formed within the SiO_2 layer with inhomogeneous distribution.

In the present paper we show that annealing a SiO_2/Si structure in CO containing gas without disturbing the SiO_2 layer leads to the diffusion of carbon through the oxide and the segregation of carbon in form of SiC crystallites solely at the interface. These crystals are in epitaxial orientation with the Si substrate and free of voids at their interface. Thereby, the annealing in CO constitutes a new simple process [8] to produce high quality epitaxial SiC seeds on Si.

Experiments performed before the submission of this abstract resulted in square shaped SiC crystallites growing into the Si (001) surface with sizes up to 100 x 100 x 30 nm. The density is 2×10^9 cm^{-2} (20 % coverage) and the size distribution is uniform. According to TEM, about 90 % of the crystallites are in perfect epitaxial orientation with the substrate. Grain boundary – free coalescence of crystallites were also observed. The dangling bond density introduced to the interface by the SiC crystallites has been measured by the C-V method in view of possible electrluminescent applications.

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Heteroepitaxy of cubic-SiC (3C-SiC) on Si(100) using porous Si as a compliant seed crystal

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The desirable integration of established and cost effective Si technology with SiC to generate a new family of bandgap engineered, high frequency, medium to high power, high temperature and radiation hard devices has been constantly challenged by the large lattice mismatch between Si and SiC (~ 20%), which has led to difficulties in achieving device-quality materials and interfaces. In this work, a new approach has been implemented to minimize the effects of interfacial strain on the grown layers. Porous Si was used as a compliant single-crystalline elastic seed for growth of 3C-SiC. The growth was then conducted using two methods. In the first, a single gas-source non-toxic trimethylsilane [$(CH_3)_3SiH$] was used for growth of epitaxial 3C-SiC. The method is environmentally friendly and is economical due to the low cost of trimethylsilane (TMS) and Si wafers. In the second, conversion of the porous Si layer into SiC was attempted using high-temperature annealing in methane. However, the latter process did not lead to total conversion of the porous layer. The porous-Si layers were made using anodization of p-type Si(100) wafers in a mixture of hydrofluoric acid (HF) and ethanol in which the anodization current, time, and HF concentration were used to control the porosity and thickness of the porous layer. SiC was grown in a UHV system that was converted into a low-pressure CVD reactor and was fitted with a resistive heating stage capable of heating the samples up to 1200 ^{o}C. The formation of stoichiometric SiC was confirmed by secondary ion mass-spectrometry (SIMS) and Fourier transform infrared spectroscopy (FTIR) while the crystal structure was examined by transmission electron microscopy (TEM) and X-ray diffraction. FTIR showed a strong peak at 800 cm^{-1}, which corresponds to the Si-C vibrational mode. Figure 1 shows a comparison between four samples demonstrating the effects of growth conditions. The intensity of the peak at 800 cm^{-1} is mainly related to the thickness of the sample while the multiple lines within the peak are an artifact of the software used by the BioRad FTIR unit. Sample 28b was grown using conversion in methane atmosphere. The

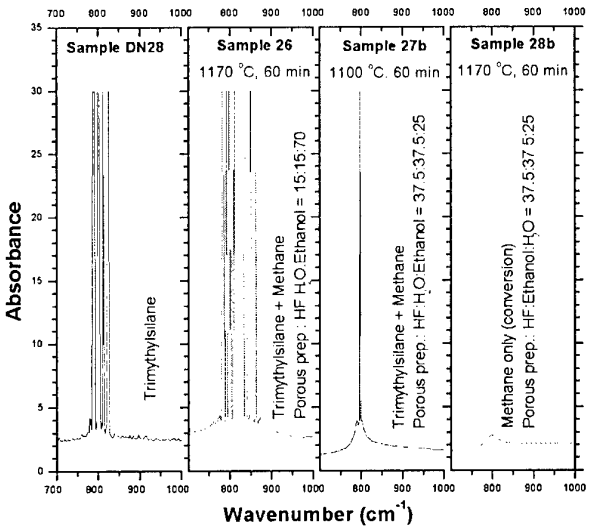


Figure 1. FTIR spectroscopy showing the dependence on growth conditions (see text).

Si-C signal is very small compared to sample 26, which was grown using a mixture of TMS and methane at the same growth temperature and for the same time. This is understandable since the C-H bonding energy in methane is larger than Si-C in TMS resulting in a higher rate of TMS dissociation at a given temperature. In addition, TMS provides both Si and C for growth, while conversion using methane is limited by diffusion of C through the newly formed SiC. The effect of growth temperature is demonstrated in the difference between sample 26 and 27b. Growth using only TMS is essentially similar to growth from a mixture of methane and TMS as shown in the example of sample DN28. Atomic force microscopy (AFM) showed the formation of rough surfaces for thin SiC layers and large flat terraces for thick SiC layers. SIMS analysis showed that the layers were stoichiometric TEM selected area diffraction indicates the formation of fully relaxed single crystalline 3C-SiC(100) on Si(100) wafers (see Figure 2). In some samples, weak spotty rings also appeared in the diffraction pattern indicating the presence of small domains of other orientations. These domains are mainly due to faulty growth within the porous layer resulting from incomplete desorption of oxide from the porous Si layer prior to deposition of SiC. Large area X-ray diffraction shows the domination of SiC(100) peaks but also suggests the presence of a minute amount of SiC(111) and SiC(022).

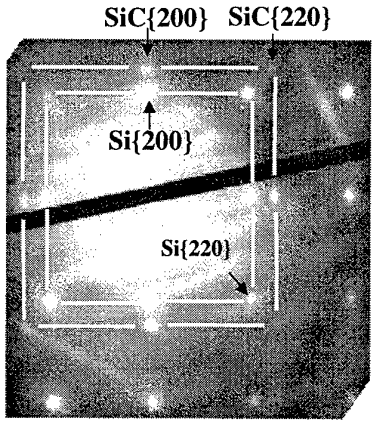


Figure 2.
Selected area diffraction from single crystalline 3C-SiC grown on porous Si substrate. The diffraction pattern represents fully relaxed Si(100) and SiC(100).

The heterojunction Si/SiC was further examined by fabricating heterojunction diodes using Ni as the metal contact to SiC and Al to the p-type Si substrate. Figure 3 shows typical I-V curve obtained from such a device. The insert shows the details of I-V curve near the origin. A record breakdown voltage of ~375V was obtained, which is, up to our knowledge, more than three times higher the highest recorded value in the literature. A high leakage current was associated with most of the heterojunction diodes. This is most likely due to leakage and tunneling through the porous interface.

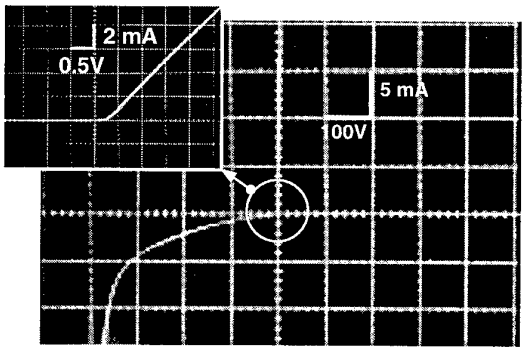


Figure 3. I-V behavior of 3C-SiC/Si(100) heterojunction diode showing a breakdown voltage of ~ 375 V, the highest reported value so far. The insert details the I-V curve near the (0,0) point

Acknowledgment: The authors gratefully acknowledge the financial support of the Office of Navel Research (ONR) administered by Dr. Colin Wood and the Defense Advanced Research Project Agency (DARPA) administered by Dr. Daniel Radack. Support from the U.S. Department of Energy (grant DEFG02-96-ER45439) is also appreciated. Special thanks to Mr. John Hudak for an outstanding technical support.

[redacted]

ThB1 Surfaces

Atomic Scale Passivation of SiC Surfaces

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Surface passivation is a central issue in successful SiC device applications. It could be achieved by oxidation but also by hydrogenation. In this presentation, I will discuss some important points of latest studies in SiC passivation such as the i) role of atomic defects, ii) oxygen/hydrogen atomic adsorption sites, iii) propagation of the oxidation reaction and H or O surface migration, iv) abrupt insulator/SiC interface formation and new Si phase on hexagonal SiC and v) role of the polytype and of surface reconstruction, composition and temperature.

The initial oxidation of hexagonal (6H,4H) SiC surfaces is investigated by combining three different techniques: core level photoemission spectroscopy (CLPS) using 3rd generation synchrotron radiation source, atom-resolved scanning tunneling microscopy (STM) and infrared absorption spectroscopy (IRAS using ^{16}O and ^{18}O) [1]. High quality clean Si-rich 6H/4H-SiC(0001) 3x3 surfaces are prepared having a very low atomic defect density (better than 2%). In strong contrast to the cases of silicon and 3C-SiC surfaces [2], initial defects (bright and dark) are not adsorption sites for oxygen atoms but result from electronic effects. Oxygen atoms interaction takes place away from the trimer-ad atom (Tri-Ad) well below the surface with oxide product formation already at extremely low oxygen exposures and with oxygen atoms in bridge bonded positions [1]. Also, again in strong contrast to Si, this initial oxidation is likely to relax the highly strained SiC surface [1]. Abrupt SiO_2/SiC interfaces could be obtained at 500°C when the oxidation is performed on a pre-deposited Si overlayer on the SiC surface [3]. Most interestingly, this Si overlayer is found to have a novel and unexpected cubic 4x3 array growing on a hexagonal SiC surface and to be highly sensitive to oxygen [4].

Molecular H_2 interaction with 3C-SiC(100) 3x2 and c(4x2) surfaces and with Si atomic lines is investigated by atom-resolved STM and valence band photoemission [5]. While the 3x2 surface reconstruction remains totally inert, the c(4x2) is highly reactive to H_2 with sticking probabilities up to 8 orders of magnitude higher than for Si(100)2x1. H_2 is initially dissociated at up-dimer adsorption sites influencing the two neighbor down-dimers. At higher exposures, H induces a 2x1 surface transformation. Interestingly, investigating H atom surface migration, we observe a strong anisotropy with H atom hoping along the dimer rows of the c(4x2) surface (AUDD) and not perpendicularly to the dimer rows. The very high reactivity difference between 3x2 and c(4x2) allows non-reacted Si atomic lines formation on a hydrogenated surface [5].

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Work sponsored in part by THALÈS (Thomson-CSF), Délégation Générale à l'Armement (DGA), Institut Français de Taipei (IFT) and National Science Council (NSC, Taipei, Taiwan).

OXIDATION STATES PRESENT ON SiC (0001) AFTER OXYGEN EXPOSURES

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The presence of one sub-oxide (Si^{+1}) besides the Si^{+4} from SiO_2 was recently revealed [1] after in situ oxygen exposures in the 10^6 L (1 Langmuir = 10^{-6} torr sec.) range on the $\sqrt{3}x\sqrt{3}$ R30° reconstructed surface of 4H-SiC(0001) crystals. The crystals were kept at elevated temperature, from 650 to 950° C, during the oxygen exposures. In studies of initial oxidation of 3x3 reconstructed surfaces of SiC (0001) the presence of three sub-oxides (Si^{+1}, Si^{+2}, and Si^{+3}) besides the Si^{+4} from SiO_2 were recently reported [2,3]. These differences motivated us to make a detailed study of the effects induced on the $\sqrt{3}x\sqrt{3}$ R30° surface of SiC (0001) after oxygen exposures from the 1 L range up to the 10^6 L range. Only two oxidation states, Si^{+1} and Si^{+4}, can be observed as discussed and illustrated below.

The Si 2p spectrum recorded from the clean $\sqrt{3}x\sqrt{3}$ R30° surface and after an oxygen exposure of 1000 L is shown in Fig. 1a. Also shown in the figure is the difference spectrum constructed between the exposed and the clean surface. The SiO_2 component is clearly seen in the spectrum recorded from the exposed surface and exhibits an energy shift of ca. 2.2 eV. That an additional Si^{+1} component is present on the exposed surface is clearly demonstrated by the difference spectrum although it overlaps quite strongly with the bulk SiC component. In Fig. 1b a peak fit procedure has been used to extract the Si 2p components involved and to determine their energy separations. The shift extracted for the Si^{+1} component is ca. 0.5 eV. Si 2p spectra recorded after different oxygen exposures are shown in Fig. 2. From these, one can directly see how the two shifted components develop with the amount of oxygen exposure. The vertical dashed lines in the figure are guides to the eye to point out the energy locations of the Si^{+1} and Si^{+4} components.

The results presented in Figs. 1 and 2 show that only two oxidation states, exhibiting energy shifts of ca 2.2 and 0.5 eV, do develop on the SiC (0001) surface after oxygen exposures at an elevated temperature. Similar results concerning energy shift and number of shifted components were however also obtained when keeping the SiC crystal at room temperature or at liquid nitrogen temperature. The same energy shift for the Si^{+4} component was also determined on samples dry oxidized ex situ in a furnace and studied using a higher photon energy [4]. Our results are in contrast to the recently reported findings on the 3x3 reconstruction of SiC (0001) where all four oxidation states were indicated. That four oxidation states do appear on oxidized surfaces of Si is well known [5] and the energy shifts for these oxidation states have been accurately determined. The 3x3 reconstruction is built up of three Si layers [3] on top of the first Si-C bi-layer so that initial oxidation of this surface more resembles that of Si surfaces is therefore not surprising. The above results will be presented and discussed.

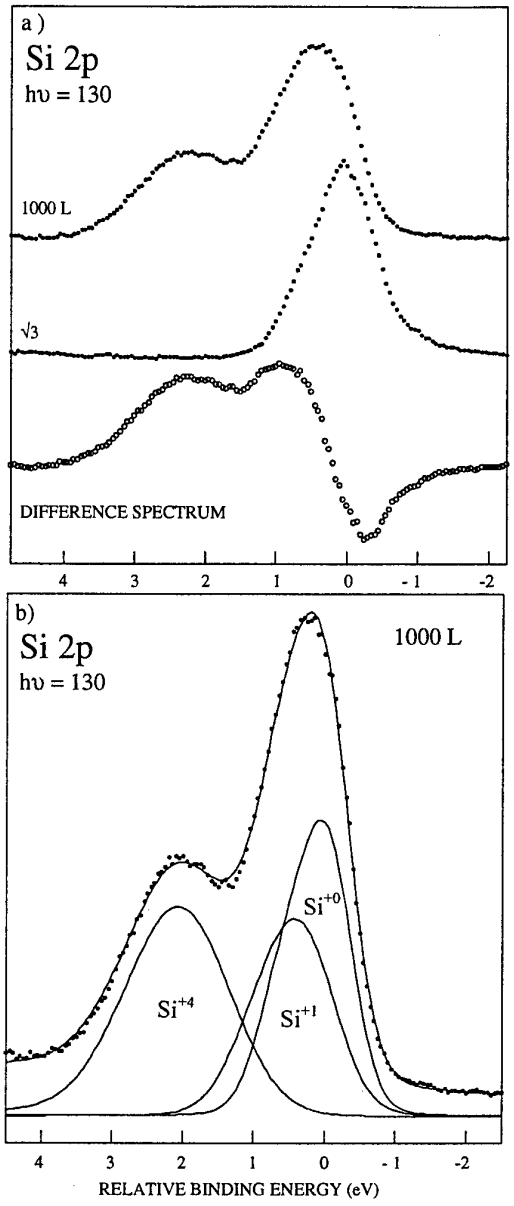


Fig.1. a) Si 2p spectra recorded at $h\upsilon = 130$ eV from the clean $\sqrt{3}x\sqrt{3}$ R30° reconstructed 4H-SiC(0001) surface and after oxidation to a total oxygen exposure of 1000 L at a substrate temperature of 800°C. The difference spectrum between after and before oxidation is shown by the bottom curve. b) The results obtained when applying a curve fitting procedure to the 1000 L spectrum in Fig. 1a showing the two oxidation states present.

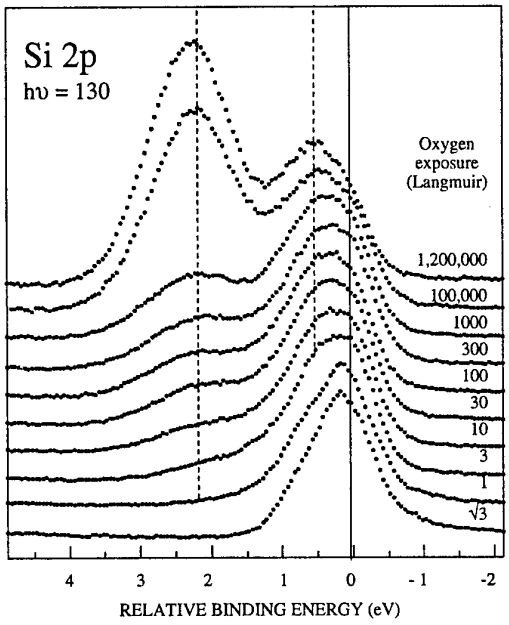


Fig.2. Si2p spectrum recorded after different oxygen exposures onto 4H-SiC at elevated temperature.

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A high resolution photoemission study of hydrogen terminated 6H-SiC surfaces

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We report on highly resolved photoemission measurements of hydrogenated 6H-SiC(0001) and $(000\bar{1})$ surfaces. Si2p and C1s core level spectra as well as valence band spectra were recorded at the synchrotron facility BESSY II with an overall energy resolution of about 250meV.

Before hydrogenation the samples (n-type 6H-SiC from CREE, Inc. and SiCrystal) were treated using a four step wet-chemical cleaning procedure. [1] The hydrogenation was carried out by heating the crystals in $1x10^5$ Pa of ultra-pure hydrogen (8.0) at temperatures of around 1000 °C. [2] In order to avoid contamination, the so prepared samples were transported under UHV conditions ($p < 1x10^{-6}$ Pa) to the synchrotron facility BESSY II.

The Si2p and C1s core levels of the Si-terminated 6H-SiC(0001) surface after thermal hydrogen treatment are depicted in Figs. 1(a) and 1(b) for surface sensitive (hν=170eV) and bulk sensitive (hν=350eV) measurements. In the Si2p core level spectrum no chemically shifted component is observable. This is not surprising, because the chemical shift of the Si 2p core level expected on account of the partially ionic Si-H bond is estimated to be 50 meV based on the Pauling electronegativities of the three elements hydrogen, silicon, and carbon. This is too small to be resolved by our present resolution. The C1s core level shows an extremely weak chemically shifted component at 2.1 eV higher binding energy which is ascribed to weakly bonded hydrocarbons C_xH_y. An estimate of the hydrocarbon layer thickness yields (0.3±0.1)Å when an effective sampling depth of λ_{eff}=4 Å is applied for the chosen geometry. The C_xH_y contamination originates from the eight hours transport to the synchrotron facility BESSY II. The main C1s component and the single Si2p line are attributed to stoichiometric SiC.

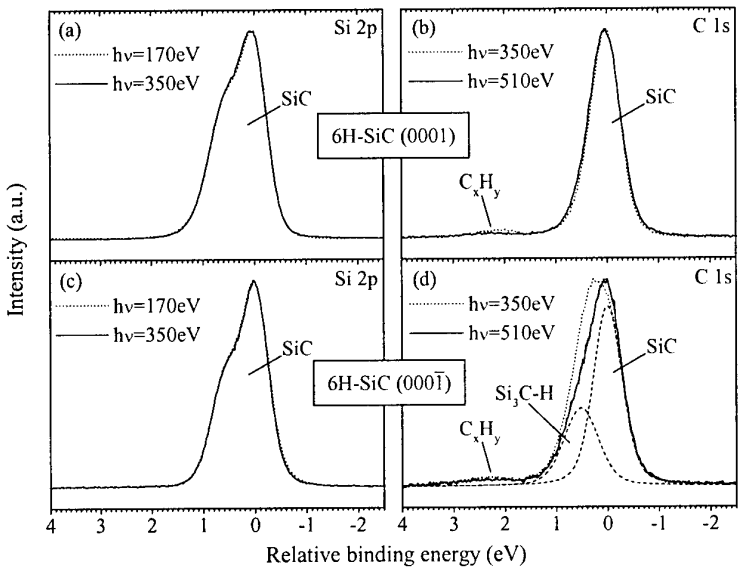


Fig. 1) Si2p and C1s core level spectra of H-terminated SiC(0001) ((a) and (b)) and H-terminated 6H-SiC$(000\bar{1})$ ((c) and (d)). The solid lines correspond to bulk sensitive, the dotted lines to surface sensitive measurements. The dashed lines in spectrum (d) show a deconvolution in two Voigt lines for the bulk sensitive measurement (hν=510eV).

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In Fig. 1(c) and (d) the corresponding Si2p and C1s core level spectra of a C-terminated and hydrogenated 6H-SiC($000\bar{1}$) surface are shown. Again, the Si2p core level does not show chemically shifted surface components. On the other hand, in contrast to the Si-face, the C1s core level exhibits a chemically shifted surface component with 0.5 eV higher binding energy compared to the bulk component. Since hydrogenated surfaces are unreconstructed and no atomic species other than silicon and carbon are detected by XPS the shifted component is ascribed to C-H bonds in a Si_3C-H configuration. This assignment agrees well with the qualitative argument that hydrogen with a larger Pauling electronegativity than silicon allows a smaller charge transfer towards carbon than silicon. This results in a higher binding energy of carbon in a Si_3C-H environment in comparison to a Si_3C-Si environment. The chemically shifted component at 2.1 eV higher binding energy relative to the bulk line is again due to hydrocarbon adsorbates.

Normal emission valence band spectra of hydrogenated SiC(0001) and SiC($000\bar{1}$) are depicted in Fig. 2. Spectrum (a) was taken on a SiC(0001) surface directly after hydrogenation. Spectra (b) and (c) were recorded on hydrogenated SiC(0001) and SiC($000\bar{1}$), respectively, after the samples had been exposed to a high dose of synchrotron radiation at hν=170 eV. A (1×1) LEED pattern was observed for all three surfaces. We emphasize the dangling bond state D at 0.7 eV above the valence band maximum (VBM) and 1.7 eV below E_F, which is observed for both terminations after irradiation. The formation of the dangling bond state D is due to radiation induced desorption of hydrogen. Since the dangling bond state is energetically located in the fundamental gap of 6H-SiC below E_F the bare, unreconstructed silicon carbide surface is semi-conducting. This observation is in contrast to theoretical calculations within the one-particle picture which predict metallic behaviour of SiC(0001) and SiC($000\bar{1}$) surfaces. [3]

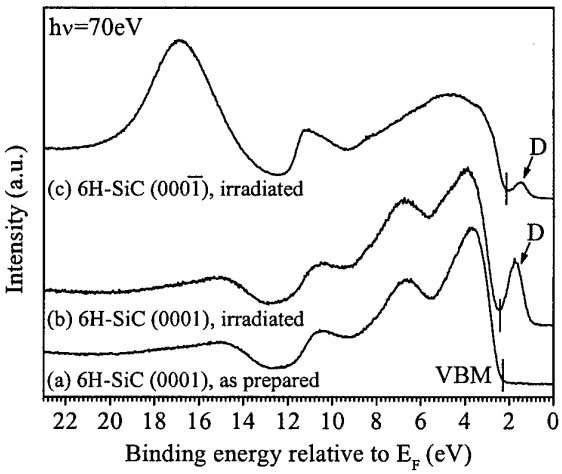


Fig. 2) Valence band spectra of H-terminated SiC(0001) and SiC($000\bar{1}$) after different preparation steps. VBM denotes the valence band maxima and D the emission maxima due to dangling bonds.

Similar dangling bond states were observed earlier for 6H-SiC($000\bar{1}$) with silicate adlayer reconstruction [4] and for SiC(0001) with ($\sqrt{3}$x$\sqrt{3}$)R30° reconstruction with a Si-adatom in T4 position. [5] In both cases the dangling bond state lies in the gap below E_F and the surfaces are semiconducting. This was explained using a Mott-Hubbard description for the dangling bond state which might also be an adequate approach for the clean hexagonal SiC surface.

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In-situ analysis of thermal oxidation on H-terminated 4H-SiC surfaces

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SiC power MOSFET is the promising for use in high-voltage and low-loss devices. However, details of the structure near the SiO_2/SiC interface formed by thermal oxidation are not fully understood. To date, many studies have been performed on SiC surface and SiO_2/SiC interface. Recently N. Sieber et. al. reported that they successfully removed the contaminants are form SiC surface by H_2 annealing and that hydrogenated SiC(0001) and SiC(000-1) surfaces are electronically and chemically passivated with the surface Fermi level position at the bulk position [1]. In this study, the initial oxidation process on a H-terminated 4H-SiC surface achieved by annealing in H_2 was investigated using in-situ Fourier-transformed infrared reflection absorption spectroscopy (RAS), Auger electron spectroscopy (AES), and low energy electron diffraction (LEED), equipped in UHV chambers.

All experiments were carried out in the UHV chamber. Therefore, we can analyze the oxide/SiC interface without effect of contamination except for the prior to the initial loading after chemical cleaning. Commercially available n-type 4H-SiC(0001) Si-face 8° off-axis wafers purchased from CREE Research Inc. were used in the experiments. H_2 annealing of the SiC surface was carried out for 1 hour at 1000℃ in 750 Torr of pure hydrogen (the dew point was -83℃). The thermal dry oxidation was performed by heating a H-terminated SiC surface at 400℃ in 750 Torr of dry oxygen (the dew point was -108℃) in same UHV chamber. An infrared heating system was employed for the heating samples in the UHV chamber.

AES spectrum for HF treated surface is shown in Fig.1 (a) and that for surface annealed in H_2 at 1000℃ is shown in Fig.1 (b). By annealing in H_2, Auger peak to peak height ratio of C(KLL) to Si(LVV), and that of O(KLL) to Si(LVV) decreased. It is indicated that hydrocarbon and oxide remained on SiC surface were reduced by annealing in H_2, although they were remained after HF treatment. Fig. 2 shows LEED pattern observed for a 4H-SiC surface immediately after H2 annealing with primary energy Ep=150 eV. The diffraction pattern corresponds to a SiC 1×1 surface structure. The spots of the LEED pattern become remarkably sharper and brighter than that for ex-situ HF-treated surface. It is suggested that SiC (1×1) ideal surface is formed by H_2 annealing. From LEED and AES results, SiC surface was cleaning by H_2 annealing. Fig. 3 shows RAS spectra of a 4H-SiC surface at Si-H stretching vibration region. Fig. 3 (a) is the spectrum for a 4H-SiC surface immediately after H_2 annealing at 1000℃. A sharp absorption band at $\sim$2130 cm^{-1} was dominantly observed.

It is implies that C_3Si-H bond is formed on a 4H-SiC surface by H_2 annealing at 1000℃. The Fig 3 (b) and (c) show the spectra that thermal oxidation was performed on H-terminated surface in O_2 ambient (750 Torr) at 400℃. The oxidation time of spectra (b) and (c) is 50 and 100 minutes, respectively. The Fig 3 (b) and (c) can be deconvoluted into three components as shown in Fig. 3. The peak frequencies were ~2130, ~2180, and ~2220 cm^{-1} . This result indicates that other bonds were formed by oxidation on the H-terminated 4H-SiC surface. It is known that the Si-H stretching frequency shifts toward a higher frequency with the increasing sum of the electron negativity of the atoms or groups bonded to the Si atom. Lucovsky [2] calculated that the stretching frequencies of various Si-H bonds, with O and C are bonded to the Si atoms, that is, ~2180 cm^{-1} for OC_2Si-H, and ~2220 cm^{-1} for O_2CSi-H. These results imply that the oxidation of the Si-C back bond occurred by heating at 400℃ in 750 Torr O_2.

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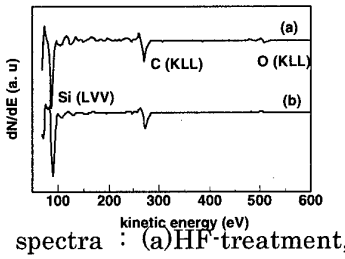


Fig. 1 AES spectra : (a)HF-treatment, (b) annealed in H_2



Fig. 2 LEED pattern for a 4H-SiC surface after annealing

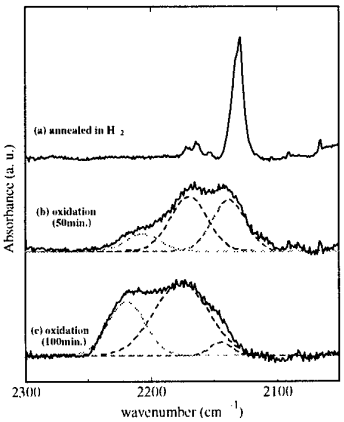


Fig. 3 FTIR-RAS spectra.
(a) annealed in H_2
(b) oxidation for 50min.
(c) oxidation for 100min.

[redacted]

ThA2 Epitaxial Growth 2

Bending of basal plane dislocations in the VPE grown 4H-SiC epitaxial layers

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The propagation of basal plane dislocations from the off-cut SiC substrate into the epilayer has been investigated by KOH etching, optical microscopy, and transmission electron microscopy (TEM). It is well known that in homo-epitaxial growth, dislocations intersecting the growth surface replicate into the overgrowth. The Burgers vector of individual dislocations remains unchanged across the interface. It is also assumed that the dislocation line direction stays the same. In the case of hexagonal SiC polytypes, this implies that screw and edge dislocations propagating along the c-axis thread through the epilayer almost perpendicular to its surface, while the basal plane dislocations should form a shallow angle with the layer surface. The results presented below indicate that this is not the case.

The samples examined in this study were 4H-SiC wafers oriented 8° from the [0001] toward the $<11\bar{2}0>$ direction with the 10 μm thick epitaxial layers grown by vapor phase epitaxy (VPE) at low pressure (~100 mbar). Epilayers were etched in molten KOH to reveal the locations where dislocations intersect the (0001) Si surface of the epilayer. After etching, the epilayer was removed by polishing and the bare substrate was etched to reveal the dislocations present in the

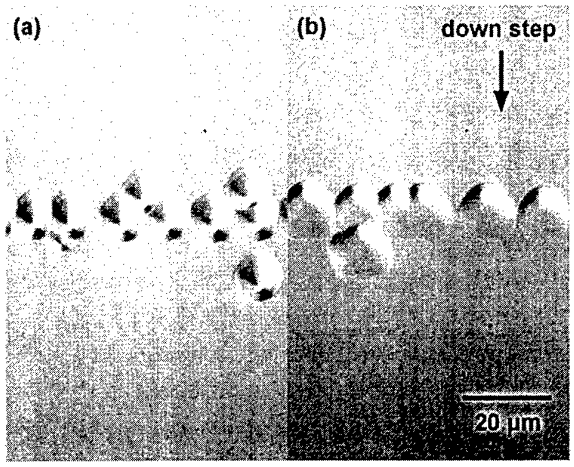


Fig. 1 Dislocation etch pits revealed by molten KOH etching of (0001) Si surfaces.
(a) On top surface of the epitaxial layer
(b) 10 μm below the epitaxial layer

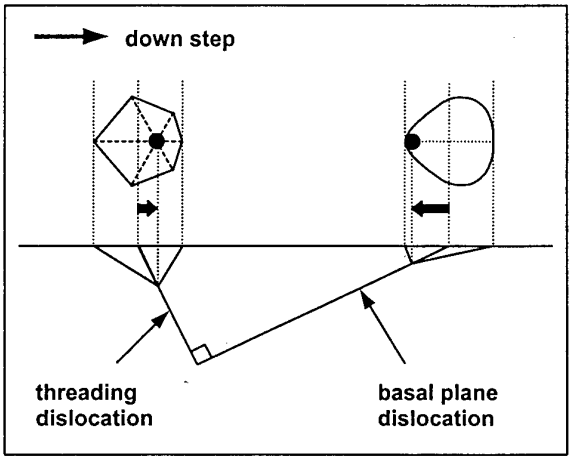


Fig. 2 Formation scheme of the two different etch pits shown in Fig. 1. Note that the point bottoms marked with large solid circles are shifted in the opposite directions.

substrate prior to growth of the epilayer. The shape and distribution of etch pits were analyzed by optical microscopy. Specifically we have analyzed etch pits in the slip bands of basal plane dislocations. In the substrate, the etch pits making up the slip bands have an oval shape characteristic of basal plane dislocations. On top of the epilayer, the same pits have a form of hexagons indicating that the dislocation line is almost normal to the surface (Fig. 1 and 2). This is a direct experimental evidence of a conversion of basal plane dislocations into a threading edge dislocation. This behavior was confirmed by conventional TEM (Fig. 3) and by gradual polishing of the wafer/epilayer structure and etching in molten KOH. The conversion was interpreted as a result of the image force in epilayers grown in the step flow mode. It is argued that this mechanism can cause the increase of the threading edge dislocation density in PVT growth and can lead to an apparent improvement in x-ray reflection width of epilayer.

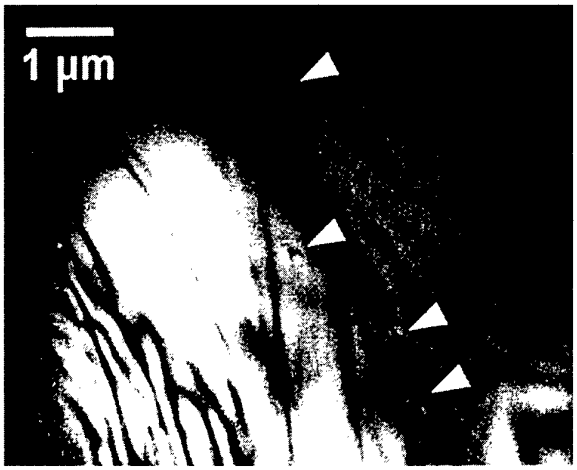


Fig. 3 Plan-view conventional TEM micrograph showing four threading dislocations corresponding to a basal plane slip band in a VPE layer.

Aluminum Doping of Epitaxial Silicon Carbide grown by Hot-Wall CVD, Effect of Process Parameters

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Aluminum is the most common p-type dopant in SiC. The incorporation of aluminum in epitaxial SiC grown by hot-wall CVD is strongly connected to the chosen growth parameters. Common process parameters such as C/Si ratio, trimethylaluminum (TMA) flow, pressure, temperature and growth rate influence the aluminum incorporation.

A detailed study of the aluminum incorporation in 4H- and 6H-SiC epitaxially grown layers for both Si- and C-faces has been performed including both thermodynamical calculations and growth runs. The calculations have been made on a H_2-SiH_4-C_3H_8-$Al(CH_3)_3$ system using a commercially available code CFD-ACE+ and typical growth conditions where consideration has been taken to whether solid phases are allowed to be formed or not. We will present results from growth runs and calculations on aluminum incorporation and its dependence on the process parameters as mentioned above. All materials have been characterized with second ion mass spectrometry, SIMS.

The incorporation of aluminum is strongly connected to the creation of available lattice sites. The calculations have shown that the highest concentration of aluminum is found in the Al, AlH, AlH_2, AlH_3 and $AlCH_3$ species which indicates that we are not dependent on dissociation of larger molecules, as in the case of nitrogen incorporation [1]. In the case of aluminum incorporation, the bonding at the surface of the aluminum atoms is more important. Aluminum, with three available bonds, will bond strongly to the three different carbon atoms at the Si-face, assuming ideal bulk terminated surface during typical growth conditions. On C-face there is only one available bond to one carbon atom on the surface. Consequently, C-face material suffers more easily from reevaporation of adsorbed aluminum containing species.

Our investigation shows that the aluminum atoms are relatively immobile on the surface. The incorporation is more related to the carbon coverage on the terrace. High carbon coverage creates more available stable sites for aluminum species to bond to. In the case of increased growth rate the aluminum incorporation increases, as shown in fig. 1a and 1b. The increased precursor flow (maintaining C/Si ratio constant), resulting in an increased growth rate, creates more available lattice sites for the aluminum species due to the increased carbon coverage. Although the silicon coverage increases at the same time it does not seem to out compete the aluminum atoms. At very high growth rates the aluminum incorporation saturates and the incorporation becomes diffusion limited. The C-face suffers from reevaporation of aluminum species but very high growth rate could reduce this effect.

The thermodynamical calculations have shown that reduced pressure increases the C/Si ratio. The increased C/Si ratio will enhance the aluminum incorporation [2]. At low growth rate the Si-face suffers from reevaporation of aluminum species due to the low carbon coverage. Consequently, at low growth rate, the aluminum incorporation increases with reduced pressure due to the increased C/Si ratio. At a critical pressure of 300 mbar the

aluminum incorporation has its maximum and a further decrease of the total pressure reduces the aluminum incorporation due to reduced partial pressure of the aluminum containing species, as can be seen in fig. 2a. At high growth rate and at atmospheric pressure (diffusion limited incorporation) all aluminum species are incorporated and the aluminum incorporation decreases with reduced pressure which is due to reduced partial pressure of the aluminum containing species, see fig. 2b. Although the C/Si ratio increases, which creates more available lattice sites, all aluminum species are already bonded to the surface and the incorporation becomes C/Si ratio independent.

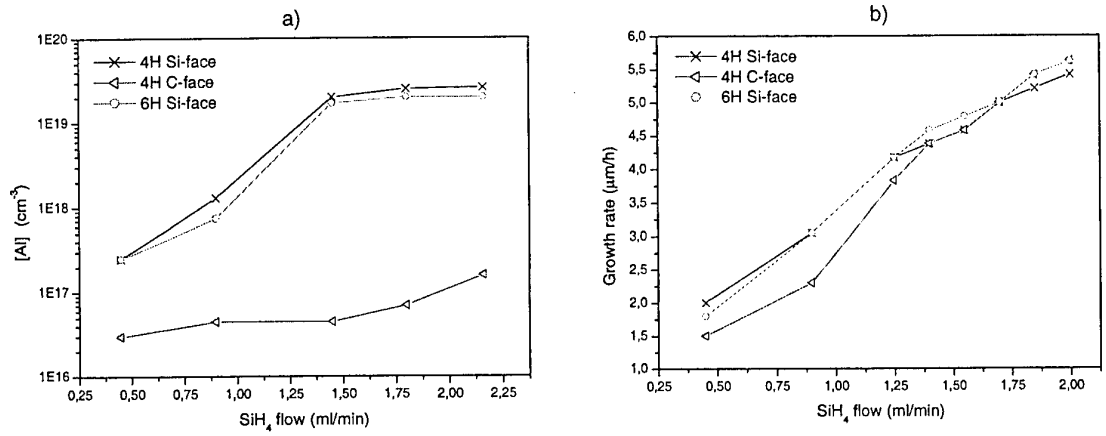


Fig.1 a) The aluminum incorporation dependency of silane input flow b) the growth rate versus silane input flow. The C/Si ratio was kept constant at 3.5, the growth temperature was T=1600 °C and the reactor pressure was P=1013 mbar.

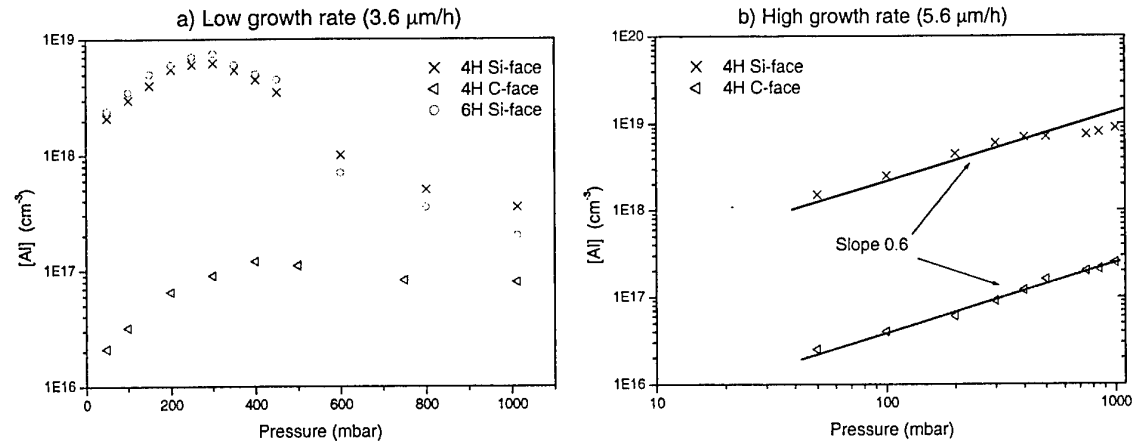


Fig. 2 The aluminum incorporation versus pressure presented at a) low growth rate and b) high growth rate. The C/Si ratio was kept constant at 3.5 and the growth temperature was T=1600 °C.

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Investigation of residual inpurities in 4H-SiC epitaxial layers grown by hot-wall chemical vapor deposition

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Introduction

A lot of work has been concentrated to realize higher growth rate in CVD at higher growth temperature. Therefore, next to the crystal imperfection, reduction of residual impurities in epitaxial layers becomes the most essential issue to be focused. There are some reports that consider graphite susceptor as a source of the contamination to the epitaxial layers [1,2]. There has been, however, no precise study on the cause and effect of residual impurities thus far.

In this work, the effectiveness of the SiC coating and the change in various impurity contamination has been investigated.

Experimental

The epitaxial layers without intentional impurity-doping were grown by using a horizontal hot-wall CVD reactor. Precurser gases used were monosilane and propane in hydrogen atmosphere. Growth pressure was around 250 mbar. Growth duration time was about 4 hours for each run. Temperature dependence on residual impurity concentraion was studied between 1500 and 1600 °C. Effect of run number was also studied. Impurity concentration was determined by SIMS analysis for B, Al, Ti, V, Cr, and Fe. Nitrogen concentration in the epitaxial film was estimated by photo luminescence [3]. Minority carrier lifetime was measured by the microwave photo conductivity decay method.

Results and discussion

It was found that when the temperature gets higher, both nitrogen, aluminum, and boron concentrations in the epitaxial layers increase. Nitrogen was the most abundant species than any other impurities studied.

On of the most important approach to reduce the contamination from the graphite susceptor has been SiC coating. Even this widely employed technique cannot be the complete answer to the prohibition from contamination at higher temperature [4]. In Fig. 1, growth run number dependence on nitrogen is shown. The dependence on aluminum and boron is depicted in Fig. 2. Also, the dependence on the transition metals is shown in Fig.3. In the present study, the coating layer became something like peeled-off after about only 4 runs. After degrading the coating layer, nitrogen concentration increases rapidly whereas aluminum and boron slowly. Effective carrier lifetime is shown as a function of growth run number in Fig. 4. The tendency of the lifetime decrease might suggest that lifetime determining impurity might be transition metals.

Summary

When the growth temperature is higher, it has been found that nitrogen is the most abundant species to contaminate the epitaxial film. We have concluded that SiC coating is not reliable for the use in this temperature range. In order to realize extremely pure epitaxial layers for high voltage device application, further development of purifying graphite is indispensable.

Acknowledgement

This work was performed under the management of FED as a part of the METI NSS Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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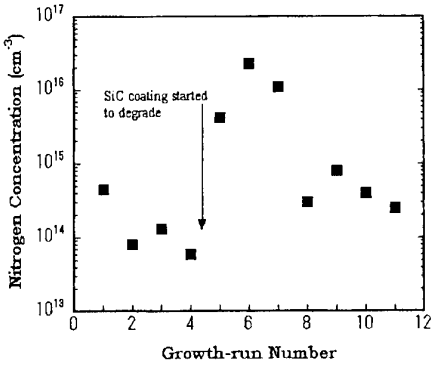


Fig. 1 Growth-run number dependence of nitrogen concentration.

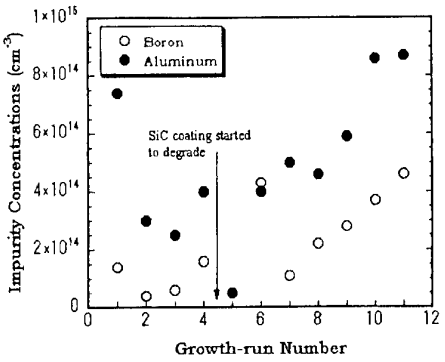


Fig.2 Growth-run number dependence of aluminum and boron concentrations.

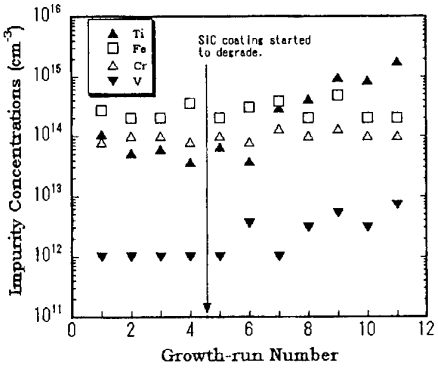


Fig. 3 Growth-run number dependence of transition metal concentrations.

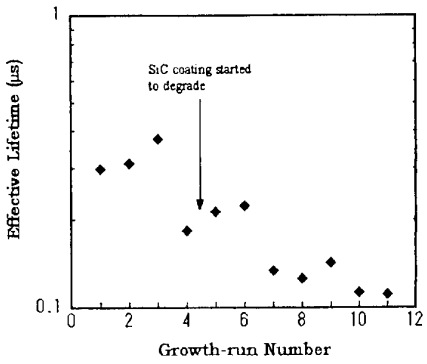


Fig.4 Effective lifeteime dependence on growth-run number

Fast Growth and Doping Characteristics of α-SiC in Horizontal Cold-wall CVD

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To consider device application of SiC, requirements for homoepitaxial growth are good surface morphology, uniformity of film thickness, uniformity and controllability of impurity doping, and high growth rate for thick epilayers. For the last requirement, hot-wall CVD, both horizontal and vertical, have been proposed and developed. In contrast, atmospheric-pressure horizontal cold-wall CVD can be carried out with a simple system, and can produce good uniformity and controllability of impurity doping. However, few has been reported on homoepitaxy at high growth rates. In this study, high-speed homoepitaxy by horizontal cold-wall CVD was investigated.

The substrates used in this study were commercially-available off-axis n-type 4H-SiC (0001) and p-type 6H-SiC (0001), and the epilayers were grown simultaneously. Source gases were SiH_4 and C_3H_8, and carrier gas was H_2 (typical flow rate: 3 slm). The typical SiH_4 flow rate was $0.85 \sim 1.5$ sccm and the C/Si ratio was $2 \sim 3$. The growth temperature was typically 1500 °C, and the growth time was $2 \sim 6$ hours.

Previously, it was reported that the growth rate was proportional to the SiH_4 flow rate [1], but a high SiH_4 concentration over 200 ppm degraded surface morphology [2]. However, by improvements of initial growth condition, good surface morphology as shown Fig. 1 was obtained at a high SiH_4 flow rate of 1.5 sccm (500 ppm).

Figure 2 shows the relationship of the growth rate and the SiH_4 flow rate. The growth rate was found to saturate at about 6 μm/h. The saturated growth rate seemed to be independent of C/Si ratio within $2 \sim 4$, growth temperature within $1500 \sim 1600$ °C, and carrier gas flow within $3 \sim 10$ slm, whereas another group reported an increase of growth rate under a high carrier gas flow [3]. The saturation of growth rate should be attributed to polymerization of SiH_4: once SiH_4 polymerizes to form clusters, the clusters are exhausted from the reaction system.

Some runs of six-hour growth were carried out to produce about 30 μm-thick epilayers. With a SiH_4 flow rate of 1.0 sccm the surface of epilayers showed severe macro-step bunching. Reducing the SiH_4 flow rate to 0.85 sccm and the C/Si ratio to 2, macro-step bunching was alleviated. In spite of low C/Si ratio of 2, the residual donor concentration was within low 10^{14} cm^{-3} as already reported for long-time growth with a lower SiH_4 flow rate [4], and was tend to decrease with increasing SiH_4 flow rate. With a SiH_4 flow rate of 0.85 sccm or above and a C/Si ratio of 3, the epilayers showed p-type conduction with a net acceptor concentration below 10^{15} cm^{-3}. These results support SiH_4 exhaustion at a high SiH_4 concentration, because the SiH_4 exhaustion leads to the increase of effective C/Si ratio, which causes the decrease of donor incorporation and the increase of acceptor incorporation.

In photoluminescence (PL), relatively strong free-exciton peaks were observed. L_1 line, which is often observed in the epilayers grown at high growth rates, were hardly observed. Figure 3 shows the relationship of PL intensities and growth conditions, with

corresponding impurity concentrations. The PL intensities are normalized with the free exciton peak marked as I_{LA}. The intensity of neutral nitrogen-bound exciton Q_0 decreases with decreasing donor concentration, and is very small in the p-type epilayer. The latter is because of ionization of nitrogen donors due to compensation with acceptors.

Schottky diodes were fabricated on the thick n-type epilayers. Schottky contacts were nickel and their diameters were $300 \sim 1500\,\mu$m. No edge termination technique was employed. Figure 4 shows typical I-V characteristics. The maximum breakdown voltage was 3.6 kV, about two thirds of ideal parallel-plane blocking voltage (5.3 kV). Using these Schottky diodes, deep levels were analyzed and will be discussed briefly.

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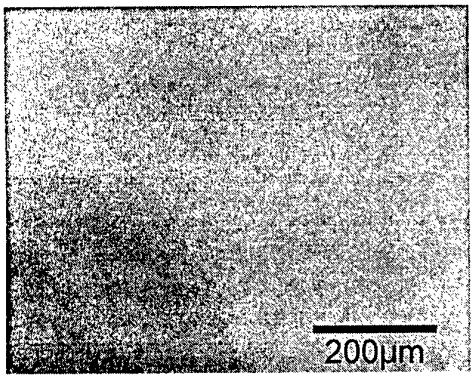


Figure 1: Surface morphology of 4H-SiC epilayer grown with SiH_4 flow rate of 1.5 sccm.

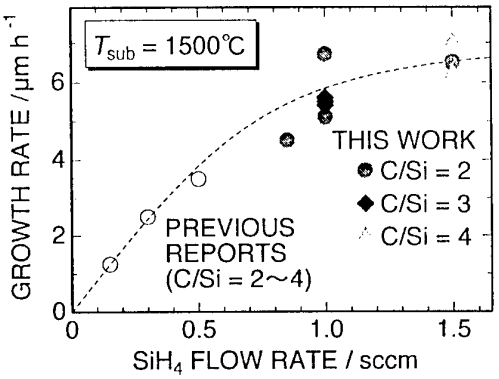


Figure 2: Relationship of growth rate and SiH_4 flow rate.

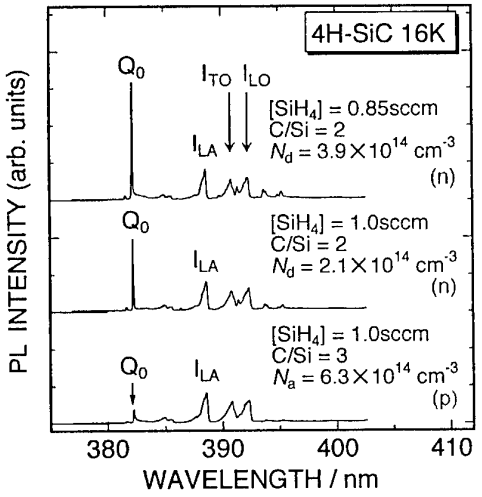


Figure 3: Relationship of PL intensities and growth conditions, with corresponding impurity concentrations.

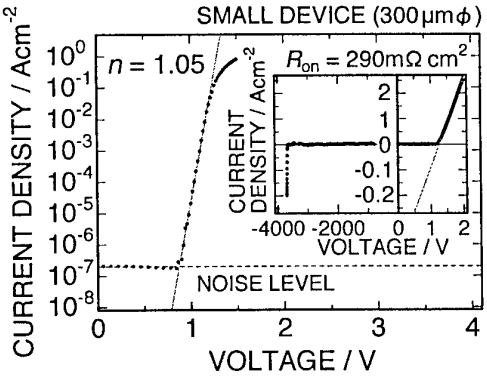


Figure 4: Typical I-V characteristics of a Ni Schottky diode on 31 μm-thick epilayer. Donor concentration of the epilayer was about 2×10^{14} cm^{-3}.

GROWTH, CHARACTERIZATION AND PROPERTIES OF SiC QUANTUM WELL STRUCTURES

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Semiconductor heterostructures and superlattices are of increasing interest in various applications. But investigations of such structures have been focused on mostly on systems consisting of different chemically materials such as GaAs/AlAs. However, in recent years also new types of heterostructures are under discussion consisting of only one material with different types of crystal structures, such as wurtzite/zinc-blende heterostructures. In such structures, for example effects due to different chemical constituents can be avoided. Therefore, by changing the crystal structure during the growth in a controlled manner, it is possible to prepare heterostructures maintaining a completely defect-free, lattice matched, and coherent interface.

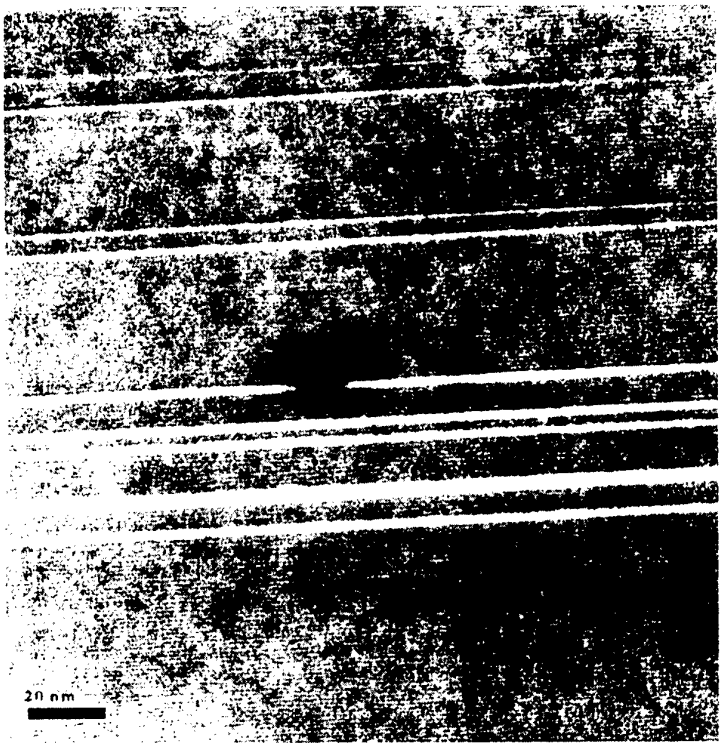
In this field silicon carbide is the most promising candidate because SiC crystallizes in more than two different stable structures with different physical properties, in particular variations of the energy gap of about 1 eV. This is what makes SiC especially interesting for semiconductor application in comparison for example to AlGaN/GaN heterojunction devices.

In this work we like to present results of the growth and the investigation of multi quantum well (MQW) structures of SiC. The growth of MQW structures consisting of some dozens of hexagonal SiC barriers and of 3C-SiC wells has been performed by solid-source molecular beam epitaxy on hexagonal off-axis substrates.

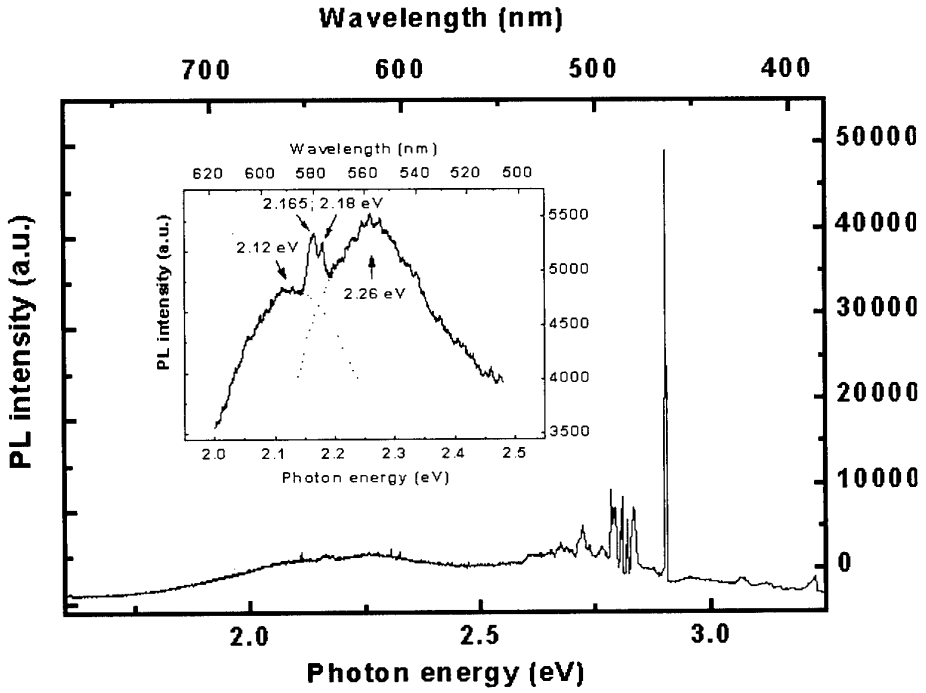
In a first step, wire-like 3C-SiC was grown selectively on some wider terraces of the substrates at lower temperatures (<1500 K), where the number if wires is determined by the width of the terraces and the temperature. In a second step, SiC was grown via a step-flow growth mode of both the hexagonal matrix material and the 3C-SiC wires at higher temperatures (1600 K) resulting in the formation of multi-heterostructures of SiC polytypes (upper figure). The thickness of the 3C-SiC layers (2.3 nm in average) is determined by the 2-3 nm heights of the steps on the substrate surface.

Photoluminescence investigations of the MQW structures reveal additional signals, which were not obtained for thick homoepitaxial layers consisting of one polytype (lower figure). This new signals can be explained within the model of a triangular electron quantum well in 3C-SiC. Furthermore, the electrons in the MQW structure should be localized in the 3C-SiC layer at one heterointerface, whereas holes may occur on the other side of the heterostructure in the hexagonal material near the second interface. This seems to be supported by capacity-voltage (C-V) measurements in which a modulation of the electron concentration was detected.

This financial support of the Deutsche Forschungsgemeinschaft (SFB 196, Projects A 03, A08, A10) is gratefully acknowledged.



High-resolution TEM micrograph of a multi quantum well structure with 3C-SiC wells (light stripes) between 4H-SiC barriers grown on 4H-SiC.



LTPL spectrum of a 3C/4H-SiC multi quantum well structure grown on 4H-SiC(0001). The inset shows the low energy region between 2 and 2.5 eV in a higher magnification.

Delta-Doped Layers of SiC Grown by "Pulse Doping" Technique

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It is expected that the delta-function doped structures have a great potential for realizing high-performance SiC devices. In this study, delta-doped layers of SiC were investigated by our original "pulse doping" technique during epitaxial growth in the hot wall type CVD system.

The vertical hot wall type CVD system equipped with the pulse valve was described elsewhere in detail.[1] Commercially available 4H-SiC wafers with n-type doping in $10^{18}cm^{-3}$ range were used for the substrates. Typical epitaxial growth temperature and pressure were 1600°C and 90kPa, respectively. The flow rates of SiH_4, C_3H_8 and H_2 carrier gas were set to 3.0sccm, 0.5sccm and 2slm, respectively. The N_2 gas was selected as n-type dopant. Typical growth rate was about 2μm/hr under the conditions described above. The pulse valve, which is a solenoid valve, can open and close within <10μs. In this study, the dopant gases were intermittently introduced and managed utilizing the pulse valve without mass flow controller. It has been derived that the carrier concentrations of the doped layers were increased from 10^{15} to $10^{18}cm^{-3}$ with increasing the on period of pulse valve from 90 to 120μs with its off period of 4ms during "pulse doping".[1]

"Pulse doping" technique enabled formation of very abrupt interface between doped and undoped layers. 10nm-thick doped (delta-doped) layer of SiC was grown utilizing "pulse doping" for 20 sec during continuous epitaxial growth. The doping profiles of the delta-doped layers were analyzed by capacitance-voltage (C-V) measurement and secondary ion mass spectroscopy (SIMS). The peak carrier concentration is $1x10^{18}cm^{-3}$ surrounded by the undoped layers with the impurity concentration of the order of $10^{15}cm^{-3}$. The full width at half maximum (FWHM) of the delta-doped layer is measured to be less than 12nm. Furthermore, it is noted that the stratified structures of the delta-doped layers are achieved in the SiC epitaxial films for the first time. Consequently, it is possible to completely shut off the supplied dopant gas within a very short term by "pulse doping", so that the delta-doped layers can be formed in the hot wall type CVD system even at higher temperature region.

In conclusion, delta-function doped layers of SiC were successfully formed by "pulse doping" technique in the hot wall type CVD system. "pulse doping" technique leads novel SiC devices, such as MESFET and MOSFET (DACFET) based on the delta-doped layered structures.[2-4]

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ThB2 Interfaces [redacted]

Measurement of the Interface Trap Density in SiC MOS Devices using the Hall Effect

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The conductance of SiC MOSFETs is currently limited by trapping of electrons in inversion layers at the SiC/SiO_2 interface. This trapping causes both a reduction in the number of free electrons and a reduction in the mobility of the remaining free electrons due to increased coulombic scattering. Trap profiles are currently characterized using capacitance-voltage (C-V) measurements using MOS capacitors on n-type SiC substrates (as opposed to p-type substrates used for n-channel MOSFETs), which makes C-V analysis more difficult and somewhat questionable.

Here we present a Hall effect technique for measuring the trap density without the drawbacks of C-V analysis. This technique has a major advantage in that the measurement is performed on the SiC MOS inversion layer and therefore the traps characterized are those which directly affect electron trapping and transport. Similar Hall effect analysis of interface traps was first discussed early in the development of silicon MOS devices [1] but was not widely adopted because the technique is too insensitive for accurate measurement of the low trap densities typical in silicon devices. The technique requires fabrication of an MOS Hall bar, which is basically a MOSFET with extra voltage taps.

In this technique [1], the Hall mobility μ_e and inversion layer electron density n_{inv} are measured as a function of the gate voltage V_{exp}. For each experimental value of n_{inv}, the surface potential $\phi s(V_{exp})$ required to induce that value of n_{inv} is calculated. Then, for any two values of $\phi s(V_{exp})$, it is also possible to calculate the theoretical *change* in gate voltage ΔV_{calc} required to cause this change in ϕs. The change in the number of trapped electrons Δn_t is then calculated from $\Delta V_{exp} = \Delta V_{calc} + q^*\Delta n_t / Cox$ where $q = 1.6x10^{-19}$ C and Cox is the gate oxide capacitance. The trap density D_{IT} is obtained from $D_{IT}(\phi s) = \Delta n_t / \Delta \phi s$.

Results for $D_{IT}(E_{TRAP})$ for trap energy E_{TRAP} referenced to the conduction band edge Ec are shown in Fig. 1 for a 6H-SiC sample. $D_{IT}(E_{TRAP})$ was calculated using Fermi-Dirac statistics which is more accurate than Maxwell-Boltzmann close to Ec. Previous measurements using low-frequency C-V analysis of a similar sample from a different wafer from the same process lot are shown for comparison [2]. Below Ec, the trap densities increase with increasing trap energy, consistent with previously reported results [2,3]. At or above Ec, $D_{IT}(E)$ appears to flatten out or even decrease. Correlation with C-V results is reasonable. The Hall measurements clearly show far less scatter than the C-V results and are more accurate.

Trap profiles for 4H-SiC and 6H-SiC samples are compared in Fig. 2. Both samples show an increasing $D_{IT}(E_{TRAP})$ with increasing trap energy below Ec. $D_{IT}(E_{TRAP})$ is significantly higher (a factor of 4-5) in 4H compared to 6H-SiC, consistent with many previous results [4].

In Fig. 3, we report an example of the use of these Hall D_{IT} measurements. Results are obtained on a single 6H-SiC MOS Hall bar (A) before stress, or (B) after stressing by high-field constant-current injection of electrons into the gate oxide. Fig. 3A shows the increase in D_{IT} after stress. Fig. 3B shows the accompanying reduction in electron mobility, plotted as a function of inversion layer effective field. The mobility reduction presumably arises due to increased scattering from the higher density of trapped electrons. It is apparent that this method should be useful in studying similar behavior, such as the long-term reliability of SiC MOSFETs under operating conditions.

In summary, we have reported on the initial use of Hall effect measurements to characterize the Dit profile in SiC MOSFETs. This approach is found to be accurate, straightforward to implement, consistent with known behavior and previous results, and is promising for future experiments. Control experiments have also been performed on silicon MOS devices and the results will be presented at the conference.

Acknowledgement: This work was partially supported by Dr. G. Campisi of ONR.

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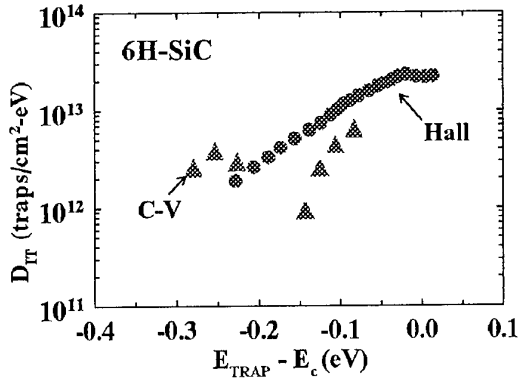


Figure 1

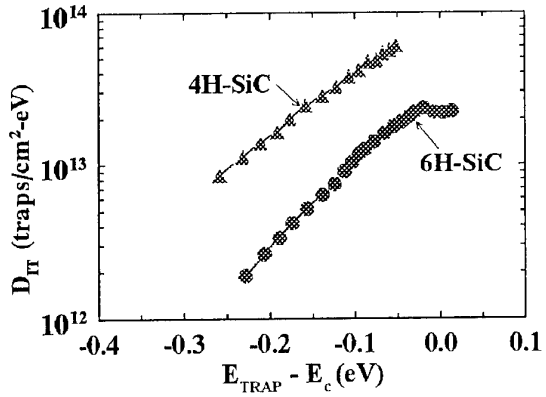
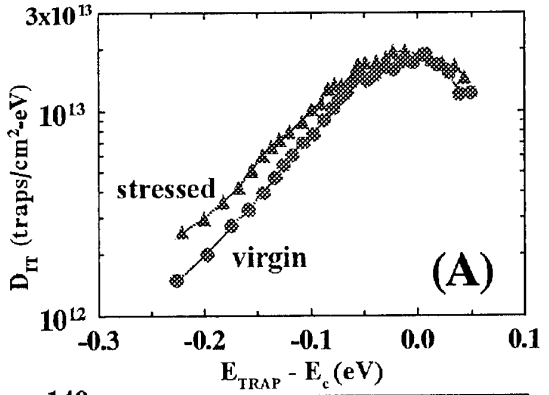


Figure 2



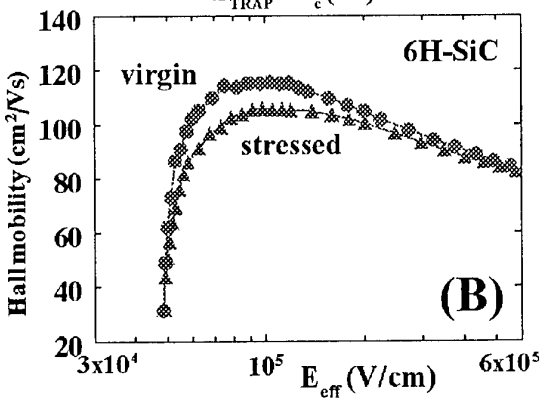


Figure 3

Passivation of the Oxide–4H SiC Interface

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Abstract: Current progress in the development of MOSFETs on 4H SiC is seriously hindered by high levels of interface traps that degrade channel mobility. However, it has been established that thermally grown oxides annealed in nitric oxide (NO) ambient provide critical improvements of the oxide–SiC interface: reduction of interface traps density [1-4], increased channel-carrier mobility [5], and increased reliability [6]. Chung *et al* [3] reported that the interface-trap density near the valence-band edge increases by about a factor of two following NO annealing. They speculated that a possible *passivation* of carbon atoms and carbon clusters by nitrogen causes shifts of interface-trap levels from the upper half of the energy gap to just above the top of the valence band. However, past [6] and present studies by our group have consistently demonstrated that NO annealing of dry oxide results in significant reduction of interface-trap density in the case of both N-type and P-type substrates. Figures 1 and 2 show that this reduction is especially pronounced around the midgap, in a direct analogy with the passivating effect of hydrogen in the case of SiO_2–Si interface. The main aim of this paper is to analyze and clarify the passivating role of nitrogen at the SiO_2–SiC interface.

The comparison of interface-trap distributions for dry, wet, and nitrided oxides (Figs. 1 and 2) leads to the following conclusions. DRY OXIDES: there are a high density of weak and strained bonds between trivalent silicon atoms from SiC and atoms in the oxide, resulting in energy levels around the midgap. WET OXIDES: Si-H and Si-OH bonds replace strained bonds, shifting the energy levels away from the midgap, however, not sufficiently to remove them from the wide energy gap of SiC (the shift is sufficient for the case of narrower energy gap of Si). NITRIDED OXIDES: much stronger Si≡N bonds are formed, their energy levels are much further from the midgap, and as a result, the levels appearing in the energy gap (interface traps) is significantly reduced. We have confirmed the existence of Si≡N bonds at the SiO_2–SiC interface by XPS analysis [7]. This analysis also revealed a small amount of C–N bonds, but they appear near the interface and could not be assigned a *passivating* role as assumed by Chung *et al.* [3]. In fact, we identified a number of experimental results indicating that C–N bonds are more likely to be associated with the nitrogen-assisted removal of carbon from the interface [8]. Therefore, we conclude that the Si≡N bonds play the passivating role at the SiO_2–SiC interface.

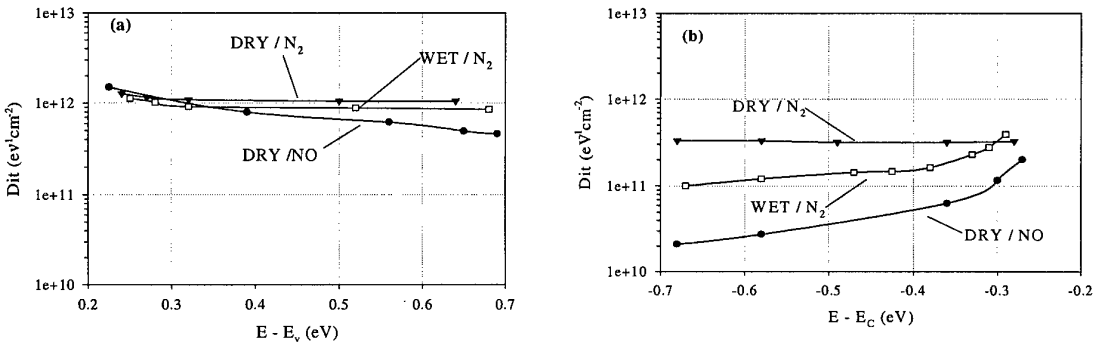


Fig. 1 Interface-trap distributions measured at 200°C by the conductance technique: (a) P-type, (b) N-type.

Much higher density of interface traps is commonly observed on P-type SiC substrates (also obvious in Figs. 1 and 2). We believe this is due to the inferior quality of these substrates, rather than strongly asymmetric distribution of the interface traps. This view is supported by the very large shifts of the C–V curves for MOS capacitors on P-type SiC (Fig.3a). Although this shift is probably due to both interface and near-interface trapped charge, the fact is that such large shifts are not observed with N-type substrates (Fig. 3b). The large reduction of the C-V curve shift in the case of nitrided oxides is probably, to a large extent, due to the nitrogen-assisted carbon removal. Nonetheless, Figs. 1 and 2 clearly reveal analogous and complementary interface-trap reduction for both P-type and N-type substrate, which can be explained by the passivating effect of Si≡N bonds.

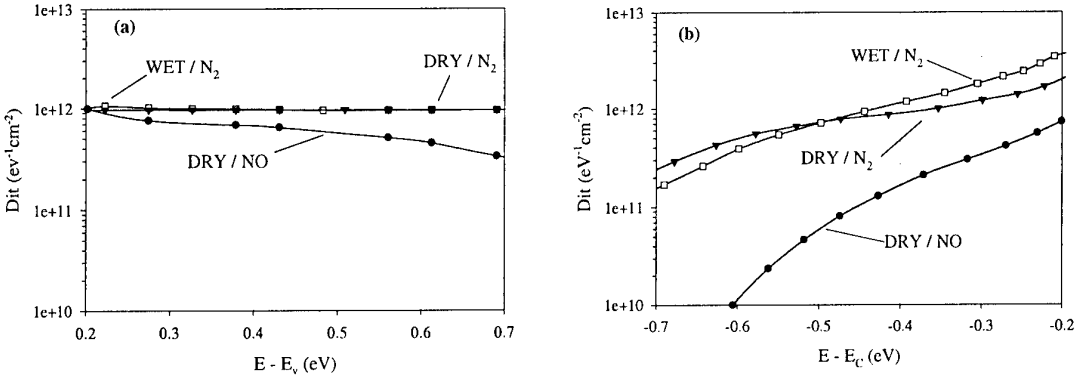


Fig. 2 Interface-trap distributions measured by the Hi-Lo CV technique: (a) P-type, (b) N-type.

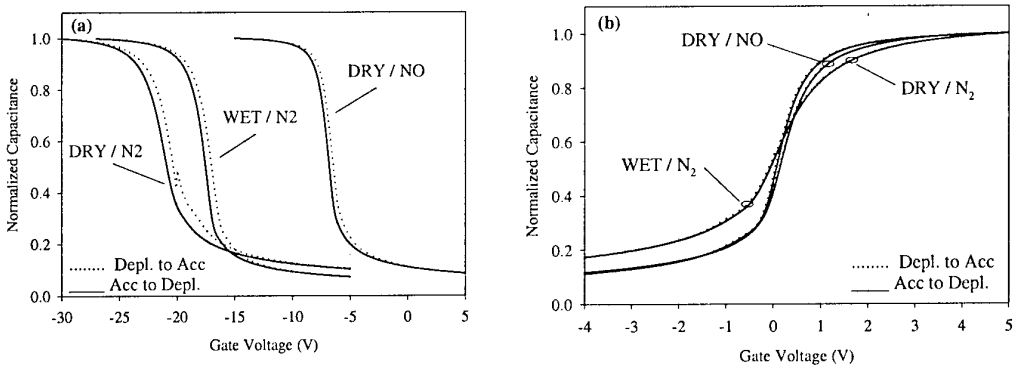


Fig 3 Normalized high-frequency C–V curves of wet, dry, and nitrided oxides: (a) P-type, (b) N-type.

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Improving 4H-SiC/SiO2 Interface Properties by Depositing Si Nitride Layer Prior to Formation of SiO2 and Annealing

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I. Introduction

Low channel mobility is known to be a major obstacle in commercialization of enhancement-mode 4H-SiC MOSFETs. Extensive studies have attributed the low channel mobility to high density of interface traps (Dit) near conduction band edge [1]. Recent studies have suggested that nitrogen incorporation in the SiO_2/4H-SiC system may have a significant impact on the interface properties [2]. In this study, we deposited an ultra-thin silicon nitride layer directly on 4H-SiC substrate prior to formation of SiO_2 and annealing, and found much reduced interface-trap density and oxide charge density. Our lowest Dit values are on the order of $1x10^{12}/cm^2$–eV or below at energies near the conduction band edge. XPS spectra confirm the presence of nitrogen at the SiO_2/SiC interface and suggest possible bonding between N and C.

II. Experimental

We use research grade n+-4H-SiC with a 10 μm epi-layer doped n-type to $2.6x10^{15}/cm^3$. Following the standard RCA cleaning, SiC wafers were loaded into jet vapor deposition (JVD) chamber. Details of the JVD system and its operation can be found elsewhere [3]. The control samples are MIS capacitors with a ONO dielectric stack consisting of a 20nm-thick JVD silicon nitride sandwiched between two10nm-thick JVD SiO_2 layers. The ONOn samples are basically the same as the control, except that they have an ultra-thin silicon nitride (≤2.0nm) layer deposited on SiC before the ONO stack deposition. The lower-case n in ONOn signifies an ultra-thin nitride layer, which was deposited in the same way as the thick nitride layer of the ONO stack [4], but with the SiH_4 follow rate adjusted to obtain optimized interface properties. The post-deposition-anneal (PDA) process consists of two steps: a 900 °C anneal in N_2 followed by a 950 °C anneal in a water vapor ambient, with each one lasting 1.5 hr. Al was used as the contacts. No post-metal-anneal was performed before electrical measurements. AC conductance measurements were carried out at room temperature to obtain Dit distribution. XPS spectra were taken on a sample with an optimized ultra-thin nitride layer at the interface and a 10nm SiO_2 on top. This sample resembles the ONOn /SiC interface but without the top O- and N-layers.

III. Results and Discussion

Figure 1 shows multi-frequency C-V curves measured on a capacitor with an ONO gate stack (right) and one with an ONOn stack (left). One can see that the addition of an ultra-thin nitride layer prior to ONO deposition sharpens significantly the slopes of these CV curves, even though the ultra-thin layer was not optimized in this sample. It seems more interesting that, compared to the control, the location where the strongest frequency dispersion occurs has shifted downward, suggesting that the energy of the peak Dit has shifted away from the conduction band edge, which should be beneficial for n-channel mobility. Encouraged by such results, we started a systematic study to optimize the effect of the ultra-thin interfacial nitride layer. Figure 2 compares the multi-frequency C-V curves of a set of samples whose interfacial silicon nitride layers were deposited with different SiH_4 flow rates. It is clearly seen that the frequency dispersion decreases systematically with decreasing SiH_4 flow rate, from 2 to 0.6 sccm, and the nitride layer deposited with a SiH_4 flow rate of 0.6sccm results in the best Dit data. Further decrease of the SiH_4 flow rate causes the C-V curves to degrade again, as manifested in the increased stretch-out and larger frequency dispersion near strong accumulation. The trend shown in Fig.2 suggests that a finite amount of Si is necessary at the interface to realize the beneficial effect, but excessive amounts of Si tend to reduce the beneficial nitrogen effect. Shown in Fig.3 are the Dit distributions of our JVD ONO and ONOn samples along with some published Dit data for comparison. As indicated by the solid triangles in Fig.3, our previous JVD ONO stack yielded Dit values no better than those samples made of conventional thermal SiO_2. However, with an ultra-thin silicon nitride layer added at the SiO_2/SiC interface, the Dit values in the energy range of 0.1 - 0.2 eV below the 4H-SiC conduction band are decreased over an order of magnitude, to $1x10^{12}/cm^2$-eV or bellow. To our knowledge, these are the lowest Dit values in this energy range that have ever been reported for 4H-SiC. Figure 4 shows the XPS spectra of, (a) N1s, (b) C1s, (c) Si2p, and (d) O1s, respectively, for a sample described in the **Experimental** Section. Despite its noisy appearance, Fig. 4(a) clearly shows the presence of nitrogen at the SiO_2/SiC interface for the ONOn sample. The binding energy of

398.3eV for N1s (~0.5eV higher than that for Si_3N_4) suggests that the ultra-thin silicon nitride layer may have evolved to an oxynitride other than a stoichiometric Si_3N_4 during the subsequent oxide deposition and PDA processes. It is also possible that some of the nitrogen atoms have bonded to C and/or Si atoms on the SiC surface, as the binding energies of the N1s peak also overlap the range for N1s in Cyanides (397.5-400.3eV). This latter possibility is supported by the broad tail on the higher energy side of the main C1s peak in Fig.4 (b). Comparing to rest of C1s spectra taken at shallower angles (not shown), this broad tail shows up only at the interface and the energy range of this tail overlaps that indicating C-N bonds. The main peak corresponds to absorbed carbon that exists throughout the depth of the film, which most likely originates from the pump oil vapor during the entire process of film deposition. Both the binding energies and the sharp, symmetric shape of the Si2p and O1s spectra shown in Figs. 4(c) and (d), respectively, demonstrate a quality SiO_2 with unnoticeable amounts of sub-oxides at the interface. The fitted Si2p spectrum in Fig. 4(c) reveals the contribution from the ultra-thin silicon nitride layer (represented by the small peak at 100.83eV) at the SiO_2/SiC interface, which is consistent with the information provided by the N1s spectrum in Fig. 4(a). However, possible contribution from the SiC substrate to this peak cannot be ruled out because the Si2p binding energies for Si bonding in SiC are coincident with energies for Si bonding in SiN_x (e.g., one silicon atom bonded to two nitrogen atoms).
In summary, we have demonstrated significant reduction of interface-trap density near the conduction band edge by adding an ultra-thin layer of silicon nitride before gate oxide deposition. This reduction is possibly related to the presence of nitrogen at the SiO_2/SiC interface. More detailed and careful XPS study is necessary to correlate the electrical improvement to possible nitrogen passivation of Si and/or C dangling bonds at the interface.

Acknowledgement
The authors wish to thank Dr. Tamagawa for his continuous support of the JVD system. This work was supported by an ONR research contract (via a subcontract from Purdue University).

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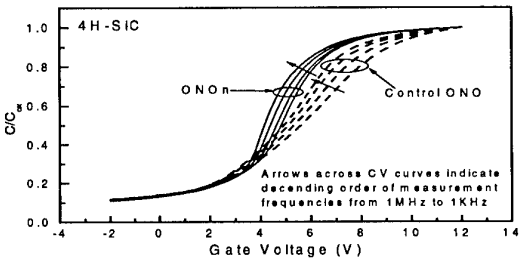


Fig.1 Multi-frequency C-V curves taken on JVD ONO & JVD ONOn samples

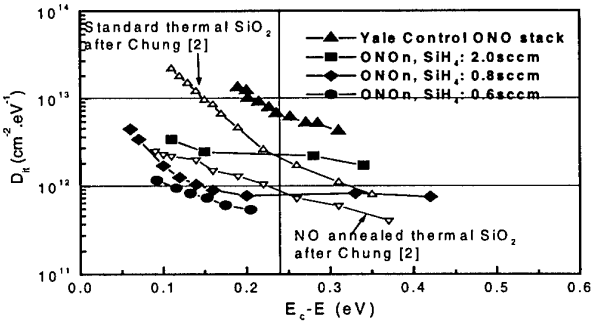


Fig.3 D_{it} distributions for JVD ONO control and ONOn samples with variable SiH_4 flow rate for the ultra-thin silicon nitride layer. Open symbols are reference data after Chung.

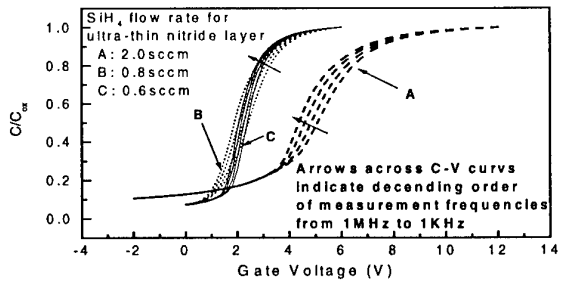


Fig. 2 C-V characteristics improved significantly with decreasing SiH_4 flow rate used for deposition of the ultra-thin interfacial silicon nitride layer

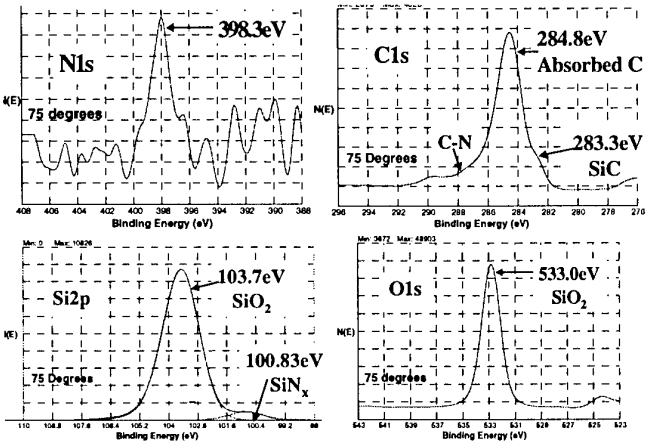


Fig. 4 XPS spectra of N1s, C1s, Si2p and O1s, respectively, taken at ONOn/4H-SiC interface.

New Evidence of Interfacial Oxide Traps in n type 4H– and 6H–SiC MOS Structures

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The great potential of silicon carbide MOS devices for high power and high temperature applications has thus far been hampered by insufficient quality of the oxide grown on SiC. A major concern in MOSFET SiC devices is the low electron channel mobility observed [1, 2]. One of the possible reasons is considered to be charge trapping in shallow interface states whose density is in general higher in 4H– than in 6H–SiC [2, 3].

In this work we study interface traps near the conduction band in n type 4H– and 6H–SiC metal–oxide–semiconductor (MOS) structures using the thermally stimulated current (TSC) technique. We find that differently prepared MOS capacitors show characteristic features in the TSC spectra, which cannot be ascribed to traps located immediately at the interface, and we assign these features to energetically shallow traps distributed in the oxide. The main difference between the TSC spectra observed for 4H– and 6H–SiC MOS structures is the manifestation of the oxide traps in a different temperature range.

Our MOS capacitors were fabricated on commercially available nitrogen doped 4H– and 6H–SiC epitaxial layers grown on the Si–face of SiC substrates and we compare oxides made using several oxidation procedures.

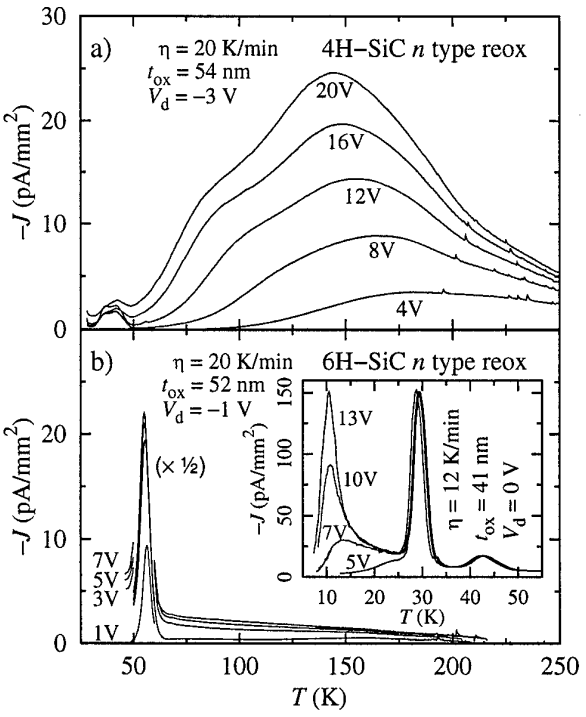


Fig. 1: TSC spectra for n type (a) 4H–SiC and (b) 6H–SiC MOS structures, measured for several charging voltages.

In the TSC technique, occupied trap levels thermally emit carriers which are detected as a displacement current. At a temperature T_0, the MOS structure is biased with the charging voltage V_0 while the temperature is lowered to T_1. The bias is then changed to the discharging voltage V_d, which usually corresponds to depletion at the interface, and the temperature is raised with a linear heating rate η while the current is measured. The volume and interface components of

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the TSC spectrum are identified by comparing measurements with various charging and discharging voltages. In addition, MOS structures were characterized using high– and low–frequency capacitance–voltage analysis.

The oxides of the MOS capacitors used for the measurements in Fig. 1 were made by dry thermal oxidation at 1150°C for 4 h, immediately followed by a reoxidation anneal at 950°C in pyrogenic steam for 3 h. The resulting oxide thickness was t_{ox}. Fig. 1(a) shows TSC spectra from a 4H–SiC MOS capacitor, measured for several values of the charging voltage. The signal below 50 K is mostly due to volume states, namely the nitrogen donor in the cubic lattice site. Above 50 K the observed TSC signal comes from interface states. When the charging voltage corresponds to depletion at the SiC/SiO_2 interface, no current is measured in this temperature range. However, when the charging voltage allows accumulation at the interface, a signal appears which grows as the charging voltage increases. Furthermore, we did not observe the saturation of the interface–related TSC signal. This indicates, that the traps responsible for this part of the spectrum are most likely distributed in the oxide. In this case, it is natural to assume that the capture cross section should be very small and dependent on the electric field in the oxide. Thus, the energy levels of these traps could be expected to be close to the 4H–SiC conduction band, in spite of the fact that they are displayed in the TSC measurements at rather high temperatures. It should be emphasized that the typical features of the TSC spectra for our 4H–SiC samples was similar for differently prepared oxides. The observed border traps are possibly a signature of the native oxide defect described by Afanas'ev *et al.* [3, 4].

Fig. 1(b) shows typical TSC spectra of 6H–SiC MOS capacitors measured for different charging voltages. The behavior of the spectra is essentially different from that presented in Fig. 1(a). Here we observe a peak at 55 K which we assign to the nitrogen donor at the cubic lattice sites. Above 60 K the TSC signal is featureless and grows only slightly with increasing charging voltage. We attribute this signal to traps located immediately at the SiC/SiO_2 interface, since it vanishes if the charging voltage corresponds to depletion at the interface and its magnitude saturates as the charging voltage increases.

We expect that due to the bandgap difference between 4H– and 6H–SiC, traps observed in the temperature range from 50 to 250 K for 4H–SiC MOS capacitors, should be displayed at lower temperatures in 6H–SiC MOS structures. The inset in Fig. 1(b) shows measurements on a 6H–SiC MOS capacitor but for a lower temperature range. We assign the peaks at 30 K and 45 K to the nitrogen donor at the hexagonal and cubic lattice sites, respectively. For temperatures below 25 K we see a similar feature to the one found in Fig. 1(a). The TSC signal grows sharply with increasing charging voltage, while no current is measured if accumulation at the SiC/SiO_2 interface is not reached. We assign this signal to interfacial oxide traps and propose that it is associated with the same interfacial traps found in 4H–SiC samples at higher temperatures.

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Observation of interface states in the whole band-gap region at 6H-SiC(0001)/SiO_2 interfaces by means of x-ray photoelectron spectroscopy under bias

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1. Introduction

Interface states in the semiconductor band-gap play an important role in the determination of electrical characteristics of metal-oxide-semiconductor (MOS) devices. Because of the wide band-gap energy of SiC, interface states only in the limited energy region are observable by means of electrical technique such as capacitance-voltage (C-V) [1] and conductance-voltage (G-V) [2] measurements. In the present study, the noble spectroscopic method, i.e., x-ray photoelectron spectroscopy measurements under bias [3-5], recently developed by our group, is applied to the observation of interface states in the SiC band-gap. It is found that a sharp interface state peak is present for dry-oxidation, while it is not observed for wet-oxidation, and the peak is attributed to graphitic carbon at the interface.

2. Experiments

An SiC wafer consisted of a nitrogen-doped n-type SiC epitaxial layer of ~10 μm thickness with the donor density of 6×10^{15} cm^{-3} and a 6H-SiC(0001) substrate. After cleanig the wafer using the RCA method, an SiO_2 layer was formed by the heat treatments at 1050 °C either in wet-oxygen or dry-oxygen. Then, a 3 nm-thick platinum (Pt) layer was deposited using a thermal evaporation method, resulting in the <Pt/SiO_2/6H-SiC(0001)> MOS structure.

XPS measurements were performed using a VG SCIENTIFIC ESCALAB 220i-XL spectrometer with a monochromatic Al K α radiation source. During the XPS measurements, the front Pt layer was grounded and a bias voltage was applied to the rear SiC surface.

3. Results and discussion

Figure 1 shows the XPS spectra in the Si 2p region for the <Pt/SiO_2/6H-SiC(0001)> MOS structure. The asymmetric peak in the lower energy region is due to Si $2p_{3/2}$ and $2p_{1/2}$ peaks of the SiC substrate, and the broad peak in the higher energy region is attributable to the SiO_2 layer. From the ratio in the area intensity of these peaks, the SiO_2 thickness was estimated to be 3.1 nm.

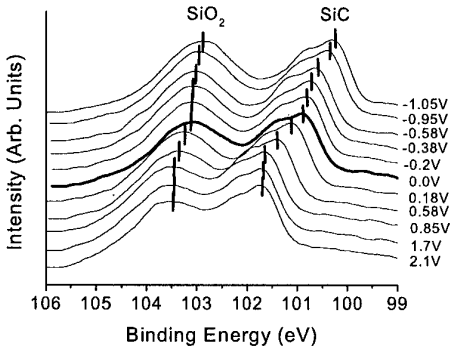


Fig. 1 XPS spectra in the Si 2p region for the <Pt/SiO_2/6H-SiC(0001)> MOS structure observed under various bias voltages applied to SiC with respect to Pt.

By the application of a positive bias to SiC, the peaks were shifted in the higher energy direction, while upon application of a negative bias, the peaks were shifted toward the lower energy. The shifts were completely reversible in contrast to chemical shifts, and they were attributed to charges accumulated in interface states by biasing. Namely, by the application of a positive (or negative) bias to SiC, the SiC Fermi level deviates downward (or upward) from the Pt Fermi level, and consequently interface states between the Pt and SiC Fermi levels are newly unoccupied (or occupied). The interface state charges induce a change in the potential drop across the SiO_2 layer, resulting in the shift of the SiC substrate Si 2p peak by the same magnitude. Therefore, by analyzing the shift of the substrate Si 2p peak measured at various bias voltages [3-5], the energy distribution of interface states can be obtained, as shown in Fig. 2. For the wet-oxidation, a broad interface state peak is present centered at 2.1 eV above the valence band maximum (VBM). For the dry-oxidation, an additional sharp peak was observed at 1.8 eV above VBM. A similar sharp peak was also observed when the wet-oxidation temperature was increased to 1150 °C, and in this case, the intensity of a C 1s

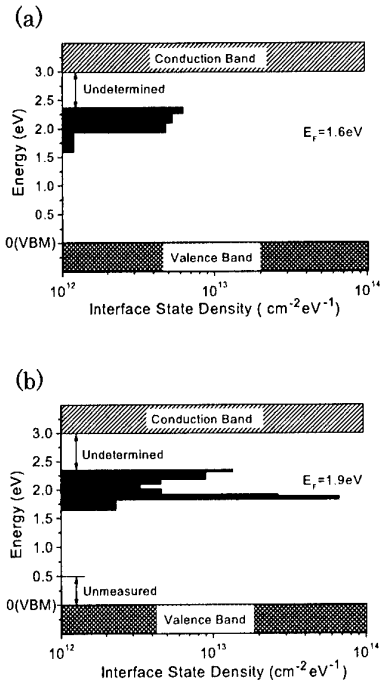


Fig. 2 Interface state spectra for the <Pt/SiO_2/6H-SiC(0001)> MOS structure with the ultrathin thermal SiO_2 layer formed in the following atmospheres: a) wet-oxygen; b) dry-oxygen.

peak due to graphitic carbon at the interface increased. Therefore, the sharp 1.7 eV-peak is attributable to interfacial graphitic carbon. It is previously reported that loss of Si occurs during high temperature thermal oxidation, resulting in the formation of graphitic carbon [6].

Figure 3 shows the current-voltage (I-V) curves for the <Pt/SiO_2/6H-SiC(0001)> MOS structure measured in the dark (solid lines) and under x-ray irradiation (dotted lines). Due to the ultrathin SiO_2 layers, the photo- and dark currents easily flowed. The I-V curve in the dark for the wet-oxide layer (curve a) was shifted in the negative bias direction from that for the dry-oxide layer (curve b). This shift is mainly attributable to the variation of the interfacial Fermi level, i.e., 1.6 eV above VBM for the wet-oxide layer and 1.9 eV for the dry-oxide layer. For the dry-oxide layer, the interfacial Fermi level is elevated because of the higher interface state density.

The I-V curve under x-ray irradiation for the wet-oxide layer was close to the ideal I-V curve shown by the dashed line [7]. This result is consistent with the relatively low interface state density. The I-V curve for the dry-oxide layer, on the other hand, deviated largely from the ideal curve. In Fig. 3, the points at the same SiC band-bending are denoted by A to C. The bias voltage at the same band-bending was determined from XPS measurements under bias. It is seen that the photocurrent densities for the MOS diodes with the dry- and wet-oxide

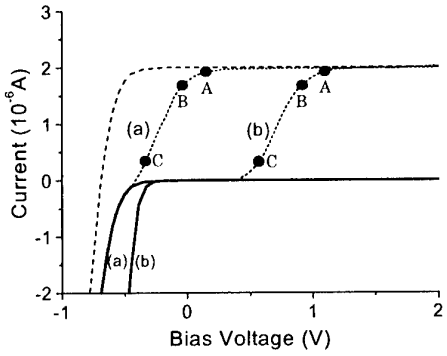


Fig. 3 I-V curves for the <Pt/SiO_2/6H-SiC(0001)> MOS structure in the dark (solid lines) and under x-ray irradiation (dotted lines) for the <Pt/SiO_2/6H-SiC(0001)> MOS structure with the ultrathin thermal SiO_2 layer formed in the following atmospheres: a) wet-oxygen; b) dry-oxygen.

layers are the same when the SiC band-bending is identical to each other. For the dry-oxide layer, the density of the interface state charges induced by the bias is high, resulting in a large potential drop across the SiO_2 layer, and consequently the net bias voltage applied to SiC is reduced. Namely, the deviation of the I-V curve from the ideal I-V curve is due to the charges accumulated in the interface states, but not due to the electron-hole recombination at the interface states.

4. Conclusions

Interface states in almost entire SiC band-gap region have been observed by means of XPS measurements under bias. For the wet-oxide layer, a broad interface state peak is present at 2.1 eV above VBM, while for the dry-oxide layer, an additional sharp peak attributable to graphitic carbon at the interafce is observed at 1.8 eV above VBM. The I-V curve measured under x-ray irradiation shifts in the positive bias direction from the ideal I-V curve due to the charges accumulated in the interface states.

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Characterization of the interfaces between SiC and oxide films by spectroscopic ellipsometry

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SiC-MOSFET is expected to have two orders of magnitude smaller on-resistance (R_{on}) than those of Si-MOSFET at the same breakdown voltage. However, so far, such a small R_{on} has not been reported. For this reason, the electron mobility in the inversion layer is thought to be severely degraded, probably due to the residual carbon at the SiO_2/SiC interfaces. Diverse oxidation and annealing methods have been studied to improve characteristic of SiO_2/SiC interfaces. Many studies have been carried out to investigate the SiO_2/SiC interfaces by, for example, C-V, X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) measurements. In the previous report, we have evaluated, for the first time, the optical constants of oxide films on SiC by spectroscopic ellipsometry[1]. In this study, we have measured the optical constants of oxide films on SiC by various oxidation ways by using spectroscopic ellipsometry, and have tried to elucidate the structure of SiO_2/SiC interfaces by comparing their refractive index-profiles.

6H-SiC epilayers, 5 μm in thickness and 5×10^{15} cm^{-3} in carrier concentration (n-type) (Cree,Inc.), were used for the measurements. The (0001) Si surfaces of SiC epilayers were oxidized by three processes, dry oxidation, pyrogenic oxidation and low temperature deposition of oxide (LTO) films. Dry oxidation was done in a pure O_2 flow at 1100°C for 16h. Pyrogenic oxidation was done in a hydrogen-oxygen flame at 1100 for 8h. LTO films were deposited by low-pressure chemical vapor deposition (LPCVD) at 400°C. The SiC substrates with the oxide layers were immersed gradually into diluted hydrofluoric acid of 8% at a constant speed to etch the oxide layers at an angle. By use of the sloped oxide films, we have measured the ellipsometric parameters (Ψ,Δ) along the slopes in the wavelength range between 250 and 850 nm at an angle of incidence of 75°. The optical constants of the oxide films, as well as the film thicknesses, assuming an optically single layer structure with uniform optical properties, were evaluated by the curve fitting of the calculated ellipsometric parameters to the measured ones. The wavelength-dependence of the apparent refractive indices of oxide films were assumed to follow Sellmeier's dispersion law, $n_{app}=\{1+((A^2-1)\ \lambda^2)/(\lambda^2-B)\}^{1/2}$ and the extinction coefficient k was assumed to be equal to 0. The parameter A indicates the refractive index at infinite wavelength, while parameter B indicates the wavelength corresponding to an intrinsic oscillation.

Figure 1 shows the thickness distribution of a pyrogenic oxide film along the slope, which reveals the oxide film was etched at an angle. Figure 2 shows the thickness dependence of n_{app} for the oxide film by pyrogenic oxidation at the wavelength λ=630nm. In the thick region, n_{app} increases with film thickness and approachs to the refractive index of bulk SiO_2 (n=1.465). In the very thin region, n_{app} decreases steeply with decreasing film thickness, approaching to 1. In the both cases of dry oxidation and LTO films, n_{app} changes with film thickness as in the case of pyrogenic oxidation. These results suggest that the refractive indices of the oxide films are not uniform but change with depth from the surfaces. We have considered that the films consist of two layers, thin interface layer and SiO_2 layer on it, and found the thickness dependence of n_{app} can be explained by the changes of the thickness of SiO_2 layers, where the thickness of an interface layer is assumed to be 1nm and its optical constants are assumed to follow Sellmeier's dispersion law. We have evaluated the values of A and

B in the Sellmeier's equation for the refractive indices of interface layers, as well as the thickness of the SiO_2 layers by use of curve fitting method. Figure 3 shows the thickness dependence of the parameter A for various oxide films. All the values of A for three oxide films are higher than the refractive index of bulk SiO_2 (n=1.465). This means there exists thin interface layers with high refractive indices, which suggests the existence of bonds with large polarization, like Si-Si bonds at the interface. The figure reveals the values of A depend on the oxidation process, and the values for LTO films are smaller than those of pyrogenic and dry oxidation. It has been reported that the LTO films have lower interface state densities and effective oxide charge densities than those of thermally oxidized films [2]. These results suggest that the values of A of the interface may relate to the electrical properties of SiC MOS structures in some extent.

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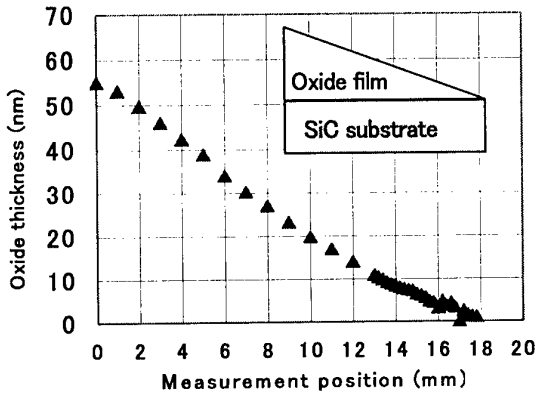


Fig.1. Variations of the thickness of a pyrogenic oxide film along the slope.

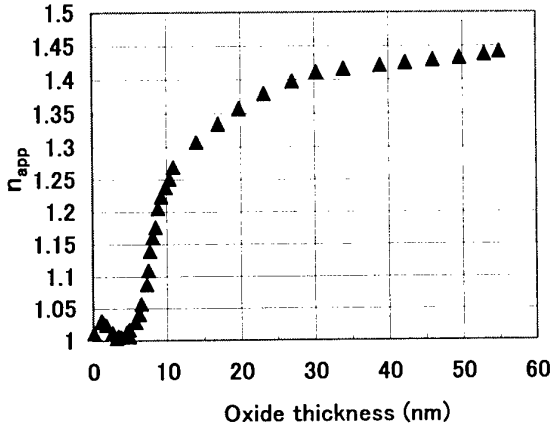
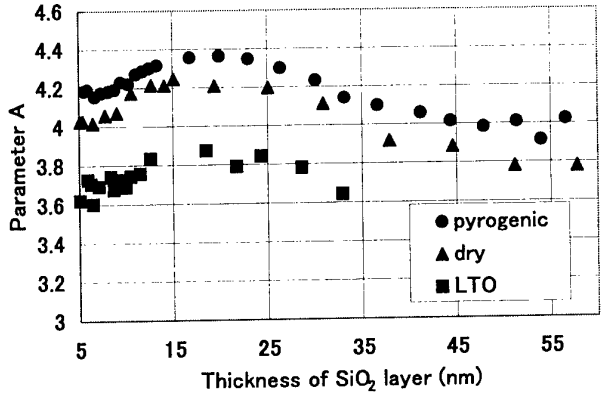


Fig.2. Thickness dependence of refractive index n_{app} for a pyrogenic oxide film (λ=630nm).



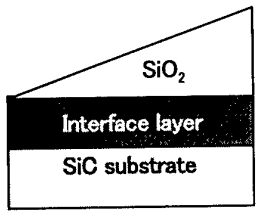


Fig.3. The values of the parameter A in Sellmeier's dispersion equation for LTO film, and pyrogenic and dry oxidation films.

ThA3 Contact and Etching



Impact of Material Defects on SiC Schottky Barrier Diodes

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This paper describes a study on the effect of material defects on SiC Schottky barrier diodes (SBDs). Similar experiments on SiC PN diodes have been reported recently [1, 2]. In this study we construct a detailed map of defects on a test wafer using SWBXT and EBIC, observe the electrical behavior of small diodes that are either defect free or contain a known defect, and determine the correlation between the observed electrical behavior and the presence of defects within the device. The study is conducted on a 50 mm diameter n-type 4H-SiC substrate with a 10 μm n-type epilayer doped 1×10^{16} cm^{-3} with nitrogen. Individual die 2 mm square are defined by RIE. Each wafer is then mapped using SWBXT and EBIC, and SBDs ranging in diameter from 30 – 200 μm are fabricated within each die. Edge termination is formed by implanting 1×10^{15} cm^{-2} boron atoms at 30 keV in 30 μm rings surrounding each diode. The implants are activated at 1050°C to remove lattice damage without activating the dopants [3]. Nickel Schottky contacts are deposited by E-beam evaporation and patterned by liftoff.

I-V measurements, shown in Figure 1, indicate a barrier height of 1.4 eV, an ideality factor of 1.1, and a typical breakdown voltage of over 1400 V. Leakage measurements on 200 devices reveal 158 diodes with nearly identical leakage characteristics, similar to those previously reported [4]. The other 42 diodes exhibit excessive reverse bias leakage, as illustrated in Figure 2.

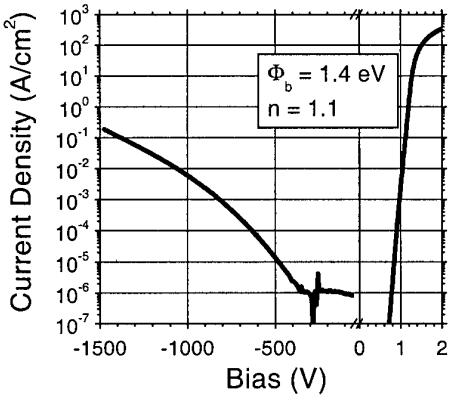


Figure 1: Forward and reverse bias I-V characteristics of nickel 4H-SiC Schottky barrier diodes

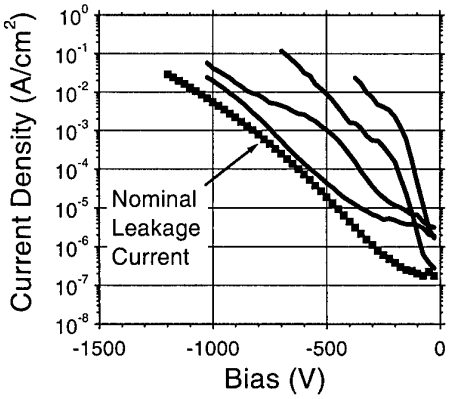
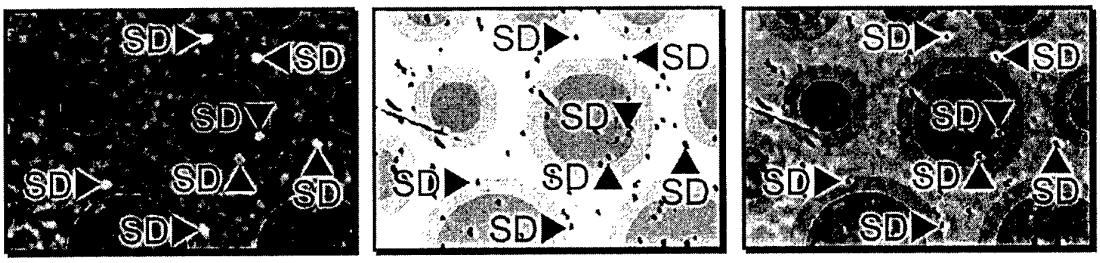


Figure 2: Comparison of reverse bias leakage current density

Examples of the obtained SWBXT and EBIC images are shown in Figure 3, including an overlay of the two images. As was demonstrated by Schnabel, *et al.* [5], each screw dislocation (SD) identified in the SWBXT images correlates to a unique recombination center (RC) visible in the corresponding EBIC image. The images are used to collect defect concentration statistics and to determine the location of each defect relative to the 200 sample diodes.



(a) (b) (c)

Figure 3: (a) SWBXT image, (b) EBIC image, (c) SWBXT / EBIC image overlay, indicating the location of screw dislocations (SDs) and other recombination centers (RCs) relative to several diodes.
Note that each SD corresponds to a RC, but not all RCs are due to SDs.

The average screw dislocation (SD) density identified by SWBXT is 4,096 cm^{-2} and the EBIC defect density is 29,400 cm^{-2}. Of 200 diodes, 59% contain SD's and 98% contain EBIC defects. Diodes are classified as 1) defect free, 2) SD in diode area, 3) SD in edge termination ring, 4) EBIC defect in diode area, and 5) EBIC defect in termination ring. The collected statistics are summarized in Table 1.

	% Bad Devices with Defect	% Good Devices with Defect
Screw Dislocations	**60%**	**58%**
Active Area	19%	19%
Edge Termination	52%	51%
Boundary	26%	27%
Recombination Centers	**98%**	**97%**
Active Area	71%	61%
Edge Termination	98%	96%
Boundary	86%	75%

Table 1: Probability of finding SDs and RCs in or near diodes with good or bad leakage characteristics

Surprisingly, to within statistical error, the probability of finding a good device is the same for each category, indicating there is no correlation between SD's or EBIC defects and excessive leakage characteristics. In fact, 58% of the 158 well-behaved diodes contain SD's and 97% contain EBIC defects, while 40% of the diodes with excessive leakage current are completely free of SD's. This unexpected result suggests that, unlike SiC PN diodes [1,2], the reverse leakage current in SiC SBDs is not dominated by either SD's or EBIC defects. While these defects may impact device performance in other ways, they do not appear to prevent the manufacture of high-voltage low-leakage SiC SBDs. A more detailed discussion of these results will be presented at the conference.

Acknowledgements: We thank P. G. Neudeck and S. G. Bailey, NASA Glenn Research Center, for assistance with processing, EBIC imaging, and for helpful conversations, and M. Dudley of SUNY Stony Brook for SWBXT imaging. This work is supported by ONR/MURI grant No. N00014-95-1-1302.

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Electrical Properties and Interface Reaction of Annealed Cu/4H-SiC Schottky Rectifiers

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Nowadays, high-blocking voltage 4H-SiC Schottky rectifiers have been demonstrated. To realize stable electrical properties under high-power and high-temperature operations for a Schottky rectifier, it is important to form a reliable metal contact. Copper (Cu) is one of the expecting materials because of its low resistivity and high thermal conductivity. Our group has reported the electrical properties of Cu/6H-SiC junctions [1]. In this paper, the relation between stability of electrical properties and chemical reactions at Cu/4H-SiC Schottky interface by thermal annealing was revealed for the first time.

An n-type 4H-SiC homoepitaxial layer with a 10 μ m thick and a donor concentration of 1.0 $\sim 1.4\times10^{16}$cm^{-3} grown on (0001) Si-face substrates were used. An ohmic contact on the back of substrate was employed by the deposition of nickel and annealed in N_2 ambient at 1000℃. Copper contacts were deposited by the RF sputtering method at room temperature. Diameter and thickness of copper contacts were 200 μ m and 200nm, respectively. To analyze effects of thermal annealing, an as-deposited Cu/4H-SiC junction was treated in N_2 ambient at 300～700℃ for 5 minutes.

Figure 1 shows current density-voltage characteristics at room temperature for typical Cu/4H-SiC Schottky rectifiers, which had good Schottky properties. After thermal annealing at 300℃, the barrier height (ϕ_B) and ideality factor (n) was slightly increased, and the reverse leakage current could be successfully reduced. The fluctuation of electrical properties under the continuous forward bias condition is shown in Fig.2. Solid and dashed lines correspond to the as-deposited and annealed Cu/4H-SiC Schottky rectifiers, respectively. With the constant forward current at 0.125A (400A/cm^2) for 1 minute, the barrier height and ideality factor of the as-deposited Cu/4H-SiC Schottky rectifier changed especially at the beginning. On the other hand, the electrical properties of annealed Cu/4H-SiC Schottky rectifiers were very stable for a long-time operation over 50 minutes. A suitable thermal annealing for a Schottky contact is very useful to improve reliability and stability in the Cu/4H-SiC electrical properties.

To discuss the electrical properties of Cu/4H-SiC Schottky contact in more detail, annealing temperature dependence of barrier height and ideality factor is studied (Fig.3). Annealing at 500℃ was found to improve the Schottky barrier height, *i.e.* the barrier height increased up to about 1.75eV, and the ideality factor was kept below 1.1. The barrier height of Cu/4H-SiC could be controlled by annealing temperature. With the increase of annealing temperature over 500℃, however, Cu/4H-SiC Schottky properties became poor : Barrier heights decreased to around 1.6eV, and ideality factor increased over 1.3. Chemical bonding structures at a Cu/4H-SiC interface were analyzed by X-ray photoelectron spectroscope (XPS) measurement, as shown in Fig.4. The reduction of Si*2p* binding energy and the

increase of Si2*p* photoelectron intensity were observed at annealing temperature over 300℃. It is considered that bonding structures of silicon atoms near the Cu/4H-SiC interface will change by the annealing, leading to the formation of stable Schottky junction and the increase of barrier height. With the increase of annealing temperature over 500℃, however, the Cu2*p* binding energy was increased. Copper near the interface chemically reacts with the silicon by the annealing, *i.e.* degradation of Schottky properties is caused by the formation of copper silicide at the Cu/4H-SiC interface.

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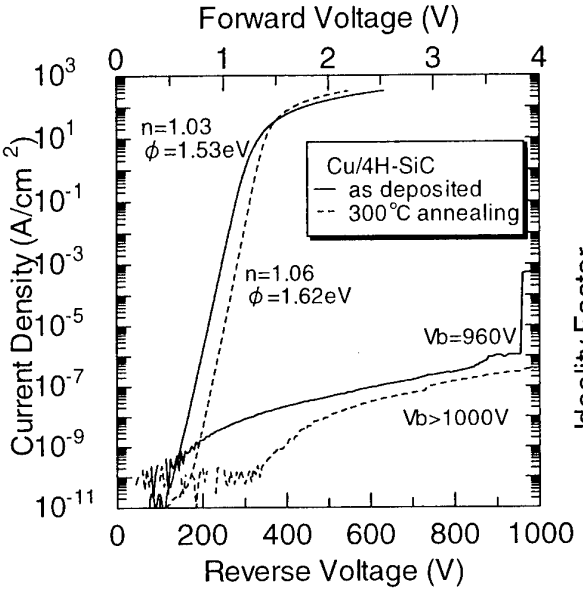


Fig.1 Current density-voltage charactoristics for Cu/4H-SiC Schottky rectifiers. Solid and dashed lines coresspond to as- deposited and 300℃ annealed Cu contacts, respectively.

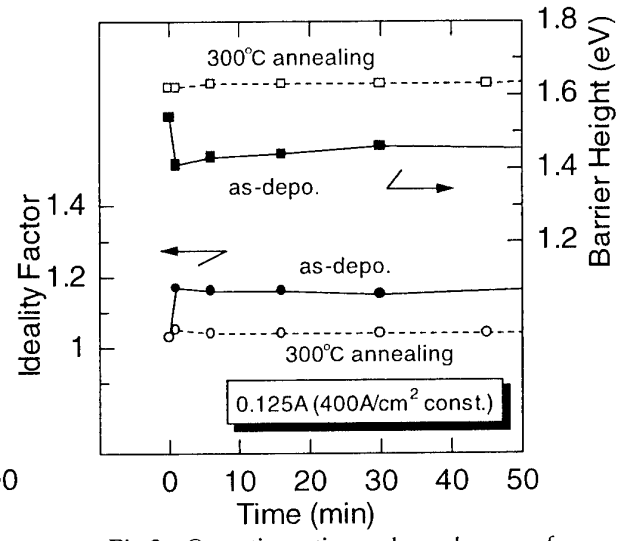


Fig.2 Operation time dependence of ideality factor and barrier height under the forward bias condition at 0.125A (400A/cm^2).

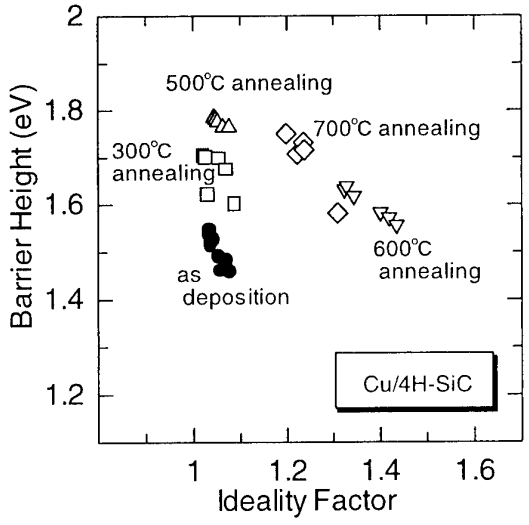


Fig.3 Annealing temperature dependence of barrier height and ideality factor for Cu/4H-SiC Schottky rectifiers.

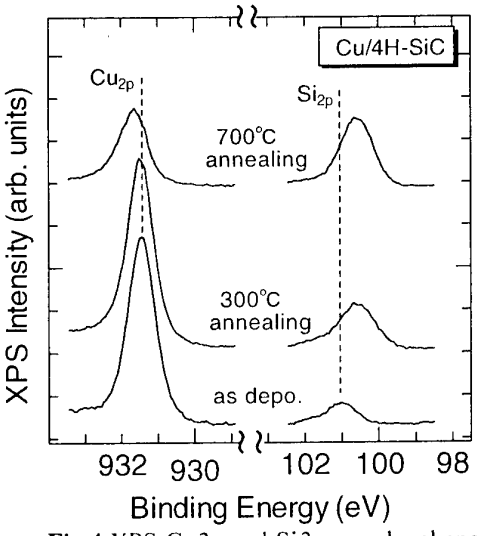


Fig.4 XPS Cu2*p* and Si2*p* core level spectra from as-deposited, 300℃, 700℃ annealed Cu/4H-SiC interfaces.

Microstructural Interpretation of Ni Ohmic Contact on n-type 4H-SiC

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Ni-based metals have attracted many attentions as an ohmic contact for n-type SiC due to their low contact resistivity. The ohmic contact formation was thought to be due to the formation of Ni_2Si phase, even the Ni_2Si were formed at temperature of as low as 600 °C.[1] Thus, ohmic contact formation mechanism of Ni remains still unclear. In this work, the microstructure and electrical properties of Ni contact were studied. From these, the origin of ohmic contact formation for Ni contact on n-type SiC is proposed.

The changes for both Schottky barrier height (SBH) and ideality factor as a function of annealing temperature are shown in Fig. 1. The SBH was 1.55 eV for as-deposited Ni contact and it increased to 1.78 eV at 600 °C. When the Ni contact was annealed at 1000 °C, ohmic contact, corresponding to the *SBH* of 0.38 eV, was formed.

Figure 2 exhibits XRD profiles of the Ni contact with annealing temperature. After annealing at 600 °C, most of Ni film was transformed to nickel silicides composed of δ-Ni_2Si and $Ni_{31}Si_{12}$. After annealing at 950 °C, peaks corresponding to NiSi and graphite (002) were newly detected. These suggest that the formation of ohmic contact on n-type SiC is not due to the formation of Ni_2Si, because the ohmic contact formation temperature (>900 °C) was far from the Ni_2Si formation one (~600 °C).

Figure 3 (a) shows the XTEM micrograph of the Ni contact on n-type SiC annealed at 950 °C and, (b) and (c) show the micro diffraction patterns at the position, marked as "1" and "2", respectively. The pattern recorded near the contact, marked as "1", was indexed as NiSi and the pattern marked as "2" was indexed as δ-Ni_2Si phase, suggesting that the composition of Si in nickel silicide forming at the interface increases with annealing temperature.

The effect of elemental diffusion on the change of electrical properties was investigated by XPS with depth for Si 2*p*, C 1*s* and Ni 2*p* at 950 °C, shown in Fig. 4. An abundance of C atoms outdiffused through the Ni silicide and accumulated at the surface.

This suggests that the predominant outdiffusion of C atoms is closely related to the formation of ohmic contact.

In SiC, V_C act as donors for electrons and Si vacancies, V_{Si}, as acceptor. The ionization energy level of V_C is located at 0.5 eV [2] under the conduction band edge, but V_{Si} is at 0.45 eV [3] above the valence band one. A number of V_C was generated due to the outdiffusion of carbon atoms when the Ni contact was annealed at 950 °C. This causes net concentration of electrons to increase under the contact because of role of V_C acting as donors. Thus, the depletion layer width and effective tunneling barrier height for the transport of electrons are simultaneously decreased, leading to the reduction of contact resistivity.

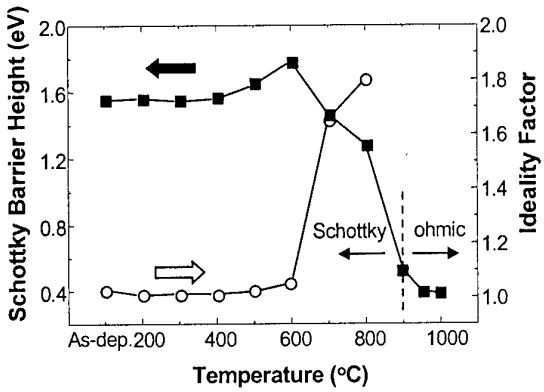


Fig.1 Schottky barrier height and ideality factor as a function of annealing temperature

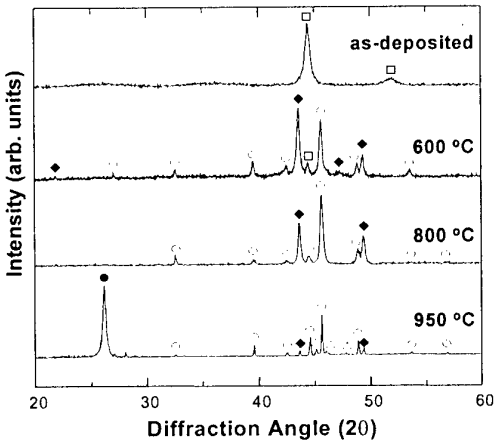


Fig. 2. Change of synchrotron X-ray diffraction pattern with annealing temperature; (□) Ni, (◆) $Ni_{31}Si_{12}$, (○) δ-Ni_2Si, (△) η-NiSi, (●)graphite.

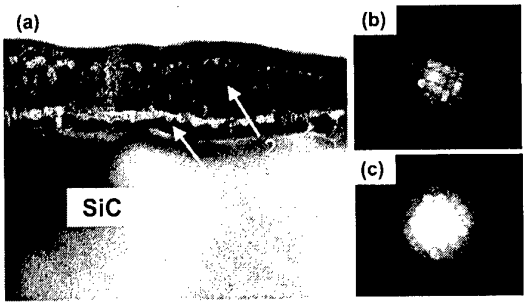


Fig.3. (a) XTEM micrograph of Ni/SiC annealed at 950 °C; micro-diffraction patterns in areas marked (b) "1" and (c) "2".

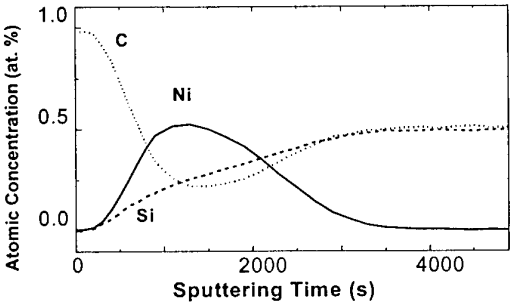


Fig. 4. XPS depth profiles of Ni, Si and C atoms for Ni contact on n-type SiC at 950 °C.

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Acknowledgment:

This work was performed through the project for "National Research Laboratory" sponsored by the Korea Institute of Science and Technology Evaluation and Planning (KISTEP).

Reduction of the barrier height and enhancement of tunneling current of titanium contacts using embedded Au nano-particles on 4H- and 6H-Silicon carbide

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Ohmic contacts are difficult to achieve on SiC due to the high Schottky barrier height. For conventional Ohmic contacts, a reduction of tunneling barrier height is attained by doping the semiconductor near the surface to degenerate levels even with surface Fermi level pinning. In this work, we demonstrate a new approach for the manufacturing of Schottky contacts to n-type 4H- and 6H-SiC as well as Ohmic contacts to p-type 4H-SiC using Ti with embedded Au nano-particles on SiC based on a previous approach in a study of electron transport at the Au/InP interface [1].

The Schottky and Ohmic contacts were formed by first depositing Au aerosol particles with a diameter of 20 nm and with a density of 90~100 μm^{-2}, see Fig.1, on the SiC surface [2]. Subsequently, Ti (2000 Å) was evaporated onto the sample. The reason for selecting Au and Ti is that they have a large barrier height difference ($\Phi_{bn,\,Au} \approx 1.75$ eV and $\Phi_{bn,\,Ti} \approx 1.12$ eV). Control samples (particle-free Ti and Au, 2000 Å) were also fabricated as reference, for the Schottky contact study. Fig. 2 shows the I-V curves for Ti with embedded Au nano-particles, particle-free Ti, and Au Schottky contacts on n-type 4H-SiC as a function of the measurement temperature. From our I-V measurements, the Schottky barrier height (SBH) for Ti with embedded Au nano-particles on SiC was 0.19 eV (4H-SiC) and 0.15 eV (6H-SiC) lower than the control Ti Schottky contacts with the ideality factor of almost unity (1.04 ± 0.03, 4H-SiC and 1.20 ± 0.13, 6H-SiC) in the temperature range of 25-300°C. It is also clear that thermionic emission is dominant.

In order to understand this reduction of the SBH for Ti with embedded Au nano-particles Schottky contacts to SiC, it has been proposed that SBH lowering is caused by an enhanced electric field due to the small size of the Au nano-particles and the large SBH difference. According to Tung's dipole-layer approach of the potential and the electronic transport at metal-semiconductor interfaces, the potential distribution for circular patch geometry at MS (metal-semiconductor) interfaces is given by [3]

$$V(0,0,z) = V_{bi}\left(1-\frac{z}{W}\right)^2 + V_a + V_n - \Delta\phi_{Ti\text{-}Au}\left(1-\frac{z}{\left(z^2+R_0^2\right)^{\frac{1}{2}}}\right) \quad (1)$$

Eq. (1) suggests that the electric field at the MS interface depends on the size of the nano-particle (R_0) and SBH difference ($\Delta\phi_{Ti\text{-}Au}$) between Ti and Au metals. According to the Eq. (1), the conduction band potential for Ti embedded Au nano-particles on n-type SiC shows there is no pinch-off, indicating no electrical shielding of Au nano-particles. In forward bias, the small barrier height Ti Schottky contact conducts current dominantly for Ti with embedded Au nano-particles as shown in Fig. 2. Due to the small size of the nano-particles and large difference of SBH, the electric field is increased at the interface. As a result, the image force lowering effect of the SBH would be more significant than usual (up to ≈ 0.10 eV if $E \approx 0.068\times10^7$ V/cm, see Fig. 3). Other authors have simulated even higher fields, $\approx 3\times10^7$ V/cm in Si [4]. This theoretical calculation is in reasonable agreement with our experimental results (0.19, 0.15 eV for 4H- and 6H-SiC, respectively). However, an extended study is needed for a more solid explanation.

We have also tested these contacts on highly doped p-type SiC material. As shown in Fig. 4, the total resistance between two TLM pads (transfer length method), spaced 5 μm apart shows that Ti with embedded Au has a lower contact resistance than that of control Ti Ohmic contacts on p-type 4H-SiC. Similarly, we also explain the reduction of the Ohmic contact resistance by the enhancement of the electric field at the MS interface, which makes the SBH thinner. This has only been shown previously on silicon [4].

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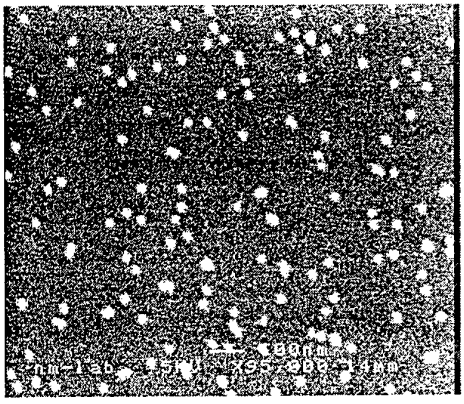


Fig. 1 SEM view of Au nano-particles (20 nm in diameter, 90 μm^{-2} in density).

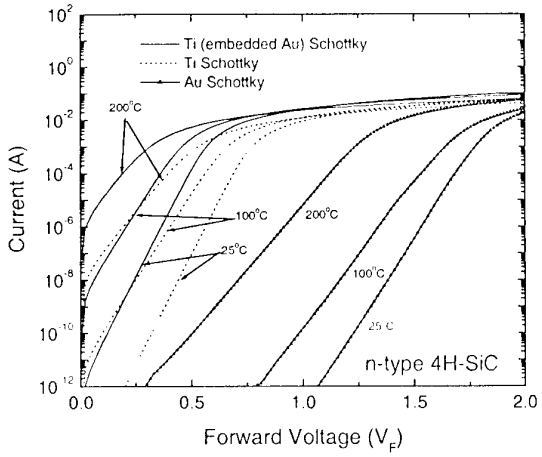


Fig. 2 I-V characteristics of Ti with embedded Au, particle-free Ti, and Au Schottky diodes to n-type 4H-SiC as a function of the measurement temperature.

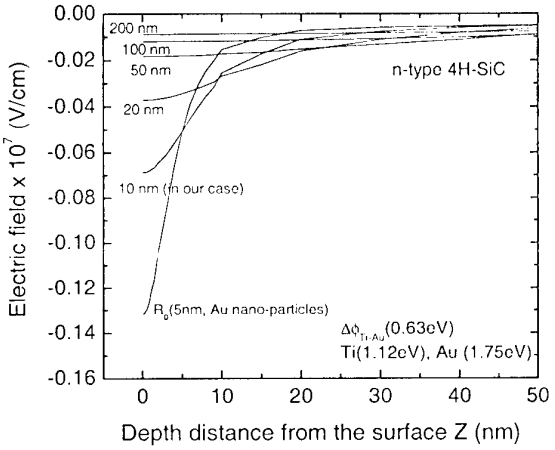


Fig. 3 Calculated electric field distribution at the MS interface using a dipole-layer approach for Ti with embedded Au Schottky diode and different radius of Au nano-particles.

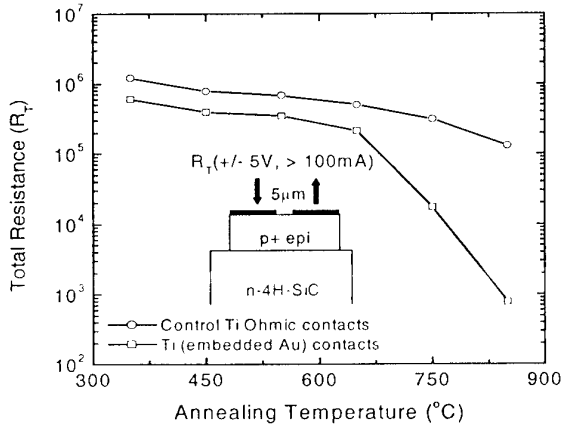


Fig.4 Comparison of the total resistance between Ti with embedded Au and particle-free Ti Ohmic contacts to highly doped p-type 4H-SiC.

A study on the reactive ion etching of SiC single crystals using inductively coupled plasma of NF_3-based gas mixtures

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The inductively coupled plasma reactive ion etching (ICP-RIE) of SiC single crystals using the NF_3 gas mixture was investigated. Mesa profiles were studied as a function of substrate bias power (25~100W), ICP coil power (700~1000W), chamber pressure (4~10mtorr), percentages of O_2 (0~40%), and the distance between the substrate holder and the source coil.

Figure 1 shows ICP-RIE characteristics of 4H-SiC mesas as a function of various process parameters. It is observed that the etch rate increases as the ICP power (Fig 1a) and the bias power increase (Fig 1b). The etch rate decreases as the sample-coil distance (Fig 1e), O_2 % (Fig 1c), and pressure (Fig 1d) are increased. Smooth surfaces (roughness $\leq$ ~1.5nm) and vertical sidewalls (about 85°) were maintained throughout the experiments.

Mesas with vertical sidewalls and smooth surfaces were obtained at the low bias conditions (Fig 2a), with the etch rate of up to 300nm/min, roughness of about 1nm, and verticality 85 °. Higher etch rates could be obtained in the case of high bias conditions (>~300V), although severe mask damage was observed (Fig. 2b).

Investigation on the effects of addition of various gases to the NF_3 mixture on the mesa profile is in progress and the results will be discussed during the presentation.

This work was performed as a part of the SiC Device Development Program (SICDDP) supported by the MOCIE (Ministry of Commerce, Industry and Energy), Korea.

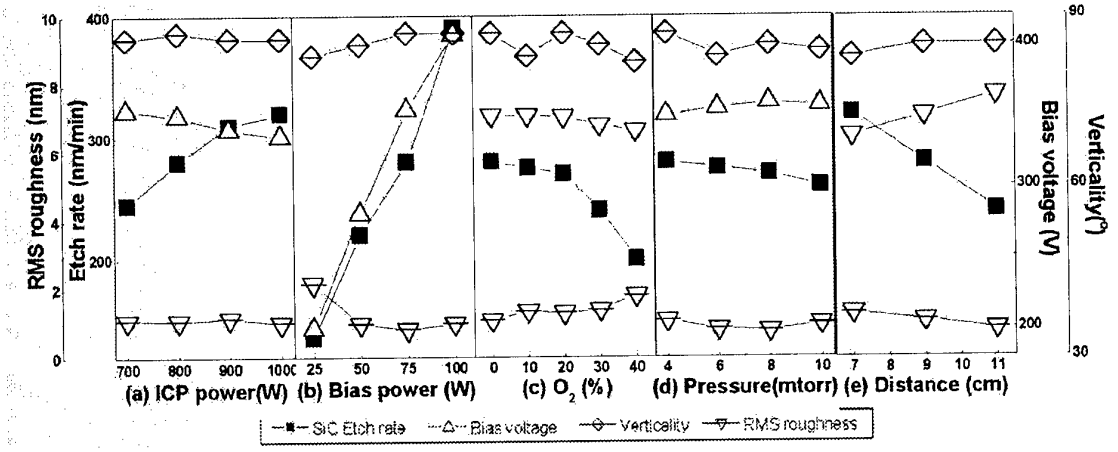
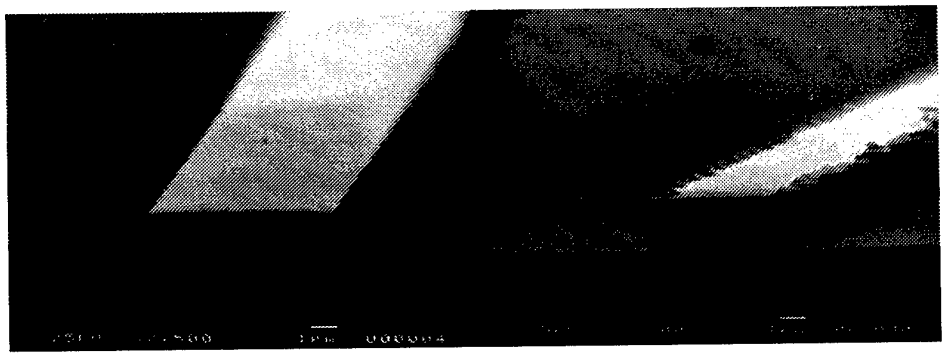


Fig. 1. Etch characteristics of 4H-SiC as a function of (a) ICP source power, (b) b ias power, (c) O_2 % within NF_3-based gas, (d) pressure, and (e) sample-coil distance



(a) (b)

Fig. 2. Cross-sectional SEM micrographs of the SiC mesas etched at the conditions of (a) 800W_50W(280V)_4mTorr_9cm-10 min and (b) 900W_100W(410V)_ 4mTorr_Ar30%-3cm-10min,

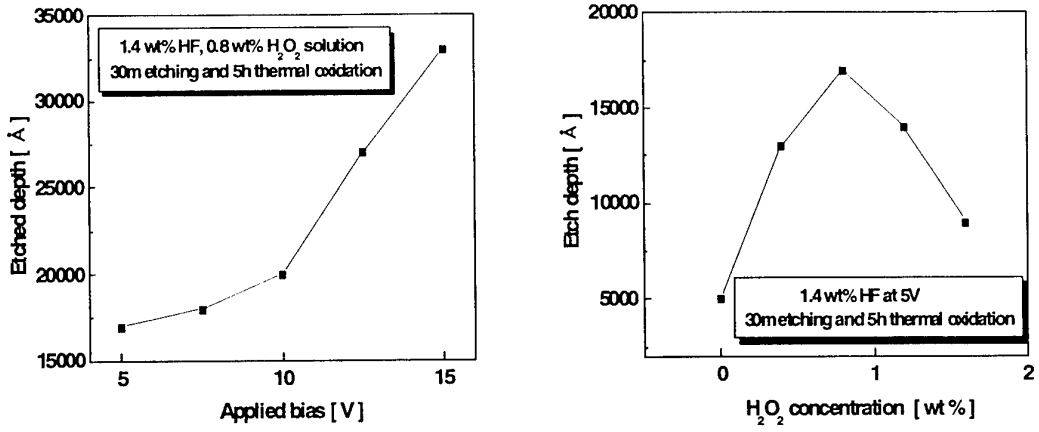
Photoelectrochemical Etching Process of 6H-SiC wafers Using HF-based Solution and H_2O_2 Solution as Electrolytes

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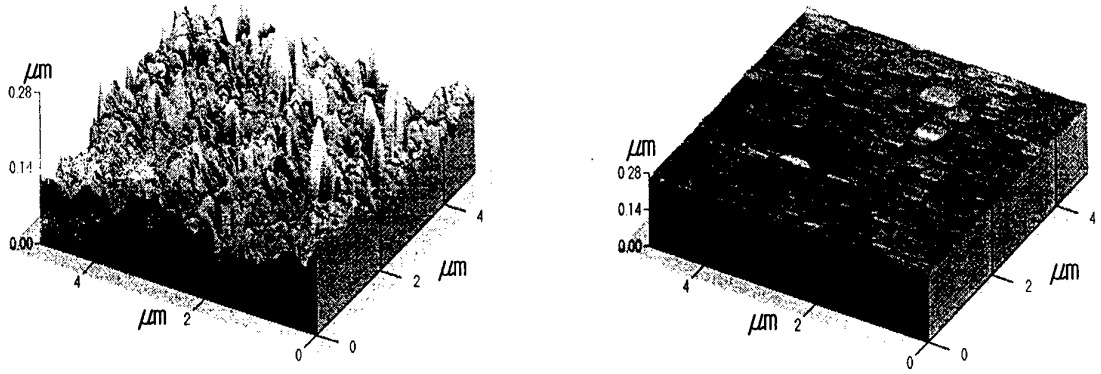
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Dry etching methods which are commonly used for the fabrication of SiC devices are known to result in ion-induced damage on the etched surface, which is highly undesirable for the high frequency and high power device operation. In this paper, we report on the photoelectrochemical (PEC) wet etching process of 6H-SiC using several electrolytes including HF-based solution, H_2O_2 solution and a mixture of HF and H_2O_2. The etching process using the HF-based solution consists of formation of porous layer on the surface of sample and thermal oxidation followed by HF dipping process to eliminate the porous layers. It is believed that the high density of pores was resulted from the reaction between oxygen and carbon. It was confirmed from the EDS analysis that most of carbon atoms were eliminated from the surface of SiC after the PEC etching, which indicates that the surface carbon was used for the formation of CO_2 or CO. An etching rate of 760 Å/min was obtained using a dilute HF (1.4 wt % in H_2O) electrolyte with the etching potential of 3.5 V. When H_2O_2 was employed as an electrolyte, an oxide layer was formed on the surface of the sample without a formation of porous layer. The formation of the oxide layer was almost linearly increased with the etching time. The thickness of oxide is about 11500 Å for the etching time of 90 min.(H_2O_2 : H_2O = 1: 210, without HF, applied bias = 2 V). The etching rate and the surface roughness were changed with the variation of etching potential and the amount of H_2O_2 into the HF electrolyte. The etching rate is increased with the applied bias in a range between 5 V and 15 V for an electrolyte with 1.4 wt % of HF and 0.8 wt % of H_2O_2 (Figure 1(a)). The etching rate is shown to be increased as the concentration of H_2O_2 is increased, but to be decreased after the concentration exceeds 0.8 wt %. The surface roughness was significantly improved when the sample was etched using the H_2O_2 without any HF in the electrolyte ; RMS roughness of about 200 Å when etched in the electrolyte with HF and 27 Å in the electrolyte with H_2O_2 only (Figure 2).



(a) (b)

Fig. 1 Effect of applied etching potential on the etching depth for an electrolyte mixed with HF (1.4 wt %) and H_2O_2 (0.8 wt %) depth (a) and the effect of the concentration of H_2O_2 on the etching depth (etching potential of 5 V).



(a) (b)

Fig. 2 AFM of surfaces of samples after PEC etching using ; (a) HF-based solution as an electrolyte and (b) H_2O_2 as an electrolyte. The RMS roughness of the samples are 200 Å (a) and 27 Å (b), respectively.

ACKNOWLEDGEMENT

This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea.

Growth of SiC on Si(100) by LPCVD and Patterning of the Grown Layers

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Cubic silicon carbide (3C-SiC) is at present a topic of considerable interest due to its great promise as a material for electronic device applications and microeletromechanical systems (MEMS) in harsh environments, or for biomedical applications [1-5]. Semiconductor materials grown directly on silicon profit by the availability of low-cost large area substrates, their superior thermal conductivity and the possibility to realize a new generation of devices monolithically integrated with silicon microelectronics. Large lattice mismatch and the difference in thermal expansion coefficients cause high residual stress and substrate bending. The stress cannot be completely relaxed by the formation of misfit dislocations. It is important to employ lower growth temperatures in order to improve the quality of the heterostructure and to improve further processing. SiC replaces silicon in MEMS devices and gas-sensors for harsh environments. Due to its high chemical stability which is an advantage of silicon carbide as a material for harsh environments it is difficult to employ standard patterning approaches – wet and even dry (poor mask selectivity) etching. New growth and patterning approaches must be developed to sustain flexibility of the device design. A novel alternative processing approach to bulk micromachining of polycrystalline SiC using Si molds was recently reported [6]. The aim of the present paper is to investigate low-temperature low-pressure CVD growth of SiC on Si(100) and Si(100) with a patterned SiO_2 mask layer for patterning the grown layer without etching SiC itself.

The growth was performed in a standard horizontal infrared-heated LPCVD machine AIX-200 designed by AIXTRON and operated at low pressure (20 to 100 hPa) utilizing the precursors carbon tetrabromide (CBr_4) and monosilane (SiH_4, 2% in H_2) as sources of C and Si, respectively. For more stable operation at high temperatures the heating system has been modified. A 150 W mercury-xenon lamp as a UV-source has been added to the set-up [7]. The growth rate at 940°C was about 0.25 μm/h. Exactly (100) oriented Si substrates with or without patterned SiO_2 mask layer were employed. Our samples were grown with or without UV stimulation. Experiments with varied CBr_4/SiH_4 flow ratios were carried out. A short Si substrate-carbonisation step [1] was added in the experiments at the beginning of the SiC growth process.

The samples obtained were investigated by atomic-force microscopy (AFM), scanning electron microscopy (SEM), photoluminescence (PL), optical microscopy, transmission electron microscopy (TEM) and load-deflection measurements. In this work we concentrated our attention to the fabrication of patterned SiC on Si substrate. The UV stimulation increased the uniformity of the grown surfaces and in most cases decreased their roughness [7].

Optical microscopy and SEM investigations showed mirror-like surfaces of the grown layers. TEM investigations of these samples revealed the transition from amorphous to fine polycrystalline and then to textured 3C-SiC films with variation of the Si/C ratio in the gas phase. We found broad PL peaks around 2.4 eV with FWHM of about 0.44 eV.

The 40-90 nm thick SiC layers were patterned employing a novel lift-off approach with SiO_2 as sacrificial layer. Silicon wafers were oxidised at 1200°C (SiO_2 thickness about 1 μm) and patterned in HF. The subsequent SiC growth was optimised for the lift-off process which was carried out in buffered HF (to lift-off SiC on SiO_2). Finally, the Si was patterned employing etching in 30% KOH using the SiC as mask. A plan-view SEM image of a micro-patterned SiC lateral resonant structure is shown in Fig. 1. The edges of the patterned structure are sharp. For structures oriented along {100} directions undercut was observed. Cracking or fracturing of the undercutted layers was not observed even in the case of a very small radius of bending. The layers obtained reveal exciting mechanical stability.

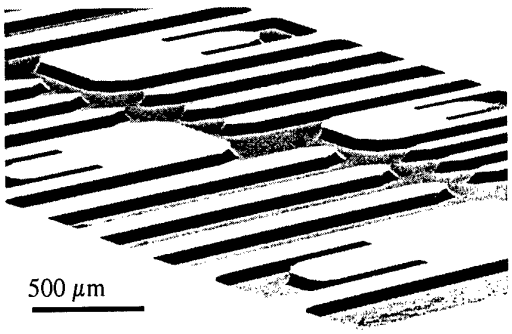


Fig. 1. Plan-view SEM image of a micro-patterned SiC lateral resonant structure grown on Si (100) substrate.

In conclusion, we have developed and described a low-cost approach to 3C-SiC LPCVD growth and patterning. LPCVD with UV stimulation has been developed as a technique for the low-temperature growth of SiC on Si with a patterned SiO_2 mask. Examples of surface micromachined structures patterned by the described lift-off approach are presented. The approach can be used for further pendeo-epitaxial growth or fabrication of micromechanical devices, gas sensors, or biomedical applications.

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ThB3 Epitaxial Growth-Nitride

[redacted]

Sublimation growth of bulk AlN crystals: materials compatibility and crystal quality

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Perspectives of bulk AlN crystal growth are attracting much interest, as AlN wafers would be the nearly ideal substrate for nitride based electronic and optoelectronic devices having small lattice mismatch with GaN, similar coefficient of thermal expansion and high resistivity. Since the pioneering work of Slack and McNelly [1] the problem of chemical compatibility of materials used in the growth cell was recognized as the key issue in bulk AlN growth. To date various crucible materials such as graphite and SiC coated graphite, nitrides (TiN, Ta_2N) and high-melting metals (W, Re and W-Re alloys) have been employed, but AlN samples are polycrystalline, still limited in size and contain much impurities (the latter is evidenced by reported crystal coloration). In this work crystal growth results obtained with the use of different materials in the reactor system are discussed in terms of process stability and crystal quality.

Crystal growth experiments were conducted in a restively heated furnace using graphite or tungsten heating elements in the temperature range 1900-2200°C. The source material was AlN powder (99%, Chempur, Germany, main residual impurity - oxygen). Seed plates 10x10 mm^2 were cut from on axis 6H-SiC crystals grown in our laboratory. The growth process was performed in an atmosphere of pure nitrogen and N_2+H_2 mixtures under the pressures ranging from 30 to 500 mbar. The following material combinations were tested:

N	Crucible	Heater	Isolation
1	Dense graphite	Graphite	Porous graphite
1a	SiC coated graphite	Graphite	Porous graphite
2	Tungsten	Tungsten	Tungsten or/and
2a	Tungsten	Tungsten	AlN and Al_2O_3 ceramics
3	Tungsten	Graphite	Porous graphite

First two arrangements 1 and 1a represent 'standard' high-temperature material combinations: (1): The main challenges with a 'pure graphite ambient' is crucible permeability for aluminum vapor and seed surface graphitization at T>2000°C. However carbon contamination of the crystal can be kept at a relatively low level, if oxygen is carefully removed from the system

prior to growth. In the initial process stage the carbothermic reduction of aluminum oxide film according to the reaction $Al_2O_3+3C+N_2=2AlN+3CO$ is very useful for preparation of an oxygen-free AlN powder charge.
(1a): Contrary to the results of Balkas et al. [2] SiC coating of graphite crucible was found to be unstable at least at T>2000°C. According to our estimations, at elevated temperatures, vapor pressures of SiC species are only slightly lower, than that of AlN, leading to growth of mixed AlN-SiC crystals. AlN-SiC alloys are interesting as substrates for MBE growth of AlN, and also exhibit useful semiconductor properties. However, the combination of 1a can not be considered as a promising way to grow semiconductor grade AlN.

A 'pure tungsten ambient' (2 and 2a) includes two other challenges. First of all W can be strongly attacked by aluminum vapor not only at high-temperatures, but also at a temperatures below 1000°C by aluminum melt droplets, if partial decomposition of AlN occurs during pre-heating of the furnace in vacuum. The life time of tungsten heaters is relatively short. We have found that W-heater stability can be sufficiently improved by a precise furnace design, but the need in further corrections undoubtedly remains. Secondly, in a tungsten furnace it is very difficult to get rid of inevitable oxygen contamination of AlN charge. Purging with N_2+H_2 mixture at 1000-1200°C is really effective only for day-long reaction times. Seeded growth is often complicated by formation of oxynitrides in the initial stage of growth.
The combination of a W-crucible and a graphite heater (3) offers important advantages, such as long heater life time, effective use of heating power and flexible cell design. A critical issue arising here is the probability of crucible damage because of WC formation on the outer surface. However it was found, that in the absence of direct contact of tungsten with graphite parts, the crucible erosion is mainly determined by the action of AlN and not by carbon. Formation of oxynitrides was not observed.

Finally, results on morphology and purity of the grown AlN crystals and layers are presented and discussed. The growth of AlN-SiC mixed crystals is described in terms of process conditions and crystallization parameters.

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Crystal growth of aluminum nitride by sublimation close space technique

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Introduction

Silicon carbide (SiC) and III-nitride like gallium nitride (GaN) and aluminum nitride (AlN) is the most promising semiconductor materials with applications to high frequency, power and temperature devises, because these semiconductors have a wide gap, a high carrier mobility, etc. In order to create such devises, high quality semiconductor substrates and layers are needed. Besides, there are many polytypes in SiC and it is known that 2H-SiC has the widest gap in SiC polytypes. In order to obtain 2H-SiC crystal, substrates that have 2H polytype and a small lattice miss match are needed. 2H-AlN is the most suitable substrate in order to grow 2H-SiC. In this background, we tried to grow AlN layers.

Heteroepitaxial growth of 2H-AlN on 6H-SiC was carried out by sublimation close space technique (SCST) [1,2] in order to obtain high quality AlN layers with a high growth rate. SCST was used in the crystal growth of SiC epitaxial layer with a high growth rate and high quality [1,2]. Besides, in the crystal growth of III-nitride compound, ammonia (NH_3) is generally used as a source of nitrogen (N). In this study, nitrogen gas (N_2) was used as a source of N.

Experiment

Crystal growth was carried out by SCST. In order to grow AlN, aluminum carbide (Al_4C_3) powder was used as a source material of Al and crystal growth was carried out in N_2 atmosphere. The growth temperature was 1900°C and the growth pressure was 1 atm. The distance between the source and the substrate was 1.0mm. 6H-SiC (0001) Si-face and (0001) 5° off oriented toward $<11\bar{2}0>$ were used as substrates. These substrates were prepared in our laboratory. The substrate and the source material were set in a graphite crucible. In order to absorb carbon from Al_4C_3 and the crucible, tantalum (Ta) plate was used. This crucible was heated by RF-generator at a frequency of 36.2 kHz. At these conditions, the growth rate was about 10μm/h.

Result and discussion

Fig.1 shows the Raman spectrum of the grown layer. The substrate which had the off axis-angle was used and the film thickness of this layer was 10μm. Two peaks, SiC and AlN, are observed. This is due to the fact of that this layer is not enough thick. However, it is confirmative that this grown layer is AlN [3].

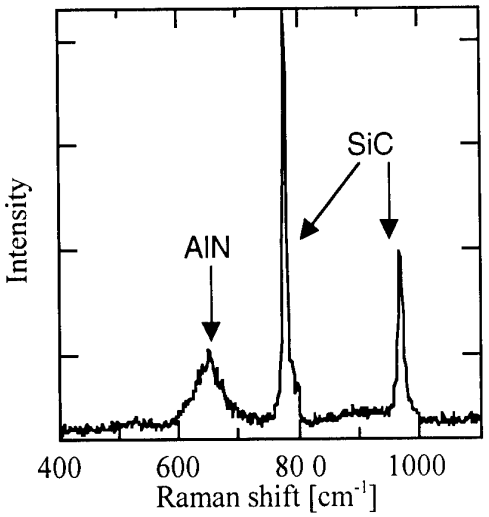


Fig. 1 Raman spectrum of grown layer

Fig. 2 shows a surface morphology of the grown layers by an optical microscope. This layer was grown on the substrate that had the off-axis angle. Because step like morphology is observed on the surface, it is considerable that crystal growth proceeds in the 2 dimensional growth, in other wards, step-flow growth [4]. When the substrate which has no off axis-angle was used, different surface morphology, hexagonal pattern, was observed. In this case, it is considerable that crystal growth proceeds in the 3 dimensional growth. Additionally, in this case, polycrystalline AlN layers were sometimes grown. Therefore, in order to obtain single crystal AlN layers, crystal growth must proceed in the 2 dimensional growth, in other wards, substrates must have the off-axis angle.

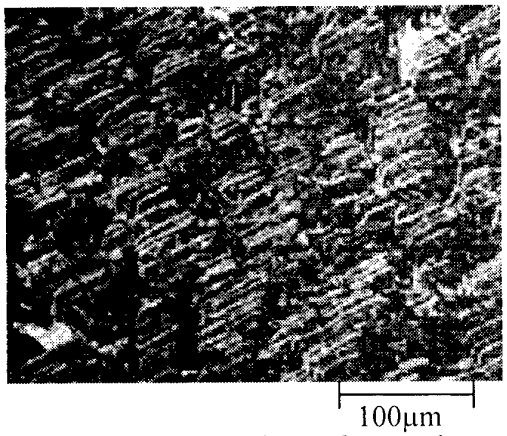


Fig.2 Surface morphology of grown layer

In this study, heteroepitaxial growth of AlN on SiC was carried out by SCST. The growth rate was only 10μm/h. In order to obtain thick layers and bulk crystal, higher growth rate must be obtained. Therefore, the growth condition must be optimized.

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Heteroepitaxial Growth of Insulating AlN on 6H-SiC by MBE

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AlN is expected as an insulator of SiC metal-insulator-semiconductor field effect transistors (MISFETs) due to its high relative dielectric constant (8.5) compared to SiO_2 (3.9). Owing to the small lattice mismatch between AlN and SiC, an AlN layer with low defect density and good structural properties can be obtained. However, there are few reports on high-performance AlN/SiC MIS devices because of large gate leakage current.[1] In order to obtain a high-quality AlN layer on a SiC substrate, a pretreatment of substrate surface is very crucial. We proposed HCl gas etching, which could remove surface polishing scratches and realize an atomically flat terrace structure,[2] as a new pretreatment method of SiC substrate for molecular beam epitaxy (MBE) of III-Ns.[3] As a result, a very flat AlN layer was obtained on an HCl gas etched SiC substrate. In this study, insulating properties of AlN on a 6H-SiC substrate was investigated by a current-voltage (I-V) measurement of Al/AlN/SiC MIS diode structures.

Substrates used in this study are commercially available n-type on-axis 6H-SiC $(0001)_{Si}$ face wafers (off angle < 0.2°). The doping level of substrates is around 1×10^{18} cm^{-3}. Substrates were pretreated by HCl gas etching in a chemical vapor deposition (CVD) system at 1300℃ for 10 min, and transferred through the air into an MBE system. AlN layers were grown at 900℃ by MBE using elemental Al and radio frequency (rf) plasma-excited active nitrogen. Al electrodes (ϕ300 μm) were formed on an AlN surface by vacuum evaporation.

Figure 1 shows insulating properties of 35 nm-thick AlN layers grown on 6H-SiC substrates and AFM images of them. The surface pretreatment of SiC substrate by HCl gas etching strongly influenced the insulating properties of AlN. The AlN layer grown on an HCl gas etched substrate had a very flat surface and exhibited excellent insulating properties. The resistivity of this AlN layer was 6.8×10^{13} Ω·cm. The leakage current was as small as 10^{-8} A/cm^2 below 2.5 MV/cm. This is a considerably hopeful result to apply this AlN for a gate insulator of SiC MISFETs.

Insulating properties of AlN layers grown on HCl gas etched SiC substrates were related to those layer thicknesses as shown in Fig. 2. Thinner AlN layers had more superior insulating properties. A 24.9 nm-thick AlN layer had excellent insulating properties with a small leakage current of 10^{-9} A/cm^2 and a relatively high breakdown field of 4.5 MV/cm. From the result of XRD measurements, thin AlN

layers were well-oriented, while beyond 50 nm, the misorientation of AlN layer gradually increased (i.e. broad peak with the linewidth of 40 arcmin becomes dominant). It indicates strong correlation between insulating properties and structural quality. Employing higher growth temperature or control of initial stage of growth will improve structural quality of AlN layers.

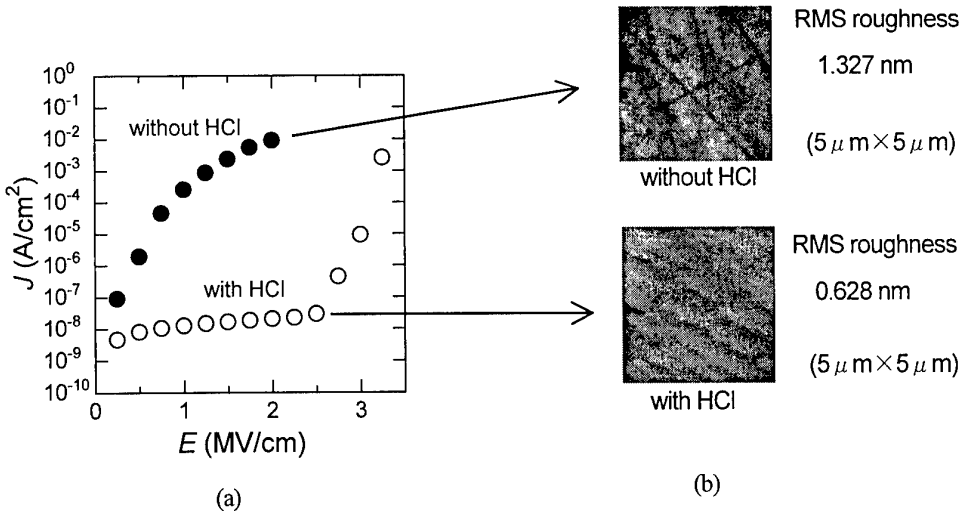


Fig. 1 (a) Insulating properties of AlN layers on 6H-SiC substrates. Thickness of AlN is around 35 nm. Open and close circles are for AlN layers with and without HCl pretreatment. (b) AFM images of those AlN layers.

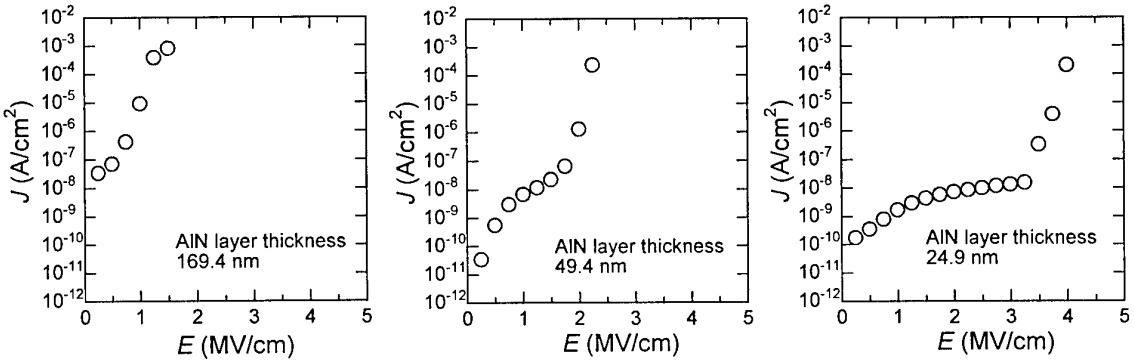


Fig. 2 Layer thickness dependence of insulating properties of AlN layers.

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Structural and Electronic Characterization of Heteroepitaxially grown AlN on Si(111) using surface-reconstruction induced epitaxy

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The multitude of desirable properties of AlN such as its wide bandgap (6.2 eV), high dielectric strength, high temperature stability, high thermal conductivity, chemical inertness, high acoustic velocity, high melting point, and piezoelectric behavior, makes this material suitable for wide range of electronic, optical and mechanical applications. Integration of AlN with Si adds many new dimensions to utilization of AlN. Examples are; integration of optoelectronic components made of direct bandgap group-III nitrides on Si (optical interconnect, LED, Lasers, waveguides), fabrication of solar blind UV and X-ray detectors, as a gate dielectric, and in MEMS. Established Si fabrication technology and the possibility of building the driver circuits on the same wafer provide another impetus for integration.

In this work, AlN was grown on Si(111) using surface reconstruction induced epitaxy. The Si(111)7x7, generated after thermal cleaning of Si, was converted to aluminum induced Si(111)$\sqrt{3}$x$\sqrt{3}$ by depositing ~0.3 ML of Al on the Si(111)7x7 surface at temperatures between 650 to 700 °C. In the $\sqrt{3}$x$\sqrt{3}$ surface configuration, Al passivates all surface Si atoms, minimizing possible interaction between the Si and the overlayer. In this case, it prevents formation of amorphous Si nitride prior to growth of AlN. In addition, the $\sqrt{3}$x$\sqrt{3}$ provides the proper template for hexagonal (001) or cubic AlN growth. The growth was then conducted using thermal Al evaporation from an effusion cell and atomic nitrogen beam from an RF atomic source. Figure 1 shows X-ray

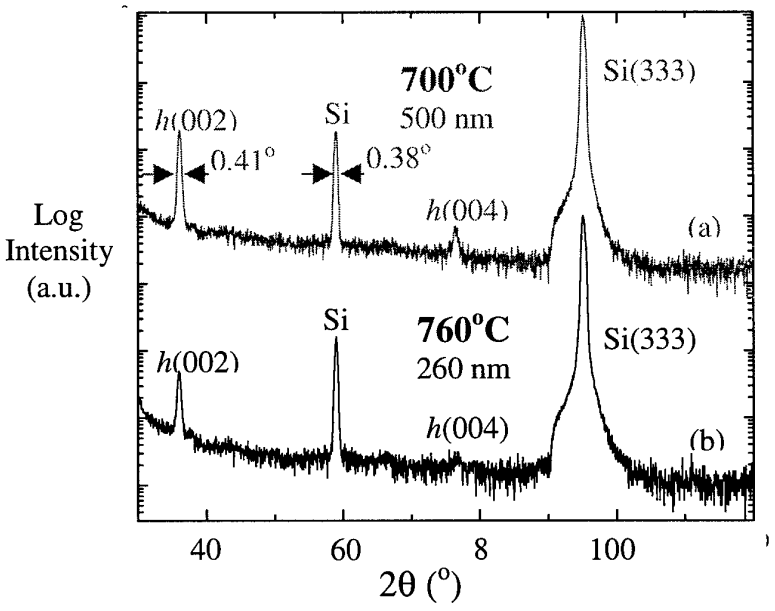


Figure 1. X-ray diffraction from hexagonal AlN(001) grown on Si(111). The FWHM measured from the layer reflection is close to that of the substrate

diffraction from samples gown at 700 and 760 °C. Except for peaks from hexagonal AlN(001) and the Si substrate no measurable intensities can be obtained from other phases or orientations. Moreover, the full width at half maximum (FWHM), measured from the layer peak, is almost equal to that of the substrate (i.e. the resolution of diffractometer) indicating highly oriented AlN layer. Epitaxial growth was achieved over a wide range of Al/N fluxes and growth temperatures extending from ~ 350 to 850 °C. As the growth temperature was lowered and the N/Al flux ratio was increased, a second peak related to cubic AlN(001) became evident indicating growth of a thin interfacial layer of cubic AlN. Figure 2 shows example of an x-ray reciprocal space mapping from an AlN layer grown at 400 °C. The elongation of the cubic peak indicates that the layer is very thin while the FWHM is equal to the resolution of the diffractometer implying a highly ordered epitaxial layer.

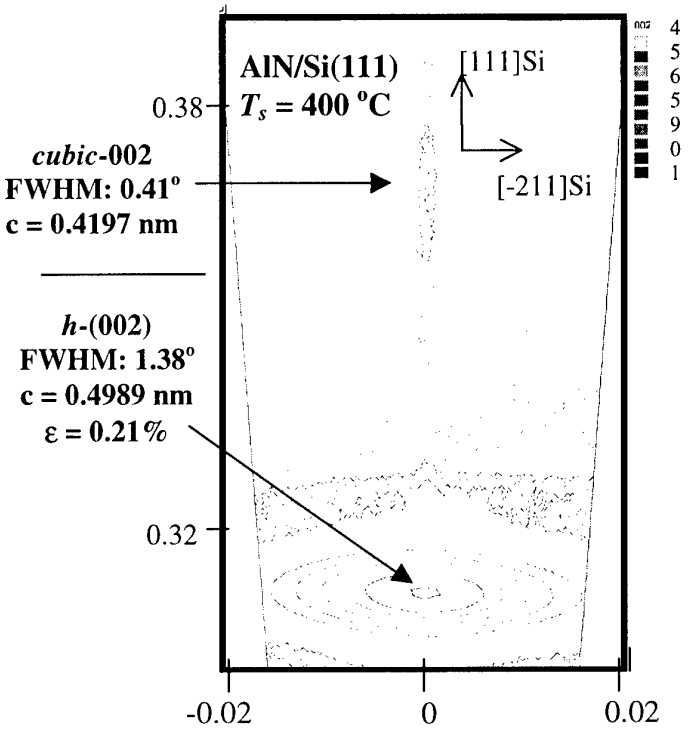


Figure 2. Reciprocal space mapping from AlN layer grown at 400 °C. A strong hexagonal AlN is evident in the map. In addition, a weak, highly oriented cubic-AlN(001) is also present.

Finally, an AlN/Si heterojunction diode was fabricated and tested. A breakdown voltage in excess of 350V was obtained and a leakage current below 100 nA was measured indicating a high quality interface (see Fig. 3).

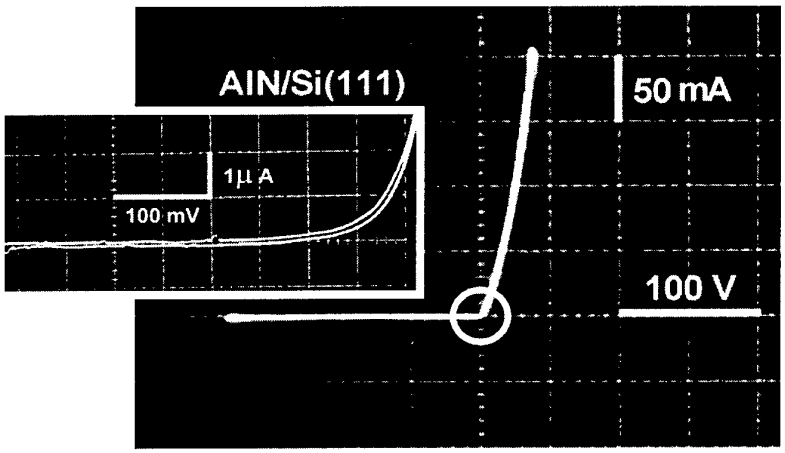


Figure 3. I-V curve from a heterojunction AlN/Si(111) diode showing a breakdown voltage of > 350 V and a leakage current below 100 nA. The breakdown is not shown in the figure.

Acknowledgment: The authors gratefully acknowledge the financial support of the Office of Navel Research (ONR) administered by Dr. Colin Wood and the Defense Advanced Research Project Agency (DARPA) administered by Dr. Daniel Radack. Support from the U.S. Department of Energy (grant DEFG02-96-ER45439) is also appreciated. Special thanks to Mr. John Hudak for an outstanding technical support.

RHEED studies of In effect on the N-polarity GaN surface kinetics modulation in plasma-assisted molecular-beam epitaxy

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III-nitride materials have attracted a great deal of attention due to its potential applications in optical and electronic devices. Recently, positive In effects on the film quality of GaN have been reported by several groups.[1-3] Under the different growth techniques and growth sources, In plays different roles according to the reports. In cases of MOCVD and NH_3-MBE, In works as a doping-effect to improve the GaN film quality. In case of rf-MBE, surfactant effect of In was found to modify the growth kinetics. In addition, lattice-polarity control of III-nitride epitaxial films recently becomes a hot topic due to its great influence on the optical and electrical properties of the films.[4] We found that the stability of GaN surface with Ga-polarity is much superior to that of GaN surface with N-polarity during the interruption of the growth at high temperature in rf-MBE.[5] This phenomenon is especially important to those who need to interrupt the growth to change the growth conditions, such as for the InGaN growth.

In this paper, we reported the In effect on the N-polarity GaN surface kinetics modulation during the interruption of GaN growth under the nitrogen flux in rf-MBE studied by RHEED. The GaN films with N-polarities were grown on sapphire (0001) substrates rf-MBE. Detail of the N-polarity GaN films preparations and the clarifications of the lattice-polarity has been published elsewhere.[6] During the GaN growth, the N_2-plasma power was 350 W and the N_2 flow rate was 5.0 sccm. The growth temperature was fixed at 700℃ and the growth rate was 0.6 μm/hr. In-situ RHEED observations along the [11-20] azimuth during the growth and the growth interruption were carried out and the RHEED images were recorded using a CCD camera. The intensity change of specific RHEED spot/streak was measured from the recorded data using an image processor with a computer.

As a summary, we found that In does have significant effects on the N-polarity GaN surface kinetics modulation in rf-MBE. We proposed a model to explain the phenomena. Based on our model, There are two effects of In on the surface kinetics modulation. First, surfactant effect as

reported was observed which made the rough surface (spotty RHEED pattern) change to smooth surface (streaky RHEED pattern). This effect was also be confirmed by the SEM observation of surface morphologies as shown in Fig. 1. Second, In can suppress the evaporation of Ga atoms from the grown surface, and reduce the reaction between Ga and N, which are the main factors resulting in the surface roughening during the growth interruption. Details will be presented at the conference.

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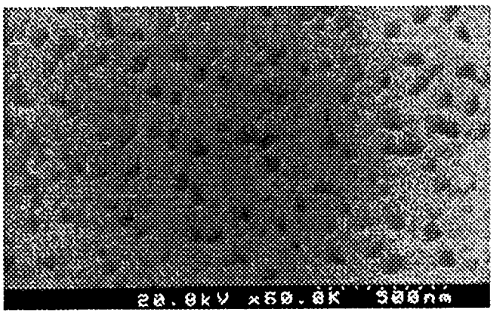
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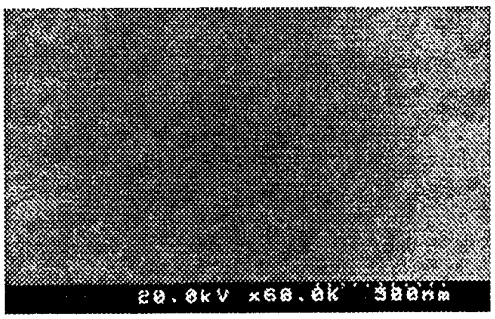
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(a)



(b)

Figure 1. SEM observations of the GaN surface morphologies (a) growth interruption without the In exposure, (b) growth interruption with the In exposure

The Growth of $(SiC)_x(AlN)_{1-x}$ Epitaxial Thin Films on 6H-SiC, by Ion-assisted Dual Magnetron Sputter Deposition

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ABSTRACT

The wide-band gap semiconductor alloy of aluminum nitride (AlN) and silicon carbide (SiC), has become a very interesting material for high-power and optical electronic applications. This alloy can eventually be used for band gap engineering by controlling the ratio of AlN:SiC, such that the band gap can be tailored between 3.0 and 6.2 eV, the band gap values of SiC and AlN, respectively. Attempts to grow $(SiC)_x(AlN)_{1-x}$ alloys or solid solutions have been made for several years by different growth techniques.[1,2] However, the quality of the material still need to be enhanced before it can be used in microelectronic applications as a semiconductor.

In this work, we demonstrate that ion-assisted dual magnetron sputter deposition in ultra-high-vacuum environment is an alternative route to grow a high quality of this material. $(SiC)_x(AlN)_{1-x}$ thin film have been grown on vicinal (3.5°) 6H-SiC substrates at the growth temperature of 1000°C. The sputtering was carried out at the total pressure of 10 mTorr of a pure (99.999999%) gas mixture between nitrogen and argon. An elemental Al-disc and a polycrystalline stochiometric SiC-disc were used as targets for the magnetrons. The alloy films were grown by co-sputtering from both targets. The composition ratio of the alloy was controlled by varying the power of each magnetron.

In-situ reflection high-energy electron diffraction (RHEED) was used to monitor the films during the growth. The cross-sectional microstructure of the alloy films and interfaces were investigated by high-resolution transmission electron microscopy (HREM). As seen in figure 1, the high resolution cross-sectional electron micrograph of the $(SiC)_x(AlN)_{1-x}$ thin film/ SiC substrate interface shows an epitaxial film, which has a hexagonal phase since the beginning of the nucleation. The film has a dense structure with a large domain size, with a domain width of about 30 nm at the base. The quality of the alloy thin films is also reflected in the opto-electronic properties. The preliminary cathodoluminescence (CL) spectrum from one of these semiconductor alloys shows promising results for the band gap tailoring of this alloy with an emission at the energy of 3.40 eV, as illustrated in figure 2. Auger electron spectroscopy (AES) has been used to determine the composition of the alloy thin film for each different growth condition, as well as, the atomic force microscopy (AFM) for characterizing the surface morphology of the films. A detailed discussion about the growth of this alloy will be presented.

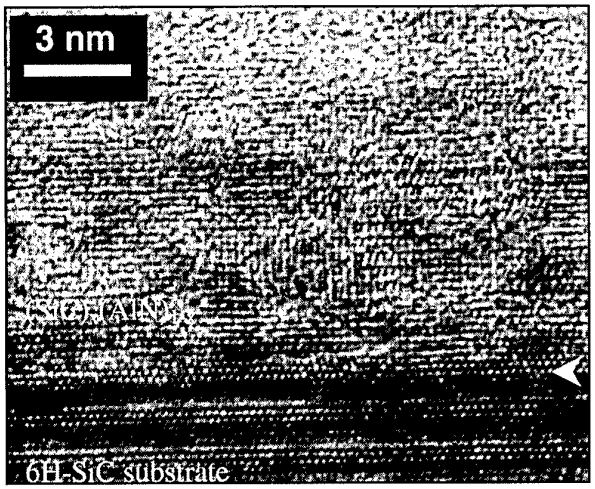


Fig. 1 High resolution electron micrograph of $(SiC)_x(AlN)_{1-x}$ alloy thin film on 6H-SiC, grown by ion-assisted dual magnetron sputter deposition, the arrow indicates the interface between film and substrate.

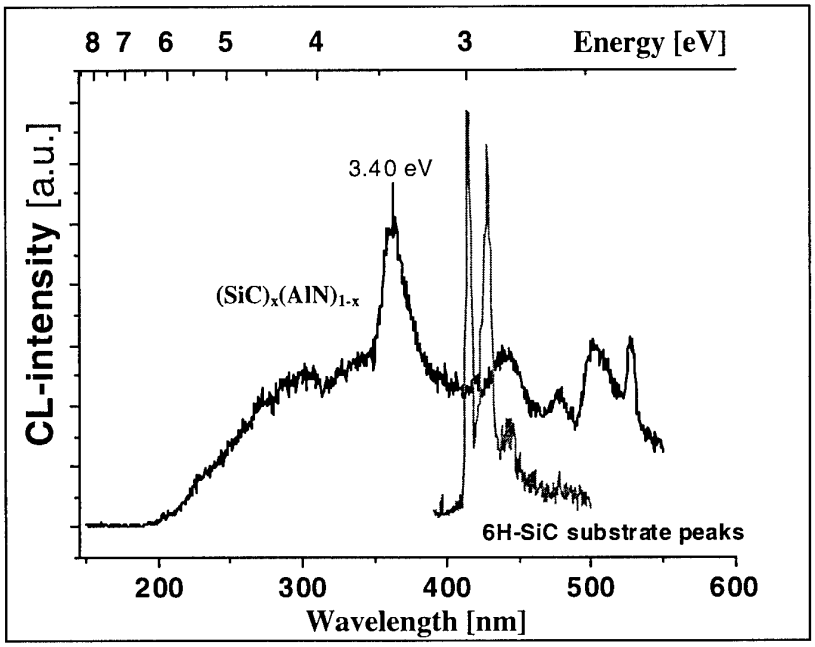


Fig.2 CL spectrum from $(SiC)_x(AlN)_{1-x}$ on 6H-SiC at 5 K, the gray line represented the CL spectrum of 6H-SiC substrate

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Growth and Characterization of GaGdN and AlGdN on SiC by RF-MBE

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In the development of superior electronic devices, the existence of lattice-matched materials and lattice-matched substrates is the most important problem. For example, in the case of GaAs substrate, the lattice-matched AlGaAs or InGaP gives high quality epitaxial films with dislocation densities less than $10^4 cm^{-2}$. For the growth of II-VI compounds on GaAs substrate, the discovery of a lattice-matched ZnMgSSe system improves film quality and the lifetime of the laser diodes [1]. On the other hand, there is no lattice-matched AlGaInN to SiC substrates. The III-nitrides lattice-matched to SiC substrates can be formed by using boron, but it is difficult to use boron in molecular beam epitaxy (MBE) growth. In this report, we will discuss another possible candidate to form a new nitride system. By the addition of Gd to GaN and AlN, GaGdN and AlGdN alloy semiconductors have been obtained, respectively, for the first time.

The films are grown on (0001) SiC substrates by MBE using RF plasma-excited nitrogen. The sample structures are as follows: GaGdN(250nm)/GaN (250nm)/AlN(20nm)/SiC and AlGdN (120nm)/AlN(180nm)/SiC.

After the growth of GaGdN, the RHEED pattern shows a 4x4 reconstruction pattern with some unusual diffraction spots, which may relate to the segregation of Gd atoms but the segregation is not observed in SEM surface observations.

Fig.1 shows the X-ray diffraction pattern for GaGdN. In addition to the diffraction from the SiC substrate and the GaN epitaxial layer, another diffraction peak caused by the GaGdN mixture is observed. The strained lattice constants for the a-axis and the c-axis of GaGdN film estimated from the (11-24) asymmetric XRD pattern are 3.20A and 5.21A, respectively. From the XPS measurement (Fig.2), the composition of Gd and Ga are estimated to be 0.06 and 0.94, which results in the film composition of $Ga_{0.94}Gd_{0.06}N$. From these results, the strained a-axis and c-axis lattice constants for wurtzite structure of GdN are evaluated to be 3.48A and 5.49A, respectively. The crystal structure of GdN is usually a rock-salt structure with a lattice constant of 4.999A [2]. Lattice constants of wurtzite GdN are estimated for the first time.

In the cathodoluminescence (CL) spectrum measured at room temperature (R.T.), band-edge, deep level and Gd^{3+} related emissions are observed, which is shown in Fig.3. The wavelength of the band emission is 370nm and slightly longer than that of GaN (363nm),

which means that bandgap shrinkage by incorporating Gd atoms occurs. The emission peak around 640nm is considered to relate to Gd^{3+} according to the analogy of GaN:Eu [3].

Fig.4 shows the R.T. CL spectrum for AlGdN film. The composition of Gd is estimated to be around 2% by XPS. There are three peaks located at 312, 317, and 322nm and the center peak is dominant. These peaks are probably due to Gd^{3+} but further investigations are needed. A similar spectrum is obtained for AlGdN films with 13% Gd composition but with extra emissions from 350 to 600nm.

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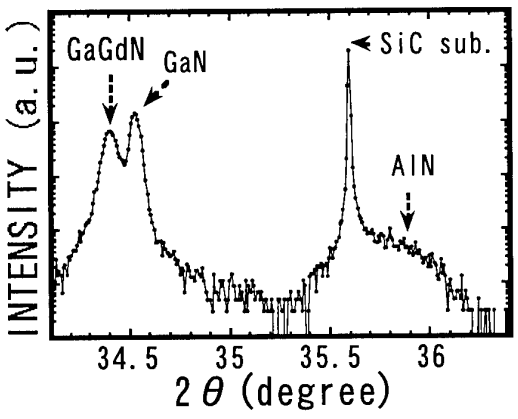


Fig.1. XRD pattern for GaGdN film.

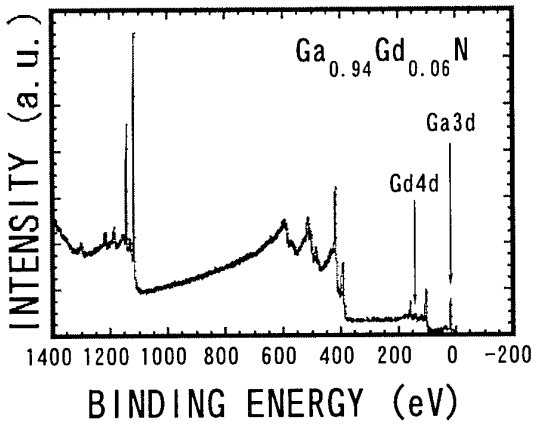


Fig.2. XPS spectrum for GaGdN film.

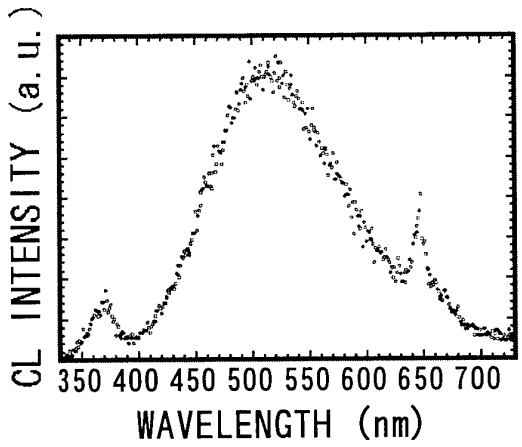


Fig.3. Room temperature CL spectrum for $Ga_{0.94}Gd_{0.06}N$ film.

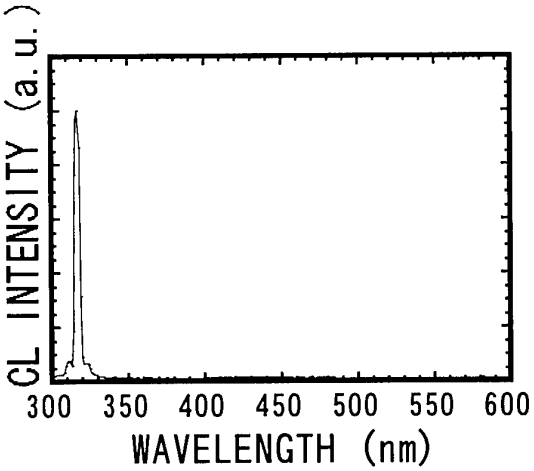


Fig.4. Room temperature CL spectrum for AlGdN film.

ThP Poster Session III



Surface Morphology of GaN Epilayer with Si_xN_{1-x} Buffer Layer Grown by Ammonia-source MBE

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GaN and related semiconductors such as AlN and InN are attractive materials for optoelectronic and high-temperature electron devices. The alloyed semiconductor of GaN, AlN and InN covers a wide bandgap range from 1.9 to 6.2 eV, promising for light emitting diodes and laser diodes. The GaN materials have also the high electron drift velocity and the high chemical stability, promising characteristics for high-temperature electron devices. Thus the growth of the high quality films is important for achieving the high performance of these devices, and there have been intensive growth studies using metal-organic chemical deposition (MOCVD), and molecular beam epitaxy (MBE).

In comparison with MOCVD technique, MBE technique has the advantages in growing the quantum structure including abrupt interface with good uniformity. However, due to the large lattice mismatch, heteroepitaxy of GaN on sapphire substrates results in the high density of dislocations, and in order to improve the film quality, it is necessary to employ additional techniques such as GaN or AlN low temperature buffer layer [1], migration enhanced epitaxy [2], In exposure [3], SiN buffer layer [4] and so on.

The usage of thin SiN films has been mainly employed in MOCVD system [4] and the significant improvement of the crystal quality has been reported. In this sturdy, we employed the SiN buffer layer for NH_3-source MBE technique.

The GaN films were grown by a Riber 32 MBE system with a reflection high-energy electron diffraction (RHEED) setup. Ga, Al and Si fluxes were supplied by Knudsen cells. NH_3 was supplied through an injector maintained at 300 ℃. The flow rate of ammonia was adjusted using a 50 SCCM mass flow controller. The chamber pressure during films growth was $5 - 6 \times 10^{-6}$ Torr. The (0001) sapphire substrates with 3000 Å Mo film deposited on the backside were used, and the substrate temperature was monitored by a pyrometer.

First, GaN epilayers without SiN buffer layer were grown as follows. The nitridation of the sapphire substrates were performed by exposing the surface to an ammonia flow of 20 SCCM at a substrate temperature of 900 ℃ for 10 min. The low-temperature (LT) GaN buffer layers with 300 - 500 Å thickness were then grown at 600 ℃, and annealed at 900 ℃ for 20 min. The growth rate of the LT GaN buffer was about 0.2 μm/h. The 1-μm thick GaN layers were then grown at the growth rate of 0.6 - 1.0 μm/h. The SEM image of the surface is shown in Fig. 1. The hexagonal surface features with a size of about 2 μm were observed. The Hall mobilities of the GaN films without SiN buffer layer were 100 - 120 cm^2/Vs. The high-

resolution X-ray diffraction (XRD) measurement was performed, and the full width at half-maximum (FWHM) of the ω–rocking curve were 830 - 860 arcsec. The FWHM of ω-2θ scans were 70 - 80 arcsec.

Next we investigated the effects of the thin SiN buffer layers. Just after the nitridation of the sapphire substrates, the SiN thin films were deposited by exposing sapphire substrate to Si and NH_3 flux for 10 min. The flow rate of NH_3 was kept at 20 SCCM, and the temperature of Si Knudsen cell was 1050 - 1200 ℃. On this SiN thin films, The LT GaN buffer layers were then deposited and annealed using the same condition as has been mentioned. The 1-μm thick GaN layers were then grown. During the growth, the RHEED patterns were more streakylike in comparison with the cases without thin SiN buffer layer. Figure 2 shows the SEM image of the surface of the grown GaN layer when the temperature of Si Knudsen cell was 1200 ℃. The surface morphology in Fig. 2 exhibits a step-like surface structure. We also found the improvement of the Hall mobility. The Hall mobilities of the GaN films with the thin SiN buffer were 150 - 160 cm^2/Vs. In terms of the XRD measurement, the FWHM of the ω–rocking curve were about 700 arcsec. The FWHM of ω-2θ scans were 60 - 70 arcsec.

The details will be discussed at the presentation.

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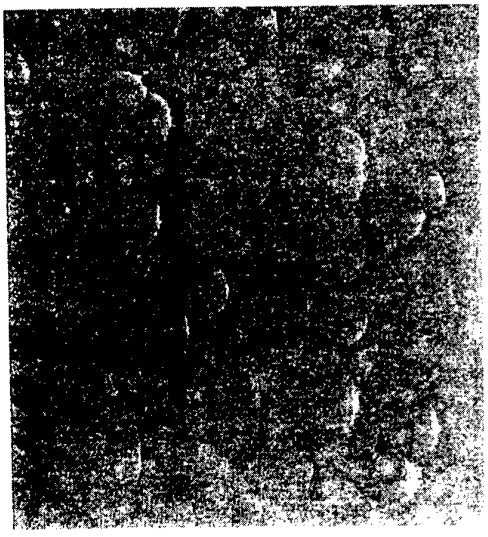


Fig. 1. The SEM image of GaN epilayer grown without SiN film.



Fig. 2. The SEM image of GaN epilayer grown with SiN film.

Metalorganic chemical vapor deposition growth of GaN thin film on 3C-SiC/Si(111) substrate using various buffer layers

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A key issue for the growth of GaN has been the lack of an ideal substrate. Most GaN has been grown on sapphire (α-Al_2O_3) since GaN substrates are not readily available [1]. The growth of high quality GaN films on silicon substrates using a SiC intermediate layer has been stimulated because of the irreplaceable merits of the Si wafer such as low cost, high surface quality, large area wafer availability, high conductivity and well-established processing techniques [2-5].

In this work, we have investigated the growth of high quality GaN films on 3C-SiC/Si(111) substrates using GaN, AlN, or GaN/AlN superlattice buffer layers with a MOCVD technique. 3C-SiC(111) films were grown on Si(111) substrates using tetramethylsilane ($Si(CH_3)_4$, TMS). GaN films were grown on 3C-SiC/Si(111) in a low pressure commercial MOCVD system using trimethylgallium (TMG), trimethylaluminum (TMA) and ammonia (NH_3). Fig. 1 shows AFM images for GaN films grown with and without buffer layers. When the GaN films grow without any buffer layer and with a 200 Å GaN buffer layer, they produce very rough surfaces (see Fig. 1(a) and (b)). However, the surface morphology is significantly improved for GaN films grown with AlN and superlattice buffer layers as can be seen in Fig. 2(c) and (d). Root mean square (RMS) roughness of the surface was about 4.21 Å for GaN films grown with superlattice buffer layers. Figure 2 shows XRD spectra for GaN films grown on SiC/Si(111) substrate using various buffer layers. For the GaN film grown directly on 3C-SiC/Si substrate, XRD spectrum shows a peak of wurtzite GaN(0002) at $2\Theta = 34.4^\circ$ with various small peaks, indicating the growth of polycrystalline-like GaN. However, the nature of polycrystallinity begins to decrease when grown on buffer layers. Consequently, the GaN film grown with a superlattice buffer layer (sample D) shows only a peak associated with the GaN(0002). Raman spectrum for the GaN films grown with superlattice buffer layer also showed the growth of high quality GaN films. Low temperature PL measurements showed that peaks associated with band edge emission and donor-accepter pair recombination (D^0A^0) were observed from GaN films grown with and without GaN or AlN buffer layers, whereas GaN films grown with the superlattice buffer layer exhibited a strong band edge peak with very weak D^0A^0 emission. The surface morphology and structural and optical properties of the GaN films were well correlated for the evaluation of GaN crystal quality.

Acknowledgement

This work was supported by grant No.(1999-2-114-008-5) from the interdisciplinary research program of the KOSEF.

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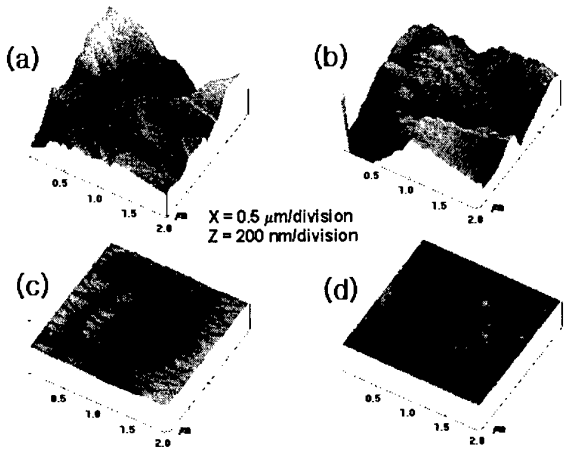


Figure 1. AFM images for GaN film surfaces grown on SiC/Si(111) substrate: (a) without buffer layer, (b) with 200 Å GaN buffer layer, (c) with 200 Å AlN buffer layer, and (d) with superlattice buffer layer consisted of four periods of 32 Å GaN layer and 20 Å AlN layers.

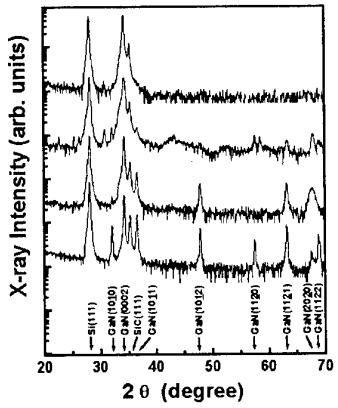


Figure 2. Wide angular range XRD spectra for GaN films grown on SiC/Si(111) substrate: (a) without buffer layer, (b) with 200 Å GaN buffer layer, (c) with 200 Å AlN buffer layer, and (d) with superlattice buffer layer.

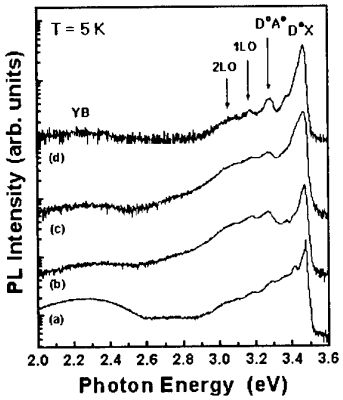


Figure 3. Low temperature (5 K) photoluminescence (PL) spectra for GaN films grown on SiC/Si(111) substrate: (a) without buffer layer, (b) with 200 Å GaN buffer layer, (c) with 200 Å AlN buffer layer, and (d) with superlattice buffer layer.

Catalytic growth of high quality GaN micro-crystals

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The preparation of amorphous GaN and GaN powder crystals is of great interest in sublimation growth of bulk GaN as well as in nano-scale optical technology [1-3]. It has been prospected that preparation of nano-crystalline GaN structures such as quantum wires or qauntum dots is one of the most promising approaches for improving the performance of optical devices based on III-nitrides [4].

In this work, GaN micro-crystals were catalytically grown using Ni-mesh by direct reaction of gallium and ammonia in a homemade quartz tubular reactor. The Ni catalyst was completely dipped in the Ga melt during the growth. The grown GaN crystals were separated from as-grown mixture by dissolving unreacted Ga and Ni catalyst in HCl solution. Figure 1 shows that the growth rate of the GaN crystals increases as the reaction temperature rises from 1000 to 1100 ℃ and the dependency of the growth rate on the temperature is much more significant in the presence of Ni catalyst. The use of the catalyst induced the increase of GaN crystal size. Figure 2 shows the TEM dark-field micrographs and the corresponding selected area diffraction pattern (SADP) along the electron beam direction $\mathbf{B}=[0\bar{1}10]$ with the reflection vectors $\mathbf{g}=0002$ (a) and $\mathbf{g}=\bar{2}110$ (b), respectively. Dark field micrographs show that the crystal consists of 2H hexagonal single crystal without any grain boundary. PL spectrum showed a strong band edge emission at the energy position of ~3.35 eV with FWHM of ~115 meV. The time-resolved photoluminescence measurements also reveal $\tau 1$ = 22 and $\tau 2$ = 109 ps for the catalytically grown GaN nano-crystals (Fig. 3), indicating the growth of high quality GaN. In order to investigate the effect of the Ni-catalyst on the cracking of NH_3 and the growth of GaN, the gas composition in the reactor was insitu analyzed using a quadrapole mass spectrometer (QMS). It was observed that reactive nitrogen species produced in the presence and absence of the Ni catalyst are different each other and the growth of GaN mostly occur by the reaction of Ga with atomic N adsorbed on Ni catalyst.

In conclusion, the Ni-catalyst stimulated the decomposition of NH_3 gas into the chemically active nitrogen atoms directly participating in the growth of GaN, resulting in the increase of the growth rate of the GaN crystals.

Acknowledgements

This work was supported by KRF Grant (KRF-99-005-D00036) through the Semiconductor Physics Research Center at Chonbuk National University.

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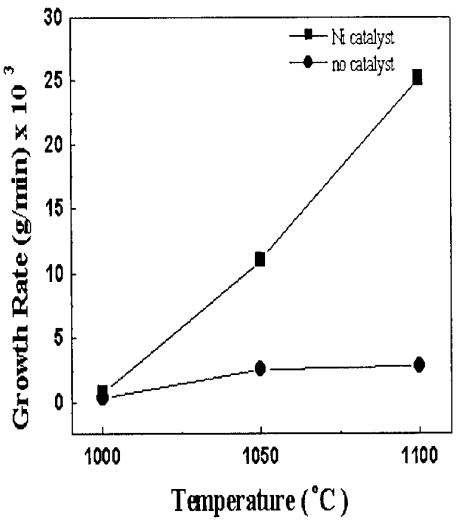


Figure 1. The growth rate of GaN crystals as a function of growth temperature at 1atm with 50sccm NH_3. (■ : in the presence and ● : absence of Ni-mesh catalyst).

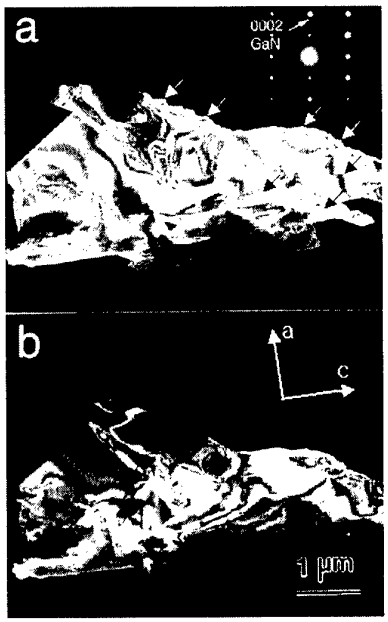


Figure 2. The dark-field micrographs and the corresponding selected area diffraction pattern (SADP) along the electron beam direction **B**= with the reflection vectors **g**=0002 (a) and **g**=$\bar{2}110$ (b), respectively.

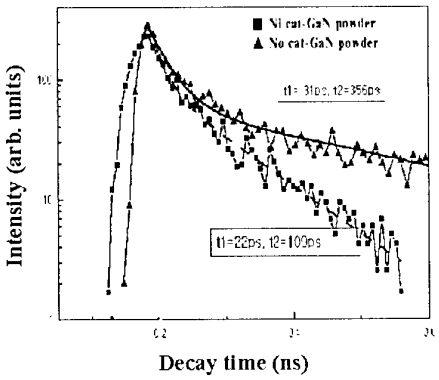


Figure 3. Photoluminescence decay for the catalytically grown GaN nano-crystals.

Crystallographic Growth Models of Wurtzite-Type Thin Films on 6H-SiC

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Epitaxial growth of GaN has been tried using various kinds of substrates so far. Of all the substrate, Al_2O_3 has been widely used for the GaN growth. Besides Al_2O_3, SiC is also expected as one of the most suitable substrates for the GaN growth, since SiC has a small mismatch in the lattice parameters with GaN and has good thermal stability under controlled atmospheres during the GaN growth. Both 6H-SiC and GaN having wurtzite structure belong to the same space group ($P6_3mc$). The lattice parameters are as follows : a=3.08, c=15.12Å for 6H-SiC and a=3.19, c=5.18Å for GaN. SiC has two opposite surface polarities along [001] direction. The main objective of our research was to establish a crystallographic growth model of GaN on the (00·1)6H-SiC with different polarities of Si and C surfaces.

Growth model of GaN on $(0001)_{Si}$SiC

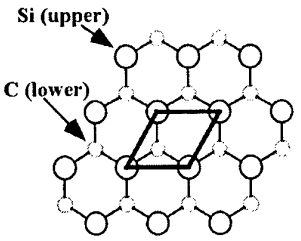
Fig.1(a) shows the surface structure of $(00\cdot1)_{Si}$SiC. Since coulomb attraction works between positive silicon ions and negative nitrogen ions, nitrogen atoms are deposited on the $(00\cdot1)_{Si}$SiC in the first growth step. Because of the covalent nature of SiC and GaN, nitrogen atoms deposit just above silicon atoms and Si(3C,N) tetrahedra are formed (Fig.1(b)). In the second growth step, three gallium atoms bond with one nitrogen atom and N(Si,3Ga) tetrahedra are formed as shown in Fig.1(c). In the third growth step, nitrogen atoms are deposited directly above gallium atoms and GaN_4 tetrahedra are formed (Fig.1(d)). Growth steps second and third should repeat alternatively and this will result in a complete wurtzite-type GaN structure. The Ga-N bond along the c-axis direction is weak compared to other three Ga-N bonds in a tetrahedron. The final layer of GaN film would be a gallium layer. That is, Ga-terminated GaN films are grown on $(00\cdot1)_{Si}$SiC.

Growth model of GaN on $(0001)_{C}$SiC

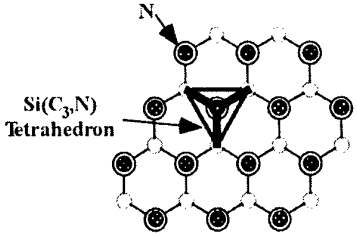
Fig.2(a) shows the surface of $(00\cdot\bar{1})_{C}$SiC. Gallium atoms are deposited on the $(00\cdot\bar{1})_{C}$SiC in the first growth step for the same reason as described in the previous section. Ga atoms deposit just above carbon atoms and C(3Si,Ga) tetrahedra are formed(Fig.2(b)). In the second growth step, each nitrogen atom is deposited onto three gallium atoms and Ga(C,3N)

tetrahedra are formed (Fig.2(c)). In the third growth step, gallium atoms are deposited directly above nitrogen atoms and NGa_4 tetrahedra are formed (Fig.2(d)). In this case, the final layer of the GaN film would be a nitrogen layer. This indicates that N-terminated GaN films are grown on $(00\cdot\bar{1})_C$SiC.

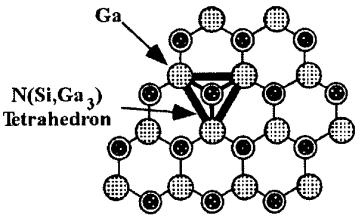
These modeling simulations were discussed from the Poling laws, and compared with the results obtained in the GaN growth on SiC substrates in literatures.



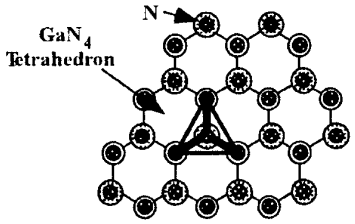
(a) Si surface terminated SiC substrate



(b) 1st step: N atoms bond with the Si on the surface to form Si(C_3 ,N) tetrahedra.

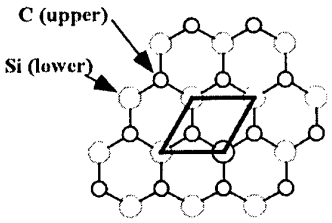


(c) 2nd step: Ga atoms bond with the just deposited N to form N(Si,Ga_3) tetrahedra.

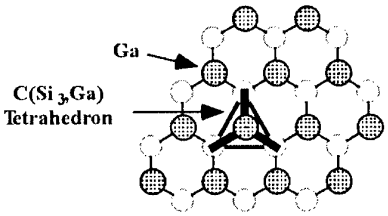


(d) 3rd step: N atoms bond with Ga to form GaN_4 tetrahedra.

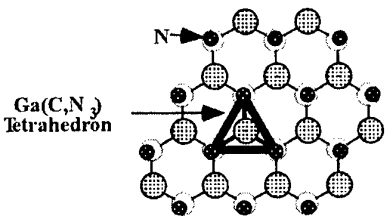
Fig.1 Growth of GaN on $(0001)_{Si}$SiC



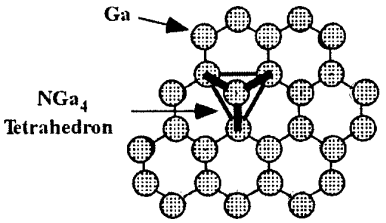
(a) C surface terminated SiC substrate



(b) 1st step: Ga atoms bond with the C on the surface to form C(Si_3 ,Ga) tetrahedra.



(c) 2nd step: N atoms bond with the just deposited Ga to form Ga(C,N_3) tetrahedra.



(d) 3rd step: Ga atoms bond with N to form NGa_4 tetrahedra.

Fig.2 Growth of GaN on $(0001)_C$SiC

Structural properties of single crystallic solid solution $(SiC)_{1-x}(AIN)_x$ obtained by sublimation epitaxy .

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Abstract

Solid solutions $(SiC)_{1-x}(AIN)_x$ - new semiconductor materials obtained in single crystallic form in every interval composition [1]. SiC and AIN form non - stop series of solid solution with a width of band gap from 3-6eV. which during definite composition have a direct gap structure [2]. Excluding this solid solutions $(SiC)_{1-x}(AIN)_x$ inherits unique mechanical, chemical and thermal properties form silicon carbide. That's why, presents perspective application of them in instruments, working in experimental condition in short wave region of optical range . Especially perspective solid solutions $(SiC)_{1-x}(AIN)_x$ in instruments, based on heterojunctions (injectional lasers, light diodes, photoreceivers,..etc). As such near parameters of lattices and coefficients of temperature expansions SiC and $(SiC)_{1-x}(AIN)_x$ allow obtaining heterojunctions on their base with lesser number of defects on heteroboundary.

This work was dedicated in the learning of processes of growth epitaxial layers

$(SiC)_{1-x}(AIN)_x$ from gaseous phases methods of sublimation and investigation of structural properties depending on technical parameters of growth.

Single crystallic epitaxial layers $(SiC)_{1-x}(AIN)_x$ grown on substrates SiC polytype 6H in the temperature range of 2300-2550K at the pressure of N_2+Ar mixture from $2\cdot 10^4$-$8\cdot 10^4$ Pa in the zone of growth .

Sublimation etching surface substrates in surplus vapors Si and next growth epitaxial layers in nonstoppable process allows to decide problem of defectness intransitional layers on the boundaries of substrates epitaxial layers, form due to the passivation of surfaces substrate of carbon during the dissociation of SiC .

Definite dependence on growth speed, composition of epitaxial layers from technological parameters. Establishment, which effected on the composition of growing layer of solid solutions $(SiC)_{1-x}(AIN)_x$ show the relation of partial pressure of argon and nitrogen in the growth zone. Growth speed increase partial pressure P_{N2} and decreases with the increase in temperature improves the structure completely of the layers.

Investigation shows possibility of controlling types of electrical conductivity with a change in partial pressure of N_2 in the working chamber. In this work it is shown the method used in obtaining anisotype heterostructures n-SiC/p-$(SiC)_{1-x}(AIN)_x$ in nonstoppable system of growing layers .

Polytype structures and completion of epitaxial layers depend on the contents of AIN. Layer with $x< 0.4$ have high completion but with increase in AIN structural completion deteriorates and also during $x\geq 0.65$ observed block structure and high nonhomogeneous composition in volume and in surface.

Volume homogeneity was formed and identified by laser introscopic method. In this work we present results of the investigation of the interaction of radiation of nitrogen laser (P=15-20kwatt, V=120mvolt., λ=0.337μm) on the dynamic reorganization of structural defects in epitaxial layers. It is found that the increase in concentration centers of radiation recombinants intensive luminescence centers , forming and burning of defects.

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PHYSICS OF HETEROEPITAXY AND HETEROPHASES

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Because of the differences in the elastic, geometric and thermal properties of host materials involved in modern heteroepitaxial growth, the interfaces of the elaborated structures can be of variable quality. It is well known that materials presenting large lattice mismatch develop misfit strains at their interfaces. Beyond the critical thickness of the growing overlayer, extended defects as misfit dislocations can be created and then can propagate into the overlayer.

We have performed a theoretical approach which enables (i) to evaluate the best choice of host materials for heteroepitaxy and (ii) to propose a valuable strategy for optimizing their interfaces. The essential idea of the theory is based on the relationship between strain gradient and dynamics as shown by elasticity theory equations. From these equations we can identify the S factor - $S=f(C_{ij})/\rho$, where $f(C_{ij})$ are the effective elastic constants and ρ the density - as the important parameter of the theory. S must be considered within an approach which takes account not only of the mismatch of the lattice parameters of the host materials, but also of the difference in their elastic-density features. The theory implies interface continuity conditions which must be fulfilled by the host material's relevant physical properties.

We have considered a wide range of heterosystems including $Si_{1-x}C_x/Si$, $Si_{1-x-y}C_xGe_y/Si$, 3C-SiC/Si, AlN/3C-SiC, GaN/3C-SiC, ... In heterostructures where a large misfit exists between the substrate and the overgrown material, the insertion of a transitional layer or the incorporation of foreign atoms aiming at improving the interface quality, may often be useful. In this case, we demonstrate that our approach can be used to predict the composition of such transitional layers. By applying the continuity conditions imposed by the present theory, i.e., by performing in-heterostructure semiconductor physics, we are then able to determine optimized choices which can be exploited in heteroepitaxial growth experiments.

Formation of Epitaxial Mesa Structures on 4H-SiC (0001) and (11$\bar{2}$0) Substrates

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Silicon carbide (SiC) is a potentially important candidate for high-power and high-frequency devices, owing to its excellent properties of wide bandgap, high electron saturation drift velocity, high thermal conductivity and high breakdown field. High-quality homoepitaxial layers can be obtained at 1200-1500 °C by chemical vapor deposition (CVD) utilizing "step-flow growth" on off-axis SiC (0001) substrates. Matsunami group has researched the growth mechanism of SiC on on-axis and off-axis 6H-SiC substrates[1]. The nucleation, lateral growth ansisotropy, and effects of off orientation have been described utilizing mesa tables on 6H-SiC (0001) substrates[2]. In this paper, we report the formation of SiC epitaxial mesa structures on partly masked 4H-SiC substrates by a CVD method. The various influences on SiC mesa structure and polytypes of grown layers are investigated.

In this work, off-axis 4H-SiC (0001) 8° inclined toward <11$\bar{2}$0> and (11$\bar{2}$0) Si face substrates were used. Masked substrates for mesa growth were prepared using a photoresist by a conventional lithographic technique and annealing at 800 °C for 10 min in Ar. The annealed photoresist (0.5 μm-thick carbon layer) as a mask for mesa growth can be removed after growth by oxidizing at 1000 °C. Epitaxial mesas were grown at 1500 °C by atmospheric-pressure CVD using a SiH_4-C_3H_8 system in a horizontal water-cooled reactor. The flow rates of SiH_4, C_3H_8, and H_2 were 0.15-0.30 sccm, 0.15-0.30 sccm, and 3.0 slm, respectively. These conditions have led to the corresponding homoepitaxial growth rates of 1.2-2.5 μm/h on maskless SiC substrates. The growth time was 30-60 min. SiC mesa epilayers were unintentionally doped with a C/Si ratio of 3, and characterized with a Nomarski microscope, a scanning electron microscope (SEM), and Raman scattering.

Figure 1 gives the Nomarski microscopic and SEM images before and after mesa growth on masked 4H-SiC substrates. Due to the anisotropy in the lateral growth rate, a circular opening before growth was deformed into a hexagonal mesa structure after CVD growth on the off-axis (0001) substrate (Fig.1(b)). Especially, along the [11$\bar{2}$0] off-direction the hexagonal shape is sharper than the other equivalent directions. This is ascribed to an additional step-flow growth on the off-axis (0001) substrate compared to the growth on an on-axis substrate. A (0001) facet on the off-axis (0001) SiC substrate can be seen at the upstream side of step-flow on the SiC mesa structure as reported by Kimoto and Matsunami[2]. The (0001) facet broadened and the elongated hexagonal mesa structure became sharper with increasing the growth time. A grooved surface emerged at the upstream side of step-flow or in the vicinity of (0001) facet. On the masked 4H-SiC (11$\bar{2}$0) substrate, the mesa structure after growth almost retained a circular shape (Fig.1(c)).

Figures 1(d) and (e) show the SEM images of SiC mesa structure on 4H-SiC substrates after the carbon mask was removed by thermal oxidation. The masked region was specular without surface degradation, resulting in the successful formation of SiC epitaxial mesa structures on SiC substrates. Since the surface migration of reactant species on the surrounding mask into the growth region occurred during the growth, the growth thickness profile across the patterned area shows a thicker periphery than the center of the patterned area.

As shown in Fig. 2, the lateral growths on the carbon mask are also observed by an SEM at the upstream and downstream sides of the [11$\bar{2}$0] off-direction. Due to the occurrence of additional step-flow growth along the [11$\bar{2}$0] off-direction, the lateral growth length on the carbon mask at the downstream side is larger than that at the upstream side.

On the off-axis (0001) masked substrate, 3C-SiC appeared on the SiC mesa structure at the upstream side of step-flow in the part of grooved surface, but only 4H-SiC epilayers without 3C-SiC were grown in the part of flat surface (downstream side of step-flow), which were verified by Raman scattering. On the (11$\bar{2}$0) masked substrate, however, no 3C-SiC was detected on the SiC mesa structure by Raman scattering. Circular SiC mesa structures with smooth morphology can be obtained on the masked (11$\bar{2}$0) 4H-SiC substrate. Details of 4H-SiC homoepitaxy on partly masked substrates will be described in the presentation.

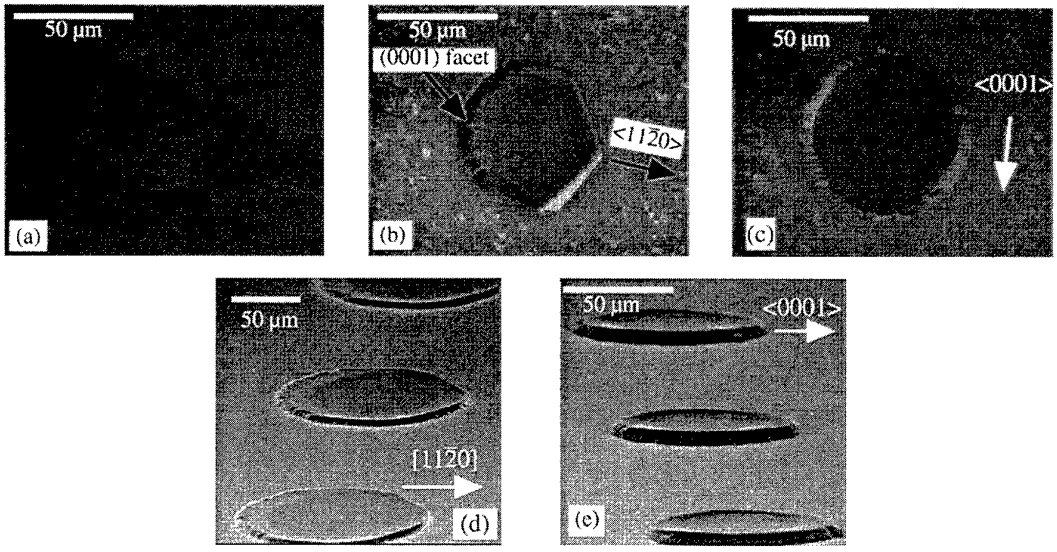


Fig. 1 Nomarski microscopic and SEM images of SiC mesa structure on 4H-SiC masked substrates: before growth (a), after growth on (b) off-axis (0001) and (c) (11$\bar{2}$0); SEM images grown on off-axis (0001) (d) and (11$\bar{2}$0) (e) substrates.

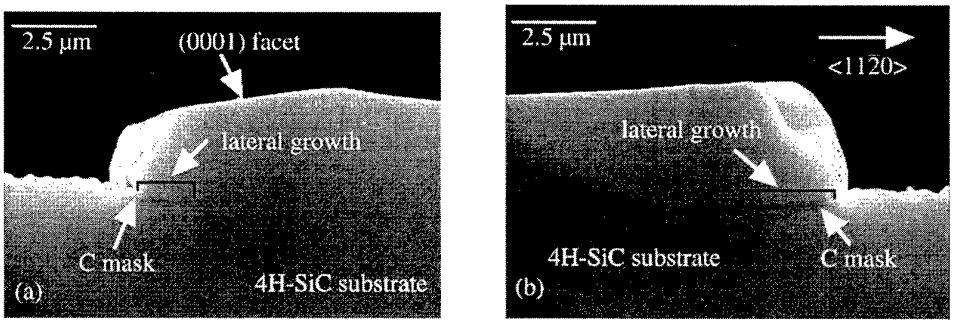


Fig. 2 Cross sectional images of SiC mesa structure with a diameter of 60 μm grown on off-axis (0001) substrate. (a) at the upstream side and (b) at the downstream side of [11$\bar{2}$0] off-axis.

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Growth of low doped 4H-SiC layers by sublimation epitaxy: effect of low doped SiC source material and tantalum in the growth environment

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Sublimation epitaxy is a technique for growth of thick epitaxial layers with growth rates up to 100 μm/h while maintaining smooth as-grown surfaces and conditions for improved structural quality [1]. The remaining issue of avoiding introduction of impurities from the growth environment to the epitaxial layer is a challenging task. The purity of the solid polycrystalline SiC source material used for feeding the epitaxial layer during growth is the most critical issue in the growth of low doped SiC layers by sublimation epitaxy.

In this paper the influence of impurities, in particular the predominantly existing boron, in relatively pure source material and the effect of tantalum (which is used in the growth cell to getter carbon and avoid graphitization of the source and epilayer by increasing the Si/C ratio in the vapor) has been studied. The layers have been characterized using capacitance-voltage measurement, deep level transient spectroscopy, minority carrier transient spectroscopy and cathodoluminescence techniques to detect electrical characteristics of electron as well as hole traps and impurities. Sublimation epitaxy [2] was performed on the Si-face of 4H-SiC substrates with surfaces off-oriented 8° in the [11$\bar{2}$0] direction. The deposition rate was ranging from ~25 μm/h up to ~200 μm/h in the temperature intervall of 1725 to 1800°C. The layers are n-type with net carrier concentrations in the E15 cm^{-3} range or low E16 cm^{-3}.

One limitation in growth of low doped epilayers by sublimation techniques is that very high purity SiC source material (total impurity concentration <E15 cm^{-3}) and tantalum are not available. The available polycrystalline SiC wafers contain nitrogen, boron and aluminium as major impurities. The typical concentrations are given in Table I for three suppliers of polycrystalline SiC wafers (denoted source A, B and C in Table I). Even though the overall purity of source C is improved in comparison to other source materials, it still contains boron. This study mainly presents results from sublimation epitaxial growth using this source material and various tantalum foils of different thicknesses and purity.

	Thickness	Purity	B conc. [atoms/cm^3]	Al conc. [atoms/cm^3]	N conc. [atoms/cm^3]
Source supplier A			Low E16	E15	E17
Source supplier B			Low E18	-*	Low E16
Source supplier C			E15 - E16	-*	<E16
Ta foil 1	25 μm	99.997%			
Ta foil 2	250 μm	99.98%			
Ta foil 3	2 mm	99.999%			

TABLE I. Summary of purity of polycrystalline SiC source and Ta foil studied in the sublimation epitaxial growth, impurity levels assessed from SIMS measurements. * - below detection limit.

The source of aluminium seems to be the tantalum foil. We will show that the thickness and purity of the tantalum foil are important to avoid aluminium. At optimized conditions the Al concentration of the layers is below the detection limit of SIMS ($5x10^{14}$ cm^{-3}) and aluminium is not observed in low-temperature photo-luminescense or cathodoluminescence measurements. The concentration of boron in the epilayers increases with increasing growth time, Fig. 1. The shallow boron center is generally formed in epitaxial growth [3] and boron in this case is believed to occupy the silicon site in the SiC lattice. During sublimation epitaxy the initial effect of the Ta foil to getter carbon is probably decreasing and thus the Si/C ratio in the vapor is decreasing during growth. This provides conditions of increased incorporation of boron in the epilayer with decreasing Si/C ratio which is in agreement with studies of the site competion effect [4].

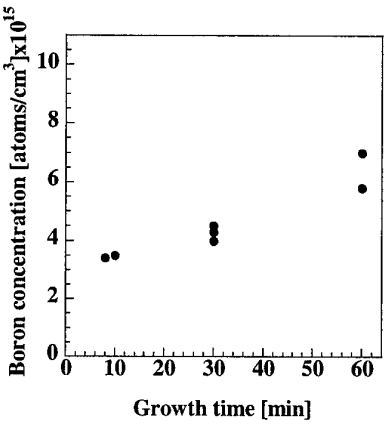


Fig. 1. Boron concentration in the layers vs growth time.

Most interestingly, in the electrical measurements we observe that the compensation level is low even though the boron concentration as measured by SIMS is in the same order as the nitrogen concentration or even higher while the layers still are n-type. This suggests that most of the boron is not electrically active. The amount of electrically active boron seems to depend on the concentration of boron in the epilayer. Investigations of deep levels in the epilayers indeed show presence of boron. Both shallow boron and deep boron D-centers are detected in the layers.

Electron trap (capture cross section)		$Z_{1,2}$	0.4-0.5 eV ($2x10^{10}$ cm^2)	0.65 ($3x10^{16}$ cm^2)	1.0 ($2x10^{14}$ cm^2)
Sample type 1	Sample 1	$4.0x10^{13}$	$2.7x10^{13}$	$1.2x10^{13}$	$3.0x10^{13}$
	Sample 2	$2.4x10^{13}$	$1.0x10^{13}$	*	$6.0x10^{12}$
Sample type 2	Sample 3	$2.5x10^{13}$	*	*	*
	Sample 4	$4.0x10^{13}$	*	*	*

Table II. Electron traps detected in two types of layers grown by sublimation epitaxy using source C, * - below detection limit.

The concentration of the $Z_{1,2}$ electron trap is in the order of ~2-4 $x10^{13}$ cm^{-3}, Table II. This is in similar concentration as measured in thick layers with similar doping but grown by high-temperature chemical vapor deposition at deposition rates ranging from 10 to 14 μm/h at growth temperature 1700°C. The concentration of $Z_{1,2}$ was decreased to $1.3x10^{13}$ cm^{-3} in the best case [5]. Other electron traps, see Table II, are either in the E12 to E13 range or below the detection limit depending on the growth conditions. More details of the boron incorporation and electron trap formation related to sublimation epitaxy growth conditions will be presented.

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Aluminium incorporation in 4H-SiC layers during epitaxial growth in a Hot-Wall CVD system

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The incorporation of aluminium during epitaxial growth in a horizontal Hot-Wall CVD system has been studied in the concentration range from $1x10^{15}$ cm^{-3} to $2x10^{18}$ cm^{-3}. Epitaxial growth was performed using silane (2% diluted in H_2) and propane (5% diluted in H_2) as process gases and trimethylaluminium (TMA) as doping source. 4H-SiC (0001) substrates off-oriented 8° towards $<11\bar{2}0>$ with diameters of 35 mm (Cree Res. Inc., SiCrystal) were used. Before loading into the Hot-Wall CVD reactor the substrates were cleaned according to the RCA procedure followed by immersion in a HF solution in order to remove the surface oxide. The substrates were etched in hydrogen atmosphere at 1550 °C adding a small quantity of propane to reduce the surface roughness and to remove a residual surface damage layer immediately before layer deposition.
Sources of residual background donor impurities, especially nitrogen, may be the susceptor, the thermal insulation and the reaction cell. To suppress the contamination by nitrogen the susceptor and the substrate holder were made of high purity graphite with SiC coating. Argon is available as a purge gas during loading and unloading the cell.
In accordance with the site competition mechanism the N incorporation can be controlled by the C/Si ratio [1]. In [2] this ratio was varied from 0.5 to 2 by keeping all growth parameters constant except the propane flow. The expected suppression of the N incorporation with increasing C/Si ratio was observed. For a C/Si ratio of 2, the N concentration is already lowered down to $2x10^{14}$ cm^{-3}. Therefore the compensation by unintentional nitrogen doping can be neglected in the investigated p-type doping range.
Typical ranges of the most important parameters for the CVD-experiments are given in Table 1.

Table 1: Typical growth parameters

silane flow, 2% diluted in H_2	propane flow, 5% diluted in H_2	C/Si ratio	temperature	system pressure	hydrogen main flow
450 sccm	90 to 120 sccm	1.5 to 2	1550 to 1600 °C	150 to 250 mbar	20 to 50 slm

The thickness of the epitaxial layers was determined by means of a Fourier transform infrared spectrometer and a software package (both obtained from BRUKER) evaluating the interference fringes which occur in the reflectance spectra. The chemical Al concentration was measured by secondary ion mass spectroscopy (SIMS) whereas the electrically active doping concentration was determined by capacitance-voltage (C-V) and Hall effect measurements. Because of the relatively high ionisation energy of the Al acceptors it was necessary to set the C-V measuring frequency down to 10 kHz for obtaining the full net acceptor concentration at room temperature.
The Al-doped epitaxial layers showed very smooth, mirror like surfaces. The net acceptor concentration estimated from C-V measurements agreed well with the Al concentration determined by SIMS. Hence, the passivation of Al acceptors by hydrogen seems to play no

significant role in comparison to boron doping [1] under our growth conditions. The Al concentration increased strongly with the Al partial pressure.

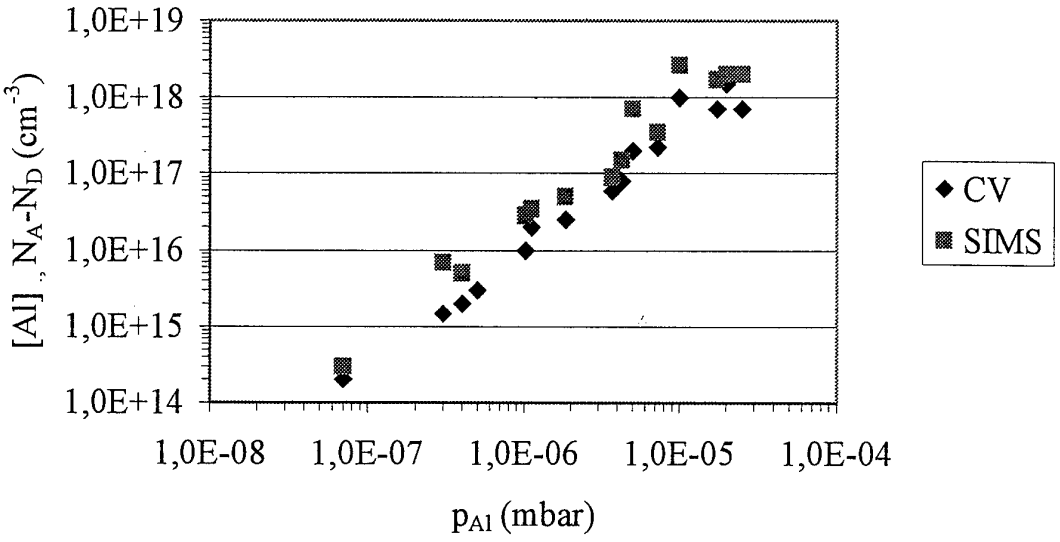


Fig.1:Al and net acceptor concentration determined by SIMS and CV measurements, respectively, in dependence of the Al partial pressure

Hall effect investigations were conducted in van der Pauw arrangement. For the evaluation of electrically active Al concentrations, the Hall scattering factor for holes given in Ref. [3] was taken into account. The Al acceptor concentrations determined by Hall effect agree well with the values obtained from SIMS and CV measurements (not shown in Fig. 1). The Hall mobility values at room temperature ranging from $66cm^2/Vs$ to $110cm^2/Vs$ in epilayers with Al concentrations varying from 10^{16} cm^{-3} to 10^{18} cm^{-3} reflect the high quality of the grown Al-doped epilayers.

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Epitaxial growth of 4H-SiC with hexamethyldisilane HMDS

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SiC is a semiconductor of great interest for high temperature and high power electronic devices. For these applications, high growth rate material is important. In this work, we studied the homoepitaxial growth of 4H-SiC using hexamethyldisilane $Si_2(CH_3)_6$ (HMDS) in place of the usual silane/propane system. HMDS is a single source C and Si precursor. It has been used for 3C-SiC heteroepitaxial growth [1, 2] in order to lower the growth temperature.

The growth was performed in a AP-CVD vertical reactor at 1600 and 1500°C on 8°off 4H-SiC substrates. In this system heteroepitaxy of 3C-SiC on Si at 1350°C with HMDS [3] leads to a maximum growth rate of 6 µm/h for a C/Si ratio of 3.5. For comparison the maximum growth rate obtained with the silane/propane system in similar growth conditions is of 3 µm/h only. Higher growth rates degrades the crystalline quality.

In this study HMDS was used as Si and C source or with addition of propane to vary the C/Si ratio from 3 to 15. Comparison was made with the silane/propane system. The HMDS flow rate was varied from 0.6 to 2.4 sccm, which corresponds to a silicon flow rate of 1.2 and 4.8 sccm respectively. The 4H-SiC layers were characterized by optical microscopy, atomic force microscopy (AFM), Raman spectroscopy and low temperature photoluminescence (LTPL). Infra-red reflectivity was used to evaluate the layer thicknesses.

The layers exhibit a defect density of about 10^4 per cm^2 highly dependent on the substrate quality. The average AFM roughness (RMS) is 0.5 nm (10x10 μm^2 scans) for both $HMDS/C_3H_8$ and SiH_4/C_3H_8 precursors. The growth rate ranged from 2.6 to 10 µm/h for HMDS flows of 0.6 to 2.4 sccm. The typical growth rate obtained with the silane (0.8 sccm) and propane mixture is 3.4 µm/h. The growth efficiency related to the Si flow is then lower for the HMDS precursor. HMDS do not allow the growth with high C/Si ratios. Only the layers grown with a C/Si ≤ 7 exhibit a mirror like morphology whereas the C/Si ratio can be as high as 15 with silane/propane.

Raman spectra exhibit two FTO modes (796 and 776 cm^{-1}), the FLA (610 cm^{-1}) and the FLO (964 cm^{-1}) modes. The quality factor κ ratio [4], which is the ratio of the intensity of the two FTO modes 796/776 increases by increasing the C/Si ratio for both precursors. LTPL spectra show the N-BE zero-phonon line Q_0 with phonon replica. The 77 meV phonon replica of the free exciton transition is also observed. A DAP Al-N band which was present on the substrate spectrum also appears. No difference in these characteristics have been observed between the silane and the HMDS system.

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Low temperature preparation of α-SiC epitaxial films by Nd:YAG pulsed laser deposition

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Introduction

Silicon carbide attracts a considerable attention since it is a promising material as high-temperature and wide band-gap semiconductor. Lots of efforts are devoted to synthesize high-quality single crystals for device applications. Recently, single crystals wafers of SiC with 2 inches diameter have been commercially available. However, because of high melting point, large size of SiC single crystal is still hard to synthesize and is very expensive. Many trials have been made for preparing epitaxial films as well. It needs high temperature process to fabricate the films for the same reason. In this study we report the fabrication of hetero-epitaxial α-SiC films on sapphire substrates at considerably low temperature (Ts=820°C) by using pulsed laser deposition (PLD).

Experimental

Silicon carbide (SiC) films were fabricated by a PLD method using the 4th harmonic (266nm) of Nd:YAG pulsed laser under the following conditions; the pulse frequency of 2Hz and the fluence of ρ=2~20J/cm^2. Targets of sintered α-SiC were purchased from Furuuchi Chemical Co. Fabrication was made on Si (111) and sapphire (001) single crystal substrates. After ultrasonic cleaning in acetone solvent, the substrate was set in a vacuum chamber and was heated to 800°C to clean the surface. All deposition was made under argon atmosphere of 50Pa, since oriented films did not grow in vacuum at low temperature. The crystallinity and orientation of the prepared films were examined by X-ray diffraction (XRD) using Cu Kα x-ray and reflection high-energy electron diffraction (RHEED), respectively.

Results and Discussions

(i) α-SiC films on Si substrates

Figure 1 shows XRD patterns of the SiC films fabricated on Si (111) substrates at 800°C using a laser fluence of (a) 20J/cm^2 and (b) 10J/cm^2. Two diffraction lines are observed at 2θ=38.08° and 81.56° which are definitely assigned to XRD from α-SiC (6H (103) and 6H (206) for 6H α-SiC). Low temperature stable SiC (β) does not give rise to signal at the angles. Full width at half maximum (FWHM) of the 6H (103) XRD line measured by ω-scan was 0.98°, indicating the growth of one-axis oriented crystalline film. The growth temperature of the film is considerably low compared with that of other methods such as CVD (Ts~1500°C). The reason may be as follows. Kinetic energy of ejected species in PLD process is much higher than that for other deposition process. The high kinetic energy may supplement the insufficiency of the energy for crystallization of the film. It is consistent with the result that the XRD peak intensity (which correlates to the crystallinity) increases with increasing the fluence of laser beam as seen in Fig.1, since increasing the laser fluence may lead to an increase of the kinetic energy.

At the present time it is not possible to fabricate the oriented films of α-SiC in vacuum at low substrate temperature around 800°C. The reason is not clear, but might be as follows. Argon atoms collide with the ejected particles and may scatter the components with low kinetic energy. As the results only particles with high energy selectively reach the surface of the substrate and make high quality of films.

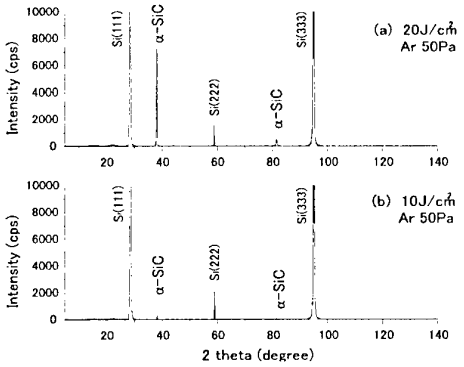


Figure 1. XRD patterns of SiC films fabricated on Si (001) at Ts= 800°C with a laser fluence of (a) ρ=10J/cm^2 and (b) 20J/cm^2.

(ii) α-SiC films on sapphire substrates

We have tried to fabricate SiC films on sapphire (001) substrates under the deposition conditions of Ts=820°C and ρ=20J/cm^2. Formation of SiC films with c-axis orientation was confirmed by XRD. The films have different orientation from that on Si substrates. Figure 2 shows RHEED patterns of a sapphire substrate and the film deposited on it. Before the deposition, two kinds of diffraction patterns are alternatively observed by every 30° rotation (Fig.2 (a) and (b)), showing the C_6 symmetry. The direction of the incident electron-beam for the images (a) and (b) is [100] and [$\bar{2}$10] of the substrate, respectively. After the deposition of the SiC, the diffraction pattern (a) turns to the dotted pattern with large separation (Fig.2 (c)). The pattern (d) is obtained at the direction where the image (b) was observed for the substrate. These results indicate that the film has the same symmetry as the substrate. Lattice constant of the film was estimated to be ~3.02Å from the separation between dotted lines. It agrees with the reported value (a=3.08Å for α-SiC). These results indicate the epitaxial growth of SiC films. It is also found from the RHEED patterns that hexagonal lattice of SiC (001) does not have the same alignment as sapphire unit lattice (solid line in Fig.3) but have the same orientation as the oxygen sub-lattice of sapphire (dotted line in Fig.3) which is rotated by 30° against the sapphire hexagon. The results are reasonably explained by the good lattice matching of SiC (001) with the oxygen sub-lattice of sapphire as seen in Fig.3 (The mismatch is only 4.1%).

SiC films fabricated on Si substrates showed no RHEED patterns except for Laue ring which is characteristic of polycrystalline films. It might be because of the large lattice mismatch of 19.8% between the film and Si (111).

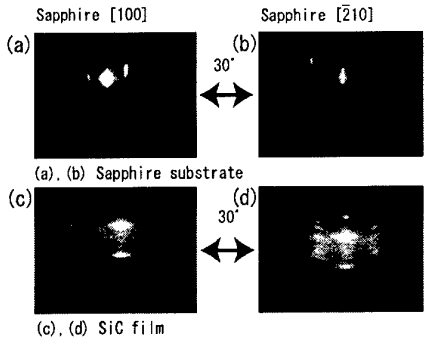


Figure 2. RHEED patterns of SiC film on sapphire substrate (a), (b) before and (c), (d) after deposition.

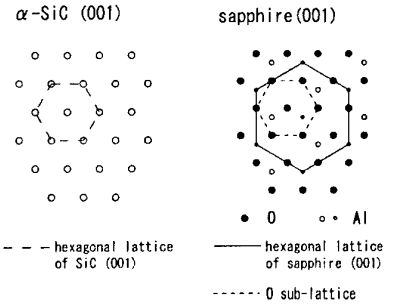


Figure 3. Schematic diagrams showing the hexagonal lattice of α-SiC (001) and sapphire (001) planes.

Fabrication and characterisation of 3C-SiC layers on 6H-SiC (0001) substrates

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Epitaxial 3C-SiC layers on 6H-SiC (0001) substrates were obtained in an ultra high vacuum MBE chamber through repeated steps of 2 mono-atomic silicon layer deposition on the (3x3) reconstruction followed by a carbonization reaction using C_2H_4 gas. Substrates of 6H structure with (0001) facets of 1 cm^2 area, grown by the modified Lely method, were on-axis N-doped single crystals. The 3C-SiC layer growth was controlled in situ by LEED, XPS and XPD. The microstructure of one deposited layer was identified by transmission electron microscopy (TEM) on a thin foil specimen corresponding to a cross-section of the layer. We found that such epilayers of 16 nm thickness are epitaxial and formed by a single 3C-SiC phase. Their epitaxy with substrates corresponds to a (111) plane of the cubic structure parallel to the (0001) 6H-SiC plane at the interface and a [110] direction of 3C-SiC parallel to a [1100] direction of the hexagonal structure. However, as such an epitaxial relationship implies three orientation possibilities the 3C-SiC structure with respect to the substrate, twinned domains were formed. When examined by TEM, superimposed twinned domains oriented along <110> zone axes give rise to moiré effects, which have previously been discussed without reaching a clear understanding of their origin [1]. We show at least, how the assumption of a 9R polytype can be ruled out from a careful analysis of both high resolution images and corresponding electron diffraction.

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Formation of extremely thin, quasi-single-domain 3C-SiC film on on-axis Si(001) substrate using organo-silane buffer layer

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Heteroepitaxially grown 3C-SiC on Si provides one of the possible solutions to the problems of limited diameter and the micropipes of present SiC wafers. The heteroepitaxy, on the other hand, suffers formation of several kinds of defects in the grown film. Among them, anti-phase boundary (APB) is considered to be the hardest barrier to eliminate, which forms deep levels in the energy gap and acts as scattering centers for carriers[1]. To suppress APBs at the interface and their subsequent development in the growing film as well, miscut Si wafers have been used to facilitate anisotropic growth to develop predominant domains[2]. The problems with this method are the formation of defects in the grown film triggered by the surface steps on the miscut Si substrate[3] and the possible degradation of the device characteristics formed on the inclined film surface. To overcome this, a method has to be developed to realize the single-domain surface without using miscut surfaces. We here present a new method to grow a quasi-single-domain 3C-SiC film on on-axis Si(100). What should be emphasized is the extremely thin thickness (45 nm) of the film, which is compared to that required in a previous study (>5 μ m)[1] to achieve the single-domain surface on an on-axis Si(001) substrate.

The method starts with formation of a 3C-SiC interfacial buffer layer on on-axis Si(001) substrate at T_s=650°C [4] using monomethylsilane (SiH_3CH_3; MMS) at P_{MMS}=5.0×10^{-5} Torr. Samples were resistively heated by passing a DC current along either [100] or [1-10] direction. A 3C-SiC film was then grown onto the buffer layer (Organo-silane buffer layer: OS-buffer layer) at T_s= 900°C using MMS at P_{MMS}=5.0×10^{-5} Torr.

Figure1 presents a reflection-high-energy-diffraction (RHEED) pattern from the on-axis Si(001) surface flash-annealed at 1000°C. The pattern, taken along the [110] azimuth, shows a (2x1)+(1x2) reconstructed surface structure with Kikuchi lines, which indicates a presence of atomically flat, double-domain surface on this starting substrate. Figure2 shows a RHEED pattern from the OS-buffer layer prepared at T_s=650°C, P_{MMS}=5.0×10^{-5} Torr for 5 minutes. Appearance of only 3C-SiC spots indicates the formation of a uniform, single-crystalline 3C-SiC buffer layer that fully covers the Si substrate. Cross-sectional TEM observation[4] indicates formation of an atomically flat SiC/Si interface without voids at this low temperature, which is ascribed to the unique adsorption nature of the MMS molecules[5]. When a 3C-SiC film was grown onto this buffer layer using a resistive heating along the [100] direction, the [110]-RHEED pattern presented fundamental spots as well as 1/2-order streaks, while the [1-10] pattern presented only fundamental spots. With post-annealing at 1000°C for 1 minute, the intensity of the 1/2-order streaks developed in the [110]-pattern (Fig. 3(a)) and a new set of 1/3-order streaks appeared in the [1-10] pattern (Fig.3(b)). There were no 1/3-order streaks in the [110] pattern and the 1/2-order streaks in the [1-10] pattern

were very weak as compared with 1/3-order streaks. These results suggests successful formation of a 3C-SiC(001) single-crystalline film with quasi-single-domain 3x2-reconstructed structure on the on-axis Si(001) substrate.

The [100] direction of the DC current used above is tilted 45° from the surface atomic steps of the Si(001) substrate, if any. To investigate the effect of the current direction on the film growth, experiments using a current along [1-10], a direction, parallel or perpendicular to the atomic steps on Si(001) surface, have been conducted. The [110]-RHEED pattern after a post-annealing at temperatures 900-1200°C, showed fundamental spots and 1/2-order streaks. This indicates that the surface reconstruction occurs in such a way that the dimer rows are perpendicular to the current direction. Applying a reverse current ([-110] direction) gave no change in the surface reconstruction, i.e., the fundamental spots and the 1/2-order streaks without the 1/3-order streaks in the [110]-RHEED pattern. These results indicate that the formation of a 3C-SiC(001) single crystal with an almost single-domain 3x2 surface structure is formed regardless of the current directions. Although the origin for the anisotropic growth and the mechanism for the reordering of the surface are not yet understood, the technological importance of the present method that realizes the formation of quasi-single-domain 3C-SiC film on on-axis Si(001) at such a thin film thickness should be obvious.

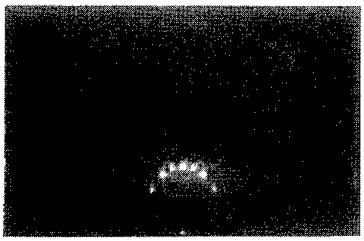


FiG.1 RHEED pattern from Si(001) (2×1)+(1×2) clean surface

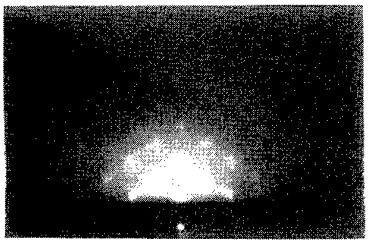


FiG.2 RHEED pattern from OS-buffer layer on Si(001)

(a) (b)

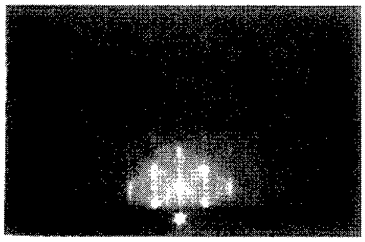


FiG.3 RHEED patterns along [110] (a) and [1-10] (b) azimuths from 3C-SiC(001) film grown on 0°-off Si(001) substrate post-annealed at above 1000°C.

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Comparison of the growth characteristics of SiC on Si between low pressure CVD and triode plasma CVD

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In order to investigate the effect of the supply of hydrogen radicals during the SiC growth, SiC films were grown on Si substrates by low-pressure thermal CVD (LPCVD) and triode plasma CVD using dimethylsilane (DMS). Activation energy for the epitaxial growth rate of SiC by LPCVD was estimated as about 90kcal/mol, whereas that by triode plasma CVD was about 45kcal/mol. Compared to the growth rate in the case of monomethylsilane (MMS), the activation energy was 20kcal/mol larger when LPCVD was used, reflecting the molecular composition, while that was about the same when the triode plasma CVD was used. Therefore, the rate-determining step for the SiC growth is considered to have been varied by supplying hydrogen radicals.

1. Introduction

Silicon carbide (SiC) is a wide band-gap semiconductor with large breakdown voltage, large saturated electron drift velocity and large thermal conductivity. Therefore, SiC has been intensively studied for the devices operating at high power, high frequency and high temperature. Among many polytypes, 3C-SiC with zincblende crystal structure can only be grown on Si substrates. Successful heteroepitaxy of 3C-SiC on Si has been achieved by atmosphere pressure chemical vapor deposition (APCVD) method at 1350°C using silanes and hydrocarbon gases after carbonization process[1]. Such a high growth temperature resulted in the generation of the residual stress (tensile) and the high-density defects such as dislocations and voids in the SiC films and in the film-substrate interface, due to large difference in thermal expansion coefficients between SiC and Si and to the high vapor pressure of Si, respectively. Therefore, lowering the growth temperature of SiC on Si is eagerly desired. Moreover, silane used for 3C-SiC growth is phyrophoric gas. Therefore, a carefully designed safety deposition system is required. Using a alternating gas supply method of SiH_2Cl_2 and C_2H_2 under low pressure after carbonization, the high quality 3C-SiC epitaxial films have been grown at 1000-1050°C[2]. The supply of hydrogen radicals without high-energy charged particles is also effective to the reduction of the growth temperature. In our previous study, the 3C-SiC films have been grown directly on Si substrates using MMS diluted with hydrogen by triode plasma CVD and LPCVD without carbonization process [3]. The organosilicon compounds such as MMS and DMS are considered to be promising candidates for the epitaxial growth of SiC because of their non-toxic and non-pyrophoric properties.

In this study, in order to investigate the effect of the supply of hydrogen radicals on the growth characteristics, SiC films were grown on Si substrates by LPCVD and triode plasma CVD using DMS.

2. Experimental

The triode plasma apparatus has a mesh grid electrode between the cathode and the

anode of a conventional diode type plasma CVD chamber, as described in a previous paper [3]. Strips cut from Si wafers ((111) just and miscut (001) 4° toward [110]) of about 8mm wide and 15mm long were used as the substrates. After evacuating growth chamber to 10^{-4}Pa, the experiment was performed. Experimental conditions are the same as the case of SiC growth using MMS, i.e. H_2 flow rate 400 sccm, DMS gas pressure during film growth 1.3×10^{-3} Pa, gas feed ratio H2/DMS=1700, substrate temperature 900-1100°C, total gas pressure during the growth 133 Pa, rf power 100 W. Hydrogen plasma was generated by an rf (13.56MHz) power source.

3.Results and discussion

Figure 1 shows the dependence of the growth rate on the growth temperature in the both cases of LPCVD and triode plasma CVD. The growth rate by triode plasma CVD was large compared with that by LPCVD in the whole temperature range of 900 to 1100°C. Activation energy for the SiC growth by triode plasma CVD calculated from the slope in this region was about 45kcal/mol irrespective of the substrate orientation. This energy was about the same as that of 43kcal/mol in the case of triode plasma CVD using MMS. On the other hand, the activation energy for SiC growth by LPCVD was 90kcal/mol. This value was 20kcal/mol larger than that in the case of MMS, and growth rate by DMS was far smaller than that using MMS below 1000°C. This difference in the activation energy considered to be due to the difference in the molecule compositions. Supplying the high-density hydrogen radicals produced by triode plasma CVD, the activation energy became small by 45kcal/mol compared with that by LPCVD. The dissociation energy of Me-SiH3 in MMS has been reported to be 85kcal/mol [4]. The activation energy for the H-desorption from the polycrystalline 3C-SiC surface has been reported to be 63 and 72kcal/mol, using temperature-programmed desorption [5]. Therefore, the high-density hydrogen radicals are considered to enhanced not only the hydrogen desorption from SiC surface but the desorption of methyl groups.

SiC films were grown even at 900°C using triode plasma CVD, while the growth was not observed in the case of LPCVD. For the SiC epitaxial growth, the growth temperature higher than 900°C is required due to the requirement of the desorption of H atoms from C-H bonds on SiC film surface [6]. From these results, the enhancement of H-desorption from SiC film surface by hydrogen radicals was confirmed.

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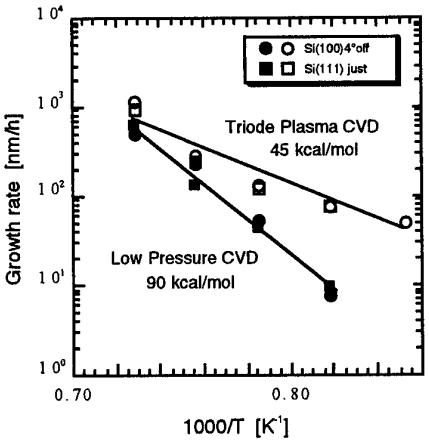


Fig. 1. Dependence of the growth rate of SiC films on the substrate temperature.

Thin film growth of 3C-SiC on Si using CH_3SiH_3 by LPCVD

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SiC is a potentially important material for as high speed, high efficiency, and high power semiconductor because of its wide band gap and its isotropic electron mobility. 3C-SiC has high electron mobility, high saturated electron drift velocity and thermal stability in the poly-type of SiC. Recently, the growth of 3C-SiC on Si substrate has been studied intensively. However, there are some problems, such as that the growth temperature is high, and the lattice mismatching of a SiC/Si interface produces defects in the grown crystal. Lower growth temperature is required because the impurity atoms diffuse into crystal at the high temperature.

In order to solve those problems, we have used monomethylsilane (MMS) as a source gas which has one atom each of Si and C in a molecule, this one source system can be simpler for both the equipment and the process than the two source gases system using silane and hydrocarbon. Growth of 3C-SiC on Si using MMS is reported in the low-temperature region [1,2].

In our study, thin SiC films have been successfully grown at the substrate temperature of 850 °C with a MMS cracking temperature of 1200 °C by very low-pressure chemical vapor deposition (LPCVD). The growth chamber was evacuated with turbo molecular and rotary pumps and was had a background pressure of 10^{-8} Torr. MMS was supplied into the cold-wall vertical CVD reactor through a cracking cell. The cracking temperature was varied from 0 to 1200 °C. The flow rate of MMS controlled by a mass-flow controller was varied from 0 sccm to 2sccm. Growth of SiC on Si(100) was conducted with 2 sccm for 3 hours and MMS pressure of 1.0×10^{-5} Torr, where thin SiC films have been grown without an initial carbonization step on Si (100).

The grown films are analyzed using auger electron spectroscopy (AES), grancing angle X-ray diffraction (XRD) and Fourier transform infrared absorption spectroscopy (FTIR). XRD pattern indicates that the grown films on Si(100) substrate is 3C-SiC under the conditions. The depth profile of the chemical composition from the surface to interface has been investigated by AES using Ar ion etching. It turns out that the growth rate of the

film was 1.5 nm/min and the C/Si ratio was about unity. The obtained SiC films are characterized by FTIR absorption spectroscopy. The strong peaks of Si-C bonds (stretching vibration) near 800 cm^{-1} and Si-H bonds (wagging vibration) near 600 cm^{-1} are observed in the IR absorption spectra [3,4] as shown in Fig.1. Si-O absorption peak is considered to be backside oxide of substrate from Attenuated total reflectance method.

As a result, absorption FTIR spectra suggest that Si-C bonds are transferred from gas to film since Si-C and Si-H bond have nearly equal binding energy.

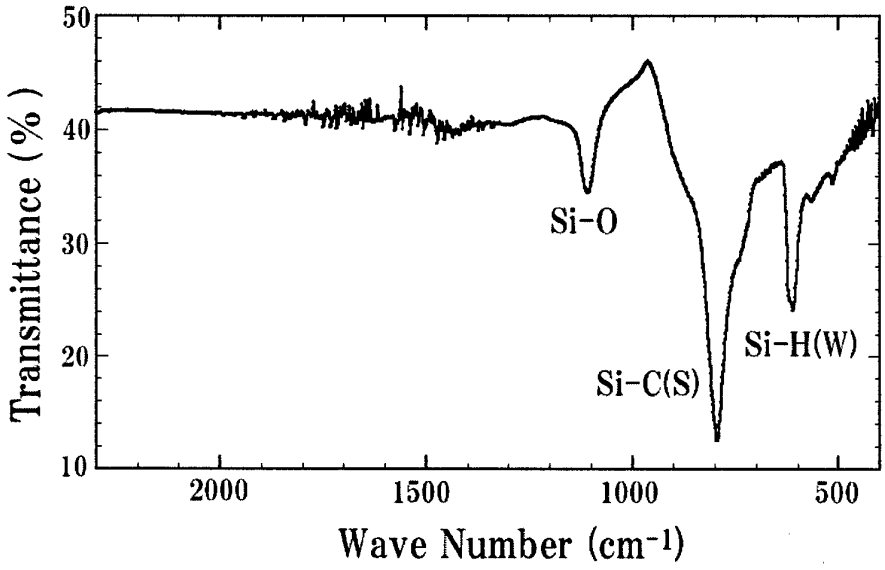


Fig.1: Absorption FTIR spectra obtained from the grown film on Si(100) at 850 °C with a cracking temperature of 1200 °C, at MMS pressure of 1.0× 10^{-5} Torr.

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The kinetic study of 3C-SiC growth on Si by pyrolyzing tetramethysilane

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The 3C-SiC has been grown mostly on Si substrates in CVD systems using the reaction of SiH_4 (or Si_2H_6) and C_3H_8 (or C_2H_4, C_2H_2) at high temperatures above 1300℃ [1]. But it is difficult to grow high quality 3C-SiC on Si because of big mismatches in lattice constants (≒ 20 %) and thermal expansion coefficients (≒ 8 %) between SiC and Si. The use of a single organosilane precursors has been investigated [2-4]. The organosilane precursors contain directly bonded Si and C atoms and decompose at relatively low temperatures. Tetramethysilane (TMS) single source have reported to grow successfully high quality 3C-SiC on Si at relatively low temperature below about 1000℃ [3-5]. However, the previous works have mainly focused on the growth and characterization of 3C-SiC films. The kinetic study should be carried out to fully understand the growth process of high quality 3C-SiC film from TMS. The kinetic data are also important for the design of CVD reactor.

In this work, we investigated the growth kinetics of 3C-SiC films on Si(111) by pyrolyzing TMS. Figure 1 shows that the SiC thickness increases linearly with the growth time with the values of 12.3, 22.9, 45.1, and 84.0 nm/min for 0.5, 1.0, 2.0, and 3.0 sccm of TMS flow rates, respectively. XRD and Raman spectroscopy indicated that the grown films is 3C-SiC(111). The growth rate increased with the growth temperature. The activation energy of the SiC growth was measured from Arrhenius plot made using the rate data measured at different temperatures (Figure 2). The measured activation energies are 72.2 and 38.16 kcal/mol in the temperature ranges of 1100 - 1250℃ and 1250 - 1420℃, respectively. QMS spectra of TMS showed that CH_3SiH_n (m/e = 42 ~ 45) and $(CH_3)_3SiH_n$ (m/e = 72 ~ 74) are major characteristic peaks for TMS with weak intensities of CH_n, C_2H_n, SiH_n, and $(CH_3)_2SiH_n$ peaks at m/e of ~15, ~26, ~30, and ~58, respectively. Figure 3 shows that with increasing the temperature, the partial pressures of hydrocarbon related species increase, while those of silicon related species decrease. On the basis of the above observation, the growth mechanism of β-SiC film in our growth system may be proposed in the following alternating reactions of gaseous Si atom and CH_3 radical. The TMS molecules are thermally decomposed to produce a gas mixture containing plenty of carbon sources and Si atoms. The CH_3 radical may adsorb on hydrogen treated clean Si surface as a carbon source. At high temperatures, the adsorbed CH_3 radical decomposes into CH_x ($x<3$) species, or comes under the attack by another $CH_3\cdot$ in the atmosphere of abundant $CH_3\cdot$ to produce the adsorbed CH_x($x<3$) species and CH_4 gas, and subsequently CH_x bond is broken by reacting with Si atom to liberate H_2 gas, leaving the formation of SiC bond. Gaseous Si atom are absorbed at hollow bridge site on C-terminated surface by surface migration or by direct arriving, forming Si terminated surface of 3C-SiC films.

Acknowledgment

This work was supported by grant No.(1999-2-114-008-5) from the interdisciplinary research program of the KOSEF.

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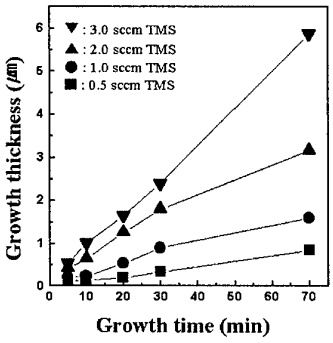


Figure 1. The thickness of 3C-SiC film as a function of growth time in terms of TMS flow rate: (▼) 3.0 sccm, (▲) 2.0 sccm , (●) 1.0 sccm, and (■) 0.5 sccm TMS flow rates. The growth was carried out at 1250 ℃ with a H_2 flow rate of 1500 sccm.

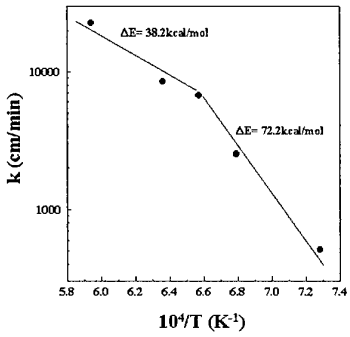
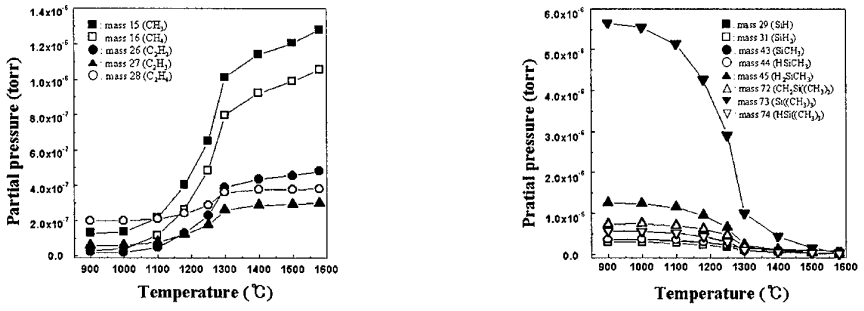


Figure 2. The Arrhenius plot of reaction rate constant, k vs. 1/T.



(a) (b)

Figure 3. The plot of partial pressures of (a) hydrocarbon related species (m/e=15, 16, 26, 27, and 28) and (b) Si related species (m/e=29, 31, 43, 44, 45, 72, 73, and 74) as a function of temperature.

Investigation of structural defects during the 4H-SiC Schottky diodes process by synchrotron topography

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In view of its excellent thermal, mechanical and electronic properties such as wide bandgap and mobility, 4H silicon carbide (SiC) is an important semiconductor material for high temperature and high power devices. The performances of the silicon carbide devices depend of the structural quality of the substrate and its purity, but, also from the process of the device. The most important structural defects in SiC crystals are misoriented domains, inclusions, macrodefects, dislocations and micropipes [1]. At the moment, these defects were found to severely limit the quality of the SiC devices. This paper is devoted to the topographic investigation of the structural defects in the substrate and those induced by the processing of Schottky diodes on 4H silicon carbide wafer.

Schottky diodes with a surface of 0.05 to 2 mm^2 were made on a 35 mm 4H-SiC wafer from CREE. The substrate was 8° off-axis. A 6 µm thick epilayer was grown using CVD technique at about 1400°C with a n-type doping. Ti was deposited and patterned on the n-type layer to realize the Schottky contact.On the backside of the substrate the ohmic contact is obtained by a full sheet metallization. Structural defects were investigated by Synchroton Topography at ESRF before any operation, after epitaxy and after metallization. Finally, some Schottky diodes were tested to do the relation between structural defects and their electrical properties.

Three techniques of Synchrotron topography were used to investigate the structural defects. White beam projection topography show the defects inside the bulk of the sample. Whereas, white beam reflection topography has the advantage to show only a small thickness at the surface of the crystal. In our case this thickness is about 20 µm. It is a very useful technique to study an epilayer. The third technique, called zebra patterns technique, consists in illuminating the crystal with a monochromatic beam, E=17keV in our case. Because of the curvature of the crystal and the narrow wavelength selected by the monochromator, only a few part of the crystal diffracts. To study the entire sample, it is necessary to turn the sample on itself. A step by step rotation gives a zebra pattern, see for example Fig 1, 2 and 3. The curvature and the structural defects can be observed by this method.

Fig 1 is a zebra pattern of the substrate before epitaxy without any other operation. The rotation between two exposures was $\Delta\omega$=0.005°. This angle and the number of the line on the image mean that the radius of the curvature is about 6 m. This topograph shows also a subgrains, indicated by an arrow on Fig. 1. The misorientation is about 30 arcsec. The complex contrast inside the circle is associated to the deformations around a micropipe.

Fig 2 and Fig 3 are zebra patterns recorded after the epitaxy and after the metallization respectively. Of course, the defects as such the micropipes and the misoriented domains remain in the crystal. A more profound analyze shows that no structural defects have been created during the process. Only the curvature radius was modified. After the epitaxy, it was about 50 m and was 11 m after the Schottky device process. The first change probably comes from an annealing phenomenon during the epitaxy. And the second one is certainly due to stress provoked by a polishing of the back face of the wafer made after the epitaxy. This polishing is necessary to obtain a good metal-semiconductor contact.

Fig 4 is a white beam reflection topograph of a part of the wafer after all the process (0001 reflections. The white spot indicated by an arrow correspond to a micropipe [2]. Smaller spots in the image are elementary screw dislocations. Because the boundary of the diodes are visible, probably due to stress introduced by the metal, we were able to locate each diode on the topography. So we made the relation between the electrical properties of the diodes and the structural defects in the wafer. We will discuss about the agreement between electrical and structural defects.



Figure 1



Figure 2

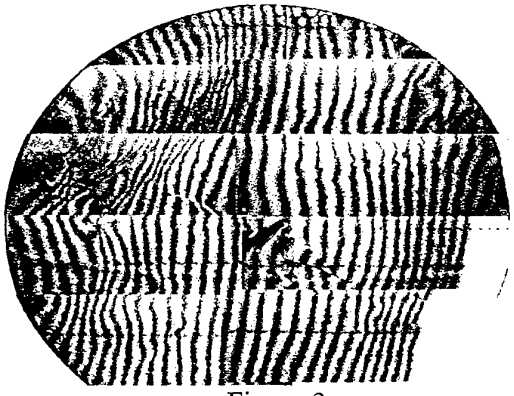


Figure 3

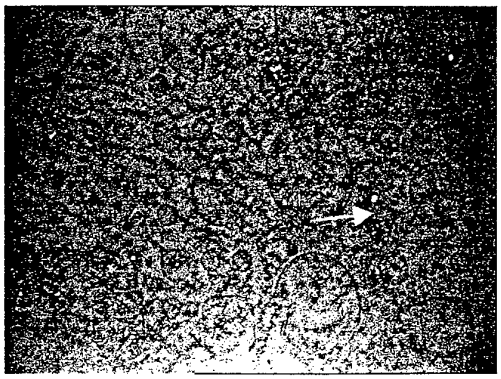


Figure 4

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Hysteresis in Transfer Characteristics in 4H-SiC Depletion /Accumulation-Mode MOSFETs

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Accumulation-mode 4H-SiC MOSFETs are being investigated to circumvent the poor inversion-layer mobility problem. In this work, we report on unusual hysteresis in transfer characteristics in n-channel depletion/accumulation-mode 4H-SiC MOSFETs. Hysteresis in transfer characteristics is observed between forward (depletion to accumulation bias) and reverse gate voltage sweeps (accumulation to depletion bias). For the reverse gate voltage sweep, the MOSFET has a positive pinch-off voltage (~7V), i.e., the depletion/accumulation-mode MOSFET is normally-off.

N-channel depletion/accumulation-mode MOSFETs have been fabricated on p-type 4H-SiC epilayers with nominal epilayer thickness and doping concentration of 10μm and $\sim 7\times10^{15}$ cm^{-3} respectively. The source/drain regions were implanted with phosphorus, and the channel region was implanted with nitrogen. The implants were annealed at 1200°C for one hour in argon. The deposited gate oxide underwent oxidation and anneals in wet and dry ambient. The channel region was implanted to a junction depth of ~0.2μm with a total dose of 1×10^{12} cm^{-2} in the wet oxide sample and 3×10^{12} cm^{-2} in the dry oxide sample.

Measurements were taken on circular geometry MOSFETs with (W/L)=8 and L=100μm. The hysteresis observed in the transfer characteristics for the forward and reverse gate voltage sweeps is shown in Fig. 1. For large gate voltages, under accumulation, the transfer characteristics for the forward and reverse voltage sweep are the same. No hysteresis was observed in the transfer characteristics on inversion-mode MOSFETs fabricated on the same chip, indicating that mobile ion contamination is not the cause of the hysteresis.

Fig. 2 shows the transfer characteristics for forward voltage sweep with different starting gate voltage. As the starting gate voltage becomes more negative, the I_D-V_G curves shift to the left and the channel pinch-off voltage is more negative. The channel cannot be pinched off for reverse voltage sweep with V_G=-30V to 70V. Similar shift in the I_D-V_G curves was also observed for reverse voltage sweeps with different starting gate voltages. For less positive starting gate voltages, the I_D-V_G curves shifted to the left (Fig. 3). For both the forward and reverse voltage sweep, the end voltage did not have any affect on the I_D-V_G characteristics. Fig. 4 compares the hysteresis observed between forward and reverse voltage sweeps at 25°C and 100°C. The pinch-off voltage is more negative at higher temperatures due to an increase in the channel doping concentration due to increasing ionization. Table 1 compares the pinch-off voltage at different temperatures; the hysteresis decreases at higher temperatures. Similar results were also obtained on depletion/accumulation-mode MOSFETs on the dry oxide sample.

The hysteresis and the shift in transfer characteristics are attributed to changes in the effective oxide charge because of changes in interface state occupancy. The interface state occupancy changes depending on the magnitude of the starting gate voltage and the direction of gate voltage sweep resulting in hysteresis in the transfer characteristics.

Acknowledgements: The authors from RPI gratefully acknowledge the support of this work by Philips Research, the Office of Naval Research under MURI Contract # M00014-95-1-1302, DARPA under contract # MDA972-98-C-0001 and NSF Center for Power Electronics Systems under award # CR-19229-427756.

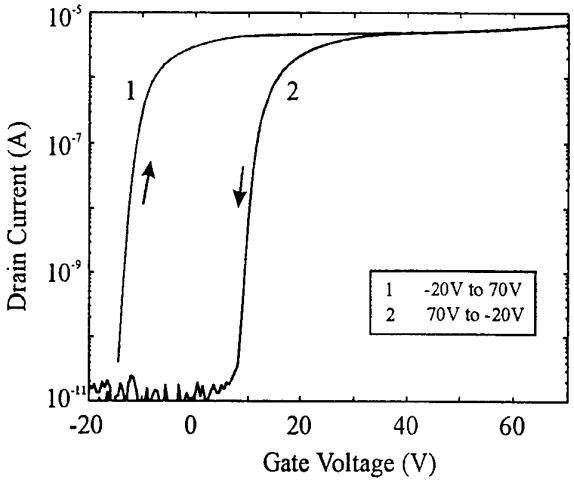


Fig. 1: Hysteresis in transfer characteristics for forward and reverse gate voltage sweeps.

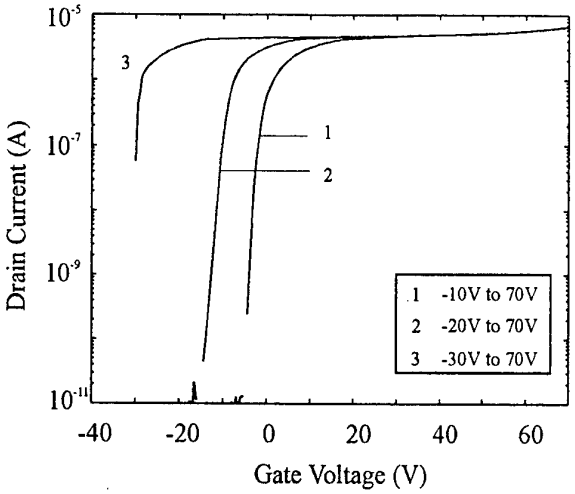


Fig. 2: Shift in transfer characteristics for different starting gate voltages in forward gate voltage sweep.

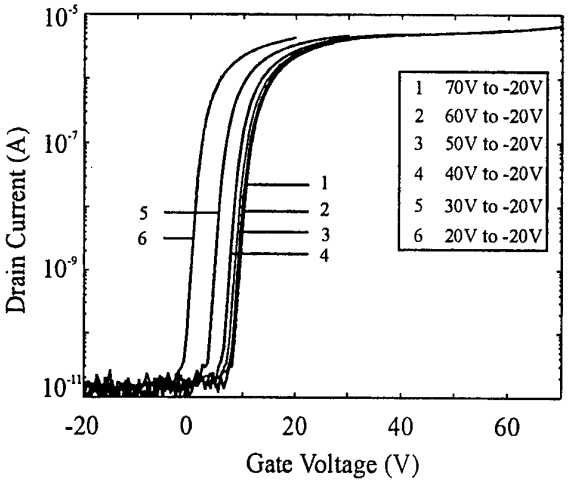


Fig. 3: Shift in transfer characteristics for different starting gate voltages in reverse gate voltage sweep.

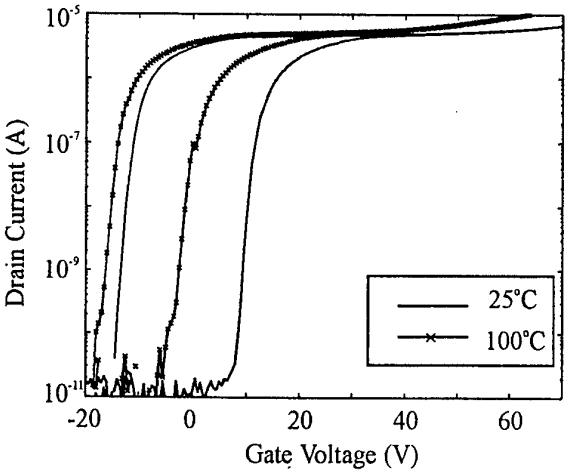


Fig. 4: Comparison of hysteresis in transfer characteristics at 25°C and 100°C.

Table 1: Comparison of pinch-off voltage between forward and reverse gate voltage sweep at different temperatures.

Temperature (°C)	$V_{P,F}$ (Forward Sweep)	$V_{P,R}$ (Reverse Sweep)	$\Delta V_P = V_{P,R} - V_{P,F}$
25	-14.5	7.0	21.5
50	-17.5	1.5	19.0
75	-18.5	-3.0	15.5
100	-17.0	-6.5	10.5
125	-17.5	-9.5	8.0
150	-18.5	-11	7.5

Depth Distribution of Lattice Damage related D_I and D_{II} Defects after Ion Implantation in 6H-SiC

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Lattice damage related defects responsible for the famous D_I and D_{II} optical emission were previously attributed to a silicon di-vacancy and a carbon di-interstitial respectively.[1,2,3] However, no clear understanding of the mechanism for their formation during implant anneal is available yet. In addition, no experimental data was reported on the depth distribution of the D_I and the D_{II} centers, which could help to better understand the mechanism for the defect formation as well as could be important from the point of view of SiC devices performance.

In this letter, the depth distribution of the D_I and the D_{II} defects that were formed by high temperature annealing of nitrogen implanted samples was investigated by etching the samples to different depths. The etching removed consequently increasing portion of the near-surface layer in which the corresponding defects resided, which allowed to use PL to probe consequently deeper in the bulk of the epilayer. The PL spectra of a sample before and after the top 0.45 microns of the material were removed by reactive ion etching are shown in Fig. 1. The intensities of the D_I lines L_1, L_2, and L_3 are still strong after the etching - as much as about 60% of what was measured from the sample before etching. This indicates that the corresponding defects penetrate well beyond 0.45 μm in the depth of the material during the defects formation. On the other hand, the D_{II} photoluminescence has completely disappeared after the etching. In order to obtain a more quantitative picture of the depth distribution of the D_I and the D_{II} defects, a group of samples was subjected to a series of RIE etches followed by PL measurements. Intensities of the D_I and the D_{II} photoluminescence normalized to their initial values before etching are plotted versus the etch depth if Fig. 2. The D_I PL did not disappear till significantly beyond the end of the ion penetration range (vertical dashed line in Fig. 2). The D_{II} PL disappeared with depth much earlier than the D_I.

The observed localization of the D_{II} PL in the region that does not extend beyond the ion penetration range indicates that there is neither a significant diffusion of the D_{II} defects themselves nor a significant diffusion of initial intrinsic defects that combine together to form the D_{II} center. More systematic "profiling" shown in Fig. 2 confirms this statement. Contrary, the D_I PL emission was still observed significantly beyond the end of the ion penetration range. This means that the distribution of the D_I centers is determined not only by the penetration depth of initial defects after the implantation but also by a higher diffusivity of the initial defects that combine together to form the D_I center during the annealing. The described difference in the distribution of the D_I and the D_{II} defects after the implant annealing in 6H-SiC will be discussed in a possible connection with the mobility of the original lattice damage defects as well as with the efficiency of their pairing to form the D_I and the D_{II} complexes.[4,5,6] Additional experiments are conducted to verify also a possible role of the different implanted species and their tendency to occupy different lattice sites during implant annealing. The pattern of the depth distribution of the

D_I and the D_{II} centers should be taken into account in studying the influence of lattice damage defects on the performance of SiC devices.

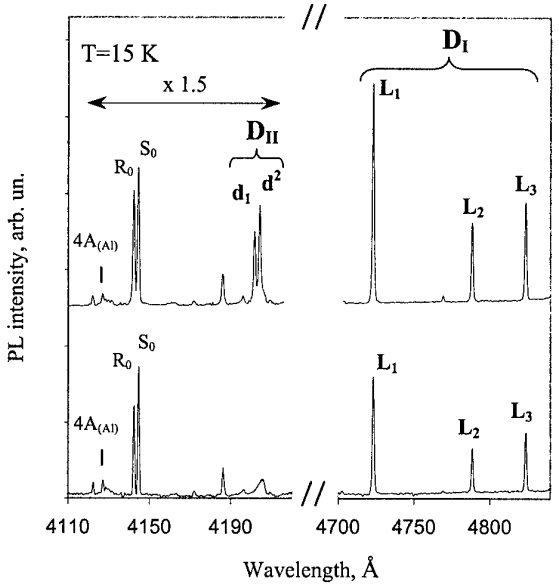


Fig. 2 PL spectra of a nitrogen implanted and annealed sample before (top) and after (bottom) 0.45 μm etch. At this depth, intensities of D_I lines are still very strong, while D_{II} PL is completely disappeared.

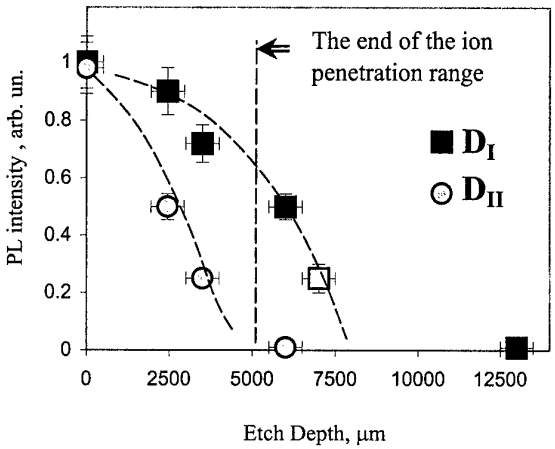


Fig. 2 Normalized PL intensity of $D_I(L_1)$ and $D_{II}(d_1)$ defect lines measured after a few consecutive etches of the surface of a SiC sample. D_I PL could still be observed even after the sample was etched beyond the end of the ion penetration range. The empty square was measured on a different sample.

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Influence of Junction Potential Distribution on Effective Impurity Ionization Time Constants in SiC for Admittance Spectroscopy Data Analysis

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Thermal admittance spectroscopy is a useful tool which allows one to obtain important information, such as activation energy and capture cross-section, about impurity levels in semiconductors [1-7]. Admittance spectroscopy was extensively used to find the activation energies of technologically important SiC impurities [4-7]. The technique is based on a strong dependence of the semiconductor junction differential admittance on the temperature and measurement ac signal frequency in the case of a semiconductor with an incompletely ionized impurity. The real part of the junction admittance, the conductance, exhibits a peak in its temperature dependence when the impurity ionization time constant is comparable with the ac measurement signal period. The imaginary part of the admittance, the capacitance, has an inflection point in the same temperature range.

In most variants of the admittance spectroscopy technique the natural logarithm of the measurement frequency is plotted versus the corresponding conductance peak positions on a $1/T$ scale. The resulting Arrhenius plot is then approximated by a straight line whose slope is proportional to the impurity activation energy and intercept determines the capture cross-section. Linearity of the Arrhenius plot follows from a rather simplified assumption of proportionality of the measurement signal frequency and the average impurity emission coefficient, for which the conductance has a peak, with the proportionality coefficient being either equal to 1 [Ref. 1] or equal to 2 [Ref. 2]. In a recent paper [8] we showed that this proportionality coefficient depends on the impurity ionization probability in the semiconductor bulk and on the junction potential distribution. These factors lead to the nonlinearity of the Arrhenius plot. The impurity ionization probability depends on temperature and impurity atom concentration, while the potential distribution additionally depends on the measurement signal parameters. In the Ref. [8] we derive an equation which describes the influence of the impurity occupation in the semiconductor bulk on the effective impurity time constant. In the present work we investigate the influence of the junction potential distribution on the effective impurity time constant. Using our general model of the junction admittance [9] we show that the proportionality coefficient between the impurity ionization time constant and the emission coefficient is a strong function of the potential distribution, which is important to take into account in the Arrhenius plot analysis.

Junction admittance is proportional to the space charge region charge change in response to a bias change. The proportionality coefficient, or the susceptibility function, is a complex quantity, which reflects the delayed response of the impurity ionization processes to bias changes. Obviously, this delay causes the junction potential to be complex as well. Junction conductance is proportional to the imaginary part of the integral over the space charge region of the product of the potential and the susceptibility function. Traditional analysis takes into account only the real part of the junction potential. However, calculations show that the product of the imaginary part of the potential and the real part of the susceptibility function may be comparable to the product of the real part of the potential and imaginary part of the susceptibility function;

these two products have opposite signs. Since conductance is determined by the sum of these products, it may differ greatly from the value of conductance predicted by the traditional analysis. This statement is illustrated by Figure 1. On this figure, integrals of the cross-products of the real and imaginary parts of the potential and susceptibility function and their sum are plotted versus temperature for N-doped 6H-SiC (the activation energy is taken equal to 0.14 eV, which corresponds to two k-sites).

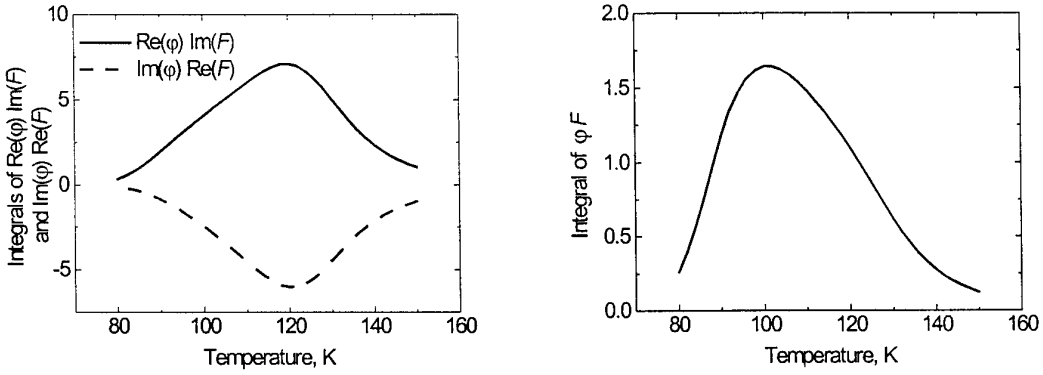


Figure 1. Components of the product of the junction potential φ and the susceptibility function F in N-doped 6H-SiC. E_A=0.14 eV, N=10^{16} cm^{-3}, σ=2.7×10^{-16} cm^{-2}, ω=4π×10^4 Hz.

The product of the real part of the potential and the imaginary part of the susceptibility function has a maximum at about 120 K. At this temperature, in accordance with the traditional theory, the impurity emission rate is approximately equal to half the measurement frequency. However, the other product also has an extremum at about the same temperature, and the sum of the two is maximal at a significantly lower temperature of 101 K, where the emission rate is 18 times smaller than at 120 K. Thus, neglecting to take into account the potential distribution in Arrhenius plot analysis produces erroneous values of impurity activation energy and capture cross-section.

We report on a detailed analysis of the impurity time constant behavior in SiC as a function of impurity parameters (activation energy and concentration) and experimental conditions (temperature, bias frequency and amplitude).

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Radiation Induced Defects in p-type Silicon Carbide

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Introduction

Single crystalline silicon carbide (SiC) is expected to be an excellent material for making high power electronic devices used under severe environment such as intense ionizing radiation field with high temperature. There is considerable interest in the mechanism of radiation damage in electronic semiconductor devices, which can be operated under intense ionizing radiation field. Therefore it is necessary to understand the characteristics of the radiation damage and annealing properties of the defects. However, only a little has been known about radiation induced defects in p-type SiC. In this study, we have performed electron spin resonance (ESR) measurements of p-type 4H and 6H-SiC irradiated with reactor neutrons or high-energy electrons.

Experimental

The samples used in this study were obtained from Cree Research Incorporation. The carrier density of Al-doped p-type 4H and 6H-SiC used in the present experiment was the order of $10^{18}/cm^3$. The irradiations were performed at the low-temperature irradiation loop facility (LTL) of the Kyoto University Research Reactor Institute (KUR) and the electron linac (LINAC) of the KUR. At the LTL, SiC samples were irradiated with the fast neutron fluence of $6\times10^{16}n/cm^2$. The LINAC was operated under the following conditions: accelerating voltage; 22 or 30MeV, pulse width; 3μs, repetition; 30pps, and peak current; 500mA (average current about 40μA). The neutron fluence was monitored by the activation method with Ni foils. Isochronal annealing was performed in the temperature range between 100℃ and 1500℃ for 5 minutes in helium atmosphere. Electron spin resonance (ESR) spectra were measured at room temperature (RT) and liquid nitrogen temperature (LNT) with an X-band (9GHz) microwave incident on a TE_{110} cylindrical cavity using the JEOL JES-TE200.

Results and discussion

Figure 1 shows ESR spectra at (a) RT and (b) LNT for electron(22MeV)-irradiated p-type 4H-SiC with 10^{18} n/cm^2. The ESR signals termed K1(Vsi), K12, K11(Vc), K1(Vsi) + K13 and K14 are observed. The K1 and K11 signals are similar to those for silicon vacancies and carbon vacancies found in electron-irradiated 3C-SiC(T1 center)[1], 6H-SiC(PA center)[2] and 3C-SiC(T5 center)[3], 6H-SiC(PB center)[4], respectively. The K12 center observed at the room temperature appears at low dose irradiation. The K1(Vsi) + K13 center, which are overlapped each other, observed at LNT appears remarkably at low dose. Moreover, the K14 center observed at LNT is a radiation-induced defect, which was produced in the early stage of the irradiation. These defects change when the irradiation advances, and then these centers decrease. The K1(Vsi) becomes predominant when it is irradiated with electron(22MeV) fluence up to $3\times10^{18}n/cm^2$. In this case, the behavior of the K1, K2, K3, and K4 centers is similar with that observed on the n-type SiC on which we have reported previouslly[5]. Finally, K11(Vc) center is not observed with the high dose irradiation. Figure 2 shows the fluence-dependence of the K1(Vsi) and K11(Vc) centers. As

shown in this figure, the carbon vacancies decrease though the silicon vacancies increase with the irradiation. It is necessary to consider about the influence on the defect generation by electronic excitation under the irradiation.

Isochronal annealing behavior of the K1(Vsi), K12, K11(Vc), K1(Vsi) + K13 and K14 signals is shown in Fig.3. An almost part of the K1(Vsi) center disappears at 700℃ and the K11(Vc) center at 300℃. An almost part of the K12 center disappears rapidly at about 400℃. After the K1(Vsi) center disappeared, the K1(Vsi) + K13 center disappears at about 1,200℃ following it reached to its maximum at about 900℃. The K14 center disappears at about 1,200℃ after reached to the maximum intensity at around 900℃.

From these facts, these defect centers are thought to be due to compound defects, which relate with the silicon vacancy.

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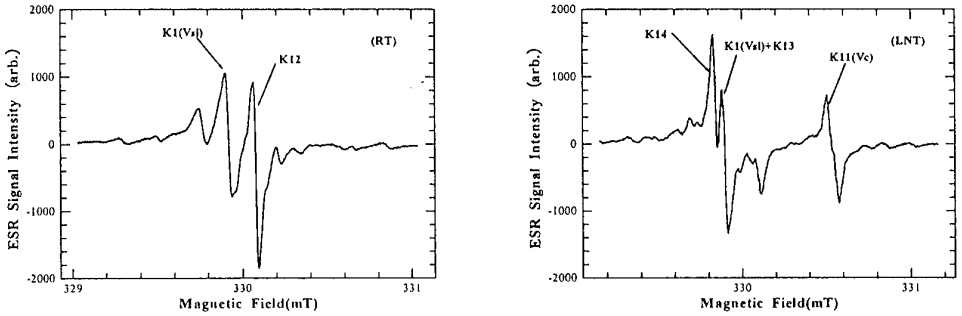


Fig. 1 ESR spectra observed at (a) RT and (b) LNT for 22MeV electron-irradiated p-type 4H-SiC.

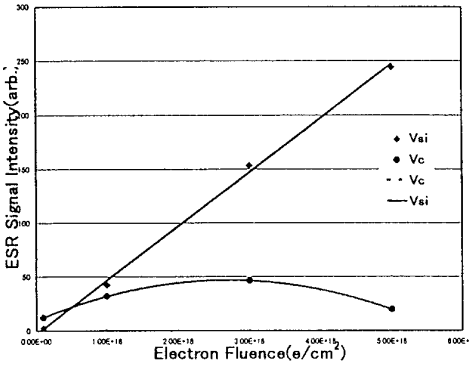


Fig. 2 The ESR signal intensities of K1(Vsi) and K11(Vc) centers in p-type 4H-SiC irradiated with 22MeV electrons as a function of the fluence.

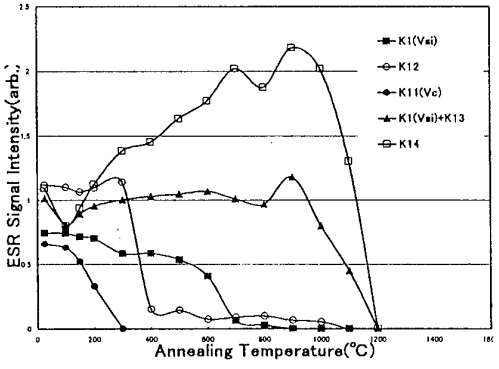


Fig. 3 Isochronal annealing behavior of the ESR centers introduced in p-type 4H-SiC by 22MeV electron irradiation.

Electrical Properties in Neutron-Irradiated Silicon Carbide

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Introduction: Silicon carbide (SiC) single crystal is expected as high power electronic devices used under severe environment such as intense ionizing radiation field with high temperature. However, the mechanism of radiation damage in electronic semiconductor devices, which can be operated under intense ionizing radiation field, has not been understood yet. Therefore, it is necessary to understand the characteristics of the radiation damage and annealing properties of the defects. In the present paper, we describe for electrical characteristics of n-type SiC irradiated with reactor neutrons.

Experimental arrangement: The SiC single crystal used in this study were manufactured by Nippon Steel Corporation. These SiC wafers were nitrogen-doped and the carrier densities were the order of $10^{18}/cm^3$ and $10^{19}/cm^3$. Ohmic contacts were made on each n-type SiC wafer by evaporating Ni dots followed by annealing at 1,100℃ for 30 minutes in Ar atmosphere.
The neutron irradiations were carried out using the low-temperature irradiation loop facility of Kyoto University Reactor(KUR-LTL). The irradiation in the LTL was carried out with the fast neutron fluence of $6\times10^{17}n/cm^2$ at 50K and 100K.The neutron fluence was monitored by the activation method using Ni foils.

The measurements of resistivity and Hall effect on n-type SiC were carried out at RT by the Van der Pauw method. Isochronal annealing of the irradiated samples was performed in the temperature range between 373K and 823K for 5 minutes in Ar atmosphere.

Results and discussion: It is well known that the electrical resistivity increases with fast neutron fluence. Though various factors are relative about how to increase the electrical resistivity, an initial carrier density of SiC would be favorable candidate.

Figure 1 shows the changes of electrical properties after the neutron irradiation as a function of the initial carrier density in n-type SiC. In this figure, the change rate of mobility becomes large with increasing of the initial carrier density, while that of the electrical resistivity small. On the other hand, the change rate of the carrier density is almost fixed.

Figure 2 shows the relation between the carrier density and mobility before and after the irradiation of the neutron. After neutron irradiation, the carrier mobility increases with the carrier

density, though the mobility has decrease according to increase the carrier density before the neutron irradiation. This is thought as follows; the donor decreases by the irradiation and consequently the ion scattering decreases. In any case, these results show that it is necessary to consider scattering with impurities.

The results of the isochronal annealing experiment are shown in Fig.3. The results indicated that the resistivity and the mobility were annealed at two recovery stages (350K, 500K) and that the carrier density did not change by the isochronal annealing up to 823K. The resistivity was recovered about 40% due to 823K annealing. These results contradict from the following experimental expectation; i.e. usually the carrier density recovers by a thermal annealing.

From these facts, these experimental results can be concluded to influence by the existence of a large amount of donor.

This work has been carried out in part under the Visiting Researcher's Program of the Research Reactor Institute, Kyoto University.

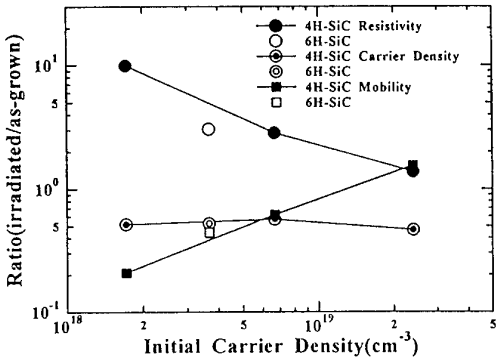


Fig.1 Changes in electric properties after neutron irradiation as a function of initial carrier density.

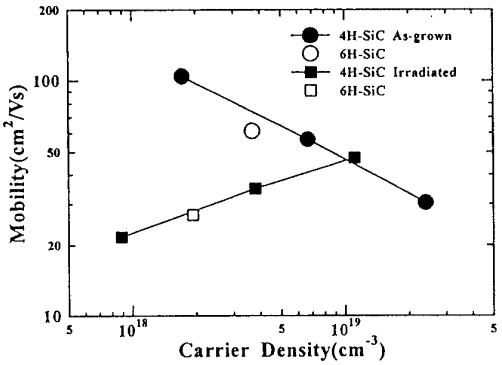


Fig.2 Carrier mobility as a function of carrier density.

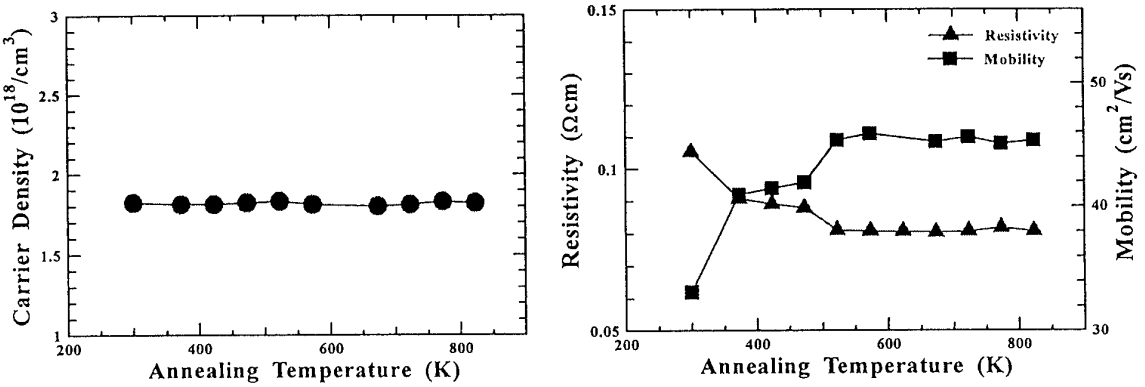


Fig.3 Isochronal annealing results of neutron-irradiated SiC.

SIMS analyses of SiO_2/SiC interface

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Establishment of reproducible and reliable control of SiO_2/SiC interface was main issue for application of SiC to a power MOSFET. The detailed discussions of the SiO_2/SiC interface are expected to open a new approach to make an applicable gate insulator for an SiC power MOSFET. In this paper, Secondary ion mass spectrometry (SIMS) analyses was undertaken to investigate the SiO_2/SiC interface.

4H-SiC(0001) off-cut wafer 3.5° toward <1120> was used as the substrate for epitaxial growth of 4H-SiC(0001) films. N-type epitaxial film with nitrogen dopant was grown using the vertical hot-wall-type chemical vapor deposition (CVD) system.[1] The surface of the epitaxial film was cleaned by the sacrificial oxidation procedure prior to the formation of SiO_2 insulator film. Then the SiO_2 insulator film on the surface of the cleaned epitaxial film was formed by thermal oxidation with or without post-oxidation annealing(POA). Detailed SIMS analyses were undertaken upon three different samples of SiO_2 insulator layers formed by (a)3-hours wet oxidation at 1100℃, (b)3-hours wet oxidation at 1100℃ followed by 3-hours POA at 900℃ and (c) 40-minutes wet oxidation at 1190℃. Depth profiles of carbon were measured using SIMS. Carbon composition was normalized as those in SiC fit to 100% in the following SIMS analyses. Background of carbon in these SIMS measurements was less than 0.5%. The SiO_2/SiC interface transition region, where carbon composition increased from 16% to the main component of SiC (84%), was observed as thin as 4.0 ～ 5.4 nm in our SIMS measurements including the apparatus limit of the depth resolution.

SIMS profile of the sample (a) shows the largest SiO_2/SiC interface transition thickness of 5.4 nm. The SiO_2/SiC interface of sample (a) includes carbon rich transition layer whose carbon concentration is 10% larger than the other two samples. Uniform carbon concentration of 2% is observed although the SiO_2 film of sample(c). While the carbon concentration at the SiO_2 surface of sample(b) is in background range, the closer the carbon concentration in the SiO_2 film gets to the SiO_2/SiC interface, the larger it becomes up to 1%.

Oxidization forming SiO_2 film on SiC leaves residual carbon flux at the SiO_2/SiC interface. The POA procedure accelerates diffusion of the residual carbon from the SiO_2/SiC interface to the surface through the SiO_2 film. High temperature oxidation can diffuse the residual carbon at the SiO_2/SiC interface during oxidation while a few % carbon concentration remains in the SiO_2 film.

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Electroluminescence Analysis of Al^+ and B^+ Implanted pn-Diodes

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Abstract: Since pn junction is used in pn diode, edge termination in SBDs or channel formation in FETs, the reduction of leakage current in pn junction is one of the key issue to realize SiC devices. We have fabricated 4H-SiC pn diodes by Al^+ or B^+ implantation into n-type epitaxial layers. The electroluminesence(EL) is effective to obtain information of transition between donors, acceptors and defects[1][2]. We have measured EL spectra for these pn diodes with high leakage currents and those with low leakage currents. Diodes with low leakage current showed steep increase with current injection in 390nm peak compared to that from donor acceptor pair (DAP) recombination, whereas the diode with high leakage current showed a relatively slow increase in 390nm peak. We speculate that recombination through DAP or defects is the reason of high leakage current and small band-edge EL peak.

Experiments:

4H SiC wafers were used in this work. Low doped n-type epitaxial layers were grown by hot wall LPCVD[3]. SiO_2 layer was formed by oxidation. Al^+ or B^+ was implanted to form p-type layer in n-type epitaxial layer, followed by high temperature activation annealing. Ni was sputterd for backside ohmic contact, followed by annealing. Contact holes were opened in SiO_2 layer. Al and Ti layers were sputterd subsequently, followed by annealing at 900℃ to obtain ohmic contact to p-type layer. Current-Voltage characteristics were measured by HP4142B. EL spectra were measured at room temperature by Multi Channel Photo Detector (MCPD-1000).

Fig. 1 shows EL spectra of Al doped pn diodes with (a) low leakage current and those with (b) high leakage current. At lower voltages 480nm peak was dominant, and by increasing bias voltage a rapid increase in 390nm peak was observed in EL spectra for Al doped diodes. Diodes with low leakage current showed steep increase in 390nm peak, whereas the diode with high leakage current showed a relatively slow increase in 390nm peak.

EL spectra of B doped pn diodes with (a) low leakage current and those with (b)

high leakage current are shown in Fig. 2. Two peaks around 530nm peak and 780nm were observed for B doped diodes at low injection current. By increasing the current injection 390nm peak appeared. Diodes with low leakage current showed steep increase in 390nm peak compared to those with high leakage current, which showed a relatively slow increase in 390nm peak and and higher 780nm peak than 530 nm peak.

Peak around 400nm is attributed to free to bound transitions[2]. The peak around 480nm is assigned to DAP recombination involving the nitogen donor and a deep acceptor level[3]. The peak around 500nm is attributed to DAP from the nitrogen donor and the deeper boron acceptor[3]. And peak at 514nm is attributed to optical transitions of conduction electrons to neutral deep B acceptor.[2] We speculate that the red peak correlates with the origin of high leakage current.

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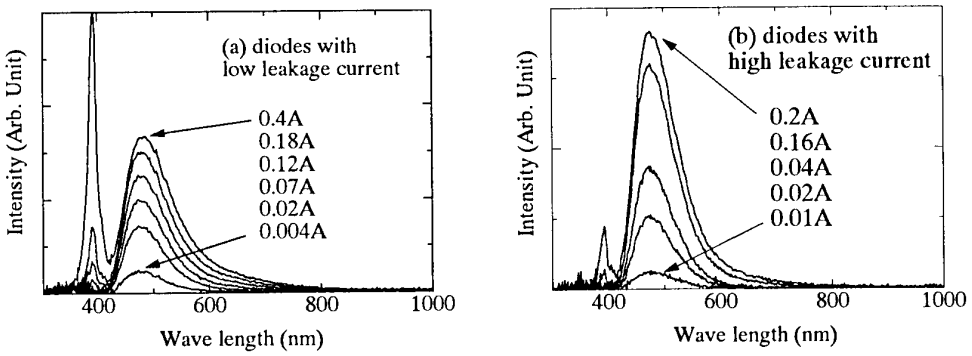


Fig. 1, EL spactra of Al doped pn diodes

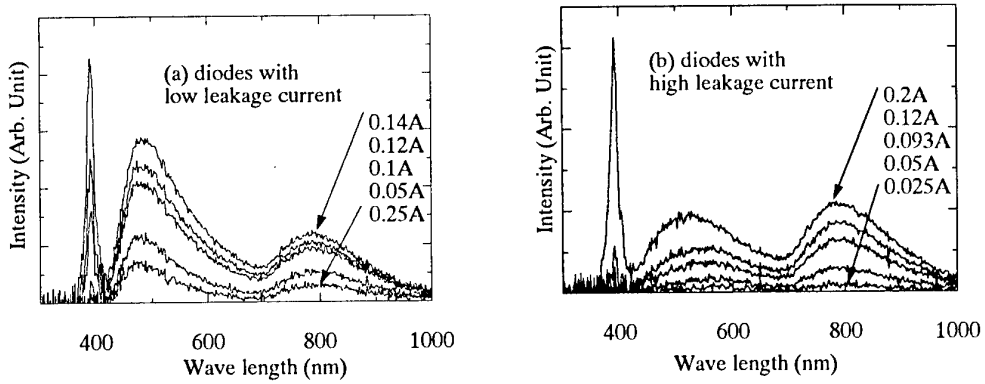


Fig. 2, EL spactra of B doped pn diodes

ON THE LOCATION OF ER ATOMS IN IMPLANTATION DAMAGED SIC BEFORE AND AFTER ANNEALING

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Ion implantation for doping of SiC has attracted increasing attention and it is known that annealing is necessary both to remove the implantation damage and to electrically activate the dopants [1]. Ion-implantation as a method for nanostructure fabrication within SiC [2] has the advantage over other methods that nanocrystals can be created in a well-defined matrix. In the latter case the dose has to be about three orders of magnitude higher (about $10^{17}cm^{-2}$) and therefore the process is accompanied by excessive matrix damage [3]. The control of defect-enhanced diffusion during annealing is thought to be the key both to an understanding of distinct doping related defect levels in SiC and to a successful implantation-based nanostructure technology.

6H and 4H-SiC(0001) was implanted with 400keV Er ions to a dose of $1x10^{17}cm^{-2}$ at 700°C, followed by rapid thermal annealing at 1600°C for 3min under Ar atmosphere. Cross-sectional samples before and after annealing were prepared for transmission electron microscopy (TEM) using mechanical polishing, dimpling and low-angle Ar-ion milling and in one case just by tripod polishing. Conventional and high-resolution (HR) TEM was carried out in a JEOL 3010 and atomic-resolution high-angle annular dark-field scanning TEM (ADF-STEM) in a FEG-JEOL2010 equipped with electron energy loss spectrometer (EELS).

TEM and EDX-analysis on as-implanted specimen show that the most strained SiC region contains the region of Er content shows that Er is not clustered there but statistically distributed within the SiC matrix. Prevailing defects are interstitial loops in basal planes. After annealing, it was revealed by atomic-resolution ADF-STEM that single Er atoms collect and that there are at least 3-5 single Er atoms in one column. Together with strain analysis on HRTEM images it can be followed that the foreign atoms place preferably in the core of lower strain of SiC matrix defects. Fig. 1 shows one typical defect in atomic resolution Z-contrast and in high-resolution contrast. The chemical nature of the atoms confirmed EELS by scanning along a single Er atom column (see Fig. 1). Typical locations of Er atom columns will be described and their connection to $ErSi_2$ nanocrystal creation will be discussed. Moreover wider conclusions will be made to the case of Ge ion implantation.

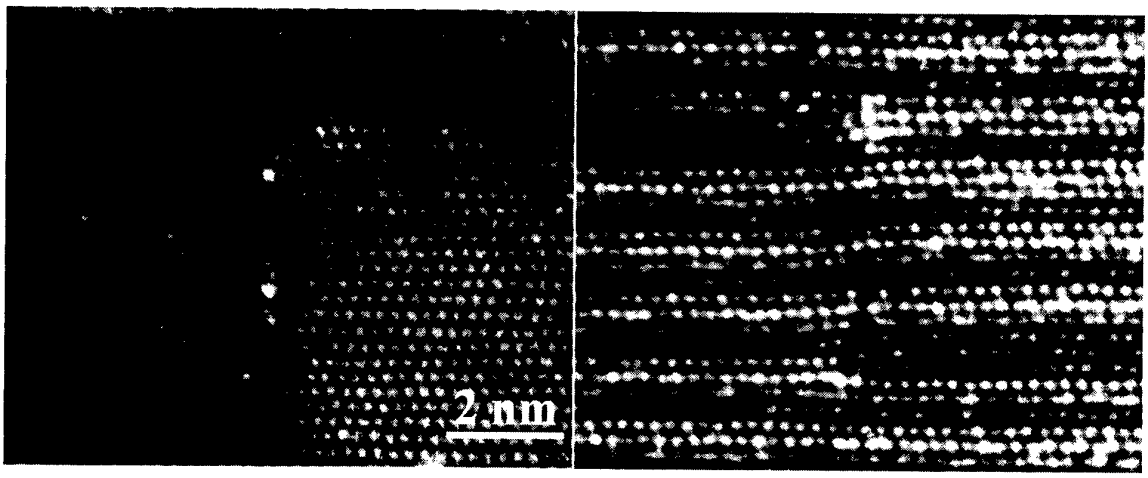


Fig. 1 Atomic-resolution ADF-STEM image showing Er atom columns at the ends of interstitial loops on the left and a corresponding defect imaged in HRTEM.

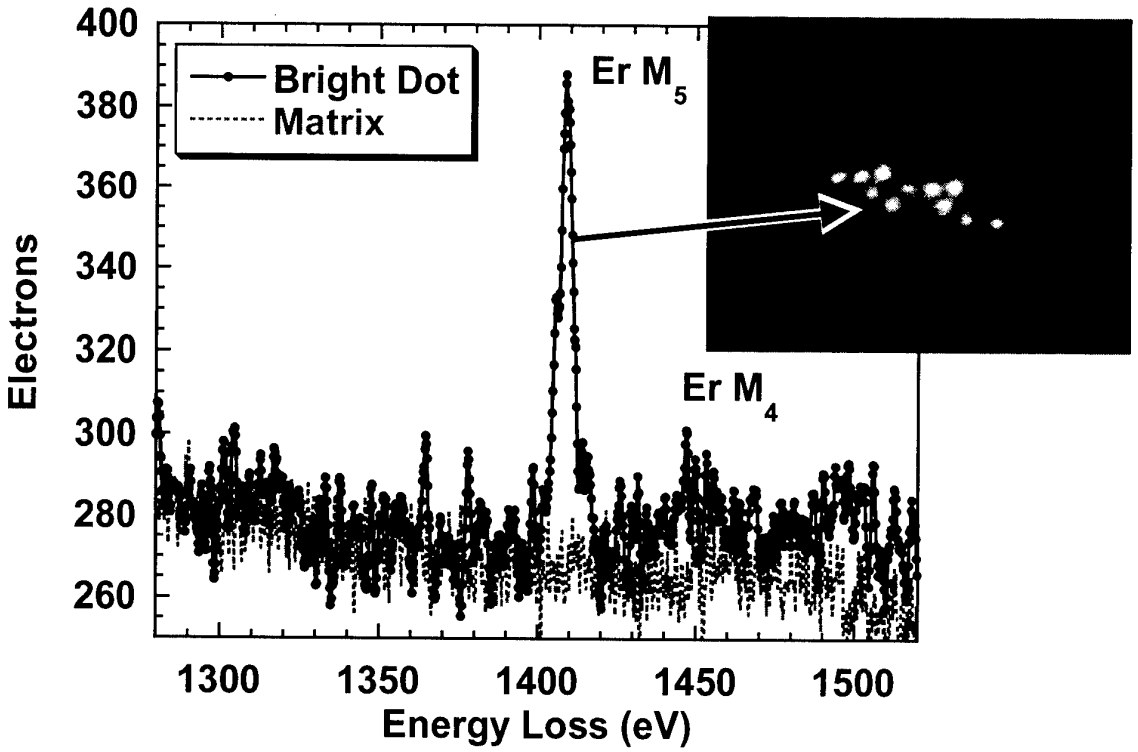


Fig. 2 A typical SiC matrix defect decorated by Er-atom columns together with the EELS spectrum of the Er M edge obtained from the single Er atom column, the arrow is pointing to.

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Direct Observation of the Solid Phase Recrystallization of Self-Implanted Amorphous SiC Layer on $(11\bar{2}0)$, $(1\bar{1}00)$, and (0001) Oriented 6H-SiC

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1. Introduction

The ion implantation method is used for selective doping in SiC device formation. In order to remove defects induced by ion implantation into the (0001) Oriented 6H-SiC , that is carried out at the substrate temperature over 500 °C, additional addition annealing is necessary at the high temperature above 1500 °C.[1] Satoh showed that the solid phase growth process is dependent on the crystal orientation.[2] It is clear that information of this type is essential to an understanding of the mechanism in which ion-inplantation induced defects disappear. The present paper discusses the substrate orientation dependence on the kinetics of furnace-annealing induced solid phase recrystallization (SPR) of self-implanted amorphous layers on SiC substrate. We report on the use of an *in situ* time resolved optical reflectivity (TROR) measurement to monitor the position and roughness of the amorphous-crystal interface in real time.

2. Experimental

Samples of n-type ($N_D - N_A \simeq 10^{17}/cm^3$) $(11\bar{2}0)$, $(1\bar{1}00)$, and (0001) oriented 6H-SiC were ion implanted with Si (40 keV 1.5 $\times 10^{15}/cm^2$ + 80 keV 2 $\times 10^{15}/cm^2$ + 110 keV 5 $\times 10^{15}/cm^2$) and C (20 keV 1.5 $\times 10^{15}/cm^2$ + 40 keV 2 $\times 10^{15}/cm^2$ + 60 keV 4 $\times 10^{15}/cm^2$) to create an self-implanted amorphous layer ($\sim$ 150 nm) on the wafer surface. Figure 1 shows the Si and C depth profiles calculated by TRIM program. Furnace induced SPR was accomplished on the resistively heated stage at 700 °C in air environment. The recrystallization kinetics was observed by the TROR technique.[3] The TROR signals provides a continuous, and sensitive measurement of a position and roughness of amorphous-crystal interface during SPR. A He-Ne laser (λ = 633 nm) is used for the probe light.

3. Results and Discussion

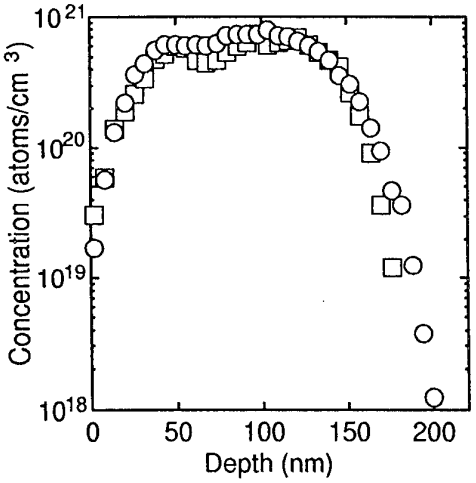


Fig. 1. Calculated profiles using TRIM of Si (○) and C (□).

In the TROR technique, oscillations of the reflectivity signal, due to interfering optical reflections from the surface and from the moving interface between the surface amorphous layer and the recrystallized SiC, are observed. Figure 2 shows a calculated reflectivity of amorphous SiC as a function of amorphous thickness on crystal SiC. Amorphous and crystalline SiC indices used in the calculation are $4 - 0.612i$ and $2.63 - 1.2 \times 10^{-5}i$, respectivery.[4] A complex reflective index of amorphous SiC was estimated by the comparison with the reflectivity of the silicon.

Figure 3 gives the shape of the TROR signals in each case for all orientations $(11\bar{2}0)$, $(1\bar{1}00)$, and (0001). In the $(11\bar{2}0)$ orientation, the TROR signal is closed to the calculated curve in comparison with Fig. 2. By comparison of the TROR signal and the calculated curve, the interference maxima and minima are assined at the depth of interface. The recrystallization rate estimated to be about 3.9 nm/min near initial amorphous-crystal interface. When the growth interface reached near the sruface, TROR signal shows attenuation of the last reflectivity oscillation. It is shown that the roughness of the growth interface increases with the recrystallization from amorphous phase to crystal phase. Comparing the $(1\bar{1}00)$ orientation growth with the case of $(11\bar{2}0)$, the recrystallization rate is late, and it estimated to be about 2nm/min. In addition to this property, the oscillation of the reflectivity observed around the surface has collapsed. It seems that whether the SPR stopped near surface layer or roughness of the regrowth interface increasea severely. In the case of the (0001) orientation, the TROR oscillation nearly disappears, which shows a very rough regrowth interface induced by furnace annealing. We obserbed directly that the recrystallization interface was greatly roughend during annealing process of ion-implantation induced amorphous layer in the (0001) orientation SiC.

In conclusion, we have succeeded the observation of the recrystallization process of SiC amorphous layer using the *in situ* TROR technique, that strongly depends on the crystall growth orientation.

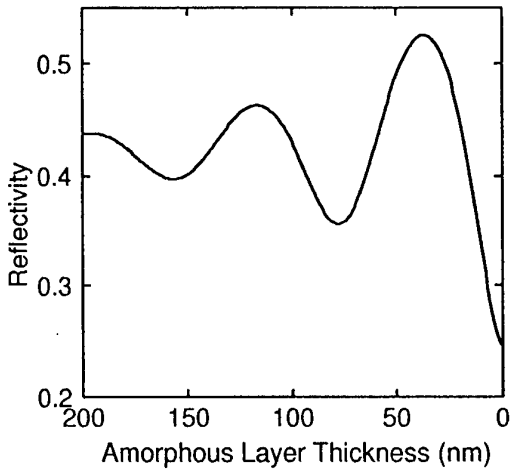


Fig. 2. Calculated reflectivity of amorphous SiC on crystal SiC as a function of amorphous layer thickness.

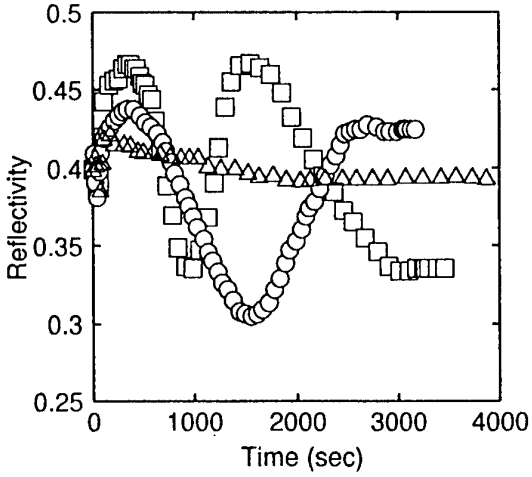


Fig.3. The TROR signals during SPR on $(11\bar{2}0)(\square)$, $(1\bar{1}00)(\circ)$, and $(0001)(\triangle)$ oriented 6H-SiC.

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Photoemission electron imaging of transition metal surface on Si and SiC

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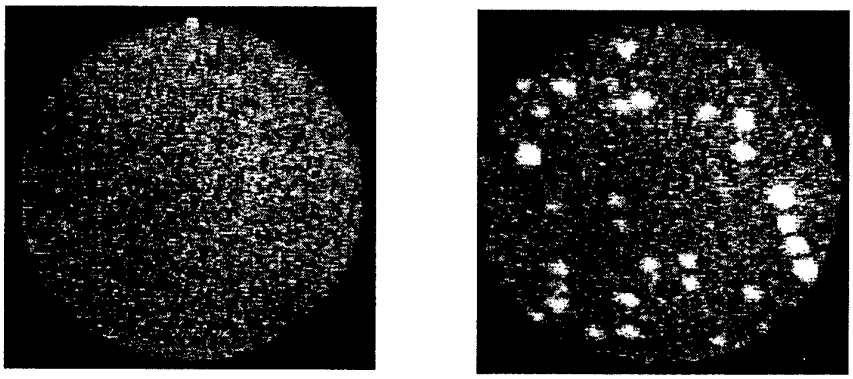
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The introduction of ultra-high-vacuum (UHV) technology in emission microscopy had made photoemission electron microscopy (PEEM) a high-resolution surface-sensitive technique for the study of surface structures. The image in the PEEM system is based on the lateral photoemission intensity distribution from a solid sample surface. The contrast mechanisms of PEEM such as topographical, elemental, chemical, magnetic, and orientation contrasts allowed a real-time view on surface reactions such as islanding and agglomeration of metals as well as their dynamics. In this study, we have conducted a real-time imaging on the annealed surfaces of transition metal films on Si and SiC surfaces and have studied the morphological variations after in-situ annealing.

Thin metal films (1nm, 2 nm, 4 nm, 10 nm, and 50 nm) of Ti, Ni, and Pd were deposited either on Si or SiC and annealed inside the PEEM chamber at ~10^{-9} Torr by filament heating and electron bombardment. The images were taken after sequential annealing from RT to over 900 °C.

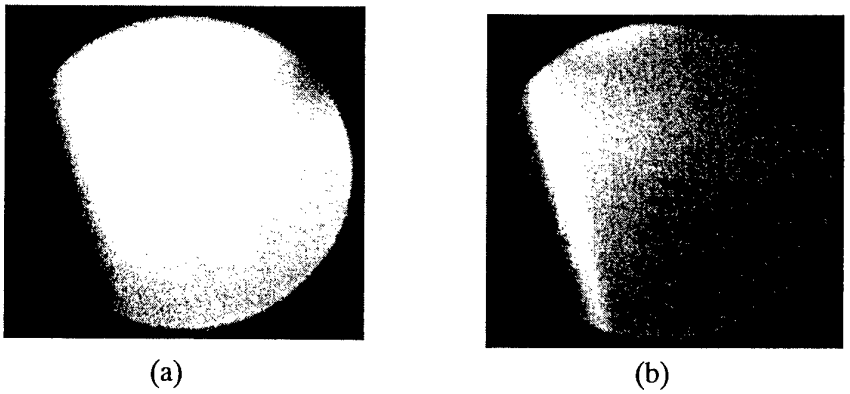
The PEEM system uses either high-pressure Hg arc lamp or synchrotron radiation for photoelectron emission and is attached to beamline BL-5 of Hiroshima Synchrotron Radiation Facility (HiSor), Hiroshima, Japan. The resolution of the system is about 15 nm and the field of view (FoV) can be varied from 2 μm to 150 μm.

We have imaged the formations of metals-nanostructures on Si and SiC surfaces, initial surface reactions as well as formations of islands (in ring-clusters) with sizes in order of microns. Also we have observed variations of brightness at elevated temperatures and contrast-reversal on some films that were due to deoxidation of the surface films and/or formation of reacted products such metal silicides and carbides/graphite. Figure 1 shows PEEM images of Ti on Si(100) surface at RT and after annealing at 700°C which is the formation temperature of Ti silicides. And Figure 2 shows Ni surface on 3C-SiC at (a) 200° and (b) 240°C.



(a) (b)

Figure 1. PEEM images of Ti (40nm)/Si(100) taken at (a) RT and (b) after 700°C.



(a) (b)

Figure 2. PEEM images of Ni (4nm)/3C-SiC taken at (a) 200 °C and (b) 240°C.

HOLE ESCAPE FROM $Ga_{1-x}In_xN$/GaN QUANTUM WELLS AND InAs/GaAs QUANTUM DOTS.

V.A. Voïtenko

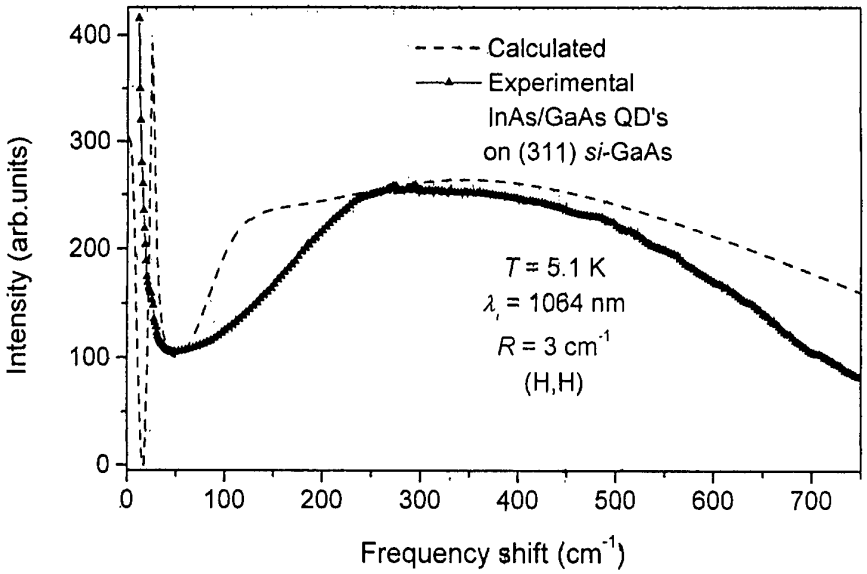
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It is shown clearly the anomalous photoexcitation of carriers in the $Ga_{1-x}In_xN$ with $x<0.15$ quantum wells (QW's) and in InAs quantum dots (QD's) and their unusual photoinjection to respectively GaN and GaAs barriers via strong Coulomb interaction results in creation of the nonequilibrium two-component electron-hole plasma in the appropriate GaN or GaAs layers. This plasma seriously affects the performance of various III-nitrides based devices since it expands through the whole specimen marking the deepest place by light emission.

One of the most important and rich phenomena exhibited advances in solid state physics of nanometer-sized semiconductor layers embedded by QD's, or QW's in which electrons are confined in one or in all three directions of space, is the role of physical mechanisms determining the efficiency of optical transitions and carrier dynamics. Electron (*e*) and hole (*h*) wave functions and their overlapping in such heterostuctures across well barriers control the dynamic strength of carrier fluctuations as well as *e-h* and polar optical interactions and determine the transport and optoelectronic properties. A large spectral misfit existing between photoluminescence (PL) maximum and PL excitation (PLE) edge in $Ga_{1-x}In_xN$/GaN QW's is usually associated with punctuated island growth mode applied for these heterostructures. A localization of photoexcited carriers into the deepest QD-like potential fluctuation is responsible for light emission. The problem is how do carriers find their way and penetrate inside such a unique potential fluctuation. Related physical items are clarified already during recent development of InAs/GaAs based QD systems.

We have investigated slabs embedded with QD's consisting of 10 periods of 1.8 MLs InAs and 5.1 nm GaAs and also sets of $Ga_{1-x}In_xN$/GaN multiple QW structures. The effective diameter (base size) of InAs QD's was ≈12 nm and the distance between neighbor dots was 25 nm. Five 3 nm thick $Ga_{1-x}In_xN$ QW's were embedded in 9 nm GaN barriers. Double difference in heterostructure constants is effectively compensated by respective ratio of base material dielectric constants: $\varepsilon_{GaN}/\varepsilon_{GaAs}\approx 2$. One of the most important points of this work is that we observed unconventional quasi- and inelastic electronic light scattering spectra in an intrinsic GaAs nanometer-sized layers embedded by QD's using a selective resonant excitation above the InAs band gap but below the GaAs band gap and respective absorption of GaN-based heterostructure. Giant enhancement (by a factor of 10^6) of optical transitions efficiency in such mesoscopic systems is registered. Despite much larger band offsets and relaxation of selection rules in $Ga_{1-x}In_xN$/GaN QW's as compared with the previous heterostructure respective enhancement is only accessible for a small number of interband transitions. The experimental observation of the enhanced in oscillator strength interband transitions results in the creation of unexpected for the case of intrinsic heterostructures the two-component nonequilibrium electron-hole plasma. We excite this novel plasma by photocreation of electrons and holes as Wentzel et. al.[1] do with the same (1064 nm line of Nd^{+3}:YAG laser, or Xe-white lamp with 0.25 m monochromator) source used for the detection of scattering or luminescence spectra. For the excitation density employed the electron-hole occupation number of the QD's itself should be approximately equal or less than 1 and the respective quantity for QW's is even more questionable. Therefore, an experimental observation of unexpected collective excitations of electron-hole pairs in QD's system unambiguously demonstrate that the two-component plasma is initially

induced by the two populations of free carriers separated in the real space. Such modes reveal the strong Coulomb electron-hole interaction. Electrons and holes are photoexcited in the QD's or QW's, but they are captured (trapped) or released due to overlapping of hole wave-functions between neighbor QD's or QW's. Such processes can lead to a fluctuating charge distribution (configuration) outside the QD's or QW's. Thus, present experiments break the news about the most important phenomena leading to a fluctuating charge distribution outside the QD's or QW's and formation of free electrons and holes in the GaAs or GaN layers with efficient direct electromagnetic coupling between the carriers. The piezoelectricity in such strained and polarized low symmetry heterostructures causes the unexpected enhancement of the coupling strength as compared to the bulk case. Therefore the transport is determined by the properties of those carriers that are injected from the QD's or QW's into the undoped GaAs or GaN barriers. Summing up the intra-subband including quadrupole momentum scattering lineshape and zero temperature approximation acoustic plasmon (AP) peak with inter-subband contribution of scattering intensity, leads to the line shape presented in figure by dashed line. Measured light scattering spectra obtained for polarized configuration from InAs/GaAs QD's structure at a lattice temperature T_l = 5.1 K [2] is plotted by solid line. Calculated spectrum describes well both AP peak position around 25 cm^{-1} and quasielastic tail and fits well inter-sub-band maximum around 250-270 cm^{-1}. Successful comparison between experimental and theoretical scattering spectra provides an evidence of plasma homogeneity.



Though relative scaling of AP intensity to inter-sub-band continuum is evidently overestimated as compared with the experimental result preference for AP formation is much more effective than for the ordinary high-frequency optical plasmons in this nonequilibrium two-component uniform e-h plasma. There is a good chance to proceed with present Raman investigation for $Ga_{1-X}In_XN$/GaN multiple QW structures using polyphenil dye laser provided respective photodetector will be available.

This work is supported by Russian Foundation for Basic Research (Grant No 01-02-17895).

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Abnormal Hysteresis Property of SiC Oxide C-V Characteristics

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Abstract. In this paper, the electrical characteristics of the thermal oxide grown on SiC were discussed. For these studies, the MOS capacitors with the size of about 31,400 μm^2 were fabricated on a 6H-SiC wafer which had a 5 μm thick n-type epi-layer with a doping concentration of 3 x $10^{15}cm^{-3}$. An about 35 nm thick oxide layer was thermally grown in wet O_2 at 1150 ℃ for the dielectric layer.

The high frequency C-V measurement results of the MOS capacitors showed an abnormal hysterisis property, which was believed to be due to the movement of the electrons trapped inside the oxide layer. In addition, it was found that the oxide had quite a large low-level leakage caused by the trap-assisted tunneling and most of the traps were located in the region near the bottom of the gate oxide.

Ⅱ. Experiments

The MOS capacitors with the size of about 31,400 μm^2 were fabricated on a 6H-SiC wafer which had a 5 μm thick n-type epi-layer with a doping concentration of 3 x $10^{15}cm^{-3}$. An about 35 nm thick oxide layer was thermally grown in wet O_2 at 1150 ℃ for the dielectric layer. In addition, a 200 nm thick Al layer were deposited on the wafer and patterned by wet etching to form the gate electrode, and a 100 nm thick Ni layer were deposited on the backside of the wafer to form the ohmic contact on the substrate. Then the high frequency C-V characteristics and the leakage current were measured using the HP4284A LCR meter and the HP 4156A parameter analyzer.

Ⅲ. Conclusions

An abnormal histeresis property was observed from the high frequency C-V characteristics of the MOS capacitor with the thermal oxide grown on the SiC substrate as its dielectric layer. This was believed to be due to the movement of the electrons trapped in the deep level traps inside the oxide layer. The electrons might move back and forth from the trap sites near the bottom side of the gate oxide to those near the top side depending on the polarity of the gate bias voltage mainly during the holding time among the measurement steps.

On the other hand, quite a large low-level leakage was observed when the gate bias voltage was positive, while it was not when the gate bias voltage was negative. The large low-level leakage with the positive voltage gate bias was believed to be caused by the trap-assisted FN tunneling, where most of the traps were located in the region near the bottom of the oxide layer.

Acknowledgments

This work was supported by grant No. 2000-2-30200-010-3 from the Basic Research Program of the Korea Science & Engineering Foundation.

This work was also done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE(Ministry of Commerce, Industry and Energy), Korea.

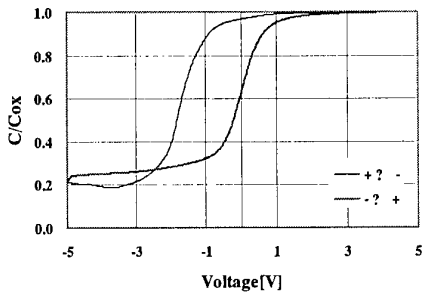


Fig. 1 High frequency C-V characteristics of SiC oxide with the gate voltage bias sweep from +5V to –5V and consecutively from –5V to +5V and each step of 0.02V

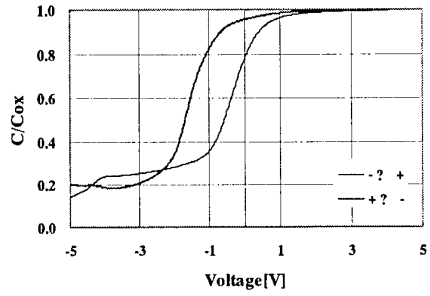


Fig. 2 High frequency C-V characteristics of SiC oxide with the gate voltage bias sweep from -5V to +5V and consecutively from +5V to -5V and each step of 0.02V

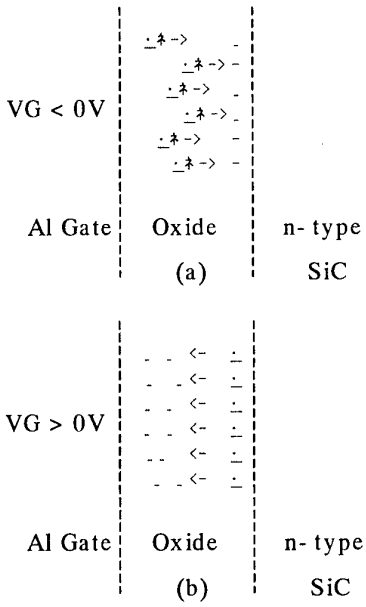


Fig. 3 Schematic diagram for trap-assisted carrier tranport (a) negative voltage and (b) positive negative voltage

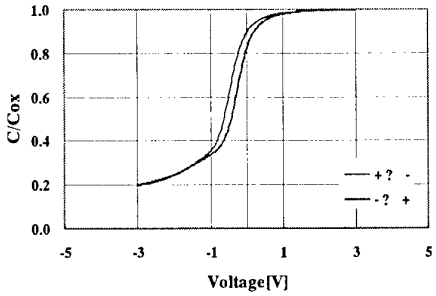


Fig. 4 High frequency C-V characteristics of SiC oxide with the gate voltage bias sweep from +3V to –3V and consecutively from –3V to +3V and each step of 0.02V

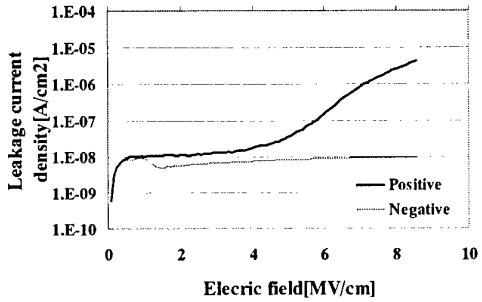


Fig. 5 Leakage Current of the SiC oxide of 35nm

Electrical characteristics of 4H-SiC pn diode grown by LPE method

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Recently, considerable progress in fabricating high power devices using SiC has been reached. It is well known that the basis of a bipolar device is a pn junction. In order to reach the excellent electrical characteristics of the bipolar devices it is necessary to improve quality of the pn junctions. The objective of the research is to study the electrical characteristics of pn diode grown by LPE method.

4H-SiC $p^+pn_0n^+$ structures were grown by LPE method. First, a n^+-layer was grown on commercial 2-inch (0001)Si 8^0-off 4H-SiC wafers. The n^+-layer serves as the layer for closing micropipe defects that usually exist on commercial substrates. The thickness of n^+–layer was 10 micron. N_d-N_a uncompensated impurity concentration in this layer was determined to be 3×10^{18} cm^{-3} An undoped n_0–layer was deposited on the n^+-layer. The thickness of n_0–layer was found to be (10-15) μm. N_d-N_a uncompensated impurity concentration in this layer was determined to be $(9\times10^{15} \div 3\times10^{16})$ cm^{-3} for different samples. Al doped and Al heavily doped epitaxial layers were grown on n_0–layer in that order. The thickness of Al doped layers was (2.0÷2.5) and (1.0÷1.5) micron for p-layer and p^+–layer, respectively. N_a-N_d concentration in the p-layer was found to be $(3\div6)\times10^{18}$ cm^{-3}. The N_{Al} concentration in the p^+-layer was determined using SIMS technique to be in order of 1×10^{20} cm^{-3}.

To study the electrical characteristics of the 4H-SiC pn structures mesa-diode with ohmic contacts were formed. Cr/Al was used as backside ohmic contact to n-type substrate, and Al as ohmic contact to top LPE p^+-layer. Al and Cr metallization was deposited by thermal vapor evaporation. The top Al metallization was patterned by conventional photolithography to form dots with diameter of 150-1500 μm. Mesa-diodes were fabricated by reactive ion etching in SF_6/O_2 gas mixture.

The position of the pn junction in the epitaxial $p^+pn_0n^+$ structure was determined using electron beam induced current (EBIC) measurements. A diffusion length of minority carriers in the n_0-layer (holes) was estimated by EBIC to be 1.5-3 microns for different samples.

The C-V characteristics of the pn junction were measured at different frequencies of 10 kHz and 1 MHz. The C-V characteristic of the pn junction was liner when plotted in C^2-V coordinates, which is typical for an abrupt junction. The cut-off voltage of the C-V characteristics was 2.97±0.02 V. The value of built-in potential was calculated to be ~3.0 eV, which is close to theoretical value of the built-in potential for a 4H-SiC pn structure doped with nitrogen and aluminum.

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Low current forward – bias testing was performed in the temperature range from 300 to 700 K (Fig.1). The forward I-V characteristics contain an exponential region: $I_f = I_S \times \exp(V/V_0)$, where I_f is forward current, I_S is the saturation current. The value V_0 was found to be independent on temperature and was determined to be about 0.1 V. The I_S showed exponential behaviour depending on temperature (Fig.2): $I_S = I_{S0} \times \exp(T/T_0)$, where I_{S0} is saturation current independent on temperature. The value of T_0 was determined to be 38.4 K. The basic property of the forward I-V characteristics is the fact that the slope of the exponential curve log(I) vs V doesn't change as a function of temperature (Fig.1). To explain such experimental results, we suppose that the electronic transport in the investigated pn junction is limited by the tunneling rate of electrons from the conduction band of n-type material into the deep traps with subsequent recombination with holes through the deep traps. We propose that there is defect layer between n_0- and p-layers. The deep traps are proposed to be located in the defect layer. Thus, the according experimental data the forward I-V characteristics for current range from 10^{-10} to 10^{-3} A in the temperature range from 300 to 700 K may be described by tunneling model of carrier transport.

The reverse I-V characteristics showed an abrupt breakdown at voltages around 150 – 500 V for different samples. Breakdown voltage, V_b, was determined as the voltage at which an abrupt change in the reverse current occurred. It was evaluated that the breakdown electrical field for the pn junction was $\sim(1.3 \div 1.8) \times 10^6$ V/cm.

The investigation of electrical characteristics of pn diode grown by LPE method will be presented in detail.

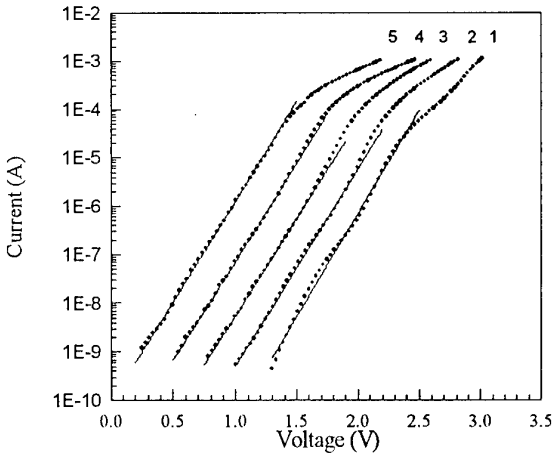


Fig.1. Forward I-V characteristics for a 4H-SiC pn diode measured at different temperatures: 1-300 K, 2-400 K, 3-500 K, 4-600 K, 5-700 K.

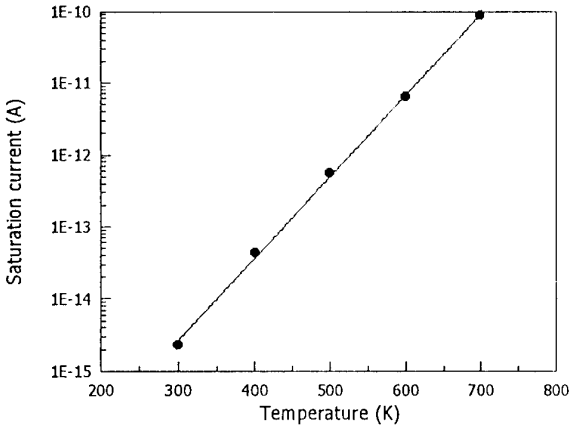


Fig.2. Saturation current as a function of temperature for a 4H-SiC pn diode.

Acknowledgements

The research is financially supported by NATO grant # SfP-971879.

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Wet-chemical preparation of silicate adlayer reconstructed SiC(0001) surfaces as studied by PES and LEED

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We have studied the effect of a wet-chemical cleaning procedure on SiC(0001) surfaces by photo electron spectroscopy (PES) using synchrotron radiation, and low-energy electron diffraction (LEED). This procedure is normally applied prior to the hydrogenation of SiC. [1-3] The four-step procedure [4] consists of step A: 10 minutes in a 4:1 mixture of H_2SO_4 (97%) and H_2O_2 (30%) at 180°C; step B: 10 minutes in HF (40%) at room temperature; step C: 10 minutes in a 4:1:1 mixture of H_2O, H_2O_2 (30%), and HCl (37%) at 80°C; step D: 5 minutes in HF (5%) at room temperature. Each step is followed by rinsing in deionized water. Photoelectron spectroscopy reveals that the wet-chemically prepared surfaces contain considerable amounts of oxygen. The amount of oxygen was found to be highest after step A of the wet-chemical procedure. The hydrogenation process allows the oxygen content to be pushed below the detection limit as was shown previously. [1-3]

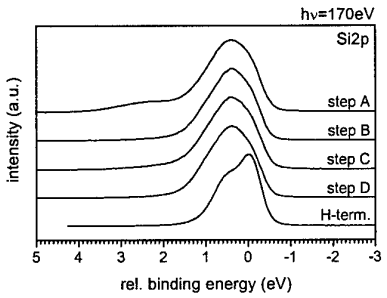


Fig. 1: Si2p spectra taken after the subsequent preparation steps at 170 eV photon energy.

preparation	Si^+ / SiC	Si^{4+} / SiC
Step A	1.30	0.50
Step B	1.52	0.13
Step C	1.33	0.20
Step D	1.45	0.07

Table 1: Relative (to bulk SiC) contributions of the Si^+ and Si^{4+} components to the Si2p spectra measured at 170eV photon energy.

In figure 1, Si2p core level spectra are shown which were taken after each wet-chemical preparation step and after hydrogenation. Whereas the spectrum taken from the hydrogenated surface shows one single line due to stoichiometric SiC, [1-3] the wet-chemically treated surfaces contain Si in higher oxidation states. This is evident from the shape of the Si2p signals which extend to higher binding energies.

The corresponding C1s spectra (not shown here) revealed two components, one of which is due to the SiC, and the other one is originating in weakly adsorbed hydrocarbons which are absent in *in-situ* experiments. [1-3]

Fig. 2(a) displays a deconvolution of the Si2p spectrum taken after step A (topmost spectrum in fig. 1) into three Voigt doublets. The fit reveals that considerable amounts of Si^+ and Si^{4+} are present at the surface. This is evident from the additional components which are shifted with respect to the bulk line by 0.5 eV and 2.0 eV, respectively. The intensity ratios determined for all four wet-chemical preparation steps are compiled in table 1. As can be seen from the table the relative intensity of the Si^+ component is almost constant. On the other hand, the Si^{4+} component is highest after step A of the wet-chemical cleaning procedure. As expected, it is smallest after the HF etches (steps B and D) and has an intermediate value after step C which is also an

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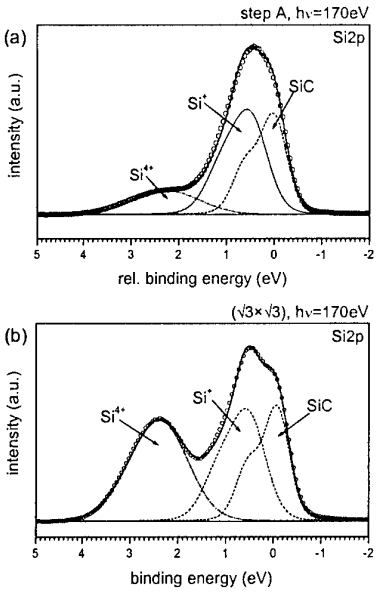


Fig. 2: Deconvolution of the Si2p spectrum obtained from (a) the SiC(0001) surface after preparation step A and (b) of a SiC(0001) surface with silicate adlayer.



Fig. 3: LEED pattern taken at 70eV from a SiC(0001) surface after a modified prepara-tion step A.

oxidizing step.

Wet-chemically treated surfaces were previously shown to be terminated by OH groups. [5] Thus, the Si^+ signal observed after steps B, C and D can be assigned to Si-OH units. The fact that the Si^+/SiC ratio is constant points towards a monolayer coverage with OH as was also suggested by Starke et al. [5]

The Si^+ signal after step A has at least partially to be assigned to a different bonding arrangement. The fingerprint of the spectrum is very similar to the one observed on a silicate adlayer-terminated SiC(0001) surface with $(\sqrt{3}\times\sqrt{3})$-R30° periodicity. [6] This silicate adlayer reconstruction is an oxygen rich termination of both, SiC(0001) and Si$(000\bar{1})$ surfaces and its structure was studied by Bernhardt et al. [7] using LEED. Figure 2(b) shows the deconvoluted Si2p spectrum of such a surface, which was prepared in a hydrogen plasma. On this surface, the Si^+/SiC ratio is 1.21. The Si^{4+}/SiC ratio, however, is 1.39 and thus three times larger than on the wet-chemically prepared surface, indicating that on the latter surface about one third of the surface is covered with the silicate adlayer reconstruction.

Indeed, despite the fact that only about one third of the surface was covered with the silicate adlayer, a weak $(\sqrt{3}\times\sqrt{3})$-R30° LEED pattern was observed on that surface. The quality of the LEED pattern, and thus the degree of surface order, depends on the conditions of the preparation, e.g. the etch time, temperature and the composition of the Piranha solution. A clear $(\sqrt{3}\times\sqrt{3})$-R30° LEED pattern (figure 3) was observed after a modified preparation Step A (10 minutes, H_2SO_4 : H_2O_2 = 3:1, 200°C). To our knowledge this is the first time that the silicate adlayer reconstruction was observed after a wet-chemical treatment. The results will also be discussed in the light of recent oxidation studies on SiC(0001) [8,9].

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Some of comparative properties of diffusion welded contacts to 6H- and 4H-silicon carbide

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In the paper submited at the last ECSCRM'2000 conference we had reported about our initial results in forming thick and large area aluminium contacts to 6H- and 4H-SiC using diffusion welding (**DW**) technique [1].

The favourable points of the work determining the practical clearness for the further R&D, in our opinion, are the follows:

- the possibility to perform by **DW** reliable, homogeneous large area thick Al contacts both to 6H- and 4H- silicon carbide;
- the possibility to make the Al / SiC Schottky contacts with evident non-linear I-V characteristics.

All the above gives every reason to continue the work in diffusion welded cotacts to silicon carbide since there are the prospect to form in comparatively simple way the Schottky contacts able for commutation of heavy currents and on the other hand such metallization technique can be propagated on the other types of SiC p-n structures for power semiconductor devices.

The n-type wafers used in our early experiments were from Cree Research, Inc.: 6H-SiC substrates of $3.6x10^{18}$ cm^{-3} doping concentration without epilayer, and 4H-SiC(I) with 5 μm. thick epilayer of $2x10^{17}$ cm^{-3} doping concentration. In both cases the doping concentrations were too high for operating Schottky diode, so for the next series of experiments the epiwafer of 4H-SiC(II) was purchased from Sterling Semiconductor,Inc. The nitrogen dopant in 6.75 μm. epilayer was $4.75x10^{15}$ cm^{-3} net concentration and the surface treatment was as Si-face polished and C-face ground.

The expert examination was made for the wafer to reveal the structural defects, their densities and distribution upon the surface area. Hence , it was determined the sections of the wafer surface most favourable for Me contacts. The macro – and microprofiles of Si- and C- faces of the wafer was measured to estimate the conformity of wafer configuration for **DW** process.

The I-V characteristics for Al / SiC Schottky contacts were measured in temperature range $20^{o} \div 600^{o}$ C.

On the special prepared specimens the specific series contact on-state resistance (Rsp) was carried out for 6H-SiC substrate and for 4H-SiC(II) epiwafer. Rsp was determined by surface potential distribution measurement near by the spot of metal contact (S.C. extrapolation method [2]).

It is clear from the Fig. 1 that the Schottky contact formed in relatively free of defects area of the 4H-SiC(II) wafer with low dopant concentration ($4.75x10^{15}$ cm^{-3}) has 20 times as large the reverse voltage than that in defected 4H-SiC(I) wafer with donor concentration $2x10^{17}$ cm^{-3}.

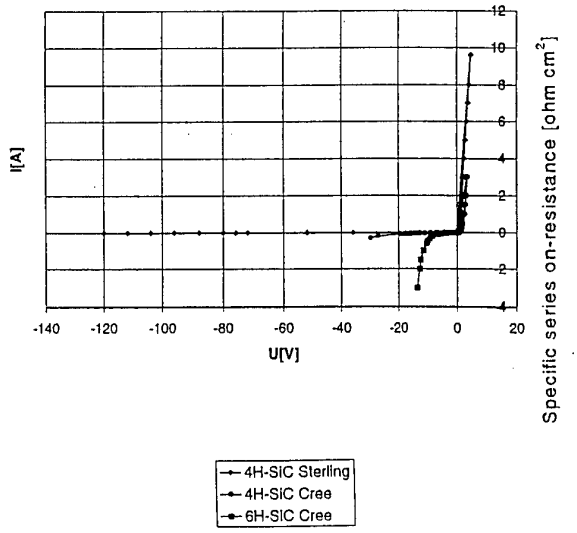


Fig. 1. I-V characteristics for 6H-and 4H-SiC structures at room temperature.

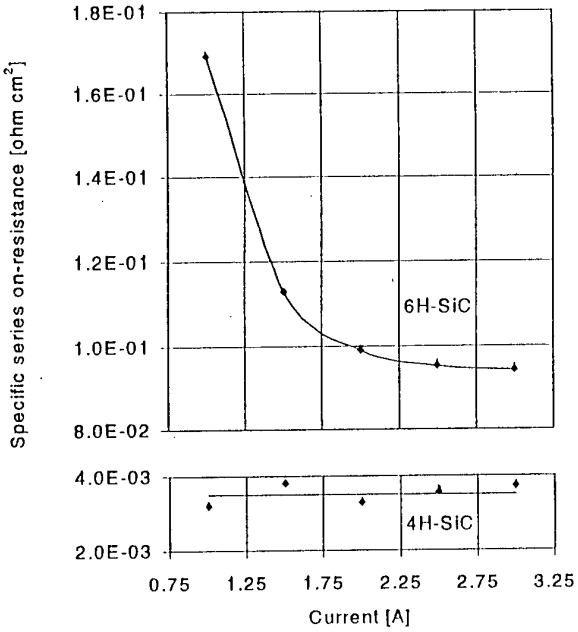


Fig.2. Variation of specific series on-resistance vs.measurement current.

Non-linearity of I-V characteristics becomes more evident not only in revers branch but in forward branch too. For I_F = 3A - U_F = 3.45V for 4H-SiC(I) and U_F = 1.86V for 4H-SiC(II).

Increase in non-linearity is to be in confirmation with the results of series contact resistance measurement. Fig.2 shows the variation of the series on-state contact resistance for 6H-SiC substrate and for 4H-SiC(II) epiwafer. It is clear that the contact on-resistance for 4H-SiC(II) is more than order lower than that of 6H-SiC substrate, indicating more or less constant on-resistance with increase in measurement current (at least in a current range of 1 to 3A).

By this time experience in using of **DW** technique applied to metal contacts for semiconductors it is possible to predict with confidence that the manufactoring of power semiconductor devices based on silicon carbide will be determined not so much as by the possibilities of **DW** technique, but by the imperfections in SiC wafers. Thus, the dimentions of metal contacts and therefor the power dissipation at high on-current as well as reverse leakage will depend on the dimentions of relatively free of defects area of silicon carbide wafers.

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Reliable ohmic contacts to LPE p-type 4H-SiC for high power p-n diode

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Silicon carbide is a semiconductor material in which a unique combination of wide bandgap, high saturation electron velocity, high breakdown field, low dopant diffusivity and high thermal conductivity is observed. These properties and a recent progress in the device processing determine SiC as the most appropriate material for high power microelectronics.

Despite the successful solution of many technology problems in the SiC device fabrication, the reliability of the ohmic contacts remains as a factor that restrict the high power device applications. The combination of good electrical and physical characteristics with stability at high operating temperatures is the principal requirement to the ohmic contacts and a prerequisite for the reliability of the power SiC devices.

Two kinds of p-type ohmic contacts to SiC, namely Al-based and Pd-based, have been studied in respect to their application in the high power p-n diode. The Al-based contacts, which have been the subject of our investigation, are the widely used Ti/Al contacts together with the Al/Si and AlSiTi ones. Pd is a very promising metal for low resistivity p-type ohmic contacts to SiC. For that reason, Pd-based contacts such as Pd, Pd/Ti, Pd/Al and new Pd/Si and Pd/Ti/Pd ones have been studied concerning their thermal properties as an alternative of the Al-based contacts for high temperature and high power applications.

The contacts investigated were formed on p-type 4H-SiC layers grown by liquid phase epitaxy (LPE) with a thickness of 0.5 μm and a doping concentration of $3x10^{19}$ cm^{-3} - $1x10^{20}$ cm^{-3}. The LPE layer was grown on a commercially available structure having a top p-type ($1x10^{19}$ cm^{-3}) 1 μm thick CVD epitaxial layer grown on n-type substrates. The contact deposition was performed by a subsequently electron beam evaporation of the metals in vacuum of $1x10^{-6}$ torr or by sputtering in argon at pressure of $3x10^{-3}$ torr. The annealing was carried out in a resistance furnace in an argon atmosphere at temperatures necessary to obtain the lowest resistivity of each contact type. A contact resistivity in the range of 10^{-5} $\Omega.cm^2$ has been obtained for both Al-based and Pd-based contacts. Therefore, the reliability of the contacts at high temperature treatments is considered as the critical factor determining their power device applications.

The reliability of the contacts has been examined by investigation of their thermal stability. The latter has been estimated by the contact resistivity behaviour during the ageing test, temperature-dependence test and temperature-current treatment test.

Ageing of the contacts for a long time has been carried out at a constant temperature ranging from 500 °C to 700 °C in an inert atmosphere (N_2) and in air. In fixed time intervals the contacts are cooled to the room temperature and the contact resistivity has been determined. The contact resistivity has been measured always at room temperature.

In the temperature-dependence test the measurements have been proceeded at a temperature increasing smoothly from 25 °C to 450 °C in air. This study gives information on the contact reliability at the corresponding operating temperature as the contact resistivity has been measured during the heating.

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During the temperature-current treatment a current with a pre-set density (up to 10^4 A/cm^2) is passed for a fixed time through the contacts at a constant temperature (up to 500 °C). This test has been also performed in air and contact resistivity has been measured at the corresponding temperature.
The experiments on ageing of the contacts developed started with heating at 500 °C in nitrogen for 100 hours. Al-based contacts as well as the Pd-based ones did not change the contact resistivity during this treatment indicating a good thermal stability (fig.1). The both contact types were also stable at operating temperatures up to 450 °C in air (fig.2). The preliminary results show that Al-based and Pd-based contacts can be used in power diodes. For that reason, the following experiments on the ageing test in air and the temperature-current test will be ultimate for the suitable contact system determination.
The results obtained on the reliability of the ohmic contact to p-type LPE 4H-SiC will be summarized and discussed in respect to their application in a high power p-n diode.

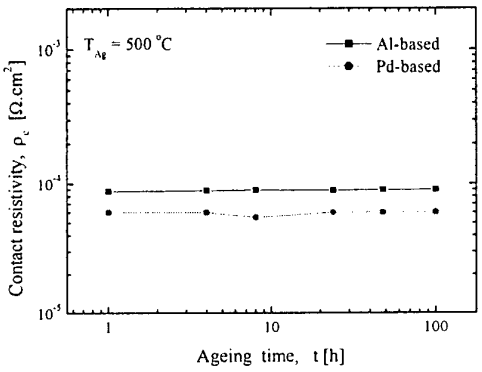


Fig. 1 Resistivity values of Al-based and Pd-based ohmic contacts to LPE p-SiC at an ageing temperature of 500 °C.

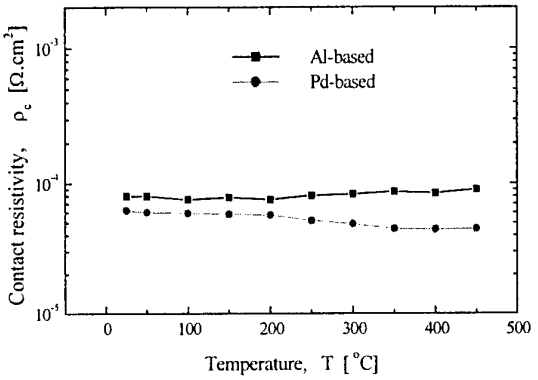


Fig. 2 Resistivity values of Al-based and Pd-based ohmic contacts to LPE p-SiC at different operating temperatures.

Acknowledgements

This work is supported financially by NATO project SfP-971879 for that the authors express their gratitude.

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Ti ohmic contact on p-type 4H-SiC

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Formation of ohmic contacts to p-type SiC semiconductor is known to be difficult, since it has a large Schottky height. Limited work has been reported about the ohmic contacts to p-type 4H-SiC, in which aluminum based metals have been used. The aluminum-based metals have drawbacks of low melting point and high driving force of oxidation in the full procedure of device fabrications. Titanium has a relatively high melting point, thus Ti-based metal contacts were attempted in this study.

Material and electrical properties of Ti ohmic contacts on p-type 4H-SiC were investigated depending on the post-annealing and the metal covering conditions. Best results are obtained as $2x10^{-4}$ ohm/cm^2 for a Pt/Si/Ti metal structure after a vacuum annealing at 900 C for 90 sec. The contact resistance was measured by a transmission line technique, and the contact resistances were improved more than one order compared to Ti and Si/Ti contacts for the annealed samples at the same conditions. Auger depth profile data shows that the Pt layer effectively reduce the oxidation of Ti films, and X-ray diffraction pattern presents that the silicon layer plays a role of diffusion barrier to the intermixing of Ti and Pt atoms, which was considered as a major cause for the large contact resistance.

Acknowledgements

This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea.

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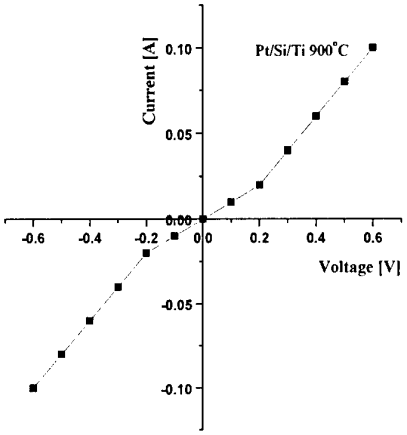


Fig. 1. I-V Characteristics Pt/Si/Ti/ p-type 6H-SiC after annealing at 900°C for 60sec.

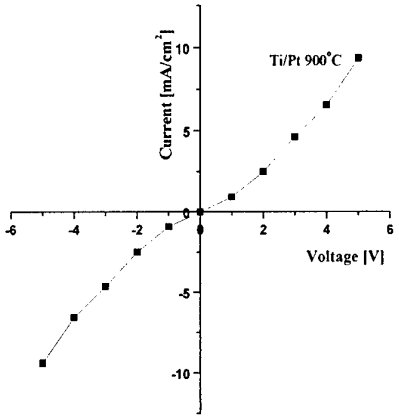


Fig. 2. Pt/Ti/ p-type 4H-SiC after annealing at 900°C for 90sec.

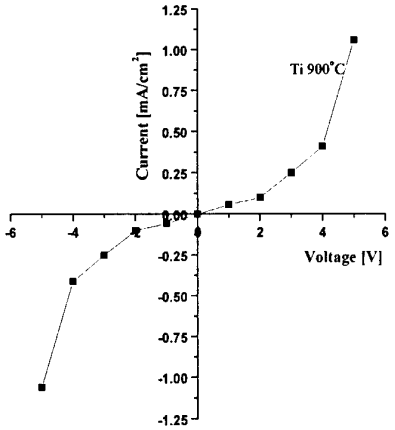


Fig. 3. Ti/ p-type 4H-SiC after annealing at 900°C for 90sec.

$NiSi_2$ ohmic contact to n-type 4H-SiC

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4H-SiC is of great attractive for high power control and high frequency devices in polymophism SiC because of high electron mobility and wide band gap. In this study, we investigated the structural and the electrical properties of $NiSi_2$ ohmic contact to n-type 4H-SiC. We have been reported $NiSi_2$ ohmic contact to n-type 6H-SiC, which is synthesized by annealing the deposited Ni and Si films at 900 °C without the reaction between Ni and SiC substrate and reveals the ohmic characteristic for the carrier concentration above 1×10^{16} cm^{-3}[1].

Samples used in this study were a 0.2-um-thick, N-doped epitaxial layer, with a carrier concentration of 2×10^{18} cm^{-3}, grown on p-type 4H-SiC substrate. After a sacrificial oxidation and HF treatment, Si film with a thickness of 92.5 nm and Ni film with a thickness of 25 nm were deposited on (0001) Si face of the sample by mean of E-gun evaporation in a vacuum of the order of 10^{-5} Pa. The thicknesses of Si and Ni films were designed to produce the stoichiometric $NiSi_2$ alloy. The samples were annealed at 900 °C for 10 min in a flow of Ar gas containing 5 wt.% H_2 gas. The composition of the formed alloy was investigated using Rutherford Backscattering spectrometry (RBS) with 1.5 MeV $^4He^+$ ions at a scattering angle of 150°. Current-voltage (I-V) characterizations were performed using Keithley 2400 source-meter combined with a micro-probe equipment at room temperature. The contact resistances were evaluated using transmission line model (TLM) method.

Figures 1 shows RBS spectra taken from Ni/Si/SiC sample before and after annealing at 900 °C for 10 min, respectively. The decrease in yield and the increase in energy width of backscattering signals from Ni and Si atoms are caused by the annealing. This result indicates that the deposited Ni film reacts with Si film by annealing at 900 °C for 10min. The atomic ratio of reacted Ni and Si was estimated to be 1:2, which corresponds to the stoichiometry of $NiSi_2$. Since the composition of the formed Ni-silicide is in good agreement with the ratio of amounts of deposited Si and Ni atoms, the deposited Ni and Si films form $NiSi_2$ alloy without the reaction with 4H-SiC substrate. As described in our previous paper, in Ni-Si system, since $NiSi_2$ alloy is the most Si-rich Ni-silicide, the stoichiometric deposition of Ni and Si films restricts the reaction of Ni and SiC substrate. The sharp edge of lower energy side in Ni signals from $NiSi_2$ indicates that the interface between $NiSi_2$ and SiC

substrate is abrupt as well as the case of 6H-SiC.

$NiSi_2$ contact showed a good ohmic characteristic to n-type 4H-SiC. Figure 2 shows the plot of resistance vs electrode distance for the $NiSi_2$ contact formed on 4H-SiC. The contact resistance (R_c) and the specific contact resistance were estimated to be 5.0 Ω and 2.7×10^{-6} Ωcm^2 using TLM-method, respectively. The specific contact resistance of $NiSi_2$ contact to n-type 4H-SiC is about three orders of magnitude smaller than that of 6H-SiC with the same carrier concentration. It is suggested that the Schottky barrier height of $NiSi_2$ contact to n-type 4H-SiC is estimated to be about 0.3 eV in according with the thermionic emission model, which is lower than that for n-type 6H-SiC (0.44 eV).[2]

In conclusion, we reported the structural and electrical properties of $NiSi_2$ ohmic contact to n-type 4H-SiC. $NiSi_2$ contact restricts the reaction between Ni metal and 4H-SiC substrate and forms the abrupt $NiSi_2$/4H-SiC interface as well as the case of 6H-SiC. $NiSi_2$ contact shows good ohmic characteristics with a low specific contact resistance of 2.7×10^{-6} Ωcm^2, which is attributed with the low Schottky barrier height at the interface.

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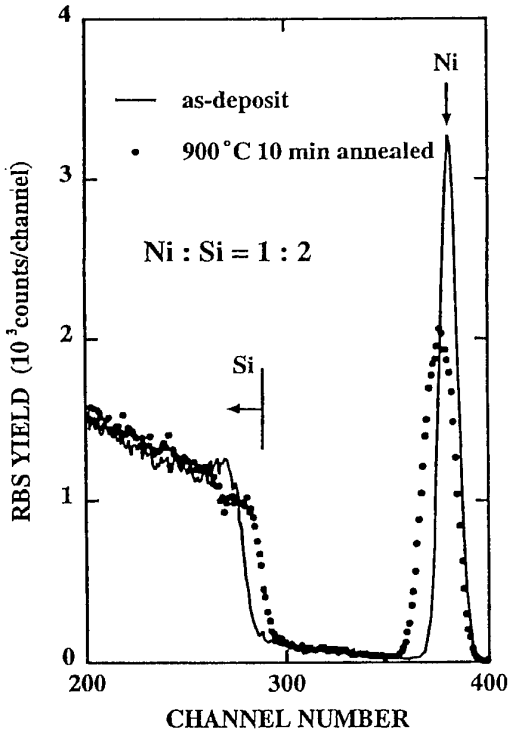


Figure 1

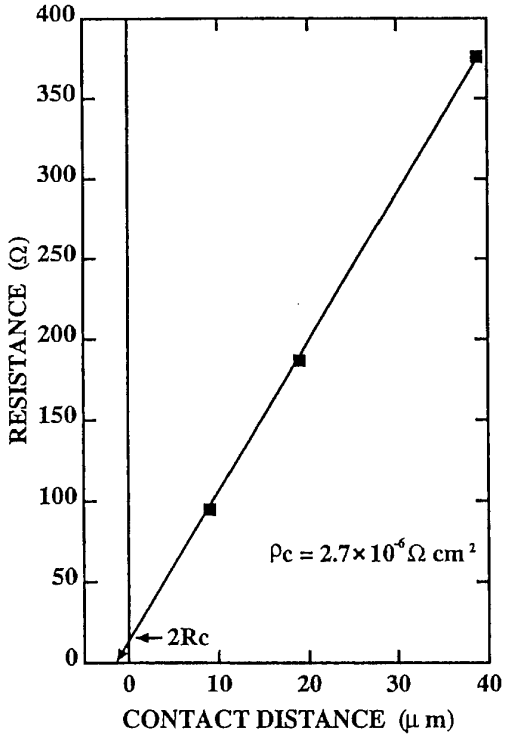


Figure 2

Influence of RTA on Ni/6H-SiC contact formation

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Rapid thermal annealing (RTA) of metal contacts has more advantages as compared with conventional techniques of heat treatment. In this research an influence of various temperatures of RTA on Ni/6H-SiC contact formation on both (0001) and (0001) faces is presented[1,2].

Single crystals samples of n-6H-SiC grown by Lely method with doping concentration of $1\text{-}3\text{x}10^{17}\text{cm}^{-3}$ were used. In first, a Ni film has been deposited on a back side of the sample followed by annealing at 1100°C. After that, Ni contacts 300x300 microns in size were formed by photolithography on the front side. The annealing has been performed in vacuum during 10 sec at the temperatures from 400 to 1100°C in the ITA-18M system with a heat rate of 100 °C/sec[3].

Current-voltage characteristics of the formed contacts after annealing at different temperatures for both Si- and C-face are presented in Fig.1. It is seen that before annealing and after annealing at 400°C the contacts have nonsymmetrical I-V characteristics. After annealing at the temperature more than 750°C, current-voltage characteristics become symmetrical. The temperature rage from 400 to 750°C is, so called, intermediate range which is associated with transient processes in the metal-semiconductor interface. Based on the measured I-V characteristics, the barrier height, specific contact resistance, saturation current as well as series resistance have been extracted[3].

Analysis of the obtained data showed that at the temperatures up to 400°C structural transformations in a Ni film, at the Ni-SiC interface, and at the near-surface region occur. This results in changing of a barrier height and surface state density. In the intermediate temperature range metastable fractions of nickel silicide are formed, while at the temperatures above 750°C the stable phase of NiSi and $NiSi_x$ are formed. Also, as it is shown, an influence of the type of a face on I-V characteristics is significantly less at the temperatures over 750°C, when the parameters of contacts mostly depend on properties of the interface $NiSi_x$/SiC.

The obtained results have shown that characteristics of an interface of one- or multiplayer metal contacts depend on the annealing temperature and a heat rate as well[4].

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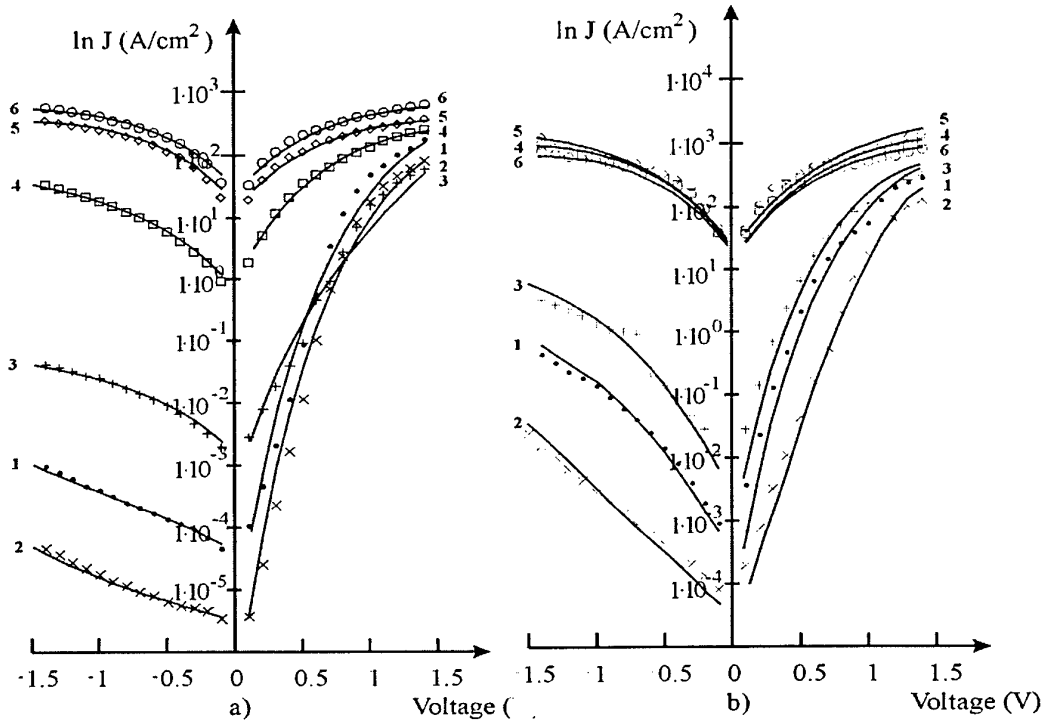


Fig.1. Current-voltage characteristics of contacts Ni/6H-SiC on (0001) face (a) and on (0001) face (b) after RTA at different temperatures: 1- as deposited; 2 – 400°C; 3 – 600°C; 4 – 750°C; 5 –900°C; 6 –1100°C.

Effect of Rapid Thermal Annealing on Parameters of Ni/21R-SiC Contacts

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At present different SiC polytypes are finding ever-widening application in manufacturing of various devices of high-temperature electronics. The heating modes of choice for retention of the SiC phase composition are those using rapid thermal annealing (RTA) with incoherent IR radiation [1]. Here we present, for the first time, the results of investigation of the effect of RTA modes on the parameters of Ni contacts to 21R-SiC (0001) and 21R-SiC $(000\bar{1})$ over a wide annealing temperature range.

The Leli-crystals of *n*-type 21R-SiC (electron concentration of $3\cdot10^{18}$ cm^{-3}) were studied. At the first stage the Ni films 100 nm thick were formed on (0001) and $(000\bar{1})$ faces using resistive sputtering. Then they were annealed in vacuum at a temperature $T = 1100$ °C for 10 s. After this similar Ni films were deposited onto the opposite faces and contacts (300×300 μm in size) were formed using photolithography. The structures obtained were annealed in vacuum at different temperatures for 10 s (the rate of change of temperature was 100 °C /s) using the ITO-18MB set [2]. We checked the contact parameters after every annealing by measuring and analyzing the *I–V* curves; besides, Auger (spectrometer LAS-2000) and structural investigations (atomic force microscope DI Nanoscope IIIa and roughness indicator Dektak 3030) were performed.

Shown in Fig.1 are the *I–V* curves of the Ni/21R-SiC $(000\bar{1})$ contacts after RTA at different temperatures. When the annealing temperature is below 400 °C, then the contact *I–V* curves are of the form of those for a Schottky diode. After annealing at temperatures over 750 °C the *I–V* curves become of the ohmic type. An analysis of the presented curves has shown that when the annealing temperature is increased, then the barrier height in contacts drops from 0.73 down to 0.38 eV, the saturation current grows and contact resistivity decreases down to $2\cdot10^{-3}$ Ω cm^2. It's remark, contact resistance estimated from I-V characteristics is some overstated. The Auger concentration depth profiles taken for the Ni/21R-SiC $(000\bar{1})$ contacts (as-deposited and after RTA at $T = 1100$ °C) are given in Fig.2.

An analysis has shown that the above results are in qualitative agreement with those obtained by other authors [3,4]. When the annealing temperatures are over 400 °C, then the processes in contacts are related to the interactions at interfaces. In this case several metastable nickel silicide phases appear with temperature growth. At high temperatures and under presence of excess Si stable NiSi and $NiSi_x$ phases can be formed [4]. It is shown that when the annealing temperature becomes over 750 °C, then the parameters of contacts to 21R-SiC are determined by the blurred $NiSi_x$–SiC interface and do not depend on the crystallographic orientation of the face. These results correlate with those concerning study of Ni surface morphology and Ni–SiC $(000\bar{1})$ interface before and after RTA. At $T = 1100$ °C substantial changes have been observed at the Ni surface and interface (Fig.3). This is supported by the features of etching of the Ni–SiC structure. Up to $T = 900$ °C the Ni surface morphology demonstrates no substantial changes; contrary to this, at the Ni–SiC interface the morphology changes can be observed after RTA at $T = 750$ °C.

An analysis of the results of our investigations shows that one should exert thorough control over the annealing modes during thermal processing of contacts. This is necessary for regulation of both phase formation in the one- and multiplayer contacts and carbon and silicon redistribution in the near-surface layer [5].

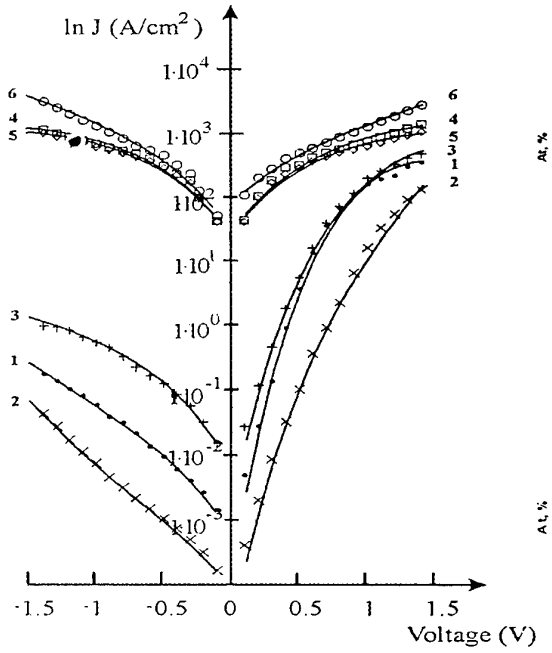


Fig.1. *I–V* curves for the Ni/21R-SiC ($000\bar{1}$) contacts before (as-deposited) (1) and after RTA at 400 (2), 600 (3), 750 (4), 900 (5) and 1100 °C (6).

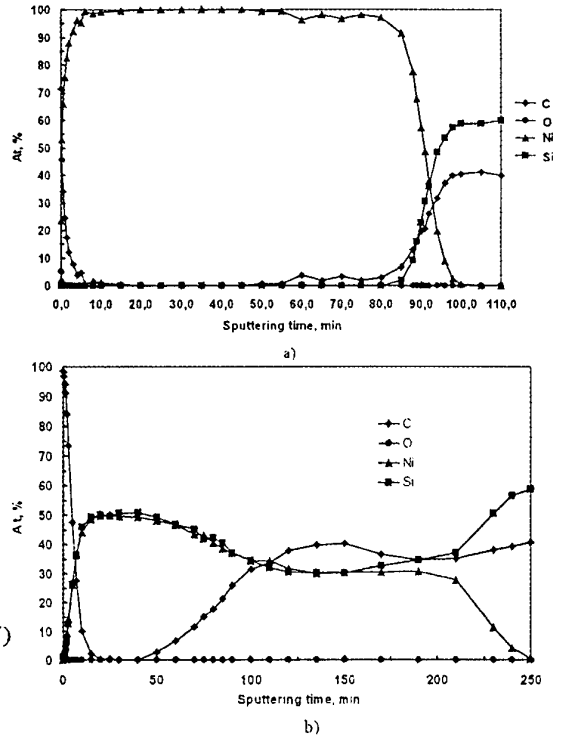


Fig.2. Auger concentration depth profiles taken for the Ni/21R-SiC ($000\bar{1}$) contact: as-deposited (a) and after RTA at 1100 °C (b).

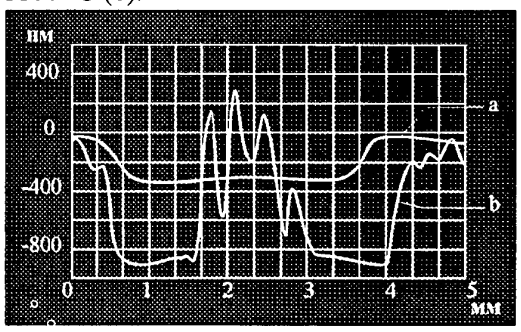


Fig.3. Auger crater profiles taken with the roughness indicator Dektak 3030 for the Ni/21R-SiC ($000\bar{1}$) contact: as-deposited (a) and after RTA at 1100 °C (b).

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CoAl Ohmic contact materials with improved surface morphology for p-type 4H-SiC

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In order to manufacture high performance SiC electronics devices, development of low resistance Ohmic contact materials for p-type SiC is one of the key issues. TiAl Ohmic contact material provided contact resistivity (ρ_c) as low as around 10^{-6} Ω-cm^2. However, this contact showed rough surface morphology after annealing at high temperatures due to excess Al addition to the TiAl contacts from the $TiAl_3$ compound stoichiometry, which was required to obtain low contact resistivity. To improve the surface morphology of this contact, we investigated CoAl contacts, because Co was reported to react with SiC at lower temperature of 600°C. Also, the Co silicide contacts to p-type 6H-SiC were reported to have a low ρ_c value of 10^{-6} Ω-cm^2 [Ref.1]. In addition, Co silicide is Ohmic contact materials have been extensively used in Si ULSI devices and would be easily applied to manufacturing SiC devices.

The purpose of this study is to develop the low resistance CoAl Ohmic contacts for p-type 4H-SiC with smooth surface morphology. We investigated the effect of the annealing temperature and the Al concentration on the electrical property and microstructure of CoAl Ohmic contacts.

A p-type epilayer (5μm thick) doped with $1.0x10^{19}$ Al/cm^3 was grown on the n-type 4H-SiC(0001) substrate by Cree Research, Inc. After chemical cleaning, the 10 nm thick SiO_2 layer was formed on the substrate by dry-oxidation. The electrode pattern were made on the SiC surface by photolithography technique and the SiO_2 layer was etched by diluted HF solution. Al and Co layers were sequentially deposited on the substrate in the high vacuum chamber by a resistance heater and an e-beam, respectively. A total typical layer thickness of Al and Co contacts was aimed to be 180 nm. After lifting off the photoresist, the samples were annealed at temperatures ranging from 800°C to 1000°C in the ultra high vacuum chamber. The annealing was carried out at 800°C for 10 min, 900°C for 5 min, or 1000°C for 2min. The electrical properties of the contacts were evaluated by the current-voltage (I-V) measurements. The specific contact resistivities were measured by the circular

transmission line model (TLM). Microstructure was analyzed by an x-ray diffraction (XRD), and the surface morphology was observed by a field emission scanning electron microscope (FE-SEM) and a stylus surface profiler.

Figure 1 shows I-V characteristics of the CoAl contacts after annealing at 800°C for 10 min. The Co contact without Al shows Schottky behavior and the contact resistance is extremely large. The CoAl contact with 10 nm or 40 nm Al layer shows Ohmic I-V behavior. However, the contact with 120 nm Al layer shows leaky rectifying behavior. After annealing at 900°C for 5 min, the I-V behaviors of the contacts with 10 nm or 120 nm Al layer changed to non-Ohmic and Ohmic behavior, respectively. After annealing at 1000°C for 2 min, both the contacts with 40 nm and 120 nm Al layer show the Ohmic behavior.

Figure 2 shows dependence of the specific contact resistivities of the CoAl contacts on the annealing temperature. The ρ_c values of the samples with 40 nm and 120 nm Al layers decrease with increase in annealing temperature. The minimum ρ_c value of 4×10^{-4} Ω-cm^2 is obtained for the contact with 40 nm Al layer after annealing at temperatures higher than 900°C. The spread of the measured ρ_c values for the CoAl contacts was much smaller than that of the TiAl contact. In addition, the surface morphology of the CoAl Ohmic contact was very smooth compared with that of the TiAl Ohmic contact even after annealing at 1000°C.

In summary, the CoAl Ohmic contacts with the smooth surface and the contact resistivity as low as 10^{-4} Ω-cm^2 were obtained after annealing at 900°C. The annealing temperature and the amounts of Al added to the CoAl Ohmic contact were lower than those prepared for the TiAl Ohmic contact.

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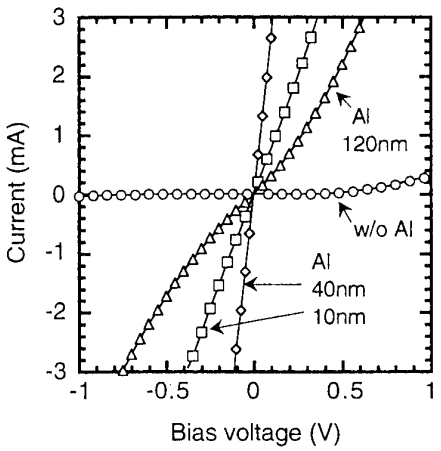


Fig. 1. The current-voltage characteristics of CoAl contacts after annealing at 800°C.

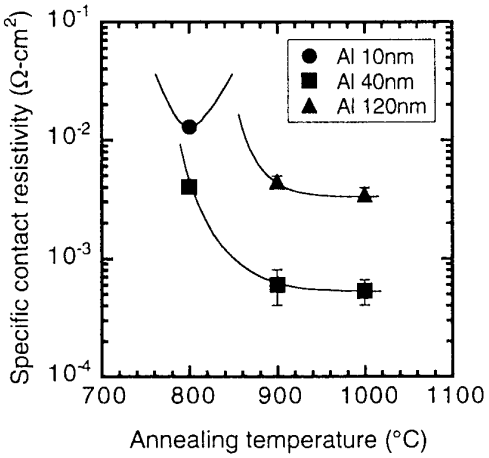


Fig. 2. The annealing temperature dependence of the specific contact resistivity of the CoAl contacts.

Effect of the temperature treatment on Au/Pd Schottky contact to 4H-SiC

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The excellent electrical and thermal properties of 4H-SiC, such as a high breakdown field, a high electron mobility, a high electron saturation velocity and high thermal conductivity make it a preferable semiconductor material for high-power Schottky rectifiers. The efficiency of these devices depends on the barrier behaviour at high operating temperatures. For that reason the good electrical characteristics of metal/SiC contacts with their thermal stability and reliability are very important for the device performance.

Different metals (Ni, Ti, Au, Pt) have been reported as Schottky contacts in 4H-SiC diodes [1-3]. The metal used as a Schottky contact in the rectifiers should combine a low resistivity and high thermal conductivity with a not very large barrier height (about 1-1.3 eV). The latter is necessary to reduce the power loss in the operating device [4].

In the present work we propose and study for the first time Pd as a suitable metal for Schottky contact to n-type 4H-SiC. The wafers used for Schottky contact formation consisted of n-type 4H-SiC layers grown by sublimation epitaxy on the Si-face of commercial n-type, approximately (7-10)x10^{18} cm^{-3}, 4H-SiC substrates. The growth was performed in a high purity graphite crucible at temperatures between 1600°C and 1800°C and base pressure of either 1.5x10^{-5} or 4.5x10^{-6} torr. Due to the specifics of the sublimation epitaxy process the layers contain Al, B, and N as typical residual impurities, resulting in compensated material. Epilayers with two carrier concentrations, 2x10^{16} cm^{-3} and 8x10^{16} cm^{-3}, were utilised in this study. They were cleaned using a standard cleaning procedure in organic solvents and etching. Prior to the metal deposition the surface was cleaned in Ar discharge. The deposition of all metals was performed by electron-beam evaporation in vacuum of 1x10^{-6} torr. The low resistance ohmic contact was formed to n-SiC substrate. It included 100 nm thick Ni annealed at 950 °C. After annealing Ti/Au (100 nm/100nm) layers were evaporated subsequently. The Schottky contact consisted of consecutively evaporated Pd (100nm) / Au (80nm) layers. The upper Au layer was deposited to protect Pd during the thermal treatments. The contact pads in a diameter of 0.6 mm were formed a using shadow mask. The samples investigated have a vertical configuration. The Schottky contact was annealed in a resistance furnace in an argon atmosphere for 5 min at temperatures ranged from 200 °C to 600 °C.

The Schottky barrier was electrically characterized by I-V and C-V characteristics. The barrier height and the ideality factor have been determined from the I-V characteristics measured on the as-deposited samples and after annealing at each temperature in the interval investigated (Fig.1). The results showed that the annealing temperature increase caused a slight increase of the barrier height up to 500 °C. The following annealing at 600 °C did not change it (Fig.2). More pronounced effect of the annealing temperature was observed on the ideality factor. It decreased up to 500 °C heating but further annealing at 600 °C did not

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improve it. These results determined the annealing temperature of 500 °C as a suitable for the Schottky contact formation. The barrier height was calculated to be 1.05 eV before annealing and 1.11 eV after annealing at 500 °C for the sample with the higher carrier concentration. For the same sample a barrier height of 1.2 eV has been determined from the C-V characteristics. An increase of the barrier height has been observed with the sample having a lower carrier concentration. The I-V measurement determined 1.14 eV and 1.2 eV before and after annealing respectively. The value of 1.31 eV has been measured from the C-V characteristic of the annealed sample. In order to explain the observed effect of the annealing on the barrier height an Auger analysis of the interface Au/Pd/SiC has been carried out.
The obtained barrier height values correspond to the requested ones for the reduction of power loss in the Schottky diode [4]. These results as well as the high thermal conductivity (71.6 W/m-K) and the low resistivity (1.06×10^{-5} Ω.cm) of Pd illustrate that it is a suitable metal for Schottky contacts to n-type 4H-SiC.
Additional experiments on thermal stability of Au/Pd/SiC Schottky contacts at high operating temperatures will also be presented.

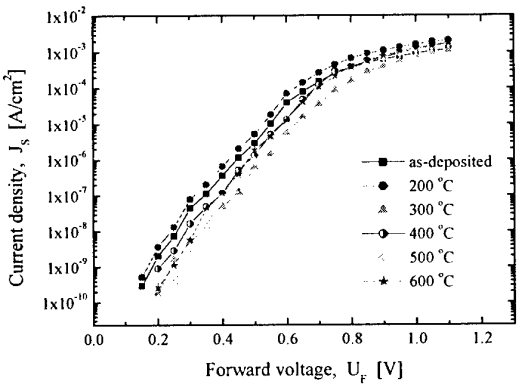


Fig.1 I-V characteristics of Au/Pd/SiC Scottky contacts after treatment at different temperatures for 5 min.

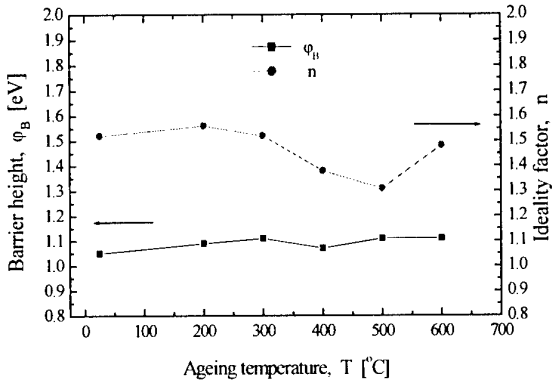


Fig.1 Values of the barrier height and the ideality factor of Au/Pd/SiC Scottky contacts after treatment at different temperatures for 5 min.

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ELECTRICAL CHARACTERISATION OF NICKEL SILICIDES CONTACTS ON SILICON CARBIDE

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Large bandgap semiconductors have been widely investigated and utilised for optoelectronic applications. However, research and commercial interest in large bandgap semiconductor and SiC electrical devices have recently increased due to the availability of high-quality SiC wafers and general advance in material fabrication techniques. SiC is a promising power semiconductor because of its large bandgap (3.0 eV for 6H and 3.2 eV for 4H) and thermal conductivity (4.9 W/cmK for 6H and 4H)[1]. For power applications, SiC large bandgap translate into a high electrical field and that allows device designs that have lower series resistance and lower power dissipation.[2,3] The great potential of SiC as a semiconductor in electronic device applications is challenged by the difficulty of controlling metal contact properties.[4,5] These properties of the metal/SiC interfaces include uniformity and thickness of the interfacial region, stability at high temperatures, and most importantly the Schottky Barrier Height (SBH) or the energy barrier for electrons traversing the interface. The Schottky barrier height determines the electrical behaviour of an ohmic or Schottky contact. An ohmic contact, important for making outside communication to a device, is defined as having: (a) a linear and symmetric current-voltage relationship for positive and negative voltages; and (b) negligible resistance compared with the bulk of the device. Therefore a low Schottky barrier is necessary to create a good ohmic contact. However, a large SBH is necessary to obtain a good Schottky, or rectifying contact.

In this paper we reported the specific contact resistance and Schottky barrier measurements of Ni/SiC-6H annealed in the range between 600 and 950 °C. The ternary phase diagram of this system[6] shows that the only stable silicide phase is the Ni_2Si. This behaviour has been confirmed in a previous paper[7] where we have shown that the Ni_2Si phase can be formed in the temperature range between 600 and 950 °C. The carbon present in the consumed silicon carbide layer precipitates in small (4 nm) clusters.

On this system several experiments have been performed to determine both the specific contact resistance and the Schottky barrier height but in these studies a simultaneous determination has not been performed in the same experimental conditions.

The specific contact resistance measurements were performed on some Transmission Line Method (TLM) structures consisting of six contact pads separated by 100 to 400 μm realised on high doped SiC substrates. The doping of the substrate was ranged between $5\cdot10^{17}$ and $7.4\cdot10^{18}$ cm^{-3}. On these substrates a SiO_2 layer, 50 nm thick, was grown by dry oxidation at 1150 °C. The TLM structures were realised by a photolitographic process and the oxide layer was finally etched by a Reactive Ion Etch (RIE) apparatus. On these structures the Ni film was deposited and subsequently reacted at 950 °C for 60 s. After the reaction the unreacted film on the silicon oxide layer was etched by a selective etch. The self aligned TLM structures were characterised on a Wentworth probe station with a Keitley 236 and a Keitley 619.

On a n^+ substrate (N_d=$7\cdot10^{18}$ cm^{-3}) an epitaxial layer 4 μm thick with a doping concentration of $2.8\cdot10^{15}$ cm^{-3} was grown by CREE Res. Inc. On these wafers a Chemical Vapour Deposited (CVD) oxide was deposited. Circular structures were opened in the oxide by a photolitographic process in the range between 100 and 240 μm diameters. Then a 200 nm Ni film was deposited, with the

previously reported parameters, and finally the metal layer was defined with a second mask to form a field plate over the oxide. These diodes were characterised in a Cascade probe station before and after an annealing process at 600 °C for 60 s.

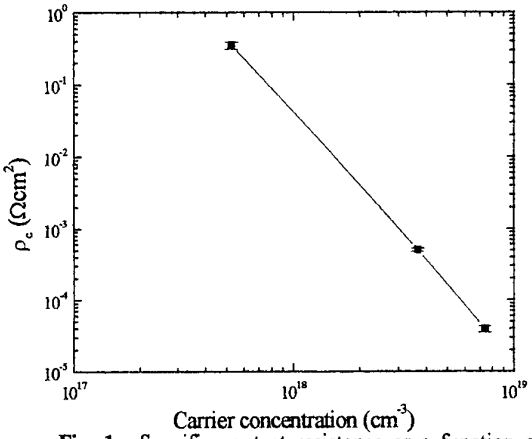


Fig. 1 - Specific contact resistance as a function of the substrate carrier concentration for Ni/SiC samples, annealed at 950°C in N_2 for 60s. The line connecting the points serves to guide the eye only

Several TLM structures have been prepared with the process previously described. A Ni film has been deposited and reacted with the silicon carbide substrate at 950 °C. The total resistance R_T measured between two TLM pads of width W, placed at distance d, can be written as:

$$R_T = 2R_C + (R_s/W)d \qquad (1)$$

where R_C is the metal/SiC contact resistance and R_S is the sheet resistance of the SiC substrate.

By separating the two contributions of the contact and sheet resistance, the specific contact resistance ρ_c can be calculated[8,9].

The data are reported in figure 1. Our data for the Ni_2Si are very close to the values reported from Crofton et al.[10] with a similar process.

The fabrication process of the Schottky diodes was explained in the experimental section. After diodes formation, these devices were characterised by I-V, I-T and C-V measurements. From the I-V data it has been observed that the characteristics were nearly ideal (n=1.07) and the Schottky barrier height was in the range of 1.30±0.01 eV.

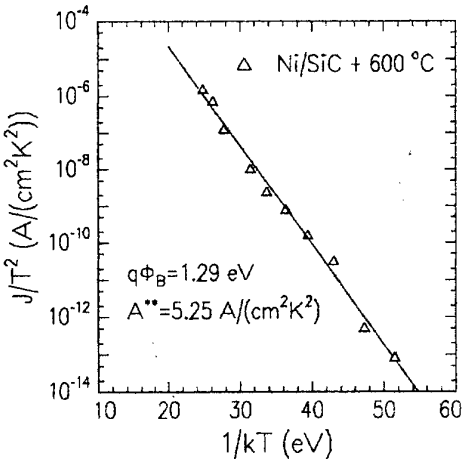


Fig. 2 – Arrhenius plot of the forward current of the Ni_2Si/SiC Schottky diode. The experimental Schottky barrier height ($q\Phi_B$) and the Richardson constant (A^{**}) are indicated in the figure.

This result was further confirmed by the I-T characteristic reported in figure 4. The Schottky barrier height was exactly the same also with this technique and the effective Richardson constant (A^{**}) was determined to be equal to 5.25 A/(cm^{2}K^2).

Low resistance ohmic contacts (3-4x10^{-5}Ωcm^2) in n-type SiC were fabricated by performing rapid thermal annealing of Ni/SiC samples in N_2 at 950°C. This kind of thermal process leads to rectifying contacts for substrate carrier concentration lower than 5x10^{17} cm^{-3}.

The analysis of the Schottky diodes with the Ni_2Si show that this system has a Schottky barrier of 1.3 eV.

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Characteristics of Schottky diodes on 6H-SiC surfaces after sacrificial anodic oxidation

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With extensive investigation for 6H-SiC device processes, commercial electronic devices are supposed to be realized soon. However, there are some difficulties in the processes. One of the difficulties is slow thermal oxidation rate of 6H-SiC, especially at (0001) Si face.[1)] This slow rate makes oxidation process time-consuming. In this work, we tried to perform anodic oxidation as a sacrificial oxidation process before contact formation. It has a great advantage that the anodic oxidation can be performed at room temperature.

n-type 6H-SiC samples with a net donor concentration of 10^{18} cm^{-3} were oxidized by applying voltage with a constant current of 1 mA/cm^2 in an electrolyte, which is a mixed solution of ethylene-glycol, water and KNO_3, for 4, 20 and 100 min. Then the oxide films were etched by HF. The Au and Ni were evaporated as Schottky contacts on the oxidized-etched surface, and Al contacts were also formed as ohmic contacts without annealing. As references, the metals were also evaporated on an as-received surface and a sacrificial thermal-oxidized-etched surface. Before the evaporation, each sample was dipped in HF and boiling water. We measured I-V and C-V characteristics for the Schottky contacts and evaluated contact resistances for Al ohmic contacts by the 4-point-pattern method.

Figure 1 shows the I-V characteristics for the Ni Schottky contacts on each surface. The Ni contacts on the as-received surface have an average ideality factor n of 1.1. The Ni contacts on the surfaces after sacrificial anodic oxidation show ideality factors n scattered within 1.1–1.4, and the Ni contacts on the surface after sacrificial thermal oxidation show n of about 1.1. The barrier heights $\phi_{I\text{-}V}$ obtained from I-V curves are 0.95 V for the as-received surface and 1.0–1.3 V for both oxidized-etched surfaces. The estimation of $\phi_{I\text{-}V}$ is somewhat unreliable due to deviation of n value from 1, but barrier heights measured from C-V characteristics $\phi_{C\text{-}V}$ show the same trend as $\phi_{I\text{-}V}$. The leakage current densities at a reverse bias of 20 V are of the order of 10^2 A/cm^2.

Figure 2 shows the I-V characteristics for the Au Schottky contacts on each surface. The n values for the Au contacts are larger than that for Ni contacts, in a range of 1.2–1.8. The $\phi_{I\text{-}V}$ for the Au contact on the as-received surface shows the lowest value of 0.90 V as in the case for the Ni contacts, while it is within 0.98–1.3 V for both oxidized-etched surfaces. The $\phi_{C\text{-}V}$ was also increased by the oxidation and subsequent etching. The leakage current densities at a reverse bias of 20 V are of the order of 10^3 A/cm^2, which is one order of magnitude larger than that for the Ni contacts.

Figure 3 shows contact resistances for the Al contacts on each surface. The contact

resistance is 1–10 Ωcm^2 on the as-received surface and 10^{-2}–10^{-1} Ωcm^2 on the oxidized-etched surfaces. Thus both the anodic and thermal oxidation processes reduce the Al contact resistance by about two orders of magnitude.

The above results show that both the anodic and thermal sacrificial oxidation processes have similar effects on the properties of the metal contacts. It has been reported that sacrificial thermal oxidation removes low crystallinity layer at the SiC surface.[2] The sacrificial anodic oxidation can also remove the defective layer and thus is expected to substitute for the sacrificial thermal oxidation.

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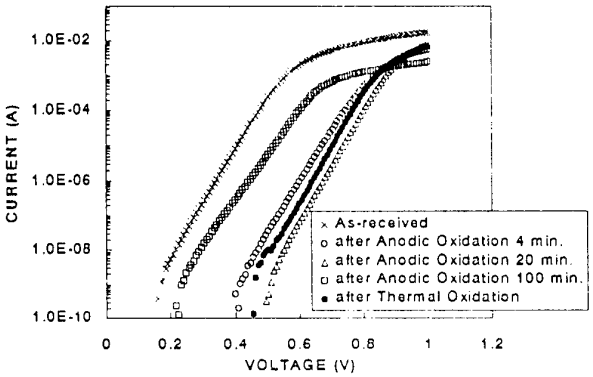


Fig. 1 I-V characteristics for Ni Schottky contacts on each surface.

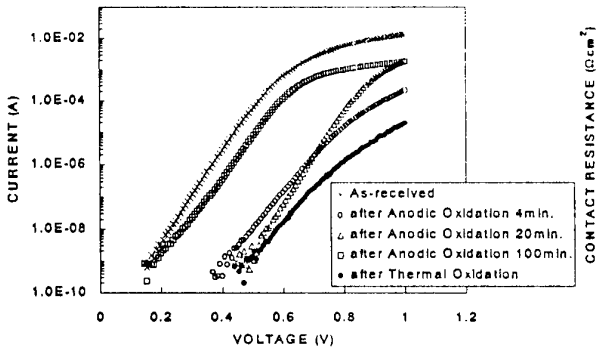


Fig. 2 I-V characteristics for Au Schottky contacts on each surface.

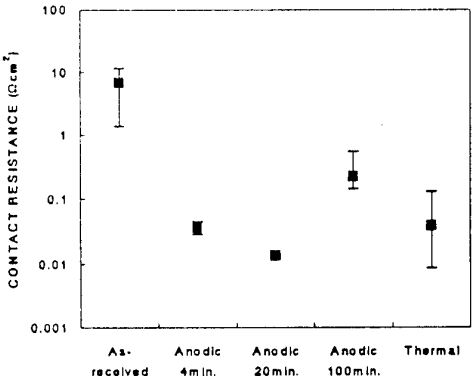


Fig. 3 Contact resistances for Al ohmic contacts on each surface.

Electrical Properties of Graphite/n- and p-Type Homoepitaxial Diamond Contact

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One important technological requirement for diamond based electronic devices is the production of reliable ohmic contacts. Graphitization of diamond induced by ion implantation is one of the commonly used methods for realization of ohmic contacts to semiconducting diamond. The details of the electrical properties, such as specific contact resistance between graphite and diamond, have not been clarified. This research exhibits the electrical properties of the graphitic electrodes formed in n-type and p-type homoepitaxial diamond films, respectively. Sulfur-doped diamond films with sheet resistance of 10^8 Ω/□w e re achieved by ion implantation in undoped homoepitaxial diamond (100) films grown by chemical vapor deposition (CVD) method. p-Type diamond films were synthesized by using trimethylboron (TMB) gas as a doping source in the CVD system. The graphitic electrode was formed by Ar^+ implantation with energy of 40keV and dose of $1\times10^{16}/cm^2$ at room temperature. The Au/Pt/Ti layers were deposited onto the electrodes and then annealed at 700°C in Argon. The electrical properties at graphitic electrode/diamond interfaces were investigated mainly by using the current-voltage (I-V) and the capacitance-voltage (C-V) measurements. It was clearly seen that the contacts gave a linear I-V characteristic from low voltage (0V) to high voltage (1500V), indicating that these interfaces have an ohmic property. The specific contact resistance (SCR) for graphite/n-type film was characterized to be in the order of 10^3 Ω·cm^2. This SCR value seems to be relatively high, but it is reasonable and enough to show the ohmic property for the present high resistive n-type diamond film. The more detailed results for n-type film as well as for p-type film will be discussed based on the electrical properties in graphite/n-type and p-type diamond films, which were characterized and compared by using linear transmission line model (TLM) and circular TLM extrapolation method (to avoid lateral current crowding effect).

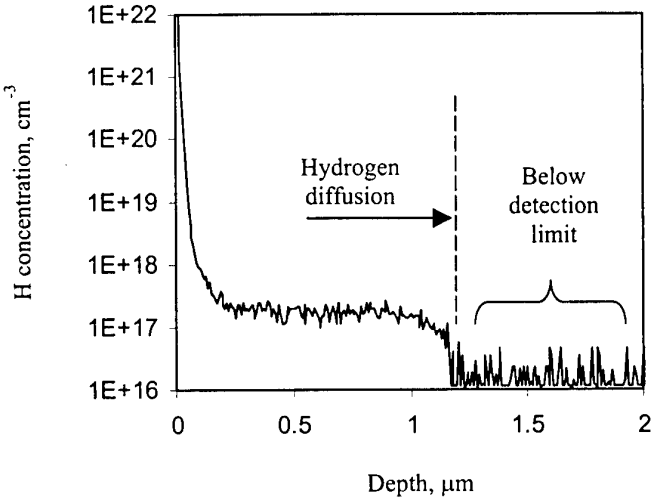
Hydrogen incorporation in SiC using plasma-hydrogenation

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A possibility to introduce hydrogen in SiC has been extensively investigated due to the importance of this topic for doping control during SiC device fabrication. The Ion Implantation technique was successfully used to study acceptor passivation in 4H and 6H samples [1]. A high temperature annealing in H_2 atmosphere was also applied to investigate passivation of nitrogen donors [2]. However, a possibility to introduce hydrogen in SiC samples by plasma hydrogenation stays an attractive alternative due to its ability to minimize surface damage inherent to the ion implantation approach as well as due to its much shorter processing times than for the case of high temperature annealing. Previous data on plasma deuteration showed a relatively shallow hydrogen penetration that could not be improved by subsequent high temperature annealing [3]. Annealing led instead to a significant reduction of the hydrogen concentration due to its outdiffusion from the samples.

It is suggested that the temperature of the plasma hydrogenation of 300^0C used in Ref. 3 is not enough to stimulate a sufficient level of H diffusion that requires much higher temperatures and/or processing times [4]. In this work we investigate the role of the sample temperature during its exposure to the hydrogen plasma on the efficiency of achieving hydrogen diffusion into the bulk of SiC crystals. Hydrogenation is performed in two different systems operating in the reactive ion etching (RIE) and the Inductively Coupled Plasma (ICP) modes at different microwave powers and pressures. Results of hydrogenation in an ICP plasma (750 W and 250 W microwave power on the top and the bottom electrodes respectively, 50 mTorr pressure) for 1 hr are shown in Fig. 1. In addition to the less than 0.1 μm deep shallow region similar to that observed after plasma deuteration in Ref. 1, a rather distinct diffusion front can be observed from this SIMS profile. An efficient passivation of Al acceptors was observed in this sample by low temperature photoluminescence spectroscopy [5]. This result is different from the SIMS profile observed after performing hydrogenation in the system operating in the RIE mode at the estimated temperature of about 300^0C. A denser plasma generated in the ICP system is expected to produce a higher degree of sample heating, which could be the reason for the much more significant level of hydrogen diffusion in this case.



Results of hydrogenation experiments at different powers and pressures during the hydrogenation will be reported and the role of the process conditions on the efficiency of hydrogen penetration will be discussed.

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Investigation of group IV nanocrystals formed by ion beam processing

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250 keV Ge ions were implanted into [0001] 4*H*-SiC bulk crystals or epitaxial layers at room temperature and 700 °C with an ion fluence of 10^{16} cm^{-2} causing a Ge peak concentration of approximately 1at% within the projected ion range (100...110 nm). After implantation thermal annealing was carried out at temperatures up to 1600 °C in Ar atmosphere (pressure 20 kPa) for 120 s with a double graphite strip RTA apparatus. The samples were analysed by means of Rutherford Backscattering Spectrometry (RBS), Cross Sectional Transmission Electron Microscopy (XTEM) methods and X-Ray Diffraction (XRD).
Whereas after room temperature implantation the implanted layers are amorphous, amorphization is prevented at 700 °C. A defect band occurs around 100...200 nm depth, i.e. deeper than the maximum of the Ge distribution (Fig. 1, left).

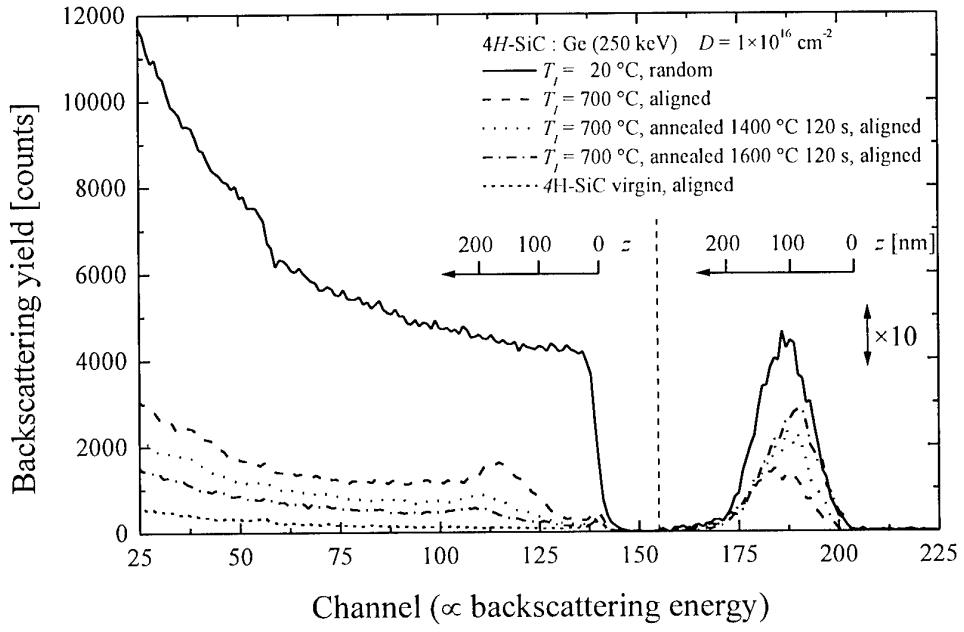


Fig. 1: RBS aligned and random spectra of a sample implanted at 700°C and annealed 120 s at 1400 °C and 1600 °C.

The decrease of the aligned RBS yield in the energy region of backscattering on Ge atoms (Fig. 1, right) with respect to the random yield (full line) indicates that a significant part of the implanted Ge is incorporated into the SiC lattice along the [0001] direction. Annealing yields to a further decrease of the damage concentration (Fig. 1, left) and an increase of the Ge content visible by the ion beam (Fig. 1, right) mainly in the near-surface region. This can be explained by the formation of Ge precipitates within the SiC lattice leading to an enhanced ion backscattering. By means of a special Z-contrast method (STEM-HAADF) in the same depth region Ge clusters with lateral dimensions between 2 nm and 12 nm were detected (not shown). High-resolution TEM identifies these clusters as Ge-rich cubic nanocrystals containing stacking faults (Fig. 2).

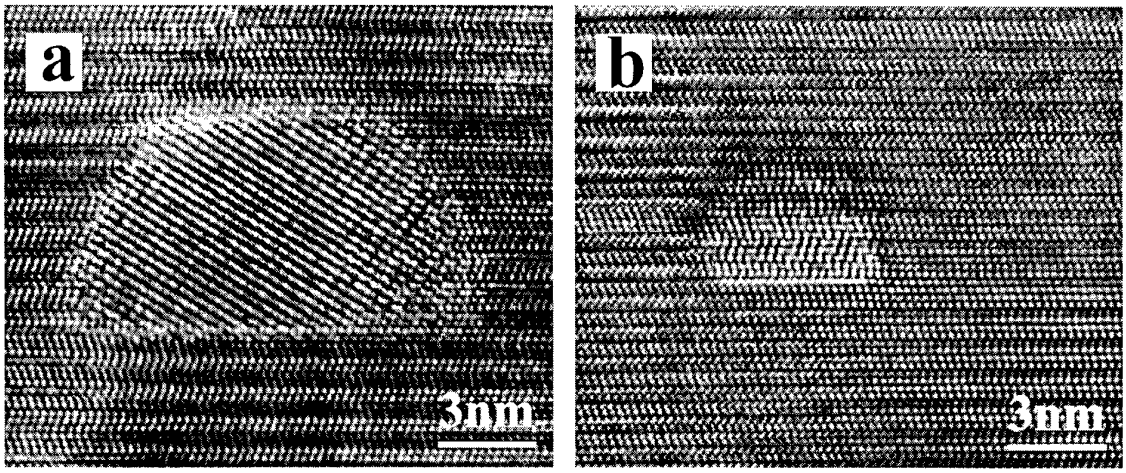


Fig. 2: HRTEM images of different Ge-rich nanocrystals formed after annealing at 1600 °C (viewed along [11-20]-direction of the 4H-SiC matrix).

The nanocrystals in most cases are not aligned with major SiC crystallographic directions which explains the increase of the RBS yield with respect to the as implanted case (Fig. 1). The existence of Ge-rich or Ge nanocrystals in Ge-implanted and annealed 4*H*-SiC layers is also confirmed by XRD analysis (not shown). The observed shift of the 111Ge reflection towards the value of crystalline Si may be the consequence of internal strain in the crystallites or be due to crystallites consisting of a mixture of Si and Ge.

The results show that Ge implantation into SiC in combination with subsequent annealing leads to the formation of Ge-rich nanocrystals.

Further investigations will be directed to the control of distribution, size and composition of the nanocrystals.

Recent progress in the preparation of a-$Si_{1-x}C_x$:H by thermal evaporation in Glow Discharge Decomposition of Methane

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ABSTRACT

Hydrogenated amorphous silicon carbide a-$Si_{1-x}C_x$:H films have been prepared successfully by thermal evaporation of silicon in an environment of glow discharge (G.D) decomposition of methane .The optimum conditions have been developed for the preparation of near stoichiometric thin films of a-$Si_{1-x}C_x$:H .The optimum conditions are, pressure of methane P_{CH4}= 5mbar, rate of deposition r_d=0.5 nm.s^{-1} , substrate temperature T_s=473K. G.D technique was used to produce carbon and hydrogen atoms to be mixed and embedded in the silicon films using capacitance technique at 18 cm distance within residual methane gas. The amorphous structure of the as-deposited and the annealed a-$Si_{1-x}C_x$:H thin films have been determined using X-ray diffraction (XRD), while the influence of hydrogenation on these a-a-$Si_{1-x}C_x$:H films have been studied using infrared IR absorption spectroscopy to confirm the hydrogen bonding of a-SiC:H, CH and a-Si:H as well as a-Si-C bond

The silicon content has been determined by atomic absorption spectrophotometer. The dependence of film structure and composition on the preparation condition was studied. The homogeneity of the films and the thickness have been examined by scanning electron microscopy SEM analysis .The optical band gap was found to increase up to 2.5 eV with increasing time of G.D (up to 60 min) decomposition of methane CH_4 using the capacitance technique with d.c biasing voltage =20V. while it decreases down to 2.25eV for G.D time of 90 min.

The optical enery gap E_g^{opt} has increased up to 2.48eV with increasing silicon content up to 60% with d.c biasing voltage but with a.c basing voltage, E_g^{opt} has decreased to its lowest value at 60 cubic centemeter per minute (ccm/min) as flow rate of methane, albeit we found that E_g^{opt} increases with increasing annealing temperature T_a. The carbon content was found to increase with increasing flow rate of methane. However the absorption edge has shifted to higher energies with increasing T_a . The band width (Urbach band tails) was observed to decrease with increasing T_s, albeit it shifted to higher values with increasing silicon content. The refractive index (n) and the real part of dielectric constant (ε_1) were found to decrease with increasing wavelength while it decreases with increasing silicon content at λ=780nm. The extinction coefficient (k') and the imaginary part of dielectric constant (ε_2) decrease with increasing wavelength .The D.C conductivity ($\sigma_{d.c}$) of a-$Si_{1-x}C_x$:H thin film was characterized by *3* transport mechanisms. The thermoelectric power and Hall effect at T_a=303K exhibit p-type for a-Si_{1-x} C_x:H thin film and then converted to n-type with increasing T_a up to 473K . Hall mobility μ_H of a-$Si_{51}C_{49}$:H increases methane up to **1113** $cm^2.V^{-1}.s^{-1}$ with increasing flow rate up to 60ccm/min and it decreased with time of **G.D** and also decreases with

increasing (T_a). Hall carrier concentration (n_H) is observed to decrease down to $2.5x10^{14}$ crn^3 with increasing flow rate of methane up to 60ccm/min, and then increases above that rate. However it increased with increasing time of G.D and then started to decrease down to $9.3x10^{14}$ cm^{-3}. on the other hand n_H has increased with increasing **T_a** up to 373K and then decreasing taking value of $7.13x10^{14}$ cm^{-3} . A.C. conductivity [$\sigma(\omega)$] of a-$Si_{1-x}C_x$:H films at T_a=473K was measured in the frequency range (100Hz — 10MHz) and at the annealing temperature range (305 - 453)K .The result is discussed in terms of the quantum mechanical tunneling QMT model of conduction, $\sigma(\omega)$ at f = 100 KHz increasing with increasing T_a up to 4.2 $x10^{-6}$ $\Omega^{-1}.cm^{-1}$ at T_a= 473K and then $\sigma(\omega)$ decreases with increasing silicon content down to 1.3x 10^{-6} $\Omega^{-1}.cm^{-1}$ at 40 at % **Si** and then increasing to 2.3 x $10^{-6}\Omega^{-1}.cm^{-1}$ at 50 at % **Si**.

A Novel Technology for the Formation of a Very Small Bevel Angle for High Electric Field Edge Termination

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The edge termination is an indispensable technology to achieve the bulk avalanche breakdown. Of numerous edge termination technologies, the positive bevel edge termination is most desired because it is the only approach being able to achieve the ideal avalanche breakdown. Besides, the drastically reduced surface electric field in a positive bevel edge terminated structure is expected to improve the device reliability. In this report, we present a technology that can form a beveled edge termination with a very low bevel angle. 4H-SiC diodes terminated by a 2° positive bevel fabricated with this technology are also presented.

In this method, a thick photo-resist (PR) is first spun on the sample. After exposure and development, a short time hot plate baking is conducted. The baking temperature and time are adjusted to control the shape of the PR pattern until the desired shape is achieved. The PR is hardened after baking. Since etching rate of semiconductor is much lower than that of PR, a mesa with a small bevel angle can be achieved using edge beveled PR pattern as the etching mask for inductively coupled plasma (ICP) etching. Figure 1 (a) shows the top view of the patterned PR before hot plate baking. The dimensions of the pattern are 130μm x 130μm. The inset is the thickness profile of the PR pattern. The thickness of the PR is 10μm. Figure 1 (b) shows the pattern after 160°C 10-second hot plate baking. The asymmetric bright pattern in Fig.1 (b) is caused by lighting and shading effect. The actual shape of PR after baking is symmetric. The thickness profile is shown in the inset. The PR at the edge shrinks to the center after baking, resulting in a beveled edge with a bevel angle of 20°. After 10 minutes ICP etching by the O_2/CF_4 plasma with a bias of 50V and a power of 700W, a beveled mesa with a depth of 0.9μm and a bevel angle of 2° is achieved. Figure 1 (c) shows the top view of the resulting beveled mesa after removing the PR. The inset is the thickness profile of the mesa. The

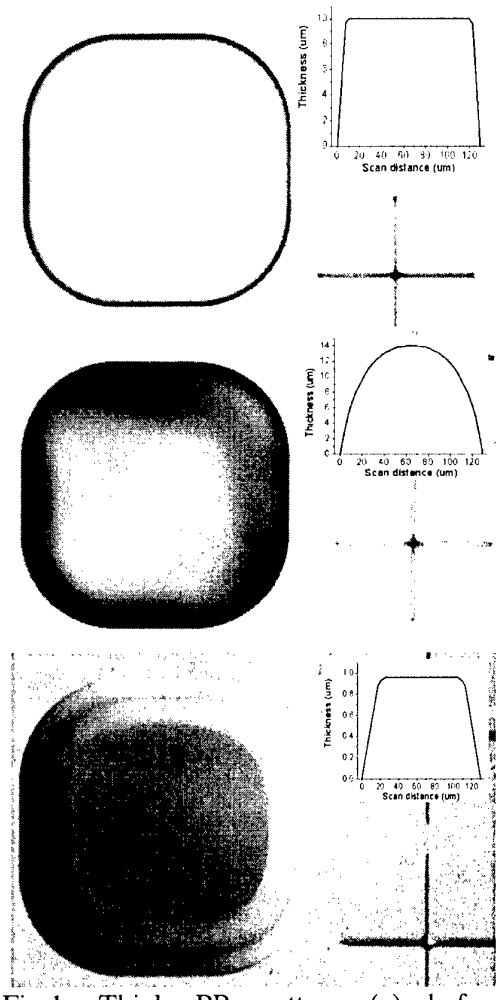


Fig.1: Thick PR pattern (a) before baking, (b) after a 160°C 10 second baking, (c) beveled mesa on 4H-SiC. Insets are thickness profiles

surface roughness of the bevel edge has been checked under SEM with 3000X magnification. No visible surface roughness has been observed.

The successful fabrication of very small bevel angle has been applied to the fabrication of 4H-SiC diodes on a wafer with SIMS profile shown in Fig.2. The wafer has a p^+pn structure grown on n^+ substrate. The doping concentration and thickness of the p^+, p, and n are $4x10^{19}/cm^3$ and 0.1μm, $2x10^{18}/cm^3$ and 0.2μm, and $3x10^{18}/cm^3$ and 2μm, respectively, with varied doping densities between p^+ and p, and p and n. Consider the varied low doping near the pn junction and the doping of the p layer being lower than the n layer, the resulting diodes have a positive bevel edge termination.

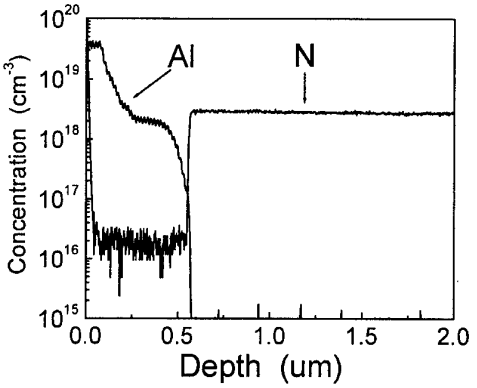


Fig.2: SIMS profile of 4H-SiC wafer

Figure 3 shows the reverse I-V characteristics of a fabricated 4H-SiC diode with 300μm diameter. Tests have been done at room temperature (RT), 100°C, and 150°C. The leakage current at 95% breakdown voltage is about $1x10^{-5}$ A/cm^2 at RT and $1x10^{-4}$ A/cm^2 at 150°C. This is comparable to the leakage current of avalanche photodiodes (APDs) with SiO_2 passiviation and multiple-step junction termination extension.[1] The diode runs very stably in deep avalanche at temperatures up to 150°C. Note that there is no passiviation layer protecting the edge of this diode. As shown in the inset, the breakdown voltage increases as the temperature increases, suggesting a positive temperature dependence of the breakdown voltage. The breakdown voltage at RT at $0.1A/cm^2$ is 63V.

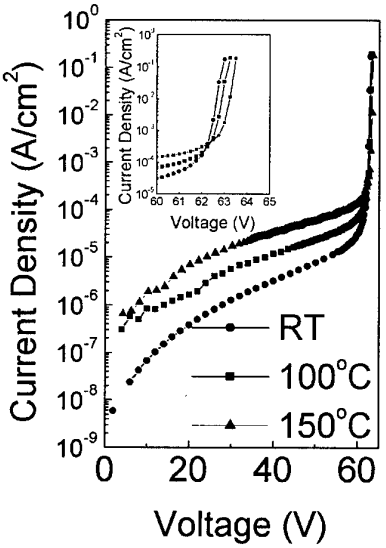


Fig.3: Reverse I-V characteristics of a 300μm diode terminated by a 2° positive bevel. The inset shows the details of breakdown at different temperatures.

In summary, a novel technology for the formation a very small bevel angle for edge termination has been developed. 4H-SiC diodes terminated by a positive bevel have been fabricated with this technology, which show a low leakage current and a positive temperature coefficient for breakdown voltage even though no passiviation has been applied to protect the edge. It should be pointed out that this technology is particularly useful for the fabrication of reliable APDs where and IMPATT diodes where high electric field junctions are normally easier to reach by dry etch process.

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Thermal analysis of GaN-based HFET devices Using the Unit Thermal Profile Approach

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GaN-based electronic devices have been demonstrated to be ideal for high power and high frequency applications. It is primary due to a two-dimensional electron gas (2DEG) generated in the AlGaN/GaN heterostructure. The 2DEG with a high mobility also permits low resistances and low noise performance not possible with SiC devices. However, GaN-based devices fabricated on the sapphire substrate are known to suffer from the serious heating effect due to the poor thermal conductivity. The thermal analysis for the GaN-based devices has been increasingly important since the heat dissipation can degrade the DC and the RF performance of devices, in particular during the high power operation. This study was motivated by the need for an accurate modeling tool for the prediction of device design to minimize the thermal effect and to optimize the device performance. This paper focuses on thermal analysis of particularly in AlGaN/GaN Heterostructure Field-Effect-Transistors (HFETs). To simulate thermal profile of device surface, approximate solution was employed. Typical geometry for modeling devices is the rectangular structure consisting of multiple layers of different materials with a rectangular heat source and the infinite double Fourier series is the solution. In our simulation, a circular embedded source was adapted instead of square heat source. Approximation of circular heat source was demonstrated as accurate as square heat source solution. Appropriate physical material parameters and structural parameters of device were implemented in the simulation. Figure 1 shows the simulated device structure. The thermal distributions around the gate of the device are shown in Figure 2 (a) and (b). It was shown that the peak temperature for the device using the sapphire as a

substrate reaches to about 280 ^{0}C with the input power of 1.5 Watts. The peak temperature when using the SiC as the substrate was calculated to be about 140 ^{0}C for the same input power. It was shown that the results of simulation match well with the experimental data. We expect that our thermal simulation lead to optimization of device performance and revised device fabrication is in progress with consideration of our thermal simulation.

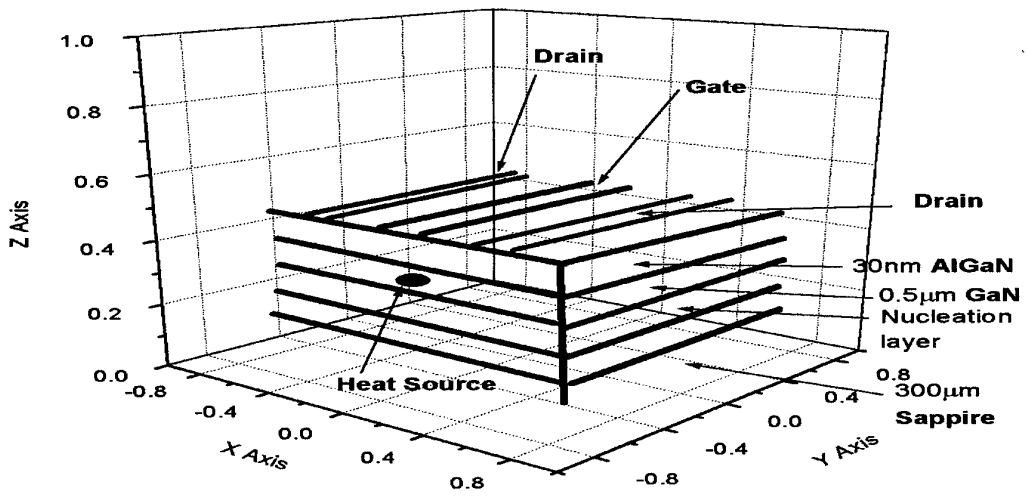
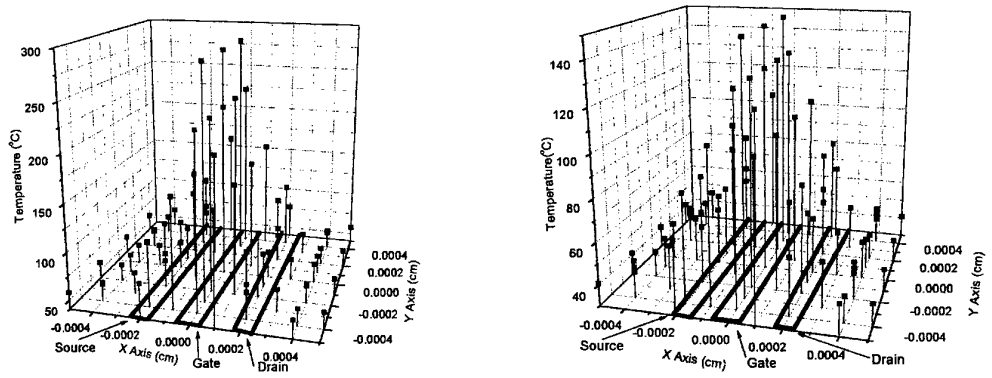


Figure 1 . The schematic simulated structure of the AlGaN/GaN HFET. Embedded circular heat source was placed under the AlGaN layer. The drawing is not in scale.



(a) (b)

Figure 2. Temperature distribution around the gate of the AlGaN/GaN HFET using a) the Sapphire substrate (thermal conductivity of 0.28 W/cm K) and b) SiC substrate (4.9 W/cm K). The gate width and length are 200 μm and 0.8 μm, respectively. The peak temperatures are about 285 °C (a) and 145 °C (b), respectively around the gate electrode.

Acknowledgment
Financial support for the second and the third group of authors are from the Ministry of Commerce, Industry, and Energy (# 990-02-03) in Korea.

Hole resonant tunneling through SiC/Si-dot/SiC heterostructures

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Si-based resonant tunneling diodes (RTDs) are of great interest for applications to high-speed electronic devices and have been studied using various material systems such as $Si/Si_{1-x}Ge_x$ [1,2], Si/CaF_2 [3], Si/SiO_2 [4]. However, the peak-to-valley current ratio is still low comparing with the GaAs-based RTDs and no room-temperature operations have been reported.

Among the many polytypes of silicon carbide (SiC), cubic 3C-SiC is a wide gap (2.2 eV) semiconductor and can be epitaxially grown on Si substrates. Since 3C-SiC/Si(100) has a wider valence band offset ($\Delta E_V \sim 0.5$ eV) than that of $Si_{1-x}Ge$, 3C-SiC is attractive for the hole barrier in RTD structures. Previously, we have investigated the 3C-SiC/Si multiplayer growth by supersonic free jet CVD and found that Si islands were formed on the SiC films at the initial growth stage [5]. Recently, we have reported the formation of SiC/Si-dot/SiC heterostructures on n^+-Si(100) and observed the current peaks and negative differential resistance due to the electron resonant tunneling from the dot structures [6]. In this study, we have grown the SiC/Si-dot/SiC heterostructures on p^+-Si(100) substrates and the current-voltage (*I-V*) characteristics were measured at room temperature by atomic force microscopy (AFM) with a gold-coated conductive tip.

The SiC films and Si-dots were grown by CH_3SiH_3 and Si_3H_8 free jets, respectively. The substrate temperature was set at 850 °C for SiC and 700 °C for the Si-dot growths. Figure 1 shows the AFM image of the sample obtained by the 1000 pulses of $CH_3SiH_3/Si_3H_8/CH_3SiH_3$ jets onto p^+-Si(100). The thickness of SiC films was estimated to be ~3 nm in this growth condition. The diameter and the height of the dots were typically ~10 nm and ≤5 nm, respectively. Figure 2 shows the *I-V* characteristics obtained from AFM tip on the dot a in Fig. 1. The current peaks and negative differential resistance were observed at -1.7 V. Based on the Si-dot height estimated to be 4 nm from AFM line profile analysis, we calculated the hole confinement energy levels. The obtained peak may be due to the resonant tunneling between the hole confinement energy level in the quantum well and the Fermi level of the emitter as illustrated in the inset of Fig. 2.

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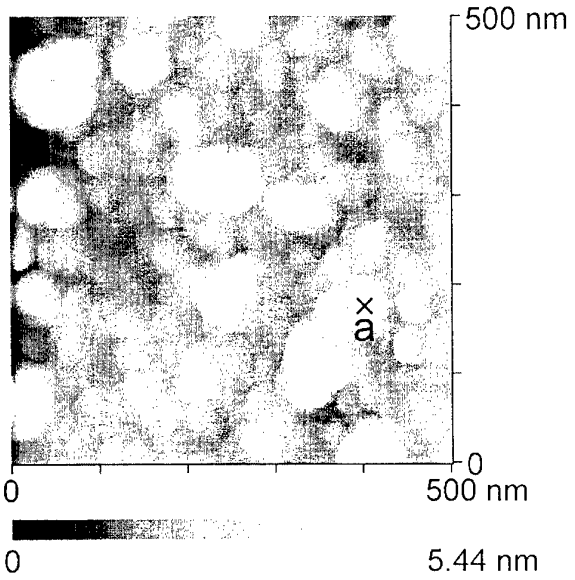


Fig. 1. AFM image of SiC/Si-dot/SiC/Si(100) surface morphology which was grown by 1000 pulses of $CH_3SiH_3/Si_3H_8/CH_3SiH_3$ free jets.

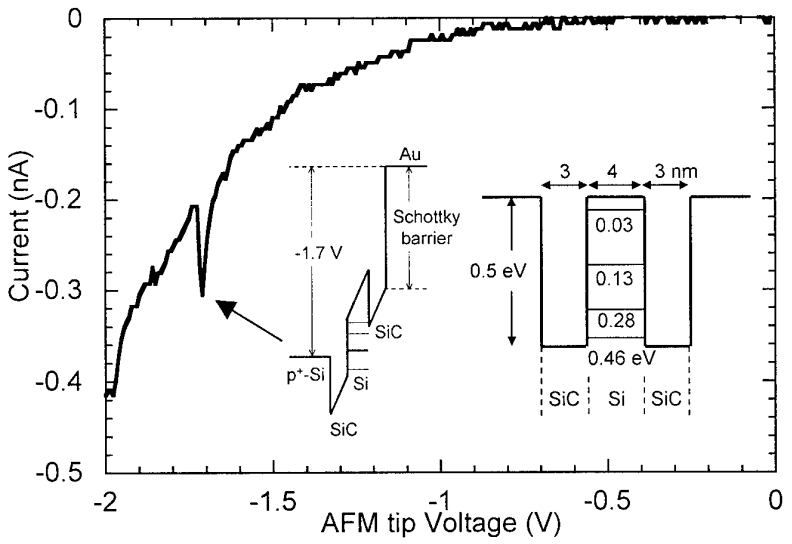


Fig. 2. *I-V* characteristics obtained from the point a in Fig. 1. together with calculated hole confinement energy levels.

Simulation of 5 kV Asymmetrical 4H-SiC Thyristor as Main Switches in EML Application and Study of its Junction Edge Termination

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The feasibility of using silicon power thyristor for Electric gun pulser has been established [1]. But a series array of a large number of devices is needed to achieve the required performance. The resulting size and weight of the pulser is non-optimal. The material properties of silicon carbide (SiC) indicate the potential of reducing the size and the power losses of the power devices [2]. This paper investigates the design and the performance of a 5 kV Asymmetrical 4H-SiC Thyristor as main switch in ElectroMagnetic Launching applications (EML). Based on the simulation results, an evaluation of 4H-SiC Thyristor is carried out with regard to electrothermal effect. A two-dimensional (2D) finite element simulation package ISE is used [3]. The ISE simulator first have allowed to estimate the maximum breakdown voltage for different thickness and doping level of an ideal plane parallel junction by using impact ionization coefficients given by Konstantinov [4]. Using these results (Fig. 1), a 35 μm epitaxial layer doped at 10^{15} cm^{-3} for the blocking layer of the thyristor should give a theoretical forward blocking voltage of 5700 V. Figure 2 shows the simulated structure where all parameters are indicated. We obtain V_F = 6V for 1800 A/cm^{-2} at 600 K.

As the periphery protection is an important issue in the design of SiC power devices, several techniques, such as MESA, Junction Termination Extension (JTE) and Epitaxial Guard Rings (EGR_s) have been studied. The optimal breakdown voltage for each technique will be presented. The study of the MESA shows that the best configuration is for a vertical etch that reaches the P buffer layer. The JTE is realised by forming at the peripheral of the device an N-type region in the P-type blocking layer by ion-implantation of nitrogen. For this region which spread in 150 μm at the peripheral, several couple of doping level and thickness of the JTE give the optimal breakdown voltage but the condition is to keep a dose of 9.10^{12} cm^{-2} of nitrogen (Fig. 3)

Another periphery protection, so called EGR_s, consist to etch the N-type epitaxial layer to form guard rings. The optimal design is obtained with 5 rings, the space between the rings is 2 μm, the ring width is 12 μm and the etch depth is 2.1 μm (Fig.4).

Futhermore we report on the simulation of the finite element thyristor inserted in the circuit application, shown in the figure 5, where the other component are Spice's model defined. The typical current for an Electromagnetic Launching application, is formed by the inductance L (L=30 μH) and the capacitance C (C=865 μF). Diodes are used as a crowbar switch. The schedule of condition imposed a thyristor able to switch a current pulse superior to 20 kA. We have then studied the minimal area of the thyristor that allows to obtain those current peak by considering the evolution of the temperature inside the structure due to the self heating (Fig. 6). The initial voltage at the capacitor is 5 kV. When the thyristor is switched-on the pulse current in the load (L and R in series) takes place. The figure 5 represents this pulse current waveform for an area structure of 20 cm^2. The current rate is di/dt = 160 A/μs, the maximum switching current is 25.7 kA and the drop voltage is only 5,5 V. By decreasing the area down to 1.5 cm^2, the maximum current is only reduced to 25.5 kA and V_F =35 V. the self heating in the structure increase the maximum temperature up to 700 K. The realisation of this device is on the way and the design has taken into account the simulation results.

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Figure 1 : Breakdown voltage for a plane parallel junction versus thickness and doping level of the blocking layer

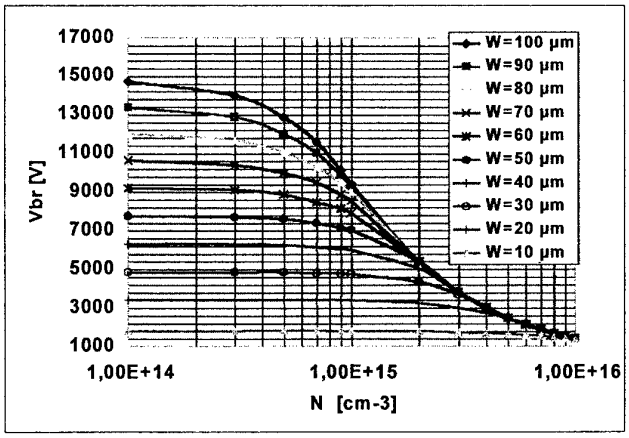


Figure 2 : Thyristor structure

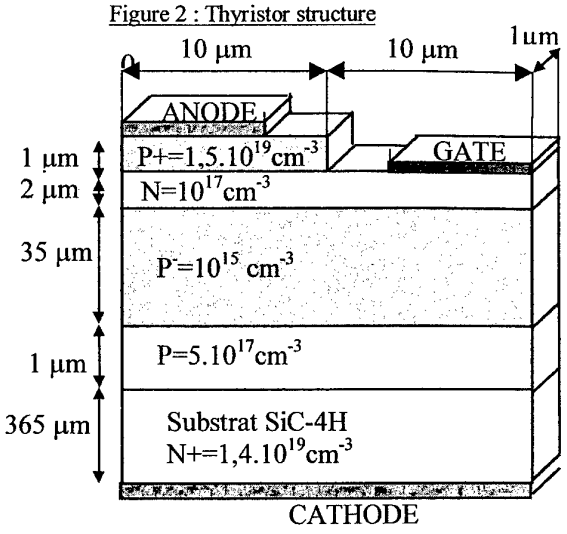


Figure 3 : optimised parameter for JTE

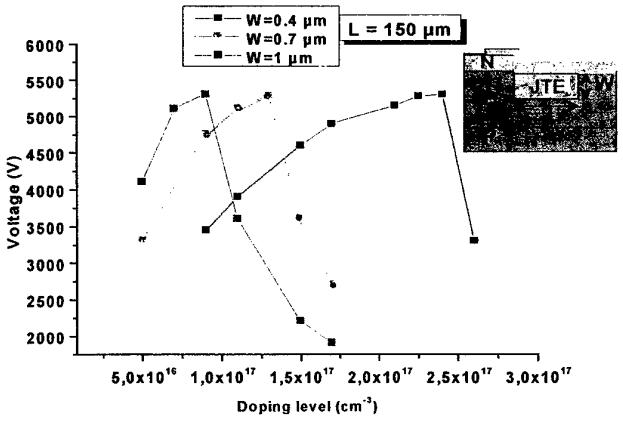


Figure 4 : voltage distribution in EGR_s

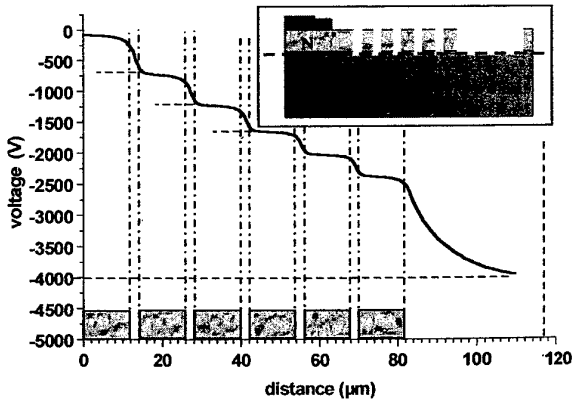


Figure 5 : application circuit and pulse current

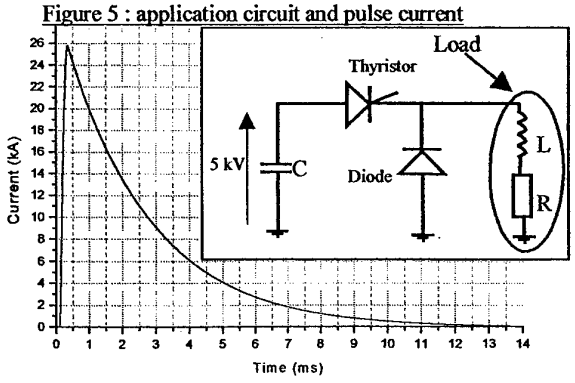
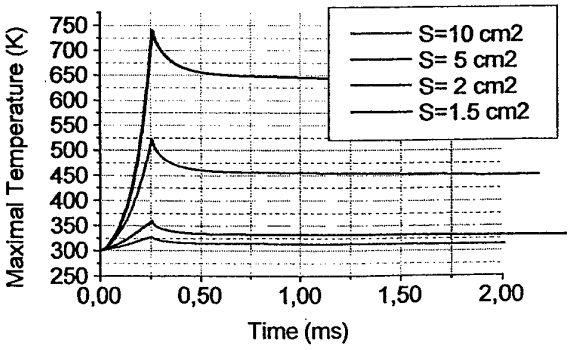


Figure 6 : Temperature versus area device



Dynamic Performance of 2.6 kV 4H-SiC Asymmetrical GTO Thyristors

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Silicon carbide shows tremendous potential for bipolar device applications such as inverters and switch-mode power supplies. Very recently, remarkable progress has been made in 4H-SiC based GTO thyristors. For example, 4H-SiC GTO thyristors with 2.6 kV forward blocking capability and up to 12 A of forward current were successfully demonstrated [1]. In this paper, we examine the turn-on and turn-off performance of these GTO thyristors.

A cross-sectional view of the thyristor structure is shown in Fig. 1. Five epilayers were grown on 380 μm thick, 8° off-axis 4H-SiC n-type substrates with resistivity of 0.02 Ω·cm. The blocking p^- (base) layer was 50 μm thick, doped to around 7×10^{14} cm^{-3}. The p^+ buffer layer served to block the spreading of the depletion layer under forward bias, thus making the device asymmetrical. The proper injection efficiency of the p^{++}(anode)-n(base) junction was provided by very heavy doping of the p^{++}-layer to 1×10^{19} cm^{-3}. It is worth noting that, owing to the relatively large ionization energy of Al in SiC (0.24-0.26 eV), only about 2 percent of the Al atoms are ionized at room temperature. As a result, the concentration of holes in the p^+-emitter grows exponentially with temperature in the range from 300 to 450 K.

Figure 2 shows the time dependence of the current density during the turn-on process in a 2.6 kV SiC thyristor at different temperatures. The steady state current density $j_o \approx 1200$ A/cm^2. It can be seen that the turn-on process is strongly temperature dependent. The total turn-on time is 1.2 μs at 293 K and only 0.4 μsec at 404 K. It can also be seen that at $T > 380$ K the temperature dependence of the turn-on process tends to saturate. Qualitative analysis, analytical calculations, and computer simulations have been made to clarify the origin of this effect. It is shown that the temperature ionization of the Al dopant in the p^+-emitter is mainly responsible for the effect. The hole concentration in the p^+-emitter grows sharply with increasing temperature, making the injection coefficient of the p^+-n junction larger.

We also report on the gate turn-off performance of 4H-SiC asymmetrical GTO thyristors with 2.6 kV breakover voltage, for temperatures ranging from 293 K to 500 K (Figs. 3-4). Both quasi-static and pulse regimes of the gate turn-off operation were studied. The temperature dependence of turn-off time and cathode holding current were investigated. At every temperature, there is a maximum value of cathode current $I_{Con\ max}$, which can be turned off by the gate current. At room temperature, $I_{Con\ max}$ is equal to 3.3 A which corresponds to current density $j_C \approx 1000$ A/cm^2. Turn-off current gain $K_G = I_C/I_G$ depends on temperature, the gate pulse duration Δt_G, and the current density in the on-state. The K_G is maximum when Δt_G is large (quasi-static turn-off by the current I_{Gst}). At $j_C = 1000$ A/cm^2, the maximum value of K_G is equal to 6. With j_C decreasing, K_G increases, and at $j_C = 300$ A/cm^2, $K_G = 12.5$. The above value of K_G is the highest reported for SiC GTO's. The turn-off gate current I_G increases with a decrease in Δt_G. The following semiempirical formula describes the I_G/I_{Gst} dependence well over the entire temperature range:

$$I_G / I_{Gst} = \frac{1}{1-\exp(-\Delta t_G / \tau^*)}, \qquad (1)$$

where τ^* is a fitting parameter which can be considered as a rough estimation of the carrier lifetime in the blocking base. The τ^* is found to grow exponentially from 0.6 to 3.6 μs in the temperature interval 293 – 502 K.

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This work was supported by the Office of Naval Research MURI program under Contract No N00014-95-1-1302, monitored by Dr. J. Zolper.

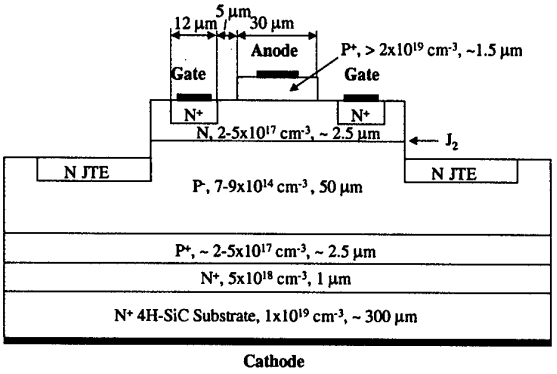


Fig. 1. Cross-sectional view of the thyristor structure under investigation.

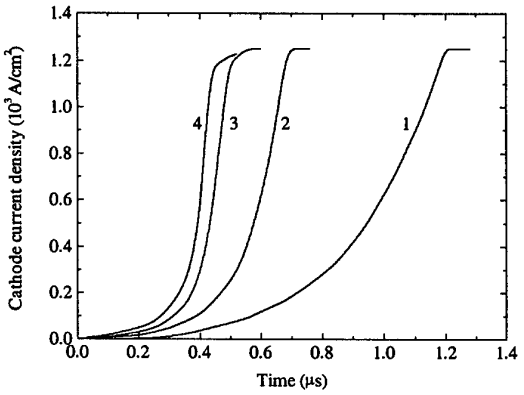


Fig. 2. Time dependence of the current density during the turn-on process at different temperatures. T (K): (1) 293, (2) 330, (3) 379, and (4) 404. Cathode voltage V_c = 200 V, load resistance R_l = 50 Ohm.

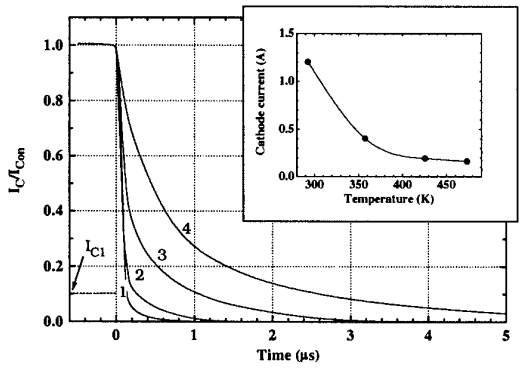


Fig. 3. The cathode current decay during the turn-off process at different temperatures. T(K): 1 – 293, 2 – 358, 3 – 426, 4 – 474. In all cases, a very long turn-off gate pulse of 100 mA is applied. For every temperature, the turn-off cathode current I_C is normalized to the cathode current $I_{Con}(T)$, where $I_{Con}(T)$ is the maximum current I_C that can be turned off by a 100 mA gate pulse. Inset shows the temperature dependence of I_{Con}.

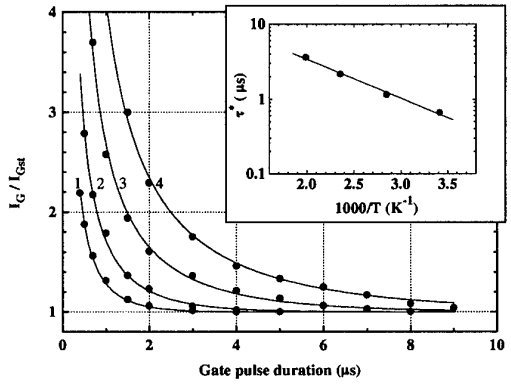


Fig. 4. The dependence of normalized turn-off gate current I_G/I_{Gst} on gate pulse duration at different temperatures. Solid lines are plotted according to Eq. (1) with τ^* as a fitting parameter. 1 – 293 K, 2 – 351 K, 3 – 424 K, 4 – 502 K. R_l = 25 Ohm. Inset shows the dependence of τ^* versus 1000/T.

Electrical characteristics of 6H-SiC bipolar diodes realized by sublimation epitaxy on Lely substrates.

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Sublimation epitaxy SE has several advantages over chemical vapor deposition such as a higher growth rate, possibility of in-situ etching...The aim of this work is to demonstrate the feasibility of bipolar diodes with high blocking voltages realized on layers grown by SE. This method allows to obtain n-type layers with doping level as low as N_d-$N_a \sim 5\times10^{15}$ cm^{-3} on n^+ 6H-SiC Lely substrates [1].

Epilayers with thickness between 10 and 20 μm have been grown, using a growth rate in the order of 15 μm/h. PN junctions have been realized by a triple implantation of Aluminum into such epilayers to create the emitter, with energies ranging from 70 to 180 keV and a total dose of 8.8×10^{15} cm^{-2}. A surrounding region, named Junction Terminal Extension (JTE), has been realized also by a 4-fold implantation of Aluminum, with energies ranging from 50 to 300 keV, with a total dose of 1.18×10^{13} cm^{-2}. The aim of this region is to decrease the probability of surface breakdown, by the spreading out of the equipotential lines. The diameters of diodes are in the range 200-800 μm. The JTE width is 250 μm, as shown by previous numerical studies.

Rectifying properties are observed in forward bias with current density between 5-10 A cm^{-2} at 2.5 V. In the reverse direction, structures has rather stable breakdowns (Figure 1) in the 800 V range. Values of the experimental breakdown voltage on diodes with the smallest diameter (200 μm) are in agreement with calculated values.

Temperature stability of this diode was investigated up to 1080 K (Figure 2).

Electrical characteristics of diodes realized on layers grown by SE epitaxy will be detailed in the full article.

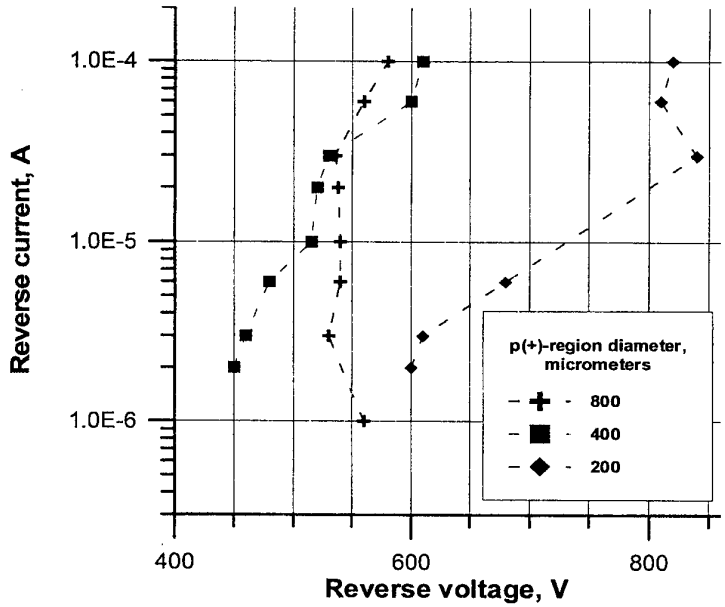


Figure 1 : Reverse current voltage characteristics of the diodes with different areas at room temperatures.

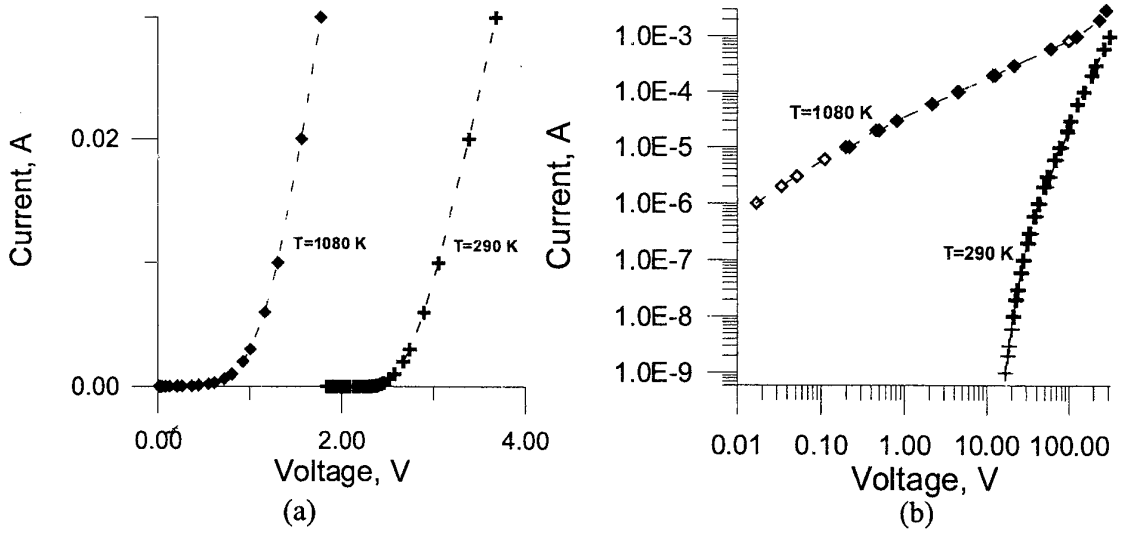


Figure 2 : Forward (a) and reverse (b) current voltage characteristics of the diodes with a diameter of 200 microns at room temperature and at 800°C.

This work was partly supported by INTAS grant N97-30834.

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On the Temperature Coefficient of 4H-SiC NPN Transistor Current Gain

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Silicon carbide (SiC) has been recognized as an attractive wide-bandgap material for high-power, high-voltage, and high temperature applications. While SiC power rectifiers are about to be commercially available, SiC power switches still require substantial development efforts. The major problems facing the MOSFET-based SiC power switches are the low inversion layer carrier mobility and the poor reliability of gate oxide under both high field and high temperature. GTOs are free of gate oxides but, being latch-on devices, are not as attractive for many power system applications such as motor control inverters. Before a novel high temperature and high power switch free of gate oxide becomes available, SiC BJTs could be a candidate for some system applications at high ambient temperatures. The disadvantages of BJT switches normally lie in two aspects. First, BJTs are current controlled switches. When designed to block high voltage and conduct high current, a substantial base current is needed. Darlington BJTs can reduce the complexity in implementing the base drive circuitry but with a substantially increased forward voltage drop. Second, BJTs normally have a positive temperature coefficient (PTC) for current due to carrier lifetime increase with increasing temperature, which makes paralleling power BJT difficult. Simulation work has, however, shown that SiC BJTs should have the desired negative temperature coefficient (NTC) due to acceptor Al's deep ionization energy (191 meV) [1]. The first experimental demonstration of 4H-SiC power BJT [2] observed an NTC while the subsequent reports reported both PTC [3] and NTC [4]. This paper focuses on the effects of base carrier lifetime, doping density, and acceptor energy level on the temperature dependence of NPN transistor gain. It will be shown that, depending on the carrier lifetime and base doping, 4H-SiC NPN transistors with Al-doped base could show both PTC and NTC. Besides, SiC NPN BJTs would generally have a PTC if an acceptor with E_A<170meV were used.

The 4H-SiC NPN cell structure used in the simulation is shown in Fig.1. Its J_C-V_{CE} curves at room temperature are shown in Fig.2. The acceptor energy level (E_A) has great effects on β as illustrated in Fig.3. When E_A<170meV, the device has a PTC in β. At E_A=170meV, the NTC in β begins to appear at current densities from 30 to150A/cm^2. When E_A=191meV, the temperature coefficient of β is negative up to 500A/cm^2 for the structure shown in Fig.1. Figs. 4 and 5 show the effect of electron lifetime in the base on β at different base doping concentrations. For a base doping concentration of 1×10^{17}cm^{-3}, the turning point of the temperature coefficient of β is at τ_n=0.291μs. Below 0.291μs, the temperature coefficient of β is positive. Above 0.291μs, the temperature coefficient of β becomes negative at around 60A/cm^2. At τ_n=2.908μs, NTC is found at the current densities from 20 to 150A/cm^2. For the base doping concentration of 2.5×10^{17}cm^{-3}, the turning point of the temperature coefficient of β is around τ_n=26ns. Below 26ns, the temperature coefficient of β is positive. Above 26ns, β has an NTC. With electron lifetimes in the base of 55ns and 257ns, an NTC is obtained at the current density up to 300A/cm^2 and 800A/cm^2, respectively. Thus, using higher base doping concentration can relax the requirement for carrier lifetime to obtain an NTC. The effect of the base doping concentration on β with an electron lifetime of 100ns is depicted in Fig.6. A PTC is found when the base doping concentration is smaller than 1.5×10^{17}cm^{-3}.

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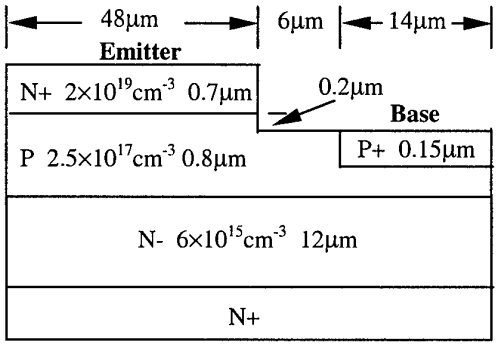


Fig.1 Cross-sectional view of 4H-SiC BJT

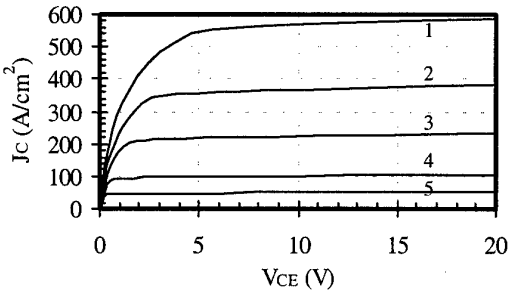


Fig.2 J_C –V_{CE} characteristics of 4H-SiC BJT at 300K.
In the base, $\tau_n=5\tau_p=0.1\mu s$, $\mu_n=441cm^2/Vs$.
1: $J_B=3.5A/cm^2$ 2: $J_B=7.1A/cm^2$ 3: $J_B=17.9A/cm^2$
4: $J_B=35.1A/cm^2$ 5: $J_B=71.4A/cm^2$

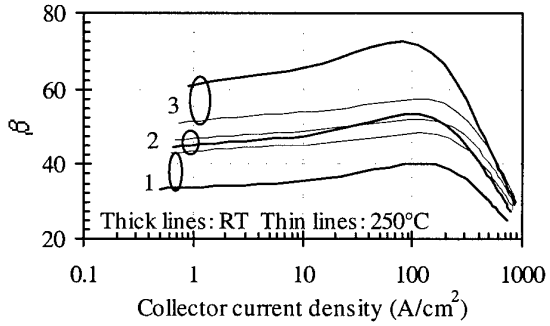


Fig.3 The effect of the acceptor energy level (E_A) on β.
$\tau_n=5\tau_p=0.1\mu s$, $\mu_n=441cm^2/Vs$, $N_B=2.5\times10^{17}cm^{-3}$.
1: $E_A=150meV$ 2: $E_A=170meV$ 3: $E_A=191meV$

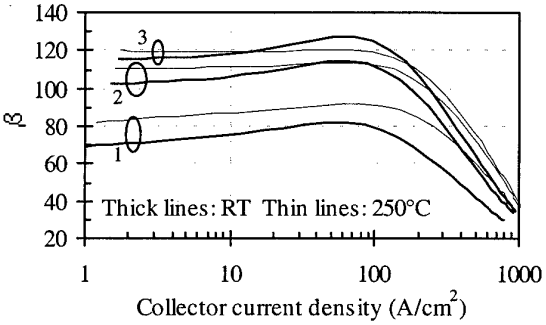


Fig.4 The effect of base carrier lifetime on β at a base doping concentration of $1\times10^{17}cm^{-3}$. $\mu_n=441cm^2/Vs$.
$\tau_n=5\tau_p$. 1: $\tau_n=0.058\mu s$ 2: $\tau_n=0.291\mu s$ 3: $\tau_n=2.908\mu s$

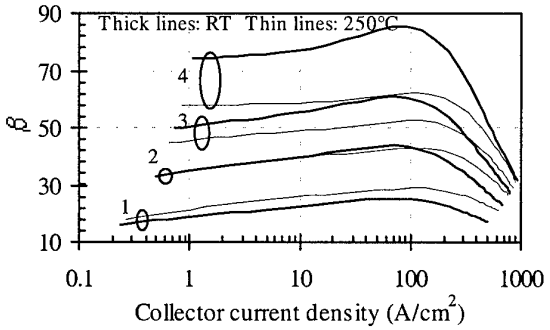


Fig.5 The effect of the carrier lifetime in base on β at a base doping concentration of $2.5\times10^{17}cm^{-3}$. $\mu_n=441cm^2/Vs$.
$\tau_n=5\tau_p$, 1: $\tau_n=10ns$ 2: $\tau_n=26ns$ 3: $\tau_n=55ns$ 4: $\tau_n=257ns$

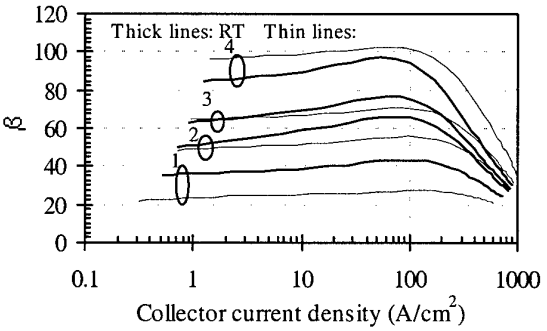


Fig.6 The effect of the base doping concentration N_B on β. $\tau_n=5\tau_p=0.1\mu s$, $\mu_n=441cm^2/Vs$.
1: $N_B=5.0\times10^{17}cm^{-3}$ 2: $N_B=2.0\times10^{17}cm^{-3}$
3: $N_B=1.5\times10^{17}cm^{-3}$ 4: $N_B=1.0\times10^{17}cm^{-3}$

A Novel High-Voltage Normally-Off Field Gated Bipolar Transistor in 4H-SiC

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The commercial availability of 3-inch wafers of 4H-SiC and the continued effort in scaling up SiC substrates by a number of companies are fostering a SiC power electronic industry. A lot of 4H-SiC high voltage and high speed devices have been demonstrated with the majority focusing on replicating the corresponding Si power devices in the hope of achieving higher power levels. It has, however, been realized that MOS-based SiC devices may not be suitable for applications under both high electric fields and high temperatures (over 150 C) due to the reliability concern of the gate oxide. In order to take full advantage of SiC superior material properties, SiC power switches free of gate oxide or insulator need to be designed and developed.

In this paper, a novel high voltage normally-off field gated bipolar transistor (FGBT) in 4H-SiC(patent pending) is proposed. Normally-off power switches are preferred over normally-on devices, which present substantial complication in practical applications such as motor control power inverters. The DC and transient characteristics of this device are investigated by performing two-dimensional numerical simulations. ISE SiC TCAD module is used in this simulation. The 4H-SiC material parameters used in the simulation are taken from most recently published literatures in order to obtain realistic results. The cross sectional view of the proposed normally-off FGBT is shown in Fig.1. A buried N^+ layer formed by using MeV deep Nitrogen implantation is used to collect the electrons injected from the emitter and to define the horizontal channel. A semi-insulating layer formed by deep Vanadium implantation is used to terminate the horizontal channel controlled by an implanted N^+P gate. The simulated DC characteristics are presented in Fig.2. The device is normally-off and blocks 3015V at 300K and over 3500V at 600 K. It can be turned on with gate voltages up to of 2.7V and 2.0V at 300K and 600K, respectively, with a negligible gate current. At 100A/cm^2, the forward voltage-drops are 3.82V and 3.58V at 300K and 600K, respectively. Since there is presently a large variation in carrier lifetimes in 4H-SiC materials although, being an indirect band gap semiconductor, its carrier lifetimes should be long, the effects of the variation of carrier lifetimes on the performance of the device have been studied and are depicted in Fig.3. The forward voltage drop improves when electron lifetime τ_n is increased to around 2μs. Although beyond 4μs the improvement is minimum for this particular design, longer carrier lifetimes should make it possible to design the device with a thicker base with improved blocking voltage capability. The vertical channel opening d is a key design parameter for high voltage normally-off FGBT. Its effects on blocking voltage and the forward current density at 5V are illustrated in Fig.4. The optimized value for d for a 3,000V FGBT is 2.5μm. The switching speed is a critical parameter for a power switch. The simulated switching waveforms for a resistive load circuit with an emitter current density of 200A/cm^2 and a blocking voltage of 1000V are summarized in Fig.5. With a dV_{GC}/dt of 5.4×10^6V/s, the turn-on time is 0.52us while the turn-off time is 1.17us at 300K. Experimental demonstration of the first 4H-SiC FGBT will be presented along with future work suggestions for improved device performance.

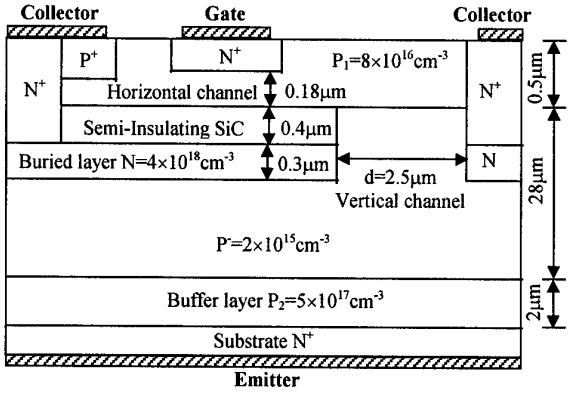
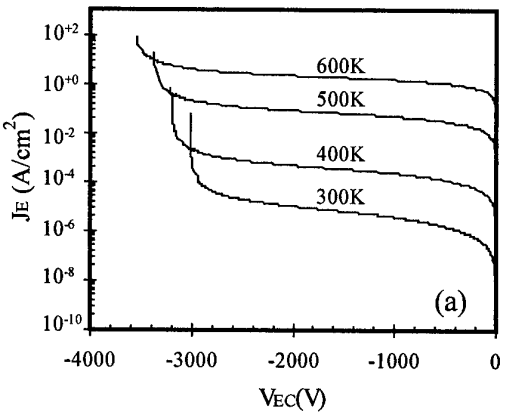


Fig.1 Cross sectional view of Normally-Off VJFET.



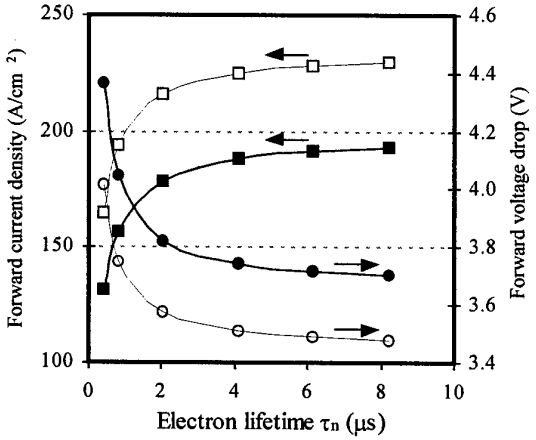


Fig.3 The effects of the variation of carrier lifetime.
Forward current density is measured at V_{CE}=5V.
Forward voltage drop is measured at J_E=100A/cm^2
Thick lines: 300K Thin lines: 600K

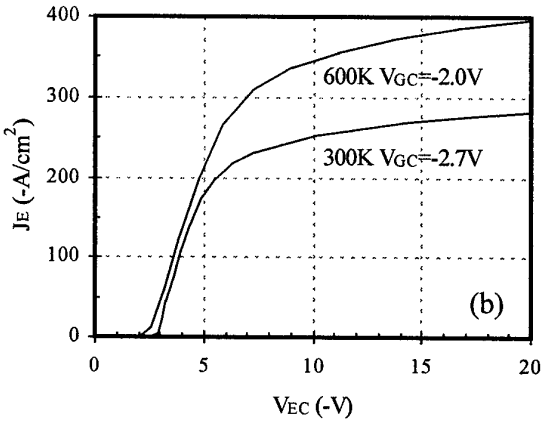


Fig.2 J_E-V_{EC} curves at (a) off-state and (b) on-state.

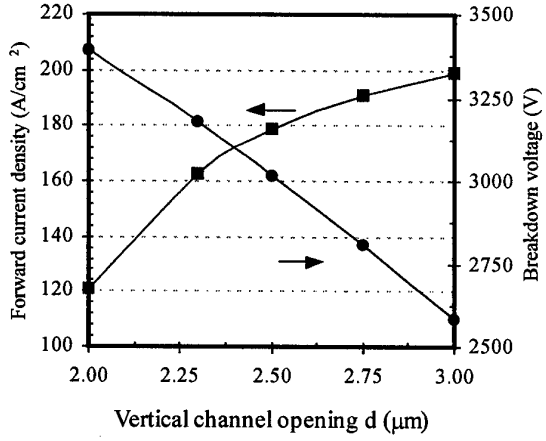


Fig.4 The effects of the vertical channel opening d on the forward current density at 5V and the breakdown voltage at 300K.

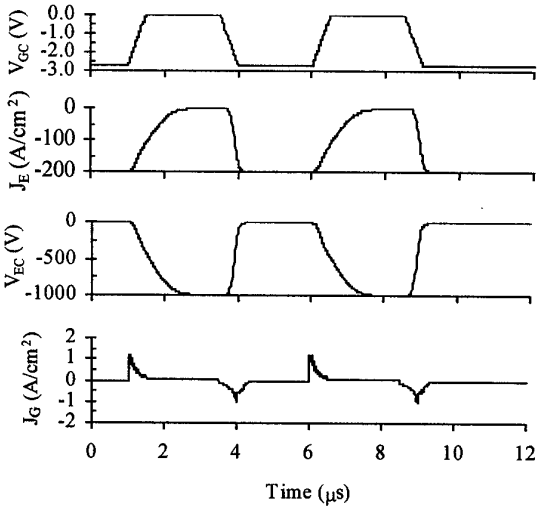


Fig.5. The switching waveforms at 300K.
dV_{GC}/dt=5.4×10^6 V/s.

Hybrid MOS-Gated Bipolar Transistor Using 4H-SiC BJT

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SiC has long been recognized as one of the candidates for high voltage, high temperature, high power applications. A novel MOS-Gated Bipolar Transistor (MGT) structure, which was demonstrated in silicon [1], was previously proposed in SiC [2]. Numerical simulations have proved that SiC MGT has several advantages over SiC IGBT, since it combines an n-channel turn-on MOSFET with an *npn* bipolar transistor, as well as a turn-off MOSFET. The schematic cross-section of the SiC MGT is shown in Fig. 1. The device is expected to have a wide Safe Operation Area (SOA) as well as a fast switching time [2]. However, current state-of-the-art 4H-SiC MOSFETs suffer from high interface trap density and low inversion layer mobility [3], making realization of a monolithic SiC MGT difficult. In this paper, we have used a silicon MOSFET driving 4H-SiC BJT to form a hybrid MGT and have characterized its performance.

The schematic of the hybrid MGT is shown in Fig. 2. The base current is provided by the turn-on MOSFET G1, which is commercial silicon MOSFET ECG 2380 with blocking voltage of 500V and on-resistance of 0.15Ω. A silicon MOSFET ECG 2984 with 50V voltage rating was used as the turn-off MOSFET G2 since high blocking capability was not required. The SiC BJT used in this structure was epi-base, epi-emitter 4H-SiC BJTs designed and fabricated by Cree Inc. [4]. The device has an on-resistance of $10.8 m\Omega \cdot cm^2$ and BV_{CEO} of 1800V.

Fig. 3 shows the forward I-V characteristics of the hybrid MGT structure. The MOSFET current I_{DS} forms the base current to turn on the BJT. As expected, there is a turn-on knee in the forward I-V characteristics, because the turn-on MOSFET G1, in between base and collector, prevents the SiC BJT from saturation. The forward drop at $100 A/cm^2$ (~1.4A) is about 4V. The maximum current is around 3A. The breakdown voltage of the hybrid MGT is limited by the blocking capability of the silicon MOSFET G1.

Fig. 4 shows the turn-on transients of the hybrid MGT. The rise time for the hybrid MGT is ~ 1.0μs. Fig. 5 shows the passive turn-off as well as the active turn-off of the hybrid MGT. During passive turn-off, the device is turned off by turning G1 off to stop the base current, so the turn-off recombination mechanism resembles an open-base turn-off of the bipolar junction transistor. At $100 A/cm^2$, the turn-off time is ~ 2.0μs. The device can also be turned off faster by using the turn-off MOSFET G2 to shunt current. Fig. 6 shows the turn-on and turn-off gate signals. The two gate signals have an offset to prevent shorting. From the active turn-off of Fig. 5, the turn-off time can be reduced to less than 0.5μs.

The hybrid MGT structure is a voltage-controlled device with good current-handling capability that circumvents the current MOS problems in 4H-SiC. It is a good example of application of SiC BJTs in power switching territory.

Acknowledgement: The authors gratefully acknowledge the support from MURI of the Office of Naval Research (Grant # N00014-95-1-1302) and NSF Center for Power Electronic Systems (Award # EEC-9731677).

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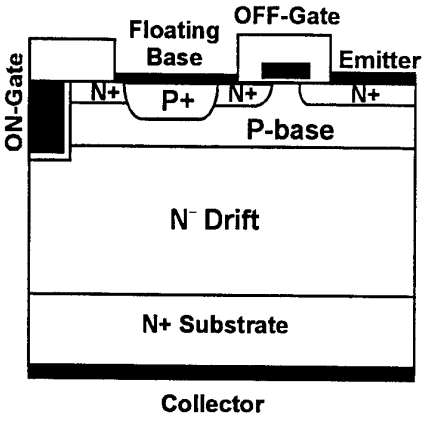


Figure. 1 Schematic cross-section of monolithic MOS-Gated Transistor

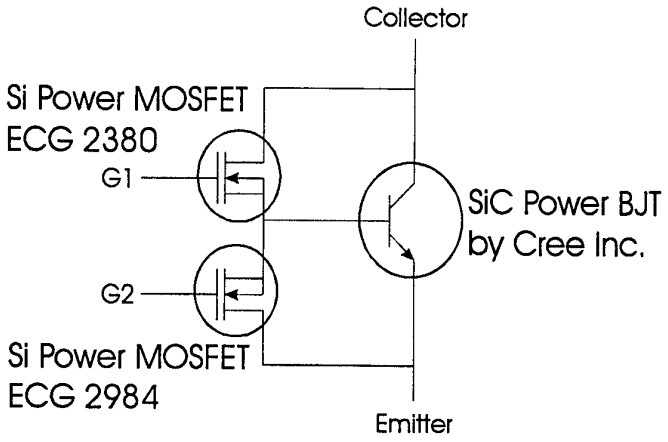


Figure. 2 Schematic of the hybrid MGT

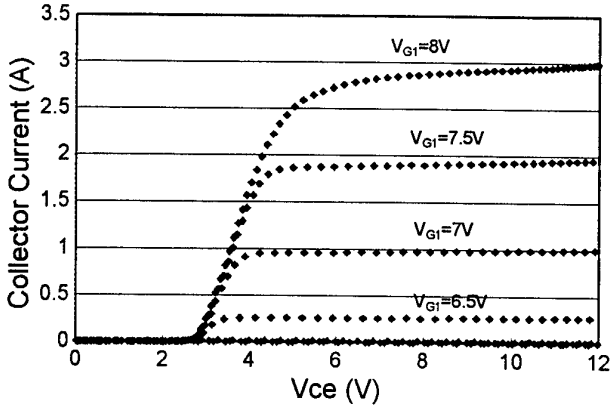


Figure. 3 Forward I-V Characteristics

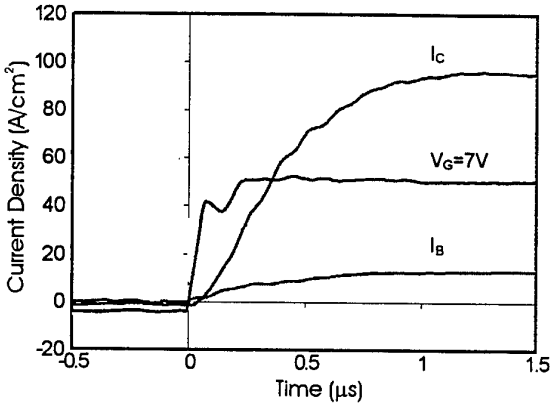


Figure.4 Turn-on transient of the hybrid MGT

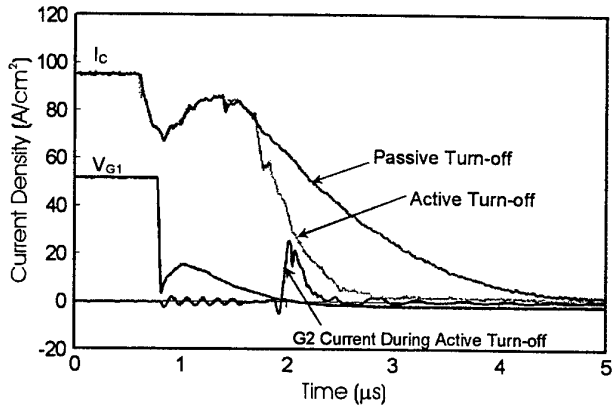


Figure. 5 Turn-off transient of the hybrid MGT

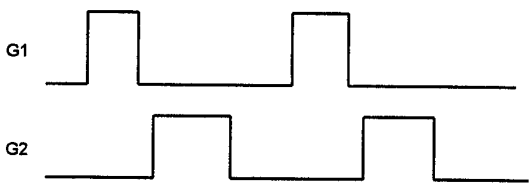


Figure. 6 Turn-off gate signals of the hybrid MGT

STUDY OF 4H-SiC HIGH VOLTAGE BIPOLAR DIODES UNDER REVERSE BIASES USING ELECTRICAL AND OBIC CHARACTERIZATIONS

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Silicon carbide presents electrical properties suitable for many applications especially for high voltage devices. 4H-SiC p^+nn^+ structures have been fabricated following Medici™ software simulations in order to sustain voltage as high as 6 kV. In particular, these diodes are realized by surrounding the emitter by a p-type region called JTE (Junction Termination Extension). The p^+ region and JTE were formed by multiple aluminum implantations at room temperature on n-type epilayer (40 µm-1×10^{15} cm^{-3}), followed by a thermal annealing at 1700 °C during 30 min. Current-voltage (I-V) characteristics at 300 K show good rectifying properties. Under reverse bias in air ambient, the curve presents two distinct zones (Fig. 1).

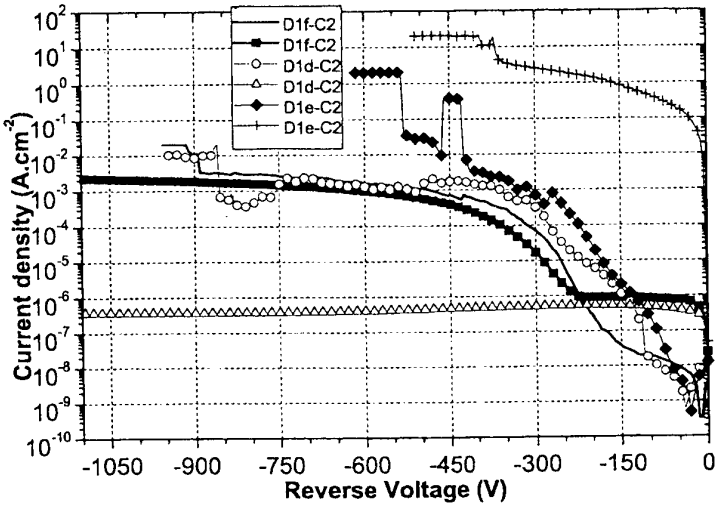


Fig. 1: Reverse electrical characteristics measured at 300 K in the air of diodes with JTE. Several bias sweeps are presented for each diode. The order of appearance in the legend corresponds to the order of I-V measurement performed on each diode.

In the first part of the initial characteristic, the current remains weak up to reverse bias, V_R = 200 V. Beyond this voltage, the current rises quickly until V_R = 400 V and saturate in the range [10^{-4}- 10^{-3}] A/cm². When V_R > 500 V, the electric arc between the anode contact and either the etched area of the sample or the moralization begin to appear. This second part of I-V curve is not reproducible. During the second measurement in the first part, we observe an increase in the current. For the second part of the characteristic, we note that for a same voltage the measured current is weaker. Those results are completed by I-V measurements performed in SF_6 ambient under small overpressure. In these conditions we observe the same behavior than in the air ambient. However, luminous white points in the emitter periphery accompany the electric arcs. Towards 2000 V the arcs involve the diodes breakdown with JTE. For the diodes without junction termination the maximum breakdown value reached is 1400 V. A luminous white points indicate the presence of a high electric field at this place.

This result is confirmed by comparing OBIC (Optical Beam Induced Current) measurements on diodes with JTE. No photocurrent is detected on JTE position and an OBIC signal peak emerges at the emitter edge for $V_R \approx 300$ V (Fig. 2). OBIC measurements performed on diodes without JTE (Fig. 3). When $V_R = 300$ V, we see a photocurrent peak at the edge of junction. Those results indicate a presence of high electric field at this place. It means that the JTE are not completely effective. The presence of high electric field to this voltage lets think that there are positive charges on the SiC surface which induce a degradation of the JTE performances. The instabilities of current noted during I-V measurements could confirm these assumptions. These measurements completed by OBIC measurement at several wavelengths and with high voltage will be analyzed in the full paper. The role of electrical activation of aluminum and surface effects will be discussed.

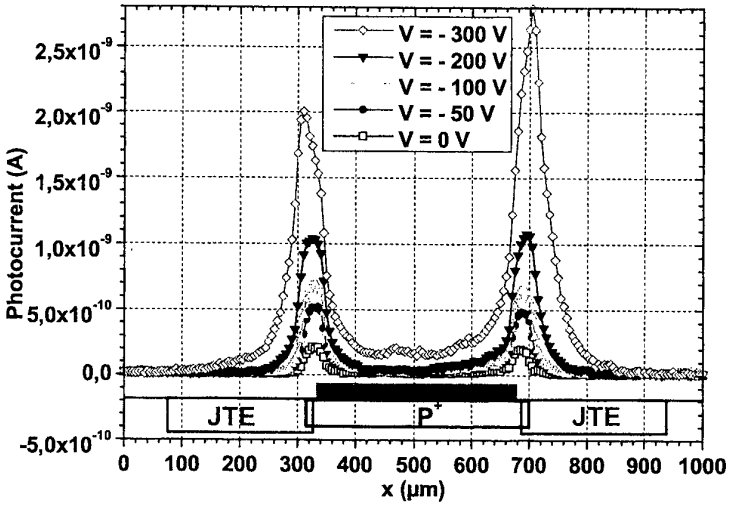


Fig. 2: OBIC measurements performed on diode with JTE at $\lambda = 363.8$ nm with $P_{opt} = 1$ W/cm² for different reverse voltage.

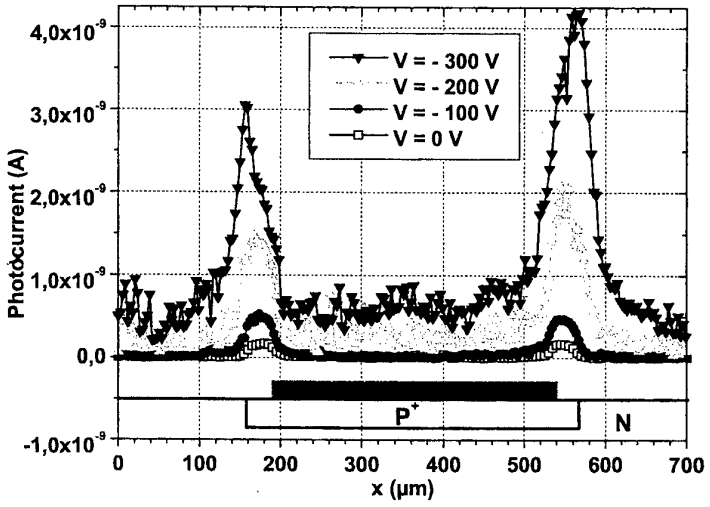


Fig. 3: OBIC measurements performed on diode without JTE at $\lambda = 363.8$ nm with $P_{opt} = 1$ W/cm² for different reverse voltage.

Highly doped implanted pn junction for SiC Zener diodes fabrication

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The objective of this work was to use implantation process to form a two side highly doped pn-junction (figure 1) in order to obtain a Zener effect. In the fabrication process we used 6H-SiC substrates N type 0.043 ohm.cm (4e18 cm^{-3}) from CREE. We performed a multiple Al implantation through a mask layer using 6 energies ranging from 330KeV to 2000KeV and two implantation temperatures (room temperature and 305°C). The total implanted dose was 5.39e15 cm^{-2} and a square box profile with a plateau chemical concentration of 4e19 cm^{-3} was expected. The peripheral protection was made by mesa etching and the contact was made with an annealed Ti/Ni metal layer.

Implantation and activation properties have been studied by physical (RBS, SIMS) and electrical (TLM, Van DerPauw) characterisation. MESA diodes have been characterised electrically measuring their static I-V characteristics. In figure 2 we represented the I-V curves of the diodes implanted at RT (sample S105) and 305°C (sample S104) for different contact annealing temperature. Before contact annealing, there is a significant difference in current capability between samples implanted a room temperature and at 305°C. After contact annealing at 900°C, the linear region of the I-V curve is similar for both samples but the series resistances are still lower for the 305°C implanted sample. When operation temperature is increased, the diode behaviour exhibits the standard decrease of the offset voltage and increase of the current for a given on-state voltage (figure 3). In the reverse mode, the diodes behaviour is particular due to the inherent structure the junction: N-side of the junction (substrate) is doped 4e18 cm^{-3} and the implanted P-type doping (extracted from TLM) is 3.35e18 and 6.3e18 cm^{-3} for RT and 305°C implantation, respectively. With these high doping levels, Zener mode conduction (tunnelling leakage currents) can be expected when the diode is reverse biased. In figure 4 the reverse I-V curves of a 305°C implanted diode are presented. We can infer three conduction regions in the reverse mode. Up to 8V, a first leakage current region similar to standard reverse biased pn diode dominated by generation/recombination currents is observed. From 8 to 42 V we can note a first increase of the leakage current. This leakage current is a tunnelling current as was confirmed by numerical simulation. A second change in the current slope is observed at 42V but it is not clear that a complete avalanche process is responsible for this current increase, unlike simulations are predicting. Figure 4 shows the reverse I-V curves of the diode for 4 consecutive measurements reaching a current of 0.1 A, corresponding to a current density of 150A/cm^2. There is no destruction nor degradation of the device and the I-V curves are very repetitive. This seems indicate that the reverse current flow is taking place through the plane area of the junction and not on the border of the device. This has to be confirmed by OBIC measurements. This behaviour is absolutely necessary to use the diode as a protection device.

When comparing the reverse characteristics of RT and 305°C implanted diodes (figure 5) we observed that the leakage current is higher for RT implanted diodes at low voltage bias (0 to 8V). This behavior has to be checked. It could be due to a higher quantity of defect, especially in the junction region. The influence of the contact annealing on the reverse current shown that the leakage current decreases at low voltage bias after annealing at 700°C. It is possible that defects have been removed by the contact annealing process.

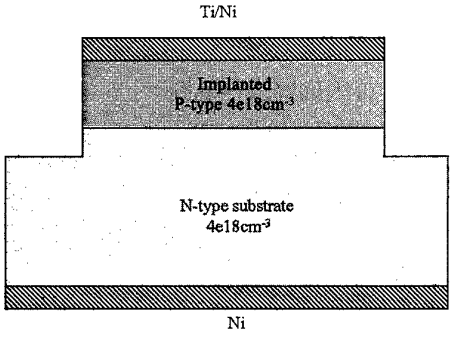


Fig. 1: Schematic cross section of the targeted implanted pn-diodes

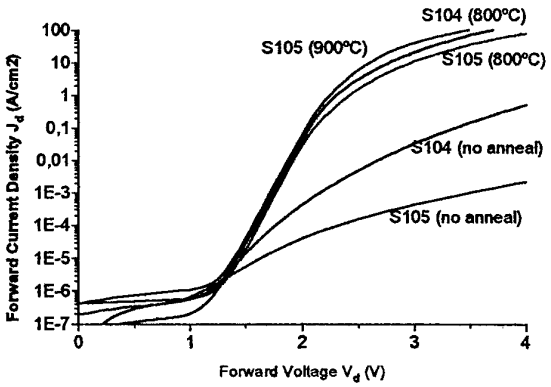


Fig. 2: Forward voltage characteristics of fabricated diodes: S104 is implanted at 305°C and S105 is implanted at room temperature.

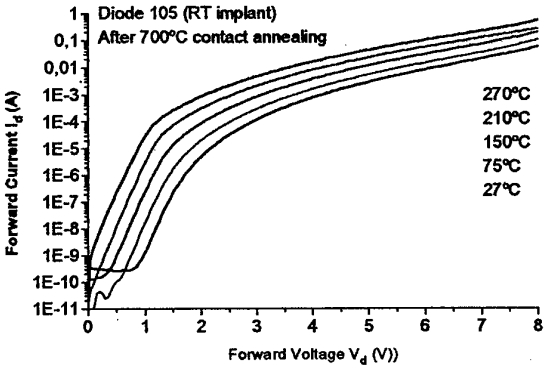


Fig. 3: Forward characteristics of a S105 diode annealed at 700°C measured at various temperatures

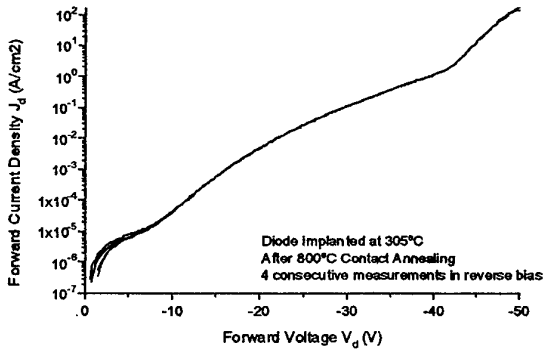


Fig 4: Reverse I-V curves of a S104 diode measured up to 100mA 4 times consecutively.

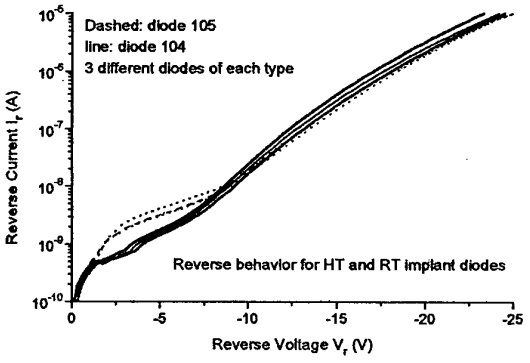


Fig 5: Reverse I-V curves (3 of each) of a S104 diode and a S105 diode

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4H-SiC pn diode grown by LPE method for high power applications

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Silicon carbide is a promising wide bandgap semiconductor material for high power applications requiring operation at high temperatures. Despite considerable progress in fabricating high power and high voltage SiC devices by CVD method, the problems with reducing defect density (micropipes) in SiC epitaxial layers and with increasing device lifetime (degradation of device characteristics connected with deep traps) remain critical tasks. Recently, it has been demonstrated that the micropipe defect density it is possible to reduce using the LPE process. It was found that the SiC epitaxial layers grown by LPE has the lower deep trap density in comparing with SiC epitaxial layers grown by CVD method. The objective of this research is to fabricate 4H-SiC pn diode using LPE method for high power application.

4H-SiC pn diode consisted from four epitaxial layers was grown by LPE method. First, a n^+-layer was grown. It serves as the layer for closing micropipe defects that usually exist on commercial substrates. The n^+-layer was deposited on (0001)Si face of the commercial 8^0-off axis 4H-SiC substrates. The thickness of the n^+-layer was about 10 μm. An undoped n_0–layer was deposited on the n^+-layer. The thickness of n_0–layer was found to be 10-15 μm. N_d-N_a concentration in this layer was determined to be $(9\times10^{15} \div 3\times10^{16})$ cm^{-3} for different samples. Al doped and Al heavily doped epitaxial layers were grown on n_0–layer in that order. The thickness of Al doped layers was (1.0÷1.5) and (2.0÷2.5) micron for p^+-layer and p–layer, respectively. N_a-N_d concentration in the p-layer was found to be $(3\div6)\times10^{18}$ cm^{-3}. The N_{Al} concentration in the p^+-layer was determined using SIMS technique to be 3×10^{19}-2×10^{20} cm^{-3}.

Low resistivity ohmic contacts to the both n- and p^+-sides of the diode have been formed. An AlSi(2%)Ti(0.15%) alloy has been used as a p-type contact to the LPE 4H-SiC layer. The metal film with a thickness of 100 nm was deposited by an e-beam evaporation in vacuum of 1×10^{-6} torr. The AlSiTi contact was formed in a resistance furnace in an argon atmosphere at 900 °C. After annealing a reproducible contact resistivity of 8×10^{-5} $\Omega.cm^2$ has been measured. After the contact formation Au was deposited as a top layer. The ohmic contact to n-side was formed using Ni. A 100 nm thick film was also deposited by e-beam evaporation at the same conditions. The annealing has been performed at temperature of 950 °C and a contact resisitvity of 5×10^{-5} $\Omega.cm^2$ has been obtained. After the ohmic properties formation an additional contact film consisted of subcequently evaporated Ti/Pt/Au layers was deposited to improve the backside metallization. The thermal stability study of the both contact types established that they were

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stable during the long time ageing at a temperature of 500 °C in nitrogen and in operating temperatures up to 450 °C in air.
The diode chip was attached to the gold-plated MoCu-base plate of the ceramic package using a high temperature eutectic Au(88%)-Si(12%) alloy. The contact pads on the diode top side were connected to the package lead by a gold wire. The electrical measurements were made up to 300 °C without degradation of the packaged diode.
The forward I-V characteristics measured at high current density up to 1.5×10^3 A/cm^2 were studied at different temperature. The reverse I-V characteristics showed an abrupt breakdown at voltage about 500 V. It was found that the breakdown electrical field for the pn junction was ~1.3×10^6 V/cm. The C-V measurements were performed at different test frequencies of 10 kHz and 1 MHz. The impurity concentration Nd-Na was uniform and did not depend on test frequencies indicating on low concentration of deep traps in n_0-layer. The C-V data indicate an abrupt pn junction. The value of built-in potential was determined to be about 3.0 eV that is close to theoretical value for 4H-SiC pn structure doped with nitrogen and aluminum.
Electrical characteristics of 4H-SiC pn diodes will be reported in detail.

Acknowledgements
This work is supported by NATO grant # SfP-971879 for that the authors express their gratitude.

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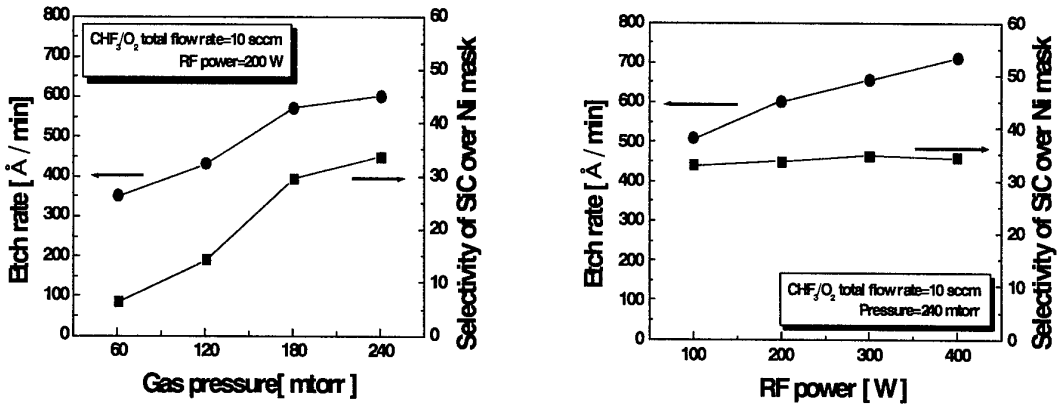
Reactive Ion Etching Process of 4H-SiC Using the CHF_3/O_2 mixture with a Post O_2 Plasma Etching Process

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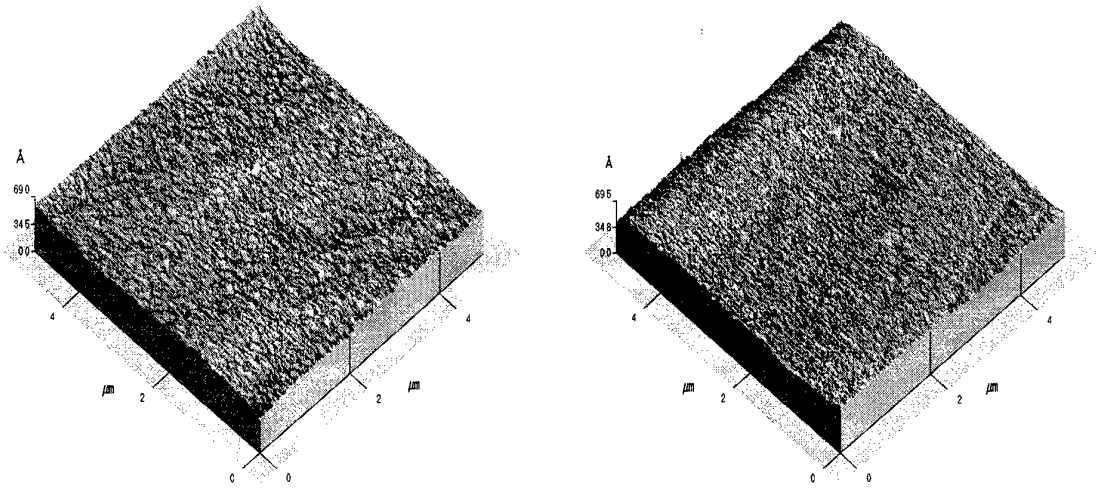
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There are several reports on the RIE (Reactive Ion Etching) process of SiC wafers using the CHF_3 as a source gas with additional H_2 or O_2 gas for the improvement of etching characteristics. It is known that the addition of H_2 gas in the CHF_3 can significantly reduce the amount of residues on the surface of etched SiC. However, the etching rate of the processing is known to relatively low. When O_2 gas is employed instead of H_2 gas with CHF_3, the etching rate can be enhanced due to a selective etching of C component in the SiC, but the surface roughness of the etched surface is known to increase due to the formation of residues. In this paper, we report on the RIE etching process of 4H-SiC wafer using the CHF_3/O_2 mixture with a consecutive O_2 plasma etching process. It was found out that the etching rate is enhanced by the addition of O_2 gas into CHF_3, while the surface roughness is significantly improved by the post O_2 plasma etching. SiC wafers with an n-type epitaxial layer grown on highly doped n-type 4H-SiC substrate were used for the RIE process. The etching rate for the RIE etching using the CHF_3/O_2 mixture was found to increase from 500 Å/min to 710 Å /min when the RF power was increased from 100 W to 400 W (Fig.1(a)). The etching rate is also increased from 350 Å/min to 600 Å/min when the gas pressure is increased from 60 to 240 mtorr at the RF power of 240 W (Fig.1(b)). The surface roughness of the 4H-SiC after the RIE with the CHF_3/O_2 mixture without the post O_2 plasma etching was measured to be about 5.0 Å. The roughness was found out to be decreased down to about 1.2 Å when the sample was accompanied with the O_2 plasma etching after the RIE with the CHF_3/O_2 mixture (Figure 2). The SEM (Scanning Electron Microscopy) analysis showed no evidence of formation of a trench which is generally induced by the excessive flow of ions reflected from the etched surface. It was concluded that the RIE etching process using the CHF_3/O_2 mixture with a consecutive O_2 plasma etching process results in a promising etching characteristics for the fabrication of SiC devices.



(a) (b)

Fig. 1 The RIE etching rate of 4H-SiC using the CHF_3/O_2 mixture etching as functions of a) gas pressure and b) RF power.



(a) (b)

Fig. 2 AFM of the surfaces of 4H-SiC etched by CHF_3/O_2 mixture a) without the post O_2 plasma process (RMS roughness of 5.0 Å) and b) with the post O_2 plasma process (RMS roughness of 1.2 Å).

ACKNOWLEDGEMENT

This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea. and by a fund from the Korea Research Foundation made in the program year of 2000 (# KRF-99-041-E00509).

FrA1 GaN Device and Bulk Growth

[redacted]

Recent Progress of AlGaN/GaN Heterojunction FETs for Microwave Power Applications

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Keywords: AlGaN, GaN, heterojunction, FET, power device, sapphire substrate, SiN, passivation

Abstract. Power AlGaN/GaN heterojunction field effect transistors on thinned sapphire substrates are demonstrated with improved power capability. A 16 mm-wide FET on a 50 μm-thick sapphire substrate exhibited a record output power of 15.9 W (on sapphire) with 9.0 dB linear gain, and 29.1 % power-added efficiency (PAE) at 34 V drain bias.

Introduction

AlGaN/GaN heterojunction field effect transistors are attracting much attention for microwave high-power applications because of their high breakdown voltage, high carrier carrying capability and high saturation velocity. Output power density values of 9.8W/mm for a 100 μm-wide device on a SiC substrate [1] and 4.6 W/mm for a 150 μm-wide device on a sapphire substrate [2] have been achieved. Total output power values of 22.9 W (CW) for a 4mm-wide hybrid-matched device [3], 51 W (pulsed) for 8 mm-wide MMIC on a SiC substrate [4], and 7.6 W (CW) for a 6 mm-wide device on a sapphire substrate [2] were reported. Relatively inferior power performance of a large periphery device on the sapphire substrate is due to the low thermal conductivity of sapphire.

In this paper, improved power performance of large periphery devices (16mm) on thinned sapphire substrates is reported.

Device Structure and Fabrication

An undoped AlGaN/GaN heterostructure was grown by metal organic chemical vapor deposition (MOCVD) on a 330 μm-thick (0001) sapphire substrate. Ti/Al ohmic electrodes were evaporated and alloyed at 650 °C for 30 sec. 0.9 μm-long Ni/Au gate electrodes were formed using optical lithography process. A standard Au-plated air-bridge process was used to fabricate multi-fingered FETs. After accomplishment of the front side process, the back side of the sapphire substrates were mechanically polished and the substrate thickness was reduced from 330 to 50 μm [5]. Ti/Pt/Au was evaporated on the mechanically thinned surface.

Device Performance and Discussion

Current-voltage characteristics for 50 and 330 μm thick FETs were measured. No degradation in DC characteristics was observed after the polishing process. 40 μm-wide device exhibited a maximum drain current of 450 mA/mm and maximum transconductance of 70 mS/mm. The threshold voltage was typically -6 V. The two-terminal gate-drain breakdown voltage was typically 100V.

Large-signal characteristics for 1mm-wide devices with 50 and 330 μm-thick were evaluated with an on-wafer load-pull system. Figure 1 shows drain bias dependence of saturated power at 1.95 GHz. The 50 μm-thick device exhibited a CW saturated output power of 1.4-1.5 W/mm with 21 dB linear gain and 40 % power-added efficiency at 40 V drain bias. This output power density is approximately 25 % higher than that of the 330μm-thick device (1.1-1.2 W/mm).

A 16 mm-wide device on the 50 μm-thick sapphire substrate was packaged into a ceramic carrier and measured with a load-pull system. Figure 2 shows the output power, the power-added efficiency and the gain as a function of the input power operated at Vd=34V. 15.9 W CW (1.0 W/mm)

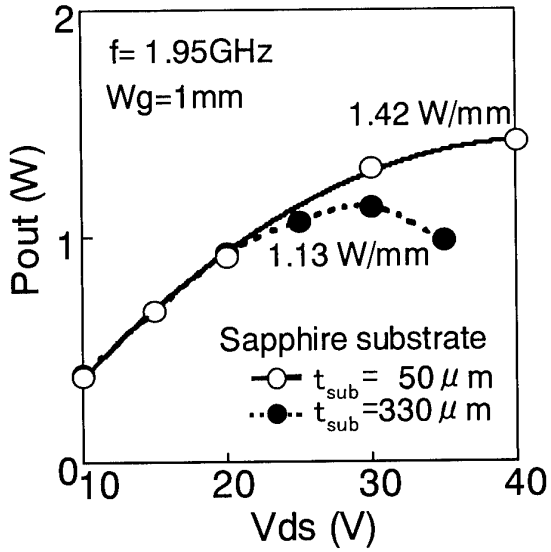


Fig. 1. Drain bias dependence of a saturated power at 1.95 GHz for 1mm-wide GaN FETs for t_{sub}=50 μm (open) and 330 μm (closed).

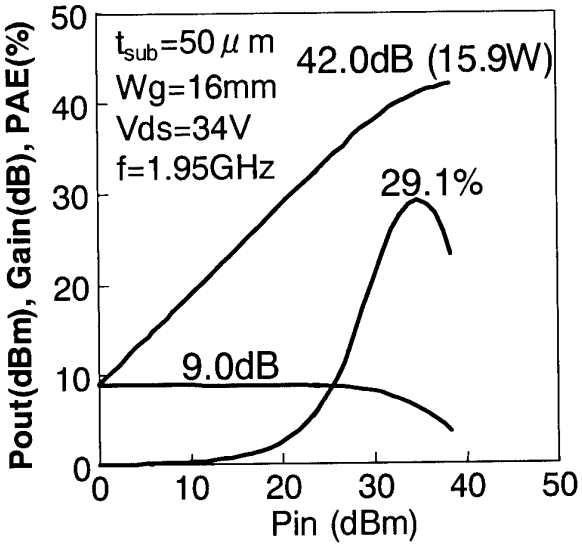


Fig.2. 1.95 GHz power sweep for 16 mm-wide FET (t_{sub}=50μm, Vds=34V).

saturated output power, 9.0 dB liner gain, and 29.1 % PAE were measured. To our best knowledge, 15.9 W output power is the highest achieved for AlGaN/GaN FETs on sapphire substrates.

Conclusions

Power AlGaN/GaN FETs on thinned sapphire substrates have been demonstrated with improved power capability. A 16 mm-wide FET on a 50 μm-thick sapphire substrate exhibited a record output power of 15.9 W (on sapphire) with 9.0 dB linear gain, and 29.1 % power-added efficiency (PAE) at 34 V drain bias.

Acknowledgments

This work was performed as a part of Regional Consortium Program supported by NEDO. The author would like to thank Y. Ando, Y. Okamoto, N. Hayama, K. Kasahara, T. Nakayama and M. Kuzuhara of NEC Corporation for preparing technical data and their useful discussions. The author would like to thank Prof. Y. Ohno for his valuable discussions at NEC. The author would also acknowledge M. Mizuta, T. Uji, and M. Ogawa with NEC Corporation for their continuing support.

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Broadband Push-Pull Microwave Power Amplifier Using AlGaN/GaN HEMTs on SiC

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AlGaN/GaN high electron mobility transistors (HEMTs) on high thermal conductivity SiC have yielded 6.9 W/mm at 10 GHz and 9.1 W/mm at 8.2 GHz in small periphery devices [1], [2]. To achieve this power density level in large periphery devices requires good management of thermal dissipation. Lower thermal dissipation can be achieved through the potentially higher power-added-efficiency (PAE) of Class B operation, relative to linear Class A operation. We demonstrate broadband Class B push-pull operation of GaN HEMTs, thereby taking advantage of the lower thermal dissipation while achieving linear operation and allowing higher power density in large-area devices.

The device fabrication, and DC and RF testing results have been reported previously [1]. The AlGaN/GaN HEMTs were grown on a semi-insulating SiC substrate using MOCVD. A 0.25 mm device with L_G=0.35 μm showed more than 800 mA/mm drain current, 220 mS/mm transconductance, and more than 60 V breakdown voltage. A 1.5 mm device (12 × 125 μm) provided 13.5 dB gain at 10 GHz (in a 50 Ω system), a f_T of 25 GHz and a f_{max} of 43 GHz, as shown in Fig. 1. A temperature dependent large signal model for these HEMTs has been developed for amplifier design.

Class B push-pull operation was achieved using two 1.5 mm GaN HEMTs and a new broadband balun at the input and output of the push-pull pair. This balun was implemented using three symmetric coupled lines and showed excellent loss, having less than 0.5 dB per balun over 5-11 GHz (3 dB bandwidth was 4-12 GHz) [3]. The fabricated amplifier is shown in Fig. 2. The balun and matching network, designed for broadband performance, were fabricated on a high thermal conductivity AlN substrate (ϵ_r = 8.5). Small-signal S-parameter measurements at V_{DS} = 15 and V_{GS}=-2.9 V resulted in a gain of 8 dB at 5 GHz for the amplifier, including input and output baluns, and a 3-dB bandwidth of 3-10 GHz, as shown in Fig. 3 . Figure 4 shows the continuous wave power sweep at 5 GHz, with V_{DS}=22 V and V_{GS} = -3.2 V. The output power was 2.5 W at about the 3-dB compression point, and the peak PAE was 14 %, being compromised for broadband operation.

To assess the linearity of the push-pull amplifier, single tone harmonic content and two-tone inter-modulation measurements were performed. Figure 5 shows the measured second and third harmonic levels of the push-pull amplifier biased at V_{DS}= 12 V and V_G = -3.2 V. The second harmonic levels measured at about the 1-dB gain compression point gradually decreased with frequency, reaching 40 dBc at the mid to high end of the band. Figure 6 shows the measured two-tone inter-modulation performance of the push-pull amplifier, with an input IP_3 of 32 dBm, indicating good linearity.

Acknowledgments: This work is supported by ONR under N00014-98-1-0371, N00014-98-1-0371 and N00014-99-C-0172 (John Zolper). The devices were fabricated by Cree Inc. under ONR contract N00014-99-C-0172 (John Zolper).

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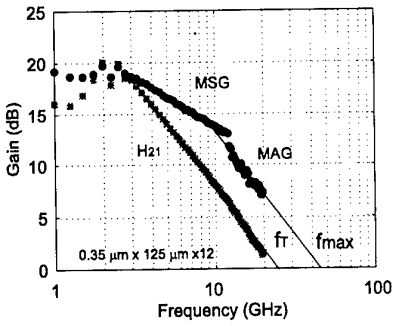


Fig. 1. Measured current gain ($|H_{21}|$) and power gain versus frequency of a 0.35 μm gate-length, 1.5 mm AlGaN/GaN HEMT on SiC

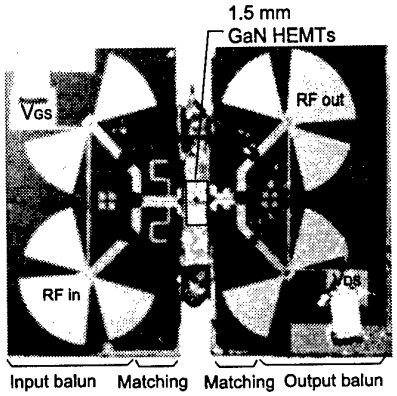


Fig. 2. Photograph of the fabricated amplifier.

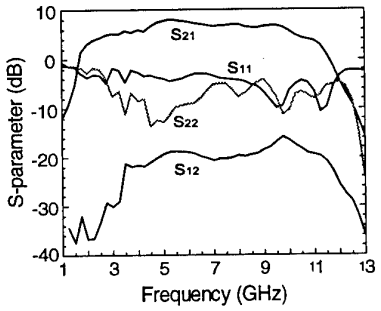


Fig. 3. Measured small-signal S-parameters for the push-pull amplifier (V_{DS}=15 V, V_{GS}=-2.9 V).

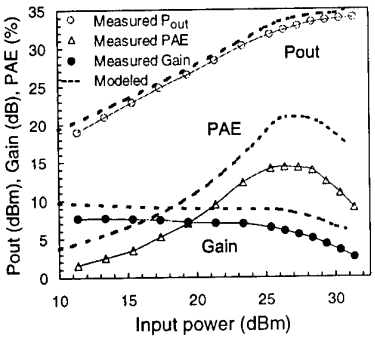


Fig. 4. Power output of Class B push-pull amplifier biased at V_{DS}=22 V, V_{GS}=-3.2 V. Simulated results are shown with a dotted line.

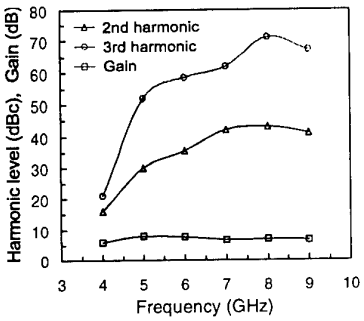


Fig. 5. Measured second and third harmonic levels of the push-pull amplifier versus frequency, biased at V_{DS}=12 V and V_G=-3.2 V. The harmonic levels were measured at about the 1-dB gain compression point.

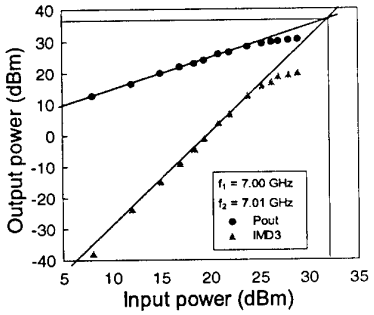


Fig. 6. Measured two-tone inter-modulation performance of the push-pull amplifier.

Gallium Nitride Power Device Design Tradeoffs

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Gallium nitride is of interest for high-voltage devices because of its wide-bandgap and high breakdown electric field. Many devices have been fabricated using the AlGaN/GaN system, including Schottky rectifiers, HBTs, and HEMTs. For high-voltage devices, it is important to understand the design tradeoffs for optimal device performance. This paper investigates these design tradeoffs for GaN power devices and compares with Silicon and 4H-SiC.

The ionization coefficients for 2H-GaN (hexagonal) were estimated using Fulop's approximation from theoretical ionization coefficients[1]. From the estimated ionization coefficient, the one-dimensional breakdown voltage and depletion width are calculated versus doping concentration (Figure 1). For unipolar devices the main device performance consideration is the specific on-resistance, with calculated results for vertical devices in 2H-GaN shown in Figure 2. For bipolar power devices, switching time, of the order of the carrier lifetime, is the key metric. The minimum carrier lifetime to achieve full conductivity modulation in the drift region of GaN devices versus breakdown is shown in Figure 3.

Termination of wide bandgap power devices must be carefully designed to prevent high fields in insulating layers on the device. Standard field-plates cannot be used without overly stressing the insulating materials. Termination structures must be used that do not expose insulating materials to high electric field, one example being epitaxial junction termination extension (JTE) which does not require implantation as shown in Figure 4.

For high-voltage HEMT structures, spontaneous and piezoelectric charge creates a high vertical electric field reducing the effective horizontal field that can be supported in lateral device structures such as the AlGaN/GaN HEMT. By estimating the polarization charge, the reduction in effective lateral critical field is calculated (Figure 5).

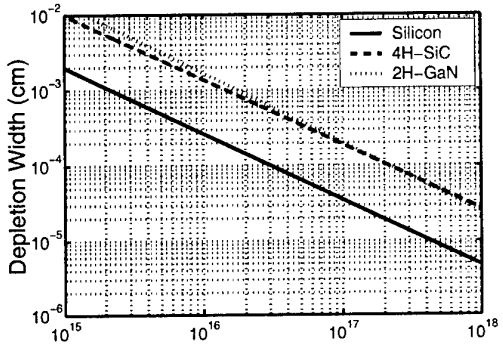
For power switching devices, a normally-off device is desirable. A normally-off HEMT has been fabricated[2] but suffers from a large gate-drain and gate-source parasitic resistance, because no 2DEG exists in these regions. Recessed-gate structures are proposed that provide normally-off operation with a reduction in the parasitic resistance by creation of a 2DEG in gate-drain and gate-source regions.

Power device design curves have been generated for 2H-GaN and compared with silicon and 4H-SiC. Unipolar and bipolar performance metrics have also been calculated. The polarization charge is shown to significantly reduce the effective lateral critical electric field for AlGaN/GaN HEMT devices.

*The authors thank N. Ramungul for providing the 4H-SiC model. K. Matocha is grateful for fellowship support from General Electric-Corporate Research and Development. The authors also acknowledge support from ONR (Grant #N00014-95-1-1302), DARPA (Contract #MDA972-98-C-0001), and the NSF Center for Power Electronics Systems (Award #EEC-0731677).

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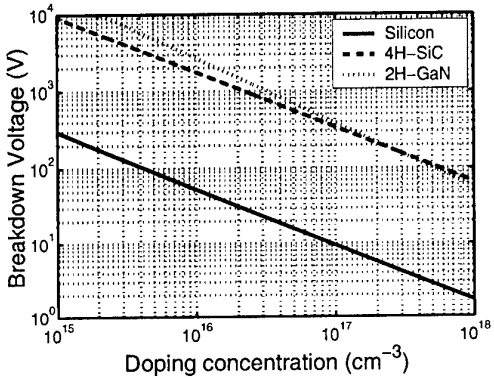


Figure 1: Parallel plate breakdown depletion width and breakdown voltage as a function of doping concentration for Si, 4H-SiC, and 2H-GaN.

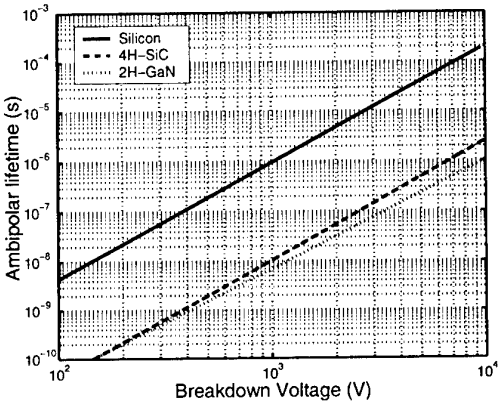


Figure 3: Ambipolar lifetime requirement for $W_d = 2L_a$, for Si, 4H-SiC, and 2H-GaN.

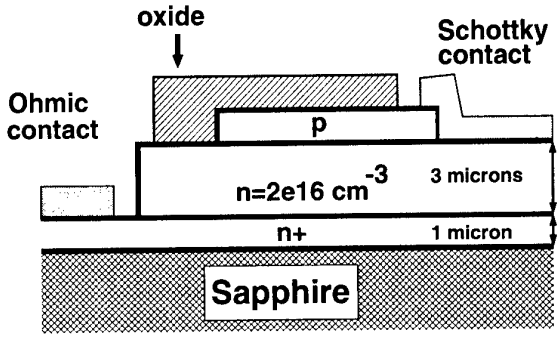


Figure 4: Epitaxial junction termination extension (epi-JTE) design for an 800 V GaN-Schottky rectifier.

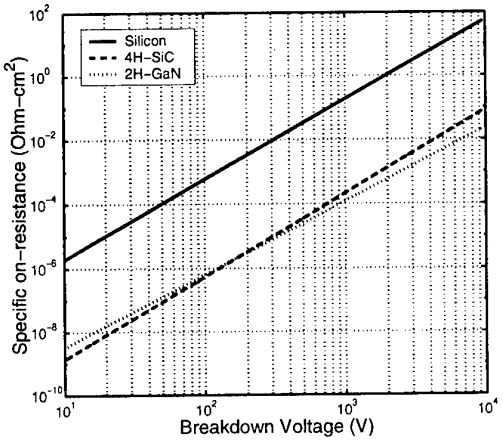


Figure 2: Specific on-resistance for Si, 4H-SiC, and 2H-GaN, using using data from Fig. 1.

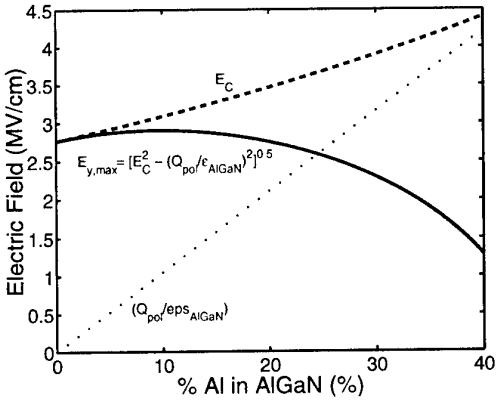


Figure 5: Critical electric field (E_C, dashed), polarization-induced field (Q_{pol}/ϵ_{AlGaN}, dotted), and effective lateral critical electric field ($E_{y,max}$, solid) as a function of Al percent in $Al_xGa_{1-x}N$.

Temperature dependence of DC characteristics of AlN/GaN Metal Insulator Semiconductor Field Effect Transistor

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AlGaN/GaN heterojunction field effect transistors (HJFETs) are promising for high temperature and high power microwave applications, and their high temperature operations at 300-450℃ [1-3] and at 800℃ [4] have been demonstrated. In these studies, the degradation of the DC characteristics at high temperature has been observed as follows: i) saturation drain current is suppressed, ii) transconductance decreases, iii) gate leakage current increases, and iv) pinch-off characteristic becomes vague.

Previously, we fabricated AlGaN/GaN HJFET with Al-content up to 100%, namely AlN/GaN metal insulator semiconductor FET (MISFET).[5] The MISFET has shown better DC characteristics at room temperature as compared with AlGaN/GaN HJFET using the conventional fabrication processing.

In this study, we investigated the DC characteristics of AlN/GaN MISFET when the device temperature was varied.

Figure 1 shows the schematic diagram of AlN/GaN MISFET. AlN/GaN heterojunction structure was grown on sapphire (0001) substrates by nitrogen plasma-assisted molecular beam epitaxy. This structure for device consists of 200-nm AlN buffer layer, 1.5-μm GaN layer, 15-nm n^+-GaN channel layer and 5-nm AlN barrier layer. After mesa isolation, in order to form Ohmic contact electrodes for source and drain, AlN barrier layer was removed by the wet chemical etching with hot phosphoric acid at 170℃ for 3min. Ti/Al/Pt/Au Ohmic contacts were formed onto the n^+-GaN channel layer. Ohmic contact resistivity ρ_c was $8.25\times10^{-6}\Omega$-cm^2. Schottky contact for the gate was formed by Al/Pt/Au e-beam evaporation. The gate length is 3 μm.

The DC characteristics of the sample were measured in vacuum chamber with pressure lower than 50 Torr. Semiconductor parameter analyzer (HP4156B) was used to measure the DC characteristics. The sample was set on the stage that consists of sapphire plate, Au seat, Ti plate, sapphire plate and the heater. During the DC measurement, temperature was monitored by thermo couple set under the heater.

The DC characteristics of the MISFET were measured from 25℃ to 500℃. Figure 2 shows the drain current-voltage characteristics of the MISFET at 25℃. The gate voltage V_{GS} has been changed from -5 to +3V by steps of 1V. The threshold voltage of the MISFET is –4V. When the drain voltage V_{DS} is high, the drain current I_D is saturated and becomes constant. Maximum transconductance g_{mmax} was 105mS/mm, and maximum drain current I_{Dmax} was 610mA/mm. When temperature increases, the saturation characteristic becomes vague, and I_D is not completely saturated. Also, sufficient pinch-off characteristic is not observed.

Figure 3 shows the temperature dependence of g_{mmax}. When temperature increases over 200℃, the value of g_{mmax} decreases. The value of g_{mmax} at 500℃ was 17mS/mm. However, after cooled down to 25℃, the MISFET showed to the initial characteristics before increasing temperature. Therefore, the Schottky contact metal for the gate electrode was not annealed by high temperature operation.

The detail will be discussed in the presentation.

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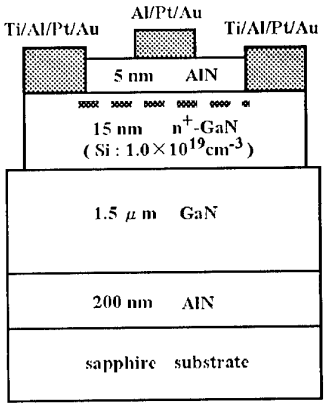


Fig. 1 : Schematic diagram of AlN/GaN MISFET.

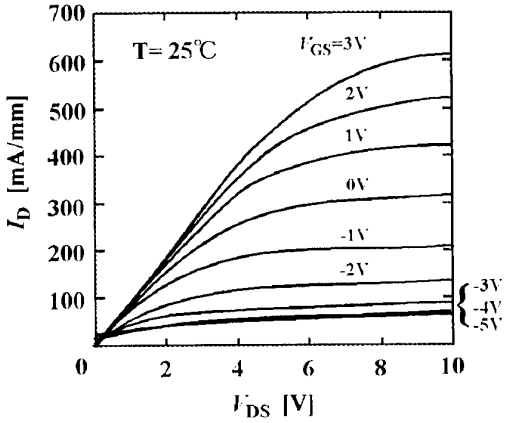


Fig. 2 : Drain current I_D as a function of drain-source voltage V_{DS} at 25℃

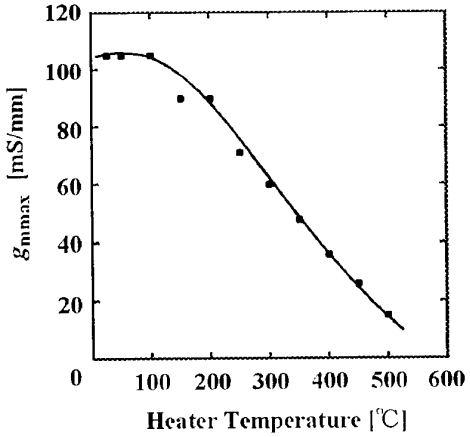


Fig. 3 : Temperature dependence of maximum transconductance.

High Performance AlGaN/GaN HEMTs with Recessed Gate

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High performance AlGaN/GaN high electron mobility transistor (HEMT) with recessed gate was successfully fabricated on sapphire substrate, as shown in Fig. 1. In order to realize high performance HEMT, it is very important not only to improve 2-dimensional electron gas (2DEG) but also to reduce the parasitic resistance. However, the increase of aluminum content in AlGaN to get high density 2DEG results in poor ohmic contact. Fig. 2 shows the comparison of contact resistances to GaN and AlGaN. Contact resistances were $8x10^{-6}\,\Omega cm^2$ in case of n-GaN ($1x10^{19}cm^{-3}$), and as high as $7x10^{-5}\,\Omega cm^2$ in case of n-AlGaN ($1x10^{18}cm^{3}$). In our recessed gate structure, ohmic contact with low resistivity can be formed on n-GaN with high electron density, which is formed on AlGaN layer with high aluminum content [1].

The substrate used here consists of a thin GaN nucleation layer, a 2.5-um-thick undoped GaN layer, a 10-nm-thick $Al_{0.26}Ga_{0.74}N$ spacer layer, a 20-nm-thick n-$Al_{0.26}Ga_{0.74}N$ ($1x10^{18}$ cm^{-3}) layer and a top 20nm-thick n^+-GaN ($1x10^{19}$ cm^{-3}) layer on sapphire substrate grown by MOCVD. Electron density and electron mobility of 2DEG were $1x10^{13}$ cm^{-2} and 736 cm^2 /Vs, respectively.

Drain and source ohmic contacts were formed with Ti (15nm)/ Al (250nm) and annealed at 550℃ for 1 min. Gate recess etching was done by reactive ion etching (RIE) in a Cl_2/H_2 plasma and gate metal (Ni/Au) was deposited on recessed area.

The HEMT with 0.5um gate length showed excellent current saturation properties, as shown in Fig.3. The maximum trans-conductance(gm) was as high as 327 mS/mm. Measured current gain cutoff frequency (fT) was as high as 32.3GHz and a maximum frequency of oscillation (fmax) was 39GHz, as shown in Fig.4. Source resistance(Rs) between source and gate were also measured.

These characteristics were compared with that of non-recessed 0.75um gate HEMT which has the same hetero structure, as shown in Table 1. Rs of recessed gate HEMT was smaller than one third of that of non-recessed gate HEMT. This will be the reason why the trans-conductance of recessed gate HEMT is three times lager than that of non-recessed gate HEMT. The gm x gate-length product and fT x gate-length product were also compared. In the recessed gate HEMT, these products were greatly improved and also nearly equal to that of the highest achieved for GaN-HEMT[2][3].

To evaluate effective electron velocity in the channel and intrinsic fT, we measured the relation of τ ($=1/2\,\pi\,fT$) and reverse of drain current (1/Id), as shown in Fig 5. The interceptof, τ_0, of τ and 1/Id relation means the effective transit time of electron flowing beneath the channel [3]. Effective electron velocity and intrinsic fT calculated from τ_0 were as high as 1.56×10^7 cm/sec and 49.7GHz, respectively. Effective electron velocity obtained here is the highest value reported to date for GaN-HEMT.

In conclusion, it can be said that AlGaN/GaN HEMT with recessed gate is a very promising device for high power and high frequency applications.

This work was performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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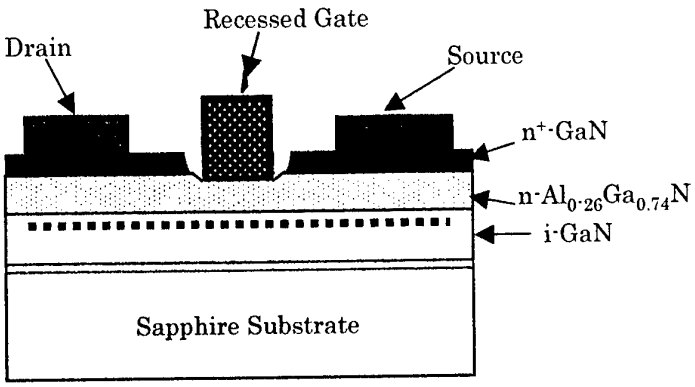


Fig. 1 AlGaN/GaN HEMTs with Recessed Gate.

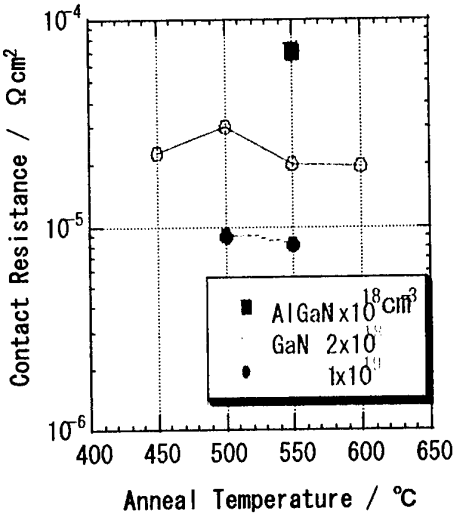


Fig. 2 Anneal temperature dependence of contact resistance.

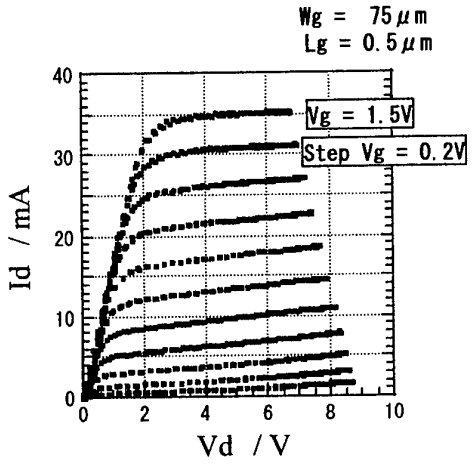


Fig. 3 DC I V characteristics of AlGaN/GaN HEMT.

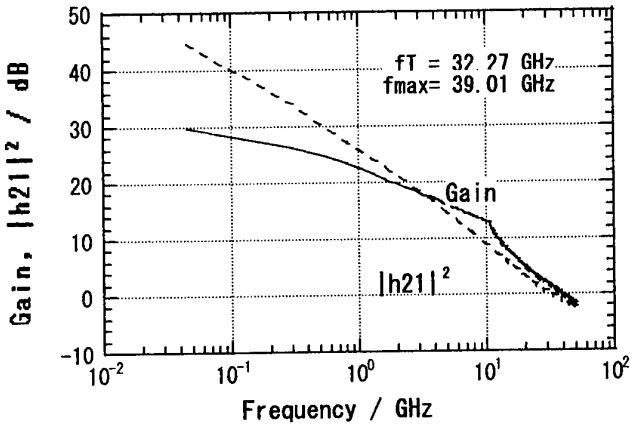


Fig. 4 Current Gain $|h_{21}|^2$ and MSG/MAG(Gain) of HEMT.

Gate structure	Non-Recessed	Recessed (This work)
Gate Length (μm)	0.75	0.5
Rs (Ωmm)	7.2	2.1
gm (mS/mm)	110	327
fT (GHz)	6.0	32.3
fmax (GHz)	25.5	39.0
gm x Lg(μm-mS/mm)	83	164
fT x Lg(μm-GHz)	4.5	16.2

Table 1 Comparison of characteristics between Non-recessed and recessed gate HEMT.

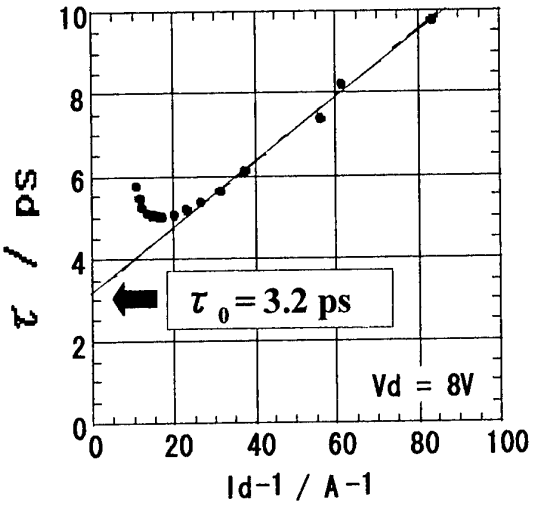


Fig. 5 Relation of $\tau = 1/2\pi fT$ vs 1/Id.

GaN Substrates Grown by Hydride - Metal Organic Vapor Phase Epitaxy (H-MOVPE) on lattice-matched oxide and silicon substrates

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The III-V nitrides - wide band-gap semiconductors have demonstrated considerable promise for various optoelectronic, high-temperature and high-power device applications. Since a suitable commercial substrate matched to GaN in both lattice parameter and thermal expansion is not available, GaN films grown on sapphire typically contain a dislocation density on the order of ~ 10^{10} cm^{-2}. This leads to the formation of threading defects and residual strains which may effect both the optical and electrical properties of devices. Epitaxially laterally overgrown (ELOG) GaN on sapphire has been used to reduce the number of threading dislocation in the GaN layer, and laser diodes (LDs) with estimated lifetimes of more than 10,000 hours have been developed. An obvious solution to minimizing defect generation at the interface is to use a GaN substrate.

Bulk GaN or thick GaN films would be of highest interest as a base structure for the device fabrication. At present, GaN bulk single crystal substrates can be grown by high-pressure synthesis, by chloride-hydride vapor phase epitaxy, the sublimation sandwich technique and liquid-phase epitaxy on sapphire or SiC substrates with subsequent substrate removal by reactive ion etching, laser ablation, or polishing.

In the present work we report on successful growth of single crystal GaN substrates by combining the rapid growth rates afforded by HVPE with the nearly lattice-matched crystal structure of $LiGaO_2$ and $LiAlO_2$ substrates. A self-separation process was developed that leaves free-standing flat single crystal GaN without the need for mechanical or chemical treatment. No cracks or residual strain were observed in the GaN wafers. It was determined that surface nitriding and cooling processes were critical in film-substrate self-separation.

A novel chemistry that uses a group III MO source reacting with injected HCl along with NH_3 for the deposition of GaN was explored. This technique can alternate between MOVPE and HVPE growth chemistries, combining the advantages of both. The advantages of this approach include the possibility of performing MOVPE or HVPE in the same reactor, high growth rates, rapid reactant switching, potentially lower background impurities, in-situ etching, elimination of HVPE source problems, and improvement in NH_3 cracking.

Seed GaN crystals were grown by MOVPE on (001) $LiGaO_2$ and (100) $LiAlO_2$ to protect the substrate from the HCl attack. The GaN layers were grown on nitrided substrate surfaces. The MOVPE GaN seed layer thickness was 0.2 to 0.3 μm. A thick GaN layer was next grown by HVPE. The estimated growth rate was 50 to 70 μm/hr. Typical HVPE GaN thickness ranged from 100 to 300 μm. A thin (0.1 to 0.2 μm) MOVPE GaN layer was grown to improve the surface morphology of the layer. The substrate nitridation and subsequent cooling processes were found to be critical for film-substrate self-separation and caused the GaN film to "lift off". Therefore substrate removal by wet chemical etching was not needed.

High quality GaN layers were grown on (111) Si substrates using AlN buffer layer by H-MOVPE technique.

Different techniques were used to assess the substrate and film quality. The surface morphology was study by AFM and SEM, while the structural quality was analyzed by XRD and TEM. The chemical composition was investigated by AES, ESCA and SIMS. Micro Raman spectroscopy was applied for film and substrate characterization as well.

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FrB1 Epitaxial Growth 3



Simulation of the large-area growth of homoepitaxial 4H-SiC by chemical vapor deposition

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1. INTRODUCTION

The SiC-base electronics applications have made tremendous progress primarily because of the commercial availability of SiC substrates of ever increasing diameter and quality. This triggers higher demands on the epitaxial process. The growth of thick epitaxial layers with low defect density and the control of the doping is an essential technique and the next step for the fabrication of devices. Our recent experimental and modelling work was recently applied to an horizontal hot-wall reactor commercially available from the Epigress company (http://www.epigress.se). Hydrogen is typically employed as the carrier gas along with silane and propane as precursor gases. Atmospheric and reduced pressures (10-100 kPa), temperature higher than 1700 K and C/Si ratios from 1 to 15 in the gas phase can be used. The quality, the growth rate and the doping level over 2" wafers are found to depend on the C/Si ratio in the gas phase supplied onto the growth surface, which suggests the importance of the intricate mixture of transport phenomena (heat and mass transfer) and reactivity.

2. SIMULATION

Thermodynamic and kinetic modelling were used to evaluate the qualitative influence of temperature, pressure and species reactivity on the deposition features. This approach is static (0D) at fixed pressure and temperature and it was difficult to give engineering conclusions. After the comparison of experiments with simulation trends in the 1700-2000 K temperature range and 25-100 kPa pressure range and many returns with simplified 2D simulations, we have decided to use a reduced and slightly modified version of the most complete and reliable heterogeneous and homogeneous kinetic database published. This reduced database includes 12 gaseous species (H_2, H, SiH_4, SiH_2, Si_2H_6, Si, C_3H_8, CH_3, C_2H_5, C_2H_6, C_2H_2, C_2H_4) and 5 surface species (Si_s, C_s, SiH_2_s, HC_s and HSi_s). The electromagnetic simulation has been performed on the hot-wall reactor in static conditions using Flux3D software package. It clearly shows that the rectangular shape of the susceptor associated with the cylindrical shape of the insulation leads to a 3D situation. The joule losses are higher in the lateral parts and consequently, the temperature is higher. A small part of the power is dissipated in the foam due to the striations. One of the drawbacks of this reactor is that the temperature along the susceptor is highly non-uniform. It is then difficult to process more than one wafer of 35-50 mm. The uniformity of the temperature distribution along the central 2/3 part of the susceptor can be slightly improved by increasing the thickness of the graphite (from 35 to 50 mm) and more by changing the position and the design of the coil. The next step is to combine iteratively this 3D simulation with heat and mass transfer.

The computation of the combined approach has been made for standard conditions using Cfdace software package and a series of user subroutines : P=25 kPa, T_{max}=1850 K, D_{H2}=80 l.min^{-1}, a C/Si ratio of 1 and a high dilution for precursors (from 1 to 6 10^{-4} in mole). The results show, for instance, that (i) gravity leads to a deposition on the top of the reactor at the exit of the susceptor (figure 1), (ii) the cold finger at the entrance of the susceptor contributes to non-uniform distributions of temperature (figure 2), (iii) deposition rate results from an intricate mixture of temperature and concentrations fields (figure 3) and (iii) that the main contributing gaseous species are SiH_2, Si, C_2H_2, C_2H_4 and CH_4. The model predict a rather good uniformity for the deposition rate, less than 10 %, for a wafer of 50 mm placed in the high temperature region (50 to 70 % of the susceptor length).

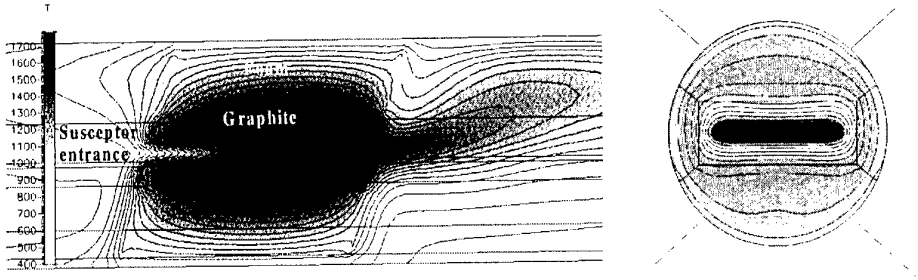


Figure 1. Influence of the gravity and of the narrow entrance of the susceptor on the temperature field for both an horizontal section (Z-cut at left) and a vertical section (X-cut at right) at the exit of the susceptor (P=25 kPa, T_{max}=1850 K, D_{H2}=80 l.min^{-1}, C/Si ratio =1 and 2 10^{-4} mole of SiH_4).

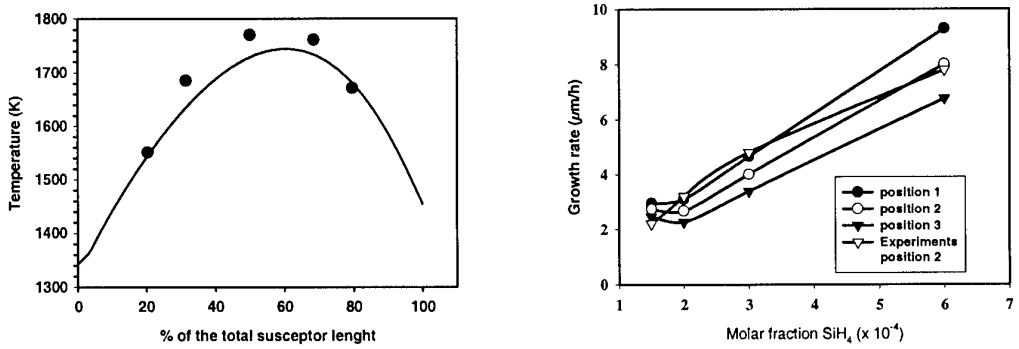


Figure 2. Comparison between the computed (—) and measured (•) temperature distribution along the centerline of the susceptor.

Figure 3. Evolution of the computed growth rate versus the molar fraction of silane (C/Si=1, temperature of figure 2) for 3 positions along the centerline of the wafer : position 1 is the leading edge, position 2 the center and position 3 the trailing edge of a single wafer located in the high temperature region of the susceptor.

In conclusion, it seems difficult to find a set of experimental parameters to process numerous wafers with a sufficient growth rate and uniformity in the standard version of this reactor. However, for a single wafer by run, high quality 4H-SiC films of 10 μm and devices have been processed. The residual doping is low (10^{14} cm^{-3}). This allows to process N-doped SiC layer when using small amount of nitrogen. We have found a non-linear dependence of the doping profile with the inverse of the initial propane flux and a strong dependence on the temperature. Hence, the production of thick 4H-SiC with low residual doping can be achieved with the hot-wall reactor used in this study. But, to reach a good doping uniformity improvements on the design of the deposition area are still needed.

Predicting growth rates of SiC epitaxial layers grown by hot-wall chemical vapor deposition

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An important technology for growth of SiC epitaxial layers is the chemical vapor deposition (CVD) technique, which has been extensively studied in recent years, both experimentally [1, 2] and theoretically [3, 4, 5]. The growth of device quality epitaxial layers, such as MESFET structures, requires precise control of the thickness and doping uniformity and of the morphological quality. Optimizing and improving the CVD process is often expensive and time consuming. Simulations can be used to gain more understanding of the process, making development faster and less expensive. Modeling of the growth rate and morphology of epitaxial layers is an important step towards process optimization.
In order to obtain an accurate model for the growth, the chemistry involved has to be correctly modeled. Some models of gas phase and surface chemistry present in SiC CVD have been proposed [3, 5], however these models do not include the formation of organo-silicon species, which are believed to play an important role in the growth process [6]. Also, the proposed models have only predicted deposition rates and not deposit composition. The growth is either limited by the amount of carbon species or by the amount of silicon species available in the gas phase immediately above the growth surface. Thus, a precise model of the gas phase chemistry is essential to obtain accurate growth rate predictions. This work will use a new model, including some organo-silicon species, to simulate growth rates along the entire susceptor. To accurately predict the growth rate it is also crucial to know the exact temperature distribution inside the susceptor. Therefore the temperature inside the susceptor was both simulated three-dimensionally and measured by an in-situ method.

For the epitaxial growth a horizontal hot-wall type CVD reactor [1] was used. It consists of a hollow graphite susceptor surrounded by insulation inside an air cooled quartz tube. The graphite is inductively heated by a copper coil. Hydrogen (H_2) is used as carrier gas, silane (SiH_4) and propane (C_3H_8) as precursors. Growth was made on 10 mm wide stripes of 4H-SiC 8° off axis substrates, which were placed along the gas flow direction covering the whole susceptor length. Normal process parameters were C/Si = 3.5, T = 1600°C, H_2 gas flow = 13 slm, SiH_4 flow = 0.9 sccm and C_3H_8 flow = 1.05 sccm and atmospheric pressure. Different cases were studied, changing various process parameters such as pressure and carrier gas flow rate. The thickness of the deposited layers was measured by FTIR and the morphology was studied using optical microscopy. The doping was measured by CV and controlled with photoluminescence. The composition of the deposited material was studied using XPS in order to obtain a quantitative measurement of the precursor losses before the area of "good" growth. The results show an alternating carbon rich and silicon rich deposit at the entrance of the susceptor. The relative amount of silicon and carbon in the deposit on the first 20 mm of the susceptor for typical growth parameters is shown in Fig. 1. Different growth models are assigned to the boundaries of the simulation domain according to the results gained by XPS.
The carbon and silicon rich deposits are also confirmed by studies of the morphology by optical microscope, where certain types of surface defects can be attributed to carbon rich or

silicon rich growth. At the entrance of the susceptor there is a region of polycrystalline growth. Downstream from this region large triangular defects can be seen before the deposition turns into a completely mirror like surface, i.e. the useable growth area. Further downstream, towards the back of the susceptor, large triangular defects are again seen. When reducing the pressure, the polycrystalline region extends further inside the susceptor, but the transition to a completely mirror like surface does not show any triangular defects. The triangular defects on the surface are believed to originate from silicon rich deposition.

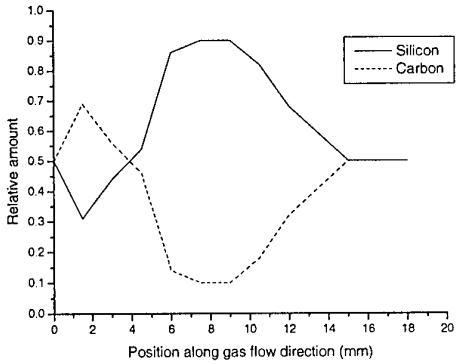


Fig. 1 The relative amount of silicon and carbon in the deposit on the first 20 mm of the susceptor (at 1000 mbar), as measured by XPS.

A slightly higher growth rate (about 10%) is observed for the reduced pressure growth compared to the growth at atmospheric pressure. This is also predicted by the simulations. The predicted and measured growth rates are shown in Fig. 2. In the figure a scaling factor has been used to compensate for the 2D effects caused by the axisymmetric approach used in the 2D simulations. Simulations were carried out for both 2D and 3D.

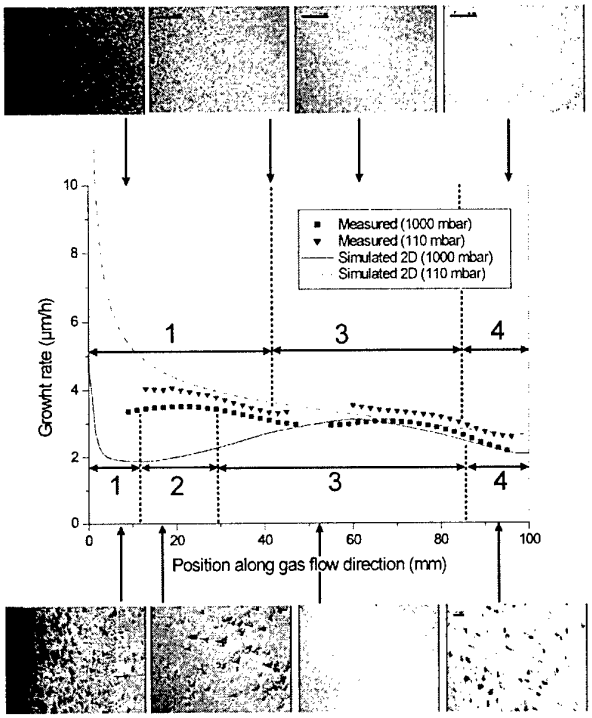


Fig. 2 Measured and predicted growth rates along the entire susceptor for two different pressures. The zones are indicating different types of growth; 1 – polycrystalline growth, 2 – triangular defects, 3 – usable growth area, 4 – defective surface.

Preliminary results from 3D simulations show good agreement with measured values.

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Characteristics of boron in 4H-SiC layers produced by high-temperature techniques

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Boron is a persistent residual impurity in SiC, especially when the growth process is performed at high (1600 – 1850°C) temperatures, which are typical in the sublimation epitaxy [1] and in the CVD epitaxy process in a vertical hot-wall ("chimney") reactor [2]. Both techniques are candidates for the growth of thick (> 30 μm) SiC layers for device applications like high-power switching, provided the demand on the material purity is satisfied. From this point of view investigations on different characteristics of B in 4H-SiC layers are important in order to establish growth parameters for controllable boron incorporation.

Boron, along with nitrogen and aluminum, can be present in as-grown sublimation epitaxy layers. The background impurities in the epilayers are unintentionally introduced from the growth environment, mainly the polycrystalline SiC source material and graphite. Boron incorporation (from $5x10^{15}$ cm^{-3} to $3x10^{17}$ cm^{-3}) in the layers can be affected by applying different growth temperatures that also change the growth rate (from 2 μm/h to 160 μm/h). The spectra in Fig. 1(a) present the cathodoluminescence (CL) signature of two layers with the same Al/N ratio and boron concentration of $(2 - 3)x10^{16}$ cm^{-3}. Formation of a strong green luminescence (GL) band at ~ 505 nm characterizes the layer produced at higher growth rate. The GL is believed to originate from deep boron centers [3].

Under CL excitation efficient GL (Fig. 1b) is recorded in the "chimney" grown epilayers characterized with B concentration below the SIMS detection limit (i.e. less than $5x10^{14}$ cm^{-3}) with a residual N doping in the range of mid 10^{13} cm^{-3}. The layers are obtained at growth rates of 15 – 25 μm/h, which is an order of magnitude higher than in the conventional CVD where no traces of GL are observed in the low doped layers. The finding that B atoms can cause strong GL even at small concentrations, provided B is introduced at higher growth rates, also holds for B residual doping in a "chimney" reactor.

We observe that the total boron concentration in the sublimation epitaxy layers and the intensity of GL related to the deep B centers increases, while the contribution from the B dopant to the net acceptor concentration, as measured by the mercury-probe CV technique, diminishes (Fig. 1c). The layers are fabricated at increasing growth rate. It has been argued that at high growth rates the Si/C ratio in the lattice increases especially if the growth rate is comparable or exceeds the rate of silicon and carbon self-diffusion [4]. As a consequence the concentration of C vacancies increases and thus gives rise to enhanced probability of forming the defect complexes considered to assist the deep B center formation, i.e. B_{Si}-V_C [5], B_{Si}-Si_C [6] or B_C [7]. Apparently, variations in the growth rate can cause redistribution between shallow and deep B-related centers, which cannot contribute to the acceptor concentration as measured by CV.

The results are further discussed in relation with the measurements done on "chimney" grown epilayers produced at growth rate of 20 μm/h and with varying the C/Si ratio.

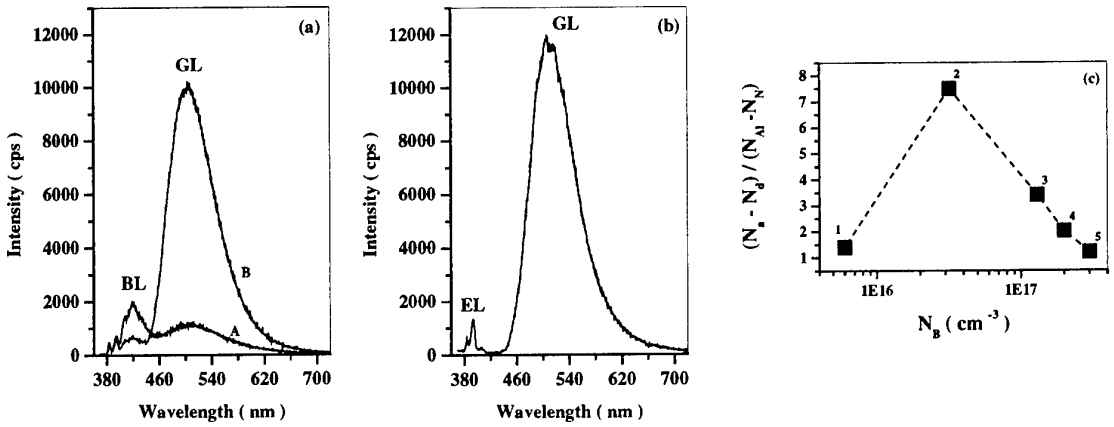


Fig. 1. *(**a**) CL spectra at 4.6 K of 4H-SiC sublimation epilayers produced at growth rate of 22 μm/h (A) and 160 μm/h (B). BL denotes blue luminescence at ~ 420 nm due to N-Al DAP recombination; (**b**) CL spectrum of a 4H-SiC "chimney" epilayer. EL denotes 4H-SiC edge luminescence starting near 380 nm; (**c**) The ratio of net acceptor concentration ($N_a - N_d$) to concentration difference ($N_{Al} - N_N$) vs. boron concentration (N_B) for the sublimation epilayers produced at increasing growth rate: 2 μm/h (1), 16 μm/h (2), 87 μm/h (3), 108 μm/h (4), 162 μm/h (5).*

The investigation indicates two acceptor levels associated with the presence of B in the 4H-SiC epilayers fabricated by two high-temperature techniques. A range of growth parameters to minimize boron incorporation in the layers and to control the preferred occupation of boron in the shallow or deep level is suggested.

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Impact of the initial surface conditions on the defect appearance in 4H-SiC epilayers

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Progress in SiC-based technology has been made in many processes, e.g. 4H-SiC growth, ion implantation, metal contacts, etc. However control of the crystal quality during bulk and epitaxial growth is far from the desired. Control during epitaxial growth can be made more precise but inherence of threading defects from the substrate can not be avoided. Besides the threading defects emerging from the substrates (e.g. micropipes and dislocations), the epitaxial layers may develop specific defects, generally viewed as structural and morphological. Common defects in SiC epitaxy are stacking faults. They may act both as nucleation sites for polytype inclusions [1] and for degradation centres of device performance [2,3]. The surface morphology of the epitaxial layers is a critical characteristic since morphological defects may eventually hinder device processing [4]. While there is a growing body of experimental evidence pointing to a variety of harmful defects in SiC epitaxial layers, the origin and the nature of the defects are not completely understood and beg explanation. Finding the reasons for defect occurrence and eliminating them is a key issue in the SiC growth technology.

With this study we attempt an insight into extended defects generation in 4H-SiC epitaxial layers in respect to nucleation on different surfaces that may occur under two different conditions. One series of samples comprises as-grown surfaces obtained by liquid phase treatment of commercial substrates, made to reduce the micropipes. The micropipe healing was performed at TDI, Inc. [5]. A second series of samples was prepared by temperature treatment at 1700-2000°C in conditions resembling the initial phase of SiC growth via sublimation.

We have used SEM, electron emission, STM and SWBXT to characterise the initial surfaces and the layers grown on them by sublimation epitaxy. With increasing roughness of the nucleation surface, i.e. step width and step height, from 500nm, respectively 20nm, to 4μm, respectively 600nm, different types of defects are generated at the interface and are developed in the subsequently grown layers. With further increase of the surface roughness conditions for polytype switching have occurred.

Fig. 1(a,b) illustrates two distinguished cases. In the first case (a) stacking faults with accompanying partial dislocations, along with threading dislocations with $\mathbf{b} = 1/3\langle 11\bar{2}0\rangle$ are observed, while in the second case (b) misfit dislocations and dislocations in three (120°) symmetric directions are imaged. These results indicate that when the growth is disturbed, the easiest grown-in defect to be formed at the substrate/layer interface are partial dislocations and stacking faults, which is consistent with the low energy of formation of this defect. Edge dislocations due to a large "mismatch" were formed when the irregularity of starting surface exceeded some critical value. It is interesting to note that also interface related micropipes have

been observed to appear in the epitaxial layers, though this is not expected in the step flow mechanism. The result was obtained by KOH etching of the substrate and of the layer and the patterns characteristic of micropipes were compared.

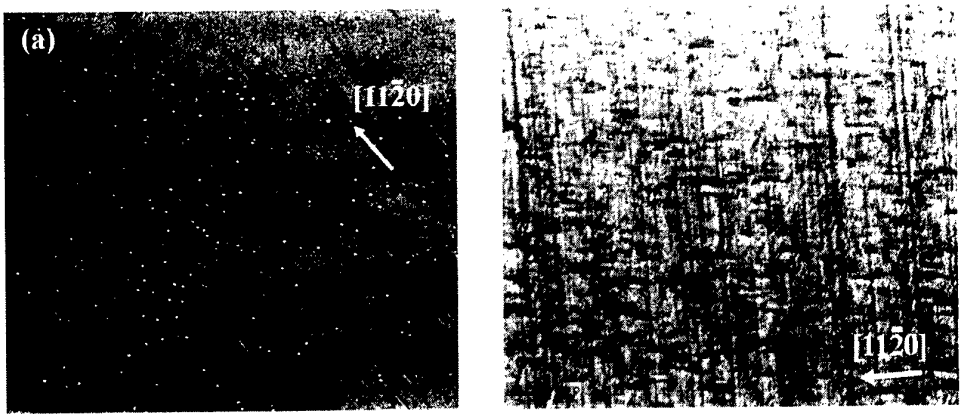


Fig. 1. Synchrotron white beam X-ray topography images of (a) stacking faults (triangular features) and (b) misfit dislocations (fine lines), in epitaxial layers grown on initial surfaces with increasing roughness.

The surfaces after the temperature treatment exhibit graphite coverage with thickness reaching 75 Å depending on the face polarity, as obtained by photo emission measurements. In contrary to the results presented in Ref. [6], this graphite is uniformly covering the substrate surface and is well ordered as proved by the LEED patterns. The STM images indicate step-wise morphology governed by the substrate off-cut. Growth on such surfaces was initiated and the results will be further discussed concerning the impact of the graphite film on the structural evolution during sublimation growth of 4H material. We have indications that the graphite film can be preserved during growth and thus to act as a two-dimensional defect in the grown layer.
Based on the experimental findings a thorough analysis of defect appearance in 4H-SiC layers will be made and a model for critical nucleation conditions of single 4H polytype will be presented.

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HIGHLY UNIFORM EPITAXIAL SIC-LAYERS GROWN IN A HOT WALL CVD REACTOR WITH MECHANICAL ROTATION

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Despite the improvements made over the past years in material growth of SiC, the epitaxial growth of highly uniform and pure layers is still an issue of development for the further commercialization of electronic devices made from SiC. The development focuses on high growth rates, purity, uniformity of layer thickness and doping concentration, and low crystal defect density. The hot wall CVD-reactor has proven to be a system for achieving high growth rates and pure layers. The thickness and doping uniformity is depending on the homogeneity of temperature and gas flow. Rotating the wafer during growth evens out possible temperature or gas flow inhomogeneities and more uniform layers can be grown.
We have developed a hot wall reactor with mechanical rotation based on the VP508 system, commercially available from Epigress, and the growth process for achieving SiC layers highly uniform in thickness and doping.

Figure 1 shows schematically the reactor design and the downstream side of the reactor in operation. The substrate lays on a satellite, which consists of tantalum carbide (TaC) coated graphite and is designed for 2" wafers. The satellite is loaded from the downstream side and placed on top of a graphite tube. The graphite tube can be moved vertical and rotates motor driven. The rotation speed is around 1 rpm.
The heating control in the reactor is done by a pyrometer, measuring the temperature above the satellite at the inclined ceiling of the susceptor (temperature maximum). The substrate temperature was calibrated by melting silicon on a SiC wafer. Silicon melted at a control temperature of 1520°C, indicating that the satellite is mainly heated by the radiation from the surrounding susceptor and not actively by the RF-field. Therefore, the susceptor has to be heated up to a much higher temperature to get the requested substrate temperature for achieving good quality SiC layers.

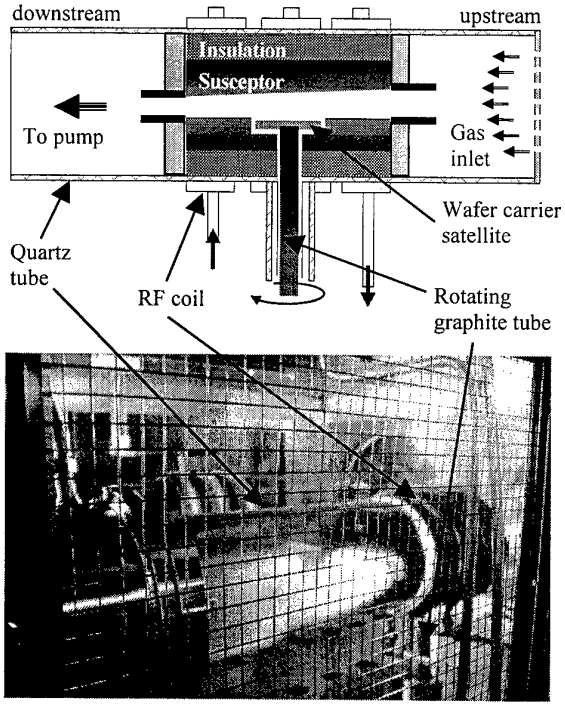


Fig. 1 Schematic drawing of the hot wall CVD reactor with mechanical rotation and the downstream side of the reactor in operation.

In our standard hot wall reactor the growth temperature is set to 1600°C, resulting in good layer morphology and low defect density. The substrate temperature is 50 to 100°C lower in the reactor with rotation. The lower substrate temperature does not affect the layer quality

in a negative way, which is probably due to that the supplied gases and the substrate surface are at a similar or higher temperature than in the standard reactor cell.
The epitaxial growth was done with a conventional precursor system of silane and propane. Nitrogen gas was used for n-type doping and trimethylaluminum (TMA) for p-type doping. The susceptor temperature was between 1650 to 1700°C, which corresponds to a substrate temperature of 1500 to 1550°C using the TaC-coated satellite. The total pressure in the reactor was set to 250 mbar. As carrier gas, hydrogen purified in a platinum cell as well as a mixture of purified hydrogen and argon was applied. Argon has a lower cooling efficiency than hydrogen and homogenizes therefore the temperature over the wafer area.

The thickness and doping characterization of the layers grown in the reactor with rotation was done mainly by capacitance voltage (CV) measurements and secondary ion mass spectrometry (SIMS). Figure 2 shows the results from CV-measurements on nitrogen doped epitaxial layers. The thickness uniformity is excellent with a standard deviation over mean value of 1% and a maximum variation over mean value of 4%, when excluding 5 mm at the wafer edge. However, the uniformity for both p- and n-doped layers grown with carrier gas hydrogen was not good. In n-doping we observed u-shape profiles with a concentration variation by a factor of 2 to 4. P-type doping showed camel like concentration distributions with a variation of about 25%. The reason for the large concentration variation is most likely related to the lower substrate temperature in combination with a cooling effect by incoming gases or the use of the TaC coated satellite.

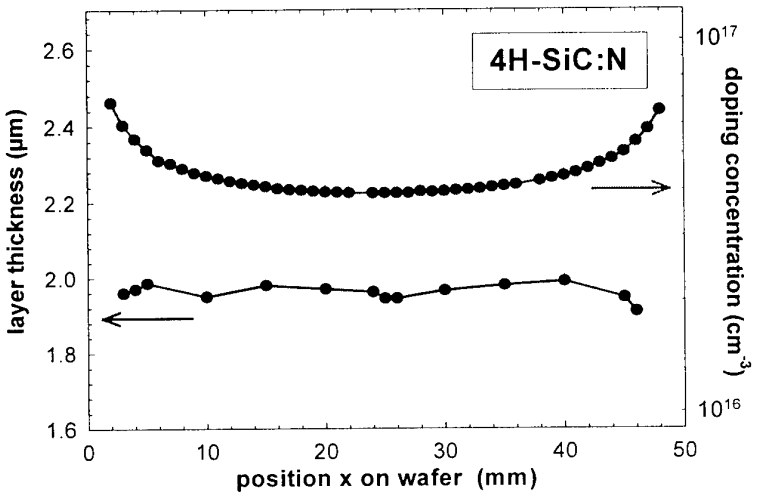


Fig. 2 Thickness and doping uniformity of n-type SiC layers grown in a hot wall CVD reactor with mechanical rotation.

From our standard hot wall reactor we have the experience that adding argon to the carrier gas gives a better layer uniformity. The same effect can be observed in the reactor with mechanical rotation. Adding around 15% argon to the hydrogen carrier gas by keeping the total carrier gas flow constant results in the doping distribution shown in figure 2. Excluding 5 mm at the edges of the wafer the concentration varies by 6% (standard deviation/mean) and 10% (maximum variation/mean).
In addition to the good thickness and doping uniformity, we observed in the reactor cell with rotation an increased growth rate in comparison to our standard hot wall reactor. Using the same precursor flows the growth rate is a factor of 1.5 to 2 higher, which is due to the lower substrate temperature in the reactor cell with rotation.

We have shown epitaxial growth of SiC with excellent thickness and doping uniformity using a hot wall reactor with mechanical rotation and a carrier gas mixture of 15% argon in hydrogen. The high uniformity of the layers gives rise to improved yield of devices, where the layer thickness and doping are critical issues.

Fast Epitaxial Growth of 4H-SiC by Chimney-type Hot-wall CVD

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Owing to recent significant progress of SiC wafer quality and epitaxial growth technology, high-performance SiC devices have been reported. Although SiC device structures have been formed by CVD, a typical growth rate is relatively low, 2∼6 μm/h [1]. Vertical hot-wall CVD has merits such as high-temperature growth. High-temperature growth suggests a great potential of high-purity thick epitaxial growth with a high growth rate. One challenge in fast epitaxial growth so far is a relatively high concentration of deep levels, called the D_1 center, found as the L_1 center in the PL measurement [2, 3]. In this work, the authors realized high-speed epitaxial growth and found that the L_1 peak and the Z_1 center could be reduced in a growth under a C-rich condition.

Epitaxial growth was performed on off-axis 4H-SiC(0001) by vertical hot-wall chimney-type CVD in a SiH_4-C_3H_8-H_2 system at 1700°C. The H_2 flow rate and the reactor pressure was 3 slm and 100 Torr, respectively. All of source gases and carrier gas were introduced from the bottom end of reactor. The C/Si ratios were varied in the range from 0.6 to 0.75 with a fixed SiH_4 flow rate of 16.3 sccm.

The high growth rates of 22μm/h and 25 μm/h were attained with a mirror-like surface for the epilayers grown with C/Si=0.6 and 0.7, respectively. The Nomarski photographs of elilayers grown for 1 h showed excellent surface morphology without wavy pits and triangle defects. A relatively smooth surface without step bunching was observed by atomic force microscopy and a small surface roughness of 0.20∼0.25 nm was obtained (Table 1). Figure 1 represents the surface morphology and the height profile of epilayer grown with C/Si=0.7. The X-ray diffraction analysis revealed a FWHM of 14 arcsec, suggesting high quality of the epilayer. From C-V measurement, the net donor concentration was determined to be as low as 4×10^{14} cm^{-3} with C/Si=0.6 and 2×10^{14} cm^{-3} with C/Si=0.7. This result agrees with "site-competition epitaxy" [4].

Figure 3(a) shows a PL spectrum at 18 K for a 22 μm-thick epilayer grown with C/Si=0.6. Relatively strong free exciton peaks were observed, indicating its high purity and high quality. A relatively strong L_1 peak, the origin of which is considered to be an intrinsic defect complex, can be observed. Figure 3(b) depicts a PL spectrum at 18 K for a 25 μm-thick epilayer grown with C/Si=0.7. It is noticeable that the L_1 peak becomes weaker, suggesting that the origin of L_1 peak decreases under a C-rich condition. DLTS measurements revealed that the Z_1 center located at E_c-0.66 eV is the dominant trap. The Z_1 center concentration was 5×10^{13} cm^{-3} and 1×10^{13} cm^{-3} for epilayers grown with C/Si ratios of 0.6 and 0.7, respectively. Although the correlation between the Z_1 center (DLTS) and the L_1 center (PL) is still unopened question, the formation of both defect centers is suppressed under a C-rich condition.

Although off-axis SiC(0001) has been exclusively employed in growth and device fabrication, micropipe has been a severe obstacle. Recently, SiC(11$\bar{2}$0), which is equivalent to the cubic(110) and has a promise for the absence of micropipes and improvement

of MOSFET performance, has been investigated [5, 6]. The author's group proposes a novel crystal plane, 4H-SiC(03$\bar{3}$8), which has an inclination of 54.74° toward $\langle 01\bar{1}0 \rangle$ from 4H-SiC(0001), and is semi-equivalent to the cubic(001). Preliminary experiments on 4H-SiC(03$\bar{3}$8) yielded a net donor concentration of 1×10^{15} cm^{-3}. Comparison with the growth on off-axis (0001) will be discussed.

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Table 1 Parameters of 4H-SiC epilayers grown with C/Si=0.6 and 0.7.

C/Si	0.6	0.7
Growth rate (μm/h)	22	25
Rms (nm)	0.249	0.200
N_d (cm^{-3})	4×10^{14}	2×10^{14}
Z_1 center concentration (cm^{-3})	5×10^{13}	1×10^{13}

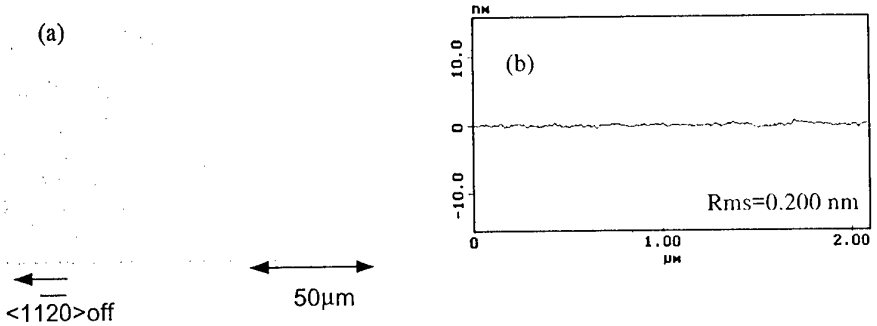


Fig. 1 (a)Nomarski photograph and (b) heigh profile of epilayer grown with C/Si=0.7.

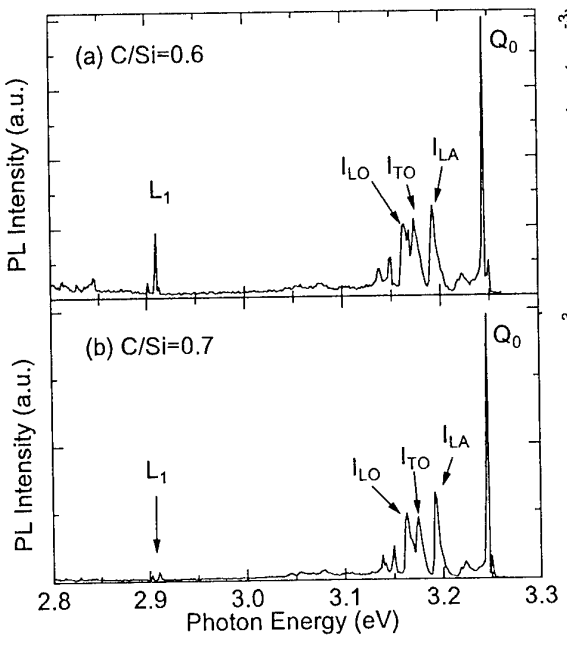


Fig. 3 PL spectra of 4H-SiC epilayers at 18K.
(a) C/Si=0.6, (b)C/Si=0.7

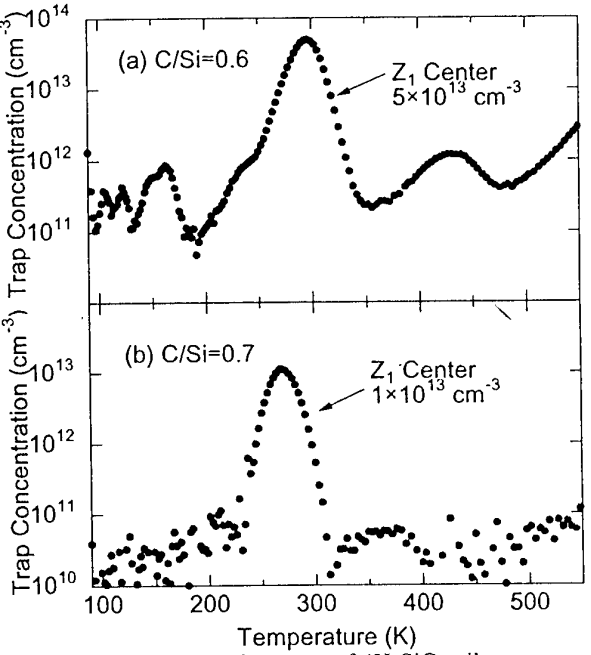


Fig. 4 DLTS spectra of 4H-SiC epilayers.
(a) C/Si=0.6, (b)C/Si=0.7

Growth and electrical characterization of the low-doped thick 4H-SiC epilayers

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High-voltage SiC devices are attractive in the development of solid-state circuit current breakers and frequency converters for power transmission and distribution systems. Tens of kV SiC bipolar devices can be expected from the superior material constants of SiC, while successful results in obtaining a 12.3 kV SiC pin diode have recently been reported [1]. The growth of very thick epilayers, along with achieving a good morphology, low doping and long minority carrier lifetime, is a key technique to obtaining such ultra high-voltage SiC bipolar devices. This paper reports the growth and electrical characterization of low-doped thick epilayers in excess of 200 μm.

We used half sections or quarter sections of 8° off 4H-SiC(0001) wafers as substrates. Epitaxial growth of 4H-SiC was performed under a reduced pressure of 40-50 Torr in a vertical radiant-heating reactor, which consists of a vertical hot-wall and inner susceptor [2, 3]. Upward SiH_4+C_3H_8+H_2 gas flow was employed in the reactor. The growth temperature was 1530-1550°C at the susceptor top, and the typical growth rate was 13-16 μm/h.

Atomic force microscopy (AFM) and Nomarski optical microscopy were used to investigate the morphology of thick 4H-SiC epilayers. Figure 1 shows an AFM image of a 246 μm-thick epilayer grown at 15 μm/h. No macro step bunching was observed, and the RMS roughness was determined as low as 0.20 nm by 10 μm x 10 μm AFM scanning. The surface was entirely specular, and the morphological defect density was less than 100 cm^{-2}. Figure 2 shows a low temperature photoluminescence (LTPL) spectrum taken from a 202 μm-thick epilayer. The LTPL spectrum shows strong free excitons and comparatively weak nitrogen bound excitons. Aluminum bound excitons and boron bound excitons are very weak.

To evaluate electrical characteristics of the thick epilayers, we fabricated Ni/4H-SiC Schottky barrier diodes (SBDs). Figure 3 shows C-V characteristics for three doping levels. From the $1/C^2$-V plots, the net doping concentrations (N_d-N_a) were determined as 1.7×10^{13} cm^{-3} for a 63 μm-thick epilayer, 6.7×10^{13} cm^{-3} for a 202 μm-thick epilayer and 4.3×10^{14} cm^{-3} for a 217 μm-thick epilayer. The $1/C^2$-V plots for the 202 μm-thick epilayer and the 217 μm-thick epilayer were fairly straight, however, the $1/C^2$-V plot for the 63 μm-thick epilayer curved at a low-voltage bias. In our DLTS measurements for epilayers doped to mid 10^{15} cm^{-3}, we found the Z_1 center with a density of $2\text{-}3\times10^{13}$ cm^{-3} in typical. For the 63 μm-thick epilayer, the doping concentration could be comparable to the Z_1 trap concentration. We also observed the L_1 line (D_1 center) from all samples used in this experiment by LTPL measurements. Influence of the deep levels (acceptor type) may be the reason for the bending of the $1/C^2$-V plot at a low-voltage bias.

In the forward I-V characteristics of the SBDs (Fig. 4), the specific on-resistance was 1.9 Ωcm^2 for the 202 μm-thick epilayer and 0.27 Ωcm^2 for the 217 μm-thick epilayer. This on-resistance implies high electron mobility with regard to the thickness and doping levels. The n-factors of 1.04 for a 1 mmϕ SBD (202 μm-thick epilayer) and 1.03 for a 0.5 mmϕ SBD (217 μm-thick epilayer) were obtained. On the other hand, the specific on-resistance of the 63 μm-thick epilayer was as high as 3.2×10^3 Ωcm^2, which corresponds to a resistivity of 5.1×10^5 Ωcm. We suppose that this rather high resistivity is a consequence of the reduction of background doping down to an equivalent concentration of the intrinsic defects.

In the reverse I-V characteristics (Fig. 5), the highest breakdown voltage of –6.3 kV was achieved for a 1.0 mmϕ SBD fabricated on the 202 μm-thick epilayer, even though no edge termination or surface passivation was processed. The leakage current density at –6.0 kV was 1.3×10^{-5} A/cm^2. Using the 217 μm-thick epilayer, the highest breakdown voltage of –6.4 kV was achieved for a 0.5 mmϕ SBD.

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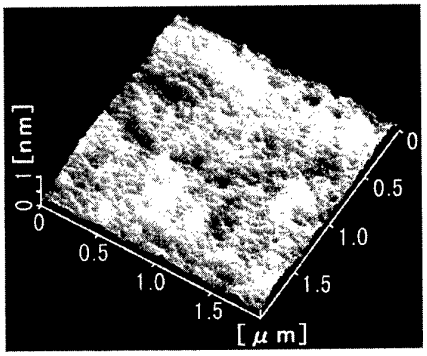


Fig. 1. AFM image of a 246 μm-thick epilayer (grown at 15 μm/h).

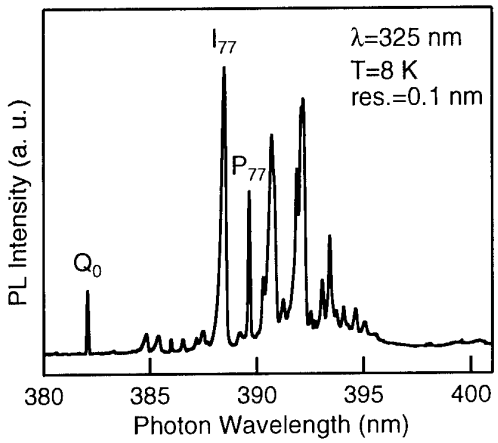


Fig. 2. LTPL spectrum taken from a 202 μm-thick epilayer (grown at 14 μm/h).

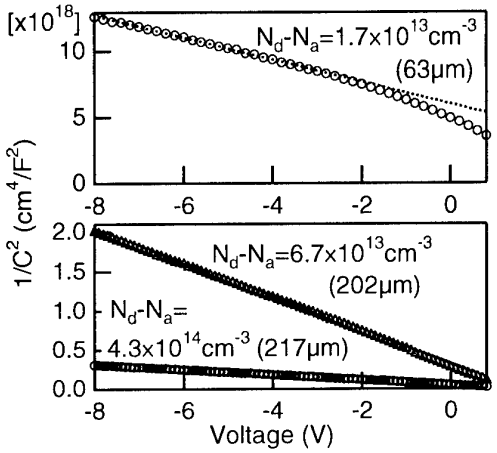


Fig. 3. C-V characteristics of Ni/4H-SiC SBDs fabricated on thick epilayers.

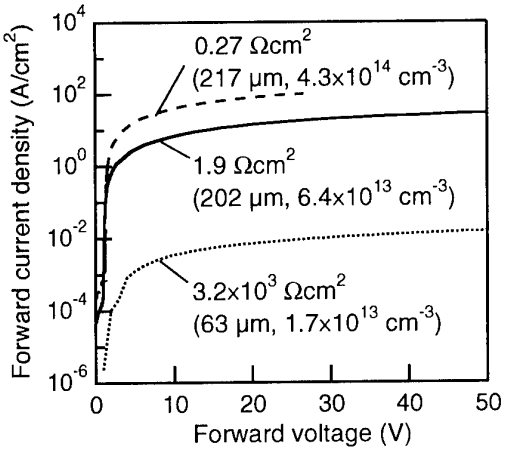


Fig. 4. Forward I-V characteristics of Ni/4H-SiC SBDs fabricated on thick epilayers.

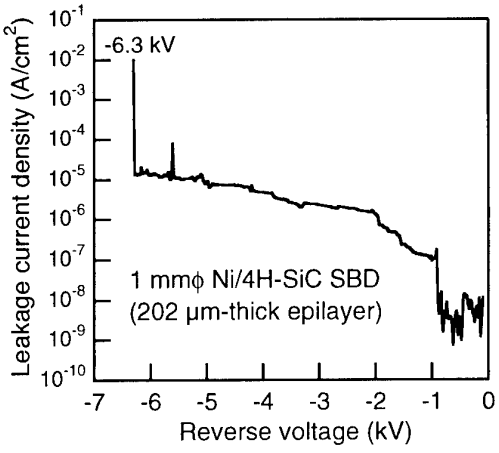


Fig. 5. Reverse I-V characteristics of a 1 mmϕ Ni/4H-SiC SBD fabricated on a 202 μm-thick epilayer.

High-Rate Epitaxial Growth of 4H-SiC using a Vertical-Type, Quasi-Hot-Wall CVD Reactor

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For power devices with high breakdown voltage, thick epitaxial layers are needed. If an epitaxial layer of 50 μm thickness is required, it takes more than 10-25 hours to grow when the growth rate is 2-5 μm/hr. This brings not only long process time but also increased consumption of substrate susceptor, which increases process cost. Therefore researches trying to obtain high growth rate of around 20-50 μm/hr have been done in recent years [1, 2]. We have obtained high growth rate of reaching about 70 μm/hr by using a vertical type, quasi-hot-wall CVD reactor. In this paper, growth conditions for obtaining high growth rate at relatively high temperature range (1600-1800 °C) are studied.

A vertical quasi-hot-wall CVD reactor which can set maximum a 75 mm diameter substrate wafer was used in this experiments. The process gases (SiH_4, C_3H_8, H_2) were distributed upwards through an inductively heated graphite nozzle. The 8° off-axis 4H-SiC (0001) substrates were attached to the susceptor so that the growth surface exposed downwards to the process gases. The growth temperature was in the range of 1600-1800 °C and the growth pressure was in the range of 2-760 Torr. The C/Si ratio was fixed to 1.5. The thickness of the grown layer was measured by observing the cleaved cross-section of substrates using scanning electron microscope. The etching rate was determined from the weight loss of the substrate using a microblance. The grown surfaces were examined with Nomarski differential interference contrast microscopy (NDIC).

Temperature dependence of the growth rate and the H_2 etching rate are shown in Fig. 1. The growth rate decreased with increasing the temperature in this range. The reason is that the H_2 etching rate increases exponentially with increasing the temperature. Pressure dependence of the growth rate and the etching rate at H_2 flow rate of 10 L/min are shown in Fig. 2. The etching rate (crosses in Fig. 2) dramatically decreased with increasing pressure. This result is qualitatively in agreement with the result using the vertical CVD reactor which we have previously reported [3]. The growth rate increased with increasing pressure in the lower pressure range of less than about 20 Torr (triangles). This may be explained in term of dramatic decrease in H_2 etching rate with increasing pressure [1, 4]. On the contrary, in the case of higher-pressure range of more than about 20 Torr, the growth rate decreased with increasing pressure (circles). This indicates that the species, which contribute to the growth, may be reduced with increasing the pressure. Figure 3 shows SiH_4 flow rate dependence of the growth rate at the pressure of 20 Torr. In this figure, solid symbols mean mirror-like surface morphologies, and open symbols mean rough surfaces. The growth rate increased with increasing SiH_4 flow rate. The grown surface, however, became rough when the SiH_4 was supplied excessively. The growth rate became low as the temperature became high. The growth rate of about 30 μm/hr was obtained at the temperature of 1800 °C and the SiH_4 flow rate of 36 cc/min when the H_2 flow rate was 10 L/min. Furthermore, the growth rate of 70 μm/hr was obtained at the same temperature and SiH_4 flow rate when the H_2 flow rate

was increased to15 L/min. Figure 4 shows the NDIC images of these grown surfaces. Fig. 4 (a) and (b) show the surface morphology of the epitaxial layer grown at the rate of 70 μ m/hr and 26 μ m/hr, respectively. Both surfaces were specular. However, the surface morphology of Fig. 4 (a) is rougher than that of Fig. 4 (b).

This work was performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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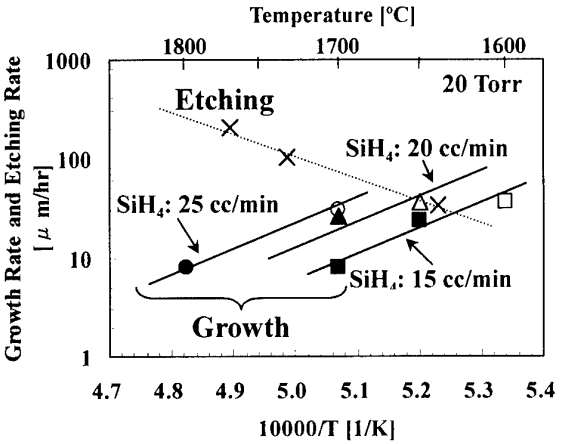


Fig. 1. Temperature dependence of growth rate and etching rate. Crosses mean etching rate. Circles, triangles, and squares mean growth rate. Solid symbols mean mirror-like surfaces and open symbols mean rough surfaces. The pressure is 20 Torr at all conditions.

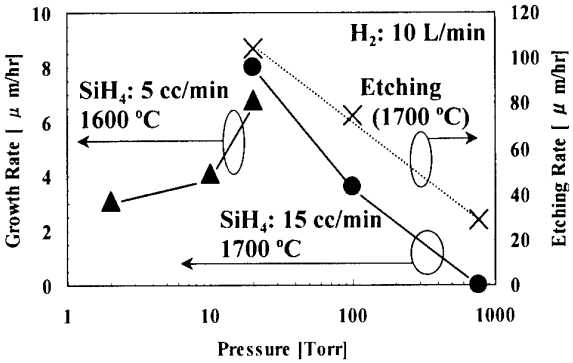


Fig. 2. Pressure dependence of growth rate and etching rate. Crosses mean etching rate. Circles and triangles mean growth rate. The condition is SiH_4 of 5 cc/min, temperature of 1600 °C for triangles and SiH_4 of 15 cc/min, temperature of 1700 °C for circles. The H_2 flow rate is 10 L/min.

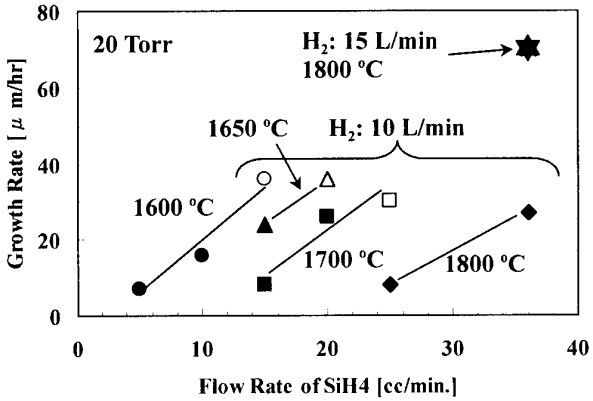


Fig. 3. SiH_4 flow rate dependence of growth rate. The H_2 flow rate is 10 L/min for circles, triangles, squares, and diamonds and 15L/min for a star. Solid symbols mean mirror-like surfaces and open symbols mean rough surfaces. The pressure is 20 Torr at all conditions.

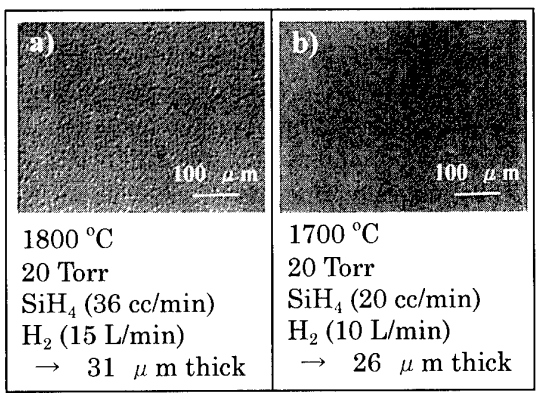


Fig. 4. Examples of NDIC images of the grown surfaces. The growth rate is 70 μ m/hr for a) and 26 μ m/hr for b).

FrA2 High Frequency Device

[redacted]

4*H*-SiC IMPATT Diode Fabrication and Testing

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Recent progress in 4*H*-SiC material characterisation, epitaxial growth and device processing paved the way to design and fabricate 4*H*-SiC IMPact-ionisation Avalanche Transit-Time (IMPATT) diodes. This paper reports on the fabrication and testing of pulsed 4*H*-SiC IMPATT diode.

Commercial 4*H*-SiC p^+-n-n^+ epitaxial wafers from Cree Inc. were used to fabricate the diodes. The n layer had a donor concentration of $1.1\cdot10^{17}$cm^{-3} and a thickness of 2 μm, which is close to the thickness of the space charge region at avalanche breakdown. The acceptor concentration in the 1 μm thick p^+ layer was equal to $8\cdot10^{18}$cm^{-3}. A rapid thermal annealing of Ni containing metal compositions was used to form ohmic contacts to p- and n-type 4*H*-SiC. This technique provides low resistivity contacts

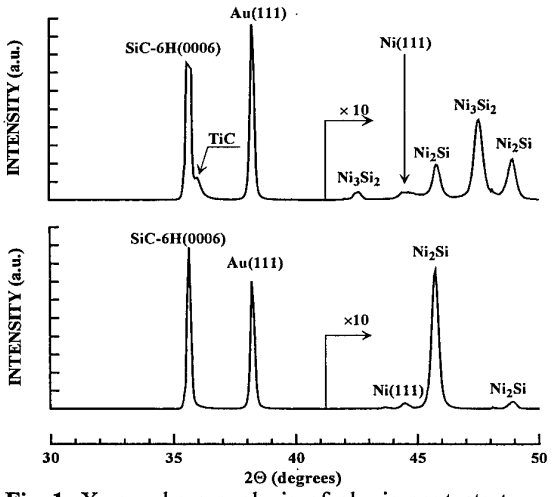


Fig. 1. X ray phase analysis of ohmic contacts to p- (top trace) and n-type SiC (bottom trace) formed on test 6H-SiC samples after Au overlay deposition.

($\sim3\cdot10^{-5}\Omega\cdot$cm^2) suitable for further overlay deposition and bonding. The structure of these contacts investigated by x-ray phase analysis is shown in Fig. 1. Another key issue of IMPATT diode device processing is a p-n junction edge termination, due to its operation at high current, high voltage, and high temperature. The edge termination by mesa structure with no sidewall surface passivation was chosen as a most convenient technique for this diode. The mesa structures with different areas were formed by reactive ion etching in SF_6/Ar gas mixture. Test samples with polished backside were fabricated to investigate the initial breakdown localisation by direct observation of the electroluminescence (Fig. 2). This investigation shows an evident correlation of preliminary breakdown with the state of sidewall surface. The RIE process was optimised to obtain contamination free, smooth surface of the sidewalls.

The diodes had breakdown voltages of 300 V and series resistivities of $6\cdot10^{-5}\Omega\cdot$cm^2.

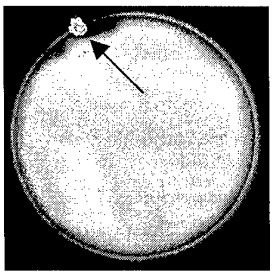


Fig 2. Electroluminescence (EL) of 4H-SiC diodes (mesa diameter of 200 μm) with preliminary breakdown. For localisation of breakdown point, EL under forward bias and at the breakdown shown by arrow are superimposed in one image.

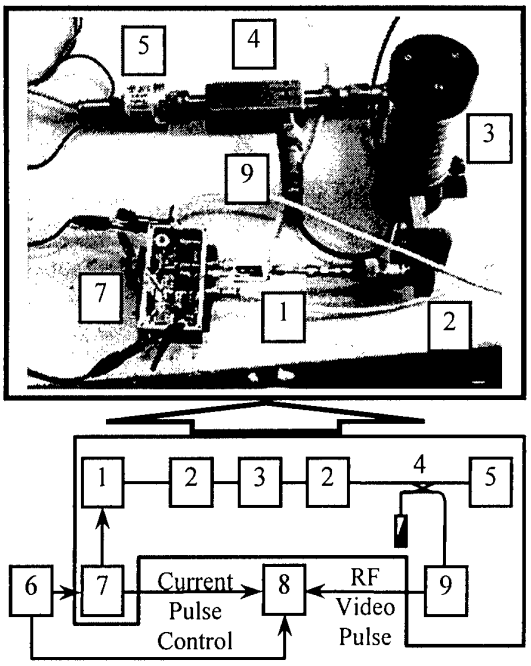


Fig. 3. View and block diagram of the experimental setup for measurement of operating frequency and output power of pulsed SiC IMPATT oscillator. 1- microstrip oscillator; 2- coaxial waveguide junction; 3- cavity-resonator wavemeter; 4- directional coupler; 5- microwave power meter; 6- pulsed voltage master oscillator; 7- pulsed current source; 8- two channel oscilloscope; 9- microwave pulse detector.

A maximum dc current density of 950 A/cm^2 was passed through the diodes. It is much lower than the anticipated operating current density of SiC IMPATT diode. For this reason, microwave measurements were done in pulse mode. The diodes were biased with dc avalanche current of 100 nA to charge the capacitance of the *p-n* junction. Then, the current pulses were applied to the diode. The shape of pulsed current and voltage was controlled by the oscilloscope.

For microwave measurements, the diodes were mounted in broad band microstrip oscillators, since the operating frequency of the diodes was expected to be from about 6 to 20 GHz. A special design of the microstrip oscillator was performed to meet the very high breakdown voltage of SiC IMPATT diodes. Fig. 3 shows an experimental setup for measurement of operating frequency and output power of pulsed SiC IMPATT diodes.

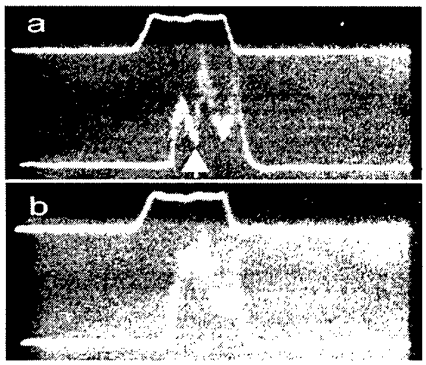


Fig. 4. The oscilloscope patterns of input current pulse (top trace) and corresponding output power video pulse (bottom trace) taken at various positions of cavity-resonator wavemeter; (a) 9.9 GHz, recess due to power absorption by wavemeter is shown by arrow; (b) 9.0 GHz, no recess on video pulse.

The microwave oscillations appeared when an input current of 0.3 A was passed through the diodes with mesa diameter of 80 μm. The corresponding threshold current density was 6 kA/cm^2. The frequency of oscillations was in X-band (8.2-12.4 GHz). A microwave power of about 300 mW was measured at the pulse current of 0.35 A and pulse width of 40 ns. The self-heating of the *p-n* junction led to the change of the diode impedance and load matching conditions during the pulse. This caused a delay of the front edge of microwave video pulse clearly seen in Fig. 4 and a frequency chirp through the pulse duration.

In conclusion, the measurements of operating frequency of SiC IMPATT diodes with specific doping profile provide the basis for their accurate numerical design. Simple frequency scaling of these experimental results shows that the maximum operating frequency of 4H-SiC IMPATT diodes (with p-n junction plane oriented close to the basal plane) does not exceed 200 GHz. This dramatically changes a traditional opinion about advanced performance of SiC for fabrication of mm-wave IMPATT diodes.

This work was partially supported by INTAS CNES 97-1386 grant. FORTH also acknowledges the support through NATO SfP 971879 grant.

HIGH-PERFORMANCE SILICON CARBIDE MESFET UTILIZING LATERAL EPITAXY

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Silicon carbide is a promising material for high power microwave applications. A new generation of microwave power amplifiers is expected with introduction of silicon carbide device technology, however the results demonstrated so far do not meet theoretical expectations. There is currently no common opinion in literature on the origin of problems. In this report we demonstrate that the shortcomings of today's silicon carbide power microwave devices originate from the limitations of conventional MESFET design. We propose a new concept of silicon carbide MESFET with near-theoretical performance.

A high breakdown field in silicon carbide does not automatically result in high operation voltages of a microwave MESFET. This can be illustrated by simulation of a standard MESFET with a low-doped p-type buffer layer. A short gate length is desirable for efficient high-frequency operation, however a decrease of the gate length results in a dramatic drop of the blocking voltage, as it is seen in curve families plotted Figure 1. The low blocking voltage originates from short-channel effects, which result in the current bypassing the physical channel and in punch-through of a parasitic bipolar transistor, as it is illustrated by the 2-dimensional plots in Figure 2.

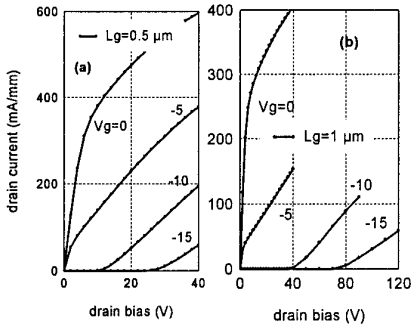


Figure 1. Simulated curve families for SiC MESFETs with uniform buffer-layer doping and a gate length of 0.5 μm (a) and 1 μm (b).

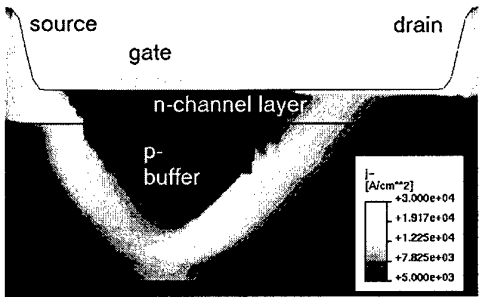


Figure 2. Simulated current contours for the source-to-drain punchthrough of SiC MESFET. Lg=1 μm, p-buffer doping is $3x10^{15}cm^{-3}$, drain and gate bias is Vd=100V, Vg=-15V.

The reason for enhancement of short-channel effects in SiC is inherently related to the high breakdown field in SiC. A high electric field implicates a greater penetration of the electric field underneath the channel. The use of either a longer gate or a higher p-type doping in the buffer layer is required to suppress the short-channel effects, however both approaches deteriorate high-frequency device performance. Additional problems appear if the MESFET is formed on a semi-insulating (SI) substrate. Charge accumulation can develop in either the buffer layer or the adjacent semi-insulating material.

The MESFET concept proposed in the present work follows the approach of self-aligned silicon LD MOS design. Self-aligned lateral diffusion (LD) technique is employed in LD MOS fabrication to form a depletion stopper in the vicinity of the source and to suppress short-channel effects. In SiC the required self-aligned doping profiles can be achieved by lateral epitaxy (LE) onto the walls of pre-etched trenches

[1]. The material outside the trenches is removed by planarization. The active region is then deposited by CVD, and source, gate and drain contacts are formed, as it is shown in Figure 3. An important advantage of the design is the possibility of forming a buried source region. This minimizes the source resistance and compensates for relatively low electron mobility in SiC.

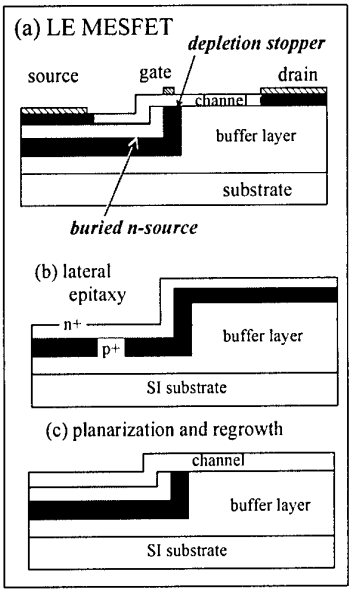


Figure 3. Cross-section of silicon carbide LE MESFET (a) and suggested fabrication scheme (b,c)

Simulations of LE (lateral epitaxy) MESFETs in 4H SiC show a dramatic performance improvement with this design. High electric field is terminated by the depletion stopper, as it is illustrated by the 2-dimensional plots of electric field in Figure 4. Inevitable electric field concentration at the gate edge has therefore no effect on the breakdown voltage. A gate of 0.1-0.3 μm is sufficient for switching a few hundred volts. The curve families for a 0.3 μm gate device show a very low output conductance and an average breakdown field of more than 200 Volts per 1 μm of the drift region length. The knee current is remarkably high due to the low source-to-gate resistance provided by the buried source design. The carrier trapping to the SI substrate is entirely eliminated in LE MESFET design, since the current pathway to the substrate is blocked by the depletion stopper.

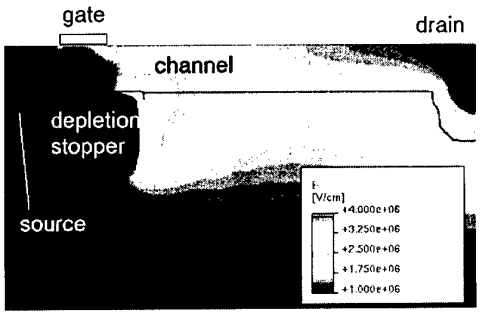


Figure 4. Contours of electric field for SiC LE MESFET simulated for Vg=-10 V, Vd=450V. Gate length is 0.3 μm, drift region length is 2 μm

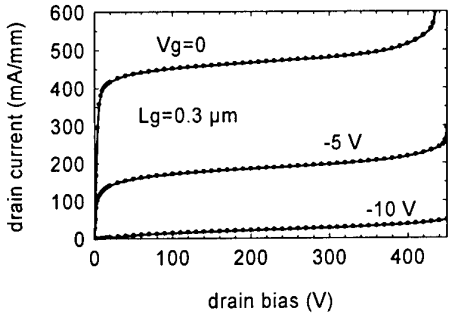


Figure 5. Simulated curve families for the LE MESFETs shown in figure 4

In the report we will discuss the dependence of LE MESFET performance on design features. The possibility of achieving a blocking voltage of up to 300 V/μm using optimized drain/stopper doping profiles will be demonstrated. The gate length can be decreased below 100 nm without considerable drop of the transconductance. Practical implementation of LE MESFET technology will be presented in a separate report at this Conference. This work was supported by the Swedish Power Microwave Consortium and by the Naval International Cooperation Program, C. Wood, supervisor.

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Hot-carrier luminescence in 4H-SiC MESFET's

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We present the first experimental results of photon emission from MESFET's built on 4H-SiC. When the device is biased in the saturation regime, energy dissipation of the channel hot electrons is possible via two main mechanisms : optical phonon scattering and impact ionization. Additionally, some electrons loose their energy by undergoing radiative transitions which can be detected in the optical range using a photon emission set-up. Analysis of this emission is of particular interest : first, it allows one to detect and localize defects giving rise to excess leakage and premature breakdown in power devices and second, it is a useful tool when investigating the hot carrier properties of FET devices. In this study, we focus on the emission mechanisms and its link to impact ionization in SiC MESFET's.

The MESFETs (see Figure 1) were fabricated at Thomson-CSF/LCR. The channel is an n-type epilayer separated from the 300 μm thick semi-insulating 4H-SiC substrate by a p-type buffer layer. Substrate and epilayers were from Cree Research. For this study, gate lengths from 1μm to 8 μm were investigated, the source/gate and drain/gate spacing were respectively around 0.5 and 2.5 μm. They are studied using a photon emission set-up already described in [1].

Summarized below are the main features which have been found :

- Light emission mechanisms in SiC MESFET's under high electric fields are strongly related to a midgap level (Figure 2). This level has already been detected in SiC MOSFET's in both 4H and 6H polytypes [1] and is responsible for a specific relationship between ionization currents and light intensity. We shall assume in this study that the relationship still holds in SiC MESFET's.
- When plotted as a function of gate voltage, the light intensity (I_ν) follows a "bell-shaped" curve (Figure 3) which reveals its link with hot carriers relaxation in the channel. In contrast, gate currents are dominated by Schottky junction leakage (not shown here) and can not be used for hot carrier analysis. Further analysis allows us to extract the ionization coefficient Bi without measuring the gate current (Figure 4).
- The position of the maximum electric field in the drift region can be monitored (Figure 5) and its shifting towards the gate edge is demonstrated when biasing the devices towards pinch-off (Figure 6).

[1] E. Bano, C. Banc, T. Ouisse, and S. Scharnholz, Solid-State-Electronics. vol.44, no.1; Jan. 2000; p.63-69

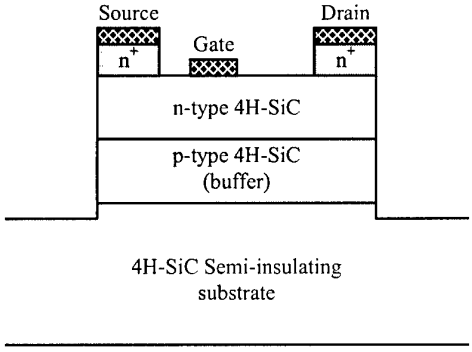


Figure 1 : Schematic cross-section of the studied devices.

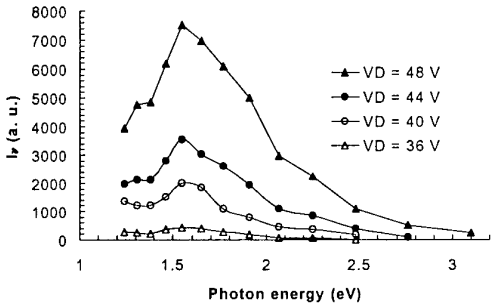


Figure 2 : Spectral analysis.

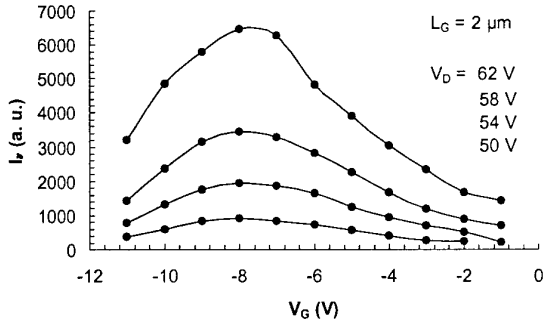


Figure 3 : "Bell shaped" behavior of the light emission.

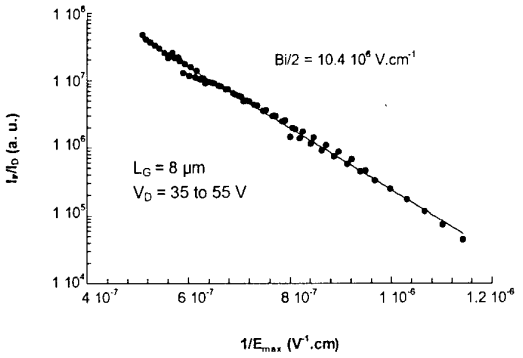


Figure 4 : Extraction of the ionization multiplication coefficient.

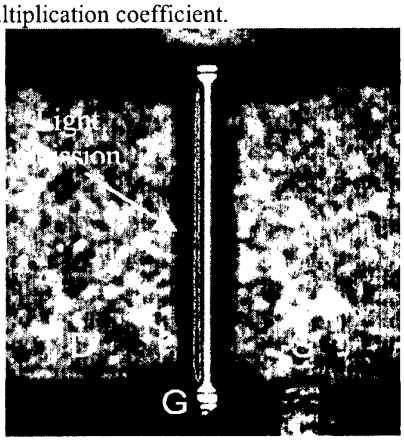


Figure 5 : Photon emission image of a device in the saturation regime superimposed on the same device under direct illumination.

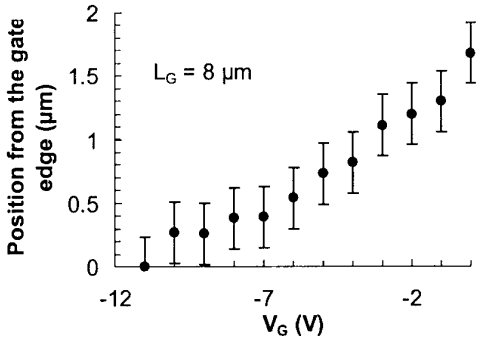


Figure 6 : Position of the electric field peak as measured by photon emission, as a function of the gate voltage.

Development and Demonstration of High Power X-Band SiC MESFETs

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Silicon Carbide (SiC) shows the promise to operate from VHF through X-Band frequencies while providing higher breakdown voltage, better thermal conductivity, and wider transmit bandwidths compared with Si or GaAs. Previously reported SiC MESFETs had small die sizes with gate widths in the range of 100s μm [1-3]. In this paper, we present for the first time the development of large SiC MESFETs with a gate length of 0.2 μm and a total width of 3.2 mm fabricated on semi-insulating 4H-SiC substrate, for high power communications applications. Devices showed a f_T = 14.5 GHz , f_{MAX} = 38 GHz , and a current gain of 16 dB at 2 GHz while biased at a high operating voltage of 40 volts.

MESFETs were fabricated on semi-insulating 4H-SiC substrate ($>10^5$ Ω-cm). Epitaxial layers consists of an undoped buffer layer, 0.25 μm channel layer doped to 2.5 x 10^{17} cm^{-3}, and a 0.075 μm n+ layer doped to 10^{19} cm^{-3}. E-beam lithography was used to define a gate length of 0.2 μm. Fig. 1 is a microphotograph of a MESFET with 32-fingers. Air-bridges were used to interconnect the drain fingers of multifinger devices. Fig. 2 shows the DC characteristics of a 32-finger MESFET with a gate periphery of 3.2 mm; the maximum drain current can be seen is 400 mA . The DC transconductance, g_m, was measured to be 40 mS. These devices exhibit high gate-drain breakdown voltage of 150 volts and a blocking voltage gain of 10. A device yield of 20% was obtained for 50 mm diameter wafers.

Small-signal RF characteristics of these MESFETs were measured on wafer and with packaging. The small signal gain calculated from the S-parameters is shown in Fig. 3; a unity current gain frequency, f_T , of 14.5 GHz was observed. The measured S-parameters are being modeled using the conventional MESFET equivalent circuit model and will be reported in the full length paper.

In summary, we have demonstrated large SiC MESFETs with 3.2 mm gate width on semi-insulating 4H-SiC substrates. These devices show very high drain current while simultaneously providing a high operation voltage of Vds=100 volts. These results demonstrate the advantage of 4H-SiC for high power microwave applications where its high thermal conductivity, high voltage and high power density capability are essential for a major reduction on system size/weight.

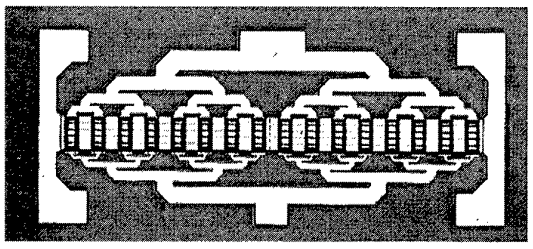


Figure 1. A photomicrograph of a SiC MESFET Die with a total gate width of 3.2 mm.

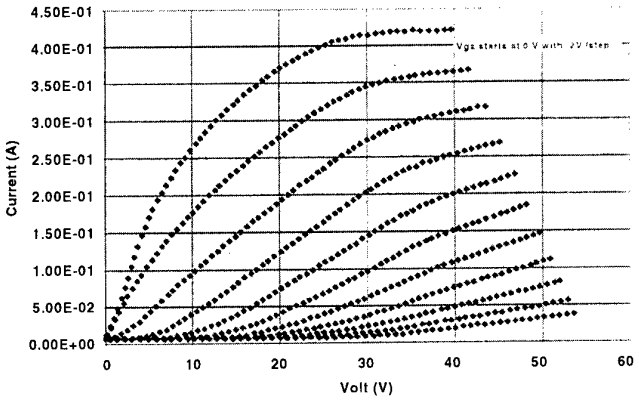


Fig. 2. DC characteristics of 3.2 mm periphery 4H-SiC MESFET.
Top trace is for V_g=0 volt.

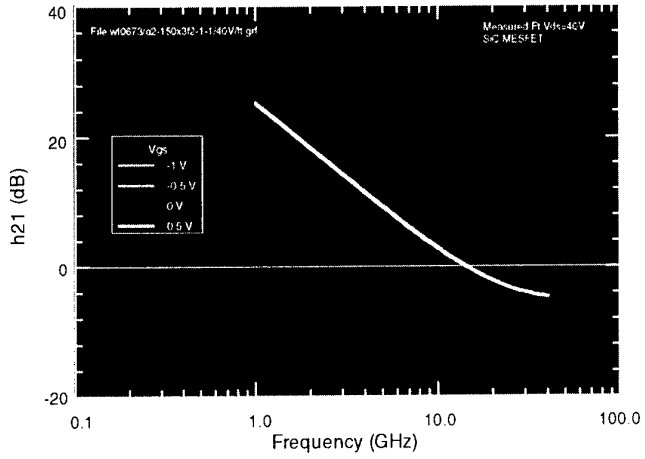


Fig. 3. Small-signal RF characteristics of 0.2 μm gate 4H-SiC MESFET
for V_d = 40 volts, and V_g = -0.5 volts.

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Influence of Semi–Insulating Substrates Purity on the Output Characteristics of 4H-SiC MESFETs

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The ability of SiC for high power RF transistors has been demonstrated by impressive results. For instance, a power density of 4.6 W/mm [1] for a transistor with gate width inferior to 1 mm as been obtained, and, an output power of 80 W at 3 GHz as also been reported [2]. Nevertheless, in the latter case, the power density was only 1.67 W/mm. The origin of this power density reduction for large transistors in comparison to smaller ones has been tentatively attributed to trapping phenomena [3]. An other possible explanation is a self heating of the structure [4]. In this study we will focus on the first point : trapping phenomena. The development of 4H-SiC MESFETs for high frequency applications requires the use of SI substrates in order to reduce parasitic losses. For SI substrates obtained by physical vapor transport (PVT), the semi-insulating behavior is usually obtained by compensation of the conductive substrates by deep level incorporation such as vanadium. Some results on "vanadium free" substrates has also been reported, but deep traps with activation energy of 1.1 eV was also present in this material [5]. Recently an other source of high purity semi-insulating substrates obtained by HTCVD has appeared on the market [6].
Using different defect characterization tools we establish a correlation between the presence of deep defects in the substrate and defective operation in the static output characteristics of the MESFETs. The defects in the structure have been analyzed by DLTS measurement on the gate contact, frequency dispersion of the output conductance as a function of temperature and current transient spectroscopy.

I_{ds}-V_{ds} measurements as a function of temperature have been performed in the range 300 K – 600 K. Different parasitic effects have been observed for the transistors realized on PVT SI substrates. The major one, shown on Fig.1, is an hysteresis effect of the output conductance when the gate voltage is successively increased and decreased. This effect is enhanced for the high gate voltage (i.e. when the current flows near the substrate). When increasing the temperature the phenomenon progressively reduces and almost disappears at 500 K. A possible explanation for this hysteresis effect is the presence of deep centers which are at the origin of a parasitic gate under the channel.

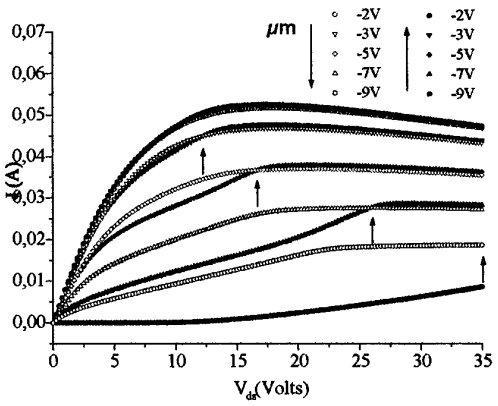


Figure 1 : Output characteristics at 300 K for a sample without buffer layer on a substrate realized by PVT. The hysteresis effect is materialized by the vertical arrows.

Random Telegraph Signal (RTS) measurements have next been realized. For samples without buffer layer, a strong RTS signal is obtained only for high gate voltage. This confirm the presence of traps near the channel/substrate interface.

In order to extract the trap signature, frequency dispersion of the output conductance has been performed in saturation regime (Vg = -5V, Vds = 5V). The predominant trap detected by this measurement has an activation energy of about 1.1 eV (Fig. 2). The identification of this trap is not yet clear. The activation energy (1.07 eV) is close to the value measured by resistivity variation as function of temperature (1.18 eV) by Augustine et al. in the case of 4H-SiC SI substrates containing Vanadium [7]. Using the same measurement method, an activation energy of 1.1 eV was also found in the case of Vanadium free 4H-SiC SI substrates by Mitchel et al [5].

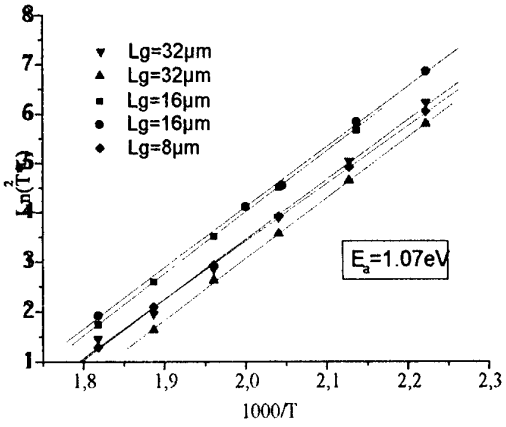


Figure 2 : Signatures obtained by frequency dispersion of drain source conductance measurements for a sample with p-type buffer layer.

From the results we have obtained, it seems clear that deep traps in the substrate are at the origin of parasitic effect on the output characteristics. Nevertheless, no evidence of defective operations in the output characteristics and no variation of the output conductance with frequency was observed in two cases :

- Firstly when an optimized buffer layer is used in order to prevent electron injection toward the substrate,
- Secondly when an high purity HTCVD SI substrate provided by Okmetic is used.

This confirms the role of the substrate purity on the devices performance and gives hope for developing 4H-SiC MESFETs technology.

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Demonstration of IMPATT Diode Oscillators in 4H-SiC

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Impact ionization avalanche transit time (IMPATT) diodes are used to generate RF power at microwave frequencies for applications such as pulsed radar. The RF power available from an IMPATT diode in the electronic limit is proportional to $(E_C \cdot v_S / f)^2$, where E_C is the critical field for avalanche breakdown and v_S is the saturation drift velocity. Since $(E_C \cdot v_S)$ in SiC is approximately 20x higher than in silicon or GaAs, the power available from a SiC IMPATT diode is theoretically about 400x higher than either silicon or GaAs.

We have fabricated both X-band and Ka-band IMPATT diodes in 4H-SiC [1,2] using the hi-lo doping structure shown in Fig. 1. In the X-band device, the p+ layer is 1.4×10^{19} cm^{-3} and 0.5 μm, the n avalanche region is 5×10^{16} cm^{-3} and 2.3 μm, while the n- drift region is 3.8×10^{15} cm^{-3} and 6.0 μm. As shown in Fig. 2, the static I-V characteristics exhibit stable avalanche breakdown at about 800 V reverse bias. Figure 3 shows the predicted operating characteristics of the X-band diode as a function of bias current density, as obtained from MEDICI simulations [1]. The maximum power is expected to be in excess of 3 kW at a bias current density of 8 kA/cm^2, with an efficiency of 9 %.

Devices are mounted in a pillbox package, coated with silicone gel to prevent arcing, and tested in a microwave cavity as shown in Fig. 4. Bias pulses of 200 - 800 ns and up to 1000 V are applied through a series resistance, resulting in bias currents of 100 - 300 mA. Figure 5 shows the spectral output of an X-band diode [1,2]. Accounting for the 20 dB pad, the RF power is about 0 dBm (1 mW) at 7.75 GHz. The envelope of the voltage waveform across the 50 Ω input impedance of the sampling scope is shown in Fig. 6.

The maximum power obtained to date is about 300 mW at X-band. This power is lower than expected due to several factors: (i) to avoid destroying the diode, the bias current is about 5x lower than the optimum in Fig. 3, (ii) v_S parallel to the c-axis in 4H-SiC may be much lower than the 2×10^7 cm/s assumed in our design [3]; if so, the transit time across the drift region may not be optimum for X-band operation, (iii) our bias circuit does not maintain a constant current during the bias pulse (see Fig. 6), (iv) the diodes tested to date are not of the optimum area for best power, and (v) the microwave environment of the cavity and bias line are not fully optimized. We expect significantly higher power once many of these factors are resolved. Latest results will be reported at the conference.

This work is supported by ONR under MURI grant N00014-96-1-1215. D. B. Janes, D. L. Landt, R. J. Trew, S. B. Creswick, and J. R. Fines provided valuable technical advice or assistance.

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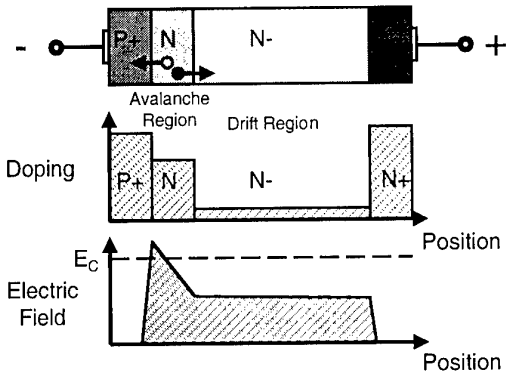


Fig. 1. Hi-lo doping structure and electric field profile of the SiC IMPATT diode.

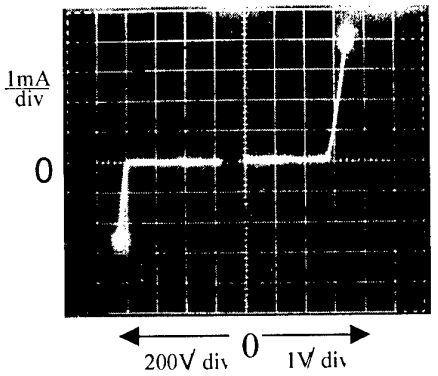


Fig. 2. Forward and reverse static I-V characteristics of the X-band diode.

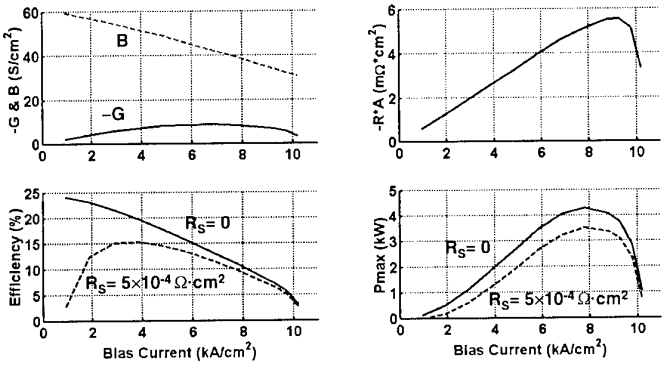


Fig. 3. Simulated admittance, negative resistance, efficiency, and power for the X-band IMP ATT diode.

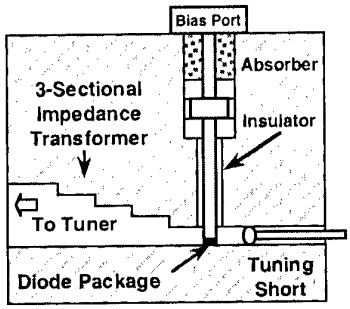


Fig. 4. Reduced-height waveguide cavity with bias port.

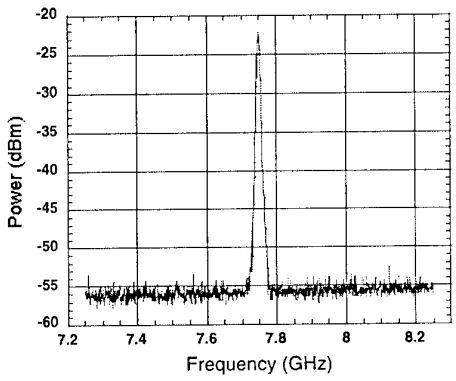


Fig. 5. Spectral output of the X-band IMPATT diode (measured with a 20 dB attenuator).

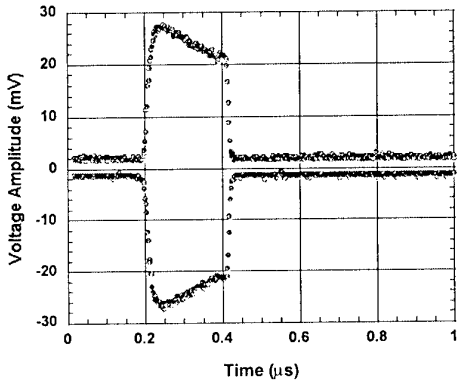


Fig. 6. Time domain envelope of the X-band IMPATT diode into the 50 Ω input of a sampling oscilloscope.

Late News

[redacted]

High Temperature performance of 10 Kilovolts, 200 Amperes (Pulsed) 4H-SiC PiN Rectifiers

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SiC is a superior material system for the fabrication of ultra high voltage devices since it is capable of sustaining a very high power density, which can be switched at an extremely high speed, while operating at very high temperatures. Such diodes would be suitable for solid state power conditioning systems for high power radar, directed energy weapons, X-ray generators, electrostatic precipitators and high power LASERs. This paper reports the highest power single chip 4H-SiC PiN rectifier demonstrated to date, with a 2 MegaWatt (Pulsed) capability.

These diodes had an active metallized Anode area of approximately 0.09 cm^2 (3mm X 3mm). A high purity, 150 μm n^- epitaxial layer doped at 7E14 cm^{-3} was used in the fabrication of these rectifiers. This voltage-blocking layer was grown using a refined hot wall CVD growth reactor yielding low epi defect densities. The highly doped, 1.8 μm p+ Anode was grown epitaxially in order to obtain good carrier injection during on-state operation. To prevent premature breakdown, the voltage blocking layer was exposed using reactive ion etching, and a 400 μm wide, optimized Junction Termination Extension (JTE) was implemented using a p-type implant at the periphery of the device edge. The SiC surface at the edges were then passivated using a thick SiO_2 layer. This termination allowed a 10 kV blocking capability with a leakage current of only 20 μA for these 3mm X 3mm diodes. Measurements conducted up to 200°C and 3 kV show practically no change in the leakage current using our measurement system with a 3 μA sensitivity. Measurements at higher voltages will be presented at the conference.

The forward characteristics were found to be fairly uniform on rectifiers fabricated throughout the wafer, with most rectifiers turning on close to the built-in voltage (2.9 to 3 V) of 4H-SiC. Thereafter, these rectifiers have a much steeper I-V slope as compared to Si diodes. At room temperature, pulsed measurements using a high power curve tracer shows that the forward voltage drop was 4.5 V at 100 A/cm^2 (10 A); 7.07 V at 500 A/cm^2 (45 A); and only 12.5 V at 2200 A/cm^2 (200 A). On-state measurements conducted in the room temperature to 200°C temperature range (in 50°C intervals) show a slight reduction in on-state voltage drop from 7.2 V to 6.9 V at 50 A on this packaged device.

These rectifiers show fairly stable reverse recovery switching characteristics as the operating temperature was increased from 25°C to 200°C. A forward current of 20 A (220 A/cm^2) was switched at a reverse dI/dt of 120 A/μsec with an applied reverse voltage of 100 V. At room temperature, the peak reverse recovery current of only 8.7 A was observed and the device turned off completely within 600 nsec. This complete turn-off time increases to 1 μsec at 200°C under similar test conditions. The peak reverse recovery increases a modest 72% to 15 A between room temperature and 200°C.

Wafer maps showing the distribution of on-state voltage drop and blocking voltage show fairly good yields when a criteria of >7 kV, 4.5 V (100 A/cm^2) is used. These data and the details of high temperature measurements will be presented at the conference.

This work is supported in part by Wright Labs under DUS&T Technology Investment Agreement number F33615-01-2-2108, monitored by Jim Scofield.

Electrical Activation of Implanted Phosphorus Ions in (0001)/(11$\bar{2}$0)-oriented 4H-SiC

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Rutherford Backscattering and Cross-Sectional Transmission Electron Microscopy investigations conducted by Satoh and Nakaike (1st Int. Workshop on Ultra-Low Loss Power Device Technology, May 2000, Nara, Japan) revealed that implantation-induced amorphous 6H-SiC epilayers oriented in ($1\bar{1}00$)-direction could largely be recrystallized at 1500°C preserving the polytype of the underlying layer, while (0001)-oriented 6H-SiC epilayers showed a high density of extended defects even after an anneal at 1700°C.

In this study, we have performed comparative Hall effect investigations on phosphorus (P)-implanted, Si-face/a-plane ((0001)/(11$\bar{2}$0)-oriented) p-type 4H-SiC epilayers in order to examine whether the electrical activation of P donors implanted into a-plane samples is also superior to that one in samples with Si-face. We implanted two P box profiles (profile 1: T_{impl} = room temperature, depth = 1.3 µm, [P] = 10^{18} cm^{-3}, profile 2: T_{impl} = 500°C, depth = 0.8 µm, [P] = 10^{20} cm^{-3}) and performed annealings in the temperature range from 1400° to 1700°C. As an example, the temperature dependence of the free electron concentration n and of the electron Hall mobility µ for two pairs of samples oriented in (0001) (samples 1(Si)/2(Si)) and in (11$\bar{2}$0) (samples 1(a)/2(a)) direction are displayed in Figs. 1(a)/(b). Sample 1/2 was implanted with the P profile 1/2. All the samples were annealed at 1600°C. The following results are observed: (i) The electrical activation of P donors implanted into (0001)- and (11$\bar{2}$0)-oriented 4H-SiC epilayers is identical; the compensation in (0001)- oriented samples in general exceeds that one in (11$\bar{2}$0)- oriented samples (see Fig. 1(a)). (ii) P donors can completely be activated in both types of samples up to a concentration of 10^{20} cm^{-3}. (iii) The electron Hall mobility strongly differs in (0001)/(11$\bar{2}$0)-oriented 4H-SiC epilayers (see Fig. 1(b)); its ratio at room temperature is in samples #1: µ(1(a))/µ(1(Si)) ≈ 1.3 and in samples #2: µ(2(a))/ µ(2(Si)) ≈ 2.2. The physical reasons for the observed differences in the electron Hall mobility will be discussed in the paper.

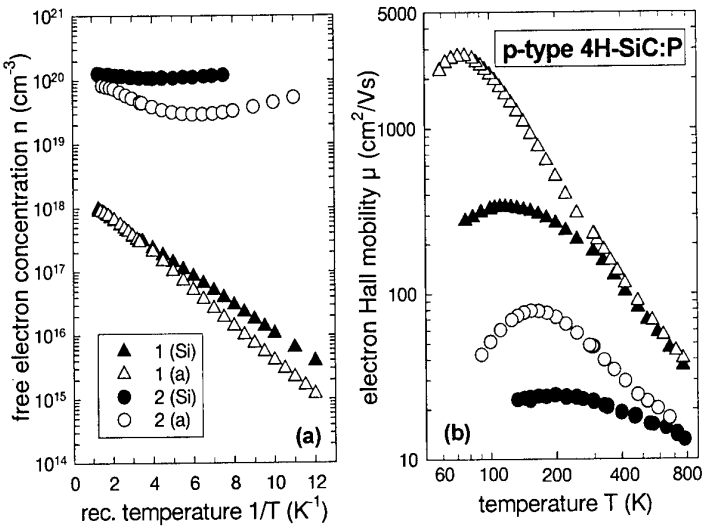


Fig.1: (a) Free electron concentration versus reciprocal temperature obtained from Hall effect investigations on P-implanted p-type 4H-SiC epilayers. (b) Hall mobility versus temperature.
Implantation:
samples 1(Si)/(a): P-box profile, depth = 1.3 µm, [P] = 10^{18} cm^{-3}, T_{impl} = room temperature.
samples 2(Si)/(a): P-box profile, depth = 0.8 µm, [P] = 10^{20} cm^{-3}. T_{impl} = 500°C.
Annealing of samples 1(Si)/(a) and 2 (Si)/(a):
T_A=1600°C, t_a=30 min.

Selective Epitaxial Growth of Pyramidal 3C-SiC on Patterned Si Substrate

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Cubic silicon carbide has been grown epitaxially on Si substrates for many years. The heteroepitaxial growth of 3C-SiC on Si has indicated the promise of high mobility devices. However, a high density of interfacial defects (misfit dislocations, voids) as well as other defects (threading dislocations, twins, stacking faults) result in the growth of lower quality material. A suitable approach towards solving this problem is the use of selective epitaxial growth on patterned silicon substrates .

Figure 1 shows the schematic of the fabrication procedure for pyramidal growth. All samples were grown by atomospheric-pressure chemical vapor deposition (APCVD) using hexamethyldisilane (HMDS). The substrates used were a (111)-oriented silicon substrates previously patterned by depositing a SiO_2 layer as the mask, followed by conventional photolithography techniques. The windows are of different shapes (square, circle, hexagonal, parallel lines) with their edges oriented mostly along the <110> directions. Thin 3C-SiC layer was grown on Si exposed through windows. After removing SiO_2 mask, patterning of the seed 3C-SiC layer was achieved by etching process to remove Si around thin 3C-SiC layer. The regrowth was carried out at the growth temperature of 1350°C. As a result of regrowth, selective growth of 3C-SiC pyramid with three facets was observed as shown in Figure 2. This approach prevents the propagation of threading dislocations originating from the 3C-SiC/Si interfaces. Therefore, lateral growth of a 3C-SiC layer until coalescence results in a 3C-SiC layer of low defect-density material. The triangular pyramids were formed on the seed 3C-SiC of different shapes (square, circle, hexagonal) without the shape of parallel lines. This indicates that the facets of each triangular pyramid do not depend on shape, wide and periodicity of the seed 3C-SiC. The air-gap was observed under the free-standing laterally grown 3C-SiC in the cross-sectional SEM.

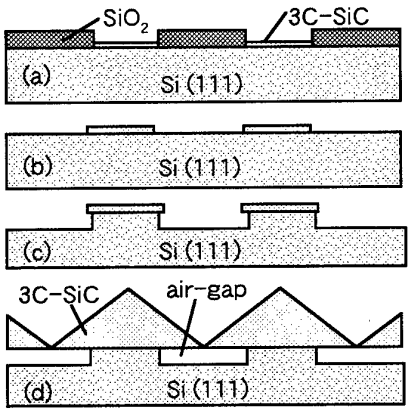


Fig. 1. Schematic of the procedure for pyramidal growth. (a) CVD of thin 3C-SiC layer at window, (b) wet etching of SiO_2 mask, (c) dry etching of Si, and (d) regrowth of 3C-SiC

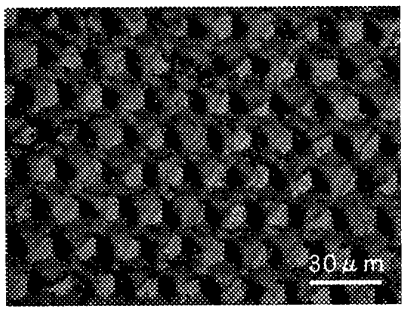


Fig. 2. Nomarski image of a triangular pyramid of 3C-SiC grown selectively by CVD.

Heteroepitaxial Growth of Defect-Free 3C-SiC on Step-Free Hexagonal (0001) SiC Mesas

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Abstract: Previous efforts to grow 3C-SiC heteroepitaxial films on Si and α-SiC substrates all yielded films containing extended defects such as double-positioning boundaries (DPB's) and/or stacking faults (SF's), leading to poor electrical performance of devices fabricated in these films. The formation of SiC mesa surfaces as large 0.2 x 0.2 mm completely free of even a single atomic step was recently reported [1]. As described in [1], these surfaces are produced on 4H- or 6H-SiC wafers (on-axis) by first dry etching trench patterns into the wafer surface to form an array of isolated growth mesas. Pure stepflow epitaxial growth, carried out under conditions that suppress 2D terrace nucleation, is then used to grow all initial surface steps on top of each mesa over to the edge of the mesa, leaving behind a top mesa surface completely free of atomic steps. However as reported in [1], mesas that initially contain screw dislocation defects cannot be flattened due to the continual spiral of new growth steps that emanate from screw dislocations during epitaxial growth.

The heteroepitaxial growth of 3C-SiC films completely free of DPB's and SF's has now been achieved at NASA Glenn on step-free 4H/6H-SiC mesas. In the absence of steps that provide a template for maintaining hexagonal substrate polytype during homoepitaxial growth, a single variant of the 3C-SiC polytype can be controllably nucleated and grown without any extended crystal defects on the step-free (0001) basal plane surface. Our experiments confirm that such defect-free growth is not possible without a step-free surface, as the presence of any steps on the nucleation surface produces disorder (i.e., extended defects) in 3C-SiC heteroepitaxial films grown thereon [2]. In particular, SF and DPB defects are observed on 3C-SiC films grown on 4H-SiC substrate mesas that could not be rendered step-free prior to 3C nucleation because they contained substrate screw dislocations. In contrast, under conditions of initial low nucleation rate on the step-free mesas, perfect 3C-SiC films (i.e., no observed defects) were reproducibly grown on mesas up to 0.4 mm by 0.4 mm in size.

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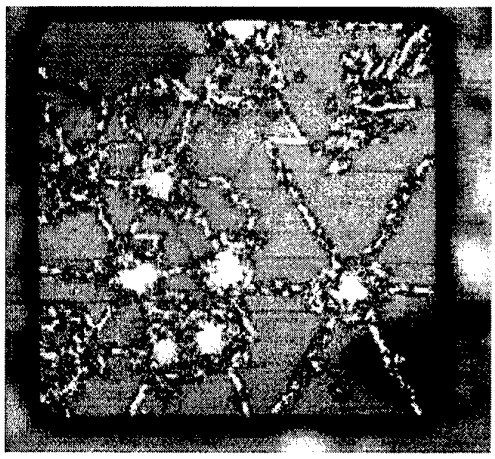


Fig. 1: Defective 3C-SiC heteroepitaxial layer with DPB's and SF's grown on a 0.2 mm x 0.2 mm 4H-SiC mesa that was not step-free because it contained screw dislocations.

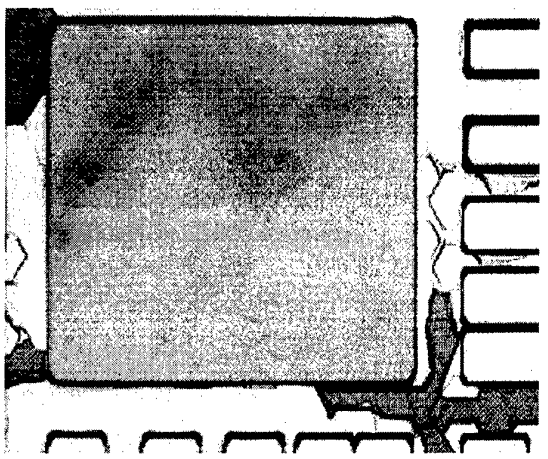


Fig. 2: 3C-SiC heteroepitaxial layer with no DPB's, and no SF's on a 0.3 mm x 0.3 mm 4H-SiC mesa. Both Fig. 1 & 2 oxidized to map polytype (dark = 3C) and defects.

AlGaN/GaN HETERO FIELD-EFFECT TRANSISTOR FOR A LARGE CURRENT OPERATION.

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GaN and related semiconductors are very promising for electric devices which can be used under high-power, high-frequency, and high-temperature conditions. Especially, it is expected that the on-state resistance of a GaN field-effect transistor (FET) is expected to be lower than that of Si or GaAs devices. However, there is no experimental report concerning the on-state resistance of a GaN-based FET. In this paper, it is reported for the first time that an AlGaN/GaN hetero FET (HFET) was operated above 20 A, and that the on-state resistance of the HFET is lower than that of a Si-based FET. A undoped $Al_{0.2}Ga_{0.8}N$(30nm)/GaN(2μm) heterostructure was grown on the sapphire substrate using a gas-source molecular beam epitaxy. The mobility of $Al_{0.2}Ga_{0.8}N$/GaN heterostructure was about 1200 cm^2/Vs at room temperature. We investigated the breakdown voltage of undoped GaN layer. The breakdown voltage of undoped GaN was over 2000 V (2 MV/cm). Before the formation of electrodes, Si-doped GaN with a carrier concentration of $5x10^{19}$ cm^{-3} was selectively grown in the source and drain regions in order to obtain a very low contact resistance.

After that, a large-size $Al_{0.2}Ga_{0.8}N$/GaN HFET was fabricated. The FET structure was formed using a dry-etching technique. The gate width was 20 cm and the gate length was 2 μm. The distance of source and drain was 6μm. The source and drain also had a multi-finger structure. The electrode materials of the source and the drain were Al/Ti/Au and the Schottky electrodes were Pt/Au. The distance between the source and drain was 6 μm. Multi-electrode structures were also fabricated using SiO_2 for isolating the source, drain, and gate electrodes, respectively. The HFET was operated at a current of over 20 A. The on-state resistance of the HFET was about 2 $m\Omega cm^2$. The transconductance (g_m) of this HFET was about 120 mS/mm. It was also confirmed that the breakdown voltage of schottky property was over 600 V. Therefore, a high power AlGaN/GaN HFET was thus demonstrated.

Comparison of 4H SiC pn, Pinch and Schottky Diodes for the 3 kV Range

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This paper investigates the static and dynamic performance of 4H SiC pn, pinch and Schottky diodes designed for 3 kV, with identical active area (1.0 mm^2) and prepared on the same wafer in order to reduce technological fluctuations. The p^+ emitters are Al implanted ($2x10^{19}$ cm^{-3}) covering the full anode area in case of the pn diode whereas patterned in 4.5 µm p^+ squares of equal distance for the pinch diode (see Fig. 1). The grid area in between these p^+ squares forms a Schottky contact (ideality 1.05). Both kinds of contacts are simply prepared with the same contact material. The Schottky diodes are equipped with or without a surrounding p^+-ring covering 20% of the anode area, respectively.

Results: All diode types block 3 kV (Fig. 2). The Schottky diodes exhibit the highest leakage current, the pn diodes the lowest. The pinch diodes are situated in between since the p regions reduce the field strength at the Schottky contact. Avalanche breakdown occurs at 3.7 kV but is overlapped by the higher leakage through the Schottky barrier in case of pinch and Schottky diodes. In context with the reverse and forward characteristics (Fig. 3) the pinch diode turns out to be the best choice:

- In normal operation (forward current $I_F \leq 2$ A) its voltage drop is less than that of the pn diode, similar to the Schottky diode and comparable to ultrafast silicon diodes. The voltage drop is hardly effected by the reduced Schottky area.
- The progressive IV characteristics even at high currents (I_F >2A) improve the pinch diode's inrush current stability. Please note the contrast to the (normal) Schottky diode without any p^+ region.
- Turn-on and turn-off experiments show the dynamic behavior to be Schottky like with very little influence of the storage charge and a recovery time of 30 ns.

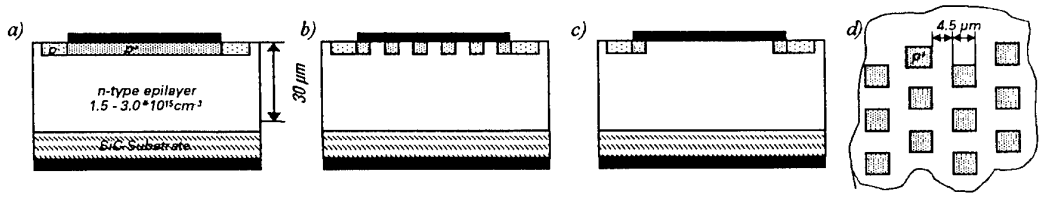


Fig. 1: Cross section of a) pn, b) pinch c) Schottky diode and d) pinch diode cell layout.

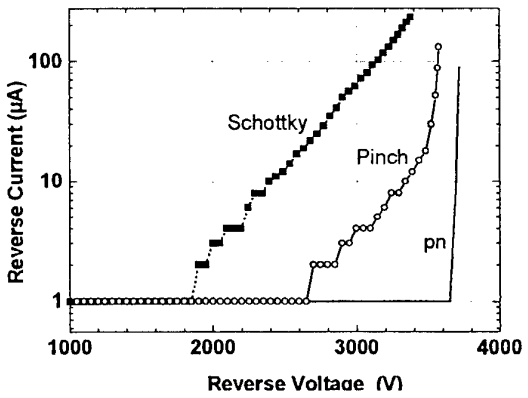


Fig. 2: Typical reverse characteristics

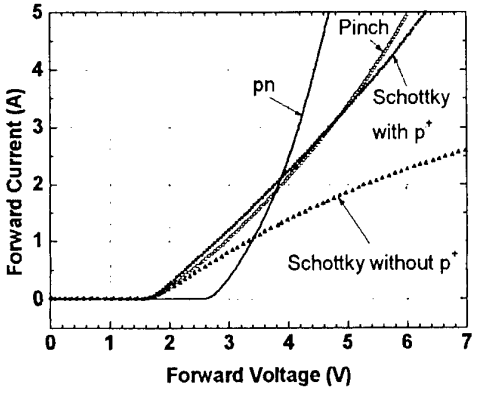


Fig. 3: Typical forward characteristics

Nanoscale Electrical Characterization of 3C-SiC Layers by Conductive Atomic Force Microscopy

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Although a great deal of work has been done on 3C-SiC epitaxial growth, high voltage device fabrication has yet to be successfully performed. We fabricated Schottky diodes on n-/n+ 3C-SiC layers grown on undulated (100) Si substrates, but obtained ohmic *I-V* characteristics. To understand the mechanism, we simultaneously carried out topography and conductivity measurement on the 3C-SiC films by using conductive atomic force microscopy (C-AFM).

The C-AFM measurements were carried out in the contact mode with a Au-coated Si_3N_4 probe, where the conductive probe serves as a nanoscale electrode. The current measurement was carried out with a forward bias of the Schottky junction applied across the sample and the probe; therefore the current image reflects the local conductivity distribution and the Schottky barrier information. Examples of simultaneously obtained topography and current images are shown in Fig. 1(a) and (b), respectively. The sample is forwardly biased at –2.2 V. The AFM topography (a) shows several faceted planes encountered at edges, with an RMS of 4.62 nm. The current image (b) shows localized distribution with highly conducting sites existed corresponding to the edges or crystalline boundaries of the topographic image, whereas other areas show almost uniform current level reflecting Schottky characteristics. It is clarified that the Schottky barrier is obtained on most area of the film, the exceptions being some ohmic leak sites due to topographic factors, crystalline defects or/and roughness.

Films with improved smoothness were also investigated and the ohmic sites decreased but leaky points still existed. It is revealed that the crystalline defects account for the highly conducting sites, which consequently caused macro ohmic characteristics. It is also proven that C-AFM is an effective tool for microscopic characterization.

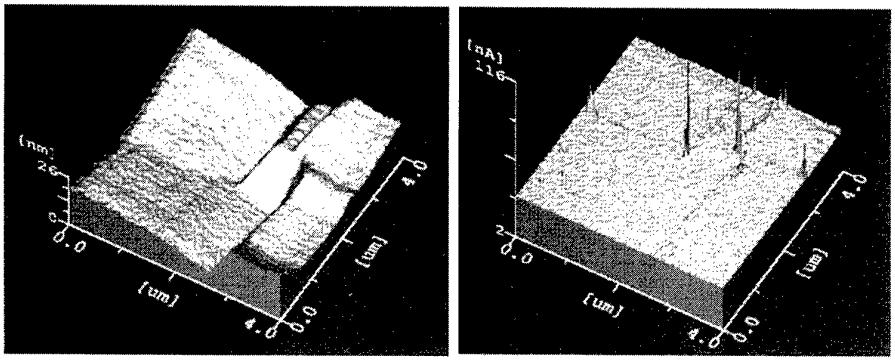


Fig.1
(a) 4 μm×4 μm, topographic image,
(b) current image,
bias V = -2.2V.

A JBS diode with surge current capability and controlled forward temperature coefficient

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The Junction Barrier Schottky (JBS) diode in SiC is a competitor to both Si PiN diodes and SiC Schottky diodes in the 600-3300V blocking voltage range. JBS diodes according to Figure 1 were processed on wafers with epitaxial layer designs for 1500-3300V. In a trade-off comparison of several designs with SiC Schottky diodes the JBS diode concept shows significant advantages in blocking voltage, blocking yield, forward temperature coefficient and surge current. These will be discussed in this contribution.

For blocking voltages up to 1700 V, negative forward voltage temperature coefficients were measured at current densities of about 100 A/cm^2 for Schottky diodes for a ΔT of 125-30 °C=95 °C (Figure 2). In this case the negative temperature dependence in the Schottky contact voltage drop dominates since the drift resistance (with an inherent positive temperature coefficient) is comparatively small (3 mOhmcm^2). For paralleling and packaging of devices a positive temperature coefficient is desired in order to have uniform current sharing. In this paper we show how the inflexion point where the temperature coefficient changes from negative to positive can be controlled in the JBS diode, thereby giving an advantage in specifying operating current density. It is the resistive contribution from the p+ grid that lowers the current density inflexion point. In Figure 3 experimental results for the inflexion points are shown for a Schottky diode in comparison with JBS diodes with different p+ grid dimensions (Schottky spacing of either 4 μm or 6 μm). The increase in

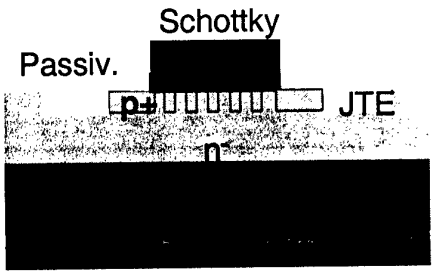


Fig. 1 Schematic cross-section of a JBS diode structure.

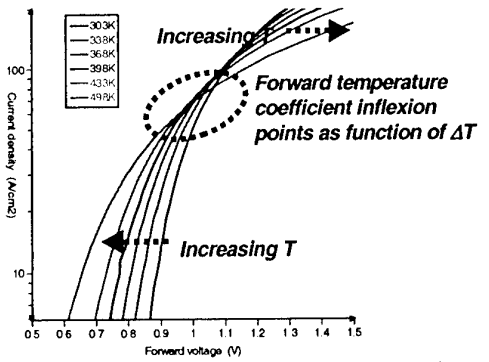


Fig. 2 Semi-log forward characteristics plot of an 1100 V Schottky diode for temperatures 303K-498K.

forward voltage due to the grid resistance is justified by the fact that higher blocking voltages are reached for the JBS diodes (1500 V compared to 1100 V for the Schottky devices on the same epi). This results in a more aggressive epi design in the JBS diode compared to the Schottky offsetting the added grid resistance. The better blocking behavior giving this lower on-state loss and the forward temperature coefficient optimization will be further discussed at the conference.

Surge current capability, i.e., that the device can sustain very high current pulses without damage, is another important issue in most diode applications. The JBS diode would show better high current characteristics than a Schottky diode if the p+ grid

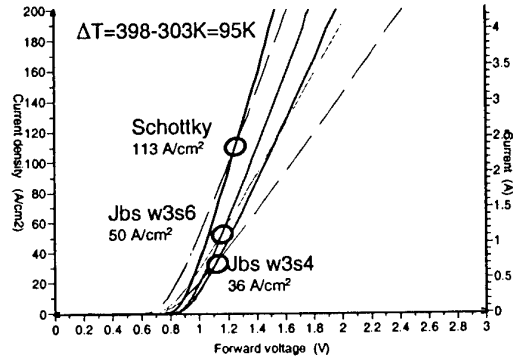


Fig. 3 Forward characteristics at 30°C (solid lines) and 125°C (dashed lines) showing the change from negative to positive temperature coefficient for a Schottky diode in comparison with two JBS designs.

Elastic and Vibrational Properties of Single-Crystal SiC as a Function of Temperature and Pressure

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We report here the first measurements of the five single-crystal elastic constants (C_{11}, C_{33}, C_{44}, C_{12} and C_{13}) for α-SiC (hexagonal, $P6_3mc$ symmetry) to 1000°C, using Brillouin light scattering technique. The results are in excellent agreement with theoretical prediction of the dC_{ij}/dT values reported by Li and Bradt (1987). The isotropic moduli and their temperature dependences, deduced from the single-crystal elastic data from Brillouin spectroscopy, are compared with the high-precision ultrasonic measurements on fully dense polycrystalline specimens of α-SiC and β-SiC (synthesized by CVD process). Except for shear moduli, the elastic moduli and their temperature derivatives for β-SiC measured to ~ 900°C, are higher than those for both single-crystal and polycrystalline specimens of α-SiC.

The pressure dependences of bulk and shear moduli of polycrystalline α and β SiC composites, determined by ultrasonic interferometry to 2 GPa, are reported. The results are in good agreement with high-pressure x-ray diffraction measurements in a diamond-anvil cell to 50 GPa. The Raman scattering measurements on 4H and 6H were made to 32 GPa. The linear positive pressure dependences of Raman shift for the TO and LO modes in the high wavenumber region (770 - 974 cm^{-1}) and corresponding mode-Grüneisen parameters, calculated from $\gamma_i = -(\partial ln\nu_i)/(\partial\ lnV)$, are in good agreement with previous studies. In contrast, the pressure dependences of the low-lying TA and LA modes in (100 - 270 cm-1 range), are mostly negative (especially for the 4H type), resulting in lower averaged values of the Grüneisen parameter (0.6). Implication of this is discussed in light of the different elastic properties and compressional behavior in the 6H and 4H polytypes.

Incorporation of Boron and the Role of Nitrogen as a Compensation Source in SiC Bulk Crystal Growth

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P-type doping during PVT growth of bulk SiC is a difficult task because of the lack of a suitable gaseous doping source. Despite recent efforts to solve this problem by applying an additional gas flow where the dopant can be introduced directly into the growth chamber [1], still the most favorable technique implies adding solid sources to the starting material. For example, adding boron carbide to the SiC powder source leads to p-type material with charge carrier concentrations p up to 10^{16} cm^{-3} [2]. This may be used for compensation with a deep donor level like vanadium to obtain semi-insulating behavior [3]. Therefore dopant incorporation homogeneity is crucial, i.e. the concentration N_A–N_D should not vary throughout the crystal.

From previous experiments it is known that nominally undoped crystals exhibit n-type behavior originating from nitrogen as residual impurity. The nitrogen content in the crystal was measured to be $N_D = 2 \times 10^{18}$ cm^{-3} at the beginning and below $N_D = 1 \times 10^{17}$ cm^{-3} at the end of growth, leading to charge carrier concentrations at 293 K as low as $n = 8 \times 10^{15}$ cm^{-3}.

Several SiC crystals were grown with different boron concentrations in the source and with different polarity of the seed. Boron is incorporated with a transfer coefficient (ratio of B content in the top of the crystal to initial B content in the source) of about 0.22 for growth on the silicon face and about 0.1 for growth on the carbon face. Chemical analysis shows that during growth the B content in the source slowly depletes, while the B content in the crystal roughly remains constant. At the end of growth, the B concentration in the source is virtually the same as in the crystal. As a result, boron incorporation is segregation-related.

The concentrations of boron acceptors and compensating donors were investigated using Hall effect measurements at 120...700 K. Solving the charge carrier neutrality equation, N_A and N_D were determined in dependence of the growth time for SiC crystals doped with B of various amounts. N_A remains constant during growth, while N_D strongly decreases. Detailed analysis shows that, especially for low compensation ($N_A/N_D \geq 10$), the onset of the freeze-out range strongly depends on N_D, which in turn leads to an almost exponential rise of the hole concentration with growth time, even though N_A–N_D remains constant.

As a conclusion, boron is incorporated homogeneously into SiC when added as a solid source, but nitrogen contamination strongly influences the charge carrier concentration below 300 K. To achieve high homogeneity of N_A–N_D, impurity control is decisive especially for low-doped growth. Finally, a decrease in the hole concentration around faceted areas, which is observed in p-type SiC growth, is found to be related to the step height on the growth surface. A model for the dopant incorporation on different step heights is proposed.

[1] T.L.Straubinger, P.J.Wellmann et al., oral presentation #72 at the conference
[2] M.Bickermann et al., Journal of Crystal Growth 233 (2001) 211
[3] M.Bickermann et al., oral presentation # 79 at the conference

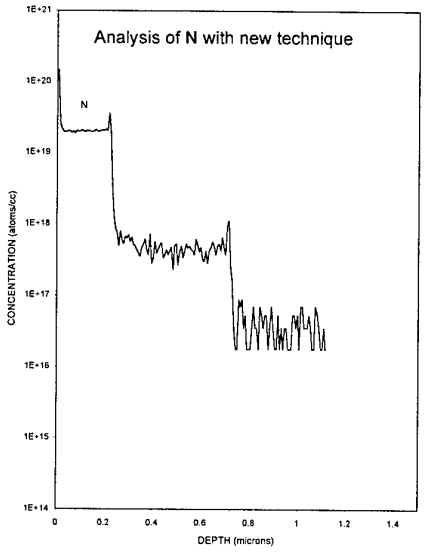
New and Improved Quantitative Characterization of SiC using SIMS

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SiC is a very important material for high-power, high-temperature, and high-radiation devices. Dramatic progress in SiC power transistors, LEDs, and sensors have made it imperative to accurately control the dopant and impurity levels. Due to its unique capabilities of high detection sensitivity for a variety of elements under depth profiling mode, Secondary Ion Mass Spectrometry (SIMS) is an essential tool for characterization of dopants and impurities in SiC material.

Over the past few years, we have made significant progress performing quantitative SIMS analysis for dopants and impurities in SiC with high sensitivity, excellent depth resolution and long term reproducibility. In this paper, we will present our development in the following areas:

(1) ***Analysis of N with much improved precision:*** A new N analysis technique was developed by monitoring atomic ions of nitrogen. This new technique provides a much improved precision and depth resolution at reasonable detection limit (see figure).



(2) ***Improvement of detection limits:*** We have modified the hardware on our commercial SIMS instruments. We are now able to achieve detection limits of 2e13 at/cm^3 for B and Al, and 1e16 at/cm^3 for N, routinely. This represents an improvement of 5 to10 over the "typical" detection limits obtained on a SIMS instrument. We have also developed a new a analytical protocol for transition metals. For example, we are able to achieve detection limit of 2e14 at/cm^3 for Fe and 5e13 at/cm^3 for Cr – a factor of 10 improvement over what can be achieved a few years ago.

(3) ***Surface contamination analysis:*** We have developed new protocols to provide accurate surface contamination measurement on SiC surfaces.

In addition, we will present the long term analysis precision studies on N, B and Al analysis. All these analyses are based on carefully prepared SiC implant standards.

Characterization of SiC Epitaxial Wafers by Photoluminescence under Deep UV Excitation

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We demonstrate that photoluminescence (PL) under deep UV light excitation is advantageous for characterizing thin epitaxial layers of *4H*- and *6H*-SiC crystals because of the short penetration depth of the light. We used the 266 nm light from a quadruple YAG laser as an excitation source. The penetration depths of the light are about 1.2 and 1.0 μm for *4H*- and *6H*-SiC crystals, respectively, which are significantly shorter than the corresponding values of 7.5 and 4.3 μm for the 325 nm light from a conventional He-Cd laser [1].

Samples were obtained from a commercial source and were heavily doped *p-on-p 4H*- and *6H*-SiC epitaxial wafers with a carrier concentration in the range of 1 x 10^{19} cm^{-3} and with an epitaxial layer thickness of about 5 μm. We performed PL spectroscopy at temperatures from 4.2 to 295 K, and PL wafer mapping at 295 K. The PL was excited by a quadruple YAG and He-Cd lasers using a back-scattering configuration.

Figure 1 shows PL spectra of a *4H*-SiC epitaxial wafer at 295 K. The spectrum (a), obtained under the 266 nm excitation from the front surface (the epitaxial layer side), represents the PL from the epitaxial layer. The near band-edge emissions at 3.20 and 3.00 eV are due to free exciton and free-to-acceptor (Al) recombination, and the 1.80 eV band has not yet been identified. Deep-level emission was below our detection limit. In contrast, the spectra (c) and (d), excited by the 325 and 266 nm light from the back surface, respectively, are the PL from the substrate. The 1.80 eV band and deep-level emission lines at 1.40, 1.12, 1.06 and 0.97 eV were observed, while no band-edge emission appeared. These deep-level emission lines have not yet been identified except for the V-related 0.97 eV line. The appearance of the band-edge emission and the disappearance of the deep-level emission in the epitaxial layer and *vice versa* in the substrate indicate the superiority of the crystalline quality of the epitaxial layer. The spectrum (b), excited by the 325 nm light from the front surface, contains both band-edge and deep-level emissions, indicating that the long penetration depth of the 325 nm light excites the substrate as well as the epitaxial layer. The 325 nm light excitation is, therefore, not suitable for the characterization of the epitaxial layer. Essentially the same results were obtained in most epitaxial 4H and 6H SiC wafers.

We performed wafer mapping of the intensity of the respective PL lines. The 1.80 eV band from the substrate shows a circular pattern, which we believe originates from the facet growth. A similar pattern was observed in the deep-level emissions. The 1.80 eV band from the epitaxial layer shows a substantially different pattern with bright spots in the central area. An opposite intensity contrast was observed in the band-edge emission. These findings suggest that the defects responsible for the 1.80 eV band in the epitaxial layer were not transferred from the substrate but were generated during the epitaxial growth.

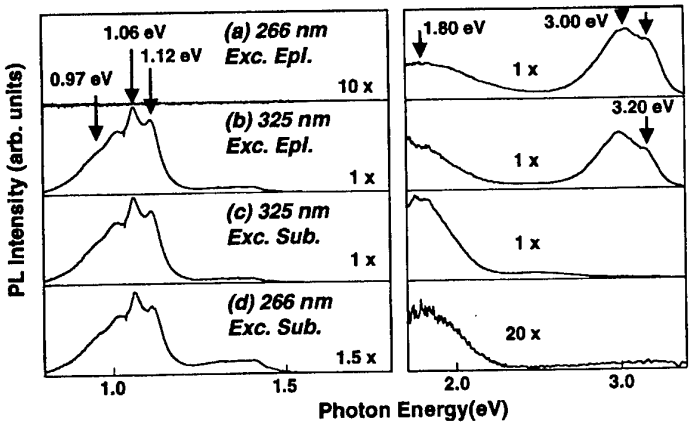


Fig. 1. PL spectra of *p-on-p 4H*-SiC epitaxial wafer at 295 K.

[1] S. G. Sridhara *et al.*: Mat. Sci. Eng. **B61-62**, 229 (1999).

Direct synthesis and growth of SiC single crystal from ultrafine particle precursor

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In the present study,we tried to grow 6H-SiC single crystals by feeding with SiC nutritious species which were synthesized on the surface of 6H-SiC seed crystals through carbothermal reduction of SiO_2 ultrafine particles by C ultrafine particles, and found that rapid epitaxial growth of the seed crystal happened.

The precursor for SiC synthesis was prepared by compounding SiO_2 and C of approximately 1 to 3 molar ratio. SiO_2 source(fumed silica) and C source(carbon black) were mixed and diluted by pure water and ball-milled with polyethylene ball and jar,for longer than 24 hours. The slurry after milling was dried and comminuted to fine particles less than 100 μm in diameter by ball-milling. The prepared precursor powder was charged on the surface of 6H-SiC seed crystal, put on the bottom of the graphite crucible with a lid.

The experiments to grow the 6H-SiC single crystal in the graphite crucible were conducted in an electric furnace with graphite heating elements, under Ar ambience of atmospheric pressure. The crucible was heated up to the target temperature of 2300°~2500°C at the ramping rate of 30°~40°C/min.and held at the top temperature for 20min.,before the start of cooling down by switching off the heater current.

The photograph of cross section of the single crystal grown at 2300°C is shown in Fig.1. About 500 μm thick layer was grown on the seed crystal of 250μm thickness. Its morphology shows a single crystal epitaxially grown on the seed crystal ,regardless of included many voids and pipes in the grown layer. Fig.2 is a cross sectional view of the single crystal grown at 2400°C. An apparent difference in number and size of visible crystal defects, exists between Fig.1 and Fig.2. The thinner grown layer of Fig.2, compared with Fig.1,implicitly shows that its surface temperature was higher than the sublimation temperature of SiC single crystal , because it had to be fed with a larger amount of SiC nutritious species, as it was grown at higher temperature than in case of Fig.1.
Based on this result we concluded that ultrafine particle precursor enabled to grow SiC single crystal at high enough temperature exceeding the sublimation temperature of seed crystal.

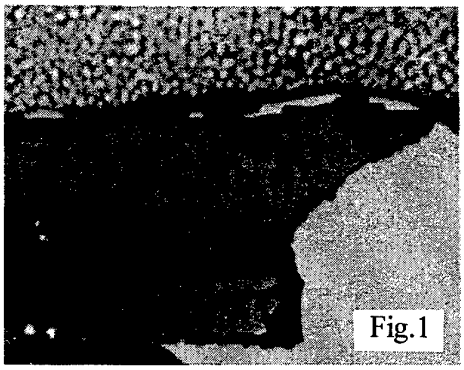
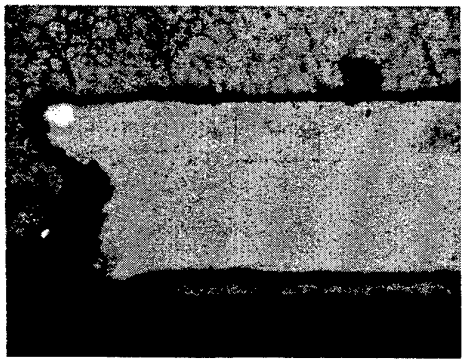


Fig.1



A

Ultrafast electron relaxation processes in SiC

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The ultrafast electron relaxation dynamics in SiC is studied by using the pump and probe transient absorption technique. It is well known that SiC has appreciable absorption band in the visible region as reported by Biedermann [1]. These absorption bands are ascribed to the inter-conduction band transition from the lowest conduction band. Instead of the valence to conduction band transition, these inter-conduction band transitions are used to probe the electrons in the lowest conduction band. The light sources employed in this experiment were a 1 kHz regenerative amplifier (Spectra Physics, Spitfire, 120 fs, 800 nm) and a tunable wavelength conversion system (SP, OPA800F). The samples used were 6H-SiC and 4H-SiC single crystals with the faces parallel to the c-axis. The electron doping levels was about 1.2×10^{18}cm^{-3} for 6H and 1.0×10^{18}cm^{-3} for 4H sample, respectively.

In 6H-SiC, the bleaching with a time constant of 1.25 ps was observed between 1.82 and 2.38 eV. The spectral profiles of this bleaching are compared with those of Bidermann bands for each polarization configurations, and this bleaching is ascribed to reflect the decrease of electron population in the lowest conduction band. The electrons in the lowest conduction band are supposed to be excited to the higher conduction band, and are speculated to relax to the lowest conduction band via inter-conduction band electron-phonon scattering, electron-electron scattering, and intra-band cooling processes. The observed relaxation time of the bleaching is concluded to reflect the inter-band scattering time [2]. In 4H-SiC, the sub-picosecond bleaching and induced absorption are also observed. Probably, this transient behavior corresponds to the shift and bleaching of Biedermann bands. We tentatively assigned the observed relaxation time to the electron-phonon scattering time in 4H-SiC.

[1] E. Biedermann, Solid State Commun. **3**, 343 (1965)
[2] T. Tomita, S. Saito, T. Suemoto, H. Harima, and S. Nakashima, Appl. Phys. Lett. **79**, 1279 (2001)

Optimized P-well profile preventing punch-through for 4H-SiC Power MOSFETs

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In order for SiC power MOSFETs to provide high breakdown voltage, punch-through that occurs in the P-well must be prevented. For that purpose, it is necessary to form a deep P-well, but that is hard to accomplish especially in SiC. Moreover, the surface concentration of the P-well should be at a low level for the channel formation. In this work an attempt was made to optimize a retrograde P-well profile. Fig. 1 shows the 4H-SiC power MOSFETs structure used. Fig. 2 shows the carrier concentration distributions of the P-well at the dashed line in Fig. 1. The carrier concentration at a depth of 0.8 μ m was high and the surface concentration was low. The optimized P-well profile was obtained by a 2-dimensional numerical simulation with *Dessis (ISE-TCAD)*. This is the first detailed analysis of a P-well profile without punch-through. Fig. 3 shows the simulation results for the reverse blocking characteristics of this device. When the peak concentration of the P-well was over 3e17 cm^{-3}, the ideal avalanche breakdown was obtained even though the P-well depth was only 0.8 μ m. This result is practical and the device can be fabricated by normal ion-implantation techniques.

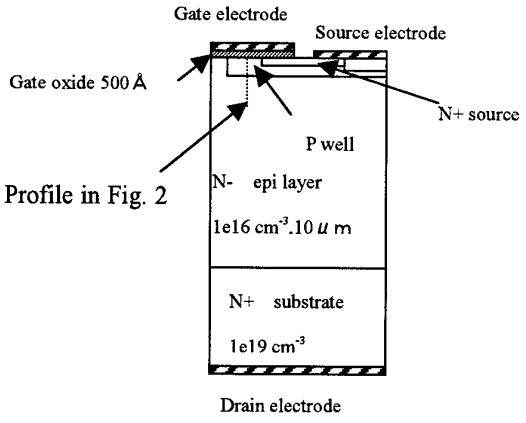


Fig. 1 Schematic cross-section of SiC-power MOSFET. Channel length=2 μ m, N-epi layer = 1e16 cm^{-3}, 10 μ m.

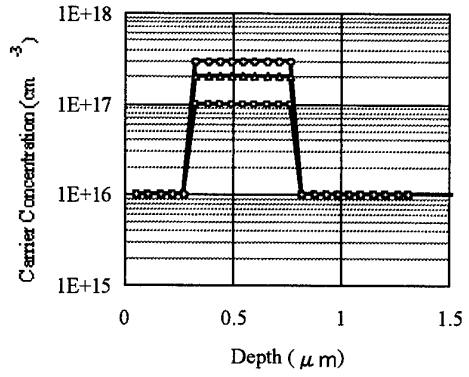


Fig. 2 P-well profile used in this wo

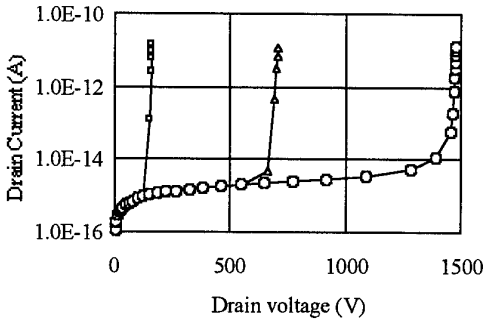


Fig. 3 Reverse blocking characteristics of SiC power MOSFETs obtained with *Dessis-ISE*. P-well peak concentrations are (□): 1e17 cm^{-3}, (△): 2e17 cm^{-3}, (○): 3e17 cm^{-3}.

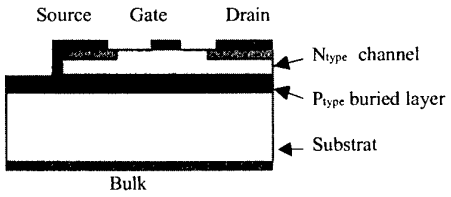
Compatibility of VJFET technology to MESFET fabrication and its interest to system integration : fabrication of 6H and 4H-SiC 110V lateral MESFET.

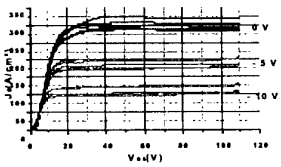
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Introduction : Integration of Power devices with their control circuitry is a usual challenge in Si and SiC technologies to increase efficiency of power switch and systems. The purpose of this article is to evaluate the integration compatibility of lateral MESFETs within a Vertical power JFET fabrication technology. The interest of this method is to allow to make control circuitry based on MESFET devices to get both power devices and control circuits on the same die. Several possibilities can be usually foreseen for the realisation of lateral SiC-MESFET [1], using conductive substrate or semi-insulated wafer. Other possibilities, more compatible with a vertical power device process, are P and N wells formation by ion implantation to form the lateral channel. The description of the fabrication process presented below is a part of the fabrication process of a VJFET designed for high voltage current limitation [2]. High energy implantation, RIE etching adjustment and metal contact annealing are the critical steps of the fabrication of this device, and will be developed, such as electrical characterization of fabricated MESFET.

Process fabrication : 6H and 4H SiC wafers with a N epitaxial layer doping concentration in the range of 5.10^{15} cm^{-3} (15µm) from Cree [INC] were used for the devices fabrication. A high energy Al implantation (2MeV, dose of $10^{14}cm^{-3}$ @400°C) has been performed to form the P buried layer. A N-type box profile was formed at the surface of the wafer by multiple N implantation ($9{,}8.10^{12}$ cm^{-2}). N was then implanted ($10^{15}cm^{-2}$) for contact zones of drain and source. The wafers were annealed at 1700°C/30min. A deep RIE etching (1,2 µm), adjusted in relation with simulated profile of Al implantation [3], was performed to contact the P buried layer. A cross section and a top picture of the fabricated MESFET is presented below.





Electrical characteristics



Picture of the fabricated MESFET

Thermal oxidation followed by an oxide deposition was realized to form the passivation layer. Ni or W layers were deposited and then annealed at different temperatures for gate and ohmic contacts. Both ohmic and Schottky contacts were simuleanously realised using one mask level for metal patterning.

Electrical characterization :

The extracted contact resitivity is in the range $4{,}6.10^{-6}$ Ω.cm² for the Ni 6H-SiC samples (annealing time: 3 min at 900°C) and $7{,}7.10^{-5}$ Ω.cm² for the 4H-SiC, values in the state of the art [4]. The PN rectifier formed between the P buried layer and the epitaxial layer (Source/Bulk) exhibits a blocking voltage around 950V @ 1.10^{-3}A/cm². The 4H-SiC MESFET specific on-resistance is 38mΩ.cm² in linear region and the transconductance is 0,4 mS.mm^{-1}. This low value is mainly due to high reverse leakage current of Schottky contact. This is the main point to improve in the next generation of devices. Two mask levels for metal deposition and patterning should be envisaged. In addition, on-state current density of 300A/cm² @ 110V in limitation mode have been reached as shown in the figure above.

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Conclusion : The full compatibility of MESFET realisation with VJFET process fabrication technology has been studied and demonstrated. The interest of high energy implantation to form deep junction is applied to the elaboration of a VJFET and lateral MESFET. Process elaboration of the MESFET will be developed, such as electrical characterization (ohmic and schottky contact study). Key points for the amelioration of the performances of the MESFET will be underlined in the final paper, as few technological adaptations will allow to improve characteristics of MESFET.

Influence of Gate Finger Width on RF Characteristics of 4H SiC MESFET

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Conventional mesa isolated SiC MESFETs with different gate finger width 100, 200, 500, 1000 μ m were fabricated on epitaxial layers grown on semi-insulating 4H-SiC substrate purchased from CREE Inc. The epitaxial layers consists of a highly doped layer, channel layer with doping density of $3.0\times10^{17}cm^{-3}$ of 0.25nm thickness and lightly doped p buffer layer. Only one gate electrode of 0.5 μ m length was drawn on each MESFETs by using electron beam lithography.

Figure 1 shows the gate finger width dependence of cutoff frequency (ft) and the maximum frequency of operation (fmax). With increasing the gate finger width, cutoff frequency rose from 4.8GHz to 11GHz. This improvement will be caused by reduction of the influence of extrinsic capacitance of MESFET on cutoff frequency. Because lager gate finger width will increase intrinsic gate-source capacitance and transconductance of MESFET, without increasing extrinsic capacitance generated by connecting pads and lines. On the other hand, the value of fmax was decreased with increasing the gate finger width. Increasing input losses due to the large gate resistance will cause this decline.

Figure 2 shows output power characteristics measured with load-pull method at 1.0GHz. Output power increased in proportion to the gate finger width. Output power over 2W can be obtained with the gate finger width of 1mm. The maximum output power density of 2.6W/mm can be obtained with the gate finger width of 200 μ m.

Acknowledgment: This work is performed under the management of FED as a part of the METI Project(R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

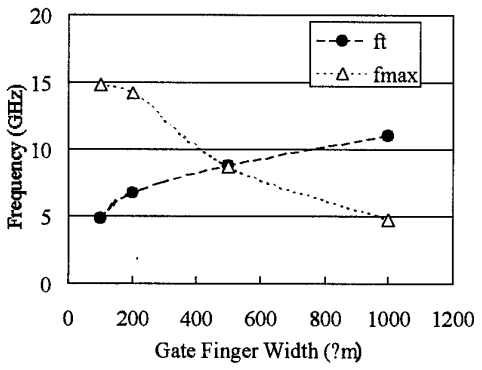


Fig.1 RF characteristics of SiC MESFET with different gate finger length.

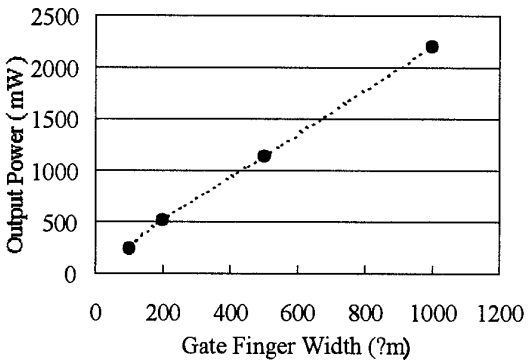


Fig.2 Output characteristics of SiC MESFET with different gate finger length.

Traveling self-confined-solvent method: A novel LPE growth of 6H-SiC

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The growth of high quality SiC without defects is an urgent target for high power device applications. The growth from liquid phase has been considered to be advantageous to improve the material quality due to the process under thermal equilibrium. In the case of SiC, however, the lack of stoichiometric liquid phase has restricted the choice of proper solvents to Si, which allows only a small solubility of C [1,2]. Thus the use of Si-solvent requires extremely high processing temperature to reach high growth rate, which induces thermal instabilities.

In this study, we propose a novel liquid phase epitaxial growth of 6H-SiC(0001) employing a new sandwich configuration with no temperature gradient. It consists of a polycrystalline SiC source platelet and a seed substrate with the 20um thick extremely thin Si-solvent layer in-between, which is formed by the self-penetration of surrounding Si liquid at temperatures above 1450C. The use of this particular thickness of the Si-solvent layer guarantees the stable growth of SiC up to 2300C, without being obstructed by thermal instabilities including thermal convection. As a result, a 300um-thick 6H-SiC single crystal of single domain was successively grown in 30 min at 2300℃ (Fig.1). The structural and optical properties of the grown layer were characterized by optical microscopy, AFM, X-ray topography, TEM, and cathode luminescence.

It is revealed that the growth front preserves smooth surface with an atomically flat terrace of 50um width terminated by a few nanometers height bunched step. This is a clear evidence showing the reduction in the thermal instabilities. The growth mechanism is directly attributed to the difference in surface energy between the substrate and the source resulting in the difference in the equilibrium concentration of C.

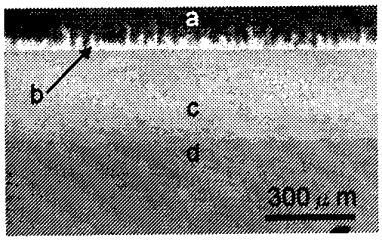


Fig. 1. Cross sectional view of grown layer. a : substrate, b : grown layer, c : Si layer, d : polycrystalline plate.

[1] D. H. Hofmann, M. H. Muller, Mater. Sci. Eng. B 61-62 (1992) 29
[2] A. E. Nikoleav, V. A. Ivantsov, S. V. Rendakova, M. N. Blashenkov, V. A. Dmitriev, J. Crystal Grpwth 166 (1996) 607

Optical and electrical characterization of free standing 3C-SiC films grown on undulant 6-inch Si substrates

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Recently, Nagasawa *et al.* of the HOYA R&D Center. Japan have announced successful CVD growth of high quality 3C-SiC films of up to a few hundred micron thick with a very small density of defects (10 /cm^{-2}) [1]. The new 3C-SiC epilayers have been grown on so-called undulant Si(001) wafers of 6-inch in diameter by CVD method to have planar defects collide and cancel out each other within the first ~50 μm from the Si/SiC hetero interfaces. Defects present in the region more than 50 μm away from the interface are dominantly twin boundary planes being parallel to each other with approximate separation distances of 3 μm.

In this work we report on the electrical and optical characterization of the free standing 3C-SiC made by the HOYA R&D Center. Two series of samples have been studied; nominally undoped samples and intentionally nitrogen doped samples of the concentration 10^{18} and 10^{17} cm^{-3}, respectively.

The electrical properties have been investigated by variable temperature Hall effect measurements for the temperature range T=10-400K. The large improvement in the low temperature free carrier mobility has been observed when the near interface heavily defected region has been lapped away.

The optical properties have been investigated by photoluminescence (PL) spectroscopy at T=3-300K. The PL spectrum at 3K shows sharp features of nitrogen donor bound excitons. Above 50K, broad peaks due to the free exciton recombination were observed for undoped sample (Fig.1) indicating a high quality of the sample. The free exciton luminescence, which is a good measure of the quality of the sample, has been observed before for homoepitaxially grown 3C-SiC [2] but never in as grown samples. Our result is remarkable considering the fact that the film has been hetero-epitaxially grown directly on Si with the growth speed of 50 μm/hour.

We would like to thank H. Nagasawa of the HOYA R&D Center for kindly providing us the samples and K. Kojima for helpful discussions.

[1] Hiroyuki Nagasawa *et al.*,
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[2] Katsushi Nishino *et al.*,
Jap. J. Appl. Phys. Vol. 36 (1997)
pp. 6405-6410

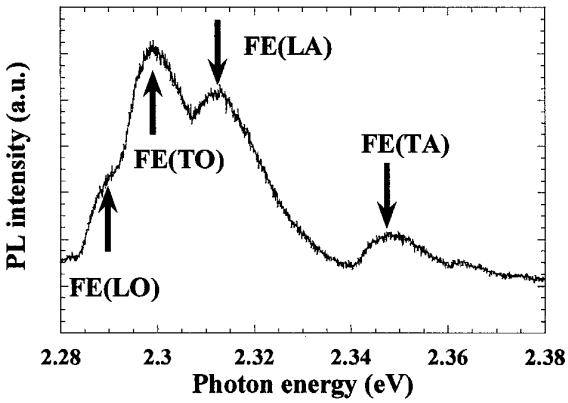


Fig.1 Free exciton luminescence of nominally undoped 3C-SiC at 80K

Study on Metamorphosing Top Si Layer of SOI Wafer into 3C-SiC Using Conventional Electric Furnace

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Based on Silicon-on-Insulator (SOI) technology, we have a plan to develop electron-photon-merged devices. This plan calls for CMOS-LSI/SOI and LED-array/GaN to be monolithically fabricated on one chip. In order to reduce the lattice mismatch between Si and GaN, we are attempting to form a GaN/SiC/SOI structure. We are using a conventional electric furnace, without any vacuum system, to metamorphose the top Si(111) layer of the SOI substrate into 3C-SiC(111) under the atmospheric pressure of propane gas in hydrogen at about 1250℃. This method of forming a SiC-on-Insulator (SiC-OI) substrate is inexpensive and makes it easy to enlarge the wafer size. In addition, the SiC-OI substrate can be applied not only to SiC devices but also to extensive substrate materials of GaN devices.

Figures 1(a) and (b) show the surface morphologies of specimens after carbonizing the top Si layers of SOI substrates, measured with a laser microscope. Figure 1(a) corresponds to an image of carbonization in hydrogen and propane after temperature elevation to about 1250℃ under a pure hydrogen ambient, while (b) corresponds to an image of carbonization by temperature elevation to about 1250℃ under a hydrogen and propane ambient. The surface micro-roughness of specimen (b) is greatly reduced compared to that of specimen (a). It is supposed that, in the case of (a), the bare Si layer reacts with such impurities as water in the hydrogen gas during the temperature elevation, leading to the increased surface micro-roughness of the specimen. In the case of (b), in contrast, the SiC layer is gradually formed at lower temperatures, which prevents impurities from reacting with the Si layer. For both specimens, however, 3C-SiC(111) peaks ($2\theta = 35.6^\circ$, Cu-kα) are clearly observed from X-ray diffraction measurements. This finding indicates that the formed SiC layers have good crystallinity.

Figure 2 shows a cross-sectional TEM image of the specimen in 1(b). The Si surface of the SOI wafer is metamorphosed into 3C-SiC(111) with the thickness of 3nm. We can therefore expect the whole 100 nm top Si layer of the SOI substrate to be metamorphosed into a uniform SiC layer by optimizing the reaction time, flow rates of gases, and so on.

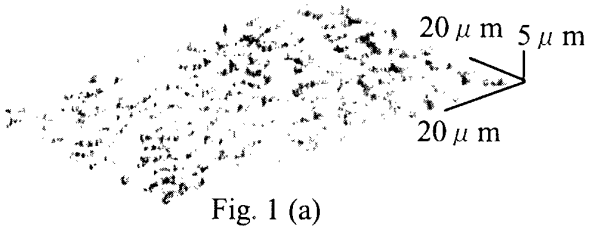


Fig. 1 (a)

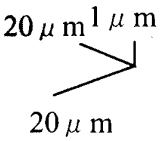


Fig.1 (b)

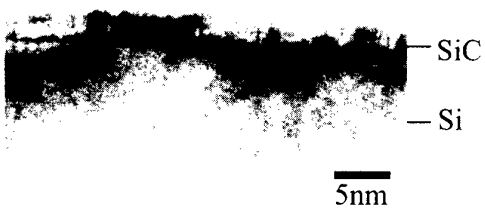


Fig.2

Radiation response of 6H-SiC MOSFETs fabricated using pyrogenic condition

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Electron-hole pairs are liberated in the silicon dioxide when exposed to ionising radiation. Subsequently most of the initially generated electron-hole pairs recombined, a fraction of them remains in the oxide layer. Under favourable biased conditions, the electrons are swept out of the oxide and the positively charged holes are trapped within the oxide and near the interface of the SiO_2/SiC system. These trapped holes degrade the channel mobility of MOSFET and pose oxide reliability issue. For this reason, many studies on the radiation effects on Si MOSFETs have been performed. Few works show the effects of gamma irradiation on SiC MOSFETs. In this paper, we present new electrical response of p-channel MOSFETs when exposed to gamma ray irradiation. Our results are also compared to the irradiated n-channel 6H-SiC and Si devices. The oxides are grown using pyrogenic condition and irradiated at zero applied bias to all the electrodes.

Fig. 1 shows the shift of the threshold voltage of the irradiated devices. The n-channel threshold voltage decreases initially due to the builtup of positive oxide trapped charge. Above 10^5Gy(SiO_2), the threshold voltage rebounds. In the case of the p-channel, both the formation of oxide trapped charge and interface traps are positively charged, and contributed to the large negative voltage shift. Fig. 2 depicts the normalised mobility as a function of absorbed dose for both the n-channel and p-channel devices. Interestingly, the initial mobility of the p-channel devices increase up to 1.3 times of its pre-radiation value before decrease on further irradiation. This increase in the hole mobility is attributed to the passivation of the interface states and reduces the scattering of the channel holes. Further irradiation results in an increase in the oxide and interface charge traps, and therefore reduces the hole mobility. At low irradiation doses, the mobility of the Si MOSFET has reduced substantially. Unlike the Si device, the electron mobility of the n-channel SiC device remains unchanged up to a dose of 3×10^5Gy(SiO_2). All these influences of gamma irradiation on the devices and device fabrication steps will be given in details in the paper.

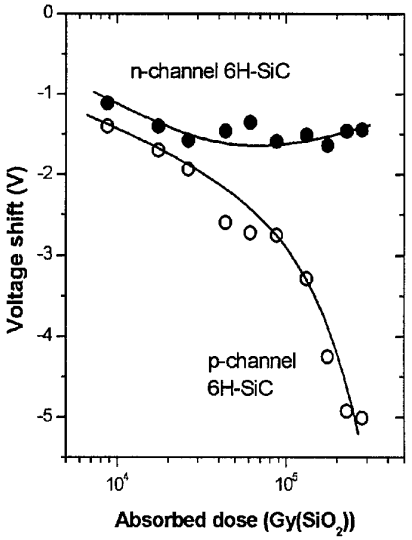


Fig. 1 The threshold voltage shift of n-channel and p-channel devices as a function of absorbed dose.

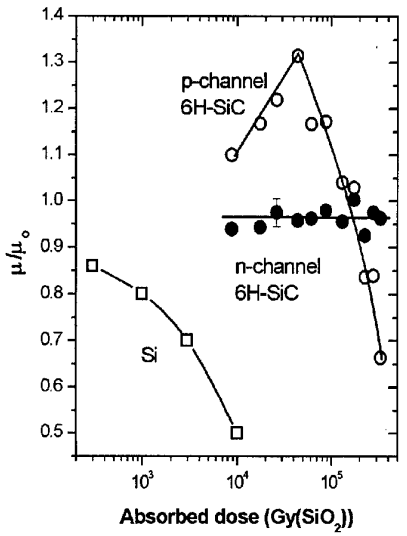


Fig. 2 The normalised mobility of the Si and SiC MOSFETs as a function of absorbed dose.

Abstract

submitted to the International Conference on Silicon Carbide and Related Materials 2001

October 28 - November 2, 2001

Tsukuba International Congress Center (Epochal Tsukuba)in Tsukuba, Ibaraki, Japan

Electrical properties of 4H-SiC thin films reactively ion-etched in SF_6/O_2 plasmas

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Effects of dry etching process on the electrical properties of 4H-SiC were investigated. Au Schottky barrier diodes(SBD's) were fabricated on the reactively ion-etched surface of 4H-SiC thin films. The surface roughness, residues and defects, which were produced during dry etching could deteriorate the electrical properties of Schottky diodes. Such harmful effects were determined by current-voltage(I-V) and capacitance-voltage(C-V) measurements. The Auger electron spectroscopy(AES) was also performed to reveal the species of residues on the etched surface after RIE process. The surface roughness before and after etching process was evaluated by the atomic force microscopy(AFM).

The I-V characteristics of SBD's on the etched surface were found to be deteriorated compared with that of the SBD's on the unetched surface from the measurement of Schottky barrier height, ideality factor and reverse leakage current. However, an increase of oxygen content in gas mixtures made an improvement in the performance of Schottky diodes. It might be ascribed to the faster removal of carbon-excess surface layers with etching-induced damage and the smoother etched surface. The RMS roughness of etched surface with AFM scan area of 5×5 μm^2 was actually improved from 8.5 Å to 5.7 Å with an increase of the oxygen content in the reactant gases form 0% to 50%. And the AES analysis revealed that the RIE etched surfaces had the residual contaminants, of which the species were fluorine and oxygen, regardless of etching conditions. These results indicate that the SBD's fabricated with higher oxygen percentage in the etchant gases had better device performance than that with lower oxygen contents in spite of residual contaminants on the surface.

Acknowledgement

This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea.

Keyword : Reactive ion etching, Schottky barrier diode, Etching-induced damage

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Influence of Excited States of Deep Acceptors on Hole Concentration in SiC

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Experimental acceptor levels ΔE_A in SiC, measured from the valence band E_V, are reported to be deeper than 150 meV. Moreover, the ground and first excited state levels of acceptors in SiC, calculated by hydrogenic acceptor [$\Delta E_r = 13.6(m^*/\varepsilon_s^2 r^2)$ eV], are 136 meV and 34 meV, respectively. The experimental ΔE_A is deeper than ΔE_1 because of central cell corrections, while ΔE_r $(r \geq 2)$ are considered to be reasonable, and should affect the hole concentration $p(T)$. Using three kinds of distribution functions, we theoretically and experimentally investigate the influence of the excited states on $p(T)$.

The proposed distribution function for electrons is expressed as

$$f\left(\Delta E_A, n, \overline{E_{ex}}\right) = \frac{1}{1+4\exp\left(-\frac{\overline{E_{ex}}}{kT}\right)\cdot\left\{g_1\exp\left(\frac{\Delta E_A-\Delta E_F}{kT}\right)+\sum_{r=2}^{n} g_r\exp\left(\frac{\Delta E_r-\Delta E_F}{kT}\right)\right\}}, \quad (1)$$

where ΔE_F is the Fermi level measured from E_V, g_r is the $(r-1)$-th excited state degeneracy factor, and n is the highest excited state, which we consider in analysis. Here, the average acceptor level $\overline{\Delta E_A}$ is expressed as $\overline{\Delta E_A} = \Delta E_A - \overline{E_{ex}}$, and $\overline{E_{ex}}$ is the ensemble average of the ground and excited state levels, which increases with T. The Fermi-Dirac distribution function corresponds to $f(\Delta E_A,1,0)$ and the conventional function is $f(\Delta E_A,n,0)$.

Using p-type 6H-SiC wafer, $p(T)$ was obtained by Hall-effect measurements. Using Free Carrier Concentration Spectroscopy (FCCS), ΔE_A, the acceptor density N_A and the compensating density N_{com} were determined, and are shown in Table 1. Figure 1 shows the $p(T)-1/T$ curves, and Fig. 2 displays the FCCS curve given by $H(T,E_{ref}) \equiv p(T)^2\exp(E_{ref}/kT)/(kT)^{5/2}$, where the simulation results mean the curves simulated using Table 1.

In $f(\Delta E_A,1,0)$, although the simulated $p(T)$ is in agreement with the experimental $p(T)$, the simulated $H(T,E_{ref})$ is not, indicating that the excited states should affect $p(T)$. In $f(\Delta E_A,n,0)$, the density of holes bound to acceptors increases, which results in the unreasonable high N_A. In our case, there are good coincidences between the experimental data and simulation results in Fig. 1 as well as in Fig. 2, and N_A and ΔE_A are considered to be reasonable.

In summary, the influence of the excited states on $p(T)$ should be considered, and the distribution function used in deep acceptors should be $f(\Delta E_A, n, \overline{E_{ex}})$.

Table 1 Results determined by FCCS

	$f(\Delta E_A,1,0)$	$f(\Delta E_A,10,0)$	$f(\Delta E_A,10,\overline{E_{ex}})$
N_A [cm^{-3}]	2.95×10^{19}	2.19×10^{20}	1.91×10^{18}
ΔE_A [meV]	182	205	189
N_{com} [cm^{-3}]	8.35×10^{17}	2.65×10^{18}	3.37×10^{16}

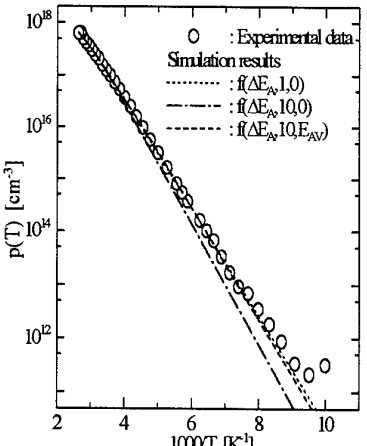


Fig. 1 Experimental and simulation results of p(T)

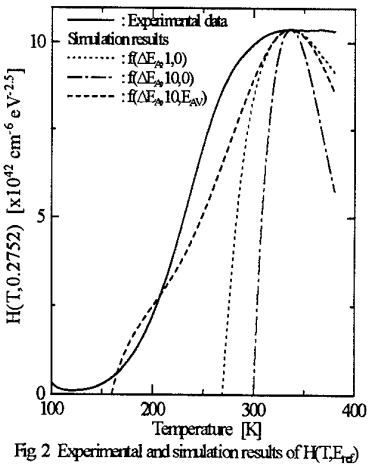


Fig. 2 Experimental and simulation results of $H(T,E_{ref})$

ALUMINIUM NITRIDE BULK CRYSTALS BY SUBLIMATION METHOD: GROWTH AND X-RAY CHARACTERIZATION

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Aluminium nitride AlN, a wide band gap material isomorphous to gallium nitride has good dielectric properties and chemical stability up to 1400°C. Despite of not enough maximum size of AlN single crystals reported so far the bulk crystals and thick epitaxial layers of aluminium nitride have a great potential as the substrate materials for GaN-based epitaxial structures.

Here, aluminium nitride crystals have been grown by sublimation technique in the conventional growth cell designed earlier for obtaining silicon carbide ingots by modified Lely (LETI) method of growth. High purity AlN powder was used as a source, a number of materials (SiC platelets, AlN/Al_2O_3 epitaxial structures, polycrystalline and textured Ta, W, C) serve as the substrates. Deposits were prepared at 1400..2100°C and reduced pressure of gas ambient ($Ar+N_2$) for 1..10 h. Conventional X-ray diffraction methods (mainly, double-crystal diffractometry and Laue pattern technique) have been employed to characterize the structure and phase composition of deposits. To prevent an effect of catalythic reduction of aluminium nitride onto the surface of graphite fittings in accordance with the reaction:

$$AlN(s) _ AlN(g) _ Al(g) + N2(g)$$

an additional foil insulation was placed into the growth cell.

We usually observe there are no any deposits onto the graphite substrate due to the reduction mechanism mentioned above. Unexpectedly, the formation of homogeneous AlN crystalline deposits onto the single crystalline SiC substrates is also hard to achieve. The samples grown at 1500..2000°C in both the vacuum and residual gas ambient were as a rule multiphase and contain both aluminium nitride and complex carbides such as Al_4SiC_4 and $Al_4Si_2C_5$. This effect probably being a result of surface graphitization of silicon carbide at the growth temperatures is also responsible for relatively small growth rates observed for SiC substrates.

Singlecrystalline growth has been achieved onto AlN/Al_2O_3 epitaxial structures at the temperatures less than 1800°C. X-ray diffraction showed that the deposits with the thickness of up to some millimeters grown onto the substrate of up to 1 inch in diameter had obvious for aluminium nitride wurtzite structure. From the practical point of view, the major problem consists in the intensive nitridation of corundum part of epitaxial structure at the high temperatures of growth leading to its cracking and even to mechanical destruction. So, corundum substrate exposed at the 1600°C for 4 hours almost completely converts into the set of oxynitrides. Nevertheless, thick corundum substrates (more than 1000 _m) with the thick epitaxial layers appear to be successfully used as the initial seed of large-scale area for AlN growth in conventional sublimation process.

Also, large-grain homogeneous textured deposits were prepared onto the metal substrates such as tantalum and tungsten. The deposits were found to be only wurtzite phase with the lattice parameters agreed with the tabulated those.

Electronic structure of the UD3 defect in 4H and 6H SiC

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For SiC device applications it is highly desirable to achieve semi-insulating substrate material. Recently it became possible to grow bulk semi-insulating SiC by the HTCVD technique. The semi-insulating behaviour is probably due to one or several deep level defects, but a definite identification of these defects has not been possible so far. However, a series of sharp photoluminescence (PL) lines in the near infrared region is often found in such samples. These lines have been labelled UD1, UD2 and UD3, and the corresponding defects are likely candidates for the semi-insulating behaviour.

The aim of this work is to provide detailed insight into the electronic structure of the ground state and the lowest lying excited states of the UD3 defect. This is achieved by a combination of PL-, PL excitation- (PLE), polarization- and Zeeman-experiments. The UD3 defect gives rise to a no-phonon (NP) PL line at low temperatures at an energy of 1.3555 eV in 4H SiC and 1.3430 eV in 6H SiC. In a magnetic field UD3 in both polytypes splits into two lines. The magnitude of this splitting is strongly angular dependent: It is largest when the magnetic field is oriented parallel to the c-axis of the crystal and basically disappears for a magnetic field orientation perpendicular to the c-axis. The splitting is observable in both PL- and PLE-experiments. In PL however there is a thermal redistribution of intensity as the temperature is varied, whereas the two lines have identical intensity at all temperatures in PLE.

At zero magnetic field the lines are completely polarized $\vec{E} \perp$c-axis.

In PLE experiments additional lines at a few meV above UD3 are found in the 4H polytype. The ones closest to the UD3 line are almost as sharp as UD3 itself and are attributed to transitions between the ground state and additional excited states with higher energies. Additional evidence for this is provided by the fact that the lowest lying additional lines can even be found in PL experiments at elevated temperatures when the corresponding levels are thermally populated.

The experimental findings can be consistently explained assuming the following electronic structure: The ground state is an orbital and spin singlet $^1A_1$. Above that there is an orbital doublet $^1E_2$. The transition between these gives rise to UD3. The g-value of $^1E_2$-states is typically highly anisotropic, which explains the strong angular dependence of the Zeeman splitting. In addition only transitions with $\vec{E} \perp$c-axis are allowed between A_1 and E_2 states. At energies above the E_2 state at least two additional singlet states have been found.

Possible candidates of the defect will be discussed based on the experimental findings.

Fabrication of 4H-SiC planar MESFETs having low contact resistance

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2) R&D Association for Future Electron Devices, Advanced Power Device Laboratory

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4H-SiC MESFETs were fabricated using high-density ion implantation to get low ohmic contact resistance without recess gate etching and contact annealing. The superior physical properties make SiC a very promising material for high power and high frequency devices especially for microwave power MESFETs. SiC MESFETs have typically had a recess-etched structure of gate active layer with a high-doped epitaxial layer for source and drain ohmic contact. The dry etching, however, leads to the degradation of device performance with the inferior gate Schottky characteristics due to the induced plasma damage in the near-surface region. Moreover, the inter-diffusion and the reaction between metal and SiC during contact annealing causes various problems such as the remaining-carbon. The ohmic contact resistance is somewhat high in the order of $10^{-4} \sim 10^{-5}\ \Omega cm^2$ because the doping concentration of high-doped layer of about $10^{19} cm^{-3}$ is not sufficient for the field-emission tunneling.

The fabrication process included mesa etching, P^+ ion implantation and activation, formation of ohmic contacts, definition of gate contact and formation of pad. The structure of wafer from Cree Inc. consisted of n-type substrate, p-type buffer layer ($N_A=9.0\times10^{15}\ cm^{-3}$) and n-type channel layer having a thickness of 0.4 μm ($N_D=1.7\times10^{17}\ cm^{-3}$) (Fig. 1). The gate length was from 2 μm to 10 μm and the gate width was 100 μm and 500 μm. Ohmic contacts were formed using Al without annealing, which means after the activation annealing of ion implantation, all processes were run at room temperature.

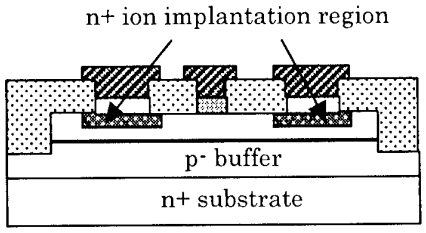


Fig. 1. Cross-sectional view of MESFET

Fig. 2 shows the Ids-Vds characteristics of a fabricated MESFET. The pinch-off voltage, the saturation drain current and the transconductance were 30 V, 415 mA/mm, and 19.3 mS/mm, respectively. Very low contact resistance of $4.8\times10^{-6}\ \Omega cm^2$ was estimated from TLM measurement, which indicate the non-annealed Al ohmic contact can be applied for the device fabrication.

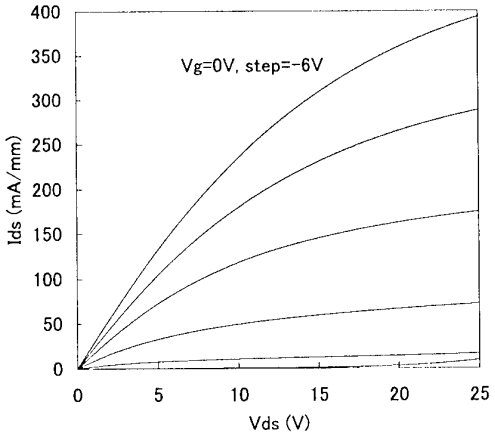


Fig. 2. DC characteristics of MESFET with 2μm gate length and 500μm gate width

Homoepitaxial growth of 4H-SiC thin film below 1000°C by microwave plasma chemical vapor deposition

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High temperature (around 1500°C) of homoepitaxial SiC film growth limits the variety of the SiC device process. Our goal is to achieve high-quality homoepitaxial α-SiC film growth below 1000°C by microwave plasma chemical vapor deposition (μPCVD) for the purpose of providing more flexibility in the SiC device process, such as epitaxial growth using SiC on insulator (SiCOI) substrates, selective epitaxial growth by use of oxide or nitride mask and so on. To our knowledge, there are no papers reporting about homoepitaxial growth of α-SiC using PCVD.

SiC films were grown on 8° off-axis 4H-SiC(0001) substrates at temperature of 970°C and microwave power of 1300W without intentional doping. Mixture source gases of CH_4 and SiH_4 were used with H_2 carrier gas. The surface morphology and crystallinity of the obtained films was characterized by atomic force microscopy (AFM) and reflection high-energy electron diffraction (RHEED), respectively. The C/Si ratio was a very important factor for fabrication of high-quality films. Extremely high C/Si ratio (C/Si=175) in comparison with that used in conventional CVD technique was required to obtain smooth and single crystalline films.

The polytype of obtained films was confirmed by confocal microprobe Raman scattering spectroscopy. Figure 1 shows the Raman scattering spectra from the ~200nm thickness SiC film grown at C/Si ratio of 175 for 10h. By focusing probe laser at surface and substrate, we distinguished the signals from the grown film and the substrate. It is known that the LO phonon-plasmon coupled (LOPC) peak becomes broader and shifts to higher frequency with increasing the free carrier density n [1]. Since the substrate was highly doped n-type 4H-SiC, the Raman line of LOPC mode was very broad as shown in Fig. 1 (a). On the other hand, in a spectrum from the film surface (Fig. 1 (b)), a sharp line ($964cm^{-1}$) corresponding to the LO mode of pure 4H-SiC was observed with the broad LOPC line from the substrate. These results indicate that homoepitaxial growth of 4H-SiC have been attained below 1000°C.

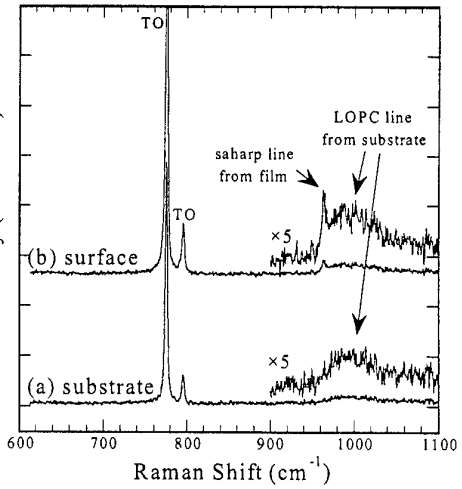


Fig. 1 Raman scattering spectra

[1] S. Nakashima *et al.*, Phys. Stat. Sol. (a) **162**, 39 (1997)

Reduced micropipe density in boule-derived 6H-SiC substrates via H etching of seed crystals

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The effect of hydrogen etching of 6H-SiC Si(0001) on-axis SiC seed surfaces prior to crystal growth has been investigated. The most common method for producing SiC substrate wafers is to place a SiC seed in a closed graphite container and then deposit SiC vapor species onto the seed from a heated SiC source. Four quarters of the 2" seed were prepared for boule growth with each quarter prepared using various treatments. A photograph of the seeds investigated is shown in Fig. 1 (left) along with the resulting substrates (right). Hydrogen etching of the seeds was performed for 30 min. at 1600°C in a cold-wall CVD reactor to reduce seed crystal surface and subsurface damage. Boule growth was then conducted in an inductively heated PVT furnace and the boule sliced into wafers and polished. The micropipe density (MPD) was then measured using differential interference optical microscopy. For a conservative analysis the MPD for each wafer quarter were averaged and a statistical analysis performed to ensure independent samples. Using a 95% confidence criteria hydrogen etching of the seed appeared to reduce the MPD in the crystal by about 24.5 $\pm$ 19.4%. Fig. 2 is a histogram of the MPD for seeds etched with hydrogen and non-hydrogen etched.

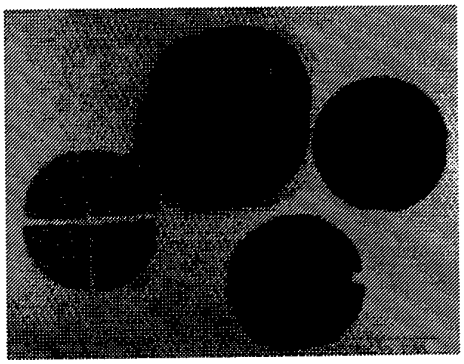


Fig. 1 Photo of tiled seeds (left) and resulting boule-derived substrates (right). 4 boules prepared in this study.

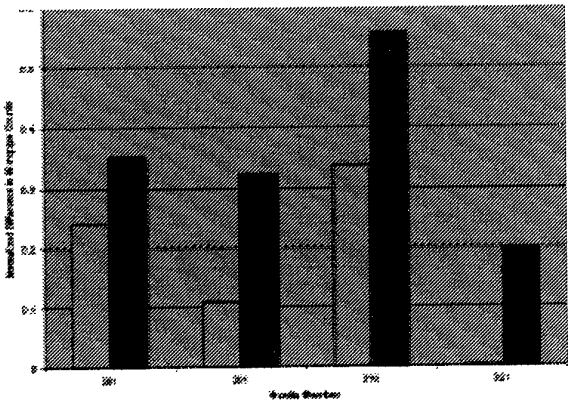


Fig. 2 MPD in boules grown using H-etched (light) and non-etched (dark) seed crystals. MPD reduced by ~ 25% with H etching.

X-ray photoelectron spectroscopy studies of post oxidation process effects on oxide/ SiC interfaces

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SiC-MOSFETs have some problems to be solved before practical use, such as their low channel mobilities and higher on-resistances than those predicted. It has been reported[1] that high interface trap density and high oxide-trapped charges of SiC MOS structures, which are estimated by *C-V* measurements, are concerned with the inferior properties of SiC MOSFETs. Also, it has been reported that some post oxidation processes, such as re-oxidation[2], have improved their *C-V* characteristics. We have reported that,[3] in the results of XPS measurements for slope shaped oxide films, several photoemission peaks corresponding to other bonding states than Si-C and Si-O bonds were observed in the oxide/SiC interfaces. In this report, we try to explore the changes of interfacial structures by post oxidation processes in terms of bonding states. We also reveal the reasons for the improvement of *C-V* characteristics by these processes.

6H-SiC homo-epilayers, 5 μm in thickness and 5 × 10^{15} cm^{-3} in carrier concentration (n-type) (Cree,Inc.), were used for the measurements. The (0001) Si faces of SiC epilayers were oxidized in a pure O_2 flow at 1100 ^{0}C for 3h. After the oxidation ceased, one of the samples was cooled down immediately ((a) quench), another one was post-oxidation-annealed in Ar gas atmosphere at 1150 ^{0}C for 3h ((b) Ar POA), and the last one was re-oxided at 950 ^{0}C for 3h ((c) Re-oxi.) The three specimens were immersed gradually into buffered hydrofluoric acid at a constant speed to etch the oxide layers at an angle. The measuring point (1 mm in diameter) of XPS was scanned along the slope of the samples. Figure 1 shows the photoelectron spectra of C1s core levels as a function of oxide thickness. It was found that the number of C-O bonds and C$^-$ bonds decrease with Ar POA and wet re-oxidation, respectively. C$^-$ bonds are probably originated from a dissociation of C-Si bond. We also discuss the influence of C$^-$ bonds and C-O bonds, in addition Si-Si bonds and Si-O-C bonds observed in Si2p, with respect to the electric properties of MOSFETs.

This work was partly performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

[1] V. V. Afanas'ev et al.: Phys. Status Solidi (a) **162** (1997) 312.
[2] L. A. Lipkin and J. W. Palmour: J. Electron. Mater. **25** (1996) 909.
[3] Y. Hijikata et al.: Appl. Surf. Sci. (in press.)

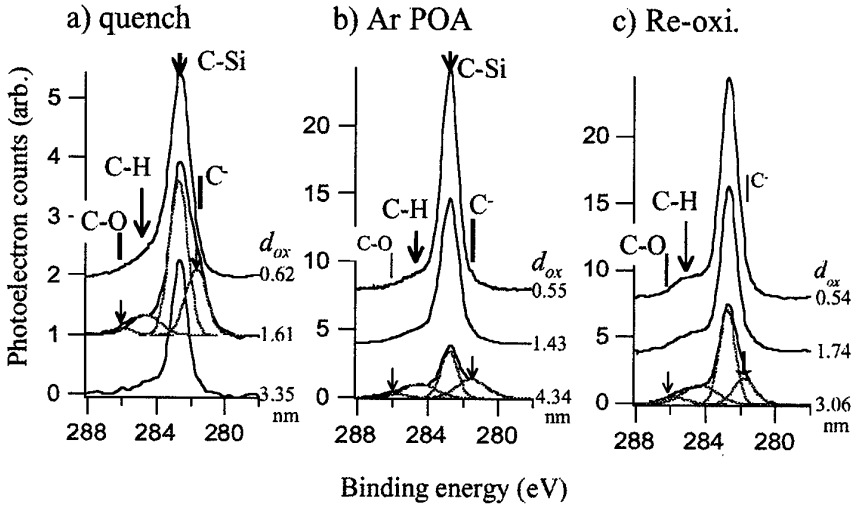


Fig.1 Photoelectron spectra of C1s core levels as a function of oxide

Replication of Defects from 4H-SiC Wafer to Epitaxial Layer

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The replication of defects such as screw dislocation and basal plane dislocation from 4H-SiC wafer to the epilayer was investigated by reflection X-ray topography. The Berg-Barrett geometry was employed using CuK α radiation and the **g** vector was $11\bar{2}8$. The incident angle to the surface of samples was 4.9 deg. and the absorption depth is 6.0 μ m under these conditions.

Figure 1 shows the topographs from (a) 4H-SiC epilayer with a thickness of 30 μ m and (b) 4H-SiC wafer on which the previous epilayer was grown. The topograph (b) was recorded before the growth of epilayer. The screw dislocations marked A are observed in both topographs at the same position. They are perfectly replicated from the wafer to the epilayer with the strained area around them. Basal plane dislocations form a network in the wafer, as marked B in topograph (b). Most of them are not replicated to the epilayer but a few are observed at same position of both topographs as marked C. The defects marked D and marked E are observed only in the epilayer. These defects are produced during the growth. The formers are needle-like and elongated to the off orientation. The topographs from epilayer depend on its thickness. Details will be shown at the conference.

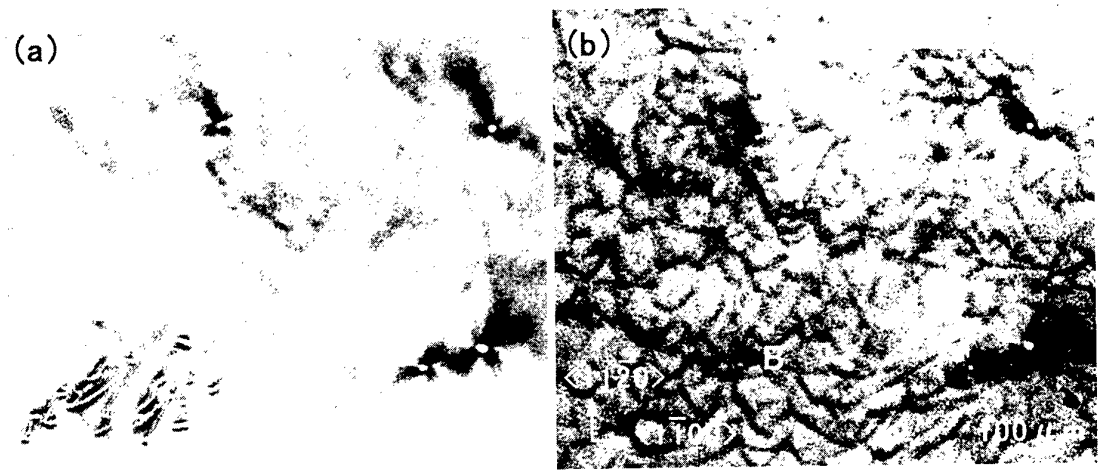


Fig. 1 Berg-Barrett topographs from (a) 4H-SiC epilayer and (b) the wafer on which the previous epilayer was grown. CuK α radiation. **g**=$11\bar{2}8$

Acknowledgement This work was performed under the management of FED as a part of the METI Project (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

Simulation of High-Temperature SiC Epitaxial Growth Using Vertical, Quasi-Hot-Wall CVD Reactor

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High-voltage SiC power devices use thick epitaxial layers so that achieving high growth rate is an important issue. It is considered that higher growth temperature might be advantageous for growing high-quality epilayers with fast growth rate. Kushibe et al., However, reported that the growth rate at high temperature rather decreases with increasing temperature because of H_2 etching of SiC[1]. We investigated the epitaxial growth model at high temperature by using computer simulation based on the competing reactions of H_2 etching and deposition taking account of the experimental data.

A vertical, quasi-hot-wall CVD reactor was used for experiments. The 2-dimensional axisymmetric model was used for simulations considering the thermal and multi-component gas-phase diffusions. The source gases were SiH_4 and C_3H_8, and carrier gas was H_2. The competing reaction on the SiC substrate surface was assumed as follows:

$$2SiC+H_2 \Leftrightarrow 2Si(g) + C_2H_2 \quad (R1)$$

The simulation indicated that the source gases are completely decomposed to Si(g) and C_2H_2 near the SiC substrate surface, and Si(g) and C_2H_2 are also generated by the H_2 etching reaction at high temperatures (≧1640℃). As the result, it is considered that epitaxial growth rate is dominated by the three major reaction paths at high temperature, namely (i)SiC etching by H_2, (ii)re-deposition of the byproducts of etching, and (iii)deposition by source gases. The experimental data were well explained by this competing growth model.

Reference: [1] K. Kushibe et al., Proc. of ICSCRM '99 (1999) 470.

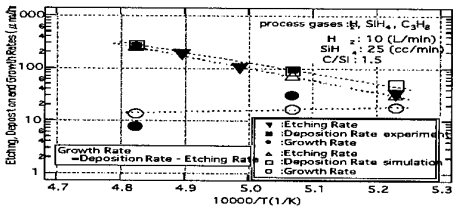


Fig.1 Temperature dependence of etching, deposition and growth rates.

Acknowledgement This work was performed under the management of FED as a part of the METI Project (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

Homoepitaxial growth of cubic silicon carbide by sublimation epitaxy

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Cubic silicon carbide has wider band gap than silicon and gallium arsenid and higher electron mobility than hexagonal silicon carbide. Therefore, cubic silicon carbide has an enough potential for low loss, high power and high frequency devices. In this work, crystal growth of cubic silicon carbide was carried out by sublimation method, especially sublimation epitaxy on cubic silicon carbide substrates.

Generally, cubic silicon carbide is grown on silicon substrates by chemical vapor deposition (CVD) [1]. However, the growth rate in CVD is very low. In this study, sublimation epitaxy was used in order to obtain thick and high quality cubic silicon carbide. In sublimation epitaxy, high quality epitaxial layers can be obtained with high growth rate (over 100μm/h) [2].

Crystal growth was carried out on cubic silicon carbide substrates. These substrates were grown on silicon or silicon carbide substrates by CVD. The growth temperature and the growth pressure during the homoepitaxial growth process were 1850°C and 30Pa, respectively. Crystal growth proceeded in argon atmosphere. In these conditions, the growth rate was about 50μm/h.

Fig.1 shows Raman spectra of the substrate and the grown layer. The thickness of the substrate and the grown layer were about 20μm and about 300μm, respectively. 3C-SiC LO phonon peak near 974cm^{-1} [1] is observed at both spectra. Therefore, it is considered that the cubic silicon carbide layer is grown on the cubic silicon carbide substrate. The surface of the grown layer was smoother than that of the substrate and anti phase boundary (APB) density was lower than the substrate.

In order to characterize grown layers, Raman scattering and X-ray diffraction were used. Moreover, the electrical property of the film and characteristics of Schottky diode will be discussed.

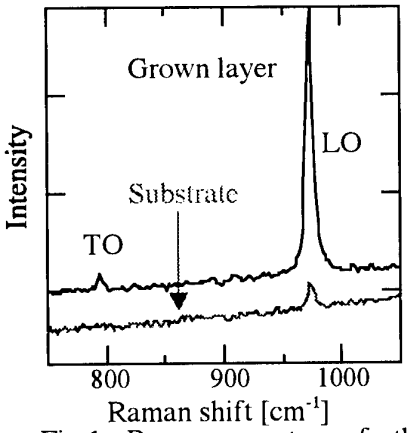


Fig.1 Raman spectra of the substrate and the grown layer.

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Electron-irradiation-induced amorphization in 6H-SiC by 300 keV transmission electron microscopy equipped with a field-emission gun

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Irradiation with energetic particles is an important technique to develop new functional materials. It is necessary to elucidate the fundamental radiation effects in SiC to obtain or maintain desirable materials properties for device production. One of the most important parameters for describing radiation damage is the threshold displacement energy (E_d), which is defined as the minimum kinetic energy to create a stable Frenkel pair. Much effort has been devoted to determine E_d of SiC, but the values estimated experimentally are considerably scattered over nearly an order of magnitude. In this study, we performed electron irradiation into 6H-SiC using *in-situ* transmission electron microscopy (TEM).

Single crystalline wafers of 6H-SiC (Cree, Inc.) were fabricated into samples appropriate for TEM study. Electron-irradiation experiments were performed at room temperature using JEOL JEM-3000F with incident electron energy of 300 keV. This facility is equipped with a field-emission gun as an electron source whose electron flux (~5×10^4 A/cm^2) is larger than conventional LaB_6 filament (~20 A/cm^2).

High-resolution TEM observations and electron diffraction experiments indicated that the electron-irradiated area is successfully amorphized, though the present irradiation conditions are beyond those required to induce a crystal-to-amorphous phase transformation (the incident electron energy of >750 keV and the temperature of <290 K) [1]. The E_d calculated assuming the incident electron energy of 300 keV turned out to be ~30 eV for silicon. The E_d obtained here is quite similar with that in experimental and theoretical reports: 30-35 eV by Rutherford backscattering technique [2] and 35 eV by molecular-dynamics calculation [3]. Because of high-electron flux of field-emission gun used here, it is considered that the damage-producing rate dominates over the recovery rate in the electron-irradiated area. We will also report an example of nano-fabrication of SiC using electron-beam-irradiation.

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Observation of 2 inch SiC wafer by SWBXT at SPring-8

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SiC bulk crystal made by sublimation method has a lot of defects and stress fields. These defects affect performance of device operation. So we must investigate and decrease defects and stress fields. X-ray topography is useful tool to observe defects and stress fields in a wafer. By using SWBXT (Synchrotron White Beam X-ray Topography), we observed the defects using facilities at SPring-8 (BL28B2). SR beam at SPring-8 has much merit, such as 8GeV electron beam energy, ultra-bright, highly directional, linearly polarized and so on. So, we tried to observe 2inch SiC wafers and discussed about defects more detail. We prepared 2 inch (0001) and (11-20) SiC wafers, which were made by sublimation method and measured by transmission and reflection mode. Fig.1 shows the topography of transmission mode. The directions of incident beam of Fig.1 (a) and (b) were <1-100> and <11-20> and diffracted planes were (11-23) and (1-103), respectively. Fig.1 (a) and (b) were observed at same area. But the images were different each other. From these images, Fig.1 (b) has more fine stripes than Fig.1 (a). Fig.2 shows these fine stripes. The contrast in Fig.1 (a) corresponded to the sub-grain boundaries, whose Burgers vector was <11-20>. And many fine stripes in fig.1 (b) were small defects or stress fields whose Burgers vector was <1-100> direction.

The defects were created by releasing the stress fields. But in the crystal, residual stress and elastic stress still exist, probably. And these stress fields appeared as small defects.

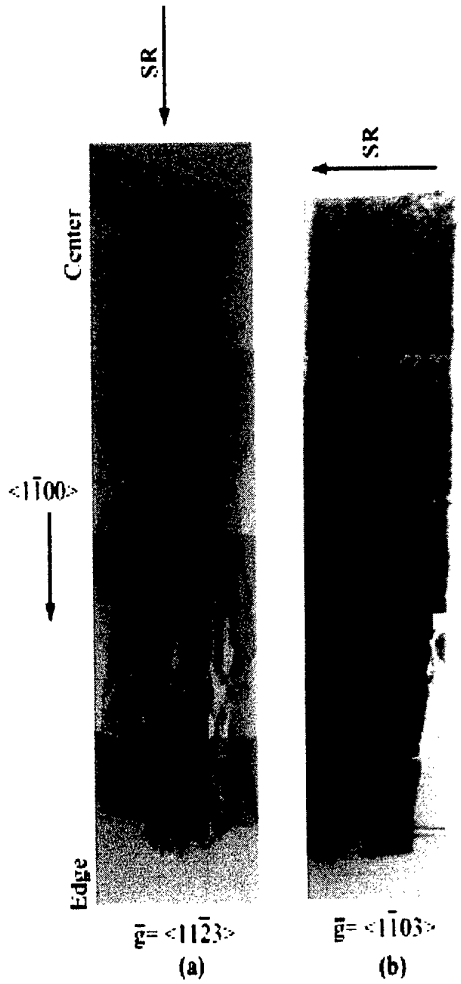


Fig.1 X-ray topography of (0001) 6H-SiC (transmission mode)

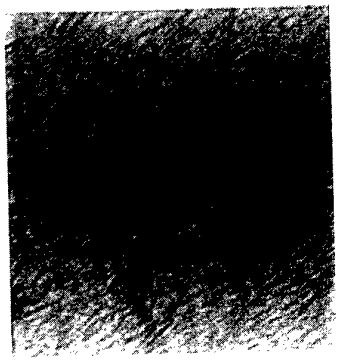


Fig.2 Enlarged image of Fig.1 (b)

Adsorbate Effects of the Surface Structure of 6H-SiC(0001) √3×√3 R30°

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Surface structures of 6H-SiC(0001) √3×√3 R30° surfaces have been studied by rocking curves of reflection high energy electron diffraction (RHEED) intensities and Auger electron spectroscopy (AES).

Two types of √3×√3 surfaces, √3×√3-Si (oxygen free) and √3×√3-C surfaces (oxygen adsorbed), were observed in a series of an annealing process. The √3×√3-Si surface was obtained by annealing the Si pre-deposited specimen in a Si flux for 3 min at 1045°C. After leaving the √3×√3 surface in a UHV chamber for 23 h, the RHEED pattern showed 1×1 periodicity, which turned into the √3×√3-C surface by annealing the 1×1 surface for 30 sec at 810°C. Rocking curves and AES spectra from the two √3×√3 surfaces clearly show that the two √3×√3 surfaces are structurally different. Peak-to-peak intensity ratios of Si LVV to C KLL peaks are 2.2 and 0.92 for the √3×√3-Si and √3×√3-C surfaces, respectively. The √3×√3-C surface transformed into the √3×√3-Si surface again by further annealing for 30 sec at 940°C. Rocking curves from the surface structures of the two √3×√3 surfaces have been analyzed by RHEED dynamical calculations based on multi-slice transfer matrix method. In conclusion, the √3×√3-Si surface is determined to be terminated with Si single-adatoms on T4 or H3 sites of the bulk surface. The two sites are not distinguished from this analysis because of the poly-type structure surface. From a preliminary analysis, the √3×√3-C surface contains C trimer structure.

In order to find what causes the phase transition from the √3×√3-Si to the √3×√3-C phases, hydrogen gas and oxygen gas are exposed to the √3×√3-Si surface at room temperature, then the samples are annealed to 700°C and 790°C in UHV, respectively. In the case of the hydrogen-treated √3×√3, the RHEED rocking curves and the Auger spectrum show good agreement with the √3×√3-C surface formed by annealing in UHV as mentioned above. Therefore, it is reasonable to suppose that the rearrangement of the √3×√3 surface in UHV is caused by adsorption of hydrogen on the √3×√3-Si surface.

Annealing Kinetics of the implantation-induced amorphous layer in 6H-SiC(0001)

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We reported that the amorphous layer on (11-00) and (112-0) oriented SiC can recrystallized to the original polytype structure by annealing below 1000 °C. However, there is a few study about the annealing kinetics of the implantation-induced amorphous layer in (0001)-oriented SiC. In this study, we report the annealing kinetics for the Ar ion implantation-induced amorphous layer of (0001)-oriented 6H-SiC in annealing temperature below 1000 °C.

Figure 1 shows the image of the cross-sectional electron transmission microscopy taken from 6H-SiC, implanted with 100 keV Ar at a dose of 2 x 10^{15}/cm^2 at room temperature, before and after annealing at 950 °C for 1 hr. In the as-implanted sample, the 120-nm thick amorphous layer can be observed. On the other hand, in the annealed sample, it is found that the amorphous layer is recrystallized to 3C-SiC, which can be divided into two regions indicated as I and II in figure. Regions I and II contain a large amount of micro-3C SiC crystals and a small amount of relatively large 3C-SiC crystals, respectively. It is suggested that the regrowth mechanism was changed during the annealing. Figure 2 shows the annealing time dependence of the thickness of the regrown 3C-SiC from 320 nm-thick amorphous layer. At the first stage, the regrowth rate is very small and is estimated to be 0.044 nm/min at 800 °C, which is 2 order of magnitude smaller than the case of (11-00)-oriented 6H-SiC. This slow regrowth corresponds to the growth of micro 3C-SiC crystals (see Region I in fig. 1). After regrowth of 3C-SiC layer with a thickness of about 60 nm, the regrowth rate is increased to 10 times faster than the first stage, which is connected to the growth of the large 3C-SiC crystals (Region II in fig.1). The regrowth rate in the second stage is estimated to be 0.35 nm/min at 800 °C. The activation energy of the regrowth of 3C-SiC is estimated to be 3.4 eV for both first and second stages, which is in good agreement with those of (11-00) and (112-0) oriented 6H-SiC.

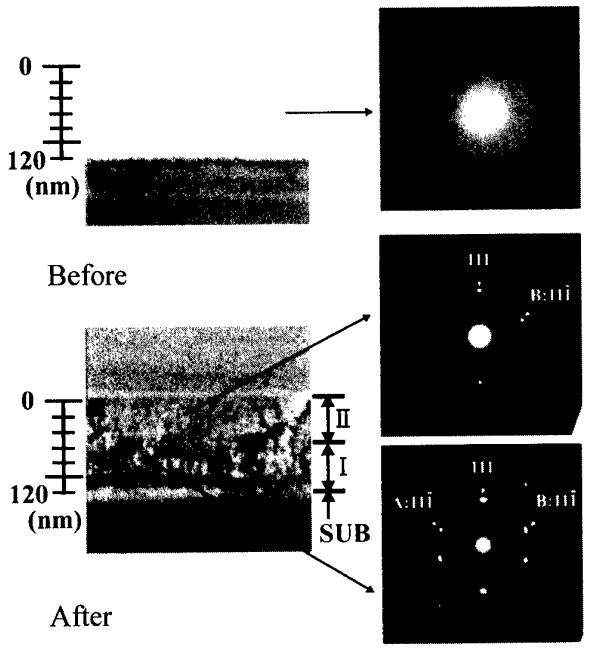


Figure 1

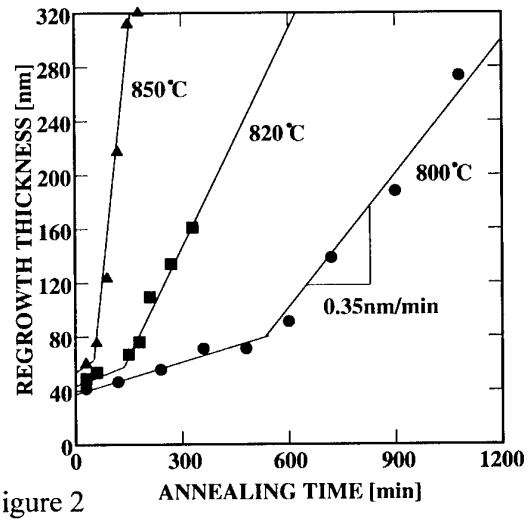


Figure 2

4*H*-SiC Schottky diodes with high on/off current ratio

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Silicon carbide Schottky Diodes (SD) with moderate blocking voltage (~300-1200V) are of great interest due to their high switching speed compared to Si PiN diodes. However, the on/off current ratio at fixed forward and reverse biases does not always compare as favourably. In this paper, we describe the fabrication and characterisation of SiC SD with moderate blocking voltage, having reduced reverse current and improved on/off current ratio.

The reverse current in a SiC SD depends on the contact metal barrier height and the applied voltage. Furthermore, the current under reverse bias is defined mainly by current flow through the contact periphery, where crowding increases the electric field. Conversely, the electrical characteristics of the diode under forward bias, are defined by the current flow through the whole diode area. Hence, the reverse current may be decreased with no increase in forward voltage drop if a thin strip of metal with higher barrier (e.g. Ni, 1.6 eV) surrounds the contact consisting of the metal with lower barrier height (e.g. Ti, 1.2 eV).

Commercial 4*H*-SiC n-n^+ wafers ($3\cdot10^{15}$cm^{-3}; 10 μm) were used to fabricate these diodes. All metals were deposited with no sample heating. Nickel, 100 nm thick, was deposited on the back side of the wafer and annealed at 1100°C to form the ohmic contact. To form the SD, titanium (4-15 nm thick) and nickel (100-150 nm) were deposited consecutively. After contact geometry definition by contact photolithography and chemical etching of Ni (Fig.1b), the Ti was etched selectively to nickel (Fig.1c) in liquid etchant. The time of overetching defined the width of the Ni strip. During specimen drying, the Ni film was bent by surface tension forces forming tight contact to SiC (Fig. 1d). Finally, the Schottky contact was formed by annealing at 450-650°C for 60 min.

The diodes had a breakdown voltage of about 750 V, with a barrier height in forward bias of 1.2 V, (as observed for Ti SD) whilst the reverse current was similar to Ni SD (Fig. 2). They had an on/off current ratio at 1V/500V of about $5\cdot10^8$. This value exceeds the on/off ratio of Ti/SiC and Ni/SiC SD fabricated on the same epitaxial wafer and exceeds those published in the literature for SD with moderate breakdown voltage. To verify the formation of Ni contact strip around Ti Schottky contact, it was decorated as indicated in Fig. 1e-1f. A SEM picture of the decorated edge strip is shown in Fig. 3. Full details of the diode fabrication and electrical characterisation will be given in the final paper.

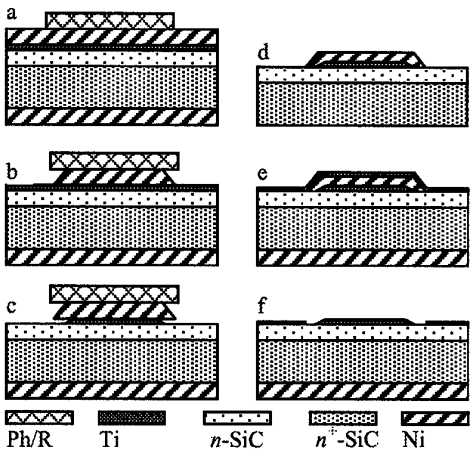


Fig. 1. Device processing flow map for (a - d) SD fabrication and (e - f) edge metal strip decoration.

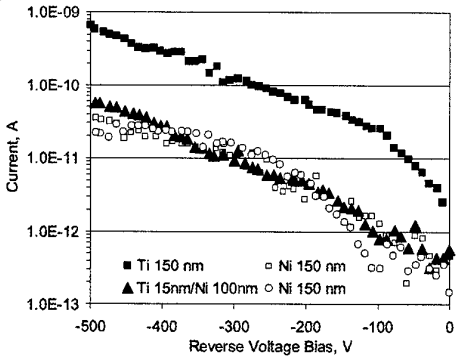


Fig. 2. Reverse currents of Ti, Ni, and Ti/Ni SD on 4*H*-SiC measured at room temperature. (SD diameter is 400 μm).

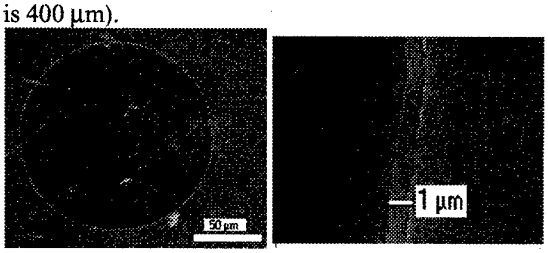


Fig. 3. SEM pictures of decorated edge metal strip.

Characteristics of MESFETs made by Ion-implantation in Bulk Semi-insulating 4H-SiC

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In this work, I-V, C-V and DLTS characteristics of fully ion-implanted n-channel Metal-Semiconductor Field-Effect-Transistors (MESFETs) made in semi-insulating (SI) bulk 4H-SiC with W/L = 280 μm/ 2 μm are studied. In order to create the source/drain and the channel regions of the MESFET, nitrogen implantations were performed to a depth of 300 nm at room temperature to volumetric concentrations of $2x10^{19}$ cm^{-3} and $6x10^{17}$ cm^{-3}, respectively. To activate the implants, annealing was performed for 15 minutes at 1450°C in an argon ambient using an AlN encapsulation. Ohmic contacts to the source/drain areas were formed by e-beam evaporation and lift-off of Ni (100 nm), followed by a 1200 °C / 3 minute anneal in vacuum. Al Schottky gate metallization (~100 nm thickness) was performed by e-beam evaporation. From capacitance-voltage (C-V) measurements taken before forming the channel recess, the channel substitutional dopant concentration was found to be $3x10^{17}cm^{-3}$, which represents a 50% activation of the implanted nitrogen species in this region. Van der Pauw Hall measurements of on-wafer test patterns showed a room temperature volumetric carrier concentration of $2x10^{17}cm^{-3}$, with a bulk electron mobility of 240 cm^2 / V·s. The pinch-off voltage and the saturation drain current (I_{dss}) of the MESFETs are found to be –18 V and ~30 mA, respectively. The drain conductance (g_d) and the mutual transconductance (g_m) calculated from the MESFET's I_D-V_{DS}-V_{GS} curves are 7.9 mS and 5.4 mS, respectively. A poor source/drain ohmic contact resistance of ~ 10^{-2} Ω-cm^2 is believed to be partially responsible for these low conductance values. The MESFETs showed stable device characteristics over the temperature range 25°C-350°C. Due to the poor ohmic contact resistance value, the channel carrier mobility extrapolated from the g_d and g_m values is about 5 times smaller than the bulk Hall carrier mobility. The residual implant lattice damage at the interface is also partially responsible for the low g_m and g_d values. To investigate the implant lattice damage induced traps in the MESFET structure, we performed Deep Level Transient Spectroscopy (DLTS) measurements on the channel/SI substrate interface in the temperature range from 200K to 550K. A Schottky gate reverse bias voltage of ~-10V was applied to push the depletion region into the vicinity of the nitrogen implanted channel and the SI substrate interface. With a proper choice of the rate window, several traps were detected at the channel/ substrate interface at 0.51 eV, 0.6 eV, 0.68 eV, 0.768 eV and 0.89 eV above the valence band edge (E_V) at relatively high concentration (N_t ~ 0.01 N_s, where N_s is the net carrier concentration). The trap located at E_v + 0.51 eV is believed to be due to a point defect created by nitrogen implantation, and the trap at E_v + 0.6 eV can be related to the deep acceptor level introduced by the V dopant in the semi-insulating material. Origins of the other traps are unknown at this time. The normalized amplitude of all peaks decreased linearly with decreasing reverse bias on the Schottky gate, indicating that the defect concentration decreases at distances further from the channel/substrate interface. The implant defect related traps might have also contributed to the poor effective carrier mobility in these MESFET devices. Optimization of the implant/annealing temperatures and source/drain ohmic contact formation parameters are expected to yield improved device performance to make ion-implantation in SI substrates an attractive doping process for SiC device fabrication.

Epitaxial growth of (11-20) 4H-SiC using substrate grown in the [11-20] direction

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Homoepitaxial growth on 4H-SiC (11-20) substrate grown in the [11-20] direction by sublimation method has been investigated by low-pressure, hot - wall type CVD reactor with $SiH_4 - C_3H_8 - H_2$ – system. Typical gas flow rate of H_2, SiH_4 and C_3H_8 were 40 slm, 6.67 sccm and 3.33 sccm, respectively. The growth temperature and the reactor pressure were 1600°C and 250 mbar, respectively.

The surface of epilayers exhibited smooth and no defects morphology with the surface roughness (Rms) of 0.14nm in 16μm square. This roughness was smaller than that of epilayer grown on conventional (11-20) substrate grown in the [0001] direction. By KOH etching experiment, it was found that the stacking fault in the substrate was replicated to the epilayer and the density of the stacking faults was in the order of 10^2 cm^{-1}. The surface morphology was not affected by the stacking faults of this density range.

Figure 1 shows the x-ray rocking curve at 11-20 reflection peak obtained from 5 μm-thick epilayer. This epilayer exhibited the sharp and single diffraction peak in both x-ray incident directions of parallel and perpendicular to c-axis. The FWHM of each peak was 13.7 and 15 arcsec respectively. In our previous study, epilayers grown on conventional (11-20) substrate exhibited splitting and broadening (FWHM=477 arcsec) of the diffraction peak in the incident direction of perpendicular to c-axis [1]. The crystalline quality of (11-20) epilayers is improved by using the substrate grown in the [11-20] direction.

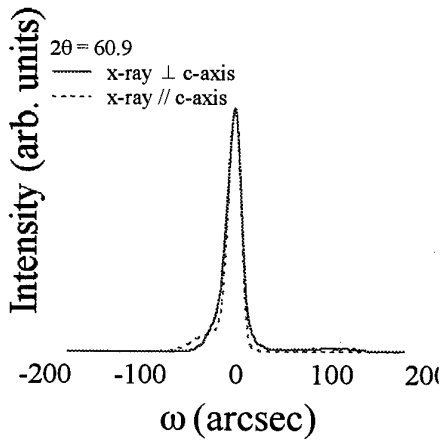


Figure 1. X-ray rocking curve of ω scan

The characteristics of MOS structure fabricated on this epilayer will be also presented in this conference.

Acknowledgement
This work was performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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Improvement of SiO_2/α-SiC interface properties by nitrogen radical treatment

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Si MOSFETs have good characteristics of fast switching and a low value of on-resistance (R_{on}) reduced year by year. The R_{on} of Si MOSFETs has almost reached a theoretical limit originated from material properties of Si. So it is important to develop MOSFETs on SiC to achieve further reduction of R_{on} for future evolution in power electronics. However, it is difficult to fabricate high performance MOSFETs on SiC because of poor interface characteristics of SiO_2/SiC. In recent years, a number of studies have been conducted on the effect of NO annealing, which improves SiO_2/4H-SiC interface properties. In this study, we propose a new method for the improvement of SiO_2/α-SiC interface quality by irradiation of N radicals with high reactivity at low temperatures.

N-type 6H- and 4H-SiC Si(0001) face epilayers with donor concentration of $2\times10^{16}cm^{-3}$ were used. After standard RCA cleaning, dry oxidation was performed at 1100℃ for 2h followed by post oxidation annealing in Ar at 1100℃ for 30min. The oxide thickness was approximately 14nm determined by accumulation capacitance in high-frequency C-V curves. In N radical treatment, N_2 gas (gas flow:1.25sccm, pressure:$1\sim5\times10^{-5}$Torr) was activated by RF power (13.56MHz, 230W) applied to an induction coil. Charged species, which would cause damage to the oxide film, were eliminated from N plasma with the use of ion trap electrodes. So electrically neutral N radicals were irradiated to the surface of the sample. After growing the oxide film and N radical irradiation, angle resolved XPS (ARXPS) measurement was carried out to estimate atomic components in the oxide film. MOS capacitors with gate electrode of Al were fabricated. High-frequency (1MHz) C(G)-V measurements were performed to evaluate SiO_2/α-SiC interface properties.

Fig.1 shows the SiO_2/4H-SiC interface trap density determined by the Terman method. Fig.1 extends that the N radical treatment reduced interface trap density from $6\times10^{12}cm^{-2}eV^{-1}$ to $4\times10^{12}cm^{-2}eV^{-1}$ at the Fermi energy for 4H-SiC. The reduction of interface trap density was also observed for 6H-SiC ($1.3\times10^{12}cm^{-2}eV^{-1}$ and $5.5\times10^{11}cm^{-2}eV^{-1}$ before and after the N radical treatment, respectively). The improved property was maintained after N_2 annealing at 1050℃. From ARXPS measurement, approximately 2-4at% N atoms were incorporated into the oxide film. Fig.2 shows N1s peak area as a function of depth, which represents N distribution in the oxide film. The result indicates that most of N atoms are accumulated at the surface of SiO_2. The improvement of interface properties was assumed to be due to interface modification by introducing small quantity of N radicals reached to the SiO_2/α-SiC interface, which could not be detected by ARXPS measurement due to low sensitivity.

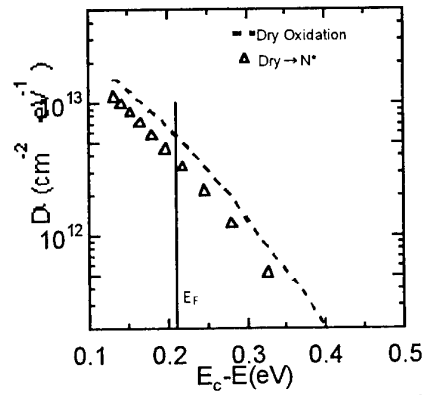


Fig.1 Energy distribution of D_{it} for n-type 4H-SiC

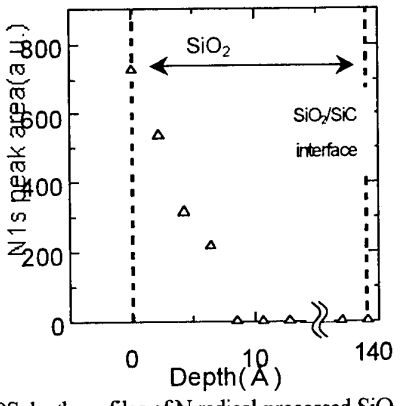


Fig.2 XPS depth profiles of N radical processed SiO_2/4H-SiC

Effects of Surface Treatments of 6H-SiC upon Metal-SiC Interfaces

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1. Introduction

Surface treatments to obtain clean and ordered surfaces of semiconductors are basic techniques. It is well known that the H terminated Si surfaces are obtained by HF treatments, and these surfaces function against chemical attacks of contaminants such as O and C, which degrade metal-Si interface quality [1]. In this study, we report on effects of surface treatments of 6H-SiC upon metal-SiC interfaces.

2. Experimental

Samples of n-type (N_D-N_A=8.61x10^{17}/cm^3) 6H-SiC (0001) Si-face were used in this study. In order to reduce scratches, as received samples were polished with colloidal silica before chemical treatments. To remove organic contaminations, H_2SO_4:H_2O_2 treatment at 150 °C was performed. After rinsing in deionized water, the samples were dipped in boiling HF (BoHF) at 95 °C (10 min x 3 sets) or in HF at room temperature (30 min). Some of BoHF and HF treated samples were rinsed in deionized water. The elemental composition of the surface was investigated by Auger electron spectroscopy (AES). For current-voltage (I-V) measurements, Al contacts were fabricated by thermal evaporation with a base pressure of ~3x10^{-7} Torr.

3. Results and Discussion

AES analysis indicated that the main elemental composition of the surfaces after chemical treatments was Si, C, and O atoms. The peak-to-peak height of the O *KLL* AES peak, which was normalized by the BoHF treated sample, was 1.00 (BoHF), 1.03 (BoHF+Rinse), 1.14 (HF), and 1.25 (HF+Rinse). After exposing these samples to air for 100 min, the O *KLL* peak-to-peak height changed to 1.10, 1.13, 1.25, and 1.36, respectively. From these analyses, it was found that the BoHF treatment removed O atoms from the surface and rinsing in deionized water added O atoms to the surface. In order to investigate metal-SiC interfaces, Al contacts were fabricated on the BoHF and HF+Rinse treated samples, subsequently exposed to air for 100 min. Fig. 1 shows I-V characteristics of the two samples. Significant differences were not found between two samples. We think that ohmic contacts were achieved because of gettering of O atoms to Al contacts and the sharp Al-SiC interface formation.

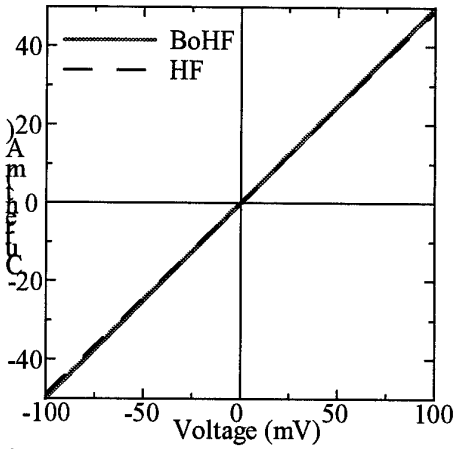


Fig. 1. I-V characteristics of the BoHF and HF+Rinse treated samples, subsequently exposed to air for 100 min.

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Hot Wall CVD Growth of 4H-SiC Using Si_2Cl_6+C_3H_8+H_2 System

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In these days, it has been succeeded in homoepitaxial growth of silicon carbide (SiC) by hot wall CVD using SiH_4+C_3H_8+H_2 system. It is desired to epitaxial growth using other safety silicon source material. And then, we have grown SiC using hexachlorodisilane (Si_2Cl_6) as a silicon source material. Si_2Cl_6 is a safe material and we already succeeded in a homoepitaxial growth of SiC by cold wall CVD. In this paper, we report homoepitaxial growth of 4H-SiC by hot wall CVD using Si_2Cl_6+C_3H_8+H_2 system.

A growth condition was as follows: Si_2Cl_6 flow rate is 0.3sccm~0.6sccm as a silicon source gas, C_3H_8 flow rate was 0.2sccm~0.4sccm as a carbon source gas, H_2 flow rate was 3.0slm as a carrier gas, a growth temperature were 1550°C~1650°C, a growth time were 60min~300min. 4H-SiC(0001)Si8.0°<11-20>off-axis was used for the substrate. A SiC coated separable cylindrical graphite blocks with square channel were used as a susceptor and a rf generator was 300kHz-20kW. The growth rate was about 2μm/hour at Si_2Cl_6 flow rate was 0.3sccm.

At 1550°C growth, though the shallow round pits increased at Si-rich condition on the surface morphology of cold wall CVD, these pits increased at C-rich condition on that of hot wall CVD. In hot wall CVD the reaction gas was effectively dissociated, and generated different active chemical species from cold wall CVD. Therefore we got such a different surface morphology tendency to C/Si ratio between cold wall CVD and hot wall CVD.

At 1650°C growth, scratch like defects that array along to [1-100] direction was observed (Figure1). We think that these defects were generated to etch the surface due to be higher the substrate temperature. As the array direction of these defects is cross to a direction of step flow, these defects have any relation to step flow. Furthermore, when we took out an upper part of the susceptor block in order to minimize the radiation heating, these defects became deeper. We think that etching was enhanced due to expand a temperature gradient to between the surface and the gas flow.

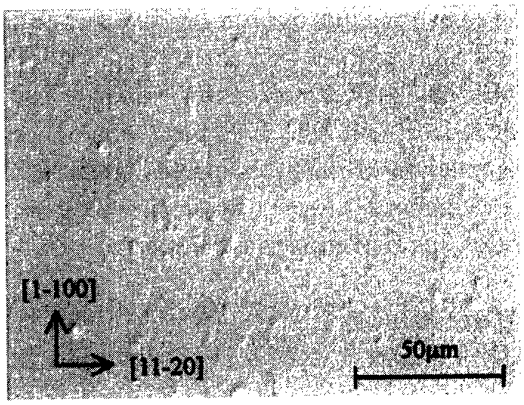


Figure1: Scratch like defects at 1650°C

Spatial mapping of the carrier concentration and mobility in SiC wafers by micro Fourier-transform infrared spectroscopy

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Silicon carbide is a promising material for applications in high-temperature, high-power, and high-frequency electronic devices due to its wide band gap, high saturated electron velocity, and high breakdown electric field. Recently, heavily doped SiC wafers have been grown in order to study the effect of heavily doping on crystal growth and defect generation. However, heavily doped SiC wafers are often not so uniform.[1] Since spatially inhomogeneous doping leads to poor quality epitaxial layers and thus to poor device performances, highly uniform doping is necessary for practical use. In the present study, we have, for the first time, tried to investigate the spatial distribution of carrier concentration and mobility in SiC wafers by micro Fourier-transform infrared (FTIR) spectroscopy. The sample used in this study was an intentionally inhomogeneous N-doped 6H-SiC wafer grown by modified Lely method. Reflectance measurements were carried out using a FTIR spectrometer at room temperature. The spatial resolution was 50 μm. Figure 1 shows typical reflectance spectra obtained from heavily doped (a) and lightly doped (b) regions. The reflectance spectra were analyzed using the dielectric function considering the contributions from phonons and plasmons.[2] From the analysis, carrier concentrations and mobilities were estimated to be 7.2×10^{19} cm^{-3} (μ = 11 $cm^2V^{-1}s^{-1}$) and 9.7×10^{17} cm^{-3} (μ = 73 $cm^2V^{-1}s^{-1}$) for reflectance spectra shown in Fig. 1(a) and (b), respectively. Figure 2 shows the carrier concentration profile in the inhomogeneously doped SiC wafer. The measurements were made at various points along the white line in the photograph taken with a transmitted light, where dark areas correspond to heavily doped regions. Our results demonstrate that the micro FTIR is a useful and nondestructive technique to characterize the spatial distribution of carrier concentration and mobility in SiC wafers.

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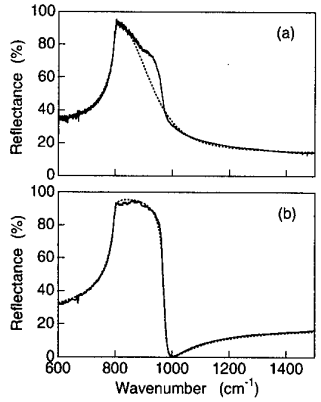


Fig. 1 Reflectance spectra of SiC.

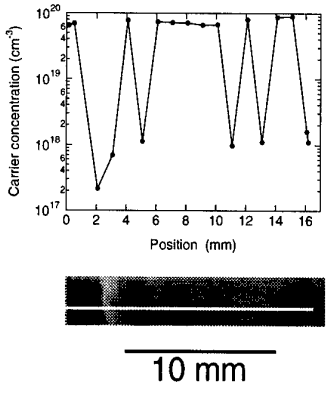


Fig. 2 Line profile of carrier concentration in SiC.

Characterization of inclusions in SiC bulk crystals grown by modified Lely method

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There have been the intense demands of a high quality silicon carbide (SiC) single crystal. However the quality still needs further improvement, because the crystals still contain a number of inclusions and defects. It is important to define the origin of the inclusions and the defects in bulk crystals to obtain a high quality bulk SiC single crystal. In this work, we have investigated two types of the inclusions, which have not been reported. They were dendrites, which consist of carbide of transition element, and the transparent inclusions with oval like shape, which were the origin of misoriented crystals.

6H-SiC bulk crystals were grown in the inductively heated furnace by modified Lely method. Commercial SiC abrasive with or without a chemical treatment were used as the source powder. The growth was performed in a high purity argon ambience at 10 Torr. The temperatures of the top and bottom of the crucible were 2200°C and 2250°C, respectively. The inclusions in the SiC bulk crystals were characterized with optical microscope and EPMA.

The dendrites were observed only in the SiC bulk crystal grown with the source powder without the chemical treatment. The components of the dendrites were measured by EPMA. The dendrites consisted of carbon, vanadium and titanium, which molar fractions were 0.41, 0.36 and 0.23, respectively. Silicon was not almost contained in the dendrites. It was considered that vanadium and titanium were incorporated into the SiC bulk crystals from the source powder and then the dendrites were generated by condensation of titanium carbide and vanadium carbide during the growth. Use of high purity source will prevent such generation of dendrite. Vanadium is used as the dopant of semi-insulating SiC single crystals. Such generation of the dendrites is a serious mater in the growth of the high quality semi-insulating SiC bulk crystals. The transparent inclusions with oval like shape are observed in the SiC bulk crystal grown with the chemical treated source powder. Misoriented phases mainly originate from these transparent inclusions. The inclusions had a small core on the optical microscopic observation. From the result of EPMA, the components of this small core consisted of carbon and silicon, which molar fractions were 0.67 and 0.33, respectively. Although the other part of the transparent inclusion also consisted of carbon and silicon, their molar fractions were 0.50 and 0.50, respectively. The transparent inclusions were considered to be the misoriented SiC phase, which was grown around a carbon-rich core.

This work was financially supported by METI partly through NEDO. The authors thank Mr. M. Okada for his help on EPMA analyses.

Temperature Dependence of Sublimation Growth on 6H-SiC (11$\bar{2}$0) Substrates

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1. Introduction

Crystal growth on (11$\bar{2}$0) substrates is strongly focused due to the high channel mobility of MOSFET [1] and the low leakage current of schottky diode [2]. Since crystals of SiC has been conventionally grown on (0001) substrates, crystal growth on (11$\bar{2}$0) substrates has not been researched sufficiently. To grow high quality crystals on this plane, further investigation of growth mechanism is important. The role of "low-temperature growth process" insertion was investigated.

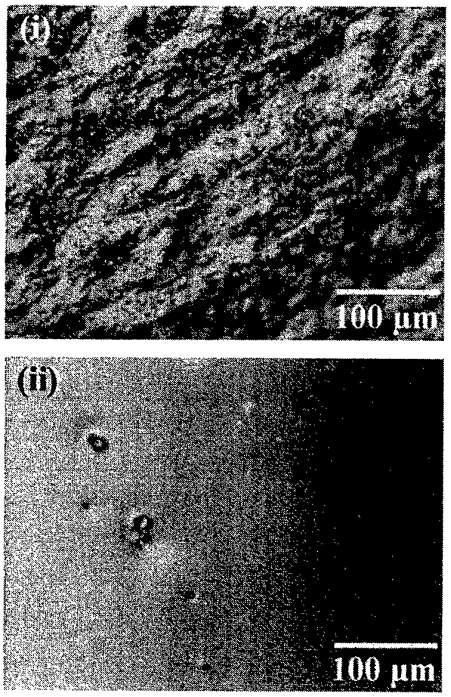
2. Experiment

Crystals were grown by the sublimation method. (11$\bar{2}$0) substrates were prepared by cutting the boules previously grown on (0001) substrates. The source material was abrasive SiC powder. Temperature at the bottom of the crucible (Tb) was monitored by optical pyrometer. Crystals were grown in argon or nitrogen atmosphere. Growth pressure (p) was approximately 40 Torr. Surface was observed by optical microscope, scanning electron microscope and atomic force microscope.

3. Results and Discussion

Figures (i) and (ii) are the surface morphology of the crystals grown on (11$\bar{2}$0) substrates in nitrogen atmosphere. Figure (i) is a crystal which grown at Tb=2400 °C and p=40 Torr for 1 hour. The surface was undulated. By introducing a "low-temperature growth process", surface flatness was improved as shown in Figure (ii). A crystal shown in Figure (ii) was grown at Tb=2100 °C and p=100 Torr for 1 hour before growing at Tb=2400 °C and p=40 Torr for 1 hour. Insertion of this "low-temperature growth process" was effective to improve crystal quality.

Since (11$\bar{2}$0) surface has a higher surface energy, an "adhesive" type growth is dominant than step flow growth. So, it is important to grow crystals in two-dimensional mode on (11$\bar{2}$0) substrates. If crystals grow in three-dimensional mode, hollow core defects would be produced [3]. To grow crystals in two-dimensional mode on (11$\bar{2}$0) substrates, atomically flat and defect free surface is key, since nucleation would preferentially occur at defect sites on the surface. At lower growth temperatures, surface diffusion length of migrating species become shorter and smaller islands nucleate with high density. This high density nucleation of islands enables the homogeneous coalescence at initial stage of the growth with low defect formation. In this way, flat surface with low defect density which is important to realize two-dimensional growth on (11$\bar{2}$0) substrates was achieved. The difference between the growth in nitrogen atmosphere and in argon atmosphere will be also presented at the conference.



Figures. *Optical microscope images of the crystals grown on (11$\bar{2}$0) substrates in nitrogen atmosphere.*
(i) 1 hour growth at Tb=2400°C, p=40 Torr.
(ii) 1 hour grown at Tb=2100°C, p=100 Torr ("low-temperature growth process"), followed by 1 hour growth at Tb=2100°C, p=40 Torr.

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Vapor Phase Epitaxial Growth of n-type SiC Using Phosphine as the Precursor

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The material properties of SiC make it an interesting semiconductor for devices operating at high temperature, high power, and high frequency. As the development of device proceeds, the demands on the quality of the epitaxial layer and the doping controllability are rapidly increasing. Nitrogen and phosphorous are the most common n-type dopants in SiC. While nitrogen doping and its incorporation mechanisms during epitaxial growth have been studied extensively by several groups [1-3], not much research work has been reported on in-situ doping using phosphorous.

We have carried out phosphorous doped SiC epitaxial growth in a horizontal, water-cooled cold wall reactor. Experiments were performed at temperatures ranging from 1500-1620°C. Silane (2% in H_2) and Propane (2% in H_2) and phosphine (1000ppm in H_2) were used as Si, C and P precursors, respectively. Substrates were (0001) Si-face 4H-SiC and 6H-SiC from Cree. The epitaxial layers were characterized by mercury probe CV measurements and SIMS. The doping dependencies on PH_3 flow, growth temperature and C/Si ratio were studied.

The influence of PH_3 flow on phosphorous doping was investigated at 100 torr and 1560°C. Flow of H_2, SiH_4 and C_3H_8 were fixed at 7slm, 1 sccm and 1.2 sccm respectively. It is shown that the n-type doping concentration in the range of mid 10^{15} cm^{-3} to mid 10^{16} cm^{-3} can be achieved when PH_3 flow was varied from 0.05 sccm to 1 sccm. Also the increase of doping concentration is approximately proportional to the square root of PH_3 flow. Study on the effect of growth temperature showed that phosphorous doping decreased when temperature is increased from 1500 to 1620°C. This was explained by the enhanced desorption of Phosphorous-containing species on the growth surface at higher temperature. The site-competition growth was carried out with C/Si ratio varied from 0.3 to 14. It was shown that phosphorous incorporation was insensitive when C/Si was higher than 3 or lower than 0.9. However, the phosphorous incorporation increases with decreased C/Si ratio when C/Si is between 3 and 0.9. This is opposite to what has been reported in reference [4]. The difference might originate from different growth conditions (pressure, H_2 flow, etc.). Our result seems to suggest that phosphorous might occupy C site rather than Si site at certain growth conditions.

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A Simple Mapping Method of Elementary Screw Dislocations in Low-doped Hexagonal SiC Epitaxial Layers

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The morphologies of etch pits of three different kinds of dislocations in low-doped hexagonal polytype epitaxial layers have been investigated by KOH etching, synchrotron white beam x-ray topography (SWBXT), optical microscopy, and atomic force microscopy (AFM). A simple method by KOH etching and polishing for monitoring elementary screw dislocations in SiC epilayers is proposed.

Elementary screw dislocations are known to reduce the breakdown voltage of SiC p-n junctions and Schottky barriers. There are major efforts underway in reducing their density in both substrates and subsequent device layers. To do so, it is important to have or to develop a method for characterization of screw dislocation density and distribution.

The samples examined in this study were 4H-SiC wafers oriented 8° from the [0001] toward the $<11\bar{2}0>$ directions with 10 μm thick epitaxial layers, and an on-axis n^+ 4H-SiC substrate. The low-doped ($\sim 10^{15}$ cm^{-3}) epitaxial layers were grown on (0001) Si surface of substrate by vapor phase epitaxy (VPE) at a low pressure (~100 mbar). Epilayers were etched in molten KOH to reveal the locations where dislocations intersect the (0001) Si surface. The shapes of etch pits were analyzed by optical microscopy and AFM. The etch pits of threading dislocations were hexagonal in shape and had two distinctly different sizes. The larger ones were more symmetric than the small ones, implying the dislocations of small etch pits were inclined. The etch pits of basal plane dislocations were oval-shaped, suggesting small angle formed by the dislocation line with the surface. Three different etch pits could be distinguished under optical microscope at ×200 magnification, owing to the difference in etch pit depth clearly visible using Nomarski differential interference optics. AFM study of lightly etched layers showed the large pits of threading dislocations are approximately twice as deep as the others. The large pits in etched morphology correspond one to one to the white dot contrasts of elementary screw dislocations in the SWBXT image. Etched epilayers were carefully polished with 6 μm diamond paste. It was possible to remove a top layer of the structure leaving only the etch pits due to elementary screw dislocations. The same method was tested on the on-axis n^+ substrate. The etch pits were all circular and in several different sizes, making it very difficult to distinguish edge and screw dislocations.

Power Schottky and p-n diodes on SiC epi wafers with reduced micropipe density

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Micropipe density reduction and its impact on device performance is a critical topic in SiC power device development. In this paper we report on 2 mm diameter devices fabricated with high device yield on 2 inch 4H-SiC wafers with reduced micropipe density (RMD). Both Schottky and p-n diodes were fabricated on epitaxial layers grown on SiC RMD wafers.

Micropipe filling process was done on (0001)Si face of off-axis commercial 2 inch 4H-SiC substrates with standard micropipe density. Micropipe density after the filling did not exceed 10 cm^{-2}. 4H-SiC device epitaxial layers about 10 microns thick with concentration N_d-N_a ~$10^{15} \div 10^{16}$ cm^{-3} were consequently grown by CVD method. Schottky diodes without edge termination were formed on the CVD layers by Ni (~15 nm) evaporation and consequent gold deposition (~0.5 μm) in the same evaporation run, to ensure good spreading of electric current.

P^+-layers for p-n diodes were grown on the CVD n-type layers by sublimation method. Uniform p-type sublimation epitaxy for 2" SiC wafers was demonstrated for the first time. Mesa structures for pn diodes were formed by reactive ion etching.

Diodes of 2000, 1000, 500 and 200 μm diameter were fabricated. For more than 58% of 2 mm diodes, the leakage current was less than 1 μA at 300 V reverse voltage. For more than 50% of 2 mm diodes reverse voltage exceeded 600 V. Forward IV characteristics had a turn-on voltage of about 1.25 V and state-on resistivity of about 4 Ω. On-state resistance was determined by doping level of the substrate and can be reduced by diode parallel connection.

Reverse blocking voltage for 2 mm pn diodes of over 700 V was obtained. For both Schottky and pn diodes electric breakdown at device periphery was frequently observed. These results show high potential of micropipe filling technology for power device development, especially for large area (>3 inch) SiC wafers. Device and material characteristics will be presented and discussed.

OXIDATION-INDUCED CRYSTALLOGRAPHIC TRANSFORMATION IN HEAVILY N-DOPED 4H-SiC WAFERS

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Crystallographic stability of SiC during processing and device operation is of concern, particularly because of the recent discovery that 4H to 3C polytype conversion can occur under carrier injection in a *pn* junction. We have discovered a pronounced crystalline instability in 4H-SiC wafers doped with unusually high levels of N (nominally 0.008 Ω-cm resistivity, ~$3x10^{19}$ cm^{-3} donors) when the wafers are subjected to a standard oxidation cycle. A total of seven such commercially obtained wafers (from five different boules), having ~2 μm thick epitaxial layers doped at the 1-1.5x10^{17} cm^{-3} level with N, were thermally oxidized at 1150 °C for 90 min. in dry O_2 to a thickness of ~325 Å. Their surfaces appeared normal and smooth prior to oxidation, but immediately after oxidation exhibited dimpled regions, usually in the centers of the wafers and surrounded by a pronounced ridge roughly 2 μm high. The sharp ridges separating dimpled from undimpled regions generally coincide with the edges of the more heavily-doped central (dark) regions in the substrates. Those regions presumably correspond to the (0001) growth facets in the substrate boule. Some transformed wafers were characterized by confocal micro-Raman scattering, synchrotron-based white beam X-ray topography (SWBXT), and photoluminescence (PL). In addition, we fabricated Schottky diodes on three wafers using Ti, Ni, and Pt and characterized their barrier heights by current-voltage (*I-V*) and capacitance-voltage (*C-V*) methods. The barrier heights are uniformly lower in the dimpled regions by about 0.47 V compared to the peripheral, undimpled regions of each wafer, *independent* of the Schottky metal (even though the barrier heights differ by up to 0.6 V among the metals). Idealities of the diodes are actually better in the dimpled regions than in the undimpled regions, and the epilayer doping does not vary between dimpled and undimpled regions after transformation. The SWBXT images show a dense cellular structure of dislocations only in the central, dimpled regions, but were not able to detect any 3C material. The Raman measurements, which sample about the top 2 μm of each sample, show phonons characteristic of 4H-SiC in both dimpled and undimpled regions, but a marked enhancement in the relative strength of several modes including A_1(LO) in the dimpled regions. The PL measurements, however, show a dramatic shift in the highest energy peak at 300 K from the usual 4H position of 3.16 eV in the undimpled peripheral regions to 2.42 eV in the dimpled areas, suggestive of 3C regions or lamellae (which may be too small to detect by Raman or topography). The 3C regions could also explain the reduced Schottky barrier heights. Transmission electron microscopy and low temperature PL are in progress to clarify the nature of the transformation. Possible causes will be considered. This effect may limit the maximum doping that can be employed in *n*-type substrates.

This work was supported by the National Science Foundation under Grant No. ECS 0080719, and by a Motorola Semiconductor Products Sector Sponsored Project.

Observation of planer defects in 2 inch SiC wafer

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SiC bulk crystal has been grown by the sublimation method. The defects such as micropipe (MP) and planer defect (PD) can cause serious problems for device performances. Therefore, it is important to reduce these defects for the realization of high device performance.

Diameter of the substrate was 40mm. As the crystal grew 15 mm, diameter was expanded to 50mm by the sublimation method. Top of the grown bulk was convex and facet appeared in the center. Three SiC wafers were cut out from the bulk. These wafers were almost transparent and observed by optical microscope (transmission mode) to investigate the PD distribution in the wafers. In each wafer, nine points were measured from the edge to the center.

Though the shape of PD was all hexagon, not all PD were regular hexagon, e.g. distorted hexagon, triangle, parallelogram and so on. The larger crystal grew, the less PD density (PDD) became. The PDD at the edge region was almost same as that at the center region. The MP density of the edge region was less than that of the center region.

Figure1 shows the distribution of PD size (PDS) in each wafer. The PDS close to the substrate was smaller than that near the surface. The PDS was smaller at the edge region than that of the center region. Before the growth, the growth surface was flat. On the flat surface, crystal grew mainly toward c-axis direction, and PD expansion was restricted. However, as crystal grew larger, growth surface became convex. In this case, growth toward a-axis direction became rapidly. So, in this region, PD was easily expanded laterally.

At several points, MP annihilation by PD was observed. There were three ways of MP annihilation, i.e. the annihilation of MP under PD at the center region of PD, at the edge region of PD and adsorption of MP out of PD at the edge region of PD.

Characterization of wafers by X-ray diffraction, Raman spectroscopy and KOH etching will be presented.

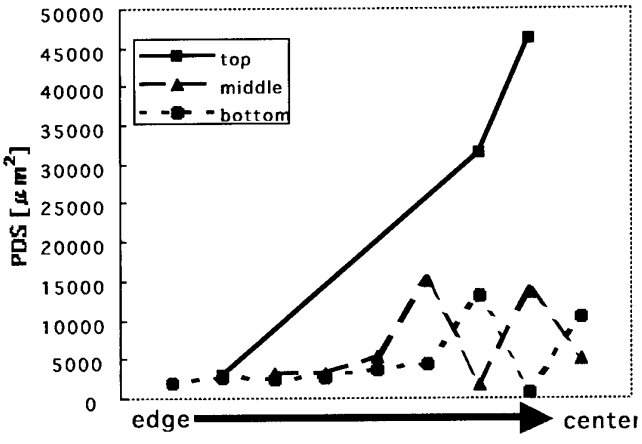


Figure1. The distribution of PDS in SiC wafers

The investigations of 4H-SiC/SiO_2 interfaces by optical and electrical measurements

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The channel mobilities of silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs) reported so far are much lower than the value expected from the bulk mobility. Many studies have been carried out to resolve these problems, nevertheless, the origin which lower device characteristics has not been clarified yet. In this report, we have examined SiC/SiO_2 interfaces by optical and electrical measurements to make clear the structures of the interfaces.

Epitaxial wafers of 4H-SiC with 8° off-oriented (0001) Si face and n type were used for the measurements. Thermal oxides were grown in pure O_2 ambient at 1200 °C. Simultaneous capacitance-voltage (C-V) measurement, Fourier-transformed infrared reflection absorption spectroscopy (FTIR-RAS) and spectroscopic ellipsometry were carried out as electrical and optical measurements, respectively. For the optical measurements, the samples were etched at an angle by dipping gradually into diluted hydrofluoric acid at a constant speed. FTIR-RAS and ellipsometric measurements were performed along the slope of the oxides films to obtain the data as a function of oxide thickness.

From C-V measurements, number of interface traps per unit area (N_{it}) were obtained to be over 7×10^{12} cm^{-2} and the shift of flat band voltage (V_{fb}) was +18 V. The apparent refractive indices derived from the spectroscopic ellipsometric measurements under the assumption that the oxide films have uniform refractive indices, do not constant but decrease with oxide film thickness, especially in the region below 10 nm in thickness. This change can be explained by the model that there exist interface layers with higher refractive indices than those of SiO_2 and SiC. Figure 1 shows the results obtained from FTIR-RAS measurement. The peak position of Si-O-Si stretch TO modes shifts to lower frequency in the region below 5 nm in thickness of oxide layers and the values become away from that of fused quartz. These results indicate that transition layers exist at the interface between SiC and SiO_2.

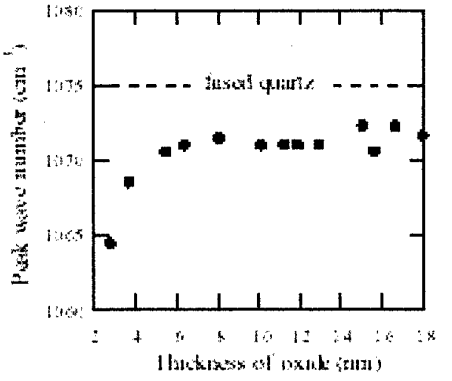


Fig. 1 Peak wave number of TO mode as a function of oxide thickness.

Growth and characterization of three-dimensional SiC nanostructures on Si

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SiC is known to be a promising candidate for high power, high temperature and high frequency devices. SiC based nanostructures could result in new and improved properties, phenomena, and processes and thus expand the potential to new optical, high-frequency and photonic applications.

In this work we present a study of morphological properties of SiC islands on Si and of three-dimensional SiC-Si nanostructures. SiC was grown on (001)Si by a pure carbonization process in a molecular beam epitaxial system using an electron gun evaporator as carbon source. At constant temperature, the SiC islands were generally growing in a three dimensional mode. At high temperatures above 800°C the nucleation density was increasing up to an effective coverage of around one tenth of a monolayer and remains constant after. The need of Si for the SiC formation as well as the Si evaporation results in a depletion of the area surrounding the SiC islands. As a result well resolved pyramids with a four fold symmetry are forming on on-axis substrates with SiC nuclei on the top. These pyramids are tilted on off-axis substrates and therefor non-symmetric. The SiC islands are growing downwards along the four edges, forming facets and maintaining the symmetry of the pyramids. In contrary, at low temperatures islands are growing faster laterally in a quasi two dimensional mode resulting in an early coverage of the surface and preventing the formation of pyramids. The size of Si pyramids can be enhanced by pre-deposition of 1 ML Ge prior to the carbonization. The saturation nucleation density in dependence on temperature, carbon flux and Ge pre-deposition was estimated and the activation energies extracted. Possible applications for the high-temperature-grown three dimensional SiC-Si structures will be discussed.

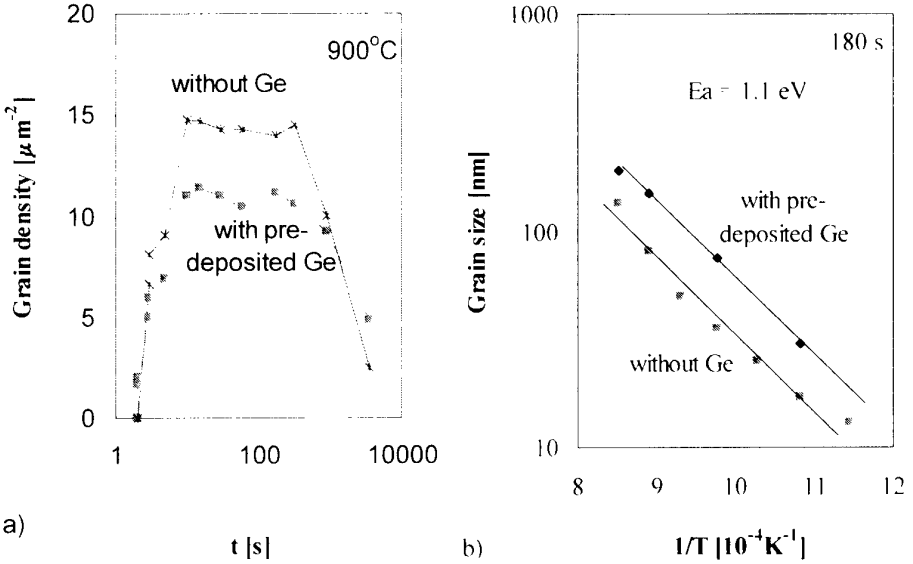


Fig. 1 Evolution of SiC islands on Si at a carbon flux of 10^{-13} $cm^{-2}s^{-1}$: a) Grain density versus time at 900°C and b) Grain size versus growth temperature after 180 s growth.

Characterization of 2 inch as Grown SiC Bulk by SWBXT at SPring-8

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There are few reports of research of SiC as grown bulk crystal without the surface morphology. So, we could research SiC bulk crystal using facilities at SPring-8 (BL28B2). Since the SR beam at SPring-8 has 8GeV electron beam energy, SR beam transmits even 2-inch SiC bulk crystal and we can observe SWBXT (Synchrotron White Beam X-ray Topography). We prepared 2-inch 6H-SiC bulk, which was made by sublimation method on (0001) 6H-SiC substrate. The height of sample is about 22mm and the shape is shown in Fig.1. The distance from sample to the film is about 300mm, the exposure time is a few seconds. The directions of incident beam were <1-100> and <11-20> and the size of incident beam was 2mm x 2mm. The Laue pattern was 2 fold symmetry and the Laue spots became rectangle. We can investigate defects easily by the Laue pattern and spots. If the sample is perfect 6H-SiC crystal, these Laue spots have no contrast. But if the defects exist in the crystal, Laue spots are inhomogeneous.

Fig.2 and 3 show the Laue pattern and topography. The contrast of Laue spot of the sample was enlarged as shown Fig.3. The incident direction and diffracted planes were <1-100> and (11-20).

Since the shape of bulk crystal is like Fig.3, the transmission length and the length of topography image are different by the measurement points.

From this figure, the contrast decreases as growing and the image of Fig.3 (c) undulates <0001> direction. We can confirm the defects in the crystal decrease as growing.

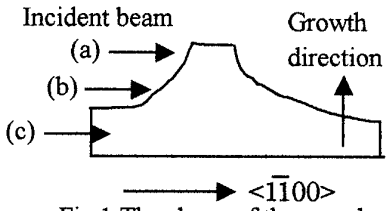
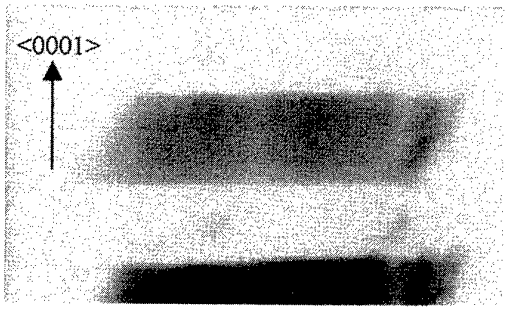
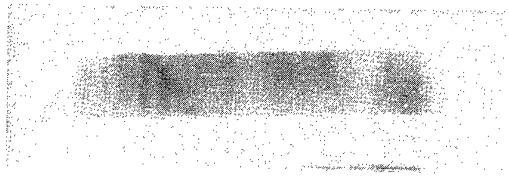
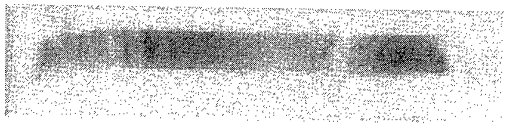


Fig.1 The shape of the sample



(a) near the surface of bulk


(b) side of bulk


(c) near the bottom area of bulk

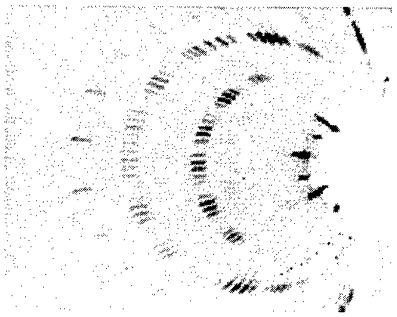

Fig.2 Laue pattern of 6H-SiC bulk crystal

Fig.3 Topography of 6H-SiC bulk crystal

The neutral silicon vacancy in SiC: Ligand hyperfine interaction

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The silicon vacancy V_{Si} in SiC is of great interest both theoretically as one of the fundamental intrinsic defects and practically, because it is created in device processing steps like ion implantation. V_{Si} can exist in various charge states within the band gap, but a definite chemical identification has so far only been possible for the negatively charged silicon vacancy. This was possible by the observation of ligand hyperfine interaction with ^{13}C atoms in the nearest-neighbour (NN) shell and with ^{29}Si atoms in the next-nearest-neighbour (NNN) shell in electron paramagnetic resonance (EPR) experiments.

The neutral silicon vacancy has been observed in optically detected magnetic resonance (ODMR) experiments in electron irradiated samples when either one of the photoluminescence (PL) bands in the near infrared called V1, V2 and V3 in 6H SiC and V1, V2 in 4H SiC was resonantly excited with a Ti:Sapphire laser [1]. This number of lines arises from the corresponding number of inequivalent lattice sites on which the defect can reside in the two polytypes. A spin triplet state with the characteristic hyperfine signature of the NNN ^{29}Si atoms was observed by monitoring each PL band. However, due to low signal intensity the hyperfine interaction with the ^{13}C atoms (only 1.11% natural abundance) in the NN shell could not be resolved. Already in the 1980's triplet EPR signals with a similar crystal field splitting had been observed after the samples had been illuminated [2]. At that time the signals were attributed to distant vacancy pairs. More recently such lines were reported even in EPR experiments in dark, even though there the spectra were dominated by the signal from the negative charge state of the silicon vacancy [3]. No ligand hyperfine interaction could be resolved.

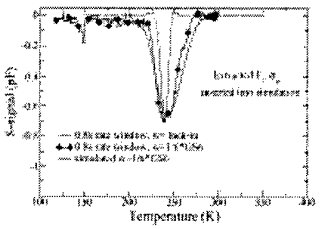
New ODMR experiments on a ^{13}C isotope enriched sample and on high quality epitaxial films now revealed these ^{13}C hyperfine lines. The hyperfine parameters of $A_{\|}^{C} \approx 28$ G and $A_{\perp}^{C} \approx 11$ G (with slight variations depending on polytype and lattice site) for interaction with the NN ^{13}C-atoms and $A^{Si} = 3.0$ G (isotropic) for the NNN ^{29}Si-atoms are very similar to the ones found for the silicon vacancy in its negative charge state. This confirms that the spin triplet observed in ODMR originates from the 'isolated' silicon vacancy.

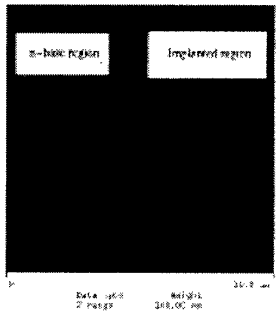
References:
[1] E. Sörman, N. T. Son, W. M. Chen, O. Kordina, C. Hallin, and E. Janzén, Phys. Rev. B **61**, 2613 (2000).
[2] V. S. Vainer and V. A. Il'in, Sov. Phys.-Solid State **23**, 2126 (1981).
[3] H. J. von Bardeleben, J. L. Cantin, I. Vickridge, and G. Battistig, Phys. Rev. B **62**, 10126 (2000).

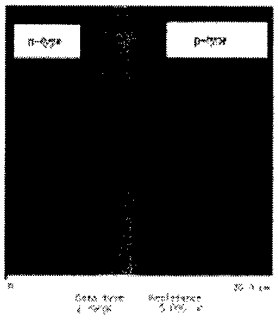
The deep boron level in high voltage pin diodes.

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Well behaved high-voltage (3.5 kV blocking voltage) 4H-SiC pin diodes were examined with respect to implantation induced electrically active defects using deep level transient spectroscopy (DLTS), admittance spectroscopy, capacitance-voltage measurements, atomic force microscopy and the new scanning spreading resistance technique (SSRM). The material used was 35 μm thick epitaxial n-type 4H-SiC layers grown on commercial Cree wafers by chemical vapor deposition. The nitrogen doping in the epitaxial layers were in the low 10^{15} cm^{-3} region. The diodes were manufactured with a shallow high concentration (10^{20} cm^{-3}) aluminum implantation and a deeper box profile of implantated boron of intermediate concentration. After the annealing process the metallurgical junction seen by secondary ion mass spectrometry SIMS displayed a "soft" junction character with an in-diffused boron tail of several micrometers. In the junction region a deep hole trap was found to dominate the metallurgical pn junction at room temperature (RT). High resolution DLTS weighting functions were used and the trap identified as the boron related D-level. This trap level effectively removed free carriers (holes) causing the in-diffused boron tail of the profile to become intrinsic. SSRM confirmed the existence of an intrinsic region where the boron had diffused into the material. By activating the trap level at temperatures *geq*600 K the junction behaved as a low doped soft junction without an intrinsic region. The electrical measurements together with the chemical boron profile gave at hand that less than 10% of the in-diffused boron resides on substitutional sites forming shallow boron acceptors. The D-level operates as a hole trap.







The figures show: top) DLTS spectra of a reverse biased diode showing the D-center, center) Topography of the are between implanted and unimplanted diode using atomic force microscopy, bottom) SSRM of same region. The bright contrast shows the intrinsic region where a large fraction of the boron has diffused and formed D-centers that effectively traps the holes in this region.

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Growth of AlN films by Hot-Wall CVD and Sublimation Techniques: effect of growth cell pressure

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The demand of using AlN in many applications such as short wavelength optical devices and SiC based FETs is increasing but the perfection of the films is still limited mainly due to the difficulty of N incorporating, the strong reactivity of Al, gettering impurities from the ambient, and the lack of lattice matched substrate material. A lot of efforts have being directed towards developing better AlN synthesis methods but still the route to device quality material is not clear.

In this study hot-wall CVD and sublimation epitaxy were used that can provide high growth temperatures advantageous for the AlN deposition. The pressure inside the growth cell can influence the growth of AlN films and their properties such as thickness, morphology, and luminescence. In the CVD experiments the growth cell pressure was set to 1000, 100 and 50 mbar while the temperature was kept at 1200°C. Sublimation growth process experiments occurred at temperature of 2100°C at the source under nitrogen pressure of 200, 500 and 900 mbar. Characterization techniques used were SEM, cathodoluminescence (CL) and infrared reflectance.

At low growth cell pressure in the CVD experiments thick AlN layers with smooth surfaces, which produce interference fringes in the reflectance spectrum (Fig. 1, 50 mbar) were obtained. AlN films grown by sublimation consist of grains with height of up to 90 μm (Fig. 2). The change of the pressure at this temperature does not influence substantially the microstructure of the sublimation grown films except for the enlargement of the grains.

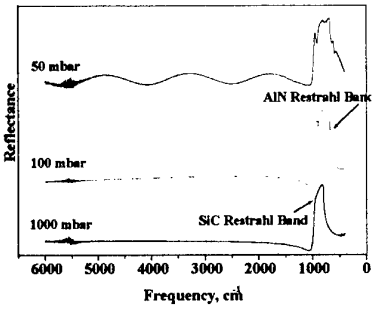


Fig. 1 Infrared Reflectance of AlN CVD layers grown at different cell pressure

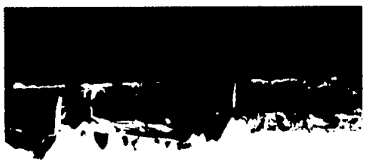


Fig. 2 SEM image in cross-section taken from the sublimation grown layer at 200 mbar

CL panchromatic images with boundaries of dark contrast were taken from the films produced in either of the two deposition methods. Our results show that under conditions of moderate growth cell pressure (100 mbar in the CVD and 200 mbar in the sublimation experiments) both processes give good quality material AlN films in which the near band edge emission in the CL spectra appears.

A method of reducing micropipe using metal mask by the sublimation growth

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The silicon carbide substrate produced by the modified Lely method generates a lot of micropipe in the growth process even if lely crystal was used for a seed crystal. And the Lely method cannot obtain large diameter substrate.
For this reason when we produce the large diameter substrate, the crystal with many defects enlarged from the Lely crystal needs to be used as a seed.
Since the micropipe propagates to the grown crystal, it is difficult to reduce the micropipe.
In this study, we tried to use metal mask to cover the micropipe. This way seems to be similar to the epitaxial lateral over growth method that can reduce the spiral dislocation, by forming and carrying out lateral over growth on the mask.

The modified Lely crystal was used for seed crystal with a thickness of 0.8mm.
After the seed crystal was performed organic washing and acid washing, the metal mask was formed by the electron beam deposition method.
The metal used for deposition is W and Pt and the thickness of mask is 0-100 Å.
Then, the modified seed crystal was fixed to the graphite lid.
The graphite crucible was filled up with SiC powder, and was overheated to 2200 degrees C with the graphite lid.
The growth pressure was 100Torr.
The grown crystal was evaluated by the polarizing optical microscope.

Figure 1 shows the cross-sectional transmission microscope photograph near the interface of a seed crystal and a growth crystal with the thickness of the metal mask about 100 Å.
It was clearly shown that micropipe stops at the interface between seed crystal and grown crystal, on both W and Pt cases.
The micropipe density was measured with a polarizing optical microscope.
We confirm that the micropipe density in grown crystal decreases 50% than the micropipe density in seed crystal..

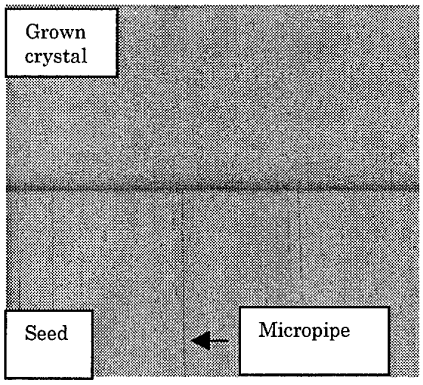


Fig.1 Cross-sectional photograph of the crystal using platinum

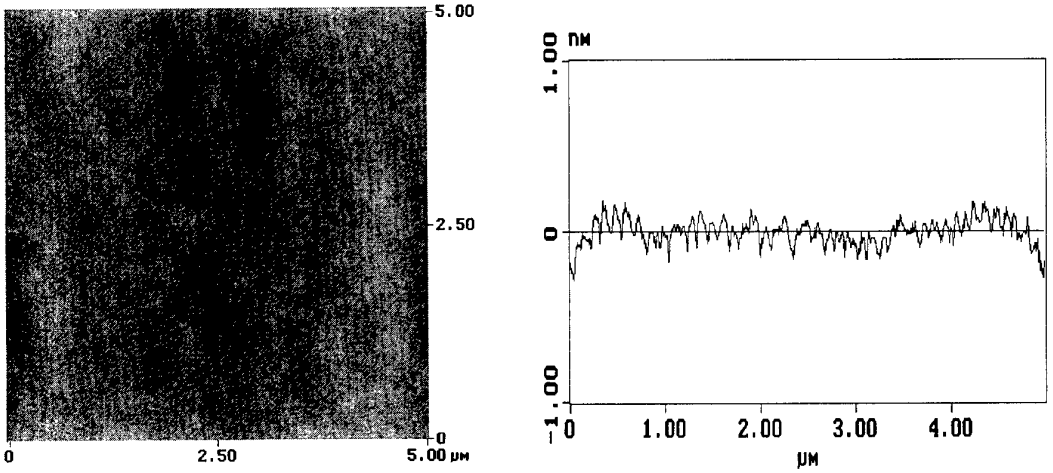
Atomic steps observation on 6H and 15R-SiC polished surface.

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6H-SiC bulk is widely used as a substrate for growth of III-Nitride epitaxial layers The smaller lattice mismatch between GaN and SiC compared to GaN and sapphire, and the high thermal conductivity makes 6H-SiC a promising substrate for nitride growth. Surface preparation before the epitaxial growth is a critical step, because every defect on the surface of the substrate is a potential source for a defect in the epitaxial layer. In a similar way, the surface roughness can be a limiting factor for the roughness of the epitaxial layer surface. The most recent SiC polishing process, produces atomically flat surface, free of scratch and damaged layer [1].
Figure a) shows with Atomic Force Microscopy the presence of atomic steps on a 0° 8' off axis 6H-SiC surface (with 1.5 Å RMS roughness). Figure b) shows the corresponding profile through the steps (with step of about 2.5 Å in hight and 110nm in length).

a) b)



Due to an advanced polishing surface preparation, bi-layer atomic steps has been revealed both on 6H and 15R-SiC. By synchrotron X-ray topography, Raman spectroscopy and atomic force microscopy we have established the strong correlation between the polished surface and the bulk crystalline quality. For instance, grain tilt and twist can be evidenced by step length and direction.

[1] J. Camassel, P. Vicente and L. Falkovski, *Optical Characterization of SiC Materials: Bulk and Implanted Layers*, Materials Science Forum Vols **353-356**, 335 (2000).

CVD SiC powder for high purity SiC Source material

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Recently, the need to the high purity SiC source material has been increasing in order to grow high quality SiC single crystal.

SiC powder which made by Acheson method has been used basically as this kind of raw materials and has been applied for abrasives and refractory.However the current powder has no cleaning way other than acid dipping or some similar treatment. Lots of reseachers studying single crystal SiC have been noticing the limitation of purity in the current raw material. Thereupon we developed high purity CVD-SiC powder for single crystal SiC. This powder is made from CVD-SiC polycrystal plate by crushing it directly. The result of the purity of the powder (A) is quite good rather than current powder(B) especially in Fe, Ni,Al,Ti as shown in Table 1.

As shown in Fig.1, the powder diameter distribution ranges from 1000 micron to 200 micron in powder(A) and 200 micron to 50 micron in powder(B). This powder source(A) will be a good precursor for getting sinlge crystal SiC by sublimation method.

Table 1: Impurity of SiC powder (by ICP-AES)

Powder type		Elements(ppm)										
		Fe	Ni	Ca	Al	P	B	Na	K	Ti	V	Zr
(A)	CVD-SiC powder after crushing [*1]	0.1	0.1	0.1	0.1	<0.1	<0.1	<0.1	<0.1	<0.1	0.1	<0.1
(B)	High Purity SiC powder by Current Acheson method [*2]	5	0.8	0.5	14	<0.1	<0.3	0.4	<0.1	3.5	0.7	0.4

[*1]3C-SiC beta type [*2]6H-SiC alpha type

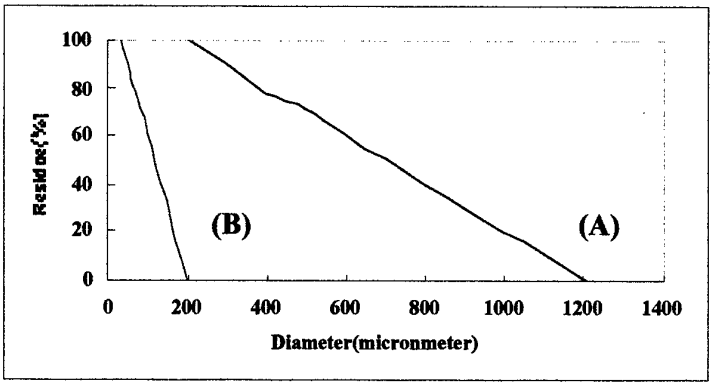


Fig.1 : Powder diameter distribution

PLD BN as an Annealing Cap for Ion Implanted SiC

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Planar SiC devices are fabricated using ion implantation because the rates of diffusion of dopants into SiC are too low even at temperatures as high as 1800°C to be technologically useful. The implanted dopants have to be activated by a high temperature anneal, and at the temperatures at which the dopants are activated, silicon evaporates preferentially from the SiC lattice. We have shown that the activation of the n-type dopant, nitrogen, is essentially complete at 1600°C with no surface degradation due to silicon evaporation when we used an AlN cap[1]. However, at temperatures > 1600°C the AlN evaporates creating hexagonal holes through which the silicon can now preferentially evaporate[2]. Unfortunately, the p-type dopants, Al and B, require temperatures at least as high as 1700°C for their complete activation[3]. Thus, a cap must be found to withstand temperatures this high and still retain the necessary qualities of the AlN cap, which are: 1) retains coverage of the SiC surface during the anneal, 2) does not react with the SiC surface during the anneal, and 3) can be removed selectively without harming the SiC surface after annealing.

We show that such a BN/AlN cap can withstand these temperatures and retain the properties of the AlN cap. This cap is created by depositing a ~200 nm AlN film by pulsed laser deposition (PLD) followed by the PLD deposition of ~300 nm BN film. The cap is removed after the anneal by ion milling the BN off, and then selectively etching away the AlN film in warm KOH. The structure of the SiC surface is then examined with a SEM and AFM, and the surface chemistry is studied by AES.

To better understand the cap properties, we recorded the surface structure of the BN with a SEM and AFM; checked for chemical intermixing at the interfaces and surface contamination of the SiC surface using AES, and examined the cap structure using FTIR spectroscopy and XRD. We are currently looking at the structure with TEM and will report the results at the meeting. Briefly, the results show that the BN film remains intact during the anneal and no intermixing of the BN and AlN films or AlN film and SiC substrate occur. We do not yet know to what extent the BN film has crystallized, but we expect the TEM results will tell us that.

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Growth characteristics of SiC in a hot-wall CVD reactor with rotation

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Rotation has been implemented in a horizontal hot-wall reactor for SiC CVD by means of gas foil levitation [1]. The bottom part of susceptor has been redesigned to carry a rotating disk with a capacity of three 2" wafers. The capacity of the reactor is three 2" wafers. Argon or hydrogen is used as the rotating medium and the rotation rate is maintained fast enough for growing thin MESFET structures. The CVD process is similar with the one previously described in [2].

Smooth surface without any decoration of dislocation defects has been achieved, after the substrate is raised slightly above the susceptor floor: the lifted-disk rotation. Under non-optimized conditions, particles are observed on the epilayer surface, presumably caused by gas phase nucleation. The best thickness uniformity has been obtained without lifting up the substrate, with 0.36% and 0.92% for 35 mm and 2" wafers, respectively. N-type doping uniformity as good as 1.35% on a 35 mm wafer has been achieved with un-lifted disk rotation as well. The good morphology in the lifted-disk rotation has been compromised by the slightly worse uniformity. However, thickness and doping uniformity values can still be as good as 6% and 7.7%, respectively for a 2" wafer. Both the intra-wafer and the run to run doping uniformities are less than □10%. Both n- and p-type doping is readily achieved. The n-type doping ranges from $5 \cdot 10^{15}$ cm^{-3} to $2\ 10^{19} \cdot cm^{-3}$, and p-type doping between $5 \cdot 10^{15}$ cm^{-3} and $5\ 10^{18} \cdot cm^{-3}$ has been obtained. MESFET structures have been grown on semi-insulating substrates with excellent doping control.

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On shallow interface states in *n* type 4H-SiC metal-oxide-semiconductor structures

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The unacceptably low electron channel mobility currently observed in 4H-SiC metal-oxide-semiconductor field-effect transistors is of major concern. A possible reason for this mobility reduction is considered to be the high density of interface states near the conduction band edge of 4H-SiC. Using capacitance-voltage (CV) analysis the interface state density as a function of energy has been estimated and is found to increase rapidly towards the conduction band edge [1].

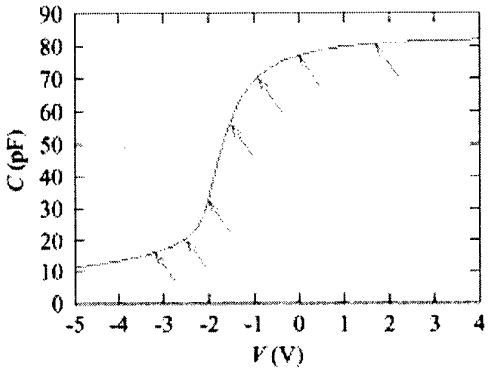


Fig. 1: A quasi-static CV measurement at 300 K for an *n* type 4H-SiC MOS. Arrows show the charging levels used in Fig. 2.

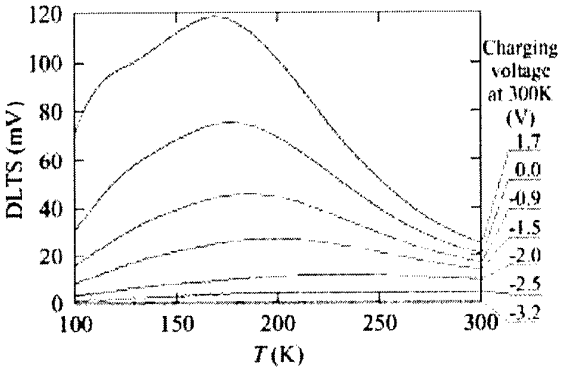


Fig. 2: DLTS spectra for an *n* type 4H-SiC MOS, measured for several charging levels. The discharging voltage is -5 V at 300 K.

In this work we examine shallow interface states by using constant capacitance deep level transient spectroscopy (DLTS) on *n* type 4H-SiC metal-oxide-semiconductor (MOS) capacitors. Fig. 1 shows a quasi-static CV measurement at 300 K. Fig. 2 shows that the DLTS spectrum measured at 1 Hz reveals an interface state peak at 170 K which grows as the charging level increases. This peak has an activation energy of approximately 0.12 eV and a number density that exceeds 10^{12} cm^{-2}. Capture rate data reveals that these interface states are slow, exhibiting a very small electron capture cross section in the range of $10^{-22} - 10^{-24}$ cm^2 at 170 K. Furthermore, we find similar traps in differently prepared oxides. In summary, slow interface oxide traps are observed whose distribution as a function of energy is a peak near the conduction band edge of 4H-SiC. These traps are possibly a signature of the native oxide defect described by Afanas'ev *et al.* [2]

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The Effect of epitaxial growth on warp of SiC wafers

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1.Introduction

Before the routine development of SiC devices can be claimed, many technological problems remain to solve. One of them is the warp of wafers. Especially, when the diameter of wafers is enlarged, it is necessary to pay attention. Tuchida et al.[1] reported that the epitaxial growth process improved the crystal bending. We investigate the effect of epitaxial growth process on the warp of SiC wafers. In this report, we performed the hydrogen etching and the epitaxial growth process on the wafers with the large warp and proposed the origin of the warp.

2.Experimental

We carried out hydrogen etchings and 4H-SiC epitaxial growth under 700Torr at 1500℃ in our Hot-Wall CVD reactor. In the hydrogen etching, the wafers were exposed to 5SLM hydrogen gas for 5min. The epitaxial growth occurred using 2.5sccm silane and 1.2sccm propane in 5SLM hydrogen carrier gas for 1h. We measured the warp of the wafer after the processes. In each process, we used one-side (Si face or C face) polished wafers. We also measured the warp of the wafers before and after polishing.

3.Result and Discussion

Table 1 shows the curvature radius of wafers after each step. Both Si-face and C-face became concave after polishing. This indicated that the polishing process induced the internal stress. After the hydrogen etching, an improvement in the warp of wafers was confirmed, because the hydrogen etching reduced the stressed layer caused by mechanical polishing. The slightly convex surface was observed due to the overpolishing of a few microns at the periphery of the wafers. Further improvement of the warp was confirmed on the Si-face after epitaxial growth (the typical carrier concentration is $7\times10^{15}cm^{-3}$ and the typical thickness is $4.5\,\mu m$). On the other hand, C-face became convex after epitaxial growth. Because the growth condition was optimized only for Si-face, not for C-face, the internal stress was supposed to be introduced in the C-face epitaxial layer

Table 1 The curvature radius after each step

		before polishing	after polising	after process
Epitaxial Growth	Si face	—	6.9m	80m
	C face	63m	11m	-6.5m
Hydorgen Etching	Si face	87m	8.1m	-31m
	C face	57m	6.6m	-21m

4.Summary

We performed the hydrogen etching and epitaxial growth on Si face and C face of the 2inch SiC wafer and measured the warp of them. We confirmed the improvement of the warp after hydrogen etching and the further improvement on Si-face after epitaxial growth.

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Infrared investigation of implantation damage in 6H-SiC

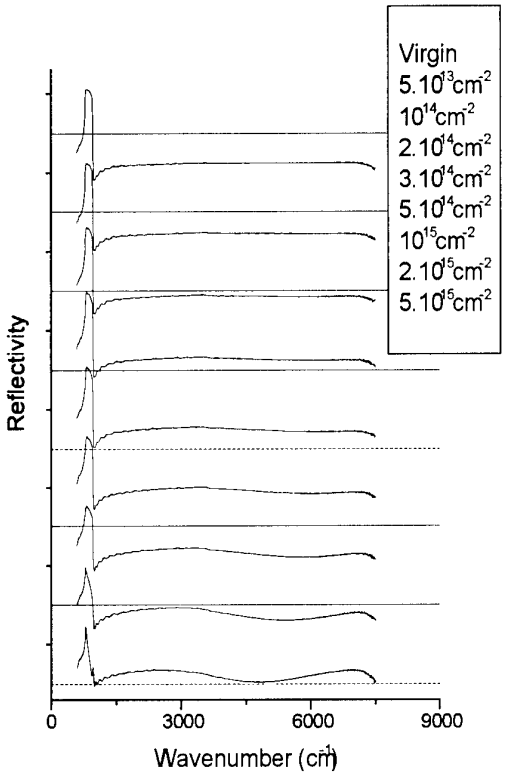
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We present the results of an infrared (IR) investigations of the effect of implantation damage on the reststrahlen band of 6H-SiC implanted with N^+-ions. The implantation energy was 160 keV and the implantation temperature 300K. The dose ranged from 5 10^{13} to 5 10^{15} cm^{-2}. After implantation IR reflectivity spectra were collected at room temperature in the middle infrared range, from 500 to 7500 cm^{-1}. We used a Brucker IRTF spectrophotometer fitted with a microscope and a MCT detector. Results are shown in Fig.1.

They demonstrate the following :

- i°) a decrease and broadening of the topmost reflectivity structure versus implantation dose. This comes from implantation damage and shows that, even if one focus only on the reststrahlen band, IR reflectivity constitutes a most sensitive tool to probe, on-line, the implantation damage ;
- ii°) a change in refractive index of the topmost (implanted) layer with respect to the host material. This change is dose-dependent and, at high dose, results in the appearance of a new (large) set of interference. This is again an useful tool to probe the in-depth extension of damage ;
- iii°) finally at very high dose (~ 5 10^{15} cm^{-2}) a new (sharp) extra feature reveals, close to the LO frequency of bulk SiC [1]. It comes because of a strong change in the optical properties of the implanted material with appearance of a new (no longer pure SiC-like) effective medium.



We have modelled our IR spectra with the use a transfer matrix method [2] and product oscillators [3]. Results will be discussed in great details.

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TCAD optimisation of 4H-SiC channel doped MOSFET with p-polysilicon gate

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Abstract

In this paper the optimisation of structure of the channel doped MOSFET, with p-polysilicon gate based on 4H-SiC is studied using TCAD simulation. It is known that the channel mobility of the depletion mode of Al-gated C-MOSFET is improved by increasing the channel doping level but that this leads to a decrease in threshold voltage, Vth [1,2]. Since p-polysilicon has higher workfunction than Al or n-polysilicon gate, which results in higher Vth, p-polysilicon gate is expected to allow further improvement of the channel mobility by increased channel doping.

The device structure used is based on a $5x10^{15}cm^{-3}$ Al doped p-type substrate, gate width of 5um, tox of 50nm, source and drain doped with Phosphorus with depth of 0.5um, channel doping with Nitrogen, a surface trapped charge density of $1x10^{11}cm^{-2}$ and a fixed charge density in gate oxide of $1x10^{17}cm^{-3}$. The p-type and n-type Polysilicon gate material is doped with Boron and Phosphorus of $1x10^{19}cm^{-3}$ respectively, and their workfunctions calculated from the doping level. The channel doping concentration and depth are optimised to achieve maximum mobility in the enhancement mode MOSFET.

Fig.1 shows that Vth decreases with increasing channel doping concentration, Nc, and depth of channel. When the product of Nc and depth exceeds $7.5x10^{11}cm^{-2}$ Vth becomes negative, i.e. depletion mode. In the case of enhancement mode, the best mobility is gained at Nc of $2x10^{16}cm^{-3}$ and depth of 0.2-0.3μm (Fig.1, 2). Electron distribution from the surface to the bulk clearly shows that the available channel conduction electron density increases with Nc (Fig.3). Fig.4 shows a comparison of mobility between gate materials with different workfunction. At the same Vth, n-polysilicon and AL gate show almost the same mobility (due to similar workfunction), while the p-polysilicon gate has about $50cm^2V^{-1}s^{-1}$ higher mobility. At a threshold voltage of 1V this represents a factor of 2 improvement, thus demonstrating the potential for improved performance with a p-polysilicon gate.

The final paper will report a new type of channel mobility model, which is based on the density of interface states, D_{IT}, and the modeling of surface deep levels. This model seems to have good agreement with experimental data. It is believed that the model is the best way to describe the SiC chennel mobility because the main cause of low mobility is high D_{IT}.

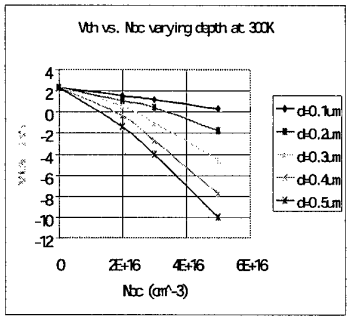


Fig.1 Vth vs. Nc with depth

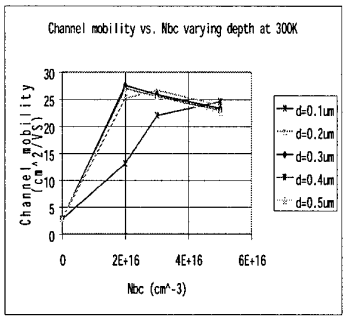


Fig.2 Mobility vs. Nc with depth

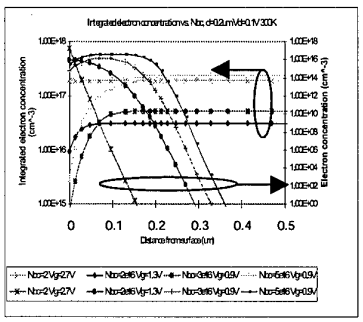


Fig.3 Electron concentration

Acknowledgement

This work was performed under the management of FED as a part of Ultra-Low Loss Power Device Technology Project supported by NEDO and was supported in part by the UK Engineering and Physical Sciences Research Council under research grant GR/L62320.

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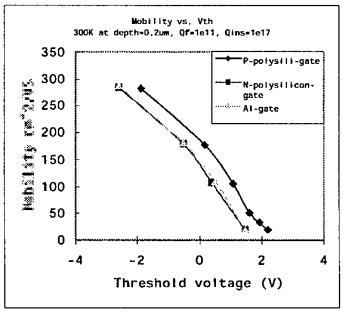


Fig.4 Mobility

Theory of Super-Junction Structure Forward Characteristics and Comparison of 4H-SiC and Si

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Abstract

Super-junction structure (SJS) can realize very low on-resistance in Si [1] and 4H-SiC [2] FET devices. The practical limits to device operation are, however, determined by a combination of the electrical characteristics of the device and the thermal constraints of the device and packaging technology. In this paper a formula for the forward drain current density (Jd) versus on-state voltage (Von) taking account of the built-in potential (Vbi) and the doping imbalance error between pillars (err=Na/Nd-1) is developed. Von and the product of Jd and breakdown voltage Vbr are studied and comparisons made between 4H-SiC and Si.

The relationship between Jd and Von is derived from junction field effect transistor (JFET) theory [3] in which the p-pillar acts like the JFET gate. The resulting relationship gives good agreement with TCAD at low voltage in the area of on-state (Fig.1).

The maximum package power dissipation is assumed to be 500W/cm^2 for Si and 1000W/cm^2 for SiC. Von is taken from the value where the Jd-Von line and the power line (Jd*Von) cross. In the case of an optimized structure and with the limitation of a minimum pillar width of 1um for realistic condition, we have found that Von remains same at low voltage and low imbalance error (Fig.2). With err=0.1 SiC 720V and Si 72V devices have about 0.2V and 0.3V Von respectively, and are both about half values of conventional FET devices at the same power dissipation. SiC 7200V and Si 720V devices display Von values of about 2V and 4V respectively (one third of conventional devices).

Jon*Vbr (switched VA product) versus Vbr (Fig.3) is one good way of measuring device performance. Fig.3 shows that for SJS the VA product increases in proportion to the square root of Vbr, while for conventional FET devices it decreases. This demonstrates the excellent performance potential of SiC SJS.

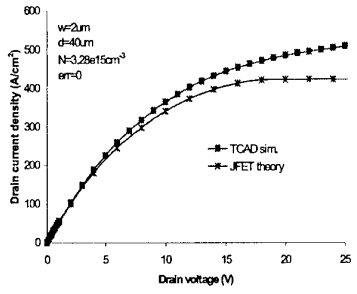


Fig. 1

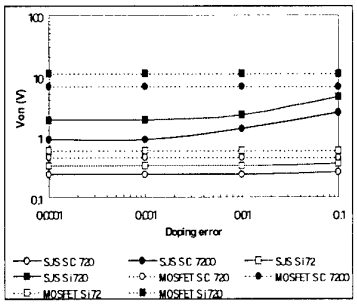


Fig.2

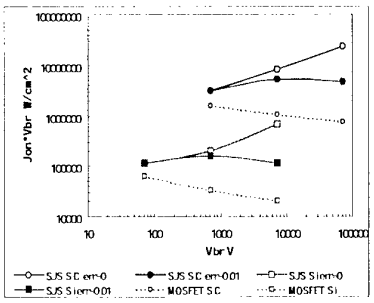


Fig.3

Acknowledgement

This work was performed under the management of FED as a part of Ultra-Low Loss Power Device Technology Project supported by NEDO and was supported in part by the UK Engineering and Physical Sciences Research Council under research grant GR/L62320.

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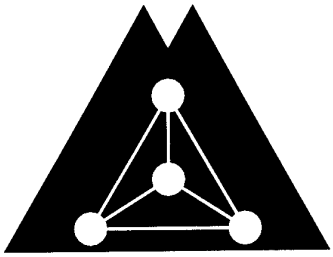
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