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MATERIALS DATA AND THEORY FOR ELECTRON EMITTERS

Design of Wideband Microwave Amplifiers Based on a Combination of Heterojunction Bipolar Transistors, Cold Cathodes, and Coplanar Waveguide Technologies

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Prior to the start of this research effort, we had investigated the effects of direct current (DC) current crowding across the emission window of an indium phosphide/cadmium sulfide/ lanthanum sulfide (InP/CdS/LaS) cold cathode shown in Figure 1 when a DC bias is applied across the CdS layer. In references [1,2], it was shown that, because of the trapping of electrons in the LaS thin film and the finite resistivity of the LaS thin film, current crowding effects can be minimized by keeping the width of the emission window W_E (Figure 1) under 50 μm while keeping the emission current density below 100 A/cm^2.

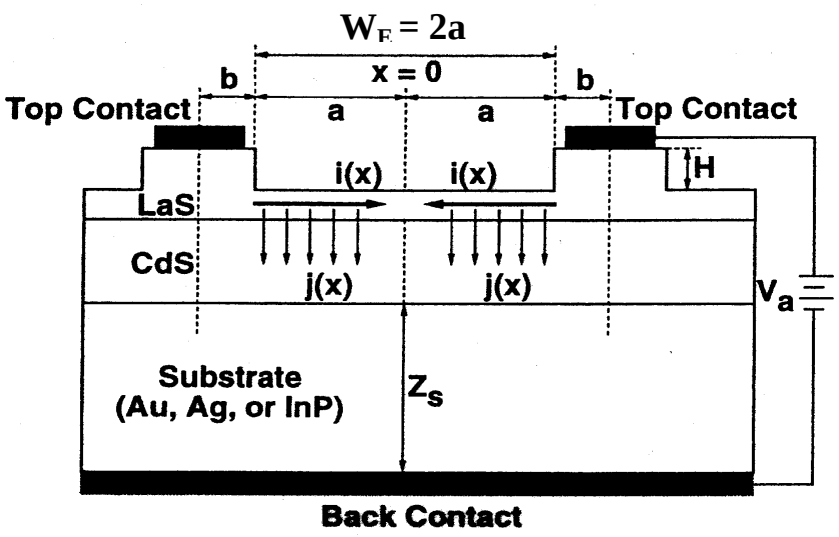


Figure 1. Cross Section of Cold Cathode Structure with Two Emitter Fingers.

During this research effort, we have extended this analysis to the case where an alternating current (AC) signal is superimposed on top of the DC signal across the CdS layer. Hereafter, we assume that the biasing conditions and geometrical parameters of the cathode are such that the effects of DC current crowding are negligible and study the effects of a small AC voltage across the CdS on top of some DC bias. The goal was to study the frequency dependence of AC current crowding effects. Since we wanted a cold cathode operating in the X-band (10 GHz (gigahertz)), we had to address the issue of uniformity of the emission current at such a high frequency of operation. If the cathode could be designed such that the AC emission current is uniform, the cathode could then be used for application in traveling wave tubes (TWTs) with a prebunched beam.

Our first approach was to design a first order model following the bipolar microwave linear power transistor design method reported by Chen and Snapp [3]. In this approach, the cathode was modeled using the transmission line model shown in Figure 2 to include the finite resistivity of the LaS thin film, and the unit area shunt conductance and shunt capacitance of the CdS layers. The effects of the finite transit time for electron to cross the CdS layer was neglected. This is a good approximation since the CdS layer is assumed to be at most a few 100 A thick in our numerical simulations. The transit time through the CdS layer is therefore expected to be of the order of a picosecond (ps) or less.

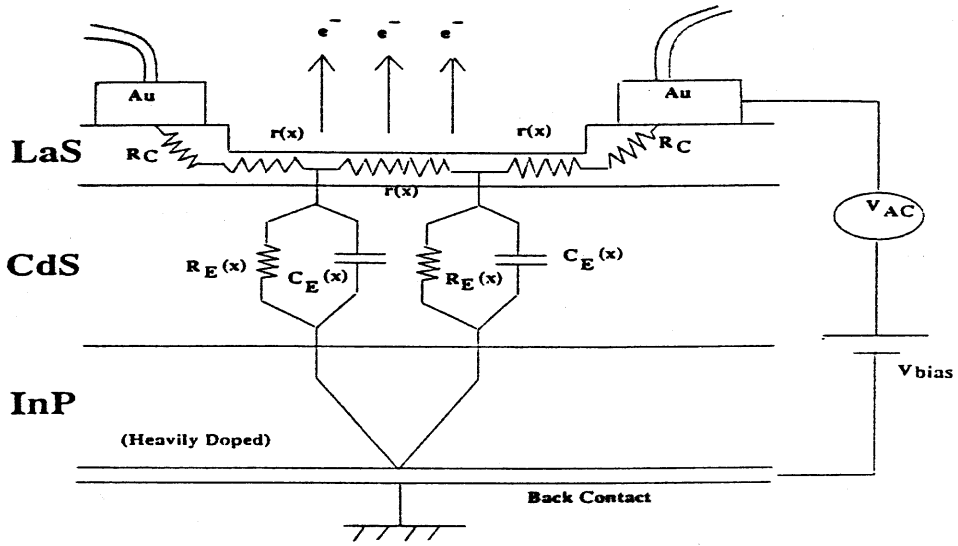


Figure 2. RC Transmission Line Approach to Calculate the Emission Efficiency of the Cold Cathode Structure When Operated with a High Frequency, Sinusoidal Voltage Source in Addition to the DC Bias V_{bias}.

Assuming a linear mode of operation, the expression for the microwave voltage across the cathode at a distance x from the center of the emission window is given by the following equation:

$$v_{ac}(x) = A_1 \exp(-g(x-a)) + A_2 \exp(g(x+a)), \qquad (1)$$

where 2a is the width of the emission window W_E and A_1, A_2 are the magnitudes of the microwave signal on either side of the emitter window. By symmetry, A_1, A_2 can be assumed to be equal, γ is the wave propagation constant, which can be expressed as follows:

$$g = \sqrt{r_b\left(g_m + jwC_{CdS}\right)}, \qquad (2)$$

where g_m and C_{CdS} are the unit area shunt conductance and shunt capacitance of the transmission line, respectively, ω is the angular frequency of the AC signal and ρ_b is the sheet resistance of the LaS thin film. The latter can be easily estimated, as follows:

$$r_b = r_{LaS}/t, \qquad (3)$$

where t is the thickness of the LaS layer (4 monolayers in all our simulations or 25 A) and ρ_{LaS} is the resistivity of the LaS thin film (selected to be 25 $\mu\Omega$-cm in our numerical examples).

Both g_m and C_{CdS} are expected to be function of the position across the emitter window if current crowding effects exist under DC biasing conditions. Hereafter, we assumed g_m and C_{CdS} to be

constant, which is equivalent to assuming a uniform DC emission current density across the emission window. In Equation (2), g_m is the small signal conductance of the cold cathode:

$$g_m = \frac{dJ_{em}}{dV_{bias}}, \tag{4}$$

where J_{em} is the emitted current density and V_{DC} is the DC bias across the CdS layer. In Equation (2), C_{CdS} is the capacitance per unit area of the cathode, which is, for simplicity, approximated as a parallel plate capacitor with thickness equal to the thickness of the CdS layer.

Using these definitions, we can derive an estimate of the ultimate frequency of operation of an InP/CdS/LaS cold cathode as follows:

$$f_T = \frac{g_m}{2pC}, \tag{5}$$

which allows us to rewrite the AC signal wave propagation constant across the CdS layer as follows:

$$g = \sqrt{r_b g_m \left(1 + j\frac{f}{f_T}\right)}. \tag{6}$$

In our earlier numerical treatments of the InP/CdS/LaS cold cathode [1,2] we have shown that in a limited range of bias, the emitted current density could be well approximated as follows:

$$J_{em} = J_o \exp(aV_{DC}), \tag{7}$$

where J_0 and α are fitting parameters to model the Fowler-Nordheim emitted current density. We used this approach to calculate the emitter-utilization factor (EU) of the cold cathode, which is defined as the ratio of the actual amount of AC emitter current to the total emitter current that would have flown if the AC current density were uniform across the emitter area and had a value equal to that at the emitter periphery, i.e.,

$$EU = \frac{\left|\int_0^{W_E/2} J_{em}(x)dx\right|}{\left|\int_0^{W_E/2} J_{em}(0)dx\right|}. \tag{8}$$

With the J_{em} exponential dependence on DC bias assumed above, the EU factor can be calculated explicitly [4] and is found to be

$$EU = \left| \frac{2}{gW_E} \tanh\left(\frac{gW_E}{2} \right) \right|. \qquad (9)$$

1.1 Numerical Results

1.1.1 Emitter Utilization Factor: In Figures 3 through 5, we plot the bias dependence of EU factor for different values of the emitter emission windows and frequencies of the external AC signal. The widths of the emission window must be kept sufficiently small to avoid the effects of DC current crowding. The width of the CdS layer was kept equal to 300 A in all simulations. The values of the parameters α and J_o are selected arbitrarily equal to 1.8 V^{-1} and 10 A/cm^2. With these values, the emitted current densities are in good agreement with our earlier calculations [1].

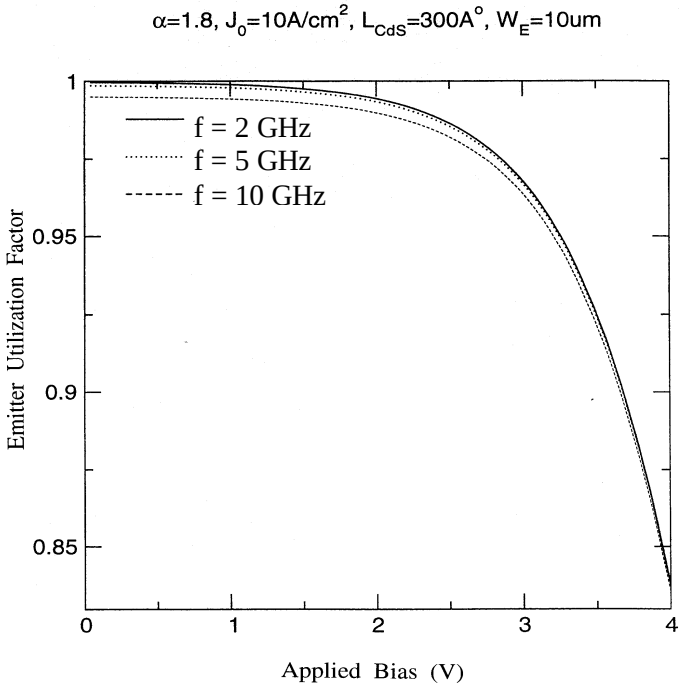


Figure 3. Bias Dependence of the Emitter Utilization Factor for an Emission Window Width of 10 μm at Three Different Frequencies of the AC Voltage Across the CdS Layer, Which is 300 A Thick.

Figures 3 through 5 show similar trends with a lower value of the EU factor at higher frequency approaching the cutoff frequency of the cathode. For the largest emission window, the EU factor decreases to around 0.4 even at the low bias value. This is an acceptable value of the EU factor. If we take as a criteria that AC current crowding effects are negligible if the EU factor is kept above 0.9, Figure 3 shows that AC current crowding are negligible even for an AC signal of 10 GHz up to a bias of about 2.8 V. Figures 3 through 5 also show that the sensitivity of the EU factor to the AC signal frequency increases for larger emitter window, as expected.

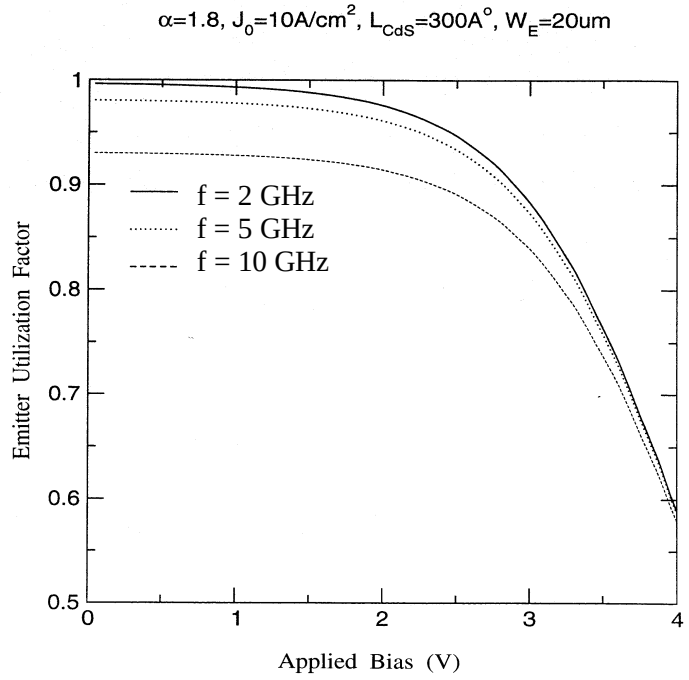


Figure 4. Bias Dependence of the Emitter Utilization Factor for an Emission Window Width of 20 μm at Three Different Frequencies of the AC Voltage Across the CdS Layer, Which is 300 A Thick.

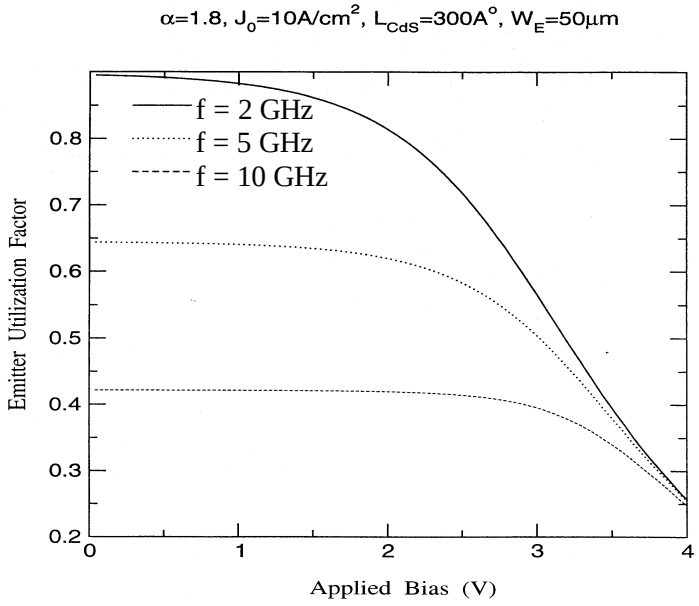


Figure 5. Bias Dependence of the Emitter Utilization Factor for an Emission Window Width of 50 μm at Three Different Frequencies of the AC Voltage Across the CdS Layer, Which is 300 A Thick.

In Figures 6 through 9, we plot the EU factor versus the emission window width W_E for different values of the applied DC bias. These figures indicate that AC current crowding should be negligible (at a frequency of 10 GHz) for an emission window width kept below 10 μm even for an external DC bias of 4V.

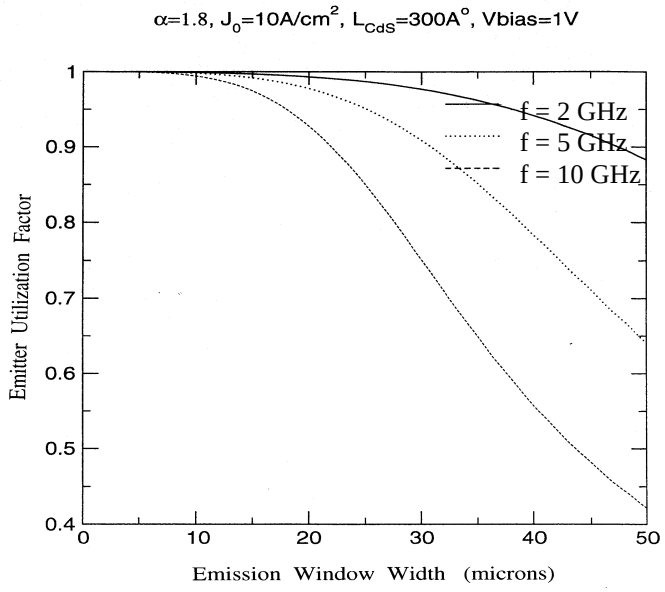


Figure 6. Emission Window Width W_E Dependence of the Emitter Utilization Factor for a DC Applied Bias of 1 V as a Function of the Frequency of the AC Signal Applied across the 300 A Wide CdS layer.

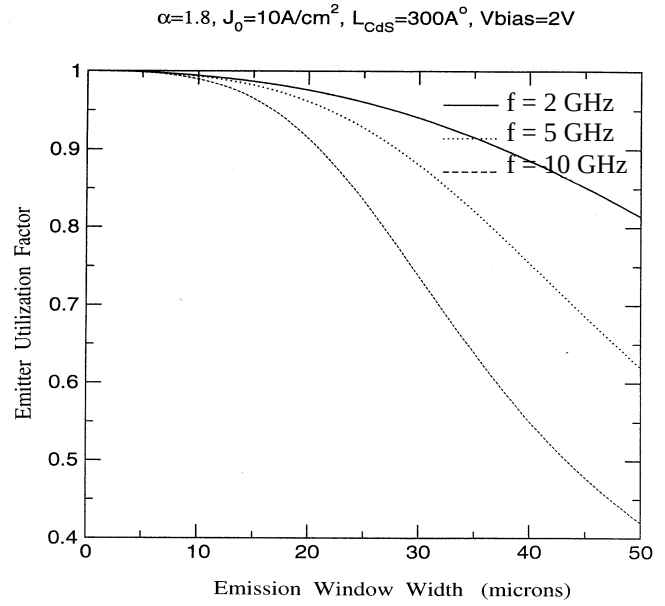


Figure 7. Emission Window Width W_E Dependence of the Emitter Utilization Factor for a DC Applied Bias of 2 V as a Function of the Frequency of the AC Signal Applied across the 300 A Wide CdS layer.

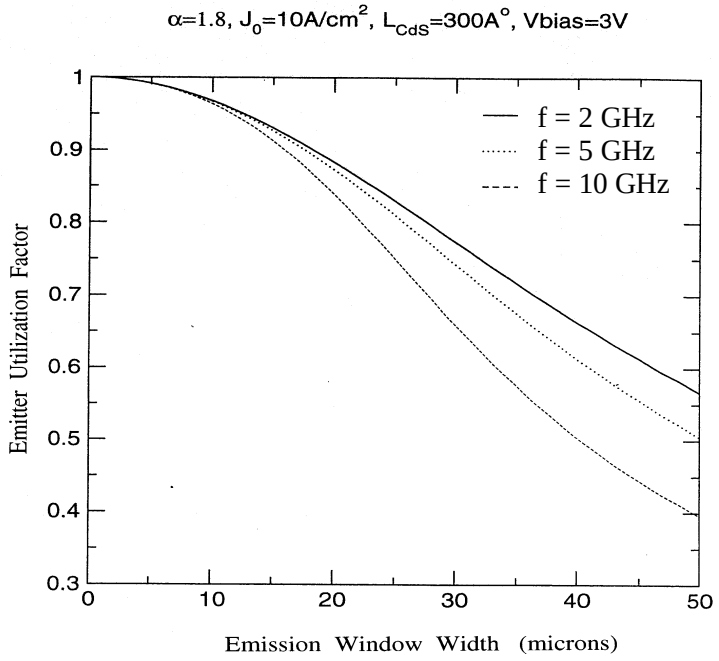


Figure 8. Emission Window Width W_E Dependence of the Emitter Utilization Factor for a DC Applied Bias of 3 V as a Function of the Frequency of the AC Signal Applied across the 300 A Wide CdS layer.

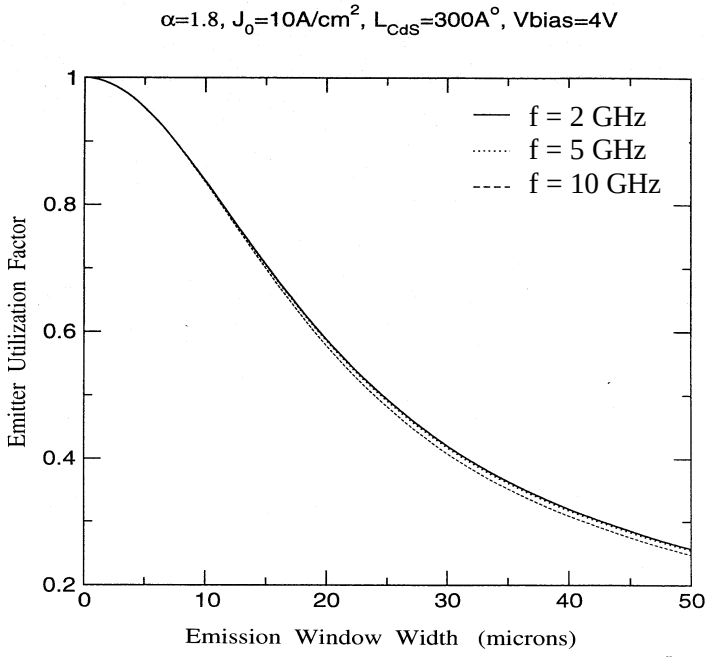


Figure 9. Emission Window Width W_E Dependence of the Emitter Utilization Factor for a DC Applied Bias of 4 V as a Function of the Frequency of the AC Signal Applied across the 300 A Wide CdS layer.

1.1.2 Amount of AC Current Crowding and InP/CdS/LaS Cold Cathode Design for Performance in the X-band: In the simulations in the previous section, we have investigated the effects of AC current crowding in an InP/CdS/LaS cold cathode. Our first order analysis of the emitter utilization factor was based on the assumption that the emitted current density could be parameterized as a function of the DC applied bias as follows:

$$J_{em} = J_o \exp(aV_{DC}), \tag{10}$$

where J_0 and α were fitting parameters to model the Fowler-Nordheim emitted current density. These parameters were selected arbitrarily in the previous section. To improve our model, we next use the model of the InP/CdS/LaS cold cathode we developed in the past to study the importance of self-heating effects in the cathode [5]. Assuming inelastic scattering in the CdS and LaS layer with a mean-free path of 300 A and room temperature operation for now, we calculated the utilization factor of a cathode with a 150 A CdS layer as a function of the width of the emission window.

We used the model described above to calculate the maximum frequency of operation and the EU factor. Next, we illustrated the AC current crowding effects by plotting the amplitude of the AC signal across the emission window for a cold cathode with a width of the CdS layer equal to 150 A. We started with the expression for the microwave voltage across the cathode at a distance x from the center of the emission window given by Equations (1) where 2a is the width of the emission window and A_1, A_2 are the magnitudes of the microwave signal on either side of the emitter window. If we normalize the AC amplitude to the value of the AC signal at the edge of the emission window, we obtain the following:

$$\left|v_{ac}(x)/v_{ac}(0)\right| = \left|\exp(-g(x-a)) + \exp(g(x+a)\right| / \left|\exp(ga)) + \exp(ga)\right|. \tag{11}$$

Figure 10 shows the variation of the emitted current density versus bias applied across the CdS layer. The results are nearly the same for window width equal to 5 and 10 μm. A fairly large current density of several thousand A/cm^2 can be obtained with a fairly small bias. This is due to the fact that the width of the CdS layer has been reduced. The curves in Figure 10 are then used to compute the maximum frequency of operation of the cathode using the model described in our earlier reports and the results for f_T are plotted in Figure 11. The results are only shown for a window width of 5 μm, but are nearly identical for the 10 μm window.

Figure 11 indicates that the cathode can operate in the X-band for a bias across the cathode equal to 1.632 V. For this bias, the effects of AC current crowding are small. For the cathode with 5 μm wide emission windows, the AC potential is only reduced by 12 percent of its value at the edges of the emission window when the cathode is operated in the X-band, as shown in Figure 12. The reduction at the center is more severe (close to 40 percent) for a 10 μm wide emission window as seen in Figure 13.

In summary, our analysis of AC current crowding in a InP/CdS/LaS cold cathode starting with the more rigorous DC model of reference [5] indicates that operation in the X-band is possible by

reducing the width of the CdS layer to 75 A and by keeping the width of the emission window under 5 μm.

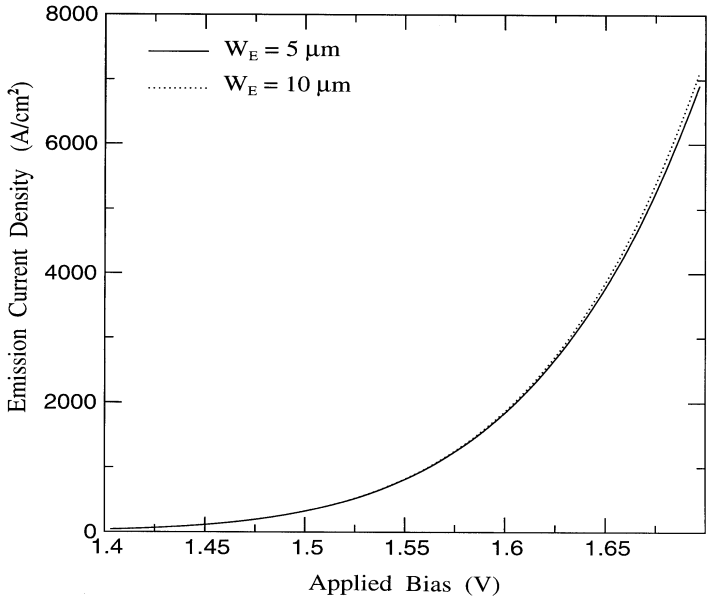


Figure 10. Emission Current Density for Emission Window Widths of 5 μm and 10 μm versus Applied Bias across the 75 A CdS Layer of a InP/CdS/LaS Cold Cathode.

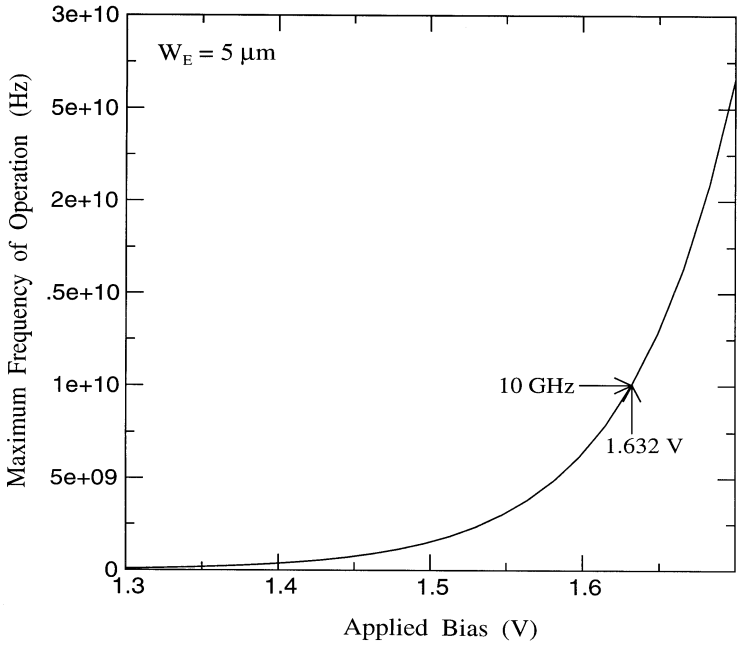


Figure 11. Maximum Frequency of Operation f_T versus Applied Bias across a 75 A CdS Layer in an InP/CdS/LaS Cold Cathode for an Emission Window Width of 5 μm.

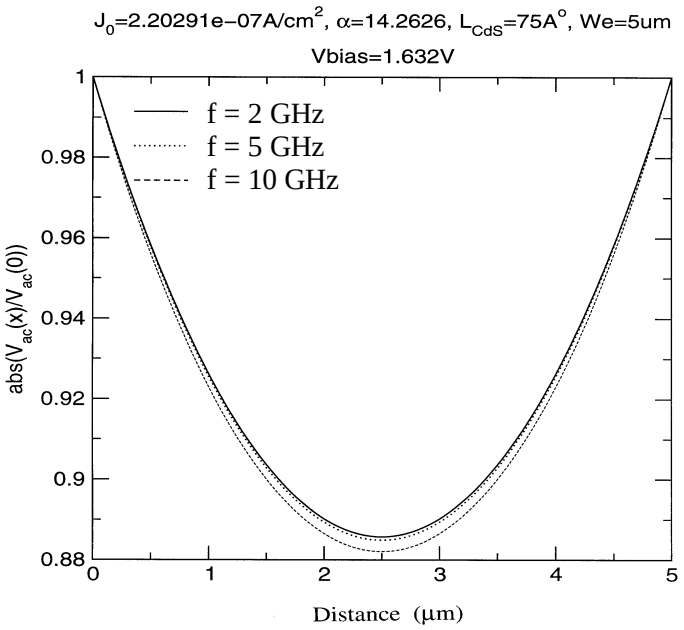


Figure 12. Amount of AC Current Crowding as a Function of Frequency for an AC signal Applied Across the 75 A CdS layer of an InP/CdS/LaS Cold Cathode with an Emission Window of 5 μm and an Applied Bias across the CdS layer of 1.63 V.

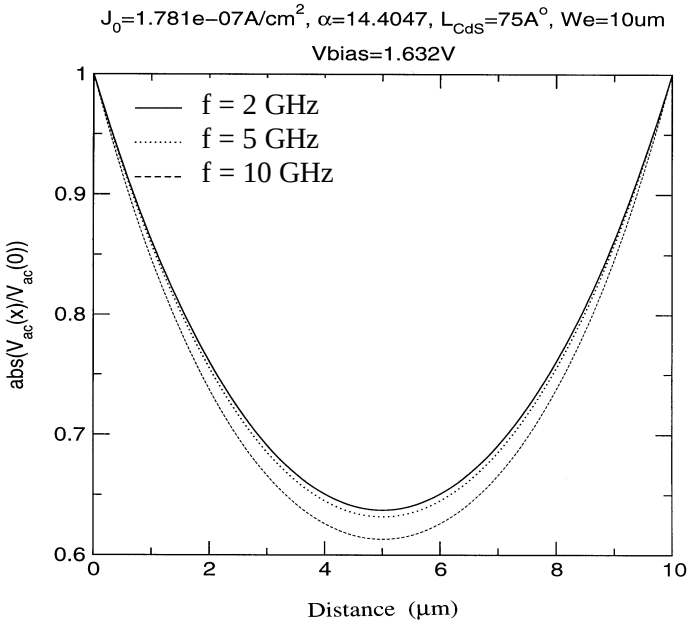


Figure 13. Amount of AC Current Crowding as a Function of Frequency for an AC signal Applied Across the 75 A CdS layer of an InP/CdS/LaS Cold Cathode with an Emission Window of 10 μm and an Applied Bias across the CdS layer of 1.63 V.

1.2 Small AC Signal Equivalent Circuit of an InP/CdS/LaS Cold Cathode

1.2.1 Development of Equivalent Circuit: Next, we focused on developing a small signal equivalent circuit of the InP/CdS/LaS cold cathode, which goes beyond the first order treatment described in section 1.1 where we used the simple estimate for the maximum frequency of operation of the cold cathode based on Equation (5). By looking more carefully at the current flow within the device (Figure 14), a small AC equivalent circuit of the cathode was derived and is shown in Figure 15. This figure shows a cross section of the cathode and the various resistive and capacitive elements controlling its high-frequency performance. The cathode can be thought as a three-terminal device (similar to a bipolar junction transistor (BJT) or heterojunction bipolar transistor (HBT)) in which the role of the emitter is played by the heavily doped InP substrate [4]. The biasing fingers play the role of the base and the anode is equivalent to the collector.

First, not all of the Fowler-Nordheim tunneling current is actually flowing through the area of the rectangular window. Some of it, emitted under the Au lines used to bias the cathode, will not be able to make it into vacuum because of the shadowing action of the Au biasing fingers. This part of the Fowler-Nordheim tunneling current is part of the base current since it will be forced to run through the Au lines. In addition, the base current also contains a component resulting from the trapping of electrons in the CdS layer. This trapping is included in our model and results not only from the effects of inelastic scattering in the CdS and LaS layers but also from the finite probably for electrons to be reflected at the CdS/LaS and LaS/vacuum interfaces.

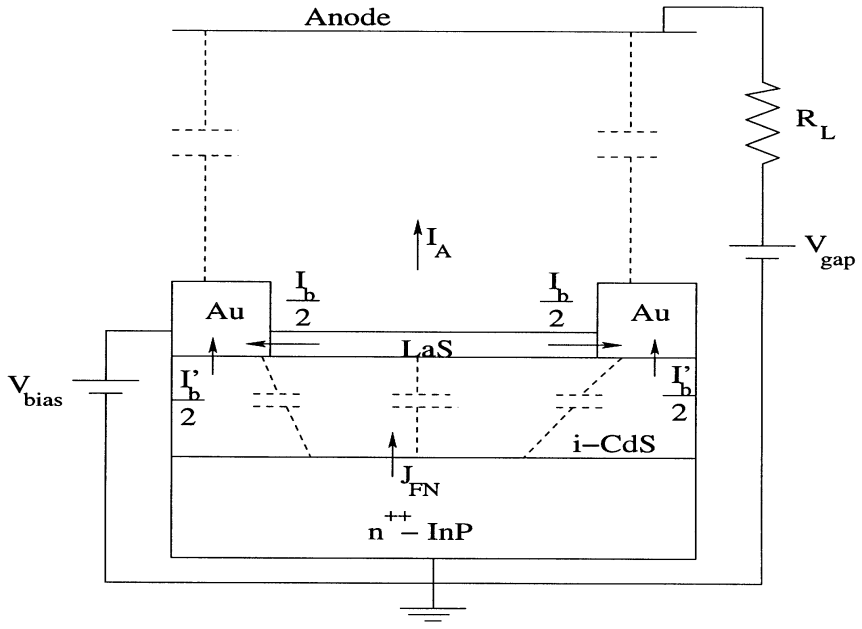


Figure 14. Cross Section of Cold Cathode Showing the Various Resistive and Capacitive Elements Controlling its High Frequency Performance.

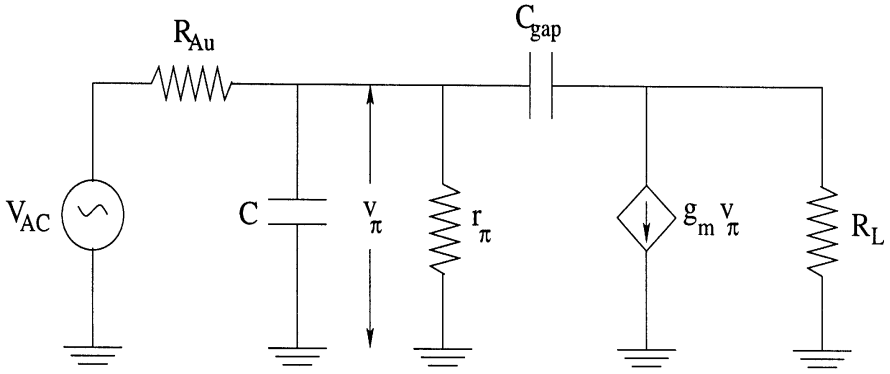


Figure 15. Small-signal AC Equivalent Circuit for Cold Cathode Structure.

We assumed that the width W_E of the Au fingers on either sides of the emission window are equal to the width of the emission window itself (but the model can be generalized to any other configuration). The amount of base current is than simply given by the following equation:

$$I_B = J_{FN}(2W_E L) + (J_{FN} - J_A)W_E L\,, \tag{12}$$

where the first term comes from the shadowing action of the two emitters fingers and the second term is due to the current trapping of electrons in the LaS thin film. In Equation (12), L is the length of the Au fingers.

In the simulations, we fitted the base current to an expression of the following form:

$$I_B = I_o \exp(aV_{bias}) \tag{13}$$

and extract the parameters I_o and α using the model discussed in reference [5]. If a small AC signal is added to V_{bias}, we could then build a hybrid-pi equivalent circuit of the diode as shown in Figure 15. From the base current expression above, we found the following small signal resistance of the emitter-base junction:

$$r_p = \left[\frac{dI_B}{dV_{bias}}\right]^{-1} = (aI_B)^{-1}, \tag{14}$$

which is a function of the DC biasing point.

The capacitance between emitter and base is simply approximated at the parallel plate capacitor with a thickness equal to the width of the CdS layer and an area equal to 3 W_E times the length L of the emission window. The DC bias and small AC signal are applied on a rectangular pad located at the end of the emitter fingers of length L. We must therefore take into account of the

finite resistance of the Au lines, which have width W_E, length L, and height H. This leads to a contact resistance R_{Au} equal to the result of the following equation:

$$R_{Au} = \frac{r_{Au} L}{W_E H}, \tag{15}$$

where ρ_{Au} is the resistivity of the Au lines.

The small AC signal controls the (collector or anode) current I_A. The latter is also a function of the DC applied bias and can be parameterized as follows:

$$I_A = I_o' \exp(a' V_{bias}) . \tag{16}$$

This leads to a transconductance for the cathode given by the following:

$$g_m = \frac{dI_A}{dV_{bias}} = a' I_A . \tag{17}$$

Finally, we included the effects of the capacitance between the anode and the LaS thin film and Au lines, which we simply model also as a parallel plate capacitance with a thickness equal to the separation between anode and cathode (which we take as 15 μm in the simulations hereafter). The AC circuit is completed by adding the load resistance R_L, which is shown schematically in Figure 15.

1.2.2 Equivalent Circuit Simulations: For the cathode, we use the following parameters: thickness of the CdS layer (75 A), anode to cathode spacing (15 μm), width of the emission window and Au lines (5 μm), and the length of the Au lines (100 μm). The resistivity of Au lines was set equal to 2.04 Ω-cm and the dielectric constant of the CdS layer was set equal to 5.4 ε_0. Furthermore, the voltage across the vacuum gap is assumed to be large enough that space-charge effects in the vacuum region do not have any influence on the anode current.

Because the capacitance between anode and cathode is rather small, the associated impedance at an assumed AC frequency of 10 GHz is rather large. With the parameters listed above, the impedance between cathode and anode is found to be about 3.2 kΩ, which is much larger than the impedance of the CdS layer capacitance (1.7 Ω) and the resistance r_π. Figure 16 is a plot of the bias dependence of the base and anode currents. The bias dependence of the small signal parameters r_π and g_m are plotted in Figure 17. Referring back to Figure 15, since the impedance of the anode-to-cathode capacitance is large, the maximum frequency of operation of the cold cathode f_T is found to be equal to the result of the following equation:

$$f_T = \frac{1}{2p\left(R_{Au} \| r_p\right) C} . \tag{18}$$

The latter is plotted as a function of V_{bias} in Figure 18. This figure shows the bias dependence of f_T for two different values of the length of the emitter fingers. Figure 18 indicates that, by appropriately designing the cathode, the unity gain frequency can be well in excess to the 10 GHz frequency range for operation of the cathode in the X-band.

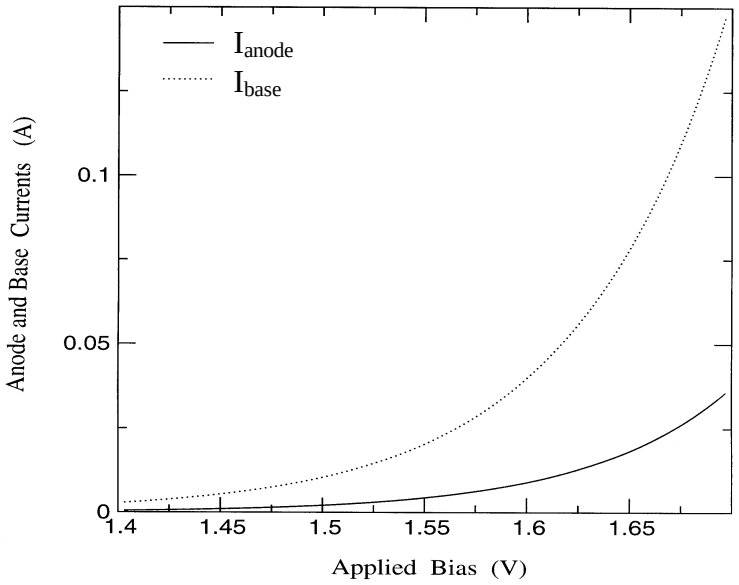


Figure 16. Base and Anode Currents for Cold Cathode Structure as a Function of the Applied Bias V_{bias}.

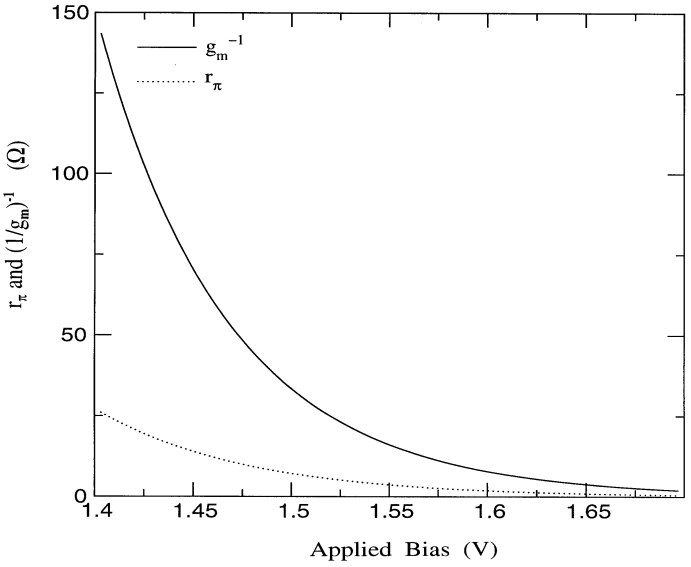


Figure 17. Small Signal Parameters r_π and g_m for the Cold Cathode as a Function of the Applied Bias V_{bias}.

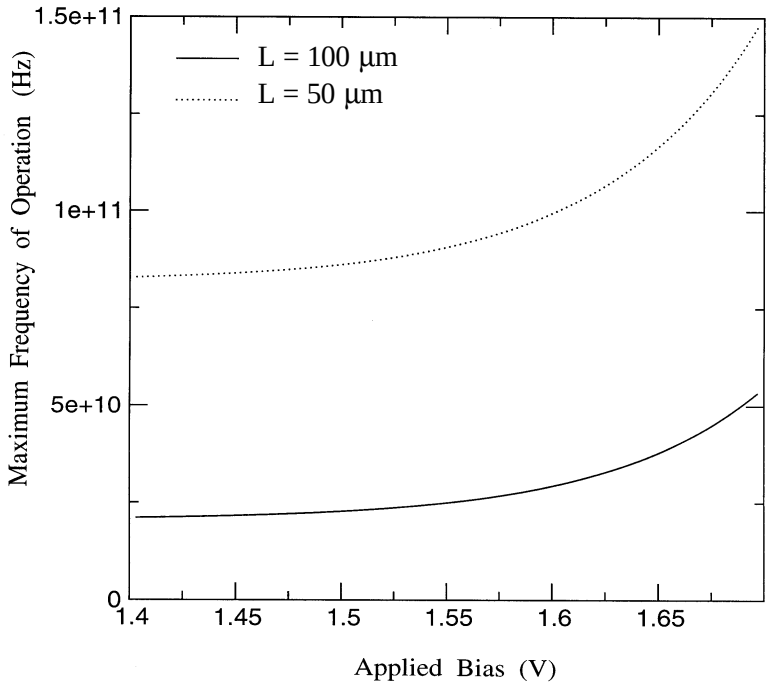


Figure 18. Maximum Frequency of Operation f_T for the Cold Cathode as a Function of the Applied Bias V_{bias}.

In summary, we have constructed a small AC signal equivalent circuit (hybrid-pi) model of an InP/CdS/LaS cold cathode indicating that frequency operation in the X-band is feasible. More accurate simulations of the frequency response of the cathode should be coupled with the self-heating effects in the cathode that would tend to increase the LaS work function thereby decreasing the anode current and simultaneously increasing the base current. This would tend to decrease the transconductance of the cathode and reduce its overall frequency performance. The overall bias dependence of the unity gain current frequency would then be expected to reach a maximum before falling at larger values of the DC bias as a result of self-heating effects.

2. Cold Cathode – HBT Integration

2.1 Geometric Considerations

For high current beam generation, the cold cathode structure must be operated at a high current density ~10^3 A/cm^2. To achieve this current density, the cold cathode structure must be provided with a high current input since the structure does not of itself produce gain. One device known for its ability to produce a high current drive output is the bipolar transistor. For the high frequency application of interest here at ~10 GHz, the heterojunction bipolar transistor (HBT) is a possibility since it can simultaneously provide high current density operation and gain at the necessary frequencies. Both GaAs-based and InP-based HBTs are of interest since the rare-earth sulfides, NdS and LaS, that are nearly lattice-matched to GaAs or InP, respectively, are potential materials for incorporation in the cold cathode structure because they have sufficiently low electron affinities.

One of the primary tasks undertaken in this contract was the investigation of the issues and obstacles arising from the monolithic integration of the cold cathode structure with an HBT. Both high-current density operation and microwave frequency performance (~ 10 GHz) were the objectives. The integration issues are very similar for the GaAs and InP-based transistors, so only the InP-base transistor integration will be considered in this initial discussion.

Two configurations were investigated for possible integration of the two devices as shown in Figure 19. The first (lateral) approach incorporates the cold cathode structure adjacent to the HBT. The HBT epitaxial layer structure is grown initially by a conventional process, e.g. molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) technologies, and the transistor is fabricated in the usual mesa etch process. Subsequently, the CdS and LaS is deposited epitaxially and the top metal grid contacts formed to complete the cold cathode structure. The n- InP collector layer could be incorporated into both structures.

In the second approach (vertical), the HBT would be positioned beneath the cold cathode structure and the n+ InP collector layer would constitute part of both devices. The HBT would be inverted in this case (collector-up) so that the output electron collector current of the HBT could be injected directly into the cold cathode. The epitaxial growth issues associated with growth of the rare-earth sulfides on the InP material were not investigated here. Rather, the issues associated with the integration, electrical operation and interaction of the two structures were examined. In the following, we summarize the results of our analysis regarding the feasibility of the two approaches to monolithic integration.

We consider first the lateral integration approach seen in Figure 19 a. Here the output collector current of the HBT is transmitted laterally through the heavily doped subcollector layer to the region beneath the cold cathode. In this case, the HBT is fabricated in the normal emitter-up configuration, which is known to be capable of high current and high frequency operation [6]. This configuration poses a number of problems, however, with respect to the efficient transfer of current from the HBT into the cold cathode. Recall that for the conventional emitter-up HBT, the transistor typically employs dual base contacts (to reduce base series resistance) and two collector contacts [6]. As a result of the device's symmetry, one half of the collector current is

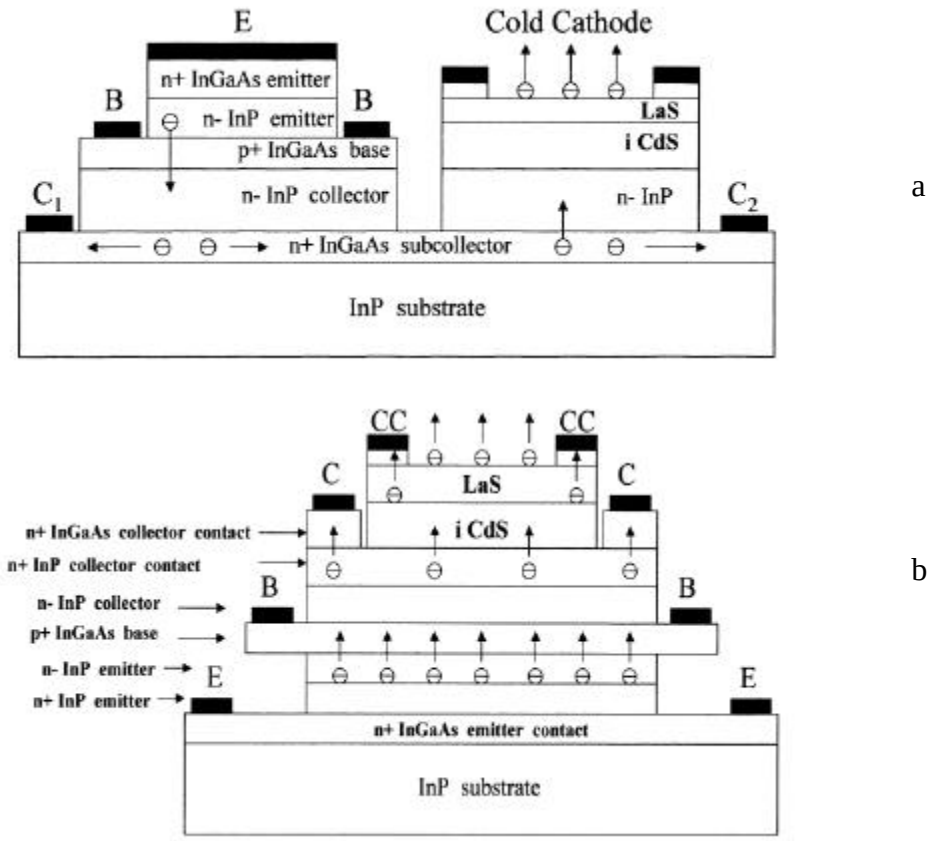


Figure 19. Cross Section of the Integration of an HBT with a Cold Cathode using the Lateral (a) and Vertical (b) Integration Approaches.

collected at each of the two collector contacts. With this in mind, when we place the cold cathode structure adjacent to the HBT, we estimate initially that approximately one half of the collector current will go to the cold cathode structure since it is replacing the second collector contact. However, this is optimistic. Without a second collector contact C_2 (positively biased) to the right side of the cold cathode structure as shown in Figure 19 a, we have little chance of drawing the electrons laterally to the cold cathode. So the presence of the second collector contact C_2 is a necessity. But the second collector contact C_2 competes with the cold cathode structure for collecting the electrons (in addition to the competition from the C_1 collector contact). In fact, the situation is actually worse than this. The collector contacts present a low impedance (~ 10's of Ωs) to the electron flow since each forms a low resitance ohmic contact. By contrast, the cold cathode structure presents a high impedance of the order of few kΩ's since we estimate an emission current of the order of 0.5 mA for a bias of 1 V. As a result, most of the collector current output from the transistor will be collected at the C_2 resulting in only a small fraction of the current being injected into the cold cathode structure. Hence, our current transfer efficiency from the transistor output into the cold cathode will be poor for this lateral integration approach. We can understand the physical origins of this effect as follows. Electrons injected into the cold cathode structure, face an intrinsic CdS layer that they must cross by thermionic emission and tunneling. This constitutes a relatively high impedance path by comparison with

the low resistance seen at the ohmic collector contacts C_1 and C_2. As a result, the current is largely shunted away from the cold cathode structure and collected at the collector contacts.

In summary, this lateral integration of the HBT and cold cathode structure does not appear to be a promising approach. There is difficulty providing efficient current transfer from the HBT's output into the cold cathode. Without efficient transfer, higher current operation for the HBT is needed with its associated problems of self-heating. Modifications to the system's design to resolve the problem do not appear attractive for controlling the emission current nor for modulation at high frequencies. Removal of the collector contacts is not a solution since doing so removes our ability to separately bias the collector junction of the HBT and the cold cathode structure. The two become connected in a simple series configuration with only a single bias across the combination.

We have also examined the related problem for the collector-up HBT integration with the cold cathode structure in a vertical configuration as shown in Figure 19 b. In this case, electrons are injected across the emitter junction of the transistor, and cross the base into the collector. A portion of these are injected across the CdS of the cold cathode and emitted into the vacuum. Similar to the lateral integration approach, we have examined the efficiency with which the output electron flow from the HBT is coupled into the cold cathode structure. In this case also, the collector contacts C compete with the cold cathode structure for the electron current. Since the current density is very nearly uniform across the collector, we can estimate the fraction of current collected by the cold cathode's anode I_A using a simple geometric argument based on the size of the collector contacts, the emission window and the top grid. The ratio of the emitted electron current I_A to the total current provided by the HBT's collector output is given by the following:

$$\frac{I_A}{I_C + I_{CC} + I_A} = \frac{A_E}{A_C} = \frac{W_E}{W_E + 2W_C + 2W_{CC}}, \qquad (19)$$

where I_C is the total current collected by the two collector contacts (a fraction of the total output current of the HBT) and I_{CC} is that collected by the top gold electrodes. Here W_E is the width of the emission window, W_C is the width of the collector contacts and W_{CC} is the width of the top cold cathode electrodes. In Equation (19), the area ratio is that of the emission window ($A_E = W_E L$) to the total collector junction area A_C (also equal to $(W_E+2W_C+2W_{CC})L$). For example, for W_E=10 μm, W_C = 1 μm and W_{CC} = 1 μm, the ratio is 10/14 = 0.71, which constitutes a reasonable transfer efficiency. From this simple approximate analysis, making the collector contacts relatively narrow compared with the emission window allows efficient current transfer from the HBT to the cold cathode. Of course, more exact numerical simulations are needed to refine this analysis. There will be some current crowding effects associated with the fact that the collector contacts pose a lower impedance than the cold cathode. One advantage that the collector-up, vertical integration approach retains over the lateral approach is that with the presence of the collector contacts, the voltage applied to the base-collector junction of the transistor and that across the CdS layer are individually adjustable.

For the HBT, implementation of the collector-up configuration presents obstacles to achieving acceptable device performance [7]. When the emitter-base junction area exceeds the collector-

base junction size, there is a significant loss in electron current injected across the emitter junction that is not collected by the collector junction, which results in serious degradation in the device's current gain. In this project we have investigated the effects of device geometry on HBT device performance for the collector-up configuration using a commercial, two-dimensional, device simulator ATLAS produced by Silvaco International [8] as well as using a simple analytical model. The purpose was to investigate the extent of degradation in device performance in utilizing the collector-up configuration. For the collector-up HBT shown in Figure 19 b, the emitter junction area has been reduced to that of the collector junction by underetching of the base region. Such an approach to device fabrication has been demonstrated using wet chemical selective etching to undercut the base mesa but not the emitter. For this modeling study, the InP/GaAsSb double heterojunction bipolar transistor (DHBT) [9] was investigated since the selective etchants are known. For the InP/InGaAs material combination more conventionally used for InP-based HBTs [6], the use of selective etchants is more difficult, though possible. Likewise, the use of selective etchants for GaInP/GaAs HBT fabrication is well known [10], though AlGaAs/GaAs HBTs are more typical GaAs-based transistors. Our simulation results, however, are largely geometry related so the exact material system investigated is not critical and the results can be generalized to any of the material systems.

Shown in Figure 20 a is the cross section for one half of the mesa isolated collector-up HBT where there has been no selective etching to undercut and reduce the width of the emitter and the emitter junction area. Shown in Figure 20 b is the case where the selective etching has been used to undercut the base contact and reduce the emitter junction area to just that of the collector junction. The latter is the preferred configuration since there is then nearly complete transfer of the electrons injected across the emitter junction into the collector and the device's current gain is large. However, in practice this is difficult to achieve so we have investigated the extent to which the device's current gain is degraded as the emitter junction area is increased from that produced for the device structure seen in Figure 20 b toward that seen in Figure 20 a. The results are shown in Figure 21 a where we have plotted the transistor's current gain as a function of the amount of the undercut. Zero undercut corresponds to the device structure seen in Figure 20 a, and an undercut of 3.5 μm corresponds to that in Figure 20 b. The results are replotted in Figure 21 b, but expressed in terms of the current gain degradation factor (i.e. device gain relative to that for the ideal case (Figure 20 b) versus the ratio of the emitter to collector junction areas. From Figures 21 a and 21 b, it is clear that without use of the undercut to reduce the emitter junction area, the transistor's gain in the collector-up configuration is very small (~2) and several orders of magnitude less than the corresponding emitter-up configuration for the same set of epitaxial layers and contact geometry. However, with the use of the lateral undercut, the device performance (current gain) can be dramatically improved to more 3800. The reason for this is that electrons injected under the base contact for devices with little undercut will likely be lost to recombination in the base increasing the base current and reducing the collector current. As a result, there will be degradation in the current gain. As shown in Figure 22, the electron distribution and flow is very nearly uniform across the emitter junction so the loss of electron flow is nearly proportional to the emitter junction area. What is significant from these results is that even an emitter junction area only 0.5 μm wider (10 percent larger area) than the collector junction results in a severe gain reduction of ~ 50 percent. These results point out the importance of using a selective etch to undercut the base layer to reduce the emitter junction area very nearly to that of the collector junction.

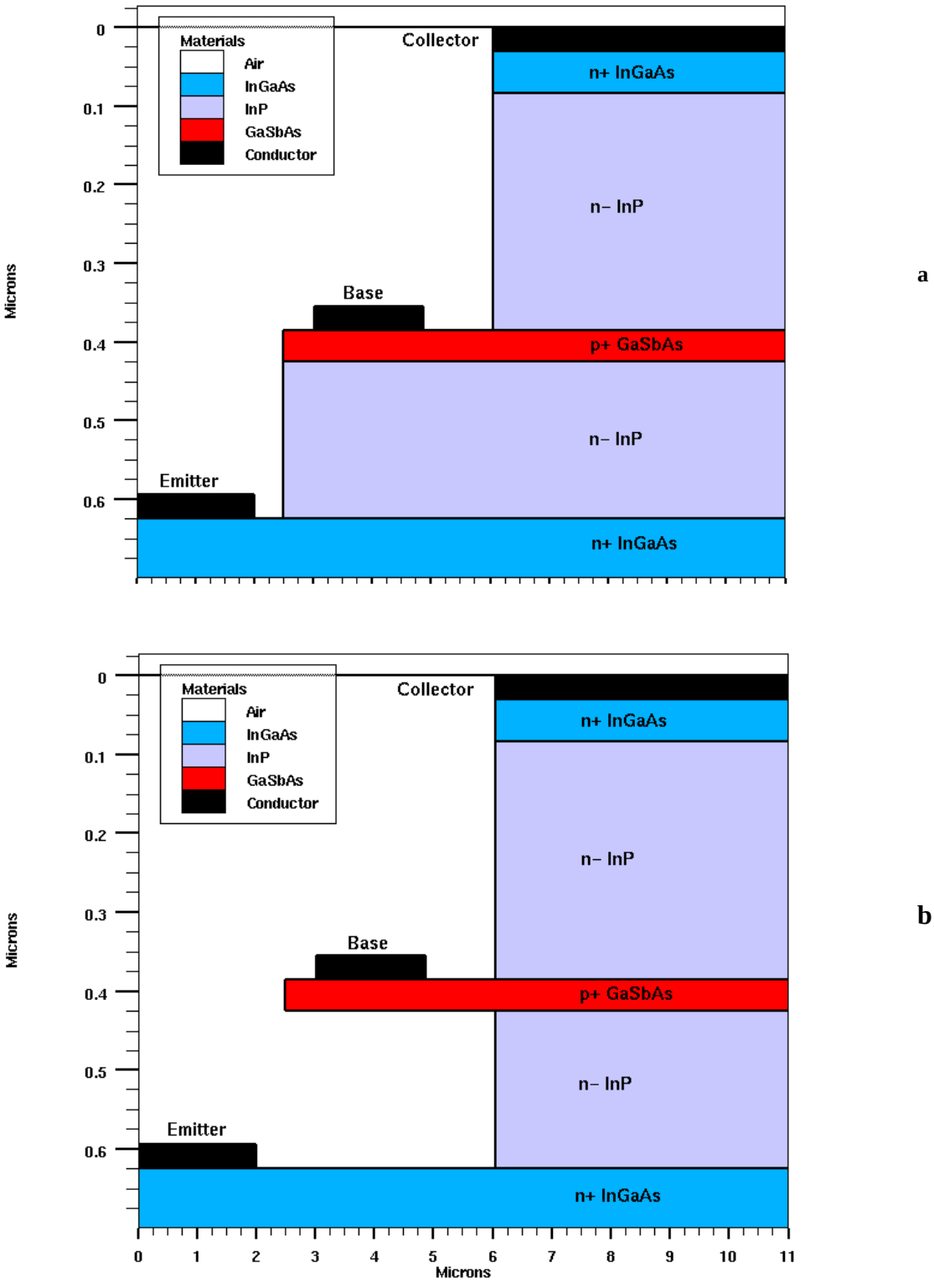
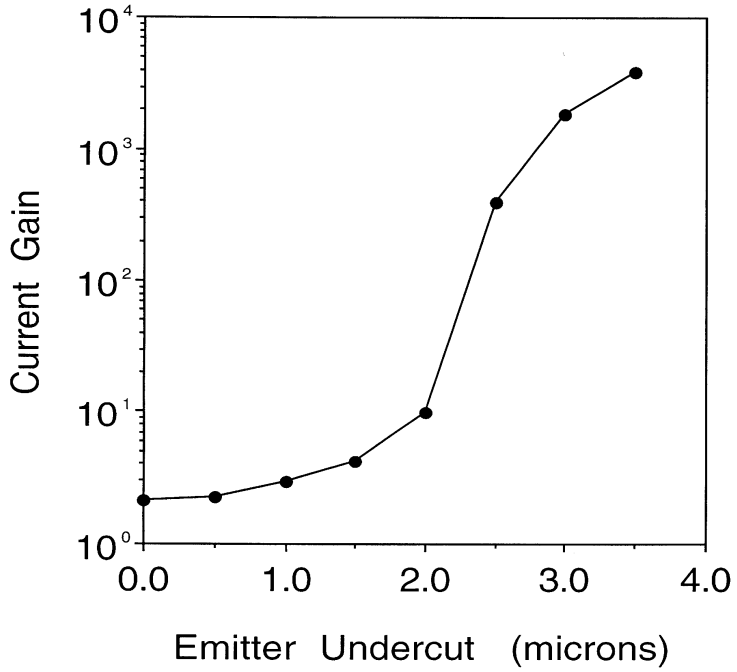
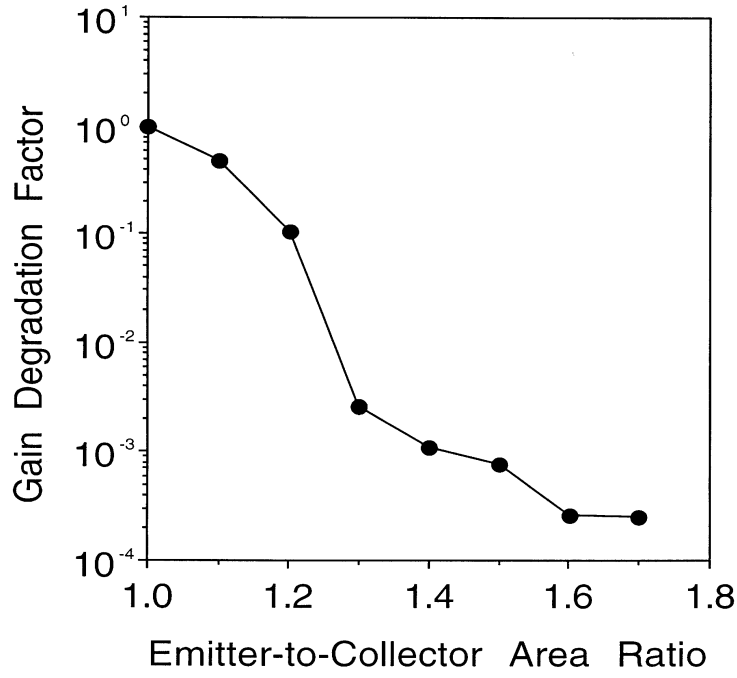


Figure 20. Cross Section of a Collector-up InP/GaAsSb HBT Showing no Lateral Undercut (a) and with Undercut (b) of the Emitter Area.



a.



b.

Figure 21. Current Gain as a Function of the Undercut of the InP Emitter (a) for a Collector-up HBT and Replot of the Results Expressed as a Degradation of Current Gain as a Function of the Ratio of the Emitter-to-Collector Junction Areas (b).

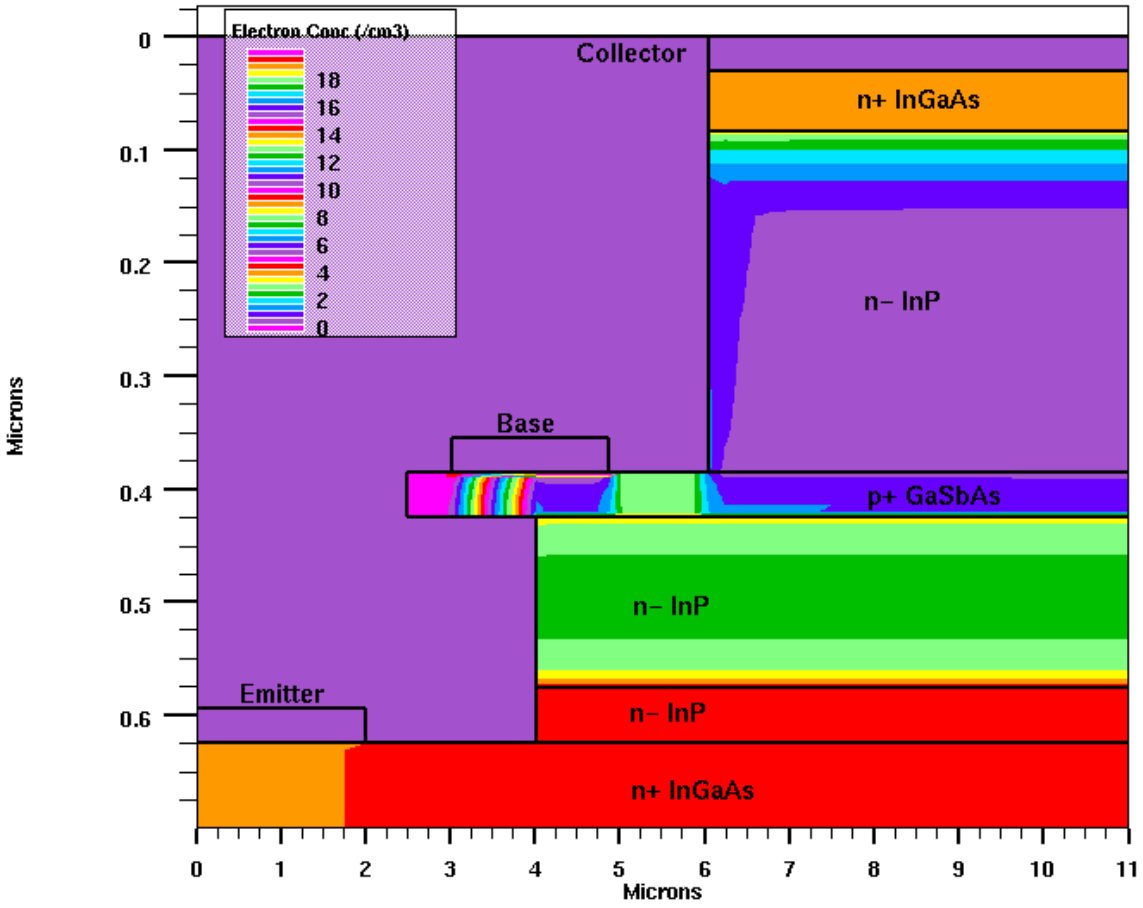


Figure 22. Electron Concentration Contours for the Device Operating at V_{BE} = 1.0V and V_{CE} = 2.0 V for the Collector-up HBT with an Undercut of 1.5 µm.

2.2 Energy Band Structure Considerations

Also considered as a part of this contract was the HBT technology that might be suitable for integration with the cold cathode structure. Both GaAs-based and InP-based HBTs were considered since rare-earth sulfides that are lattice-matched to GaAs and InP, respectively, have been investigated and found to have low electron affinities. We consider first the InP-HBT technology compatible with the CdS and LaS materials. Shown in Figures 19 a and b are the emitter-up and collector-up configurations, respectively, for an InP/InGaAs HBT, which is the conventional material system utilized for InP-based HBTs [6]. However, the need for an n+InP layer for use in the cold cathode structure and its simultaneous use as the collector of the InP/InGaAs HBT poses a problem with this implementation. Shown in Figure 23 is the energy band structure for this proposed integration of the InP/InGaAs HBT and cold cathode structure. The narrow band gap InGaAs base region has a wide band gap InP layer as the emitter and collector so that the device constitutes a double heterojunction bipolar transistor (DHBT). As a result of the conduction band discontinuity (0.25 eV) at the base-collector junction in the HBT, there will be a severe limit to electron flow from the base into the collector and a corresponding degradation in the device's collector current and current gain [6]. The development of double heterojunction InP/InGaAs HBTs has been pursued and successful demonstration of high performance devices has necessitated the development of approaches to reducing the effect of this band discontinuity, including compositional grading or use of a graded superlattice at the base-collector junction [11,12]. These approaches complicate considerably the epitaxial growth technology required to fabricate the device's multilayer structure. They also complicate the device's fabrication. As a result, integration of an InP/InGaAs DHBT with a CdS/LaS cold cathode structure is more problematic and less attractive. Alternative approaches need to be considered.

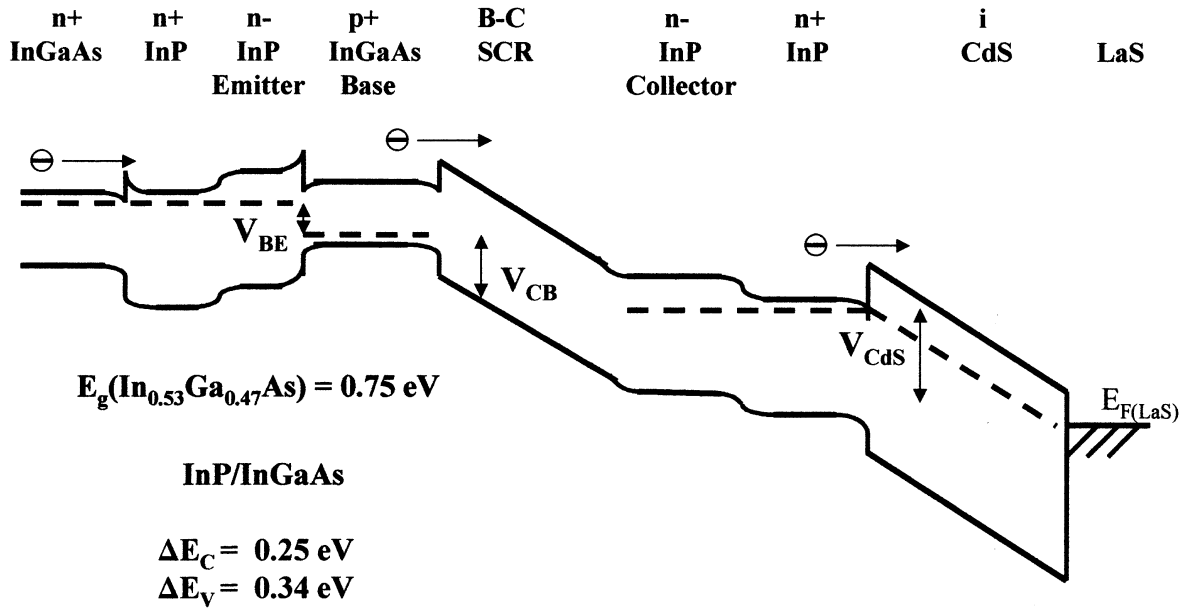


Figure 23. Energy Band Diagram for InP/InGaAs Double Heterojunction Bipolar Transistor Integrated with a LaS/CdS/InP Cold Cathode Structure.

Recently, there have been reports in the literature of an alternative, narrow gap material GaAsSb for use as the base of an InP-based DHBT [9,13]. $GaAs_{0.51}Sb_{0.49}$ has a bandgap of 0.81 eV (close to the 0.75 eV for InGaAs) and can be grown lattice-matched to InP. What is also interesting and attractive about GaAsSb is that its conduction band edge is above that of InP by 0.18 eV so that we have a type II heterojunction (offset band edges instead of inset edges). As a result, the energy band diagram for the InP/GaAsSb DHBT looks like that shown in Figure 24. Note that there is no conduction band barrier at the collector heterojunction so that a double heterojunction device can be built. InP/GaAsSb DHBTs have been successfully demonstrated with high gain and microwave frequency capability. Since the collector is n-type InP, the device is also attractive for integration with the CdS/LaS cold cathode structure as seen in Figure 24. Selective etching techniques have also been employed in building InP/GaAsSb DHBTs [9,13] so that the fabrication of the collector-up HBT with lateral undercutting of the base to reduce the emitter area is also feasible.

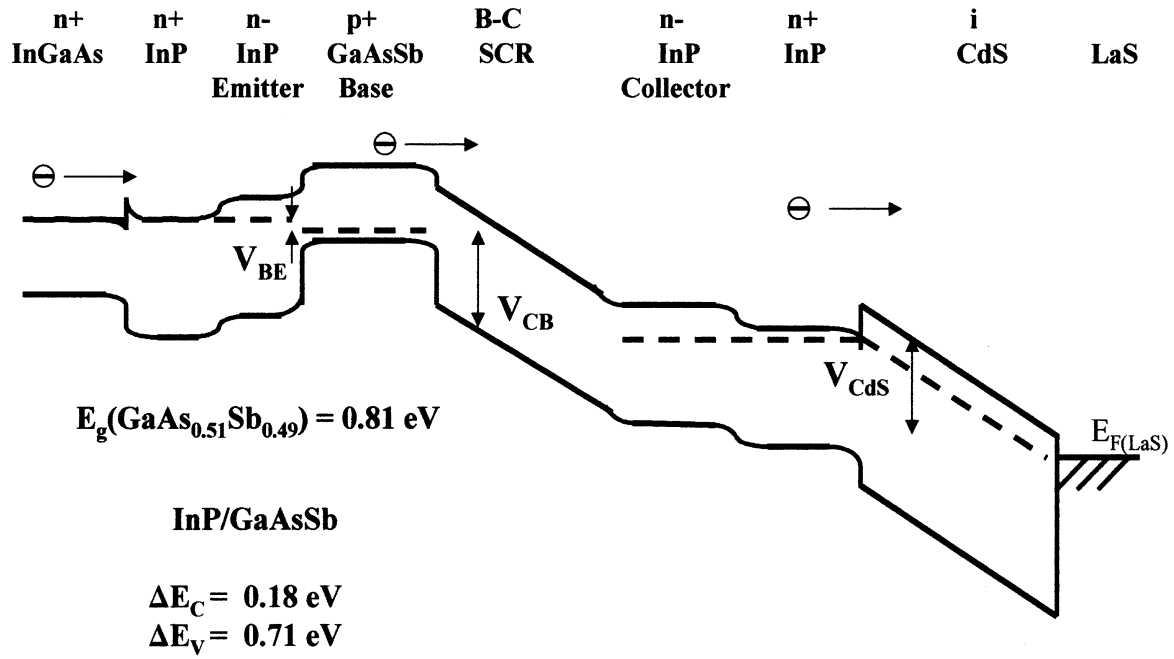


Figure 24. Energy Band Diagram for InP/GaAsSb Double Heterojunction Bipolar Transistor Integrated with a LaS/CdS/InP Cold Cathode Structure.

GaAs-based HBTs have also been investigated for possible integration with NdS employed in the cold cathode structure since NdS is closely lattice-matched to GaAs. For GaAs-based HBTs, the dominant material technology is AlGaAs/GaAs HBTs. Shown in Figure 25 is a possible scheme for integrating an AlGaAs/GaAs HBT with a NdS cold cathode structure. In this case, since GaAs is desired as the collector, the device used is a single heterojunction HBT with an AlGaAs emitter layer. For the cold cathode structure, AlGaAs is proposed as the wider band gap, insulating material and NdS as the low electron affinity electrode material. Such an HBT structure would be relatively easy to grow and obtain since the AlGaAs material is essentially lattice-matched to GaAs for all compositions. For fabricating the collector-up HBT,

selective etching has been reported for etching AlGaAs versus GaAs, so the undercut of the base layer could be used to reduce the emitter junction area.

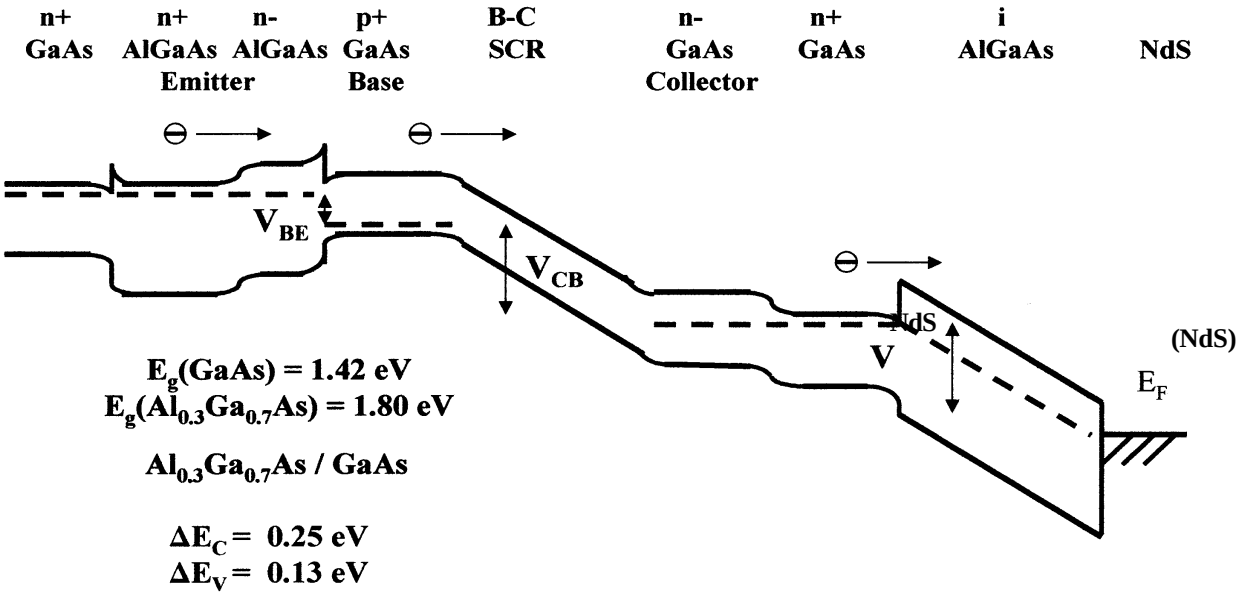


Figure 25. Energy Band Diagram for AlGaAs/GaAs Heterojunction Bipolar Transistor Integrated with a NdS/AlGaAs/GaAs Cold Cathode Structure.

As an alternative to AlGaAs/GaAs HBTs, GaInP/GaAs HBTs have recently been reported with good high-frequency performance [10,14]. GaInP can be grown lattice matched to GaAs and has a bandgap of 1.84 eV, similar to AlGaAs, but has a much smaller (0.11 eV) conduction band discontinuity. The GaInP material has a number of characteristics that make it superior to AlGaAs for devices, particularly HBTs, including a reduced tendency to incorporate oxygen during growth and formation of related defects. In addition, selective etching has been shown to work in fabricating these devices [10,14], which makes its use in fabricating the collector-up HBT more feasible than in the AlGaAs/GaAs HBT case. Recently, a collector-up GaInP/GaAs HBT has beeen reported [15]. Shown in Figure 26 is the energy band diagram for this GaInP/GaAs HBT integrated with an NdS/GaInP/GaAs cold cathode structure.

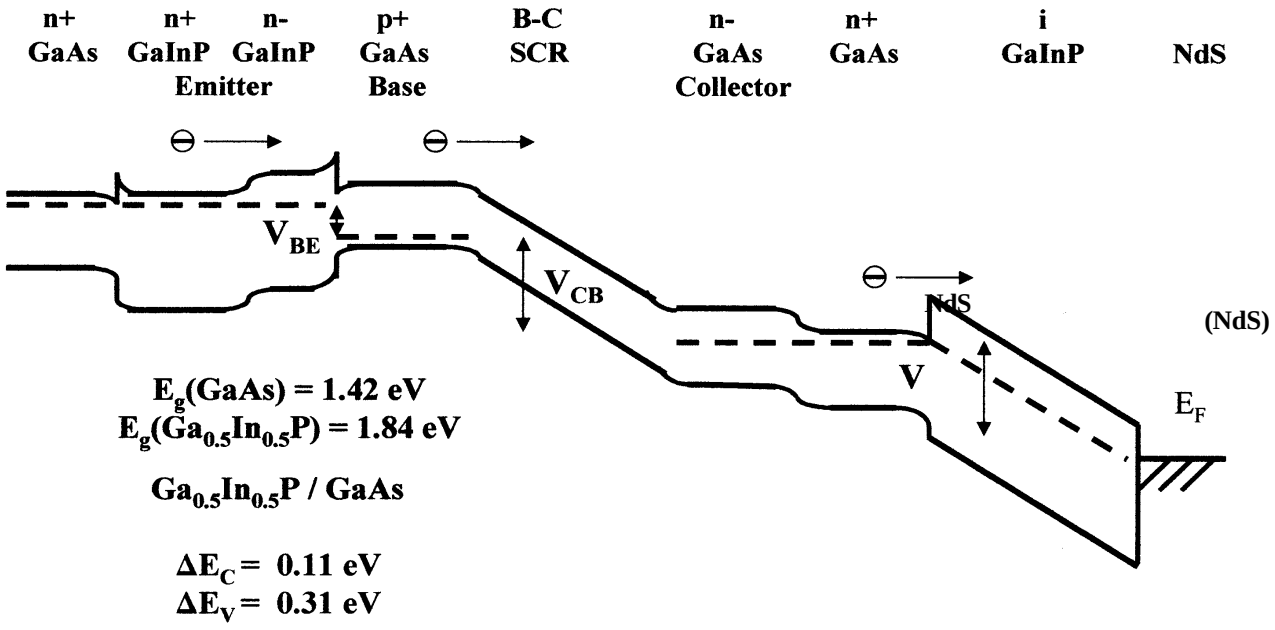


Figure 26. Energy Band Diagram for GaInP/GaAs Heterojunction Bipolar Transistor Integrated with a NdS/GaInP/GaAs Cold Cathode Structure.

In summary, monolithic integration of a III-V HBT with a cold cathode structure appears feasible and attractive. Our analysis shows that the collector-up device and vertical configuration are more attractive than the emitter-up device and lateral integration when the efficiency of the electron transfer is considered. However, further modeling of the integrated collector-up HBT and cold cathode structure is needed to determine the exact electron injection efficiency that can be achieved and the extent of its dependence on the integrated device's structure, e.g., collector contact size, emission window size, CdS thickness. As far as materials issues, integration of CdS/LaS/InP cold cathode with an InP-based HBT appears feasible. InP/InGaAs HBTs using an InP collector present some difficulty due to the conduction band discontinuity at the collector heterojunction, that requires a more complex epitaxy, e.g. compositional grading, to reduce the barrier. Newer InP/GaAsSb HBTs are more attractive since there is almost no conduction band discontinuity impeding electron injection into the InP collector. In addition, selective etching technology has been demonstrated in the fabrication of these InP/GaAsSb HBTs, which is important for fabricating high performance collector-up HBTs. GaAs-based HBTs are also possible using NdS. AlGaAs/GaAs HBTs are suitable, but newer GaInP/GaAs HBTs are more attractive for better device performance and reliability. In addition, selective etching has been developed and demonstrated for GaInP/GaAs HBTs, which is useful in fabricating the collector-up HBT.

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LIST OF ACRONYMS

AC	Alternating Current
BJT	Bipolar Junction Transistor
DC	Direct Current
DHBT	Double Heterojunction Bipolar Transistor
EU	Emitter Utilization Factor
HBT	Heterojunction Bipolar Transistor
MBE	Molecular Beam Epitaxy
MOCVD	Metal-Organic Chemical Vapor Deposition
TWT	Traveling Wave Tube