Analog CMOS Interface Circuits for UMSI Chip of Environmental Monitoring Microsystem

A report Submitted to Canopus Systems Inc.

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1. Overview

The objective of this project has been to implement the analog interface circuitry of the UMSI chip for the Environmental Monitoring Microsystem. This circuitry provides the readout for capacitive sensors, a resistive sensor, and interface for sensors with direct voltage output. The analog interface circuit block is highly programmable and provides offset and gain adjustments. It also supports self-test for physical capacitive sensors. This report describes the general architecture and detailed description of the design. Also simulated performance of the circuit is presented.

2. General Architecture

The overall architecture of the interface is shown in Fig 1. The circuit uses 6-to-1 input multipplexer to interface with up to 6 capacitive sensors, 6 resistive sensors, and 6 sensors with direct voltage output .

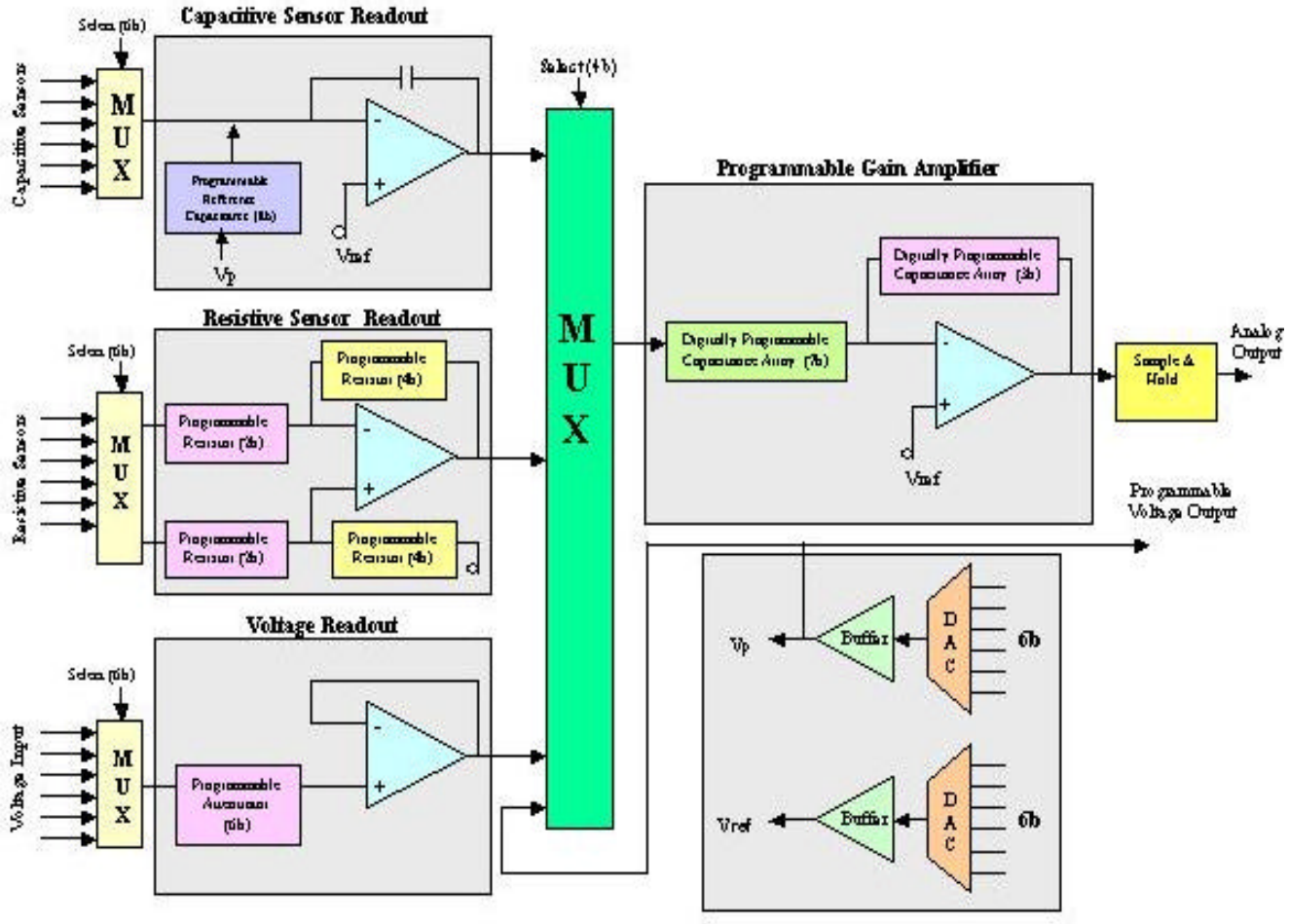

Fig. 1: Overall architecture of the UMSI chip analog interface.

Each of the individual readout blocks develops an output voltage proportional to the input parameter. The capacitive readout develops a voltage proportional to the difference in capacitance between a 'sense' capacitor and a reference capacitor. Similarly, the resistive sensor readout interfaces with a resistive sensor half or full bridge, and provides an output corresponding to the bridge resistor change. The voltage readout stage attenuates the input voltage change to a desired range. The output from the readout blocks is fed, via a multiplexer to a gain stage, which amplifies the input signal by a programmable factor to accommodate sensors with various sensitivities. The multiplexer allows output selected from any of the readout circuits to be amplified by the gain stage. The output voltage of this stage is finally stored on a capacitor in the sampled and hold stage

Additionally, there is a 6-bit DAC, or digital to analog converter, which is used to generate voltage Vp and Vref. The voltage Vref is applied to the capacitive sensor readout, programmable gain amplifier, and sample and hold stage so as to cancel any 'offset'. Offset is a non-ideality where there is an output signal present in the absence of any input signal. The voltage Vp is used for self-test of the physical capacitive sensor. Self test is performed by applying a pulse train of magnitude Vp to the capacitive sensor for a period of time, T_{test}. The resulting electrostatic force on plates of the physical capacitive sensor causes a change in its capacitance value of Δc. This value is then readout using the capacitive readout circuit. The values of T_{test},Vp and Δc can be used to establish whether the physical capacitive sensor is operating correctly or not.

In the next sections the architecture, operations and a representative simulation of each of these blocks will be presented in detail.

3. Capacitive sensor readout

The capacitive readout circuit uses a switched-capacitor front-end, as is shown in Fig. 2. This circuit detects the difference between input sense capacitor and reference capacitor, and provides an analog voltage proportional to the capacitance difference at the output.

3.1. Circuit Operation

During ϕ_1 (reset phase), the reset switch is closed and Cs and Cref are charged through the charge integrator output. At the end of the reset phase voltage across Cs is equal to Vref –Vp and hence the charge stored in Cs is equal to Cs (Vref-Vp), while the voltage across Cref is equal to Vref –Vss and hence the charge stored in Cref is equal to Cref (Vref-Vp). After ϕ_1(reset) goes low (integrate phase), the voltage across Cs changes to Vref –Vss and hence the change in the charge stored in Cs is equal to Cs (Vp-Vss), while the voltage across Cref changes to Vref –Vp and hence the change in the charge stored in Cref is equal to Cref (Vss-Vp). The net change in charge is (Cs-Cref) (Vp-Vss). This net change in charge is transferred to feedback capacitor. The magnitude of the output voltage will be equal to (Vp-Vss)(Cs-Cref)/Cf that is, the output voltage is proportional to the difference between the capacitance of the input sense capacitor and the capacitance of the reference capacitor. Note that a dummy switch ($reset_d$) is used to reduce clock switching noise at the high impedance nodes. (The dummy switches are designated using the subscript $_d$)

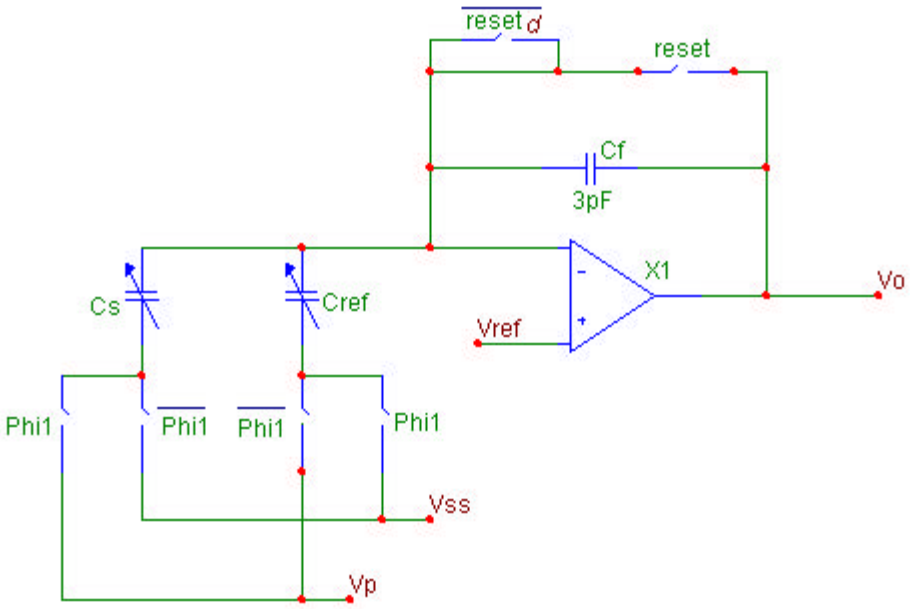

Fig. 2: Capacitive sensor readout circuit.

The building blocks of this circuit are the OTA (Operational Transconductance Amplifier), switches and capacitors. The switches are realized as fully complementary transmission gate. The reference capacitor is realized in a programmable form as shown in Fig. 3. The effective capacitance is the equal to the sum of the capacitors whose switches are closed. Thus the maximum value of capacitance happens when all switches are closed, and is equal to 12.75pF, and the minimum value of capacitance is 50fF.

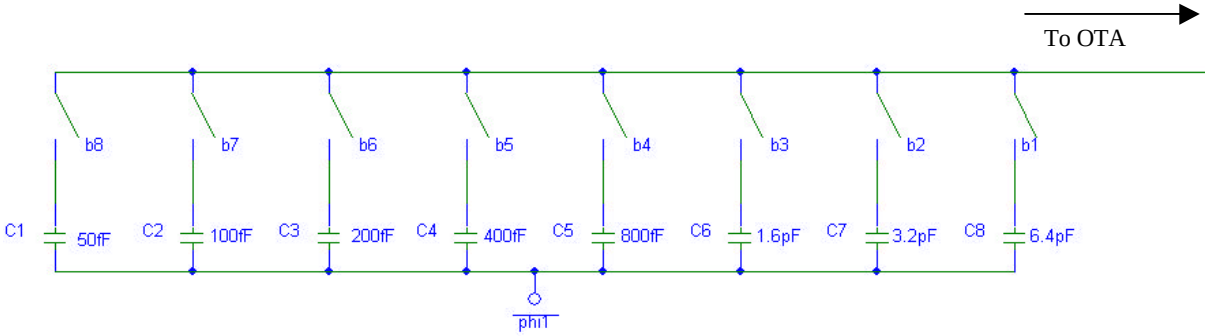

Fig 3: Schematic of 8-bit programmable reference capacitor array.

3.2. OTA Design

There are two main requirements on the OTA. A high gain is required to ensure precision operation. A rapid settling time is needed to ensure that the output settles to within a very small error in the half the clock period. The topology chosen to implement this OTA is an NMOS input folded cascode OTA. The schematic is shown in Fig. 4 . MN1-MN2 form the input differential pair, MN11 acts as the tail current source pair, MP5 MP6 are cascode transistors to the input differential pair, MP3 MP4 form the PMOS current source and MN7, MN8, MN9, MN10 form a wide swing cascoded NMOS current source.

As the load is purely capacitive and no output stage is required. A single stage op amp with a single high impedance node at the output is suitable. A cascode gain stage was selected for its high gain and its immunity from the Miller effect at high frequencies. The folded topology was used because this allows the input and output voltages to be at the same level. This feature is necessary because the input is shorted to the output for part of the operation (reset phase). NMOS input transistors are because the higher mobility of NMOS devices result in a higher transconductance and hence a higher gain and higher bandwidth than PMOS devices biased at comparable current levels

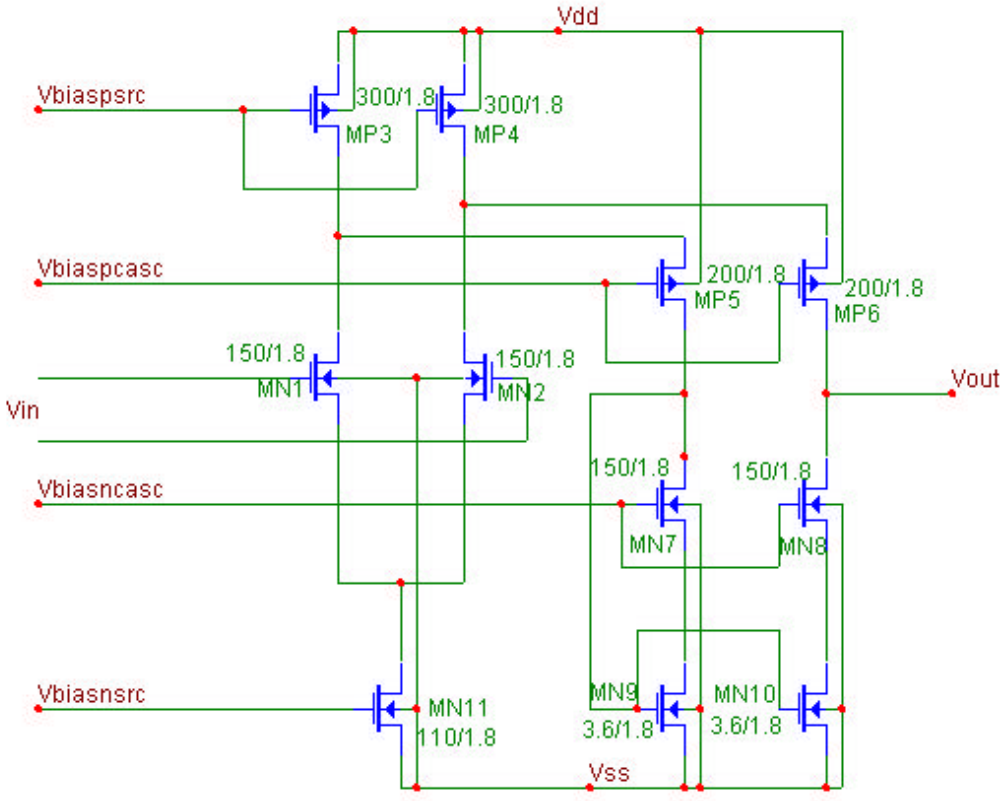

Fig. 4: Schematic of Folded Cascode amplifier.

3.3. Design Challenges

The most difficult specification to meet was to ensure that the quiescent output voltage was 1.5 V (half of the supply voltage). The nominal value of V_T for the N-mos device in our process was 0.655. Using a conventional cascode configuration, the quiescent output voltage would easily exceed 1.5V. With the wide swing cascode, however, this specification became easily achievable. The general advantage of this current mirror over the conventional cascode is that a wider output voltage swing is possible. In fact V_{out}(min) in a conventional Cascode is $V_T+2\Delta V$ (ΔV is the overdrive voltage) while for the wide-swing cascode it is just $2\Delta V$.

3.4. Bias circuit

The bias circuit that generates voltages V_{bias1} to V_{bias4} is shown separately with W/L ratios in Fig5. The circuit toplogy shown is known a wide swing constant transconductance bias circuit. The term wide swing is applied since all the current mirrors are wide swing cascode current mirrors. This biasing circuit has the property that the transconductance of any of the transistors in the bias loop is dependent **only** on W/L ratios and on the value of the resistor R_b.. The transconductance of the bias circuit determines the transconductance of the all transistors in the OTA. This endows the OTA as a whole with immunity towards process variations. This immunity with respect to process variations was observed by running OTA simulations with all process corners. This bias circuit is used to provide bias to all the OTAs in the switched capacitor readout circuit.

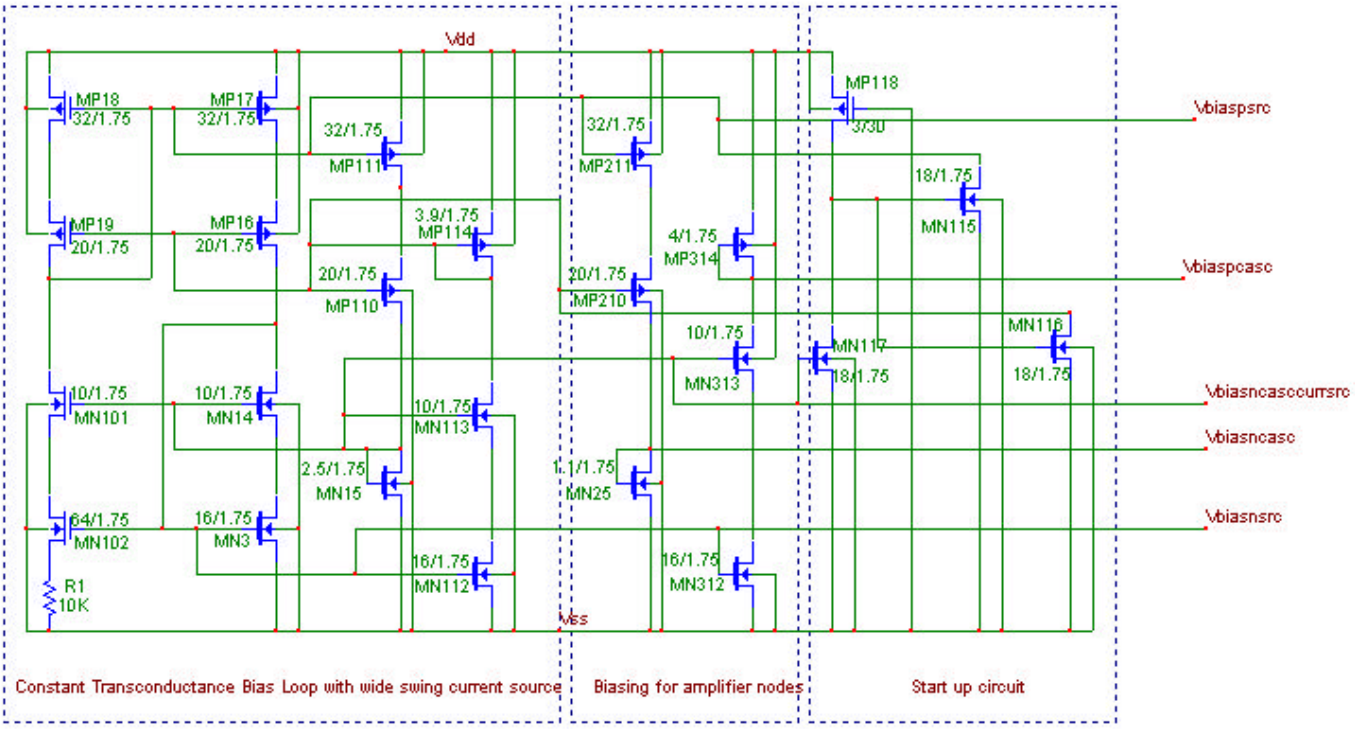

Fig. 5: Schematic of the OTA bias circuit.

3.5. Simulation Results

Various simulations were carried out using Star-HSPICE 2000.2. The results are tabulated below.

Table 1: Summary OTA simulated performance.

Parameter	**Value**
Low Frequency Gain	79 dB
Unity GBW	24MHz
Phase Margin	46 degrees
Slew Rate	49V/μs
Transient Settling Time (step size=1v)	33ns
Power Dissipation (with bias circuit)	< 1.1 mW @ 3V supply
Input/Output range	0.8 to 3V
CMRR	107dB (DC)
PSRR	80dB
Supply voltage	3V
Process Technology	0.35um AMI, 2P, 2M
Load Capacitance	3 pF

4. Resistive sensor readout

The resistive sensor develops a voltage that varies with resistance by using a resistive full bridge, which converts an imbalance in resistor values to a voltage. The schematic of resistive sensor readout is shown in Fig. 6.

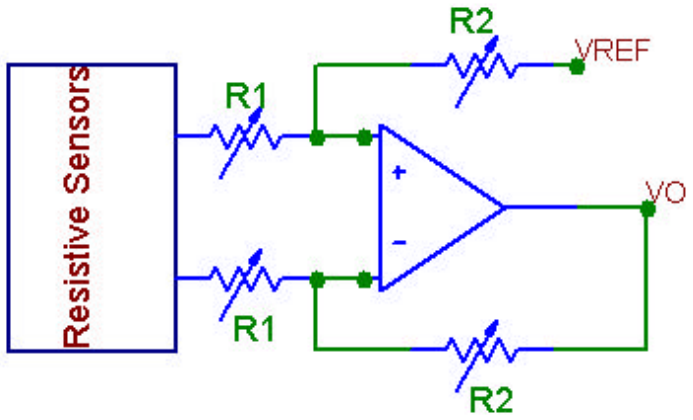

Fig. 6: Schematic of resistive sensor readout.

The bridge output voltage is applied to the input of a closed loop differential amplifier. The gain of this amplifier is given by the ratio of R2to R1 The building blocks of this circuit are the Opamp (Operational Amplifier), and resistors.. The resistors are realized in a programmable form as shown below in Fig. 7 and Fig. 8. The effective resistance is equal to the sum of resistors whose switches are open. For instance, in the case that both switches are open the resistance value is equal to 10KΩ.

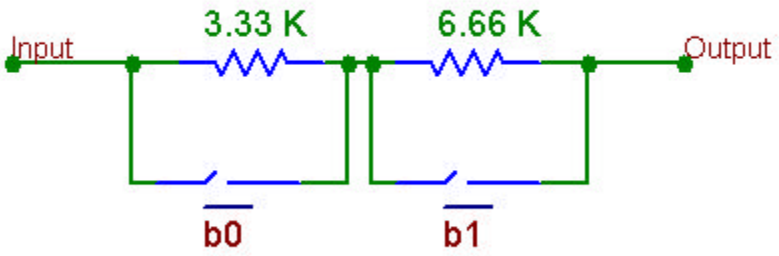

Fig. 7: Implementation of resistor R1 of Fig. 6.

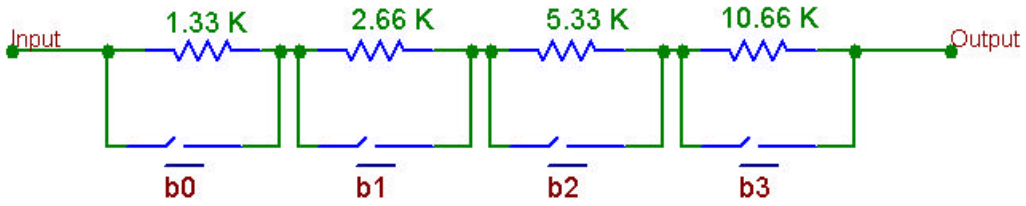

Fig. 8: Implementation of resistor R2 of Fig. 6.

4.1. Opamp design

There are three main requirements on the Opamp of the resistive sensor readout front-end. A high gain is required to ensure precision operation, large output voltage swing is required to accommodate a large output signal, and the output needs to be buffered to drive current into a resistive load.

.The opamp has a two stage topology, as illustrated in Fig. 9. The first stage is an NMOS input telescopic cascode. The second stage is a PMOS common source. . MN1-MN2 form the input differential pair, MN9 acts as the tail current source, MN3 MN4 are cascode transistors to the input differential pair, MP5 MP6 MP7 MP8 form a wide-swing cascaded PMOS current source, MP10 is a common source amplifier and MN11 is its current source,. CC is the miller compensating capacitor and R1 is the nulling resistor.

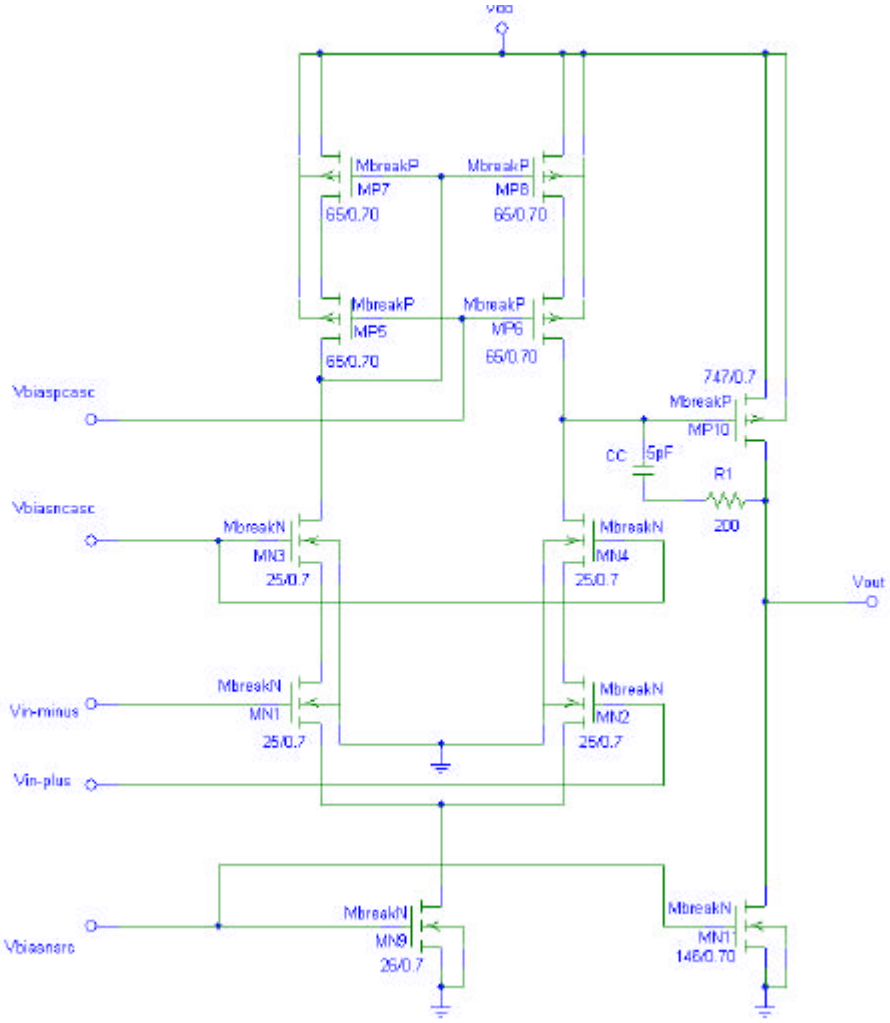

Fig. 9: Schematic diagram of two stage opamp.

The gain of the Opamp is derived mainly from the first stage while the swing is produced by the second stage. A telescopic cascode is chosen here because it dissipates about half the power of a folded cascode of comparable bandwidth. Miller compensation is used together with a nulling resistor so as to obtain a high phase margin with low power dissipation

4.2: Bias circuit

The bias circuit used is shown in Fig, 1A in Appendix A. The architecture is similar to the one used for the OTA, however, the sizes of the transistors used to bias the opamp nodes are different reflecting the differing bias voltage needs of the telescopic first stage.

4.3: Simulation results

A summary of the simulated performance of the designed opamp is presented in Table 2.

Table 2: Summary of the opamp simulated performance.

Parameter	**Value**
Low Frequency Gain	82 dB
Unity GBW	17.6HMHz
Phase Margin	86 degrees
Input/Output range	0.8 to 3V
CMRR	90dB (DC)
Power Dissipation	2.4 mW @ 3V supply
PSRR	80dB
Power supply	3V
Process Technology	0.35um AMI, 2P, 2M
Load resistor	10K

Also the resistive sensor circuit is simulated using output from a resistive full bridge so as to approximate as closely as possible operation using resistive sensor outputs. Figure 10 shows the schematic of the resistive bridge.

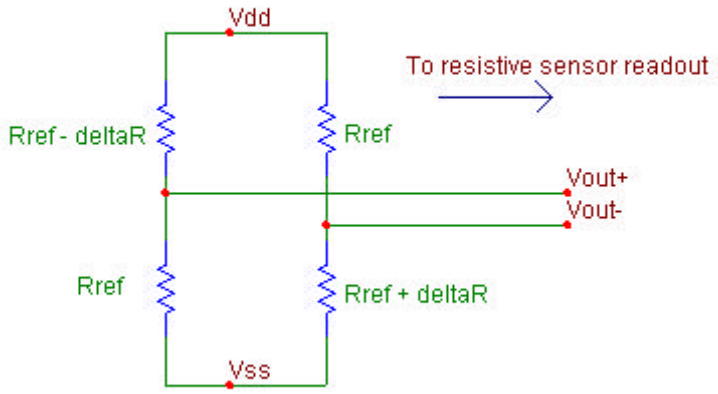

Fig. 10: Schematic of resistive full-bridge.

The value of delta R is swept, simulating a resistive sensor response to an input parameter. Figure 11 shows the output voltage plot. and voltage of the readout circuit plotted. This plot is given on the next page. It is clearly seen that the output voltage varies non-linearly with changes in resistance

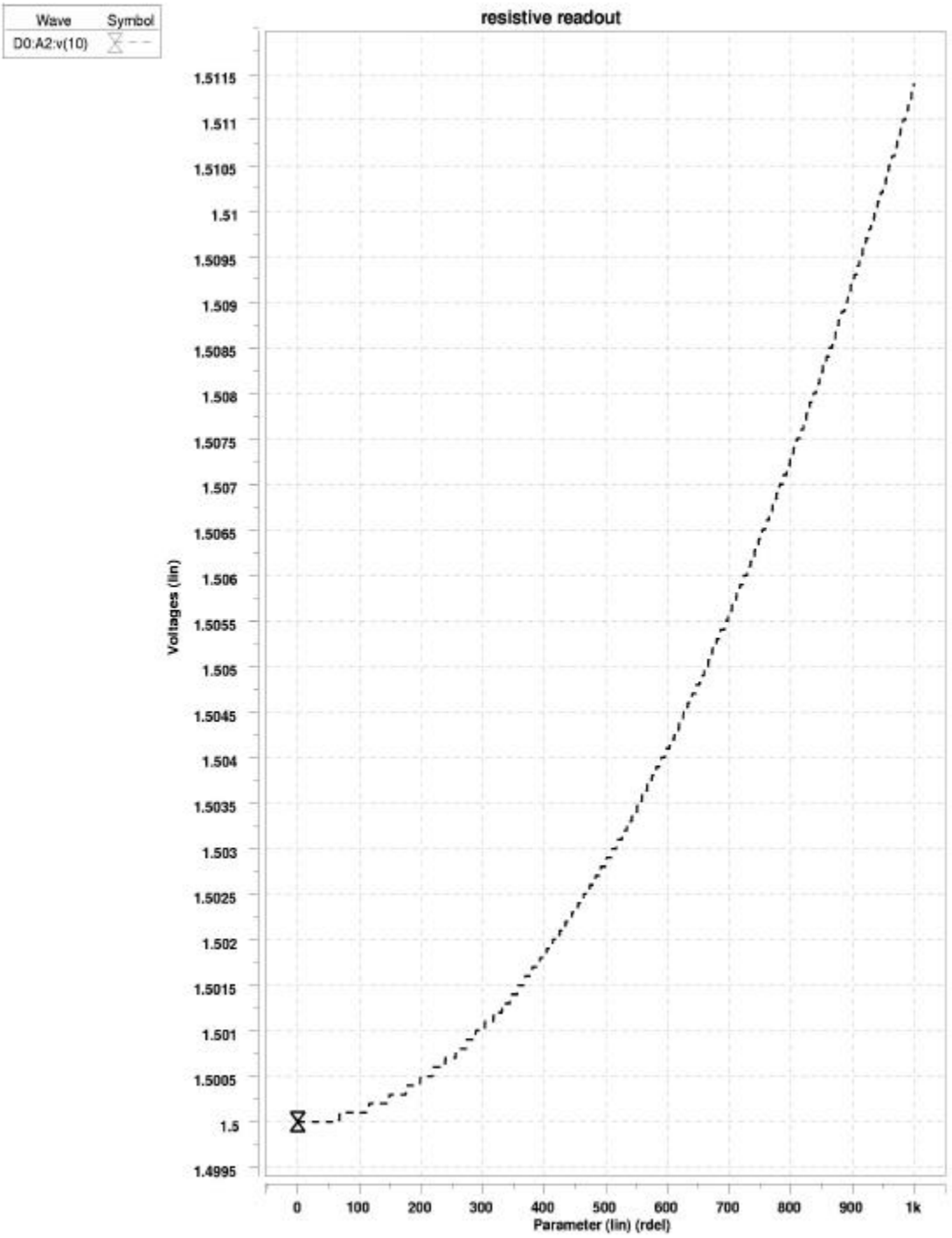

Fig. 11: Resistive readout output voltage versus resistance change.

5. Interface for sensors with voltage output

This block provides control over the voltage range, by attenuating it and feeding it to the programmable gain amplifier stage of the UMSI chip. The schematic of the voltage readout is shown in Fig. 12.

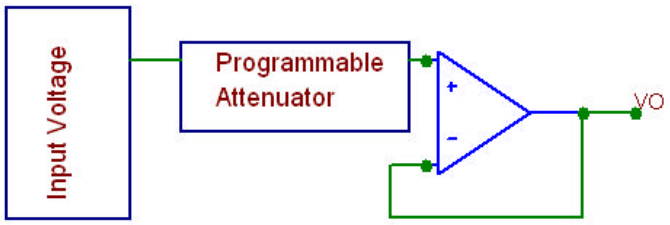

Fig. 12: Schematic diagram of the interface for sensors with voltage output.

The input voltage is attenuated by a programmable attenuator and is fed into the non inverting input of the opamp. The very high gain of the opamp forces the voltage at the inverting node (and hence the output voltage) to be equal to the voltage at the non inverting node. The function of the opamp is to provide buffering.

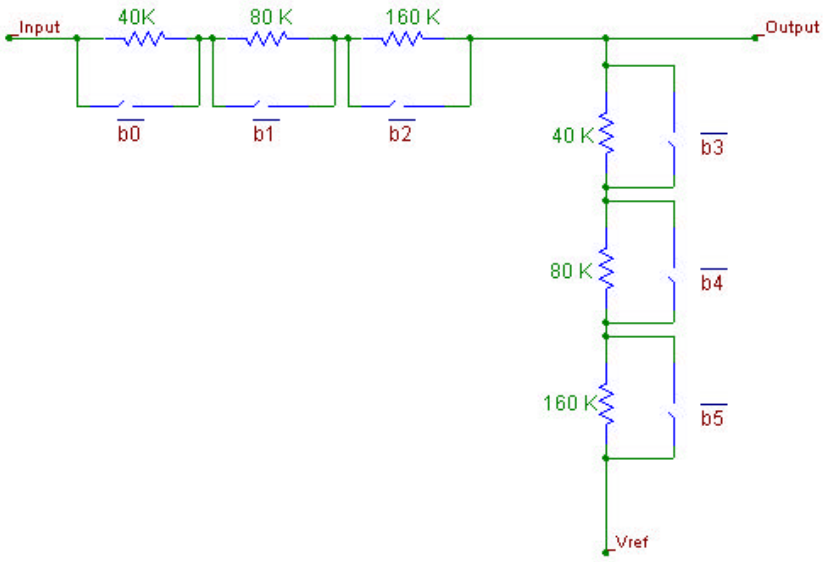

Fig. 13: Schematic of the programmable attenuator.

The input attenuator is implemented as shown below in Fig. 13. The programmable attenuator is implemented as a resistive divider. The attenuation coefficient is set by the positions of the switches. The effective resistance of each of the legs of the resistive divider is equal to the sum of resistors whose switches are open.

6. Programmable gain stage and sample and hold

This circuit amplifies the input voltage by a factor determined by ratio of capacitors Cin to Cf2 and holds this value at the output. The schematic of a programmable gain stage followed by sample and hold is shown in Fig. 14.

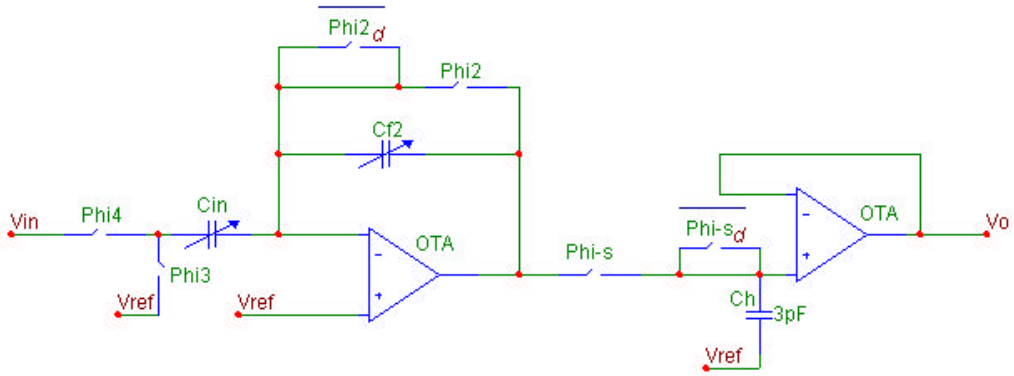

Fig. 14: Schematic of gain stage followed by sample and hold.

6.1. Circuit Operation:

ϕ_s (ϕ_3) and ϕ_2(ϕ_4) are non overlapping clocks. During ϕ_2 (ϕ_3)(sample phase), the reset switch is closed and Cin is charged through the charge integrator output. At the end of the reset phase voltage across Cin is equal to Vin–Vref and hence the charge stored in Cin is equal to Cin (Vin-Vref). After ϕ_3 goes high (integrate phase), the voltage across Cin changes to zero and hence the change in the charge stored in Cin is equal to Cin (Vin-Vref). This change in charge is deposited on the left plate of the feedback capacitor (a charge of equal magnitude and opposite polarity made available through the output is deposited on the right plate of the feedback capacitor). The magnitude of the output voltage will be equal to (Vin-Vref)(Cin)/Cf2 that is, the output voltage is scaled by the ratio of Cin to Cf2 . Note that a dummy switch ($reset_d$) is used to reduce clock-switching noise at the high impedance nodes. (The dummy switches are designated using the subscript $_d$)When ϕ_3 is high ϕ_s is also high and this output voltage is sampled onto the capacitor Ch and held there until ϕ_s goes high again. During this time the output of the sample and hold equals the last output of the programmable gain stage.

The OTA, bias circuit and switches used in this circuit are same as the ones used in the capacitive readout.. The input capacitor Cin and the feedback capacitor Cf2 are realized in a programmable form as shown below in Fig. 15 and Fig. 16. The effective capacitance is the equal to the sum of the capacitors whose switches are closed. The combination of the two programmable capacitors provides 1024 different gain settings varying from 0.25 to 31.75.

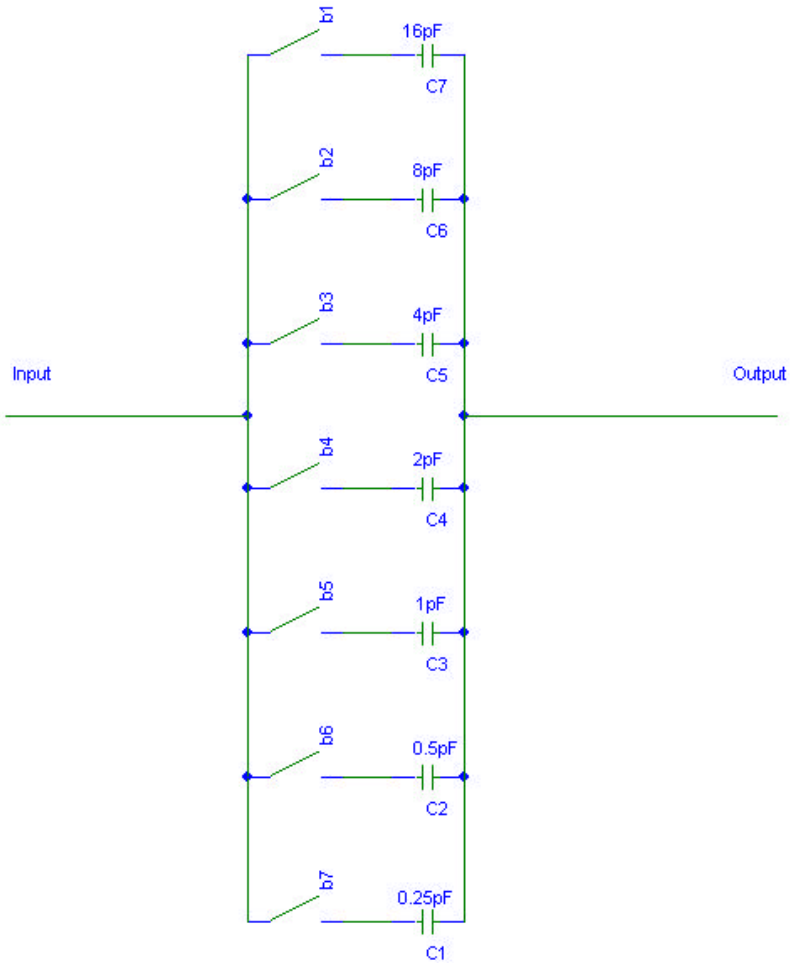

Fig 15: Schematic of 7-bit programmable input capacitor array.

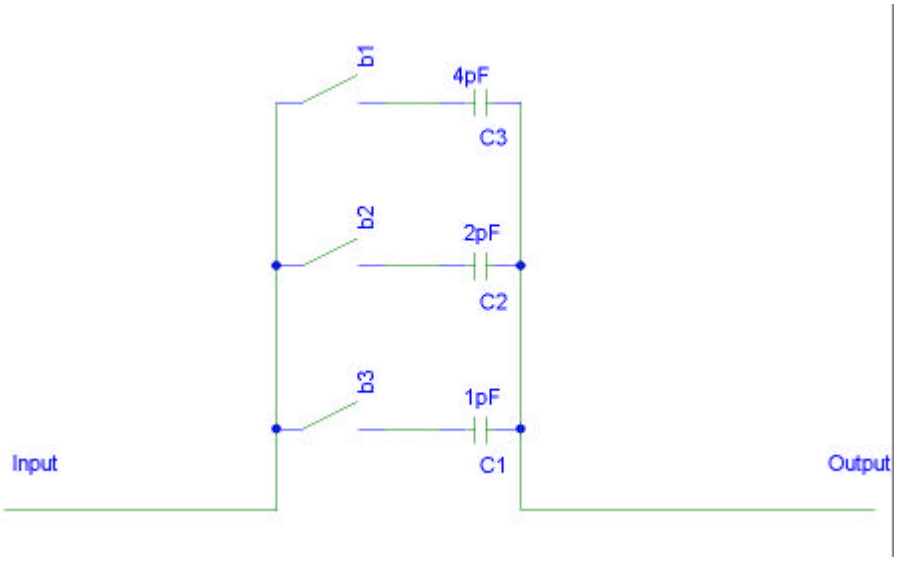

Fig. 16: 3-bit digitally programmable capacitive array connected as a feedback capacitor across the gain stage

6.2. Capacitive readout interfaced with programmable gain and sample & hold stage.

In order to illustrate one possible path through the interface circuit we have chosen the example of capacitive readout interfaced with programmable gain and sample & hold stage.

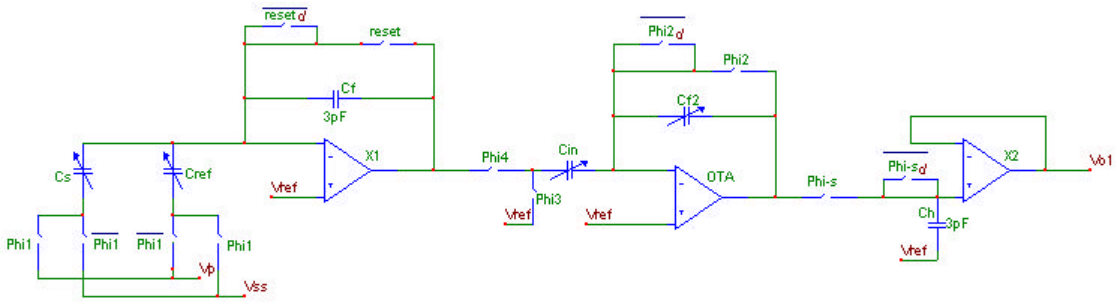

Fig. 17: Schematic of capacitive readout interfaced with programmable gain and sample & hold stage.

ϕ_1 and ϕ_2 are two non-overlapping clocks. During ϕ_1, the reset switch of the charge integrator is closed and Cs is charged through the charge integrator output. Once ϕ_1 goes low, a packet of charge proportional to the difference between Cs and Cref is integrated on the feedback capacitor. Next as ϕ_2 goes high, the second stage is reset and, Cin charge to the output level of the first stage. The gain of the second stage is determined by the ratio of the total capacitance switched into its input to the feedback capacitance Cf2. Clock phases ϕ_3 and ϕ_4 are slightly delayed ϕ_1 and ϕ_2 clock phases Finally, the output of the second stage is sampled and held at the input of the third stage during ϕ_s.

6.3. Simulation Results

The circuit was simulated using the capacitors values shown in Table 3. Vref is taken to be 1.5v Vp is taken to be 3 V, Vss =0V. The clocks had a frequency of 2/3 MHz. The non-overlap time of the clock phases was 250 ns. The clock delays are 100 ns. The simulation output waveform is presented in Fig. 18.

Table 3: The capacitor values used in the capacitive readout, programmable gain amplifier, and sample & hold simulations.

Capacitor	Value
Cs1	3.2pF
Cref1	3pF
Cf1	3pF
Cin	9pF
Cf2	3pF
Ch	3pF

This graph shows the clock phase ϕ_s (dotted line) well as the output voltage (solid line). The result shows that for an input capacitance difference of 0.2pF the output voltage changes by 0.6V.This predicted by equation $\Delta Vout = (\Delta C/Cref)*(Cin/Cf2)*(Vp-Vss)$.

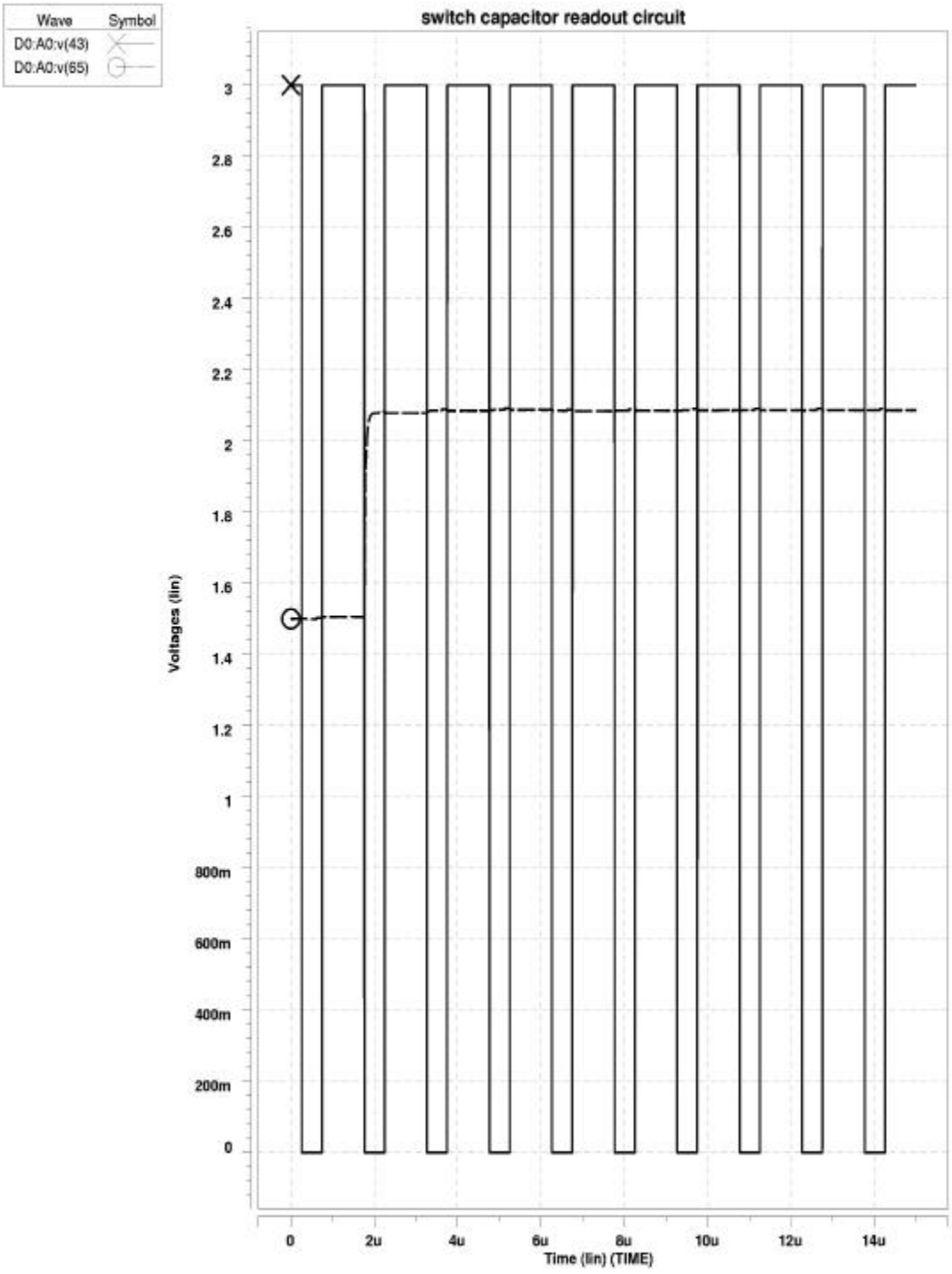

Fig. 18: Simulated output of the capacitive readout, programmable gain amplifier, and sample & hold stage.

7. Digital-to-Analog Converter (DAC)

Figure 19 shows the schematic of the 6 bit DAC. This circuits converts an input digital signal represented by bits b1to b6 to an analog output. Bits b6 thru to b1 sets the voltage at the non-inverting node of the opamp by directing the current from the respective current sources to flow through the 3K resistor. The voltage at the non-inverting node of the opamp is an IR1 drop below the positive power where I is the total current flowing through the resistor R1. That is this voltage is proportional to current I. The relation between the input digital code to the output analog voltage is inverting, which corresponds to a linearly decreasing output voltage as the input code is incremented. The very high gain of the amplifier forces the voltage at the inverting node and hence the output voltage to be equal to voltage of the noninverting node. As a result we have an output voltage which proportional to current I. The function of the opamp is to provide buffering. Note the current source labeled Ibias is used to set the output voltage that results when all switches to current sources. This voltage is set so that we have an voltarge range for the DAC which is symmetric around analog ground. For our design we have chosen an output voltage range from 0.5V to 2.5V.

The building blocks of this circuit are the Opamp (Operational Amplifier), and switched current sources. The switched current sources are realized as shown in Fig. 20.

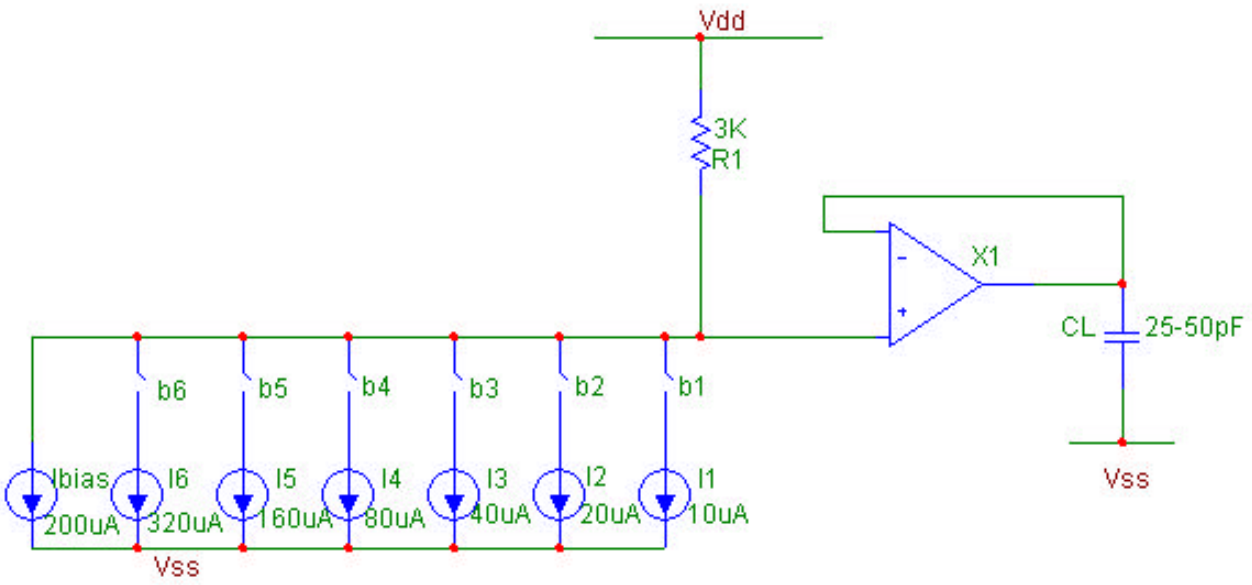

Fig. 19: Schematic of 6 bit current steering DAC.

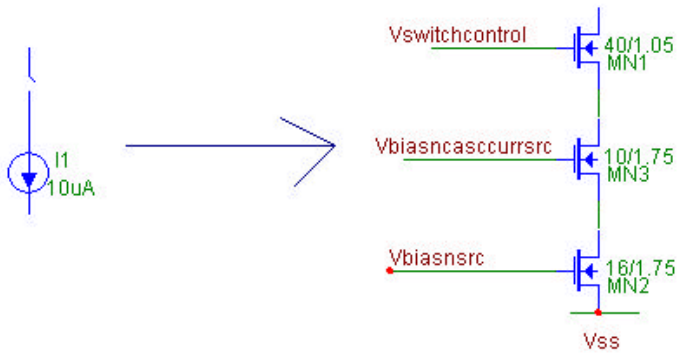

Fig. 20: Implementation of switched current source.

The other current sources are realized by combining in parallel several of the current sources shown in Fig. 20. For instance, the 20uA current source is realized by connecting two of the 10uA current sources in parallel, and the 320uA current source is implemented by connecting 32 of 10uA sources together in parallel.

7.1. Opamp design

The requirement for this opamp is the same as the requirements for the opamp used for the resistive sensor readout except that it is required to be able to drive a varying capacitive load and lower of a resistive load. Thus the power dissipation can be reduced since the resistance load requirement is relaxed. The Opamp topology chosen, is identical to the resistive readout Opamp, and is shown in Fig. 21. The transistors have been resized to reflect the difference in drive requirements.

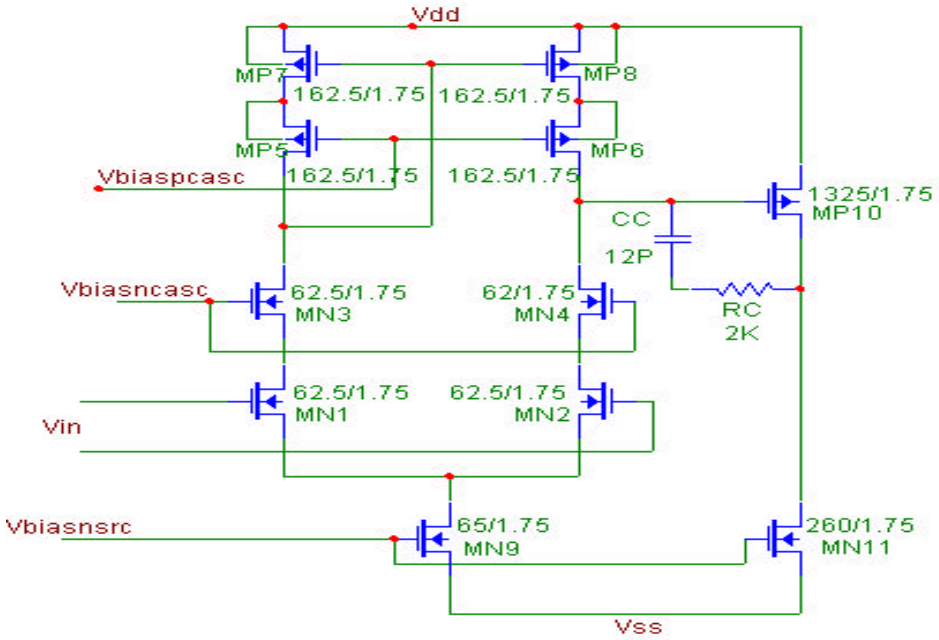

Fig. 21: Schematic of opamp used in DAC

7.2. Bias circuit

The bias circuit used is shown in Fig. 2A of Appendix A. The architecture is similar to the previously presented bias circuits in this report, however, the sizes of the transistors used to bias the opamp nodes are changed to reflect the different bias voltage needs of this opamp.

7.3. Simulation results

The simulated performance of the DAC opamp is presented in Table 3. The load capacitances in the simulations were deliberately chosen to be large values. The reason for this choice is that the phase margin for two stage amplifiers *decrease* with *increasin*g load capacitance. So if we verify that the amplifier has a high phase margin for a 50 pF load capacitance, the stability for smaller capacitive is verified as well. Also note the amplifier has a large dc gain, which provides better than 11b accurate unity gain buffer for input voltage range from 0.5V to 2.5V.

Table 3: Summary of the DAC opamp simulated performance.

Parameter	**Value**
Low Frequency Gain	120 dB
Unity GBW	6 MHz with load capacitance = 25 pF 5 Mhz with load capacitance = 50 pF
Load Capacitance	25-50pF
Phase Margin	89 degrees with load capacitance = 25 pF 73.8 degrees with load capacitance = 50 pF
Input/Output range	0.8 to 3V
CMRR	90dB (DC)
Power Dissipation	780uW @ 3V supply
PSRR	80dB
Power supply	3V
Process Technology	0.35um AMI, 2P, 2M

The DAC was simulated, stepping the bits controlling the switched current sources from 000000 all the way up to 111111 one bit at a time. The simulation waveform is presented in Fig. 21. The output has a descending staircase shape that corresponds to the inverting relation between the input digital code to the output analog voltage. The output steps down uniformly in response to uniform periodic increments in input all the way from 2.5V to 0.5V

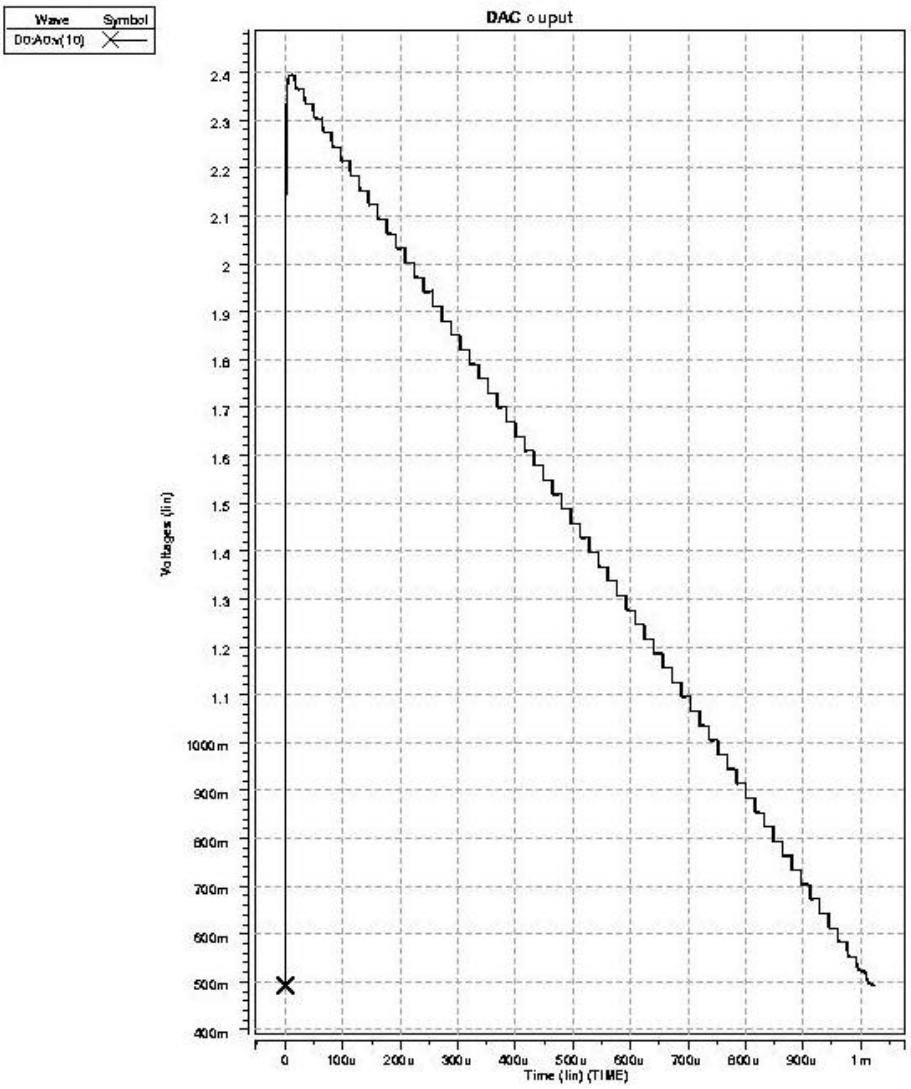

Fig. 21: Simulated output of the DAC as the input digital code is incremented.

The DAC circuit was also simulated to make sure that the worst case settling time (that is transition from all switches closed to all switches open or vice versa with load =50pF) is less than 10us. The result of this simulation is presented in Fig. 3A in Appendix A. The graph shows the output of the DAC (opamp output) along with the non-inverting input to show the settling

Analog ground (Vref) generation.

The buffer used for the DAC can also be used to generate the Vref analog ground signal. The voltage between the positive power supply and ground is divided by two. The divider is formed by two the resistive R1 and R2 as is shown in Fig. 21. This voltage is applied to the non-inverting terminal of the opamp. The very high gain of the opamp forces the voltage at the inverting node (and hence the output voltage) to be equal to the voltage at the non-inverting node. The function of the opamp is to buffer the voltage.

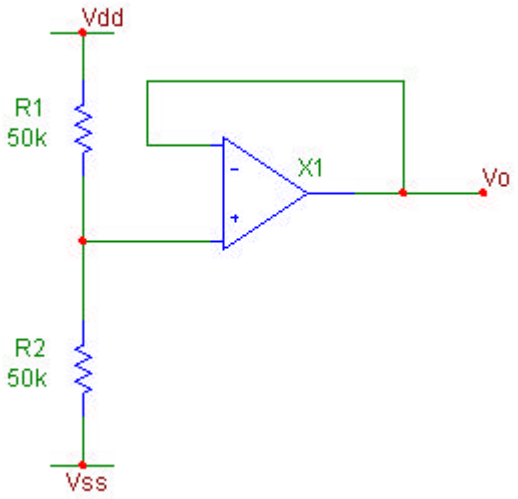

Fig. 22: Schematic of Vref (Analog ground) generator.

Appendix A

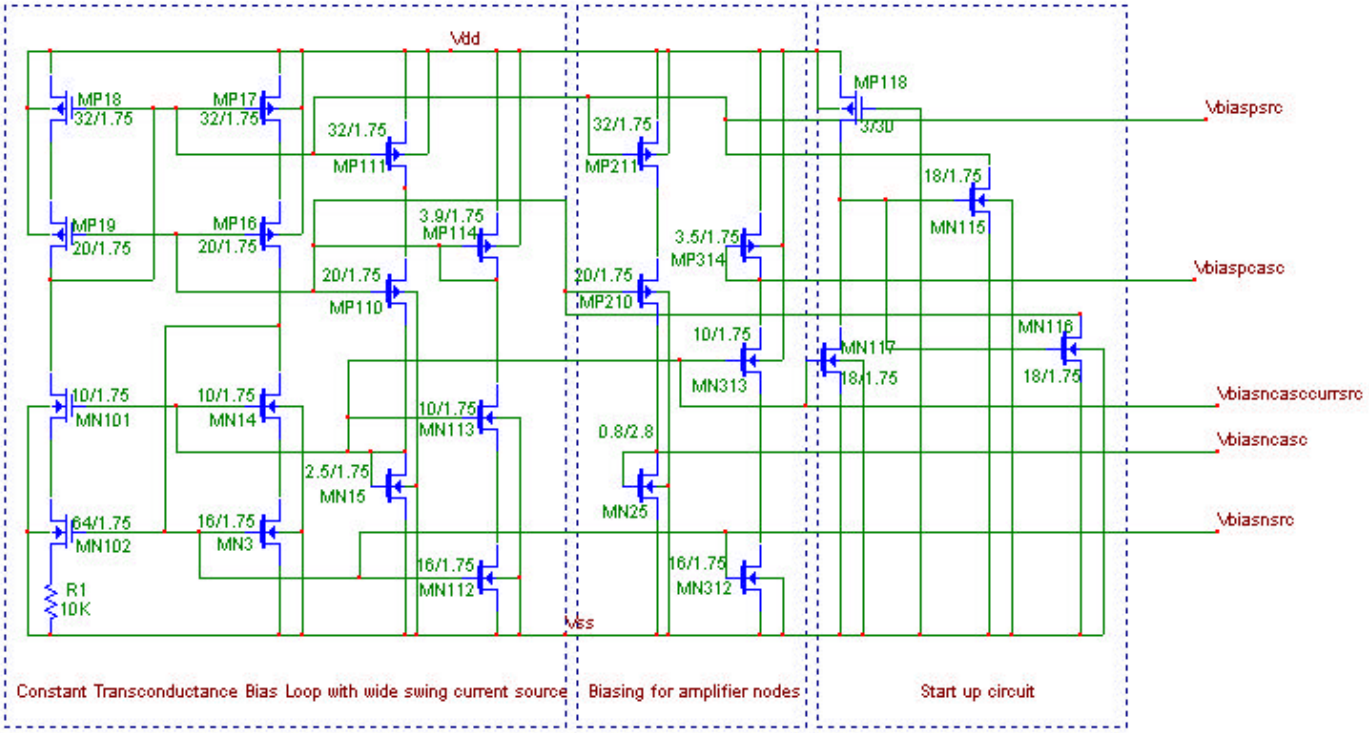

Fig. 1A: Bias circuit for resistive readout opamp.

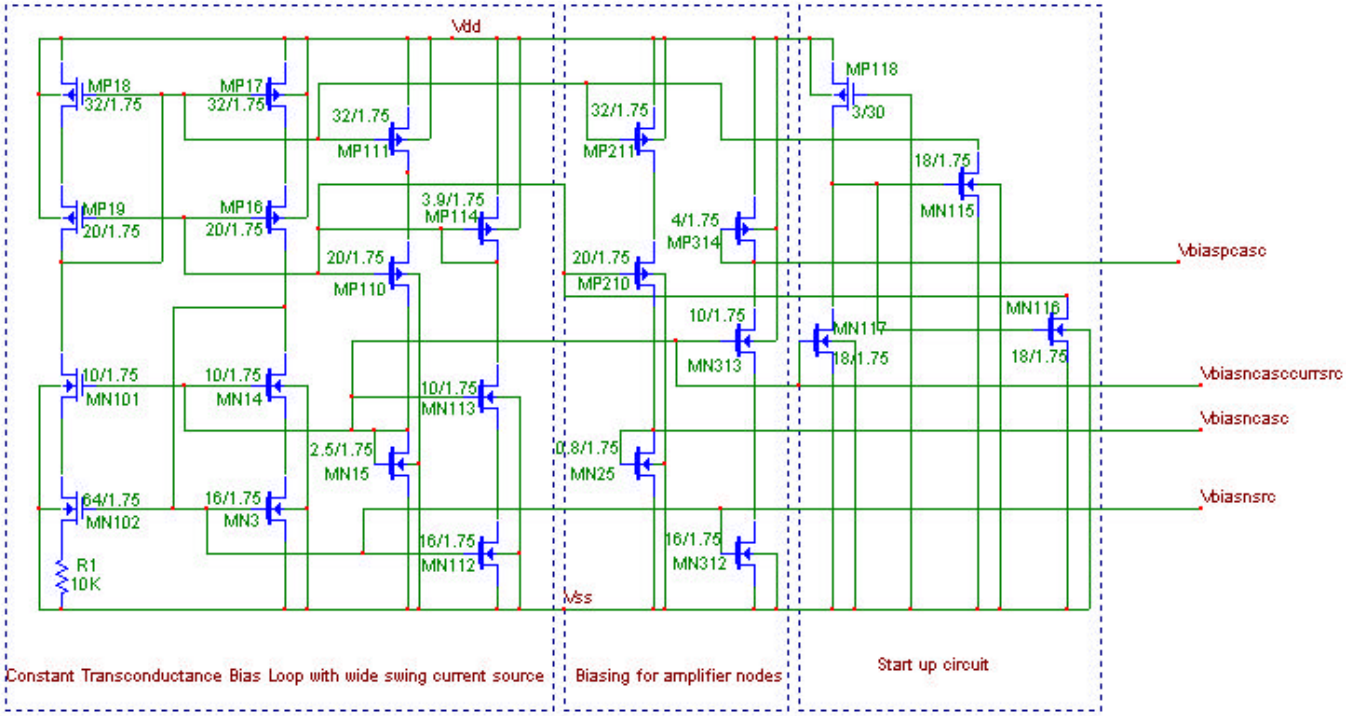

Fig. 2A: Bias circuit for DAC opamp.

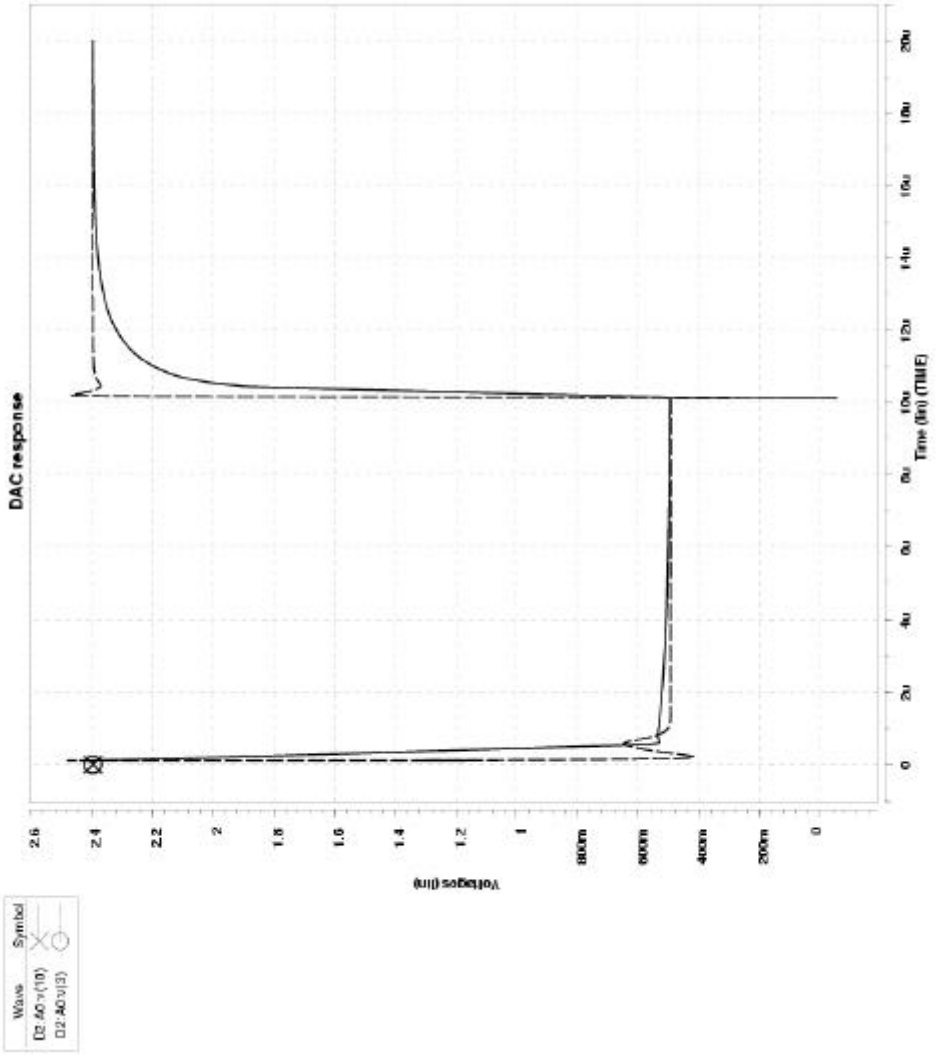

Fig3A: Worst case settling time for DAC.