

# REPORT DOCUMENTATION PAGE

Form Approved  
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Service, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington, DC 20503.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY) 02-07-2002		2. REPORT DATE July 2, 2002		3. DATES COVERED (From - To) July 31, 1996 - Dec. 01, 2002	
4. TITLE AND SUBTITLE  Large area heteroepitaxial growth using compliant substrates				5a. CONTRACT NUMBER N00014-96-1-1179	
				5b. GRANT NUMBER N00014-96-1-1179	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S)  Wen I. Wang, Professor				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)  Department of Electrical Engineering Columbia University 500 W. 120th St. New York, NY 10027				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)  Office of Naval Research Ballston Center Tower One 800 North Quincy Street Arlington, VA 22217-5660				10. SPONSOR/MONITOR'S ACRONYM(S)	
				11. SPONSORING/MONITORING AGENCY REPORT NUMBER	
12. DISTRIBUTION AVAILABILITY STATEMENT  Distribution unlimited					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT  In situ relaxed SiGe epitaxial layers with low threading dislocation densities grown on compliant Si-on-insulator substrates was achieved. The first semi-quantitative theory for the mechanism of the reduction of dislocation density in epilayers grown on compliant substrates was developed. High mobility two-dimensional electrons in AlGaIn/GaN heterostructures were prepared on sapphire substrates by molecular beam epitaxy (MBE). Sb was used for the first time as surfactant to improve the growth of GaN. Also reported are many firsts, including the exploitation of strain-modulated epitaxy, the use of LGO substrate for GaN substrate removal, and the demonstration of GaN devices bonded to Si enabled by bonded substrate removal.					
15. SUBJECT TERMS					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON Wen I. Wang
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER (Include area code) 212-854-1748, 212-854-3105

20020717 125

OFFICE OF NAVAL RESEARCH

Final Technical Report

FOR

31 July 1996 through 01 December 2001

\*\*\*\*\*

Grant Number: ONR N00014-96-1-1179

TITLE OF GRANT: Large area heteroepitaxial growth using compliant substrates

NAMES OF PRINCIPAL INVESTIGATOR: Professor Wen I. Wang

(subcontractors: Prof. April Brown at Georgia Tech, Prof. Lester Eastman at Cornell University, Prof. T.S. Kuan at SUNY Albany)

NAME OF ORGANIZATION: Electrical Engineering Department,  
Columbia University

ADDRESS OF ORGANIZATION: Electrical Engineering Department,  
Columbia University, 500 West 120th Street, New York, N.Y. 10027

\*\*\*\*\*

Reproduction in whole, or in part, is permitted for any purpose of the  
University States Government.

This document has been approved for public release and sale: its distribution is unlimited.

The objective of this MURI grant was to develop large area heteroepitaxial growth using compliant substrates by molecular beam epitaxy. The MURI grant was led by Columbia University (Prof. Wen I. Wang), with participants including Prof. April S. Brown at Georgia Tech, Prof. Lester F. Eastman at Cornell University, and Prof. T.S. Kuan at SUNY Albany.

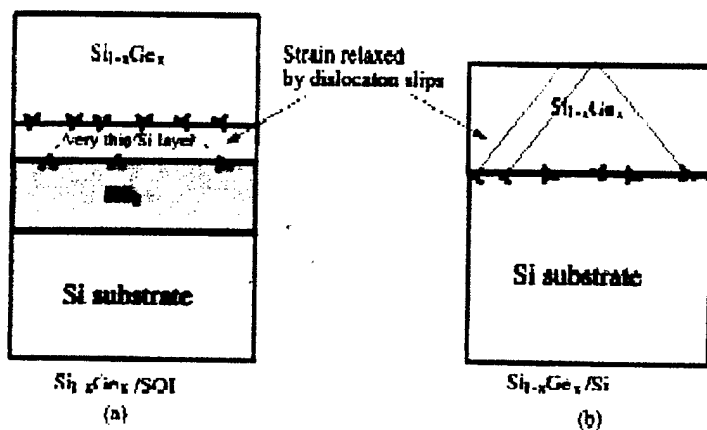
## Technical Achievements

### Columbia University achieved

#### **In situ relaxed SiGe epitaxial layers with record low threading dislocation densities grown on compliant Si-on-insulator substrates**

High quality relaxed  $\text{Si}_{0.6}\text{Ge}_{0.4}$  films as thick as  $1.0\ \mu\text{m}$  have been achieved as grown on silicon-on-insulator (SOI) substrates with  $200\ \text{\AA}$  Si(100)-oriented compliant substrates. This represents the thickest relaxed layers grown by this technique. A greater than five order of magnitude reduction in threading dislocation density was achieved by compliant growth compared to growth on unmodified Si (100) substrates. Additionally, for the first time, we show that it is not necessary to separate the growth and relaxation processes, and relaxation during growth is governed by the nature of the compliant substrate structure that causes dislocations to terminate at the unique crystalline-amorphous  $\text{SiO}_2$  interface. Results indicate that utilizing SOI as a compliant substrate which is effective in producing high quality  $\text{Si}_{1-x}\text{Ge}_x$  films can be extended to other films, where film relaxation ~via dislocation nucleation and growth cannot be conveniently separated from the synthesis method.

Columbia University achieved nearly dislocation-free SiGe epilayers by MBE growth on the SOI compliant substrates. There is not a single dislocation was observed in the  $\text{Si}_{0.6}\text{Ge}_{0.4}$  film grown on SOI substrate at Columbia University. All the dislocations are confined in the thin Si layer of the SOI substrate, indicating the net dislocation image force was toward the SOI substrate. The compliant substrate properties are clearly demonstrated by this TEM result. At least five orders of dislocation density improvement in the  $\text{Si}_{0.6}\text{Ge}_{0.4}$  relaxed film has been achieved by using SOI substrate instead of straight Si substrate. To the best of our knowledge, it is the first time achieving this high quality relaxed  $\text{Si}_{0.6}\text{Ge}_{0.4}$  films as thick as  $1.0\ \mu\text{m}$  directly on SOI. A key feature here is that relaxation was achieved during film growth ~*in situ!* and not separately postgrowth annealing!. Results indicate that the SOI substrate with a  $200\ \text{\AA}$  top Si layer is compliant at all practical temperatures, and compliancy is not necessarily related to the SOI fabrication technique or the nature of the Si/SiO<sub>2</sub> interface. The effectiveness of the as-grown SOI technique in achieving device-quality relaxed SiGe films is, thus, clearly demonstrated.



Dislocation formation in (a)  $\text{Si}_{1-x}\text{Ge}_x$  films on SOI compliant substrate and (b)  $\text{Si}_{1-x}\text{Ge}_x$  film on straight  $\text{Si}$  substrate.



Cross-sectional TEM of the  $\text{Si}_{0.6}\text{Ge}_{0.4}$  film as thick as  $1.0 \mu\text{m}$  film grown on (a) SOI(001) substrate and (b) Si(001) substrate.

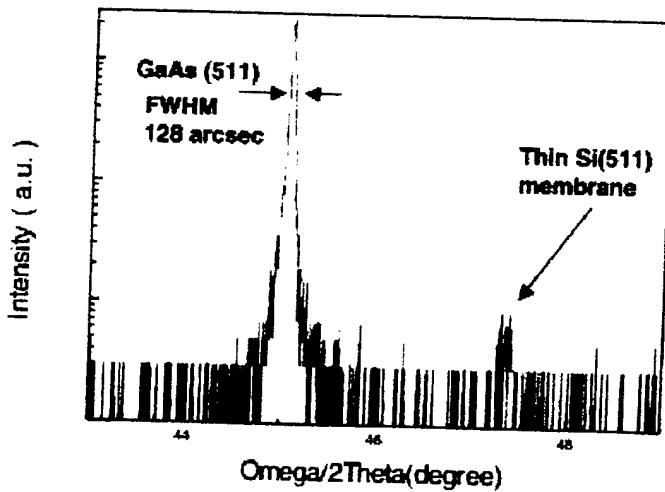
## **Columbia University developed the first semi-quantitative theory for the mechanism of the reduction of dislocation density in epilayers grown on compliant substrates, in collaboration with SUNY Albany**

A simplified model of the mechanism of dislocation reduction in epilayers grown on compliant substrates by molecular-beam epitaxy has been developed based on the dislocation theory and detailed experiments. Theoretical results calculated with this model indicate that up to 100-fold defect reduction can be achieved by using a silicon-on-insulator compliant substrate for the thick epilayer growth as compared to that of using a conventional Si substrate. The advantage of growing thick epilayers on compliant substrates can be predicted quantitatively. The mechanism of a nearly dislocation-free SiGe alloy, as well as GaAs epilayers grown on silicon-on-insulator compliant substrates, is explained and the dislocation density calculated with this model is in good agreement with our experimental results.

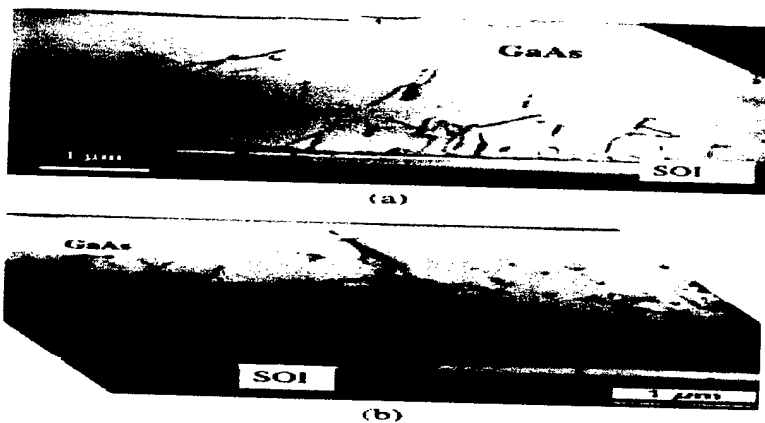
With these quantitative expressions, our model can estimate the number of dislocations attracted and annihilated at the epilayer/Si/oxide interfaces and the associated strain relaxation accomplished. The model also considers the tensile stress in the oxide layer caused by the thermal mismatch at a high growth temperature, which provides another driving force for dislocations to slip toward the epilayer/Si/oxide interfaces. Using this model, the dislocation densities were calculated for the SiGe epilayers (with 2% lattice mismatch to Si) with different thicknesses of 10, 100, and 1000 nm grown on SOI compliant substrates. Table I shows the calculated results. For comparison, the calculated results for other epilayers grown on conventional Si substrates are also shown in Table I. It suggests that 100-fold defect reduction can be achieved by using a SOI compliant substrate as compared to that of using a conventional Si substrate for epitaxial growth. The model estimates the dislocation density in the SiGe epilayer with thickness of 1  $\mu\text{m}$  grown on a SOI compliant substrate (with the thin Si membrane of 100 nm) can be as low as 16 per square centimeter, which is much less than the dislocation density of 3000 per square centimeter in the SiGe epilayer with the same thickness grown on the Si conventional substrate as indicated in Table I. In our experiment of SiGe compliant growth, a level of  $5 \times 10^8/\text{cm}^2$  dislocation density was observed near the SiGe/SOI interface by TEM. These dislocations remain close to the edges of SiGe/Si/SiO<sub>2</sub> interfaces due to attraction by the image force from the oxide layer. It is clear that SOI compliant substrates are effective in producing high-quality SiGe epilayers. With this model, the mechanism of the reduction of the dislocation density can be explained for the thick SiGe and GaAs epilayers with very low dislocation density grown on SOI compliant substrates. The advantage of growing thick epilayers on compliant substrates can be predicted quantitatively. The theoretical data calculated with this model are in good agreement with previous and our experimental findings.

Epilayer thickness (nm)	Dislocation density in epilayers	
	grown on Si	grown on SOI
10	$5.4 \times 10^{10}/\text{cm}^2$	$5.4 \times 10^9/\text{cm}^2$
100	$1.6 \times 10^7/\text{cm}^2$	$1.6 \times 10^5/\text{cm}^2$
1000	$3.0 \times 10^3/\text{cm}^2$	$16/\text{cm}^2$

Theoretical dislocation density in SiGe (2% mismatch) grown on conventional Si substrates and SOI compliant substrates.



X-ray diffraction from a 3- $\mu\text{m}$ -thick GaAs epilayer grown on the SOI compliant substrate which has a 100 nm Si (511) membrane. The smaller peak located at  $47.48^\circ$  comes from this thin membrane.



Cross-sectional transmission electron microscopy of GaAs grown on SOI (511) compliant substrates with a 100 nm Si thin membrane (a), and with a 200 nm Si thin membrane (b).

## Columbia University demonstrated

### **the highest two-dimensional electron mobility in AlGaN/GaN heterostructures grown on sapphire substrates entirely grown by molecular-beam epitaxy**

High-quality AlGaN/GaN heterostructures have been grown by ammonia gas-source molecular-beam epitaxy on sapphire substrates. Incorporation of a low-temperature-grown AlN interlayer during the growth of a thick GaN buffer is shown to substantially increase the mobility of the piezoelectrically induced two-dimensional electron gas (2DEG) in unintentionally doped AlGaN/GaN heterostructures. For an optimized AlN interlayer thickness of 30 nm, electron mobilities as high as 1500 cm<sup>2</sup>/V s at room temperature, 10 310 cm<sup>2</sup>/V s at 77 K, and 12 000 cm<sup>2</sup>/V s at 0.3 K were obtained with sheet densities of 9×10<sup>12</sup> cm<sup>-2</sup> and 6×10<sup>12</sup> cm<sup>-2</sup> at room temperature and 77 K, respectively. The 2DEG was confirmed by strong and well-resolved Shubnikov–de Haas oscillations starting at 3.0 T. Photoluminescence measurements and atomic force microscopy revealed that the densities of native donors and grain boundaries were effectively reduced in the AlGaN/GaN heterostructures incorporating low-temperature-grown AlN interlayers.

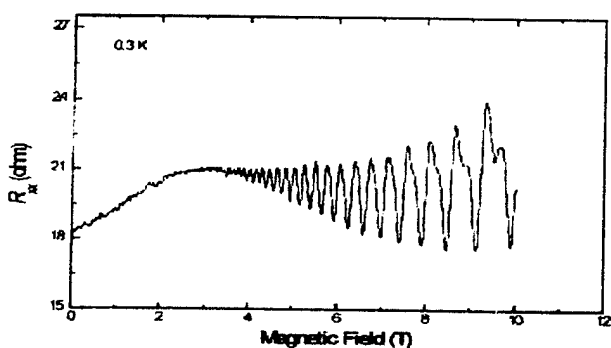
By inserting a low-temperature-grown AlN interlayer during the growth of a thick GaN buffer, the overall quality of the AlGaN/GaN heterostructures was significantly improved. The 2D electron mobilities for the structures were as high as 1500, 10 310, and 12 000 cm<sup>2</sup>/V s at room temperature, 77 K, and 0.3 K, respectively. The 2DEG was confirmed by strong and well-resolved Shubnikov–de Haas oscillations. Photoluminescence measurements and atomic force microscopy revealed that native point-defect densities and grain boundaries were effectively reduced in the AlGaN/GaN heterostructures incorporating AlN interlayers.

The effect of the LTG AlN layer thickness on the Hall mobilities of the AlGaN/GaN heterostructures was also investigated. The Hall mobility was measured to be as high as 10 310 cm<sup>2</sup>/V s at 77 K and 12 000 cm<sup>2</sup>/V s at 0.3 K, representing the best results for growth of AlGaN/GaN heterostructures directly on sapphire by a single growth process. The electron sheet densities for these samples were in the mid-10<sup>12</sup> cm<sup>-2</sup> range, which are in good agreement with the calculated values for Al<sub>0.2</sub>Ga<sub>0.8</sub>N/GaN heterostructures based on a model in which only the piezoelectric effect was considered.

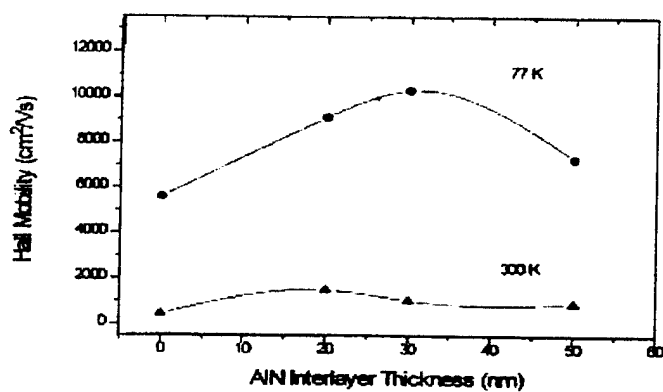
AlGaIn GaN sample ID	LTG AlN interlayer	$\mu$ (cm <sup>2</sup> /V s) 300 K	$\mu$ (cm <sup>2</sup> /V s) 77 K	$N_s$ (10 <sup>13</sup> cm <sup>-2</sup> ) 300 K	$N_s$ (10 <sup>13</sup> cm <sup>-2</sup> ) 77 K
3-551	No	610	6120	1.4	0.7
3-557	No	870	5700	1.5	1.0
3-594	Yes	1130	10 310	0.9	0.6
3-595	Yes	1500	12 000 <sup>a</sup>	0.6	0.6
3-596	Yes	901	7320	1.3	0.6

<sup>a</sup>Hall mobility measured at 0.3 K.

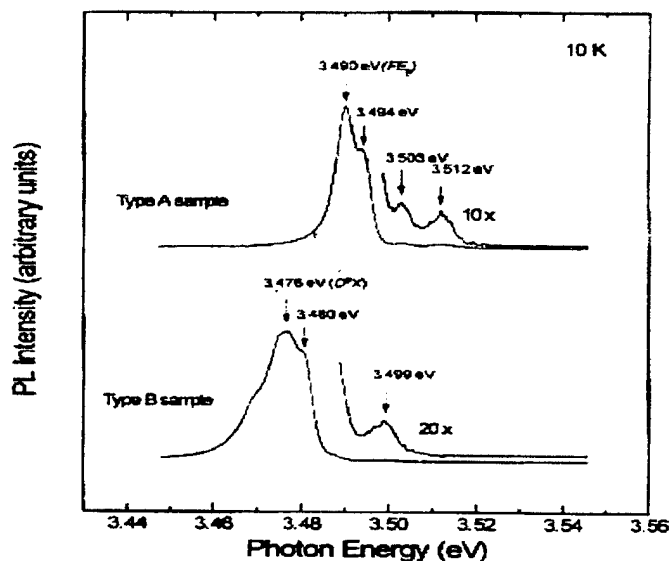
Electron mobilities and sheet densities measured at 300 and 77 K for a number of AlGaIn/GaN heterostructure samples.



Magnetoresistance  $R_{xx}$  at 0.3 K as a function of magnetic field for the AlGaIn/GaN heterostructure. The Shubnikov–de Haas (SdH) oscillations start at 2.8 T.



Room-temperature and 77 K electron mobilities for the AlGaIn/GaN heterostructures with AlN interlayers of different thickness.



Excitonic region of photoluminescence spectra for the type-A (with AlN interlayer) and the type-B (without AlN interlayer) AlGaIn/GaN heterostructures.

## Columbia University demonstrated

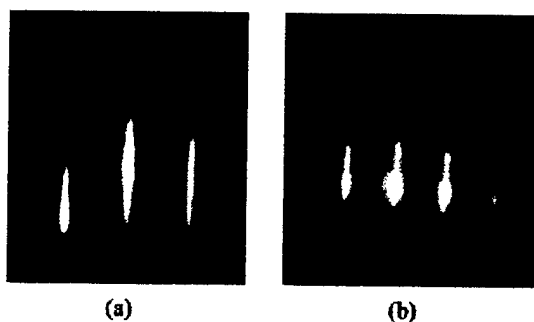
### the first use of Sb as a surfactant to improve the growth of GaN by molecular beam epitaxy

In this work, the effect of Sb on the molecular beam epitaxy (MBE) growth of GaN and its optical properties was investigated. One monolayer Sb predeposition before GaN growth and different Sb beam equivalent pressures applied throughout the GaN growth were used to study the effect of Sb on GaN growth by ammonia gas-source MBE. The presence of Sb remarkably enhanced two-dimensional growth as evidenced by *in situ* reflected high energy electron diffraction (RHEED). RHEED patterns became streaky much more rapidly when GaN was grown in the presence of Sb than that without Sb, indicating that Sb can act as an effective surfactant to smooth the growth front of GaN and enhance the layer-by-layer growth mode for the MBE growth of GaN. The full width at half maximum of the (0004) x-ray diffraction rocking curve measured from the GaN epilayer grown with one monolayer Sb predeposited as surfactant was as narrow as 70 arcsec. In the photoluminescence measurement, besides the characteristic near band edge excitonic emissions, new transitions related to Sb-isovalent traps were observed from GaN samples grown with Sb, whose zero phonon line was located at 3.27 eV with phonon replicas on the lower energy side. Intensities of the emissions related to Sb-isovalent traps increased with Sb partial pressures applied during GaN growth.

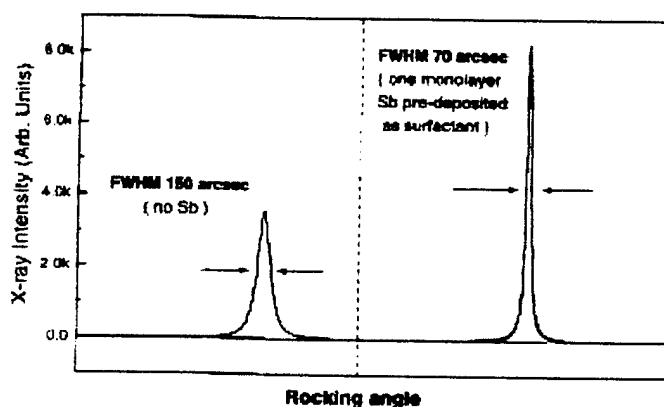
For the GaN epilayer grown with one monolayer Sb predeposited before GaN growth as surfactant, the full width at half maximum (FWHM) was 70 arcsec and was much narrower than that of GaN grown without Sb, indicating superior crystallinity. Our results

clearly suggest that Sb can act as an effective surfactant for GaN growth. Yellow band emission related to deep-level impurities and defects was absent. Excitonic emission (EE) at 3.47 eV and its weak phonon replica at 3.37 eV can be clearly identified. A significant increase of band edge emission intensity was exhibited.

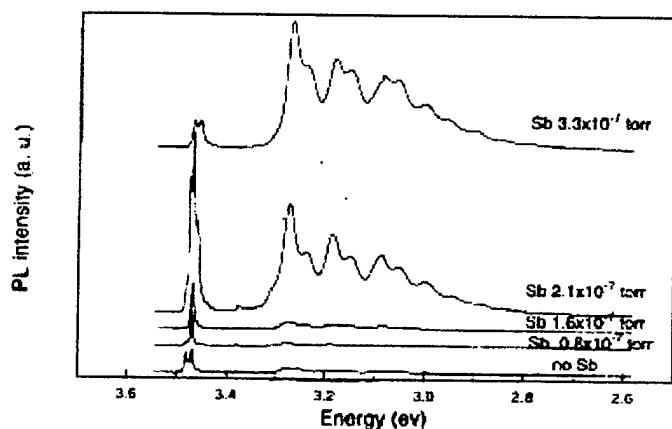
Growth of GaN on sapphire was dramatically improved with one monolayer Sb which was predeposited as surfactant. RHEED patterns became streaky much more rapidly when GaN was grown in the presence of Sb than that without Sb, indicating that Sb can act as an effective surfactant to smooth the growth front of GaN and enhance the layer-by-layer growth mode for MBE growth of GaN. The FWHM of the (0004) XRD rocking curve of the GaN epilayer grown with one monolayer Sb as surfactant was as narrow as 70 arcsec. The influence of Sb on the photoluminescence of GaN was investigated. Transitions related to Sb isovalent traps were observed and their intensities increased with Sb beam flux.



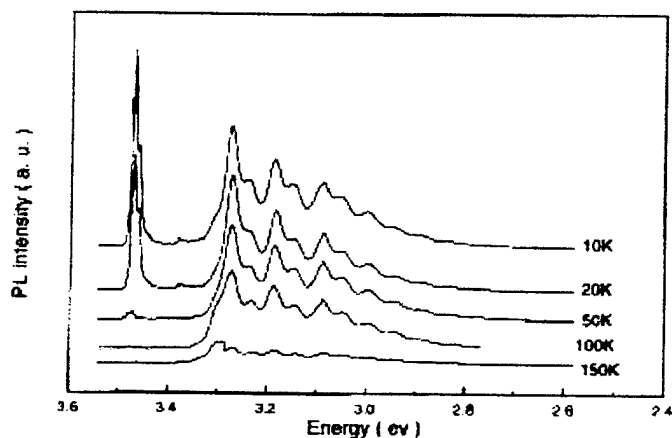
Comparison of GaN RHEED patterns: (a) 20 nm GaN overgrowth with Sb as surfactant and (b) 20 nm GaN overgrowth without Sb.



(0004) XRD rocking curves of GaN films grown with one monolayer predeposited Sb as surfactant and without Sb.



Photoluminescence spectra of GaN epilayers grown in the presence of different Sb beam fluxes by GSMBE.



Temperature-dependence photoluminescence spectra of GaN film grown with Sb.

- Z. Yang, J. Alperin, W. I. Wang, S. S. Iyer, T. S. Kuan, and F. Semendy. "In situ relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial layers with low threading dislocation densities grown on compliant Si-on-insulator substrates". *J. Vac. Sci. Technol. B* **16**, 1489 (1998)
- C. W. Pei, J. B. Héroux, J. Sweet, W. I. Wang, J. Chen, and M. F. Chang. "High quality GaAs grown on Si-on-insulator compliant substrates". *J. Vac. Sci. Technol. B* **20**, 1196 (2002)
- L. K. Li, B. Turk, W. I. Wang, S. Syed, D. Simonian, and H. L. Stormer. "High electron mobility AlGaIn/GaN heterostructures grown on sapphire substrates by molecular-beam epitaxy". *Appl. Phys. Lett.* **76**, 742 (2000)
- C. W. Pei, B. Turk, W. I. Wang, and T. S. Kuan. "Mechanism of the reduction of dislocation density in epilayers grown on compliant substrates". *J. Appl. Phys.* **90**, 5959 (2001)

- C. W. Pei, B. Turk, J. B. Héroux, and W. I. Wang. "GaN grown by molecular beam epitaxy with antimony as surfactant" J. Vac. Sci. Technol. B 19, 1426 (2001)
- M. L. Seaford, D. H. Tomich, K. G. Eyink, L. Grazulis, K. Mahalingam, Z. Yang and W. I. Wang. "Comparison of GaAs Grown on Standard Si (511) and Compliant SOI (511)" Journal of Electronic Materials, 29, 906 (2000)

## Cornell University

### Theoretical and Experimental Studies of Heteroepitaxy on Compliant Substrates

As a part of the MURI-compliant substrates, successful fabrication of p-n junctions by wafer bonding was demonstrated by Cornell University. These curves were not close to ideal. This can be attributed to amorphization of bonded interface and/or presence of oxide at surface, and also surface leakage, given the large surface area of samples. The role of dislocations in raising the barrier height across the bonded interface has been discussed. AlGaIn/GaN structures on the Lithium Gallate substrates were processed. Some problems were encountered in processing.

**Compliant Substrates:** The ever increasing use of various compound semiconductor materials for device fabrication has imposed great challenge on the semiconductor industry as there are very few substrates available. The composition of the materials grown on these substrates is often limited by the lattice-mismatch.

**Introduction:** One of the potential applications of the compliant substrates and the bonding interface is to form electrical junctions across the interface. Cornell University looked at the electrical behavior of the bonded interface, with and without the affect of twist and screw dislocations at the interface. When the wafers are bonded with a mismatch along the planar interface (twist bonding), twist dislocations are formed. An array of screw dislocations is formed on the interface which helps accommodate the strain in lattice mismatched interfaces. When an off-cut wafer is bonded to a normal wafer, a series of edge dislocations is formed on the interface. The density of dislocations in each case is given by:

#### Wafer bonding of off-cut wafers

Distance between dislocations

$$d = b \cos(\theta) / (1 - \cos(\theta))$$

Where,  $b$  = Burgers vector

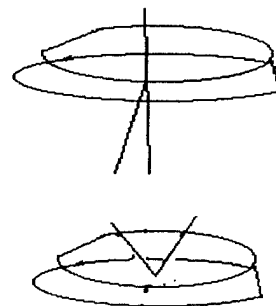
$\theta$  = angle of off-cut

#### Twist wafer bonding of wafers

Distance between dislocations

$$d = b / \sin(\theta)$$

Where,  $b$  = Burgers vector



$\theta$ =angle of twist bond

For the dislocations in diamond cubic lattice, 60-degree dislocation has a row of atoms with a dangling bond along the edge of the half-plane.

Both 30-degree and 90 degree partials form dislocations energy levels.

These partials charge up in edge dislocations and impede the current transport across the bonded interface.

**Bonding:** As a part of the MURI - compliant substrates, a bonding machine was fabricated at Cornell University. This wafer bonding system was fabricated to provide a controlled atmosphere and elevated temperatures required for wafer bonding. The bonding machine was designed to have a process chamber free of contaminants, hot zone capable of up to 1000 C, compatibility with clean room environments and upgradeability to larger wafer sizes.

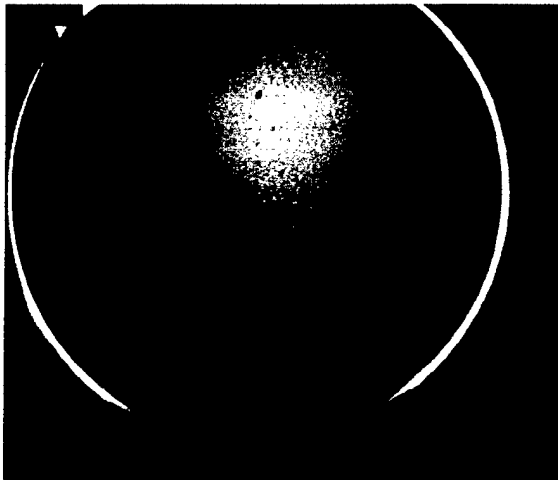
**Experiments:** Cornell University studied the bonding behavior of GaAs wafers. Our aim was to obtain a bonding interface good enough to fabricate p-n junctions from it. The semiconductors Cornell University tried to bond with the above mentioned apparatus were 2" GaAs wafers. The wafers were solvent cleaned in an ultrasonic bath. These cleaned wafers were loaded immediately into the UHV chamber in the MBE machine.

Several experiments were undertaken. These included bonding of p and n doped wafers, and, p and n doped wafers and n-n wafers where one of the wafers (n-type) is off-cut by 10 degrees.

Cornell University grew 1 $\mu$ m thick layer of 1e18 doped n-GaAs and then 5e17 doped n-GaAs on a 2" n-GaAs wafer by Molecular beam epitaxy. (Correspondingly 1e18 p-GaAs and then 5e17 p-GaAs on 2" p-GaAs wafer). These wafers were unloaded from the UHV chamber and immediately put together for Vanderwaals's bonding. This was done to avoid formation of oxide at the interface which is detrimental to any application related to current transport. These vanderwaal's bonded wafers were loaded into the Bonding Machine. The bonding chamber was purged with  $N_2$  gas for 15 minutes. The wafers were bonded in a  $H_2$  atmosphere. The pressure applied was 50psi and the temperature was 500C.

The bonded wafers were cut into 2mil X 2mil square pieces. The current measurements were done using HP4145 setup.

**Results:** Cornell University was able to successfully bond 2" GaAs wafers. When the wafers are bonded together defects may be introduced at the bonding interface by the oxides or the particulates. Cornell University was usually able to avoid these by immediately bonding the wafer after taking out from the UHV Molecular Epitaxy Chamber. The bonded wafers were observed through the long wavelength IR camera for defects and/or air-bubbles



**Bonded GaAs-GaAs wafers viewed through IR camera.**

The bonded interface was also observed by Transmission Electron Microscopy. No interface air-bubbles were observed.



**Transmission Electron micrograph of bonded interface**

**Electrical Results:** The bonded wafers were cut into 2 mil X 2 mil pieces by a diamond saw. The fact that these wafers survived sawing demonstrates the bonding strength. The ohmic contacts were made by:

n type: Ni/Au-Ge/Ag/Au

100/1000/1000/1500 Å

p type : Ti/Au

400/1000 Å

The I-V curves were measured by the HP4145 setup using needle probes. The current formula used to explain the results is:

$$I = I^* e^{\left(\frac{qV}{nKT}\right) - 1} e^{\left(-\frac{\phi_B}{KT}\right)} + \frac{V}{R_s}$$

Where  $I^*$  = saturation current

$$V = \text{applied voltage}$$

$$R_s = \text{surface resistance}$$

$$\phi_B = \text{barrier height}$$

$$n = \text{ideality factor}$$

Cornell University expected surface leakage to play an important role in determination of currents given the large area of the p-n junctions.

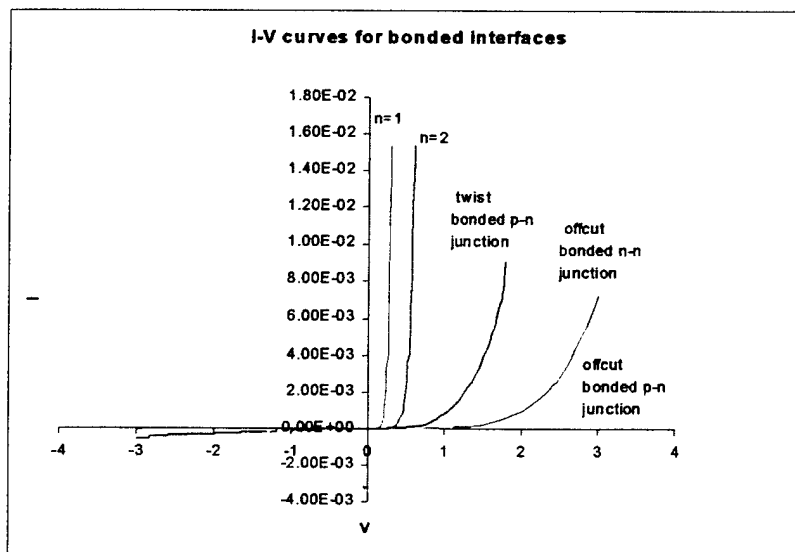
The results from the following three cases were analyzed:

Twist Wafer Bonding: p<sup>+</sup>-n<sup>+</sup> GaAs wafers

Off-cut wafer bonding: p<sup>+</sup>-n<sup>+</sup> GaAs wafers

Off-cut wafer bonding: n<sup>+</sup>-n<sup>+</sup> GaAs wafers

Cornell University observed that the off cut bonded wafers have significantly higher value of barrier thickness. The high value of ideality factor can also be explained by amorphousness of interface and/or oxides, making  $n > 1$ .



**I-V curves for twist and off-cut bonded interfaces**

**Conclusions:** Cornell University observed higher barrier in the off cut bonded wafers. The charging of dislocations raises the local barrier required by the electrons to go through the interface. Hence an enhanced barrier to current transport is observed, as shown in the figure representing the model.

### Lithium Gallate

Compliant universal substrates are the materials designed to accommodate high lattice mismatch and allow fabrication of devices from new materials. One of these

materials is Lithium Gallate (LiGaOx). Epi-layers with GaN/AlGaN heterostructure have been successfully grown on these substrates.

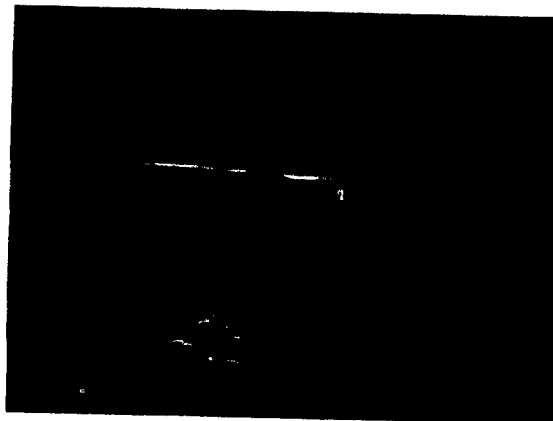
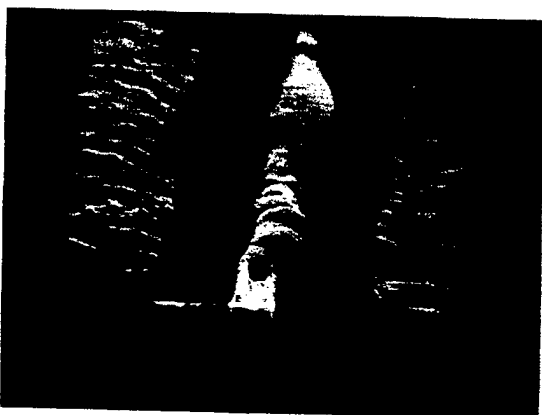
**Processing:** The GaN/AlGaN on Lithium Gallate samples were processed at the Cornell Nanofabrication Facility. The samples showed good uniformity in properties and yielded good ohmic contacts. The contact resistance and sheet resistance values were 0.65 ohms/mn and 400 ohms/sq. Following problems were observed during processing: Lithium Gallate substrate tends to stick to hot surfaces with temperature as low as 170 C. This made processing difficult and may contribute to failures by introducing micro-cracks.

**Results:** Two samples were processed. First sample displayed an unexplained failure along the gate when the gate and drain biases are applied. The following reason could be attributed to the failure:

**Something is wrong in the epi.**

The above reason can cause failure by creating a short on the surface. The second sample had a micro-crack in it at the beginning and failed during rapid thermal annealing for ohmic contacts by expansion of crack.

**Conclusions:** Lithium Gallate is an interesting substrate for accommodating high lattice mismatch associated with compound semiconductor growth. Further comments on the devices made on these substrates can be made on further processing (2 samples in process).



**Destruction of epi layer along the gate on application of bias.**

**Georgia Tech** pursued research as part of the MURI effort. The PI at Tech was Professor April S. Brown. Key accomplishments include:

- First use of bonded substrate removal for compliant substrate fabrication
- First use of metal-bonds for compliant substrates
- Exploitation of new concept- strain-modulated epitaxy
- First use of LGO substrate for GaN substrate removal
- GaN material improvements enabled by LGO substrate
- First demonstration of GaN devices bonded to Si enabled by bonded substrate removal

An account of the topics, publications and presentations related to the project are given below.

The Georgia Tech effort began with work on the use of metal bonds and substrate removal to enable compliant substrates. Publications and presentations on this work are:

Carter-Coman, C.A., Brown, A.S., Jokerst, N.M., Dawson, D.E., Bicknell-Tassius, R., Feng, Z.C., Rajkumar, K.C., and Dagnall, G., "Strain Accommodation in Mismatched Layers by Molecular Beam Epitaxy: Introduction of a New Compliant Substrate Technology," Journal of Electronic Materials, 25(7), pp. 1044-1047, October 1996.

Carter-Coman, C., Brown, A.S., and Jokerst, N. M., "Compliant Substrates for Reduction of Strain Relief in Mismatched Overlayers," MRS Conference Proceedings, vol. 441, pp. 361-366, Boston, MA, November 1996.

Carter-Coman, C.A., Brown, A.S., and Jokerst, N.M., "Analysis of InGaAs layers on GaAs compliant substrates by double crystal x-ray diffraction," Applied Physics Letters, 70 (13), pp. 1754-1756, June 1997.

Carter-Coman, C.A., Bicknell-Tassius, R. Benz, R., Brown, A.S., and Jokerst, N., "Analysis of GaAs Substrate Removal Etching with Citric Acid:  $H_2O_3$  and  $NH_4OH: H_2O_2$  for Application to GaAs Compliant Substrates," Journal of the Electrochemical Society, 144, 2, pp. L29-L31, 1997.

Carter-Coman, Carrie, Bicknell-Tassius, Robert, Brown, April S., and Jokerst, Nan Marie, "Metastability Modeling of Compliant Substrate Critical Thickness using Experimental Strain Relief Data," Applied Physics Letters, 71 (10), pp. 1344-1346, 8 September 1997.

Carter-Coman, C., Brown, A.S., and Jokerst, N.M., "Compliant Substrate Technology," WOCSEMMAD, San Antonio, TX, February 1997.

Strain-modulated epitaxy approach was developed, in which the bonded interface constrains a lithographically induced pattern to realize a strain-modulation at the growth surface and to exploit strain-dependent growth kinetics. Also explored was the spatial control of self-assembled quantum dots through this technique. Publications and presentations are:

Carter-Coman, Carrie, Brown, April S., Metzger, Robert A., Jokerst, Nan Marie, Pickering, Jason, and Bottomley, Lawrence, "A New Mechanism for Spontaneous Nanostructure Formation on Bottom-Patterned Compliant Substrates," Applied Physics Letters, 71 (19), pp. 2773-2775, 10 November 1997.

Carter-Coman, Carrie, Brown, April S., and Jokerst, Nan, "Compliant Substrates for SME," Electronic Materials Conference, Fort Collins, CO, June 1997.

Shen, J.J., Brown, April S., Metzger, Robert A., Sievers, Barry, Bottomley, Lawrence, Eckert, Patrick, and Carter, Brent, W., "Modification of Quantum Dot Properties Via Surface Exchange and Annealing: Substrate Temperature Effects," Journal of Vacuum Science and Technology B, 16(3), pp. 1326-1329, May/June 1998.

Brown, April S., Shen, J. J., and Jokerst, Nan, "Strain-Modulated Epitaxy for Self-Assembled Quantum Dots," Georgia Tech Nanostructures Meeting, December 1999.

Shen, Jeng-Jung, Brown, April S., Wang, Jack, and Wang, Z.L., Self-Assembled Quantum Dot Transformations via Anion Exchange, Journal of Vacuum Science and Technology B, 19, Issue 4, pp. 1463-1466, July 2001.

Shen, Jeng-Jung, Brown, April S., Wang, Yongquian, Wang, Z.L., "Modification of Self-Assembled Quantum Dots via Anion Exchange", 2000 Fall MRS Meeting, Boston, MA.

A new approach was developed for decoupling the strain and composition of epitaxial devices by creating bonded "quasi-substrates". A presentation describing this process is:

1. Jeng-Jung Shen, Tong-ho Kim, April Brown, Pete Moran and Thomas Kuech, "Growth and Characterization of GaInAs/AlInAs HEMT Structures on Oxide-Bonded GaInAs Substrates," International Symposium on Compound Semiconductors, San Diego, CA, 2000.

The most extensive and continuing effort has been on the growth of GaN on Lithium Gallate to exploit 1) improved properties of GaN on a nearly-lattice-matched oxide substrate, and 2) to remove the substrate and enable heterogeneous integration. Publications and presentations are:

Doolittle, W.A., Kropewnicki, T.J., Carter-Coman, Carrie, Stock, S., Kohl, P., Jokerst, N., Metzger, R.A., Kang, S., Lee, K., May, G., and Brown, A.S., "Growth of GaN on Lithium Gallate Substrates," Journal of Vacuum Science and Technology B, 16(3), pp. 1300-1304, May/June 1998.

Kropewnicki, T., Doolittle, W. Alan, Carter-Coman, Carrie, Kang, Sangbeom, Kohl, Paul, Jokerst, Nan, and Brown, April S., "Selective Wet Etching of Lithium Gallate", Journal of the Electrochemical Society, vol. 145, no.5, pp. L88-L90, May 1998.

Kang, S., Doolittle, W., Brown, A. S., and Stock, S., "Electrical and structural characterization of  $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  heterostructures grown on  $\text{LiGaO}_2$  substrates", Appl. Phys. Letters, Vol. 74, No22, 31 May 1999.

Doolittle, W. A., Kang, S., Kropewnicki, T.J., Stock, S., Kohl, P. and Brown, A.S., "MBE Growth of High Quality GaN on Lithium Gallate," Journal of Electronic Materials, vol. 27, no. 8, pp. L58-L61, August 1998.

Matyi, R. J., Doolittle, W.A., Brown, A. S., "High resolution X-ray diffraction analysis of  $\text{GaN}/\text{LiGaO}_2$ ", J. Phys. D: Appl. Phys., Vol 32 (1999), A61-A64.

Doolittle, W. A., Kang, S. and Brown, A. S., "MBE growth of high quality GaN on  $\text{LiGaO}_2$  for high frequency, high power electronic applications", Solid State Electronics, Volume 44, Issue 2, 1 February 2000, pp. 229-238.

Brown, April S., Doolittle, W. Alan, Kang, Sangbeom, Shen, Jeng-Jung, Wang, Z. L., and Dai, Z. "The Growth of GaN on Lithium Gallate ( $\text{LiGaO}_2$ ) Substrates for Material Integration" Journal of Electronic Materials, Volume 29, Issue 7, Pages 894-896, July 2000.

Kang, Sangbeom, Doolittle, W. Alan, Lee, K. K., Brown, April S., Dai, Z. R., Wang, Z. L., and Stock, Stuart R. Characterization of  $\text{AlGaIn}/\text{GaN}$  Structures on Various Substrates Grown by Radio-Frequency Plasma Assisted Molecular Beam Epitaxy, Journal of Electronic Materials: Special Issue on Wide Bandgap Semiconductors. (December 2000)

Doolittle, W.A., Brown, A.S., Kang, S., Seo, S.W., Huang, S., and Jokerst, N. M. "Recent Advances in III-V Nitride Devices grown on Lithium Gallate," accepted for publication in *physica status solidi B*.

Seo, S. W., Lee, K. K., Kang, S. B., Huang, S., Doolittle, W. A., Jokerst, N. M., Brown, A. S., and Brooke, M. A., "The Heterogeneous Integration of GaN Thin Film MSM Photodetectors Onto Silicon," accepted for publication in *Photonics Technology Letters*.

Brown, April, "Molecular Beam Epitaxial GaN", *Frontiers in Science Meeting*, La Jolla, CA, April 4, 2000.

Brown, April and Doolittle, Alan, "GaN Growth on Sapphire and Lithium Gallate", *Seventeenth Conference on Crystal Growth, (AACG/WEST)*, Fallen Leaf Lake, CA, June 4-7, 2000.

S. Kang, W. A. Doolittle, A. S. Brown and S. R. Stock, "Comparison of AlGa<sub>N</sub> and Ga<sub>N</sub> grown on various substrates; step flow growth on LiGaO<sub>2</sub> at low growth temperature", *Proceedings of the International Conference on Silicon Carbide and Related Materials*, October 10-15, Raleigh NC.

Doolittle, Alan, Kang, Sangbeom, Kropewnicki, T., Kohl, P., and Brown, A.S., "Growth of Ga<sub>N</sub>, AlGa<sub>N</sub>, and InGa<sub>N</sub> on Lithium Gallate by MBE," *Electronic Materials Conference*, Charlottesville, VA, June 1998.

Doolittle, William, A. and Brown, April S., "High Quality Gallium Nitride on Lithium Gallate for High Frequency Power Devices", *TMS Workshop on Minority Carrier Wide Bandgap Devices*, Panama City, FL Feb. 1999.

Doolittle, William, A. and Brown, April S., "Comparison of AlGa<sub>N</sub> and Ga<sub>N</sub> Grown on Various Substrates: Benefits and Limitations of Growth on LGO at Low Substrate Temperature," *First Ga<sub>N</sub> Electronic Device Workshop*, Cornell University, August 1999.

Huang, Sa, Kang, Sangbeom, Doolittle, Alan, Seo, Sang-Woo, Lee, Kyeong, Jokerst, Nan, and Brown, April, "GaN MSM Photodetectors on Lithium Gallate: Demonstration of Performance and Integration Onto Si," *Electronic Materials Conference*, University of Notre Dame, June 2001.

Kang, Sangbeom, Doolittle, Alan, Dai, Z., Wang, Z.L., Stock, Stuart, and Brown, April, "Advancement in the Electrical Properties of AlGa<sub>N</sub>/Ga<sub>N</sub> Heterostructures Grown by Molecular Beam Epitaxy on Lithium Gallate," *Electronic Materials Conference*, University of Notre Dame, June 2001.

S.W. Seo, K.K. Lee, Sangbeom Kang, S. Huang, W. Alan Doolittle, N.M. Jokerst, and A.S. Brown, "Ga<sub>N</sub> metal-semiconductor-metal photodetectors grown on lithium gallate substrates by molecular-beam epitaxy", *Appl. Phys. Lett.* 79, 9, Aug. 27, 2001, 1372-1374.

Overview papers on compliant substrates and integration are:

Brown, A.S., "Compliant Substrates Technology: Status and Prospects," *Journal of Vacuum Science and Technology*, 16 (4), pp. 2308-2312, July 1998.

Brown, A. S. and Doolittle, W. A., "GaN Compliant Substrate Processes", *Journal of Electronic Materials*, 29 (7) pp. 894-896, July 2000.

Brown, April S. and Doolittle, W. Alan, "The status and promise of compliant substrate technology", *Applied Surface Science*, Volume 166, Issues 1-4, Pages 392-398, 9 October 2000.

- (Invited Presentation) Brown, A.S., "Compliant Substrate Technology," Physics of Semiconductor Interfaces, Salt Lake City, January 1998.
- Brown, A.S., "Compliant Substrate Technology," Workshop on Bonded Semiconductors, Puerto Rico, February 1998.
- Doolittle, William and Brown, April, "Compliant Substrate Processes", Proceedings of Materials Research Society, San Francisco, CA, April 5-9, 1999.
- (Invited Presentation) Brown, April and Doolittle, W. Alan," Status and Promise of Compliant Substrate Technology," International Conference of Semiconductor Interface Science and Technology", Gothenberg, Sweden, June 1999.
- Brown, April and Doolittle, W. Alan, "Compliant Substrates," International Conference on Compliant and Bonded Substrates, Orlando, FLA, September, 1999.
- Brown, April, Doolittle, W. Alan, Jokerst, Nan Marie, and Kuech, Thomas, "Heterogeneous Integration", *IEDM*, December 2001.
- Brown, April, Jokerst, Nan Marie, Doolittle, W. A., "GaN on Lithium Gallate: Enabling Heterogenous Integration," Workshop on Frontiers in Electronics, St. Croix, Virgin Islands, January 2002
- Brown, A.S., "Status of Compliant Substrates," Advanced Heterostructures Workshop 98, Hawaii, Dec. 1998.
- Shen, J. J. and Brown, April S., "Compliant Substrate Processes", WOCSEMMAD, New Orleans, February, 1999.
- A. S. Brown, W.A. Doolittle, N.M. Jokerst, S. Kang, S. Huang, and S.W. Seo, "Heterogeneous Materials Integration: compliant substrates to active device and materials packaging," *Materials Science and Engineering B87* (2001) 317-322.

**New discoveries, inventions, or patent disclosures: None**