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Semiconductor memory is one of' the key elements in modem computing systems. Today, floating-gate ("flash) memory, which exhibits very long writing and erasing time, is widely used in many appiicati.ons. One way to achieve dramatic speed-np of floating-gate memories by quantum-mechanical tunneling is through implementation of specially shaped ("crested") tunnel barriers. In contrast to the conventional unifonn Fowler-Nordheim barriers used. in existing floating gate memories, the maximum height of the crested barrier may be strongly suppressed with even moderate changes of applied electric field. The most important step in the development of the crested barrier idea is to find suitable combinations of semiconductor materials, which would provide barriers with tunneling transparency changing by 18 orders of magnitude under a change of applied voltage by a factor of 2 to 3, in moderate electric fields.

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"AlInGaN-based Crested Quantum Tunneling Barriers for Advanced Data Storage Systems "

STTR Phase I Program

Sensor Electronic Technology, Inc.
21 Cavalier Way
Latham, NY 12110

Contract Number: **F49620-01-C-0049**

Final Report

Period of Performance: 09/28/01 -- 04/28/02

Program description

Semiconductor memory is one of the key elements in modern computing systems. Today, floating-gate ("flash") memory, which exhibits very long writing and erasing time, is widely used in many applications. One way to achieve dramatic speed-up of floating-gate memories by quantum-mechanical tunneling is through implementation of specially shaped **("crested")** tunnel barriers. In contrast to the conventional uniform Fowler-Nordheim barriers used in existing floating gate memories, the maximum height of the crested barrier may be strongly suppressed with even moderate changes of applied electric field. The most important step in the development of the crested barrier idea is to find suitable combinations of semiconductor materials, which would provide barriers with tunneling transparency changing by 18 orders of magnitude under a change of applied voltage by a factor of 2 to 3, in moderate electric fields.

The implementation of crested barriers is relatively straightforward using composite semiconductors such as GaAs/AlGaAs, where the barrier shaping may be achieved with either a gradual change of the layer composition during its epitaxial growth or by modulation doping. However, the maximum barrier height (conduction band offset) available in these materials is too small to provide sufficient retention time at room temperature. One of the best possible material systems for crested barrier implementation is AlInGaN alloys. The bandgap and conduction band offset of AlN are largest, and sufficient for using this material for the top ("crest") of the barrier, while n^+-doped GaN may be used for the system electrodes. Moreover, $Al_xGa_{1-x}N$ alloys are thermodynamically stable for any x.

We proposed to develop technology for advanced digital memory and data storage systems utilizing wide-band-gap quaternary AlInGaN-based crested multi-layer tunnel barrier concept. Our technical approach is based on a new way to reach a dramatic speed-up of floating gate memories by using quantum-mechanical tunneling through specially shaped ("crested") tunnel barriers. In contrast to the usual, uniform Fowler-Nordheim barriers used in existing floating gate memories, the maximum height of the crested barrier may be strongly suppressed with even moderate changes of applied electric field. The implementation of the crested barrier design is expected to yield barriers with tunneling transparency changing by 18 orders of magnitude under a change of applied voltage by a factor of 2 to 3. The read/write time is expected to reduce below 10 ns.

Fig. 1 compares the conduction band diagrams of three structures. The standard uniform SiO_2 barriers, (See Fig. 1a) which is currently widely used in the technology, cannot combine the low transparency necessary for long retention time at low electric fields with the high transparency necessary for fast read/erase at acceptably high fields (say, 10 MV/cm). Higher fields decrease the memory cell endurance (the maximum number of read/erase cycles) and may even lead to electric breakdown of the barrier. The situation changes immediately if we consider a barrier with a "crested" potential profile peaking in the middle, for example the triangular barrier shown in Fig. 1b.[1],[2] A positive effect of "graded" tunnel barriers on the speed of field-induced electron injection was noticed long ago.[3],[4] However, the asymmetrical barriers studied in those works could not provide short erase time and hence the bit-addressable memory operation as a whole. Of course, this opportunity may be restored by connecting two barriers with opposite barrier slopes in parallel, but this option may be too complex for practical applications. In reality, the trilayer barrier structure shown in Fig. 2c was proposed, which may reasonably well approximate the triangular barrier.

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[1] K. K. Likharev, "Layered tunnel barriers for nonvolatile memory devices", *Appl. Phys. Lett.*, vol. 73, pp. 2137-2139, Oct. 1998

[2] A. N. Korotkov and K. K. Likharev, "Resonant Fowler-Nordheim tunneling and its possible applications", in: *1999 IEDM Tech. Digest* (IEEE Press, Piscataway, NY, 1999), pp. 223-226.

[3] D. J. DiMaria, "Graded or stepped energy band-gap-insulator MIS structures (GI-MIS or SI-MIS)", *J. Appl. Phys.*, vol. 50, pp. 5826-5829, Sep. 1979

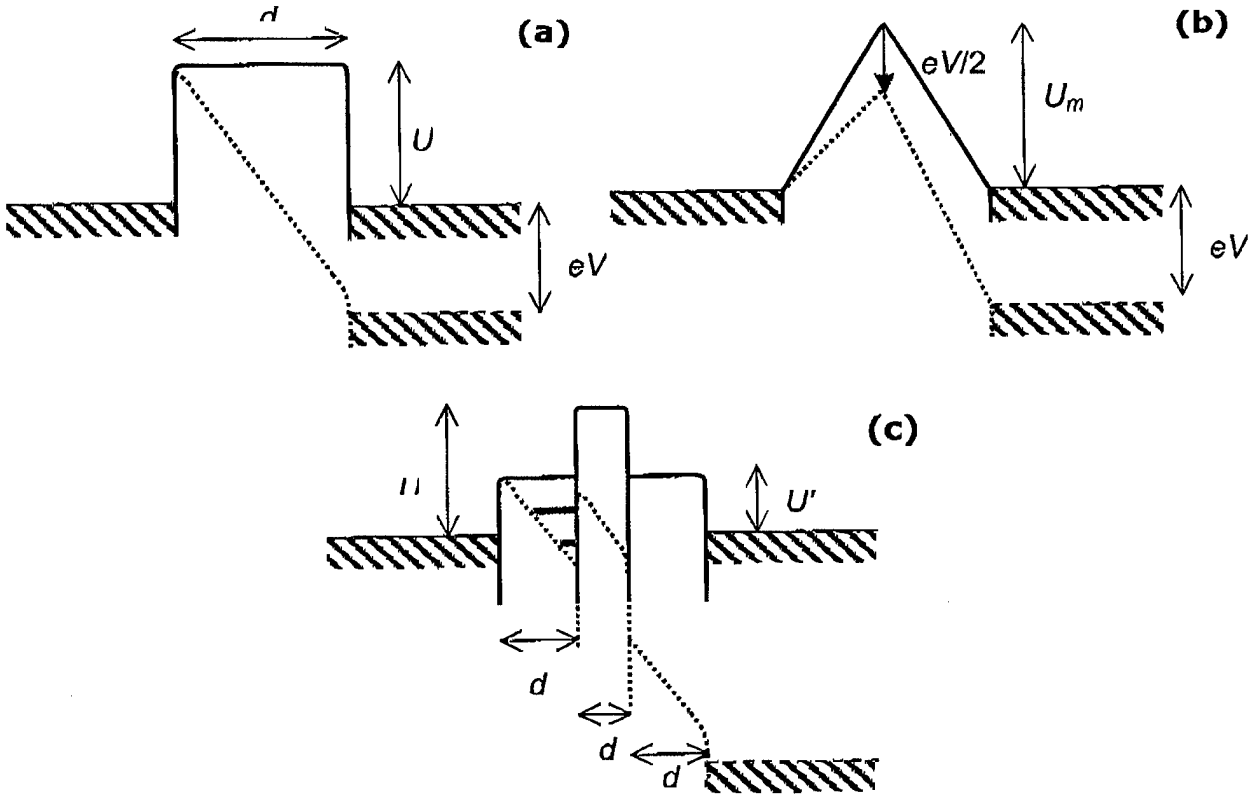

Fig. 1. Conduction band edge profiles of various tunnel barriers (solid lines) and their deformation at high applied voltage (dashed lines): (a) usual, uniform tunnel barrier; (b) ideal crested barrier; (c) realistic trilayer crested barrier. In the lower panel (c), thick horizontal lines show the position of electron subbands formed in the triangular quantum at the interface between the first and the second layer (schematically).

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[4] F. Capasso, F. Beltram, R. J. Malik, and J. F. Walker, "New floating-gate AlGaAs/GaAs memory devices with graded-gap electron injector and long retention times", *IEEE Electron Device Lett.*, vol. 9, pp. 377-379, Aug. 1988

Accomplishments:

1. Modeling

Firstly, we tried to calculate the on-off current for different biases in the high aluminum content AlInGaN-based crested barriers.

1. Calculation results for crested GaN-$Al_{0.5}Ga_{0.5}N$-AlN- $Al_{0.5}Ga_{0.5}N$-M barriers:

Assumed parameters:

- effective masses: $m_{GaN} = 0.20\ m_0$, $m_{Al0.5Ga0.5N} = 0.34\ m_0$, $m_{AlN} = 0.48\ m_0$

- conduction band edge shifts: $\Delta U_{GaN\text{-}Al0.5Ga0.5N} = 1.05$ eV,
$\Delta U_{Al0.5Ga0.5N\text{-}AlN} = 1.05$ eV

- middle layer thickness: $d_{AlN} = 5$ nm (not a very critical parameter)

Legend:

V – total applied voltage (in Volts),

j – current densities (in Amperes per m^2):

jF – resonant tunneling assuming full subband,

jDF – direct tunneling assuming full subband,

jE - resonant tunneling assuming empty subband,

jEF - direct tunneling assuming empty subband,

j – the resulting current.

τ - floating gate recharging time scale (in seconds).

Results:

(a) $d_{Al0.5Ga0.5N} = 3.5$ nm

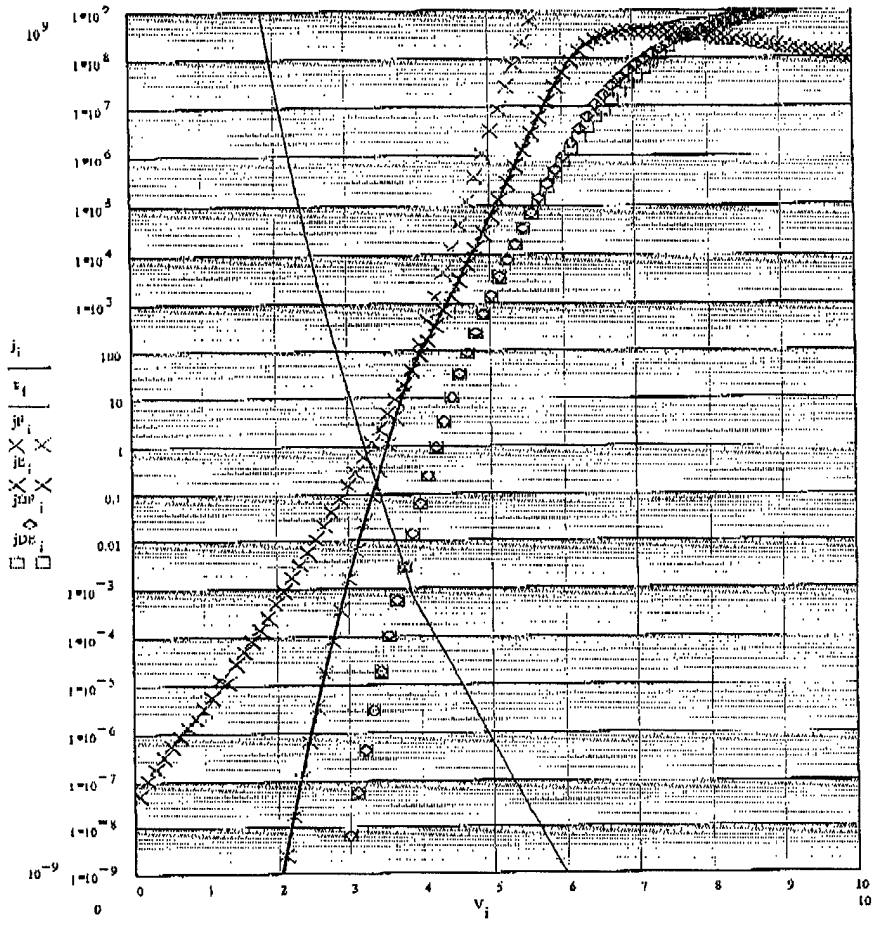


Fig. 2 Bias dependence of the tunneling current in AlGaN/GaN/AlGaN structure, AlGaN thickness 3.5nm

$d_{Al0.5Ga0.5N} = 4.0$ nm

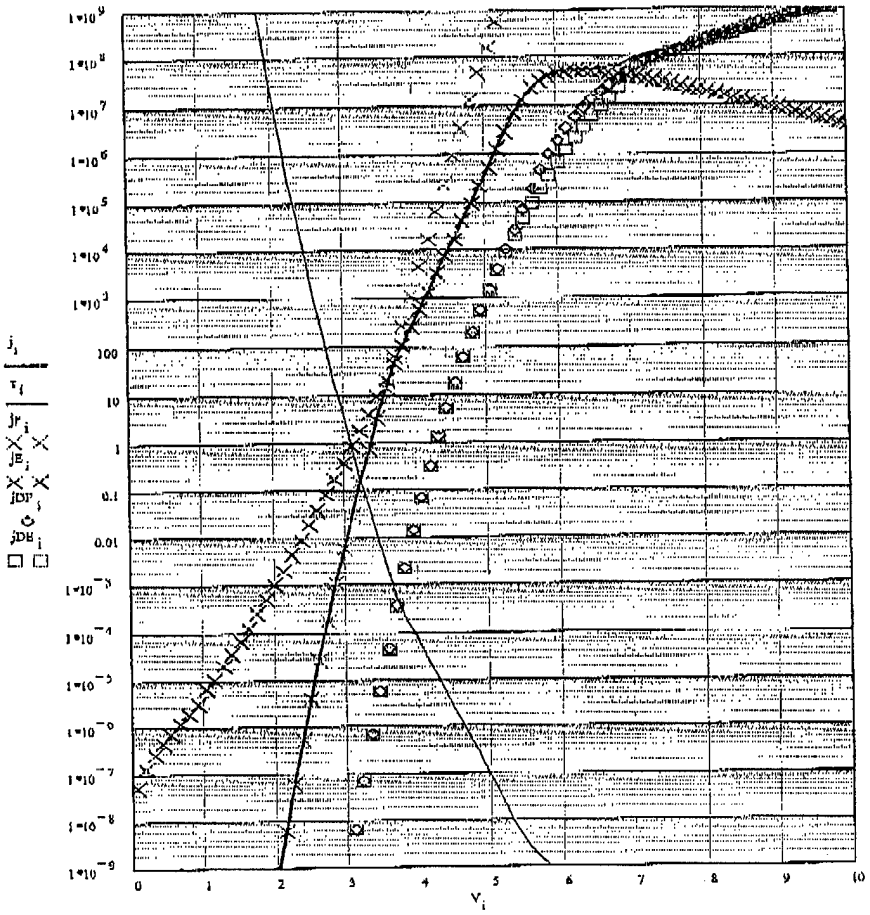


Fig. 3 Bias dependence of the tunneling current in AlGaN/GaN/AlGaN structure, AlGaN thickness 3.5nm

$d_{Al0.5Ga0.5N} = 4.5$ nm

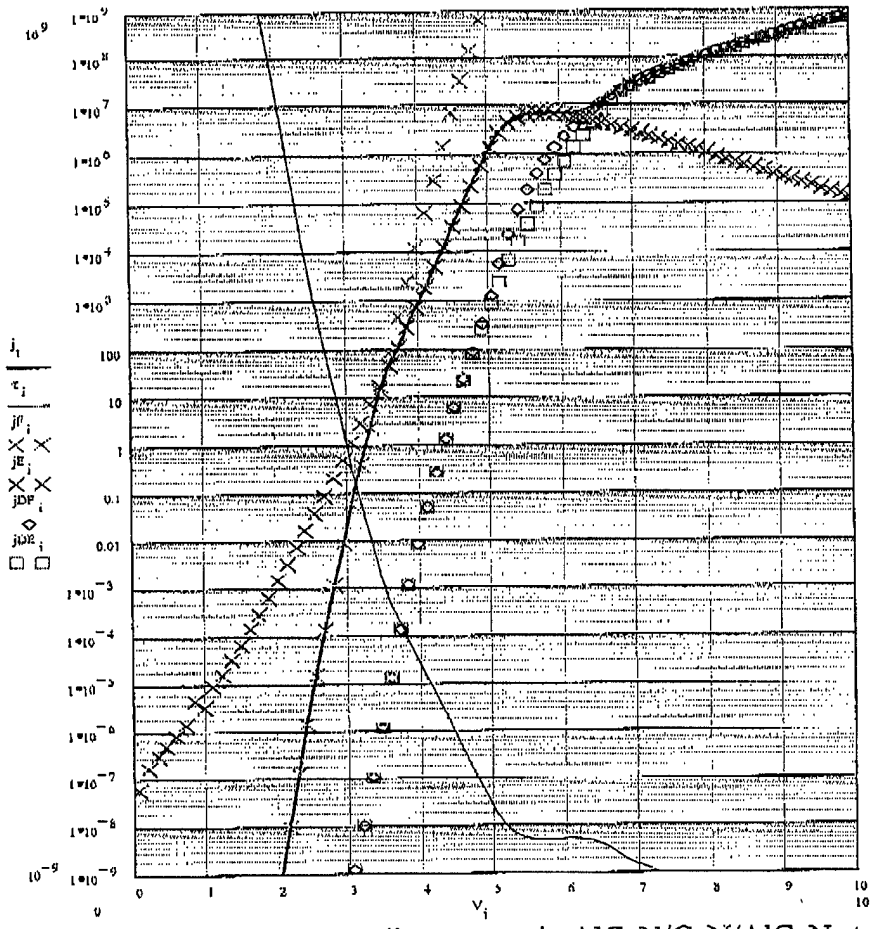


Fig. 4 Bias dependence of the tunneling current in AlGaN/GaN/AlGaN structure, AlGaN thickness 4.5nm

Discussion:

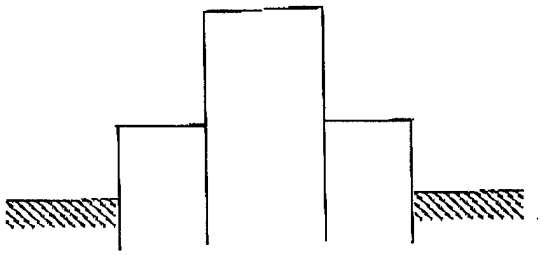
Accepting as a performance criterion the ratio $r = V_W/V_R$, where is the "minimum write voltage" corresponding to $\tau = 1$ ns, while is the "maximum retention voltage" corresponding to $\tau = 10$ years $\approx 3\times10^8$ s, we see that the minimum $r \approx 3.0$ is achieved at $d \approx 4.0$ nm; however, deviations from this goal thickness by ~ 0.5 nm are not too crucial.

Notes:

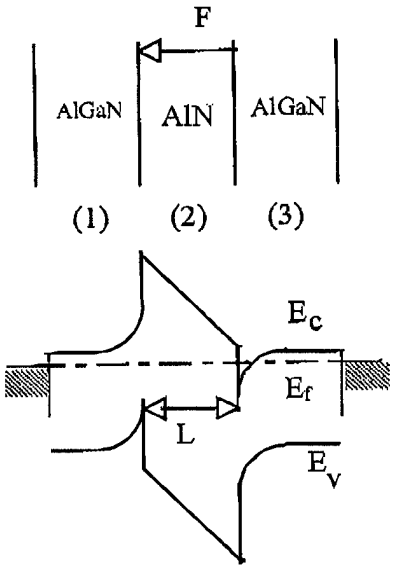
1) For different criteria the optimum thickness may be somewhat different. For example, we can argue that if retention time is of the order of a few seconds, memory refresh is not a big burden. From this point of view, some reduction of d (to about 3 nm) may be beneficial.

2) A different concentration of Al ($x \neq 0.5$) in outer layers may lead to a somewhat different d_{opt} , and a better r_{min}. If you let me know the practical range of x, I will try to carry out a more thorough optimization.

3) For All these calculations, we assume the ideal three-layer system is used. (see Fig. 5a.) However, in real AlInGaN systems, because the large mechanical strain formed between the AlN/AlGaN interface and the large piezoelectric charge, the band diagram is usually different from the ideal case, as shown in Fig. 5b and Fig. 5c. These effects can strongly influence the performance of these barriers. (See Section 3) Thus, they have to be seriously considered in further modeling efforts.



(a)



(b)

Fig. 5 Crested barrier band structure (a) ideal (only conduction band is shown) (b) AlGaN/AlN/AlGaN (50%), AlGaN doped

2. Calculation results for the control, uniform GaN-AlN-M barrier

d_{AlN} = 10 nm

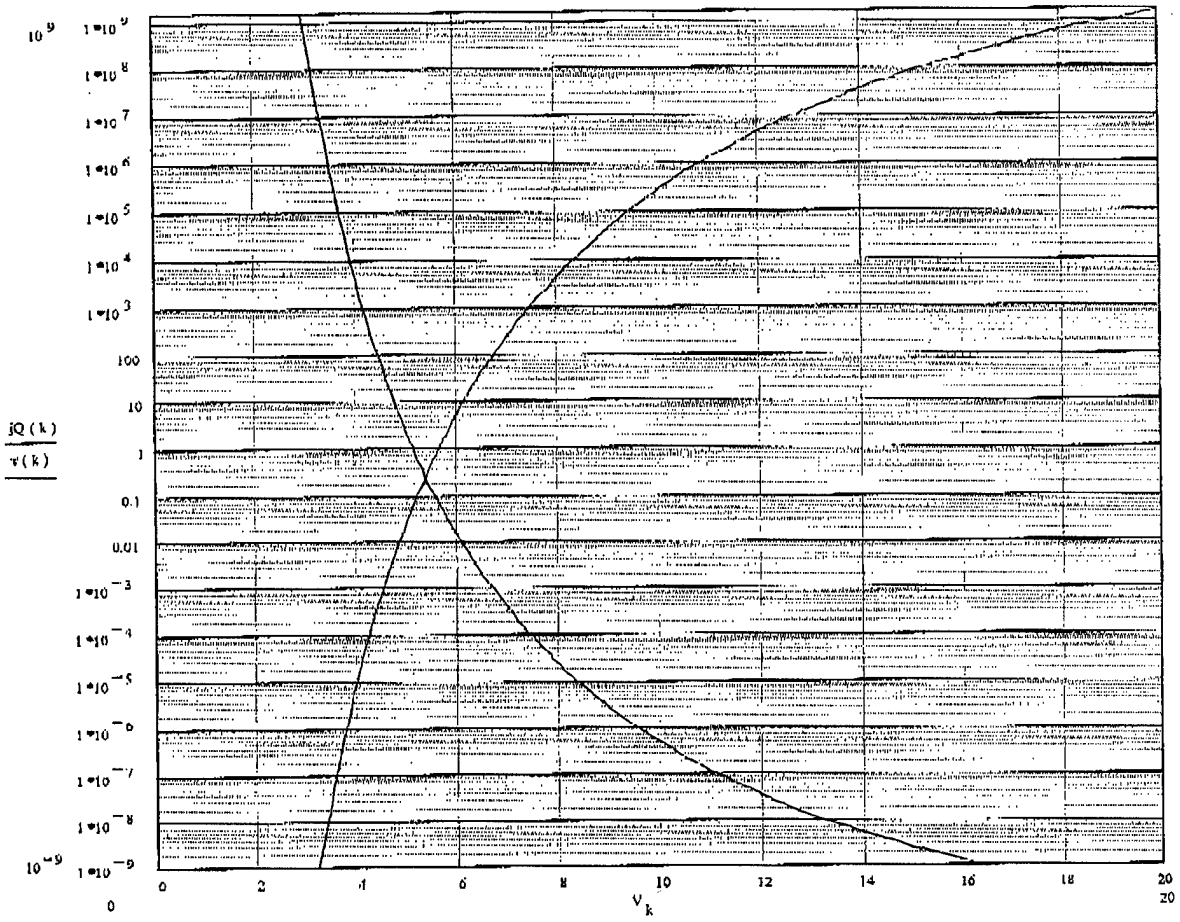


Fig. 6 Calculation results for the control, uniform GaN-AlN-M barrier, with AlN thickness of 10nm

Discussion:

We see that in a uniform barrier the ratio $r = V_W/V_R$ is very large (> 5). Even more importantly, the write time 1 ns is reached at unrealistically high electric field $E = V/d \approx 16$ MV/cm, apparently beyond the breakdown threshold. (For the crested barriers, the write field is also large, about 4 MV/cm, but may be acceptable; at least for high-quality Al_2O_3, SiO_2, and Si_3N_4, breakdown is above 10 MV/cm.)

2. Material growth and characterization

We designed and deposited the first high aluminum content AlInGaN-based barrier structures. We tested the performance of these barriers. The preliminary device characterization results is presented and analyzed in this report.

1. Device Structures

The epilayer structure was grown using low-pressure MOCVD technique. The deposition of nominally undoped highly resistant GaN was followed by the growth of AlGaN barrier layer. Insulating SiO_2 layer was deposited by Plasma Enhanced Chemical Vapor Deposition method at elevated temperatures. The structures are shown as in Fig. 7. We used two kind of materials as the barrier material, AlN and $Al_{0.2}Ga_{0.8}N$, as is clear from the figure. We will compare these two structures in the following sections.

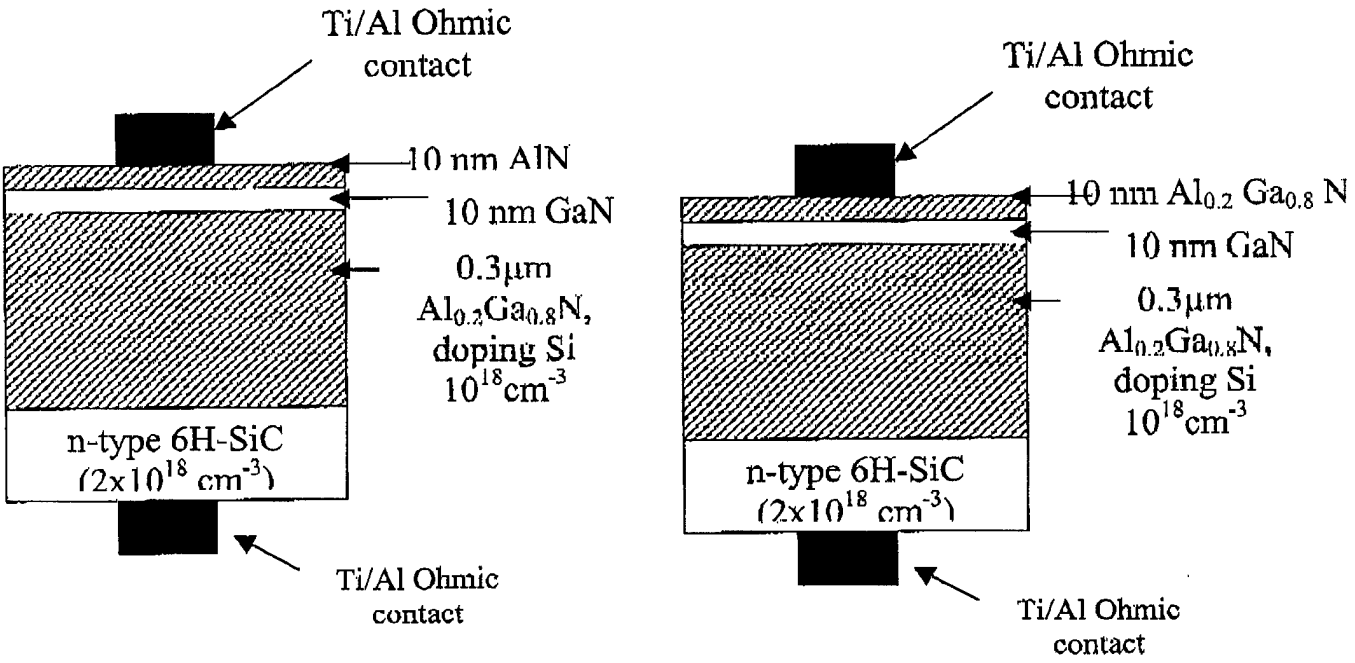


Fig. 7. Epilayer designs for the first quantum-well barrier structure
(a) AlN as barrier layer (A1826) (b) $Al_{0.2}Ga_{0.8}N$ as barrier layer (B1104)

2. Test Results

The current-voltage characteristics of both layers are shown in Fig. 8. The estimated vertical resistance of A1826 is between 40~60Ω (depending on forward or backward bias) and the 13.6Ω for B1104. To compare with the simulation results of the previous report, we also plotted the forward current in semi-log scale. (Fig. 9)

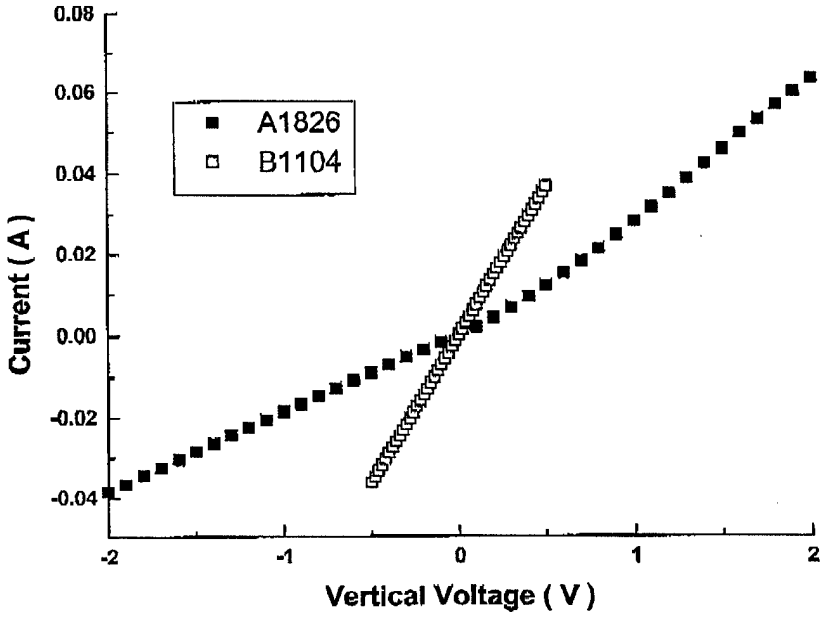


Fig. 8 Current-Voltage characteristics of the two barrier structures

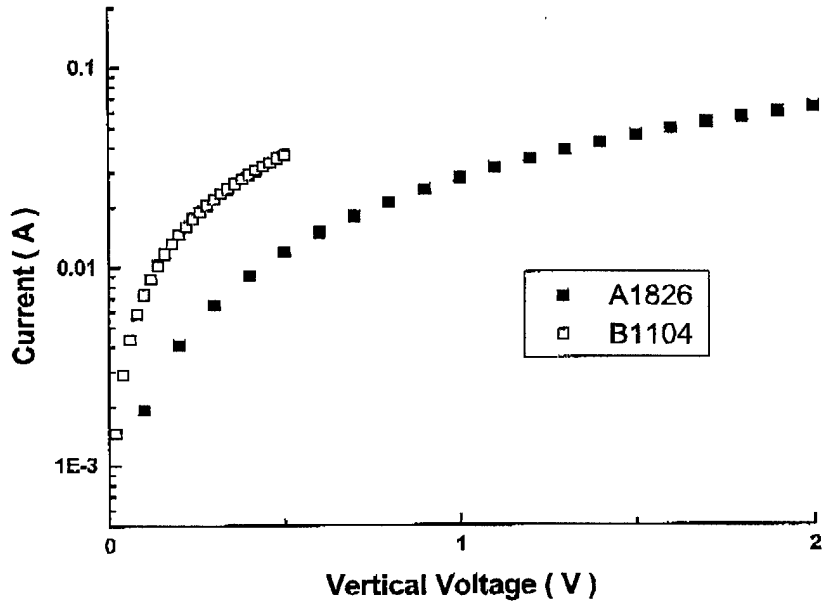


Fig. 9 Forward characteristics of the two structures in semilog scale

In order to analyze the top barrier layers, we also deposited transmission line structures (TLM) to test the contact resistance. The test results on B1104 is shown in Fig.

10. The contact resistance is estimated to be $1.51x10^{-6}\Omega.cm^2$. The results indicate that the top barrier layer is conducting for some reason.

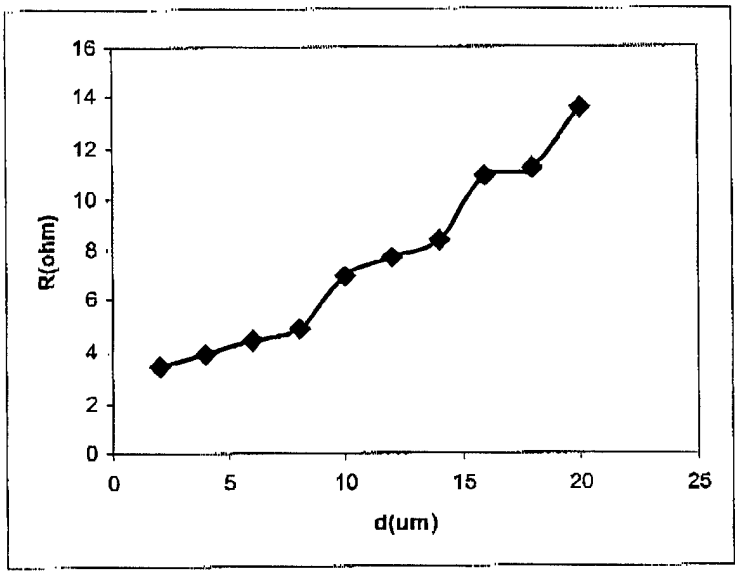


Fig. 10 TLM test results (W=200μm)

Fig. 11 and Fig. 12 show the drain and gate characteristics for the field effect transistors patterned on A1826.

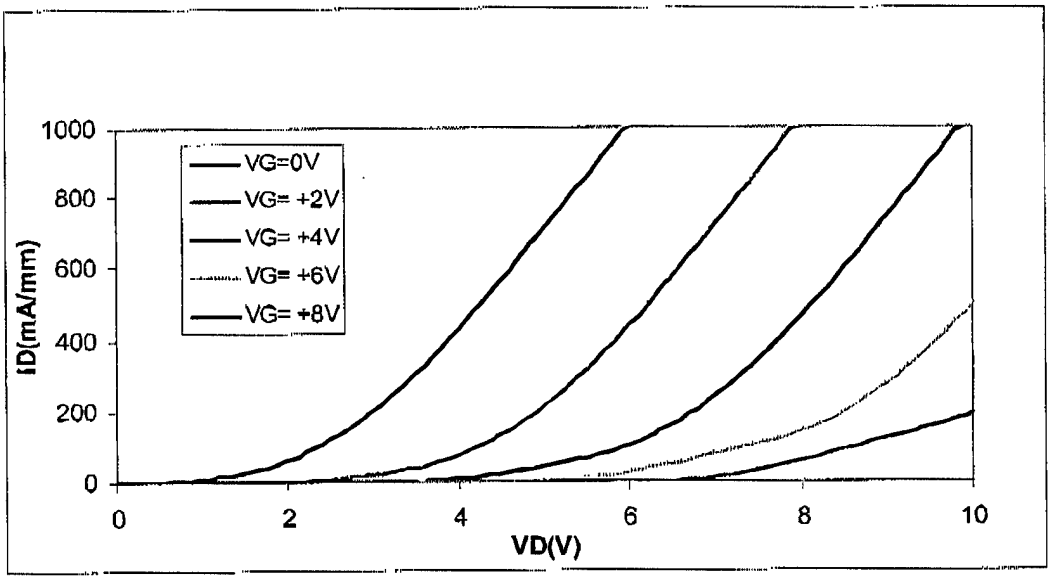


Fig. 11. Id-Vds characteristics of the FET structure on A1826 (W/L=100μm/5μm)

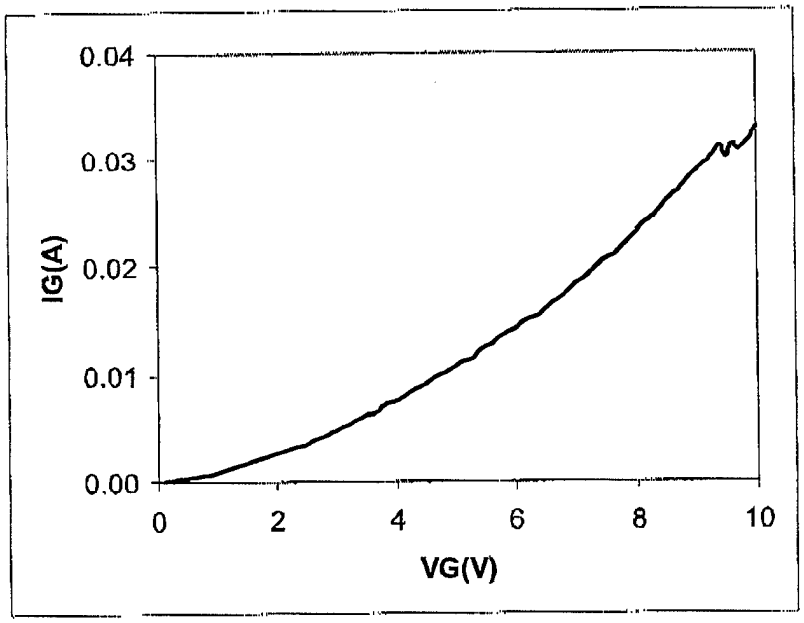


Fig. 12. Gate characteristics of the FET structure on A1826 (W/L=100μm/5μm)

In order to test the maximum voltage swing, we did some transient measurement. The results are shown in Fig. 13. The maximum current is around 900mA at 6V and the rise/fall times are estimated to be about 1.6μs/2μs, respectively.

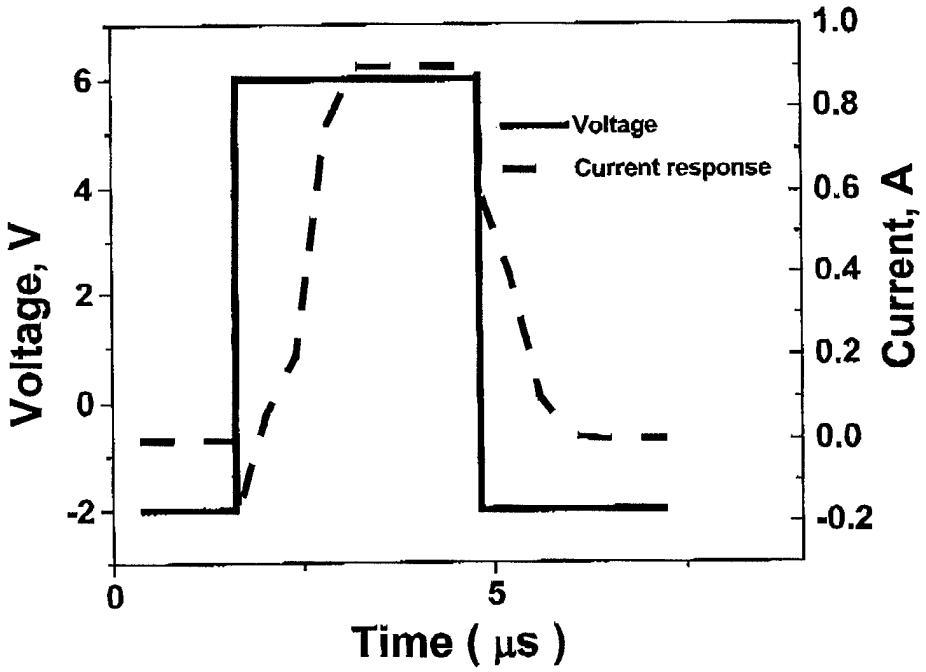


Fig. 13 Transient response of the barrier structure

3. Analysis

Apparently, the current deposited structures did not accomplish the predicted V_W/V_R ratio we obtained from the theoretical calculation. We studied the cause of the non-ideality in our grown epilayer structure. Two causes were found for the high vertical conduction: the aging of the unpassivated epilayers and the presence of excessive strain which leads to large piezoelectric charge in the SIS structure.

1. Aging effects.

Fig. 14 shows the influence of the aging effect on the PL characteristics of bulk single crystalline AlN. Both M-plane and C-plane sample were tested. M-plane AlN shows a much more stable PL while the C-plane surface shows a dramatic reduction on the main line intensity after one month. At the same time we observed increase in the deep level emission in the range from 3.5 eV to 4.7 eV. Thus, these preliminary data demonstrated that m-face samples exhibit the most stable optical properties. In contrast, c-face crystal "aging" was noticeable on a weekly basis.

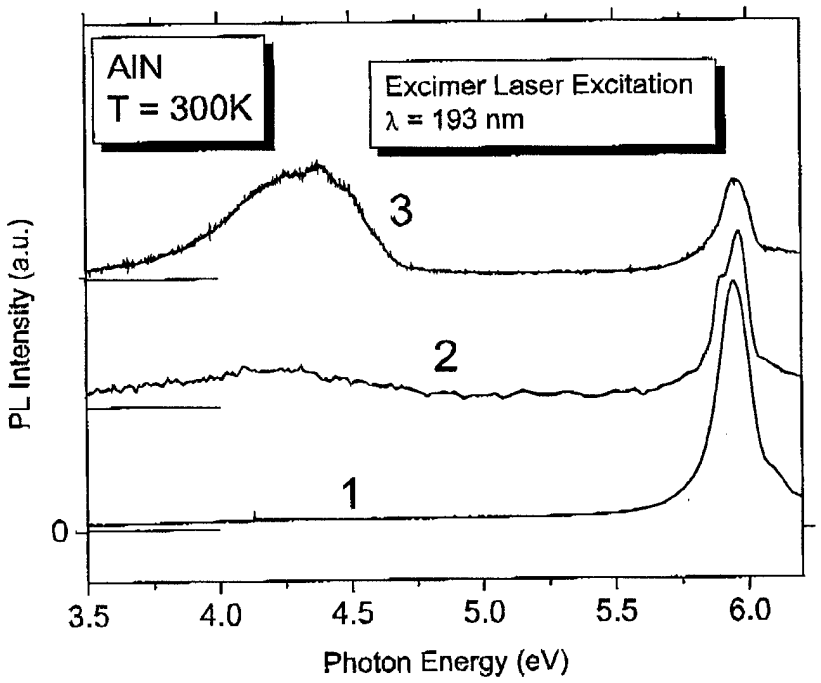


Fig. 14. PL properties of different bulk AlN. Curves 2 and 3 correspond to C-plane surface of bulk single crystalline AlN PL measured on 04/05/02 and 05/22/02 respectively. Curve 1 corresponds to freshly cleaved surface of the same sample (M-plane).

We speculate that changes in optical properties of AlN films are primarily due to Al oxidation process. However, more detailed studies are required in order to understand the mechanism(s) of high Al- content material "aging". The "aging" manifested itself by a significant reduction (or even disappearance) of the main PL line intensity, which we attribute to the band edge emission. The aging of a-face crystals was significantly less that for c-face and more pronounced than for m-face.

We should stress here that although "aging" was very different for various crystal faces, all surfaces exhibited more than order of magnitude lower PL intensity compared to a freshly cleaved bulk crystal surface. Similar results were obtained for AlN and high Al content (> 50%) AlGaN epitaxial layers grown over sapphire substrates.

We also observed this kind of aging process in our AlGaN/GaN HEMT technology. The heterostructure consisted of a 1 μm insulating GaN layer capped with a 30 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, which was doped with Silicon approximately to 2 x 10^{18} cm^{-3}. No surface passivations of any forms were performed any time within the data collection process.

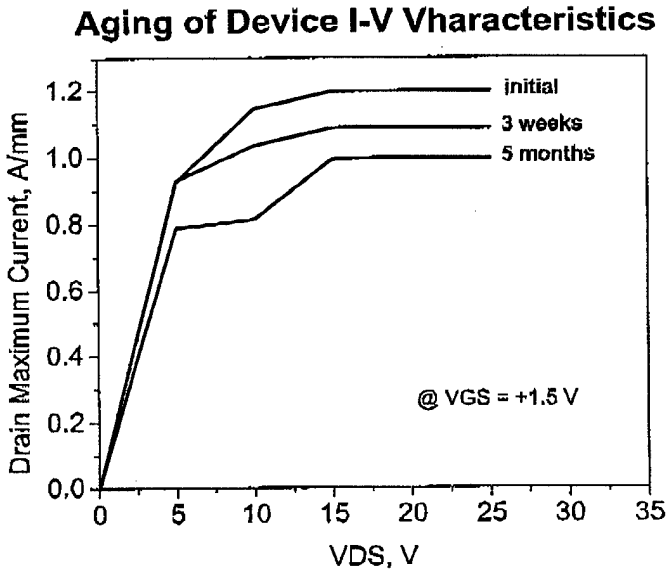


Fig. 15 HEMT maximum drain current (Saturation Current) 5 months after processing, three weeks after processing, and within a 24-hours time-frame after processing.

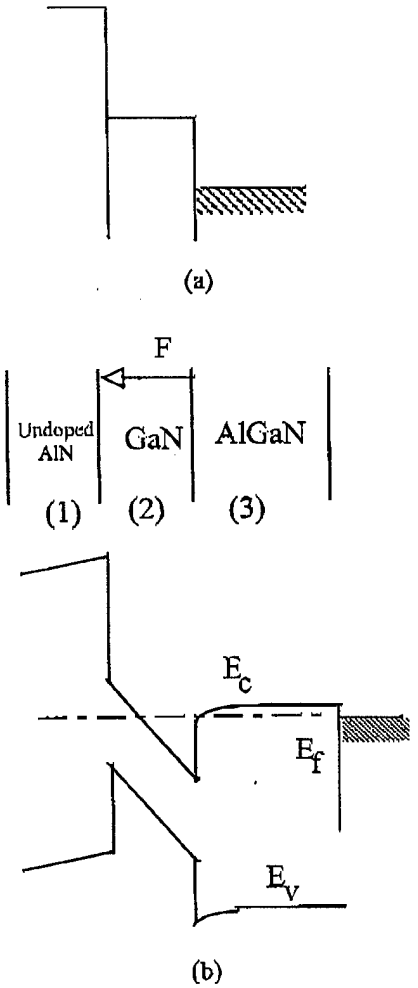


Fig. 17 Estimated band diagram of the half-crested barrier (a) Ideal conduction band structure (b) Band structure including the piezoelectric charge effect

It is shown that when the thickness of the GaN layer is larger than the critical thickness (around 10nm), there will be local strain relaxation because of excessive strain in the structures. These excessive strains are dependent on the Al composition.

In Fig. 18, the calculation results of the sheet electron density generated by the piezoelectric doping in AlGaN/GaN structure[5]. The results shows thinner AlGaN with larger Al content will yield a higher piezoelectric charge. Thus, for our $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ structure, when x=1 and the top AlN thickness is only 10nm, there should be considerable piezoelectric charge at the interface. Even at x=y=0.2, the with the GaN and AlGaN

[5] M. S. Shur, A. D. Bykhovski, R. Gaska, and A. Khan, GaN-based Pyroelectronics and Piezoelectronics, in Handbook of Thin Film Devices, Volume 1: Hetero-structures for High Performance Devices, Edited by Colin E.C. Wood, Handbook edited by Maurice H. Francombe, pp. 299-339, Academic Press, San Diego, 2000

thickness of 10nm, partial stress relaxation may exist in the layer which induced large piezoelectric charge density. The conductance in AlGaN/GaN/AlGaN structure should be smaller than the AlN/GaN/AlGaN structure due to its smaller strain effect as can be seen from Fig. 18.

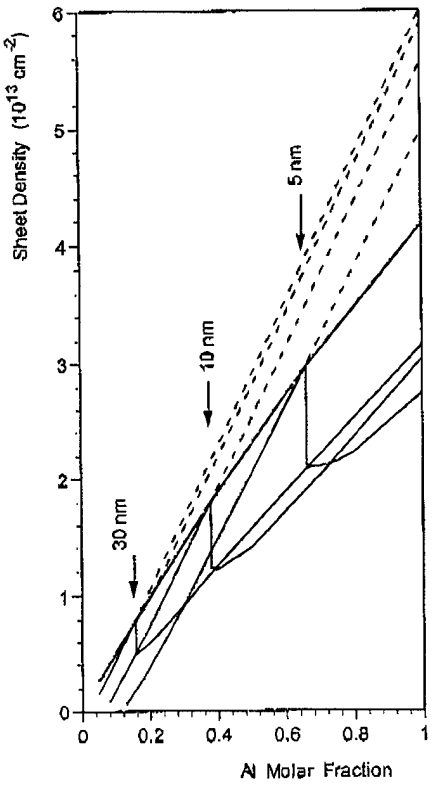


Fig. 18. Electron sheet density, n_s, induced by polarization in $Al_xGa_{1-x}N$-GaN heterostructures with different aluminum molar fractions and various AlGaN barrier layer thicknesses: 1 - 30 nm; 2. 20nm; 3 - 10 nm; 4 - 5 nm. Arrows show the onset of strain relaxation. Thick solid line shows sheet electron density corresponding to critical thickness of AlGaN versus aluminum molar fraction. Dashed lines show n_s for unrelaxed heterostructures. (From [5])

The deviation of the band diagram from the ideal band structure (See Fig. 17) makes the whole AlN/GaN/AlGaN layer sensitive to metallization quality. Another effect we may have to consider is the tunneling effect in the AlN because of its small thickness. Both of these technology issues can increase the vertical conductance of our structure. We believe the large unrelaxed strain is another reason for a large vertical conductance in our crested barrier structure. We should investigate the influence of the large sheet charge density on the on/off ratio of the rectification in the future.

Dr. Jianyu Deng
Principal Investigator