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VACUUM PACKAGING FOR MICROELECTROMECHANICAL SYSTEMS (MEMS)

Raytheon Company

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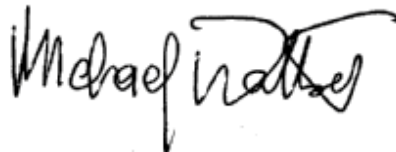
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13. ABSTRACT (Maximum 200 Words) The Vacuum Packaging for MEMS Program focused on the development of an integrated set of packaging technologies which in totality provide a low cost, high volume product-neutral vacuum packaging capability which addresses all MEMS vacuum packaging requirements. The program balanced the need for near term component and wafer-level vacuum packaging with the development of advanced high density wafer-level packaging solutions. Three vacuum packaging approaches were pursued: large area component level; 4"/6" wafer-level; and wafer-level microshell encapsulation. The program focused on packaging for MEMS accelerometers and gyros; IR MEMS a-Si microbolometer and ferroelectric detectors; and RF MEMS resonators. Successful demonstrations were accomplished with IR MEMS microbolometers in sub 10 mTorr vacuum packages, inertial MEMS resonant accelerometers in sub 200 mTorr vacuum packages and an RF MEMS resonator demonstration. In addition to the successful demonstrations, numerous component and wafer-level vacuum packages passed extensive MIL standard environmental tests.				
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1. EXECUTIVE SUMMARY

1.1. Program Goals and Raytheon Electronics Systems Team

The Vacuum Packaging for MEMS Program focused on the development of an integrated set of packaging technologies which in totality provide a low cost, high volume product-neutral vacuum packaging capability which addresses all MEMS vacuum packaging requirements. The program focused on low cost, product-neutral vacuum packaging for enhanced performance MEMS sensors including inertial MEMS accelerometers and gyros; IR MEMS a-Si microbolometer and ferroelectric detectors; and RF MEMS resonators. A vacuum level of less than 10 mTorr is required in some of these applications.

The Raytheon Electronics Systems Team is shown in Table 1.1.1 and included the University of California at Berkeley (UC Berkeley) Sensor and Actuator Center; the Massachusetts Institute of Technology (MIT); and Sandia National Laboratories. In addition, under the program, Raytheon carried out system insertion activities with government agencies including the Air Force Research Laboratory (AFRL); the Naval Surface Weapons Center (NSWC); and the Army Research Laboratory (ARL). The program goals of each of the team members towards the development of an integrated set of MEMS vacuum packaging technologies are summarized in the Table 1.1.1.

Table 1.1.1. Raytheon Electronics System Team including participating government agencies for system insertion activities together with goals of each team member.

Team Member	Principal Investigator	Program Goals
Raytheon	Thomas Shimert	1. Large area component level vacuum packaging 2. 4”/6” wafer-level vacuum packaging using solder seal 3. System insertion activities with government agencies
MIT	Martin Schmidt	4. High density wafer-level vacuum packaging
UC Berkeley	Roger Howe	5. Wafer-level microshell/microcap encapsulation vacuum packaging 6. Wafer-level packageable inertial MEMS resonant accelerometer and gyroscope design, layout and testing
Sandia	Steve Montague	7. Fabrication of wafer-level packageable inertial MEMS resonant accelerometers and gyroscopes
AFRL	Duane Gilmour	8. MIL standard environmental testing of IR MEMS and inertial MEMS vacuum packages
NSWC	Don Garvik	9. MEMs Torpedo Fuzing/Safety and Arming System chip-level package assembly
ARL	Bill D’Amico	10. High-g shock testing of wafer-level vacuum packages

1.2. Program Approach to Product-Neutral MEMS Vacuum Packaging

A description of the product-neutral vacuum packaging strategy employed under the program together with the team member's respective technology thrusts to achieve comprehensive low cost, product-neutral MEMS vacuum packaging is described in more detail in Figure 1.2.1. The program balanced the need for near term wafer-level vacuum packaging with the development of advanced high density wafer-level packaging solutions. The three approaches pursued were Large Area Component Level Vacuum Packaging (Raytheon); 4"/6" Wafer-level Vacuum Packaging (Raytheon /MIT); and Wafer-level Microshell Encapsulation Vacuum Packaging (UC Berkeley).

Large Area Component Level Vacuum Packaging (Raytheon)

The large area component level packaging approach in Figure 1.2.1 involves a large cavity (0.7" x 0.7") 84 pin ceramic package sealed with a silicon or germanium lid. The lid is solder-sealed to the package in an integrated seal process that employs a vacuum bake cycle followed by an *in situ* package seal. The process had been used extensively at Raytheon in the prototype production of smaller 16 pin CERDIP vacuum packages (0.32"x0.21" cavity). The component level packaging approach targeted the near term packaging demands for large area MEMS applications including large 6 axis inertial MEMS as well as large IR MEMS arrays including the important large staring uncooled IR focal plane array applications (i.e., 640x480 and 1024x1024 formats). In addition, the large area component level packaging permits the rapid demonstration, evaluation and system insertion of vacuum-packaged prototype and specialty MEMS chips.

Wafer-Level Vacuum Packaging

Wafer-level vacuum packaging is the low cost, high volume MEMS packaging approach developed under this program. The intrinsic low cost of this approach stems from the fact that all die on a wafer are sealed in one step and subsequently tested at the wafer-level thereby yielding substantial saving in time, materials and labor. All the team members contributed to this effort. The wafer-level packaging strategy balanced the need for near term wafer-level vacuum packaging with the development of advanced, higher risk high density wafer level packaging solutions. The wafer-level packaging approaches are also described in Figure 1.2.1.

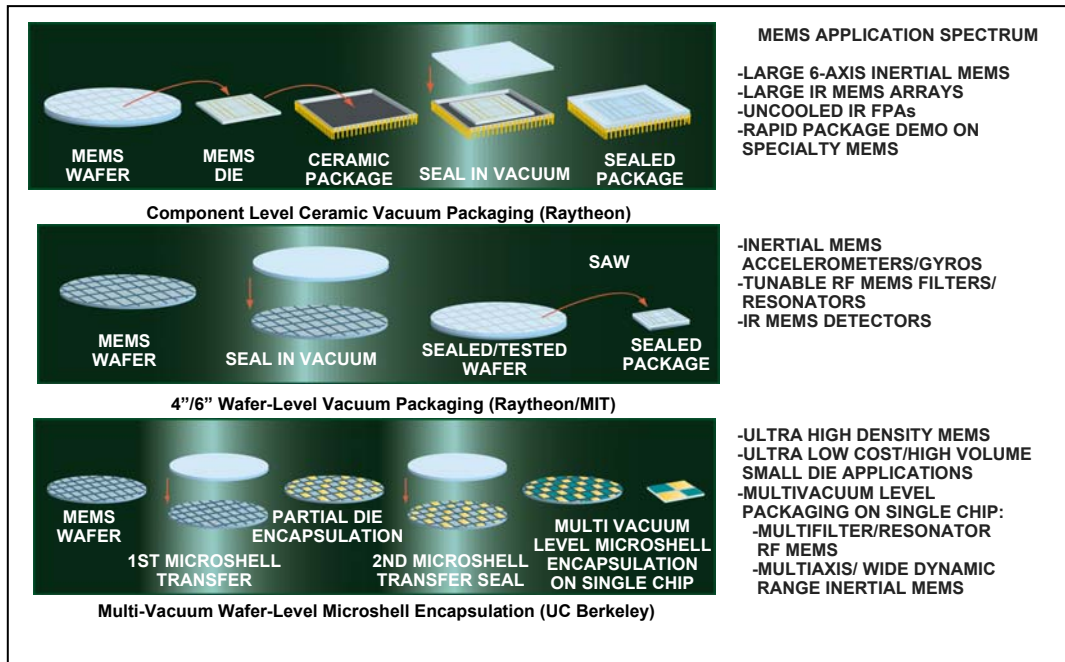


Figure 1.2.1 Product-Neutral Vacuum Packaging Strategy.

4''/6'' Wafer-Level Vacuum Packaging (Raytheon /MIT)

Raytheon was responsible for the development of the near term production solution to 4''/6'' wafer-level vacuum packaging which employs a solder seal approach. This solder seal approach had been used successfully in component level vacuum packaging developed at Raytheon and as such was the most mature sealing method. This approach employs the same basic processing steps used in the component level packaging process thereby substantially reducing development risk.

Advanced high density 4'' wafer-level packaging development was carried out by MIT. The focus of the MIT effort was to increase die density by reducing seal ring area requirements and increasing interconnect density. Reduced seal ring area was accomplished by replacing the thick plated solder seal process with a thin Au thermocompression bonding approach. Increased interconnect density was achieved by using a through-cap interconnect process. The payoff of this high density wafer-level package development is lower cost production. The advanced wafer-level package interconnect and seal ring technology will be transitioned into the long term wafer-level production process as the technology is proven.

The targeted applications for wafer-level vacuum packaging include inertial MEMS accelerometers and gyros; tunable RF filters and resonators; and IR MEMS uncooled detectors and IR MEMS high speed sources.

Wafer-Level Microshell Encapsulation Vacuum Packaging (UC Berkeley)

The second wafer-level packaging approach employs a wafer-wafer transfer SiGe microshell or microcap encapsulation process. UC Berkeley was responsible for this development effort. In this approach, microcaps are surface micromachined on a donor wafer. The microcaps are

tethered to the donor wafer. During the seal the microcaps are transferred to the MEMS wafer. Each microcap encapsulates an individual die. The donor wafer is freed by breaking the tethers. The microshell encapsulation process offers the potential for an ultrahigh density packaging process for ultra low cost, high volume MEMS applications. In addition, the microcap transfer process offers the unique capability for multi-vacuum level packaging on a single chip thereby meeting the vacuum packaging requirements of multifilter/resonator RF MEMS and multiaxis or wide dynamic range inertial sensors for which the component MEMS may require different operating vacuum levels.

With regard to risk versus payoff of the wafer-level vacuum packaging approaches pursued under the program, the Raytheon solder bonding approach is the most mature approach and offers a near term low cost package production process. In fact, as this program ends, Raytheon is in the process of transitioning its 6" wafer-level solder seal vacuum packaging approach into production in the manufacture of its infrared imaging 120x160 amorphous silicon (a-Si) focal plane arrays. The somewhat riskier MIT high density Au thermocompression bonding approach with increased interconnect density offers the payoff of lower cost. The UC Berkeley microshell encapsulation process, while the riskiest approach, offers the payoff of ultra high density MEMS packaging. More importantly, this approach offers the unique capability for multi-vacuum level packaging on a single chip thereby permitting MEMS chip designers to use vacuum level as a design parameter in complex RF and inertial MEMS chips. This potentially can lead to a substantial increase in the capability of these MEMS chips.

1.3. Summary of Major Program Accomplishments

A summary of program accomplishments relative to program goals is contained in Table 1.3.1. Also included in the table is a summary of System Insertion Efforts carried out under this program.

Table 1.3.1 Summary of major accomplishments.

Program Goal	Accomplishment
Large area component-level vacuum packaging (Raytheon)	• <10 mTorr IR MEMS microbolometer large area component-level ceramic vacuum package milestone demonstrated using 84 pin alumina ceramic package (0.7"x0.7" cavity). • Multi-package sealing process for 84-pin vacuum package for large area (>1 cm²) MEMS milestone demonstrated. • Inertial MEMS high-Q resonator vacuum package milestone demonstrated using 16 pin CERDIP and 84-pin ceramic vacuum packages. • Demonstrated packaging of Inertial MEMS Double Tuning Fork Resonant Accelerometer in 84-pin ceramic vacuum package. • Delivered vacuum packaged RF MEMS resonators to the University of Michigan in 84 pin ceramic packages.
4"/6" Wafer-level vacuum packaging using AuSn solder seal	• <10 mTorr IR MEMS microbolometer 1" wafer-level vacuum package milestone demonstrated. • <10 mTorr IR MEMS microbolometer 4" wafer-level vacuum package milestone demonstrated. • Validation of 4" wafer-level vacuum packaging process by achieving 99% seal yield (103 of 104 IR MEMS bolometer die) over a 4" IR MEMS wafer. • Demonstrated 6" wafer-level vacuum packaging process for IR MEMS microbolometers. • Demonstrated IR MEMS bolometer wafer-level vacuum package with 38 month stability with no degradation in package vacuum. • Demonstrated 1" wafer-level packaged Inertial MEMS chip with sub 100 mTorr vacuum. • Demonstrated wafer-level vacuum packaging of inertial MEMS accelerometers, gyros and microresonators using 6" wafer-level packaging process.
High density wafer-level vacuum packaging (MIT)	• Demonstrated thru-wafer interconnect scheme for capping wafer for high density wafer-level vacuum packaging. • Demonstrated Au thermocompression bond over 300-350°C temperature range. • Optimization of thermocompression bond metrology system for 4" wafers. • Optimized Au lift-off process, Ti/Al metallurgy; and Au deposition process for improved Au thermocompression bond yield. • Developed silicon fusion bond characterization tool that minimizes instrument non-linearity. • Demonstrated Au thermocompression vacuum seal with sub 0.15 atm vacuum.

Table 1.3.1 Summary of major accomplishments (continued).

Program Goal	Accomplishment
Wafer-level microshell encapsulation vacuum packaging (UC Berkeley)	• Demonstrated first polysilicon wafer-wafer microcap transfer process. • Demonstrated new process for SiGe structural layer and Ge sacrificial layer mold for the microshell vacuum encapsulation structure. • Optimized low stress SiGe microcap process and release etch for the microshell vacuum encapsulation structure. • Demonstrated successful transfer of 1.8 mm x 1.8 mm poly-SiGe hexsil microcaps to MEMS resonator chip wafer using thermocompression bonding. • Developed etchant ducts in SiGe microcap to improve mass transport of reactants and products during SiGe microcap release process. • Improved gold rivet design to increase transfer yield of released SiGe microcap from donor to MEMS wafer.
Design and fabrication of Wafer-level packageable inertial MEMS accelerometers and gyros (UC Berkeley and Sandia)	• Operational wafer-level packageable resonant accelerometer and microresonator structures demonstrated
MIL standard environmental testing of IR MEMS and inertial MEMS vacuum packages (System Insertion Activity involving AFRL/Raytheon)	• Demonstrated up to 1500 Hrs @150°C high temperature bake stability for Inertial MEMS and IR MEMS ceramic vacuum packages and IR MEMS wafer-level vacuum packages. • Demonstrated 1000 Hrs high temp/high humidity (85°C/85% RH) bake stability IR MEMS wafer-level vacuum packages. • Demonstrated 150 Hrs accelerated high temp/high humidity (130°C/85% RH) bake stability IR MEMS ceramic and wafer-level vacuum packages. • Demonstrated 1000 cycles -65°C to 150°C for Inertial MEMS and IR MEMS ceramic vacuum packages.
High-g shock testing of wafer-level vacuum packages (System Insertion Activity involving ARL/Raytheon)	• 6 IR MEMS microbolometer wafer-level packages were delivered to ARL for high-g shock testing. • Demonstrated IR MEMS wafer-level microbolometer 10,000-g shock test without failure.
MEMs Torpedo Fuzing/Safety and Arming System chip-level package assembly (System Insertion Activity involving NSWC/Raytheon)	• Raytheon worked with NSWC to provide a chip level package for the MEMS F/S&A. • Raytheon initially delivered 27 silicon base test chip-to-ceramic initiator test chip assemblies to NSWC for environmental testing (thermal shock, mechanical shock and accelerated aging). • Raytheon packaged and delivered 10 functional MEMS F/S&A chips to NSWC.

In addition to the system insertion activities carried out under this program, the insertion of wafer-level vacuum packaging into an uncooled imagers 160x120 a-Si focal plane array (FPA) was carried out under the DARPA ATO funded Autonomous Networked Tactical Sentries (ANTS) Program (Ed Carapezza) and the DARPA MTO Fused Image Sensor (FIS) Program (Ray Balcerak). Under these programs, Raytheon demonstrated a proof-of-concept low cost, low power uncooled infrared micro IR camera. To accommodate the size and cost requirements, the a-Si 120x160 focal plane array (FPA) employed wafer-level vacuum packaging developed under the Vacuum Packaging for MEMS program. This is the first system demonstration employing a wafer-level packaged IR MEMS a-Si microbolometer FPA.

2. DESCRIPTION OF RESEARCH CARRIED OUT TO MEET PROGRAM GOALS

2.1. Component Level Packaging

The component-level ceramic packaging approach shown in Figure 2.1.1 was carried out early in the program to target near term demands for packaging of large area MEMS applications. These included multiaxis inertial MEMS chips as well as large format monolithic uncooled detectors and focal plane arrays (FPAs) such as 320x240 and 640x480 array formats. In addition, the large area component-level packaging permits the rapid demonstration and evaluation of vacuum packaged prototype and specialty MEMS chips.

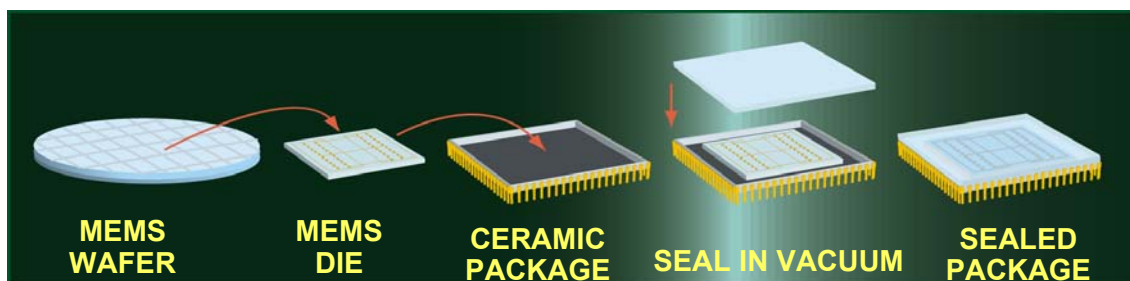


Figure 2.1.1 Component-level vacuum packaging approach.

2.1.1. Large Area IR MEMS Microbolometer Component-level Packaging Demonstration

The first large area vacuum packaging demonstration carried out under the program involved the packaging of IR MEMS a-Si microbolometer arrays. The a-Si microbolometer structure is a surface micromachined low thermal mass pixel structure suspended above the substrate by long thermal isolation legs as shown in Figure 2.1.1.1. The microbolometer detects infrared radiation by efficiently absorbing IR energy incident on the detector structure that causes the suspended pixel to heat up. The a-Si has a temperature coefficient of resistance of approximately 2.7%/K. Hence a change in pixel temperature causes a modulation in the a-Si resistance which is used to detect the incident radiation. To achieve maximum pixel temperature change and hence microbolometer signal, these 2 mil pixel elements are well thermally isolated from the substrate by long thermal isolation legs giving rise to high thermal resistance, $R_{th} > 4 \times 10^7 \text{ K/W}$. In fact the thermal resistance of the pixel with respect to the substrate is within a factor of 4 of the radiative thermal resistance limit.

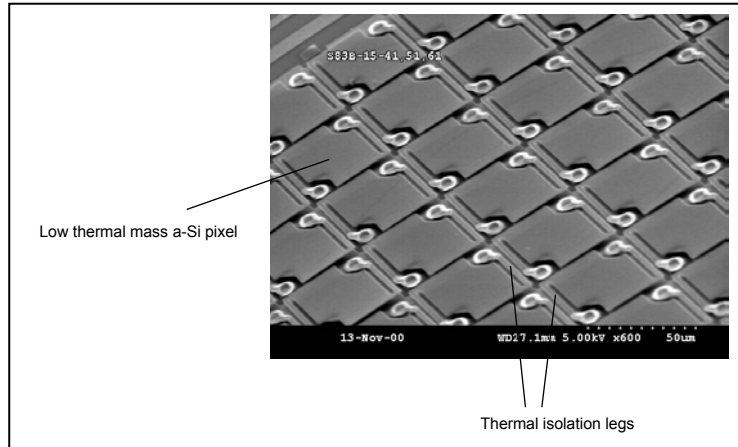


Figure 2.1.1.1 IR MEMS a-Si microbolometer pixel structure.

To practically achieve the maximum signal, the microbolometer must be vacuum packaged to minimize thermal conductance through residual gas in the package. Figure 2.1.1.2 shows a plot of residual package vacuum pressure varied between 1 Torr and 1 mTorr versus microbolometer thermal resistance (R_{th}). The data shows that residual package vacuum impacts thermal resistance for vacuum pressures down to ~ 10 mTorr. Below 10 mTorr, package vacuum has minimal effect on thermal resistance. Hence a package vacuum requirement of <10 mTorr was established for IR MEMS microbolometer detectors and FPAs.

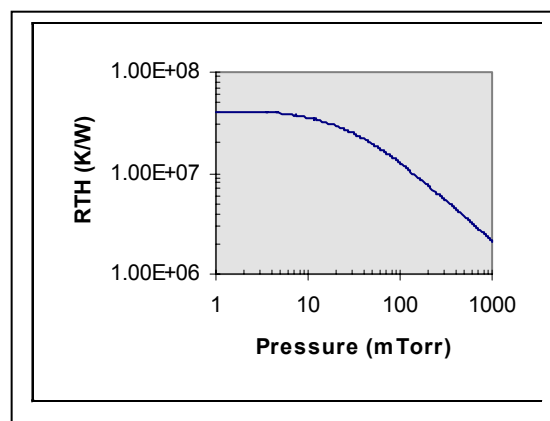


Figure 2.1.1.2 Impact of residual package vacuum pressure (mTorr) on microbolometer thermal resistance (R_{th}).

The demonstration of large area IR MEMS microbolometer vacuum packaging was carried out using two 256×78 a-Si microbolometer arrays mounted in the 84-pin alumina ceramic package as shown in Figure 2.1.1.3. This 84-pin alumina ceramic package has a $0.7'' \times 0.7''$ cavity area. In this package, designed for nonimaging sensor applications, each of the 256×78 arrays are electrically connected into three large area superpixel arrays to enhance detector sensitivity. The package shown in Figure 2.1.1.3b employed a AuSn solder-sealed antireflection (AR)-coated

germanium window with an 8-12 μm spectral bandpass. The Ge window is used because of its transparency in the 8-12 μm spectral band and also because of the low coefficient of thermal expansion (CTE) mismatch between the alumina (Al_2O_3) ceramic package ($\text{CTE}_{\text{Al}_2\text{O}_3 \text{ ceramic}} \sim 7 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$) and the Ge window ($\text{CTE}_{\text{Ge}} \sim 6.3 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$). Close CTE match was found to be critical requirement for a high yield, reliable AuSn solder seal process using this large package because of the relatively high AuSn solder wetting temperature of 283C.

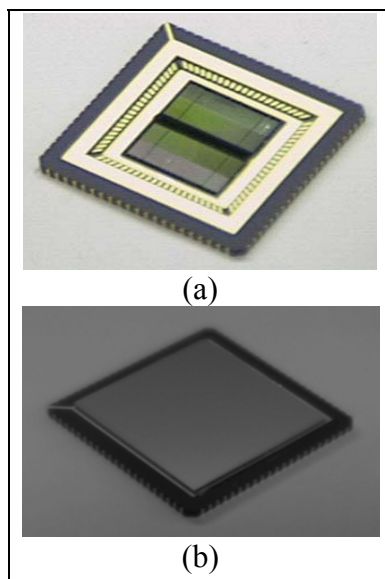


Figure 2.1.1.3 84- pin Ceramic Package a) showing mounted arrays, b) sealed (cavity dimensions: 0.7”x0.7”)

Vacuum packaging results obtained on the sealed 84 pin package are shown in Figure 2.1.1.4. Obtaining an accurate calibration of the microbolometer signal (and hence thermal isolation) as a function of vacuum is a key element in obtaining an accurate vacuum measurement for the sealed package. The obvious approach involves mounting the package in a vacuum Dewar prior to sealing and carrying out signal versus vacuum level measurements to obtain a calibration curve. However, this approach does not take into account any small change in microbolometer signal that may occur during the sealing process or the effect of IR transmission through the lid. To remove these calibration uncertainties, package calibration was performed after the package was sealed and tested by drilling a hole in the lid of the sealed package, thereby breaking the package vacuum. The package was subsequently placed in a vacuum Dewar and a post-seal calibration curve of microbolometer signal versus vacuum level was carried out. This calibration method mitigates any possible changes in microbolometer signal due to the solder seal process and lid IR transmission effects. A large area 84 pin ceramic vacuum package post-seal calibration curve of microbolometer signal versus vacuum level is shown in Figure 2.1.1.4. The microbolometer signal level measured for the sealed package in this case is 101 mV. From the calibration curve in the figure, this corresponds to sealed package vacuum of 3 mTorr, which meets the sub 10 mTorr package vacuum requirement.

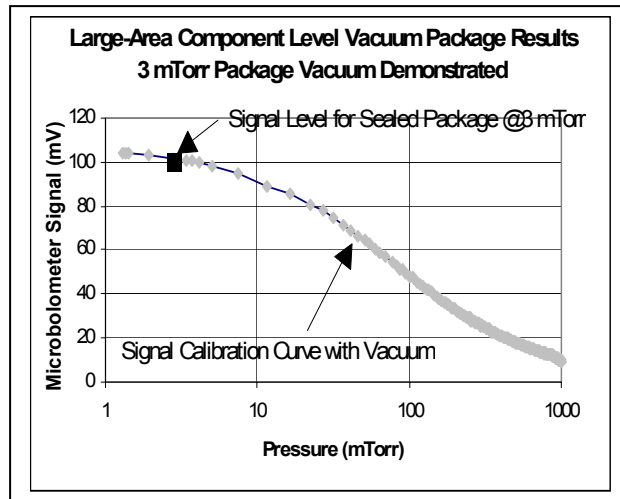


Figure 2.1.1.4 IR MEMS 84-pin ceramic vacuum packaging results.

As remarked above, a Ge lid/window ($CTE_{Ge} \sim 6.3 \times 10^{-6} \text{ C}^{-1}$) was used in this demonstration because of the close CTE match with the alumina (Al_2O_3) ceramic package ($CTE_{\text{Al}_2\text{O}_3 \text{ ceramic}} \sim 7 \times 10^{-6} \text{ C}^{-1}$). An alternate lid/window choice would be silicon. However, silicon ($CTE_{\text{silicon}} \sim 3.3 \times 10^{-6} \text{ C}^{-1}$) is a poor match to the alumina ceramic package. Attempts to seal alumina ceramic packages with silicon lids proved unreliable. This is because the lid/package CTE mismatch caused the package seal to break after solder seal, as the package cooled from the AuSn wetting temperature of 283°C to ambient temperature. This was due to stress between the lid and the package. As an alternative to an alumina ceramic package, a mullite ceramic package, with $CTE_{\text{Mullite}} \sim 4.2 \times 10^{-6} \text{ C}^{-1}$, which is a close match to silicon with a $CTE_{\text{silicon}} \sim 3.3 \times 10^{-6} \text{ C}^{-1}$, was investigated. It was found that the mullite package/silicon lid combination proved a reliable component-level vacuum packaging system.

Finally, an IR MEMS large area component vacuum package demonstration involving the simultaneous seal of five packages was carried out under the program. In this multi-package seal demonstration, four of the five 84-pin ceramic packages sealed resulting in an 80% seal yield.

2.1.2. Inertial MEMS Microresonator Packaging Demonstration

The first Inertial MEMS vacuum packaging demonstrations carried out under the program involved the packaging of microresonators in the 16-pin Cerdip ($0.210'' \times 0.320''$ cavity) shown in Figure 2.1.2.1a and b and the 84 pin ceramic package shown in Figure 2.1.2.1c. The results obtained for the UC Berkeley-designed, Sandia-fabricated 140 kHz microresonators is shown in Figure 2.1.2.2. The 140 kHz microresonator signal versus vacuum level calibration was carried out using an unsealed reference package #20 in a vacuum Dewar. The results of the calibration taken over the range 14-500 mTorr are shown in Figure 2.1.2.2a using a 10V field plate bias. The calibration shows the signal amplitude remains constant below ~ 200 mTorr indicating that the microresonator amplitude is unaffected by the package vacuum. Above 200 mTorr, the signal amplitude begins to drop. At ~ 500 mTorr, the microresonator ceased oscillating.

In Figure 2.1.2.2b, the signal amplitude versus field plate bias for 3 sealed microresonator packages is compared with the calibrated reference package #20 results taken in the Dewar test at 14 mTorr. The sealed package results are in excellent agreement with the reference package results indicating that the package vacuum in the sealed packages is below ~ 200 mTorr and is not affecting the microresonator properties.

This demonstration established a 200 mTorr package vacuum requirement for the Inertial MEMS microresonator structure.

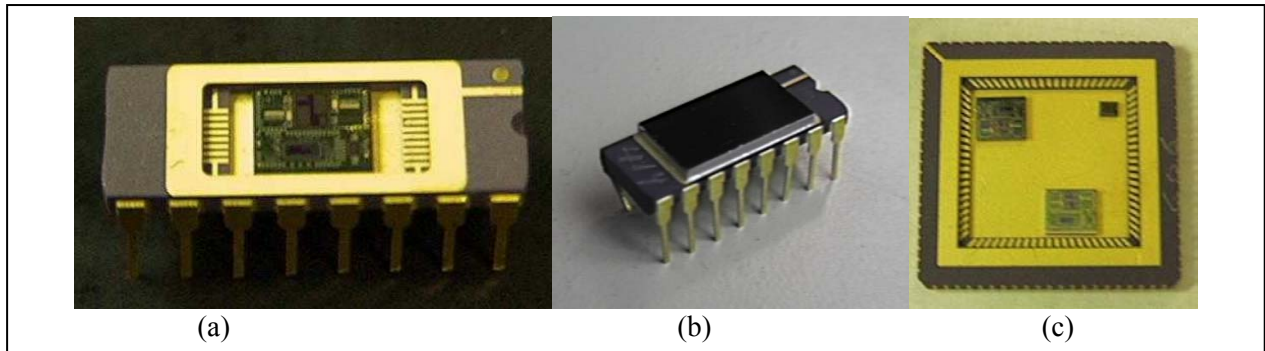


Figure 2.1.2.1 a) 16 pin Cerdip with 140 kHz microresonator die, b) Sealed package with Si lid, c) Two Inertial MEMS die with microresonators and resonant accelerometers (RXLs) mounted in 84-pin ceramic package.

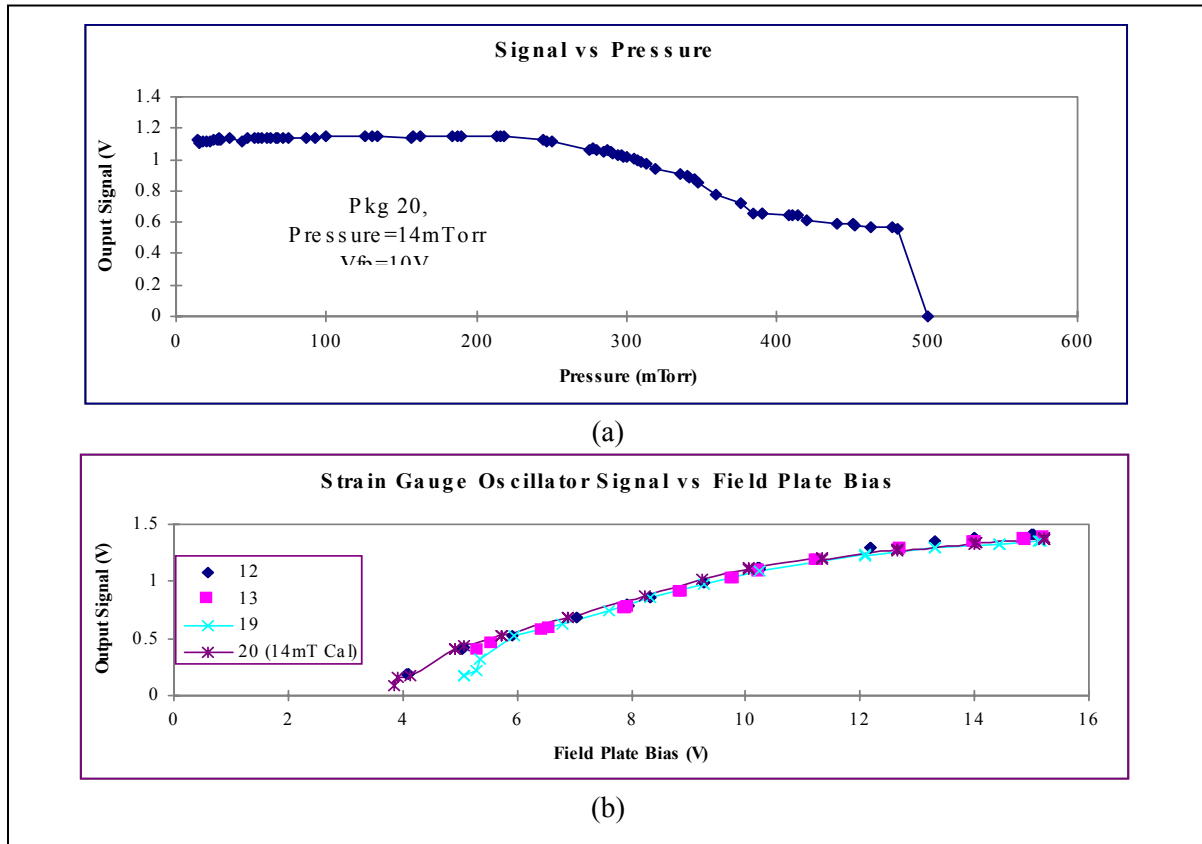


Figure 2.1.2.2 a) 140 kHz microresonator output signal amplitude versus vacuum for reference package #20 using 10V field plate bias, b) Output signal amplitude versus field plate bias for sealed packages #12, 13, 19 and reference package #20 at 14 mTorr.

2.1.3. Inertial MEMS RXL Component-level Packaging Demonstration

During the program, the Raytheon Team demonstrated a vacuum packaged inertial MEMS double tuning fork resonant accelerometer (RXL) in the 84 pin ceramic package shown previously in Figure 2.1.2.1c. An optical photograph of the double tuning fork RXL is shown in Figure 2.1.3.1a. An inertial MEMS RXL demo unit using the vacuum packaged RXL is shown in Figure 2.1.3.1b. The UC Berkeley-designed, Sandia-fabricated RXL employed dual 140 kHz microresonator structures. It was verified that each of the 140 kHz microresonators in the RXL exhibited a signal versus vacuum level calibration curve similar to that shown above in Figure 2.1.2.2a. This served to establish the 200 mTorr package vacuum requirement for the RXL as well.

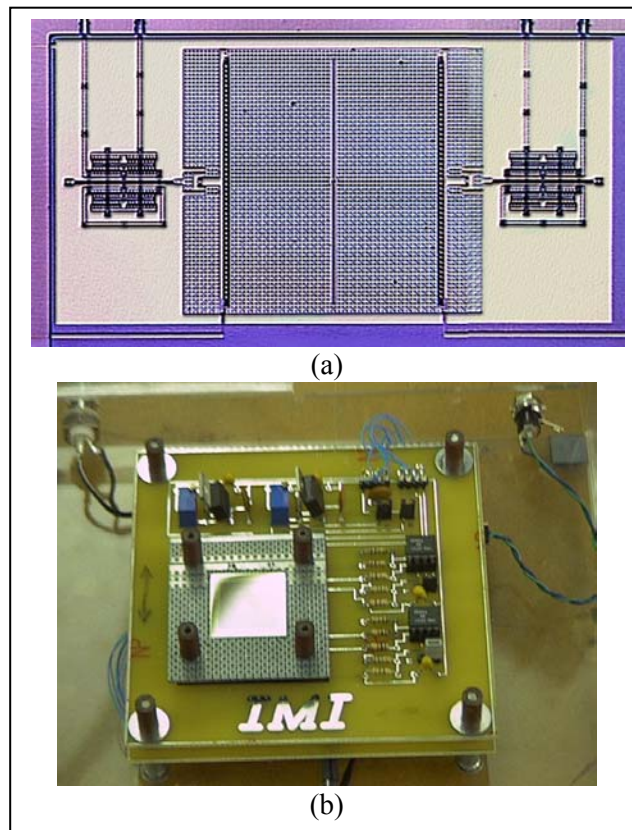


Figure 2.1.3.1 a) Optical photograph of double tuning fork RXL, b) RXL demo unit.

A successful demonstration of the double tuning fork RXL was carried out using the demo unit shown in Figure 2.1.3.1b. The resonant accelerometer exhibited <2 kHz mismatch tuning fork frequency. This represented the first demonstration of a functioning vacuum packaged double tuning fork RXL.

2.2. Wafer-level Vacuum Packaging (Raytheon)

Packaging is a significant cost driver in MEMS production. A major goal in this program was to demonstrate a wafer-level approach to vacuum packaging that significantly reduced cost by carrying out package sealing tasks at the wafer-level as opposed to the die or chip level. This reduces touch labor and cycle time by eliminating the labor-intensive task of having to handle die and package die separately in ceramic packages. The wafer-level packaging approach is described in Figure 2.2.1. Under the program Raytheon demonstrated a high temperature AuSn (283°C) solder-seal wafer-level packaging approach. In addition, Raytheon also demonstrated a low temperature Indium (156°C) solder seal approach. The initial demonstrations involved 1" IR MEMS microbolometer and Inertial MEMS proof-of-concept demonstrations. Subsequently, 4" and 6" wafer-level package demonstrations and validations were carried out.

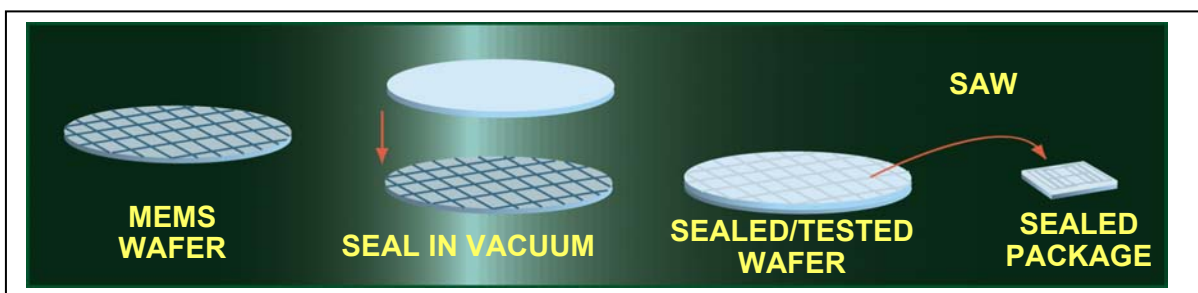


Figure 2.2.1 Wafer-level vacuum packaging approach.

2.2.1. IR MEMS Microbolometer 1" Wafer-level Packaging Demonstration

A 1" wafer-level IR MEMS microbolometer package is shown in Figure 2.2.1.1. In the 1" format a total of 6 individual microbolometer die were sealed simultaneously. A sealed 1" wafer is shown in Figure 2.2.1.1a. An unsealed 1" wafer showing the seal ring geometry for the six individually packaged a-Si microbolometer die is shown in Figure 2.2.1.1b. The 1" wafer contains four 2 channel nonimaging sensor style microbolometer package die and two 4 channel package die, respectively. The sealed bolometer cavity is addressed using a metal interconnect running under the gold seal ring as shown in Figure 2.2.1.1b. The seal ring is 0.035" wide. The AuSn solder preform was 0.030" wide and 2 mils thick. The interconnects are electrically isolated from the seal ring by an $\sim 3500\text{\AA}$ insulating SiN layer deposited over the gold seal ring. In the seal process, the AuSn preform was placed on the lid wafer and the IR MEMS microbolometer wafer was placed upside down aligned with the lid wafer seal ring. An approximately 0.25" stainless steel plate was placed over the inverted MEMS wafer to provide additional weight during the seal process. In the case of IR MEMS microbolometer packaging, the Si lid thickness was no more than 0.025" to minimize IR absorption in the lid material. An antireflective coating was also applied to the Si lid which enhanced the IR transmittance of the lid.

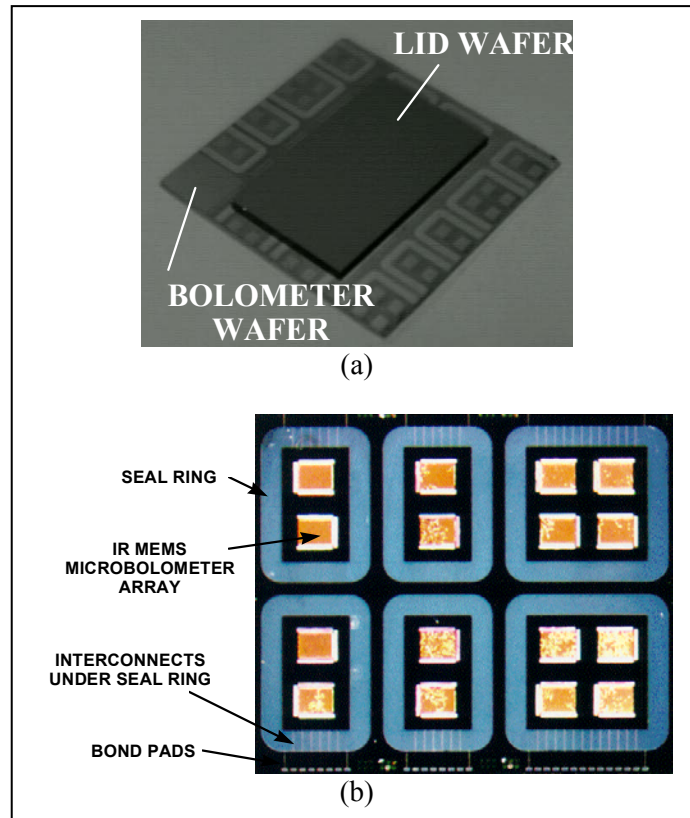


Figure 2.2.1.1 a) 1'' wafer-level vacuum package, b) Seal ring architecture.

Wafer-level vacuum package results from the 1'' package demonstration are shown in Figure 2.2.1.2. As with the component-level ceramic vacuum package demonstration, to obtain accurate calibration of a wafer-level vacuum packaged die, a hole was drilled in one of the sealed packages and the package was placed in a vacuum Dewar to obtain the calibration curve of microbolometer signal versus vacuum pressure shown in the figure. Using the curve, the signal in the sealed package (54 mV) corresponds to a sealed vacuum level of 9 mTorr. Note that this signal is half that observed in the large area vacuum package shown in Figure 2.1.1.4 because in these initial IR MEMS vacuum package demonstrations, the lid wafer was not antireflection (AR) coated. This demonstration served to show that <10 mTorr package vacuum could be achieved in an IR MEMS microbolometer wafer-level package. Finally, it is noted that early in the program a total of twelve 1'' wafer-level IR MEMS packages were sealed giving early indication that the sealing process was reliable and repeatable.

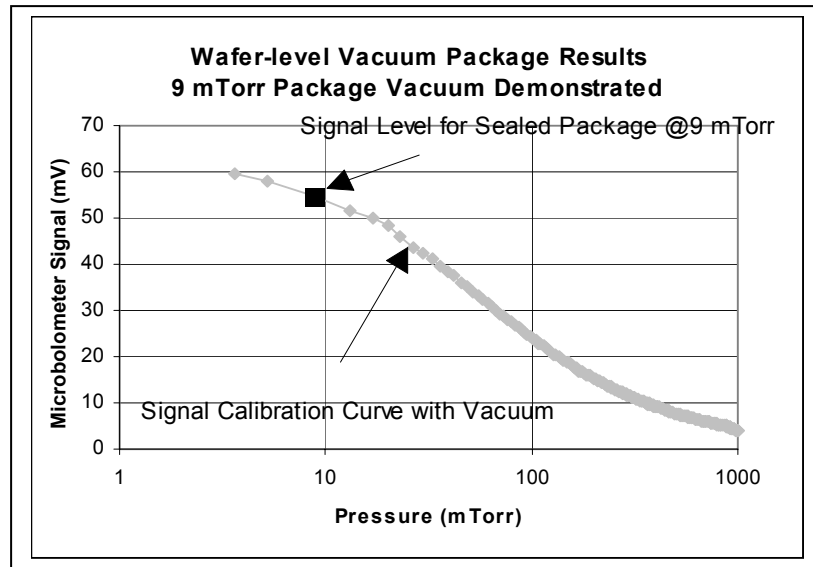


Figure 2.2.1.2 Sub 10 mTorr package vacuum demonstration in 1" IR MEMS microbolometer wafer-level package.

2.2.2. Vacuum Stability of Wafer-level Packaged IR Bolometer Packages

Over the duration of the program, one of the 1" wafer-level IR MEMS microbolometer packages that was sealed early in the program on 11/26/97 was periodically retested a total of 16 times to assess vacuum stability in each of the 6 die. The results of the vacuum level stability measurements of the six package die in a 1" IR MEMS wafer-level vacuum package are shown in Figure 2.2.2.1. The vacuum level stability measurements were carried out over a 38 month period. The microbolometer signal in five of the six package die is shown to remain steady or increase indicating that wafer-level package vacuum has not deteriorated. The rise in signal seen in the results is likely due aging effects in this early microbolometer design in which the microbolometer pixel body was prone to thermal shunting to the substrate due to pixel stress. An increase in pixel response is an indication that the pixel thermal shunting was ameliorating in the aging process. A short developed in package die #1 making data unavailable after the third measurement. These results are the first demonstration of a long term reliable wafer-level IR MEMS microbolometer vacuum package.

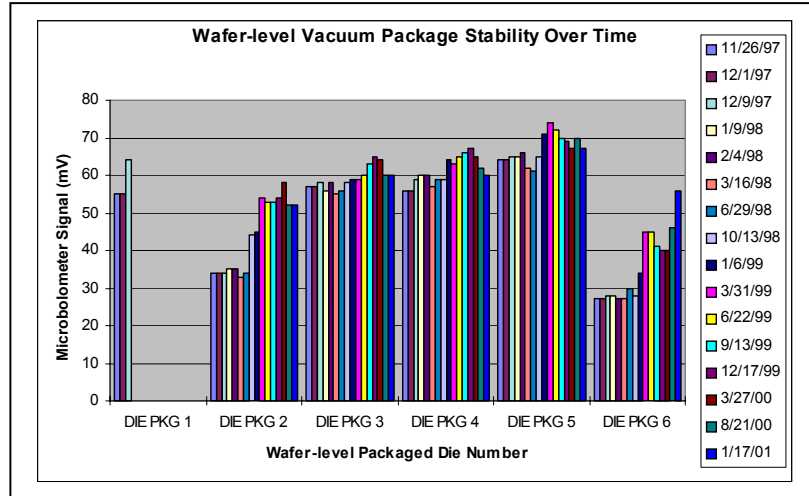


Figure 2.2.2.1 Wafer-level package stability results over 38 month period.

2.2.3. IR MEMS Microbolometer 4" and 6" Wafer-level Packaging Demonstration

Following the successful completion of the proof-of-concept 1" wafer-level IR MEMS microbolometer vacuum packaging, 4" wafer-level packaging was demonstrated. A 4" IR MEMS microbolometer wafer and seal ring architecture is shown in Figure 2.2.3.1. The seal ring geometry was identical to the 1" wafer-level process described in 2.2.1. The gold seal ring is 0.035" wide. The AuSn solder preform was 0.030" wide and 2 mils thick. The interconnects are electrically isolated from the seal ring by an $\sim 3500\text{\AA}$ insulating SiN layer deposited over the gold seal ring. In the seal process, the AuSn preform was placed on the lid wafer and the IR MEMS microbolometer wafer was placed upside down aligned with the lid wafer seal ring. An approximately 0.25" aluminum plate was placed over the inverted MEMS wafer to provide additional weight during the seal process. In the case of IR MEMS microbolometer packaging, the AR-coated Si lid thickness was no more than 0.025" to minimize IR absorption in the lid material.

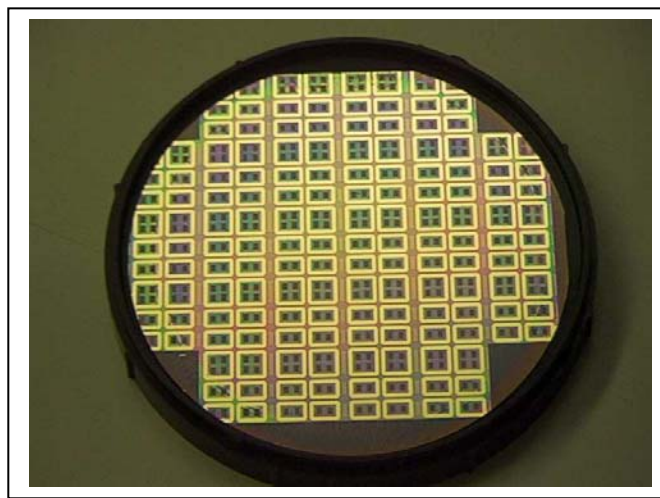


Figure 2.2.3.1 4" wafer-level packageable IR MEMS microbolometer wafer.

The results of the 4" demonstration are shown in Figures 2.2.3.2 and 2.2.3.3. The results in Figure 2.2.3.2 show the microbolometer signal voltage for 32 sealed die measured over the 4" wafer. Of the 32 die, 25 produced a microbolometer voltage output, indicating a successful vacuum seal. The 7 die with no microbolometer output did not seal. Hence, a seal yield of 78% over the 4" wafer was achieved in this demonstration.

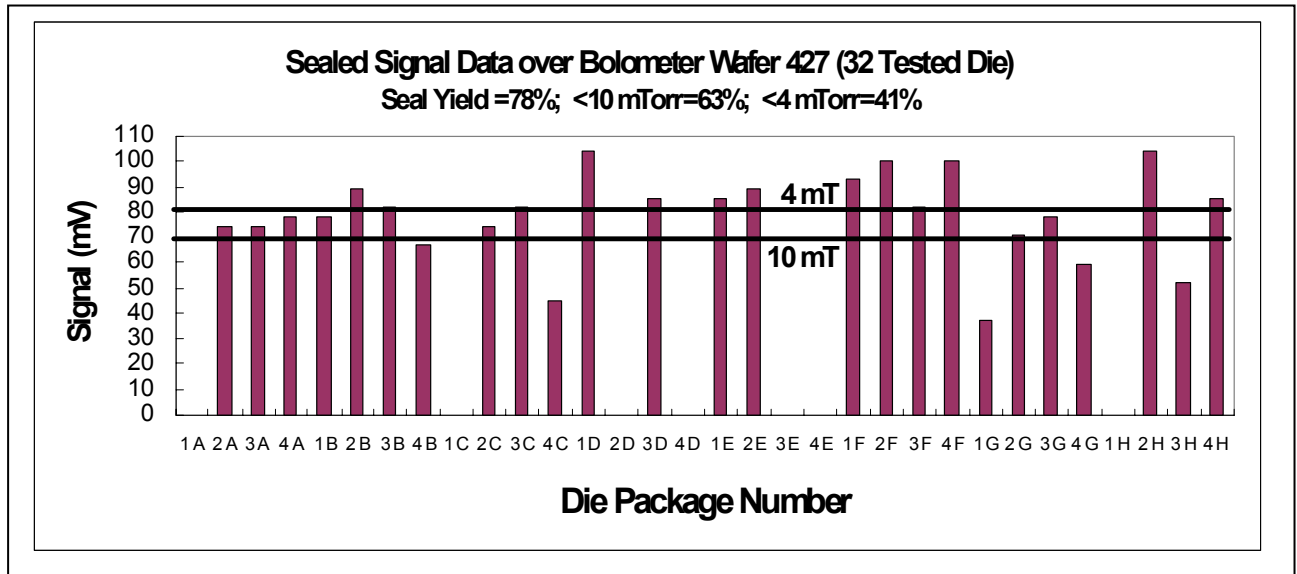


Figure 2.2.3.2 4" wafer-level vacuum package results from IR MEMS microbolometer wafer 427

Quantitative package vacuum data was obtained by drilling a hole in two packages, 427-2B and 427-3C, and placing them in a vacuum Dewar, to obtain the signal versus vacuum calibration curves shown in Figure 2.2.3.3. The calibration curve for package 2B in Figure 2.2.3.3a indicates a vacuum level of 4 mTorr for a signal level of 82 mV. The calibration curve for package 3C in Figure 2.2.3.3b indicates a vacuum level of 10 mTorr for a signal level of 68 mV. Assuming these calibration curves are representative for the packaged die over the 4" wafer, lines at 82 mV and 68 mV, indicating 4mTorr and 10 mTorr, respectively, have been placed in Figure 2.2.3.2. These lines show that out of the 32 tested packages, approximately 63% of the packages across the wafer sealed with vacuum ≤ 10 mTorr and 41% sealed with vacuum below ≤ 4 mTorr. With this demonstration, the 4" IR MEMS wafer-level vacuum package milestone was achieved.

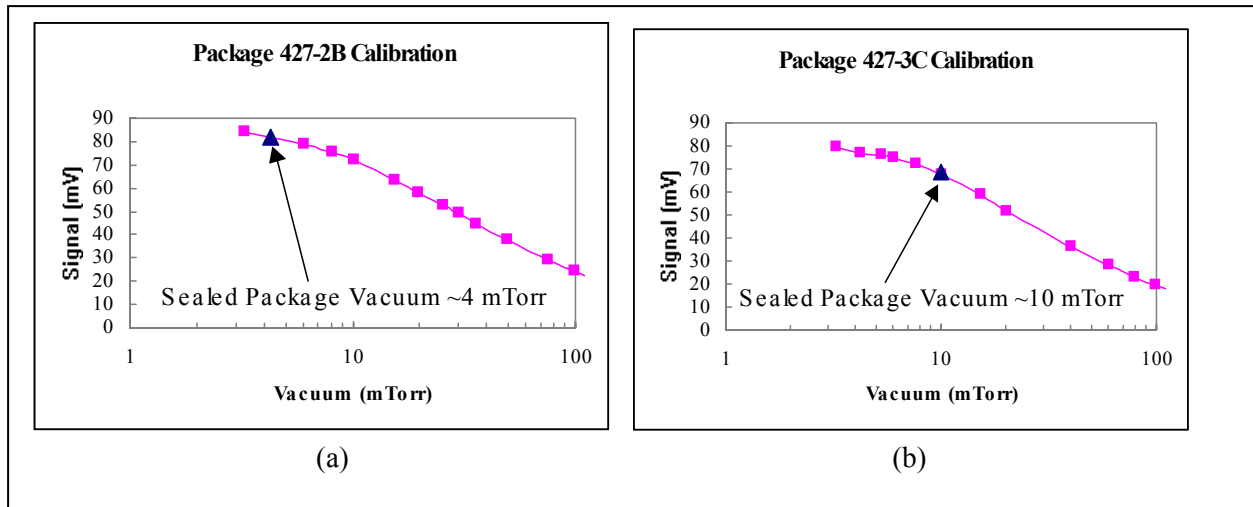


Figure 2.2.3.3 Microbolometer signal versus vacuum calibration curves for a) package 427-2B (4 mTorr sealed vacuum) and b) package 427-3C (10 mTorr sealed vacuum).

The 4" wafer-level packaging was subsequently upgraded to accommodate 6" wafers. The IR MEMS microbolometer wafer used in the 6" wafer-level package demonstration is shown in Figure 2.2.3.4. The 6" wafer is mounted on a 0.25" thick tooling plate that also shows two self-alignment pins used to align the microbolometer wafer to the lid wafer.

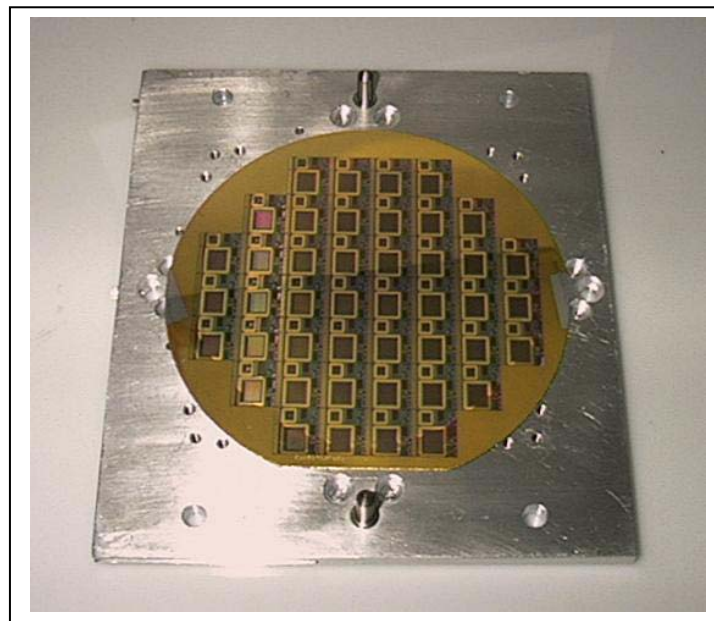


Figure 2.2.3.4 IR MEMS microbolometer wafer used in the 6" wafer-level package demonstration mounted on a 0.25" tooling plate.

2.2.4. Inertial MEMS 1" and 6" Wafer-level Vacuum Packaging Demonstration

As with the IR MEMS microbolometer, the initial wafer-level Inertial MEMS package demonstration was carried out using a 1" wafer-level packaging solder process. The UC Berkeley-designed (see Section 2.5.5)/Sandia-fabricated (see Section 2.6) chip-level packaged Inertial MEMS chip containing resonant accelerometer, gyroscope and microresonator structures is shown in Figure 2.2.4.1. Following seal, UC Berkeley demonstrated functionality of the resonant accelerometer and microresonator structures. In addition, using pull-down structures in the package, a vacuum level of less than 100 mTorr was verified meeting the sub 200 mTorr Inertial MEMS package vacuum requirement.

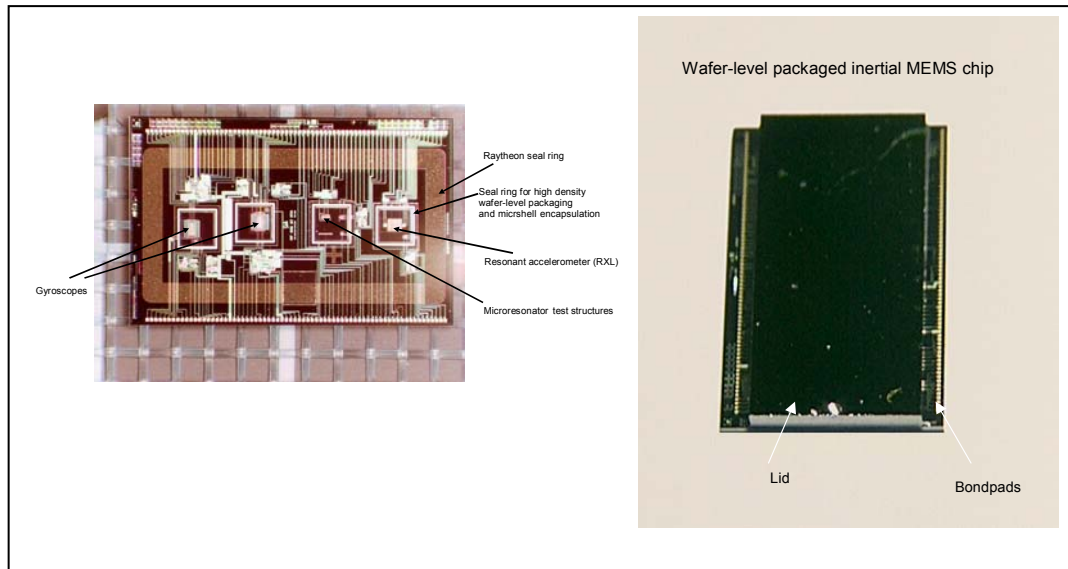


Figure 2.2.4.1 1" wafer-level packaged Inertial MEMS chip.

Raytheon subsequently carried out a wafer-level Inertial MEMS packaging demonstration using the upgraded 6" wafer-level packaging tooling. This upgrade was necessary to be compatible with the 6" wafers Sandia delivered for the final inertial MEMS wafer-level packaging demonstration under the program. Because of tooling limitations at Sandia, the 6" wafers were sawn into quarters to carry out the IMEMS release process and critical drying steps. Three quarters of a 6" Inertial MEMS wafer after the release and drying process are shown mounted on the 6" wafer tooling in Figure 2.2.4.2. A total of 12 Inertial MEMS packages sealed and sawn from a quarter wafer using the 6" wafer tooling are shown in Figure 2.2.4.3a. A close-up of a single package with bond pads, which were opened in the sawing process, is shown in Figure 2.2.4.3b.

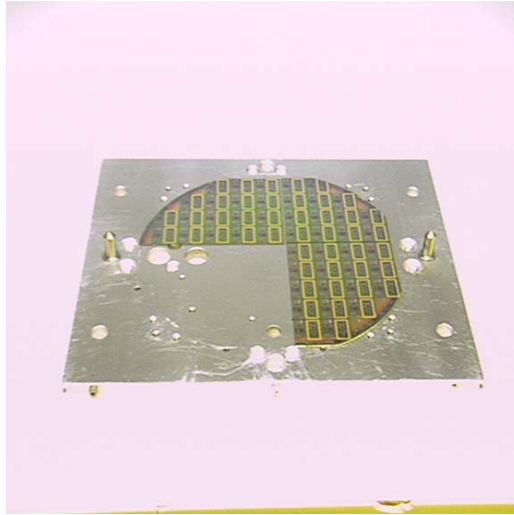


Figure 2.2.4.2 Three quarters of 6" Inertial MEMS wafer mounted on the 6" wafer tooling.

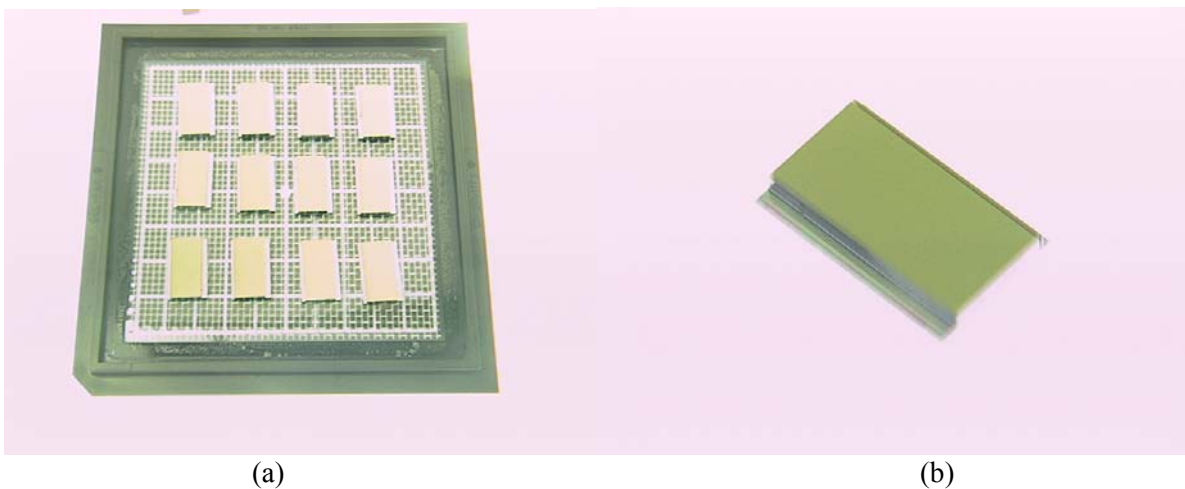


Figure 2.2.4.3 a) 12 Inertial MEMS packages sealed using 6" wafer tooling, b) Close-up of sealed Inertial MEMS package.

2.2.5. System Insertion of Wafer-level Vacuum Packaging into an Uncooled a-Si 120x160 Micro IR Camera

The development of wafer-level vacuum packaging under this program enabled the proof-of-concept demonstration of the low cost, low power uncooled a-Si micro IR camera shown in Figure 2.2.5.1. The a-Si micro IR camera demonstrations were carried out under the DARPA ANTS and FIS Programs, leveraging the wafer-level packaging developed under this program.

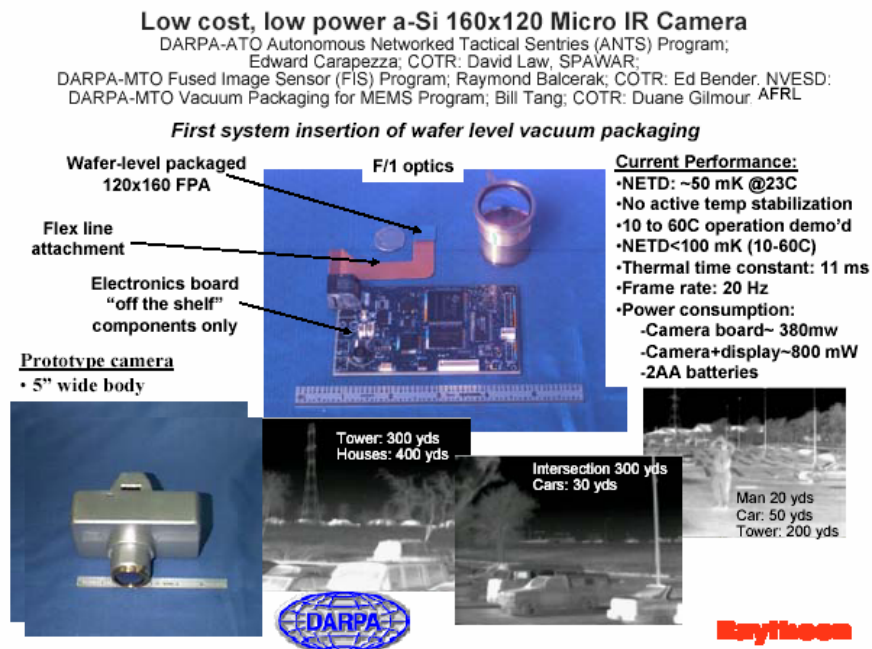


Figure 2.2.5.1 a-Si 120x160 micro IR camera employing a wafer-level vacuum packaged focal plane array.

2.3 MIL Standard Testing of MEMS Vacuum Packages (Raytheon/AFRL)

Under the program, environmental testing of Inertial MEMS and IR MEMS bolometer ceramic vacuum packages and IR MEMS wafer-level vacuum packages were carried out at the Air Force Research Laboratory, Rome, NY. A summary of the environmental testing is shown in Figure 2.3.1. The temperature and humidity related test results are shown in Figure 2.3.2. The vibration test results will be discussed later, (See Figure 2.3.4.). In addition, high g shock testing was performed by the Army Research Lab, Aberdeen Proving Ground, MD.

MIL Standard Test	First Iteration	Second Iteration	Third Iteration
1. High Temperature Storage- MIL-STD-883, Test Method 1008 (150°C, 1000 hours)	100 hours	250 hours	650 hours
2. Temperature Cycling- MIL-STD-883, Test Method 1010 (-65°C-150°C, 1000 cycles)	100 cycles	250 cycles	650 cycles
3. Random Vibration- MIL-STD-883, Test Method 2026 (9 g _{rms} for 1 hour)	1 hour		
4. Accelerated Temperature/Humidity Test (130°C/85%RH- 150 hours)	25 hours	50 hours	75 hours
5. Temperature/Humidity Test (85°C/85%RH- 1000 hours)	100 hours	250 hours	650 hours

Figure 2.3.1 Environmental test summary.

A total of 14 ceramic and wafer-level vacuum packages sealed using a high temperature AuSn (283°C) solder seal were subjected to a minimum of 1000 hours at 150°C. Twelve of the 14 packages including 6 wafer-level packages maintained <10 mTorr vacuum with no signal degradation. Of the two packages suffering failures, both were 16 pin Cerdip. One 16 pin Cerdip developed a vacuum failure after 100 hrs and another 16 pin Cerdip developed an electrical failure after 100 hours.

Test	Package #	Package Type	Total Hrs/Cycles	Comments
High Temp Storage (150C, 1000 Hrs) -High Temp AuSn Solder (283C)	593 (IR)	84 pin ceramic	1500	Passed
	595 (IR)	84 pin ceramic	1500	Passed
	580 (IR)	84 pin ceramic	1000	Passed
	449 (IR)	16 pin Cerdip	900	Passed
	A9 (inertial)	16 pin Cerdip	1000	Passed
	626 (IR imaging array)	16 pin Cerdip	1500	Passed
	625 (IR imaging array)	16 pin Cerdip	100	Vacuum failure @100hrs
	539 (IR imaging array)	16 pin Cerdip	100	Electrical failure @100 hrs
	<u>WLVP-1 (6 IR die pkgs)</u>	wafer-level	1000	Passed
	14 packages (total)			(<10 mTorr vacuum)
Modified High Temp Storage (120C, 1000 Hrs) -Low Temp In Solder (<156C)	<u>WLVP-3 (6 IR die pkgs)</u>	Wafer-level	1000	Passed (4 of 6 pkgs survived 1500 hrs) (<100 mTorr vacuum) -can't maintain <10 mTorr
Temp Cycling (-65C-150C, 1000 Cycles) -high temp AuSn solder -low temp In solder	582 (IR)	84 pin ceramic	1000	Passed (35% signal drop)
	69 (IR)	16 pin Cerdip	1000	Developed open @100 cyc
	A10 (inertial)	16 pin Cerdip	1000	Passed
	529 (IR imaging array)	16 pin Cerdip	1000	Passed
	WLVP-2 (2 IR die pkgs)	wafer-level	1000	1 fail 1000 cy; 1 fail 350cy
	<u>WLVP-2 (2 IR die pkgs)</u>	wafer-level	1000	67-73% signal drop/ Vacuum >10 mTorr
Accelerated High Temp/High Humidity (130C/85%RH, 150 Hrs)	593 (IR)	84 pin ceramic	150	Passed
	595 (IR)	84 pin ceramic	150	Passed
	626 (IR imaging array)	16 pin Cerdip	150	Passed
	<u>WLVP-6 (2 IR die pkgs)</u>	wafer-level	150	27-32% signal drop
	5 packages (total)			
High Temp/High Humidity (85C/85%RH, 1000 Hrs)	WLVP-5 (2 IR die pkgs)	Wafer-level	1000	Passed
Note: Packages 593 , 595 , 626 have survived 1500 Hrs @150C and 150 Hrs @130C/85%RH with no vacuum degradation				

Figure 2.3.2 Summary of environmental test results.

A modified high temperature storage test (1000 hrs @120°C) was carried out on 6 IR MEMS microbolometer wafer-level vacuum packages sealed with low temperature Indium (156°C) solder. The results show 50-70% microbolometer signal degradation in the 6 wafer-level packages. The signal degradation is due to a drop in package vacuum over the 1000 hr test. This is shown in Figure 2.3.3 which compares package vacuum results for the high temperature AuSn solder and low temperature Indium solder packages. In the case of the AuSn solder package, the package vacuum remained <10 mTorr throughout the 1000 hr bake test. In contrast, in the Indium solder package, the package degraded from ~ 11 mTorr after seal to ~61 mTorr after 1000 hrs bake at 120°C. An Indium solder package bake was further extended another 500 hrs for a total of 1500 hrs and the pressure increased to 67 mTorr. The explanation for these results is the high temperature AuSn solder seal cycle allows for an extended high temperature vacuum bake prior to seal at 283°C which provides sufficient outgassing to maintain sub 10 mTorr package vacuum during the high temperature bake stability test. In contrast, in the low temperature Indium solder seal cycle, the vacuum bake prior to seal is carried out below 156°C.

The lower temperature vacuum bake results in insufficient outgassing of the package prior to seal. As a result, the package vacuum degrades during the bake stability test. From these tests we conclude that the high temperature AuSn solder is necessary for IR MEMS packaging which requires sub 10 mTorr package vacuum. However, the low temp Indium solder may find application in Inertial MEMS packaging due to the less demanding ~200 mTorr vacuum requirement. As such, in some cases the low temperature solder which exhibited sub 100 mTorr vacuum after the high temperature bake may be useable for some inertial MEMS vacuum packaging applications.

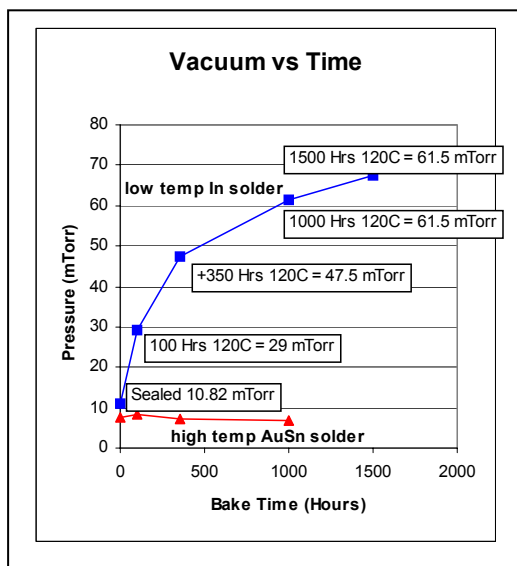


Figure 2.3.3 Comparison of package vacuum versus bake time for high temp AuSn and low temp Indium solder wafer-level vacuum packages.

Ceramic and wafer-level vacuum packages were also subjected to temperature cycling (-65°C to 150°C, 10 packages), accelerated high temp/high humidity (130°C/85%RH, 5 packages) and high temp/high humidity (85°C/85%RH, 2 packages). In the case of the high temp/high humidity tests, five of the seven packages maintained vacuum with no drop in IR MEMS bolometer signal. Two packages suffered a 27-32% drop in signal. The temperature cycling appears the most demanding test with three of the ten packages developing hard vacuum failures. Two packages maintained vacuum with no degradation in IR MEMS bolometer signal. Failures in the temperature cycling tests are likely due to mechanical stresses induced during temperature cycling that caused solder bond failures resulting in hard vacuum failures.

The random vibration test results carried out by AFRL are shown in Figure 2.3.4. A total of 12 wafer-level IR bolometer packages were subjected to random 9 g_{rms} vibration testing for 1 hour. 8 of the 12 packages survived the test. Three of the packages that failed exhibited mechanical damage. This damage was likely sustained in shipping the packages back to Raytheon after the random vibration tests since the packages had loosened from their mountings during shipping.

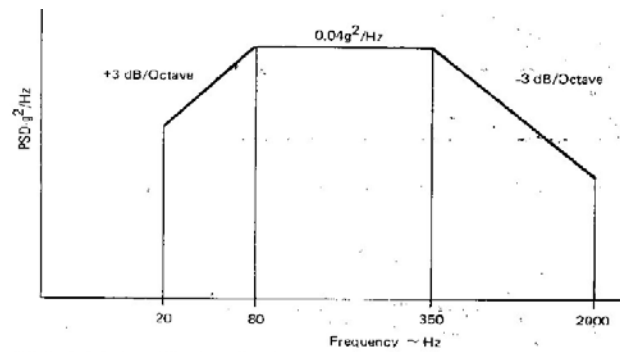


Figure 5. Random Vibration Spectrum



Test	Package #	Package Type	Total Hrs	Comments
Random Vibration (9 g _{rms} for 1 hour)	WLVP-3 (5 IR die pkgs)	wafer-level	1	5 of 5 pkgs passed
	WLVP-1 (5 IR die pkgs)	wafer-level	1	2 of 5 pkgs passed (mechanical damage)
	WLVP-2174 (2 IR die pkgs)	wafer-level	1	1 of 2 pkgs passed (1 package with low signal)
	12 packages total			8 of 12 packages passed

Figure 2.3.4 Random vibration test results from AFRL.

Finally, high g shock testing was carried out at ARL. In these tests, a wafer-level packaged microbolometer array was subjected to the 10,000-g shock profile in Figure 2.3.5. Subsequent microbolometer testing by ARL confirmed the microbolometer packages were operational after the 10,000-g test indicating that the package had survived the test. The significance of this vibration and shock testing is that the IR MEMS microbolometer wafer level packages show a substantial robustness to mechanical vibration and shock. In fact, surviving a 10,000g shock indicates that a wafer-level packaged microbolometer could be used in an application that involves gun-launched deployment of the sensor.

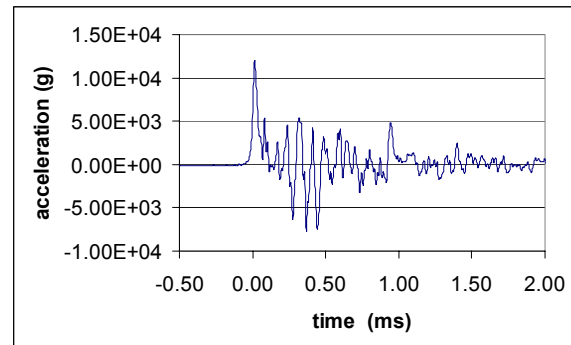
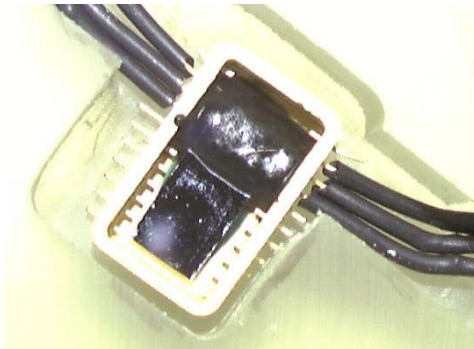


Figure 2.3.5 High 10,000-g shock test results at ARL.

2.4. High Density Wafer-level Vacuum Packaging using Au Thermocompression Bonding (MIT)

The goal of the MIT effort under this program was the demonstration of a high density wafer-level vacuum packaging process using a narrow ($\sim 100\text{ }\mu\text{m}$) gold seal ring and the demonstration of a Au thermo-compression bond protocol. While this demonstration was not fully accomplished, a gold thermo-compression bond protocol for a $100\text{ }\mu\text{m}$ wide seal ring was demonstrated along with a bond strength metrology process. In addition, a high density thru-wafer interconnect technology was demonstrated by personnel supported on other programs. These technologies have important relevance to this program. As such, MIT demonstrated the essential components necessary for a high density wafer-level vacuum packaging process.

2.4.1. Au-Au Thermocompression (TC) Bonding Process Overview

In this process, an approximately $1\text{ }\mu\text{m}$ thick Au layer is deposited and patterned on the surfaces of the two wafers to be bonded (with a barrier metal such as Ti). The wafers are cleaned using UV ozone and aligned together. After alignment, the wafers are heated to 300°C , pressed together, and held for 10 minutes at 0.5MPa of pressure to complete the bond. After an overview of the process development, the details of the process are summarized below.

Development of a wafer-level TC bond

The first effort of this program was to convert what had previously been a die-level TC bond process into one that could be performed at the wafer level. The first step was the acquisition of hardware that enabled aligned wafer bonding. MIT utilized a tool set made by Electronic Visions that includes an aligner and a wafer-bonding chamber. The aligner is used to register the wafers to within approximately $2\text{ }\mu\text{m}$, and the bonder is used to press them into contact and heat them. A wafer holding jig is used to hold and transport the aligned wafer pair from the aligner to the bonder. Four issues were critical in the development of a wafer-level bond: a smooth Au deposition process, a reliable Au patterning process, stable barrier metals, and detailed equipment protocols.

Smooth Au process

Given that the Au films are only $1\text{ }\mu\text{m}$ thick, any protrusions or irregularities in the surface that are of this order in height can compromise the bond quality. The first potential source of such protrusions can be due to a poor deposition process. MIT worked hard to optimize a Au e-beam evaporation process to minimize these effects. Two things are of particular importance in this regard. First, the deposition system must be kept meticulously clean. MIT found it necessary to do a full clean and wipe down of the vacuum chamber prior to deposition to ensure that particulate did not collect on the wafer and to ensure that contaminants did not collect in the Au target. This is especially important in a system where a variety of metal films are deposited. In a production process, it is likely that one would want a dedicated Au deposition system. The second important parameter is the specific deposition recipe. The source heating and soaking prior to deposition is critical to establish an equilibrium of the Au melt. In addition, there is a transient that occurs when the deposition shutter opens. MIT found that if these parameters are not carefully controlled, Au ‘balls’ can deposit on the wafer due to source ‘spitting’ as shown in

Figure 2.4.1.1. Proper ramp and soak recipes can largely eliminate this, but require some iteration to achieve.

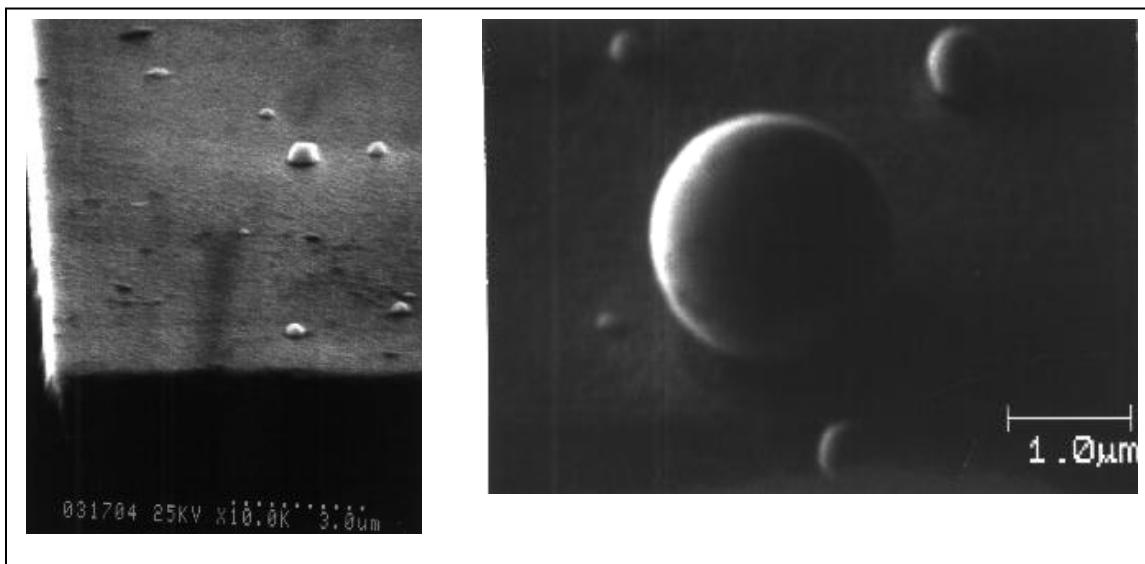


Figure 2.4.1.1 Appearance of Au ‘balls’ on wafer due to source spitting during deposition. The balls can severely compromise the bond quality, and thus careful control of the deposition process is critical.

Reliable Au Patterning

The Au patterning options considered include lift-off and wet etching (MIT did not have a dry etch at its disposal). The wet etch process did not produce good quality narrow lines, so MIT developed a lift-off process using image reversal resist. The most troublesome aspect of lift-off as it relates to TC bonding is the potential to form Au ‘wings’ at the edge of the patterned feature, where the Au partially covers the edge of the resist. This is described in Figure 2.4.1.2. These wings will prevent bonding. MIT found that exposure and develop time for the image reversal resist has the most significant impact on the presence of wings. With an optimized exposure and development process, MIT succeeded in eliminating any problems with Au wings.

Stable barrier metals

MIT used a 10 nm thick Ti layer as a barrier and adhesion metal between the Au and the silicon substrate. MIT found that during the bonding cycle (300°C), it was possible for some amount of barrier metal breakdown to occur as shown in Figure 2.4.1.3. The Au and Ti can begin to interdiffuse, leading to Au coming into contact with the silicon. This leads to silicon diffusing to the surface of the Au and forming an oxide. The result is a significant change in the surface that prevents bonding. This manifests itself as a non-uniform bond, with regions un-bonded over the wafer surface. The 10 nm Ti layer is marginally stable. MIT conducted a study of the influence of barrier metal thickness. The results suggest that thicker barrier metal is better, but does not completely eliminate the effect. MIT found that the most robust solution is to deposit the Ti/Au

layer on approximately 150-300 nm of silicon dioxide. This appears to completely eliminate this problem and results in high quality bonds.

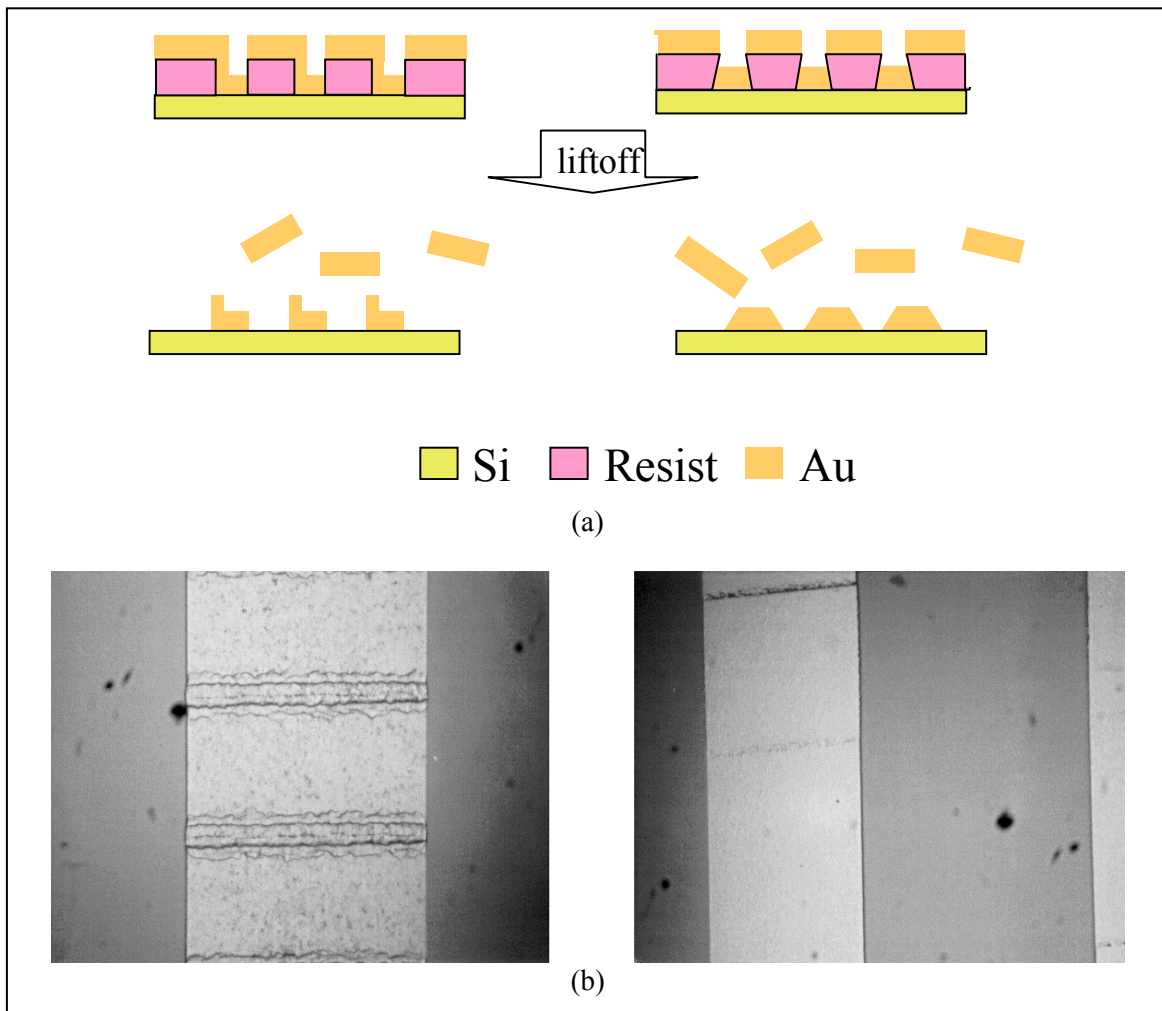


Figure 2.4.1.2 (a) Illustrates the effect of a poor lift-off process that develops 'wings', (b) Photomicrograph of the imprinting of the 'wings' in a crossed structure. The wings preclude strong bonds.

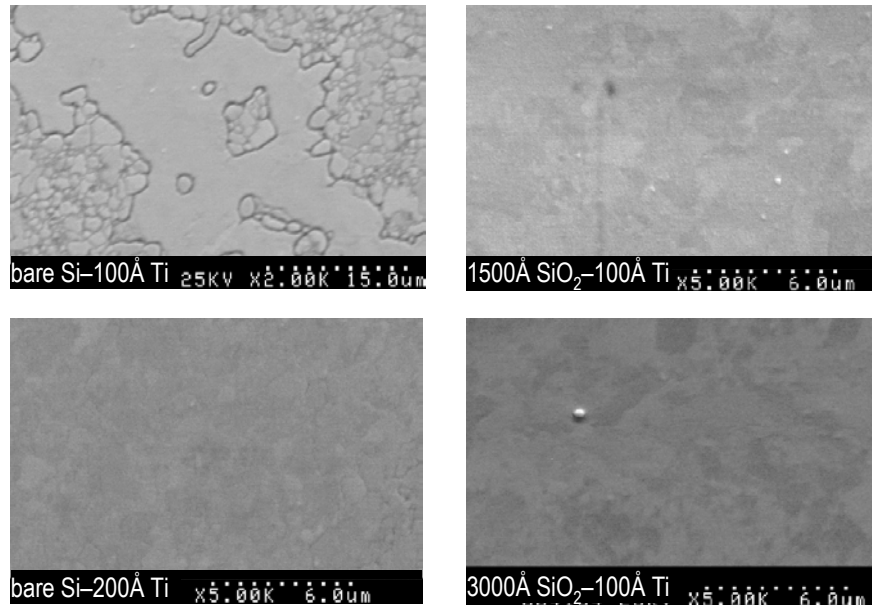


Figure 2.4.1.3 An ensemble of images of Au films deposited with various thicknesses of Ti (10nm, 20nm) and thickness of SiO₂ (150nm, 300nm). The thin Ti without SiO₂ shows reaction of the silicon with the gold.

2.4.2. Detailed Au-Au Thermocompression (TC) Bonding Protocol

The equipment for Au-Au thermocompression bonding has a wide parameter set (specific to the tool) for bonding. The most important parameters are temperature, pressure, bond time, bond ambient, and bond sequence. The bond sequence refers to the specific order in which the wafers are heated, contacted, pressed and then unloaded. MIT now has a detailed protocol that has been optimized over the three year program to give consistent bonding.

Starting wafers:

Each bonding pair consists of 4" n-type Si wafers with average thickness of 525 μm and 450 μm , respectively, the latter being a double-side polished (DSP) wafer.

Process:

- 1) Alignment marks are dry etched into both sides of the DSP wafer using an Applied Materials Precision 5000 Etcher.
- 2) While more detailed description of the testing procedure can be found in the next section, the next sequence of steps describes the fabrication process for forming a KOH etched central trench in the DSP wafer in order to prepare the wafer for mechanical testing. Following thermal oxidation, the wafer is patterned and wet etched in BOE to form the KOH etch mask. The wafer is etched in 20% KOH solution at 80°C to form a 500 μm wide, 60 μm deep trench. The oxide is then stripped and the wafer coated with 5 to 6 μm thick resist. A 100 μm wide feature is next dry etched into the wafer, forming a 1 μm recess around the KOH etched trench. Thin resist tends to recede from the edges of a deep etch. Metal would thus be

- deposited along the perimeter of the trench and connects the metal lines horizontally at the edges of the KOH etched trench. By having a shallow recess around the perimeter, the Au lines remain separated as defined by the design.
- 3) Approximately 300 nm of thermal oxide is grown on both wafers.
 - 4) Next, both wafers were identically patterned with Clariant AZ5214-E image reversal resist. A Karl Suss Model MA-4 Mask Aligner (320 nm contact aligner) is used for the initial exposure. The wafers are then flat baked on a piece of metal in an oven at 120°C for 90s. Following a second exposure, a blanket or flood exposure, the wafers are developed in AZ 422 developer. The initial exposure time was found to be a major factor in determining the slope of the resist profile. A 20s exposure time results in a negatively sloped profile while a 30s exposure produces a nearly 90° slope.
 - 5) Metals are then e-beam deposited onto the wafers. The system is pumped down to mid-to-lower 10^{-6} torr before starting any deposition. The wafers are placed in a lift-off (planar, horizontal) plate, which rotated during the deposition to enhance uniformity. A 10 nm Ti adhesion layer is first deposited, followed by Au deposition, typically 0.5 to 0.7 μm . To prevent Au source spitting, 2-3 min of soak and pre-deposition periods are used, and the deposition rate is slowly ramped from 2 A/s to 5 A/s in the first 100 nm of deposition. The deposition rate is kept constant at 5 A/s for the remainder of the process.
 - 6) The metals are lifted by soaking the wafers in acetone. While metals begin to lift in minutes, wafers were often left to soak overnight. The wafers are then ultrasonically agitated for a minute, to ensure the complete removal of metals and resist.
 - 7) The wafers are then exposed to UV-Ozone for 90 min for the organics removal immediately prior to aligned bonding.
 - 8) The wafers are aligned using an Electronic Visions EV450 aligner. Three triangular separators, about 100 μm thick and 1 cm long, are inserted between the wafers at the edges to maintain a vertical separation between wafers until bonding.
 - 9) Bonding is done using an Electronic Visions AB1-PV Bonder. The chamber is purged twice with nitrogen before heating began. Following the temperature ramp and the 3-minute stabilization period at 300°C, 0.02 MPa pressure is applied over the wafer and the separators are withdrawn. A bonding pressure of 0.5 MPa is then applied across the wafer (corresponding to 7 MPa of pressure on the Au with the line-patterns that were used), for 10 minutes. The temperature is subsequently ramped down.
 - 10) The mechanical testing specimens are made by dicing the bonded wafers into 8mm wide strips. In addition, a width-wise cut is made above the KOH-etched notch to the DSP wafer, exposing the bonded interface, thereby forming the notch required for the mechanical testing procedure.

Figure 2.4.2.1 illustrates schematically the process described above.

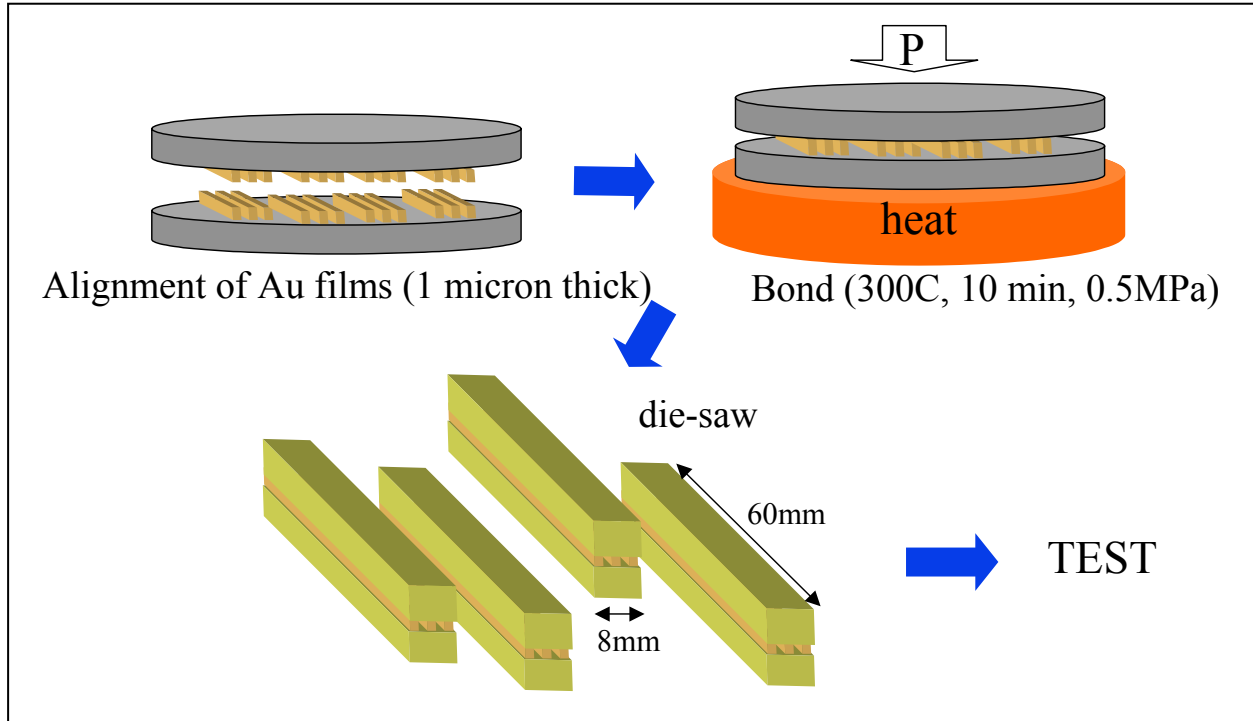


Figure 2.4.2.1 The Au-Au thermocompression bonding process.

2.4.3. Development of Bond Metrology

MIT focused a large amount of attention on developing new bond strength measurement techniques. MIT intended to address two limitations of conventional strength measurements including poor resolution; and inability to measure pattern-dependent bond strength. In addition, MIT demonstrated the use of IR imaging methods as a gross-level *in-situ* monitor of the bond quality.

The bond strength method MIT developed is commonly used in composites research, but prior to this had never been used for wafer bonding. The procedure involved creating a pre-crack in a bonded sample and then loading the sample in a 4-pt bending jig. The deflection of the sample is measured versus the load. When the sample begins to crack, the load reaches a plateau. This load is recorded and can be linearly related to the debond energy. This is in contrast to so-called ‘knife-edge’ techniques in which the debond energy is 4th power dependent on the measured crack length. The net result is much less noisy data, and better resolution on subtle bond variations. Four major activities were needed to establish this bond strength method: sample preparation protocol; pre-crack definition; loading and visualization hardware; and a data analysis method including a calibration standard.

The sample preparation protocol has now been fully refined and is described in Figure 2.4.3.1. Wafers are patterned with lines and spaces of Au, a pre-crack notch is formed, and the wafers are bonded. After bonding, the wafer is die-sawed into strips. These strips are loaded into a 4-pt bending fixture, which can be subsequently loaded into a commercial tensile testing tool

(Instron) for loading. The optimal pre-cracking method required considerable iteration. In the end, a method for creating a photolithographically defined unbonded region was implemented. The die saw is used to cut through one wafer to the unbonded region, thus completing the pre-crack. This method gave consistent loading characteristics in the Instron tool. The commercial tester had to be modified for testing of the wafer-bonded samples. First, a small load cell was used due to the comparatively low loads necessary to fracture these samples. Second, a visualization system was implemented that permitted monitoring and measuring the crack in real time. This measurement greatly increases the confidence in the data. Finally, the data analysis required the fabrication of silicon fusion bonded calibration standards which have pre-defined crack lengths. This calibration was essential to the rational analysis of the Au-Au TC bond samples.

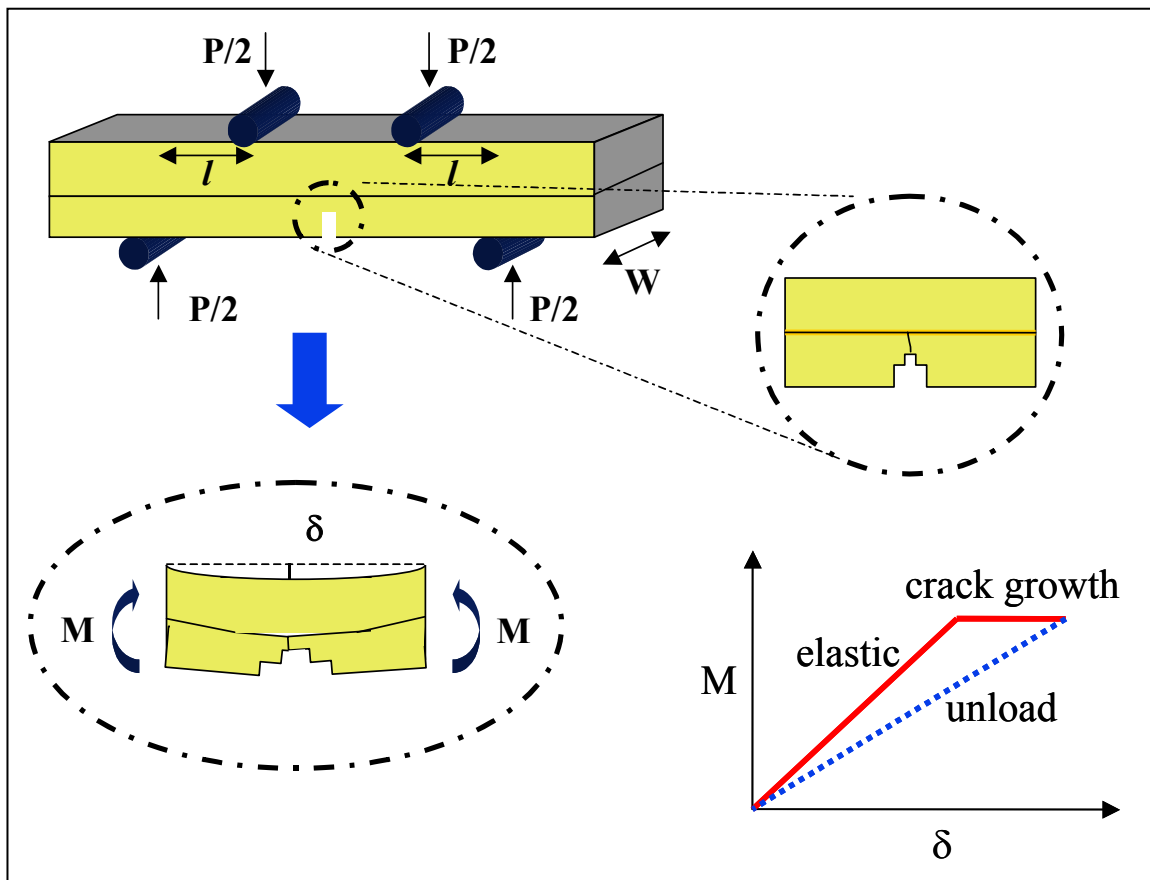


Figure 2.4.3.1 An illustration of the bond strength technique.

The four-point bend delamination technique that was used allows quantification of the resultant bond toughness. As implied by its name, the specimen was loaded at four points, two rollers above and two below the specimen, symmetric about the vertical axis of the specimen. In the region in between the inner rollers, a constant moment condition is maintained. This allows the extraction of a critical strain energy release rate, given by the equation¹:

¹ P. G. Charalambides, J. Lund, A. G. Evans, and R. M. McMeeking, "A test specimen for determining the fracture resistance of bimaterial interfaces," *J. Appl. Mech.*, vol. 56, pp. 77-82, 1989.

$$G_c = \frac{1.5(1-\nu^2)}{E} \left(\frac{P_c l}{b} \right)^2 \left(\frac{1}{h_2^3} - \frac{1}{(h_1 + h_2)^3} \right)$$

where E is the Young's modulus, ν is the Poisson's ratio, P_c is the critical load at which crack propagation occurs, l is the distance between the upper and lower rollers, b is the width of the specimen, and h_1 and h_2 are the thickness of the regular wafer (un-notched) and DSP (notched) wafer, respectively.

Mechanical tests were performed using a servo-hydraulic mechanical testing machine in its displacement-controlled mode at a rate of 0.15 mm/min. The specimen rested on the outer rollers, which sat on a fixture that was rigidly attached to the upward moving crosshead. The inner rollers were attached to the stationary portion of the testing machine via an adjustable grip. The adjustable grip improved the positional leveling of the top apparatus. The alignment of the apparatus was checked immediately prior to testing with strain gauges located below the inner rollers. A 100 N load cell was used to monitor the load. Load and cross-head displacement data were captured by a LabVIEW program while real-time observations of the specimen were made with a Questar long working distance microscope.

An example of measured bond strength for two representative wafers is shown in Figure 2.4.3.2. Samples with differing line widths were measured on each wafer. These samples highlight a significant variation in bond strength for two nominally similar samples. The result of the variation was a difference in failure mode. The lower bond strength was recorded on a sample where the failure occurred at the Ti/Au interface, whereas the higher strength was recorded on a sample that failed in the Au. This demonstrates that the high resolution of the measurement enables resolution of subtle process variations that impact bond strength. This level of strength variation would not be resolvable to this degree by other techniques.

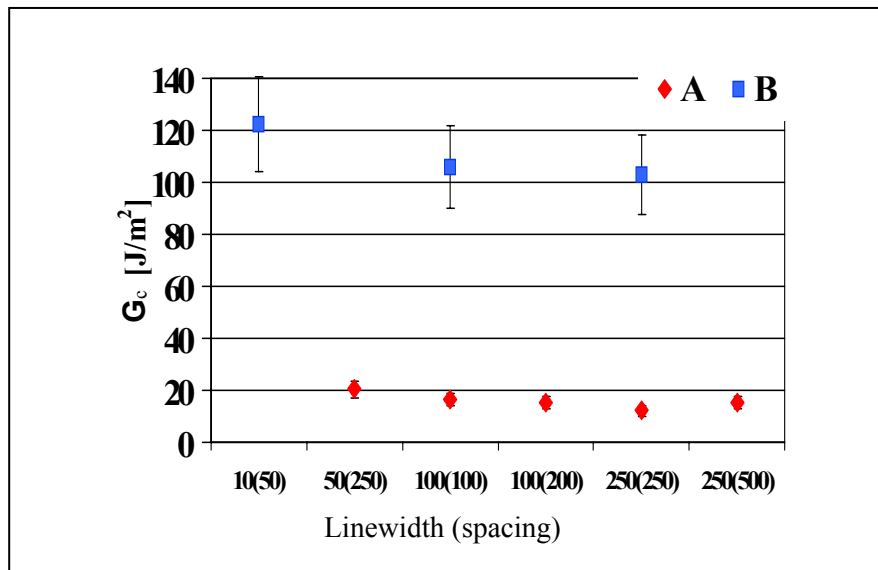


Figure 2.4.3.2 Measured strength on two identically processed samples. The weaker bond was a result of a Ti/Au failure, which highlights a process variation.

2.4.4. Thru-wafer Vias

An important part of the overall wafer-level vacuum packaging process is the demonstration of a lead transfer method. In this respect, MIT developed a novel thru-wafer high-density interconnect via process that utilizes DRIE and is completely compatible with the Au-Au TC bond process which offers easy integration with the TC bond, and low parasitic capacitance. The process for forming the thru-wafer interconnect is shown in Figure 2.4.4.1. First, a circular trench is etched in a silicon wafer. The width of the trench is set to be less than 2x the thickness of an insulator (e.g. silicon dioxide) that is later deposited. The depth is set to 10-20 μm . This depth is determined by a trade-off in mechanical strength of the via, and process limits. An electrical insulator is next deposited. In our implementation, the preferred insulator is silicon dioxide deposited in a plasma deposition system using a TEOS recipe. The insulator thickness in this case is approximately 5-15 microns, and the trench width is less than 10-30 microns. Following the deposition, a via is opened in the insulator to make contact to the substrate. A conductor (polysilicon or metal) is next deposited to serve as a lateral interconnect layer. Lastly, a DRIE process is performed which etches down to the bottom of the insulating trench. This DRIE step electrically isolates the via from the surrounding substrate. SEM images of a via are shown in Figure 2.4.4.2.

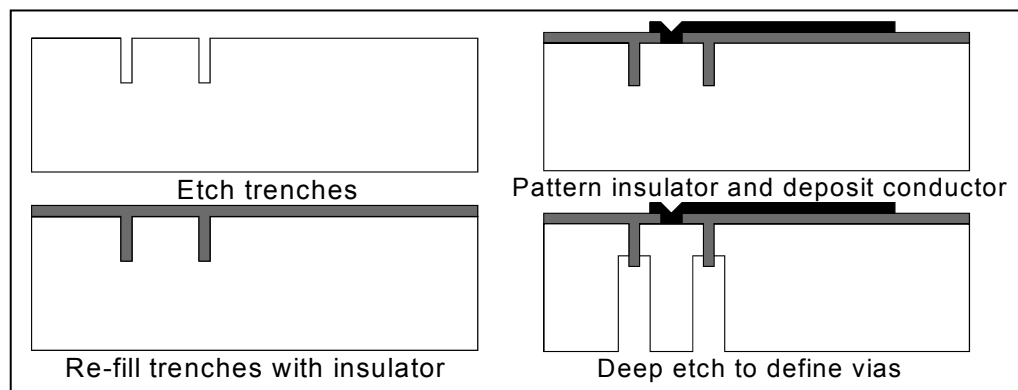


Figure 2.4.4.1 Thru-wafer interconnect process.

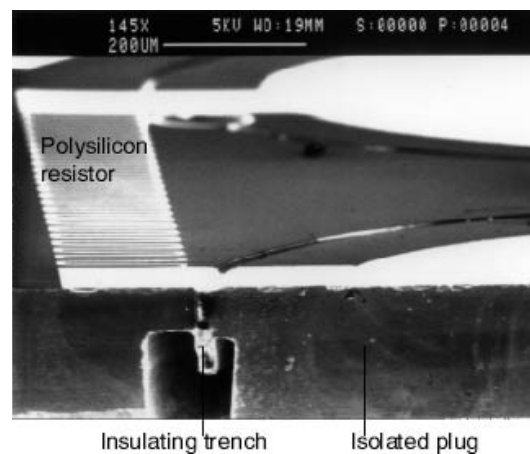


Figure 2.4.4.2 SEM Images of a via.

2.4.5. Vacuum Bonding

A preliminary measurement of vacuum bonding was attempted prior to the contract end. Two wafers were bonded under vacuum conditions. One wafer had been processed to form a cavity with a thin membrane. The downward deflection of the membrane was measured to determine the vacuum level. The measurement resolution was 0.15 atm. The vacuum level was measured to be below this limit.

2.4.6. Future Work

The goal of the MIT effort under this program was to demonstrate wafer-level vacuum sealing using the TC bond protocol. Under the program, MIT achieved reliable TC bonding but did not fully demonstrate vacuum capability. However, MIT accomplished more than expected in developing a unique bond strength measurement protocol that is important for a wide range of bond strength measurements. Also, this method can be implemented in a production environment, much like test patterns in IC processes. This should be important in volume manufacturing of MEMS parts. Lastly, the TC bond developed is now reliable and robust, and can be used in a wide range of MEMS packages, particularly with the incorporation of the high density thru-wafer vias. An area for future work is the implementation of the TC bond protocol together with the high density thru-wafer vias to complete a high density wafer-level vacuum packaging demonstration.

2.5. Wafer-Wafer Transfer Microcap Vacuum Encapsulation (UC Berkeley)

The UC Berkeley effort on this program focused on the development of wafer-wafer transfer microcap vacuum encapsulation, first using polysilicon and then SiGe microcaps for ultra low cost, high density vacuum packaging of resonant accelerometers, gyroscopes and microresonator structures. To support this effort, UC Berkeley also carried out under this program the design and layout of wafer-level vacuum packageable inertial MEMS resonant accelerometers gyroscopes and microresonators. These wafer-level packageable inertial MEMS devices were fabricated under the program by Sandia National Laboratories using the Sandia IMEMS process (Section 2.6).

2.5.1. Hexsil Vacuum Microcaps

One of the UC Berkeley goals under the program involved the demonstration of a wafer-wafer transfer microshell vacuum encapsulation process. The approach to microshell packaging carried out by UC Berkeley involved the transfer of surface-micromachined caps or microcaps from a “donor” wafer to the MEMS wafer. The main advantage of using a transferred microcap packaging process is that very precise tolerances can be achieved that allow for very small seal ring areas for ultra low cost, high density packaging applications.

Polysilicon Microcaps

The first Berkeley vacuum microshell concept pursued under this program involved the fabrication of polysilicon microcaps. In this approach, a surface-micromachined polysilicon cap was fabricated on a “donor” wafer, released, and then transferred to a “target” wafer that contained the MEMS microdevices to be packaged. Break-away tethers were employed to affix the microcap to the donor wafer prior to transfer. The cap can also employ hexsil stiffening ribs to have sufficient rigidity to avoid collapsing under the pressure of an atmosphere. A schematic of the transferred hexsil cap process is shown in Figure 2.5.1.1.

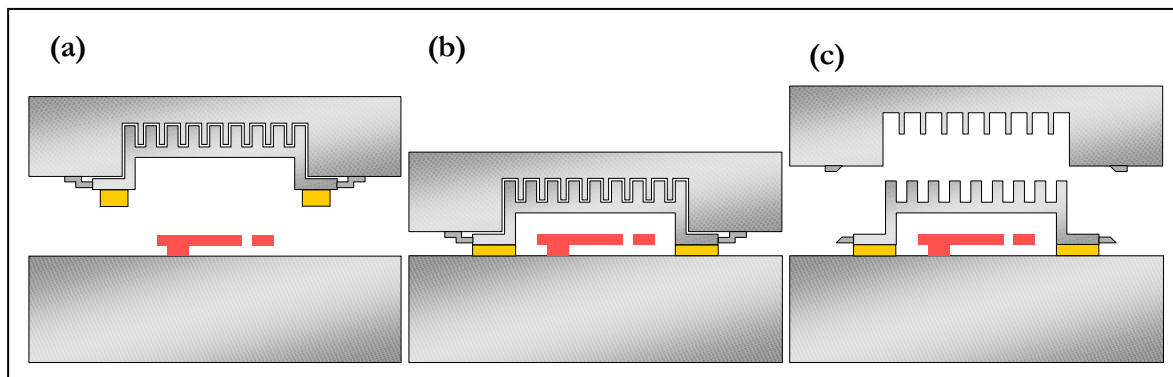


Figure 2.5.1.1 Schematic of hexsil cap transfer (a) Hexsil cap is fabricated on a “donor” wafer, and is aligned with MEMS wafer, (b) The two wafers are brought together and bonded, (c) The wafers are separated, the tethers holding the cap to the donor break, and the hexsil cap is transferred to the target.

In the polysilicon hexsil vacuum cap process carried out in the first year of this program, the hexsil cap was fabricated in a conventional hexsil process using a polysilicon structural layer and a silicon dioxide sacrificial layer. In the first year of the program UC Berkeley demonstrated the fabrication of polysilicon microcaps and the subsequent non-vacuum transfer from a donor wafer to a MEMS resonator chip wafer using gold bump compression bonding. In this demonstration, the microcaps were made of a single layer of 2 μm polysilicon. The gold bumps, which were electroplated to a height of 5-7 μm , also acted as tethers for securing the cap to the donor chip wafer prior to transfer. The microcaps were fabricated on the donor wafer with a sacrificial oxide layer between the donor and the microcap. Completion of the microcap fabrication process involved etching the sacrificial oxide layer in HF leaving the released polysilicon microcap tethered to the donor wafer by gold bump tethers.

In the microcap transfer process, the donor and MEMS chip wafers were aligned using a chip-scale flip-chip aligner and bonder. In the transfer process, the gold bumps are adhered to thin gold pads on the MEMS resonator chip by using gold compression bonding. The gold compression bonding, which requires about 500 pounds of force for a 0.5 cm^2 chip area, was performed immediately after aligning the donor and MEMS chip wafers. The gold bumps tended to compress to approximately half their original height and securely fix the cap to the MEMS chip. The two chip wafers were then separated by breaking the gold tethers, leaving the cap affixed to the MEMS chip. In this polysilicon microcap transfer demonstration, 100% yield in microcap transfer (20 out of 20 resonator microcaps) was achieved for microcaps with lateral dimensions of less than 500 μm . The larger microcaps only partially transferred. A partially transferred large cap bonded to gold pads on a MEMS resonator chip is shown in Figure 2.5.1.2.

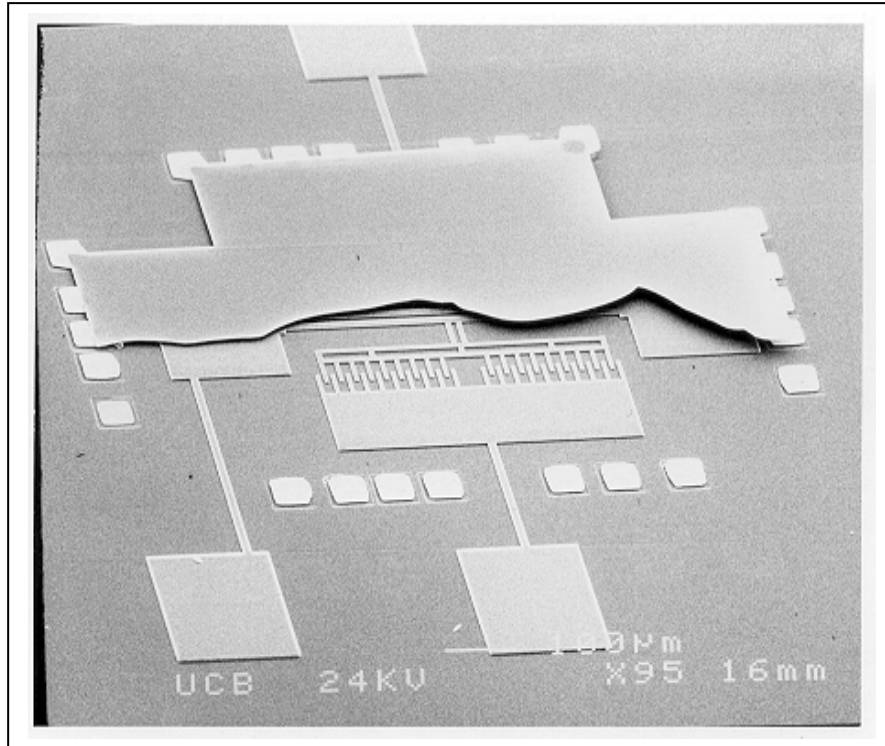


Figure 2.5.1.2 Partially transferred polysilicon microcap over large MEMS resonator device.

SiGe Microcaps

During the first year of the program it became apparent that the fabrication of high-aspect-ratio hexsil structures would be much easier using poly-SiGe that was in rapid development at UC Berkeley as a structural material for MEMS. In the SiGe process, the structural layer is silicon or a silicon-rich SiGe. The sacrificial layer is a germanium or germanium-rich SiGe. The advantages of SiGe over polysilicon/SiO₂ are:

- Only one furnace step is necessary for depositing both the sacrificial germanium layer and the structural silicon layer;
- The germanium layer is etched in RCA-1 cleaning solution (NH₄OH:H₂O₂:H₂O 1:1:5) or 30% H₂O₂:H₂O with etch selectivity to both polysilicon or oxide. In contrast, the polysilicon/SiO₂ involved more aggressive and dangerous HF to etch the SiO₂ sacrificial layer;
- Both Si-rich and Ge-rich layers deposit conformally, eliminating problems with non-conformal oxide in the polysilicon/SiO₂ process;
- High deposition rate;
- Low deposition temperature;
- Low as-deposited stress and stress gradient.

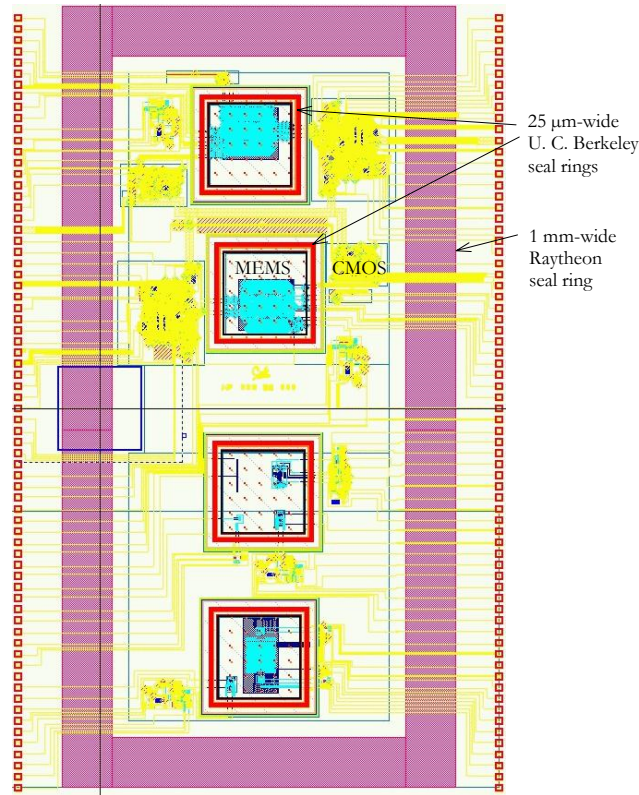


Figure 2.5.1.3 Layout of Sandia multi-purpose IMEMS chip showing seal ring targets for UC Berkeley and Raytheon vacuum packaging efforts.

On this program poly SiGe hexsil vacuum microcap development was carried out for the packaging of UC Berkeley designed, Sandia fabricated resonant MEMS accelerometers, gyroscopes, high-frequency resonators, and vacuum gauges, all of which require vacuum packaging. The Sandia IMEMS process is discussed further in Section 2.6. The Sandia IMEMS chip is shown in Figure 2.5.1.3. The layout shows the various IMEMS accelerometer, gyroscope and microresonator structures surrounded by a 25 μm seal ring that was used by UC Berkeley in the vacuum microcap development. In addition, a wider 1 mm wide seal ring was used by Raytheon for their wafer-level packaging demonstration discussed previously in Section 2.2.4.

The approach taken by the UC Berkeley effort on this program was to transfer hexsil caps onto the thinner, 25 μm -wide gold target rings. A close-up of a seal ring is shown in Figure 2.5.1.4.

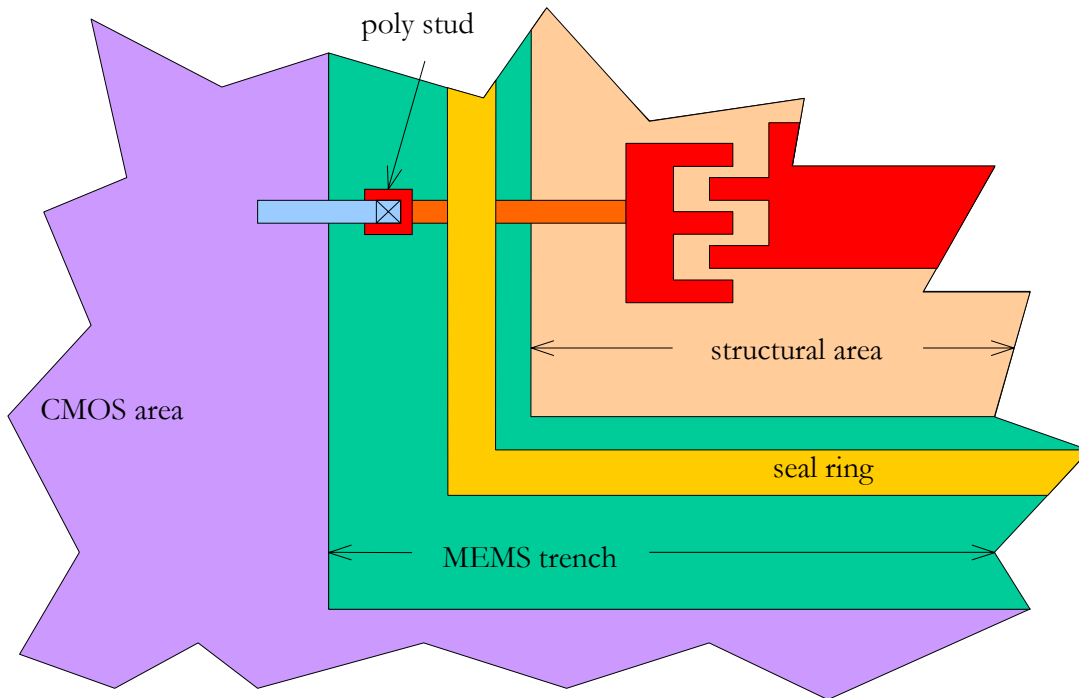


Figure 2.5.1.4 Detailed layout of Sandia IMEMS chip showing UC Berkeley seal ring target.

Although this technique was riskier than the Raytheon wafer-level packaging approach, if successful, it would offer an ultra low cost, high density MEMS packaging approach especially for small MEMS devices. A key feature of the Sandia IMEMS process was the planar region around the MEMS devices where the gold target ring was patterned, giving an area free of topography to form a seal. A cross section of this region is shown in Figure 2.5.1.5.

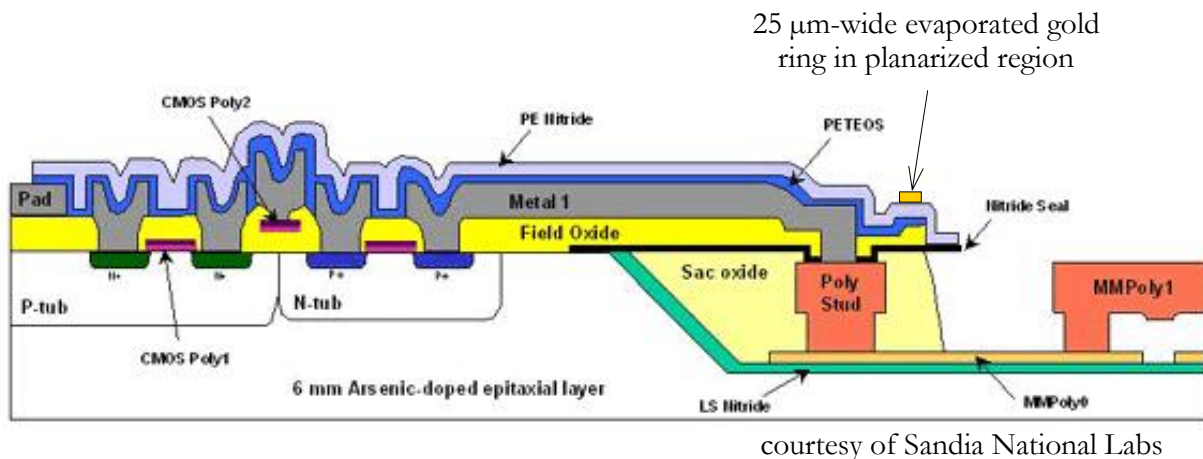


Figure 2.5.1.5 Cross-section of Sandia IMEMS layout showing planarized region with evaporated gold seal ring target for UC Berkeley vacuum packaging effort.

2.5.2. Design and Fabrication of SiGe Hexsil Microcaps

The main design features of the SiGe hexsil vacuum caps were as follows. Firstly, since the total size of the caps required for the Sandia process was $1.8 \times 1.8 \text{ mm}^2$, a matrix of honeycomb ribs was needed to provide stiffness. Secondly, a recess was required that would provide clearance between the cap and the MEMS device. Thirdly, an electroplated gold seal ring matching the built-in seal ring on the target chip was required. The basic fabrication sequence for the poly-SiGe hexsil packaging effort is shown in Figure 2.5.2.1. The detailed process flow is described in Table 2.5.2.1.

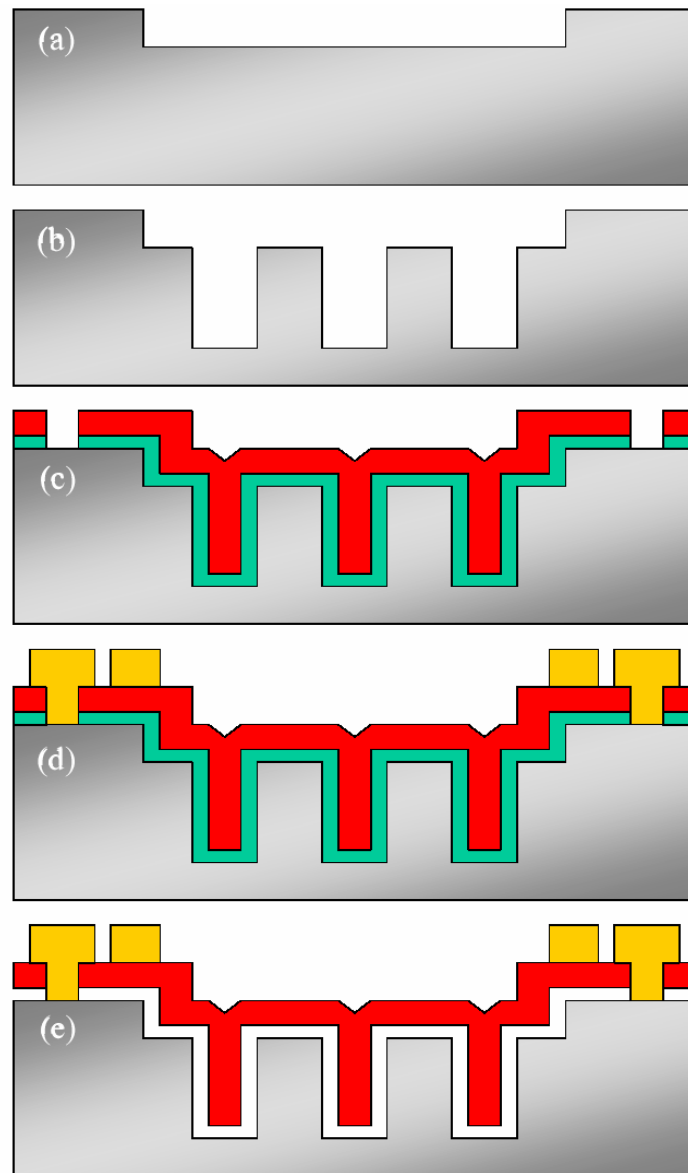


Figure 2.5.2.1 Process flow for poly-SiGe hexsil vacuum packages.

The first step in the fabrication process involves preparing the hexsil molds. Firstly, the recesses were patterned with a recess mask, and etched in a STS deep reactive ion etcher to a depth of around 5 μm (Figure 2.5.2.1a). For these shallow recesses ($<6\mu\text{m}$), photoresist coverage in the following steps was not a significant problem, but a 4 μm thick layer of photoresist was usually applied in later steps to safely cover the edges of the recess where the photoresist would be thinner. The second step was to etch 6 μm wide, 50-100 μm deep trenches into the wafer to provide the hexsil matrix, again using the STS (Fig 2.5.2.1b). After photoresist removal and wafer cleaning, a 0.5 μm thermal oxide was grown on the hexsil molds. This oxide was stripped in HF, thus smoothing the scalloping on the sides of the trenches caused by the STS etch, and removing “grass” at the bottom of the trenches. The wafers were reoxidized to provide an etch stop for the patterning of the poly-SiGe layers.

After mold fabrication, the deposition and patterning of the sacrificial poly-Ge and structural poly-SiGe layers was performed. Due to the slight lateral undercut during the deep trench etch and the first oxidation and its removal, the trenches became wider than their design width of 6 μm . UC Berkeley found that the new dimensions must be taken into account before finalizing the desired thickness of the depositions. A typical final trench width was 8 μm . As a result, 2.5 μm of poly-Ge and 3 μm of poly-SiGe resulted in properly filled trenches. The deposition conditions for the poly-Ge sacrificial layer were 350°C, 600 mT, and 88 sccm of GeH_4 , resulting in an average deposition rate of 60 Å/min. A 40% Ge recipe was used for the SiGe structural layer which was done at 500°C and 300 mT, with flow rates of 186 sccm for SiH_4 and 33 sccm for GeH_4 . This recipe resulted in a deposition rate of about 88 Å/min. These layers were patterned with a PLY0 face sheet mask in a Lam polysilicon etcher, which removed both the structural and sacrificial layers and stopped on the underlying thermal oxide (Fig 2.5.2.1c).

The next step was to form the metal bumps and seal ring for transfer (Figure 2.5.2.1d). First, a seed layer of chrome/gold (150 Å Cr, 1000 Å gold) was thermally evaporated over the wafer. In order to ensure that all regions of gold were electrically connected for the subsequent electroplating step, it was important to achieve continuous coverage over the wafer. For the deposition of chrome and the first 500 Å of gold, the wafer was tilted about its in-plane diagonal axis so that the top-right edge was elevated about an inch. Subsequently, the bottom-left edge was elevated in the same fashion and the remaining 500 Å of gold was evaporated. Using this technique assured that a metal film on the vertical sidewalls of any features would form an electrically continuous path down into the base of the feature. After the seed layer deposition, the plating mask was patterned. For this step, thick photoresist was used, since the desired thickness of the gold bumps and seal ring was around 6-8 μm . SJR5740 photoresist was spun on at 3500 rpm for 15 sec and baked for 7 min at 115°C, resulting in a thickness of about 8 μm . This was exposed with a dark-field Au mask and developed to form the electroplating molds for the gold bumps and seal rings. Gold was electroplated from a plating bath (Technic, Inc.) at 48°C using a platinum electrode as the positive terminal and the wafer as the negative terminal. A current of approximately 5 mA was applied for about 30 min, resulting in the proper plated gold thickness measured by profilometry.

To prepare the MEMS structures for release, the wafer was diced using photoresist to protect the front side. The photoresist was subsequently removed with acetone and the gold/chrome seed layer was removed by wet etching. The release of the MEMS structures was done in 30% H_2O_2

in a convection oven at 90°C (Figure 2.5.2.1e). For the large (1.8 mm)² caps, an etch time of 36h was normally sufficient for release. The chips were then rinsed in DI water and transferred to methanol. The bonding and transfer to unpatterned, gold-coated silicon chips or Sandia iMEMS chips was done using a Research Devices flip-chip bonder. Many combinations of pressure and temperature were tried. Good results were obtained by heating to 150°C and applying 65 kg of force.

Table 2.5.2.1. Standard Poly-SiGe Hexsil Cap Process Flow.

1. Starting wafers 4" (100) p-type.
2. Recess etch
 - 2.1. [svgcoat, gcaws2, svgdev] lithography with mask TRN1, 2 μm g- line photoresist
 - 2.2. [STS] 5 μm DRIE, recipe HEXA100
 - 2.3. [spindryer3] strip resist, PRS-3000
3. Trench etch
 - 3.1. [svgcoat, gcaws2, svgdev] lithography with mask TRN0, 4 μm g-line photoresist
 - 3.2. [STS] 50-100 μm DRIE, recipe HEXA100
 - 3.3. [spindryer3] strip resist, PRS-3000
4. Mold smoothing
 - 4.1. [tylan1/2] oxidation, recipe SWETOXB, 1100°C, 40 min, 0.5 μm
 - 4.2. [sink8] strip oxide in 5:1 BHF
5. Depositions
 - 5.1. [tylan1/2] oxidation to protect mold, SWETOXB, 1100°C, 40min, 0.5 μm
 - 5.2. [tystar19] sacrificial poly-Ge, 350°C, 600 mT, 88 sccm GeH_4
 - 5.3. [tystar19] structural poly-SiGe, 40% Ge, 500°C, 300 mT, 88 sccm GeH_4
6. Face sheet patterning
 - 6.1. [svgcoat, gcaws2, svgdev] lithography with mask PLY0, 4 μm g-line photoresist
 - 6.2. [lam5] etch poly-SiGe and poly-Ge, recipe 5003
 - 6.3. [spindryer3] strip resist, PRS-3000
 - 6.4.
7. Gold seed layer
 - 7.1. [v401] evaporate chrome/gold seed layer, 150Å Cr, 500Å Au with wafer tilted with top-right edge up about 1 inch, 500Å Au with wafer tilted with bottom-left edge up 1 inch.
8. Plating mask patterning
 - 8.1. [spinner1] 8 μm SJR5740 resist, spun 15 sec at 3500 rpm, softbake 7 min at 115°C
 - 8.2. [gcaws2] lithography with mask AU
 - 8.3. [manual develop] 3.5 min, Microposit Developer Concentrate, no bake.
9. Gold electroplating
 - 9.1. [plating sink] gold plating bath (TG 25E RTU, Technic, Inc.),
 - 9.2. 48°C. 5 mA for 10 min, check thickness by profilometry (as200)
 - 9.3. [PRS-3000 bath] strip resist, ~15 min.
10. Dicing
 - 10.1. [svgcoat] coat with protective photoresist layer
 - 10.2. [disco] dice into 1 cm^2 chips
11. Release
 - 11.1. remove photoresist in acetone
 - 11.2. wet etch Au and Cr seed layer (Gold Etchant TFA, Transene Co., CR-7 Chrome Mask Etchant, Cyantek Co.)
 - 11.3. etch sacrificial poly-Ge, 30% H_2O_2 heated to 90°C in oven, approximately 0.5 $\mu\text{m}/\text{min}$.
 - 11.4. rinse in DI water
 - 11.5. transfer to methanol
12. Transfer
 - 12.1. [flipchip] align and bond chip with target die (bare Cr/Au target or Sandia iMEMS chip).

2.5.3. SiGe Results

SiGe hexsil packages were successfully released and transferred onto unpatterned, gold-coated target dice without MEMS structures. Figure 2.5.3.1 shows a SEM of several 1.8x1.8 mm² caps. In the figure, fully transferred caps are evident. Also evident are a broken, partially transferred cap and a bare gold seal ring indicating that a transferred cap is missing.

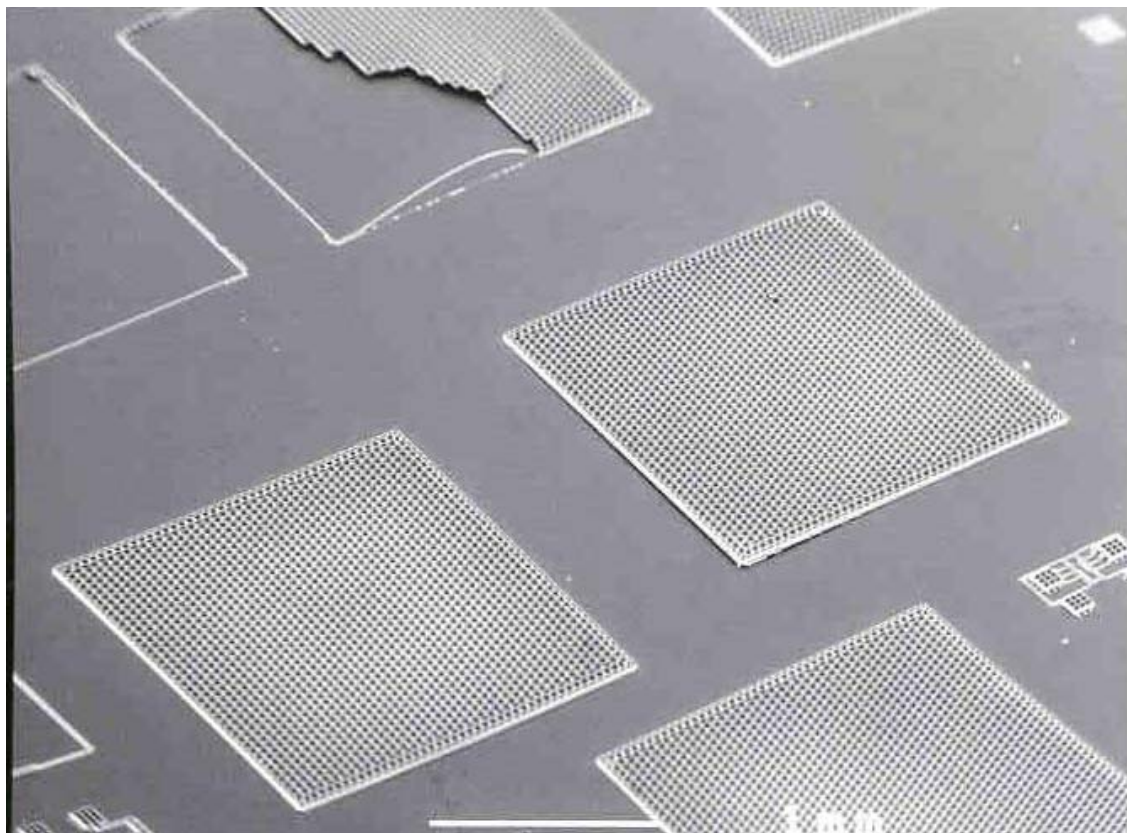


Figure 2.5.3.1 Several poly-SiGe hexsil caps transferred to a gold-coated silicon substrate.

The most common failure mechanism preventing successful SiGe hexsil cap transfer appeared to be the co-planarity of the donor and target chips. The chips need to be separated in the vertical direction by 50-100 μm with less than approximately 2 μm lateral movement to prevent the hexsil structures from being sheared and broken. For this reason, the planarity of the transfer and separation were of utmost importance. The Research Devices flipchip bonder has a lower chuck whose angular orientation is held in place by a vacuum system. The lower chuck is normally planarized prior to transfer by bringing it into contact with the upper chuck, releasing the vacuum to allow the chucks to become co-planar, and then restoring the vacuum to lock them into the new orientation. However, due to slight variations in the planarity of the chips, planarizing the chucks in this way resulted in successful transfers less than 10% of the time. Instead, it was found that if the planarization process was done with the chips already mounted on the chucks, a success rate closer to 50% was achieved.

Attempts to transfer vacuum caps onto Sandia IMEMS chips were also made. Using the same planarizing technique as above, UC Berkeley was able to achieve bonding and partial transfer of

one cap in 5 attempts. The small number of available chips limited the number of transfer attempts. Figure 2.5.3.2 shows this transferred cap partially covering the MEMS area on the IMEMS chip.

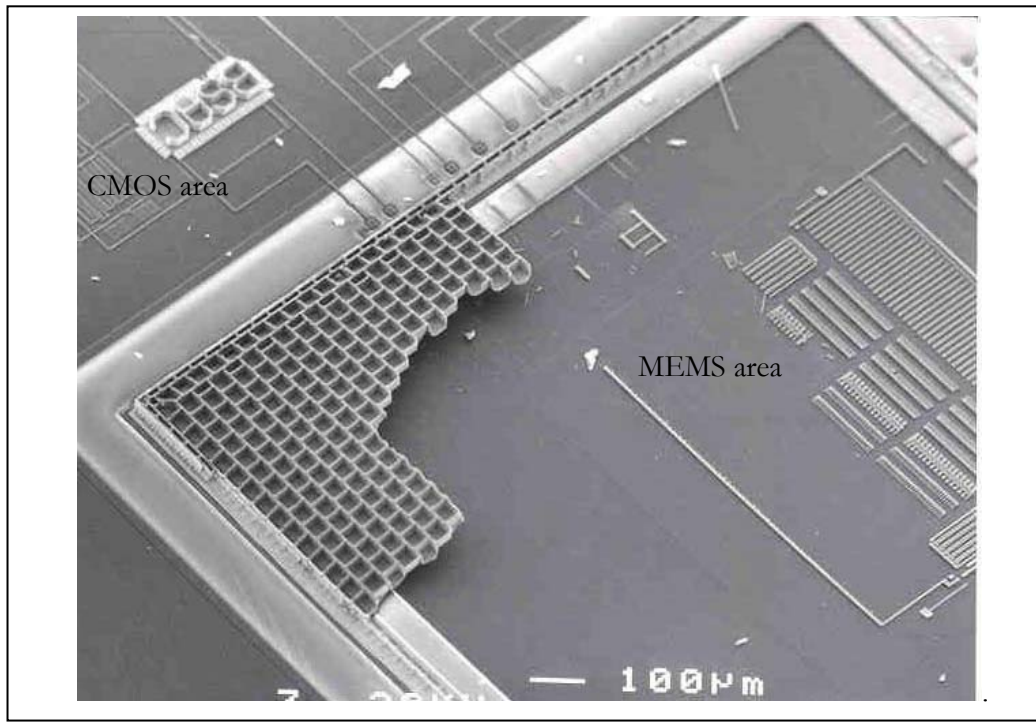


Figure 2.5.3.2 A poly-SiGe hexsil cap partially transferred to a Sandia integrated MEMS chip

Once the bonding and transfer technique at ambient pressure was demonstrated, the next step was to attempt to seal the devices in vacuum. In order to do this, a vacuum bonding chuck was built, which is pictured in Figure 2.5.3.3. This tool is evacuated by a vacuum line, and a compressive force is applied by an external press, with heating supplied by three cartridge heaters inserted into the base.

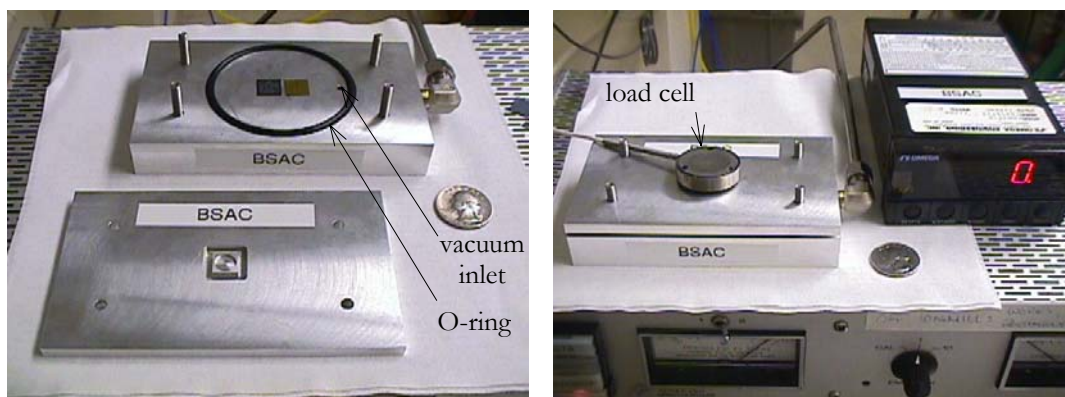


Figure 2.5.3.3 Photographs of vacuum bonding tool.

The force was measured using a load cell between the press and the top of the bonding device. Temperature was measured with a thermocouple inserted into a small hole beneath the chip. In order to achieve vacuum bonding, the two chips were aligned in the flipchip bonder and gently tack-bonded together to affix them without completely sealing the gold rings to each other. Next, the two-chip stack was moved to the vacuum bonding device, which was evacuated and heated, and an external force was applied. After this vacuum sealing step, the chips were placed back into the flipchip bonder for controlled separation. However, after separation, the transfer yield was reduced to near zero, and vacuum seals were not achieved. It was hypothesized that the act of removing the two-chip stack from the flipchip bonder, placing them into the vacuum bonding device, and back into the flipchip bonder, disrupted the very precise alignment required to separate the chips without shearing the structures. A possible solution to this problem might be to design and construct a set of chucks for holding the chip stack during the entire alignment, vacuum bonding, and separation processes. Such a scheme may be able to maintain the very precise co-planarity required for hexsil transfer processes.

2.5.4. SiGe Process Developments

This section details the process developments that were undertaken under this program in order to improve the poly-SiGe hexsil packaging technology.

Etchant Ducts

One of the major problems that was encountered was the incomplete release of the large (1.8 mm)² caps. Some caps were not fully released even after they had been etched for two to three times longer than the expected release time. These chips were cleaved, and the newly exposed edge was imaged in a microscope. Under the center of the caps, unetched poly-Ge was apparent, and under the extremities of the cap, the poly-Ge was removed. However, at the interface of these two regions, a transparent layer of material was observed. This material dissolved both in DI water and in hydrogen peroxide at room temperature, so it was hypothesized that it was a germanium oxide. To confirm this, the composition of the oxide was determined using Energy Dispersion Spectroscopy in a scanning electron microscope. This technique works by impinging an electron beam on a surface and measuring the characteristic x-ray wavelengths given off as the constituent atoms are excited by the electrons. Figure 2.5.4.1a contains a side view SEM of the cleaved region of an unreleased cap showing the oxide material. Figure 2.5.4.1b shows the EDS analysis of the region shown in the box in Figure 2.5.4.1a, indicating that the material was indeed a germanium oxide. H₂O₂ oxidizes poly-Ge to form GeO and then GeO₂, which dissolves in water. Since the material in question dissolves in water, it is presumed to consist primarily of GeO₂.

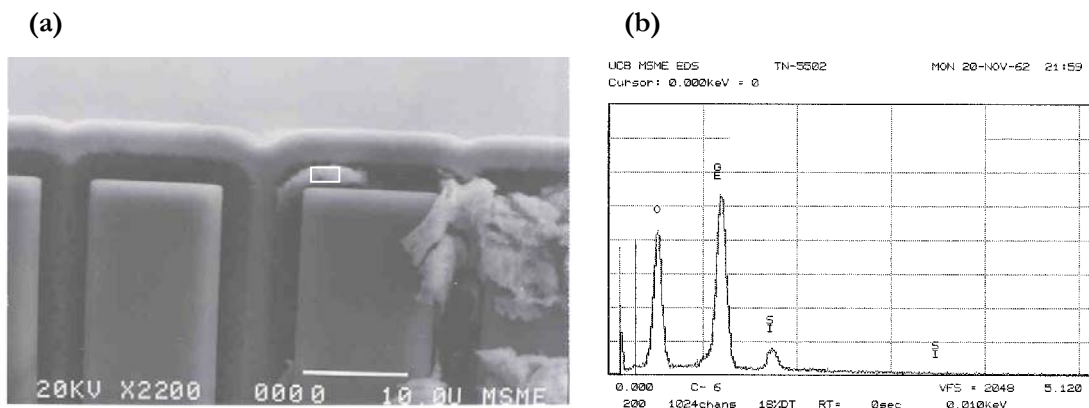


Figure 2.5.4.1 (a) SEM of unreleased cap cleaved through its center, revealing residue, (b) EDS spectrum taken of residue, showing that it is a germanium oxide.

Since the germanium oxide dissolved in water once it was exposed by cleaving but not when it was still underneath the structures, indicates that the dissolution process was mass-transport limited. A lack of fluid circulation, leading to a high concentration of aqueous GeO_2 near the interface may have prevented the oxide from dissolving during release. The formation of bubbles beneath the structure was considered as a possible cause. Therefore, a surfactant (Triton X-100) was added to the H_2O_2 . However, no improvement was observed. Attempts to improve the flow with agitation were also unsuccessful, which is not surprising considering the extensive length and narrow width of the diffusion path to the interface. Therefore, in order to increase the mass transport of the chemicals involved, a new design utilizing etchant ducts was fabricated. The ducts were designed to improve the flow of products and reactants in order to facilitate the efficient removal of the GeO_2 interfacial layer.

The fabrication of etchant ducts in the poly-SiGe hexsil cap process is shown in Figure 2.5.4.2.

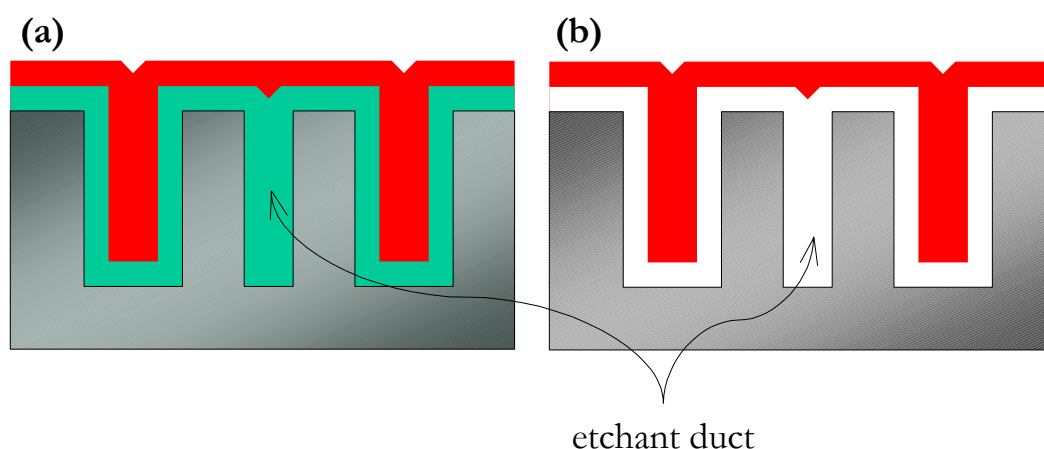


Figure 2.5.4.2 Cross sectional schematic showing ducts for increased diffusion of reactants and products to improve microstructure release. (a) Before release, (b) after release.

In this process, thin trenches form etchant ducts beneath the structure, while normally sized trenches would result in structural beams. Here, we used 3 μm -wide trenches (compared to the standard 6 μm width), which became completely filled with sacrificial poly-Ge before the structural poly-SiGe deposition. Upon release, these trenches form ducts to enhance the diffusion of products and reactants. These ducts were fabricated beneath the structure, as well as extending outward from the structure like fins, as shown in Figure 2.5.4.3. The fins are also visible in the images in Figure 2.5.4.4. The fins increase the cross sectional area for diffusion between the sacrificial layer beneath the cap and the bulk.

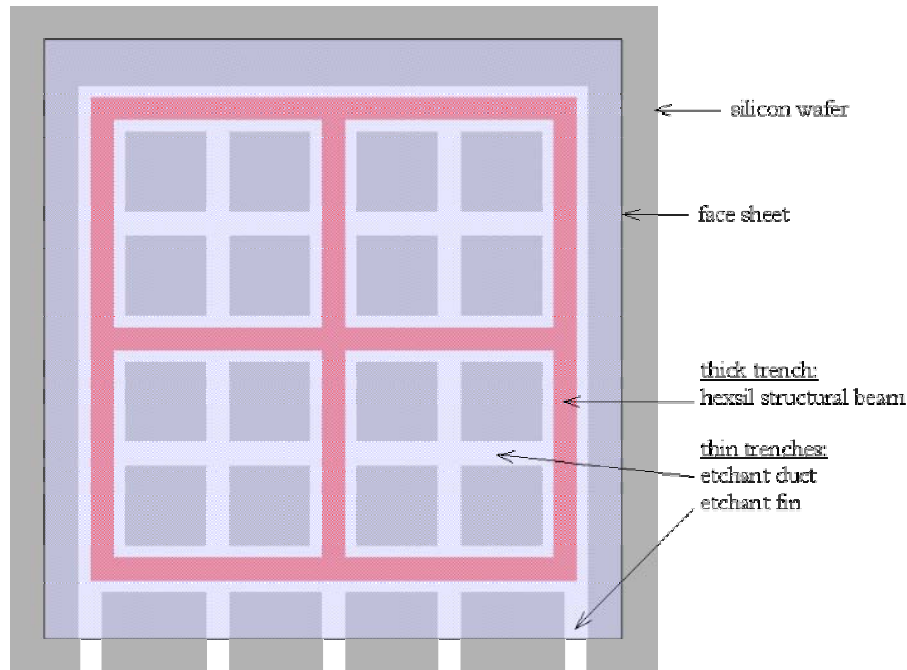


Figure 2.5.4.3 Layout schematic of a hexsil structure showing etchant “ducts” and “fins” for improving release.

Figure 2.5.4.4 shows four partially etched test structures with and without etchant ducts and fins. In the figure, (a) has no ducts or fins, (b) has fins, (c) has ducts, and (d) has both fins and ducts. Since no improvement was shown between (c) and (a), it was concluded that the ducts beneath the structure do not significantly aid in releasing the structure. This is probably because these ducts can only increase the flow within a single “cell” of the hexsil structure, but cannot facilitate flow between cells. However, since in (b) and (d), the etch has proceeded farther than in (a) and (c), it is apparent that the fins do increase the diffusion and facilitate release.

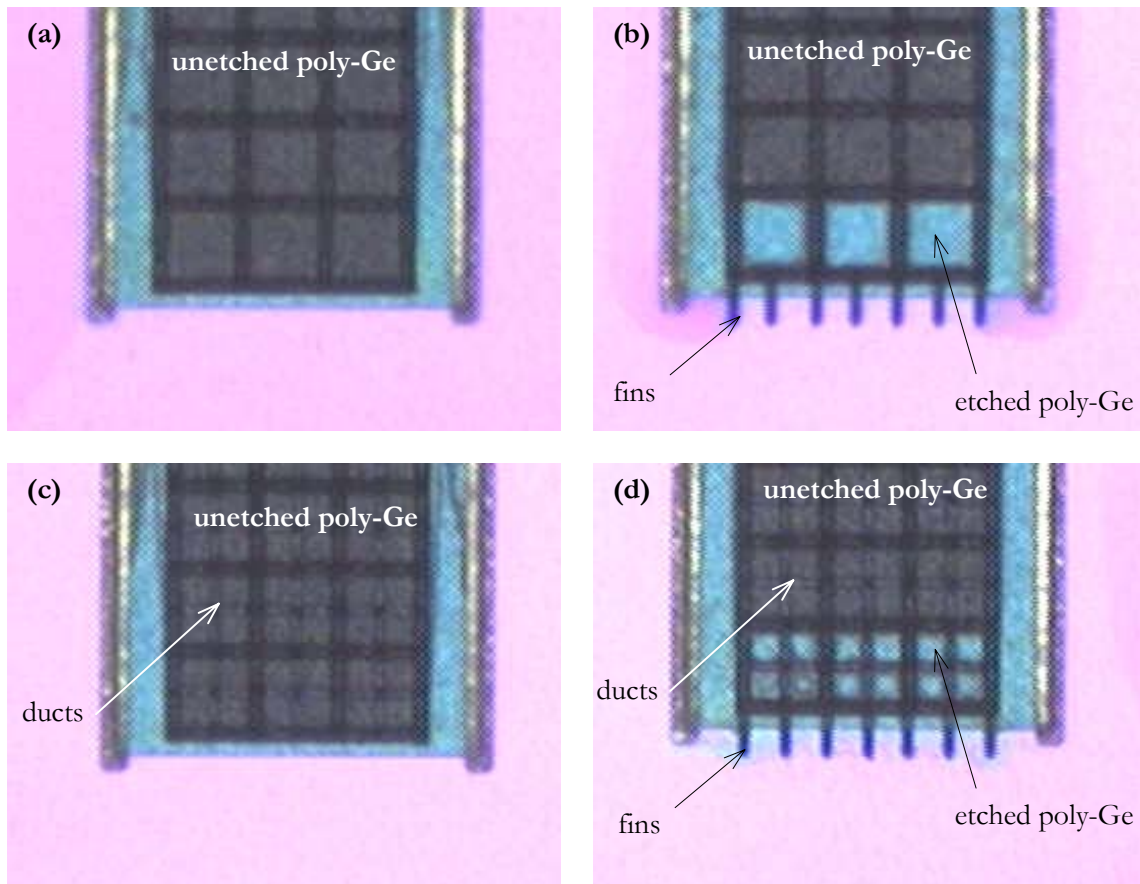


Figure 2.5.4.4 Microscope images of etchant duct test structures, etched partially in H_2O_2 . (a) Without ducts or fins, (b) Without ducts under structure, but with fins extending outward from structure, (c) With ducts under structure, but without fins extending outward, (d) With both ducts under structure and fins extending outward.

Poly-SiGe hexsil structures might be more reliably released if, in addition to fins, a deep set of thin ducts were etched beneath the trenches, as shown in Figure 2.5.4.5. In contrast to the ducts demonstrated under this program, this type of duct would increase the cross-sectional area for flow between cells underneath the entire structure, rather than just within each cell.

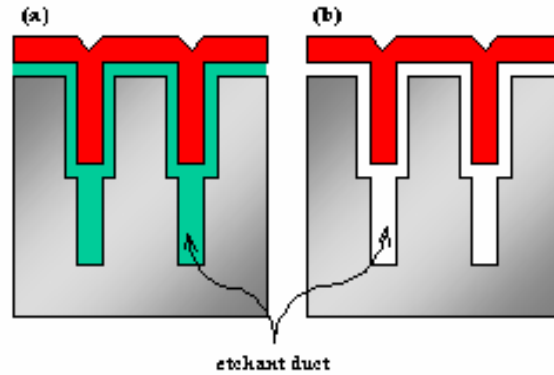


Figure 2.5.4.5 Cross section of possible duct layout, which would facilitate flow beneath the entire hexsil structure and improve release. (a) Before release, (b) after release.

Gold Stud and Seal Ring Designs

A second problem encountered in the UC Berkeley development of poly-SiGe hexsil micropackages was low transfer yield. The initial attempts used a plated gold “staple” design for affixing the structures to the donor substrate prior to transfer. However, hexsil caps were frequently found to be broken after transfer, or not transferred at all. This was presumed to be due to the geometry of the design, which transferred the compression load to the hexsil structure rather than absorbing it in the gold itself, as shown in Figure 2.5.4.6a. This caused the structure to impact the bottom of the mold during compression. An SEM of the staple design, before transfer, is shown in Figure 2.5.4.7.

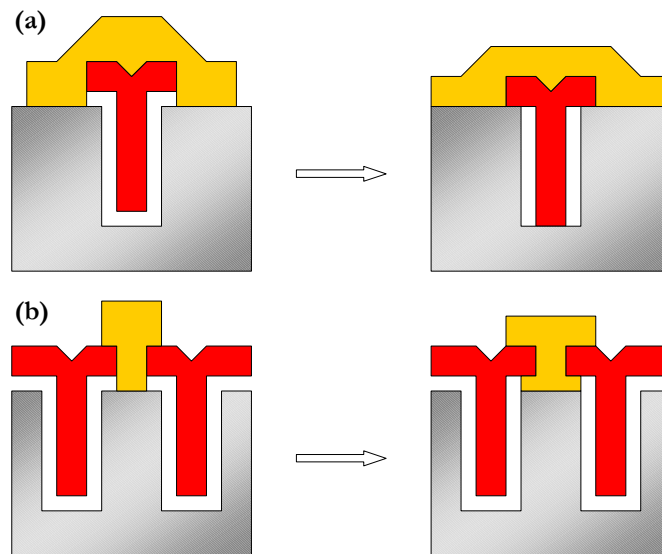


Figure 2.5.4.6 Schematics of (a) “staple” and (b) “rivet” gold bump designs before and after compression.

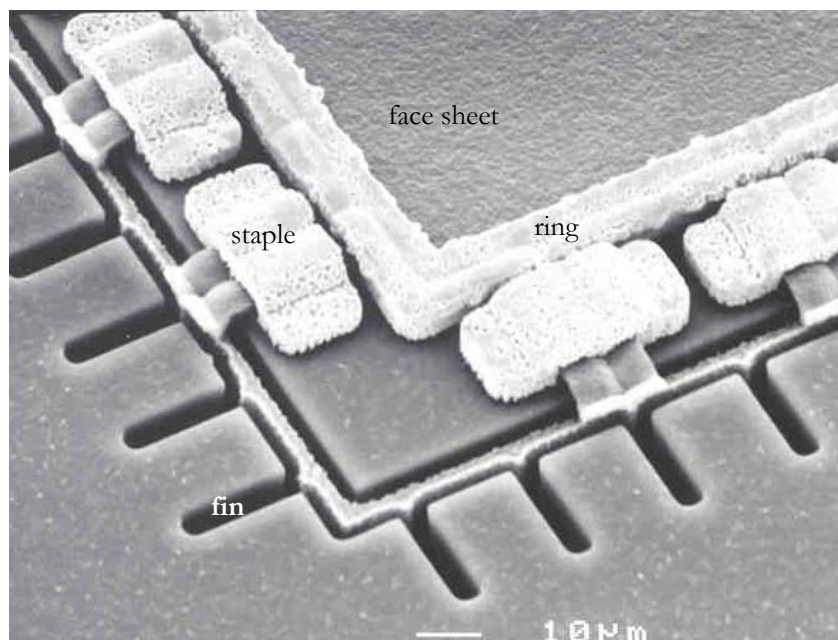


Figure 2.5.4.7 Seal ring design using electroplated gold “staples” to hold released cap to donor wafer.

A second design used a gold “rivet” to improve the transfer yield, as shown above in Figure 2.5.4.6b. In this design, the gold bumps were plated into small holes directly over unetched portions of the wafer to couple the load to the substrate more efficiently. The gold rivets on silicon pedestals support the compression load without allowing the hexsil structure to contact the bottom of the mold wafer. Furthermore, the bottom of the rivet flattens beneath the hexsil structure upon compression, enhancing its adhesion to the structure. A SEM of the rivet design, before transfer, is shown in Figure 2.5.4.8a, along with a SEM of a rivet design with a double seal ring in Figure 2.5.4.8b. Although a detailed comparison of the transfer yield between the rivet and staple designs was not possible due to release problems and unavailability of the flip-chip bonder, the instances of breakage were lower for rivet designs than for staple designs.

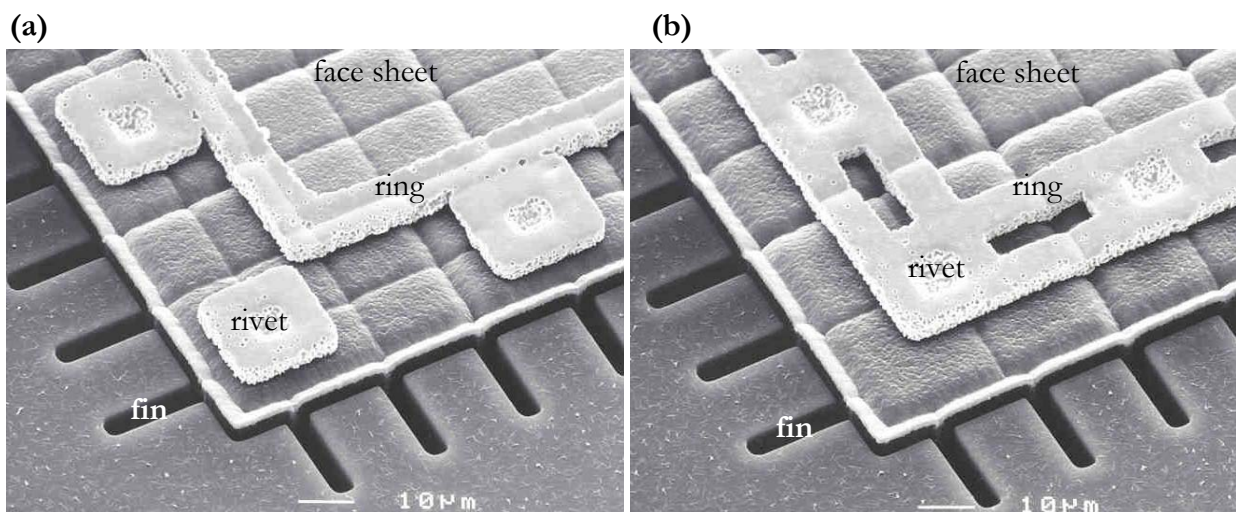


Figure 2.5.4.8 Seal ring design using “rivets” to hold released cap to donor wafer. This design transfers the compression load directly to the substrate, rather than through the hexsil structure.
 (a) Single seal ring (b) double seal ring.

2.5.5. Wafer-level Vacuum Packageable Inertial Sensor Design and Test

A second goal of the UC Berkeley effort under this program was the design and test of a wafer-level vacuum packageable inertial MEMS chip. This chip was described in Figure 2.2.4.1 and Figure 2.5.1.3. This chip was used in the inertial MEMS wafer-level vacuum packaging demonstration carried out by Raytheon as described previously in Section 2.2.4 and in the hexsil microcap development carried out by UC Berkeley in the previous sections. On the chip layout was included a resonant accelerometer, a resonant gyroscope and micro resonator test structures. The chip was fabricated at Sandia National Labs using the IMEMS process.

Berkeley designs in the Sandia IMEMS process included a resonant accelerometer, a gyroscope, and various vacuum test structures. While a design flaw in the sustaining amplifier for the gyroscope rendered it nonfunctional, the other devices yielded data. Unfortunately, the anti-stiction coating used in IMEMS caused a major decrease in yield in the wafer-scale packaged devices, due to debris accumulation beneath the surface microstructures, which caused shorts to the supply voltage.

Resonant sensing, the technique to represent an input measurement as a resonant frequency shift of a sensing device, has been demonstrated as a sensitive detection technique for microaccelerometers. The resonant accelerometer (Figure 2.5.5.1) was designed to be compatible with the Sandia National Labs IMEMS foundry process. The resonant accelerometer consists of a central proof mass, and a lever that transmits the force applied to the proof mass axially to two resonant sensors that are implemented as double-ended tuning fork (DETF) structures. A Pierce oscillator circuit sustains motion at resonance in the DETF resonators. A die photo of the structure is shown in Figure 2.5.5.2. In the current design, a single lever is employed to amplify the force applied to the proof mass with an overall magnification of 30.

Conventionally packaged samples of the device obtained from Sandia National Labs were tested in a MMR technologies vacuum chamber with ambient pressures ranging between 200 mtorr to 30 mtorr. The device was functional with the resonant frequency of the sensors being around 120 kHz, which is slightly under the designed value. Figure 2.5.5.3 shows the output spectrum of the oscillator that has a noise floor of about -82 dBc/Hz. The response of the sensor to forces applied along the detection axis was tested, and a scale factor of approximately 16 Hz/g was obtained. The response of the sensor to an applied test electrostatic force is indicated in Figure 2.5.5.4. The measured values of the oscillator noise floor and the scale factor translate into an estimated noise floor of about $38 \mu\text{g}/\sqrt{\text{Hz}}$ for the overall device. Also, at the end of the program, functionality of resonant accelerometers that were wafer-level vacuum packaged by Raytheon was demonstrated.

An area for future work involves correcting the design flaw in the sustaining amplifier for the gyroscope to make it functional. This would allow the demonstration of a wafer-level vacuum packaged gyroscope. In addition, this inertial MEMS chip could be used for an inertial MEMS microshell vacuum encapsulation demonstration.

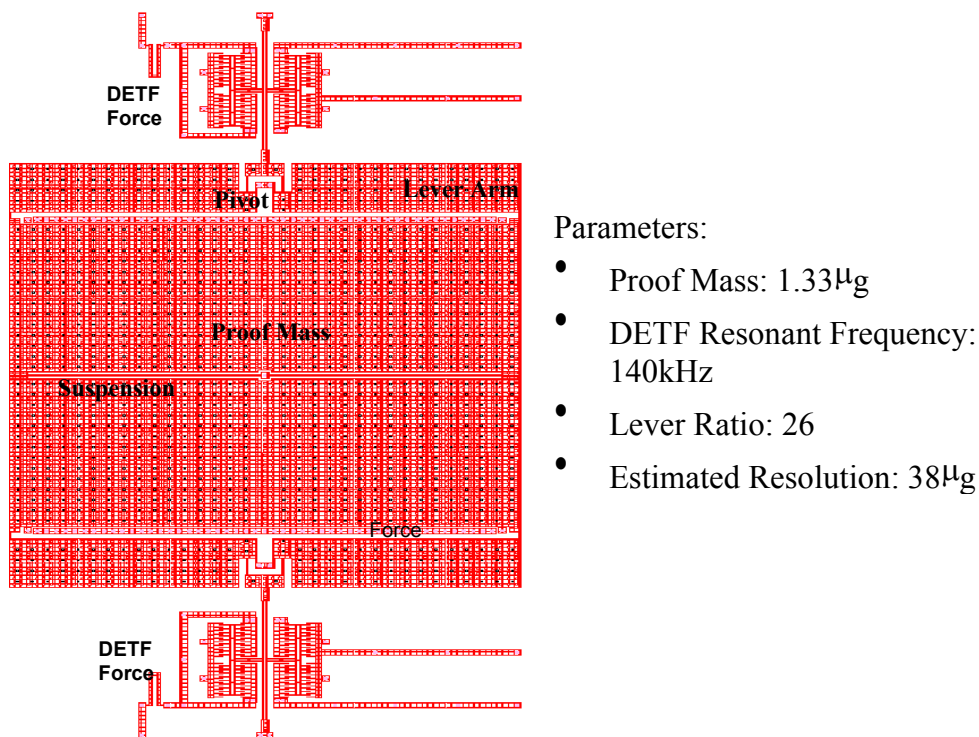


Figure 2.5.5.1 Layout of the RXL

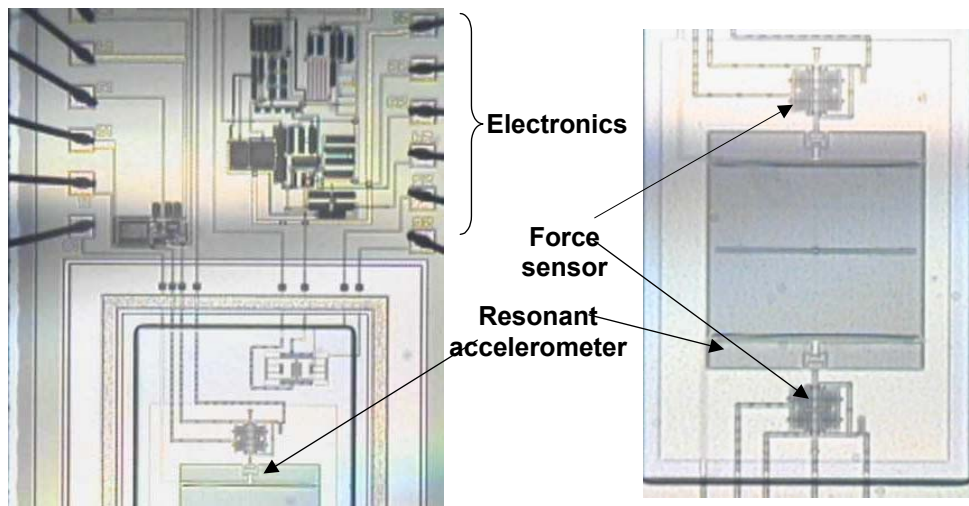


Figure 2.5.5.2 Die photo of the RXL.

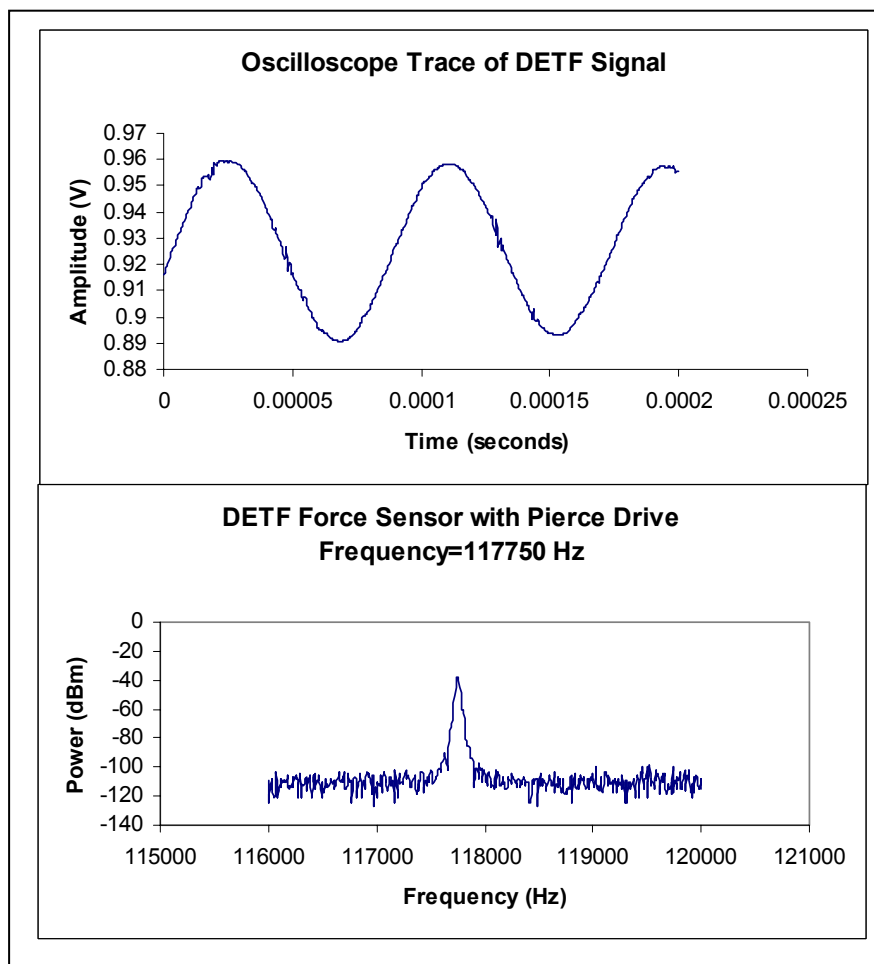


Figure 2.5.5.3 Waveform and spectrum of typical oscillator output

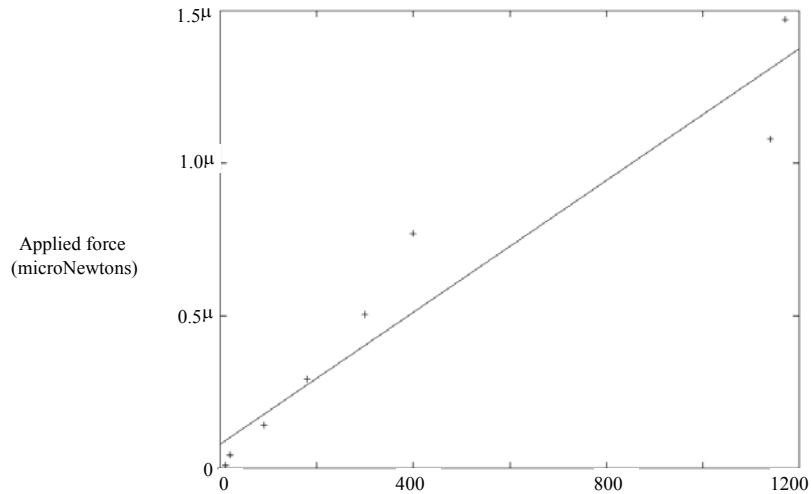


Figure 2.5.5.4 Frequency shift vs. force for a single tuning fork.

2.6. Sandia Inertial MEMS Fabrication Effort

The primary role of Sandia National Laboratories in this program was to supply integrated micro-electromechanical systems (IMEMS) suitable for demonstration of the vacuum sealing techniques proposed by the other program participants. Sandia developed common anchor points for all three vacuum lids that did not require changes in the current IMEMS fabrication process. The anchor points were gold-coated with a lift-off patterning process to complete the seal ring base on the die. In addition, the seal rings were designed to enable different vacuum lid approaches to be exercised independently and to use standard wire bonding techniques. The first seal ring, called the macro-scale seal ring, was used by Raytheon. The lids attached to this seal ring covered both the MEMS sensor, and CMOS electronics area. Electrical interconnects were routed under the gold seal ring to external bond pads that enabled standard wire bonding techniques to be used as shown in Figure 2.6.1. The width of the macro-seal ring was approximately 800 μ m.

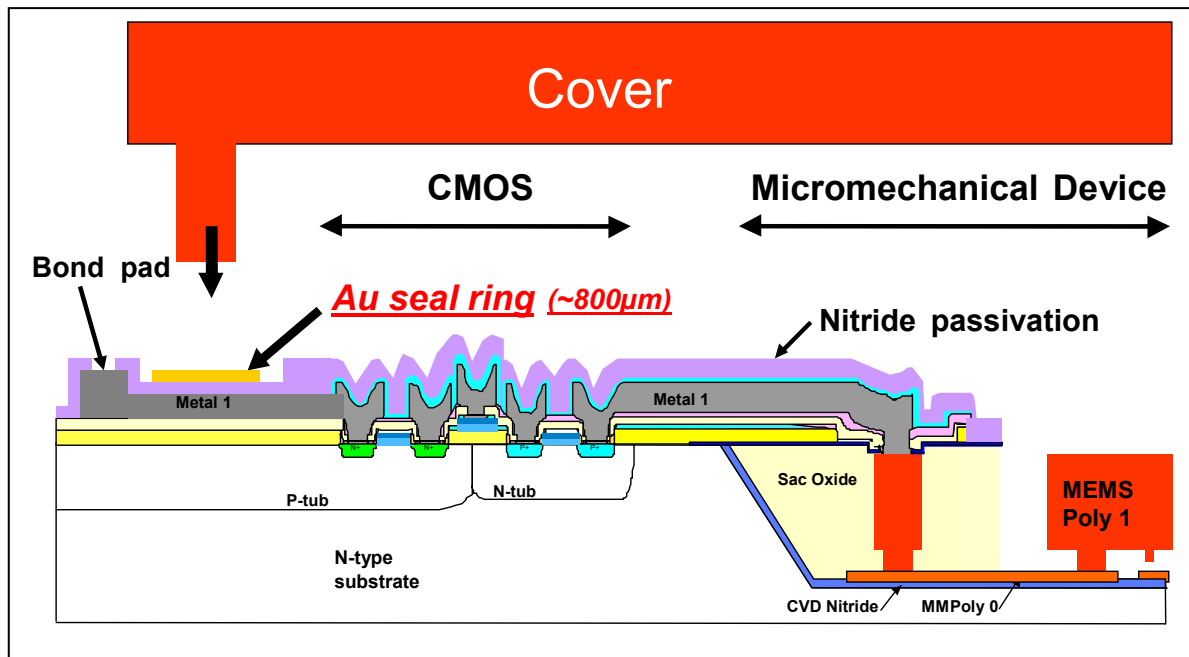


Figure 2.6.1 Raytheon macro-scale seal

Both UC Berkeley and MIT used the other seal ring, called the micro-seal ring. In this case, two options were developed that allowed the vacuum lids to be attached to either gold-aluminum or gold to conductive polysilicon seal rings. The placement of these micro-seal rings enabled another potential feature; multiple lids attached to a single die. This could enable independent control of pressure levels under each micro-lid. The width of the micro-seal ring was approximately $25\mu\text{m}$ to $50\mu\text{m}$. The design team decided to focus on the metal-seal ring approach in this project in order to minimize lid to die contact resistance as shown in Figure 2.6.2. Approximately 50 IMEMS accelerometers were delivered to Raytheon prior to starting the final design and layout to determine feasibility of the lid-sealing approach. Although these dice did not have the optimal seal ring designs, they were packaged with the macro-scale approach, tested and were fully functional. Based on these encouraging initial results, the decision was made for U.C Berkeley to begin design and layout activity on the new RS192 reticle set. Close cooperation between the program participants and UC Berkeley's prior experience designing in the Sandia technology, contributed to a final "production-ready" design. The first lot completed fabrication and samples were tested at UC Berkeley. Figure 2.6.3 shows a completed RS192 die. These initial samples did not have the seal rings and were found to be functional. Additional wafers (2ea) were delivered to Raytheon and MIT for the gold lift-off step.

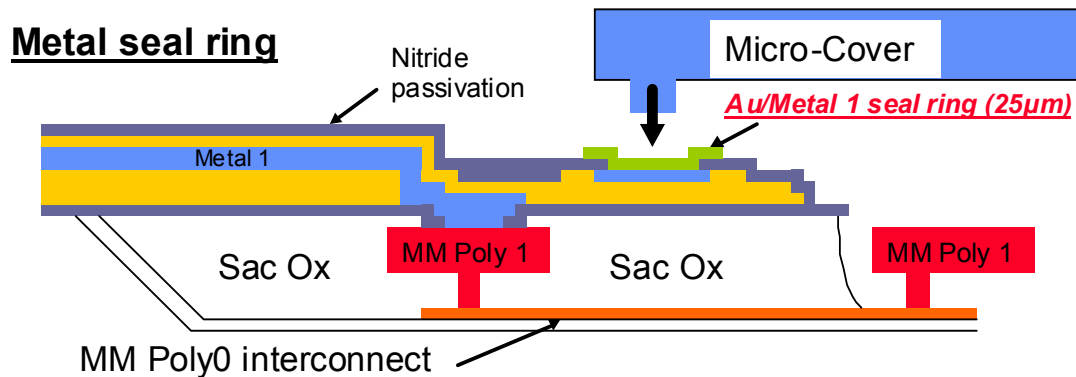


Figure 2.6.2 UC Berkeley, MIT micro-scale seal.

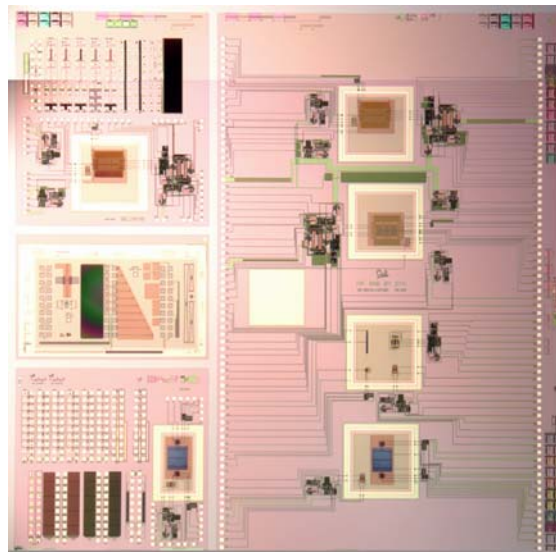


Figure 2.6.3 Completed RS192 die (without Au seal rings). See Figure 2.2.4.1 for die with seal ring.

The next step was to develop and implement the seal ring and MEMS release process. The approach taken was to allow partially completed wafers to be sent to Raytheon and MIT for the gold seal ring lift-off process. Wafers would be returned to Sandia for the MEMS HF release and Super Critical CO₂ (SCCO₂) drying steps. Wafers previously sent to Raytheon and MIT were returned with their respective gold seal rings now in place. Because of concerns about gold cross-contamination of tools in Sandia's Microelectronics Development Lab (MDL), these wafers were photo-patterned for HF release by a Suss contact alignment system in Sandia's Compound Semiconductor Research Lab (CRSL), then diced, released and dried at the MDL. Photo-resist is designed to protect the CMOS and Au seal rings during the release etch. One concern here is the amount of residual gold protruding vertically at the edge of the seal ring due to the lift-off process. If this material were too high it may not be covered effectively by the

protective photo-resist layer and would fail in the release etch. Raytheon, UC Berkeley and MIT were made aware of Sandia's concerns and Sandia worked hard to minimize this effect in their lift-off processes. Upon subsequent inspection, the release process did not appear to affect the Au seal rings indicating the amount of residual gold from the lift-off was within process tolerance. These devices were then delivered to the other program participants for lid attach and testing.

The second phase of this program involved delivery of released, quarter wafer, IMEMS pieces to be used in the multiple-dice sealing demonstration. Additional wafers from the RS192 lot were processed through gold lift-off, and diced into quarter pieces. These pieces were released, SCCO2 dried and delivered to Raytheon, MIT and UC Berkeley for lids and testing.

2.7. Wafer-level Packaging of University of Michigan RF MEMS Resonators (Raytheon)

Another Raytheon goal under the program was a quasi-wafer-level RF MEMS vacuum packaging demonstration using University of Michigan RF MEMS resonator chips. The key technical challenge in the RF MEMS wafer-level package demonstration was the development of a low loss, low capacitance, high frequency RF interconnect. While a full RF MEMS quasi-wafer-level vacuum packaging demonstration was not achieved, Raytheon did make progress in developing a form and function RF MEMS wafer-level package demonstration. The quasi-wafer-level packaging approach is shown in Figure 2.7.1 and utilizes existing University of Michigan RF MEMS resonator chips shown in Figure 2.7.2. The form and function RF MEMS wafer-level package demonstration employs double-side polished 0.045" thick silicon lid and base wafers in which a 0.020" cavity was etched in each. The combined 0.040" clearance in the cavity allowed the RF MEMS resonators to be solder die attached and wire bonded to the base wafer. Photographs of etched lid and base cavity 1" wafers are shown in Figure 2.7.3. An RF MEMS die is mounted in the base 1" wafer cavity. An RF MEMS wafer-level package is also shown.

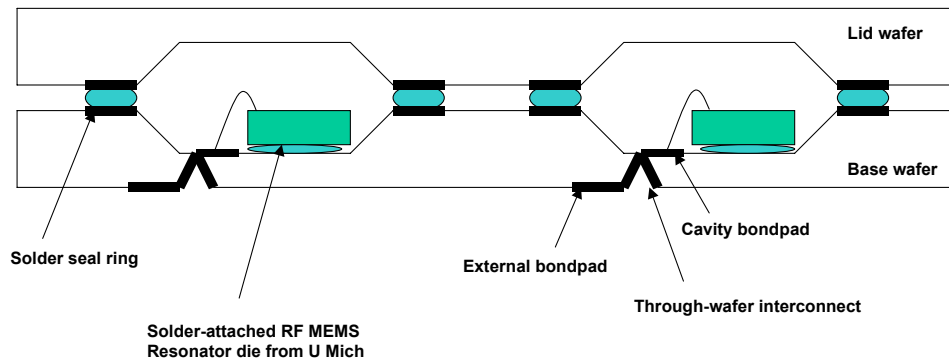


Figure 2.7.1 RF MEMS Wafer-level Vacuum Package with Low Loss Through Wafer Interconnect.

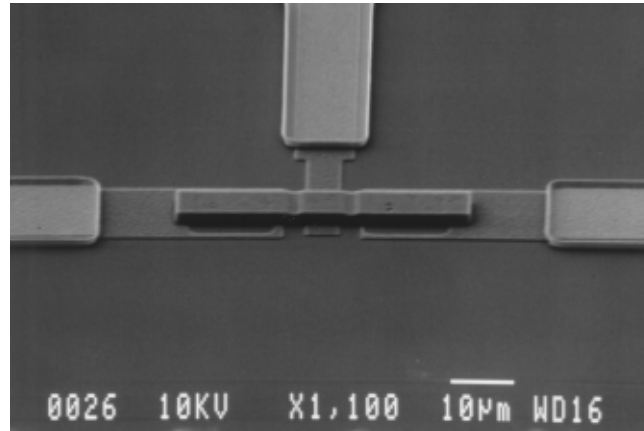


Figure 2.7.2 U. Michigan RF MEMS Resonator.

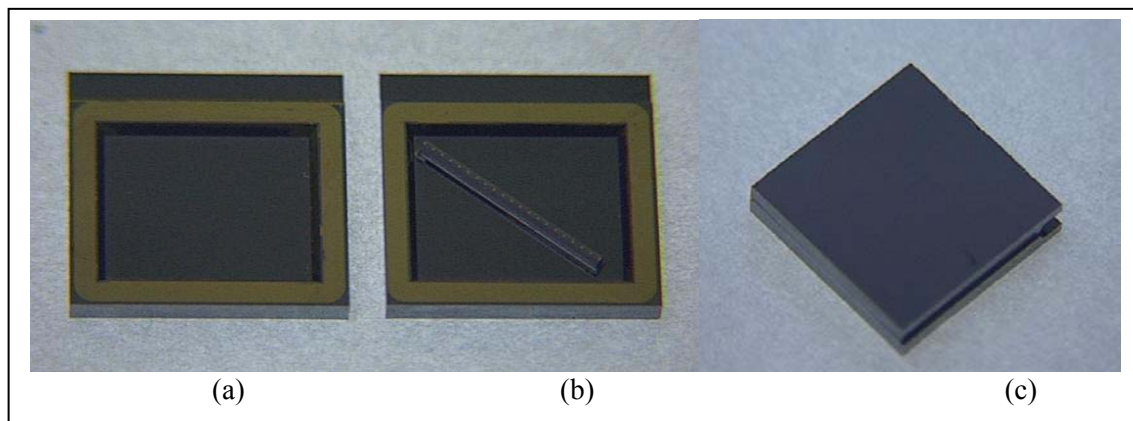


Figure 2.7.3 a) 1" lid and b) base etched cavity wafers with RF MEMS resonator die mounted in base wafer cavity. c) RF MEMS wafer-level package

The key technical challenge in the RF MEMS wafer-level package demonstration was the development of a low loss, low capacitance, high frequency RF interconnect. The approach attempted under this program involved KOH etch of through wafer vias. Results of via etch tests using KOH are shown in Figure 2.7.4. The KOH etching of the vias proved difficult to control. Depending on via size, the result was either under-etching or over-etching of the via. Under-etching resulted in the via not completely etching through the $\sim 0.020''$ cavity. Over-etching caused adjacent vias to merge, which would give rise to shorting upon metallization.

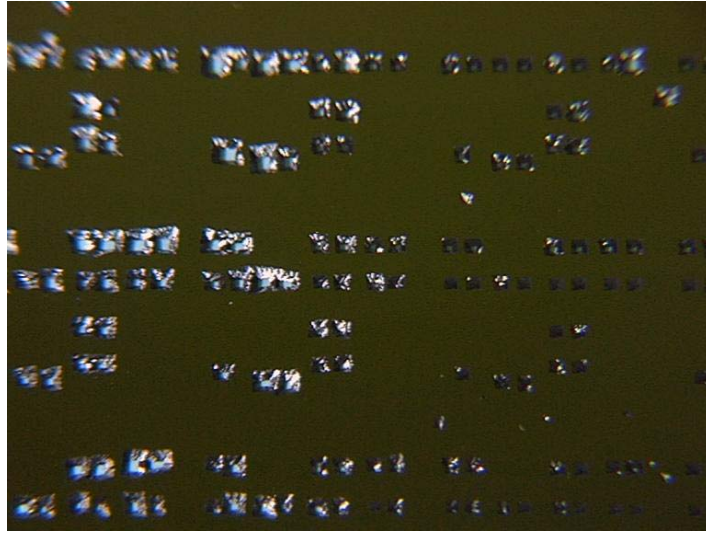


Figure 2.7.4 KOH-etched through-wafer vias.

RF MEMS wafer level vacuum packaging offers a fertile area for future work. The development of a low loss, low capacitance, high frequency RF interconnect is key to its success. Furthermore, a redesign of the RF MEMS resonator chip into a wafer-level packageable format with seal ring is recommended in any future work.

3. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The goal of Vacuum Packaging for MEMS Program was the development of an integrated set of packaging technologies which in totality provide a low cost, high volume product-neutral vacuum packaging capability which addresses all MEMS vacuum packaging requirements. These include inertial MEMS (accelerometers, gyros); IR MEMS (uncooled detectors and high speed IR sources); and RF MEMS (filters and resonators). Vacuum level of less than 10 mTorr is required in some applications.

The product-neutral vacuum packaging strategy employed each team member's respective technology thrusts to achieve comprehensive low cost, product-neutral MEMS vacuum packaging. The program balanced the need for near term wafer-level vacuum packaging with the development of advanced high density wafer-level packaging solutions. The two near term approaches demonstrated by Raytheon under the program included large area component level vacuum ceramic packaging and 4"/6" wafer-level vacuum packaging

The large area component level ceramic vacuum packaging approach involves a large cavity (0.7" x 0.7") 84 pin ceramic package solder sealed to a germanium lid using AuSn solder. IR MEMS microbolometer vacuum packaging with sub 10 mTorr package vacuum was demonstrated. Inertial MEMS resonant accelerometer vacuum packaging with sub 200 mTorr package vacuum was also successfully demonstrated. An RF MEMS resonator vacuum packaging demonstration was also successfully carried out under the program.

The second near term vacuum packaging approach carried out by Raytheon was 4"/6" wafer-level vacuum packaging using the AuSn solder seal process. Under the program, 4" and 6" wafer-level IR MEMS vacuum packaging demonstrations were successfully carried out in which the required sub-10 mTorr package vacuum requirement was achieved. Also, periodic testing of an IR MEMS wafer-level vacuum package during the program indicated no degradation in package vacuum over the 38 month period during which the package was tested. The AuSn solder-seal 4"/6" wafer-level vacuum packaging approach developed by Raytheon was so successful, it was used to wafer-level package an uncooled amorphous silicon (a-Si) 120x160 focal plane array. This wafer-level packaged FPA was used in a low cost, low power micro infrared camera developed under the DARPA ANTS and FIS Programs. This is the first system demonstration employing a wafer-level packaged IR MEMS a-Si microbolometer FPA. In addition the IR MEMS microbolometer wafer-level vacuum packaging demonstrations, Raytheon also carried out an inertial MEMS wafer-level vacuum package demonstration using a UC Berkeley-designed, Sandia-fabricated resonant accelerometer/gyro chip.

Extensive MIL Standard environmental testing by AFRL on Raytheon IR MEMS and inertial MEMS packages was also carried out with substantial success. These tests included high temperature storage (150°C, 1000 hrs); temperature cycling (-65°C to 150°C, 1000 cycles); accelerated temperature/humidity (130°C/85%RH, 150 hrs); temperature /humidity (85°C/85%RH, 1000 hrs) and random vibration (9 g_{rms}, 1 hr). In addition, a Raytheon IR MEMS wafer-level vacuum package successfully survived a 10000-g shock test carried out by ARL in a simulated gun launch survivability test.

With regard to the Raytheon solder seal approach to wafer-level vacuum packaging, an area for future work involves the reduction in seal ring width thereby increasing die density on the wafer. The seal ring employed under this program was 0.035" wide. It is expected that with further development the seal ring could shrink to approximately 0.015" to 0.020".

The development of advanced high density wafer level packaging solutions were carried out by MIT and UC Berkeley. The focus of the MIT effort was the development of high density wafer level vacuum packaging processes. The focus of the UC Berkeley effort was the development of wafer-wafer transfer microshell vacuum encapsulation technology.

The goal of the MIT effort under this program was to demonstrate wafer-level vacuum sealing using gold thermocompression (TC) bonding to reduce seal ring width to 100 μm and to develop thru wafer interconnects to reduce real estate requirements for interconnects. The payoff of this high density wafer-level package development is lower cost production. Under the program, MIT achieved reliable gold TC bonding and did demonstrate vacuum bonding with a modest sub 0.15 ATM vacuum. However, MIT accomplished more than expected in developing a unique bond strength measurement protocol that is important for a wide range of bond strength measurements. MIT also demonstrated a thru wafer interconnect process. An area for future work is the implementation of the TC bond protocol together with the high density thru-wafer vias to complete a high density wafer-level vacuum packaging demonstration.

The second advanced wafer level packaging approach carried out by UC Berkeley employed a wafer-wafer transfer microshell vacuum encapsulation process. The microshell encapsulation process offers the potential for an ultrahigh density packaging process for ultralow cost, high volume MEMS applications. In addition, it offers the unique capability for multi-vacuum level packaging on a single chip thereby meeting the vacuum packaging requirements of multifilter/resonator RF MEMS and multiaxis or wide dynamic range inertial sensors for which the component MEMS may require different operating vacuum levels. While the UC Berkeley wafer-level microshell encapsulation vacuum packaging goal was not achieved under the program, the successful transfer at atmosphere of polysilicon and poly-SiGe hexsil encapsulation structures using thermocompression bonding was successfully demonstrated. An area for future work is to extend this demonstration to include a vacuum transfer process as originally intended under this program.

Also under the program, Raytheon attempted a quasi-wafer-level RF MEMS vacuum packaging demonstration using University of Michigan RF MEMS resonator chips. The key technical challenge in the RF MEMS wafer-level package demonstration was the development of a low loss, low capacitance, high frequency RF interconnect. While a full RF MEMS quasi-wafer-level vacuum packaging demonstration was not achieved, Raytheon did make progress in developing a form and function RF MEMS wafer-level package demonstration.

Finally, under the program Raytheon working with NSWC used its wafer-level packaging techniques to develop a MEMs Torpedo Fuzing/Safety & Arming System chip-level package assembly (System Insertion Activity involving NSWC/Raytheon). Raytheon initially delivered 27 silicon base test chip-to-ceramic initiator test chip assemblies to NSWC for environmental testing (thermal shock, mechanical shock and accelerated aging) after which Raytheon packaged and delivered 10 functional MEMS F/S&A chips to NSWC.

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