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*Sub-Threshold Silicon MESFETs with 25 nm Gate Lengths for  
Ultra High Speed/Low Power Information Processing*

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Introduction

Operating a field effect transistor in the sub-threshold regime has several advantages:

- the  $g_m/I_D$  ratio is maximized  $\Rightarrow$  highest bandwidth for a given current drive
- low drain voltage for current saturation i.e.  $V_d^{sat} \sim 3 kT/e$
- input noise resistance,  $R_N \sim 1/g_m$ , is also minimized for a given  $I_D$

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However, the performance of conventional sub-threshold circuits based on weakly inverted MOSFETs are severely limited by:

- poor transistor matching for short gate lengths  $\Rightarrow L_g^{\min} > 1 \mu\text{m}$
- low cut-off frequencies,  $f_T$
- lack of accurate device models and CAD tools
- susceptible to radiation damage and  $1/f$  noise

As a result, sub-threshold CMOS has not advanced since its development in the 1970s and is limited to low frequency applications such as digital watches and pocket calculators.

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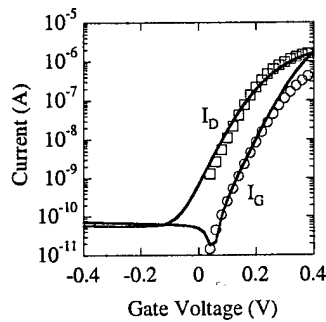
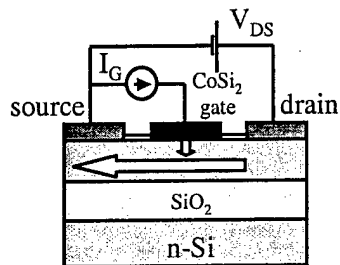


### Results

We have developed a new ultra-low power technology suitable for ultra-high speed/low power information processing – see references [1-3]

Based on a sub-threshold MESFET architecture we are calling the device a Schottky Junction Transistor (SJT). It requires no gate dielectric making it more radiation tolerant and easier to scale than a MOSFET. An input gate current  $I_G$  controls a much larger channel current  $I_D$  via a current gain,  $\beta \gg 1$ . The operating mode resembles that of a bipolar junction transistor but the SJT is a majority carrier device.

Measured data from a 2  $\mu\text{m}$  gate length SJT

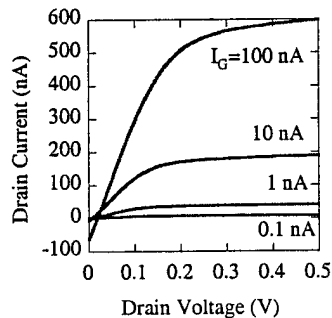


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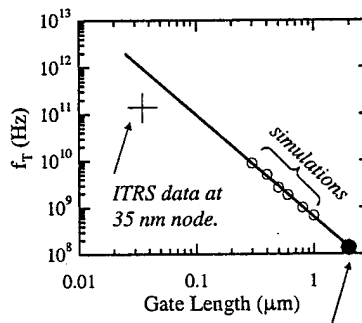


Data from prototype 2  $\mu\text{m}$  devices agree well with numerical simulations. When extended to the deep sub-micron regime cut-off frequencies significantly higher than that expected from the ITRS Roadmap are predicted

Measured SJT Family of Curves  
For  $L_G = 2$  microns



High Cut-off Frequencies for  
Drain Currents  $\sim 10^{-7}$  A



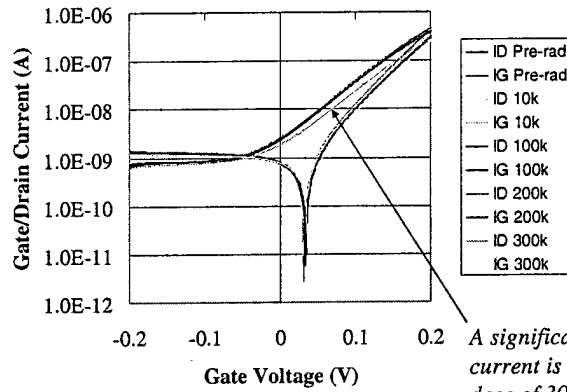
Measured result for  $L_G = 2$   $\mu\text{m}$  is  $\sim 10X$   
higher than an equivalent MOSFET

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### Preliminary Results Suggest the Device is Radiation Tolerant

Chip#2, Device#13 Gummel Radiation Variation



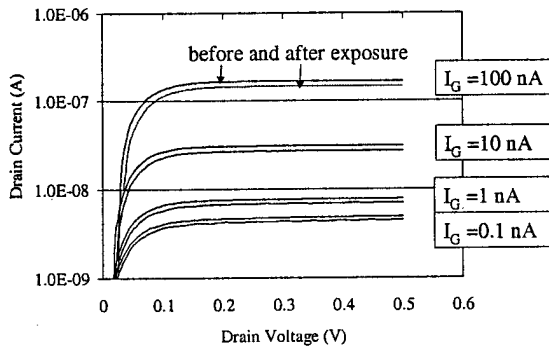
A significant shift in the drain current is only observed for a dose of 300 krad of 50 keV x-rays and can be attributed to bond pad leakage rather than degradation in the intrinsic device itself!

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### Family of curves before and after 300 kRads of 50 keV x-rays

Measured Family of Curves



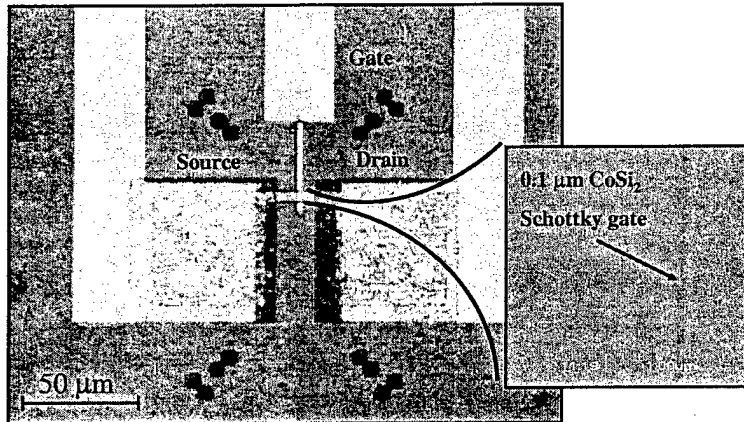
Device behavior is maintained even after moderately high radiation doses. Further improvement is possible by optimizing the layout.

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### Progress towards sub-micron devices

We have developed an electron beam lithography process for 0.1  $\mu\text{m}$  gate length SJs. Results from these devices will be used to calibrate the numerical models before moving to sub-100 nm devices



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### Conclusions

- Simulations indicate that sub-100 nm gate length SJs are capable of operating at frequencies larger than that required by the ITRS Roadmap
- Data from prototype SJs with gate lengths of 2  $\mu\text{m}$  agree well with the numerical simulations.
- The prototype devices demonstrate good radiation tolerance
- An electron beam lithography process has been developed for 100 nm SJs

### References

- [1] "The Schottky Junction Transistor – Micropower Circuits at GHz Frequencies" T. J. Thornton IEEE Electron Device Letters 22, 38-40 (2001)
- [2] "Physics and Applications of the Schottky Junction Transistor" T. J. Thornton IEEE Transactions on Electron Devices 48, 2421-2427 (2001)
- [3] "Schottky Junction Transistors for Micropower RFICs" J. Spann, Zhiyuan Wu, P. Jaconelli, Jinman Yang, T. J. Thornton Proc IEEE Radio Frequency Integrated Circuits, Seattle (2002)

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