CIRCUITRY FOR A WIRELESS MICROSYSTEM FOR NEURAL RECORDING MICROPROBES

Hao Yu, Khalil Najafi
Center for Wireless Integrated MmicroSystems (WIMS), The University of Michigan, MI, USA

Abstract-**Integrated circuits for use in a wireless microsystem used in neural recording is described. The implantable microsystem will be powered and transmit digitized data using RF telemetry. Recorded neural signals are amplified, multiplexed, digitized using a 2nd order sigma-delta modulator, and then transmitted to the outside world by an on-chip transmitter. The circuit is designed using a standard 1.5μm CMOS process. Several circuit blocks have been desgigned, fabricated and show to operate as expected.**
Keywords **- Telemetry, Microsystem, Sigma-delta, Microprobe**

I. INTRODUCTION

Direct recording of neural activity has been longed for by physiologists and scientists in order to unveil the secrets of biological neural networks, which may inspire the innovations in artificial intelligence, human physiology and biomedical prosthesis. The silicon micromachined microelectrode developed at the University of Michigan is one of the successful approaches to record the neural signals from the central and peripheral nerve systems [1]-[3,] and some efforts have been made to accomplish the above goal [4]-[6]. A low-power, wireless prototype of an integrated circuit chip is being developed for an implantable multi-channel recording microprobe for central nervous system. The integrated circuit chip is powered using RF telemetry by an external coil that is separated from the receiver coil by a distance of several millimeters. The chip allows recording of ±500 μV neural signals from axons regenerated through a micromachined silicon sieve electrode. These signals are amplified using pre-amplifiers, multiplexed, digitized with a 10-bit sigma-delta modulator, and then transmitted to the outside world using an on-chip transmitter. The circuit is designed using a standard 1.5μm CMOS process.

It is obvious that inductive RF power delivery and data transmission are desired in the design of the implanted recording microsystem to reduce potential hazards of interconnect wires and batteries to tissues in chronic recording applications. One of the main challenges of the required system is to transfer sufficient power to the implant and produce clean power supply needed for high-resolution recording and conversion to digital format of the recorded data.

II. SYSTEM OVERVIEW

The IC block diagram, shown in Fig. 1, illustrates the operation of the telemetry system.

A. Front-end circuitry

The front-end circuitry includes circuit blocks of voltage regulators, clock recovery, ASK demodulator, power-on-reset and RF limiter [7,8].

The front-end circuitry receives power and commands from the external transmitter so as to keep the implanted chip functional. It also recovers clock and reset signals for digital blocks as well as protect the on-chip electronics from high RF voltage.

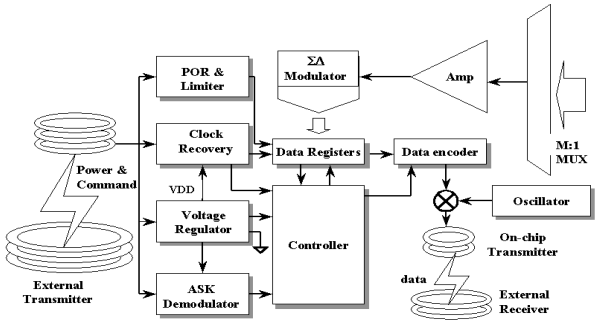

Fig. 1. Block diagram of a wireless microsystem for multichannel neural recording

B. Sigma-Delta Modulator (ΣΔM)

Ten bit or higher resolution is required in neural recording. However, RF power delivery may introduce high power supply noise to the implanted chip, which may be much higher than 0.1% required by 10 bit resolution. In order to achieve the high resolution, over-sampling method is chosen to implement the ADC [9,10]. In this application, a second order sigma-delta modulator was designed to sample the neural signals with a frequency of 2MHz, more than 64 times the neural signals' Nyquist rate of 20kHz [11].

C. Control logic and On-chip data transmitter.

The on-chip active transmitter is used to transmit the digitized data to the external receiver. Because the bandwidth of this transmitter sets the limit for recording data transmission, it is desirable to have a carrier frequency as high as possible[12,13]. The functions of the control logic include decoding the received commands from the front-end, selecting the corresponding probe and channel, controlling A/D and the internal transmitter.

III. CIRCUIT DESCRIPTION

A. Bandgap Reference and Voltage Regulator

A series regulator is designed to provide stable power supply to on-chip electronics, illustrated in Fig. 2.

The receiver coil, D1 and C1 form a half-rectifier. The opamp works in the negative feedback loop to adjust the current through the pass device Mpass so that the regulated voltage Vdd can keep constant. Note that the power supply of the bandgap reference[14] is from the output of the regulator rather than the output of the half-rectifier; this configuration can lead to more accurate and

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Abstract

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stable voltage reference. However, a startup circuit is needed to drive the circuit out of zero quiescent state.

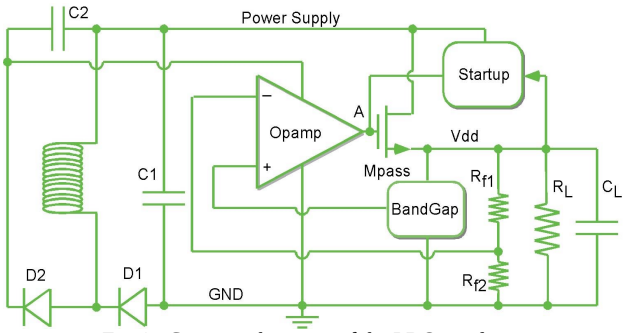

Fig. 2. Circuit architecture of the LDO regulator

A PMOS can also be used as the pass device and achieve low dropout, however, the common-emitter configuration may lead to instability problem when load capacitance C_L changes in a wide range [15,16]. In order to solve the high dropout problem associated with NMOS pass device, a simple voltage-doubling block, made up of C2 and D2, is used to provide higher supply voltage to the opamp, which consumes very low power.

B. ASK Demodulator

Since ASK is used in command transmission, the ASK demodulator was designed to decode the commands from the modulated RF signal. Fig. 3 shows the circuit schematic of the ASK demodulator [17]. P01 and P02 are matched transistors, while the capacitances of C1 and C2 are much different, therefore, the responses of the two low-pass filters, formed by (P01,C1) and (P02,C2), to the same amplitude shift across the receiver coil are much different. The succeeding comparator senses the difference and generates the demodulated command bits. The ratio P1:P3 is set to be larger than one to provide hysteresis, so is the ratio P2: P4.

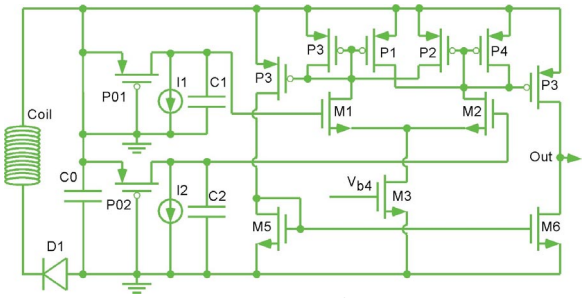

Fig. 3. The circuit schematic of ASK demodulator

C. Clock Recovery Circuit

The schematic of the clock recovery circuitry is shown in Fig. 4, where NMOS P0 with long channel length is used as a resistor. If the coil receives the sinusoid RF signal, the waveform at the gate of M2 is a sinusoid with the average of 1.65v, it is then compared with 1.65v to regenerate the clock signals. The second stage of the comparator uses a latch-type differential stage, where the transistors M3 and M4 switch the current sources so that current only flows during transition phases to reduce power consumption.

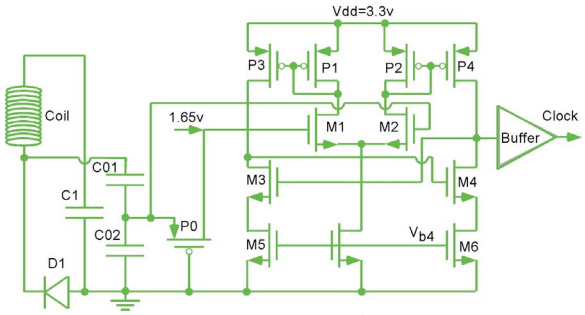

Fig. 4. The circuit schematic of clock recovery

D. RF Limiter

The induced voltage across the receiver coil may exceed 15V under the condition of short distance from the external transmitter and large load impedance, which may cause breakdown of the implanted electronic circuits. A RF limiter, shown in Fig. 5, can be used to prevent breakdown. When the induced voltage exceeds a specific value, the RF limiter begins to sink a large amount of current so as that the induced voltage will not rise too high.

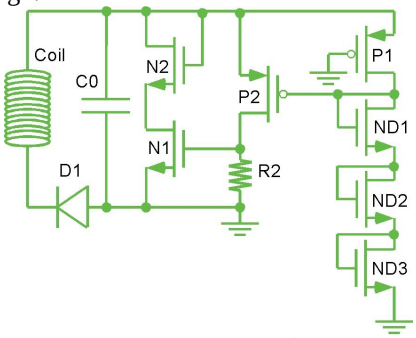

Fig. 5. The circuit schematic of RF limiter

E. Sigma-Delta Modulator

Oversampled sigma-delta A/D converters have the advantage that they trade greatly reduced analog circuit accuracy requirements for increased digital circuit complexity. This converter only requires a single-bit A/D and D/A converter with a relatively inaccurate differential summing amplifier and integrator. These analog circuits are much easier to implement in a digital VLSI circuit than the accurate analog circuits required in flash or algorithmic A/D converters that require precise resistors or capacitors. In addition, the power supply noise can limit the accuracy of the flash or algorithm A/D converters, while it does not affect the accuracy of sigma-delta A/D converters. By trading off between the costs and requirement, a second order $\Delta\Sigma$ modulator is

chosen in this 10-bit resolution application. The block diagram of a second order sigma-delta modulator is illustrated in Fig. 6. G1, G2 are the gains of the first and second summing amplifiers respectively, and they are also the scale factors of the modulator. G1 and G2 are chosen to be 0.2 to ensure that the two integrator outputs mostly vary within the normal output range of the practical opamp. The circuit is shown in Fig. 7.

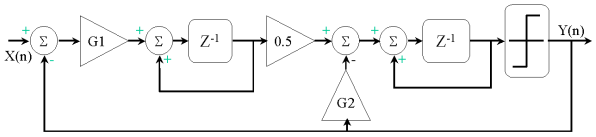

Fig. 6. The block diagram of the 2nd order sigma-delta modulator

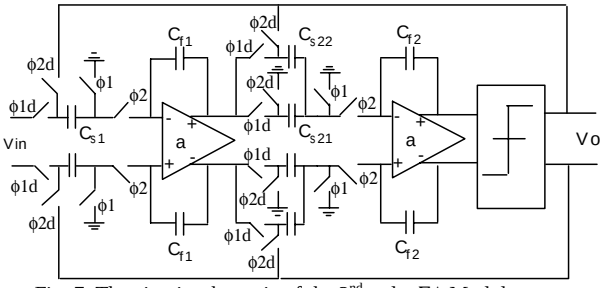

Fig. 7. The circuit schematic of the 2nd order ΣΔ Modulator

Fully differential Operational Transconductance Amplifiers (OTA) are used in the modulator because they help to increase the circuit's power supply ripple rejection as well as the dynamic range. Common-mode feedback is necessary to define the DC voltages at the high impedance output nodes of the fully differential OTAs. In this application, a switched capacitor common-mode feedback is used because of its good linearity and low power consumption. Simulation results are shown in Fig. 8, where the spectrum of the reconstructed waveform is compared with that of the original 2kHz sinusoid input to ΣΔM. The input and reconstructed spectra match each other quite well. (The DFT is based on 100 even samples in 4 cycles.)

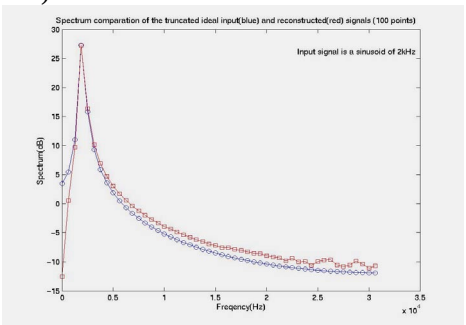

Fig. 8. The spectra comparison of input and reconstructed signals

F. On-chip Data Transmitter

A ring oscillator was used in the on-chip data transmitter design, because it is the fastest oscillator available on chip. Simulation result shows that the oscillation frequency can exceed 100MHz in standard 1.5um CMOS process. An ASK, OOK (On-off keying), can be used to modulate the transmission of recorded data. The advantage is there is no oscillation during off period, which may save the power consumption by 50%.

IV. MEASUREMENT RESULTS

A prototype front-end circuit was fabricated and tested in a a double-poly, double-metal, n-well AMI1.5um CMOS process. The test circuit consisted of voltage regulators, clock recovery block and Power-On-Reset. The photograph of the chip is shown in Fig. 9.

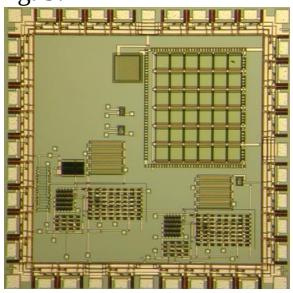

Fig. 9 The photograph of the fabricated chip

All four chips function as expected. The line regulation is better than 2mV/V when the input voltage swings from 8V to 13V, shown in Fig. 10.

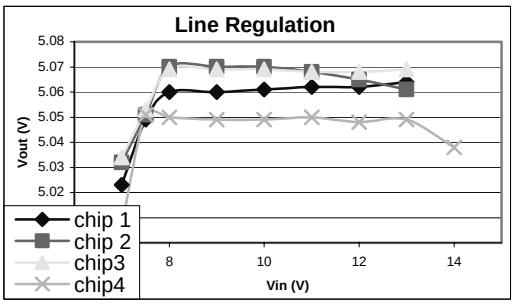

Fig. 10. The measured line regulation

The load regulation is better than 4mV/mA for all four chips, shown in Fig. 11.

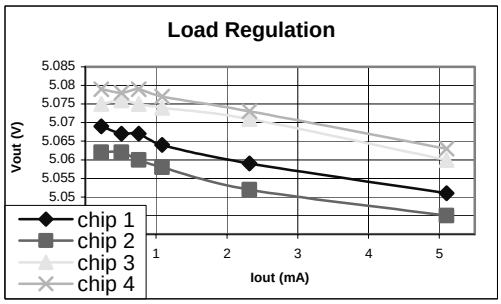

Fig. 11. The measured load regulation

Ripple rejection ratio of the regulator is 46dB at 4MHz, which can be seen from Fig. 12. At 4MHz, the input ripple of the regulator is 2V(p-p); the output ripple is 10mV(p-p).

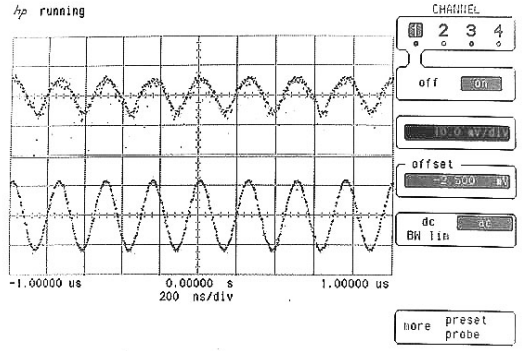

Fig. 12. Measured ripple rejection of the regulator

The bandgap voltage reference presents better stability than the regulator output. It changes less than 5mV as long as the half-wave rectifier output exceeds 6.5V. POR and clock recovery circuitry are relatively simple and all function as expected. A summary of the measured circuit performance is listed in Table I.

TABLE I
Measured performance of the front-end circuits

Circuit Block	Power Consumption	Die Size (μm^2)	Specifications
Voltage Regulator	460uW	500x500	Load Regulation: **4mv/mA** Line Regulation: **2mv/v** Ripple Rejection: **46dB**
BandgapReference	40uW	150x100	Vref= 1.262v
POR	0 after Reset	60x100	T_{reset} = 70us-150us
Clock Recovery	350uW	120x100	Frequency = 4MHz
ASK demodulator	130uW	350x100	----

The Sigma-Delta modulator, internal data transmitter were designed and they are being fabricated in MOSIS.

V. CONCLUSION AND FUTURE WORK

A wireless microsystem for neural recording microprobes has been presented. The system includes three major functional blocks, front-end, sigma-delta A/D, control logic and on-chip data transmitter. The front-end block receives the RF signals from the external transmitter, then generates the regulated power supply, recovers the clock and command data for internal control circuits. The prototype front-end circuit shows satisfactory measurement results. The 2nd order sigma-delta A/D converter was designed to achieve 10-bit resolution under the condition of relatively large power supply noise. The data transmitter was implemented to return the digitized data to the external world and control logic is capable of command decoding, channel selecting and transmission controlling. The whole prototype microsystem is being fabricated and waiting for the testing in the future.

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