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THESIS

DC-DC POWER CONVERSION WITH GALVANIC ISOLATION

by

Jason A. Zengel

June 2003

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As the navy transitions to all electric warships, there will be many changes to the power distribution schemes found aboard ships today. It will be necessary to maintain reliability while supplying the various components onboard with the proper voltage levels. Since transformers cannot be used to alter voltage levels while providing galvanic isolation in DC power systems, it is necessary to find an efficient method to incorporate the increased safety provided by galvanic isolation in a DC power distribution system. This thesis examines the design and control of one possible element for a future Electrical Distribution System (EDS), a DC-DC converter with galvanic isolation. The main purpose of this study is to provide a working model with associated theoretical proof and simulations. MATLAB will be used to provide observations of the converter's operation and the success of the control scheme implemented. Future work on this topic will be assisted by the inclusion of a parts list as well as recommendations for enhancing the prospects of this technology.

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DC-DC POWER CONVERSION WITH GALVANIC ISOLATION

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ABSTRACT

As the navy transitions to all electric warships, there will be many changes to the power distribution schemes found aboard ships today. It will be necessary to maintain reliability while supplying the various components onboard with the proper voltage levels. Since transformers cannot be used to alter voltage levels while providing galvanic isolation in DC power systems, it is necessary to find an efficient method to incorporate the increased safety provided by galvanic isolation in a DC power distribution system. This thesis examines the design and control of one possible element for a future Electrical Distribution System (EDS), a DC-DC converter with galvanic isolation. The main purpose of this study is to provide a working model with associated theoretical proof and simulations. MATLAB will be used to provide observations of the converter's operation and the success of the control scheme implemented. Future work on this topic will be assisted by the inclusion of a parts list as well as recommendations for enhancing the prospects of this technology.

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EXECUTIVE SUMMARY

A 10-kHz DC-DC converter with galvanic isolation has been designed in order to display the feasibility of efficiently achieving galvanic isolation while changing voltage levels within an EDS. The Naval Research Advisory Committee (NRAC) has concluded that future naval vessels will become all-electric. In order to facilitate the varying power needs of shipboard components in an all-electric warship, a future EDS must house several conversion devices. The purpose of this thesis is to provide both a design and a working model of one such component, the Ship Service Converter Module (SSCM).

The full-bridge converter designed in this thesis consists of the following major components: an inverter, a high frequency transformer, and a full-bridge rectifier. The inverter portion of the converter consists of Insulated Gate Bipolar Transistors (IGBT), protective diodes, an inductor, and associated control circuitry. The high frequency transformer uses a METGLAS core to limit eddy current losses and Litz wiring to lower skin-depth concerns in the primary and secondary windings. The full-bridge rectifier uses diodes to create a DC output that is smoothed using a capacitor in parallel with the load.

The converter design began by selecting arbitrary input (500 V DC) and output voltages (300 V DC). Next, a load range (37.5 Ω – 112.5 Ω) was selected to display the converter's ability to handle load fluctuations. By treating the components as ideal and selecting a modified square mode control scheme for the inverter, standard buck-chopper equations defined the system's operation. A minimum capacitance of 17 μF, a minimum inductance of 0.75 mH, and a duty cycle of 60% were all calculated; however, a minimum capacitance of 100 μF was necessary to achieve a viable transient response.

The DC-DC converter was unable to operate properly without the addition of a controller. A proportional-integral-derivative (PID) controller was chosen due to its success in controlling prior buck-choppers designed by Naval Postgraduate School (NPS) students. Sensing equipment that monitored the output voltage, inductor current, and load current provided the input to the controller. The controller than calculated an asso-

ciated duty cycle that was fed to the Pulse-Width Modulation (PWM) chip in order to properly fire the IGBTs.

The operation of the converter was simulated using MATLAB across the entire load range. The bode plots, step responses, and frequency responses are all presented as an illustration of the converter's successful operation. The efficiency of the converter was calculated to be greater than 95%. The actual operation of the converter should come close to mirroring the theoretical calculations due to the wealth of prior data on related systems.

This research proves that a SSCM can achieve galvanic isolation needed for increased safety and reliability without a significant loss in operational efficiency. Future research on this converter should be done in order to further validate the findings contained in this thesis. Future research should start by constructing the converter designed in this thesis and testing the operation of the converter under various circumstances. Also, efficiency can be improved by either more complex control schemes of the inverter portion of the converter or use of a more involved full-bridge rectifier. Finally, the transformer design could be further studied to improve the converter's operation.

I. ELECTRICAL DISTRIBUTION SYSTEMS

A. INTRODUCTION

This chapter provides a background into the current state of naval power distribution onboard naval vessels. This chapter will serve to illustrate the advantages of using a new architecture for power distribution. The converter that is studied in this thesis will be introduced, and the converter will improve the reliability of any future power distribution system chosen by the United States Navy.

B. RADIAL ALTERNATING CURRENT ELECTRICAL DISTRIBUTION SYSTEM

The Electrical Distribution System (EDS) employed by current naval vessels has been relatively unchanged since the 1940s. The EDS relies on multiple redundancies with many protective features and is known as a radial architecture [1]. The system attempts to maintain power flow to vital loads even with several casualties simultaneously taking place. Primary power originates from Ship's Service Turbine Generators (SSTG) that produce 460 V, 60 Hz, Alternating Current (AC). Either Diesel Generators (DG) (surface vessels) or batteries (subsurface vessels) can supply power if a SSTG experiences a casualty.

The power supplied by the SSTG's is fed to distribution switchboards that serve as centers for distribution of power. Power then flows from the distribution switchboards to various load centers that contain the ship's electrical loads. The distribution switchboards have either vital or non-vital loads. Vital loads are loads that are necessary for the ship to communicate, maneuver, or defend itself while non-vital loads encompass the remaining loads.

The EDS attempts to maintain power to vital loads at all times. Several redundancies and protections are built into the EDS to provide greater reliability. All vital load switchboards are powered by at least two sources. The switchboards are also capable of supplying power to one another if needed. Automatic Bus Transfers (ABT) sense when power is being disrupted to vital loads and then act to provide power from an alternate

source [1]. For instance, if a SSTG (primary source of power to a vital load switchboard) was to be lost, the ABT would supply power from the DG (secondary source of power to a vital load switchboard).

The EDS has many protective features that also attempt to isolate damage and increase reliability. Circuit breakers are used to remove power from a load that is drawing excess current prior to the faulty load damaging the entire EDS. Fuses are used to isolate faults even further from electrical distribution switchboards.

The current EDS that the United States Navy employs is known as the radial system due to the manner in which the loads receive power from various places through many wires. The amount of wiring needed to maintain high reliability with a radial EDS also has many drawbacks. When wires carry power from one compartment in a ship to another compartment, the watertight integrity of the ship is lowered. Bulkhead penetrations should be minimized as often as possible, but they are a necessity in a radial EDS. Excess wiring also adds weight, cost, and maintenance to a naval vessel. Figure 1 illustrates a simplified example of a current naval EDS [2].

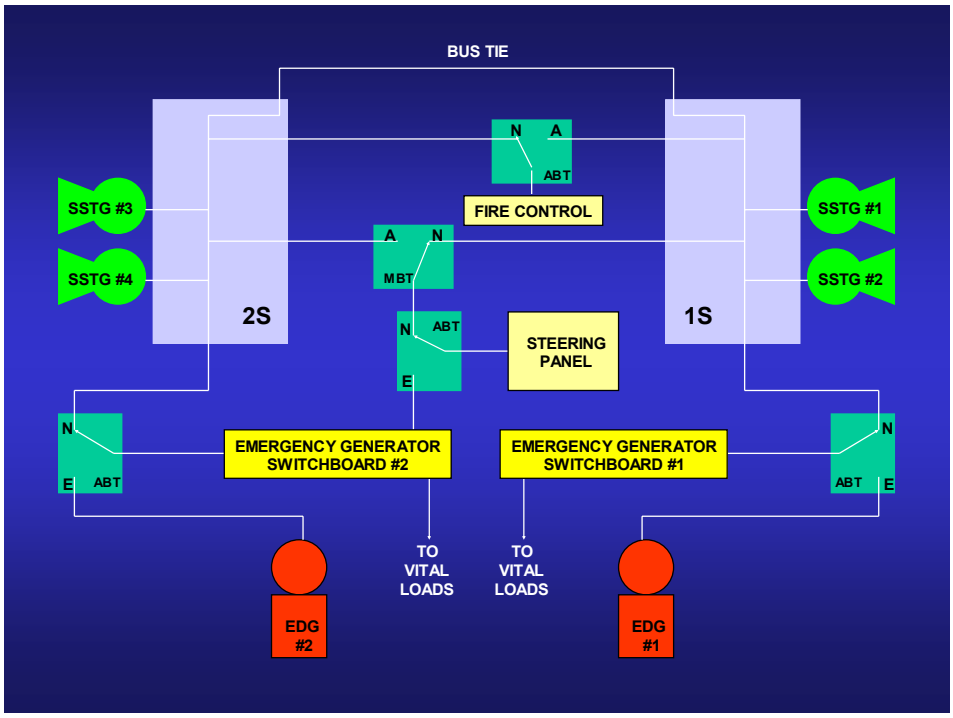

Figure 1. Simplified Example of Current Naval EDS. (From Ref. [2].)

C. DIRECT CURRENT ZONAL EDS

Current research taking place investigates the advantages of using a Direct Current Zonal EDS (DCZEDS) in future naval vessels. The DCZEDS will need to maintain high reliability in battle conditions to become a viable solution to the Navy. There are many advantages to DC power that will be discussed later; however, there are also several disadvantages associated with using DC power.

The DCZEDS (see Figure 2) will most likely be powered by gas turbines like General Electric's LM-2500 (PS in Figure 2). The gas turbines will serve as the prime mover for an AC generator whose output will be immediately converted to DC by a Ship's Service Converter Module (SSCM) [1]. The DC output of the SSCM will provide power to both the port and starboard main busses. The port and starboard main busses are supplied by at least two power sources to provide increased reliability to the EDS.

The port and starboard busses will run down each side of the naval vessel creating only one bulkhead penetration per compartment. One main bus will be located above the waterline while the other bus will be located below the waterline. The DC voltage supplied by one of the two main busses will be stepped-up or stepped-down to the appropriate voltage needed to supply a load bank. Loads can then be taken directly off the load bank if they are DC and operate at the voltage present on the load bank. A Ship's Service Inverter Module (SSIM) is needed in order to invert DC into AC to supply loads that need AC to function [3]. Additional step-up or step-down converters are needed to supply loads off of a load bank if the voltages needed are at a different level than that of the load bank.

Circuit breakers and fuses can supply over-current protection and fault isolation in the DCZEDS as in the AC Radial EDS (ACREDS); however, in order to prevent cascading faults, each individual load must be protected in such a manner. Electrical isolation is achieved in AC by use of transformers, but transformers cannot be used in DC power systems.

Since DC cannot utilize a transformer, a converter module must be used every time it is desired to change the level of voltage. There is extensive data available to prove that the use of a converter such as the "buck chopper" is highly efficient and reli-

able. Most research being done for DCZEDS incorporates various converters to achieve desired voltage levels. Although modern converters are highly efficient, they cannot match the efficiency of an AC transformer when altering voltage. Figure 2 illustrates a simplified example of a DZEDS [1].

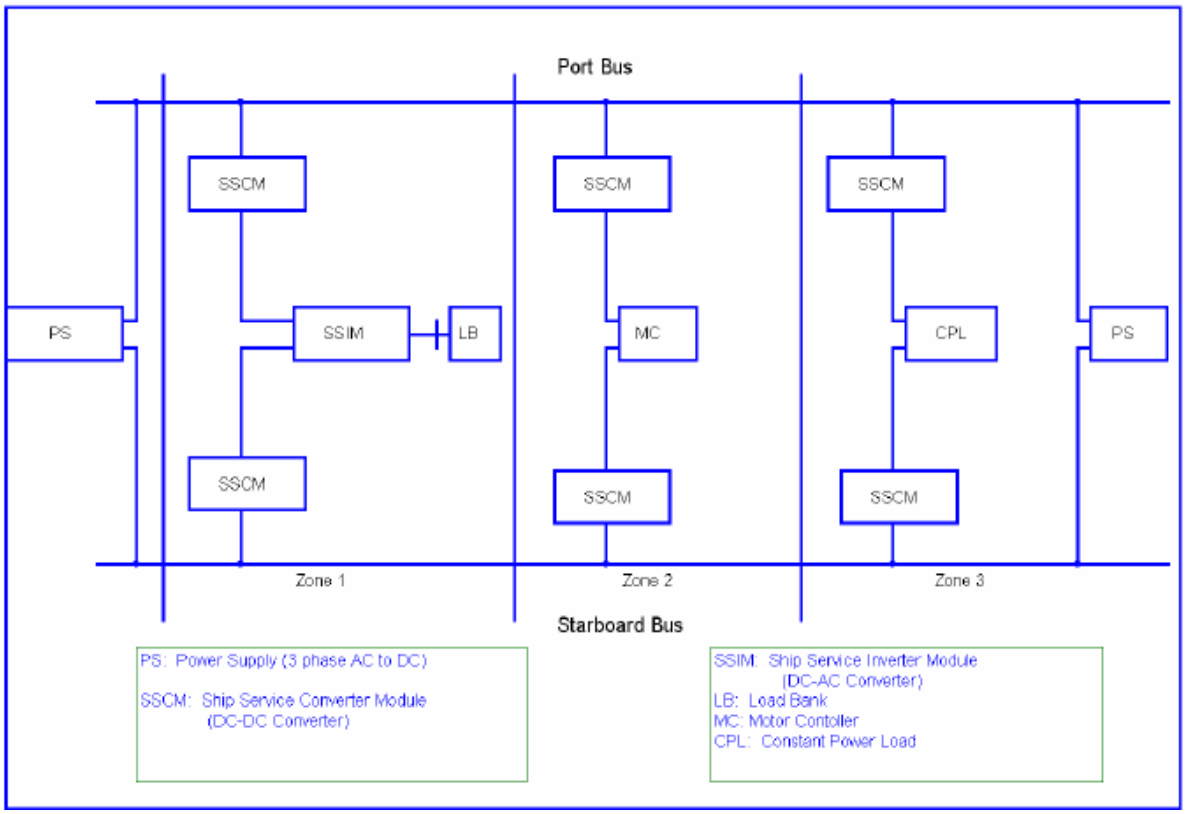

Figure 2. Simplified Example of DCZEDS (From Ref. [1].)

D. ADVANTAGES AND DISADVANTAGES OF RADIAL VERSUS ZONAL

Although the decision to replace AC with DC has not been made, the decision to use zonal architecture to replace radial architecture has widely been accepted. Zonal architecture has many advantages and few disadvantages over radial architecture. Table 1 illustrates the weight reductions realized by switching from a radial to a zonal EDS, and Table 2 shows the cost comparison for a radial and zonal EDS. The following is a list of advantages that using a zonal EDS will provide:

- Less overall weight,
- Less complicated circuit tracing,

- Improved watertight integrity,
- Less maintenance,
- More cost effective to produce,
- Increased crew safety, and
- Improved ship survivability.

Apparatus	Removal (LT)	Install (LT)	Net Change (LT)
Foundation	3.3	4.3	+1.0
Power Cables	116.7	79.8	-36.9
Switchgear	20.8	20.0	-0.8
Total	**140.8**	**104.1**	**-36.7**

Table 1 Zonal vs. Radial EDS Weight Comparison (From Ref. [4].)

Apparatus	Radial (Material and Labor)	Zonal (Material and Labor)
Foundation	34k	44k
Power Cables	4,151k	2,839k
SWBD and Load Centers	1,807k	1,736k
Total	**5,992k**	**4,619k**

Table 2 Zonal vs. Radial EDS Cost Comparison in Dollars (From Ref. [4].)

There are several disadvantages inherent in switching to a zonal EDS that must be addressed:

- Little operational data,
- Large initial design costs, and
- Costs for training overhaul for crew.

While these problems arise with any major change in military hardware, it is still something that must be examined. There has been significant research done to show that the benefit of switching to a zonal architecture far outweighs the disadvantages.

E. AC VERSUS DC EDS

The decision to replace the current AC EDS with a DC EDS has had recent set-backs. In transitioning from theory to practice, a primarily DC EDS has lost some of its appeal. Initial claims of higher efficiency and improved survivability have been largely discounted. In fact, the use of converters in a primarily DC EDS will provide an efficiency disadvantage when compared to an AC EDS. Also, there has been no proof that a switch to a DC EDS will increase survivability. Claims of less noise signature due to the lack of a 60-Hz cyclical hum in DC systems neglect important facts. The noise signature emanating from the many DC-DC converters necessary in an all DC EDS will be as harmful, if not worse, than the 60-Hz hum present in an AC EDS. Current proposals appear to trending towards a hybrid AC zonal EDS, and Figure 3 shows the most current proposal for the next generation EDS [5].

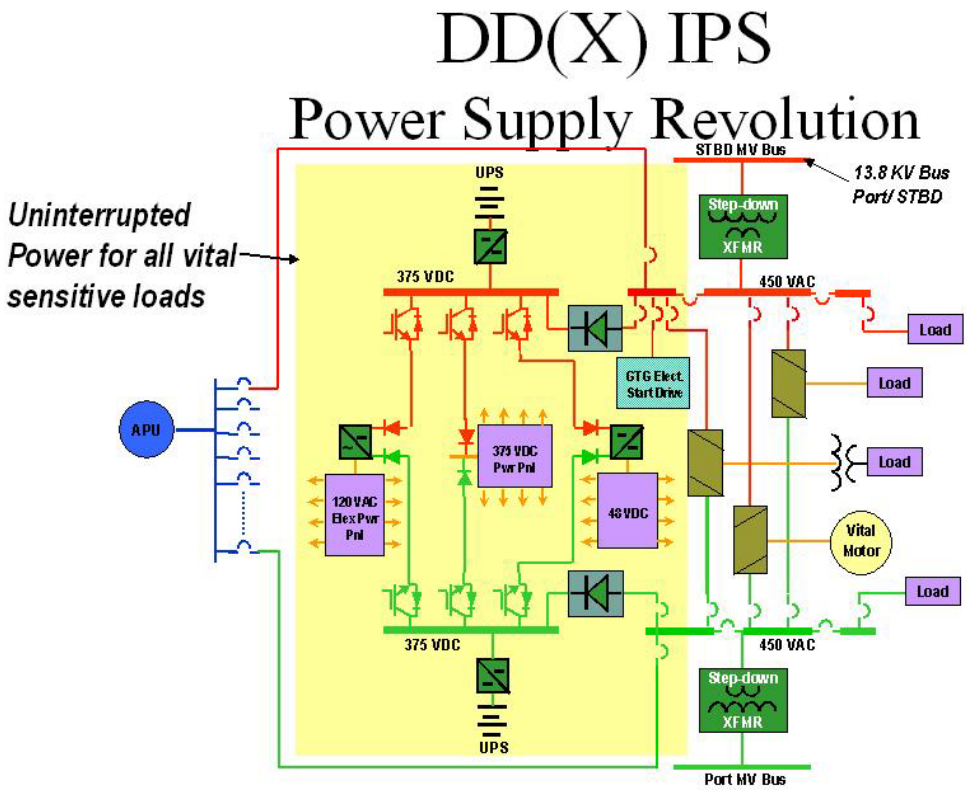

Figure 3. Hybrid AC Zonal EDS (From Ref. [5].)

Figure 3 can be broken down into several major parts. There are port and starboard main buses that operate at 13.8 kV AC. The main busses have their voltages

stepped down to 450 V AC to supply power to switchboards. The various AC loads onboard the ship can draw their power from the 450 V AC switchboards. A rectifier will convert the power from the 450 V AC switchboards to 375 V DC in order to power DC switchboards. The 375 V DC switchboards will power the DC loads onboard the ship, and a SSCM will be needed in order change the DC voltage levels from the 375 V DC switchboards. An auxiliary power source (APU in Figure 3) will provide a source of emergency power should the primary source of power to the main busses be interrupted.

F. THESIS OVERVIEW

This thesis shall examine methods of achieving galvanic isolation between the primary and secondary side of a Full Bridge Converter (FBC). Since transformers are not a viable option of separating sources and loads in DC, it is necessary to find another method of achieving galvanic isolation. This thesis shall center on the approach of inverting DC to AC, using a transformer, and then rectifying the power back into DC. Although this method may seem complex and rather inefficient, it will be illustrated that such an approach is both simple and efficient.

Either rectified AC output of an AC generator, or DC power from a DC bus, will be supplied to the primary side of the FBC. The primary side of the converter will consist of a DC-AC inverter that will invert the DC voltage into a pseudo-sinusoidal AC voltage. The pseudo-sinusoidal AC voltage will then enter the primary side of a transformer where the voltage will be "stepped-down" to a lower voltage. The "stepped-down" voltage will then be rectified using a full-bridge rectifier. The output of the rectifier will then be smoothed into a constant DC output by the use of a large capacitor.

G. CHAPTER OVERVIEW

Chapter II provides an overview of how the FBC operates. The converter will be broken down into the three major parts and each part will be described in greater detail. Chapter III uses state-space analysis to derive the equations necessary to simulate the performance of the converter. Once the system is modeled via a system transfer function, prior work done at Naval Postgraduate School (NPS) Monterey, California shall be refer-

enced to provide a suitable means to control the converter. Chapter IV will provide an example of a FBC. Finally, Chapter V discusses simulation results, draws conclusions, and provides some recommendations for further related research.

II. FBC ANALYSIS

A. PURPOSE

There are several available methods for galvanically isolating a DC source from a DC load. Each method has some relative advantages, as well as disadvantages, over another method. This thesis serves to examine a possible solution for the SSCM for a future naval EDS. After the method is chosen, the components of the topology will be discussed in this chapter.

B. AVAILABLE CONVERTER TOPOLOGIES

1. Flyback Converter

The flyback converter shown in Figure 4 was the first DC-DC converter examined [6]. DC voltage is applied to the left side of Figure 4, and an electronic switch (labeled Q1 in Figure 4) will control current flow. When Q1 is turned on, current will flow through the primary side of the flyback transformer producing the primary side current waveform shown in Figure 4. Current then exits the secondary side of the transformer and travels through the diode labeled CR1 to the load. When Q1 is turned off, there is no path for current flow. The primary and secondary side current waveforms are triangular, and they are shown in Figure 4.

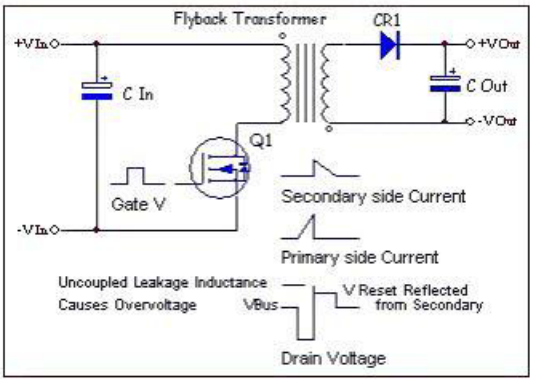

Figure 4. Flyback Converter (From Ref. [6].)

The flyback converter is one of the more simple methods of galvanically isolating a DC source from its load [6]. The converter is derived from the buck-boost converter that is used to "step-up" or "step-down" voltage without galvanic isolation [7]. This topology falls under the unidirectional core excitation category of DC-DC converters with galvanic isolation since the transformer uses only the positive part of the flux curve (quadrant 1) [7].

This converter is best suited for low power applications because of the triangular current waveforms shown in Figure 4 that form on the primary side of the transformer during operation [6]. These triangular waveforms cause high losses on the primary side as well as a high ripple current and high ripple voltage on the secondary side [6]. This converter is not suited for use as a high power SSCM.

2. Forward Converter

The next converter studied was the forward converter that is shown in Figure 5 [8]. DC voltage (V_{IN}) is applied to the left side of Figure 5, and an electronic switch (SW in Figure 5) controls the current flow. After SW is turned on, current flows through the primary side of the transformer causing a buildup of flux on the primary side of the transformer. After sufficient flux is built up on the primary side of the transformer, current will flow out of the secondary side of the transformer and through the load that is on the right side of Figure 5. When SW is turned off, the inductor on the secondary side will cause current to continue to flow through the load using the recirculating diode (D2 in Figure 5).

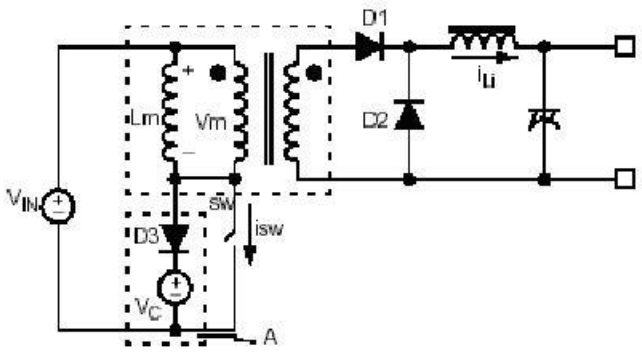

Figure 5. Forward Converter (From Ref. [8].)

The forward converter operates very similar to a buck chopper [7,8]. This converter is also unidirectional, and the converter has some design considerations that make it non-ideal for use as a SSCM. The converter must use demagnetizing coils (Lm in Figure 5) in order to prevent converter failure from energy storage in the transformer [8]. This converter will have additional losses from the leakage currents in the extra coils.

3. Push-Pull Converter

After eliminating the forward converter as a possible solution, the push-pull converter shown in Figure 6 was examined [9]. DC voltage is applied to the left side of Figure 6 (V_{in} in Figure 6), and the two electrical switches (T1 and T2 in Figure 6) control current flow through the converter. When T1 is turned on, current flows through the top portion of the primary side on the center-tap transformer, and current will exit the secondary side of the center-tap transformer and flow to the load through D1. When T1 is turned off, T2 will be switched on causing current to flow through the bottom portion of the primary side of center-tap transformer. Current will then exit the bottom portion of the secondary side of the center-tap transformer through D2 and to the load. An output filter consisting of an inductor and a capacitor will cause the output signal to be both continuous and smooth.

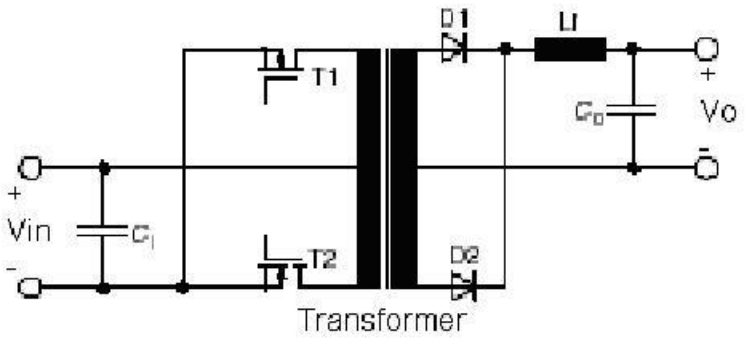

Figure 6. Push-Pull Converter (After Ref. [9].)

Power limitations of the center-tap transformer prevent the use of the push-pull converter at high powers. This converter provides a relatively small voltage ripple on the output while operating efficiently; however, this converter is not suited for high power operations, due to the power limitations of the center-tap transformer, and is not plausible as a SSCM [9].

4. Half-Bridge Converter

The Half-Bridge Converter (HBC) shown in Figure 7 was studied following the push-pull converter [10]. DC voltage is applied to the left side of Figure 7, and electrical switches (T1 and T2 in Figure 7) are used to control current flow. When switch T1 is turned on, current flows through T1, through the top of the primary side of the transformer, out the secondary side of the transformer, through the full-bridge rectifier, and to the load. When T1 is turned off, and T2 is turned on, current flows through the bottom of the primary side of the transformer, out the secondary side of the transformer, through the full-bridge rectifier, and to the load. An output filter consisting of an inductor and a capacitor creates a smooth and continuous output signal.

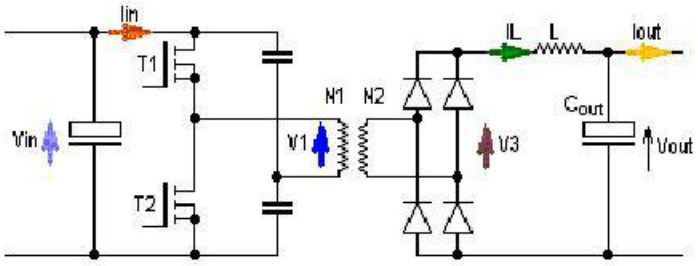

Figure 7. Half-Bridge Converter (From Ref. [10].)

This converter has many advantages over the previous converters, but is not suited for high-power operations. The power limitations of the electrical switches prevent the use of the HBC in high-power operations. By introducing another set of electrical switches, the HBC can become a FBC that is able to handle higher powers.

5. FBC

The Full Bridge Converter (FBC) is the proper topology for high power DC-DC power conversion with galvanic isolation and is shown in Figure 8. The operation of the FBC will be analyzed in great detail later in this chapter as well as in Chapters III and IV of this thesis. This converter is able to handle the high power levels needed to operate

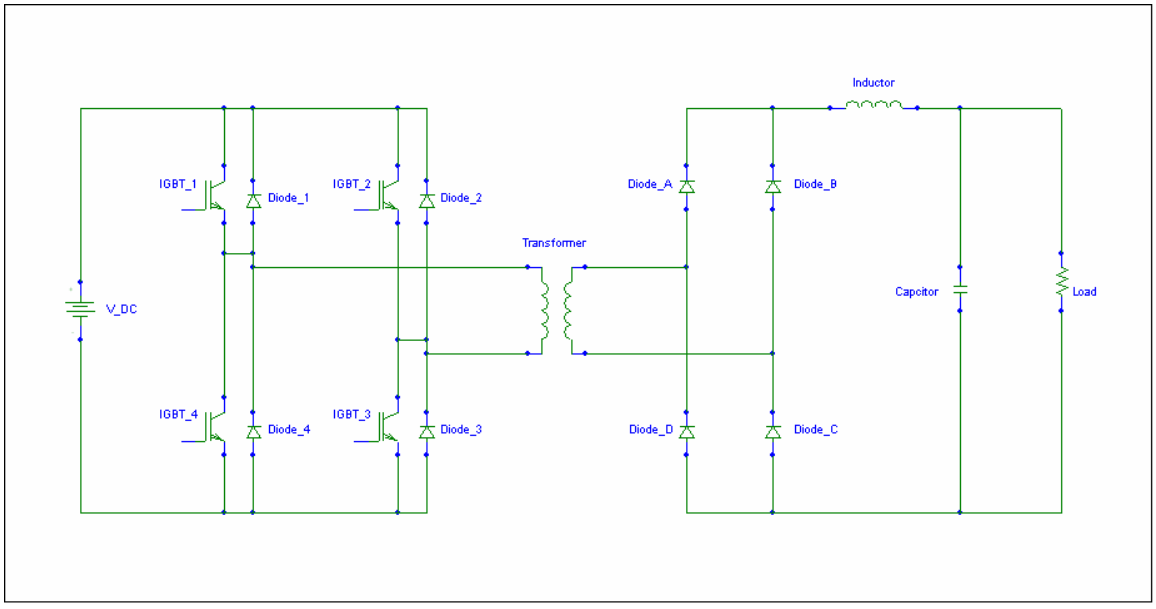

Figure 8. Full Bridge Converter

as a SSCM while also operating efficiently [7,9]. This topology also allows for prior research done at NPS on "buck choppers" to be utilized if it is operated in a select manner. The control scheme needed to ensure reliable and successful operation can also be derived with minor alterations from prior work at NPS.

The FBC converter can be modified in order to raise efficiency. The FBC can be operated in a resonant manner by including capacitors in parallel with the Insulated Gate Bipolar Transistors (IGBT) and an inductor in series with the load. Operating efficiency can be improved at the cost of complicating the control scheme and the additional components. Each additional component lowers the converter reliability and increases the troubleshooting difficulty. The increase in cost, the lowering of reliability and the complication in operation make the resonant converter less ideal than the standard FBC.

C. INVERTER PORTION OF FBC

1. Purpose

The inverter portion of the FBC is the most complex and important portion of the whole circuit. The inverter will receive its input from the rectified output of a SSTG or from a DC supply bus. The DC input is then inverted to provide a pseudo sinusoidal output that will be fed into the primary side of the transformer portion of the FBC. The inverter portion of the FBC is highlighted on the left side of Figure 9.

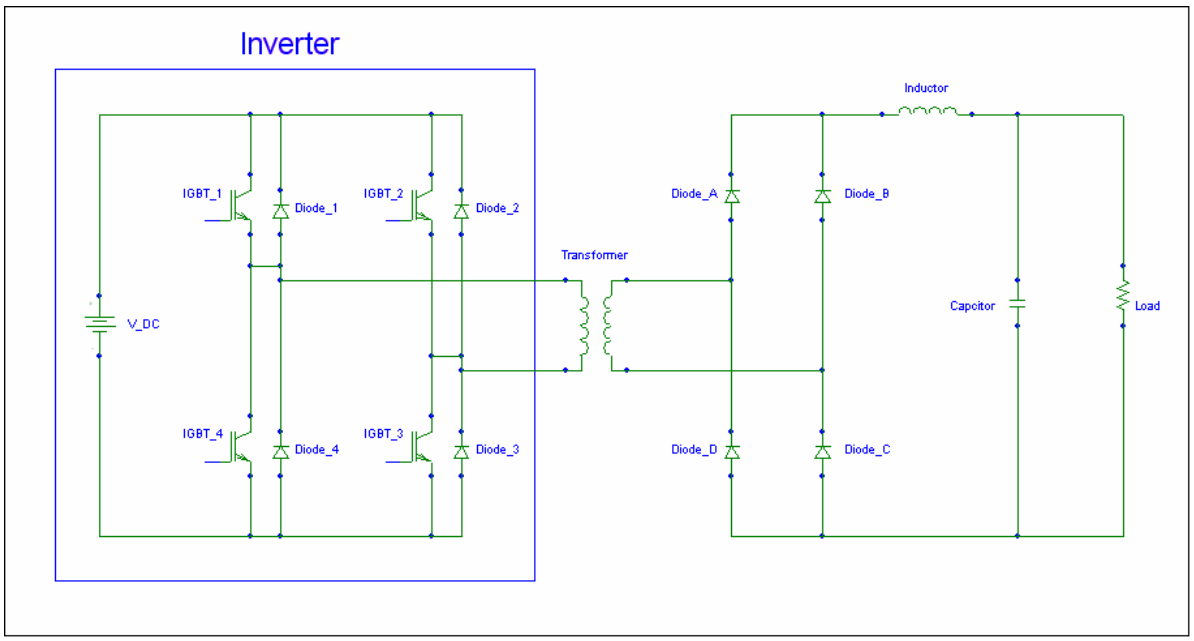

Figure 9. Inverter Portion of FBC

2. Components

The inverter that was used for this thesis was a Single-Phase Bridge Inverter (SPBI). The SPBI consists of four IGBTs, four anti-parallel diodes, a DC source, and associated wiring and control circuitry. The IGBT functions as a switch and its operation shall be further explained.

a. IGBT

As stated, the IGBT acts as an electrical switch. Figures 10 and 11 show the perspective view and the vertical cross section of a n-channel IGBT respectively [7].

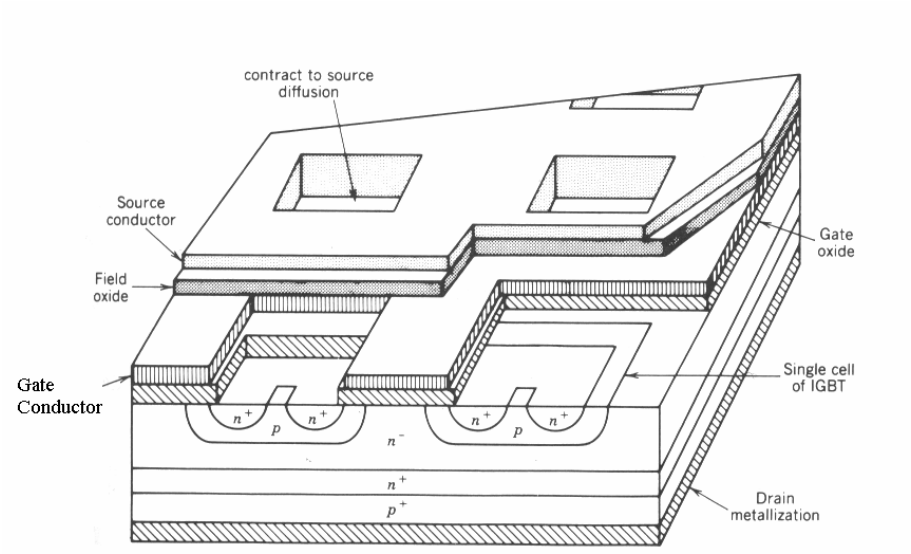

Figure 10. Perspective View of an IGBT (From Ref. [7].)

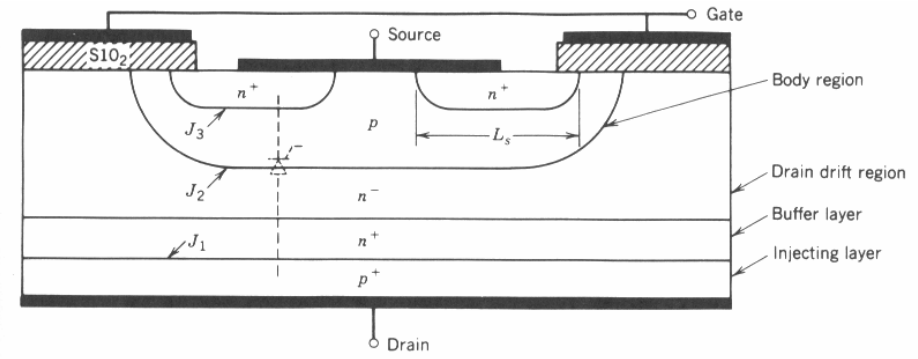

Figure 11. Vertical Cross-Section of an IGBT (From Ref. [7].)

A p-channel IGBT is also available, but for the remainder of this thesis, all future references to IGBTs will be assumed to be n-channel IGBTs.

The IGBT was created in order to realize an electrical switching device that has the quick switching capabilities of a Metal Oxide Surface Field Effect Transistor (MOSFET) with the low on-state conduction losses of a Bipolar Junction Transistor (BJT) [7]. An IGBT appears to be quite similar in construction to a typical MOSFET with a p+ layer forming the drain of the IGBT. The *i-v* characteristics of the IGBT are

shown in Figure 12. Figure 12 will enable an easier explanation of the operating regions of the device.

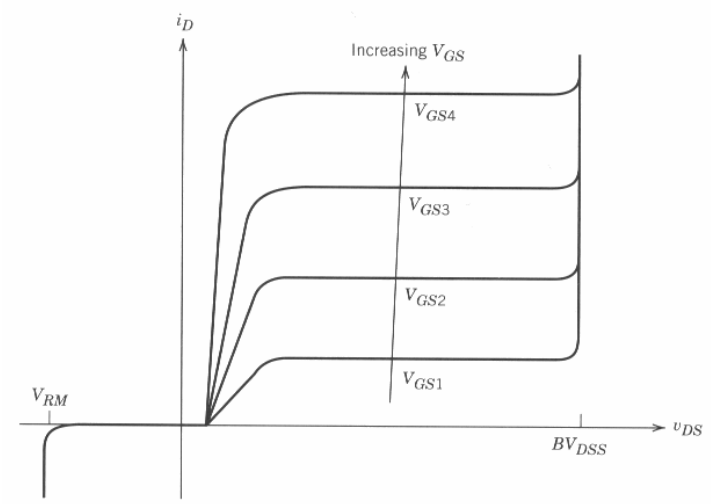

Figure 12. Output Characteristics of an IGBT (From Ref. [7].)

The Reverse Blocking Voltage (V_{RM}), and voltages below V_{RM} will cause the IGBT to conduct in the reverse direction [7]. This voltage is controlled by the junction labeled J1 in Figure 11, but is usually limited due to the n+ buffer region of the IGBT that is needed to lower on-state losses [7]. The voltage BV_{DSS} is the upper limit for blocking any operation of the IGBT in the forward direction while the IGBT is off. The junction labeled J2 controls this voltage, and voltages above this will cause the IGBT to conduct in the forward direction [7]. The *i-v* characteristic curve operates qualitatively similar to a logic-level BJT except that the controlling parameter is gate-source voltage (V_{GS}) and not input current [7]. To operate in the on-state, V_{GS} must exceed the device's threshold V_{GS}. In the on-state, the voltage drop across the IGBT is currently 1.7 V for new IGBTs [11].

b. Anti-Parallel Diodes

The anti-parallel diodes in the circuit serve as current flow paths to prevent circuit damage due to an inductor's inability to change current value instantaneously. The diodes must be able to switch quickly to perform their task, so a fast-

switching diode is needed. The diodes have a voltage drop across them of approximately 1.4 V [12].

3. Operation

Sine Pulse-Width Modulation (PWM) can be utilized in order to operate the inverter efficiently. Sine PWM uses a series of pulses with various pulse widths to simulate a sine wave. By using more pulses, PWM can prove to be quite effective; however, in order to utilize sine PWM operation of the inverter, a complicated control scheme must be devised that will cause both an increase in switching losses across the IGBTs and a lower system reliability. The increased switching frequency of the IGBTs also causes more noise. Although the increased switching losses caused by sine PWM operation are less than the losses due to harmonics in more rudimentary operating schemes, sine PWM was not selected in this thesis because the small increase in efficiency does not merit lower reliability and increased cost.

The SPBI used in the FBC will be operating using either a square-wave switching scheme or a modified square-wave switching scheme with a delay angle. Operating the SPBI using square-wave switching will allow the FBC to handle high voltage and current without having excessive losses from the switching devices. Since the IGBTs are only cycled once per cycle, the switching losses are much lower than in other switching schemes such as sine Pulse-Width Modulation (PWM).

Both the square-wave switching scheme and the modified square-wave switching scheme with a delay angle will fire IGBTs 1 and 3 shown in Figure 9 for the first half of its operating cycle, and then IGBTs 2 and 4, also shown in Figure 9, will be fired for the second half of the operating cycle. Figure 13 illustrates the gating signals and resulting output waveform.

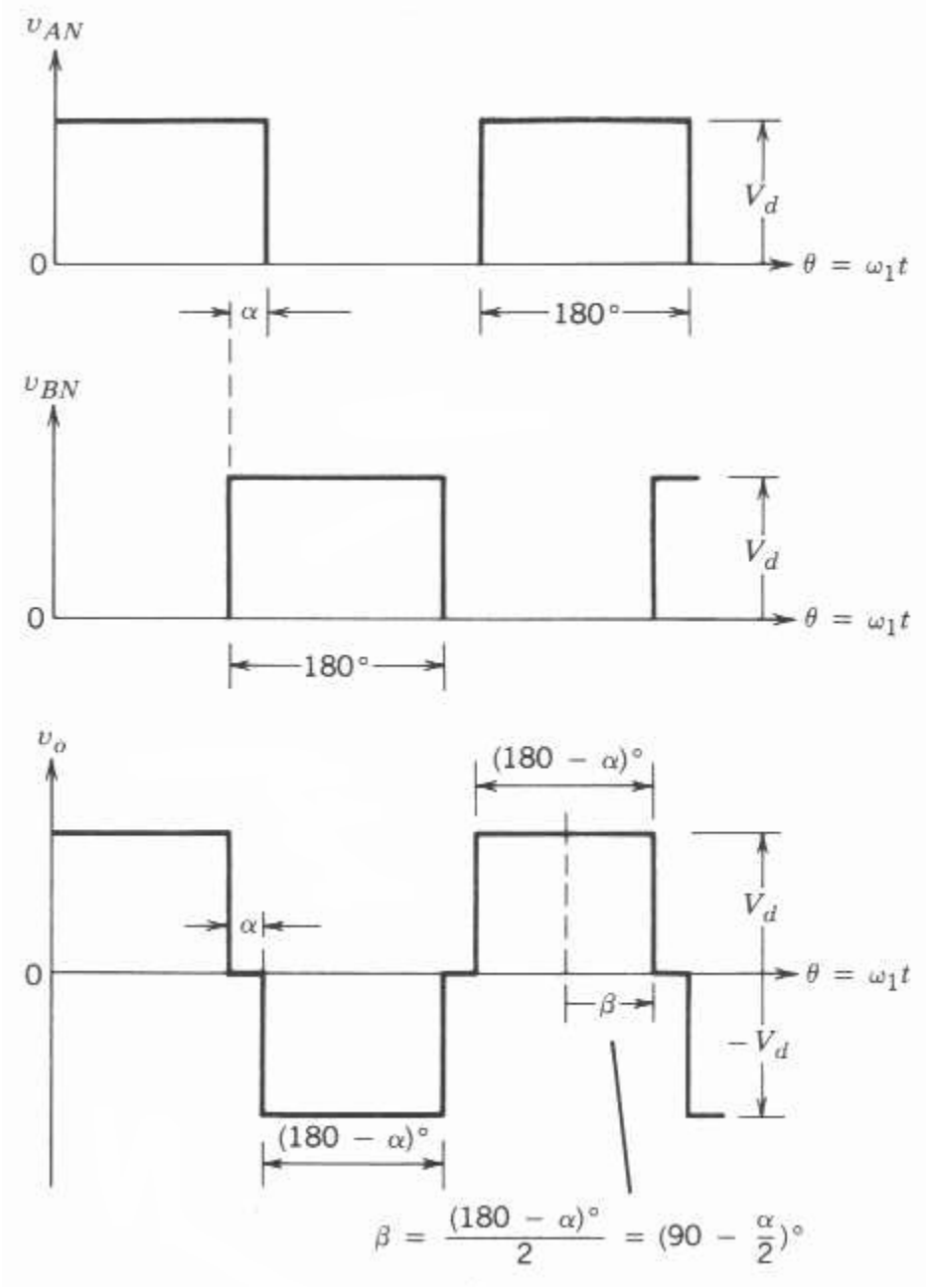

Figure 13. Waveforms Used by Voltage Cancellation Control of a Single-Phase Inverter (From Ref. [7].)

Figure 13 shows the resulting output waveform (V_o) of the inverter portion of the FBC when operating in modified square-wave mode. IGBTs 1 and 3 in Figure 9 are gated by the signal V_{AN} in Figure 13, and IGBTs 2 and 4 in Figure 9 are gated by the signal V_{BN} in Figure 13. By overlapping a small portion of V_{AN} and V_{BN}, a delay angle α is

introduced. An interlock in the control circuitry of the inverter forces the gating signals of the IGBTs to be low whenever a positive signal is sensed on all four IGBTS. The interlock causes all four IGBTs shown in Figure 9 to be turned off. The amplitude of the ouput signal of the inverter can be controlled by altering the delay angle.

The output voltage (V_o) and output angular frequency (ω_o) can be determined by the input voltage level (V_d) and firing period of one cycle of the IGBTs (T). The output voltage (V_o) is calculated using Fourier analysis while ω_o can be computed directly.

$$\omega_o = \frac{2\pi}{T}, \tag{4-1}$$

$$V_o = \frac{4V_d}{n\pi}\sin(n\beta)\sin(n\omega_o t). \tag{4-2}$$

Only the odd harmonics are present in the system, and they decrease exponentially as illustrated below. Figure 14 shown below is for the single case where the delay angle is equal to zero.

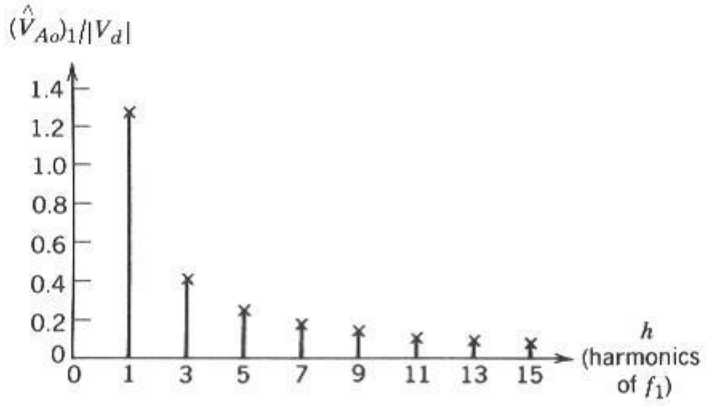

Figure 14. Magnitude of Harmonics of Single-Phase Inverter Operating in Square-Wave Mode (From Ref. [7].)

As shown by the calculations above, the fundamental voltage of the inverter output is easy to calculate. The root mean square (RMS) voltage can also be derived from the fundamental voltage by dividing by the square root of two [13].

$$V_{o,1} = \frac{4V_d}{\pi}\sin(\beta)\sin(\omega_o t), \tag{4-3}$$

$$V_{o,1,RMS} = \frac{2\sqrt{2}V_d}{\pi}\sin(\beta). \tag{4-4}$$

The load current and the fundamental RMS load current can be calculated as follows [7,14]:

$$i_o = \frac{4V_d}{n\pi Z_n}\sin(n\beta)\sin(n\omega_o t - \theta_n), \tag{4-5}$$

$$\theta_n = \tan^{-1}\left[\frac{n\omega_o L - \dfrac{1}{n\omega_o C}}{R}\right], \tag{4-6}$$

and

$$i_{o,1,RMS} = \frac{\sqrt{2}V_{o,1,RMS}}{Z_1}\sin(\beta). \tag{4-7}$$

The shape of the load current waveform is dependent on the capacitive and inductive elements present in the load. Figure 15 shows the output waveforms generated when an inverter is operating in square-wave mode with different load configurations [13]. The waveform shown at the top of Figure 15 is the output of an inverter operating in square-wave mode. The second waveform shown in Figure 15 illustrates the voltage across a load containing underdamped resistive, capacitive, and inductive elements. The waveform is more sinusoidal and is leading. The third waveform shown in Figure 15 is the voltage across a load containing overdamped resistive, capacitive, and inductive elements. The waveform is now lagging and sinusoidal. A resistive and inductive load will cause the signal across the load to become lagging and triangular as shown in Figure 15. A capacitive and resistive load will create an output across the load that is almost a square wave. A purely resistive load will result in a pure square-wave through the load.

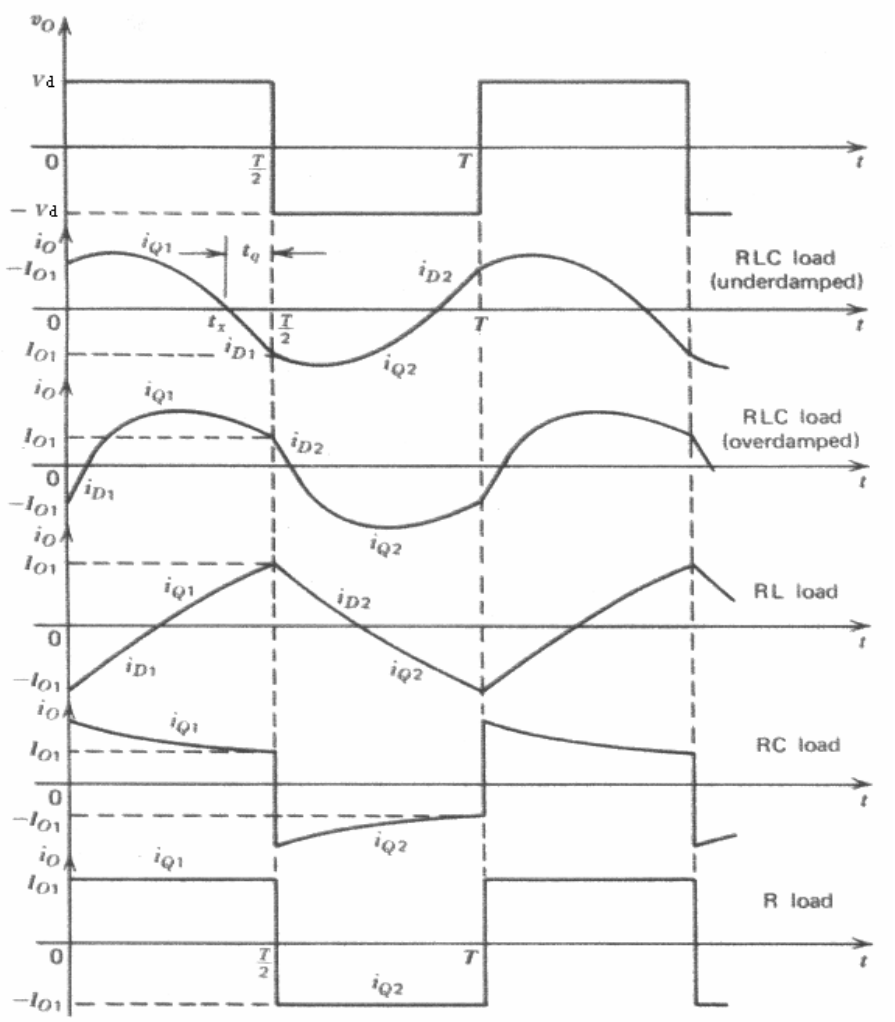

Figure 15. Output Waveforms of Single-Phase Inverter Operating in Square-Wave Mode Under Various Loads (From Ref. [13].)

The inverter will be able to adjust to changes in the load by varying the delay angle. As the delay angle increases the output of the inverter will decrease. The losses associated with the inverter portion of the FBC will be analyzed in the efficiency section of Chapter IV.

D. TRANSFORMER PORTION OF FBC

1. PURPOSE

The transformer portion of the FBC serves two purposes. First, the transformer will "step-up" or "step-down" the voltage from the primary side to the secondary side. In this thesis, the transformer will "step-down" the voltage from the primary side of the transformer to the secondary side of the transformer. The second purpose of the transformer is to provide galvanic isolation between the primary and secondary. The galvanic isolation achieved by using the transformer is the greatest benefit of using a FBC. Figure 16 highlights the transformer portion of the FBC.

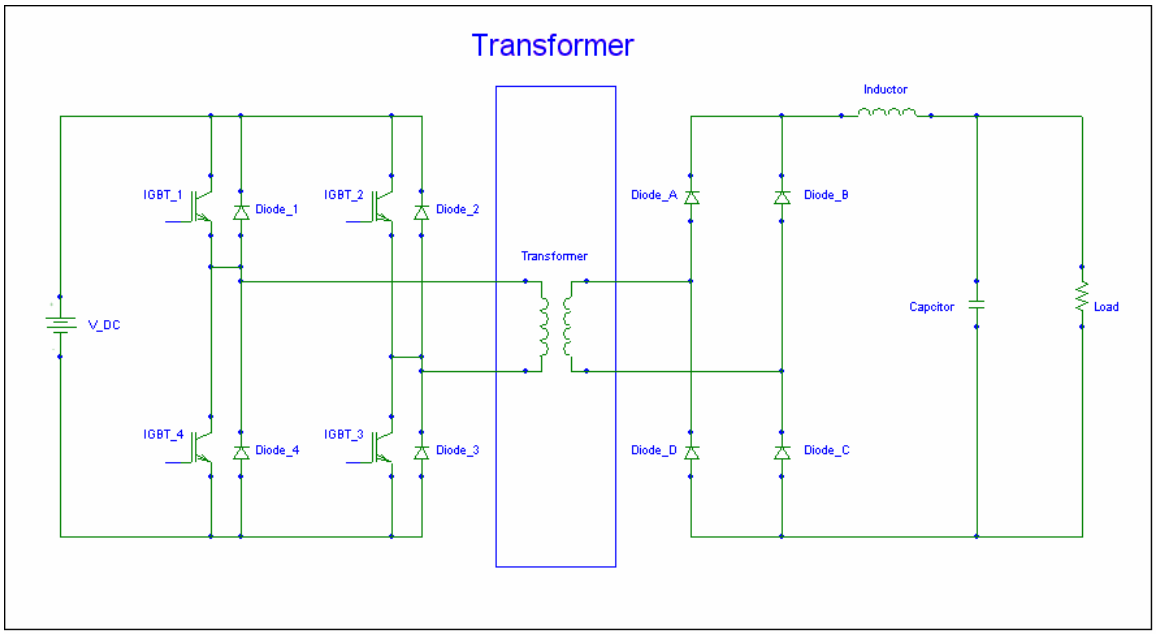

Figure 16. Transformer Portion of the FBC

a. Transformer Construction

A transformer has three major components. The three major components are the core, the primary winding, and the secondary winding. All three components are vital in both transformer construction and transformer selection. A transformer should be able to provide the desired results while minimizing the various associated losses to

maintain the overall efficiency of the system. All three components shall be discussed further in the following sections.

b. Transformer Core

The transformer core can be made from two broad classes of materials. The first class of cores is made from various alloys of iron. The core can be constructed from alloys made principally from iron and small amounts of other elements including chrome and silicon [7]. These cores are used in applications with frequencies generally below 2 kHz due to eddy current losses that increase with higher frequencies. This class of cores can also be made from powdered iron and powdered iron alloys. The powdered iron cores are constructed from small iron particles electrically isolated from each other in order to provide greater resistivity than laminated cores. Powdered iron cores have lower eddy current losses than laminated cores and can be used with higher frequencies. The second type of cores is built using ferrites. Ferrite materials are basically oxide mixtures of iron and other magnetic elements [7]. Ferrite materials have large electrical resistivity but low saturation flux densities. Also, ferrite cores have only hysteresis losses. By having no eddy current losses, ferrite cores are ideal cores for high frequency applications. Hysteresis losses are calculated as follows [7]:

$$P_{m,sp} = kf^{a}(\beta_{ac})^{d}, \tag{4-8}$$

where $P_{m,sp}$ is the hysteresis loss per unit volume, β_{ac} is the AC flux density, f is the operating frequency, and k, a, and d are operating constants of a particular core material. Eddy current losses are calculated as follows [7]:

$$P_{ec,sp} = \frac{d^{2}\omega^{2}\beta^{2}}{24\rho_{,core}}, \tag{4-9}$$

where $P_{ec,sp}$ is the eddy current loss per unit volume, d is the lamination thickness, ω is the radian frequency, β is the magnetic flux density, and $\rho_{,core}$ is the core conductivity.

c. Primary Winding/Secondary Winding

The primary and secondary windings are usually built using copper conductors due to the high conductivity and malleability of copper. The copper wires have a DC resistance that will create power losses, and the high frequencies can cause the power losses to increase greatly for AC power applications due to skin effects [7]. The AC power losses can be calculated after calculating the DC power losses and adjusting the results for skin effects [7]. Figure 17 shows the cross-sectional view of a double-E core transformer [7].

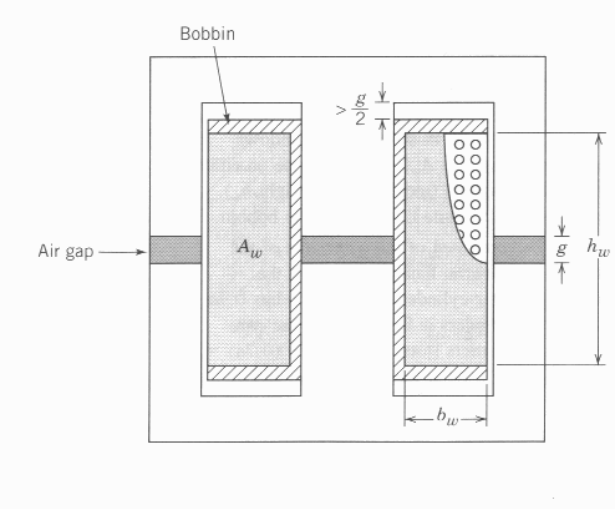

Figure 17. Cross-Sectional View of Double-E Core Transformer (From Ref. [7].)

The DC power losses through the transformer can be calculated as follows,

$$P_{Cu,sp} = \rho_{Cu}(J_{RMS})^2, \tag{4-10}$$

$$J_{RMS} = \frac{I_{RMS}}{A_{Cu}}, \tag{4-11}$$

where A_{Cu} is the effective copper area, I_{RMS} is the RMS current, $P_{Cu,sp}$ is the power dissipated per unit of copper volume, and ρ_{Cu} is the resistivity of copper. Now that the DC power losses have been calculated, the AC power losses can be calculated by introducing the skin effect as follows,

$$P_{w,sp} = k_{Cu}\rho_{Cu}(J_{RMS})^2, \tag{4-12}$$

$$k_{Cu} = \frac{NA_{Cu}}{A_w}, \tag{4-13}$$

where $P_{w,sp}$ is the power dissipated per unit of winding volume, k_{Cu} is the copper fill factor, N is the number of turns of copper wire, A_{Cu} is the cross-sectional area of copper wire, and A_w is the area of the winding window.

The value of power dissipated by a copper winding at one-hundred degrees Celsius is,

$$P_{w,sp} = 22k_{Cu}(J_{RMS})^2 \qquad \text{(No skin effect).} \tag{4-14}$$

The power dissipated at one-hundred degrees Celsius with a noticeable skin effect present can be calculated as follows [7]:

$$P_{w,sp} = 22k_{Cu}\frac{R_{Cu}}{R_{DC}}(J_{RMS})^2 \qquad \text{(Skin effect present),} \tag{4-15}$$

where R_{Cu}/R_{DC} is the ratio of AC resistance of the copper conductor to DC resistance of the copper conductor.

The power dissipated is not noticeably increased until the diameter of the copper conductor is greater than two times the skin depth [7]. The skin depth of various frequencies is shown in Table 3. The inverter portion of the FBC will operate at several thousand Hertz, and the problems associated with skin depth will require Litz wiring [7]. Litz wiring twists many smaller copper conductors together to alleviate the skin depth concerns while providing sufficient conductivity to prevent excessive resistance [7].

Frequency	*50 Hz*	*5 kHz*	*20 kHz*	*500 kHz*
δ	10.6 mm	1.06 mm	0.53 mm	0.106 mm

Table 3 Skin Depth Effects in Copper Conductors (From Ref. [7].)

E. RECTIFIER PORTION OF THE FBC

1. Purpose

The rectifier portion of the FBC rectifies the AC output of the secondary side of the transformer into a DC signal. The DC signal is then filtered to provide a smooth DC source of power to the load. The circuit must be able to operate at a high frequency while maintaining overall system efficiency. The rectifier portion of the FBC is shown in Figure 18.

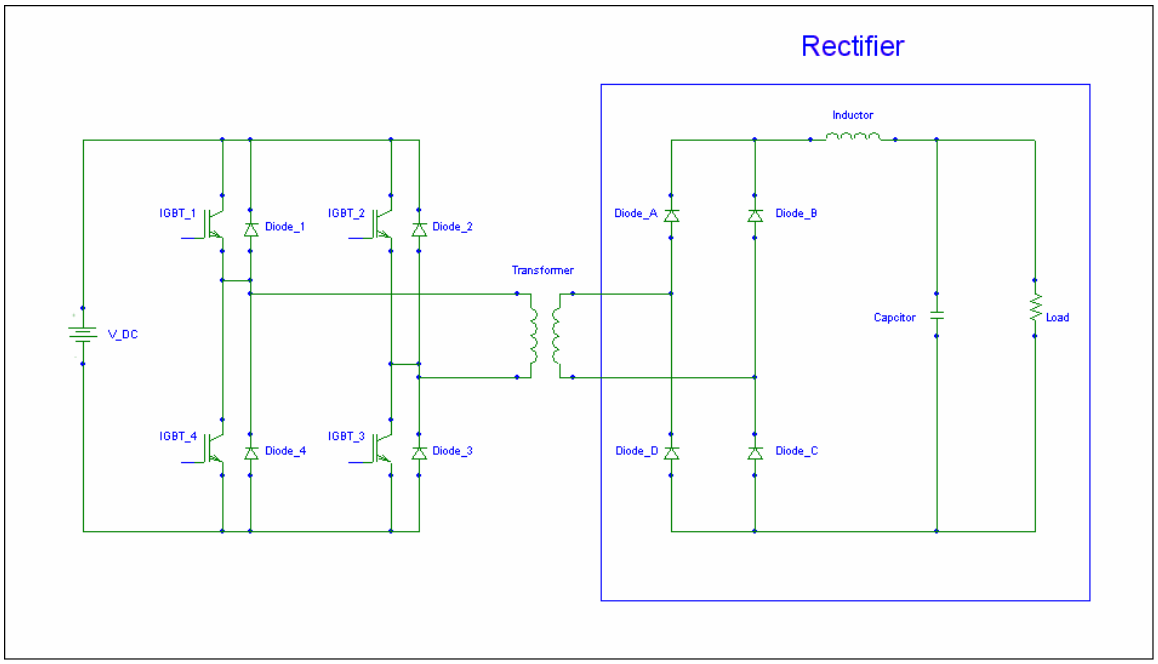

Figure 18. Converter Portion of the FBC

2. Construction and Operation

The full-bridge diode circuit consists of four diodes. Diode_A and Diode_C conduct when IGBT_1 and IGBT_2 are operating. When IGBT_2 and IGBT_4 are turned on, Diode_B and Diode_D conduct and provide a path for current flow to the load. The current flow to the load always flows into the positive terminal of the load. Since the load may require a constant DC signal, a filter is necessary to smooth out the ripple from the bridge rectifier. A large capacitor is placed in parallel with the load in order to create a constant DC output.

F. CHAPTER REVIEW

This chapter provided a background into why the FBC was chosen as the appropriate topology to serve as the SSCM onboard future naval vessels. The FBC was then studied as to how the three major portions of the converter operate in tandem to achieve the desired results. Several of the more intricate components of converter were examined in greater detail. Chapter III will analyze the operation of the converter in greater detail in order to create a model for simulation. Chapter IV will use the background examined in Chapter II to calculate several parameters of the converter while operating in an example.

III. MODELING OF FBC

A. PURPOSE

The purpose of this chapter is to derive the FBC's characteristic equation by state-space analysis. After the characteristic equation that governs the operating parameters of the converter is derived, a suitable method for controlling the converter is detailed. The converter should be able to respond quickly to load changes that could occur due to the dynamic operating characteristics of naval vessels.

B. STATE-SPACE ANALYSIS OF FBC

1. Mode 1

The first mode of operation of the converter has the following path for current flow (see Figure 19): from the source, through IGBT_1, in the dotted primary side of the transformer, out the dotted secondary side of the transformer, through diode_A, through the output filter, through the load, through diode_C, in the non dotted secondary side of the transformer, out the non dotted primary side of the transformer, through IGBT_3, and returning to the source. The transformer, when treated as an ideal transformer with a unity turns ratio, can be removed from the circuit. Both IGBT_1 and IGBT_3 can be treated as ideal switches that are closed and can therefore be removed. Figure 20 shows the simplified circuit used for analysis.

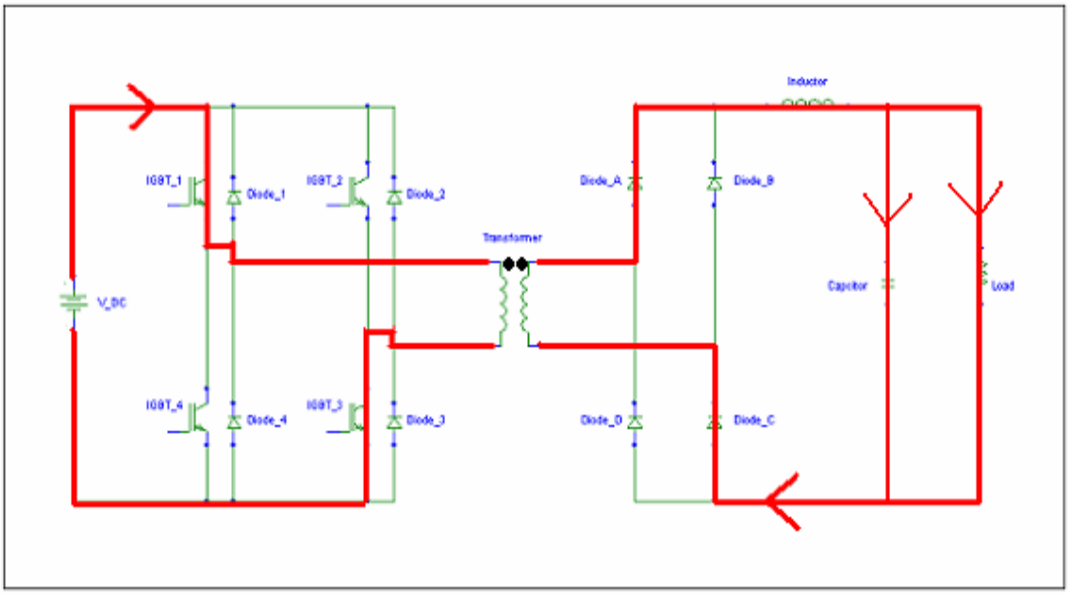

Figure 19. Circuit Trace for Mode 1 of the FBC

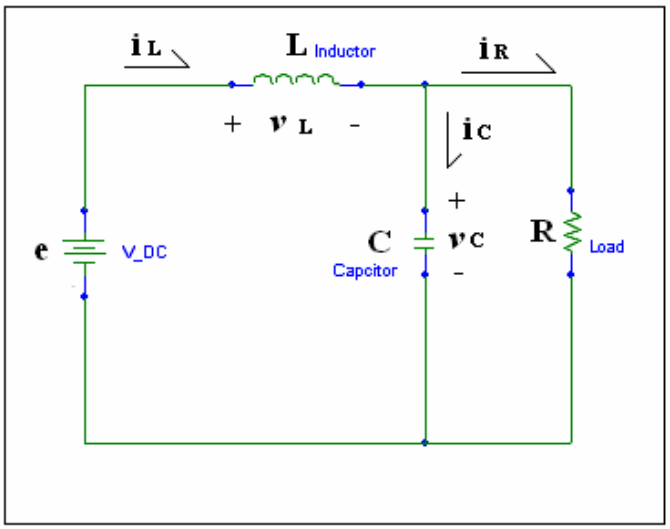

Figure 20. Simplified Circuit for Mode 1 of FBC

During the first mode, the following equations describe the system [14]:

$$i_L = i_R + i_C, \tag{3-1}$$

$$i_L = \frac{V_c}{R} + \frac{CdV_c}{dt}, \tag{3-2}$$

$$\frac{dV_c}{dt} = \frac{1}{C}\left[i_L - \frac{V_c}{R}\right], \tag{3-3}$$

$$e = V_L + V_c, \tag{3-4}$$

$$e = \frac{Ldi_L}{dt} + V_c, \tag{3-5}$$

and

$$\frac{di_L}{dt} = \frac{1}{L}[e - V_c]. \tag{3-6}$$

2. Mode 2

In the second mode, the FBC has all four IGBTs in the off state. The anti-parallel diodes will allow the residual current within the transformer to dissipate on the primary side, and this will be viewed as insignificant in the operating characteristics of the converter. The load will continue to have continuous current flow due to the sufficiently large inductor. The path for current flow during mode 2 is shown in Figure 21, and the electrical elements are once again viewed as ideal, causing the circuit to simplify as shown in Figure 22.

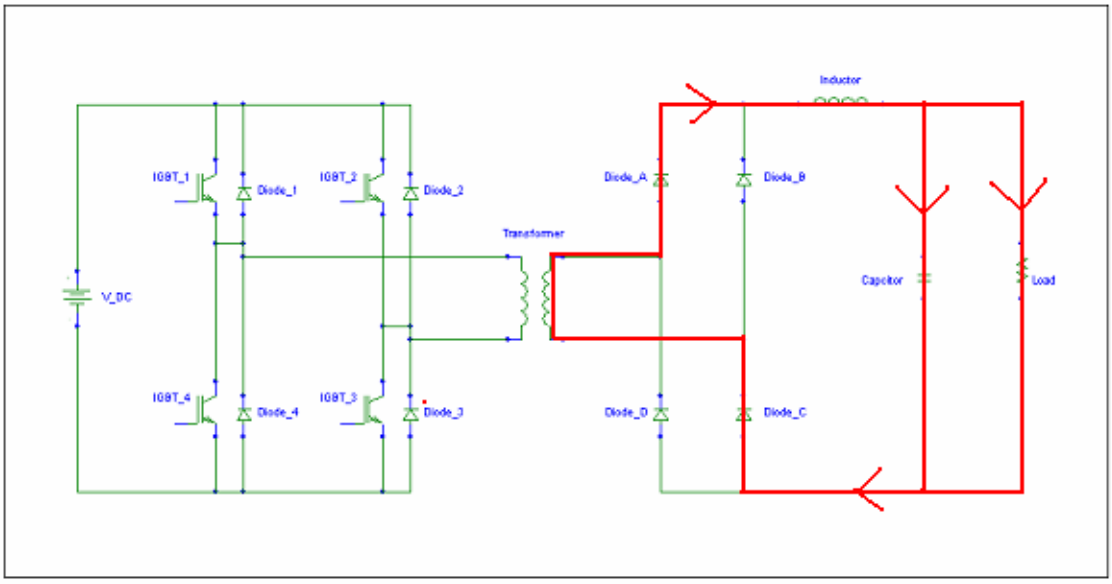

Figure 21. Circuit Trace for Mode 2 of FBC

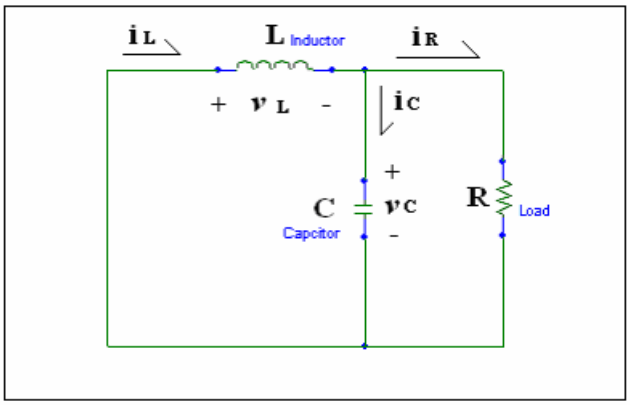

Figure 22. Simplified Circuit for Mode 2 of FBC

This mode of the converter can be described by the following equations [14]:

$$i_L = i_R + i_C, \tag{3-7}$$

$$i_L = \frac{V_c}{R} + \frac{CdV_c}{dt}, \tag{3-8}$$

$$\frac{dV_c}{dt} = \frac{1}{C}\left[i_L - \frac{V_c}{R}\right], \tag{3-9}$$

$$0 = V_L + V_c, \tag{3-10}$$

$$0 = \frac{Ldi_L}{dt} + V_c, \tag{3-11}$$

and

$$\frac{di_L}{dt} = \frac{1}{L}\left[0 - V_c\right]. \tag{3-12}$$

3. Mode 3 and 4

Mode 3 of the converter has both IGBT_2 and IGBT_4 switched on providing the following path for current flow (see Figure 23): from the source, through IGBT_2, in the non dotted primary side of the transformer, out the non dotted secondary side of the transformer, through diode_B, through the output filter, through the load, through diode_D, in the dotted terminal of the secondary side of the transformer, out the dotted primary side

of the transformer, through IGBT_4, and returning to the source. This mode simplifies to the equivalent circuit shown in mode 1 resulting in identical dynamic equations.

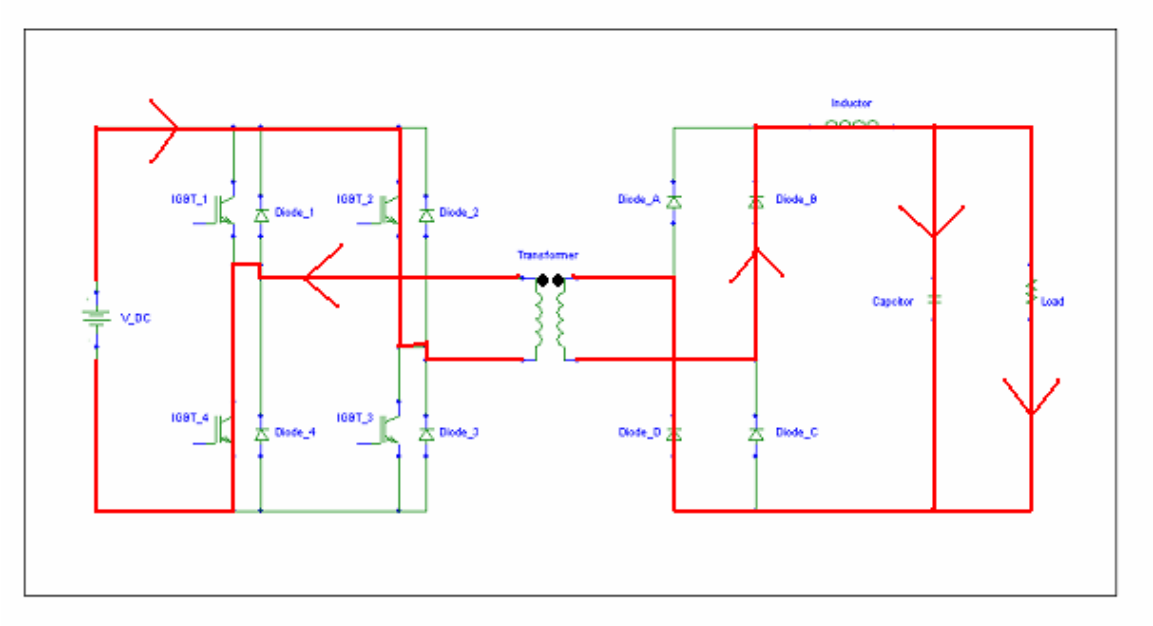

Figure 23. Circuit Trace for Mode 3 of FBC

Mode 4 of the converter has all IGBTs operating in a non conducting mode of operation. The path for current flow (see Figure 24) goes through the inductor, through the load, through diode_D, through diode_B, and returning to the inductor. Mode 4 of the converter proves to operate by the identical dynamic equations defined during mode 2 of operation.

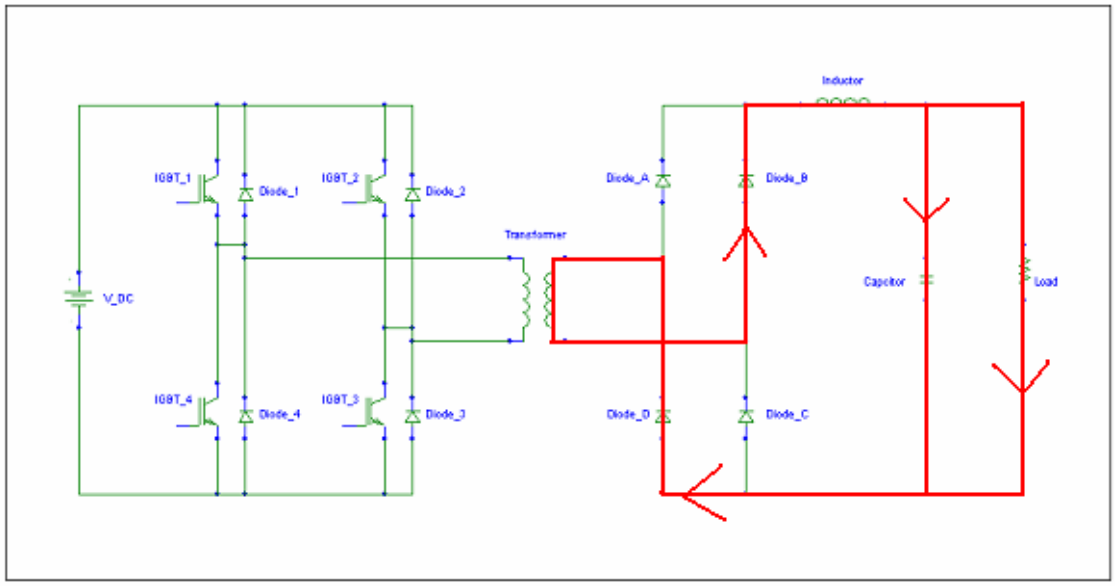

Figure 24. Circuit Trace for Mode 4 of FBC

4. Weighting the Equations

Now that two sets of dynamic equations are defined that model the behavior of the converter, they must be weighted for their specific operating periods [7]. If d is the fractional interval that switching pairs are closed (IGBT_1 and IGBT_3 or IGBT_2 and IGBT_4), then a weighting equation can be defined as follows [14]:

$$d = D + \hat{d}, \tag{3-13}$$

$$\hat{d} = 1 - d. \tag{3-14}$$

Here D is the static portion of the equation while $\hat{d}$ is the small signal or ripple portion of the equation. After weighting the equations and performing some minor simplifications, the following two equations are defined,

$$\frac{dV_c}{dt} = \frac{1}{C}\left[i_L - \frac{V_c}{R}\right], \tag{3-15}$$

$$\frac{di_L}{dt} = \frac{1}{L}\left[de - V_c\right]. \tag{3-16}$$

5. Introduction of Small Signal Components

Each variable within the weighted equations contains a DC and ripple portion that must be defined. The list of equations below will provide the needed small signal components [14],

$$e = E + \hat{e}, \tag{3-17}$$

$$i_L = I_L + \hat{i}_L, \tag{3-18}$$

$$V_c = V_c + \hat{V}_c, \tag{3-19}$$

$$d = D + \hat{d}, \tag{3-20}$$

$$\frac{di_L}{dt} = \frac{d\hat{i}_L}{dt}, \tag{3-21}$$

and

$$\frac{dV_c}{dt} = \frac{d\hat{V}_c}{dt}. \tag{3-22}$$

After introducing the small signal components, two new sets of equations can be defined. There is a set of DC, or non-ripple, equations, and there is a set of ripple equations.

$$I_L = \frac{V_c}{R}, \tag{3-23}$$

$$V_c = DE, \tag{3-24}$$

$$\frac{d\hat{V}_c}{dt} = \frac{1}{C}\left[\hat{i}_L - \frac{\hat{V}_c}{R}\right], \tag{3-25}$$

and

$$\frac{d\hat{i}_L}{dt} = \frac{1}{L}\left[E\hat{d} - \hat{V}_c\right]. \tag{3-26}$$

Note that since we are not interested in the input ripple, those terms were removed [7,14]. Also, any combination of two ripple elements were viewed as trivial and subsequently set to zero. By using the Laplace transforms and the two ripple equations, a transfer function for the converter can be found as,

$$\frac{\hat{V}_c}{\hat{d}} = \frac{E}{LCs^2 + \left[\frac{L}{R}\right]s + 1}. \tag{3-27}$$

C. BIDIRECTIONAL OPERATION

An additional advantage of using a FBC is the ease at which the converter can become bidirectional. As shown in Figure 25, bidirectional operation can be achieved by adding an output filter across the original source, a second inverter in place of the original full bridge rectifier, and two diodes to remove the inductor portion of the filter from the side operating as the source.

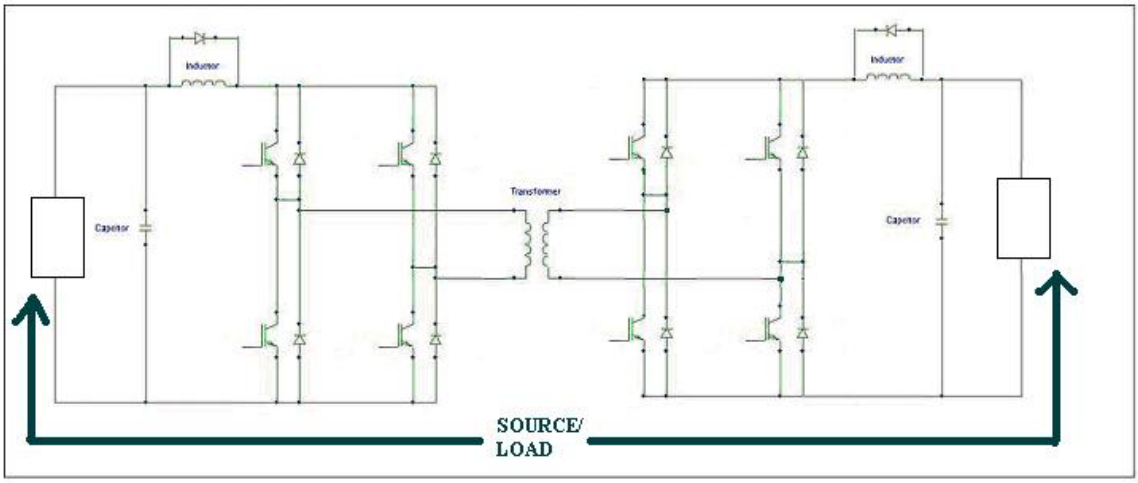

Figure 25. BIDIRECTIONAL FBC

The ability for the converter to operate in a bidirectional manner increases the value of the converter as part of an EDS. If the power source was interrupted from one side of the converter, the other side could supply power if a backup source of power was present.

D. CONTROLLER DESIGN

There has been extensive work done at NPS that details the control of various buck choppers. The control scheme that is most widely accepted as the most effective is displayed in Figure 26 [1].

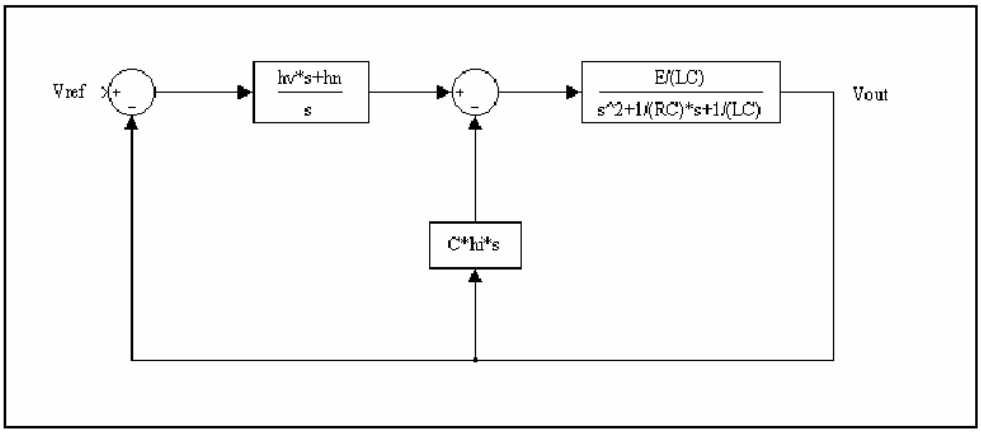

Figure 26. Buck Converter Closed-Loop System (From Ref. [1].)

The duty cycle is used to control the output voltage level. The duty cycle for the FBC with the controller used in this thesis can be calculated as follows [1],

$$d(t) = -h_v(v_{out} - v_{ref}) - h_n \int (v_{out} - v_{ref})dt - h_i(i_L - i_{out}), \tag{3-28}$$

where $d(t)$ is the duty cycle, h_v is the proportional voltage gain, h_n is the integral voltage gain, and h_i is the derivate voltage feedback gain.

This control scheme is known as proportional integral derivate (PID). Due to the fact that the control loop will operate at a much lower frequency than the inverter portion of the FBC's switching frequency, the switching harmonics of the control will be filtered out. The closed-loop transfer function for the control circuit and the FBC were derived as

$$\frac{V_{out}}{V_{ref}} = \frac{\frac{E}{LC}(h_v s + h_n)}{s^3 + \left(\frac{1}{RC} + \frac{Eh_i}{L}\right)s^2 + \left(\frac{1}{LC} + \frac{Eh_v}{LC}\right) + \frac{Eh_n}{LC}}. \tag{3-29}$$

A multi-loop control scheme was utilized for several reasons. In order for the system to provide the proper output, a setpoint (or gain) must be chosen. The system gain is set with the h_v term. The proportional gain is calculated to have the converter provide the proper output voltage level during steady state. The error between the output voltage and reference voltage provides the controller with the information necessary to change the firing of the IGBTs to remove the error and return the output voltage to the desired level.

The integral portion of the controller is needed to eliminate the offset in the converter. If only a proportional controller was used, any changes in the input would cause the converter's output to settle at an output voltage that is different that the desired output voltage (this is known as offset voltage). By measuring the time that the output voltage error is present, the controller can act to eliminate any associated offset problems. The integral gain is set by adjusting h_n. Having a proportional and integral controller will cause the controller to be rather oscillatory without the addition of derivate control.

Derivate control is achieved by measuring the difference between the inductor current and the output current. The h_i term is the derivative constant and is used to prevent overshooting the desired output level when the controller is compensating due to present error signals. The derivate term causes the converter to slow down its corrective behavior as the output voltage approaches the desired output voltage.

By including the proportional, integral, and derivate portions of control, a system that is both responsive and accurate can be created. The PID concept is well established in industry, and many converters designed by prior students at NPS have chosen this type of control. Since it is not difficult to measure the needed inputs for a PID controller in the FBC, it is worth the added difficulty to create a PID controller than to use an inferior method of control.

E. BUCK CHOPPER TO FBC

During the simplification process of treating mode 3 and mode 4 of the converter as identical to mode 1 and mode 2, some adjustments must be noted to the overall transfer function. Mode 1 and mode 2 comprise only one-half of the operating cycle, and it is necessary to define some relationships.

$$D = 2\beta, \tag{3-30}$$

$$\alpha = 1 - D, \tag{3-31}$$

and

$$\omega_o = 2\omega. \tag{3-32}$$

When either solving for controller variables or simulating the system response, it is necessary to use twice the actual FBC frequency. When solving for the actual components of the FBC, the real switching frequency of the converter will be used.

F. CHAPTER REVIEW

Chapter III provided the actual transfer functions that will be used to model the operation of the FBC. By treating the components as ideal while performing some suitable simplifications, previous work done at NPS on buck choppers could be expanded for use in the FBC. Chapter IV simulates the FBC using MATLAB in order to test the capabilities of the FBC.

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IV. FBC SIMULATIONS

A. PURPOSE

The purpose of this chapter is to provide a solid example supported by various simulations in order to highlight the feasibility of the FBC. The converter will be operating in the step-down or "buck" mode for the example although it can operate in step-down, step-up, or unity gain isolation mode. Also, the example can be modified and altered in numerous ways to achieve specific objectives not targeted in this thesis.

B. COMPONENT SELECTION AND SIZING

1. Inductor (*L*)

The inductor in the circuit will serve to maintain continuous current flow to the load during all modes of converter operation. The inductor shall be chosen to be sufficiently large enough to maintain continuous current for load variations of 50%. An arbitrary load (*R*) of 75 Ω was chosen for this example. The input voltage (*E*) is 500 V DC. The critical inductance formula for a buck chopper can be altered to provide the critical inductance for the FBC as follows [1,3,4,7,14],

$$L_{CRIT} = \frac{TR}{2}\left[1 - D\right], \tag{4-1}$$

$$L_{CRIT} = TR\left(1 - 2\beta\right). \tag{4-2}$$

The FBC will be operating in order to provide an output voltage of 300 V DC; therefore, it is necessary to calculate the proper duty cycle and associate delay angle as

$$D = \frac{V_c}{E} = \frac{300}{500} = 0.6. \tag{4-3}$$

The converter will operate at 10,000 Hz in order to minimize audible switching noise, required inductor size, minimize inductor ripple current, and maximize the allowable closed-loop control bandwidth. As stated by earlier, the actual frequency to be used in

modeling the converter is twice the switching frequency. Now that sufficient operating characteristics have been defined, the critical inductance can be calculated directly from Equation 4-2,

$$L_{CRIT} = (0.00005)(37.5)(1-0.6) = 0.75 \text{ mH}. \tag{4-4}$$

2. Capacitor (*C*)

The capacitor placed in parallel with the load serves to minimize the output voltage ripple. The output of the converter will prove useless if the waveform being produced is not very near to being a pure DC signal. The first step in calculating the minimum required capacitance is to solve for the difference between the maximum and minimum inductor current [14],

$$I_{L,MAX} - I_{L,MIN} = \frac{E - V_c}{L} DT = \frac{500 - 300}{0.75}(0.6)(0.00005) = 8 \text{ A}. \tag{4-5}$$

Now a specific goal of maintaining the output voltage ripple to less than 1% of the output voltage is defined [14],

$$\Delta V_c = (\%\text{ripple})(V_c) = (0.01)(300) = 3 \text{ V}. \tag{4-6}$$

Now the minimum capacitance can be directly calculated using the following equation from reference [7,14],

$$C_{\min} = \frac{(I_{L,MAX} - I_{L,MIN})T}{8\Delta V_c} = \frac{(8)(0.00005)}{(8)(3)} = 17 \text{ μH}. \tag{4-7}$$

Since the value of the capacitor also has an effect on the system transients, it is necessary to use a larger value to ensure proper system operation. Also, the value of the capacitor needs to be larger in order to ensure the ability of the converter to maintain a desirable output voltage during transients. A value of 100 μF was selected because it provides desirable results.

C. UNCONTROLLED, CLOSED-LOOP SYSTEM RESPONSE

1. Full Load

The closed-loop transfer function of the system is calculated using a 37.5 Ω load (R), 100 μF value of capacitance (C), and a 0.75 mH value of inductance (L) from Equation 3-27,

$$\frac{\hat{V}_c}{\hat{d}} = \frac{500}{7.5e^{-8}s^2 + 2e^{-5}s + 1}. \tag{4-8}$$

The system stability can be verified by several means. The easiest approach is to plot the pole locations that are derived from factoring the denominator of the transfer function. Matlab was used in order to provide a graphical illustration of both the system poles and holes in Figure 27.

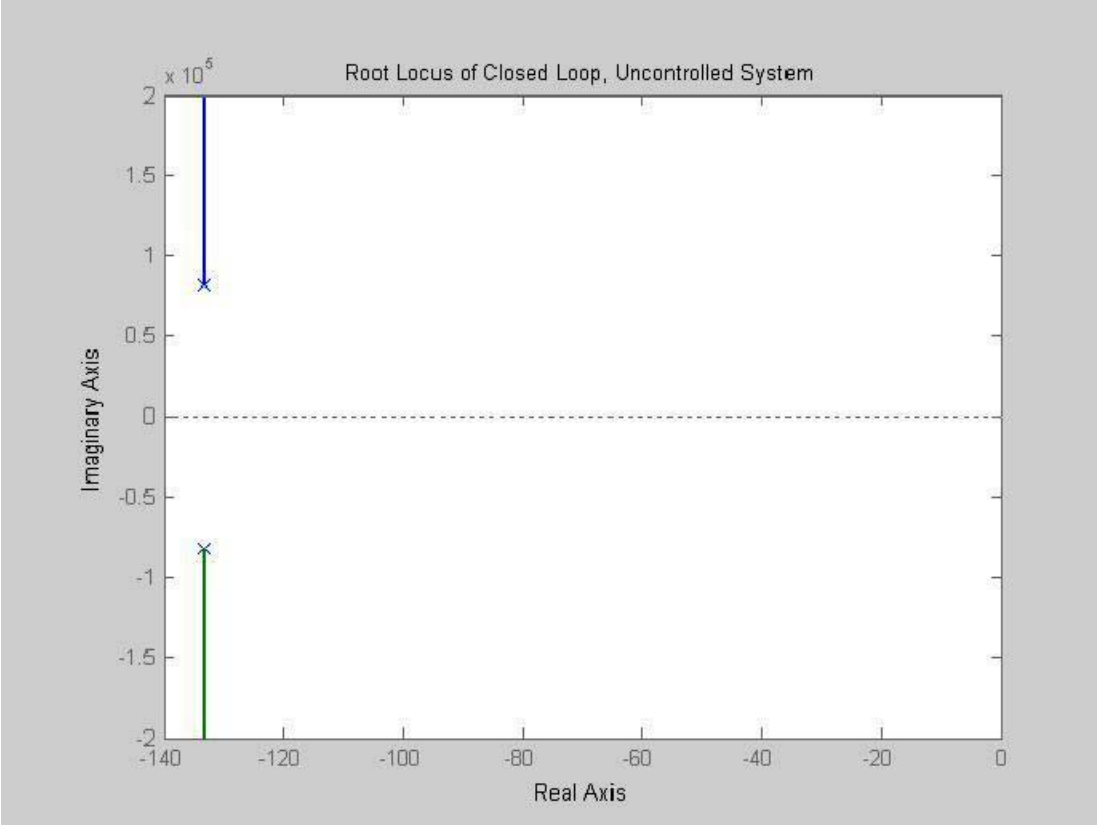


Figure 27. Root Locus of Uncontrolled, Closed-Loop FBC Under Full Load

Several important factors can be determined by studying the root locus of the closed-loop, uncontrolled transfer function. First, the system is proven to be stable due to the fact that all the poles are located in the left half plane. The poles are located at $(-133 \pm j81650)$. Secondly, since the imaginary portion of the poles are larger that the real portion, the system will be highly oscillatory. The system's response to a step function was illustrated by Figure 28.

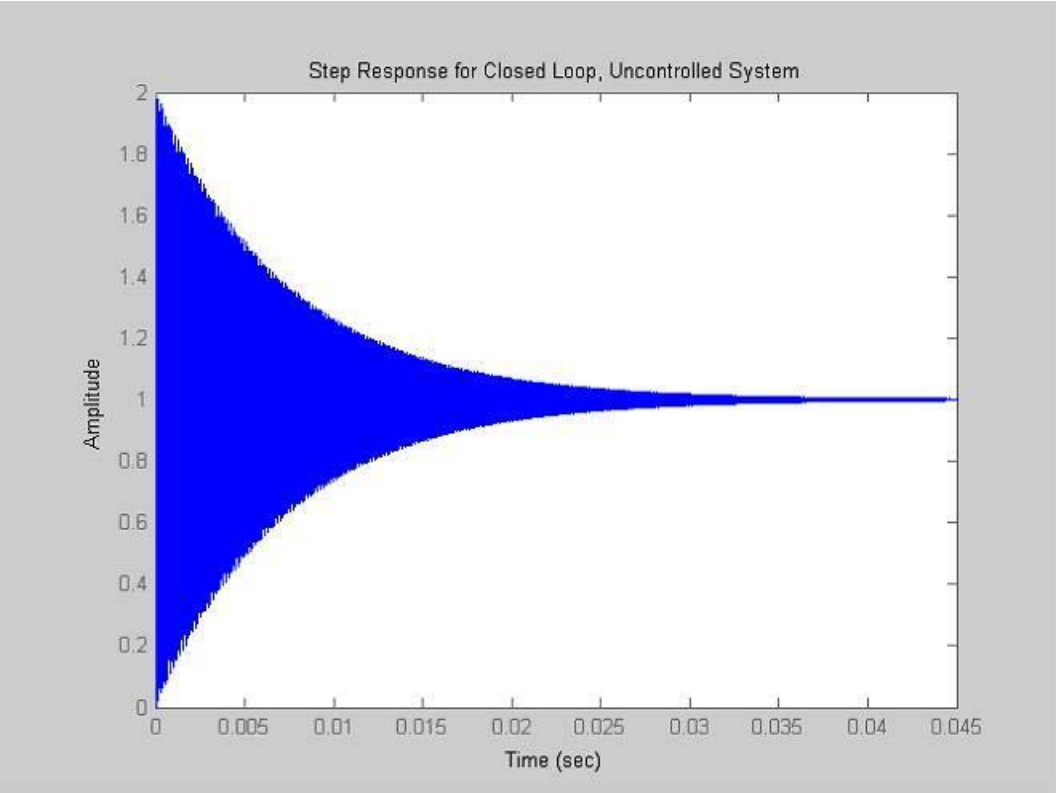


Figure 28. Step Response of Uncontrolled, Closed-Loop FBC Under Full Load

The step response for the closed-loop, uncontrolled system illustrates several undesirable traits. Notice that the system is extremely oscillatory during the settling time. Also, the system takes approximately 45 ms to settle out and achieve a steady state. Finally, the frequency response of the system can be viewed by the use of a Bode plot and the output was shown in Figure 29.

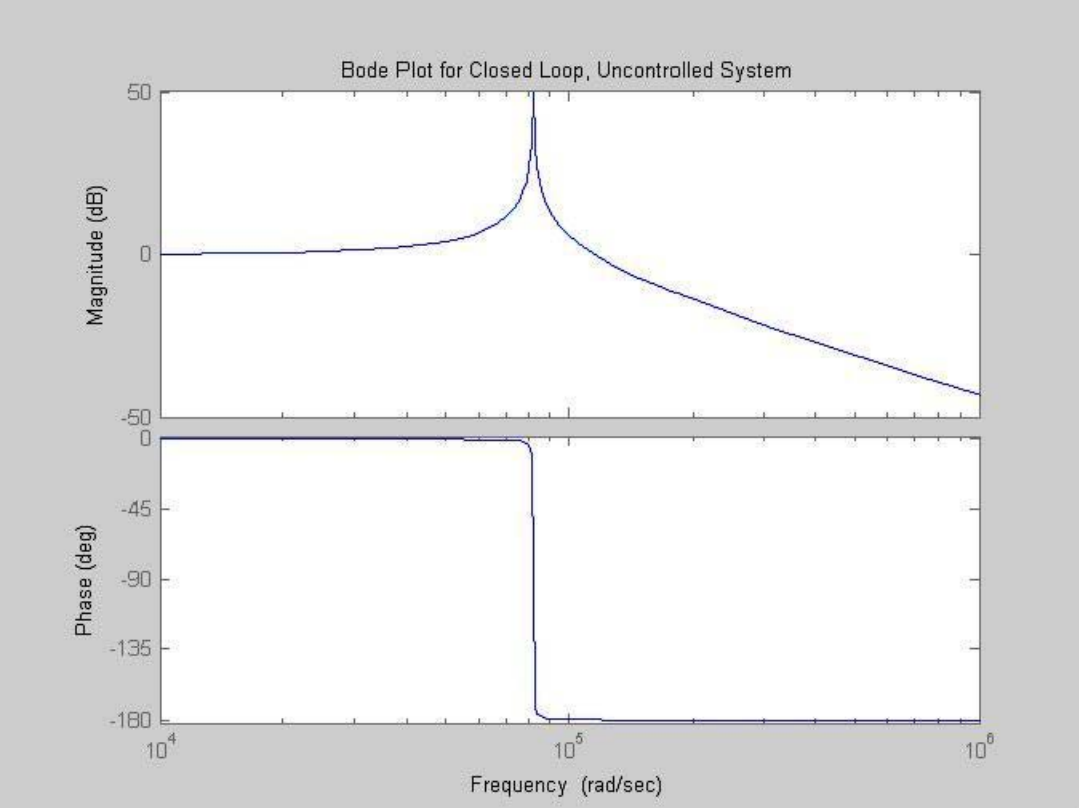


Figure 29. Frequency Response of Uncontrolled, Closed-Loop FBC Under Full Load

The large peak of over 50 dB can cause the system to suffer large overshoots and operate outside the acceptable range of various components. This is another problem that must be corrected by the controller.

2. Minimum Load

The minimum load situation is simulated using all the previously stated variables with the exception of the load being 112.5 Ω in place of 37.5 Ω. The following transfer function and three graphs illustrate the closed-loop, uncontrolled system response during minimum loading. Figure 30 shows the root locus of the system, and Figure 31 displays the step response of the system. The frequency response is shown in Figure 32. From

Equation 3-27, the transfer function is

$$\frac{\hat{V}_c}{\hat{d}} = \frac{500}{7.5e^{-8}s^2 + 6.667e^{-6}s + 1}. \tag{4-9}$$

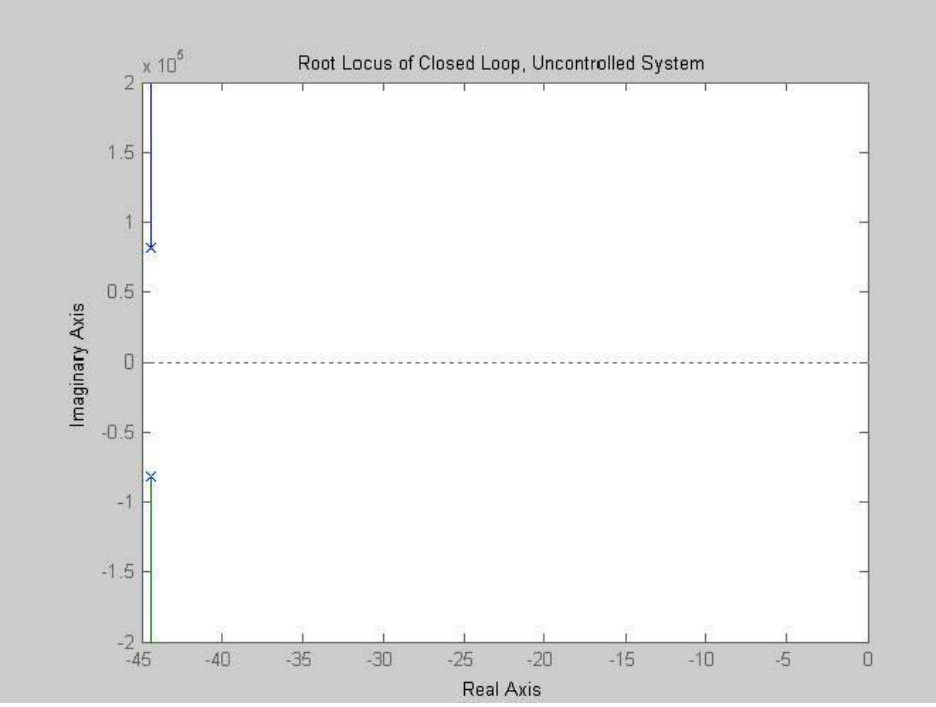


Figure 30. Root Locus of Uncontrolled, Closed-Loop FBC Under Minimum Load

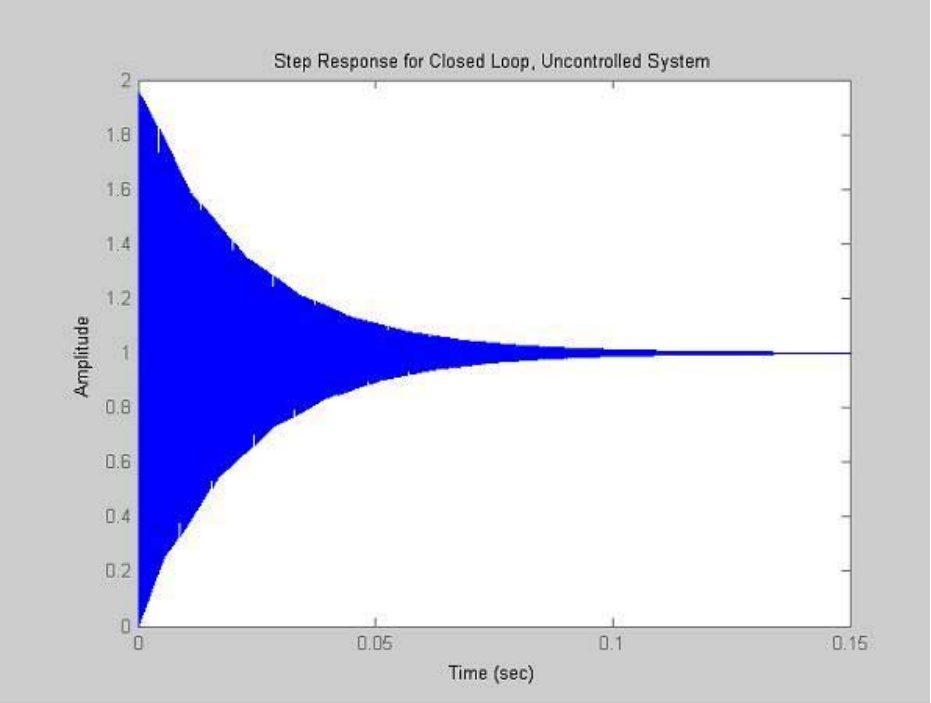


Figure 31. Step Response of Uncontrolled, Closed-Loop FBC Under Minimum Load

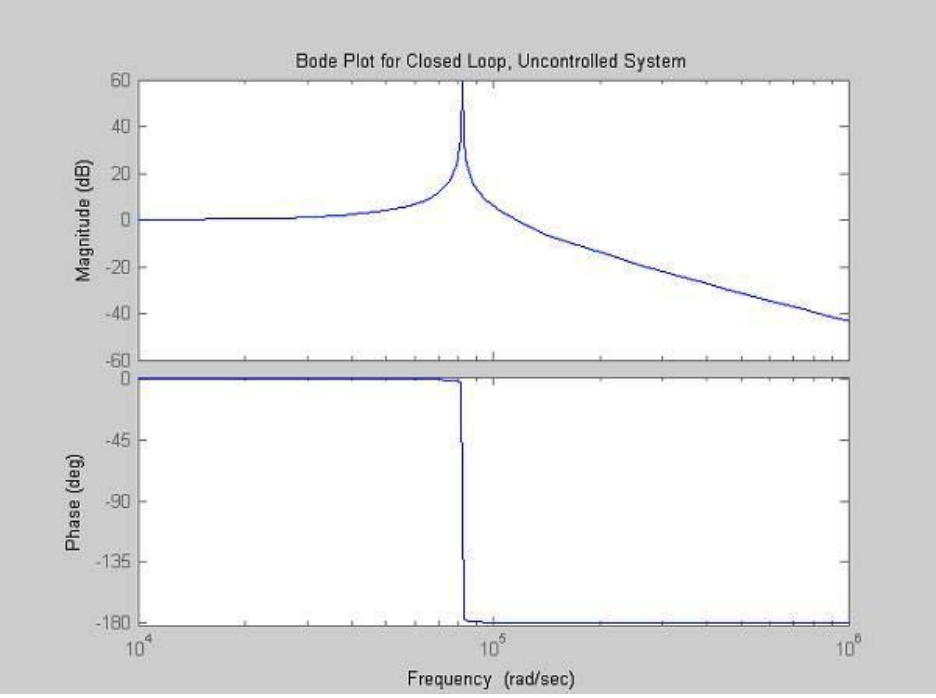


Figure 32. Frequency Response of Uncontrolled, Closed-Loop FBC Under Minimum Load

The uncontrolled system response with minimum loading illustrates the same undesirable characteristics that the uncontrolled full load system displayed. The need for a controller to decrease the settling time and to minimize the overshoot is evident.

D. CONTROLLED, CLOSED-LOOP SYSTEM RESPONSE

1. Full Load

The control method detailed in Chapter III was simulated under full load conditions. The output was treated as a resistance of 37.5 Ω while maintaining all the previous assumptions and calculations. The controlled, closed-loop transfer function is displayed below,

$$\frac{\hat{V}_c}{\hat{d}} = \frac{1.33e^8 + 1.667e^{11}}{s^3 + 1.342e^4 s^2 + 1.467e^8 s + 1.667e^{11}}. \tag{4-10}$$

Next, it was vitally important to ensure that the new, controlled system remained stable. The best manner to do so was to view the root locus of the system and verify that all poles remained in the left-half plane, as illustrated by Figure 33.

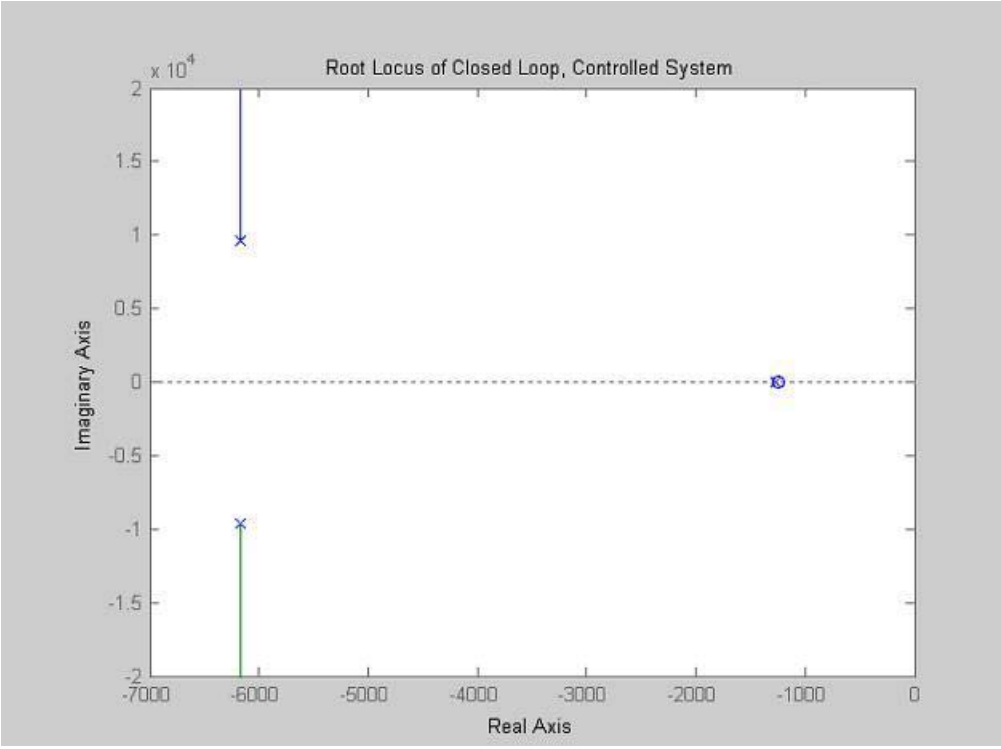


Figure 33. Root Locus of Controlled, Closed-Loop FBC Under Full Load

Notice that the poles of the system are located at $(-1270, -6076 \pm j9711)$. All poles are located in the left half plane ensuring stability. Although the imaginary portions of the two complex poles are larger than the real portion, it was observed that the system was not oscillatory; therefore, the pole locations were not altered as they result in desirable results. The system response to a step function is shown in Figure 34.

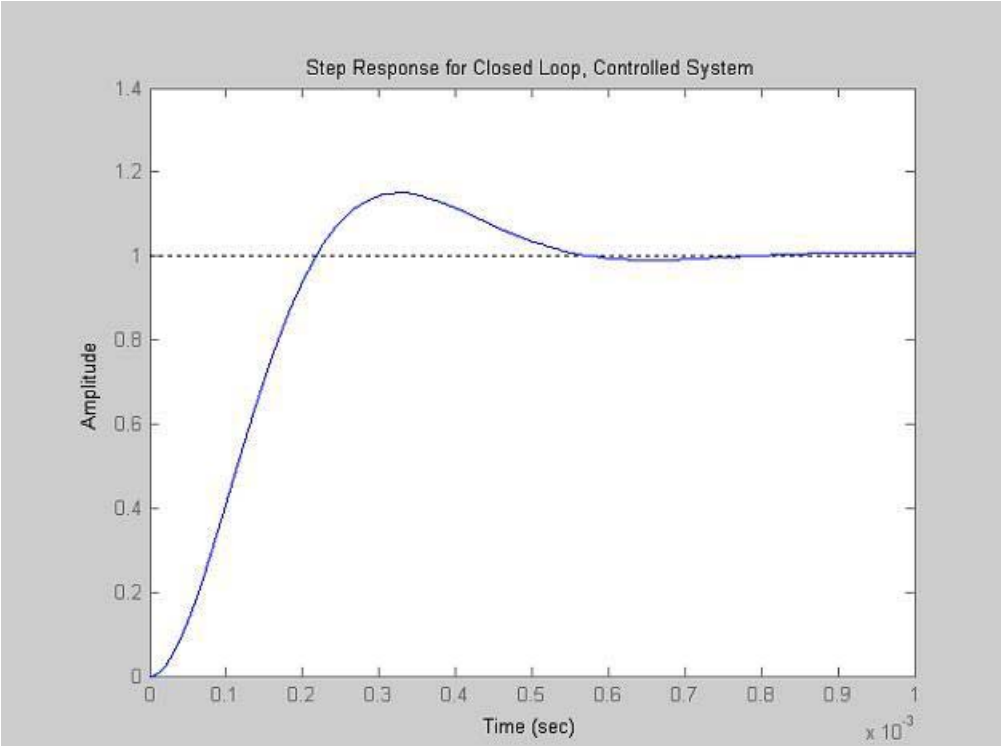


Figure 34. Step Response of Controlled, Closed-Loop FBC Under Full Load

Notice how the system now has a small overshoot of approximately 17%. The system also settles in 0.68 ms. Both the overshoot and system settling times are much smaller than the uncontrolled system proving the success of the controller. The Bode plot of the system is examined in Figure 35.

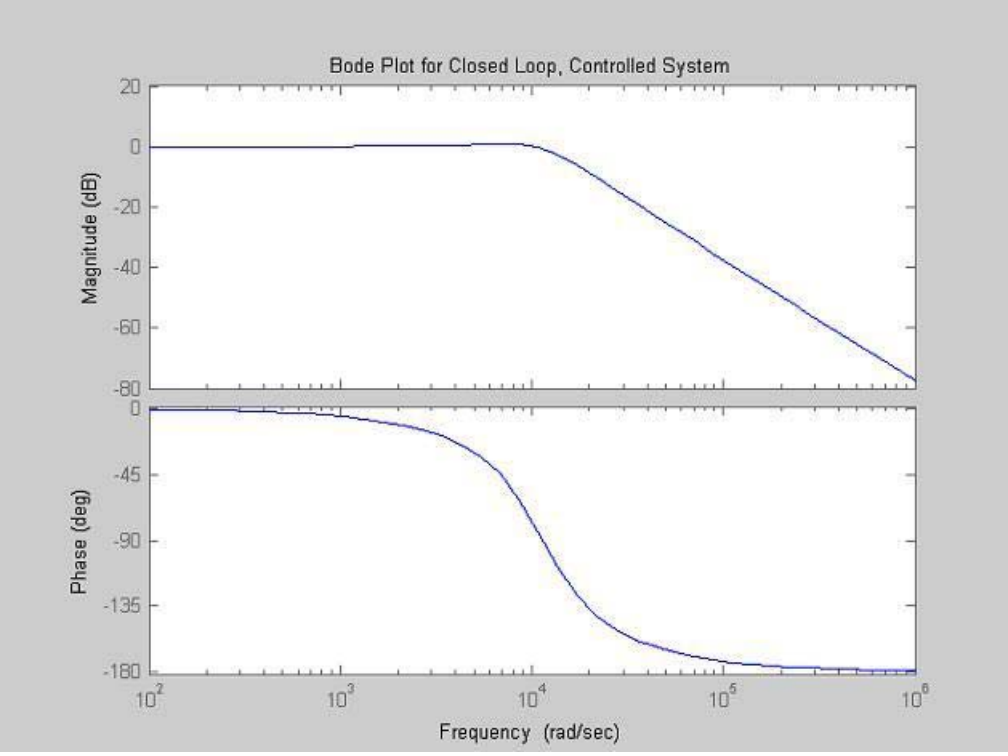


Figure 35. Frequency Response of Uncontrolled, Closed-Loop FBC Under Full Load

Notice how there is no large peak that would cause undesirable system responses.

2. Minimum Load

The system must now be simulated under minimum loading to ensure that the system can handle the required operating range of 37.5 Ω to 112.5 Ω. The resistance was set to 112.5 Ω for these simulations. Figure 36 displays the root locus of the system, and Figure 37 illustrates the system's response to a step input. Figure 38 shows the system frequency response by showing the Bode plot. The system transfer function is

$$\frac{\hat{V}_c}{\hat{d}} = \frac{1.333e^8 s + 1.667e^{11}}{s^3 + 1.342e^4 s^2 + 1.467e^8 s + 1.667e^{11}}. \tag{4-11}$$

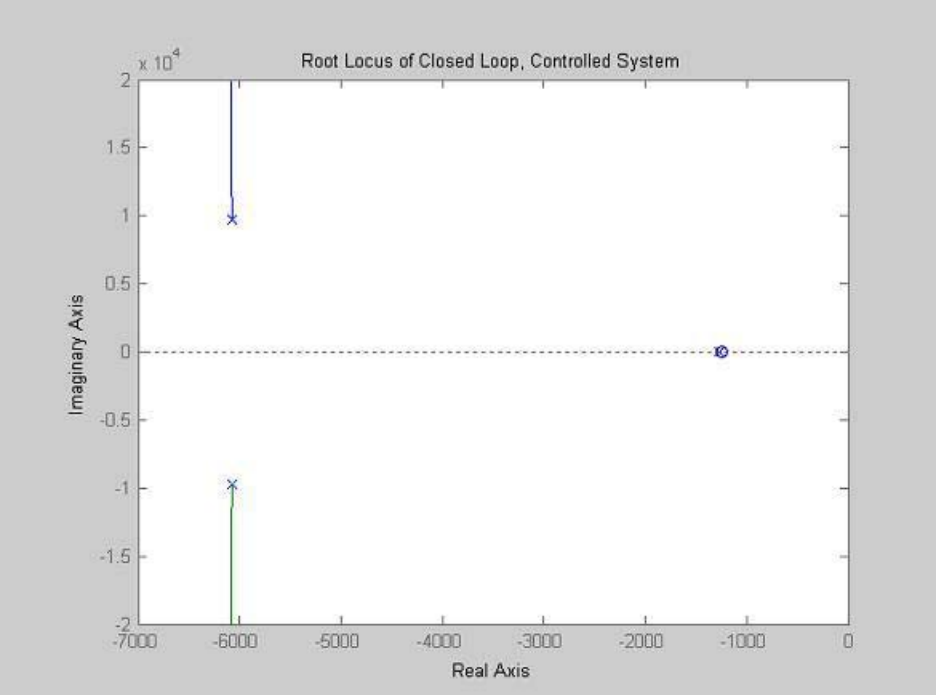


Figure 36. Root Locus of Controlled, Closed-Loop FBC Under Minimum Load

Figure 36 has several important characteristics. The root locus has no poles in the right-half plane indicating that the system was stable. The pole and hole located near -1250 on the real axis are close enough to cancel each other out. The two poles located at $-6125 \pm j9750$ are close enough to the real axis to prevent excess oscillations.

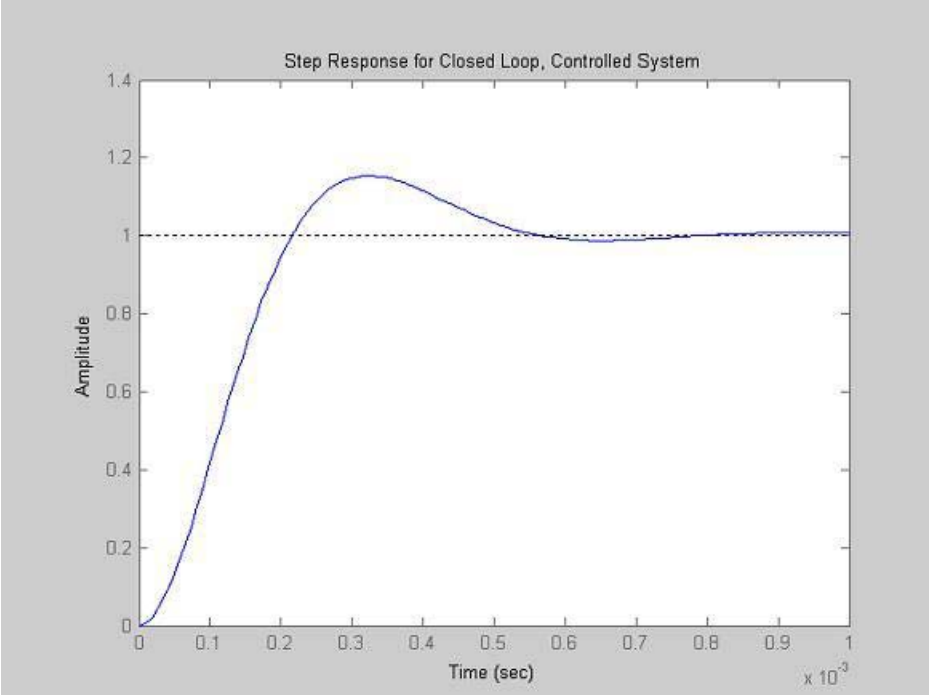


Figure 37. Step Response of Controlled, Closed-Loop FBC Under Minimum Load

The step response of the system under minimum load was excellent. The system became stable at 0.66 ms. The overshoot reached a maximum of only 17%.

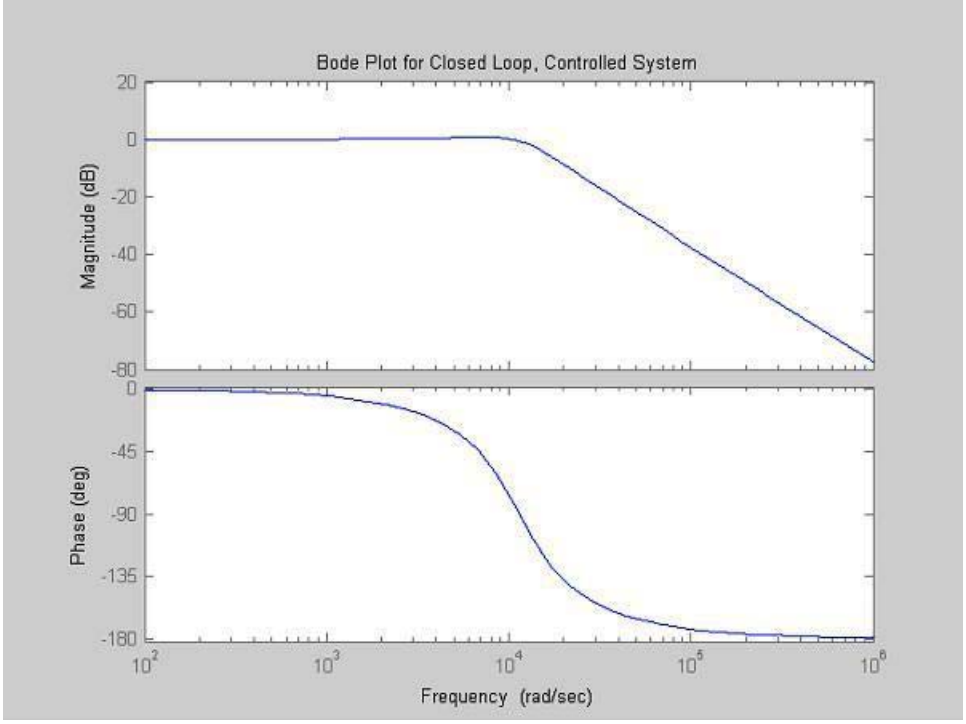


Figure 38. Frequency Response of Controlled, Closed-Loop FBC Under Minimum Load

The frequency response of the system while under minimum load was nearly ideal as shown by Figure 38. The system was proven to operate as required under minimum loading, and the FBC was shown to be successful at handling extremely large load fluctuations while exhibiting virtually no adverse characteristics.

E. SYSTEM EFFICIENCY

1. System Power

Since the theoretical efficiency of the FBC needs to be addressed, the input power supplied to the converter is the best starting point. The input power to the converter can be calculated as follows [7]:

$$I_{,MAX} = DE\left[\frac{1}{R} + \frac{(1-D)T}{2L}\right] = (0.6)(500)\left[\frac{1}{75} + \frac{(0.4)(0.00005)}{(2)(0.00075)}\right] = 8 \text{ A}, \qquad (4\text{-}12)$$

$$I_{,MIN} = DE\left[\frac{1}{R}\frac{(1-D)T}{2L}\right] = (0.6)(500)\left[\frac{1}{75} - \frac{(0.4)(0.00005)}{(2)(0.00075)}\right] = 0, \quad (4\text{-}13)$$

$$I_{,SOURCE} = \left[\frac{I_{,MAX} + I_{,MIN}}{2}\right]D = \left[\frac{8+0}{2}\right](0.6) = 2.4 \text{ A}, \quad (4\text{-}14)$$

and

$$P_{,SOURCE} = EI_{,SOURCE} = (500)(2.4) = 1,200 \text{ W}. \quad (4\text{-}15)$$

2. IGBT Switching Losses

The IGBTs have unavoidable losses known as switching losses. The switching losses can be accurately estimated using the tables provided in the data sheet for the IGBT located in Appendix A [16]. The switching losses per IGBT, based on operating at rated voltage, current, and frequency, is 8 W. Thirty-two Watts are lost due to switching losses total because there are four IGBTs in the FBC. The 32-W represents 2.67% loss of efficiency.

3. Transformer Losses

The transformer to be used is a METGLAS transformer with a 2705M alloy core whose power consumption is described in References [16,17]. The power consumed by the transformer was 7.56 W resulting in an efficiency loss of 0.63%.

4. Bridge Rectifier

By selecting the IXYS FBE 22-06N1 Fast Single Phase Rectifier Bridge, the power dissipated in the diodes is 0.2 W per diode. The total power consumed by the diodes will be 0.8 W or 0.0667% [18].

5. Other Losses

There are various other losses associated in the FBC that are less of an influence on the overall system efficiency. There are losses due to inductance, capacitance, and

resistance in the conductors. Those losses will typically result in an efficiency loss of 1.0%.

6. Output Power

The total losses in the system amount to less than 60 W when liberally allowing for other losses. The system has an overall efficiency of at least 95%. The output power will be 1140 W.

F. CHAPTER REVIEW

Chapter IV showcased the ability of the FBC to operate both efficiently and responsively. The converter has an efficiency of over 95%, and the control schemes derived by prior work at NPS for "buck choppers" could be utilized. Chapter V will draw conclusions about the FBC and offer advice for future research.

V. CONCLUSIONS

A. SUMMARY OF FINDINGS

This research proved that a FBC could be constructed with Commercial Off-the-Shelf (COTS) parts in an efficient manner (Parts list is displayed in Appendix C). Also, this research proved that the control schemes for "buck choppers" that have been researched at NPS could be used to control the FBC. The key areas analyzed in this thesis are:

- Detailed schematics,
- Galvanic isolation,
- State-space analysis of FBC,
- Simulation of FBC, and
- PID control of FBC.

This research proves that a FBC is a feasible option for use as a SSCM. The FBC is able to operate in a step-up, step-down, or unity-gain isolation mode. The ability of the FBC to operate in three modes allows the converter to replace the buck converter, the boost converter, and the buck-boost converter. Also, by only using one converter topology throughout any future naval vessel's EDS, there would be a reduction in the training necessary to maintain the proper operation of the EDS.

B. FUTURE WORK

As the United States Navy moves towards the implementation of a new EDS, it will be necessary to continue to research DC-DC converters. The FBC serves to increase the reliability and survivability of future naval vessels by galvanically isolating the source and the load. Future work that can be done to better understand and improve the FBC includes:

- Building/testing the converter simulated in this thesis,
- Operating the inverter portion of the FBC in a pulse-width modulation mode,
- Researching/testing alternative components, and/or
- Varying the operating characteristics to monitor effects on efficiency.

Since the move to an improved EDS is almost certain, it would be prudent to design the EDS to be as reliable as possible. The galvanic isolation created by the FBC, as well as its other advantages over conventional choppers, outweighs the minor loss of efficiency caused by the transformer.

APPENDIX A. DATA SHEETS

Appendix A contains the data sheets for components of the FBC detailed in this thesis. The data sheets provide vital operating characteristics for future work done relating to this thesis.

A. SEMIKRON SK 45 GH 063 IGBT MODULE [15]

SK 45 GH 063

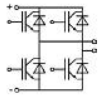
SEMIKRON

Absolute Maximum Ratings			
Symbol	Conditions [1]	Values	Units
V_{CES}		600	V
V_{GES}		± 20	V
I_C	T_h = 25/80 °C	45 / 30	A
I_{CM}	t_p < 1 ms; T_h = 25/80 °C	90 / 60	A
$I_F = -I_C$	T_h = 25/80 °C	57 / 38	A
$I_{FM} = -I_{CM}$	t_p < 1 ms; T_h = 25/80 °C	114 / 76	A
T_j		– 40 ... + 150	°C
T_{stg}		– 40 ... + 125	°C
T_{sol}	Terminals, 10 s	260	°C
V_{isol}	AC, 1 min	2500	V

Characteristics					
Symbol	Conditions [1]	min.	typ.	max.	Units
V_{CEsat}	I_C = 30 A; T_j = 25 (125) °C	–	1,8(2,0)	–	V
$t_{d(on)}$	V_{CC} = 300 V; V_{GE} = ± 15 V	–	45	–	ns
t_r	I_C = 30 A, T_j = 125 °C	–	35	–	ns
$t_{d(off)}$	$R_{Gon} = R_{Goff}$ = 22 Ω	–	250	–	ns
t_f	inductive load	–	25	–	ns
$E_{on} + E_{off}$		–	2,65	–	mJ
C_{ies}		–	2,8	–	nF
R_{thjh} [3]		–	–	1,0	K/W
Inverse Diode [2]					
$V_F = V_{EC}$	I_F = 30 A; T_j = 25 (125) °C	–	1,3(1,2)	1,5(1,45)	V
V_{TO}	T_j = 125 °C	–	0,85	0,9	V
r_T	T_j = 125 °C	–	8	16	mΩ
I_{RRM}	I_F = 30 A; V_R = 300 V	–	30	–	A
Q_{rr}	di_F/dt = – 500 A/µs	–	3,0	–	µC
E_{off}	V_{GE} = 0 V; T_j = 125 °C	–	0,9	–	mJ
R_{thjh} [3]	per Diode	–	–	1,2	K/W
Mechanical Data					
M_1	mounting torque	–	–	2,5	Nm
w		–	30	–	g
Case			T 19		

SEMITOP® 3
IGBT Module

SK 45 GH 063



GH

Features

- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminium oxide ceramic (DCB)
- N channel, homogeneous Silicon structure (NPT-Non punch-through IGBT)
- High short circuit capability
- Low tail current with low temperature dependence
- UL recognized, file no. E 63 532

Typical Applications

- Switching (not for linear use)
- Inverter
- Switched mode power supplies
- UPS

[1] T_h = 25 °C, unless otherwise specified
[2] CAL = Controlled Axial Lifetime Technology (soft and fast recovery)
[3] Thermal resistance junction to heatsink

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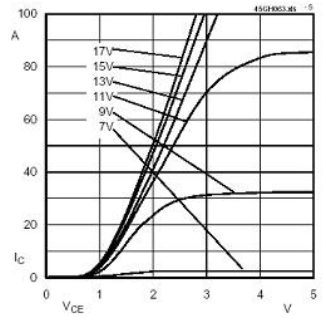

Fig. 5 Typ. output characteristic, t_p = 80 µs; 25 °C

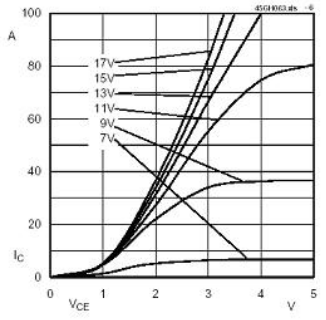

Fig. 6 Typ. output characteristic, t_p = 80 µs; 125 °C

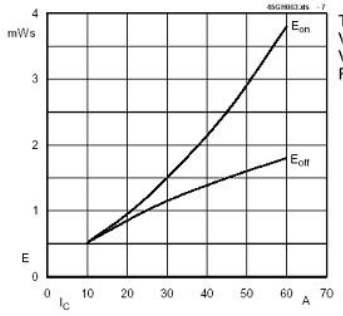

Fig. 7 Turn-on /-off energy = f (I_C)

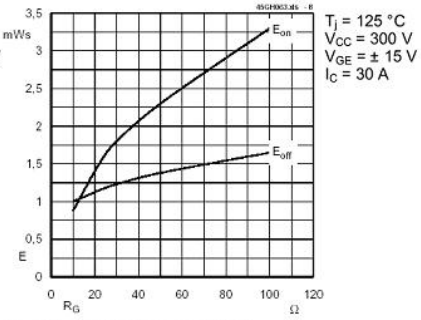

Fig. 8 Turn-on /-off energy = f (R_G)

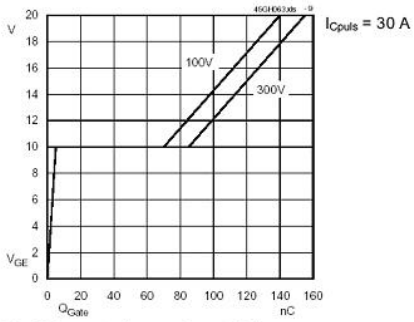

Fig. 9 Typ. gate charge characteristic

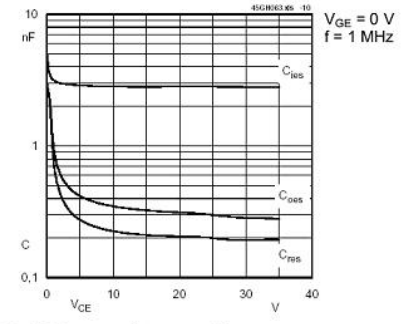

Fig. 10 Typ. capacitances vs. V_{CE}

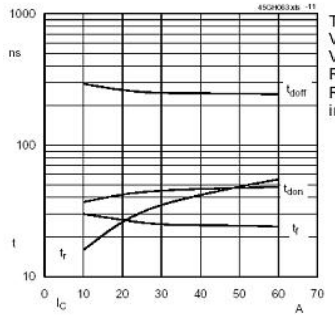

Fig. 11 Typ. switching times vs. I_C

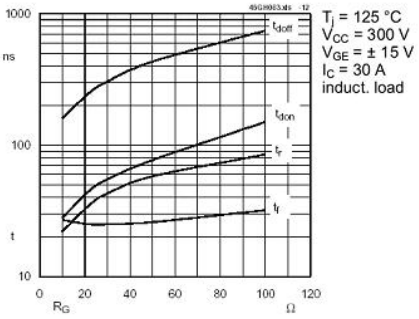

Fig. 12 Typ. switching times vs. gate resistor R_G

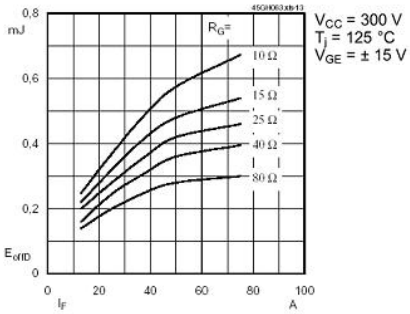

Fig. 13 Diode turn-off energy dissipation per pulse

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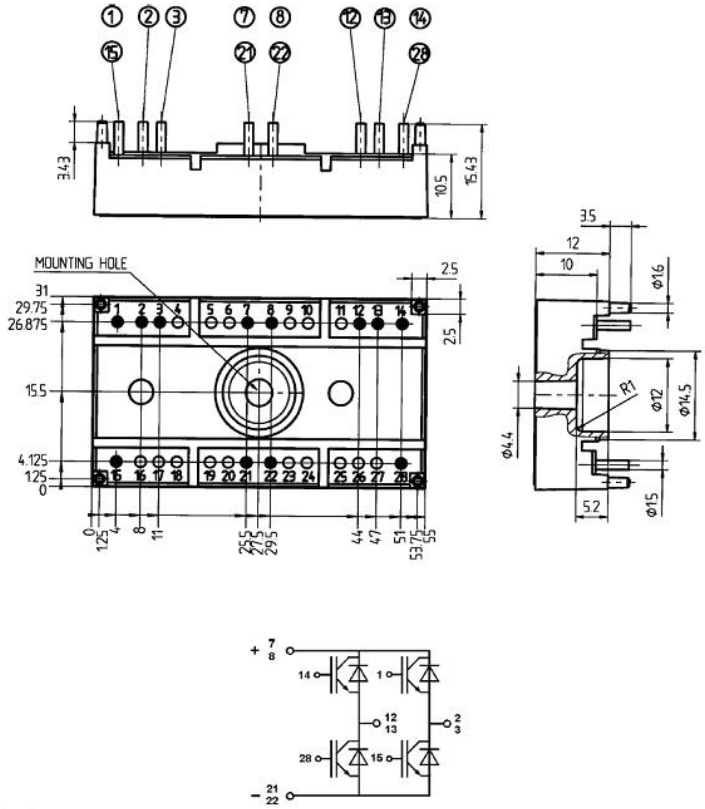

Dimensions in mm

B. SEMIKRON IGBT DRIVER BOARD [15]

SKHI 21 A, SKHI 22 A / B

SEMIKRON

Absolute Maximum Ratings

Symbol	Term		Values	Units
V_S	Supply voltage prim.		18	V
V_{iH}	Input signal volt. (High)	SKHIxxA	V_S + 0,3	V
		SKHI22B	5 + 0,3	V
$Iout_{PEAK}$	Output peak current		8	A
$Iout_{AVmax}$	Output average current		40	mA
f_{max}	max. switching frequency		50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT		1700	V
dv/dt	Rate of rise and fall of voltage secondary to primary side		50	kV/µs
V_{isolIO}	Isolation test voltage	Standard	2500	Vac
	input-output (2 sec.AC)	Version „H4"	4000	Vac
V_{isolI2}	Isolation test voltage ouput 1 - output 2 (2 sec.AC)		1500	V
R_{Gonmin}	Minimum rating for R_{Gon}		3	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}		3	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse		4 [1]	µC
T_{op}	Operating temperature		- 40... + 85	°C
T_{stg}	Storage temperature		- 40... + 85	°C

Electrical Characteristics (T_a = 25 °C)

Symbol	Term		Values min.	typ.	max.	Units
V_S	Supply voltage primary side		14,4	15	15,6	V
I_{SO}	Supply current primary side (no load)		–	80	–	mA
	Supply current primary side (max.)		–	–	290	mA
V_I	Input signal voltage	SKHIxxA on/off	–	15 / 0	–	V
		SKHI22B on/off	–	5 / 0	–	V
V_{IT+}	Input threshold voltage (High)	SKHIxxA	10,9	11,7	12,5	V
		SKHI22B	3,5	3,7	3,9	V
V_{IT-}	Input threshold voltage (Low)	SKHIxxA	4,7	5,5	6,5	V
		SKHI22B	1,5	1,75	2,0	V
R_{in}	Input resistance	SKHIxxA	–	10	–	kΩ
		SKHI22B	–	3,3	–	kΩ
$V_{G(on)}$	Turn on gate voltage output		–	+15	–	V
$V_{G(off)}$	Turn off gate voltage output	SKHI22x	–	-7	–	V
		SKHI21A	–	0	–	V
R_{GE}	Internal gate-emitter resistance		–	22	–	kΩ
f_{ASIC}	Asic system switching frequency		–	8	–	MHz
$t_{d(on)IO}$	Input-output turn-on propagation time		0,85	1	1,15	µs
$t_{d(off)IO}$	Input-output turn-off propagation time		0,85	1	1,15	µs
$t_{d(err)}$	Error input-output propagation time		–	0,6	–	µs
$t_{pERRRESET}$	Error reset time		–	9	–	µs
t_{TD}	Top-Bot Interlock Dead Time	SKHI22x	3,3	–	4,3	µs
		SKHI21A	0	–	4,3	µs
V_{CEstat}	Reference voltage for V_{CE}-monitoring		–	5 [2]	10	V
			–	6 [3]	10	V
C_{ps}	Coupling capacitance primary secondary		–	12	–	pF
MTBF	Mean Time Between Failure T_a = 40° C		–	2,0	–	10^6 h
m	weight		–	45	–	g

SEMIDRIVER®
Hybrid Dual IGBT Driver
SKHI 22 A / B

- Double driver for halfbridge IGBT modules
- SKHI 22 A/B H4 is for 1700 V-IGBT
- SKHI 22 A is compatible to old SKHI 22
- SKHI 22 B has additional functionality

Hybrid Dual MOSFET Driver
SKHI 21 A

- drives MOSFETs with $V_{DS(on)}$ < 10 V
- is compatible to old SKHI 21

Preliminary Data

Features

- CMOS compatible inputs
- Short circuit protection by V_{CE} monitoring and switch off
- Drive interlock top/bottom
- Isolation by transformers
- Supply undervoltage protection (13 V)
- Error latch/output

Typical Applications

- Driver for IGBT and MOSFET modules in bridge circuits in choppers, inverter drives, UPS and welding inverters
- DC bus voltage up to 1200V

[1] see fig. 6
[2] At R_{CE} = 18 kΩ, C_{CE} = 330pF
[3] At R_{CE} = 36 kΩ, C_{CE} = 470pF, R_{VCE} = 1kΩ

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External Components

Component	Function	Recommended Value
R_{CE}	Reference voltage for V_{CE}-monitoring $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1,4$ (1) with R_{VCE} = 1kΩ (1700V IGBT): $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1,8$ (1.1)	10kΩ < R_{CE} < 100kΩ 18kΩ for SKM XX 123 (1200V) 36kΩ for SKM XX 173 (1700V)
C_{CE}	Inhibit time for V_{CE} - monitoring $t_{min} = \tau_{CE} \cdot \ln\left[\frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}(V)}\right]$ (2) $\tau_{CE}(\mu s) = C_{CE}(nF) \cdot \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)}$ (3)	C_{CE} < 2,7nF 0,33nF for SKM XX 123 (1200V) 0,47nF for SKM XX 173 (1700V) 0,5µs < t_{min} < 10µs
R_{VCE}	Collector series resistance for 1700V IGBT-operation	1kΩ / 0,4W
R_{ERROR}	Pull-up resistance at error output $\frac{U_{Pull-Up}}{R_{ERROR}} < 15mA$	1kΩ < R_{ERROR} < 10kΩ
R_{GON}	Turn-on speed of the IGBT [4]	R_{GON} > 3Ω
R_{GOFF}	Turn-off speed of the IGBT [5]	R_{GOFF} > 3Ω

[4] Higher resistance reduces free-wheeling diode peak recovery current, increases IGBT turn-on time.
[5] Higher resistance reduces turn-off peak voltage, increases turn-off time and turn-off power dissipation

PIN array

Fig. 2 shows the pin arrays. The input side (primary side) comprises 10 inputs (SKHI 22A / 21A 8 inputs), forming the interface to the control circuit (see fig.1).

The output side (secondary side) of the hybrid driver shows two symmetrical groups of pins with 4 outputs, each forming the interface to the power module. All pins are designed for a grid of 2,54 mm.

Primary side PIN array

PIN No.	Designation	Explanation
P14	GND / 0V	related earth connection for input signals
P13	V_S	+ 15V ± 4% voltage supply
P12	V_{IN1}	switching signal input 1 (TOP switch) positive 5V logic (for SKHI22A /21A, 15V logic)
P11	free	not wired
P10	/ERROR	error output, low = error; open collector output; max 30V / 15mA (for SKHI22A /21A, internal 10kΩ pull-up resistor versus V_S)
P9	TDT2	signal input for digital adjustment of interlocking time; **SKHI22B: to be switched by bridge to GND (see fig. 3)** **SKHI22A /21A: to be switched by bridge to V_S**
P8	V_{IN2}	switching signal input 2 (BOTTOM switch); positive 5V logic (for SKHI22A /21A, 15V logic)
P7	GND / 0V	related earth connection for input signals
P6	SELECT	signal input for neutralizing locking function; to be switched by bridge to GND
P5	TDT1	signal input for digital adjustment of locking time; to be switched by bridge to GND

ATTENTION: Inputs P6 and P5 are not existing for SKHI 22A/ 21A. The contactor tracks of the digital input signals P5/ P6/ P9 must not be longer than 20 mm to avoid interferences, if no bridges are connected.

Secondary side PIN array

PIN No.	Designation	Explanation
S20	V_{CE1}	collector output IGBT 1 (TOP switch)
S15	C_{CE1}	reference voltage adjustment with R_{CE} and C_{CE}
S14	G_{ON1}	gate 1 R_{ON} output
S13	G_{OFF1}	gate 1 R_{OFF} output
S12	E1	emitter output IGBT 1 (TOP switch)
S1	V_{CE2}	collector output IGBT 2 (BOTTOM switch)
S6	C_{CE2}	reference voltage adjustment with R_{CE} and C_{CE}
S7	G_{ON2}	gate 2 R_{ON} output
S8	G_{OFF2}	gate 2 R_{OFF} output
S9	E2	emitter output IGBT 2 (BOTTOM switch)

ATTENTION: The connector leads to the power module should be as short as possible.

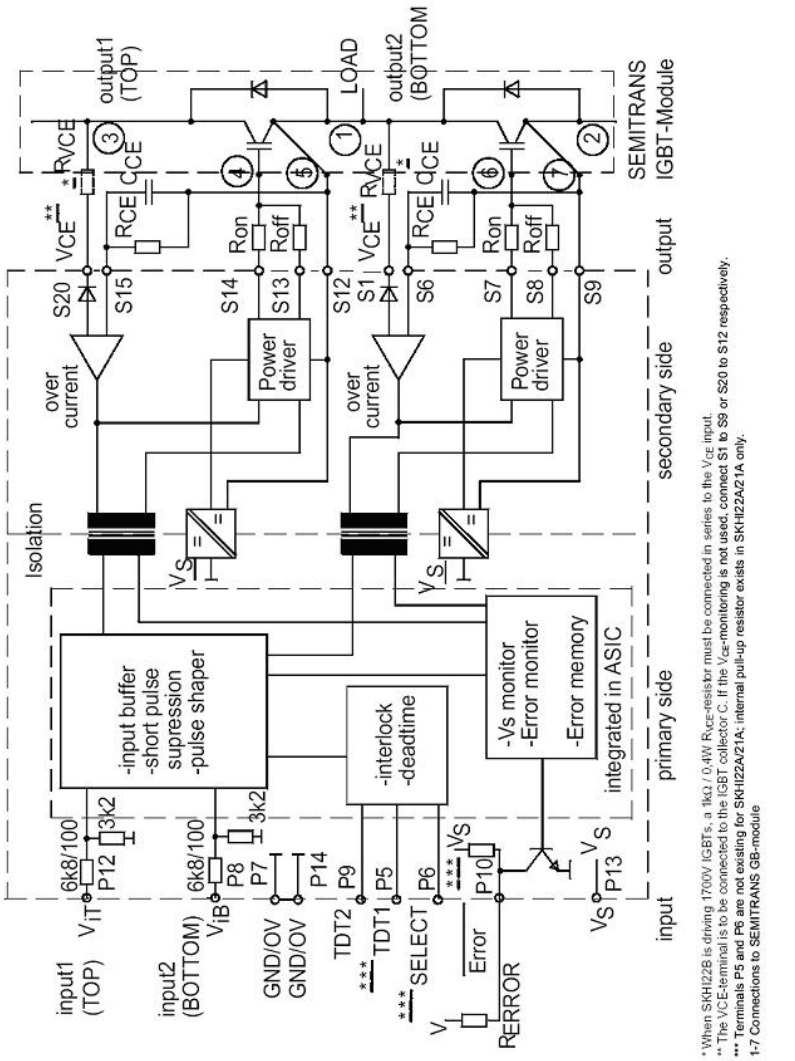

Fig. 1 Block diagram of SKHI 22 A / B / 21 A

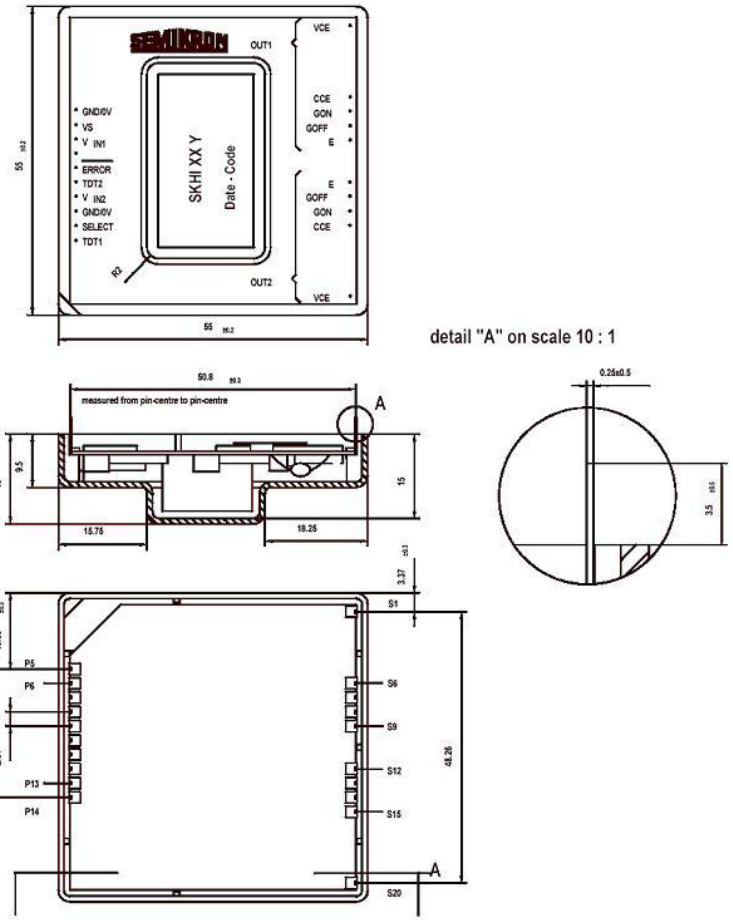

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Fig. 2 Dimension drawing and PIN array (P5 and P6 are not existing for SKHI22A/21A)

SEMIDRIVER®

SKHI 22A / 22B und SKHI 21A

Hybrid dual drivers

The driver generation SKHI 22A/B and SKHI 21A will replace the hybrid drivers SKHI 21/22 and is suitable for all available low and medium power range IGBT and MOSFETs.

The SKHI 22A (SKHI 21A) is a form-, fit- and mostly function-compatible replacement to its predecessor, the SKHI 22 (SKHI 21).

The SKHI 22B is recommended for any new development. It has two additional signal pins on the primary side with which further functions may be utilized.

The SKHI 22A and SKHI 22B are available with standard isolation (isolation testing voltage 2500 VAC, 1min) as well as with an increased isolation voltage (type "H4") (isolation testing voltage 4000 VAC, 1min). The SKHI 21A is only offered with standard isolation features.

Differences SKHI 22-22A (SKHI 21-21A)

Compared to the old SKHI 22/21 the new driver SKHI 22A / 21A is absolutely compatible with regards to pins and mostly with regards to functions. It may be equivalently used in existing PCBs.

The following points have to be considered when exchanging the drivers:

- **Leave out the two resistors RTD for interlocking dead time adjustment at pin 11 and pin 9.**
- **The interlocking time of the driver stages in halfbridge applications is adjusted to 3,25 µs. It may be increased up to 4,25 µs by applying a 15 V (VS) supply voltage at Pin 9 (TDT2) (wire bridge)**
- **The error reset time is typically 9µs.**
- **The input resistance is 10 kΩ.**

As far as the SKHI 22A is concerned, the negative gate voltage required for turn-off of the IGBT is no longer -15V, but -7V.

General description

The new driver generation SKHI 22A/B, SKHI 21A consists of a hybrid component which may directly be mounted to the PCB.

All devices necessary for driving, voltage supply, error monitoring and potential separation are integrated in the driver. In order to adapt the driver to the used power module, only very few additional wiring may be necessary.

The forward voltage of the IGBT is detected by an integrated short-circuit protection, which will turn off the module when a certain threshold is exceeded.

In case of short-circuit or too low supply voltage the integrated error memory is set and an error signal is generated.

The driver is connected to a controlled + 15 V-supply voltage. The input signal level is 0/15 V for the SKHI 22A/ 21A and 0/5 V for the SKHI 22B.

In the following explanations the whole driver family will be designated as SKHI 22B. If a special type is referred to, the concerned driver version will explicitly be named.

Technical explanations[1]

Description of the circuit block diagram and the functions of the driver

The block diagram (fig.1) shows the inputs of the driver (primary side) on the left side and the outputs (secondary side) on the right.

The following functions are allocated to the primary side:

Input-Schmitt-trigger, CMOS compatible, positive logic (input high = IGBT on)

Interlock circuit and deadtime generation of the IGBT

If one IGBT is turned on, the other IGBT of a halfbridge cannot be switched. Additionally, a digitally adjustable interlocking time is generated by the driver (see fig. 3), which has to be longer than the turn-off delay time of the IGBT. This is to avoid that one IGBT is turned on before the other one is not completely discharged. This protection-function may be neutralized by switching the select input (pin6) (see fig. 3). fig. 3 documents possible interlock-times. "High" value can be achieved with no connection and connection to 5 V as well.

P6 ; SELECT	P5 ; TDT1	P9 ; TDT2	interlock time t_{TD}/µs
open / 5V	GND	GND	1,3
open / 5V	GND	open / 5V	2,3
open / 5V	open / 5V	GND	3,3
open / 5V	open / 5V	open / 5V	4,3
GND	X	X	no interlock

Fig. 3 SKHI 22B - Selection of interlock-times: „High"-level can be achieved by no connection or connecting to 5 V

Short pulse suppression

The integrated short pulse suppression avoids very short switching pulses at the power semiconductor caused by high-frequency interference pulses at the driver input signals. Switching pulses shorter than 500 ns are suppressed and not transmitted to the IGBT.

Power supply monitoring (V_S)

A controlled 15 V-supply voltage is applied to the driver. If it falls below 13 V, an error is monitored and the error output signal switches to low level.

1. The following descriptions apply to the use of the hybrid driver for IGBTs as well as for power MOSFETs. For the reason of shortness, only IGBTs will be mentioned in the following. The designations "collector" and "emitter" will refer to IGBTs, whereas for the MOSFETs "drain" and "source" are to be read instead.

Error monitoring and error memory

The error memory is set in case of under-voltage or short-circuit of the IGBTs. In case of short-circuit, an error signal is transmitted by the V_{CE}-input via the pulse transformers to the error memory. The error memory will lock all switching pulses to the IGBTs and trigger the error output (P10) of the driver. The error output consists of an open collector transistor, which directs the signal to earth in case of error. SEMIKRON recommends the user to provide for a pull-up resistor directly connected to the error evaluation board and to adapt the error level to the desired signal voltage this way. The open collector transistor may be connected to max. 30 V / 15 mA. If several SKHI 22Bs are used in one device, the error terminals may also be paralleled.

ATTENTION: Only the SKHI 22A / 21A is equipped with an internal pull-up resistor of 10 kΩ versus V_S. The SKHI 22B does not contain an internal pull-up resistor.

The error memory may only be reset, if no error is pending and both cycle signal inputs are set to low for > 9 µs at the same time.

Pulse transformer set

The transformer set consists of two pulse transformers one is used bidirectional for turn-on and turn-off signals of the IGBT and the error feedback between primary and secondary side, the other one for the DC/DC-converter. The DC/DC-converter serves as potential-separation and power supply for the two secondary sides of the driver. The isolation voltage for the "H4"-type is 4000 V_{AC} and 2500 V_{AC} for all other types.

The secondary side consists of two symmetrical driver switches integrating the following components:

Supply voltage

The voltage supply consists of a rectifier, a capacitor, a voltage controller for - 7 V and + 15 V and a + 10 V reference voltage.

Gate driver

The output transistors of the power drivers are MOSFETs. The sources of the MOSFETs are separately connected to external terminals in order to provide setting of the turn-on and turn-off speed by the external resistors R_{ON} and R_{OFF}. Do not connect the terminals S7 with S8 and S13 with S14, respectively. The IGBT is turned on by the driver at + 15 V by R_{ON} and turned off at - 7 V by R_{OFF}. R_{ON} and R_{OFF} may not chosen below 3 Ω. In order to ensure locking of the IGBT even when the driver supply voltage is turned off, a 22 kΩ-resistor versus the emitter output (E) has been integrated at output G_{OFF}.

V_{CE}-monitoring

The V_{CE}-monitoring controls the collector-emitter voltage V_{CE} of the IGBT during its on-state. V_{CE} is internally limited to 10 V. If the reference voltage V_{CEref} is exceeded, the IGBT will be switched off and an error is indicated. The reference voltage V_{CEref} may dynamically be adapted to the IGBTs switching behaviour. Immediately after turn-on of the IGBT, a higher value is effective than in the steady state. This value will, however, be reset, when the IGBT is turned off. V_{CEstat} is the steady-state value of V_{CEref} and is adjusted to the required maximum value for each IGBT by an external resistor R_{CE} to be connected between the terminals C_{CE} (S6/S15) and E (S9/S12). It may not exceed 10 V. The time constant for the delay of V_{CEref} may be increased by an external capacitor C_{CE}, which is connected in parallel to R_{CE}. It controls the time tmin which passes after turn-on of the IGBT before the V_{CE}-monitoring is activated. This makes possible any adaptation to the switching behavior of any of the IGBTs. After t_{min} has passed, the V_{CE}-monitoring will be triggered as soon as $V_{CE} > V_{CEref}$ and will turn off the IGBT.

External components and possible adjustments of the hybrid driver

Fig. 1 shows the required external components for adjustment and adaptation to the power module.

VCE - monitoring adjustment

The external components R_{CE} and C_{CE} are applied for adjusting the steady-state threshold and the short-circuit monitoring dynamic. R_{CE} and C_{CE} are connected in parallel to the terminals C_{CE} (S15/ S6) and E (S12/ S9) .

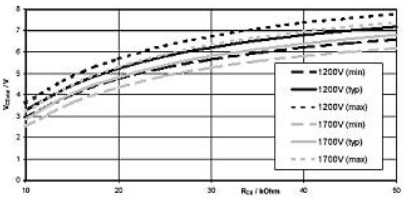

Fig. 4 V_{CEstat} in dependence of R_{CE} (T_{amb} = 25°C)

Dimensioning of R_{CE} and C_{CE} can be done in three steps:

1. Calculate the maximum forward voltage from the datasheet of the used IGBT and determine V_{CEstat}
2. Calculate approximate value of R_{CE} according to equation (1) or (1.1) from V_{CEstat} or determine R_{CE} by using fig.4.
3. Determine t_{min} and calculate C_{CE} according to equations (2) and (3).

Typical values are

for 1200 V IGBT: V_{CEstat} = 5 V; t_{min} = 1,45 µs,
R_{CE} = 18 kΩ, C_{CE} = 330 pF

for 1700 V IGBT: V_{CEstat} = 6 V; t_{min} = 3 µs,
R_{CE} = 36 kΩ, C_{CE} = 470 pF

Adaptation to 1700 V IGBT

When using 1700 V IGBTs it is necessary to connect a 1 kΩ / 0,4 W adaptation resistor between the V_{CE}-terminal (S20/ S1) and the respective collector.

Adaptation to error signal level

An open collector transistor is used as error terminal, which, in case of error, leads the signal to earth. The signal has to be adapted to the evaluation circuit's voltage level by means of an externally connected pull-up resistor. The maximum load applied to the transistor shall be 30 V / 15 mA.

As for the SKHI 22A / 21A a 10 kΩ pull-up resistor versus V_S (P13) has already been integrated in the driver.

IGBT switching speed adjustment

The IGBT switching speed may be adjusted by the resistors R_{ON} and R_{OFF}. By increasing R_{ON} the turn-on speed will decrease. The reverse peak current of the free-wheeling diode will diminish. SEMIKRON recommends to adjust R_{ON} to a level that will keep the turn-on delay time $t_{d(on)}$ of the IGBT < 1 µs.

By increasing R_{OFF} the turn-off speed of the IGBT will decrease. The inductive peak overvoltage during turn-off will diminish.

The minimum gate resistor value for R_{OFF} and R_{ON} is 3 Ω. Typical values for R_{ON} and R_{OFF} recommended by SEMIKRON are given in fig. 5

SK-IGBT-Modul	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kΩ	R_{VCE} kΩ
SKM 50GB123D	22	22	330	18	0
SKM 75GB123D	22	22	330	18	0
SKM 100GB123D	15	15	330	18	0
SKM 145GB123D	12	12	330	18	0
SKM 150GB123D	12	12	330	18	0
SKM 200GB123D	10	10	330	18	0
SKM 300GB123D	8,2	8,2	330	18	0
SKM 400GA123D	6,8	6,8	330	18	0
SKM 75GB173D	15	15	470	36	1
SKM 100GB173D	12	12	470	36	1
SKM 150GB173D	10	10	470	36	1
SKM 200GB173D	8,2	8,2	470	36	1

Fig. 5 Typical values for external components

Interlocking time adjustment

Fig. 3 shows the possible interlocking times between output1 and output2. Interlocking times are adjusted by connecting the terminals TDT1 (P5), TDT2 (P9) and SELECT (P6) either to earth/ GND (P7 and P14) according to the required function or by leaving them open.

A typical interlocking time value is 3,25 µs (P9 = GND; P5 and P6 open). For SKHI 22A / 21A the terminals TDT1 (P5) and SELECT (P6) are not existing. The interlocking time has been fixed to 3,25 µs and may only be increased to 4,25 µs by connecting TDT2 (P9) to V_S (P13).

ATTENTION: If the terminals TDT1 (P5), TDT2 (P9) and SELECT (P6) are not connected, eventually connected track on PC-board may not be longer than 20 mm in order to avoid interferences.

SEMIKRON recommends to start-up operation using the values recommended by SEMIKRON and to optimize the values gradually according to the IGBT switching behaviour and overvoltage peaks within the specific circuitry.

Driver performance and application limits

The drivers are designed for application with halfbridges and single modules with a maximum gate charge Q_{GE} < 4 µC (see fig. 6).

The charge necessary to switch the IGBT is mainly depending on the IGBT's chip size, the DC-link voltage and the gate voltage.

This correlation is also shown in the corresponding module datasheet curves.

It should, however, be considered that the SKHI 22B is turned on at + 15 V and turned off at - 7 V. Therefore, the gate voltage will change by 22 V during every switching procedure.

Unfortunately, most datasheets do not indicate negative gate voltages. In order to determine the required charge, the upper leg of the charge curve may be prolonged to + 22 V for determination of approximate charge per switch.

The medium output current of the driver is determined by the switching frequency and the gate charge. For the SKHI 22B the maximum medium output current is $Iout_{AVmax}$ < ± 40 mA.

The maximum switching frequency f_{MAX} may be calculated with the following formula, the maximum value however being 50 kHz due to switching reasons:

$$f_{MAX}(kHz) = \frac{4 \cdot 10^4}{Q_{GE}(nC)}$$

Fig. 6 shows the maximum rating for the output charge per pulse for different gate resistors.

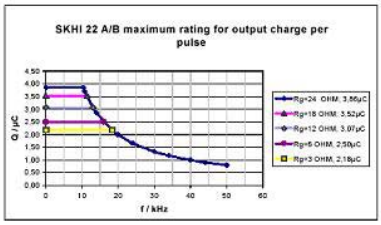

Fig. 6 Maximum rating for output charge per pulse

Further application notes

The CMOS-inputs of the hybrid driver are extremely sensitive to over-voltage. Voltages higher than V_S + 0,3 V or below – 0,3 V may destroy these inputs. Therefore, control signal over-voltages exceeding the above values have to be avoided.

Please provide for static discharge protection during handling. As long as the hybrid driver is not completely

assembled, the input terminals have to be short-circuited. Persons working with CMOS-devices have to wear a grounded bracelet. Any synthetic floor coverings must not be statically chargeable. Even during transportation the input terminals have to be short-circuited using, for example, conductive rubber. Worktables have to be grounded. The same safety requirements apply to MOSFET- and IGBT-modules!

The connecting leads between hybrid driver and the power module should be as short as possible, the driver leads should be twisted.

Any parasitic inductances within the DC-link have to be minimized. Over-voltages may be absorbed by C- or RCD-snubbers between the main terminals for PLUS and MINUS of the power module.

When first operating a newly developed circuit, SEMIKRON recommends to apply low collector voltage and load current in the beginning and to increase these values gradually, observing the turn-off behaviour of the free-wheeling diode and the turn-off voltage spikes generated accross the IGBT. An oscillographic control will be necessary. In addition to that the case temperature of the module has to be monitored. When the circuit works correctly under rated operation conditions, short-circuit testing may be done, starting again with low collector voltage.

It is important to feed any errors back to the control circuit and to switch off the device immediately in such events. Repeated turn-on of the IGBT into a short circuit with a high frequency may destroy the device.

Mechanical fixing on PCB:

In applications with mechanical vibrations (vehicles)[2] do not use a ty-rap for fixing the driver, but - after soldering and testing - apply special glue. Recommended types: CIBA GEIGY XP 5090 + 5091; PACTAN 5011; WACKER A33 (ivory) or N199 (transparent), applied around the case edge (forms a concave mould). The housing may not be pressed on the PCB; do not twist the PCB with the driver soldered on, otherwise the internal ceramics may crack. The driver is not suitable for big PCBs.

SEMIKRON offers a printed circuit board (PCB) type SKPC2006 compatible for mounting a SKHI 21A or SKHI 22A. This PCB contains the necessary tracks to connect the external capacitors C_{CE} and resistors R_{CE}, R_{on}, R_{off} (see fig. 1).

The PCB may directly be plugged to SEMITRANS 3-IGBT modules and be fixed to the heatsink by 3 thread bolts.

Dimensions: L x W x H = 96 x 67 x 1,5 mm.

For further details please contact SEMIKRON.

2. tested acceleration (x; y; z-axis):10-100 Hz: 1,5 g; shock: 5 g (TÜV according to LES-DB-BN 411002)

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C. METGLAS 2705M CORE TRANSFORMER [17]

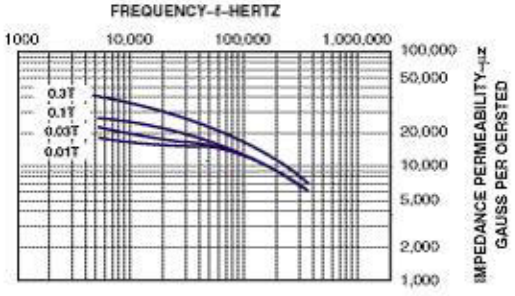
METGLAS® Solutions

[redacted]

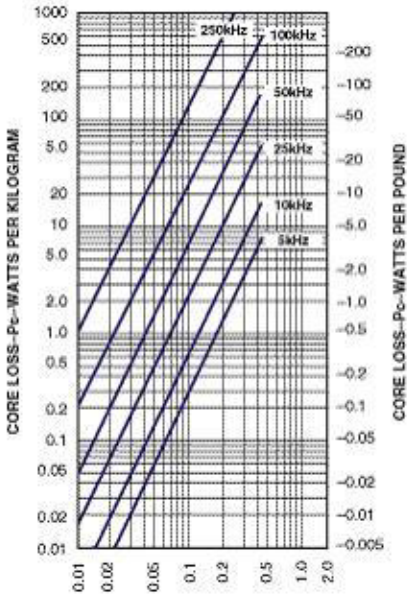
Magnetic Materials

METGLAS® Magnetic Alloy 2705M (Cobalt-based)

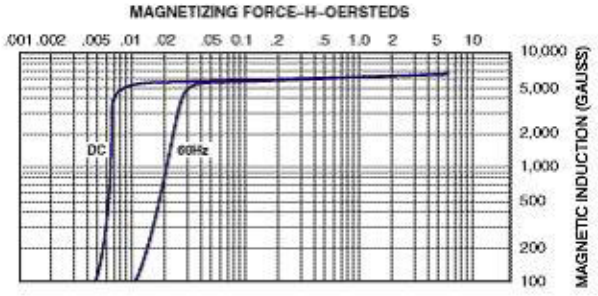
Typical Impedance Permeability Curves
METGLAS® Alloy 2705M
Longitudinal Field Anneal



Typical Core Loss Curves
METGLAS® Alloy 2705M
No-Field Anneal



Typical Initial Magnetization Curves
METGLAS® Alloy 2705M As-cast



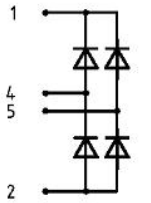
D. BRIDGE RECTIFIER [18]

IXYS Advanced Technical Information

Fast Single Phase Rectifier Bridge
in ISOPLUS i4-PAC™

FBE 22-06N1

V_{RRM} = 600 V
$I_{D(AV)M}$ = 20 A
t_{rr} = 80 ns



Input Rectifier Bridge

Symbol	Conditions	Maximum Ratings	
V_{RRM}		600	V
I_{FAV}	T_C = 90°C; sine 180° (per diode)	10	A
$I_{D(AV)M}$	T_C = 90°C	20	A
I_{FSM}	T_{VJ} = 25°C; t = 10 ms; sine 50 Hz	40	A
E_{AS}	I_{AS}= 0.9 A; L_{AS}=180 µH; T_C = 25°C; non repetitive	0.1	mJ
P_{tot}	T_C = 25°C (per diode)	35	W

Symbol	Conditions (T_{VJ} = 25°C, unless otherwise specified)	min.	typ.	max.	
V_F	I_F = 15 A; T_{VJ} = 25°C		2.0	2.2	V
	T_{VJ} = 125°C		1.5		V
I_R	V_R = V_{RRM}; T_{VJ} = 25°C			0.06	mA
	T_{VJ} = 125°C		0.1		mA
I_{RM}	I_F = 10 A; di_F/dt = -400 A/µs; T_{VJ} = 125°C		11		A
t_{rr}	V_R = 300 V		80		ns
R_{thJC}	(per diode)			3.5	K/W

Data according to IEC 60747 and refer to a single diode unless otherwise stated.

Features

- HiPerFREDTM Epitaxial Diodes
  - fast and soft reverse recovery – low switching losses
  - avalanche rated
  - low leakage current
- ISOPLUS i4-PACTM package
  - isolated back surface
  - enlarged creepage towards heatsink
  - application friendly pinout
  - high reliability
  - industry standard outline

Applications

- high frequency rectifiers, output rectifiers of switched mode power supplies
- single phase mains rectifiers with minimized electromagnetic emissions
- power factor correction in conjunction with boost chopper (FID.../FMD... type)

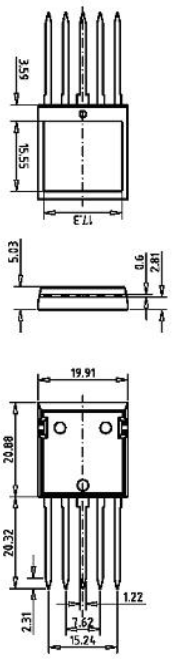
IXYS reserves the right to change limits, test conditions and dimensions.

Component

Symbol	Conditions	Maximum Ratings	
T_{VJ}		-55...+150	°C
T_{stg}		-55...+125	°C
V_{ISOL}	$I_{ISOL} \leq 1$ mA; 50/60 Hz	2500	V~
F_C	mounting force with clip	20...120	N

Symbol	Conditions	Characteristic Values min.	typ.	max.	
d_S, d_A	pin - pin	1.7			mm
d_S, d_A	pin - backside metal	5.5			mm
R_{thCH}	with heatsink compound		0.15		K/W
Weight			9		g

Dimensions in mm (1 mm = 0.0394")



E. INDUCTOR [19]

BOURNS®

Features

- Available in E12 series
- Low height of only 2.7 mm
- High Isat of 3.2 Amps

Applications

- Input/output of DC/DC converters
- Power supplies for:
  - Portable communication equipment
  - Camcorders
  - LCD TVs
  - Car radios

SDR0703 Series - SMD Power Inductors

Electrical Specifications

Bourns Part No.	Inductance 100 kHz		Q Ref.	Test Frequency (MHz)	SRF Min. (MHz)	RDC (Ω)	I rms Max. (A)	I sat Typ. (A)
	(µH)	Tol. %						
SDR0703-1R0M	1.0	± 20	25	7.96	160.0	0.042	2.20	3.20
SDR0703-1R2M	1.2	± 20	25	7.96	145.0	0.047	2.00	3.00
SDR0703-1R8M	1.8	± 20	25	7.96	105.0	0.052	1.90	2.70
SDR0703-2R2M	2.2	± 20	24	7.96	95.0	0.060	1.80	2.60
SDR0703-2R7M	2.7	± 20	23	7.96	80.0	0.065	1.70	2.50
SDR0703-3R3M	3.3	± 20	23	7.96	65.0	0.075	1.65	2.35
SDR0703-3R9M	3.9	± 20	22	7.96	70.0	0.080	1.58	2.25
SDR0703-4R7M	4.7	± 20	20	7.96	60.0	0.100	1.50	2.10
SDR0703-5R6M	5.6	± 20	20	7.96	56.0	0.105	1.40	2.00
SDR0703-6R8M	6.8	± 20	20	7.96	45.0	0.115	1.30	1.90
SDR0703-8R2M	8.2	± 20	20	7.96	40.0	0.150	1.10	1.50
SDR0703-100K	10	± 10	23	2.52	36.0	0.170	1.00	1.40
SDR0703-120K	12	± 10	20	2.52	36.0	0.180	0.90	1.30
SDR0703-150K	15	± 10	23	2.52	30.0	0.240	0.75	1.12
SDR0703-180K	18	± 10	20	2.52	30.0	0.280	0.70	1.05
SDR0703-220K	22	± 10	20	2.52	26.0	0.300	0.65	0.95
SDR0703-270K	27	± 10	20	2.52	20.0	0.400	0.60	0.88
SDR0703-330K	33	± 10	17	2.52	20.0	0.450	0.56	0.82
SDR0703-390K	39	± 10	18	2.52	18.0	0.550	0.50	0.73
SDR0703-470K	47	± 10	20	2.52	15.0	0.720	0.40	0.64
SDR0703-560K	56	± 10	20	2.52	13.0	0.800	0.39	0.60
SDR0703-680K	68	± 10	18	2.52	13.0	0.900	0.38	0.56
SDR0703-820K	82	± 10	18	2.52	12.0	1.18	0.33	0.47
SDR0703-101K	100	± 10	33	0.796	11.0	1.56	0.27	0.40
SDR0703-121K	120	± 10	32	0.796	10.0	1.75	0.26	0.37
SDR0703-151K	150	± 10	30	0.796	9.0	2.00	0.25	0.34
SDR0703-181K	180	± 10	33	0.796	7.0	2.70	0.19	0.30
SDR0703-221K	220	± 10	31	0.796	7.0	3.00	0.18	0.28
SDR0703-271K	270	± 10	30	0.796	7.0	3.60	0.17	0.22
SDR0703-331K	330	± 10	33	0.796	6.0	4.80	0.16	0.19
SDR0703-391K	390	± 10	36	0.796	5.5	6.20	0.14	0.18
SDR0703-471K	470	± 10	33	0.796	5.0	7.00	0.13	0.16
SDR0703-561K	560	± 10	36	0.796	4.2	9.20	0.11	0.15
SDR0703-681K	680	± 10	32	0.796	4.0	10.50	0.10	0.15
SDR0703-821K	820	± 10	32	0.796	3.6	12.00	0.09	0.14
SDR0703-102K	1000	± 10	30	0.252	3.2	14.20	0.08	0.13

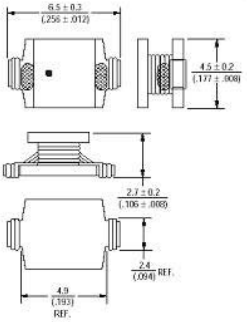
General Specifications

Test Voltage.....0.1 V
Reflow Soldering ...230 °C, 10 sec. max.
Operating Temperature...-40 °C to +125 °C
(Temperature rise included)
Storage Temperature...-40 °C to +125 °C
Resistance to Soldering Heat
.....260 °C for 5 sec.

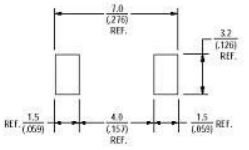
Materials

Core .....Ferrite
Wire .....Enamelled copper 130 °C
Base.....LCP
Adhesive 6020H-6
Terminal .....Cu & Sn/Pb
Rated Current
.....Ind. drop 10 % typ. at Isat
Temperature Rise .....20 °C max.
at rated Irms
Packaging .....500 pcs. per reel

Product Dimensions



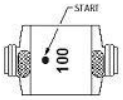
Recommended Layout



DIMENSIONS: MM / (INCHES)

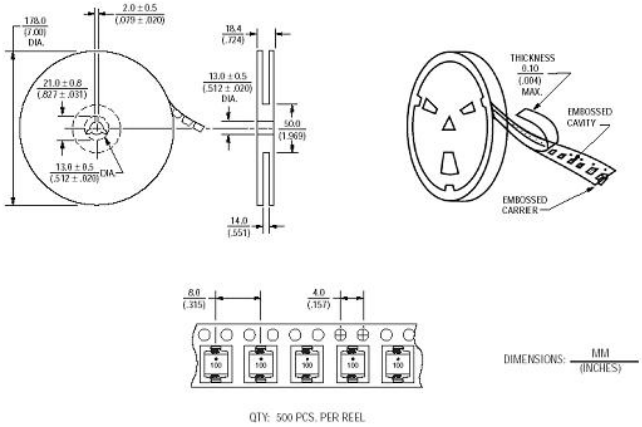
Electrical Schematic

Typical Part Marking



Specifications are subject to change without notice.

Packaging Specifications



QTY: 500 PCS. PER REEL

REV. C, 12/02
Specifications are subject to change without notice.

APPENDIX B. MATLAB CODE

The Matlab code contained in Appendix B provides the Bode plots, step response plots, and the frequency response of the FBC with the controller and without the controller. The code can be used to verify the proper operation of the FBC under various loads simply by changing the value of the resistance.

A. DC-DC ISOLATION CONVERTER

1. MATLAB M-File (thesis.m)

```
%*****************************************************************
% thesis.m
%
% This program simulates the operation of the DC-DC isolation
% converter described in Chapter IV
%
% Written by; Jason A. Zengel 3-13-2003
% Last mod: 4-2-2003
%*****************************************************************

close all;
clear all;

%*****************************************************************
%System constants
%*****************************************************************

E = 500;
R = 37.5;
Vc = 300;
D = .6;
L = .75e-3;
C = 100e-6;


%*****************************************************************
% Closed-loop system with full load
%*****************************************************************
```

```
G_closed = tf([E],[L*C L/R E])
rlocus(G_closed);
title('Root Locus of Closed-Loop, Uncontrolled System');
figure;
step(G_closed);
title('Step Response for Closed-Loop, Uncontrolled System');
figure;
bode(G_closed);
title('Bode Plot for Closed-Loop, Uncontrolled System');

%************************************************************
% Closed-loop system with minimum load
%************************************************************

R = 112.5;
G_closed = tf([E],[L*C L/R E])
figure;
rlocus(G_closed);
title('Root Locus of Closed-Loop, Uncontrolled System');
figure;
step(G_closed);
title('Step Response for Closed-Loop, Uncontrolled System');
figure;
bode(G_closed);
title('Bode Plot for Closed-Loop, Uncontrolled System');

%************************************************************
% closed-loop controlled DC DC Isolation Converter minimum load
%************************************************************

hv = .02;
hi = .02;
hn = 25;

G_closed_controlled = tf([hv*(E/(L*C)) hn*(E/(L*C))],[1
(1/(R*C)+(E*hi)/L) (1/(L*C)+(E*hv)/(L*C)) (E*hn)/(L*C)])
figure;
rlocus(G_closed_controlled);
title('Root Locus of Closed-Loop, Controlled System');
figure;
step(G_closed_controlled);
title('Step Response for Closed-Loop, Controlled System');
figure;
bode(G_closed_controlled);
title('Bode Plot for Closed-Loop, Controlled System');
```

```
%************************************************************
% closed-loop controlled DC DC Isolation Converter full loading
%************************************************************

R = 37.5;
hv = .02;
hi = .02;
hn = 25;

G_closed_controlled = tf([hv*(E/(L*C)) hn*(E/(L*C))],[1 (1/(R*C)
+(E*hi)/L) (1/(L*C)+(E*hv)/(L*C)) (E*hn)/(L*C)])
figure;
rlocus(G_closed_controlled);
title('Root Locus of Closed-Loop, Controlled System');
figure;
step(G_closed_controlled);
title('Step Response for Closed-Loop, Controlled System');
figure;
bode(G_closed_controlled);
title('Bode Plot for Closed-Loop, Controlled System');
```

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APPENDIX C. PARTS LIST

Appendix C contains a part list of components needed to construct the FBC detailed in this thesis. The part list contains a part description, the manufacturer of the part, the quantity needed of the part, and the cost.

A. DC-DC ISOLATION CONVERTER PARTS AND COST

Part Description	Manufacturer	Quantity	Cost	Reference (if applicable)
IGBT - SK45GH063	Semikron	1	$323.50	
Hybrid Dual IGBT Driver Board - SKHI22 A/B	Semikron	1	$65.55	
Rack Mounted Chasis	Newark	1	$92.26	[1]
Low Power AC-DC Switches 92F5324	Newark	1	$50.00	[1]
Capacitor - C0G7565	Novacap	10	$215.40	
Isolation Amplifier – (AD-215) 630-8042	Allied Electronics Inc.	2	$99.81	[1]
18-Pin PWM Chip – 296-2508-5-ND	Digikey	1	$5.28	[1]
Resistors	Various	About 45	About $63	
Op-Amps	Various	6	About $16	
Diodes	Various	4	About $22	
Transformer- METGLAS 2705M Core	Various	1	$118.76	
Bridge Rectifier – FBE 22-06N1	IXYS	1	$86.55	
Wiring	Various	Varies	$85.60	
Current Sensor – CLN - 50	Allied Electronics Inc.	2	$28.00	
Inductor – SDR0703 - 1ROM	Bourns	1	$175.50	

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