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13. ABSTRACT ***(Maximum 200 Words)***

This program developed inertial-grade micromachined accelerometers and gyroscopes and their associated electronics and packaging for a variety of military and commercial applications. In-plane, out-of-plane and monolithic 3-axis accelerometers have been developed with their interface electronics. Analysis, simulation, fabrication, and testing techniques for these accelerometer systems have been developed. Different types of accelerometers were tested with the interface electronics. 1.08 micro-g open-loop and 10 micro-g closed-loop resolutions were achieved with out-of-plane accelerometers. For in-plane accelerometers open-loop resolutions are 80 micro-g and 1.6 micro-g for SOG and all-silicon devices, respectively. Single-chip, three-axis accelerometers are consistent with the out-of-plane and all silicon in-plane accelerometers.

Polysilicon ring gyroscopes utilizing high aspect ratio combined poly and single crystal silicon (HARPS S) technology were developed. This technology provides tall structure (-80 micron) and large sense/drive gaps, which are essential to achieve high performance gyroscopes. The gyroscopes were tested with readout electronics, control circuitry, and quadrature control loop, and achieve a quality factor of 1,200 and 2deg/sec in 10Hz BW. A single crystal silicon gyroscope was developed in order to obtain small parasitics, large quality factor, and large structural mass. This device has 15 micron thick single crystal silicon on a glass substrate, large (10 micron) sense/drive gap. The single crystal silicon gyroscope achieves a quality factor of 12,000, good linearity (0.02%), large sensitivity (132 mV/deg/sec), and low output noise (10.4 deg/hr/Hz).

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Abstract

This program focuses on developing inertial-grade micromachined accelerometers and gyroscopes and their associated electronics and packaging for use in a variety of military and commercial applications.

During the project timeline in-plane, out-of-plane and monolithic 3-axis accelerometers have been developed with their interface electronics. Analysis, simulation, fabrication, and testing techniques for these accelerometer systems have been developed. All different types of accelerometers have been tested with the interface electronics. 1.08μg open-loop and 10μg closed-loop resolution have been achieved with out-of-plane accelerometers. For in-plane accelerometers open-loop resolutions are 80μg and 1.6μg for SOG and all-silicon devices, respectively. Single-chip, three-axis accelerometers are consistent with the out-of-plane and all-silicon in-plane accelerometers.

Polysilicon ring gyroscopes utilizing high aspect ratio combined poly and single crystal silicon (HARPSS) technology has been developed. This technology provides tall structure (~80μm) and large sense/drive gaps, which are essential to achieve high performance gyroscopes. The gyroscopes are tested with readout electronics, control circuitry, and quadrature control loop, and achieve a quality factor of 1,200 and 2°/sec in 10Hz BW. A single crystal silicon gyroscope has been developed in order to obtain small parasitics, large quality factor, and large structural mass. This device has 150μm thick single crystal silicon on a glass substrate, large (10μm) sense/drive gap. The single crystal silicon gyroscope achieves a quality factor of 12,000, good linearity (0.02%), large sensitivity (132 mV/°/sec), and low output noise (10.4 °/hr/√Hz).

Summary

This program focuses on developing inertial-grade micromachined accelerometers and gyroscopes and their associated electronics and packaging for use in a variety of military and commercial applications. Most micromachined inertial sensors available today are far from being suitable for navigation, guidance, seismic and microgravity measurements. It is indeed critical to reduce the size, cost, and weight of inertial instruments without compromising their overall performance. Under this project we have developed truly inertial-grade accelerometers and gyroscopes for use in navigation, guidance, seismic / microgravity measurements, and high performance commercial applications. During the project timeline:

1. *Out-of-plane* accelerometer which has a full wafer thick proof-mass, polysilicon electrodes on both sides of the wafer, controllable damping, and small air gap has been developed. This accelerometer utilizes a combined surface and bulk micromachining technology to obtain high sensitivity, low noise, and low/controllable damping which are key factors essential in achieving micro-g and sub-micro-g resolution. In order to mitigate residual stress of long polysilicon electrodes, in-situ and Rapid Thermal Annealing (RTA) have been performed and demonstrated stress-free electrodes successfully, which results in high yield manufacturing process.

2. Three different types of *in-plane* accelerometers have been developed: A Silicon-On-Glass (SOG) accelerometer, an all-silicon accelerometer, and a sub-micrometer gap accelerometer. The SOG device utilizes Deep Reactive Ion Etching (DRIE) and wafer bonding technologies to build thick (~120μm) proof-mass with a narrow sensing gap. This device can be monolithically integrated with CMOS readout circuits. The all-silicon accelerometer implements a well-characterized combined surface and bulk micromachining technology to obtain a wafer thick (~475μm) proof-mass and very narrow sensing gap (~1.1μm), which provide high sensitivity and low noise characteristics comparable with high performance *out-of-plane* devices. The sub-micron gap accelerometer uses an electron beam lithography and DRIE to achieve 0.2μm sensing gap. Unlike conventional accelerometers, this device utilizes comb drive sense/drive electrode configuration to achieve large dynamic range and low noise floor by taking advantage of the sub-micron sensing gap.

3. A monolithic three-axis accelerometer using two *in-plane* and one *out-of-plane* accelerometers has been developed. The accelerometer is small size, self-aligned, and easy to package. All three devices have full-wafer thick silicon proof-mass, large area polysilicon sense/drive electrodes, and small sensing gap (<1.5μm). The accelerometer has > 5pF/g measured sensitivity and sub-micro-g/√Hz mechanical noise floor for all three axes.

4. A low-offset, low noise interface electronics operating as a 2nd-order electromechanical sigma-delta converter has been implemented. This chip operates the accelerometer in closed-loop mode which results in higher dynamic range, linearity and bandwidth. A fully differential switched-capacitor type front-end circuit has been utilized in this chip due to its parasitic insensitive operation.

5. Simulations to help identify the limits provide guidelines and verify performance parameters have been performed. Modeling and simulation of the closed-loop accelerometer includes the electrode movement in addition to all other non-linearities and non-idealities. The system is modeled and simulated in the time domain using SIMULINK. Besides this, noise components of the system identified in detail. Noise analysis has showed that as the Brownian noise of the device decreases to sub-μg range, the electronics becomes dominant in the overall noise performance. The electrical noise sources have been identified through the noise analysis and second-generation interface electronics has been implemented with a better noise performance.

6. A novel readout circuit, the multi-step electromechanical sigma-delta modulator architecture, has been introduced and implemented. This technique is based on using a two-element multi-step sensor array similar to a multi-step data converter. Basically the first element does coarse measurement, its output is deducted from the input of the second element and the second element performs a fine measurement on the smaller differential input. Multi-step architecture provides high signal-to-noise ratio (SNR) and improves the dynamic range. The fabricated chip was tested individually and the open-loop operation with *out-of-plane* accelerometer was verified.

7. All different types of accelerometers have been tested with the interface electronics. 1.08μg open-loop and 10μg closed-loop resolution have been achieved with *out-of-plane* accelerometers. For *in-plane* accelerometers open-loop resolutions are 80μg and 1.6μg for SOG and all-silicon devices, respectively. Single-chip, three-axis accelerometers are consistent with the *out-of-plane* and all-silicon *in-plane* accelerometers.

8. Polysilicon ring gyroscopes utilizing High Aspect Ratio combined Poly and Single crystal Silicon (HARPSS) have been developed. This technology provides tall structure (~80μm) and large sense/drive gaps between the ring and sense/drive electrodes, which are essential to achieve a high performance micromachined gyroscope. In order to increase quality factor, which is necessary to achieve high sensitivity, anchors have been improved and the quality factor has been increased by more than a factor of 4. Monolithic integration with readout circuits using U of M Enhancement/Depletion NMOS process has been also performed.

9. In order to achieve a high performance gyroscope by reducing the parasitics, increasing quality factor, and mass of the structure, single crystal silicon gyroscope has been developed. This device has 150μm tall structure, large (10μm) sense/drive gap by using <111> oriented single crystal silicon. Meander support spring design has been

implemented in stead of half-circle support to minimize imperfect fabrication effects on splitting two flexural modes, which results in better mode matching and facilitating electronic tuning. The single crystal gyroscope provides the quality factor of 33,000 in vacuum environment (1 mTorr).

10. A polysilicon gyroscope is tested by using simple source follower readout circuits, control circuitry to lock the resonant frequency of a gyroscope, and quadrature control loop to null out the zero rate output. With quality factor of 1,200, drive amplitude of 0.15μm, and sense node parasitic capacitance of 2pF, the resolution is measured to be 2°/sec in 10Hz BW. A single crystal silicon gyroscope provides high Q (12,000), good linearity (0.02%), large sensitivity (132 mV/°/sec), and low output noise (10.4 °/hr/√Hz).

Introduction

Precision inertial instruments are at the heart of many present day military and navigational systems. The most important of these involve the use of inertial instruments for navigation and guidance of a series of systems ranging from rockets and missiles to personal navigation systems for soldiers in the field. For all of these applications, performance levels of at least micro-g for an accelerometer, and degree-per-hour for a gyroscope is desirable. The attractive features of MEMS as applied to inertial measurement systems are its potentially low cost, drastically reduced size and weight, and low power dissipation, all of which are prerequisites for the development of next generation military systems. Although much work has been done on trying to develop microaccelerometers with micro-g accuracy, and micro-gyroscopes with better than 10 degree-per-hour performance, miniature devices that are capable of delivering such performance are still only a goal.

The overall objective of this project is to develop micro-g and nano-g accelerometers as well as degree-per-hour micro-gyroscopes. This requires the development of packaging and assembly for the sensors and all of the associated control and signal processing electronics, as well as detailed characterization, calibration, and testing of the instrument module to understand the performance limits. The fabrication process and device structure of our accelerometers addresses many of the problems with previous efforts aimed at μg accelerometer development. This technology uniquely enables fabrication of 3-axis sensitive devices with very low noise floor (by using large proof-mass and controlling the damping) and large sensitivity (by using large proof-mass, small air-gap over large area) - all on a single silicon wafer. These devices potentially could provide very low-temperature sensitivity and good long-term stability.

Our efforts in the interface circuit development are focused on achieving high sensitivity, low-noise, low-drift and good long-term stability. Design and development of ultra-low noise and extremely low-drift and highly stable interface circuitry forms another part of this task; which aims at reducing the electronic noise of the system and its contribution to the overall drift and performance stability. Reaching extremely low noise performance, resulting in atto-farad resolution in several 100Hz bandwidths with a low temperature sensitivity and low-drift will require novel circuit techniques.

Another objective of this project is to develop new silicon-micromachining fabrication technologies, low-power precision interface circuits, and vacuum packaging techniques to achieve degree-per-hour inertial micro-gyroscopes. A single-wafer, all-silicon, high aspect-ratio p++/polysilicon trench-refill technology has been developed to implement vibrating ring structures that provide features required for achieving “tactical-grade” level of performance. The trench-refill process utilizes polysilicon as the structural element with its superior and homogenous material properties and is capable of producing very thick vertical polysilicon structures through deposition of only 1-2 μm LPCVD polysilicon layers. In order to further improve the resolution and achieve inertial-grade performance, very thick ring and sense

electrode structures with very small capacitive gaps are required to produce a large sense capacitance between the ring and the output electrodes. These can be all accomplished using a high aspect-ratio, polysilicon surface-micromachining fabrication technology. Polysilicon structures with thickness in the hundreds of microns will be fabricated using deep RIE techniques. Also, these devices should operate in vacuum to achieve high mechanical quality factor and low-noise parasitic-insensitive integrated electronics are needed to resolve very small (atto-Farad) capacitance changes of the device. High-performance parasitic-insensitive interface circuits for measuring very small capacitive changes of the sensor will be designed and developed. We will also develop chip-level vacuum packaging techniques for the gyroscope structure to achieve high mechanical quality factor.

A. Micromachined Accelerometers

1. Methods, Assumptions and Procedures

In this project we have developed *in-plane*, *out-of-plane* and 3-Axis accelerometers. The following sections describe the device structures, fabrication process, and interface electronics for readout.

1.1. Out-of-plane (Vertical, Z-Axis) Micromachined Accelerometers

1.1.1. Motivation

Previous efforts to make high performance microaccelerometers have included capacitive [1-3], resonant [4, 5], and tunneling sensors [6, 7]. The main advantage of the resonant sensors is their direct digital output. However, these devices typically have small bandwidths that are limited by the output readout. Tunneling accelerometers use a constant tunneling current between a tunneling tip and its counter electrode to sense the proof-mass displacement. These accelerometers can achieve very high sensitivity since the tunneling current is highly sensitive to displacement. However, these devices have large drift and noise levels at low frequencies. Due to the small allowable displacement at the tip, these types of sensors require a very stiff feedback loop, reducing the useful bandwidth and dynamic range.

Capacitive accelerometers have become very attractive and promising for high-precision μg resolution accelerometers, due to their high sensitivity, dc response, low noise, and simple structure. The open-loop sensitivity of a capacitive accelerometer is proportional to the proof-mass size and capacitance overlap area, and is inversely proportional to the spring constant and air gap squared. Therefore a large proof-mass, narrow gap and high Q (low damping) are helpful for achieving low noise floor. The large proof-mass can be formed by the LIGA process and electroplating or by using the whole silicon wafer thickness and bulk micromachining. The LIGA process is not easily accessible and the structures are very sensitive to temperature. The majority of silicon μg accelerometers achieve high resolution by using a thick and large proof-mass. These devices use silicon-glass anodic bonding [1, 2] or silicon-silicon fusion bonding [3] as part of their fabrication process. Since one of the requirements is low damping, it is hard to form damping holes in these approaches. Therefore, these devices have to be packaged in a controlled environment.

Our proposed approach relies on a single-wafer all-silicon capacitive accelerometer. The microaccelerometer has an all-silicon fully-symmetric structure. It employs a combined surface and bulk micromachining fabrication process to obtain a large proof-mass, controllable/small damping, and a small air gap for large capacitance variation - all on a single silicon wafer.

Hence the microaccelerometer has high sensitivity, low noise floor, and low/controllable damping which are the key factors for attaining μg and sub-μg resolution in capacitive accelerometers.

1.1.2. Structure

This section summarizes the device structure briefly. Figure 1 shows the microaccelerometer structure. The device uses the whole wafer thickness to attain a large proof-mass, utilizes a sacrificial thin film to form a uniform and conformal gap over a large area, and forms sense and actuation electrodes by depositing polysilicon on the wafer. These electrodes, while thin, are made very stiff by embedding thick vertical stiffeners in them so that force rebalancing of the proof-mass becomes possible. The device microfabrication technology utilizes a trench refill technique to form thick stiffeners by depositing thin polysilicon films. Any damping hole configuration and geometry can be easily formed on the polysilicon electrodes to optimize damping coefficient and capacitance. The proof-mass and its supporting rim have the whole wafer thickness and are formed by anisotropic etching of the silicon wafer (bulk micromachining). The electrodes are polysilicon plates created on both sides of the proof-mass and anchored on an isolation dielectric at the frame. The device has low temperature sensitivity as the polysilicon electrodes and silicon frame expansion coefficients match each other closely. Furthermore, the device has a good long-term stability as it is all-silicon and no wafer bonding is used in its fabrication process.

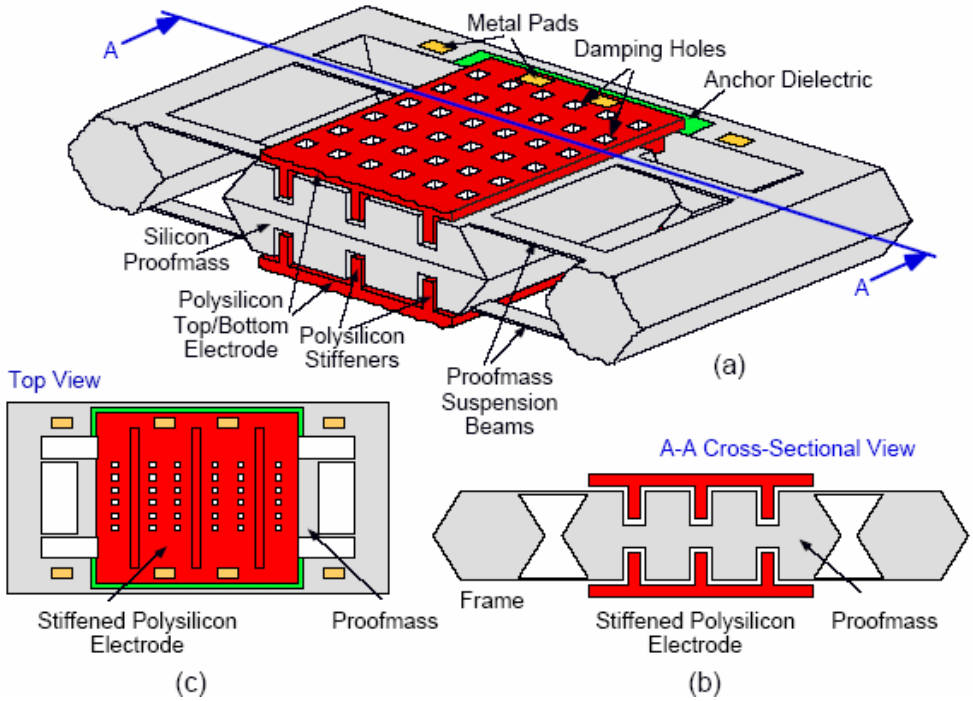


Figure 1: Micro-g accelerometer structure (a) Device structure, (b) A-A cross-sectional view, (c) Top view.

1.1.3. Accelerometer resolution

The accelerometer resolution is determined by its electrical and mechanical noise levels. The electrical signal to noise ratio can be improved by enhancing the sensor and the readout circuit sensitivity, and reducing the circuit electrical noise. The mechanical noise of the accelerometer is caused by the Brownian motion of the gas molecules surrounding the proof-mass and the Brownian motion of the proof-mass suspension or anchors. The Total Noise Equivalent Acceleration (TNEA $(m/\sec^2\sqrt{Hz})$) is shown to be [8]:

$$TNEA = \frac{\sqrt{4K_B TD}}{M} = \sqrt{\frac{4K_B T\omega_r}{QM}} \qquad \text{Equation 1}$$

where K_B is the Boltzmann constant and T is the temperature in K. Equation 1 clearly shows that in order to reduce the mechanical noise, the quality factor and proof-mass need to be increased.

The quality factor can be increased by reducing the damping. The device damping is caused by both structural and viscous damping. However, the structural component is orders of magnitude smaller than the gas viscous damping even at low pressures (a few mTorr), and can be neglected [9].

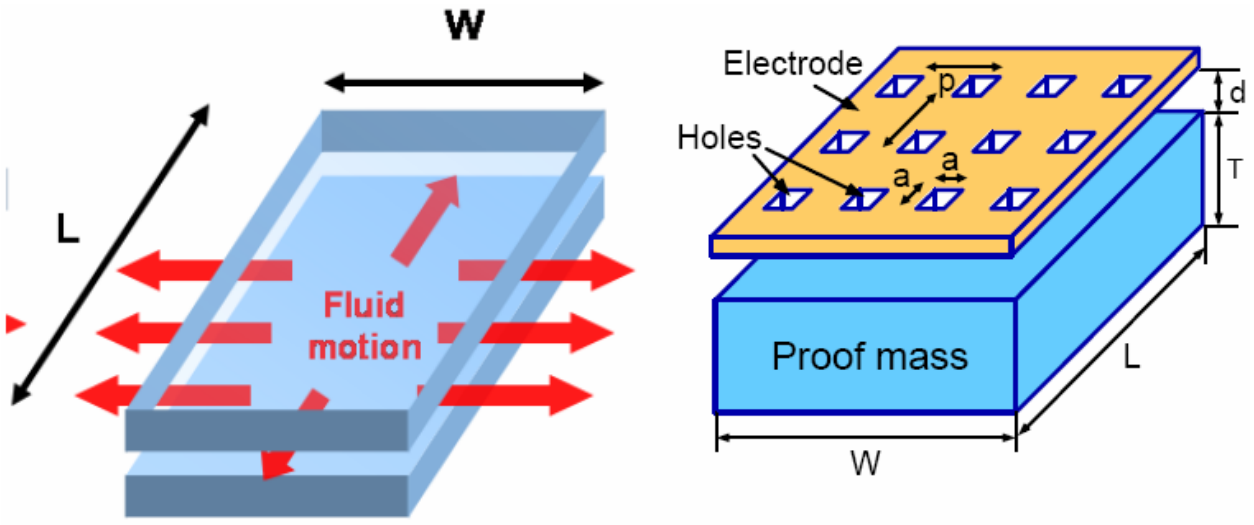
The viscous damping in micromachined devices is categorized into squeeze film damping [10, 11] and couette-flow damping [12]. In vertical accelerometer, the perpendicular motion of the proof-mass with respect to the electrodes results in squeeze film damping as shown in Figure 2. In order to reduce damping, our approach implements incorporating holes in the plates to effectively divide them into a number of smaller plates. In this manner the total damping can be calculated by adding up the damping of the smaller plates, which effectively results in a lower damping with the 4th-order dependence of the damping factor on the plate dimensions (Equation 2). The damping factor of a perforated plate with equally spaced damping holes shown in Figure 2 is expressed by Equation 3:

$$D = c\mu\frac{W^3 L}{d^3} \qquad \text{Equation 2}$$

$$D = 0.427N\mu\frac{L_{eff}^{\ 4}}{d^3}, \qquad L_{eff} = \sqrt{p^2 - a^2} \qquad \text{Equation 3}$$

(a) Damping without perforation (b) Damping with perforation

where W and L are the larger and smaller dimensions of the (smaller) plate, d is the separation, μ is the viscosity of the ambient fluid, c is a form factor depending on the ratio of W/L, N is the number of smaller plates (or the damping holes), and L_{eff} is the effective plate length and is related to the damping hole size (a) and pitch (p).



(a) Parallel plate configuration (b) Perforated electrode configuration

Figure 2: Conventional parallel plate damping configuration and perforated electrode configuration implemented in our approach.

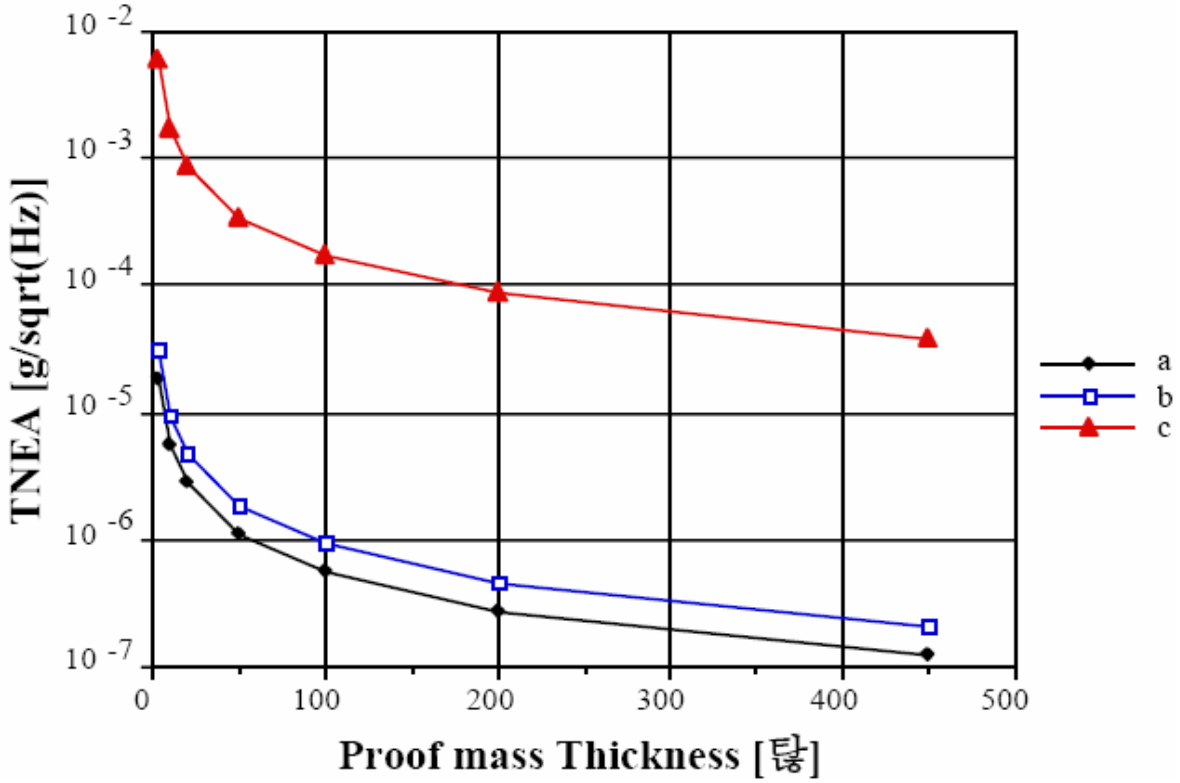


Figure 3: Total Noise Equivalent Acceleration (TNEA) due to Brownian motion at atmospheric pressure for a device with 1x2 mm^2 mass/electrode area and 1.5 µm air gap with (a) 4µm damping holes with 9µm pitch, (b) 5µm damping holes with 15µm pitch, (c) no damping holes.

In order to verify and show the effectiveness of damping holes in reducing the damping factor and lowering the mechanical noise floor, the device TNEA versus the proof-mass thickness at atmospheric pressure for three different cases: (a) 4μm damping holes with 9μm pitch, (b) 5μm damping holes with 15μm pitch, (c) without any damping holes; is plotted in Figure 3. The device has a mass/electrode area of 2mm x 1mm and 1.5μm gap.

As can be observed, sub micro-g noise floor is achievable at atmosphere by using both thick proof-mass and damping holes. Note that by forming the damping holes in the electrode rather than the proof-mass, there is no loss in the mass size. Further, by using small damping holes the fringing capacitance becomes comparable with the lost capacitance due to reduction in surface area, and thus there is almost no loss of sense capacitance either. Table 1 shows design specifications of the *out-of-plane* accelerometer.

Table 1: *Out-of-plane* accelerometer specifications.

Proof-mass size	2mm×1mm×475μm
Mass of the proof-mass	2.2 mg
Sense area	300μm×1000μm×5
Spring constant	88.7 N/m
Stiffness of an electrode	1080 N/m
Resonant frequency	1.05 kHz
Noise floor @ atm.	0.84 μg/√Hz
Base capacitance	41 pF
Max. acceleration	± 1.6 g
Open loop sensitivity	1.25 pF/g

1.1.4. Fabrication

The fabrication process for the double-sided accelerometer is shown in Figure 4. The process requires seven masks and using a double sided polished p-type silicon wafer of <100> orientation. The wafer is first subjected to shallow boron diffusion (3-4μm thick) by using thermal oxide mask. This defines the shape of the proof-mass, the suspension beams, and the supporting rim. Then, 50-60μm deep trenches are formed using deep reactive ion etch (DRIE) for vertical electrode stiffeners. After the DRIE, 1.5μm of LPCVD oxide is deposited which

serves as the sacrificial layer and determines the air-gap. The LPCVD oxide is patterned to form dimples to reduce stiction and limit the travel range against shock. The trenches are then refilled with 2000Å of LPCVD nitride, and 2.5µm of LPCVD polysilicon. The polysilicon is deposited at 580ºC and in-situ annealed at 625ºC for 2hrs, which helps alleviate any compressive stress in the polysilicon film. The polysilicon is doped with boron and patterned to form the electrode plates with damping holes. Next 4000-5000Å of LPCVD (capping) oxide is deposited and patterned to form metal contacts and openings to the bulk silicon for the subsequent etch in Ethylene Diamine Pyrocatecol (EDP). Then Cr/Au is evaporated for contact metal. To minimize the etch time in EDP and also make sure that the etchant undercuts the electrodes, silicon is selectively etched by using DRIE. Finally, the device is etched in EDP, released by removing the sacrificial oxide in HF, and dried in super critical CO_2 environment to avoid stiction.

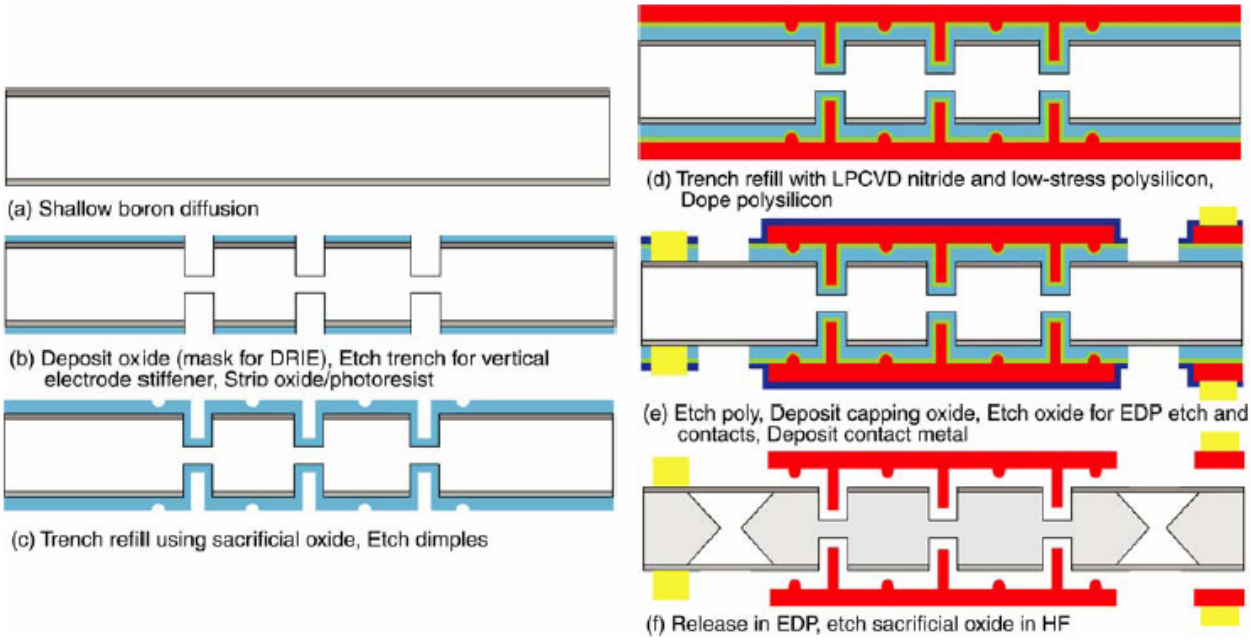
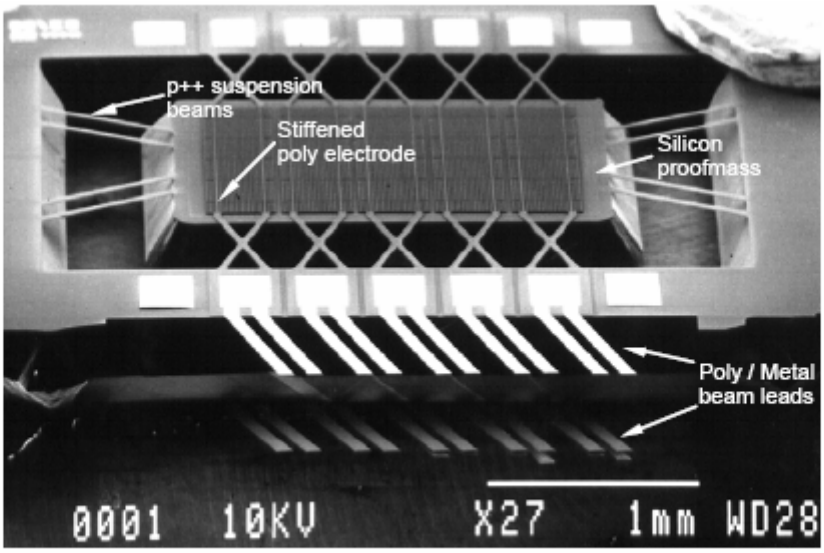
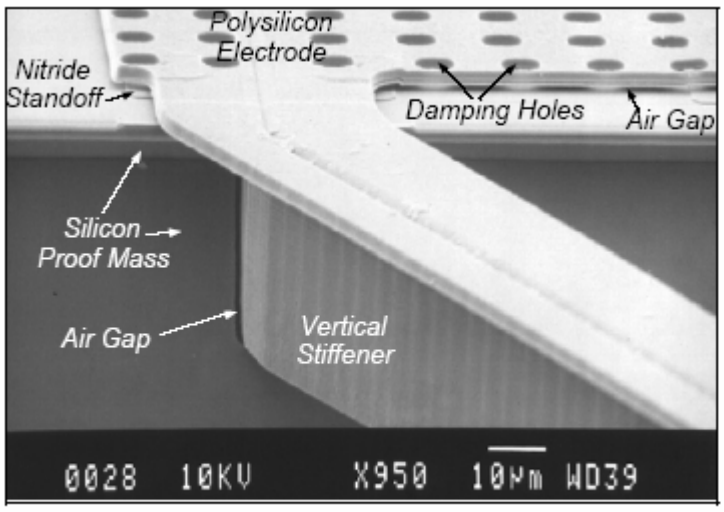


Figure 4: Fabrication process sequence of an *out-of-plane* accelerometer.

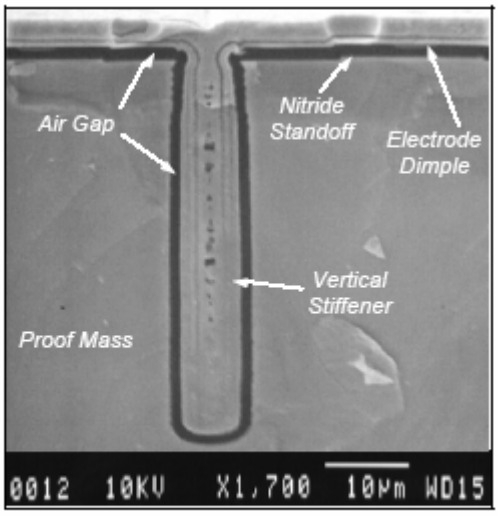
Figure 5 shows a SEM view of the device with 2mm x 1mm proof-mass. The device has five electrically isolated electrodes on each side, which are anchored at the rim using stiffened polysilicon supports. The polysilicon/metal beam leads are on the topside and the bottom side. An enlarged view of a single electrode stiffener support and a close-up view of the cross-section of proof-mass as well as stiffened poly electrode are also shown in Figure 5. The electrode damping holes can be clearly seen in this figure. The electrode dimples reduce the effective contact area of electrode and proof-mass, and hence help with reducing stiction.



(a) SEM view of an accelerometer with 2mm x 1mm proof-mass.



(b) A close-up SEM view of polysilicon electrode, its vertical embedded stiffener, and the proof-mass.



(c) A cross-section of the proof-mass and the stiffened polysilicon electrode.

Figure 5: A fabricated *out-of-plane* accelerometer.

The 2mm long polysilicon electrodes with a very narrow conformal gap provide a high sensitivity accelerometer. However, the residual stress from a polysilicon film causes the long electrodes to buckle even though vertical stiffeners are embedded, resulted in non-linear response and even impeding the free motion of the proof-mass. Thus, stress free polysilicon film is very necessary for our accelerometer.

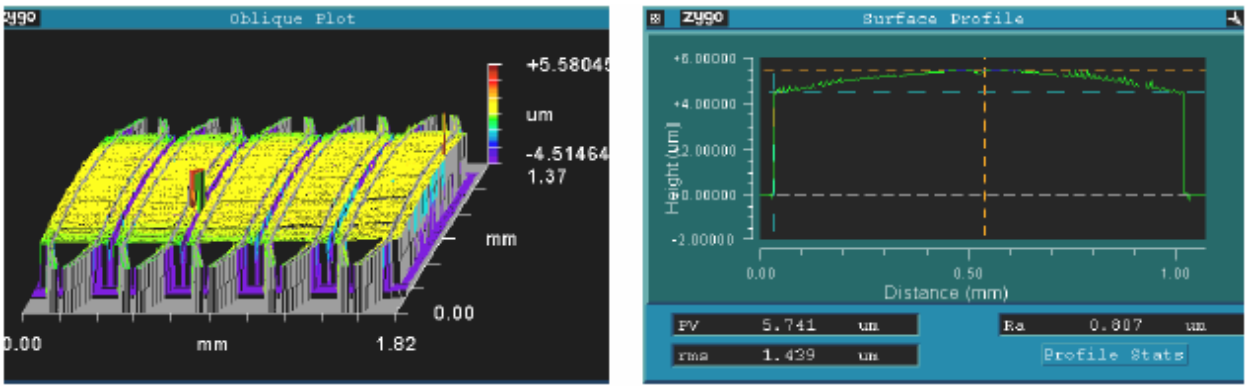


Figure 6: Surface scan along the width of the electrode using an interferometer (ZYGO) shows warped polysilicon electrodes due to stress.

Figure 6 shows surface scans, using the ZYGO, of a device after HF release and super-critical CO_2 drying. The polysilicon electrodes bend (~0.8μm) from its normal position due to compressive stress in the trench-refilled stiffeners.

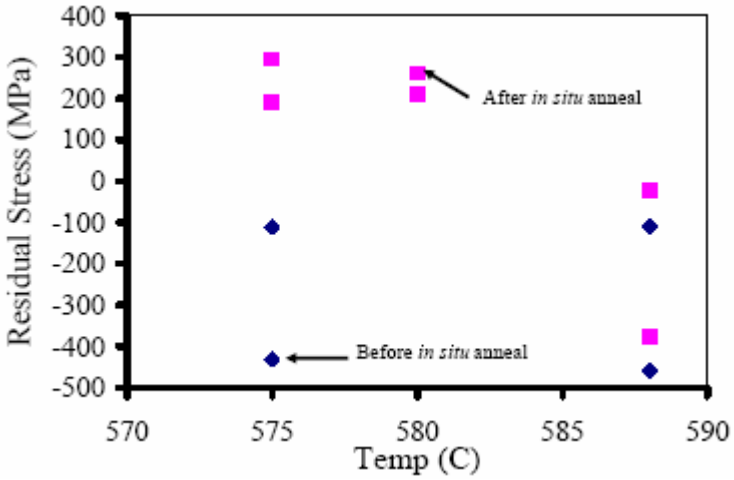


Figure 7: Residual stress of as-deposited polysilicon and in situ annealed polysilicon, deposited at 570°C, 580°C, and 588°C.

In order to form stress free polysilicon electrodes, we have developed two methods; one is in situ annealing. the other is rapid thermal annealing (RTA). Figure 7 shows a plot of residual stress of as-deposited polysilicon and in situ annealed polysilicon, deposited at 570°C, 580°C, and 588°C. The wafers were annealed in situ at 625°C for 2 hours in nitrogen ambient. The un-annealed films were compressive for all deposition temperatures. An in situ anneal had a significant effect on the stress levels, resulting in tensile stress of ~200MPa for the polysilicon films deposited at 570°C, and 580°C. The in situ had no effect on the polysilicon film deposited at 588°C. This is believed that the transition from amorphous to polysilicon (crystallization) in fine-grained polysilicon occurs at the amorphous-silicon dioxide interface layer during the annealing cycle and cause the stress in the amorphous layer to change towards tensile.

Figure 8 shows a plot of residual stress of polysilicon deposited at 580°C and in situ annealed at 625°C for 2 hours and the effect of the subsequent steps on the stress. The stress of the in situ annealed polysilicon after boron doping is +76MPa (tensile) and the stress of the in situ annealed undoped polysilicon after being exposed to the boron doping conditions is -70MPa (compressive). The stresses almost cancel each other. To reduce the variations in the stress due to position of the wafer in furnace, the wafers are annealed in a RTA at 1100°C for 2 minutes. Figure 9 shows a surface map obtained by ZYGO.

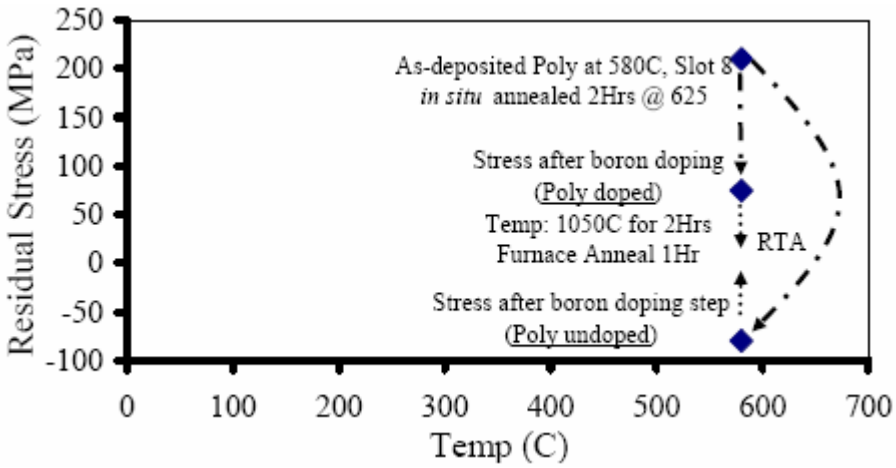


Figure 8: The residual stress of in situ annealed polysilicon and the effect of subsequent steps on the stress.

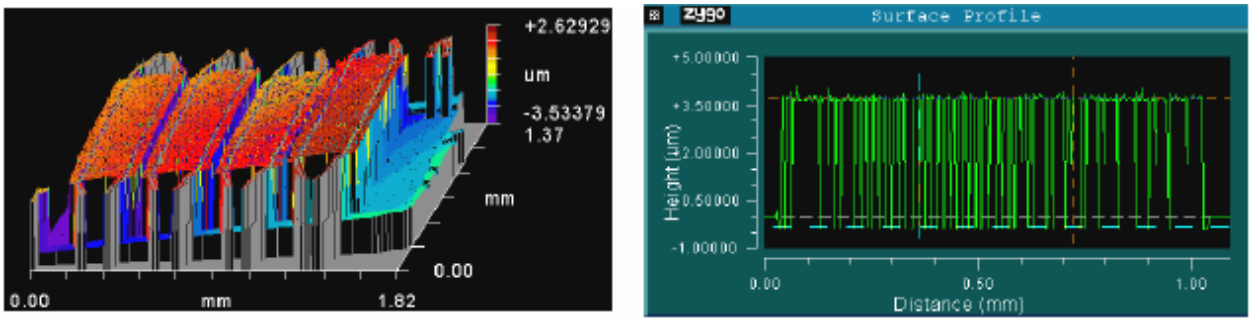


Figure 9: Surface scan using the ZYGO for devices after anneal.

1.2. In-plane (Lateral, X-Y Axis) Micromachined Accelerometers

1.2.1 Motivation

Figure 10 shows the noise performance for *in-plane* (x- and y-axis) and *out-of-plane* (z-axis) micromachined accelerometers reported in the literature in the last 20 years. Note that the noise floor in the figure indicates not mechanical noise only, but the total system noise. In this report, noise represents the overall system noise unless it is stated as mechanical or electronic noise.

Most of the reported high performance devices are sensitive to *out-of-plane* (vertical, z-axis) acceleration since it is easier to fabricate large proof-mass and large-area electrodes along the z-axis. These sensors utilize full wafer thickness for their proof-mass, and a small sensing gap [3, 13]. Those characteristics (large proof-mass, large-area electrodes, and a small sensing gap) enables these *out-of-plane* accelerometers to achieve high sensitivity and low noise performance. However, it is not easy to achieve these features for *in-plane* (lateral, x-, y-axis) sensors that are sensitive to acceleration parallel to the sensor substrate because of the difficulty in fabricating high aspect-ratio vertical sense/drive electrodes with small sensing gaps. Although surface micromachined accelerometers can be integrated with interface electronics to improve performance, due to their small mass they typically have a noise floor of 0.03-1mg/√Hz at atmospheric pressure [14-17]. Although vacuum packaging substantially reduces the mechanical noise of a surface micromachined accelerometer and lowers the output noise floor, it is desirable to operate sensors in atmosphere since vacuum packaging is not cost effective [15].

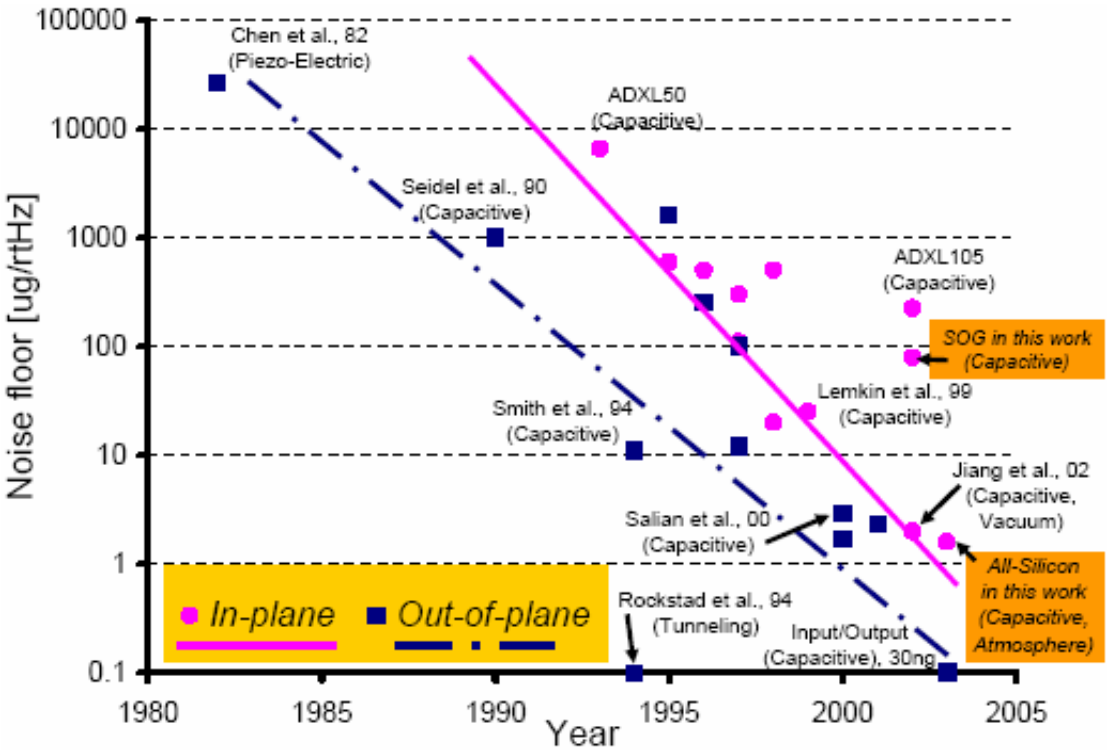


Figure 10: Performance improvements for *In-plane* & *Out-of-plane* micro-accelerometers.

In order to increase the proof-mass size above what is typically achievable using surface micromachining, Silicon-On-Insulator (SOI) or wafer-bonded accelerometers utilizing Deep Reactive Ion Etching (DRIE) technology have been developed [18-21]. These accelerometers utilize a 25-120μm thick single-crystal silicon proof-mass to reduce overall system noise. However, most of these accelerometers either do not provide high enough resolution needed for inertial-grade performance, or have complicated fabrication processes and large parasitics. Table 2 summarizes the characteristics of commercialized or in-development *out-of-plane* and *in-plane* accelerometers.

Table 2: Sensitivity/Noise ratio comparison between *out-of-plane* and *in-plane* accelerometers.

	Out-of-plane [22, 23]	*In-plane*		
		SM* [14, 17, 24]	SOI [18, 20]	BM* [19]
Mass (micro-gram)	> 2000	0.1~1.5	80~100	~80
Sense gap (μm)	< 1.5	1.5~2.3	2.5~3.0	~4
Sense capacitance (pF)	> 20	~0.1	6.2	0.075
Sensitivity (fF/g)	> 5000	0.1~4.5	50~100	0.8
Noise floor (μg/√Hz)	0.03~1.1	32~110	25	330
Sensitivity/Noisefloor	> 4400	0.001~0.14	2~4	0.002

* SM and BM stand for surface and bulk micromachined, respectively.

In order to achieve the high-sensitivity low-noise devices, in this report, three approaches are proposed. One utilizes DRIE and wafer bonding technologies to build a thick (~120μm) proof-mass with a narrow sensing gap. The other accelerometer is an all-silicon device implemented with a well-characterized combined surface and bulk micromachining technology. The third one is an accelerometer with sub-micron sensing gap utilizing electron beam lithography and DRIE.

1.2.2. Silicon-on-Glass (SOG) Accelerometer

In this section, we report a low noise, high sensitivity *in-plane* bulk-silicon accelerometer utilizing a thick (~120μm) proof-mass with a narrow sensing gap (~3.4μm) using wafer bonding technology and DRIE.

1.2.2.1. Structure

Figure 11 shows the SOG *in-plane* accelerometer structure. The accelerometer has a 120μm-thick proof-mass suspended over a glass substrate. This structure is simple and utilizes the well-known lateral combs for sensing and force feedback, except that it has a very large proof-mass and sense capacitance because of the substantial thickness of the device structure and the small sensing gap realized by DRIE.

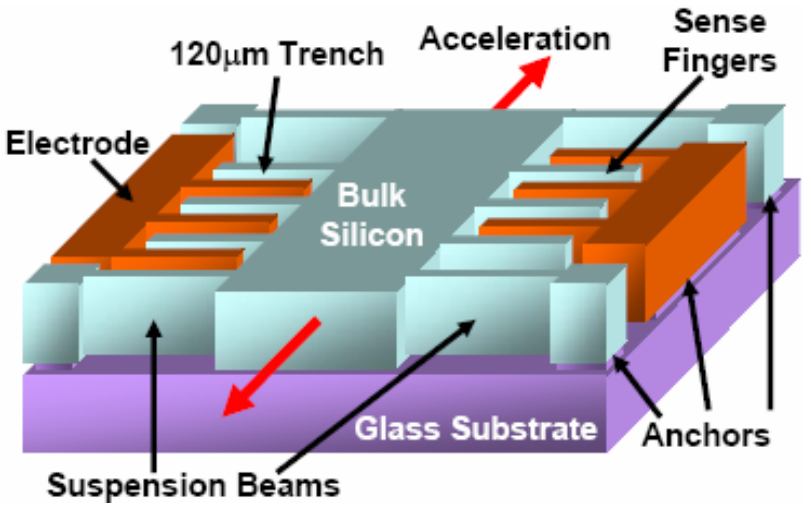


Figure 11: A schematic view of SOG *in-plane* accelerometer.

1.2.2.2. Design Optimization

In order to achieve high sensitivity and low noise performance, a target object function is defined as (Sensitivity / Mechanical noise):

$$\frac{Sensitivity}{MechanicalNoise} \propto \frac{\sqrt{A \cdot n}}{H_{electrode} \cdot k} \frac{M^2}{d_o^{1/2}} \qquad \text{Equation 4}$$

where A is sensing area, n is the number of sense electrodes, $H_{electrode}$ is the height of an electrode, k is the spring constant, M is the mass of proof-mass, and d_o is sensing gap.

As shown in the equation, six independent parameters determine the object function, with a number of dependent design parameters which would be constrained by application specifications. The dependent parameters are:

1) Mechanical dimensions:
   Length / Width ratio of proof-mass, Length & Width of sense fingers, Die size
2) Physical characteristics:
   Cross-axis sensitivity, Quality factor, Shock resistance, Operating range
3) Electrical properties:
   Sense capacitance, Cut-off frequency, Pull-in voltage, Stability in closed-loop operation

The initial design target for mechanical noise density is 10μg/√Hz. The thickness of the proof-mass is 120μm, but it could be made thicker. Each dependent parameter can vary within a range of what is considered a good estimate for a low-g, low-frequency application. In order to perform an efficient optimization process, a customized weight function has been assigned to each parameter to avoid unnecessary trivial minor adjustments.

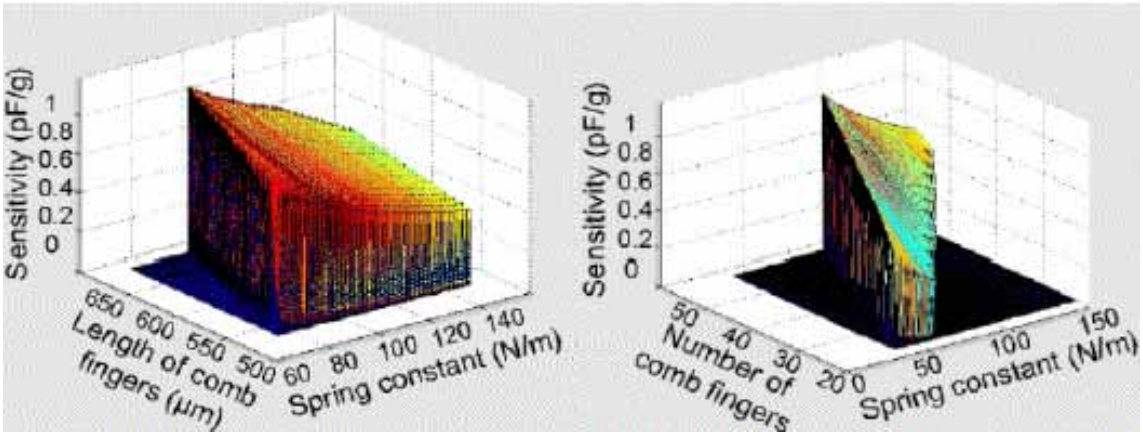


Figure 12: Parameter optimization.

Figure 12 shows two 3D plots of the optimization. The plots illustrate how high sensitivity can be obtained according to two independent with four fixed parameters based on mechanical noise of 10μg/√Hz device. Table 3 summarizes the optimized design parameters. Note that the mass of the proof-mass is close to a milligram, which is an order of magnitude higher than surface-micromachined devices. Also, sense capacitance is substantial enough to guarantee immunity to parasitic capacitances, which enables hybrid assembly with readout electronics.

Table 3: SOG accelerometer design parameters.

Mass of the proof-mass	0.5 milli-gram
Resonant frequency	2.14 kHz
Thickness of the proof-mass	120 μm
Sensing gap	2.0 μm
Sense capacitance	32.1 pF
Spring constant of suspension beams	90.4 N/m
Cross-axis sensitivity	< 0.1 %
Sensitivity / Mechanical noise	(0.78 pF/g) / (10 μg/√Hz)

1.2.2.3. Fabrication

The fabrication process has only five-steps, requiring 3 masks as shown in Figure 13. The process is simple, requires no special steps other than Deep RIE, and does not require any high-temperature processing, which is favorable for post-CMOS processing. The glass substrate bonded to the single crystal silicon is insulating, which reduces parasitics and thereby facilitates interfacing with a hybrid readout circuit.

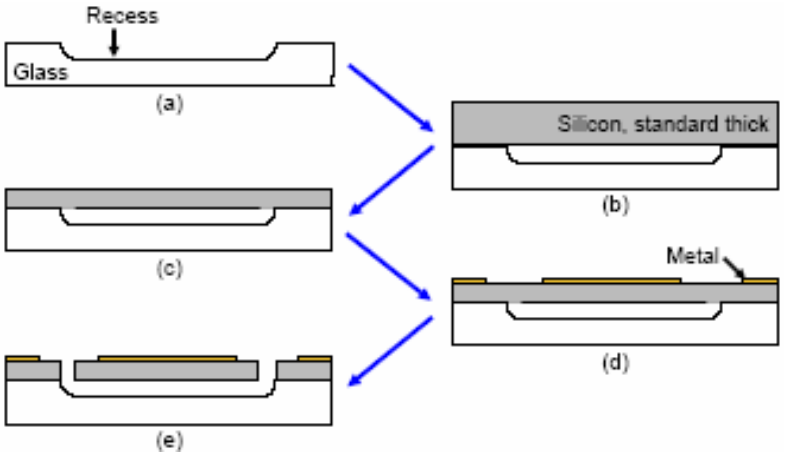


Figure 13: Fabrication sequence.

First, a glass substrate with a shallow recess (~3µm) is prepared for anodic bonding (a). Then, a standard silicon wafer is anodically bonded to the glass substrate (b). The silicon wafer is then thinned to 120µm using standard Chemical Mechanical Polishing (CMP) (c). After the CMP step, the metal contacts (200Å Cr/ 5000Å Au) are evaporated and patterned. Finally, the wafer is DRIE etched to define the proof-mass and sensing fingers.

Figure 14 shows SEM views of the SOG accelerometer and a shock stop. The accelerometer dimensions are $2.2\times3.0\times0.12mm^3$. The shock stop prevents the excessive movement of the proof-mass to protect sense fingers from an external shock. Figure 15 shows a vertical etch profile and sense gap after 70 minutes Deep RIE, which provides more than 100 µm with angle of 89.5°. Although the sensing gap is designed to be 2µm, it becomes wider, 3.2µm, due to finite lateral etch during the high aspect ratio etch. This reduces device sensitivity because the sensitivity is proportional to d_o^{-2}.

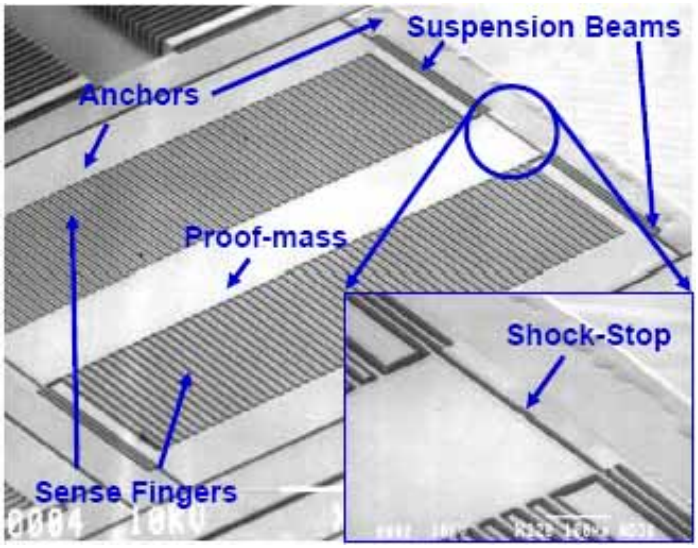


Figure 14: Top view of fabricated SOG accelerometer and shock stop.

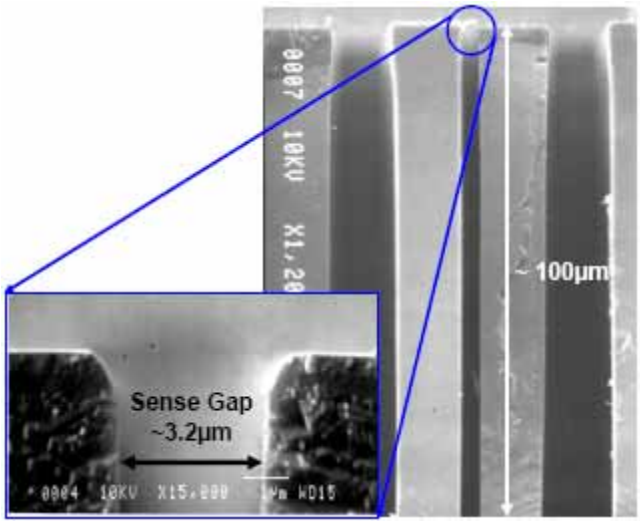


Figure 15: Vertical etch profile of sense fingers and sense gap after 70minutes Deep RIE.

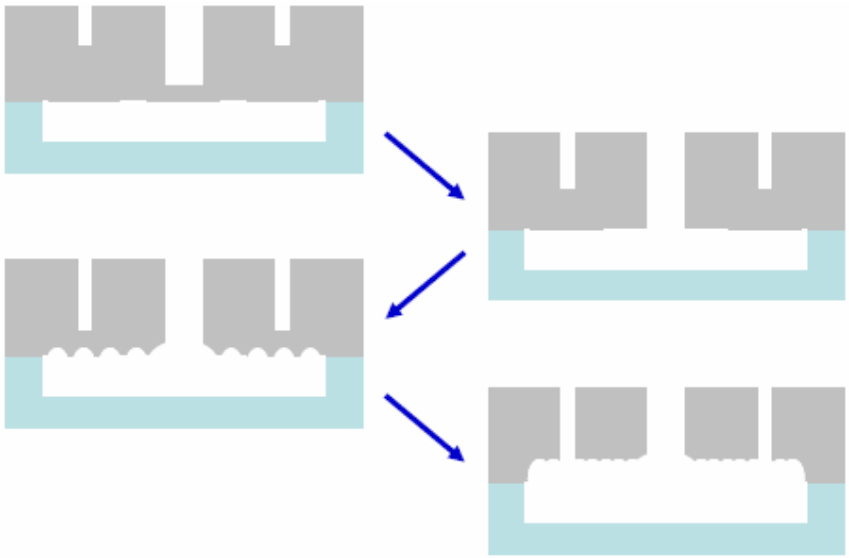


Figure 16: Micro-loading effect.

Micro-loading effect becomes significant when etching two different width trenches side-by-side. Obviously, SOG devices have different size trenches, which make them vulnerable to this effect. Figure 16 illustrates the micro-loading effect. As the DRIE etch proceeds, a wide trench is etched faster than a narrow trench due to different etch rates. Once the etching of the wide trench is complete, positive ions reach the bottom of silicon through the wide trench, get charged up on the glass substrate, and attack silicon from the bottom side, which results in a thinner structure [25]. After 70 minutes etch, the proof-mass from the device is taken and placed upside down to observe the micro-loading effect, as is shown in Figure 17. Note that the roughness of the sense fingers is due to the non-directional etch from the bottom of silicon through the wide trench. The cross sections of the proof-mass and the sense fingers are also shown in Figure 17. The thickness of the sense fingers is 100µm instead of 120µm, which results in 20% sensitivity

reduction due to the loss of sense area. Moreover, the vertical etch profile is compromised as well due to the micro-loading effect, which introduces non-linearity.

In order to prevent etching from the back side, before bonding the silicon wafer to the glass substrate, a shielding metal layer is deposited on the glass under the silicon. In so doing, both silicon and glass have the same electrical potential, which prevents charging up the dielectric substrate [25]. As a result, sense fingers maintain their original height and near ideal vertical sidewall profile as shown in Figure 18.

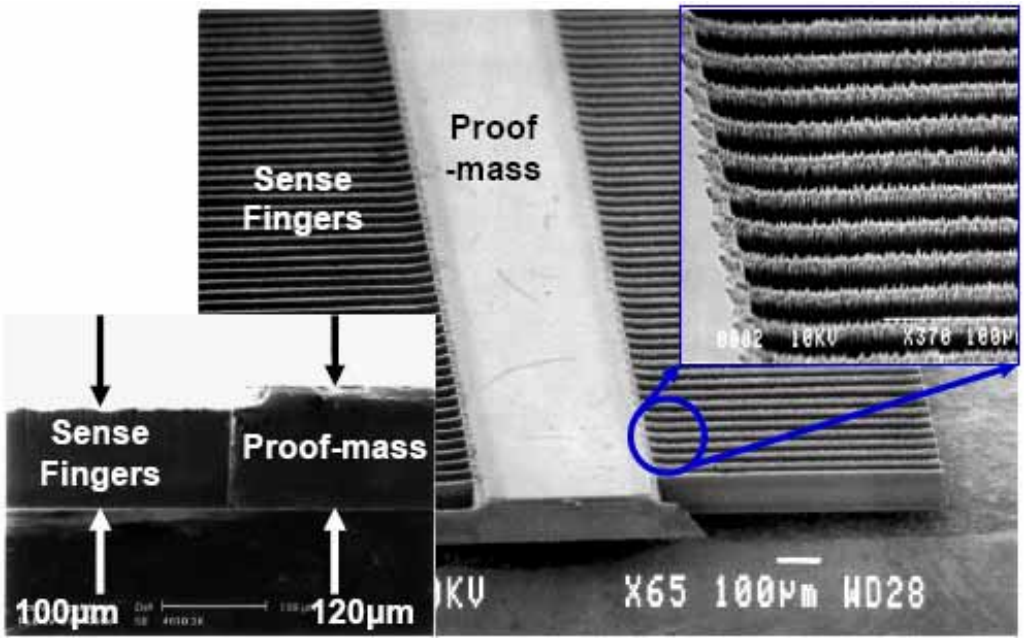


Figure 17: Micro-loading effect on the SOG accelerometer.

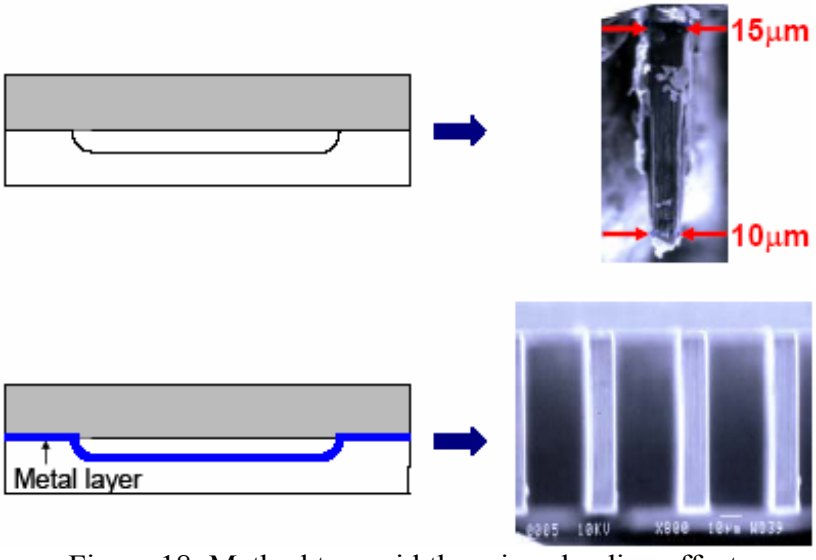


Figure 18: Method to avoid the micro-loading effect.

1.2.2.4. Post-CMOS Monolithic Implementation Technique Utilizing SOG Configuration

1.2.2.4.1. Motivation

Surface micromachining technology has been used extensively for industrial MEMS sensor products [17, 26-28]. One of the biggest advantages of surface micromachining technology is easy monolithic integration with electronics. However, surface micromachined devices often do not satisfy the requirements of high performance applications. In order to meet these requirements, devices fabricated using SOI or bulk micromachining utilizing wafer bonding technologies have been developed [20, 21, 29, 30]. The Silicon-On-Glass (SOG) device, presented in the previous section, is one of them. Although these devices offer higher sensitivity and lower noise floor than surface micromachined devices, monolithic circuit integration with these devices is a challenge. This is because the sensors often require additional steps before or after standard circuit fabrication process.

In this section, a standard post-CMOS monolithic fabrication technique utilizing the SOG configuration is presented. This technique implements a dielectric bridge, silicon islands, and SOG configuration to provide simple, robust, and fully post-CMOS compatible MEMS integration technique.

1.2.2.4.2. Monolithic implementation technique.

In order to satisfy all the requirements for monolithic implementation and micro-g accelerometer, the SOG configuration utilizing silicon islands and a dielectric bridge is developed. The implementation technique is simple, very robust, and low temperature, which makes it fully compatible with post-CMOS fabrication. A glass substrate supports the silicon islands and signal routing is provided with the help of a dielectric bridge between the silicon islands. Anodic bonding and DRIE steps are required to build the MEMS devices.

Figure 19 illustrates the monolithic implementation scheme. All pieces of silicon are supported on a glass substrate. A metal layer is used for interconnection lines. Different silicon regions are electrically isolated from each other since the DRIE step separates the bulk silicon into electrically isolated silicon islands. Although the thickness of silicon is chosen as 120μm in this work, it can be thicker up to full wafer thickness. It is determined by the capability of DRIE, which is limited only by the required aspect ratio of MEMS structures.

Figure 20 illustrates the structure of the dielectric bridge carrying signals between silicon islands. The interconnection lines made of a metal layer go over the silicon islands with the help of the dielectric bridge. The dielectric bridge consists of a number of layers such as thick field oxide and CVD oxide. The films used in the bridge should be selected carefully since they may cause significant amount of stress to buckle the bridge. To enhance the mechanical strength, polysilicon layers which are also available in conventional IC fabrication could be added to the bridge. The routing of signal lines is performed underneath the silicon islands, which is not

exposed to post-CMOS fabrication process steps. Power supplies from outside, such as V_{DD}, V_{SS}, ground or testing and sensing pads are connected from the top of silicon islands.

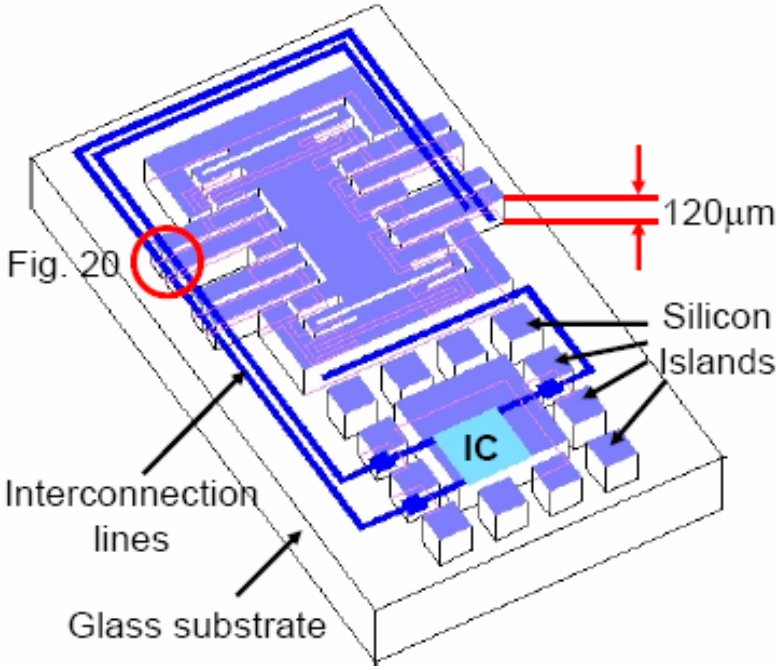


Figure 19: SOG monolithic implementation scheme.

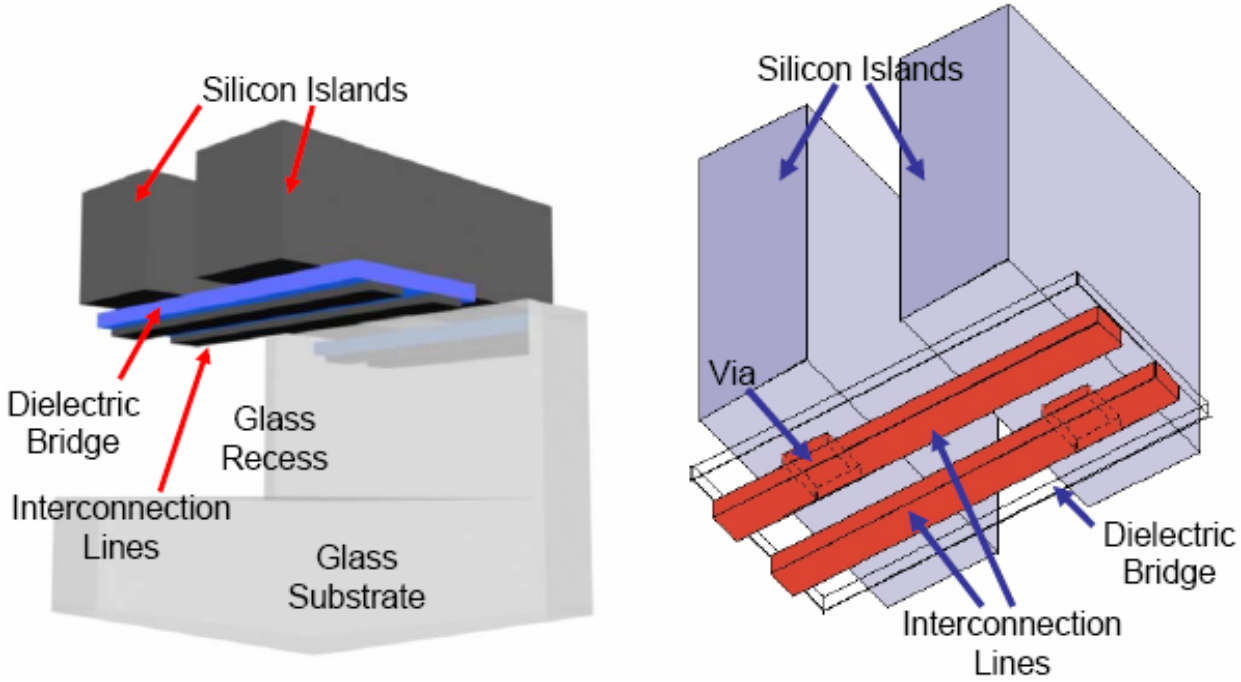


Figure 20: Dielectric bridge and silicon islands.

1.2.2.4.3. Fabrication

Figure 21 illustrates the simplified integration process. First, conventional IC fabrication is performed on a silicon wafer. A glass substrate with a recess and a shielding metal is also prepared. The metal is deposited and patterned on the glass substrate not only to avoid the micro-loading effect from the following DRIE, but also to protect the IC from large electric field during the bonding process. Next, the fabricated silicon wafer is anodically bonded to the glass substrate, and is thinned to the desired thickness using CMP. Finally, metal contacts are formed, and DRIE is used to define the MEMS structure, silicon islands, and dielectric bridges. Note that every single piece of silicon is anchored (bonded) to the glass substrate.

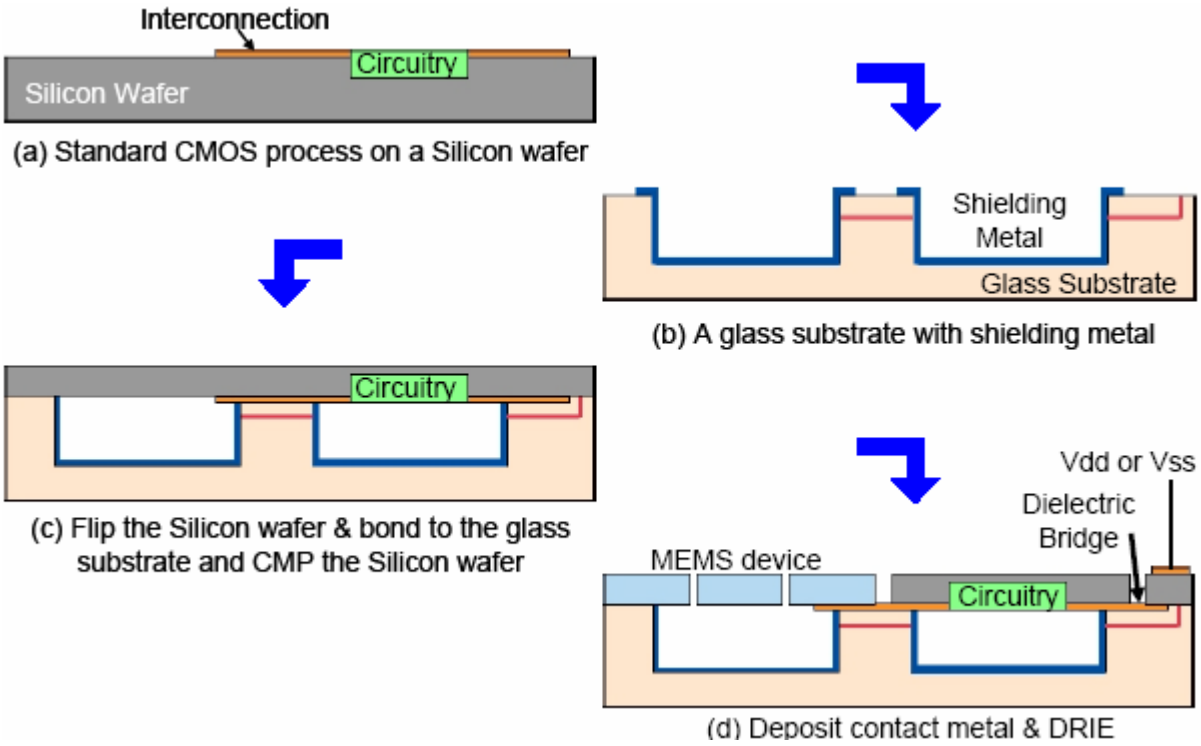


Figure 21: Fabrication sequence of SOG monolithic implementation.

An integrated SOG accelerometer has been fabricated using the U of M 3μm 2-poly 1-metal CMOS process. The architecture of the CMOS circuits is a regular 2nd order electromechanical Σ-Δ modulator, which is exactly the same as the 1st generation read-out circuits that we have developed [31]. Since the U of M CMOS process only allows 2-poly and 1-metal, signal routing of the circuits is quite limited. Also, the performance of the circuits is not much improved than the 1st generation circuits due to 3μm fabrication process. In this work, the purpose of monolithic integration is to present monolithic implementation capability of SOG configuration with CMOS electronics.

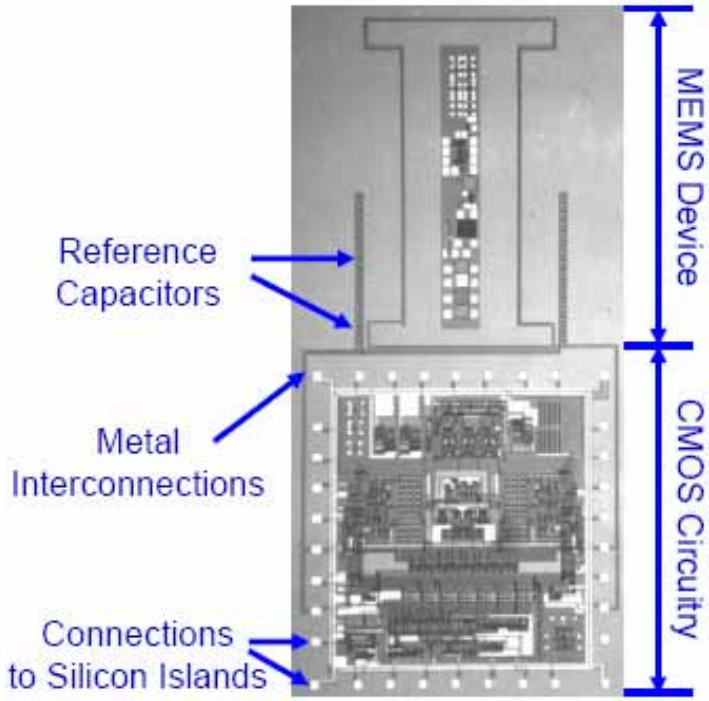


Figure 22: Fabricated integrated MEMS device with readout electronics.

Figure 22 shows an optical photograph of a MEMS device integrated with readout electronics before post-CMOS fabrication process. Reference capacitors for full bridge operation of the MEMS device, metal interconnections, and connection to silicon islands are shown.

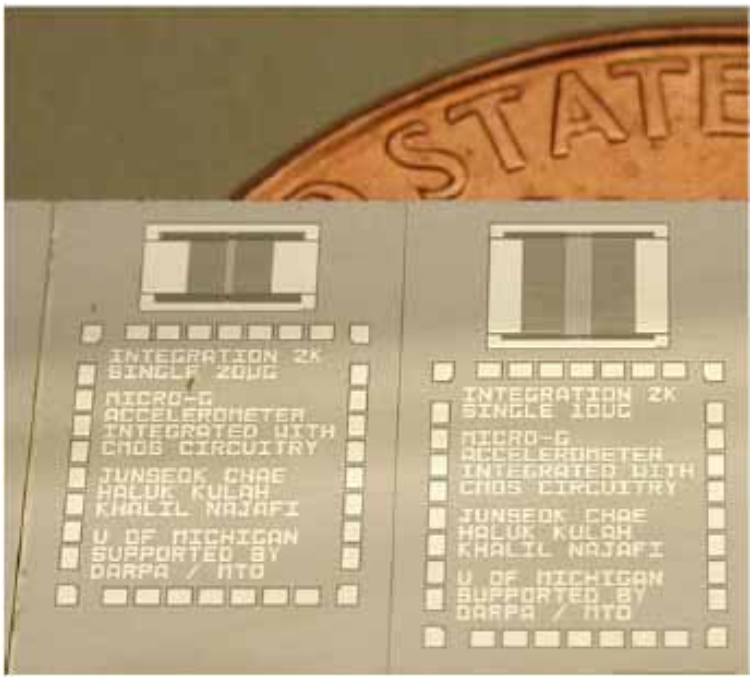


Figure 23: Fabricated chip after Post-CMOS process.

The fabricated wafer is bonded upside down to a glass substrate. Figure 23 shows the fabricated chip after post-CMOS fabrication steps, including anodic bonding, CMP, and DRIE. Each metal pad on top of a silicon island is electrically isolated from another, and is used to connect to the outside world.

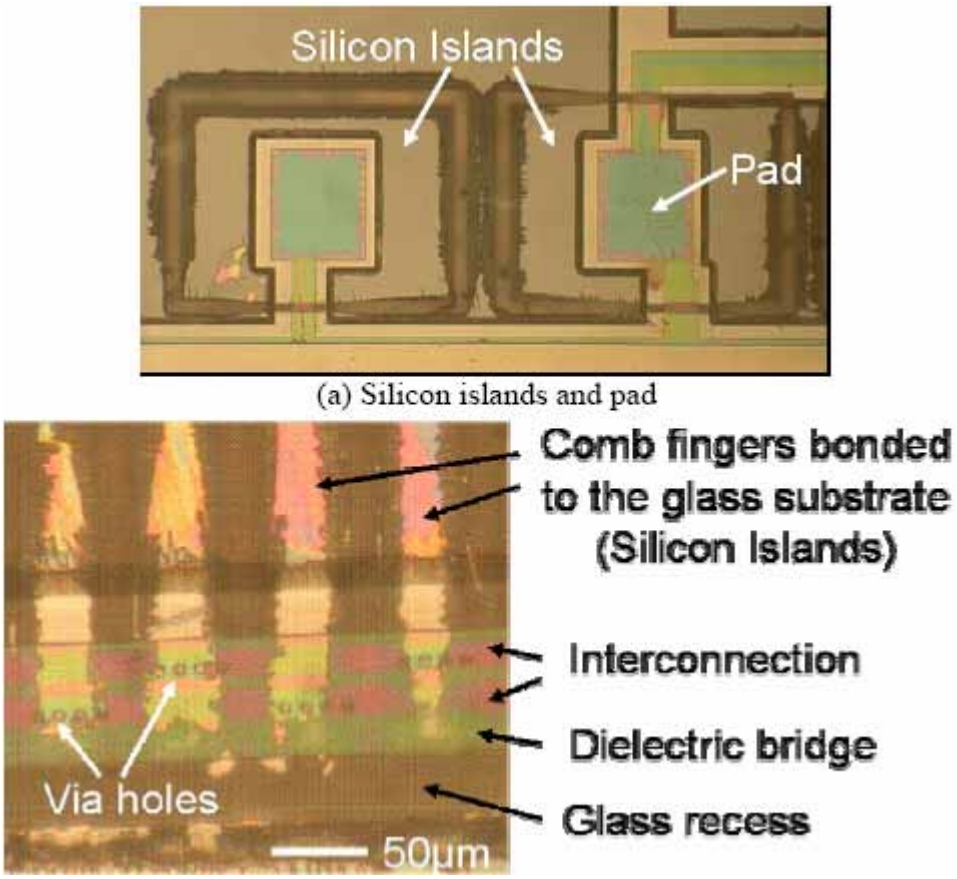


Figure 24: Silicon islands, dielectric bridges, and interconnection.

Figure 24 shows the silicon islands, dielectric bridges, and interconnection seen from the back side of the wafer through the glass substrate. Each Pad from readout circuit forms silicon islands bonded to the glass substrate (a). Comb fingers are bonded to the glass substrate as well, and each of them is electrically connected by interconnection lines on the dielectric bridge (b).

1.2.3. All-Silicon Accelerometer

In this section, a high-sensitivity, low-noise *in-plane* all-silicon accelerometer which utilizes a full wafer thickness proof-mass, high aspect-ratio electrodes, and small conformal sensing gaps using a combined surface and bulk micromachining technology is presented.

1.2.3.1. Structure

The all-silicon *in-plane* accelerometer structure is illustrated in Figure 25. This has a large proof-mass, stiff sense/drive electrodes, and a small and reproducible sensing gap. The silicon proof-mass is supported using high aspect-ratio polysilicon springs, which are formed by refilling deep-etched trenches [32]. Polysilicon trench refilling is also used to form vertical sense/drive electrodes, which are attached to the fixed support rim and span the entire width of the proof-mass. The cross-section of differential capacitive sense/drive electrode pairs is also shown in the figure. The proof-mass is released in wet silicon etchants such as EDP. This same etching step is used to etch the silicon around the outside perimeter of the sense/drive electrodes as illustrated. Unlike conventional *in-plane* accelerometers, the proposed *in-plane* silicon accelerometer uses a bridge-type electrode configuration.

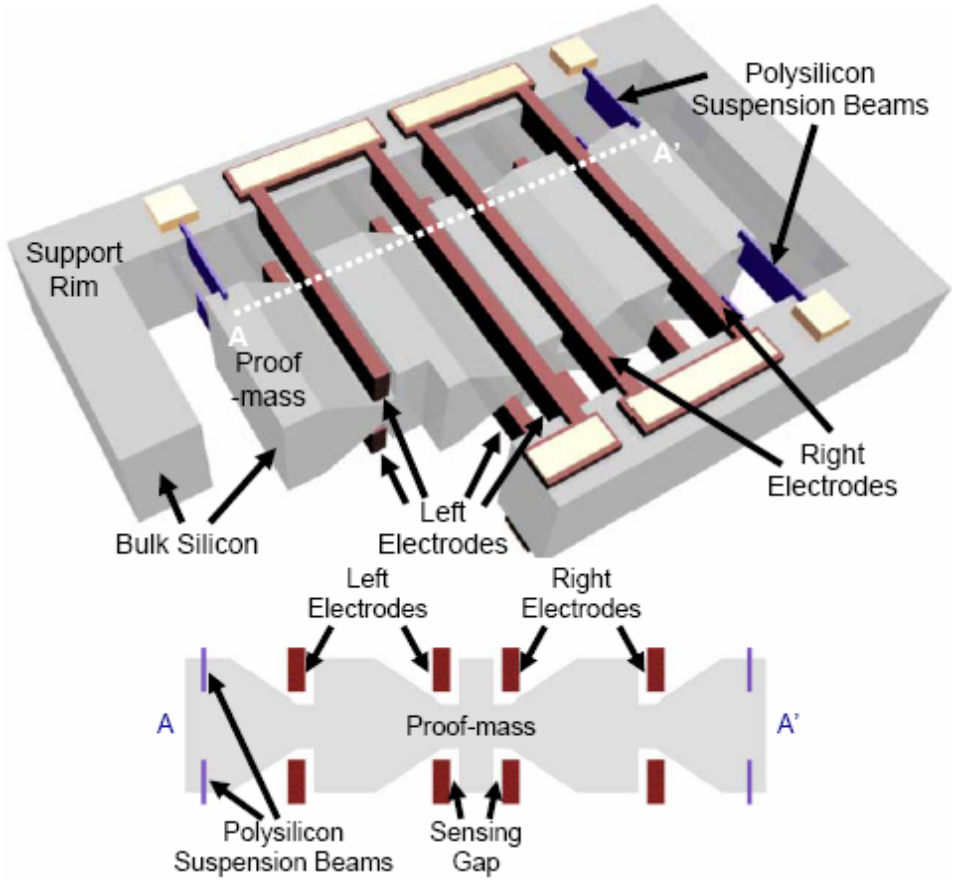


Figure 25: Top view and cross-section of the proposed *in-plane* accelerometer [33].

Note that one side of the proof-mass forms the sense capacitor with the sense/drive electrodes, while the other side is etched and does not form a capacitor with the electrodes. This is necessary and important in order to ensure that the sensitivity of the device is not compromised when the proof-mass moves. The electrodes and beams are also formed on the bottom side of the device to reduce cross-axis sensitivity and offset.

Most capacitive accelerometers utilize force feedback to achieve a high dynamic range and high bandwidth [24, 28, 34]. This feedback force is applied between two sets of sense/drive electrodes, one attached to the substrate and the other attached to the proof-mass. When a voltage is applied between these electrode sets, electrostatic force is generated and tends to attract the proof-mass toward the fixed electrodes. Obviously, it is important that the sense/drive electrodes be stiff enough so as not to bend when this force is applied. Otherwise, the feedback force causes unstable operation [35]. Many *in-plane* devices use long and narrow comb finger electrodes on a relatively small proof-mass (few micro-gram weight, 2~50μm thickness). These long and narrow comb fingers cannot be used if the proof-mass gets bigger—in the order of milli-gram weight with full wafer thick (~500μm)—because the fingers are not stiff enough to resist bending in the direction of the applied force. Therefore, a more rigid configuration of electrodes is required to ensure stable operation for the *in-plane* accelerometer with large proof-mass.

The proposed *in-plane* accelerometer uses bridge-type electrode configuration. The bridge electrode configuration is much stiffer per unit length than cantilever type electrode. The stiffness (k, spring constant) of a cantilever beam (conventional scheme) is 64 times smaller than that of a bridge configuration with the same mechanical dimensions for the beam [36]. Note that the length of the sense/drive electrode is preferred to be large in order to increase sense area which is necessary to achieve high-sensitivity. Since the stiffness of a beam (electrode) is inversely proportional to l3 (length of a beam), the sense electrode in a cantilever-type comb finger scheme can bend when a large force is applied if the proof-mass becomes heavy.

The bridge configuration electrodes are implemented by polysilicon trench refilled technique in the *in-plane* silicon accelerometer. The thickness of the sense/drive electrodes made of polysilicon is determined by the width of trenches. The stiffness of the electrodes is mainly limited by the thickness of the electrodes, which is, at maximum, twice the thickness of the deposited polysilicon layer. The stiffness of the bridge electrode configuration can be further increased by using cross-bar inter-electrode stiffeners as illustrated in Figure 26. By using these stiffeners, stable and stiff electrodes a few millimeters long, as needed in high-sensitivity devices, can be formed.

Specifications of the *in-plane* silicon accelerometer are summarized in Table 4. Note that the estimated sensitivity is comparable to that of *out-of-plane* devices while mechanical noise is sub-μg/√Hz due to large proof-mass.

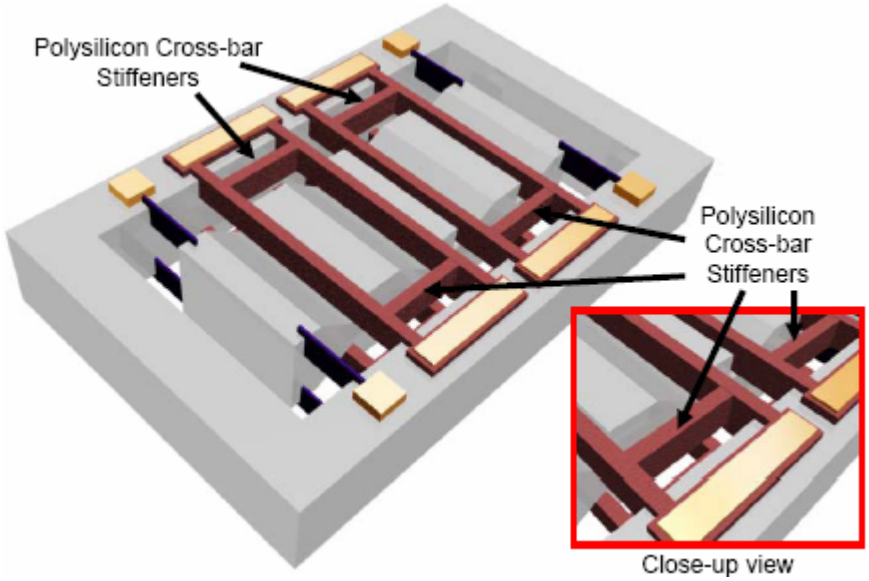


Figure 26: Improve stiffness of electrodes by using inter-electrode cross-bar stiffeners.

Table 4: *In-plane* silicon accelerometer design specifications.

Size of the proof-mass	2.4×1.0 mm^2
Length of an electrode	2 mm
Sense area	70 μm × 760 μm × 20
Sensing gap	1.2 μm
Resonant frequency	0.5 kHz
Sense capacitance	7.7 pF
Estimated Sensitivity	6.8 pF/g
Mechanical Noise floor	0.7 μg/√Hz

1.2.3.2. Fabrication

Figure 27 shows the fabrication process of the accelerometer. It is a double-sided process (although processing can be carried out only on one side of the wafer) that requires six masks, utilizes silicon dioxide as a sacrificial layer, and defines device structure with anisotropic wet etching at the end of the process. This is the same exact process used for fabricating an *out-of-plane* accelerometer which has been developed by our group and does not require any additional steps [13].

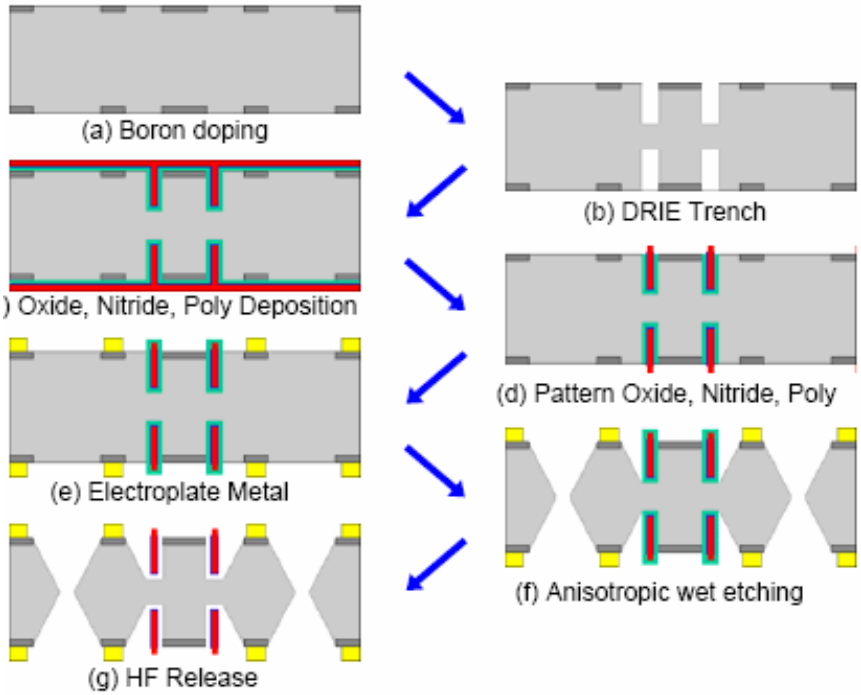


Figure 27: Fabrication process sequence of the *in-plane* accelerometer.

The process starts with a shallow p^{++} boron diffusion, defining the proof-mass and supporting rim, on <100> double-side polished p-type silicon wafers. Then, 70μm deep trenches are etched in the silicon to be used later to form the vertical electrodes. The trenches are then refilled completely with oxide for a sacrificial layer, nitride, and doped polysilicon. After polysilicon deposition, annealing is followed to alleviate any compressive stress in the polysilicon. Next, the polysilicon and nitride films are etched using RIE and another oxide (capping) is deposited. The oxide is patterned to form metal contact vias and openings to the bulk silicon for the subsequent anisotropic wet etching such as EDP. Then, contact metal is electroplated. To minimize the anisotropic wet etching time and help undercut the electrodes by the etchant, some of the single-crystal silicon is etched by DRIE. After the DRIE, Anisotropic wet etching is followed not only to define the proof-mass and supporting rim but also to etch the unnecessary silicon around the sense/drive electrodes. This step is important since the unnecessary silicon would reduce the capacitance change from an external acceleration resulting in sensitivity degradation. Finally, the sacrificial oxide layer is removed by HF.

Anisotropic wet etching is crucial for the *in-plane* silicon accelerometer. It not only defines the proof-mass and the rim by selective etching, but also removes unnecessary silicon around sense/drive electrodes. Figure 28 illustrates how the anisotropic wet selective etching defines the proof-mass, rim, and sense/drive electrodes. After DRIE to minimize the anisotropic wet etching time and to help undercut the electrodes, Anisotropic wet etching is performed to separate the proof-mass from the rim as well as remove unnecessary silicon around the sense/drive electrodes. Note that sense/drive sides of the electrodes are protected by boron diffused layer while the other sides are removed by anisotropic wet etch.

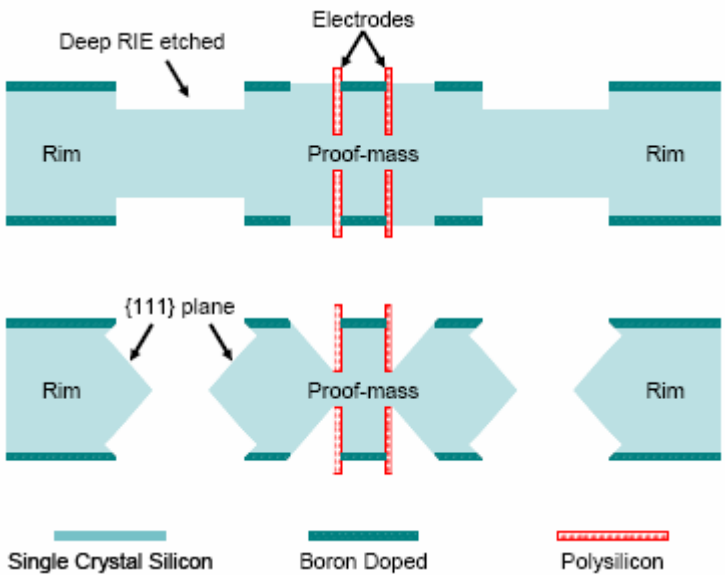


Figure 28: Anisotropic wet etch for the proof-mass, the rim, and the sense/drive electrodes.

In order to remove un-needed silicon around the sense/drive electrodes, the electrodes are at an angle with respect to <110> direction as illustrated in Figure 29. The wet etchant etches the bulk silicon until it meets <111> crystal planes. Without the corrugated electrodes, the wet etching stops when two <111> planes meet to form a V-groove. This does not remove un-needed silicon from the electrodes. By properly designing the shape of the electrodes, the wet etch continues until the <111> plane form a deep V-groove below the electrodes, as illustrated.

A fabricated accelerometer and close-up views of electrodes and polysilicon beams are shown in Figure 30 (a). Figure 30 (b) shows the cross-section of one 70µm tall electrode and the sensing gap of only 1.1µm.

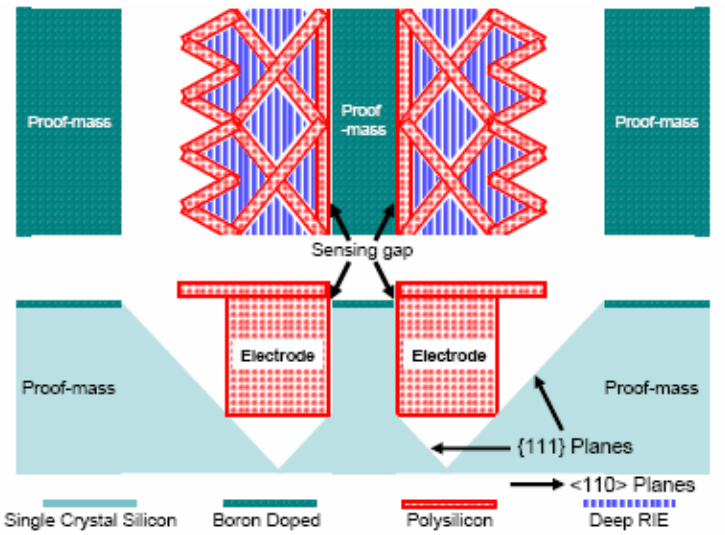
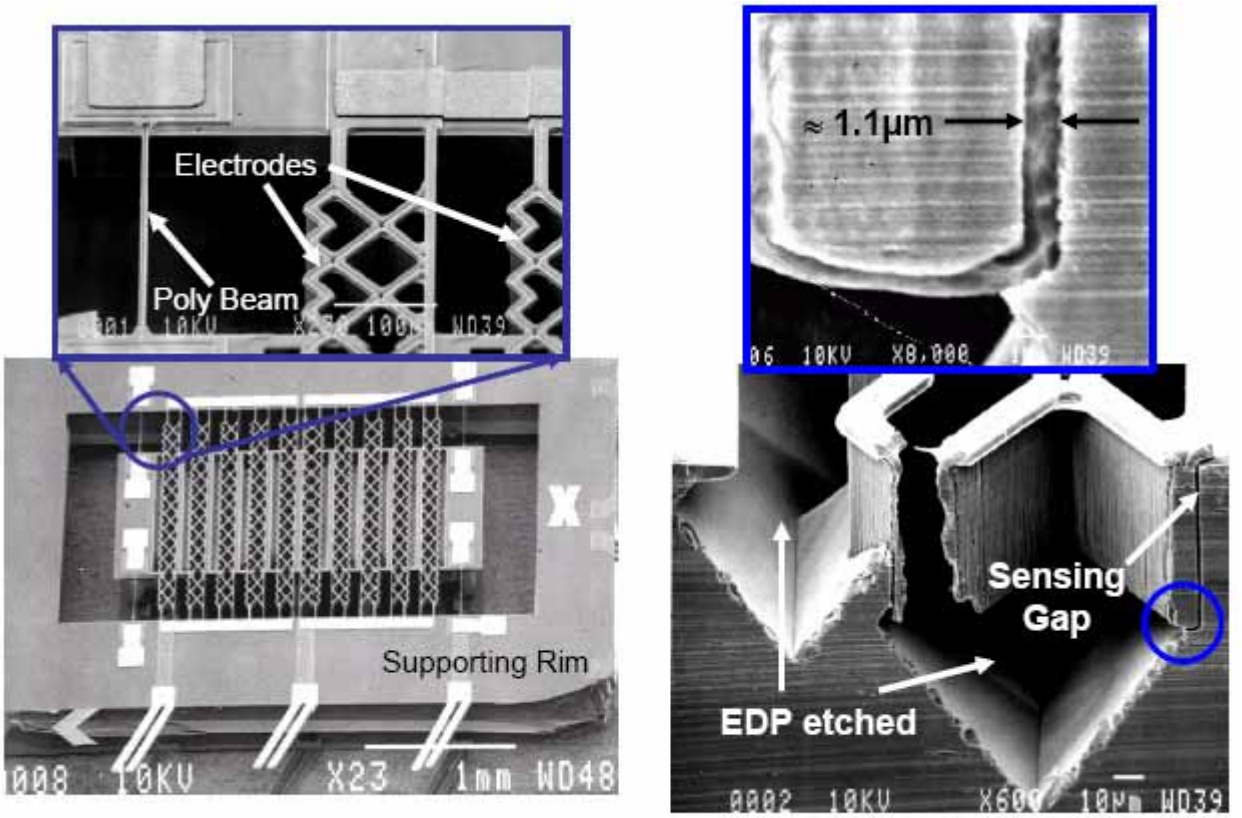


Figure 29: Anisotropic wet etch around the sense/drive electrodes.



(a) Top view of the *in-plane* silicon accelerometer.

(b) Cross section of the sense/drive electrode and sensing gap.

Figure 30: SEMs of a fabricated all-silicon *in-plane* accelerometer

1.2.4. A sub-micrometer gap accelerometer

A single crystal silicon accelerometer which takes advantage of sub-micrometer lithography and high density plasma etching in an inductively coupled plasma source has been developed. The high aspect ratios obtained using electron beam lithography and high density plasma etching allow very small capacitive gaps to be fabricated and very small sensor motion to be detected. This increases the sensitivity of the device and makes possible the measurement of μg acceleration signals. Also, the single crystal silicon accelerometer is fabricated from the surface and requires no wafer bonding or backside processing. It is 3 μm thick with 0.2 μm comb gaps and compatible with integrated circuit (IC) processing techniques. Figure 31 shows an acceleration sensing structure. The device has 3 μm thick proof-mass with mass of 9.0 micrograms, and comb fingers with 3μm width, sensing gap of 0.2μm between them.

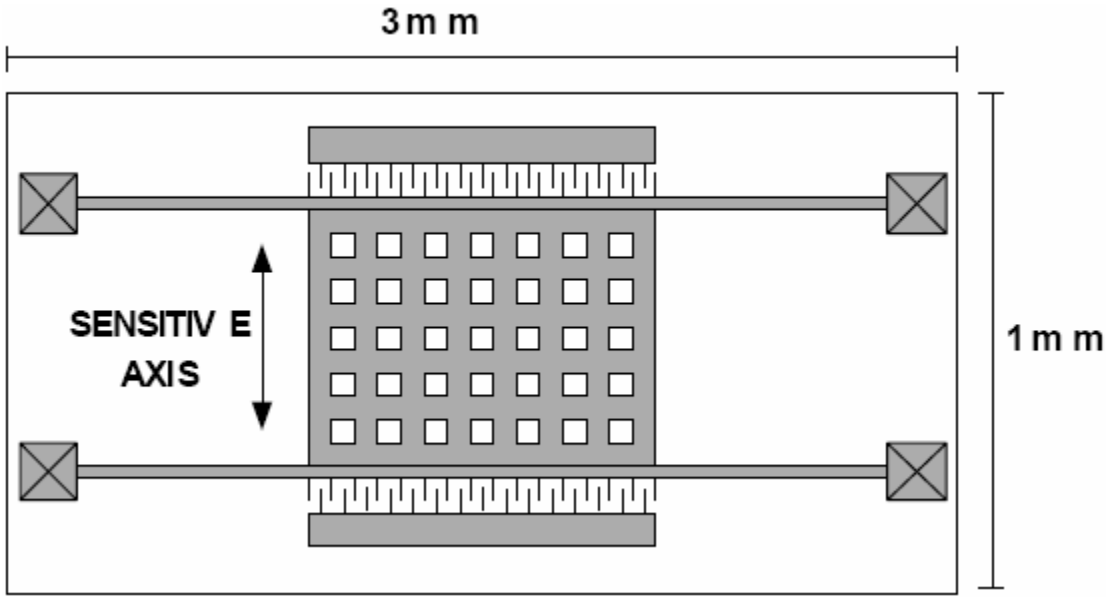


Figure 31: A schematic of a 1 mm by 3 mm die containing the acceleration sensor.

This structure has some advantages that make it particularly strong in certain applications. Since the substrate and the sensor are both made of single crystal silicon, it is expected that the sensor performance will be less sensitive to temperature variations. Typically, sensor output will vary with temperature due to the difference in thermal expansion coefficient between the sensor structure and the material to which it is anchored. However, since this device and the substrate are all made of silicon, both will expand and contract at the same rate with varying temperature, and the output should remain stable over temperature. The comb drive on this sensor utilizes a varying overlap area for capacitance change. This is often not used because the capacitance change is inversely proportional to the gap (a) between combs instead of utilizing a varying gap which has the change of inversely proportional to the square of the gap (b).

$$\Delta C = \frac{\varepsilon \cdot t}{d}\frac{F}{k} \qquad \text{(a)} \qquad \Delta C = \frac{\varepsilon \cdot A}{d^2}\frac{F}{k} \qquad \text{(b)}$$

where t is the thickness of a structure, d is the gap, F is applied force to the structure, k is spring constant, and A is sense area.

However, since the gaps utilized here are so small, adequate capacitance change can be achieved with the varying area comb drive and its advantages can be exploited. One advantage of this type of comb drive is that the pull-in voltage can be made very large. As the length of the comb fingers is increased, the pull-in voltage can be increased. The only limit to this occurs when the comb fingers are too long, they become less stiff in the off axis direction and can pull-in with off axis acceleration. However, if they are kept stiff, large accelerometer displacement can occur without any change in sensitivity. This large displacement was simulated and accelerations as high as 1000 g could be tolerated before the maximum stress in the device reached the yield strength of 7 GPa for silicon.

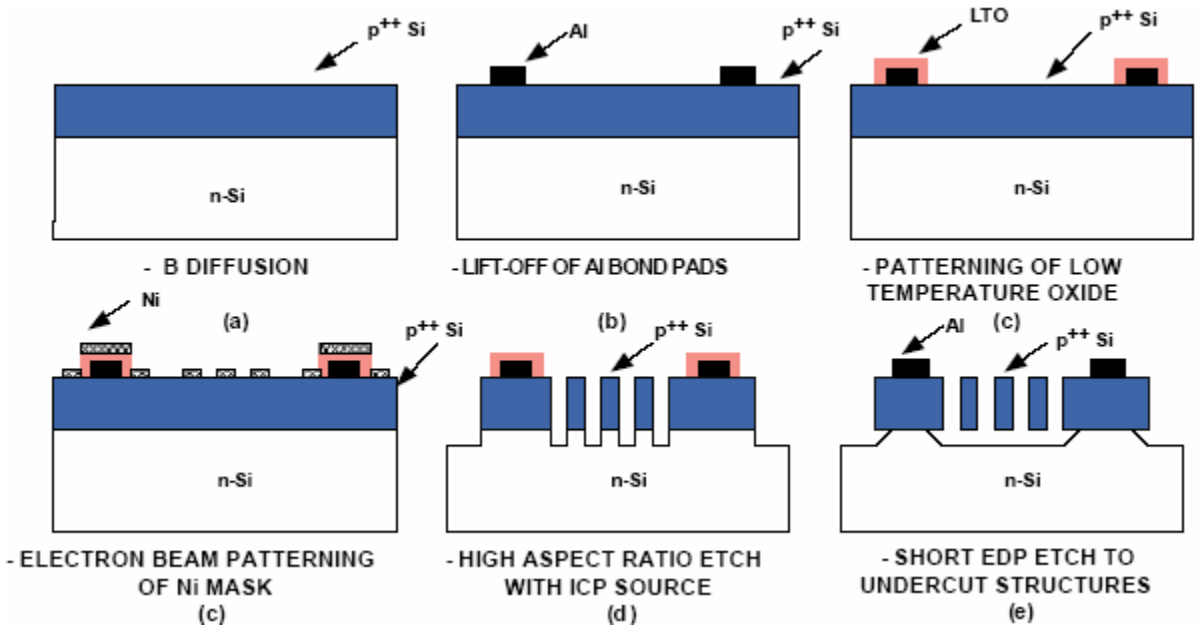


Figure 32: A schematic process flow for fabrication of the acceleration sensor with Al bond pads.

The sensors were fabricated using a simple 3 mask process which is shown schematically in Figure 32. The process begins with a shallow boron diffusion into an n-type silicon wafer to form a 3 µm thick p^{++} layer which determines the thickness of the final device. Next, a 1 µm thick aluminum layer is lifted off to form the aluminum bond pads as well as serve as alignment marks in the electron beam lithography system. A low temperature oxide (LTO) layer is deposited and patterned to cover the aluminum bond pads. This will protect the bond pads from the release etch in EDP. Electron beam lithography is then used to pattern polymethylmethacrylate (PMMA) to define the accelerometers with sub-micrometer beams and comb gaps. This patterned resist is used to lift off a 230 nm thick evaporated nickel dry etch masking layer. After lift off, DRIE is performed in an inductively coupled plasma (ICP) system. Next, the samples are etched in EDP for 15 min to release the structures. Finally the nickel mask is removed in hydro chloride acid (HCl) and the LTO is removed in buffered hydrofluoric acid (BHF).

Figure 33 shows a die photo of the completely released accelerometer. The surface around the structure shows texturing from the EDP release etch. And the suspended structure is shown in Figure 34 (a). The proof-mass can be seen suspended by one of the four beams and the aluminum bond pad is in the top of the figure. The comb fingers are also visible which provide drive capability and also serve to electrically sense the motion of the structure. In Figure 34 (b), a higher magnification of the comb fingers shows the vertical profile and sub-micrometer gaps generated by etching the high aspect ratio p^{++} doped single crystal silicon in Cl_2. These comb drives are 3 µm thick with 0.2 µm gaps in between.

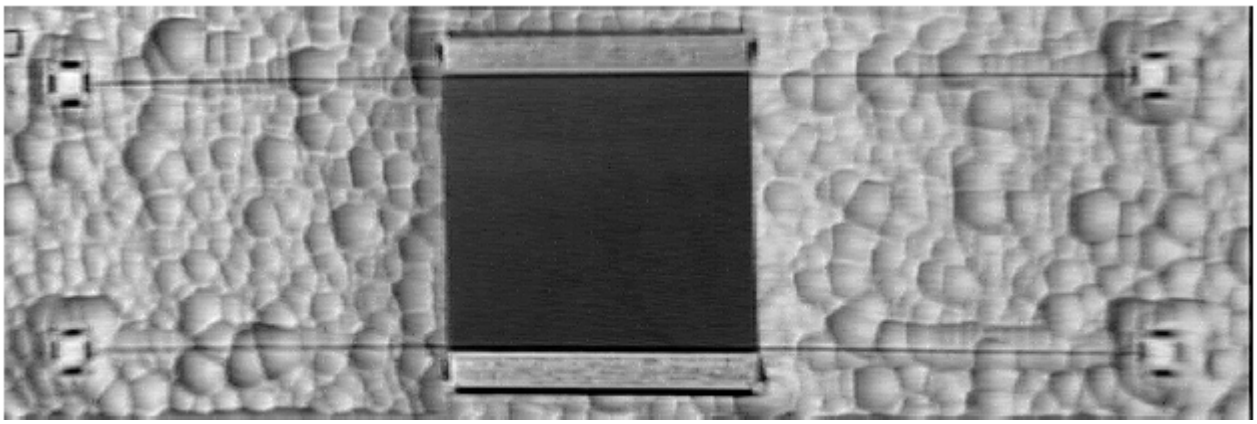


Figure 33: Die photo showing the whole accelerometer structure.

Preliminary tests were performed with fabricated devices. Figure 35 (a) presents a plot of capacitance-voltage (C-V) curve of a device with a 0.4μm beam width. Negative voltages must be applied so that the p^{++}/n diodes are kept reverse biased. The junction diodes will also have a junction capacitance, C_j, which varies with voltage. Therefore, this junction capacitance will serve to mask the sensitivity during C-V measurements. However, under normal device operation, a constant bias is applied, so that the junction capacitance will not vary. Thus, the junction capacitance variation should be subtracted out from the total measured capacitance change, yielding the capacitance change due to movement of the structure alone as also shown in Figure 35 (b). The measured sensitivity for one set of combs was 39.62 fF/g. Thus, operating using both combs will produce a sensitivity of 79.2 fF/g, which is higher than the calculated sensitivity of 44.2 fF/g.

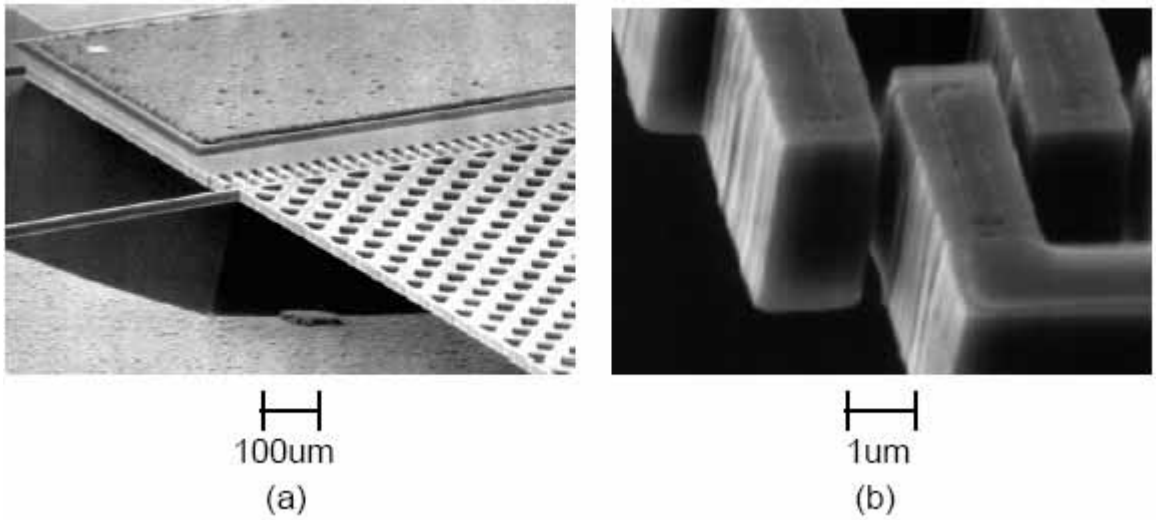


Figure 34: (a) SEM of a completely released accelerometer (b) Higher magnification of the comb drive showing the 3 μm thick high aspect ratio comb fingers with 0.2 μm gaps in between.

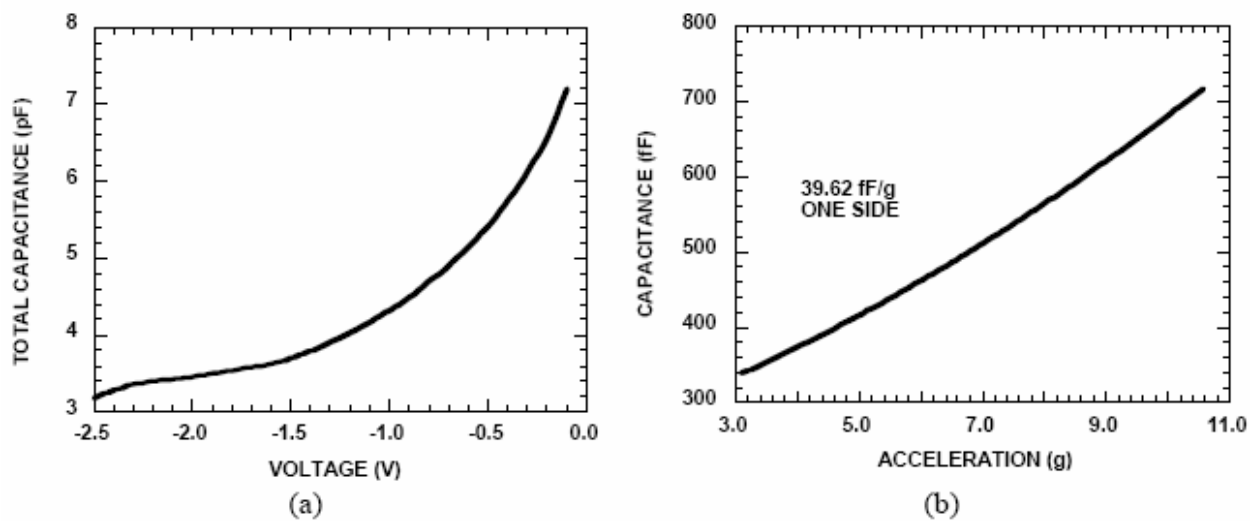


Figure 35: (a) C-V curve for fabricated accelerometer with 0.4 μm wide beams. (b) C-g curve determined by subtracting out junction capacitance variation.

Table 5 summarizes performances of two different accelerometers. The accelerometer sensitivity can be further improved by fabricating even narrower beams. 0.2 μm wide beams with 0.1 μm wide gaps can provide a sensitivity of 76 pF/g with a mechanical noise of 4.4 μg/√Hz.

Table 5: Expected and measured performances for 2 different accelerometers

	1μm beam width	0.4μm beam width
Spring constant	0.127 N/m (0.146 N/m)	0.03 N/m (0.027 N/m)
Sensitivity	6.3 fF/g (7.0 fF/g)	79.2 fF/g (44.2 fF/g)

1.3. Three-Axis Monolithic Accelerometer

1.3.1. Motivation

Since the first micromachined accelerometer was introduced in the late 70's [37], a few accelerometers have been developed to achieve micro-g resolution. However, most of the reported high performance capacitive accelerometers are only sensitive to a single-axis [3, 15, 20, 23]. For some applications such as inertial navigation, a micro-g resolution 3-axis accelerometer system is highly desired. In order to build a 3-axis precision accelerometer system, generally individual devices are hybrid mounted on the faces of a cube [23, 38]. This introduces misalignment of individual sensors, increases the cost, occupies large area, and requires complicated packaging.

Although a few integrated single-chip 3-axis capacitive micro-accelerometers have been reported [16, 39], due to small mass, low sensitivity, or low performance readout circuit, their output

noise floors are at best in the 0.04–1mg/√Hz range. Our group has reported *in-plane* (x- and y-axis) and *out-of-plane* (z-axis) capacitive silicon accelerometers with micro-g resolution [22]. Both implement a combined surface and bulk micromachining technology [32] and utilize an almost identical fabrication process. Thus, two *in-plane* and one *out-of-plane* accelerometers can be integrated onto a single substrate. This section presents a fully-integrated 3-axis accelerometer with a hybrid low-noise CMOS readout circuit providing truly micro-g performance for all three axes.

1.3.2. Structure

Figure 36 shows the structure of the 3-axis accelerometer. The 3-axis chip is a monolithic integration of three individual single-axis accelerometers. This reduces the size of the entire system and eliminates cross-axis sensitivity due to misalignment of individual devices. The 3-axis accelerometer is mechanically connected together by polysilicon connectors, which electrically isolate the three accelerometers to ensure cross-talk free operation. Unlike surface micromachined devices, the 3-axis chip utilizes a combined surface and bulk micromachining technology so that it has large structural mass (full wafer thick, 475µm), and large area electrodes with small sensing gap (<1.5µm), which produces high-sensitivity low-noise accelerometers. The size of the 3-axis chip is 7×9mm^2. All three devices have large proof-mass (~2milli-gram), large sense area (1~3mm^2), and small sensing gap (<1.5µm), resulting in high sensitivity and sub-µg/√Hz mechanical noise floor.

The specifications of the 3-axis accelerometer are summarized in Table 6. As shown, both *in-plane* and *out-of-plane* devices have high sensitivity (> ~3pF/g) and sub-µg/√Hz mechanical noise.

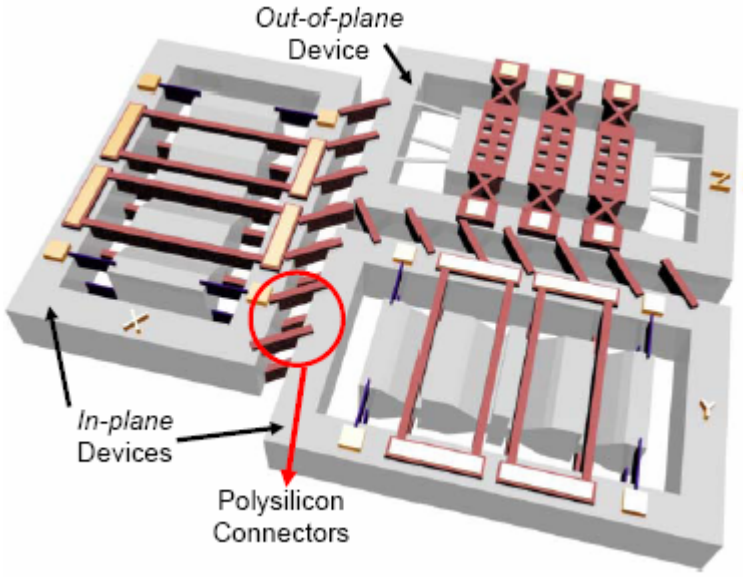


Figure 36: 3-axis single-chip micro-g accelerometer.

Table 6: 3-axis single-chip accelerometer specifications.

	In-plane	*Out-of-plane*
Mass [milli-gram]	2.65	2.2
Sense area [mm^2]	1.1	3.0
Sensing gap [μm]	1.2	1.5
Sense capacitance [pF]	7.7	17.7
Resonant freq. [kHz]	0.49	1.00
Spring constant [N/m]	25	88
Sensitivity [pF/g]	6.8	2.9
Mech. Noise [μg/√Hz]	0.7	0.7

1.3.3. Fabrication

The 3-axis accelerometer has almost identical fabrication process of *out-of-plane* and *in-plane* all-silicon devices previously described in this report. The polysilicon connectors, the only added part, between these devices are fabricated when their polysilicon electrodes are formed.

Figure 37 shows a fabricated 3-axis single-chip accelerometer. Two *in-plane* (x- and y-axis) and one *out-of-plane* (z-axis) devices are mechanically connected by polysilicon connectors. These connectors provide electrical isolation between individual devices to ensure cross-talk free operation as well as micro-scale alignment accuracy. The connectors are not really needed for the 3-axis accelerometer and the accelerometer could operate without them. The connectors are added to monitor individual single-axis devices for testing purpose as well as to have an individual access to the devices.

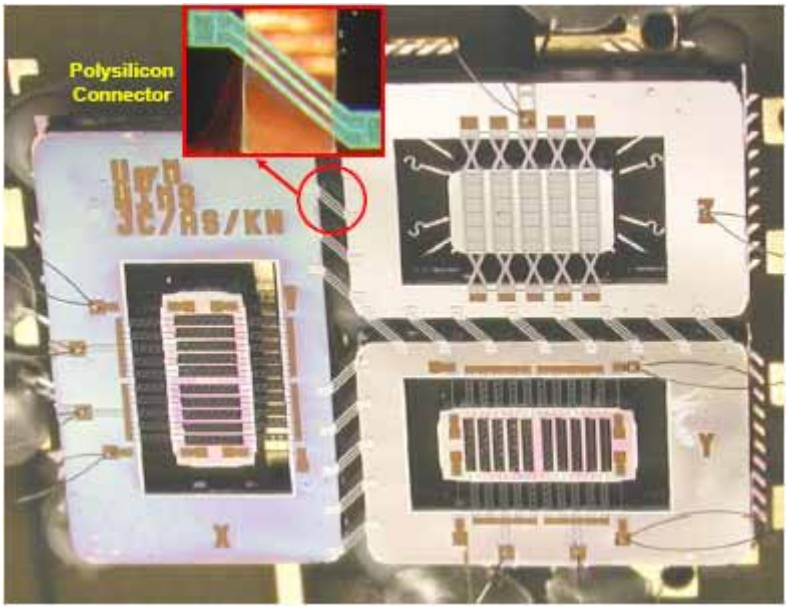


Figure 37: Photograph of the integrated single-chip 3-axis accelerometer, measuring 7×9mm^2.

1.4 Interface Electronics

1.4.1 Motivation

The silicon sensor is interfaced with the necessary circuitry to detect the capacitance change and to operate the sensor in a closed-loop force-rebalanced mode. Closed-loop operation of the micro-g accelerometer provides higher dynamic range, linearity, and bandwidth. The closed-loop approach requires the interface electronics to read out the capacitance change due to the deflection of the proof-mass, and provide a force-feedback signal to null the proof-mass position. Furthermore, the interface circuitry is required to realize the challenging task of over 18 bits analog-to-digital data conversion. Through this project three different generations of the interface electronics has been developed.

1.4.2 First Generation Interface Electronics

The first generation interface chip operates as a 2nd order electromechanical sigma-delta modulator together with the accelerometer. Figure 38 shows the general block diagram of the interface chip. The circuit forward path consists of a charge integrator and a regenerative latching comparator. The front-end charge integrator provides the capacitance readout as well as the electronic integration needed for the sigma-delta modulator loop. It has a fully-differential configuration to reduce the common-mode switching and power supply noise. Also a fully-differential circuit provides larger signal swing and cancels the even harmonics. The front-end amplifier uses a switched-capacitor circuit to cancel offset and flicker-noise, which also effectively results in enhancing the open-loop dc gain of the amplifier. The chip also integrates a digital lead-compensation circuit to stabilize the loop. The sensor-start-up block of the chip provides a proper power-on start for the sensor. Figure 39 shows the die micrograph of the chip.

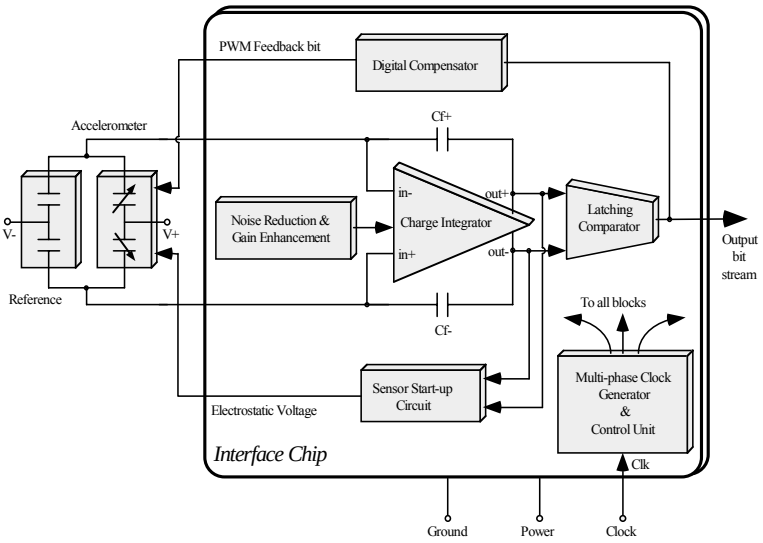


Figure 38: Schematic diagram of the μg accelerometer interface and control circuit.

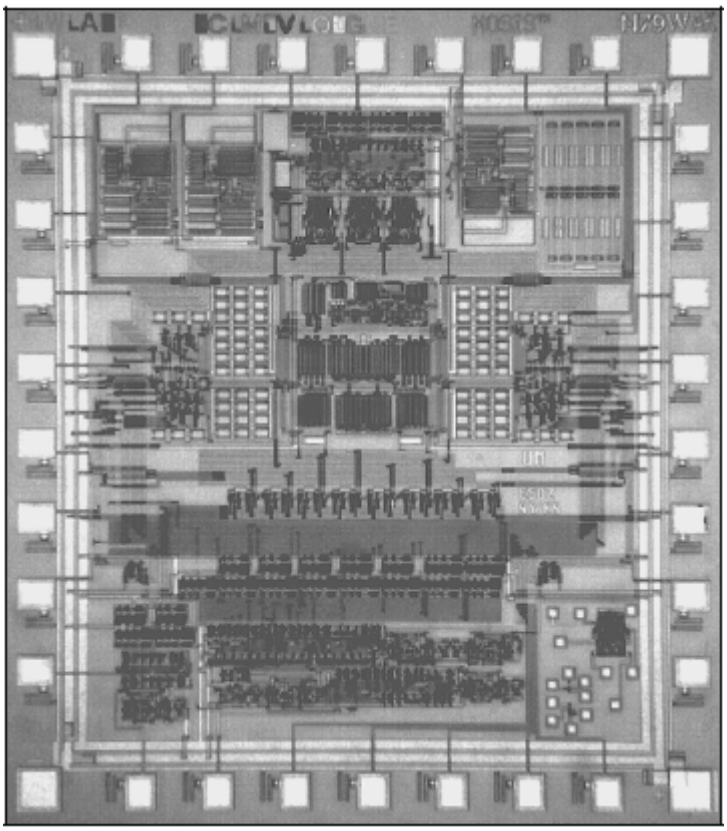


Figure 39: Die photograph of the interface chip.

Figure 40 shows the chip differential analog output with four charge integration cycles with a 500fF input capacitance difference. The output noise amplitude spectrum shown in Figure 41 indicates a good cancellation of 1/f noise and other low frequency noise sources. This is very essential to the application of the sensor in inertial navigation and microgravity measurements. A summary of the measured circuit parameter are presented in Table 7.

1.4.3 Second Generation Interface Electronics

The first generation interface chip has been integrated with *out-of-plane* accelerometers and tested in open-loop. These test results indicated that although the Brownian noise of the accelerometer itself is less than 1μg, the overall noise of the system is much higher than this showing that it is the interface electronics dominating the system noise. Therefore, to achieve sub-μg performance, it is inevitable to improve the readout circuit performance. According to this result, the electromechanical sigma-delta system has been analyzed in detail and all the noise sources were identified.

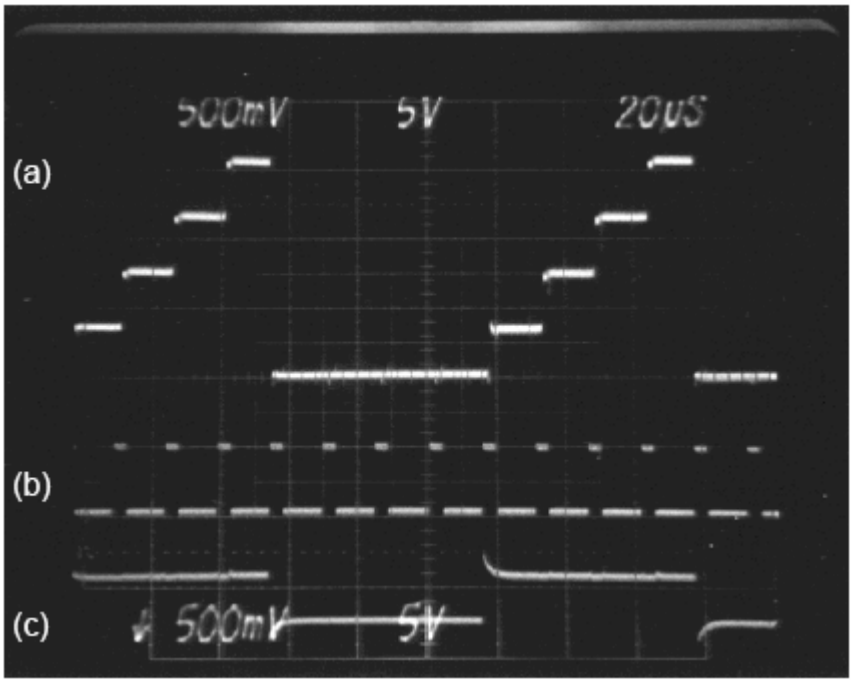


Figure 40: The chip differential analog output with four charge integration cycles followed by an active low reset. The input capacitance difference for this measurement has been 500fF: (a) Differential output, (b) Charge integration clock (Readout phase), (c) Active low reset signal.

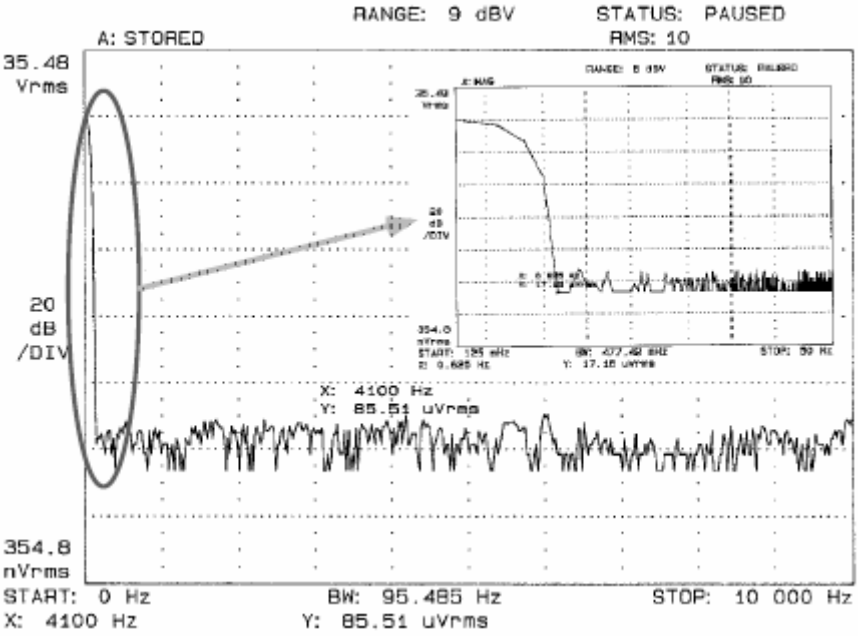


Figure 41: The output noise spectrum. A very good near dc low-noise performance is observed in the inset close-up.

Table 7: Interface circuit measurement results and parameters.

Interface IC Parameter	Value
Size	2.6 x 2.4 mm^2
Sampling Clock	200kHz
Power Dissipation	<6.6mW @ 5V
Capacitance Sensitivity	0.3-1.1V/pF
Noise Floor	85 μV/√Hz
Capacitance Resolution	<75 aF
Dynamic Range (1Hz BW)	95dB
Offset	2.7mV without Switch Chopper Stabilization 370μV with Switch Chopper Stabilization (82 ppm with respect to full output range)

Sensor & Interface IC Module	
Equivalent Acceleration Resolution	< 6.9μg/√Hz
Full Scale Range	±1.2g with 5V Supply

There are several noise sources affecting the overall system resolution of an accelerometer system. These noise sources can be classified in two main groups: mechanical and electrical [40, 41]. Mechanical noise is due to the Brownian motion of the proof-mass and is directly related to sensing structure design and environment. It has been shown that this noise can be decreased down to 0.1μg/√Hz by using the accelerometers developed by our group [13, 41, 42]. The electronic noise has different components including front-end amplifier noise, kT/C, mass residual motion, sensor charge referencing voltage and clock jitter. Some of these noise sources are effective in open-loop operation, whereas the others are critical in closed-loop mode of operation.

Table 8 presents some of the individual noise components, their expressions and values for different parameters. As the table shows, most of the electrical noise sources mainly depend on sampling frequency and the value of integration capacitance. Figure 42 shows the dependence of total electronics noise on integration capacitance and sampling frequency. According to simulations, it is possible to improve the overall system resolution down to hundreds of nano-g level while achieving a high dynamic range, by operating the circuit at 1MHz sampling clock with a 15pF integration capacitance. However, operating the system under this condition requires a high performance front-end circuit capable of driving high capacitive loads with a high slew rate and low-noise. Based on these preliminary noise analysis results, we have redesigned our interface circuit such that it can operate at higher frequencies with an increased integration capacitance resulting in a better noise performance.

Table 8: Electrical noise components and their values for different sampling frequencies and integration capacitances.

Noise Source	Expression	fs=100kHz Cint=5pF	fs=1MHz Cint=5pF	fs=1MHz Cint=15pF
Front-end amplifier	$\sqrt{\frac{16}{3}\frac{C_S+C_P}{C_{\text{int}}}\frac{kT}{C_{out}}\frac{1}{f_s}}$	0.66μV/√Hz	0.21μV/√Hz	0.12μV/√Hz
kT/C	$\sqrt{\frac{4kT}{f_s C_{\text{int}}}}$	0.18μV/√Hz	0.06μV/√Hz	0.03μV/√Hz
Sensor Charging Reference Voltage	$\sqrt{\frac{2V_n^2 C_S}{f_s R_{sw} C_{\text{int}}^2}}$	0.89μV/√Hz	0.28μV/√Hz	0.16μV/√Hz
Quantization	$n_{rms} = e_{rms}\frac{\pi^2}{\sqrt{5}M^{2.5}}$	0.08μV/√Hz	0.0025μV/√Hz	0.0025μV/√Hz

*C_s+C_p=100pF,C_{out}=10pF, V_n^2 is the charging reference voltage noise assumed to be white with a spectral density of 10nV/√Hz, C_s=10pF

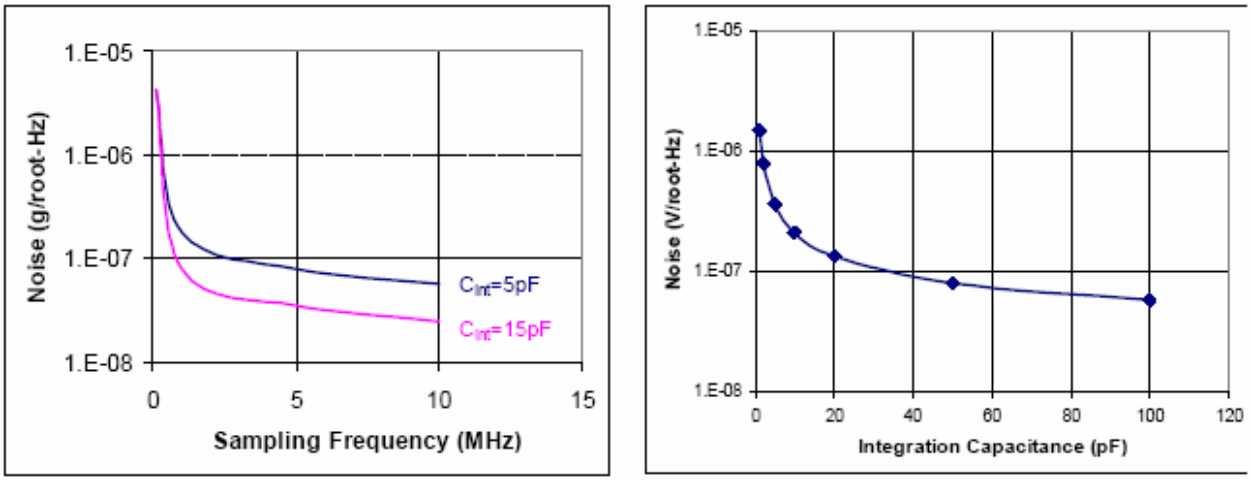


Figure 42: Total system noise for different sampling frequencies and integration capacitances.

Figure 43 shows the simplified block diagram and die photograph of the second generation chip. Each sub-component of the interface chip has been redesigned optimally to minimize the overall circuit noise and to operate the circuit at higher sampling frequency. This circuit is designed in AMI 0.5μm three-metal two-poly n-well process.

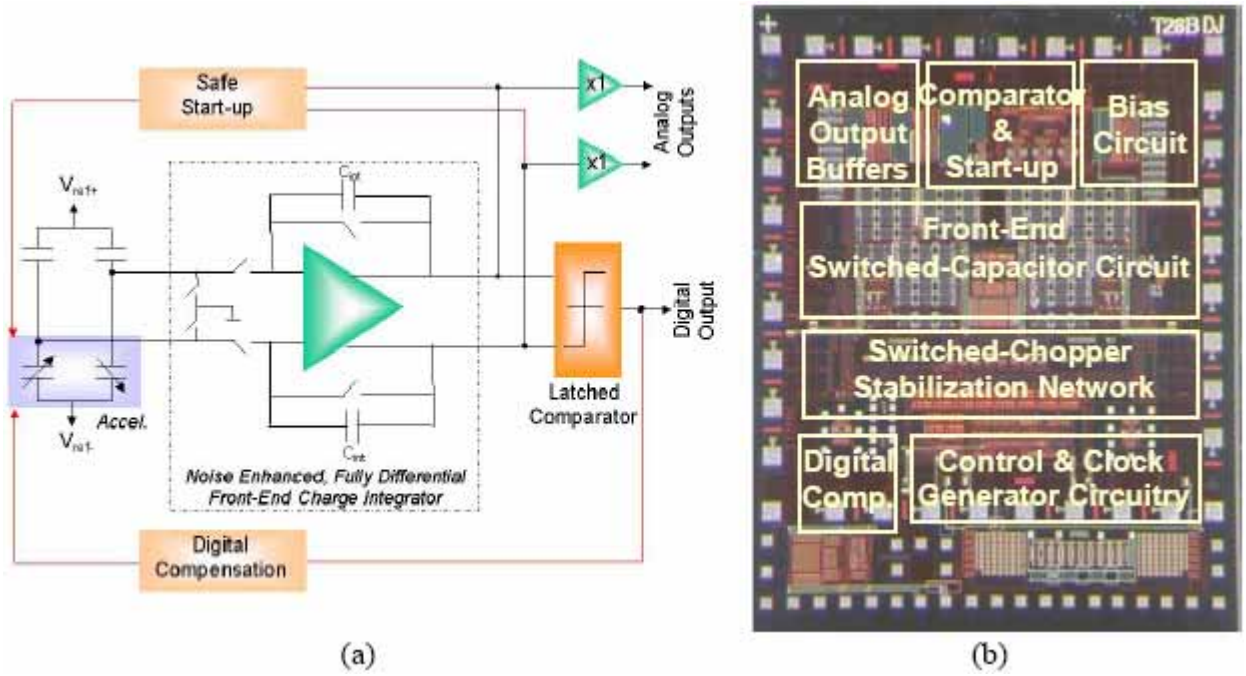


Figure 43: (a) Simplified block diagram of the new interface electronics. (b) Die photograph

To summarize the performance parameters, this second generation interface electronics operates from 1MHz clock and provides an adjustable sensitivity between 0.2 and 1.2V/pF with a dynamic range better than 120dB. It can resolve capacitance differences smaller than 15aF, which means that by using this IC in conjunction with an all-silicon accelerometer with 38.8pF/g differential capacitance sensitivity, an equivalent resolution of 0.5μg/√Hz can be achieved without any need for vacuum or other special packaging. This chip dissipates less than 7.2mW from a single 5V supply, and occupies an area of 1.8x1.9mm^2 in 0.5μm process. Table 9 summarizes the performance parameters of the designed circuit and compares its performance with the previous circuit.

Table 9: Performance parameters of the new interface electronics chip

Parameter	1st Generation	2nd Generation
Size	2.4x2.6mm^2	1.8x1.9mm^2
Sampling Clock	200kHz	~1MHz
Power Dissipation	< 6.6mW	<7.2mW
Capacitance Sensitivity	0.3-1.1V/pF	0.2-1.2V/pF
C_{int} (laser trimmable)	4-15pF	4-20pF
Minimum Resolvable Capacitance Difference	<75aF	<15aF
Dynamic range	95dB	>120dB

1.4.4 Multi-Step Sigma-Delta Interface Chip

Besides improving the hybrid sub-system performance by second generation interface chip, we have developed a new readout technique, called multi-step electromechanical sigma-delta modulator. This technique is based on using a two-element multi-step sensor array similar to a multi-step data converter. Basically the first element does coarse measurement, its output is deducted from the input of the second element and the second element performs a fine measurement on the smaller differential input. Multi-step architecture provides high signal-to-noise ratio (SNR) and improves the dynamic range. Clearly this approach requires higher complexity of external electronics; however it is still more cost effective than using a large number of high-precision sensor elements.

Figure 44 shows the block diagram of the proposed multi-step sigma-delta closed-loop accelerometer array obtained by controlling the stage feedback gain. For an electromechanical sigma-delta modulator, the system configuration remains the same except for the sensor block which is embedded in the loop.

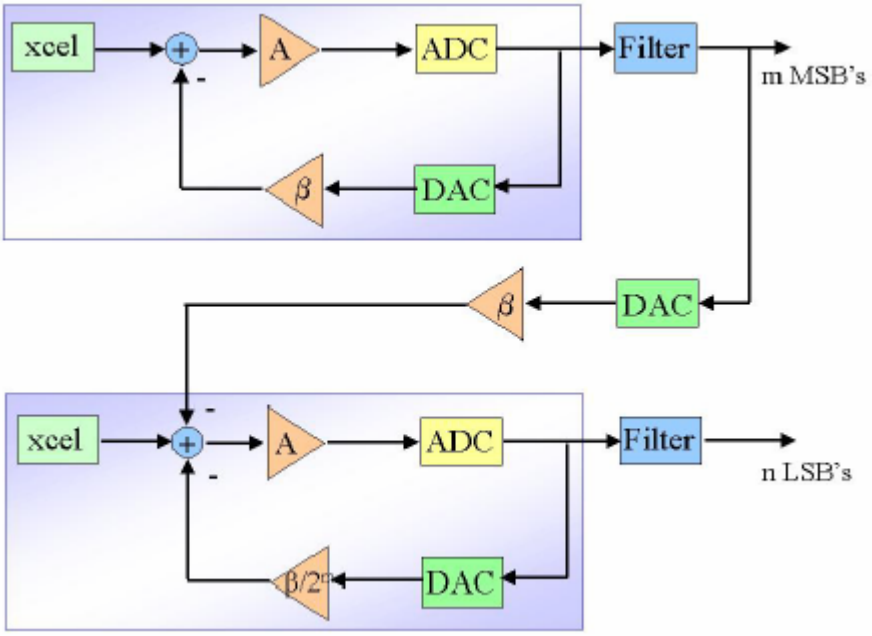


Figure 44: General block diagram of a multi-step sigma-delta closed-loop accelerometer array obtained by controlling the stage feedback gain.

Each loop in this diagram operates as a regular electromechanical second order sigma-delta modulator together with the sensor. It operates the accelerometer in an oversampled electromechanical sigma-delta modulation loop to read the sensor capacitance variation, force-rebalance the proof-mass, and obtain a direct digital output. In the multi-step operation, there are two sigma-delta loops like this. Figure 45 shows a detailed block diagram of this architecture where multi-electrode accelerometer implementation and different feedback paths are indicated. The first loop makes the coarse measurement. In the second loop, accelerometer has two

different electrode sets. One set is for internal feedback of the fine sigma-delta modulator and the other one for the digital output of the first loop, i.e. the coarse modulator. The ratio of the feedback from the coarse sigma-delta loop to the fine sigma-delta loop plays a critical role for stability and in this design it is chosen as 2:1; but a higher ratio can be used by using a digital compensator to stabilize the loops.

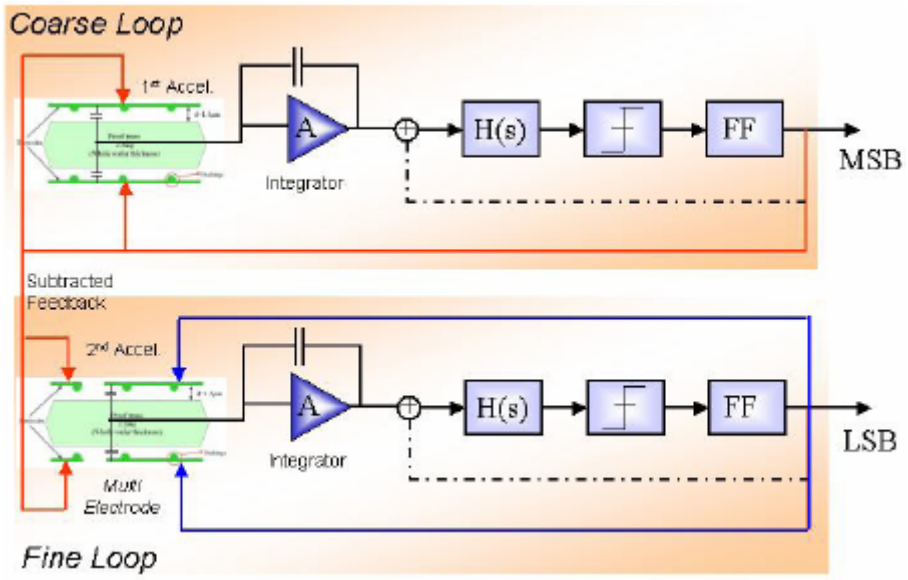


Figure 45: Two accelerometers and the interface circuit block diagram showing the multi-step operation.

The multi-step accelerometer system is nonlinear, mixed-continuous and discrete-time, and consists of both mechanical and electrical parts. This system has been modeled and simulated in time domain using SIMULINK. The mechanical sense element is represented by a second order lumped model while the interface and control circuits are modeled by a combination of continuous/discrete transfer functions, and all the required signal processing operations for the two-bit digital output has been implemented by MATLAB functions.

Electromechanical simulations have been performed to verify stability of the multi-step system with the combination of the lead compensation scheme and the inner electronic feedback loops. Figure 46 shows the complete model for the multi-step converter with the *out-of-plane* accelerometers and sigma-delta control loops. Figure 47 shows the simulation results for the closed-loop operation of both multi-step and conventional second order sigma-delta converter indicating that using a two-element multi-step converter improves the resolution more than two times.

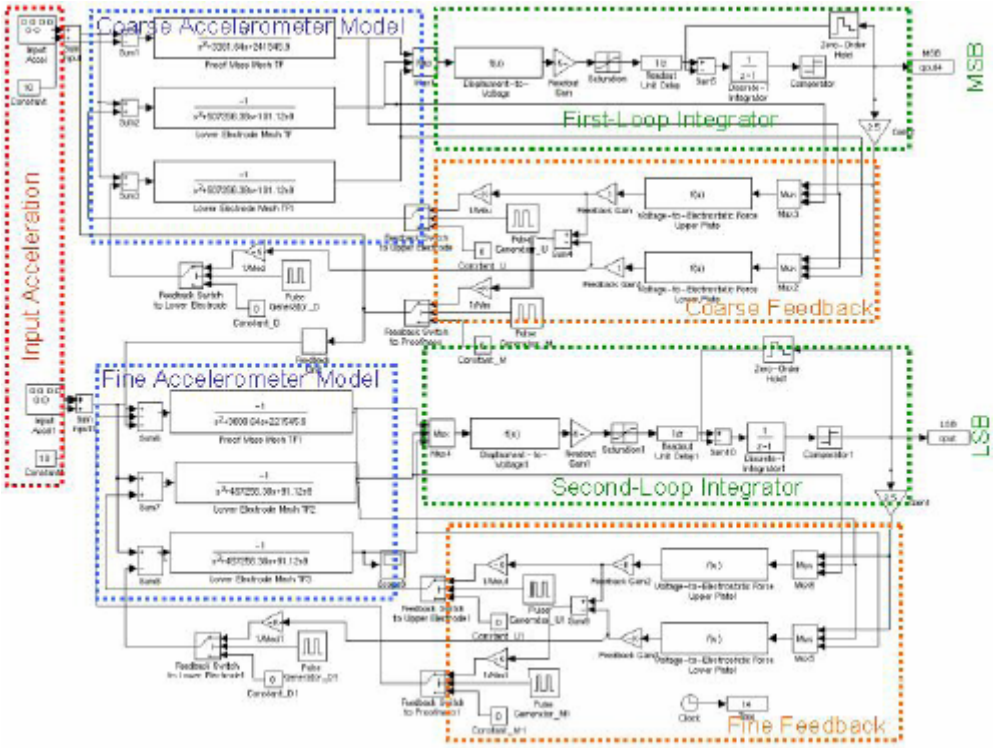


Figure 46: The complete model for the multi-step converter with the *out-of-plane* accelerometers and sigma-delta control loops.

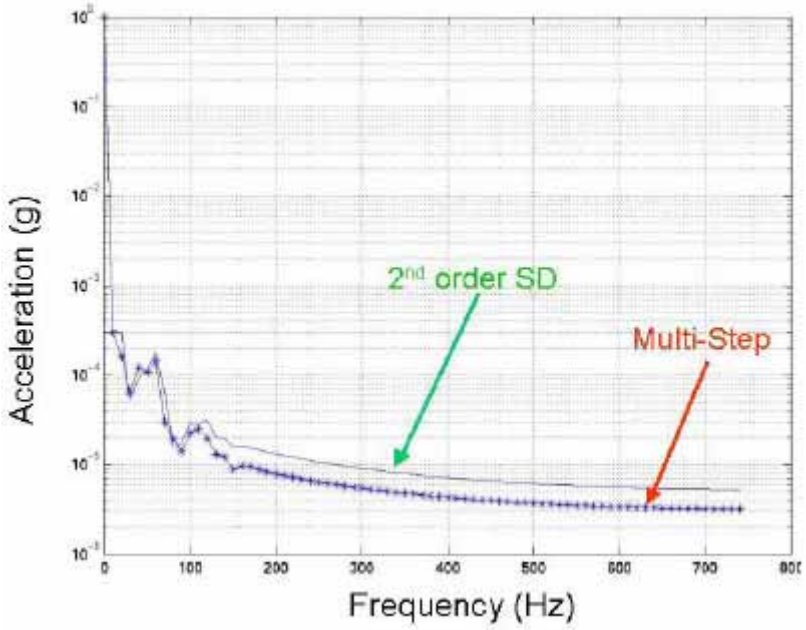


Figure 47: Simulation results for the closed-loop operation of both multi-step and regular 2nd order Σ-Δ converter.

The interface chip has been fabricated in 0.5μm three-metal two-poly n-well CMOS process. Figure 48 shows the die photograph of the fabricated chip. Figure 55 shows the hybrid subsystem employing two *out-of-plane* accelerometers with the interface electronics. The chip is designed as both testable and programmable for different kinds of output loads and power supply levels. Two electronically trimmable capacitor arrays have been implemented in the layout to cancel the offset caused by the difference in the base capacitances of the accelerometers. It has been tested in open-loop and functionality has been verified.

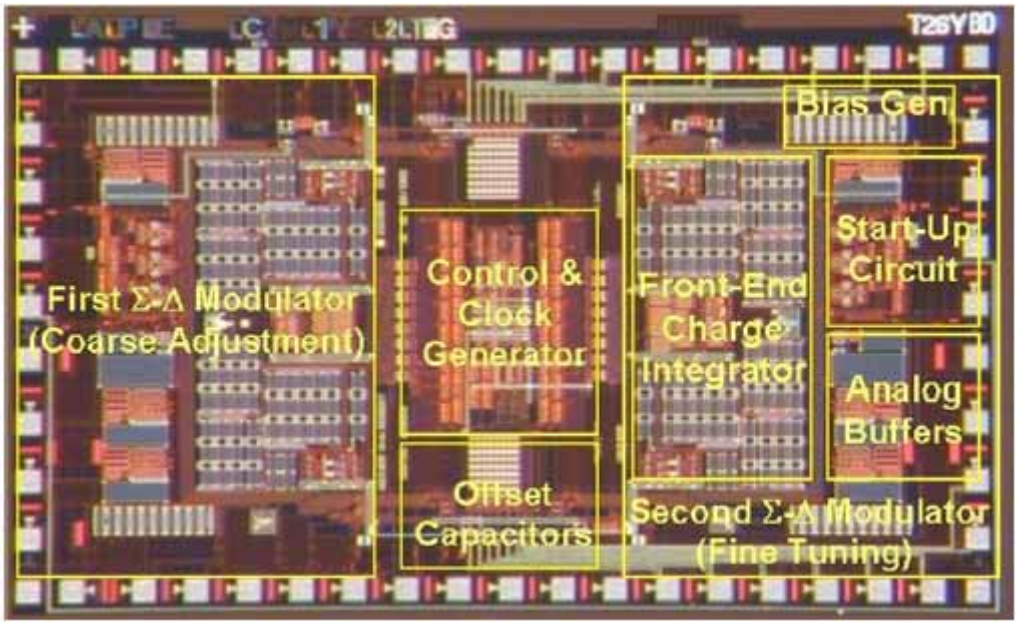


Figure 48: Die micrograph of the fabricated chip.

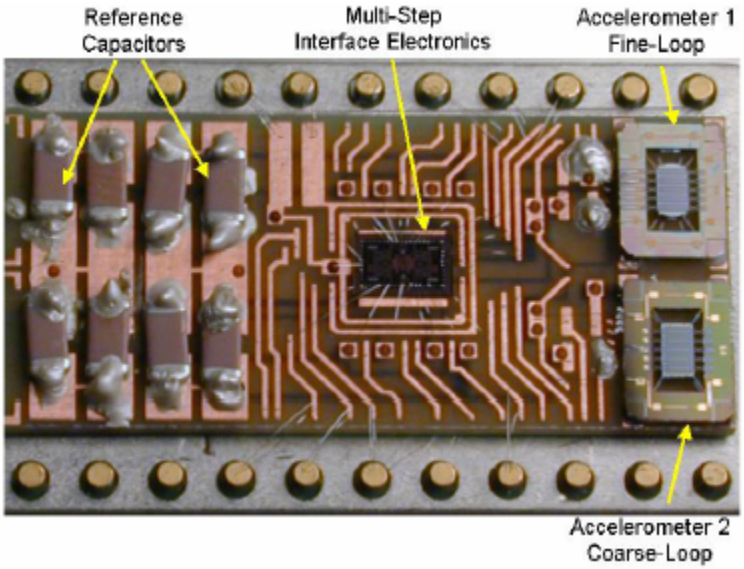


Figure 49: Hybrid system employing the interface electronics with two *out-of-plane* accelerometers.

Table 10 shows the performance parameters for the fabricated chip. Figure 50 shows the noise spectrum for the open-loop analog output for 5pF input capacitance difference showing that the system can resolve better than 20aF in open-loop. This means that by using this IC in conjunction with an all-silicon accelerometer, sub-μg level of equivalent resolution can be achieved without any need for vacuum or other special packaging. This chip dissipates less than 12mW from a single 5V supply, and occupies an area of 1.8x3.1mm^2 in 0.5μm process.

Table 10: Performance parameters for the multi-step interface chip.

Sensor Parameters	
Sensitivity	1.3pF/g (2x1mm^2 bridge)
Mechanical Noise	0.7μg/√Hz
Interface IC Parameters	
Sampling clock	1MHz
Power dissipation	<12mW @ 5V
Capacitance sensitivity	0.2-1.2V/pF (adjustable)
Resolution	<20aF
Sensor and Interface Module	
Sensitivity	0.26-1.6V/g (2x1mm^2 bridge)
Open-loop resolution	<1μg/√Hz (2x1mm^2 bridge)
Full scale range	±1.35g with 5V supply

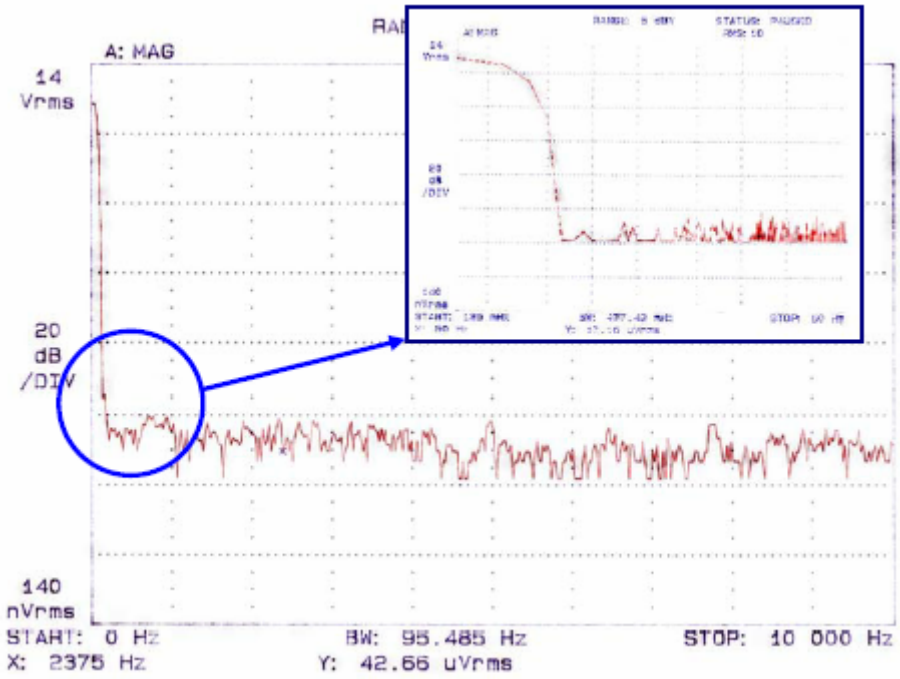


Figure 50: Noise spectrum of the open-loop analog output for 5pF input capacitance difference.

2. Test Results and Discussion

2.1. Out-of-plane Hybrid System

Figure 51 shows the *out-of-plane* hybrid subsystem with the sensor and the circuit assembled onto a PC board and mounted inside a standard DIP package. The sensor and the interface circuit are packaged close to each other to minimize parasitics [14].

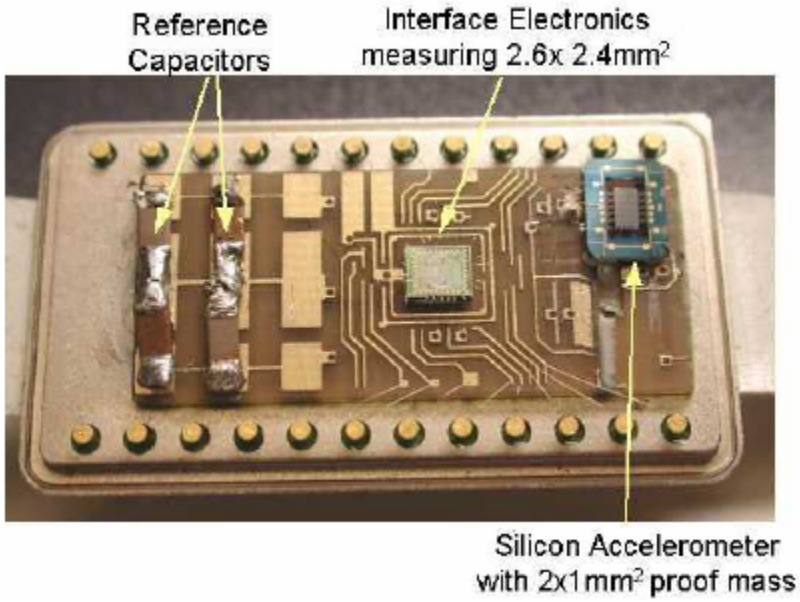


Figure 51: Hybrid packaged *Out-of-plane* accelerometer and the interface chip in a 24-pin IC package.

2.1.1. Open-Loop Tests:

Open-loop tests were performed on a dividing head, in a 1g gravitational field, by changing the acceleration on the sensor from -1g to +1g. While changing the applied acceleration, the differential analog output voltage of the interface electronics was measured. Figure 52 shows a measured open-loop sensitivity of 960mV/g.

The output noise of the hybrid module is measured by using a HP 3561 dynamic signal analyzer with a 50kΩ reference resistor as shown in Figure 53. This figure indicates that the resistor has 32nV/√Hz noise density which matches well with the estimated thermal noise of the resistor (note that the measurement bandwidth is 11.72Hz). Thus, the hybrid module can resolve 1.08μg/√Hz. It has been verified through the tests that the periodic peaks in this plot are due to environmental factors and are not related with the output signal.

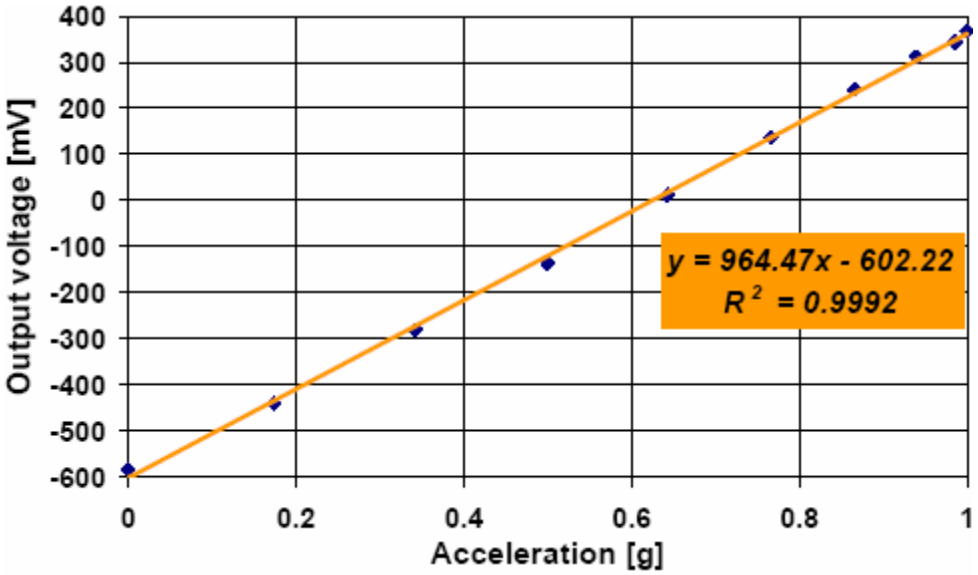


Figure 52: Open-loop sensitivity of the *Out-of-plane* system.

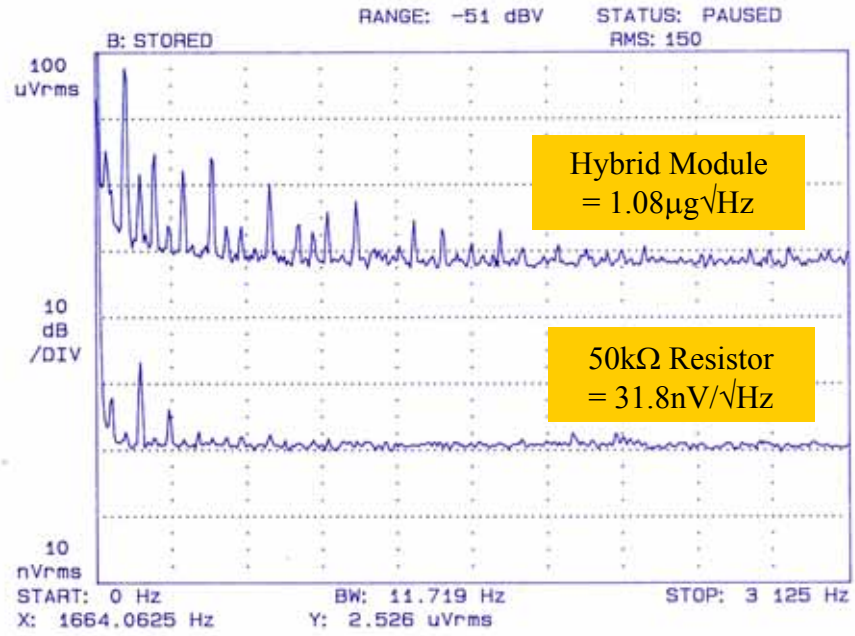


Figure 53: Noise measurement for the hybrid system indicating a resolution of 1.08µg/√Hz.

Figure 54 shows the dependence of the open-loop noise floor on sampling frequency. As shown in the figure, although there is a constant difference between the two curves for all frequencies, the theoretical and measured curves have the same trend and the noise floor decreases with increasing the sampling frequency as expected.

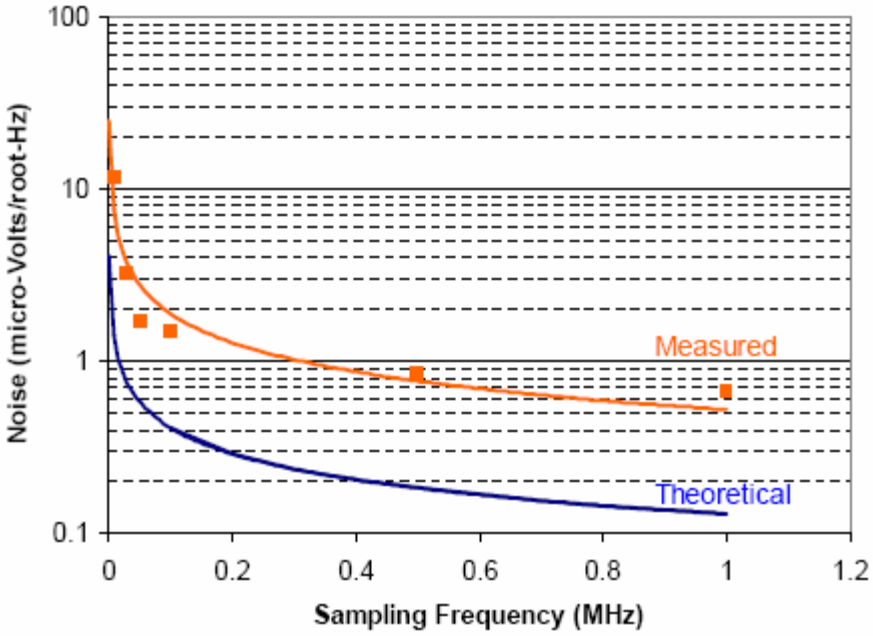
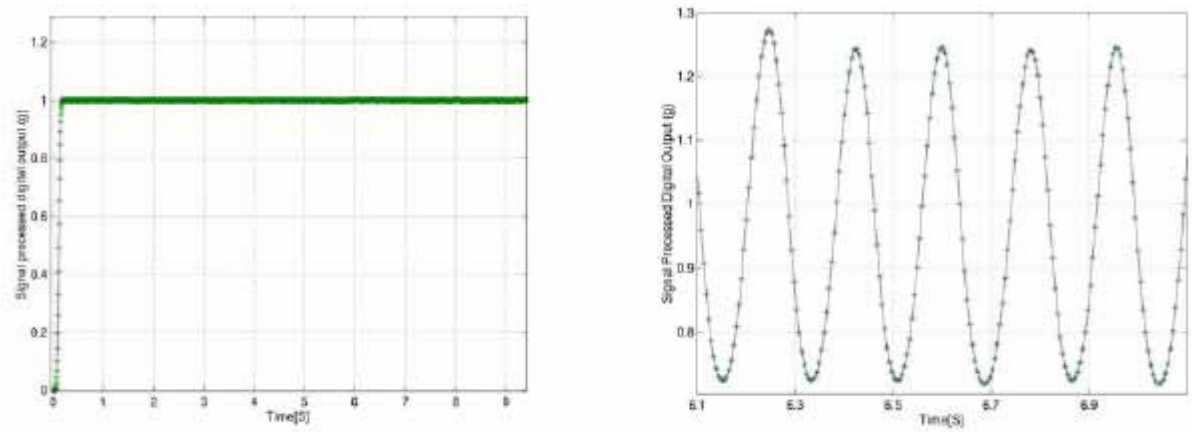


Figure 54: Measured noise levels at different frequencies.

2.1.2. Closed-Loop Tests:

The closed-loop test setup uses a shaker table, a data acquisition board and LABVIEW and MATLAB programs for signal processing. Since the interface electronics uses a high oversampling sigma-delta modulation technique, the PWM output bit stream has to be processed to obtain a useful signal. This is realized by transferring the digital output to a computer by means of a data acquisition board, and processing the signal (decimating and digital filtering). A $sinc^3$ filter, FIR filter, decimator and D/A converter have been implemented in MATLAB for this purpose.

The entire system has been operated in closed-loop and the functionality of the system has been verified through extensive tests. Figure 55 shows the decimated PWM digital outputs for (a) pure 1g DC input and (b) 0.25g sinusoidal input acceleration on top of a 1g DC. As the figure shows, the applied input acceleration is recovered successfully. Note that in Figure 55 (a), the only applied acceleration is the 1g gravitational field. The output voltage is constant, except for variations due to noise generated in the system and/or picked up from the environment.



(a) (b)

Figure 55: Closed-loop measurement results for the hybrid sensor system: (a) for 1g DC input acceleration, (b) for 0.25g sinusoidal input acceleration on top of 1g DC input.

Figure 56 shows the Fourier transform of the signal processed PWM output for 1g DC bias for sampling frequencies of 100 kHz and 400 kHz. As the figure shows, by increasing the sampling frequency four times, the noise floor decreases by approximately 16 times. This means that the noise is inversely proportional to f_s^2, and hence the mass residual motion is dominant. It has been observed that this noise source is not effective anymore for higher sampling frequencies. Moreover, as the span of the measurement increased beyond 15 Hz, the undesired peaks become insignificant and the noise level stays constant at higher frequencies.

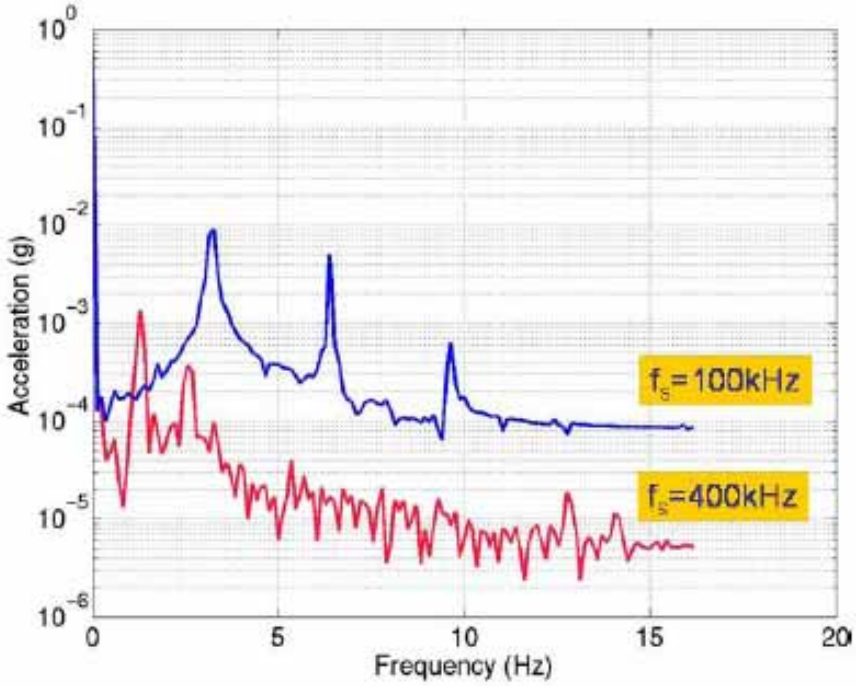


Figure 56: Measured noise spectrum for closed-loop operation under 1g DC bias.

These results indicate that at sampling frequencies lower than 400 kHz, the mass residual motion is the dominant noise source in closed-loop mode of operation. As the sampling frequency is increased more than 400 kHz, this noise source becomes insignificant compared to others and the overall noise is improved by the square root of the sampling frequency. The system can resolve better than 10µg in closed-loop mode for a sampling frequency of 400 kHz. Table 11 summarizes the measured system parameters.

Table 11: Performance parameters of the hybrid system.

CMOS readout electronics	
Sensitivity	0.2-1.2V/pF
Dynamic Range	>120dB
Resolution	<15aF
MEMS accelerometers	
Sensitivity [pF/g]	4.9
Mech. Noise [µg/√Hz]	0.7
MEMS device and interface circuit module	
Sensitivity [V/g]	0.96
Open-Loop Noise Floor [µg/√Hz]	1.08
Closed-Loop Noise Floor [µg/√Hz]	<10

2.2. SOG In-plane Hybrid System

Test setup and the testing procedure are identical for the *in-plane* and 3-Axis accelerometers. Figure 57 shows the block diagram of the CMOS capacitive interface chip and its hybrid connection to the sensor. Figure 58 shows the hybrid system assembled onto a PC board and mounted in a standard 24-pin IC package. The sensor and the interface circuit are packaged close to each other to minimize the parasitics. Note that the sensor die includes several devices and only one is connected to the readout circuit.

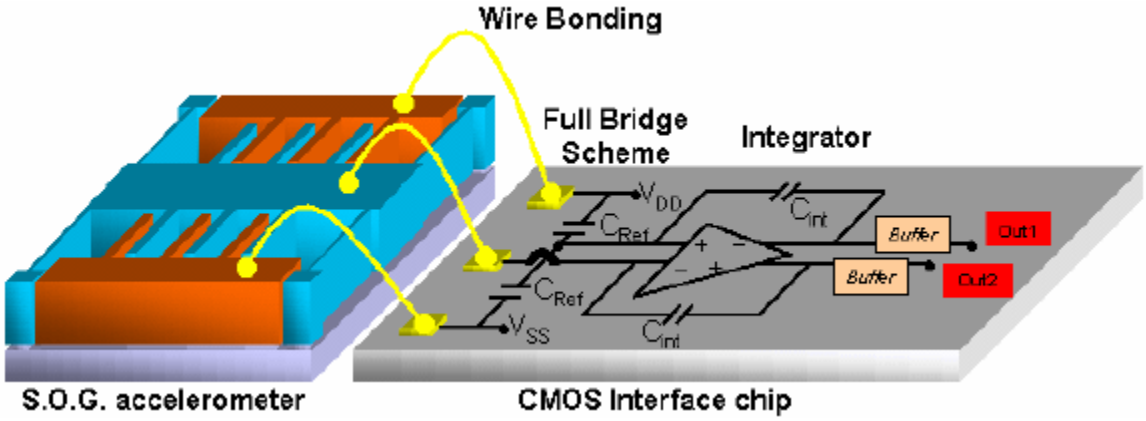


Figure 57: Hybrid accelerometer/circuit system.

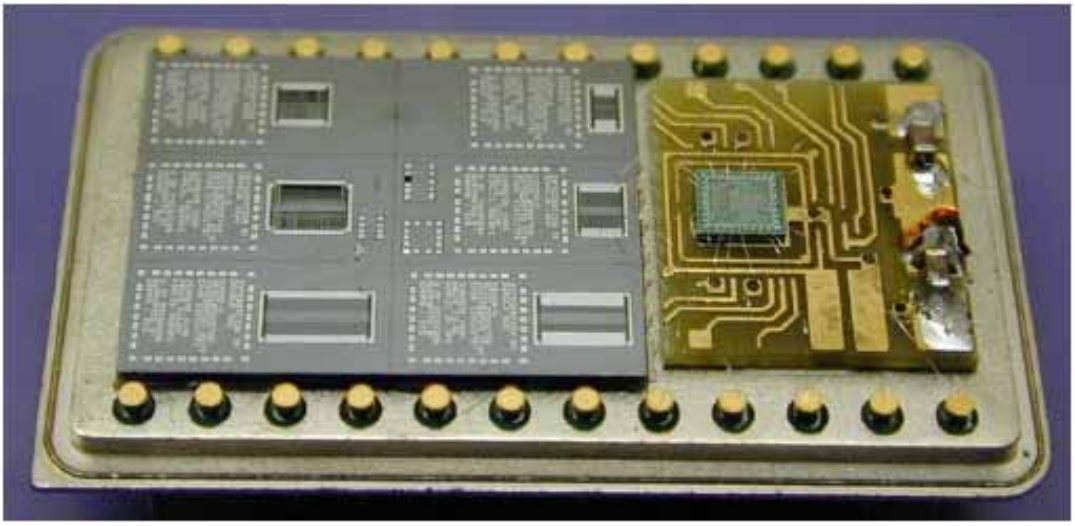


Figure 58: Hybrid system in IC package.

The hybrid system has been tested for sensitivity and resolution in open-loop configuration. The open-loop tests have been performed on a dividing head, in a 1g gravitational field, by changing the acceleration on the sensor from -1g to +1g. The sensor has a measured open-loop sensitivity of ~140fF/g, which is lower than expected because of the larger sensing gap distance (3.2μm) than designed (2.0μm). Figure 59 shows the open-loop test results for the hybrid system with respect to acceleration indicating a sensitivity of ~40mV/g. This result matches with the expected value since the readout circuit itself has a voltage gain of 330mV/pF. Noise floor of the system is measured using a dynamic signal analyzer HP3561. Figure 60 shows the measured output noise spectrum of the complete module with a dc input of 1g showing a noise floor better than 100μg/√Hz.

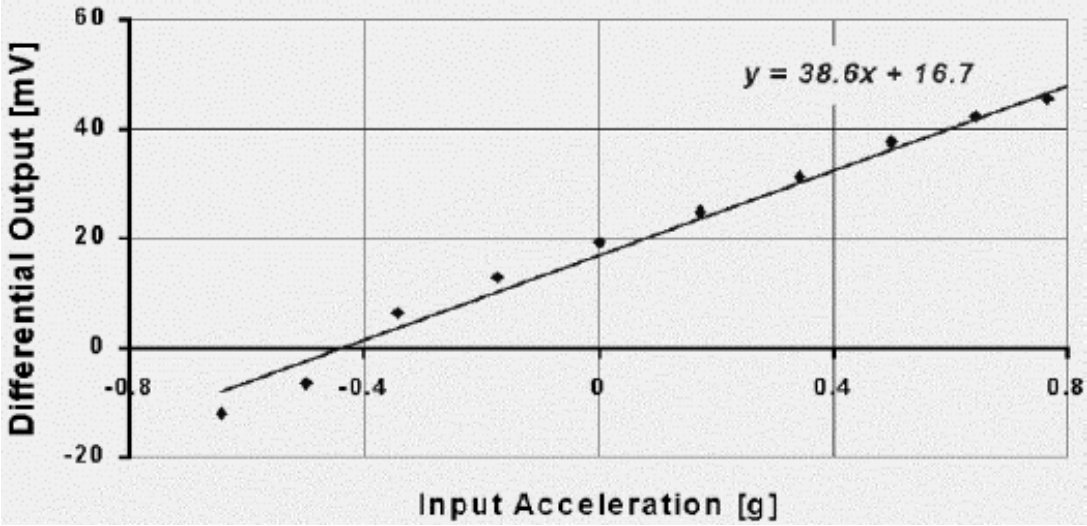


Figure 59: Open-loop test result of the hybrid system.

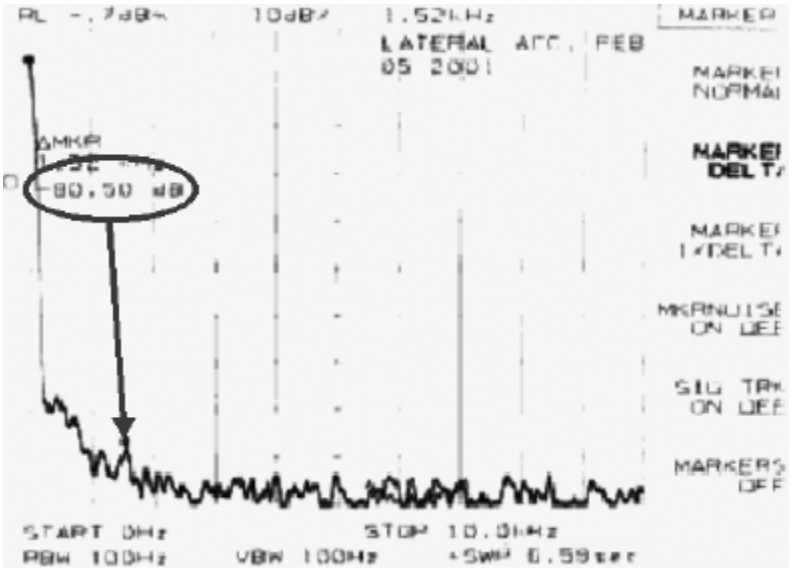


Figure 60: Output spectrum of the sensor/circuit module.

2.3. SOG In-plane Monolithic System

The threshold voltages of nMOS and pMOS transistors were measured to be 0.74V, 0.49V, respectively (Figure 61). Obviously, the positive pMOS threshold voltage is not what was expected, and results in malfunction of the entire readout circuit. We do not know why the pMOS transistor's threshold voltage was off target, but nMOS was right on target. This is likely due to some contamination or a problem in ion implantation.

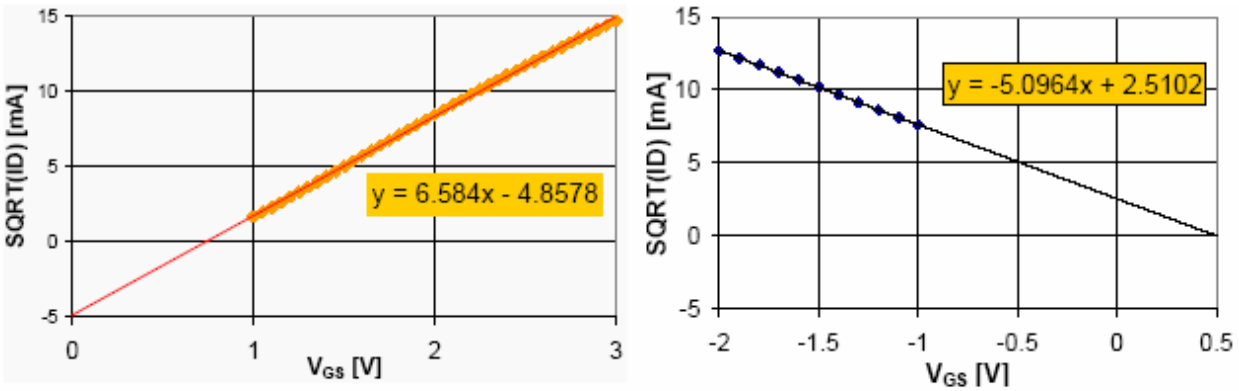
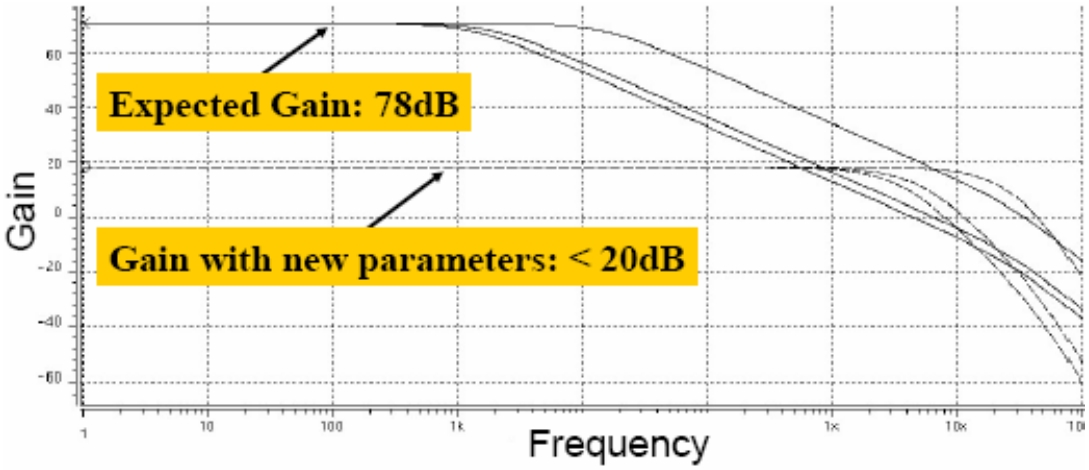


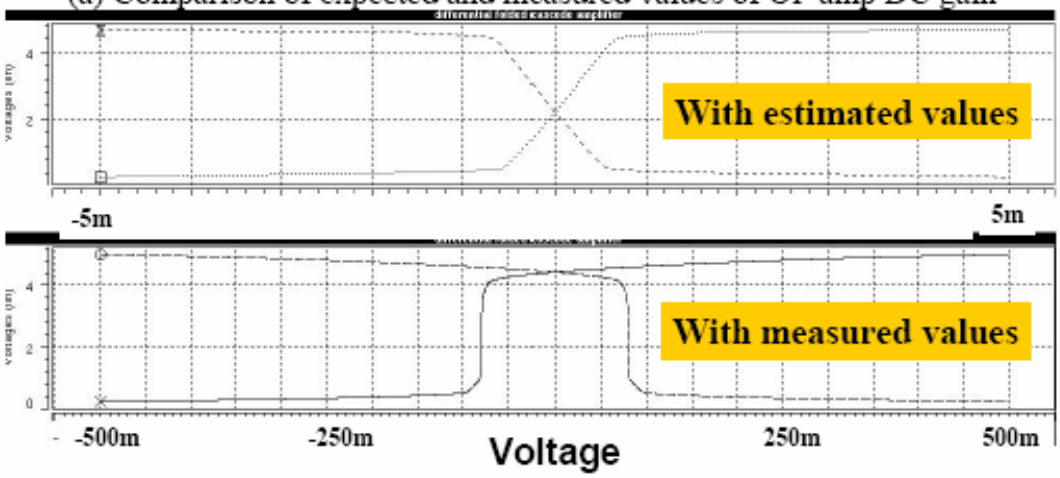
Figure 61: Transistor V_{GS} vs. I_D characteristics

Main circuit blocks of the interface chip have been re-simulated with the positive pMOS threshold voltage. Figure 62 show the comparison of fully-differential operational amplifier simulation results with expected and measured parameters. As shown in Figure 62 (a), amplifier DC gain is decreased from 78dB to 18dB. Also the amplifier offset voltage is calculated to be

more than 100mV according to Figure 62 (b). Operational amplifier and the switched-capacitor circuit are the most critical parts of the whole circuit. It is obvious that with the positive pMOS threshold voltage, none of them operates correctly.



(a) Comparison of expected and measured values of OP amp DC gain



(b) DC characteristics of OP amp with positive pMOS threshold voltage

Figure 62: Performance comparisons of OP amp with estimated and measured transistor characteristics.

Although MEMS devices integrated with CMOS circuit were not realized successfully, the basic elements of the integrated process have been successfully demonstrated. It has been shown that a standard CMOS wafer can be bonded to glass, polished back, and Deep RIE etched to form MEMS. The dielectric bridge enables the operation of the circuits and MEMS, and it has been shown that the dielectric bridge can be successfully fabricated. The problem associated with the threshold voltage of pMOS transistors can be overcome by using standard CMOS wafers from a foundry.

2.4. All-Silicon In-plane Hybrid System

Figure 63 shows the CMOS capacitive interface chip and its hybrid connection to the accelerometer. Two fixed external reference capacitors are used to establish a full-bridge scheme. By using the interface circuit, the hybrid module provides overall sensitivity of 0.49V/g. The hybrid module can resolve 1.6μg/√Hz as shown in Figure 64. Table 12 summarizes the measured specifications of the accelerometer, the interface circuit, and the hybrid module.

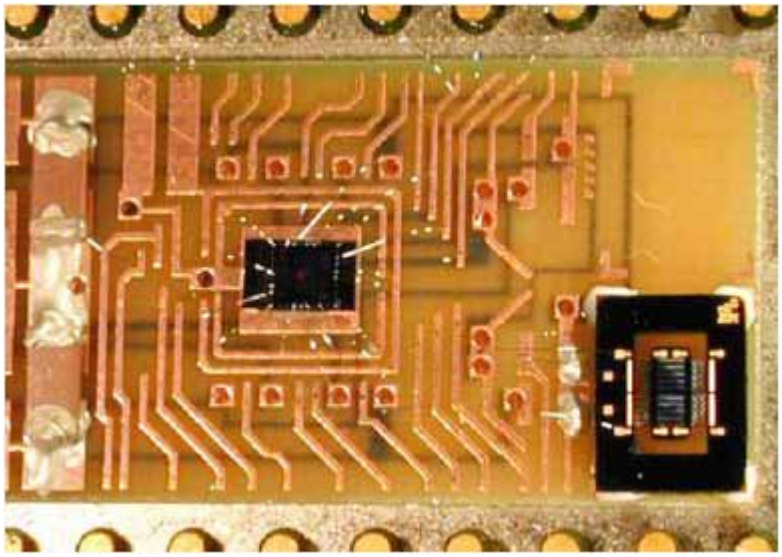


Figure 63: Hybrid accelerometer and readout circuit module.

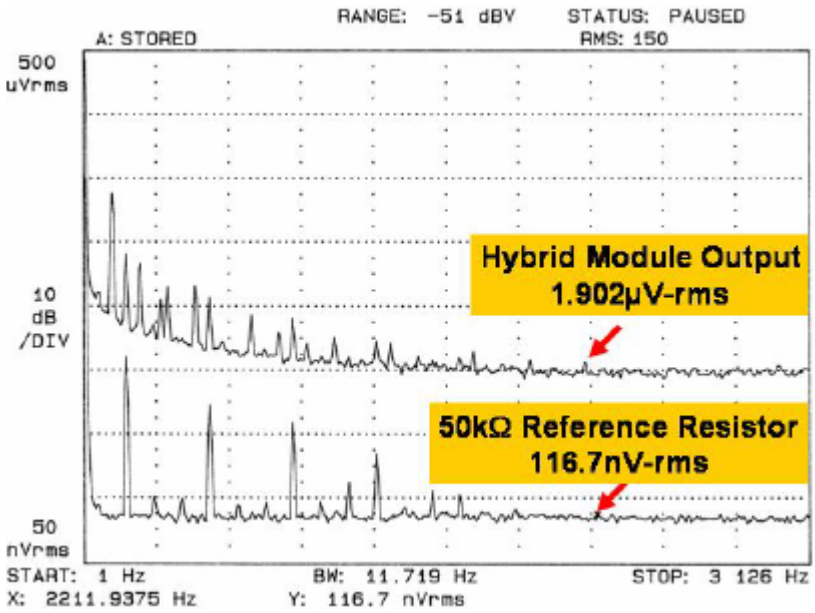


Figure 64: Output noise floor.

Table 12. Measured hybrid module specifications

Micro-accelerometer	
Spring constant	17.1N/m
Sensitivity	5.6pF/g
Interface CMOS circuit	
Clock frequency	500kHz
Dynamic range	120dB
MEMS device and interface circuit module	
Sensitivity	0.49V/g
Total noise floor	1.6μg/√Hz

2.5. 3-Axis Accelerometer System

The 3-axis chip has been fully tested electrostatically and mechanically on a precision turn table with all of its readout electronics. Figure 65 shows measured differential capacitance vs. input acceleration. In the range of ±0.3g, the 3-axis chip provides sensitivity of 8.0, 7.9, 4.9pF/g for X, Y, Z, respectively, with a small offset and excellent linearity. Note that *in-plane* devices have smaller offset (0.09pF) than *out-of-plane* device (0.2pF). The offset for *out-of-plane* device ($|\Delta C_{Top} - \Delta C_{Bottom}|$ at zero acceleration) is due to gap variation on top and bottom of the wafer. However, the offset for *in-plane* devices ($|\Delta C_{Right} - \Delta C_{Left}|$ at zero acceleration) is more immune to fabrication variation.

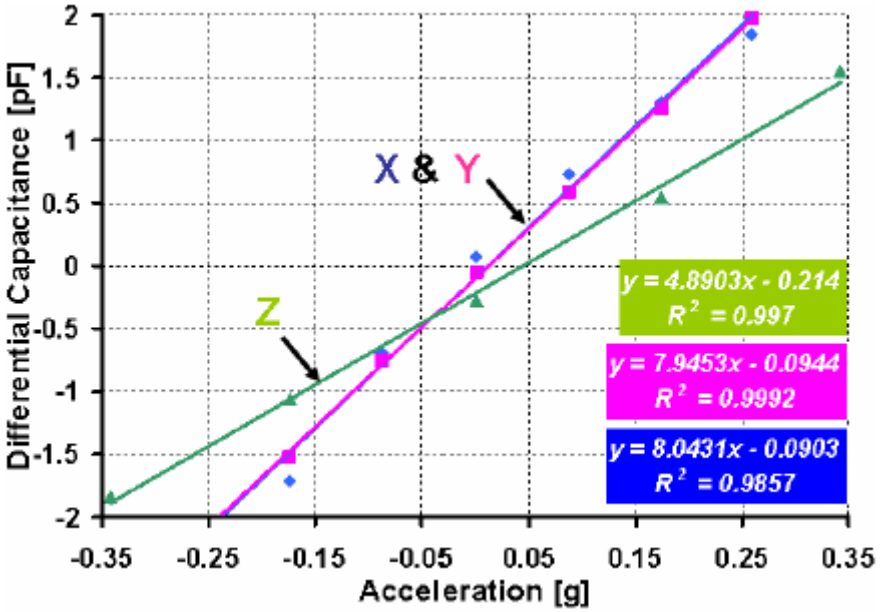


Figure 65: Measured capacitance change according to input acceleration.

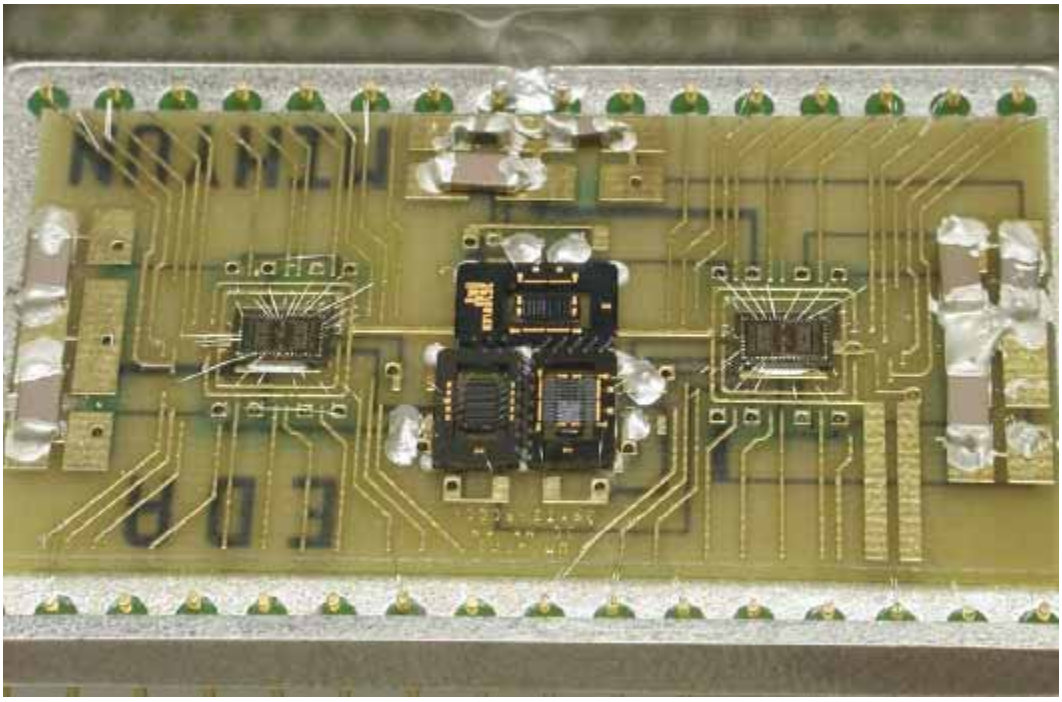


Figure 66: Hybrid module in a DIP package.

Figure 66 shows a hybrid 3-axis accelerometer with two CMOS Σ-Δ readout circuits in a DIP package. Each readout circuit contains two Σ-Δ readout circuits and external reference capacitors are used to establish a full-bridge scheme. The size of the entire package is $3x4.5x1cm^3$.

In-plane and *out-of-plane* accelerometers combined with readout circuit provide system gain of 0.49V/g and 0.96V/g, respectively. The hybrid module can resolve 5.5μg-rms (*in-plane*) and 3.7μg-rms (*out-of-plane*) with a 11.7Hz BW, which provides 1.60μg/√Hz and 1.08μg/√Hz noise spectral density for the *in-plane* and *out-of-plane* devices, respectively. It has been observed that there are some variations in system gain for different devices. Table 13 summarizes the measured specifications of the 3-axis accelerometer, the interface circuit, and the hybrid module.

The drift of the accelerometer is determined primarily by the package and assembly. Therefore, to determine the true stability of the device, the packaging scheme needs to be optimized. The packaging scheme of the current system is not optimum. Nevertheless, the temperature and drift characteristics of this system have been tested in an environmental chamber ESPEC-SU240. Figure 67 shows rest capacitances that were recorded by using a HP-4284A precision LCR meter every 1 minute for 1 hour at 25, 50, and 80°C. The temperature Coefficient of Offset (TCO) is obtained as 70ppm/°C up to 50°C and 500ppm/°C up to 80°C. This is mainly caused by the mismatch of Coefficient of Thermal Expansion (CTE) of the device and its packaging. The device is mounted on the PCB by non-conductive epoxy. CTE of the materials used for the device itself such as silicon, polysilicon, silicon nitride are 2.4-2.9ppm/°C, while PCB and non-conductive epoxy have CTE of 20-25ppm/°C and 40-60ppm/°C, respectively [43-45]. This

indicates that packaging and assembly techniques are major limiting factors. Thus, improved packaging and assembly techniques are expected to significantly reduce TCO. The drift of the accelerometer is measured to be ~400ppm for 1 hour.

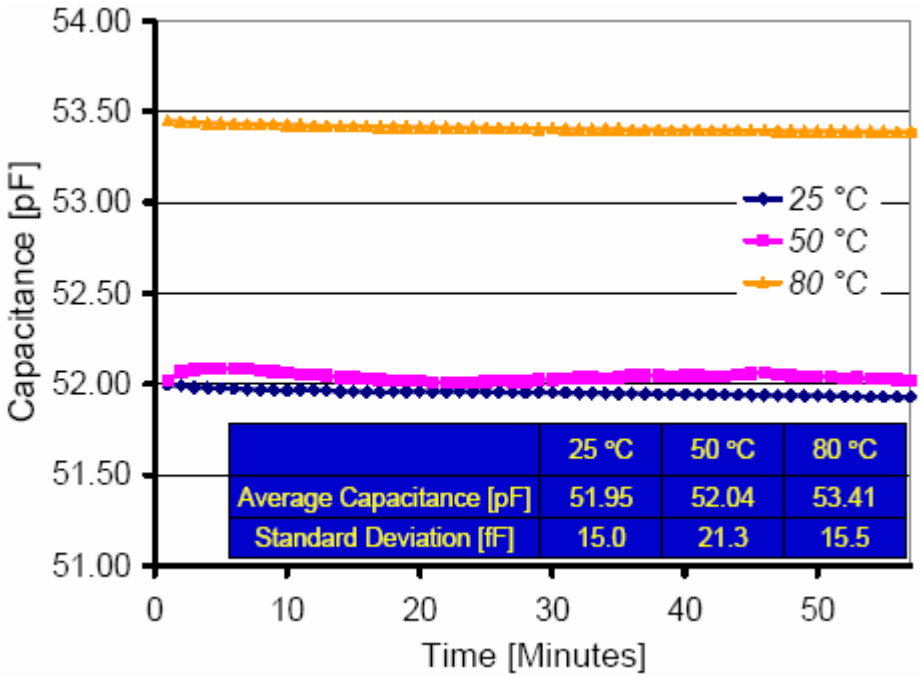


Figure 67: Temperature and Drift characteristics show TCO of 500ppm/°C up to 80°C and drift of ~400ppm for 1 hour.

Table 13: Measured 3-axis accelerometer system specifications.

CMOS Readout Electronics			
Sensitivity	0.2V/pF		
Electronic Noise	790nV/√Hz		
3-Axis Single-Chip Accelerometer			
	X	Y	Z
Sensitivity [pF/g]	8.0	7.9	4.9
Mech. Noise [µg/√Hz]	0.7*	0.7*	0.7*
MEMS Device and Interface Circuit Module			
Sensitivity [V/g]	0.49	0.49	0.96
Noise floor [µg/√Hz]	1.60	1.60	1.08

* denotes estimated

3. Performance Improvement and Discussion

The performance of micromachined accelerometers has been dramatically improved since the first micro-accelerometer was introduced. Figure 68 shows noise performance comparison chart for *in-plane* and *out-of-plane* micromachined accelerometers reported in the literature in the last 20 years. Most of the reported high performance devices are sensitive to *out-of-plane* acceleration since it is easier to fabricate large proof-mass and large-area electrodes along the z-axis. Note that the noise floor in the figure indicates not mechanical noise only, but accelerometer system noise.

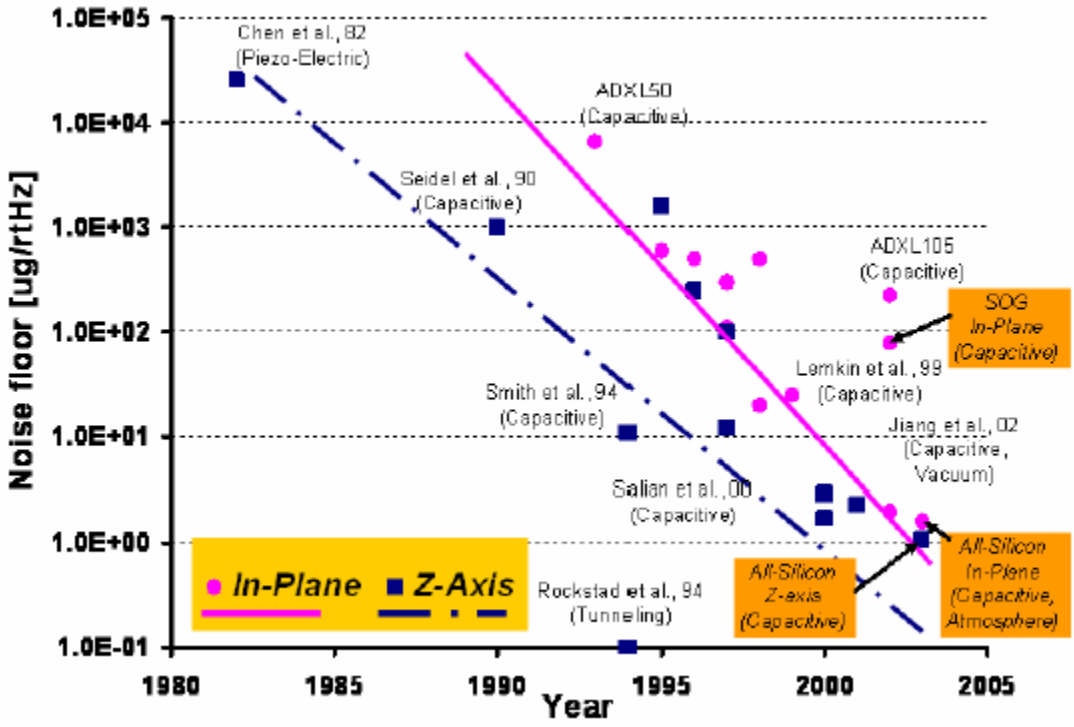


Figure 68: Performance improvements for micromachined accelerometers

Silicon capacitive accelerometers reported in this here need further testing to determine temperature sensitivity, bias stability, scale factor stability, and long term drift. In order to achieve sub-micro-g resolution with >120dB dynamic range, an accelerometer with sub-µm sensing gap, larger sensing area and extremely low-noise interface readout circuit is required. Packaging is a big challenge to achieving further performance improvement. This needs to be improved to achieve not only nano-g resolution but also low temperature sensitivity, low drift, and long-term bias stability.

Further research is required to improve the accelerometer system noise performance down to nano-g range, which is required for some applications such as space navigation and seismology. The system presented here is capable of resolving sub-micro-g performance and it can resolve better than this if it is operated in vacuum environment. However as the noise floor is decreased

to sub-micro-g levels, it is getting difficult to measure the accelerometer performance accurately. Therefore, better testing methods have to be developed for accurate measurements. Especially for vacuum operation of the system, packaging and the test setup should be improved accordingly.

As electronic noise approaches sub-μg/√Hz, the mechanical noise of the accelerometer will begin to dominate over the electronic noise. Vacuum packaging might be necessary to lower the overall mechanical noise to sub-μg/√Hz. However, the stability of operation in a vacuum environment should be carefully considered for closed-loop operation. In order to ensure stability in vacuum environment, digital compensation needs to be implemented in the readout circuit.

New readout architectures can be investigated for better overall performance. The multi-step readout technique is presented in this project for the first time, and hence it is required to be analyzed much more in detail to become a mature concept. The digital filters, decimator, and the other digital blocks can be implemented on the same chip with the readout electronics to achieve a single chip, signal-processed output accelerometer system. It is hoped that the work outlined in this project can further the development of high-performance navigational-grade accelerometers.

B. Micromachined Gyroscopes

1. Motivation

This task aims at developing single-axis, high performance “tactical and inertial grade” micromachined gyroscopes which can provide degree-per-hour resolution and bias stability, and very high scale factor accuracy in a bandwidth of 10 to 100 Hz. While low cost, low power, micromachined "tactical grade" gyroscopes can be extensively used in guidance of tactical weapons, such as short-range missiles, "inertial grade" ones are necessary for applications in submarines, aircraft systems, GPS-aided navigators and other inertial positioning systems [46]. We have developed two types of gyroscopes. One is polysilicon gyroscope utilizing high aspect ratio trench refilled polysilicon structure. The other is single crystal silicon gyroscope utilizing a <111> direction single crystal silicon in order to obtain high resolution, high sensitivity, and good temperature performance.

2. Polysilicon Gyroscope

Figure 69 shows the ring gyroscope structure. The device is a resonating structure, for which the vibration space can be spanned into two identical flexural modes, separated from each other by 45 degrees. The structure is electrostatically driven in its flexural frequency at one mode, while the capacitive change at the other mode is ideally zero. In case of a rotation of the body around its axis, there will be a capacitive change at the other mode because of the Coriolis force, which will behave like a current generator. The generated current is read to obtain the rotation information.

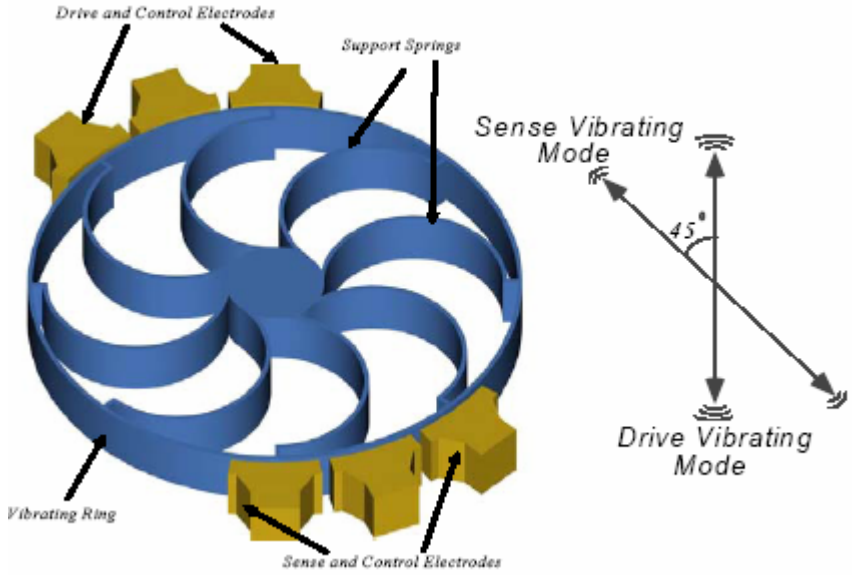


Figure 69: Ring gyroscope and flexural modes.

The gyroscope under development is a high-aspect ratio polysilicon vibrating ring gyro realized by trench refill technology. While the high aspect ratio polysilicon micromachining technology is capable of producing polysilicon ring and sense electrode that have thickness of 70-80µm, it suffers from a few limitations and gyroscopes fabricated using the technology will have difficulty producing degree per hour performance. One constraint is the size of the capacitive gaps between the ring and sense electrode. In the high aspect ratio polysilicon micromachining technology, this gap is limited by the thickness of the sacrificial oxide layer, which is typically less than 2µm. However, the next generation of high performance micromachining gyroscopes require large vibration amplitude (>2µm) to improve performance of device. This requires a technology which can produce capacitive gaps of larger than 2µm. Another constraint is the thickness of the structure. High performance gyroscopes requires large mass, hence trench depth should be made as deep as possible. However, for thick trenches with depth greater than 100µm, the blanket etch used in the high aspect ratio polysilicon micromachining process will cause excessive etching of the side wall polysilicon at the top of the trench which makes subsequent lithographic steps difficult. Finally, the high aspect ratio polysilicon micromachining process requires etching of trenches with different mask opening. Due to RIE lag, trenches with different thickness are formed, which is not desirable for device fabrication.

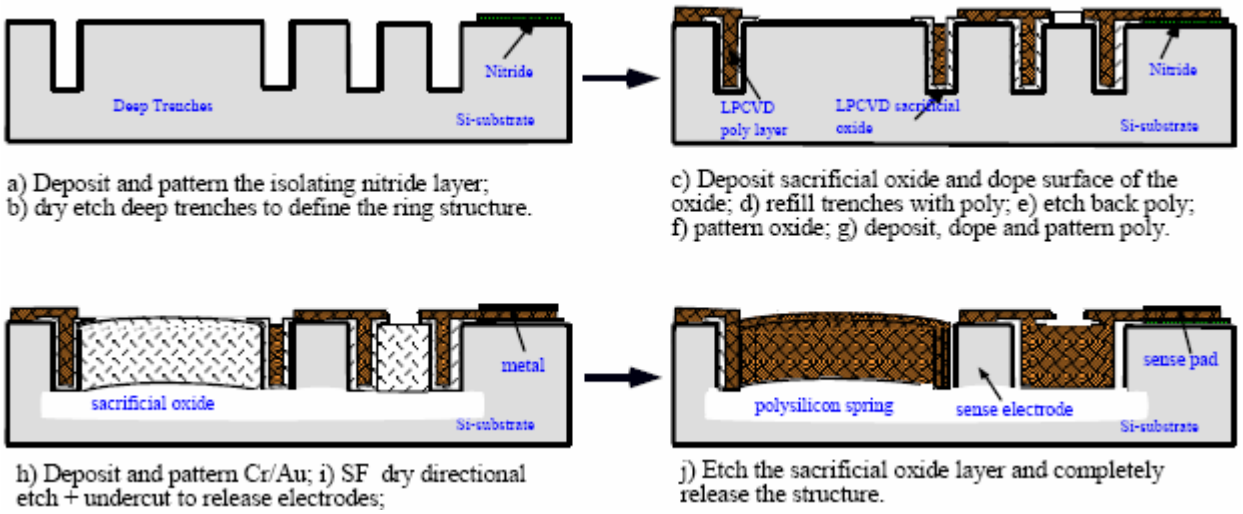
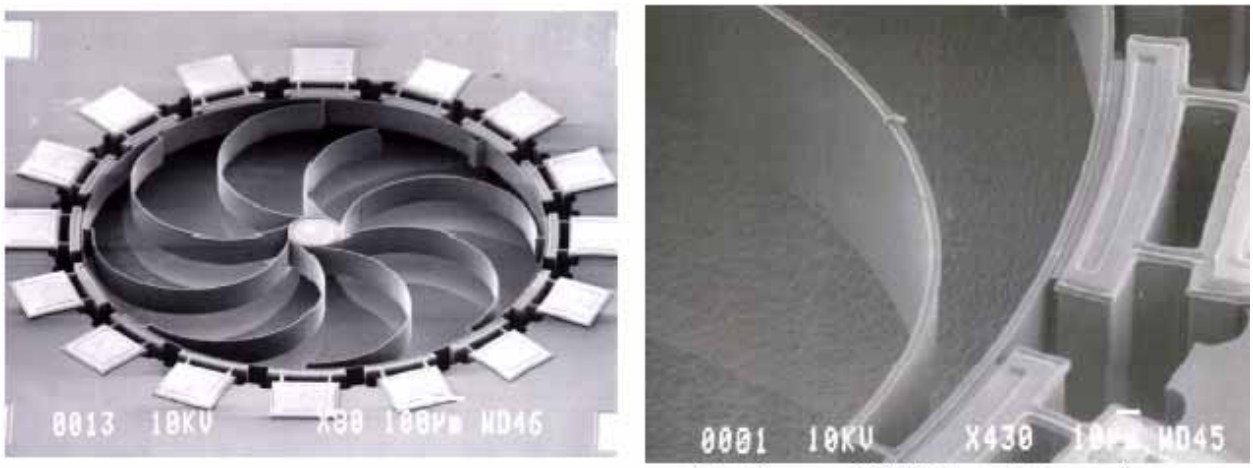


Figure 70: Fabrication process flow for high aspect ratio dry release polysilicon MEMS technology

A new batch of gyroscopes has been fabricated using the new "high aspect ratio dry release polysilicon" process. Using this process, the thickness of the sense electrode will be comparable to the thickness of the polysilicon ring. This process, however, gives the flexibility of fabricating devices with gaps between the ring and sense electrode as large as 4µm. There is no blanket etch step required and the thickness of the ring is only limited by the capabilities of the DRIE process. Figure 70 shows the fabrication process for the high aspect ratio dry release polysilicon MEMS process. 80µm trenches with straight sidewalls (90°±1°) are dry etched into the substrate using the STS deep etcher. Then, a layer of sacrificial oxide (~1.5µm) is deposited using LPCVD process at high temperature. The high temperature is used to ensure conformal coating of oxide

in the trenches. Then LPCVD polysilicon is deposited to completely fill the trenches, thus forming the ring of the gyroscope.

The sacrificial oxide layer on the wafer surface is then patterned and more polysilicon is deposited. This second layer of polysilicon is used to provide the overhanging structure to hold both the ring and the sense electrodes. The device is metalized and after another lithographic step, the device is dry etched using an isotropic recipe. The isotropic etch releases the sense electrode, which is made of single crystal silicon, from the substrate wafer. Trenches refilled with sacrificial oxide are used to provide sidewall protection for the sense electrode while the isotropic dry etch undercuts the sense electrode to isolate it from the substrate.
Figure 71 show the SEM view of a prototype device and a close-up view of the same device. The devices have been tested and some preliminary results have been obtained, they will be reported further. However, the quality factor measured for the devices are in the range of 500-4000. Higher quality factor is desired and new mask set has been design to reduce anchor dissipation.

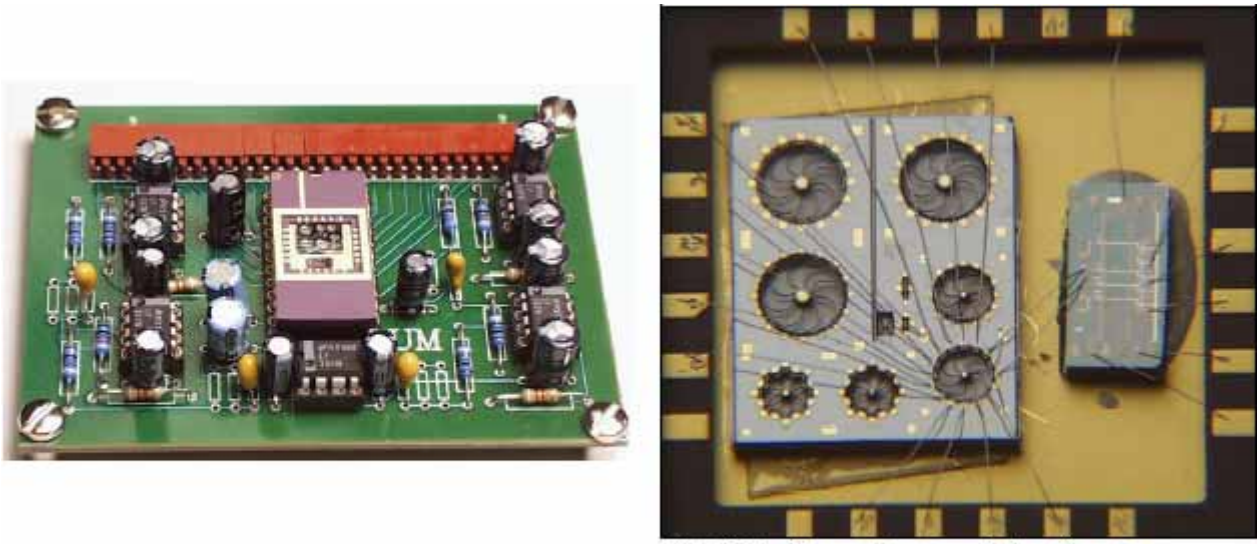


(a) Top view

(b) Close up SEM shot of ring and sense electrode

Figure 71: SEM show of prototype device fabricated with high aspect ratio dry release polysilicon MEMS technology

The setup for the whole rate table system is concluded, and some primary results are obtained. Due to the need of high precision measurement to achieve the degree-per-hour target, all of the parasitic capacitance components were tried to be canceled over the last decade. In order to cancel the parasitic capacitance associated by the interface circuitry constructed on a proto-board, this circuit is converted to a PC board. Figure 72 (a) shows the picture of the PC board designed, and fabricated.

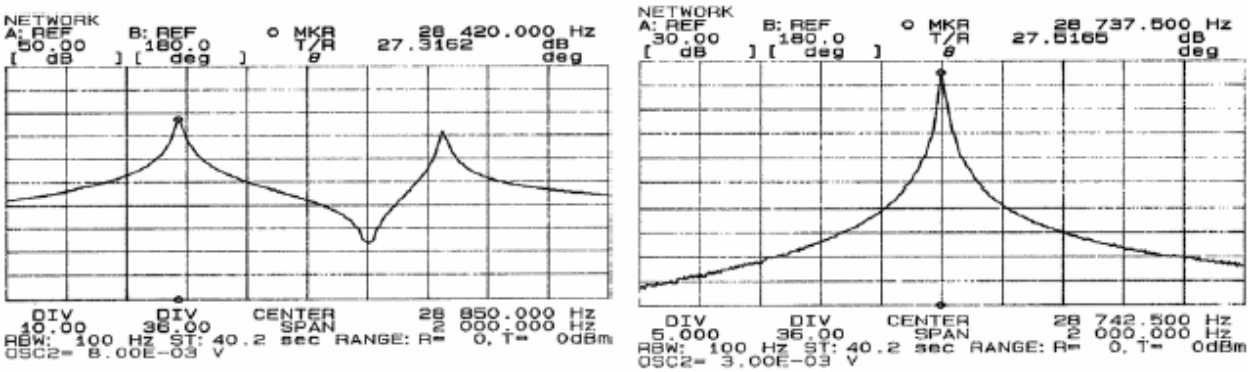


(a) Interface PC board

(b) Hybrid attachment of the ring gyroscope and the unity-gain buffer IC chip in a 24-pin ceramic DIP package.

Figure 72: Fabricated gyroscopes and interface PC board

The outputs of the structures are passed through a source follower, which is a separate die, connected to the gyroscopes by wire-bonds. This hybrid connection, shown in Figure 72 (b), increases the input capacitance and degrades the performance. In order to get rid of the loading problems created by this connection, a new design is in the development phase which integrates the gyro structures and the source follower on the same die.



(a) Before balancing

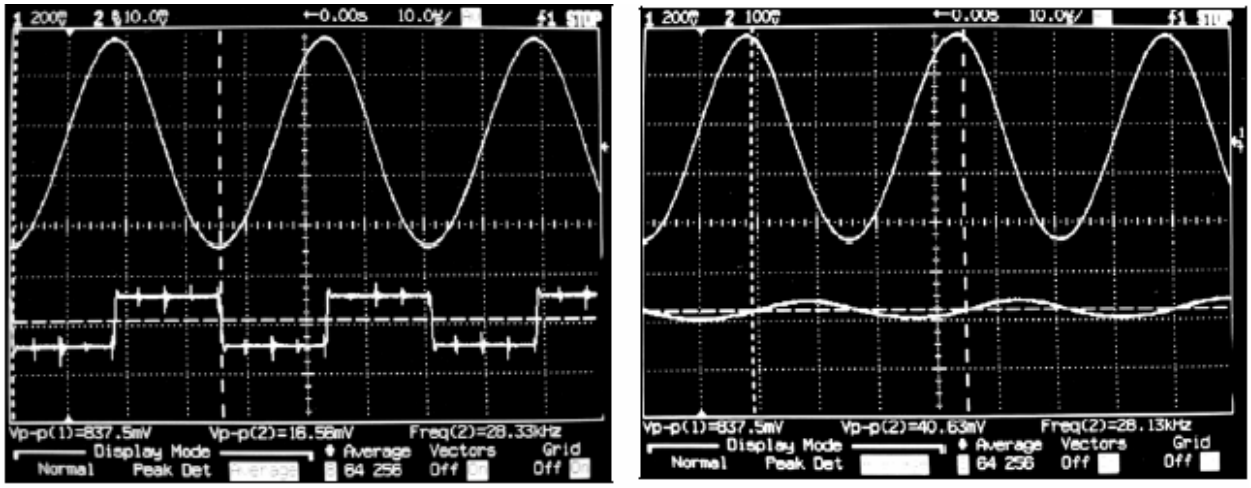
(b) After balancing

Figure 73: (a) Before balancing: Two flexural resonant peaks of a prototype single ring gyroscope have different frequencies. (b) After balancing: two peaks merge together after electronic tuning and the frequencies become equal. The balancing voltages needed to null 800Hz of frequency split were less than ±6 Volts in magnitude.

Preliminary tests are done on the current structures under those constraints using the current setup. Figure 73 shows the two flexural resonant peaks before and after the balancing voltages

are applied. As can be, perfectly balanced structures can be obtained by the adjustment of the voltage values. The frequency split between the two modes is approximately 800 Hz, for this testing. A new balancing and biasing methodology is being investigated for now, which will drop the frequency split below 100 Hz, and the polarization voltage, which leads better and easier balancing of the structures.

The quality factor of this structure is measured to be 1200, although they are designed to be several of magnitude higher. The reasons for having lower quality factor are investigated and the problems are to be solved in the new batch. Control circuitry is now constructed on a proto-board and will be converted to PC board soon. The control circuitry is a phase-locked loop circuitry which continuously drives the gyro at the resonant frequency, keeping the vibration amplitude constant. Another loop, the quadrature control loop, continuously nulls out the zero rate output of the structure due to drift in the operation. Figure 74 shows the drive signal generated by the control circuitry and the output signal of the gyroscope and the zero rate output of the structure after external biasing.



(a) (b)

Figure 74: (a) Square-wave drive signal generated by the lock-in amplifier and the output signal from the gyroscope. (b) Zero Rate Output (ZRO) of the gyroscope (bottom trace) after balancing. The top trace shows the output of the drive mode.

The tests including the quadrature control loop have been done recently, in light vacuum conditions. The output of this test is given in Figure 75. It should be noted that since this measurement was carried out under light vacuum conditions, the quality factor was as low as 200, which is much lower than the desired value. Using the preliminary results got from these tests the rate result shown in Figure 76 is obtained.

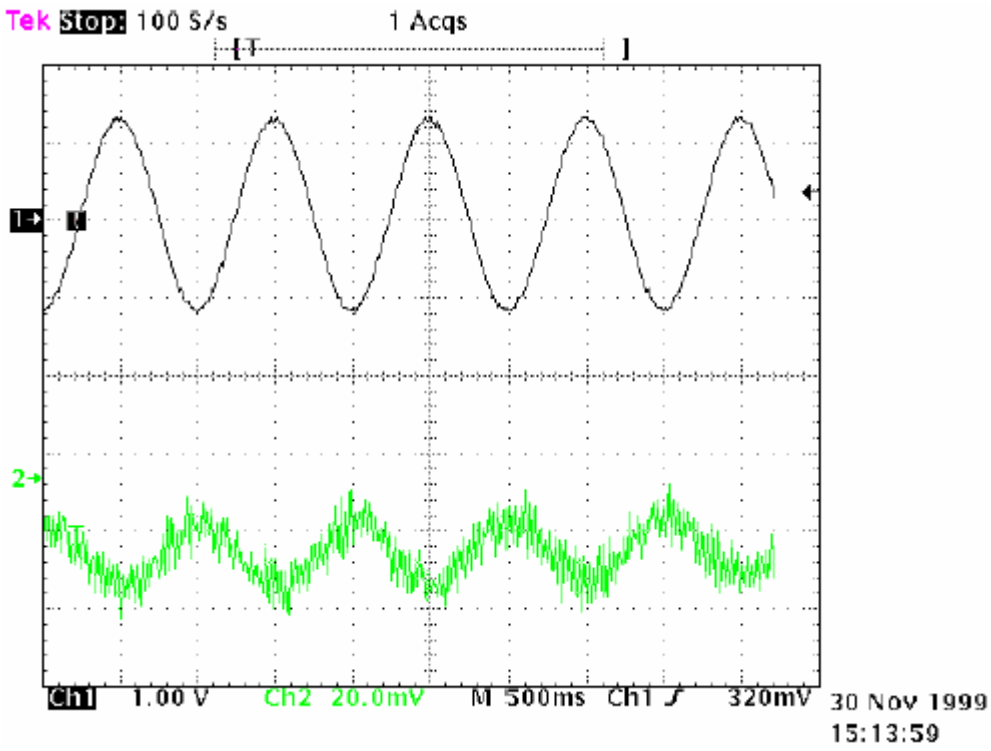


Figure 75: Response of a prototype single ring gyroscope to a 5Hz sinusoidal rate with an amplitude of ±120 deg/sec.

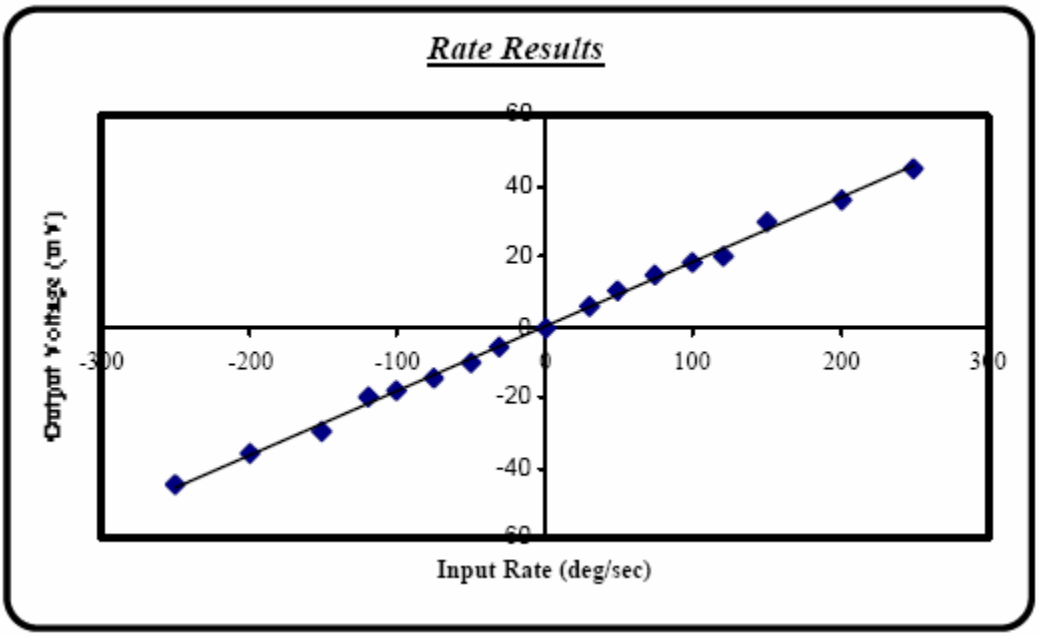


Figure 76: Response of a single ring gyroscope to input rotation rates in a 5Hz BW. The sensitivity of this device under light vacuum (Q≈250) was around 200μV/deg/sec.

In order to increase the quality factor, which in turn would increase the sensitivity, some modifications for the anchor release pattern are done. Figure 77 shows one ring structure with the modified anchor to the silicon.

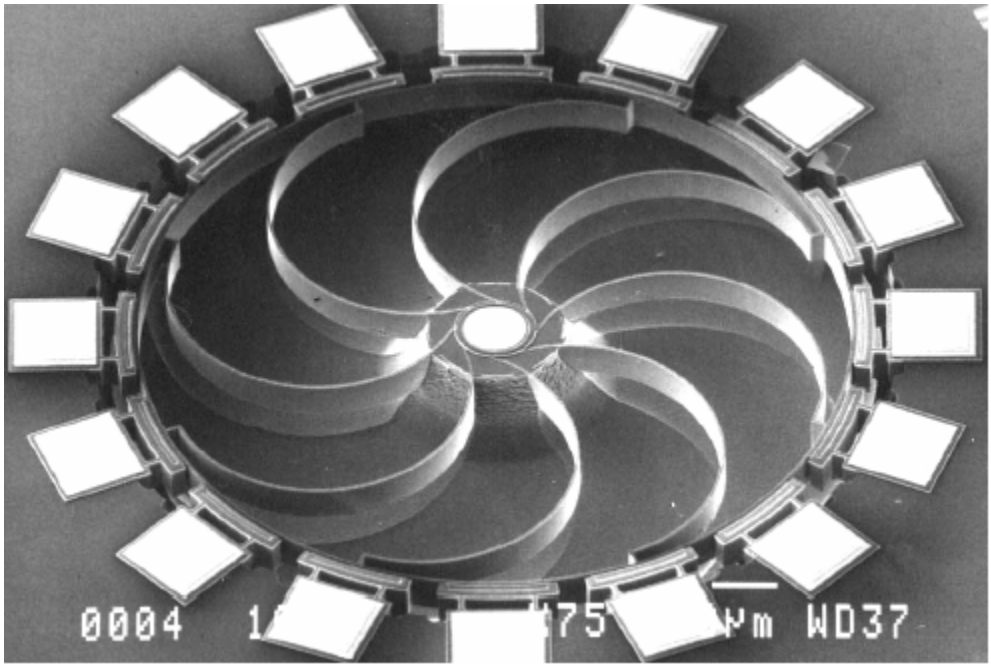


Figure 77: One ring gyroscope with modified anchor

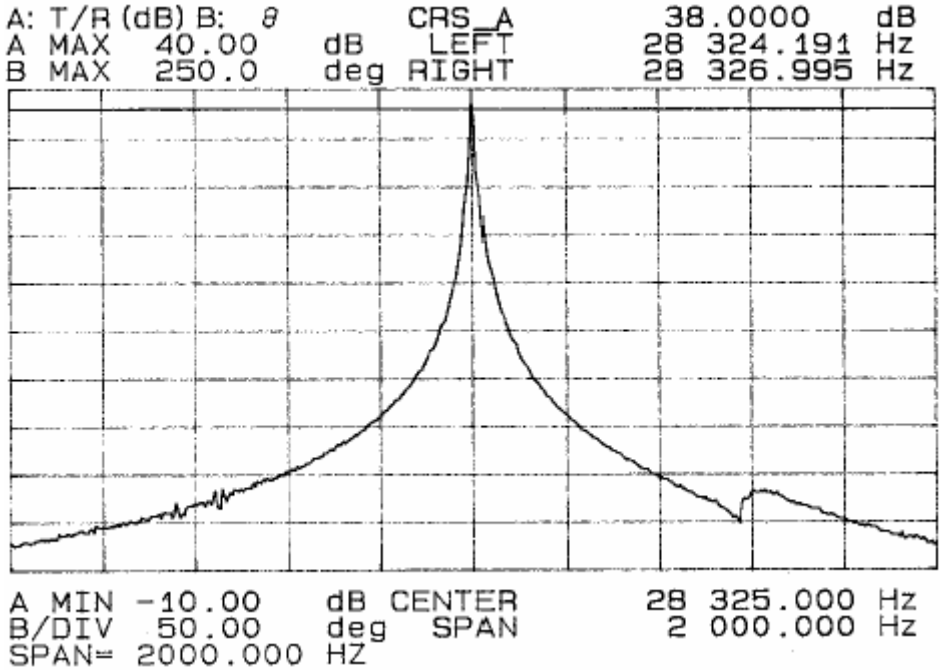


Figure 78: Frequency response of the single double-ring gyroscope (Q=5000)

The anchor point is now stiffer and possible loss of quality factor due to anchor point is eliminated. The tests show that the quality factors of the structures are increased to 5000 by this slight modification. Figure 78 shows the frequency response of the double-ring structure with the modified anchor.

By this simple modification, quality factor is increased significantly, but it is still five times lower than the designed values. To understand the nature of the loss, which causes low quality factor, several finite element simulations were performed. These simulations showed that the energy loss is mainly because of the high stress at the intersection points of the anchor and the support springs as shown in Figure 79.

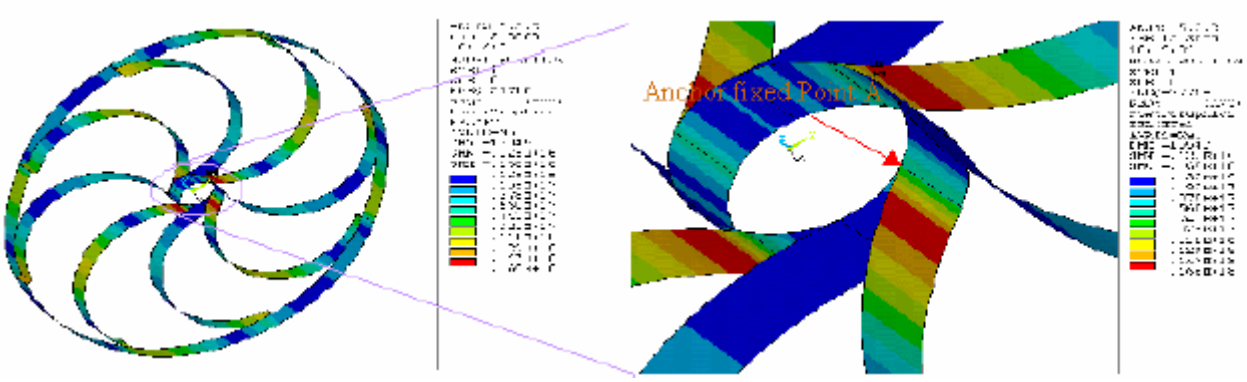


Figure 79: FEM simulation results of single-ring gyroscope

A new anchor structure, which eliminates these high stress points is designed and fabricated successfully, but hasn't been tested yet. Besides the improvement of the structures, integration of a buffer circuitry with the device would increase the performance by an order of magnitude. By integration, the parasitic capacitances associated with the wire bonds would be canceled out, which in turn increase the sensitivity of the devices. In order to integrate the device with the circuitry the fabrication process is enhanced with an inclusion of several NMOS steps. As for the circuitry, simple Enhancement/ Depletion NMOS process is selected for the sake of simplicity. The cross-section of the proposed structure with the circuitry is given in Figure 80. The process consists of 14 masks in total.

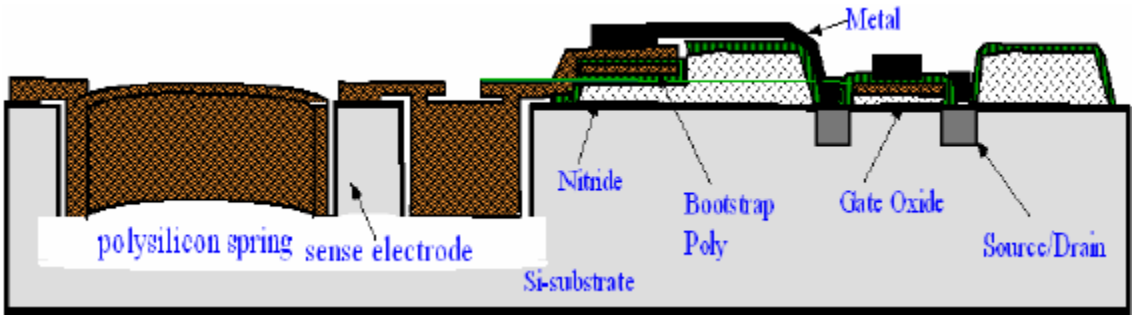


Figure 80: Cross section of the new structure with the NMOS circuitry

Figure 81 shows the schematics of the buffer circuitry and the layout of the new electrode structure. The buffer circuitry is a simple depletion NMOS source follower, which is biased with a diode connected enhancement NMOS transistor. To reduce the parasitics, bootstrapping is used in the circuitry, with another poly silicon layer, which can be seen from the cross-section.

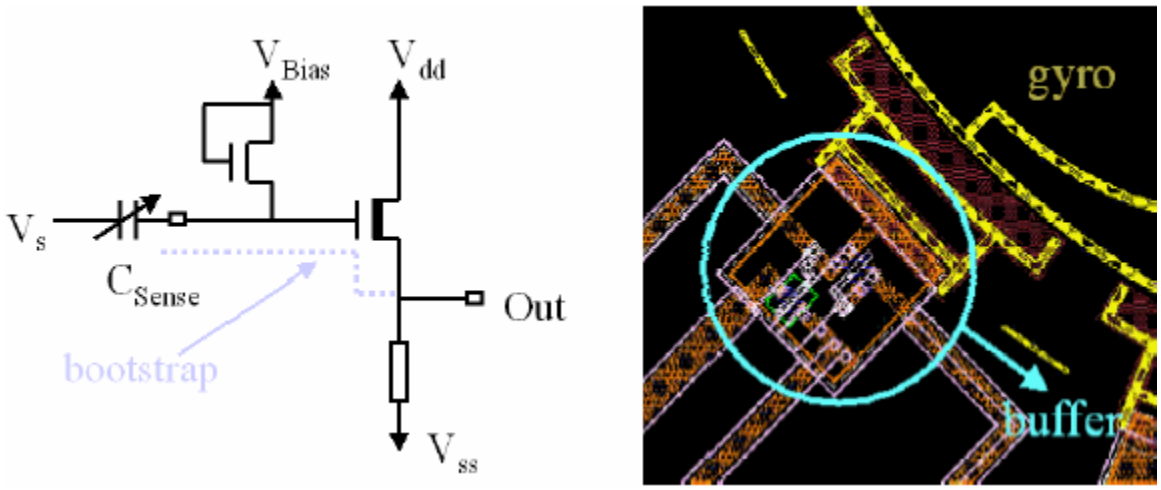


Figure 81: Schematics and the layout of the buffer circuitry

A first trial run had been conducted and several problems have been found. The most important problem is the over-etching of the polysilicon layer, which connects the sense electrodes to the pads as shown in Figure 82. Because of this problem the signal generated by the gyroscope could not be transferred to the pad, and the single crystal silicon, increasing the mass of the structure, which should be hanged to the ring by this polysilicon layer is etched.

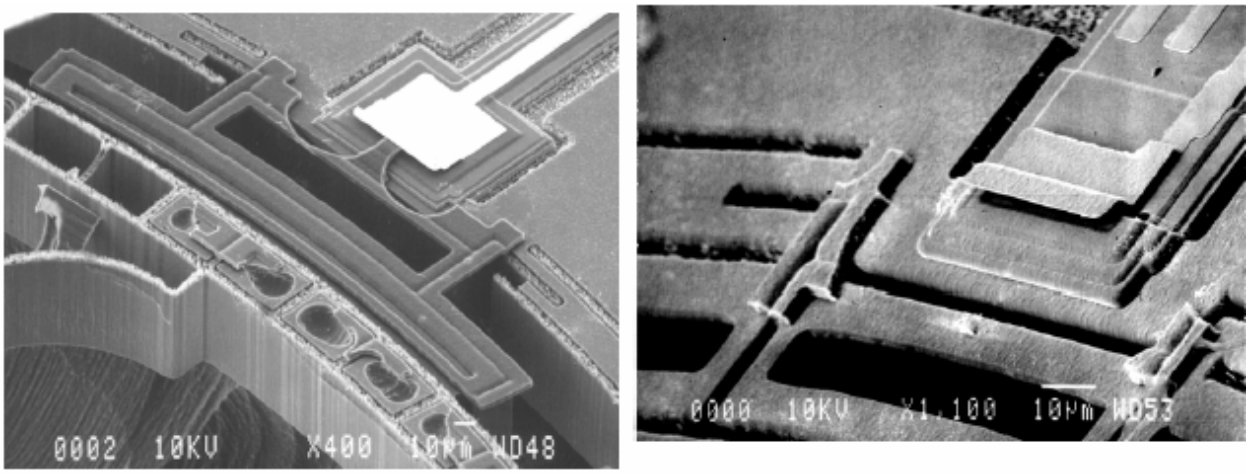


Figure 82: Over-etched electrode and ring structures.

Table 14 compares the test results and simulation data of the single ring gyroscopes. The minimum detectable signal was around 2deg/sec. It is lower than expected due to the low quality

factor of the structure. The parasitic capacitance was higher than expected because of the wire bonds between the device and the circuitry, which will be eliminated by integration.

Table 14: Test results summary of Single Ring Gyroscope.

	Designed Parameters	Testing Results
Ring Diameter	1.1mm	1.1mm
Support ring diameter	0.42mm	0.42mm
Sense gap	1.5 μm	1.4 μm
Ring width	4μm	3.6μm
Height of ring	80μm	80μm
Height of sense electrode	80μm	60μm
Resonant freq. of flexural mode	27.3kHz	28.2kHz
General mass	3.61μg	__
Quality factor	20000	1100
Total capacitance	0.5pF	2pF
Equivalent input noise of buffer	1μV/√Hz	__
Polarization voltage	7V	2.5V
Bias volt of buffer	4V	4V
Minimum detectable signal	0.04 °/sec (10Hz BW)	2°/sec

Table 15: New Design with Hanged Crystal and Soft Anchor

	One-Ring Gyro	Two-Ring Gyro	Four-Ring Gyro
Ring Diameter	1.1mm	1.6mm	2.4mm
Sense gap	1.4μm	1.4μm	6μm
Ring width	4μm	4μm	4μm
Height of ring	80μm	80μm	80μm
Post Diameter	420μm	320μm	1040μm
Resonant freq. of flexural mode	31.78kHz	29.84kHz	28.66kHz
Quality factor	20000	20000	20000
Total capacitance	0.5pF	0.5pF	0.5pF
Electronic noise floor	4.31e-3 °/sec/√Hz	2.85e-3 °/sec/√Hz	1.96e-3 °/sec/√Hz
Brownian noise floor	1.22e-2 °/sec/√Hz	5.12e-3 °/sec/√Hz	7.85e-4 °/sec/√Hz
Min. detectable signal	0.041 °/sec	0.018 °/sec	0.0066 °/sec

Table 15 summarizes the expected performances of the designs with the new anchor structure. The readout circuitry is an amplifier with two channels to amplify the signal obtained from a gyroscope. A PCB is being used for this circuitry to reduce the parasitics. A new PCB is now being designed and will be fabricated to accommodate the new gyroscopes with the integrated circuitry. The new readout circuitry includes four three channel, two of which are output channels. These output channels are the compliment of each other, taken from the opposite electrodes. The signals from these channels will be added to multiply the sense signal by two.

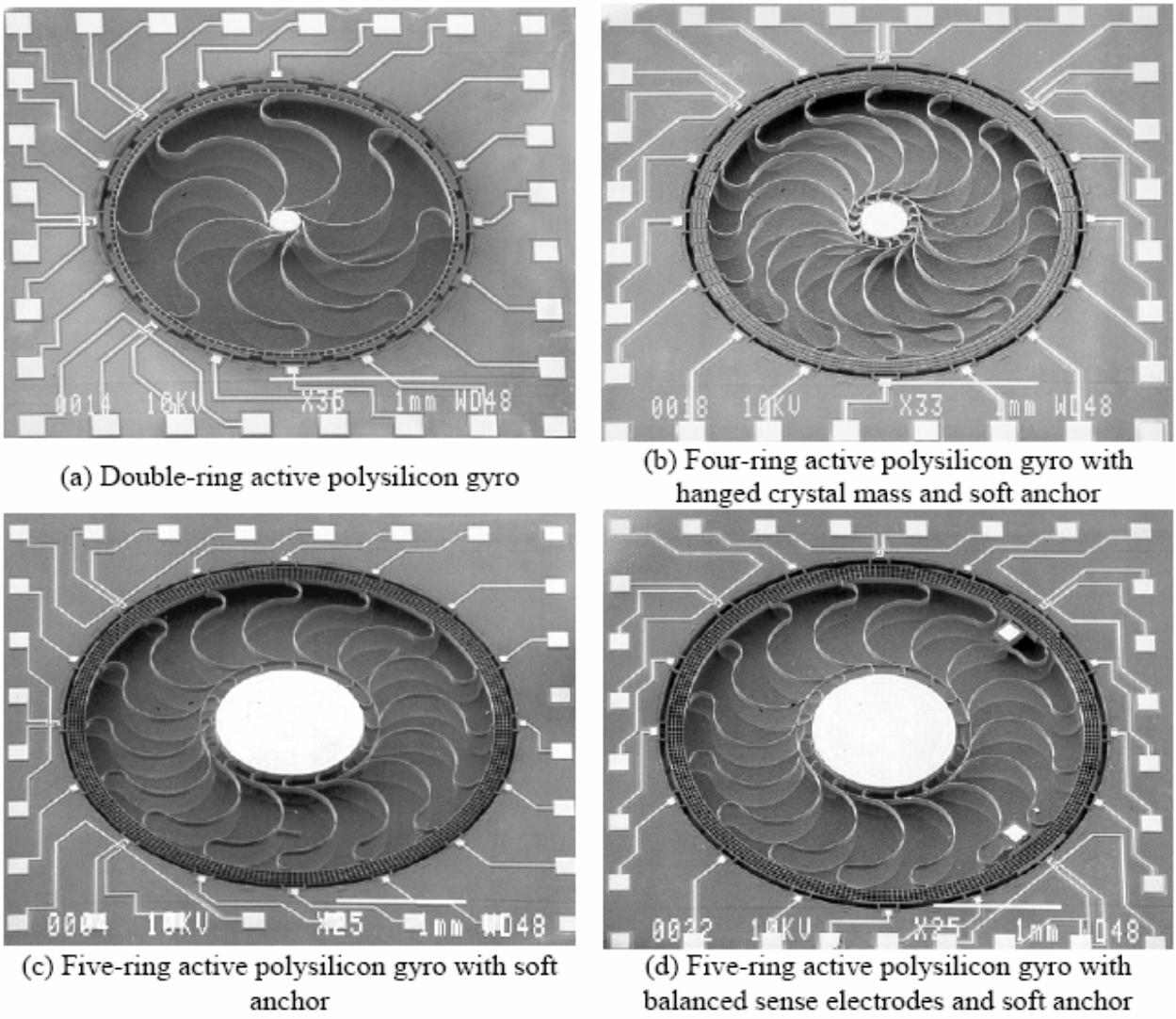
The readout circuitry is a PLL circuitry that locks to the resonant frequency of the structure and drives it at constant amplitude. This circuit is still on a protoboard and will be transferred to a PCB to reduce the area it occupies and reduce the parasitics.

Although the high aspect ratio polysilicon micromachining technology is capable of producing polysilicon ring and sense electrodes that have a thickness of 70-80μm, it has one shortcoming that makes it difficult to fabricate devices with degree per hour performance. This shortcoming is the limited width and thickness of the structure. High performance gyroscopes require large mass, hence trench depth and width should be made as deep and wide as possible. However, for thick trenches with depth greater than 100μm, the blanket etch used in the high aspect ratio polysilicon micromachining process will cause excessive etching of the side wall polysilicon at the top of the trench which makes subsequent lithographic steps difficult. Moreover, the high aspect ratio polysilicon micromachining process requires etching of trenches with different mask opening. Due to RIE lag, trenches with different thickness are formed, which is not desirable for device fabrication. It should be mentioned that these limitations are not an inherent problem with this technology and will be removed as the DRIE technology continues to improve and we are capable of fabricating even deeper trenches with higher aspect ratios than possible with existing processes.

Another shortcoming of the first polysilicon gyroscopes was the readout of the sensor signal. The current generated by the gyroscope with a rotation rate in the order of degrees per hour is extremely small, that can only be picked up by capacitive sensing. Equation 5 gives the sensitivity of the proposed structure. As can be seen in order to increase the signal level the parasitic capacitances should be eliminated and quality factor should be increased.

$$\Omega_{Z(Electronic)} \cong \frac{\left(C_d + C_{pad} + C_{inp}\right)}{4A_g\left(V_p - V_{bias}\right)} \cdot \frac{d_0^2}{\varepsilon \cdot h \cdot r \cdot Sin(\Delta\theta)} \cdot \frac{1}{q_{drive}} \frac{\omega}{Q} \cdot V_n \cdot \sqrt{BW} \qquad \text{Equation 5}$$

In order to decrease the parasitic capacitances caused by the wire bonds used to connect the gyroscopes to the buffer circuitry in a hybrid fashion, a simple buffer stage that is integrated with the gyroscope is designed in our second-generation polysilicon gyroscopes. The main problem was that the field oxide was etched away when we did the HF release after Deep RIE isotropic etching formed the gyro structure. Because we used post-NMOS process to fabricate the integrated gyro, it is very important to protect the circuitry part in a long-time HF release process. Figure 84 shows the gyro structure and buffer circuitry before and after HF release. As we can see, the overhang polysilicon electrode and some metal lines were gone after HF release process because the field oxide was attached. The process we have developed has a yield way below our expectations, moreover complicating the process with an additional 7 masks (total 15 masks).



(a) Double-ring active polysilicon gyro

(b) Four-ring active polysilicon gyro with hanged crystal mass and soft anchor

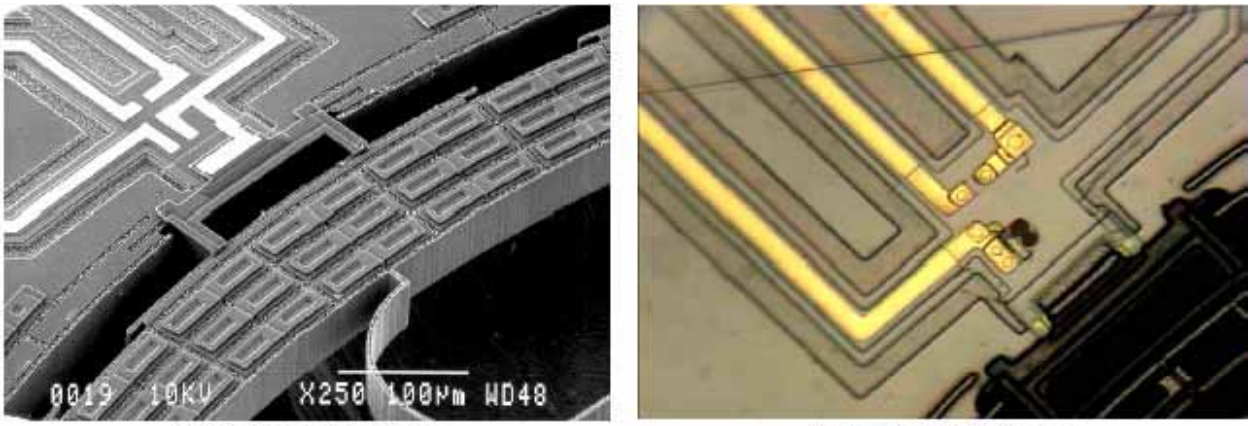
(c) Five-ring active polysilicon gyro with soft anchor

(d) Five-ring active polysilicon gyro with balanced sense electrodes and soft anchor

Figure 83: SEM pictures of the integrated polysilicon ring gyroscopes

To increase device sensitivity, increase output signal, and reduce the effects of parasitic capacitance, we have developed a new technology for the fabrication of single-crystal silicon gyroscope. In this technology, the parasitic effects is reduced, material quality factor and the general mass of gyro will be increased. All of these will reduce the device noise (Equation 5 and Equation 6), thus increasing the overall sensitivity of gyroscope. After several failures on integration trials and our limited resources, we have shifted our focus to the single crystal ring gyroscope.

$$\Omega_{z(Brownian)} = \frac{1}{2A_g q_{drive}} \sqrt{\frac{k_B T}{\omega M Q}} \sqrt{BW} \qquad \text{Equation 6}$$



(a) Before HF release (b) After HF release

Figure 84: Overhang polysilicon electrode and some metal lines was gone because the field oxide was attached during the HF release.

3 Single crystal silicon gyroscope

Single crystal silicon ring gyroscopes have great advantages over their polysilicon counterparts including, but not limited to, extremely simple fabrication steps (four masks), low temperature process, large mass, high Q factor, low parasitic, vacuum packaging compatible, and high G shock survival (robust and rigid device structure). In order to ensure that the single crystal silicon ring gyro operates properly, (111) orientation silicon is used because it has uniform and homogeneous material properties such as Young's modulus over the (111) surface. This is critical for the ring gyro to be able to obtain flexural sense and drive modes that are closely matched in frequency and track over temperature.

The process sequence of the single crystal ring gyroscope is given in Figure 85. The process begins with a 100 μm DRIE etching of the silicon wafer. The wafer is then metallized where electrical contacts are to be made to silicon. A glass wafer is processed to form recess areas under the vibrating ring, and the wafer is metallized to form interconnects and contact regions to the silicon devices. The two wafers are bonded anodically, and the silicon is back etched to release the structures completely.

Figure 86 shows the SEM photographs of first two batches fabricated and tested structures. Primary tests had been performed on these devices and it has seen that the resonant Q of these devices are very high, it is more than 14,000, which is significantly larger than what we obtained with polysilicon devices. But unfortunately, we couldn't measure their gyro performance because the frequency splits between drive and sense modes of these devices were too large to be matched by electric tuning.

a.)(SiGyro): DRIE define gyro structure (100µm)

b.)(SiMetal): Deposit and pattern metal on silicon wafer. [Lift-off process, Ti (20nm) /Pt (80nm)]

c.)Mask #3 (G1Recess): Wet etch glass recess (5µm)

d.) Mask #4 (G1Metal): Deposit and pattern metal on glass wafer. [Lift-off process, Ti (20nm) /Pt (80nm), shielding]

e.) Anodic bonding.

f.)Back etching

g.)Mask #6 (Bonding pad): Deposit and pattern metal on silicon wafer. [Lift-off process, Cr (20nm) /Au (300nm)]

Figure 85: Process sequence of Single Crystal Gyroscope

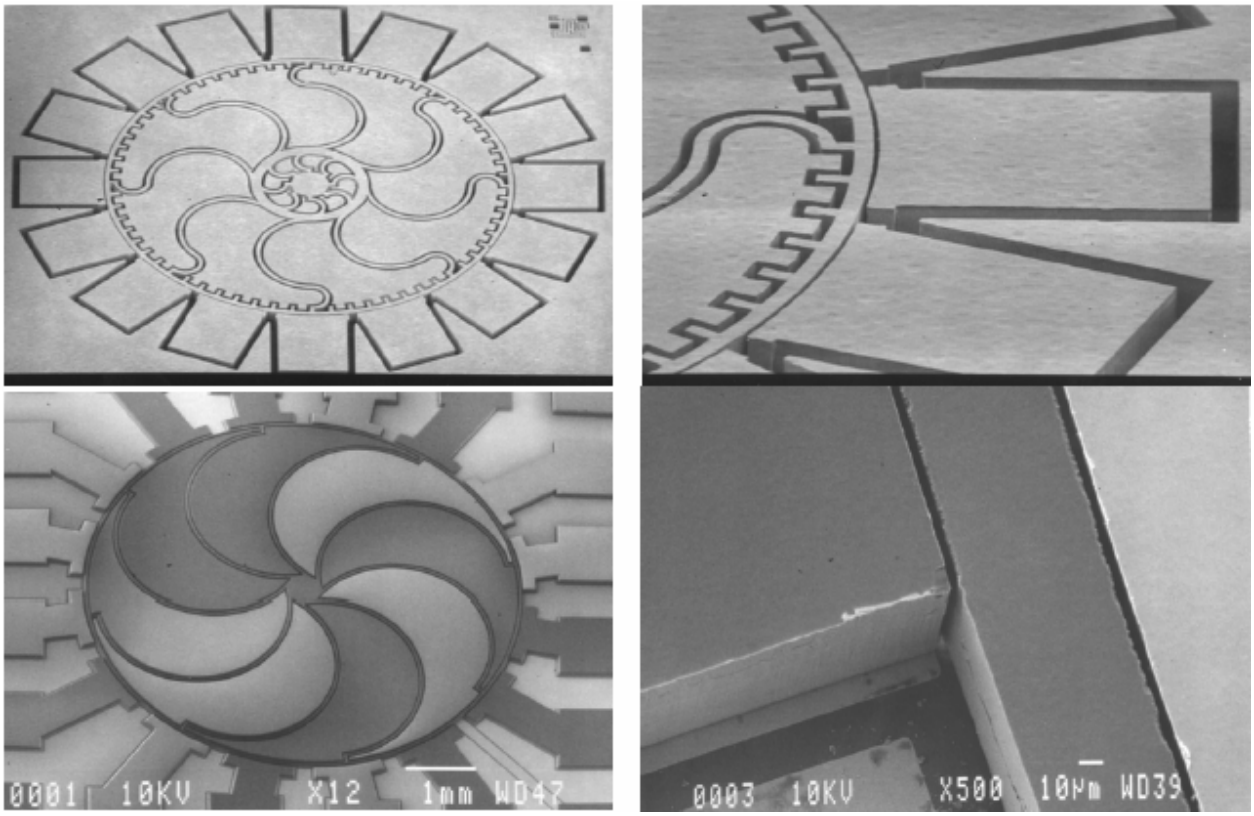


Figure 86: SEM shots of single crystal gyroscope (Up: the first run. Down: the second run)

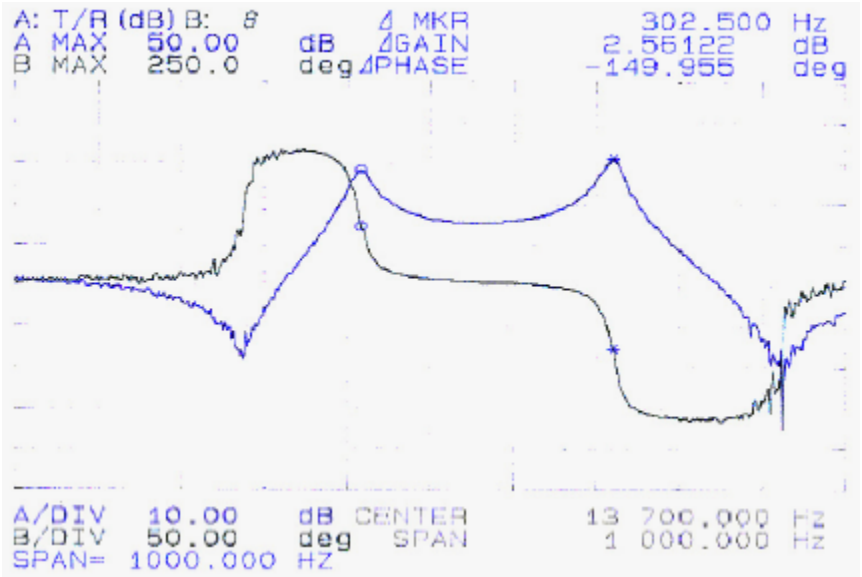
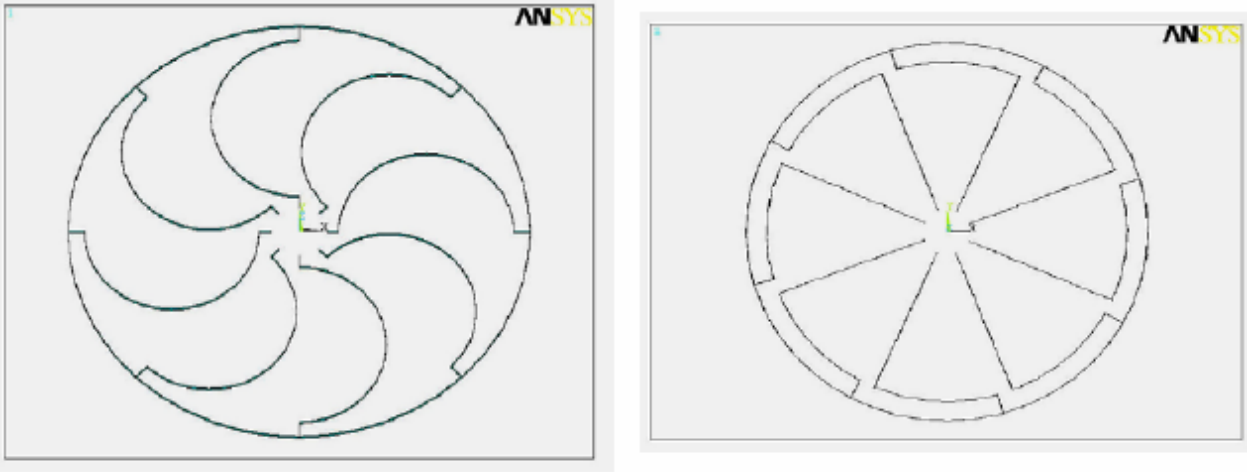


Figure 87: The 2.2% frequency split of two flexural modes in a crystal silicon ring gyroscope

Electric tuning is an attractive feature in the vibrating ring gyroscope. Any frequency mismatch between the sense and drive modes that occur during the fabrication process should be able to be

electronically compensated by using the tuning electrodes around the structure. This is very important in operating ring gyroscope. Gyro sensitivity will be amplified by Q times if the resonant frequencies of drive and sense modes are matched. Figure 87 shows the two flexural resonance peaks of such a single crystal silicon ring gyroscope with a frequency split of 303Hz while the center frequency is 13.8 KHz. Comparing with our poly silicon ring gyroscope, where the frequency split was around 60 Hz (0.21%) with the center frequency of 28KHz, the frequency split of single crystal silicon gyroscope (2.2%) is too large. It has been demonstrated that this large frequency split is hard to be balanced by electric tuning. This blocked us to get the gyro performance.

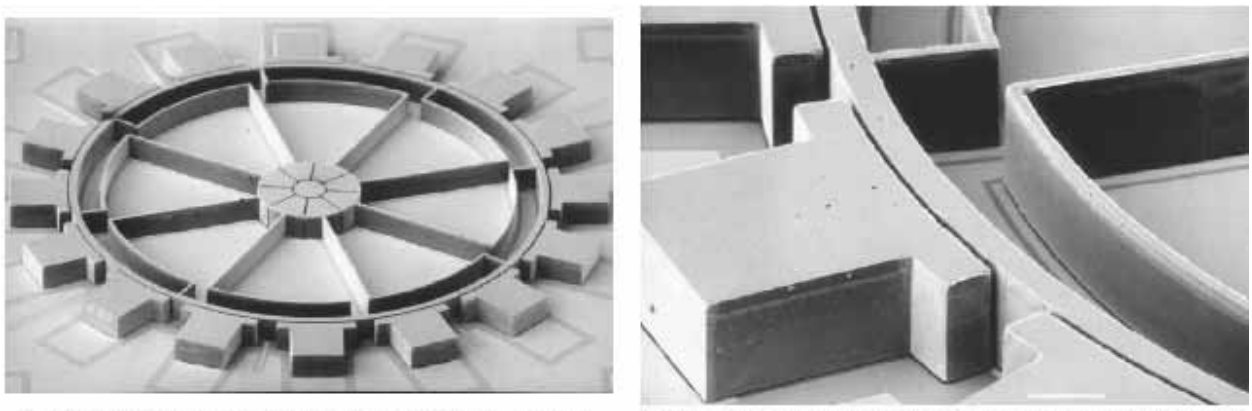


(a) Half-circle support spring (b) Meander support spring

Figure 88: The FEM modals of two different support spring ring gyroscope structures

After careful theoretical study and FEM simulation, we found the frequency split of two flexure modes in single crystal silicon ring gyroscope was due to the imperfect fabrication is significantly small if the half-circle support springs are replaced by meander springs. Figure 88 shows the FEM models of these two structures. Generally, the imperfect fabrication includes material anisotropy, non-uniform mass distribution, and unsymmetrical mechanical and electric spring effects. It is demonstrated in our current research; this frequency split in meander spring ring gyro is about a half of one in half-circle spring ring gyro. Therefore, the meander spring design provides better mode matching and facilitates tuning.

Figure 89 shows the new fabricated and tested single crystal silicon ring gyroscope. Note that the ring is 50μm wide, 150μm tall and 2.7mm in diameter to provide much larger mass and reduce thermal noise. The quality factor Q of flexure mode of the resonant ring is 33,000 in vacuum environment (1 mTorr). High Q will significantly increase the sensitivity of the gyro. The frequency spectrum of the resonant ring is shown in Figure 90. The flexure mode frequency is 25.94 kHz, which is closed to FEM simulation (27 KHz). The difference between them is because the width of ring in the gyro device is a little bit smaller than the one we designed due to the over undercut in the Deep RIE etching process.



(a) SEM of new fabricated and tested single crystal ring gyroscope.

(b) A close up view of ring structure, 150μm tall sense electrode and 10μm gap.

Figure 89: The SEM of new fabricated and tested single crystal silicon ring gyroscope.

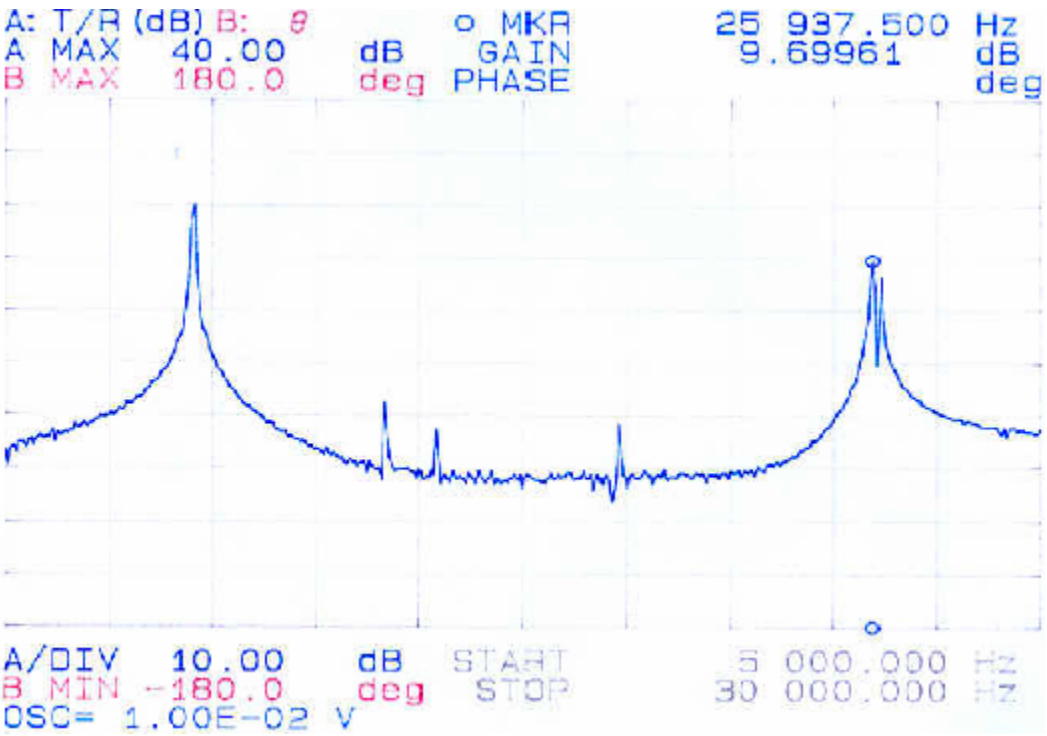
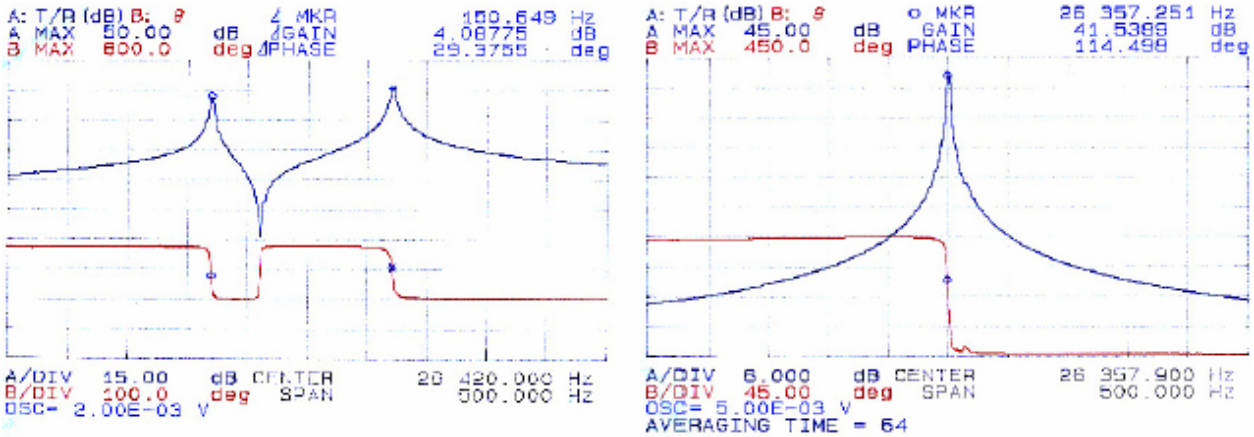


Figure 90: The frequency spectrum of single crystal silicon ring gyroscope. The frequency of flexure modes is around 25.94 kHz.



(a) Frequency split (150Hz) of two flexure modes due to imperfect fabrication

(b) After electronic tuning, two modes are matched. The Q after balanced is 8,900

Figure 91: Resonant frequency of two flexure modes of the gyro before and after balancing

The resonant frequencies of two flexure modes of the gyro before and after balancing are shown in Figure 91. The frequency split before balancing is 150Hz, about 0.58%, which is much smaller than that in the half-circle spring supported gyro which we did before, but it is still larger than what we had got in poly silicon gyro (0.21%). Fortunately, we can match these two flexure modes this time by applying relative higher balancing voltages, which are around 80 volts while the polarization voltage is 50 volts.

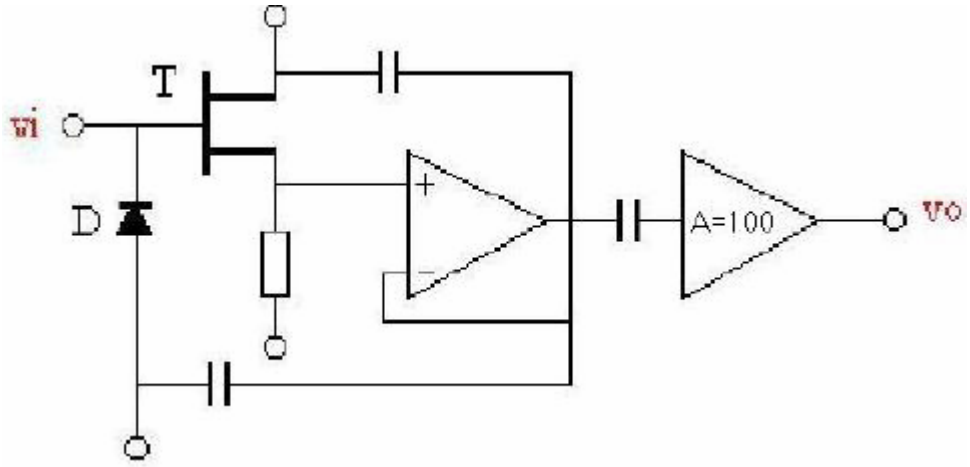


Figure 92: Schematic of interface circuitry by secreted components.

As mentioned earlier, using single crystal gyroscopes would reduce parasitic effects, thus increasing the signal level. A hybrid connection of a high performance readout interface circuit was designed and fabricated by surface mount technology. Figure 92 shows its schematic. The gain of this circuitry is 100. Its input capacitance is significant reduced by bootstrapping bias diode and the drain of JFET. It is around 0.8pF including all wire bonding interconnection. Because the low noise JFET and diode are chosen, the noise generated by the circuit is very low.

A hybrid package of such an interface circuitry with a single crystal silicon ring gyroscope is shown in Figure 93. The equivalent input noise is 30nV/√Hz at 30 kHz, which is shown in Figure 40. A hybrid package of such an interface circuitry with a single crystal silicon ring gyroscope is shown in Figure 94.

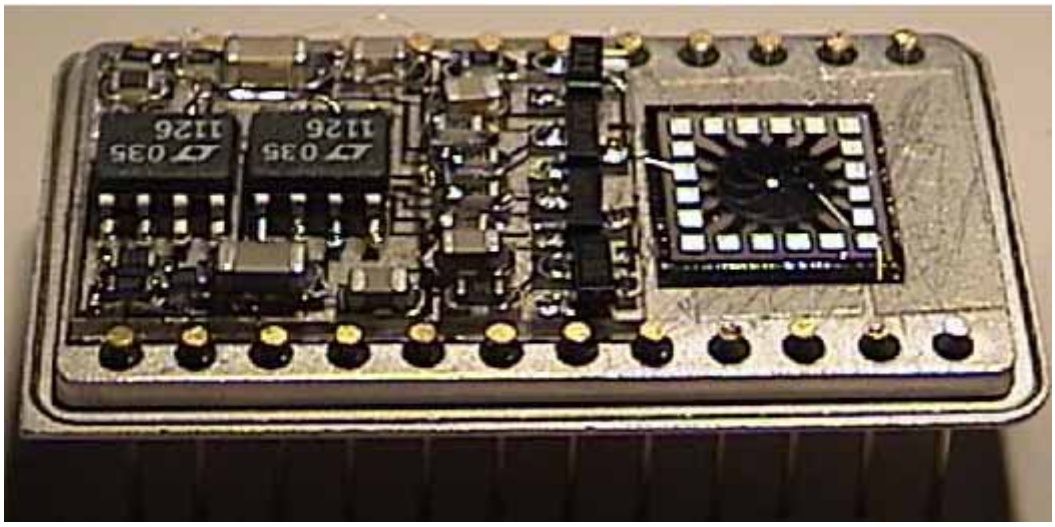
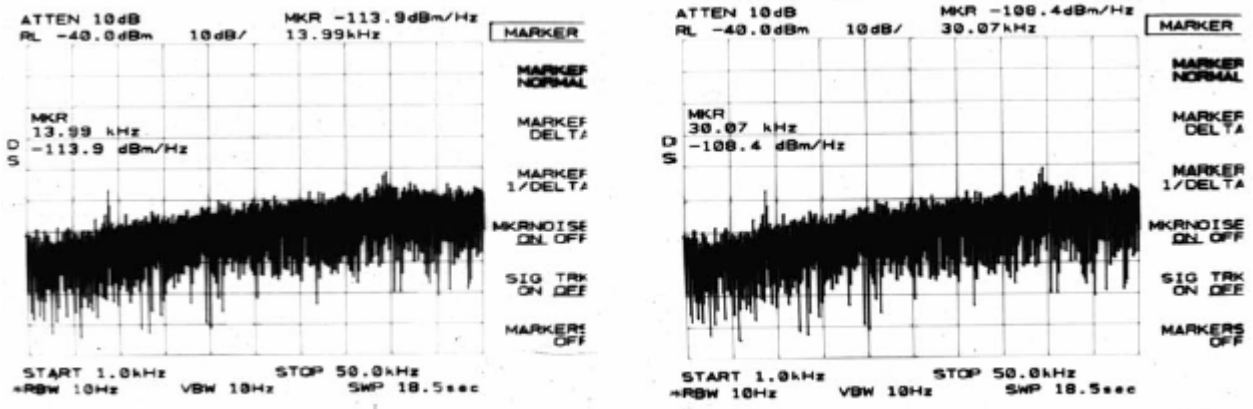


Figure 93: Hybrid package of an interface circuitry and a single crystal silicon ring gyro.



(a) The noise floor is -114dBm/Hz at 14kHz (b) The noise floor is -108dBm/Hz at 30KHz

Figure 94: The noise floor of interface circuitry.

The full control electronics for gyro operating is shown in Figure 95. There are two operation modes for measuring the rotation rate. One is open loop operation mode. In this way, the primary mode aligned the 0° pickoff will be driven to a fixed amplitude [by using the Amplitude Gain Control (AGC) loop] at the ring resonant frequency (by using PLL main loop) by applying a drive force at the 180° electrode. When the device is not rotating, the secondary mode will not be excited and will, therefore, have zero amplitude. Rotating the sensor in-the-plane of the ring causes energy to be transferred from the primary mode to the secondary mode due to the Coriolis

acceleration induced coupling. This energy coupling, in turn, causes amplitude to buildup in the secondary mode such that the 225° pickoff can measure the rotation rate.

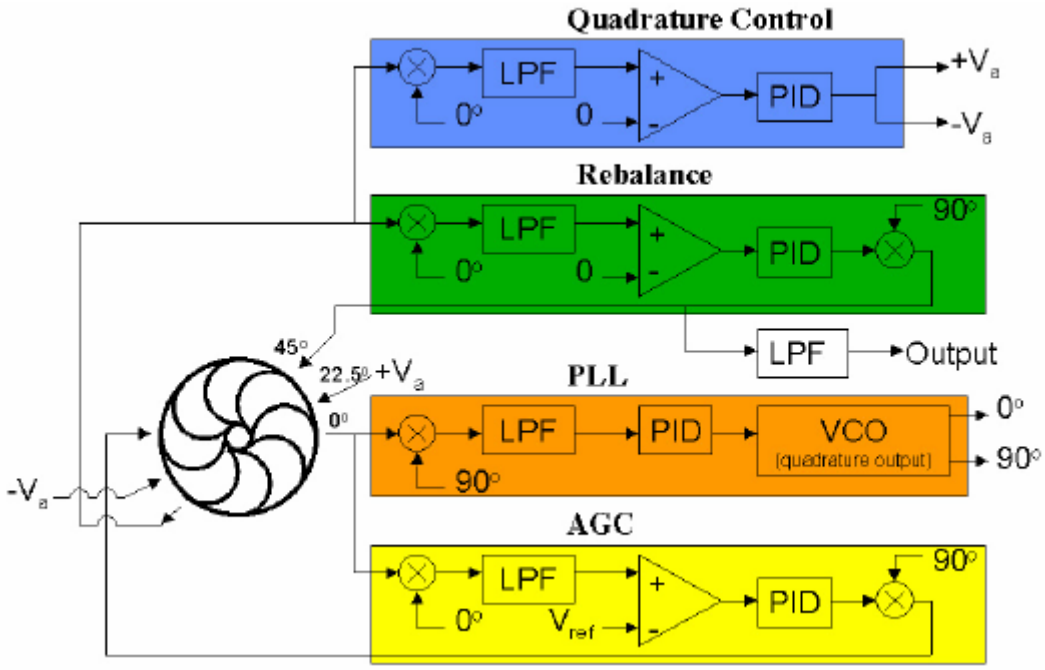


Figure 95: The control electronics for operating a ring gyroscope.

Another ring gyro operating mode is closed loop. This is a force-to-rebalance mode. In this mode of operation, the vibration amplitude at 225° pickoff is continuously monitored and driven to zero by apply the necessary drive force at the 45°-drive electrode (by using the rebalance loop) to rebalance the Coriolis acceleration induced coupling. With this feedback arrangement, no amplitude is built up in the secondary mode, which requires time for energy storage, thus allowing the response time of the sensor to be increased as needed by the closed-loop electronics. There is a penalty, however, for increasing the bandwidth as this also increases the sensor noise. In our current testing, the gyro works in open loop mode.

The PLL and AGC loop are used to drive the primary vibration mode of single crystal silicon ring gyroscope. Waveforms from the gyro are shown in Figure 96. We can see the expected 90° phase difference between the square wave drive signal (1000 times scale) and the detected sinusoidal ring vibration verifying the proper operation of these control loop. Figure 97 shows the outputs of two pickoffs in a balanced single crystal silicon ring gyroscope. The frequency doubling at node line (zero rate output at 225° pickoff) is also noticed in zero rate output testing.

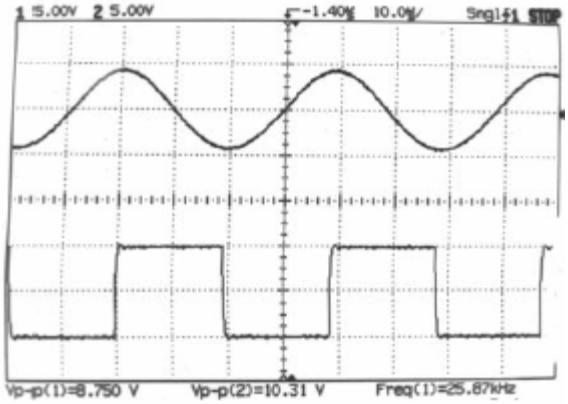
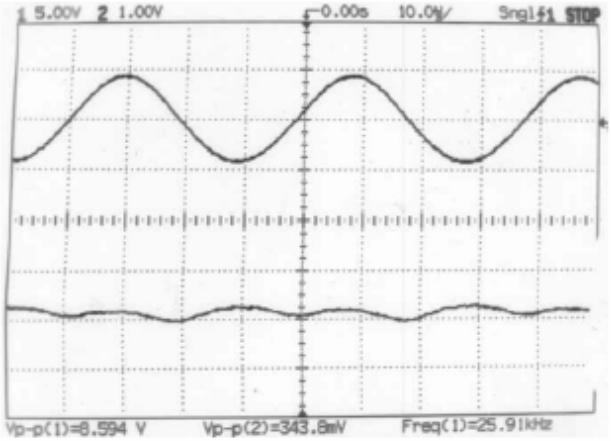
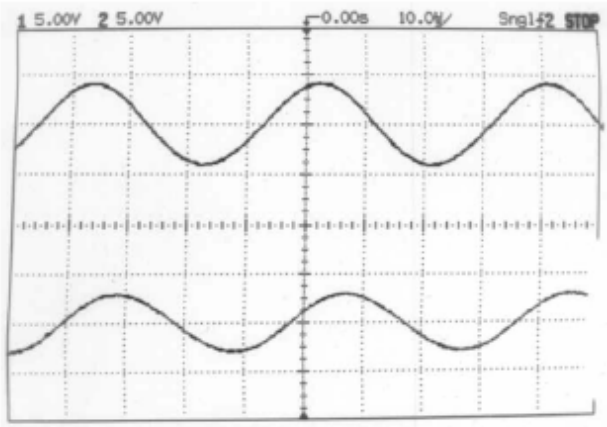


Figure 96: Primary mode drive and sense signals.

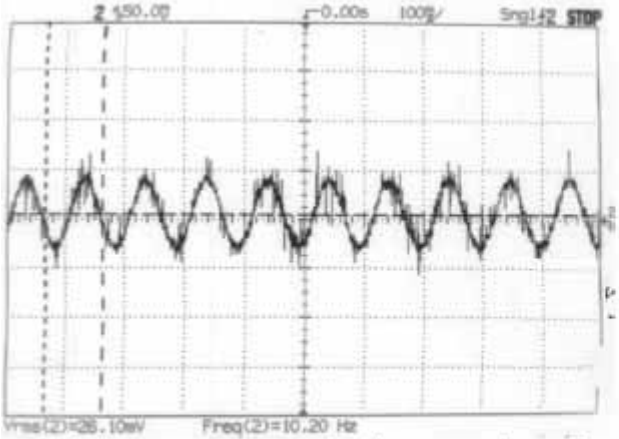


(a) Zero rate output (drive at 180°)

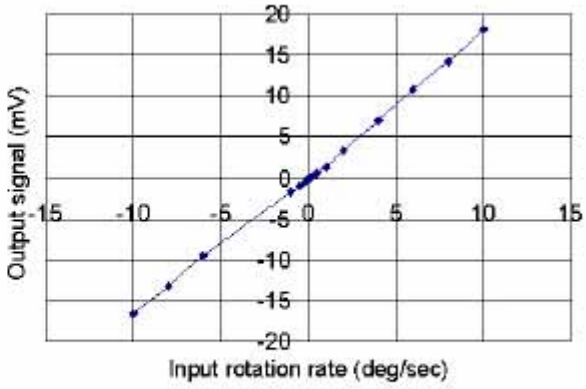


(b) Balanced two pickoffs (drive at 202°)

Figure 97: The outputs of two pickoffs in a balanced single crystal silicon ring gyroscope.



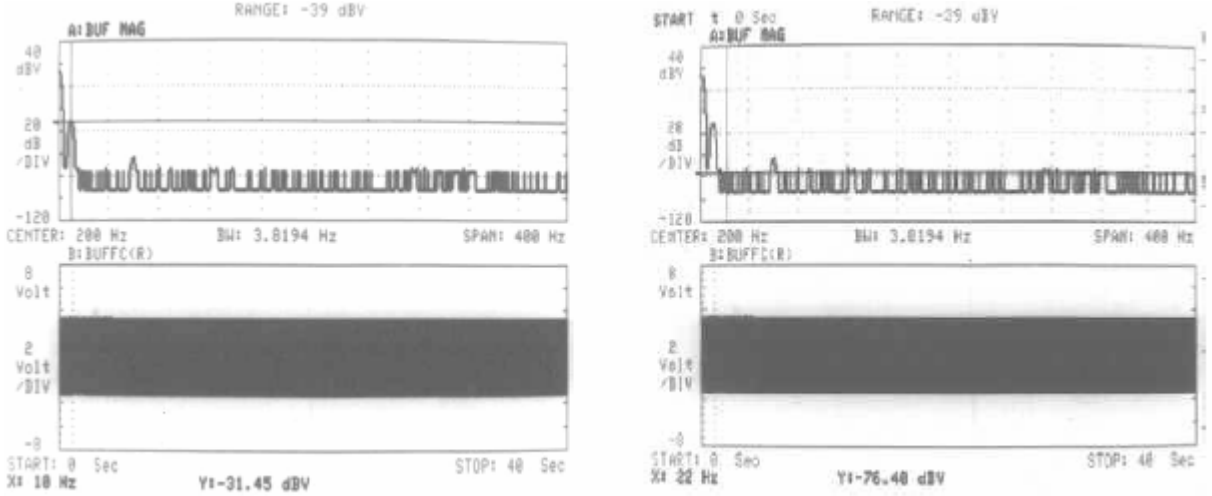
(a) The gyro output at the input rotation of 1deg/sec at 10Hz sinusoidal rotation.



(b) Gyro response at a constant rotating input, with a sensitivity of 1.8mV/°/sec.

Figure 98: Measured rate results from single crystal silicon ring gyroscope.

Figure 98 shows the rate test results. It can be seen the gyro has a good linearity. The sensitivity of crystal silicon ring gyro (1.8mV/°/sec) is much higher than that of polysilicon ring gyro (0.06mV/°/sec) because of large sense capacitance and high Q. The sinusoidal response of the gyro should be better than what we got here if a force-to-rebalance operation mode was used in the measurement. The time constant of gyro system is around 0.685sec ($2Q/f_0$, while Q=8900, f_0=26000Hz is the gyro resonant frequency). Therefore, the gyro couldn't fully response a 10Hz input. The resolution of single crystal silicon ring gyroscope could be figured out by noise spectrum analysis, which is shown in Figure 99. It shows the resolution of gyro system is 10deg/hour/√Hz. Table 16 shows the summary of single crystal silicon ring gyroscope.



(a) Gyro response= −31.45dBV (b) The noise floor= −76.40dBV

Figure 99: Gyro noise spectrum analysis while the input rotation rate of 1deg/sec at 10Hz.

Table 16: Specifications of single crystal silicon ring gyroscope.

Parameter	Expected	Measured
Ring Diameter (mm)	2.7	2.7
Ring Thickness (μm)	50	46
Ring Height (μm)	140	152
Res. Freq. (kHz)	27.1	25.94
Sense gap (μm)	5.0	10.0
Rest sense capacitance (fF)	91.1	50.6
Driving amplitude (μm)	0.5	1.1 (estimated)
Quality factor	10,000	12,000
Electronic Noise (μV/√Hz)	1.0	0.1
Polarization Volt. (V)	50	50
Brownian Noise (°/sec/√Hz)	1.90e-4	
Electronic Noise (°/sec/√Hz)	0.79e-4	
Min. Detectable Signal (°/sec/√Hz)	2.06e-3	3.0e-3

Conclusion

This program focuses on developing inertial-grade micromachined accelerometers and gyroscopes and their associated electronics and packaging for use in a variety of military and commercial applications. Most micromachined inertial sensors available today are far from being suitable for navigation, guidance, seismic and microgravity measurements. It is indeed critical to reduce the size, cost, and weight of inertial instruments without compromising their overall performance. Under this project we have developed truly inertial-grade accelerometers and gyroscopes for use in navigation, guidance, seismic / microgravity measurements, and high performance commercial applications. During the project timeline:

Out-of-plane accelerometer which has a full wafer thick proof-mass, polysilicon electrodes on both sides of the wafer, controllable damping, and small air gap has been developed. This accelerometer utilizes a combined surface and bulk micromachining technology to obtain high sensitivity, low noise, and low/controllable damping which are key factors essential in achieving micro-g and sub-micro-g resolution. In order to mitigate residual stress of long polysilicon electrodes, in-situ and Rapid Thermal Annealing (RTA) have been performed, and demonstrated stress-free electrodes successfully, which results in high yield manufacturing process.

Three different types of *in-plane* accelerometers have been developed: A Silicon-On-Glass (SOG) accelerometer, an all-silicon accelerometer, and a sub-micrometer gap accelerometer. The SOG device utilizes Deep Reactive Ion Etching (DRIE) and wafer bonding technologies to build thick (~120μm) proof-mass with a narrow sensing gap. This device can be monolithically integrated with CMOS readout circuits. The all-silicon accelerometer implements a well-characterized combined surface and bulk micromachining technology to obtain a wafer thick (~475μm) proof-mass and very narrow sensing gap (~1.1μm), which provide high sensitivity and low noise characteristics comparable with high performance *out-of-plane* devices. The sub-micron gap accelerometer uses an electron beam lithography and DRIE to achieve 0.2μm sensing gap. Unlike conventional accelerometers, this device utilizes comb drive sense/drive electrode configuration to achieve large dynamic range and low noise floor by taking advantage of the sub-micron sensing gap.

A monolithic three-axis accelerometer using two *in-plane* and one *out-of-plane* accelerometers has been developed. The accelerometer is small size, self-aligned, and easy to package. All three devices have full-wafer thick silicon proof-mass, large area polysilicon sense/drive electrodes, and small sensing gap (<1.5μm). The accelerometer has > 5pF/g measured sensitivity and sub-micro-g/√Hz mechanical noise floor for all three axes.

A low-offset, low noise interface electronics operating as a 2^{nd}-order electromechanical sigma-delta converter has been implemented. This chip operates the accelerometer in closed-loop mode which results in higher dynamic range, linearity and bandwidth. A fully differential switched-

capacitor type front-end circuit has been utilized in this chip due to its parasitic insensitive operation.

Simulations to help identify the limits provide guidelines and verify performance parameters have been performed. Modeling and simulation of the closed-loop accelerometer includes the electrode movement in addition to all other non-linearities and non-idealities. The system is modeled and simulated in the time domain using SIMULINK. Besides this, noise components of the system identified in detail. Noise analysis has showed that as the Brownian noise of the device decreases to sub-μg range, the electronics becomes dominant in the overall noise performance. The electrical noise sources have been identified through the noise analysis and a second-generation interface electronics has been implemented with a better noise performance.

A novel readout circuit, the multi-step electromechanical sigma-delta modulator architecture, has been introduced and implemented. This technique is based on using a two-element multi-step sensor array similar to a multi-step data converter. Basically the first element does coarse measurement, its output is deducted from the input of the second element and the second element performs a fine measurement on the smaller differential input. Multi-step architecture provides high signal-to-noise ratio (SNR) and improves the dynamic range. The fabricated chip was tested individually and the open-loop operation with *out-of-plane* accelerometer was verified.

All different types of accelerometers have been tested with the interface electronics. 1.08μg open-loop and 10μg closed-loop resolution have been achieved with *out-of-plane* accelerometers. For *in-plane* accelerometers open-loop resolutions are 80μg and 1.6μg for SOG and all-silicon devices, respectively. Single-chip, three-axes accelerometers are consistent with the *out-of-plane* and all-silicon *in-plane* accelerometers.

Polysilicon ring gyroscopes utilizing High Aspect Ratio combined Poly and Single crystal Silicon (HARPSS) have been developed. This technology provides tall structure (~80μm) and large sense/drive gaps between the ring and sense/drive electrodes, which are essential to achieve a high performance micromachined gyroscope. In order to increase quality factor, which is necessary to achieve high sensitivity, anchors have been improved and the quality factor has been increased by more than a factor of 4. Monolithic integration with readout circuits using U of M Enhancement/Depletion NMOS process has been also performed.

In order to achieve a high performance gyroscope by reducing the parasitics, increasing quality factor, and mass of the structure, single crystal silicon gyroscope has been developed. This device has 150μm tall structure, large (10μm) sense/drive gap by using <111> oriented single crystal silicon. Meander support spring design has been implemented in stead of half-circle support to minimize imperfect fabrication effects on splitting two flexural modes, which results in better mode matching and facilitating electronic tuning. The single crystal gyroscope provides the quality factor of 33,000 in vacuum environment (1 mTorr).

A polysilicon gyroscope is tested by using simple source follower readout circuits, control circuitry to lock the resonant frequency of a gyroscope, and quadrature control loop to null out

the zero rate output. With quality factor of 1,200, drive amplitude of 0.15μm, and sense node parasitic capacitance of 2pF, the resolution is measured to be 2 °/sec in 10Hz BW. A single crystal silicon gyroscope provides high Q (12,000), good linearity (0.02%), large sensitivity (132 mV/°/sec), and low output noise (10.4 °/hr/√Hz).

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