

Georgia Institute of Technology



# Design Space Exploration and Optimization of Embedded Cache Systems via a Compiler

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**<http://www.crest.gatech.edu>**

The research presented here is funded in part by DARPA contract Nos. F33165-99-1-1499 (DIS) and F30602-00-2-0564 (PACC), HP Labs and Yamacraw

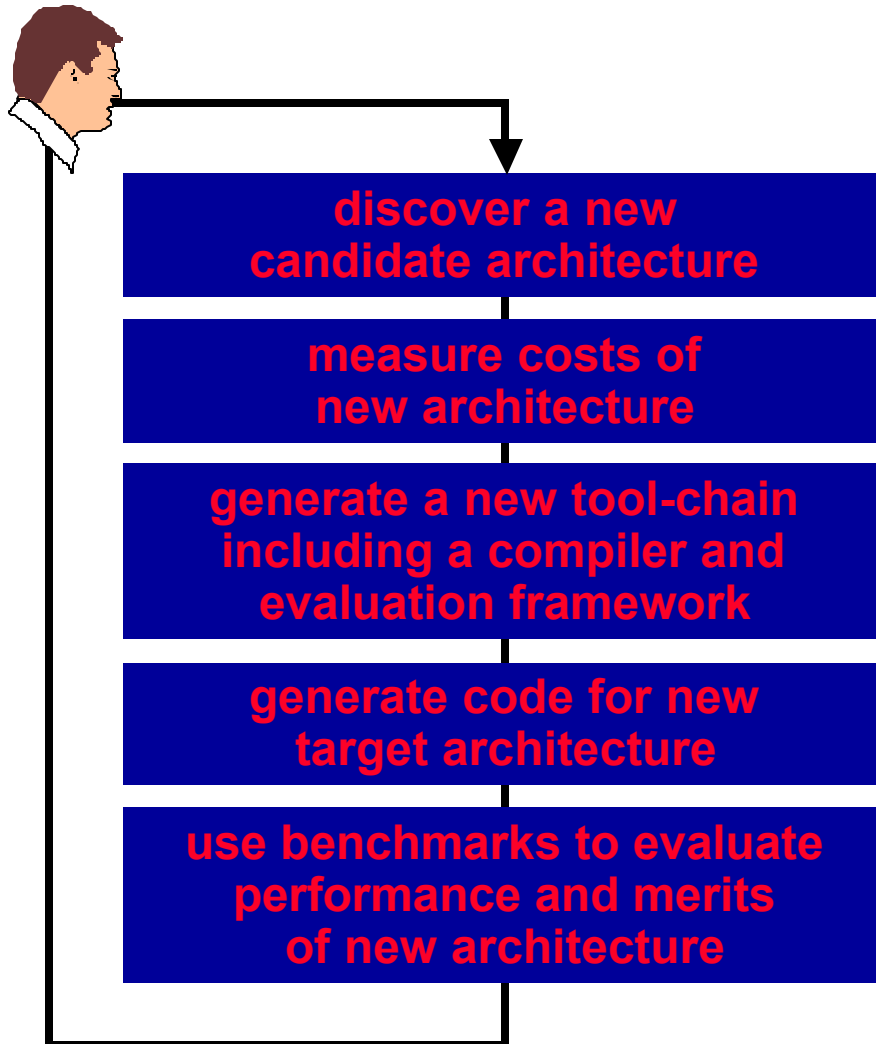
## Report Documentation Page

*Form Approved  
OMB No. 0704-0188*

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1. REPORT DATE <b>21 MAY 2003</b>	2. REPORT TYPE <b>N/A</b>	3. DATES COVERED <b>-</b>		
4. TITLE AND SUBTITLE <b>Design Space Exploration and Optimization of Embedded Cache systems via a Compiler</b>		5a. CONTRACT NUMBER		
		5b. GRANT NUMBER		
		5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S)		5d. PROJECT NUMBER		
		5e. TASK NUMBER		
		5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) <b>Center for Research on Embedded Systems and Technology, Georgia Institute of Technology</b>		8. PERFORMING ORGANIZATION REPORT NUMBER		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSOR/MONITOR'S ACRONYM(S)		
		11. SPONSOR/MONITOR'S REPORT NUMBER(S)		
12. DISTRIBUTION/AVAILABILITY STATEMENT <b>Approved for public release, distribution unlimited</b>				
13. SUPPLEMENTARY NOTES <b>The original document contains color images.</b>				
14. ABSTRACT				
15. SUBJECT TERMS				
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT <b>UU</b>	
a. REPORT <b>unclassified</b>	b. ABSTRACT <b>unclassified</b>	c. THIS PAGE <b>unclassified</b>		18. NUMBER OF PAGES <b>4</b>
				19a. NAME OF RESPONSIBLE PERSON

# High Performance Embedded Processors Conventional Design Flow

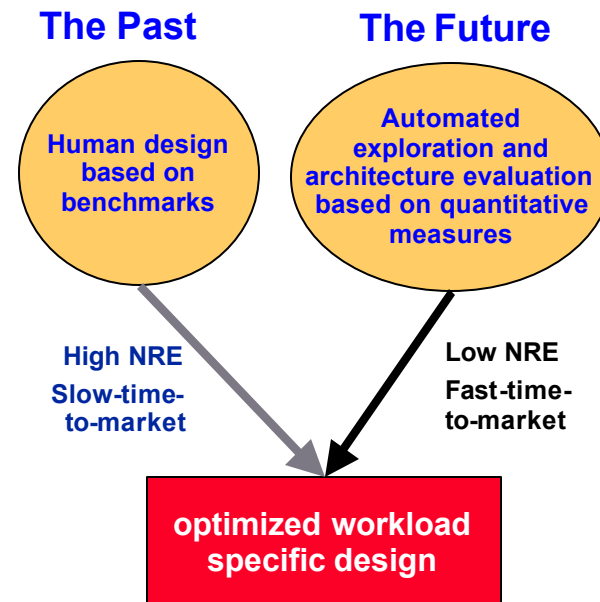
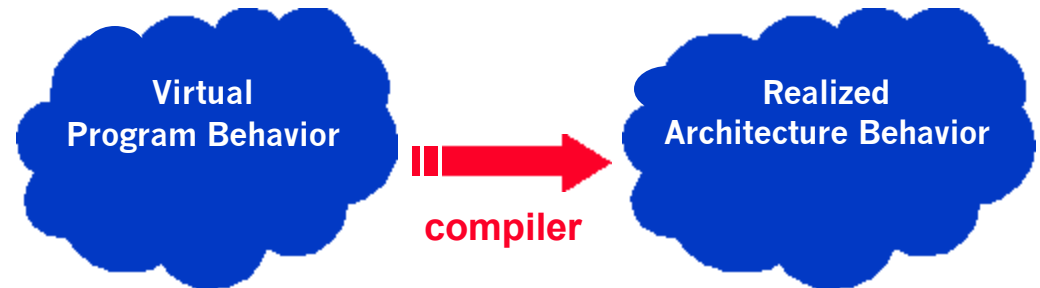


- Current strategy is ad hoc engineering
- *The system engineer is on the critical path*
- High engineering costs
  - How can the lessons learned from one design be used in new contexts?
- Slow time-to-market

# Desiderata – A New Paradigm

- Is it possible to capture, quantify, and characterize the virtual program behavior?
- Is it possible to track or measure the program behavior as a result of the applied compiler optimizations?
- Is it possible to interpret the virtual program behavior in light of an architectural context?
  - Evaluation of the architecture without actual synthesis

## Our Fundamental Philosophy





## *Example Design Space Exploration Via Data Remapping*

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- Remapping reduces the size of the working set and decreases the demand bandwidth of the application
- We may leverage the benefits afforded by data remapping to optimize the architecture
  - Tradeoff cache size and performance
  - Halving of the cache requirements as well as the power consumed while preserving performance goal
- *Systematic exploration of the design space based on quantitative measures*