Design Space Exploration and Optimization of Embedded Cache Systems via a Compiler

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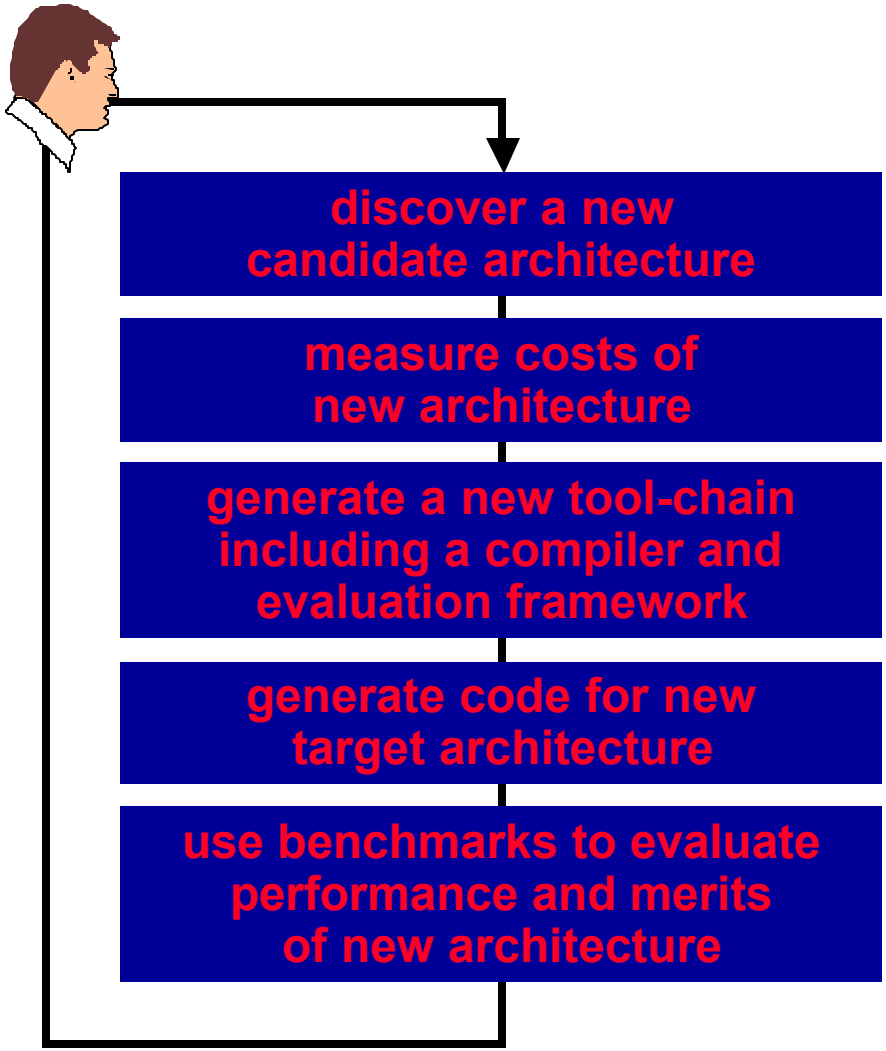
High Performance Embedded Processors Conventional Design Flow

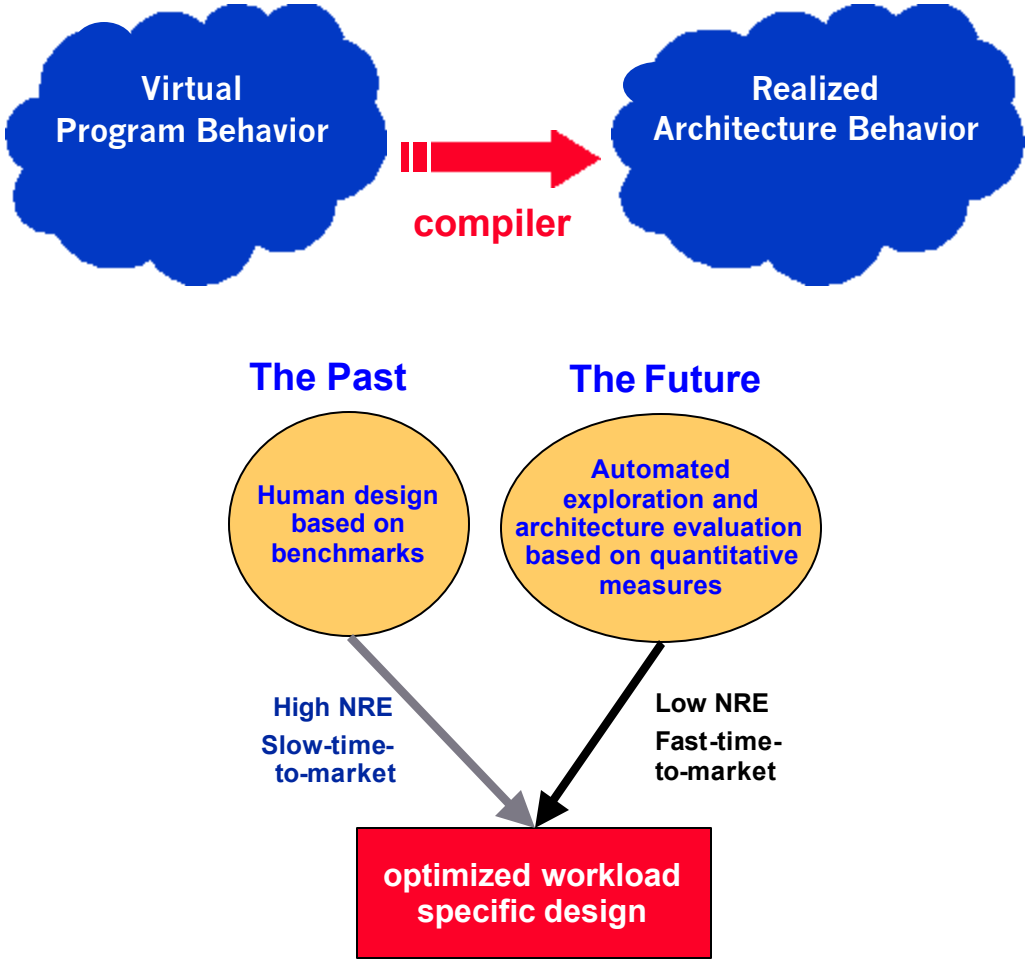


- Current strategy is ad hoc engineering
- *The system engineer is on the critical path*
- High engineering costs
  - How can the lessons learned from one design be used in new contexts?
- Slow time-to-market

Desiderata – A New Paradigm

- Is it possible to capture, quantify, and characterize the virtual program behavior?
- Is it possible to track or measure the program behavior as a result of the applied compiler optimizations?
- Is it possible to interpret the virtual program behavior in light of an architectural context?
  - Evaluation of the architecture without actual synthesis

- Our Fundamental Philosophy



Example Design Space Exploration Via Data Remapping

- Remapping reduces the size of the working set and decreases the demand bandwidth of the application

- We may leverage the benefits afforded by data remapping to optimize the architecture
  - Tradeoff cache size and performance
  - Halving of the cache requirements as well as the power consumed while preserving performance goal

- *Systematic exploration of the design space based on quantitative measures*