



High-Temperature, 400 W, DC-to-AC Inverter Using Silicon Carbide Gate Turn-Off Thyristors and *p-i-n* Diodes

**by C. Wesley Tipton, Stephen B. Bayne, Charles J. Scozzie, Timothy Griffin,
and Bruce Geil**

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Sensors and Electron Devices Directorate, ARL

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14. ABSTRACT A high-temperature, 400 W, DC-to-AC inverter has been developed using silicon carbide gate turn-off thyristors and <i>p-i-n</i> diodes. We demonstrate the inverter driving a three-phase, inductive motor up to 580 W and device case temperatures up to 150° C. The inverter circuit was constructed to perform the first characterization of these SiC devices under significant electrical and thermal stresses, investigate the parametric operating space of the SiC devices, and uncover circuit-related failure modes. We discuss our electrical screening criteria of the SiC components, electrical stresses brought about by circuit topology, component failure modes, and inverter performance. We will use the results of this work in the development of future SiC components.					
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1. Introduction

The intrinsic material properties of silicon carbide (SiC) hold the promise of a new generation of power electronics with expanded operating regimes of temperature, switching frequency, breakdown voltage, and current density. However, material defects, such as micropipes and screw dislocations (*1*), have slowed the proliferation of SiC technology by limiting device performance and yield. Today, SiC wafers can be made with fewer than 1 micropipe/cm², making devices for applications requiring high power density and high operating temperatures feasible. The promise of high-temperature operation (case temperatures of greater than 150 °C) and increased efficiency make SiC an important technology for both military and commercial power conversion and control applications.

Over the last few years, many researchers have characterized *single* SiC devices or mixed-technology circuits (in which a silicon power switch e.g., MOSFET or IGBT is combined with a SiC diode) as part of the SiC device development process (*2–11*). However, there have been few reports that address issues related to the implementation of SiC-based circuits for specific applications and even fewer that address the safe operating areas (SOA) of SiC devices or their reliability at these operational boundaries. The first report of an all-SiC 3-phase, DC-AC inverter was presented by Seshadri, et al. (*12*) in 1999. Although Seshadri's inverter used SiC gate turn-off thyristors (GTOs) and *p-i-n* diodes, it was operated at ambient temperature and at voltage and current levels so low that the authors were unable to "...determine typical switching characteristics of the individual SiC components." Clearly, there exists a need to evaluate SiC technology under relevant circuit stresses.

We have demonstrated a DC-AC inverter using 4H-SiC GTOs (in GTO mode) and *p-i-n* diodes driving three-phase, inductive loads up to 580 W and device case temperatures up to 150° C. The inverter circuit described in this article was constructed to characterize the performance of SiC devices under relevant circuit stresses, investigate the parametric operating space of the SiC devices, and uncover circuit-related failure modes. We discuss our electrical screening criteria of the SiC components, electrical stresses brought about by circuit topology, component failure modes, and inverter performance.

2. Background

2.1 DC-to-AC Inverter

A simplified schematic of the switching section of a three-phase inverter is given in Figure 1. This circuit consists of three, half-bridge sub-circuits each of which has two switches (S) and two antiparallel diodes (D). In each leg (A, B, or C), only one switch (e.g., S_1 or S_2) is active at any given time and the output of each half-bridge, V_{AN} for example, depends only on the input bus voltage (V_I) and the state of the switches. When driving inductive loads, the antiparallel diodes provide an alternate current path once a switch has been turned off. Sinusoidal, pulse-width modulation (PWM) control techniques are often employed to produce an alternating current from the DC bus. Conceptually, the sine wave is approximated by comparing a high-frequency triangular wave with the desired low-frequency sine wave. The resultant waveform is a PWM control signal that can be applied to the upper switch and its complement is applied to the lower switch of one of the inverter's legs. To generate three-phase outputs, three low-frequency sine waves (displaced by 120°) are used to generate the six PWM control signals.

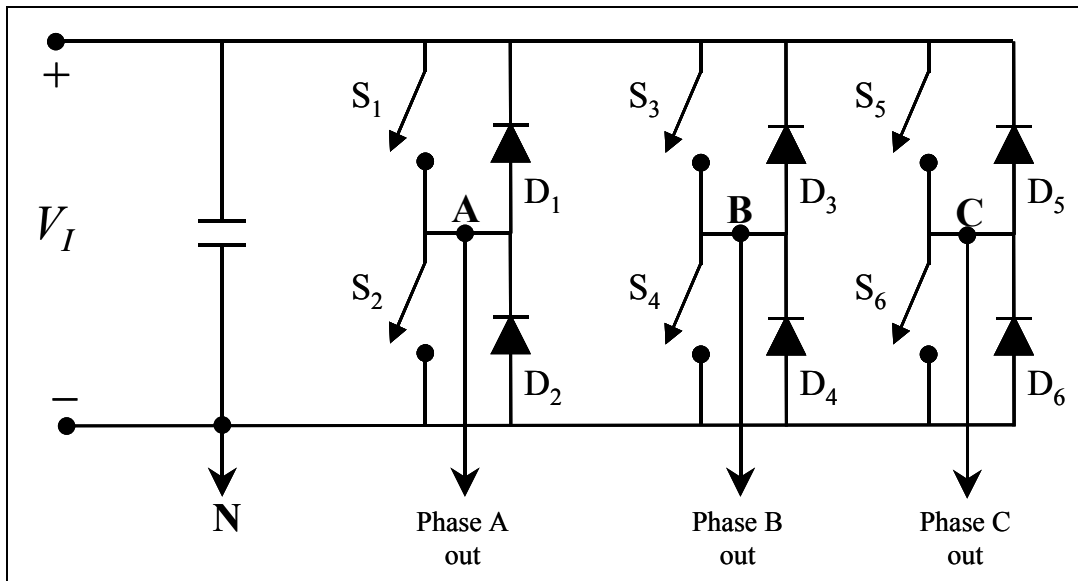


Figure 1. Simplified three-phase, full-bridge DC-AC inverter circuit.

2.2 SiC Gate Turn-off Thyristor and SiC p - i - n Diode

As noted above, the switching devices in this DC-AC inverter are SiC GTOs. An idealized cross section of the 4 mm^2 (anode mesa area) GTO is given in Figure 2. This device was designed and fabricated by CREE Inc. to provide 1200 V forward blocking voltage and a maximum controllable current density of 500 A/cm^2 (or 7 A based on an active area of 37% of the total mesa area). As these devices are asymmetric, their reverse blocking voltage is limited to 250 V. The junction termination extension (JTE) reduces the electric field crowding at the edges of the

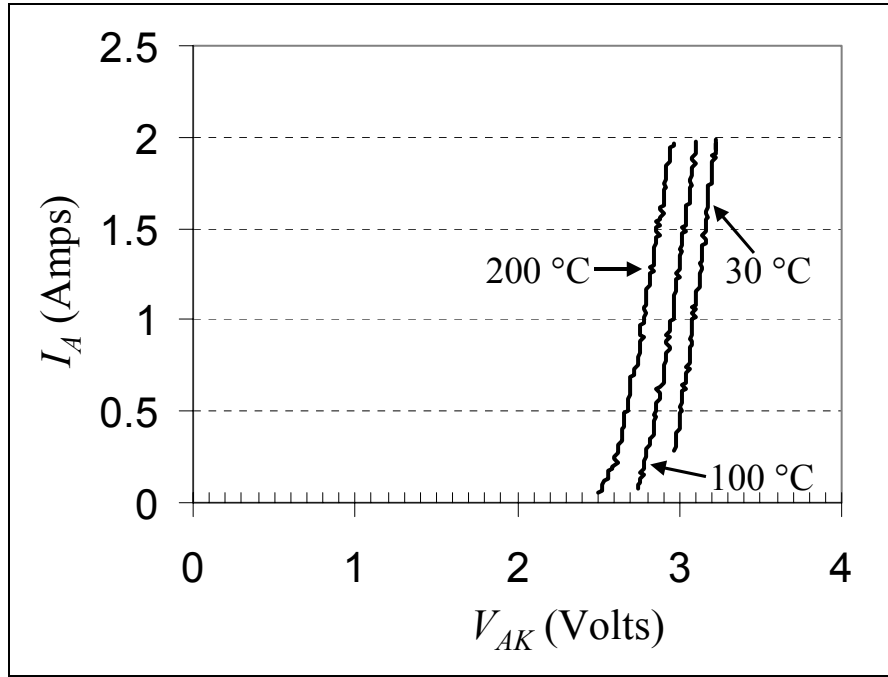


Figure 3. Typical forward-conducting characteristics of the SiC, 4 mm² GTO.

Figure 4 shows the forward conduction characteristic of a typical SiC *p-i-n* diode as a function of case temperature. The turn-on voltage decreased from 3 to 2.6 V as the case temperature increased from 25 ° to 250 °C. The diodes were screened to ensure a forward blocking-voltage of at least 800 V with a leakage current of no greater than 5 μA. Further information relating to the CREE SiC *p-i-n* diodes used in this work can be found in (16,17).

To operate at high voltages, we initially encapsulated the SiC diodes and GTOs with Duralco 4460 low viscosity coating using a curing temperature profile of 4 hours at 110 °C followed by 4 hours at 175 °C. We found, however, that the encapsulant caused a failure mode in the GTO that was not present in the diode. Figure 5 compares the forward blocking characteristic of a GTO before and after the encapsulation process. Before encapsulation, the blocking voltage was in excess of 800 V. (Typically, forward blocking screenings were performed to 800 V although limited testing found that devices exceeded 1800 V.) After encapsulation, the blocking voltage dropped below 50 V. Based on our characterizations, we hypothesize that the GTO's passivation material(s) are degraded by the encapsulation, which in turn provides a leakage current path between the cathode and gate regions (refer to Figure 2). Because of these results, GTOs used in the inverter circuit were not encapsulated and we therefore limited maximum operating voltages to 600 V (450 V supply voltage and 150 V inductive overshoot).

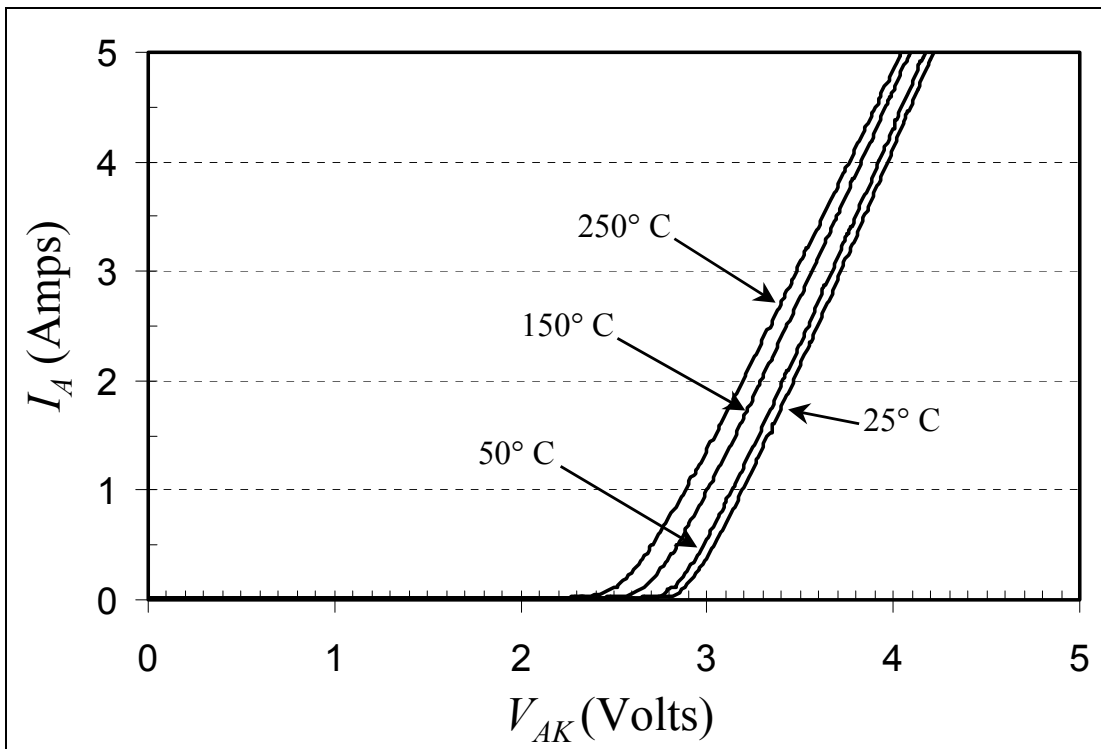


Figure 4. Typical forward-conducting characteristics of the SiC, 1 mm² *p-i-n* diode.

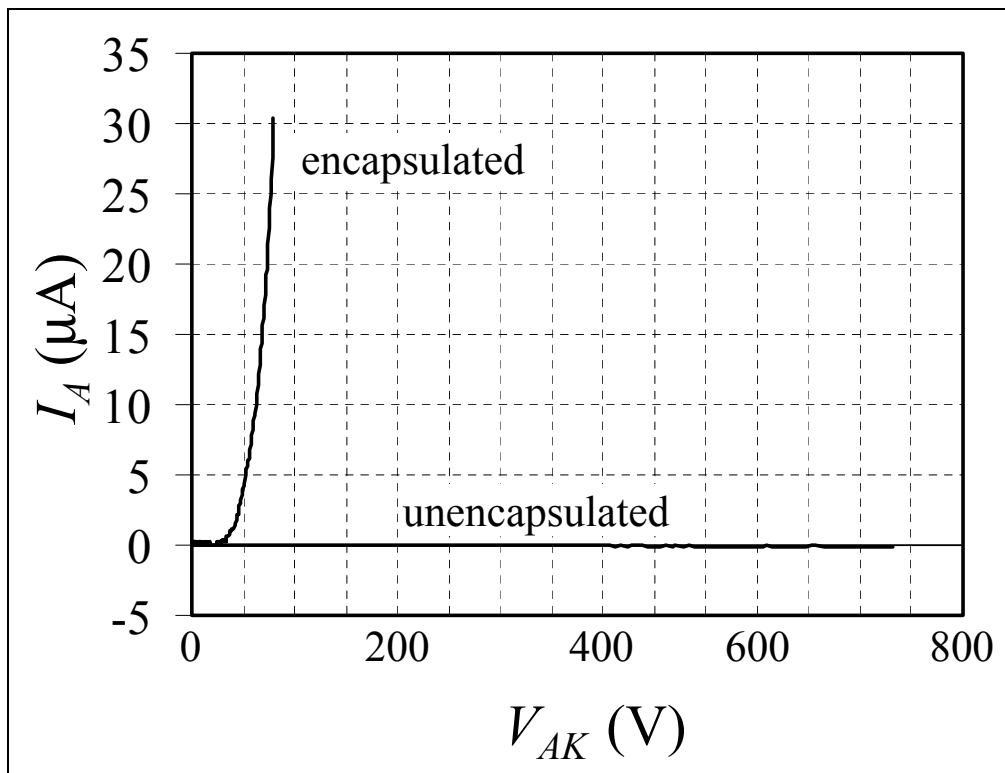


Figure 5. GTO forward-blocking voltage degradation due to encapsulation.

3. Inverter Implementation

A block diagram of the SiC inverter circuit is shown in Figure 6. The primary DC power supply was varied between 0 and 600 V and was “stiffened” with a 500 μF capacitor. We used a Motorola ITC137 motion control development board to generate the PWM pulses for the GTO gate drivers. The PWM signals were generated under open-loop control (no feedback between motor and controller), and had a switching frequency (f_s) of 2 kHz. We synthesized the output waveforms using a 1024-point look-up table that contained the values of the first quadrant of the sine function. The switching frequency determined the number of points from the table that were used to generate the sinusoidal output, while the drive frequency (0 to 60 Hz) was determined by the rate at which the values from the table were output to the drive electronics. Due to the GTO’s drive-current requirements, a custom gate-drive circuit was designed to interface the PWM controller with the GTOs. This circuit operated the GTOs using a turn-off gain of 1 and a turn-on gain of 7. We isolated the gate drive circuit from the PWM driver board by an optocoupler and its output stage consisted of two, silicon MOS transistors connected in a push-pull configuration. High-voltage isolation of the gate-drive circuit from the bridge circuit was accomplished using DC-DC converters—two 12V, 60W converters (PICO LPA120) were used on each gate-drive circuit to produce the bipolar GTO gate currents.

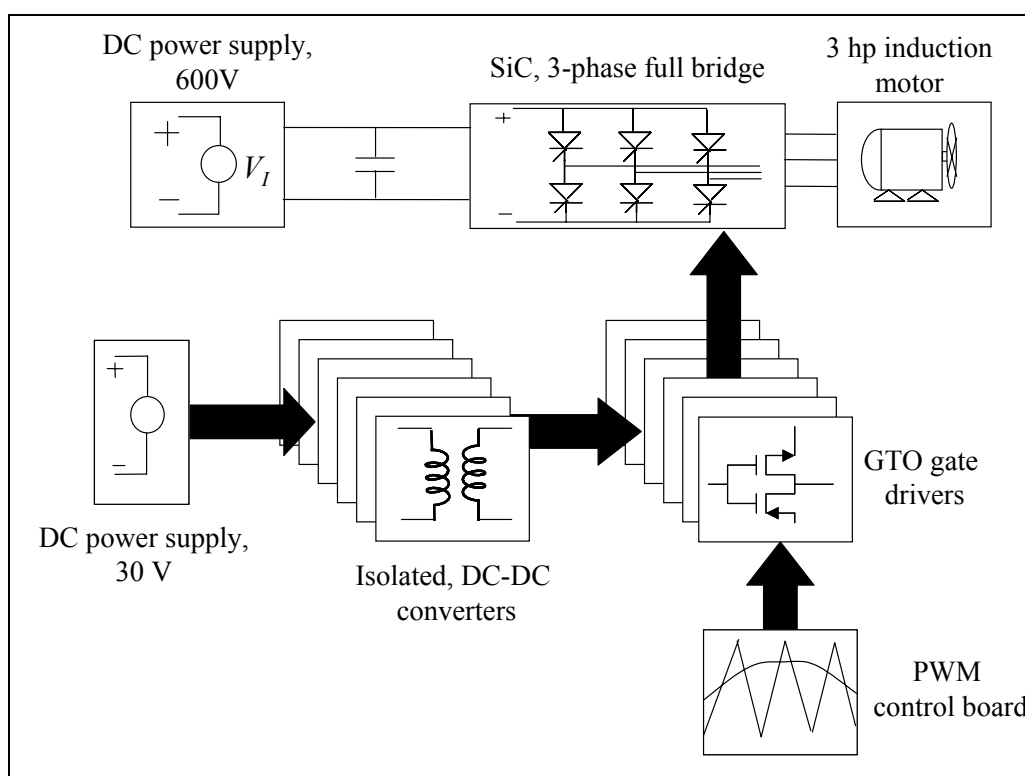


Figure 6. Block diagram of DC-AC inverter.

Figure 7 shows a schematic of the three-phase, full-bridge circuit consisting of the SiC GTOs and diodes, turn-on snubbers (SN_{on}), and turn-off snubbers (SN_{off}). The GTOs and antiparallel diodes were mounted on a heat sink and were electrically isolated by a 0.01" layer of muscovite mica.

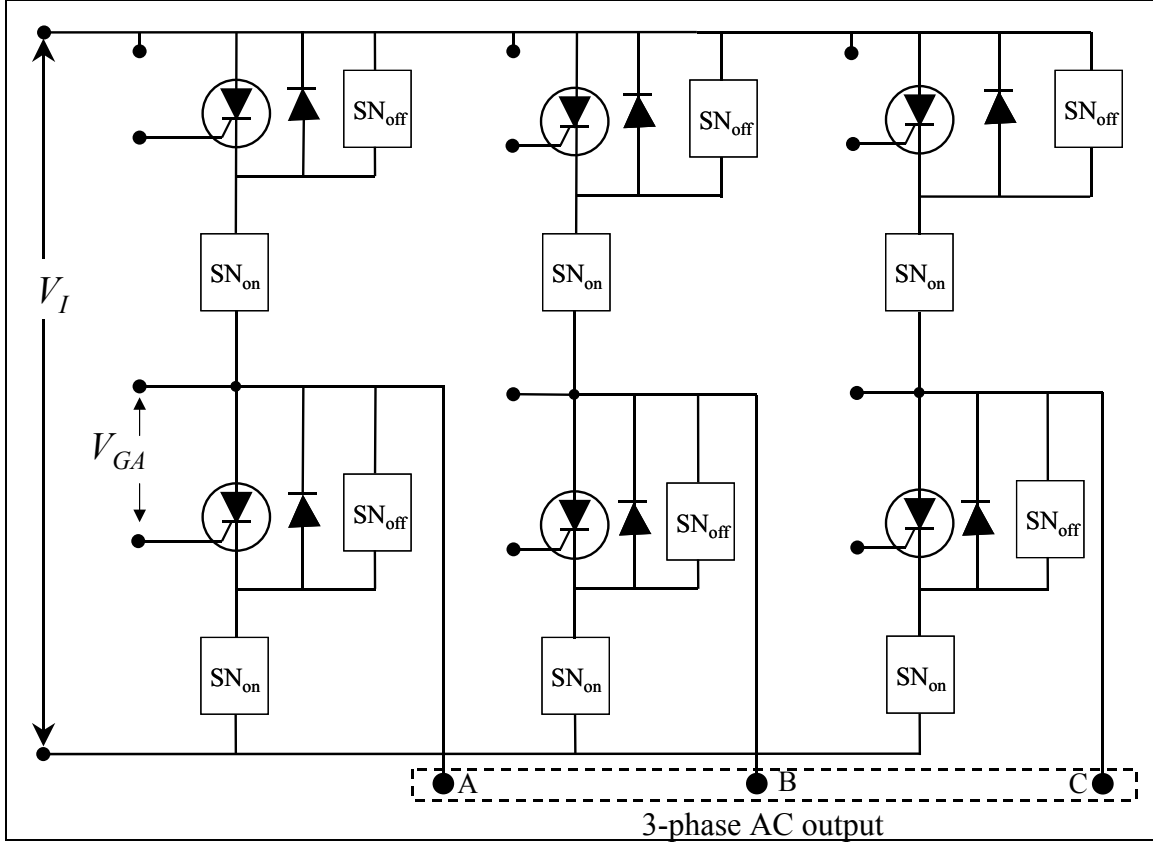


Figure 7. Simplified DC-AC inverter circuit schematic.

The bridge circuit topology requires that the designer prevent the input power bus from being directly shorted by the switching elements. To avoid the short-circuit condition in the present circuit, two parameters must be properly designed. The first design consideration is the possibility of exceeding the maximum rate of rise of the V_{AK} , such that a GTO being turned off is inadvertently latched on. In the forward-blocking state, the center junction (J_2 of Figure 2) of the GTO is reversed biased and therefore has a small junction capacitance that dominates all other internal capacitances. For a sufficiently large voltage transient across this junction capacitance, a displacement current will be produced that satisfies the conditions for turn-on (18). To prevent this mode of turn-on, a turn-off snubber circuit was implemented to limit the rise-time of V_{AK} . The turn-off snubber circuit shown in Figure 8(a) was designed to limit the dV_{AK}/dt to 200 V/ μ s. The turn-off snubber capacitance (C_{off}) is given by

$$C_{off} = I_M t_f / (2V_I) , \quad (1)$$

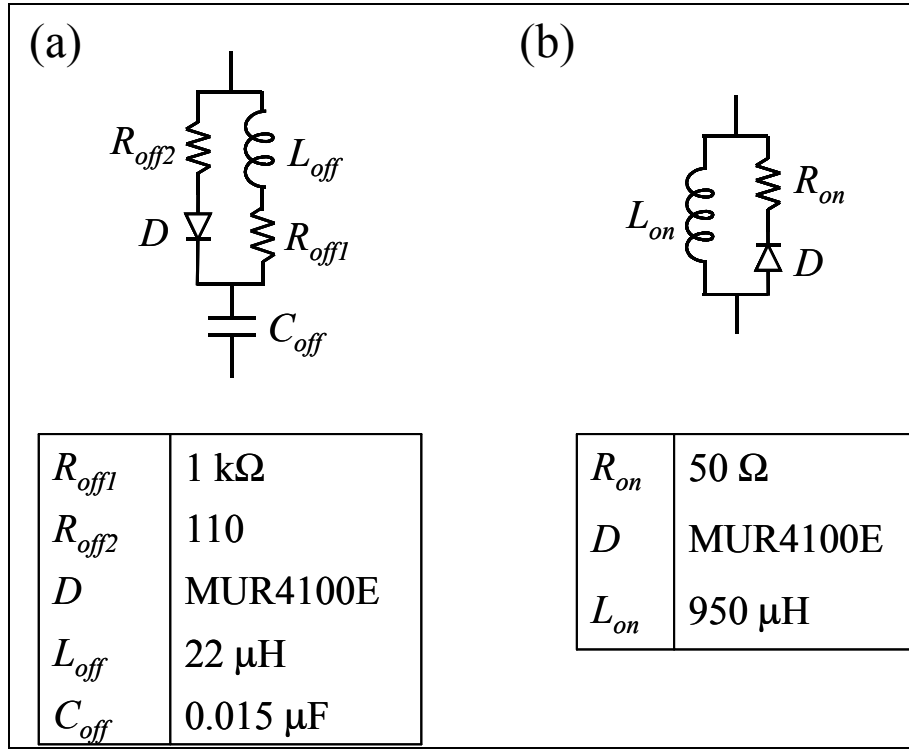


Figure 8. Snubber circuits: (a) turn-off and (b) turn-on.

where I_M is the maximum current through the GTO and t_f is the anode current's fall-time (19). For a capacitance value greater than C_{off} , the GTO voltage rises more slowly and takes longer than t_f to reach V_L . The value for C_{off} used in the snubber circuit was 0.015 μ F. The value of the snubber resistor (R_{off1}) was chosen so that the current through it is 20% of I_m or

$$R_{off1} = V_L / 0.2 I_M . \quad (2)$$

The value for R_{off1} used in the snubber design is 1k Ω . For the turn-off snubber to be effective, the minimum on-time of the switch should be greater than the capacitor's discharge time so that the capacitor's voltage can discharge to $\approx 0.1 V_L$ before the beginning of the next switching cycle; therefore, the minimum on time for the GTO should be

$$t_{on} > \ln(10) R_{off1} C_{off} . \quad (3)$$

Based on Equation 3, we programmed the PWM pulse widths to produce a maximum on-time of 470 μ s and a minimum on-time of 30 μ s to avoid the possibility of incomplete switching. Due to circuit topology, as the upper GTO is turned on and its V_{AK} decreases, the lower GTO's V_{AK} increases at this same rate. The opposite effect occurs during turn-off. If the upper device's slew rate (dV_{AK}/dt) is allowed to be large during turn-off, there is a possibility that the lower GTO will be inadvertently latched on. The resistor R_{off2} was added in series with the snubber diode to increase the charging time of C_{off} . Inductor L_{off} limits the peak current through the GTO during turn-on.

The second design consideration is the *dead time* associated with the PWM control signals. The dead time is the time interval between turning off the upper GTO and turning on the lower GTO (or vice versa) in the same half-bridge and is determined by the device turn-off time and snubber decay times. Catastrophic GTO failure would occur if both devices in one half-bridge were to conduct simultaneously. The PWM control software was modified to produce a conservative, 15 μ s dead time.

A reliability consideration for thyristors is that of exceeding a critical value of dI_K/d_t during turn-on. The turn-on process begins with the formation of excess-carrier density areas near the gate regions. These regions spread laterally until the entire cross-sectional area of the GTO is filled with excess carriers. If a large current is allowed to flow early in the turn-on process, localized heating could damage or destroy the device. In half-bridge circuits, a turn-on snubber should always be used when a turn-off snubber is used because large transient currents arise from C_{off} . When the upper switch in the half-bridge is turned on, a capacitive charging current from the lower device's snubber capacitor flows through the upper device. The capacitive current causes extra stress on the device; therefore a turn-on snubber is used to limit the capacitive charging current. The turn-on snubber circuit shown in Figure 7(b) was designed to limit the slew rate to 50 A/ μ s. The snubber inductor L_{on} minimizes transient currents through the GTO; however, a large inductance will cause excessive voltage transients on the GTO at turn off. When selecting the value of resistor R_{on} , consideration must be taken for the decay time of the inductor. During turn-off, the inductor's current should decay to $0.1I_M$ so that the snubber will be effective during the next turn-on cycle. The equation for the minimum turn-off time (t_{off}) is

$$t_{off} > \ln(10)L_{on}/R_{on} \quad (4)$$

Both turn-on and turn-off snubber circuits used the MUR 4100E fast-recovery silicon diode. A detailed design procedure for snubbers can be found in (19).

The demonstration load was a three-phase, 60 Hz, two-pole, 3 hp, 460 V induction motor having a full-load speed of 3475 rpm and a full load current of 3.8 A (rms). The mechanical load for the motor was a direct-drive fan. The power (P_{inv}) delivered to the motor by the inverter, which includes the losses in the motor and the mechanical power delivered to the fan, is given by

$$P_{inv} = \sqrt{3}V_{LL}I_L \cos(\Theta) \quad (5)$$

where V_{LL} is the line-to-line voltage, I_L is the line current, and $\cos(\theta)$ is the power factor of the motor. The power factor is a function of load and at full load is 0.89, at three-quarter load is 0.85, at one-half load is 0.76, and at one-quarter load is 0.56.

Based on Equation 5 and assuming full load, the inverter would be required to deliver 2695 W of power to the motor (steady-state). Although this steady-state power requirement is within the capability of the 4 mm² GTO, there are several issues that limited the demonstration power level. Based upon the motor's design, its starting current can be significantly greater than the steady-

state value. For example, the starting current of the demonstration motor is 34 A (rms) or 48 A (peak) which is an order of magnitude greater than the 4 mm² GTO can control! One method of reducing the starting current is to gradually increase the line voltage and frequency to their full power values. Note, however, that the line frequency must be increased proportionally to the line voltage. Otherwise, the motor's core will saturate and excessive magnetization currents will flow, thereby causing switch failure. In practice, the open-loop, soft starting technique is plagued by an instability attributed to electro-mechanical energy resonance (20). The instability manifests itself as an oscillation in motor speed (and line current) usually occurring at low frequencies and light loads and depends on many system parameters such as f_s , motor geometry, motor core loss, and line voltage. In the present system, we found that the instability occurred at a drive frequency of ≈ 30 Hz and a DC bus voltage of 350 V. The instability, therefore, required us to limit the demonstration power levels so that the GTOs would not be destroyed.

During inverter operation, currents were monitored using Tektronix P5207 current probes and voltages were monitored using Tektronix P5205 differential voltage probes.

4. Results and Discussion

In the subsequent discussion of data, we first present the overall operation of the inverter and then detail the performance of the SiC components. To study operation at elevated temperatures, the case temperatures of the GTOs and SiC diodes were regulated from 50 ° to 150 °C. Figure 9 shows the three-phase sinusoidal output currents of the inverter circuit operating at 150 °C at a peak value of ≈ 2.5 A. During the course of our evaluations, a maximum peak-output current of 3.5 A was obtained at a case temperature of 50 °C, frequency of 30 Hz, and DC bus voltage of 350 V. To estimate the power delivered by the inverter at 150 °C, we begin by calculating the PWM-generated sinusoidal line voltage. The line voltage may be estimated as

$$V_{LL} \approx V_I(0.6m_a), \quad (6)$$

where m_a is the PWM amplitude modulation factor (17). Using Equation 6, a value of 0.8 for m_a , and a bus voltage of 350 V, we find V_{LL} to be 168 V (rms). (Note that 168 V is the line voltage supplied to the motor whereas the SiC components are stressed at the DC bus voltage of 350 V.) Using Equation 5, a peak line current of 2.5 A, and a power factor of 0.8, we estimate P_{inv} to be 400 W. A similar calculation for the maximum achieved power at 50 °C gives P_{inv} to be 580 W.

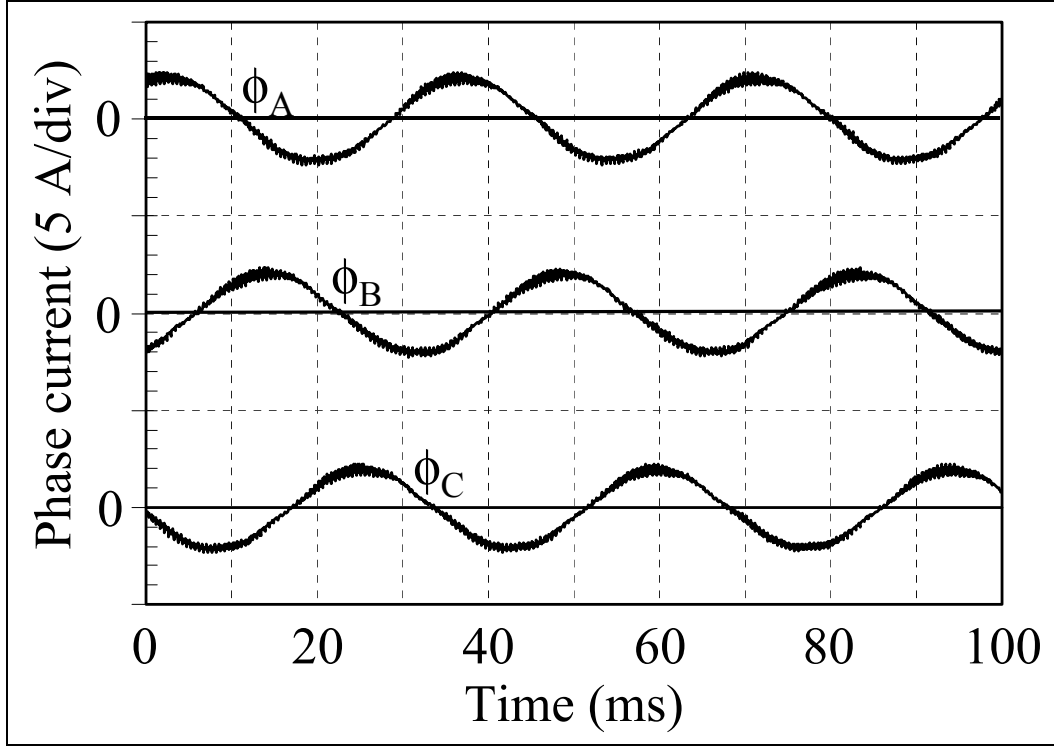


Figure 9. Three-phase line currents of a 3-hp induction motor with SiC devices operated at a DC bus voltage of 350 V and case temperatures of $\approx 150^\circ\text{C}$.

Figure 10 shows the switching waveforms for the lower GTO in the “A” phase of the inverter circuit operated at 50°C case temperature. The upper waveform shows the cathode current peaking at 3.6 A with rising and falling slew-rates of 0.1 and $1.7\text{ A}/\mu\text{s}$, respectively, and the second waveform shows the corresponding V_{AK} . When the GTO is switched off (e.g., at $180\text{ }\mu\text{s}$), the voltage across the device rises to a peak value of $\approx 550\text{ V}$ due to stray inductance in the circuit; and after $125\text{ }\mu\text{s}$, decays to 300 V. The turn-on dV_{AK}/dt is $-300\text{ V}/\mu\text{s}$ and the turn-off dV_{AK}/dt is $150\text{ V}/\mu\text{s}$. The lower two waveforms in Figure 10 show the gate current (I_G) and gate-anode voltage (V_{GA}). The device turns on with a gate current of -0.48 A , which corresponds to a turn-on gain of 7.3. The maximum gate current at turn-off was 3.5 A, which corresponds to a turn-off gain of 1. At turn-on, the gate-anode junction is forward biased at a V_{GA} of -3.2 V .

Figure 11 shows a series of waveforms characterizing GTO turn-off. Figure 11(a) shows V_{GA} along with I_G and the cathode current (I_K). Initially, the GTO was conducting 1 A. At $3.5\text{ }\mu\text{s}$, a turn-off voltage of +12 V was applied to the gate. We note a transient gate current of 2.5 A even though a turn-off gain of 1 only requires a peak I_G of 1 A. However, the gate current is not flowing exclusively in the gate-anode path as evidenced by a transient current (I_{trans}) observed flowing through the GTO’s cathode. We complete the analysis of the current path of I_{trans} with the data of Figure 11(b). Though not for the same PWM cycle, this data shows that I_{trans} also flows through the antiparallel diode as indicated in Figure 12. When the antiparallel diode was removed from the circuit, I_{trans} was also eliminated. We attribute I_{trans} to the diffusion capacitance of junction J_2 .

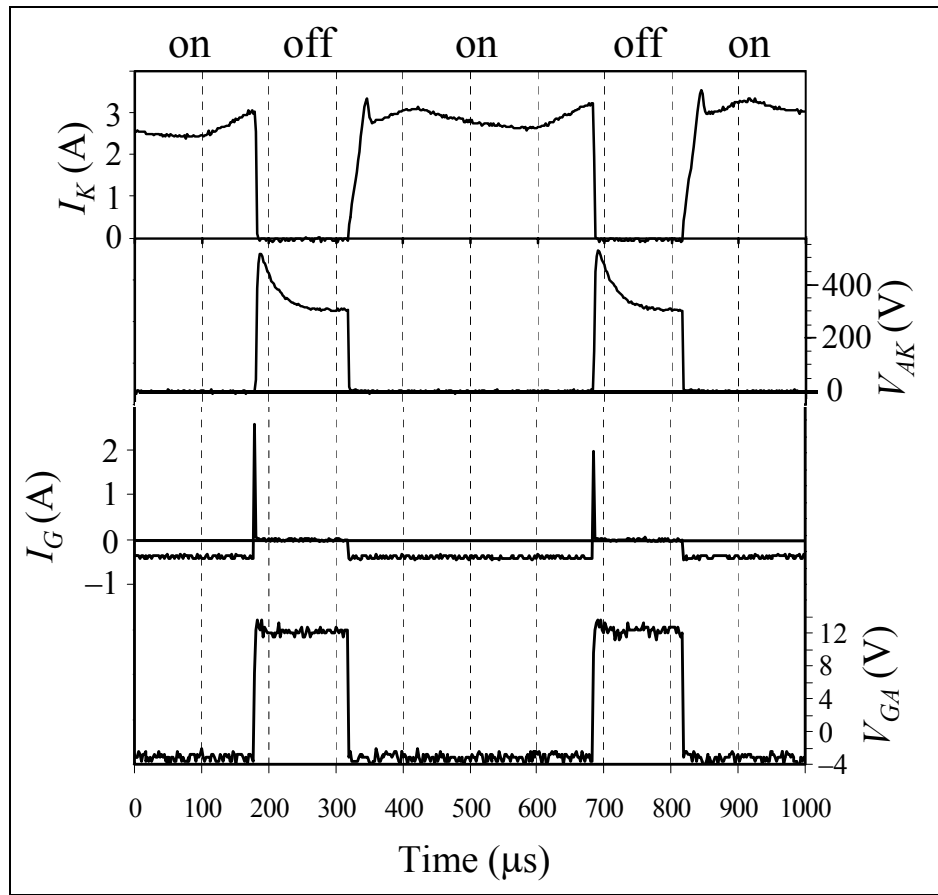


Figure 10. Characteristic GTO waveforms during a portion of the PWM switching sequence.

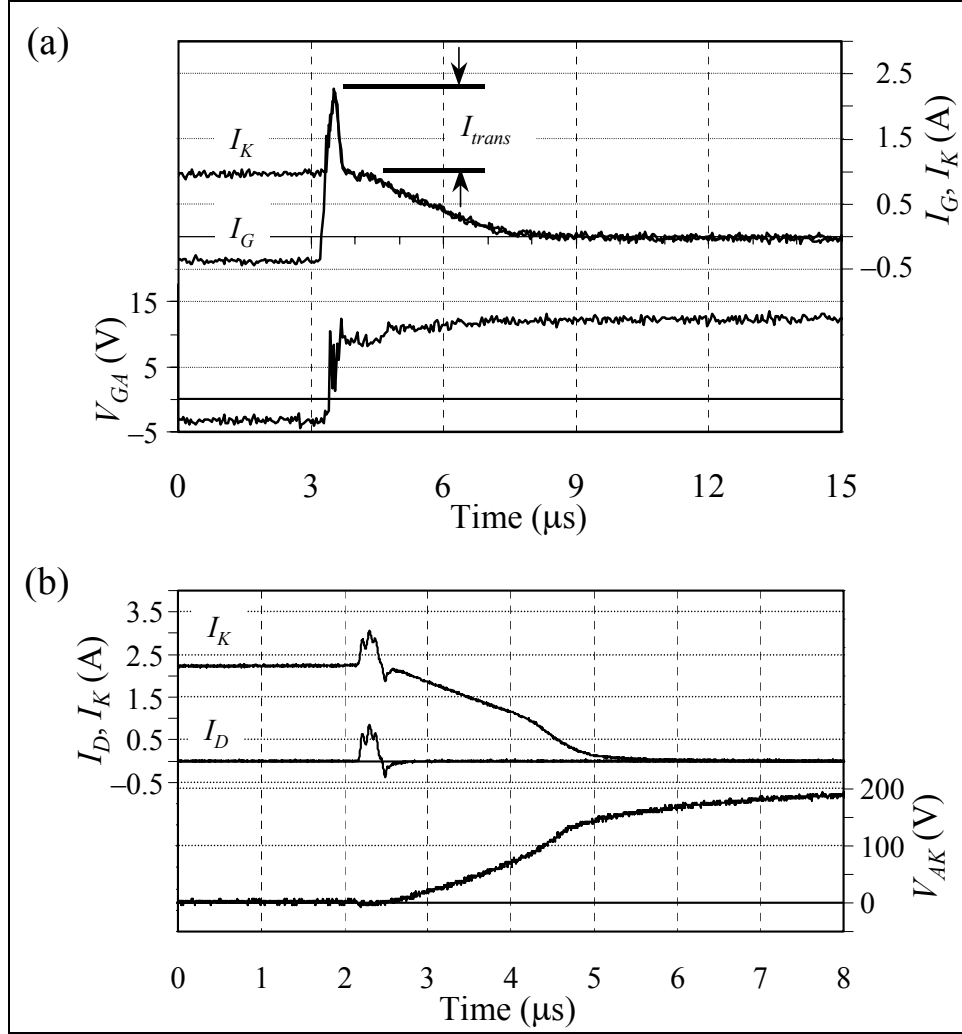


Figure 11. Transient current observed in the (a) GTO and (b) antiparallel diode.

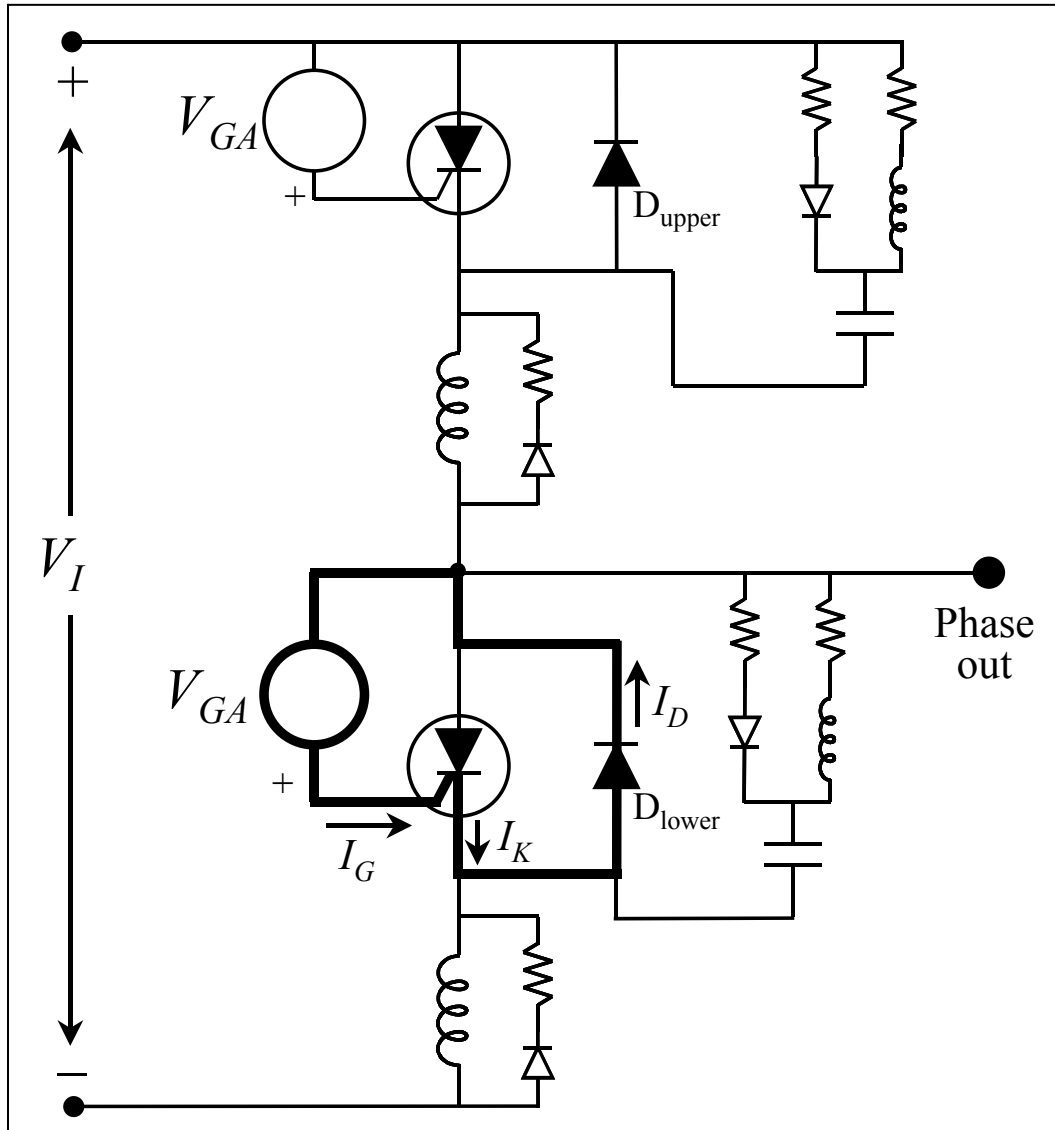


Figure 12. Path of the transient current observed during GTO turn off.

We also investigated the switching interaction between GTOs and the antiparallel diodes. Figure 13 shows the following waveforms for a single phase of the inverter circuit: lower GTO cathode current $I_{K(Lower)}$, upper antiparallel diode current ($I_{D(Upper)}$), anode-cathode voltage of the upper GTO ($V_{AK(Upper)}$), and the upper GTO cathode current ($I_{K(Upper)}$). Initially, the upper GTO is blocking 300 V, the lower GTO is conducting 3 A, and the upper diode is reverse blocking. At 190 μ s, the lower GTO is turned off and the upper diode goes from reverse blocking to conducting. The voltage across the upper GTO is now the on-state voltage of the upper diode (≈ 3.2 V). At 210 μ s, the upper GTO is turned on; however, most of the load current continues to flow through the upper diode. At 300 μ s, the upper GTO is turned off and I_{trans} can be seen in the $I_{D(Upper)}$ and $I_{K(Upper)}$. At 350 μ s, the lower GTO is turned on and I_D is commutated from the upper diode to the lower GTO. Because the snubbers and inductive load limited dI_k/dt , no reverse recovery current was observed in the antiparallel diodes when current was commutated from the diodes to the GTOs.

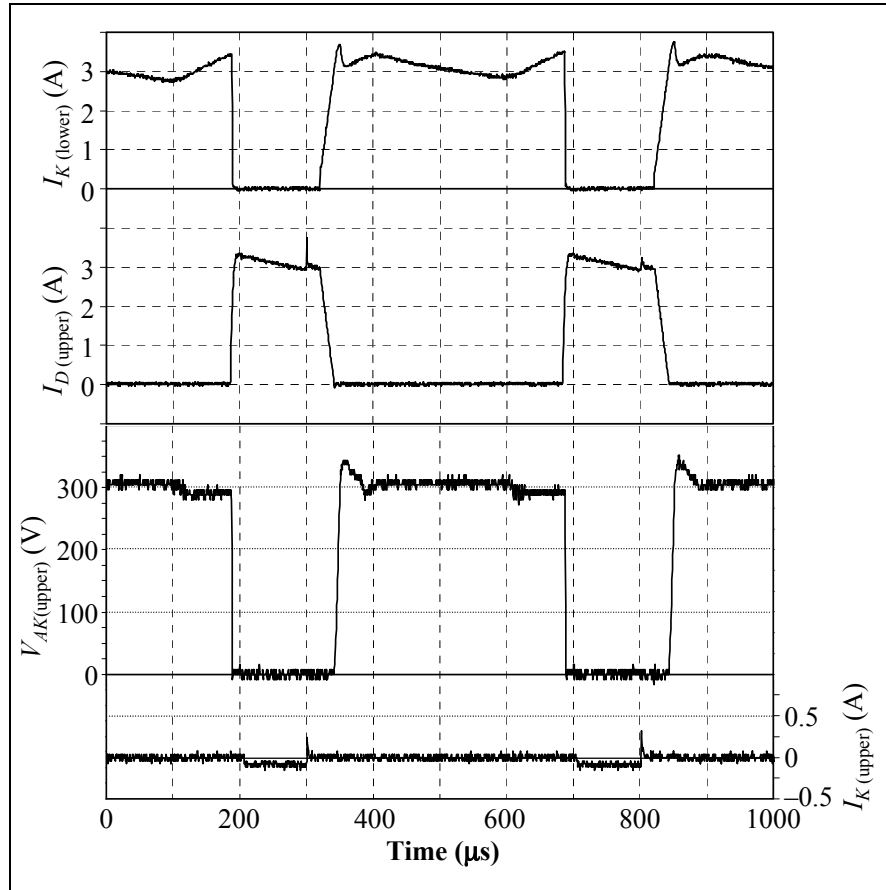


Figure 13. Half-bridge inverter switching waveforms.

Figure 14(a) shows the instantaneous power dissipated in a typical GTO (defined as the on-state V_{AK} multiply by I_K) operating at 300 V and conducting 3.5 A. (The high frequency, low-level noise in this figure is an artifact of the resolution of the digital oscilloscope.) During the turn-off process, the peak power dissipated in the device is 370 W with a pulse width (full width, half

maximum, t_{FWHM}) of $\approx 2 \mu\text{s}$. In our circuit, turn-off power transients dominate the switching losses because the snubber circuits allow the voltage across the device to fall before the current starts to rise. The average switching power loss is approximated as

$$P_s \approx V_I I_m t_{FWHM} f_s \quad (7)$$

and, using the data of Figure 14(a), is found to be 4 W. The average conduction power loss can be similarly approximated by

$$P_c \approx V_{on} I_m t_{on} f_s, \quad (8)$$

where t_{on} is the average, per-cycle on-time of the GTO and V_{on} is the on-state V_{AK} . Since this is a PWM system, we take t_{on} to be the average conducting pulse width of $220 \mu\text{s}$ and using Figure 14(a), find P_c to be 5 W. During switching, power is also dissipated in the GTO gate as shown in Figure 14(b). The power dissipation shown in this figure was taken for an I_K of 3 A. During turn-off, the peak power dissipated in the gate is 18 W with a pulse width of $2 \mu\text{s}$. The average conduction power dissipated in the device is 0.7 W and the total average power dissipated in the gate is 0.8 W.

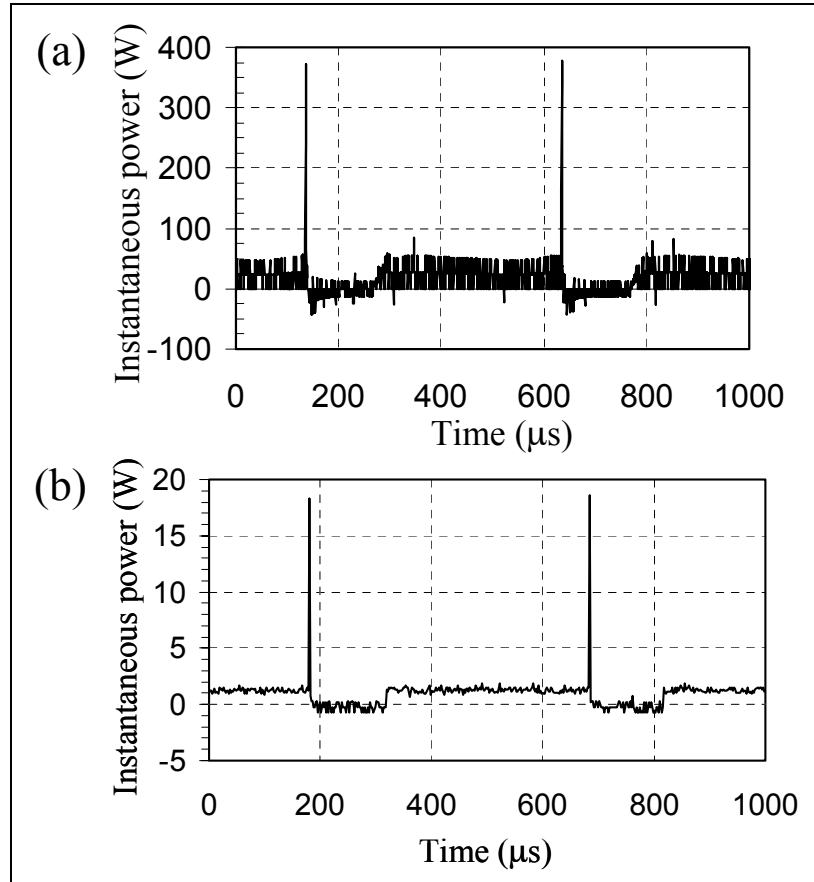


Figure 14. Instantaneous power dissipation in a typical GTO: (a) anode-cathode path and (b) gate-anode path.

5. Summary

We have performed the first demonstration of an all-SiC DC-AC inverter (using SiC power switches and SiC diodes) operated in excess of 400 W and at case temperatures of approximately 150° C. Two factors, related to the system's implementation, limited the operational power levels of this circuit. The first factor, load instability, caused excessive current spikes and GTO failures and can be corrected by using a closed-loop PWM controller. The second limiting factor was a packaging-induced GTO failure. Given that unencapsulated GTOs were operated without this type of failure, higher power operation can be achieved through hermetic packaging of the GTOs. In summary, we have found that SiC device technology is at a state of maturity whereby practical circuits can now be implemented. It is our hope that many more SiC circuits will be implemented by the power electronics community so that the performance and reliability of this technology can be optimized.

References

1. Trivedi, M.; Shenai, K. Performance of Silicon Carbide Devices in Power Converters. *Energy Conversion Engineering Conference and Exhibit (IECEC) 35th Intersociety*, **July 2000**, 1, pp 37–46.
2. Trivedi, M.; Shenai, K. Practical Limits of High-Voltage Thyristors on Wide Band-Gap Material. *J. of Appl. Physics*, **2000**, 88 (12), pp 7313–7320.
3. Wright, W.; Carter, J.; Alexandrov, P.; Pan, M.; Weiner, M.; Zhao, J. H. Comparison of Si and SiC Diodes During Operation in Three-Phase Inverter Driving AC Induction Motor. *IEEE Electron Device Letters*, **2001**, 37 (37), pp 787–788.
4. Wondrak, W.; Held, R.; Niemann E.; Schmid, U. SiC Devices for Advanced Power and High-Temperature Applications, *IEEE Trans. Industrial Electronics*, **2001**, 48 (2).
5. Garuda, V. R.; Kazimierczuk, M. K.; Ramalingam, M. L.; Tunstall, C.; Tolkkinen, L. High Temperature Performance Characterization of Buck Converters Using SiC and Si Devices, *IEEE Power Electronics Specialists Conference*, **1998**, 2, pp 1561–1567.
6. Katulka, G. L.; Hepneer, D. J.; Davis, B.; Irwin, D. E.; Ridgley, M.; Kornegay, K. Characterization of Silicon Carbide and Commercial-Off-The-Shelf (COTS) Components for High-G Launch and EM Applications, *IEEE Trans. Magnetics*, **2001**, 37, pp 248–251.
7. Shenai K.; Neudeck, P. G. Performance Evaluation of Silicon Carbide Devices in Power Converters, *Energy Conversion Engineering Conference and Exhibit, (IECEC) 35th Intersociety*, **2000**, 1, pp 37–46.
8. Weizel, C. E.; Palmour, J. W.; Carter, Jr., C. H.; Moore, K.; Nordquist, K. J.; Allen, S.; Thero; C.; Bhatnagar, M. Silicon Carbide High-Power Devices, *IEEE Trans. Electron Devices*, **1996**, 43, pp 1732–1741.
9. Siergiej, R. R.; Casady, J. B.; Agarwal, A. K.; Rowland, L. B.; Seshadri, S.; Mani, S.; Sanger P. A.; Brandt, C. D. 1000V 4H-SiC Gate Turn Off (GTO) Thyristor, *Compound Semiconductors, IEEE International Symposium*, **1997**, pp 363–366.
10. Sehadri, S.; Casady, J. B.; Agarwal, A. K.; Siergiej, R. R.; Rowland, L. B.; Sanger, P. A.; Brandt, C. D.; Barrow, J.; Piccone, D.; Rodrigues R.; Hansen, T. Turn-off Characteristics of 1000 V SiC Gate-Turn-Off Thyristors, *Proceedings of 1998 International Symposium Devices and ICS*, **1998**, pp 131–134.

11. Agarwal, A. K.; Ivanov, P. A.; Levinshtein, M. E.; Palmour, J. W.; Rummyantsev, S. L.; Ryu S. H.; Shur, M. S. Turn-off Performance of a 2.6 kV 4H-SiC Asymmetrical GTO Thyristor, *Material Science Forum*, **2001**, 353–356, pp 743–746.
12. Seshadri, S.; Agarwal, A. K.; Hall, W. B.; Mani, S. S.; Macmillan, M. F.; Rodrigues, R.; Hanson, T.; Khatri S.; Sanger, P. A. Current Status of SiC Power Switching Devices: Diodes and GTOs, *Mat. Res. Soc Symp. Proc.*, **1999**, 572, pp 23–32.
13. Li, X.; Tone, K.; Cao, L. H.; Alexandrov, P.; Fursion, L.; Zhao, J. H. Theoretical and Experimental Study of 4H-SiC Junction Edge Termination, *Material Science Forum*, **2000**, 338–342, pp 1375–1378.
14. Agarwal, A.; Ryu, S. H.; Singh, R.; Kordina, O.; Palmour, J. W. 2600 V, 12 A, 4H-SiC, Asymmetrical Gate Turn Off (GTO) Thyristor Development, *Material Science Forum*, **2000**, 338–342, pp 1387–1390.
15. Ryu, S. H.; Agarwal, A. K.; Singh, R.; Palmour, J. W. 3100 V, Asymmetrical, Gate Turn-Off (GTO) Thyristors in 4H-SiC, *IEEE Electron Device Letters*, **2001**, 22, pp. 127–129.
16. Singh, R.; Irvine, K. G.; Palmour, J. W.; Levinshtein M. E.; Rumyanetsev, S. L. 4H-SiC Bipolar PiN Diodes with 5.5 kV Blocking Voltage, *Proc. Device Res. Conf.*, **1998**, pp 86–87.
17. Hefner, A.; Singh, R.; Lai, J.; Berning, D.; Bouché S.; Chapuy, C. SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, *IEEE Trans. Power Electronics*, **2001**, 16, pp 273–280.
18. Blicher, A. *Thyristor Physics*, New York: Springer-Verlag, 1976, pp 8–11.
19. Mohan, N.; Undeland, T.; Robbins, W. *Power Electronics Converters, Applications, and Design*, New York: Wiley, 1995, pp 613–695.
20. Ziang, Y. Q. Instability Compensation of V/Hz PWM Inverter-fed Induction Motor Drives, *Conference Record of the 1997 IEEE Thirty-Second IAS Annual Meeting*, **1997**, pp 613–620.

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