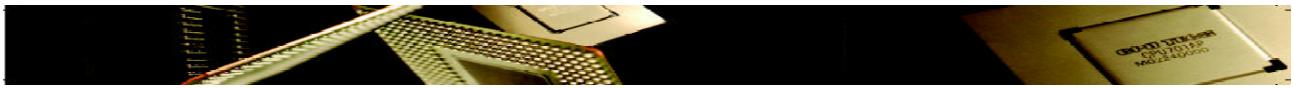
CPU TECH

H-60 Mission Avionics Technology Insertion

Final Report
January, 2004



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Revision History

Revision #	Date	Comments
1.0	1/26/04	Initial Release

1.0 Executive Summary

Due to funding pressures, program and personnel realignments, existing helicopters are going to be required to remain in service longer. However, the need to maintain, upgrade and enhance the relative stature of the U.S. arsenal and their expanding missions continues to exist. Currently, the H-60 mission avionics systems utilize processors that implement the required functionality. However, avionics microprocessors are hampered in two significant areas: performance, and the fact they are 16-bit computers, which limits the memory and size of the operand among other things. The fact that these processors have fallen behind can be readily seen in today's systems: the response time is degraded due to insufficient processing through-put, the types of missions that can be executed on a given flight are limited, and often old features must be eliminated in order to add new ones. These deficiencies reduce mission effectiveness, limit aircraft potential and expose pilots to increased risk.

The software base that has developed over time for these processors has been estimated to be well over $40 billion. This includes operating systems and application software. The databases themselves as well as the development tools would constitute a significant addition to this investment. All of the software has been proven and matured. To discard all of the old software and start anew would cost billions of dollars in re-write costs and testing to attain the same level of confidence in the new software. This huge re-investment to achieve essentially the same capability that currently exists would occur at a time when funding is being reduced. Simply substituting a MIPS R4000™, PowerPC, Intel i960™, or other existing non-compatible commercial processor increases the performance and memory allowed, but is not necessarily the best solution. Re-compiled software requires re-certification since different compilers do not produce exactly the same code, and re-compilation does not address the legacy software such as CMS-2 and JOVIAL. It is estimated that the cost to recreate a software base by recoding the software is about 3.5 times the cost of rehosting the software on new hardware. Most commercial processors do not readily support redundancy and reconfigurability, which is a definite advantage when a pilot is trying to bring back a crippled plane. Likewise, adding instructions to accelerate frequently used routines is not possible with standard commercial processors.

2.0 Scope

2.1 Program Overview

The objective of this H-60 Mission Avionics Technology Insertion Small Business Innovation Research (SBIR) Phase I program is to investigate the legacy technology and implementation details of the appropriate H-60 avionics and flight control systems. The three major events associated with this program are the collection of relevant data, the technical analysis of applicability of System-on-a- Chip (SoC) integration and the generation of the final report which includes technical recommendations for Phase II and Phase III programs.

The collection of the relevant data started at award of the contract and lasted for the month and a half of the contact. There was some further initial data gathering during the next couple months to provide additional information during the technical analysis.

CPU Tech's assessment of the applicability of applying new commercial system on chip technology to the H-60 avionics and flight control system was based on the documentation it was able to obtain and is highlighted in the following sections of this report.

The work under this contract included the technical analysis of the architecture, performance, behavior, reliability, environmental conditions, physical implementation, configuration, software, sustainability, power and heat issues, and other relevant factors at the system level of the H-60 mission avionics where documentation was available.

After the technical analysis is described, the final report on the applicability of SoC technology addresses the system issues of increasing processing power, reducing the number of parts, decreasing the heat and power requirements, improving system reliability and addressing parts obsolescence problems with no impact on operation. In addition, any CPU Tech SoC design will be 100% compatible with current avionics and flight control systems, will require no changes to internal wiring, will require no changes to interface signals and will maintain compatibility with test systems.

This final report shows the results of the CPU Tech's technical analytical assessment of several of the H-60 avionics and flight control systems and its appropriateness to the new processing paradigms of SoC technology. It also includes CPU Tech's technical recommendations regarding a strategy for implementing a Phase II advanced development program which would lead to a Phase III implementation program.

Section 3 lists the applicable documents that were reviewed. Section 4 describes the technical analysis of the H-60 mission avionics systems and their applicability of SoC integration. Section 5 describes the technical recommendations regarding a strategy for a Phase II advanced development program.

2.2 CPU Tech and SoC Technology

CPU Tech is a fabless System-on-a- Chip (SoC) company that develops compatible, next generation solutions for the commercial and military markets. We are committed to making state-of-the-art technology practical for critical electronic systems in industries such as Defense and Aerospace, Medical Instrumentation, Life Sciences, and High End Computing Solutions.

By dramatically changing the economics of systems development, CPU Tech makes tomorrow's technology available now... for any application regardless of volume.

An SoC is a single device that contains processors, memory, buses, controllers and software. It represents the next generation of highly integrated chips. As chip process technology became more refined, larger and larger transistor die-size budgets became available to design engineers to build their chips. The SoC evolution was a natural outcome of these large transistor budgets, which engineers now use to incorporate more of the system logic onto a single chip.

The commercial market has addressed the issue of "bringing along" a vast existing software base when introducing the latest in hardware technology. A good example is Intel's® X86/Pentium™ family of microprocessors. Intel has done a tremendous job of ensuring "compatibility" in every next generation microprocessor so as not to abandon the tremendous value of existing software. At the same time, the latest technology enables enhanced features and functions for applications. This strategy has worked very successfully for both Intel and the customer.

Compatible evolution for high end systems cannot be achieved without the ability to provide functional testing and verification of all critical aspects of system operation. Reliability is an unconditional requirement. The complex nature of SoC devices presents an enormous challenge to validation and test engineering. The ability to perform this function manually is simply not an option where full coverage is mandatory. The key to overcoming this formidable challenge is automation.

The defense and aerospace industries are supported by a large software base developed over decades, running complex and, oftentimes, mission critical applications. The tremendous cost of developing this highly specialized software base and lengthy certification requirements, when applicable, make it important to "bring along" these family jewels as technology advances. Unfortunately, in most instances, the underlying hardware lacks a technology road map for the future.

For processing systems, the cost of initial SoC insertion is only half the story. Given their lengthy life cycles - oftentimes spanning many decades - a greater cost consideration is long term maintenance and operability. Developers of processing systems find themselves continually at the mercy of component manufacturers who routinely discontinue parts as new products are introduced. Their relatively low volumes do not provide the necessary incentive for suppliers to continue production as demand dwindles. CPU Tech's SoC solutions are designed specifically to be foundry independent and are escrowed for the benefit of its customers. This resolves component obsolescence concerns for the life of the system.

The CPU Tech Difference

CPU Tech has made a decade-long investment in R&D for the creation of advanced Electronic Design Automation (EDA) tools that enable rapid development and testability of large SoCs. Compatible system designs, processor cores of any type, and formal verification technology are automatically generated from a system specification. Use of CPU Tech's system-level EDA tools results in solutions with the highest levels of assured quality and reliability. A customer's actual application software is shown running on a precise model of their existing system using CPU Tech's advanced EDA tools.

SoC development has traditionally been an expensive proposition. The majority of the cost is for the design and engineering of the chip up to the point of production. Chip providers that use the traditional brute-force, labor intensive development methodology must rely on large volume sales in order to experience an acceptable Return On Investment (ROI). Since CPU Tech has automated the up-front process, it is able to reduce the cost of SoC development to a fraction of what it costs to do it in the traditional manner. Because CPU Tech's advanced tools make it possible to cost effectively manage the complex process of creating and applying SoC technology, a new paradigm has emerged.

3.0 Applicable Documents

187A157 Rev B: Multi-Mission Helicopter Flight Avionics Segment Interface Control Document

187A225 Rev A: Interface Control Document for the MH-60R Multi-Mission Helicopter Air Vehicle Segment for EMD II / LRIP I

230A446 Rev B: Multi-Mission Helicopter Stores and Self-Defense Avionics Segment Interface Control Document

6953771 Rev N: MH-60R Air Weapons System and Multi-Mission Helicopter Avionics System Specification

MH-60R Interactive Electronic Technical Manual

Software Loading Procedures

Software development language and Lines of Code estimates

NAVY Training System Plan for the AN/ALE-47 Countermeasures Dispensing System

4.0 Technical Analysis

The technical analysis of the H-60 mission avionics systems was based on the documentation listed in section 3. This documentation included several H-60 Mission ICDs, system specifications, software processing and code information, the MH-60R Interactive Electronic Technical Manual (IETM), software loading procedures and software language and lines of code estimates. CPU Tech's technical analysis of the H-60 mission avionics systems and our experience with providing processor compatible SoC technology that provided increased processing power, 100% software compatibility and addressing obsolescence concerns enabled us to determine which mission avionics processing systems which make them potential candidates for SoC technology. The block diagram of the MH-60 helicopter avionics system is shown in figure 4.0.

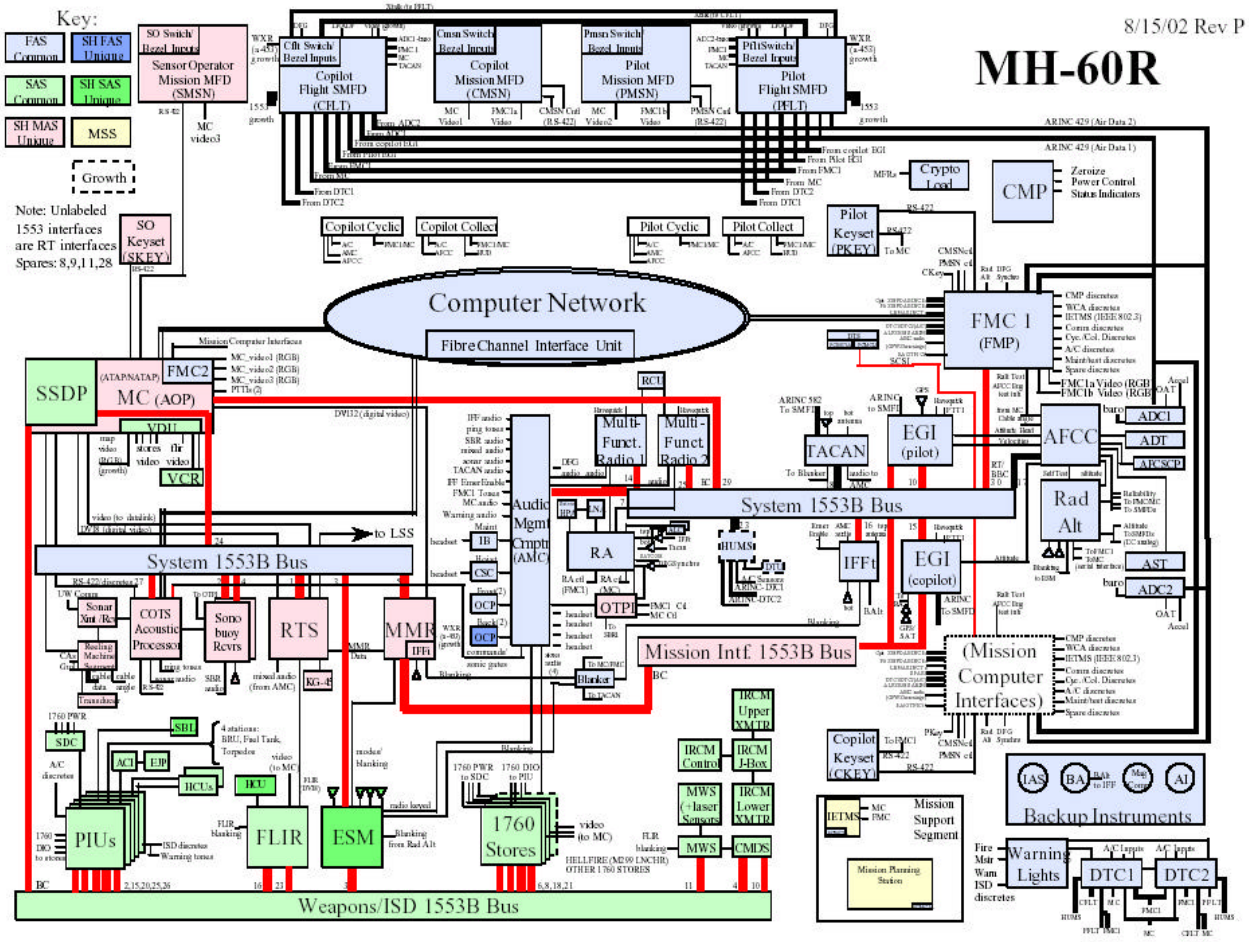

Figure 4.0:MH-60 Avionics System Block Diagram

The MH-60 block diagram shows the complexity of the mission avionics systems. There is a significant amount of data and video processing performed by the MH-60. This data is controlled and distributed throughout the H-60 using multiple interfaces including Fibre Channel and FDDI interfaces, 1553B serial interfaces as well as Arinc 429, RS422 and RS423 interfaces. The systems use video and data processors, such as the PowerPC 603e, Power PC 750, ADSP 21060 digital

signal processor the Sharp LH2194 DSP and the TMS320C80 graphics processor. These processors have limited lifetimes and those that are not obsolete already will soon become obsolete. The types of systems where there is significant processing power utilized for data communications, data processing and video processing are where we focused our efforts and analysis on the MH-60. Using the documentation provided, we analyzed these systems within the MH-60 for applicability to SoC technology and came up with a recommendation for which systems will achieve the most benefit.

The criteria that CPU Tech used in determining the applicability to SoC technology is identified in section 4.1 and the H-60 Mission Avionics technical analysis on the H-60 mission avionics systems that we identified are described in section 4.2.

After analyzing the documentation and having some brief discussions with Navy personnel, we identified a set of ten core H-60 systems that had systems architectures, system detailed block diagrams, performance, functional operation, growth or system issues such as reliability and obsolescence that had applicability to SoC technology. These ten H-60 mission avionics systems are listed below:

- Mission Computer Set
- Air Data Computer Set
- Automatic Flight Control System
- Multi-function Display Set
- Stores Management System
- Mass Storage Set
- Electronic Support Measures
- Audio Management Computer
- Multi-function Radio Set
- Digital Data Concentrator set

In addition to the ten core set of H-60 mission avionics systems listed above, there are three other computing systems in the H-60 that could benefit greatly from SoC insertion. Among these are:

- AN/APS-147 Multi Mode radar
- AN/AAR-47 Missile Approach Warning System
- Acoustic Processor

4.1 Applicability to SoC technology

Defense and Aerospace system designers have limited options when it comes to upgrading systems to meet future requirements. Once a processor has been selected and billions of dollars spent on writing, testing and qualifying the system software, the designers used to be limited to the current architecture. This was dictated by the huge investment of software that was already qualified for the system. Now, system designers have another option with SoC technology. CPU Tech has developed an SoC development process that takes advantage of the best of commercial technology without the penalty of prohibitive development costs or devastating obsolescence. Now that CPU Tech has made it economically practical, the time has come to reap the benefits of compatible SoC, including:

- 100% compatibility with current processor
- Higher performance
- Lower power
- Smaller size
- Lighter weight
- Higher reliability
- Increased Scalability
- Supports future growth requirements
- Applicability to extreme environments
- Lower recurring costs
- Elimination of obsolescence issues

These benefits associated with SoC technology are what we used to perform our technical analysis and were used to drive our recommendation for Phase II advanced development and Phase III implementation programs. A more detailed analysis of all these benefits will be conducted in Phase II to determine the specific SoC architecture that would apply to each system.

4.2 H-60 Mission Avionics System Technical Analysis

There are thirteen H-60 mission avionics systems that CPU Tech performed a technical analysis of that identified them as applicable to SoC technology. The technical analyses for these thirteen systems are described in the following sections.

4.2.1 Mission Computer Set

The Primary Mission Computer is housed in a VME bus 15 slot card cage. Processing functions include video processing, IO processing, and applications processing. The current applications processing software utilizes the PowerPC 603e instruction set. Graphics processing is performed using the TMS320C80 graphics processor. The PMC interfaces to other avionics systems by means of dual Fibre Channel interfaces, 1553B serial interfaces, RS422 and RS423 interfaces, Ethernet interface, digital and analog video interfaces, analog and digital discrete signals. All of these functions require ten cards within the VME card cage. The primary Flight Management Program software resides on the applications processing module.

The block diagram for the primary mission computer is show in Figure 4.2.1.

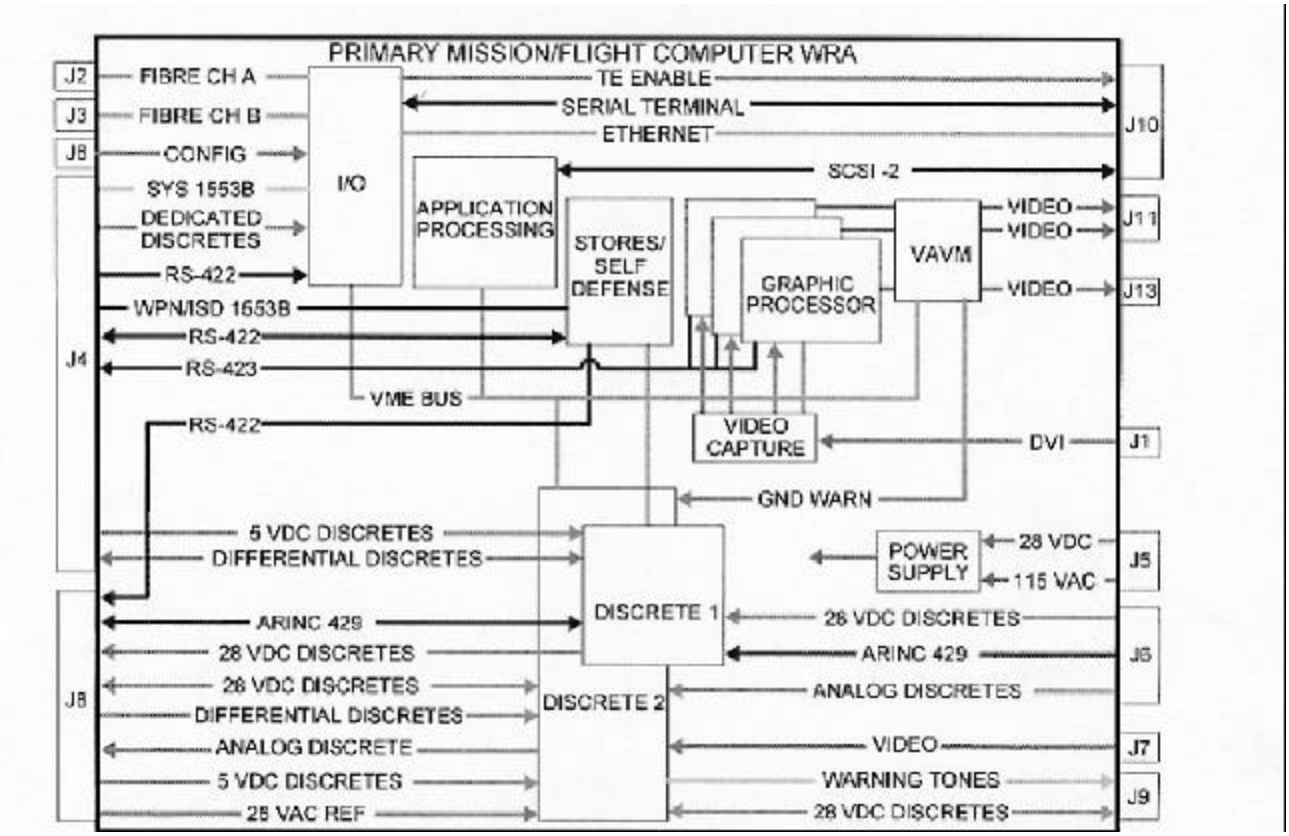

Figure 4.2.1: Primary Mission Computer Block Diagram

The Backup Mission Computer performs a subset of the functions of the Primary Mission Computer in the case of PMC failure. A six-slot VME chassis houses internal modular assemblies for IO processing, graphics processing, and discrete interfaces. Flight Management Program software is resident within this system. Cards are used for IO and graphics processing are the same as those used in the primary mission computer.

All of the digital functions within the PMC and BMC are good candidates for SoC insertion, with an emphasis placed on binary compatibility with the operational software SoC insertion would reduce the number of cards required in both the primary and backup mission computers, providing room for addition of extra processing capability.

4.2.2 Air Data Computer Set

Dual ADCs process inputs from pitot and static ports, accelerometers, and temperature sensors. Data is output over Arinc 429 interfaces to the data handling and controls and displays systems. No information is available regarding the internal implementation of the ADC processing modules. However, the necessary functionality of input interfacing, processing of air data, conversion to Arinc format, and built in test would readily be incorporated into an SoC design.

The interface diagram for the air data computer set is show in Figure 4.2.2.

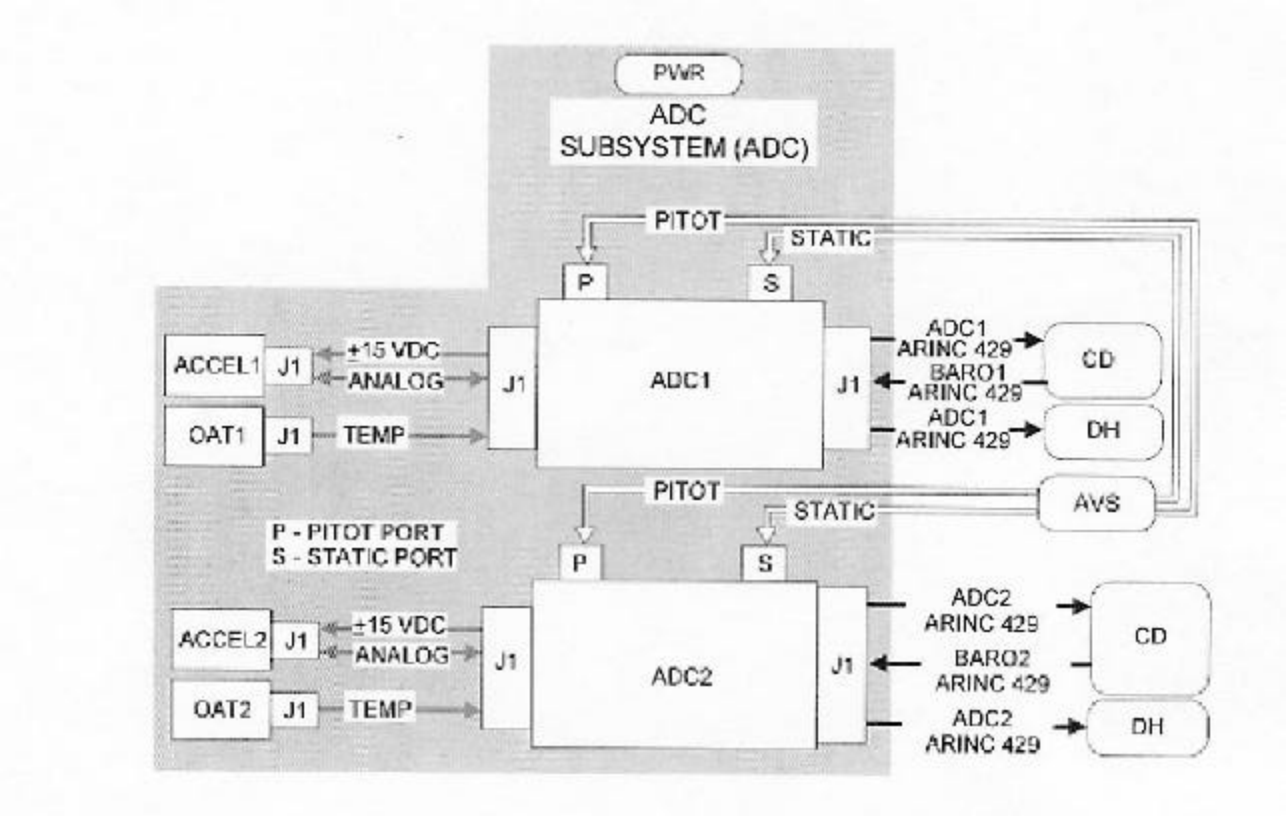

Figure 4.2.2: Air Data Computer Interface Diagram

4.2.3 Automatic Flight Control System

The Automatic Flight Control System processing module consists of a central processing unit with random access memory and non-volatile memory, 1553 interface, analog to digital and digital to analog interfaces. The CPU function and RAM can be integrated into a single SoC device, along with the 1553 interface and logic associated with the A/D and D/A interfaces. The obsolescence risk of the discrete digital components would be eliminated.

The block diagram for the Automatic Flight Control System is show in Figure 4.2.3.

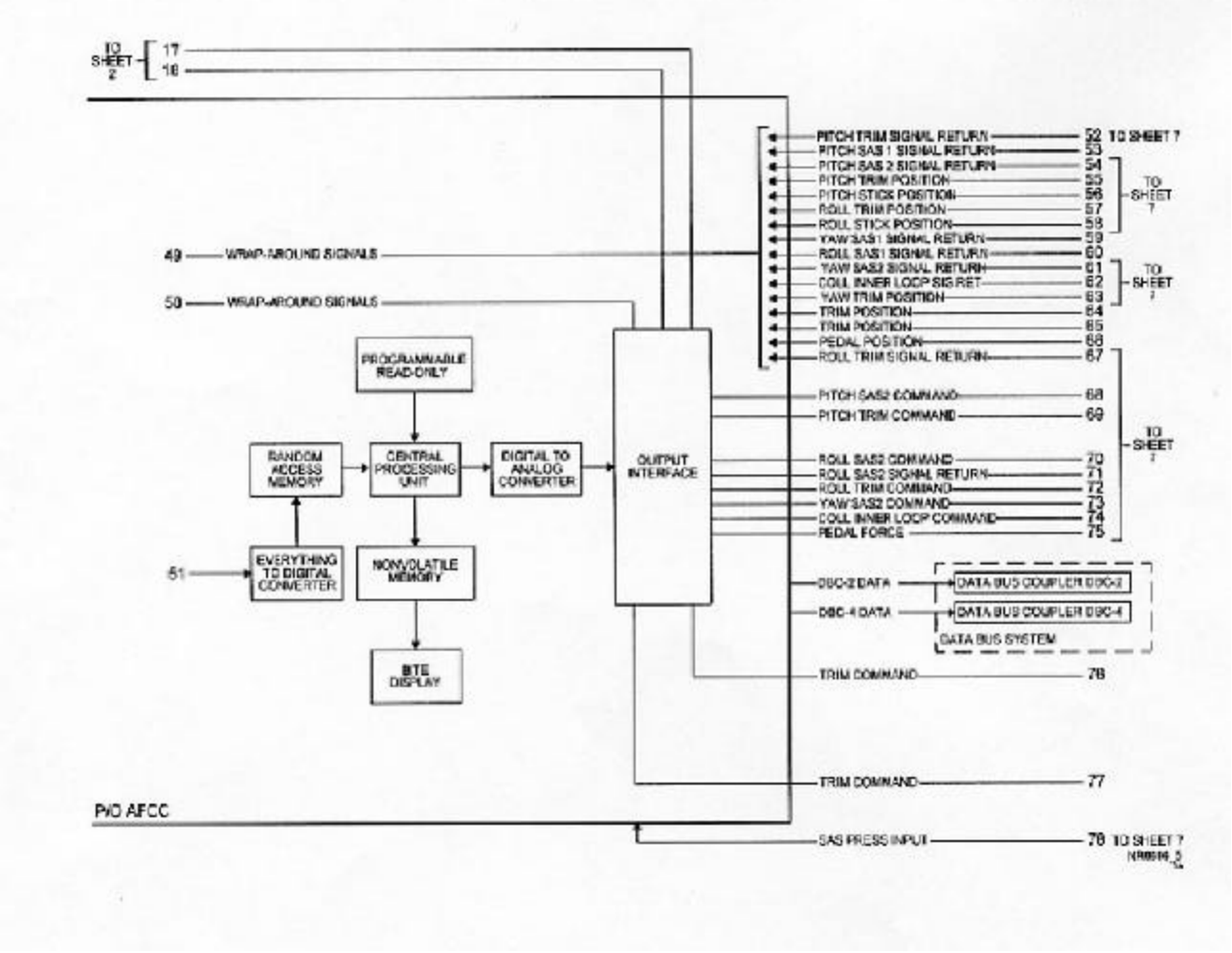

Figure 4.2.3: Automatic Flight Control System Block Diagram

4.2.4 Multi-function Display Set

The Multi-function Display Set contains a main CPU, graphics and video processing, and IO processing which are interconnected via a PCI bus. It includes many interfaces to external systems, such as 1553 interface, 2 video input channels, 1 video output channel, Arinc 429 and Arinc 582 interfaces, Ethernet interface, SCSI interface, RS422 interface, Synchro to digital conversion.

The block diagram for the Multi-function Display Set is show in Figure 4.2.4.

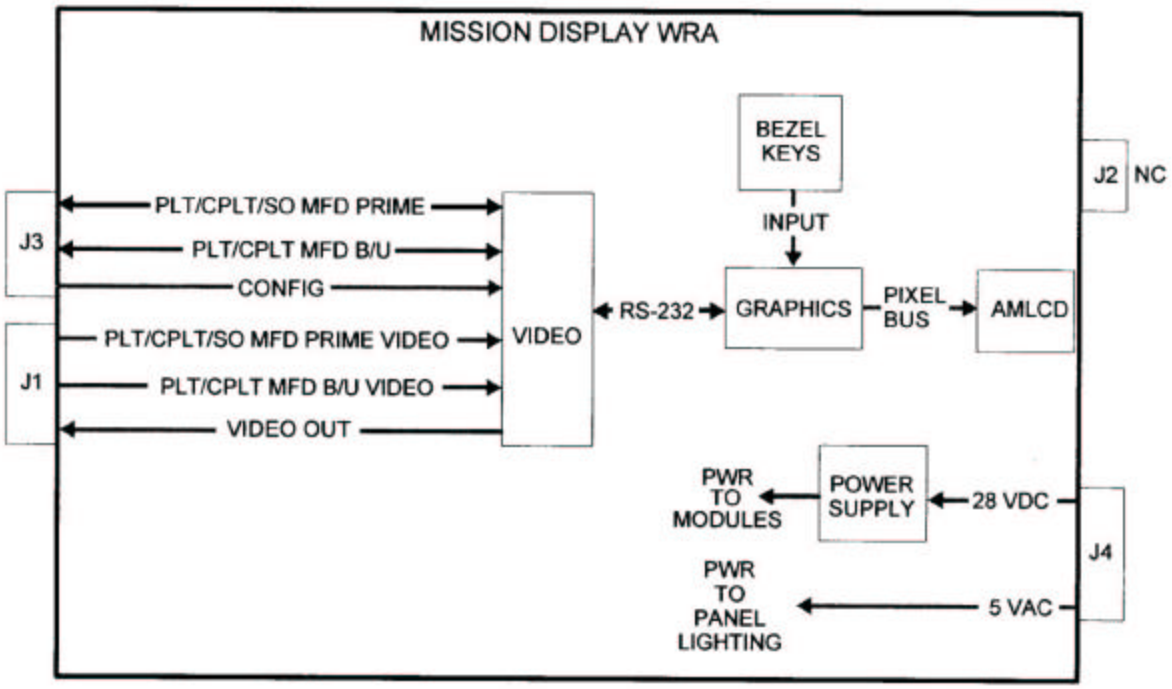

Figure 4.2.4: Multi-function Display Set Block Diagram

4.2.5 Stores Management System

The Stores Management System contains four Processing Interface Units (PIU), each with a micro controller, external interface cards, motherboard (backplane) and power supply. A 1553 serial bus interfaces to the data handling subsystem. The existing documentation only refers to the internal design of the PIU as “GFE to be supplied”, so no detailed specifications are available. However, micro controllers typically have high obsolescence risk, so these subsystems would be good candidates for SoC insertion. In addition, the PIU shares several interface standards with other avionics subsystems, such that SoC development for these interfaces would easily be leveraged across the PIU and other subsystems.

The block diagram for the Stores Management System is show in Figure 4.2.5.

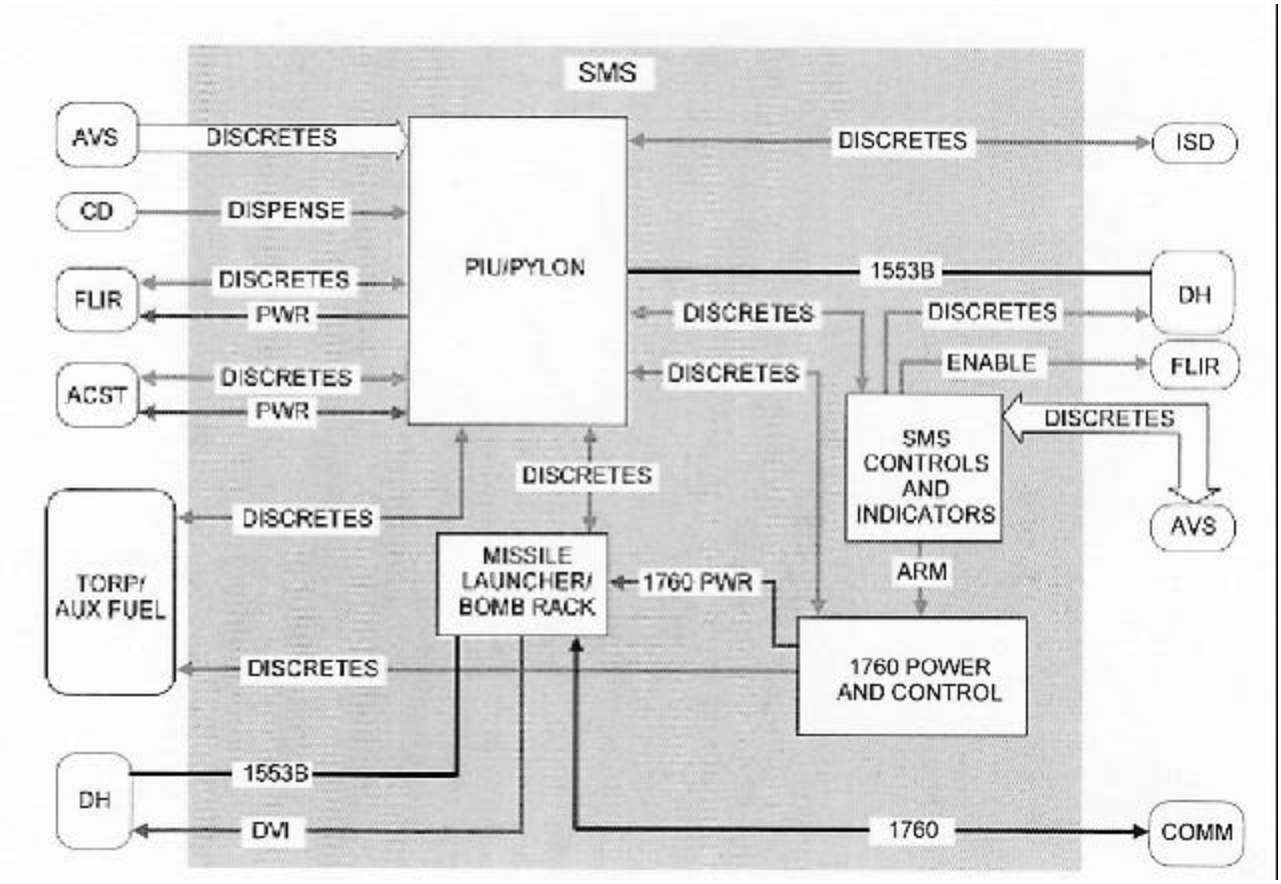

Figure 4.2.5: Stores Management System Block Diagram

4.2.6 Mass Storage Set

Data storage subsystem contains a SCSI disk drive and dual PCMCIA card interfaces (mission and recovery). This is controlled by the primary mission flight computer. These components are essentially commodities based on commercial open standards, so SoC insertion would not add significant benefits for these components. The 80C186XL-based micro controller presents an obsolescence risk, as does the SCSI-2 controller. These functions, along with the discrete IO logic and PCMCIA controller logic, can be integrated into a single SoC to mitigate these risks.

The block diagram for the Mass Storage Set is show in Figure 4.2.6.

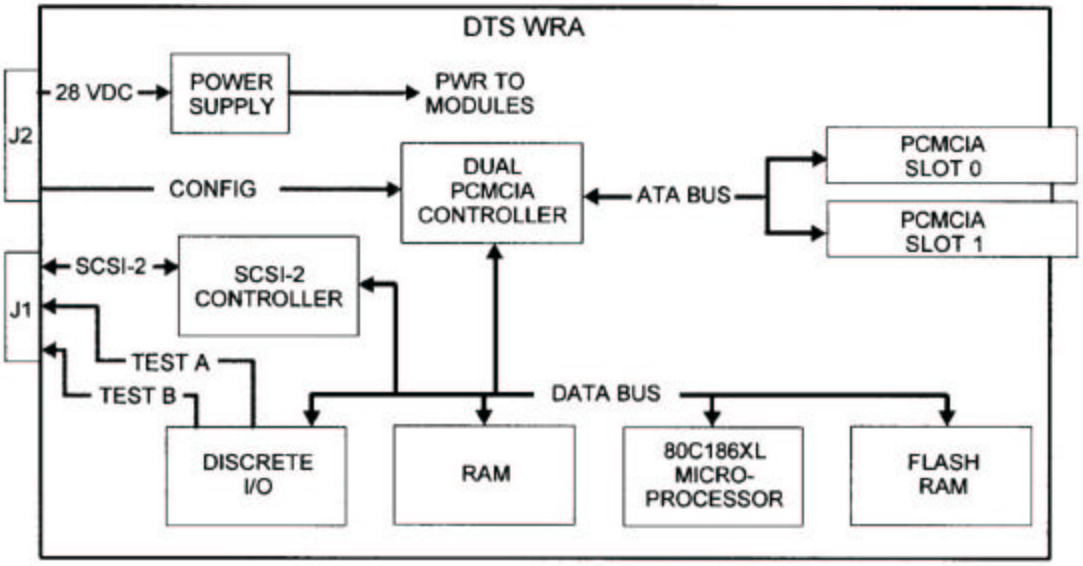

Figure 4.2.6: Mass Storage Set Block Diagram

4.2.7 Electronic Support Measures

The Electronic Support Measures AN/ALQ-210 Receiver Processor is based on a PowerPC 603e single board computer. This is the same single board computer that is utilized in the Primary Mission Computer, so it would be subject to the same obsolescence risks and throughput limitations. The benefit of SoC insertion would be very high, and the SoC development effort would leverage greatly from the SoC efforts on the PMC. Additional functions within the Receiver Processor include baseband receivers, pulse processing, and down conversion functions. When further technical information is available on these functions, additional SoC insertion opportunities could be identified within the ESM.

The block diagram for the Mass Storage Set is show in Figure 4.2.7.

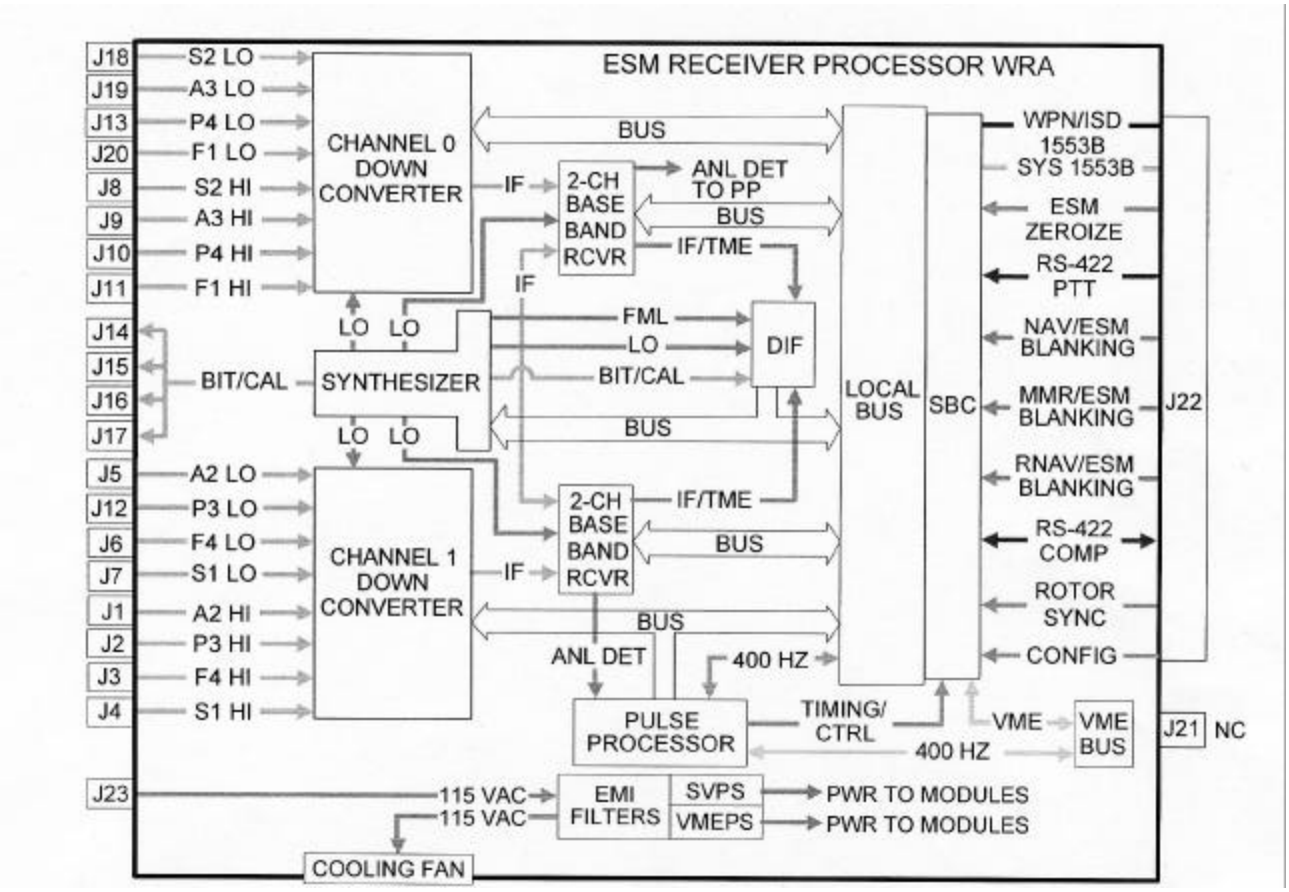

Figure 4.2.7: Mass Storage Set Block Diagram

4.2.8 Audio Management Computer

The Audio Management Computer contains five modules in a VME chassis. These modules provide a central processing unit with a 1553B serial bus interface, two 12-channel audio interface modules, FDDI interface and discrete audio interfaces.

The block diagram for the Audio Management Computer is show in Figure 4.2.8.

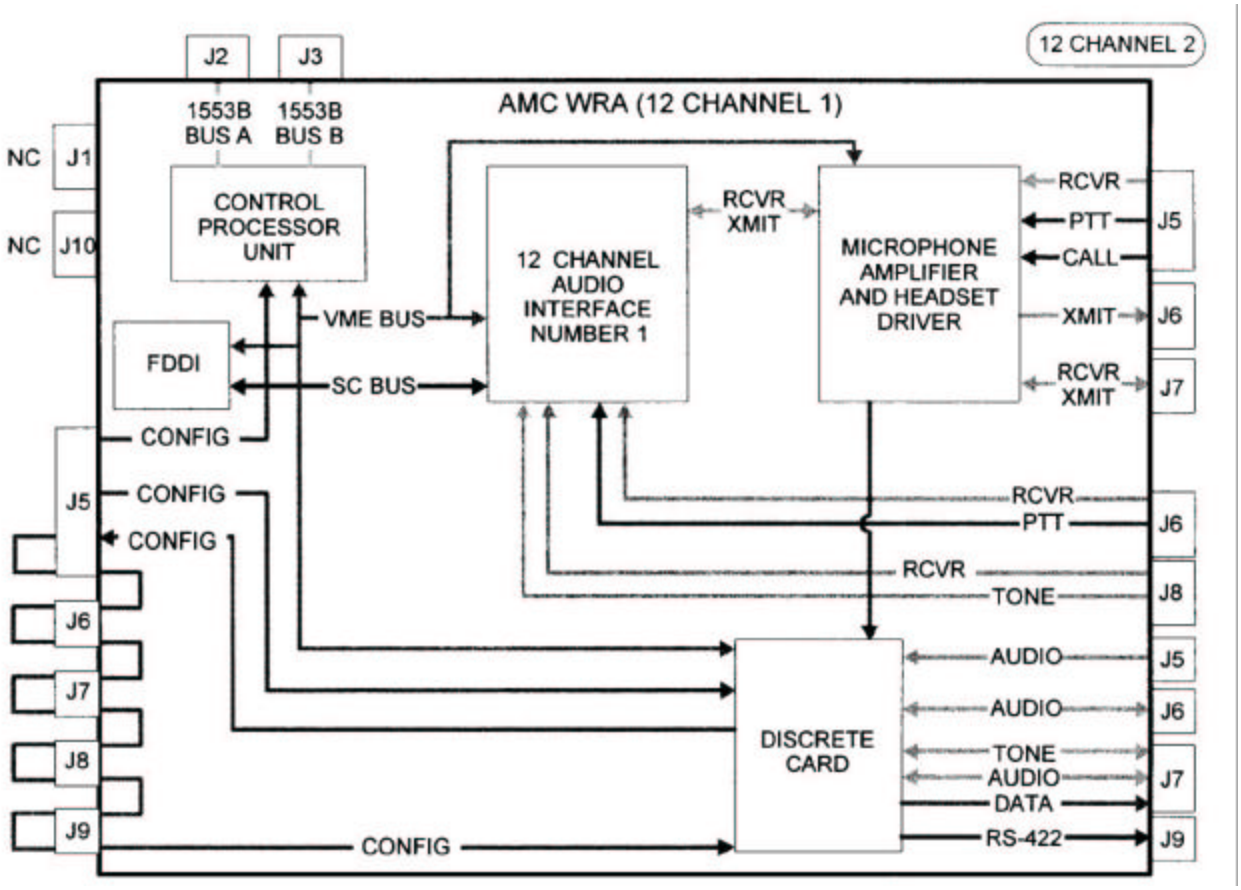

Figure 4.2.8: Audio Management Computer Block Diagram

4.2.9 Multi Function Radio Sets

There are two AN/ARC-210 Multi Function Radio Sets per aircraft. Each contains a digital signal processor, control functions, frequency synthesizer, power amplifier and receiver. A 1553B serial bus interface and other discrete interfaces connect the MFRS to external systems. No further technical information about the existing design is available.

The block diagram for the Multi Function Radio Sets is show in Figure 4.2.9.

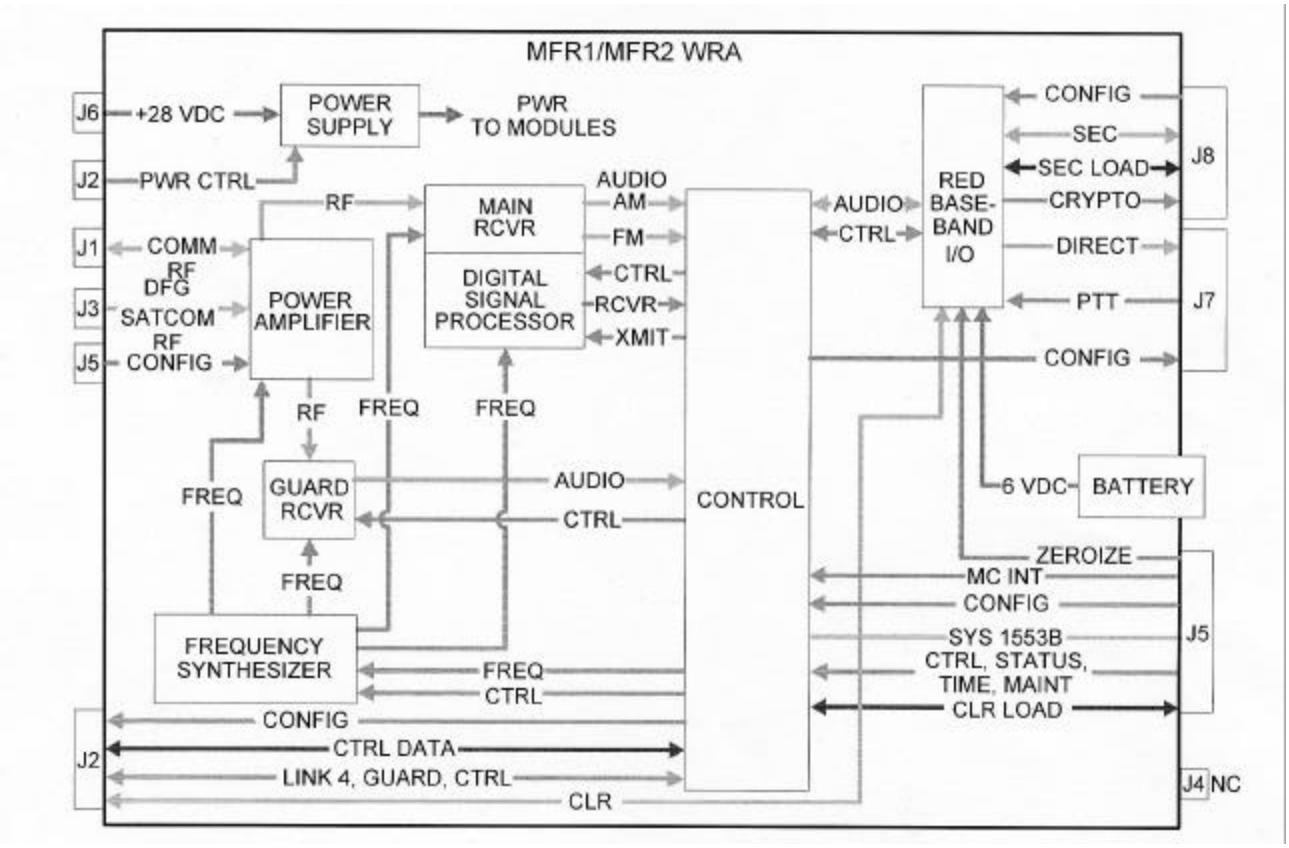

Figure 4.2.9: Multi Function Radio Sets Block Diagram

4.2.10 Digital Data Concentrator

The Digital Data Concentrator contains discrete inputs and outputs, dual Arinc 429 interfaces, and discrete-to-Arinc conversion functions. Two data concentrator units are installed in each aircraft. All of the internal functions would easily reduce to a single SoC device on a single circuit car assembly. A small number of analog interface components would provide the connection between the discrete signals and the SoC device.

The block diagram for the Digital Data Concentrator is show in Figure 4.2.10.

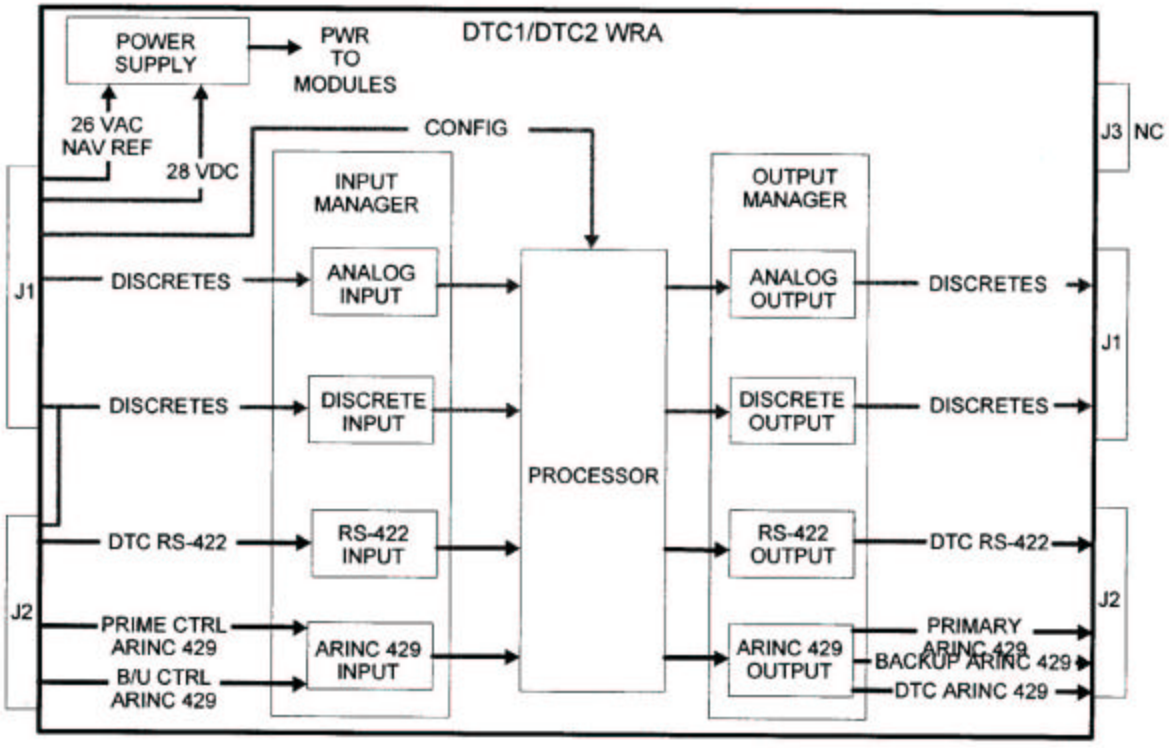

Figure 4.2.10: Digital Data Concentrator Block Diagram

4.2.11 AN/APS-147 Multi Mode radar

The Radar Data Processor contains 17 cards that implement IFF processing, IQ data processing, general IO processing and scan conversion of radar video data. The software is hosted primarily on the ADSP 21060 digital signal processor and also on the obsolete Sharp LH2194 DSP. SoC insertion has the potential to greatly reduce the number of cards and components required. Large savings of power, heat dissipation, weight, and volume are possible. In addition, reliability would be greatly increased due to the reduction in components.

The block diagram for the AN/APS-147 Multi Mode radar is show in Figure 4.2.11.

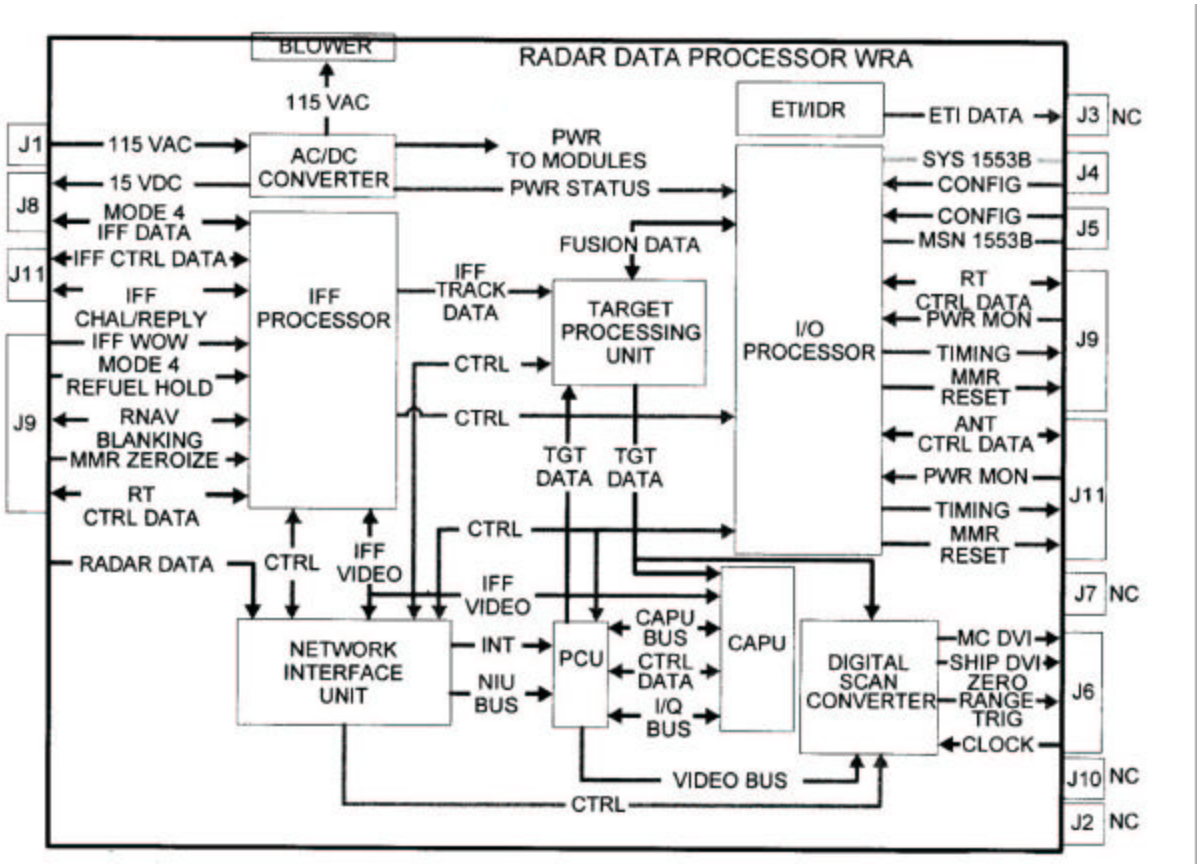

Figure 4.2.11: AN/APS-147 Multi Mode radar Block Diagram

4.2.12 AN/AAR-47 Missile Approach Warning System

The computer processor (CP) module contains a microprocessor card and a system interface card, in a chassis that is 640 cubic inches and weighs 16 pounds. 1553B interface, RS-485 interface and discrete I/O are also contained within the system.

The block diagram for the AN/AAR-47 Missile Approach Warning System is show in Figure 4.2.12.

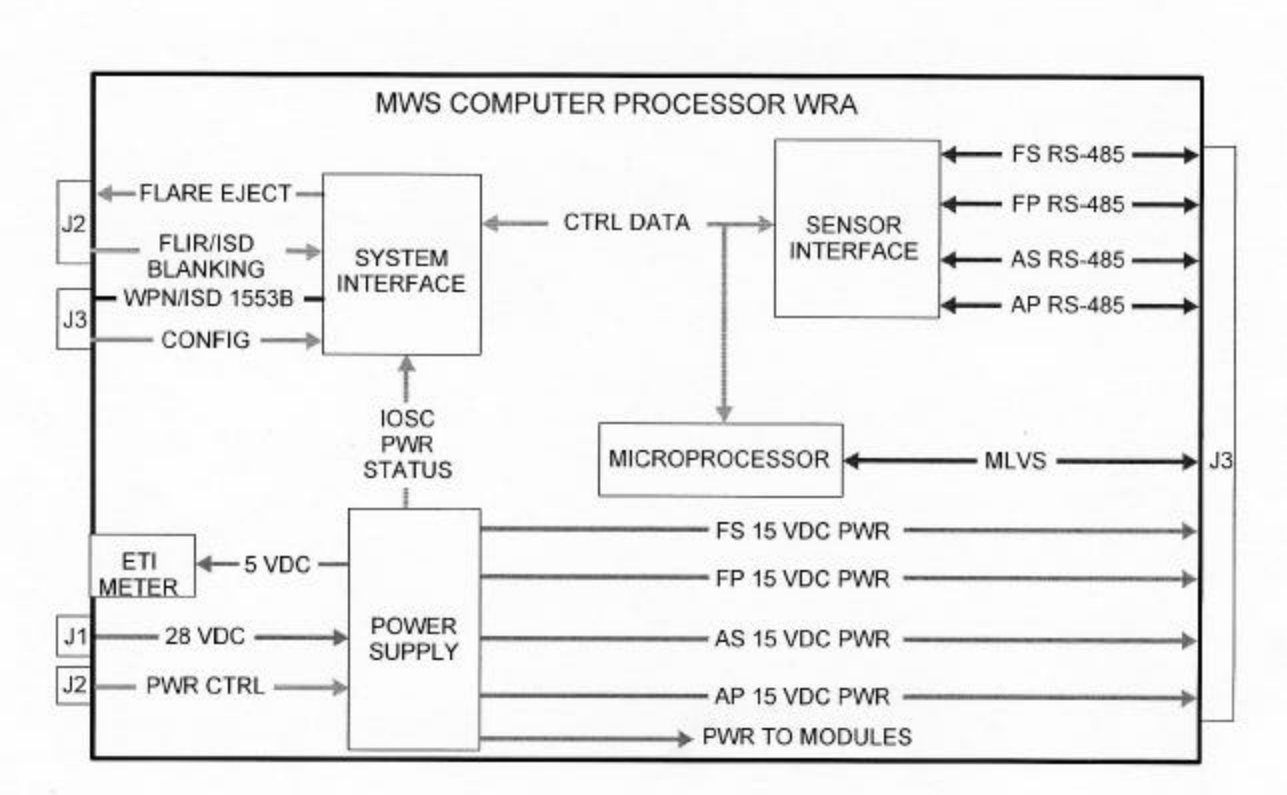

Figure 4.2.12: AN/AAR-47 Missile Approach Warning System Block Diagram

4.2.13 Acoustic Processor

The Acoustic Processor contains four single board computer modules in a 15 slot VME chassis. Each SBC contains a PowerPC 750, 128 Mbytes of RAM, 16 Mbytes of flash, and a PCI interface, as well as a 1553B interface and Ethernet interface.

The block diagram for the Acoustic Processor is show in Figure 4.2.13.

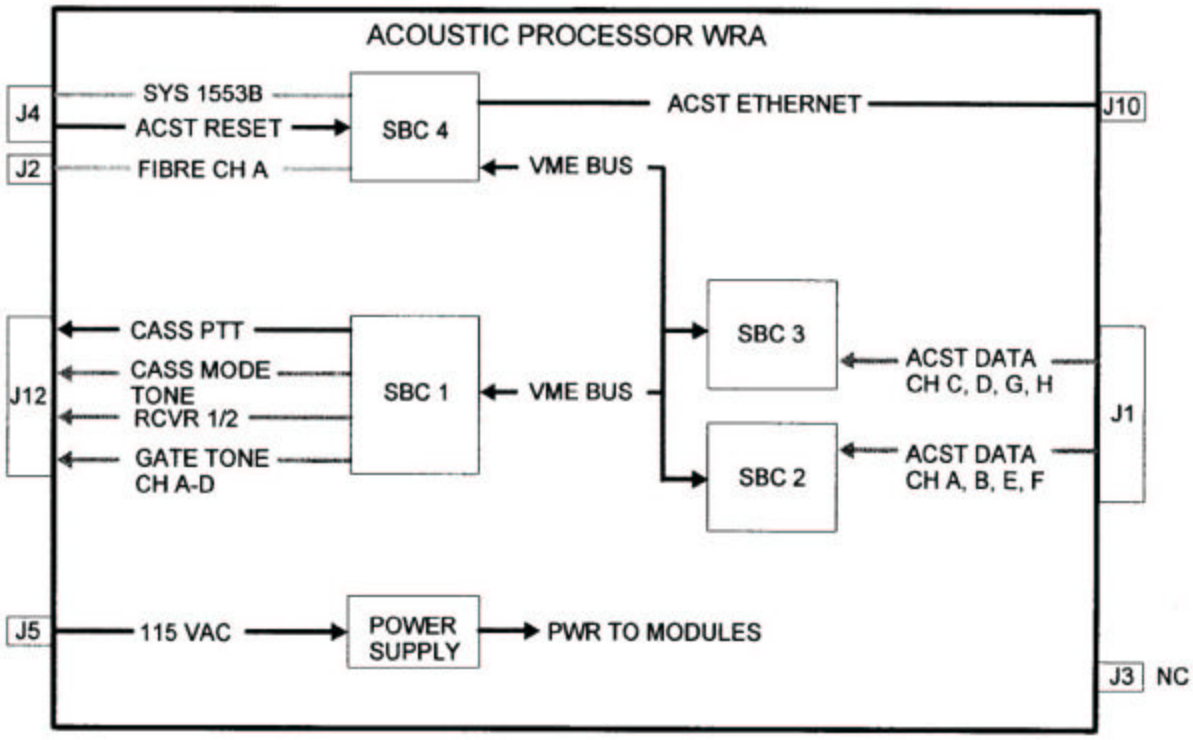

Figure 4.2.13: Acoustic Processor Block Diagram

5.0 Technical Recommendations

All of the above H-60 mission avionics systems have some applicability to SoC technology. However, based upon the assessment of available data, the following four core systems have the best potential for utilizing SoC technology:

1) Primary Mission Computer
2) Backup mission Computer
3) Electronic Support Measures Receiver Processor
4) Digital Data Concentrator

To follow up on this Phase I study, a Phase II advanced development program should be initiated. As a minimum, the Phase II base effort would analyze additional data on the four systems identified above and CPU Tech will furnish a technical description of the architecture that would be applicable to these H-60 mission avionics systems and provide an explicit roadmap on how to implement SoC technology into each of these systems.

The phase II advanced development program would minimally require the following information on each system to be analyzed.

- Detailed logic diagrams and schematics
- Functional specifications
- ICDs
- System Test Plans
- Obsolescence Issues
- Processing Requirements and limitations
- Future processing requirements

Information on processing requirements and limitations, future processing and system requirements and obsolescence issues are necessary to not only meet the requirements of today's system, but to determine the best implementation strategy that will meet the H-60 future growth requirements. The hardware architectural studies will determine which features and structures to include, and in what configurations, for the optimal performance at a reasonable cost. The simulations and analysis conducted during Phase II will conclusively prove that whether a processor(s) can be designed and will enable us to scope the complexity of the Phase III implementation effort to design the actual prototype chips and system hardware. Architectural issues will have been resolved and the appropriate silicon process technology will have been identified.

The Phase II advanced development program will focus on:

1) Develop SoC architecture with binary compatibility with existing processors
2) Optimize architecture for performance
3) Minimize part obsolescence

4) Increase system reliability
5) SoC capable of being targeted to any foundry

The Phase III implementation program will focus on:

1) Detailed design of system
2) Virtual verification
3) Integration with BVT and SystemLab development tools
4) SoC verification
5) Hardware system verification
6) Available in a Timely and Affordable Manner

The elements of Phase II and Phase III are contained in our processor design process.

6.0 SoC Design Process

CPU Technology has also worked with a large number of organizations concerning creation of 100% software compatible processors. After studying the problem with achieving 100% software compatibility, the CPU Technology team developed a processor design process that utilizes their system development tools. This process, along with our system development tools, has enabled CPU Tech to create high performance, contemporary SoC designs that are 100% compatible with an existing avionics processors. The major phases for the processor design process are shown in Figure 6.0.

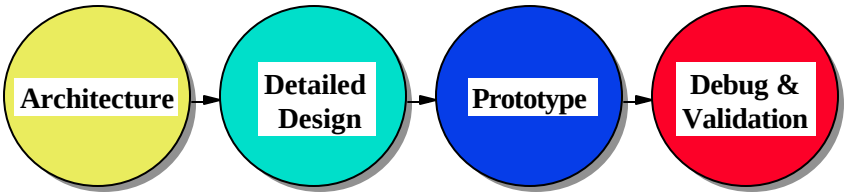

Figure 6.0, Processor Design Process

The scope for the Phase II effort is comprised of the first phase (Architecture), which is explored in detail in the following sections. The second, third and fourth phases would be done in a Phase III Implementation program.

6.1 Phase II Advanced Development Program

The objective of the architectural phase is to optimize overall SoC performance against customer current and future requirements, i.e. footprint, performance, size, weight, etc., and technology constraints. The architectural stage may be broken down into the steps shown in Figure 6.1-1.

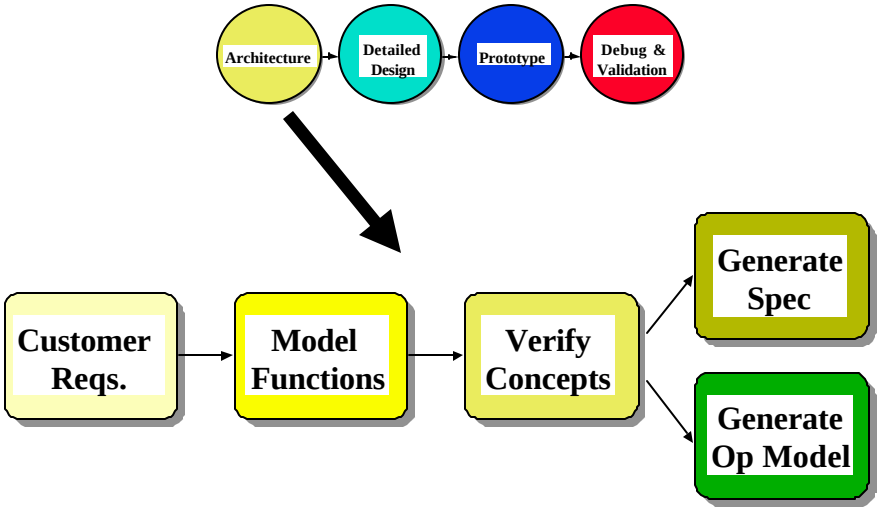

Figure 6.1-1, Architecture Flow Diagram

The first step is to evaluate the impact of customer requirements, including technology constraints, such as selected process technology, and then analyzing the potential architectural impact.

An initial architecture is developed and modeled using the model developed during the model step and integrated in SystemLab™, a virtual prototyping environment. The virtual prototype can also contain key elements of the customer's system. A sample of a SystemLab screen is shown in Figure 6.1-2.

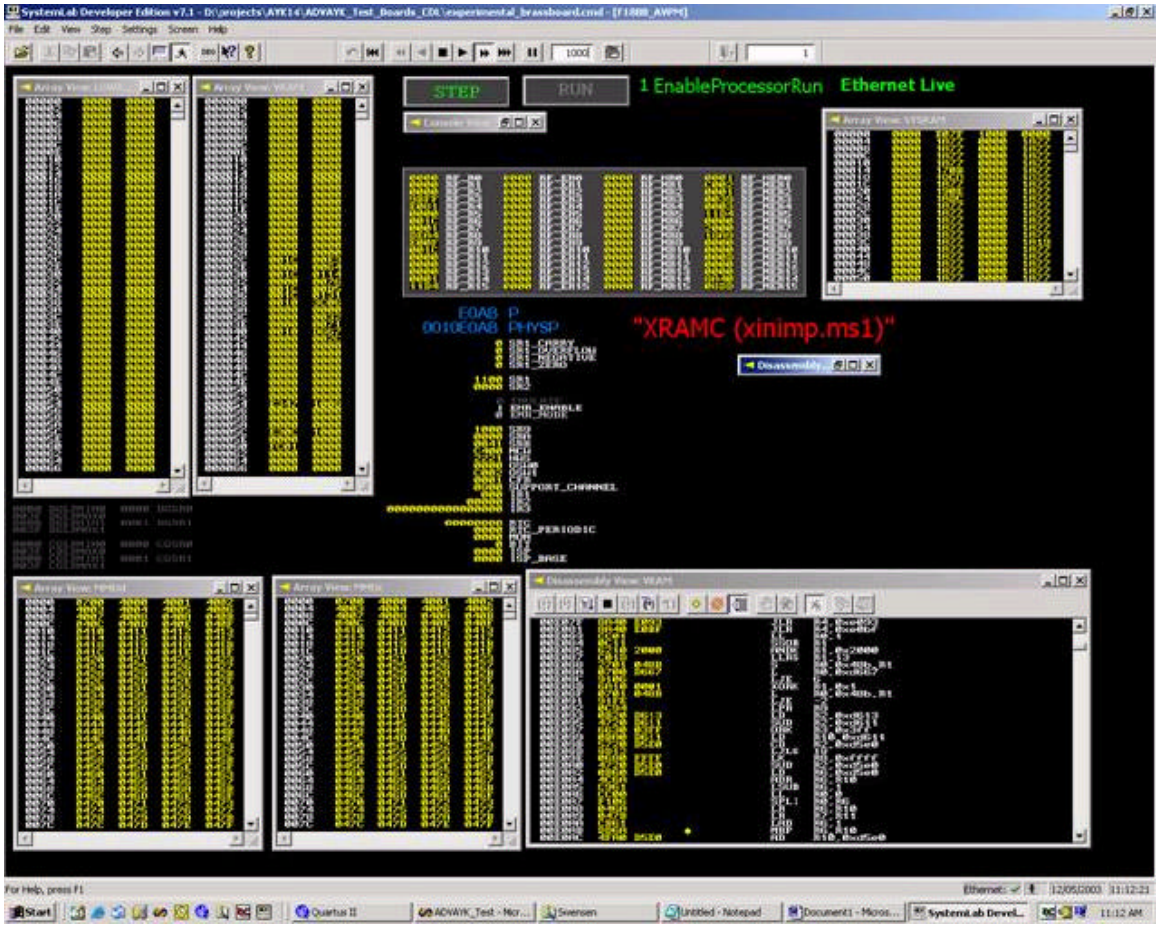

Figure 6.1-2: SystemLab Virtual Prototyping Instrumentation

In parallel, benchmarks are created representing worst case scenarios of the system operation. CPU Technology also obtains available performance benchmarks and application code samples. By executing these benchmarks on the SystemLab virtual prototype, interesting properties of the processor design and the overall system can be examined. For example, the virtual prototype will be instrumented to show details such as the percentage of time a processor is idle, a histogram of executed instructions, system bus utilization, etc. These metrics provide reliable system performance information and identify performance bottlenecks. Using the metrics resulting from modifications made following performance analysis, trade-offs are made to yield an optimized processor architecture.

The two system development toolsets that would be used by CPU Tech in the advanced development and implementation phases are:

1) Behavioral Verification Technology™ (BVT)
BVT is a software technology, which enables the rapid development of specification-based validation test suites for any system. BVT was originally created by CPU Tech to address the SoC market. Over the last eight years, most of the several major SoC and microprocessor semiconductor companies have licensed BVT. BVT's features and benefits are summarized below in Table 6-1.

Feature	Benefit
Tests every instruction/function in every mode	Full functional test coverage
Each test is independent	Can quickly test/re-test feature Can run tests in parallel
Specific tests	Know which operations and conditions that have been tested
High level approach	Design independent Supports multiple generations

Table 6-1, Behavioral Verification Technology Summary & Benefits

The Soc behavioral model will become part of a virtual prototype for the board design. Since the model can run code, the design can be fully debugged prior to receiving the physical chips. This concurrent engineering will ensure that the board is available when the chip is available in order to accelerate the insertion of this technology into existing systems. BVT will enable the rapid development and application of specification-based validation test suites

CPU Tech has implemented several SoCs utilizing their Behavioral Verification Technology™ (BVT) technology which will be used to develop the BVT itself in Phase III. The BVT would be used in Phase III to verify the compatibility of the SoC with the current H-60 processors.

2) SystemLab™,

CPU Tech has developed a virtual system prototyping environment, for analyzing complex information, architecture evaluation, hardware/software co-design, existing system analysis,

upgrades and enhancements. SystemLab will be used in both the Phase II advanced development and the Phase III implementation programs

6.2 Phase III Implementation Program

The Phase III implementation program would focus on the last three phase of the SoC design process. These phases are:

- Detailed design
- Prototype
- Debug and Verification

The following sections describe our process for generating binary compatible processors using our BVT and SystemLab system development tools and our virtual verification of the processor.

6.2.1 Virtual Verification Process

CPU Tech's virtual specification-based verification/validation tools employed in the methodology offer a competitive advantage. Over 70% of the system development effort is spent in validation. If change activity and recall efforts are included as part of the total development cost, validation cost may be as high as 90% of the total cost of a product. CPU Tech's verification/validation tools allow the operation and observation of processor functions prior to chip fabrication. They enable the generation of virtual system models and analysis of system behavior in critical situations that cannot be readily created on the physical system and apply to the entire processor or system development lifecycle:

CPU Tech uses a virtual system modeling (virtual prototyping) approach to validation, applying behavioral verification tools that confirm the mutual compatibility of the virtual system model, the physical system and the specification. A top-down development strategy using virtual system models and applying BVT also reduces the time-to-market of complex systems and processing components by as much as 40%. Derivative products can be easily architected and validated from the foundation created by the use of this technology.

Using BVT, it is possible to generate a highly structured, methodical, repeatable set of test suites that cost-effectively test the full functionality of processing components to their specifications:

- Each function is checked comparing the results to the expected behavior
- Highly automated testing provides a means to cover all logical possibilities
- Side effects are measured, ensuring that one operation does not cause others to fail
- Ranges of inputs and dependent sequences are tested
- Test programs do not presume a particular hardware implementation
- Tests can be applied to models, simulations or the physical hardware
- Testing is optimized for speed, accuracy, and repeatability, thus providing an excellent debug environment

- Validation suites can be created from written specifications, or inputs can be taken from high level third party behavioral tools
- Automated failure test reports, listing tests performed, with expected and actual results shown

7.0 Acronyms

The following acronyms are used in the report

CP	Computer Processor
EDA	Electronic Design Automation
EMD	Engineering and Manufacturing Development
FCS	Flight Control system
ICD	Interface Control Document
IETM	Interactive Electronic Technical Manual
IFF	Identification Friend or Foe
I/O	Input/Output
LRIP	Low Rate Initial Production
MH	Multi-Mission Helicopter
R&D	Research and Development
ROI	Return on Investment
SoC	System On a Chip
SBIR	Small Business Innovation Research